

Design and characterisation of High-Voltage CMOS (HV-CMOS) detectors for particle physics experiments

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Abstract

As particle searches and physics requirements in high energy particle physics experiments become more sophisticated, particle tracking detectors that are more precise, accurate, and resilient must be developed while remaining cost-effective. One promising candidate for producing future silicon particle tracking detectors is High-Voltage Complementary Metal-Oxide-Semiconductor (HV-CMOS) technology. This technology is emerging within the particle physics community and has been selected for the Mu3e experiment and proposed for use in the upgraded LHCb experiment at the High-Luminosity Large Hadron Collider (HL-LHC) at CERN. Commercialised technologies such as HV-CMOS benefit from a relatively fast, low-cost manufacturing process when compared to bespoke techniques used in the production of the current state-of-the-art hybrid pixel detector modules. Unlike hybrids, detectors fabricated in HV-CMOS technologies implement readout electronics into the same substrate used for particle sensing. Detectors, therefore, require no costly additional assembly and, on top of this, can be very thin, decreasing multiple scattering experienced by traversing particles, for example. In recent years, HV-CMOS pixel detectors have demonstrated excellent radiation tolerance however, there is still room for improvement, as it is currently approximately one order of magnitude lower than that of hybrids. HV-CMOS pixel detectors therefore cannot entirely replace hybrids in the new generation of collider experiments as they are and consequently cannot be used for the inner layers of silicon trackers in future experiments where radiation tolerance requirements are even higher.

One of the ways hybrid detectors mitigate radiation damage effects is by increasing the operating voltage, which is typically much higher than is currently possible with HV-CMOS detectors. Work in this thesis is aimed at increasing the breakdown voltage of HV-CMOS pixel detectors in an effort to increase their operating voltage and, therefore, their radiation tolerance. In this way, it might one day be possible to use the technology to produce particle tracking detectors that exhibit qualities attributed to both hybrid and HV-CMOS detectors: very thin, highly radiation tolerant detectors, with small pixels, and excellent time resolution, that are also relatively inexpensive to produce in very large quantities. In this thesis, a methodology for quickly and accurately recreating HV-CMOS pixels using Technol-

ogy Computer-Aided Design (TCAD) simulations is presented. The resulting TCAD structures were used to aid in the design of the second prototype developed within the CERN RD50 collaboration, RD50-MPW2. Additionally, Edge Transient Current Technique (e-TCT) measurements of backside biased HV-CMOS pixel detectors are presented, which facilitated the development of a new HV-CMOS detector prototype UKRI-MPW0. The simulations and design of UKRI-MPW0 are presented, and measurements of fabricated samples demonstrate a breakdown voltage > 600 V. An irradiation campaign is underway, and a second prototype is planned for submission before the end of the year.

Declaration

I declare that the work presented in this thesis is my own and is the result of my own activities under the supervision of Dr. Eva Vilella (University of Liverpool), Dr. Nicola Massari (FBK), and Prof. Joost Vossebeld (University of Liverpool).

Matthew Franks

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Preface

From a sociological point of view, the study of particle physics has many benefits in our everyday lives. The photon for example, is the elementary particle of the electromagnetic interaction, one of the four fundamental forces along with gravity. Given different energies, the photon can be utilised by us in different ways. Electromagnetic radiation fills our homes with light at night, it cooks our food, and it allows us to communicate with our loved ones on the other side of our planet. At very high energies, photons can be used in the medical field to see into the human body, sterilise medical equipment, and even kill cancer. Other particles are also used in the medical field: while antimatter can sound like science fiction, the antimatter partner of the electron, the positron, can also be used to image the human body in a medical procedure known as Positron Emission Tomography (PET); beams of protons generated by particle accelerators are also used to destroy cancer, in a process called hadron therapy. These last two examples require technologies also developed for particle physics: detectors and particle accelerators. All of the uses described so far come from an understanding of the underlying principles of particles however, general research work can also produce innovations. Tim Berners-Lee invented the World Wide Web (WWW) while working at CERN (European Organisation for Nuclear Research), and it is one of the core components of the internet as we know it today. It is certainly possible that as we attempt to discover new particles and refine our understanding of them, more invaluable technologies could be conceived.

Chapter 1

HV-CMOS in particle physics

1.1 Introduction

This thesis aims to explore methods to improve the performance of High-Voltage Complementary Metal-Oxide-Semiconductor (HV-CMOS) technology as silicon particle tracking detectors for high energy physics experiments, such as those at the Large Hadron Collider (LHC) at CERN. In particular, it will mainly focus on the improvement of radiation tolerance of HV-CMOS detectors through the increase of operating voltage which will be studied using simulations, implemented by designing new detectors, and verified through laboratory measurements.

The outline of this thesis is as follows. This chapter gives an introduction to detectors developed in HV-CMOS technology including a summary of important detector parameters in section 1.1. The motivations behind current particle physics experiments and this work are discussed in section 1.2. A brief overview of current and next generation particle physics experiments is given in section 1.3 including the requirements in terms of detector parameters. In section 1.4, more specific details are given about two experiments, one of which will utilise HV-CMOS detectors and in the other, HV-CMOS detectors are under consideration. Chapter 2 gives details about the physics of silicon detectors and in particular, HV-CMOS detectors, which are necessary for the remainder of the thesis. The current state-of-the-art HV-CMOS, MAPS, and hybrid detectors are also reviewed.

Chapters 3, 4, and 5 present work performed for this thesis. Chapter 3 presents a methodology for simulating HV-CMOS pixels using Technology Computer Aided Design (TCAD). Chapter 4 is a study of issues related to a previously designed detector, and lessons learned are applied to the design of an optimised detector. Chapter 5 focusses on measurements of thinned, backside biased HV-CMOS detectors. A new prototype backside biased detector is also presented, which was designed as a first step towards greatly improving the radiation tolerance of HV-CMOS detectors.

Finally in chapter 6, there is a final discussion, conclusions, and recommendations for future work. A glossary of acronyms and abbreviations is provided at the end of this work.

1.1.1 HV-MAPS

HV-CMOS technology is a manufacturing technique used to construct Integrated Circuits (ICs). It has been available for many decades [1], and is used in the automotive [2] and electronics [3] industries where the high voltage is used in switches to drive devices such as motors and displays. However, it is relatively new within the particle physics community, having only been proposed in 2007 [4] and planned for use in its first experiment, Mu3e in 2013 [5].

In those and the following years, HV-CMOS technology has been used to develop what are known as High-Voltage Monolithic Active Pixel Sensors (HV-MAPS) [6] (see figure 1.1). A *pixel sensor* is a particle sensor that implements a matrix of diodes, known as pixels, into a semiconductor substrate (usually silicon), as opposed to something like columns in strip [7] or 3D sensors [8]. The position of the pixel is used to record the position of impinging particles. In the particle physics field, simply put, an *active* sensor is one that makes use of electronics to amplify and process signals generated by the crossing particles. Processing might include time stamping, for example. The *high voltage* aspect of HV-MAPS is used to increase the size of the pixel diode depletion region (this is expanded on in Chapter 2) compared to regular Monolithic Active Pixel Sensors (MAPS) [9] which are produced in ‘standard’ (low-voltage) CMOS technologies. This ensures particles are detected very quickly and with a high Signal-to-Noise Ratio (SNR). Finally, a *monolithic* detector is one that implements the sensor and electronics in the same IC. This differs from a type of silicon tracking sensor commonly used in high energy physics experiments which are known as hybrid detectors [10]. For particle physics applications, HV-CMOS technology could be very useful because the high voltage aspect should improve the certain detector parameters compared to MAPS, while retaining the benefits of MAPS compared to hybrids.

Hybrid detectors are a combination of an IC produced in standard CMOS technologies and a separate sensing device (this is also expanded on in chapter 2). The two devices are bonded together in a process known as *hybridisation*. These so-called hybrid detectors have been hugely successful in experiments such as ATLAS [11] and CMS [12] at the LHC where radiation tolerance is critical. This is because the sensor and readout chips can be optimised separately for example, tailoring the design of the sensor to achieve high operating voltages, and using smaller technology nodes for the readout chip to increase readout speeds. However, their production requires

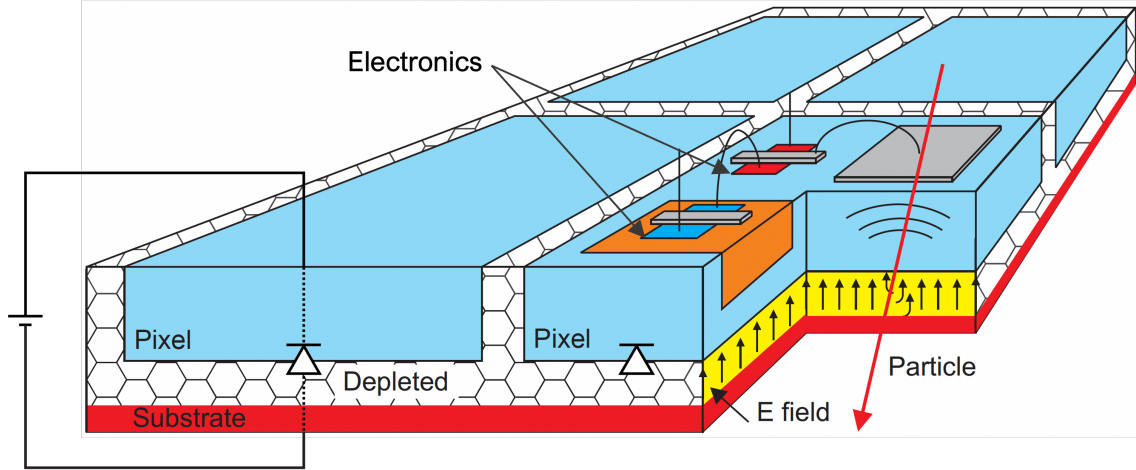


Figure 1.1: Four HV-CMOS pixels. Image is modified from reference [4].

bespoke manufacturing procedures, and is not only time-consuming and expensive, but also introduces superfluous material into experiments. In fact, the authors of reference [10] state that the bonding process could be avoided altogether by integrating the detector into the silicon wafer to form monolithic sensors. Advantages would include reduced multiple Coulomb scattering (due to less detector material) and smaller pixel size, describing what would become MAPS.

MAPS are particle tracking detectors developed in standard CMOS technologies and implement both readout and sensor on the same IC. This is beneficial compared to hybrid detectors as it reduces manufacturing complexity, cost, and detector material. Typically, the sensing element is a partially depleted, thin ($1 - 20, \mu\text{m}$ [13]) epitaxial layer grown on top of the silicon substrate, as in the MIMOSA detector [14] and MAPS used in the STAR experiment [15], for example. A more recent example and another from the LHC, the ALICE experiment [16], has just upgraded its Inner Tracking System (ITS) from hybrid pixel sensors¹ to MAPS technology, which is known as ALPIDE (ALice Pixel DETector) [17]. Due to the benefits of CMOS technology, the so-called ITS2 improves the precision of its particle track reconstruction capabilities by decreasing the size of pixels and reducing the total material budget, compared to the ITS. ALPIDE allows moderate voltages and uses a high resistivity ($> 1000 \Omega \cdot \text{cm}$) epitaxial layer to increase the size of the depletion region. However, while still fairly resistant to radiation damage (no performance degradation seen up to $2.7 \cdot 10^{13} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$), the detectors would be unlikely to withstand prolonged use in high radiation environments such as those at ATLAS and CMS (approximately $2.0 \cdot 10^{16} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$ [18]) and a more radiation tolerant technology (such as hybrid detectors) must be used.

Developing HV-MAPS detectors using HV-CMOS technology is a novel method,

¹and silicon strip and drift sensors

which aims to improve the performance of monolithic sensors. One particular area of interest is increasing the radiation tolerance by making use of high voltages and high resistivity substrates for example, to maximise the size of depletion regions. Typically, for particle detectors developed in HV-CMOS technology, pixels are implemented into the substrate as opposed to a thin epitaxial layer, which allows very large depletion regions to form ensuring more effective and faster charge collection compared to devices fabricated in standard CMOS technologies. In recent years, studies have been conducted to determine if HV-CMOS detectors could survive the harsh challenges imposed by the CERN High-Luminosity LHC (HL-LHC) upgrade [19]. Measurements have shown that the radiation tolerance of HV-CMOS detectors is excellent. In test beam data, HV-CMOS detectors demonstrated hit efficiencies up to 99.7% at fluences up to $1.0 \cdot 10^{15} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$ and 97.6% efficiency at fluences up to $5.0 \cdot 10^{15} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$ [20]. However, the fluences expected over the lifetime of the upgraded ATLAS and CMS experiments, is approximately one order of magnitude higher. Therefore, the experiments have opted for hybrid pixel detectors [18, 21, 22], which demonstrate higher radiation tolerances. HV-CMOS has been proposed for use in the LHCb experiment [23] where radiation tolerance requirements are lower [24]. This would be the first high energy particle collider environment to utilise detectors developed in HV-CMOS technology. More information about this is given at the end of the chapter. A summary of the HV-CMOS detector parameters discussed in this section is given in the next section, and these parameters are compared with the current state-of-the-art MAPS and hybrid detectors.

1.1.2 Summary of detector parameters

The new generation of particle colliders will increase both the energy and the number of collisions to search for new physics which requires increasingly precise particle trackers, in terms of both timing and position. Next generation detectors must reliably extract particle information, interfering as little as possible with the particles themselves, whilst remaining impervious to any damage caused by the high energy particles, and must survive for many years. These criteria can be summarised with the following detector properties:

- High speed: detectors must be fast to detect and analyse multiple particle events.
- High time resolution: arrival time of detected particles must be precisely recorded for accurate particle track reconstruction.
- High granularity: detectors must be able to accurately record the position of a detected particle for track reconstruction. This is given by the size of the

pixel/ $\sqrt{12}$.

- Low material budget: thinner detectors decrease the probability that particles will scatter off detector material and change velocity.
- High radiation tolerance: detectors at accelerators like the LHC must be resilient to accumulated damage caused by high energy particles and radiation to maintain performance.
- Low power consumption: detectors must not consume a lot of power as this determines the amount of cooling required.

Table 1.1 shows values comparing these criteria for HV-CMOS, hybrid detectors, and MAPS particle trackers. All three detector types benefit from the advantages of CMOS technology, meaning detectors can be fast and have high time resolution. However, hybrids and MAPS can be significantly faster due to the use of smaller technology nodes. This combined with a sensor component capable of very high operating voltages, make hybrids suited to the high radiation environments of current particle accelerators. But the requirement of bump bonding also leads to constraints related to cost, detector thickness, and pixel sizes for example. MAPS and HV-CMOS on the other hand, by implementing both CMOS and sensor on the same chip reduce the detector material with respect to hybrids, which can also be further thinned to very small thicknesses. HV-CMOS detectors like hybrids, enable implementation of small pixels but could in theory develop smaller pixels like their standard CMOS counterparts such the ALPIDE detectors in the ALICE experiment ($28\text{ }\mu\text{m} \times 28\text{ }\mu\text{m}$) [25], but this has yet to be demonstrated. For future experiments, development in silicon pixel detectors is ongoing to improve these parameters which is discussed in reference [26]. Specifically, hybrid detector development is focussed on reducing the thickness of detectors and size of pixels, whereas HV-CMOS aim to increase radiation tolerance and increase readout rates.

1.2 Aims and motivations

The general aims of particle physics experiments are to study the nature of particles that make up matter and radiation. Today, this is centred on refining SM parameters and discovering new physics. Recent discoveries such as the top quark and the tau neutrino at Fermilab in 1995 and 2000, and the Higgs boson in 2012 at CERN completed the SM however, there are still many unanswered questions. In terms of undiscovered particles, present day and future experiments are searching for hints of dark matter (DM) and someday possibly gravitons, but also aim to understand imbalances observed in nature, such as the apparent overabundance of matter in the

Table 1.1: Table comparing HV-CMOS, hybrid, and MAPS particle tracker parameters.

Parameter	Unit	HV-CMOS	Hybrid (planar)	MAPS
Speed	Gbit · s ⁻¹	3.75 [*]	5.12 [¶]	5 ^{‡‡}
Time resolution	ns	6.7 [†]	0.2 ^{**}	≥ 2.0 ^{‡‡}
Pixel size	μm ²	50 × 50 [‡]	50 × 50 [¶]	28 × 28 ^{§§}
Detector thickness	μm	50 [‡]	100 + 150 [¶]	50 ^{‡‡}
Radiation tolerance	n _{eq} · cm ⁻²	5.0 · 10 ^{15§}	2.0 · 10 ^{16††}	1.0 · 10 ^{15‡‡}
Power consumption	mW · cm ⁻²	160	700 [¶]	40 ^{§§}

^{*}K. Arndt et al. (2021) [27]. Has three serial links, each running at 1.25 Gbit · s⁻¹

[†]A. Schöning et al. (2020) [6].

[‡]R. Casanova et al. (2018) [28].

[§]M. Benoit et al. (2018) [20] (97.6% efficiency).

^{||}F. Keizer on behalf of the LHCb collaboration (2021) [29].

[¶]ATLAS Collaboration et al. (2018) [30] (1.28 Gbit · s⁻¹ × 4). Detector thickness is sensor + readout.

^{**}X. Llopart et al. (2022) [31].

^{††}(Expected value) D. Contardo (2020) [26].

^{‡‡}H. Pernegger et al. (2021) [32].

^{§§}M. Mager et al. (2016) [25].

universe with respect to antimatter. These phenomena are not described by the SM but can be instead described via theoretical extensions to the SM known as BSM physics, such as supersymmetry for example. In this section the motivation for high energy physics experiments will be briefly introduced to give context and motivation to this thesis.

1.2.1 The Standard Model

The SM of particle physics is a theoretical framework that describes all matter and radiation that surrounds us, as well as the ways that matter and radiation can interact. All experimentally verified fundamental particles of matter and radiation are represented in figure 1.2, which are grouped into two categories: fermions and bosons. Put simply, these are the names given to matter and radiation, respectively. Fermions are further divided into quarks and leptons, the first generation of which are the components of atoms, like the hydrogen in the Sun, or the carbon in our bodies. In the context of particle physics experiments, the SM can be used to predict the likelihood of certain interactions between particles occurring; predictions that have been rigorously tested and confirmed by some of the world's most sophisticated and precise equipment. It is arguably one of the greatest theoretical and experimental scientific achievements to date. However, there is still work to be done. It is known that the SM is not the final theory, as it describes three of the four known

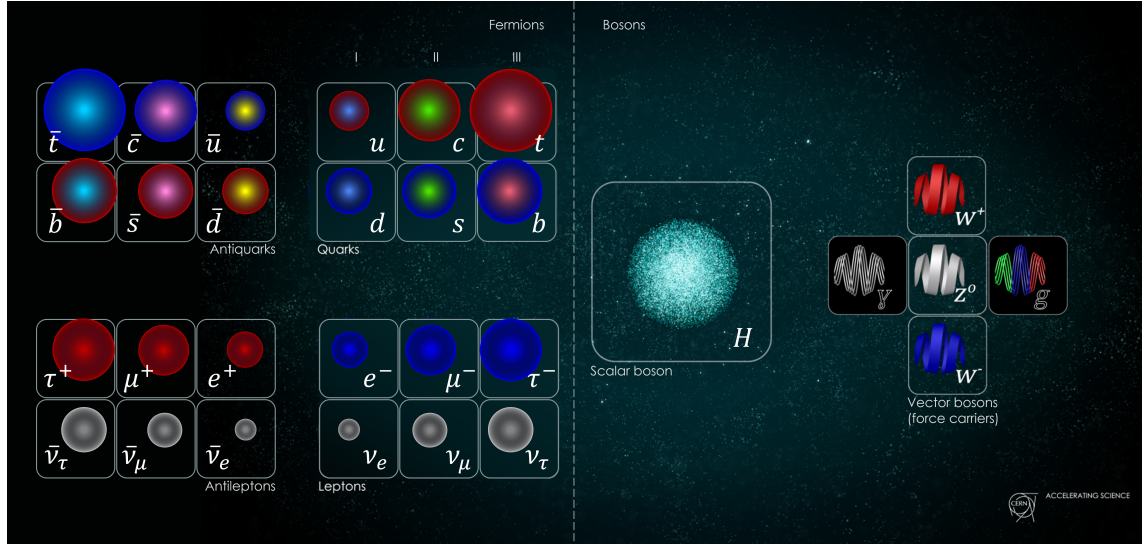


Figure 1.2: Particles of the Standard Model. Fermions are on the left and bosons are on the right. The size of the depicted fermions is approximately related to their mass (in $\text{MeV} \cdot \text{c}^{-2}$). Electromagnetic charge of the particles is shown in red (+) and blue (-). Figure is modified from reference [36].

fundamental forces of nature: the electromagnetic, weak, and strong forces. The best description of gravity, the fourth force, is provided by the theory of general relativity (GR) and so far, efforts are currently ongoing to unite GR with the SM into a theory of everything (ToE) with theoretical frameworks such as string theory [33–35].

To test the SM, physics experiments smash high energy particles into each other (or into stationary targets) in order to produce more particles. Tracking systems around the collision point are designed to detect the secondary particles and record precise position and timing information to reconstruct the particle path or *track*. This information can then be used to identify the secondary particles and determine the interaction that occurred. This is repeated many times and compared to SM predictions. If there are any deviations between the measurements and the theoretical predictions, it could mean that some unknown physics is responsible.

1.2.2 Current Beyond Standard Model (BSM) searches

Despite the successes of the SM, such as predicting the existence of new particles like the Higgs boson [37, 38], we know it is not the final picture, as for example, it does not describe gravity. We observe the effects of gravity around us every day and it is perhaps the most familiar of the fundamental interactions. Why is a theory of all matter and the interactions between them unable to describe something so essential to our everyday experience and understanding? This is an open problem in physics. In addition to this, some other open problems include the very nature of quarks and

leptons. Are quarks and leptons truly fundamental, or are they themselves made of something smaller? Another open problem rests with the number of generations of quarks and leptons. Why are there three generations, for example? There are currently searches for a fourth generation of matter (particles are known as t' , b' , τ' , and ν'_τ). But what mechanism explains the number of generations, and is it limited? Why are there not just one or two generations?

While the direct observation of a graviton, the hypothetical boson of the gravitational interaction, is likely very far off, its presence is nonetheless predicted. Reference [39] states that string theories are the most likely possibility for the underlying theory of particle physics and gravity. String theories postulate that point-like particles are instead described by one-dimensional strings, vibrating in 10- or 11-dimensional spacetime. One of the vibration modes of these strings has the exact properties of a graviton. Every particle in the SM emerges from one of these string vibration modes. These strings are however, theorised to be much too small for current experiments to observe. 10- or 11-dimensional string theories are known as superstring theories and are able to solve many open problems in physics, but many more questions are raised. Where and what are these extra dimensions? Nothing has so far hinted anything outside of our everyday 4-dimensional experience (three spatial and one temporal). Superstring theories also require the existence of another set of particles, counterparts to the SM particles. This is known as *supersymmetry* and the particles are known as the supersymmetric partners to the SM particles. Where are these particles? Experiments at the Large Hadron Collider (LHC) such as ATLAS [11] and CMS [12] are currently searching for extra dimensions and supersymmetric particles but so far, nothing has yet been observed. At the time of writing, the LHC has just emerged from a phase known as Long Shutdown 2 (LS2), a time dedicated to upgrading the machinery and equipment. During the next few years, the machine will operate at an increased energy and luminosity (number of collisions), in a phase known as Run 3 (R3) to further push their searches and attempt to solve some of these problems. This will be expanded upon in the next section.

Supersymmetry also provides what is known as a Lightest Supersymmetric Particle (LSP) for example, which is a candidate for DM. Here emerges another open problem in particle physics, the SM does not describe over 80 % of the matter in the universe. A so far unobserved, new form of matter is hypothesised to make up 84.4 % [40], with the rest attributed to ‘everyday’ (baryonic) matter. Between 0.5 %–1.6 % of dark matter can be attributed to SM neutrinos, but the rest is currently unknown [40]. DM is referred to as ‘dark’ as it does not interact electromagnetically i.e., it does not absorb or emit photons, and is therefore very difficult to detect directly in experiments. Its existence has been inferred from gravitational effects such as gravi-

tational lensing of the bullet cluster [41] and the rotational velocities of galaxies [42], for example. As a side note, according to the recent data from the Planck satellite [43] matter itself also only makes up about 31 % of the total energy density of the universe, with the other 69 % attributed to dark energy (DE), another unknown substance, leaving approximately 95 % of the total energy density of the universe currently undiscovered. A detailed report of everything discussed in this section and more can be found in the 2020 (and 2021 update) of the Review of particle physics by the Particle Data Group [40] along with references therein for further reading.

1.3 High energy particle physics experiments

1.3.1 Present experiments

1.3.1.1 LHC

Particle physics experiments are typically the result of collaboration between institutions from many countries, involving large groups of scientists from all over the world, that span many decades. CERN is the site of the LHC, the largest and highest energy particle accelerator in the world. Underground at the LHC (blue ring in figure 1.3a), protons are accelerated to nearly the speed of light along paths bent into circular shapes by strong magnets. Two beams of protons travel around the tunnels (see figures 1.3b and 1.3c) many times in opposite directions and are eventually brought together into four collision points, which are the locations of four large particle detection experiments: ALICE [16] ATLAS [11], CMS [12], and LHCb [23]. Other experiments at the LHC not shown in figure 1.3a are the FASER [44], LHCf [45], MoEDAL [46], and TOTEM [47] experiments. A detailed review can be found in reference [48]. When two of these very high energy protons collide, many more particles are produced, which are detected and analysed by the experiments positioned around the beam.

An example, used here to demonstrate the layout of a detector, is the CMS detector, which can be seen in figure 1.4a. The experiments consist of many layers of detectors (the CMS example is labelled in figure 1.4b) made from many different specialist materials. Starting from the outside, the muon chambers are gaseous, the hadronic calorimeter is a brass-scintillator, and the electromagnetic calorimeter is made of lead-tungstate scintillating-crystals. The central detector, closest to the beamline, is made of strip trackers and pixel detectors which are composed entirely of silicon [12]. It is the silicon pixel detectors placed close to the beamline that are the focus of this thesis. Experiments combine many different types of detectors as they are each sensitive to different particle types and help distinguish them. The details of other detector types go beyond the scope of this thesis, but electromag-

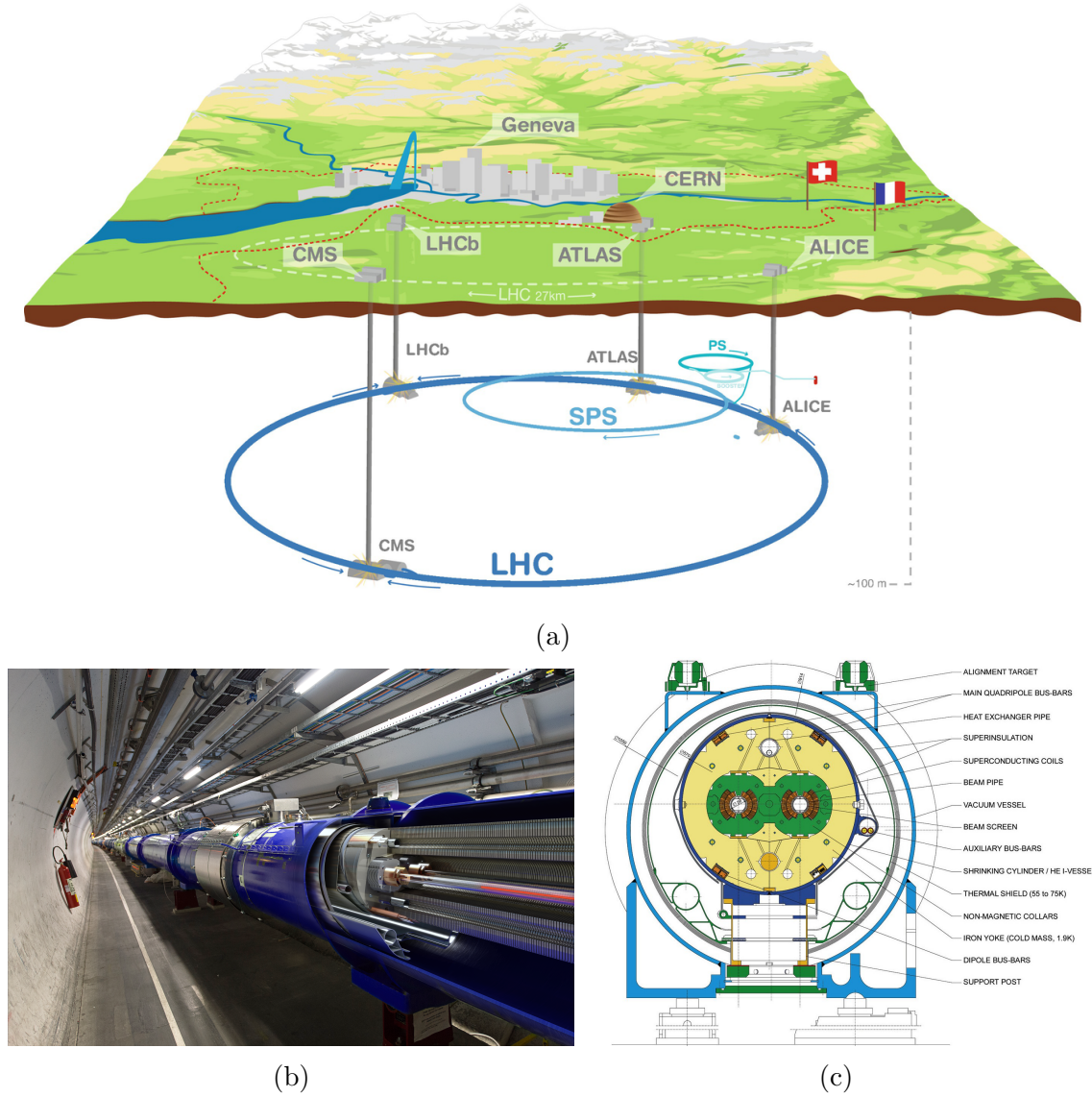


Figure 1.3: (a) Diagram of the Large Hadron Collider (LHC) underground at the CERN site showing the locations of the four biggest experiments, ALICE, ATLAS, CMS, and LHCb. Experiments that are not shown include FASER, LHCf, MoEDAL, and TOTEM. Image credit: CERN. (b) Photo of the LHC tunnel with a superimposed 3D render of the dipole [49]. (c) Cross-section diagram of the LHC dipole magnet [36].

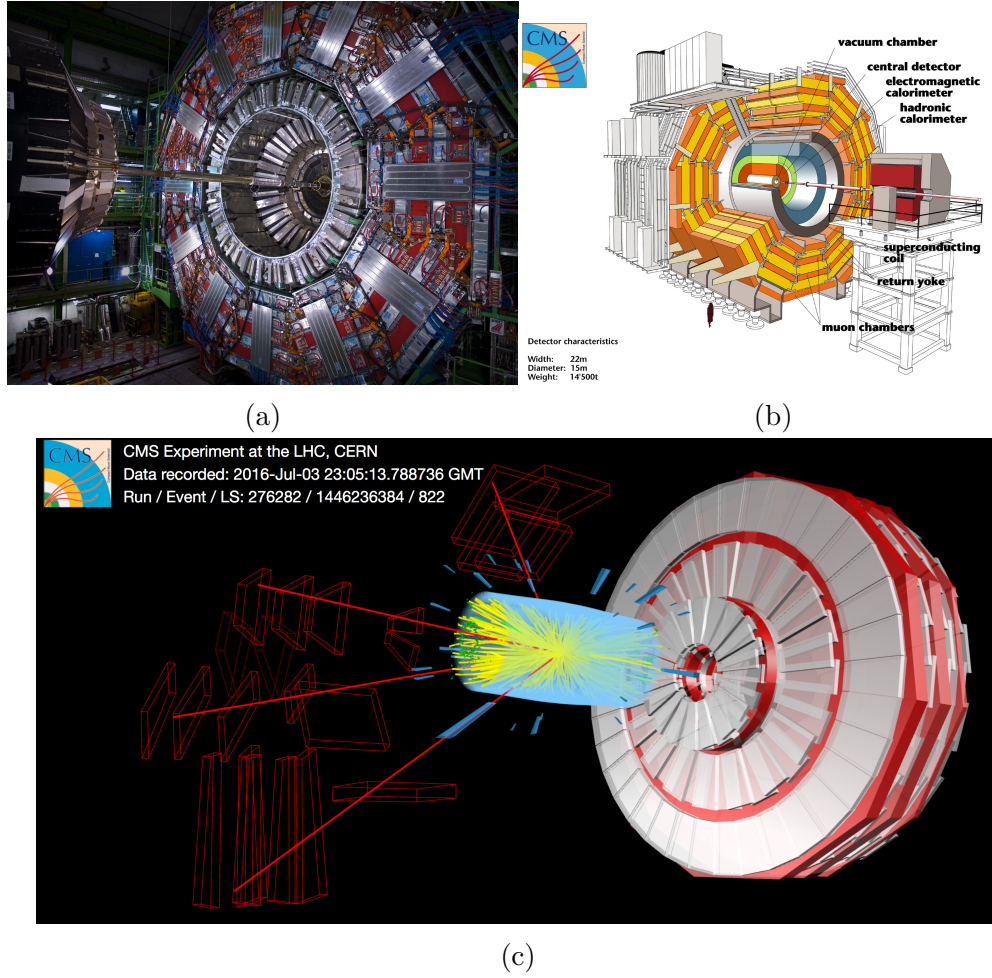


Figure 1.4: An example of a particle detection experiment at the LHC. (a) A photo of the CMS detector. (b) A diagram of the CMS detector. (c) Reconstructed track of a particle detection event at CMS. Credit: CERN [50].

netic and hadronic calorimeters for example, are usually placed in the outermost regions and serve to distinguish between charged and neutral hadrons respectively. Charged pions, common decay products, are hadrons and will make tracks in both the electromagnetic and hadronic calorimeters. Muons are not hadrons but carry negative charge and would therefore not make tracks in the hadronic calorimeter but would in the electromagnetic. Both muons and pions are visible to silicon detectors, which then aid in accurately reconstructing particle tracks close to the original interaction point. Figure 1.4c shows an example of two Z^0 boson decays, reconstructed from four muon tracks (thick red lines) using detections in the segments of the outer layers (hollow red shapes).

Constructing the central part of detectors from silicon is quite typical for experiments such as this as it exhibits properties excellently suited to these conditions. According to reference [12], during the operation of the LHC, an average of 1000 particles were produced every 25 ns (bunch crossing time). Therefore, the inner layers

require high granularity to distinguish individual particles, must be able to detect particles quickly, use less material to limit particle scattering, and be resilient to the damage that traversing high energy particles can cause. Silicon satisfies all these criteria. When combined with CMOS technology, silicon also provides the ability to make fast readout electronics that can perform additional functions on-chip such as signal amplification, storage of detection timing information, and discarding of ‘unimportant’ events using discriminators or comparators, providing both very accurate position and timing information. At present, most of the silicon pixel detectors in these experiments are what are known as *hybrid* detectors. These detectors have been used in physics experiments for many years [10, 51, 52] and have been very successful but also have their downsides. They are quite expensive and time-consuming to produce. This is something that can be solved by using commercial CMOS or HV-CMOS technology. However, it has not yet been demonstrated that CMOS, especially HV-CMOS detectors can function in high radiation environments such as those in the previously discussed CMS experiment. A more specific comparison between standard CMOS, HV-CMOS detectors and hybrids is given in the next chapter.

At the time of writing (end of 2022), the LHC has entered a the R3 phase. After 3 years in LS2, the LHC has upgraded its machinery and equipment to increase the collision energy of beams from 13 TeV to 14 TeV and increase the integrated luminosity by approximately a factor of 2 from 190 fb^{-1} to 350 fb^{-1} with respect to Run 2 (R2). A timeline of the LHC plan can be seen in figure 1.5. From the perspective of silicon detectors, many more particles will be produced in interactions, which means detectors will need to be smaller, faster, and more resilient. Detectors have been upgraded accordingly, with features such as decreased detector material to allow low transverse momentum tracking [17], reduced pixels sizes [17, 53], higher radiation tolerances [54, 55], replaceable innermost layers for very high radiation regions [55], and thinner sensors to increase charge collection efficiency [56].

1.3.2 Near-future experiments

1.3.2.1 HL-LHC

The next stage in the LHC lifetime is the High Luminosity LHC (HL-LHC) [19], which aims to further increase the integrated luminosity by almost a factor of 10 with respect to the R3 LHC. This introduces many challenges, especially for detectors. Going to higher energies and luminosities means detectors will need to be faster, more accurate, and more resilient to radiation damage. R&D to improve silicon detectors is already underway. An example in the context of this thesis is the new proposed detector for the LHCb experiment the Mighty Tracker [24] which could



Figure 1.5: LHC/HL-LHC plan (last update February 2022) [57].

utilise HV-CMOS detectors and would be one of the first experiments in a high energy collider environment to make use of HV-CMOS technology.

The LHC is already the highest energy particle collider in the world and after the HL-LHC upgrade ready for Run 4 (R4), could be for the next 20 years [19]. By increasing the luminosity, there will be a larger number of collision events and therefore an increase in statistics, a very important parameter needed to distinguish rare particle interactions from strong backgrounds of more common interactions. The HL-LHC is therefore discussed here as it represents a very challenging environment for silicon detectors. The increased number of events means detectors will need to withstand the radiation damage caused by the additional particle flux. To do this, the ATLAS and CMS experiments for example, will make use of silicon hybrid detectors just like in R3. ATLAS for example, will replace its Inner Detector (ID) [58] with the new Inner Tracker (ITk). This will be composed of hybrid detector modules where sensors will be a combination of strips [21] and very small pixels ($50 \mu\text{m} \times 50 \mu\text{m}$) [18] qualified to operate in very high radiation environments. This is however not quite high enough for the expected accumulated radiation levels and detectors will be replaced partway through the lifetime of the HL-LHC. In the CMS experiment, where the radiation tolerance requirements are similar [22], its Inner Tracker (IT) will also be made entirely of hybrid pixel detectors with small pixels ($50 \mu\text{m} \times 50 \mu\text{m}$ or $25 \mu\text{m} \times 100 \mu\text{m}$).

Where the radiation tolerance requirements are lower, the ALICE and LHCb experiments will explore the use of sensor technologies based on CMOS [59] and HV-CMOS [24], respectively. These will be discussed more in the next chapter, but the use of CMOS technologies in ALICE for example, allows for very small pixels ($15 \mu\text{m} \times 15 \mu\text{m}$) and a total sensor thickness of 20–40 μm which represents a significant reduction compared with detectors an order of magnitude thicker in ATLAS and CMS. In the LHCb experiment, the proposed Mighty Tracker will use a combi-

nation of scintillating fibres and HV-CMOS. The scintillating fibres will cover a large area, and where higher radiation tolerance, high granularity, material thickness, and accurate timing are the main considerations will make use of HV-CMOS. The sensors in these experiments have not been qualified to operate in the highest radiation levels expected at ATLAS and CMS. Nevertheless, HV-CMOS detectors exhibit many properties that can improve the performance of experiments. Therefore, one of the aims of this thesis will be to identify techniques used in hybrid technology that make them radiation tolerant and apply these to HV-CMOS technology to have all the advantages that both technologies offer.

However, the HL-LHC is far from the ultimate goal of particle physics experiments. There are already plans to explore the energy ranges far beyond those achieved at the LHC already. Of course, this means detector technology will also continue to be pushed beyond today's accomplishments.

1.3.3 Far-future experiments

1.3.3.1 FCC

Looking beyond the HL-LHC, the Future Circular Collider (FCC) program is the future generation of colliders at the CERN site. The FCC collaboration aims to increase the energy of collisions by a factor of 7 with respect to the HL-LHC to 100 TeV, in order to discover physics beyond the SM and precisely measure SM parameters [60]. This higher energy will require improvements in detector technology never before seen in terms of low mass, low power, high granularity, time resolution and radiation tolerance, something which could be provided by future HV-CMOS detectors.

The FCC project will begin with construction of a 100 km tunnel at the CERN site and the upgrade is planned in two stages: the FCC-ee which could be operational by 2039 at the end of the HL-LHC, and the FCC-hh starting in 2050–2060 [61]. FCC-ee is an e^-e^+ collider designed as a so-called Higgs and electroweak factory to study Z, W and Higgs bosons as well as top quarks [62]. The FCC-hh is a 100 TeV proton-proton collider which is planned to be built into the same tunnel allowing for ee, hh, or eh collisions. At these energies, the authors of reference [61] state that many more Higgs particles can be produced compared to the LHC, allowing them to be studied in more detail. In addition, particles with masses of a few TeV can be produced, including DM candidates such as the *wino* [60].

Like the LHC, four detector points are planned around the beamline, two high and two low luminosity. Reference [60] provides details of an example FCC-hh detector, which features a central tracker likely to be made from silicon (see figure 1.6a). Based on the larger number of collisions per bunch crossing and increased

luminosity (see table 1.2), a silicon layer at a radius of 2.5 cm would receive a neutron equivalent fluence of $8.0 \cdot 10^{17} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$ (figure 1.6b) and a total ionising dose of around 270 MGy (figure 1.6c), verified in the study by FLUKA [63] simulations. This is almost two orders of magnitude higher than even the most radiation tolerant silicon detectors are designed to withstand and presents a significant challenge for designers. Design, fabrication, and testing of new chip iterations can take around 12 months so it is not too early to begin considering these numbers when designing new detectors.

Table 1.2: Table comparing LHC, HL-LHC, and two phases of the FCC parameters (adapted from reference [64]).

Parameter	Unit	LHC	HL-LHC	FCC	
Collision energy	TeV	14	14	100	
Circumference	km	27	27	100	
Bunch spacing	ns	25	25	25	25*
Luminosity	$10^{34} \text{ cm}^{-2} \text{ s}^{-1}$	1	5	5	30 [†]
Events	bunch crossing ⁻¹	27	135	170	1000 [†]
NIEL	$\text{n}_{\text{eq}} \cdot \text{cm}^{-2}$	$3.6 \cdot 10^{15\ddagger}$	$2.0 \cdot 10^{16\S}$	$8.0 \cdot 10^{17*}$	

*M. Benedikt et al. (2018) [60]

[†]F. Zimmermann et al. (2020) [62].

[‡]W. Adam et al (2021) [55].

[§]ATLAS Collaboration et al. (2017) [18].

1.4 HV-CMOS in experiments

1.4.1 Mu3e

The Mu3e experiment at the Paul Scherrer Institut (PSI) [5] will be the first experiment to utilise sensors developed in HV-CMOS technology [65]. HV-CMOS technology was chosen specifically because a critical aspect of the experiment is that there must be minimal detector material in order to reduce multiple scattering of particle decay products and maximise the momentum resolution. Standard CMOS also fulfils this requirement, but a timing resolution better than 20 ns is also required [65] so HV-CMOS technology was chosen as the high voltage can be used to create large depletion regions in the substrate and ensure fast charge collection [66].

The experiment will search for Charged Lepton Flavour Violation (CLFV) via the decay of an antimuon into two positrons and an electron $\mu \rightarrow e^+e^-e^+$ [67], a detection that would be an indication of so far undiscovered physics. In this decay, the number of muonic and electronic leptons before and after the decay is not conserved, quantities which should be according to the SM. LFV has been observed

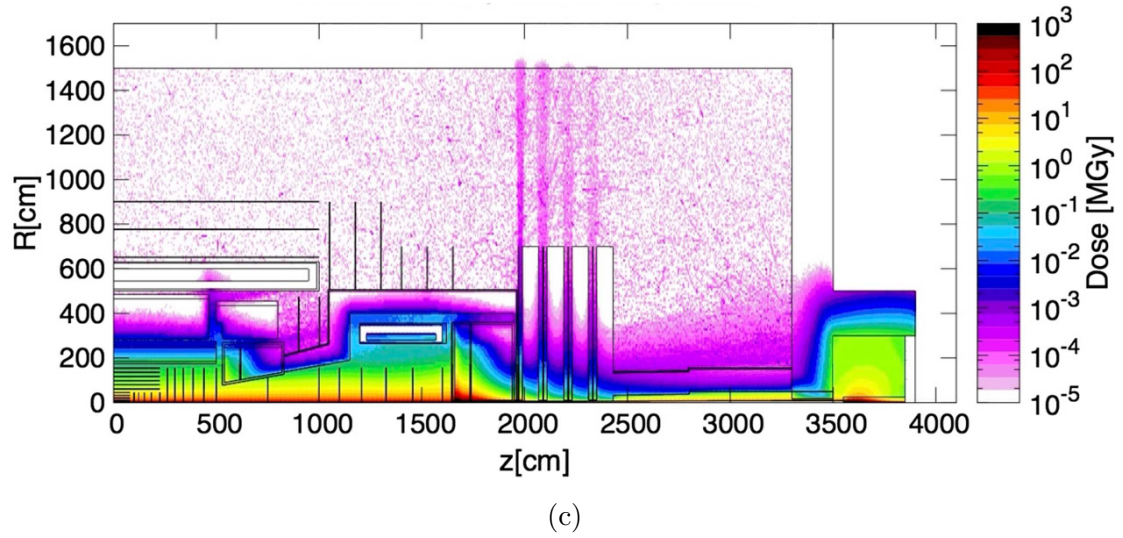
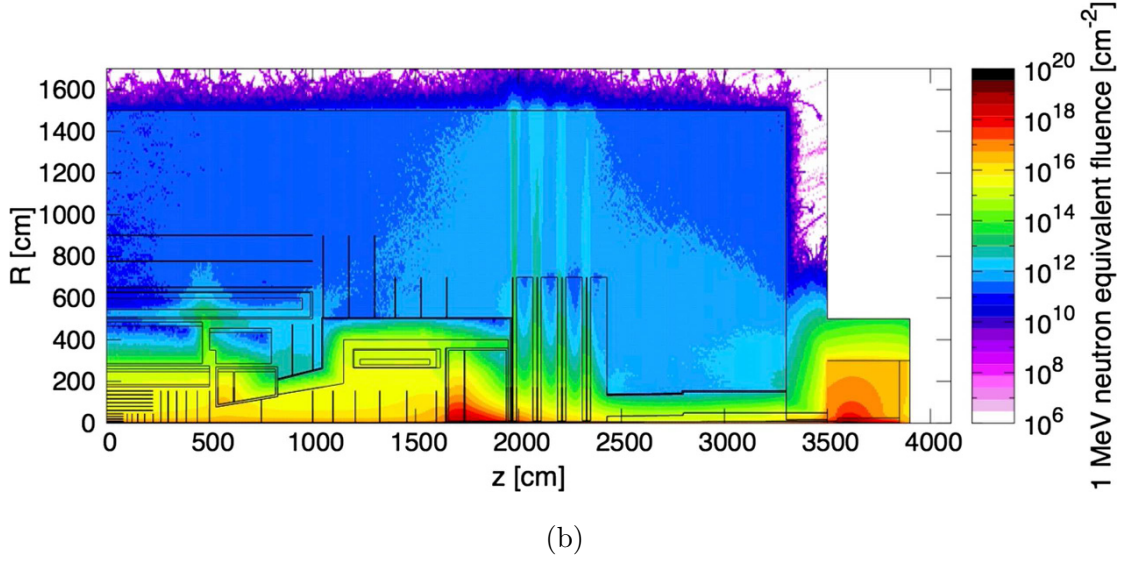
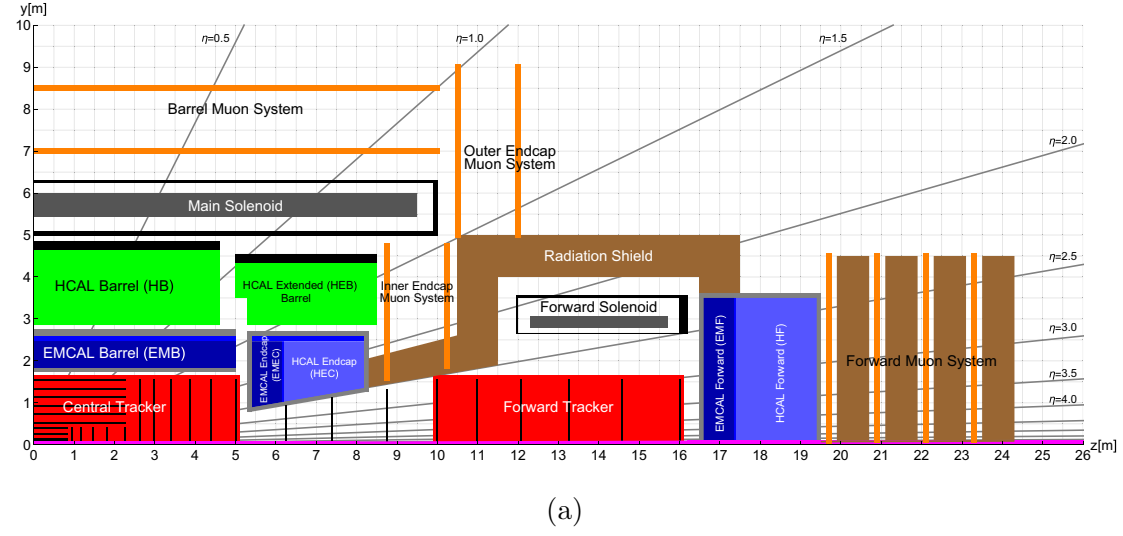


Figure 1.6: (a) Cross-section diagram of the FCC reference detector. (b) FLUKA simulations of NIEL radiation damage to the reference detector. (c) FLUKA simulations of TID radiation damage. All images from reference [60].

to occur in neutrinos, which are able to change flavour via neutrino oscillations but LFV has never been observed for the charged leptons. According to reference [5] this decay can occur via neutrino oscillation (figure 1.7b) but is heavily suppressed and therefore unobservable. Any detection of this decay would therefore be a strong suggestion of new physics. Supersymmetric models [68] for example, predict this decay at a much higher, observable rate (see figure 1.7c).

Experimental detections are expected to be dominated by a background produced by a similar decay $\mu^+ \rightarrow e^+e^-e^+\bar{\nu}_\mu\nu_e$, where lepton flavour is conserved through the production of neutrinos. Neutrinos are invisible to detectors, and therefore this interaction is almost indistinguishable however, the existence of the neutrinos can be inferred through a measurement of missing energy. For this reason, minimal detector material is required to reduce multiple scattering of decay products and reduce the position uncertainty of detections for very precise track reconstruction (figures 1.7d and 1.7e). This will be achieved through the use of HV-CMOS, which integrate readout electronics and the sensitive element into the same chip, which cuts the amount of detector material with respect to hybrid silicon detectors for example. Detectors in the experiment will be thinned to $50\text{ }\mu\text{m}$, with more specific details given in the next chapter.

1.4.2 LHCb

The LHCb experiment sits at one of the four main detector points around the LHC. It was built to study rare decays of bottom and charm hadrons (the b in LHCb stands for *beauty*, another name for the bottom quark) and aims to understand why the universe contains more matter than antimatter. In R3 of the LHC, the proposed upgrade to the Mighty Tracker for LHCb experiment makes use of HV-CMOS detectors, which would make the LHCb the first high energy collider experiment to utilise detectors fabricated in HV-CMOS technology.

A diagram of the LHCb Phase-II detector is shown in figure 1.8a, with the Upstream Tracker (UT) on the left and downstream on the right side of the magnet. HV-CMOS detectors are proposed for use in the so-called SciFi & Silicon Tracker, part of the downstream, which is made of three stations T1, T2, and T3. Each station covers an area of 30 m^2 and is composed of four layers of detectors each. Each layer is split into three sections, the Outer, Middle, and Inner Trackers (OT, MT, and IT). Upgrade of the OT was completed during LS2 (beginning 2019) in preparation for operation in R3, currently scheduled to begin some time in 2022.

The MT and IT, dubbed the MlghTy tracker is to be made entirely of HV-CMOS detectors, and will be upgraded in two stages, the IT first in LS3 and the MT in LS4. A cross-section of one layer is shown in figure 1.8b. The physics case

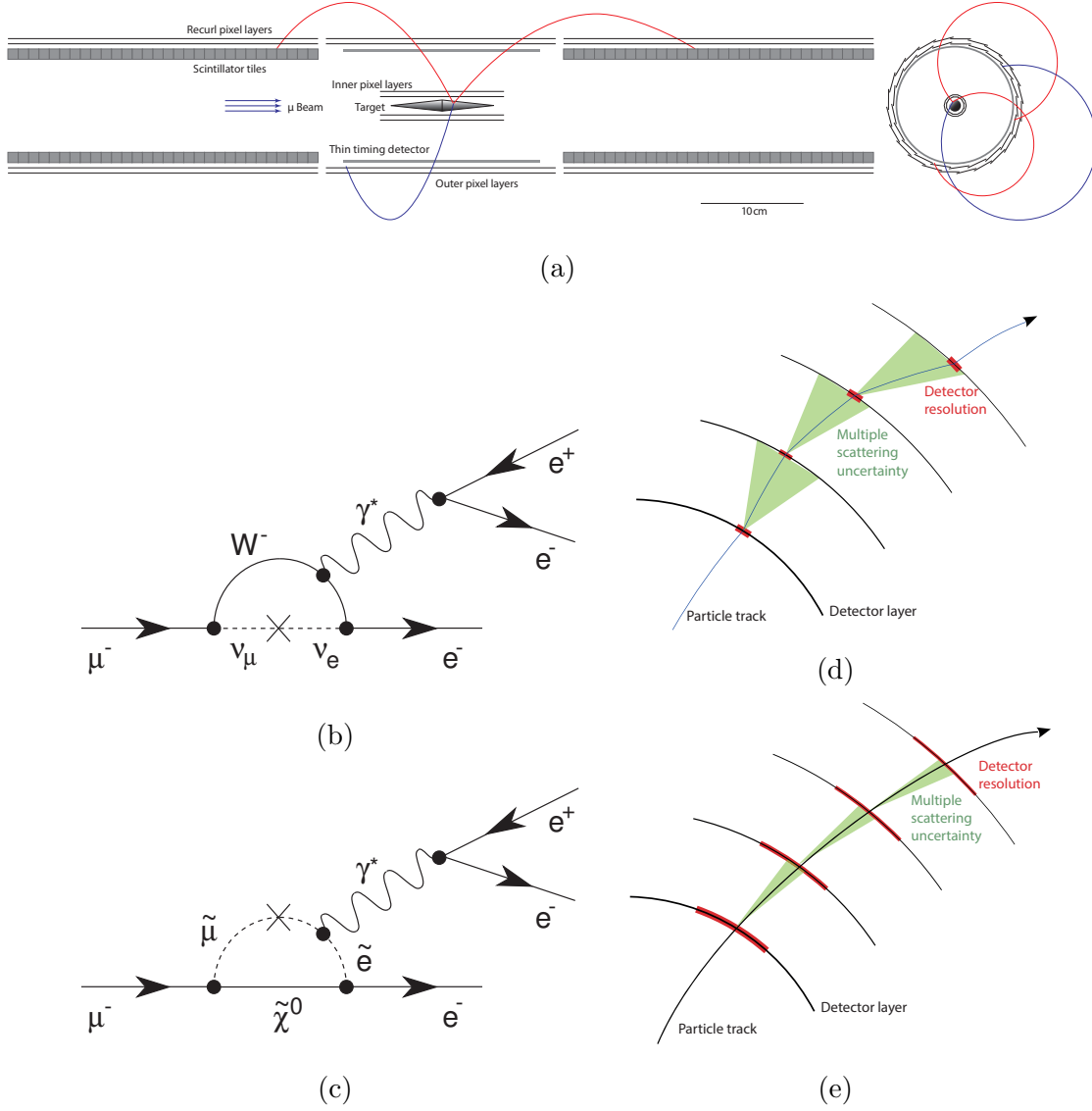


Figure 1.7: (a) Diagram of Mu3e detector. (b) Feynman diagram for the $\mu \rightarrow eee$ process via neutrino oscillation [5]. (c) Diagram for lepton flavour violation involving supersymmetric particles [5]. (d) Particle tracking in scattering dominated regime [67]. (e) Particle tracking in the spatial resolution dominated regime [67].

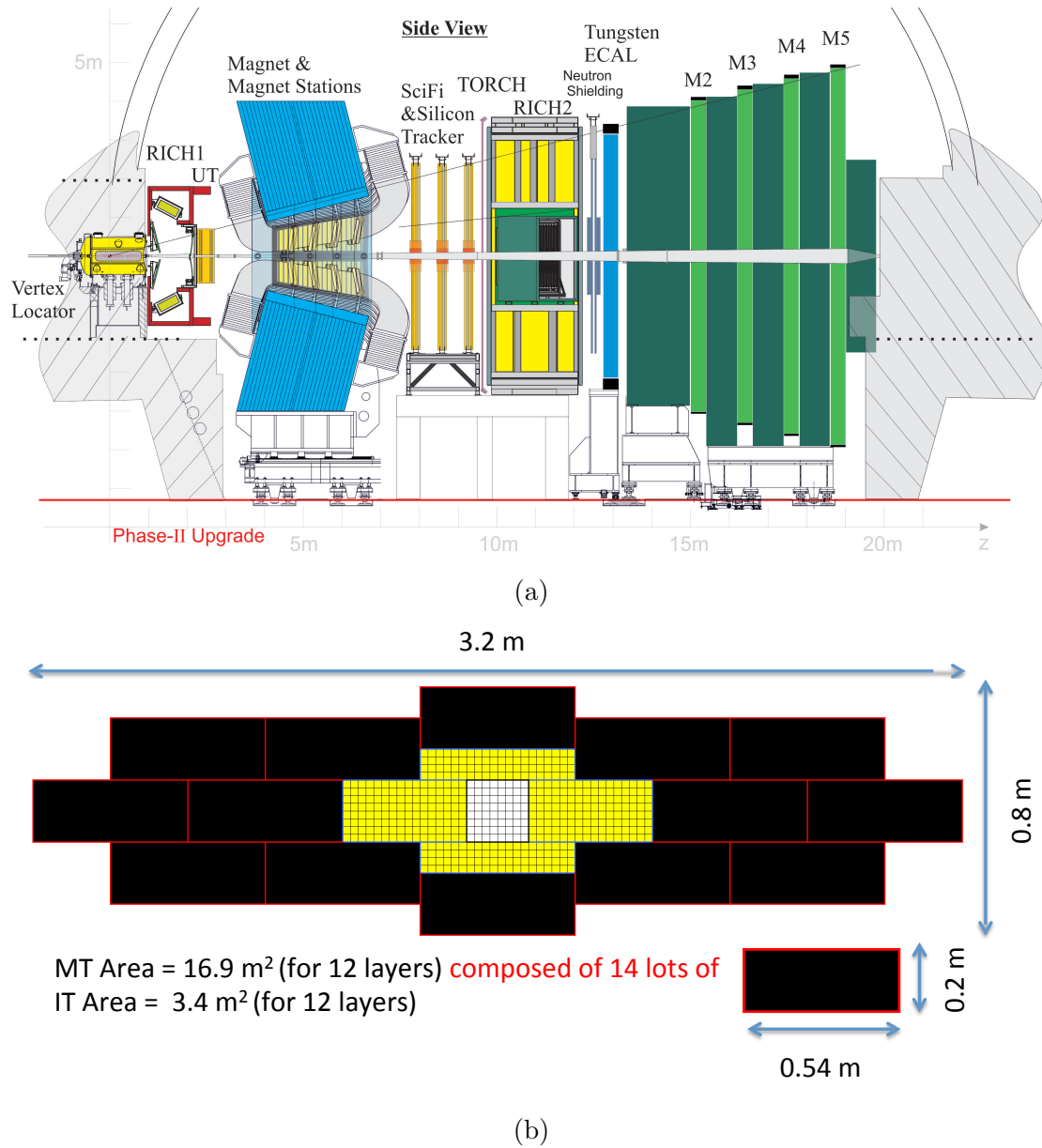


Figure 1.8: (a) Diagram of LHCb Phase-II detector upgrade. (b) Diagram of one layer of Silicon Tracker, Middle Tracker and IT Inner Tracker (IT).

for the experiment was published in 2019 [69] in order to outline its motivations and align some of the requirements for detectors. With the increase in luminosity of the LHC, the mean number of collisions will increase, producing many more particles. From the point of view of detectors, many more particles leads to increased occupancy and therefore the granularity of detectors must be increased. In addition, for accurate matching between upstream and downstream tracks, detector material must be minimised and timing information provided.

HV-CMOS technology was therefore proposed due to the fact that small pixels can be implemented, which could include time stamping electronics on the same chip, therefore reducing the total amount of material. Additionally it was chosen for its low production cost compared to hybrid detectors, and fast turnaround times [24]. As there are 12 layers in total, the T-stations require 20 m^2 of silicon [70]. Radiation tolerance studies also presented in the document demonstrate that HV-CMOS technologies have already been characterised to work by the Mu3e and ATLAS collaborations beyond the requirements of this experiment. Reference [70] also mentions that the maximum integrated fluence at the UT will be $3 \cdot 10^{15} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$ which may also be achievable with HV-CMOS technology.

The next chapter will discuss the Mu3e and LHCb HV-CMOS pixel detectors in more detail, and compare them with MAPS and hybrid detectors. Particular attention will be paid to how radiation damage affects HV-CMOS detectors, which is not a problem in the Mu3e experiment, but is of utmost importance when considering HV-CMOS for future high energy physics experiments such as the LHCb, and maybe even experiments at the FCC.

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Chapter 2

Physics of silicon particle detectors

2.1 Introduction

In the previous chapter, the current status of particle tracking detectors fabricated using HV-CMOS technology was explored. The properties that make silicon detectors uniquely suited to the inner layers of high energy physics experiments were discussed, along with the motivations for improving existing detectors, and the goals of future particle physics experiments. On the topic of future experiments, a brief summary of how HV-CMOS technology is currently being used to develop detectors for the Mu3e experiment was given, in addition to the plans for its use in the LHCb experiment at CERN.

This chapter goes into more detail about the physics of HV-CMOS particle tracking detectors. Section 2.1 covers the fundamental concepts related to the physics of silicon, important CMOS fabrication processes, and the way that high energy particles and radiation damage the structure of detectors, therefore degrading their performance. In section 2.2, more information about the internal structure of HV-CMOS technology is given, how devices fabricated in HV-CMOS technologies function as particle and radiation detectors, and some experimental results characterising the performance of HV-CMOS detectors after radiation damage. Finally in section 2.3, a review of some state-of-the-art HV-CMOS, standard CMOS, and hybrid silicon detectors is given to quantify the status of important parameters such as pixel size and radiation tolerance across multiple technologies.

2.1.1 Silicon substrate

The performance of a detector depends on the purity and regularity of the silicon substrate. The performance of a p-type substrate for example can be increased by carefully controlling the amount of p-type dopant intentionally added to the substrate. Using a low concentration gives a high resistivity and large depletion

regions can be created at relatively low substrate bias voltages to maximise particle detection signals. It was also shown that radiation tolerance can be increased by oxygenating both p-type and n-type substrates [1]. However, the original silicon lattice must be free of defects for optimal performance. Defects refer to irregularities in the highly ordered crystal, which can be introduced naturally during the growth of the crystal, through necessary mechanical processing (e.g., cutting, dicing, lapping, polishing etc.), or lattice atoms can be displaced by the very radiation they are built to detect. Damage to the substrate can cause macroscopic effects such as increase in leakage current, changes in the effective doping concentration, and decrease in charge collection which will be expanded upon in section 2.2.3. The types of defects that can be found in the bulk and how they can affect detector performance will be discussed in this section.

2.1.1.1 Lattice structure

Silicon is a group IV (sometimes known as carbon group or group 14) element and for a basic explanation of lattice structure, the Bohr model of the atom is sufficient. In the Bohr model, electrons in an isolated atom occupy distinct energy levels or shells. Group IV elements have four electrons in their outer shell (see figure 2.1a) which are known as valence electrons. These four electrons can be shared with four other atoms (which in turn share their valence electrons) to form covalent bonds, filling all outer shells with eight electrons (see figure 2.1b). At low temperatures, a crystal of pure silicon is an insulator, but given enough thermal energy, the valence electrons can be liberated and are free to move around the lattice, resulting in electrical conduction.

2.1.1.2 Doping

For electronics applications, silicon is doped with group III and group V elements intentionally to increase the conductivity. Group V elements such as phosphorus, contain five valence electrons in their outer shell. Once introduced, the additional electron is free for electrical conduction at temperatures higher than 0 K (see figure 2.2a). This leaves behind a positively charged ion within the lattice which is known as a *donor* atom, as it has donated an electron. Silicon doped with a group V element is known as *n-type* silicon, as the majority of charge carriers are negatively charged electrons.

However, for most HV-CMOS applications, p-type silicon is used. Elements from group III, such as boron, have three electrons in their outer shell. If a group III element is introduced into the lattice, one bond remains open for free electrons from the lattice to occupy. This is known as a *hole* (see figure 2.2), a quasiparticle

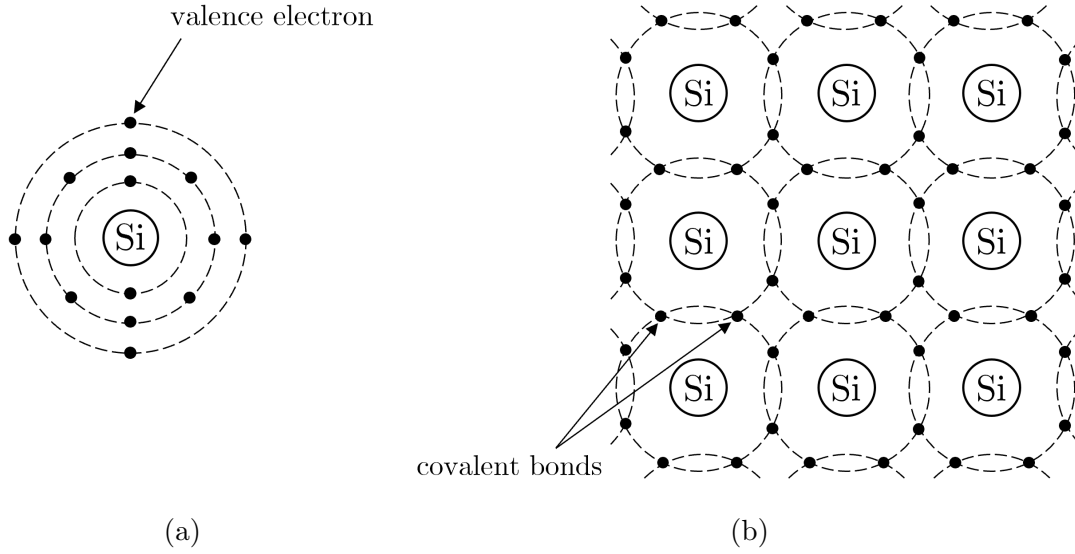


Figure 2.1: (a) Bohr model of an atom of silicon. There are four electrons in the outermost or *valence* shell. (b) 2D diagram of pure silicon crystal lattice structure showing only the valence shells. Each atom of silicon shares one of its valence electrons with each of its four neighbours.

that is free to move throughout the lattice by the successive creation of new holes when electrons move to fill them. Once the outer shell of the boron dopant is filled, a negatively charged ion is formed. Dopants from group III are therefore called *acceptor* atoms, as they accept electrons from the lattice. As holes are the absence of an electron, they are said to be positively charged. Since the majority charge carriers of silicon doped with group III elements are positively charged holes, the material is known as *p-type* silicon.

2.1.1.3 Band diagrams

This can also be described using band theory, which is useful to describe other properties such as radiation damage. To begin, the Bohr model in figure 2.1a is a simplified structure of the atom. In reality, each electron shell is split into *orbitals*. For silicon the actual structure of electrons in the atom is represented using the notation: $1s^2 2s^2 2p^6 3s^2 3p^2$ (see the right of figure 2.3), where the large number is the shell number, the letters are the names given to the orbitals (s is the first, p is the second), and the superscript number is the number of electrons in that orbital. The final two: 3s and 3p are the valence orbitals, which each contain two electrons for a total of four.

When a large number N of silicon atoms are brought together into a lattice (i.e. as the distance between atoms decreases to the lattice spacing a , figure 2.3), the valence orbitals arrange themselves into energy *bands* known as the *valence band* and the *conduction band*. This is because electrons are fermions and are unable to

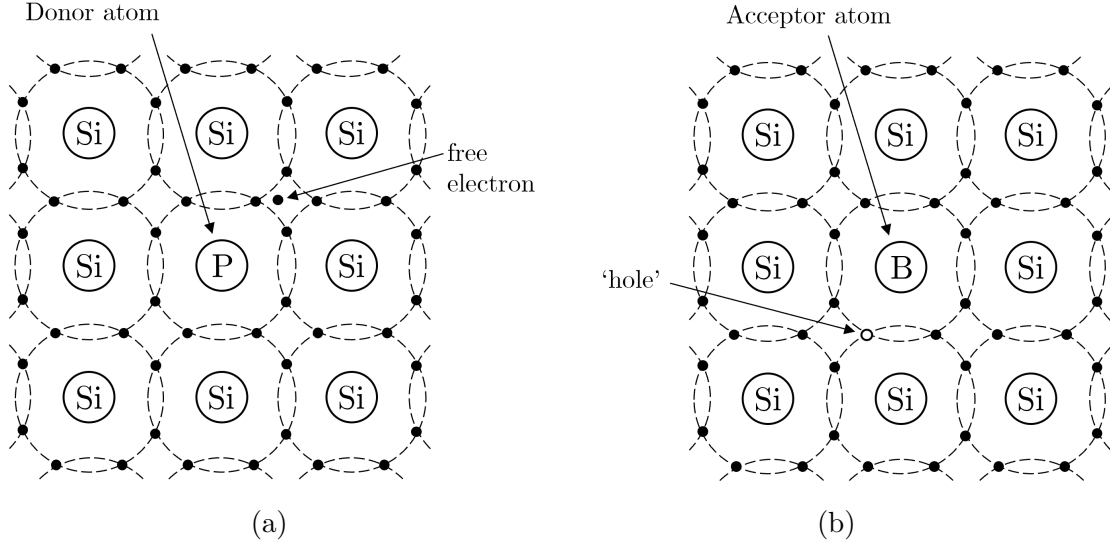


Figure 2.2: (a) 2D diagram of a phosphorus donor atom in a silicon crystal lattice showing only the valence shells. One of the electrons in the valence shell of the phosphorus atom is donated to the lattice. (b) Boron acceptor atom in a silicon crystal lattice showing only the valence shells. As boron atoms only contain three electrons in their valence shells, one bond remains free, which is known as a hole.

share the energy state of electrons in the shells of neighbouring atoms due to the Pauli exclusion principle. The energy levels of the electrons are packed so tightly together ($\Delta E = 1/N$) that they can almost be thought of as continuous band of available energies (left of figure 2.3) where E_V is the highest energy state in the valence band, E_C is the lowest energy state in the conduction band. E_g is the band gap energy, or the difference between the conduction band and valence band energies $E_C - E_V$. E_F is the Fermi level which is the hypothetical energy level in the bandgap which has a 50% probability of being occupied by an electron.

At low temperatures ($T = 0\text{ K}$) valence electrons are constrained to the lattice and occupy the valence band. There are no free electrons in the conduction band as E_g is too large and therefore, electronic conduction is not possible. When there is enough thermal energy (for example, at room temperature), electrons are able to jump from the valence band to the conduction band (figure 2.4a). Electrons are therefore free to move about the lattice and conduction is possible (occupying conduction band energy states). An electron transitioning between the valence band to the conduction band also creates a hole in the valence band. This process of electron-hole pair production is known as carrier *generation*. The reverse of this process is known as carrier *recombination*.

When dopants are introduced, energy levels or states are added into the band gap. For a group V element, the state is said to be a donor type and exists at an energy level E_D very close to the conduction band ($E_C - E_D = 0.045\text{ eV}$ [2]). Donated charge carriers are able to easily jump into the conduction band and conduct electricity

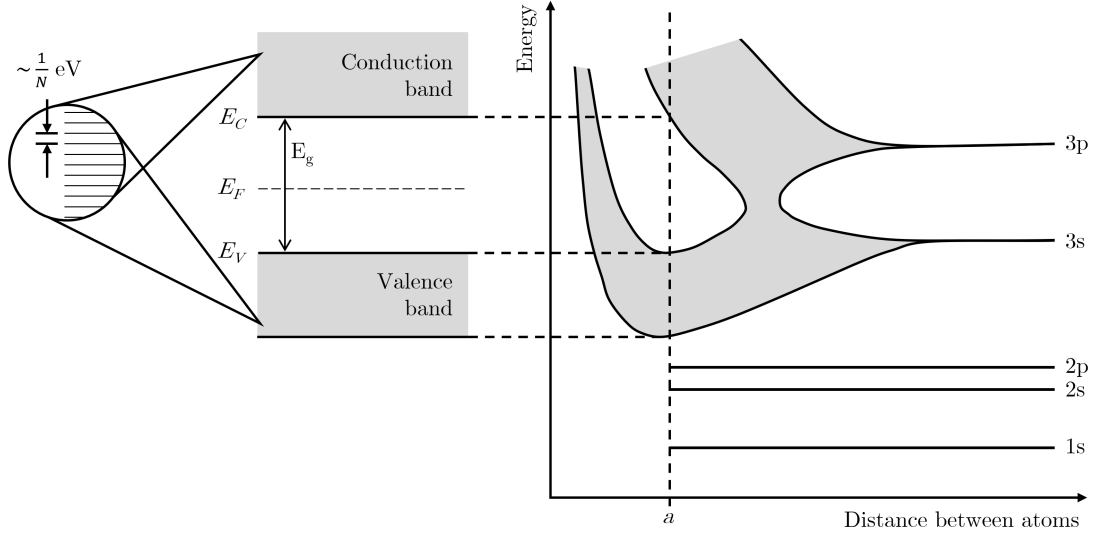


Figure 2.3: Valence and conduction bands of a silicon lattice.

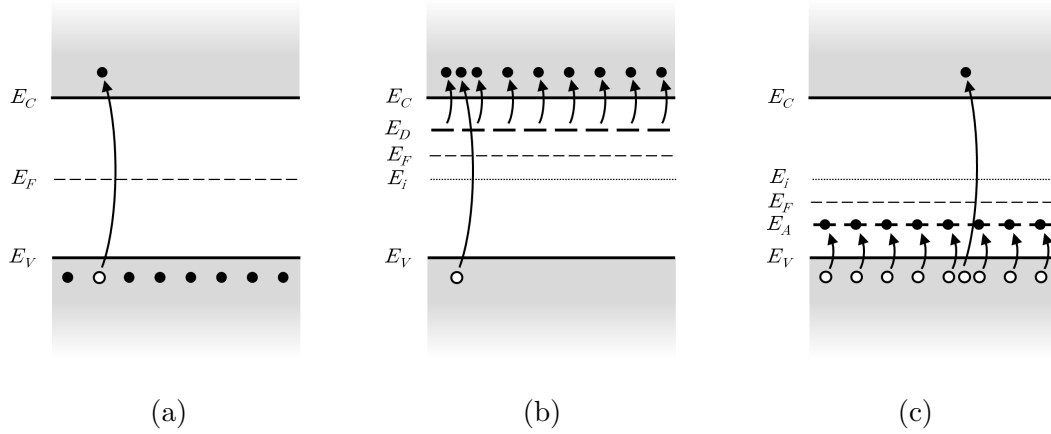


Figure 2.4: (a) Band diagram of carrier generation. The opposite is carrier recombination. (b) Band diagram of n-type silicon. (c) Band diagram of p-type silicon.

(figure 2.4b). For group III dopants, states are said to be acceptor type and reside at an energy E_A very close to the valence band energy ($E_A - E_V = 0.045 \text{ eV}$ [2]). Electrons in the valence band are able to jump to this energy level leaving holes in the valence band (figure 2.4c). As a consequence of doping with donor (acceptor) type atoms, the Fermi level is raised (lowered) above (below) the intrinsic value E_i .

2.1.1.4 p-n junction

As mentioned before, in HV-CMOS technologies a p-type silicon substrate is typically used. To implement the diodes or *pixels* into the substrate, n-type silicon is used to form an interface that is known as a *p-n junction*. P-n junctions exhibit the characteristics of a diode when an external voltage is applied i.e., current flows mainly in one direction.

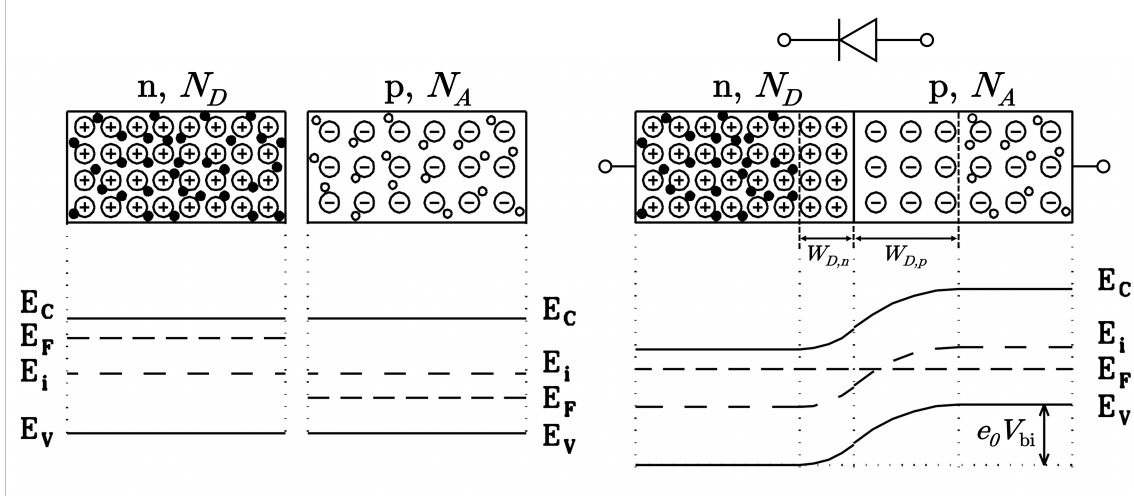


Figure 2.5: Diagram of the lattice and band diagram of a p-n junction diode with its parts separated (left) and brought together (right). Image modified from reference [2].

The image on the left of figure 2.5 (taken from reference [2]) shows a diagram of the lattice structure of separated n-type silicon with donor concentration N_D and p-type silicon with acceptor concentration N_A , and their respective band diagrams. In a p-n junction diode, the two regions are in contact (right of figure 2.5). Under equilibrium conditions (no external voltage), electrons from the n-type region diffuse into the p-type region and recombine. Similarly, holes from the p-type region diffuse into the n-type region and recombine. The positively charged donor ions that are fixed in the lattice in the n-type region give it a positive charge, and the negatively charged acceptor ions fixed in the lattice in the p-type region give it a negative charge. The result is an electric field that repels further carriers from the interface, which face a potential barrier given by the *built-in potential* $e_0 V_{bi}$ where e_0 is the elementary charge and V_{bi} is the *built-in voltage*. This creates a region depleted of charge carriers known as the *depletion region*, and it is the electric field in the depletion region that is responsible for the improved performance of particle detectors developed in HV-CMOS technology compared to standard CMOS technology. This is expanded upon in section 2.2.2. The width of the depletion region W_D is given by [2]:

$$W_D = \sqrt{\frac{2\epsilon_{Si}\epsilon_0(N_A + N_D)}{e_0 N_A N_D}} \cdot V_{bi} \quad (2.1)$$

where ϵ_0 is the vacuum permittivity, ϵ_{Si} is the relative permittivity of silicon, and $W_D = W_{D,n} + W_{D,p}$, where $W_{D,n}$ is the width of the depletion region in the n-type, and $W_{D,p}$ is the width of the depletion region in the p-type.

Forward bias

When the p-type region is connected to the positive terminal and the n-type region is connected to the negative terminal (i.e., $V > 0$), this is known as a *forward bias* (see figure 2.6a). This bias causes a force on the electrons and pushes them from the n-type region towards the p-type region. The same can be said for the holes, which are pushed towards the n-type region. In this regime, the width of the depletion region decreases and is narrow enough for carriers to cross the junction and current can flow. The voltage across the junction decreases to $V_{bi} - V$ and the width of the depletion region will decrease to [2]:

$$W_D = \sqrt{\frac{2\epsilon_{Si}\epsilon_0(N_A + N_D)}{e_0N_A N_D} \cdot (V_{bi} - V)} \quad (2.2)$$

Reverse bias

The opposite scheme, when the n-type region is connected to the positive terminal and the p-type region is connected to the negative terminal ($V < 0$), is known as *reverse bias* (figure 2.6b). Charge carriers are pulled away from the junction, which leaves behind more charged ions, increasing the width of the depletion region and the electric field. Carriers are unable to cross the large depletion width and there is minimal current flow. When silicon is used in particle physics experiments as particle sensors, it typically consists of p-n junction diodes operated in the reverse bias condition. When a particle traverses the depleted silicon, the energy of the particle is transferred to the lattice and electron-hole pairs are generated. In depleted silicon, the electron-hole pairs are quickly separated and drift towards their respective electrodes ensuring fast and large signals, as opposed to non-depleted silicon where charges diffuse through the lattice. However, high energy particles and radiation can damage the silicon substrate and affect the size of the depletion region and therefore affect performance.

2.1.1.5 Radiation damage

In addition to intentionally introduced dopants into silicon (or oxygenated silicon), the lattice may contain several unintentional so-called *point defects*. These may be: vacancies, which are the absence of a silicon atom of its position in the lattice; interstitials, where either silicon or some other impurity may exist between lattice atoms; or substitutional where impurities take the place of silicon in the lattice. A diagram from reference [2] is shown in figure 2.7a. These types of defects create additional levels within the silicon bandgap which electrons can use to transition more easily from the valence to the conduction band for example. If this occurs

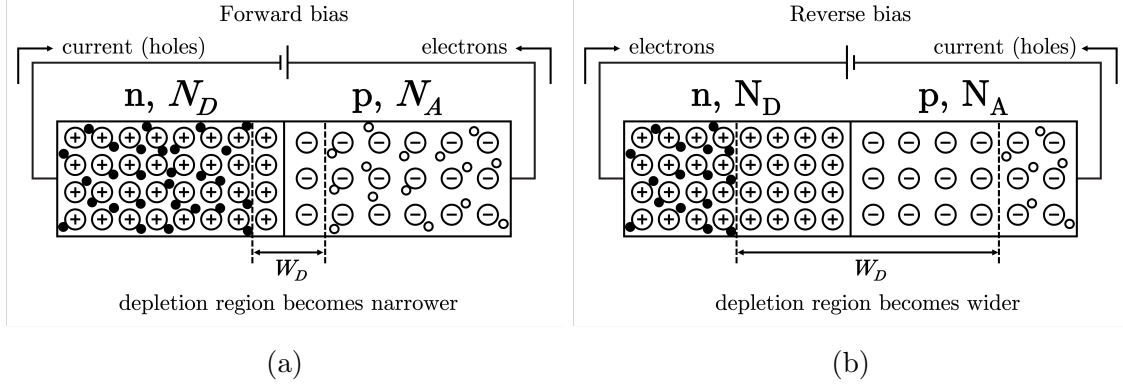


Figure 2.6: (a) Diagram of the effect of forward bias on a p-n junction. (b) Effect of reverse bias on a p-n junction. Image modified from reference [2].

in the depleted substrate when the detector is reverse biased, the electrons will be collected before recombination, resulting in leakage current [3]. So-called line defects are also possible (figure 2.7b) [2].

The final defect depicted in figure 2.7a is what is known as a *Frenkel pair*, which can be created by radiation colliding with a lattice atom [1], displacing it, resulting in an interstitial next to a vacancy. If a particle has a high enough energy, it can create multiple defects along its path over a short distance, which are known as *defect clusters*. All the examples given so far are not necessarily permanent or fixed in place in the lattice. It is possible that Frenkel pairs recombine for example through thermal annealing at room temperature. However, it is also possible that these defects can diffuse through the lattice and combine with other defects into more stable *defect complexes*, for example divacancies (two vacancies next to each other, see table 2.1). A detailed list with energy levels, charge states and annealing temperatures can be found in reference [2]. In the same way that boron and phosphorus add acceptor or donor states in the silicon bandgap (respectively), defects may also be of acceptor or donor type. The consequences are macroscopic effects. These defects contribute to the effective doping concentration and therefore affect the size of the depletion region (see equation 2.2). In addition, these defects affect carrier mobility, and can trap electrons or holes generated in the depletion by incoming particles, which reduces the signal. The effect of radiation damage on detectors fabricated using HV-CMOS technology will be discussed in section 2.2.3.

2.1.2 Detector surface

At the edges of the lattice, there are open bonds that are not shared with other silicon atoms. These are known as *dangling bonds*. At these surfaces, the silicon is intentionally exposed to oxygen in a controlled way, to form SiO_2 . This would otherwise happen naturally due to oxygen in the atmosphere but there are also

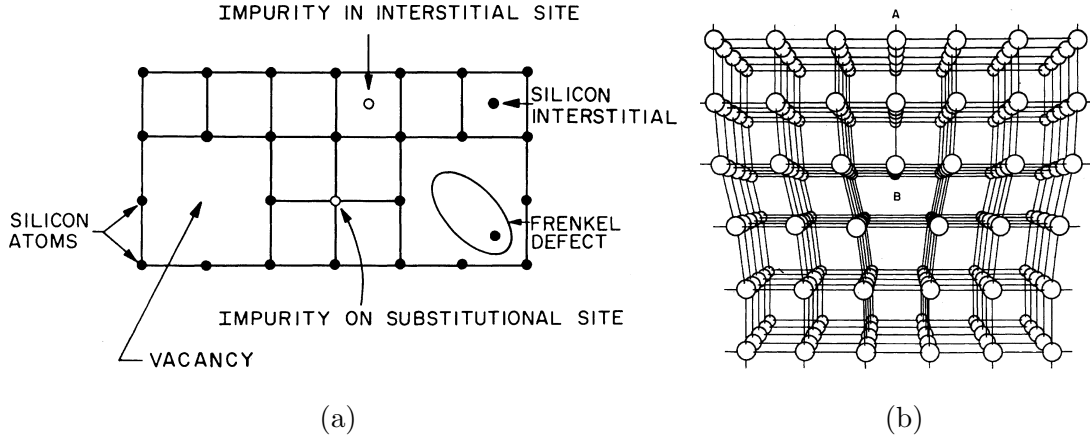


Figure 2.7: (a) Diagram of different types of point defect represented in a 2D lattice [2]. (b) Diagram of a line defect [2].

Table 2.1: Characteristics of some example defects in silicon [2].

Defect	Charge state	Energy level	Annealing temp. [K]
interstitial	I^-	$E_C - 0.39$	140–180
	I^0	$E_V + 0.40$	540–600
	I^+		370–420
vacancy	V^{--}	$E_C - 0.09$	
	V^-	$E_C + 0.40$	≈ 90
	V^0	$E_V + 0.05$	150
	V^+	$E_V + 0.13$	
	V^{++}		
divacancy	V_2^{--}	$E_C - 0.23$	≈ 570
	V_2^-	$E_C - 0.39$	≈ 570
	V_2^0	$E_V + 0.21$	≈ 140
	V_2^+		≈ 570

other pollutants. This Si-SiO₂ interface is used for passivation from the pollutants, but also in a number of structures in HV-CMOS (and standard CMOS) technologies such as transistor gate oxides, Metal-Oxide-Semiconductor (MOS) capacitors, and Shallow Trench Isolation (STI). The SiO₂ that is formed occupies most of the dangling bonds, but some are left over which have a negative effect on the performance of detectors. In addition, the lattice structure at the surface of the silicon is not perfect. There are many deformities left over from cutting the wafers from the ingot, and these are further enhanced after exposure to ionising radiation due to the intrinsic properties of the surface materials and its structure, which will be described in this section.

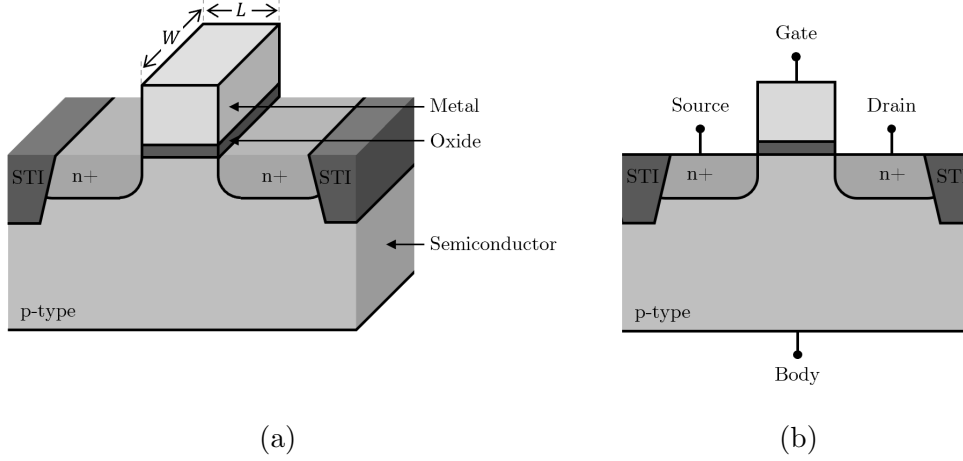


Figure 2.8: (a) 3D diagram of a MOSFET. (b) 2D cross-section diagram of a MOSFET with terminal names.

2.1.2.1 MOSFET

Complementary Metal-Oxide-Semiconductor (CMOS) refers to the complementary nature of using both n-type and p-type MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors) to construct electronic components, such as logic gates. The naming convention “metal-oxide-semiconductor” comes from the physical structure of a MOSFET: a metal gate on top of a thin oxide layer, on a semiconductor body. This is depicted in figure 2.8a, with the terminal names given in figure 2.8b. In this case, an nMOS transistor is shown, so-called as the majority charge carriers responsible for the function of the device are negatively charged electrons. MOSFETs are created on the surface of silicon wafers and two types of Si–SiO₂ interface described above can be seen in the figures: the gate oxide, and STI. The interface created between the silicon substrate and the SiO₂ STI is highlighted here as it is responsible for some effects that become important later in this thesis. The effects described in this section also apply to the gate oxide–substrate interface, but this goes beyond the scope of this thesis.

2.1.2.2 Si–SiO₂ interface

An important to note property of SiO₂ is that it possesses some intrinsic positive charges which are fixed in place. These are known as fixed oxide charges Q_f . Reference [2] explains that unlike the highly ordered lattice of the silicon substrate, the structure of SiO₂ is amorphous, and the positive charge could be due to holes trapped in the defects. The number of defects increases with vicinity to the Si–SiO₂ interface due to the transition between the two materials, where the charge density at the interface is around 10^{10} – 10^{12} cm^{−2}. Reference [4] provides a detailed description of the structure (figure 2.9). At the bottom of the image is the pure silicon

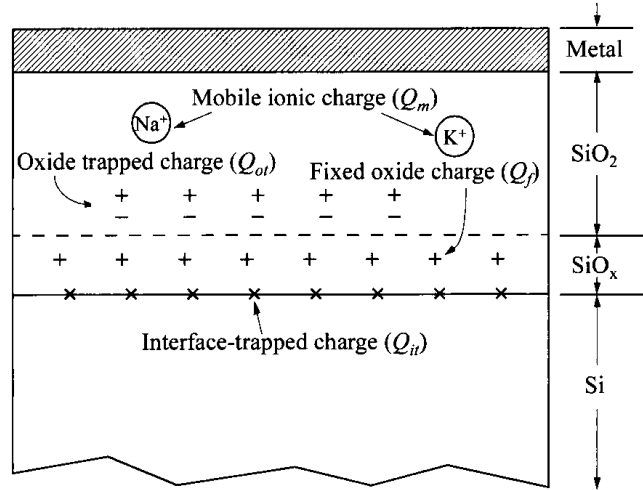


Figure 2.9: Cross-section diagram of a MOS capacitor [4] showing traps and charges.

crystal, above that a single layer of incompletely oxidised silicon (what the authors call SiO_x where $2 > x > 1$), and finally the remaining amorphous SiO_2 . In p-type silicon, the positive oxide charges cause electrons to accumulate at the Si– SiO_2 interface, forming a thin conducting layer or inversion layer [2]. This is detrimental in the structure in figure 2.10 shown in the next section, as the conducting layer forms between the diode electrodes.

2.1.2.3 Radiation damage

This effect only worsens in the presence of ionising radiation due to additional generated and subsequently captured holes. A good description is also given in reference [2] and summarised here. Using a similar description to the last section, SiO_2 in detectors can be thought of as regions with high densities of defects or additional energy levels within the bandgap. When ionising radiation passes through this region, charge carriers are generated which become trapped in the defects. However, as SiO_2 is an insulator, the bandgap (see figure 2.4a) is much larger than that of silicon for example therefore, emission of charge carriers is much more difficult. In addition, the mobility of electrons in SiO_2 is many orders of magnitude larger than for holes, therefore holes are much more likely to become trapped whereas electrons can diffuse out of the SiO_2 . This increases the charge density, which saturates at $3 \cdot 10^{12}$ [2]. Because of the non-uniform structure of SiO_2 , damage introduced by non-ionising radiation displacing nuclei is negligible.

2.2 HV-CMOS technology

As discussed in the previous chapter, in recent years, studies have been conducted to determine if HV-CMOS detectors could survive the harsh challenges imposed

by the CERN HL-LHC upgrade. Measurements have shown that the radiation tolerance of HV-CMOS detectors is excellent. As a reminder, in test beam data HV-CMOS detectors demonstrated hit efficiencies up to 99.7% at fluences up to $1 \cdot 10^{15} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$ and 97.6% efficiency at fluences up to $5 \cdot 10^{15} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$. However, the fluences expected over the lifetime of the upgraded ATLAS and CMS experiments for example, is approximately $2 \cdot 10^{16} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$ i.e. approximately one order of magnitude higher. Therefore, the experiments have opted for hybrid pixel detectors, which demonstrate higher radiation tolerances. This section covers the details of detectors developed in HV-CMOS technology. In 2.2.1 the internal structure of pixels is given. In 2.2.2, the particle detection mechanism of depleted silicon sensors is expanded upon. Finally in 2.2.3, the macroscopic effects of radiation damage on HV-CMOS detectors is discussed.

2.2.1 Structure of HV-MAPS

HV-CMOS technologies share many similarities with standard (‘low-voltage’) CMOS technologies but make use of additional implants to isolate low voltage and high voltage regions. Like CMOS, electronic components are incorporated directly into the wafer or *substrate*. The substrate is a single-crystal semiconductor, usually silicon, with some impurities added intentionally to increase the conductivity. For typical particle physics applications, a 2D array of diodes is implemented into the substrate by designers, which act as the sensing elements for particle detection. These diodes are known as *pixels* and detectors are known as *pixel detectors*. Individual pixels typically take a square or rectangular shape, and are arranged into matrices: rows and columns of pixels in a evenly spaced grid pattern for position sensitivity. Matrices can range in size, from matrices with less than 100 pixels for testing in laboratories for example, to much larger arrays ($> 50,000$ pixels) for experimental applications. This means that HV-MAPS sensor sizes can range from a few square millimetres (i.e., the minimum size allowed by manufacturers), to matrices encompassing the scale of the wafer (8 inches) using stitching, depending on the intended use.

A cross-section diagram of a typical HV-MAPS pixel produced for particle physics applications in an HV-CMOS technology based on LFoundry 150 nm technology can be seen in figure 2.10. In this example, a $300 \mu\text{m}$ thick, low concentration p-type silicon substrate (depicted in green) is used, with opposite type (n-type, in orange colours) pixels. Note that there is no reason that silicon types in this example could not be exchanged. Each coloured box represents a different well, which are formed by implantation of n-type or p-type dopants. The high concentration p-type well (p+), shallow p-type (SP) well stacks on the outside of the image are used to bias the substrate to the *substrate bias voltage* V_{sub} . In

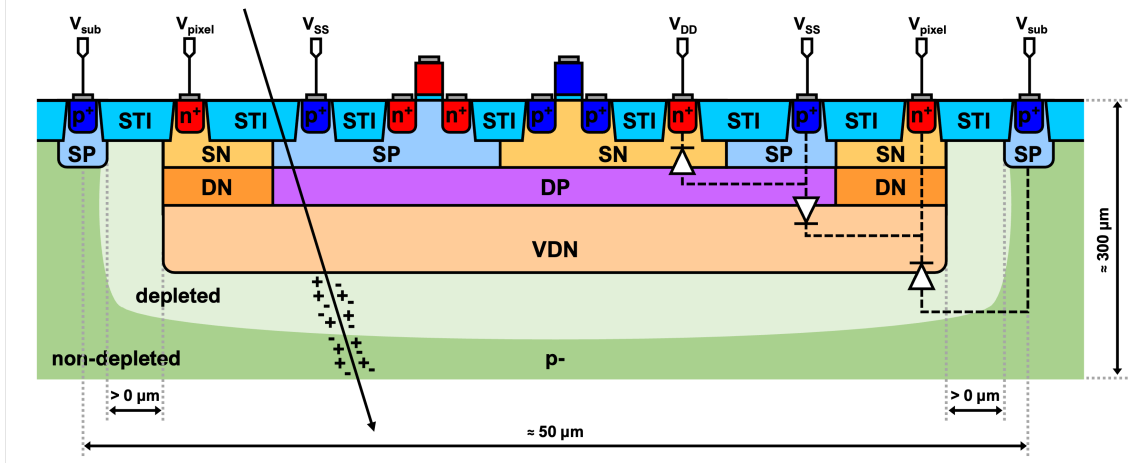


Figure 2.10: Cross-section diagram of a typical pixel produced in HV-CMOS technology (LFoundry 150 nm).

three dimensions, these take the shape of a single ring that surrounds the other implants in the centre of the image. This ring (along with the p-type substrate) forms the anode of the pixel diode. The very deep, buried n-type well (VDN) forms the cathode of the pixel diode, and is biased to the pixel bias voltage V_{pixel} through the high concentration n-type well (n+), shallow n-type (SN), deep n-type (DN) stacks. Other HV-CMOS vendors may achieve this structure in other ways, but the principle is the same. For the purposes of particle detection, the pixel diode is reverse biased by setting $V_{pixel} = 0$ V (or a small, positive voltage if transistors are present and need to be powered) and V_{sub} to a negative high voltage (≈ -100 V). The depletion region of this p-type substrate–VDN junction then extends (mostly) into the more lightly doped (p-) substrate, creating a large volume that is sensitive to impinging particles. This will be discussed in more detail in the next section.

In three dimensions, the n+/SN/DN stacks also form a ring shape and together with the VDN well, enclose the wells containing CMOS electronics (red for NMOS, blue for PMOS in the image), in order to isolate these low-voltage regions from the high-voltage substrate. The function of circuits is therefore limited to the available area, dictated by the size of the VDN well, which can be approximately $40 \mu m \times 40 \mu m$ for the smallest pixels. The SN and SP wells serve another function here, forming the body of PMOS and NMOS transistors, respectively and transistor source and drain terminals are formed using p+ and n+ wells. SP wells are typically biased to the ground voltage $V_{SS} = 0$ V through a p+ well and SN wells to $V_{DD} \approx 1-2$ V via an n+ well in order to ‘power’ transistors. In typical particle physics applications, in-pixel electronics could consist of signal amplification, particle time stamping, and hit discrimination circuits, for example. It is worth mentioning that the high doping concentration n+ and p+ wells are isolated from each other using a process known as Shallow Trench Isolation (STI), which have been included in the diagram as they

are responsible for some important side-effects which will be discussed throughout this thesis. These are formed by excavating small pits (trenches) in the silicon that are subsequently exposed to oxygen gas, which reacts with the silicon to fill the trenches with silicon dioxide, an insulator. This prevents regions of high electric field forming between the high doping concentration wells of opposite type which causes electrical breakdown. The final well in the diagram is the deep p-type well (DP) which is implanted underneath the SP and SN wells. It is used to isolate those SN wells that contain electronics from the (n-type) cathode of the pixel diode (the VDN well), the latter of which is susceptible to transient currents created by traversing particles. Once again, in three dimensions, the p+/SP stacks form a ring to enclose these SN wells from the sides. The alternating opposing well types (and appropriate biasing) form three reverse biased diodes that are depicted in the diagram.

An ideal diode would only allow current to flow in one direction i.e., when the electric potential is greater at the anode than the cathode, there is a flow of current, and in the opposite situation there is no current flow. These are the *forward* and *reverse bias* scenarios discussed in the last section. In reality, when a diode is reverse biased there is a very small (but non-negligible) current which is known as the reverse saturation or *leakage current* I_{leak} (see figure 2.11). During particle detection experiments, the pixel diode is operated at a voltage (V_{sub}) somewhere along this current plateau, since I_{leak} is low. Increasing the operating voltage within this region is beneficial to the performance of the detector as the size of the depletion region is increased, with no penalty in terms of increasing I_{leak} . However, if a large enough reverse voltage is applied across the diode, the diode will *break down*, and a large current will flow between the terminals. The voltage at which this occurs is known as the *reverse breakdown voltage* or sometimes just *breakdown voltage* V_{BD} , and is unique to each diode. Operating diodes far beyond this value for extended periods of time is not recommended as this risks permanently damaging it. In particle physics applications, the pixel diode is designed specifically to ensure a very large V_{BD} , and a very low I_{leak} , two important parameters with respect to particle detection.

The first parameter I_{leak} , is a contributor to the detector noise [2] and should therefore be as low as possible to retain a high SNR. The second parameter V_{BD} , is the limiting factor in the maximum V_{sub} of the diode. If the p+/PW stacks between neighbouring pixels are biased to V_{sub} (as is done in MuPix and ATLASPix, other groups leave them floating), a simple way to increase V_{BD} is to include spacing between the pixel diode electrodes, since V_{BD} is proportional to this distance (labelled $> 0 \mu\text{m}$ in figure 2.10). This, however, increases the overall size of the pixel, and the trade-off must be considered depending on the requirements of the detector. V_{BD}

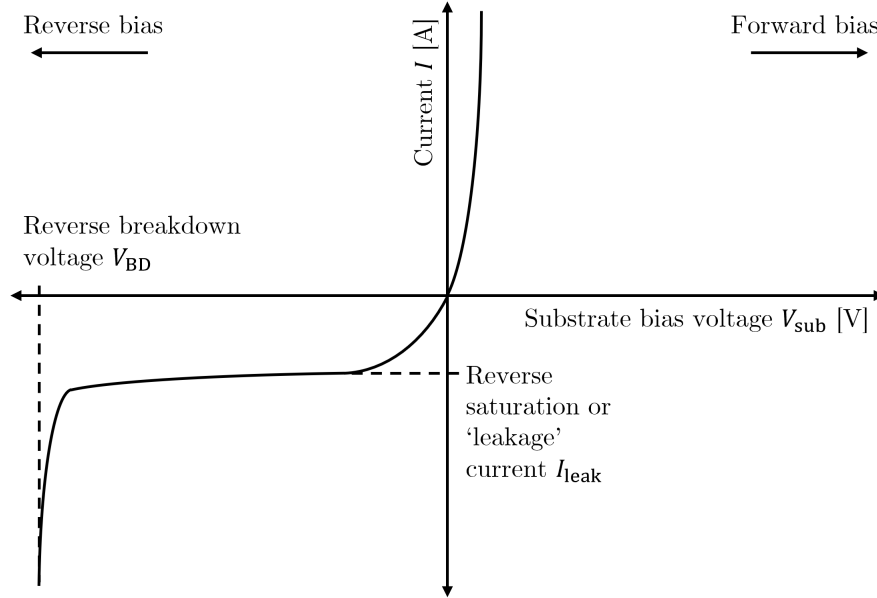


Figure 2.11: Diagram of the I–V characteristics of a diode. The sensing element in HV-CMOS pixels are reverse biased diodes.

is typically under 100 V (much larger than voltages in standard CMOS processes) but V_{sub} should however, preferably be as high as possible, as it ensures traversing particles are detected quickly with high SNR and improves the performance of detectors after damage due to radiation. This will be discussed in more detail in the next section.

2.2.2 Particle detection mechanism

The particle detection mechanism is similar to that of other silicon sensors, such as those in hybrid modules. When the pixel diode is reverse biased, the interface between the pixel and the substrate becomes depleted of charge carriers, forming the depletion region. When particles travel through the silicon, their energy is transferred to the atoms in the lattice, generating electron/hole pairs. Under the influence of the electric field in the depletion region, these charge carriers move towards their respective diode electrodes which in turn generates an electrical current, signifying a detection. In depleted silicon, the presence of the electric field ensures the primary carrier transport mechanism is drift as opposed to diffusion in non-depleted silicon, which allows charge collection to occur much faster. The size of the depletion region determines the number of charge carriers that can be collected by drift, which is about $80 \mu\text{m}^{-1}$ in depleted silicon [5, 6]. This means that a larger depletion region is beneficial, as more charge carriers increases the current and therefore the SNR. As the substrate is lightly doped with respect to the pixel, the depletion region extends into the substrate, laterally outwards from the pixel (towards other pixels or

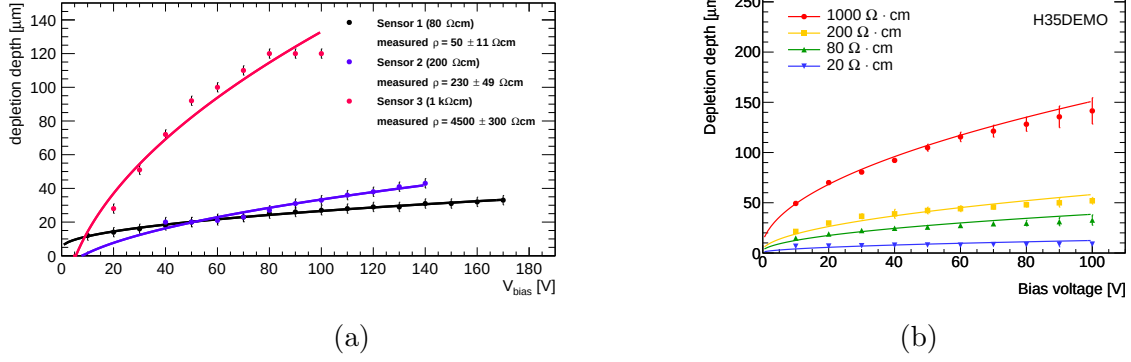


Figure 2.12: (a) Measurements of W_D with respect to V_{sub} for three samples with different substrate resistivities from reference [8]. (b) Measurements of W_D with respect to V_{sub} for four samples with different substrate resistivities from reference [9].

structures), and vertically down towards the opposite side of the detector. Like the p-n junction described in the previous section, the size of the depletion region with respect to substrate bias voltage V_{sub} follows a square root law, and for a p-type silicon substrate, the thickness of the depletion region W_D in μm is approximated from equation 2.2 as [7]:

$$W_D = 0.3\sqrt{\rho(V_{\text{sub}} + V_{\text{bi}})} \quad (2.3)$$

where ρ is the resistivity of the substrate in $\Omega \cdot \text{cm}$. ρ is intrinsic to the substrate, and depends on the amount of impurity added to the silicon at the time of its initial growth. Since ρ is therefore a constant that depends on the detector, the size of the depletion region (and therefore the number of charges generated) can be increased by increasing V_{sub} . However, it can also be seen from equation 2.3 that it is beneficial to utilise a substrate with an initially high resistivity so that the size of the depletion region can be maximised with an equivalent voltage. Figures 2.12a and 2.12b show measurements of the depth of the depleted region with respect to substrate bias voltage for detector samples with different substrate resistivities [8, 9]. Samples with a higher substrate resistivity have a larger depletion region at the same substrate bias voltage and will therefore collect more charge from traversing particles, giving a higher SNR.

Planar silicon sensors in the CERN experiments for example, typically make use of very high- ρ silicon and operate at high voltages to ensure the depletion region extends throughout the entire depth of the silicon [10]. This is known as *full depletion* and the voltage at which the silicon is fully depleted is known as the full-depletion voltage V_{FD} . Detectors are operated at or above V_{FD} in order to maximise the SNR, and V_{FD} for state-of-the-art, high- ρ , 300 μm thick planar silicon sensors is about 100 V [11]. When designing silicon pixel detectors, it is therefore important

to consider the reverse breakdown voltage V_{BD} , which is the limiting factor in the operating voltage. Planar silicon sensors are therefore designed to ensure $V_{BD} > V_{FD}$.

Another effect that must be considered when designing detectors concerns the increase in V_{FD} with damage dealt to the detector by impinging radiation. After prolonged use in high radiation experimental environments, defects are introduced into the otherwise highly regular crystal lattice, which causes a change in the size of the depleted volume. Generally speaking, the size of the depletion region will decrease with an increase in radiation damage but this relationship will be explored more in the next section. This, combined with an increase in the leakage current, has a drastic negative effect on the SNR. This can be overcome by ensuring $V_{BD} \gg V_{FD}$, to ensure that the sensor can always be fully depleted, irrespective of the amount of radiation damage. This effect will be discussed in more detail the next section.

2.2.3 Effects of radiation damage

Silicon detectors such as those in experiments at CERN, are usually placed as close to the beamline as possible. This is because pixels can be very small, and detectors are therefore capable of very high spatial resolution and allow for very accurate particle track reconstruction. However, as a result of their vicinity to the beamline, they are constantly bombarded by high energy particles and radiation, which poses a significant threat to the performance of the detector over its lifetime. Over the many years of operation of hybrid silicon detectors in CERN, there have been many studies of how radiation damage affects both sensors [1, 12–14] and the readout chips [15–17]. In recent years, similar studies have been used to characterise the performance of HV-CMOS pixel detectors under similar conditions [9, 18, 19]. This section will briefly outline these latter studies and the metrics used to measure radiation tolerance.

The performance of silicon particle detectors depends heavily on the initial crystal lattice in which they are constructed. Any defects in the otherwise regular lattice structure have a largely negative effect on the detector behaviour, manifesting in forms such as undesirable leakage currents, for example. These lattice defects can be introduced in several unintended ways such as improper handling, or after postprocessing steps (e.g., dicing from the wafer), but can also be inevitably introduced after prolonged use in high radiation environments. Radiation damage effects are characterised into two groups depending on the type of radiation: ionising or non-ionising. Ionising radiation, such as high energy X-rays or gamma rays, mainly affect the silicon dioxide (e.g., STI) at the surface of devices, which is mostly detrimental for the performance of electronic circuits. It is the damage introduced by non-ionising radiation that will be the focus of this section. High energy particles

that travel through the detector material can displace atoms in the lattice, which leaves defects deep within the substrate. This has negative effects on the macroscopic detector behaviour such as: increase in leakage current, which increases noise; change in the resistivity of the silicon, which affects the size of depletion region and therefore detection signal; and a reduction of the charge collection capabilities due to increased charge trapping probability. Measurements demonstrating these three effects will be discussed here, and the details behind the radiation damage mechanism are presented at the end of this chapter.

Increased leakage current

Firstly, defects in the silicon lattice introduced by non-ionising radiation increase the detector leakage current. This is detrimental to the function of the device as a particle detector, as it increases detector noise. Reference [14] shows a linear dependence on the leakage current increase ΔI_{leak} with radiation damage:

$$\Delta I_{\text{leak}} = \alpha \Phi_{\text{eq}} V \quad (2.4)$$

where α is the so-called current-related damage factor, Φ_{eq} is the radiation damage term, and V is the volume of the sensitive depletion region. Radiation damage by any hadron of any energy is typically expressed in terms of the 1 MeV neutron equivalent fluence, expressed as Φ_{eq} and will be throughout this thesis. The increase in I_{leak} with Φ_{eq} is also dependent on temperature and can therefore be mitigated somewhat by reducing the detector operating temperature.

Change in substrate resistivity

Secondly, extended use of detectors in the presence of non-ionising radiation changes the resistivity of the substrate over time. As mentioned before, the substrate resistivity depends on the concentration of dopants in the substrate, which is known as the effective doping concentration N_{eff} , where $\rho \propto 1/N_{\text{eff}}$. Radiation displaces atoms in the lattice, modifying N_{eff} which is modelled by the below formula [1]:

$$N_{\text{eff}}(\Phi_{\text{eq}}) = N_{\text{eff}0} - N_c \cdot (1 - \exp(-c \cdot \Phi_{\text{eq}})) + g_c \cdot \Phi_{\text{eq}} \quad (2.5)$$

where $N_{\text{eff}0}$ is the initial doping concentration or the amount of impurity added during crystal growth (i.e., when $\Phi_{\text{eq}} = 0$), N_c is the concentration of dopant atoms that have been removed, c is the dopant removal constant, and g_c is the stable damage introduction rate. Figure 2.13a shows measurements from the same study, of $N_{\text{eff}}(\Phi_{\text{eq}})$ of initially n-type substrates of silicon pixel and microstrip detectors, with varying concentrations of oxygen and carbon (added to improve radiation tolerance).

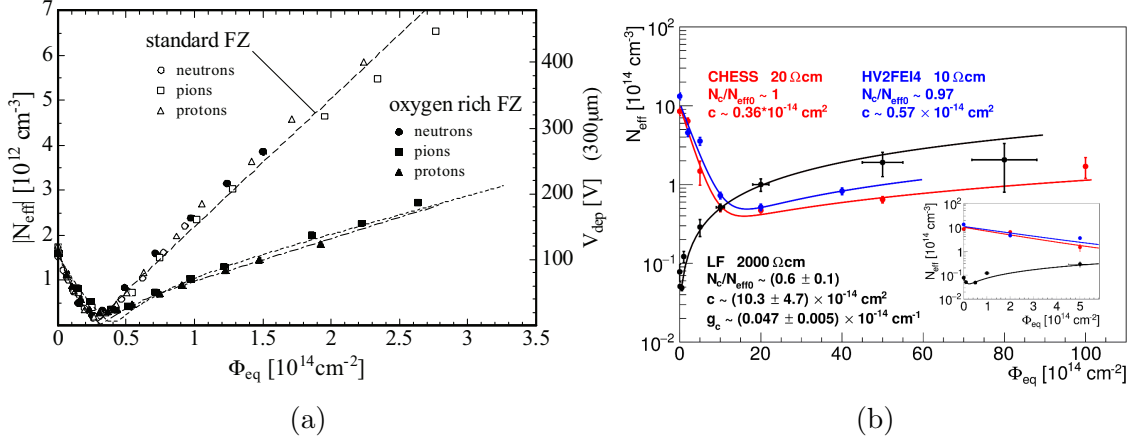


Figure 2.13: (a) N_{eff} dependence on Φ_{eq} ($V_{\text{dep}} = V_{\text{FD}}$) for samples on float-zone (FZ) and oxygen-rich FZ silicon from reference [1]. (b) N_{eff} dependence on Φ_{eq} for varying initial substrate resistivity from reference [20].

Figure 2.13b shows measurements of HV-CMOS pixel detectors of p-type substrate of varying resistivities (i.e., concentrations of p-type dopants) [20] where the same formula is used to study the behaviour. After irradiation with non-ionising radiation up to a low fluence ($\approx 5 \cdot 10^{13} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$), detectors experience an exponential decrease in N_{eff} until all dopants have been removed ($N_{\text{eff}0}/N_c = 1$). This effect known as *acceptor removal* or *donor removal*, depending on the electrical type of the silicon. For the n-type silicon in the first study, the damage introduces acceptor-like defects into the lattice which eventually causes the n-type substrate to effectively change to p-type. This is known as *type inversion*. Historically, n-type substrates were used, but typically p-type substrates are now used as most defects due to radiation damage are acceptor type and these affect p-type silicon less according to reference [21]. Then as irradiation increases ($> 5 \cdot 10^{13} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$), the $g_c \cdot \Phi_{\text{eq}}$ term dominates and N_{eff} increases approximately linearly. The value of g_c is therefore a good figure of merit for radiation tolerance, as it can be seen in figure 2.13a that substrates rich in oxygen - intentionally introduced to improve radiation tolerance - have a gentler slope, resulting in a smaller change in $N_{\text{eff}}(\Phi_{\text{eq}})$, and a drastically lower V_{FD} .

On this note, the change in ρ with Φ_{eq} can also be understood in terms of W_D . Like those presented in figure 2.12, measurements of $W_D(V_{\text{sub}})$ of multiple samples of the same HV-CMOS detector irradiated to different fluences reveal a general decrease in W_D as Φ_{eq} increases as shown from data in studies [18] and [19] (see figures 2.14a and 2.14b). This can be attributed to the general increase in N_{eff} . In these studies, the data are fitted with a modified version of formula 2.3:

$$W_D = \sqrt{\frac{2\varepsilon_{\text{Si}}\varepsilon_0}{e_0 N_{\text{eff}}}} \cdot V_{\text{sub}} \quad (2.6)$$

Despite a general initial increase in $W_D(\Phi_{\text{eq}})$ in data from reference [18] due to

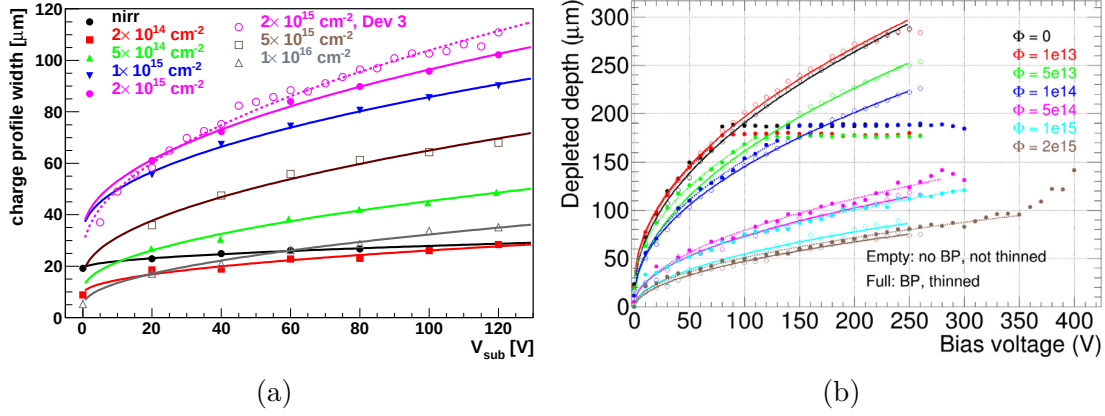


Figure 2.14: (a) W_D (“charge profile width” in this publication) dependence on V_{sub} for multiple samples irradiated to different fluences from reference [18]. The starting resistivity was $20 \Omega \cdot \text{cm}$. (b) W_D (‘depleted depth’ in this text) dependence on V_{sub} (‘bias voltage’) for multiple samples irradiated to different fluences from reference [19]. The starting resistivity was $> 2000 \Omega \cdot \text{cm}$.

the decrease of N_{eff} at low fluences, W_D unavoidably decreases as the samples are irradiated to higher fluences. Not only is this undesirable as the detector behaviour changes over its lifetime - something which must be understood if detectors are to be used in experiments - but this also negatively affects detector performance in terms of charge collection, something which is discussed in more detail in the next section. Samples from the second study [19] irradiated up to $1 \cdot 10^{14} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$ reach full depletion (V_{FD}) which can be seen by the plateau in data at around $180 \mu\text{m}$ – $190 \mu\text{m}$. Samples irradiated to the higher fluences in this study ($> 1 \cdot 10^{14} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$) are unable to be fully depleted due to the increase of V_{FD} past V_{BD} ($V_{\text{FD}} > V_{\text{BD}}$)¹.

Reduced charge collection

Lastly, another important detector property affected by radiation damage is its ability to collect charge Q generated by traversing particles. As damage due to irradiation increases, a general decrease in Charge Collection Efficiency (CCE) is observed. This is detrimental to the performance of detectors, as less charge can be collected, reducing an SNR already negatively affected by an increase in leakage current. Results of CCE measurements of two HV-CMOS detectors are discussed in this section, one low and one high resistivity ($20 \Omega \cdot \text{cm}$ and $> 2000 \Omega \cdot \text{cm}$, the CHESS-1 device from figure 2.13b and another high resistivity similar to the LF device in the same figure), described in references [18] and [19] respectively. As seen from the measurements (see figures 2.15a and 2.15b), the general trend in the

¹Detectors irradiated to high fluence in this study exhibit an observed increase in V_{BD} (from an initial value of around 100 V to 150 V after irradiation), but not enough to counteract the increase in V_{FD} .

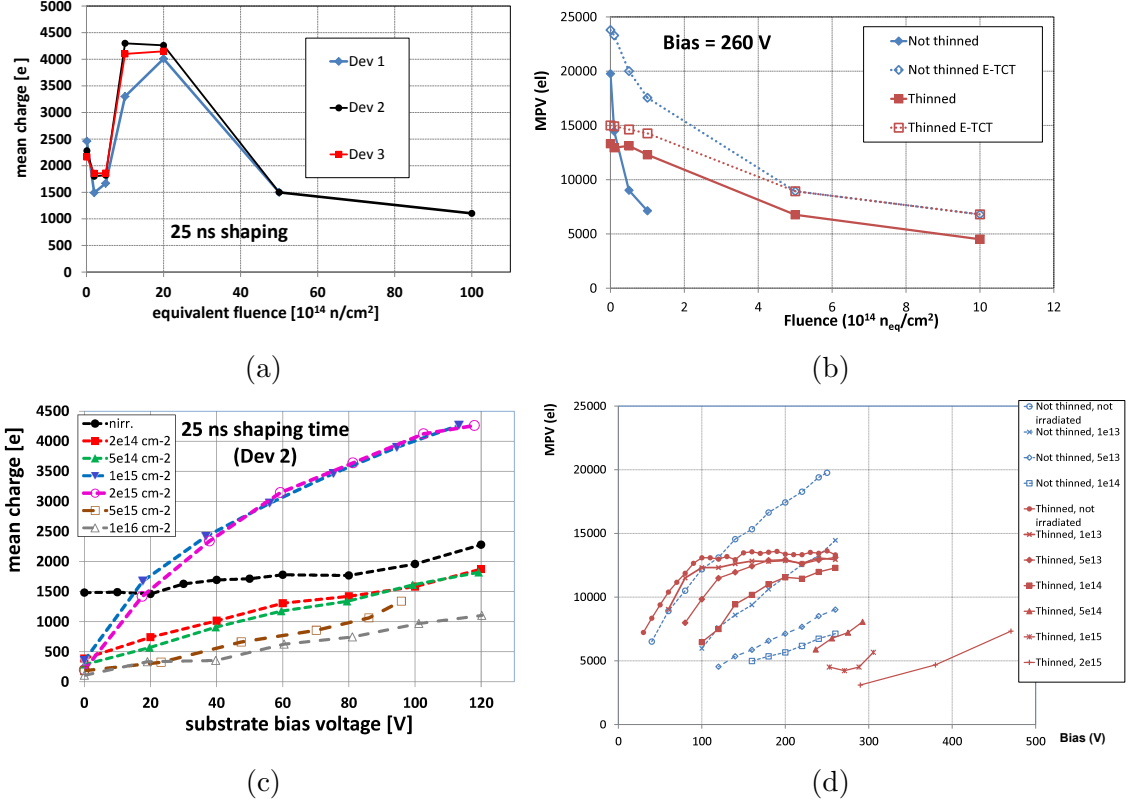


Figure 2.15: (a) at 120 V from [18]. (b) at 260 V from reference [19]. (c) from [18]. (d) from reference [19].

number of electrons collected decreases as Φ_{eq} increases, with the initial increase in the data from [18] attributed to acceptor removal. Measurements are typically performed by firing high energy electrons at the sensor, causing them to traverse the entirety of the detector material. In this way, particles pass through both depleted and non-depleted bulk, and the effects of radiation damage on both states of silicon can be studied. This is achieved by both collimating the electron source and placing a readout trigger on the opposite side of the detector to favour those high energy electrons that behave as Minimum Ionising Particles (MIPs).

The results in figures 2.15a and 2.15b can be explained by examining the number of electrons collected with respect to V_{sub} (figures 2.15c and 2.15d), and by comparing with their corresponding results of measurements of W_D (figures 2.14a and 2.14b in the previous section). In the study of non-irradiated, low substrate resistivity devices (10 – 20 Ω cm) in reference [18], the charge collection is observed to increase approximately linearly with V_{sub} . It depends on two components: the contribution due to drift, when charge carriers are generated in the depletion region in the presence of an electric field; and diffusion, when charge carriers are generated in the non-depleted bulk. The formula as given in reference [18] is:

$$Q(V_{sub}) \approx a + b \cdot V_{sub} \quad (2.7)$$

where a and b are the diffusion and drift components respectively. According to the authors, for the non-irradiated sample, (figure 2.15c), the 1500 or so electrons collected at $V_{\text{sub}} = 0\text{ V}$ are collected due to diffusion, and the subsequent increase with respect to V_{sub} is due to the growth of the depletion region and therefore contributions due to carriers collected by drift. The contribution due to diffusion at $V_{\text{sub}} = 0\text{ V}$ in irradiated samples diminishes, due to an increased probability of charges becoming trapped in defects in the now damaged substrate. However, the same linear trend due to the drift contribution is observed for samples irradiated up to $5 \cdot 10^{14} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$, demonstrating that carriers collected by drift are affected less by charge trapping. It can be seen that the amount of charge collected by drift largely depends on the size of the depletion region, when the data is compared with measurements of W_D (figure 2.14a). Samples irradiated to $1 \cdot 10^{15} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$ and $2 \cdot 10^{15} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$ exhibit larger depletion regions due to acceptor removal and more charge is collected by drift (larger b). The growth of the depletion region following the square root law $\sqrt{V_{\text{sub}}}$ becomes more apparent and the linear behaviour in equation 2.7 no longer holds. However, the effect of increased charge collection lessens as damage continues to increase with Φ_{eq} . The sample irradiated to $5 \cdot 10^{15} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$ for example, has a larger measured W_D than the non-irradiated sample but collects less charge as charge trapping also affects charges in the depletion region due to g_c .

Similar results are obtained by the group in reference [19] (figure 2.15d), a general decrease in charge collection is seen as Φ_{eq} increases. But in contrast to the previous study, samples with higher substrate resistivity ($> 2000 \Omega \cdot \text{cm}$) were used, and the effects of acceptor removal are not as pronounced (see figure 2.13b) and there is no initial increase in $Q(\Phi_{\text{eq}})$. The increase in $Q(V_{\text{sub}})$ is also seen (figure 2.15d), but it should be noted that both thinned and non-thinned detectors were used in this study. Thinned detectors (shown in red in the figures), reach a maximum Q at low Φ_{eq} when detectors reach full depletion i.e., due to the maximum possible size of W_D as it reaches the backside of the detector. As W_D generally decreases with Φ_{eq} , the thinned samples are no longer able to reach full depletion and V_{sub} is limited by V_{BD} (V_{FD} increases past V_{BD}).

There are two noteworthy effects seen in this study when considering the design of future detectors. The first is that thinning, and backside biasing detectors is beneficial to charge collection in irradiated devices. Despite the maximum value of W_D , thinned detectors collect more charge than non-thinned counterparts at equivalent Φ_{eq} (seen most clearly in figure 2.15d, samples irradiated to $1 \cdot 10^{14} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$, data shown with squares), due to charge trapping, the weighting field in the sensors, and the electric field structure after irradiation as detailed in reference [14]. The second is that increasing V_{sub} is beneficial from a charge collection point of view.

V_{BD} of the detector irradiated to the highest fluence in this study ($2 \cdot 10^{15} \text{ n}_{eq} \cdot \text{cm}^{-2}$) increases quite dramatically and more charge can be collected. This suggests that could the detector breakdown voltage be improved, operating voltages of HV-CMOS particle detectors greater than those seen in reference [19] (figure 2.15d) might be possible, and the amount of charge collected could be increased, despite accumulated radiation damage, maintaining an optimal SNR. This demonstrates that careful consideration of the detector breakdown voltage during the design phase is critical in ensuring radiation tolerance.

2.3 Review of the state-of-the-art

In this section current HV-CMOS detectors are assessed. The review includes the HV-CMOS pixel detectors developed for the Mu3e and LHCb experiments, MuPix and MightyPix and a third example, developed for general radiation tolerance R&D named LF-Monopix. This section mainly focusses on devices from the point of view of the sensors. Areas of interest include the manufacturing process used, wafer properties, pixel characteristics, and general design attributes that improve radiation tolerance. Electronics will only be touched on briefly and references are provided for further reading.

As HV-CMOS is an emerging technology in the particle physics community, features from other species of detectors are also reviewed. Hybrid detectors are known to exhibit high radiation tolerance and have been chosen for the next generation of experiments. Therefore, those detectors are examined here in order to evaluate the techniques used for ensuring high radiation tolerance to potentially improve the design of HV-CMOS detectors. A state-of-the-art MAPS, ALPIDE, is also studied. This section of the review is by no means exhaustive, and will cover just a few important examples.

2.3.1 HV-CMOS pixel detectors

2.3.1.1 MuPix

The MuPix series of chips are detectors developed for the pixel tracker at the Mu3e experiment, the first experiment to make use of HV-CMOS detectors. MuPix10 [22] is the latest of the MuPix generations (at the time of writing MuPix11 is in the fabrication stage) and is being studied as a potential candidate for the final version to be used in the experiment. It was produced using the $0.18 \mu\text{m}$ process from TSI [23] on $200 \Omega \cdot \text{cm}$ p-type substrate, and the structure of the chip is similar to the diagram in figure 2.10 above. Pixels are implemented in deep n-wells, which are reverse biased to -80 V to deplete the substrate to a depth of $\approx 40 \mu\text{m}$ and create

a large sensitive volume. The signal is then amplified by an amplifier built directly into the pixels. Pixels measure $80\,\mu\text{m} \times 80\,\mu\text{m}$ with an active area nearly the size of the full chip area (3 mm are left at the periphery for readout electronics).

The chip is particularly interesting because sensors in the Mu3e experiment must be incredibly thin, the total thickness of each chip being $50\,\mu\text{m}$. This will be the first demonstration that very thin HV-CMOS sensors are possible, which is useful in experiments because multiple scattering is reduced, and as demonstrated in reference [19], can improve charge collection efficiencies in irradiated sensors with respect to non-thinned samples. The radiation tolerance requirements for the Mu3e experiment are low however, but MuPix10 sensors were designed with radiation tolerant features, such as Enclosed Layout Transistors (ELTs) (and of course, charge collection by drift) [24]. In this way, the radiation tolerance of the TSI $0.18\,\mu\text{m}$ technology can be studied for future projects such as MightyPix.

2.3.1.2 MightyPix

During LS3 of the LHC in 2026, CERN experiments plan to use the time to upgrade their systems ready for R4 and the HL-LHC in 2029. The so-called Upgrade Ib for the LHCb experiment [25], involves the installation of the proposed Inner Tracker (IT). Upgrade II would then begin during LS4 after R4 which would include installation of the Middle Tracker (MT). Both the IT and MT form the MighTy Tracker, and would be composed of silicon detectors fabricated using HV-CMOS technology, dubbed MightyPix. The group is exploring the use of the $0.18\,\mu\text{m}$ process from TSI, the same as the recent MuPix generations, building on those designs and those of a predecessor, ATLASPix.

The preliminary specifications of the MightyPix sensors [26] states that the current proposed pixel size is $100\,\mu\text{m} \times 300\,\mu\text{m}$ (width $\times$ height), with the possibility of reducing the size to $50\,\mu\text{m} \times 150\,\mu\text{m}$. This is larger than the state of the art, but the experiment does not require pixels as small as MuPix or ATLASPix. For the width of the pixel, the momentum resolution results from this width and a reduction below $100\,\mu\text{m}$ only benefits the highest momentum particles, according to studies. The resolution of the detector in the same direction as height of the pixel is expected to be dominated by multiple scattering below $300\,\mu\text{m}$. In addition to this, the document states that smaller pixels can be disadvantageous as reducing the size of pixels increases the number of bits required for readout, factors which need to be considered during the design phase.

One of the main requirements of the MightyPix chips is radiation tolerance, as detectors in LHCb experiment in R4 of the LHC must survive neutron equivalent fluences up to $6 \cdot 10^{14} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$ [26]. The future detector can benefit from studies conducted on devices produced in the same technology, namely ATLASPix and

MuPix sensors. The study in reference [24] demonstrates charge collection efficiencies above 98% for ATLASPix1 sensors irradiated up to $2 \cdot 10^{15} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$. This is a device produced in a very similar $0.18 \mu\text{m}$ technology from ams AG [27] and the authors state that MuPix10 and ATLASPix3 sensors are expected to have similar results. It could therefore be concluded that should MightyPix sensors be designed in a similar way, they should have a radiation tolerance sufficient for LHCb R4.

2.3.1.3 LF-Monopix

Finally, a detector produced in LFoundry 150 nm HV-CMOS technology [28] is investigated, known as LF-Monopix [29]. The device is very interesting for this study as it exhibits a breakdown voltage higher than 250 V. The reason for this is it was originally designed as a proof of concept that a fully monolithic sensor was capable of operating in the outer pixel layers of the Phase-II ATLAS upgrade where radiation levels would be $1.5 \cdot 10^{15} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$ [29]. The large operating voltage would ensure large depleted volumes even after radiation damage. To achieve this, the device was fabricated on very high resistivity p-type substrate ($> 2000 \Omega \cdot \text{cm}$) to ensure large depletion regions even at the highest fluences. Additionally, according to reference [30], the bias voltage is possible due to an optimised guard ring layout.

Of interest are also the passive HV-CMOS sensors designed within the same group that also exhibit high breakdown voltages. The structure of the sensors is similar to planar sensors, which will be discussed in the next section. Pixels in the study in reference [31] are passive i.e., contain no electronics, and the samples are therefore read out by bump bonding to a readout chip. This structure is very similar to hybrid pixel detector modules, except that an HV-CMOS process was used to fabricate an n-in-p sensing device. By modifying the structure with respect to figure 2.10, the breakdown voltage can be increased and therefore the radiation tolerance. The pixels (see figure 2.16a) measure $50 \mu\text{m} \times 50 \mu\text{m}$ (in line with the state of the art), whose structure follows a similar design as figure 2.10 above, with some modifications. Firstly, lots of space is left for the gap between pixel diode electrodes, just less than $10 \mu\text{m}$ for $50 \mu\text{m}$ pixels even with the largest deep n-well width of $30 \mu\text{m}$, assuming minimal sized so-called p-stop implants (the size of which are not specified). Simulations and confirmation with measurements described in chapter 4 of this thesis show that increasing this distance increases V_{BD} if p-stop is biased. Secondly, the samples were thinned from the backside and processed to allow backside biasing (not shown in the diagram). This was shown in reference [19] to increase charge collection efficiency with respect to non-thinned, topside biased detectors. And thirdly, a polysilicon field-plate (shown in grey in figure 2.16a) is used to evenly distribute high electric field that forms between the pixel diode electrodes and therefore increase the breakdown voltage [32]. This is described in more detail

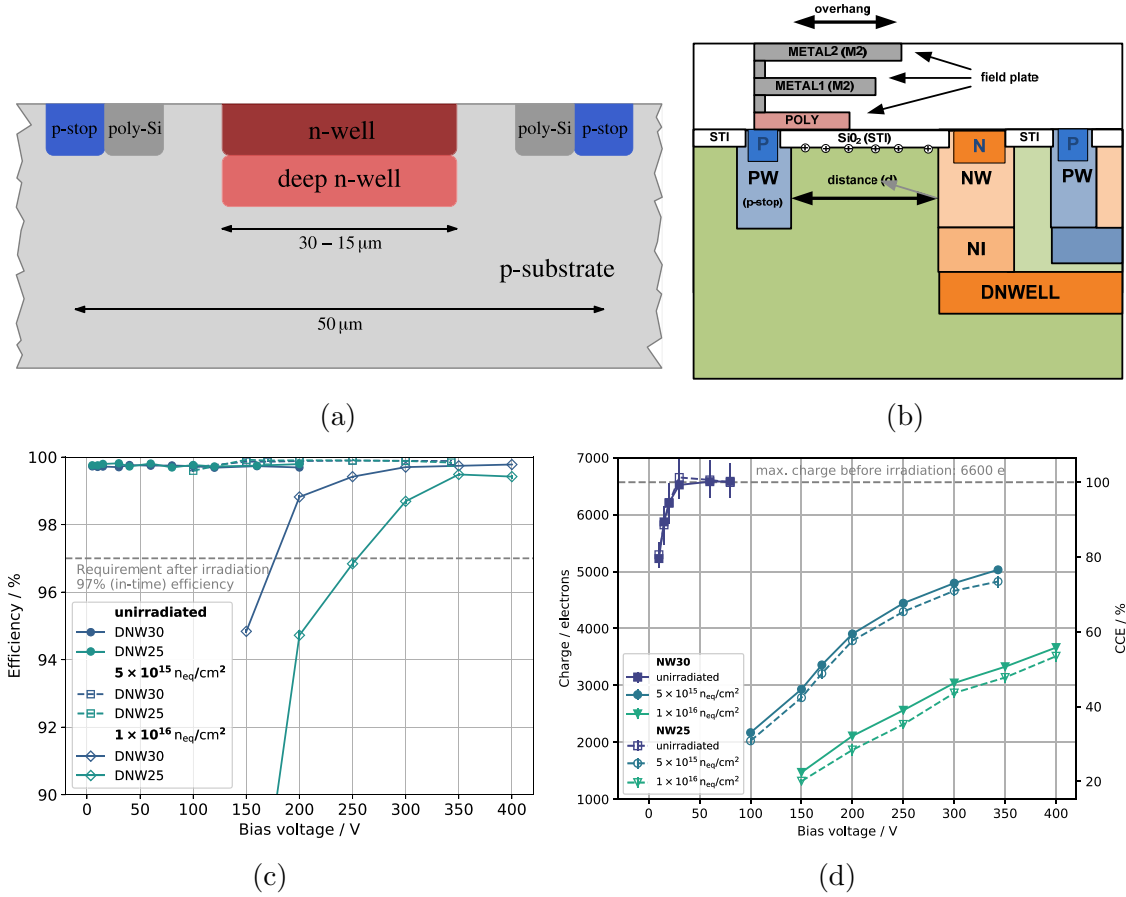


Figure 2.16: (a) Cross-section of one pixel with deep n-well in Monopix samples [31]. (b) Cross-section of sensor produced in LF15 technology from reference [33]. (c) Hit-detection efficiency of irradiated Monopix samples, produced in LFoundry 150 nm (LF15) technology [31]. (d) Charge collection efficiency of irradiated Monopix samples [31].

in the PhD thesis of one of the authors of the paper [33] and shown in figure 2.16b.

The study in reference [31] reports a hit-detection efficiency of $> 99\%$ and charge collection efficiency of 55% up to a fluence of $1 \cdot 10^{16} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$. This is achieved by ensuring samples can be biased to very high voltages: 220 V for non-irradiated samples, with no breakdown seen at 350 V for irradiated samples. This can be seen most clearly when analysing plots of the hit-detection and charge collection efficiencies, shown here in figures 2.16c and 2.16d. The hit-detection efficiency for the sample irradiated to the highest fluence is below their requirement (97%) at a bias voltage of 250 V. This can be increased to $> 99\%$ by increasing the bias voltage to 350 V, since no breakdown is observed. The charge collection efficiency follows the same linear trend described by equation 2.7. At 150 V bias voltage, samples irradiated to $1 \cdot 10^{16} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$ exhibit a CCE of 20% and increasing the bias voltage to 400 V can increase the charge collection efficiency to 55%.

A summary of the detectors discussed in this section is in table 2.2.

Table 2.2: Comparison of state-of-the-art HV-CMOS pixel detector parameters. ATLASPix3 was included as it is a predecessor of MightyPix.

Parameter	MuPix10	MightyPix	ATLASPix3	Monopix
Process	H18 (TSI)	H18 (TSI)	H18 (TSI)	LF15
Sensor size [mm ²]	20.2 × 23.0	≈ 20 × 20 [†]	20.2 × 21.0	3.8 × 3.8
Substrate resistivity [Ω · cm]	200	—	200	> 2000
Detector thickness [μm]	50	100–150 [†]	200	100
Pixel matrix	250 × 256	—	132 × 372	64 × 64
Pixel size [μm ²]	80 × 80	100 × 300*	150 × 50	50 × 50
Active area [mm ²]	20.1 × 20.0	(> 95%)	19.8 × 18.6	—
V _{BD}	100	—	—	220 (> 350)
NIEL [n _{eq} · cm ⁻²]	N/A	6.0 · 10 ^{14†}	—	1.0 · 10 ^{16‡}
TID [MRad]	N/A	40 [†]	—	580–660 [‡]

*50 × 150 being explored [26].

[†]Required [26].

[‡]Tested [31].

2.3.2 Hybrid pixel detectors

Generally, hybrid pixel detectors consist of two silicon layers, one for electronics and one for particle detection, that are bonded together using a technique called bump bonding. This process is known as hybridisation. The electronics chip is typically produced using standard CMOS processes, and the sensor can be produced using other bespoke technologies to ensure optimal performance, even after many years of use in high radiation environments. Hybrid pixel detectors are therefore placed very close to the beam in experiments not only because of their ability to withstand harsh radiation environments, but also their high precision tracking capabilities. The ATLAS and CMS experiments at CERN have used hybrid detectors from the start, and have implemented hybrid pixel detectors in the innermost regions of their experiments for R3 of the LHC sometime this year (2022). In addition, both ATLAS and CMS have opted to use hybrid detectors also during R4, which is currently projected for 2027. This section therefore outlines the structure of hybrid detectors and how they function in order to investigate possible improvements for HV-CMOS detector design.

2.3.2.1 The first hybrid detector

Figure 2.17 shows a diagram of the first hybrid pixel detector that was developed for the LAA project [34]. The electronics chip was fabricated in a $3\text{ }\mu\text{m}$ CMOS process and features a 9×12 matrix of $200\text{ }\mu\text{m} \times 200\text{ }\mu\text{m}$ pixels. Each pixel contains a pad for bump bonding, and a simple circuit consisting of an amplifier, comparator, and digital storage. The amplifier amplifies the signal created by impinging particles, which is sent to the comparator. The comparator either ignores signals below a certain threshold, or sends the signal for storage as a single bit, which connects the row and column lines “corresponding to the activated pixel”.

In measurements of the device, two types of $300\text{ }\mu\text{m}$ thick sensor chips were used: one $3\text{ mm} \times 3\text{ mm}$ chip with an array of $250\text{ }\mu\text{m} \times 250\text{ }\mu\text{m}$ diodes, and the other, a silicon-micron-resolution strip detector with a strip pitch of $100\text{ }\mu\text{m}$. Further details of the so-called *microstrip* detector used in the measurements were not given, but an example can be seen in figure 2.17b [35], developed for the NA11 experiment at CERN. The microstrip detectors in this experiment consist of a $280\text{ }\mu\text{m}$ thick n-type single-crystal silicon substrate, which is contacted through the back with an n+ implantation and metallisation. $12\text{ }\mu\text{m} \times 36\text{ mm}$ strips of p+ implantations with aluminium contacts are implemented on the topside, and separated by silicon dioxide.

Hybrid detectors have improved since they were first conceived in terms of decreased pixel size, lower power consumption, lower noise etc. and are still in use in current experiments and planned for use in future experiments. Some of the new hybrids for use in the CERN experiments are investigated below.

2.3.2.2 ATLAS hybrids

ATLAS [36] is a general-purpose detector searching for extra dimensions, supersymmetric particles and studying Higgs boson decays. The ATLAS detector consists of many layers of different types of detector for multiple purposes. The innermost detector, known as the Inner Detector (ID), is split into three sub-detectors of which, the innermost silicon pixels are hybrid pixel detectors which consist of the FE-I3 readout chip [37] bump bonded to a pixel sensor [11]. The pixel detector system in the ID was designed to last 10 years [38] and withstand a fluence of $1 \cdot 10^{15}\text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$ in the 10 years of operation, it will therefore not be upgraded until LS3 ready for R4 and R5. The following are therefore the parameters of the current detector.

The pixel readout chip FE-I3 was produced using a $0.25\text{ }\mu\text{m}$ CMOS process. It consists of an 18×160 matrix of $50\text{ }\mu\text{m} \times 400\text{ }\mu\text{m}$ pixels. Each cell contains a circuit very similar to the LAA hybrid detector but with some improvements. The charge signal from the sensor is amplified by an amplifier, this is sent to a discriminator with

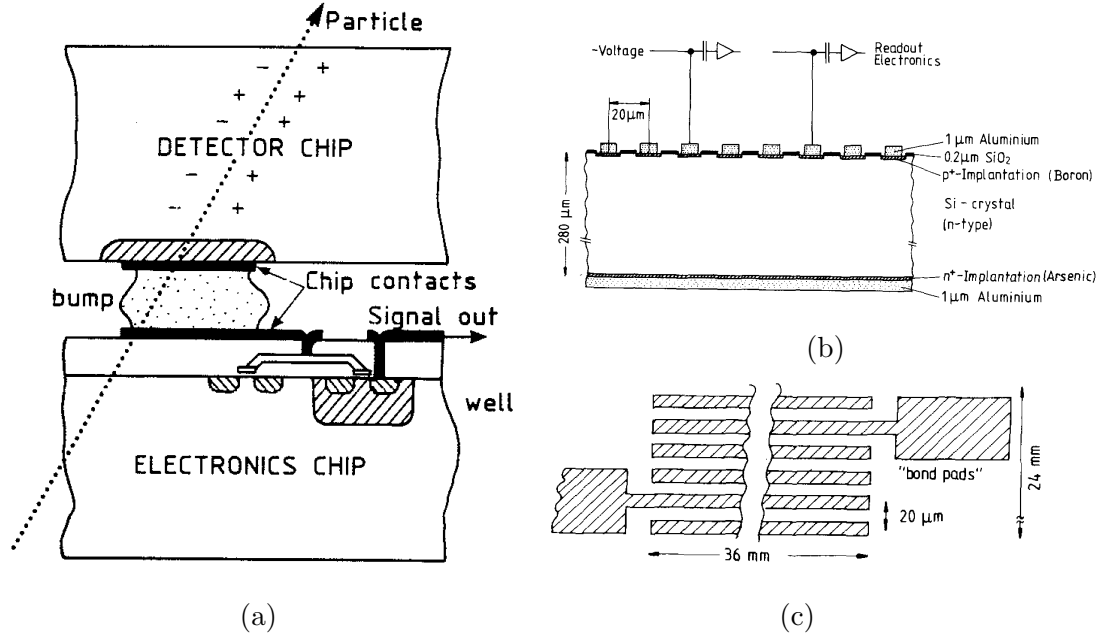


Figure 2.17: (a) Cross-section diagram of a hybrid detector developed for the LAA project from reference [34]. (b) Cross-section diagram of a microstrip detector [35]. (c) Top view of the strip pattern on a microstrip detector [35].

a programmable threshold, and the hit pixel address, hit time stamp, and digitised amplitude are sent to the periphery for further processing. This demonstrates what is possible when technologies with reduced node size are used, despite a reduction in the pixel area. To ensure a radiation tolerant design, a number of techniques were employed by the authors such as: ELTs (‘annular transistors’ in the paper); Single-Event Upset (SEU) tolerant latches are used to store bits; and each so-called ‘global configuration’ bit is stored in a type of Triple Modular Redundancy (TMR) system, where if one bit is flipped (for example by SEU), the other two are able to restore the correct value using majority logic.

The pixel sensor consists of a $256 \pm 3 \mu\text{m}$ thick, high resistivity (‘close to intrinsic charge concentration’) n-type wafer to which oxygen is added to improve radiation tolerance. The wafer is processed on both sides: A matrix of n+ implants form the pixels on the topside, which are $50 \mu\text{m} \times 400 \mu\text{m}$ due to the limitations created by the design of the electronics; and multiple p+ implantations on the backside form sensor guard rings and a large p–n junction which, when reverse biased, depletes the substrate from the backside (figure 2.18a). This differs from the typical design of HV-CMOS sensors in figure 2.10 above in which pixels are of opposite type to the substrate. According to the document, the sensor must be fully depleted for pixels to be isolated from each other, which according to measurements (figure 2.13a) is around 150 V. This is not the case for irradiated samples, however. During irradiation, p-type-like defects are introduced into the lattice (g_c term in equation

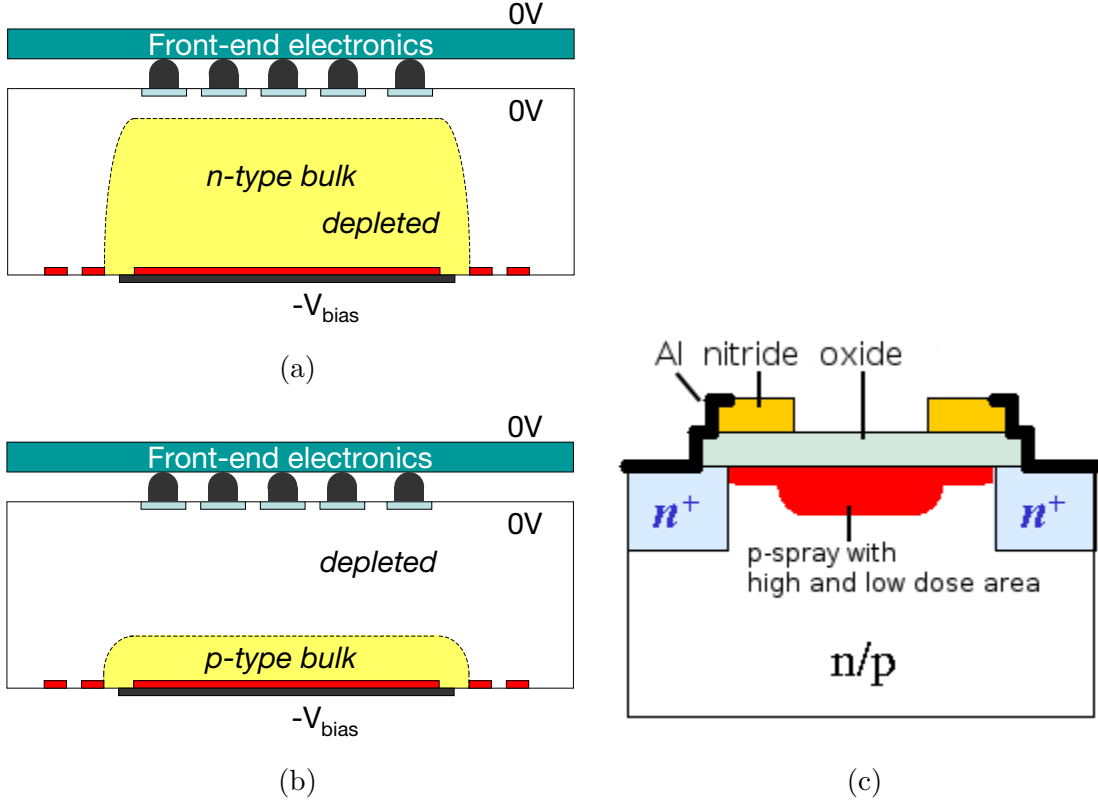


Figure 2.18: (a) Non-irradiated ATLAS hybrid detector. n-type bulk depletes from the backside where if $V_{bias} < 150$ V, pixels are not isolated. (b) Irradiated ATLAS hybrid detector after type inversion. Irradiation has introduced acceptor-like defects into the substrate rendering it p-type. Substrate now depletes from the topside and pixels no longer require full depletion for isolation. (c) Zoom of space between two pixels (n^+), which are isolated by p-spray implant. All images from reference [11]

2.5) which eventually causes the n-type substrate to effectively change to p-type (type inversion) and the p-n junction moves to the topside (figure 2.18b). Pixels are therefore isolated and no longer require full depletion, however operating voltages of up to 600 V are required for good CCE after ten years of operation [36]. Due to this type inversion effect, the authors of reference [39] suggested that oxygenated p-type substrate improves radiation tolerance.

Another detail of the pixels to be considered is a pixel-to-pixel isolation technique using a so-called p-spray or p-stop. Since both the pixels and substrate are n-type, a p-type dopant is implanted between the pixels to increase the resistance between them. This also aids with effects due to oxide charge at the Si-SiO₂ interface [40]. This study investigates two types of isolation: p-stop [41] a high-concentration implant as mentioned previously in Monopix HV-CMOS samples, and p-spray [42] a ‘medium’-concentration implant.

For what is called the ATLAS Phase-II upgrade, the ID will be replaced by the Inner Tracker (ITk) which will be made of hybrid $50\ \mu\text{m} \times 50\ \mu\text{m}$ pixel detectors [43]

close to the beamline and silicon strip detectors surrounding that. Details of the strip detectors will not be investigated here. The increase in luminosity will greatly increase the number of events and detectors will need to withstand the additional flux of $2 \cdot 10^{16} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$. A mix of two different technologies will be used for the sensor part of the hybrids: 3D sensors for innermost part where the fluence will be highest and planar sensors for the outermost part. These 3D inner layers will be replaced part way through the lifetime of the HL-LHC after a fluence of $1.3 \cdot 10^{16} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$ [44, 45]. These sensors have been designed to be compatible with the FE-I4 readout chip [46].

2.3.2.3 CMS hybrids

The Compact Muon Solenoid (CMS) experiment [47], is another general-purpose detector at the LHC and like ATLAS, is searching for supersymmetric particles and extra dimensions. The inner part of the experiment consists of silicon pixel detectors which surround the beam pipe. The original pixel detector was replaced by the new CMS Phase-1 pixel detector during the 2016/2017 technical stop of the LHC which should function until the end of R3. However, the innermost layer will have to withstand $3.6 \cdot 10^{15} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$ which is twice as high as its operational limits and will therefore be replaced during LS2. The pixel detectors are also hybrids, where planar silicon sensors are bump-bonded to a CMOS readout chip (ROC in this literature) [48]. The Phase-1 pixel detector is made up of two types of silicon sensor modules, BPIX and FPIX for the so-called barrel and forward disks, respectively. The innermost BPIX modules will be the focus here. Two ROCs were also designed: PSI46dig for the outer layers and PROC600 for the innermost layer. The details of which are given in references [49] and [50] respectively.

Specifics of the so-called planar sensor are given in reference [10]. The overall structure is very similar to the ATLAS sensors in the last section but is nevertheless reviewed here because of the detail provided. The substrate is $285 \mu\text{m}$ thick, oxygenated, n-type silicon with a substrate resistivity of $3.7 \text{ k}\Omega \cdot \text{cm}$. Pixels measure $100 \mu\text{m} \times 150 \mu\text{m}$, and are implemented using n+ implants, which are isolated from each other using p-spray. This is also to suppress shorting of pixels via the electron accumulation layer, according to the authors. This will be expanded upon in the next section. The authors also mention that the corners of pixel collection electrode implants are rounded to reduce electric field peaks, an effect that is investigated in simulations and measurements in the next chapter of this thesis. Overhanging field plates were not used to reduce electric field at the edges of pixels due to limitations of the metal layer and connections to each pixel, according to the authors. There is also a $180 \mu\text{m}$ wide n-type ring surrounding the pixels called the bias ring and a second large n-type area outside that, up to the scribe line. This second structure

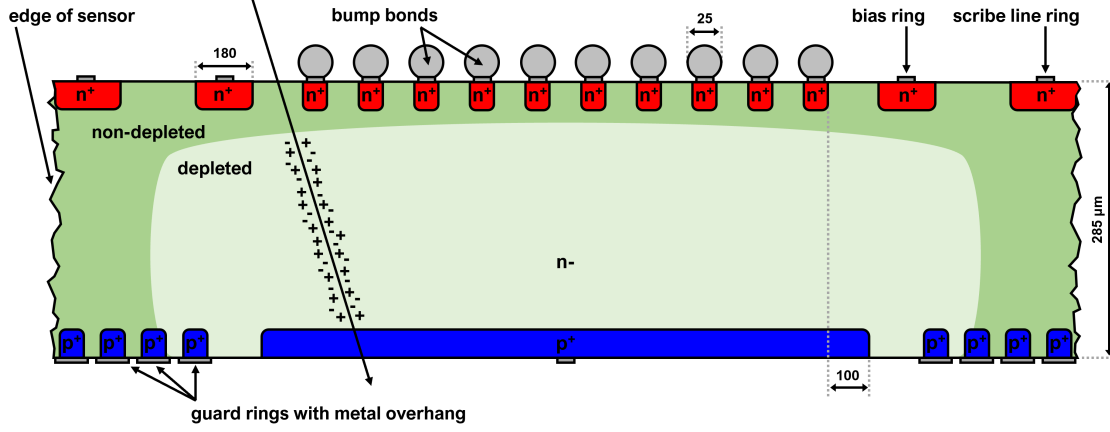


Figure 2.19: A labelled cross-section diagram of the sensor described in [10]. No cross-section diagram is given in the paper therefore this was created based on the information given.

serves two purposes. It is connected to ground to ensure the edge of the sensor is grounded and collects the current in the guard ring region. Again like the ATLAS sensors, the backside of the substrate is doped with a large p-type implant in the centre so that the depletion region extends upwards towards the pixels. The article details that this is surrounded by 16 concentric p-type guard rings in order to drop the potential at the edges of the sensor. These increase in distance from $10\text{ }\mu\text{m}$ to $50\text{ }\mu\text{m}$, with metal overhanging in both directions to reduce the electric field at the edge of implants. A cross-section diagram of the sensor is not given, but a diagram has been produced here based on the information given in the text (figure 2.19).

Then, during LS3 in 2024–2026, a new silicon tracker will be installed. It will have two components, the outer tracker (OT) made of silicon strips (and so-called macro-pixels) and the inner tracker (IT) made entirely of hybrid pixel detectors [43]. The IT is closest to the interaction point and will sustain a fluence of $2.3 \cdot 10^{16}\text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$. Pixel sizes are $50\text{ }\mu\text{m} \times 50\text{ }\mu\text{m}$ or $25\text{ }\mu\text{m} \times 100\text{ }\mu\text{m}$ and like ATLAS, will use 3D sensors for the innermost part of the IT and planar sensors where the fluence is lower. Both with a thickness of $150\text{ }\mu\text{m}$ [51].

2.3.3 MAPS

2.3.3.1 ALICE

ALICE [52] is dedicated to studying the strong interaction and quark-gluon plasma, a new phase of matter thought to exist immediately after the big bang. During LS2, the current Inner Tracking System (ITS) which uses a combination of silicon strip sensors, silicon drift sensors, and silicon hybrid pixel sensors was upgraded to the new Inner Tracking System (ITS2). According to reference [53] the ITS2 is composed entirely of CMOS Monolithic Active Pixel Sensors (MAPS) known as

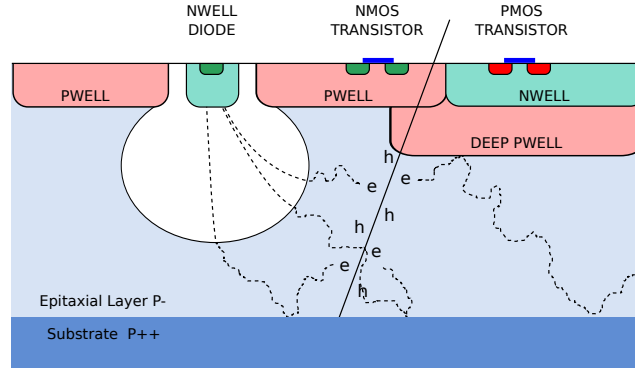


Figure 2.20: Cross-section diagram of the ALPIDE MAPS sensor from [57] produced in the 180 nm CMOS process from TowerJazz. The deep p-well allows isolation of PMOS transistors.

ALPIDE (ALice PИxel DETector). MAPS, like HV-CMOS, integrates the sensor and the readout electronics on a single chip reducing the material budget and improving vertex reconstruction and low momentum tracking.

ALPIDE is interesting because detectors are incredibly thin and pixels are incredibly small due to the technology node size. It is produced in the TowerJazz 180 nm CMOS process [54], which uses a $> 1 \text{ k}\Omega \cdot \text{cm}$ resistivity epitaxial layer on a p-type substrate which has a total thickness of $50 \mu\text{m}$ for the sensors closest to the beamline. The process provides a deep p-well to isolate PMOS transistors, allowing full CMOS in pixels (see figure 2.20). The pixel size for R3 will be decreased from $50 \mu\text{m} \times 425 \mu\text{m}$ to $29 \mu\text{m} \times 27 \mu\text{m}$. Simulations show the maximum accumulated NIEL over the lifetime of the detector will be $1.7 \cdot 10^{13} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$, and samples were verified up to $2.7 \cdot 10^{13} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$.

Then during LS3, preparing for the environment of R4, ITS2 will be upgraded to the new ITS3. Reference [55] presents interesting studies of wafer-scale MAPS detectors, with a pixel size of $15 \mu\text{m} \times 15 \mu\text{m}$ and reduced thickness of $20\text{--}40 \mu\text{m}$ which will mean wafers can be bent into curved cylinders. This removes the need for support structures, considerably reducing the material budget. The detectors will also be moved closer to the beamline which means particle flux will increase by 60% [56] and therefore radiation damage to detectors, which as the authors note, still remains below the level to which ALPIDE detectors were verified. Studies submitted to arXiv demonstrate that measurements of other properties of these detectors are currently ongoing.

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Table 2.3: Comparison of state-of-the-art detectors at CERN.

Parameter	ATLAS	CMS	ALICE
Technology	Hybrid	Hybrid	MAPS
Sensor size [mm ²]	—	18.6 × 66.6	15.0 × 30.0
Substrate resistivity [Ω · cm]	'close to intrinsic'	3700	> 1000
Sensor thickness [μm]	256 ± 3	285	50 [†]
Pixel matrix	144 × 328	52 × 80	512 × 1024
Pixel size [μm ²]	400 × 50	100 × 150	29 × 27
Active area [mm ²]	—	16.2 × 64.8	—
V _{BD}	> 500*	> 600*	'moderate'
NIEL [n _{eq} · cm ⁻²]	1.0 · 10 ¹⁵	3.6 · 10 ¹⁵	1.7 · 10 ¹³
TID [MRad]	—	120	2.7

*Irradiated detectors.

[†]Thickness of inner detectors, outer detectors are 100 μm.

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Chapter 3

Simulations of HV-CMOS pixels

3.1 Introduction

This chapter gives a detailed account of the methods used in this thesis to simulate HV-CMOS pixels and detectors using Technology Computer Aided Design (TCAD). TCAD is a tool able to simulate CMOS fabrication processes, and the electrical behaviour of many different materials. It can therefore be used to model silicon detectors and predict the performance of devices before fabrication, or to identify or verify any problems post-fabrication, due to radiation damage for example.

In this chapter, the LFoundry 150 nm HV-CMOS process [1] is studied in depth, as this is a common technology node used by designers in the CERN RD50 collaboration [2] for developing particle detectors. The doping concentrations of LFoundry implants have been reconstructed analytically to greatly decrease the simulation time required to model them with Monte Carlo (MC) methods. These simulated implants were used to reproduce a pixel from an RD50 HV-CMOS detector almost instantly. The quality of this technique was verified using reverse current–voltage (I – V) characteristic simulations and compared with a pixel simulated using a MC approach. The results from both methods are almost identical.

As a figure of merit, the breakdown voltage V_{BD} extracted from the simulations was compared with the expected value provided by the manufacturer. The mismatch was confirmed not to be due to the simulation method or choice of physics models. The analysis of the different reverse I – V characteristic simulation methods and available physics models provided in the TCAD software is also presented here. In order to match simulations with the expected value, refinements to the model were made at the device physics level, in the form of the addition of fixed oxide charges. The value of the expected V_{BD} was confirmed with measurements of a fabricated sample in chapter 4, which matches the simulations presented here.

Finally, a technique for extracting the simulated depth of the depletion region

is also presented, which has been improved with respect to the automatic tool provided in the TCAD software. This is most evident when the tool is used on pixels simulated to have sustained damage due to non-ionising radiation, where the tool no longer functions. The radiation damage model provided by the group in reference [3] is also summarised here, and applied to the same I – V characteristics and depletion depths simulations. The results show characteristics that resemble observations in measurements shown in chapter 5 which is encouraging. All simulations in this section and for the remaining chapters of the thesis have been performed at a temperature $T = 300$ K.

3.1.1 LFoundry 150 nm technology node

As mentioned in the previous chapter, for fully complementary HV-CMOS detectors a technology that includes methods for isolating both PMOS and NMOS electronics from the high-voltage substrate is required. CMOS Designers in the CERN RD50 group use the 150 nm technology node from LFoundry as it provides both deep buried p-type and n-type wells but also because high resistivity ($> 2000 \Omega \cdot \text{cm}$) substrates can be used, which maximises the size of pixel depletion regions.

The RD50 collaboration is a group within CERN, dedicated to research and development (R&D) of radiation tolerant semiconductor devices for high energy physics applications. Within RD50, there is a specific group that develops particle detectors fabricated in HV-CMOS technologies, which includes (but is not limited to) TCAD simulations, ASIC design, and characterisation of devices.

For TCAD simulations, the LFoundry 150 nm process is useful because the foundry also provides files containing simulations of their CMOS processes. This allows the designers to perform simulations of novel designs before fabrication to ensure they function as intended. In this chapter, all TCAD simulations presented have been performed using the LFoundry 150 nm process. This section briefly outlines the important aspects of the technology and gives an example of an HV-CMOS pixel designed by the RD50 group using the 150 nm technology.

3.1.1.1 Implants

The 150 nm technology node from LFoundry makes use of a p-type substrate (known as the p-substrate), available in a range of resistivities ($10 - > 2000 \Omega \cdot \text{cm}$). It includes an n-type well (NWell or NW) and a p-type well (PWell or PW) for PMOS and NMOS logic respectively, that can be powered using shallow, high concentration n-type (n+) and p-type implants (p+), respectively. In addition, there are two buried deep n-type wells NISO (N-type ISolation) and DNWell, and one buried deep p-type well PSUB. NISO and PSUB lie at approximately the same depth to allow

isolation of PWELL and NWELL respectively. DNWELL is the deepest which can be used to isolate p-type wells from the p-substrate.

3.1.1.2 RD50-MPW2

RD50-MPW2 is a Multi Project Wafer (MPW) submission in the 150 nm HV-CMOS process from LFoundry. The chip was submitted and designed by the CERN RD50 collaboration in February 2019 for particle physics experiments. The design effort performed as part of this thesis will be given in the next chapter. A cross-section diagram of one of the active $60\,\mu\text{m} \times 60\,\mu\text{m}$ pixels is shown in figure 3.1a (diagram adapted from reference [4]). The cross-section of a passive $50\,\mu\text{m} \times 50\,\mu\text{m}$ pixel implemented for testing is shown in figure 3.1b. The spacing between the pixel electrodes was decreased from $8\,\mu\text{m}$ to $3\,\mu\text{m}$ with respect to figure 3.1a to match the geometry of a previous submission RD50-MPW1 [5]. More information about that study will also be given in the next chapter. TCAD simulation studies in this chapter are based on this second cross-section.

Like the diagram of a typical HV-CMOS pixel (HV-CMOS pixel) given in the previous chapter (figure 2.10), the p-substrate (anode) and DNWELL (cathode) form the p-n junction which makes the pixel diode. The diode is reverse biased by biasing the p-substrate to a negative high voltage through the p+/PWELL stacks on the outer edges of the pixel and the DNWELL is biased through the n+/NWELL/NISO stacks to 0 V (or a low, slightly positive voltage). As the potential difference across the electrodes is increased, the depletion region grows mostly into the lighter doped p-type substrate, which forms the sensitive area for particle detection. The DNWELL is also used in combination with the n+/NWELL/NISO stack ring to isolate NMOS electronics from the high voltage p-substrate. Subsequently, the PSUB layer is used in combination with its own p+/PWELL stack ring to isolate PMOS electronics from the DNWELL. It should be noted that the cross-section in figure 3.1a differs from the diagram in the previous chapter in a few ways. Firstly, the area of the PSUB layer was slightly reduced to decrease the PSUB-DNWELL capacitance (work described in reference [4] for a previous chip submission). Secondly, the n+/NWELL/NISO stack on the right-hand side which is slightly wider to include room for signal amplification and sensor biasing electronics.

The cross-section of the pixel from figure 3.1b was simulated using the Synopsys® Sentaurus TCAD tool [6], based on the method described in reference [7] with some modifications which will be described in the next section. Firstly, the TCAD tools used in this chapter will be briefly introduced.

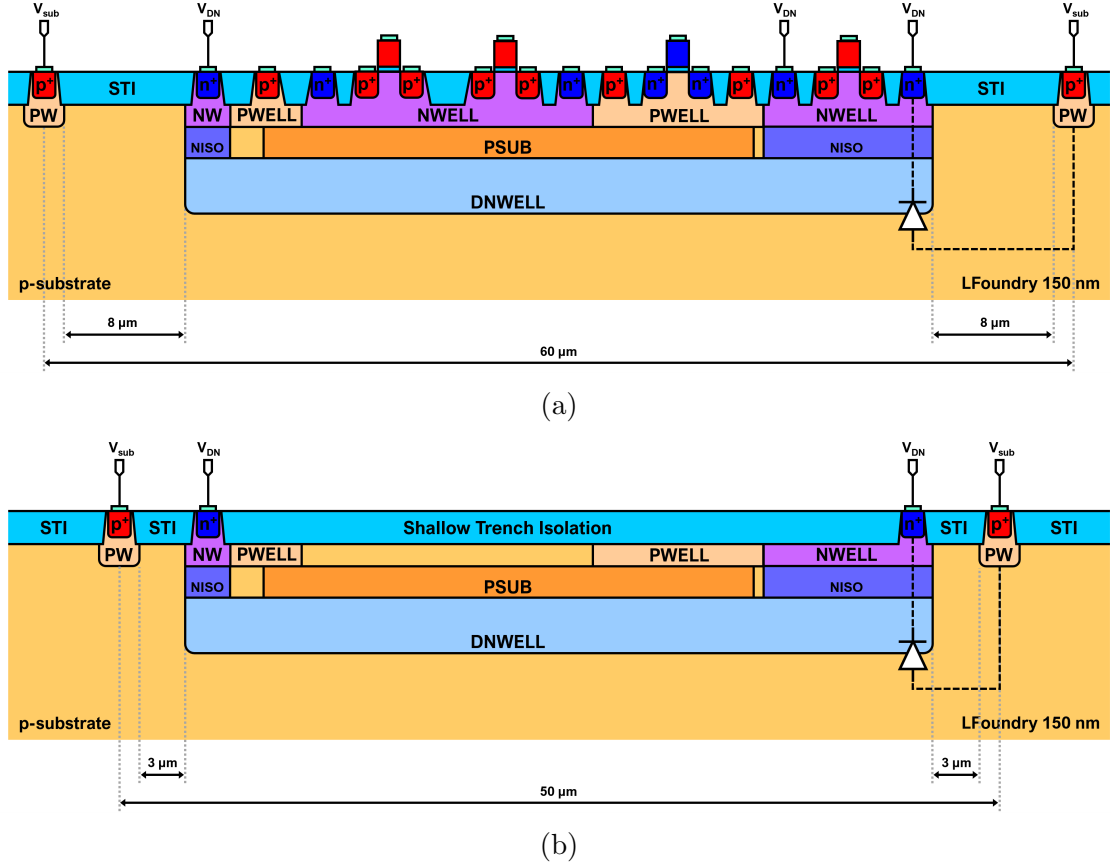


Figure 3.1: (a) Cross-section diagram of an active pixel from RD50-MPW2. The deep p-well (PSUB) is slightly narrower and the NWELL/NISO stack on the right is slightly wider with respect to figure 2.10. Respectively, this is to reduce the PSUB–DNWELL capacitance, and include amplification and biasing electronics [7]. (b) Cross-section diagram of a passive pixel from RD50-MPW2 that was used in this TCAD study. The geometry matches that of pixels in a previous submission RD50-MPW1 (note the decreased electrode pspacing).

3.1.2 TCAD tools

Sentaurus from Synopsys is a TCAD tool suite used to simulate semiconductor technologies. Put simply, tools are separated into two types: *structure generation* and *device simulation*. Tools such as Sentaurus Process are able to simulate CMOS process technologies such as etching, deposition, and implantation, to create the desired electrical component or structure. Sentaurus Device, another tool, is able to simulate the electrical behaviour of a device, analogous to performing an experiment or measurement in a laboratory. Tools are typically arranged into workflows, the output of the Sentaurus Process simulation, a p–n junction diode for example, is fed directly into the Sentaurus Device simulation, which could produce device characteristics such as I – V curves. The main tools used in this study will be discussed in more detail in the following sections.

As simulations, naturally both structure generation and device simulation tools

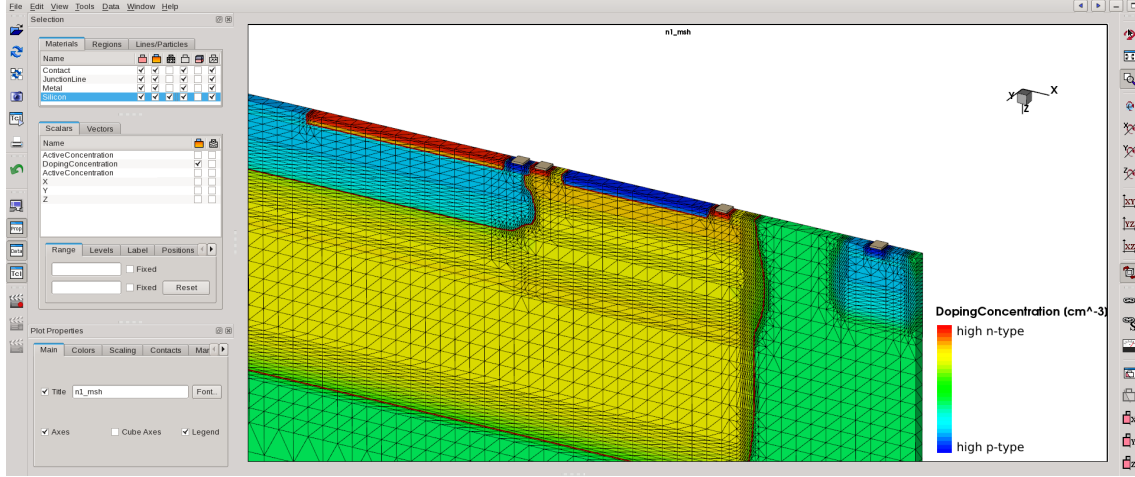


Figure 3.2: Screenshot of TCAD visualisation software.

are approximations of reality. Each tool uses numeric methods that require the device to be spatially discretised. This is performed by a *mesh* generator. An example of a mesh can be seen in figure 3.2. For semiconductor devices such as this, continuous properties like doping concentration are represented on a grid of points, with values in between those computed using interpolation. The mesh must be densest in regions of the device where for example high electric fields are expected, such as at p–n junction interfaces to properly resolve avalanche generation of charge carriers, for example.

3.1.2.1 Process simulations

Sentaurus Process is a structure generation tool in the Sentaurus TCAD suite. It simulates semiconductor device fabrication processes such as ion implantation, metal deposition, oxide growth, etching etc. As an example in the context of HV-CMOS detector research, the tool can be used to simulate all the processing steps necessary to form a pixel. Starting from a doped volume of silicon, a user can provide the dopant species, beam doses, and beam energies, to multiple implant commands to generate p- and n-type wells in the silicon at the desired concentration and depth using full atomistic MC simulations. This will be seen in more detail in this chapter. In addition to this, mechanical action on the silicon can be simulated, such as etching which is a fundamental step in the formation of STI (see figure 3.3). It is also possible to simulate photolithographic processes. Photoresist can be positioned manually, or GDS files (Graphic Design System, industry standard IC design files) can be imported to the software to automatically generate masks. In this way, structures can be created with little user intervention.

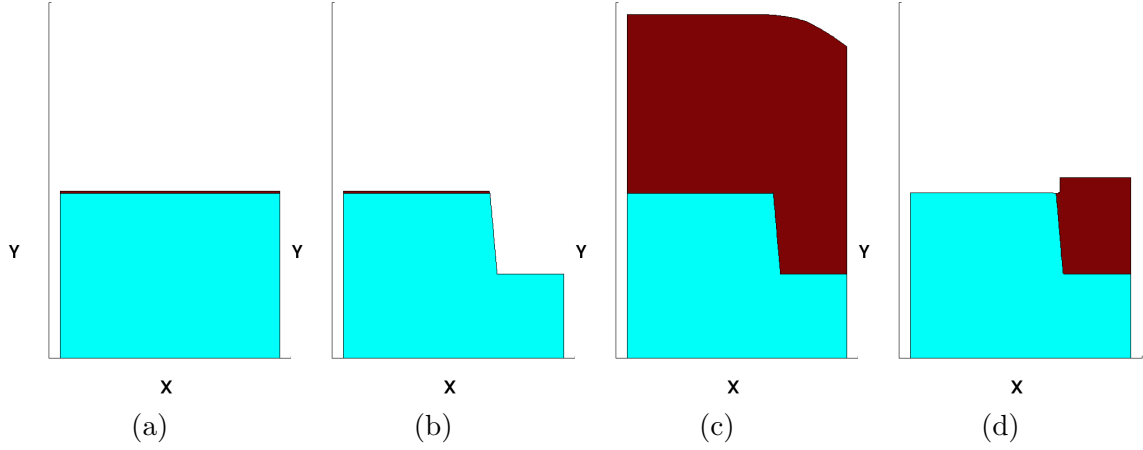


Figure 3.3: Sentauros process simulation of STI formation. (a) Initial silicon crystal (blue) with thin SiO₂ layer (brown). (b) Trench etching step. (c) Oxide deposition step. (d) Remaining oxide etching step.

3.1.2.2 Structure simulations

Sentauros Structure Editor is another structure generation tool however, structures are defined geometrically rather than through simulation of fabrication processes. In 3D space, devices are constructed by combining shapes such as cuboids or extrapolating from 2D faces. More complex geometries can be created by adding or subtracting basic forms and rounding edges using filleting or chamfering, similar to ‘traditional’ CAD. Within the tool, it is also possible to simulate ion implantation to fully model semiconductor devices. An example of this is shown in figure 3.4. Typically, 2D simulations are performed to save computing time, but the third dimension (y , in this case) has been extended for visual aid. A deep silicon substrate was defined using a simple cuboid (pink), then doping windows (equivalent of the negative space of a photolithographic mask) were defined on the topside of the silicon using rectangles (green). 1D concentrations of dopants or doping profiles must then be applied to the silicon in the vertical (z) direction, to form wells only in those areas where the windows are specified. This will be expanded upon in this chapter.

3.1.2.3 Device simulations

Sentauros Device is the final main tool used in this study. As the name suggests, this is a device simulation tool, which is used to simulate the characterisation of semiconductor devices, analogous to performing experiments on devices in a laboratory. The electrical behaviour of individual devices can be simulated, or devices can be combined in a circuit with or without other simulated devices (see figure 3.5). Before Sentauros Device can be used to perform experiments however, it must know the geometry of the device, the materials it is made from, and the concentrations of dopants in the semiconductor. Therefore, structure generation tools such

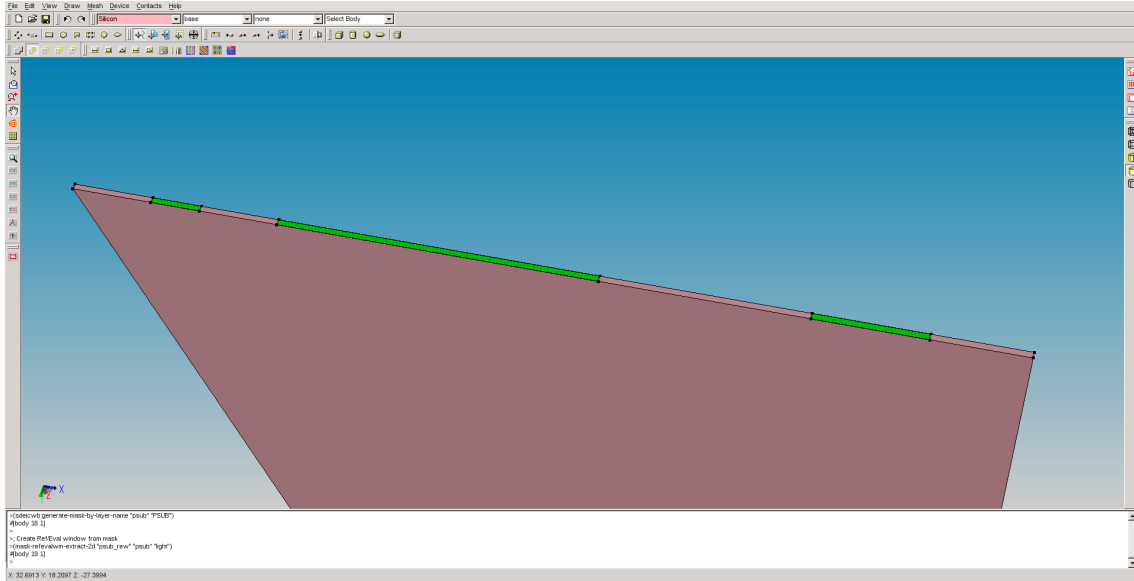


Figure 3.4: Screenshot of Sentaurus Structure Editor software used to construct an semiconductor device. The silicon substrate is shown in pink and doping windows are shown in green where 1D doping profiles can be applied to form implant wells.

as Sentaurus Process or Sentaurus Structure Editor must be used first. In addition, the tool can be told which physics models to account for, which can be selected depending on if the user requires accuracy or computing speed. Models chosen govern physical phenomena such as behaviours of charge carriers within the lattice and at interfaces, carrier generation and recombination processes, and carrier charge trapping. An in-depth study of available physical models for reverse breakdown (i.e., avalanche generation) of a diode for example, is presented in this chapter.

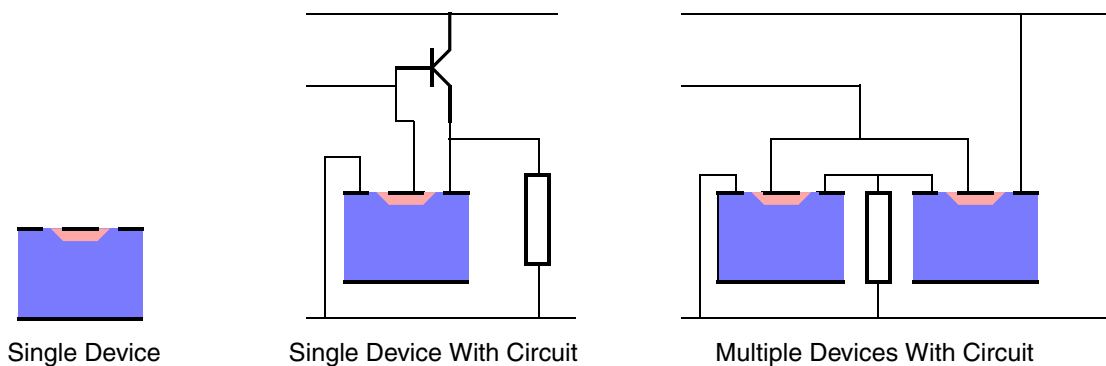


Figure 3.5: Diagram demonstrating three types of simulation in Sentaurus Device. The semiconductor structure simulated with Sentaurus Process or Sentaurus Structure Editor can be simulated by itself (Single Device), as part of a circuit, or with other instances of TCAD structures in a circuit. From reference [8]

3.2 TCAD simulations of a single pixel

The cross-section of a pixel from RD50-MPW2 (figure 3.1b) was simulated using the Sentaurus TCAD tool suite from Synopsys® [6]. The method presented here is based on the method described in [7] with some modifications which will be explained in this section. As suggested by the author, the doping profiles were improved in this work, by characterising them with fitting functions using ROOT [9]. Small process simulations of all the individual implant types in the LFoundry 150 nm technology (NWell, PWell, NISO etc.) were performed using Sentaurus Process. Vertical and lateral doping profiles were sampled from these simulations and fitted with mathematical functions. These individual functions were recombined in Sentaurus Structure Editor to construct a pixel.

The main goal of this chapter is to demonstrate that given mathematical definitions of the doping concentrations of implants, a simulated HV-CMOS pixel can be generated very quickly and very accurately using Sentaurus Structure Editor. This was verified by generating the same structure with Sentaurus Process (the ideal case) and comparing results of reverse I - V characteristic simulations performed using Sentaurus Device. The results are very similar despite the much shorter simulation time required to generate the structure in Sentaurus Structure Editor.

This suggests that this method could be used to generate any type of structure possible in the LFoundry 150 nm technology accurately, without the need for time-consuming process simulations. This methodology could also theoretically be repeated for any technology node given the necessary inputs for implantation process simulations therefore not limiting this work to the LFoundry 150 nm node.

3.2.1 Structure simulation of a pixel

For simulation purposes the cross-section in figure 3.1b was chosen for a number of reasons. Firstly, it includes all implant types, which means the validity of this study can be tested on all of them. Secondly, it included contacts to the pixel electrodes which are necessary for accurate electrical simulation in Sentaurus Device. Thirdly, the cross-section includes the wider NWell/NISO stack on the right-hand side, to investigate possible asymmetries in the design. Finally, there are no contacts to the central PWell and PSUB layers that are isolated from the p-substrate by the DNWell. This last point was to keep simulation time to a minimum as the complicated shape of the STI, and the high doping concentration gradient of the p+ wells creates many more mesh nodes, and increases simulation time of this already very large simulation.

In contrast to the method in [7], it has been assumed here that most of the structure is in fact, covered by shallow trench isolation (STI), which is important

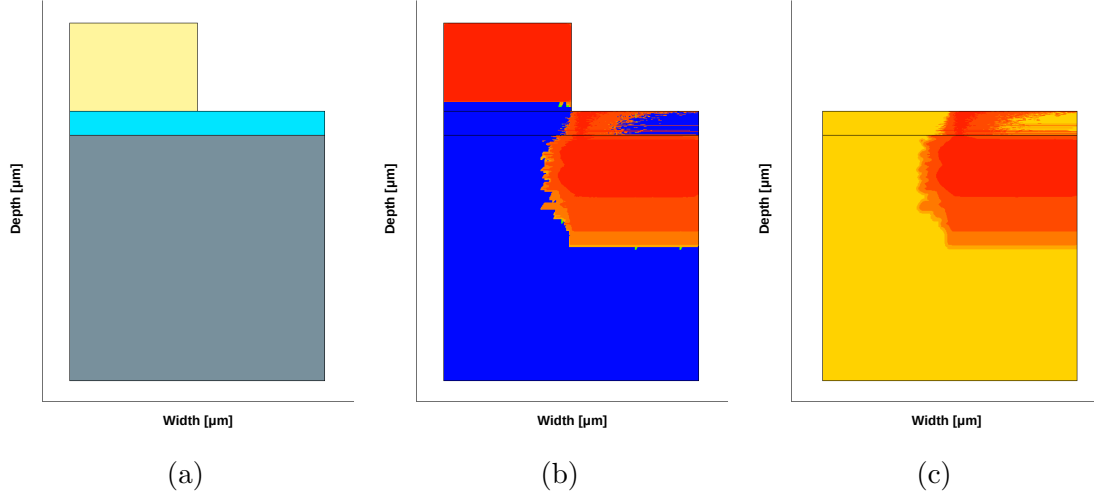


Figure 3.6: (a) Example Sentaurus Process simulations to demonstrate the concept of the small process simulations. This is not an LFoundry 150 nm implant. (a) Small region of silicon (grey), covered with a thin layer of silicon dioxide (blue), and photoresist (beige), covering half of the structure. (b) Same structure after ion implantation simulation, showing areas of high and low dopant concentration. (c) Same structure after photoresist etching and annealing steps.

as the final doping profiles are changed, and therefore the doping concentrations of the implants which affects parameters such as V_{BD} . The difference between doping profiles with and without STI is revealed when compared with simulations of the same test structure pixel cross-section produced with Sentaurus Process.

3.2.1.1 Process simulations of individual wells

A Sentaurus Process simulation of the LFoundry 150 nm HV-CMOS process was provided by the foundry. It contains simulated process steps, such as implantation, annealing, and etching. It is possible to provide a GDS file of any IC design and run this through the simulation deck to create any structure. However, since the pixel is $50\text{ }\mu\text{m}$ wide, a Sentaurus Process simulation of this size would take many hours to run, even with a capable computer. Therefore here, for each well type offered by the foundry, a small 2D simulation was created. This had to be large enough to characterise the full 1D vertical doping profile, and estimate the lateral doping profile of each well type, but small enough to keep simulation time to a minimum. Using a dummy well as an example, the following section describes the method used to extract the doping profiles of individual wells from Sentaurus Process, which are then fitted with functions using ROOT. For this example, false implant energies and doses were used and the species hidden to convolute processes kept confidential by the foundry. The small process simulation can be seen in figure 3.6.

Figure 3.6a shows the small area of silicon that was defined, with initial resistivity

set to $10\ \Omega \cdot \text{cm}$, which is the standard substrate resistivity provided by the foundry. As a note, studies of HV-CMOS sensors include using high resistivity substrate to maximise the size of the depletion region. It is assumed here that the implant energies and implant doses do not change with substrate doping. A thin layer of silicon dioxide was placed on top of this to account for the STI. This is important as etching and oxidation steps are performed before implantation, and the mean energy loss of charged particles through the STI is not negligible and changes the final doping profile in the silicon due to the combined stopping power of the different materials [7]. This can be seen in figure 3.7a. The implantation with STI is shallower and has a higher concentration. The multiple peaks seen in both curves arise from implanting dopant ions with different energies. In this case, there are two main peaks as two different implant energies were used.

A photoresist layer thick enough to block the implant was applied to half of the structure, in order to recreate the conditions at an implant interface as the doping profile in the lateral direction also needs to be accounted for. A mesh was defined with finer concentration at the top of the simulation to ensure the doping profile could be properly sampled near the final implant region. In figure 3.6b, the same structure can be seen after a MC ion implantation simulation with a dopant. A well has formed in the region of silicon that is not covered by photoresist. However, there is some lateral extension of the well into the region covered by photoresist. Dopant can also be seen in the silicon dioxide near to the photoresist. Both of these phenomena are due to scattering of dopant ions.

Figure 3.6c shows the structure after photoresist etching and annealing steps. Annealing steps were performed that would account for all annealing steps that the foundry does for their various process steps. This is important as annealing changes the final shape of the doping profile described in the next section. The well boundaries are smoother and there is now also a low concentration of the dopant throughout the structure.

Vertical doping profiles

To mathematically characterise each implant, first the doping concentration was sampled in the vertical (depth) direction. This was achieved by extracting a 1D doping profile from the simulation of each implant. A comparison of the doping profiles before and after annealing can be seen in figure 3.7b. A smooth curve is shown here so it is easier to see the difference, but in reality, these doping profiles are sampled at points along the mesh. The vertical slice of the simulation after annealing was then imported into ROOT. In this case a superposition of Gaussian functions were fit to the vertical doping profiles. But error functions are also used for other implant types as these are the functions that are available in Sentaurus

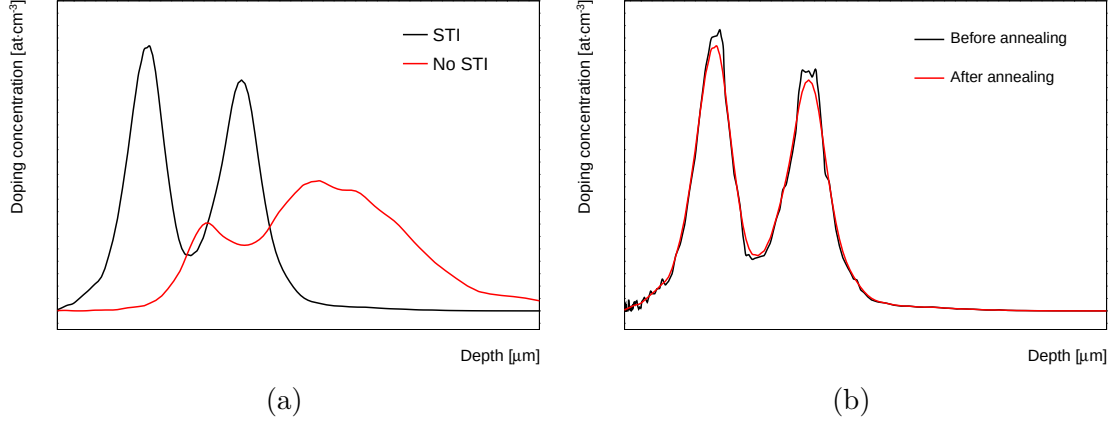


Figure 3.7: (a) Comparison of doping profiles of the same well type after annealing, with and without STI. (b) Comparison of doping profiles of the same well type with STI, before and after annealing.

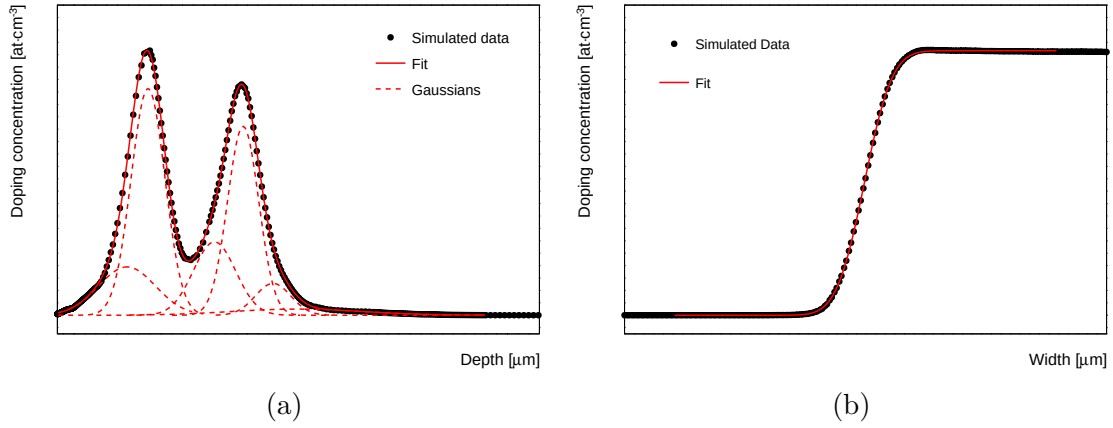


Figure 3.8: (a) Vertical doping profile after annealing fit with equation 3.1. (b) Lateral doping profile at the peak depth after annealing, fit with equation 3.2.

Structure Editor when defining doping profiles. The number of Gaussians, initial fitting parameters, and fitting parameter limits were chosen by eye, but the fitting was handled by ROOT. In the case of figure 3.8a, the fitted function was simply

$$N(z) = a_1 \exp\left(\frac{(z - \mu_1)^2}{-2\sigma_1^2}\right) + a_2 \exp\left(\frac{(z - \mu_2)^2}{-2\sigma_2^2}\right) + \dots + a_n \exp\left(\frac{(z - \mu_n)^2}{-2\sigma_n^2}\right) \quad (3.1)$$

where N is the doping concentration, z is the depth, n is the number of Gaussian functions and a , μ , and σ are the fitting parameters, peak height, mean, and standard deviation of the Gaussian functions respectively. In this case $n = 6$, which was chosen arbitrarily to make fitting easier, it could therefore be possible to use less. The fitted parameters were then extracted from ROOT and fed into Sentaurus Structure Editor.

To test the general concept, the same structure as the Sentaurus Process simu-

lation in figure 3.6c was reconstructed in Sentaurus Structure Editor. A region of silicon with the same dimensions was defined and the resistivity was set by applying a uniform doping profile with concentration calculated using reference [10], assuming a temperature of 300 K. A vertical doping profile was applied to the silicon by defining a linear, so-called reference/evaluation (ref/eval) window on the right half of the simulation, on the surface on the substrate. Doping profile parameters were set equal to those extracted from the fit (equation 3.1) shown in figure 3.8a. The resulting simulation is displayed in figure 3.9a. A vertical doping profile was extracted from this simulation and compared with the original vertical doping profile from Sentaurus Process shown in figure 3.9b. The profiles are very similar demonstrating the function fit in ROOT and imported into Sentaurus Structure Editor was acceptable. The silicon dioxide was added to make the final comparison clearer and has no effect on the doping in this case. It can be seen that the vertical doping profile leaves an abrupt boundary at the ref/eval window interface, which is unphysical, as seen in the process simulations in the last section which showed some movement of dopants in the lateral direction. When compared with figure 3.6c, there is no lateral extension of the doping. In HV-CMOS pixels, this extension decreases the effective distance between neighbouring wells which has some important effects that will be seen later. It must therefore also be modelled.

Lateral doping profiles

At the location of the maximum doping concentration in figure 3.9a, a 1D horizontal slice of the doping profile from Sentaurus Process was also extracted and imported into ROOT. This can be seen in figure 3.8b. Since it takes the shape of an error function it was fitted with

$$N(x) = \frac{N_{max}}{2} \cdot \left(\operatorname{erf}\left(\frac{x - x_0}{L}\right) + 1 \right) \quad (3.2)$$

where N_{max} is the maximum doping concentration, x_0 is the centre of the simulation which is also the position of the edge of the photoresist, and L is the diffusion length of the profile known in Sentaurus Structure Editor as the Lateral Diffusion Factor (LDF). L was then extracted and imported into Sentaurus Structure Editor. The final comparison can be seen in figure 3.10. Figure 3.10b could be improved by taking more lateral samples, fitting more error functions and using different L values for each Gaussian in equation 3.1.

A comparison of simulation times can be seen in table 3.1. It can be seen that a Sentaurus Structure Editor simulation takes much less time to run than a Sentaurus Process simulation. The times here do not include the time taken for extracting and analysis of doping profiles, which is important to consider. However, it can be easy

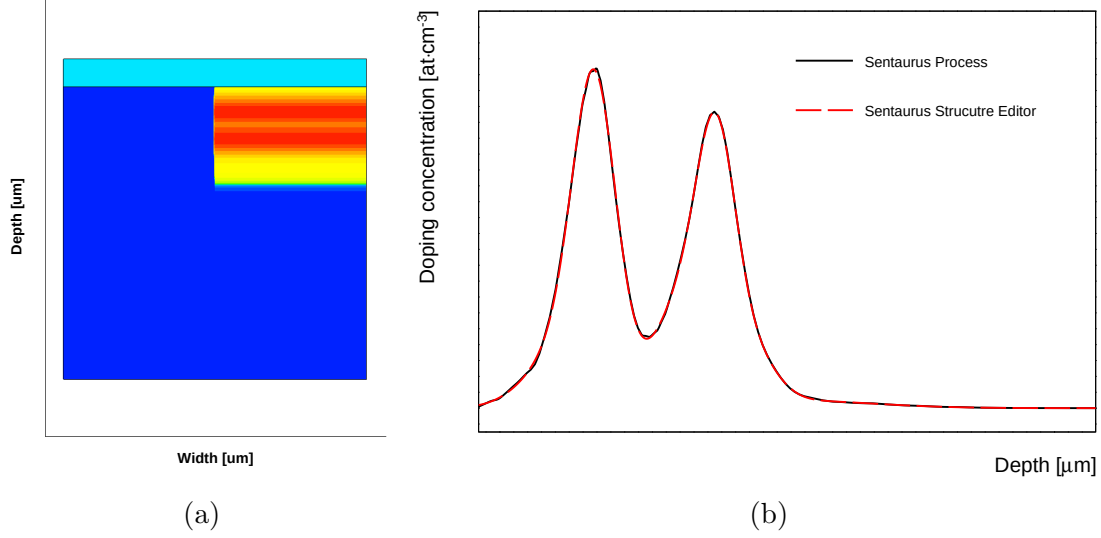


Figure 3.9: (a) Doping concentration of Sentaurus Structure Editor simulation. (b) Comparison of Sentaurus Process vertical doping profile with doping profile extracted from the Sentaurus Structure Editor simulation.

to imagine once the doping profiles for all wells are properly characterised, creating very large simulations with different, potentially complicated structures becomes much more manageable than would have been in Sentaurus Process. Something that will be seen in the next section.

	time [h]
Sentaurus Process	04 : 40 : 46
Sentaurus Structure Editor	00 : 01 : 28

Table 3.1: Times taken for simulations in figure 3.10 to run.

3.2.1.2 Structure simulation combining wells

To demonstrate that the implants can be characterised separately and then combined into other structures successfully, computing time was dedicated to performing a very large Sentaurus Process simulation of an entire pixel. To create an accurate simulation of one pixel, a GDS file of a passive pixel from RD50-MPW2 test structures was imported into Sentaurus Process using the Sentaurus IC WorkBench Edit/View Plus (ICWBEV Plus) tool. 2D masks were created from all the layers of the pixel (PWELL, NWELL, etc.) and then imported into the Sentaurus Process simulation that was provided by LFoundry. This simulated cross-section produced by the LFoundry Sentaurus Process simulation deck can be seen in figure 3.11a. The colour of the plot represents doping concentration, where dark blue is high p-type concentration (p+ wells) and red is high n-type concentration (n+ wells). A large, 2D region of silicon of width 150 μm and depth 280 μm was defined as the

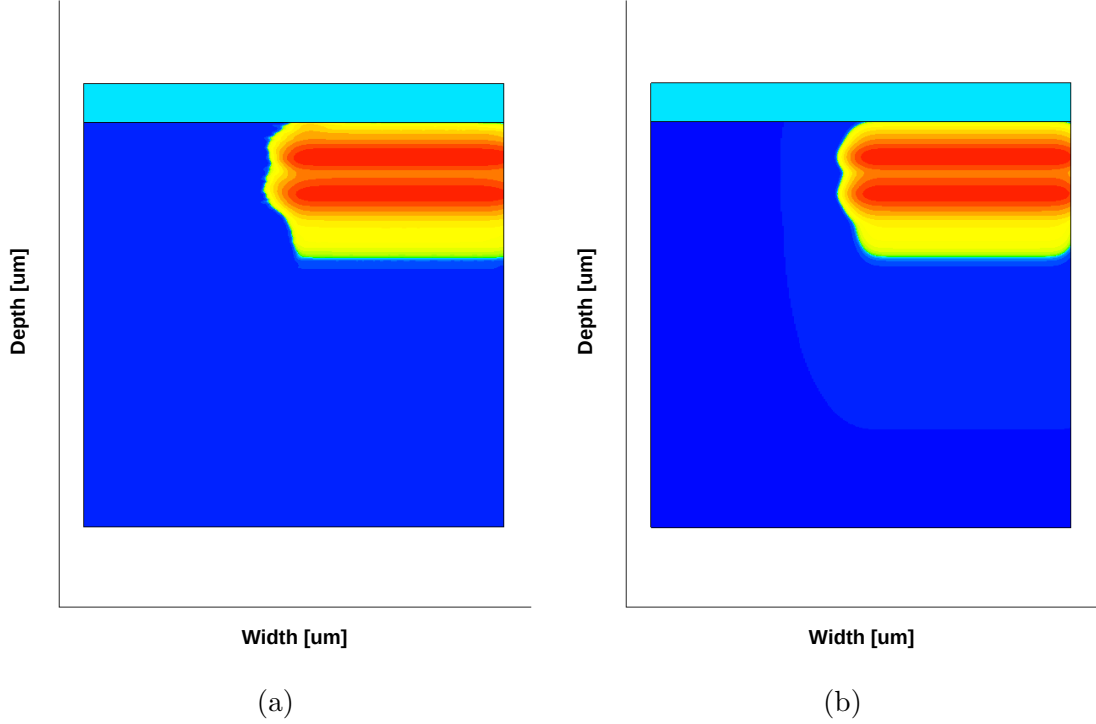


Figure 3.10: (a) Final doping concentration of Sentaurs Process simulation. (b) Sentaurs Structure Editor version with imported vertical doping profiles and lateral profiles.

p-substrate, which was set to a resistivity of $1900 \Omega \cdot \text{cm}$ by doping with boron. It is therefore displayed in green as the p-type concentration is relatively low when compared to p+, for example. The actual doping concentration values, and the scales of the x and y axes have been removed to protect confidential information. One of the scales has also been distorted in all following images so that the depth of wells cannot be inferred from the known width of the pixel. It can be seen that most of the topside of the simulation is covered in STI (shown in blue with a black outline), in contrast to the assumptions made in [7]. In addition, where there are ‘openings’ in STI (where n+ and p+ wells are implanted), it can be seen that the implants travel much further into the substrate. This can be seen most clearly near the outer edges of the DNWELL, but also in the outer PWELLS.

The pixel cross-section, reconstructed in Sentaurs Structure Editor using the doping profiles described in the previous section can be seen in figure 3.11b. Using the same parameters as figure 3.11 a large, 2D region of silicon ($150 \mu\text{m} \times 280 \mu\text{m}$) was defined, and the resistivity was set to $1900 \Omega \cdot \text{cm}$ by defining a constant doping profile with boron concentration set to $6.986 \cdot 10^{12} \text{cm}^{-3}$ [10]. STI was also included in the simulation by defining isosceles trapezium regions of silicon dioxide, where the height, and difference in length between the parallel edges were extracted from the Sentaurs Process simulation by eye. These were defined inside the silicon region,

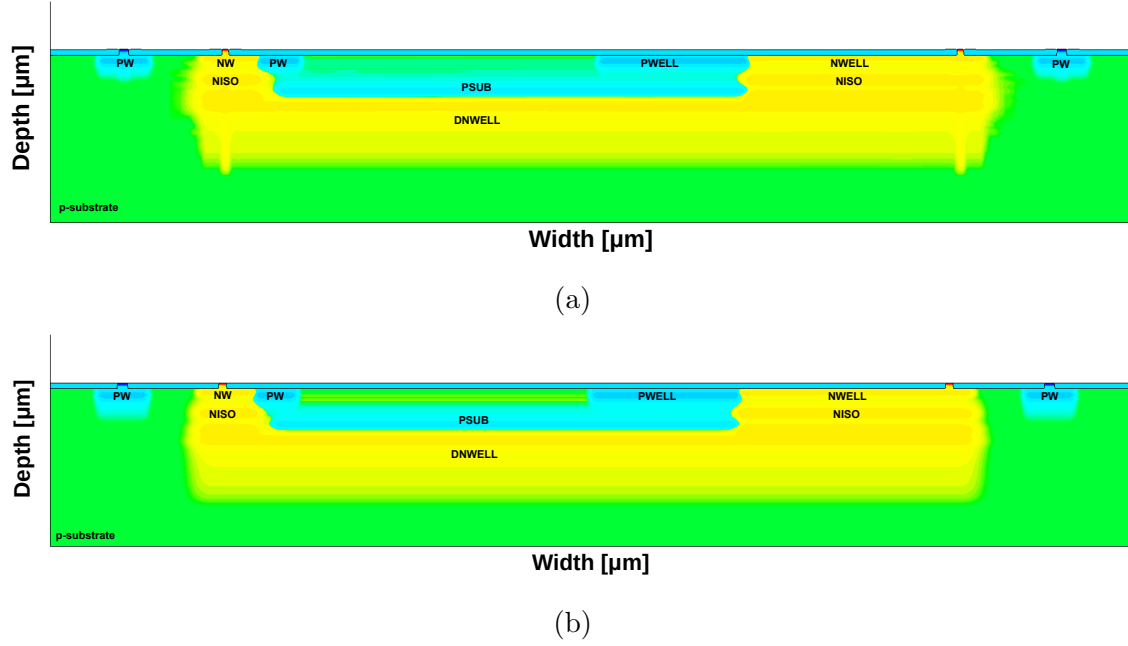


Figure 3.11: (a) Time-consuming Sentaurus Process simulation of the pixel cross-section shown in figure 3.1b. (b) Fast, accurate recreation of the same pixel cross-section using Sentaurus Structure Editor and doping profiles extracted from Sentaurus Process simulations of individual implants.

with overlap behaviour set to “New Replaces Old” to mimic the effect of silicon etching and oxide growth. The implants (NWE, PWE etc.) were introduced into the substrate by defining linear ref/eval windows on the topside of the substrate, parallel to the surface. The positions of the wells were calculated from the GDS file and input manually. This method could be improved by importing the GDS file and creating masks using ICWBEV, similar to the Sentaurus Process method. Then the vertical doping profiles (and LDFs) extracted from the Sentaurus Process simulations in the last section were placed in their corresponding windows.

In both simulations, contacts were implemented by assigning contact labels to the exposed edges of the substrate created between two STI regions. The two substrate contacts were given the same label “ V_{HV} ” and the two DWELL contacts were given the same label “ V_{DN} ” to ensure corresponding contacts are always at the same voltage in Sentaurus Device simulations described in the next section. The first thing to notice when comparing the two simulated pixel cross-sections is that the doping due to the “openings” in STI seen in the Sentaurus Process simulation have not been accounted for and cannot be seen in the Sentaurus Structure Editor simulation. Other than this, the simulations look remarkably similar. The colour of figure 3.11b represents doping concentration, and the scale is the same as that in 3.11a. Another remarkable aspect of this simulation is the amount of time needed to create the structure. The times can be seen in table 3.2.

	time [h]
Sentaurus Process	59 : 48 : 12
Sentaurus Structure Editor	00 : 00 : 29

Table 3.2: Times taken for simulations in figures 3.11a and 3.11b to run.

It should be mentioned that the time taken to simulate one implant in Sentaurus Structure Editor (shown in table 3.1) is higher than the time taken to simulate a whole pixel in Sentaurus Structure Editor. This is due to the very high number of mesh nodes used in the simulation to characterise the single implant. Again, the time shown in table 3.2 does not include the time taken to simulate individual wells in Sentaurus Process and extract and fit vertical and lateral doping profiles, but this does demonstrate that by using this method, any other structure could be created in a very short time and then simulated with Sentaurus Device. This could be highly desirable when experimenting with different design choices before fabrication. This method will be used in chapter 4 and in chapter 5.

3.2.2 Study of example reverse breakdown methods

In order to demonstrate that the faster approach to creating a device (in Sentaurus Structure Editor) is an effective substitute to the lengthy but theoretically more accurate Sentaurus Process approach, both models were imported into Sentaurus Device simulations and the results were compared. As a common measurement used to characterise HV-CMOS detectors are reverse I - V characteristics, the reverse bias characteristics were investigated using simulations. With their Sentaurus TCAD software package, Synopsys provide a number of example simulations, including one specifically designed for breakdown simulations. Within this example, there are six methods for calculating breakdown voltage, that include tracing the reverse characteristic curve of a simple MOSFET.

According to the Sentaurus Device training material provided with the software, breakdown simulations are difficult to perform as breakdown phenomena are divided into two distinct regions, prebreakdown and postbreakdown. In the prebreakdown region, the current is low and almost constant (reverse saturation) so a voltage-controlled sweep works best. In the postbreakdown region, even a small change in the voltage results in a very large increase in current and a current-controlled sweep works best. How to switch between voltage-controlled and current-controlled sweeps at or before the point of reverse breakdown is how the methods differ.

By default, these example simulations were designed for simulating the current that flows between the source and the drain of a MOSFET. In this work they were therefore modified to be used on the simulated RD50-MPW2 pixel cross-section

generated with Sentaurus Structure Editor shown in the last section (figure 3.11b). The same simulation was also performed on the pixel cross-section generated with Sentaurus Process (figure 3.11a) and compared to test the validity of the Sentaurus Structure Editor simulation, and will be reviewed in this section. While only one of these simulations methods was used in the remainder of this work, evaluating them all demonstrates that the results of breakdown simulations are largely independent of the method used and depend mostly on the models of physical phenomena selected. Describing them provides a good opportunity to discuss how breakdown simulations and Sentaurus Device in general works, and provides a good introduction to the models and the technique used for the remainder of this work.

Approximate Breakdown Analysis

The first method in the example simulations provided by Synopsys is known as the Approximate Breakdown Analysis (ABA). This method is incredibly fast as it only computes electrostatic potential from the Poisson equation (equation 3.3) and does not compute the quasi-Fermi potentials of mobile charges i.e. it does not solve the carrier transport equations for the electron and hole current densities. Instead, the quasi-Fermi potentials are considered constant. This method can therefore only be used in situations where a device is in equilibrium (all contacts are biased to the same voltage), which is not the case here and will not give accurate results. The method is nonetheless highlighted for the sake of introducing the reader to Sentaurus Device.

The electrostatic potential ϕ is computed from the Poisson equation [8]

$$\nabla \cdot (\varepsilon \nabla \phi - \vec{P}) = -q(p - n + N_D - N_A) - \rho_{\text{trap}} \quad (3.3)$$

where ε is the electrical permittivity, $\vec{P}$ is the ferroelectric polarisation, q is the elementary charge, N_D and N_A are the ionized donor and acceptor concentrations respectively, and ρ_{trap} is the charge density contributed by traps and fixed charges (this is seen later). As p and n are described by fixed quasi-Fermi potentials (see next section), the electron and hole densities n and p are computed from the electron and hole quasi-Fermi potentials (in this case, assuming Fermi statistics) [8]

$$\begin{aligned} n &= N_C F_{1/2} \left(\frac{E_{F,n} - E_C}{kT} \right) \\ p &= N_V F_{1/2} \left(\frac{E_V - E_{F,p}}{kT} \right) \end{aligned} \quad (3.4)$$

where $F_{1/2}$ is the Fermi integral of order 1/2, N_C and N_V are the effective density-of-states, E_C and E_V are the conduction and valence band edges,

$$\begin{aligned} E_{F,n} &= -q\Phi_n \\ E_{F,p} &= -q\Phi_p \end{aligned} \tag{3.5}$$

are the quasi-Fermi energies for electrons and holes, and Φ_n and Φ_p are the quasi-Fermi potentials for electrons and holes. In the case of this method as mentioned before, Φ_n and Φ_p are assumed to be constant. In this method, breakdown due to avalanche generation is simulated when one of the ionisation integrals (I_n or I_p) equals one

$$I_n = \int_0^W \alpha_n(x) \exp \left(- \int_x^W (\alpha_n(x') - \alpha_p(x')) dx' \right) dx \tag{3.6}$$

$$I_p = \int_0^W \alpha_p(x) \exp \left(- \int_0^x (\alpha_p(x') - \alpha_n(x')) dx' \right) dx \tag{3.7}$$

where α_n and α_p are the ionisation coefficients for electrons and holes, and W is the width of the depletion region [11].

The results of the simulation on the pixel simulated with Sentaurus Process are displayed in figure 3.12a and the pixel simulated with Sentaurus Structure Editor in figure 3.12b. The reverse breakdown voltage is computed when one of the ionisation integrals equals one (solid green line in the figures) and is shown as a dashed green line. The breakdown voltage of the pixel simulated with Sentaurus Process $V_{BD,p} = -19.69$ V and for the pixel simulated with Sentaurus Structure Editor $V_{BD,s} = -20.73$ V. The simulations provide very similar results which is a good indication that the pixel simulated with Sentaurus Structure Editor is a suitable replacement for the lengthy Sentaurus Process simulation.

It should be noted however that both calculated breakdown voltages are lower than the expected value of the breakdown voltage $V_{BD} = -60$ V provided by the foundry. This is the value specifically for this pixel geometry i.e., when the spacing between the pixel electrodes is $3 \mu\text{m}$. The fact that the simulated value here is lower is expected as this method is likely to underestimate breakdown as it assumes constant quasi-Fermi potentials and does not include models for other physical phenomena which make simulations more accurate.

Ionisation Integrals With Carriers Analysis

The second method is known as the Ionisation Integrals with Carriers (IIC) analysis. The method is very similar to the previous method since the ionisation integrals are calculated while ramping up the bias voltage, except in this case the full carrier transport equations, known as the continuity equations, are solved and the quasi-Fermi potentials are no longer considered constant. The continuity equations take

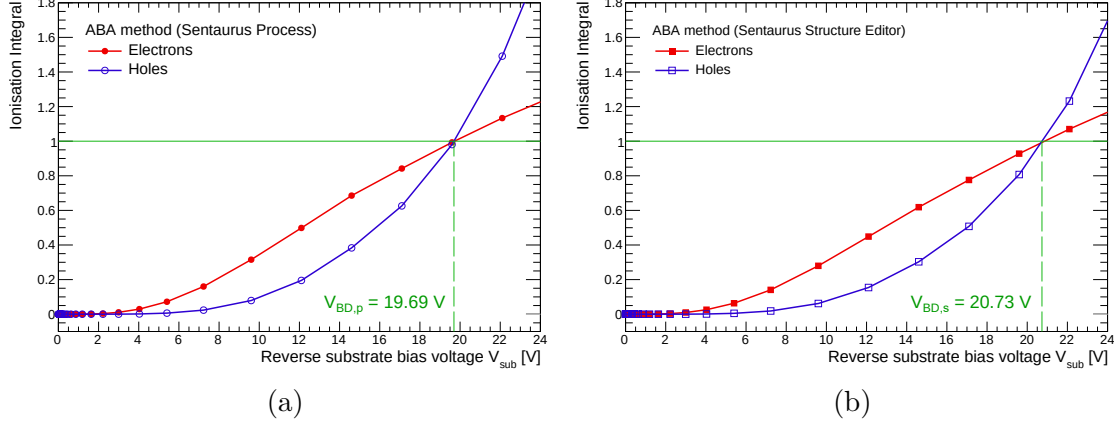


Figure 3.12: (a) Simulated electron and hole ionisation integrals (equations 3.6 and 3.7) for the structure simulated with Ssentaurus Process (shown in figure 3.11a). (b) Same plot for the structure simulated with Ssentaurus Structure Editor (shown in figure 3.11b). The extracted breakdown voltages are shown with dashed lines.

the form [8]

$$\begin{aligned} \nabla \cdot \vec{J}_n &= q(R_{\text{net},n} - G_{\text{net},n}) + q \frac{\partial n}{\partial t} \\ -\nabla \cdot \vec{J}_p &= q(R_{\text{net},p} - G_{\text{net},p}) + q \frac{\partial p}{\partial t} \end{aligned} \quad (3.8)$$

where $\vec{J}_n$ and $\vec{J}_p$ are the electron and hole current densities and can be computed by Ssentaurus Device using a range of transport models. $R_{\text{net},n}$ and $R_{\text{net},p}$ are the electron and hole net recombination rates, $G_{\text{net},n}$ and $G_{\text{net},p}$ are the electron and hole net generation rates. The drift-diffusion model is the default carrier transport model in Ssentaurus Device and is the model used in these simulations. According to the user guide, by default Ssentaurus Device assumes Einstein-diffusivity, which means the diffusivities D_n and D_p are given by the electron and hole mobilities μ_n and μ_p by the Einstein relation:

$$\begin{aligned} D_n &= kT\mu_n \\ D_p &= kT\mu_p \end{aligned} \quad (3.9)$$

The drift component of the drift-diffusion model is then given by:

$$\vec{J}_n = -nq\mu_n \nabla \Phi_n \quad (3.10)$$

$$\vec{J}_p = -pq\mu_p \nabla \Phi_p \quad (3.11)$$

In addition to solving the continuity equations, this method also includes more physical models than the last method. In Ssentaurus Device, a number of physical models can be switched on to make simulations more accurate, such as carrier

mobility degradation, carrier generation and recombination processes, and semiconductor bandgap descriptions, among others. Those mentioned are switched on for all subsequent methods and will be discussed below.

In the last method since no mobility models were specified, Sentaurus Device assumed a constant mobility which is only dependent on the temperature. This is inaccurate and should only be used for undoped materials. In doped devices like this one, carriers scatter off the impurities introduced by doping, therefore, a model to describe this effect is switched on. To further increase the accuracy, more mobility models are activated including, doping-dependent degradation μ_{doping} , degradation due to the silicon-silicon dioxide interfaces $\mu_{\text{interfaces}}$, and velocity saturation in high electric fields $\mu_{\text{saturation}}$. These are then combined by Sentaurus Device using Matthiessen's rule

$$\frac{1}{\mu} = \frac{1}{\mu_{\text{doping}}} + \frac{1}{\mu_{\text{interfaces}}} + \frac{1}{\mu_{\text{saturation}}} \quad (3.12)$$

Sentaurus Device includes a number of options for μ_{doping} but this simulation uses the default Masetti model [12], since the material is silicon. $\mu_{\text{interfaces}}$ becomes important in simulations of MOSFETs since carriers interact with the gate oxide-body interface when moving through the channel. While the structure used in this simulation does not have MOSFET channels, it does include STI between the diode terminals, therefore this model could still be important. In breakdown simulations, high electric fields will inevitably play a role. This is important to consider since carrier drift velocity is not proportional to electric field and saturates. High-field saturation models consist of three submodels: the mobility model, the velocity saturation model and the driving force model for which Sentaurus Device provides many options that can also be combined in different ways. In this instance, the default Canali mobility model [13] is used. The Canali model is also used for the velocity saturation, and the gradient of quasi-Fermi potential is used as the driving force.

Another important model to consider is the band structure. In Sentaurus Device, the band structure is described by the band gap, electron affinity and the band edge density-of-states and there are different models to describe these. The main difference between models is how they handle bandgap narrowing, which is active by default and is therefore accounted for. If no bandgap model is selected (as in the ABA method), by default, Sentaurus device uses the Bennett-Wilson model [14]. In these following simulations, the Slotboom bandgap model [15–18] is used.

Carrier generation and recombination processes are also very important as they describe how carriers travel between the valence and conduction bands. The models specified in this example method are the doping dependent Shockley-Read-Hall (SRH) recombination, the nonlocal path band-to-band tunnelling model, and of

course, avalanche generation. In the previous method the only physical model that is specified is the avalanche generation model, which was used to approximate the breakdown using ionisation integrals. In this method, the ionisation integrals are computed, and can be used for analysis, but the breakdown is estimated in a different way. The avalanche driving force F_{ava} that is specified is the gradient of the quasi-Fermi level

$$F_{\text{ava}} = |\nabla \Phi_{n,p}| \quad (3.13)$$

however, in this particular breakdown method, the script instructs Sentaurus Device to exclude the avalanche generation term from G_{net} in the continuity equations (equation 3.8). This is because, by calculating the continuity equations including carriers generated by avalanche multiplication, one loses the benefit of faster simulation time of ABA. The carrier generation due to avalanche multiplication is then calculated in a postprocessing step. This avalanche current is the portion of the current due to avalanche generation only, and is computed by integrating the avalanche generation rate over all semiconductor regions of the device for each step in the bias ramp. The avalanche current is then compared with the pixel diode leakage current and the point where the avalanche current exceeds the leakage current is the breakdown point.

The results of the simulation on both the Sentaurus Process pixel and the Sentaurus Structure Editor pixel can be seen in figures 3.13a and 3.13b respectively. The extracted breakdown voltages $V_{\text{BD},p} = -36.07 \text{ V}$ and $V_{\text{BD},s} = -37.56 \text{ V}$ are shown with dashed green lines. These again differ from $V_{\text{BD}} = -60 \text{ V}$ given by the foundry which is expected, as avalanche generation is excluded from the continuity equations. Nonetheless, the extracted breakdown voltages for both pixels are similar further supporting the idea that the Sentaurus Structure Editor pixel is a good model of the Sentaurus Process pixel.

However, the values of the breakdown voltages extracted from avalanche currents are puzzling, as physical models have been included in this method and the value should therefore be closer to the expected value. It is suspected that the computation of the avalanche current calculated in the postprocessing step is not valid for structures other than MOSFETs in its current state. Therefore out of curiosity, the ionisation integrals for both simulated pixels were also plotted, just like the previous method (ABA) and are shown in figures 3.13c and 3.13d, respectively. The breakdown voltages $V_{\text{BD},p} = -72.66 \text{ V}$ and $V_{\text{BD},s} = -74.97 \text{ V}$ are shown with the green dashed line and are obtained when one of the ionisation integrals equals one (shown with the solid green line). It should be noted again that by comparing $V_{\text{BD},p}$ and $V_{\text{BD},s}$, one can see they are very similar, further suggesting the Sentaurus

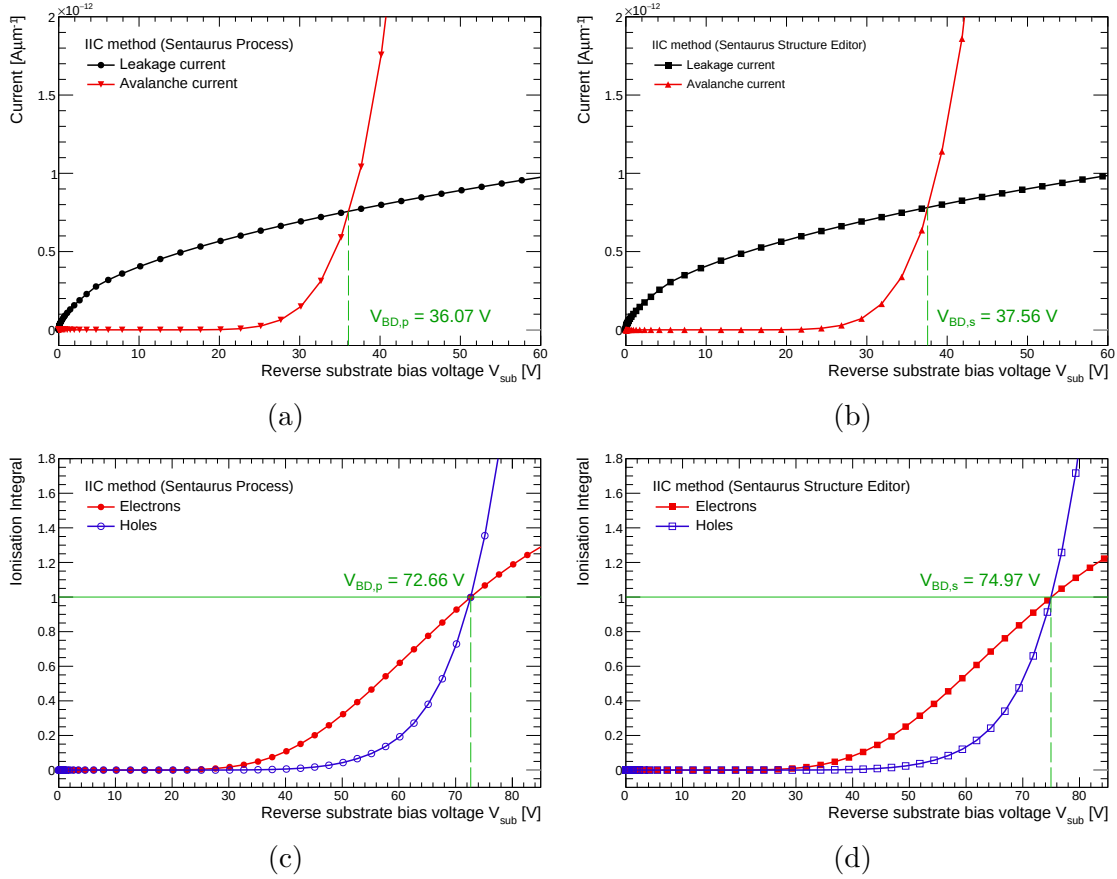


Figure 3.13: (a) Reverse leakage current and current due to avalanche generation only of the pixel simulated with Sentaurus Process. Reverse breakdown is shown with the green dashed line. (b) Same plot for the pixel simulated with Sentaurus Structure Editor. (c) Electron and hole ionisation integrals (equations 3.6 and 3.7) as a function of the substrate bias voltage for the pixel simulated with Sentaurus Process. The breakdown voltage is shown with the green dashed line. (d) The same plot for the pixel simulated with Sentaurus Structure Editor.

Structure Editor pixel is a sufficient model. In this method the results are more accurate than those obtained with the ABA method which becomes apparent when the results are compared to the value $V_{BD} = -60$ V given by the foundry. This is because the continuity equations are solved and more physical phenomena are modelled. However, they are higher than the breakdown given by the foundry but are given particular attention here as they are consistent with the results of the other simulation methods shown in the next sections.

External resistor method

The next method is known as the external resistor method which works by attaching a resistor to one of the electrodes. As mentioned before, this switches the simulation from a voltage-controlled sweep prebreakdown, to current-controlled sweep postbreakdown when the current increases and most of the voltage drops across the

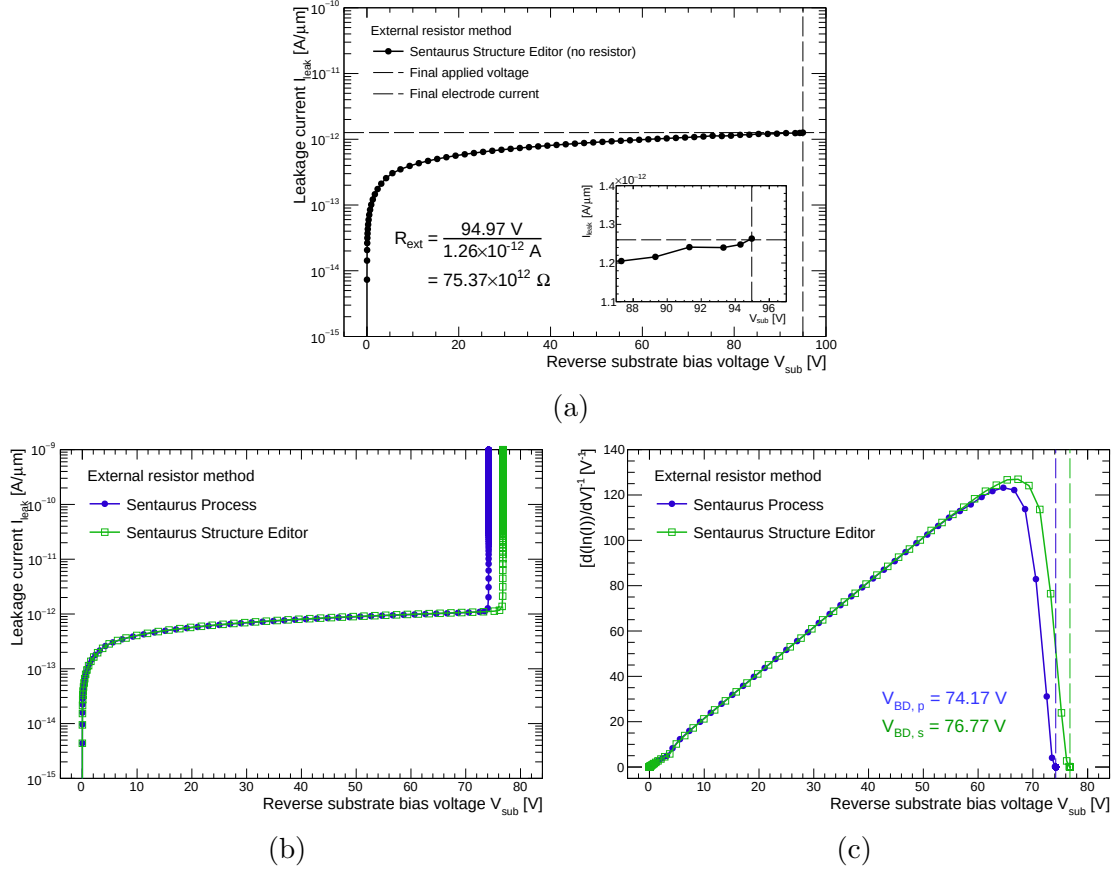


Figure 3.14: (a) External resistor method simulation with no resistor attached demonstrating failure to converge and resistor size calculation. Voltage and current at which the simulation fails to converge is shown with dashed lines. (b) Simulated reverse I – V characteristic curves of both the Sentaurus Process (solid blue circles) and Sentaurus Structure Editor (hollow green squares) pixels using the external resistor method. (c) Inverse logarithmic derivative curves of the reverse I – V simulations.

resistor. The size of the resistor is important and is determined by running the simulation once with no resistor attached. This is shown in figure 3.14a. According to the training material, the simulation will fail to converge near or shortly after breakdown, and the size of the resistor is then obtained by dividing the applied voltage by the current at the electrode. In this case, the voltage was 94.97 V and the current was 1.26 pA, which gives a resistance of 75.37 T Ω . Therefore almost a 100 T Ω would be required which is very large so a 1 T Ω resistor was deemed to be sufficient and used in subsequent simulations.

The active physical models are the same as in the last method, except that the avalanche generation rate is not excluded from the continuity equations. The generation rate due to avalanche multiplication (i.e., impact ionisation) G_{ii} is expressed as

$$G_{ii} = \frac{1}{q}(\alpha_n |\vec{J}_n| + \alpha_p |\vec{J}_p|) \quad (3.14)$$

and the ionisation coefficients can be calculated using a range of models. In this case the van Overstraeten-de Man model [19] is used, which is the default. In addition, the simulation is instructed to stop when the so-called *break criterion* is met i.e., when the current at the V_{HV} contact $I_{HV} = 1 \text{ nA} \cdot \mu\text{m}^{-1}$. This is analogous to compliance current in laboratory measurements.

The simulation was run again with a $1 \text{ T}\Omega$ resistor attached for both the pixel simulated with Sentaurus Process and Sentaurus Structure Editor and the results can be seen in figure 3.14b. In order to obtain the I - V curves, the `InnerVoltage` variables must be plotted against `TotalCurrent`. Since there was an external resistor defined, there is a difference between `InnerVoltage` and `OuterVoltage` and `InnerVoltage` must be used to obtain the voltage drop across the simulated pixel. In the original example simulation, the breakdown voltage of the MOSFET would have been estimated from the curve by simply extracting the voltage at which the current reaches a certain value ($0.1 \text{ mA} \cdot \mu\text{m}^{-1}$). This technique was modified for estimating the reverse breakdown voltage of this pixel using the method proposed in [20]. The Inverse Logarithmic Derivative (ILD) was calculated using the equivalence from [21]

$$\text{ILD} = \left(\frac{d \ln(I(V))}{dV} \right)^{-1} \equiv \left(\frac{1}{I} \cdot \frac{dI(V)}{dV} \right)^{-1} \quad (3.15)$$

and plotted as a function of substrate bias voltage, which can be seen in figure 3.14c. The minimum was used to estimate reverse breakdown for both the Sentaurus Process pixel, $V_{\text{BD},p} = -74.17 \text{ V}$ and the Sentaurus Structure Editor pixel, $V_{\text{BD},s} = -76.77 \text{ V}$. Like the two previous methods, comparing the Sentaurus Process and Sentaurus Structure Editor simulations, we can see again that the results are similar, but note that $V_{\text{BD},s}$ is very slightly higher than $V_{\text{BD},p}$, which is consistent with all methods shown so far.

Voltage-to-current boundary condition switching method

Another way to switch between a voltage-controlled ramp and a current-controlled ramp is to manually specify a switching point. In Sentaurus Device, there are a number of ways to simulate ramps, and all methods described so far have used a `Quasistationary` ramp.

Somewhat simplified, in a `Quasistationary` ramp, a `Goal` must be provided, such as a voltage, for the ramp to reach. If a voltage is provided, it is called the final voltage V_f . For the MOSFET, $V_f = 6 \text{ V}$ but this was changed to $V_f = 60 \text{ V}$ for

the case of the pixel. Sentaurus Device attempts to ramp up the voltage of the pixel step by step, solving for physical quantities (such as current density and electric field) at each mesh node as it goes. Some variables can be specified to calculate the step size at each step n : the initial step size, which is the first step size used; the minimum and maximum step size, which limit the step size; and the increment and decrement, factors which control how much to increase or decrease the step size by after solutions converge or diverge, respectively.

An initial voltage V_i must also be specified, which in this case is 0 V. Sentaurus Device begins by solving the device under these initial conditions. Then, Sentaurus Device attempts to ramp up the device according to the step size information provided. In this case, the initial step size is $2 \cdot 10^{-3}$. The first voltage step is calculated using the formula

$$V = V_i + n(V_f - V_i) \quad (3.16)$$

which would be $V = 0.12$ V. If the solution converges, the step size is increased by the increment factor, which in this case is 1.41. Therefore the new step size is $2.82 \cdot 10^{-3}$,¹ which makes the next step $n = 4.82 \cdot 10^{-3}$. Thus, the next voltage to solve would be calculated again using equation 3.16 and $V = 0.2892$ V. If the solutions continue to converge, the step size continues to increase until it reaches the maximum step size. If however, the solver fails to converge on a solution (diverges), the step size is decreased by the decrement factor and Sentaurus Device attempts to re-solve.

In this example method, in order to switch between a voltage-controlled ramp and a current-controlled ramp, two **Quasistationary** ramps are used. In the first, a voltage **Goal** is specified. As mentioned before, this was set to -60 V. In the second, a current **Goal** is specified, which was set to 1 nA. When the device successfully reaches 60 V, the current-ramp initiates and the current is ramped using an analogous formula to 3.16, until the current at the specified electrode reaches 1 nA. This switching point can be seen in figure 3.15a with the dashed line. Before this point, for both the Sentaurus Process and the Sentaurus Structure Editor pixels, the voltage can be seen to increase in steps of 1.5 V, since the specified maximum step size is 0.025. Then the step size changes depending on the initial step size of the new **Quasistationary** command, and whether solutions converge or diverge. No external resistor is necessary and is therefore not used in this method. The breakdown voltages are extracted using the same technique as the previous method (equation 3.15). Figure 3.15b shows that this simulation method produces very similar results to the external resistor method.

¹In reality this second step size is also affected by the number of iterations in the previous solve, but a description of this goes beyond the scope of this thesis.

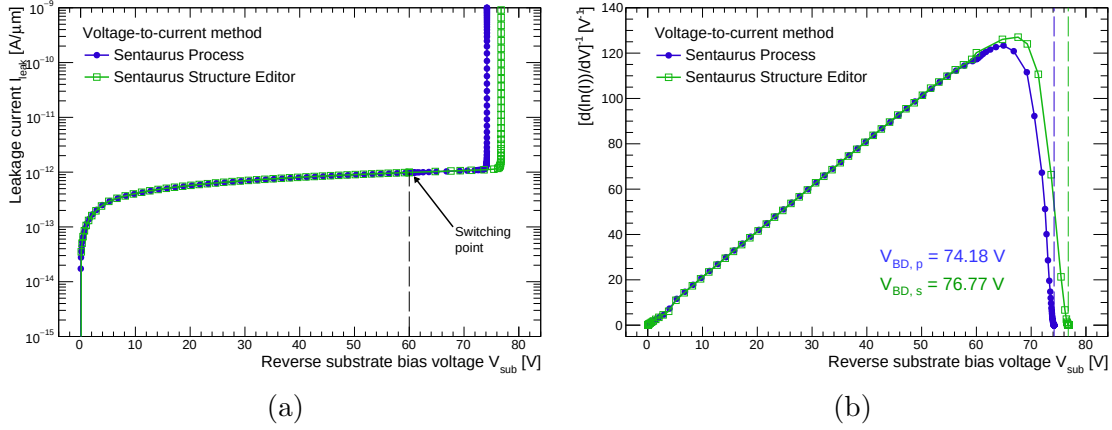


Figure 3.15: (a) Simulated reverse I - V characteristic curve using the voltage-to-current method. (b) Inverse logarithmic derivative curve of the reverse I - V simulation.

Continuation method

As mentioned before, all previous methods have used **Quasistationary** ramps. This method uses a different command known as **Continuation** which ramps the device based on a dynamic load-line technique [22]. It is similar to the external resistor method, except that instead of manually applying a resistor to one of the electrodes, the **Continuation** command automatically calculates the value of the resistor based on the slope of the I - V curve, which should require almost no user-intervention. However, the example simulation uses a special case of the **Continuation** command, where the adaptive algorithm is not switched on until the current and voltage reach certain limits, **Iadapt** and **Vadapt** respectively which if used, must be specified. The example simulation does this because at low bias voltages, currents can be noisy which can cause the slope to be calculated incorrectly. Before this point, a **Quasistationary** ramp is used.

In addition, a window for the **Continuation** command must be defined, in order to stop the simulation if the current or voltage increases to a value outside this window. This is similar to the break criterion of the previous methods, therefore the maximum voltage must be set to a value higher than the breakdown voltage to avoid stopping the simulation early. The window was defined in this case by setting **MinVoltage** = 0 V, **MinCurrent** = 0 A, **MaxVoltage** = 100 V, and **MaxCurrent** = $1 \text{ nA} \cdot \text{cm}^{-1}$. The original simulation was modified further by switching off the parameter **NewArc** as this caused the simulation not to converge. Among other changes, **NewArc** limits the maximum value of the resistor to 100 M Ω which was much lower than the needed resistance calculated in the external resistor method. Switching off **NewArc** instead limits the maximum value of the resistor to 100 T Ω .

The results of the simulations on both pixel types can be seen in figure 3.16a.

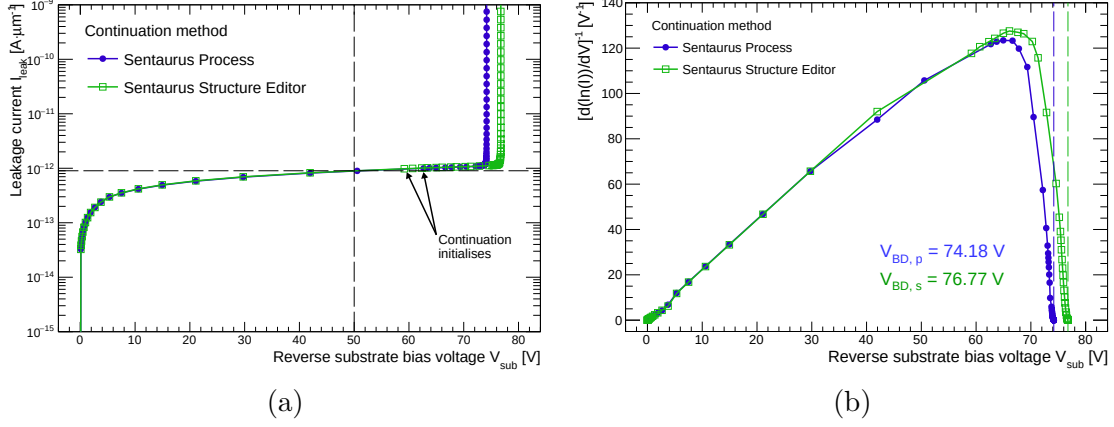


Figure 3.16: (a) Simulated reverse I - V characteristic curve using the continuation method. Dashed lines show limits of adaptive algorithm initialisation (b) Inverse logarithmic derivative curve of the reverse I - V simulation.

The vertical and horizontal black dashed lines represent the limits that the voltage and current of the device must reach in order for the **Continuation** algorithm to switch on. These are $V_{\text{adapt}} = 50 \text{ V}$ and $I_{\text{adapt}} = 9 \cdot 10^{-13} \text{ A} \cdot \text{cm}^{-1}$ respectively. When both the voltage and current of the device increase above these values, the adaptive algorithm initialises (shown with the arrows). The breakdown voltages were again calculated using the ILD seen in figure 3.16b. The results are exactly the same as the voltage-to-current method.

Transient method

The final method works in a very similar way to the external resistor method (including connecting a large resistor to one of the electrodes) but instead of using a **Quasistationary** command to ramp the device, it uses a **Transient** command. These two work in much the same way, except that the **Transient** command solves the device as a function of time t instead of the arbitrary step n where the ramp speed is in $\text{V} \cdot \text{s}^{-1}$. The device is solved step by step from an **InitialTime** to a **FinalTime**, which must both be specified. Like the **Quasistationary** command, the time step increases first by the initial step size (**InitialStep**, in seconds) and, if successful, continues to increase by the **Increment** factor until it reaches the maximum step size (**MaxStep**). If at any point, the simulation fails to converge, the time step is reduced by the **Decrement** factor and Sentaurus Device attempts to re-solve. Once the simulation reaches the **FinalTime** (or the break criterion, or the step size decreases below the minimum step size (**MinStep**)), it stops.

Results in **Transient** simulations can be sensitive to ramp times. In the original simulation of the MOSFET, Sentaurus Device is instructed to ramp the drain contact to 100,000 V in 1 s where the simulation will stop if the drain current reaches

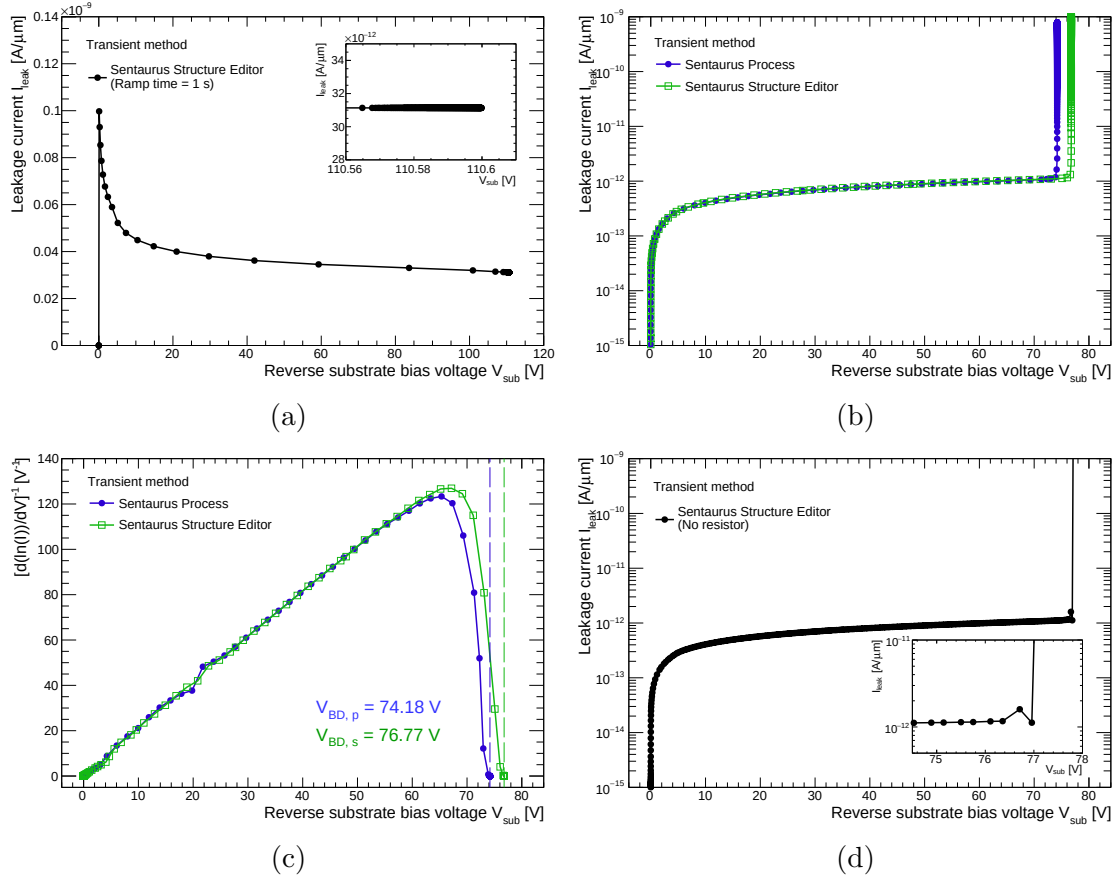


Figure 3.17: (a) Simulated reverse I - V characteristic curve of the structure simulated with Sentaurus Structure Editor using the transient method with fast ramp rate. (b) Same as (a) with modified slower ramp rate for both simulated pixels. (c) Inverse logarithmic derivative curve of the reverse I - V simulation. (d) Same as (a) with modified ramp rate and no external resistor attached.

1.443 mA (break criterion)². Figure 3.17a is the result if these settings are used on the pixel. Therefore, this particular method was modified by adjusting the voltage ramp rate to $1 \text{ V} \cdot \text{s}^{-1}$, as these were similar to the conditions used in the laboratory measurements. **MaxStep** was also increased from 0.01 s to 2 s to decrease simulation time. The results from both the Sentaurus Process and Sentaurus Structure Editor pixels can be seen in figure 3.17b. The breakdown voltages were extracted by calculating the ILD just like the previous methods, shown in figure 3.17c. The results of all methods are summarised in table 3.3.

Summary and conclusions

From the results in table 3.3, comparing $V_{\text{BD},p}$ to $V_{\text{BD},s}$, we can see that there is approximately only a 1 V or 2 V difference in the computed breakdown voltage between the pixel simulated in Sentaurus Process and the pixel simulated in Sentaurus

²Since the drain contact is biased through a large resistor, as the drain current increases, most of the voltage will drop across the resistor.

Structure Editor. This is no more than is seen in sample-to-sample variation in fabricated devices (see tables 4.1, 4.2, and 4.3 in the next chapter), suggesting that the Sentaurus Structure Editor simulation is a very good replacement for the Sentaurus Process simulation. The doping profiles extracted one by one from the small Sentaurus Process simulations could be used to construct other pixel geometries or possibly other devices, and provide accurate results without relying on a lengthy Sentaurus Process simulation. However, it should be noted that the computed breakdown is always lower for the Sentaurus Process simulation. This could suggest some accuracy is lost in the final reconstructed 2D doping profile in Sentaurus Structure Editor, or it has been changed in some other way. This could be tested by performing more MC Sentaurus Process simulations of the same cross-section with different initial MC seed values and comparing.

Method	$V_{BD, p}[\text{V}]$	$V_{BD, s}[\text{V}]$
ABA	-19.69	-20.73
IIC	-72.66(-36.07)	-74.97(-37.56)
Resistor	-74.17	-76.77
Voltage-to-current	-74.18	-76.77
Continuation	-74.18	-76.77
Transient	-74.18	-76.77

Table 3.3: Results from six different breakdown voltage simulation methods on two simulated structures. Values shown in brackets are determined using avalanche currents computed in a postprocessing step.

Comparing method to method, we can see that the ABA and IIC methods underestimate the breakdown voltage compared to the others. This is understandable as they are considered approximations. The ABA method does not take into account the carrier continuity equations and only computes the electrostatic potential from the Poisson equation. In reality, carriers affect the electrostatic potential and are in turn affected by the electrostatic potential. In addition, in this particular case the model used for avalanche generation is “less physical” [8] than the other models available in Sentaurus Device for calculating avalanche generation, and other physical phenomena are not taken into account (such as carrier recombination). In contrast, the IIC method takes into account the same physical phenomena as the other methods, and solves the carrier continuity equations. The only difference between IIC and the remaining methods is that it does not include the avalanche generation term i.e. avalanche generated carriers in the continuity equations. This keeps simulation time to a minimum, but sacrifices accuracy.

The fact that all subsequent simulation methods are almost exactly the same to two decimal places strongly suggests that the simulated breakdown voltage is independent of the simulation method used. Therefore any of these methods (external

resistor, voltage-to-current, continuation, or transient) could be used for reverse I - V characteristic simulations and the choice would be left to user preference. In this work the external resistor method was excluded as a viable option for two reasons. The first is that the method requires the simulation to be run twice, once to determine the size of the load resistor and once to solve the characteristic curve. The second, is that the method also requires a very long time to converge. Sentaurus Device computes the voltage ‘outside’ the resistor in the variable `OuterVoltage`, requiring many iterations to reach the desired simulation break criterion: the current inside the simulated device. The voltage-to-current and continuation methods were also excluded, as they require some prior knowledge of the characteristic curve. The voltage-to-current method works best when the switching point is specified before the voltage boundary condition would no longer converge. This could be approximated in a similar fashion to above by defining the switching point some tens of volts before the known breakdown voltage, or the simulation could be run twice in a similar fashion to the resistor method to determine the point that the simulation diverges.

There is a similar problem with the continuation method as it is now. When the current is low (and potentially noisy) a `Quasistationary` ramp is used to avoid convergence issues. The `Continuation` command only initialises after the current limit (or voltage limit, or both) is reached, which must be specified. This is akin to the switching point of the voltage-to-current method and the user must have a good idea for the value of these limits beforehand. This works well in the case of attempting to reproduce the RD50-MPW2 reverse characteristic curves, because the breakdown voltage is known. If one wishes to use these simulations to make predictions about devices that have not yet been fabricated and measured, the simulations could still need to be run twice. The continuation method could be modified to use only the `Continuation` command (setting `Vadapt` and `Iadapt` to 0, the default) but this was not tested. In addition, since the derivative of the curve is calculated at every point, the `Continuation` can be more computationally expensive.

Therefore the only remaining method is the transient method. In the example simulations, the transient method is the only other method that makes use of the large external resistor connected in series to one of the terminals. The size of the resistor used was the same as that determined by the external resistor method, however the transient method therefore still required a total of two simulations to compute the breakdown voltage, which is not ideal. Out of curiosity, the simulation was run without the resistor attached to imitate what would happen in future simulations if the size of the resistor needed to be determined. The results can be seen in figure 3.17d. This second simulation gave similar results, which is useful as the method potentially requires less user-intervention at the beginning, but as it can

be seen from the number of points, the Sentaurus Device simulation was unable to converge on solutions with large step sizes. Therefore throughout this work, this method is used, but some modifications were made to help with convergence. These modifications will be described in the next section. In addition, the simulation is run once and if convergence problems are still encountered, the size of the resistor is calculated and connected to one of the terminals and the simulation is re-run. It should also be mentioned that these methods still overestimate V_{BD} with respect to the value expected by the manufacturer (≈ -60 V). This was found to be most likely due to the presence of positive charges in SiO_2 which were not accounted for in these example methods. Additionally, the physics models used were possibly more suited to simulate a transistor. Therefore, in the next section a study of the physics models provided by Synopsys in their Sentaurus package will be studied and adapted to a pixel, and fixed positive oxide charges will also be studied using simulations.

3.2.3 Customised reverse breakdown method

In this section, the physics models and `Transient` command parameters used in the example transient method simulation were taken into consideration and modified to better suit a pixel. It was assumed that the original simulation was designed (and physics models chosen) specifically with the simulated MOSFET in mind. Thus, some models are not valid for larger scale objects such as the pixels in HV-CMOS detectors, or for the doping concentrations present in these pixels. However, Sentaurus Device offers a large choice of models for different physical phenomena. Starting with avalanche generation as an example, there are six options to model the ionisation coefficients, and each model can use four different driving forces. In addition, there is an option to include a dependency on the bandgap in avalanche models. This gives a total of 48 simulations, if one wishes to test how all combinations compare to laboratory measurements.³ On top of this, there are six different bandgap models. Including all of these in investigations would lead to a total of 288 different combinations that could be performed. And this does not include the multitude of options available for phenomena such as carrier recombination and mobility degradation. Therefore, an extensive comparison such as this is not given here and default models are used in a lot of cases. However, in the following customised method alternative choices for some of the models were made.

³This does not take into account the fact that in Sentaurus Device, different avalanche models and avalanche driving forces can both be chosen for electrons and holes in the same simulation. This would increase the total number of possible combinations considerably.

Analysis of previous results

The transient simulation of the pixel simulated with Sentaurus Structure Editor was analysed at points before and after breakdown in order to understand the underlying mechanism. In addition to the modifications made to the example transient simulation described in the previous section, a `Plot` command was added to the `Transient` command to save a snapshot of the simulation just before breakdown. In this case when the ramp time = 70 s or in this case, when $V_{\text{sub}} \approx -70$ V. This value might differ when an external resistor is attached due to the voltage drop across it. Quantities that one wishes to view must be added to a `Plot` section (different from the `Plot` command) before the simulation is run. In the original example simulations, the doping concentrations (`Doping`), total current density (`TotalCurrentDensity`), and electric field (`ElectricField`) can be viewed, among others. Figure 3.18 shows the pixel cross-section, with the implant wells annotated. The colour of the plot represents total current density in $\text{A} \cdot \text{cm}^{-2}$ where blue is low and red is high. Figure 3.18a shows the total current density of the pixel in prebreakdown ($V_{\text{sub}} = -70$ V) and 3.18b shows postbreakdown ($V_{\text{sub}} = -76.77$ V).

The first thing to notice about figure 3.18a is that both the p-substrate and the n-type wells are depicted in yellow. This is because these are the pixel diode electrodes and therefore one component which should have the same current flowing through it. The green region at the top-centre of the image represents the total current density of the p-type wells that are isolated from the substrate by the n-type wells. The total current density here is lower than that of the pixel as it is decoupled by the natural p-n junction that is formed. At the very top of the image, the thin blue-green regions represent the total current density inside the STI, the outermost openings are the substrate contacts (the anode of the diode), and the innermost openings are the DNWELL contacts (the cathode). It can be seen on the right of 3.18b (postbreakdown) that there is a large current flowing directly between the contacts.

According to reference [23], of the three mechanisms responsible for breakdown (thermal instability, tunnelling, and avalanche multiplication), avalanche multiplication is the most important when considering reverse breakdown of a p-n junction. This can be visualised in Sentaurus TCAD by changing the field to impact ionisation (`ImpactIonization`, in number of carriers $\text{cm}^{-3}\text{s}^{-1}$). This can be seen in figures 3.18c (prebreakdown) and 3.18d (postbreakdown), where again, blue is low and red is high and the wells are annotated. During postbreakdown on the right-hand side, a region of high impact ionisation can be seen between the pixel electrode contacts. This is because impact ionisation requires a certain threshold electric field strength, something that can also be visualised in Sentaurus TCAD. This can be seen in

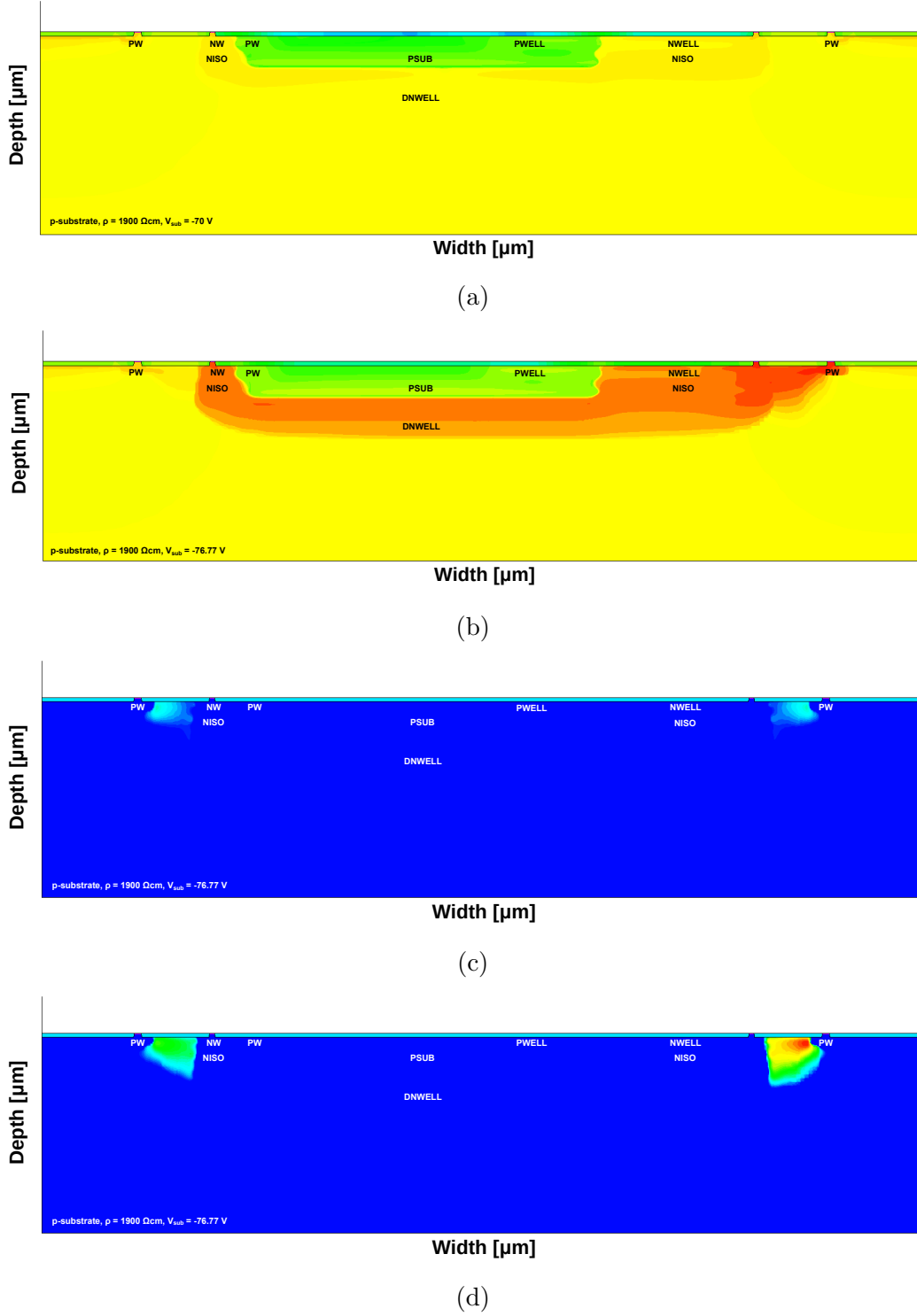


Figure 3.18: (a) Total current density of pixel simulated in Sentaurus Structure Editor prebreakdown ($V_{\text{sub}} = -70 \text{ V}$). (b) Total current density of the same pixel in (a) postbreakdown ($V_{\text{sub}} = -76.77 \text{ V}$). The scale is the same in (a) and (b). (c) Impact ionisation of pixel simulated in Sentaurus Structure Editor prebreakdown ($V_{\text{sub}} = -70 \text{ V}$). (d) Impact ionisation of the same pixel in (c) postbreakdown ($V_{\text{sub}} = -76.77 \text{ V}$). The scale is the same in (c) and (d).

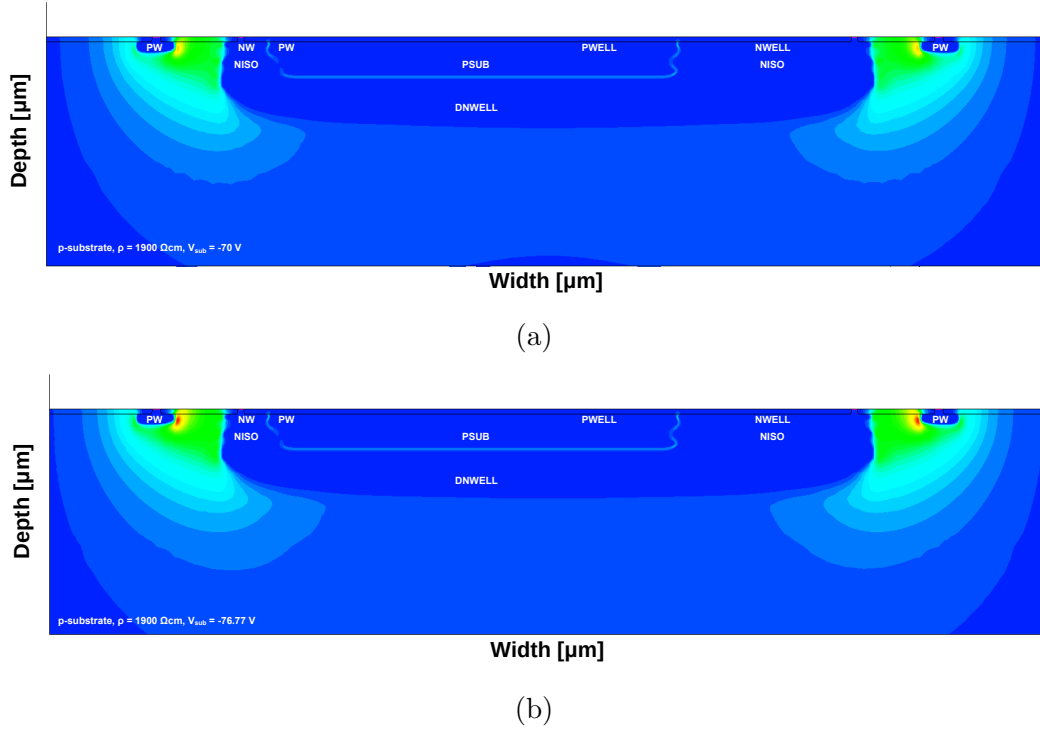


Figure 3.19: (a) Electric field of the pixel simulated in Sentaurus Structure Editor prebreakdown ($V_{\text{sub}} = -70 \text{ V}$). The positions of the wells used to construct the pixel are labelled. (b) Electric field of the same pixel in (a) postbreakdown ($V_{\text{sub}} = -76.77 \text{ V}$). The scale is the same in both images.

figures 3.19a (prebreakdown) and 3.19b (postbreakdown). The asymmetry is most likely due to the asymmetrical shape of the pixel.

Blue represents regions of low electric field strength and red regions of high electric field. In both images, it can be seen that the electric field is low where wells have been implanted, and higher in the p-substrate which corresponds to the depletion region. The maximum value of the electric field postbreakdown is around $4 \cdot 10^5 \text{ V} \cdot \text{cm}^{-1}$ suggesting this is the threshold field strength for impact ionisation. Zoomed in images of doping concentration, total current density, and electric field of the breakdown region can be seen in figure 3.20.

3.2.3.1 Study of avalanche models

The accuracy of available avalanche models in Sentaurus Device was investigated. So far, it has been shown that the simulated breakdown voltage was independent of the breakdown method used. Therefore, in TCAD simulations, it could be important to carefully consider the model used to describe avalanche generation to reproduce the breakdown seen in laboratory measurements. Sentaurus Device offers six alternative models to compute the ionisation coefficients in equation 3.14. According to the user guide, the Hatakeyama avalanche model [24] was developed for 4H-SiC devices and

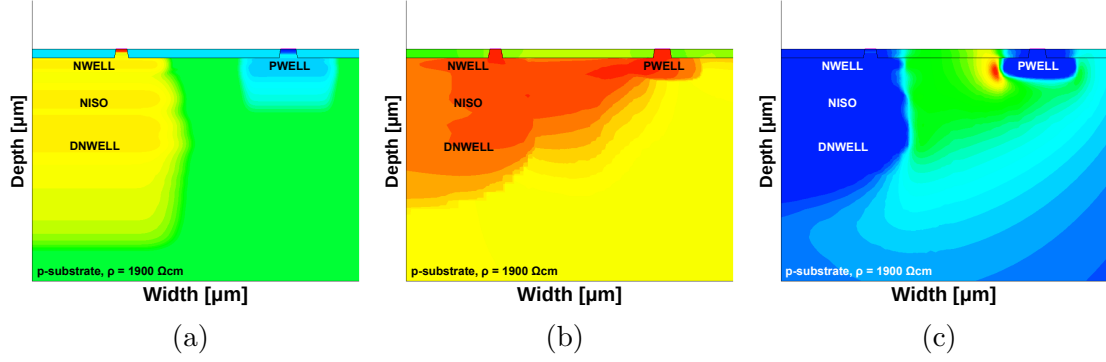


Figure 3.20: (a) Doping concentration of pixel (diode) simulated in Sentaurus Structure Editor, zoomed on region where breakdown happens. Wells have been labelled. (b) Total current density of same region of (a) postbreakdown ($V_{\text{sub}} = -76.77$ V). Current is flowing between the electrodes. (c) Same region as (a) and (b) showing region of high electric field.

will therefore not be used here, leaving just five models: the van Overstraeten-de Man model, the default, used in the previous section; the Okuto-Crowell model [25]; the Lackner model [26]; the University of Bologna model [27–29]; and the new University of Bologna model [30–32]. The main differences between the models are the temperature and electric field ranges they apply to. In this study temperature is always assumed to be 300 K so electric field is the main consideration. The ranges of electric fields can be seen in the table 3.4 below.

Model	$\vec{E}[\text{V} \cdot \text{cm}^{-1}]$
van Overstraeten-de Man	$1.75 \cdot 10^5 - 6.00 \cdot 10^5$
Okuto-Crowell	$1.00 \cdot 10^5 - 1.00 \cdot 10^6$
Lackner	$1.00 \cdot 10^5 - 1.00 \cdot 10^6$
Uni. of Bologna	$5.00 \cdot 10^4 - 6.00 \cdot 10^5$
New Uni. of Bologna	$5.00 \cdot 10^4 - 6.00 \cdot 10^5$

Table 3.4: Electric field ranges of avalanche generation models in Sentaurus Device. The maximum value of the electric field postbreakdown in figure 3.19 is around $4 \cdot 10^5 \text{ V} \cdot \text{cm}^{-1}$ which is in range of all models.

In addition to models for ionisation coefficients, Sentaurus Device offers multiple choices for the driving force for impact ionisation F_{ava} : **ElectricField**, used in the previous section to activate the ABA breakdown method; the gradient of the quasi-Fermi level, **GradQuasiFermi** (equation 3.13), the default used in the other methods in the previous section; the component of the electrostatic field in the direction of the current, **Eparallel**; and the carrier temperature, **CarrierTempDrive**. **CarrierTempDrive** can only be used when the hydrodynamic carrier transport model is used (instead of the drift-diffusion model, which is the case here) and therefore will not be studied here. This leaves just **GradQuasiFermi** and **Eparallel**.

As it was shown in the previous section that the pixel simulated with Sentaurus Structure Editor is a good model of the pixel simulated in Sentaurus Process, only the Sentaurus Structure Editor pixel will be used here to further reduce the number of variables. All other models and options were kept the same as those in the example transient method simulation. In addition, the option for bandgap-dependent avalanche generation was switched on only for the van Overstraeten-de Man ionisation coefficient model with the gradient of the quasi-Fermi level as the driving force.

The results of the simulations of all five avalanche models can be seen in figure 3.21. Figure 3.21a shows simulations using the `GradQuasiFermi` driving force and figure 3.21b shows the simulations using the `Eparallel` driving force. Figure 3.21c shows the additional simulation comparing bandgap-dependent and non-bandgap-dependent van Overstraeten-de Man ionisation coefficient models. It can be seen by comparing (a) to (b) that the driving force used makes little difference to the computed breakdown voltage. The computed breakdown voltage varies only slightly model to model, most likely due to the fact that the maximum electric field in the device lies within the applicable range of all models. The computed breakdown voltage is also still always higher than the laboratory measurements and the result predicted by the foundry (≈ -60 V). This can be improved slightly by switching on the option for bandgap dependence (figure 3.21c) where the computed breakdown voltage has decreased slightly, but only by about 1 V. This could suggest that either all models are not accurate, or that there is some other mechanism or phenomenon responsible for the breakdown in laboratory measurements. One important note is that in these simulations, the third dimension is not properly considered (see section simulations in the next chapter).

To summarise, for all simulations presented in this thesis, the default van Overstraeten-de Man was chosen, as the results showed that this model gives the closest value to the laboratory measurements. This is the same model that was used in the example methods (equation 3.14). Unlike the example methods, two changes have been made. First, despite giving similar results with respect to `GradQuasiFermi`, the electric field parallel to current (`Eparallel`) was chosen as the driving force as it is the physically correct driving force according to reference [8]. Second, bandgap dependence for avalanche generation was switched on as this was shown to slightly improve the simulation results with respect to the expected value of V_{BD} .

3.2.3.2 Study of models of other physical phenomena

This section is a brief study of the other types of physics models available in Sentaurus Device which will be used in the simulations in this thesis. To reiterate, there

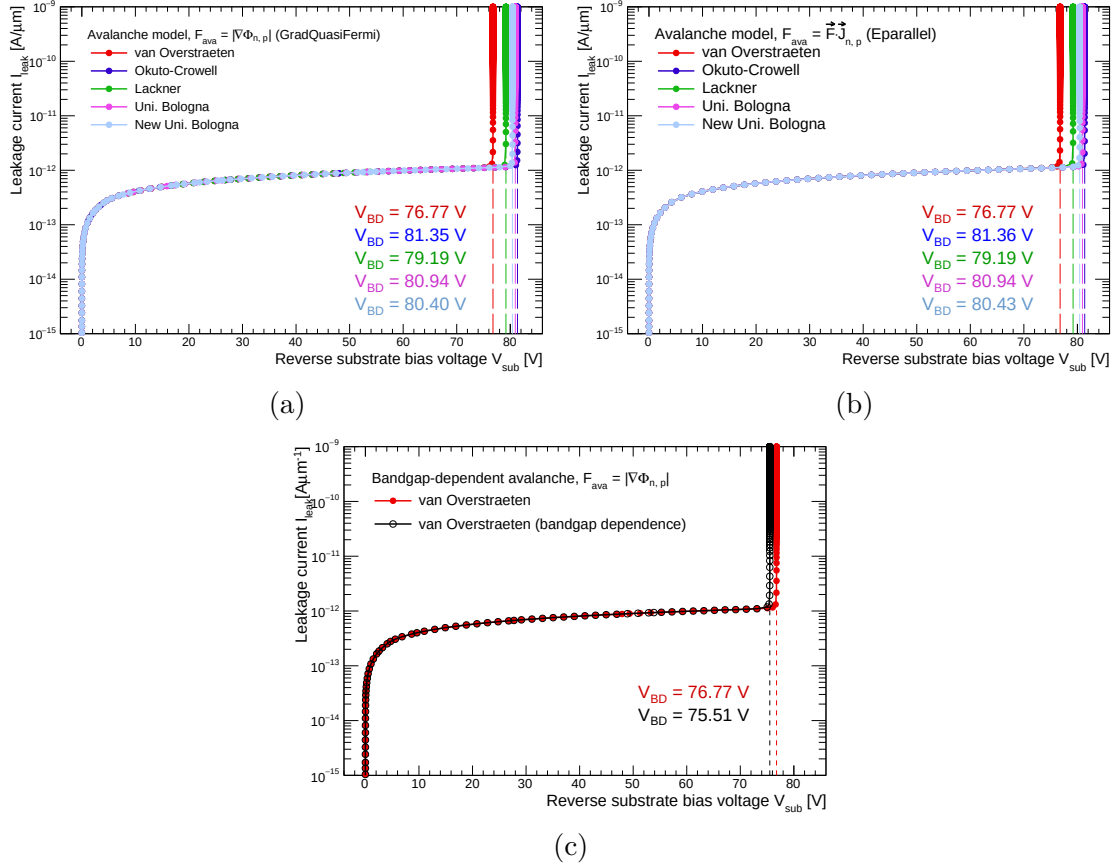


Figure 3.21: Simulated reverse I - V characteristic curves and computed breakdown voltages of the structure simulated using Sentaurus Structure Editor. All simulations were performed using the transient method, using different models for computation of ionisation integrals, with the avalanche driving force as (a) the gradient of the quasi-Fermi level and (b) the component of the electrostatic field in the direction of the current. (c) Curves comparing bandgap-dependent van Overstraeten-de Man ionisation coefficients model with gradient of the quasi-Fermi level driving force.

are many models available and to simulate all of them and all possible combinations would be very time-consuming. Therefore in most cases only a few models have been investigated. Models are separated into categories such as: generation and recombination processes, bandgap physics, and carrier transport, which will be discussed in this section one by one.

For generation and recombination processes, avalanche generation (discussed and summarised in the previous section) was of course, switched on. In the example methods studied, doping dependent SRH recombination was activated, However, band-to-band tunnelling was switched off as it can be neglected for a device with p-n junctions with doping concentrations of less than $1 \cdot 10^{19} \text{ cm}^{-3}$ on both sides, and where the electric field is less than $8 \cdot 10^5 \text{ V} \cdot \text{cm}^{-1}$ [8]. A simulation demonstrating this was performed and the results are shown in figure 3.22a. The computed breakdown voltage is unchanged.

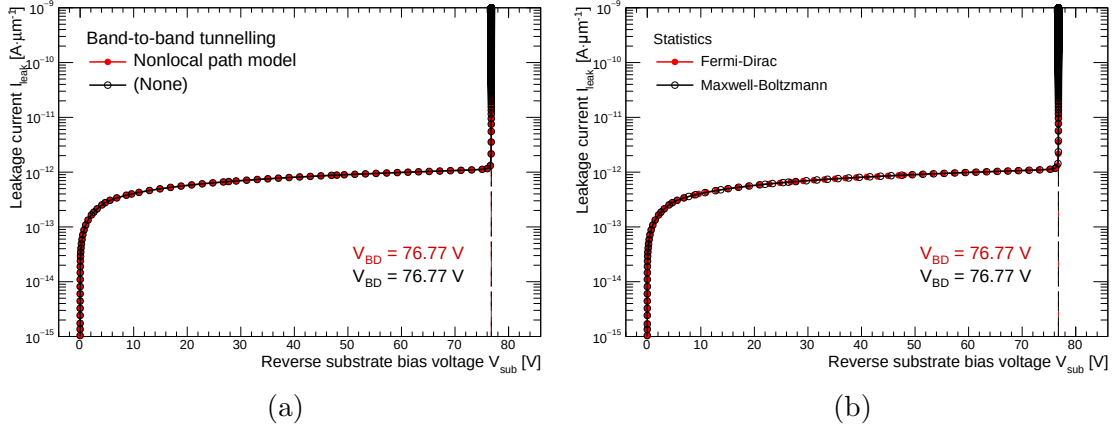


Figure 3.22: (a) Simulated reverse I - V characteristic curves of the structure simulated with Sentaurus Structure Editor using the transient method with band-to-band tunnelling model switched on and off. (b) Simulated reverse I - V characteristic curves of the structure simulated with Sentaurus Structure Editor using the transient method with both Maxwell-Boltzmann and Fermi-Dirac statistics.

There are a range of bandgap models available in Sentaurus Device which will not be examined in detail here. The main difference between bandgap models is how they handle doping dependent bandgap narrowing, which is only important in the high doping regime [8] so it is switched on, which is the default, but the same model used in the example methods is used here. A deep investigation into the different mobility models is also not investigated here, and therefore, the same mobility models will be used, except **Eparallel** is used for the high field saturation mobility model driving force as it is the physically correct model according to reference [8]. In particular, mobility degradation due to silicon-silicon dioxide interfaces $\mu_{\text{interfaces}}$ (**Enormal**) was most likely originally included in the example MOSFET simulation because the electric field induced by the gate voltage causes carriers to interact with the body-gate oxide interface. A similar structure is formed in the pixel seen in figure 3.20c. Carriers flow between the diode electrode contacts underneath the STI and could interact with the p-substrate-STI interface. This is expanded upon soon.

Just like the non-approximate methods, the full set of carrier transport equations are solved and the carriers generated by impact ionisation are included in the generation term G_{net} in the continuity equations (equations 3.8). Again, the drift-diffusion model is used as the carrier transport model, assuming Einstein-diffusivity. However, unlike the example methods, Maxwell-Boltzmann statistics were used in the method presented here instead of Fermi-Dirac statistics. Although Fermi statistics are physically more accurate, simulations are slower. In addition Fermi statistics only become important for carrier densities larger than $1 \cdot 10^{19} \text{ cm}^{-3}$ in the active regions of the device [8]. This could be the case when performing simulations of transistors (such as in the example methods) but the doping concentrations in the

active regions of the pixels in this study are much lower. This was tested by performing the same simulation as figure 3.17a on the Sentaurus Structure Editor structure with Fermi statistics switched off and the results are shown in figure 3.22b. It can be seen that the computed breakdown voltage is unaffected.

3.2.3.3 Si–SiO₂ interface traps

A possible mechanism for the difference in simulated and expected breakdown voltages is suggested and described in this section. The authors of reference [23] discuss how the silicon–silicon dioxide (Si–SiO₂) interface affects the performance of metal-oxide-silicon (MOS) capacitors. Fixed oxide charges Q_f and charge trapped at the interface Q_{it} arise as a consequence of the processes used to form SiO₂. A detailed description of the cause is provided in reference [33]. In summary, after silicon wafers are cut from the single-crystal ingot, or silicon is etched before STI formation for example, atoms at the surface no longer share all bonds with neighbours, leaving dangling bonds. The silicon surface is therefore chemically reactive and electrically conductive and is intentionally passivated by thermally grown SiO₂. However, there can still be a high concentration of defects at and close to the interface, introducing energy levels in the forbidden silicon bandgap giving rise to Q_{it} and Q_f . These are distinct from oxide trapped charges Q_{ot} , created by X-ray radiation, simulated in studies similar to this work [34, 35]. The author of reference [33] also notes that defect concentrations depend on the orientation of the silicon crystal, and can also differ depending on the cleaning and polishing processes used in the technology. A study on how these different processes affect the final resistivity and breakdown voltages of a test structure can be found in [36]. However, processes and materials used by semiconductor foundries are confidential, therefore accounting for the effect in simulations is difficult since nothing can be known with certainty. Effects must be measured directly in a laboratory, possibly using the structure suggested in reference [36], or they could be inferred.

It is known that HV-CMOS pixels in this study make use of STI, and SiO₂ is a good assumption of the material. Therefore, a Si–SiO₂ interface would be present in the active area due to the intentional blocking of automatic PWELL generation (discussed later), and is best seen in figure 3.20a. STI is formed everywhere where there is no p+ or n+, including in the spacing between the PWELL and NWELL that respectively enclose the contacts for pixel anodes and cathodes. This volume becomes depleted of charge carriers when the pixel is in operation. The authors of reference [36] mention that defects associated with STI are known to have an effect on CMOS image sensor performance, such as dark currents [37, 38].

In Sentaurus TCAD, traps and fixed charges modify the electrostatic potential by contributing to the charge density in the Poisson equation via the ρ_{trap} term

(equation 3.3). The effects of Q_f and Q_{it} are not accounted for automatically however, and must be specified by the user. To model the combined effect of Q_f and Q_{it} ($Q_{it,f}$), charge trapping was added to the simulations above by defining uniformly distributed fixed positive charges at the Si-SiO₂ region interfaces. Although not strictly correct - since Q_{it} is bias dependent [23] and Q_f reside close to but not directly at the interface - a comprehensive study goes beyond the scope of this work and this method reduces all required variables to one, the concentration. The effects should however be possible to simulate more precisely using a combination of fixed charges, dynamic trap occupation and a transient ramp, knowing the appropriate trap concentrations, energy levels, and capture and emission cross-sections.

Since the concentration of defects in this technology is not known, simulations were initiated using the lower limit $Q_{it} = 10^{10} \text{ cm}^{-2}$ suggested in reference [23], and increased arbitrarily until V_{BD} was similar to the expected value. The results can be seen in figure 3.23. It can be seen that the breakdown is approximately the same as the expected value when $Q_{it} = 6.0 \cdot 10^{11}$, the same order of magnitude proposed by the model in reference [39], which used a value of $4.0 \cdot 10^{11}$ for oxide charge concentration of unirradiated devices. This is also within the range given by reference [40] (10^{10} – 10^{12}). In reality, the number presented in this work is most likely lower since it is demonstrated in the next chapter that performing a 3D simulation of the junction shows that the square shape of the corner gives rise to a region of high electric field decreasing the breakdown voltage. It should be noted that the leakage current is not affected much so more studies need to be done, also seen in the next chapter.

3.2.3.4 Miscellaneous simulation details

As the aim of this study is to compare 2D simulations with laboratory measurements, the third dimension must be accounted for. By default, Sentaurus Device sets the third dimension (in this case, the length of the pixel) equal to $1 \mu\text{m}$. In other words, the area factor of the simulation **AreaFactor** = $1 \mu\text{m}$. Therefore, to approximately compare with laboratory measurements, the current must be multiplied by the remaining dimension of the pixel, which is about $50 \mu\text{m}$. In the example breakdown methods, for the **Transient** command, the break criterion was set to 1 nA, which when multiplied by 50, would increase the current by almost two orders of magnitude to $0.1 \mu\text{A}$. In measurements however, typically the compliance current is set to $10 \mu\text{A}$ or even 10 mA when leakage currents are particularly high. Therefore, to properly characterise the simulated curve postbreakdown and compare with measurements, the break criterion of the **Transient** command was set to 0.1 mA.

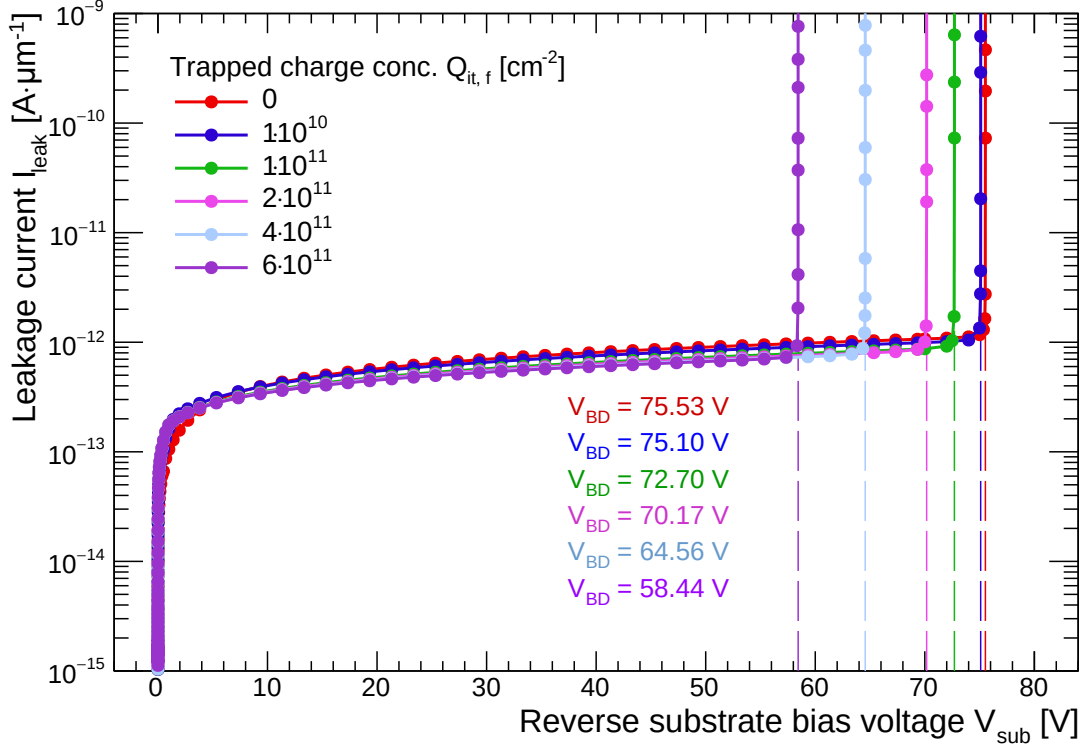


Figure 3.23: I - V simulations with charge trapping at Si-SiO₂ interfaces.

3.3 Simulation of radiation damage

A study of the I - V behaviour and depletion depth of pixels after effects due to radiation damage was performed using Sentaurus TCAD. Radiation damage was modelled using the University of Perugia model [3], which is deemed to be sufficient to model radiation damage up to a neutron equivalent fluence of $2.0 \cdot 10^{16} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$, similar to the maximum fluence accumulated during the lifetime of silicon detectors at the HL-LHC. The model includes both bulk and surface radiation damage effects, but only bulk effects are considered here in order to compare with measurements of irradiated samples presented in chapter 5.

3.3.1 Microscopic model

Defects introduced into the silicon lattice by radiation are modelled by additional energy levels in the silicon bandgap where charge trapping can occur. In TCAD simulations, these energy levels are described by: the trap type, acceptor (donor) types are uncharged when empty and positively (negatively) charged when occupied; the energy level in terms of the conduction band energy E_C ; the electron and hole trapping cross-sections, σ_e and σ_h ; and the trap introduction rate η . The trap concentration N_{trap} can be calculated by assuming a linear increase with neutron equivalent fluence Φ_{eq} related by η [41].

$$N_{\text{trap}} = \eta \Phi_{\text{eff}} \quad (3.17)$$

The table of the energy levels from reference [3] is given in table 3.5.

Table 3.5: Bulk radiation damage model from reference [3] where E_C is the conduction band energy, η is the trap introduction rate, and σ_e and σ_h are the electron and hole capture cross-sections.

Trap type	Energy [eV]	η [cm ⁻¹]	σ_e [cm ²]	σ_h [cm ²]
Donor	$E_C - 0.23$	0.006	$2.3 \cdot 10^{-14}$	$2.3 \cdot 10^{-15}$
Acceptor	$E_C - 0.42$	1.613	$1.0 \cdot 10^{-15}$	$1.0 \cdot 10^{-14}$
Acceptor	$E_C - 0.46$	0.900	$7.0 \cdot 10^{-15}$	$7.0 \cdot 10^{-14}$

3.3.2 Macroscopic effects

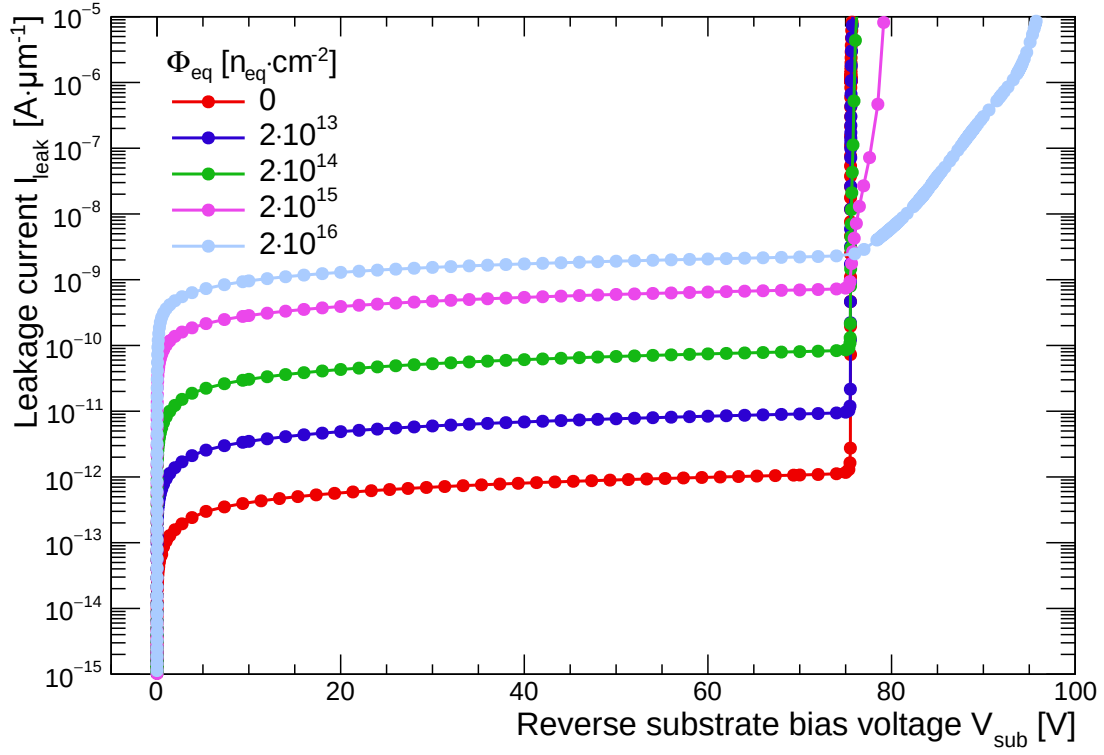
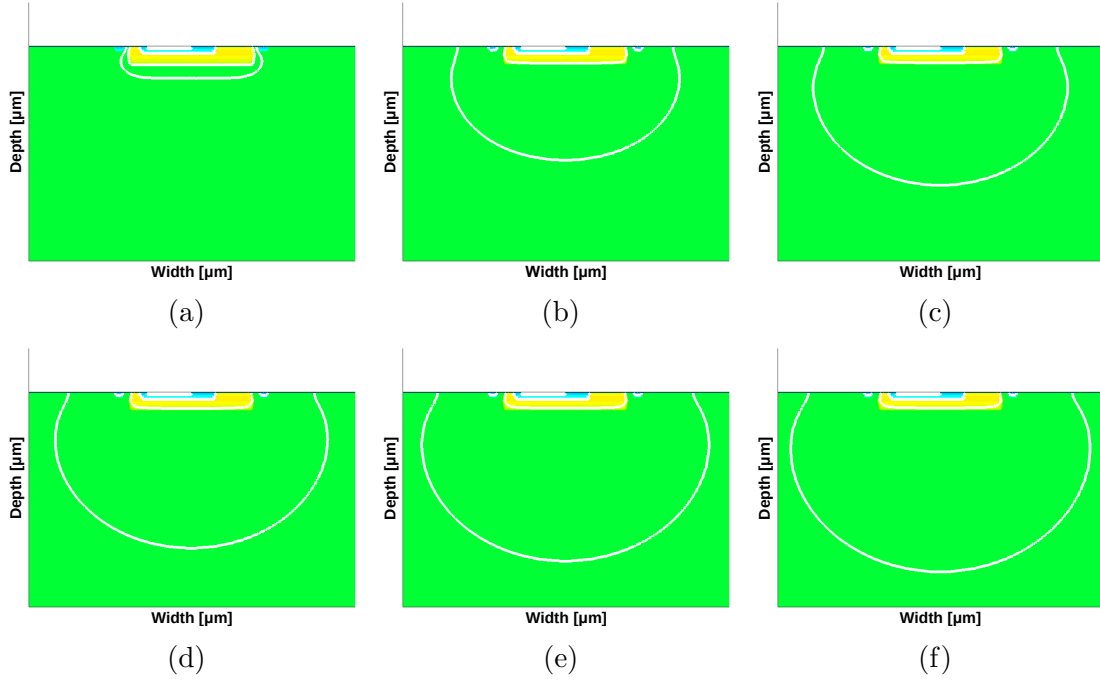
3.3.2.1 I – V characteristics

The model was added to the Sentaurus device breakdown simulations presented in the previous sections and performed on single pixels. The simulated reverse I – V characteristic curves for four fluences can be seen in figure 3.24. The reverse saturation current increases with fluence which is expected when additional energy levels are introduced into the forbidden gap and is seen in measurements presented in chapter 5. Another pleasing effect of the model is the softening of the breakdown for higher fluences which is also seen in the measurements. This possibly due to the change in effective doping concentration, and variations in the electric field distribution as mentioned in [3].

3.3.2.2 Depletion region depths

Snapshots of the I – V simulation are saved at 10 V intervals, which can be seen in figure 3.25. The colours of the plot represent doping concentration, and the boundaries of the depletion region are drawn with a solid white line. As the substrate bias voltage is increased, the depletion region grows downwards and laterally into the lower doped substrate.

To calculate the depletion depth, the Sentaurus Visual program offers a tool to extract the simulated edges of the depletion region [42]. This is where the tool draws the white contour lines in the figures. However, this method fails for high fluence simulations. Therefore a new method was developed, based on the technique in reference [7] except that the edges are calculated using the p-substrate hole density instead of the space charge. This is because Sentaurus Visual calculates the edge of the depletion region using the formula:


 Figure 3.24: Simulated reverse I - V characteristics for radiation damaged pixels.

 Figure 3.25: Simulated depletion regions for $\Phi_{eq} = 0$ for substrate bias voltages $V_{sub} =$ (a) 0 V. (b) -10 V. (c) -20 V. (d) -30 V. (e) -40 V. (f) -50 V.

$$n \cdot \frac{\rho_n}{N} - p \cdot \frac{\rho_p}{N} = 0.05 \quad (3.18)$$

where N is the doping concentration, ρ_n and ρ_p are the electron and hole densities, and:

$$n = \max\left(\frac{N}{|N| + 1}, 0\right) \quad (3.19)$$

$$p = \max\left(\frac{-N}{|N| + 1}, 0\right) \quad (3.20)$$

Since Sentaurus considers p-type doping as negative i.e. $N_A < 0 < N_D$, the doping concentration is $N = -6.986 \cdot 10^{12} \text{ cm}^{-3}$ for a p-type substrate of resistivity $\rho = 1900 \Omega \cdot \text{cm}$. Therefore equations 3.19 and 3.20 approximate to $n = 0$ and $p = 1$, respectively. Equation 3.18 rearranged for ρ_p therefore becomes:

$$\rho_p = 0.05 \cdot N \quad (3.21)$$

This means that the contour lines are drawn when the hole density is 5% of the doping concentration.

A vertical cut of the hole density scalar field is taken at the centre of the pixel for each substrate bias voltage. These profiles for the lowest and highest simulated fluence are shown in figure 3.26. The high values of hole density on the left of each plot corresponds to the PSUB layer. The scale of the hole density is zoomed to retain confidentiality of the PSUB hole concentration, and horizontal scale has been removed to keep the implant depth confidential. The vertical black lines in figure 3.26a are the edges of the depletion region extracted using the Sentaurus Visual tool, which are not available for figure 3.26b and therefore not shown. The dashed lines are depletion edges calculated using the new method presented here. To do this, the profiles are fitted with error functions:

$$\rho_p(z) = \frac{|N_{\text{eff}}|}{2} \cdot \left(\text{erf}\left(\frac{z - A}{B}\right) + 1 \right) \quad (3.22)$$

where N_{eff} is the effective doping concentration of the substrate (which changes with fluence), z is the depth of the substrate, and A and B are free parameters to fit the curve. A corresponds to the switching point of the error function and B is its slope. The boundary of the depletion region is evaluated when the value of the error function exceeds 10% of the fitted N_{eff} rather than 5% as equation 3.18 states, as this matched with the Sentaurus Visual tool better.

The width of the depletion region W_D was then calculated by subtracting the depth of p-substrate–DNWELL junction from the depletion region boundary as the pixel implants are assumed not to be depleted. This assumption is not strictly cor-

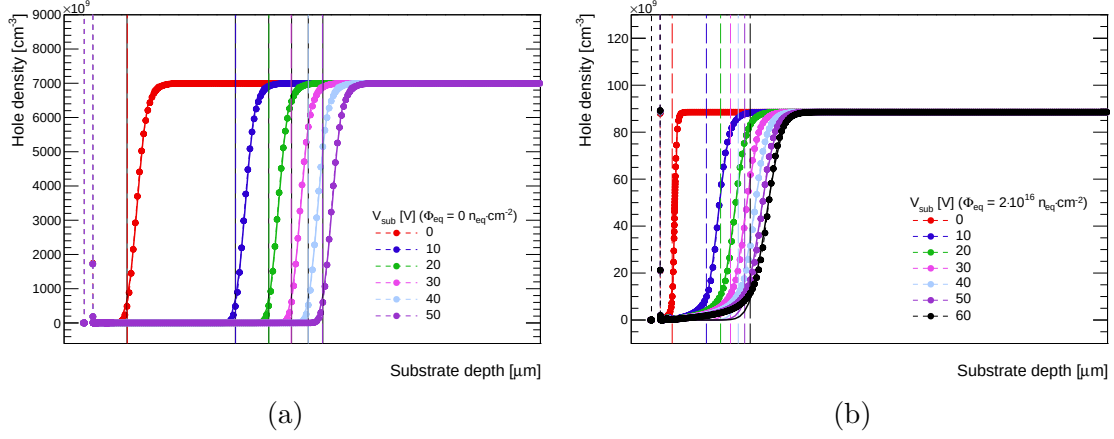


Figure 3.26: Vertical cuts at the centre of the pixel for simulated hole densities at different substrate bias voltages for (a) $\Phi_{\text{eq}} = 0$ n_{eq}·cm⁻². (b) $\Phi_{\text{eq}} = 2 \cdot 10^{16}$ n_{eq}·cm⁻². The black vertical lines in (a) are the extracted depletion edge values from Sentaurus Visual. The dashed lines in both figures are the calculated depletion edge values from the fits.

rect however, since the depletion region also grows slightly into the DNWELL. A better calculation of W_D would therefore also require evaluation of the boundary of the depletion region in the DNWELL implant using the electron density. Nevertheless, the depth of the p-substrate–DNWELL junction is automatically evaluated by Sentaurus Visual when the net doping concentration ($N_D + N_A$) is equal to zero. The calculated W_D is plotted as a function of V_{sub} and Φ_{eq} in figure 3.27. The simulation demonstrates what is seen in measurements such as those in figures 2.14a and 2.14b in the previous chapter and that will be presented here in chapter 5. W_D generally decreases as Φ_{eq} increases. This can be mitigated somewhat by increasing V_{sub} , but there is a general decrease in the volume of the depleted area as the substrate becomes more damaged.

3.4 Summary

This chapter outlines the techniques used to simulate HV-CMOS pixels in chapters 4 and 5 of this thesis. The aim of this work was to provide a simulation framework that could be used to accurately reproduce the doping profiles of all implants a given CMOS technology, which could be used to generate any required structure very quickly. Electrical behaviour of the generated structure could then be simulated to predict performance of devices before fabrication, potentially saving both money and time.

Individual implants in the LFoundry 150 nm HV-CMOS process were simulated using MC process simulations and characterised mathematically to create individual doping profiles of each implant. These doping profiles were then combined to gener-

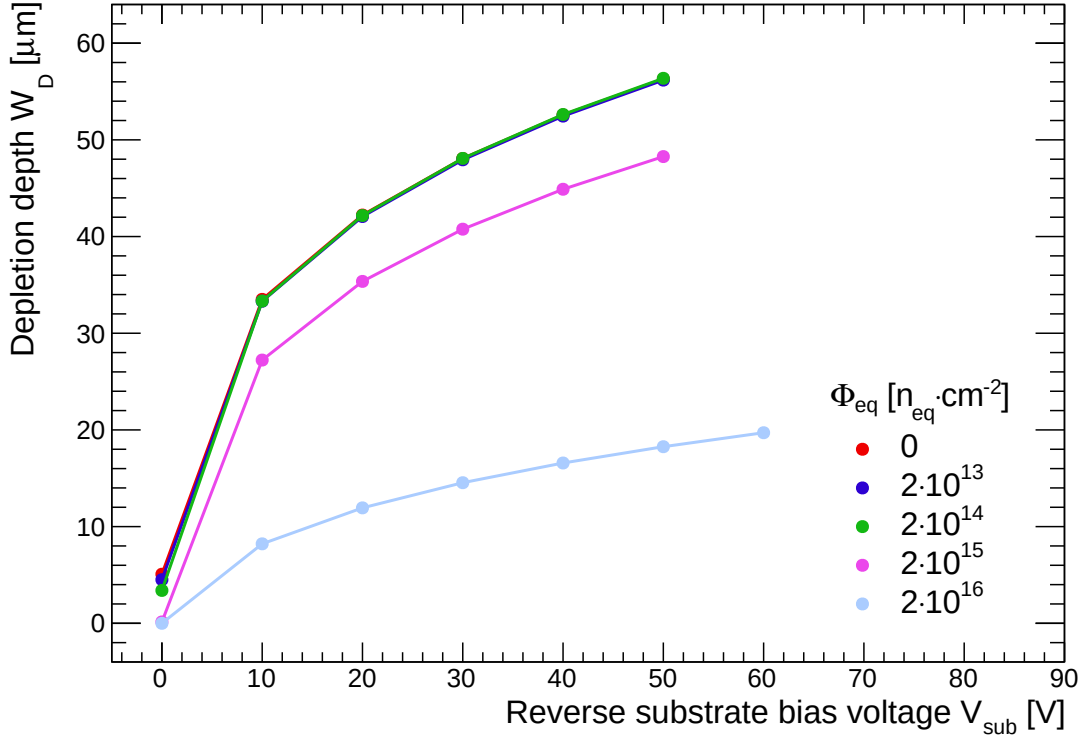


Figure 3.27: Simulated reverse I - V characteristics for radiation damaged pixels.

ate a 2D cross-section of an HV-CMOS particle detector, RD50-MPW2 requiring a computing time of < 1 minute (“fast structure”). A physically more accurate, identical structure was simulated using pure MC process simulations requiring > 2 days of computing time (“slow structure”). To verify the accuracy of the fast structure, results of reverse I - V characteristic simulations were compared with the results of the same simulations of the slow structure. Differences in the simulations were minimal, suggesting that the technique described here could be used to accurately generate any desired structure and simulate electrical behaviour, without the need for lengthy process simulations. This technique could also possibly be extended to other technologies.

A study of the example breakdown simulation methods provided with the Sentaurus TCAD tool suite from Synopsys was also given. Building on this, a fast, accurate method for simulating the reverse I - V characteristics of pixel diodes was developed and presented. The accuracy of this technique was verified by comparing extracted breakdown voltages of the generated RD50-MPW2 pixel (fast structure) with the value expected by the manufacturer which was shown to match well. The simulation was further validated by reproducing trends seen in depletion depth measurements before and after irradiation, and I - V characteristics after irradiation. The methods used in these simulations are also presented.

It should be noted that not all simulations in this thesis have been performed

using the doping profiles extracted here. This is due to the fact that this work was completed during the simulation stage of RD50-MPW2 development, sometime after investigations into RD50-MPW1 had finished. The next chapter discusses the TCAD simulations used to investigate RD50-MPW1 and how the simulations presented in this chapter were used to develop RD50-MPW2. A note will be made when old doping profiles have been used.

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Chapter 4

Optimising detector parameters

As discussed in chapter 2, two important parameters of pixels in HV-CMOS detectors are the breakdown voltage V_{BD} and the leakage current I_{leak} . As pixels in HV-CMOS technologies are reverse biased diodes, V_{BD} determines the maximum voltage pixels can be operated at. I_{leak} determines the noise in particle detection signals and an increase in I_{leak} increases the power dissipation in detectors [1]. To quickly summarise the information from chapter 2, a high V_{BD} is desirable as maximising the operating voltage V_{sub} improves performance both before and after damage due to irradiation. A higher V_{sub} is beneficial as this results in larger depletion regions and faster charge collection. When particles cross this sensitive depletion region, charge carriers are generated and drift to the electrodes due to the electric field. A larger depletion region means more charge is collected which increases the signal-to-noise ratio (SNR) of the signal created by the traversing particle. A high V_{sub} is also used to mitigate effects due to radiation damage. After irradiation, the resistivity of the substrate changes, decreasing the size of the depletion region which can be counteracted by increasing V_{sub} . Damage to the silicon lattice also introduces energy levels into the forbidden gap. Increasing V_{sub} can reduce the probability that moving charges will become trapped in these energy levels, maintaining a high SNR. Irradiation also increases I_{leak} . A lower I_{leak} is beneficial as the higher this current, the lower the SNR and power dissipation. As samples become irradiated during use in high radiation experiments, this effect only worsens. A device with an initially low I_{leak} could exhibit lower leakage currents also after irradiation.

Therefore, it is important to be able to predict how certain design choices might affect I_{leak} and V_{BD} before fabrication. This chapter is split into two halves which each discuss a case study of a prototype developed within the RD50 collaboration at CERN. RD50-MPW1 in section 4.1 and its successor RD50-MPW2 in section 4.2. RD50-MPW1 was submitted for fabrication in 2017, and laboratory measurements of fabricated devices showed that they suffered from high I_{leak} . TCAD simulations were used to investigate the reasons for this high I_{leak} and are presented. The cause

was determined to be the presence of silicide in the active areas of the devices injecting charge into the depletion region.

RD50-MPW2 was designed and submitted in 2019 as part of this thesis, and laboratory measurements demonstrate that both I_{leak} and V_{BD} have been significantly improved compared to RD50-MPW1. The TCAD simulations used to identify the best conditions for increasing V_{BD} and reducing I_{leak} for the design of RD50-MPW2 and its pixels are presented. This includes studies of isolating silicide in active areas to reduce I_{leak} , and increasing pixel electrode spacing and modifying pixel corner geometry to increase V_{BD} . The laboratory measurements of RD50-MPW2 verifying the design choices are also shown. Analysis of the results show that RD50-MPW2 pixels with the same electrode spacing as those in RD50-MPW1 ($3\text{ }\mu\text{m}$) have the same $V_{\text{BD}} \approx -57\text{ V}$ but much lower I_{leak} compared to RD50-MPW1. However those pixels in RD50-MPW1 and RD50-MPW2 have square and rounded corner geometries, respectively. The square corners were confirmed not to be the cause of high I_{leak} as three other types of pixel were implemented into RD50-MPW2 and tested in the laboratory. The three pixel types have square, rounded, and chamfered corners respectively, and each have a pixel electrode spacings of $8\text{ }\mu\text{m}$. For each pixel measured, $V_{\text{BD}} \approx -127 \pm 3.5\text{ V}$ and I_{leak} is similar. This confirms that the changes made with respect to the silicide in RD50-MPW2 are the cause of the improved I_{leak} compared to RD50-MPW1.

As a brief introduction to content of the following chapter, laboratory measurements of reverse I - V characteristic curves of two pixels are shown in figure 4.1. One $50\text{ }\mu\text{m} \times 50\text{ }\mu\text{m}$ pixel from RD50-MPW1 and one $50\text{ }\mu\text{m} \times 50\text{ }\mu\text{m}$ from RD50-MPW2 in solid black and red lines respectively. The details of the measurements are discussed later however it can be seen that I_{leak} of a single RD50-MPW1 pixel reaches almost 0.1 mA before -30 V , which is much too high. With the compliance current set to 10 mA , I_{leak} continues to increase, and a breakdown can be seen at around -57 V . In the measurement of a single RD50-MPW2 pixel the reverse saturation current is much lower and stable at around 100 pA , demonstrating that the studies presented here reduced I_{leak} by many orders of magnitude. These measurements were performed at room temperature.

4.1 RD50-MPW1

RD50-MPW1 [2] is an MPW submission in the 150 nm HV-CMOS process from LFoundry [3]. It was developed and submitted as part of the CERN RD50 collaboration in November 2017 and fabricated in two substrate resistivities, $500\text{ }\Omega \cdot \text{cm}$ and $1900\text{ }\Omega \cdot \text{cm}$. Figure 4.2a shows the layout of the detector. The device consists of two large matrices of pixels, one at the top for photon counting applications and

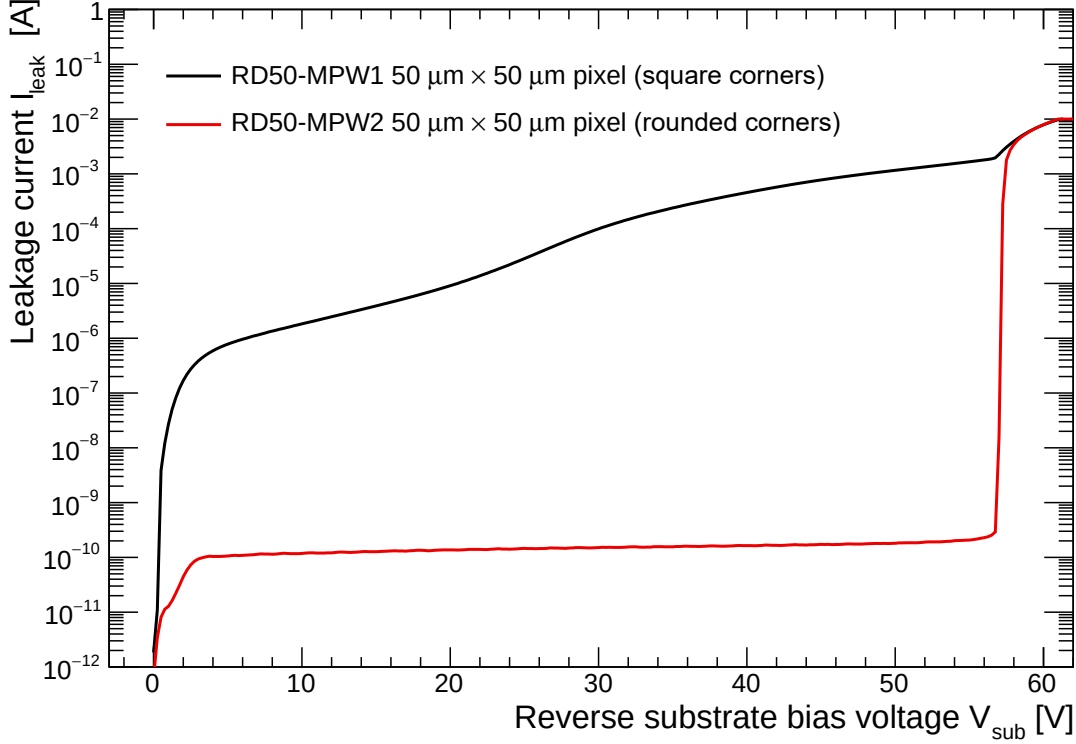


Figure 4.1: Measurements of reverse I - V characteristic curves of single, $50\ \mu\text{m} \times 50\ \mu\text{m}$ pixels from the RD50-MPW1 (black) and RD50-MPW2 (red) prototypes.

one at the bottom for particle physics experiments and test structures were included along the top edge of the device. Figure 4.2b shows a test structure that consists of a 3×3 matrix of passive, $50\ \mu\text{m} \times 50\ \mu\text{m}$ pixels that is the focus of this study. This test structure was included for e-TCT measurements and the pixels share the same design as pixels in the particle physics matrix but do not include readout electronics. The test matrix includes two readout channels. One for the central pixel, and one for the outer eight pixels that are shorted together.

A cross-section diagram of one of the pixels in the particle physics matrix is displayed in figure 4.3a. The pixel is implemented following the method described in [4] and functions in the same way as the pixels described in the last two chapters. The p-substrate (anode) and DNWELL (cathode) form the pixel p-n junction diode. The diode is reverse biased by biasing the p-substrate to a negative voltage through the p+/PWELL stacks on the outer edges of the pixel and the DNWELL is biased through the n+/NWELL/NISO stacks to 0 V which forms the depletion region which is the sensing volume for particle detection. The DNWELL is also used in combination with the n+/NWELL/NISO stack ring to isolate PMOS and NMOS electronics from the high voltage p-substrate. Like RD50-MPW2 described in the last chapter, this cross-section includes the wider n+/NWELL/NISO stack on the right-hand side which is slightly wider to include room for biasing electronics. The

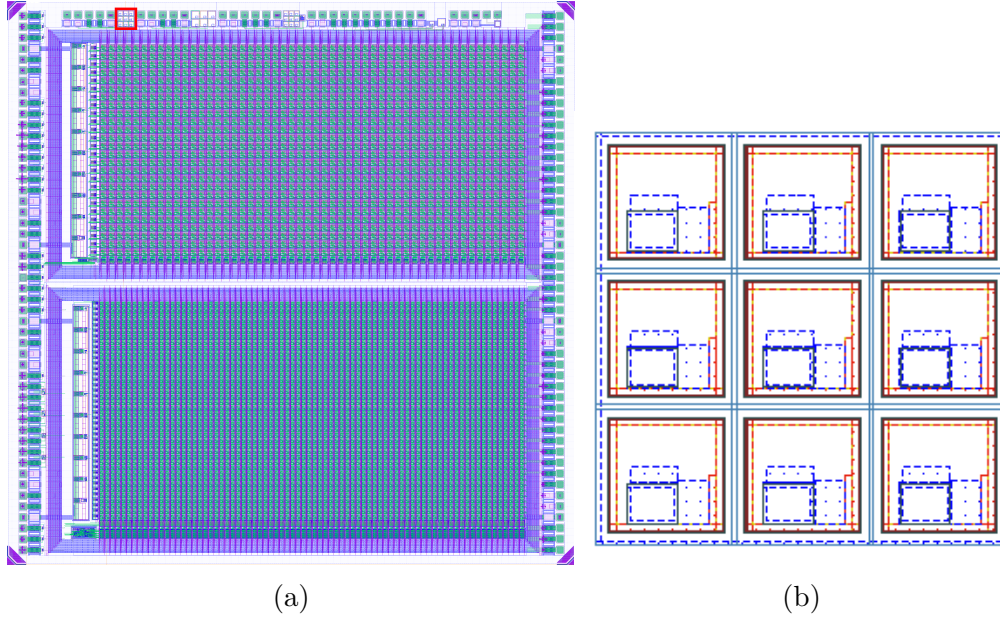


Figure 4.2: (a) RD50-MPW1 layout. A test structure is highlighted at the top in red. (b) Test structure consisting of a 3×3 matrix of $50 \mu\text{m} \times 50 \mu\text{m}$ pixels for e-TCT measurements.

PSUB layer here is also narrower than that of the typical pixel described in chapter 2 to reduce the PSUB–DNWELL capacitance.

Fabricated samples of RD50-MPW2 were received in April 2018 and I – V measurements were conducted on the central pixel of the test structure shown in 4.2b [5]. A cross-section of one of the pixels can be seen in figure 4.3b. The reverse I – V characteristics that were also conducted as part of this study show the pixel exhibits a similar reverse breakdown voltage of around -57 V . This value is expected according to the LFoundry 150 nm technology documentation which states devices should have a breakdown voltage around -60 V . This is due to the geometry of the cross-section, specifically, the $3 \mu\text{m}$ spacing between the pixel diode electrodes (this is expanded upon in the following sections). However, the pixel had a much higher leakage current than expected. Despite this, it was still possible to do e-TCT measurements of irradiated devices [6], demonstrating that devices still work successfully as particle detectors. However, in order to improve future submissions TCAD simulations were used to study the design of the device, and determine the cause of the high leakage current. The following section describes the investigation of the high leakage current of RD50-MPW1.

4.1.1 Investigation of high I_{leak}

4.1.1.1 I – V measurements

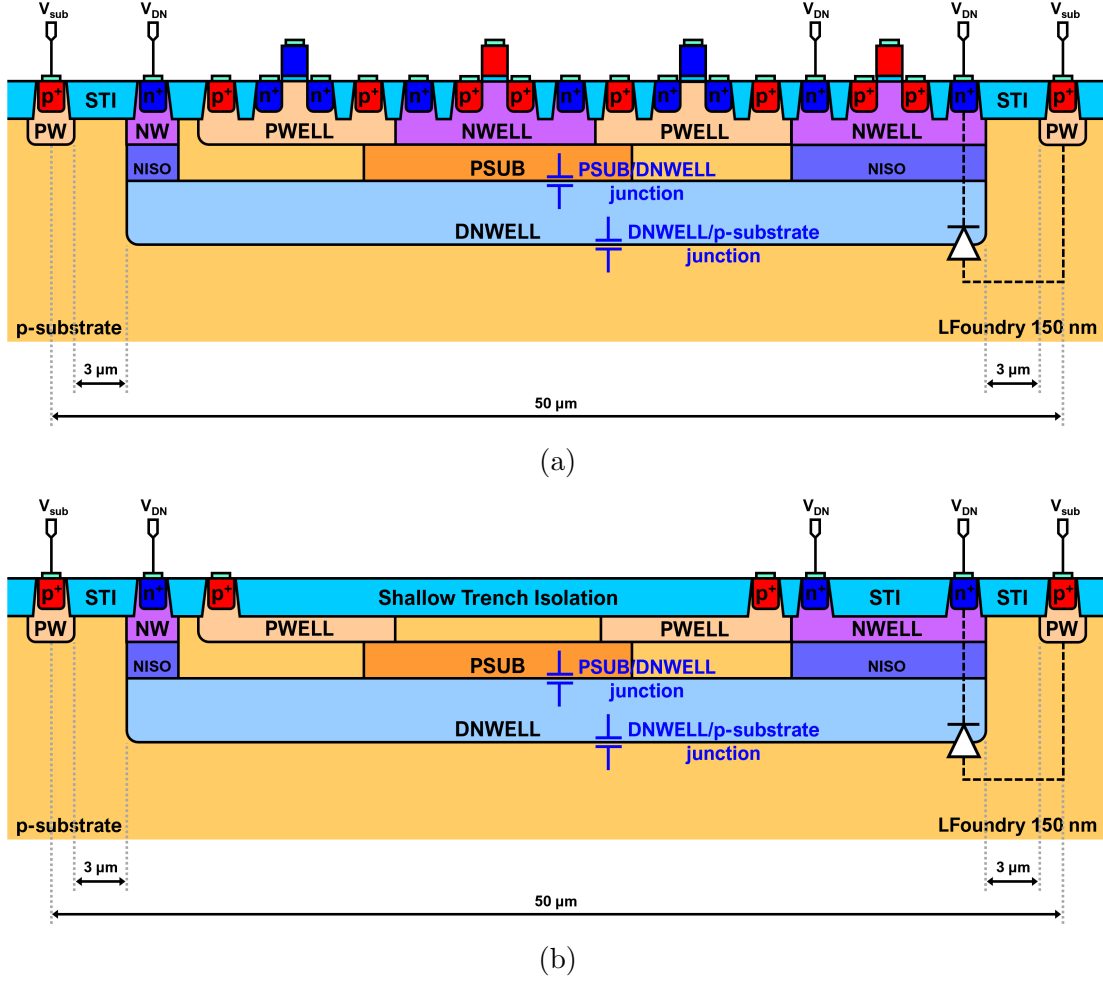


Figure 4.3: (a) Cross-section diagram of one pixel from the RD50-MPW1 particle physics matrix. (b) Cross-section diagram of one pixel from the RD50-MPW1 e-TCT test structure matrix.

It is clear from the results of the measurement of a single RD50-MPW1 pixel in figure 4.1 (solid black line) that the leakage current is high. This is especially clear when compared to an $I-V$ measurement of a similar pixel from RD50-MPW2, implemented specifically with a similar geometry to compare with RD50-MPW1. The changes made to this second prototype will be discussed in the next half of this chapter, and the experimental method used to test RD50-MPW1 will be described in this section.

The test structure highlighted in figure 4.2b provides five pads: a substrate contact; a pad for the DNWELL of the central pixel, which has protection diodes; a pad for the DNWELLs of the outer neighbouring pixels that are shorted together, which also has protection diodes; and two pads for biasing the protection diodes, one for each electrode. The p-type wells inside the pixels were shorted to the anodes of the protection diodes in the ASIC design. The location and layout of the test structure can be seen in figure 4.4. Samples were measured using a probe station

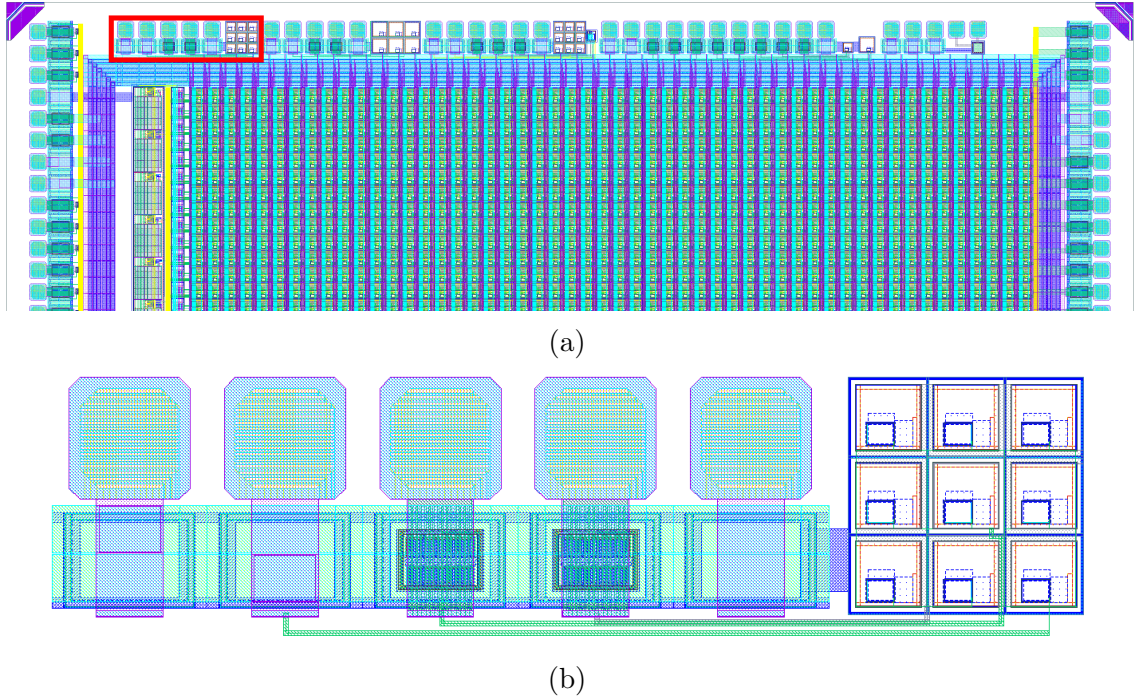


Figure 4.4: (a) Zoom of top half of RD50-MPW1 layout. The test structure and pads is highlighted with a red square. (b) Layout of RD50-MPW1 test structure for e-TCT measurements.

with four test probes in a dark cabinet. The four test probes were each connected to four separate source meter units (SMUs) with a shared ground. One probe was connected to each protection diode pad, one probe was connected to the pad for the central pixel, and one probe was connected to the substrate pad. The protection diodes were reverse biased by applying a small positive voltage to the cathodes (1.8 V in this technology) using one of the source meters, and the anodes were biased to 0 V using a second source meter. The pixel was also biased to 0 V using a third source meter. Using a ramp speed of $-1 \text{ V} \cdot \text{s}^{-1}$ and a step size of 0.25 V, the substrate was slowly ramped to high negative voltage using the fourth source meter connected to a computer. The measurement was halted when the SMUs reached compliance current (10 mA). The result is the black line in figure 4.1.

4.1.1.2 Cause of high I_{leak}

In this design, it was discovered that the cause (or at least, the main cause) of the high leakage current was due to *salicidation* on the surface of the substrate. Salicidation is term used for a process in CMOS ASIC fabrication and is a contraction of **self-aligned silicidation**. Silicidation is the process of reacting metal (such as Ti) with the silicon substrate (or polysilicon gates) to form a metal silicide (such as TiSi_2). It is known as self-aligned as it does not require photolithography like other processes such as implantation. Patterning is instead achieved by exposing silicon

(and polysilicon) underneath a previously grown dielectric such as SiO_2 , via etching. Metal is then deposited over the entire wafer and annealed and only exposed areas react with the metal. The metal silicide goes on to be used in the creation of low resistance contacts in future process steps. In a similar fashion to polysilicon and metal layers, silicide also includes dummy filling structures that generate in “empty” areas of the design, to satisfy foundry minimum density requirements.

In order to avoid dummy silicide structure generation directly into active areas, LFoundry also automatically generates PWELL in areas of the design left empty. Therefore it must be kept in mind that in order to create a cross-section like those in figures 4.3, another layer not shown in those diagrams must be used. A layer specifically for blocking the automatic generation of PWELL known in the technology as PWELL blockGen. This is demonstrated in figure 4.5a. PWELL is still implanted where it is purposefully intended by the designer. If PWELL blockGen is not used, the cross-section in figure 4.5b would be created and, if fabricated, would cause a similar problem to that of the LFHVMAAPS_FEI3 chip described in [7]. The distance between the PWELL enclosing the substrate contacts and n-type wells that make up the pixel would be $0\text{ }\mu\text{m}$ and the breakdown voltage reduces

Therefore in RD50-MPW1, this PWELL blockGen layer was used, in order to maximise the breakdown voltage. However, it was erroneously placed over other areas of the chip, without taking into account the other automatically generated structures, such as silicide. Therefore during fabrication, silicide was generated directly on the surface of the substrate in empty areas. This can be best seen in test structure measured in the previous section. Of the five pads in figure 4.4b, two contain protection diodes (the third and fourth, from the left) that can be seen below the pad contact plates. The regions of the silicon substrate directly underneath the contact plates, to the left and right of the pad diodes, and in between p-substrate/DNWELL junction electrodes are left empty, except for PWELL blockGen. These areas on the surface of the substrate were therefore filled with silicide structures during fabrication. The cross-section of the intended pad diode is depicted in figure 4.6a. In this cross-section, the p-substrate–DNWELL diode houses the p-well–n+ protection diodes. The structure is similar to that of a pixel, except it is wider, and the spacing between the p-substrate–DNWELL diode electrodes is $10\text{ }\mu\text{m}$. This means that with the inclusion of the PWELL blockGen layer, this diode will have a breakdown voltage larger than that of the pixels. However, figure 4.6b depicts what was fabricated. Silicide filling layers were generated directly on the surface of the substrate, including in the guard rings of all electronics blocks (e.g., bias block, config registers, etc.) or in other words, active areas. When the substrate underneath the filling structures become depleted, the leakage current increases due to charge injection.

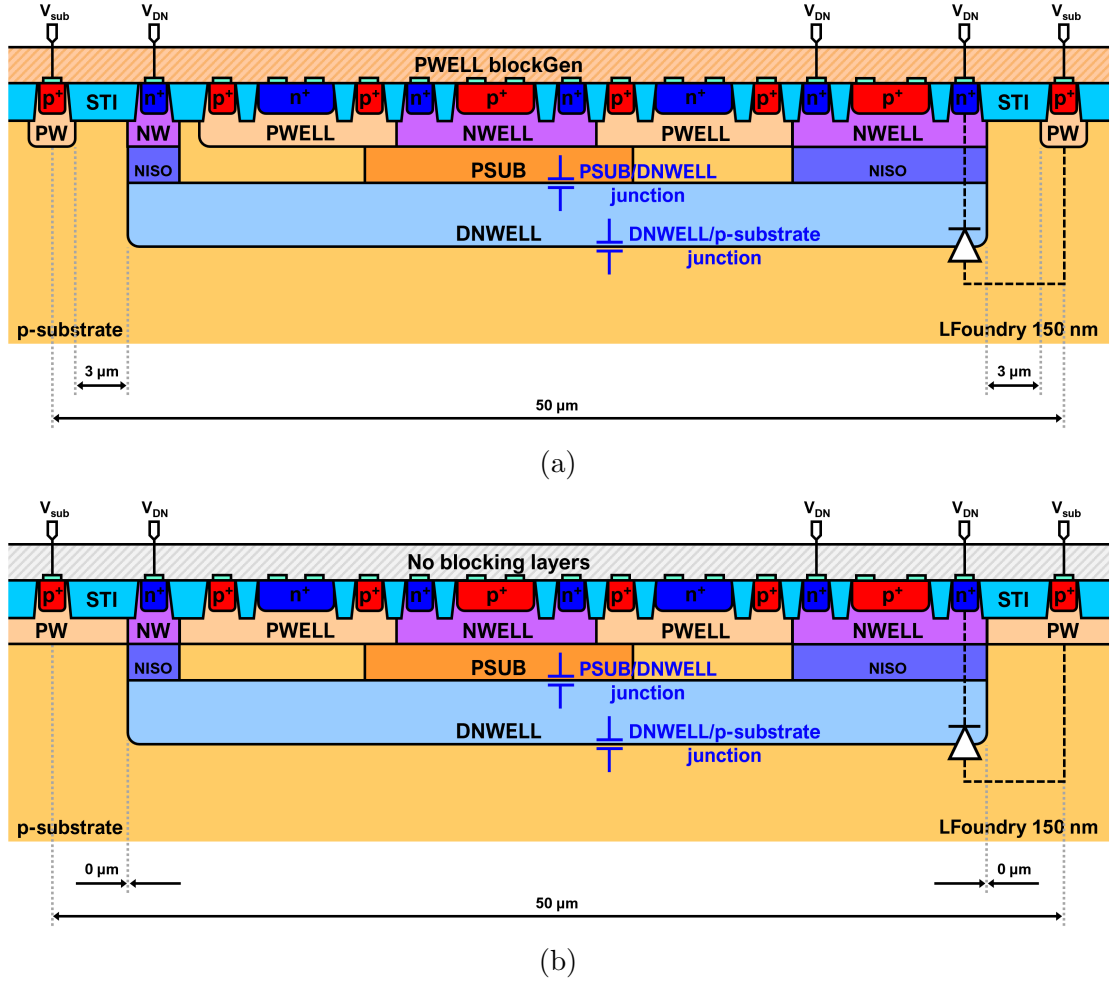


Figure 4.5: (a) Diagram of RD50-MPW1 pixel cross-section demonstrating placement of PWELL blockGen layer. (b) Hypothetical pixel cross-section demonstrating how cross-section in (a) would change without PWELL blockGen. STI has not been included in these figures for simplicity.

4.1.1.3 Simulation of high I_{leak}

This was simulated using Sentaurus Structure Editor. As a caveat, this and some of the other Sentaurus Structure Editor and Sentaurus Device simulations presented in this chapter were performed in the early stages of the research, before the method in chapter 3 was developed. Doping profiles were taken from [8] which explains some of the differences in doping concentrations seen in figures. It will be mentioned when these previous doping profiles have been used. A large region of silicon was defined and doped with a constant boron doping profile. The silicon was wide enough for the pad diode, defined at the centre, with space on the edge for the filling structures. Ref/eval windows for each well were defined using measurements from the GDS file and the appropriate doping profiles were applied to each window. Trapezium regions of silicon dioxide were defined everywhere there is not n+ and p+. The p+ and n+ wells inside the p-well isolated from the substrate were excluded from the simulation

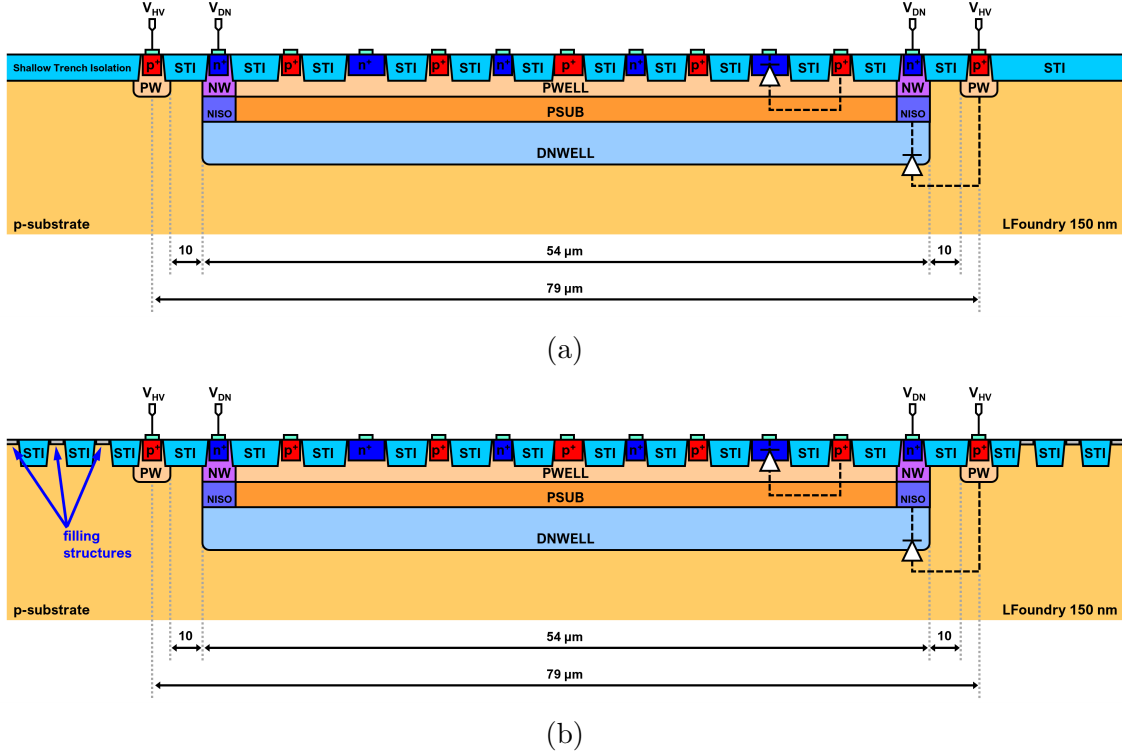


Figure 4.6: (a) Cross-section diagram of the intended pad diode from the RD50-MPW1 test structure (figure 4.4b). (b) Cross-section diagram of the fabricated pad diode. Filling structures were generated on the surface of the substrate, depicted on the right and left of the diagram.

to simplify it. Contacts were placed to enable contact with the substrate and the deep-nwell. The structure can be seen in figure 4.7a. As the control, the structure was designed to mimic the intended cross-section depicted in figure 4.6a where the STI reaches the edge of the structure. This can be seen more clearly in figure 4.7b. To simulate the fabricated cross-section, openings were made in the STI and thin regions of metal silicide were defined. The locations and measurements correspond to those extracted from the postprocessed GDS file. This can be seen in figure 4.7c.

The same Sentaurus Device breakdown simulation described previously was used here on both structures. The n-type layers were biased to 0 V, and the substrate was slowly ramped up to high negative voltage until the current at the anode reached the break criterion. The results of the simulation can be seen in figure 4.8. In black is the ‘ideal’ or intended pad diode design (diagram in figure 4.6a and simulation in figure 4.7b). The breakdown voltage of the pad diode is higher than the simulated pixel in chapter 3 because the spacing between the p-substrate–DNWELL junction is larger (10 μm instead of 3 μm). When the salicide structures are added to the surface of the substrate, the leakage current increases when the depletion region grows laterally and touches them. The results are shown in figure 4.8 in red. It should be noted that this is not as high as the measurements of RD50-MPW1 in

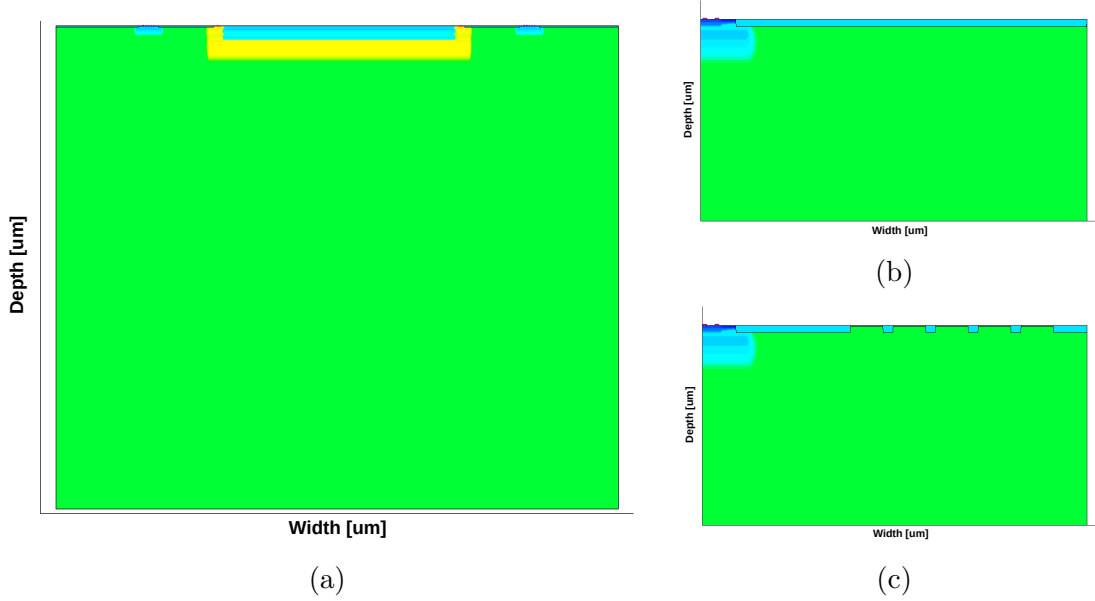


Figure 4.7: (a) Simulation of figure 4.6a. (b) Zoom of top right corner of (a). STI covers the topside. (c) Zoom of top right corner of simulation of figure 4.6b, there are openings in the STI where a very thin layer of conductive material is placed.

figure 4.1, even if the area factor and number of pad diodes is accounted for, but the results are significant as nothing else investigated caused the simulated current to increase as much. Snapshots of the two simulations at $V_{\text{sub}} = -100$ V can be seen in figure 4.9 where the colour of the plots represents total current density from low in blue to high in red. The scales are the same in both images. In figure 4.9a, the current in the substrate is relatively low with respect to that in figure 4.9b where charge carriers can be seen injecting into the depletion region from the metal silicide filling structures.

The inconsistency with respect to measurements is most likely an artefact of the generated structure, rather than the simulation method. A cross-section of the pad diode in the horizontal direction according to figure 4.4 was used. Many more silicide structures reside under the pad plates to the ‘north’ of the pad diode and in fact, cover a large area of the entire chip. It is possible that using a vertical cross-section and a much wider substrate, thus allowing the depletion region to grow laterally and contact more filling structures, would result in a larger simulated leakage current, closer to that seen in measurements. However, the width of substrate needed to reproduce the results is likely too large to simulate effectively. Nonetheless, the conclusions drawn from the simulations are assumed to be correct due to the success of initial RD50-MPW2 measurements. To verify that the simulations presented here can in fact model reality successfully, the measured reverse I – V characteristics of RD50-MPW2, the second prototype, were reproduced. This will be shown in the next chapter.

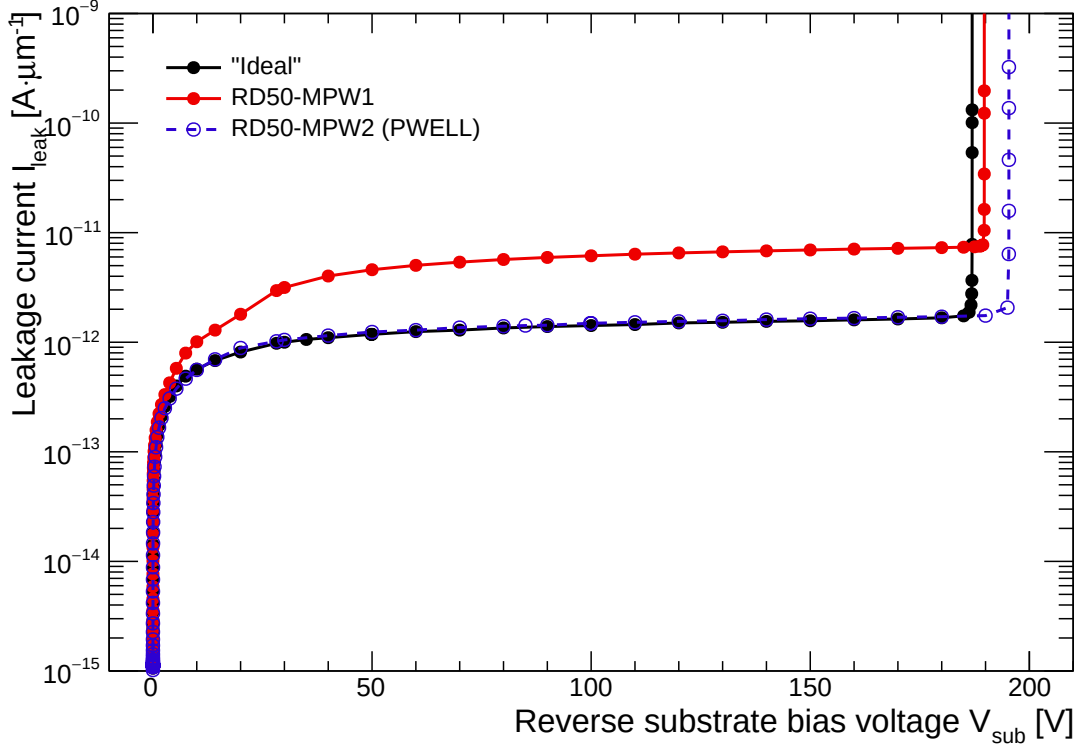


Figure 4.8: I - V characteristic curve simulations of pad diodes in the test structure implemented for e-TCT measurements in RD50-MPW1. Black lines and markers are for the structure shown in figure 4.7b and red for 4.7c. Blue hollow circles represent leakage current when PWELL is used to isolate filling structures.

4.2 RD50-MPW2

RD50-MPW2 [9] is an MPW submission in the 150 nm technology node from LFoundry, like RD50-MPW1. It was also designed by and submitted as part of the CERN RD50 collaboration like RD50-MPW1 in February 2019 but with a wider range of substrate resistivities $10 \Omega \cdot \text{cm}$, and 500 – $1100 \Omega \cdot \text{cm}$, $1900 \Omega \cdot \text{cm}$, and $> 2000 \Omega \cdot \text{cm}$. It has an area of $3212 \mu\text{m} \times 2120 \mu\text{m}$ and was fabricated on $280 \mu\text{m}$ thick wafers. One of the aims of the submission and indeed, the aim of this study was to improve parameters such as the leakage current and breakdown voltage with respect to RD50-MPW1. The layout can be seen in 4.10a. The device consists of a range of structures including: an active 8×8 matrix of $60 \mu\text{m} \times 60 \mu\text{m}$ HV-CMOS pixels, more information can be found in reference [10]; a bandgap voltage reference; single-event upset (SEU) tolerant memories; and test structures on the left and right edges. Test structures on the left include a range of single-photon avalanche diodes (SPADs) and test structures on the right include passive HV-CMOS pixel matrices for e-TCT measurements. These are the main focus of this work. There are four matrices, which each consist of nine pixels arranged in a 3×3 grid. These are very similar to the test structures in RD50-MPW1 and also include two readout

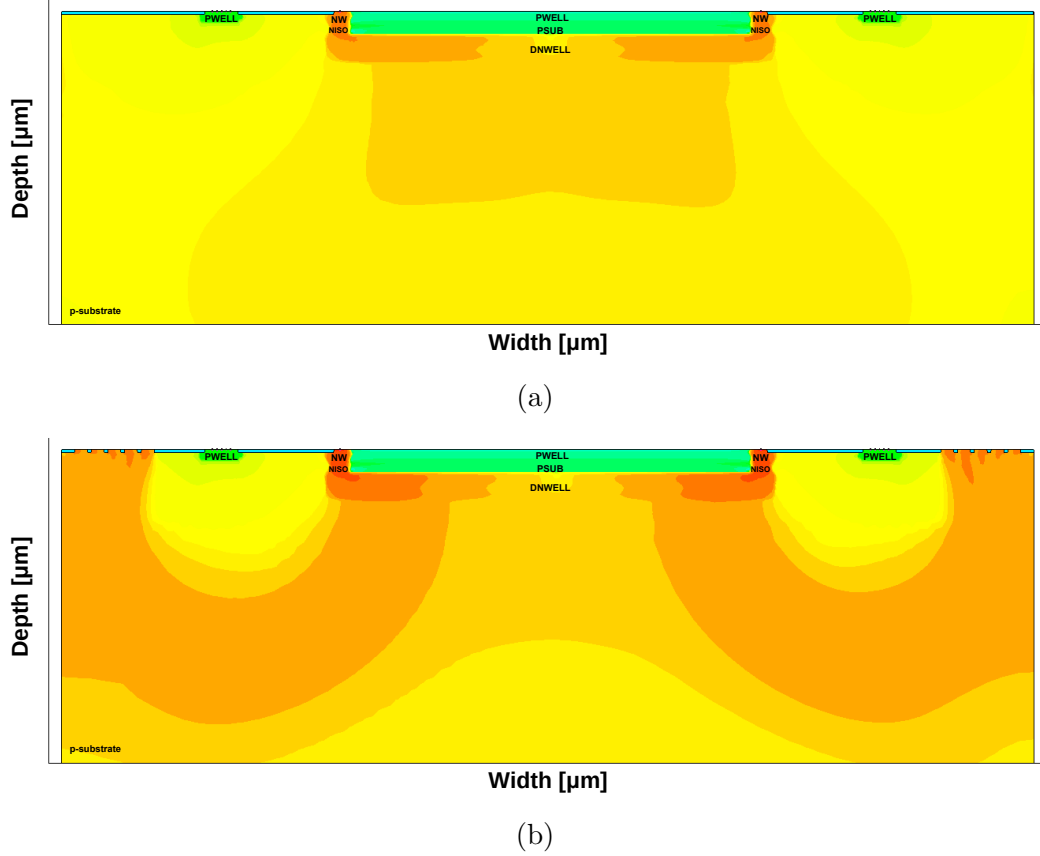


Figure 4.9: (a) TCAD simulation of intended RD50-MPW1 test structure pad diodes. The colour of the plot is total current density. (b) Simulation of fabricated pad diodes. High current density can be seen coming from silicide filling structures on the surface of the substrate.

channels, one for the central pixels and one for the eight neighbouring pixels that are connected in parallel. Pixels in the top test structure are $50\text{ }\mu\text{m} \times 50\text{ }\mu\text{m}$ and were included to compare with RD50-MPW1 measurements. This can be seen highlighted in red in 4.10a and magnified in 4.10b. Pixels in the other three matrices are $60\text{ }\mu\text{m} \times 60\text{ }\mu\text{m}$ to mimic pixels in the active matrix. The difference between these three structures are the shape of the corners.

In this work everything that was learned from simulations (and measurements) of RD50-MPW1 was used to improve the design of this second prototype RD50-MPW2. This section is split into four subsections: simulations that were used to improve both the breakdown voltage and leakage current, and how these things were implemented into the design; I_{leak} measurements of fabricated samples; and simulations reproducing the I - V characteristics. Samples were received in February 2020 and measurements in this study began in March 2020. I - V measurements confirm what was seen in simulations: leakage current is significantly reduced by ensuring silicide filling structures are enclosed in PWELL, increasing the spacing between the electrodes increases the breakdown voltage, and rounding or cutting off

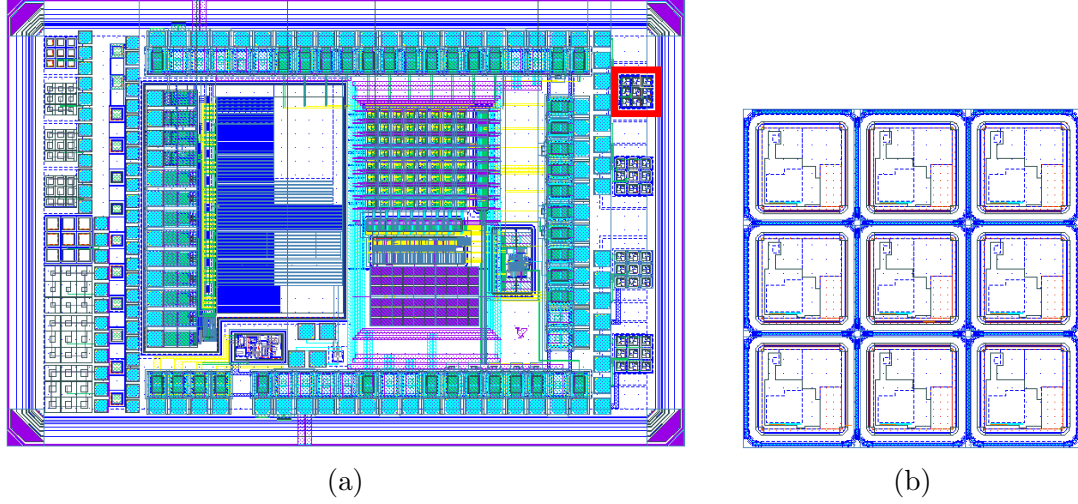


Figure 4.10: (a) RD50-MPW2 layout. A test structure implemented for I – V and e-TCT measurements is highlighted on the right in red. (b) Test structure consisting of a 3×3 matrix of $50 \mu\text{m} \times 50 \mu\text{m}$ pixels with rounded corners.

90° pixel corners has a positive effect on the breakdown voltage.

4.2.1 Improving leakage current

The leakage current was the main problem with RD50-MPW1 and something to avoid in RD50-MPW2. The main cause was due to silicide on the surface of the substrate. In accordance with advice given by the foundry, this can be solved by ensuring automatically generated silicide filling structures are enclosed in PWELL and not in contact with active areas. In this section, this will be demonstrated with simulations. Simulations were based on those used to study the RD50-MPW1 leakage current with the previous doping profiles from reference [8].

4.2.1.1 Silicide

Despite the fact that RD50-MPW1 samples perform well as detectors, it was important to lower the leakage current in the RD50-MPW2 prototype. As mentioned in the previous sections, erroneous use of the PWELL blockGen layer was the cause of metal silicide growth in active areas of the samples. Careful placement of this layer allows spacing of pixel electrodes to ensure high voltage, but also automatic generation of PWELL to contain dummy silicide filling structures. This is represented in figure 4.11. When PWELL blockGen is placed over the whole substrate, PWELL will not generate automatically, and other automatically generated structures will do so on the surface of the substrate (figure 4.11a). If PWELL blockGen is placed intentionally, PWELL will be generated everywhere there is not PWELL blockGen or NWELL. A modified version of the simulation shown in figure 4.7c was created by

4.2.2.2). It was seen in the LFHV MAPS_FEI3 chip [7] that a spacing of $0\ \mu\text{m}$ between the edge of the PWELL and the edge of the NWELL yields a breakdown voltage of around 22 V. Here (and in reference [5]), in measurements of RD50-MPW1 the spacing between the pixel electrodes is $3\ \mu\text{m}$ and the breakdown voltage is around 60 V, suggesting a relationship between electrode spacing and breakdown voltage. In this section simulations are used to examine how increasing the spacing changes the breakdown voltage. However, increasing the electrode spacing does have a downside, if all other measurements in the pixel are kept the same, the size of the pixel must increase. If the size of the pixels increase, granularity decreases, decreasing spatial resolution of detected particles. Therefore the function of the pixel must be considered when choosing parameters for the design and trade-offs may need to be made.

Another property of pixels investigated here is the shape of the implanted well corners. Looking closely at figure 4.2b, it can be seen that all corners of the pixels are 90° . Within their Process Design Kits (PDKs), foundries can offer different ways to define implant shapes: along orthogonal lines to make 90° corners (square pixels), lines at 45° (octagonal pixels), and sometimes lines at any angle to make pixels with more complex corner shapes. When designing at the layout level in high voltage applications (such as SPADs) corner shapes become important, as sharp 90° corners can lead to regions of high electric field and therefore early breakdown, similar to Premature Edge Breakdown (PEB) seen in SPAD devices [11]. Presented here are the results of simulations investigating three corner types: square, or 90° ; chamfered or 45° ; and rounded.

4.2.2.1 Corner geometry

In this section 3D simulations will be used to study how the simulated breakdown voltage is affected by three-dimensional corner geometries. Something designers do is round the corners off to reduce high electric field [11]. Pixels can take many shapes, but are typically rectangular (width and height may vary) with one of three corner shapes, depending on the intended function. These are presented in figure 4.13: figure 4.13a depicts a square pixel, with 90° corners; 4.13b depicts an octagonal pixel (a square with chamfered corners), the pixel has the same dimensions but the corners have been cut at 45° angles, noting that eight larger angles (135°) remain where high electric field can still form; and 4.13c depicts a pixel with filleted (rounded) corners, where no sharp corners remain.

The difficulty in simulating these shapes in Sentaurus TCAD lies in Sentaurus Structure Editor. Fortunately, Sentaurus Structure Editor provides tools for chamfering and filleting corners of material regions, but these cannot be applied to ref/eval windows, which must be used for doping. Ref/eval window shapes must be de-

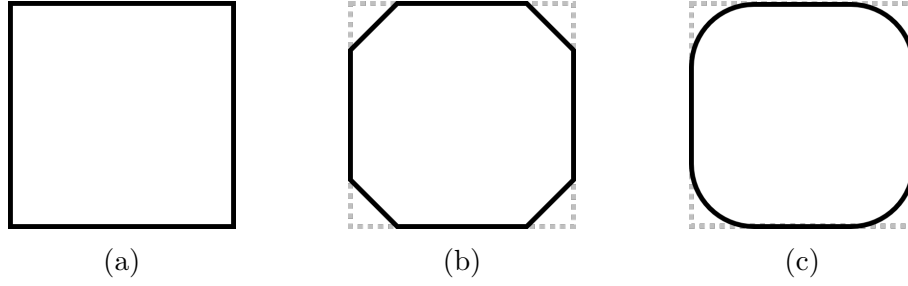


Figure 4.13: Diagram of top-down view of pixel corner shapes. (a) Square pixel with 90° corners. (b) Pixel with chamfered (or 45°) corners. (c) Pixel with rounded (filleted) corners.

defined in a GDS layout editor first and imported (for which software licenses can be expensive), or their geometries can be calculated by hand or using a script and coordinates imported (which could be time consuming). On top of this, in 3D (as opposed to 2D cross-sections), some doping regions take the shape of “rings” (such as the n^+ /NWELL/NISO stack ring for contacting the buried DNWELL), which also cannot be created easily in Sentaurus Structure Editor. In this work, this difficulty is overcome by defining and manipulating temporary 2D regions of material, and creating ref/eval windows using the Sentaurus Structure Editor `extract-refwindow` function, which defines a ref/eval window with the same shape as the specified geometric face. This allows simulations to be performed completely inside the Sentaurus framework, without any external programs or plugins. An example of this can be seen in figure 4.14 for a doping window with a ring shape.

Rings have an outer edge and an inner edge, therefore a 2D rectangle with the width and length of the outer edge of the ring was defined (figure 4.14a). The material of the rectangle is unimportant as it will be deleted at the end. The corners were then manipulated with the fillet or chamfer tool (any combination of any corner shape can be used and combined), depending on the desired shape (figure 4.14b). Another 2D rectangle with the width and length of the inner edge of the ring was defined above the plane of the first rectangle (figure 4.14c). The corners of this second rectangle were also manipulated with the fillet (or chamfer) tool (figure 4.14d). The second rectangle was translated down to the plane of the first rectangle with the overlap behaviour set to “New Replaces Old” (figure 4.14e). The second rectangle is then deleted and since overlap behaviour was set to “New Replaces Old”, the second rectangle was subtracted from the first rectangle, leaving a ring shape with the outer and inner corners rounded (figure 4.14f). The `extract-refwindow` function was used on the remaining ring shape (figure 4.14g) and then the remaining ring shape was deleted leaving just the ref/eval window. For ring shapes with 90° corners, steps b and d were skipped, and for non-ring shapes, steps c–f were skipped.

Then, the large cuboid of silicon was defined for the substrate with the surface on

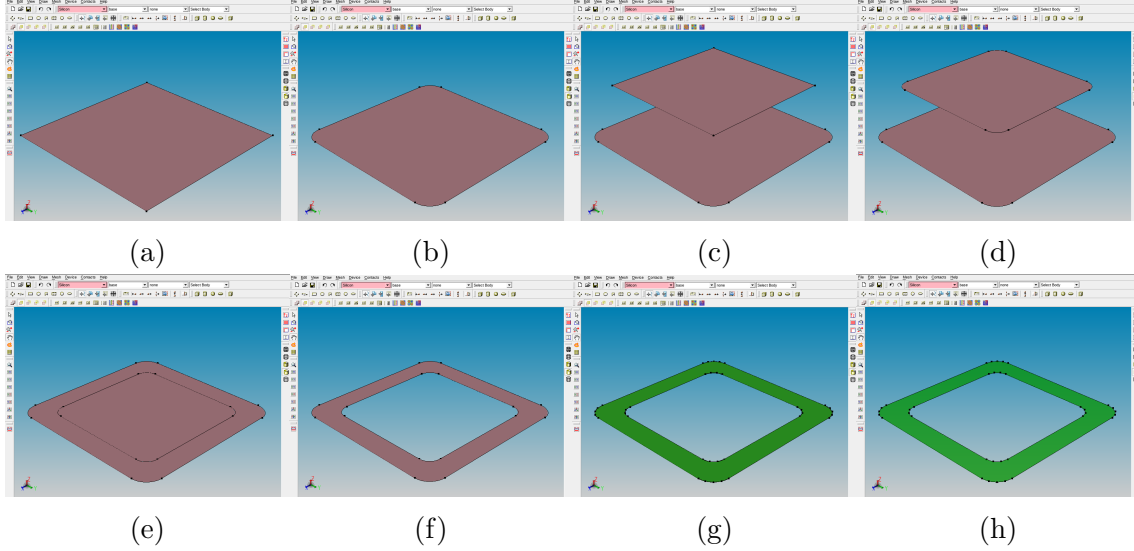


Figure 4.14: Method for creating ring-shaped ref/eval windows in Sentaurus Structure Editor (a) 2D rectangular region of material defined in 3D space. (b) Corners filleted. (c) Another rectangular region defined above the plane of the first. (d) Corners of the second rectangle filleted. (e) Second region translated down into the same plane as the first. (f) Second rectangle subtracted from the first. (g) Ref/eval window created from the new shape. (h) Material deleted leaving only the ref/eval window.

the same plane as the ref/eval windows. This can be seen in figure 4.15a for a pixel with 90° corners where the pink region is silicon, green is the ref/eval window of the PWELL ring, and the ref/eval window of the DNWELL is currently selected, shown highlighted in orange. The n^+ /NWELL/NISO stack required to bias the DNWELL is not shown here for simplicity. Figures 4.15b and 4.15c show pixels with chamfered corners and filleted corners respectively. Doping profiles for each well were applied to respective ref/eval windows. Since no STI is defined in these simulations, and therefore no openings in the substrate could be used to define contacts, two metal rings were defined in a similar way to the steps described in the previous paragraph and set as the contacts.

This structure would be too large to simulate in 3D however, therefore just one of the corners of the pixel was extracted from the structure. This can be seen in figure 4.16. Figure 4.16a displays a $50\mu\text{m} \times 50\mu\text{m}$ HV-CMOS pixel with chamfered corners, where the colour of the plot represents doping concentration. High n-type concentration is depicted in red and high p-type concentration in blue. The NISO and DNWELL layers are buried beneath the p-substrate. The structure extracted from this is highlighted in the dashed white box and shown in figure 4.16b. Three variants of the pixel corner are shown, square, chamfered, and rounded. From these cuts, the buried NISO and DNWELL layers can be seen. The region and size was chosen to reduce simulation time, but focussed on the area of importance

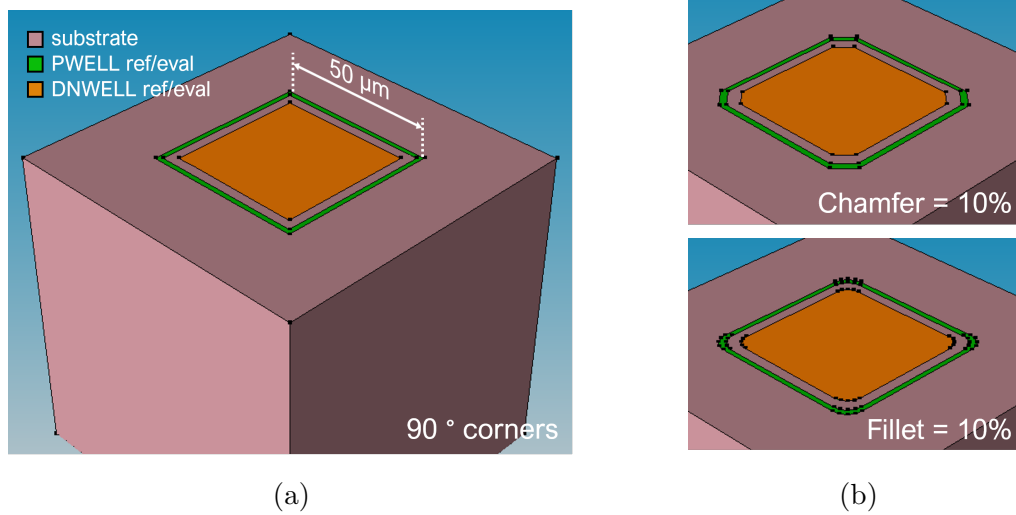


Figure 4.15: Screenshots of Sentaurus Structure Editor after two ref/eval windows have been created and a 3D region of silicon has been defined. Silicon substrate is shown in pink, ref/eval window of PWELL ring for biasing the substrate is shown in green and the ref/eval window of DNWELL is shown in orange (a) 90 ° corners. (b) (top) Chamfered corners. (bottom) Rounded corners.

identified in the simulations shown in figures 3.19, 3.20c, and 4.25b. The Sentaurus Structure Editor simulations here were performed before the method in the previous chapter was developed, using the doping profiles from [8]. For this reason and added simplicity, they also do not include SiO₂ STI as this would further increase the already significantly large simulation time.

A Sentaurus Device breakdown simulation was then performed on each structure and the results can be seen in figure 4.17. It should be noted that this Sentaurus Device simulation was also developed before the evaluation in chapter 3. Therefore the results are different from those simulations and the measurements in figure 4.1, but we can nevertheless learn something from the general trend they show. The physics models used are very similar to those in [8] except some have been removed to reduce simulation time and the model used for calculating the ionisation coefficients was Okuto-Crowell. Therefore we can compare the results of these simulations to the results of the 2D simulation in figure 3.21 that used the Okuto-Crowell model. The simulated breakdown voltage of the 2D structure overestimates the breakdown with respect to measurements ($V_{BD} = 81.35$ V). Simulating a 3D structure reduces the simulated breakdown voltage down to $V_{BD} = 73.62$ V due to high electric field at the corner (see figure 4.18), suggesting that the 3D corner would play a role in fabricated samples.

Figure 4.18 shows the simulated structures at $V_{sub} = -70$ V, where the colour of the plot represents electric field strength. Blue is low and red is high and the scale is the same in all figures. Figure 4.18a shows the 3D structure, similar to figure 4.16b.

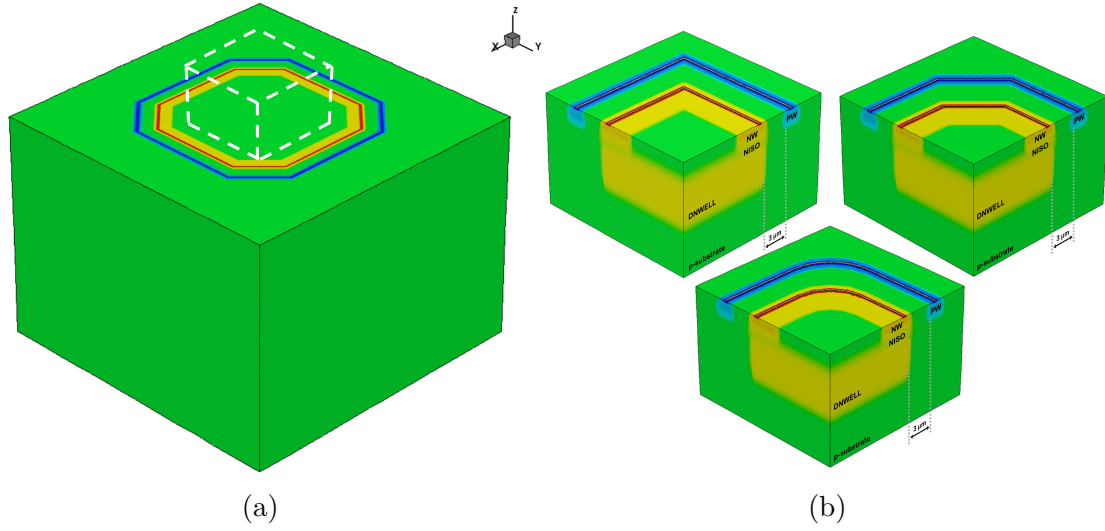


Figure 4.16: (a) 3D TCAD simulation of HV-CMOS pixel with chamfered corners. The colour of the image represents doping concentration from high n-type concentration in red to high p-type concentration in blue. The extracted structure in (b) is shown with a white dashed box. (b) Extracted structure from (a) also demonstrating variant corner shapes. The cut reveals the buried NISO and DNWELL layers.

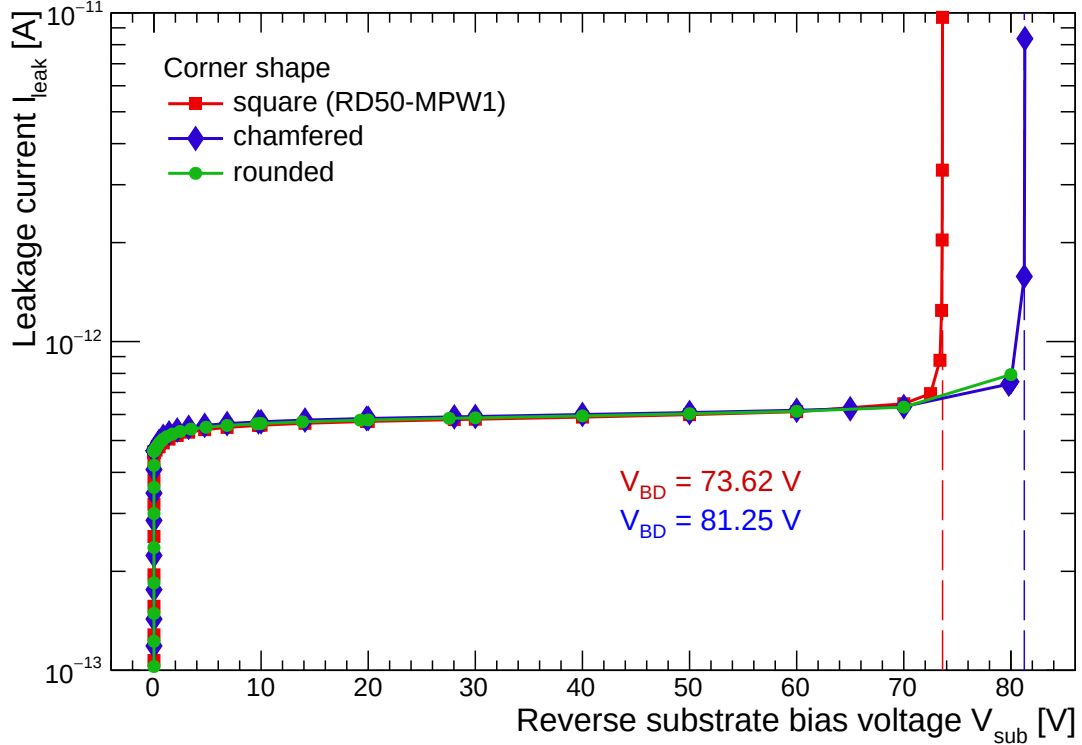


Figure 4.17: Simulated reverse I - V characteristic curves of three differently shaped 3D pixel corners. 90° corner shown with squares in red, chamfered corner shown with blue diamonds, and rounded corner shown with green circles.

The electric field is at its highest between the PWELL ring and NWELL/NISO stack ring. Figure 4.18b shows a top-down view of the structures from figure 4.18a to demonstrate the cut plane shown in figure 4.18c which shows the electric field at the sharpest points in all corners. It can be seen that the 90° corner exhibits the largest electric field, which is expected, and the electric field decreases as the corner angle decreases. Simulating a 3D chamfered corner brings the breakdown voltage back up to a similar value ($V_{BD} = 81.25\text{ V}$) as for 2D simulations suggesting the high electric field that would form due to the 90° corner has been suppressed. The simulation of the rounded corner terminated at $V_{sub} = -80\text{ V}$ due to memory issues after an estimated simulation time of 800 hours. However, it is still possible to infer that V_{BD} of the rounded pixel is larger than square pixel because at -80 V , the current is still low. I_{leak} of the rounded pixel is slightly larger than that of the chamfered pixel, but the breakdown should be more or less the same as the chamfered pixel. It cannot be determined from this simulation which corner, chamfered or rounded, is better for higher breakdown voltage. However, in contrast to what is seen in these simulations, it is seen in measurements that the breakdown voltage of fabricated RD50-MPW1 and RD50-MPW2 pixels with square and rounded corners (respectively), both with an electrode spacing of $3\text{ }\mu\text{m}$ should be approximately equal to -57 V (see results in figure 4.1 and in the next section). This suggests some other more important effect is dominating, possibly charge trapping in the region of high electric field. This would need to be simulated to confirm this hypothesis, possibly by minimising the substrate size and decreasing coarse meshing to reduce simulation time.

4.2.2.2 Electrode spacing

Another property of the pixel design that was investigated here to increase breakdown voltage was the spacing between the sensing diode electrodes. Figure 4.19a shows diagrams of the pixel cross-section, zoomed in to one of the junctions. From top to bottom, the spacing between the PWELL and NWELL that contain the diode electrodes is increased from $3\text{ }\mu\text{m}$ (in RD50-MPW1) to $4\text{ }\mu\text{m}$, $6\text{ }\mu\text{m}$, and $8\text{ }\mu\text{m}$. These are spacings that would be large enough to increase the breakdown voltage significantly, but not so large that the size of the pixel is greatly increased. For example with $3\text{ }\mu\text{m}$ spacing, pixels in RD50-MPW1 were $50\text{ }\mu\text{m} \times 50\text{ }\mu\text{m}$. Leaving all other parameters intact and increasing the only this spacing to $8\text{ }\mu\text{m}$ increases the pixel size by $10\text{ }\mu\text{m}$ ($5\text{ }\mu\text{m}$ on either side) to $60\text{ }\mu\text{m} \times 60\text{ }\mu\text{m}$.

Zoomed in images of the simulated structures are shown in figure 4.19b. The simulations are simply modified versions of the Sentaurus Structure Editor simulation shown in figure 3.11b. The ref/eval windows of the p+/PWELL implant stack have been laterally translated, along with the opening in the STI. Like the corresponding adjacent diagrams, the $3\text{ }\mu\text{m}$ spacing has been increased to $4\text{ }\mu\text{m}$, $6\text{ }\mu\text{m}$,

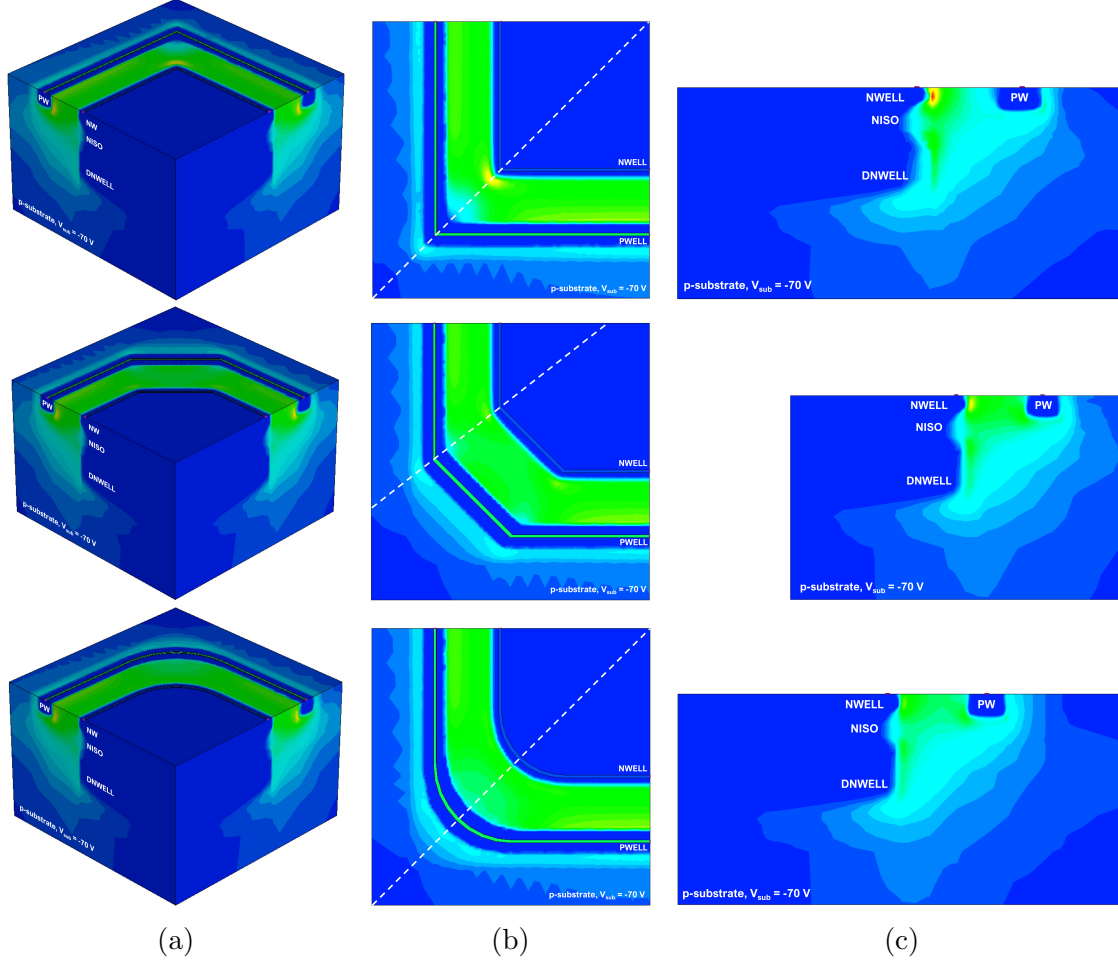


Figure 4.18: (a) 3D TCAD simulations of three differently shaped pixel corners where $V_{sub} = -70$ V. Colour of the plots represents electric field where blue is low red is high. From top to bottom the corner shapes are 90° , chamfered, and rounded. (b) Top-down view of the simulations in (a) demonstrating the cut position. (c) Cuts of simulations in (a).

and $8\ \mu\text{m}$, with all other parameters preserved. The customised transient Sentaurus Device simulation was run on the structures and the results are shown in figure 4.20. It can be seen that the breakdown voltage increases with an increase of electrode spacing. This confirms that the simulations have a tendency to overestimate the breakdown voltage when compared to measurements (see section 4.2.3).

4.2.3 I – V Measurements

Based on the results of these simulations, pixels in the 8×8 active matrix of the RD50-MPW2 submission were implemented with $8\ \mu\text{m}$ spacing between the diode electrodes, and rounded corners. This increased the pixel size to $60\ \mu\text{m} \times 60\ \mu\text{m}$, larger with respect to RD50-MPW1, but should also increase the breakdown voltage. PWELL blockGen was placed in between the NWELL and PWELL to ensure the spacing was retained. Measurements of the active matrix are not presented here,

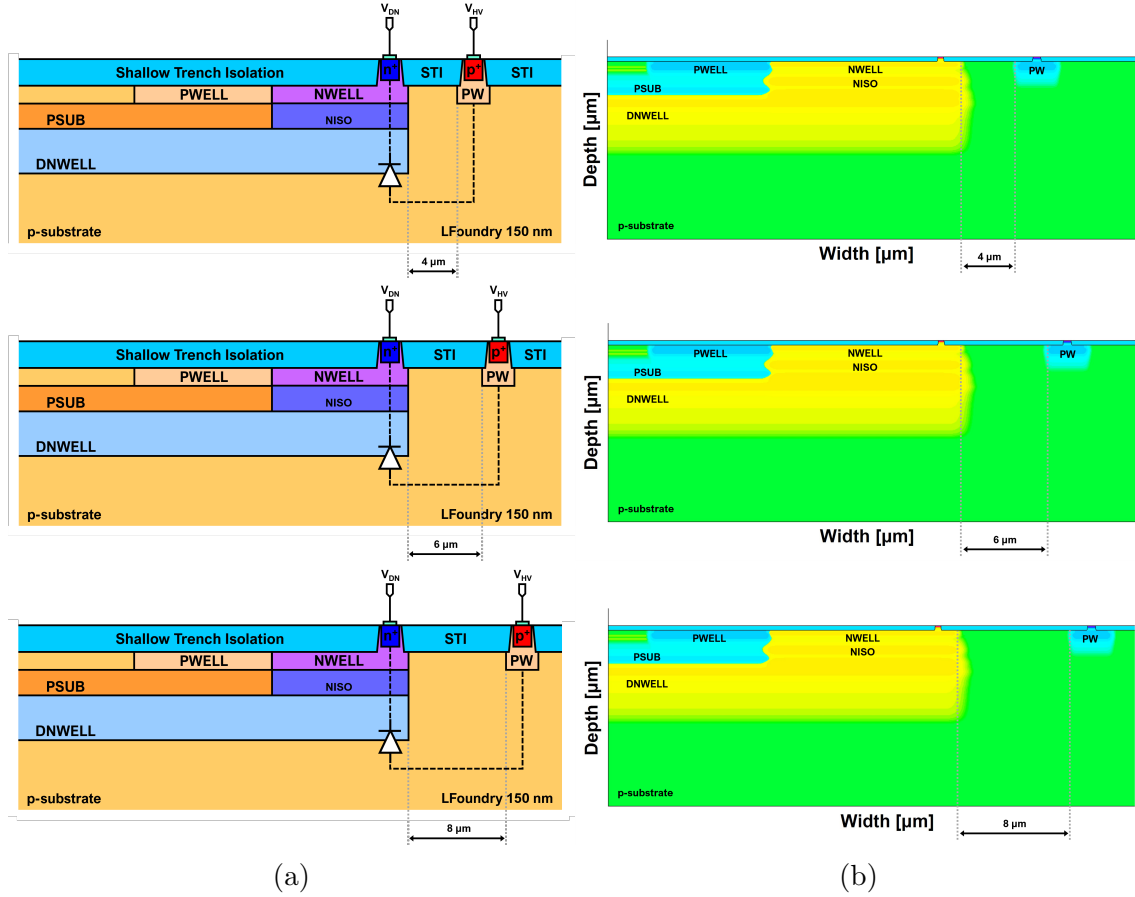


Figure 4.19: (a) Cross-section diagrams of different spacings between pixel diode electrodes. (b) Simulated cross-sections of different spacings between diode electrodes.

but a passive test structure made using the same pixel dimensions was included, seen at the bottom of the right edge of the floorplan. A zoomed in portion of the floorplan can be seen in figure 4.21a, and the test structure is highlighted in magenta at the bottom of figure 4.21b. It consists of a 3×3 matrix of passive, $60 \mu\text{m} \times 60 \mu\text{m}$ HV-CMOS pixels. There are two readout channels, one for the central pixel and one for the outer eight neighbouring pixels, very similar to the structure implemented into RD50-MPW1 described in the first half of this chapter. Above this are two almost identical structures, the only difference being the shape of the pixel corners, which are chamfered and squared, shown in the middle and the top of figure 4.21b, in green and blue respectively. And finally at the top of the floorplan is another 3×3 matrix of passive HV-CMOS pixels, this time with $50 \mu\text{m} \times 50 \mu\text{m}$ and rounded corners included to compare with RD50-MPW1 measurements.

Test structures in this submission are slightly different from test structures in RD50-MPW1 as they have no protection diodes. They have four pads: a substrate contact; a pad for the DNWELL of the central pixel; a pad for the DNWELLs of the outer neighbouring pixels that are connected together; and a pad for the p-type

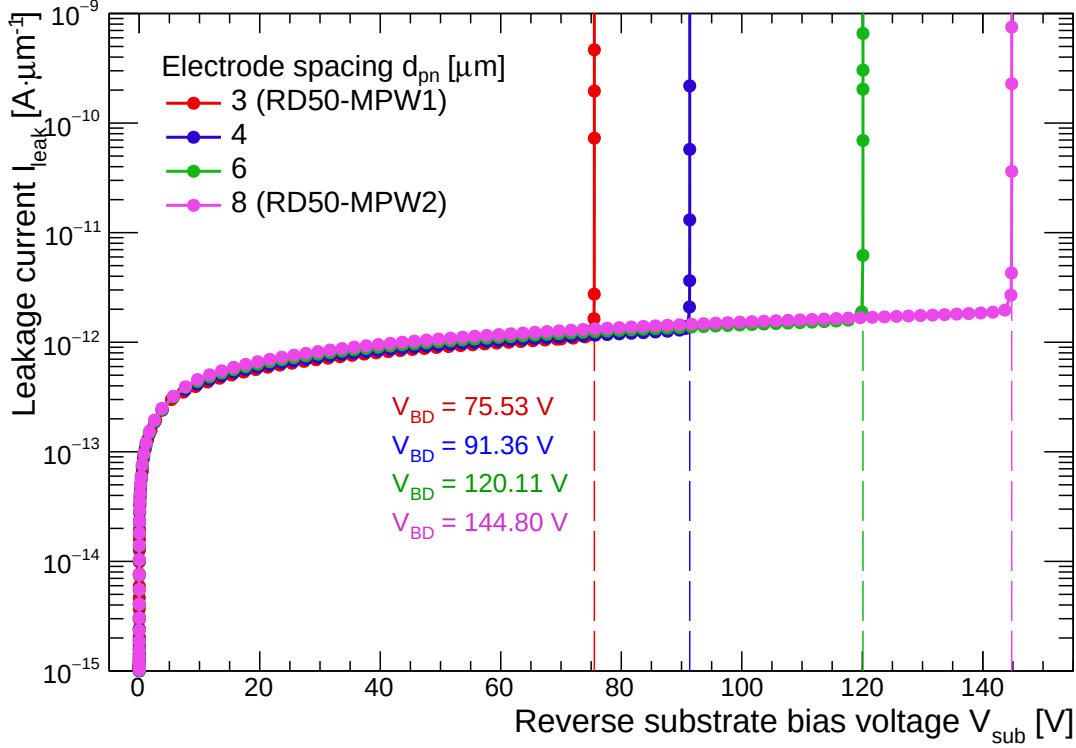


Figure 4.20: Simulated reverse I – V characteristic curves of pixels with increasing electrode spacings. Breakdown voltages are marked with vertical dashed lines.

wells of all pixels that have been shorted and are isolated from the substrate by the DNWELL. Samples were measured in the same setup as RD50-MPW1 samples except only three test probes and SMUs were used. Both the central DNWELL and the p-type wells of all pixels were biased to 0 V using separate SMUs, and the substrate was connected using the third. The substrate SMU was slowly ramped to high voltage using a ramp speed of 1 Vs^{-1} in 0.25 V steps, until the current measured by the SMU reached compliance current, which was set to $10 \mu\text{A}$.

I – V measurements of all four test structures from multiple samples with a range of substrate resistivities (500 – $1100 \Omega \cdot \text{cm}$, $1900 \Omega \cdot \text{cm}$, and $> 2000 \Omega \cdot \text{cm}$) are shown in figure 4.22 and results summarised in tables 4.1, 4.2, and 4.3. Breakdown voltages were extracted by calculating the ILD of each curve. Measurements show simulations presented here were successful in predicting the general trend in breakdown voltages of RD50-MPW2 samples and aided in producing detectors with leakage currents many of orders of magnitude lower than RD50-MPW1. There are not enough statistics to make any definite conclusions about sample-to-sample breakdown voltages, but starting with of $50 \mu\text{m} \times 50 \mu\text{m}$ pixels, breakdown voltages do not vary much with substrate resistivity. In addition, comparing them with the measured RD50-MPW1 sample (figure 4.1), the breakdown voltages are similar, despite simulations demonstrating that rounded corner pixels should have a higher breakdown

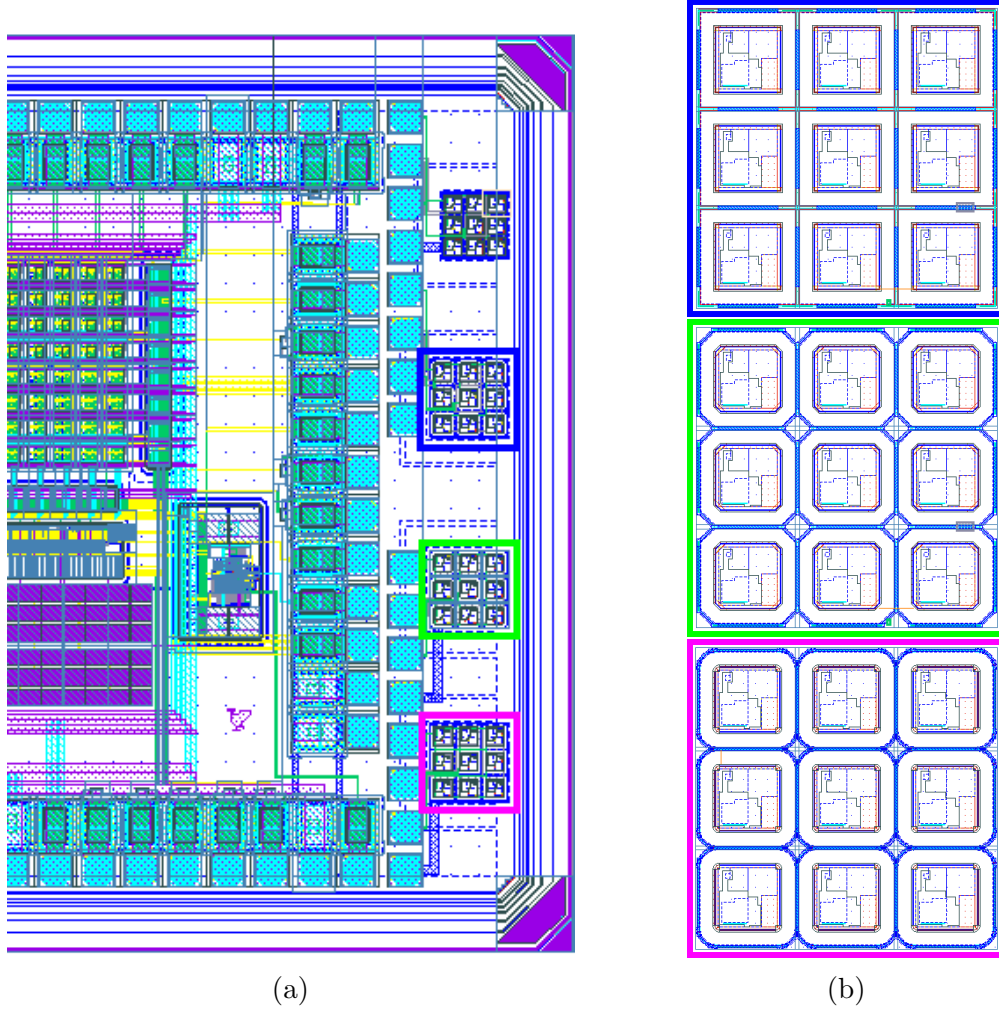


Figure 4.21: (a) Zoom of right side of RD50-MPW2 floorplan showing test structures implemented for e-TCT measurements. (b) Zoom of test structures showing corner shapes.

voltage. The reason for this is largely unknown but simulations do not account for charge trapping at the Si-SiO₂ interface which could be the biggest contribution. It is also possible that shapes defined with coordinates off-grid or edges with angles $0^\circ < \theta < 45^\circ$ or $45^\circ < \theta < 90^\circ$ such as the rounded corners here, have unpredictable effects on Optical Proximity Correction (OPC). The similar V_{BD} between $50\ \mu\text{m} \times 50\ \mu\text{m}$ RD50-MPW1 and RD50-MPW2 pixels but vastly different I_{leak} could suggest that the differing corner geometries are the cause. However, this is shown not to be the case with the measurements of the other test structure pixels on RD50-MPW2 which have different corner geometries.

For $60\ \mu\text{m} \times 60\ \mu\text{m}$ pixels, generally pixels with 90° corners have the lowest breakdown voltages, but only by around 1 V with respect to using chamfered or rounded corners. Again, this was less than was predicted by 3D simulations of $50\ \mu\text{m} \times 50\ \mu\text{m}$ cross-sections, but it is possible the wider pixel spacing of the measured $60\ \mu\text{m} \times 60\ \mu\text{m}$ pixels would lessen this effect. Pixels with rounded or chamfered

Table 4.1: Summary of I – V measurements of 500 – $1100 \Omega \cdot \text{cm}$ substrate resistivity RD50-MPW2 samples.

Wafer	$\rho [\Omega \cdot \text{cm}]$	Sample	$V_{\text{BD}} [\text{V}]$			
			$50 \mu\text{m}^2 \text{ (R)}$	$60 \mu\text{m}^2 \text{ (S)}$	$60 \mu\text{m}^2 \text{ (C)}$	$60 \mu\text{m}^2 \text{ (R)}$
W7	500–1100	1	55.50	128.75	130.25	128.00
		2	56.25	129.00	129.50	129.50
		3	56.00	128.50	130.50	129.75
		4	55.50	128.00	128.00	128.00
W8	500–1100	1	55.50	128.50	129.00	129.00
		2	55.75	128.75	129.75	128.25
		3	56.00	129.00	130.25	129.00
		4	55.25	127.75	127.50	127.25
		Mean	55.72	128.53	129.34	128.59
		Range	1.00	1.25	3.00	2.50

corners tend to have the highest average breakdown voltages across all resistivities but only by a small amount compared to square corners, which was predicted by the 3D simulations when the electric field at the corner is considered. Lower resistivity samples tend to have higher breakdown voltages but the benefits of using medium to higher resistivity come from the maximised size of the depletion region, which could outweigh the 3 V–4 V improvement in breakdown voltage by using lower resistivity. To summarise, pixels with wider spacing increase the breakdown voltage but also increase the pixel size, and must be balanced depending on requirements. Chamfered or rounded corners are recommended to increase breakdown voltage, but the simplicity of designing with chamfered corners outweighs the possible minute increase in breakdown voltage seen in rounded pixels. The fact that I_{leak} is approximately the same across all RD50-MPW2 pixel types shows that I_{leak} is independent of corner geometry. Logically, this demonstrates that the differing corner geometries between RD50-MPW1 and RD50-MPW2 $50 \mu\text{m} \times 50 \mu\text{m}$ pixels is not the cause of I_{leak} , and the fix was the isolation of silicide in active areas in RD50-MPW2.

4.2.4 Simulation of I – V characteristics

Finally, in this section simulations of a $50 \mu\text{m} \times 50 \mu\text{m}$ passive pixel from the RD50-MPW2 test structures will be described and compared with the measurement in figure 4.1. The simulation is produced using the method described in chapter 3, and demonstrates how other structures (other pixels in this case) can be generated very easily. A $50 \mu\text{m} \times 50 \mu\text{m}$ pixel was used rather than a $60 \mu\text{m} \times 60 \mu\text{m}$ pixel in order to compare with measured results from both RD50-MPW1 and RD50-MPW2. It will be shown that when a larger simulated substrate region is used and the other pixels in the matrix are accounted for, simulations are consistent with measurements. In

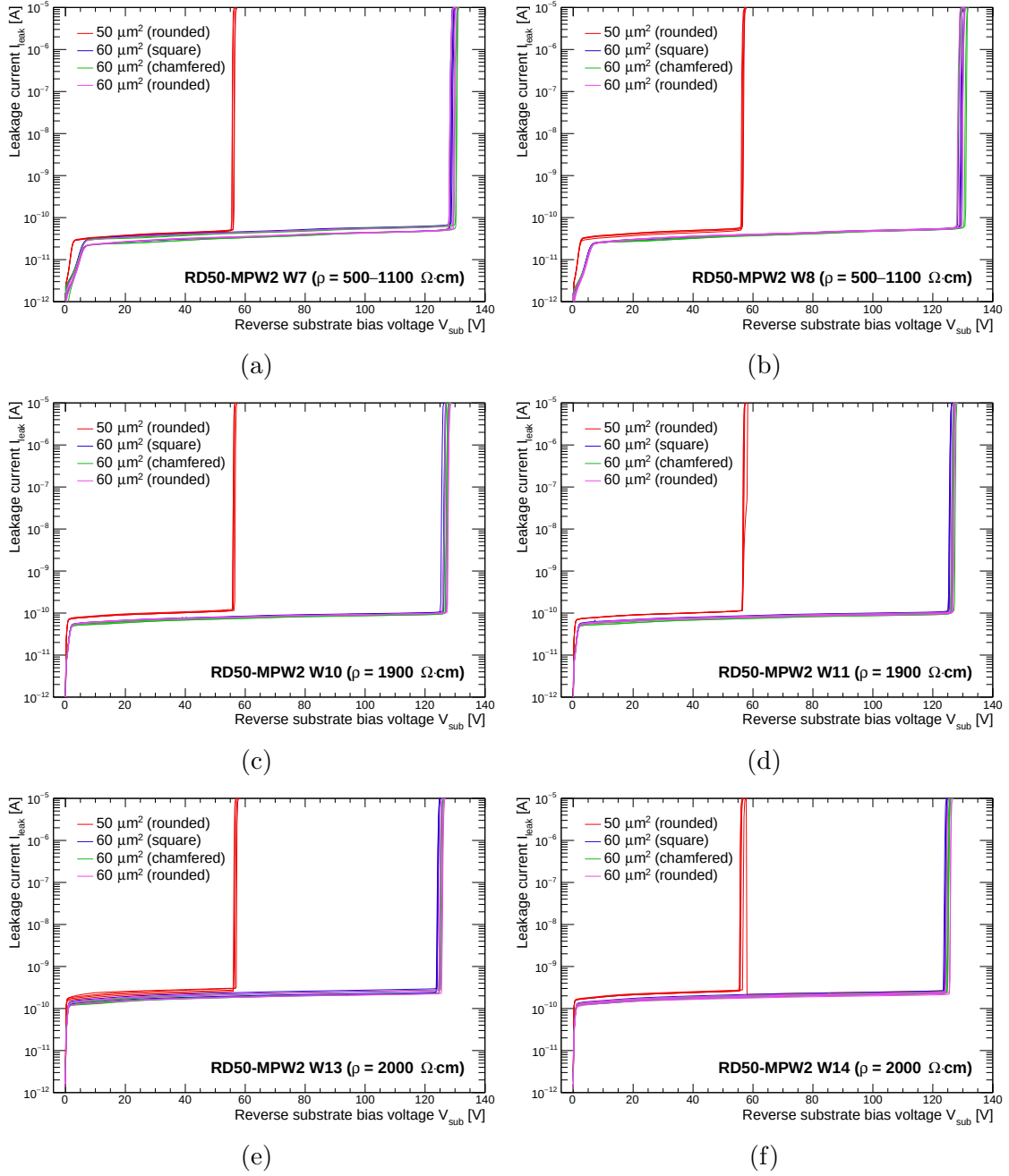


Figure 4.22: Results of I - V measurements of central pixels of all four test structures from RD50-MPW2 samples. (a) One sample from standard resistivity wafer 6. (b) Four samples from wafer 7 ($500\text{--}1100\ \Omega \cdot \text{cm}$). (c) Four samples from wafer 8 ($500\text{--}1100\ \Omega \cdot \text{cm}$). (d) Four samples from wafer 10 ($1900\ \Omega \cdot \text{cm}$). (e) Four samples from wafer 11 ($1900\ \Omega \cdot \text{cm}$). (f) Four samples from wafer 13 ($> 2000\ \Omega \cdot \text{cm}$). (g) Four samples from wafer 14 ($> 2000\ \Omega \cdot \text{cm}$).

Table 4.2: Summary of I - V measurements of $1900 \Omega \cdot \text{cm}$ substrate resistivity RD50-MPW2 samples.

Wafer	ρ [$\Omega \cdot \text{cm}$]	Sample	V_{BD} [V]			
			$50 \mu\text{m}^2$ (R)	$60 \mu\text{m}^2$ (S)	$60 \mu\text{m}^2$ (C)	$60 \mu\text{m}^2$ (R)
W10	1900	1	56.50	126.00	127.00	127.50
		2	55.75	126.00	127.00	127.50
		3	55.75	126.50	127.25	127.50
		4	56.25	125.25	126.25	126.50
W11	1900	1	57.50	124.75	125.75	126.25
		2	56.00	125.00	125.75	126.25
		3	56.00	125.00	126.00	125.50
		4	56.50	125.75	126.75	126.50
		Mean	56.28	125.53	126.47	126.69
		Range	1.75	1.75	1.50	2.00

Table 4.3: Summary of I - V measurements of $> 2000 \Omega \cdot \text{cm}$ substrate resistivity RD50-MPW2 samples.

Wafer	ρ [$\Omega \cdot \text{cm}$]	Sample	V_{BD} [V]			
			$50 \mu\text{m}^2$ (R)	$60 \mu\text{m}^2$ (S)	$60 \mu\text{m}^2$ (C)	$60 \mu\text{m}^2$ (R)
W13	>2000	1	56.50	124.00	125.00	125.50
		2	56.25	124.00	125.00	125.75
		3	57.00	124.25	125.00	124.75
		4	56.00	123.75	125.75	124.75
W14	>2000	1	56.50	124.00	125.00	125.75
		2	55.50	124.00	125.00	125.75
		3	55.50	124.00	125.00	124.50
		4	55.75	123.75	124.75	124.25
		Mean	56.13	123.97	125.06	125.13
		Range	1.50	0.50	1.00	1.50

reality, fabricated pixels are three-dimensional objects and exact simulations of such structures require simulation in three dimensions, which are time-consuming and difficult to perform. To circumvent this, Sentaurus Device includes an area factor (**AreaFactor**) to account for the remaining dimension which can be used in 2D simulations. This is simply a multiplication factor for currents and charges [12]. A diagram of figure 3.1b with the third dimension expanded with an **AreaFactor** is depicted in figure 4.23a. The cross-section is simply stretched in the remaining dimension, demonstrating that the **AreaFactor** does not reproduce the structure exactly as would be seen in a fabricated device. This scenario is depicted in figure 4.23b. Wells other than p+ and n+ are hidden in this image, buried beneath the STI in the p-substrate. This can be seen more clearly later in section 4.2.2.1.

Therefore the **AreaFactor** can only be used for a good approximation. However, even if the third dimension of the pixel in previous simulations is taken into

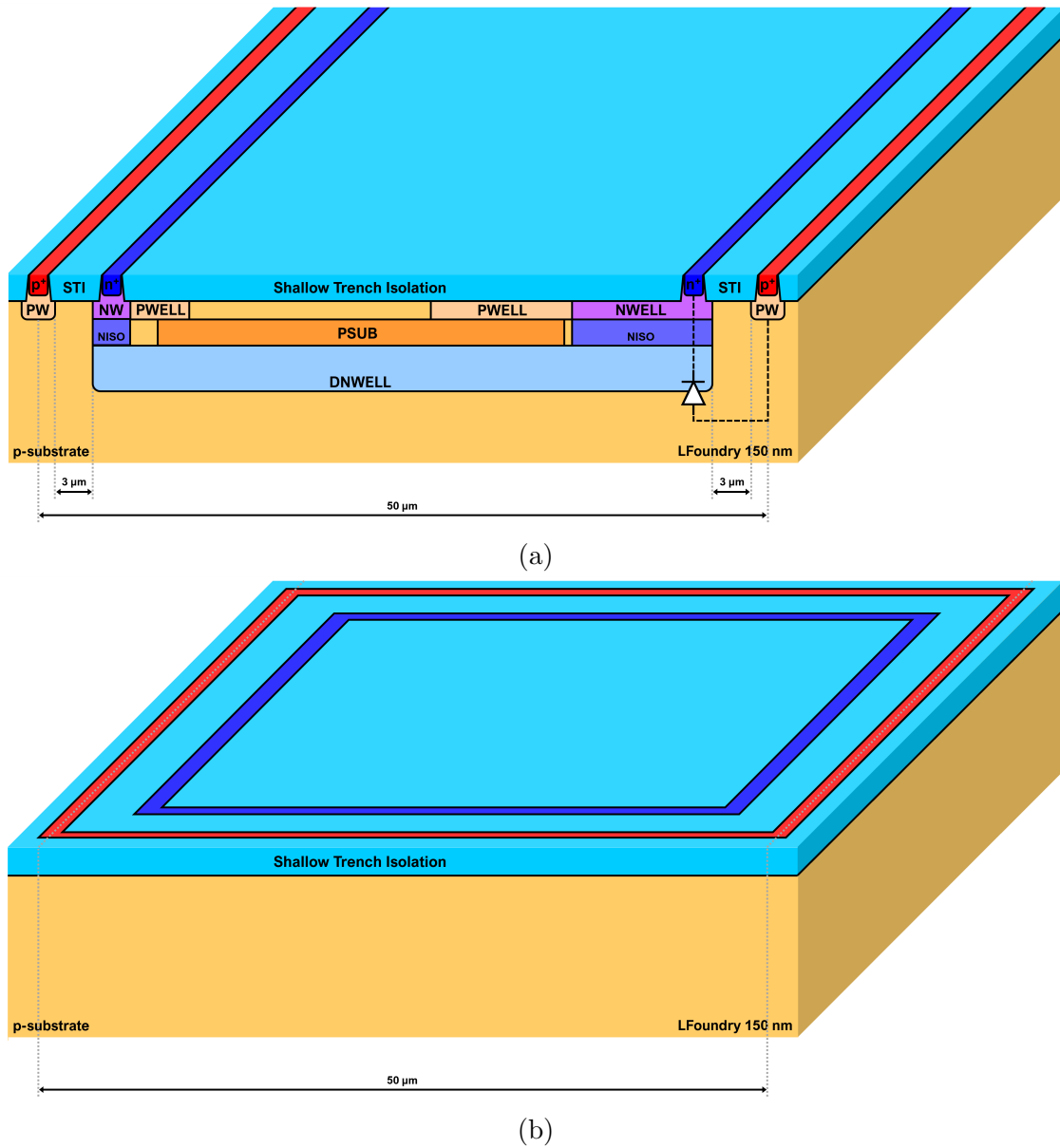
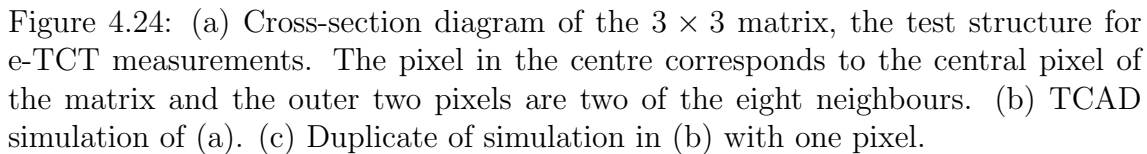


Figure 4.23: (a) Diagram of the pixel cross-section expanded in the third dimension with a Sentaurus Device **AreaFactor**. (b) Diagram of fabricated pixel in three dimensions. The pixel cross-section is hidden in this image by the p-substrate, buried under the STI.

consideration by multiplying the pixel current by the depth of the pixel, the simulated current is still lower than that of the measurements. This could be because the three dimensional pixel is not accurately represented. But, more likely the reason for the discrepancy between measurements and simulations is that although the central pixel is isolated from the neighbouring eight pixels, it is still part of a system that shares a common substrate. Therefore, the true cross-section of the test structure that includes the central pixel cross-section described in the previous sections actually consists of three pixels. This is depicted in figure 4.24a. With an **AreaFactor** this will represent the fabricated test structure better, but it should be noted that this still does not account for the remaining six pixels. In the fabricated device, the outer eight pixels are connected in parallel, represented in the diagram with the same label $V_{\text{neighbours}}$. The central pixel is isolated represented with the label V_{central} . The measurements will be discussed in more details in the next section, but due to the limited number of probes available with the equipment, the neighbouring pixels were left floating in measurements and were not grounded.

The simulated cross-section can be seen in figure 4.24b. This is identical to the simulation shown in figure 3.11b, except the size of the substrate region has been extended laterally and two pixels were added, including the p-type wells for the substrate contacts on the outer edges. This was achieved by replicating all ref/eval windows and spatially transforming them horizontally by the width of the pixel ($\pm W_{\text{pixel}}$), and applying the appropriate doping definitions. STI regions also needed to be added to account for the new openings in the surface of the substrate containing p+ and n+ wells. All substrate contacts were labelled with “ V_{HV} ”, to ensure all p-type wells for substrate contacts are biased to the same voltage, reflecting the fabricated design. Again like the fabricated design, the central pixel n-type wells were given the label “ V_{central} ” and new contacts were defined for the two outer pixels, which were both given the same label “ $V_{\text{neighbours}}$ ” to reflect the fact that the central and eight neighbouring pixels have separate readout channels. The same customised Sentaurus Device simulation was performed on the structure, with $Q_{\text{it}} = 0 \text{ cm}^{-2}$ and as mentioned before, the outer neighbouring pixels were left floating to mirror the setup in the measurements.

The results can be seen in figure 4.25a. By introducing more pixels into the shared substrate, the leakage current increases, which is expected for connected pixels. The leakage current should increase proportionally with the number of pixels. However, this is not the case in this structure, since the outer pixels are floating, but the pixels are close together and share a depletion region, “collecting” leaked charge carriers from the neighbouring pixels seen as an orange colour between the pixels in figure 4.25b. The shared depletion region can be seen in both figures 4.25b and 4.25c bounded by solid white lines. The depletion region underneath the central



pixel is deeper because it is the only biased pixel. The breakdown voltage has also decreased, most likely due to threshold electric field being reached early due to contributions from the other pixels. This can be seen in 4.25c. Two regions of high electric field are depicted in red outside the central pixel n-type wells like previous simulations. This time there are contributions from other regions of lower electric field outside the p+/PWELL substrate contact stacks shown in a green colour from the neighbouring pixels. This becomes clearer when looking back at figures 3.19a and 3.19b. There are regions of lower electric field (in green) outside the p+/PWELL substrate contact stacks. When the pixel is duplicated and transformed, the red region from the central pixel and green region from the neighbouring pixel combine.

As mentioned before, this 2D structure must be multiplied by an **AreaFactor** to compare with measurements. But this will not be accurate as demonstrated in figure 4.23a. Multiplying the 2D simulation by the remaining dimension of the pixel, its length L_{pixel} creates a larger, rectangular DNWELL, which seems to be the main contribution to the leakage current. A more accurate thing to do would be to multiply by the length of the DNWELL L_{DNW} , to ensure a square shape. However for the simulation of the three pixels, this still does not include contributions from the other eight pixels. A simple solution would be to multiply the simulation by $3L_{\text{DNW}}$, but that assumes three pixels connected and six floating, due to the nature of the **AreaFactor**, which is not the case in the measured structure. Therefore the simulation was run again with the wide substrate and just the central pixel, to isolate its contribution. The simulated structure is shown in figure 4.24c and the results are shown in figure 4.25a with green hollow circles. The difference between the simulations with one pixel and difference substrate widths is minimal, demonstrating that the size of the substrate region has little effect on results.

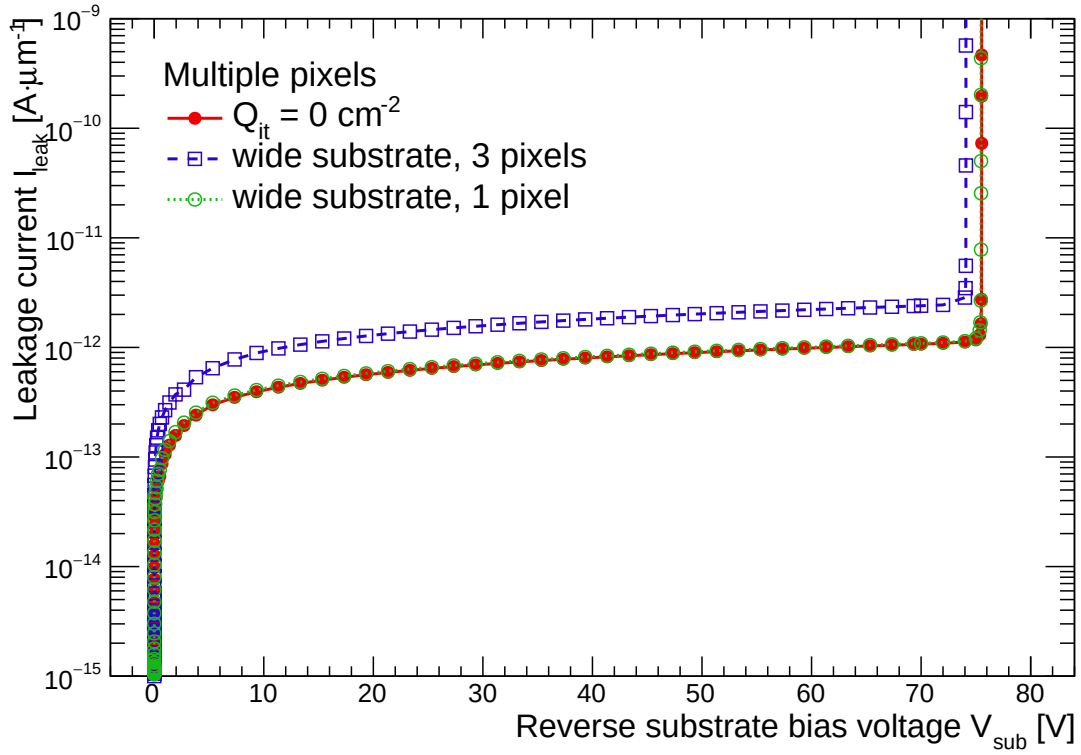
Finally, to simulate the measured current $I_{\text{simulated}}$ of the central pixel, first the current of one single neighbour pixel was computed. This was done by subtracting the current of the lone central pixel I_{central} from the current of the simulation of three pixels I_{triplet} , and dividing by two.

$$I_{\text{neighbour}} = \frac{I_{\text{triplet}} - I_{\text{central}}}{2} \quad (4.1)$$

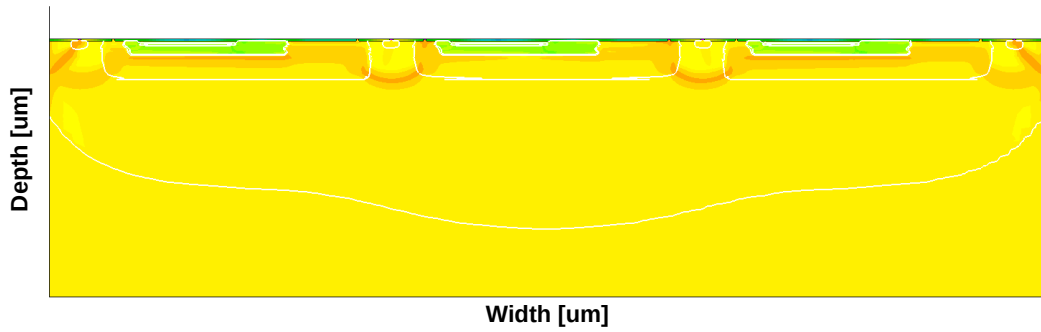
This is multiplied by the number of neighbouring pixels and summed.

$$I_{\text{simulated}} = 8I_{\text{neighbour}} + I_{\text{central}} \quad (4.2)$$

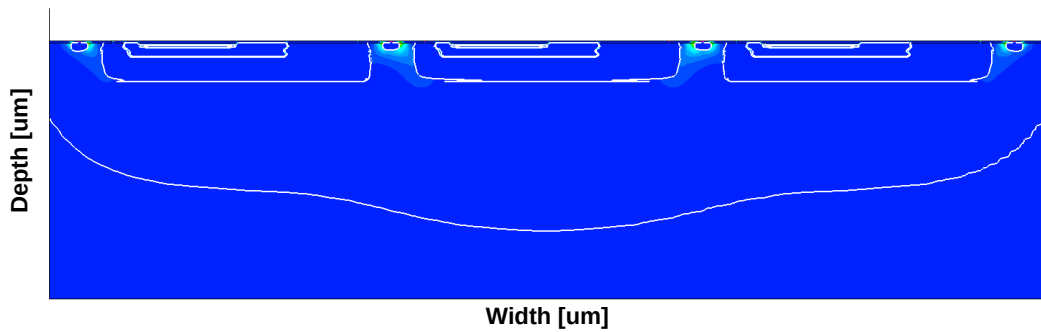
The results with $Q_{\text{it, f}} = 6.5 \cdot 10^{11} \text{ cm}^{-2}$ are displayed in figure 4.26. The comparison with measurements is very good.



(a)



(b)



(c)

Figure 4.25: (a) I – V simulations of multiple pixels. (b) Snapshot of current density simulation demonstrating shared depletion region and leakage current from outer floating pixels collected by biased central pixel. (c) Snapshot of electric field. High electric field can only be seen either side of the central biased pixel as the neighbour pixels are floating.

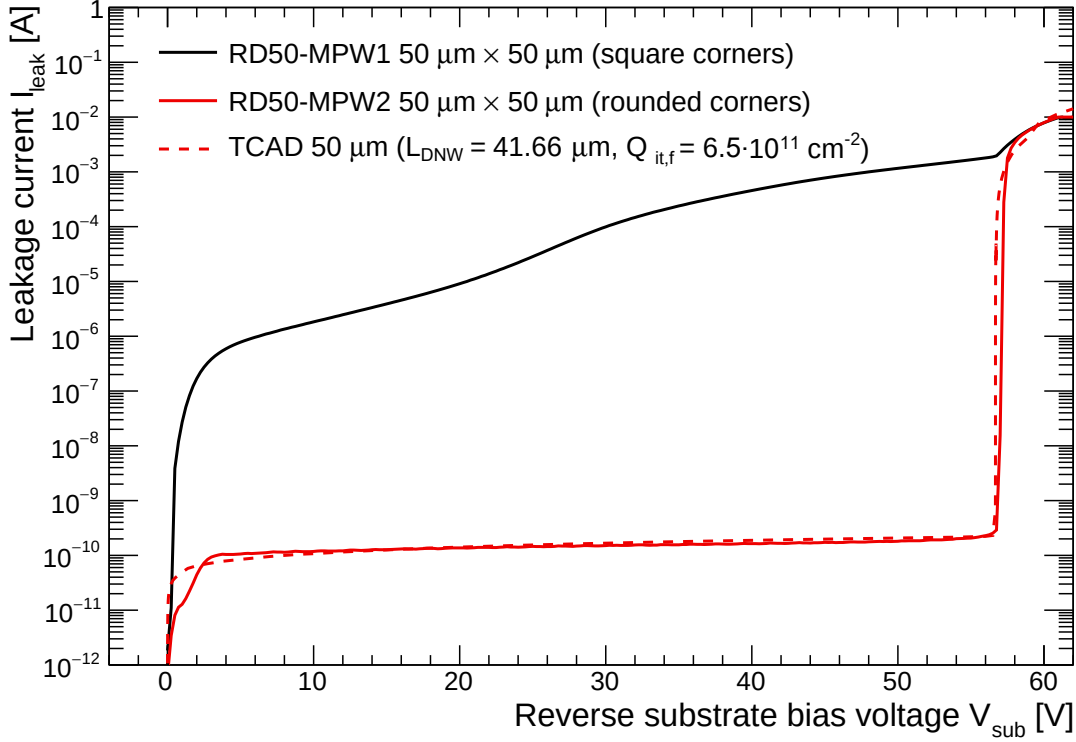


Figure 4.26: Measurements of reverse I - V characteristic curves of single, $50\,\mu\text{m} \times 50\,\mu\text{m}$ pixels from the RD50-MPW1 (black) and RD50-MPW2 (red) prototypes performed at room temperature. The results of TCAD simulations is shown with a red dashed line, performed at 300 K.

4.2.5 Summary

The investigations into RD50-MPW1 with TCAD simulations presented in this thesis aided in the development of a new prototype HV-CMOS detector within the RD50 collaboration known as RD50-MPW2. One of the general aims of the RD50-MPW2 submission, and a main aim of this thesis, was to improve detector parameters with respect to RD50-MPW1 specifically, reducing the sensor leakage current, and increasing pixel breakdown voltages. An improvement in either of these parameters would result in an improvement of radiation tolerance with respect to RD50-MPW1.

TCAD simulations were used to identify the source of the unusually high I_{leak} in RD50-MPW1 devices. The simulations shown were able to account for one order of magnitude of the observed leakage current. TCAD simulations were also used to investigate changes to the design that would lower I_{leak} back down to a reasonable level. These changes were implemented into the new prototype which was fabricated, and changes were verified to be successful with I - V measurements. The measured leakage current of test structure pixels in RD50-MPW2 was many orders of magnitude lower than measurements of equivalent pixels in RD50-MPW1.

TCAD simulations were also used to identify techniques to increase the pixel

breakdown voltage with respect to RD50-MPW1. Simulations of different pixel diode electrode spacings demonstrated that breakdown voltage can be increased at the cost of increased pixel area. 3D Simulations of different pixel corner geometries also demonstrated that breakdown voltage can be increased by chamfering or rounding square corners. Test structures were implemented into RD50-MPW2 to verify these simulations and I – V measurements confirmed the general trend.

Finally, the TCAD simulation method presented in chapter 3 was used to replicate the measured reverse I – V characteristics of RD50-MPW2 pixels. The incredible matching between measurements and simulations confirms the accuracy of the simulation method, and demonstrates that it should be possible to use the technique to predict the behaviour of future structures developed in the LFoundry 150 nm technology accurately.

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Chapter 5

Studies of backside biased sensors

5.1 Introduction

5.1.1 New prototype detector UKRI-MPW0

In this chapter the development of a new prototype HV-CMOS pixel detector, UKRI-MPW0 is presented which was developed under the UK Research and Innovation (UKRI) programme. The main aim of this study is to dramatically increase the breakdown voltage of monolithic HV-CMOS detectors in order to improve their radiation tolerance. The ultimate goal is that they could one day replace current hybrid detectors and be used in silicon tracking layers of future experiments like the HL-LHC or the FCC, where the requirements for radiation tolerance are very high.

During development, detectors can go through many iterations (the MuPix series of chips for example, are on their tenth iteration). The main aim of this ‘zeroth’ submission was to demonstrate that the breakdown voltage of HV-CMOS detectors can be increased significantly by adopting a structure similar to the design of planar sensors in hybrid detectors. This involves processing both the topside and backside of the wafer. The benefit with respect to planar sensors is that HV-CMOS detectors can be fully monolithic, and have no need to be hybridised (i.e., bonded to a readout chip). They can therefore be more cost-effective as they require less complicated assembly, and detector material can be minimised which reduces multiple scattering.

UKRI-MPW0 was designed in the LFoundry 150 nm technology and submitted in the November 2020 MPW run. An image of the submission can be seen in figure 5.1a. The device consists of two large matrices which have completely unique pads and can be operated entirely independently. The second matrix is identical to the first matrix, except some transistors have been replaced with Enclosed Layout Transistors (ELTs), in order to test their radiation tolerance. In addition, a range of test structures have been included at the top and bottom. Test structures at the top include 3×3 matrices of pixels, with sizes ranging from $40 \mu\text{m} \times 40 \mu\text{m}$ to

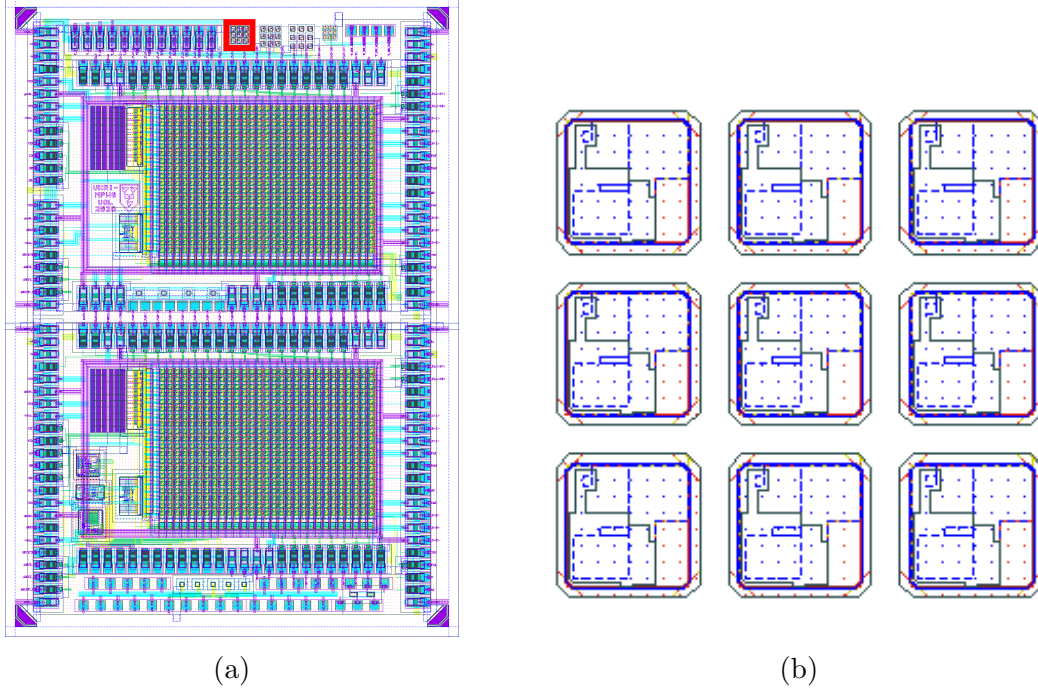


Figure 5.1: (a) Image of the UKRI-MPW0 submission. A test structure included for e-TCT measurements is highlighted in red at the top. (b) Test structure consisting of a 3×3 matrix of $50 \mu\text{m} \times 50 \mu\text{m}$ pixels. There is no p-type implant grid between pixels.

$70 \mu\text{m} \times 70 \mu\text{m}$, that have been included for e-TCT measurements. A test structure of $50 \mu\text{m} \times 50 \mu\text{m}$ pixels is shown in figure 5.1b.

5.1.2 Structure of the device

The structure of UKRI-MPW0 is modelled on that of n-in-n planar silicon sensors currently used in the ATLAS and CMS experiments at the LHC (shown in figure 2.18), which will be summarised here. The main aspect of sensors such as these is that n-type pixels are implemented on the topside of an n-type wafer and a p-type junction to deplete the substrate, and p-type guard ring structures are implemented on the backside. This enables very high substrate bias voltages (no breakdown below 500 V) as high doping concentration regions at different potentials are separated by the 200–300 μm thick substrate. It is important to point out that as both the substrate and pixels are n-type, pixels are isolated from each other using a low-concentration p-spray implantation to avoid electron accumulation layers at the Si-SiO₂ interface between pixels. This must be low concentration to avoid high electric field leading to avalanche multiplication of carriers and early breakdown. This isolation is also important even after n-type substrate type inversion due to irradiation, as inversion layers can form between pixels due to the positive charges in the SiO₂.

The prototype HV-CMOS detector presented here follows a very similar design to those planar sensors, except that the substrate is p-type and no patterning was available for the backside implants to implement a guard ring structure on the backside. The topside of the wafer in UKRI-MPW0 was processed using the LFoundry 150 nm HV-CMOS technology node however, any and all p-type implantations are isolated from the p-type substrate by the buried n-type implants. The backside of the wafer was processed separately by Ion Beam Services (IBS), which for this prototype, simply included a non-patterned p+ implantation, annealing and metallisation steps. The availability of patterned, backside implantation could be investigated in the future to form a separate high-voltage contact, and concentric, p-type guard rings on the backside to drop the potential from the high-voltage contact to the conductive edge, like those in hybrids presented in chapter 2. The result is a detector like a planar sensor, where high-concentration p-type and n-type implants are separated by the thickness of the substrate, but full CMOS readout electronics have been implemented inside the n-type pixels. A diagram is shown in figure 5.2a. Measured breakdown voltages of fabricated, non-irradiated samples exceed 600 V, which will be presented at the end of this chapter. For this prototype, no pixel-to-pixel isolation other than the natural p-n junction formed with the substrate has been implemented due to the lack of a p-spray implant in the LFoundry technology. A diagram of the possible next iteration of the prototype is shown in figure 5.2b. At the time of writing, possible p-spray techniques are being investigated including TCAD structure simulations of the best final doping concentrations and depths, TCAD process simulations of required implant energies and doses, and searches for potential vendors.

5.1.3 Discussion

The alternative pixel-to-pixel isolation technique known as p-stop, is a higher concentration p-type implant which can be implemented in LFoundry technology in the form of the PWELL implant. In fact, backside processed monolithic HV-CMOS detectors with large breakdown voltages have already been achieved by another group [1] using p-stop in the Monopix chips. Before irradiation, measurements of devices show breakdown voltages around 260 V. For this reason, p-stop was avoided in UKRI-MPW0 as it is believed to be the cause of early breakdown due to the formation of high electric field between the n-type pixels and the relatively high concentration p-stop. This phenomenon was observed in the simulations of RD50-MPW2 presented in the previous chapter.

In RD50-MPW2, PWELL was used (in conjunction with a high concentration p+ implant) to isolate pixels like p-stop. However, these implants were also used to bias

the substrate and were therefore at a fixed potential, but the principle is the same. The presence of negative acceptor ions that form p-type implants in close proximity to the positive donor ions in n-type implants cause regions of high electric field to form between them. It was demonstrated in simulations in the previous chapter that this could be mitigated somewhat by increasing the spacing between the implants. However, this increases the size of pixels, which is undesirable if accurate track reconstruction is a requirement. It should be noted that another method used to reduce the electric field between opposite type implants that was mentioned in chapter 2 that involves distributing the electric field using polysilicon field plates and overhanging metal layers. Based on the other literature given in the chapter, the Monopix designers likely used this technique. The combination of backside biasing and the use of field plates increases the breakdown voltage with respect to RD50-MPW2 but excluding the relatively high concentration p-type implants entirely allows for even higher breakdown voltages as is the case with UKRI-MPW0. This principle will be explored in section 5.2.

In section 5.3, measurements of two other backside biased HV-CMOS detectors H35DEMO [2] and MuPix8/ATLASPix1 [3, 4], developed in other technologies will be presented. The work follows on from that presented in references [5] and [6]. Both detector types were fabricated using single-sided HV-CMOS processes and were designed with p-type wells between pixel n-type implants for isolation and biasing the substrate. For the study presented here, samples were backside processed at IBS to allow backside biasing and top-side p-type wells were left floating during measurements. The Edge Transient Current Technique (e-TCT) measurements presented not only provide inputs for Charge Collection Efficiency (CCE) measurements such as the studies presented in references [7–9], but also demonstrate that the backside processing from IBS is a viable option for future detectors. Samples presented in this study represent a range of substrate resistivities, the high resistivity H35DEMO, and two types of MuPix8/ATLASPix1 samples, low and medium resistivity. Samples have also been irradiated to fluences up to $2 \cdot 10^{16} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$, the level expected in the inner layers of experiments at the HL-LHC. This thesis provides more details about the H35DEMO measurements published in reference [10].

This will be followed in section 5.4 by the simulations used to investigate the backside processing technique used on H35DEMO and MuPix8/ATLASPix1 samples, and investigate a new backside processing technique. Section 5.5 includes the simulations used in the design of the top-side elements of UKRI-MPW0 such as guard rings and filling structures. Finally section 5.6 presents preliminary I – V measurements of UKRI-MPW0 samples confirming the breakdown voltage.

5.2 Simulations of the concept

The design is based on the principle demonstrated by simulations and subsequent measurements of RD50-MPW2: that the distance between p-type and n-type wells that form the pixel electrodes is one important factor in determining the reverse breakdown voltage. For biased PWELLS, $V_{BD} \approx -57\text{ V}$ for pixels that have an electrode spacing of $3\text{ }\mu\text{m}$ ($50\text{ }\mu\text{m} \times 50\text{ }\mu\text{m}$ pixels), and $V_{BD} \approx -127\text{ V}$ for pixels that have an electrode spacing of $8\text{ }\mu\text{m}$ ($60\text{ }\mu\text{m} \times 60\text{ }\mu\text{m}$ pixels). However, if this distance is increased any further to increase V_{BD} , the area of pixels increases without recovering any additional area for readout electronics. If the p-type wells forming topside substrate contacts are removed entirely, and the substrate is biased using only the backside contact, the effective spacing between diode electrodes increases from $3\text{ }\mu\text{m}$ or $8\text{ }\mu\text{m}$, to the thickness of the chip ($\approx 300\text{ }\mu\text{m}$) and V_{BD} can be increased while maintaining small pixel sizes.

To demonstrate this principle, three scenarios are presented, and displayed in figure 5.3. The first scenario shown in figure 5.3a is a typical pixel, like those in RD50-MPW1 and RD50-MPW2 presented in chapter 4. TCAD simulations of this type of pixel presented in chapter 3 show that when the sensing diode is reverse biased, reverse breakdown occurs in the region between the electrodes, labelled V_{HV} and V_{DN} in the image where the spacing is $3\text{ }\mu\text{m}$. It was shown in the studies of the RD50-MPW2 submission, that V_{BD} is dependent on this distance between these electrodes. Both TCAD simulations and measurements of fabricated devices show that by increasing this distance, reverse breakdown can be increased. This was confirmed by measurements of test structures included in the submission.

In the second scenario shown in figure 5.3b, a typical pixel (like in the first scenario) has been backside processed and the topside substrate PWELLS have been left floating. This is very similar to the situation in measurements of H35DEMO and MuPix8/ATLASPix1 presented in the next section. TCAD simulations of a backside processed pixel with floating topside contacts presented in the next section show that the breakdown voltage can be increased, but is still limited by the p-type wells used in the floating topside contacts. It should be noted that guard rings have not been included in this simulation or any of the other two scenarios to keep the simulation as simple as possible. High breakdown voltages of designs like this (backside p-type contact and floating p-type implants between pixels) have been obtained with specific guard ring structures implemented at the edge of the chip [11].

And finally, the third scenario shown in figure 5.3c, is a typical pixel but without topside substrate contacts. The substrate is biased using only the backside contact. TCAD simulations of a pixel with the topside contacts removed and the substrate

biased from the backside show that the breakdown voltage can be increased significantly. This is due to the increased spacing between diode electrodes, from $< 10 \mu\text{m}$ to the thickness of the chip ($280 \mu\text{m}$, in this case). In a final design of a sensor like this, the entire chip would need to be designed in this way. In LFoundry 150 nm technology for example, there are no PWELL or PSUB implants on the topside of the design except for those that are isolated from the substrate by DNWELLs. One of the benefits of this design is that pixel size no longer includes the width of the PWELL or the distance between PWELL and NWELL that are required for high breakdown voltage. Therefore detector granularity could be slightly increased by making the pixel size can be smaller.

5.2.1 Structure simulations

The three scenarios were simulated using TCAD. The doping profiles used were those from reference [5] as these simulations were performed before the method presented in this thesis in chapter 3 was developed. The simulation of the first scenario is displayed on the left of figure 5.4a where the colour of the plot is doping concentration. The legend has been removed to hide the exact doping concentrations, but blue represents high p-type concentration and red represents high n-type concentration. The red squares highlight the zoomed-in images shown on the right. The inset on the top-right shows a zoomed-in view of the topside of the simulation, demonstrating that the simulated pixel has topside substrate contacts, seen on the right in blue. The inset on the bottom-right shows a zoomed-in view of the backside of the simulation and demonstrates that this simulated scenario has no backside doping or contact. Figures 5.4b and 5.4c show the second and third scenarios, respectively. In the top-right inset of 5.4b the topside substrate contact can be seen, and this is left floating. The top-right inset of 5.4c shows that this topside substrate contact has been removed. The bottom-right insets of figures 5.4b and 5.4c show that both scenarios have a backside p-type well which biases the substrates.

Each simulation consists of one pixel in a large area of substrate. The pixel cross-section is equivalent to the simulations in the previous chapter. No SiO_2 STI (and therefore no oxide charges) was defined to make simulations as simple as possible and keep simulation times short. The full depths of the simulations are equal to the estimated thickness of final fabricated samples. The width of the simulation was chosen arbitrarily to allow the depletion region to grow laterally, but keep the simulation time to a minimum. In these initial simulations, the substrate resistivity was set to $500 \Omega \cdot \text{cm}$ by defining a constant doping profile throughout the substrate. The species used was boron and the concentration was set to $2.657 \cdot 10^{13} \text{cm}^{-3}$ [12]. The backside contact was created in the same way that the topside substrate

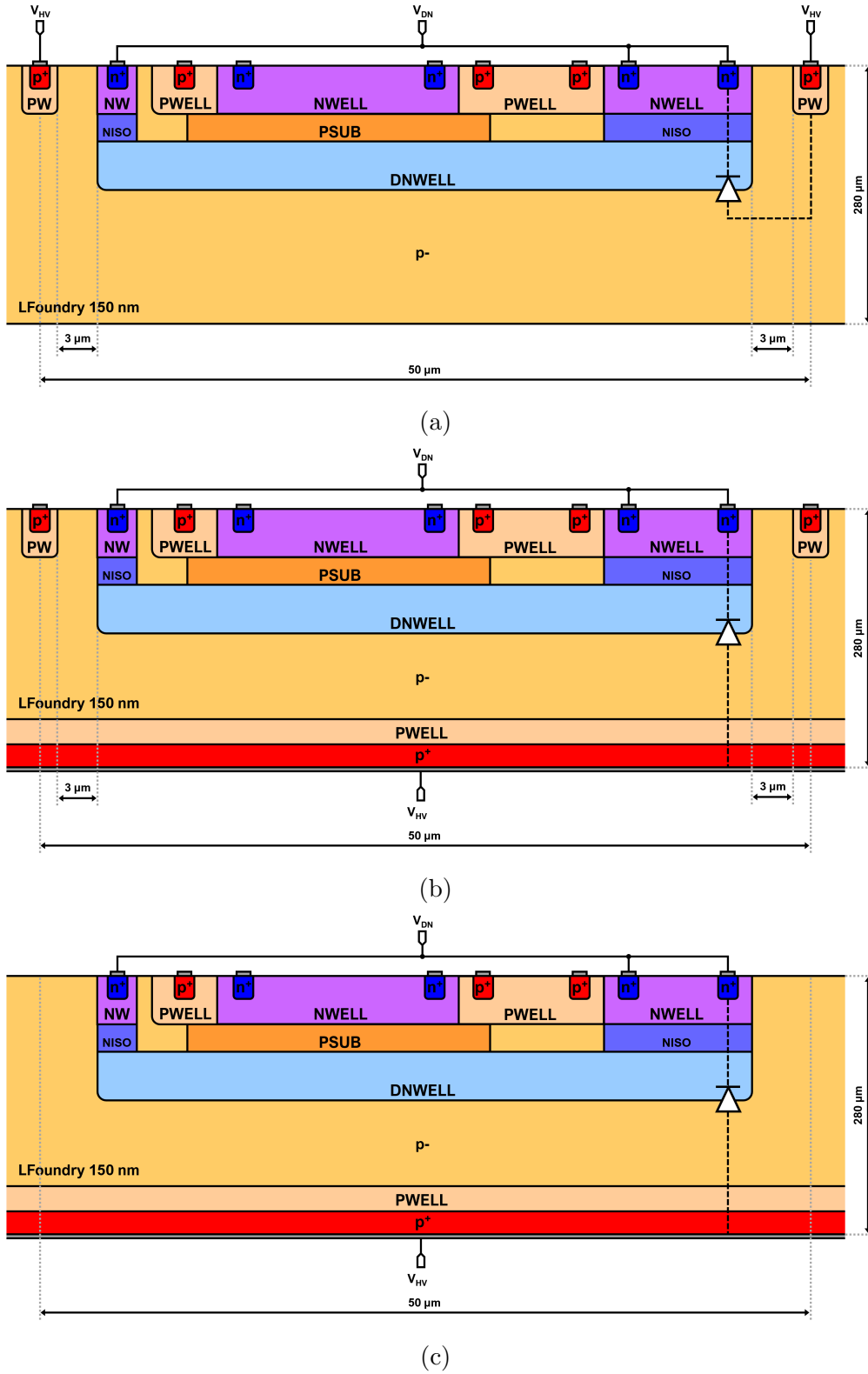


Figure 5.3: (a) Cross-section diagram of a typical pixel in LFoundry 150 nm technology. This is scenario 1. (b) The same cross-section, backside processed. The topside substrate contacts are left floating and the substrate is now biased to high voltage from the backside. This is scenario 2. (c) The same cross-section where topside contacts have not been included. This is scenario 3.

contacts are defined using p+ and PWELL doping profiles to keep the properties of the contact the same between all scenarios. A thin region of metal across the width of the simulation was also defined. The temperature was set to 300 K in all simulations. No scenario with a low-concentration p-spray has been simulated as this is not available in the LFoundry 150 nm technology. The simulation was designed to recreate what would currently be possible in their technology. A scenario with p-spray will need to be performed in the future.

5.2.2 Device simulations

In all three simulations, the pixel was biased to 0 V. Then, depending on the scenario, using a transient ramp similar to that described in chapter 3, the appropriate substrate contacts are ramped to negative high voltage in 1 Vs^{-1} steps. Figure 5.5 shows the results of these simulations. The first scenario is shown with a solid line. The reverse breakdown voltage is approximately 80 V which matches what was seen in chapter 3. Scenario 2 is shown with a dashed line. The reverse breakdown voltage is approximately 180 V which shows that the breakdown voltage can be increased by backside biasing and leaving the topside contacts floating. This is because the topside contacts are not at a fixed potential and the electric field therefore does not become high enough for avalanche breakdown. It is possible that this value could be increased further if some guard rings were implemented at the edge of the simulation like those in reference [11].

Scenario 3 is shown with a dotted line. The reverse breakdown is approximately 900 V. This is due to the fact that there is no high concentration p-type implant necessary to form high electric field for avalanche multiplication. The 300 V or so difference between simulations and measured values are likely due to idealisations in simulations. Current generation due to diced edges are not taken into account, nor are contributions from simulating in three dimensions. Nevertheless, this shows that by removing the topside p-type contacts entirely, the breakdown voltage can be increased significantly. These simulations form the basis for the UKRI-MPW0 design. The following sections describe the simulations and design considerations in order to convert this idea from a single pixel to a chip-wide design.

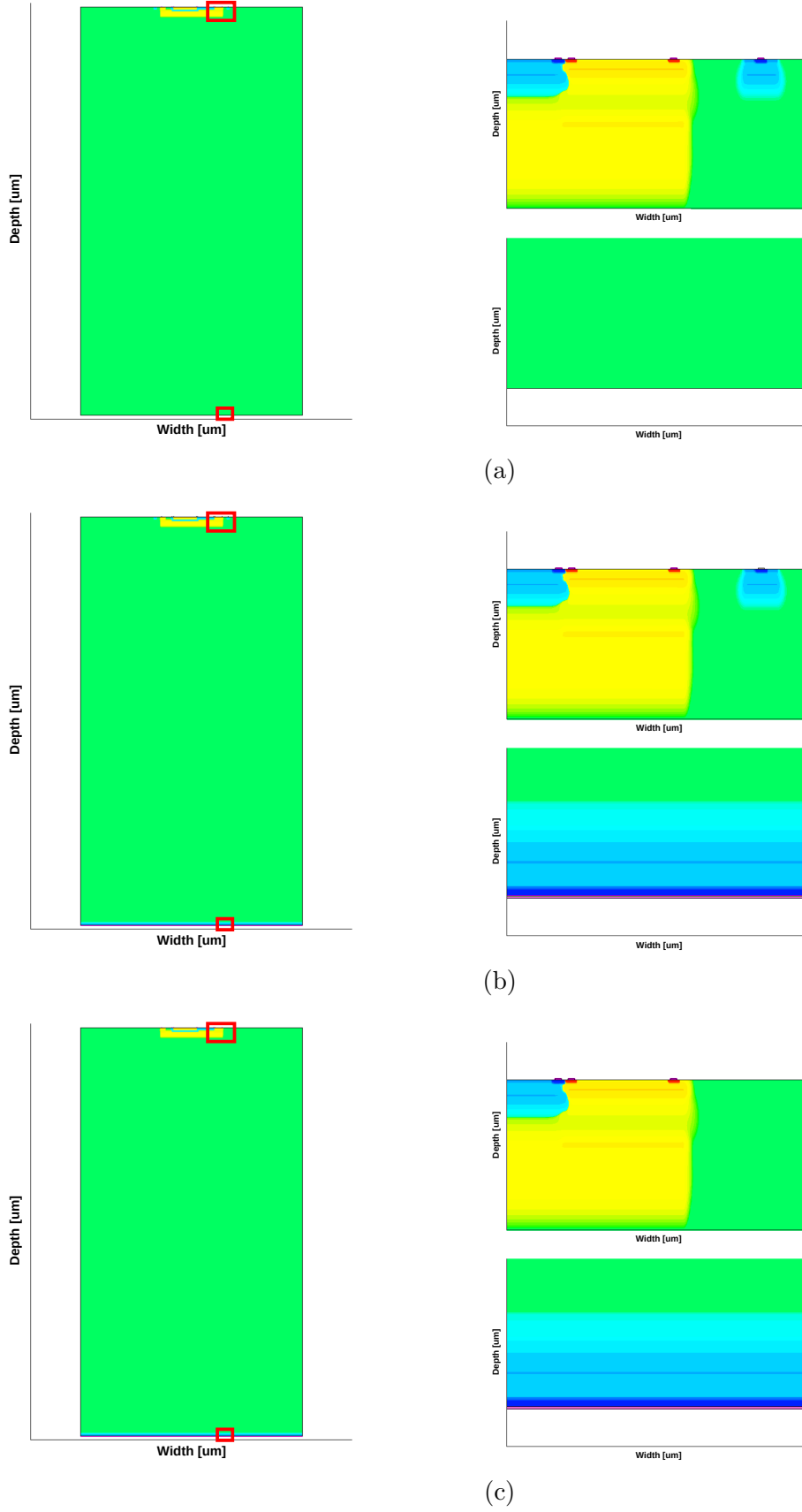


Figure 5.4: (a) TCAD simulation of scenario 1. (b) TCAD simulation of scenario 2. (c) TCAD simulation of scenario 3. The red squares in the images on the left highlight the insets on the right.

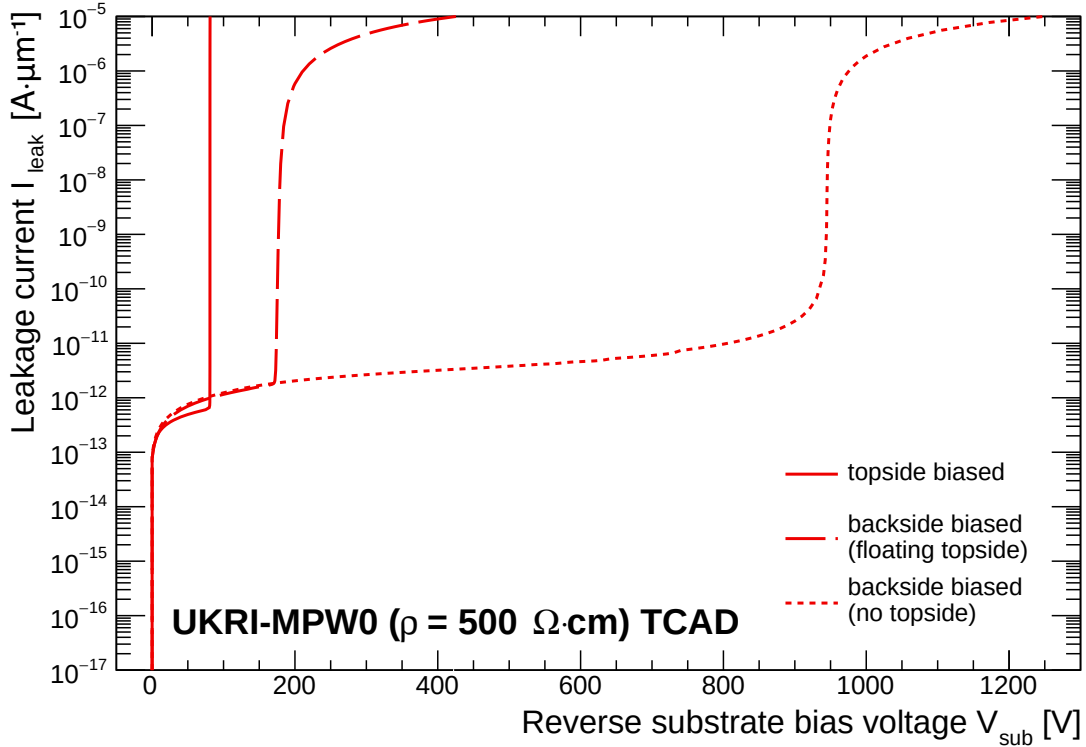


Figure 5.5: Results of TCAD simulations. A backside biased pixel with no p-type implants on the topside has a significantly larger reverse breakdown voltage than pixels with p-type wells on the topside.

5.3 Measurements of backside processed HV-CMOS detectors

5.3.1 Experimental setup

A Particulars scanning-TCT system [13] was used for the measurements. A diagram can be seen in figure 5.6. The main components are the three *stages*, that are capable of sub-micron movement in each of the three directions labelled x , y , and z . The sample under test, is mounted on stages x and z , and is therefore able to move in two directions (into the page and vertical directions in figure 5.6, respectively). The final stage is reserved for the focussing optics of the laser that can be moved in the remaining y direction (horizontal in figure 5.6). By moving the laser optics the waist of the laser beam can be placed directly below the structure under study.

In e-TCT measurements [14], the edge of the sample is illuminated with a collimated and pulsed infrared laser of wavelength 1064 nm. In response to the laser pulse, electron-hole pairs are generated inside the depleted bulk, and drift towards the collecting electrodes due to the electric field. The charge carriers induce a current at the collecting electrodes, which is amplified by a discrete amplifier and the signal is digitised and recorded by a DRS4 evaluation board from the Paul Scherrer

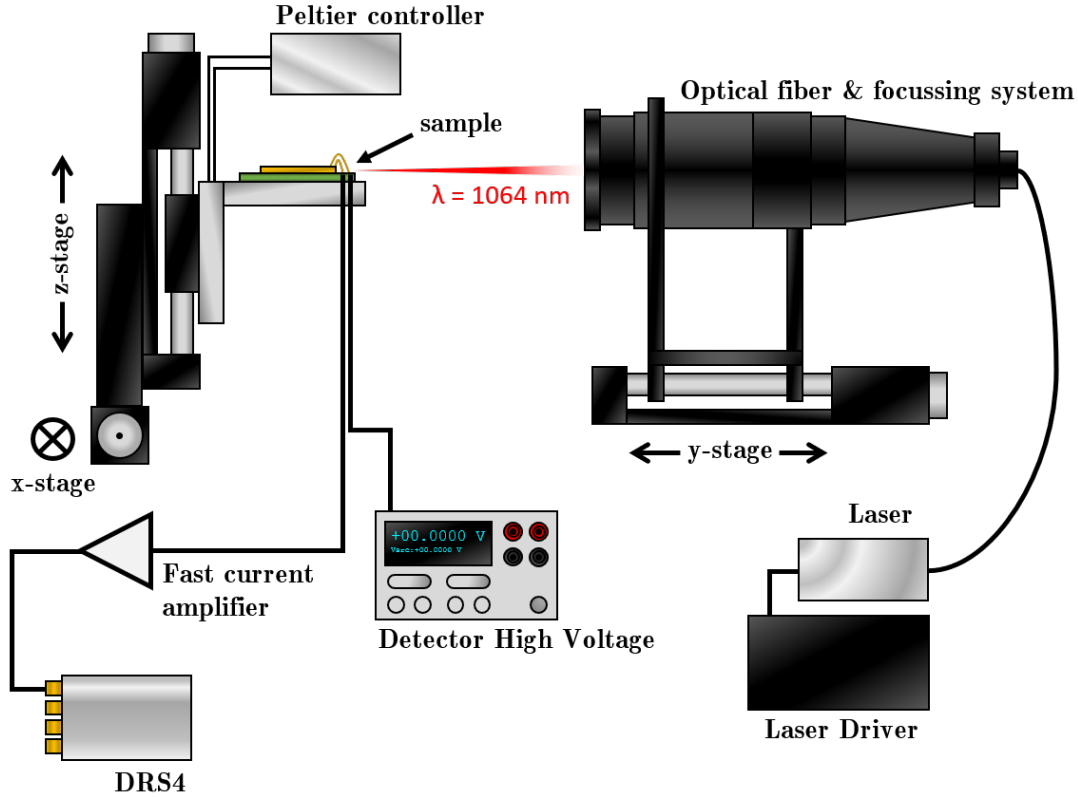


Figure 5.6: Diagram of the e-TCT setup used in this study.

Institut (PSI) [15]. An analysis library is provided [16] which is based on ROOT [17].

To reduce contributions from noise to the signal and avoid effects of annealing in irradiated samples, the x - z stage can be cooled via the Peltier controller. In this study, the stage was kept at -20°C for the duration of the measurements. The system is isolated inside a metal box, which is continually flushed with nitrogen to prevent condensation.

5.3.2 H35DEMO

The H35DEMO (see figure 5.7a) is a pixel demonstrator device, fabricated in an engineering run in 2015 in the $0.35 \mu\text{m}$ HV-CMOS process from ams AG [18]. It measures $18.49 \text{ mm} \times 24.40 \text{ mm}$, and uses a p-type substrate, with samples produced with nominal resistivities between $20 \Omega \cdot \text{cm}$ and $1000 \Omega \cdot \text{cm}$. The chip contains four large matrices of pixels, and test structures at the top and bottom of the device, which are described in detail in reference [2]. The measurements in this work have been performed on the test structure shown in figure 5.7b, which is highlighted in red also at the bottom of figure 5.7a.

This test structure consists of a 3×3 matrix of passive HV-CMOS pixels, each measuring $50 \mu\text{m} \times 250 \mu\text{m}$, which share the same cross-section as the pixels in

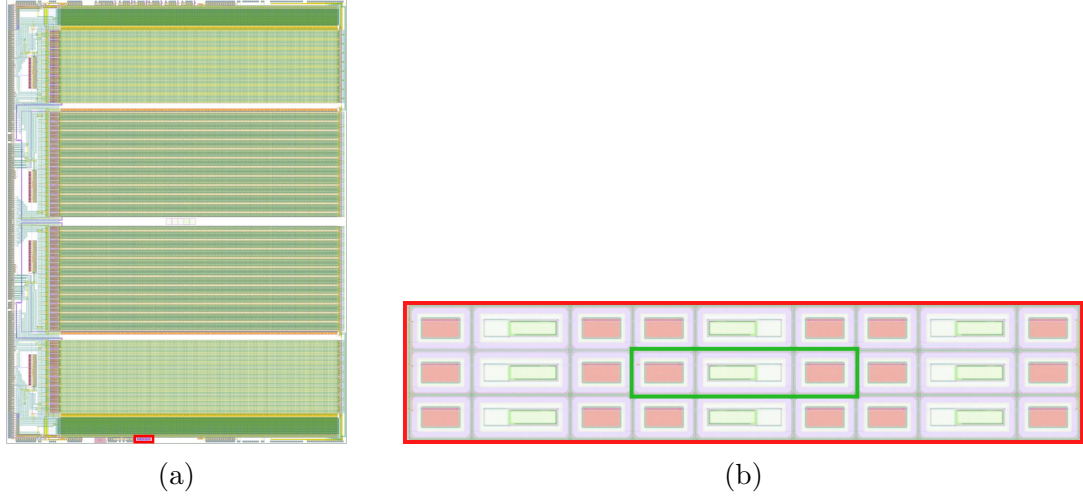


Figure 5.7: (a) Image of the H35DEMO chip. The test structure used in these measurements is highlighted in red at the bottom (b) Test structure used in e-TCT measurements. The central pixel is highlighted in green.

the larger matrices. The size of the pixels was chosen to match the size of pixels of the FE-I4 readout chip [19]. A diagram of the pixel cross-section can be seen in Figure 5.8a. The substrate is p-type which is biased to high negative voltage through the p+, shallow p-tub, deep p-tub stacks (p+/SPTUB/DPTUB) on the outsides of the diagram and each pixel is implemented by means of three deep n-tubs (DNTUB) which forms three reverse biased diodes connected in parallel. The depletion region grows downwards into the substrate which forms the sensitive area for particle detection. Shallow n-tubs (SNTUB) and shallow p-tubs (SPTUB) implemented into the central DNTUB as this follows the design of the pixels in the larger matrices, where NMOS and PMOS logic are implemented into SPTUBs and SNTUBs respectively (with the exception of one of the matrices which includes logic in all three DNTUBs).

The test structure provides two readout channels, one to access the central pixel (highlighted in green in figure 5.7b) and the other one to access the outer eight pixels, which are shorted together. The central pixel is the main focus of the work here, but the outer pixels can be used to study charge sharing effects. Results of other studies of e-TCT measurements of H35DEMO samples can be found in [9, 20, 21], and test beam measurements can be found in [22].

5.3.2.1 Post-fabrication processing

Backside processing

After fabrication, an undiced wafer of $600\text{--}2000\ \Omega \cdot \text{cm}$ H35DEMO samples was sent to Ion Beam Services (IBS) [23] for backside processing and dicing. Backside processing included TAIKO thinning from $700\ \mu\text{m}$ to $100\ \mu\text{m}$ using 4000 grade mesh

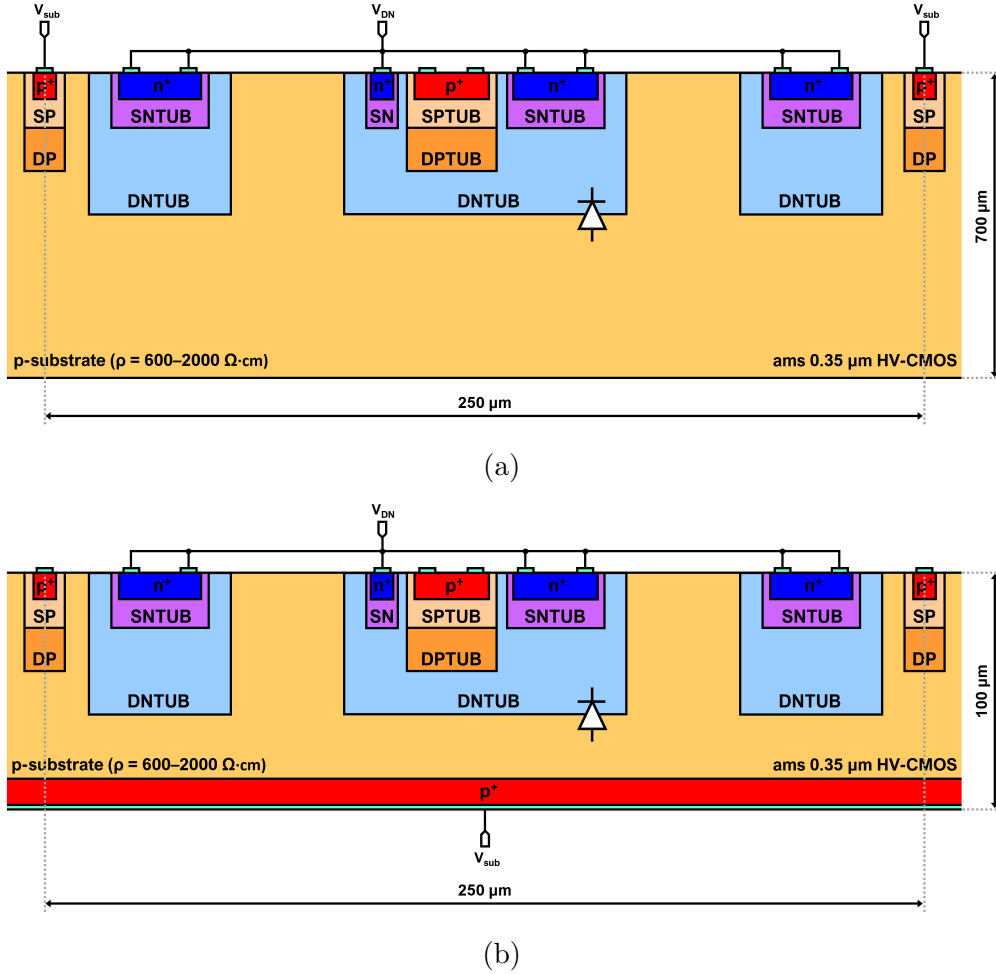


Figure 5.8: (a) Cross-section diagram of an H35DEMO test structure pixel. The default substrate thickness is 700 μm. (b) The same cross-section after thinning to 100 μm. The topside substrate contacts are left floating and the substrate is now biased to high voltage from the backside.

and plasma etching to remove potential defects, backside p+ implantation with boron (dose $5 \cdot 10^{14}$ at · cm⁻²), rapid thermal annealling (RTA) at 450°C for 30 seconds to activate the implantation, and backside metallisation to a thickness of 1022 nm with titanium and aluminium to create a contact [6].

Polishing edges

After dicing, a large, raised line of silicon could be seen on the edge of samples (figure 5.9a). This is a problem as it can refract laser light in the e-TCT measurements. Therefore, the bottom edges of the samples (according to figure 5.7a) were polished with 3 μm lapping sheet and 1/10 μm grade diamond paste to remove the defects. Only this edge of the samples was polished, as it is the edge illuminated with the laser in the measurements and since after thinning, the samples became very brittle and polishing a single edge reduced the likelihood of breakages. A photo of the edge

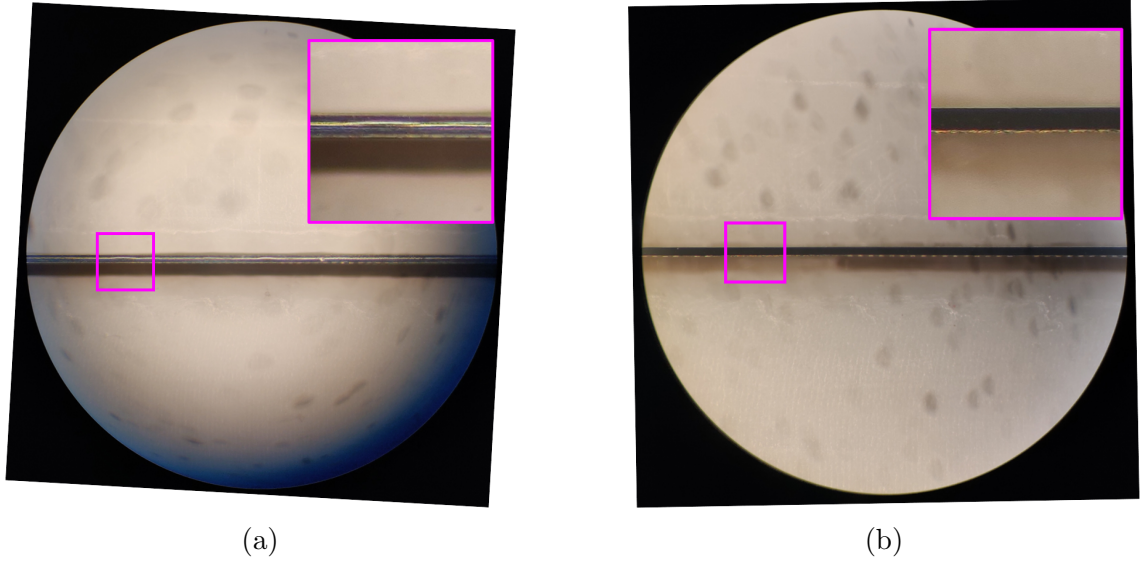


Figure 5.9: (a) Edge of H35DEMO sample before polishing. The white line that can be seen is a raised line of silicon left over after dicing (b) Edge of the same sample in (a) after polishing.

of a sample after polishing can be seen in figure 5.9b.

Irradiation campaign

Six samples were irradiated with neutrons at the TRIGA reactor at the Jožef Stefan Institute (JSI) in Ljubljana [24]. Individual samples were irradiated to different 1 MeV neutron equivalent fluences Φ_{eq} ranging from $1 \cdot 10^{14} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$ to $2 \cdot 10^{16} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$. No annealing was performed on the samples, which were kept cold using frozen ice packs during transport from the JSI facility and during all $I - V$ and e-TCT measurements in this study. Table 5.1 shows the measured fluences.

Table 5.1: Samples in this study, their resistivities and fluences measured

Sample	$\rho [\Omega \cdot \text{cm}]$	$\Phi_{\text{eq}} [10^{14} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}]$								
		1	2	5	10	20	30	50	100	200
MuPix8/ATLASPix1 W1	50–100		.	.	.	.		.	.	
MuPix8/ATLASPix1 W2	100–400	.	.	.	.	.		.	.	.
H35DEMO	600–2000	.		.			.	.	.	.

PCB

The custom PCB designed at Liverpool features a large pad to enable backside biasing. Samples were glued to this large pad using silver conductive paint. The test structure pads were wirebonded to the PCB in order to process readout signals. Each sample in this work was glued to a PCB by hand, therefore there are variations in the position of pixels relative to the system sample to sample.

5.3.2.2 I - V measurements

Current-voltage (I - V) measurements were used to determine the approximate reverse breakdown voltages V_{BD} of each sample, and therefore, the safe maximum operating voltages samples can be biased to in e-TCT measurements. The pad of the PCB for backside biasing the samples was connected to the negative terminal of a Keithley 2410 source meter and the pad of the central pixel was connected to the positive terminal. The supply was ramped to a negative high voltage in 1 V steps, and the current was recorded. Compliance current was set to $10\ \mu\text{A}$. At this value, the diode was considered to have reached reverse breakdown, and the measurement was stopped. This was repeated for a non-irradiated sample and the irradiated samples.

Leakage current I_{leak} is not studied in great detail in this work, but it can be seen in figure 5.10 that I_{leak} increases with Φ_{eq} . This is expected due to lattice damage in the bulk and is described in reference [25] with formula 2.4 presented in chapter 2. Variations in V_{BD} of the non-irradiated and low fluence samples can be expected due to initial sample-to-sample variation, but higher fluence samples ($3 \cdot 10^{15}\ \text{n}_{\text{eq}} \cdot \text{cm}^{-2}$ and above) were observed to exhibit a softer breakdown, allowing samples irradiated to higher fluences to be biased to higher voltages in e-TCT measurements. This effect can be confirmed somewhat quantitatively with the TCAD simulations in chapter 3, in simulations of samples in a different technology (see figure 3.24). I_{leak} of the non-irradiated sample and sample irradiated to $1 \cdot 10^{14}\ \text{n}_{\text{eq}} \cdot \text{cm}^{-2}$ (at low voltages) was too low to measure accurately with the equipment available. The increase in leakage current for the sample irradiated to $1 \cdot 10^{14}\ \text{n}_{\text{eq}} \cdot \text{cm}^{-2}$ is not understood.

5.3.2.3 E-TCT Measurements

Focus finding in x

In order to see a cross-sectional image of the depletion region of the pixel, the sample is biased to a fixed voltage and the optics to sample distance is fixed. The latter value is initially approximated according to the installation instructions [26] at 8.5 cm for an infrared laser. The laser is then moved closer and further away in a trial and error fashion until the signal strength is largest. In this example, the substrate was biased arbitrarily to $V_{\text{sub}} = -14\ \text{V}$, y was fixed to $y = 37200\ \mu\text{m}$ in system coordinates, and the sample was scanned at $5\ \mu\text{m}$ steps in x and $2\ \mu\text{m}$ steps in z . At each position, a current waveform was recorded (see figure 5.11a) and the collected charge Q is calculated by integrating the current I :

$$Q = \int_{t_i}^{t_f} I\ dt \quad (5.1)$$

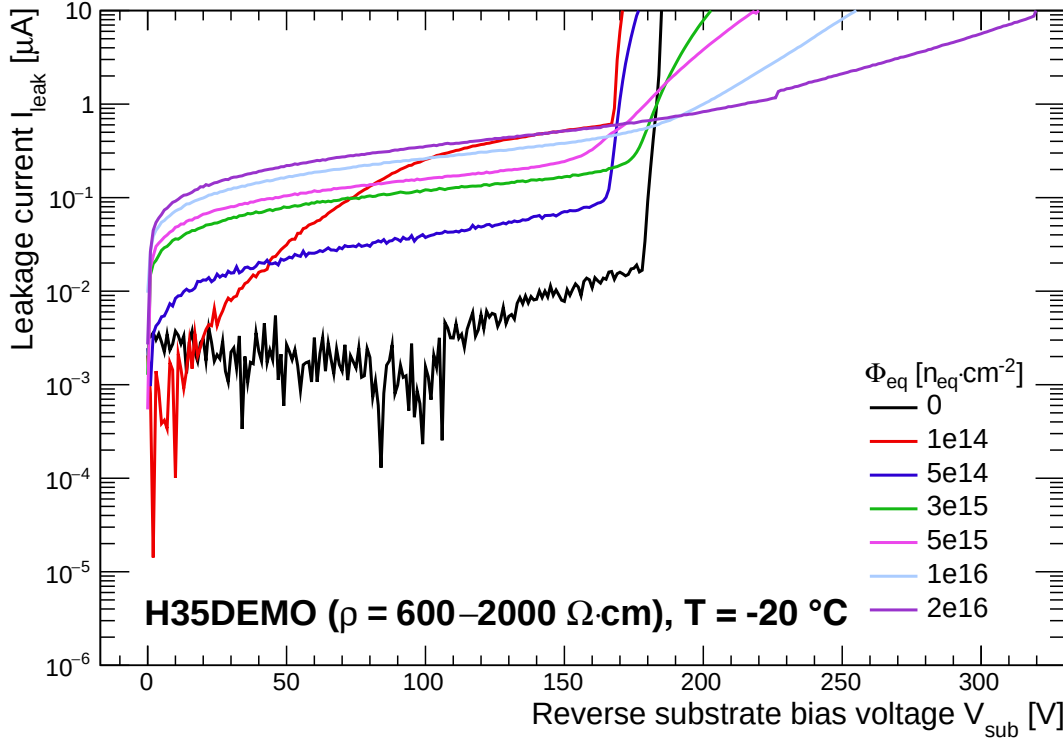


Figure 5.10: I - V measurements of backside biased irradiated H35DEMO samples.

where t_i is the initial time and t_f is the final time. The integration time used was 7 ns. The charge was plotted as a function of x and z positions in a 2D histogram to build up an image of the depletion region of the central pixel (see figure 5.11b) where the colour of the plot corresponds to the charge collected. The dimensions in this image are equivalent to the cross-section diagram of the pixel seen in figure 5.8b. The left edge of the depletion region is at approximately $x = 30150 \mu\text{m}$ and the right side of the depletion region is at $x = 30400 \mu\text{m}$. The width of the depletion region is therefore approximately $250 \mu\text{m}$ which is appropriate as this is the same as the width of the pixel. The topside of the pixel is at approximately $z = 19320 \mu\text{m}$ and at around $z = 19260 \mu\text{m}$ is the boundary or bottom of the depletion region. This means that approximately $60 \mu\text{m}$ of the substrate is depleted at $V_{\text{sub}} = -14 \text{ V}$. The shape is due to the fact that the pixel is divided into three diodes. A small peak in charge collection can be seen at around $z = 19220$ where below this depth no more charge is collected. This corresponds to the backside of the sample, which again is appropriate as samples were thinned to $100 \mu\text{m}$. The small peak in charge collection at the backside is due to the p+-p-substrate transition. The difference in Fermi levels is enough to create an electric field.

Figures 5.11c and 5.11d show a waveform and charge collection distribution of the outer eight pixels in the test structure. More charge is collected as this charge represents the sum of total charge collected by the eight pixels surrounding the cen-

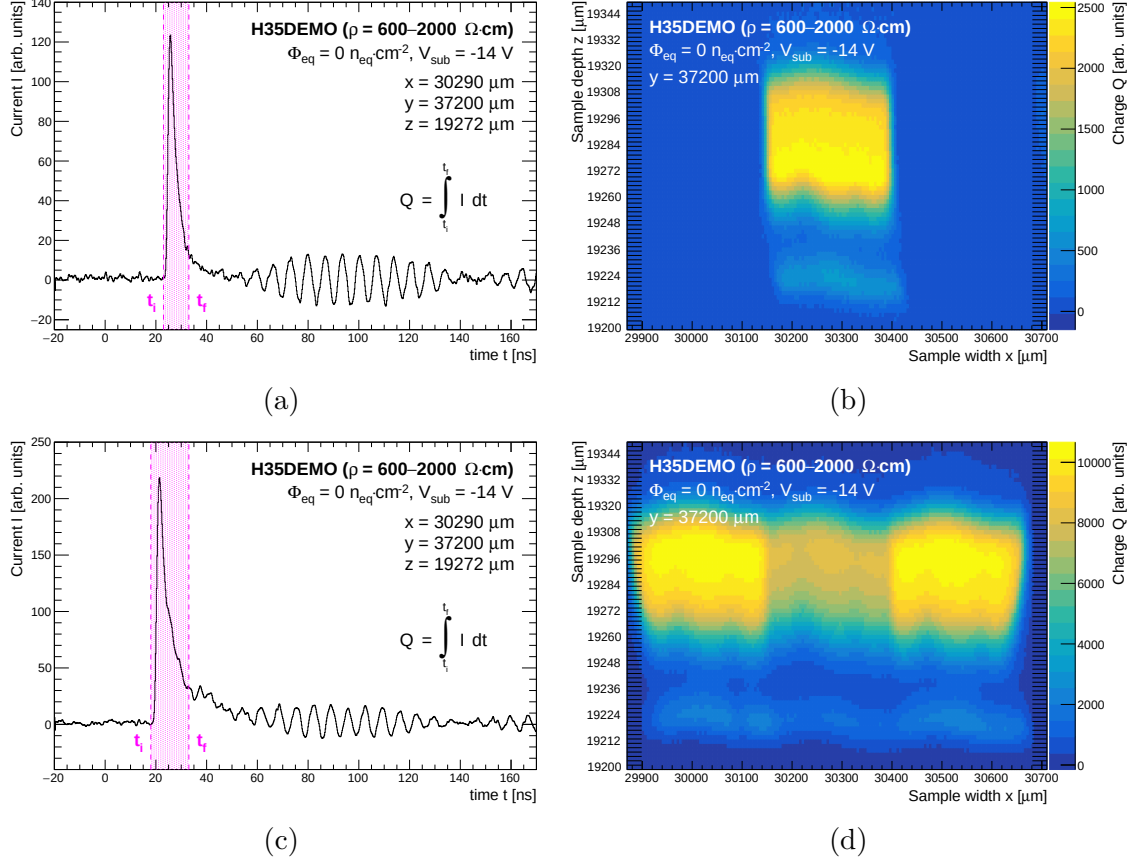


Figure 5.11: (a) Current waveform of the central pixel of non-irradiated H35DEMO test structure biased to $V_{sub} = -14 \text{ V}$ recorded at laser position (x, y, z) . This is integrated between t_i and t_f to calculate the charge Q collected. (b) 2D histogram of integrated waveforms corresponding to the central pixel. The scan is performed in the x and z directions at fixed y and V_{sub} . (c) Current waveform of outer pixels in the test structure. (d) x - z scan of outer pixels.

tral pixel, but is not eight times as large as the central pixel due to the intensity profile of the beam i.e. the waist of the beam is not focussed directly under these pixels. The left edge of the charge collection profile is at approximately $x = 29900 \mu\text{m}$ and the right is at $x = 30650 \mu\text{m}$. This means the width of the depletion region is approximately $750 \mu\text{m}$, which makes sense as there are three pixels in this direction. The centre of the central pixel is approximated from figure 5.11b $x_0 = 30275 \mu\text{m}$ and used in the next measurement.

Characterisation of the beam profile and focus finding in y

Optimal optics to sample distance y was chosen using the knife-edge technique i.e., at the position y where the change in charge collected is the greatest as z changes. The method is outlined in reference [27] for strip and pad detectors. This work follows the method for strip detectors in the edge configuration, but has been modified to account for the sample technology.

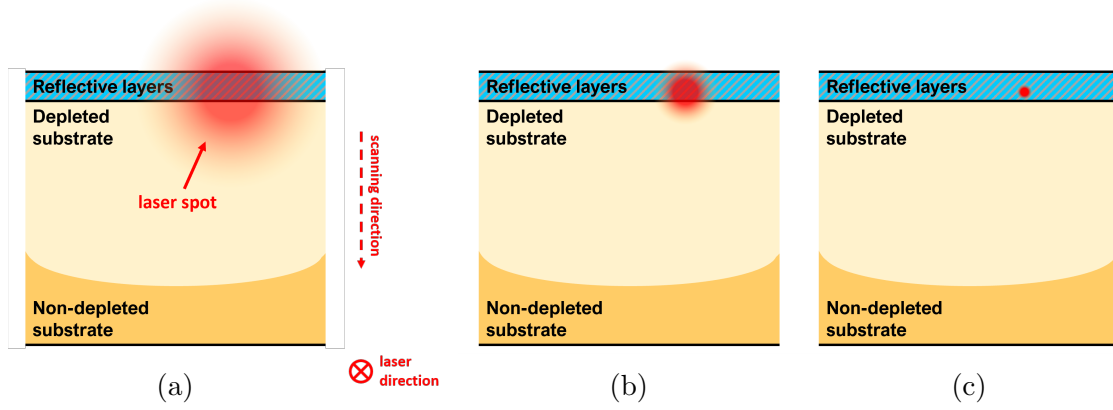


Figure 5.12: (a) The beam waist is not focussed. (b) Slightly unfocussed beam waist. (c) The beam waist is focussed. While near-zero charge would be collected in this instance, moving the high-intensity spot from the reflective (i.e. non-sensitive) metal/dielectric layers to the sensitive substrate produces the greatest change in collected charge. This means the laser is the most focussed.

The sample was biased to a fixed voltage $V_{\text{sub}} = -100 \text{ V}$ to ensure it was fully depleted, but below breakdown. In this way, either the topside or the backside could be used to characterise the beam profile. In this case the topside of the sample was used. The laser was moved up and down in the z direction between the interface of the non-sensitive/reflective topside dielectric/metal layers and the depleted silicon bulk (see figure 5.12a). When the laser is pointed at the non-sensitive metal layers and not focussed, a small amount of charge is collected anyway. The laser is then moved closer to the sample and the metal–silicon interface is scanned again (see figure 5.12b). Less charge is collected as there is less laser in the bulk but the beam is more intense. y is increased again and as z decreases (in this case), the smaller, more intense spot will give the greatest change in collected charge.

Just like the x focus finding, a waveform is recorded at each position and integrated to calculate charge. The result is figure 5.13a. The left side of the plot corresponds to the side closest to the polished edge of the sample and the right hand side is the bulk of the sample. The charge collected is highest when the waist of the beam is directly underneath the pixel where $y \approx 37400 \mu\text{m}$. If we take the projection of the histogram at this value of y , we can see the charge collection profile (figure 5.13b). As the sample was fully depleted we can see that the approximate width of this profile is around $100 \mu\text{m}$. This again, makes sense as these H35DEMO samples were thinned to $100 \mu\text{m}$. A sample of the data near the waist, $37050 \mu\text{m}$ – $37700 \mu\text{m}$ of the beam was taken and projections of the data were then plotted. An error function was fit to each projection

$$Q(z) = \frac{Q_{\text{max}}}{2} \left(\text{erf} \left(\frac{z - z_0}{w} \right) + 1 \right) \quad (5.2)$$

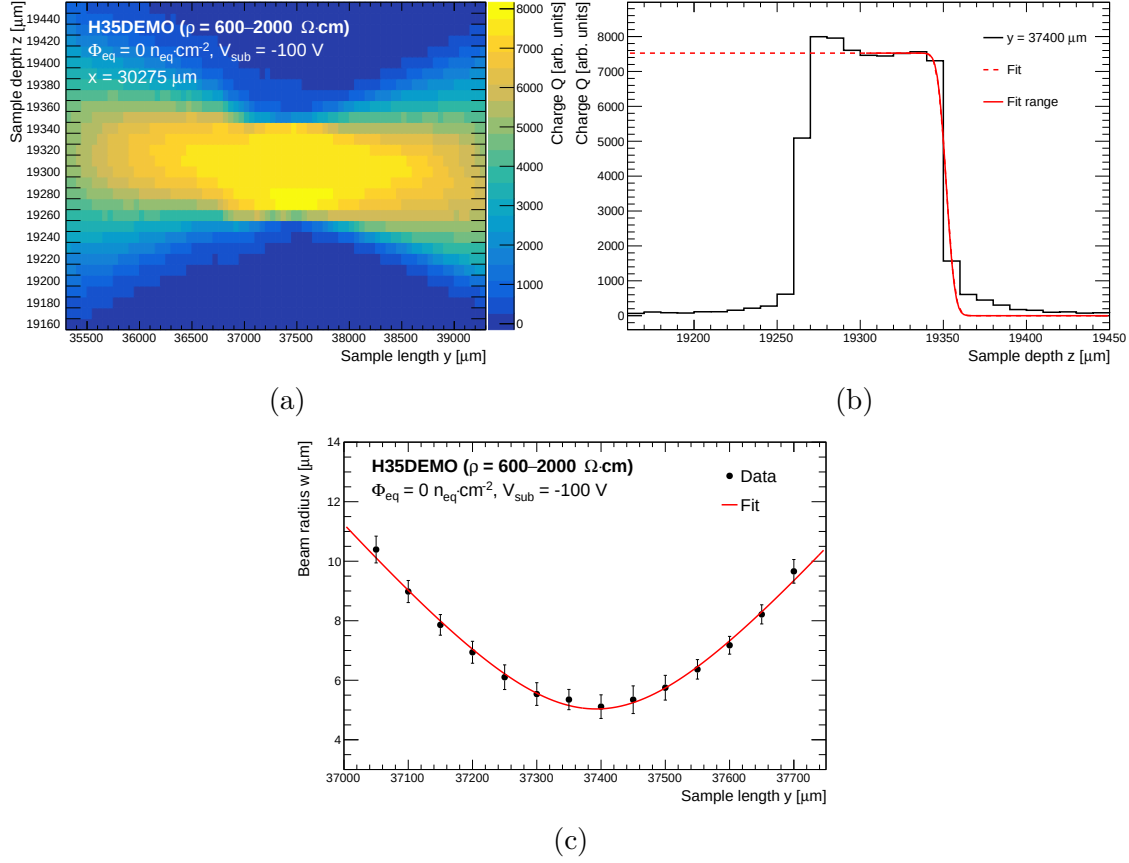


Figure 5.13: (a) 2D histogram of integrated waveforms corresponding to the central pixel. The scan is performed in the y and z directions at fixed x and V_{sub} . (b) Example of projection from (a). An error function is fit to the edge corresponding to the topside of the sample to extract the beam radius w . (c) Plot of w against y . The minimum beam radius is the beam waist w_0 , and the corresponding value of y is the position at which the laser is focussed y_0 .

where Q_{max} is the maximum charge ignoring the peak at the backside, z_0 is the position of the topside of the sample and w is the beam radius. Extracting w from the fit and plotting this against y produces figure 5.13c. The data was fit with

$$w(y) = w_0 \sqrt{1 + \left(\frac{y - y_0}{y_R} \right)^2} \quad (5.3)$$

where w_0 is the minimum value of the beam radius, known as the beam waist, y_0 is the optimum position for the laser, and y_R is the Rayleigh length given by

$$y_R = \frac{\pi w_0^2 n_{\text{Si}}}{\lambda} \quad (5.4)$$

where n_{Si} is the refractive index of silicon and λ is the wavelength of the laser. y_0 is extracted from equation 5.3 and set as the position of the laser. $y_0 = 37392.4$ in this case. $w_0 \approx 5$ which means the beam diameter is about $10 \mu\text{m}$.

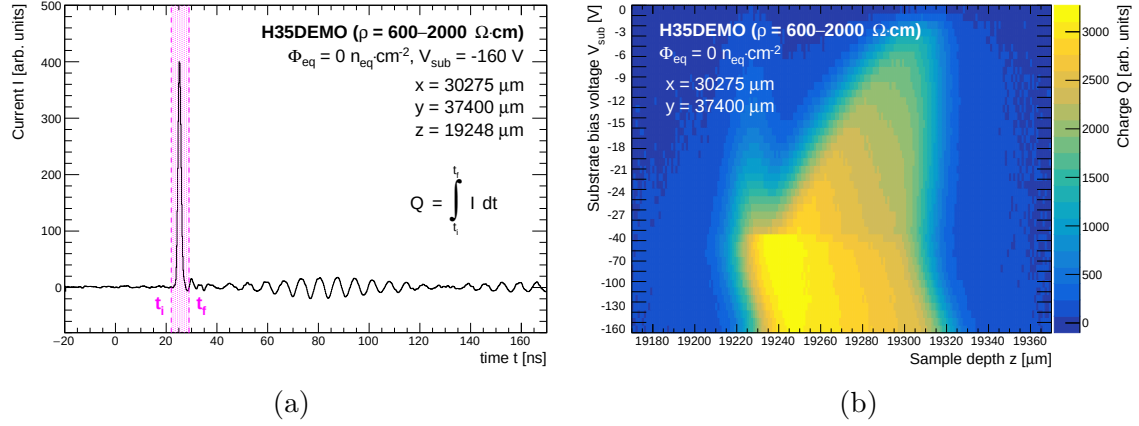


Figure 5.14: (a) Example of a waveform and integration window from the z - V_{sub} scan. x and y are fixed to x_0 and y_0 which are determined using x - z and y - z scans respectively. (b) Scan in z and V_{sub} for a high resistivity, thinned, backside biased, non-irradiated, H35DEMO sample.

Calculating the size of the depletion region

A scan in just the z direction at fixed $x = x_0$ and $y = y_0$ values for different bias voltages was used to characterise the growth of the depletion region. The sample is biased to high voltage, but below breakdown $V_{\text{sub}} = -160$ V and the z stage is moved in $1 \mu\text{m}$ increments. At each step, a waveform is recorded and integrated to calculate the charge collected (figure 5.14a). The voltage is decreased by 10 V, the stage is reset, and the sample scanned again in the z direction in $1 \mu\text{m}$ steps. The result is figure 5.14b. This is repeated until $V_{\text{sub}} = 0$ V. These measurements were repeated for each irradiated sample as well (see figure 5.15), including x and y focussing as each sample was at a different position with respect to the laser. It can be seen for samples that reach full depletion that a finer (2 V) voltage step was used before full depletion. The non-linear scale can be seen on the left axis of results for the non-irradiated sample, and samples irradiated to $1 \cdot 10^{14} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$ and $5 \cdot 10^{14} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$.

If we look at the projections of figure 5.14b, we can see the charge collection profiles at different values of V_{sub} (see figure 5.16a). The topside of the sample is on the right at approximately $z = 19310 \mu\text{m}$. As V_{sub} increases, charge Q increases, as does the width of the profile. This width is used to estimate the depth of the depletion region. Two peaks in charge collection can be seen. The first on the left at approximately $z = 19225 \mu\text{m}$ is due to the backside p+ implant, where an electric field is created by the highly doped backside p+ implant–low-doped p-substrate interface. The second, that can be seen best at voltages greater than $V_{\text{sub}} = -15$ V, is always seen at the depletion region boundary, and is due to the charge sharing between other pixels in the test structure (section 5.3.2.3). Similar to reference [21],

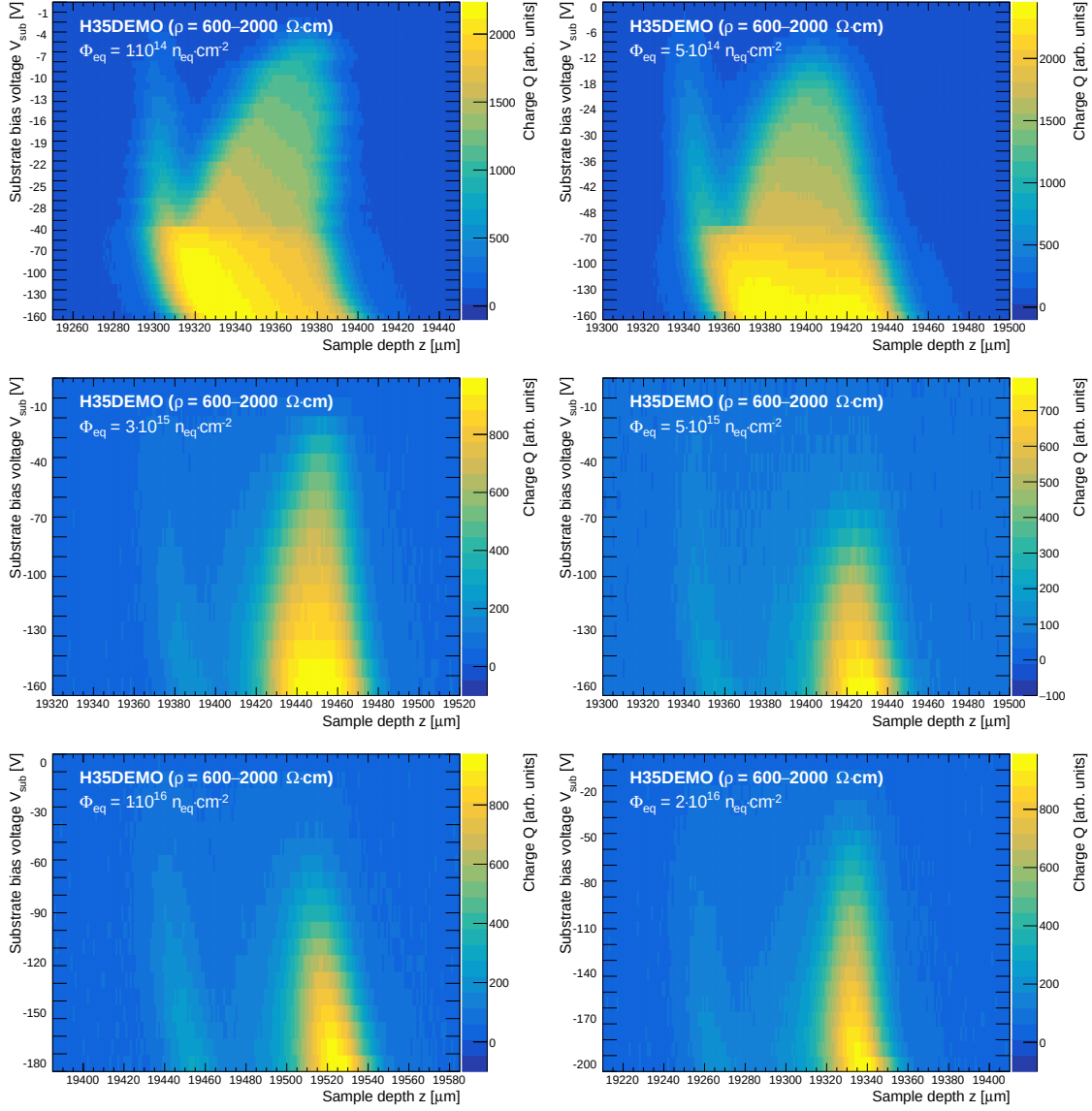


Figure 5.15: Scans in z and V_{sub} for high resistivity, thinned, backside biased, irradiated, H35DEMO samples.

to estimate the width of the charge collection profile, and therefore the depth of the depletion region, each projection was fitted with the equation

$$Q(z) = \frac{Q_{\text{max}}}{2} \left(\text{erf} \left(\frac{z - z_1}{w_1} \right) - \text{erf} \left(\frac{z - z_2}{w_2} \right) \right) + Q_1 \exp \left(\frac{(z - \mu_1)^2}{-2\sigma_1^2} \right) + Q_2 \exp \left(\frac{(z - \mu_2)^2}{-2\sigma_2^2} \right) + c \quad (5.5)$$

where Q_{max} again is the maximum charge ignoring the charge collection peaks, z_1 and z_2 , and w_1 and w_2 are the positions and widths of the error functions respectively. Q_1 , μ_1 , and σ_1 and Q_2 , μ_2 , and σ_2 are the peak heights, means, and standard deviations of Gaussians functions used to model the charge collection peaks. c is used to model

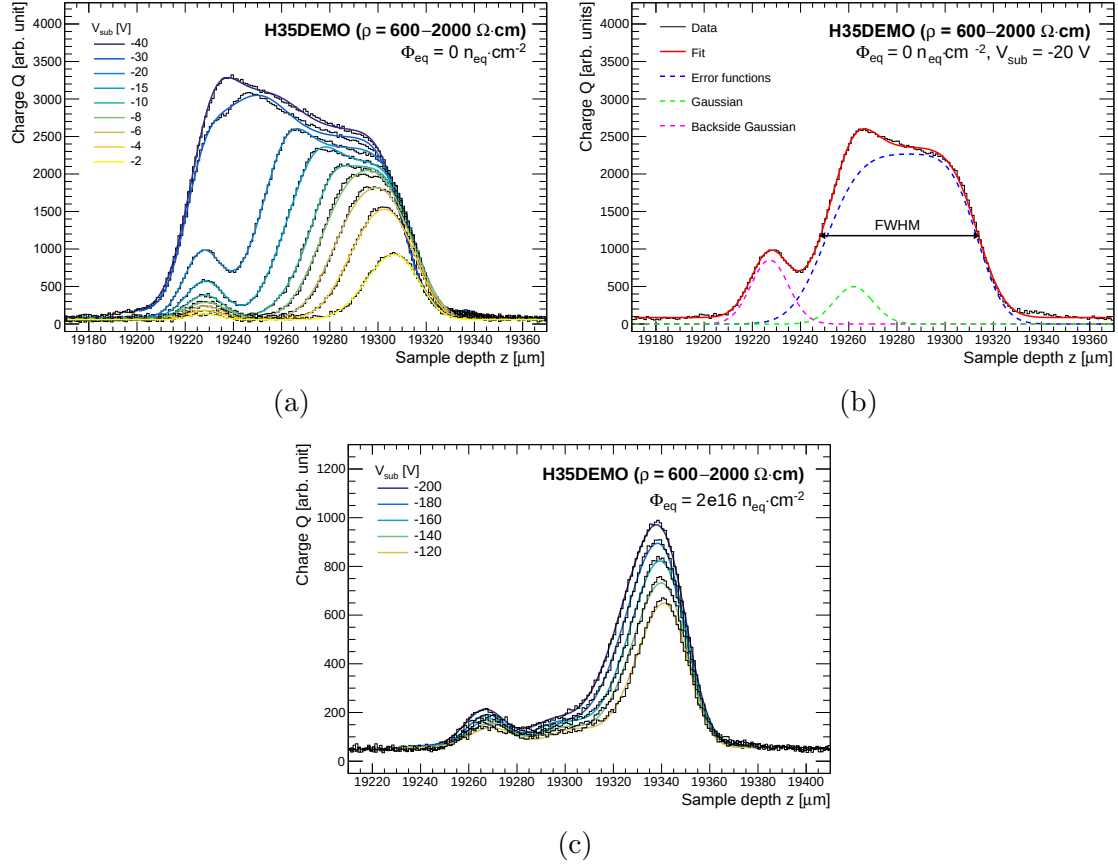


Figure 5.16: (a) Charge collection profiles for different values of substrate bias voltage V_{sub} for a high resistivity, thinned, backside biased, non-irradiated, H35DEMO sample. (b) Equation 5.5 fit (in red) to the charge collection profile at $V_{\text{sub}} = -20 \text{ V}$. The components of equation 5.5 are shown in dashed lines. The approximation of the depletion depth W_D (FWHM) is shown with a black arrow. (c) Charge collection profiles for a sample irradiated the highest fluence $\Phi_{\text{eq}} = 2 \cdot 10^{16} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$.

the noise for a better fit. An isolated projection for $V_{\text{sub}} = -20 \text{ V}$ can be seen in figure 5.16b. The components of equation 5.5 are plotted with dashed lines. The error functions in blue model the majority of the charge collection profile, created by the pixel depletion region. The Gaussian function in pink, centred at approximately $z = 19225 \mu\text{m}$ models the peak in charge collection at the backside. The second Gaussian function in green, centred at around $z = 19260 \mu\text{m}$, models the peak in charge collection due to charge sharing. Figures 5.16c and d demonstrate the same thing for the sample irradiated to the highest fluence, $2 \cdot 10^{16} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$.

The FWHM is evaluated when $Q(z)$ is equal to $Q_{\text{max}}/2$ plus the noise and provides an estimation for the depth of the depletion region W_D

$$W_D = k_2 - k_1 \quad (5.6)$$

where k_2 is the position of the top electrode and k_1 is the boundary of the depletion region. $k_2 \approx 19315 \mu\text{m}$ for the non-irradiated sample, which corresponds to the

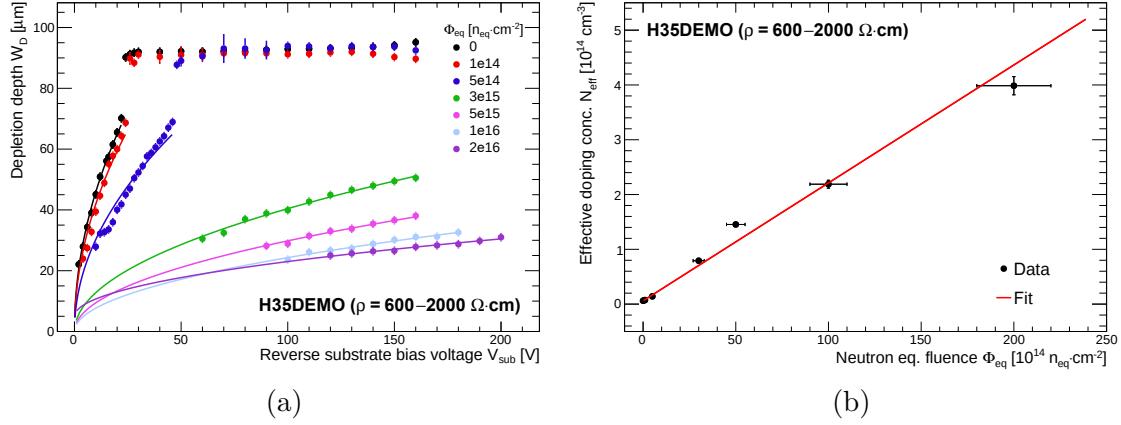


Figure 5.17: (a) Depletion depth W_D as a function of substrate bias voltage V_{sub} for a non-irradiated sample (black) and samples irradiated up to neutron equivalent fluence $\Phi_{\text{eq}} = 2 \cdot 10^{16} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$. (b) Evolution of effective doping concentration N_{eff} with Φ_{eq} .

underside of the deep n-well, close to the topside of the sample. When W_D is compared to V_{sub} , we get the black curve in figure 5.17a. W_D increases with V_{sub} following the square root law [28]

$$W_D = W_{D_0} + \sqrt{\frac{2\varepsilon_{\text{Si}}\varepsilon_0}{e_0 N_{\text{eff}}}} \cdot V_{\text{sub}} \quad (5.7)$$

where ε_{Si} is the relative permittivity of silicon, ε_0 is the vacuum permittivity, e_0 is the elementary charge, and N_{eff} is the effective doping concentration of the substrate. W_{D_0} is a parameter introduced to describe the collected charge measured at $V_{\text{sub}} = 0 \text{ V}$ [7]. It is a consequence of the non-zero laser beam width w_0 , charge collection by diffusion, and built-in depletion. N_{eff} is then extracted from the fits from all samples, and plotted against Φ_{eq} (figure 5.17b). The values of N_{eff} , the errors ΔN_{eff} , and the reduced χ^2 can be seen in table 5.2. The data is then fitted with [29]

$$N_{\text{eff}} = N_{\text{eff}_0} - N_c \cdot (1 - \exp(-c \cdot \Phi_{\text{eq}})) + g_c \cdot \Phi_{\text{eq}} \quad (5.8)$$

where N_{eff_0} is the initial doping concentration i.e. the doping concentration of the non-irradiated sample, c is the acceptor removal constant, N_c is the concentration of acceptors that have been removed and g_c is the stable damage introduction rate. The extracted values can be seen in table 5.5. In high resistivity silicon, all acceptors are removed at low fluence since the initial concentration is low. An example of such a measurement can be found in reference [30]. Since there are no measurements of low fluence samples presented here, N_c and c were set to 0. Therefore it can be seen that N_{eff} increases linearly with Φ_{eq} with $g_c = 0.022 \pm 0.001 \text{ cm}^{-1}$ (see figure 5.17b). This is slightly larger than the typical value of 0.02 cm^{-1} reported in literature, but consistent with high resistivity samples in other technologies [8, 30].

Table 5.2: Effective doping concentrations N_{eff} extracted from fits to measurements of depletion depth for H35DEMO samples irradiated to different fluences.

$\Phi_{\text{eq}} [\text{n}_{\text{eq}} \cdot \text{cm}^{-2}]$	$N_{\text{eff}} [10^{14} \text{cm}^{-3}]$	$\Delta N_{\text{eff}} [10^{14} \text{cm}^{-3}]$	χ^2/NDF
0	0.061	0.001	0.85
$1 \cdot 10^{14}$	0.073	0.001	4.89
$5 \cdot 10^{14}$	0.141	0.002	3.81
$3 \cdot 10^{15}$	0.791	0.016	0.27
$5 \cdot 10^{15}$	1.454	0.044	0.10
$1 \cdot 10^{16}$	2.189	0.072	0.10
$2 \cdot 10^{16}$	3.986	0.166	0.06

5.3.3 MuPix8/ATLASPix1

MuPix8/ATLASPix1 (see figure 5.18a) is a device shared between two large chips MuPix8 [3] and ATLASPix1 [4]. These were the first large HV-CMOS prototypes for the Mu3e and ATLAS experiments respectively. The chip was fabricated in an engineering run in 2016 in the $0.18 \mu\text{m}$ HV-CMOS from ams AG. The samples measure $23 \text{mm} \times 23 \text{mm}$ and samples were produced in different substrate resistivities 20, 50–100, 100–400, and 600–1100 Ωcm [31]. The left side of the chip (orange in figure 5.18a) consists of a single large matrix of MuPix pixels, and the right side (blue-green) consists of three large matrices of ATLASPix pixels. At the top of the chip are a range of test structures, including one for e-TCT measurements. This is the focus of this study.

This test structure is shown in figure 5.18b, which is highlighted in blue in figure 5.18a. The structure is similar to the structure studied in the last section. It is a 3×3 matrix of passive however, pixels measure $125 \mu\text{m} \times 33 \mu\text{m}$ each. These pixels are smaller than the pixels in the last section, but are designed to still be compatible with the FE-I4, where six pixels arranged in a 2×3 pattern correspond to two FE-I4 cells in a column. Like the structure in the last section however, this structure also provides two readout channels. One to access the central pixel (highlighted in green in figure 5.18b), and the other to access the outer eight pixels, which are shorted together.

A cross-section diagram of one pixel can be seen in figure 5.19a. Pixels are designed in a similar manner to pixels in the previous section. The substrate is p-type and is biased to high negative voltage using the p+, p-well (p+/PTUB) stacks on the outer edges of the pixels. The three deep n-wells (DNTUBs) again, create three reverse biased diodes connected in parallel which form a single pixel. The depletion region grows downwards into the substrate which forms the sensitive volume. Pixels in this test structure are passive, however in the large matrices, PMOS electronics are implemented in n-wells (NTUBs) and NMOS electronics are implemented in p-wells (PTUBs), these wells are included in these pixels for parasitic

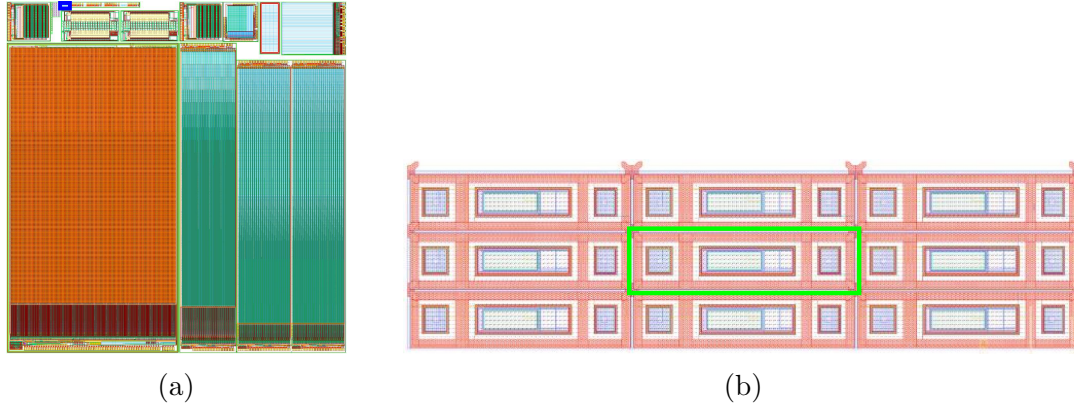


Figure 5.18: (a) Image of the MuPix8/ATLASPix1 chip. The test structure used in these measurements is highlighted in blue at the top (b) Test structure used in e-TCT measurements. The central pixel is highlighted in green.

capacitance studies, something that is not covered here.

5.3.3.1 Samples

Two different sample types were studied in this work from two different wafers. Samples from the first wafer (W1) have a substrate resistivity of $50\text{--}100\ \Omega \cdot \text{cm}$. Samples from the second wafer (W2) have a substrate resistivity of $100\text{--}400\ \Omega \cdot \text{cm}$. Both wafers were thinned to $300\ \mu\text{m}$ at Optim Wafer Services [32]. However W2 was further backside processed at IBS in the same manner as the H35DEMO samples in the previous section to allow backside biasing (figure 5.19b).

5.3.3.2 Post-fabrication processing

Polishing edges

Small scratches persisted on the edge of the samples after dicing (figure 5.20a). Samples were polished in the same manner as H35DEMO samples. Firstly, the edge closest to the test structure (the top edge according to figure 5.18a) was polished with $3\ \mu\text{m}$ lapping sheet (see figure 5.20b). Then to remove finer defects, the same edge was polished with $1/10\ \mu\text{m}$ grade diamond paste (see figure 5.20c).

Irradiation campaign

These samples were also irradiated with neutrons at the TRIGA reactor at JSI. Samples from W1 were irradiated to 1 MeV neutron equivalent fluences between $1 \cdot 10^{14}\ \text{n}_{\text{eq}} \cdot \text{cm}^{-2}$ and $1 \cdot 10^{16}\ \text{n}_{\text{eq}} \cdot \text{cm}^{-2}$. Samples from W2 were irradiated to fluences up to $2 \cdot 10^{16}\ \text{n}_{\text{eq}} \cdot \text{cm}^{-2}$ and measurements also include a non-irradiated sample. Table 5.1 shows the fluences measured for both sample types.

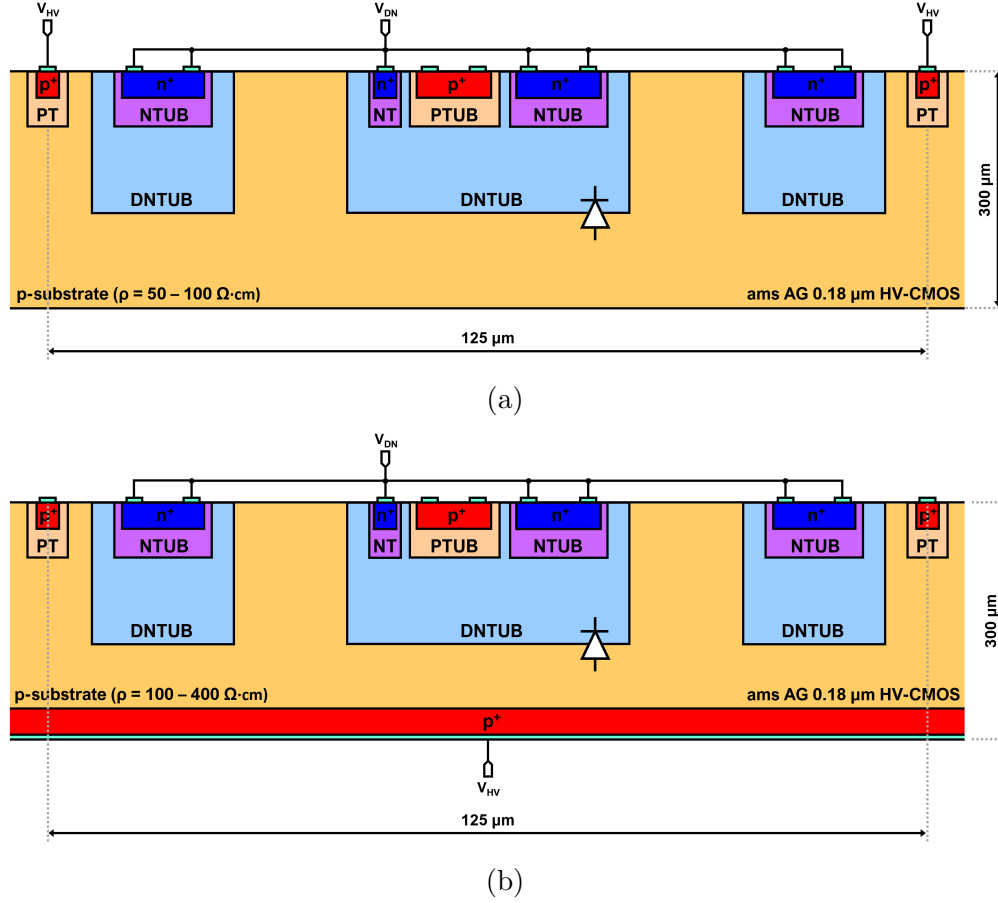


Figure 5.19: (a) Cross-section diagram of a MuPix8/ATLASPix1 test structure pixel. (b) The same cross-section after backside processing. The topside substrate contacts are left floating and the substrate is now biased to high voltage from the backside. Both sample types have been thinned to $300\ \mu\text{m}$.

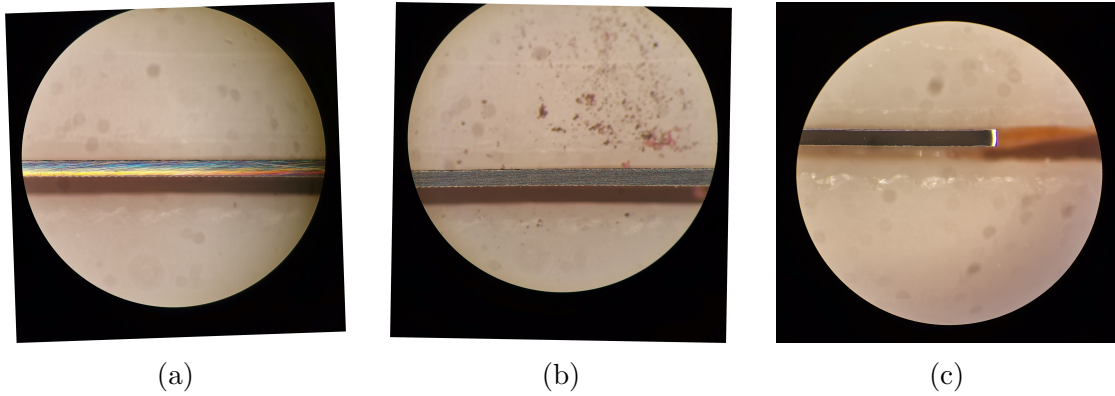


Figure 5.20: (a) Edge of a MuPix8/ATLASPix1 sample after dicing. (b) Same sample after polishing with $3\ \mu\text{m}$ grit lapping sheet. (c) Same sample after polishing with $1/10\ \mu\text{m}$ grade diamond paste.

5.3.3.3 I – V measurements

In the same manner as H35DEMO measurements, samples are cooled to -20°C before taking measurements. These can be seen in figure 5.21a for the W1 samples

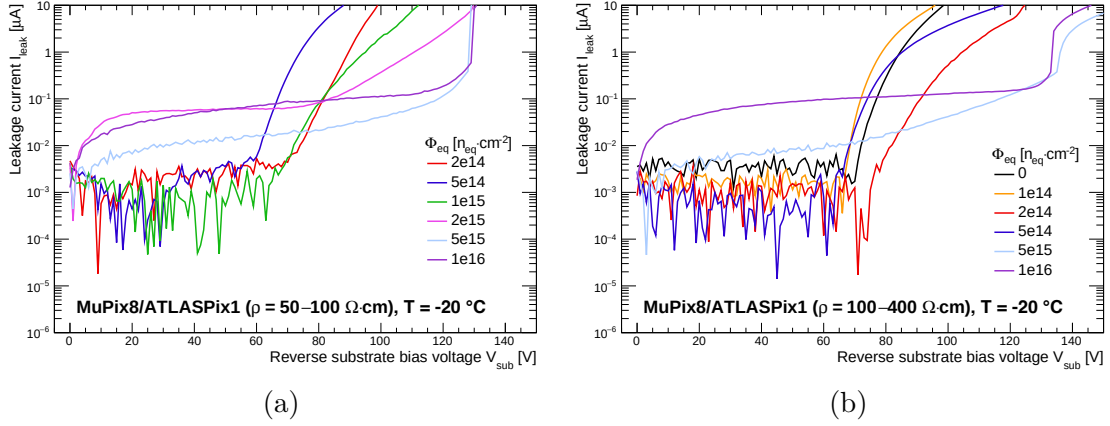


Figure 5.21: (a) I - V measurements of topside biased, irradiated MuPix8/ATLASPix1 samples. (b) I - V measurements of backside biased, irradiated MuPix8/ATLASPix1 samples.

and in figure 5.21b for the W2 samples. For most samples, the leakage current is too low to measure accurately with the equipment. The exception are samples irradiated to high fluence because leakage current increases which is expected for irradiated samples. For the low fluence samples, reverse breakdown occurs when $V_{\text{sub}} \approx -60$ V, which is the maximum voltage samples were biased to in e-TCT measurements. Higher fluence samples exhibit a softer breakdown, which approximately increases with fluence. Therefore these samples were biased to higher voltages in measurements. This effect was also seen in measurements of H35DEMO samples in the previous section.

5.3.3.4 E-TCT Measurements

The same setup that was used for the H35DEMO measurements was also used for MuPix8/ATLASPix1 samples. The only difference between the measurements is the position of the samples with respect to the system. This can be seen in figure 5.22. In figure 5.22a, a diagram comparing the top-down perspectives of an H35DEMO sample on a PCB and a MuPix8/ATLASPix1 sample on a PCB shows the difference in the distance to the laser (y direction). Figure 5.22b shows the same comparison but from the side. It shows the same difference in distance to the laser, but also demonstrates that MuPix8/ATLASPix1 samples are slightly thicker, and therefore the pixels are located at a slightly higher elevation z .

Focus finding in x

As can also be seen in the diagram in figure 5.22a, the gap in the PCB marks the approximate location of the test structure. This is at the same location in both PCBs. Therefore a similar x range as in H35DEMO measurements in order to locate

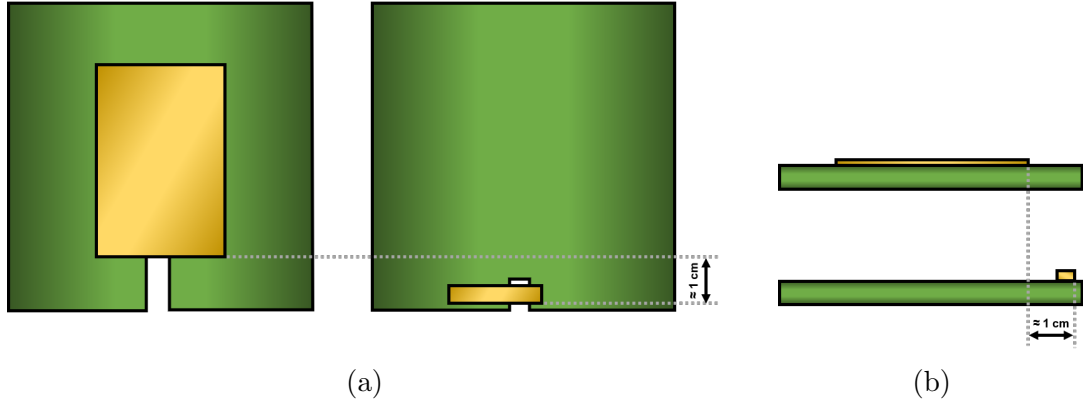


Figure 5.22: (a) Diagram of the top view of an H35DEMO sample on its PCB (left) and a MuPix8/ATLASPix1 on its PCB (right). MuPix8/ATLASPix1 samples are approximately 1 cm closer to the laser than H35DEMO samples (b) Diagram of the side view of samples on the PCBs. MuPix8/ATLASPix1 samples are thicker than H35DEMO samples.

the pixel. Since MuPix8/ATLASPix1 samples are also thicker, a z was assumed to have increased. It can also be seen that there is approximately 1 cm difference in y between sample types. y was therefore fixed to a value approximately $10,000 \mu\text{m}$ less than in H35DEMO measurements. Since samples have low resistivity, it was assumed the depletion region would be smaller and V_{sub} was fixed to just lower than V_{BD} in order to have as large a depletion region as possible and make the pixel easier to find.

The x - z scan of a topside biased $50\text{--}100 \Omega \cdot \text{cm}$ sample, irradiated to $2 \cdot 10^{14} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$ can be seen in figure 5.23a. The sample was scanned in the x and z directions at $5 \mu\text{m}$ steps. Pixels in the test structure under study are $125 \mu\text{m}$ wide and the charge collected by the depletion region of the central pixel of the test structure can be seen between $x = 30085 \mu\text{m}$ and $x = 30210 \mu\text{m}$. The location of the topside of the sample can be determined to be at a depth of approximately $z = 19910 \mu\text{m}$ where charge collection begins. The depletion region extends to a depth of approximately $z = 19895 \mu\text{m}$. This means that the substrate is depleted to a depth of $15 \mu\text{m}$ at $V_{\text{sub}} = -60 \text{ V}$. The centre of the pixel was extracted by eye from this image $x_0 = (30085 \mu\text{m} + 30210 \mu\text{m})/2 = 30147.5 \mu\text{m}$ and this was used in the next measurement to focus the laser. A waveform integration time of 10 ns was used which can be seen in figure 5.23b.

Focus finding in y

The next step was to determine the precise position in y to focus the laser. The x position and substrate bias voltage are kept constant and y and z were varied to produce figure 5.24a. The sample was scanned in the z direction over a range

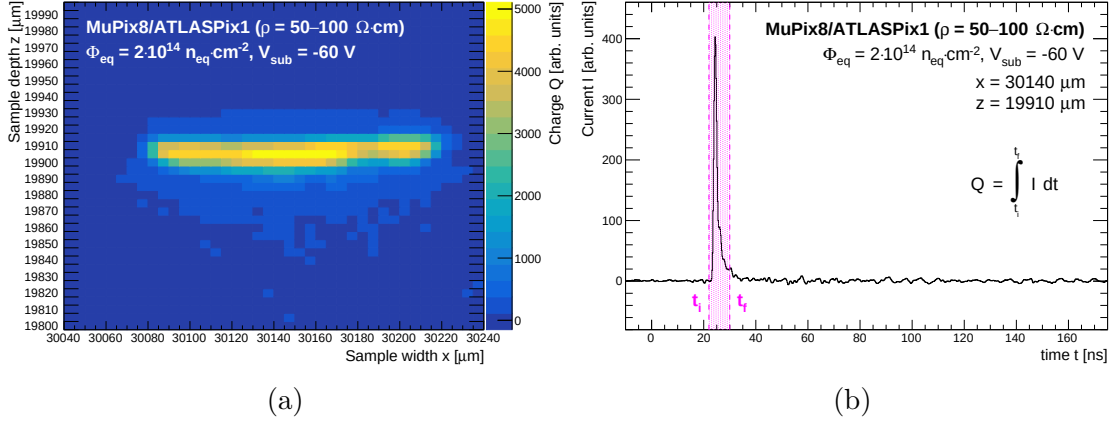


Figure 5.23: (a) x - z scan of a topside biased, MuPix8/ATLASPix1 sample irradiated to $2 \cdot 10^{14} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$. (b) Waveform recorded at laser position $x = 30140 \mu\text{m}$, $y = 28200 \mu\text{m}$, $z = 19910 \mu\text{m}$, $V_{\text{sub}} = -60 \text{ V}$. This is integrated between t_i and t_f to calculate charge collected Q .

of $200 \mu\text{m}$ in $5 \mu\text{m}$ steps, and in the y direction over a range of 2 mm in $20 \mu\text{m}$. This is because pixels are only $33 \mu\text{m}$ in the y direction, it is therefore particularly important to ensure the laser is focussed correctly. The laser is focussed underneath the central pixel when the signal is the highest and the change in charge collection with a decrease in z is the greatest. This can be seen in figure 5.24a at $y \approx 28200 \mu\text{m}$. A sample of the projections are chosen near this value, between $y = 28060 \mu\text{m}$ and $y = 28380 \mu\text{m}$ and an error function (equation 5.2) is fit to the topside of the charge collection profile $z_0 = 19910 \mu\text{m}$ (see figure 5.24b). Q_{max} is initially set to the maximum charge collected and the minimum of the fit range is set to the left edge of the bin with the maximum charge. The fit range must be specified in order to properly fit the right side of the charge collection profile without taking into account the left edge of the charge collection profile, which is due to the boundary of the depletion region in the sensor bulk. The whole fit is shown with the dotted line and the fit range is the solid line. Charge collection outside the sample area ($z > 19910 \mu\text{m}$) is assumed to be 0 although there is some noise. w is extracted from this fit and plotted against y of the sampled charge collection profiles. This can be seen in figure 5.24c. This data is then fit with equation 5.3. y_0 is extracted from the fit and fixed as the laser position in the next measurement.

Calculating the size of the depletion region

With the x and y positions of the laser fixed to x_0 and y_0 respectively, the sample is scanned in the z direction in $1 \mu\text{m}$ steps at voltages ranging from just below V_{BD} to 0 V in 2 V steps. At each step a waveform is recorded and integrated to calculate charge (figure 5.25a). The resulting $z - V_{\text{sub}}$ scan can be seen in figure 5.25b. All above steps are repeated for each fluence, and for all samples from W2. The results

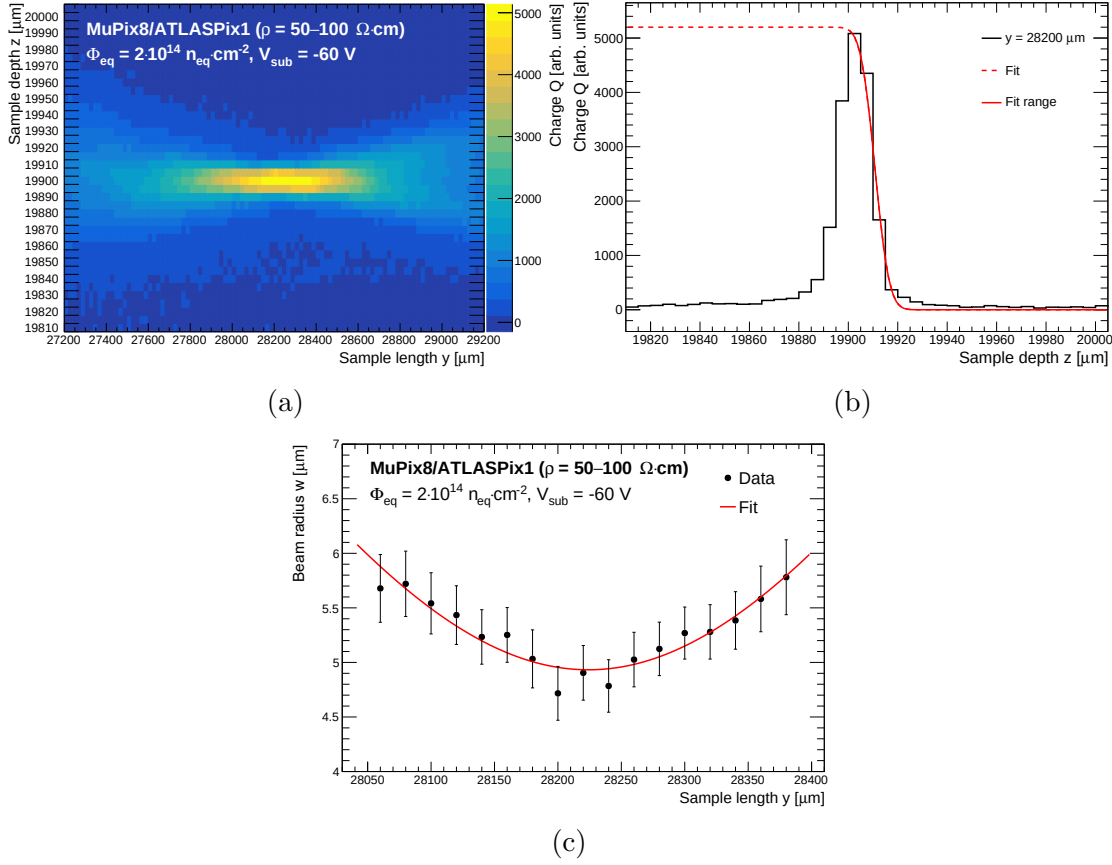


Figure 5.24: (a) Scan in y and z of a MuPix8/ATLASPix1 sample irradiated to $2 \cdot 10^{14} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$. (b) The width of the error function is the approximate beam radius. (c) Width of error functions at different y . The lowest value of w is the beam waist.

are shown in figures 5.26 and 5.27.

The projections of figure 5.25b can be seen in figure 5.28a. For each voltage taken for each sample, the depletion depth is estimated from the FWHM of the charge collection profiles (equation 5.6), shown by the black arrow in figure 5.28. However in this case, k_1 and k_2 are calculated using simple linear interpolation between points (z_1, Q_1) and (z_2, Q_2) , and (z_3, Q_3) and (z_4, Q_4) (see figure 5.28).

$$\begin{aligned} k_1 &= \frac{z_2 - z_1}{Q_2 - Q_1} \cdot \left(\frac{Q_{\text{max}}}{2} - Q_1 \right) + Q_1 \\ k_2 &= \frac{z_4 - z_3}{Q_4 - Q_3} \cdot \left(\frac{Q_{\text{max}}}{2} - Q_3 \right) + Q_3 \end{aligned} \quad (5.9)$$

where Q_{max} is the maximum charge collected, extracted from the bin containing the highest value, shown as a red dashed line in the figure. z_2 is the first bin above $Q_{\text{max}}/2$, and $z_1 = z_2 - \Delta z$. z_3 is the last bin above $Q_{\text{max}}/2$, and $z_4 = z_3 + \Delta z$. k_2 corresponds to the topside of the sample and k_1 is the boundary of the depletion region in the substrate. The FWHM calculated is plotted against V_{sub} . The results

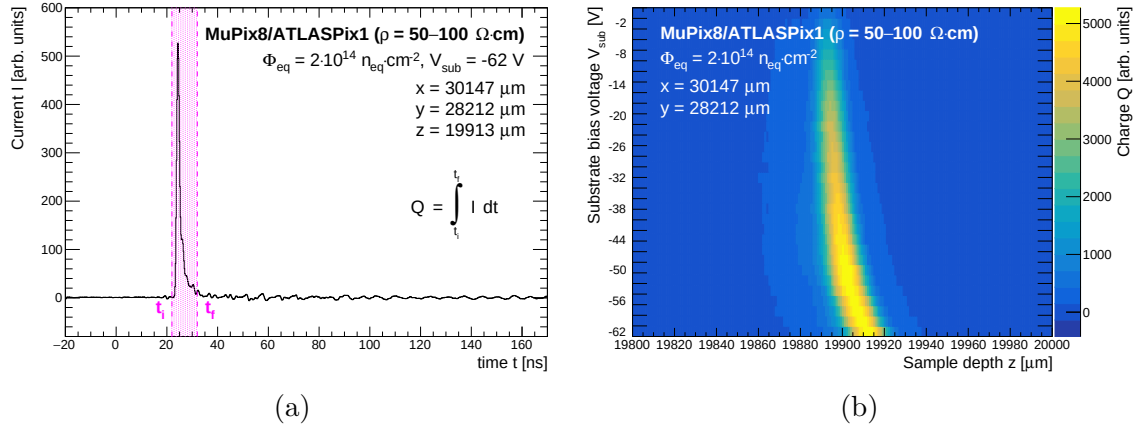


Figure 5.25: (a) Example of a waveform and integration window from the $z - V_{\text{sub}}$ scan of a topside biased MuPix8/ATLASPix1 sample irradiated to $2 \cdot 10^{14} \text{ neq} \cdot \text{cm}^{-2}$. x and y are fixed to x_0 and y_0 which are determined using $x - z$ and $y - z$ scans respectively. (b) Scan in z and V_{sub} for the same sample.

Table 5.3: Effective doping concentrations N_{eff} extracted from fits to measurements of depletion depth for MuPix8/AtLASPix1 W1 (50–100 Ωcm) samples irradiated to different fluences.

$\Phi_{\text{eq}} [\text{neq} \cdot \text{cm}^{-2}]$	$N_{\text{eff}} [10^{14} \text{ cm}^{-3}]$	$\Delta N_{\text{eff}} [10^{14} \text{ cm}^{-3}]$	χ^2/NDF
$2 \cdot 10^{14}$	5.589	2.155	0.09
$5 \cdot 10^{14}$	4.616	2.293	0.46
$1 \cdot 10^{15}$	1.845	0.006	5.26
$2 \cdot 10^{15}$	0.719	0.025	10.17
$5 \cdot 10^{15}$	2.192	0.194	3.15
$1 \cdot 10^{16}$	6.217	0.971	0.89

can be seen in figures 5.29a and 5.30a. Each set of data is fit with equation 5.7, N_{eff} is extracted, and plot against Φ_{eq} . The values of N_{eff} , the errors ΔN_{eff} , and the reduced χ^2 can be seen in tables 5.3 and 5.4. The results can be seen in figures 5.29b and 5.30b. The data are fit with equation 5.8. The extracted values can be seen in table 5.5.

5.3.4 Summary and conclusions

One high resistivity (600–2000 Ω·cm) wafer of H35DEMO samples and one medium resistivity (100–400 Ω·cm) wafer of MuPix8/ATLASPix1 samples were backside processed to enable backside biasing. Backside processing involved thinning of the wafer, p+ beamline implantation, rapid thermal annealing, and metallisation. One low resistivity (50–100 Ω·cm) wafer containing MuPix8/ATLASPix1 samples was also studied but was not backside processed. Individual samples from all wafers were irradiated to different fluences up to and including $2 \cdot 10^{16} \text{ neq} \cdot \text{cm}^{-2}$ to study the effect of radiation damage on I – V characteristics and charge collection properties.

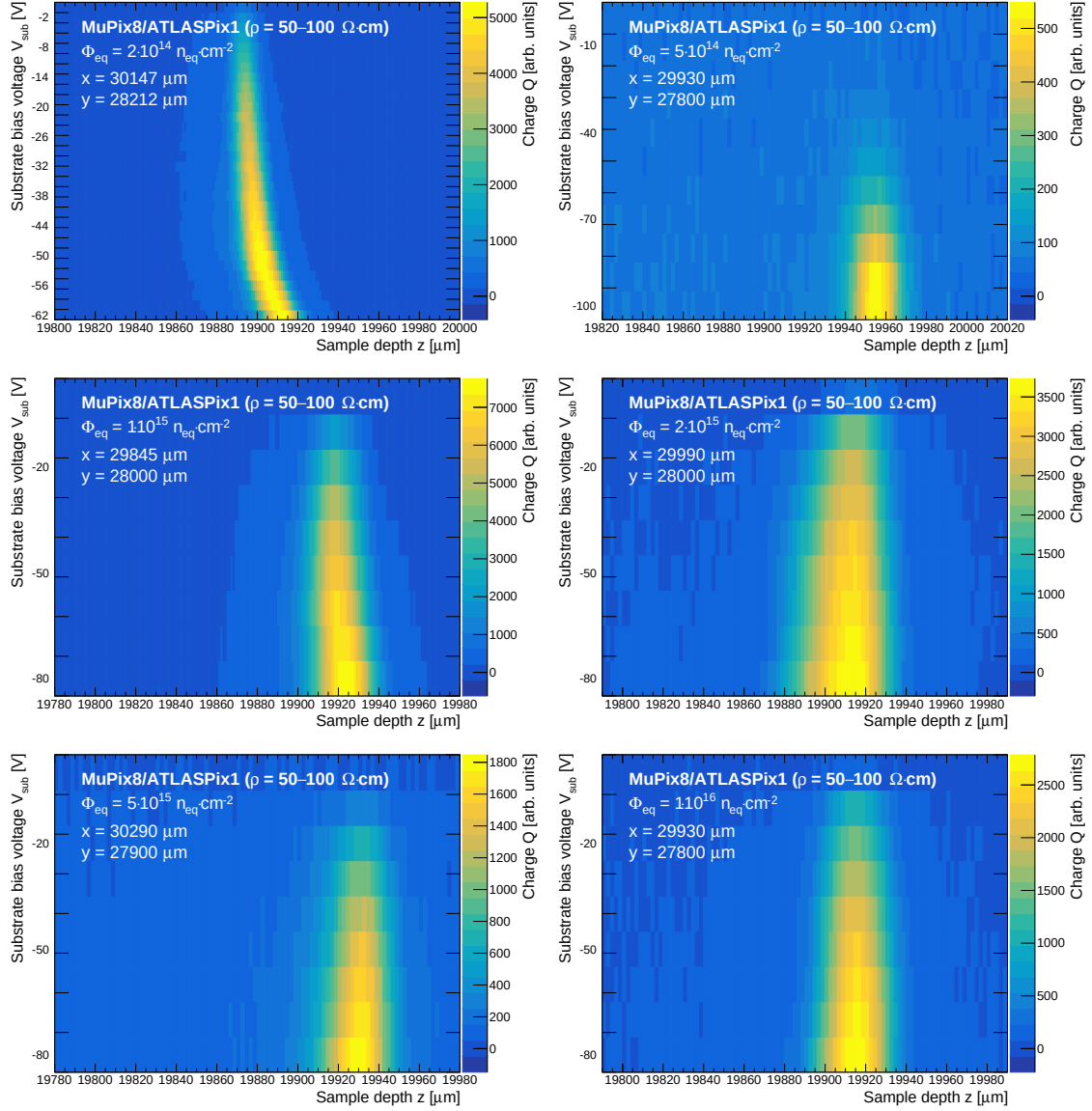


Figure 5.26: Scans in z and V_{sub} for low resistivity, thinned, topside biased, irradiated, MuPix8/ATLASPix1 samples.

Table 5.4: Effective doping concentrations N_{eff} extracted from fits to measurements of depletion depth for MuPix8/AtLASPix1 W2 (100–400 Ωcm) samples irradiated to different fluences.

$\Phi_{\text{eq}} [\text{n}_{\text{eq}} \cdot \text{cm}^{-2}]$	$N_{\text{eff}} [10^{14} \text{cm}^{-3}]$	$\Delta N_{\text{eff}} [10^{14} \text{cm}^{-3}]$	χ^2/NDF
0	0.791	0.055	0.33
$1 \cdot 10^{14}$	0.701	0.142	1.73
$2 \cdot 10^{14}$	0.540	0.066	0.07
$5 \cdot 10^{14}$	0.852	0.249	0.25
$1 \cdot 10^{15}$	0.751	0.017	0.17
$5 \cdot 10^{15}$	2.765	0.296	0.37
$1 \cdot 10^{16}$	4.937	2.043	0.47
$2 \cdot 10^{16}$	9.929	4.349	0.30

5.3. MEASUREMENTS OF BACKSIDE PROCESSED HV-CMOS DETECTORS

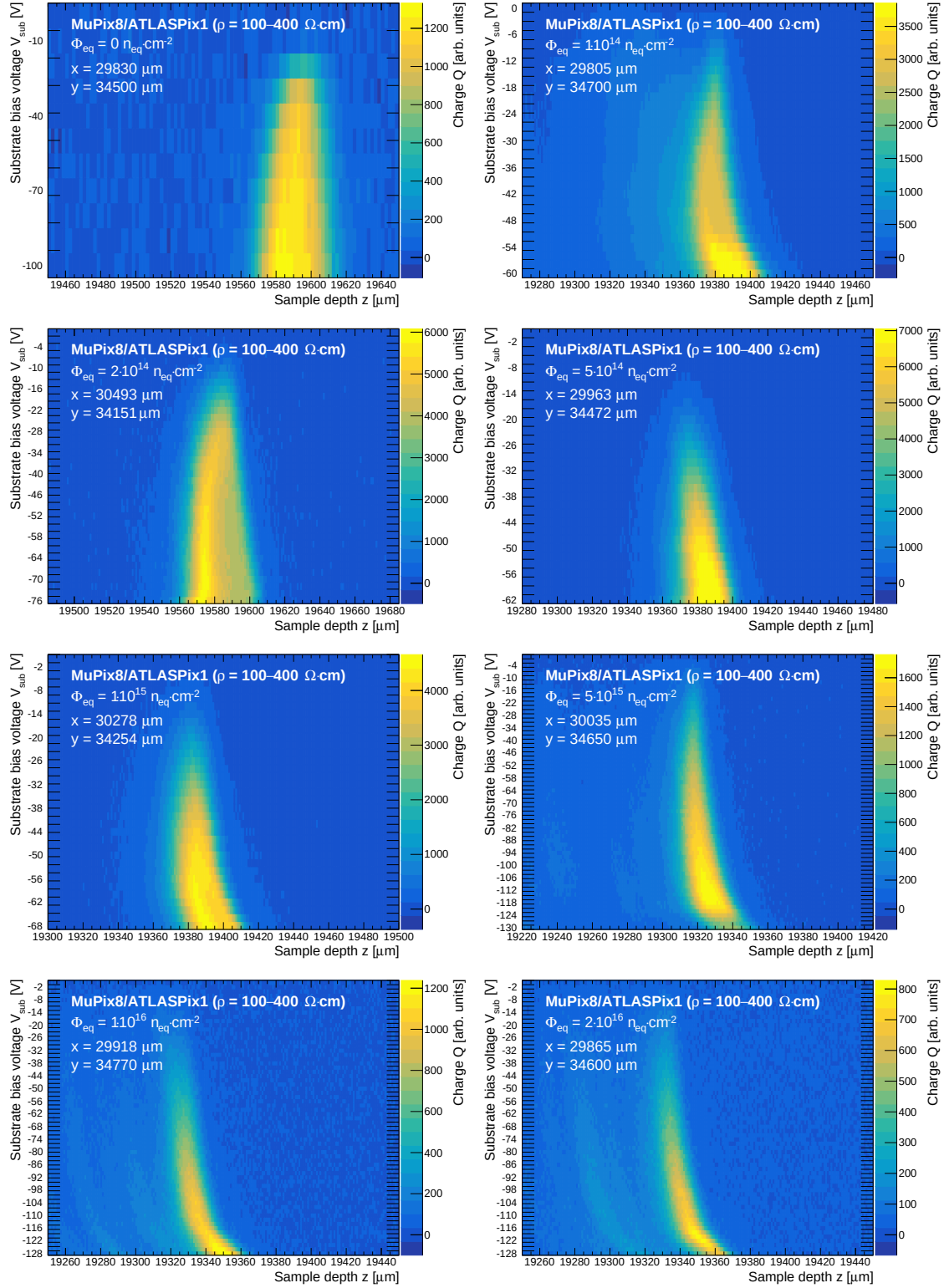


Figure 5.27: Scans in z and V_{sub} for medium resistivity, thinned, backside biased, irradiated, MuPix8/ATLASPix1 samples.

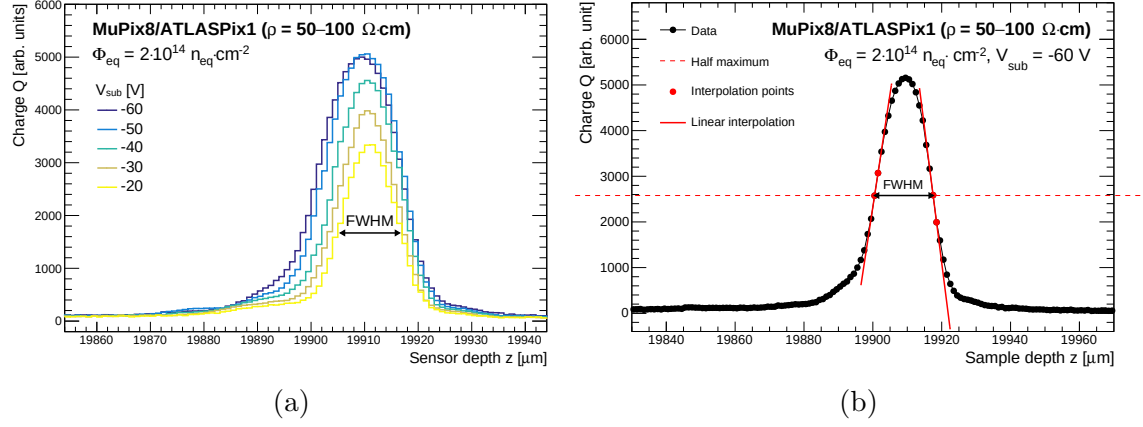


Figure 5.28: (a) Charge collection profiles for different values of substrate bias voltage V_{sub} for a high resistivity, thinned, backside biased, non-irradiated, H35DEMO sample. (b) Equation 5.5 fit (in red) to the charge collection profile at $V_{\text{sub}} = -20$ V. The components of equation 5.5 are shown in dashed lines. The approximation of the depletion depth W_D (FWHM) is shown with a black arrow.

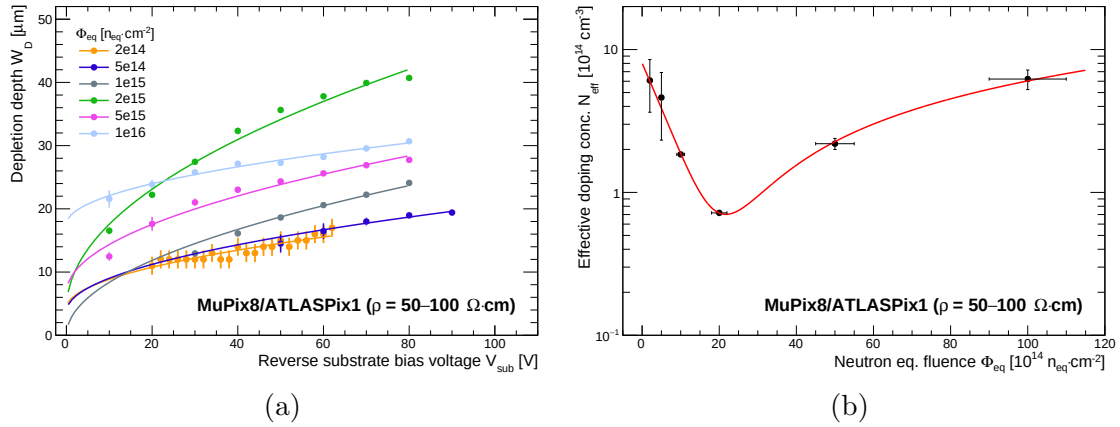


Figure 5.29: (a) Depletion depth W_D as a function of substrate bias voltage V_{sub} for MuPix8/ATLASPix1 samples irradiated up to neutron equivalent fluence $\Phi_{\text{eq}} = 1 \cdot 10^{16}$ n_{eq}·cm⁻². (b) Evolution of effective doping concentration N_{eff} with Φ_{eq} .

I – V characteristics show a general increase in leakage current with neutron equivalent fluence. This is expected due to the introduction of defects into the silicon lattice and therefore additional energy levels within the silicon bandgap which increases generation of charge carriers. Softer breakdowns were also exhibited for those samples irradiated to the highest fluences. Both of these phenomena can be reproduced using TCAD simulations (see chapter 3). The breakdown voltages of the backside biased, non-irradiated H35DEMO samples presented here are similar to the topside biased samples presented in reference [22]. This is an example demonstrating that backside biasing H35DEMO samples and leaving topside contacts floating is not enough to increase the breakdown voltage, further suggesting that the presence of the p-type wells is problematic with regards to breakdown voltage.

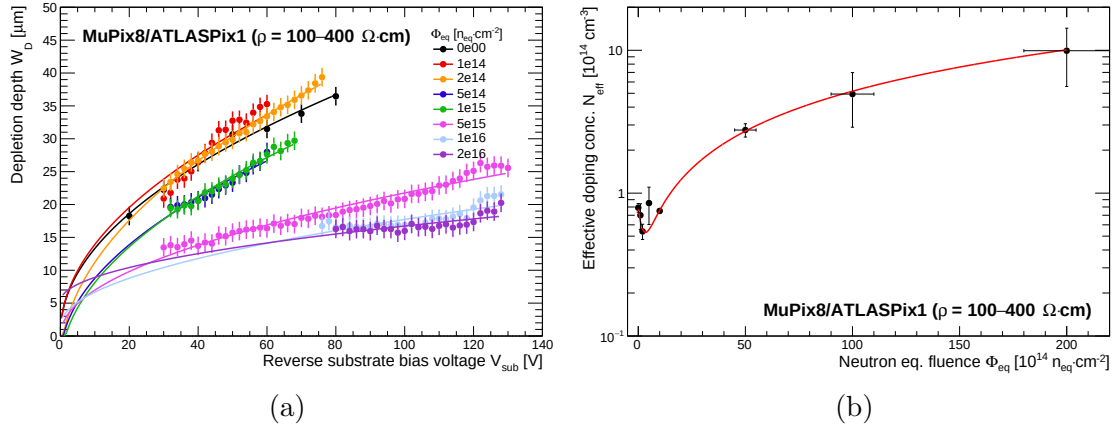


Figure 5.30: (a) Depletion depth W_D as a function of substrate bias voltage V_{sub} for backside biased, $100\text{--}400 \Omega \cdot \text{cm}$ MuPix8/ATLASPix1 samples irradiated up to neutron equivalent fluence $\Phi_{\text{eq}} = 2 \cdot 10^{16} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$. (b) Evolution of effective doping concentration N_{eff} with Φ_{eq} .

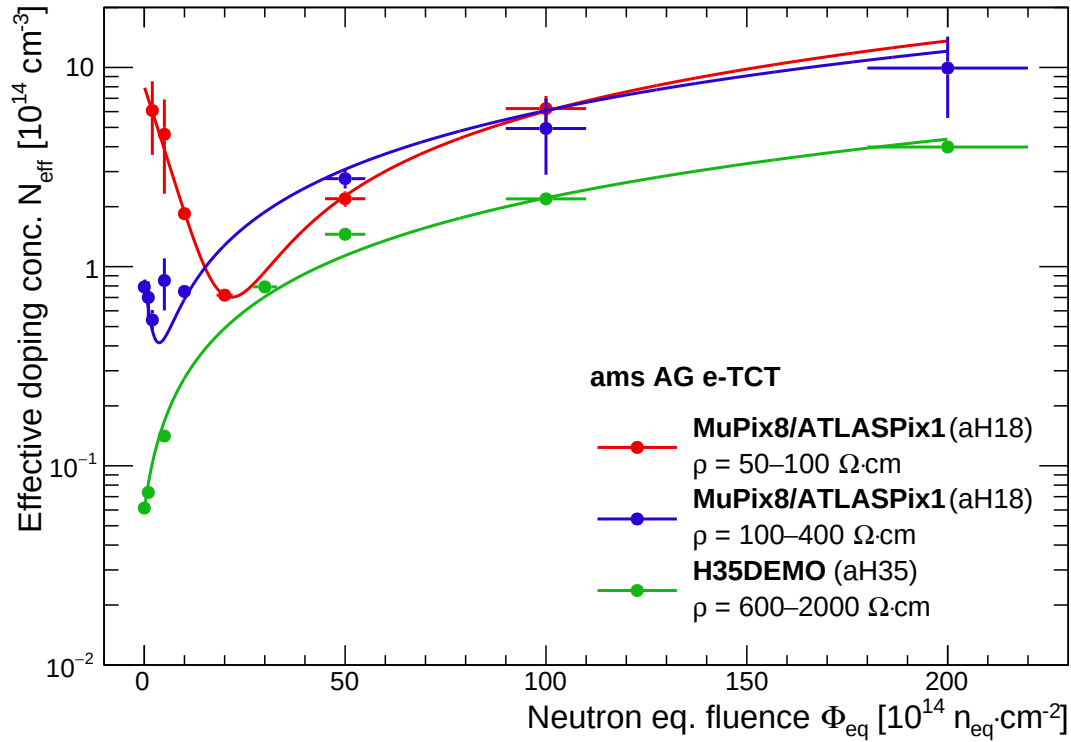


Figure 5.31: Figures 5.17b, 5.29b, and 5.30b collated.

Table 5.5: Parameters extracted from equation 5.8 fit to data in figure 5.17b. ρ is converted from $N_{\text{eff}0}$ using reference [12].

Parameter	Unit	MuPix8/ ATLASPix1 W1	MuPix8/ ATLASPix1 W2	H35DEMO
$N_{\text{eff}0}$	10^{14} cm^{-3}	8.020 ± 3.148	0.792 ± 0.055	0.060 ± 0.001
N_c	10^{14} cm^{-3}	9.552 ± 2.445	0.529 ± 0.118	-
c	10^{-14} cm^2	0.128 ± 0.051	0.485 ± 0.228	-
g_c	cm^{-1}	0.076 ± 0.018	0.049 ± 0.001	0.022 ± 0.001
ρ	$\Omega \cdot \text{cm}$	16.81 ± 6.60	168.0 ± 11.7	2212 ± 35
$N_c/N_{\text{eff}0}$		1.191 ± 0.559	0.668 ± 0.156	-
χ^2/NDF		0.09	0.44	5.54

E-TCT measurements were used to study how the depth of the depleted volume changes with substrate bias voltage, substrate resistivity, and irradiation damage. This data was used to extract the effective doping concentration of the substrate, which was shown to change depending on the neutron equivalent fluence. For the high resistivity backside biased H35DEMO samples, the effective doping concentration was shown to increase approximately linearly with neutron equivalent fluence, corresponding to a stable damage introduction rate of $0.022 \pm 0.001 \text{ cm}^{-1}$. This is slightly larger than the typical value of 0.020 cm^{-1} reported in literature [25], but consistent with high resistivity devices in other technologies [8, 30]. A decrease in effective doping concentration at low fluences corresponding to the removal of acceptor-like states seen in other literature was not observed. This is due to the initial high resistivity p-type substrate which contains a low concentration of acceptor dopants. Acceptor removal is therefore expected to be completed at low fluences ($10^{13} \text{ n}_{\text{eq}} \cdot \text{cm}^{-2}$) which were not measured in this study. The initial substrate resistivity of the device can be estimated from $N_{\text{eff}0}$ extracted from the fit and calculated using reference [12]. In this case $\rho = 2212 \pm 35 \Omega \cdot \text{cm}$ which is slightly higher than the range given by the foundry, but the measurement is consistent with other studies of this device [20, 21].

For the medium resistivity backside biased MuPix8/ATLASPix1 samples, an exponential decrease in the effective doping concentration is observed for low fluences which is due to the acceptor removal effect. This effect is observable in these samples due to their higher initial acceptor doping concentration. Acceptor removal is observed to be incomplete as parameter $N_c/N_{\text{eff}0} < 1$. The acceptor removal constant $c \approx 0.5 \cdot 10^{-14} \text{ cm}^2$ is consistent with measurements of different samples also produced in technologies from ams AG, $c = 0.57 \cdot 10^{-14} \text{ cm}^2$ for a $10 \Omega \cdot \text{cm}$ device, and $c = 0.36 \cdot 10^{-14} \text{ cm}^2$ for a $20 \Omega \cdot \text{cm}$ device (no errors are given). [7]. As fluence increases, the introduction of stable acceptor-like states then dominates, increasing linearly at a rate of $0.049 \pm 0.001 \text{ cm}^{-1}$ which was left as a free parameter.

This is larger than the value seen in reference [7], where the parameter is fixed to $g_c = 0.02, \text{cm}^{-1}$, and similar measurements in reference [9] in which g_c is also fixed to 0.02cm^{-1} based on conclusions drawn in reference [25]. In that study, measurements of oxygen-rich, high resistivity ($> 1000 \Omega \cdot \text{cm}$) wafers shown that $g_c = 0.02 \text{cm}^{-1}$ and does not depend on the oxygen concentration. However, measurements of similar resistivity devices to this study in a similar technology irradiated with neutrons also report a larger value of $g_c = 0.03 \text{cm}^{-1}$ [20]. The extracted substrate resistivity $168 \pm 11.7 \Omega\text{cm}$ is within the range quoted by the foundry.

Finally, the low resistivity topside biased MuPix8/ATLASPix1 samples show a similar behaviour to the medium resistivity samples. Acceptor removal is observed to be complete as $N_c/N_{\text{eff}_0} \approx 1$. The value of c is lower than values of similar resistivity devices in similar technologies in references [7] and [20], but similar to the value of a chip with a similar substrate resistivity produced in a similar technology in reference [9] and follows the trend of other devices presented in that study. g_c is again larger than the value of 0.02cm^{-1} but is within variations seen in reference [20] when left as a free parameter in the function fitting procedure. The value of the resistivity extracted from the fit $16.81 \pm 6.60 \Omega \cdot \text{cm}$ lies outside the range quoted by the foundry however, no measurements of a non-irradiated device were presented here and low fluence, low resistivity samples exhibit depletion depths of a similar size to the laser beam waist thus giving large errors of extracted N_{eff} making it difficult to fit for the y -intercept $N_{\text{eff}_0} \approx 1$.

Regarding the backside processing, the results of measurements of backside processed wafers demonstrate that backside biased detectors processed with the technique from IBS function well. The peak in charge collection at the backside of MuPix8/ATLASPix1 samples was observed in the laboratory, but not seen in measurements here as the substrate is $300 \mu\text{m}$ thick which is outside the range of the scans presented. However, it is present in measurements of all H35DEMO samples here, which were thinned to $100 \mu\text{m}$. Studies of the cause and effects of this will be interesting for future detectors backside processed at IBS where high resistivity substrates and high voltage will be used and full depletion is therefore expected. As mentioned in reference [6] the peak is due to the low temperature of the annealing step where the boron is not fully activated. The implantation and annealing steps will be studied with TCAD simulations in the next section along with another backside processing method available from the same vendor.

5.4 Simulations of backside processing

Both the H35DEMO and MuPix8/ATLASPix1 sample types measured in the previous section were backside processed at IBS. Some details about the backside pro-

cessing were given in the previous section but it will be covered in more detail in this section. The wafer was thinned using so-called TAIKO thinning [33] to $100\text{ }\mu\text{m}$, implanted with boron using beamline implantation (BI), thermally annealed using rapid thermal annealing (RTA) at a temperature of 450°C for 30 seconds, and then metallised with titanium and aluminium to a thickness of 1022 nm . However, as was shown in measurements of the H35DEMO, this backside processing method showed a peak in charge collection at the p+ implant–p-substrate interface. This was due to the low annealing temperature which did not activate all of the boron, nor recover the lattice damage, creating a gradient of space charge and therefore an electric field, as described in reference [6]. However, simply increasing the annealing temperature is not necessarily an option as high temperatures can affect the dopants on the topside which can affect transistor properties, for example.

A new type of backside processing available from IBS was therefore also investigated. This second backside processing method also consists of thinning and metallisation, but the dopant is implanted using plasma immersion ion implantation (PIII) and then annealed using laser annealing (LA). PIII creates very shallow, high concentration implants as opposed to the relatively deep, low concentration implants resulting from BI. The benefit of this is that the implant can be annealed with LA. In LA, the implanted area is heated with a laser beam, which localises the high temperatures necessary to properly activate dopants to the area the beam is focussed. This is beneficial with respect to the more ‘global’ RTA, as it should not affect the properties of the implants on the topside of the wafer.

To investigate the effectiveness of these two methods for backside processing of future designs, the implantation and annealing steps were recreated using the Sentaurus Process TCAD tool from Synopsys. Once the vertical doping profiles from these methods had been properly simulated, they were then imported into Sentaurus Structure Editor. These vertical doping profiles were then combined with simulated doping profiles presented in chapter 3 to make the pixels. SDE was used in order to simulate larger structures, such as individual pixels in a large substrate to save on simulation time. Finally, reverse I – V characteristics were simulated using Sentaurus Device in order to compare the backside processing methods.

5.4.1 Beamline implantation and rapid thermal annealing

Two alternative backside processing methods, available from IBS, were investigated. The first type of backside processing investigated was BI and RTA. The same type used on H35DEMO and MuPix8/ATLASPix1 samples described in the previous section.

A 1D region of silicon was defined with a length of $5\text{ }\mu\text{m}$. This length was used

to properly characterise the vertical doping profile while keeping simulation time to a minimum. A simple meshing scheme was employed with 1 nm spacing close to the implant surface, and node spacing increasing to 10 nm at a $1\text{ }\mu\text{m}$ depth. No doping was applied to the silicon substrate in this simulation so that the doping profile could be applied to silicon with any constant doping field.

The p-type implant was introduced into the substrate using Sentaurus MC implantation, with the number of pseudoparticles set to 100,000. The other inputs for the implantation simulation were set to those that were used on the wafers in the measurements in the previous section. These were provided by IBS. Boron was used as the doping species, implant energy was set to 50 keV, and a beam dose of $5 \cdot 10^{14} \text{ ions} \cdot \text{cm}^{-2}$ was used. As it is also necessary to specify the wafer tilt and rotation angles and as these were unknown, they were both assumed to be 0° . An annealing step was then applied to the simulation, again using inputs provided by IBS, for 30 seconds at a temperature of 450°C . An image of the results of this simulation in 2D can be seen in figure 5.32a, and a zoom to the implant region can be seen in figure 5.32b where the color of the plot represents active boron concentration. For visual clarity, the width of the 1D simulation was extended to $0.5\text{ }\mu\text{m}$ with a mesh node spacing of 50 nm in the x direction. The 1D doping profile before and after annealing can be seen in 5.32c. It can be seen that by using an annealing temperature of 450°C , not all of the boron is properly activated. This reflects the conclusion in reference [6]. A third example simulation is presented and shows that more boron can be activated by using a higher temperature. Use of higher temperatures on real samples may be unfeasible however, since annealing effects could affect transistors on the topside, for example.

5.4.2 Plasma immersion ion implantation and laser annealing

The second type of backside processing investigated was plasma immersion ion implantation. The implantation is performed by extracting positively charged ions from a plasma with a pulsed negative voltage [34]. A 1D region of silicon of depth $0.5\text{ }\mu\text{m}$ was defined. It is known that the implant depth of plasma implantation is shallower than for beamline implantation. The depth of the silicon can therefore be smaller and therefore the simulation will be faster. To simulate the implantation step the MC plasma implantation module from Sentaurus Process was used. The simulation inputs such as dopant species and implant energy, were provided by IBS. For the dopant species, a BF_3 plasma is used. BF_3 plasma contains different boron ions including BF_2 , BF , and B . Ion abundances used in this study were taken from [35], shown in table 5.6.

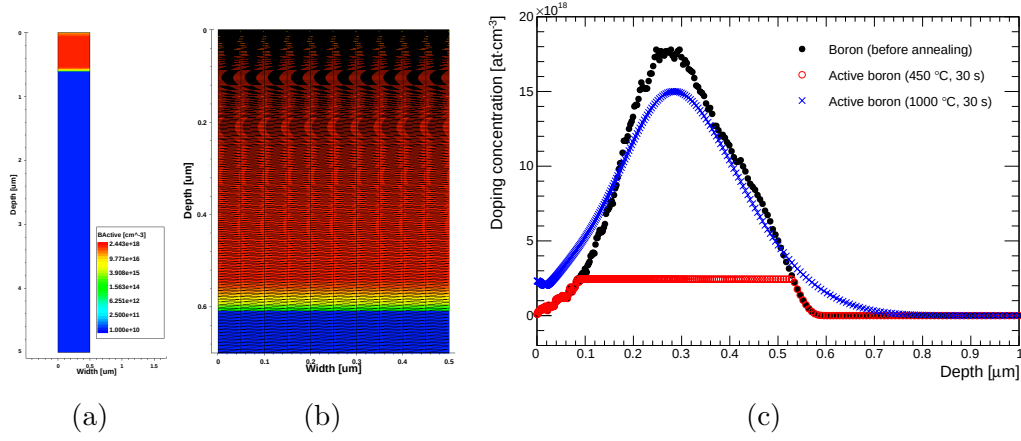


Figure 5.32: (a) Sentaurus Process TCAD simulation of IBS backside p+ implantation and thermal annealing. (b) Zoom of (a) showing the simulation mesh. The colour scale in both plots is active boron concentration (c) 1D simulated doping profile of the backside p+ implantation before (solid markers) and after (empty markers) thermal annealing. Not all of the boron is activated when annealing is performed at 450 °C as was done with measured samples. However, more boron can be activated by using a higher temperature. An example doping profile after annealing at a temperature of 1000 °C can be seen with blue × symbols.

Ion species	Abundance
B	5
BF	15
BF ₂	80
BF ₃	0

Table 5.6: Species abundances extracted from BF₃ plasma [35].

A Sentaurus Process simple source was used, which assumes the different ions extracted from the plasma have the same energy. The energy distribution model that was used was the Burenkov model [36]. The implant energy E_{implant} was calculated from the extraction voltage $V_{\text{extraction}} = 2 \text{ kV}$ provided by IBS using the formula from [34]

$$E_{\text{implant}} = Q_{\text{ion}} \cdot V_{\text{extraction}} \quad (5.10)$$

where Q_{ion} is the charge on the ion in units of elementary charge. The charges of ions extracted from the plasma are assumed to be +1. Therefore $E_{\text{implant}} = 2 \text{ keV}$.

Since it was suspected that RTA would not be sufficient to activate boron in BI let alone PIII, LA was investigated. LA benefits over RTA because the temperature can be localised. This means that a high enough temperature can be used to activate all dopants, and this step is much less likely to affect electronics on the topside of the sample by further annealing implanted wells. The downside with using this method in this case is that samples backside processed with this method have not

been tested in our lab.

To simulate this process step, the flash or laser anneal model in Sentaurus Process [37] was used. According to IBS, the laser is used in melting mode, therefore the melting laser anneal model was switched on. In melting mode, the phase of the silicon must be considered. This is achieved by introducing a phase field variable ϕ to the heat transfer equation [37].

$$\rho c_P \frac{\partial T}{\partial t} = \nabla \cdot (\kappa \nabla T) + G + 30\rho L \phi^2 (1 - \phi)^2 \frac{\partial \phi}{\partial t} \quad (5.11)$$

where T and t are temperature and time. ρ , c_P , and κ are the mass density, specific heat capacity, and conductivity respectively. L is the unit mass latent heat and is phase-dependent. In addition, c_P and κ also vary with phase. Since the only material considered in this simulation is silicon, the default variables are used as they are assumed to be well-known. More information about the phase dependence of equation 5.11 can be found in the user guide. G is the heat generation rate, calculated by

$$G = I_0 \cdot g \quad (5.12)$$

where I_0 is the intensity, calculated using the intensity model for flash annealing and g is the normalized profile calculated using the energy implantation method. The intensity was specified using a Gaussian model [37]

$$I_0 = \frac{\Phi}{\sqrt{2\pi}t_s} \exp\left(-\frac{(t-t_0)^2}{2t_s^2}\right) \quad (5.13)$$

where Φ is the energy dose in $\text{J} \cdot \text{cm}^{-2}$, $t_0 = 3t_s$ and

$$t_s = \frac{t_p}{2\sqrt{2\ln 2}} \quad (5.14)$$

where t_p is the pulse duration in seconds. According to IBS, $\Phi = 550 \text{ mJ} \cdot \text{cm}^{-2}$ and $t_p = 20 \text{ ns}$. The result can be seen in figure 5.33.

The normalized profile g was calculated using the energy implantation method [37]

$$g = \alpha \exp\left(-\int_{l=0}^{l=d} \alpha dl\right) \quad (5.15)$$

where l is the light path, the lateral decay length d was set to the default value and α is the absorption coefficient of the material, which in this case is silicon, and it is also assumed the default value is sufficient. In a similar way to the BI and RTA simulations, an image of a 2D simulation is provided for visual clarity in figure 5.34a and a zoom of the implant region in figure 5.34b where the color of the plots is the

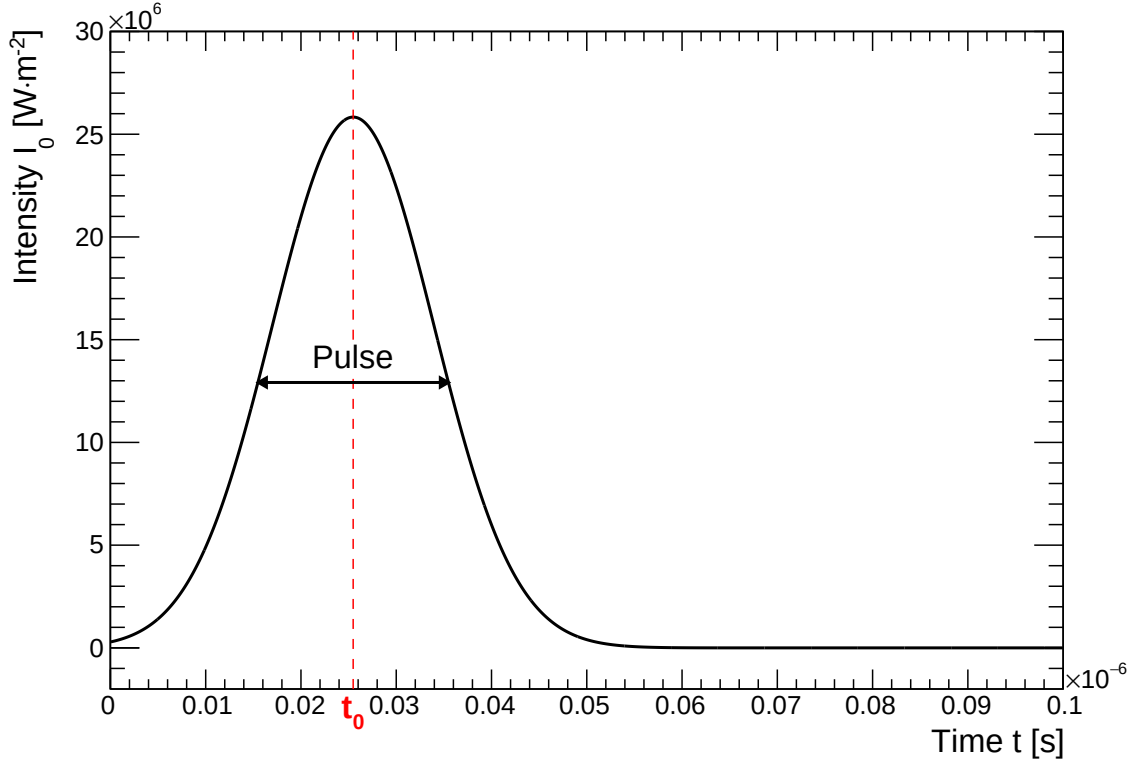


Figure 5.33: Heat intensity with respect to time calculated using the intensity model flash annealing [37] and inputs from IBS.

active boron concentration. The 1D doping profile before and after annealing can be seen in figure 5.34c. Before using the doping profiles in other simulations, the results were validated by comparing the doping profiles with those in literature. The profile before annealing matches well with SIMS measurements of the profile under the same conditions and simulations under similar conditions which are presented in reference [36]. The simulated data after annealing has a much flatter profile. It is difficult to find literature with the exact conditions simulated here, but SIMS data presented in [38] show profiles with a similar flat shape and small peak at the deepest part of the profile.

5.4.3 Simulated I – V characteristics

In order to determine the effectiveness of backside implants as ohmic contacts, a comparison of I – V simulations is presented. As these backside processing methods were investigated for the UKRI-MPW0 prototype, a backside biased pixel in LFoundry 150 nm technology was simulated. Using Sentaurus Structure Editor, a very large 2D region of silicon was defined with depth equal to the estimated thickness of fabricated wafers and large width in order to allow the depletion region to grow. This can be seen in figure 5.35a. The substrate resistivity was set to $1900 \Omega \cdot \text{cm}$ as this is a common value for high resistivity substrates available from LFoundry.

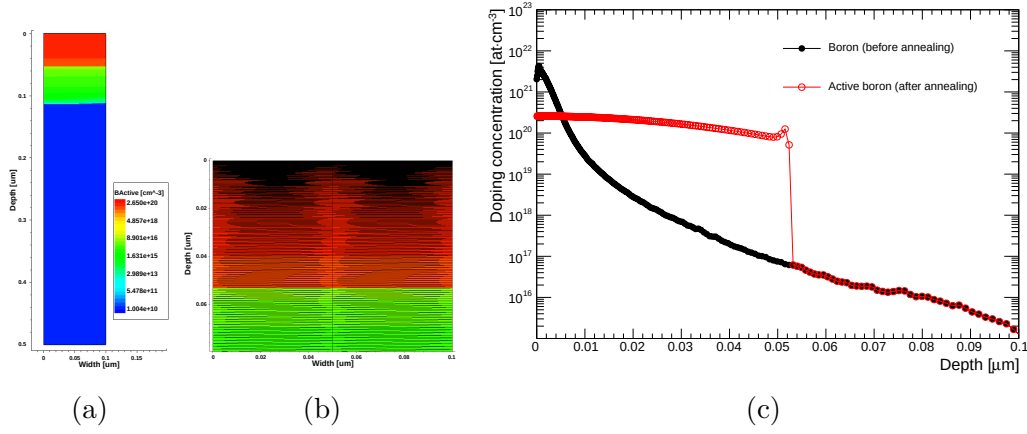


Figure 5.34: (a) Sentaurus Process TCAD simulation of IBS backside p+ plasma immersion ion implantation and laser annealing. A shallower region of silicon was defined with respect to figure 5.32a to keep the simulation time down. (b) Zoom of (a) showing the simulation mesh. The colour scale of both plots is active boron concentration. (c) 1D simulated doping profile of the backside p+ implantation before (solid markers) and after (empty markers) laser annealing.

This was achieved by applying a constant doping profile to the silicon region, with boron concentration of $6.986 \cdot 10^{12} \text{ cm}^{-2}$ [12]. A typical pixel in LFoundry 150 nm technology was implemented using a similar method to those above and presented in the previous chapter, with no topside substrate contacts. The simulation is then split into three so-called ‘experiments’ in order to test the two types of backside implantation, and one control, where no backside implantation is defined. In the first, the doping profile resulting from BI and RTA Sentaurus Process simulations is applied across the width of the backside (figure 5.35b). In the second, the doping profile resulting from PIII and LA simulations is applied across the width (figure 5.35c). And finally in the third, no backside implant is defined (figure 5.35d). It is assumed in the final fabrication that IBS will use the same process for applying metallisation for both backside processing methods. Therefore a 1022 nm thick region of aluminium was defined across the width of the backside in all three experiments.

The I - V simulations are performed in the same manner as those presented above and in the previous chapter. For the reverse characteristics, the deep n-well (and the wells inside the deep n-well) is biased to 0 V and the backside contact is ramped to negative high voltage using a transient ramp. Instances of the simulation were saved at 50 V steps to characterise the growth of the depletion region, described later. As usual, the simulation stops when the current measured at the backside contact is greater than $10 \mu\text{A}$. The difference in breakdown voltage of about 200 V with respect to the simulation in figure 5.5 is most likely due to fact that the topside pixel doping profiles used were those developed in chapter 3. With respect to the backside doping profiles, it can be seen that despite the low activation of the beamline implantation

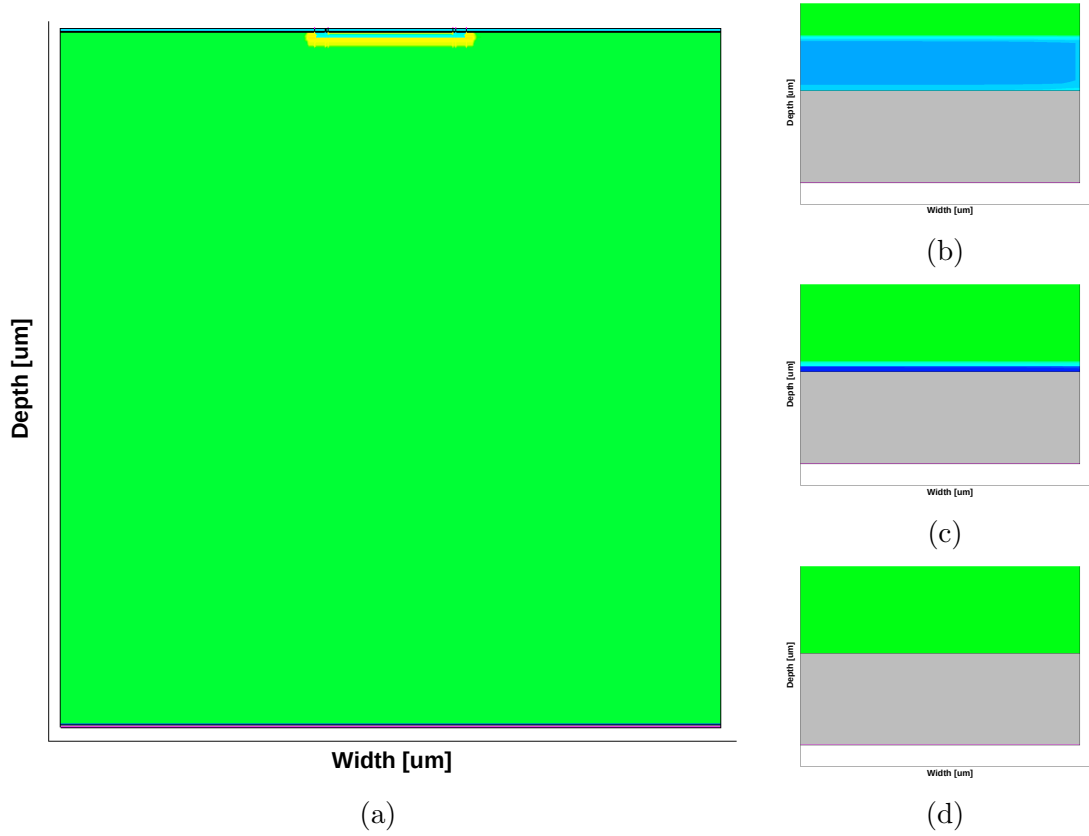


Figure 5.35: (a) A 2D TCAD simulation of a single pixel in LFoundry 150 nm technology, in a large area of substrate. The substrate is biased from the backside using three different doping profiles shown in (b), (c), and (d), and a large metal contact that spans the width of the simulation. (b) Simulated BI + RTA doping profile on the backside of the simulation. The grey region is the aluminium contact. (c) Simulated PIII + LA doping profile. (d) Only metallisation. No doping profile was defined on the backside.

and the shallow profile of the plasma implantation, both doping profiles function equally well. This is shown in figure 5.36a when compared to the simulation without backside doping, at a substrate bias voltage of $V_{\text{sub}} \approx -600 \text{ V}$, there is an increase in leakage current. The reason for this can be seen when the depth of the depletion region is investigated.

The depleted depth was estimated quickly using the Depletion Region Edges tool in a Sentaurus Visual TCL script (see user guide [39]) and plotted in figure 5.36b. Instances of the transient simulation are saved at 50 V steps, and a vertical profile directly in the centre of the pixel was extracted. The edges of the depletion region were plotted using the tool and retrieved. It can be seen that the simulated device is fully depleted at $V_{\text{sub}} \approx -600 \text{ V}$ when the data reaches a plateau at a depth of $280 \mu\text{m}$ (i.e., the thickness of the substrate), corresponding to full depletion. In the case of the simulation with backside metallisation and no backside doping, once the simulated substrate is fully depleted, there is an increase in current due to charge

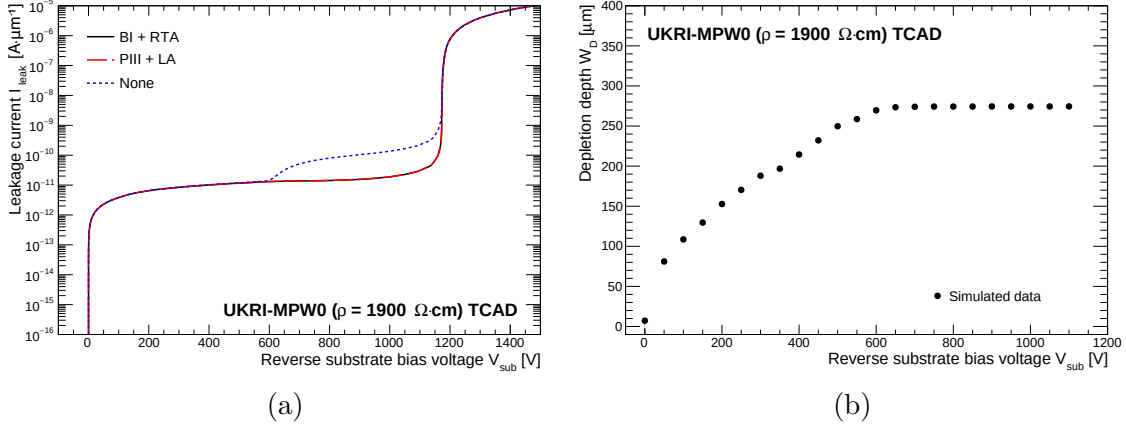


Figure 5.36: (a) TCAD simulations of reverse current–voltage characteristics of three backside biased pixels. The solid line shows the pixel that is backside doped using a doping profile from simulated beamline implantation (BI) and rapid thermal annealing (RTA) processes. The dashed line shows the pixel that is backside doped using a simulated plasma immersion ion implantation (PIII) and laser annealing (LA) doping profile. The dotted line shows the simulation of a pixel that contains no backside doping. (b) TCAD simulation of estimated depletion depth at 50 V instances from the simulation with no backside implant.

injection. This is not seen with either backside doping profiles extracted from BI and RTA simulations or PIII and LA simulations.

As both backside processing methods were shown to provide a good contact in these simulations, two wafers of backside processed UKRI-MPW0 were produced, one with BI and RTA and one with PIII and LA. The first was backside processed with PIII and LA to see if there was an improvement with respect to the peak in charge collection at the backside seen in e-TCT measurements. Despite this charge collection peak, H35DEMO and MuPix8/ATLASPix1 samples backside processed with BI and RTA perform well. Therefore, the second wafer was processed with BI and RTA to ensure at least one wafer was guaranteed to work since measurements have not been performed on wafers backside processed with PIII and LA in our laboratory, and their performance cannot be verified. In the next section, the simulations used to explore the topside elements such as the seal ring, guard rings and filling structures will be discussed.

5.5 Simulations and design of topside elements

The measurements of the H35DEMO and MuPix8/ATLASPix1 samples presented in the previous section corroborate that HV-CMOS detectors backside biased with the process from IBS work well. This was the first step in developing HV-CMOS detectors that do not include substrate contacts on the topside. Presented in this

section are the simulations and design of the new backside biased HV-CMOS detector UKRI-MPW0. The design differs from other backside biased devices in similar technologies [1, 11] as the backside p-type implant that biases the substrate is the only p-type implant in direct contact with the substrate. There are no topside substrate contacts, floating or otherwise. This is very similar to the structure of planar sensors in hybrid pixel detector modules.

In order to achieve this, a number of structures that are typically implemented on the topside of HV-CMOS detectors required modification, in addition to the pixels. In the LFoundry 150 nm technology, this included elements such as the seal ring, pad diodes like those seen in studies of RD50-MPW1 in chapter 4, and filling structures that were used in RD50-MPW2 improvements also in chapter 4. For structures like the pad diodes that have a cross-sectional structure very similar to pixels i.e., a DNWELL with NWELL/NISO stack ring that contains CMOS electronics surrounded by a PWELL ring, it was enough to remove the PWELL ring. However, elements such as the seal ring and filling structures required more study to understand the consequences of removing p-type implants. These studies are presented in this section.

One known problem with the removal of p-type implants between n-type implants is the formation of inversion layers at the STI-p-substrate interface due to the attraction of minority carriers to the overall positive charge of SiO_2 . This allows current to flow between neighbouring n-type wells. In the case of UKRI-MPW0, these could be pixels, or pixels and other structures, such as the n-type seal ring designed to collect current from the dicing edge. This is highly undesirable. However, as this is a known problem, simulation time was not dedicated to study the magnitude of this effect. In the following simulations, oxide charges were not included to try and simplify simulations as much as possible. This will however, need to be investigated in the future as this effect was observed in fabricated UKRI-MPW0 samples. A remedy to this effect will also need to be studied, such as a low-concentration p-type spray to counteract the inversion layer, but maintain high breakdown voltages. At the end of this section, there is also a preliminary study of MOS structures on the topside. One concern of applying such high voltages to CMOS devices was dielectric breakdown of STI, Inter-Layer Dielectric (ILD), and Inter-Metal Dielectric (IMD) which could possibly include overhanging metal layers or polysilicon field plates layers seen in planar sensors and Monopix chips. However, more study needs to be done in this context, such as TCAD simulations.

5.5.1 Seal ring

In CMOS technologies, seal rings are structures surrounding designs that protect samples from mechanical stress and contamination during the die sawing process. A typical seal ring makes use of an uninterrupted ‘tower’ of all available metal and metal via layers, from the topmost metal layer down to the contact layer on topside of the substrate, in continuous rings. For a p-type silicon substrate, a p-type well can then be placed underneath the contact layer, so that the seal ring can double as a substrate contact [40]. The LFoundry 150 nm technology makes use of such a seal ring. Therefore, in order to ensure there were no other p-type implants in contact with the substrate on the topside, the seal ring was modified by changing all p-type wells for their n-type counterparts. The seal ring therefore doubles as a Current Terminating Structure (CTS) described in reference [41], which decouples high I_{leak} generated at the cut-edge of the detector from the sensitive volume of the pixels. This is discussed in more detail in section 5.5.2. Further details of the modified seal ring design are not presented here in order to preserve intellectual property, but TCAD simulations of the observed macro-effects are. However, it should be noted briefly that the seal ring is made using NWELL, NISO and DNWELL, to improve reverse breakdown characteristics. This is discussed in section 5.5.4. In addition, the seal rings are biased in these simulations, which also improved breakdown voltage in these simulations. This is expanded upon in section 5.5.5.

The first simulation that is presented is of one pixel in a large area of substrate, with a depth of $280\,\mu\text{m}$, the estimated thickness of final wafers. This can be seen in figure 5.37a. The DNWELL is biased to 0 V and has no topside p-type substrate contacts. Instead, the substrate is biased to negative high voltage from the backside (which cannot be seen in the image). The distance between the pixel and the edge of the simulation is approximately equal to the distance between the outermost pixels and the edge of the chip in RD50-MPW2. This is symmetrical on either side to allow the depletion region of the pixel to grow properly. At the edges of the simulation, a seal ring is implemented by means of p+/PWELL stacks, metal contacts, one metal layer, and SiO_2 as ILD. This is also biased to high voltage. This is compared to an identical simulation where the seal ring is n-type (see figure 5.37b), implemented via an n+/NWELL/NISO/DNWELL stack. In this scenario, the seal ring is biased to 0 V, like the pixel.

The reverse I – V characteristics simulation results can be seen in figure 5.38. For a pixel biased from the backside, without topside substrate contacts, and a p-type seal ring, the breakdown voltage is around $-700\,\text{V}$. It is high because the effective distance between n-type and p-type wells is the pixel–seal ring distance. If designers wanted to decrease the inactive area of devices, this distance would need to be

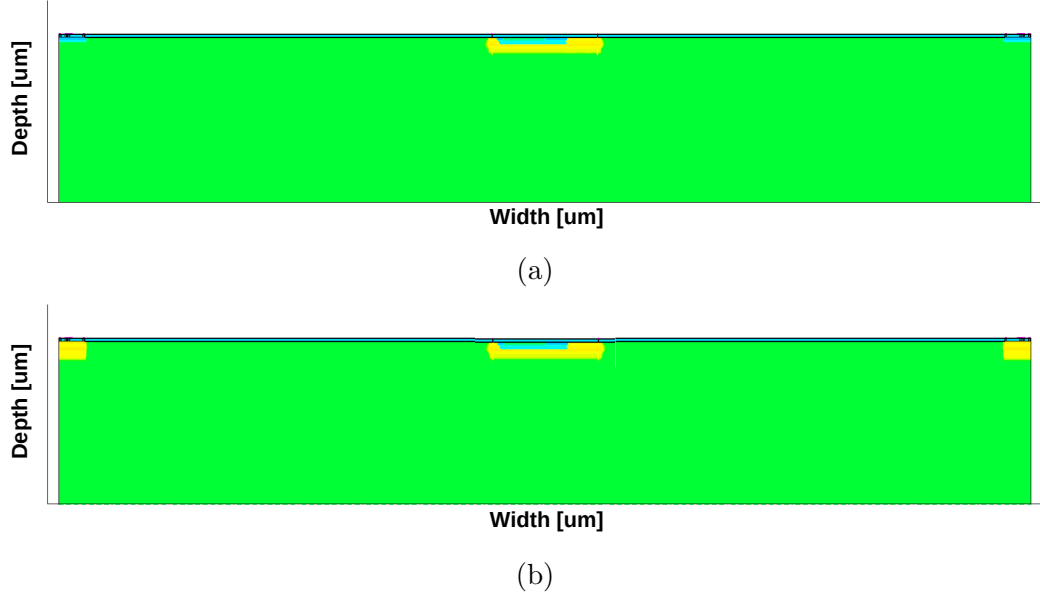


Figure 5.37: (a) 2D TCAD simulation of one pixel in a large substrate with p-type seal ring on the outer edges. The full depth of the simulation is not shown in this image. The colour of the plot represents doping concentration. (b) Identical simulation except for n-type seal ring.

decreased, and therefore, the breakdown voltage would decrease. Work is currently ongoing in the Monopix chips and the third RD50 prototype RD50-MPW3 to design guard rings to reduce this inactive area and maintain high breakdown voltages [42]. Measured breakdown voltages of -340 V are reported. Guard ring-like structures used in this submission will be discussed in the next section.

Reverse I - V characteristics of the identical simulation but with a deep n-type seal ring are shown in the red curve. The breakdown voltage is much higher, as the distance between p-type and n-type contacts is equal to the thickness of the chip. The leakage current is approximately three times higher as there are three ‘pixels’ (the left seal ring cross-section, the pixel, and the right seal ring cross-section i.e., n^+ /NWELL/NISO/DNWELL stacks biased to 0 V) in the simulation contributing to the leakage current. In fact, this demonstrates another important advantage of this type of design. By using a biased, n-type seal ring, there should be no need to implement area-consuming guard rings and the active area of the detector can be increased, while maintaining large p-type-n-type distance to keep the breakdown voltage high. This is discussed in the next section.

5.5.2 Guard rings

In CMOS technology, seal rings are used for passivation and absorbing mechanical stress during the die sawing process. However, the edges of samples that remain after dicing are heavily damaged and are areas full of defects. This is sometimes referred

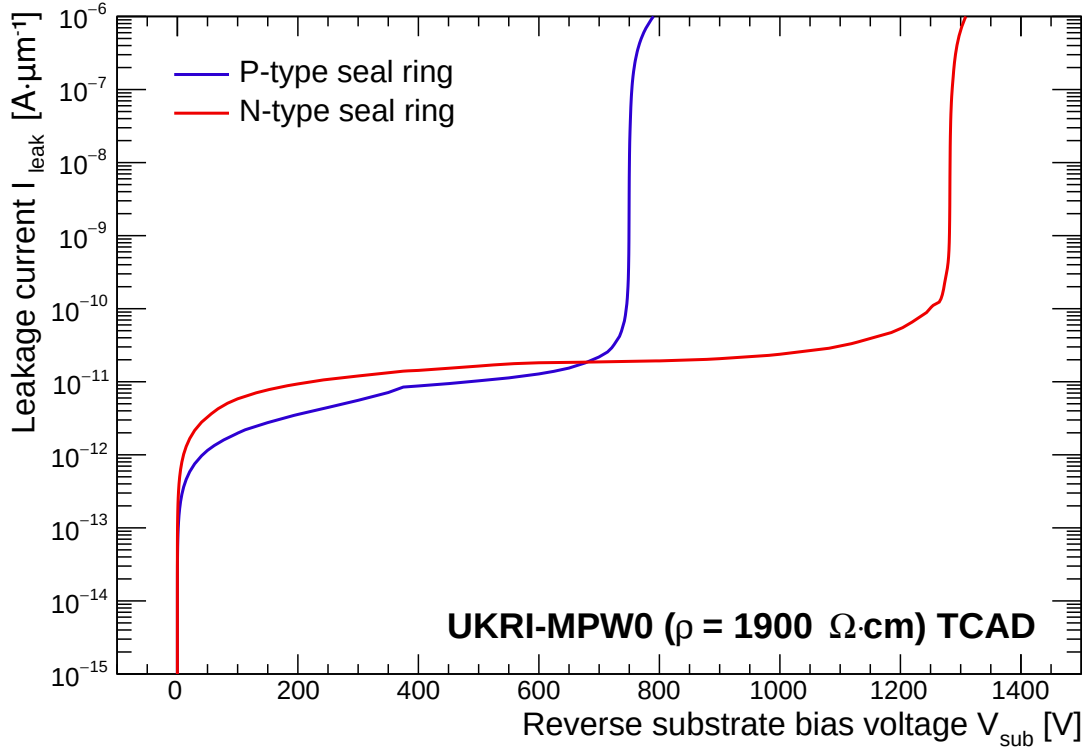


Figure 5.38: Reverse I - V characteristics of simulations shown in figure 5.37.

to as an *active edge*, as the high density of defects in this region add additional levels into the silicon bandgap which increases the generation of charge carriers. This is a problem in sensors such HV-CMOS that use large depletion regions as sensing elements as leakage currents can increase by many orders of magnitude if depletion regions come into contact with the damaged edge. Designers remedy this by implementing other types of rings known as *guard rings* around the sensitive area to protect it from the active edge. Guard rings have been simulated using TCAD in n-on-p sensors in reference [43] and [44], the latter of which studies a structure similar to that in this section with p-spray implemented. A similar design to reference [43] was simulated and implemented in HV-CMOS detectors [45], and new guard ring designs for HV-CMOS detectors are being developed and tested [42].

In the referenced designs, floating p-type rings on a p-type substrate are used for two reasons. The first is to interrupt Si-SiO₂ inversion layers at the surface which provide a conductive path from the edge to the sensitive area. The second is to control the potential drop between the sensitive area and the edge, which is otherwise unknown and unpredictable. This can lead to early, local breakdowns if the potential drop is too large over short distances. These p-type rings might be used in combination with overhanging metal layers or polysilicon field plates to minimize high fields [43, 45], or even n-type rings in close proximity [42] to reduce the field.

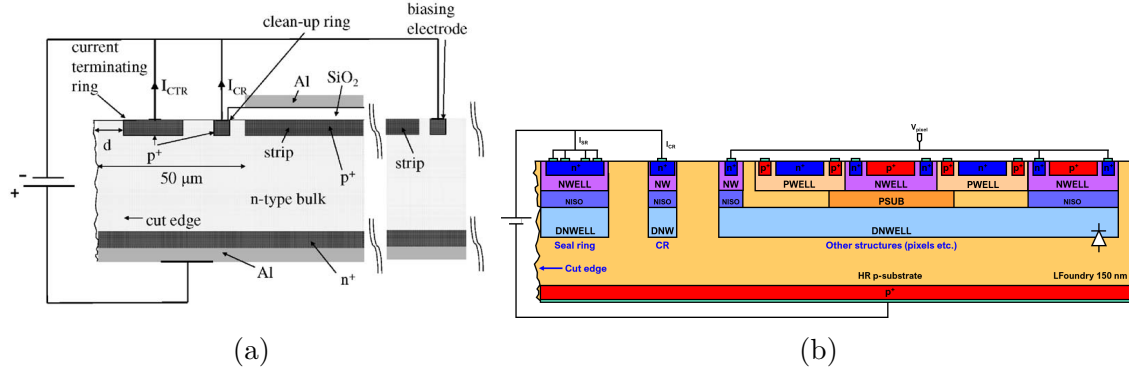


Figure 5.39: (a) Diagram of cross-section of a silicon detector with a CTS [48]. (b) Similar CTS implemented in CMOS technology.

In the UKRI-MPW0 prototype submission, the aim was to demonstrate that removing PWELL implanted into the p-type substrate increases the breakdown voltage. Therefore, to maintain this principle, a guard ring structure that also requires no p-type wells on the topside needed to be investigated. Otherwise, a very large area at the periphery of the chip would be required for the guard rings. In addition, a large spacing between p-type guard rings and n-type sensing pixels would be needed, something approximately equivalent to the thickness of the chip, to maximise breakdown voltage. Therefore in this design, a structure similar to that used in the edgeless planar sensors in the TOTEM experiment [46] were adopted, which is known as a (CTS) [47, 48]

The structure can be seen in figure 5.39a and consists of a biased, current terminating ring (CTR) that surrounds the whole sample, and a concentric clean-up ring (CR) between the CTR and the active area (the strips in this case) in the centre of samples. The CTR collects the current generated at the cut edge surface, and the CR ‘cleans up’ the remaining current generated at the cut edge that cannot be collected by the CTR due to diffusion into the bulk [49]. This structure has been simulated and implemented in the LFoundry 150 nm HV-CMOS technology, exploiting the seal ring to be used as the CTR, and implementing a CR (see figure 5.39b). As mentioned before, the seal ring in the LFoundry 150 nm node is made of p+ and PWELL implants. For this submission, these implants were converted to their n-type counterparts n+ and NWELL, and NISO and DNWELL were added. The reason for the addition of NISO and DNWELL is described in section 5.5.4 It should be noted that the detectors presented by the authors of references [47] and [48] use an n-type substrate, backside biased with an n+ implant, and strips and the CTS implemented on the topside using p+ implants. These are the opposite dopings from those used here, but the principle is the same.

TCAD simulations were used to investigate the effectiveness of this n-type seal ring and another n-type implant as a CTS are presented. The same simulations

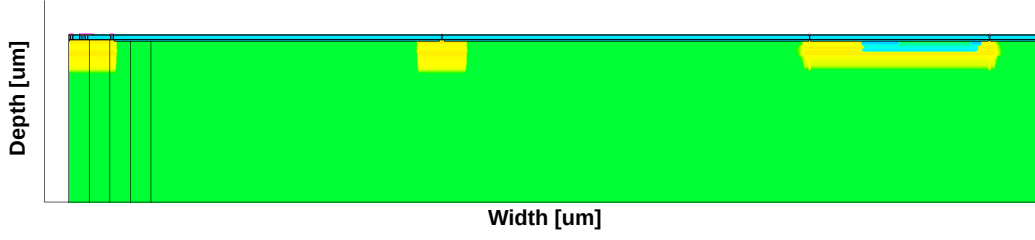


Figure 5.40: 2D TCAD simulation of one pixel in a large substrate with n-type seal ring/CTR and another n-type implant acting as a CR. Together, these form the CTS [48]. The regions modelled as damaged silicon from the dicing process can be seen on the left. The full depth of the simulation is not shown in this image. The colour of the plot represents doping concentration.

presented in the last section are used here. However, damage due to dicing is included and modelled using the method described in [41]. This can be seen in figure 5.40. The seal ring/CTR, the CR, and the pixel are all connected to separate voltage sources which are all biased to 0 V. Like the other simulations seen so far, the substrate is then biased to negative high voltage in 1 V s^{-1} steps using a transient ramp.

The results of the simulation can be seen in figure 5.41 and will be discussed in terms of leakage currents and breakdown voltages. The solid black line represents the absolute value of the current simulated at the backside substrate contact I_{sub} , and is the sum of the currents simulated at the seal ring/CTR I_{CTR} , the CR I_{CR} , and the pixel I_{pixel} . It can be seen that the current simulated at the CTR is the largest, due to the introduction of energy levels in the silicon band gap in the defect region increasing the carrier generation at the edges. It should be noted of course, that in measurements of a real device with this design, I_{CTR} would be much higher, since the seal ring surrounds the entire chip and the third dimension in this simulation is just $1 \mu\text{m}$. The next largest current is measured at the CR, which is expected as it is the next closest structure to the damaged region. Then it can be seen that the leakage current at the pixel is the lowest which means the CTS is functioning as it should. As with the planar sensors presented in references [47] and [48], a CTS maintains a large breakdown voltage by ensuring a large p-type–n-type distance, keeps leakage current at the pixels low, and decreases the inactive area of detectors.

It should be noted that I–V measurements in the referenced papers show the detectors were stable up to 200 V however, no breakdown is presented. Comparing the breakdown voltage in the simulations in this section to those in the previous section shows that it is increased even further from approximately -1200 V to approximately -1700 V . In other words, The inclusion of another n-type implant in the ‘empty’ space between the seal ring and the pixel increases the breakdown voltage with respect to that seen in figure 5.38. This will be expanded upon in the next

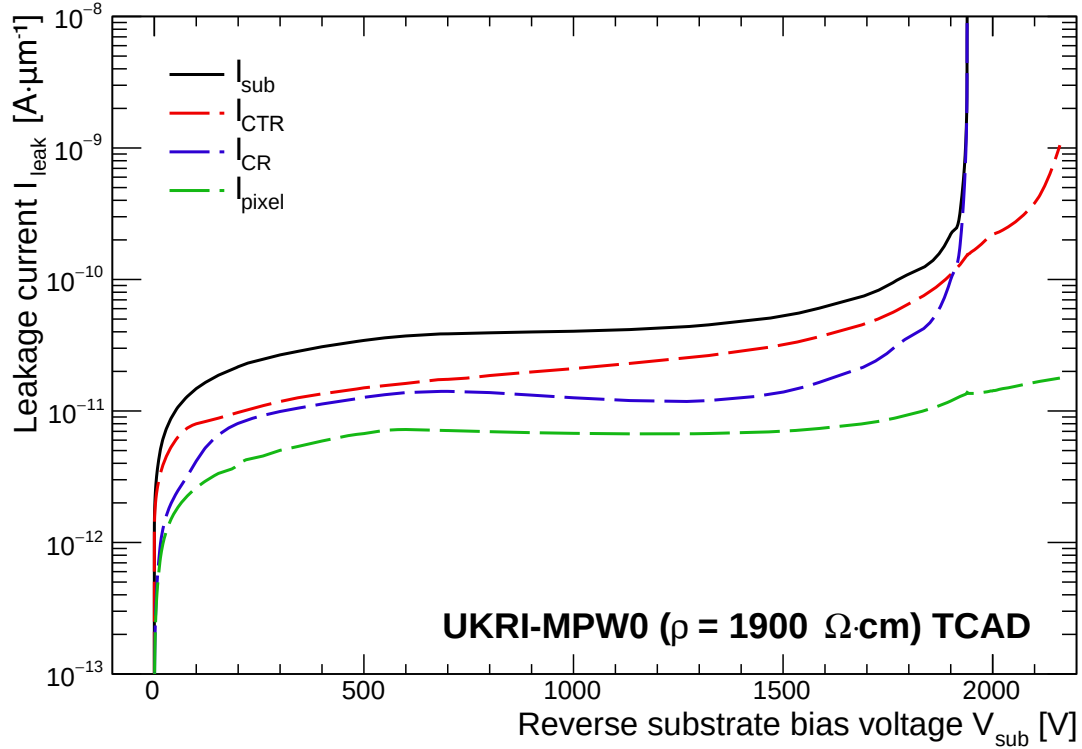


Figure 5.41: Reverse I - V characteristic simulations of the structure in figure 5.40. I_{sub} is the absolute value of the current simulated at the backside substrate contact and is the sum of the currents simulated at the seal ring/CTR I_{CTR} , the CR I_{CR} , and the pixel I_{pixel} .

section. Note that these values are much higher than the measured value which is expected due to idealities in simulations, but it could suggest that it is important to bias all n-type wells in the detector to maximise the breakdown voltage. This was not the case in I - V measurements presented in the final section of this chapter which will be covered in more detail in that section.

5.5.3 Filling structures

At the end of the previous section, it was noted that it could be necessary to fill ‘empty’ areas on the topside with n-type implants in order to maximise the breakdown voltage. At the same time, CMOS foundries automatically fill empty space with dummy filling structures to ensure good planarity after Chemical Mechanical Polishing (CMP) in a process known as *planarisation*. It was seen in measurements of RD50-MPW1 and RD50-MPW2, and confirmed with simulations in previous chapters that it is necessary to enclose these dummy filling structures with a p-type implant to ensure low leakage current. In a similar manner to simulations of RD50-MPW1, simulations of the dummy filling structures are considered here for UKRI-MPW0. In a design where there can be no p-type wells on the topside, n-

type must be used instead. This section presents simulations confirming the validity of using n-type layers (NWELL, NISO, and DNWELL) to enclose dummy filling structures instead of p-type and keep leakage current to a minimum.

The same simulations used in the study of RD50-MPW2 were used here to demonstrate the concept. As a reminder, the structure that was simulated was a simplified version of one of the pad diodes from the RD50-MPW1 submission. This is shown in figure 5.42a. Since automatic PWELL generation was blocked in the RD50-MPW1 submission to ensure high breakdown voltage, silicide filling structures were automatically placed directly on the substrate. When the pixel is reversed biased, the depletion region grows laterally into the substrate, comes into contact with the silicide, and carriers inject into the depletion region, increasing the leakage current. This can be seen in figure 5.43a which is a snapshot of the transient simulation at $V_{\text{sub}} = -100$ V. The colour of the plot represents electron current density, where red is high and blue is low.

Figure 5.42b shows the filling structures enclosed in an n-type implant, in this case NWELL. It should be noted that this simulation differs from the UKRI-MPW0 submission in two ways. Firstly, filling structures in fabricated samples are enclosed in NWELL, NISO, and DNWELL. Secondly, this simulation includes topside p-type substrate contacts, which was not the case in UKRI-MPW0. This simulation was performed simply to demonstrate the concept that the filling structures can be enclosed in n-type layers to reduce the leakage current with respect to the RD50-MPW1 simulations. Figure 5.43b shows a snapshot of this simulation when $V_{\text{sub}} = -100$ V. When compared to figure 5.43a, it can be seen that by enclosing the filling tiles in NWELL, no more current from the silicide is seen.

The I - V characteristic curves of simulations of filling structures from chapter 4 can be seen in figure 5.44 with the results from the UKRI-MPW0 simulation added. It can be seen that NWELL acts as a suitable enclosure for these conductive filling tiles and returns leakage current down to the ‘ideal’ level. As a reminder, the ideal level was a simulation without silicide filling structures. The simulated breakdown voltage is lower in this simulation because the distance between the new NWELL enclosures and the topside p-type substrate contacts is less than the distance between the pixel and the topside substrate contacts. This is not the case in the final design of UKRI-MPW0 as there are no topside contacts.

5.5.4 Blocks without deep n-type implants

Something that was considered in the design process at the beginning was including an n-type seal ring simply made from NWELL without the deep n-type layers NISO and DNWELL. Presented in this section is a simulation identical to that shown in

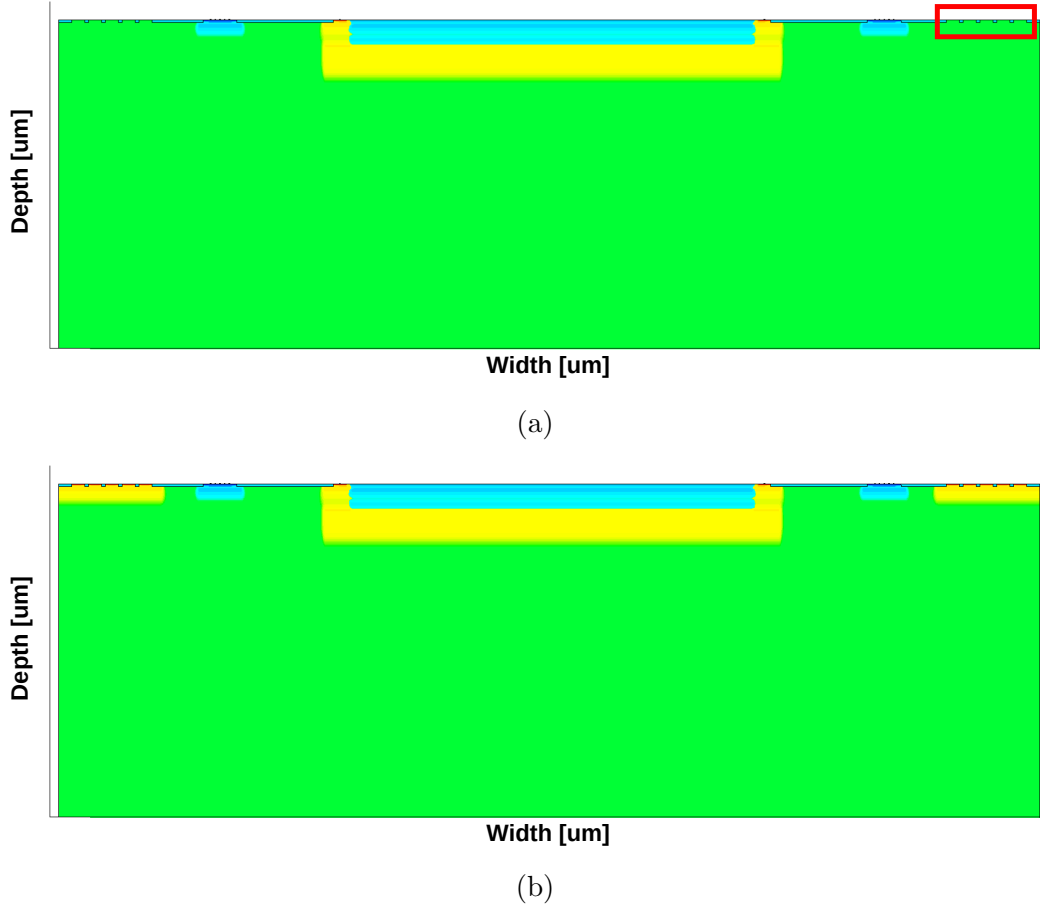


Figure 5.42: (a) Simulation of the topside biased pixel with dummy filling structures implemented on the substrate, presented in chapter 4. These are marked with a red square. Colour of the plot is doping concentration. (b) Dummy filling structures enclosed in NWELL.

section 5.5.1, with a seal ring made from only NWELL. The cross-section is shown in figure 5.45a.

The results of the simulations are presented in figure 5.46. For reference, the simulation of one pixel and a biased deep n-type seal ring from section 5.5.1 is shown in a dashed black line. The red line shows the reverse I - V characteristics of the simulation of a pixel and n-type seal ring where the seal ring is implemented using just NWELL. The lower breakdown voltage demonstrates the importance of including both NISO and DNWELL in all blocks in a final design.

5.5.5 Non-biased blocks

In addition to ensuring n-type implants include deep n-type layers, all n-type implants must also be fixed to a known voltage (in this case, to 0 V) in order to achieve the highest of breakdown voltages. A simulation identical to that in the previous section was created, except that the seal ring was implemented using NWELL,

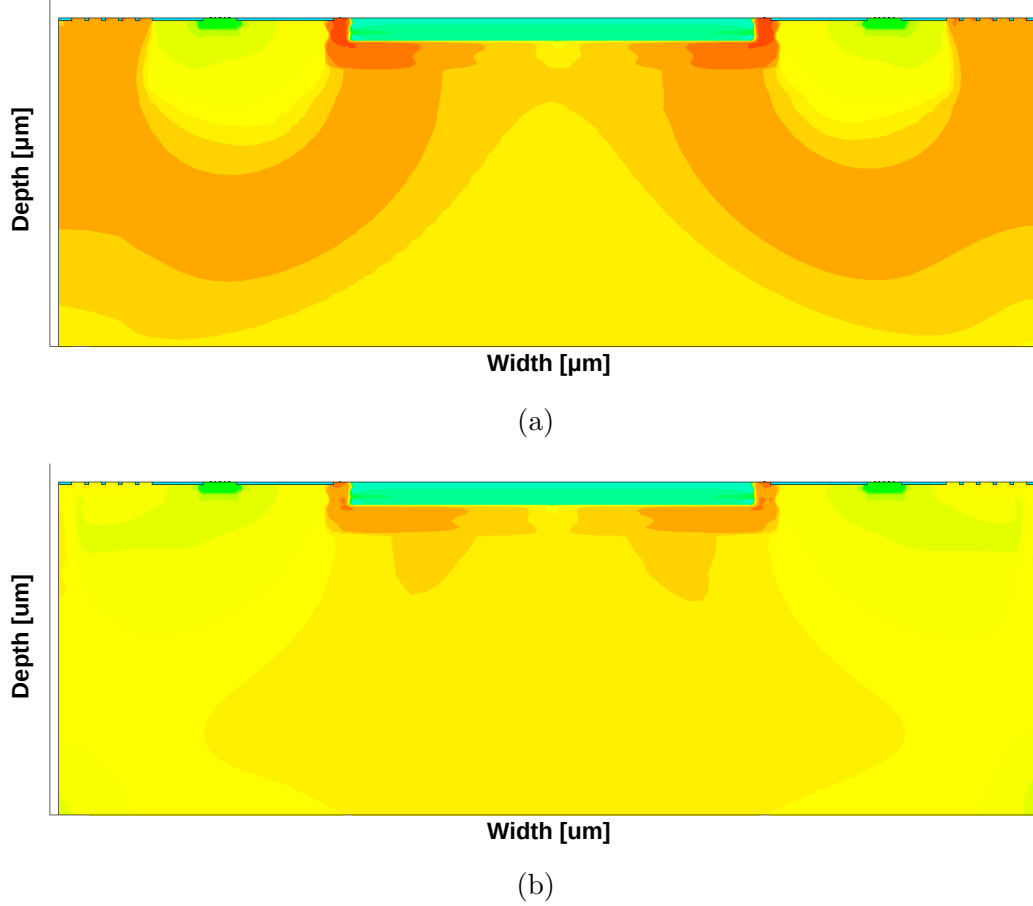


Figure 5.43: (a). Simulation of topside biased pixel at $V_{\text{sub}} = -100 \text{ V}$. Colour of the plot is electron current density. Current can be seen flowing between dummy filling structures and pixel. (b). Identical simulation with dummy filling structures enclosed in NWELL. $V_{\text{sub}} = -100 \text{ V}$. No current can be seen between dummy filling structures and pixel due to inclusion of NWELL.

NISO, and DNWELL, but was left floating. A diagram of this can be seen in figure 5.45b. The results of the simulation can be seen in the solid blue line in 5.46. The breakdown voltage is higher than that of a simulation with a seal ring made using NWELL, but lower than the simulation of a biased seal ring made from NWELL, NISO, and DNWELL shown in section 5.5.1 used here for reference. This demonstrates the importance of biasing all blocks in a final design. If one block (the seal ring for example) was left floating, the breakdown voltage would be lower. This needs to be confirmed with measurements (see section 5.6).

5.5.6 Dielectric breakdown of MOS structures

One area of concern for a design at such high voltages is dielectric breakdown. At sufficiently high voltages, dielectrics become conductive which can be destructive. In CMOS technologies, dielectrics are used for STI, to isolate metals from polysil-

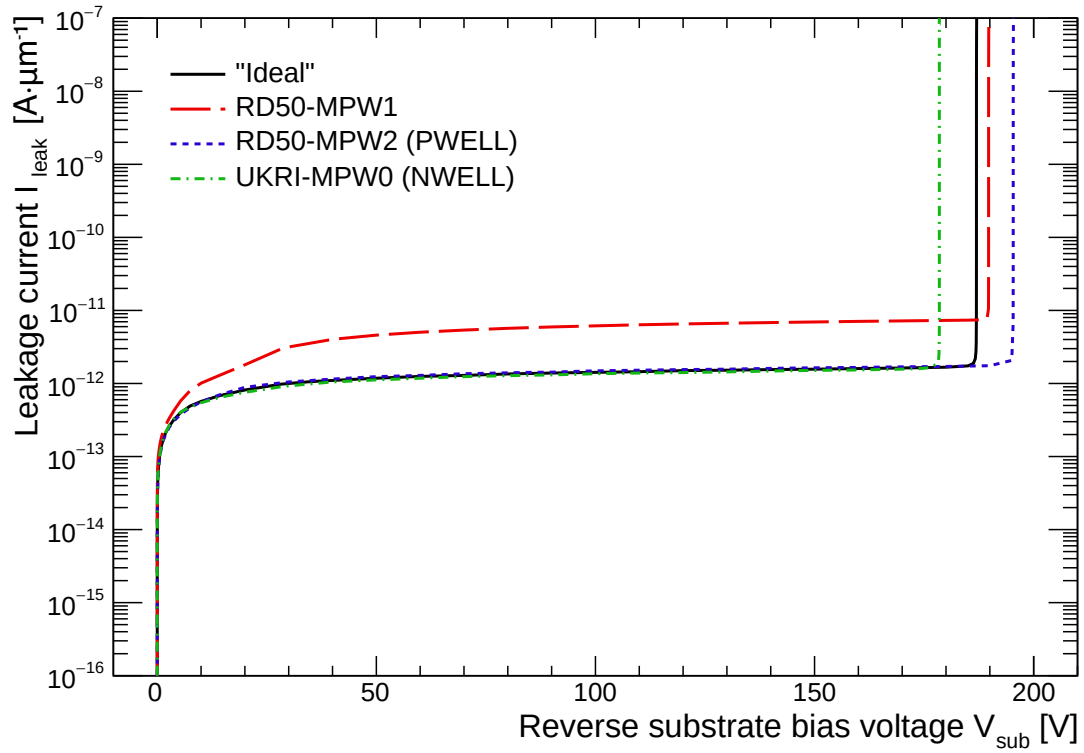


Figure 5.44: Reverse I - V characteristics of simulations in figure 5.42. Adding NWELL to RD50-MPW1 simulation reduces the leakage current back to ‘ideal’ level.

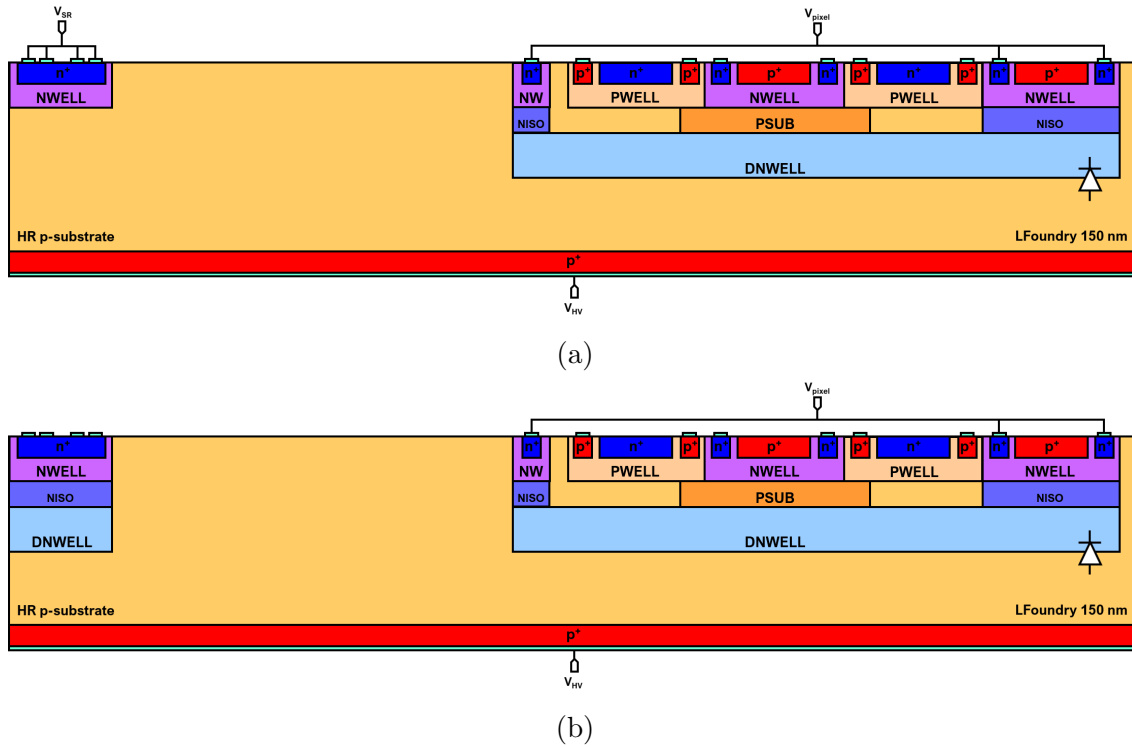
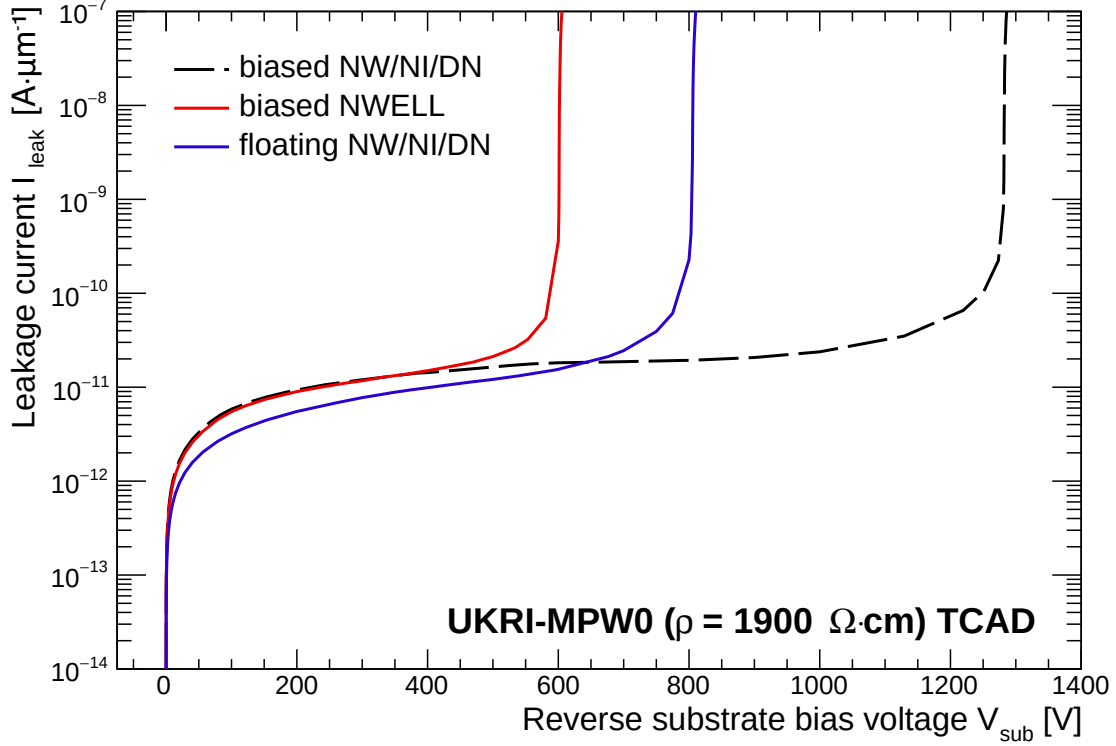


Figure 5.45: (a) Diagram of a biased seal ring implemented with NWELL instead of an NWELL/NISO/DNWELL stack. One pixel can be seen on the right. (b) Diagram of a non-biased NWELL/NISO/DNWELL seal ring.


 Figure 5.46: Simulated reverse I - V characteristics.

icon gates (ILDs), and to isolate metals from each other (IMDs). For this reason, careful attention was paid to low level metal layers biased to voltages close to 0 V overhanging the high negatively biased silicon substrate, and polysilicon field plates were avoided. A diagram of a simple MOS structure can be seen in figure 5.47. Since it is known that there is dielectric material between components in fabricated samples, it is possible that a sufficiently large potential difference could destroy the dielectric material and potentially the sample.

The exact materials and thicknesses of the ILD and IMDs in the 150 nm technology node from LFoundry are unknown, but the phenomenon can be explained with a dielectric such as silicon dioxide. This is a dielectric commonly used in CMOS technologies. The breakdown voltage of a dielectric $V_{BD,d}$ is given by the formula [50]

$$V_{BD,d} = E_{ds}d \quad (5.16)$$

where E_{ds} is the dielectric strength and d is the separation between the conductors either side of the dielectric. The dielectric strength of silicon dioxide is equal to $10^7 \text{ V} \cdot \text{cm}^{-1}$ [51]. Assuming the dielectric is something in the range of $0.1\text{--}1.0 \mu\text{m}$, $100 < V_{BD,d} < 1000$. This is within the range of bias voltage expected to be applied to this device. Therefore all care was taken to ensure that no first or second layer metals were overhanging NWEELLs as higher metal layers are likely further away

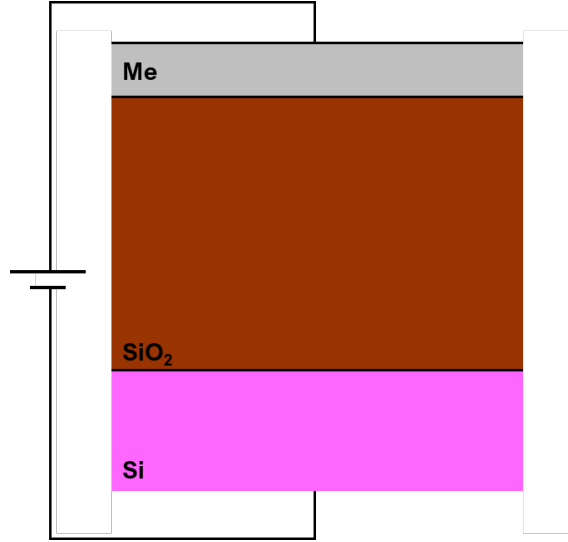


Figure 5.47: Diagram of Metal-Oxide-Semiconductor (MOS) capacitor.

from the substrate (i.e., $> 1.0 \mu\text{m}$). However, this is just a back-of-the-envelope calculation, and choices to exclude field plates and metal overhang were made due to time constraints. A more accurate analysis is required using known dielectric materials and thicknesses in the technology. It is possible that polysilicon field plates and metal overhang could also be used in designs like UKRI-MPW0 to reduce field maxima.

5.6 Measurements of fabricated UKRI-MPW0 samples

UKRI-MPW0 was designed and submitted in the November 2020 MPW run in the LFoundry 150 nm technology node with design choices made based on the simulations presented here. Two wafers have been fabricated in high resistivity ($1900 \Omega\cdot\text{cm}$) and were backside processed at IBS. One wafer was backside processed using BI and RTA and the other was backside processed with PIII and LA to test both methods. Wafers were received in Liverpool in June 2021, where testing commenced to validate the simulations presented here.

The I - V characteristics of the test structure with $60 \mu\text{m} \times 60 \mu\text{m}$ pixels implemented for e-TCT was measured. This is located at the top of the device (near the edge) and is shown in red in figure 5.48. Also shown in black, green and blue are similar test structures with different sized pixels. The test structures adopt the same design as those implemented in all designs seen so far in this thesis: a 3×3 matrix of pixels with two channels, one for the central pixel, and one for the outer eight pixels which are shorted together. Each test structure in this submission contains pixels of different sizes. From left to right, the pixels measure $50 \mu\text{m} \times 50 \mu\text{m}$ (highlighted

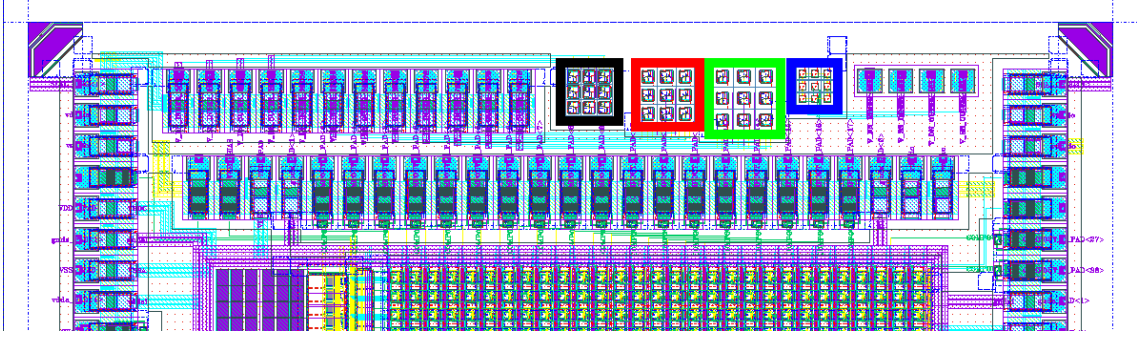


Figure 5.48: Location of UKRI-MPW0 test matrices. From left to right, the pixels in the matrices measure $50\ \mu\text{m} \times 50\ \mu\text{m}$ (highlighted in black), $60\ \mu\text{m} \times 60\ \mu\text{m}$ (highlighted in red), $70\ \mu\text{m} \times 70\ \mu\text{m}$ (highlighted in green), and $40\ \mu\text{m} \times 40\ \mu\text{m}$ (highlighted in blue).

in black), $60\ \mu\text{m} \times 60\ \mu\text{m}$ (highlighted in red), $70\ \mu\text{m} \times 70\ \mu\text{m}$ (highlighted in green), and $40\ \mu\text{m} \times 40\ \mu\text{m}$ (highlighted in blue). The $60\ \mu\text{m} \times 60\ \mu\text{m}$ pixels are the same size as those in the active matrices, and the others were implemented to test the effects of cross-talk which were foreseen to be a problem in this submission due to the absence of pixel-to-pixel isolation. In the first three matrices, the size of the DNWELLS are the same, but the spacing between them are different. The fourth and final matrix employs smaller DNWELLS, with the same DNWELL–DNWELL spacing as pixels in the active matrix. Specific details about the pixel sizes can be found in table 5.7.

Table 5.7: UKRI-MPW0 e-TCT test structure pixel details.

Parameter	Unit	Matrix 1	Matrix 2	Matrix 3	Matrix 4
Pixel width	μm	50.00	60.00	70.00	40.00
Pixel height	μm	50.00	60.00	70.00	40.00
DNWELL width	μm	41.66	41.66	41.66	21.66
DNWELL height	μm	41.66	41.66	41.66	21.66
DNWELL spacing	μm	8.34	18.34	28.34	18.34

I – V measurements were conducted at room temperature using a manual probe station in a dark cabinet. Measurements presented here were performed on one sample that was backside processed using BI and RTA, and one sample that was backside processed with PIII and LA. The substrate is biased using the probe station chuck through the backside contact which was connected to the negative terminal of a Keithley 2410. The current at the central pixels of the $60\ \mu\text{m} \times 60\ \mu\text{m}$ matrices and the seal ring were measured using a Keysight B2981A and two probes, one to bias the CTR and one to bias the central pixel in each test structure. The compliance current for the measurements was set to 4 mA. The eight outer pixels were left floating during the measurements along with filling structures, and all other structures. The results of the measurements can be seen in figure 5.49a. The

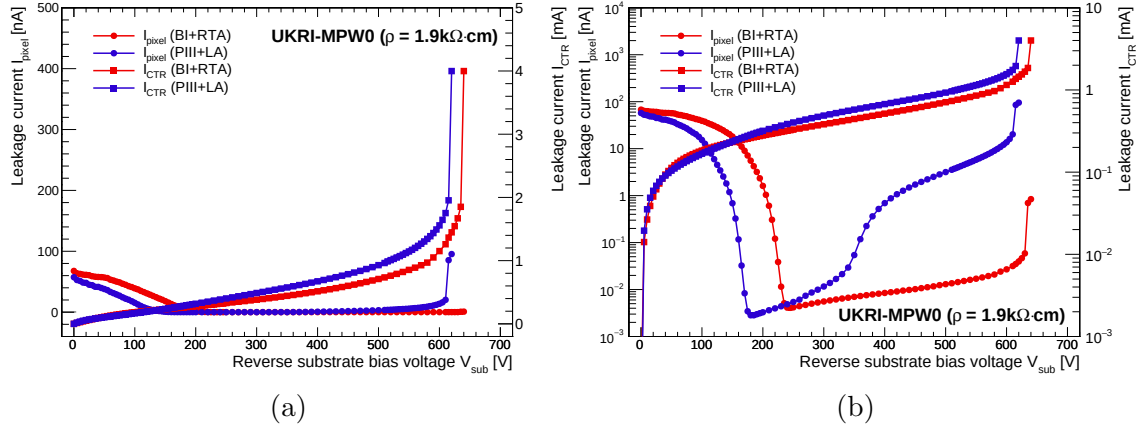


Figure 5.49: (a) I-V measurements of the CTR and central pixel of the $60 \mu\text{m} \times 60 \mu\text{m}$ test structure of UKRI-MPW0 samples. Sample processed with BI+RTA is shown in red and sample processed with PIII+LA is shown in blue. The left axis shows the current measured at the pixel and the points are represented by circular markers. The right axis shows the current measured at the CTR where the points are square markers. (b) Same as (a) with a logarithmic scale. Data courtesy of C. Zhang.

current measured at the central pixel pad I_{pixel} is shown using circular markers with the scale given on the left axis. The current measured at the CTR (seal ring pad) is shown using square markers and the scale is given on the right axis. The colours represent the samples backside processed using the two different methods.

Extracting by eye, the observed breakdown voltage is greater than 600 V. The leakage current at the seal ring rises approximately linearly (ohmic behaviour) until around 600 V when the current starts to rise exponentially. A high current at the pixels is observed at lower voltages (≈ 150 V) which then seems to saturate until breakdown. The difference between the simulated breakdown voltage of around 1000 V and the measured breakdown voltage is thought to be due to a combination of idealities in simulations and biasing conditions in the measurements. In measurements, just the CTR and a single pixel were biased. Viewing the measurements with a logarithmic scale (figure 5.49b) highlights the unusual behaviour observed at the pixels. A high current is observed at lower voltages which most likely a result of the lack of p-type isolation on the topside. An NPN transistor has most likely formed with the CTR and pixel as terminals and the p-substrate as the body. Without the p-type isolation, conductive channels between n-type implants are formed at the Si-SiO₂ interface. If there is a slight potential difference between the CTR and the pixel, electrons may be being drawn out of the pixel. At high enough bias voltages and therefore, large enough lateral depletion, a pinch-off effect can be seen and no current flows. This would need to be simulated to confirm. Nevertheless, the > 600 V breakdown voltage is a promising result. The very high current observed at the CTR is most likely due to current generated from the cut edge. It

might be possible to reduce this somewhat in a future design by using patterned backside implants and metallisation to form concentric, p-type guard rings around a high-voltage substrate contact to drop the potential towards the cut edge.

5.7 Summary

A new prototype monolithic HV-CMOS detector UKRI-MPW0 was submitted in the November 2020 MPW run in the LFoundry 150 nm node. The aim of this prototype was to demonstrate that the reverse breakdown voltage of such a detector can be increased significantly with respect to the state of the art by biasing the p-type substrate through a backside contact and excluding relatively high-concentration p-type implants (PWELL) between n-type implants from the topside design. The result is a detector that can be biased to > 600 V, similar to the structure and performance of n-on-p planar sensors, but with full CMOS electronics implemented in the same substrate. This is achieved thanks to the 150 nm HV-CMOS technology from LFoundry, which allows PWELL implants for NMOS transistors to be implemented on the topside if they are isolated from the p-type substrate by DNWELL and NWELL/NISO stack rings. The goal of developing HV-CMOS detectors such as this is to improve their radiation tolerance so that they might be used in future particle physics experiments where high radiation tolerance, high granularity, low material budget, and cost-effectiveness are requirements of silicon detectors.

In this thesis, the initial concept was demonstrated with the use of TCAD simulations. These simulations showed that the reverse breakdown voltage of a single pixel can be increased dramatically if the topside substrate contacts are removed, and the substrate is biased through a backside contact. TCAD simulations were also used in order to understand what must be done to extrapolate this design to a full HV-CMOS chip. This included simulations of topside elements such as the chip seal ring, guard rings, and filling structures, and also process simulations of two backside processing techniques available from IBS: BI and RTA, and PIII and LA. I - V and e-TCT measurements of two previous submissions in other HV-CMOS technologies H35DEMO and MuPix8/ATLASPix1 that had been backside processed using BI and RTA at IBS and backside biased, demonstrated that HV-CMOS detectors that have been backside processed using IBS techniques function very well. This backside processing technique was therefore used to backside process one UKRI-MPW0 wafer, and a second wafer was backside processed using the new PIII and LA method. I - V measurements of fabricated UKRI-MPW0 samples backside processed with PIII and LA exhibit breakdown voltages > 600 V, validating the concept presented in this thesis.

The next steps are to continue measurements of UKRI-MPW0, and begin the

design of the next prototype, UKRI-MPW1. Future measurements of UKRI-MPW0 related to this thesis include e-TCT measurements of both wafer types which are currently ongoing at Liverpool. Samples have also been irradiated with neutrons and I - V and e-TCT measurements of irradiated samples are also planned to study how radiation damage affects these detectors. Results of preliminary I - V measurements suggest that inter-pixel isolation is required, as anticipated, to account for inversion layers formed between pixels and other n-type structures by positive oxide charges in SiO_2 layers. The TCAD simulations performed in this section can be repeated with the addition of fixed positive oxide charges to confirm this. Since a very high breakdown voltage has now been demonstrated, development of a low-concentration p-spray implant with the LFoundry 150nm technology can now begin. This can be done using CMOS process TCAD simulations to understand how to develop an implant with high enough doping concentration to counteract fixed positive charges, but low enough to maintain high breakdown voltages. The simulations presented here can then be repeated a third time with oxide charges and the low-concentration p-type pixel isolation to determine if the implant is successful.

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Chapter 6

Conclusion

Future particle physics experiments such as the HL-LHC and FCC will increase the energy and number of particle collisions to unprecedented levels. This will affect the requirements of silicon detectors which will need to increase their timing and position tracking capabilities, reduce their material budget to reduce multiple scattering, and increase their radiation tolerance, to name a few examples. As an alternative to the current hybrid pixel detector modules, HV-CMOS particle tracking detectors are a promising candidate. Small diodes can be implemented into the silicon substrate which when reverse biased, form large depletion regions that are sensitive to particles. Additionally, thanks to multiple-well processes, full CMOS electronics can be embedded directly into the pixels on the same substrate, reducing production costs and the amount of detector material with respect to hybrid pixel detector modules. Currently, one active area of research is the improvement of radiation tolerance of HV-CMOS detectors. In silicon detectors, as damage due to radiation increases, the size of the sensitive volume decreases and detector leakage current increases, eventually reducing the SNR of detection events to insignificant levels. One way to mitigate the effects of radiation damage is to increase the operating voltage of detectors. This is however limited by the reverse breakdown voltage, which for HV-CMOS detectors is relatively low compared to planar sensors in hybrid pixel detector modules. The work in this thesis builds on previous work to increase the reverse breakdown voltage of HV-CMOS pixel tracking detectors and therefore potentially their radiation tolerance.

A methodology for developing fast and accurate TCAD models of HV-CMOS pixels was developed and presented. Individual implants available in the LFoundry 150 nm HV-CMOS technology were characterised separately and used to reconstruct an HV-CMOS pixel. The reconstruction required less than 1 minute of computation time. An identical pixel was simulated using process simulations which required nearly 60 hours of computation time, even with a very capable desktop computer. The accuracy of the reconstructed model was verified by comparing breakdown

voltages extracted from reverse I - V characteristic simulations with those of the pixel formed using process simulations. The difference in results is no more than is seen in sample-to-sample variations in fabricated samples, validating the model. The extracted breakdown voltages from both the reconstructed pixel and the pixel formed from process simulations did not match the expected value provided by the manufacturer, however. This expected value was confirmed with measurements of fabricated samples. Therefore, a more refined reverse breakdown simulation method was developed, which matches very well with the laboratory measurements. The presented methodology therefore hypothetically enables any structure possible in the LFoundry 150 nm technology to be simulated very quickly and very accurately, which is useful for simulating novel designs pre-fabrication, saving both time and money. While the results of the method presented here are only applicable to structures designed in the LFoundry 150 nm technology, the method itself could be repeated and applied to other technologies if the process parameters are known.

The TCAD simulations that were developed were used to identify methods for optimising the leakage current and breakdown voltage of HV-CMOS detectors developed within the RD50 collaboration. One of the first prototype chips in the LFoundry 150 nm technology developed within RD50 was RD50-MPW1. This prototype suffered from unusually high leakage current. The cause was investigated and identified in this study, and a second prototype RD50-MPW2 was developed and submitted in February 2019. I - V measurements of fabricated samples were performed, and confirmed that the high leakage current problem had been solved. Another goal of the second prototype was to increase the breakdown voltage with respect to the first prototype. A few design choices with respect to pixel geometry were investigated with TCAD simulations including pixel diode electrode implant spacing, and implant corner shapes. The simulations showed that the breakdown voltage could be increased by increasing electrode spacing and by using cut-off or rounded corner shapes. These results were also confirmed by I - V measurements performed on fabricated samples.

Knowledge gained from the study of RD50-MPW1 and the development of RD50-MPW2 led to the development of a new prototype HV-CMOS particle tracking detector UKRI-MPW0. The aim of UKRI-MPW0 and future prototypes is to increase the radiation tolerance of HV-CMOS pixel detectors. This zeroth prototype aims to demonstrate this is possible by adopting a design similar to planar silicon pixel sensors in hybrid pixel detector modules to increase the maximum operating voltage. For planar sensors in the past, the result of this was highly radiation tolerant silicon sensors that survived many years in the harsh conditions of the LHC experiments. The basic idea is that relatively high concentration p-type implants and n-type implants are implemented on opposite sides of the wafer which reduces internal electric

fields enabling higher breakdown voltages and therefore higher operating voltages. TCAD simulations of an HV-CMOS pixel in the LFoundry 150 nm technology presented here suggest that by using a similar design - n-type pixel cathodes on the topside and the p-type pixel anode on the backside - the breakdown voltage can be increased quite significantly with respect to the state of the art. Backside p-type implantation and biasing is a technique already used in current state-of-the-art HV-CMOS pixel detectors, however relatively high concentration p-stop implants are used to isolate adjacent n-type implants on the topside. Simulations presented here suggest that these p-stop implants limit the maximum possible breakdown voltage. Another topside n-type isolation technique, such as p-spray, would therefore need to be investigated for HV-CMOS detectors to counteract the formation of inversion layers at the surface due to positive charges in the oxide. Also presented in this thesis were the TCAD simulations used to investigate how the concept presented here could be scaled up to a full chip. This included simulations of n-type topside components such as guard rings and filling structures, and also two methods for a backside p-type implant. I - V and e-TCT measurements presented in this thesis demonstrate that HV-CMOS detectors fabricated in a different technology but backside processed with one of the investigated methods function well.

The UKRI-MPW0 prototype was submitted in the LFoundry 150 nm technology November 2020 MPW run as a proof of concept that implementing n-type and p-type implants on opposite sides of the wafer can increase the breakdown voltage of HV-CMOS detectors. Two high resistivity wafers were fabricated and each wafer was backside processed with one of the investigated methods to test their validity. No topside n-type isolation method was implemented as p-spray is not available in this technology. I - V measurements of fabricated samples exhibit breakdown voltages > 600 V, higher than current state-of-the-art HV-CMOS detectors. There is a need therefore to investigate p-spray options for future submissions. This will need to counteract inversion layers that would form due to the intrinsic positive charge of surface oxides, but also take into account additional positive charge that is accumulated due to irradiation by ionising radiation.

Abbreviations

ABA Approximate Breakdown Analysis. Method used in Synopsys Sentaurus TCAD simulations to evaluate the breakdown voltage of devices.

ALICE A Large Ion Collider Experiment. Experiment at the LHC.

ASIC Application Specific Integrated Circuit.

ATLAS A Toroidal LHC ApparatuS. Particle detector experiment at CERN.

BI Beamline Implantation.

CERN European Organisation for Nuclear Research (French: Conseil Européen pour la Recherche Nucléaire).

CLFV Charged Lepton Flavour Violation.

CMOS Complementary Metal-Oxide-Semiconductor.

CMP Chemical Mechanical Polishing.

CMS Compact Muon Solenoid.

CR Clean-up Ring. Inner ring in the CTS.

CTR Current Terminating Ring. Outer ring in the CTS.

CTS Current Terminating Structure.

DE Dark Energy.

DM Dark Matter.

DNTUB Deep n-well in ams technology.

DNWELL Deep n-well in LFoundry 150 nm technology.

DPTUB Deep p-well in ams H35 technology.

ELT Enclosed Layout Transistor.

e-TCT Edge Transient Current Technique.

FASER ForwArd Search ExpeRiment. Particle detector experiment at CERN.

FCC Future Circular Collider.

FE-I4 Front-End readout chip developed for the ATLAS experiment.

FE-I3 Front-End readout chip developed for the ATLAS experiment.

FLUKA Fluctuating Cascade (German: FLUktuierende KAskade). Monte Carlo simulation package.

FWHM Full Width at Half Maximum.

GDS Graphic Design System. File format of IC photomasks.

GR General Relativity.

H35DEMO Pixel DEMOnstrator device produced in the 0.35 μm HV-CMOS technology from ams AG (H35).

HL-LHC High-Luminosity Large Hadron Collider.

HV-CMOS High-Voltage Complementary Metal-Oxide-Semiconductor.

IBS Ion Beam Services.

IC Integrated Circuit.

ICWBEV IC WorkBench Edit/View. Tool for driving TCAD simulations from GDS layout files from Synopsys Sentaurus.

ID Inner Detector of the ATLAS experiment.

IIC Ionization Integrals with Carriers analysis. Method used in Synopsys Sentaurus TCAD simulations to evaluate the breakdown voltage of devices.

ILD Inter-Layer Dielectric in CMOS processes.

IMD Inter-Metal Dielectric in CMOS processes.

IT Inner Tracker. HL-LHC upgrade of the innermost silicon detector of the CMS experiment.

ITk Inner Tracker. HL-LHC upgrade of the innermost silicon detector of the ATLAS experiment.

ITS Inner Tracking System in the ALICE experiment at the LHC.

ITS2 Inner Tracking System 2. Upgrade of the ITS in the ALICE experiment at the LHC.

JSI Jožef Stefan Institute.

LA Laser Annealing.

LDF Lateral Diffusion Factor. Quantity used in Synopsys Sentaurus Structure Editor TCAD simulations.

LFV Lepton Flavour Violation.

LHC Large Hadron Collider.

LHCb Large Hadron Collider beauty. Experiment at the LHC.

LHCf Large Hadron Collider forward experiment. Particle detector experiment at CERN.

LS2 Long Shutdown 2 of the LHC, started in December 2018.

LS3 Long Shutdown 3 of the LHC, currently scheduled for 2026.

LS4 Long Shutdown 4 of the LHC.

LSP Lightest Supersymmetric Particle.

MAPS Monolithic Active Pixel Sensor.

MC Monte Carlo.

MoEDAL Monopole and Exotics Detector At the LHC. Particle detector experiment at CERN.

MOS Metal-Oxide-Semiconductor capacitor.

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor.

MPW Multi-Project Wafer.

Mu3e Particle physics experiment searching for charged lepton flavour violation in the muon to two positrons and one electron decay.

MuPix8 8th iteration of the MuPix HV-CMOS detector for the Mu3e experiment.

MuPix8/ATLASPix1 HV-CMOS particle detector submission shared between MuPix8 and ATLASPix1.

NISO Medium depth n-well in LFoundry 150 nm technology.

NMOS N-channel Metal-Oxide-Semiconductor.

NTUB N-well in ams aH18 technology.

NWELL N-well in LFoundry 150 nm technology.

OPC Optical Proximity Correction.

PCB Printed Circuit Board.

PDK Process Design Kit.

PEB Premature Edge Breakdown.

PET Positron Emission Tomography.

PIII Plasma Immersion Ion Implantation.

PMOS P-channel Metal-Oxide-Semiconductor.

PSI Paul Scherrer Institut.

PSUB Deep p-type layer in 150 nm technology from LFoundry.

PTUB P-well in ams aH18 technology.

PWELL P-well in LFoundry 150 nm technology.

R2 Run 2 of the LHC. 2015-2018.

R3 Run 3 of the LHC. Started July 2022.

R4 Run 4 of the LHC. Currently scheduled for 2029.

RD50 Research & Development group 50 within CERN.

RD50-MPW1 Device produced in the 150 nm HV-CMOS technology from LFoundry produced within the RD50 collaboration.

RD50-MPW2 Second iteration of particle detector prototype produced within the RD50 collaboration in the 150 nm HV-CMOS technology from LFoundry.

ROOT Rapid Object-Oriented Technology. Data analysis framework.

RTA Rapid Thermal Annealing.

SEU Single-Event Upset.

SIMS Secondary-Ion Mass Spectrometry.

SM Standard Model.

SMU Source Meter Unit.

SNR Signal-to-Noise Ratio.

SNTUB Shallow n-well in ams H35 technology.

SPAD Single-Photon Avalanche Diode.

SPTUB Shallow p-well in ams H35 technology.

SRH Shockley-Read-Hall.

STI Shallow Trench Isolation. Used in CMOS processes.

TCAD Technology Computer-Aided Design.

TCT Transient Current Technique.

TMR Triple Modular Redundancy.

ToE Theory of Everything.

TOTEM TOTal Elastic and diffractive cross section Measurement. Particle detector experiment at CERN.

UKRI UK Research and Innovation.

UKRI-MPW0 Backside biased sensor designed by University of Liverpool HV-CMOS group in LFoundry 150 nm technology.

WWW World Wide Web.