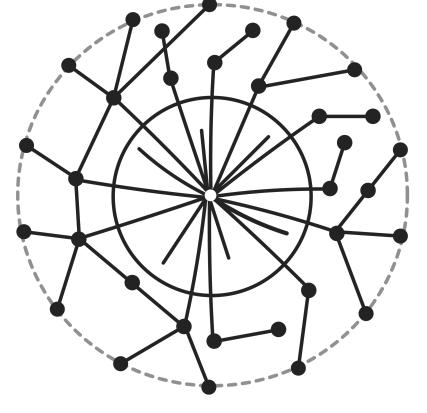


# High Speed data scouting

Exploring RoCE and 400G Ethernet for CMS Level-1 Trigger Scouting



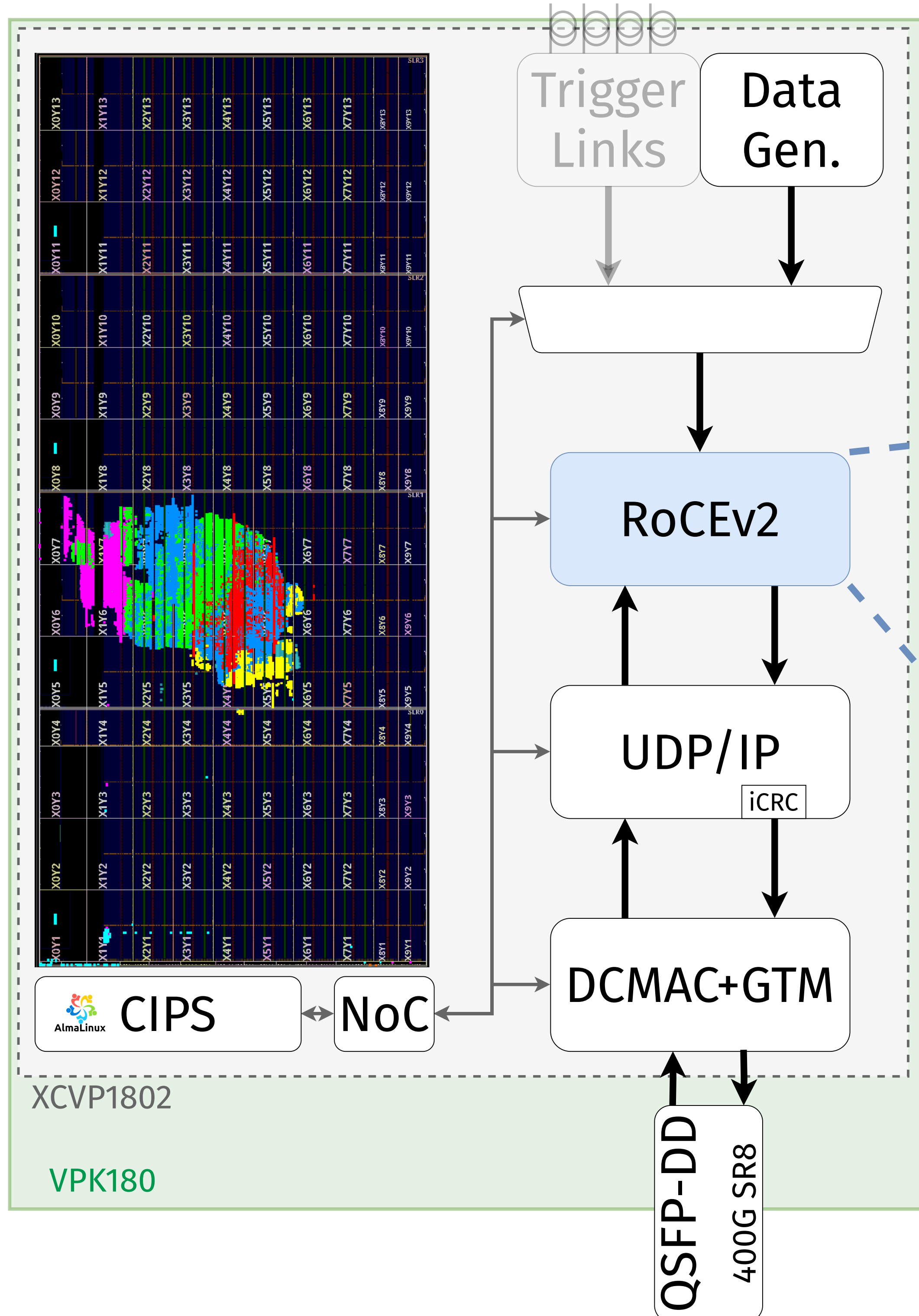
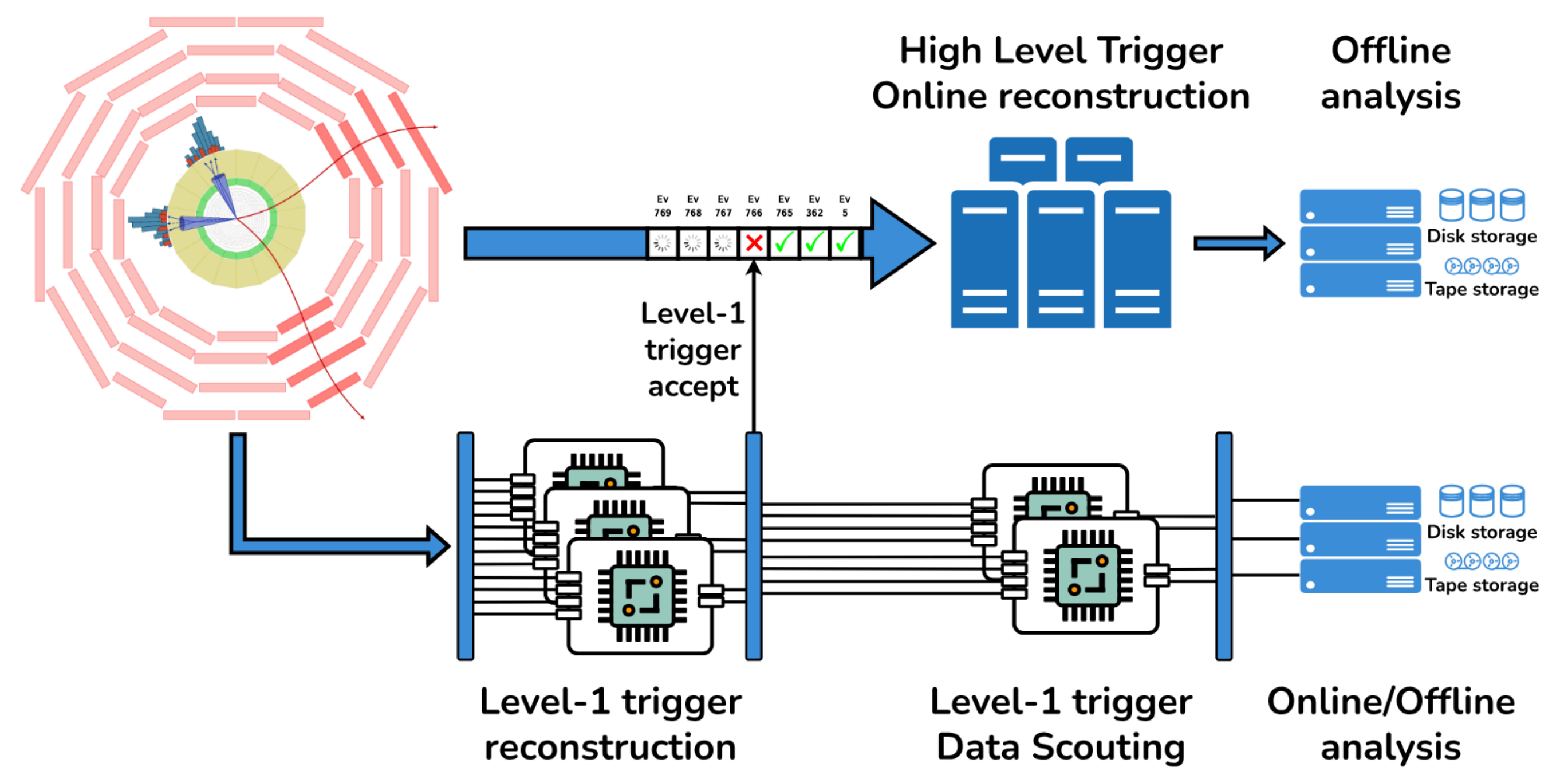
NextGen

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<sup>1</sup>CERN, <sup>2</sup>University and INFN Padova

**L1-Trigger Data Scouting:** collect and analyze objects reconstructed by the L1T processors at 40MHz  
⇒ Explore signatures evading the trigger chain  
⇒ Demonstrator during LHC Run3, full system for HL-LHC

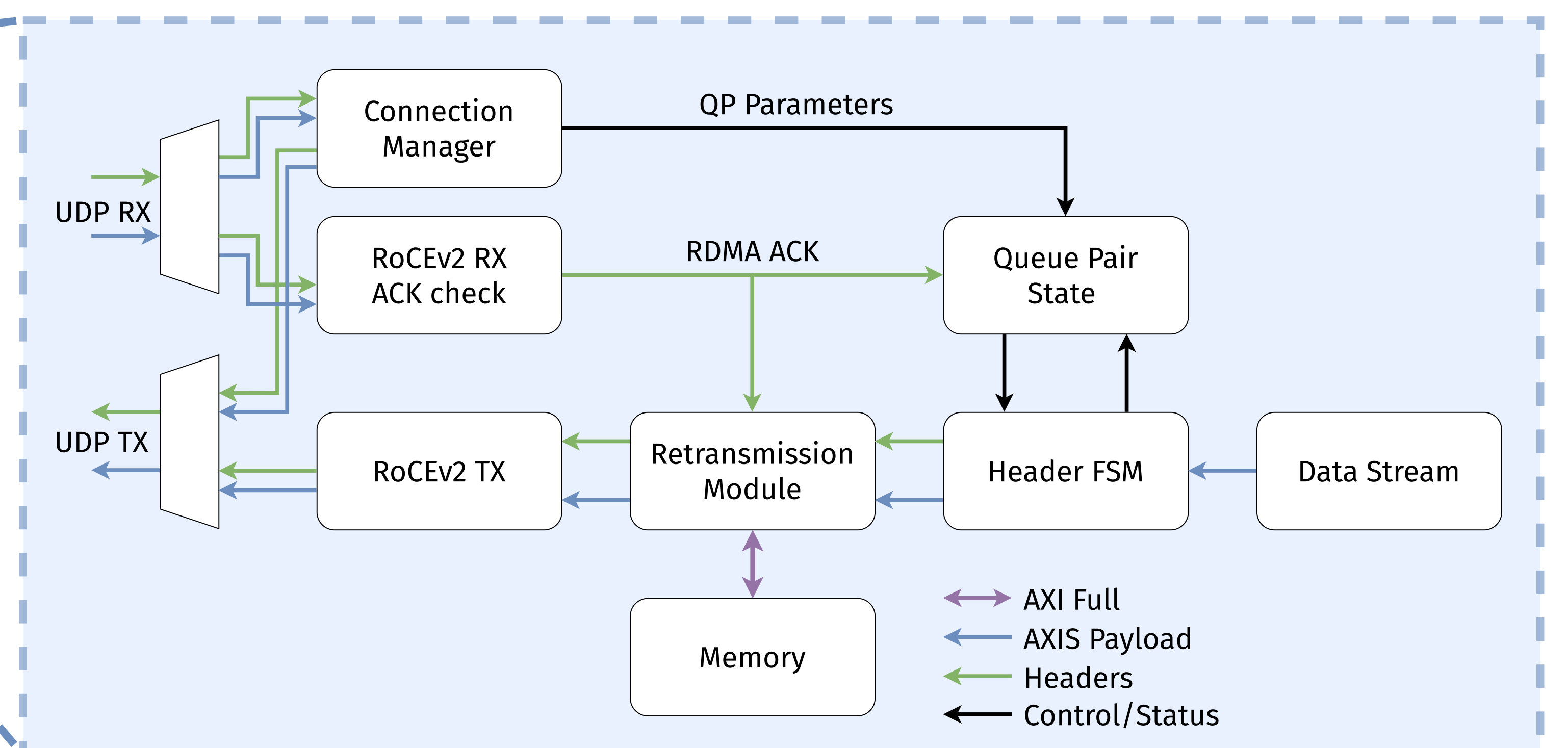
**Next Generation Trigger** project: extend the capabilities and physics reach of the L1 scouting system  
⇒ More inputs from the trigger to be processed, larger DAQ bandwidth needed (~7 Tbps)  
⇒ Designing a **DAQ board** using new FPGAs (**versal**) and exploring new network technologies (**RoCEv2**)



Developed firmware based on the **FeROCE** network stack (Front-end RDMA over Converged Ethernet) [G. Bortolato et al 2024 JINST 19 C03038]

⇒ Implemented on the **VPK180** evaluation board and scaled to **400Gb**.

⇒ In the Versal CIPS, Linux (Alma9) runs an application using IPbus for control and monitoring.



Resource utilization: 120k LUT, 230k Regs, 120 BRAM, 138 URAM  
⇒ Resource utilization can be significantly reduced (e.g. rework DCMAC axis segmented interface, smaller FIFOs, ...)

Tested with a data generator, sending fixed-size messages  
⇒ Receiver memory allocated to **DDR** or **GPU memory**  
⇒ **CPU utilization negligible** during the data transfer thanks to the remote direct memory access (Kernel bypass)

