Integration and testing of readout L1DDC boards at BB5 laboratory for New Small Wheel Upgrade

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In this project we focused mostly on configuring and testing readout boards called Level-1 Data Driver Cards (L1DDC). These electronic components, among with MMFE8 boards and Address Data Driver Cards (ADDC) are integrated into micromegas detectors and strip Thin Gas Chambers in the New Small Wheel Upgrade of ATLAS Experiment.

I. INTRODUCTION

ATLAS is one of the four main experiments in the Large Hadron Collider (LHC) at CERN. During the period from 2019 to 2020 called Long Shutdown 2, muon stations of ATLAS called Small Wheel will be replaced by New Small Wheel (NSW) Upgrade. Among all others, the new detectors consist of resistive micromegas and the small-strip Thin Gap Chambers (sTGC). To read out the large number of electronic channels that carry experimental data and in order to survive harsh experimental conditions, new electronics is fabricated and installed. The NSW micromegas double wedge with the locations of the electronic cards is shown in Figuure 1. Our main focus were L1DDC boards. The L1DDC is an intermediate

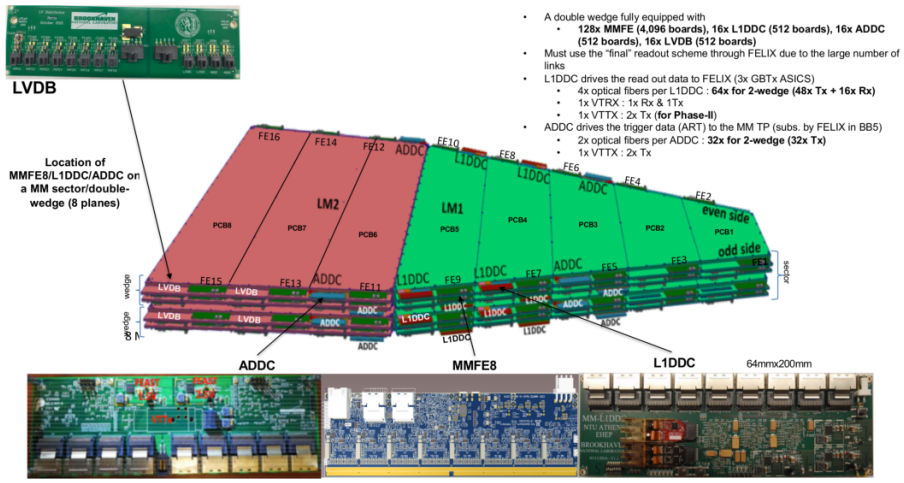

FIG. 1. NSW micromegas double wedge and associated electronic cards

board that implements a bidirectional link with the USA15 and especially with FELIX software. The L1DDC is connected with eight MMFE8 and one ADDC board for the micromegas case and with three s/pFEB boards for the sTGC. In total, 1024 L1DDC boards will be used for the upgrade of the NSW (512 for the micromegas detectors and 512 for the sTGC).

II. TESTING OF THE BOARDS

Our main task was to test the performance of L1DDC boards in various conditions. First of all, the boards needed to be fused. eFuse is a technology invented by IBM which allows for the dynamic real-time reprogramming of chips and ASICs. The eFuses use electrically

programmable PMOS gate oxide anti-fuses to provide a flexible solution for performance tuning, memory repair and the updating of configuration and version data. After fusing, a set of tests must be performed in order to decide if the final L1DDC board is appropriate for the on-chamber integration. Firstly, they are sent to CERN QART (Qualty Assurance Reliability Tesitng) and Bond Laboratory for thermal testing up to 60 °C. After that, they have been put under low voltage endurance test for at least eight hours. After that, they are ready for the final testing. A typical setup for the testing procedure is shown in Fig. 2. On the one path, the PRBS data were fed to the GBT frame and were transmitted to the

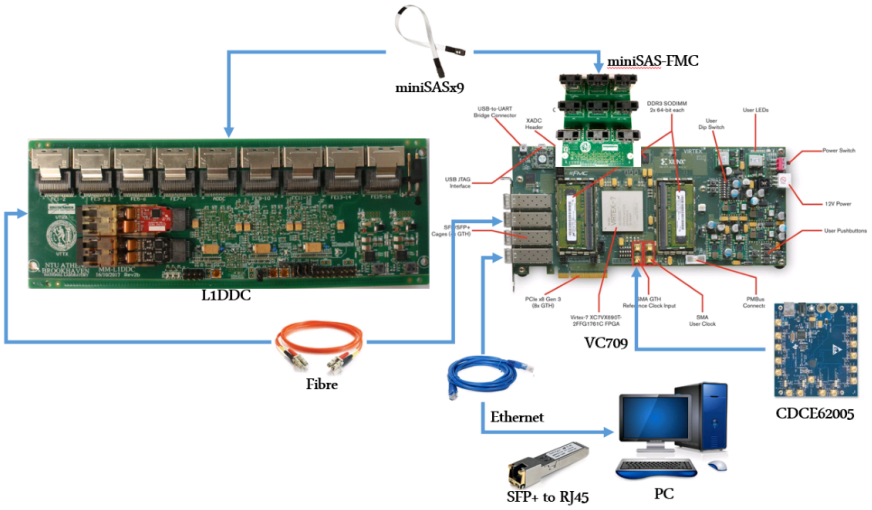

FIG. 2. Typical setup for final L1DDC testing

GBTX via the fiber (VTRX and VTTX connectors) and then via the serial lines back to the FPGA. On the other path, the PRBS data were serialized and transmitted to the GBTX via the serial lines and then to FPGA via the fiber. In both cases data were received back to the FPGA and checked for errors. The results were written in *.log* files. A PC was used to communicate with the VC709 using Ethernet and UDP packets.

III. ADDITIONAL WORK

Apart from board testing, we have taken part in New Small Wheel integration and chamber assembling. The chambers that arrived in the BB5 laboratory were positioned and aligned, assembled into wedges, on a common middle support. The twinaxial (TwinAx) cables had been recieved from the manufacturer with the connectors attached and then

covered with Kapton foil. Namely, each L1DDC board connects to eight MMFE boards of the same side layer. Also, each ADDC board connects to eight MMFE boards of the same side layer. Each L1DDC and ADDC pair are connected with a TwinAx cable. All these cables are stored inside the spacer frame for a micromegas double wedge, amounting to 272 cables inside the frame. Routing these cables is challenging, due to the limited space and the addition of structural bars between the frame plates and the central bar which does not allow easy crossing. An example of a final routed frame is shown in Fig. 3. The cables are

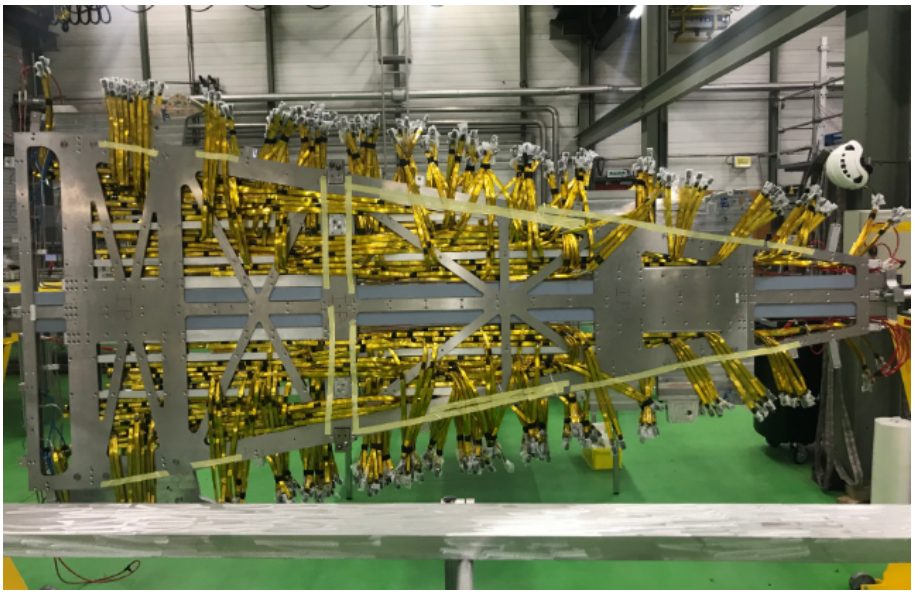

FIG. 3. TwinAx cable routing on a complete Spacer Frame

also tested for data integrity and then cleaned and protected until installation. Gas leak and high voltage test stations were employed for quality control of the chambers. There were many intermediate steps to be done until the setup is complete, such as screws and copper tape preparation, integration of the cables (LV, HV, temperature sensors) and fibers (alignment, readout) using a scheme and lastly mounting the boards to chambers. The first complete micromegas small frame is then place on a cosmic stand in order to be tested with the muons from the cosmic radiation.

IV. REFERENCES

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