

Design of a Tracking Processor Unit for LHCb Data Acquisition system

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As a Summer Student Project, the first part of the design of a Track Processor Unit (TPU) has been investigated. This short report will elaborate upon this project. The structure will be as follows: The first part will be a short introduction with the project goal, afterwards the process will be described and it will be finalized with the results.

For the HL-LHC upgrade, LHCb is going to update their Data Acquisition system (DAQ system). The proposed system is shown in Figure 1. The working of the system is quite sophisticated. The different detectors within LHCb will send data to a set of 500 Event Builder (EB) nodes via fiber optics. Every EB node will receive data from a certain (part of the) detector. The job of the EBs is to package this data from all different detectors in packages which contain all detector data from a certain set of events. So the EBs will convert the event information from per detector data to per event data. This process is called event building.

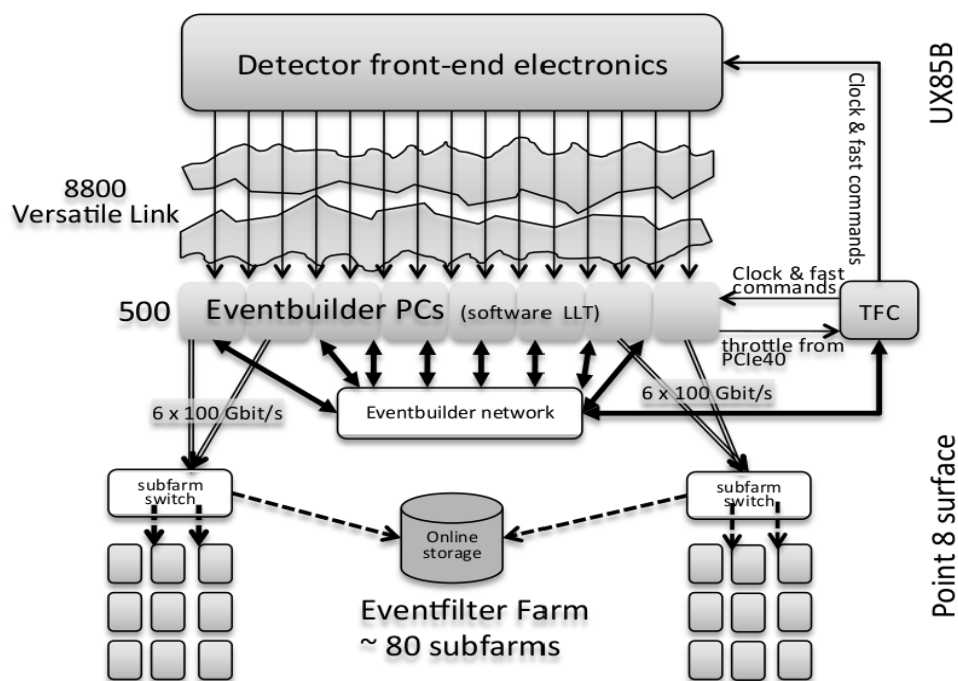


Figure 1: Schematic view of the proposed DAQ system for HL-LHCb upgrade.

The implementation of the event building algorithm is as follows: One EB node is elected to build a certain set of events. All EB nodes having data of this set of event send this data to the elected node, after which the elected node will combine the data and send it to the Event Filter Farm (which does triggering in software). This process of Event Building is very memory intensive because the data stream can be up to 100 Gb/s. So a large amounts of data are written to and read from EBs main memory.

The LHCb collaboration is investigating the possibility to add an extra accelerator to the EBs. A subset of EB nodes will get a PCI-Express expansion card. This card, which in this research is based upon an FPGA (but different kind of accelerator could be used as well), will run the Artificial Retina algorithm¹ to do already some partial track reconstruction within the EB nodes. This accelerator is therefor called the Tracking Processor Unit (TPU). The TPU will get the detector data out of main memory via Direct Memory Access (DMA) transaction and will write data back to main memory via DMA transactions as well. Within the current system, the data of the detectors is written to the main memory of the event builders via DMA as well (by the so called PCIe40 expansion card), but the transactions are only one way. The goal of the summer student project is to make a demonstration setup to perform this two-way DMA by a given FPGA PCIe expansion card (Bittware A5PL). It is required that the firmware (digital design) of the FPGA and the drivers for the TPU are based upon the firmware and drivers for the already existing PCIe40.

The process for making such a setup would be to first port the existing firmware to the given FPGA expansion board as well as porting the simulation environment to the given device family. Afterwards the drivers should be altered such they support two way DMA transactions and finally the firmware should be altered as well to support two way DMA. If that all is done, a short demonstration program should be written which demonstrates two-way DMA transfers.

During the project is was managed to port the existing firmware to the given FPGA expansion card. Also the simulation environment was ported to the given device family, although there are still some minor issues with it. It was not managed to alter the drivers and firmware to implement two way DMA transfers. However a detailed look was given at the current structure of the drivers and firmware such that it is know what should be changed. This has been documented firmly. Also some proper high level documentation has been written about the existing firmware and drivers (which was basically non-existing) such that someone can easily continue this research project without the need to found out how the system works her/himself.

¹ For more information about the Artificial Retina algorithm, see for example:

- Abba, G. Punzi, F. Spinella, P. Marino, D. Tonelli, S. Stracka, F. Lionetto, D. Ninci, M. Petruzzo, A. Cusimano, et al. A specialized track processor for the LHCb upgrade. Technical report, 2014.
- L. Ristori. An artificial retina for fast track finding. Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 453(1-2):425– 429, 2000.