
Development and Reliability Testing of a new Low-Voltage Power Supply for the ATLAS Hadronic Tile-Calorimeter Phase-II Upgrade



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Declaration

I, Ryan Peter Mckenzie, (Student number: 732595) declare that this thesis titled, “Reliability testing and upgrade of a low voltage power supply for the front-end electronics of the ATLAS Tile Calorimeter Phase-II Upgrade”, is submitted in fulfillment of the requirements for the Degree of Doctor of Philosophy, represents my own work except where appropriate acknowledgement has been given.

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It is an unfortunate fact that all PhD. graduates are unable to distill their profound thanks and appreciation for all of those individuals who have played a part in their development into a mere page (or two). I too find myself in this position and therefore dedicate my thesis to every individual who has offered their time willingly and for the only purpose being that of assisting a young researcher.

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Research Outputs

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CONFERENCES:

- **Mckenzie R. on behalf of the University of the Witwatersrand Institute for Collider Particle Physics**, LV bricks at Wits. Status of pre-production and plans toward PRR , TileCal Collaboration Week, CERN, 11th June 2024.
- **Mckenzie R. on behalf of the Tile-Calorimeter System**, Tile Phase-II Upgrade Status, ATLAS Collaboration Week, CERN, 15th February 2024.

- **Mckenzie R. on behalf of the Tile-Calorimeter System**, Tile Status Report, ATLAS Collaboration Week, CERN, 13th February 2023.
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Deep-Inelastic Scattering , Stony Brook University, 2021. Accepted for publication.

- **Mckenzie R.** The Burn-in testing of advanced custom low-voltage power supply components within ATLAS TileCAL testing facilities, 5th International conference on particle physics and astrophysics, online, 2020.
- **Mckenzie R.** A new low-voltage power supply for the ATLAS TileCal front-end electronics, Seventh Common ATLAS CMS Electronics Workshop for LHC Upgrades, Online, 2020.

Author's Contribution

This thesis is the result of the author's contribution as part of the University of the Witwatersrand, Institute of Collider Particle Physics towards the ATLAS TileCal Phase-II Upgrade. The author was specifically involved in the Phase-II Upgrade activities of the Low Voltage Power Supply system and in particular the thermal performance study of the Phase-II Upgrade Brick. The author contributed to the radiation hardness certification of a key active component that was selected due to the findings of the thermal performance study. A reliability analysis was subsequently undertaken by the author to determine the predicted annual failure rate of the Phase-II upgrade variant that incorporated the design changes recommended by the High-efficiency Brick studies. The author was also heavily involved in the development of the quality assurance procedure that is to be applied post-manufacturing of the Phase-II Upgrade as well as a key custom apparatus known as the Burn-in station and its procedure that it is charged with applying to the Bricks. Finally, the author is currently overseeing the pre-production and quality assurance testing of the V8.6.0 Phase-II Upgrade Brick in South Africa.

Preface

The Large Hadron Collider (LHC), located at the Conseil Européen pour la Recherche Nucléaire (CERN) also known as the European Laboratory of Particle Physics, is a two-ring-superconducting-hadron accelerator and collider located on the Franco-Swiss border. The LHC was successfully commissioned in 2010 for proton–proton collisions and is expected to deliver 500 fb^{-1} before Long Shutdown three (LS3) that is schedule to commence in 2026.

Its successor, the HL-LHC, will provide a levelled instantaneous luminosity of $\mathcal{L} = 5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ and is projected to deliver an integrated luminosity of more than 4000 fb^{-1} to its two general purpose detectors, known as A Toroidal LHC Apparatus (ATLAS) and Compact Muon Solenoid (CMS), over a span of 10 years. The main motivation to upgrade the LHC is to fully exploit its physics potential. Through a series of machine and detector upgrades, it is possible to increase the instantaneous luminosity. This could unlock many of the physics processes that are today inaccessible to the LHC because of the lack of statistics. The primary impacts of the HL-LHC on the detector environment are a direct consequence of an increase in delivered instantaneous luminosity.

The ATLAS experiment will undergo its Phase-II Upgrade during Long-Shutdown 3 to ensure peak performance during high-luminosity operations. ATLAS is composed of several specialized sub-detectors one of which is the hadronic Tile-Calorimeter (TileCal). The TileCal will undergo numerous upgrades one of which will be to the Low-Voltage (LV) power distribution system that services its on-detector electronics. The on-detector finger Low-Voltage Power supplies form the second stage of the LV system. Their primary functional device is a transformer-coupled buck converter, known as a Brick, which is responsible for converting bulk power to that required by the on-detector electronics. All legacy Bricks will be replaced with a new version that employs several design changes to enable their reliable operation within the HL-LHC detector environment.

In this thesis, the development of the Phase-II Upgrade Brick is presented with an emphasis placed on its thermal performance and reliability. A thermal analysis of the proposed upgrade Brick versions is presented with design changes occurring as a result. Due to the design change incorporating a new active component an irradiation campaign is conducted to qualify it for use within the high-luminosity detector environment. A reliability analysis of the Phase-II upgrade Brick is conducted necessitated by the change of many critical components. The quality assurance procedure of the Bricks that is undertaken post-production is presented with particular attention placed on their Burn-in testing.

Research Context and Rationale

In the first quarter of 2029, the start of the operation of the High Luminosity Large Hadron Collider (HL-LHC) is planned. The resulting environment has necessitated the development of new electronics, both on- and off-detector, to ensure the continued peak performance of the ATLAS experiment. The development, testing, production, quality assurance testing, installation and commissioning of new electronics falls under the Phase-II upgrade. The Hadronic Tile-Calorimeter (TileCal) is a sub-detector of ATLAS. The TileCal performs several critical functions within ATLAS such as: the measurement and reconstruction of hadrons, jets, hadronic decays of τ -leptons and missing transverse energy. It also participates in muon identification and provides inputs to the Level-1 calorimeter trigger system.

The TileCal will be undergoing an upgrade of its low-voltage power distribution system amongst numerous other upgrades. This system is responsible for the reliable delivery of low-voltage power to the on-detector readout electronics. A key element of this system is the finger Low-Voltage Power Supply (LVPS) Brick. A Brick functions to step-down bulk power received from off-detector power supplies to the power required by the Phase-II upgrade front-end electronics.

The LVPS Brick Phase-II upgrade is equally shared in its entirety between South Africa and the United States of America as per the signed memorandum of understanding between the respective countries and CERN, the European Organization for Nuclear Research. As per this agreement, South Africa has committed to the development, production, quality assurance testing, and installation of 1024 Bricks within the TileCal.

Objectives

The overarching intent of the research herein contained is the completion of the South African responsibilities to the TileCal Phase-II upgrade. These objectives can be subdivided into the following broad categories each of which will be addressed throughout the course of this thesis:

- The development and completion of the TileCal Phase-II Upgrade finger Low Voltage Power Supply Brick. This includes all secondary objectives required for design completion such as radiation hardness certification, thermal optimization, and reliability analysis of the Brick.
- The development of a quality assurance procedure to be used during the Brick production to ensure high reliability.
- The development of a custom Burn-in station for the Phase-II Upgrade Brick quality assurance procedure.
- The successful Pre-production of the Phase-II Upgrade Bricks in South Africa.

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Chapter 1

The ATLAS Experiment at the High Luminosity Large Hadron Collider

1.1 The Large Hadron Collider Machine

The Large Hadron Collider (LHC), situated at the European Laboratory of Particle Physics (CERN), is a dual-ring superconducting hadron accelerator and collider [1]. Representing the newest component of CERN's accelerator complex, depicted in Figure 1.1, the LHC serves as the final stage in a series of particle accelerators that act as its pre-accelerators. Its primary objective is to investigate particle physics phenomena at energy levels and luminosities previously unattainable.

The LHC was successfully commissioned in 2010 for proton–proton collisions with a centre-of-mass energy of $\sqrt{s} = 7 \text{ TeV}$, which progressively increased to $\sqrt{s} = 13 \text{ TeV}$ during Run 2 with a peak value of $\sqrt{s} = 13.6 \text{ TeV}$, and peak instantaneous luminosity of $\mathcal{L} = 20.04 \times 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$ having been recorded during the Run 3 that commenced in July of 2022. The LHC also collides heavy ions, in particular lead nuclei, at 5.5 TeV per nucleon pair, at a design luminosity of $\mathcal{L} = 10^{27} \text{ cm}^{-2} \text{ s}^{-1}$. By design, the two counter rotating beams cross at the four Interaction Points (IPs) located along the circumference of the LHC. A specialized detector is positioned around each of the IPs. These are: A Toroidal LHC Apparatus (ATLAS) [2], the Compact Muon Solenoid (CMS) [3], A Large Ion Collider Experiment (ALICE) [4] and the Large Hadron Collider beauty (LHCb) [5] experiment. ATLAS and CMS are multipurpose detectors designed to test the standard model and search for new physics at the TeV scale. ALICE specialises in heavy-ion physics and LHCb focuses on B-meson physics.

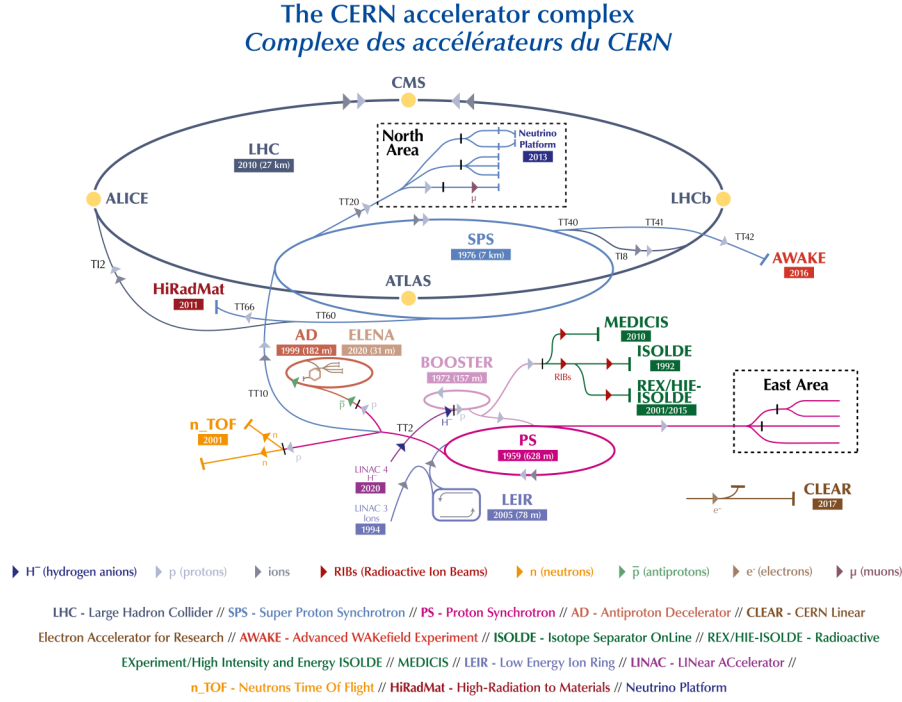


Figure 1.1: The CERN accelerator complex, layout in 2022 [6].

1.1.1 Beam Cycle of a Nominal Large Hadron Collider Fill

The Large Hadron Collider beams are not continuous in nature but are rather a composition of discrete successive particle clouds known as bunches. The structure of the bunches within a beam is referred to as its filling scheme. This topic will be covered in subsection 1.1.2. There are multiple beam modes that in succession to form a successful beam cycle. These are SETUP, INJPROT, INJPHYSICS, RAMP, FLATTOP, SQUEEZE, ADJUST, STABLE, and BEAMDUMP that can be observed in Figure 1.2. SETUP is the mode during which the new parameters for the beam are prepared for the next cycle. INJPROT is the mode during which the protons are injected into the SPS. INJPHYSICS is the mode in which the beams of 450 GeV are injected into both beam-pipes of the LHC. Different filling schemes are possible in the LHC. See subsection 1.1.2. RAMP is the mode in which the beams are accelerated up to 6.8 TeV (13.6 TeV center-of-mass energy at IP). FLATTOP is the mode when the energy cannot be increased anymore. SQUEEZE is the mode in which the beam optics at the experiments are manipulated. ADJUST is the mode in which the first collisions take place. Finally STABLE beams are declared and proton-proton collisions commence. Over time the intensity of the beams ("number of protons") reduces which is known as burn-off. Eventually the beams are deemed to be too depleted to allow for efficient data taking and a BEAMDUMP is initiated. If at any point sub-optimal conditions are detected a BEAMDUMP (both beams are kicked into a

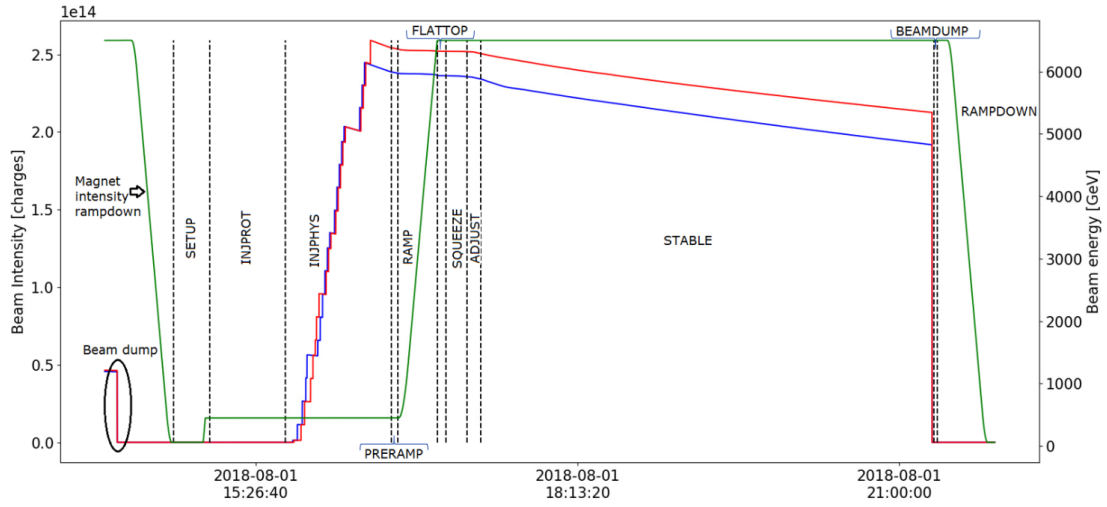


Figure 1.2: LHC Cycle of a nominal fill (fill 7006). The intensity of Beam 1 and Beam 2 is represented in blue and red, respectively. The the energy of the beams over the entire cycle is represented in green. The dashed black lines represent the transition between beam modes. The name of each beam mode is placed between two dashed black lines [7].

beam-dump at IP6 where they deposit their energy) will be immediately initiated. During nominal operation the LHC runs consecutive fills one after another in order to deliver the maximum possible luminosity to the detectors which then attempt to record as much proton-proton collision data as possible.

1.1.2 LHC Filling Schemes

The LHC has various filling schemes with each representing a specific mode of operation. The two primary modes are attributed to whether the LHC is accelerating either protons or heavy-ions. There are multiple filling schemes for each of the primary modes each of which being providing different machine performance [8].

In the case of proton operation for maximal luminosity, a beam is filled with up to 2808 bunches of 1.15×10^{11} protons spaced by at least 25 ns.

The bunches are grouped in trains that are separated by gaps. At the end of the filling scheme there is a long gap (10 μ s) that allows the RF cavities of the LHC to recharge their energy as well as allowing for the LHC beam-dump kicker magnets rise time. This gap colloquially referred to as the "abort gap". The revolution time of the LHC is known as an orbit which lasts 89 μ s. An example of a 25 ns filling scheme employed on the 7th of July 2023 is provided in (2.1) below:

$$25ns_2464b_2452_1842_1821_236bpi_12inj_hybrid \quad (1.1)$$

The convention for naming standard filling schemes is applied in (2.1). That is, 25 ns refers to the bunch spacing and 2464b refers to total number of bunches within a beam. The sequence of numbers 2452_1842_1821 indicates the number of colliding bunches at ATLAS/CMS, ALICE and LHCb, respectively. They few non-colliding bunches are required for beam stability. There are 11 trains in this filling scheme where bpi stands for “bunches per injection” and 12inj refers to the number of injections per beam.

Multiple hard-scattering interactions per bunch-crossing (μ) can occur in the center of the IPs. This can be tuned by several parameters of the beam operation. This can potentially lead to large occupancy of the front-end electronics in the experiments, and this effect is known as pile-up.

1.2 The Large Hadron Collider Injectors Upgrade

The LHC Injectors Upgrade (LIU) project has the ultimate goal of making the injectors capable of reliably delivering the beams required by the High Luminosity LHC (HL-LHC) [9]. To achieve this target, the intensity of the injected beam has to be doubled, and its brightness multiplied by 2.5 (2.3×10^{11} p/b with 25 ns bunch spacing within emittances of $2.1 \mu\text{m}$). The LIU successfully took place during the Long-Shutdown 2 (LS2) in which numerous upgrades to the accelerator complex were made. The Linear Accelerator 4 (Linac4) was integrated into the injector complex with an increase the energy of the Proton-Synchrotron Booster to reduce the beam emittance also being undertaken. An upgrade to the collider collimation system was also made.

1.3 The High-Luminosity Large Hadron Collider Machine

All of the hadron colliders in the world preceding the LHC have produced a combined total integrated luminosity of about 10 fb^{-1} . In contrast the LHC delivered nearly 30 fb^{-1} by the end of 2012 data taking and is expected to deliver 300 fb^{-1} before Long Shutdown three (LS3) that is schedule to commence in 2026. The HL-LHC will provide a levelled instantaneous luminosity of $\mathcal{L} = 5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ and is projected to deliver an integrated luminosity of more than 4000 fb^{-1} over a span of 10 years of operation as illustrated in Figure 1.3.

1.3.1 Luminosity

After the collision energy that sets the limit of the particles that can be produced in the event, the luminosity is the most important parameter of a collider, because it is proportional to the number of particles that are produced:

$$N_{process} = \sigma_{process} \int \mathcal{L}_{Int} dt \quad (1.2)$$

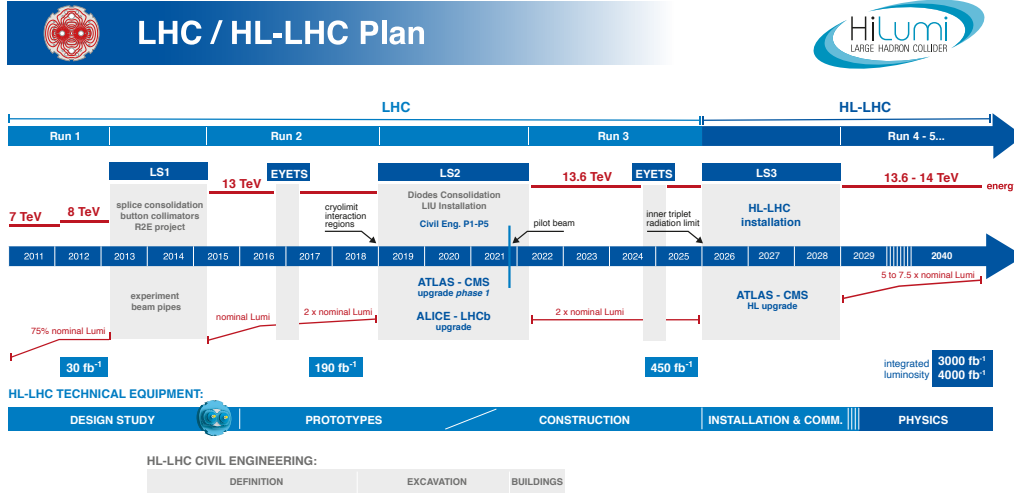


Figure 1.3: LHC / HL-LHC Plan updated in February 2022.

where $N_{process}$ is the number particles for any particular process and $\sigma_{process}$ is the cross-section for that process.

The (instantaneous) luminosity $\mathcal{L}$ can be expressed in units of inverse number of events per unit time as:

$$\mathcal{L} = \gamma \frac{n_b N^2 f_{rev}}{4\pi\beta^* \varepsilon_n} R; \quad R = \frac{1}{\sqrt{1 + \frac{\theta_c \sigma_z}{2\sigma}}} \quad (1.3)$$

where γ is the proton beam energy in unit of rest mass; n_b is the number of bunches per beam; N is the number of bunches populated; f_{rev} is the revolution frequency; β^* is the focal length of the collision point ε_n is the transverse normalized emittance; R is a luminosity geometrical reduction factor; θ_c is the full crossing angle between colliding beam; and σ , σ_z are the transverse and longitudinal RMS sizes, respectively.

For physics purposes, luminosity integrated over time is the relevant parameter. Unfortunately, integrated luminosity does not solely depend on LHC machine performance (time of operation), but also on many external parameters including injector performance, availability and quality of technical services, and the detector's capability of recording events. Figure 1.4 illustrates the variance between the luminosity provided by the LHC and the luminosity detected by ATLAS. It displays the cumulative luminosity over time delivered to (green) and recorded by ATLAS (yellow) during periods of stable beams for proton-proton collisions at 13.6 TeV. The delivered luminosity encompasses the luminosity provided from the initiation of stable beams until the LHC instructs ATLAS to transition the detector into a safe standby mode, facilitating either beam dump procedures or beam studies. The detected luminosity accounts for both the inefficiency of

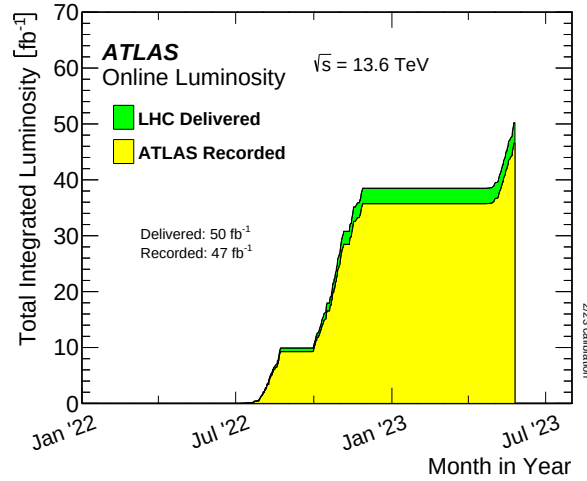


Figure 1.4: Cumulative luminosity versus time delivered to (green) and recorded by ATLAS (yellow) during stable beams for p-p collisions at 13.6 TeV centre-of-mass energy in LHC Run 3 (2022-2023).

the data acquisition system (DAQ) and what is known as the ‘warm start’ inefficiency. This refers to the period when the stable beam status is initiated, during which the tracking detectors experience a ramp-up of high-voltage operations, and for the pixel system, the activation of preamplifiers. The presented luminosity data is based on a preliminary calibration for 13.6 TeV, derived from van-der-Meer scans conducted in 2022.

1.3.2 Upgrade Motivation

The main motivation to upgrade the LHC is to fully exploit the physics potential of the LHC. Through a series of machine and detector upgrades, it is possible to increase the instantaneous luminosity, the number of interactions per bunch-crossing, and the interesting physics events keeping the detector acceptance close to 100% [10]. This could unlock many of the physics processes that are today inaccessible to the LHC because of the lack of statistics. For example, the Higgs self-interaction which is a process described by the standard model and expected since the discovery of the Higgs, is 2 orders of magnitude less likely than any other standard model process. Not to forget that in the current economic situation, an upgrade of the LHC is far more accessible than a complete redesign and production of and accelerator, as proposed by the Future Circular Collider.

1.3.3 Consequences of High Luminosity

Achieving Higher Luminosity

The number of bunches circulating in the LHC cannot be substantially increased due to multiple contributing factors from the injector chain such as beam impedance and beam-beam interactions in the LHC [11]. In order to realize the luminosity requirements

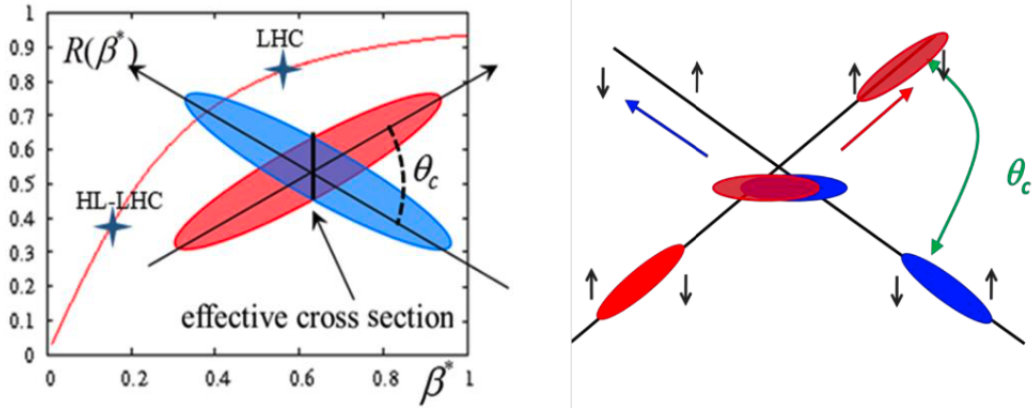


Figure 1.5: (Left) Effect of geometrical reduction factor, as defined in Equation 1.3, on luminosity vs. β^* with two operating points shown: nominal LHC and HL-LHC. The sketch of bunch crossing shows the reduction mechanism. (Right) Effect of the crab cavities on the two beams [14].

of the HL-LHC the number of protons per bunch (beam brightness) of the LHC needs to be increased while also reducing the value of the beams focal length at the IP (β^*).

The LHC beam brightness is dependant on the performance of the accelerators of the injector complex. The LHC Injectors Upgrade (LIU) project has the ultimate goal of making the injectors capable of reliably delivering beams with a brightness of 2.3×10^{11} protons per bunch as required by the HL-LHC. The project covers Linac4 and the upgrades of the Proton Synchrotron Booster (PSB), the Proton Synchrotron (PS) and the Super Proton Synchrotron (SPS) [9].

The reduction of β^* at ATLAS and CMS will be achieved by means of stronger and larger aperture low- β triplet quadrupole magnets that will be installed during LS3. [12]. The drawback of very small β^* is that it requires a larger crossing angle θ_c . With reference to Equation 1.3, it can be observed that this results in a reduction of the R geometrical factor thereby reducing the achievable instantaneous luminosity. Figure 1.5 illustrates the effect of the geometrical reduction factor on Luminosity as a function of β^* .

The non-zero crossing angle implies an inefficient overlap of the colliding bunches. Without any changes at the IPs the HL-LHC beams would experience an additional 128 parasitic collisions excluding those at the IPs due to the fact that they share a common beam pipe in the four interaction regions. The solution chosen to compensate for this effect is the use of 16 superconducting compact radio frequency deflecting (crab) cavities (2 cavities per beam per IP side = 16 total) which when used can recover upto 70% of the Peak Luminosity. The effect of crab cavities on the two beams at an IP is illustrated in Figure 1.5 (Right) in which the small arrows indicate the torque applied to the beam by transverse varying RF fields. This action rotates the bunch in the x - z (or y - z) plane about the centre-of-mass of the bunch. The kick is transformed to a relative displacement of the head and the tail of the bunch at the IP imposing a head-on collision [13].

HL-LHC Impact on Detector Environment

The primary impacts of the HL-LHC on the detector environment are a direct consequence of an increase in delivered instantaneous luminosity. The expected annual dose received by ATLAS and CMS per year in the HL-LHC era will be similar to the total dose of the 3 previous LHC runs combined providing challenges to both the legacy detector systems as well as those of the Phase-II upgrade. The increase in instantaneous luminosity also results in an increase in pileup (μ) which has a significant impact on detector performance. At the nominal luminosity of the HL-LHC, the average number of interactions in a single bunch crossing $\langle\mu\rangle = 140$ to 200. Specifications of each upgrade detector component are therefore defined for up to $\langle\mu\rangle = 200$ interactions per bunch crossing. The predicted average number of interactions per bunch crossing is calculated using the formula:

$$\langle\mu\rangle = \mathcal{L} \times \frac{\sigma_{inel}}{n_b} \times f_{rev} \quad (1.4)$$

where the total inelastic proton–proton cross section is assumed to be $\sigma_{inel} = 85$ mb at $\sqrt{s} = 14$ TeV, the LHC revolution frequency is $f_{rev} = 11.245$ KHz, and n_b is the number of colliding bunches at IP1. The benchmark scenario with $\langle\mu\rangle = 200$ is obtained assuming $n_b = 2808$ and a peak instantaneous luminosity of $\mathcal{L} = 7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$.

1.4 The ATLAS Experiment and its Upgrades

This section describes the ATLAS Experiment at the LHC, its upgrades for the HL-LHC and present a selection of reliability considerations that have to be taken into account due to ensure peak performance during high-luminosity operations.

1.4.1 The ATLAS Experiment

ATLAS is a general-purpose p-p and heavy-ion detector that was first proposed in a letter of intent in 1992 [15]. The detector design and optimization was guided by physics requirements such as sensitivity to the largest possible Higgs mass range while also having the ability to cope with a broad variety of expected physics processes thereby providing flexibility for the potential discovery of new and unexpected physics phenomena.

As shown in Figure 1.6 the ATLAS detector is located approximately 100 m underground, within the experimental cavern (UX15), at IP1 of the LHC. Its dimensions are 25 m in height and 44 m in length. The overall weight of the detector is approximately 7000 tonnes. The detector which occupies most of UX15 does not operate in isolation. Off-detector readout and control electronics as well as services are housed in the adjacent service galleries, USA15 and US15. The hardware present in these caverns benefit from the close proximity to the detector which facilitates fast and efficient communication while also being shielded from radiation allowing access during machine runs.

The detector itself is controlled and monitored twenty four hours per day by three separate shift teams, during data taking periods, in the ATLAS Control Room (ACR) which is situated on the ground floor of the main ATLAS control building (SCX1). It should also be noted that remote access to the ATLAS systems at P1 is possible thereby allowing experts to rapidly respond to changing detector conditions.

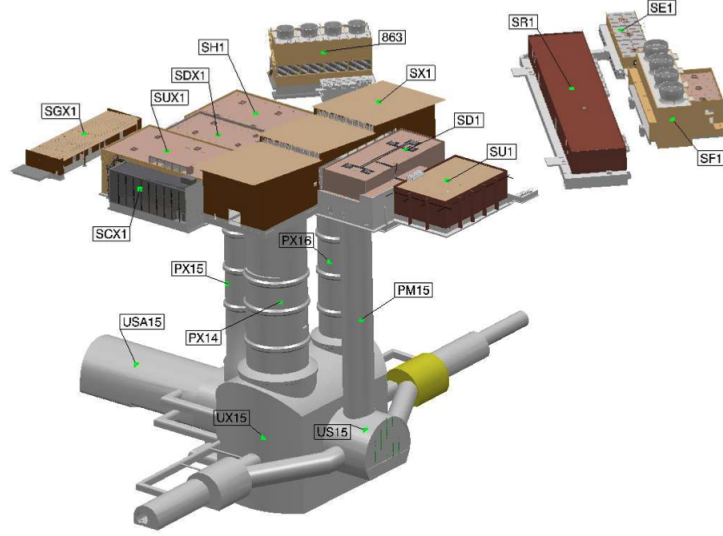


Figure 1.6: Layout of surface buildings and of access shafts to the ATLAS cavern at point 1.

As per the ATLAS letter of intent, the basic design criteria of the detector are the following:

- Due to the experimental conditions at P1 the detector requires fast, radiation-hard electronics and sensor elements.
- High detector granularity is needed to handle the particle fluxes and to reduce the influence of overlapping events.
- Large acceptance in pseudorapidity (η)¹ with almost full azimuthal angle (ϕ) coverage is required.
- Good charged-particle momentum resolution and reconstruction efficiency in the inner tracker are essential. For offline tagging of τ -leptons and b-jets, vertex detectors close to the interaction region are required to observe secondary vertices, as shown in Table 1.1.

¹ATLAS makes use of a right-handed coordinate system with its origin located at the nominal interaction point (IP) in the centre of the detector and the z-axis along the beam pipe. The x-axis points from the IP to the centre of the LHC ring, and the y-axis points upwards. Cylindrical coordinates (r, ϕ) are used in the transverse plane, where ϕ is defined as the azimuthal angle around the z-axis. The pseudorapidity is defined in terms of the polar angle θ as $\eta = -\ln \tan(\theta/2)$. Angular distance is measured in units of $\Delta \equiv \sqrt{(\Delta\eta)^2 + (\Delta\phi)^2}$.

- Very good electromagnetic (EM) calorimetry for electron and photon identification and measurements, complemented by full-coverage hadronic calorimetry for accurate jet and missing transverse energy (E_{miss}^T) measurements.
- Good muon identification and momentum resolution over a wide range of momenta and the ability to determine unambiguously the charge of high P_T muons.
- Triggering on low P_T thresholds, providing high efficiencies for most physics processes of interest at the LHC.

Detector component	Required resolution	Coverage	
		Measurement	Trigger
Tracking	$\sigma_{P_T}/P_T = 0.05\%P_T \oplus 1\%$	$ \eta < 2.5$	-
EM calorimetry	$\sigma_E/E = 10\%/\sqrt{E} \oplus 0.7\%$	$ \eta < 3.2$	$ \eta < 2.5$
Hadronic calorimetry			
Barrel/endcap	$\sigma_E/E = 50\%/\sqrt{E} \oplus 3\%$	$ \eta < 3.2$	$ \eta < 3.2$
Forward	$\sigma_E/E = 100\%/\sqrt{E} \oplus 10\%$	$3.1 < \eta < 4.9$	$3.1 < \eta < 4.9$
Muon spectrometry	$\sigma_{P_T}/P_T = 10\% \text{ at } P_T = 1 \text{ TeV}$	$ \eta < 2.7$	$ \eta < 2.4$

Table 1.1: General performance quantities of the ATLAS detector. The units for E and p_T are in GeV unless otherwise stated [16].

To fulfill the above mentioned performance goals the ATLAS detector took the form illustrated in Figure 1.7. It is a hermetic detector with bilateral symmetry about the IP and is composed of multiple sub-detectors each of which specializing in the detection of specific final state signatures as well as a hybrid magnet system.

Magnet System

The magnet system configuration had a major influence on the overall design and performance of the ATLAS detector. The purpose of the magnet sub-systems is to provide the magnetic field for the various detectors while having a structure that is light and open to reduce potential secondary scattering. A central solenoid magnet provides a 2 T axial magnetic field parallel to the beam axis which is used by the inner detector. A toroid magnet composed of a barrel section and two end-caps generate a tangential magnetic field of approximately 0.5 T and 1 T for the muon spectrometer in the barrel and end-cap regions, respectively.

Inner Detector

The Inner Detector (ID), illustrated in Figure 1.8, is designed to reconstruct tracks and decay vertices, from the primary vertex up until the electromagnetic calorimeter, for all

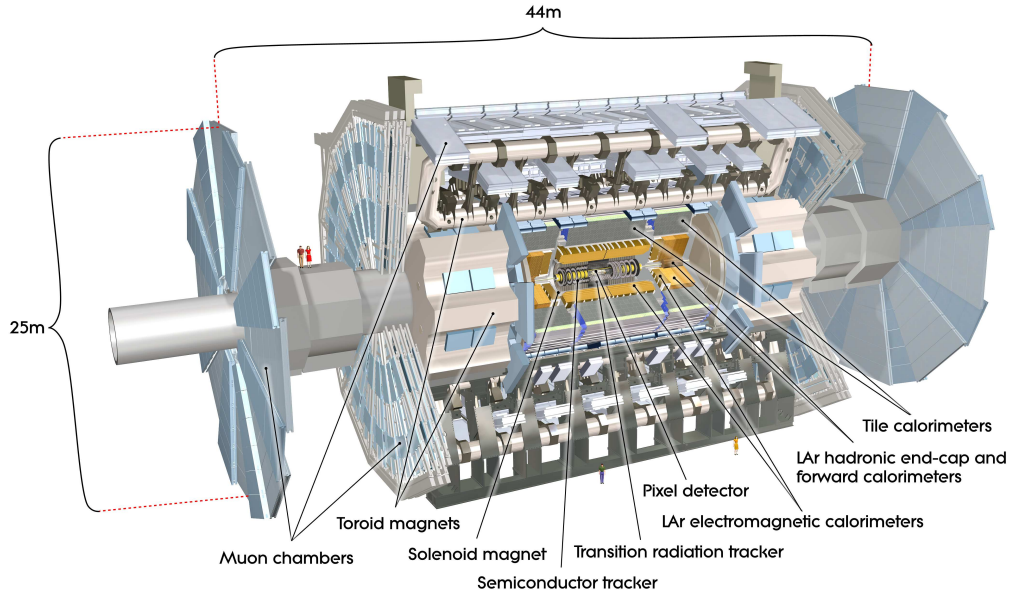


Figure 1.7: The ATLAS experiment [17].

events and with high efficiency. The inner detector also makes use of additional information from the calorimeter and muon systems allowing it to contribute to electron, photon, and muon identification. It also supplies extra signatures for short-lived particle decay vertices.

The ID is entirely contained within the central cylindrical solenoid. It combines high-resolution detectors at inner radii with continuous tracking elements at outer radii. The ID consists of three distinct sub-detectors exploiting different techniques of particle detection. These are in order of location with increasing radii from the beam-axis: the silicon Pixel detector, the SemiConductor Tracker (SCT) and the Transition Radiation Tracker (TRT) the primary parameters of which are stated in table Table 1.2 [18].

Pixel Detector

The pixel detector is designed to provide a very high-granularity, high-precision set of measurements as close to the interaction point as possible. The system initially consisted of three concentric barrel layers and four disks located on either side which complete the angular coverage. A new fourth pixel sensor layer, Insertable B-Layer (IBL), was installed as the inner most layer in 2014. This was the first major upgrade project of the ATLAS detector [19].

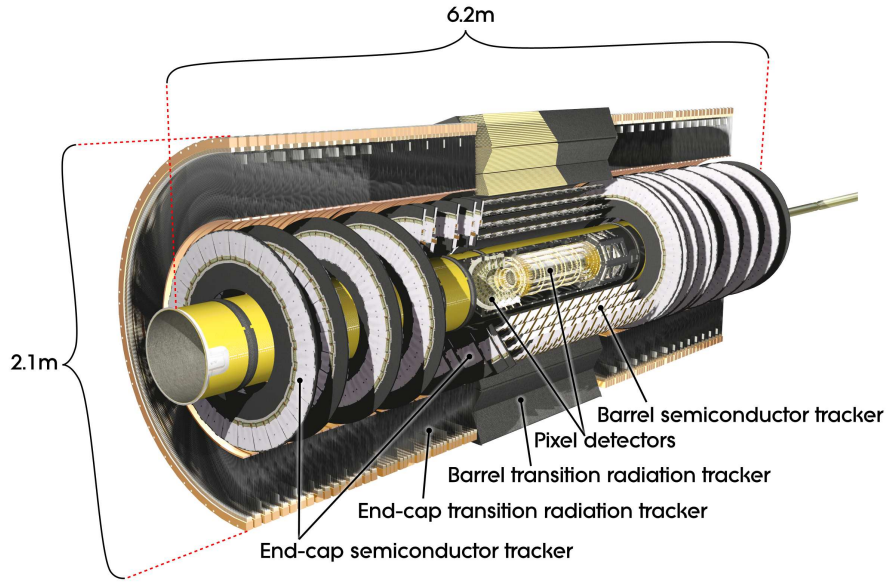


Figure 1.8: The Inner Detector [16].

Semiconductor Tracker

The SCT system is a silicon micorstrip detector designed to provide four precision measurements per track in the intermediate radial range, contributing to the measurement of momentum, impact parameter and vertex position, as well as providing good pattern recognition due to its high granularity. The SCT, like the pixel detector, consists of four barrel layers and two symmetric end-caps with 3 rings each.

Transition Radiation Tracker

The TRT is a gaseous tracking detector based on the use of proportional drift tube detectors (straws), which can operate at the very high rates needed by virtue of their small diameter (4 mm) and the isolation of the sense wires within individual gas envelopes. It provides particle identification capability through the generation of transition radiation photons when the particles change medium. The straw tubes were initially filled with an operating with the chosen Xe/CF₄/CO₂ working mixture. However, due to irreparable gas leaks which developed in the gas system part of the TRT detector is now flushed with a gas mixture composed primarily of argon necessitated by its lower cost [20].

Calorimeters

The ATLAS detector employs electromagnetic and hadronic calorimeters each of which using different techniques suited to the varying requirements of the physics processes of interest, their location, and the radiation environment in which they operate. They are all

System	Position	Area (m ²)	Resolution $\sigma(\mu m)$		Channels ($\times 10^6$)	Coverage ($ \eta $)
			$R\phi$	z		
Pixel	Insertable B-Layer		9	59.5	12	3.0
	B-Layer	0.2	12	66	16	2.5
	Barrel layers	1.4	12	77	81	1.7
	End-cap disks	0.7	12	77	43	1.7 - 2.5
SCT	Barrel layers	34.4	16	580	3.2	1.4
	End-cap wheels	26.7	16	580	3.0	1.4 - 2.5
TRT	Barrel straws		170 (per straw)		0.1	2.5
	End-cap straws		170 (per straw)		0.32	0.7 - 2.5

Table 1.2: Parameters of the Inner Detector including the Insertable B-layer. The resolutions quoted are typical values (the actual resolution in each detector depends on $|\eta|$.) [18, 19, 21].

sampling calorimeters, where only a fraction of particle shower is measured in the active regions, and the rest is absorbed in the passive regions.

Calorimeter energy measurement relies on the principle that the energy released within the detector material by charged particles, primarily through ionization and excitation, correlates with the incident particle's energy. To ascertain the energy of a detected particle, understanding the correlation between measured signals and deposited energy is essential, accomplished through detector calibration and calorimeter energy resolution. Energy resolution dictates the accuracy of measuring a particle's energy, determined experimentally by how accurately the energy of known-energy particles is replicated in calorimetric measurements.

The energy resolution of a calorimeter as a function of incident energy (E) can be parametrized as:

$$\frac{\sigma(E)}{E} = \frac{a}{\sqrt{E}} \oplus \frac{b}{E} \oplus c \quad (1.5)$$

In the context of energy resolution, the term a represents stochastic fluctuations related to the physical development of the shower, whether electromagnetic or hadronic. In sampling calorimeters, where active layers alternate with absorber layers, the energy deposited in the active medium varies from event to events, leading to sampling fluctuations. These fluctuations pose the primary limitation to the energy resolution of such detectors. The term b , denotes electronic noise, arising from the readout chain's electronic noise, which is contingent on the detector technique and the characteristics of the readout circuitry. Additionally, the term c , encompasses contributions unrelated to the particle's energy. Instrumental effects causing variations in the calorimeter response based on the particle's impact point on the detector result in response non-uniformities, contributing to additional energy smearing for particles distributed over large calorimeter areas, thereby yielding a constant term in the energy resolution. Addition in quadrature is represented by $\oplus$. An artist representation of the ATLAS calorimeters is shown in figure 1.9.

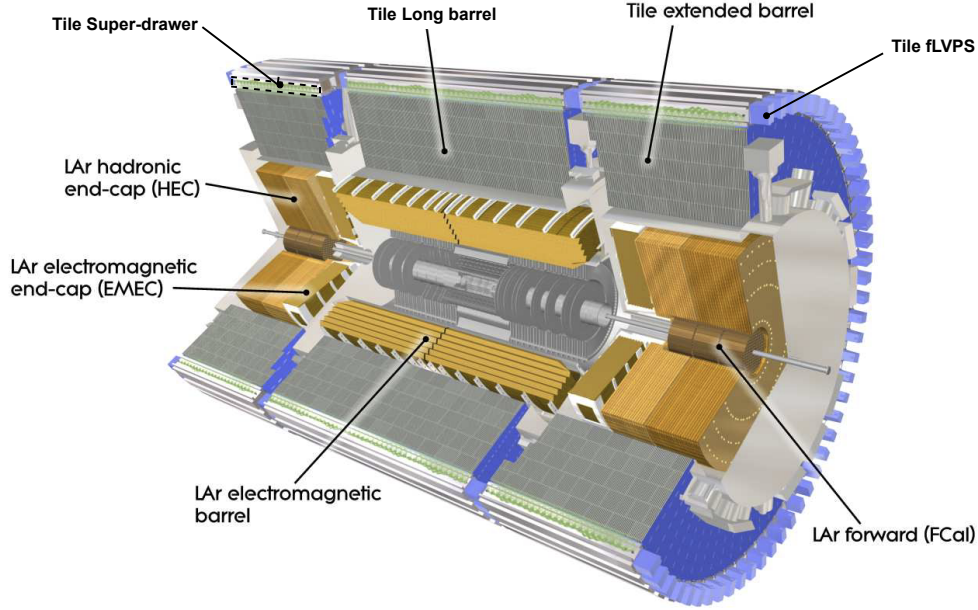


Figure 1.9: Layout of the ATLAS calorimeter systems.

Liquid Argon Calorimeters

The Liquid Argon (LAr) electromagnetic (EM) calorimeter is an accordion-shaped detector that uses Liquid Argon as the active detector medium due to its intrinsic linear behaviour, its stability of response over time and its intrinsic radiation-hardness, and lead as the passive medium. The EM calorimeter is divided into a barrel section covering the pseudorapidity range ($|\eta| < 1.475$) and two end-caps covering ($1.375 < |\eta| < 3.2$), each one housed in its own cryostat.

The LAr EM barrel calorimeter consists of two half-barrels that are bilaterally symmetric about $z = 0$. A gap of 4 mm is present between both half-barrels. A half-barrel is divided in 16 modules which when assembled provide full ϕ coverage without azimuthal cracks. The calorimeter is made of 1024 accordion-shaped absorbers, inter-spaced with copper read-out electrodes. The electrodes divide the space between the absorbers into two liquid argon gaps. This structure can be observed in Figure 1.10.

Each end-cap calorimeter contains an Electro-Magnetic End-cap Calorimeter (EMEC), a Hadronic End-cap Calorimeter (HEC), and a Forward Calorimeter (FCal). This structure is illustrated in Figure 1.11.

The EMEC uses the same accordion design concept as in the EM barrel. The EMEC absorber plates are separated by 8.5 mm gaps filled with liquid-argon and a structure of three electrodes that divide the gap into four drift spaces of 1.8 mm. . The total thickness of the EM calorimeter is above 22 radiation lengths for the barrel and above 24 for the end-caps.

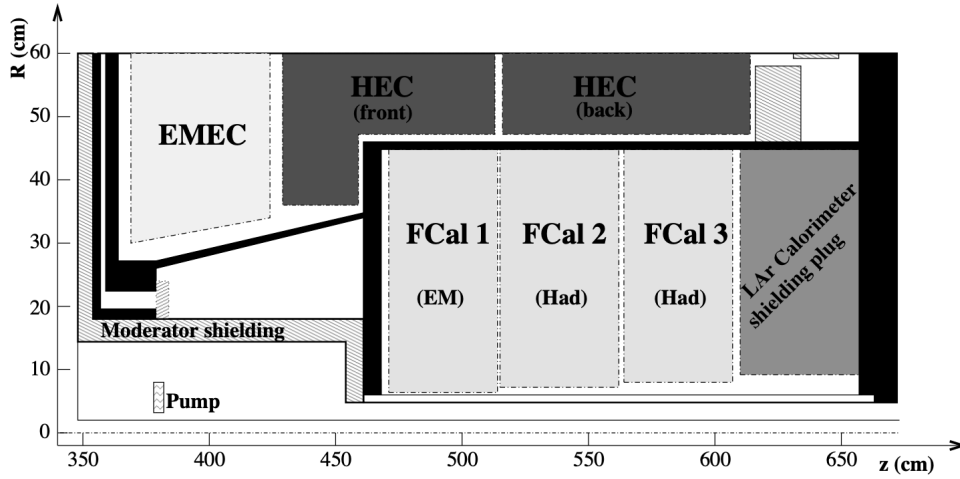


Figure 1.11: Diagram showing the inner structure of an end-cap calorimeter. The material in front of the FCal and the shielding plug behind it are also shown. The black regions are structural parts of the cryostat.

both edges providing perfect hermeticity. Staggering of the tiles in Z prevents cross-contamination of light between adjacent scintillation tiles. Fibers are grouped together to define three-dimensional cells which constitute the finest granularity of the detector. Each cell is readout by two Photo-Multiplier Tubes (PMTs). The TileCal and its Phase-II upgrade will be covered in greater detail in chapter 2.

Muon Spectrometer

The muon spectrometer uses the arrangement of toroidal magnets and gaseous detectors to identify charged particles and measure their momenta. The muon spectrometer forms the outer part of the ATLAS detector and is divided into three regions: the barrel region, transition region, and end-cap region. Four different detector technologies were employed throughout the system depending on the required spatial and timing resolution, resistance to radiation and engineering considerations: Monitored Drift Tube chambers (MDT), Cathode Strip Chambers (CSC), Resistive Plate Chambers (RPC) and Thin Gap Chambers (TGC). CSCs were replaced by a combination of Micro-Megas and TGCs during LS2 in the form of the New Small Wheel (NSW).

As can be seen in figure 1.13, the chambers in the barrel region are arranged in three concentric cylindrical layers around the beam axis at radii of approximately 5 m, 7.5 m, and 10 m. In the two end-cap regions, muon chambers form large wheels, perpendicular to the z -axis and located at distances of 7.4 m, 10.8 m, 14 m, and 21.5 m on either side of the interaction point.

Monitored Drift Tube Chambers

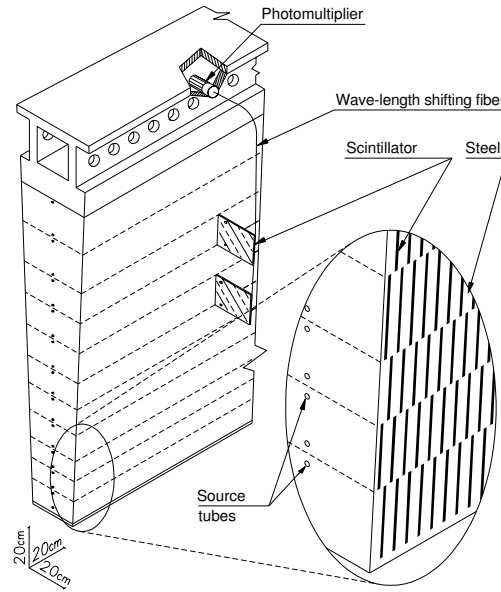


Figure 1.12: Diagram of a TileCal module illustrating its components and structure [23].

The Monitored Drift Tube chambers (MDT's) perform the precision momentum measurements. These measurements combine high measurement accuracy, predictability of mechanical deformations and simplicity of construction. These chambers consist of three to eight layers of pressurised drift tube with a diameter of 30 mm, operating with Ar-CO₂ gas at 3 bar. The electrons resulting from ionisation are collected at the centrally located W-Re wire. The operating gas was selected due to exhibiting good ageing properties such as deposits on the wires having never been observed although a non-linear space-drift time relation and a long drift time result in poor spacial resolution performance at high rates.

Thin Gap Chambers

The Thin Gap Chambers (TGCs) form the the Big-wheels as well as a portion of the Small-wheels. TGCs are multi-wire proportional chambers with the characteristic that the wire-to-cathode distance of 1.4 mm is smaller than the wire-to-wire distance of 1.8 mm. A gas mixture of CO₂ and highly flammable n-C₅H₁₂ (n-pentane) is used. Due to its flammability the gas mixture needs to be flushed prior to access being granted to the detector cavern.

Cathode Strip Chambers

In the forward region, Cathode-Strip Chambers (CSC) were used in the inner tracking layer, instead of MDTs, due to their higher rate capability and time resolution. The CSCs, located at the inner radii, in combination with TGCs on the outer radii formed the Small-wheel. This increased rate capability has been shown to be insufficient, in end-cap region and in particular in the small wheel, for high-luminosity operations. The expected

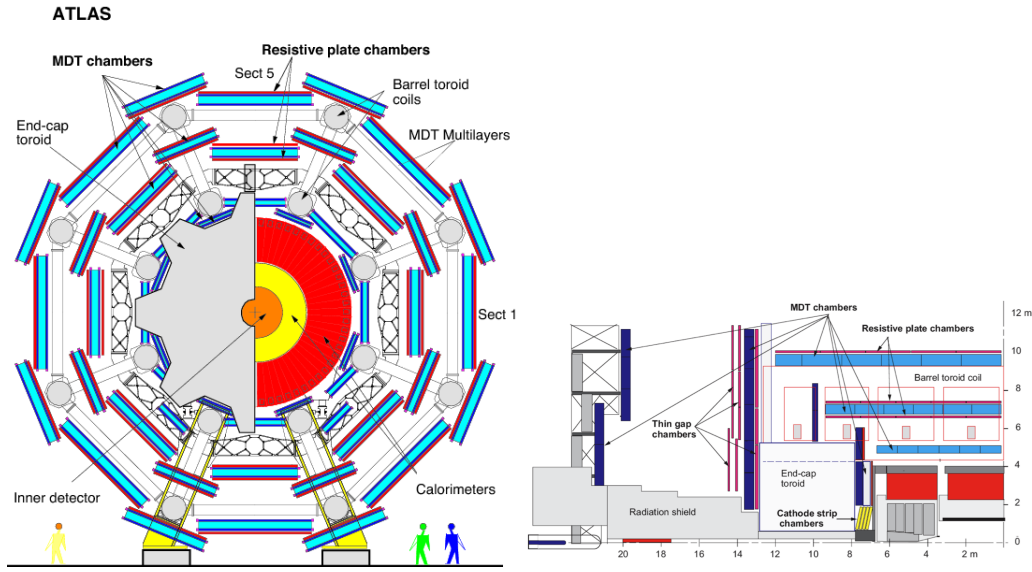


Figure 1.13: (Left) A schematic view of the Muon spectrometer in the xy (left) and (Right) in the rz .

hits rate exceeds the existing detector capability and compromises muon tracking performance motivating the now completed Phase-I upgrade of the Small-wheel which will be covered explicitly in subsection 1.4.3.

Resistive Plate Chambers

The Resistive Plate Chambers (RPC) are gaseous detectors consisting of parallel electrode plates. These detectors utilize two resistive plates, composed of phenolic-melaminic plastic laminate (Bakelite), which are maintained parallel to each other with a separation distance of 2 mm using insulating spacers. The gas volumes within the chambers are filled with a mixture of $C_2H_2F_4$, $Isobutane - C_4H_{10}$, and SF_6 . This combination offers advantages such as low operating voltage, non-flammability, and affordability, while also providing a plateau for safe avalanche operation. An electric field established between the plates enables the formation of avalanches along ionizing tracks towards the anode.

Trigger and Data Acquisition System

The ATLAS Trigger and Data Acquisition System (TDAQ) is composed of two highly integrated systems, namely the Trigger and Data Acquisition (DAQ) systems [24]. The Trigger system selects events at two different stages of the DAQ: Level-1 (L1), and High Level Trigger. Each Trigger level refines the decisions made by the previous level allowing the ATLAS Trigger to select interesting events from the very large background produced by the LHC. Events generated at 40 MHz are stored in the various sub-systems Front-End (FE) pipeline memories. The DAQ system receives and buffers the event data received by the detector readout electronics at L1 trigger accept rate of approximately 75 KHz (upgradeable to 100 KHz).

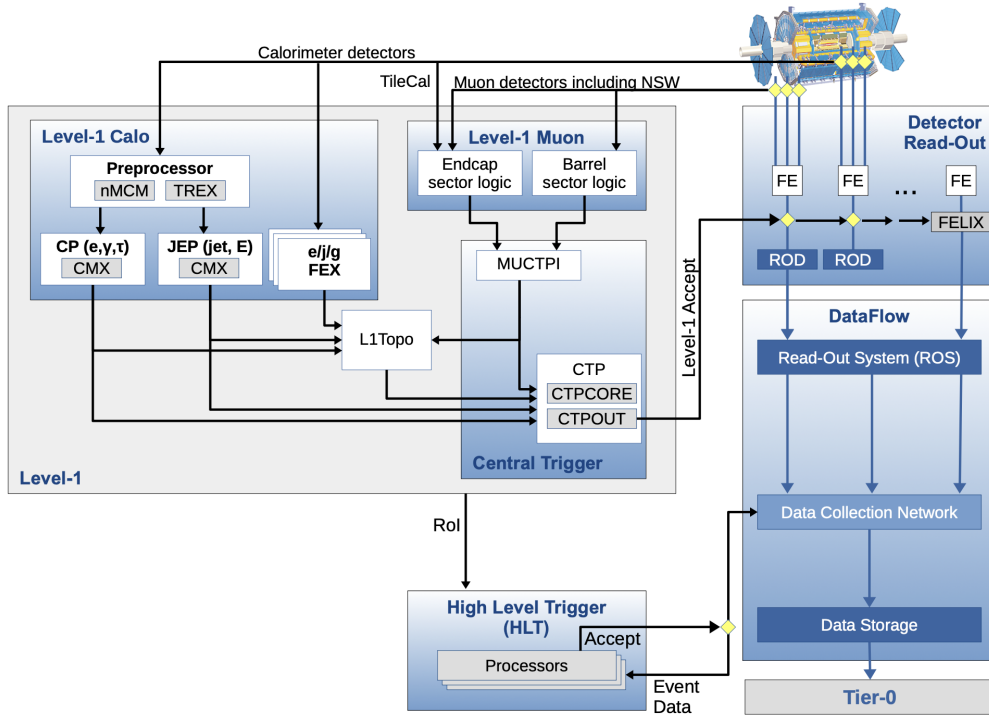


Figure 1.14: A functional diagram of the ATLAS Trigger and Data Acquisition system in Run 3.

The L1 Trigger implemented using custom-made electronics consists of the L1 Calorimeter (L1Calo) and the L1 muon triggers. The L1Calo Trigger searches for signatures of high- E_T objects such as electrons and photons, jets, and τ -leptons decaying into hadrons, as well as events with large E_T^{miss} and large total transverse energy. The L1 muon Trigger is based on signals in the muon trigger chambers as well as signals from the Hadronic Tile Calorimeter (TileCal) which are indicative of co-incidence of muons. The L1 Muon searches for patterns of hits consistent with high- P_T muons originating from the interaction point. Regions with potential interesting objects or Regions of Interest (ROI), are created using information from L1Calo and L1Muon within the Central Trigger Processor (CTP).

Since Run 2, the High Level Trigger bases its decision on a subset of data from the event defined by the RoI's such as coordinates, energy, and type of signature to further reduce the amount of data that must be transferred from the detector readout to below 3.5 KHz. The Event filter uses offline analysis procedures on fully-built events to further select events down to a rate, of approximately 200 Hz, which can then be recorded for subsequent offline analysis.

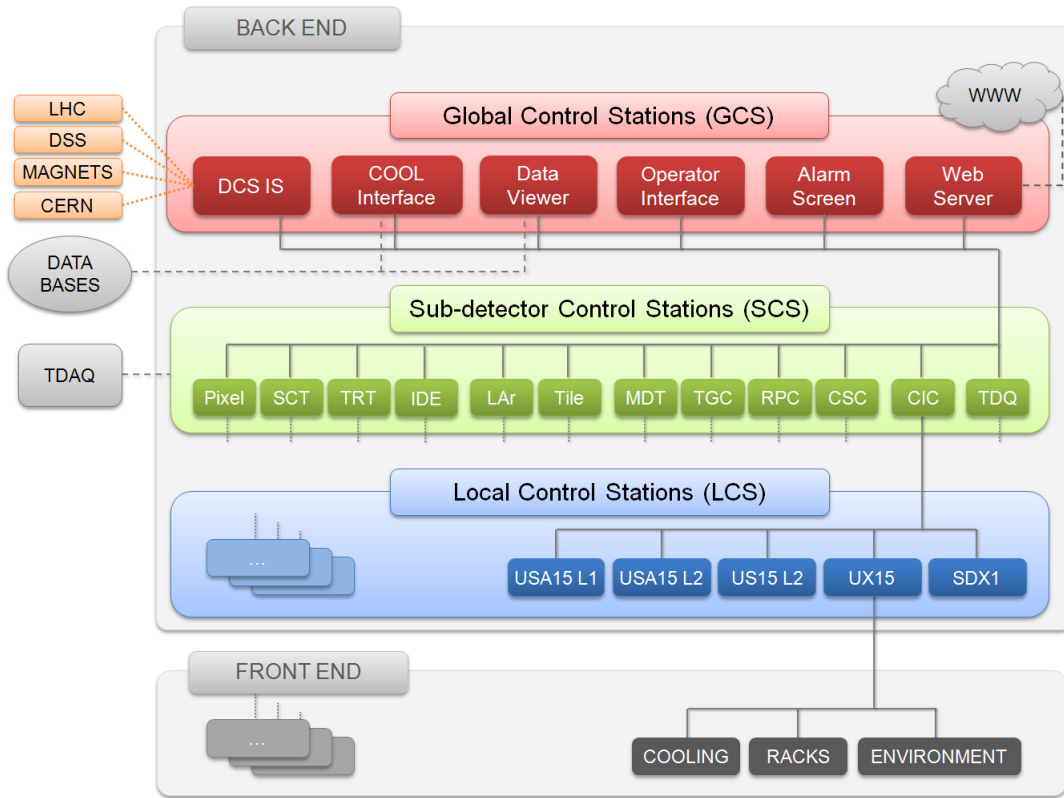


Figure 1.15: A functional diagram of the ATLAS Detector Control System architecture.

Detector Control System

Complementary to TDAQ, the Detector Control System (DCS) enables the coherent and safe operation of the ATLAS detector. It supervises the different detector hardware elements such that they transition into the the selected operational conditions, continuously monitors and archives its run-time parameters, and automatically performs corrective actions if necessary. Furthermore, the DCS provides a human interface for the full control of ATLAS and its sub-detectors both the ATLAS Control Room and remotely.

As seen in Figure 1.15, the DCS employs a hierarchically organised tree-like architecture that mirrors that of the ATLAS experiment with each element having a certain level of operational independence. The Front-End (FE) consists of purpose built hardware to control the detector as well as supporting services. The standardization of the DCS hardware, both commercial and custom made, and the software interfaces is of primary importance for the homogeneous control of all different detector components. Due to the environmental conditions within the experimental cavern (UX15) a custom general-purpose Input/Output concentrator known as the Embedded Local Monitoring Board (ELMB) was developed [25]. The ELMB is designed and certified to be radiation tolerant and can therefore be placed inside the detector in locations shielded by the calorimeters.

The ELMB serves two primary functions: it can either be directly integrated into

the detector electronics or connected to a general purpose motherboard, allowing for the attachment of various sensors.

The back-end comprises three layers: Local Control Stations for overseeing subsystem processes, Sub-detector Control Stations (SCS) for managing individual sub-detectors independently, and Global Control Stations (GCS) with human interfaces in the ATLAS control room for overseeing overall operations.

1.4.2 Detector Reliability Considerations

The reliability of a particle detector is a fundamental consideration during the design process. There are two overarching reasons for this. The first reason is that the failure of even a small portion of a sub-detector can lead to reduced performance and intolerable defects in the collected data rendering the data of little use for analysis. Secondly, when considering larger sub-systems, such as cooling systems, the impact of failures can render the detector unable to take data whatsoever. These failures can have broad reaching consequences as a failure that presents within the ATLAS detector could trigger a beam-dump of the LHC thereby impacting data taking at CMS and vice versa. Due to the scale and complexity of modern particle detectors reliability needs to be intrinsic to their design. Numerous design and operational strategies are employed within detectors such as ATLAS which range in scale from individual electronic components up to an entire systems architecture. In the subsequent paragraphs various approaches used to improve detector reliability are considered with specific implementation within the ATLAS detector being reference to.

Radiation Damage Mitigation

Radiation damage is an unavoidable environmental consequence of operating a particle detector. In some cases shielding can be employed to reduce the exposure of a system but in many others this is not possible. To address this radiation damage mitigation is a concept in which the affect of radiation damage is accounted for in the design of a system. Due to the Inner-detectors close proximity to the IP both its design and operation take into account the affect of radiation damage on sensors, on-detector electronics, mechanical structure and services. Ensuring sufficient signal performance throughout the lifetime of the detector is imperative for both the Pixel and SCT sensors. The cumulative radiation dose significantly impacts the sensors, affecting their operational voltage, which is influenced by the effective doping concentration and subsequent temperature-sensitive annealing. Additionally, the cumulative dose correlates directly with the increase in sensor leakage current. The n-type bulk material effectively becomes p-type over time. The effective doping concentration then grows with time in a temperature-dependent way. To contain this annealing and to reduce the leakage current the sensors are operated in the temperature range -5°C to -10°C requiring coolant temperatures

of approximately -25°C . The above mentioned operating temperatures are maintained throughout the year with exceptions being unplanned interventions (which can occur at any time) and planned interventions that occur during the year-end technical stop. During this period maintenance of both ID cooling systems is performed with both Pixel and IBL reaching room-temperature for a period of a few weeks.

Active Component Radiation Tolerance Assurance

The detectors at the LHC encounter substantial fluxes of extremely energetic particles stemming from proton-proton and heavy-ion collisions, resulting in detrimental effects on detector performance. Consequently, it is crucial to implement radiation-tolerant designs for the detectors thereby ensuring consistent and reliable performance throughout their operational lifespan. Aerospace grade electronic components are typically considered for use within such an environment. However, Commercial Off-The-Shelf (COTS) active electronic components provide a preferable alternative for use in large scale experiments due to their lower cost per unit with the caveat that the components need to exhibit radiation tolerance to allow for their use within the HL-LHC detector environment. The process of component certification is overseen by the ATLAS Radiation Effects Task-Force (RETF) and the required testing for which is undertaken by the respective sub-detectors that wish to utilize the component. Traditionally the radiation environment, for the purpose of electronic radiation damage estimates, has been characterised by three quantities: the Total Ionising Dose (TID), the 1 MeV neutron equivalent fluence (number of particles per unit area), specified for silicon as Φ_{neq}^{Si} and the hadron fluence above 20 MeV (Φ_{20}^{had}).

Targeted Design Redundancy

Single point failures are inherently undesirable within any system. This is further heightened when considering a complex experiment such as ATLAS. Numerous considerations are made when looking to implement design redundancy on- and off-detector such as the impact on detector performance and the associated cost of its implementation. The Hadronic Tile-Calorimeter employs redundancy in its readout whereby each calorimeter cell is read out by two individual Photo-Multiplier Tubes (PMT's). The use of two PMT's also guarantees a sufficient light yield from the respective cell as well as allowing for their cross-calibration. Redundancy was selected as the mode in which to improve reliability of the detector readout as repairs to the Wavelength Shifting optical Fibers is impossible due to lack of access. The PMTs are located within the structural girder on the outer radii of the detector therefore having no impact on detector performance.

Leakless Systems

The thermal behaviour is an important consideration in some large detectors such as the TileCal. The large iron mass (heat capacity) of the detector contributes to the temperature stability of the electronics inside its modules, but a dedicated cooling system must evacuate heat dissipated by the front-end electronics lest it accumulate over time. It is imperative to maintain stable local temperatures to within 1°C . This as a temperature variation of 1°C would induce a PMT gain variation of 0.2% [26]. The TileCal employs a so called leakless cooling system in which the coolant's working pressure is below atmospheric pressure and is discussed in detail in section 2.11.

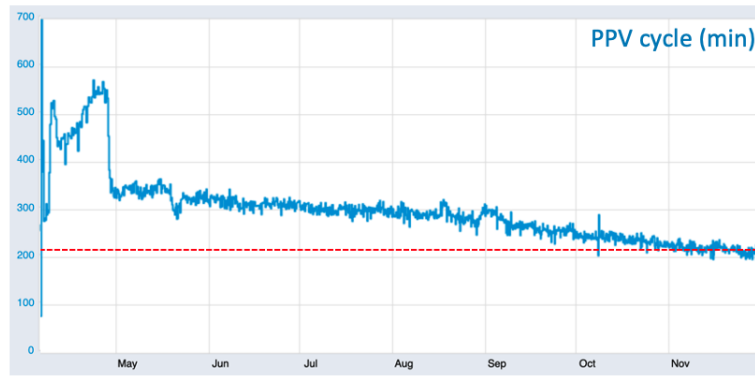


Figure 1.16: The TileCal cooling plant pump cycle duration from April 2022 to December 2022.



Figure 1.17: The TileCal cooling plant pump cycle duration from 25th January 2023 to 12th February 2023.

In the case of failure of a cooling pipe, or connector, air will be sucked into the cooling system and return to a storage tank off detector. This prevents coolant leakage within TileCal and allows for the detector to continue operations even if a leak is detected [27]. The severity of the leak dictates the actions taken with "minor" leaks deemed acceptable provided that the temperature of the detector is within operational limits. These leaks

are address in the subsequent year-end technical stop. The TileCal experienced such leaks which became progressively worse during the period from May to December 2022. The linear downward trend of the PPV cycle can be observed in Figure 1.16. A PPV cycle is defined as the duration of time between sequential cooling system vacuum pump operations. A decrease in PPV cycle time indicates that the pumps need to be operated more frequently to maintain the required pressure within the system. A series of interventions were undertaken during the 2022 Year-End Technical Stop (YETS) period with testing occurring from January 2023 up until commissioning of the system on the 9th of February. Although the intervention did not increase the PPV cycle to 700 minutes, as was the previous baseline, the stable value of approximately 450 minutes, pictured in Figure 1.17 was deemed to be acceptable.

System Segmentation

The muon system, much like others within ATLAS, boasts a high degree of segmentation, enhancing reliability by localizing any faults to specific areas. Similarly, the electrical services of the muon system are divided into segments. However, due to budget constraints, maintaining maximum power supply modularity throughout the system wasn't feasible. Consequently, every two MDT chambers are powered from a single low-voltage supply channel. The segmentation of MDT high-voltage supplies is finer, with each multi-layer of three (four) tube layers receiving power from an individual channel. Both TGCs and RPCs have separate low-voltage supplies for analogue and digital readout electronics. To serve the 3588 chambers of the TGC system, a total of 3732 high-voltage channels are utilized. The service architecture is designed to mirror this modularity, minimizing data loss in the event of a supply channel failure. Constructing MDT chambers from individual tubes offers numerous advantages. The rigidity of the tube assembly ensures both high mechanical precision and chamber robustness. This design also contributes to a high level of MDT chamber reliability, as a failure in one tube cannot propagate to others within the chamber.

1.4.3 Phase-I Upgrade of the ATLAS Experiment

The Phase-I upgrade of the ATLAS Experiment took place during the LS2 from December 2018 to April 2022. The focus of this upgrades were the Muon spectrometer, the LAr, and the Level-1 trigger. As discussed in 1.3.3 the accelerator underwent a series of upgrades with the resulting increase in instantaneous luminosity, and ATLAS took the opportunity to exploit the physics potential that it offered.

Phase-I upgrade of the Muon spectrometer

The trigger rates, detector occupancy, and momentum resolution in the Muon spectrometer are significantly influenced by the level of background radiation present in the cavern.

The Phase-I upgrade of the Muon spectrometer primarily targets the Muon inner station of the Muon end-cap, incorporating the installation of the New Small Wheel (NSW) A and C, as well as new Barrel Inner Short chambers in sectors 7 and 8 of the Muon detector (BIS7/8). Positioned in the inner region of ATLAS, as depicted in Figure 1.13, the NSW is situated in an area characterized by the highest flux of cavern background radiation within the muon spectrometer.

Phase-I upgrade of the LAr Calorimeter

The Level-1 trigger system necessitates increased transverse granularity and depth details to decrease rates and enhance resolution for various trigger objects. This necessitated a partial upgrade of the front-end read-out architecture of the Liquid Argon calorimeter (LAr), which forms a component of the input stage of the Level-1 calorimeter trigger, along with modifications to the interfaces between the two systems.

Phase-I upgrade of the Trigger

Utilizing data from the New Small Wheel (NSW) and upgraded Liquid Argon calorimeter (LAr), enhancements to the Level-1 trigger electronics aim to bolster performance under higher pile-up conditions and offer greater trigger flexibility. While no significant architectural alterations to the current detector read-out and data acquisition are planned, the Phase-I trigger operation must adhere to the existing latency limits of the Phase-0 system. Consequently, FELIX has been introduced as the detector read-out for NSW and LAr, facilitating the accumulation of valuable experience before its full integration into the detector by Phase-II. Moreover, this implementation streamlines the read-out electronics of the sub-detectors.

1.4.4 Phase-II Upgrade of the ATLAS Experiment

The overarching goal of the Phase-II upgrade of the ATLAS experiment is to maintain the excellent performance of the sub-detectors in terms of efficiency, resolution, and background rejection for all physics objects within the HL-LHC environment for the duration of its operation.

Challenges Imposed by the HL-LHC

The HL-LHC will impose numerous challenges on the ATLAS detector that in its current state (post Phase-I upgrade) it is unable to overcome. The detector has been operational since 2008 in which the first p-p events were recorded. The lifetimes of various sub-detectors will be nearing after the intermediate Phase-I upgrade thereby necessitating their replacement regardless of future performance requirements. This as the performance of said components will exhibit significant degradation at their end-of-life. An

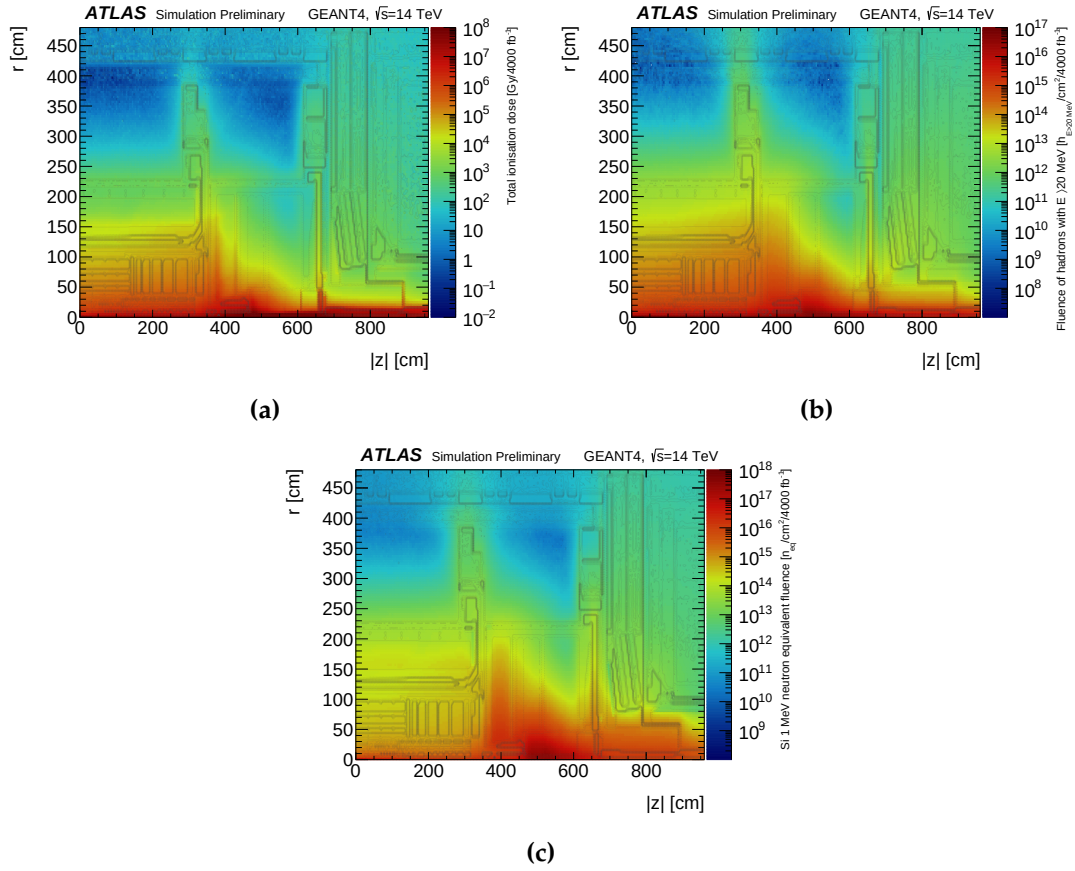


Figure 1.18: Radiation maps of the Total Ionisation Dose (TID) (a), Fluence of hadrons with $E > 20 \text{ MeV}$ (b) and 1 MeV neutron equivalent fluence (c) from GEANT4 [28] simulations of the ATLAS detector in a configuration for the Phase-II upgrade of the HL-LHC.

example of approaching lifetimes is within the Inner-detector where the silicon tracking systems will be approaching the end of their lifetimes $\mathcal{L} = 700 \text{ fb}^{-1}$ and $\mathcal{L} = 400 \text{ fb}^{-1}$ for the strip and pixel systems, respectively.

This challenge is further compounded when considering that the legacy on-detector electronic components are not qualified for operation within the HL-LHC environment with regards to both the instantaneous luminosity and the large integrated luminosity of 4000 fb^{-1} associated with the planned duration of the detector operation. The radiation levels are predicted by combining scaled measurements and simulations in order to define the qualification requirements for electronic systems. A radiation map for Total Ionisation Dose (TID) (a), Fluence of hadrons with $E > 20 \text{ MeV}$ (b) and 1 MeV neutron equivalent fluence (c) from GEANT4 [28] simulations of the ATLAS detector in a configuration for the Phase-II upgrade of the HL-LHC are presented in Figure 1.18. The simulations are based on 50k inelastic proton-proton events generated with PYTHIA 8 [29] using an ATLAS specific tune [30]. The TID and hadron fluence distributions are consistent with expectations. Higher magnitudes are observed close to the beam axis and forward regions due to the dominance of minimum-bias interactions and in the gap

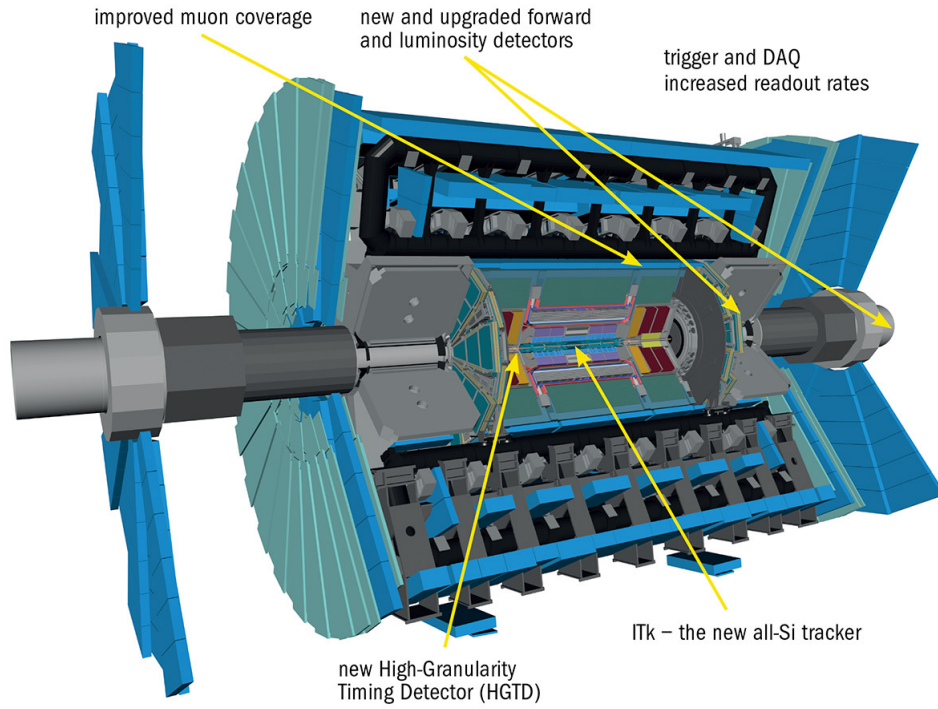


Figure 1.19: Schematic of the ATLAS detector for the HL-LHC era.

located between the barrel and end-caps. These simulations are utilized by the ATLAS experiment to determine radiation tolerance criterion for the Phase-II upgrade as will be done in section 3.1.1.

Trigger and Data Acquisition Upgrades for Phase-II

The upgrade of the Trigger and Data Acquisition (TDAQ) system is a core element of the preparation of the ATLAS detector for high luminosities. The trigger requirements for the high luminosity, both on the rate and on the latencies, imply a revision of the read-out electronics architecture towards a free-running scheme where all data are sent off-detector. The Phase-II Trigger system will contain a L0-only hardware trigger at 1 MHz [24]. It will continue to sample data from the detector at bunch crossing rate, and will be equipped with new feature extractors for the Calorimeter and Muon systems that will be combined at a Global Trigger with improved acceptance and momentum resolution, in order to reduce the consequences of pile-up.

The read-out of the experiment will replace the custom ROD electronics by a common FELIX infrastructure that will interface the front-end links of the sub-detector electronics with a commercial networking infrastructure.

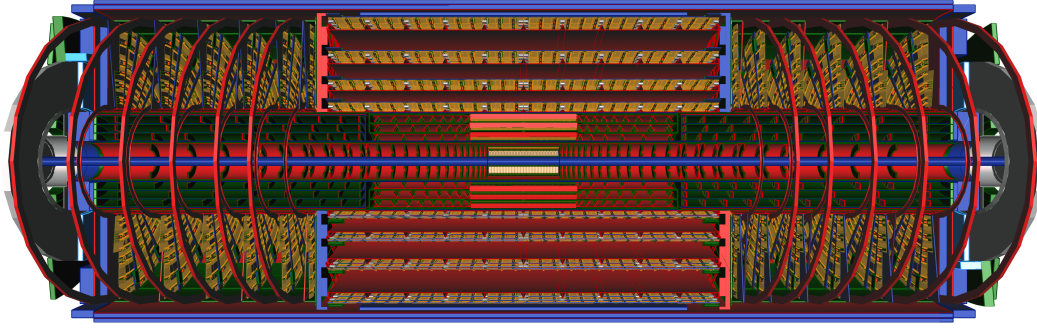


Figure 1.20: The Inner Tracker.

Inner Tracker

The Inner Tracker (ITk), illustrated in Figure 1.20, is an all silicon tracker that will replace the current ATLAS Inner Detector (ID). It will provide extended tracking coverage up to $|\eta| < 4$, and support the full 1 MHz L0-only Trigger rate. The ITk is made of two distinct subsystems, namely the Pixel Detector [31] that is surrounded by a Strip Detector [32]. The Pixel Detector consists of five flat barrel layers and multiple inclined or vertical ring-shaped end-cap disks. The Strip Detector has four strip double-module layers in the barrel region and six end-cap disks. The ITK will be installed within ATLAS as a single monolithic unit. The material distribution within its volume has been reduced by more than a factor of in the forward region versus the current ID [33].

High-Granularity Timing Detector

The High-Granularity Timing Detector (HGTD) is designed improved time resolution in order to effectively suppress the effects of pileup in the forward region. Data transmission at a rate of 40 MHz will allow unbiased, bunch-by-bunch measurements of the luminosity as well as the implementation of a minimum-bias trigger. The HGTD, as illustrated in Figure 1.21, will be located in the gap region between the barrel and the end-cap calorimeters, at a distance in z of approximately ± 3.5 m from the nominal interaction point in the volume currently occupied by the Minimum-Bias Trigger Scintillators, which will be removed [34]. Each HGTD end-cap is the integration of one hermetic vessel, two instrumented double-sided layers (mounted on two cooling/support disks), and two moderator pieces placed inside and outside the hermetic vessel. The sensors will be operated at low temperatures (-30°C) to mitigate the impact of irradiation.

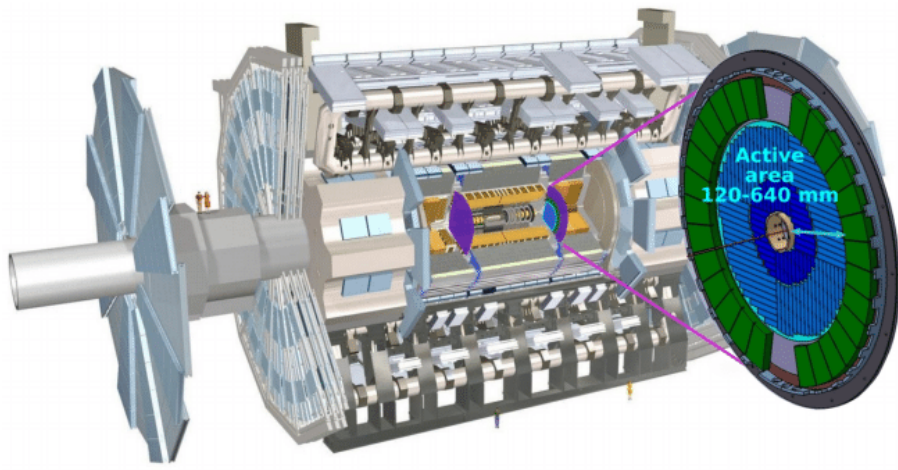


Figure 1.21: Schematic illustrating the High Granularity Timing Detector and its location within ATLAS.

Liquid-Argon Calorimeter

The Phase-II upgrade of the Liquid-Argon (LAr) calorimeter focuses on the readout electronics, power distribution system and Detector Control System (DCS). Upgrade of the readout electronics is necessary due to both current radiation damage and future radiation hardness requirements as well as to accommodate the upgrade Trigger system. The LAr front-end electronics will be further upgraded with the replacement of the primary read-out and calibration boards take place during LS3. The main architectural difference between the existing readout system and that of the upgrade system is the switch from an analog on-detector Level-1 pipeline to a “free-running” design in which signals from all calorimeter cells are “continuously” digitized at 40 MHz (the bunch-crossing rate) and subsequently sent off-detector. This approach removes all constraints imposed by the LAr readout on the trigger system, since full granularity data will be available and the latency and Level-1 bandwidth become essentially unlimited [35]. Replacement of the Front-End (FE) electronics implies simultaneous replacement of the back-end electronics as well. For the Phase-II upgrade, the new FE electronics will mostly use voltages lower than the present ones necessitating replacement. The overall architecture of the current DCS system will remain the same for Phase-II, despite the necessary changes in the FE

including the incorporation of the Embedded Local Monitoring Board (ELMB) 2 which is a replacement for the obsolete ELMB and tolerates higher levels of radiation than its predecessor.

Tile Calorimeter

A complete overhaul of the readout electronics of the hadronic Tile Calorimeter (TileCal) will take place for the Phase-II upgrade to be compatible with the new ATLAS L0/L1 trigger architecture, to meet the increased radiation tolerance requirements of the front-end readout electronics, which are located on-detector, and to provide higher granularity information to the trigger processors [36]. The upgrade to the front-end electronics will be accompanied by an upgrade to the Detector Control System (DCS), High-voltage and Low-voltage systems. The Photo-multiplier tubes in the most exposed regions of the calorimeter will also be replaced due to ageing accounting for approximately 10% of their total population [37]. Further details will be provided in chapter 2.

Muon Spectrometer

The Phase-II upgrade of the muon spectrometer involves installing new chambers, replacing some existing chambers with new ones, and upgrading a significant portion of the front-end, trigger, and readout electronics. The chamber upgrades address weaknesses of the present chambers and their layout. To maintain a high trigger efficiency, new RPC chambers with increased rate capability will be installed on the inner (BI) MDT chambers of the barrel. The MDT chambers will be replaced by new sMDT chambers with reduced overall thickness so that the sMDT chambers and the new RPCs fit in the same envelope as the original MDT chambers.

A significant enhancement in performance is essential for elements within the muon spectrometer system, encompassing both the muon precision tracking and triggering systems [38]. The current readout system for the trigger chambers in the barrel (RPC) and end-cap (TGC) will be inadequate to accommodate the new L0/L1 trigger scheme. This is because the existing electronics are tailored for maximum latencies of $3.2\ \mu\text{s}$ (TGC) and $6.4\ \mu\text{s}$ (RPC), and for trigger rates of up to 100 kHz. The electronics upgrades will ensure that the low trigger thresholds can be maintained and trigger rates remain manageable in the high-rate necessitating replacement. The electronics chain of the MDT precision chambers will also be completely redesigned.

Chapter 2

The Phase-II Hadronic Tile Calorimeter

In the previous Chapter we briefly introduced the Large Hadron Collider (LHC), its Injectors upgrade, as well as its High Luminosity Upgrade thereby providing much needed context for the ATLAS experiments Phase-II Upgrade which is itself a direct consequence of the aforementioned upgrades to the LHC. The Phase-II Upgrade of ATLAS was subsequently covered in detail including all sub-detectors and their associated upgrades with the new Trigger and Data Acquisition system of the experiment also being covered. In keeping with the theme of this thesis a subsection was also devoted to detector reliability considerations within the context of the ATLAS experiment as a prelude to the topic which we will continue to develop throughout the Chapters that follow.

In this Chapter we will introduce the Hadronic Tile Calorimeters (TileCal) Phase-II upgrade starting with its global structure and mechanics after which we will proceed to the detectors trigger and readout electronics with particular emphasis being placed on the on- and off-detector readout electronics. The topics of signal reconstruction, energy reconstruction and the detectors calibration systems are covered for completeness. The detectors High- and Low- voltage power distribution systems are then presented in brief with the Chapter concluding on the topic of the on-detector services and cooling.

The aim of this Chapter is to present the Phase-II Upgrade TileCal in its entirety so as to provide a global perspective of its function and operation. This is prudent as when considering any topic within the context of particle detectors it is vital to understand the intricate relationship between all detector sub-systems and their impact on detector performance. This fact becomes readily apparent when considering the Low-Voltage (LV) power distribution system that provides LV power to all on-detector electronics. This is noticeably brief as it will be covered thoroughly in chapter 3.

2.1 Detector Structure

A gap of 6.9 cm is present between the Long and Extended barrels once the detector is in the closed position. This gap which can be seen in Figure 2.1 is required due to the presence of Inner Detector and Liquid Argon Calorimeter services and readout cables. This

volume is a concern for loss of energy therefor an stepped Intermediate Tile Calorimeter (ITC) is included in the design. The ITC is composed of three distinct calorimeter structures. These are the Plug, Gap and Crack scintillators. The plug is a reduced section of a standard module comprised of Cells D4 and C10, that fits within the free space around the services [39]. To further maximize the amount of active material the Gap (E1 and E2) and Crack (E3 and E4) cells extend downwards with the Crack cells occupying the space between the barrel and end-cap cryostats. These special cells are only composed of scintillator and are exceptionally read out by only a single PMT.

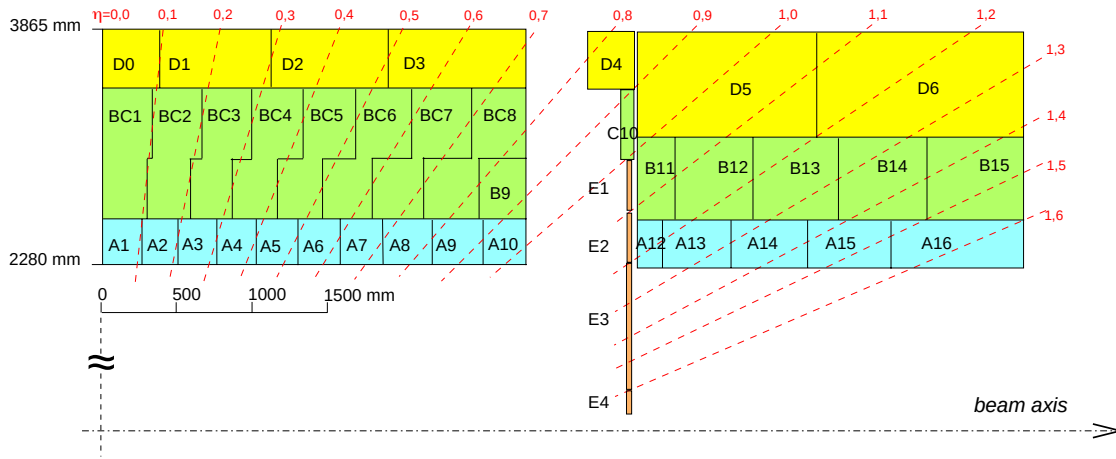


Figure 2.1: (Left) Schematic of the TileCal cell distribution for half of a long-barrel module . (Right) An extended-barrel module with lines that illustrate the projective pseudorapidity [23].

2.2 Mechanics

Within the TileCal the Photo-Multiplier Tubes (PMTs), electrical, optical and cooling services, and front-end electronics are housed within removable aluminium Super-drawers (SD). The SDs are inserted into the girder of each module located on the outer radius with EB modules requiring a single drawer and LB modules requiring two SDs due to their length. Therefore, a total of 256 SDs are required for the entire calorimeter.

Each Phase-II SD is modular and consists of 4 connected independent units, called Mini-Drawers (MDs). The contents of a MD will be covered in section 2.4. A simplified MD cross-section is illustrated in Figure 2.4. The increased modularity of the Phase-II drawers (legacy SDs were partitioned into only two sub-drawers) allows simplified handling during installation as well as during on-detector maintenance due to the limited space available within the inner-barrel.

A Long-barrel module utilises 45 PMTs to readout its cells requiring the use of all four MDs as can be seen in Figure 2.3 (left). The Extended-barrel modules require only 32 PMTs due to the EB cell architecture. If four standard MDs were used the mini-drawers

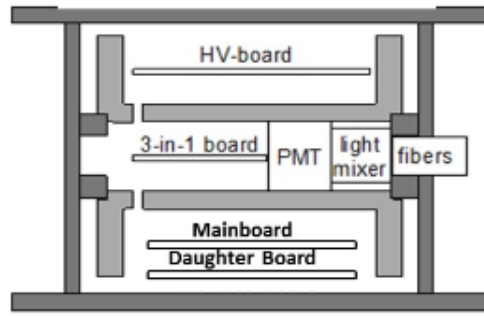


Figure 2.2: Mini-drawer cross-section.

MD3 and MD4 would house only four and six PMTs, respectively. All 32 PMTs in the extended barrel can be read out using only three sets of electronic boards. This has allowed the use of special mini-MDs which function to connect the adjacent MDs services and house two PMTs each. The use of these drawers illustrated in Figure 2.3 (right) provides resource saving as a set of MD readout electronics need not be installed as their PMTs are read out by the adjacent MDs.

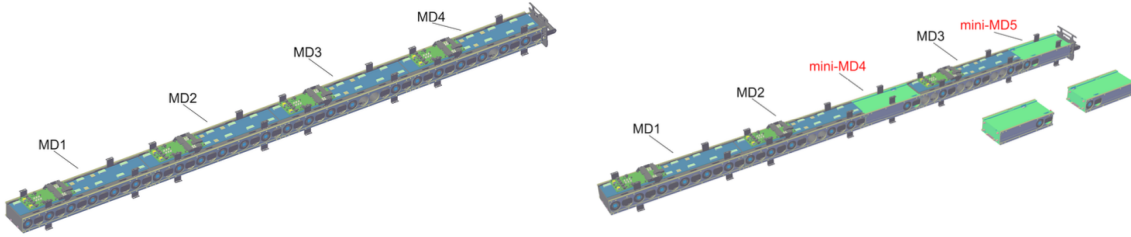


Figure 2.3: TileCal Phase-II Super-drawer architecture for the Long-barrel (left) and Extended-barrel (right).

2.3 Trigger and Readout Electronics

The main difference with respect to the legacy detector is that the Phase-II detector will transfer digitized data from the on-detector electronics to the off-detector electronics for every bunch crossing (40 MHz) with the pipeline memories being located entirely off-detector, simplifying the design and allowing for future upgrades of the pipeline memories and reconstruction techniques, while reducing the impact of radiation damage on the detector. This requires a huge increase in the data bandwidth between the on-detector and the off-detector electronics using CERN wide standard technologies and COTS components as much as possible. Similarly to the mini-drawer design the electronics are also split in two fully redundant halves in order to minimize the single point failures that

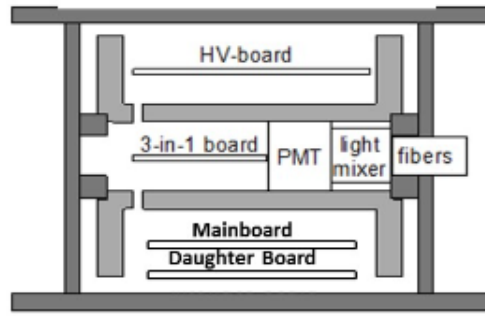


Figure 2.4: Mini-drawer cross-section.

might render un-usable a full super-drawer. Figure 2.5 shows a flow diagram of the on- and off-detector electronics involved in the detector read-out.

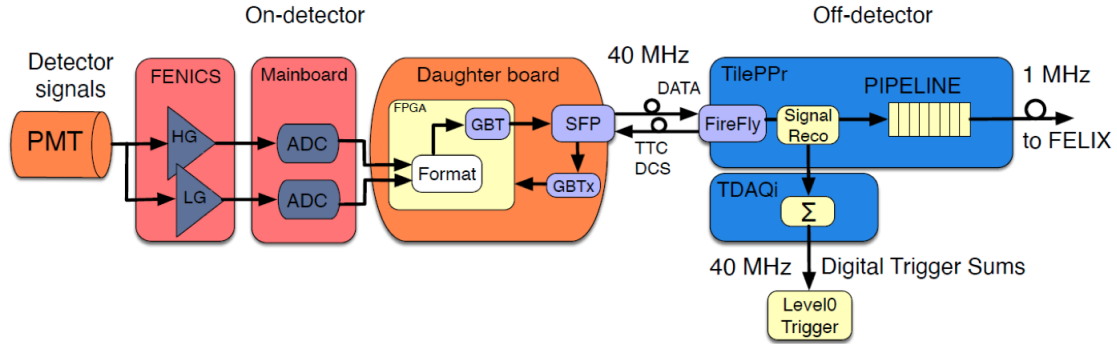


Figure 2.5: Diagram of the TileCal trigger and readout electronics at the HL-LHC [40].

The impact on the trigger is that it is no longer necessary to propagate the L0-accept signal to the on-detector electronics, as they will be processed by the off-detector pipeline memories. However, the other Trigger, Timing, and Control (TTC) commands are necessary in order to synchronize the read-out counters and configure the components for operation. Details will be provided in the following paragraphs.

2.4 On-Detector Readout Electronics

The on-detector readout electronics are housed within a Super-drawer which is composed of up to four Mini-drawers (MDs). A single MD contains 12 PMT Blocks, 12 FEN-ICS boards, 1 Mainboard, 1 Daughterboard, and a High-Voltage Bus board.

2.4.1 Photo-Multiplier Tube Block

Scintillation light from a TileCal cell is transferred via Wavelength Shifting (WLS) fibres to a Photo-Multiplier Tube (PMT) Block that is housed within a Mini-drawer. A PMT

block is illustrated in Figure 2.6. A PMT Block consists of a tube made of mild steel that houses a light-mixer (light-guide), a Hamamatsu R7877 PMT (legacy PMTs) or Hamamatsu R11187 (10% replacement PMTs), its high-voltage divider, as well as the Front-End board for the New Infrastructure with Calibration and signal Shaping (FENICS). The PMTs amplify the optical signal received and convert it into an analog signal (current) that is conducted to the FENICS.

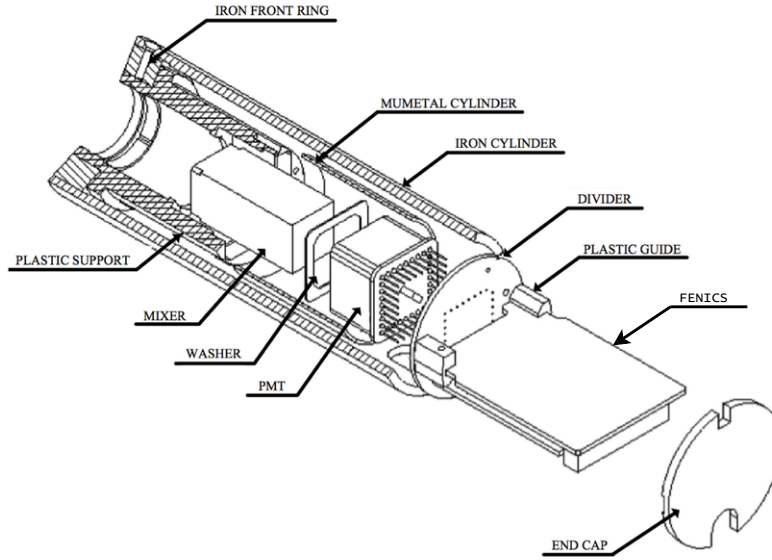


Figure 2.6: Schematic of a TileCal PMT Block.

2.4.2 Front End board for the New Infrastructure with Calibration and signal Shaping

The analog signal is then conducted to the Front End board for the New Infrastructure with Calibration and signal Shaping (FENICS) of which there is one per PMT Block. Each board has a two-stage fast readout with a shaper and an amplification chain which delivers two signals with a gain ratio of 1 and 32 to cover the dynamic range from 10 fC to 800 pC. The shaper is a linear passive filter with 7 poles leading to a pulse shape with a Full Width at Half Maximum (FWHM) of 50 ns (making a digitization at the LHC clock of 25 ns possible). After further amplification the analog signal is converted into a differential analog signal. The differential analog signal is then sent to the Mainboard (MB) via a double-pair cable (with tuned properties to ensure no signal distortion) to be digitized on a 12-bits Analog-to-Digital Converter (ADC). The FENICS also have an integrator readout. This readout is responsible for low averaged current typically induced by minimum-bias events, Van Der Meer scans, and Cs¹³⁷ calibration scans. It is composed by a low noise amplifier, an integrator with an integration time of 10 ms, and a system of switches and resistors to have six gains (0.3, 25, 25.3, 50.3, 125.3, 150.3 V/ μ A) to cover

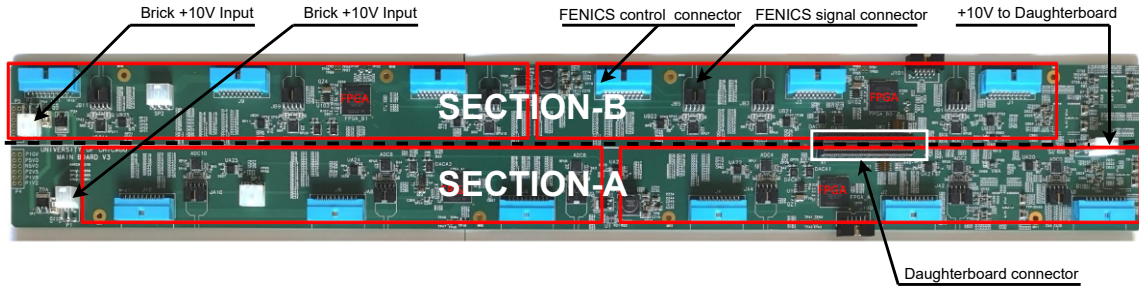


Figure 2.7: Labelled image of a Mainboard.

the dynamic range. The integrator analog output is sent to the MB to be digitized on a 16-bits ADC. The FENICS also contains two calibration sub-systems: the Charge Injector System (CIS) for the physics signal readout calibration, and current injection system for the integrator readout. The calibration systems will be explored in section 2.7.

2.4.3 Mainboard

One Mainboard (MB) is located in each Mini-drawer and is physically divided into two bilaterally symmetric sections called the A-side and B-side as can be seen in Figure 2.7. 6 PMT signals from the FENICS cards are routed in from each side. The two sides' electronics are completely independent, with each side having its own +10 V DC finger Low-Voltage Power Supply (fLVPS) Brick to power both its electronics, the attached FENICS, as well as its associated Daughterboard (DB). The fLVPS will be covered in depth in subsection 3.2.2. The MB electronics is grouped into 4 sections each serviced by a Field Programmable Gate Array (FPGA). To support the 3 PMTs, in each of the four sections, there are 6 channels of 40 Msps 12-bit ADCs and 3 channels of 50 kHz 16-bit ADCs for the slow integrators. Each FPGA controls low-gain and high-gain ADCs, including input bias-voltage levels. Both low-gain and high-gain fast signals from each PMT are digitised in parallel by a dual 12-bit 40 Msps ADC. The dual ADC data are sent to a DB at a speed of 560 Mbps. The other functionality of the FPGA is to serve as a communication hub between the FENICS cards and the Daughterboard.

2.4.4 Daughterboard

The Daughterboard (DB) serves as the high-speed on-detector communication interface connecting the TileCal front-end and back-end, situated in the USA15 region. As depicted in Figure 2.8, the DB design is bilaterally symmetric and employs a redundant scheme, where each half (A or B) of the board operates independently and is independently powered by +10 V from the Mainboard. The DB is linked to the Mainboard via a 400-pin FMC docking connector and multi-gigabit optical links to the off-detector Tile Pre-Processor (TilePPR). Utilizing four redundant GigaBit Transceiver optical links operating

at 9.6 Gbps, the DB packages and transmits digitized channel data to the TilePPr. Additionally, the TilePPr communicates Detector Control System (DCS) and run-configuration data to the DB over 4.8 Gbps links. The DB also includes two cable interfaces with the Cesium calibration system and the on-detector high-voltage interface (HV-OPTO). Due to ongoing revisions, the DB design has not been finalized, with the latest version being V6. For further details, refer to [41].

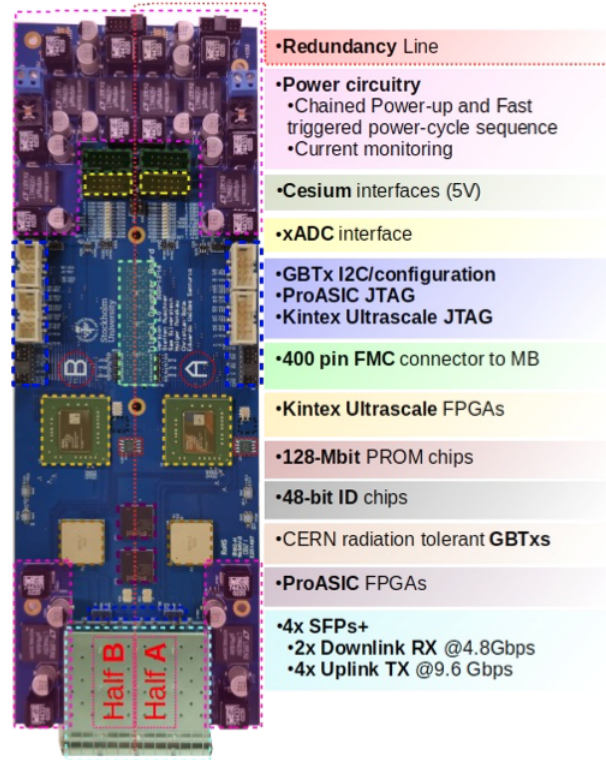


Figure 2.8: Image of the Daughterboard version 6 [41].

2.5 Off-Detector Readout Electronics

2.5.1 TileCal PreProcessor

The TileCal PreProcessor (TilePPr) serves as the central component of the back-end system, responsible for receiving digitized data transmitted from the on-detector electronics and storing them in pipeline memories (with a capacity of $(10 \mu s)$) while awaiting a trigger decision. Additionally, it acts as the interface between the front-end electronics and the ATLAS TDAQ. A TilePPr module, illustrated in Figure 2.9, consists of an Advanced Telecommunication Computing Architecture (ATCA) Carrier board equipped with four Compact Processing Modules (CPMs) and one Trigger and Data Acquisition interface

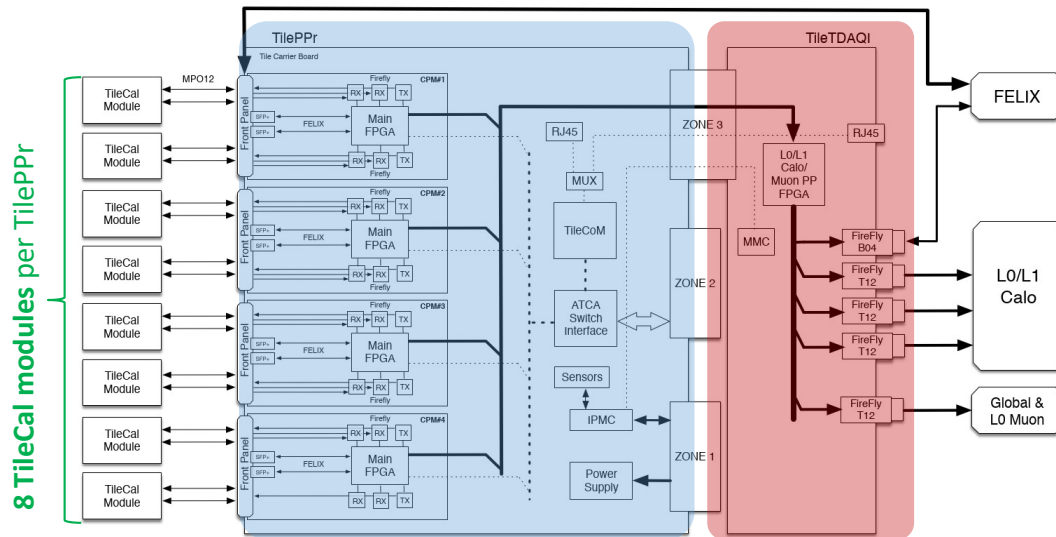


Figure 2.9: Block diagram of TilePPr and TDAQi.

(TDAQi). Embedded within the PPr is a Tile Computer-on-Module (TileCoM) mezzanine. Each TilePPr has the capability to read out and manage up to 8 TileCal modules, necessitating a total of 32 TilePPrs to fully read out the entire TileCal detector [42].

Each CPM communicates with two TileCal modules, 1 in the Long-Barrel and 1 in the Extended-Barrel, to minimize the impact of a CPM failure on detector performance. Each CPM is able to process the data from 8 mini-drawers (2 TileCal Modules). Therefore, 32 TilePPr are needed to read-out the entire detector. The CPMs utilize high speed optical connections to communicate with the FE electronics and are responsible for the TTC distribution to the detector, run configuration of the on-detector electronics, data acquisition, cell energy reconstruction, and data transmission to the TDAQi. Cell energy reconstruction will be briefly covered in section 2.7. The interface with the Front-End Link eXchange (FELIX) system for data readout will be implemented in the CPMs whereas the TDAQi will provide the trigger primitives monitoring. Upon receiving the Level-0 trigger signal, the data will be transmitted to the FELIX via the TDAQi. Data can be forwarded to or from multiple destinations connected to a network such as data-acquisition, monitoring, detector control, calibration, or configuration systems [43].

The TileCoM mezzanine carries out three main functionalities. These include remote configuration of on-detector electronics and TilePPr FPGAs, interfacing the TilePPr with

the ATLAS Trigger and Data Acquisition (TDAQ) system and Detector Control System (DCS) [44].

2.5.2 Trigger and Data Acquisition interface

The Trigger and Data Acquisition interface (TDAQi) module, a custom-designed Advanced Telecommunication Computing Architecture (ATCA) Rear Transition Module, is attached to each PPR, totaling 32 in all. It facilitates the interface between the TilePPr and the FELIX and trigger processors. Housing the Trigger FPGA, the TDAQi receives calibrated energy and time data per cell from the CPMs in the PPr for every bunch crossing through low-latency links. The Trigger FPGAs compute trigger objects with varying granularity and energy resolution, such as electrons, jets, global triggers, and muons, transmitting the results through low-latency high-speed optical links to the first-level trigger (Level-0). These trigger processors encompass the Level-0 Muon (L0Muon) trigger system, the electromagnetic Feature Extractor (eFEX), the jet Feature Extractor (jFEX), the global Feature Extractor (gFEX), and the Global trigger system. Additionally, the TDAQi includes optical connections to FELIX for data validation sent to the trigger system.

2.6 Signal Reconstruction

As mentioned previously, the raw signal (current) from each TileCal channel (PMT) is shaped into the form of an analog pulse with FWHM of 50 ns and amplified by the FEN-ICS. The signal is then sent to the Mainboard where digitization takes place every 25 ns. The digitized signal is then sent off-detector to the TilePPr for online processing via the Daughterboard.

Within the TilePPr the electrical signal for each TileCal channel is reconstructed from seven consecutive digital samples, taken every 25 ns. These samples are referred to as S_i where $1 \leq i \leq 7$, and are in units of ADC counts. Depending on the amplitude of the pulse, either high- or low-gain is used to maximised the signal to noise ration while avoiding saturation. The reconstruction of the signals amplitude, time phase, and pedestal (electronic noise) during physics runs is done using the Optimal Filtering (OF) technique [45].

The signal amplitude (A), time phase (τ), and pedestal (p) for a channels pulse are calculated using the ADC count of each sample S_i taken at time t_i with respect to the LHC 40 MHz clock:

$$A = \sum_{i=1}^7 a_i S_i \quad \tau = \sum_{i=1}^7 b_i S_i \quad p = \sum_{i=1}^7 c_i S_i \quad (2.1)$$

The weights (a_i , b_i , c_i) are derived to minimise the bias on the reconstructed amplitude, time, and pedestal introduced by electronic noise. A different set of weights is extracted for both high- and low-gain [46].

This technique weights the samples in accordance with a normalised reference pulse shape. The reference pulse shape used for all channels is taken as the average pulse shape from test beam data, with reference pulses for both high- and low-gain modes.

In each digitizer, the clock is adjusted to ensure that signal pulses, arising from collisions at the interaction point, reach their maximum amplitude at the central (S_4) sample in synchrony with the LHC clock. The resulting value of τ represents the slight time difference in nanoseconds between the expected pulse peak and the reconstructed signal peak, which arises from variations in particle travel time and uncertainties in the electronics readout.

This method involves assigning weights to the samples based on a normalized reference pulse shape. The reference pulse shape utilized across all channels is derived from the average pulse shape observed in test beam data, encompassing reference pulses for both high- and low-gain modes. The clock in each digitizer is adjusted to ensure that signal pulses, stemming from collisions at the interaction point, reach a peak at the central (S_4) sample, synchronized with the LHC clock. The reconstructed value of τ signifies the slight time phase difference in nanoseconds between the anticipated pulse peak and the time of the actual reconstructed signal peak, resulting from variations in particle travel time and uncertainties in the electronics readout.

2.7 Energy Reconstruction and Calibration Systems

The energy of each TileCal cell is the sum of the energies from its two channels (PMTs). In each TileCal channel the signal amplitude is proportional to the energy deposited in the cell. Therefore, the OF algorithm can be used for energy reconstruction. The raw amplitude of a signal pulse $A(ADC)$, as determined by the OF algorithm, is converted to channel energy ($E_{channel}$) within the TilePPr according to the following formula:

$$E_{channel}(GeV) = A(ADC) \cdot C_{ADC \rightarrow pC} \cdot C_{pC \rightarrow GeV} \cdot C_{cesium} \cdot C_{laser} \quad (2.2)$$

Where $C_{ADC \rightarrow pC}$ stands for conversion of the Analog-to-Digital Converter (ADC) counts to charge in pC. $C_{pC \rightarrow GeV}$ is the relation between the detector response (in pC), and the energy deposited within the detector (in GeV). This constant was determined during dedicated test beam campaigns. Finally, C_{cesium} and C_{laser} are used to maintain the energy scale constant. These above constants are determined by dedicated calibration systems of the same name. The $C_{pC \rightarrow GeV}$ is fixed whereas the remaining calibration constants evolve in time and are provided by individual systems which will be described in more detail in the subsections to follow.

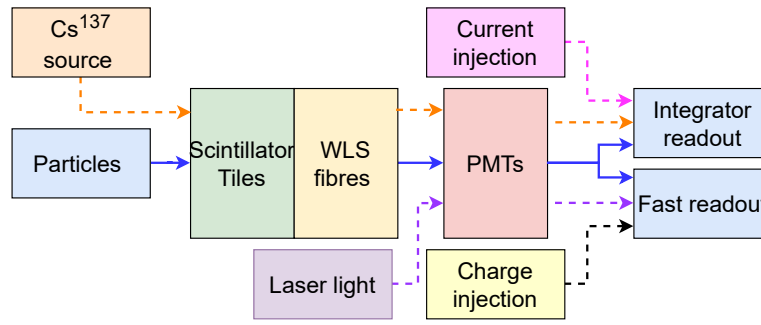


Figure 2.10: Flow diagram of the read-out signal path of the TileCal calibration systems. [23]

2.7.1 Cs-137 System

The TileCal utilizes Cs^{137} γ -ray sources, propelled by a hydraulic system, to calibrate and monitor its optical components (scintillators, WLS fibres, their optical coupling, etc.) and the PMTs [47] by extracting the C_{cesium} constant for each readout channel. The system is composed of three identical sections, one for the long barrel and two for extended barrels. They are functionally independent, and have identical sets of sensors on the source paths, source garages, hydraulics drives, front-end electronic modules and power supplies. The source tubes in which the Cs^{137} capsule traverses the TileCal module layers can be observed in Figure 1.12.

The Cesium calibration system is able to correct the residual non-uniformities after the gain equalisation of all channels and thus preserve the electromagnetic energy scale of the calorimeter. A Cs-scan of the TileCal consists of source that traverses all modules (not including gap and crack cells) and deposits a known energy of 0.662 MeV gamma rays within the cells. Cs-scans are undertaken approximately once per month during a dedicated 8 hour slot in which no activities are undertaken in UX15 (maintenance, collisions, etc) and are directly overseen by the TileCal operations team. When a scintillating tile is traversed by the Cs^{137} source, the emitted gamma rays induce light in the scintillator. The light is transported to a PMT via WLS fibres. The system makes use of a separate integrator read-out, as described in subsection 2.4.2, from that of the physics read-out. A paper by G. Blanchot et al. provides a detailed description of the current Cs-137 calibration system which was upgraded for LHC Run-II [48].

The upgrade of the TileCal readout electronics, new radiation hardness requirements and the ageing of existing electronic boards necessitate the upgrade of the Cesium calibration system control electronics [49]. These electronics are located within various positions within UX15. The Cs-137 on-detector modules are particularly noteworthy as their radiation hardness requirements are the same as those of the fLVPS due to their location.

The Cs calibration system was designed to operate for the duration of the original

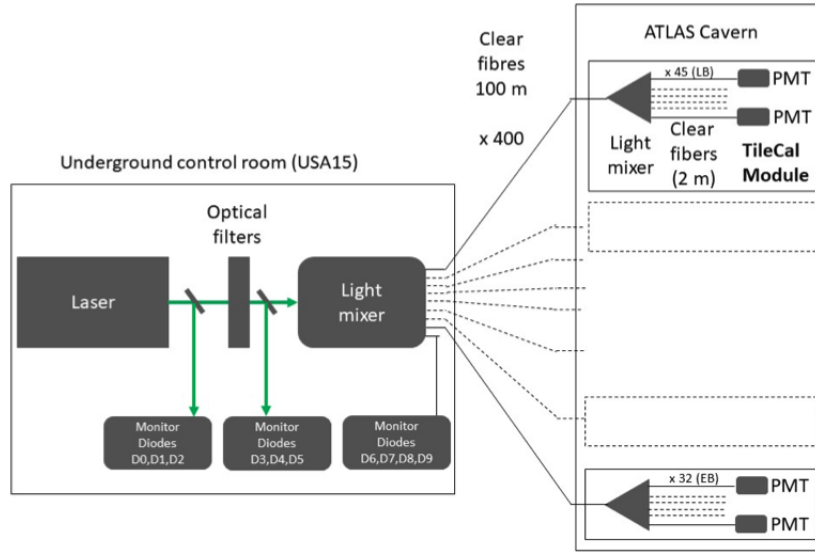


Figure 2.11: Functional block diagram of the Laser calibration system.

ATLAS design lifetime (10 years). The considerable increase of ATLAS experiment lifetime (>25 years), as well as recent problems caused by the hydraulic equipment ageing and wear motivated upgrades. The aging of the Cs system is becoming apparent as small leaks were detected in the long-barrel in early 2023. A successful intervention was undertaken whereby a commercial sealing additive was added to the working medium (de-mineralized water) after which multiple pressure tests were performed. A successful pressure test was conducted in February 2023 in which a stable pressure of 2 ATM was maintained thereby allowing for Cs scans to safely resume.

2.7.2 Laser System

The Laser system monitors the PMTs and the readout electronic components by extracting the C_{laser} constants for every readout channel. It can be operated independently (stand-alone) or inside the TDAQ infrastructure. The stand-alone operation of the Laser system allows for the verification of the system response, to monitor its stability, and to perform its internal calibration. The TDAQ mode is the main operating mode of the Laser system [50], in which a calibration trigger, that is requested and acknowledged by the CTP, is used to pulse light of known intensity into the detector, within empty bunch-crossings (the "abort gap"). This allows for the monitoring of fast gain variations during a physics run as well as the timing of the energy deposits. Additionally, dedicated scans are undertaken once per day shortly after the beam has been bumped, during the inter-fill period.

The TileCal laser system is installed in the ATLAS main service cavern, USA15, and is therefore not subject to radiation hardness requirements. It consists of a laser source,

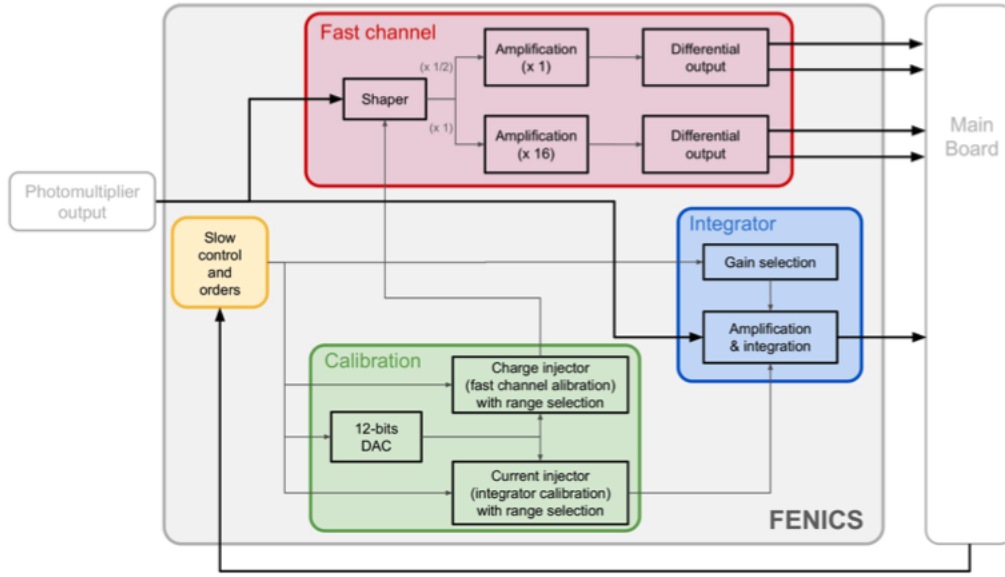


Figure 2.12: Functional block diagram of a FENICS.

light guides and beam expanders, an optical filter wheel to adjust the light intensity, and beam splitters to simultaneously dispatch the uniform light to all of the TileCal PMTs through clear optical fibres. In addition, the system is equipped with a calibration setup designed to monitor the light in various points of the dispatching chains. This as the actual intensity of the pulses has variations of approximately 5 %. Therefore, the system includes dedicated photodiodes to precisely measure the intensity of each pulse.

The optics box (laser source and optical components), and the electronics (laser control system and interface to the TDAQ) will be replaced due to ageing and they will also be modified to comply with the ATLAS Phase-II TDAQ system.

2.7.3 Charge and Current Injection Systems

The Charge and Current injection systems are used to calibrate the fast (physics) and slow (integrator) readout channels, respectively. The calibration systems both inject signals with similar properties to those produced by the PMTs and of precisely known amplitude over the entire dynamic range of the readout ADCs located on the Mainboard, as discussed in subsection 2.4.3. As mentioned in subsection 2.4.2, The Charge and Current injection systems are located on each and every FENICS allowing for the calibration of every readout channel. A functional block diagram is illustrated in Figure 2.12 in which both the fast and integrator readout are depicted.

The Charge injection system is used to determine the $C_{ADC \rightarrow pC}$ calibration constant for every fast readout channel. This constant gives the relation between the value of the charge produced by the PMT and the amplitude of the signal pulse expressed in ADC counts.

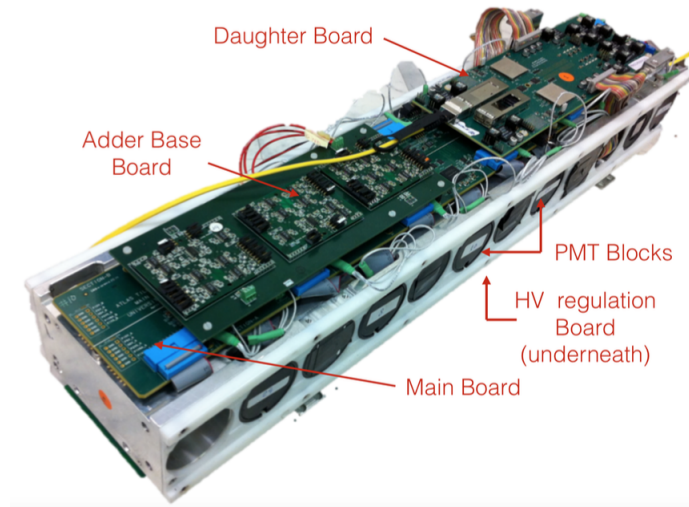


Figure 2.13: A hybrid Demonstrator mini-drawer.

A current spike of known amplitude is injected into the fast readout by the Charge injection system. The spike is produced by the discharge of one, of two possible, precision capacitors into the fast readout shaper circuit. The two capacitors allow for the calibration of the entire dynamic range of the fast channel covered by the two gains (low- and high-gain). During data taking both capacitors are directly connected to ground via fast low-resistance switches. When one of the switches is opened the associated capacitor can be charged by a voltage that is applied by a 12-bit on-board DAC across a resistor. When the switch is closed the capacitor discharges producing a current spike. A pulse of known amplitude is then produced by the shaper that is almost identical to the shape of a physics pulse.

The Phase-II upgrade Charge Injection System makes use of a new injection switch that leads to the significant improvement in the linearity seen in the charge injection calibration.

The main function of the slow readout channel is to monitor any current induced by continuous energy deposits, as mentioned in subsection 2.4.2. The sources of the continuous energy deposits span 7 orders of magnitude. Therefore, 6 programmable gains are required to cover the entire dynamic range of the 16-bit ADCs. The 6 gains are defined by six transimpedance values (a transimpedance amplifier circuit is employed) obtained using different combinations of four resistors. The calibration of the selectable transimpedances is done using a reference current that is produced when a known voltage is applied to a precision resistor.

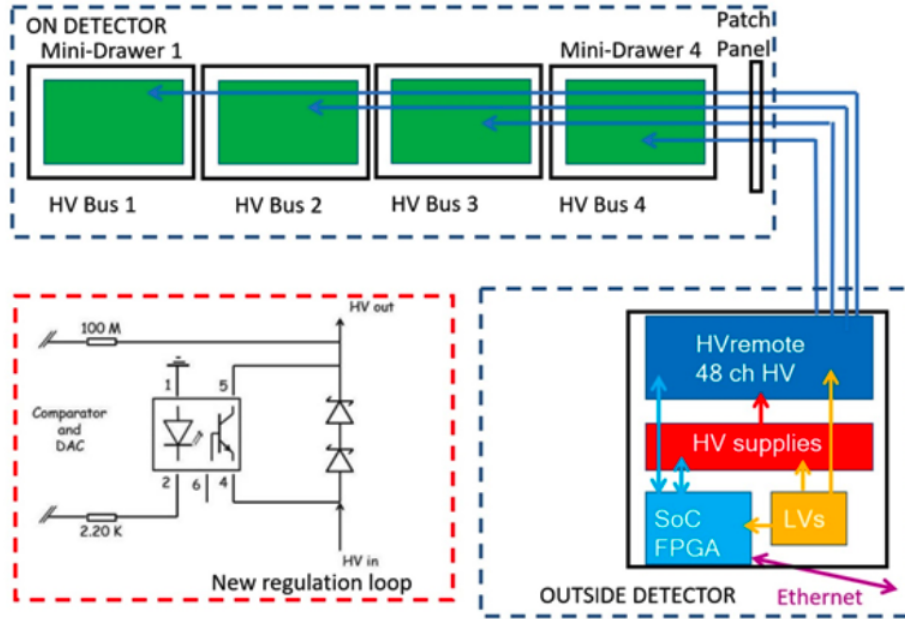


Figure 2.14: Block diagram of the remote High-Voltage (HV) power distribution system as well as the HV regulation loop.

2.8 High-Voltage Power Distribution System

The Phase-II Upgrade High-Voltage (HV) Power Distribution System will feature a remote regulation setup located off-detector and situated in technical cavern USA15. Compared to the current TileCal HV system, the primary functional enhancement involves the incorporation of on/off control for each group of 4 PMTs (channels). This HV system comprises HVremote boards and HV supplies boards, housed in crates in USA15 and connected to the detector via 100-meter-long cables. Within the detector, entirely passive HVbus boards (1 per mini-drawer) distribute HV to each PMT within the mini-drawers [51].

The HVremote boards regulate HV for individual PMTs using the regulation loop depicted in Figure 2.14. This new regulation loop is a modification of the legacy design currently utilized within TileCal, with minor enhancements made possible by the operation in the absence of radiation, allowing for the simplification of regulation loops through the removal of certain transistors. The number of HVremote boards required for the TileCal operation is 256.

A single input HV power supply (-830 or -950 V) can power up to 24 PMTs (channels). The voltage for each PMT (channel) can be adjusted down to 360 V, consistent with the legacy TileCal design.

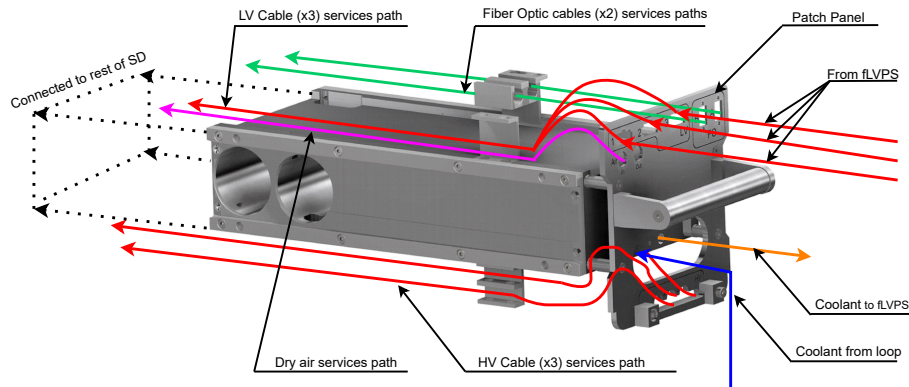


Figure 2.15: Computer Aided Design of a portion of an unpopulated Phase-II Upgrade Extended Barrel Super-Drawer with a Patch panel affixed. Note that the various services paths are "routed" through the patch panel.

2.9 Low-Voltage Power Distribution System

The Low-Voltage (LV) power distribution system is responsible for providing LV power to all on-detector read-out electronics and provides feedback and control through a monitoring system. The Phase-II upgrade LV power distribution system and its upgrade motivation will be covered in detail in chapter 3.

2.10 Detector Services

All TileCal SDs require electrical, optical, and cooling services to function. The services are run from their sources in USA15 or UX15 to ATLAS and then subsequently to the 256 TileCal Modules. These sources can be bulk power supplies, off-detector electronics or a cooling plant. The cooling services will be presented independently in section 2.11. The TileCal services are routed to patch panels that are affixed to each of the SDs as seen in Figure 2.15. These panels serve as an interface between the SDs and their services. It allows for a SD to be pre-assembled and installed as a homogeneous unit within a Module girder and then connected to the TileCal services for operation. A patch panel is the interface where services are interconnected to the SD internals. The connections take different forms depending on the service in question (electric connectors, fibre optic adapters, coolant quick connect couplings). The patch panel also serves a mechanical role in that it holds the High-Voltage (HV) cables, the Low-Voltage (LV) connectors and the fibre optic cable adapters in place. This is important so that the cables do not exert mechanical stress on the electronics to which they are connected.

There are two types of patch panel, one for the Long-Barrel (LB) modules and the other for the Extended-Barrel (EB) Modules. Two types are required as the SDs in the LB and EB are comprised of 4 Mini-drawers and 3 Mini-drawers, respectively. This is

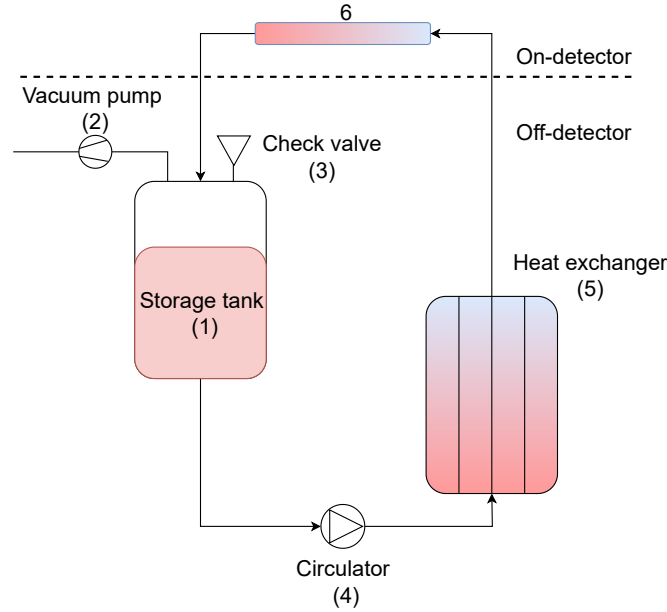


Figure 2.16: Functional block diagram of the TileCal Leakless Cooling System. Adapted from [52].

apparent on the Patch panels as and each Mini-drawer requires a dedicated HV and LV power input. Therefore, an LB patch panel has four cut outs for the LV input whereas an EB has three. There is also a minor change in the indexing on the HV bracket. A schematic of a Long-barrel Patch panel can be seen in Figure B.10 for further context.

2.11 On-detector Cooling

The TileCal on-detector cooling system will be presented in order to provide context to the cooling requirements of the on-detector electronics. These requirements are directly influenced by the efficiency of the fLVPS Brick which forms a core aspect of its development covered in chapter 4. The detector cooling requirements need to be calculated in order to determine if the current TileCal cooling plant has sufficient capacity for the Phase-II upgrade.

2.11.1 Leakless Cooling System

The TileCal employs a closed Leakless Cooling System (LCS) to extract heat from the on-detector electronics. The TileCal LCS was developed under the ATLAS Calorimeter Cooling Project which sought to design a common framework for the cooling systems of both the TileCal and the LAr Calorimeter. The LCS v.2 design was selected for use for both detectors [52]. The operating principle of this system as, described with reference

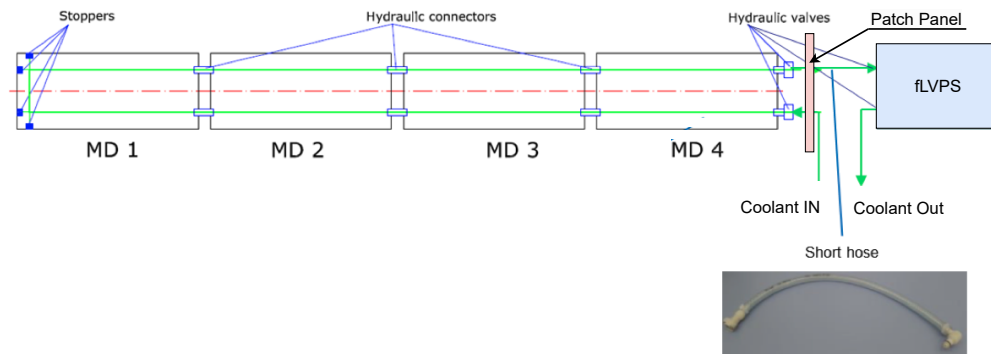


Figure 2.17: Block diagram of a TileCal Superdrawer illustrating the direction of coolant flow. Observe that the fLVPS receives coolant that has been heated by the front-end electronics.

to Figure 2.16, is that coolant is held in the storage tank (1) at sub-atmospheric pressure. This pressure is monitored and then maintained by a vacuum pump (2). The affect of the vacuum pump operation was previously illustrated in Figure 1.16. A check valve is attached to the storage tank (3) which discharges any excess air in the event overpressure. The coolant is moved by a circulator (4) into the heat exchanger (5) in which it is cooled. The coolant then circulates to the on-detector electronics whereby it extracts the heat produced by their operation after which it returns to the storage tank for the process to be repeated.

An LCS is necessitated when a coolant leak would result in fatal consequences for a detector, as would be the case for the TileCal. The cooling lines of the TileCal are a combined length of 2200 m and span the entire detector much like arteries and veins within a human. This can be seen in Figure 2.18. The cooling lines are further highly integrated into the TileCal Super-Drawer (SD) mechanics whereby they connect to the metal channels that run throughout the SD to facilitate heat transfer, as illustrated in Figure 2.17. The resulting discontinuities in the piping from routing to the detector, the integration into the mechanics, as well as the connectors to the fLVPS present numerous potential points of failure. These failure points would be adjacent to High voltage distribution boards and FE electronics for the former the fLVPS Bricks in the case of the later. As the pressure in the cooling pipes is lower than the atmospheric pressure a leak in the cooling circuit does not result in the leakage of coolant but rather air will be sucked into the system. This behaviour of the LCS has the added benefit that a leak in the cooling circuit will present itself as an increase in pressure within the storage tank. This in turn results in a proportionate increase in the frequency in which the vacuum pump is operated. Therefore, this frequency can be used to monitor the status of the cooling system as presented in section 1.4.2.

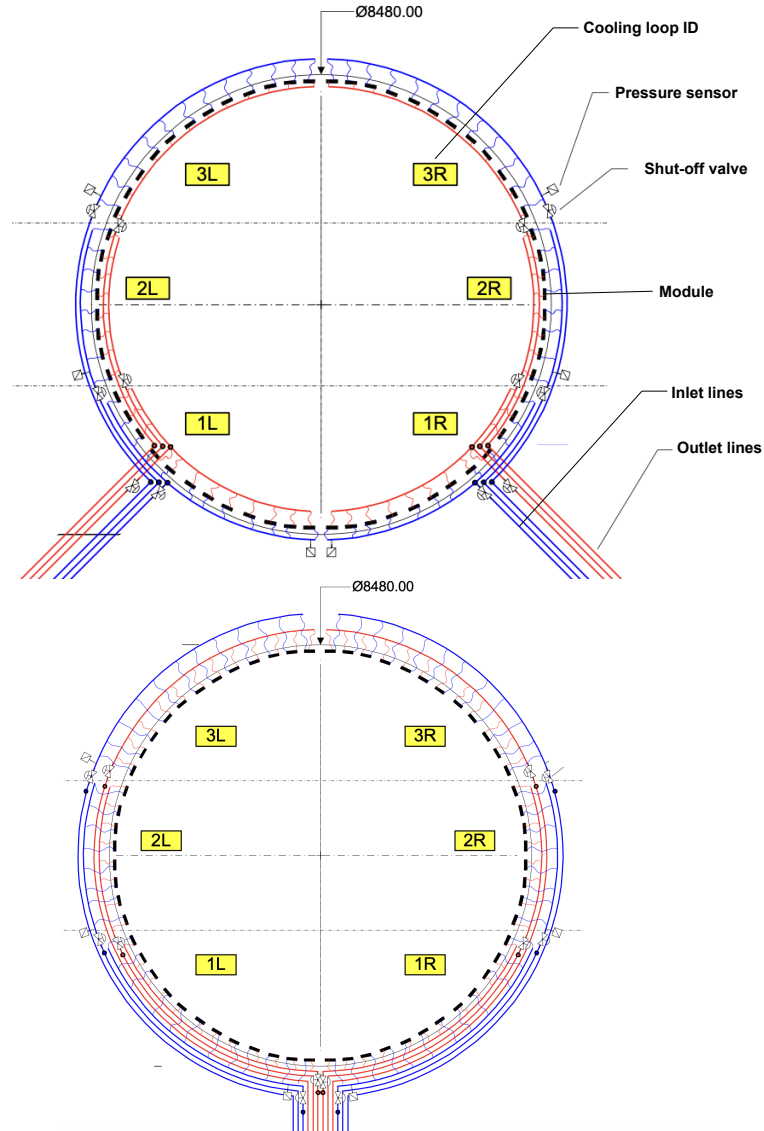


Figure 2.18: Schematics of the TileCal on-detector Extended-Barrel (Top) and Long-Barrel (Bottom) cooling circuit. Adapted from [52].

2.11.2 Cooling Requirements

The TileCal Front-End (FE) electronics and fLVPS produce a non-negligible amount of heat during normal operation. This heat needs to be extracted from the TileCal as it cannot be allowed to accumulate or radiate to its surroundings due to the associated degradation in performance as mentioned in section 1.4.2. The operating temperature of the FE electronics and fLVPS Bricks needs to remain within allowable limits as exceeding them would result in accelerated ageing or in extreme circumstances outright failure of components. The fLVPS Bricks have inbuilt over-temperature protection circuitry to prevent such an occurrence and will be discussed in section 3.4.

The current TileCal LCS makes use of a cooling plant with a 77 kW cooling capacity which was selected based on the legacy on-detector cooling requirements while allowing some headroom. It was assumed that each super-drawer and its associated fLVPS (regardless of position in EB or LB) require 300 W of cooling [53].

The TileCal LCS cooling circuits, for both the Extended- and Long-Barrel sections, are illustrated in Figure 2.18. Each of the 4 cooling circuits (1 per barrel section) are subdivided into 6 cooling loops. A cooling loop is the smallest portion of the cooling circuit that can be remotely opened and closed by the operation of an isolation valve. An individual cooling loop consist of an inlet line that brings 16°C coolant flowing at a rate of 86l/h to each of the 8 or 12 TileCal modules that it services. The modules are connected to the cooling loop in parallel ensuring that each modules receives input coolant of the same temperature.

TileCal Version	Location	Power to be extracted (w) per module	
		FE electronics	fLVPS
Legacy design parameters	Extended Barrel	200	100
	Long Barrel	200	100
Total = 76 800 W			
Actual legacy data 2018	Extended Barrel	120	80
	Long Barrel	170	74
Total = 56 832 W			
Upgrade design fLVPS 56% efficiency	Extended Barrel	138	108
	Long Barrel	184	144
Total = 73 472 W			
Upgrade design fLVPS 67% efficiency	Extended Barrel	138	68
	Long Barrel	184	90
Total = 61 440 W			

Table 2.1: TileCal Front-End (FE) electronics and fLVPS power extraction requirements for the Legacy design parameters, measured legacy system, Upgrade design with 56% and 67 % efficient fLVPS.

Chapter 3

Phase-II Upgrade Low-Voltage Power Distribution System

In this Chapter we will delve into the Phase-II Upgrade of the Low-Voltage Power Distribution System as we narrow our focus toward the crux of this thesis, that is the second stage of this system. We begin with a detailed presentation of the upgrade motivation while introducing key concepts such as Radiation Effects in Semiconductors and Radiation Hardness Qualification which present significant challenges to any development of on-detector electronics.

The distribution and regulation of low-voltage power will then be presented as this complex system is successively broken down into its constituents which comprise three distinct stages of voltage regulation as well as control and monitoring.

The second stage of the LV power and distribution system is looked at in significant detail with careful attention paid to the design history of the finger Low-Voltage Power Supply Brick. This is necessitated as the Bricks are iterative in nature with all previous insights and improvements having been incorporated into the upgrade design. The Chapter comes to a close with the Bricks physical design and a functional overview.

The aim of this Chapter is to provide all relevant technical details so as to equip the reader for the Chapter that follows in which we will look at the development of the phase-II Upgrade Brick.

3.1 Upgrade Motivation

Radiation Effects in Semiconductor Electronics

Radiation effects in semiconductor devices pose a serious concern for the performance and survival of devices operating in the ATLAS detector radiation environment. These radiation effects will be described in the context of Metal-Oxide Semiconductor Field-Effect Transistors (MOSFETs) therefore providing critical insight for section 4.2. The operation of a semi-conductor components in a detector radiation environment is generally subjected to a mix of particles with a wide range of energies. The energy and type of particles that the components experience is dependant on the energy of the initial colliding

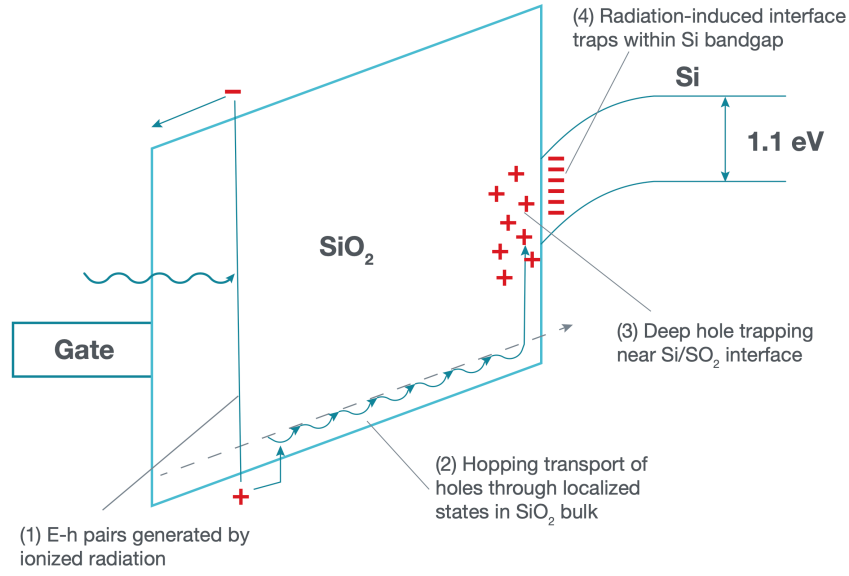


Figure 3.1: Band diagram of a Metal-Oxide Semiconductor device with positive gate bias showing the effect of ionizing radiation on carrier generation, transporting and trapping.[54].

particles at the Interaction Point (IP), their location relative to the IP, and the type and amount of material located between the IP and the components.

A high-energy particle will lose its kinetic energy as it traverses through matter (semi-conductor material in our case). As the energy is deposited within the semi-conductor various types of damage can occur. This damage can be broadly defined as either ionisation or displacement damage. The type of damage that occurs is dependant on the fundamental interaction between the impinging particle and the material (semi-conductor lattice). These can be either electromagnetic or nuclear interactions for ionisation and displacement damage, respectively.

Ionization damage is the dominant mechanism when energetic photons, protons, pions and ions interact with semi-conductor material. Different electromagnetic interactions occur depending on the energy of the photon. These, listed in order of increasing incident photon energy, are complete absorption (photo-electric effect), the Compton effect, and pair production. The amount of energy deposited in a material through ionising interactions is determined by the Linear Energy Transfer (LET) function:

$$LET = \frac{1}{\rho} \frac{dE}{dx} \quad (3.1)$$

that is defined as the energy loss per unit length normalized by the density of the material.

Total Ionizing Dose (TID) is the amount of energy deposited by ionisation within a

target material. TID effects are cumulative and are caused by the ionization of insulating films (such as SiO_2) used in modern integrated circuit technologies such as Metal-Oxide Semiconductor Field-Effect Transistors (MOSFETs). Electron-hole pair production by ionisation is the principle energy loss mechanism for high energy electron and ion irradiation in matter.

In the case of MOSFETs and With reference to Figure 3.1:

- Electron-hole pairs are created in SiO_2 layers by impinging ionizing radiation (1).
- The electrons created are highly mobile and rapidly move under the influence of the electric field created by the bias voltage to the gate electrode thereby not allowing for all of the electrons and holes to recombine. The holes, which have lower mobility, diffuse (2) close to or near the Si- SiO_2 interface where they accumulate as a charged layer.
- The holes are responsible for an accumulated positive charge in MOS devices during irradiation (3). The effect is the same as applying a positive voltage on the gate.

In Negative carrier MOS (NMOS) this shifts the device to the on state as during normal operation, which with enough accumulated charge can lead to a stuck on state, whereas in Positive carrier MOS (PMOS) the device shifts to the off-state. The radiation-induced buildup of interface traps right at the Si- SiO_2 interface. These traps are localized states with energy levels in the Si band-gap.

Single Event Effects (SEE) are instantaneous disruptions in semi-conductor devices resulting from the ionisation mechanisms described above. The traversal of a single energetic charged particle through the device ionizes atoms in a column along its track creating free electrons-holes pairs as illustrated in Figure 3.2. These charge carriers are prevented from recombining when in the presence of an electric field. For this reason SEEs are usually generated in reverse-biased p-n semiconductor junctions. These free charge carriers are eventually collected at the circuit nodes in the form of transient currents. The type of SEE that results from the traversal of a charged particle through a semiconductor device depends on various parameters such as the manufacturing technology of the device and the irradiation conditions. A distinction is made between destructive and non-destructive SEE. Non-destructive SEEs cause an observable event in the devices output whereas destructive SEE permanently damage or destroy the component. Examples of non-destructive SEE are Single Event Upsets (SEUs) and Single Event Transients (SETs). The effects of these SEE are a bit flip in digital storage elements and a transient voltage spike, respectively.

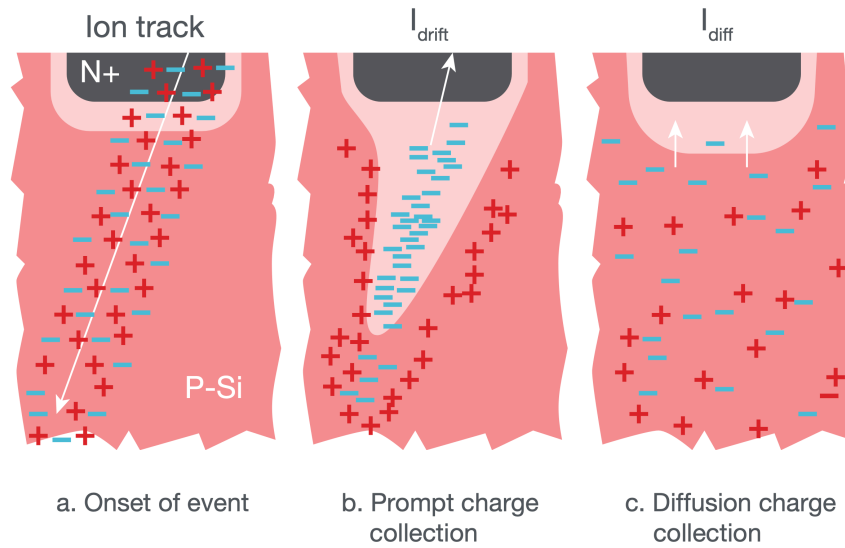


Figure 3.2: Phases in a reverse-biased p-n diode [55].

Common destructive SEE observed in MOSFETs are Single Event Burnout (SEB) and Single Event Gate Rupture (SEGR). A SEB results in an feedback mechanism whereby a current between the drain and source is initiated and increases until breakdown resulting in permanent destruction. SEGR once initiated allows a high current flow through the gate oxide creating destructive thermal runaway. SEE testing of commercial silicon power MOSFETS is covered extensively in [56].

For sufficiently high particle energies, the energy transferred via elastic or inelastic nuclear collisions may be sufficient to exceed the binding energy of the silicon atom, within the lattice, displacing it from its position and in doing so creating a localized vacancy. The displaced atom creates an interstitial, also known as a point defect, which is highly mobile at room temperature. This process is illustrated in Figure 3.3. If the recoil energy of the primary, knock-on, nucleus is higher than binding energy, this nucleus can produce displacement of yet another nucleus. A cascading-process will continue and a chain of vacancies and interstitials will produced until the recoil energy is below the binding energy of the lattice. The probability of such a displacement occurring is greater for incident particles with higher mass and/or energy and results in the accumulation of physical damage to the silicon crystal structure. This displacement damage is difficult to model making the calculation of the fractional energy loss of the incident particle during atomic displacements equally difficult to obtain. In order to calculate this value a parameter that plays the same role as LET for ionisation damage is needed.

3.1.1 Radiation Hardness Qualification

The radiation effects introduced in section 3.1 need to be considered when developing electronic devices for use within a radiation environment such as that experienced by

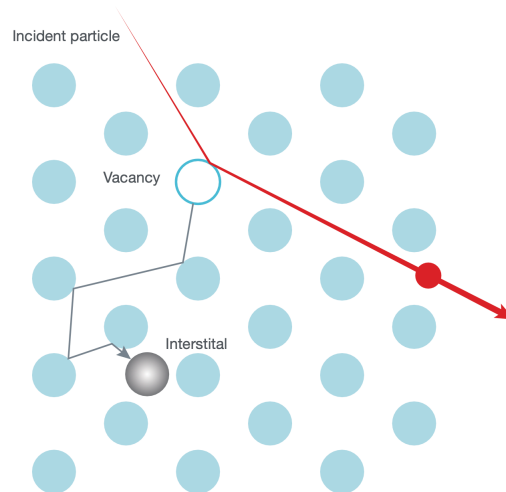


Figure 3.3: Vacancy (light gray) and interstitial defect (dark gray) created in a silicon crystal lattice (blue) by an energetic particle (red) [57].

the TileCal on-detector electronics and their associated finger Low-Voltage Power Supplies (fLVPS). This is not only to ensure nominal operation but also the longevity of the component/device.

One approach is to make use of aerospace grade electronic components which are certified for use within such environments. The type, rate, and energy of the radiation that they can endure and still operate nominally is indicated within their specifications. Although this is considered to be a "simpler" option these components are cost prohibitive especially when considering the unit number required for large experiments.

The second, preferred, option is to make use of Commercial Off-The-Shelf (COTS) electronic components. These components have the benefit of a low unit cost in comparison to an aerospace grade equivalent. They are however not qualified for use within a radiation environment (they have not been proven to be radiation hard). In order to address this shortfall the proposed fLVPS Bricks COTS components need to be independently qualified for use by the TileCal. A procedure for this qualification has been developed by the ATLAS experiment [58]. The procedure starts by determining the Simulated Radiation Level (SRL). From the SRL the Radiation Tolerance Criteria (RTC) are calculated by applying appropriate safety factors. The RTC serve as the test criteria. A proposed COTS component is selected for qualification. The batches of components then undergo qualification testing in dedicated irradiation campaigns for TID, NIEL and SEE making use of their respective RTC. If the tests are successful the qualified batches are purchased. This process will be applied below in order to obtain the RTC for the fLVPS components¹. These RTC will then be used for the qualification of an Phase-II Upgrade

¹It should be noted that it is a common occurrence that electronic manufacturers do not always guarantee that COTS components come from a single batch which if required may result in additional costs being incurred. Also, in some cases the single-batch components need to be procured prior to qualification as this

fLVPS Brick electronic component in section 4.2.

Simulated Radiation Levels within ATLAS

The radiation level induced in detector material is dependant on its location within the detector as with respect to the collision (interaction) point. Simulated Radiation Levels (SRL) have been computed for the various ATLAS regions, using GEANT4, in order to predict their radiation environment as a result of HL-LHC operation. These results were presented in section 1.4.4. In the context of Phase-II upgrade on-detector electronics the SRLs enable the prediction (to good approximation) of the radiation environment in which electronics are required to operate. The units for the SRL for TID, NIEL, and SEE are provided in Table 3.1 and their specific values for the entire fLVPS are located in Table 3.2.

Simulated Radiation Level	Unit
TID	Grey (Gy)
NIEL	1 MeV n _{eq} /cm ² ($\Phi_{n_{eq}}^{Si}$)
SEE	>20 MeV p+/cm ² (Φ_{20}^{had})

Table 3.1: Simulated radiation levels and their associated unit of measurement [59].

The units provided in Table 3.1 are not trivial and therefore warrant some explanation. The energy deposited per gram of material is called the dose (D) and is expressed in rads or Grays (Gy), whereby:

$$1 \text{ rad} = 100 \text{ erg/g} = 6.24 \times 10^{13} \text{ eV/g} \quad \text{and} \quad 1 \text{ Gray} = 1 \text{ J/kg} = 100 \text{ rad} \quad (3.2)$$

Particle fluence (Φ) is defined as:

$$\Phi = \int \phi dt \quad \text{where} \quad \phi = \frac{n}{At} \quad (3.3)$$

where ϕ represents the particle flux (number of particles (n) per unit area (A), per unit time (t)) integrated over the total exposure time.

The 1 MeV equivalent neutron fluence ($\Phi_{n_{eq}}^{1\text{MeV}}$) is used to express the neutral particle contribution in radiation and is usually specified for silicon as $\Phi_{n_{eq}}^{Si}$. The number of created lattice dislocations (bulk damage) in the irradiated material is to good approximation proportional to this quantity. It is the fluence of 1 MeV neutrons producing the same damage in a material as induced by an arbitrary fluence with a specific energy distribution. The displacement damage induced by neutrons in semiconductors can be normalized by displacement damages induced by 1 MeV neutrons through the hardness parameter (k) which is material dependant.

is the only way to guarantee that they do in fact come from a single batch. These considerations need to be taken into account when considering using a COTS component as they do pose significant risks.

That is:

$$\Phi_{equivalent} = k \int \phi(E) dE = k \Phi_{total} \quad (3.4)$$

Where the energy distribution of particle beam fluence is given by $\Phi(E)$ [60].

Safety Factors

Safety Factors (SF) are utilised in the Radiation Tolerance Criterion calculation, which will be presented in section 3.1.1. These factors account for uncertainties that are either unknown or intrinsic to given simulation estimates or testing procedures. A SF is a dimensionless constant and is subjective in nature as opposed to a traditional uncertainty value. When undertaking a risk assessment, which is required to determine the SFs for a component, the possible consequences of failure and possibilities to replace a failing component are considered. In practice the quantity considered is the product of risk and impact (cost, down-time, performance degradation). Efforts are made to minimise the above mentioned risk, but the procedure to achieve this can become too complicated or costly to be practical. If a failure would severely impact data-taking of ATLAS or if it could lead to cascading, or propagating damage, then exhaustive efforts should be made in order to minimise the risk. If, however, the failure would have no major consequences and if the component can be easily replaced, it might not be justified to select a more costly alternative. This methodology is highly subjective and utilises the decades of experience gained by the ATLAS experiment as well as a rigorous review process to ensure that the COTS components approved for the Phase-II upgrade are fit for purpose. In many cases it is preferred that the risk be estimated by exploring the failure margins of the COTS component. That is, the components are irradiated well beyond the defined RTC or even up to failure. Although such test might not be sufficient to provide absolute confidence they are likely to constrain most of the possible failure modes thereby increasing confidence.

The above considerations were taken into account when selecting the following safety factors for the Phase-II upgrade fLVPS Bricks. SF_{sim} is the Safety Factor applied to cover pure simulation uncertainties in SRL_x . A uniform value of $SF_{sim} = 1.5$ is applied, as is recommended throughout ATLAS, for all simulated radiation quantities.

SF_{test} is a newly introduced testing-related safety factor that accounts for uncertainties unique to the TID, NIEL and SEE testing procedures which are represented as SF_{TID} , SF_{NIEL} and SF_{SEE} , respectively.

SF_{TID} varies based on the technology of the component and the dose rate experienced during the irradiation campaign. For most components the damage due to TID depends not only on the total dose, but also on the dose rate. For some bipolar transistors the damage is typically larger at Low Dose Rates (LDR) which is known as the Enhanced LDR effect, or ELDR. To account for this the SF for bipolar components is chosen to be

$SF_{TID} = 5$. On the contrary, Complementary Metal-Oxide Semiconductor (CMOS) components have long been considered as exempt from LDR effects and therefore in this case $SF_{TID} = 1$.

$SF_{NIEL} = 1.3$ as the NIEL irradiation tests of the considered components were initially only performed in a monoenergetic beam. For new electronics tests with both protons and neutrons (mixed field) are strongly recommended in order to exclude possibly significant NIEL violation. These mixed field effects have become more apparent in recent irradiation campaigns undertaken by the ATLAS experiments sub-detectors and as such dedicated mixed field irradiation campaigns have been necessitated.

SEE testing of the fLVPS Brick components took place at the Paul Scherrer Institute (PSI) Proton Irradiation Facility (PIF) and will be further elaborated upon in section 4.2. An $SF_{SEE} = 2.0$ is applied to hadron fluences above $E_{cut} = 20 \text{ MeV}$ as is the case with the PIF beam. This SF is necessitated due to possible neutron interactions below 20 MeV of energy that are enough to trigger upsets in sensitive electronics.

SF_{lot} is a safety factor that accounts for lot-to-lot variation of the same type of components that occurs as a result of manufacturing inconsistencies [59]. $SF_{lot} = 1$ for all fLVPS active components as each component type is procured from a single lot thereby eliminating the need for this safety factor.

Radiation Tolerance Criteria

The ATLAS Radiation Tolerance Criterion (RTC) are calculated for all on-detector Phase-II Upgrade electronics to ensure reliable operation for 10 years (4 ab^{-1}) of operation of the HL-LHC. All on-detector components subject to the RTC are required to perform nominally and survive beyond their associated RTC. The ATLAS Phase-II Upgrade RTC for radiation effect x is defined as [59]:

$$RTC_x = SRL_x \times SF_{sim} \times SF_{test} \times SF_{lot} \quad (3.5)$$

Where RTC_x is expressed in the same units as SRL_x (dose or equivalent fluence). SRL_x represents the Simulated Radiation Level of the quantity relevant for radiation affect x . Several Safety Factors (SF) are applied as described in section 3.1.1. Therefore the TileCal RTC, as per Equation 3.5 can be expressed for the radiation effect types TID, NIEL and SEE as:

$$RTC_{TID} = SRL_{TID} \times SF_{sim} \times SF_{TID} \quad (3.6)$$

$$RTC_{NIEL} = SRL_{NIEL} \times SF_{sim} \times SF_{NIEL} \quad (3.7)$$

$$RTC_{SEE} = SRL_{SEE} \times SF_{sim} \times SF_{SEE} \quad (3.8)$$

The fLVPS radiation hardness requirements for 10 years (4 ab^{-1}) of operation of the HL-LHC are provided in Table 3.2 and are calculated using Equation 3.4, Equation 3.5 and Equation 3.6.

	Radiation effect	TID (Gy)				NIEL ($1 \text{ MeV } n_{eq}/\text{cm}^2$)		SEE ($>20 \text{ MeV } p+/\text{cm}^2$)	
	Location	LB		EB		LB	EB	LB	EB
	SRL_x	89.1		30.4		4.46×10^{12}	8.0×10^{11}	6.0×10^{11}	2.65×10^{11}
	Component type	Other	Bipolar	Other	Bipolar	All	All	All	All
Safety Factors	SF_{sim}	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5
	SF_{test}	1	5	1	5	1.3	1.3	2	2
	SF_{tot}	1	1	1	1	1	1	1	1
RTC	Mono-energetic	133.6	668	45.6	228	8.7×10^{12}	1.56×10^{12}	1.82×10^{12}	2.65×10^{11}
	Mixed field	-	-	-	-	6.69×10^{12}	1.20×10^{12}	-	-

Table 3.2: fLVPS Radiation Tolerance Criteria (RTC) in the Long-Barrel (LB) and Extended-Barrels (EB) of the TileCal for 10 years (4 ab^{-1}) of operation of the HL-LHC as of September 2023. It is important to note the date of the RTC values as they have been subject to change over the duration of the Phase-II Upgrade.

3.1.2 Low-voltage System Improvement

It was well understood from the onset that the TileCal Low-voltage (LV) System would need to be replaced as part of the Phase-II Upgrade due to its age and the new radiation hardness requirements imposed by HL-LHC operation. This necessary replacement was seen as an opportunity to implement design changes to the system that capitalize on experience gained during the production of the legacy LV system as well as decades of operational experience. A simplified block diagram of the present system is presented in Figure 3.4. As can be seen, it is a two-stage power distribution and regulation system. Stage 1 consists of commercial 200 V DC bulk power supplies located off-detector in USA15 where no radiation hardness requirements are imposed. The 200 V DC power is provided to the 256 fLVPS (Stage 2), located on-detector, via cables approximately 200 m in length. Within the fLVPS eight custom V7.5.0 Bricks facilitate the final step down of the voltage before providing it to the various on-detector electronics. There are eight types of V7.5.0 Bricks located in each fLVPS, within the current system, each of which having a tailored output for the particular local circuitry that it services. This results in each of the eight bricks being different in terms of the output voltage and current and necessitates different designs and components. Although the various Brick types made use of many common components and the same basic design their intrinsic differences presented challenges such as increased production costs while also calling for spares of each type be manufactured and stored for the duration of the experiment. To address these challenges a 3-stage LV system has been designed for the Phase-II Upgrade which will be covered in detail in section 3.2. The newly introduced third stage takes the form of Point-Of-Load (POL) regulators that are located on the Mainboards and Daughterboards presented in subsection 2.4.3 and subsection 2.4.4, respectively. These POL regulators

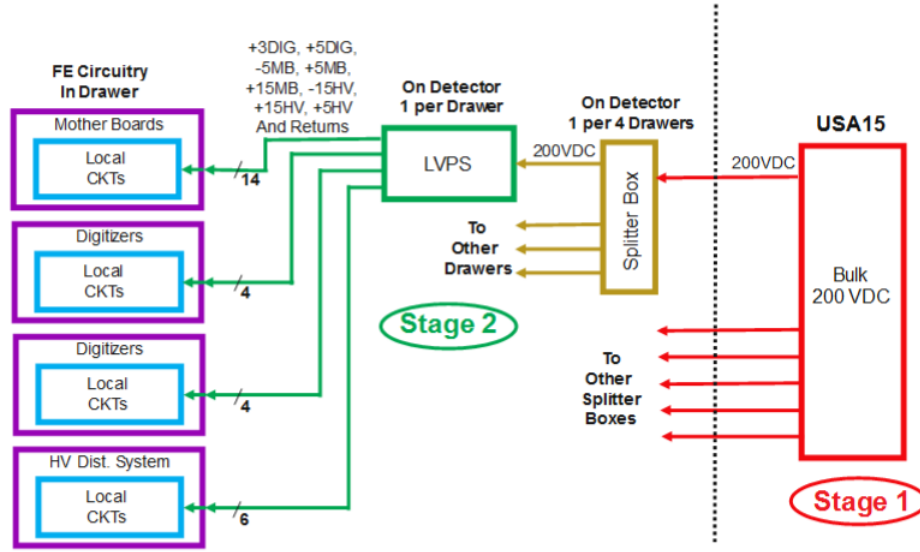


Figure 3.4: Block diagram of the present 2-stage Low-Voltage power distribution system. Note that the control and monitoring of the LV system are not included in this diagram[36].

facilitate the final step-down of the power received from the Bricks and in doing so allow for a single Brick type with a uniform output to be employed throughout the TileCal thereby addressing the aforementioned challenges.

The current LV system is separated into two groupings of Bricks within the fLVPS. One group supplies power to the High Voltage (HV) distributor electronics, and the second powers the digitizer and analog read-out electronics located on a MotherBoard (MB). Each group has different requirements. As mentioned in the preceding paragraph these requirements result in eight types of V7.5.0 Brick. Details of the legacy on detector electronics are provided in the 1996 TileCal Technical Design Report [39]. Three of these Bricks service the HV distributor boards with LV power and have +5 V, +15 V, and -15 V outputs. On the MB the read-out digitizer electronics are powered by +5 V and -5 V whereas the readout front-end analog electronics are powered by +5 V, -5 V, and +9 V Bricks.

The legacy LV system has the capability to power-cycle (switched off and on again) either the HV or MB group of the fLVPS or the entire fLVPS (both groups). Power-cycles can be initiated both automatically and manually and can be motivated by many factors. Automatic power cycles can be initiated by the Detector Control System when there is a trip of a single Brick which can happen in either the HV or MB side. In this case a shutdown of the fLVPS side affected will be initiated, followed by automatic restart. An automated power-cycle can also be initiated due to a trip of a full fLVPS, although this

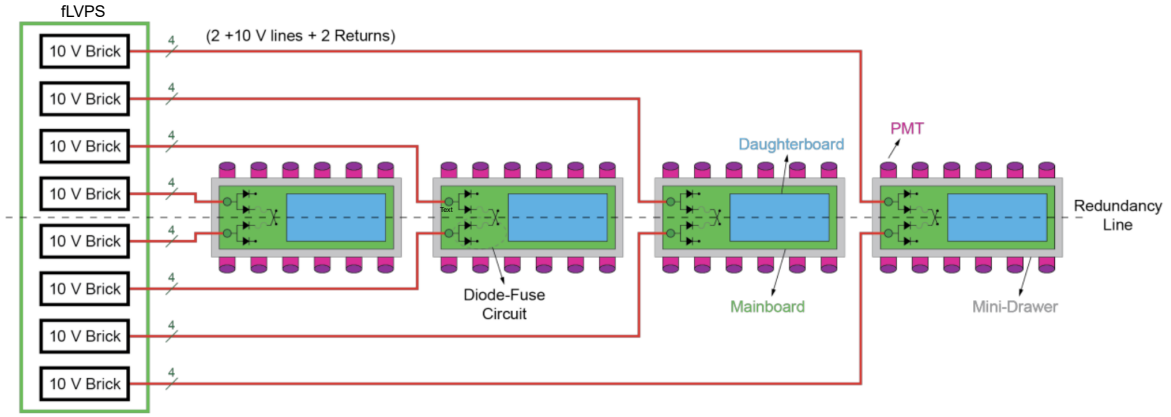


Figure 3.5: Block diagram of the proposed, but not implemented, Low-Voltage system single Brick redundancy [36].

is exceedingly rare. Other reasons for automated power-cycles are an over-current condition in the +5V MB Brick and on request from the DAQ which in both cases results in a power-cycle of the MB side. Manual power-cycles are undertaken when the initial automatic power-cycle requested by the DAQ (only fLVPS MB side) does not work which is apparent when there are still many of errors in the DAQ. By manually initiating a full power cycle we fully reset the front-end electronics which in most cases resolves the DAQ errors.

As the Phase-II Upgrade Front-End (FE) electronics have an entirely different architecture the power cycling of two groups of Bricks, as in the legacy system, is inadequate. This as each of the new Bricks powers an identical portion of the FE electronics. That is, a single Brick provides power to one-half of both the MB and DB as described in subsection 2.4.3 and subsection 2.4.4, respectively. The increase in modularity of the FE electronics has required a commensurate increase in the modularity of the fLVPS control which has taken the form of newly introduced tristate functionality. This functionality allows for the on/off control, as well as power cycling, of individual Bricks and will be described in detail in section 3.3.

In the current LV system, failure of only one of the eight V7.5.0 Bricks within an fLVPS will result in a loss of data from the entire module that it services. The aforementioned increase in modularity of the Phase-II Upgrade FE electronics reduces the impact of a single Brick failure to the loss of only one eighth of a module (half of a Mainboard and Daughterboard). It was proposed to implement redundancy in the LV system such that two Bricks will operate in parallel and provide power to both halves of the Mainboard and Daughterboard as illustrated in Figure 3.5. In case one Brick fails the other would provide the full output power needed by the entire MD. In the case that both bricks in the MD fail, only a fourth of the data from the entire module is lost. In this configuration fuses are added on the Mainboard of each MD in series with two schottkey diodes as an

added level of protection. The addition of the fuses was to prevent a hard fault on one side of the Mainboard, such as a short circuit, from disabling both sides. It was observed that during short conditions on one side of a Mainboard the fuse would not blow fast enough and would result in the other sides Brick tripping due to its over-current protection. The Brick would continuously trip as there was not sufficient time for the fuse to blow. Unfortunately, suitable fast fuses could not be identified which resulted in this design aspect not being implemented as there would be the potential for a fault isolated to one part of a Mainboard or Daughterboard to propagate to the entire MD instead of nullifying it. It should be noted that this circuitry is still present in all Mainboards produced for the Phase-II upgrade but is disabled by not inserting the removable fuses. The redundancy circuitry is illustrated in Figure 3.10 for completeness.

Although the phase-II Upgrade system is not redundant against individual Brick failures the increased modularity resulting from the implementation of the Super-Drawer and Mini-Drawer design concept, as described in section 2.2, coupled with the bilateral symmetry employed within the Mainboard and Daughterboard reduces the impact of a single Brick failure on data taking. This impact is reduced further as a single TileCal cell is read-out by two PMTs located on different sides of the redundancy line of a Mini-Drawer. Therefore, the failure of a single Brick will result in the loss of 8 channels (PMTs) but not of an entire TileCal cell. In addition to this reduction, the design of the new fLVPS Brick emphasizes reliability with a dedicated analysis into anticipated failure rates being conducted in section 6.2.

3.2 Power Distribution and Regulation

The Phase-II Upgrade power Low-Voltage (LV) distribution and regulation system consists of three stages as illustrated in Figure 3.6. Each stage has an associated transformation of the input power characteristics after which the transformed output power is provided to the next successive stage. The three stages listed from stage one to stage three are the bulk power supplies, finger Low-Voltage Power Supplies (fLVPS), and Point-Of-Load (POL) voltage regulators.

3.2.1 Bulk Power Supplies (Stage-1)

The first bulk power supplies used by the TileCal were of custom design and provided 200 V DC via three-channels to the 256 fLVPS. These were replaced with commercial single channel 200 V DC output power supplies during Long-Shutdown 1 (LS1) due to frequent hardware failures. The replacement power supplies, which are still in use, have a maximum output of 2.4 kW which allowed for the use of the existing 200 V DC infrastructure (cabling, splitter boxes etc).

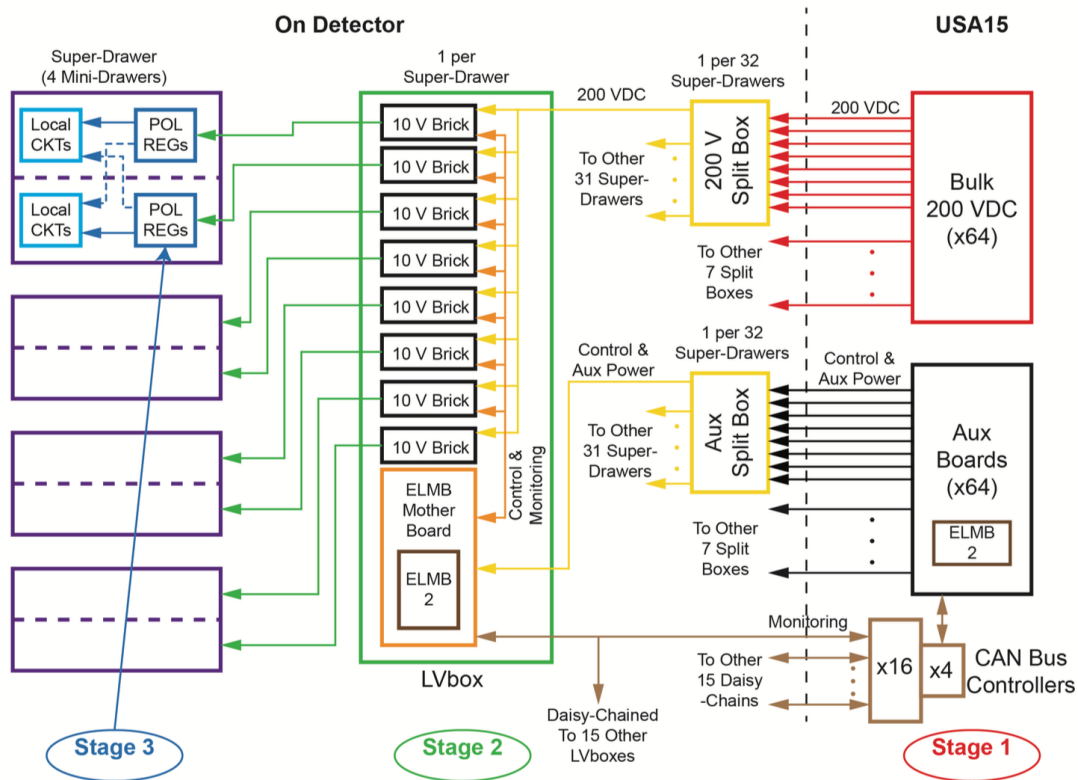


Figure 3.6: Block diagram of the Phase-II Upgrade 3-stage low-voltage power distribution system and its associated control and monitoring system [36].

The current single channel LV bulk power supplies will reach the end of their operational lifetime in 2025 thereby necessitating their replacement. Both the current and Phase-II Upgrade replacement bulk power supplies are Commercial Over-The-Shelf (COTS) hardware which is possible due to their location within USA15 which imposes no radiation hardness requirements on the electronics therein contained. COTS power supplies have the same benefit as COTS electronic components in that they have a lower per unit cost as compared to equivalent custom electronics, readily available spares, and manufacturer support. The location of the bulk power supplies within USA15 provides the additional benefit of year round access which has always been the case for the LV bulk supply. The first stage of the upgrade LV system will mirror that of the legacy system. There will be 64 new single channel bulk power supplies each of which providing 200 V DC power via 200 m long cables to a 1-to-4 splitter box which subsequently distributes the power to four adjacent fLVPS as illustrated in Figure 3.7.

3.2.2 Finger Low-Voltage Power Supplies (Stage-2)

The finger Low-Voltage Power Supply (fLVPS) constitutes the second stage of the LV system. Its location in the overall TileCal LV distribution architecture is shown in Figure 3.6.

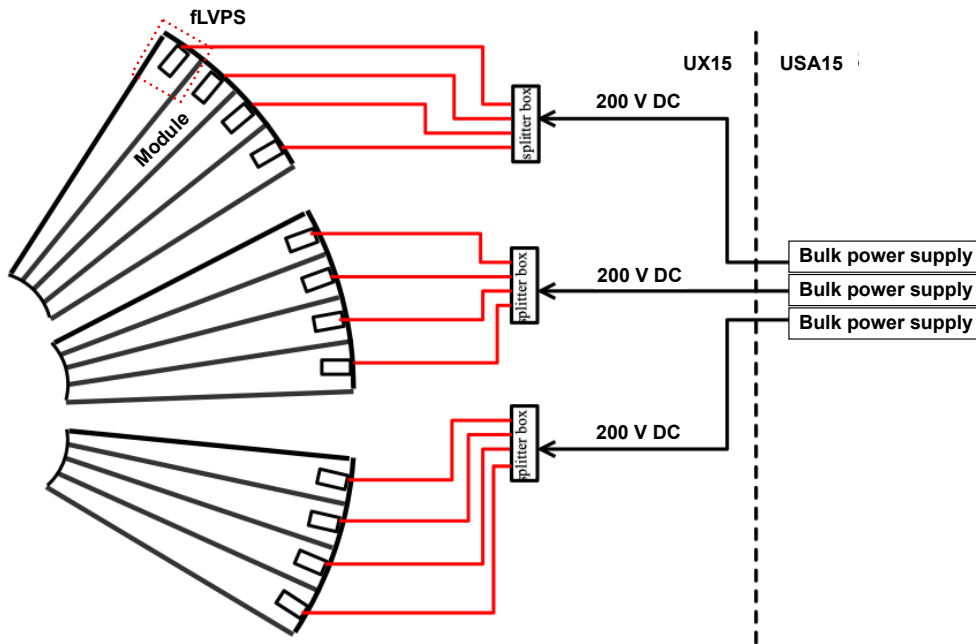


Figure 3.7: Block diagram illustrating the connection of three 200 V DC single channel bulk power supplies to 1-to-4 splitter boxes each of which distributing 200 V DC power to four adjacent modules fLVPS. There are 64 bulk supplies servicing all 256 fLVPS of the TileCal. Note that the fLVPS and module mechanical structure is not accurately depicted.

It functions to step-down 200 V DC power to 10 V DC power that is sent to the Point-Of-Load Voltage regulators (LV system 3rd stage) located on the front-end electronics. The fLVPS also provides control and monitoring capabilities of the Bricks therein contained. Each fLVPS supplies power to one Super-Drawer (SD) associated with a TileCal module and consists of the following components: A chassis, one Cooling plate, eight Bricks, a Fuse board, an Embedded Local Monitoring Board Motherboard (ELMB-MB), an ELMB, and a 72-pin Harting connector.

As can be seen in Figure 3.8, all fLVPS components are housed within a steel enclosure (Chassis) that acts as a shield not only against mechanical forces, but also against the ambient magnetic field generated by the toroidal magnets. The chassis is made out of two pieces of 1 mm thick steel sheet shaped by bending. The two pieces slide over one another. The choice of Chassis metal was made so as to have a magnetic permeability such that the field strength inside of it is maintained below 50 Gauss, as in the current version. The surface of the chassis sheets is anodized to prevent rusting. While the Phase-II Upgrade chassis is identical to the those currently in use, they cannot be recycled from the existing units since assembly of the new ones must commence well ahead of Long-Shutdown 3. Therefore, 256 Chassis will be produced.

The fLVPS overall physical dimensions are fixed at 175 mm x 170 mm x 156 mm due to the size of the available volume inside the fingers, where they must fit. These fixed

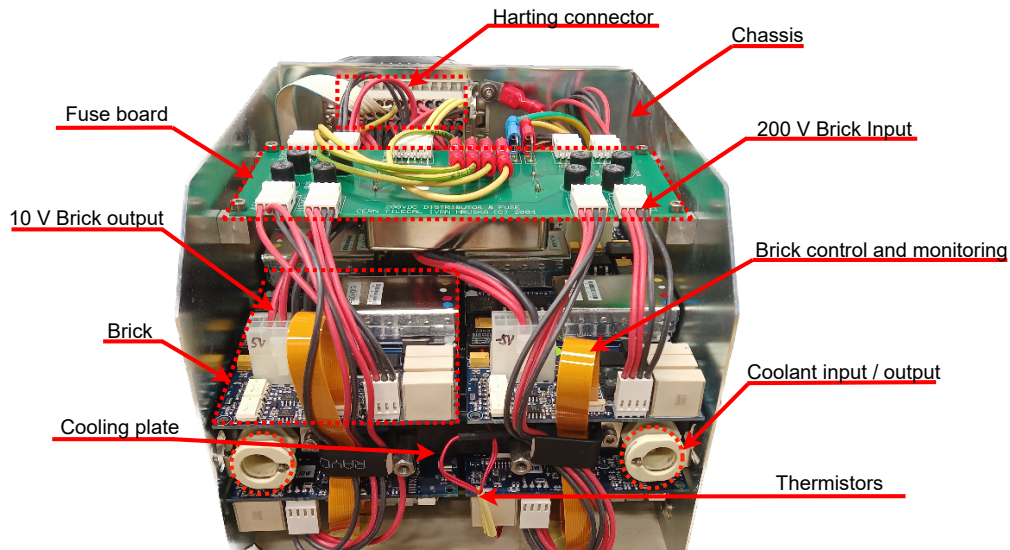


Figure 3.8: Labelled image of a finger Low-Voltage Power Supply (fLVPS) with its lid removed. Note that the Embedded Local Monitoring board (ELMB) and its Motherboard are not visible as they are on the "underside" of the fLVPS.

dimensions influence the form factors of all components within an fLVPS. Due to this limitation, all Phase-II fLVPS components have maintained the same form factor as the legacy components that they will replace. This decision was made due to the reduced complexity as opposed to overhauling the internal structure of an fLVPS as well as taking into account that the Phase-II fLVPS components are of an iterative design based on their associated legacy component. This approach allowed for reduced time and cost associated with the development of the Phase-II Upgrade fLVPS by building upon decades of previous research and development.

A water-cooled heat-sink, referred to as a cooling plate, is employed within an fLVPS in order to keep the operational temperature of the Bricks below their over-temperature protection trip point of 70°C , amongst other considerations. The cooling plates form part of the on-detector cooling system which was presented in section 2.11. A disassembled cooling plate, can be seen Figure B.2, and has dimensions of 166 mm x 145 mm x 20 mm.

Eight Bricks are located within an fLVPS where they are directly affixed to the cooling plate by nylon bolts with four Bricks mounted on the "top" and the other four located on the "bottom". The nylon bolts ensure grounding isolation between the Bricks and the heatsink and clamp the Bricks ceramic heat-conducting posts (with thermal paste applied at their thermal interface) to the cooling plate. During installation within an fLVPS "gap-pads" are inserted between two active components on the Brick and the cooling plate to assist in their cooling and will be further discussed in subsection 3.4.1. The structure of a Brick will be covered in detail in section 3.4, its thermal consideration and those of the fLVPS in general will be presented in section 4.1. Since a Long-Barrel Super-drawer has

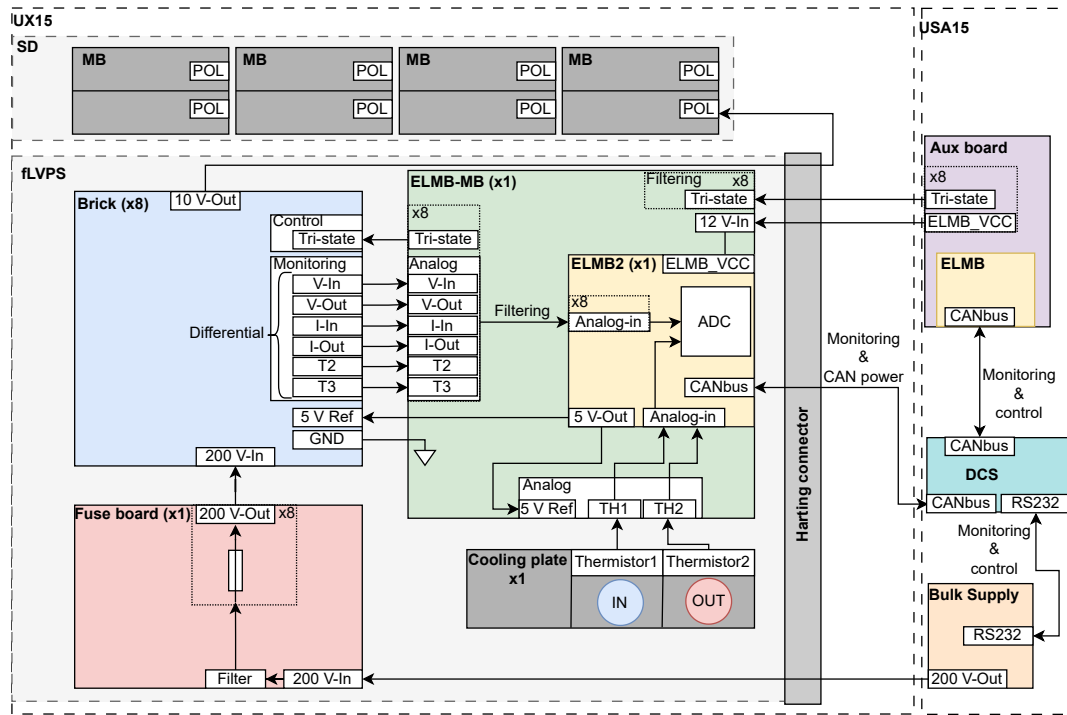


Figure 3.9: Block diagram of a finger Low-Voltage Power Supply (fLVPS), its components, as well as connections to the on-detector and off-detector electronics.

four mini-drawers, eight Bricks are required in the fLVPS whereas for an Extended-barrel Super-Drawer has only three mini-drawers and thus only six Bricks are required. For the sake of interchangeability should the need arise, eight Bricks will be put in all fLVPS regardless of their location within the TileCal.

The 200 V power received from off-detector is routed through a fuse-board, of which there is one per fLVPS, to the eight Bricks. The fuse-board distributes power in parallel to eight filtered outputs, one per Brick. The two stage symmetrical common mode Electromagnetic Compatibility (EMC) filter suppresses 300 kHz and higher harmonic frequencies noise generated by the Bricks thereby preventing propagation to the 200 V common bus. Each output has a dedicated fuse which guards the associated Brick from local faults. The fuses are 800 mA time lag fuses. Their specification is based on the Bricks specification of a nominal input current of 280 mA and max current rating of 880 mA. Although the maximum Brick current is greater than the nominal rating of the fuse, the fuse specifications state that currents up to 1.50 times the nominal rated can be maintained for a minimum of 1 hour without disruption. In the event of a catastrophic failure in a Brick, the fuses would prevent the failure from affecting the 200 V power supply and other Bricks in the fLVPS. The fuse-board also has a common point that serves as a reference node. This common point is connected to the fLVPS chassis, the finger, as well as the center point of the EMC filter. It is also connected to three electromagnetic shielding connectors, one for the CANbus cable, one for the 200 V DC cable, and another for the

Auxillary cable. The fuse-board also has a common point that serves as a reference node. This common point is connected to the fLVPS chassis as well as the center point of the EMC filter. It is also connected to three electromagnetic shielding connectors, one for the CANbus cable, one for the 200 V DC cable, and another for the Aux cable. A labelled image of a fuse-board is provided in Figure B.8.

There is one ELMB-MB per fLVPS as illustrated in Figure 3.9. The ELMB2-MB, which is the Phase-II Upgrade iteration, provides the interconnections between the ELMB2, the cabling from the Auxillary board in USA15, the CANbus network, and the eight Bricks. The ELMB2-MB also provides capacitive filtering and transient voltage protection of the LVPS tri-state control lines. The tri-state control of the Bricks will be discussed in section 3.3. The ELMB2-MB only makes use of resistors, capacitors, transient protection diodes and does not contain any active electronic components.

The ELMB2 is a general purpose plug-in board developed for slow-control and monitoring purposes of the LHC detector front-end electronics. It is backwards compatible with the ELMB which is currently used within the ATLAS detector [61]. The design and use of the ELMB2 was compelled by the obsolescence of some components, end-of-life problems anticipated during HL-LHC era, and more stringent radiation hardness requirements for the Phase-II Upgrade. The ELMB2 features 64 differential analog inputs that are digitized by a 16-bit ADC with allowable input ranges from 25 mV to 5 V and conversion rates from 2 Hz to 100 Hz. It also has 24 bi-directional digital Input/Outputs (IOs). An fLVPS makes use of 58 (7 per Brick and 2 cooling plate thermistors) of the ELMB2 analog inputs. It communicates the digitized temperature, voltage and current measurements via CANbus using the CANopen protocol to the DCS. The ELMB2 also provides the 5 V reference voltage for the Brick and cooling plate thermistors.

All electrical power and communication signals that go in to or come out of an fLVPS are channeled through a 72-pin Harting connector. These include the input voltage from the 200 V DC supply and eight output 10 V DC to the mini-drawer's front-end electronics as well as power for the ELMB2. Six CANbus lines are needed for the ELMB2. Eight tri-state control lines, one per Brick also pass through the Harting connector. A schematic of fLVPS wiring harness including the Harting connector can be seen in Figure B.3.

The fLVPS is included in the Superdrawer cooling loop and therefore the TileCal leakless cooling system in order to dissipate the heat generated by the Bricks as they are not 100% efficient. This interface is illustrated in Figure 2.17 with the TileCal cooling loop (circuit) structure is provided in the appendix to provide additional context Figure 2.18. The fLVPS receives the coolant once it has already passed through the Superdrawer cooling the front-end electronics. The coolant enters the cooling plate where it flows through a winding coolant channel until it exits the the cooling plate and returns to the cooling loop. The intake and exhaust coolant temperatures are monitored by two thermistors attached to the cooling plate adjacent to the respective connectors. An image of a disassembled cooling plate illustrating the internal cooling channel and the location of the

Parameter	Value
B Field	1000 G
Noise	< 20 mV RMS
Volume	175 mm x 170 mm x 156 mm
Efficiency	> 80%
Nominal Output Power	< 125 W

Table 3.3: Basic design parameters of the Phase-II Upgrade fLVPS. Note that the radiation hardness parameters are provided in Table 3.2.

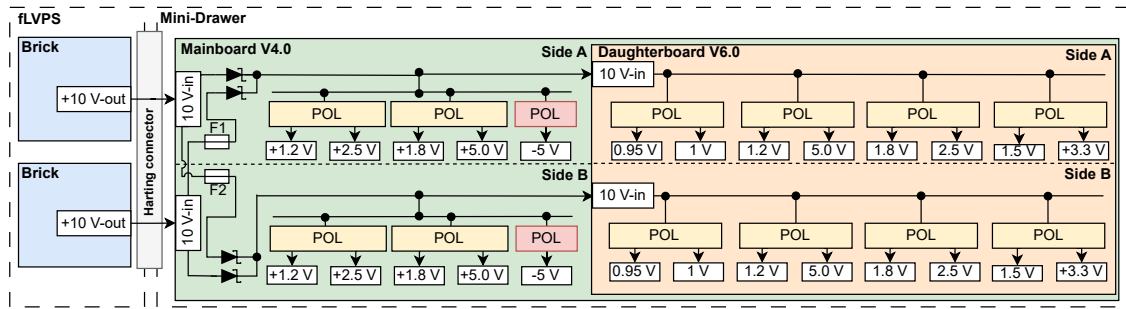


Figure 3.10: Block diagram illustrating the routing of 10 V DC power from two fLVPS Bricks to the Point-Of-Load (POL) voltage regulators located on a Mainboard and Daughterboard "pair". Note that the ORing of the input power from the two Bricks is included for completeness as it is present in the final Mainboards but the fuses labelled F1 and F2 are removed thereby disabling this functionality.

thermistors be seen in Figure B.2.

3.2.3 Point-Of-Load Regulators (Stage-3)

The third stage of the LV regulation takes the form of Point-Of-Load (POL) voltage regulators that are directly incorporated in the design of the Mainboard (MB) and Daughterboard (DB) which they service. The LV power distribution and regulation is bilaterally symmetric, about a redundancy line that runs through the centre of both the MB and DB Printed Circuit Boards (PCBs) which were discussed in chapter 2. Each side of both PCBs are entirely independent in all aspects with the caveat that there is redundancy in their power supply for which the circuitry is present but not utilised. The proposed redundancy was briefly discussed in subsection 3.1.2.

Two types of POL regulators are employed by the front-end electronics with the first and second POL regulator types indicated as yellow and red "blocks" in Figure 3.10, respectively. Each MB receives two channels of nominal +10 V DC from independent fLVPS Bricks with each channel being responsible for powering one half of the MB and the associated half of the DB. The white Brick input 4-pin headers can be seen on either side of the redundancy line of the MD in Figure 2.7. Each channel has its own power rail that is responsible for providing power to the MBs local POL regulators. The power rails

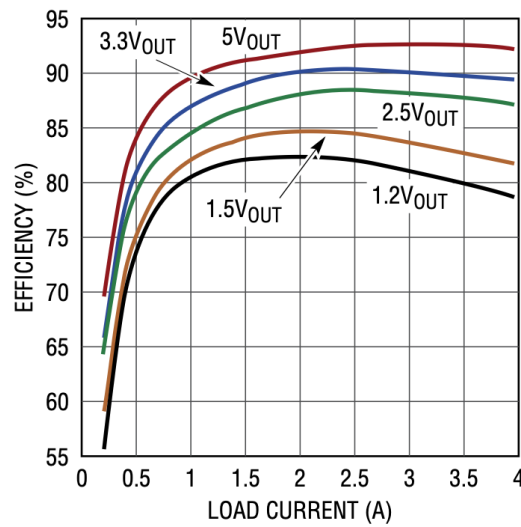


Figure 3.11: Linear Technology LTM4619 efficiency as a function of applied load for +12 V input and +1.2 V, +1.5, +2.5 V, +3.3 V, +5 V outputs as per the manufacturer specifications sheet. Note that the input voltage for all LTM4619 employed on the Mainboard and Daughterboard is +10 V nominal, as received from an fLVPS Brick, with an upper limit of +11.5 V imposed by the Bricks over-voltage protection.

are also independently connected to the +10 V DC power rails of each DB side. The two separate +10 V DC power 2-pin headers located on the DB, which are blue, are visible in Figure 2.8

The first type of POL regulator, which is used by both the MB and DB, is a (Linear Technology LTM4619) dual output standalone non-isolated switching mode DC/DC power supply that includes the switching controller, power FETs, inductor, and all support components within a compact single package. This POL regulator can receive input voltages ranging from 4.5 V to 26.5 V. It supports two outputs with voltage ranges of 0.8 V to 5 V, each set by a single external resistor. Each of these regulators can deliver 4 A continuous current (5 A peak) for each output. As can be seen in Figure 3.11, the LTM4619 is highly efficient which allows for heat sinking to be done via the PCBs themselves which radiate heat to the surroundings. There is inefficient thermal coupling between a MD and its Mini-drawer as nylon standoffs are used to connect the two.

The second POL regulator type takes the form of an entire 10 V input -5 V output inverting converter incorporated into each side of the MB. The converter is centred on a wide input voltage range inverting controller Integrated Circuit (IC). This IC as well as the power FETs, dual-inductor, and all support components form part of the MB design.

As can be seen in Figure 3.10, each side of an MB makes use of three distinct POL regulators to convert the +10 V DC input power received from a Brick to five logic voltages for both itself and the up to 6 FENICS cards. Each MB side has a +1.2 V, +1.8, +2.5 V, +5 V and -5 V outputs. All voltage levels are used by the Mainboard besides the -5 V which is routed to the FENICS cards.

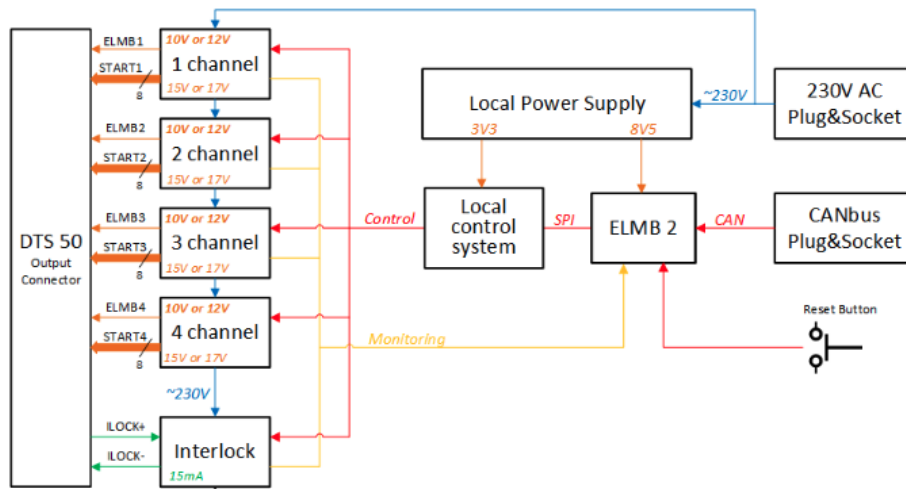


Figure 3.12: Block diagram of a Phase-II Upgrade Auxiliary board.

The DB employs four distinct POLs to regulate 10 VDC, that it receives from the MB, to eight locally utilised logic voltage levels. These are +0.95 V, +1.0 V, +1.2 V, +1.5 V, +1.8 V, +2.5 V, +3.3 V and +5.0 V outputs.

The output power characteristics are monitored for all of the POL voltage regulators located on the MB and DB. The MB measures its POL voltage levels, as well as the + 10 VDC input power received from the two Bricks, which are then buffered and routed to the DB for monitoring. Real-time signals of the voltage status and current draw are sent to the DB and monitored so that a reboot can be triggered if currents go above their thresholds. The DB similarly monitors the output voltages and currents of its POLs.

3.3 Control and monitoring of the Low-Voltage System

The Phase-II Upgrade Auxiliary Control Boards (AuxBoard) are the main off-detector elements of the remote control system for the TileCal finger Low Voltage Power Supplies (fLVPS). They are located in Underground Service Area USA15 with each one being responsible for servicing four consecutive fLVPS accounting for a total of 64 AuxBoards.

The AuxBoards are VME based printed circuit boards which operate on standard 220 V AC power. Each AuxBoard has passive components, transistors, six transformers to provide isolated power lines, and several connectors. An AuxBoard employs a local ELMB2, which was discussed previously in subsection 3.2.2, that serves as the interface with the Detector Control System (DCS) through CAN bus. The AuxBoard serves several roles each of which is depicted in the functional block diagram in Figure 3.12.

The AuxBoards provide remote on/off control of the on-detector fLVPS Bricks. This

control is implemented by the use of a tri-State system which enables the individual control of every Brick within the TileCal. The tri-state system, as its name implies, is composed of three distinct states that are referred to as Start, Run and Disable. Each state is defined as a specific voltage level on the tri-state cable that connects the AuxBoard to a Bricks start circuitry. The tri-state system will be further elaborated upon in subsection 3.4.3.

An Auxboard is responsible for providing independent 12 V DC power to each of the four ELMB2s located within the fLVPS that it services. The benefit of the ELMB2s being externally powered, and not for instance being powered by the Bricks, is that the monitoring is still possible even if the on-detector electronics are not powered on. This may have limited use as the ELMB2 mostly monitors various Brick performance metrics. That being said, the ELMB2 is also responsible for monitoring the cooling-plate temperature which has been useful in recent detector thermal performance studies.

The power lines (labelled ELMB1, ELMB2, ELMB3 and ELMB4) can be seen in Figure 3.12. These lines are run from the AuxBoard in USA15 to the TileCal modules where they are routed through the Harting connector of an fLVPS to the ELMB-MB, and then finally to the ELMB2 which is depicted in Figure 3.9. Each line can be controlled independently so that each on-detector ELMB2 can be turned on/off or power cycled without affecting the other three ELMB2s powered by the same AuxBoard. Each power line is protected by a dedicated fuse, so that in case of triggering of the fuse, only one ELMB2 would be turned off thereby preventing the propagation of the hardware "failure" of a single ELMB2.

An AuxBoards local ELMB2 allows for the monitoring of important currents and voltages on the board itself. One such current is that which powers the on-detector ELMB2. It is important that both current and voltage to the on-detector ELMB2s are monitored to allow for the detection of early signs of radiation damage. The AuxBoards local ELMB2 need not monitor the voltage of each of the outgoing tri-State lines, as these are monitored by the on-detector ELMB2.

The AuxBoards serve a key detector safety role in that they are responsible for providing the low-voltage system interlock as part of the TileCal interlock which is illustrated in Figure 3.13. This low-voltage interlock functions to shut down the off-detector bulk 200 V DC power supplies if fault criteria are met. The interlock feature is implemented on the AuxBoard using a current loop. As can be seen in Figure 3.13 there are a total of 64 low-voltage interlock loops, 1 per AuxBoard. The AuxBoard injects a small current of approximately 5 mA into its dedicated current loop, which is monitored by the Detector Safety System (DSS) of ATLAS. In case of emergency the DSS opens the loop and the 200 V DC power supplies servicing the four associated fLVPS will be switched off. The fLVPS Bricks will subsequently switch off as well as the front-end electronics to which they provide power. The Bricks will remain off until the interlock fault is remedied and a tri-state Start signal is requested by the DCS.

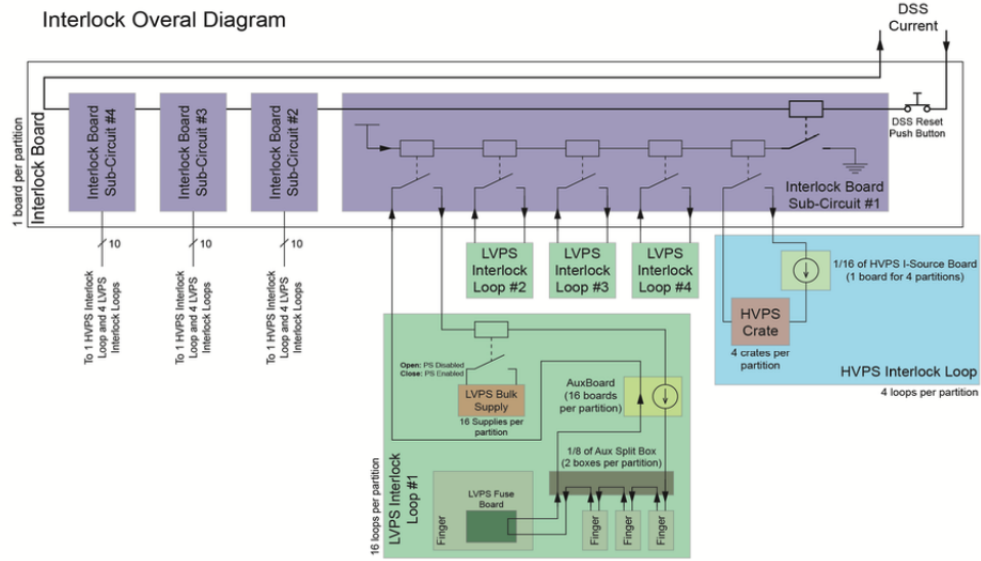


Figure 3.13: Diagram of the Interlock Loop of the TileCal.

3.4 finger Low-Voltage Power Supply Brick

3.4.1 Design History

In this section the design history of the finger Low-Voltage Power Supply (fLVPS) Brick will be covered in brief. This is motivated as many of the design constraints and considerations that were present in the development of the legacy Bricks are still present in their Phase-II Upgrade development, albeit to a more demanding degree in some cases. There have been numerous design iterations of the Bricks as alluded to by their versioning. The V6.5.4 and V7.5.0 will be looked at explicitly due to these versions having been installed and operated within the TileCal. The iterative nature of the fLVPS Brick design is motivated not only due to the success of previous designs and the inherent benefits of refining a well-understood system, but also due to the stringent design limitations imposed by their unique operating environment and location.

V6.5.4 Design Insights

The V6.5.4 Brick was the first version to be installed and operated within the TileCal in 2007. This Brick version is the progenitor for all of those that followed with certain design aspects and components of this version being present in the Phase-II Upgrade Brick design.

The first and most prominent design aspect that propagated to the Phase-II Upgrade Brick is that of its form factor. As previously mentioned in subsection 3.2.2, the fLVPS occupies a fixed volume within the TileCal finger which will not changed during the



Figure 3.14: Top view of a V6.5.4 fLVPS Brick [62].

upgrade. This extends further in that the mounting holes, of which there are 5, occupy the same position as well. This results in the new replacement cooling plates being identical to those currently within the TileCal. An interesting note is that although the current 256 TileCal cooling plates could in principle be reused this will not be done as the Phase-II fLVPS will be assembled prior to the upgrade commencing due to time restrictions. These aspects are important to consider as the effectiveness of the thermal coupling of the Bricks to the cooling plates plays an important role their operating temperature and therefore in their reliability and longevity.

The innovative method of thermally coupling the Bricks to the water-cooled cooling plates via custom Al_2O_3 ceramic spacers (henceforth referred to as ceramic posts) was necessitated due to the small form factor of the Bricks. This as their use allows for both sides of the Printed Circuit Board (PCB) to be populated with electronic components thereby effectively doubling the PCB size [62]. This design feature has been employed in all subsequent TileCal Bricks and the will be looked at in detail in subsection 3.4.2.

Another common observable feature between the V6.5.4 Brick and subsequent versions are a custom planar transformer that was developed "in-house" for the TileCal Brick. A deconstructed transformer can be seen in Figure 3.15. It has a nominal switching frequency of 300 kHz and multiple windings. It has one primary winding and four secondary windings. Three of the secondary windings power the Bricks active components whereas the fourth is the main secondary output that drives the load. The magnetic field strength where these power supplies reside is of order 200 Gauss. The outer shield of the fLVPS box provides some magnetic shielding but the transformers require additional shielding. The shield is made from nickel-plated steel and is rated to withstand 100 Gauss without affecting performance. The shield also serves a secondary feature in that it acts as a heat sink. There is thermally-conductive compound on the top and bottom of the core to the top and bottom of the shield.

The V6.5.4 provides a unique perspective in that it was the first time that the TileCal

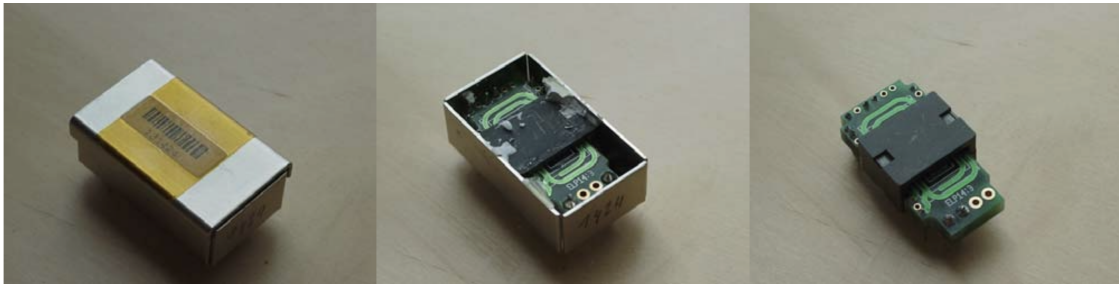


Figure 3.15: Images depicting the deconstruction of an fLVPS Brick transformer. Observe the black transformer core centrally located in the transformer.

on-detector electronics were powered by these custom made power supplies in the ATLAS environment produced by LHC collisions. Careful attention should be paid to the history of the V6.5.4 Bricks, lest it be repeated. This as the phase-II Upgrade Bricks will also be subject to similar "uncertainty" when installed and operated within the ATLAS High-Luminosity LHC environment. This "uncertainty" arises due to the fact that simulations were and are used to a great degree to predict the magnetic field and the radiation environment within the finger volume [63, 64].

Initially, the V6.5.4 Bricks operated satisfactorily; however, they started to display a propensity for trips as the luminosity of the LHC was gradually raised during commissioning. A trip is characterized as a spontaneous event wherein a Brick shuts off. This trip rate correlated with the beam luminosity, suggesting that the performance of the V6.5.4 Brick would continue to degrade, rendering it unsuitable for its intended use.

A plot of the observed trips versus luminosity during 7.5 months of operation in 2011 is shown in Figure 3.16. In these cases, an individual fLVPS trips, but was usually automatically restarted by the Detector Control System after a period of approximately 2 minutes, although sometimes the recovery required human intervention. These trips were inherently problematic as they resulted in the loss of data from the affected modules for several minutes.

In addition to the tripping as a function of luminosity, the V6.5.4 Bricks exhibited a relatively high failure rate during the first two years of operation amounting to approximately 6 Bricks per year. This behaviour will be elaborated upon in section 3.4.1.

V7.5.0 Design Insights

It was decided that an inevitable replacement for the V6.5.4 was required primarily motivated by the the spontaneous tripping as a function of luminosity. As such, a critical study was carried out to determine how the design might be improved. Further information such as experience gained during repair and technical support activities for the early running period of the bricks from 2007 to 2009 was available. These were used to formulate specifications and goals for the redesign project which would finally yield the V7.5.0 Brick.

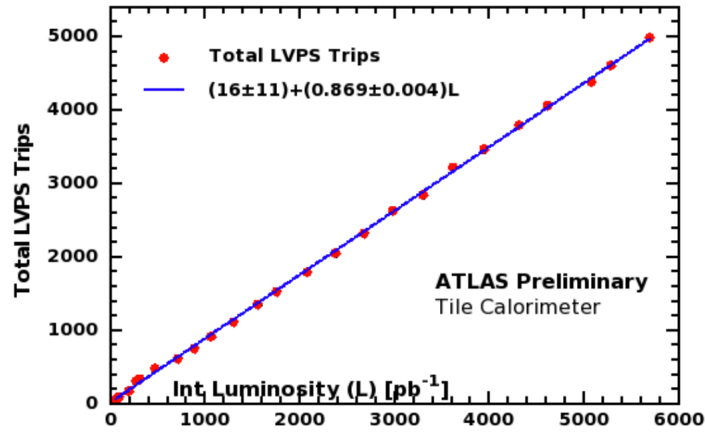


Figure 3.16: Number of finger Low-Voltage Power Supply (LVPS) trips observed versus delivered luminosity, Mar. 13 – Oct. 30, 2011 [65].

All of the design improvements incorporated into the V7.5.0 have been carried across to the Phase-II Upgrade iteration which necessitates a brief review with particular emphasis being placed on the Brick trips, thermal improvements and irradiation campaigns as these will provide insight into the methodology employed in chapter 4.

A performance study of the V6.5.4 Bricks uncovered that the source of the spontaneous tripping was in fact the inbuilt Over-Voltage Protection (OVP) and Over-Current Protection (OCP) circuits and more specifically the sensitivity of these circuits to electronic noise. These circuits, when operating normally, serve to protect a Brick in the case of an Over-voltage and/or Over-Current condition on their output by initiating a trip. It was observed the noise of the V6.5.4 Bricks was large, of order 0.9 V peak-to-peak (Pk-Pk) and that the magnitude of this noise was a function of the applied load. The output voltage noise of the V6.5.4 Brick can be seen in Figure 3.17 (a). The V6.5.4 Bricks exhibited a sensitivity to the load currents in the front-end electronics as the OVP and OCP circuits needed to process signal voltages superimposed with the noise.

The reduction of noise within the Brick was chosen as a primary design change to be made in order to address the spontaneous tripping. This required the identification and minimisation of primary current loops, introduction of interleaving ground planes, and the incorporation of differential techniques in the signal processing. In particular, the OVP and OCP circuits of the V7.5.0 Brick are fully differential up to the final comparator. These techniques resulted in a significant improvement in the noise performance of a factor of 5 at the highest load currents when measured single-ended and significantly more when measured with a differential probe. The significant improvement in noise performance of the V7 Brick is apparent in Figure 3.17 (b).

Five prototype fLVPS, using V7.5.0 Bricks, were installed in the TileCal in December 2010. During the following 8 months of collisions there was only a single trip of the new supplies observed in comparison to the approximately 15 trips per module, on average, for all others in the long barrel. The single trip was attributed to a Single Event Upset

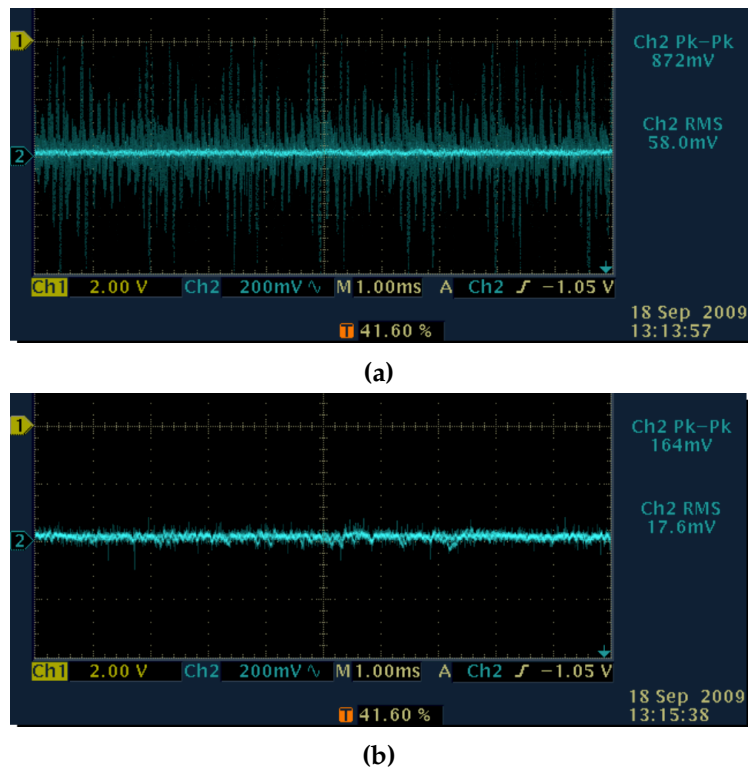


Figure 3.17: Output voltage noise of a V6.5.4 Brick (a) and V7 Brick (b) [65].

leading to the conclusion that the design changes had successfully addressed the problem of spontaneous tripping of the Bricks.

The V7.5.0 design also looked to address the observed reliability issues with the V6.5.4 Brick. Two components were identified as being primarily responsible for their poor reliability. This was possible as all repairs made to the Bricks during the 2009 – 2010 operational period were recorded. The two most frequent failures noted were that of the LT1681 controller chip and the IR2110S Field-Effect Transistor (FET) driver [66, 67]. The function of these critical components, which are also used in the Phase-II Upgrade Brick, will be described in subsection 3.4.3.

In benchtop studies, it was noted that the above mentioned parts became very hot during nominal operation. Although the Bricks are actively cooled within an fLVPS the V6.5.4 Bricks had no direct thermal coupling of these specific components to the cooling plate resulting in localised hot-spots. These components were moved to the bottom side of the V7.5.0 Bricks (between the cooling plate and the Brick PCB) which allowed coupling to the cold plate via a thermally conductive and electrically insulating gap-pad. The gap-pad was inserted between the components and the cooling plate when the V7.5.0 fLVPS were assembled. An illustration of this configuration is provided in Figure 3.19. The use of gap-pad is being continued in the Phase-II upgrade where it will be inserted between the LT1681 (schematic label U1), IR2110s (schematic label U2) and the cooling plate during the assembly of the fLVPS as in the V7.5.0 fLVPS assembly. The location of

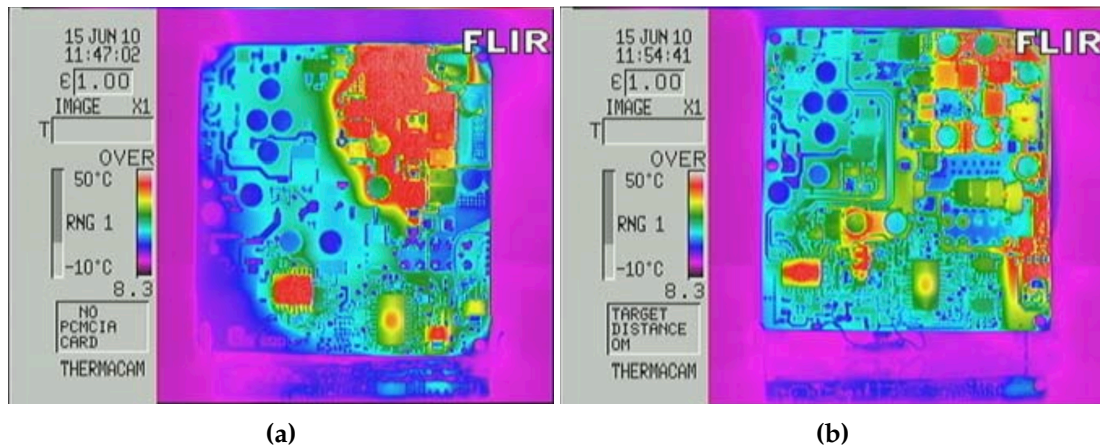


Figure 3.18: Thermal image of +5MB V6 Brick (a) and +5MB V7 Brick (b) under a 13 A load [65].

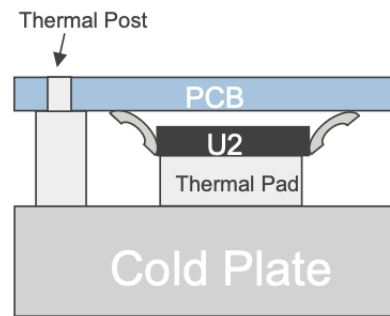


Figure 3.19: Illustration of the use of a thermal gap pad to facilitate improved cooling of the IR2110s (U2) Field-Effect Transistor (FET) driver. The LT1681 (U1) controller chip has an indetical configuration.

these active components will become more apparent in subsection 3.4.2.

To further improve the thermal performance of the V7.5.0 Brick the material of the ceramic posts mentioned in section 3.4.1 was changed from Aluminum Oxide (Al_2O_3) to Aluminum Nitride (AlN) which resulted in approximately nine times better thermal coupling to the cooling plate. The overall improvement to the V7.5.0 Bricks thermal performance can be seen in Figure 3.18. The implications of this change of ceramic post material for the Phase-II Upgrade will become readily apparent in section 4.1.

While the V6.5.4 bricks had undergone radiation hardness certification in 2004 as per the current ATLAS policy on radiation tolerant electronics prior to installation within the TileCal it was decided that V7.5.0 should be re-tested even though the new design has prioritised the use of the V6.5.4 active components [71, 72].

These irradiation campaigns began in December, 2010, and continued through May, 2011. The program included dedicated campaigns with 1 MeV equivalent neutrons, 188 MeV protons, and 1 MeV gammas. The performance of certain critical active components,

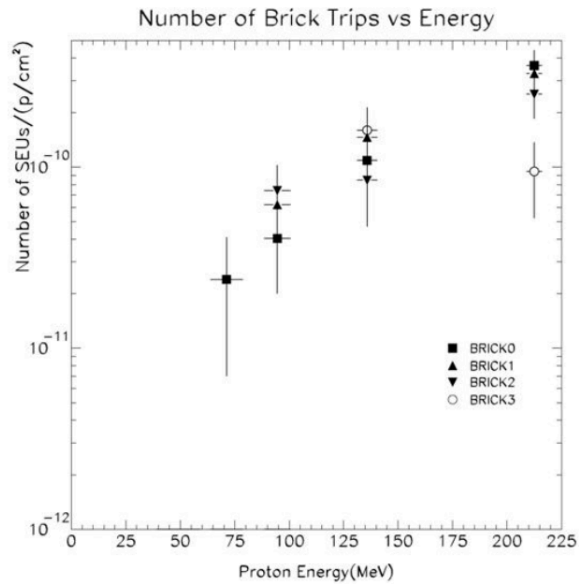


Figure 3.20: Energy dependence of trips of the LT1681 controller chip [65].

namely the LT1681 controller chip, the IR2110 FET driver, and the HPCL-7800 opto-isolators were of particular interest. It was found that these components performed sufficiently during both the TID and NIEL irradiation campaigns with only minor performance degradation having been observed [73].

However, the LT1681 showed a sensitivity to Single Event Upsets (SEU) which was traced to a flip-flop in the soft-start circuit inside the chip. This behaviour was found to be interesting as the component had been previously tested for SEU susceptibility, during the V6.5.4 Brick development, with no such trips having been observed. Therefore, an energy-scan was undertaken the results of which are presented in Figure 3.20. The trip rates can be seen to have a dependence on the protons incident energy.

A design change was subsequently implemented to the soft-start circuitry which nullified this behaviour in the V7.5.0 Bricks. This design change has been propagated to all of the successive Brick versions.

It should be noted that the HCPL7800 opto-isolator and IR2110s FET driver exhibited

Thermal Posts		
Brick version	Description	Thermal Conductivity (W/m °K)
V6.5.4	Aluminium Oxide (94%)	18 [68]
V7.5.0	Aluminium Nitride	140-180 [69]
Gap Pad		
V6.5.4	Not used	-
V7.5.0	Berquist GAP PAD TGP 2700	2.7 [70]

Table 3.4: Thermal conductivity of the on-detector V6.5.4 and V7.5.0 Bricks thermal posts and gap pad where applicable.

a tendency to fail at very high dose rates. The components were deemed to pass the radiation hardness certification due to the high safety factor imposed (SF_{TID}).

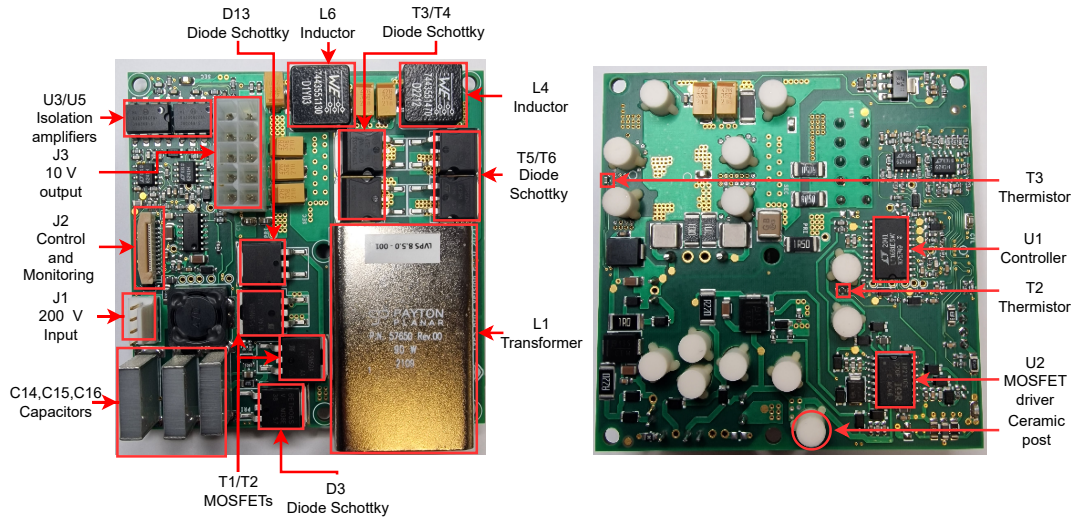


Figure 3.21: Top (Left) and bottom (Right) view of a V8.5.0 Brick produced in South Africa.

3.4.2 Phase-II Upgrade Brick Physical Description

The Bricks Printed Circuit Board (PCB) consists of 6 layers with dimensions of 80.26 mm by 80.26 mm. Both the PCB cores and pre-pregs are made out of halogen-free FR4 material as defined by IEC 61249-2-21 [74]. This is a design mandate imposed by CERN as halogen containing PCBs produce more corrosive and toxic smoke when burnt as opposed to non-halogen equivalents.

As can be seen in Figure 3.21, the PCB has multiple holes that run through its entire stack-up. There are 5 mounting holes for attachment to the cooling plate inside the fLVPS as well as 14 holes that allow for the thermal posts to attach directly to the the components mounted on the top side of the Brick. The thermal posts are each glued to the bottom side of the Brick using epoxy (Araldite AV 4076-1). A supplementary parametric solid of the Brick stack-up is provided in Figure C.1,

The thermal posts are ceramic cylinders made from either Aluminium Nitride or Aluminium Oxide depending on the origin of the Bricks production being in the United States of America or South Africa, respectively. The posts are used to directly transfer heat from Brick components to the fLVPS cooling plate and are $7\text{ mm} \pm 0.1$ in height and $6\text{ mm} \pm 0.1$ in diameter. Adherence to these dimensions is of the utmost importance as if the posts are too long or short thermal contact of the offending post will be non-existent or the planarity of Brick to the cooling plate will be affected. If the posts are too thin their capacity for heat transfer is diminished whereas if they are too wide they will not fit into the holes in the PCB. These dimensions are provided in Figure 3.22 (a). The cylinders come in two additional types, namely metallized and non-metallized. The metallized cylinders, of which there are 8 per Brick, have one Silver-Palladium metallized face which will be in contact (physically soldered during reflow manufacturing process) with the

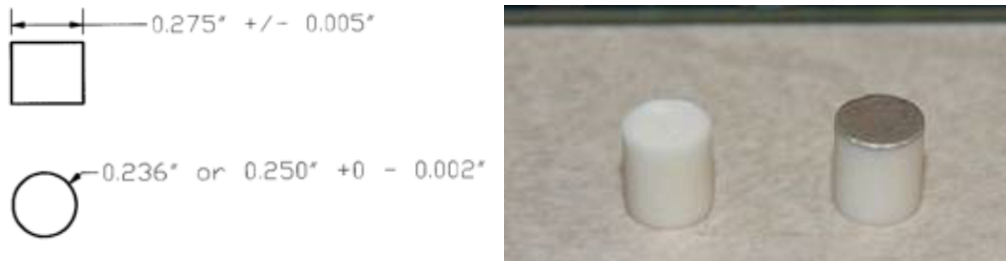


Figure 3.22: Dimensions of a thermal post (a). Image of a non-metallized (left) and metallized (right) aluminium oxide thermal post (b).

pad of the switches and diodes located on the top of the Brick PCB. The components to which these metallized posts are pictured in Figure 3.21 where they are labelled T1, T2, T3, T4, T5, T6, D3, D13 MOSFETs and diodes. The remaining 6 non-metallized posts are responsible for transferring heat from the components that cannot be directly soldered to the thermal posts. These are the L1 transformer (4 posts) and L4/L6 inductors (1 post each). These components require a non-silicone based thermal grease (TG-N909) be placed between the bottom of their case and the top of the thermal posts to facilitate the conduction of heat [75]. An Image of a non-metallized and metallized aluminium oxide thermal post can be seen in Figure 3.22 (b).

The U1 controller and U2 MOSFET driver can be seen in Figure 3.21 (Right). As previously mentioned, a gap-pad is located between these integrated circuits and the fLVPS cooling plate to allow for direct thermal coupling. Observe the close proximity of U1 and U2 to the ceramic posts responsible for cooling the T1/T2 MOSFETs and D3/D13 schottky diodes. U1 is also relatively close to the T2 thermistor which is responsible for initiating a trip of the Brick if the over-temperature protection circuitry trip point is met. The protection circuitry will be covered in subsection 3.4.3. The second thermistor (T3) is located on the periphery of the PCB in between the T5 and T6 schottky diode thermal posts. This thermistor is only used for monitoring purposes.

All of the Brick connectors are located on its top-side (pointing away from the cooling plate when installed within an fLVPS). A 4-pin connector (J1) is used to receive the 200 V DC from the fuse board, with two pins for + 200 V and two return pins. There is also a 10-pin output connector (J3) to deliver the 10 V DC output of the Brick to the Harting connector on the fLVPS. This connector makes use of 5 pins for +10 V DC and 5 return pins. There is also a small 20-pin connector (J2), which connects the Brick to the Embedded Local Monitoring Board (ELMB) Motherboard with a ribbon cable. This connector is used to receive the control signals from the ELMB-MB, and send the monitoring signals in Differential Analog format to ELMB-MB and then on to the ELMB2 as previously depicted in Figure 3.9.

Description (Schematic ID)	Function	Part number
4-pin wire-to-board header (J1)	200 V DC input.	22-29-2041 [76]
20-pin FFC/FPC connector (J2)	Communication with ELMB2.	52559-2052 [77]
10-pin Mini-fit Jr. header (J3)	10 V DC output.	39-28-1103 [78]

Table 3.5: Brick connectors description and associated part numbers.

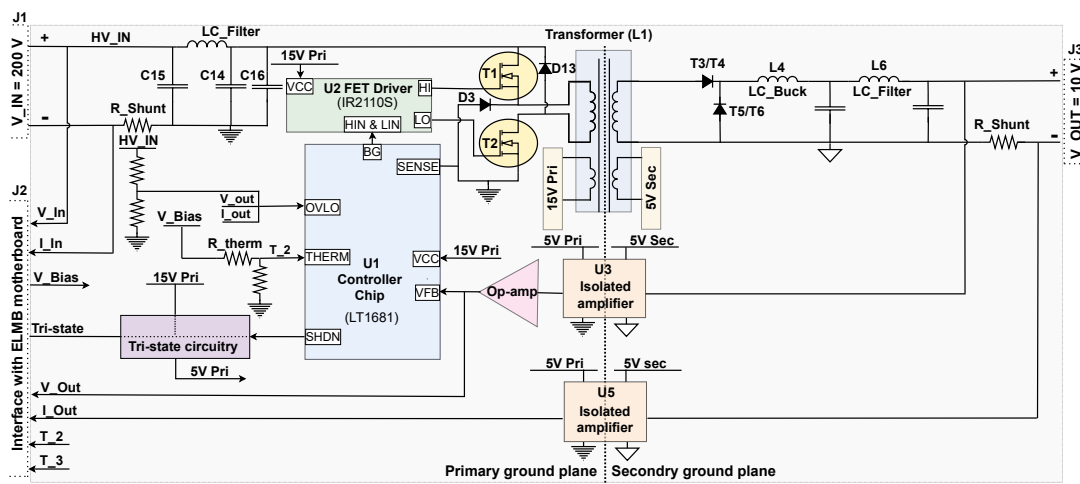


Figure 3.23: Functional block diagram of an fLVPS Brick.

3.4.3 Phase-II Upgrade Brick Functional Overview

The circuit analysis that is to follow is an adaptation of a paper by S. Patil and others with the notation being altered to reflect that of the Brick [79].

A TileCal Brick is an isolated switch-mode power supply with a two switch forward converter topology. A functional circuit diagram, derived from the V8.6.1 fLVPS schematics provided in Appendix E, can be seen in Figure 3.23. The fully custom design makes use of only Commercial Off-The-Shelf (COTS) electronic components as motivated in subsection 3.1.1. The circuitry of the Brick can be partitioned into five distinct sub-circuits according to their functionality. These are the regulation, power, control, in-built protection and filtering sub-circuits.

The Bricks design is centred around the Linear Technology LT1681 dual transistor synchronous forward controller chip (U1) as illustrated in Figure 3.23. The LT1681 is involved in the output voltage regulation, in-built protection and control of the Brick. The controller chip employs the Pulse Width Modulation (PWM) control method to regulate the output voltage and operates at a fundamental (switching) frequency of $f_{switching} = 300 \text{ kHz}$ [66]. That is, the output voltage of the Brick is controlled by a feedback loop that varies the ratio of the closed- and open-times of the high-side (T1) and low-side (T2) MOSFETs. This ratio is referred to as the duty cycle (D). The duty cycle of the Brick can vary from a few percent to a maximum of 45%. Generic PWM square waveforms illustrating 0%, 25% and 50% duty cycles can be seen in Figure 3.24.

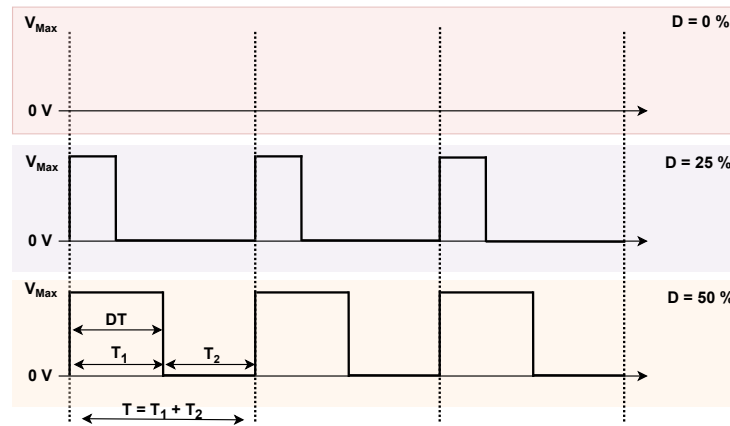


Figure 3.24: Generic PWM square waveforms illustrating duty cycles (D) of 0 %, 25 % and 50 % for a constant switching period (T), time at high-state (T_1) and time at low-state (T_2). Note that the duty cycles of 0 % and 50 % are used for illustrative purposes only and cannot be operated at by the Brick.

The Bricks duty cycle is regulated by the LT1681 using two inputs. The first input is VFB, the “slow” feedback path, which monitors the Bricks output voltage with a bandwidth of 1 KHz. The second “fast” feedback path monitors the current through the low-side transistor (T_2) on the primary side via the SENSE pin. Both feedback paths are designed so as to ensure the continuous-mode operation of the power converter¹. The LT1681 provides the output clock via the BG pin to the IR2110 Field-Effect Transistor (FET) Driver (U2) logic input pins HIN and LIN for the high-side (HI) and low-side (LO) gate driver output pins, respectively. This is a transistor driver that has sufficient current and voltage drive to drive the high-side (T_1) and low-side power (T_2) FETs that perform the switching on the primary side of the Brick.

At this point it is beneficial to further simplify Figure 3.23 to three equivalent circuits, each of which representing the power electronics state during a period of the Bricks operation. An equivalent circuit is a theoretical circuit that retains all of the electrical characteristics of the physical circuit while being simpler to interpret. It should be noted that the L1 transformer is represented by an ideal transformer and an inductor whose inductance L_m is equal to that of the primary winding of L1.

The design uses synchronous switching. That is, both the high-side (T_1) and low-side (T_2) transistors turn on and conduct for the duration that the output clock is in the high state, and both are in the off state when the clock is low. This creates pulsed DC voltage of variable duration. The equivalent circuit for when T_1/T_2 are turned on (Clock in high-state and voltage applied to V_{HI} and V_{LO} gates by the U2 FET driver) is shown in Figure 3.25 a. As a result the input voltage V_{in} is applied across the primary winding of the transformer (L1) which causes the magnetising current I_m to increase. That is, the

¹Continuous mode operation is characterized by the current through the choke (L4) being continuous (no zero value) within a single switching period (T).

magnetic flux is built up in the transformer core. On the secondary side, T3 and T4 are forward biased (current can flow) and the secondary current is equal to the inductor current i_{L4} . During this interval, the increase in i_{L_m} and i_{L4} are given by $(\Delta i_{L_m})_{On}$ and $(\Delta i_{L4})_{On}$ in Equation 3.9 and Equation 3.10, respectively:

$$(\Delta i_{L_m})_{on} = \frac{V_I DT}{L_m} \quad (3.9)$$

$$(\Delta i_{L4})_{on} = (nV_{In} - V_{Out}) \frac{DT}{L_4} \quad (3.10)$$

Where D is the duty cycle of T1/T2, T is the switching period, and $n = \frac{N_{Pri}}{N_{Sec}}$ is the primary-to-secondary winding turn ratio of the transformer (L1). From Figure 3.25(a), the following current and voltage equations can be written:

$$i_{In} = i_{T1} = i_{T2} = n(i_{L4}) + i_{L_m} \quad (3.11)$$

$$i_{D3} = i_{D13} = 0 \quad (3.12)$$

$$V_{T1} = V_{T2} = 0 \quad (3.13)$$

$$V_{D3} = V_{D13} = V_{In} \quad (3.14)$$

When T1/T2 are turned off and D3/D13 are forward biased, the equivalent circuit is shown in Figure 3.25(b). The primary voltage becomes $-V_{In}$ due to the conduction of D3 and D13. This causes i_{L_m} to decrease thereby demagnetising the transformer core. On the secondary side, the reversed secondary voltage ceases the conduction of T3/T4, while T5/T6 are forward biased to allow the continuous flow of i_{L4} . During this interval, both i_{L_m} and i_{L4} are falling. The decrease in i_{L_m} and i_{L4} are expressed by $(\Delta i_{L_m})_{Off}$ and $(\Delta i_{L4})_{Off}$ in Equation 3.15 and Equation 3.16, respectively:

$$(\Delta i_{L_m})_{Off} = -V_{In} \frac{\Delta t}{L_m} \quad (3.15)$$

$$(\Delta i_{L4})_{Off} = -V_{Out} \frac{\Delta t}{L_4} \quad (3.16)$$

Where $\Delta t = DT$ is a time spent resetting the magnetic flux. From Figure 3.25(b), the following current and voltage equations are obtained:

$$i_{In} = -i_{L_m} \quad (3.17)$$

$$i_{D3} = i_{D13} = i_{L_m} \quad (3.18)$$

$$V_{T1} = V_{T2} = V_{In} \quad (3.19)$$

$$V_{D3} = V_{D13} = 0 \quad \text{assuming perfect diode} \quad (3.20)$$

When both T1/T2 and D3/D13 are not conducting, the equivalent circuit is shown in Figure 3.25(c). This state occurs when magnetic flux in the transformer core has been completely reset. That is $i_{L_m} = 0$. The primary voltage now is zero as is the secondary voltage. On the secondary side, i_{L4} continues to fall, but remains positive. Since both T3/T4 and T5/T6 are conducting, the current i_{L4} splits between the two parallel paths. The decrease in i_{L4} is given by $(\Delta i_{L4})_{Off1}$ in Equation 3.21:

$$(\Delta i_{L4})_{Off1} = -V_{Out} \frac{\Delta t_1}{L_4} \quad (3.21)$$

Where $\Delta t_1 = (1 - D)T - \Delta t$. From Figure 3.25(c), the following current and voltage equations are obtained:

$$i_{In} = 0 \quad (3.22)$$

$$i_{D3} = i_{D13} = 0 \quad (3.23)$$

$$V_{T1} = V_{T2} = \frac{V_{In}}{2} \quad (3.24)$$

$$V_{D3} = V_{D13} = \frac{V_{In}}{2} \quad (3.25)$$

The steady state condition exists when the net change in i_{L4} over one switching period is zero, that is:

$$(\Delta i_{L4})_{On} + \Delta i_{L4} + (\Delta i_{L4})_{Off1} = 0 \quad (3.26)$$

Substituting Equation 3.10, Equation 3.16, and Equation 3.21 into Equation 3.26 yields:

$$V_{Out} = \frac{DV_{In}}{n} \quad (3.27)$$

Therefore, we have shown that given a stable input voltage (from the off-detector bulk power supplies) the output voltage of the Brick is a dependant only on the duty cycle of the T1/T2 MOSFETs and the turn-ratio (n) of the L1 Transformer. As the transformers turn-ratio is fixed we have that the Bricks output voltage is solely controlled by the duty cycle of the switching MOSFETs.

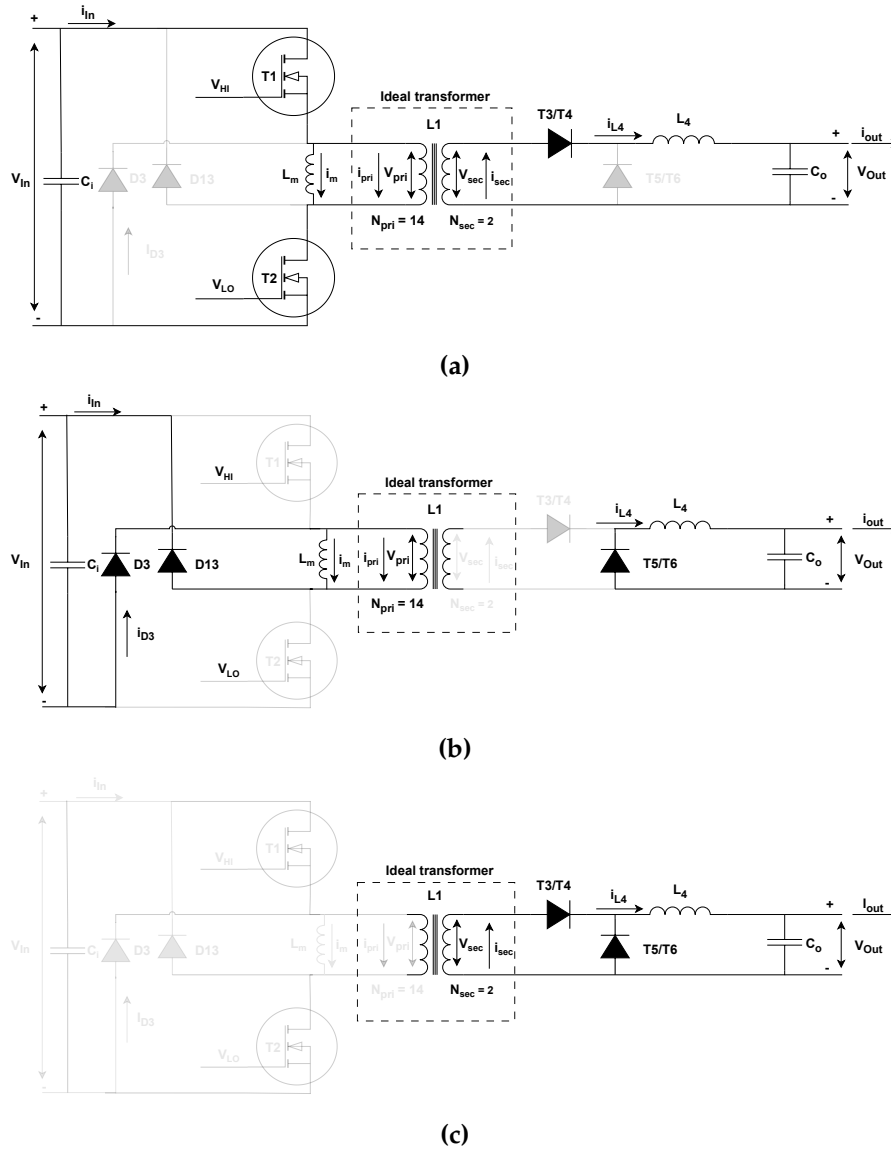


Figure 3.25: Equivalent circuits of the Bricks power circuitry for duty cycle (D) and period (T) during intervals $0 < t < DT$ (a), $DT < t < T - DT$ (b) and Components that are conducting current are indicated by black circuit symbols.

To illustrate this relationship we can calculate the average duty cycle (D) for a Brick operating at a stable nominal load given $V_o = 10 \text{ V DC}$ (output voltage to front-end electronics point-of-load regulators), $V_i = 200 \text{ V DC}$ (input from off-detector bulk power supplies), $N_{pri} = 14$, and $N_{sec} = 2$:

$$D = \frac{V_o}{V_i} \frac{N_{pri}}{N_{sec}} = 35\% \quad (3.28)$$

This value falls midway between the upper and lower bounds for the duty cycle in the V8.6.1 Brick performance specifications provided in Table C.1.

From the preceding analysis, the Bricks voltage and current waveforms can be drawn as shown in Figure 3.26.

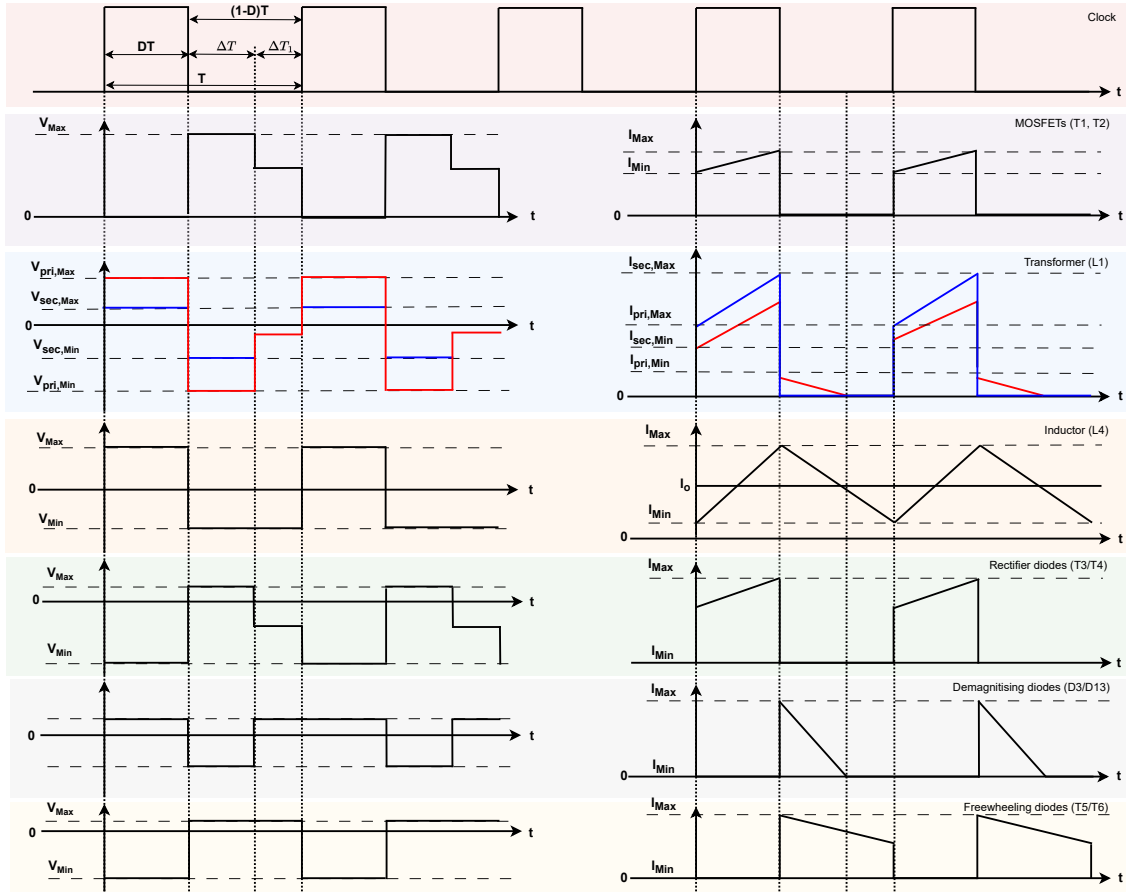


Figure 3.26: Idealized voltage (left column) and current (right column) waveforms for a Brick operating nominally. These waveforms assume a stable output voltage (Constant duty cycle).

Control of the Phase-II Upgrade fLVPS Brick is limited to switching the device on and off as opposed to the V7.5.0 Bricks that are currently installed within the TileCal which also allow for voltage trimming of their output. This functionality is no longer required due to the introduction of a third stage to low-voltage power distribution system, as previously mentioned. That is, the point-of-load regulators that undertake the final regulation of the power on the front-end electronics remove the necessity for fine tuning the output of the Bricks.

The on/off control of the Brick is facilitated by the newly introduced Tri-state functionality. The tri-state system consists of three distinct states as introduced in section 3.3. Each Brick receives a tri-state signal from the off-detector Auxiliary Board via theELMB mother board which is then interpreted by its start circuitry. A Brick can only be in a single state at a one moment in time. These Start and Disable states are requested by the

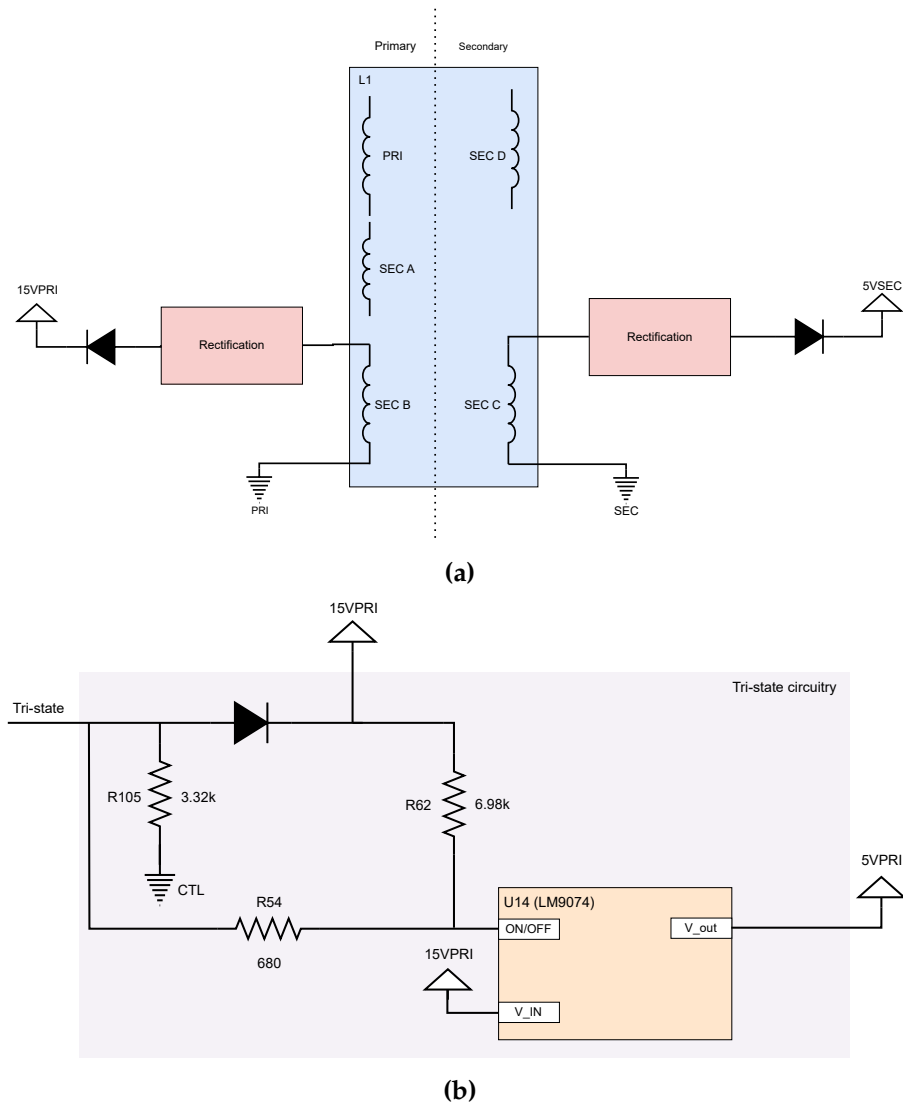


Figure 3.27: Functional block diagrams of the V8.6.1 Brick transformer (a) and tri-state circuitry (b).

DCS and applied to the respective Bricks by the AuxBoards. Each Auxboard can provide up to 32 independent tri-state signals as required for four Long-Barrel fLVPS which each contain 8 Bricks. Four Extended-Barrel fLVPS only require 24 tri-state lines but for simplicity of production and interchangeability all AuxBoards are identical regardless of which barrel region fLVPSs they are tasked with controlling. Due to having a limited number of wires in the tri-state cables, all 32 tri-State signals share two common return wires only. This requires that the Bricks are sent a Start signal sequentially due to the high current experienced on the tri-State lines during the Start state.

To understand the Bricks tri-state circuitry one needs to pay attention to Bricks active components which are powered by the Brick itself. The active components are responsible for control of the switching of Bricks power circuitry amongst other functions. The

Brick powers its active components (5 V DC and 15 V DC) both on its primary and secondary sides using secondary windings within the L1 transformer except for 5 V DC on the primary side which is provided by the U14 voltage regulator. The Bricks transformer with secondary windings and its tri-state circuitry are illustrated in Figure 3.27.

A Start signal is imposed by the AuxBoard on the tri-state line to power on a Brick. This 15-17 VDC signal lasts approximately 1 second and initially powers the primary side control circuitry of a Brick. After starting successfully, the Brick then powers both its primary and secondary sides. This necessitates that the input 200 V DC provided by the off-detector bulk power supplies be supplied to the Brick prior to it receiving the Start signal. The 15-17 VDC signal is routed to the 15VPRI power rail of the Brick (through a forward biased diode) where it is distributed to the appropriate active components on the primary side as well as U14 Figure 3.27.

Once a Brick has been started it automatically enters the Run state without any intervention of the AuxBoard. In this state the circuitry of a Brick imposes a voltage of 6.0 ± 0.2 V on its tri-State line, when it is in high impedance mode, which keeps the Brick enabled. However, if the brick is off, the high impedance state does not turn it on, as there is no voltage on the brick. Therefore, once a brick is turned off (for example due to a trip) only a Start signal can turn it back on.

This voltage is imposed as the 15VPRI power rail is now receiving power from the SECB secondary winding of the L1 transformer which is provided to the U14 ON/OFF pin and the tri-state line via two voltage dividers. The voltage divider circuits are illustrated in Figure 3.27 (b).

Applying the voltage divider equation for the tri-state line in the RUN state we have that:

$$V_{TRI-STATE} = 15VPRI \left(\frac{R105}{R105 + R54 + R62} \right) = 15 \left(\frac{3320}{3320 + 680 + 6980} \right) \approx 4.5 \text{ V} \quad (3.29)$$

This voltage signal is monitored by the Auxilliary board which is interpreted by the DCS as the Brick being on.

Similarly, for the U14 ON/OFF pin we have that:

$$V_{ON-OFF} = 15VPRI \left(\frac{R105 + R54}{R105 + R54 + R62} \right) \approx 5.5 \text{ V} \quad (3.30)$$

A voltage of 5.5 V is within the U14 ON/OFF pin high state bounds which enables its output voltage of 5 V that powers the feedback circuitry of the Brick on its primary side.

The Disable signal is used to switch off a Brick and requires that the voltage on the tri-state line falls below 2 V DC which is the upper bound of the U14 ON/OFF pin. When this occurs the U14 output is disabled and subsequently the feedback loop of the Brick.

Signal name	Line voltage (V)	Line current (mA)	Duration (s)
Start	15.0-17.0	150	1
Run	4.5 ± 0.2	-	-
Disable	< 2.0	0	-

Table 3.6: Phase-II Upgrade fLVPS Brick tri-state voltage signals.

This is achieved by the AuxBoard shorting the tri-state line to ground which also disables the control circuitry of the Bricks via the 15VPRI power rail.

The tri-state signals voltage levels, and duration where applicable are provided in Table 3.6 and are illustrated in Figure 3.28.

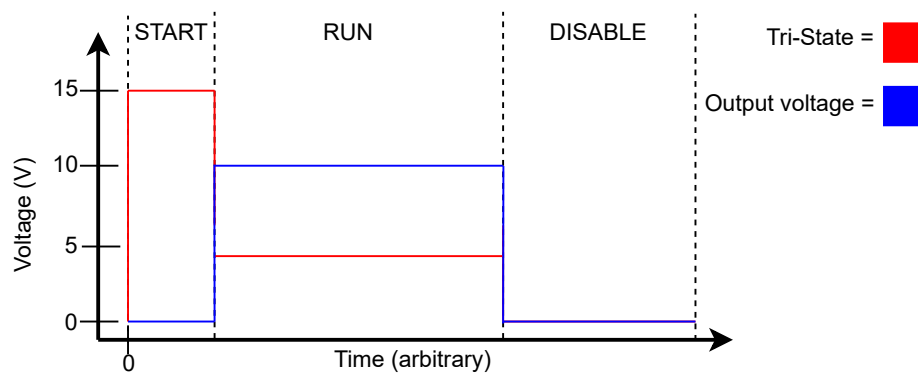


Figure 3.28: Idealized plot of a V8.6.1 Bricks Tri-state line and output voltage for the START, RUN and DISABLE states.

The Brick has three types on inbuilt automatic protection that initiate a trip if any of their thresholds are met. These are: Over-Voltage Protection (OVP), Over-Current Protection (OCP) and Over-Temperature Protection (OTP). The OVP circuitry the 10 VDC output for over-voltage conditions. The protection circuitry functions not only to protect the Bricks in the event of malfunction but also the front-end electronics. The V8.6.1 Brick protection circuitry trip points are provided in Table 3.7.

Description	Value
Over-Voltage Protection	11.75 V
Over-Current Protection	6.5 A
Over-Temperature protection	70°C

Table 3.7: V8.6.1 Brick protection circuitry trip points. It is important to note that there is a variance in the trips points of certain Brick versions. The specific trip-points of previous Brick versions will be emphasized and provided where necessary.

Chapter 4

Development of the Phase-II Upgrade finger Low-Voltage Power Supply Brick

In this chapter the development of the Phase-II Upgrade finger Low-voltage Power Supply Brick (fLVPS) will be presented in chronological order. The motivation, methodology, and apparatus utilised will be furnished starting with the Bricks thermal performance and subsequent optimisation after which we will continue to the Radiation Hardness Qualification of the active electronic component proposed as a result of the Thermal Optimisation Studies. Finally, the topic of reliability in electronics will be introduced culminating with the Quality Assurance testing of the fLVPS Brick.

The aim of this chapter is to provide the reader with the much needed context and all necessary information directly related to the studies presented in chapter 5, chapter 6 and chapter 7.

4.1 Phase-II Upgrade Brick Thermal Performance and Optimisation

4.1.1 Motivation

In 2020 the V8.1.0 Brick was the latest iteration which had been produced at both the University of the Witwatersrand (Wits) and the University of Texas at Arlington (UTA). The Bricks produced were identical in design with the caveat that the Bricks produced by Wits and UTA made use of aluminium-Nitride and aluminium Oxide thermal posts, respectively. Thermal considerations of the Brick, including the thermal posts, were introduced in section 3.4.1 and subsection 3.4.2. At this time the difference was motivated due to the cost and long lead-time time associated with importing the aluminium nitride posts into South Africa. To overcome these problems a local manufacturer, CERAdvance, was found [80]. This sole manufacturer in South Africa has the capability to only produce aluminium oxide posts and not the aluminium nitride variant.

The impact on thermal performance of the Bricks due to this design variation was not quantitatively understood. It was assumed that the Bricks would operate at a higher temperature as a consequence of the lower thermal conductivity of the oxide posts (an order of magnitude lower than that of the nitride posts). The thermal figures of merit, including the thermal conductivity of the oxide and nitride posts were provided in Table 3.4. At the time this was the extent of our knowledge. Of course, similar studies had been conducted many years prior as was shown in section 3.4.1. Due to the substantial changes in the Brick design between the two versions (V7.5.0 and V8.1.0) these studies could not be extrapolated to the new Phase-II Upgrade Brick but did however provide insight into differential thermal performance of the two post types as well as areas of the Brick which should be subject to heightened scrutiny.

It was decided that a study should be conducted in order to gain a better understanding of the Phase-II Upgrade Bricks thermal performance when using aluminium oxide thermal posts.

The thermal performance and optimisation study had the following aims:

- Investigate the V8.1.0 and V8.4.2 Bricks thermal performance.
- Determine if the aluminium oxide thermal posts allow for adequate cooling of the Brick under nominal load.
- Identify any hot spots on the Brick if they existed.

4.1.2 Devices Under Test

The thermal performance and optimisation studies necessitated the use of multiple sub-variants of the Phase-II Upgrade Bricks each of which needing to be produced in a small-batch well in advance. The design variation and commonalities between these Devices Under Test (DUTs) are illustrated in Figure 4.1.

The first distinction made between the DUTs is whether or not they include a variable. For the purpose of these studies a variable is defined as a macroscopic difference in the composition of a DUT that is anticipated to impact its thermal performance. Variable and Baseline DUTs include and exclude variables, respectively. The selection of variables was based on experience gained from the review of previous thermal studies, as presented in section 3.4.1, coupled with an understanding of physical and functional characteristics of the Brick as presented in subsection 3.4.2 and subsection 3.4.3.

The Baseline DUT was a single V8.1.0 Phase-II Upgrade Brick, the schematics of which are provided in Figure E.1 and Figure E.2, that served as control for the subsequent experimentation. This Brick version was used as the Baseline as it was the latest iteration during the formative stages of the study.

The primary electronic components of DUTs that are of interest for this thermal performance study were the T1 and T2 MOSFETs, as well as the L4 inductor. These function

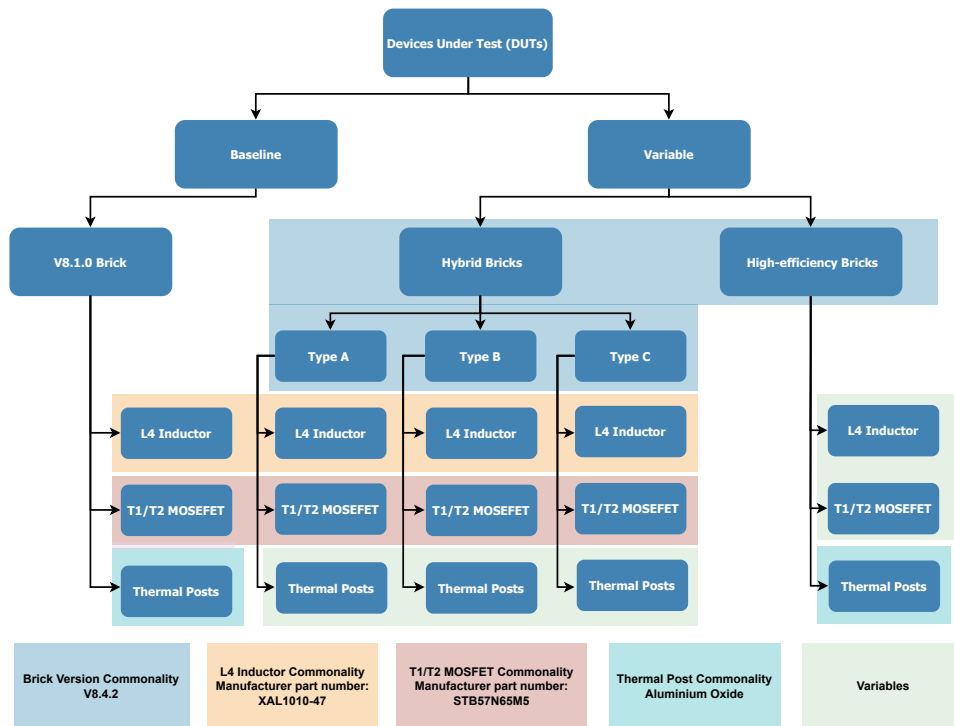


Figure 4.1: Thermal performance and optimisation studies Devices Under Test, their commonalities and differences.

of these components was covered in detail in subsection 3.4.3. Note that these components (part numbers) are different to those used by the V8.5.0 Brick pictured in Figure 3.21 in the Brick iterations discussed in this study. The part numbers of these components are provided in Table 4.1. Particular emphasis was placed on these components as they are key sources of conduction and switching power losses and thus heat generation. The commonality of these components is indicated across the Baseline and Variable DUTs in Figure 4.1. These components are listed in Table 4.1

Schematic ID	Description	Part number
T1,T2	Power MOSFET	STB57N65M5 [81]
L1	Custom transformer	57650
L4	Power inductor	XAL1010 [82]

Table 4.1: Baseline Brick electronic components of interest.

The Variable DUTs are subdivided into two sub-categories namely Hybrid Bricks and High-Efficiency Bricks each of which specifically manufactured to investigate different thermal performance phenomena based on the variable applied. Both of these sub-categories are based on V8.4.2 Bricks, the schematics of which are provided in Figure E.3 and Figure E.4. The key design change between the standard V8.1.0 and V8.4.2 Bricks was the introduction of the tri-state functionality which required no significant changes

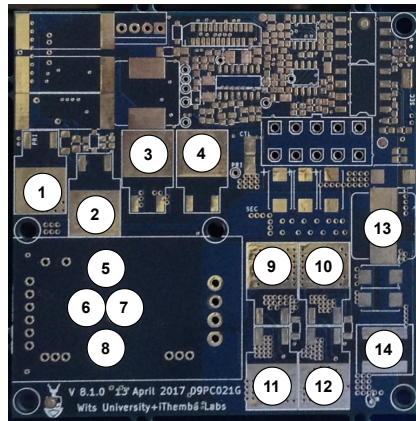


Figure 4.2: Hybrid Brick thermal post location Identification Numbers (IDs). Note that the posts physical location on the Printed Circuit Board (PCB) is identical for all Phase-II Upgrade Bricks.

to the PCB design or components, and most importantly has no impact on the thermal performance of the Bricks. As such, these two standard Brick versions can be considered identical for the purpose of these studies.

The Variable DUTs are sub-divided into Hybrid and High-efficiency Bricks. These two DUT types approach thermal optimisation and performance of the South African Phase-II Upgrade Bricks in entirely different ways.

The Hybrid DUTs, so named due to the hybrid composition of thermal posts, work on the base assumption that the heat produced by the Bricks during nominal operation is not to be addressed at the source (i-e component level) but rather that the heat needs to be efficiently sunk from the Brick. This approach has That is, all electronic components including the L4 inductor and T1/T2 MOSFETs are identical to those on the Baseline Brick with the caveat of the aforementioned tri-state start circuitry. There are several benefits to this approach that will be discussed in the subsequent paragraph. To this end, three Hybrid Brick variants were produced (A, B and C) with the variable between each variant being the thermal posts. Each Hybrid Brick variant employed a different distribution, in terms of number and location, of aluminium oxide and nitride thermal posts as indicated in Table 4.2. An accompanying figure, Figure 4.2, is provided that indicates the post IDs (locations).

A total of eight Hybrid Bricks were produced in a single panel. This number was not arbitrary as it was necessitated by the PCB core and pre-preg size. The Brick variants were not produced in equal numbers as greater statistics of the B and C type Bricks were desired as these variants were anticipated to yield the most favourable results. A single A variant (A1), four B variants (B1, B2, B3, B4) and three C variants (C1, C2, C3) were produced.

The locations and post type used (either nitride or oxide) by the Hybrid Brick variants were selected based on the known thermal properties of the material, as provided

Variant	Post Material	Post Type	Post Number	Post IDs
A	Al_2O_3	Non-metalized	5	5,6,7,8,13
	Al_2O_3	Metalized	4	9,10,11,12
	AlN	Non-metalized	1	14
	AlN	Metalized	4	1,2,3,4
B	Al_2O_3	Non-metalized	5	5,6,7,8,13
	Al_2O_3	Metalized	6	1,4,9,10,11,12
	AlN	Non-metalized	1	14
	AlN	Metalized	2	2,3
C	Al_2O_3	Non-metalized	3	5,8,13
	Al_2O_3	Metalized	6	1,4,9,10,11,12
	AlN	Non-metalized	3	6,7,14
	AlN	Metalized	2	2,3

Table 4.2: V8.4.2 Hybrid Brick variants, their thermal post composition and distribution.

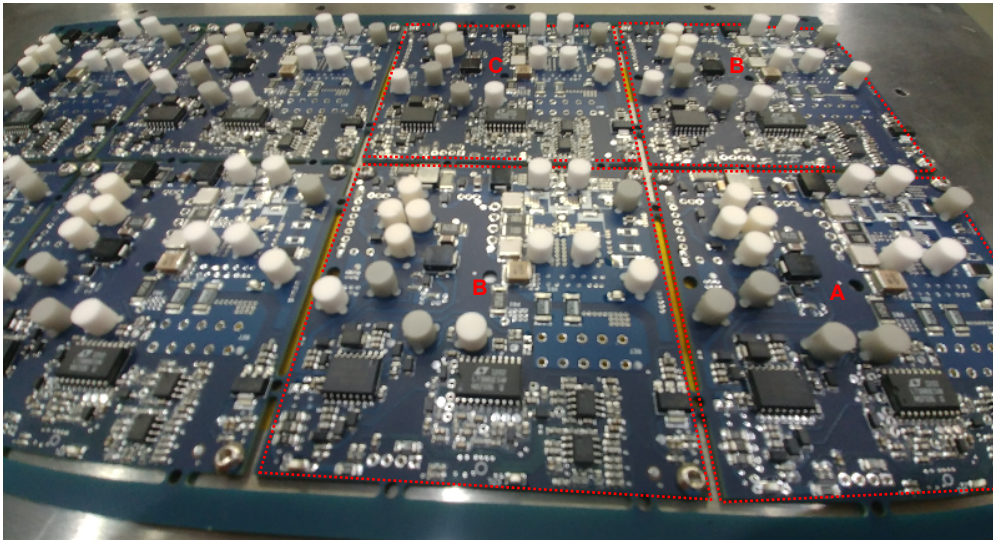


Figure 4.3: Image of a 8-up V8.4.2 Hybrid Brick panel mid-way through population. A, B and C type Hybrid Bricks are labelled. The different aluminium nitride (grey) and oxide (white) thermal post distributions of the Hybrid Brick types can be observed.

in Table 3.4, with anticipated hot-spots receiving the more thermally conductive nitride posts. Different variations were employed as a secondary objective was to maximise thermal performance while minimising the use of the imported nitride thermal posts. An image of the small batch panel of eight Hybrid Bricks can be seen in Figure 4.3.

The High-efficiency Bricks approached the thermal performance and optimisation of the Phase-II Upgrade Bricks by directly targeting the sources of the heat. To this end the all thermal posts used by the Hight-efficiency Bricks are aluminium oxide so as to allow direct comparison of their thermal performance to that of the Baseline DUT. The components determined to be the primary cause of the heat, which itself is a result of

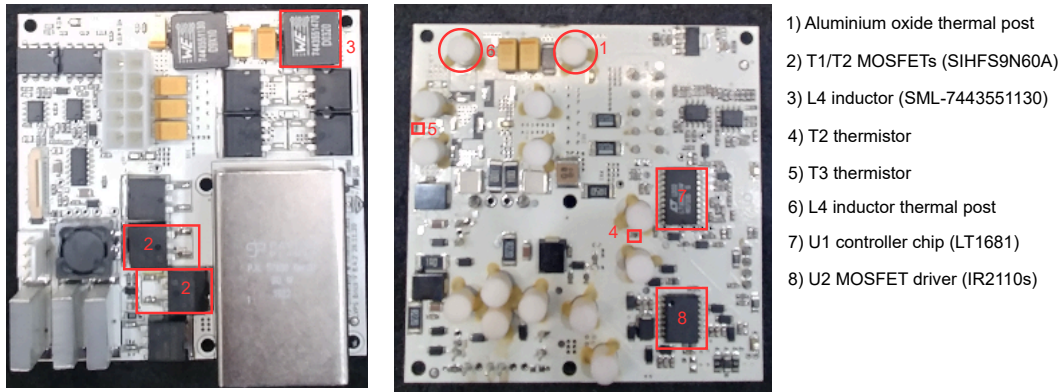


Figure 4.4: Top (Left) and bottom (Right) image of a V8.4.2 High-efficiency Brick.

inefficiency in the power conversion process, were the T1/T2 MOSFETs and the L4 inductor which are highlighted in Figure 4.4. This would be the first step when considering such a study in a typical commercial setting but as we know, these Bricks are required to operate within the radiation environment produced within the TileCal as a result of HL-LHC collisions. The implications of this are that if the high-efficiency Bricks are found to exhibit desirable thermal performance the newly proposed component/s would need to undergo further irradiation hardness qualification, as described in subsection 3.1.1. A component is by no means guaranteed to pass such campaigns which brings inherent risk in terms of production delays.

The selected T1/T2 MOSFETs and the L4 inductor are listed in Table 4.3. The SIHFS9N60A MOSFETs were selected due to their lower switching and conduction losses. Both the SIHFS9N60A and STB57N65M5 MOSFETs have identical D2PAK footprints as can be seen in Figure 4.4. This has two implications: The first is that no changes to the PCB design were required to accommodate the "new" component and the second is that no reduction in the operating temperature of the MOSFETs can be attributed to the increase in the area of the thermal interface between the components and the PCB/thermal posts. The selection of the SML-7443551130 inductor will be motivated in the thermal analysis that follows.

Schematic ID	Description	Part number
T1,T2	Power MOSFET	SIHFS9N60A [83]
L4	Power inductor	SML-7443551130 [84]

Table 4.3: High-efficiency Brick selected (variable) electronic components.

4.1.3 Experimental Apparatus

The experimental apparatus employed in this study form what is referred to as the Initial/Final test station. This test station is used as part of the post-manufacturing quality

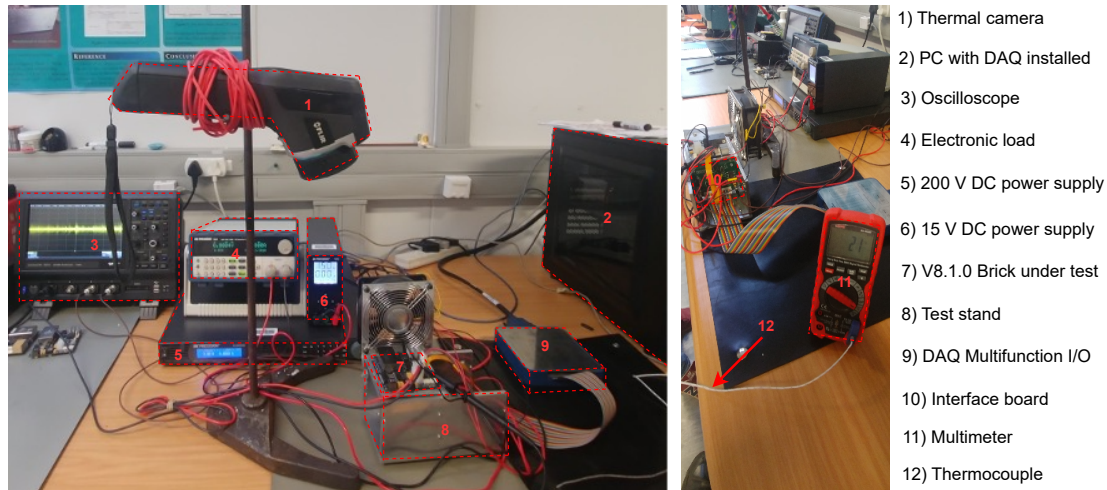


Figure 4.5: Images of the thermal performance study apparatus.

assurance procedure which will be further elaborated upon in chapter 7. A paper on the test station can be found here [85]. The Initial/Final test station functions to measure and test various performance metrics of a Brick but for the purpose of this study it was only used to allow for its operation by using its manual control feature and for the monitoring of the Bricks two inbuilt thermistors.

With reference to Figure 4.5, the test station can be seen to be composed of a test stand (8) to which the DUT (Brick) (7) is mounted as well as the interface board (10).

The test stand serves the additional function of allowing passive cooling of the Brick as its thermal posts are in contact with its aluminium frame. Active cooling can also be employed for prolonged testing by switching on a fan that is attached to the test stand. This method of cooling, using forced air, is not a reasonable analog to the way in which the Bricks are cooled within an fLVPS within the TileCal. Details of the TileCal leak-less cooling system were furnished in section 2.11. Further details pertaining to cooling of the the Bricks ,when on-detector, were provided in subsection 3.2.2 with additional context to the detector services found in section 2.10. A supplementary image of a disassembled fLVPS cooling plate can be found in Figure B.2. To overcome this shortfall the Initial/Final test station was augmented by a separate water-cooled system composed of an fLVPS cooling plate, to which the DUTs were affixed, that was serviced by a water chiller. An image of the augmented apparatus is provided in Figure D.1. In the paragraphs that follow all mention to active cooling refer to the water cooling of the DUTs using this system. The aforementioned interface board is responsible for interfacing the control and monitoring electronics of the test station with the Brick.

As can be seen in Figure 4.5:

- The control and monitoring of the Brick is undertaken by a custom LabVIEW application running on a Personal Computer (2)

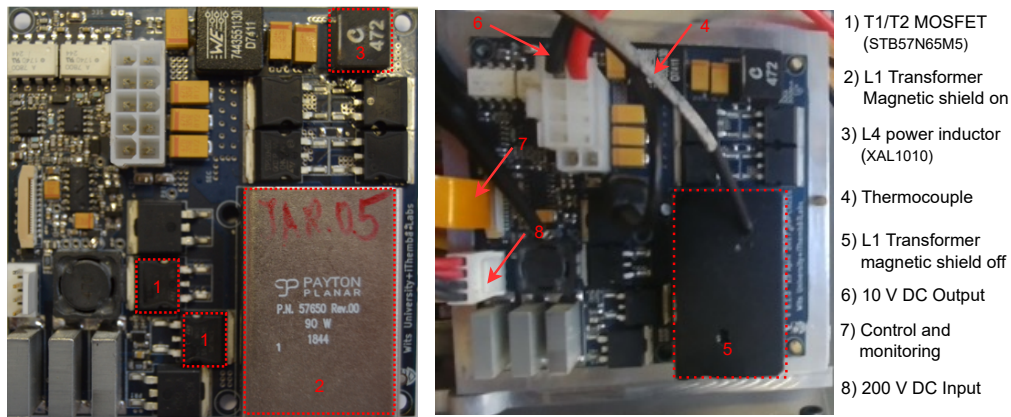


Figure 4.6: V8.1.0 Baseline Brick prior to testing (left) and during testing (right). Observe that the magnetic shielding has been removed from the L1 transformer to allow direct measurement of the transformer core using a thermocouple probe.

- The Brick steps the input voltage down to 10 V DC which is then supplied to an electronic dummy-load (4) that emulates the TileCal on-detector electronics. The applied load can be set to any value within the Bricks trip points.
- The Bricks start signal is provided by a non-programmable bench-top power supply set to 15 V DC. The power supply is connected to a relay located on the interface board which closes and routes the start signal to the Brick when instructed to do so by the LabVIEW application. This control signal comes from the DAQ Multifunction I/O (9) that is also responsible for monitoring the Bricks performance measurements in a similar way to that of ELMB2, within an fLVPS, functions. These values are the input and output voltages and currents as well as the two thermistor temperature measurements.
- As the study was focused on investigating the global thermal performance of the Brick it was decided that the two point temperature measurements provided by the Bricks on-board thermistors were insufficient. Therefore, thermography was employed by using a thermal camera (1).

4.2 Phase-II Upgrade Brick Metal-Oxide Semiconductor Field-Effect Transistor Single Event Effect Radiation Hardness Certification

4.2.1 Motivation

Due to the substantial improvement in thermal performance of the High-efficiency Bricks when compared to Hybrid B-type DUTs, as presented in section 4.1, it was decided that the proposed T1/T2 MOSFET (SIHFS9N60A) and L4 inductor (SML-7443551) components would be adopted for the Phase-II Upgrade Bricks subject to the component passing radiation hardness certification.

The SIHFS9N60A MOSFET is an active component therefore it was required to undergo radiation hardness certification as outlined in subsection 3.1.1. This section will cover the Single Event Effect (SEE) radiation hardness certification of the component that took place in 2021 and not the Non-Ionizing Energy Loss (NIEL) which took place at other irradiation facility and was conducted by other members of the research group. The Total Ionizing Dose (TID) certification similarly will not be covered although the DUTs irradiated for the SEE certification were also used for the TID certification. This was possible as various performance metrics were measured on the DUTs prior to irradiation at the PIF facility which were then repeated post irradiation to assess their TID performance. It should be noted that the Radiation Tolerance Criteria (RTC) calculated and presented in Table 3.2 are the current RTC as of 2023. The RTC that were used during this irradiation campaign were those which predated the values states in Table 3.2. The relevant RTC will be stated where necessary.

4.2.2 Device Under Test

The Device Under Test (DUT) is the SIHFS9N60A power MOSFET with a D2PAK package identical to that of the "legacy" STB57N65M5 MOSFET. The use of an identical package means that no changed to the Bricks Printed Circuit Board (PCB) will be required if the DUT passes its radiation certification. Figures of merit for both the proposed and legacy MOSFETs are provided in Table 4.4. The table includes the maximum Drain voltage that can be applied in the OFF-State (V_{Rated}), the maximum current that can be conducted in the 0N-State (I_D), and the on-resistance (R_{on}).

Part number	Package	V_{DS} (V)	I_D (A)		$R_{DS(on)}$ (Ω)
			$T_c = 25^\circ C$	$T_c = 100^\circ C$	
SIHFS9N60A	D2PAK	600	9.2	5.8	0.75
STB57N65M5	D2PAK	710	42	26.5	0.063

Table 4.4: Figures of merit of the proposed Phase-II Upgrade V8.6 Brick (SIHFS9N60A) and the V8.4.2 Bricks (STB57N65M5) T1/T2 power MOSFETs.

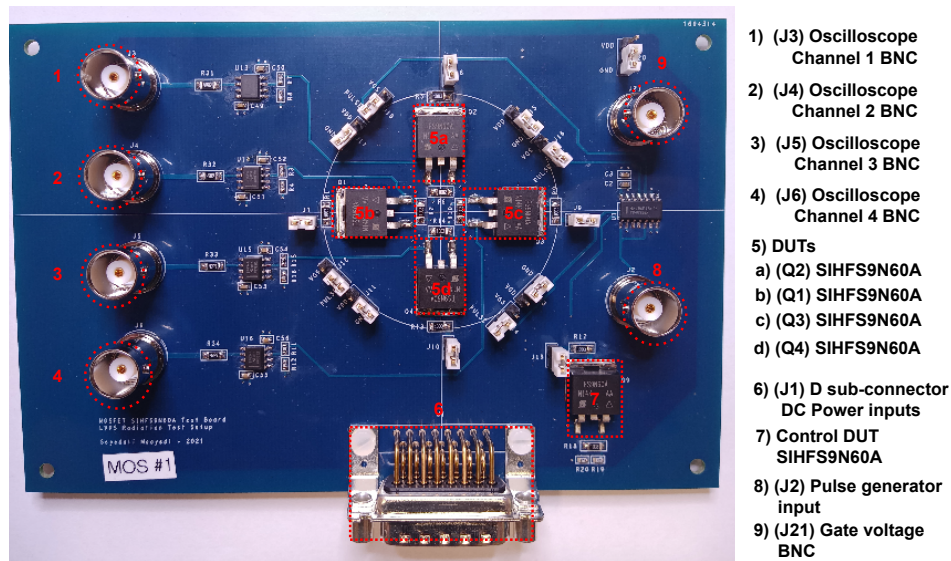


Figure 4.7: Front view of the SIHFS9N60A MOSFE test PCB.

A total of 16 DUTs were irradiated and monitored for the SEE certification. All DUTs were purchased from a single manufacturing lot with enough components procured for both pre- and main-production for both institutes. The procurement of enough SIHFS9N60A MOSFETs prior to them being proven to be able to survive and perform as required in the ATLAS inner barrel has a high risk associated with it but is necessitated as single lot procurement is highly challenging and there was no way to reserve a lot in the case of these MOSFETs.

The DUTs are mounted to a test PCB, which is pictured in Figure 4.7. This test PCB serves two primary purposes in that it is used for both the SEE and TID radiation hardness certification. This is possible as both require exposure to ionizing radiation (such as a proton beam). It is beneficial that irradiation for both certifications occurs simultaneously as access to beam-time is limited and has a high associated cost. To allow for the simultaneous irradiation of the DUTs (both SEE and TID) the PCB has two distinct sets of circuits each tailored to the specific type of test. As this section is focused on the former certification only this circuitry will be discussed but to avoid confusion the TID circuitry should be mentioned to avoid confusion as it is present on the test PCB. The TID pulse generator BNC connector (8) is visible on the front of the PCB as well as a gate voltage monitoring BNC (9). Both of these should be ignored.

The PCB serves numerous roles such as physically holding the four SEE DUTs (5a, 5b, 5c, 5d) in the beam. The DUTs need to be symmetrically located and aligned centrally within the beam to ensure equal irradiation. To facilitate this a cross-hair is printed on the test PCB. A control DUT (7), which is located outside of the beam and subsequently not irradiated, is also affixed to the test PCB. The four DUTs are monitored for SEE by a four channel oscilloscope which is connected to the PCB via four dedicated BNC connectors

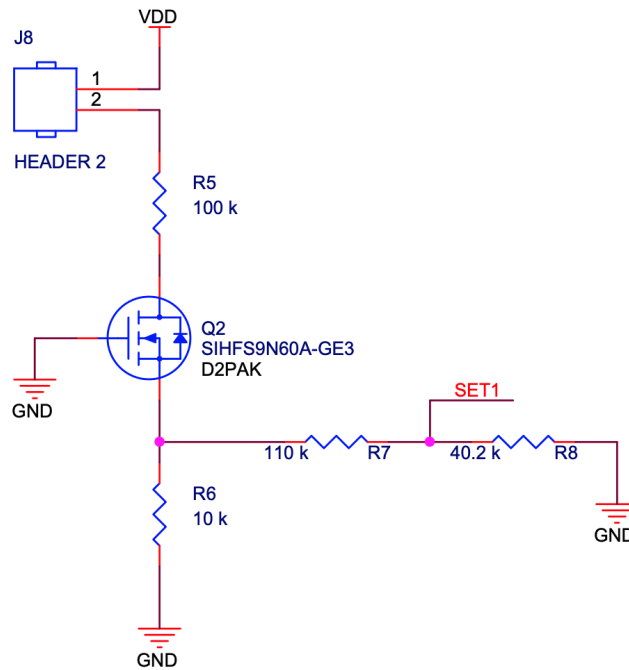


Figure 4.8: Schematic of the SIHFS9N60A Single Event Effect test circuitry for a single MOSFET. The test PCB has four identical circuits each one responsible for testing a single MOSFET. VDD = 200 V DC.

(1, 2, 3, 4). The DUTs associated BNC connector and oscilloscope channel are provided in Table 4.5. The 200 V DC bias voltage that is applied to the DUTs is provided by a DC power supply and routed to the DUTs via a D sub-connector (6). The applied bias voltage is not arbitrary as it needs to emulate that which will be experienced by the DUT when operating within the fLVPS Brick which receives bulk 200 V DC power from off-detector power supplies as explained in section 3.2.

PCB BMC connector	Associated MOSFET	Oscilloscope channel
J3	Q2	1
J4	Q1	2
J5	Q4	3
J6	Q3	4

Table 4.5: DUT circuit identifier and associated BMC connector and oscilloscope channel number.

The SEE test PCB circuitry is illustrated in Figure 4.8 with the the entire DUT test PCB schematic provided in Figure E.10 for reference. There are four identical ciruits, one for each DUT. VDD is the 200 V DC bias voltage that is routed through a head(jumper) (J8) to the DUT. The header can be removed if the DUT experiences a hard failure so as to isolated it from the VDD power rail allowing for testing to continue. The MOSFET (Q2) has its gate attached to ground as seen in Figure 4.8.

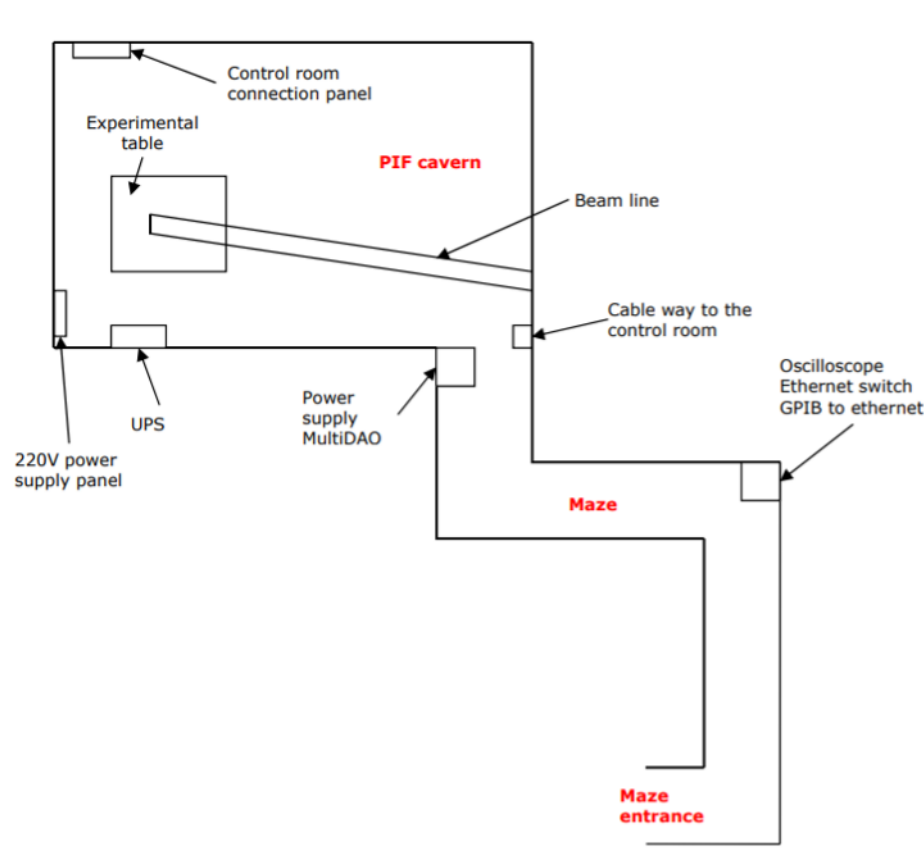


Figure 4.9: Schematic of the Paul Scherrer Proton Irradiation Facility (PIF) experimental area.

A MOSFET should only turn on and conduct if the gate voltage goes higher than the source voltage. In this case as the gate is connected to ground the MOSFET stays off unless there is a Single Event Burnout (SEB). SEBs can be partitioned into two distinct types, namely destructive and non-destructive. A destructive SEB of the MOSFET is characterized by the permanently shorting of VDD to ground. Even though the gate is connected to ground it will act as a short between drain and source. If a destructive SEB occurs the MOSFETs associated VDD jumper must be removed. A non-destructive SEB is characterized as a short between the MOSFETs source and drain which occurs for a very small duration of time like a transient. The transient is propagated via the SET1 track to a buffer and subsequently routed to the oscilloscope via the BNC connector to be recorded.

The oscilloscope was set to trigger at a threshold of 72 mV which was found to be at the threshold of the observed electronic noise of the test setup.

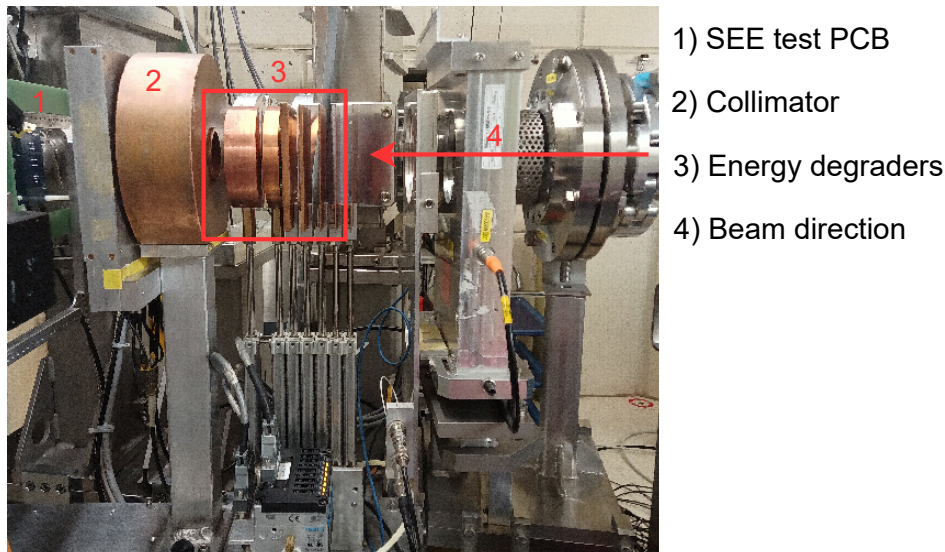


Figure 4.10: Image depicting the experimental table at the end of the PIF beam-line. The SEE DUT test PCB (1) can be seen mounted to the experimental table immediately after the collimator (2). The proton beam travels from right to left in the image and passes through a series of energy degraders (3) before reaching the collimator.

4.2.3 Irradiation Facility and Experimental Apparatus

SEE testing was performed at the Paul Scherrer Institute (PSI), using the Proton Irradiation Facility (PIF). The initial proton beam for the PIF is delivered from the PROSCAN accelerator with the help of the primary energy degrader, which allows setting the initial beam energy from 230 MeV down to 74 MeV if required. The initial beam energies can be set to 230, 200, 150, 100 and 74 MeV. The beam is subsequently guided to the experimental area, pictured in Figure 4.9, where the PIF facility is located.

The irradiation is controlled from the experimental barracks located on top of the PIF area. Connections were made between the experiment room and the control room using the connection panel allowing for direct control and monitoring of the experiment from the barracks. The instruments used for the experiments are placed as far as possible from the beam-line in the maze to ensure that they are not irradiated.

The PIF cavern is equipped with an experimental table at the end of the beam-line, pictured in Figure 4.10, that allows the Device Under Test (DUT) to be oriented in the x, y and z direction. This feature allows precise centering of the DUTs in the beam. The PCB to which the DUTs are attached and which facilitates their testing is attached to a metallic frame mounted on the experimental table. On top of the experimental table are located, listed from left to right in Figure 4.10, a copper collimator that has a diameter of 60 mm, energy degraders and then other beam monitoring equipment.

Prior to irradiation the test PCB is aligned with the central axis of the beam making use of a laser cross-hair which can be seen in Figure 4.11.

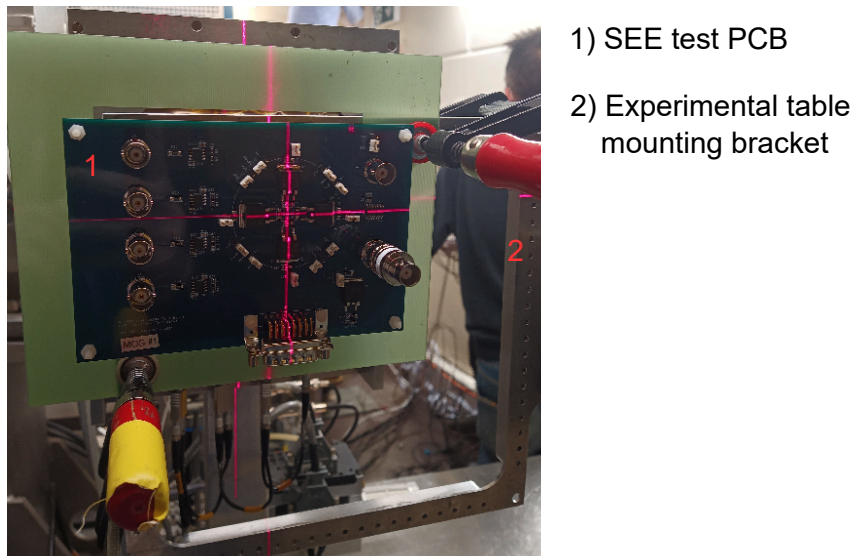


Figure 4.11: Alignment of the SEE DUT test PCB (1) on the experimental table using a laser cross-hair. The test PCB is affixed to a mounting bracket (2).

4.3 Brick Reliability and Lifetime Analysis

4.3.1 Motivation

The quantification of the reliability of the Phase-II Upgrade Brick is motivated due to several factors which can be broadly categorised under manufacturing, maintenance and detector performance considerations.

As the Bricks will be manufactured using single-lot active components it is vital that enough are produced during the production run to not only fully populate the TileCal, 2048 units, but that sufficient spares are also produced. The spare Bricks will be used to replace any Bricks that fail during the ~ 10 year operational period of the HL-LHC and those Bricks that fail during the post production quality assurance testing. The reliability of the Bricks once installed, commissioned and fully operational within the TileCal will be the subject of the analysis that follows, whereas quality assurance testing of the Bricks and the associated failures will be discussed in chapter 7.

The last reliability analysis was undertaken during the Final Design Review (FDR) process in October 2020. At this time, the "standard" V8.4.2 was the latest Brick iteration at the time and as such was the subject of this analysis. Therefore, this analysis needs to be repeated for the pre-production V8.6.1 Brick which has incorporated the design changes motivated in section 4.1 and certified for use in the ATLAS HL-LHC environment post radiation hardness certification, as presented in subsection 4.2.1. The analysis will employ the same methodology as that of the reliability analysis of the V7.5.0 Brick as published by A. Senthikumaran et al [86].

4.3.2 Introduction to Reliability in Electronics

The reliability of the Brick can be defined as the probability that it will perform its required function, provide 10 V DC power to the front-end electronics, without failure under certain predefined operating conditions for a stated period of operation. A Brick failure, as defined in an operational context, is the permanent inability to provide power to its associated front-end electronics, necessitating replacement during the Year-End Technical Stop (YETS). It should be noted that this definition of Brick failure precludes the occurrence of any transient behaviour such as trips which were discussed in section 3.4.1.

The Bricks are considered to be non-repairable as access to them within the TileCal is limited to only once per year during nominal ATLAS and HL-LHC operations. This is because once a Brick has failed it, as well as its associated front-end electronics to which it provided power, will remain offline until replacement. This distinction is important as the approach to conduct a reliability analysis varies between repairable and non-repairable systems.

The lifetime of a Brick is specified as the time at which its electrical parameters have drifted out of the specified provided in Table C.1. During the Bricks lifetime the instantaneous probability of the first and only failure is called the hazard rate $\lambda(t)$. The term "hazard rate" is used interchangeably with "failure rate" within most reliability literature. This rate varies over the lifetime of a Brick with an idealised characterisation of the time variation of the hazard rate is shown in Figure 4.12. The observed "reliability curve" is commonly referred to as the bathtub curve due to its apparent shape. There are three distinct reliability periods associated with this curve namely the Infant mortality, Nominal operational and Wear-out periods.

The Infant mortality period covers the early stages of device use, the failure rate is relatively high and decreases over time. The failures occurring in this region are generally due to manufacturing defects at both the component and system level. In the context of the fLVPS Brick this period would occur during the first months of operation within the Phase-II Upgrade TileCal during the commissioning process which is inherently undesirable. Any Bricks that fail would need to be replaced which would require access to the inner-barrel of ATLAS which would be limited. There would also be the compounding issue that the replacement Bricks would themselves be in the Infant mortality period. Decreasing hazard rates are observed in systems which become less likely to fail as their survival time increases. The burn-in of electronic systems, such as the Bricks, is a good example of the way in which knowledge of a decreasing hazard rate can be applied to facilitate an improvement in system reliability. The infant mortality period and addressing it using burn-in will be discussed further in chapter 7.

After the Infant mortality period a much lower and stable (constant) failure rate region occurs. This region is referred to as the Useful life period. The failures that occur in this region are often referred to as "random failures" which can be due to small device or component defects that were not severe enough to present themselves during the Infant

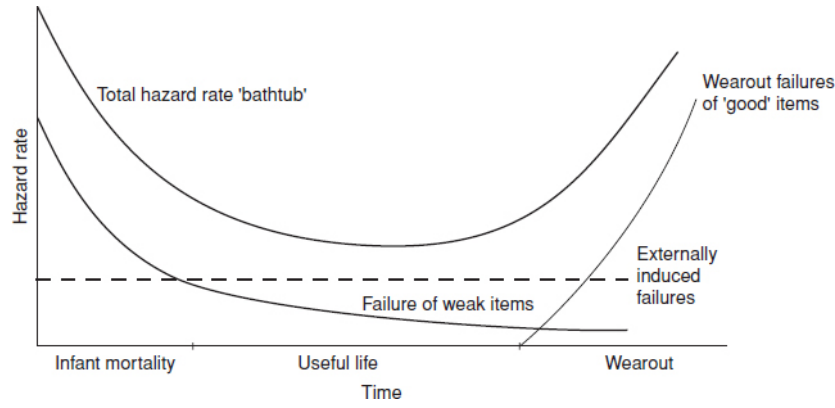


Figure 4.12: The Classical Bathtub Curve illustrating the Infant mortality, Useful life and Wear-out periods [87].

mortality period. Random failures can also be due to factors such as accidental ambient factors and over-stress factors such as transient circuit overloads. The Wear-out period is the final period of a systems lifetime. Within this period a rapid increase in the failure rate is observed. The Wear-out region is driven by normal material/device degradation.

The Useful life period, in which a constant failure rate is observed, will be the focus of the subsequent reliability analysis. The constant failure rate is given by the total number of failures divided by the total operational time of the devices.

The failure rate of a system, a Brick in this context, as according to the basic series reliability model, is given by:

$$\lambda_{Brick} = \sum_{i=1}^n \lambda_i \quad (4.1)$$

Where λ_i is failure rate of the i -th component of a Brick in which there is no redundancy. Failure rates of components are quoted in reliability data sheets. These rates are expressed as the number of failures per one billion device hours of operation.

This expression or "unit" is referred to as the devices Failures-In-Time (FIT) where 1 FIT is defined as:

$$1 \text{ FIT} = \frac{1 \text{ failure}}{1 \times 10^9 \text{ hours}} \quad (4.2)$$

The Mean Time To Failure (MTTF) is another reliability metric that is used to characterise non-repairable systems. it is defined as the average elapsed time for a part or component to fail for the first and only time.

The MTTF of a Brick is given by:

$$MTTF = \frac{1}{\lambda_{Brick}} \quad (4.3)$$

and is generally expressed in units of hours or years.

4.4 Phase-II Upgrade Brick Quality Assurance

The following section is based on the original form of a published paper titled "A Burn-in Apparatus for the ATLAS Tile Calorimeter Phase-II Upgrade Transformer-Coupled Buck Converters" before manipulation to conform to the journals style and other requirements [88]. This section is used with great appreciation to all co-authors.

4.4.1 Motivation

Access to the LVPS Bricks occurs approximately once per year during the Year-End Technical Stop (YETS) of the ATLAS detector, requiring the Bricks to be in the open position. Consequently, if a Brick experiences a permanent failure, it remains in that state until the upcoming YETS. This leads to a portion of a module's Front-End (FE) electronics specifically, one-eighth (sixth) in the case of a single Brick failure for a long (extended) barrel module being offline for a corresponding period. During this downtime, the offline FE electronics are entirely incapable of collecting collision data, underscoring the critical importance of Brick reliability. A failure is defined as the permanent inability of the fLVPS to provide power to its associated front-end electronics, necessitating replacement.

The reliability of electronic devices, such as Bricks, may deviate from their predicted design reliability due to latent and patent defects associated with production and its components. Post-manufacturing, quality assurance testing is essential for all fLVPS Bricks to address this issue [89]. The goal is to enhance the reliability of the surviving population by identifying and excluding Bricks with such defects.

4.4.2 Quality Assurance Procedure

Figure 4.13 illustrates the quality assurance procedure, consisting of five distinct tests: automated visual inspection, X-ray scan, initial testing, Burn-in, and final testing. Each test is tailored to ensure the high reliability of the Brick population upon installation on the detector by detecting and/or stimulating any patent or latent defects that may be present.

Upon completion, each Brick is assigned a unique identification barcode to facilitate tracking throughout its lifespan in the experiment. Subsequently, the Bricks undergo an automated visual inspection to identify and rectify visible manufacturing defects. Following this, an X-ray scan is performed to focus on detecting potential solder outgas voiding that may have occurred between specific components during the reflow process, such as the primary-side switching FETs and the associated ceramic post. The identification of these voids is crucial due to their tendency to reduce thermal conductivity between the electronic component tab and the ceramic post at the thermal interface.

Both initial and final testing procedures are identical, utilizing the same test apparatus and methodology, and are named based on whether they occur before or after Burn-in, respectively [85]. These tests assess various performance metrics to ensure that the

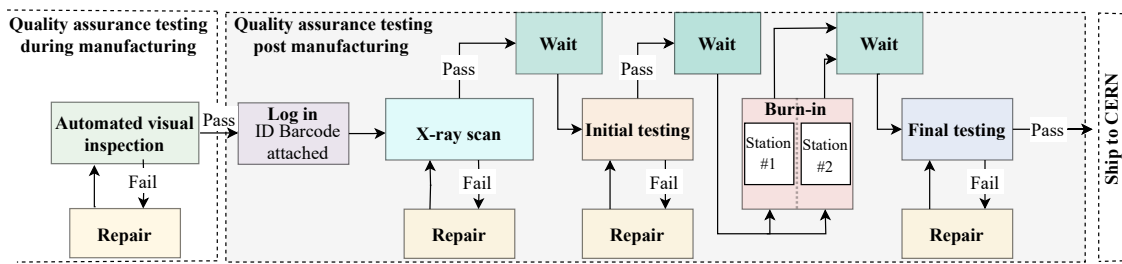


Figure 4.13: Block diagram illustrating the finalized fLVPS Brick quality assurance procedure

tested Brick operates within its design specifications. Conducting performance testing both before and after Burn-in offers valuable insights into potential performance degradation resulting from the Burn-in process and helps screen out Bricks that may have suffered permanent damage. However, Bricks with latent defects that marginally affect their functionality may not be identified through performance testing alone, potentially leading to their installation within the TileCal. Such Bricks may fail early in the life of the Phase-II Upgrade TileCal, contributing to a high initial failure rate, commonly observed in the electronic infant mortality region.

System-level Burn-in is mandatory for all manufactured Bricks. This Burn-in occurs when the Bricks are fully assembled and operational. The purpose of Burn-in is to detect patent and/or latent defects that may not have been identified during initial testing. Burn-in primarily targets patent defects that may emerge during the early life of the Bricks. However, it's important to note that latent defects, typically surfacing during normal operation, can be transformed into patent defects through external overstress application [90].

The Burn-in process subjects the Bricks to overstress conditions, such as elevated operating temperatures and applied loads, beyond their nominal operating conditions. This stimulates failure mechanisms within the non-performant Brick population. While Bricks need not experience catastrophic failure during Burn-in, potential deterioration in performance is identified during final testing. It's crucial to emphasize that Burn-in doesn't enhance the reliability of an individual Brick but rather improves the overall reliability of the surviving Brick population by removing any identified non-performant Bricks.

Efforts will be made to repair Bricks removed from the population due to their high per-unit cost and the unique nature of the active components, independently certified for radiation hardness in production lots. These lots, containing a fixed unit number, are approved for use in production. Repaired Bricks undergo the quality assurance procedure again until they pass the entire process or are deemed irreparable. The Burn-in apparatus is custom-designed to accommodate the unique nature of the Bricks it tests, a process further discussed in subsequent paragraphs.

4.4.3 Burn-in Station

The Burn-in station follows an iterative design akin to that of the Bricks and is responsible for executing the Burn-in procedure. The primary design imperative for the latest Burn-in station is its capability to consistently apply the Burn-in procedure to each of the Phase-II Upgrade Bricks during the testing of the entire Brick population. Given the extensive scale of Brick quality assurance testing, additional requirements are imposed to accommodate the involvement of many junior researchers. Thus, it is imperative that the Burn-in station's operation is both straightforward and secure, allowing utilization by non-experts. The station is composed of several distinct components namely the test-bed (A), pictured in Figure 4.14, cooling system that utilised an external water-chiller (C), a +200 V DC High Voltage (HV) power supply (B), electrical wiring, custom hardware and software. The custom wiring document is provided in Appendix F.

The Burn-in station incorporates its custom hardware and the Bricks undergoing the Burn-in procedure within the test-bed as will be seen in subsection 4.4.4. The test-bed is fully enclosed in a metal (main chassis) and perspex (top and front lid) enclosure, mitigating the impact of external environmental factors on the operating temperature of the Bricks. Additionally, the test-bed serves a safety function by preventing inadvertent contact with electrified elements. Thermal and electrical insulation is employed within the test-bed to prevent internal water condensation and potential electrical shorts, with the entire system being physically grounded. A Computer-Aided Design of the test-bed is provided in Figure F.1 with the test-bed panel and frame schematics provided in Figure F.2 and Figure F.3, respectively.

An active cooling system is employed to regulate the operating temperature of the Bricks—a critical Burn-in parameter—during the Burn-in process and to dissipate heat generated by the dummy loads they power. This cooling system utilizes a commercial external water chiller that adjusts distilled water to the desired set-point before circulating it to the four Brick Cooling Plates and subsequently to the four dummy load CPs, all within a single cooling loop. This cooling loop is illustrated in Figure 4.15. A custom inlet (1-4) and outlet (4-1) water manifold is required. The schematics of the custom manifold are provided in Figure F.4. Implementing a single cooling loop allows a single external water chiller to control the Burn-in temperature of the Bricks and cool the dummy-load boards. The water chiller possesses sufficient cooling capacity to regulate the temperature of two Burn-in test-beds simultaneously. While this design reduces the cost of the Burn-in stations, it introduces additional complexities in cooling the dummy load boards. The coolant temperature can be manipulated to induce corresponding changes in the temperature of the Bricks, facilitating the setting of the Brick Burn-in operating temperature.



Figure 4.14: Labelled image of a Wits Burn-in test station. The test-bed (A), with its perspex cover and lid removed, can be seen on the left-hand side of the image. Input power to the Bricks is provided by the programmable DC power supply (B). The control of the applied Brick Burn-in temperature parameter is undertaken by a water chiller, which is also responsible for removing heat from the dummy loads (C). The control and monitoring of the Burn-in procedure and DC power supply are undertaken by the Burn-in LabVIEW application running on a personal computer (D).

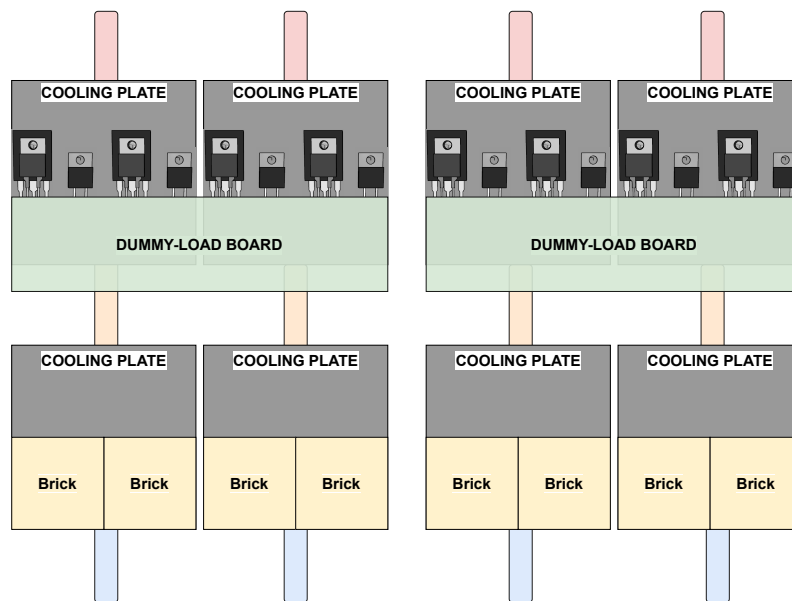


Figure 4.15: Simplified block diagram of the Burn-in Stations cooling system within the test-bed. The blue pipes indicate cold inlet coolant and the red pipes indicate hot outlet coolant. The Bricks receive the coolant first so as to allow precise temperature control.

4.4.4 Burn-in Station Custom Hardware

The burn-in station custom hardware is composed several Printed Circuit Boards (PCBs) that can be seen in Figure 4.16. The PCBs are subdivided into four types, namely, the

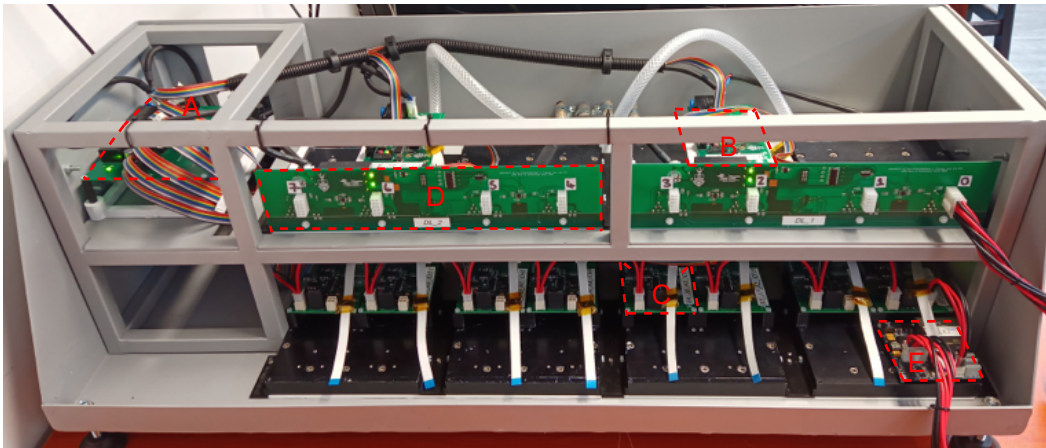


Figure 4.16: Labelled image of a Wits Burn-in station test-bed with its perspex covers removed. A single Brick undergoing Burn-in in Channel 0 can be observed (E). The main board (A) is connected to two Load Interface Boards (B), each of which is connected to an associated Dummy Load Board (D). The Main Board is also connected to eight Brick Interface Boards (C). The black cooling plates to which both a Brick and the Dummy Load Boards are affixed can also be observed. Note that only one of each PCB type is labelled.

Main Board (MB), the Brick Interface Board (BIB), the Load Interface Board (LIB) and the Dummy Load Board (DLB). The PCBs are supplied by 220 V AC mains power which is rectified using DC-DC converters to supply power to the active components.

As illustrated in Figure 4.17, there is one MB per burn-in station responsible for addressing and demultiplexing (one-to-many signal channelisation) of the interface boards (BIBs and LIBs). The addressing and demultiplexing scheme allows serial communication from a Burn-in LabVIEW Application (BLA) running on a PC, to communicate via a Universal Serial Bus (USB) to a Universal Asynchronous interface on the MB to the various interface boards. A program running on the PIC of the MB sequentially polls each of the interface boards to perform a particular task. There are eight BIBs per burn-in station with one associated with each of the Bricks undergoing the burn-in procedure. The BIBs provide control and monitoring of their respective Bricks while the LIB provide control and monitoring of a dummy load connected to the respective Brick. A single Brick is connected to a BIB for readout of performance measurements where the Brick output power is connected to a DLB that incorporates closed-loop Voltage Controlled Current Sink (VCCS) circuitry. The upcoming sections present a more comprehensive analysis of the main hardware components and their functions.

The addressing and demultiplexing scheme allows serial communication from a Burn-in LabVIEW Application (BLA) running on a PC, to communicate via a Universal Serial Bus (USB) to a Universal Asynchronous interface on the MB to the various interface boards. A program running on the PIC of the MB sequentially polls each of the interface boards to perform a particular task. There are eight BIBs per burn-in station with one associated with each of the Bricks undergoing the burn-in procedure. The BIBs

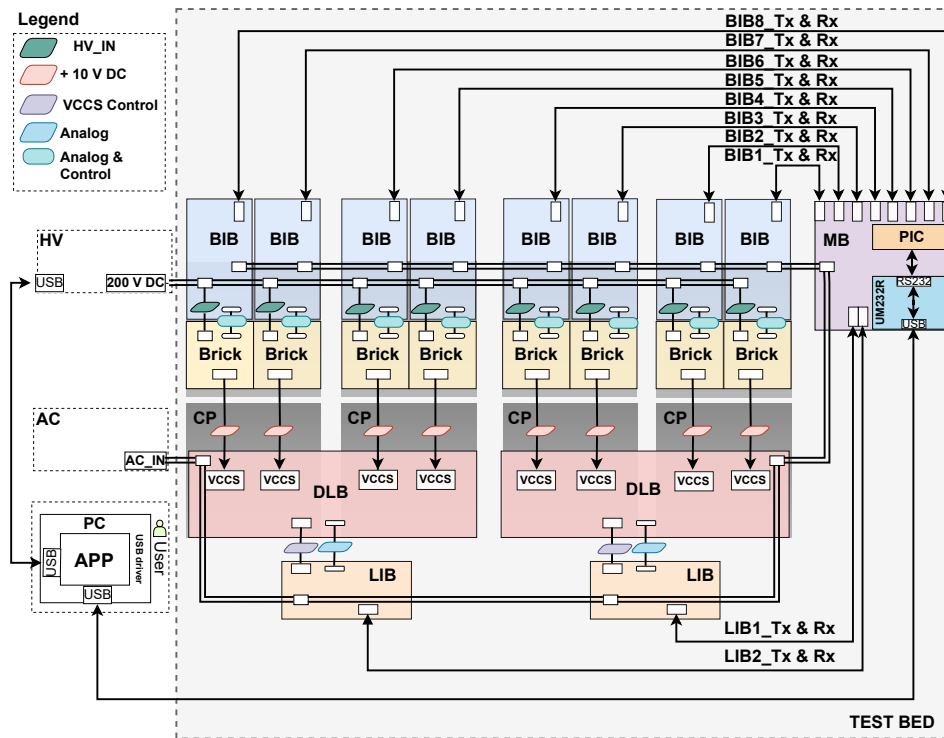


Figure 4.17: A simplified block diagram of the Burn-in station illustrating the test-bed and inter-connections between the various custom hardware components of the complete system.

provide control and monitoring of their respective Bricks while the LIB provide control and monitoring of a dummy load connected to the respective Brick. A single Brick is connected to a BIB for readout of performance measurements where the Brick output power is connected to a DLB that incorporates closed-loop Voltage Controlled Current Sink (VCCS) circuitry. The upcoming sections present a more comprehensive analysis of the main hardware components and their functions.

Mainboard

The Burn-in station is employs a single MB responsible for communicating to the BIBs and LIBs through an application-specific control and monitoring program developed in LabVIEW. As illustrated in Figure 3.18(b), the BLA sends commands to the PIC over a USB to RS232 converter (UM232R) for serial communication to the PIC. A Data Terminal Ready (DTR) signal line of the UM232R passes through an opto-coupler (6N137S) and is momentary triggered once a communication link is established with the BLA, causing the PICs of the MB and interface boards to reset.

Universal Asynchronous Receiver / Transmitter (UART) hardware flow control is partially introduced by asserting and deasserting a Request To Send (RTS) signal from the UM232R to address the interface boards using the select lines denoted by S0-S9 shown

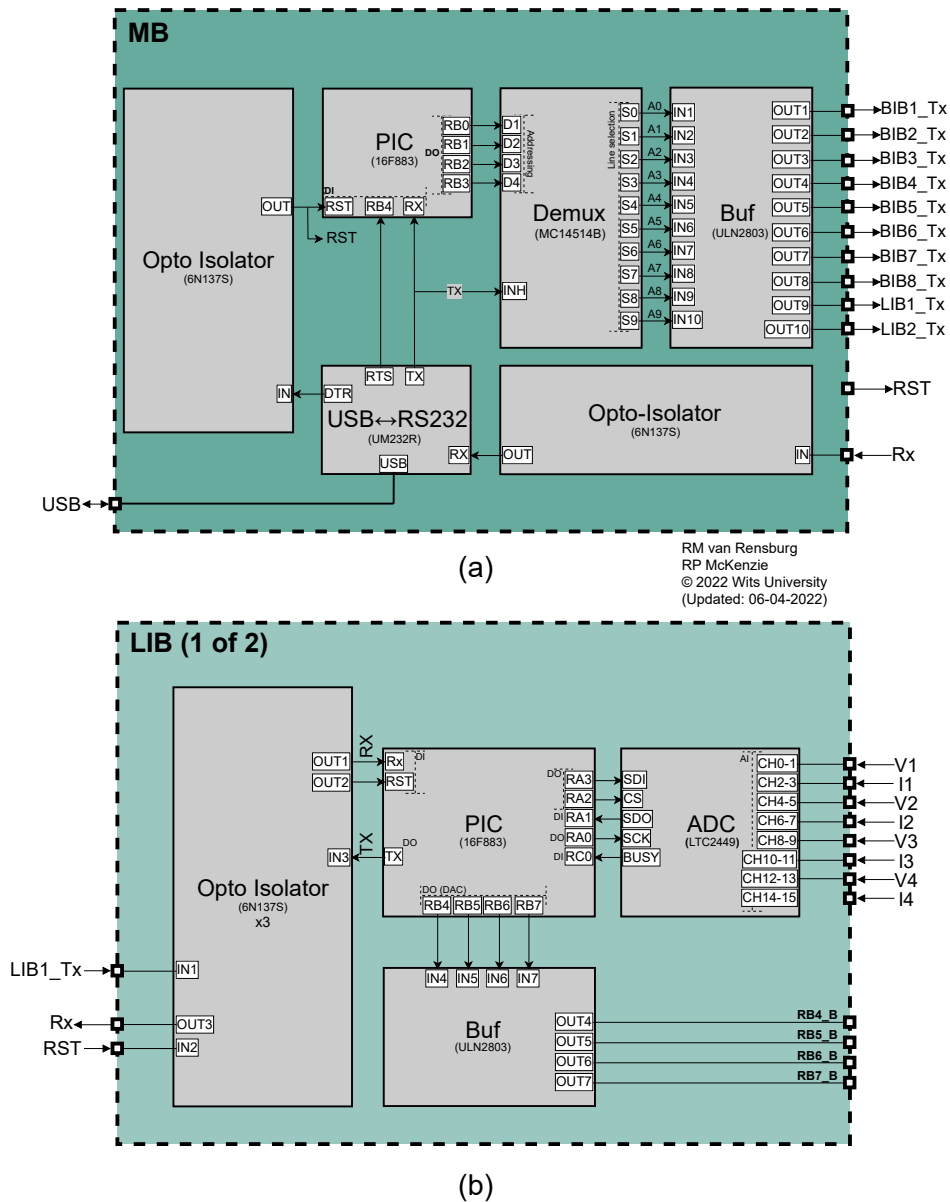


Figure 4.18: Simplified block diagram illustrating burn-in station hardware components and interconnects. The (a) MB ensures bi-directional serial communication to interface boards. A serial signal (BIB1_Tx...BIB8_Tx and LIB1_Tx...LIB2_Tx) is sequentially transmitted from the MB to their respective interface boards, where (b) represent one of the two LIBs.

in Figure 4.18. Assert and deassert of the RTS line is controlled by the BLA through the RTS digital output of the UM232R fed to a digital input RB4 of the PIC. Once the RTS line is asserted, the PIC firmware of the MB enters a conditional statement that reads a serial signal (Rx) from the UM232R (Tx) that changes the states of the digital outputs RB0-RB4 that feeds to the data lines D1-D4 of the demultiplexer (MC14514). The data lines D1-D4 correspond to a four-bit address that selects the line representing an interface board for communication over the desired select lines S0-S9 through the inhibit line (INH) of the

demultiplexer. While the RTS line is deasserted, addressing is complete and requests are sent by the BLA followed by USB to RS232 conversion to the selected interface board address A0-A9 to perform a particular task. Since the demultiplexer inverts the serial bit signal representing a character or string of characters representing a particular task for the interface boards to perform, buffer (ULN2803) circuits are implemented for buffering PIC control outputs and reverting the serial bit signal in its original state send by the BLA. The BIBs and LIBs perform tasks such as enabling and disabling Bricks, setting load currents and reading analog channels for measuring Brick and load performance.

An opto-coupler (6N137S) with an open collector output acts as a line receiver that provides signal isolation of the UART signals transmitted from the interface boards. The UART signals from the interface boards are transmitted to the UM232R converter and ultimately the BLA over USB for monitoring and data logging.

Interface Board

A Burn-in station contains eight BIBs and two LIBs, which connect eight Bricks and two DLBs, respectively. A BIB provides the control and data acquisition of a Brick and a LIB provides the control and data acquisition of a dummy load. As illustrated in the block diagram in Figure 4.18 each of the serial signals (BIB1_TX to BIB8_TX) transmitted from the MB have a dedicated BIB where an Analog-to-Digital Converter (ADC) reads directly from the Brick. Similarly, each of the serial signals (LIB1_TX to LIB2_TX) transmitted from the MB have a dedicated LIB, where the ADC reads from one of the two DLBs shown in Figure Figure 4.19. The control and data acquisition of the interface boards are explained in more detail in the upcoming sections.

Brick Interface Board Control

As discussed in section 4.4.4, a serial signal (from either one of the BIB1_TX...BIB8_Tx signals) transmitted by the BLA represents a particular task to perform by the PIC (Part No. 16F883). With reference to Figure 4.19, the serial signal is first buffered through an opto-coupler (Part No. 6N137S), which provides signal isolation from the MB and is received by an Rx input of the PIC. The Rx signal is then processed by the PIC firmware where a particular task is performed to read the analog measurements from a Brick.

To enable and disable a Brick, a logical AND gate (Part No. SN74LVC) and a dual-solid-state relay (Part No. LBA716) are used to switch +15 V DC to a tristate input of a Brick. A tristate represents three voltage levels to start Bricks from an Embedded Local Monitor Board (ELMB), however, only an external 0 V DC and +15 V DC signal is needed to enable or disable a Brick, respectively, during a Burn-in procedure.

The control of a Brick may be dissected using a logic truth table as follows: When both digital outputs RB0 and RB2 of the PIC are logic low (0 V DC), the tristate line of the solid-state relay is connected to the GND (0 V DC). When RB0 is logic low and RB2 is

Consequently, with the High-Voltage (HV) switched by the MOSFET, the Brick will start once the NO-2 outputs a +15 V DC signal on the tristate input of the Brick.

Brick Interface Board Data Acquisition

A 24 bit delta-sigma low-noise ADC (Part No. LTC2449), which provides eight differential or 16 single-ended analog input channels, is incorporated into the data acquisition of the interface boards. With reference to Figure 4.18 (b) and Figure 4.19 (c), the ADC has an internal 4 kHz multiplexer capable of scanning each of the eight differential channels at 500 Hz. The ADC uses the Serial Peripheral Interface (SPI) protocol for bi-directional communication with the PIC. The PIC provides a clock signal to the Serial Clock (SCK) input of the ADC to ensure data transfer synchronization. During the control of the SCK during an ADC data output cycle from the PIC, analog measurements are taken by first sending a serial bit stream request containing the resolution with the desired analog input channel to read from the Serial Data Input (SDI) of the ADC. The ADC responds by transmitting a serial bit stream from the Serial Data Output (SDO), representing the analog value measured by the particular channel. The Chip Select (CS) input of the ADC is controlled by the PIC and kept at a logic low during the analog-to-digital conversion cycle. While the conversion is in progress, the Busy line of the ADC is kept at a logic high and is fed back as a digital output to the PIC. Once the conversion is complete and the serial bit stream representing an analog value is transmitted to the PIC, a new conversion cycle is requested when a low-to-high transition is signaled on the CS input. An ADC driver that incorporates SDI, SDO, SCK, CS and Busy signals is implemented in the PIC firmware of the interface boards. The BIB data acquisition involves reading four differential inputs, namely input current (I_IN), input voltage (V_IN), output current (I_IN), output current (I_OUT) and two single-ended temperature measurements (T_MEAS_2 and T_MEAS_3) from the Brick. The serial bit stream representing an analog value is transmitted back to the Rx input of the MB in for monitoring and data logging in the BLA.

Load Interface Board Control

The LIB controls the load current of a Brick by sending digital commands received by the BLA to a Digital-to-Analog Converter (DAC) located on the DLB. As discussed in section 4.4.4, a serial signal (from either the LI1_TX or LI2_TX signals) transmitted by the BLA represents a particular task to perform by the PIC (Part No. 16F883). With reference to Figure 4.19 (c), the serial signal is first buffered through an opto-coupler (Part No. 6N137S), which provides signal isolation from the MB and is received by an Rx input of the PIC. The Rx signal is then processed by the PIC firmware, where the DAC commands are sent over to the DLB shown in Figure 4.19 (d). The PIC digital outputs RB4, RB5, RB6 and RB7 in Figure 4.19 (c), are dedicated to controlling the Data, CLK, load and LDAC signals of the DAC (Part No. TLV5620IDR) shown in Figure 4.19 (d). The digital

conversion is fed as the setpoint to a Voltage-Controlled Current Sink (VCCS) located on the DLB and explained in more detail in section 4.4.4.

Load Interface Board Data Acquisition

The LIB uses the same data acquisition hardware as explained in section 4.4.4. The LIB data acquisition involves reading eight differential inputs representing voltage and current measurements from their respective Bricks, where a DLB acts as resistive loads for four bricks. Similarly, a second DLB provides resistive loads for the other four Bricks. With reference to Figure Figure 4.19 (c), the serial bit stream representing an analog value is transmitted back to the Rx input of the MB in Figure 4.18 (a) for monitoring and data logging in the BLA.

Dummy Load Board

A Burn-in station contains two DLBs that incorporate four VCCSs, which use high precision operational amplifiers and N-channel MOSFETs. The MOSFET is capable of a drain-to-source voltage of 200 V and supplying 50 A of drain current with a maximum on-resistance of 0.4 ohms. The amplifier acts as a comparator for error detection, which outputs a correction voltage to the gate of the MOSFET (Part No. IRFP260NPBF).

As illustrated in Figure 4.19 (d), a controlled voltage (O1) from the DAC is fed to the inverting input of the amplifier (Part No. OPA2197IDR). Closed-loop feedback is established by a voltage taken from a shunt resistor (R_{shunt}) fed back to the non-inverting input of the amplifier. The Brick supplies a +10 VDC to the drain of the MOSFET, where the voltage over the shunt resistor (R_{shunt}) is proportional to the load current.

Resistors R1 and R2 in Figure 4.19 (d) further provide voltage attenuation of the control signal to the inverting input of the amplifier and can be adjusted for higher current control while capacitor C1 and resistors R3 and R4 are configured as a low-pass differential RC filter to ensure loop stability. A voltage signal is fed into the gate of the MOSFET, which adjusts the on-resistance, whereby the current is sunk from the source to the drain of the MOSFET to the Ground (GND). The MOSFET dissipates heat through a cooling plate, which is water-cooled.

The thermostat (Part No. 67F110) switch, denoted by TS in Figure 4.19 (d), provides additional protection by closing upon a rising temperature of between 85 °C and 95 °C and consequently shorting the inverting input of the amplifier to the GND. The short to the GND leads to almost no current flowing through the drain to source of the MOSFET. Voltage divider circuits (R_{shunt} , R6, R7 and R9, R10, R11) are used as signal attenuators for the Brick output voltage and load current measurements fed to differential inputs of the ADC.

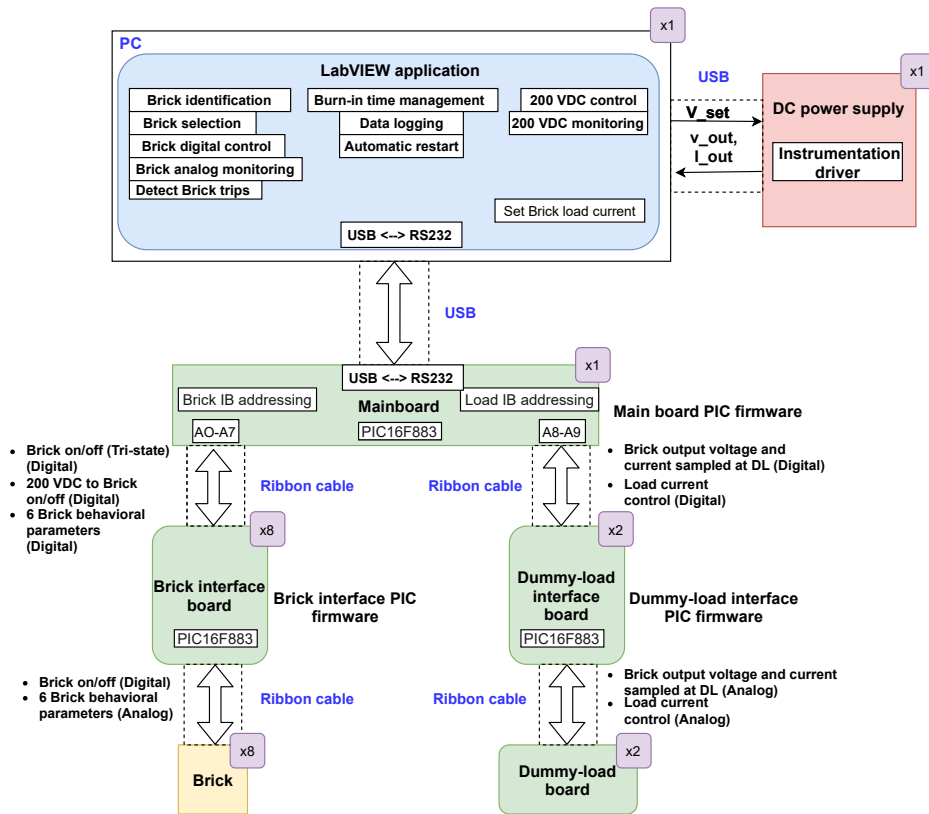


Figure 4.20: A simplified block diagram of the Burn-in station communication system. A Burn-in LabVIEW Application (BLA) running on a PC is responsible for the control, monitoring and management of the Burn-in procedure.

4.4.5 Custom fLVPS Brick Burn-in Station Software

This section presents Work done in collaboration with Roger Van. Rensburg, of the school of physics at the University of the Wiatersrand.

With reference to Figure 4.20, the BLA provides control and monitoring of the Burn-in station and communicates via USB to both the MB and HV power supply using separate USB ports. The PC runs the BLA responsible for Brick identification, Brick selection, Brick control (Brick start, stop and set current load), Brick load performance (Brick input and output measurements), HV control and monitoring, Brick trip detection, Brick automatic restart, Burn-in time management and data logging.

An addressing scheme is implemented for communication from the BLA through the MB to the interface boards, where addresses A0 to A7 represent the BIBs and addresses A8 to A9 the LIBs. The Bricks are controlled and monitored by sending serial commands to the BIB addresses A0 to A7. Similarly, Brick loads are initialised and monitored by sending serial commands to the LIB addresses A8 and A9. LIB addresses A8 and A9 control and monitor loads to Bricks 1 to 4 and Bricks 5 to 8, respectively. The BLA mainly consists of an initialisation sequence, the Burn-in sequence and a stop sequence to end the Burn-in procedure and exit the program. The following sections present the BLA using

simplified flowcharts, which describe key aspects of the BLA functional design specification. The software was originally developed by Argonne National Laboratory (ANL) in 2006 for the version 6 Bricks [62]. In conjunction with various Test-stand and Burn-in station hardware upgrade campaigns [91], the software has undergone major revisions during the ensuing years for the utilisation of the current Wits and UTA Burn-in stations.

The following itemized description of the BLA is made with reference to the flowchart illustrated in Figure 4.21. The flow chart is also provided as subdivided figures for the Start, Main and Stop sequence in Figure F.6, Figure F.7 and Figure F.8, respectively:

- The initialization sequence commences with two serial port communication interfaces being initialised for communication from the PC to the MB and HV power supply. The identification numbers of the IBs are checked for errors followed by a user prompt to enter the desired load current of each Brick for the Burn-in procedure. Text files are created for logging data into a file directory entered by the operator on the front panel of the BLA. Each IB is associated with an address from A0 to A9, which is polled by the BLA and controlled by the MB. Once the Brick load current commands are received from the BLA, the load currents are set by the PIC firmware of the respective LIB in Subroutine 5. Subsequently, the Bricks are sequentially started in Subroutine 6 and the HV power supply is enabled at +200 VDC. Once complete, calibration constants are initialised for Brick measurements consisting of first-order polynomials. The time duration of the Burn-in procedure is captured by the operator before entering the main loop, as shown at the end of the flowchart. The initialise sequence is only executed once.
- The main sequence starts counting down the entered Burn-in time duration. The Burn-in procedure consists of a stacked sequence structure, which cycles through each of the Brick and HV measurements until the Burn-in time has expired. A cycle is incremented once all eight Brick measurements are completed. In Subroutine 3, Brick performance measurements are read at address x, followed by a conditional statement, which checks if the Brick tripped by comparing measurements to predefined values. In Subroutine 4, the load current is set for the specified Brick and can be changed during a Burn-in procedure.

In Subroutine 8, serial commands are sent from the BLA at address x to the respective Brick to read analog values (I_{in} , V_{in} , I_{out} , V_{out} , T_1 , T_2 , T_3). In Subroutine 7, if a Brick address is equal to 0–3, measurements are also taken at Address 8, representing LIB1, by sending serial commands to take analog measurements from the DLB1 (I_o , V_o). Similarly, load measurements are repeated for Brick addresses 4–7.

Once the measurements are read by the BLA, the values are conditioned in the software through calibration constants followed by logging measurements for analysis offline. The sequence of measuring a cycle of eight Bricks is repeated and the loop is exited once the Burn-in time has expired, followed by an entrance in the stop sequence, as shown at the end of the flowchart.

- The stop sequence disables the HV power supply and stops each of the eight Bricks one at a time. The serial ports are closed and reports are generated for data analysis offline. The stop sequence is only executed once.

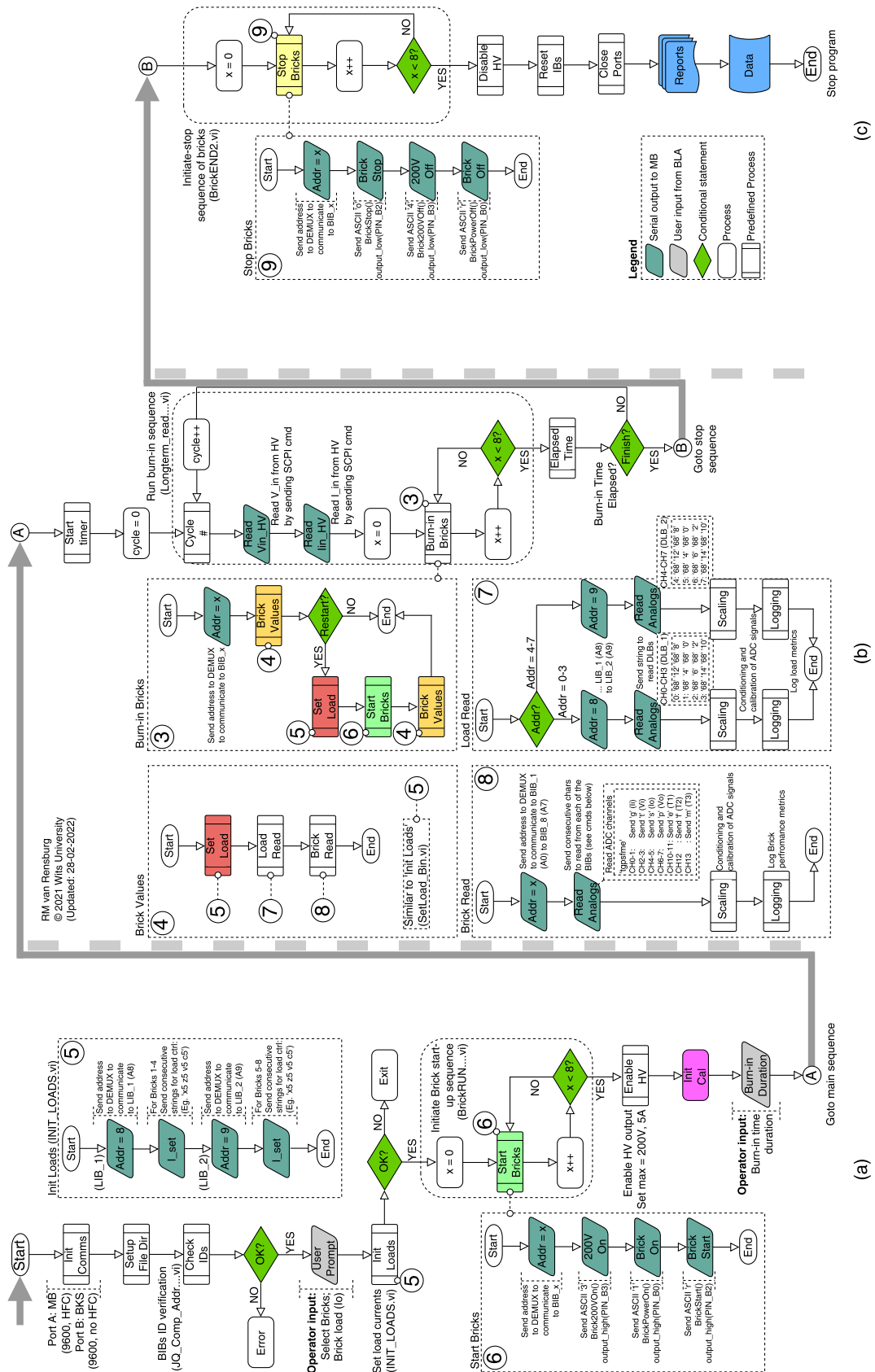


Figure 4.21: Simplified BLA represented as flowcharts describing (a) initialisation sequence (b) burn-in procedure sequence and (c) stop sequence. Due credit is given to Roger Van. Rensburg of the University of the Witwatersrand School of physics for creating this diagram.

Chapter 5

Phase-II Upgrade Brick Thermal Performance and Optimisation

The investigation of the Phase-II Upgrade Bricks thermal performance and its subsequent optimisation is presented in this chapter.

5.1 Baseline V8.1.0 Brick

The Baseline V8.1.0 Brick underwent two distinct tests, namely a thermal runaway test and an actively cooled temperature stability test. The thermal runaway test served to assess the Bricks thermal performance over the entirety of its possible temperature range. The lower bound of this range is determined by Bricks temperature at start-up. This temperature is dependent on the ambient temperatures as well as the temperature of the heatsink to which it is affixed. It is assumed that the Brick is in thermal equilibrium with the heatsink at start-up. The upper-bound, in contrast, is a fixed point determined by the Bricks Over-Temperature Protection (OTP) circuitry. This point is referred to as the OTP trip point and has a value of 70 °C, as per the specification sheet, for all V8 Bricks. The Brick was placed on to the Initial/Final test stand, with no active cooling present, with gap-pads having been inserted between the U1 controller chip, U2 MOSFET driver and the test stand and thermal paste suitably applied to the thermal interface of all thermal posts.

The test stand, in the case, functioned as a passive heatsink and was measured to be 17 °C at the start of testing ($t = 0$). This temperature was not selected (or controlled) but was rather the ambient temperature of the laboratory on that day and was deemed to be reasonable. This as the start temperature of the Brick has no affect on the temperature at which the Brick will initiate a trip. The Brick was then left to run, with a nominal load of 2.3 A applied, until the OTP circuitry initiated a trip. Three temperature measurements were recorded. These are the T2 and T3 inbuilt thermistor measurements as well as as an external thermocouple measurement. The locations of the T2 and T3 thermistors on the Brick were indicated in Figure 3.21 whereas the thermocouple was located adjacent to the transformer core. For this test the top of the transformers magnetic shield was removed to allow access to its core. As can be seen in Figure 5.1, a trip occurred at a

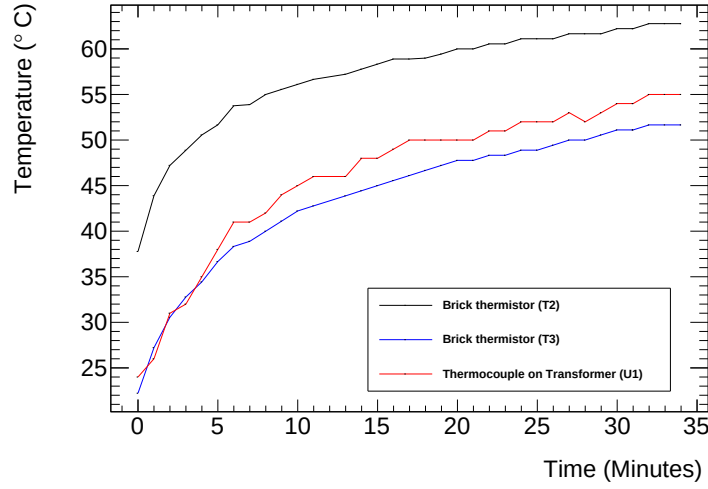


Figure 5.1: Thermal profile of the Baseline V8.1.0 Brick from start up until initiation of its Over Temperature Protection.

recorded thermistor (T2) temperature of 62 °C. It took 34 minutes under these operating conditions for a trip to occur which only provides insight into the heat capacity of the test stand and is of no interest in this test.

The discrepancy between the trip set point (70°C as per the specification document) and the actual measured trip point (62°C) for the single thermal runaway test shall be considered below. The temperature protection circuitry of the Brick and the temperature measurement T2 both make use of the same voltage divider circuit as pictured in Figure 5.2. A thermistor (labelled R1 for convenience) is the functional component that allows the voltage divider to produce an analog signal that is proportional to the temperature of the thermistor and thus the location on the Brick where it is located. A Negative Temperature Coefficient (NTC) thermistor is employed which has a resistance characteristics that its resistance value decreases as its temperature rises.

The voltage divider equation gives the following expression for the voltage on the U1 THERM pin ($V_{THERM} = V_{Out}$) in Figure 5.2:

$$V_{Out} = V_{In} \left(\frac{R2}{R1 + R2} \right) \quad (5.1)$$

where $V_{In} = 5\text{ V}$, $R1 = 10\text{K } \Omega$ at 25°C and $R2 = 680\text{ } \Omega$.

The temperature of the NTC is determined from its resistance using the Steinhart-Hart equation with one parameter. The reason for using this single parameter formula is that NTC thermistor manufacturers provide a β value at a temperature of 25°C. That is, for thermistor R1 we have that:

$$R = R_{ref} \exp \left[\beta \left(\frac{1}{T} - \frac{1}{T_{ref}} \right) \right] \quad (5.2)$$

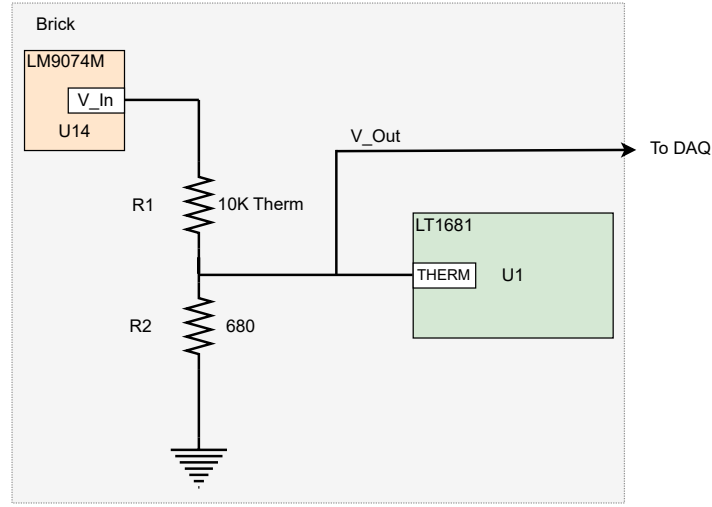


Figure 5.2: Functional block diagram of the Phase-II Upgrade Brick temperature protection circuitry which utilizes a standard voltage divider circuit.

Where R_x is the thermistor resistance at temperature T_x , expressed in Kelvin, and β is a constant representing the relationship between the resistance and temperature of an NTC thermistor provided by the manufacturer.

Let us first calculate the required thermistor temperature to initiate a Brick trip under nominal conditions. The nominal voltage required on the THERM pin of the LT1681 (U1) required to initiate a trip is $V_{THERM} = 1.25\text{ V}$ as per its specification sheet. Given this we can calculate the resistance of the thermistor using equation 8.1 as follows:

$$R1 = R2 \left(\frac{V_{In} - V_{Out}}{V_{Out}} \right) = 2040.0\ \Omega \quad (5.3)$$

As per equation 8.2 and given $\beta_{25-85^\circ\text{C}} = 3380$, $T_0 = 298.15\text{ K}$ and $R_0 = 10000\ \Omega$, the values of which coming from the R1 specification sheet, we have that:

$$T_{THERM} = \frac{\beta T_{ref}}{T_{ref} \ln\left(\frac{R_{THERM}}{R_{ref}}\right) + \beta} = 345.88\text{ K} = 72.73^\circ\text{C} \quad (5.4)$$

Based on the above calculation it is apparent that a nominal trip should not occur at the Over Temperature Protection (OTP) trip point stated in the Brick specification sheet (70°) but rather at 72.73° . Although this finding is of interest, as it suggests that the resistance of R2 needs to be changed so that the actual nominal and stated OTP trip point are identical, it does not in an of itself provide any evidence as to why a trip at 62° occurred.

It is known that the stated values of electronic components be they a voltage or resistance, as in this case, have an associated tolerance (error). This tolerance is generally provided in the specification sheet of the component by any reputable manufacturer. These tolerances can be expressed as a normalised Gaussian probability density function $\rho(x)$ with mean (μ) and standard deviation (σ):

$$\rho(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{(x-\mu)^2}{2\sigma^2}} \quad (5.5)$$

With the probability density function of the LT1681 THERM pin and of the voltage divider circuit denoted by ρ_{THERM} and $\rho_{V_{Out}}$, respectively. In order to produced these probability density functions we require both their standard deviation and mean. As per its specifications sheet we have that the LT1681 nominally initiates a trip at $V_{THERM} = 1.25 \text{ V}$, therefore $\mu_{THERM} = 1.25 \text{ V}$. This pin has a 4% tolerance which yields $\sigma_{THERM} = 0.05 \text{ V}$ [66].

The voltage divider circuit needs to be treated in a different manner as the tolerance of its output voltage is dependant on the tolerances of its constituent circuit elements. Namely, the tolerance of the R1 thermistor, R2 resistor, as well as the tolerance of the input voltage received from the LM9074M. These tolerances are provided in Table 5.1.

ID in Figure 5.2	Schematic ID	Part number	Tolerance (%)
Same	U14	LM9074M [92]	$\sigma_{V_{In}} = 3$
R2	R10	RC0603FR-07680RL [93]	$\sigma_{R2} = 1$
R1	R78	NCP18XH103J03RB [94]	$\sigma_{R1} = 5$

Table 5.1: Tolerances of the components in Figure 5.2 as per their specification sheets.

Consider a function $f = f(\alpha_1, \alpha_2, \dots, \alpha_n)$ of one or more parameters α_i , each with a corresponding tolerance σ_i . Assuming that these parameters are normally distributed and that the tolerance (errors) are not correlated we have that:

$$\sigma f = \sqrt{\sum_i \left(\frac{\partial f}{\partial \alpha_i} \sigma_i \right)^2} \quad (5.6)$$

Therefore, the propagated error of the voltage divider circuit (V_{Out}) denoted $\sigma_{V_{Out}}$ can be expressed as:

$$\begin{aligned} \sigma_{V_{Out}} &= \sqrt{\left(\frac{\partial V_{Out}}{\partial V_{In}} \sigma_{V_{In}} \right)^2 + \left(\frac{\partial V_{Out}}{\partial R1} \sigma_{R1} \right)^2 + \left(\frac{\partial V_{Out}}{\partial R2} \sigma_{R2} \right)^2} \\ &= \left(\frac{R2}{R1 + R2} \sigma_{V_{In}} \right) \oplus \left(\frac{-V_{In} R2}{(R1 + R2)^2} \sigma_{R1} \right) \oplus \left(\frac{V_{In} R1}{(R1 + R2)^2} \sigma_{R2} \right) \end{aligned} \quad (5.7)$$

Where $\oplus$ indicates addition in quadrature.

To determine the values of the above partial derivatives we require the nominal values for V_{In} , $R1$ and $R2$. We know that $R2 = 690.0\Omega$ and $V_{In} = 5.0V$ but the value of resistor $R1$ is temperature dependant as it is a thermistor. As we are investigating a trip at 62°C the nominal value of $R1$ at this temperature needs to be calculated using Equation 5.2:

$$\begin{aligned} R1 &= R1_{ref} \exp \left[\beta \left(\frac{1}{T} - \frac{1}{T_{ref}} \right) \right] \\ &= 10000 \exp \left[3380 \left(\frac{1}{335.15} - \frac{1}{298.15} \right) \right] \\ &= 2850.64\Omega \end{aligned} \quad (5.8)$$

Therefore, for $R1 = 2850.64\Omega$, $R2 = 690.0\Omega$ and $V_{In} = 5.0V$ we have that:

$$\frac{\partial V_{Out}}{\partial V_{In}} = 0.1926 \quad (5.9)$$

$$\frac{\partial V_{Out}}{\partial R1} = -0.0003 \quad (5.10)$$

$$\frac{\partial V_{Out}}{\partial R2} = 0.0011 \quad (5.11)$$

Given the above values and that $\sigma_{R1} = 5\%$, $\sigma_{R2} = 1\%$, $\sigma_{V_{In}} = 3\%$ of their nominal values Equation 5.7 yields:

$$\begin{aligned} \sigma_{V_{Out}} &= \left((0.1926) \left(\frac{3}{100} \right) (5) \right) \oplus \left((-0.0003) \left(\frac{5}{100} \right) (2850.64) \right) \oplus \left((0.0011) \left(\frac{1}{100} \right) (680) \right) \\ &= 0.0489V \end{aligned} \quad (5.12)$$

The above standard deviations and means are presented in Table 5.2 alongside their associated probability density function for ease of reference.

Probability density function	Units (V)	
$\rho_{THERM}(V)$	$\mu_{THERM} = 1.25V$	$\sigma_{THERM} = 0.05V$
$\rho_{V_{Out}}(V)$	$\mu_{V_{Out}} = 1.25V$	$\sigma_{V_{Out}} = 0.0489V$

Table 5.2: $\rho_{THERM}(V)$ and $\rho_{V_{Out}}(V)$ associated means and standard deviations.

The probability density functions for the LT1681 THERM pin and voltage divider output circuit is shown in Figure 5.3.

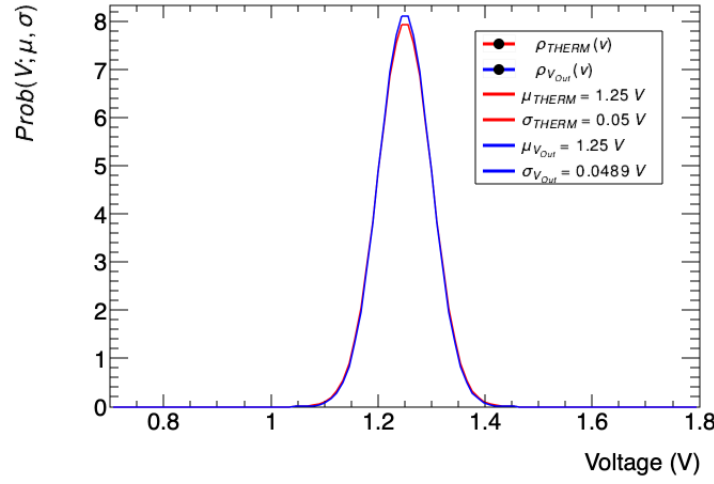


Figure 5.3: Probability density functions of LT1681 THERM pin (red) and voltage divider output circuit (blue).

The probability that the LT1681 will initiate a trip of the Brick due to an applied voltage to its LT1681 THERM pin that is 1σ (0.05 V) or more below the nominal trip point of THERM pin (1.25 V) is given by:

$$\begin{aligned}
 P_{THERM}(V < 1.20) &= \int_{-\infty}^{1.20} \rho_{THERM}(v) dv \\
 &= \frac{1}{\sigma_{THERM} \sqrt{2\pi}} \int_{-\infty}^{1.20} e^{-\frac{(v-\mu_{THERM})^2}{2\sigma_{THERM}^2}} dv \\
 &= \frac{1}{0.05\sqrt{2\pi}} \int_{-\infty}^{1.20} e^{-\frac{(v-1.25)^2}{2(0.05)^2}} dv \\
 &= 0.16
 \end{aligned} \tag{5.13}$$

Similarly, the probability that the voltage divider will output a voltage of 1.20 V or lower when the thermistor temperature is at 62 °C is given by :

$$\begin{aligned}
 P_{VOut}(V < 1.20) &= \int_{-\infty}^{1.20} \rho_{VOut}(v) dv \\
 &= \frac{1}{\sigma_{VOut} \sqrt{2\pi}} \int_{-\infty}^{1.20} e^{-\frac{(v-\mu_{VOut})^2}{2\sigma_{VOut}^2}} dv \\
 &= \frac{1}{0.0489\sqrt{2\pi}} \int_{-\infty}^{1.20} e^{-\frac{(v-1.25)^2}{2(0.0489)^2}} dv \\
 &= 0.15
 \end{aligned} \tag{5.14}$$

As $P_{THERM}(V < 1.20)$ and $P_{VOut}(V < 1.20)$ are statistically independent we have that

the probability that both the LT1681 will initiate a trip of the Brick due to an applied voltage of 1.20 V or lower to its therm PIN and that the voltage divider will output a voltage of 1.20 V or lower when the thermistor temperature is at 62°C is given by:

$$\begin{aligned} P(P_{THERM}(V > 1.20), P_{V_{Out}}(V > 1.20)) &= (P_{THERM}(V > 1.20))(P_{V_{Out}}(V > 1.20)) \\ &= (0.16)(0.15) \\ &= 0.02 \end{aligned} \tag{5.15}$$

Thermal images were taken every minute for the duration of the thermal runaway test so as to observe the development of possible hot-spots. A hot-spot, in this case, is characterized as a localized region of the Brick that exhibits a higher temperature in comparison to the mean temperature of the entire Brick.

Four of the thermal images taken at $t = 0, 14, 24$ and 34 minutes are presented in Figure 5.4. At $t = 0$ minutes, a uniform starting temperature of 17.2°C which is equivalent to that of the test-stand, to which it is affixed, can be observed. This temperature was not selected but was rather the ambient temperature of the laboratory on that day of testing and was deemed to be reasonable. The Brick was immediately subjected to an applied load of 2.3 A that was maintained for the duration of the test. These starting conditions are often referred to as a "cold-start".

At $t = 14$ minutes various hot-spots can be observed to have developed across the Brick with the majority of their locations being occupied by the power electronic components, as one would expect. The power received by a Brick from the off-detector bulk power supplies is not equal to that which it outputs to the front-end electronics that it services. That is, the Brick is not 100% efficient. Due to the law of conservation of energy the discrepancy between the input and output power needs to be accounted for. This lost electrical energy is converted into thermal energy due to various physical phenomena that occur each of which being dependant on the particular device that is generating the heat. Some of these phenomena will be addressed when considering the High-efficiency Bricks.

An important observation to be made is that the heat produced by a component (resulting in a hot-spot) is thermally conducted by the printed circuit board to adjacent components. This can be seen when comparing Figure 5.4 (b) and Figure 5.4 (c). This unwanted conduction of heat is problematic as the maximum operating temperatures of the adjacent components may be exceeded. Consequently, it is important that when a hot-spot is investigated that the offending source producing the heat must not be considered in isolation but rather it and all adjacent components should be considered. In the ten minutes that elapsed between the thermal images being taken not only has the maximum measured temperature increased from 48.4°C to 66.5°C the conduction of heat away from the various hot-spots can also be seen.

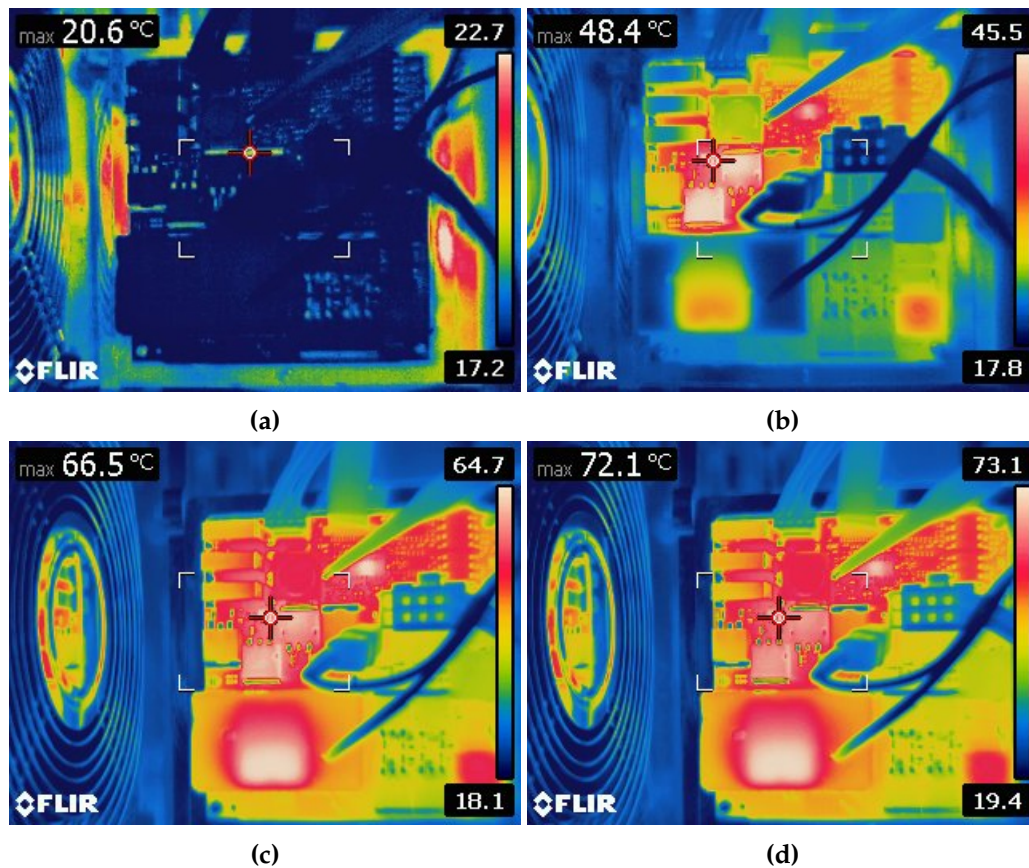


Figure 5.4: Thermal images of a V8.1.0 Brick under 2.3 A load taken at $t = 0$ minutes (a), $t = 14$ minutes (b), $t = 24$ minutes (c) and $t = 34$ minutes (d). It is important to observe the auto scale of the temperature gradient on the right hand side of the images.

Figure 5.4 (d) was taken at $t = 34$ minutes just prior to the Bricks over-temperature protection circuitry initiating a trip. The maximum temperature, as recorded by the FLIR-E63900 thermal camera, was 72.1°C which closely aligns with the temperature trip point of 72.3°C that was calculated in Equation 5.4. The aforementioned thermal camera has an accuracy of $\pm 2^{\circ}\text{C}$ for an ambient temperature range of 10°C to 35°C and an object temperature above 0°C both of which temperature ranges were met when the images were taken. The thermal cameras accuracy cannot account for the discrepancy between the recorded trip temperature and that recorded by the thermal camera. This independent thermal measurement when considered alongside the result obtained in Equation 5.15 provides sufficient evidence to conclude that the measured temperature of the Brick, at the moment of its trip, being 62°C was incorrect. Due to the small sample size any further deductions as to how this value may have arisen would be purely speculative.

When comparing the recorded temperature of Brick when it trips to the thermal image taken at the same time we are in-fact comparing two different but related thermal measurements. That is, the recorded temperature is the temperature of the thermistor itself whereas the thermal image measurement provides the highest temperature in its

field of view the location of which is indicated by a cross-hair in the image. The cross-hair is centred on the case of the T1 MOSFET, as seen in Figure 5.4 (d), thereby providing its case temperature.

The Baseline Brick temperature stability test was conducted following the thermal runaway test making use of the same V8.1.0 DUT. The primary purpose of this test was to provide a control to which all further thermal stability tests could be compared. Due to manufacturing inconsistencies at both the device and component level it is best practice to obtain an averaged thermal profile for a population of DUTs of the same type. Unfortunately, this was not possible for this DUT as only one was available at the time of testing.

The thermal stability test required that active cooling of the Brick be implemented. This necessitated a minor change to the apparatus introduced in subsection 4.1.3. In this test, and all temperature stability tests that follow, the Brick was affixed to a water-cooled cooling plate identical to those used within an fLVPS as pictured in Figure D.1. The cooling plate was maintained at a 15°C set point by an external water chiller. Sufficient time was given so as to allow the Brick to reach thermal equilibrium with the cooling plate, the coolant of which was maintained at 15°C set point by an external water chiller for the duration of the experiment.

A load of 2.3 A was applied to the Brick which was then run for 20 minutes. This duration was deemed acceptable as dynamic thermal equilibrium was attained after 5 minutes as indicated by the plateauing of all temperature measurements as can be seen in Figure 5.5. The thermal measurements taken mirrored those of the previous test with the further inclusion of another thermocouple measurement. The new thermocouple, labelled MOSFET (T2), had its probe directly attached to the T2 MOSFET case.

In Figure 5.5 it can be observed that the Brick thermistor (T2) temperature stabilised at $\mu_{\text{thermistor}} = 50.0^\circ\text{C}$ and that the thermocouple measurement of the T2 MOSFETs case stabilised at $\mu_{\text{thermocouple}} = 47.0^\circ\text{C}$. A discrepancy between these two values is expected as the Brick thermistor T2 is located on the opposite side of the PCB as compared to the primary side switching MOSFETs. This can be seen in Figure 4.4. However, what is unexpected is that the measured MOSFET case temperature is lower than the measured T2 thermistor temperature. This as the MOSFETs are the primary heat source on the Brick and no recorded temperatures on the Brick should exceed their case temperatures. The above statement is further supported as only a portion of heat produced by the MOSFETs is conducted through the PCB to the thermistor with radiation and convection losses occurring from the MOSFET cases and the PCB.

It is important that this discrepancy be investigated as the Brick thermistor (T2) temperature measurement is a key thermal performance metric. The discrepancy of 3.0°C could be accounted for by both the accuracy of the thermistors voltage divider circuit as well that of the thermocouple. The thermocouple is the easier of the two to address so this shall be done first. A Fluke 179 multimeter thermocouple was used the accuracy of

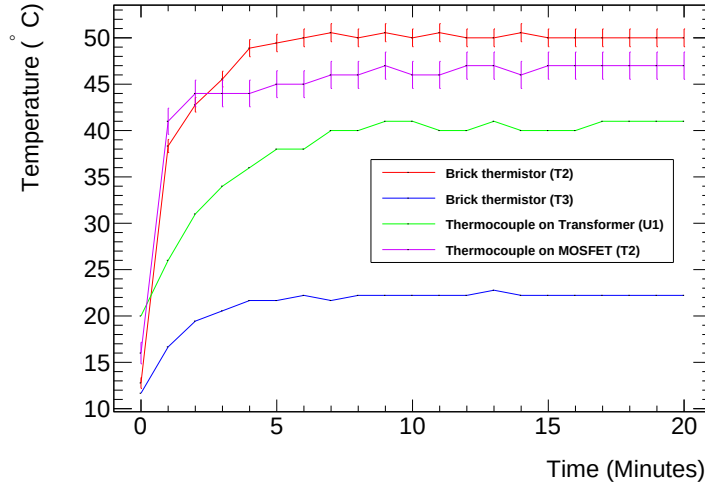


Figure 5.5: Thermal profile of the Baseline V8.1.0 Brick, when actively cooled, from start up until thermal equilibrium is reached.

the temperature measurement of which is $\pm(1.0\% + 10)$ as provided in its specification sheet [95].

Therefore, for a temperature measurement of 47.0°C we have that:

$$\sigma_{\text{Thermocouple}} = \frac{47}{100} + 10 = 1.47^\circ\text{C} \quad (5.16)$$

Interpreting the thermistor data is more involved as there are multiple sources of uncertainty in this measurement. Based on previous calculations we know that the temperature of the thermistor is related to its resistance by the following equation:

$$T_{\text{Therm}} = \frac{\beta T_{\text{ref}}}{T_{\text{ref}} \ln\left(\frac{R_{\text{Therm}}}{R_{\text{ref}}}\right) + \beta} \quad (5.17)$$

Where R_{Therm} is the thermistor resistance at temperature $T_{\text{Thermistor-measured}}$ and β is a constant representing the relationship between the resistance and temperature of an NTC thermistor provided by the manufacturer. R_{ref} is the resistance of thermistor at the reference temperature T_{ref} the values of which are also provided by the manufacturer. Looking at Equation 5.17 and the thermocouple specification sheet we can see that there are two contributions to the uncertainty in T_{Therm} . The first contribution comes from the β constant which has an uncertainty of 1%. The second contribution comes from the measured thermistor resistance ($R_{\text{Thermistor-measured}}$). Based on our previous encounter with these uncertainties in the preceding pages we know that this uncertainty does not only arise due to the thermistor itself but also from the voltage divider circuit that is used to measure its change in resistance as a function of temperature.

Equation 5.17 takes the following form when expressing R_{therm} in terms of the voltage divider output:

$$T_{Therm} = \frac{\beta T_{ref}}{T_{ref} \ln\left(\frac{R_2}{R_{ref}} \left(\frac{V_{In}-V_{Out}}{V_{Out}}\right)\right) + \beta} \quad (5.18)$$

Given Equation 5.18, we have that the uncertainty of the thermistor temperature measurement is:

$$\sigma_{T_{therm}} = \left(\frac{\partial T_{therm}}{\partial \beta} \sigma_{\beta}\right) \oplus \left(\frac{\partial T_{therm}}{\partial R_2} \sigma_{R_2}\right) \oplus \left(\frac{\partial T_{therm}}{\partial V_{In}} \sigma_{V_{In}}\right) \oplus \left(\frac{\partial T_{therm}}{\partial V_{Out}} \sigma_{V_{Out}}\right) \quad (5.19)$$

Where the respective partial derivatives of Equation 5.18 yield the following:

$$\frac{\partial T_{therm}}{\partial \beta} = \frac{\beta T_{ref}^2 V_{Out}}{V_{In} - V_{Out}} \frac{1}{(T_{ref} \ln\left(\frac{R_2}{R_{ref}} \frac{V_{In}-V_{Out}}{V_{Out}}\right) + \beta)^2} \quad (5.20)$$

$$\frac{\partial T_{therm}}{\partial R_2} = \frac{-\beta T_{ref}^2}{V_{In} - V_{Out}} \frac{V_{In}}{V_{Out}} \frac{1}{(T_{ref} \ln\left(\frac{R_2}{R_{ref}} \frac{V_{In}-V_{Out}}{V_{Out}}\right) + \beta)^2} \quad (5.21)$$

$$\frac{\partial T_{therm}}{\partial V_{In}} = \frac{-\beta T_{ref}^2 V_{Out}}{V_{In} - V_{Out}} \frac{1}{(T_{ref} \ln\left(\frac{R_2}{R_{ref}} \frac{V_{In}-V_{Out}}{V_{Out}}\right) + \beta)^2} \quad (5.22)$$

$$\frac{\partial T_{therm}}{\partial V_{Out}} = \frac{\beta T_{ref}^2}{V_{In} - V_{Out}} \frac{V_{In}}{V_{Out}} \frac{1}{(T_{ref} \ln\left(\frac{R_2}{R_{ref}} \frac{V_{In}-V_{Out}}{V_{Out}}\right) + \beta)^2} \quad (5.23)$$

Making use of Equation 5.19 and the values provided in Table 5.3 we are able to determine that the uncertainty in the Brick thermistor measurement, at the stable temperature of 50 °C, is:

$$\sigma_{T_{therm}} = 0.96 ^\circ\text{C} \quad (5.24)$$

The uncertainties in the Brick thermistor measurement ($\sigma_{T_{therm}}$) and in the thermocouple measurement ($\sigma_{T_{thermocouple}}$) calculated above are presented in Figure 5.5. It can be observed that at thermal equilibrium these two measurements are within approximately 0.6 °C at their 1 σ limits. This result indicates that the Brick thermistor temperature measurement is a reasonable analog to the case temperature of the Bricks switching MOSFETs (the greatest heat source) case temperatures and therefore can be confidently used as a thermal performance metric of the Brick.

	Value	Tolerance (1σ)	Description
R_2	680 Ω	1%	Voltage divider resistor R2.
R_{ref}	10 K Ω	-	Thermistor resistance when at T_{ref} .
T_{ref}	298 K	-	Thermistor reference temperature.
β	3380	1%	Thermistor β constant in range 25 – 85 °C
V_{In}	5 V	3%	Voltage divider input.
V_{Out}	0.70	0.05 V	Voltage divider output.

Table 5.3: Relevant constants for the calculation of the Brick thermistor uncertainty measurement [94].

5.2 Hybrid V8.4.2 Brick

Having established the thermal performance of the Baseline DUT the next step is to investigate the thermal performance of the variable DUTs and whether or not the variables introduced improve their thermal performance in comparison to that of the Baseline DUT. The on-Brick thermistor measurements will serve as the performance metric that will be used to compare the thermal performance of the DUTs.

The design variations and commonalities between the DUTs was succinctly illustrated in Figure 4.1. The Hybrid DUTs, as outlined in subsection 4.1.2, were the first to be investigated. The variable introduced in these DUTs was the targeted use of aluminium nitride (AlN) thermal posts in key locations as opposed to the sole use of aluminium oxide posts (Al_2O_3). The AlN posts which have a significantly higher thermal conductivity when compared to that of the Al_2O_3 posts, as can be seen in Table 3.4, were placed in specific locations to address localized hot-spots. Three Hybrid DUT types were created each with a unique distribution of thermal posts. The composition and distributions for the A-, B- and C-Type Hybrid DUTs thermal posts was outlined in Table 4.2 with the post ID locations illustrated in Figure 4.2.

The testing of the V8.4.2 Hybrid Bricks was immediately hampered by the A- and C-type Bricks experiencing mechanical damage to their thermal posts during transport resulting in some thermal posts becoming detached. This, although undesirable, did serve a purpose in that suitable changes were made to the packaging of the Bricks post-manufacturing thereby preventing a recurrence of such damage during pre- or main-production. The B-type Bricks were shipped in another package and arrived unscathed. It was decided that the B-type Hybrid Bricks would be tested with reproduction of the A- and C-types only to take place if unfavourable results were to be observed.

The four "identical" V8.4.2 B-type Bricks (B1, B2, B3, B4) underwent thermal stability testing as with the previous V8.1.0 Baseline Brick in which they were put under an applied load of 2.3 A and run until they reached thermal equilibrium with the actively cooled cooling plate as indicated by a plateauing thermal profile. Each test spanned 20 minutes with the tests commencing from a cold start.

There was however one development that took place during the course of this testing

		Temperature °C	
Brick Version	Applied load (A)	Coolant	Ambient
Baseline V8.1.0	2.3	15	24
B1 Type Hybrid V8.4.2	2.3	15	24
B2 Type Hybrid V8.4.2	2.3	15	24
B3 Type Hybrid V8.4.2	2.3	15	24
B4 Type Hybrid V8.4.2	2.3	18	24
All High-efficiency V8.4.2	2.3	18	22

Table 5.4: Thermal stability test experimental constants. Observe the change in coolant temperature from 15° C to 18° C. This change was made so as to reflect an approximate fLVPS cooling plate temperature as the cooling system became better understood during the course of experimentation.

as our understanding of the on-detector conditions of the fLVPS improved. It was found that the on-detector cooling plate temperature was not 15 °C, as previously thought, but was actually 18 °C. This was determined by making use of the TileCal DCS system to read-out the two external thermistors that are adjacent to the coolant inlet and outlet of the cooling plate for all TileCal fLVPS. The location of the thermistors can be observed in Figure 3.8. The discrepancy between the two temperatures is due to the fact that the fLVPS does not receive the coolant directly from the cooling loop, as pictured in Figure 2.18, but rather after the coolant has already passed through the associated Super-drawer removing heat from the front-end electronics and therefore increasing in temperature. This can be seen in Figure 2.17. Table 5.4 above provides all relevant experimental constants for the thermal stability tests.

The resultant thermal profiles are provided in Figure 5.6. The first observation to be made in the above thermal profiles is the separation of the T2 and T3 thermistor measurements with the T2 measurements always being higher which is entirely anticipated due to our understanding of the localized hot-spots on the Brick. All of the thermistor measurements have a smooth profile besides those of the B3 Hybrid Brick which exhibited anomalous transient behaviour at $t = 8$ minutes. A positive and negative temperature spike are observed in the T2 and T3 thermistor measurements, respectively. There is a slight "recovery" observed in both temperatures over the period of several minutes. At the time of data taking it was noted that the Brick was bumped in error. It was decided to present this data as the result is of particular interest due to the unanticipated inverse impact on the two thermal measurements. It is hypothesized that the Brick, although physically attached to the cooling plate, experienced separation of the thermal posts adjacent to the T2 thermistor and the cooling plate whereas the posts adjacent to the T3 thermistor were pressed into the cooling plate with more force. As the thermistors are located on "opposite" sides of the Brick a downward motion of one side would indeed cause the other side to raise resulting in a smaller gap at the thermal interface in the former and a larger gap at the thermal interface in the latter. This observed behaviour

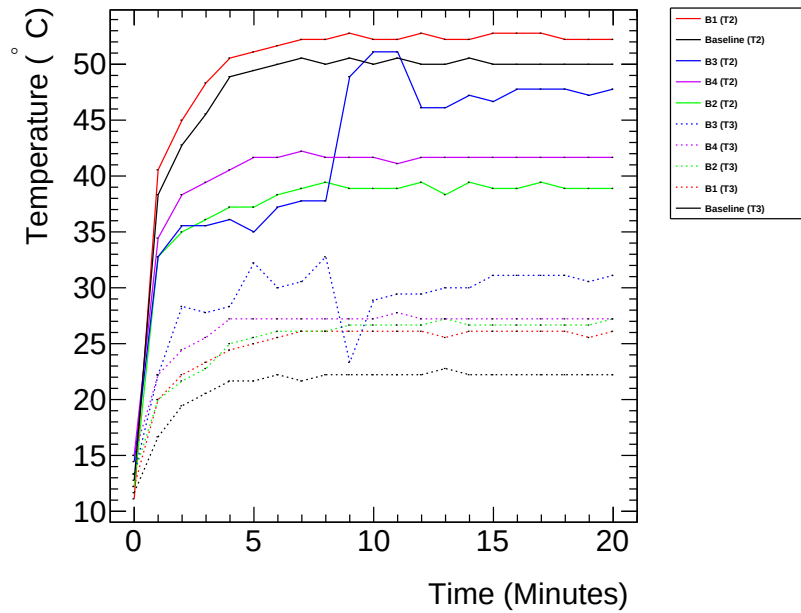


Figure 5.6: Thermal profile of the V8.4.2 Hybrid B Variant Bricks without gap-pads from start-up until thermal equilibrium is reached when actively cooled.

highlights the vulnerability of the Bricks thermal performance to mechanical displacement and therefore motivates the careful handling of the Phase-II fLVPS during assembly, handling, transport and installation.

It is anticipated that the B Variant Bricks T2 temperature would be lower than that of the Baseline Brick ($T = 50^{\circ}\text{C}$) as they employ AlN thermal posts, which have a greater thermal conductivity than that of the Al_2O_3 posts, to affix the T1/T2 Brick MOSFETs to the cooling plate. Brick B1 does not exhibit this behaviour, with a T2 thermistor measurement of $T = 52^{\circ}\text{C}$, although it is within approximately 2σ of the Baseline Brick as per Equation 5.24. A definitive statement as to the reason for this observed behaviour is not prudent as only one thermal profile was taken of the B1 Brick under these exact conditions. That being said, as the other B variant Bricks, including the anomalous B3, behaved as anticipated it can be loosely stated that another variable such as the pressure between the thermal posts and the cooling plate may account for this behaviour although this would constitute confirmation bias. Therefore, multiple thermal profiles would need to be taken to address this observation. This was not done the reason for which will be addressed in the Variant Hybrid Brick study that is to follow.

The B Variant Bricks T3 thermistor measurements are expected to be lower than those of the Baseline Brick, similarly to the behaviour observed in T2 thermistor measurements. The reason for this is that the L4 inductor, which is adjacent to the T3 thermistor, also makes use of an AlN thermal post instead of an Al_2O_3 post. However, this is not observed in Figure 5.6 as all B Variant Bricks measurements are above that of the Baseline Brick at thermal equilibrium. This behaviour may be attributed to inadequate thermal coupling

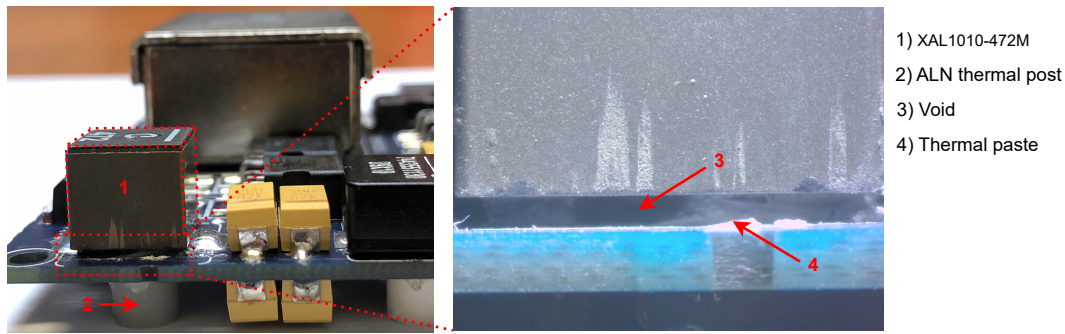


Figure 5.7: Image of a B-Type V8.4.2 Hybrid Brick indicated the location of the L4 inductor (XAL1010 [82]) (left) and its thermal interface with PCB (right).

of L4 inductors thermal post to the cooling plate due to a loose mounting bolt but as all of the B Type Bricks exhibit this increased temperature, albeit with a small sample size, it was decided to investigate this behaviour further.

When anticipating that the use of the *AlN* thermal post for the L4 inductor will reduce its operating temperature and therefore that of the T3 thermistor we are in fact making an assumption that the thermal conductivity of the post itself is the dominating characteristic affecting the Bricks thermal performance in the region surrounding the T3 thermistor. This assumption was implicitly made with the T2 thermistor measurement. In the case of the L4 inductor and T3 thermistor measurement doing so is not entirely appropriate due to the thermal interface between the top of the post and the component that it is responsible for cooling directly is different to that of the T1/T2 MOSFETs. Recall that there are two types of posts, namely metallized and non-metallized, as described in subsection 3.4.2. The distinction between the posts is also made in Table 4.2. The metallized posts allow for direct soldering of the component to their top surface whereas the non-metallized posts require a thermal interface medium (thermal grease) to be applied between the two. The MOSFETs adjacent to the T2 thermistor are soldered directly to their metallized *AlN* posts. The L4 inductor which is adjacent to the T3 thermistor is thermally coupled to its post with thermal grease as also described in subsection 3.4.2. Due to the above the heat generated by the components flows through paths with different thermal characteristics. The thermal interface between the L4 inductor and its thermal post is a new variable that warrants investigation.

An image of this thermal interface can be seen in Figure 5.7. Poor thermal coupling between the L4 (XAL1010) inductor and PCB/thermal post due to the presence of voids was observed. The poor coupling is a result of manufacturing considerations in that the footprint and case design of the XAL1010 made manual population of the component and application of thermal grease difficult and non-uniform with most components found to have significant voids in the thermal paste. Based on the above observations it was hypothesized that although a reduction of the T3 thermocouple temperature should

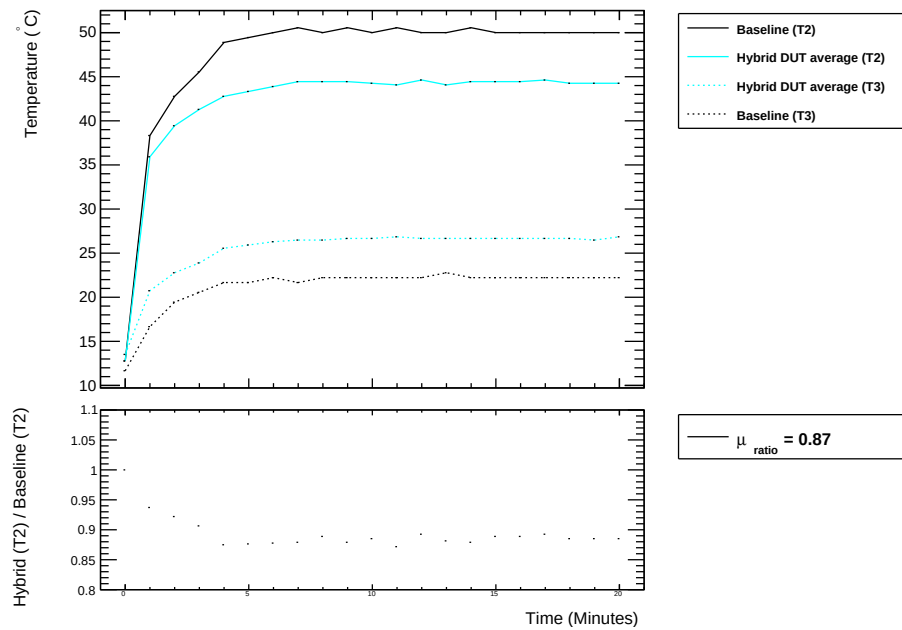


Figure 5.8: Thermal profiles of the averaged Hybrid B Variant Bricks, excluding the anomalous Brick B3, and the Baseline Brick without the use of thermal gap pads (top). Ratio of the averaged Hybrid B Variant Brick and the Baseline Brick T2 thermistor temperatures (bottom).

have been observed due to the change to an *AlN* post although this was not the case due to inadequate thermal coupling between the *AlN* post and the L4 inductor. To test this hypothesis the XAL1010 inductor was replaced with a new component in the High-efficiency Brick variant. The component, listed in Table 4.3, was selected as it has a form factor that should allow for improved thermal coupling to the thermal post. Further details on the new L4 inductor will be provided when considering the High-efficiency bricks which made use of them.

Figure 5.8 provides a comparison of the thermal profiles of the averaged Hybrid B Variant Bricks, excluding the anomalous Brick B3, and the Baseline Brick. This figure highlights the points made in the previous paragraphs regarding the notable separation between the T2 and T3 temperatures, the increased thermal performance of the Hybrid DUT in the region surrounding the T2 thermistor and the unanticipated lack of improvement in the region surrounding T3 thermistor. The ratio of the averaged hybrid B variant and Baseline Bricks T2 thermistor temperature measurements is provided. It can be seen that the Hybrid DUTs exhibited improved thermal performance with a $\mu_{Ratio} = 0.87$ over their entire averaged thermal profile.

It was well established in section 3.4.1 that the use of the gap-pads contributed to a significant reduction in the temperature of the IR2110s (U2) Field-Effect Transistor (FET) driver and the LT1681 (U1) controller chip, to which they were directly coupled to, as well as a global reduction in the temperature of the V7.5.0 Bricks. A figure illustrating

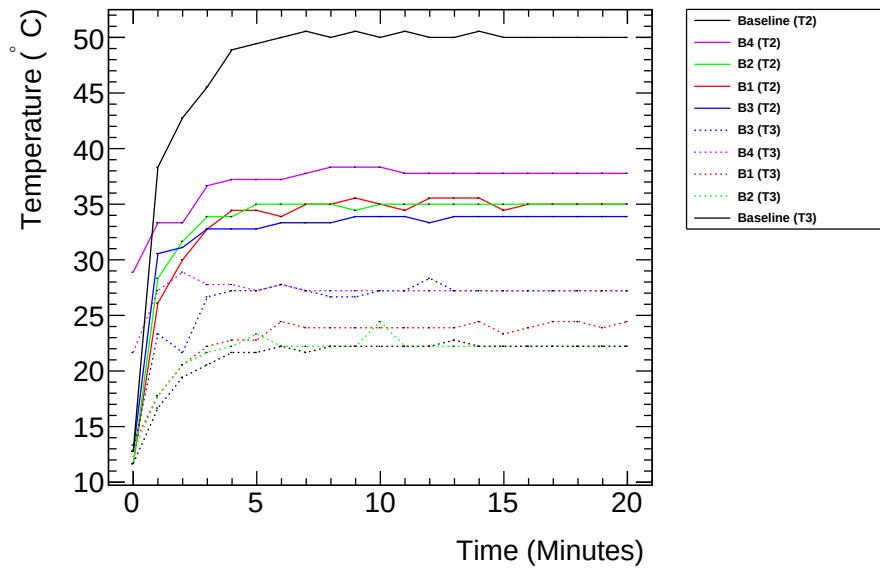


Figure 5.9: Thermal profile of the V8.4.2 Hybrid B Variant Bricks with gap-pads from start-up until thermal equilibrium is reached when actively cooled. The two gap pads are located between both the U1 controller chip, U2 MOSFET driver and the cooling plate.

the use of a gap pad was provided in Figure 3.19. As the Bricks final configuration when assembled within the Phase-II Upgrade fLVPS will make use of the thermal gap pads it was decided that the thermal performance of the Hybrid Brick variants should be investigated in said configuration.

The four B Variant Hybrid Bricks (B1, B2, B3, B4) underwent the same test procedure as with the previous set of tests but with the application of the gap pads which thermally couple the U2 FET driver and U1 controller chip to the cooling plate. The thermal gap pad information was provided in Table 3.4. All experimental constants were maintained as per Table 5.4.

The resulting thermal profiles for the four Bricks are presented in Figure 5.9. As with the previous tests a separation between the T2 and T3 thermistor temperature measurements with smooth profiles can be observed. Thermal equilibrium is reached between the Bricks and the cooling plate at around $t = 5$ minutes.

The anomalous transient behaviour of Brick B3 as observed at $t = 8$ minutes in Figure 5.6 can indeed be attributed to the Brick being bumped in err during testing as previously stated. This as the transient behaviour is not seen in Figure 5.9. On the contrary, B3 is observed to exhibit the best thermal performance of all of the hybrid DUTs during this round of experimentation.

Figure 5.10 provides a comparison of the thermal profiles of the averaged Hybrid B Variant Bricks, including the previously anomalous Brick B3, and the Baseline Brick. Note that thermal gap pads were used when obtaining these thermal profiles. This figure

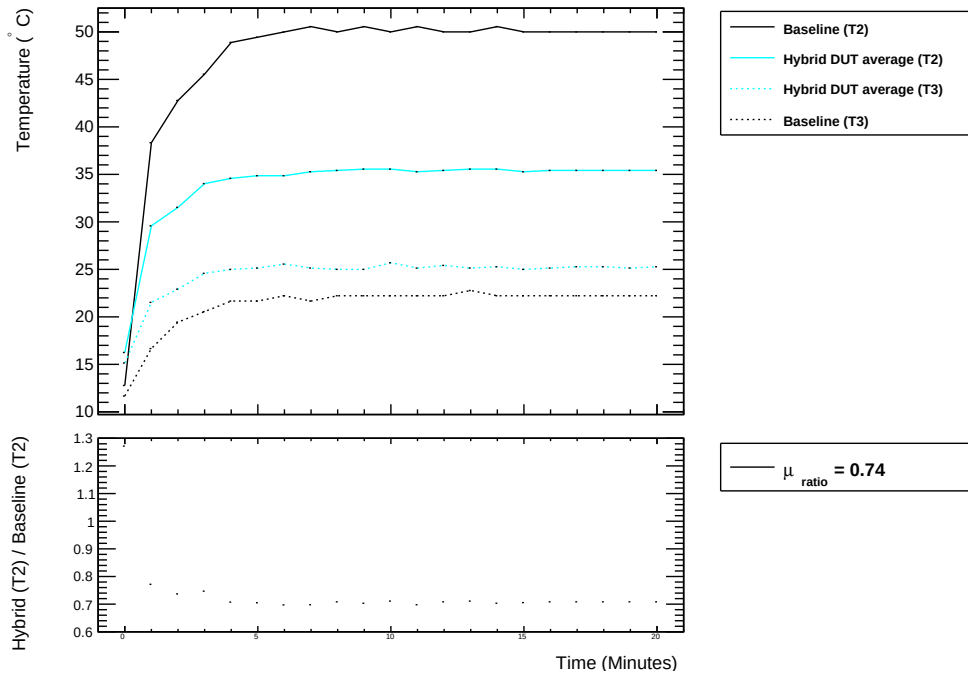


Figure 5.10: Thermal profiles of the averaged Hybrid B Variant Bricks and the Baseline Brick with the use of thermal gap pads (top). Ratio of the averaged Hybrid B Variant Brick and the Baseline Brick T2 thermistor temperatures (bottom).

highlights the points made in the previous paragraphs regarding the notable separation between the T2 and T3 temperatures albeit it with a smaller separation of approximately 10°C as opposed to 18°C in the non-gap pad configuration. This is indicative of an increased thermal performance of the Hybrid DUT in the region surrounding the T2 thermistor. The reason for this increased performance becomes apparent when looking at the underside of a Brick in Figure 4.4 (right). The Brick pictured is a High-efficiency variant but the locations of all components are identical for all DUTs referred to in the thermal studies. Observe the close proximity of the U1 controller chip (labelled 7) and the U2 MOSFET driver (labelled 8) to the T2 thermistor (labelled 4). The thermal gap pads when applied to U1 and U2 do not only provide direct cooling of the components but also serve as an additional route for the sinking of the heat produced by the T1/T2 MOSFETs (labelled 2) to the cooling plate thereby reducing the overall temperature of the hot-spot. A lack of improvement in the region surrounding T3 thermistor is again observed in the Hybrid B variant when gap pads are used. This can be attributed to a localised reduction in temperature surrounding the gap-pads location.

The ratio of the averaged hybrid B variant and Baseline Bricks T2 thermistor temperature measurements is provided in Figure 5.10 (bottom). It can be seen that the High efficiency DUTs exhibited improved thermal performance with a $\mu_{Ratio} = 0.74$ over their entire averaged thermal profile.

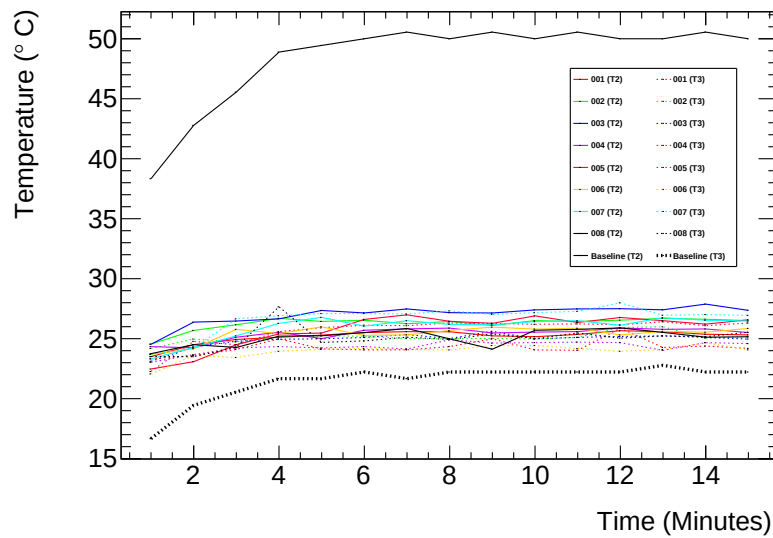


Figure 5.11: Thermal profile of the High-efficiency Bricks with gap-pads from start-up until thermal equilibrium is reached when actively cooled.

5.3 High-efficiency Bricks

The eight High-efficiency V8.4.2 Bricks (001 - 008) underwent the same procedure for their temperature stability test with an applied load of 2.3 A. Gap-pads were used with the cooling plate being maintained at the "new" temperature of 18 °C for all of these tests. The thermal profiles of the High-efficiency Bricks with gap-pads from start-up until thermal equilibrium is reached are provided in Figure 5.11.

The gap between T2 and T3 thermistor measurements as seen in the Baseline and Hybrid Brick DUTs is no longer present for all eight DUTs. This is primarily due to the decrease in the T2 thermal profiles which is itself attributed to the increase in efficiency of the new T1/T2 primary side switching MOSFETs (SIHFS9N60) as well as the use of thermal gap pads on the U1 controller chip and U2 MOSFET driver.

The High-efficiency DUTs averaged T3 thermal profile is very similar to that of the Hybrid B type DUTs with a mean value of 24° C and 25° C, respectively. As the uncertainty in the Bricks thermistor measurements is approximately 1° C, as previously calculated and presented in Equation 5.24, the two values are functionally indistinguishable. This observation supports the previously stated hypothesis on page 118. It stated that the thermal performance of the region surrounding the T3 thermistor was dominated not by the type of thermal post responsible for the direct cooling of the L4 inductor but rather by the thermal interface between the top of the thermal post and the bottom of the L4 inductor case. As the only variable between the High efficiency and Baseline Brick with regards to the L4 inductor and T3 measurement is that the L4 inductor of the

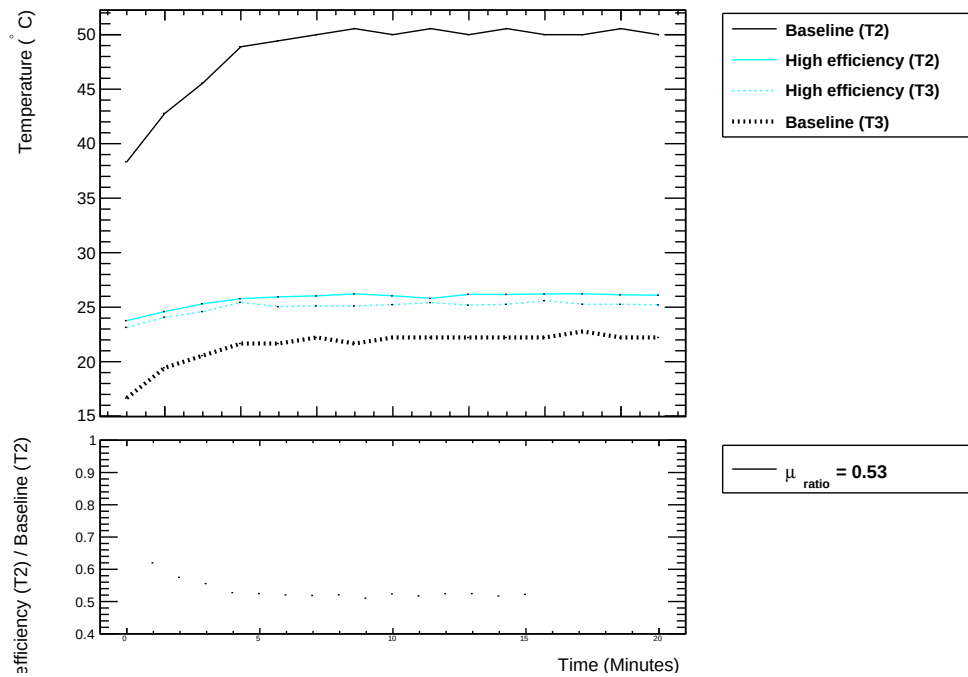


Figure 5.12: Thermal profiles of the averaged High efficiency Bricks and the Baseline Brick with the use of thermal gap pads (top). Ratio of the averaged High efficiency Bricks and the Baseline Brick T2 thermistor temperatures (bottom).

High-efficiency Brick, as shown in Figure 4.1, was changed of the L4 inductor to SML-744355113. The L4 inductor with an improved form factor (SML-744355113) is pictured in Figure 4.4.

The ratio of the averaged High efficiency and Baseline Bricks T2 thermistor temperature measurements is provided in Figure 5.12 (bottom). It can be seen that the High efficiency DUTs exhibited improved thermal performance with a $\mu_{Ratio} = 0.53$ over their entire averaged thermal profile.

5.4 Conclusions

DUT Type	μ_{ratio}
Baseline Brick	1
B1 Hybrid Bricks without gap pad	0.87
B1 Hybrid Bricks with gap pad	0.74
High efficiency Bricks with gap pad	0.53

Table 5.5: Devices Under Test (DUT) figures of merit and their values.

Chapter 6

Phase-II Upgrade Brick MOSFET Single Event Effect Radiation Hardness Certification and Subsequent Reliability Analysis

In this Chapter the radiation hardness certification and subsequent reliability analysis of the SIHFS9N60 power MOSFET, selected as a result of the preceding chapter, will be covered.

The aim of the first part of this chapter is to ascertain if the thermally motivated MOSFET is viable for use within the ATLAS radiation environment. If this is indeed the case the newly proposed MOSFET can be adopted into the final Brick design which would then allow for the use of Aluminium Oxide thermal posts in the South African production.

The second part of this chapter aims to quantitatively establish the reliability of a Phase-II Upgrade Brick in the newly proposed format, including the SIHFS9N60 MOSFET, so as to ensure that it equal to or greater than that of the legacy Brick designs. This as the impact of the fLVPS Brick on detector performance can then be deemed to be minimal.

6.1 High Efficiency Metal-Oxide Semiconductor Field-Effect Transistor Single Event Radiation Hardness Certification

The DUTs motivated by the thermal performance and optimisation studies namely SIHFS9N60 the Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET) were irradiated with a mono-energetic 200 MeV proton beam with a flux of 3×10^8 p/cm²/s until a fluence of 1.59×10^{12} p/cm² was reached (pre 2023 Radiation Tolerance Criteria). Recall that the ATLAS RTC were discussed in section 3.1.1. It should be noted that the RTC for the Long-Barell (LB), which has a higher fluence requirement, is used. This as components that pass the SEE irradiation certification for the LB can also be used in the Extended-Barrel (EB) thereby allowing for a single Phase-II Upgrade Brick to be

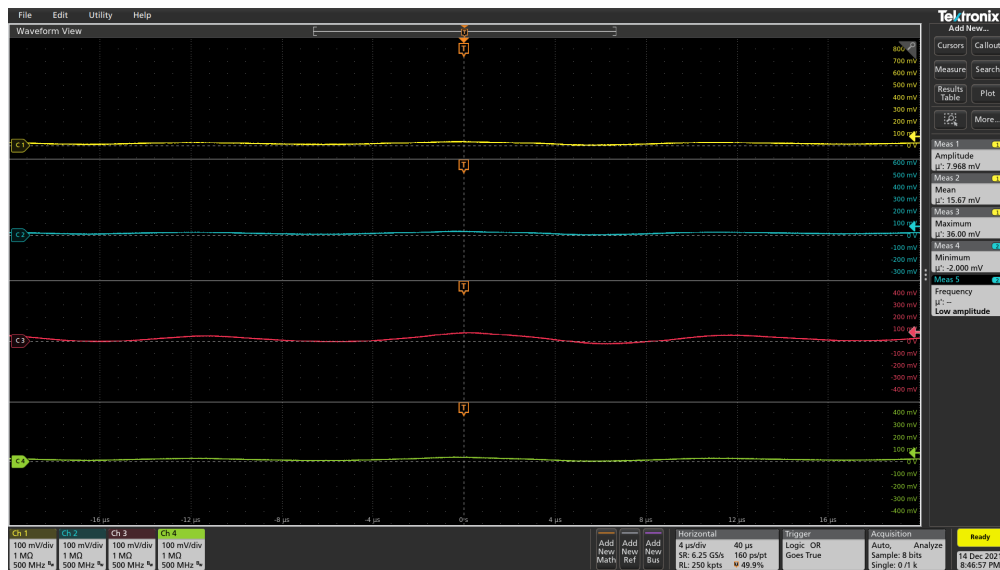


Figure 6.1: Oscilloscope screenshot of the four DUTs undergoing irradiation. Only small fluctuations indicative of electronic noise are present.

produced for the entire detector. This reduces manufacturing cost and complexity. The irradiation was subdivided into four runs with the total required fluence equally shared amongst the runs with a power cycle of the test PCB taking place between runs to assess the performance of the DUTs which may have experienced damage that only presents itself from start-up.

The SEE irradiation was concluded with no SEBs having been observed (neither destructive nor non-destructive). A screenshot of the oscilloscope is provided in Figure 6.1 with only small fluctuations indicative of electronic noise being present.

6.2 Phase-II Upgrade V8.6.1 Brick Reliability Analysis

We begin the analysis by simplifying the functional block diagram of a Brick provided in Figure 3.23. The simplified reliability circuit shown in Figure 6.2 is not a functional circuit, but is sufficient for the purposes of reliability calculations. It contains the critical components in the Brick, as previously determined in the V7.5.0 reliability analysis, where it is assumed that a failure of any of the primary components used in the forward converter portion of the circuit will result in a catastrophic failure.

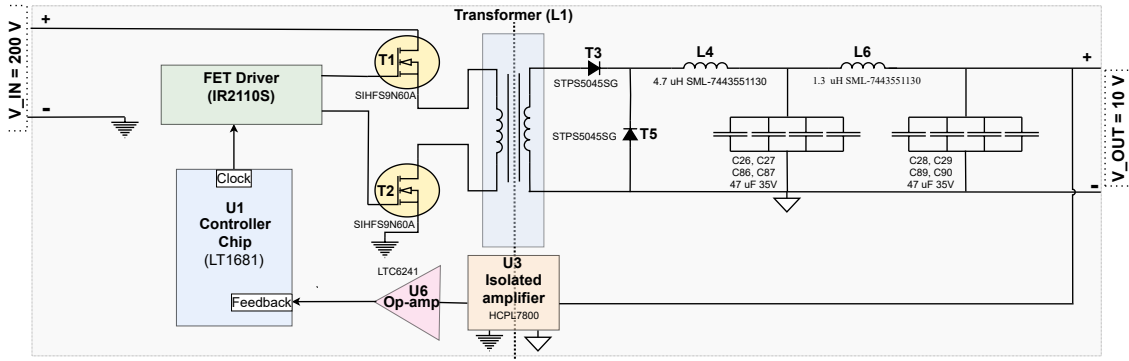


Figure 6.2: V8.6.1 Brick simplified reliability analysis circuit diagram. Note that this is not an equivalent circuit.

A signal flow drawing for the simplified reliability circuit is shown in Figure 6.3. It is assumed that any failure of the components shown will open the signal flow loop and cause a failure of the Brick. According to Equation 3.2 and the signal flow diagram in Figure 6.3 we have that:

$$\begin{aligned}
 \lambda_{Brick} &= C_i \sum_{i=1}^n \lambda_i \\
 &= 2\lambda_{Power\ MOSFET} + 2\lambda_{Schottky\ rectifier} + \lambda_{4.7\ uH\ Inductor} \\
 &\quad + 8\lambda_{Tantalum\ capacitor} + \lambda_{1.3\ uH\ Inductor} + \lambda_{Isolation\ amplifier} \\
 &\quad + \lambda_{Op-amp} + \lambda_{Controller\ chip} + \lambda_{MOSFET\ driver}
 \end{aligned} \tag{6.1}$$

where n is the total number of component types considered and the co-efficient c_i represented the number of i -th components considered.

It is important to note the omission of the L1 transformer in the reliability circuit and associated failure rate equation. This is due to no failures of this custom transformer having ever been observed thereby having an effective failure rate of $\lambda_{Transformer} = 0$ for all time t .

In addition to the forward converter electronics eight tantalum capacitors are included on the secondary side as these components were found to have the lowest reliability in the previous analysis. These capacitors exhibit two distinct failure modes, one being as an open-circuit and the other as a closed circuit. The intermediate case where the component continues to operate but with significantly different performance is not considered here. Large capacitor values are required in the forward converter necessitating connections of multiple capacitors in parallel. The way in which these components are connected is important when considering their failure modes. If a single capacitor fails as an open circuit, the performance of the circuit may be diminished but the circuit may not fail catastrophically. However, if a single capacitor fails as a short circuit, then

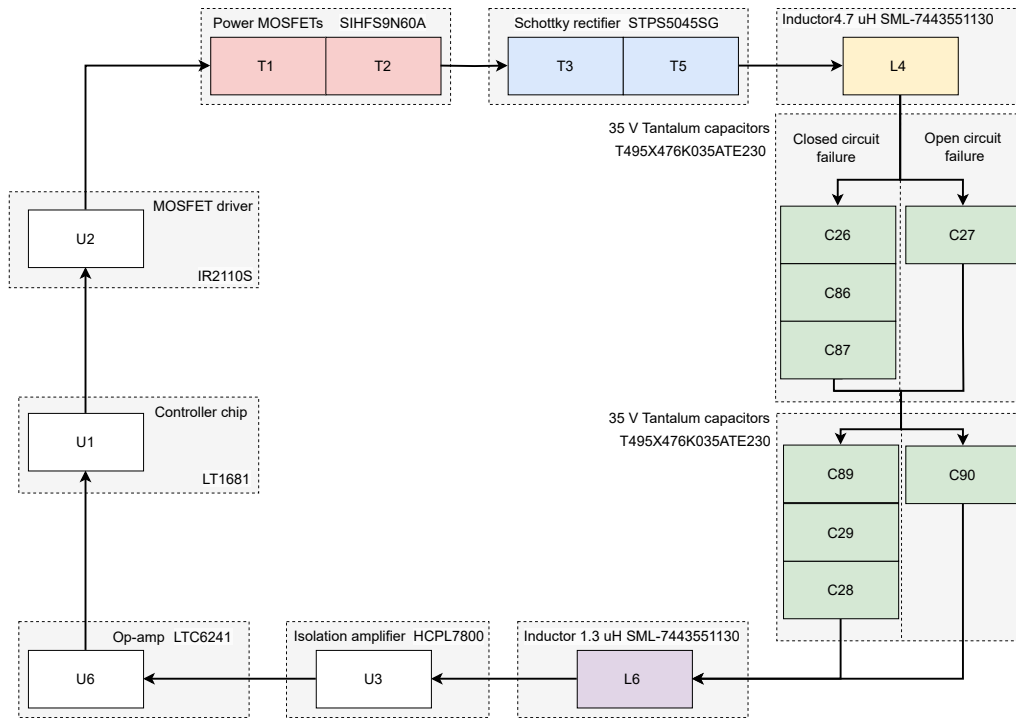


Figure 6.3: Reliability block diagram corresponding to the V8.6.1 Brick simplified reliability analysis circuit diagram.

having multiple capacitors in parallel is of no significance. Generally, tantalum capacitors fail most of the time as short circuits and sometimes, as open circuits. A weighting function is added to the capacitor failure rate to account for this behaviour. Using the FITS data, when a tantalum capacitor fails, we will assume that $\frac{1}{4}$ of the time it fails as an open circuit, while $\frac{3}{4}$ of the time it fails as a short circuit. This assumption is based on operational experience and takes the form of an additional coefficient, which is multiplied by the original c_i of $\lambda_{Tantalum\ capacitor}$. This coefficient is $\frac{3}{4}$ yielding a final $c_i = \frac{24}{4}$.

In the V6.5.4 Brick design, many of the tantalum capacitors were operated very close to their maximum rating (15V operation, 20V rating.) In the V7.5.0 and V8.6.1 Brick design tantalum capacitors with a rating of 35V for 15V operation were selected. The FIT value of a Tantalum capacitor is heavily influenced by the difference between its rated voltage and the operating voltage. This baseline value needs to be de-rated to take into account not only the voltage considerations but also the operating temperature of the capacitors. This process can be undertaken using the failure rate model provided by the capacitor manufacturer and implemented in the form of a FIT calculator the graphical user interface of which is shown in Figure 6.4. In this figure it can be observed that the capacitor type was set to a $47\ \mu F$ Tantalum (solid chip) with a rated voltage of 35V and a maximum operating temperature of $125^\circ C$ as per the manufacturers specifications sheet. The operating voltage and temperature was set to 15V and $37^\circ C$ which were selected as worst case values based on experience. The calculator yielded a FIT value of

Figure 6.4: KEMET FIT calculator graphical user interface.

Circuit reference	Manufacturer part number	FIT (failures/10 ⁹ hr at 60% CL)	MTTF (Hours)	MTTF (Years)
U1	LT1681	6.04 [96]	165 562 913	18 900
U2	IR2110S	3.01 [97]	332 225 913	37 925
U3	HCPL7800	18.0 [98]	55 555 555	6 242
U6	LTC6241	9.17 [99]	109 051 254	12 449
T1, T2	SIHFS9N60A	0.227 [100]	4 405 286 343	502 886
T3, T5	STPS5045SG	0.476	2 100 840 336	239 822
L4	7443551470	0.75	1 333 333 333	152 207
L6	7443551130	0.75	1 333 333 333	152 207
C26, C27	T495X476K035ATE230	5.03*	198 807 157	22 694
C28, C29	-	-	-	-
C86, C87	-	-	-	-
C89, C90	-	-	-	-
System prediction		51.31	19 489 378	2225

Table 6.1: Reliability data for the critical components of the Phase-II Upgrade Brick. *The FIT value of the tantalum capacitors provided incorporates voltage de-rating and is calculated using the KEMET FIT calculator. Note that a year is assumed to have 365 days.

Brick version	MTTF (Years)	Failure rate (Bricks per year)	
		Predicted	Observed
Previous reliability analysis			
V6.5.4	165.17	12.4	5.2*
V7.5.0	406.92	5	2
Current reliability analysis			
V8.6	2225	1	-

Table 6.2: Predicted and observed failure rates of the V6.5.4, V7.5.0 and V8.6 fLVPS Bricks without the application of an ad-hoc correction factor. No observed rates are available for the V8.6 Brick as they have not operated within the TileCal at an appreciable number as only 8 Bricks have been used on-detector to power the TileCal demonstrator module. Nevertheless, no failures of V8.6 Bricks have been observed on-detector.

5.03. This FIT value as well as all other relevant values, as taken from the manufacturers specification sheets, are Table 6.1. Inputting the data provided in Table 6.1 into From Equation 6.1 yields a MTTF = 2225 years for the system (V8.6.1 Brick simplified reliability analysis circuit diagram) in Figure 6.3.

The MTTF for a single Brick is found to be 2225 years. Assuming that the TileCal is fully populated having a population of 2048 Bricks, this gives an estimated failure rate per year of:

$$\text{Estimated failure rate}_{V8.6} = 2048/2225 \approx 1 \text{ Brick/year} \quad (6.2)$$

Recall that the previous reliability analysis was used to predict the reliability of the v7.5.0 Brick prior to it replacing the V6.5.4 Bricks which were on-detector at the time. The methodology used above when applied to the legacy V7.5.0 and V6.5.4 Bricks was found to over-estimate the Bricks annual failure rate [86]. The predicted and observed failure rates of these Brick versions are provide alongside the predicted failure rate of the V8.6 Brick in Table 6.2. Up to this point the annual failure rate has assumed that the Bricks operate continuously throughout the year. As we know, the ATLAS detector does not operate (take actual data) year round due to the Year End Technical Stop (YETS) which accounts for approximately two months per year. The previous analysis assumed that the Bricks were offline for YETS and therefore saw fit to scale the observed failure rates by adding an additional 2 months weighting of the the failures to the observed failure rate*. Although at face value this makes sense it is in fact an incorrect assumption. This as although the detector is not taking in the case of the TileCal the low-voltage system is kept on for the majority of YETS as repairs to the front-end electronics need to be validated and in general perturbing the system in any way, including what would essentially be a power cycle of the entirety of the TileCal, is discouraged. The observed failure rates stated in Table 6.2 are based on this assumption. However, this assumption will not be made in the analysis of the Phase-II Upgrade Bricks based on opertional experience.

Brick version	Year	Number of failures observed
V6.5.4	2009	4
	2010	4
	2011	5
V7.5.4	-	2

Table 6.3: Summary of the V6.5.4 Bricks on-detector failures during the first three years of operation as well as the failures of the V7.5.0 bricks during their first year of operation. The number of V6.5.4 Brick failures were sourced from the previous reliability analysis whereas the V7.5.0 Brick failures were sourced from the TileCal operations team.

As seen in Table 6.3, the previous reliability analysis over estimated the V6.5.4 Bricks annual failure rate when using the current form above. Due to this the analysis employed a statistically motivated ad-hoc correction factor (ξ) whose purpose is to bring the predicted and observed failure rate of the V6.5.4 Brick into agreement.

We have that:

$$\xi = \frac{\text{observed failure rate}}{\text{predicted failure rate}} \quad (6.3)$$

The statistical analysis was predicated on the assumption that its accuracy is dependant on the total number of failure instances (the size of the dataset). As this analysis employs the same methodology and it too has a small dataset the same statistical motivation will be made here. This is further supported as the Bricks are iterative in nature with substantial commonality between the V7.5.0 and Phase-II Upgrade Bricks. The recorded failure instances for both the V6.5.4 and V7.5.0 Brick are provided in Table 6.3.

The correction factor applied to the V7.5.0 Brick reliability analysis was $\xi_{V7.5.0} = 0.42$. This factor was calculated using Equation 6.3 and the actual versus the predicted failure rate of this Brick version. The facator was then applied to the V7.5.0 Bricks initially predicted failure rate to obtain the final predicted failure rate provided in Table 6.2. This factor cannot be applied to the predicted failure rate of the V8.6 Brick as there were substantial design changes between the V6.5.4 and V8.6 with most of these taking place in the V7.5.0 Brick as expanded upon in section 3.4.1 and section 3.4.1.

Therefore, the same methodology needs to be applied to the predicted versus actual failure rate of the V7.5.0 Brick to obtain the correction factor for the V8.6 Brick using Equation 6.3:

$$\xi_{V8.6} = \frac{\text{observed failure rate}}{\text{predicted failure rate}} = \frac{2}{5} = 0.4 \quad (6.4)$$

Given the failure rate predicted in eq:V8.6 failue rate pre-correction this yields a final predicted value of the V8.6 Bricks annual failure rate:

$$\text{Estimated failure rate}_{V8.6} = 0.4(1) = 0.4 \quad (6.5)$$

6.3 Conclusions

The Single Event Effect irradiation hardness certification of the SIHFS9N60 power MOSFET was successfully concluded at the PSI Proton Irradiation Facility and can than therefore be used in the Phase-II Upgrade Bricks allowing for their improved thermal performance as presented in section 4.1. This finding therefore allows for the use of Aluminium Oxide thermal posts in the South African Brick production as was motivated in subsection 4.1.1.

A subsequent reliability analysis was conducted on the V8.6.0 fLVPS Brick that includes the newly certified radiation hard SIHFS9N60 power MOSFET. The final estimated failure rate of 0.4 Bricks per year means that 4 Bricks can be expected to fail over the entire operation lifetime of the HL-LHC (10 years). This conclusion although encouraging does not take into account any random occurrences during this lifetime such as coolant leaks (unlikely as explained in section 1.4.2), mechanical damage during fLVPS assembly or during YETS as the fLVPS needs to be removed to access a modules front-end electronics. The impressive reliability exhibited by the V7.5.0 Brick is not only dependant on the component system FIT values but also implicitly included the impact of a robust Quality Assurance (QA) procedure that was applied to all of the V7.5.0 Bricks prior to their installation within the TileCal. As such, for the estimated failure rate calculated above to be true a similar QA procedure must be implemented on the Phase-II Upgrade Bricks.

Chapter 7

Phase-II Upgrade fLVPS Brick Burn-in Station Commissioning

In this chapter commissioning of the custom Burn-in Station for the finger Low-voltage Power Supply Bricks will be presented.

7.1 Burn-in Station Preliminary Commissioning

Preliminary commissioning begins with a visual inspection of all safety-critical hardware. Particular emphasis is placed on the temperature control system and all electrical connections due to the inherent danger posed by their close proximity. This process consists of a review of all coolant pipe joints, coolant levels within the water chiller, electrical and thermal insulation of the cooling plates, grounding of the test-bed, inspection of all cable connections and the PCBs to which they are connected, and ensuring that the mica films located between the dummy load power MOSFET tabs are correctly affixed. It was found that the thermostats located above the dummy load MOSFETs, which act as inbuilt thermal protection circuitry, have a propensity to trip during normal operation. As a result, the thermostats were replaced with an identical package with a trip point of 130 °C, as opposed to the previous thermostats, which had a trip point of 110 °C. The maximum allowable MOSFET junction temperature was taken into account when making this design change.

Thermography was used as a part of the commissioning process due to its ability to provide a macroscopic view of the thermal behaviour of the Burn-in station. The findings of the thermal review were corroborated by the use of an external thermocouple. Key areas such as the dummy load power MOSFET and the primary-side switching MOSFETs of the LVPS Bricks were reviewed with their operating temperatures being measured at 30.2 °C and 62.12 °C, respectively. The cooling plates were found to be at 38 °C (Figure 7.1, bottom-right) which was 2.0 °C lower than the temperature setpoint of the water chiller. This deviation will be taken into account when applying the Burn-in procedure.

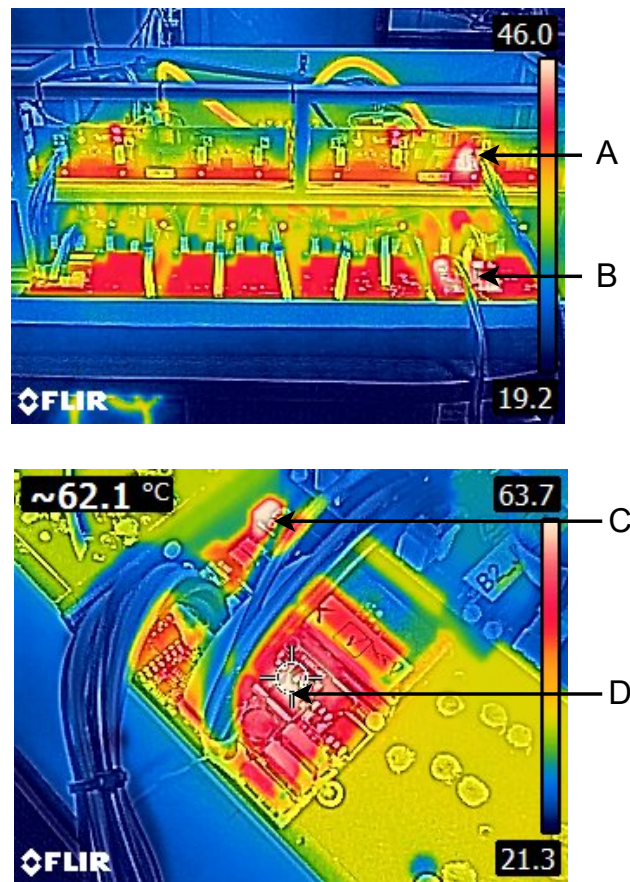


Figure 7.1: Thermal image of a Burn-in station, with its covers removed, during the Burn-in of a Brick located in Channel 1 of 8 (top). A dummy load voltage-controlled current sink (A) can be seen converting the power received from a V8.4.2 Brick undergoing Burn-in (B) into heat. A thermal image of a special sub-variant of a V8.4.2 Brick undergoing Burn-in (bottom). The target is centered on heat generated by the primary-side MOSFETs (D). This sub-variant made use of new, more efficient, switching MOSFETs, which were adopted in all subsequent versions. A second hot spot can be observed on the top corner of the Brick (C). This is an inductor that forms part of the buck converter on the secondary side. This component was changed to one with a form factor that allowed for better thermal coupling to the ceramic post below it. This new (L4) inductor can be seen in Figure 3.21.

7.2 Preliminary Burn-in Procedure

The Burn-in procedure subjects the Bricks to sub-optimal operating conditions, which function to stimulate failure mechanisms within the Bricks. This procedure is the subject of ongoing research. These conditions need to fall within the extrema allowed for by the Brick design and operation. There are two reasons for this. The first is related to effective Burn-in, and the second is related to the implementation of the Burn-in procedure. Firstly, the failure mechanisms stimulated must be of the kind that can be experienced during operation within the TileCal such as an increased operating temperature. Secondly, the

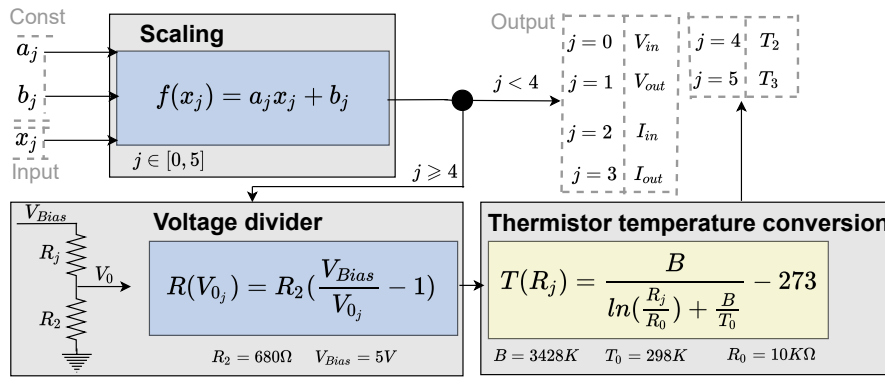


Figure 7.2: Block diagram illustrating the linear scaling of digitised Brick Burn-in parameters. The temperature parameters, $j \geq 4$, require additional processing in that the digitised thermistor voltage is converted into its equivalent resistance and, then subsequently, into its operating temperature.

Burn-in parameters must be restricted to the parameters provided in Table 7.1 due to the Bricks' inbuilt protection circuitry. A Brick will initiate a trip (immediate shutdown) if the OCP or OTP trip points are reached during Burn-in. If the operating parameters are set to within the variance of the trip points, intermittent Brick trips would occur during the Burn-in procedure, which would not only be operationally taxing, but also bring the validity of the Burn-in results into question, whereas if the parameters are set higher than this variance, the Bricks will start and immediately trip so that Burn-in could not take place.

Parameter	Burn-In	Nominal	Protection
Operating temperature	60 °C	35 °C	70 °C (OTP)
Applied load	5.0 A	2.3 A	6.9 A (OCP)
Output voltage	10 V	10 V	11.85 V (OVP)
Run-time	8 h	-	-

Table 7.1: Preliminary Phase-II Upgrade Brick Burn-in parameters, nominal V8.6.0 Brick operating parameters (over-voltage, over-current, over-temperature), and protection circuitry trip points.

The run-time of the Burn-in procedure is an important parameter. One needs to weigh the efficacy of the Burn-in process against the practicality of undertaking the Burn-in of a large population of Bricks within a finite time period. The above points combined with previous experience obtained through the Burn-in of the V7.5.0 Bricks were considered, resulting in the Burn-in parameters provided in Table 7.1 being selected. The 8 h run-time originated from the development of the V6.5.4 Brick and its associated quality assurance procedure by Argonne National Laboratory. The explicit calculations in which this run-time was determined were unfortunately not recorded, with information provided only in the form of internal presentations of the Burn-in procedure. As this Burn-in

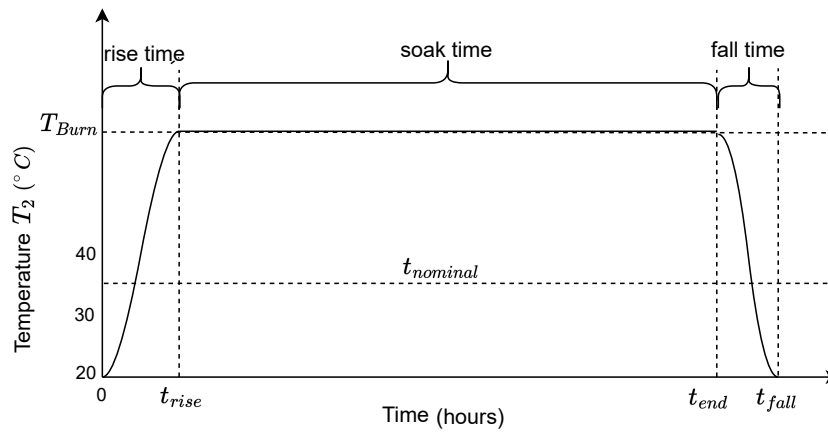


Figure 7.3: Generalised Phase-II Brick preliminary Burn-in procedure thermal profile. The Burn-in temperature (T_{Burn}) is 60°C as measured by the Bricks T2 thermistor.

duration has been successful when applied to two previous Brick versions, it was considered as a good starting point for the preliminary Burn-in procedure. That being said, numerous components have been changed in the subsequent Brick versions, and a naive assumption of the equivalency of their behaviour during Burn-in presents a major risk. Therefore, a quantitative analysis of the Burn-in duration and its efficacy are the subject of ongoing research.

A generalised Phase-II Brick Burn-in procedure thermal profile is illustrated in Figure 7.3. The T_2 temperature value originates from a thermistor located in between the primary-side MOSFETs. This thermistor, which records one of two on-Brick temperatures, was selected as it is utilised in the Brick OTP circuitry in which it measures the highest on-Brick temperatures originating from the MOSFET switching losses. The thermal profile can be sub-divided into three distinct regions. These are known as the rise, soak, and fall regions. At the onset of the Burn-in procedure, the Bricks are switched on and put under a 5 A load. The Bricks and the cooling system are in thermal equilibrium at 20°C at this point. This lower bound was selected due to it being the average on-detector temperature of the Bricks when they are not in operation. The temperature steadily climbs via the action of the cooling system, increasing the temperature of the heat-sinks. This process is assisted by the Bricks' self-heating due to inherent power conversion inefficiency. The characteristic curve is a result of the heat capacity of the system and the conductive, as well as radiative losses. The soak region begins after time T_{rise} and continues for a total time period known as the soak time at the Burn-in temperature of 60°C . The Burn-in procedure run-time is taken as the sum of the rise and soak time. This is because the Brick must remain under load during the entirety of the Burn-in procedure. At the eight-hour mark, the Burn-in procedure is terminated with the Bricks being switched off and brought down to their starting temperature. The time that it takes for the Bricks to be brought down to their starting temperature is known as the fall time.

7.3 Burn-in Station Final Commissioning

The Burn-in station records and displays numerous behavioural parameters. The purpose of these measurements is to ensure that the Burn-in procedure is being correctly applied while also providing insight into the performance of the Bricks during Burn-in. The raw data originate from two distinct sources, as can be seen in Table 7.2. That is, the performance data are measured by the Bricks themselves and the dummy load boards to which they provide power. The data produced by these two sources take two types of paths to the PC, which are illustrated in Figure 4.20. The first path type considered consists of raw analog data measured by a Brick, or dummy load board, which is then converted by the ADC of the associated interface board into a representative serial bit stream. The bit stream is then transmitted to the BLA, where it is scaled, displayed, and logged. The scaling of a Brick's raw digital data is illustrated in Figure 7.2. It was assumed that the relationship between the raw analog data and the corresponding digital data is linear within a small deviation from nominal. Therefore, a linear function $f(x_j)$ was used to perform the scaling of the $j - th$ raw data x_j . The scaling of x_j was achieved by the selection of appropriate calibration constants a_j and b_j , which correspond to a gain and offset, respectively. The selection of appropriate gain and offset values to ensure equality between the physical values and the recorded and displayed values constitutes the calibration of the Burn-in station.

Origin	Measurement	Label on BLA front panel
Brick	Input voltage	Vin
	Output voltage	Vout
	Input current	Iin
	Output current	Iout
	Temperature 2 ¹	T2
	Temperature 3	T3
Dummy-load board	Brick output voltage measured at load	Vload
	Brick output current measured at load	Iload
DC power supply	Burn-in station input voltage	Vin
	Burn-in station input current	Iin

Table 7.2: Burn-in station performance measurements and their origin.

The calibration constants are unique for each $j - th$ value of a Brick and for each of the eight Bricks. This procedure is followed for $j < 4$. For the remaining two measurements, the data need to be converted from a voltage (V_0) that is representative of the temperature of the T_2 or T_3 thermistors (Part No. NCP18XH103J03RB) into their actual temperature. This takes the form of two additional steps. The first step uses the scaled

¹The lack of a Temperature 1 measurement is an artifact of the removal of this measurement which was used in previous iterations of the Brick. The measurements are taken by thermistors located at the 2 and 3 positions. Position 2 is adjacent to the primary side switching MOSFETs of the Brick whereas position 3 is located adjacent to the output filtering stage.

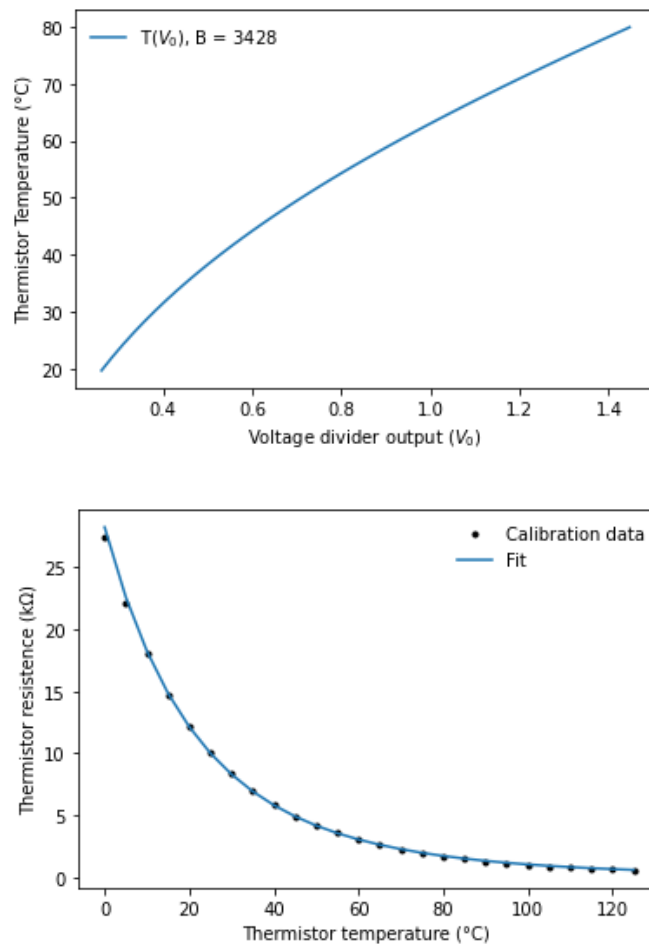


Figure 7.4: Thermistor temperature as a function of the voltage divider output voltage (top) and its calibration curve (bottom).

voltage to determine the thermistors' resistance R_j . This resistance is then used to calculate the thermistors' temperature. The relationship between the voltage received from the voltage divider and the thermistors' operating temperature is illustrated in Figure 7.4 left. The thermistor B value of 3428 k was chosen with the thermistor calibration curve for this value illustrated in Figure 7.4, right. The dummy load raw data undergo the same process of scaling and associated calibration as the current and voltage measurements of the Bricks for each of the eight dummy load channels (1 channel per Brick).

To further assess whether the final commissioning of the Wits Burn-in station was successful, an entire Burn-in procedure was applied to a V8.4.2 Brick. A special V8.4.2 Brick, with the "new" higher-efficiency MOSFETs and L4 inductor as updated in the V8.5.0 Brick, was used. This was performed so that the V8.4.2 Brick provided an approximate analog to the V8.5.0 Brick in terms of thermal characteristics and efficiency. This was necessitated as the V8.5.0 Brick shown in Figure 3.21 (and five others like it) had not been produced at the time of testing. The low sample size (one Brick) of the V8.4.2

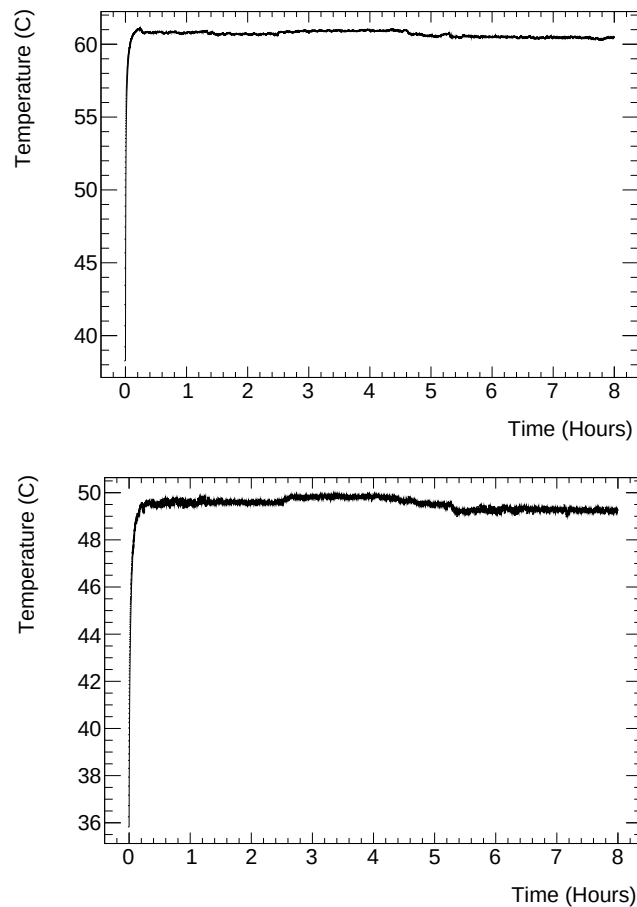


Figure 7.5: Thermal profile of a Phase-II Upgrade LVPS V8.4.2 Brick undergoing 8 h Burn-in testing. The T2 and T3 thermistor values are presented on the top and bottom, respectively. The lack of an anticipated trailing edge indicating the reduction of the Brick lower temperature bound is due to the cessation of data recording at the end of Burn-in procedure. This behaviour is being addressed in the latest Burn-in LabVIEW Application.

Brick was due to the majority of the South African Bricks being sent directly to CERN for use in the TileCal Phase-II Upgrade test beam campaigns. In order to increase the sample size and corroborate the current findings, the measurements presented below will be repeated with the six V8.5.0 Bricks.

The measurements of the Bricks' T2 and T3 temperature, as well as their efficiency during the Burn-in procedure, provide a probe into not only the performance of the Bricks, but also that of the Burn-in station. The T2 and T3 thermal profiles depicting the Burn-in of a single V8.4.2 Brick are illustrated in Figure 7.5. Three key observations can be made when comparing these thermal profiles to the idealised thermal profile illustrated in Figure 7.3. The first observation is that there is a difference of 10 °C between the T2 and T3 thermistor values, which was expected. This difference is due to their location, illustrated in Figure 3.21, being adjacent to the switching MOSFETs and LC-buck, respectively. These components output a different amount of heat during operation. The

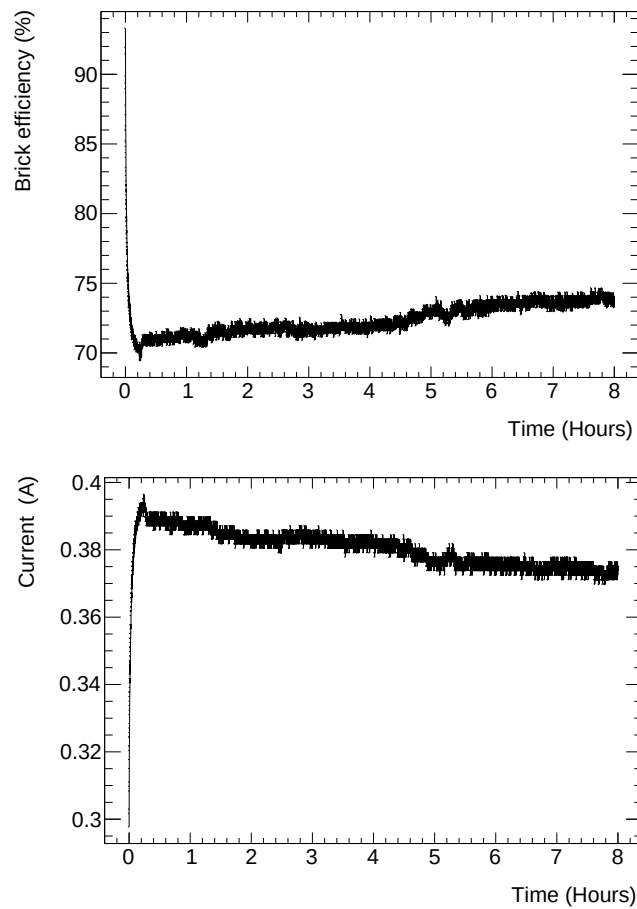


Figure 7.6: Efficiency plot of a Phase-II Upgrade LVPS V8.4.2 Brick undergoing Burn-in testing (top). The Brick's efficiency is defined as the ratio of the output and input power expressed as a percentage. The behaviour of the Brick's input current measurement over the Burn-in procedure (bottom).

second observation that can be made is that the starting temperature is not 20 °C, as motivated previously in Section 7.2. This is a consequence of the way in which the Burn-in temperature control is currently being implemented. Due to the Bricks not being 100% efficient, “self-heating” produces a ΔT between the thermostat values and cooling plate of approximately 20 °C. Therefore, to achieve the Burn-in temperature of 60 °C, the cooling plates need to be maintained at 40 °C. The thermal profile can be brought back into the specifications by either starting the cooling station at the commencement of the Burn-in procedure or programming the cooling station to ramp its temperature. The former ad hoc option is to be implemented, but development is anticipated for the latter. Finally, the trailing edge of the thermal profile is not visible. This is due to the data acquisition being terminated at the end of the Burn-in procedure. Although the thermal behaviour is well understood and should subsequently decrease to 40 °C, this will be addressed.

The efficiency of the V8.4.2 Brick during Burn-in is illustrated in Figure 7.6 (top).

The high efficiency observed at the start of the Burn-in procedure, which sharply decreases, can be attributed to the RC time constant associated with the input current measurement circuitry and is, therefore, not indicative of the Brick's actual efficiency at startup. The input current has an inverse relationship with the efficiency with its behaviour at Brick startup seen in Figure 7.6 (bottom).

7.4 Conclusions

The preliminary and final commissioning of the first WITS custom Brick burn-in station were completed successfully. The burn-in procedure and station calibration are crucial for ensuring the reliability and performance of the Bricks under operational conditions. An entire burn-in procedure was applied to a V8.4.2 brick with updated components to approximate the performance of a V8.5.0 brick. Key observations include a consistent 10 °C difference between T2 and T3 thermistor values due to component placement, the need to adjust the cooling station's starting conditions to achieve desired thermal profiles and that the thermostats for dummy load MOSFETs tripped frequently during normal operation. Ongoing research and adjustments continue to refine these processes so as to ensure that the burn-in parameters can be reliably applied by the station.

Chapter 8

Summary and Outlook

This Thesis is comprised of six main chapters. The first of which "The Large Hadron Collider and its Upgrade" introduced the LHC and its operation. Upon this, the upgrade preceding the HL-LHC was presented in brief so as to present the development of the machine in chronological order. This is a key aspect that was adhered to in this thesis, that is, the chronological presentation of the topics herein contained. This was emphasised as the logical, controlled and planned development of the LHC and its detectors underpins the methodology employed at CERN and within the research methods applied in this thesis. As second overarching topic within this thesis is that of scale, one that again has constant presence at CERN and in the field of High-energy physics as a whole. As the thesis unfolded the immense scales of the LHC accelerator complex and the ATLAS experiment were progressively broken down until the primary "object" of interest, the TileCal fLVPS Brick, was reached in a fashion that oriented the reader as to its role and importance within the experiment and therefore in taking collision data. This was done while progressively introducing the reader to the concepts and considerations of detector reliability.

Details of the HL-LHC machine were furnished with the motivation for its upgrade provided. This motivation can be put succinctly as a means to fully exploit the physics potential of the LHC by achieving higher instantaneous luminosity. The main consequences of the increased luminosity at the ATLAS interaction point, namely an increased annual radiation dose of detector systems within the cavern and the substantial increase in pile-up to $\langle \mu \rangle = 140$ to 200, were provided.

The next chapter to follow, "The ATLAS experiment and its upgrades", is based firmly upon the foundation and motivation provided by the previous chapter. The legacy Experiment was partitioned into its various sub-detectors and systems each of which being explained in enough detail so as to provide a global perspective. In keeping with the chronological development of the ATLAS experiment the Phase-I Upgrade was covered in brief. The Phase-II Upgrade, the motivation for which being to ensure the detectors performance in the HL-LHC environment, was covered with finer granularity.

The scope of the thesis progressively narrowed in the fourth chapter to the principal sub-detector considered and its upgrade, the Hadronic Tile Calorimeter (TileCal). An in-depth presentation of this sub-detector is required as the fLVPS Brick (2048 in total) is

located within it. The Bricks are themselves an element of the TileCals Low-Voltage (LV) power distribution system that functions to provide LV power to the on-detector readout electronics. The cooling of the on-detector electronics is presented in anticipation of the thermal considerations which are pervasive in the chapters that follow.

The LV system of the TileCal was presented with its upgrade motivation being furnished. A key aspect of the upgrade being that of radiation hardness certification.

The historical background of the Brick is presented in chapter 6. This is particularly important as the Phase-II Upgrade Brick is an iteration of the legacy versions discussed (V6.5.4 and V7.5.0). The principle developments in thermal performance and reliability that took place between the V6.5.4 and V7.5.0 Brick are presented with many of the design features introduced in the V7.5.0 being carried over into the Phase-II Upgrade Brick. This becomes apparent in the section that follows in which the physical description of the latest iteration of the Brick is presented along with a detailed functional overview.

Having thoroughly introduced the Brick, the development of the its phase-II successor commenced with a characterisation of the V8.4.2 Bricks thermal performance necessitated by manufacturing constraints experienced in South Africa surrounding the inability to produce Aluminium Nitride thermal posts locally. In an attempt to employ the locally manufactured Aluminium oxide thermal posts, which have a poorer thermal conductivity, several novel Hybrid Brick variants were produced each with a different distribution of thermal post types (Aluminium nitride or oxide). Through the production of these the location of the primary hot-spots surrounding the T1/T2 MOSFETs and the L4 inductor were identified.

Following the identification of the principal hot-spots a High-efficiency Brick variant was produced that utilized a more efficient MOSFET as well as a new L4 inductor with a form factor that is more conducive to efficient thermal coupling to its thermal post. The High-efficiency Brick was shown to exhibit a substantial improvement in thermal performance with a mean temperature measurement (T2) adjacent to the MOSFETs being reduced from approximately 50°C in the Baseline variant to 25°C.

Based on the significant improvement in thermal performance the High-efficiency Brick variant was selected as the next iteration of the Phase-II Upgrade Brick. Due to the change in the T1/T2 MOSFETs, which are active components, an irradiation hardness certification commenced. This certification spans the distinct sub-certifications of Single-Event Effect (SEE), Total Ionizing Dose (TID) and Non-Ionizing Energy Loss (NIEL). The results of the SEE sub-certification are presented with the new T1/T2 MOSFETs shown to operate nominally within a mono-energetic 200 MeV proton beam with a flux of 3×10^8 p/cm²/s until a fluence of 1.59×10^{12} p/cm² was reached (pre 2023 Radiation Tolerance Criteria). TID and NIEL certification were not presented but were passed thereby certifying the High-efficiency Brick for use within the HL-LHC environment within the TileCal.

A reliability analysis was then conducted on High-efficiency Brick which was designated as the V8.6.0 Phase-II Upgrade Brick. It was found that the estimated annual failure rate of V8.6.0 Brick is 0.4 which is a notable improvement to the V7.5.0 Brick which exhibited a failure rate of two Bricks per year. It was noted that the results obtained in the reliability analysis will only be valid if a robust quality assurance procedure is followed with the Phase-II Upgrade Brick production as in the case of the V7.5.0 Bricks.

The new quality assurance procedure for the Phase-II Upgrade Bricks was presented with a focus being placed on the development of the custom burn-in apparatus and the burn-in procedure that it is charged with applying. The University of the Witwatersrand Burn-in station was successfully been developed, manufactured, and commissioned. The station is poised for use within the pre-production of 108 units,

Outlook

The development of the Phase-II Upgrade finger Low-Voltage Power Supply Brick has been concluded with the pre-production of 104 pre-production Bricks having successfully taken place in South Africa. The directly responsible WITS fLVPS team is pictured in Figure 8.1. Finally, the fLVPS Brick project is globally on schedule as can be seen in Figure G.1. The quality assurance testing of the new Bricks has commenced with many new insights being gained into the custom apparatus as well as the Bricks themselves with future academic outputs on the topics being anticipated.



Figure 8.1: A picture of the South African TileCal Phase-II Brick team at Jemstech (the population House) during pre-production. From left to right, Thabo Pilusa, Vongani Chabalala, Ryan Mckenzie holding the first pre-production Brick and Charl Swanepoel of Jemstech.

List of Abbreviations

ACR	ATLAS Control Room
ADC	Analog-to-Digital Converter
ALICE	A Large Ion Collider Experiment
ANL	Argonne National Laboratory
ATCA	Advanced Telecommunication Computing Architecture
ATLAS	A Toroidal LHC Apparatus
BIB	Brick Interface Board
BLA	Burn-in LabVIEW Application
CAD	Computer-Aided design
CERN	Conseil Européen pour la Recherche Nucléaire also known as the European Laboratory of Particle Physics
CIS	Charge Injector System
COTS	Commercial Off-The-Shelf
CMOS	Complementary Metal-Oxide Semiconductor
CMS	Compact Muon Solenoid
CP	Cooling Plates
CPM	Compact Processing Modules
CS	Chip Select
CSC	Cathode Strip Chambers
CTP	Central Trigger Processor
DAC	Digital-to-Analog Converter
DAQ	Data Acquisition
DB	Daughterboard
DC	Direct Current
DCS	Detector Control System
DLB	Dummy-Load Board
DSS	Detector Safety System
DTR	Data Terminal Ready
DUT	Device Under Test
EB	Extended-Barrel
eFEX	electromagnetic Feature Extractor
ELDR	Enhanced Low Dose Rate
ELMB	Embedded Local Monitoring Board

ELMB-MB	Embedded Local Monitoring Board MotherBoard
EM	Electro-Magnetic
EMC	Electromagnetic Compatibility
EMEC	Electro-Magnetic End-cap Calorimeter
FCal	Forward Calorimeter
FE	Front-End
FET	Field-Effect Transistor
FELIX	Front-End Link eXchange
FENICS	Front End board for the New Infrastructure with Calibration and signal Shaping
FIT	Failures-In-Time
fLVPS	finger Low-Voltage Power Supply
FPGA	Field Programmable Gate Array
FWHM	Full Width at Half Maximum
GCS	Global Control Stations
gFEX	global Feature Extractor
HEC	Hadronic End-cap Calorimeter
HGTD	High-Granularity Timing Detector
HL-LHC	High Luminosity Large Hadron Collider
HV	High-Voltage
IBL	Insertable B-Layer
IC	Integrated Circuit
ID	Inner Detector
IP	Interaction Point
ITC	Intermediate Tile Calorimeter
ITK	Inner Tracker
jFEX	jet Feature Extractor
LAr	Liquid Argon
LB	Long-Barrel
LCS	Leakless Cooling System
LDR	Low Dose Rates
LET	Linear Energy Transfer
LHC	Large Hadron Collider
LHCb	Large Hadron Collider beauty
LIB	Load Interface Board
LINAC	Linear Accelerator
LIU	LHC Injectors Upgrade
LV	Low-Voltage
LVPS	Low-Voltage Power Supply
MB	Mainboard
MD	Mini-Drawer

MDT	Monitored Drift Tube
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
MTTF	Mean Time To Failure
NIEL	Non-Ionizing Energy Loss
NMOS	Negative carrier Metal-Oxide Semiconductor
NSW	New Small Wheel
OCF	Over-Current Protection
OF	Optimal Filtering
OTP	Over-Temperature Protection
OVP	Over-Voltage Protection
PCB	Printed Circuit Board
PIC	Programmable Integrated Circuit
PIF	Proton Irradiation Facility
PPr	Pre-Processor
PS	Proton Synchrotron
PSI	Paul Scherrer Institute
PMOS	Positive carrier Metal-Oxide Semiconductor
PMT	Photo-Multiplier Tube
POL	Point-Of-Load
PWM	Pulse Width Modulation
RETF	Radiation Effects Task-Force
RF	Radio Frequency
RMS	Root Mean Squared
ROD	
ROI	Regions of Interest
RPC	Resistive Plate Chambers
RTC	Radiation Tolerance Criteria
RTS	Request To Send
SCK	Serial Clock
SCS	Sub-detector Control Stations
SCT	Semi-Conductor Tracker
SD	Super-drawers
SDI	Serial Data Input
SDO	Serial Data Output
SEB	Single Event Burnout
SEE	Single Event Effects
SEGR	Single Event Gate Rupture
SET	Single Event Transients
SEU	Single Event Upsets
SF	Safety Factor

SPI	Serial Peripheral Interface
SPS	Super Proton Synchrotron
SRL	Simulated Radiation Level
TDAQ	Trigger and Data Acquisition
TDAQi	Trigger and Data Acquisition interface
TGC	Thin Gap Chambers
TileCal	Hadronic Tile-Calorimeter
TileCoM	Tile Computer-on-Module
TilePPr	TileCal PreProcessor
TID	Total Ionising Dose
TRT	Transition Radiation Tracker
TTC	Trigger, Timing, and Control
UART	Universal Asynchronous Receiver / Transmitter
USB	Universal Serial Bus
UTA	The University of Texas at Arlington
VCCS	Voltage Controlled Current Sink
WITS	The University of the Witwatersrand
WLS	Wavelength Shifting
YETS	Year End Technical Stop

Bibliography

- [1] L. Evans et al. “LHC Machine”. In: *JINST* 3 (2008), S08001. DOI: 10.1088/1748-0221/3/08/S08001. URL: <https://cds.cern.ch/record/1129806>.
- [2] The ATLAS Collaboration. “The ATLAS Experiment at the CERN Large Hadron Collider”. In: *JINST* 3 (2008), S08003. DOI: 10.1088/1748-0221/3/08/S08003. URL: <https://cds.cern.ch/record/1129811>.
- [3] The CMS Collaboration. “The CMS experiment at the CERN LHC. The Compact Muon Solenoid experiment”. In: *JINST* 3 (2008). Also published by CERN Geneva in 2010, S08004. DOI: 10.1088/1748-0221/3/08/S08004. URL: <https://cds.cern.ch/record/1129810>.
- [4] The ALICE Collaboration. “The ALICE experiment at the CERN LHC. A Large Ion Collider Experiment”. In: *JINST* 3 (2008). Also published by CERN Geneva in 2010, S08002. DOI: 10.1088/1748-0221/3/08/S08002. URL: <https://cds.cern.ch/record/1129812>.
- [5] The LHCb Collaboration. “The LHCb Detector at the LHC”. In: *JINST* 3 (2008). Also published by CERN Geneva in 2010, S08005. DOI: 10.1088/1748-0221/3/08/S08005. URL: <https://cds.cern.ch/record/1129809>.
- [6] E. Lopienska. “The CERN accelerator complex, layout in 2022.” In: (2022). General Photo. URL: <https://cds.cern.ch/record/2800984>.
- [7] S. Morales Vigo. “Beam Loss Monitors in the Large Hadron Collider”. Presented 08 Jul 2020. 2020. URL: <https://cds.cern.ch/record/2747978>.
- [8] R. Bailey et al. *Standard Filling Schemes for Various LHC Operation Modes*. Tech. rep. Geneva: CERN, 2003. URL: <https://cds.cern.ch/record/691782>.
- [9] H. Damerau et al. *LHC Injectors Upgrade, Technical Design Report*. 2014. DOI: 10.17181/CERN.7NHR.6HGC. URL: <https://cds.cern.ch/record/1976692>.
- [10] G. Apollinari et al. *High-Luminosity Large Hadron Collider (HL-LHC): Preliminary Design Report*. CERN Yellow Reports: Monographs. Geneva: CERN, 2015. DOI: 10.5170/CERN-2015-005. URL: <https://cds.cern.ch/record/2116337>.
- [11] O. Bruning. “LHC challenges and upgrade options”. In: *Journal of Physics: Conference Series* 110.11 (2008), p. 112002. DOI: 10.1088/1742-6596/110/11/112002. URL: <https://dx.doi.org/10.1088/1742-6596/110/11/112002>.

- [12] E. Todesco et al. "The High Luminosity LHC interaction region magnets towards series production". In: *Supercond. Sci. Technol.* 34.5 (2021), p. 053001. DOI: 10.1088/1361-6668/abdba4. URL: <https://cds.cern.ch/record/2759601>.
- [13] R. Calaga. "Crab Cavities for the High-luminosity LHC". In: (2018), THXA03. DOI: 10.18429/JACoW-SRF2017-THXA03. URL: <https://cds.cern.ch/record/2673544>.
- [14] B. Schmidt. "The High-Luminosity upgrade of the LHC: Physics and Technology Challenges for the Accelerator and the Experiments". In: *Journal of Physics: Conference Series* 706.2 (2016), p. 022002. DOI: 10.1088/1742-6596/706/2/022002. URL: <https://dx.doi.org/10.1088/1742-6596/706/2/022002>.
- [15] "ATLAS: letter of intent for a general-purpose pp experiment at the large hadron collider at CERN". In: (1992). URL: <https://cds.cern.ch/record/291061>.
- [16] The ATLAS Collaboration. "The ATLAS Experiment at the CERN Large Hadron Collider". In: *JINST* 3 (2008). Also published by CERN Geneva in 2010, S08003. DOI: 10.1088/1748-0221/3/08/S08003. URL: <https://cds.cern.ch/record/1129811>.
- [17] J. Pequena. "Computer generated image of the whole ATLAS detector". 2008. URL: <https://cds.cern.ch/record/1095924>.
- [18] *ATLAS inner detector: Technical Design Report, 1*. Technical design report. ATLAS. Geneva: CERN, 1997. URL: <https://cds.cern.ch/record/331063>.
- [19] M. Capeans et al. *ATLAS Insertable B-Layer Technical Design Report*. Tech. rep. 2010. URL: <https://cds.cern.ch/record/1291633>.
- [20] B. Mindur. "ATLAS Transition Radiation Tracker (TRT): Straw tubes for tracking and particle identification at the Large Hadron Collider". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 845 (2017). proceedings of the Vienna Conference on Instrumentation 2016, pp. 257–261. ISSN: 0168-9002. DOI: <https://doi.org/10.1016/j.nima.2016.04.026>. URL: <https://www.sciencedirect.com/science/article/pii/S0168900216301905>.
- [21] *IBL Efficiency and Single Point Resolution in Collision Events*. Tech. rep. All figures including auxiliary figures are available at <https://atlas.web.cern.ch/Atlas/GROUPS/PHYSICS/PUBLISHED/INDET-PUB-2016-001>. Geneva: CERN, 2016. URL: <https://cds.cern.ch/record/2203893>.
- [22] *ATLAS liquid-argon calorimeter: Technical Design Report*. Technical design report. ATLAS. Geneva: CERN, 1996. DOI: 10.17181/CERN.FWRW.F00Q. URL: <https://cds.cern.ch/record/331061>.
- [23] *Approved Tile Calorimeter Plots*. Tech. rep. Geneva: CERN, 2023. URL: <https://twiki.cern.ch/twiki/bin/view/AtlasPublic/ApprovedPlotsTile>.

- [24] R. S. “The Performance of the ATLAS Trigger System in the LHC proton-proton Collisions”. In: *Physics Procedia* 37 (Dec. 2012). DOI: 10.1016/j.phpro.2012.02.503.
- [25] B. I. Hallgren et al. “The Embedded Local Monitor Board (ELMB) in the LHC Front-end I/O Control System”. In: (2001). DOI: 10.5170/CERN-2001-005.325. URL: <http://cds.cern.ch/record/530675>.
- [26] The ATLAS Collaboration. “Operation and performance of the ATLAS Tile Calorimeter in Run 1”. In: *Eur. Phys. J. C* 78.12 (2018). 69 pages in total, author list starting page 53, 28 figures, 11 tables, submitted to EPJC. All figures and tables are available at <https://atlas.web.cern.ch/Atlas/GROUPS/PHYSICS/PAPERS/TCAL-2017-01>, p. 987. DOI: 10.1140/epjc/s10052-018-6374-z. arXiv: 1806.02129. URL: <https://cds.cern.ch/record/2622093>.
- [27] P. Bonneau et al. “Cooling system for the TILECAL hadron calorimeter of the ATLAS detector”. In: (Feb. 1998).
- [28] S. Agostinelli et al. “Geant4—a simulation toolkit”. In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 506.3 (2003), pp. 250–303. ISSN: 0168-9002. DOI: [https://doi.org/10.1016/S0168-9002\(03\)01368-8](https://doi.org/10.1016/S0168-9002(03)01368-8). URL: <https://www.sciencedirect.com/science/article/pii/S0168900203013688>.
- [29] T. Sjostrand et al. “A Brief Introduction to PYTHIA 8.1”. In: *Comput. Phys. Commun.* 178 (2008), pp. 852–867. DOI: 10.1016/j.cpc.2008.01.036. arXiv: 0710.3820. URL: <https://cds.cern.ch/record/1064095>.
- [30] *The Pythia 8 A3 tune description of ATLAS minimum bias and inelastic measurements incorporating the Donnachie-Landshoff diffractive model*. Tech. rep. Geneva: CERN, 2016. URL: <https://cds.cern.ch/record/2206965>.
- [31] *Technical Design Report for the ATLAS Inner Tracker Pixel Detector*. Tech. rep. Geneva: CERN, 2017. DOI: 10.17181/CERN.F0ZZ.ZP3Q. URL: <https://cds.cern.ch/record/2285585>.
- [32] *Technical Design Report for the ATLAS Inner Tracker Strip Detector*. Tech. rep. Geneva: CERN, 2017. URL: <https://cds.cern.ch/record/2257755>.
- [33] C. Solans Sanchez. “ATLAS toward the High Luminosity era: challenges on electronic systems”. In: *Proceedings of The European Physical Society Conference on High Energy Physics — PoS(EPS-HEP2021)*. Vol. 398. 2022, p. 826. DOI: 10.22323/1.398.0826.
- [34] *Technical Design Report: A High-Granularity Timing Detector for the ATLAS Phase-II Upgrade*. Tech. rep. Geneva: CERN, 2020. URL: <https://cds.cern.ch/record/2719855>.

- [35] *ATLAS Liquid Argon Calorimeter Phase-II Upgrade: Technical Design Report*. Tech. rep. Geneva: CERN, 2017. DOI: 10.17181/CERN.6QIO.YGH0. URL: <https://cds.cern.ch/record/2285582>.
- [36] *Technical Design Report for the Phase-II Upgrade of the ATLAS Tile Calorimeter*. Tech. rep. Geneva: CERN, 2017. URL: <https://cds.cern.ch/record/2285583>.
- [37] G. Di Gregorio. *Long term aging test of the new PMTs for the HL-LHC ATLAS hadron calorimeter upgrade*. Tech. rep. Geneva: CERN, 2021. DOI: 10.1109/NSS/MIC44867.2021.9875660. URL: <https://cds.cern.ch/record/2798642>.
- [38] *Technical Design Report for the Phase-II Upgrade of the ATLAS Muon Spectrometer*. Tech. rep. Geneva: CERN, 2017. URL: <https://cds.cern.ch/record/2285580>.
- [39] *ATLAS tile calorimeter: Technical Design Report*. Technical design report. ATLAS. Geneva: CERN, 1996. DOI: 10.17181/CERN.JRBJ.7028. URL: <https://cds.cern.ch/record/331062>.
- [40] A. Valero Biot. *Diagram of the TileCal trigger and readout electronics at the HL-LHC*. Tech. rep. Geneva: CERN, 2023. URL: <https://cds.cern.ch/record/2855963>.
- [41] E. V. Santurio et al. "A Revised Version of the ATLAS Tile Calorimeter Link Daughterboard for the HL-LHC". In: *IEEE Trans. Nucl. Sci.* 68.9 (2021), pp. 2414–2420. DOI: 10.1109/tns.2021.3103408. URL: <https://cds.cern.ch/record/2783294>.
- [42] A. Cervelló et al. "The TileCal PreProcessor interface with the ATLAS global data acquisition system at the HL-LHC". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 1043 (2022), p. 167492. ISSN: 0168-9002. DOI: <https://doi.org/10.1016/j.nima.2022.167492>. URL: <https://www.sciencedirect.com/science/article/pii/S0168900222007847>.
- [43] J. T. Anderson et al. *FELIX: a High-Throughput Network Approach for Interfacing to Front End Electronics for ATLAS Upgrades*. Tech. rep. 8. Geneva: CERN, 2015. DOI: 10.1088/1742-6596/664/8/082050. URL: <https://cds.cern.ch/record/2016626>.
- [44] M. Gololo et al. "Tile Computer-on-Module for the ATLAS Tile Calorimeter Phase-II upgrades". In: *Journal of Instrumentation* 17.06 (June 2022), P06020. DOI: 10.1088/1748-0221/17/06/P06020. URL: <https://dx.doi.org/10.1088/1748-0221/17/06/P06020>.
- [45] M. Marjanovic. *ATLAS Tile calorimeter calibration and monitoring systems*. Tech. rep. Geneva: CERN, 2018. URL: <https://cds.cern.ch/record/2625460>.
- [46] The ATLAS Collaboration. "Operation and performance of the ATLAS Tile Calorimeter in Run 1". In: *The European Physical Journal C* 78.12 (Nov. 2018). DOI: 10.1140/epjc/s10052-018-6374-z. URL: <https://doi.org/10.1140%2Fepjc%2Fs10052-018-6374-z>.

- [47] I. Vichou. *Calibration and Monitoring of the Tile Hadronic Calorimeter of ATLAS with A137Cs Source*. Tech. rep. Geneva: CERN, 1998. URL: <https://cds.cern.ch/record/683609>.
- [48] G. Blanchot et al. "The Cesium source calibration and monitoring system of the ATLAS Tile Calorimeter: design, construction and results". In: *Journal of Instrumentation* 15.03 (Mar. 2020), P03017. DOI: 10.1088/1748-0221/15/03/P03017. URL: <https://dx.doi.org/10.1088/1748-0221/15/03/P03017>.
- [49] N. Shalanda et al. "Radioactive source control and electronics for the ATLAS tile calorimeter cesium calibration system". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 508.3 (2003), pp. 276–286. ISSN: 0168-9002. DOI: [https://doi.org/10.1016/S0168-9002\(03\)01700-5](https://doi.org/10.1016/S0168-9002(03)01700-5). URL: <https://www.sciencedirect.com/science/article/pii/S0168900203017005>.
- [50] M. Agaras et al. "Laser calibration of the ATLAS Tile Calorimeter during LHC Run 2". In: *Journal of Instrumentation* 18.06 (June 2023), P06023. DOI: 10.1088/1748-0221/18/06/P06023. URL: <https://dx.doi.org/10.1088/1748-0221/18/06/P06023>.
- [51] A. Da Silva Gomes et al. *Upgrade of the ATLAS Tile Calorimeter High Voltage System*. Tech. rep. Geneva: CERN, 2021. URL: <https://cds.cern.ch/record/2789722>.
- [52] G. Blanchot et al. *ATLAS Cooling Systems: LCS v.2 Full Scale Test*. Geneva: CERN, 2001. URL: <http://cds.cern.ch/record/1072145>.
- [53] G. Schlager. "Development and Test of the Cooling System for the ATLAS Hadron Tile Calorimeter". Presented on 08 Sep 2002. 2002. URL: <https://cds.cern.ch/record/779813>.
- [54] R. Baumann. "Radiation-induced soft errors in advanced semiconductor technologies". In: *IEEE Transactions on Device and Materials Reliability* 5.3 (2005), pp. 305–316. DOI: 10.1109/TDMR.2005.853449.
- [55] P. C. M. RC. M. Hsieh et al. "A field-funneling effect on the collection of alpha-particle-generated carriers in silicon devices". In: *IEEE Trans Electron Device Letters* 2.4 (1981), pp. 686–693.
- [56] A. Papadopoulou. "Single Event Effect Testing of Commercial Silicon Power MOSFETs. MOSFET ". Presented 26 Oct 2020. 2020. URL: <https://cds.cern.ch/record/2744728>.
- [57] K. B. C. R. Koga S. H. Penzin et al. "Single event functional interrupt (SEFI) sensitivity in microcircuits". In: *Proceedings of the Fourth European Conference on Radiation and Its Effects on Components and Systems (RADECS)* 4 (1998), pp. 311–318.

- [58] M. Dentan. "Overview of the ATLAS policy on radiation tolerant electronics". In: (2000). DOI: 10.5170/CERN-2000-010.270. URL: <https://cds.cern.ch/record/478882>.
- [59] M. Huhtinen et al. *Safety Factor and Testing Procedure Recommendations of the Radiation Effects Task Force*. Tech. rep. Geneva: CERN, 2020. URL: <https://cds.cern.ch/record/2718449>.
- [60] M. Moll. "Radiation damage in silicon particle detectors: Microscopic defects and macroscopic properties". PhD thesis. Hamburg U., 1999.
- [61] K. S. Nicpon et al. "The Embedded Local Monitor Board upgrade proposals". In: *PoS TWEPP2018* (2019), p. 034. DOI: 10.22323/1.343.0034. URL: <https://cds.cern.ch/record/2710377>.
- [62] I. Hruska et al. "Radiation-Tolerant Custom Made Low Voltage Power Supply System for ATLAS/TileCal Detector". In: (2007). DOI: 10.5170/CERN-2007-007.369. URL: <https://cds.cern.ch/record/1091490>.
- [63] S. Baranov et al. *Estimation of Radiation Background, Impact on Detectors, Activation and Shielding Optimization in ATLAS*. Tech. rep. Geneva: CERN, 2005. URL: <https://cds.cern.ch/record/814823>.
- [64] S. B. Vorojtsov et al. *3D Magnetic Field Calculations in the Finger Region of the TileCal*. Tech. rep. Geneva: CERN, 1999. URL: <https://cds.cern.ch/record/683936>.
- [65] G. Drake. *Design of a New Switching Power Supply for the ATLAS TileCAL Front-End Electronics*. Tech. rep. Geneva: CERN, 2012. URL: <https://cds.cern.ch/record/1493583>.
- [66] *LT1681 controller IC*. <https://www.analog.com/en/products/lt1681.html#product-overview>. Accessed: 07-12-2023.
- [67] *IR2110s gate driver IC*. <https://www.infineon.com/cms/en/product/power/gate-driver-ics/ir2110s>. Accessed: 07-12-2023.
- [68] *Legacy Aluminium Oxide thermal posts*. <http://accuratus.com/alumox.html>. Accessed: 04-12-2023.
- [69] *Legacy Aluminium Nitride thermal posts*. <http://accuratus.com/alumni.html>. Accessed: 04-12-2023.
- [70] *Berquist Gap Pads 2500*. https://www.henkel-adhesives.com/us/en/product/thermal-gap-pad-materials/bergquist_gap_padtgp2700.html. Accessed: 04-12-2023.
- [71] M. Dentan. "Overview of the ATLAS policy on radiation tolerant electronics". In: (2000). DOI: 10.5170/CERN-2000-010.270. URL: <https://cds.cern.ch/record/478882>.

- [72] G. Drake et al. *An Upgraded Front-End Switching Power Supply Design for the ATLAS TileCAL Detector of the LHC*. Tech. rep. Geneva: CERN, 2011. URL: <https://cds.cern.ch/record/1398264>.
- [73] *HCPL-7800 isolation amplifier*. <https://www.broadcom.com/products/optocouplers/industrial-plastic/isolation-amplifiers-modulators/isolation-amplifiers/hcpl-7800>. Accessed: 07-12-2023.
- [74] *IEC 61249-2-2:2005*. <https://webstore.iec.ch/publication/5008>. Accessed: 04-12-2023.
- [75] *T-Global Technology TG-N909 Non-Silicone Thermal Grease*. <https://www.tglobaltechnology.com/product/tg-n909-non-silicone-thermal-grease/>. Accessed: 04-12-2023.
- [76] *Molex 22-29-2041*. <https://www.molex.com/en-us/products/part-detail/22292041>. Accessed: 09-12-2023.
- [77] *Molex 52559-2052*. <https://www.molex.com/en-us/products/part-detail/525592052>. Accessed: 09-12-2023.
- [78] *Molex 39-28-1103*. <https://www.molex.com/en-us/products/part-detail/39281103>. Accessed: 09-12-2023.
- [79] S. Patil et al. "Design and implementation of multiple output forward converter with Mag-amp and LDO as post regulators for space application". In: *International Journal of Engineering, Science and Technology* 12 (Sept. 2020), pp. 43–56. DOI: 10.4314/ijest.v12i3.5.
- [80] *CERAdvantage*. <https://ceradvance.co.za/product/line-ox-sf/>. Accessed: 07-12-2023.
- [81] *STB57N65M5 power MOSFET*. <https://www.st.com/en/power-transistors/stb57n65m5.html>. Accessed: 08-12-2023.
- [82] *XAL1010*. <https://www.coilcraft.com/en-us/products/power/shielded-inductors/molded-inductor/xal/xal1010/>. Accessed: 07-12-2023.
- [83] *SIHFS9N60A*. <https://www.vishay.com/docs/91287/sihs9n60.pdf>. Accessed: 07-12-2023.
- [84] *SML-7443551130*. <https://www.we-online.com/components/products/datasheet/7443551130.pdf>. Accessed: 07-12-2023.
- [85] E. Nkadimeng et al. "A monitoring and control test bench for assessing the upgraded low voltage power supplies for the ATLAS Tile Calorimeter Phase-II Upgrade front-end electronics". In: *JINST* 17.07 (July 2022), P07025. DOI: 10.1088/1748-0221/17/07/P07025. URL: <https://dx.doi.org/10.1088/1748-0221/17/07/P07025>.

- [86] A. Senthilkumaran et al. "Reliability Analysis of a Low Voltage Power Supply Design for the Front-End Electronics of the ATLAS Tile Calorimeter". In: (2012). URL: <https://cds.cern.ch/record/1489570>.
- [87] "Introduction to Reliability Engineering". In: *Practical Reliability Engineering*. John Wiley Sons, Ltd, 2011. Chap. 1, pp. 1–18. ISBN: 9781119961260. DOI: <https://doi.org/10.1002/9781119961260.ch1>. eprint: <https://onlinelibrary.wiley.com/doi/pdf/10.1002/9781119961260.ch1>. URL: <https://onlinelibrary.wiley.com/doi/abs/10.1002/9781119961260.ch1>.
- [88] R. Mckenzie et al. "A Burn-In Apparatus for the ATLAS Tile Calorimeter Phase-II Upgrade Transformer-Coupled Buck Converters". In: *Instruments* 7.4 (2023). ISSN: 2410-390X. DOI: 10.3390/instruments7040041. URL: <https://www.mdpi.com/2410-390X/7/4/41>.
- [89] R. Mckenzie et al. "Quality assurance testing of the ATLAS Tile-Calorimeter Phase-II upgrade low-voltage power supplies". In: *The Proceedings of SAIP2021* (2021). DOI: 10.1088/1748-0221/3/08/s08003.
- [90] R. P. Mckenzie. "A Burn-in Test Station for the ATLAS Phase-II Tile-Calorimeter Low-Voltage Power Supply Transformer-Coupled Buck Converters". In: *Instruments* 7.1 (2023). ISSN: 2410-390X. DOI: 10.3390/instruments7010003. URL: <https://www.mdpi.com/2410-390X/7/1/3>.
- [91] M. Hibbard et al. "ATLAS TileCal low voltage power supply upgrade hardware and testing". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 936 (2019). Frontier Detectors for Frontier Physics: 14th Pisa Meeting on Advanced Detectors, pp. 112–114. ISSN: 0168-9002. DOI: <https://doi.org/10.1016/j.nima.2018.10.198>. URL: <https://www.sciencedirect.com/science/article/pii/S0168900218315122>.
- [92] LM9074M System Voltage Regulator. <https://www.mouser.com/datasheet/2/405/lm9074-442906.pdf>. Accessed: 25-01-2024.
- [93] RC0603FR-07680RL 680. https://eu.mouser.com/datasheet/2/447/YAGEO_PYu_RC_Group_51_RoHS_L_12-3313492.pdf. Accessed: 25-01-2024.
- [94] NCP18XH103J03RB 10K NTC thermistor. <https://www.murata.com/-/media/webrenewal/products/thermistor/ntc/ncp/ncp18.ashx?la=ja-jp&cvid=20211118090222000000>. Accessed: 25-01-2024.
- [95] Fluke 179 specifications sheet. <https://www.fluke.com/en/product/electrical-testing/digital-multimeters/fluke-179>. Accessed: 27-02-2024.
- [96] LT1681 reliability specifications sheet. <https://www.analog.com/media/en/technical-documentation/reliability-data/r352.pdf>.
- [97] IR2110s reliability specifications sheet. <https://www.infineon.com/cms/en/product/power/gate-driver-ics/ir2110s/>.

-
- [98] *HCPL7800 reliability specifications sheet*. <https://docs.broadcom.com/doc/AV02-3680EN>.
 - [99] *LTC6241 reliability specifications sheet*. <https://www.analog.com/media/en/technical-documentation/reliability-data/r465.pdf>.
 - [100] *SIHFS9N60A reliability specifications sheet*. <https://www.vishay.com/docs/90764/silicon.pdf>.
 - [101] M. Hibbard. "Accelerated ageing of a switching power supply prototype". PhD thesis. University of Texas at Arlington., 2018. URL: <https://rc.library.uta.edu/uta-ir/handle/10106/27761>.

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Appendix A

A.1 TileCal Phase-II Upgrade Cooling Requirements Calculation

	Item	Power (W)	Comments
Output power	LB fLVPS EB fLVPS	8 Bricks $\times$ 23 = 184 6 Bricks $\times$ 23 = 138	based on 10 V and 2.3 A output
Power delivered	LB fLVPS EB fLVPS	184 / 0.67 = 275 138 / 0.67 = 206	based on 67% Brick efficiency
Power delivered	All LB fLVPS All EB fLVPS	(128 $\times$ 275) = 35200 (128 $\times$ 206) = 26368	128 fLVPS in LB 128 fLVPS in EB
Power dissipated	200 V fLVPS input cables	1000	Based on 2021 data
Ambient heat	Cooling lines	16300	Calculated in 2023 likely inaccurate
Required Cooling capacity	Sum of all contributions	61570 + 10000 + 16300 = 788700	Exceeds legacy cooling capacity of 77 000 w

Table A.1: TileCal Phase-II on-detector cooling requirements. Calculation by Dr. Seyedali Moeyedi.

A.2 TileCal Bulk Low-Voltage Power Distribution

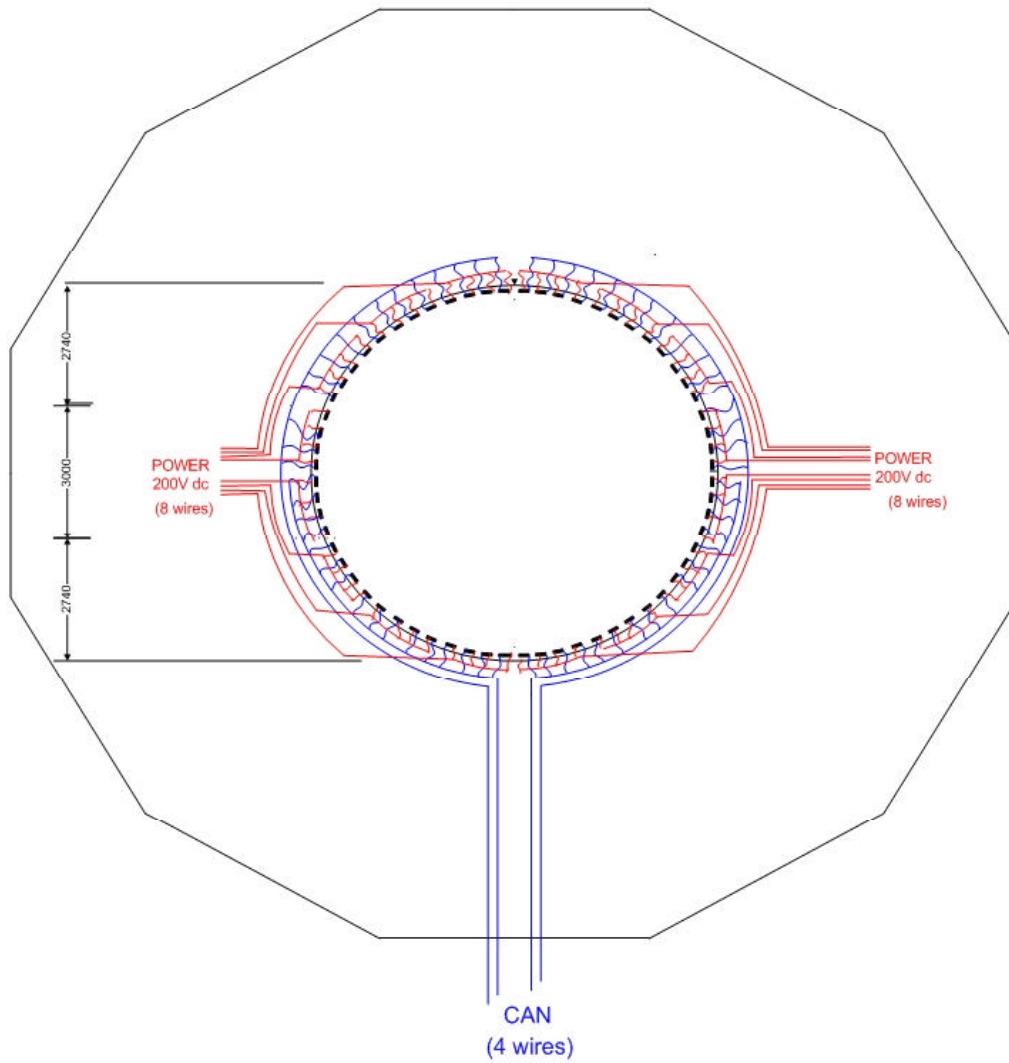


Figure A.1: Routing of 200 V cables and CAN wires to the 64 TileCal LVPS modules in a single barrel section.

Appendix B

TileCal Phase-II Upgrade fLVPS components

B.1 fLVPS Chassis and Cooling Plate

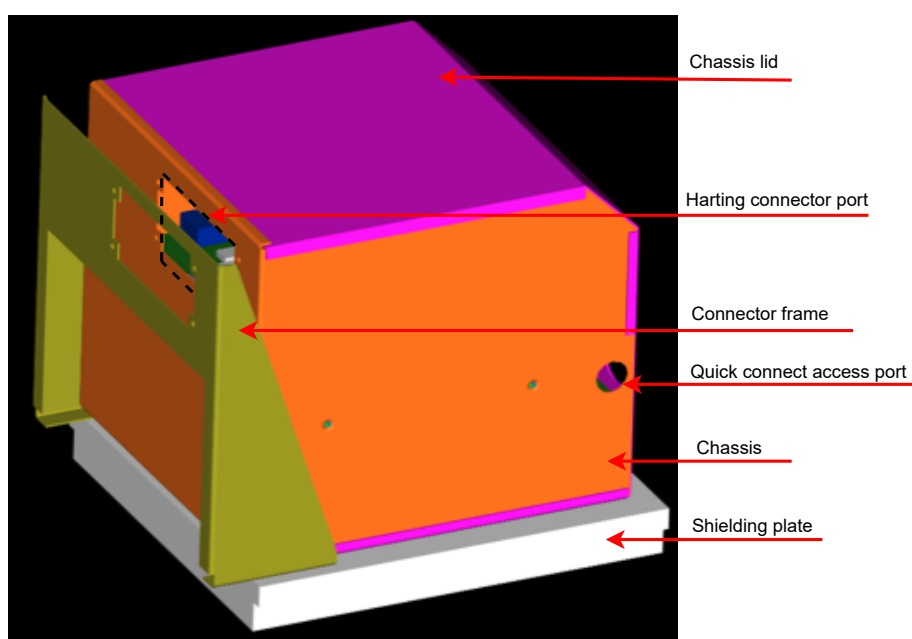


Figure B.1: Labelled computer-Aided-Design image of an fLVPS chassis.

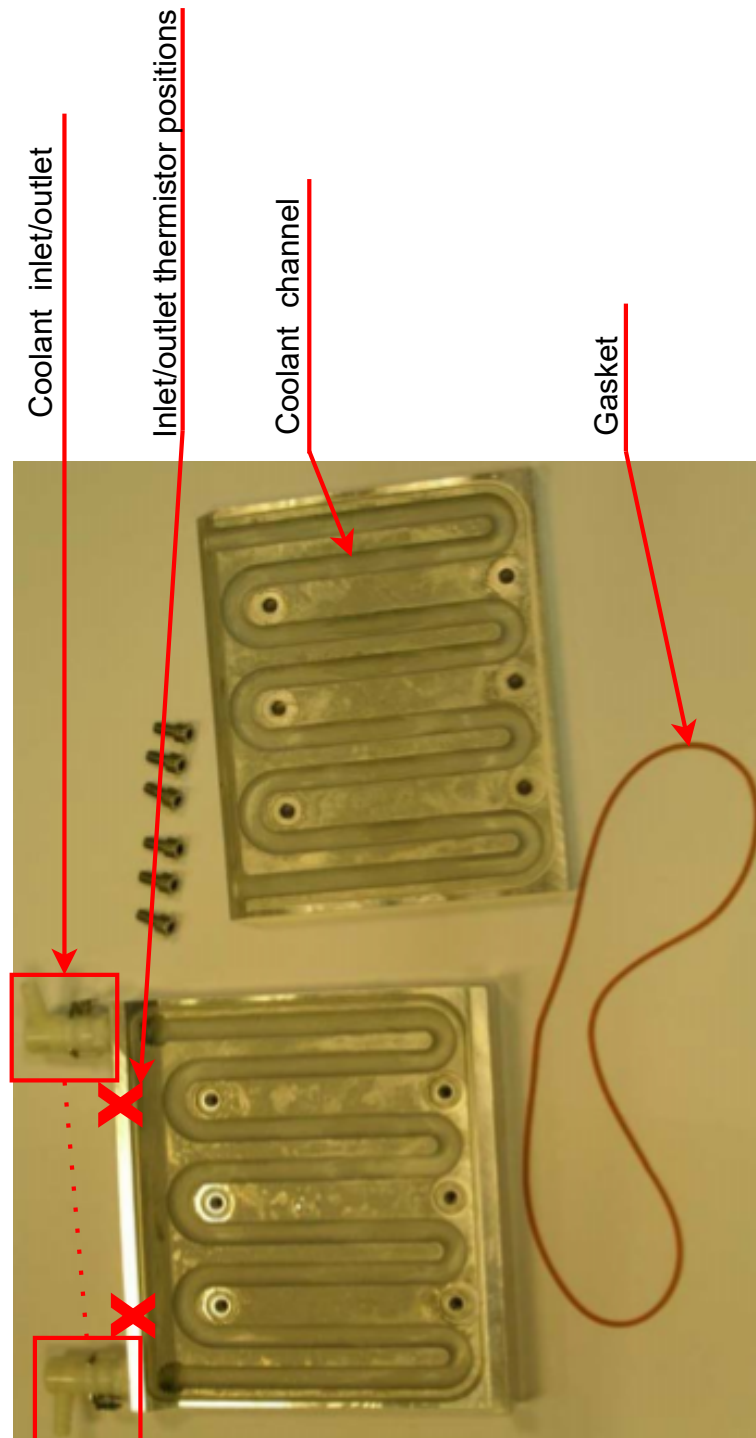


Figure B.2: Image of a disassembled fLVPS cooling plate.

B.2 fLVPS Cabling

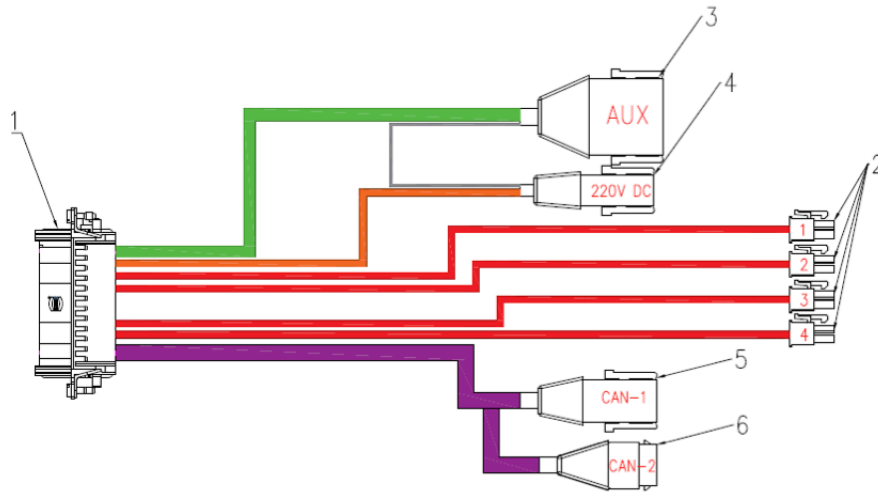


Figure B.3: Diagram of an Phase-II Upgrade Long-Barrel fLVPS external cable harness.

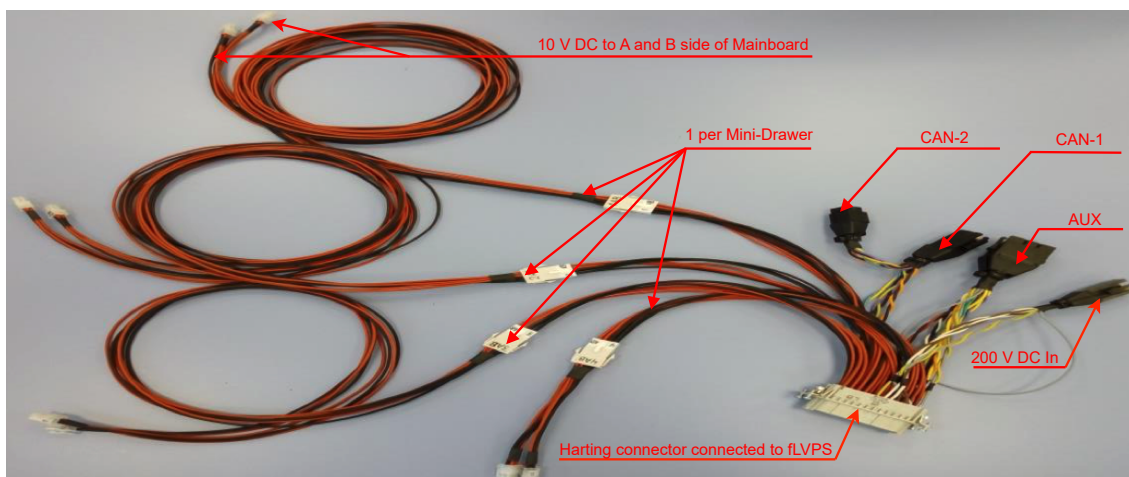


Figure B.4: Image of an Phase-II Upgrade Long-Barrel fLVPS external cable harness.

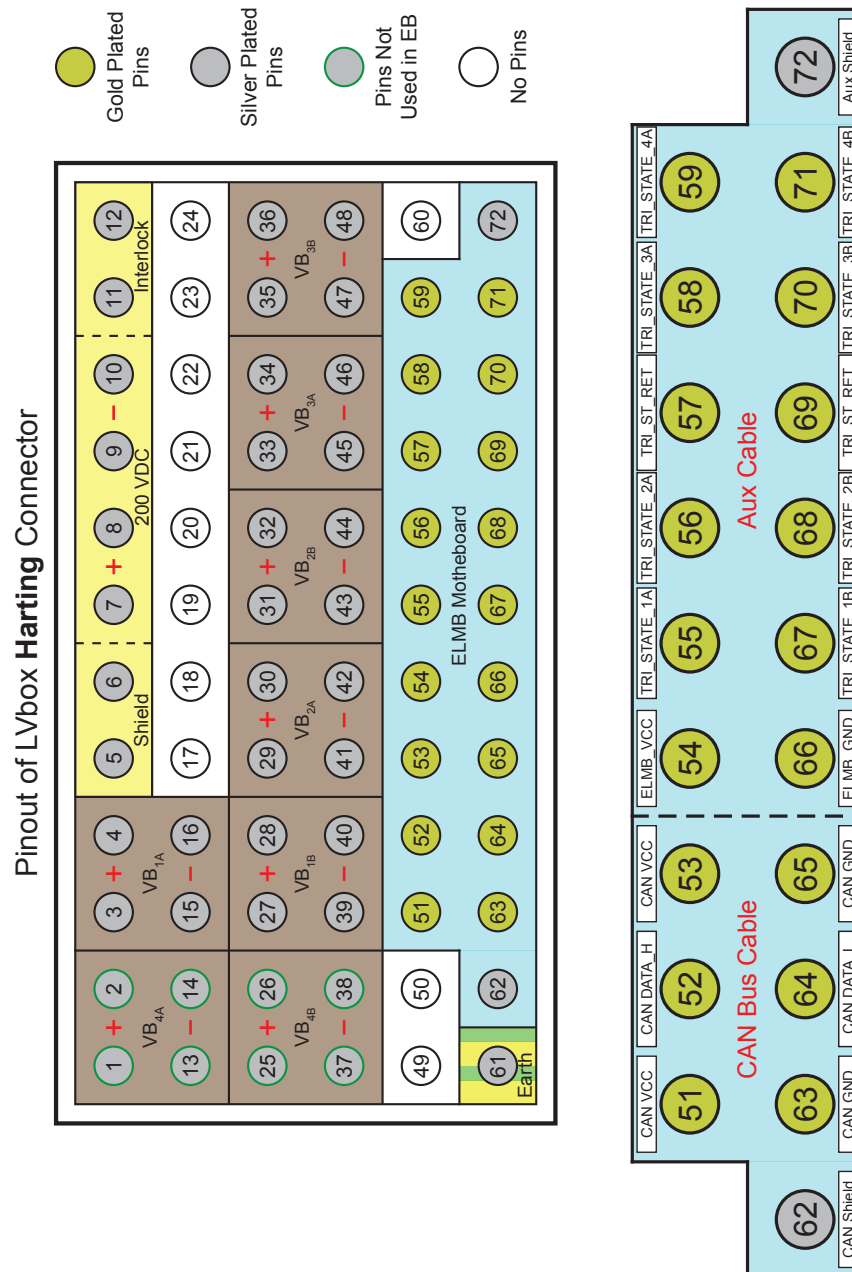


Figure B.5: Diagram of a phase-II Upgrade fLVPS Harting connector pin-out.

B.3 Embedded Local Monitoring Board 2 and its associated Motherboard

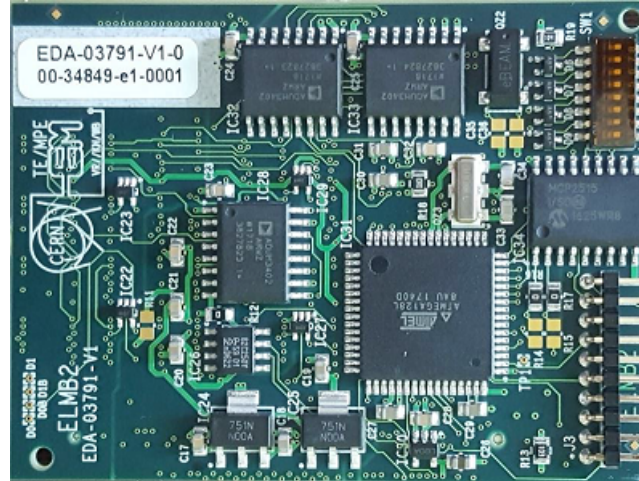


Figure B.6: Image of an ELMB2.

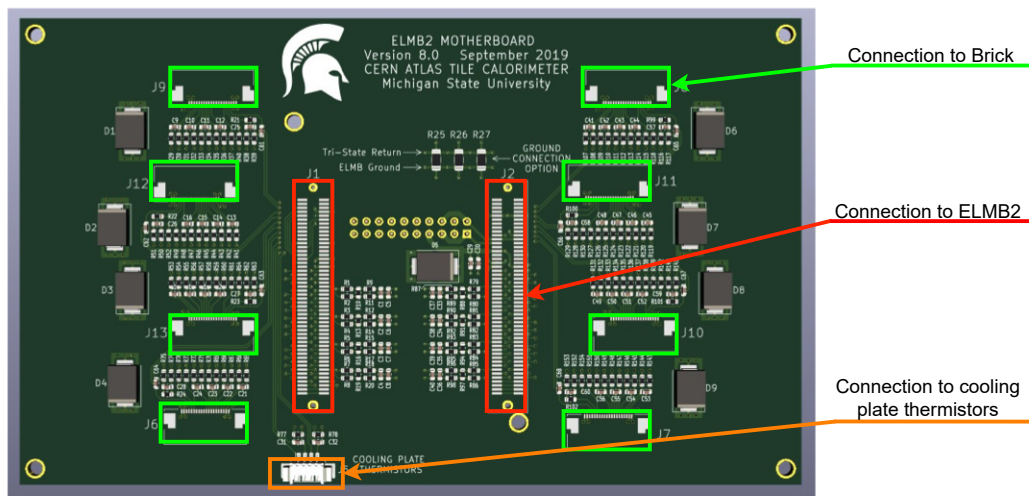


Figure B.7: Labelled Computer-Aided-Design image of an ELMB2 Motherboard.

B.4 fLVPS Fuseboard

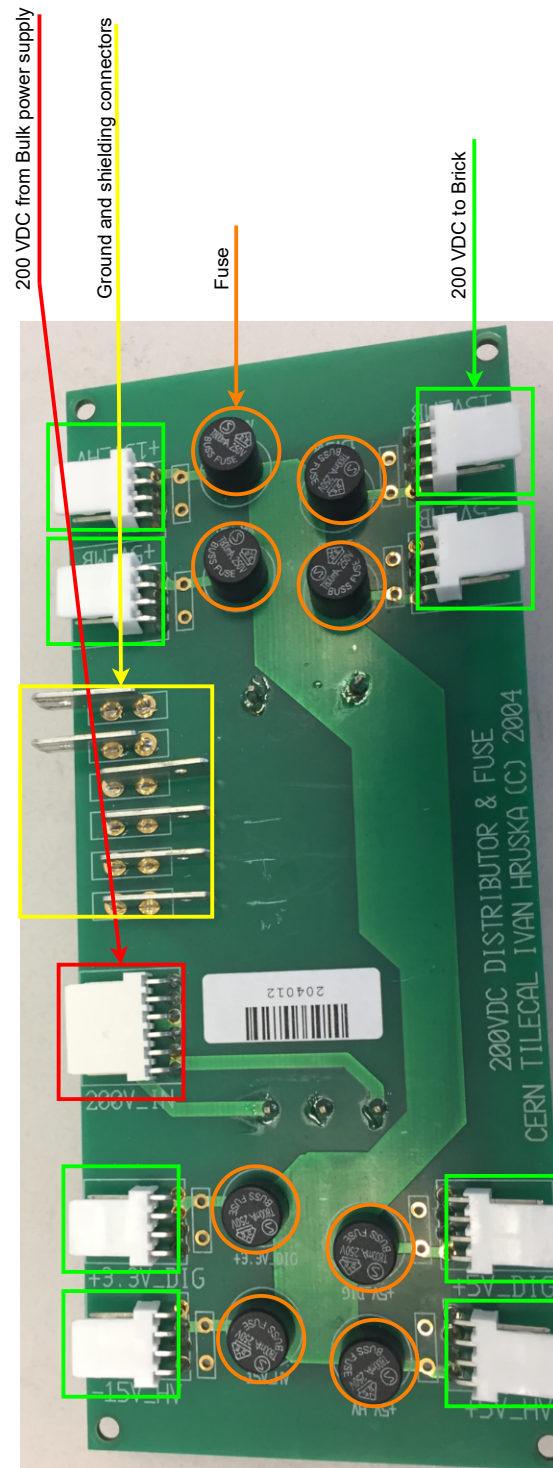


Figure B.8: Labelled image of an fLVPS Fuseboard.

B.5 TileCal Phase-II Upgrade Long-Barell Patch Panel

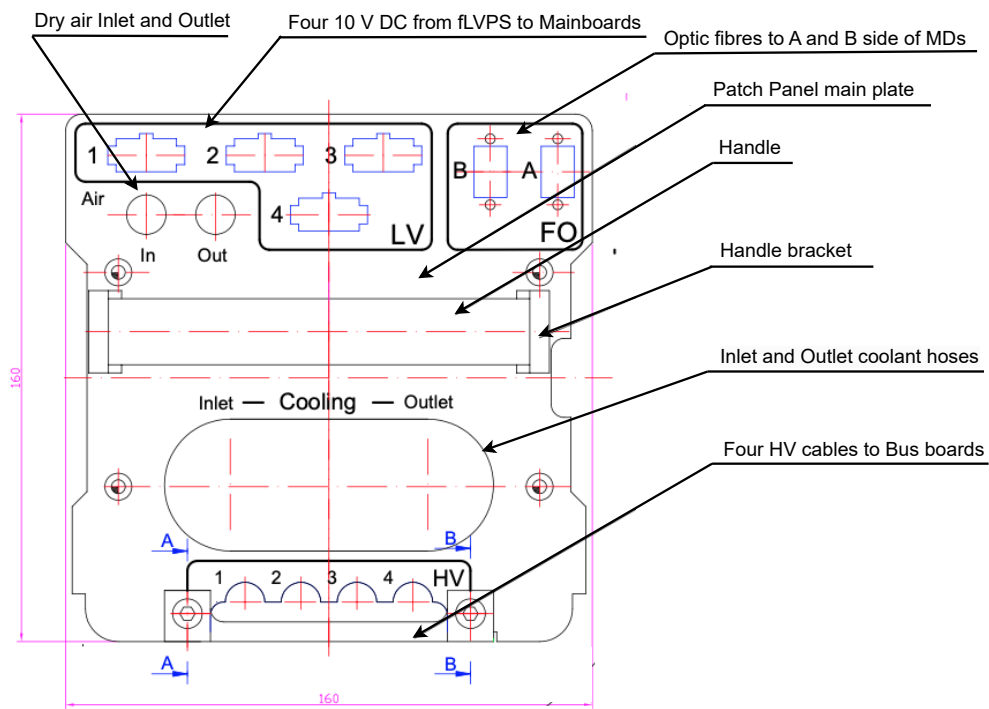


Figure B.9: Schematic of a TileCal Phase-II Upgrade Long-Barell Patch panel.

B.6 TileCal Module Services

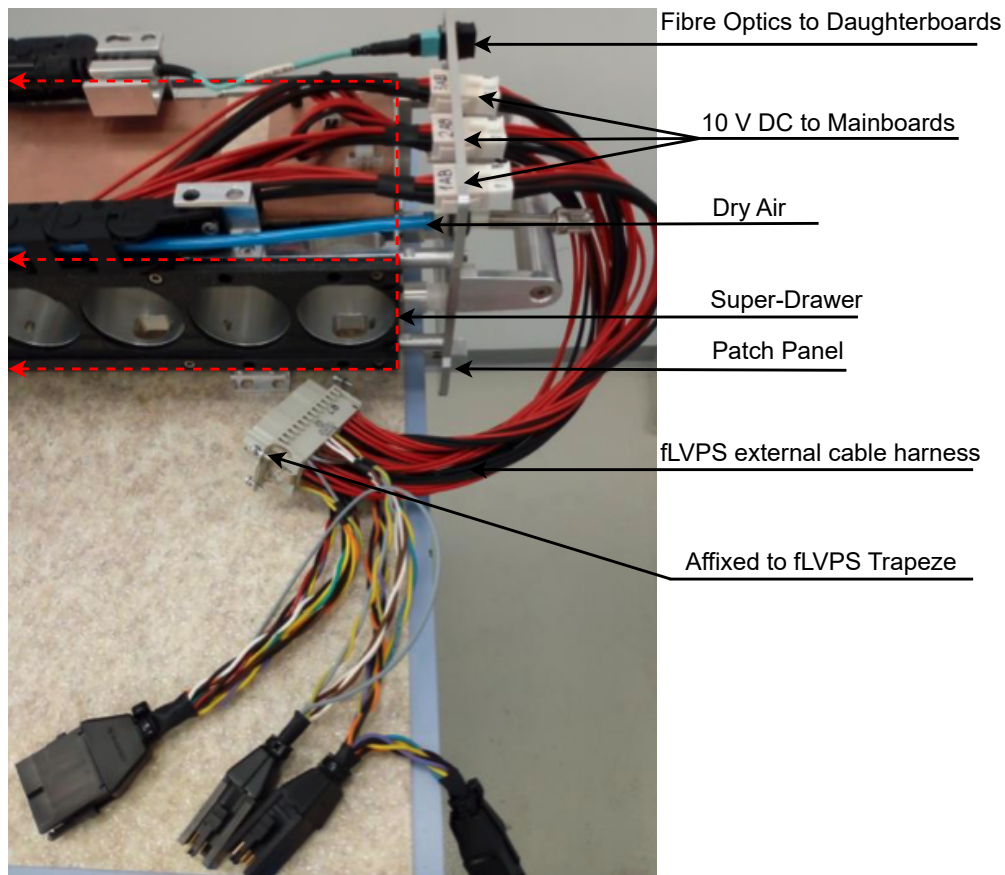


Figure B.10: Image of an extracted Extended-Barrel Super-Drawer, without front-end electronics or PMTs inserted, with a fLVPS external cable harness affixed. The optic fibres that fan out to the Daughterboards are visible as well as a dry air hose. Note that the High-Voltage cables that are routed to the PMT HV BUS boards are not connected in this image.

Appendix C

fLVPS Brick

C.1 Physical Description

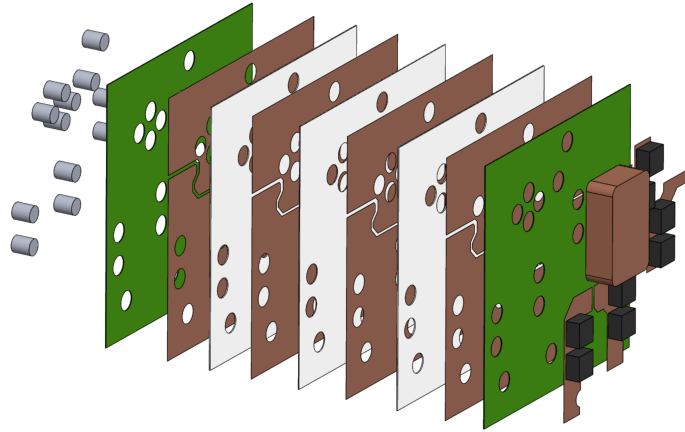


Figure C.1: Parametric solid model of a Brick [101].

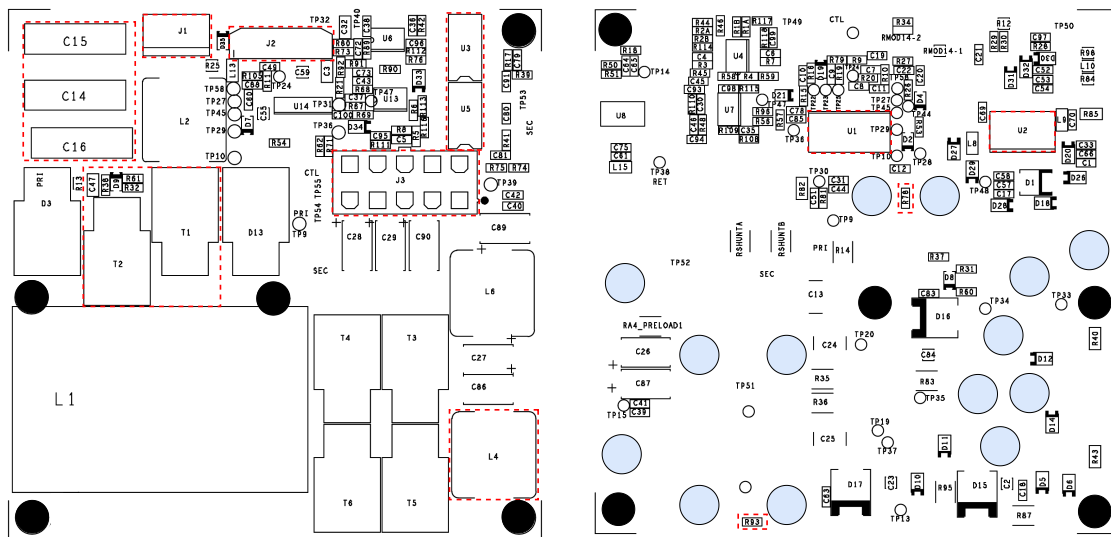


Figure C.2: Top (left) and Bottom (right) assembly layout of a V8.6 fLVPS Brick.

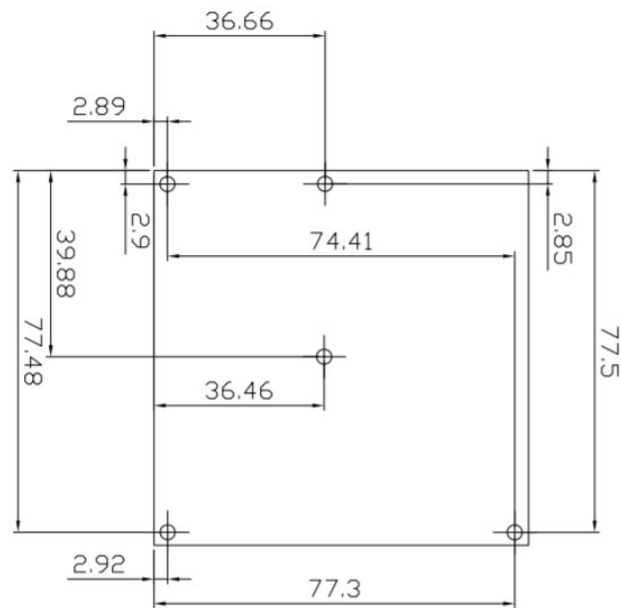


Figure C.3: Phase-II Upgrade fLVPS Brick dimensions and mounting hole locations.

Description	Value
Maximum Current at Minimum Stable Load	< 2 A
Frequency Standard Deviation at Minimum Stable Load	<1000 Hz
Duty Cycle Standard Deviation	< 0.4%
Output Voltage at Minimum Stable Load	9.8 V to 10.2 V
Input Voltage Range	180 V to 220 V
Output Over Voltage Protection Trip Point	11.5 V to 12 V
Input Over Voltage Protection Trip Point	234.76 V to 236.27 V
Over Current Protection Point	6.25 A to 6.75 A
Over Temperature Protection Trip Point	70°
Output Voltage Ripple (p2p) at Nominal Load (2.3 A)	< 0.5 V
Output Voltage Ripple (RMS) at Nominal Load (2.3 A)	<0.05 V
Average Duty Cycle at Nominal Load (2.3 A)	30% to 40%
Duty Cycle Standard Deviation at Nominal Load (2.3 A)	< 0.6%
Frequency at Nominal Load (2.3 A)	280 kHz to 320 kHz
Efficiency at Nominal Load (2.3 A)	>65%
Startup Delay	50 ms to 150 ms
Load Regulation	< 50 mV/A
Line Regulation	< 2 mV/V
Maximum Current Dynamics	< 0.3 A/us

Table C.1: V8.6.1 fLVPS Brick performance specifications.

C.2 Fundamentals of Transformers

A transformer is a passive electronic component that consist of at least two inductively coupled windings and possibly an iron core, as is the case with the fLVPS Brick. The input and output windings are referred to as the primary and secondary windings, respectively. The turns ratio of the magnetically coupled windings can be adjusted to obtain the desired relationship between input and output voltages. The Bricks transformer(L1) has a primary-to-secondary winding ratio of 14:2 indicating that it is a step-down transformer. The primary and secondary windings are galvanically separated, thus only the transfer of AC signals is possible.

When an AC voltage is applied to the primary windings of the transformer, a magnetic flux is generated, as described by Faraday's law of electromagnetic induction:

$$V_{pri} = N_{pri} \frac{d\phi_1}{dt} \quad (C.1)$$

Where V_{pri} is the voltage applied to the primary windings, N_{pri} is the number of turns of the primary windings and ϕ_1 is the generated electromagnetic flux. The induced alternating magnetic field permeates through the iron core to the secondary windings and induces a voltage at the secondary windings, as again indicated by Faraday's law of induction:

$$V_{sec} = N_{sec} \frac{d\phi_2}{dt} \quad (C.2)$$

Where V_{sec} is the voltage induced in the secondary windings, N_{sec} is the number of turns of the secondary windings and ϕ_2 is the magnetic flux that permeates the secondary windings. Assuming that the primary and secondary windings are perfectly inductively coupled (an ideal transformer) we have that:

$$\frac{d\phi_1}{dt} = \frac{d\phi_2}{dt} \quad (C.3)$$

The substitution of Equation C.1 and Equation C.2 into Equation C.3 yields:

$$\frac{V_{pri}}{V_{sec}} = \frac{N_{pri}}{N_{sec}} = n \quad (C.4)$$

Where n is defined as the primary-to-secondary turn ratio.

Appendix D

fLVPS Brick Thermal Performance Studies

D.1 Apparatus

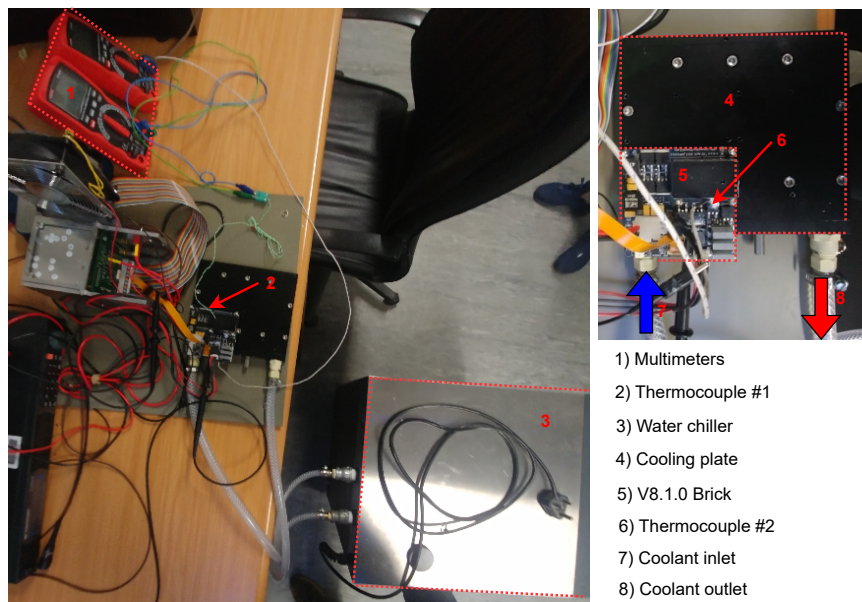


Figure D.1: Active cooling thermal performance study apparatus. This apparatus builds upon that which was presented in subsection 4.1.3 with the addition of a second thermocouple as well as active cooling of the Brick.

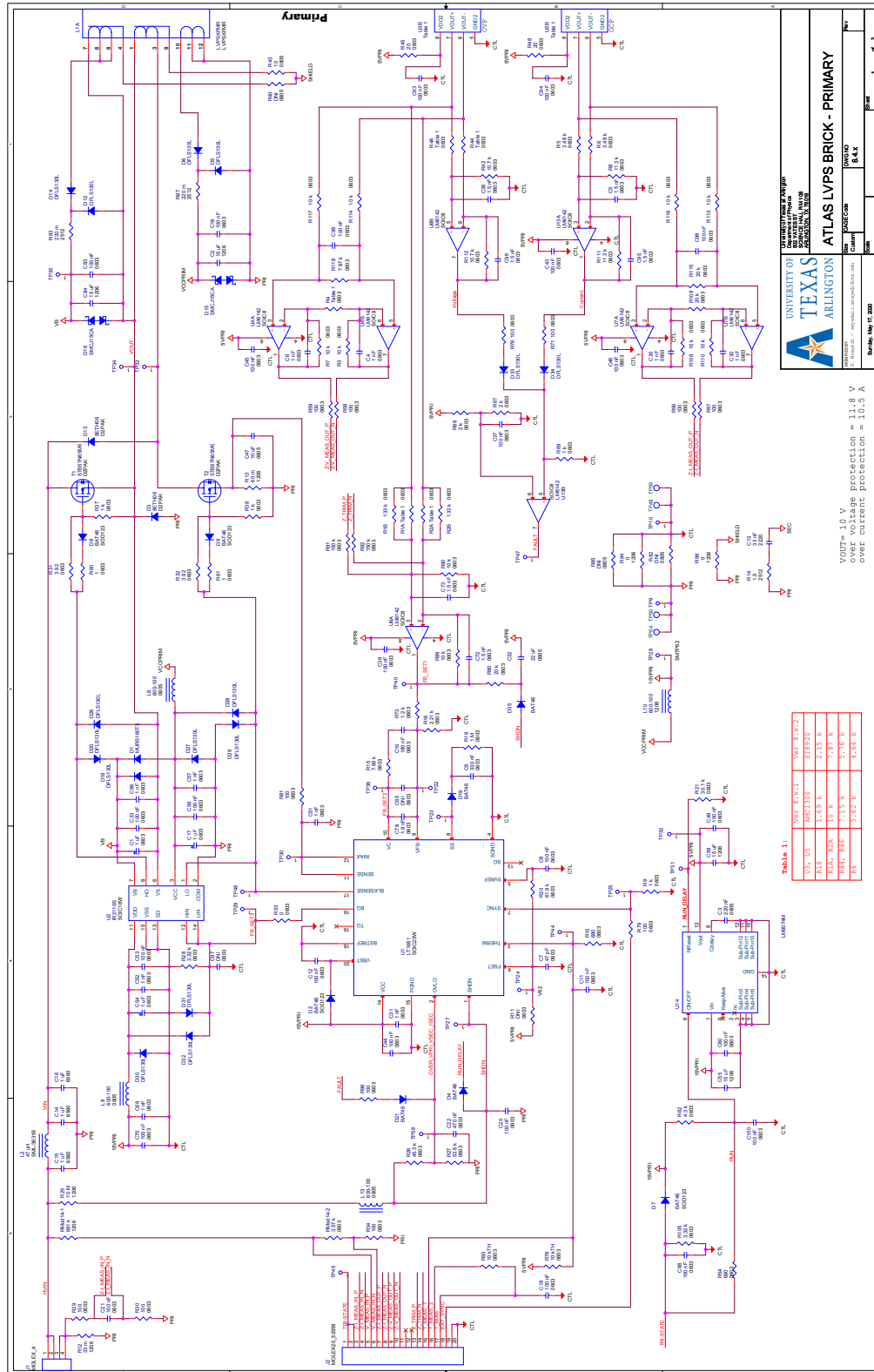
Appendix E

fLVPS Brick Schematics

See next page.





Figure E.3: Schematics of the primary side of the V8.4.2 *flVPS* Brick.

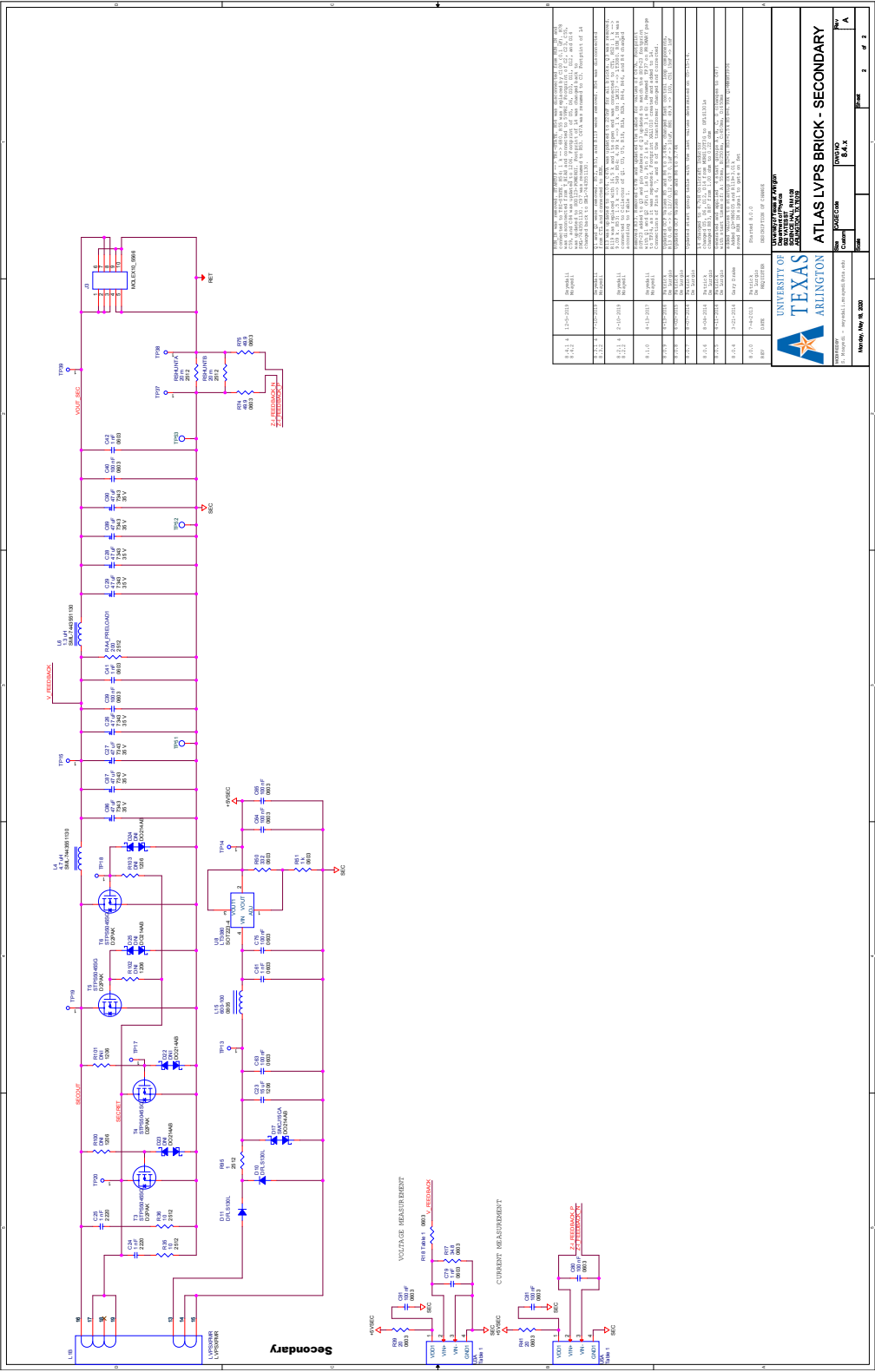


Figure E.4: Schematics of the secondary side of the V8.4.2 fLVPS Brick.

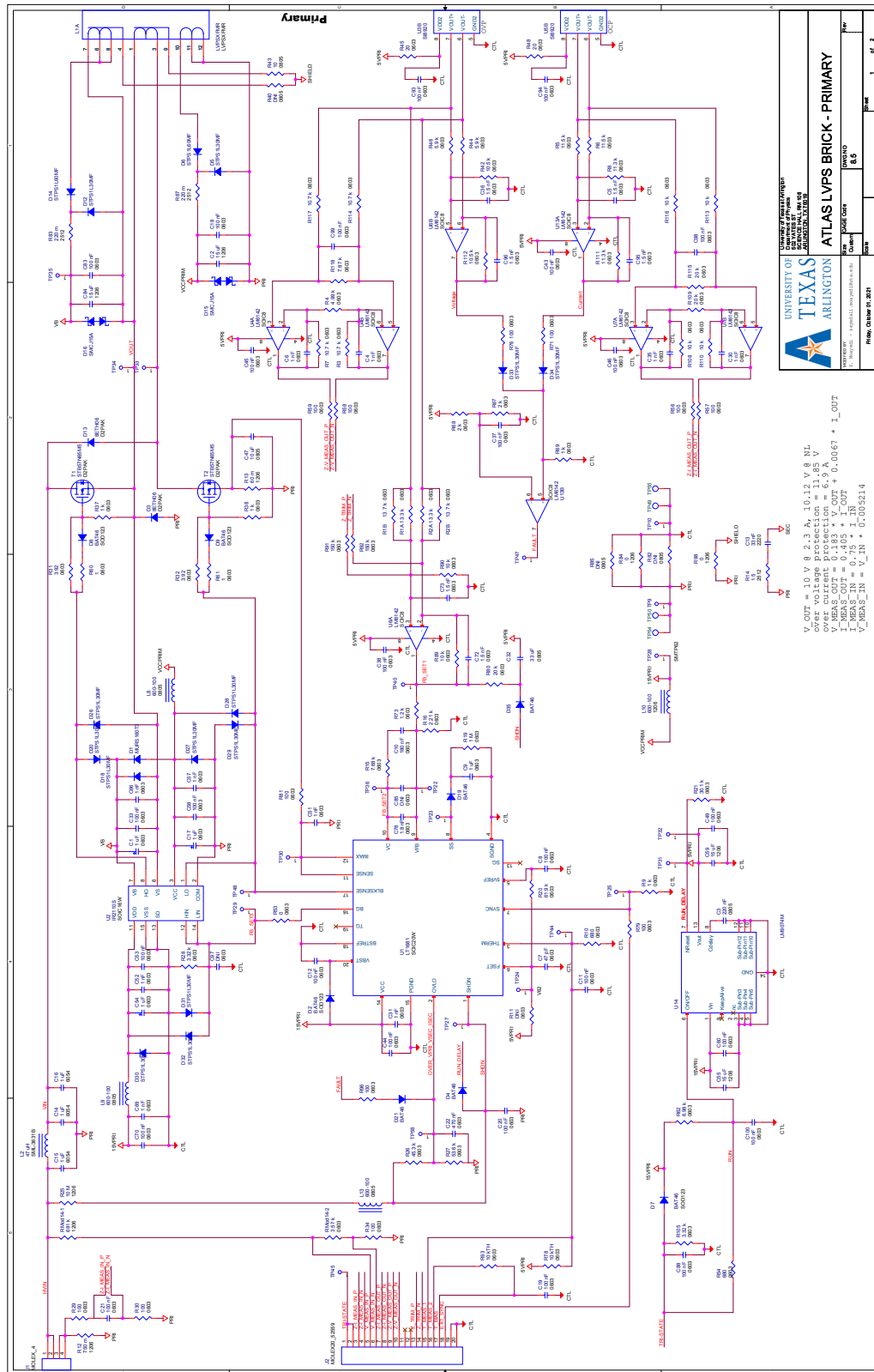
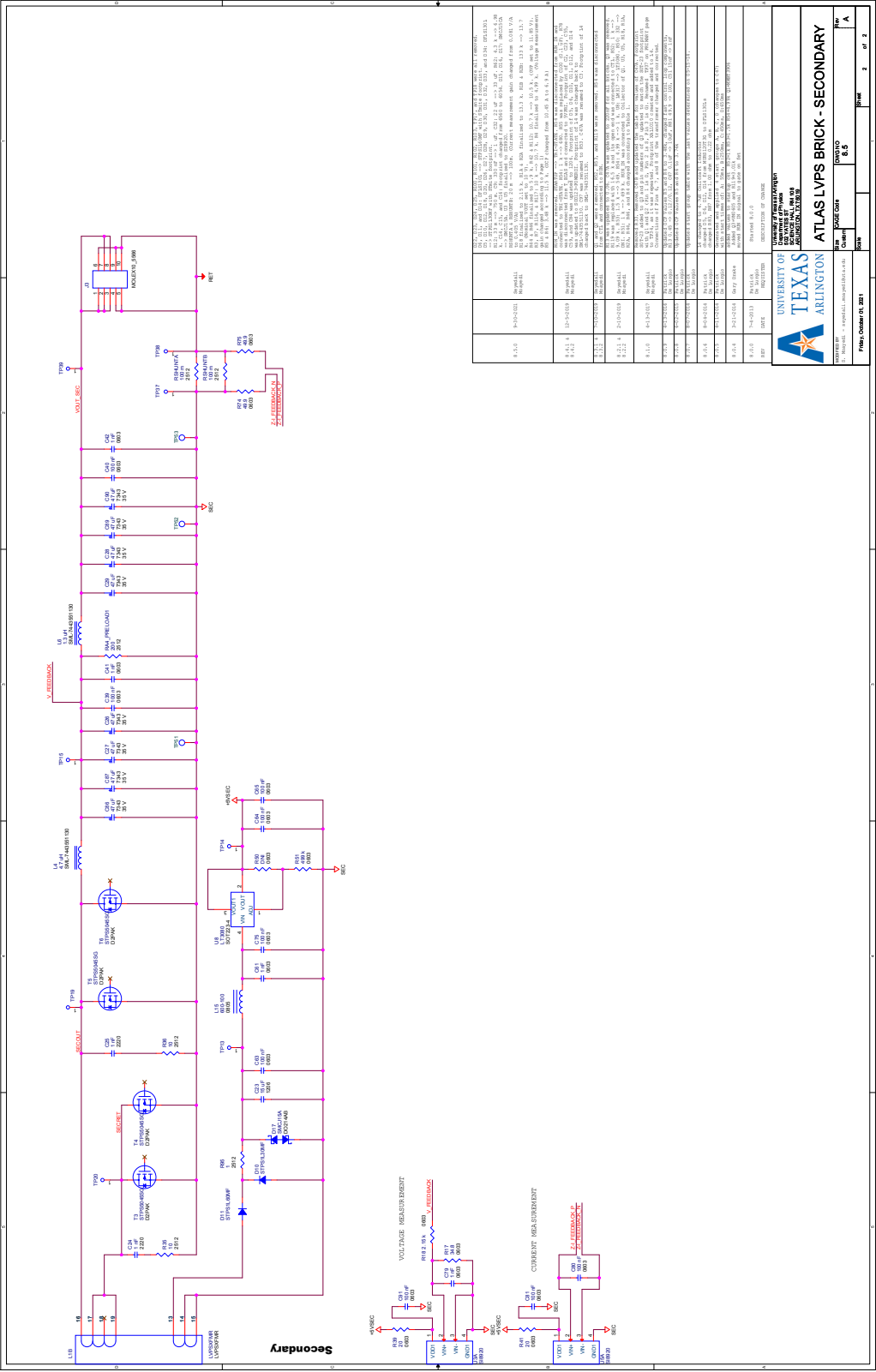


Figure E.5: Schematics of the primary side of the V8.5.0 fLVPS Brick.





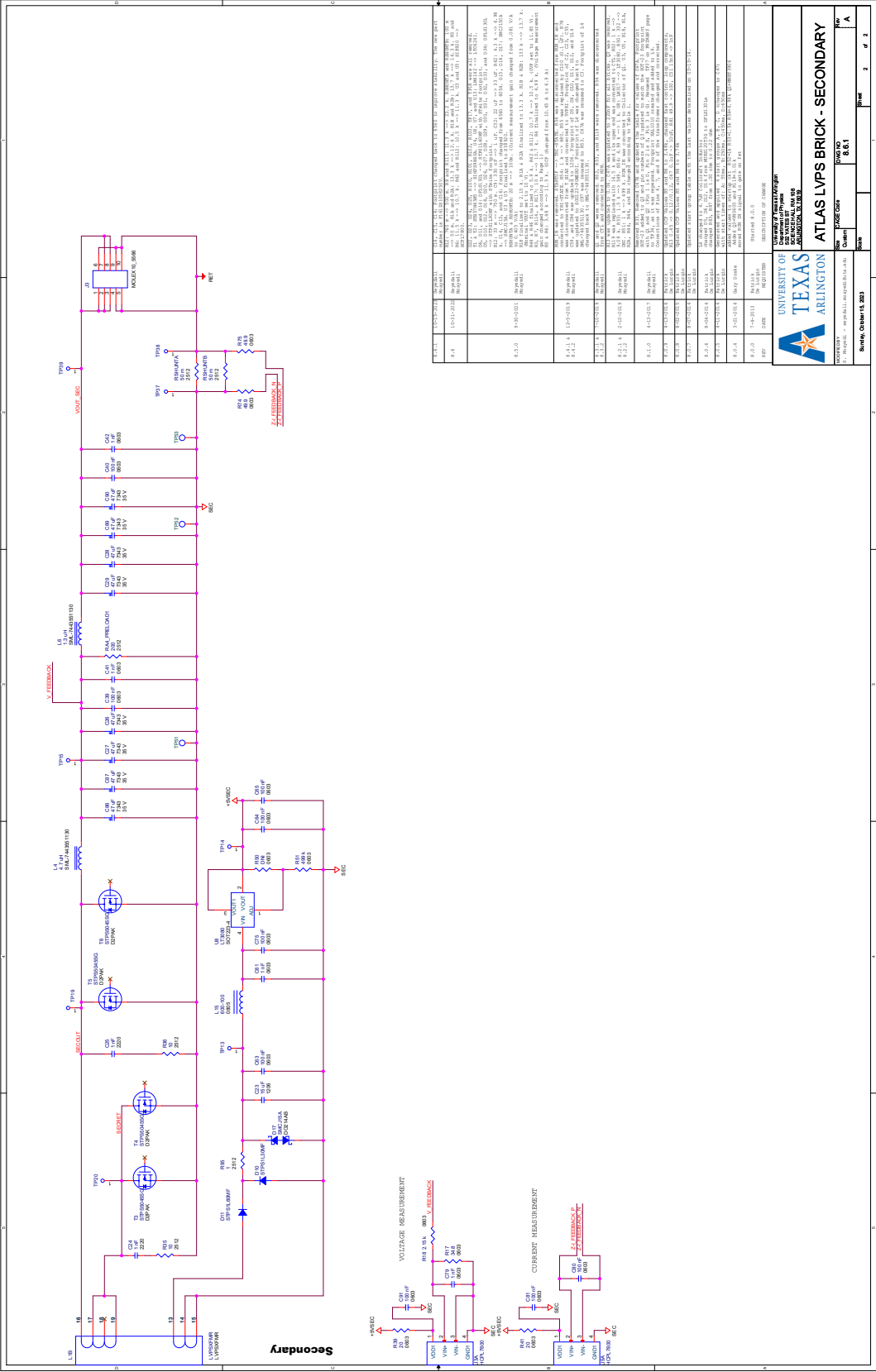


Figure E.8: Schematics of the secondary side of the V8.6.1 *flVPS* Brick.

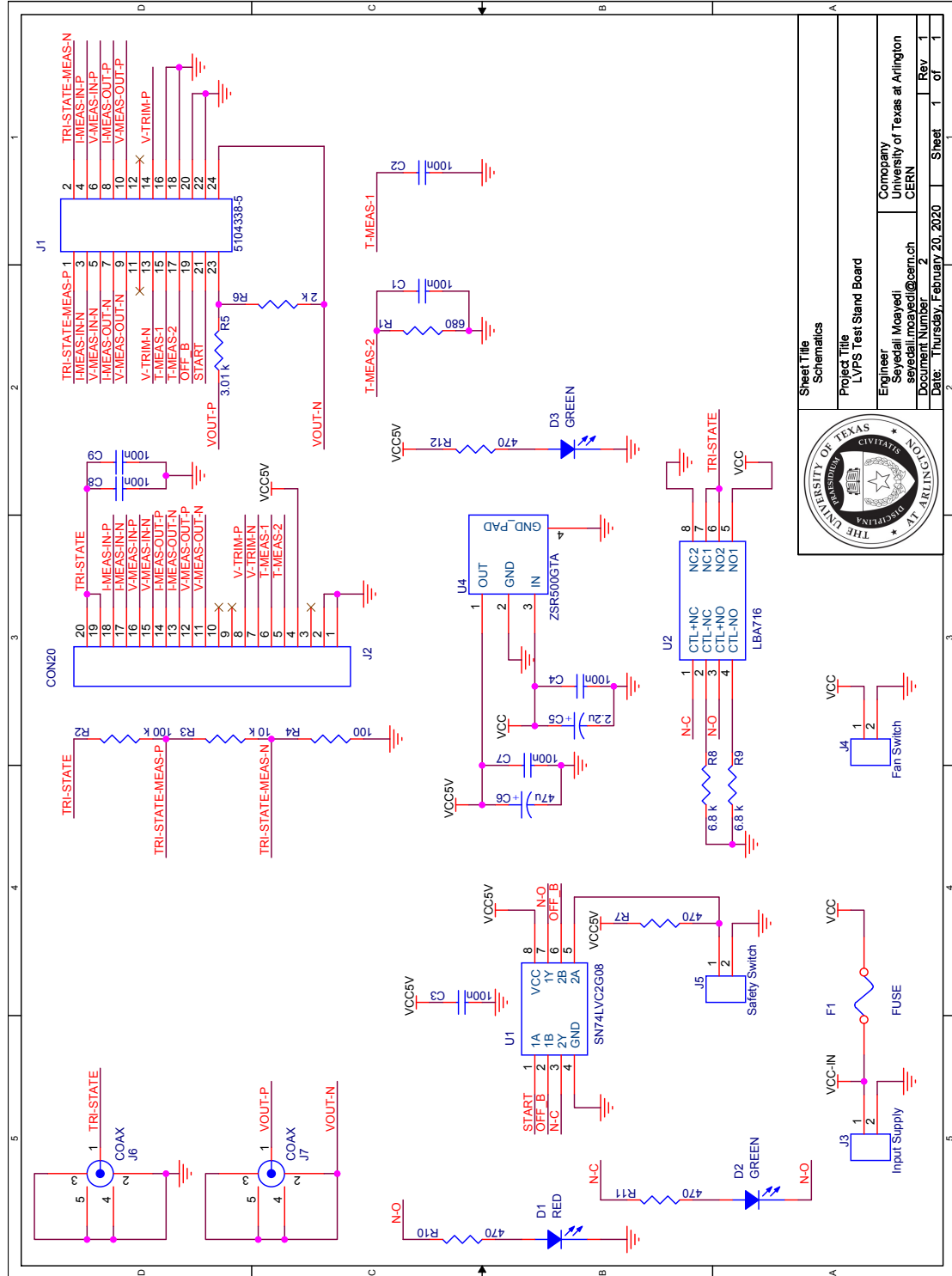


Figure E.9: Schematic of the fLVPS Brick Initial/Final test station Interface Board.

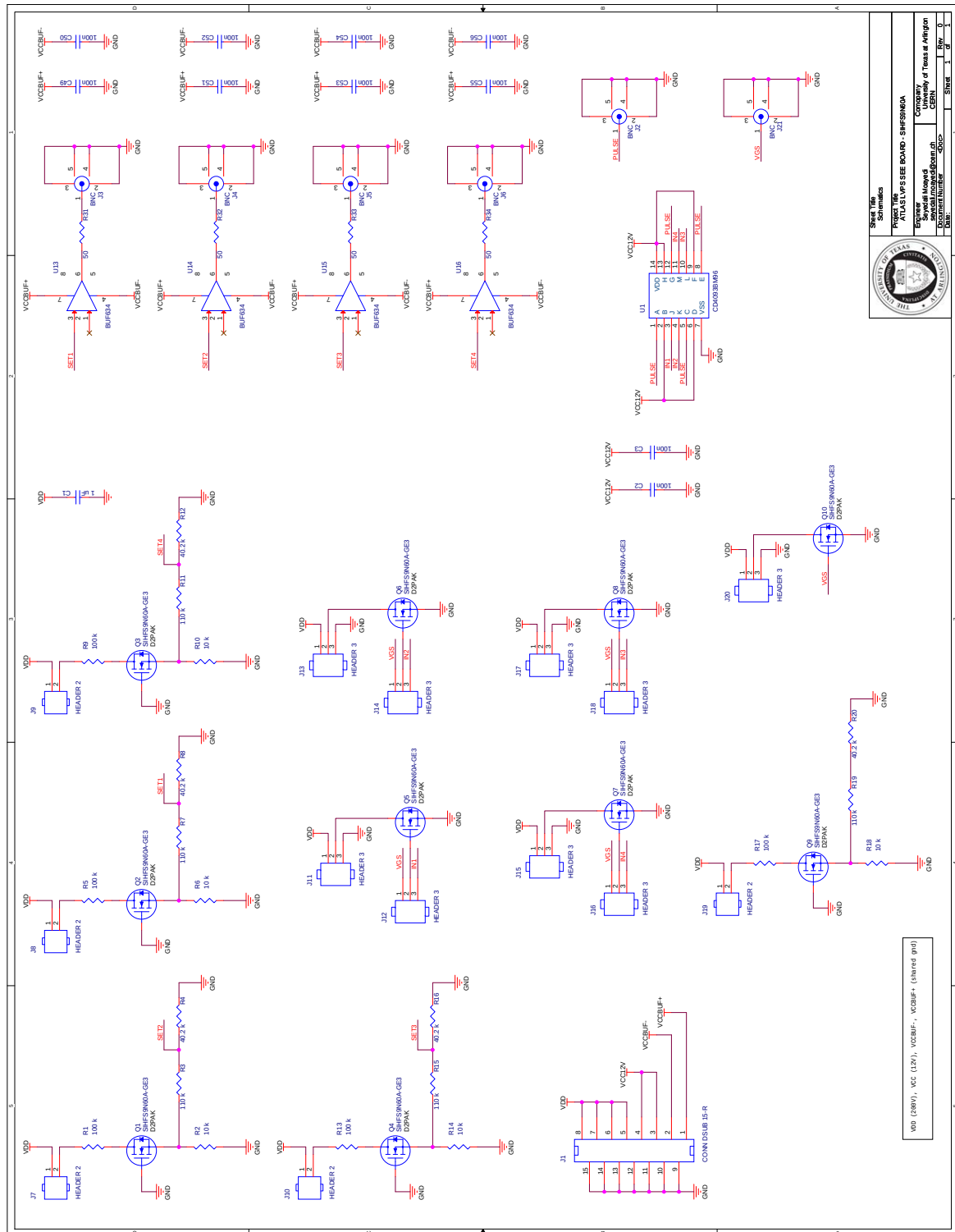


Figure E.10: Single Event Effect test Printed Circuit Board schematic.

Appendix F

fLVPS Brick Burn-in Station

F.1 Burn-in Station Mechanics, Hardware and Wiring

..

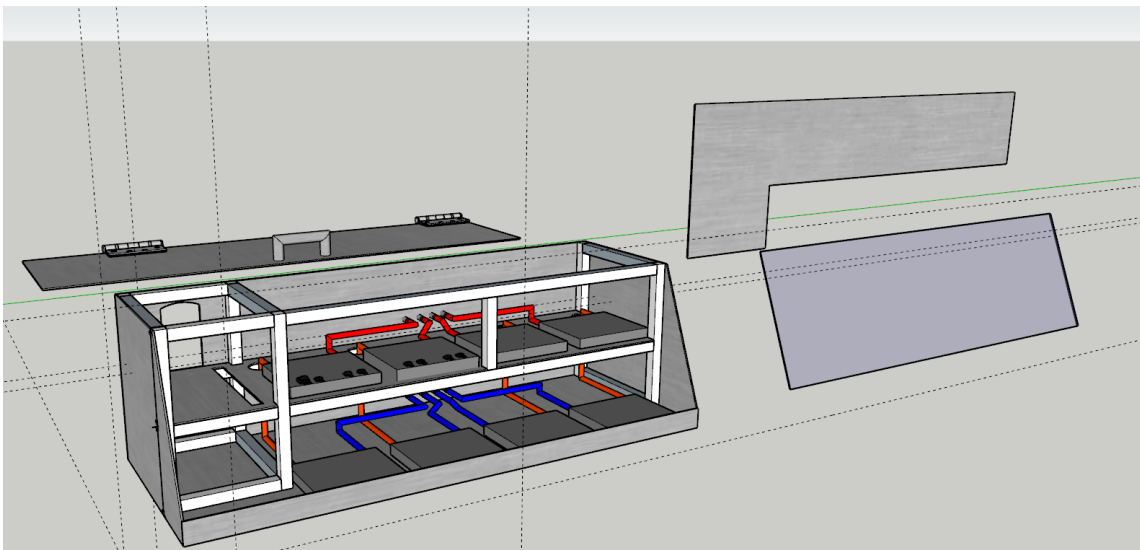


Figure F.1: A Computer-Aided Design of the Burn-in test bed with the cooling plates and pipes installed.

PRODUCED BY AN AUTODESK STUDENT VERSION

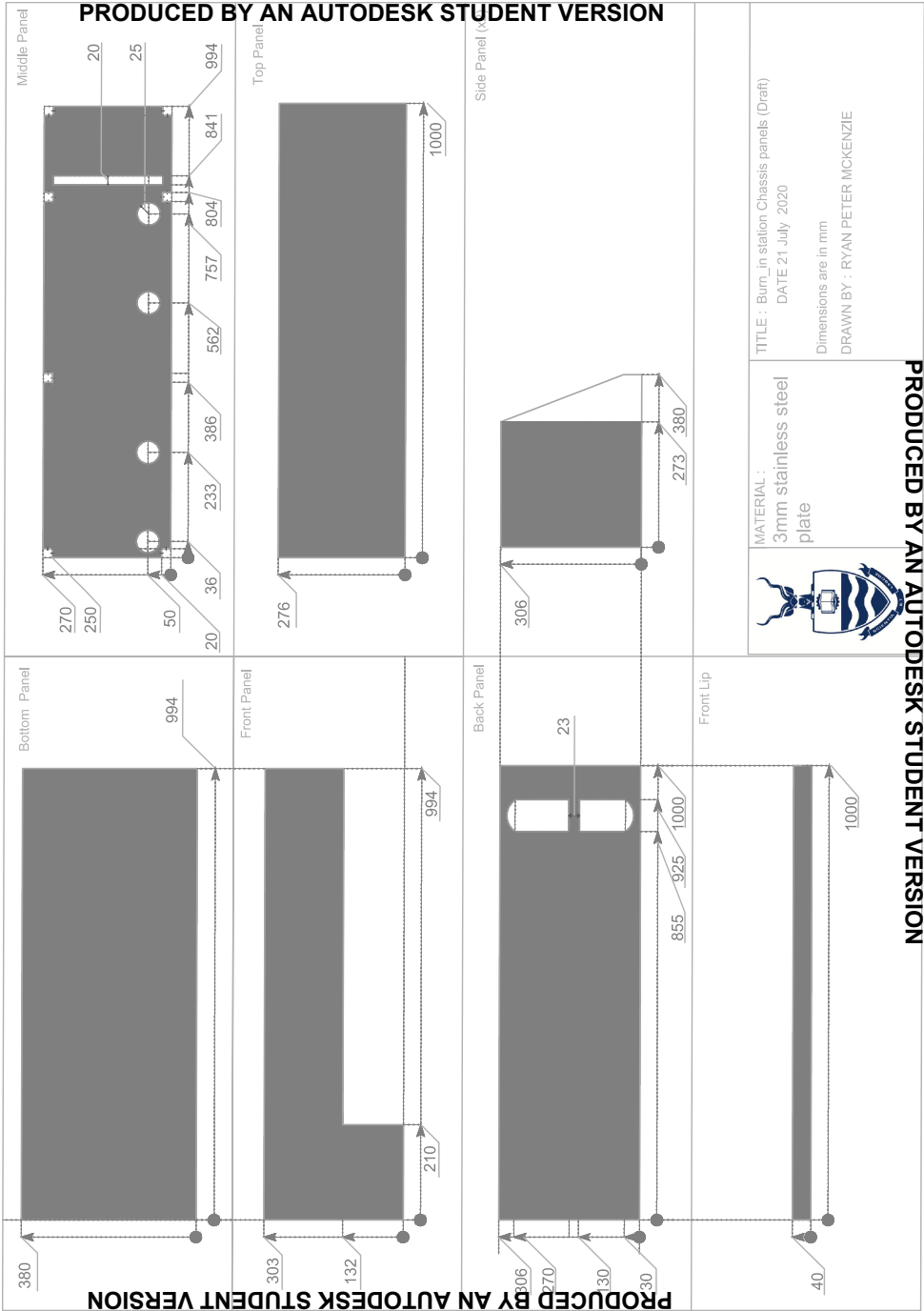
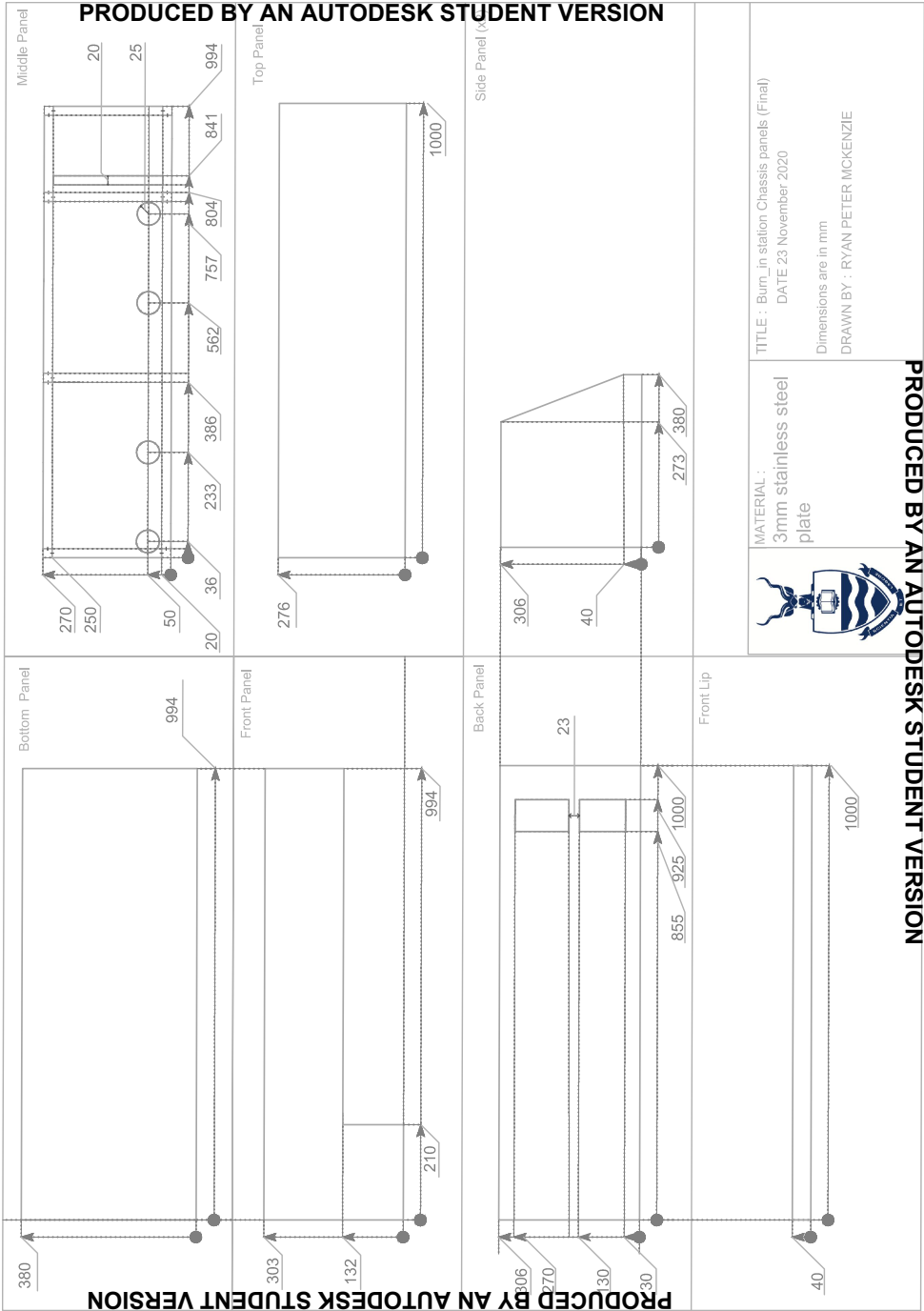
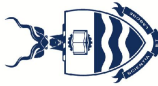


Figure F.2: Burn-in station test-bed panel schematics.

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PRODUCED BY AN AUTODESK STUDENT VERSION



MATERIAL :
3mm stainless steel
plate

TITLE : Burn_in station Chassis panels (Final)
DATE 23 November 2020
Dimensions are in mm
DRAWN BY : RYAN PETER MCKENZIE

Figure F.3: Burn-in station test-bed frame schematics.

SA-ATLAS

University of the Witwatersrand

LVPS Brick Burn-in Station

Wiring Document



Author: Ryan Mckenzie

Date: 27/01/2020

Version 2.0

Notes:

- **TLDR- The final wiring and connector BOM is located on pages 11 and 12;**
- All of the boards receive an input AC power supply;
- Each Brick-interface board received 200 VDC which is routed to the LVPS Brick;
- All the boards have input AC power connections. These were not included in the first block diagram for sake of simplicity, please see the separate Burn-in station 220 V AC block diagram;
- Each board has an AC/DC converter which can handle a 110V and 220V input. This is important due to the input AC power being sourced directly from the laboratory mains;
- Remember to include USB-B male to USB-C male cable for connection from Main board to PC.

Diagram 1: Burn-in Station Block Diagram, Seyedali Moeyedi

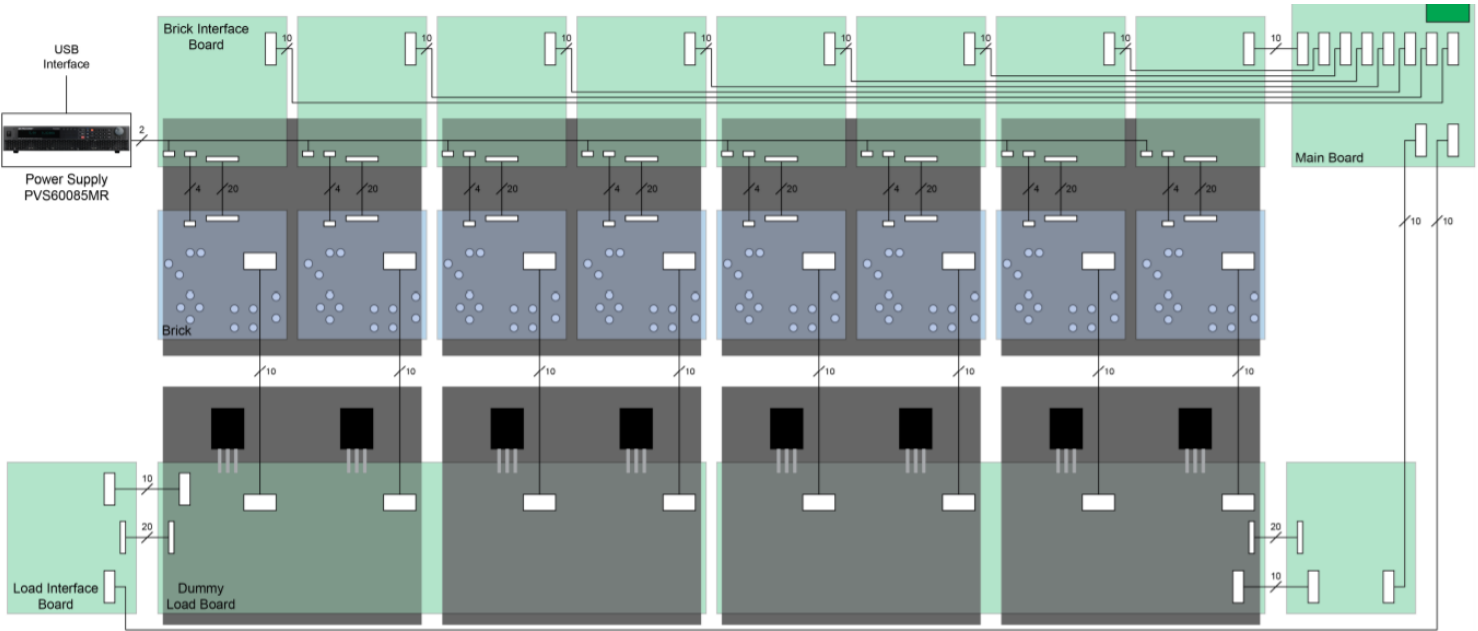
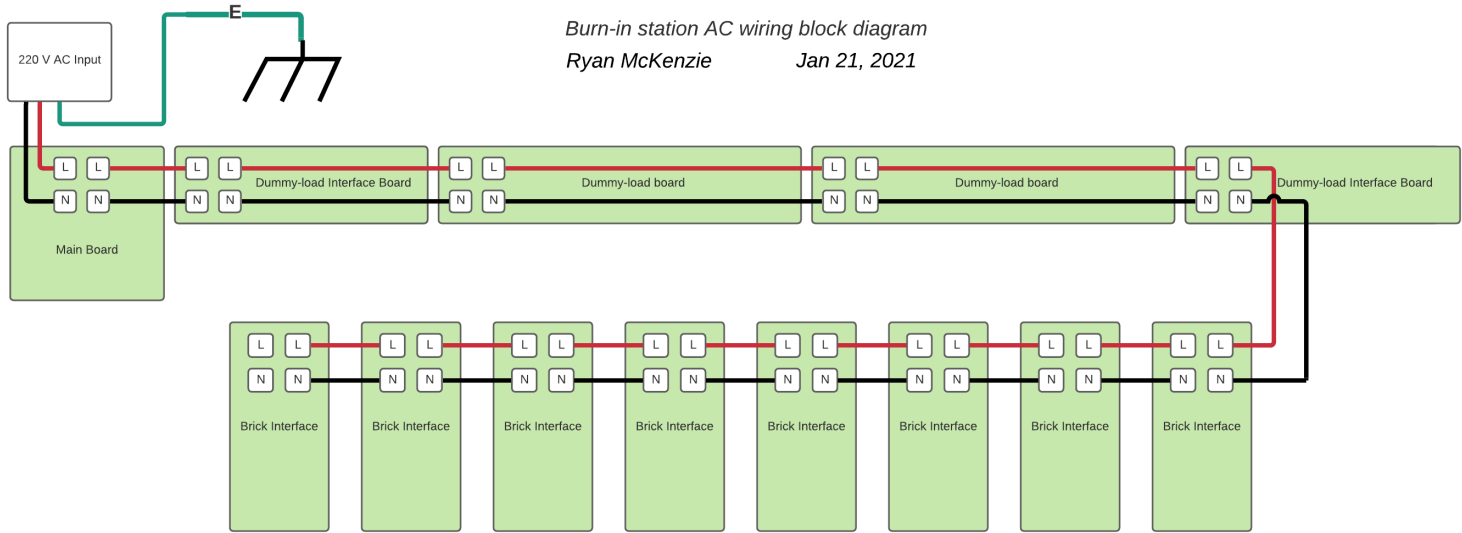


Diagram 2 : Burn-in station 220 V AC block diagram



Single Main-Board Connectors as per BOM

Reference	Quantity	Manf. Part Number	Description
MB:J1	1	874270442	Connector Header Through Hole 4 position 0.165" (4.20mm)
MB: J2,J3,J4,J5,J6,J7,J8,J9 J10,J11,J12	11	302-S101	Connector Header Through Hole 10 position 0.100" (2.54mm)

Single Dummy-Load Board Connectors as per BOM

Reference	Quantity	Manf. Part Number	Description
DL:J1	1	0525592052	20 Position FFC, FPC Connector Contacts, Vertical - 1 Sided 0.020" (0.50mm) Surface Mount
DL:J2	1	302-S101	Connector Header Through Hole 10 position 0.100" (2.54mm)
DL: J3	1	874270442	Connector Header Through Hole 4 position 0.165" (4.20mm)
DL: J4,J5,J6,J7	4	39281103	Connector Header Through Hole 10 position 0.165" (4.20mm)

Single Brick Interface Board connectors as per BOM

Reference	Quantity	Manf. Part Number	Description
BI: J1	1	0525592052	20 Position FFC, FPC Connector Contacts, Vertical - 1 Sided 0.020" (0.50mm) Surface Mount
BI:J3	1	68000-102HLF	Connector Header Through Hole 2 position 0.100" (2.54mm)
BI: J4,J5	2	302-S101	Connector Header Through Hole 10 position 0.100" (2.54mm)
BI: J6,J7,J8	3	874270442	Connector Header Through Hole 4 position 0.165" (4.20mm)

Single Dummy-Load Interface Board connectors as per BOM

Reference	Quantity	Manf. Part Number	Description
LI:J1	1	0525592052	20 Position FFC, FPC Connector Contacts, Vertical - 1 Sided 0.020" (0.50mm) Surface Mount
LI: J2,J4,J5	3	302-S101	Connector Header Through Hole 10 position 0.100" (2.54mm)
LI: J3	1	68000-102HLF	Connector Header Through Hole 2 position 0.100" (2.54mm)
LI: J6	1	874270442	Connector Header Through Hole 4 position 0.165" (4.20mm)



Figure 1 Manf. Part Number 874270442



Figure 2: Manf. Part Number 302-S101



Figure 3 Manf. Part Number 0525592052



Figure 4: Manf. Part Number 39281103

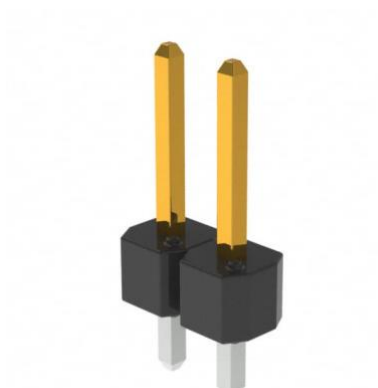


Figure 5: Manf. Part Number 68000-102HLF

Corresponding Connectors for 2 Burn-in stations

❖ Note: The corresponding connectors stated are by no means the only viable option

ID No#	PCB Mounted connector	Manf. Part Number	Mating component	Manf. Part Number	Total unit number (X2 Burn-in stations)
1a	Connector Header Through Hole 4 position 0.165" (4.20mm)	874270442	CONN RCPT HSG 4POS 4.20MM	39-01-3042	58
1b			CONN SOCKET 18-20AWG CRIMP TIN	457501112	58(4) = 232
2	Connector Header Through Hole 10 position 0.100" (2.54mm)	302-S101	Wurth Elektronik 10-Way IDC Connector Socket for Cable Mount, 2-Row	61201023021	1 Tray of 96 units
3	20 Position FFC, FPC Connector Contacts, Vertical - 1 Sided 0.020" (0.50mm) Surface Mount	0525592052	N/A	N/A	N/A
4a	Connector Header Through Hole 10 position 0.165" (4.20mm)	39281103	Molex, Mini-Fit Jr Female Connector Housing, 4.2mm Pitch, 10 Way, 2 Row	39-01-2100	16
4b			CONN SOCKET 22-26AWG CRIMP GOLD	0460182541	16(10) = 160
5a	Connector Header Through Hole 2 position 0.100" (2.54mm)	68000-102HLF	CONN RECPT 2POS 2.54MM CRIMP	65039-035LF	20
5b			CONN SOCKET 22-26AWG CRIMP GOLD	47745-000LF	20(2) = 40



Figure 6: Manf. Part Number 39-01-3042



Figure 7: Manf. Part Number 0457501112



Figure 8: Manf. Part Number 61201023021



Figure 9: Manf. Part Number 39-01-2100



Figure 10: Manf. Part Number 65039-035LF

Additional connectors for 2 Burn-in stations

ID no#	Manf.	Manf. Part number	Description	Location	Total unit number (2x Burn-in stations)
6	Molex	22-01-3047	Molex, KK 254 Female Connector Housing, 2.54mm Pitch, 4 Way, 1 Row	200 VDC Connector between brick interface board and LVPS brick	16
7	Molex	08-55-0102	Molex KK 254 Female Crimp Terminal Contact 22AWG	22-01-3047 Insert	16(4) = 64



Figure 11: Manf. Part Number 22-01-3047



Figure 12: Manf. Part Number 08-55-0102

Required Cables for 2 Burn-in stations

ID no#	Manf.	Manf. Part number	Description	Location	Total unit number (2x Burn-in stations)
8	Würth Elektronik	687720200002	Würth Elektronik 6877 FFC Jumper Cable, 0.5mm Pitch, 20 Way, 200mm Cable Length, 500 mA, 60 V ac	Between interface board – Dummy_load (4)and interface-board and Bricks (16) + spare	25
9	RS Pro	7481964	RS PRO Tinned Copper Test Lead Wire 1 mm ² CSA 500 V 19 A Red Silicone, 332 Strands 5m	Parallel PCB AC power and HV DC power	12
10	RS Pro	7481973	RS PRO Tinned Copper Test Lead Wire 1 mm ² CSA 500 V 19 A Black Silicone, 332 Strands 5m	Parallel PCB AC power and HV DC power	12
11	RS Pro	196-4684	RS PRO Arctic Grade Electrical Wiring Cable, 3 Core, Orange, 100m, 2.5 mm ² CSA	Input power cable from mains to Burn-in station	1
12	RS Pro	790-3726	Roline Male USB A to Male USB B USB Cable, 3m	Main board connection to PC.	2
13	RS Pro	214-0677	RS PRO 10 Way Unscreened Flat Ribbon Cable, 12.7 mm Width, 25m	Between main board and Interface Boards	1

Sundries for 2 Burn-in stations

ID no#	Manf.	Manf. Part number	Description	Total unit number (2x Burn-in stations)
14			Plug	2
15			Ring terminal	2
16	RS Pro	822-9631	RS PRO M12 Cable Gland With Locknut, Nylon, IP68	1
17	RS Pro	144-3712	RS PRO Plastic Flexible, Split Conduit Black 10.7mm x 10m 3.3mm	2



Figure 11: RS PRO M12 Cable Gland With Locknut, Nylon, IP68



Figure 14: RS PRO Plastic Flexible, Split Conduit Black 10.7mm x 10m 3.3mm

Final BOM (2 x Burn-in stations)

- ❖ Note: The lengths of cable stated below have not been explicitly calculated but have rather been assumed while accounting for shortcomings by ordering approximately 50% over and above said assumption. This has been deemed acceptable as spare cabling will be of great value to have on-hand.

ID no#	Manf.	Manf. Part number	Description	Total number of units
1a	Molex	39-01-3042	CONN RCPT HSG 4POS 4.20MM	6 packs of 10
1b	Molex	457501112	CONN SOCKET 18-20AWG CRIMP TIN	3 packs of 100
2	Würth Elektronik	61201023021	Würth Elektronik 10-Way IDC Connector Socket for Cable Mount, 2-Row	1 tray of 96
4a	Molex	39-01-2100	Molex, Mini-Fit Jr Female Connector Housing, 4.2mm Pitch, 10 Way, 2 Row	4 packs of 5
4b	Molex	39-00-0039	Molex MINI-FIT Series, 5556 Series Number, Crimp Contact, Female, 24AWG to 18AWG, Tin Plating	2 packs of 100
5a	Amphenol ICC (FCI)	65039-035LF	CONN RECPT 2POS 2.54MM CRIMP	2 Pcks of 10
5b	Amphenol ICC (FCI)	47745-000LF	CONN SOCKET 22-26AWG CRIMP GOLD	5 packs of 10
6	Molex	22-01-3047	Molex, KK 254 Female Connector Housing, 2.54mm Pitch, 4 Way, 1 Row	2 packs of 10
7	Molex	08-55-0102	Molex KK 254 Female Crimp Terminal Contact 22AWG	1 pack of 100
8	Würth Elektronik	687720200002	Würth Elektronik 6877 FFC Jumper Cable, 0.5mm Pitch, 20 Way, 200mm Cable Length, 500 mA, 60 V ac	30

9	RS Pro	7481964	RS PRO Tinned Copper Test Lead Wire 1 mm ² CSA 500 V 19 A Red Silicone, 332 Strands 5m	12 x 5m lengths
10	RS Pro	7481973	RS PRO Tinned Copper Test Lead Wire 1 mm ² CSA 500 V 19 A Black Silicone, 332 Strands 5m	12 x 5m lengths
11	RS Pro	196-4684	RS PRO Arctic Grade Electrical Wiring Cable, 3 Core, Orange, 100m, 2.5 mm ² CSA	1 x 100m length
12	RS Pro	790-3726	Roline Male USB A to Male USB B USB Cable, 3m	2 x USB cables
13	RS Pro	214-0677	RS PRO 10 Way Unscreened Flat Ribbon Cable, 12.7 mm Width, 25m	1 x 25m length
16	RS Pro	822-9631	RS PRO M12 Cable Gland With Locknut, Nylon, IP68	1 pack of 10
17	RS Pro	144-3712	RS PRO Plastic Flexible, Split Conduit Black 10.7mm x 10m 3.3mm	2 x 10 m

Line item 8 correction

ID no#	Manf.	Manf. Part number	Description	Total unit number (2x Burn-in stations)
8*	RS Pro	179-2560	RS PRO FFC Jumper Cable, 0.5mm Pitch, 200mm Cable Length	30
8**	Wurth Elektronik	7427221	Wurth Elektronik 3 W 800 Ferrite Sleeve, 10 max. wires, Inner dims. 14 x 1mm	20

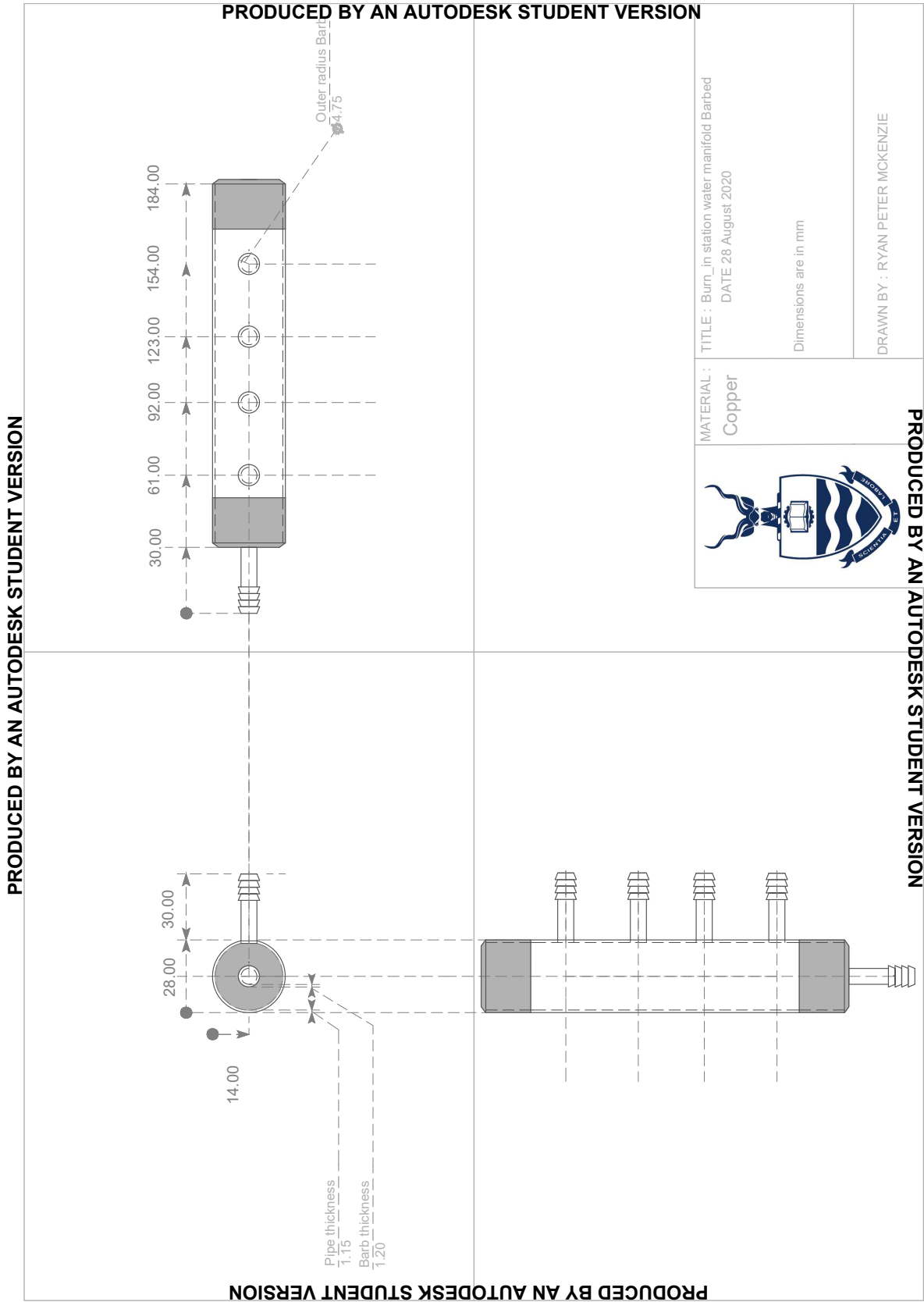
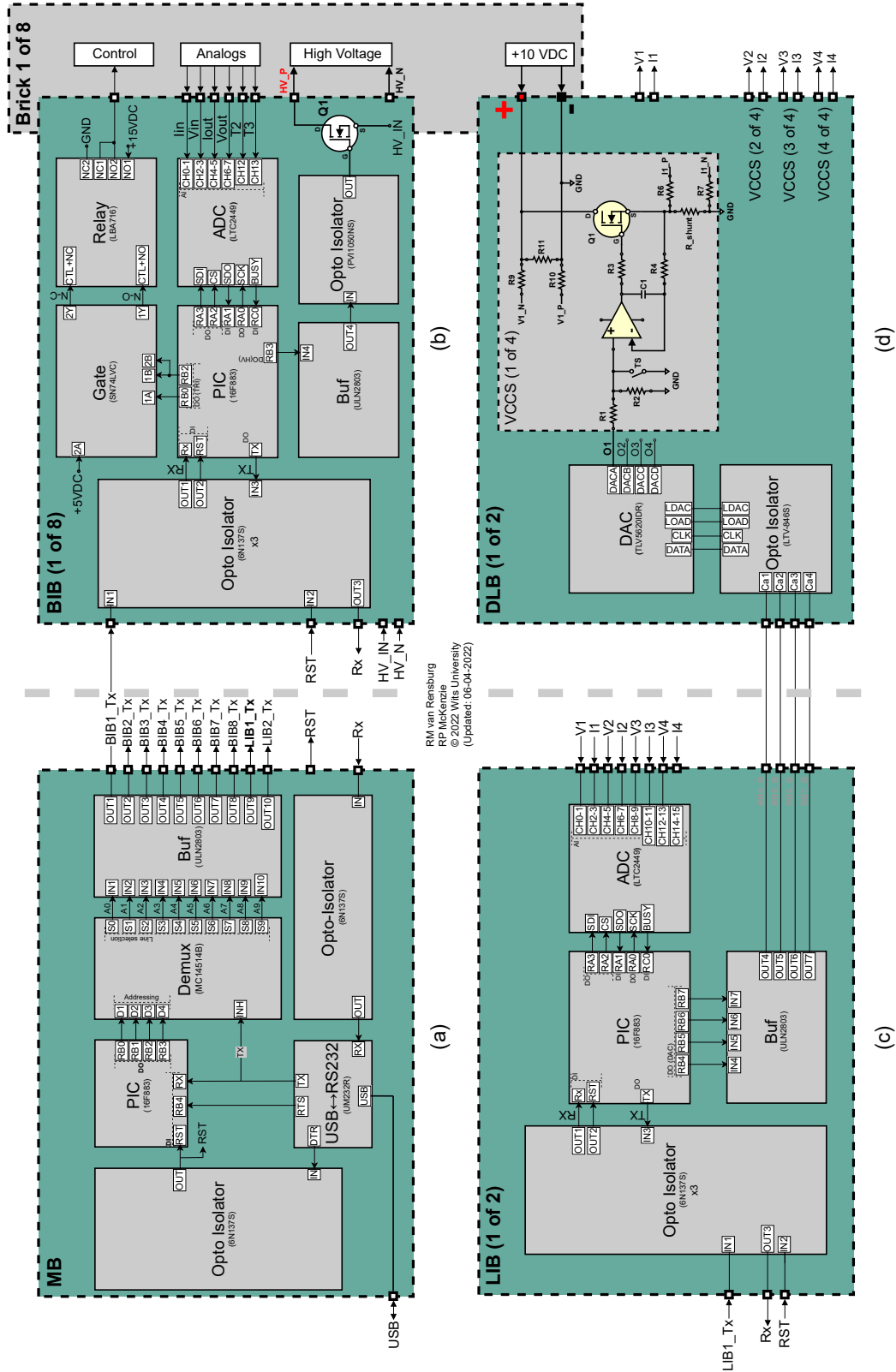


Figure F.4: Burn-in station water manifold. There are two manifolds per Burn-in station. The first is an inlet manifold and the second is an outlet manifold.



F.2 Burn-in LabVIEW Application

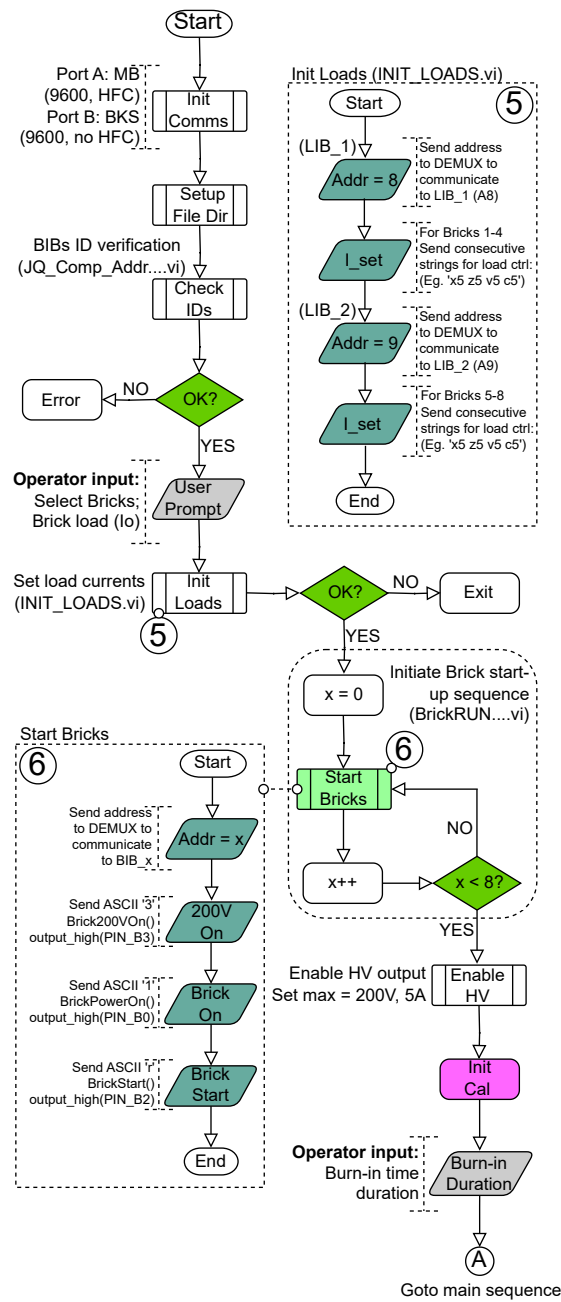


Figure F.6: Simplified Burn-in LabVIEW Application initialisation sequence.

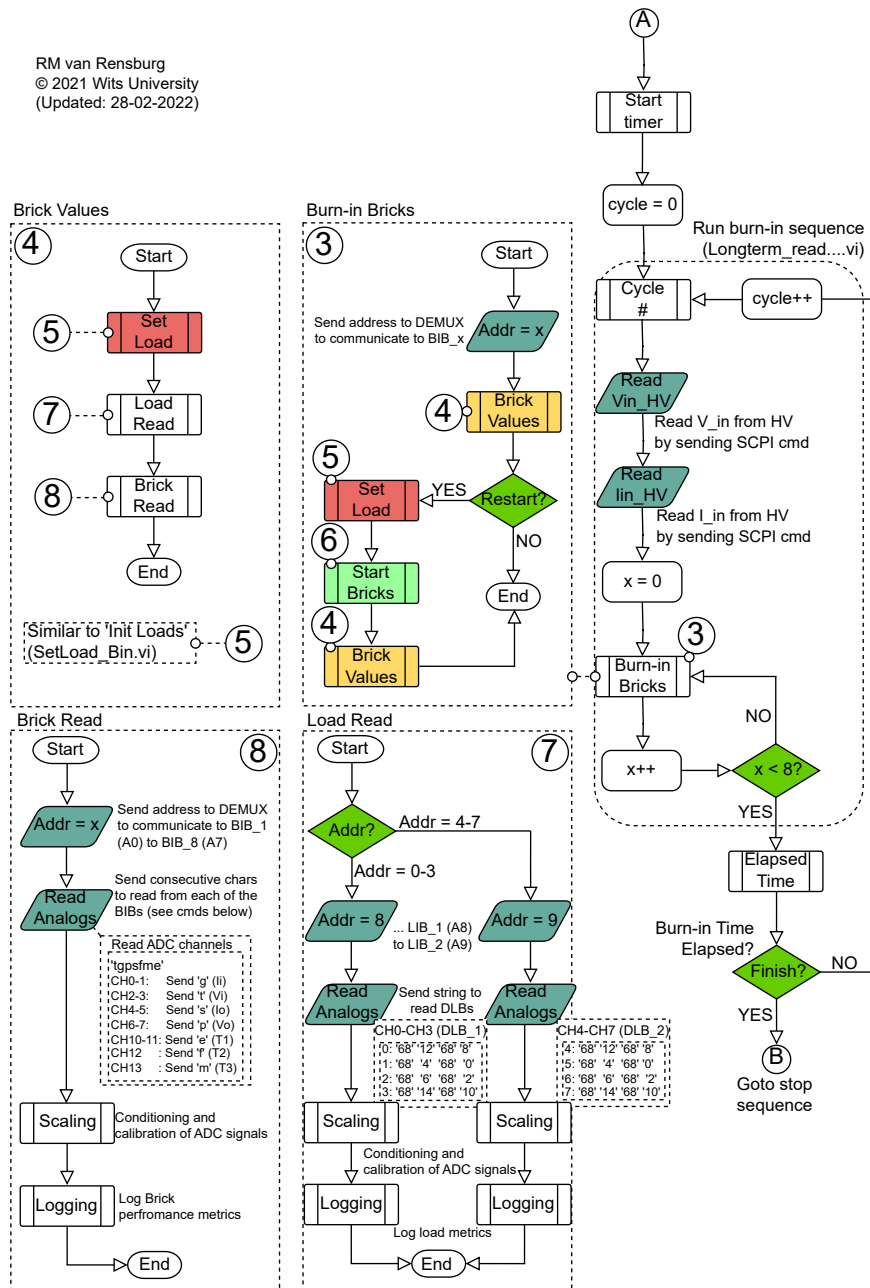


Figure F.7: Simplified Burn-in LabVIEW Application main Burn-in sequence.

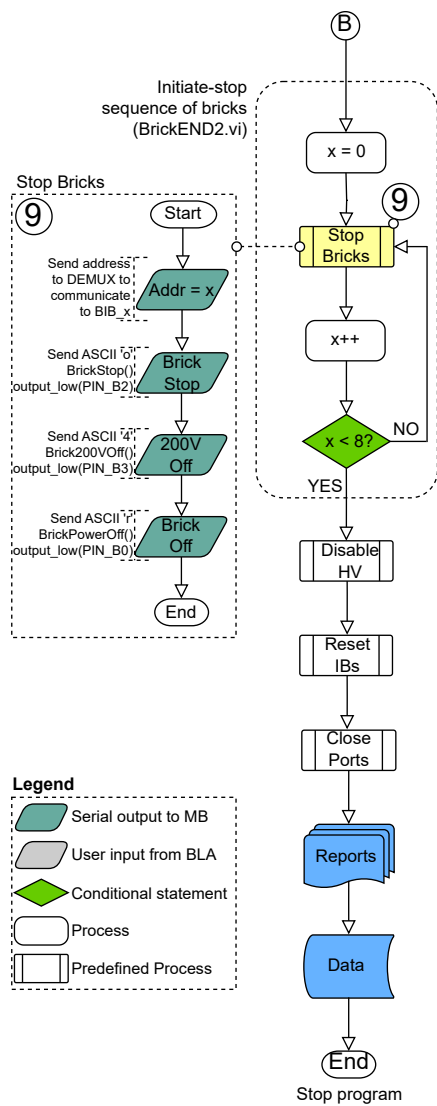
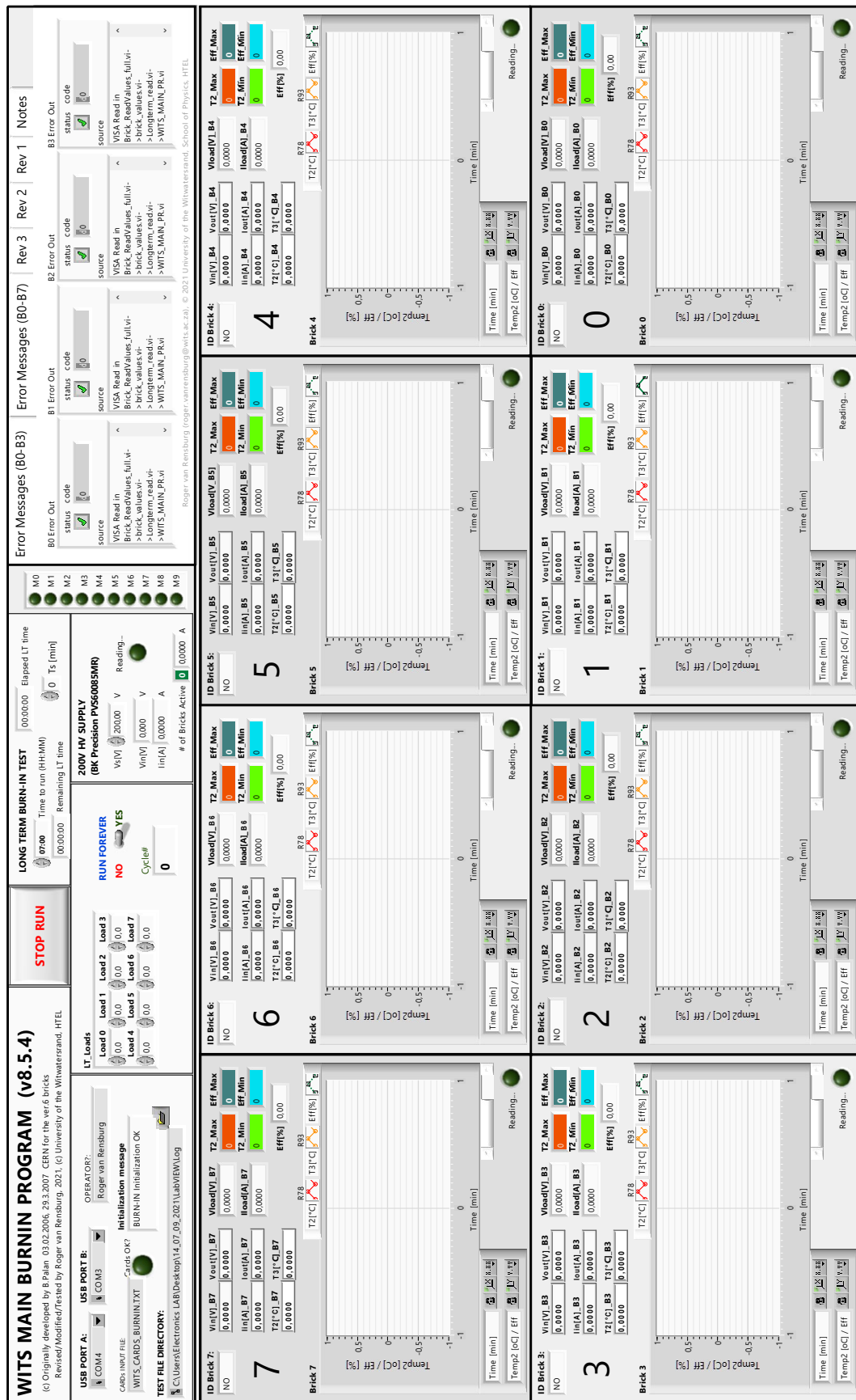


Figure F.8: Simplified Burn-in LabVIEW Application stop sequence.



Appendix G

fLVPS Brick Project Schedule

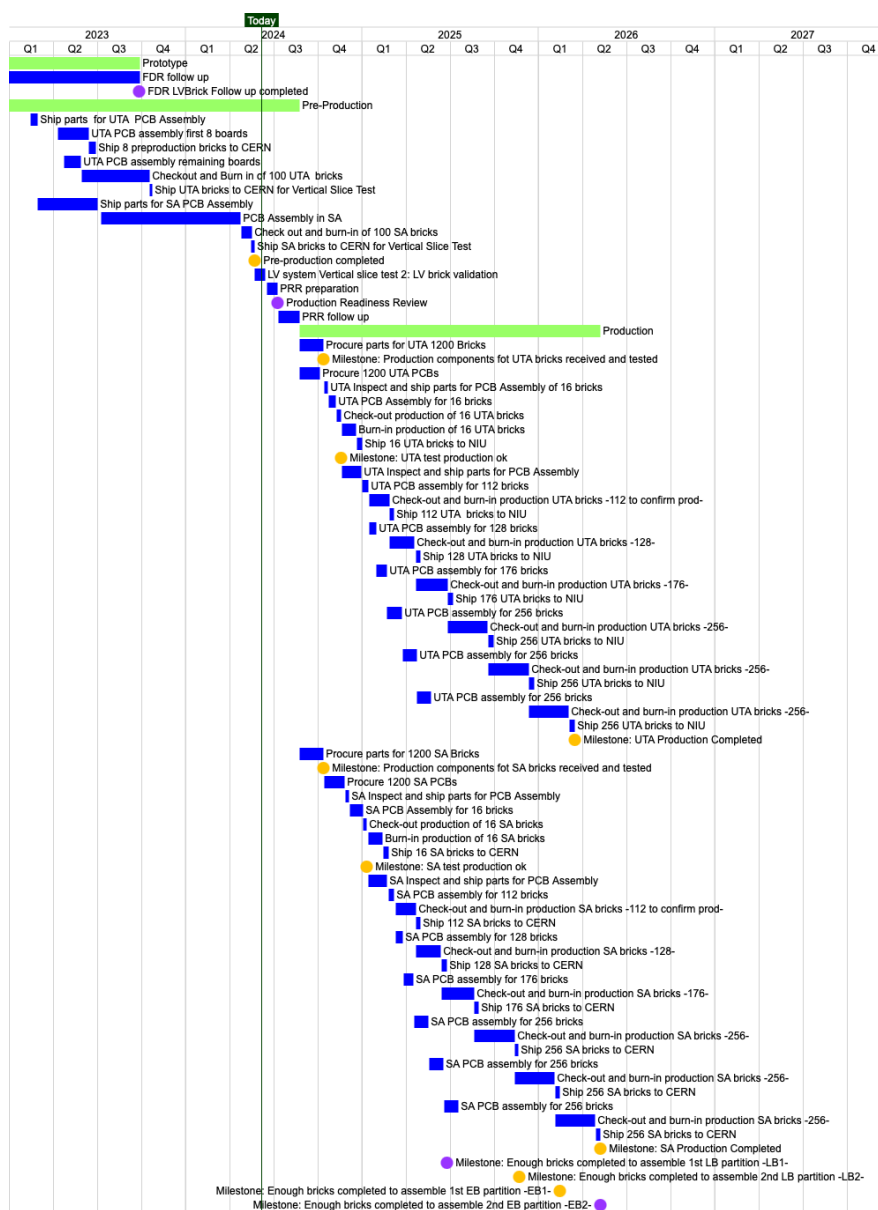


Figure G.1: Gantt chart of the TileCal Phase-II Upgrade Brick project as of 6 June 2024.