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DISSERTATION

INTEGRATED CIRCUITS FOR THE SYNCHRONISATION OF HIGH-ENERGY PHYSICS EXPERIMENTS

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Kurzfassung

Diese Arbeit beschreibt die Entwicklung von anwendungsspezifischen integrierten Schaltungen (ASICs) für die Synchronisation von Hochenergiephysikexperimenten.

Das Problem der Synchronisation findet man in vielen komplexen Systemen. Die speziellen Anforderungen an die in zukünftigen Teilchendetektorsystemen zur Synchronisation verwendeten integrierten Schaltungen sind neben geringem Stromverbrauch und Unempfindlichkeit gegenüber Versorgungsspannungsschwankungen vor allem in der Robustheit gegenüber hohen Strahlungsdosen gegeben.

Integrierte Schaltungen zur Synchronisation erfüllen zwei wichtige Aufgaben:

(a) Erzeugung von präzisen **Signalverzögerungen**

(b) **Distribution** von Synchronisationssignalen

Die vorliegende Arbeit behandelt daher zuerst die Frage, wie integrierte Schaltungen zur präzisen Verzögerung von digitalen Signalen gebaut werden können. Wir geben zunächst einen Überblick über die dabei zur Verfügung stehenden Methoden, und beschreiben dann die Implementierung einer strahlungsharten Schaltung, die eine Delay-Locked Loop (DLL) zur automatischen Kalibrierung verwendet. Wir analysieren dabei, wie die erzielbare Präzision mit den Matching-Eigenschaften der Transistoren zusammenhängt.

Der zweite Teil widmet sich dem Problem der Taktdistribution: Ein kombiniertes Takt- und Datensignal wird zur detektorweiten Synchronisation über eine Glasfaserleitung übertragen. Wir beschreiben die Entwicklung einer strahlungsharten integrierten Schaltung zur Takt- und Datenregeneration aus dem Biphase Mark codierten optischen Signal, basierend auf einer Phase-Locked Loop (PLL). Dabei behandeln wir ausführlich die Designaspekte der PLL Komponenten: Zunächst analysieren wir, welche Zusammenhänge in einer PLL gegeben sein müssen, um das Schleifenverhalten unabhängig von Bauteilparametern zu machen. In der Folge behandeln wir die Frage, wie der interne Oszillator ohne externes Referenzsignal auf die Zielfrequenz gebracht werden kann, wobei wir eine neuartige Frequenzdetektorschaltung beschreiben. Drittens stellen wir einen neuen Phasendetektor vor, der es erlaubt, direkt auf ein Biphase Mark codiertes Signal einzurasten. Viertens beschreiben wir eine Vorgangsweise, um den durch intrinsisches Rauschen verursachten Jitter in Oszillatoren zu berechnen.

Der dritte Teil dieser Arbeit beschreibt den "Timing, Trigger and Control Receiver" ASIC. Dieser komplexe analog-digitale Chip, der in allen für den Large Hadron Collider (LHC) geplanten Experimenten verwendet werden wird, stellt sämtliche zur Detektorsynchronisation benötigten Signale bereit.

Der Schwerpunkt der Dissertation ist die Entwicklung integrierter Schaltungen mit CMOS Transistoren. Ihre Beiträge sind erstens die analytischen Resultate, die das Design von Phase-Locked Loops und die Matching-Eigenschaften von Verzögerungsleitungen betreffen. Zweitens die vorgestellten neuen Schaltungen (Frequenzdetektor und Phasendetektor), und drittens, die Implementierung der Schaltungen selbst, welche breite Verwendung in allen derzeit am CERN entwickelten Experimenten finden werden.

Abstract

This work describes the design of Application Specific Integrated Circuits (ASICs) for the synchronisation of High-Energy Physics Experiments.

The problem of synchronisation arises in many complex systems, being as small as a microprocessor, or as big as one of the high energy physics experiments being currently developed at CERN for the Large Hadron Collider (LHC). The particularity of the latter environment is primarily given by the high amount of radiation inside the detector. The circuits have to withstand a total radiation dose of up to 10 Mrad, which is by far more than what is found in space applications. Additional requirements are low power and robustness against changes in supply voltage.

There are two central tasks of synchronisation circuits, which are

- (a) the **generation of accurate delays**, and
- (b) the **distribution** of timing signals.

The first question, that this thesis gives an answer to, is thus how to design circuits for generating accurate programmable delays. We will summarise the available methods, and present a radiation-hard circuit, which uses a Delay-Locked loop (DLL) for the automatic calibration of active delay lines. We will analyse how the matching properties of the devices in the delay line affect the expected timing accuracy.

The second part deals with the problem of clock recovery. The current plan for the synchronisation system, which is going to distribute the timing information in all future LHC experiments, foresees a combined clock and data signal to be transmitted over an optical fibre with a biphase mark encoding. We present a radiation-hard circuit based on a Phase-Locked Loop (PLL), which recovers a low-jitter clock and data from the optical signal. We broadly discuss the design of the various components of PLLs: First we investigate how a PLL must be designed to make it independent to changes in device parameters. Secondly, we describe how the internal oscillator can be set to the right frequency without an external frequency reference. At this occasion, we introduce a novel frequency detector circuit for Biphase and Nonreturn-to-zero data. Thirdly, we present a novel phase detector, which allows the PLL to lock directly on a Biphase Mark input signal. Finally, we present a method to predict cycle-to-cycle jitter in ring oscillators caused by intrinsic device noise.

The third part of this work describes the "Timing, Trigger and Control Receiver" ASIC. This complex analog-digital chip, which will be used in all future LHC experiments, generates all the required signals for detector synchronisation.

The focus of this thesis is primarily on integrated circuit design with MOS transistors. Its contributions are threefold: First we present analytical results concerning the design of matched delay lines and Phase Locked Loops (PLLs). Secondly, we introduce new circuits, i.e. a novel frequency and a novel phase detector and - last but not least - we present the actual implementation of the circuits, which will find broad use in all future LHC experiments at CERN.

List of Abbreviations and Acronyms

ALICE	A Large Ion Collider Experiment
ASIC	Application Specific Integrated Circuit
ATLAS	A Toroidal LHC ApparatuS (LHC Experiment)
BiCMOS	Combined Bipolar and CMOS
CERN	European Laboratory for Particle Physics
CMOS	Complimentary MOS
CMS	Compact Muon Solenoid LHC experiment
CP	Charge Pump
DLL	Delay-Locked Loop
DMILL	Durci Mixte Logico-Lineaire
FD	Frequency Detector
FET	Field Effect Transistor
LHC	Large Hadron Collider
LHC-b	An LHC Experiment for the Study of CP violation in B-meson decays
LPE	Last Positive Edge detection
MOS	Metal On Silicon
NMOS	N-type MOS
NRZ	Nonreturn-to Zero
PD	Phase Detector
PFD	Phase-Frequency Detector
PLL	Phase-Locked Loop
PMOS	P-type MOS
SEL	Single Event Latchup
SEU	Single Event Upset
SIMOX	Silicon Isolated By Implanted Oxide
SOI	Silicon on Insulator
TTC	Timing, Trigger and Control
TTCrx	Timing, Trigger and Control Receiver
VCO	Voltage-Controlled Oscillator
XOR	eXclusive Or

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Chapter 1

Introduction

1.1 Synchronisation of Particle Detectors

The synchronisation of large particle detectors such as ATLAS or CMS, currently being developed for the Large Hadron Collider (LHC) at CERN, is a formidable task. The total number of signal channels is in the order of 100 million, each delivering data every 25ns. A comparison of the physical dimensions of the detector (about 40m in length and 20m in diameter for ATLAS) with the speed of light gives a first impression of the differences in signal propagation time to expect. But why is synchronisation important, and at what points the signals have to be synchronised ?

To answer these questions, it is first necessary to understand the principles of data acquisition in a particle detector. Every 25ns, two bunches of particles collide inside the detector, producing a large number of collision products. Most collisions, however, do not contain any interesting events, so the data is simply discarded. If the event is interesting, however, then the data of *all* signal channels has to be saved for this specific time-slot. A time-slot is identified by its unique *bunch-crossing number*. The question, which kind of event is worth to be memorised, is determined by the physics experiment to which the collider shall give an answer to, e.g. the quest for a new particle of certain mass etc. There is one instance judging every 25ns if the raw data of a certain time slot has a chance to contain an interesting event: This instance is commonly referred to as the *Level 1 trigger generator*.

The level 1 trigger generator receives its input from only a subset of the raw data, and has to be fast in order to cope with the data rate of 40MHz. By introducing the trigger concept, it is possible to reduce the gigantic quantity of raw data by at least two orders of magnitude. Subsequent trigger levels (level 2 and 3) further decimate the amount of data. An event which passes the final trigger is ultimately considered to be interesting, and, consequently, is stored on tape for later analysis. Since the higher order triggers have more time to process the data, they can implement algorithms of higher complexity. There is one problem with the level 1 trigger, however, which is, that its actual hardware is located outside the detector. The subset of the raw data needed by the trigger therefore must be transported to this location, and the trigger decision must be brought back to the detector.

This, of course, takes time¹. The time between sending new data to the trigger generator and the arrival of the trigger decision is referred to as the *Trigger latency*. The detector electronics somehow has to memorise the data during the trigger latency time by means of analog or digital pipelines. When the trigger accept signal finally arrives in the case of an interesting event, the data at the end of the pipeline is then sent outside the detector to be further processed by higher order triggers. A simplified image of the situation is shown in Fig. 1.1. As seen in the figure, there are four points which require timing alignment:

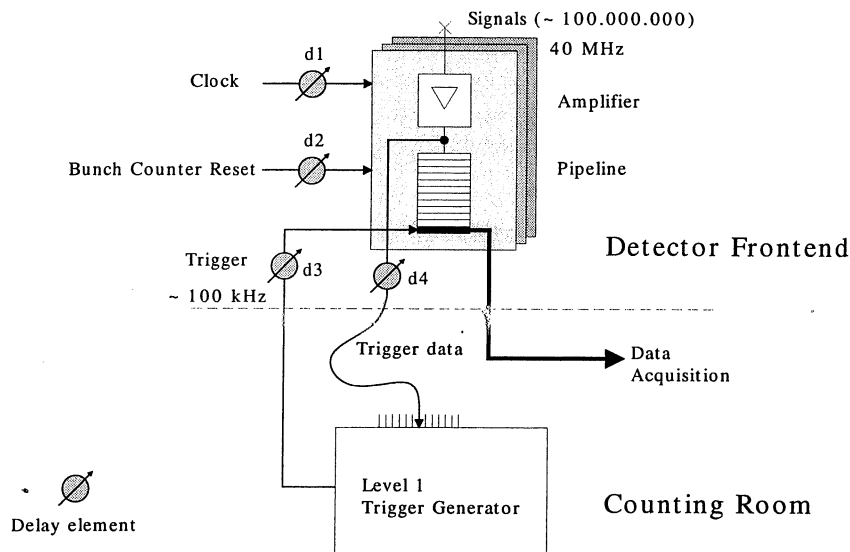


Figure 1.1: Simplified structure of the trigger and data acquisition process.

First, the clock of the frontend electronics. The clock determines when a data sample is taken from the detector hardware, e.g. a wire chamber. In order to choose the optimum sampling instant, the clock phase has to be correctly adjusted. The thereby required timing precision depends on the signal shape of the specific detector, some detectors needing sub-nanosecond precision.

Secondly, as seen in the figure, the data at the input of the Level 1 trigger generator originates from a multitude of different subdetectors. Consequently, before entering the trigger generator, this data must be aligned with a resolution of at least 25ns in order that all data originate from the same bunch-crossing.

Thirdly, the trigger signal going back to the frontend electronics must arrive at a time such that the last element in the pipeline carries the data from the event which caused the trigger decision. It therefore must be possible to delay the trigger signal before entering the frontend with a resolution of at least 25ns.

Fourthly, it must be possible to uniquely identify a bunch-crossing: In the frontend electronics, the sampled data is labelled with the bunch-crossing number. The synchronisation

¹Apart from the propagation delays in the electrical wires and optical fibres, also the electronics delay and the particle time-of-flight has to be considered.

signal, which periodically² resets the bunch crossing counter, therefore has to arrive at the same time in all detector elements.

1.1.1 Strategies for Setting up the Timing of the Experiment

Several hundred thousand readout elements thus receive synchronisation signals. The phases of all these signals have to be adjusted, initially during the commissioning phase of the experiment, but also during normal operation. Two methods are currently being considered to find the correct values for timing adjustment [PHFA-98, TRIG-98, WROC-98]:

- (a) Test pulses
- (b) LHC beam

Test pulses can be exploited for providing synchronisation between the trigger and the data acquisition system. A test pulse can be either produced by irradiating the detector with a laser beam [BENE-98], or can be injected electronically (before or after the amplifier in Fig. 1.1). The delay value of the trigger signal (d3 in Fig. 1.1) can then be adjusted until the read out data corresponds to the test pulse signal.

The LHC beam is then used for global synchronisation: Since not all 3564 time-slots of one LHC beam revolution contain particles, the beam displays the structure shown in Fig. 1.2. If a time-slot is empty, no signal can be detected. If, however, the data read out from the detector exceeds a threshold value, a hit is inserted in a histogram over the bunch crossing number. After a sufficiently long time, the histogram is then matched against the bunch structure of Fig. 1.2, which allows to determine the position of the zero bunch crossing and to adjust the delays accordingly.

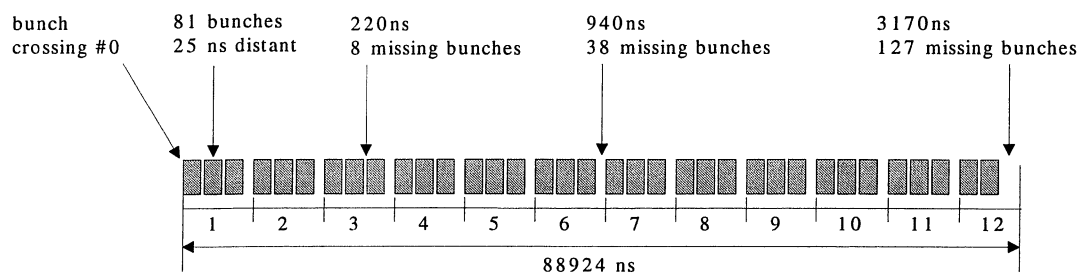


Figure 1.2: The bunch structure of the LHC beam.

²A single revolution of a bunch of particles takes $88.924\mu\text{s}$ or 3564 bunch-crossing intervals. The LHC machine provides the so-called "Orbit" signal which signals the start of a new revolution with a frequency of 11.246 kHz.

1.2 Integrated Circuits for Synchronisation

There are two central tasks of integrated circuits for synchronisation, which are

- (a) Generation of accurate programmable delays
- (b) Distribution of timing signals

The signals which thereby have to be precisely timed and distributed comprise the clock, the level 1 trigger decision, and a signal to indicate the bunch number zero. This thesis is concerned with the design aspects of integrated circuits, which provide the tasks (a) of generating accurately controlled delays, and (b) of recovering a low-jitter clock signal from an encoded data stream. Due to the high amount of radiation inside the detector, the integrated circuits have to withstand a high dose of radiation. Additional requirements on the circuits are low power and high power supply rejection.

Contributions of this Work

In this thesis we will present three integrated circuits, which provide crucial components of the synchronisation system, i.e.

- (1) A radiation-hard self-calibrating delay generation ASIC³ with a resolution of 1ns. This chip, apart from the aspect of radiation-hardness, is the first of its kind to use a delay-locked loop to calibrate the signal delays in slave delay lines.
- (2) A radiation-hard 80 MHz clock-and data recovery circuit, used for receiving the clock and data from an optical link.
- (3) A system-on-chip for the distribution of the clock and the other synchronisation signals. It incorporates the clock-and data recovery circuitry of (2), together with additional high resolution clock de-skewing capabilities. Most of the circuit area, however, is occupied by digital logic, implementing two different transmission protocols, a command interpreter, counters, and delay pipelines. This chip, referred to as the "Timing, Trigger and Control Receiver ASIC" or "TTCrx", is a central component of all particle detector synchronisation systems, and will be utilised in all LHC experiments (ATLAS, CMS, ALICE, LHCb) at CERN [RD12-96].

The circuits were designed to be robust against changes in device parameters in order to increase their immunity against radiation. We will present results of circuits (1) and (2) before and after a gamma-irradiation to a level of 10 Mrad. We will introduce practices for robust design for radiation hardness, and will report on the effects of radiation-induced device mismatch.

We will present results concerning the design of circuits for delay generation and clock recovery, which, beside their application in the high-energy physics environment, are of common interest to circuit design:

³Application Specific Integrated Circuit

- (a) *Matching of delaylines*: We will analyse the factors which determine the matching properties in active delay lines, and show that the matching requirements in a closed loop are four times less stringent than in the open-loop case.
- (b) *Symmetric loads*: We present an analytic solution of the frequency vs voltage function in Voltage-Controlled Oscillators (VCOs) with symmetric loads, and show that the function given in [MANE-96] only holds for a limited frequency range.
- (c) *Parameter-independent biasing*: We analyse the conditions for achieving parameter-independent loop-dynamics in Phase-Locked Loops (PLLs). We present one VCO structure, which is parameter-independent for the whole VCO frequency range, and one VCO using symmetric loads, which is largely independent of transistor-device parameters for a single frequency.
- (d) *Frequency detector for Biphase and NRZ signals*: As an alternative to the Rotational Frequency Detector [MESS-79], commonly used in clock recovery applications, we present a novel FD, which (1) overcomes the limitation of a 50% lower frequency offset bound, and (2) does not require a quadrature VCO input.
- (e) *Phase detector*: We describe a novel phase detector, which uses a state-machine to guarantee direct lock to a Biphase Mark input sequence.
- (f) *Stability limit in PLLs with bang-bang phase detectors*: We will show how a stability criterion relates jitter and static power-supply rejection.
- (g) *Oscillator noise analysis*: We adapted the cyclo-stationary model from [HAJI-98a] to calculate cycle-to-cycle jitter in the time domain. The expected jitter is in good accordance with the measurements.

The contributions made during the course of this research have led to the following publications:

1. **T. Toifl, R. Vari, P. Moreira, A. Marchioro**, *A 4 channel rad-hard delay generation chip with 1ns timing resolution for LHC*, accepted for publication in IEEE Transactions on Nuclear Science, 1999
2. **T. Toifl, P. Moreira, A. Marchioro, P. Placidi**, *Analysis of Parameter-Independent PLLs with Bang-Bang Phase Detectors*, Proc. IEEE Internat. Conf. on Electronics, Circuits and Systems (ICECS'98), Lisboa, Portugal, Sept. 1998
3. **T. Toifl, P. Moreira**, *A Simple Frequency Detector for Biphase and NRZ Clock Recovery*, Electronics Letters, Vol. 34, Nr. 20, 1.Oct. 1998
4. **T. Toifl, P. Moreira**, *A Radiation-Hard 80 MHz Phase-Locked Loop for Clock and Data Recovery*, to be presented at IEEE Internat. Symposium on Circuits and Systems ISCAS'99, Orlando, Florida, USA, June 1999
5. **A. Marchioro, P. Moreira, T. Toifl, T. Vaaranemi**, *An Integrated Laser Driver Array for Analogue Data Transmission in the LHC Experiments*, Proceedings of the 3rd Workshop on Electronics for LHC Experiments, London, UK, Sept. 1997

6. **T. Toifl, P. Moreira, A. Marchioro**, *A Radiation-Hard Clock and Data Recovery Circuit for LHC*, Proceedings of the 4th Workshop on Electronics for LHC Experiments, Rome, Italy, Sept. 1998

7. **C. Posch, T. Toifl**, *A Mixed Signal Data Receiver/Clock Synchronizer ASIC for Analog Frontend Chips in LHC Experiments*, Proceedings of the 4th Workshop on Electronics for LHC Experiments, Rome, Sept. 1998

1.3 Structure of This Work

Following this introduction, Chapter 2 contains a short overview on radiation effects in semiconductor devices, and describes available radiation-hard technologies.

The following part (Chapter 3-4) is concerned with the question of how to design integrated circuits for the generation of programmable delays. While Chapter 3 gives an overview of the available methods, Chapter 4 describes the actual implementation of a radiation-hard self-calibrating delay generation ASIC.

The problem of how to distribute synchronisation data in the detector system is discussed in Chapters 5-8. After the description of the generic system for clock and data distribution in Chapter 5, we will then focus on the different design aspects of Phase-Locked Loops (PLLs) for clock recovery: Chapter 6 presents a design procedure for parameter-independent PLLs, and Chapter 7 contains the description of a novel frequency detector circuit for Biphase and Nonreturn-To-Zero data. The overall implementation of a radiation-hard clock and data recovery circuit is then presented in Chapter 8. In the course of the chapter, the novel phase detector for Biphase Mark code will also be described.

Chapter 9 describes the "Timing, Trigger and Control Receiver ASIC", a system-on-chip providing the entire functionality for generating the clock and the other synchronisation signals for the experiments.

Apart from the main part of this text, we also want to emphasise the importance of the appendices, which actually contain most of the analysis, but, for reasons of compactness, were not included in the body of the thesis. Appendix A derives an expression for the expected maximum non-linearity in delay lines, and Appendix B gives an expression for the delay matching in a current-starved inverter cell. In Appendix C we present an analytical solution for differential oscillators using symmetric loads. A procedure for analysing VCO noise is presented in Appendix D, followed by the derivation of a stability limit in bang-bang phase-locked loops in Appendix E.

Chapter 2

Overview of Radiation Effects in Integrated Circuits

The effects of radiation in integrated circuits are classified into two groups

- (a) **Total dose effects**, which describe the accumulated degradation of device parameters due to a slow modification of the device structure.
- (b) **Single event effects**, in which the operation of the circuit is disturbed due to an instantaneous interaction with an energetic particle.

2.1 Total Dose Effects

The following total dose effects have to be considered

- (a) Charge trapping in the oxide
- (b) Interface state creation
- (c) Bulk displacement

While items (a) and (b) mainly influence the behaviour of MOS transistors, bulk displacement effects mostly concern bipolar devices.

2.1.1 Charge Trapping in the Oxide

The most important effect of radiation in MOS transistors is the accumulation of positive charge in the $Si-SiO_2$ layer. The mechanism is the following [ALEX-96]: When ionising radiation passes through silicon dioxide, free electrons and holes are generated. Electrons have a much higher mobility than holes and are swept out of the oxide. The less mobile holes tend to be trapped near the silicon interface. The positive charge then induces a negative charge in the Si at the Si/SiO_2 interface, which changes the effective threshold voltage of the MOS transistor. The threshold voltage of NMOS transistors is thereby moving towards

lower values, i.e. the transistor can be switched on with smaller values of V_{gs} , while the absolute value of the threshold voltage for PMOS transistors is rising, hence requiring higher (absolute) values of V_{gs} to switch the transistor on. Consequently, as the threshold voltage of NMOS transistors gets lower, the sub-threshold leakage current is rising exponentially. This increase in leakage current, which is found in ordinary and parasitic NMOS transistor structures, is the most important problem concerning the radiation hardness of MOS devices.

The number of trapped holes depends on the direction and the magnitude of the electric field in the oxide during the irradiation. If the electric field across the oxide is zero, then most holes can recombine and escape from being trapped. The worst case is a positive bias applied to the gate electrode, because then the resulting electric field drives the holes to the Si/SiO_2 interface.

Two physical processes can remove the trapped holes from the oxide: Thermal annealing and tunnelling. The time constant for *thermal annealing* gets lower for higher ambient temperatures. A complete thermal annealing thereby often requires temperatures of up to $450^\circ C$ [MA-88].

The *tunnel annealing* process is only effective for holes trapped within a distance of $5nm$ from the substrate or the gate electrode, because the tunnelling probability is rapidly decreasing with distance. Consequently, only deep submicron processes with a gate thickness $< 10nm$ can profit from this effect. In fact, due to the tunnel annealing process, the measured V_t -shifts in deep submicron devices caused by radiation are very small [SAKS-84].

2.1.2 Leakage Current Due to Parasitic NMOS Transistors

MOS transistors are typically designed for a self-aligned process in which the polysilicon gate material is deposited over a thin oxide region. The source/drain implant is then performed and fills the region not covered by field oxide and poly. Unfortunately, the material at the transition between the field oxide and the thin oxide produces a parasitic transistor, depicted in Fig. 2.1, which is very susceptible to total ionising dose effects. The silicon dioxide in this region, known as the bird's beak, is under mechanical stress produced by the dynamics of the oxide growth process and the transition from thin to thick oxide. The transition region is of variable thickness and experiences a relatively high electric field from the combination of poly gate bias and the fringing fields from the source to drain bias. As a consequence, the parasitic transistors at the bird's beak accumulate a high amount of positive charge, which lowers the transistor's threshold voltage and ultimately causes a high leakage current. The parasitic transistor at the bird's beak can be avoided, however, by using reentrant transistors [MADR-89], shown in Fig. 2.2.

A second parasitic NMOS structure is found between the $n+$ (drain- or source) diffusions of two neighbouring transistors. In order to prevent leakage current to flow along this path, a $p+$ -guard ring must be set around the NMOS transistor [SNOE-98].

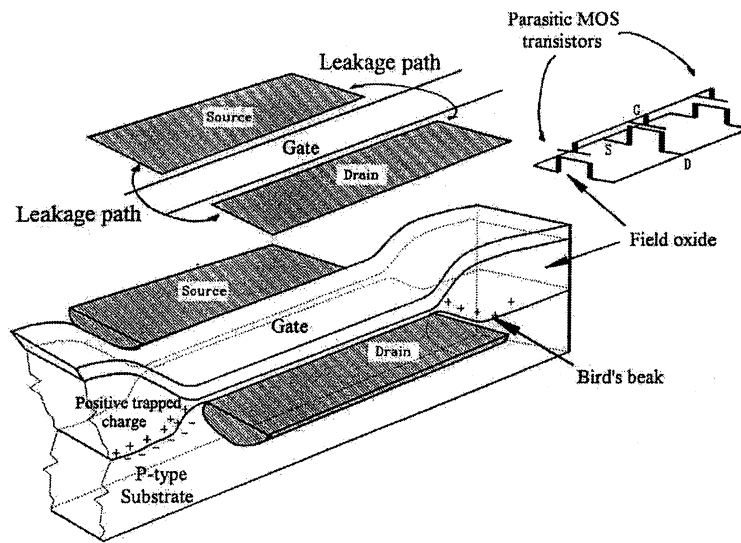


Figure 2.1: Parasitic MOS transistor at the interface between gate oxide and field oxide.

2.1.3 Interface State Creation

Interface states (also referred to as interface traps or surface states) are electronic energy levels located at the Si/SiO_2 interface that can capture or emit electrons or holes. These electronic levels arise because of the lattice mismatch at the interface, disconnected chemical bonds or impurities. Energetically they are located at energy levels between the valence band and the conduction band. The following effects can be observed:

- (a) Shift of the threshold voltage V_t : This shift is positive in NMOS transistors, and hence counteracts the V_t -shift caused by positive charges trapped in the oxide. In PMOS transistors, the resulting V_t -shift is negative, which further decreases the value (=increases the absolute value) of V_t .

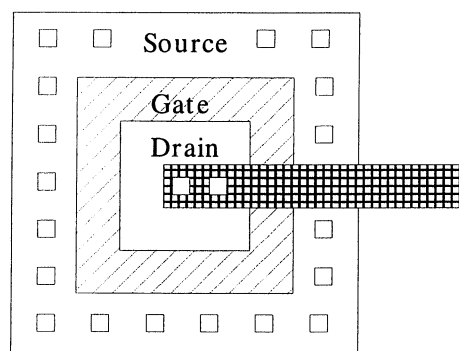


Figure 2.2: Structure of MOS transistor with enclosed gate for avoiding the bird's beak at the interface between gate oxide and field oxide.

- (b) Degradation of the carrier mobility μ .
- (c) Flattening of the sub-threshold slope of the MOS transistor.
- (d) Increase of $1/f$ -noise coefficient and corner frequency.

2.1.4 Bulk displacement

Bulk displacement effects result from the displacement of atoms from their normal sites in the crystal lattice due to an interaction with energetic particles. It causes a diminution of carrier mobility and density in bipolar transistors, being effective mainly in the lightly doped base region. It does not play a role in MOS transistors, however, due to the high doping concentration in the drain and source regions [MADR-89].

2.2 Single Event Effects

Single event effects are caused by ionisation along the path of a single energetic particle passing through an integrated circuit. If the deposited charge is big enough to switch on a parasitic thyristor structure, as shown in Figure 2.3, then a Single Event Latchup (SEL) occurs, often leading to the destruction of the integrated circuit.

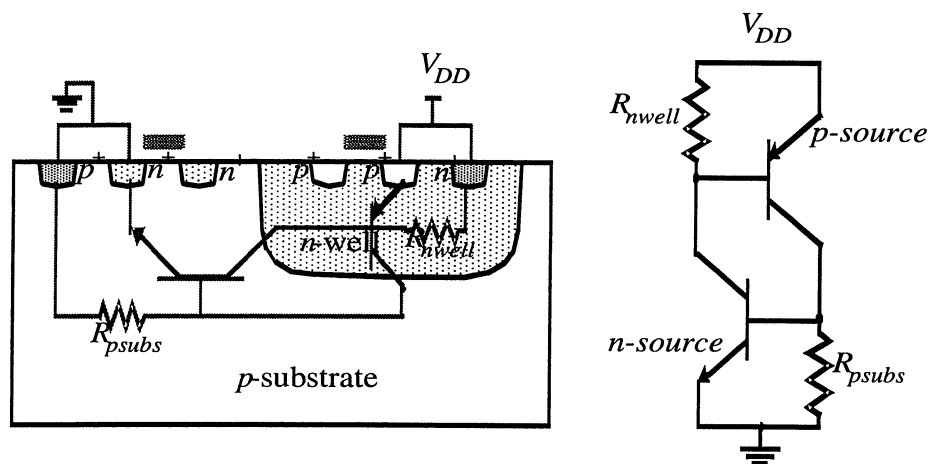


Figure 2.3: Single Event Latchup (SEL) due to charge deposited on parasitic thyristor structure (adapted from [RABA-96]).

A second effect is single event upset (SEU), creating problems in digital circuits. Here the deposited charge changes the logical state of a node, thereby introducing an erroneous bit in the logic.

2.3 Available Solutions for Radiation-Hard Electronics

In order to build radiation-hard integrated circuits, two solutions exist at present: First, dedicated radiation hard technologies, which were developed in the past for space and military applications. These technologies are either based on Gallium-Arsenide or use a Silicon On Insulator (SOI) technology. Secondly, the now emerging deep submicron technologies [MARC-98], which are intrinsically radiation-hard due to their small oxide thickness.

2.3.1 Dedicated Rad-Hard SOI Process

Figure 2.4 shows a cross-section of the DMILL¹ technology, which was used to fabricate the circuits described in the subsequent chapters. DMILL is a Silicon on Insulator (SOI) process, where the oxide layer is created with a SIMOX (Silicon Isolated By Implanted Oxygen)-process [ALLE-97]. The technology offers NMOS and PMOS transistors, a vertical NPN bipolar transistor and a junction FET device. As seen in the figure, the devices are completely isolated, vertically by the buried layer of SiO_2 , horizontally by trenches. Since there is no $n-p-n-p$ structure, the possibility of a single event latchup is excluded. The Single Event Upset (SEU) rate is also reduced, since the path where a particle can deposit charge is limited by the oxide layer. Special steps in processing results in a carefully grown oxide, which limits the radiation-induced V_t shift to 200mV for PMOS and 150mV for NMOS transistors after a total dose of 10 Mrad [DENT-98]. Unlike the case of a standard process, the thin oxide is extended around the whole NMOS transistor, thereby avoiding the parasitic transistors under the thick oxide and keeping the leakage current low.

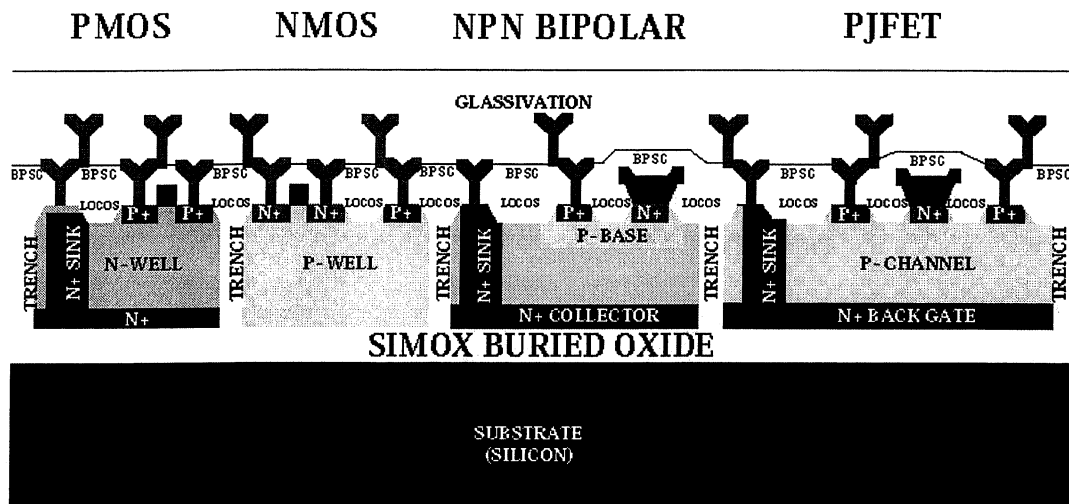


Figure 2.4: Cross-section of device structures available in the DMILL SOI technology.

¹DMILL="Durci Mixte Logico-Lineaire"

2.3.2 Commercial Deep Submicron Technologies

The present trend for radiation-hard electronics is the use of commercial deep submicron ($< 0.35\mu\text{m}$) technologies, which are intrinsically insensitive to irradiation. Figure 2.5 shows the dependence of the radiation-induced V_t shift as a function of the oxide thickness. It can be seen that for $t_{ox} \gtrsim 50\text{nm}$ the expected shift in threshold voltage scales with the square of the oxide thickness. If the oxide thickness gets $\lesssim 10\text{nm}$, the expected threshold shift goes down even stronger, due to the above-mentioned tunnel annealing effect. Values of $+5$ and -30mV , respectively, for NMOS and PMOS transistors were measured for a quarter micron technology ($t_{ox} = 7\text{nm}$) and a total dose of 10 Mrad [GIRA-99].

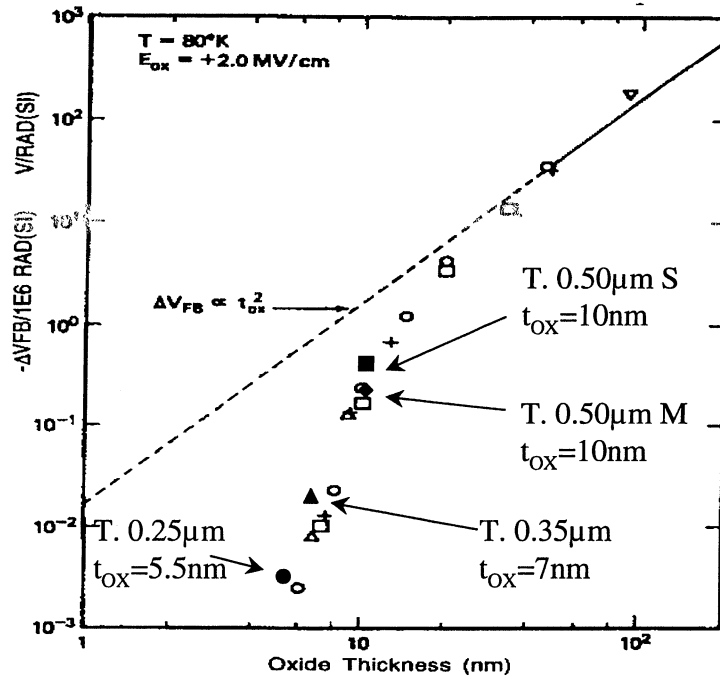


Figure 2.5: V_t -shift caused by charges trapped in the oxide as a function of t_{ox} (Source: adapted in [GIRA-99] from [SAKS-84]).

Commercial technologies are sensitive to leakage current effects caused by parasitic transistors under the thick field oxide. This leakage current can be avoided, however, by using (a) reentrant NMOS transistors, and (b) by placing guard rings around the NMOS transistors to eliminate the leakage current path between the source/drain diffusions of neighbouring devices.

The possibility of a Single Event Latchup (SEL) cannot be excluded in a standard technology. Guard rings have to be set around the devices to keep the base potential of the parasitic bipolar transistors at GND or V_{DD} . The Single Event Upset (SEU) rate is expected to be higher when going to smaller feature sizes since the capacitances become lower. Hence, a smaller deposited charge is sufficient to switch a logical node. This problem can be overcome by using special radiation-hardened flip-flop structures [ANDR-82, FACC-98].

Chapter 3

Generation of Precise Delays

As discussed in Chapter 1, one of the key issues in designing circuits for synchronisation is the question of how to accurately delay digital signals by a programmable value. This chapter gives an overview of the various techniques that can be applied for this task. The optimum method to choose then depends on the type of the signal, constraints on timing resolution, overall delay range, power consumption, and the process data of the available technology. As the parameters of basic devices change with process variations, temperature, and radiation dose, it is however impossible to achieve satisfactory absolute timing accuracy without an external reference. We will first define measures for the characterisation of delay generation circuits, and then give an overview of the available circuit structures. In Chapter 4, we will then describe the implementation of a radiation-hard delay generation circuit with a resolution of 1ns.

3.1 Definitions

In the following we will define some measures to characterise circuits for generating delays.

Resolution and Accuracy

The measured delay τ_n for a programmed delay step n is given by

$$\tau_n = t_0 + n \cdot \Delta t + \delta_n, \quad (3.1)$$

where t_0 is the intrinsic zero-tap delay, Δt is the delay step value defining the circuit's **resolution**, and δ_n is the deviation from the ideal value. The accuracy of the circuit is commonly measured by the **differential nonlinearity**

$$dnl_n = \delta_{n+1} - \delta_n \quad (3.2)$$

and the **integral nonlinearity**

$$inl_n = \delta_n \quad (3.3)$$

Both differential and integral nonlinearity are a function of the tap number n . To summarise the overall quality of a circuit it is convenient to calculate their standard deviation and peak-to-peak range over all N delay taps.

Monotonicity

A delay characteristic is said to be monotonic, if for all n

$$\tau_{n+1} > \tau_n. \quad (3.4)$$

Hence, increasing the delay step value n must also result in an increase of the measured delay. Monotonicity is an important property of a delay generation device, since it allows to search for an optimum delay of a signal without getting caught in local minima.

Signal Classification

The input signals can be classified into three groups

- (a) Periodic (frequency known and constant)
- (b) Synchronous
- (c) Asynchronous

Periodic signals with a frequency, which is constant and known, e.g. the clock, have the following properties

- (a) They provide an inherent timing reference. Hence, the timing generation circuit can use the signal itself to calibrate delay values.
- (b) The delay range is limited to one cycle time.
- (c) Delay values greater than the cycle time are mapped onto the delay value modulo the cycle time.

While property (a) can be exploited for the calibration of the delay elements, properties (b) and (c) can be used to increase the resolution by adding up two or more coarse delays as described in Section 3.4.2.

Synchronous signals are aligned to the clock, which allows to use certain delay generation techniques (e.g. pipelining) not available for the most general case of asynchronous signals. Furthermore, since the timing of synchronous signals is defined with respect to the clock signal, they can benefit from the fine-delay generation techniques for periodic signals by re-sampling the synchronous signal with a phase-shifted clock. (See also Chapter 9.)

In the next sections we will discuss the various methods for generating delays.

3.2 Digital Pipeline

The simplest method of delaying digital signals is the pipelining method, as shown in Fig. 3.1. A signal runs through a shift-register, and a multiplexer then chooses the n -th output, corresponding to a delay of n clock cycles. With this purely digital method very long delays with excellent differential and integral linearity can be achieved. The signal has to be either synchronous, i.e. aligned in phase with the clock, or must be sampled before. In the latter case, the peak-to-peak jitter is then at least one clock cycle time. The achievable resolution is very much limited by the maximum clock rate of the registers in the pipeline. Therefore, it is 1-2 orders of magnitude lower than what can be achieved with analog methods (e.g. delay locked loops).

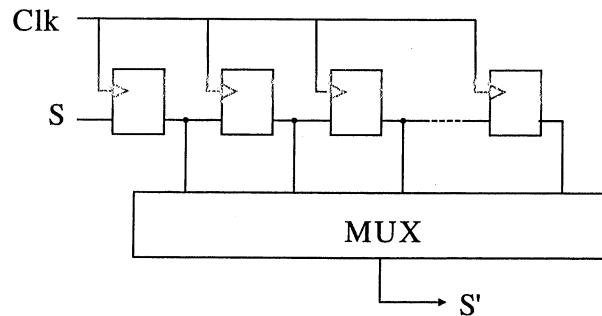


Figure 3.1: Delay generation by digital pipeline.

3.3 Passive Delayline

Passive delay lines, schematically shown in Fig. 3.2, consist of distributed RC-delay lines and a multiplexer to select one output. They can be used to achieve very high resolution, in the order of 10ps. Since the edge travelling in the delay line smoothens out with distance, their maximum delay range is limited. Calibration of passive delay lines can be achieved by changing a variable capacitance individually at each node. It is however difficult to achieve equidistantly spaced time intervals, which can be scaled by a common control voltage.

3.4 Voltage-Controlled Active Delayline

A voltage-controlled delay line (Fig. 3.3) consists of a chain of k identical delay stages, with each cell having a delay depending on the control voltage V_c . A multiplexer selects one of the outputs. The delay cells can be made of, for instance, two current-starved CMOS inverters in cascade, shown in Fig. 3.4. Symmetry between rising and falling signal edges

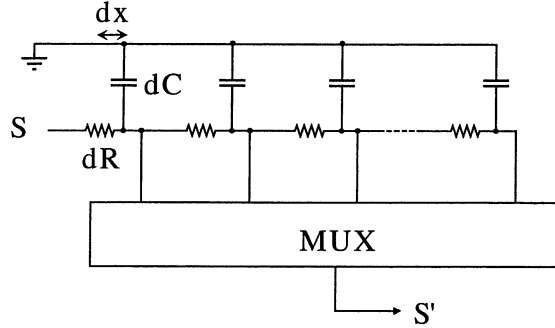


Figure 3.2: Delay generation by passive delay line.

requires that both inverter cells are identical (and also identically loaded).¹

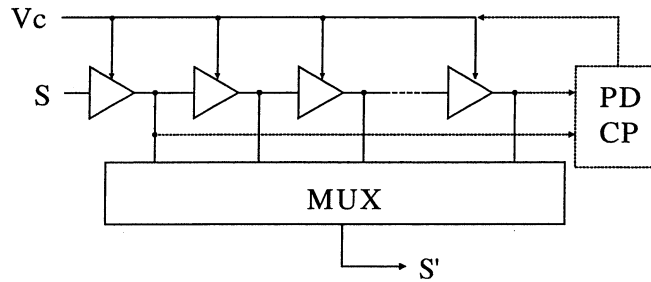


Figure 3.3: Voltage-controlled active delay line and DLL.

3.4.1 Delay Locked Loop (DLL)

If the input signal is periodic, a delay-locked loop [JOHU-88] can be built by adding additional circuitry to the delay line: A phase detector compares the rising edges of the zeroth and the last (n -th) tap. It then adjusts the control voltage V_c such that the overall delay is equal to one period of the input signal. Hence the period is divided into n equidistantly spaced intervals. The so-adjusted control voltage V_c is a useful byproduct, which can be used to define the delay of asynchronous signals in matched slave-delay lines². The achievable time resolution is in the order of 3-4 maximum inverter delays for a given technology. No high frequency clock is needed, so the power consumption is relatively low.

¹In contrast to the NMOS and PMOS branches of the current-starved inverter, which do not necessarily have to be symmetrical.

²As demonstrated in the next Chapter.

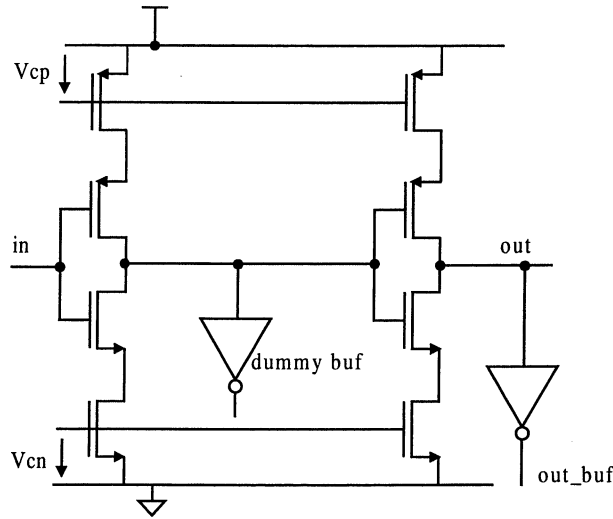


Figure 3.4: Delay element consisting of two starved inverter cells. To achieve symmetry for rising and falling edges both stages have to be identical.

3.4.2 Two DLLs in Cascade

To generate delays for periodic signals with sub-gate delay resolution, the Vernier delay generation method [CHRI-95a] can be used: Two delay generation stages are cascaded, one divides the clock cycle in intervals of N steps, the second in M steps. The resulting resolution is then the clock period divided by the least common multiple of M and N . An implementation of a phase shifter circuit using two DLLs will be presented in Chapter 9. The achievable accuracy is mainly determined by the matching of the delay cells and cross-talk between two output signals.

3.5 Delay Interpolation

If a signal is available together with a precisely delayed version of it³, delay interpolation [KNOT-94, YANG-96] can be used to increase the timing resolution. A delay interpolation circuit weights and mixes the two input signals, as seen in Fig. 3.5, thereby achieving delays in the interval defined by the two input signal edges. Although the achievable resolution is high, it is difficult to achieve linear fine delay spacing within the interval.

3.6 Ramp Generation

In a method which is found in commercially available circuits [ANDE-97, DALL-98], time is measured by ramping up a voltage on a capacitor and comparing it against a stable reference voltage. As seen in Fig. 3.6, one ramp is used for the rising edge, and one for the

³which can, for example, be tapped from a DLL

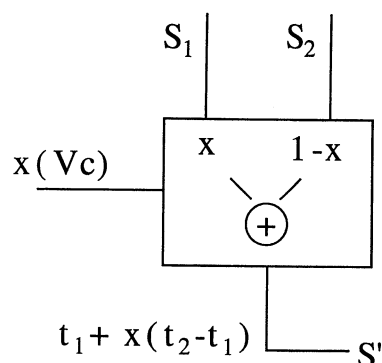


Figure 3.5: Delay interpolation circuit.

falling edge. The delay is chosen by setting the charging current of the capacitor with a current DAC. In order to achieve high accuracy the current has to be well defined. Hence, laser trimming [DALL-98] must be used to overcome process variations. Although not found in present applications, it would also be possible to define the current by a reference clock signal through a DLL.

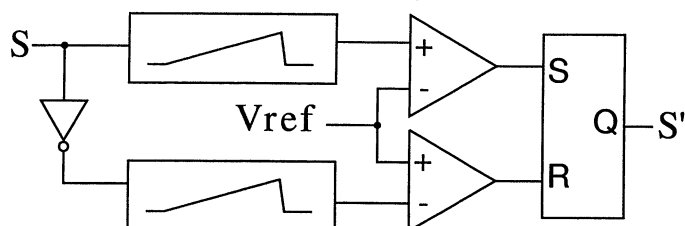


Figure 3.6: Delay definition through ramp generation.

Chapter 4

4-Channel Rad-Hard Delay Generation ASIC

In the previous chapter, we described the various methods available to generate precise delays of digital signals. We mentioned that, since the properties of integrated circuits depend on process variations, temperature, supply voltage and radiation dose, it is necessary to use an external timing reference for calibration. In this chapter, we describe the implementation of a 4+1¹ channel delay generation ASIC [PHOS-98, TOIF-99], which uses the 40 MHz LHC clock for this purpose.

The delay of four asynchronous signals and one clock channel can be independently programmed with a timing resolution of 1ns and a total range of 0-24 ns. The circuit will be used at various locations within the synchronisation systems² of ATLAS and CMS.

The timing calibration is based on a Delay-Locked loop (DLL), which regulates the time the clock signal travels in its delay line such that it amounts to exactly one period of the reference clock. The so-derived delay control voltage V_c is then applied to the four slave delay lines. Since the slave delay lines are matched to the delay line in the DLL, the timing calibration is effectively transferred to the four slave delay lines. By tapping the signal at different positions in the delay line with a multiplexer, delay values of an integer fraction of the reference period (in this case 1/25 of 25ns) can be generated.

The delay values of the four signal channels and the clock channel can be individually programmed via an I2C interface [SIGN-92]. Due to an automatic reset logic, the chip does not need an external reset signal. A first version of the chip was developed in a standard (non-rad-hard) 0.8 μ m technology, and the successful prototype was then transferred to the radiation-hard DMILL process.

Fig. 4.1 shows the basic architecture of the chip. Its central part is a DLL, which locks to the external 40 MHz clock. The four signal channels contain voltage-dependent delay lines receiving their control voltage from the DLL. The digital part of the circuit consists of an I2C interface and an automatic reset generation / initialisation logic.

¹Beside the four asynchronous signal channels also the delay of the clock channel can be programmed.

²The initial application was in the Liquid Argon Calorimeter of ATLAS [ATLA-96], where the chip was required to select the optimum time to sample the signal coming from the detector.

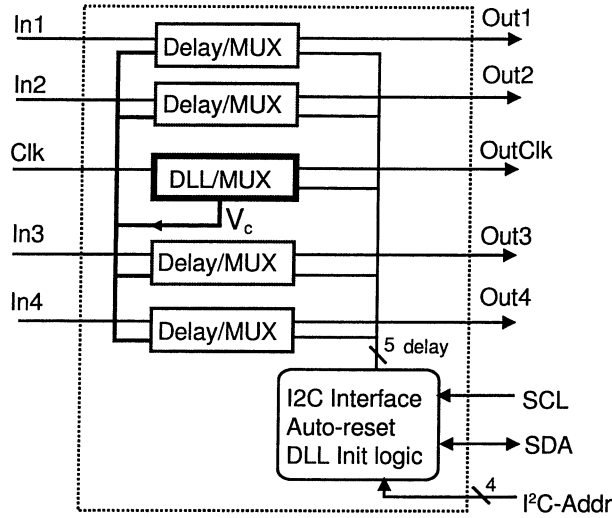


Figure 4.1: Block diagram of the delay generation chip. The delay-locked loop (DLL) is synchronised to the 40 MHz LHC clock, thus deriving the delay control voltage V_c . Four slave delay lines are then controlled by this voltage.

A block diagram of the DLL is shown in Figure 4.2³. It consists of a voltage-controlled delay line, a phase detector, a loop filter, a charge-pump and a voltage converter / buffer circuit. The delay line is a chain of 2×24 current-starved inverters⁴ [WEST-93]. The variable current sources in the current-starved inverter cells are controlled by voltages V_{cn} and V_{cp} . The V_c/V_{cnp} -Converter circuit of Fig. 4.2, on the one hand, derives V_{cn} and V_{cp} from V_c , and, on the other hand, acts as a buffer in order to avoid any coupling from the signal channels to the DLL. The outputs of the delay line are fed into a multiplexer, which then chooses one of the 25 delayed clock signals.

The signal edge coming out at the end of the delay line is compared with the incoming clock signal through a phase-detector, deriving a binary decision whether the signal delay was greater or smaller than one period of the reference clock (25ns at 40MHz). The phase-detector is implemented as a balanced flip-flop [JOHU-88]. The decision of the phase-detector (either *early* or *late*) is used to control a charge-pump, which adds or removes charge on a capacitor forming the loop-filter, thus increasing or decreasing V_c and its associated delay value. The slave delay lines receive the common control voltage V_c from the DLL, which is then fed into an identical V_c/V_{cnp} -Converter circuit to generate local versions of V_{cn} and V_{cp} .

³The layout of the DLL is shown in Fig. G.2 of page 119.

⁴Additional delay elements were added, however, at the beginning and at the end of the delay line in order to define the signal shape for tap zero, and to achieve equal loads for both phase detector inputs.

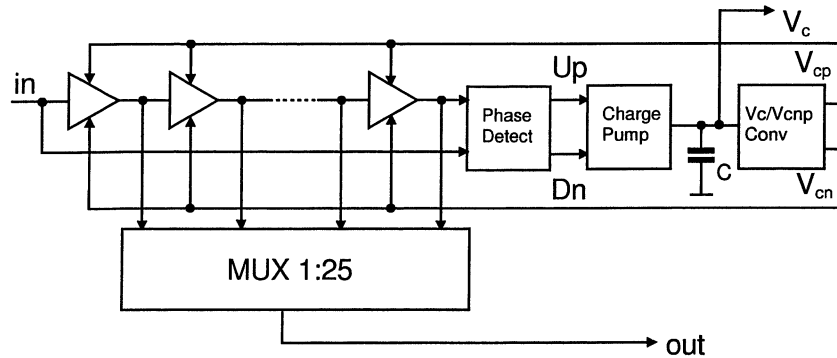


Figure 4.2: Delay-locked loop architecture: The incoming signal edge travels along a delay chain, where the overall delay is a function of V_c . A phase detector compares the so-delayed edge to the next edge of the reference signal. Depending on the decision of the phase detector, V_c is either decreased or increased, thus keeping the delay at exactly 25ns.

4.1 Matching Considerations

Process parameters, such as the MOS transistor transconductance β , threshold voltage V_t , and (gate or diffusion) capacitances C are not exactly identical over the whole chip area. Pelgrom showed [PELG-89] that there are two different causes for mismatch: One is short-distance mismatch due to local statistical variations in the fabrication process, the other is referred to as long-distance mismatch, which is caused by a slowly varying gradient of parameters over the wafer.

Let σ_1^2 denote the variance of the delay time of a single delay element. It can be shown that in a DLL structure, where the sum of all delay times is forced to equal the cycle time, the maximum value of the expected integral nonlinearity appears in the middle of the delay chain, with a variance given by $N\sigma_1^2/4$. (A derivation can be found in Appendix A.) The slave delay lines receive the control voltage from the DLL and do not have a feedback loop which would adjust the overall delay to exactly one cycle. Therefore, the maximum integral nonlinearity is expected to occur at the end of the delay line with a variance of $N\sigma_1^2$. Hence:

The matching requirements in a closed loop are 4 times less severe than in the case of an open structure.

Since the variance of the device parameters is inversely proportional to the transistor area [MICH-93], large devices were used in the chain of starving inverter cells and the V_c/V_{cnp} -Converter circuit. On the other hand, the structure was made as compact as possible in order to avoid long-distance effects. Although no precise matching parameters were available from the manufacturers at design time, a simple analysis of matching in the delay-chain was instructive, which is outlined in Appendix B.

As the analysis shows, in order to achieve good delay matching, it is necessary to avoid low values of $V_{gs} - V_t$ in the delay line transistors.

Another source of mismatch are shadow effects from surrounding structures, which were circumvented by using exactly the same layout in the DLL as in the slave delay lines (Fig. 4.3)⁵, with the exception that the phase detector and the charge-pump, although present in the layout, are deactivated. The power supply rails were designed to be wide enough not to affect the delay properties due to voltage drops induced by the supply currents.

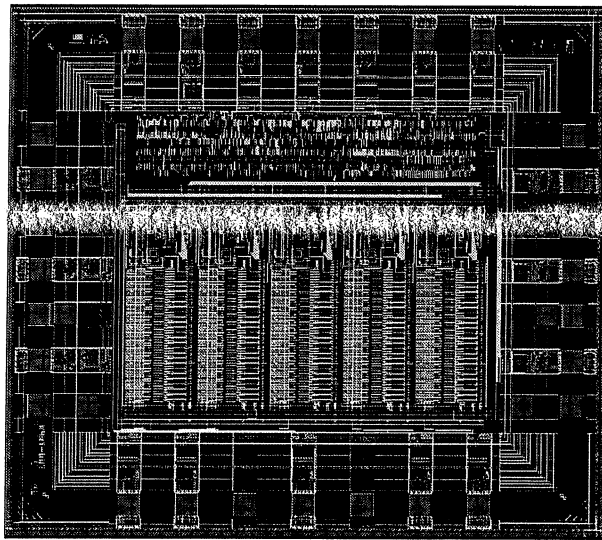


Figure 4.3: Layout of the delay generation ASIC (standard $0.8\mu m$ technology). The upper third contains the digital logic, the lower part the layout of the DLL (centre), surrounded by the four slave delay lines. The chip dimensions are 2.6×2.5 mm².

4.2 Digital control logic

The chip contains an I2C interface, which allows the user to program the delays in the four signal channels and in the clock channel. Since no reset signal was provided at the system level, the chip was designed to have an automatic reset logic. At the first activity on the I2C clock line after power-up, a sixteen bit wide register is compared against a constant hard-wired binary word. If the register content is different from this number, an internal reset signal is activated and an initialisation procedure is started, which guarantees that the DLL properly locks to exactly one clock period.

⁵See also Fig. G.1 on page 117.

4.3 Measurement results

4.3.1 Non Radiation-Hard Version

Figures 4.4 - 4.7 contain the results of the non-radiation-hard version of the chip. The curve displayed in Figure 4.4, showing the measured delay vs. programmed delay, demonstrates the correct operation of the circuit. To quantify the differential nonlinearity, the distribution of the delay steps is calculated as shown in Figure 4.5. The RMS value of the deviation from the nominal value was found to be 26ps.

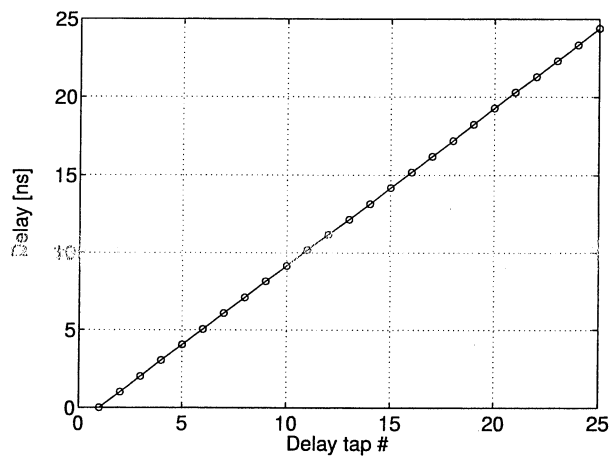


Figure 4.4: Measured delay vs. programmed delay. (Non-rad hard version)

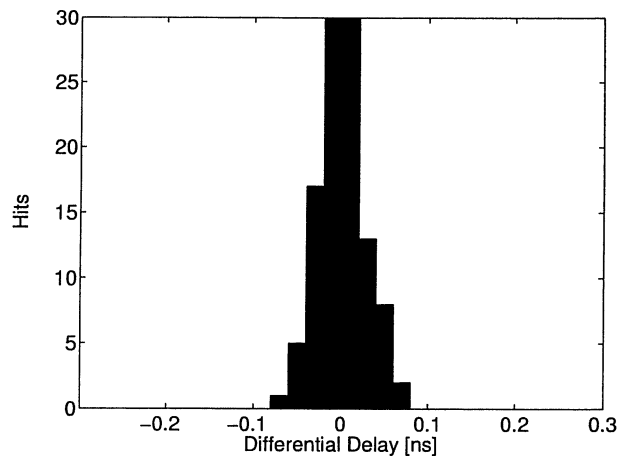


Figure 4.5: Distribution of differential delay steps. (Non-rad hard version). The RMS value of the differential nonlinearity amounts to 26ps.

The integral nonlinearity of the circuit is shown in Fig. 4.6. It can be seen that the delay channels adjacent to the DLL in the chip layout (Channel 2 and 3) are confined to

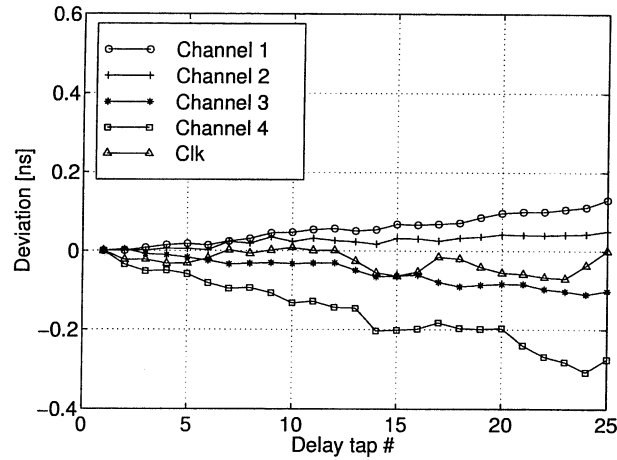


Figure 4.6: Integral deviation of the delay value from its nominal value.

a maximum deviation of less than 120ps. Using the result from Appendix A, this value approximately corresponds to the expected standard variation of $\sqrt{25} \cdot 26ps = 130ps$ at the last tap. The two outer delay channels (1 and 4) show larger deviations. This can be explained by the long-distance matching properties of MOS transistors [PELG-89] as discussed previously.

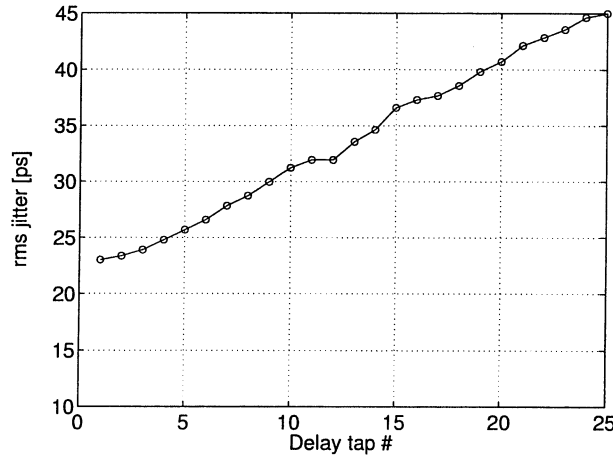


Figure 4.7: RMS Jitter as a function of the selected delay tap. (Non-rad hard version)

The jitter at the output of the chip as a function of delay tap is shown in Figure 4.7. The maximum jitter is measured at the last tap and amounts to 45ps rms.

The DLL alone dissipates 23mW at a supply voltage of 3.3 V, from which 17mW are static power consumption in the 5 V_c/V_{cnp} -Converter circuits, and 6mW are due to the 40 MHz clock signal rippling through the delay line. The additional power consumption in the signal channels amounts to 0.35mW/ (MHz · Channel) when driving a capacitive load of 15pF at the output.

4.3.2 Radiation-Hard Version

The radiation hard version of the delay generation chip was tested before and after irradiation to a total dose of 10Mrad. The irradiation was performed with an 10 keV X-ray machine and a dose rate of 10 krad/min. The circuit was connected to a 3.3 V power supply, and a 40 MHz clock signal at its input during irradiation.

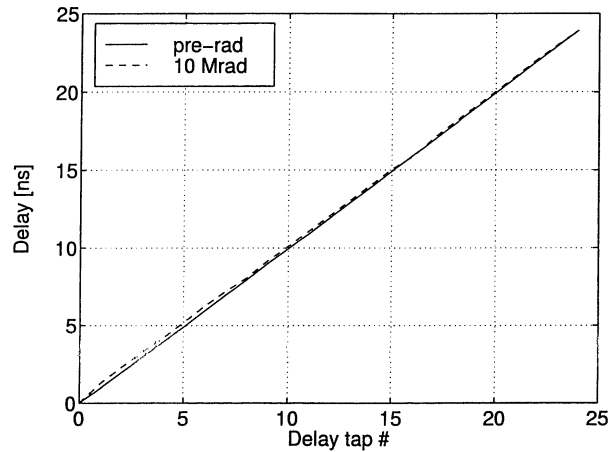


Figure 4.8: Measured delay vs. delay tap before and after an irradiation of 10 Mrad.

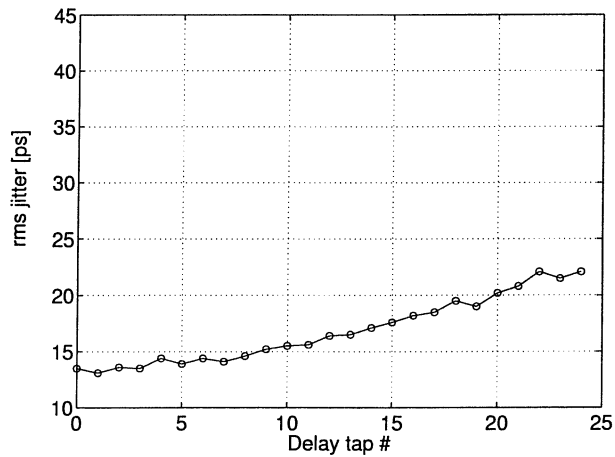


Figure 4.9: Measured jitter as a function of delay tap. (Rad-hard version)

Figure 4.8 shows the global characteristic of the circuit before and after irradiation. It can be seen that the circuit is fully functional after 10Mrad. Figure 4.9 shows the measured jitter before irradiation. The jitter value at the last tap is smaller than 25ps, which is lower than in the non-radiation hard version due to a reduction of the charge-pump gain. It was seen that the amount of jitter was not affected by radiation, hence showing the same low jitter even after 10 Mrad.

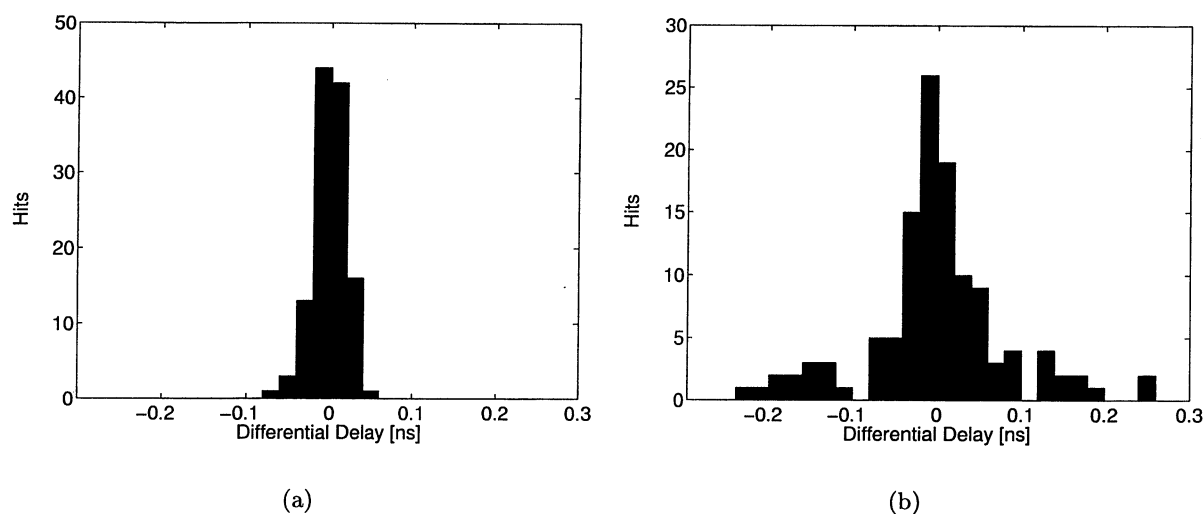


Figure 4.10: Differential nonlinearity before (a) and after (b) irradiation.

Figure 4.10 displays the distribution of the differential nonlinearity before and after irradiation. The non-irradiated chip displays very small deviations, which indicates good matching between the devices. In the irradiated chip, however, the difference between certain taps deviated by about 200ps from the ideal value of 1ns. Since these deviations were repeated with the periodicity of the multiplexer structure, it was deduced that they were due to radiation-induced mismatch in the multiplexer circuit. The reason for this is the following: Although the technology is radiation hard, the changes in V_t are not negligible. The amount of the V_t -shift caused by radiation depends on the biasing conditions, i.e. the gate-bulk voltage, of the transistor during irradiation. Hence, those branches of the multiplexer which were switched on during the irradiation process suffered a more severe degradation than the others. In fact, mainly the threshold voltages of the NMOS transistors got lower in the selected branch, making the devices slightly faster. This radiation effect, however, would be found in any multiplexer structure, and can only be avoided by continuously changing the value of the multiplexer selection input during irradiation.

Figure 4.11 displays the integral nonlinearity as a function of delay tap before and after irradiation. Before irradiation, all the channels are confined within a range of 150ps, which degrades to 550ps after irradiation. The signal channels adjacent to the DLL (Channel 2 and 3), however, do not deviate more than 300ps after irradiation. The basic power consumption of the rad-hard circuit before irradiation is 30mW, which increases to 36mW after 10Mrad. This is due to higher currents in the V_c/V_{cnp} -Converter circuit, and an increase in leakage current. The power consumption in the signal channels amounts to 0.35mW/ (MHz · Channel), which is not affected by radiation.

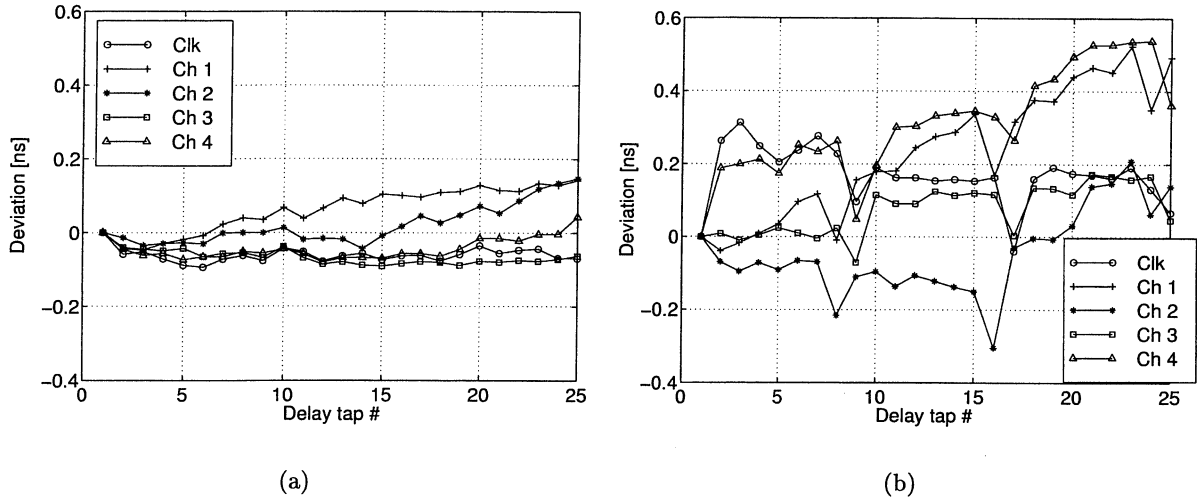


Figure 4.11: Integral nonlinearity before (a) and after (b) irradiation.

4.4 Conclusions

In this chapter, we presented the architecture, the implementation in both a radiation-hard and a standard $0.8\mu m$ technology, and the measurement results of an ASIC which delays digital signals with a resolution of 1ns by using a delay-locked loop (DLL) for its calibration. We discussed the various topics of matching, crucial for this type of circuit. The radiation-hard chip showed a maximum integral deviation of 150ps before irradiation. After a 10 Mrad of gamma-irradiation, the maximum integral deviation was measured to be 550ps in the outer channels, and 300ps in the two inner channels, which is well within the requirements of the application. The deviation was smaller for the two channels adjacent to the DLL because of long-distance matching effects. A very low maximum jitter value of 23ps rms was measured before and after irradiation.

Chapter 5

Distributing Timing Information

An important synchronisation task is the distribution of a low-jitter clock signal. A system where the clock is distributed together with synchronisation data was developed by the RD12 collaboration at CERN. This "Timing, Trigger and Control" (TTC) distribution system [TAYL-98] will be used in all future LHC experiments.

A block diagram of the TTC system is shown in Fig. 5.1. A high power laser transmitter delivers a Biphase Mark encoded 80 MHz bit stream to an optical fibre. The signal is then distributed through two levels of passive optical dividers with a total fan-out of 1024. At the end of the fibre, the optical input is converted to an electrical signal by a pin-photodiode with integrated pre-amplifier. The signal then enters a Receiver ASIC, which recovers clock and data from the Biphase encoded data stream.

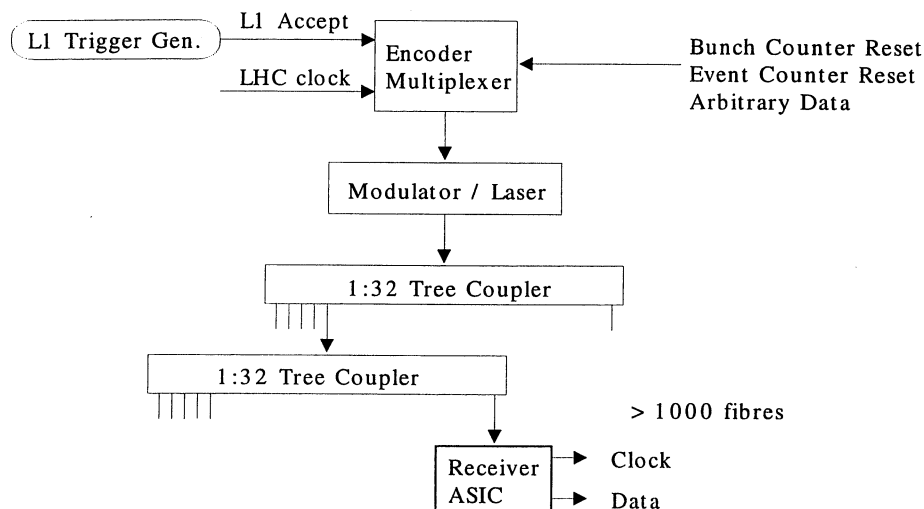


Figure 5.1: Block diagram of the Timing, Trigger and Control (TTC) Distribution System. The Level 1 Trigger signal is distributed together with other synchronisation data over an optical fibre system.

In the following we will concentrate on the receiver circuit, which performs the crucial

task of clock and data recovery. Its central part is a phase-locked loop.

5.1 Phase-Locked Loops for Clock Recovery

Phase-Locked Loops (PLLs) provide an important class of circuits for synchronisation purposes. Their main function is the phase alignment of an internal oscillator signal with an external reference signal. The reference signal can be either periodic (i.e. a square wave) or an encoded data stream, e.g. using a Biphasic encoding format. In the latter case, the PLL is then re-generating the clock signal associated with the data stream - hence it performs the important function of clock recovery. By using a PLL it is possible to filter out jitter from an imperfect input signal.

Fig. 5.2 displays a block diagram of a typical charge-pump¹ PLL [GARD-80]: A phase detector measures the phase difference between the input signal and the signal generated by an internal Voltage-Controlled Oscillator (VCO). According to the decision of the phase detector, a charge pump then conducts a current in or out the loop filter. This changes the VCO control voltage V_c and its associated frequency.

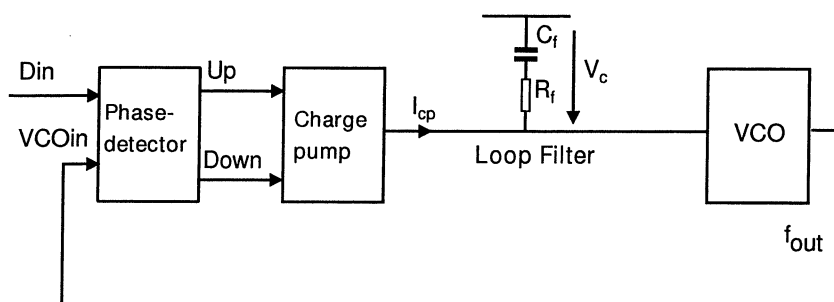


Figure 5.2: Basic components of a charge-pump PLL.

Various design aspects of Phase-Locked Loop components will be discussed in the next chapters. In Chapter 6, we will investigate how PLLs have to be designed in order to make them independent of transistor device parameters, which are changing with radiation dose, temperature and process variations. Chapter 7 gives an answer to the question of how to set the internal oscillator to the right frequency without using an external reference. Chapter 8 then describes the overall implementation of a radiation-hard clock and data recovery circuit. The circuit can be used stand-alone, but was also integrated in the "Timing Trigger and Control Receiver" (TTCrx) ASIC, described in Chapter 9, which contains a complete system-on-chip to distribute synchronisation data.

¹A charge pump is a device which conducts a constant (positive or negative) current for a time specified by the control signals *up* and *down*. In contrast to continuous-time PLLs with passive loop filter, charge pump PLLs have the advantage of zero static phase error.

Chapter 6

Design of Parameter Tolerant PLLs

In this chapter, we will investigate how a Phase-Locked Loops (PLL) can be designed in order to make it independent - or at least highly tolerant - to variations of device parameters. This is a necessary design practice since radiation effects further increase the parameter spread in MOS transistors. A high parameter spread means high uncertainty at design time, which can only be overcome by (a) setting system parameters¹ conservatively to allow worst case conditions, or (b) by providing means for programming system parameters during operation, which makes the utilisation of the device more difficult in a complex systems. A parameter-tolerant design practice thus allows to set system parameters close to their optimum value without having to program parameters during operation.

6.1 Principle of Parameter Independence

The loop dynamics in a PLL, which determine the stability of the system and its ability to filter out noise, depend on the type of VCO, loop filter, phase detector and charge pump used, and should be well controlled. Parameter variations due to a change in process parameters, temperature and supply voltage usually have a direct influence on the way the control loop behaves. Exposing the circuit to radiation changes the device parameters even more, and thus introduces an additional factor of uncertainty. Although present radiation hard technologies keep the parameter variations within limits, the drift of the CMOS transistor threshold voltage V_T and device transconductance β still cannot be neglected.

Hence, it is desirable to find structures, for which the reaction of the control loop is independent, or at least to a high degree tolerant, to these parameter changes. The aim of this chapter, therefore, is to analyse common charge-pump PLL structures and to determine the conditions for achieving a parameter-independent behaviour. For simplicity, we will only focus on second-order PLLs. First, we will investigate PLLs using a linear phase detector, i.e. the charge-pump is switched on to a time proportional to the measured phase difference, then we will focus on the case of a sample (or "bang-bang") phase detector, where the charge-pump is always switched on for a constant time. In each case, after deriving a general criterion for parameter independence, the concept will be tried out on two

¹e.g. the charge pump current

different differential oscillator structures commonly found in current PLL implementations [REYN-94, MANE-96, KIM-97].

6.2 Parameter Tolerant PLLs Using a Linear Phase Detector

A functional diagram of a charge-pump PLL with a linear phase detector is shown in Fig. 6.1. Θ_i and Θ_o denote the excess phases of the input and the VCO signals, respectively. The loop filter consists of a resistor R_f and a capacitance C_f , as shown in Fig. 5.2. The VCO is described by the gain constant K_v [Hz/V]. The charge pump is switched on for a time proportional to the phase difference Θ_e between the input signal and the VCO signal. Hence, the system is linear, but discrete in time due to the switching behaviour. If the loop bandwidth is small enough, however, the loop behaviour can be described by a continuous time approximation [GARD-80] and the analysis can be performed in the s-domain.

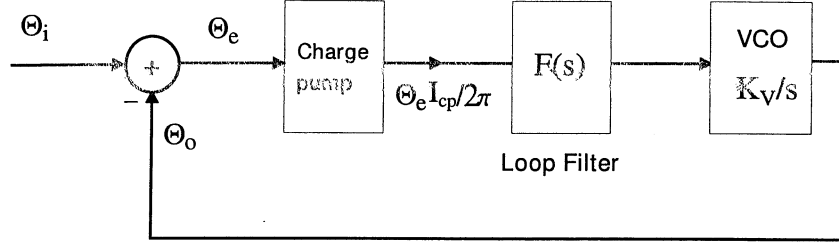


Figure 6.1: Charge-pump PLL with a linear phase detector.

The transfer function $H(s) = \Theta_o(s)/\Theta_i(s)$ is given by [RAZA-96]

$$H(s) = \frac{1 + sR_fC_f}{1 + sR_fC_f + s^2[\frac{C_f}{I_{cp}K_v}]}, \quad (6.1)$$

which can be written as

$$H(s) = \frac{1 + 2\zeta(s/\omega_n)}{1 + 2\zeta(s/\omega_n) + (s/\omega_n)^2}, \quad (6.2)$$

where ζ is the damping factor, given by

$$\zeta = \frac{1}{2} \cdot \sqrt{I_{cp} \cdot K_v \cdot R_f^2 \cdot C_f}, \quad (6.3)$$

and ω_n is the loop bandwidth [rad/s], given by

$$\omega_n = \sqrt{\frac{I_{cp}}{C_f} \cdot K_v}. \quad (6.4)$$

I_{cp} denotes the charge pump current, K_v the gain of the oscillator in [Hz/V], and R_f , C_f are the values of the resistor and capacitor in the loop-filter. In order to optimise the loop

performance, we want to control ζ and ω_n as accurately as possible. Ideally, ζ and the ratio of the loop bandwidth to the VCO frequency ω_n/ω_v should stay constant over all frequencies.

$$\begin{aligned}\zeta &= \text{const}, \\ \omega_n/\omega_v &= \text{const}.\end{aligned}$$

The VCO characteristic of common CMOS ring oscillators can be modelled by a function $f_v(V_c, V_t, \beta, C_o)$, describing how the VCO frequency depends on the loop control voltage V_c , the MOS threshold voltage V_t , MOS transconductance β , and the capacitance of the oscillator cell C_o . While V_c is controlled by the operation of the PLL, the device parameters are determined by the fabrication process, temperature, and changes due to irradiation. The VCO loop gain K_v with unit [Hz/V] is the derivative of $f_v(V_c)$ with respect to V_c ,

$$K_v = \frac{df_v}{dV_c} = f'_v(V_c). \quad (6.5)$$

We can now substitute K_v by $f'_v(V_c)$

$$\zeta = \frac{1}{2} \sqrt{I_{cp} \cdot R_f^2 \cdot C_f \cdot f'_v(V_c)}, \quad (6.6)$$

$$\omega_n/\omega_v = \sqrt{\frac{I_{cp}}{C_f} \frac{f'_v(V_c)}{(2\pi)^2 f_v^2(V_c)}}. \quad (6.7)$$

Examining eqs. (6.6) and (6.7), we can see that we have to adapt the parameters I_{cp} , R_f and C_f to achieve a constant behaviour. It is difficult to achieve variable capacitances, so we will only try to adapt the values for the charge pump current I_{cp} and the filter resistor R_f .

Solving eqs. (6.6) and (6.7) for I_{cp} and R_f results in expressions for the charge-pump current and loop-filter resistor

$$I_{cp}(V_c) = K_1 \cdot C_f \cdot \frac{f_v^2(V_c)}{f'_v(V_c)}, \quad (6.8)$$

$$R_f(V_c) = K_2 \cdot \frac{1}{C_f} \cdot \frac{1}{f_v(V_c)}, \quad (6.9)$$

with constants K_1 and K_2 defined as

$$K_1 = (2\pi)^2 \cdot \left(\frac{\omega_n}{\omega_v}\right)^2 \quad (6.10)$$

$$K_2 = \frac{1}{(2\pi)} \cdot \frac{2\zeta}{(\omega_n/\omega_v)} \quad (6.11)$$

Hence, for a given oscillator characteristic $f_v(V_c)$, parameter independence can be achieved for all frequencies provided that we can find a circuit structure generating I_{cp} and R_f according to (6.6) and (6.7).

Two types of differential ring oscillator structures, frequently used in today's PLL circuits, were analysed: one uses a simple MOS transistor as voltage-controlled resistor in the delay cell, while the other makes use of symmetric loads.

6.2.1 VCO with Simple Transistor as Voltage-Controlled Resistor

Figure 6.2 shows the first oscillator structure under investigation [REYN-94]. A single PMOS transistor in the ohmic region acts as a variable resistor. The frequency is controlled by changing the equivalent resistance via its gate-source voltage. A replica cell is used together with a differential amplifier to keep the voltage swing in the oscillator constant. It was verified in SPICE [NAGE-75] simulations that the relationship between frequency and control voltage is fairly accurately given by

$$f_v(V_c) = \frac{\beta_p}{2n \cdot C_o} (V_c - V_t), \quad (6.12)$$

where n denotes the number of delay stages in the ring oscillator, and C_o is the load capacitance of one delay stage.

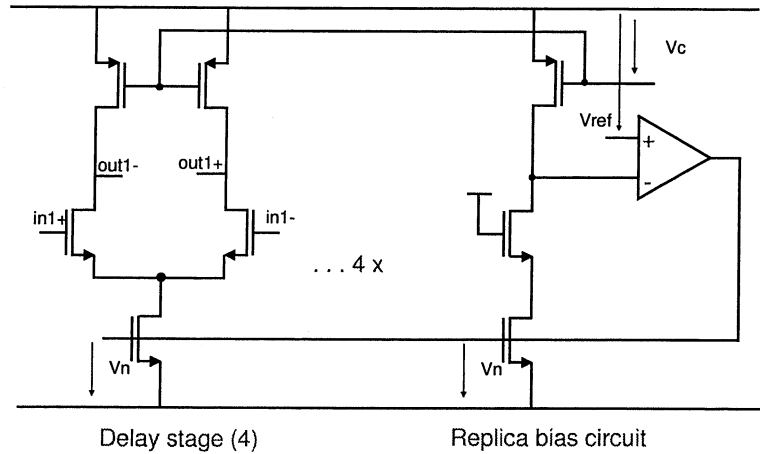


Figure 6.2: VCO with single MOS transistor as voltage-controlled resistor.

Fig. 6.3 displays the simulation results (circles) together with the prediction of (6.12). This relationship is only valid, however, when the load transistors stay in the linear region. The voltage swing used in the simulation was 1V, corresponding to $1.25V_t$. At the lower swing limit, the drain-source voltage V_{ds} of the PMOS load transistor therefore equals $-1V$. Keeping the load in the linear region requires

$$|V_{gs}| > |V_{ds}| + |V_t| = 2.25|V_t| \quad (6.13)$$

Hence, (6.12) is only accurate for $V_c > 2.25V_t$, which could also be verified in the simulation. By differentiating (6.12) we derive the oscillator gain

$$K_v = f'_v(V_c) = \frac{\beta_p}{2n \cdot C_o}, \quad (6.14)$$

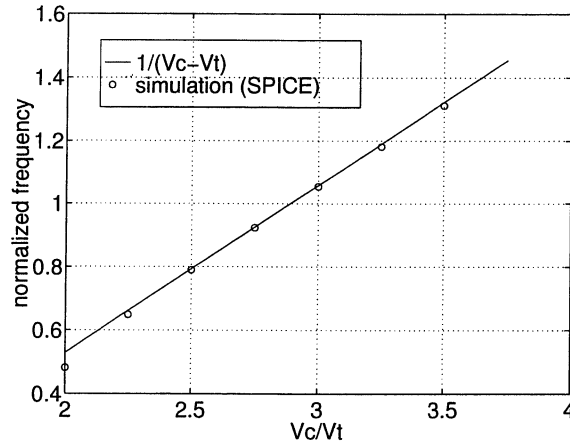


Figure 6.3: Frequency f_v vs. control voltage V_c in VCO with single MOS transistor as voltage-controlled resistor. Prediction according to (6.12) (solid), and simulation results (circles).

which can now be inserted together with (6.12) in the equations for parameter independence (6.6), (6.7).

$$I_{cp}(V_c) = K_1 \cdot \frac{1}{2n} \cdot \frac{C_f}{C_o} \beta_p (V_c - V_t)^2 \quad (6.15)$$

$$R_f(V_c) = K_2 \cdot 2n \cdot \frac{C_o}{C_f} \frac{1}{\beta_p (V_c - V_t)} \quad (6.16)$$

Eq. (6.15) has the form of the equation relating drain current to gate-source voltage in a long-channel MOS transistor. Hence, the charge pump current can be derived by a simple MOS current source with transconductance parameter β'_p [A/V^2]

$$I_{cp} = \frac{\beta'_p}{2} (V_c - V_t)^2. \quad (6.17)$$

Equating (6.17) with (6.15) and solving for β'_p results in

$$\beta'_p = K_1 \cdot \frac{1}{2n} \cdot \frac{C_f}{C_o} \cdot \beta_p. \quad (6.18)$$

The transconductance parameters β_p , β'_p [A/V^2] are defined as

$$\beta_p = \frac{W}{L} \mu_p C_{ox} \quad (6.19)$$

$$\beta'_p = \frac{W'}{L'} \mu_p C_{ox}, \quad (6.20)$$

with transistor width W' and length L' [m], channel mobility μ_p [$m^2/V \cdot s$], and oxide capacitance per area C_{ox} [F/m^2].

Substituting (6.19), (6.20) in (6.18) and combining with (6.10) results in

$$\frac{\omega_n}{\omega_v} = \frac{1}{2\pi} \cdot \sqrt{\frac{W'/L'}{W/L} \cdot n \cdot \frac{C_o}{C_f}}, \quad (6.21)$$

being defined by ratios of device sizes and capacitances, which can be very accurately reproduced in any CMOS technology.

To realise a resistor of the form (6.16), the filter can be implemented using the structure shown in Figure 6.4. A PMOS transistor with its gate connected to the V_c is used as a voltage-controlled resistor. Since the voltage drop along the resistor is reasonably small during the operation of the PLL, the equivalent resistance can be written as

$$R_f = \frac{1}{\beta_{p,f}(V_c - V_t)}, \quad (6.22)$$

with $\beta_{p,f}$ resulting from (6.16) in

$$\beta_{p,f} = \beta_p \cdot \frac{C_f}{C_o} \cdot \frac{1}{2n \cdot K_2}. \quad (6.23)$$

The damping factor ζ is then given by

$$\zeta = \frac{1}{2} \cdot \sqrt{\frac{(W'/L') \cdot (W/L)}{(W/L)_f^2}} \cdot \sqrt{\frac{C_f}{2n \cdot C_o}}, \quad (6.24)$$

which is also determined by ratios of device sizes and capacitances. We conclude:

For the case of an oscillator with single transistor loads operating in the linear region and a linear phase-detector, parameter-independent loop dynamics can be achieved for the whole frequency range by (a) deriving a charge pump current by a simple PMOS current source and (b) using the loop filter implementation of Figure 6.4.

6.2.2 VCO with Symmetric Loads.

As seen in Fig. 6.5, symmetric load elements are composed of two identical transistors, one of them connected to the loop control voltage V_c , while the second transistor is diode-connected. It is straightforward to show that the I vs. V_{ds} curve for this structure is indeed symmetric around $V_c/2$, which can be expressed as

$$I_{sl}(V_{ds}) = I_0 - I_{sl}(V_c - V_{ds}) \quad (6.25)$$

for a certain voltage V_c , I_0 being the current at $V_{ds} = V_c$. The voltage swing in the oscillator is regulated to equal V_c by a differential amplifier and a half-buffer replica cell. A VCO

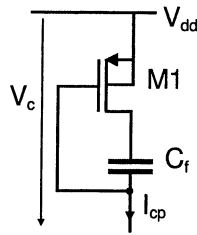


Figure 6.4: Filter structure to be used for parameter independence. Transistor M1 is used as a voltage-controlled resistor.

with symmetric loads and the structure of Fig. 6.5 has some desirable properties: First, the voltage controlled resistor resembles more an ideal resistor, at least for $V_c > 2V_t$, which makes the cell more immune to power-supply noise. Secondly, since the swing amplitude is equal to the control voltage, there is no need for a dedicated circuit to generate the swing-voltage, which would show some dependence on supply voltage. Hence, since one differential amplifier is sufficient to regulate the bias current with a replica biasing circuit, high power supply rejection can be achieved. Thirdly, the voltage swing becomes higher when the transistor transconductance parameter gets lower. A higher voltage swing directly translates to an improved immunity to thermal and substrate noise. This beneficially counteracts an increase in device noise caused by irradiation or an increase in temperature. As shown in

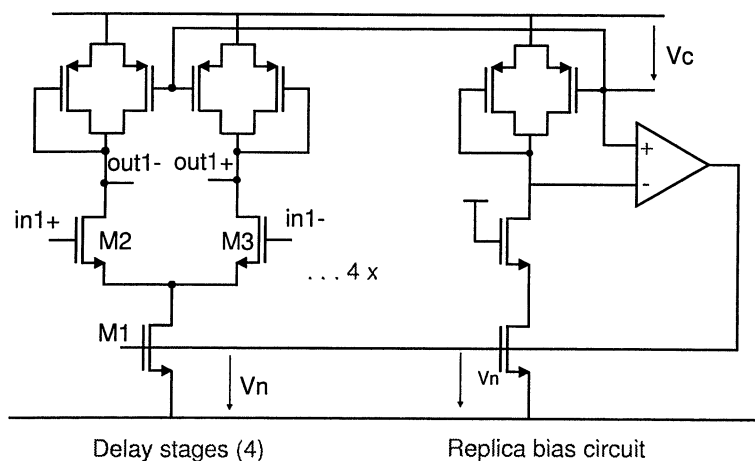


Figure 6.5: VCO with symmetric load as voltage controlled resistor.

Appendix C, the delay of a buffer stage with symmetric load elements can be expressed by

$$\Delta t(V_c) = \begin{cases} \infty & \text{if } V_c < V_t, \\ \frac{C}{\beta} \left[\frac{\pi}{2} \frac{1}{V_c - V_t} + \frac{2V_t - V_c}{(V_c - V_t)^2} \right] & \text{if } V_t < V_c < 2V_t, \\ \frac{C}{\beta} \left[\frac{\frac{\pi}{2} - \arccos \sqrt{\frac{(V_c - V_t)^2}{(V_c - V_t)^2 + (V_c - 2V_t)^2}}}{V_c - V_t} + \frac{\log \left(1 + \frac{(V_c - 2V_t)^2}{(V_c - V_t)^2} \right)}{V_c - 2V_t} \right] & \text{if } V_c \geq 2V_t. \end{cases} \quad (6.26)$$

This formula can be reasonably well approximated by

$$\Delta t(V_c) = \frac{C_o}{\beta_p} \frac{V_c}{(V_c - V_t)^2}, \quad (6.27)$$

which is much easier to use in further analytical investigations than (6.26). The frequency of an n -stage VCO can then be expressed as

$$f_v(V_c) = \frac{\beta_p}{2n \cdot C_o} \frac{(V_c - V_t)^2}{V_c} \quad (6.28)$$

In the literature [MANE-96], one can find the assumption of a $f(V_c)$ -characteristic of symmetric load VCO like the one found in the previous chapter for the simple MOS load

$$f_v(V_c) = \frac{\beta_p}{2n \cdot C_o} (V_c - V_t). \quad (6.29)$$

That a VCO characteristic given by (6.29) is incorrect, however, can be verified by using Figure 6.6, which displays the oscillator characteristic and its approximations resulting from the analytical solution, and Figure 6.7, which compares the predictions with the SPICE simulation: it can be seen that (6.29) is only a good approximation for $V_c > 3V_t$. The oscillator gain $f'_v(V_c)$, on the other side, is reasonably well approximated by a curve described by (6.29), as can be seen by comparing the slopes of the exact curve to the $1/(V_c - V_t)$ approximation.

The frequency characteristic of a differential oscillator using symmetric loads can be very well approximated by

$$f_v(V_c) = \frac{\beta_p}{2n \cdot C_o} \frac{(V_c - V_t)^2}{V_c}$$

Differentiating (6.28) results in

$$f'_v(V_c) = \frac{\beta_p}{2n \cdot C_o} \frac{(V_c - V_t)^2}{V_c^2}. \quad (6.30)$$

Inserting (6.28), (6.30) in (6.8), (6.9) yields expressions for the desired current and loop filter resistance

$$I_{cp}(V_c) = K_1 \frac{C_f}{C_o} \beta_p \frac{(V_c - V_t)^3}{(V_c + V_t)}, \quad (6.31)$$

$$R_f(V_c) = K_2 \frac{C_o}{C_f} \frac{V_c}{\beta_p (V_c - V_t)^2}. \quad (6.32)$$

Unlike the case of eqs. (6.15), (6.16), it is not possible to find simple structures fulfilling the equations. If the frequency range is limited and the supply voltage is high enough to guarantee $V_c > 3V_t$, however, then the oscillator characteristic (6.29) can be used. In this case, by selecting I_{cp} and R_f through (6.15) and (6.16) parameter independence can be achieved.

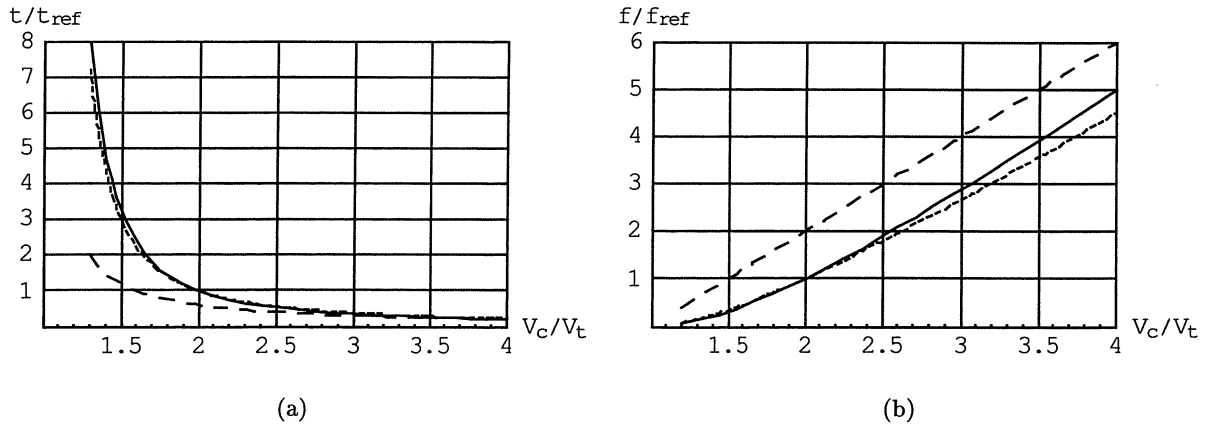


Figure 6.6: Δt vs. V_c/V_t (a), and f vs. V_c/V_t (b) in a symmetric load delay cell. Exact solution (solid), $1/(V_c - V_t)$ (dashed), and $V_c/(V_c - V_t)^2$ (dotted).

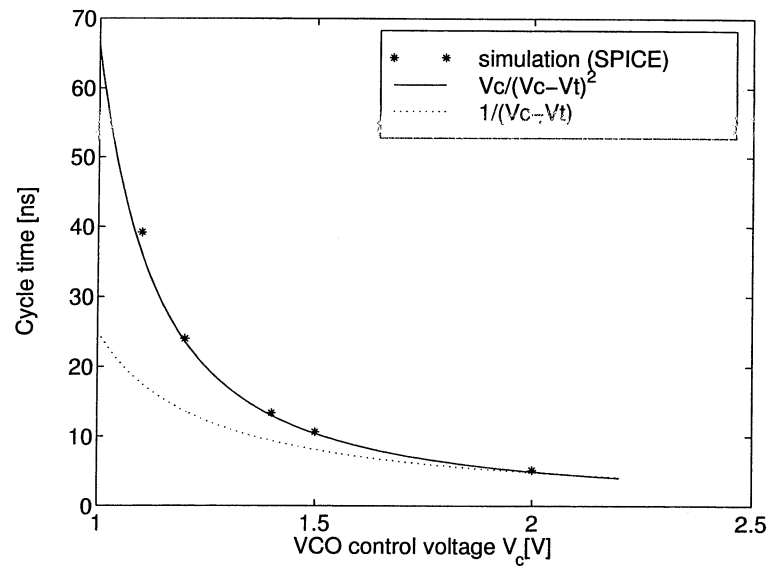


Figure 6.7: $\Delta t(V_c)$ in symmetric load VCO: Comparison of simulation results with predictions (6.27)(solid) and (6.29)(dotted).

6.3 Parameter Tolerant PLLs Using a Sample Phase Detector

In the case of a PLL with a sample (or "bang-bang") phase detector [TOIF-98b], as shown in Fig. 6.8, the charge pump is switched on for the whole cycle time. The response of the phase detector therefore is no longer proportional to the actual phase difference, but corresponds to the *sign* of the phase difference. Consequently, the phase detector is strongly non-linear, which does no longer allow the use of a Fourier- or Laplace transform to analyse the system. Therefore, a step by step analysis in the time-domain has to be performed.

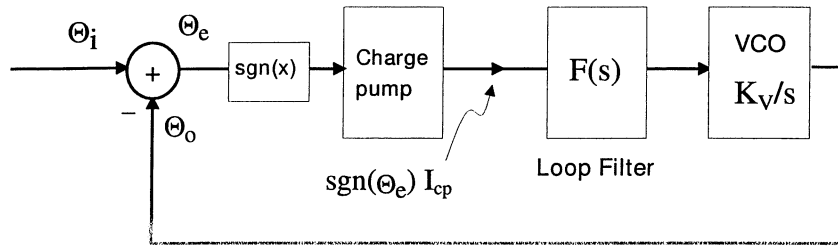


Figure 6.8: Charge-pump PLL with a sample phase detector.

Figure 6.9 shows the typical behaviour of the control voltage in a PLL with a bang-bang phase detector. The loop filter capacitance C_f is responsible for the integral part of the loop response, while the immediate jumps of V_c stem from the filter resistance R_f , thereby providing the proportional part. Since the changes of the control voltages are small, the changes in the loop delay per VCO cycle are proportional to ΔV_c .

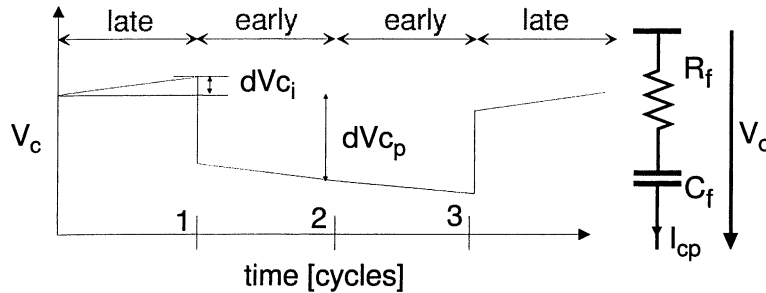


Figure 6.9: Typical behaviour of V_c in a PLL with bang-bang phase-detector.

$$\Delta T = \Delta V_c \cdot \frac{dT}{dV_c}, \quad (6.33)$$

where dT/dV_c is the derivative of the $T(V_c)$ curve of a given oscillator at the operation point V_{c0} . Assuming a constant charge-pump current I_{cp} and a cycle time T , the voltage change stemming from the proportional part equals

$$\Delta V_c^p = I_{cp} \cdot R_f, \quad (6.34)$$

and the voltage change from the integral part is

$$\Delta V_c^i = \frac{I_{cp} \cdot T}{C_f}. \quad (6.35)$$

Hence, the contributions to the change in one cycle are given by

$$\Delta T_p = I_{cp} \cdot R_f \cdot \frac{dT}{dV_c}, \quad (6.36)$$

$$\Delta T_i = \frac{I_{cp} \cdot T}{C_f} \cdot \frac{dT}{dV_c}. \quad (6.37)$$

In order to achieve stability in a bang-bang PLL, the proportional part should dominate over the integral part [WALK-92].

6.3.1 Criterion for Parameter Independence

Ideally, the ratio of the proportional part and the integral part to the cycle time should be well defined and not depend on device parameters

$$\Delta T_p/T = \text{const.}, \quad (6.38)$$

$$\Delta T_i/T = \text{const.} \quad (6.39)$$

Solving for $I_{cp}(V_c)$ and $R_f(V_c)$ results in

$$I_{cp}(V_c) = \frac{\Delta T_i}{T} \cdot \frac{C_f}{T'(V_c)} \quad (6.40)$$

$$R_f(V_c) = \frac{\Delta T_p}{\Delta T_i} \frac{T(V_c)}{C_f}. \quad (6.41)$$

By replacing $T(V_c)$ with $1/f(V_c)$, and $T'(V_c)$ with $f'(V_c)/f^2(V_c)$, eqs. (6.40) and (6.41) can be written as

$$I_{cp}(V_c) = K_1 \cdot C_f \cdot \frac{f_v^2(V_c)}{f'_v(V_c)}, \quad (6.42)$$

$$R_f(V_c) = K_2 \cdot \frac{1}{C_f} \cdot \frac{1}{f_v(V_c)}, \quad (6.43)$$

with constants K_1 and K_2 defined as

$$K_1 = -\frac{\Delta T_i}{T} \quad (6.44)$$

$$K_2 = -\frac{\Delta T_p}{\Delta T_i} \quad (6.45)$$

Equations (6.42), (6.43) have exactly the form of eqs. (6.8), (6.9) found for the case of a linear phase-detector. Hence the same analysis as in Section 6.2 applies.

For achieving parameter independence in a PLL with a bang-bang phase detector, the same structure as in the case of a linear phase-detector can be used with constants K_1 , K_2 given by (6.44) and (6.45).

6.3.2 Parameter Tolerant VCO with Symmetric Loads for a Single Frequency

In the previous section, we have seen that for the case of an oscillator with symmetric loads it is not possible to achieve parameter-independence for a broad range of frequencies. The assumption of a simple $f(V_c)$ relationship made in [MANE-96] proves only to be valid for $V_c > 3V_t$. The current trend, however, is to design for ever lower supply voltages, hence the range of V_c is limited. In the case of the PLL described in this thesis, the minimum supply voltage was given by $V_{DD,min} = 3.0V$ and $V_{tp} = 0.8V$ (typical). The maximum value of V_c is further limited by the requirement that for the NMOS transistor M1 in Fig. 6.5 to act as a current source, its drain-source voltage V_{dsn} has to be greater than $\Delta V_{n,max} = (V_{gsn} - V_{tn})_{max}$. The drain-source voltage of M1, V_{dsn} is related to the voltage swing (and control voltage) of the oscillator, V_c , through

$$V_{dsn} = V_{DD,min} - V_c - V_1, \quad (6.46)$$

where V_1 is the maximum drain-source voltage of the MOS transistor in the differential pair, which by simulation was found to be 0.4 V. Hence, a condition for V_c can be stated in order to keep M1 in saturation

$$V_c < V_{DD,min} - \Delta V_{n,max} - V_1. \quad (6.47)$$

Assuming $\Delta V_{n,max}$ to be 0.6 V results in a maximum value for V_c of 2.0 V, or $2.5 V_t$, which is already outside the region where (6.29) is a good approximation for the oscillator behaviour.

In the previous sections, we were looking for PLL structures having well defined loop behaviour not only independent of device parameters, but also independent of the actual VCO operating frequency. The simpler case, where the operating frequency is constant and known in advance, is also frequently found in many applications.

We can differentiate (6.27) in order to calculate the relative delay sensitivity

$$\frac{1}{T} \frac{dT}{dV_c} = -\frac{(V_c + V_t)}{V_c} \cdot \frac{1}{V_c - V_t}, \quad (6.48)$$

which can be written as

$$= -\gamma(V_c, V_t) \cdot \frac{1}{(V_c - V_t)}. \quad (6.49)$$

Since V_c is connected to T, V_t, β_p through (6.27), we can express γ as a function of these parameters

$$\gamma = \gamma(T, V_t, \beta). \quad (6.50)$$

It now turns out that for quite a broad range of variations in V_t and β_p , γ stays fairly constant. Figure 6.10 shows the value of $\gamma/1.6$ for the expected range of V_t drawn on the horizontal axis, and β_p as a parameter. As one can see, the deviation of γ is within a 5% range. Now, the charge-pump current can be derived proportional to $(V_c - V_t)$,

$$I_{cp} = \frac{V_c - V_t}{R_{ref}}, \quad (6.51)$$

resulting in a proportional part of the loop response

$$\frac{\Delta T_p}{T} = \frac{R_f}{R_{ref}} \cdot \gamma, \quad (6.52)$$

which is then accurately defined. The integral part of the loop response is given by

$$\frac{\Delta T_i}{T} = \frac{T}{C_f} \cdot \frac{\gamma}{R_{ref}}, \quad (6.53)$$

where T is given by definition. Thus, the accuracy of (6.53) is determined by the passive components R_{ref} and C_f . Of course, one could argue now, that in fact we have not gained anything, because we are now depending on the deviations of resistances and capacitances. Many analog technologies, however, offer precision resistors and capacitors, which are not as dependent on temperature and irradiation as the transistor device parameters.

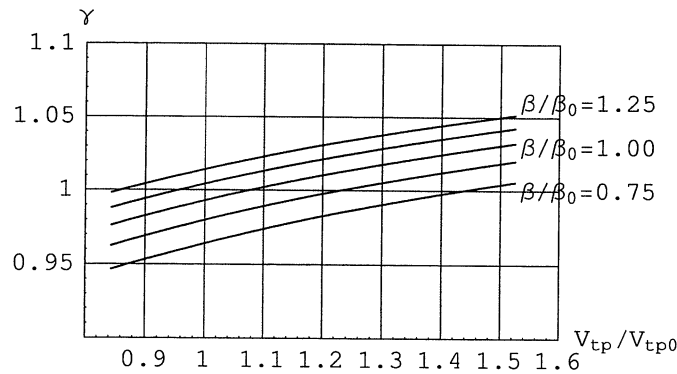


Figure 6.10: γ as a function of threshold-voltage for different values of β_p .

Measurement Results

The previous structure was used in a PLL to recover clock and data from an 80 MHz Biphase Mark bit stream². The jitter was measured as a function of temperature³, with results shown in Fig. 6.11. The input signal was a 0-1 Biphase Mark sequence generated by an HP 8110A pulse generator. It can be seen that the jitter only changes very little with temperature. It is only 2 ps lower at a temperature of 5°C than at 80°C, which can be explained by a reduction of oscillator noise.

6.4 Conclusions

In this chapter, we showed how the charge pump current and the loop filter resistance must relate to a given oscillator description $f(V_c)$ in order to achieve parameter-independent loop dynamics. For the case of a VCO using a single transistor in saturation we presented a structure which was parameter-independent for the whole frequency range of the VCO. For this kind of VCO and the given ratio between minimum supply voltage and V_T , the frequency range is however limited to $\pm 50\%$. VCOs with symmetric loads, on the other hand, are able to cover a very broad frequency range, but due to their $f(V_c)$ -characteristic it is impossible to find simple structures to achieve parameter-independence on the whole frequency range. Parameter tolerance can be achieved, however, if the VCO frequency is constant and known in advance, as was the case in our application.

²Further results of the PLL using the parameter-tolerant biasing can be found in Chapter 8.

³The temperature was measured on the back cover of the device.

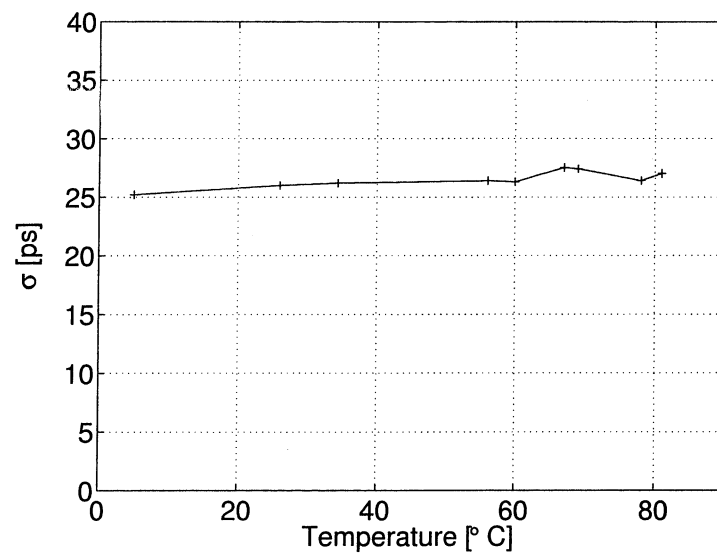


Figure 6.11: Effect of temperature on the standard deviation of clock jitter.

Chapter 7

Frequency Acquisition in Clock Recovery Circuits

The initial frequency of the Voltage-Controlled Oscillator (VCO) in a monolithic implementation of a clock-recovery PLL cannot be determined at design time, since it depends on variations in process, temperature, supply voltage and radiation dose. Therefore, a frequency detector circuit has to adjust the VCO control voltage until the oscillator frequency corresponds to the symbol rate of the input signal. After the target frequency is reached, a phase detector then can take over for phase-lock.

As seen in Fig. 7.1, the task of a frequency detector circuit is to compare the internal clock signal from the VCO to the incoming data sequence. It has to derive a decision, if the frequency of the clock signal should go up or down. Unlike the case of a simple square wave, it is not possible to define a signal period for a Biphasic or Nonreturn-to-zero (NRZ) encoded signal. As seen in Fig. 7.2, the time between two rising (of falling) edges depends on the

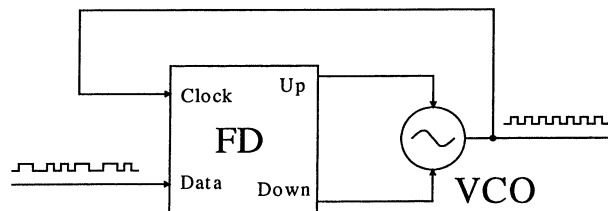


Figure 7.1: Basic function of a frequency detector. By comparing the *Clock* with the *Data* input, a decision (either *Up* or *Down*) is derived to control the VCO.

transmitted symbol. For the Biphasic Mark¹ case with bit period T_0 , the time between two rising edges can be either T_0 , if a Biphasic Mark One is transmitted, $2T_0$ for the case of a

¹The family of Biphasic codes consists of the Biphasic Mark, Biphasic Space and Manchester encoding schemes. Biphasic Mark and Space encodings have a fixed transition at the beginning of the symbol, Manchester encoding in the middle. A One in a Biphasic Mark code is encoded by an additional transition in the middle of the symbol, in the Biphasic Space code it is the opposite case, where the Zero has an additional middle transition. A Manchester encoded 0 corresponds to a 0-1 step, a One to a 1-0 step. From the viewpoint of frequency detection, however, all Biphasic codes look the same.

Biphase Mark Zero, or $3/2T_0$ if a Zero follows a One (or vice versa). The situation is even more complicated for a NRZ signal, where every multiple $nT_0, n > 2$ of the bit time can be found as period between two rising edges.

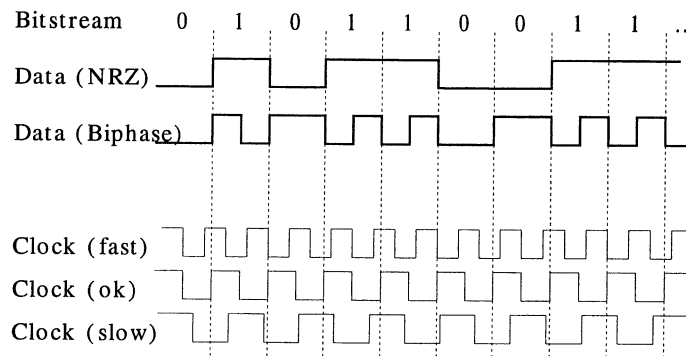


Figure 7.2: Properties of Biphase and NRZ data.

7.1 Available Solutions

Three solutions are commonly used to solve the frequency acquisition problem in monolithic implementations of clock recovery PLLs:

- (a) External frequency reference
- (b) Training sequence
- (c) Rotational frequency detector

In the case of an external frequency reference, an off-chip signal, e.g. coming from a quartz, is applied to the PLL to train the on-chip VCO to the data rate [CHEN-96, BANU-93]. A tri-state phase-frequency detector (PFD) [SHAR-76] works in this situation, because both the input signal from the quartz and the VCO signal are ordinary square-wave signals. After frequency acquisition, the PLL input is then switched to the incoming data stream in order to acquire phase-lock.

In the case of frequency acquisition with a training sequence [MIYA-91, RAU-97], the data protocol is defined such that the first part of the data stream is a square-wave synchronisation signal. Frequency lock can then be acquired during the duration of the square wave signal with a phase-frequency detector. This method is used, for example, for reading out data from hard disc-drives [MIYA-91].

The rotational frequency detector, proposed by Messerschmidt [MESS-79] as a digital implementation of the quadri-correlator [RICH-54], gives correct decisions also for Biphase and NRZ input signals. Hence, there is no need for a special training sequence. Fig. 7.3 shows the basic implementation of the rotational FD. Its principle of operation, shown in Figure 7.4, is the detection of cycle slips. The full cycle of the VCO is divided into four quadrants, A, B, C and D . The quadrant is encoded via two VCO clock signals in

quadrature. A transition on the data signal samples the two quadrature clock phases, and hence contains the information of the quadrant of the sampling instant. This value is then compared to the previous sample value of the quadrant. If the quadrant changed from *A* to *B*, as depicted in Fig. 7.4(a), then the VCO clock must be too fast. On the other hand, if the quadrant changes from *A* to *D*, as shown in case (b), then the VCO must be too slow. Fig. 7.4(c) displays the situation that the VCO frequency is below the lower frequency range of the FD. A transition from *A* to *B* is seen by the circuit, corresponding to the situation in (a). Hence, the (erroneous) decision will be that the VCO is too slow. The frequency discrimination range thus is limited to $\pm 50\%$ the data rate with a square wave input, and $\pm 25\%$ with random NRZ input [DEVI-96]. Therefore, in order to guarantee a frequency range inside the discrimination bandwidth, some applications require laser trimming of the VCO middle frequency [DEVI-96], increasing the cost of the circuit.

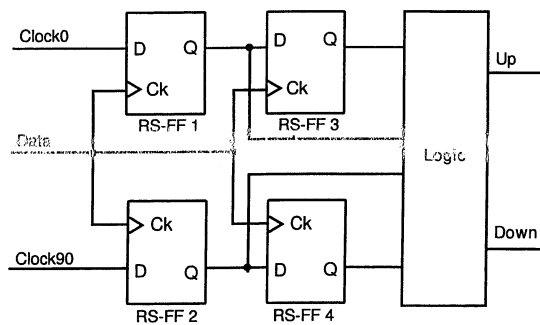


Figure 7.3: Rotational frequency detector implementation.

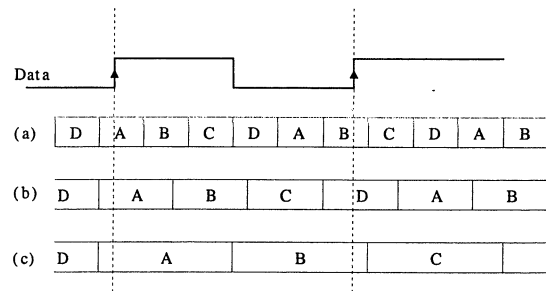


Figure 7.4: Rotational FD : principle of operation.

7.2 Novel Frequency Detector Circuit

A solution to the frequency acquisition problem had to be found for a radiation hard clock and data recovery circuit². Using an external frequency reference (option a) was prohibited since this would have required additional circuits to be tested for their radiation-hardness. Also the use of a training sequence (option b) was ruled out, since this would have led to complications at the system level. The rotational frequency detector (option c) was also not the ideal choice, because the oscillator had a very large frequency range, outside the rotational frequency detectors lower frequency limit of 50 %. Hence, a new circuit was developed, which will be described in the following. Although originally designed to be solely used with a Biphase Mark encoded signal, it turned out that the principle of the frequency detector can also be applied for Nonreturn-to-zero encoded input signals.

For the following discussion, we will assign the names *Data* and *VCO* for the Biphase Mark input signal and the signal from the oscillator, respectively. The basic version of the proposed frequency detector circuit [TOIF-98a] detects the condition of two consecutive

²See Chapter 8.

positive edges on *Data* without any positive edge on *VCO* in-between, as shown in Fig. 7.5(a). Hence it follows:

The VCO period is compared to the *smallest period between two rising edges* of the incoming data stream.

The resulting "frequency-too-low" signal is maintained until the next rising edge of the incoming data signal. If the VCO period is smaller or equal to the smallest data transition period, however, then there is always at least one rising edge on *VCO* between two rising *Data* edges and no further "frequency-too-low" events can be detected. The case that the VCO frequency is too high is shown in Fig. 7.5(b). Here, the condition is detected that the Data signal stays high during a time longer than one clock period. It is clear that for the detection of a "frequency-too-low" event, a short period of the Biphase code is needed (e.g. a Biphase Mark One), whereas a long period (a Biphase Mark Zero) is required for the "frequency-too-high" detection. Assuming that symbols One and Zero are randomly distributed in a Biphase Mark or Manchester code, both conditions will be detected. The "frequency-too-low" and "frequency-too-high" signals are then used to control the VCO via a charge pump.

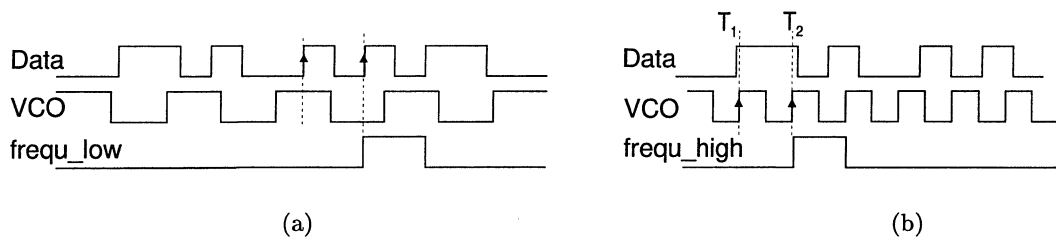


Figure 7.5: A "frequency-too-low" condition (a) is detected when there is no rising edge on the VCO signal between two rising edges on the data signal. A "frequency-too-high" condition (b) is detected when there is no transition on the Data signal between two rising edges of the VCO signal.

7.2.1 Implementation

The "frequency-too-low" events can be found through the aid of a signal containing the information, on which of the two incoming signals (*VCO* or *Data*) the last positive edge occurred. This signal can be generated by a "Last-Positive-Edge" (LPE) detection circuit, which is discussed below.

Sampling the output signal of the (ideal) LPE circuit at the rising edge of *Data* results in the correct output of the frequency detector (Fig 7.6).

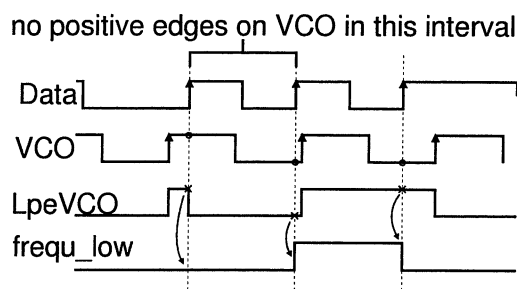


Figure 7.6: The principle of operation of the frequency detector circuit. When high, the signal *LpeVCO* indicates that the positive edge of *VCO* was last. Sampling the signal with the rising edge of *Data* results in the correct *frequ_low* signal (after inversion).

In practice, however, the situation is more involved, due to the finite response time of the LPE circuit and the setup time requirement of the sampling flip-flop. Hence, sampling only the output of the LPE circuit would sometimes result in a false detection of a "frequency-too-low" condition. This situation is shown in Fig. 7.7: Although there are never two consecutive positive edges of *Data* without a positive edge on *VCO*, *frequ_low* is asserted erroneously.

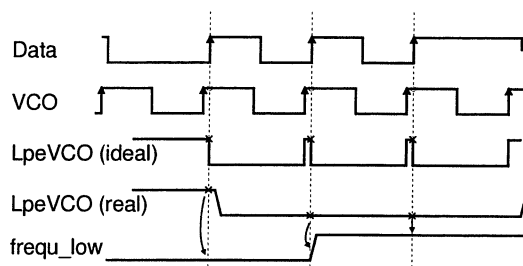


Figure 7.7: Erroneous detection of a "frequency-too-low" event due to the response time of the LPE circuit.

A basic version of the proposed circuit which overcomes this problem is shown in Fig. 7.8. Besides sampling the output of the LPE circuit *LpeVCO*, which becomes high when the last rising edge occurred on *VCO*, also *VCO* itself is sampled at the rising edge of *Data*. By using a balanced flip-flop [JOHU-88], which is designed to have zero setup time, the arrival times of the signal edges can be accurately compared. The "frequency-too-low" condition is detected when the samples of both signals (*VCO* and *LpeVCO*) are zero, meaning that the positive edge of the *VCO* signal has not yet arrived at the sampling instant. The *frequ_low* signal can finally be derived by a NOR gate.

In a refined version of the circuit (Figure 7.9), the OR operation is moved in front of the sampling operation, which requires one flip-flop less. To achieve symmetry in the delay paths, however, the *Data* signal has to run through a dummy OR gate, the other input connected to ground.

To be able to detect the case that the *VCO* frequency is too high, the circuit can be

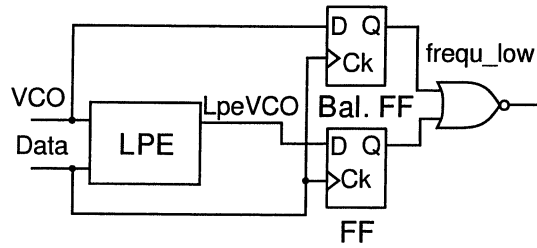


Figure 7.8: Basic version of the proposed frequency detector circuit.

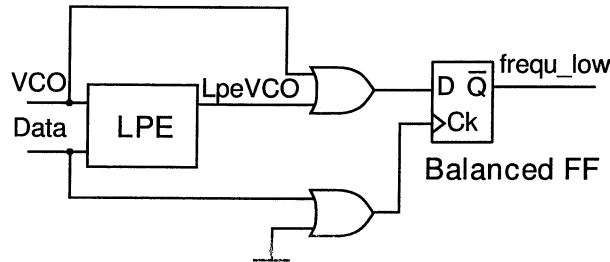


Figure 7.9: Modified version of the proposed frequency detector circuit, using only one flip-flop.

extended, as shown in Fig. 7.10. According to the principle of Fig. 7.5(b), a "frequency-too-high" event is detected when *Data* stays high for more than one clock period. This condition is met when a) a One is sampled on *Data* at T_2 , and b) the last positive edge occurred on the *VCO* signal. Unlike the case for the "frequency-too-low" condition, now the falling edge of *Data* has to race against *VCO*. Since a balanced flip-flop can only compare rising edges, the negated *Data* input must be used. In the case that a rising edge on \overline{Data} would occur immediately before the sampling time T_2 , the LPE circuit would not change fast enough, and a false "frequency too high" condition would be detected, a situation which can be seen in Fig. 7.11(b): Although the *VCO* frequency is higher than the data rate, NORing the samples of *LpeData* and \overline{data} would result in the detection of a "frequency-too-high" condition. To solve this problem, the \overline{Data} signal, delayed by a time $\tau > \tau_{LPE}$, with τ_{LPE} being the time from the arrival of the positive edge on *Data* to the assertion of *LpeData*, must also be considered in the decision. Only when the samples of all *LpeData*, \overline{Data} , and \overline{Data}_{del} are zero, the "frequency-too-high" signal is asserted.

7.2.2 LPE Circuit

The LPE circuit must accurately compare the arrival times of the rising edges of two incoming signals and outputs the information, which of the two signals was last. A simple version of an LPE circuit can be seen in Figure 7.12. A positive edge in either the *VCO* or *Data* signal provokes a negative impulse on *VCO'* or *Data'*, setting or resetting the RS-flip flop. In the case that the impulses are overlapping, the RS-FF will remain in the state defined by the signal (either *VCO'* or *Data'*), which was the last to go high again. It is to

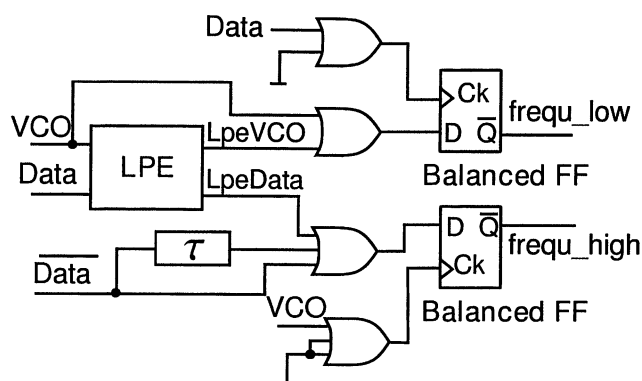


Figure 7.10: Extended Biphase frequency detector. The lower branch detects the condition that there is no transition of the Data signal during two rising edges of VCO.

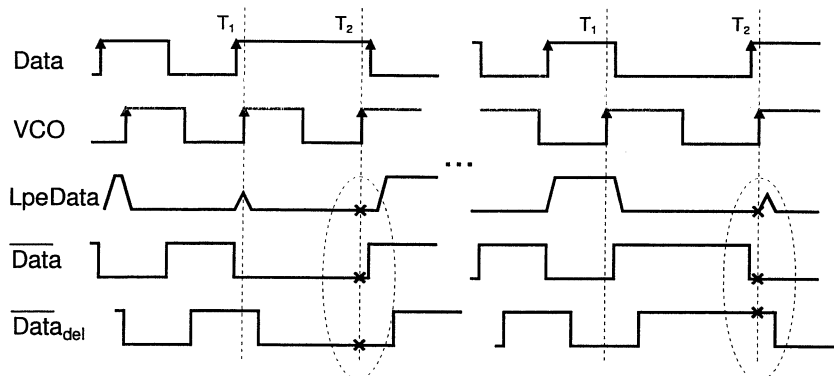


Figure 7.11: Correct Detection of a "frequency-too-high" condition with a delayed version of \overline{Data} .

note that the circuit's ability to compare the timing of the two incoming signals relies on the matching of the two delay paths.

To overcome the need for the signal delays, the self-timed circuit, shown in Figure 7.13 can be used. Here RS-FF 3 is used to discriminate the time differences of the incoming rising edges. To understand the operation of the circuit we refer to Fig. 7.14.

We assume that the rising edge on *Data* comes shortly before the rising edge on *VCO*. At the output of RS-FF 3, $Data'$ will go to zero, which causes RS-FF 4 to set *LpeData* to 1 (and *LpeVCO* to 0). Since *Data* has become 0, RS-FF 2 will toggle its state and *EnData* will go to 0. Now, since the *Data* branch is deactivated, the high level of the *VCO* signal will cause VCO' to become 0, setting *LpeVCO* to 1 (and *LpeData* to 0). Finally, *EnVCO* is deactivated, so both branches are inactive. A zero in the *VCO* and *Data* signals resets RS-FF1 and RS-FF2, putting *EnVCO* and *EnData* in its high state again.

The flip-flops RS-FF 1-3 can be viewed as an impulse separator. The small difference in arrival time of *VCO* and *Data* is translated into reasonably separated, non-overlapping pulses on VCO' and $Data'$. The impulse length is defined by the path delay through RS-

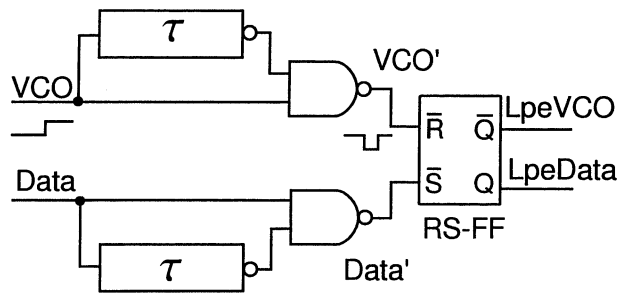


Figure 7.12: Simple last positive edge detection circuit.

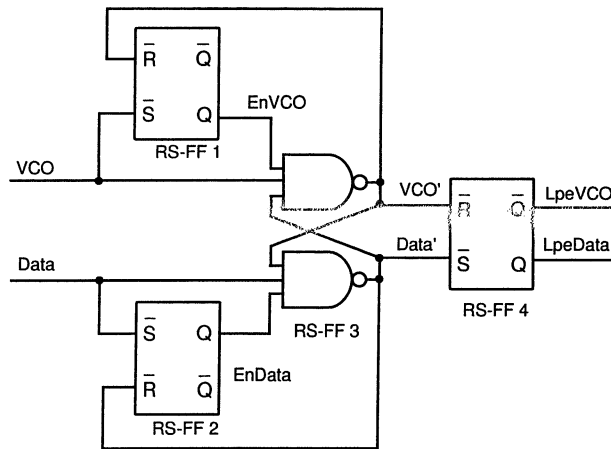


Figure 7.13: Self timed LPE circuit.

FF3 and RS-FF1 (or RS-FF2). These impulses then change the state of RS-FF 4, thereby storing the information which of the signals had the last positive edge.

The self-timed version of the LPE circuit has the advantage that it does not rely on the matching between two signal delays, but is slower and more complex than the simple LPE circuit.

7.2.3 Simulation Results

SPICE simulations made on an extracted layout of the frequency detector circuit are shown in Figure 7.15. The first positive edge on *Data* comes slightly after *VCO*, while the second positive edge on *Data* comes slightly before *VCO*, establishing a "frequency too low" condition. It can be seen that the LPE circuit of Fig. 7.13 effectively resolves the small time differences of the input pulses.

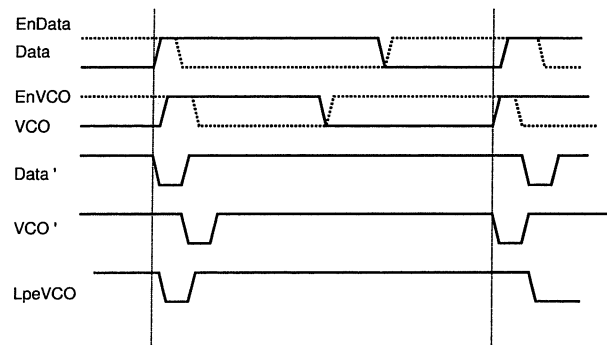


Figure 7.14: Timing diagram of the Self timed LPE circuit.

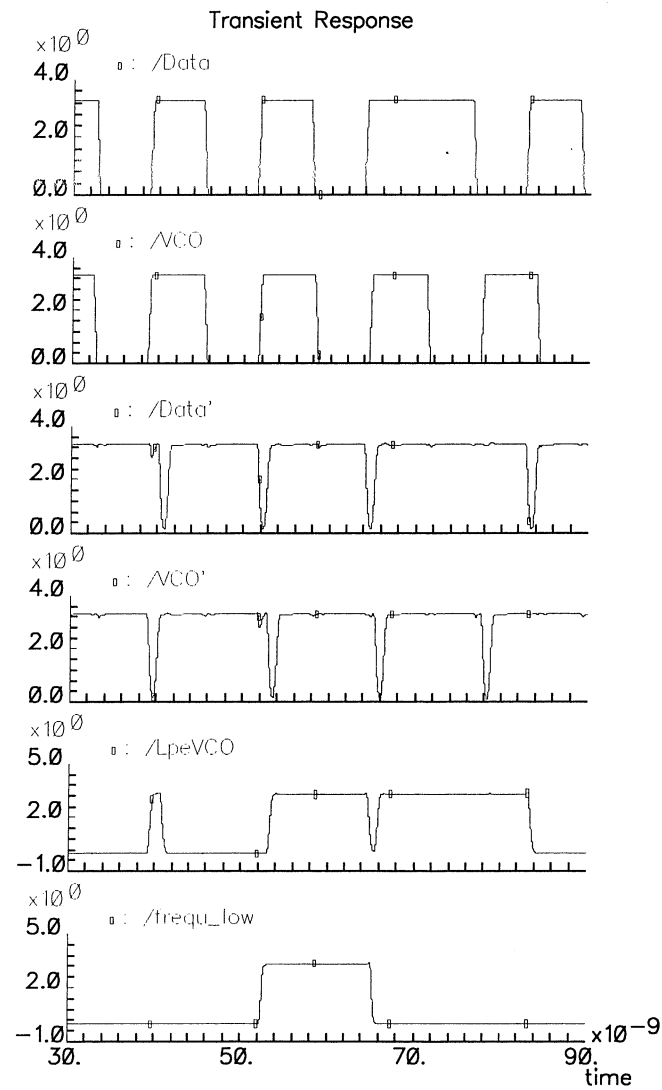


Figure 7.15: SPICE simulation of the frequency detector circuit.

7.3 Application to NRZ Clock Recovery

Frequency acquisition for Nonreturn-to-zero (NRZ) signals is similar to the Biphase case, since also in the NRZ case the VCO clock signal has to be compared against the shortest transition period of the data signal. The VCO frequency will then be half the symbol rate.

In contrast to the rotational frequency detector [MESS-79], the proposed circuit will also make correct decisions at VCO frequencies below 50% of the target frequency down to DC.

An additional advantage is that the circuit does not need a quadrature oscillator input. One major drawback of the proposed circuit, however, is its inability to detect when the VCO frequency is too high. This problem can be overcome by starting the frequency acquisition process with the lowest VCO frequency, letting the frequency detector gradually approach the target frequency.

7.4 Experimental Results

The frequency detector was implemented in the 80 MHz clock and data recovery circuit described in Chapter 8, using a $0.8\mu\text{m}$ CMOS technology. The simple LPE circuit from Fig. 7.12 was chosen to keep the circuit complexity as low as possible. Fig. 7.16 shows the measured frequency acquisition behaviour for the case that the input signal is a Biphase Mark 0-1 idle sequence. It can be seen how the pulses of the frequency detector raise the oscillator frequency, thereby approaching the target frequency of 80 MHz. Fig. 7.17 displays the measured acquisition behaviour for a $2^{12} - 1$ pseudo-random Nonreturn-to-zero (NRZ) input signal. The target frequency of 80 MHz (=half the 160MHz bit rate) is approached in a similar time as in the Biphase case.

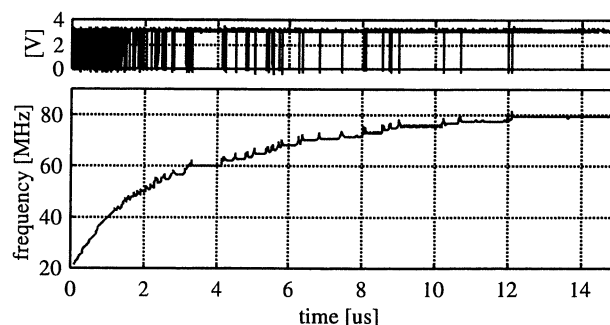


Figure 7.16: Measured frequency acquisition behaviour for a Biphase Mark Inversion signal. The upper part of the graph shows the (negated) frequency_low signal.

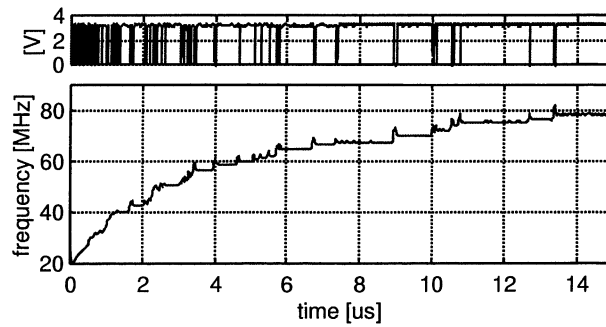


Figure 7.17: Measured frequency acquisition behaviour for a $2^{12} - 1$ pseudo random bit sequence, Nonreturn-to-zero (NRZ) input signal.

7.5 Conclusions

In this Chapter, we presented a novel frequency detector circuit, which overcomes the lower frequency limitation of the Rotational Frequency Detector [MESS-79], and which does not require a quadrature VCO input. The correct function of the circuit with Biphase and NRZ data was proved in a clock and data recovery circuit (See Chapter 8).

Chapter 8

Radiation Hard Clock and Data Recovery Circuit

As described in Chapter 5, a Biphasic Mark encoded 80 MHz bit stream is used in the TTC system to transmit the clock and the other timing signals over an optical fibre network. This chapter describes the integrated circuit, which receives the signal from the fibre and recovers the clock and data from the Biphasic encoded data stream. The circuit contains a Limiting Amplifier, where the signal coming from a pin-photodiode¹ is restored, and a Phase-Locked loop (PLL) to regenerate the clock. In the PLL, we make use of the parameter-tolerant biasing scheme of Chapter 6 and the frequency detector of Chapter 7. We will first outline the overall structure of the circuit, and then discuss those PLL design topics not yet discussed in detail in the previous chapters, such as the novel phase detector and the analysis of the intrinsic oscillator noise.

8.1 Basic Architecture

Figure 8.1 displays the basic architecture of the circuit.² The Biphasic modulated signal, received by the pin-photodiode (plus pre-amplifier), enters a four-stage limiting amplifier. The so-regenerated signal is then converted to a pseudo-differential CMOS signal³, which is fed into a Phase-Locked loop (PLL) to extract the clock. An implementation of the frequency detector circuit proposed in Chapter 7 guarantees that the target frequency of 80 MHz is reached, and a novel phase-detector, which is described below, then directly locks to the Biphasic Mark input signal.

8.2 Limiting Amplifier

Fig. 8.2 displays the structure of the Limiting Amplifier. It consists of four identical gain cells, a differential to CMOS-levels converter, an input biasing circuit, and a current biasing

¹The photoreceptor device also contains an integrated pre-amplifier together with the pin-photodiode.

²The chip layout is shown in Fig. G.3 of page 121.

³I.e. two full-swing CMOS signals of opposite polarity.

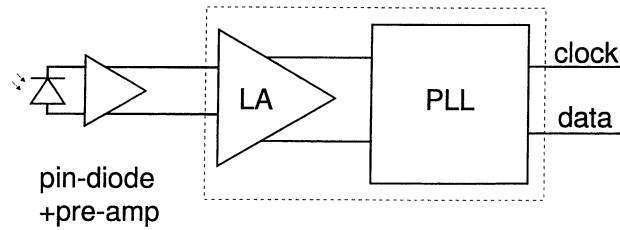


Figure 8.1: Block diagram of the Clock-and Data Recovery circuit. The chip consists of a bipolar Limiting Amplifier (LA) and a Phase-Locked Loop (PLL).

circuit for the gain cells.

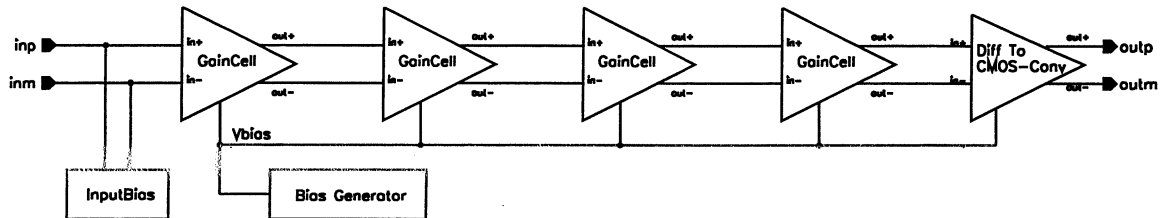


Figure 8.2: Block diagram of the Limiting Amplifier with Bias circuits.

The structure of the gain cells is depicted in Fig. 8.3. Each cell is implemented as an emitter-coupled differential pair of bipolar transistors with resistive loads and a subsequent emitter-follower stage, similar to the structure in [WANG-97]. The emitter-follower stage provides low-impedance outputs and shifts the voltage levels by one V_{BE} . The number of gain stages should be kept low to limit noise and power consumption [JIND-87]. Four was found to be an optimum value to achieve sufficient gain, also when the forward gain β of the bipolar transistors decreases to 25% of its initial value after irradiation.

A biasing circuit defines the current in the gain cells, which is mirrored in the current sources $M1 - M3$ (via the gate-source voltage $bias$ in Fig. 8.3). The current is derived via a resistor matched to the load resistors $R1$ and $R2$ in the gain cells. This effectively avoids that the differential pair transistors $Q1$ and $Q2$ are slowed down by entering saturation.

The differential to CMOS-levels converter is implemented as a symmetrical CMOS OTA [LAKE-94] with a subsequent inverter stage.

8.3 Phase-Locked Loop (PLL)

The design of the PLL [TOIFL-98c], with a block diagram depicted in Fig. 8.4, was governed by the following requirements:

- (a) The VCO frequency should not be influenced by variations of the power supply voltage. Consequently, a differential oscillator structure was preferable. The voltage at the loop filter is directly connected to the oscillator cells, thereby avoiding any conversion circuit and its associated dependence on power supply voltage.

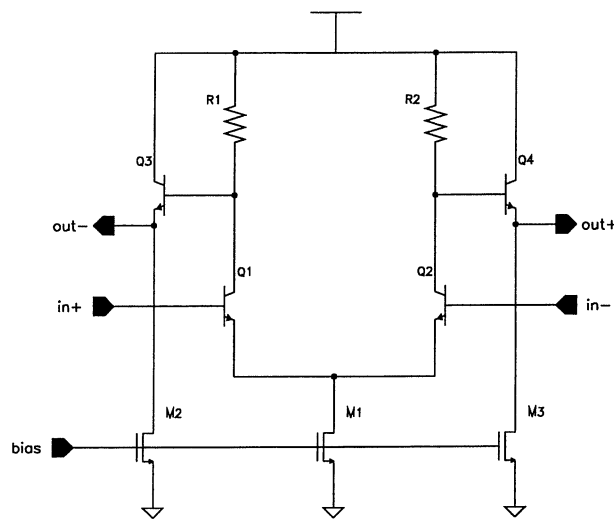


Figure 8.3: Limiting Amplifier Gain Stage.

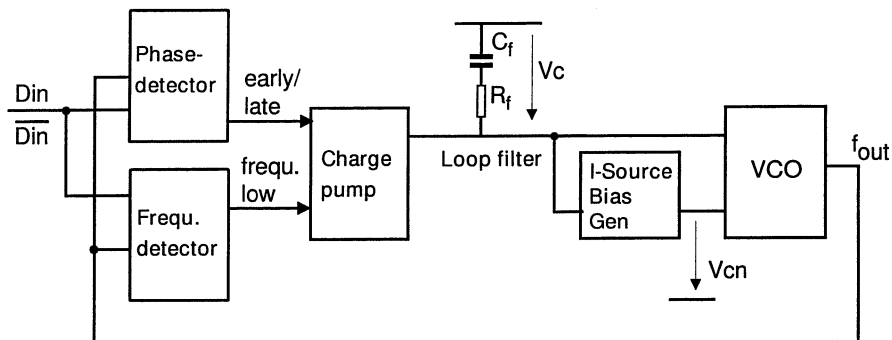


Figure 8.4: Phase-Locked Loop block diagram.

- (b) The phase detector must guarantee safe lock to a random Biphase Mark input sequence. Eventual mismatch in the charge pump, caused by radiation, should not lead to a phase offset. These requirements resulted in the phase detector described below.
- (c) The loop dynamics should not depend on ambient conditions, process parameters, or the effects of irradiation. Hence a PLL biasing scheme as described in Section 6.3.2 was used.
- (d) The thermal noise in the oscillator should be sufficiently small, which requires relatively high currents in the oscillator.

8.3.1 Voltage-Controlled Oscillator (VCO)

The VCO is implemented as a differential ring oscillator. To achieve low power consumption, the number of delay cells should be as low as possible [MCNE-94]. Due to the requirements of the phase detector, described below, four was found to be an optimum value.

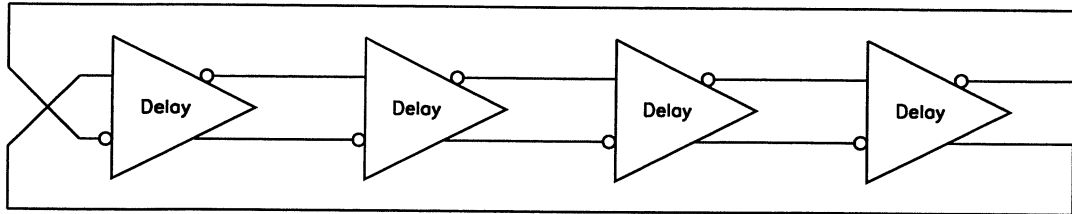


Figure 8.5: Four stage differential ring oscillator.

In order to estimate the jitter caused by the intrinsic noise in the VCO, we developed a procedure which is outlined in Appendix D. It is based on the cyclo-stationary model introduced by [HAJI-98a] and takes the time dependence of the noise sensitivity and the noise sources into account. Instead of calculating phase noise in the frequency domain, we directly derive expressions for jitter in the time domain. The analysis is performed for thermal and $1/f$ -noise. The resulting value could then be included in a behavioural model to simulate the PLL using Verilog [VERI-91].

Using the actual device parameters, the predicted standard variation of the cycle jitter caused by thermal noise resulted in a value of 2.1ps. Interestingly, the main contribution was found to come from the current source transistor in the differential pair.

Unlike the case of thermal noise, it is not possible to calculate a value for cycle jitter for $1/f$ -noise, since it is theoretically infinite. But as $1/f$ -noise only causes a slow variations of the cycle time, the loop can easily correct for the changes. As shown in Appendix D, it is however possible to calculate the variance of *cycle-to-cycle* jitter caused by $1/f$ -noise. It is shown that the contribution of $1/f$ -noise to jitter is negligible compared to the contribution from thermal noise.

8.3.2 Phase Detector

The phase detector was carefully designed to guarantee the acquisition of lock in two important cases: On the one hand, for a random binary data stream (a), and, on the other hand, for the periodic 0-1-0-1.. idle sequence (b) at the input of the circuit. In order to study the phase acquisition process, the overall PLL was simulated at a behavioural level using Verilog. An important result of the simulations was that the regularity of the Biphasic code can cause various pathological cases of a false lock. Figure 8.6 shows the desired state of phase-lock (a), the case of a false lock to the middle transition (b), which is likely to happen when there are long strings of ones in the data stream, and the case of locking to a rational multiple of the symbol frequency (c).

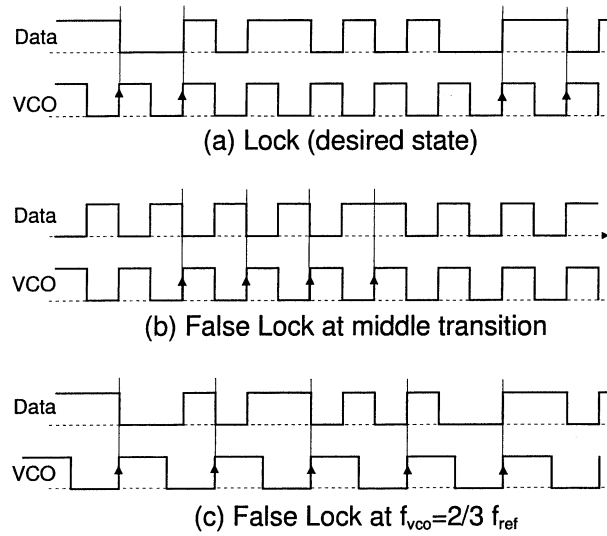


Figure 8.6: The desired state of phase lock (a), and the pathological cases of locking to a middle transition (b), and locking to $2/3 f_{ref}$ (c).

Basic Functionality

The phase detector is a modification of the sample phase detector from Alexander[ALEX-75]. Its basic operation is to sample the incoming data signal with the clock signal generated in the VCO. The outcome of the phase detector circuit is a binary value, either *early* or *late*. Although this would, in principle, require only a single flip-flop, the actual phase detector implementation has to be more complex. As shown in Figure 8.7, the signal is sampled at five time positions, corresponding to the rising edges of five clock phases $\Phi_0 - \Phi_4$, equidistantly spaced with an angle of 45° . The resulting sample values are $S_0 - S_4$. The reasons for the increased complexity are the following:

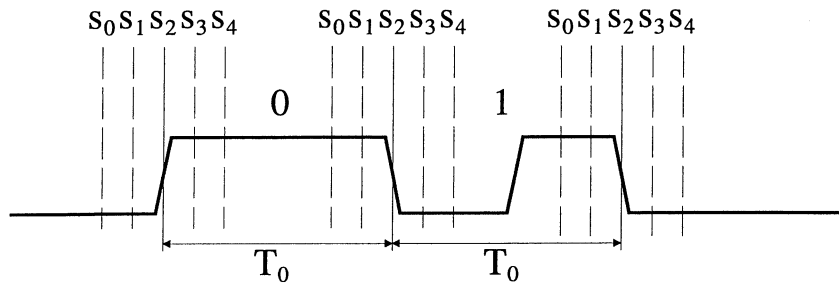


Figure 8.7: Sample instances of the phase detector. Sampling the signal with clock phases $\Phi_0 - \Phi_4$ results in sample values $S_0 - S_4$.

First, since the edges of the Biphase Mark code used as a reference can either be falling or rising, the *early/late* decision has to be based on two samples, one reference sample S_0

and one master transition sample S_2 .

Secondly, to assure a fast and safe acquisition of lock, the phase detector was extended with a state machine, acting on the outcome of the sample values. Samples S_1 and S_3 are used to define a *small gate* around the master transition edge Φ_2 . Whenever $S_1 \neq S_3$, there must be a transition of the input signal within the gate. The state machine will only start the lock-in process when there is a transition of the input signal within this gate. The samples S_0 and S_4 define a *large gate*. The purpose of the large gate is to detect when the loop has lost lock.

Thirdly, the samples S_0 and S'_4 (which is S_4 from the previous cycle) are used to recover the data information from the incoming Biphase encoded stream. Since the data edge indicating a one occurs at a phase angle of 180 degrees, the optimum sampling instants are at phase angles of 90° and 270° , which corresponds to the clock phases Φ_4 and Φ_0 . In the case of a Biphase Mark zero there is no middle transition, so S'_4 equals S_0 , in the case of a Biphase Mark one they are different. Hence, the data information can be extracted using an Exclusive OR-gate.

Early/Late Signal Generation

A simplified schematic of the phase detector frontend section is shown in Figure 8.8. The logic elements are differential latches and Exclusive-OR gates. The latches marked with an arrow pointing upward are transparent when the clock is high. Two opposite latches comprise a master-slave flip-flop. The (differential) input signal din/\overline{din} is sampled at the rising edges of Φ_0 and Φ_2 , resulting in sample values S_0 and S_2 . In order to avoid a glitch on the *early/late* signal at the output of the XOR gate, S_0 is re-timed by a latch becoming transparent with the rising edge of Φ_2 . Hence, both inputs to the XOR gate, S_0 and S_2 , change at the same time.

Data Generation

In order to recover the data, the Biphase Mark input signal is sampled at two positions, Φ_4 and Φ_0 . At the rising edge of Φ_0 , the output of the flip-flop clocked by Φ_4 still contains the sampled value S'_4 from the last cycle. This value is then XORed with L_0 , which is the input signal latched at Φ_0 . The result is sampled by another flip-flop at the rising edge of Φ_2 . The reason for using the latched value L_0 and not the sampled value S_0 is to gain speed by avoiding the additional signal delay in the second latch.

Lock-In State Machine

The state machine takes the signals from the phase detector frontend and controls the lock-in process by enabling and disabling the charge pump.

The state transition graph is shown in Figure 8.9. After a reset, the frequency detector forces the VCO frequency close to the reference frequency of the Biphase signal. The frequency detector is then deactivated, and the phase detector turned on. The state machine is initially in the "Unlocked" state. In this case, the charge pump is switched off. The *early/late* signal is ignored, and the VCO frequency stays constant. Since the frequency will

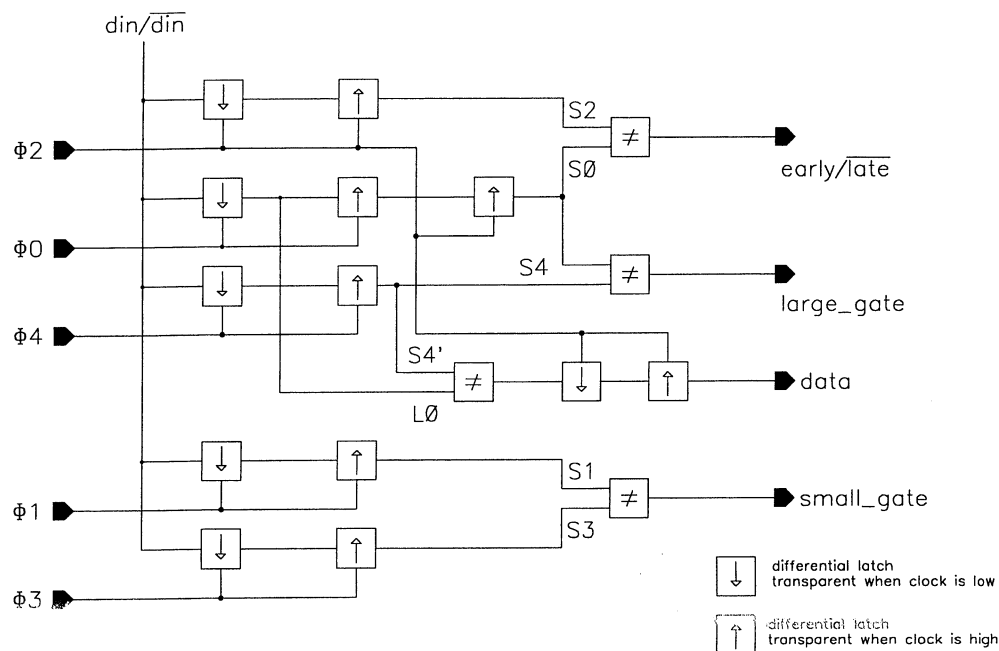


Figure 8.8: Block Diagram of the Phase-Detector Frontend.

never be exactly the reference frequency, the phase difference between the VCO signal and the reference signal will change from cycle to cycle by a rate proportional to the difference in frequency, thereby producing cycle slips. Upon the detection of a cycle slip the state changes to "Pre-locked", and the charge pump is turned on, which starts the lock-in process. The detection of a cycle slip is accomplished by detecting that

- (a) the $early/\overline{late}$ signal changes its value
- (b) there was an edge within the small gate

In this case, the phasor of the VCO signal has crossed the phasor of the reference signal: if the decision was *early* in the previous cycle(s), and then changes to *late*, the VCO frequency is lower than the reference symbol rate, and vice versa.

Hence, after a change of its value, the $early/\overline{late}$ -signal indicates the direction of the cycle slip, corresponding to the sign of the frequency difference.

The charge pump can now be safely turned on, and the VCO frequency controlled by the $early/\overline{late}$ signal. If the frequency difference was small enough, the VCO frequency reaches the reference frequency before the accumulated phase difference makes the reference signal edge leave the small gate. The phasor of the VCO signal would change direction and cross the reference phasor from the other side, again changing the decision of the $early/\overline{late}$ signal.

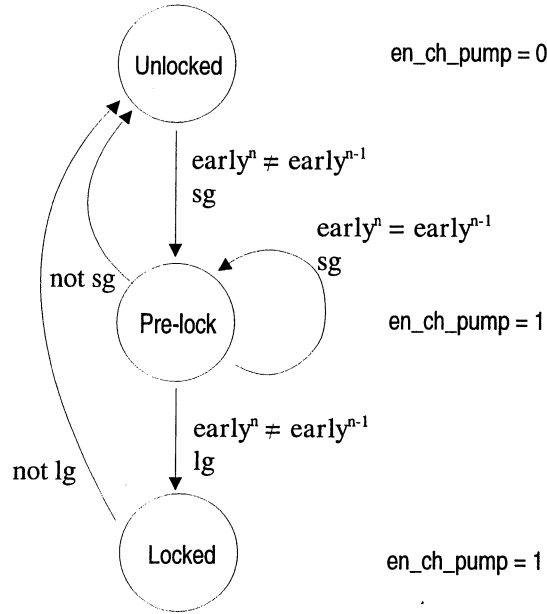


Figure 8.9: State transition graph for the lock-in state machine. The signals *early*, *sg* ("small gate") and *lg* ("large gate") from the phase-detector frontend are inputs to the state machine. The output signal *en_ch_pump* controls the operation of the charge pump.

This happened, the state changes to "Locked", where the charge pump stays activated. The frequency finally stabilises and phase lock is achieved.

If the phasor leaves the small gate before the reference frequency is reached, however, the state goes back to "Unlocked", and the state machine waits for the next cycle slip. Although the lock attempt failed, the VCO frequency was at least moved in the right direction, allowing lock in one of the next attempts. Once the state machine is in the "Locked"-state, the large gate is used to detect if for some reason the loop has lost lock. If there is no transition detected within the large gate, the state then goes back to "Unlocked".

Frequency Range

The frequency range for which lock acquisition can be guaranteed is defined by the width of the small gate. In the following analysis, we will derive the upper and lower bound of the frequency range. We assume that the clock phases coming out the ring oscillator are equidistantly spaced by tapping the signals from consecutive stages of the VCO. Let t_w denote the half-width of the small gate, which corresponds to the time delay between two consecutive clocks and is defined as a fraction of the VCO period t_{vco}

$$t_w = \frac{t_{vco}}{n}, \quad (8.1)$$

where n equals two times the number of buffer stages in the oscillator. Figure 8.10 displays the situation to derive first order bounds on the minimum and maximum frequency. As

described above, the incoming data signal is sampled with three consecutive clock phases Φ_1 , Φ_2 and Φ_3 , leading to sample values S_1 , S_2 and S_3 . To start the lock-in procedure a cycle slip must be detected inside the small gate. The maximum VCO cycle time $t_{vco,max} = 1/f_{min}$ is found for the case that two consecutive transitions of the Biphasic signal just fall in two consecutive small gates

$$t_{vco,max} - 2t_w = T_0, \quad (8.2)$$

where T_0 denotes the cycle time of the Biphasic signal. Substituting (8.1) into (8.2) results in

$$t_{vco,max} = \frac{n}{n-2}T_0, \quad (8.3)$$

or, equivalently,

$$f_{min} = \left(1 - \frac{2}{n}\right) \cdot f_0, \quad (8.4)$$

with $f_0 = 1/T_0$. The maximum frequency is similarly given by

$$f_{max} = \left(1 + \frac{2}{n}\right) \cdot f_0. \quad (8.5)$$

Another constraint on the frequency bounds is due to the nature of the Biphasic Mark encoding. The distance between two edges can either be $T_0/2$, T_0 or $3T_0/2$. To avoid a lock attempt to either $2f_0$ or $2/3f_0$, the frequency bounds f'_{max} and f'_{min} can be defined according to Figure 8.11:

$$f'_{min} = \frac{2}{3}\left(1 + \frac{2}{n}\right) \cdot f_0, \quad (8.6)$$

$$f'_{max} = \left(2 - \frac{4}{n}\right) \cdot f_0. \quad (8.7)$$

The third bound on the frequency range stems from timing constraints in the state machine and in the charge pump. Considering the overall signal delay after the decision to start a lock-in procedure, the charge-pump is switched on with nearly one cycle delay in the worst-speed case. Similarly, it is switched off with one cycle delay. If the frequency difference is too high, the *early/late* signal would only be correct during one period. In this case, the right value of the *early/late* signal would not reach the charge pump, while in the consecutive cycle, a wrong value would direct the VCO frequency in the wrong direction. Hence:

It must be assured that, once the lock-in procedure is started, there are at least two consecutive correct *early/late*-decisions.

It is to note that the *early* signal is generated by XORing S_0 and S_2 with a separation in time of $2t_w$. The frequency bounds resulting from these situations, depicted in Figures 8.12 and 8.13, are then given by

$$f''_{min} = \left(1 - \frac{3}{2n}\right) \cdot f_0, \quad (8.8)$$

$$f''_{max} = \frac{2}{3} \left(2 - \frac{1}{n}\right) \cdot f_0. \quad (8.9)$$

Figure 8.14 combines (8.4)-(8.9) in a graph displaying all the lower and upper bounds on the frequency range as a function of n . It can be seen that n must be greater than 4 in order to guarantee proper lock-in, and for $n = 8$ the opening of the eye is maximised. Fortunately, the case of $n = 8$ corresponds to a spacing in phase of 45° , which is the case in the actual implementation.

Width of Large Gate

The width of the large gate is governed by the need to assure stability. In the case of a step change in power supply, the VCO frequency will also change slightly, causing the phase of the VCO signal to run away from the reference phase. Due to the correction movement of the loop, the frequency difference will eventually be equalised. It must be assured, however, that during the correction process the phase difference between the VCO and the reference signal never exceeds the half-width of the large gate. In this case, the loop would lose lock, and the state-machine would be reset to the "Unlocked"-state. It is shown in Appendix E, that the maximum static deviation in loop cycle time which would not lead to a loss of lock t_{max} is given by

$$\Delta t_{max} = \Delta t_p + \sqrt{2\Delta t_i \cdot t_{wl}}, \quad (8.10)$$

where Δt_p , Δt_i [s] denote the proportional and integral part of the loop response, and t_{wl} [s] denotes the half-width of the large gate.

Since Δt_p and Δt_i should be made as small as possible to achieve low jitter, the width of the large gate should be maximised together with the power supply rejection of the VCO.

With the width of the large gate fixed, the achievable jitter is related to the static power supply rejection of the VCO. The less the VCO frequency is expected to deviate, the smaller values for Δt_i and Δt_p can be chosen.

In the actual implementation t_w amounts to $3.125ns$ in the locked case. Using the nominal values of $\Delta t_p = 10ps$ and $\Delta t_i = 1ps$ results in a maximum acceptable deviation in cycle time of $t_{max} = 84.1ps$, which is within the limits of a change in cycle time resulting from a step in power supply of 1V.

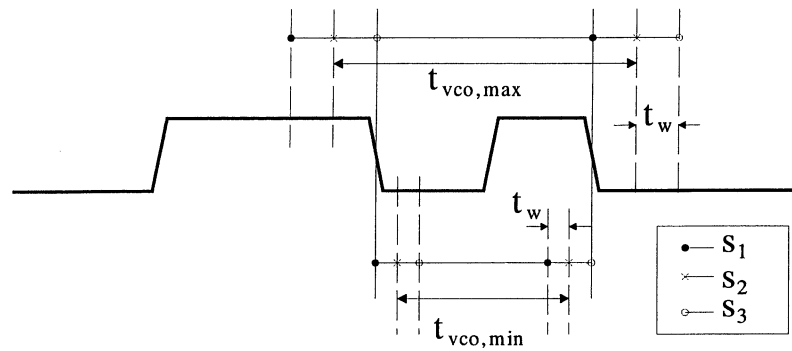


Figure 8.10: Minimum and maximum oscillator period leading to a safe detection of a cycle slip. The three samples defining the window are t_w apart.

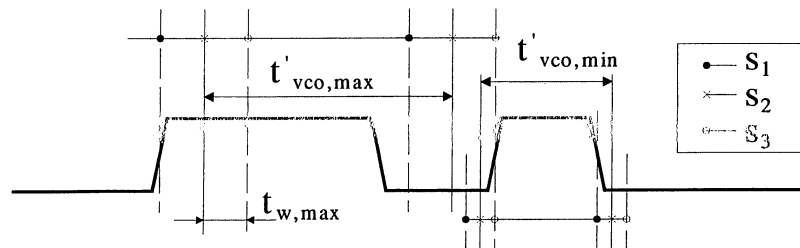


Figure 8.11: Maximum oscillator period to avoid a lock-in procedure at $2/3f_0$ and $2f_0$.

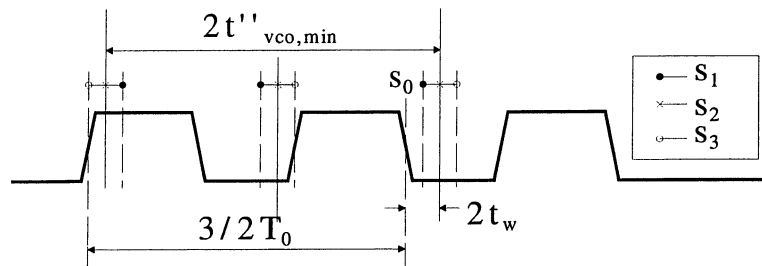


Figure 8.12: Minimum oscillator period to assure at least two correct decisions of the phase detector.

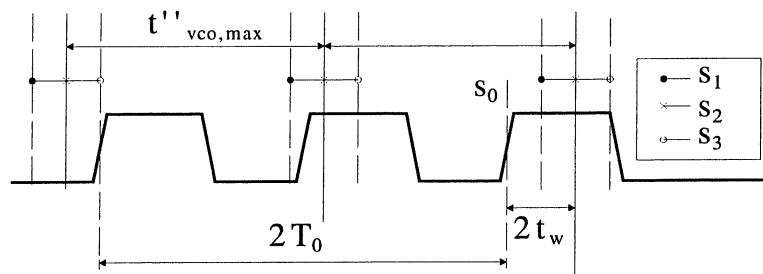


Figure 8.13: Maximum oscillator period to assure at least two correct decisions of the phase detector.

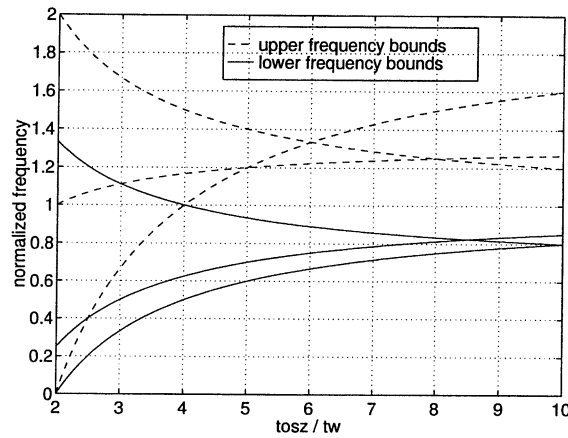


Figure 8.14: Bounds on the minimum and maximum VCO frequency as a function of the width of the small gate.

Lock to Middle Transition

In the case that there is a long string of Biphase Mark ones, there is the possibility of an erroneous lock to the middle transition, as being depicted in Figure 8.6 (b). At the first occurrence of a zero, however, the loop would fall out of lock, because there would be no transition within the large gate. The state machine is thereby reset to the "Unlocked" state, which assures that a subsequent one does not lead to a further lock to the middle transition. The phase then slowly drifts away, and the next detected cycle slip occurs at the correct edge.

8.3.3 Replica Current Biasing Circuit

In order to regulate the voltage swing of the oscillator, we make use of the replica current biasing circuit [MANE-96] shown in Fig. 8.15. It consists of a half-buffer replica cell (M5-M8) and a differential amplifier (M0-M4). The maximum voltage swing ΔV in the oscillator cells appears when all the current is directed into one branch. This is the case which is simulated in the replica cell, with V_s corresponding to the maximum voltage swing. The control voltage of the NMOS current source in the differential oscillator stages V_n is regulated by the differential amplifier.

Control Loop Transfer function

As seen in Fig. 8.15, the current source of the differential amplifier is controlled by the VCO control voltage V_c . Hence, the poles and zeroes of the system change with the operating frequency of the oscillator. Also the poles of the feedback path in the replica cell, of course, change with V_c . The transfer function of the closed loop $H(s) = V_s(s)/V_c(s)$ is derived in Appendix F. It is shown that due to the variable biasing of the amplifier, the relevant poles in both the amplifier and the feedback path all shift according to \sqrt{I} . Hence, the

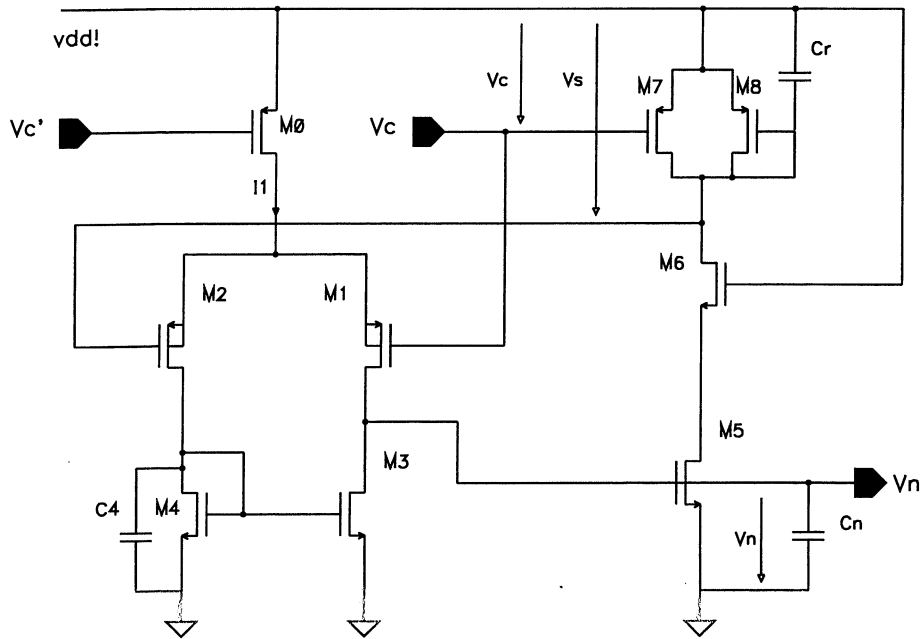


Figure 8.15: Replica current biasing circuit with differential amplifier to regulate the voltage swing.

dependence on I cancels out, and the loop damping factor ζ stays constant.

8.4 Measurement results

Power Supply Rejection

For a supply voltage of 3.3 V, the oscillator frequency was measured to have a sensitivity by 0.6 % /V supply voltage variation.

Cycle Jitter

The cycle jitter of the free-running VCO was measured by using a method described in [MCNE-94] and resulted in a value of 1.9 ps/cycle for the 80 MHz oscillator frequency, which is very close to the predicted value of 2.1 ps/cycle derived in Appendix D.

Long-term Jitter

The histogram of the long-term jitter⁴ for the case of a constant sequence of ones is shown in Fig. 8.16. The rms value amounts to only 18 ps, (peak-to-peak 120 ps). After irradiation, however, this value degrades to 33ps rms. The difference to the value before irradiation

⁴Long-term jitter is measured by triggering on an external clock reference.

stems from radiation-induced mismatch in the charge pump currents⁵. For the case of a $2^9 - 1$ pseudo-random noise sequence at its input, the jitter before irradiation amounted to 53 ps rms (peak-to-peak 369 ps), which slightly degraded to 58 ps (peak-to-peak 404 ps) after 10 Mrad (Fig. 8.17). A curve proving that jitter does only little depend on temperature was already shown in Fig. 6.11 on page 46.

The long-term jitter of the whole circuit (PLL plus Limiting Amplifier) is shown in Fig. 8.18 as a function of optical input power. The input signal was an alternating sequence of zeroes and ones. As shown in the figure, for a minimum input power of -27 dBm, the rms jitter value stays below 50 ps, even after the 10 Mrad irradiation.

The measured clock jitter for -20dBm input power, a $2^{12} - 1$ pseudo-random sequence in channel B and a simulated trigger signal in channel A with a frequency of 100 kHz amounted to a value of 64.5 ps rms (peak-to-peak 378 ps) before irradiation, and 68.8 ps rms (peak-to-peak 433 ps) after irradiation.

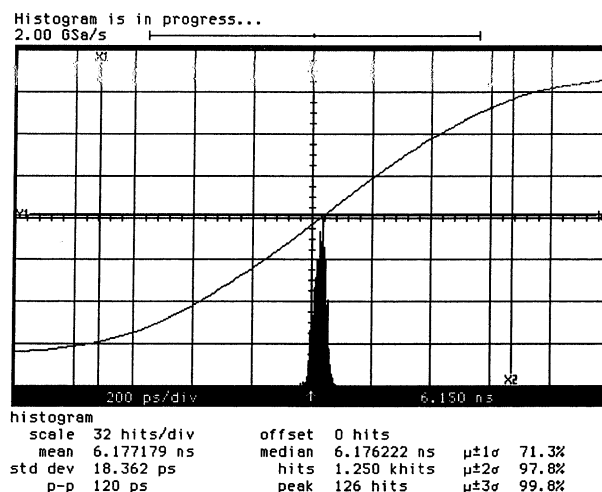
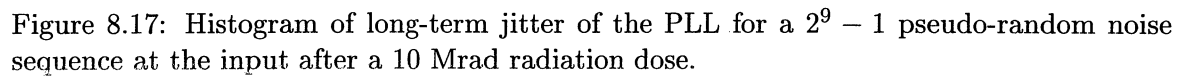


Figure 8.16: Histogram of long-term jitter of the PLL for a constant sequence of ones at the input before irradiation.

Power Consumption

At a supply voltage of 3.3V, the circuit consumed a total power of 47 mW, of which 17 mW is used in the Limiting Amplifier, and 30 mW in the PLL. After irradiation, the overall power consumption was measured to be 45mW, hence staying approximately constant.

⁵Since the charge pump currents have to be very small ($< 1\mu A$), every V_t mismatch leads to a considerable mismatch of the currents charging up or down. It was found that after irradiation the down current (in the NMOS transistors) was about twice the up current (PMOS transistors).



In this chapter, we presented the design of a radiation-hard clock and data recovery circuit based on a phase-locked loop. The circuit extracts a low-jitter clock from the Biphase Mark input sequence. Although the jitter slightly increases after irradiation due to a radiation-induced mismatch in the charge-pump, it still stays considerably low even after 10 Mrad of gamma-irradiation. The prototype circuit also proves the correct function of the novel frequency detector, phase detector and the parameter-independent biasing scheme.

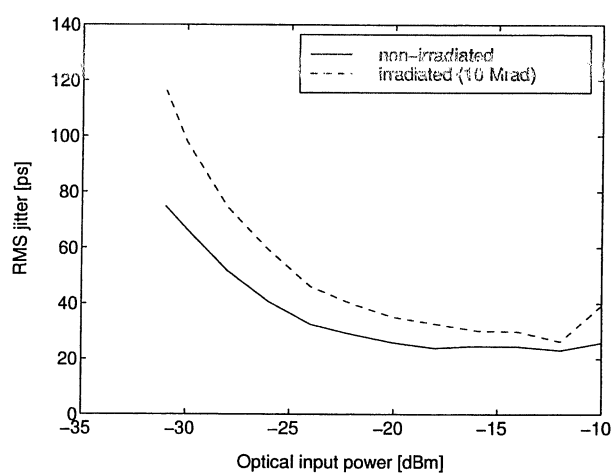


Figure 8.18: Long term jitter as a function of optical input power.

Chapter 9

Timing, Trigger and Control Receiver ASIC

9.1 Function and Architecture

The Timing, Trigger and Control Receiver (TTCrx) ASIC is a complex analog-digital chip, which generates all the required signals for the synchronisation of the connected detector electronics. A block diagram of the circuit is shown in Fig. 9.1. It performs the following functions: First, it recovers a low-jitter clock from a Biphasic Mark encoded signal at its input. It then provides two de-skewed clock signals, which can be independently phase-shifted in steps of 104ps. Secondly, it receives the level 1 trigger signal, and makes it available at its output with low latency. Thirdly, it receives the other synchronisation signals, i.e. the bunch counter reset strobe and the event counter reset strobe. All synchronisation signals can be delayed by a programmable value, up to a maximum delay of 400ns. Fourthly, the chip provides the functionality for transmitting arbitrary data to the connected components, using one of two data formats.

After clock and data recovery, the 80 Mbit/s input data stream is separated into two 40 Mbit/s channels, denoted A and B. While channel A is reserved for transmitting solely the level 1 trigger decision, channel B is used to transmit other synchronisation signals together with arbitrary data, which are made accessible to connected components through a parallel port.

Data Formats

Two data formats are supported, which are outlined in Fig. 9.2. The shorter one, referred to as "broadcast command" format, has a net data length of 8 bit, the longer "individually-addressed command" format has a net data length of 16 bit. The idle symbol in the B channel is 1, hence a zero is used as a start bit in both formats. The following bit (marked FMT) specifies the format type (0 for short, 1 for long) of the packet. The 8 or 16 bit long data word is then followed by a check sum, used for hamming error detection/correction. Data sent in the "Broadcast" format is received by all TTCrx chips in a system. In contrary,

the long or "Individually Addressed" format contains a 14 bit device address, thus allowing to access specific chips in a system. Address 0 serves as a generic address, so data sent to this address is received by all chips in the system. An additional bit in the individually-addressed command frame (E) specifies if the data word is sent to the external port (E=1), or if the command is to be interpreted internally in the TTCrx.

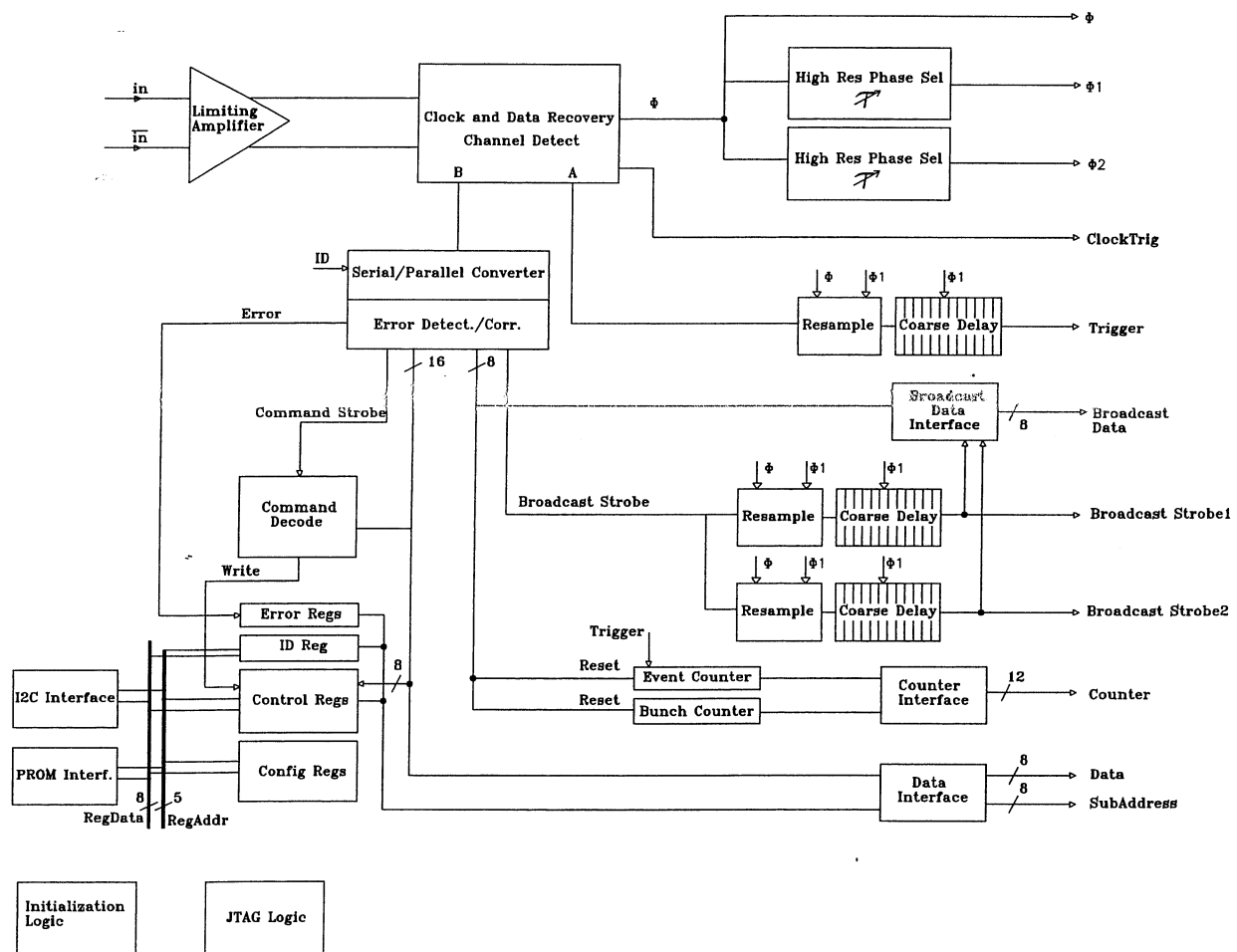


Figure 9.1: Timing, Trigger and Control Receiver block diagram.

On-Chip Counters

Two counters are implemented on the chip, which are crucial for detector synchronisation

- (a) **Bunch counter.** This counter is 12 bits wide and is incremented with every cycle of the 40 MHz clock. The counter is reset upon the reception of a "Bunch Counter Reset" command, which is usually received every 3564 bunch crossings, corresponding to a full revolution of the particles in the accelerator tunnel. The content of the bunch counter is used to label and identify data from the frontend electronics.

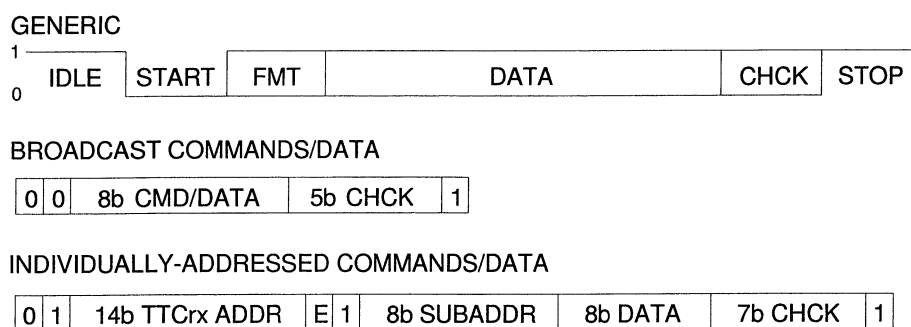


Figure 9.2: Data formats: Generic structure (top), broadcast commands (middle) and individually-addressed commands (bottom).

- (b) **Event counter.** This counter is 24 bit wide and is increased upon the reception of a level 1 trigger signal. It is reset upon the reception of an "Event Counter Reset" command.

The chip also incorporates a hamming error-detection/correction logic. The number of errors are logged in two error counters: One contains the number of single-bit errors, which can be corrected by the chip, the other keeps track of the number of unrecoverable transmission errors.

Interfaces

Apart from the optical link, the chip is also able to communicate via an I2C-Interface [SIGN-92], which allows to read and write the internal registers of the TTCrx. Optionally, an external serial PROM can be used to supply initial register values after a reset. A JTAG interface [JTAG-90] was added for testing purposes.

Generated Signals

The following signals are generated by the circuit

- (a) 40 MHz **clock signal** clk_0
- (b) Two **phase-shifted (de-skewed) clock signals** clk_1 and clk_2 . The phase shift with respect to clk_0 can be programmed individually with a resolution of 104ps.
- (c) **Level 1 Trigger:** The trigger signal corresponds to the bit stream in channel A. The signal is synchronised with clk_1 , consequently, it can be delayed with a resolution of 104ps. An additional coarse delay pipeline provides an overall delay range of 400ns.
- (d) **Combined clock and trigger signal.** This signal is equivalent to clk_0 , with the difference, that, upon reception of a trigger, one clock impulse is blanked out.
- (e) **Serial Data signal**, corresponding to the raw bit stream in Channel B.

- (f) **Broadcast command bus.** An 8-bit parallel output bus, used to transfer data in the broadcast format. Two different broadcast command strobes signal the arrival of new data. Both strobe signals can be individually delayed in digital pipelines for a total of 16 cycles (=400 ns).
- (g) The **Individually-addressed command bus** is divided into an 8 bit "Sub-address"-bus and an 8 bit "Data" bus.
- (h) **Bunch Counter and Event Counter.** Both counters are multiplexed on a 12 bit parallel bus.
- (i) **Two error strobe signals.** One signals the occurrence of a single bit transmission error, which can be corrected due to the hamming encoding, the other indicates the appearance of a fatal error, i.e. more than one bit in error.
- (j) **Error counters:** upon the reception of an "Error Counter Dump" command, the content of the error counters appears on the Data bus.

9.2 Clock and Data Recovery

The core of the clock and data recovery circuit is composed of a Limiting Amplifier and a Phase Locked Loop (PLL), which were already presented in detail in Chapter 8. The 80 MHz clock, originating in the PLL, is divided by two in order to derive the 40 MHz LHC clock. As channels A and B are time division multiplexed, there is a fundamental ambiguity for the clock phase: it can be aligned to either channel A or B. This ambiguity is solved by identifying the channels through a property of the trigger data in channel A: by definition, there can never be more than 11 consecutive ones transmitted. A channel-check circuit therefore counts the number of consecutive ones in channel A. If the number exceeds eleven, the phase of the 40 MHz clock is inverted, and the assignment of channel A and B is swapped.

9.3 High Resolution Clock Phase Shifter

The high-resolution clock phase shifter is based on the vernier principle [CHRI-95a]. It consists of two cascaded delay generation blocks, each implemented as a Delay Locked Loop (DLL) combined with a multiplexer. The first DLL has a delay line of length 16, thereby dividing the full clock cycle into 16 equidistantly spaced time intervals, whereas the second DLL divides the clock cycle by 15. The overall delay is thus given by

$$\tau_x = \frac{m}{16} \cdot T + \frac{n}{15} \cdot T, \quad (9.1)$$

with m, n being the values at the selection input of the multiplexers, and T the 25ns clock cycle time. Taking into account the periodicity of the clock signal results in an overall delay

$$\tau_x = \frac{[(m+n) \cdot 15 + n] \bmod 240}{240} \cdot T, \quad (9.2)$$

which is graphically shown in Fig. 9.4. The 25ns cycle time is thus divided into 240 equidistant steps of 104 ps. To get an estimate of the expected nonlinearity, we can calculate its variance depending on the delay tap numbers n, m . Using the results from Appendix A, the maximum variance of the integral nonlinearity is expected when both DLLs are tapped in (or near) the middle ($m=8, n=7$) position. Assuming the variance of the single cell delay in the two DLLs to be equal and given by $\sigma_1^2 = \sigma^2(\Delta T/T)$, the resulting maximum variance¹ is then given by

$$\sigma_{max}^2 = \frac{7 \cdot 8}{15} \sigma_1^2 + \frac{8 \cdot 8}{16} \sigma_1^2 \approx 7.7 \sigma_1^2 \quad (9.3)$$

The design goal is a σ_{max} of half the timing resolution

$$\sigma_{max} = \frac{1}{2} \cdot \frac{104ps}{25000/16ps}, \quad (9.4)$$

$$\sigma_1 = \sigma_{max} / \sqrt{7.7} = 1.26\% \quad (9.5)$$

Hence, for every process corner the standard deviation of the delay in a single delay cell should not exceed 1.26%.

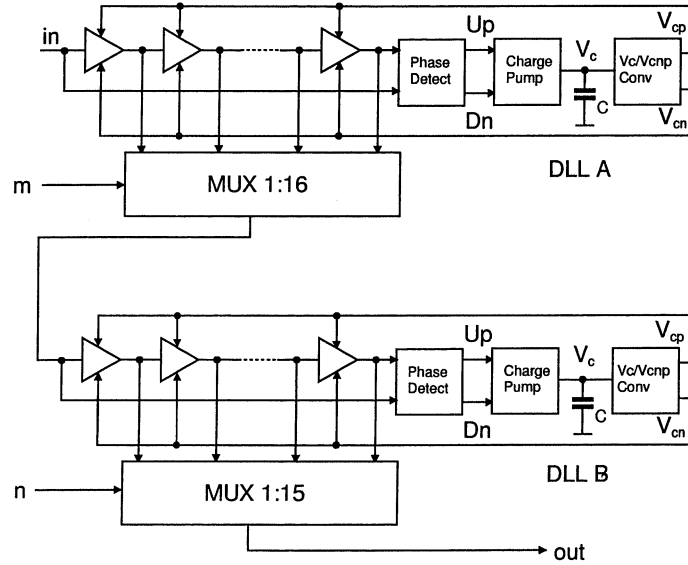


Figure 9.3: Vernier clock phase shifter block diagram.

9.4 Data Re-sampling

Three signals need to be aligned with the skewed clock: the trigger signal, and the two broadcast command strobes. Originally, those signals are aligned with clk_0 , hence they

¹The contribution of the mismatch in the two multiplexers is neglected in first order.

	$(m+n) \bmod 16$															
n	0	15	30	45	60	75	90	105	120	135	150	165	180	195	210	225
	1	16	31	46	61	76	91	106	121	136	151	166	181	196	211	226
	2	17	32	47	62	77	92	107	122	137	152	167	182	197	212	227
	3	18	33	48	63	78	93	108	123	138	153	168	183	198	213	228
	4	19	34	49	64	79	94	109	124	139	154	169	184	199	214	229
	5	20	35	50	65	80	95	110	125	140	155	170	185	200	215	230
	6	21	36	51	66	81	96	111	126	141	156	171	186	201	216	231
	7	22	37	52	67	82	97	112	127	142	157	172	187	202	217	232
	8	23	38	53	68	83	98	113	128	143	158	173	188	203	218	233
	9	24	39	54	69	84	99	114	129	144	159	174	189	204	219	234
	10	25	40	55	70	85	100	115	130	145	160	175	190	205	220	235
	11	26	41	56	71	86	101	116	131	146	161	176	191	206	221	236
	12	27	42	57	72	87	102	117	132	147	162	177	192	207	222	237
	13	28	43	58	73	88	103	118	133	148	163	178	193	208	223	238
	14	29	44	59	74	89	104	119	134	149	164	179	194	209	224	239

Figure 9.4: Correspondence between the programmed delay value (in units of 104ps) and the multiplexer selection values m and n .

must be re-sampled. Since the clock skewing range extends over a full period of the clock cycle, simply sampling the data with clk_1 would, for a certain range of the introduced delay, lead to erroneous results. To solve the problem the data is latched in the middle of the clock cycle. Depending on the value of the programmed delay, the sample is then taken either from the original signal or from the latched value. Fig. 9.5 schematically displays the situation:

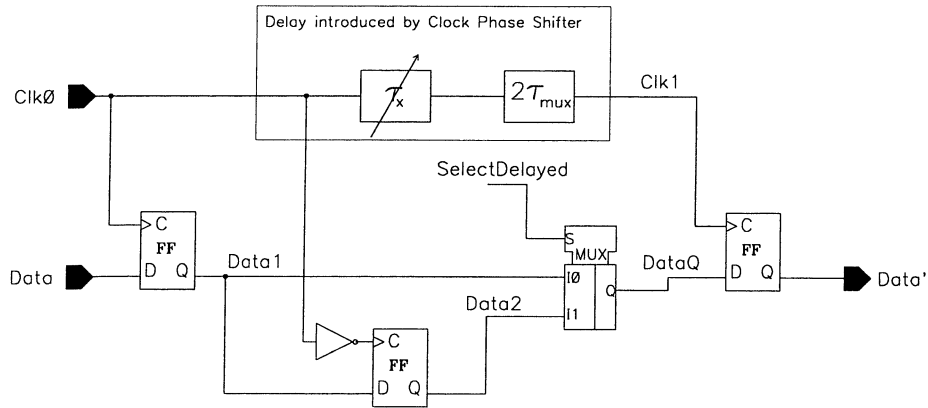


Figure 9.5: Data re-sampling unit.

The original clock (clk_0) is delayed in the vernier delay generation stage to generate clk_1 . The overall delay Δt_{clk} from clk_0 to clk_1 is given by

$$\Delta t_{clk} = \tau_x + 2\tau_{mux}, \quad (9.6)$$

where τ_x denotes the programmed delay, which is known, and τ_{mux} is the (unknown) delay of the multiplexer connected to each of the two DLLs. This multiplexer delay can deviate by a large amount due to variations in process, temperature and supply voltage. *Data1* is the signal aligned with clk_0 , from which *Data2* is latched in the middle of the clock cycle. *SelectDelayed* specifies which of the signals (*Data1* or *Data2*) is sampled.

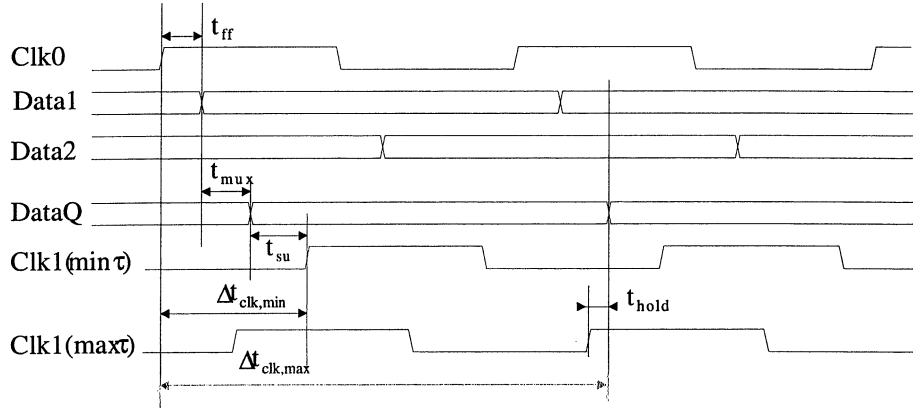


Figure 9.6: Data re-sampling time diagram.

To establish a rule for what values m, n of the programmed delay the sample should be taken from *Data1* or *Data2*, it is necessary to consider certain timing constraints, which have to be fulfilled for all process corners: Fig. 9.6 depicts the timing diagram of the circuit. In order to guarantee that sampling the original signal results in a correct result, clk_1 must have a minimum delay to clk_0 , given by

$$\Delta t_{clk,min} = t_{ff} + t_{mux} + t_{su}, \quad (9.7)$$

with t_{ff} the propagation delay of the flip-flop (clock to data), t_{mux} the delay of the multiplexer, and t_{su} the setup-time of the flip-flop. An upper bound on t_{clk} is given by

$$\Delta t_{clk,max} = 25ns + t_{ff} + t_{mux} + t_{hold} - 2\tau_{mux}. \quad (9.8)$$

Combining (9.7), (9.8) with (9.7) results in the constraints on the programmed delay value τ_x

$$\tau_x > t_{ff} + t_{mux} + t_{su} - 2\tau_{mux} \quad (9.9)$$

$$\tau_x < 25ns + t_{ff} + t_{mux} - 2\tau_{mux} \quad (9.10)$$

The resulting allowed range for τ_x considering all process variations was then found to be

$$-6.8ns < \tau_x < 7.1ns. \quad (9.11)$$

A delay τ_x corresponds to a Vernier delay index n_x given by

$$n_x = \frac{(\tau_x + 25ns) \bmod(25ns)}{104ps}, \quad (9.12)$$

which results in an allowed interval $n_x = [175 \dots 239, 0 \dots 68]$. Dividing the range as shown by the frame in Fig. 9.4 thus fulfils the requirement of (9.11).

9.5 Command Decoding Logic

The command-decoding and error-correction logic, which was based on a previous circuit [CHRI-95b], uses clock gating [PIGU-96] in order to keep power consumption low. The internal clock signal for this part of the circuit is thus only activated upon an actual transmission of data in the B-channel.

9.6 Layout

The layout of the chip, shown in Fig. 9.7², comprises three different sections: The two clock phase shifters³, located in the upper right corner of the chip, the clock-and data recovery circuitry⁴, which is situated right below, and the digital logic, occupying most of the chip surface. Since the requirements on jitter and time-resolution are high, the sensible clock signals had to be protected against cross-talk by running them in shielded channels, consisting of a ground-connected poly layer below the signal wire and metal wires running in parallel for lateral shielding. Decoupling capacitances were added to minimise cross-coupling from the digital part over the power lines. The analog part was surrounded by large guard rings to reduce the effects of coupling over the substrate. The output pads of the clock signals are each surrounded by power supply pads.

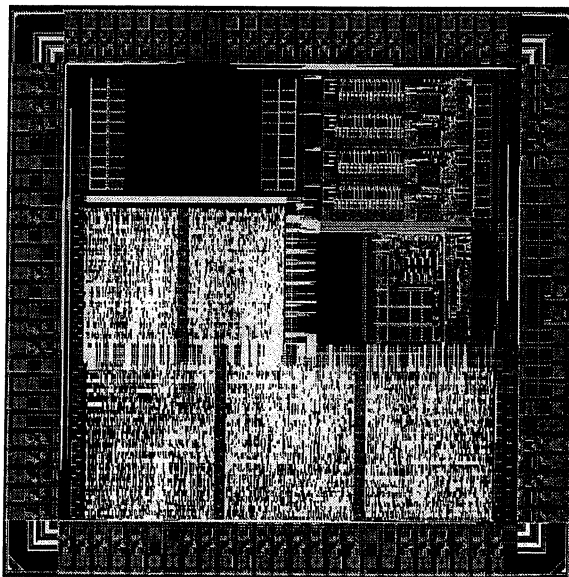


Figure 9.7: Layout of the TTCrx chip. The chip dimensions are $4.5 \times 4.5 \text{ mm}^2$.

²See also Figure G.4 on page 123.

³Figure G.6 on page 127.

⁴Figure G.5 of page 125.

9.7 Measurement Results

A prototype of the TTCrx chip was fabricated in a $0.8\ \mu\text{m}$ standard (non rad-hard) BiCMOS process. The clock recovery circuit, previously designed in the rad-hard DMILL process, was translated and included in the design. The final version of the TTCrx chip, however, will again be implemented in the rad-hard DMILL SOI technology. The chip was fully functional in the first prototype run.

High Resolution Clock Phase Shifter

The correct operation of the clock phase shifter can be seen in Figure 9.8, which displays the measured delay of the de-skewed clock as a function of the programmed delay. The integral deviation of the measured curve from the ideal curve is shown in Fig. 9.9. The curve shows some systematic errors from tap 20-150, which is probably a consequence of cross-coupling to an 80 MHz signal. Still, the integral non-linearity, with a maximum deviation of about one tap and an rms value of 61ps, is considerably low. The differential deviation is shown in Fig. 9.10, the rms value of the deviation amounts to 23ps, which corresponds to a standard deviation of a single DLL delay element of $23/\sqrt{2} = 16\text{ps}$ or 1.0% of a delay step, which is about the value that was to be expected from (9.5).

Jitter

Figures 9.12 and 9.13 show the rms and peak-to-peak clock output jitter as a function of optical input power. The input signal consisted of a sequence of alternating zeros and ones. For the nominal input power of -20 dBm, the rms value was measured to be 32 ps, peak-to-peak 231 ps. The measured clock-jitter for a $2^{12} - 1$ pseudo-random sequence in channel B, and a simulated trigger signal in channel A with a frequency of 100 kHz resulted in a value of 52.2 ps rms (418 ps peak-to-peak) for an optical signal with a power of -20dBm.

Trigger latency

The trigger latency, shown in Fig. 9.11 was measured to be 70 ns.

Power consumption

At a supply voltage of 3.3V, the chip consumed 140mW under typical operation conditions⁵.

⁵100 kHz Trigger in Channel A, random Data with 2% occupancy in Channel B, bunch counter outputs updated every 25ns.

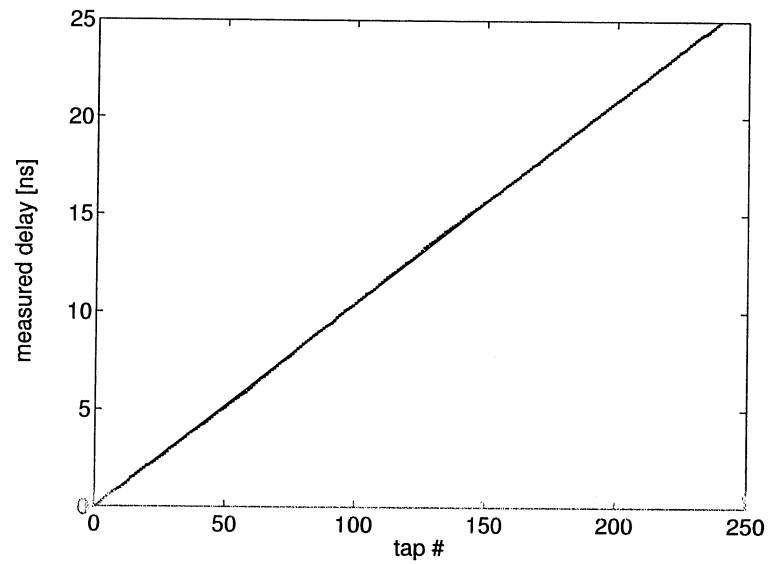


Figure 9.8: Measured delay as a function of programmed delay.

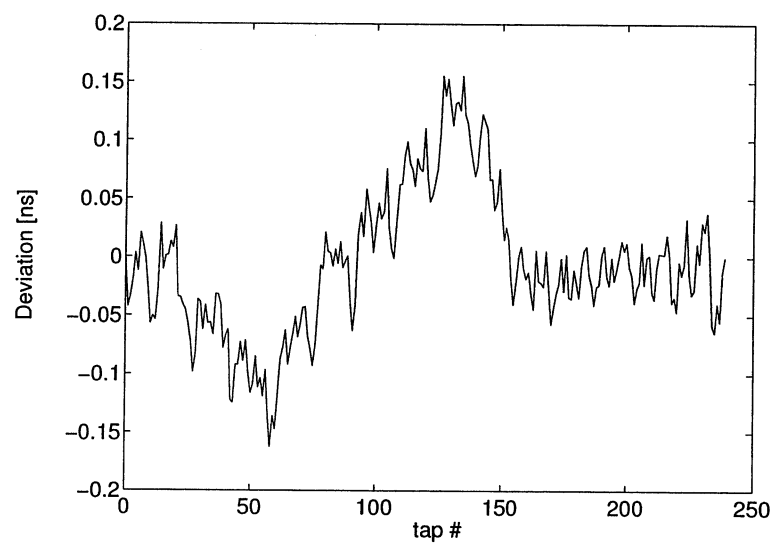


Figure 9.9: Integral deviation from ideal curve as a function of delay index.

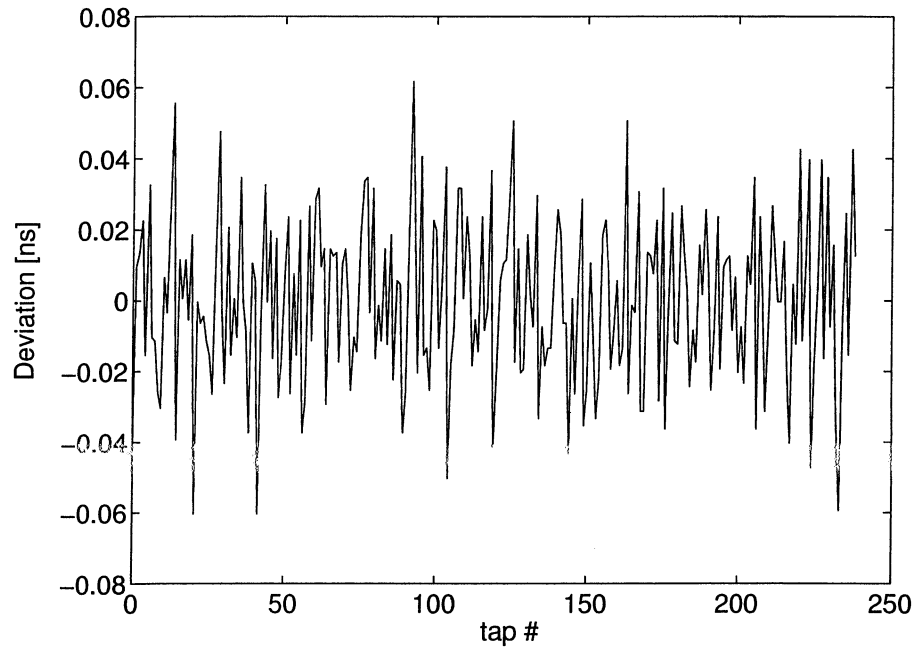


Figure 9.10: Differential deviation as a function of delay index.

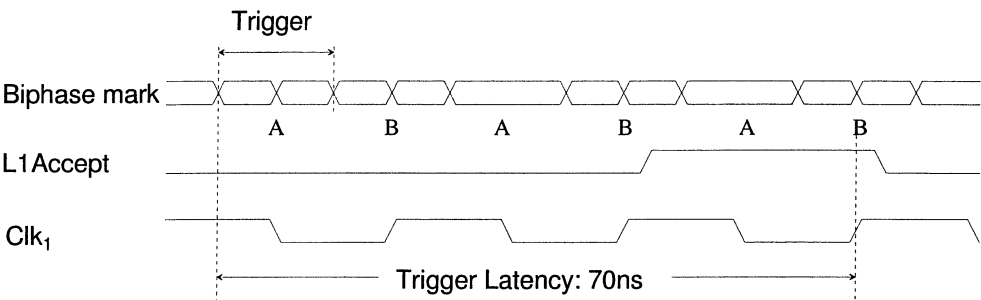


Figure 9.11: Trigger latency measurement.

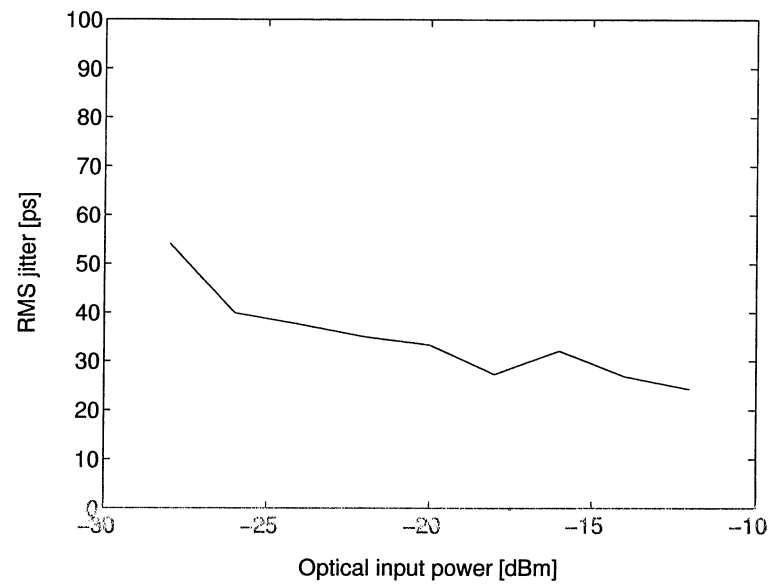


Figure 9.12: RMS jitter as a function of the optical input power.

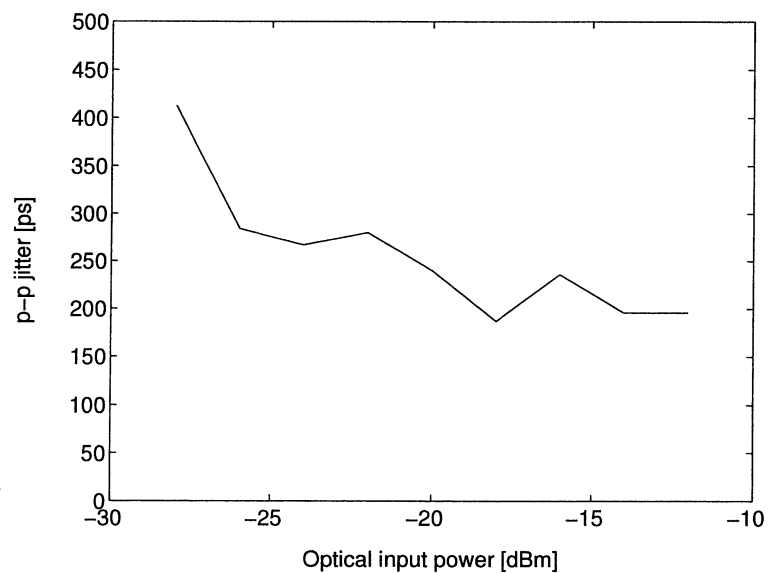


Figure 9.13: Peak-to-peak jitter as a function of the optical input power.

Chapter 10

Conclusions

In this work, we have presented three integrated circuits, which are crucial components for the synchronisation system of the now-developed high energy physics experiments at CERN.

- (1) Radiation-hard self-calibrating delay generation ASIC. This chip is the first of its kind to use a delay-locked loop to calibrate the signal delays in slave delay lines. At present, it is also the only radiation-hard chip available to generate precise delays. Its application is foreseen in a variety of locations within the trigger and data-acquisition system of ATLAS and CMS.
- (2) The radiation-hard 80 MHz clock and data recovery circuit proved the correct function of the novel frequency detector, phase-detector and the parameter-tolerant biasing concept. Although merely developed to test the new circuit structure and then be later included in the TTCrx ASIC, the chip itself can also be used stand-alone. Very low jitter was achieved, and the chip showed only minor degradations after a 10 Mrad gamma-irradiation.
- (3) Timing, Trigger and Control Receiver Chip. Since the prototype proved the correct function of the circuit, and the effects of irradiation on the crucial clock and data recovery and delay generation modules were studied in circuits (1) and (2), it is now straightforward to transfer the design to a radiation-hard technology. The chip, in either its current or the future radiation-hard version, will be a central part of the timing distribution system of all LHC particle detector systems (ATLAS, CMS, ALICE and LHCb).

Concerning the design of radiation-hard circuits, we conclude that the main problems are the increased spread in device parameters and radiation-induced mismatch. We proposed the following methods to achieve a robust design:

- (a) A parameter-tolerant PLL biasing scheme assures constant loop dynamics.
- (b) Using the clock signal as an external reference accurately defines the timing in delay generation circuits, independent of any device parameters.

- (c) A frequency detector with a wide detection range guarantees lock for an extended frequency range in clock and data recovery PLLs.

Concerning the design of matched delay lines and phase-locked loops, we arrived at the following conclusions:

- (a) *Matching of delay lines:* We analysed the factors, which determine the matching properties of delay lines, and showed that the matching requirements in a closed loop is by a factor of four less stringent than in the open loop case. Hence, it is easier to achieve good delay accuracy with periodic signals than with asynchronous signals.
- (b) *VCOs with Symmetric loads:* We presented an analytical solution of the frequency vs. control voltage curve $f(V_c)$ in VCOs with symmetric loads. We showed that the $f(V_c)$ curve given in [MANE-96] only holds for a limited frequency range.
- (c) *Parameter-independent biasing in PLLs:* We showed how the charge pump current and the loop filter resistance must relate to a given oscillator description $f(V_c)$ in order to achieve parameter-independent loop dynamics. For the case of a VCO using a single transistor in saturation, we presented a structure which was parameter-independent for the whole frequency range of the VCO. For this kind of VCO, the frequency range was however found to be limited to $\pm 50\%$. VCOs with symmetric loads, on the other hand, have a very broad frequency range, but due to its $f(V_c)$ -characteristic it is impossible to find simple structures to achieve parameter-independence for the whole frequency range. Parameter tolerance can be achieved, however, if the VCO frequency is constant and known in advance, as was the case in our application.
- (d) *Frequency detector for Biphase and NRZ signals:* We presented a novel frequency detector, which overcomes the lower frequency limitation of the Rotational Frequency Detector, and which does not require a quadrature VCO input. The correct function of the circuit with Biphase and NRZ data was proven in the clock and data recovery circuit.
- (e) *Phase detector:* The novel PD uses a state-machine to guarantee direct lock to a Biphase Mark input sequence. We showed how the lock-in range depends on the spacing of the signal samples. The correct function of the novel Phase Detector was also proven in the clock and data recovery circuit.
- (f) *Stability limit in bang-bang phase detectors:* We showed how a bang-bang phase-locked loop responds to a jump in frequency, and derived an expression for the maximum frequency the circuit can accept without losing lock. We then showed how this stability criterion relates jitter and static power supply rejection.
- (g) *Oscillator noise analysis:* We adapted the cyclo-stationary model from [HAJI-98a] to calculate cycle jitter and cycle-to-cycle jitter in the time domain. We showed that $1/f$ -noise did not have a significant effect on cycle-to-cycle jitter. The predicted value is in good accordance with the measurements.

Appendix A

Derivation of the Expected Integral Nonlinearity In a DLL

Assuming that the relative delay variance in one delay element is given by

$$\sigma_1^2 = \sigma^2(\Delta T/T), \quad (\text{A.1})$$

then the variance of the delay in a non-controlled delay-line after m delay elements is simply the sum of the variance from m elements

$$\sigma_m^2 = m\sigma_1^2(\Delta T/T). \quad (\text{A.2})$$

In a DLL, however, the overall delay after N stages is regulated to exactly one cycle time, hence imposing a constraint on the sum of all delay times

$$\sum_{k=1}^N T_k = T_{cycle}. \quad (\text{A.3})$$

Under this constraint, the variance of the delay after m stages is, of course, different to the open-loop case. It is to expect that the variance is smallest at the beginning of the delay line, reaches its maximum in the middle, and gets smaller again at the end. To derive the expected deviation we model a delay cell by

$$T_k(x) = x \cdot (T_0 + \delta_k), \quad (\text{A.4})$$

where k is the index of the delay cell, x is a multiplier describing the scaling of the delay with the control voltage, T_0 is the expectation value of the delay, and δ_k is the deviation from the expectation value due to device mismatch.

Inserting (A.4) into (A.3) determines the value of x

$$x = \frac{T_{cycle}}{N \cdot T_0 + \sum_{k=1}^N \delta_k}. \quad (\text{A.5})$$

Hence, for a given delay line, a correction value x is found by the DLL in order to achieve an overall delay of T_{cycle} . We now want to know the variance of the delay time after m delay cells, normalized to the ideal delay value of a single delay cell

$$\sigma_m^2 = \sigma^2 \left(\frac{\sum_{k=1}^m T_k}{T_{cycle}/N} \right) = \sigma^2(y). \quad (\text{A.6})$$

By substituting (A.5) for T_{cycle} , the expression in the bracket can be rewritten

$$y = \frac{N \cdot x \sum_{k=1}^m T_0 + \delta_k}{x \sum_{l=1}^N T_0 + \delta_l} = m \frac{1 + \sum_{k=1}^m \frac{\delta_k}{mT_0}}{1 + \sum_{l=1}^N \frac{\delta_l}{NT_0}}, \quad (\text{A.7})$$

Since $\frac{\delta_k}{T_0} \ll 1$, (A.7) can be approximated by

$$y \cong m + \sum_{k=1}^m \frac{\delta_k}{T_0} - \sum_{l=1}^N \frac{m\delta_l}{NT_0} = \quad (\text{A.8})$$

$$= m + \sum_{k=1}^m \left(1 - \frac{m}{N}\right) \frac{\delta_k}{T_0} - \sum_{l=(m+1)}^N \frac{m}{N} \frac{\delta_l}{T_0}. \quad (\text{A.9})$$

The expression contains a sum of weighted independent normal random variables, hence the variance of y is

$$\sigma^2(y) = \sigma^2\left(\frac{\delta_k}{T_0}\right) \left[m \left(1 - \frac{m}{N}\right)^2 + (N - m) \left(\frac{m}{N}\right)^2 \right] = \quad (\text{A.10})$$

$$= \sigma_1^2 \cdot \left[\frac{m \cdot (N - m)}{N} \right]. \quad (\text{A.11})$$

It is straightforward to show that the function has a maximum in the middle of the delay line ($m = N/2$), with

$$\sigma_{N/2}^2 = \frac{N}{2} \sigma_1^2. \quad (\text{A.12})$$

Consequently, the variance of the maximum time deviation in a DLL structure is 1/4 the value of a non-controlled delay-line.

Appendix B

Derivation of the Delay Matching in a Current-Starved Inverter Cell

To get a better understanding of matching in the delay elements, the variance of the delay time as a function of transistor matching parameters can be derived. Using a simple model of a starved inverter cell, the delay time T can be expressed as

$$T = \frac{C}{\beta(V_c - V_t)^2}, \quad (\text{B.1})$$

where C [F] is the overall load capacitance, β [A/V^2] denotes the device transconductance of the MOS current source, $V_c(= V_{gs})$ the control voltage of the current starved inverter cell, and V_t the threshold voltage. For simplicity, we will assume perfect symmetry between NMOS and PMOS transistors.

For small deviations of the parameters C , β , V_t , (B.1) becomes

$$T(\Delta\beta, \Delta V_t, \Delta C) = \frac{C + \Delta C}{(\beta + \Delta\beta)[V_c - (V_t + \Delta V_t)]^2}. \quad (\text{B.2})$$

The deviation ΔT from its nominal value T_0 can be approximated by the first term of a Taylor series expansion

$$\Delta T(\Delta\beta, \Delta V_t, \Delta C) = \frac{\partial T}{\partial \beta} \Delta\beta + \frac{\partial T}{\partial V_t} \Delta V_t + \frac{\partial T}{\partial C} \Delta C, \quad (\text{B.3})$$

resulting in

$$\frac{\Delta T}{T} = -\frac{\Delta\beta}{\beta} + \frac{2V_t}{(V_c - V_t)} \Delta V_t + \frac{\Delta C}{C}. \quad (\text{B.4})$$

Now, the variance of the relative delay deviation can be calculated, assuming independence between the parameters,

$$\sigma^2\left(\frac{\Delta T}{T}\right) = \sigma_\beta^2 + \frac{4}{(V_c - V_t)^2} \sigma_{V_t}^2 + \sigma_C^2, \quad (\text{B.5})$$

where $\sigma^2(\cdot)$ denotes the variance operator, and σ_β^2 , $\sigma_{V_t}^2$, σ_C^2 are defined as

$$\sigma_\beta^2 = \sigma^2(\Delta\beta/\beta) = K_\beta/(WL), \quad (\text{B.6})$$

$$\sigma_{V_t}^2 = \sigma^2(\Delta V_t/V_t) = K_{V_t}/(WL) \quad (\text{B.7})$$

$$\sigma_C^2 = \sigma^2(\Delta C/C) = K_C/(WL), \quad (\text{B.8})$$

being inversely proportional to the transistor device area $W \cdot L$ [MICH-93] with proportionality factors K_β , K_{V_t} and K_C . Hence, the variance of the delay deviation of a single cell can be expressed as

$$\sigma^2\left(\frac{\Delta T}{T}\right) = \frac{1}{WL} \left[K_\beta + \frac{4}{(V_c - V_t)^2} K_{V_t} + K_C \right]. \quad (\text{B.9})$$

It can be seen that in order to achieve good matching, it is necessary to use devices with large area, and to make sure that $V_c - V_t$ does not get too small for the whole range of operating conditions.

Appendix C

Analytical Solution of Symmetric Load Behaviour

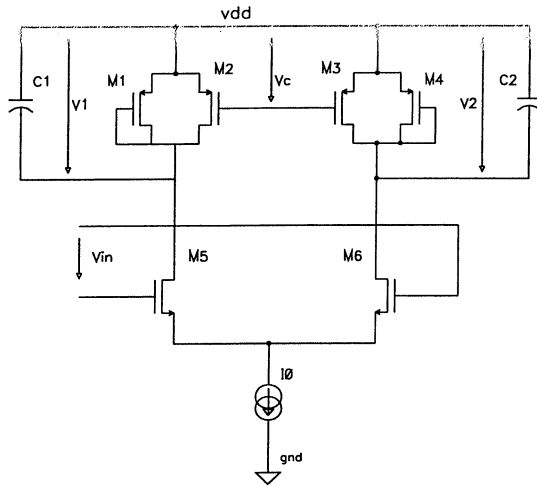


Figure C.1: Differential delay cell with symmetric loads.

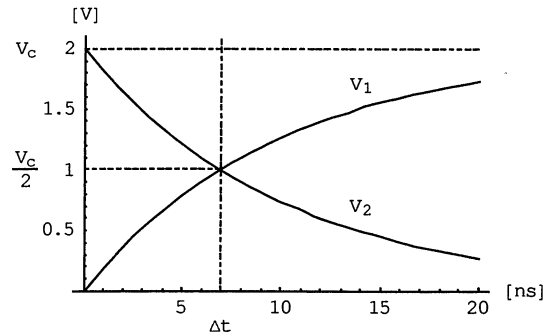


Figure C.2: Voltage behaviour after switching instant.

This chapter presents an analytical solution for the delay time as function of control voltage $\Delta t(V_c)$ of a differential structure with symmetric loads, shown in Figure C.1. Symmetric loads consists of two MOS transistors of the same dimensions, one connected to the control voltage V_c , while the other is diode-connected. A current I_0 is steered by a differential stage in either the left or the right branch of the structure. I_0 is regulated such that the voltage, referenced to ground, at the lower swing limit equals $V_{DD} - V_c$. In this point, the gate-source voltages of both transistors amount to $-V_c$. Assuming non-minimum length transistors, the simple MOS square-law can be applied, resulting in a current $I_0 = \frac{2\beta}{2}(V_c - V_t)^2$.

Figure C.2 displays the transients of the output voltages V_1 and V_2 after the switching moment. It is assumed that the current through the delay cell I_0 switches immediately from the left to the right branch after the input voltage V_{in} changes polarity. V_1 starts at 0 V

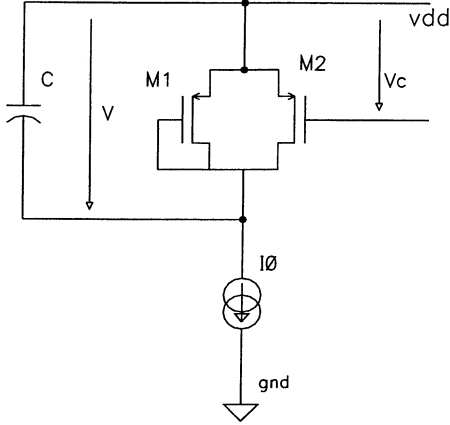
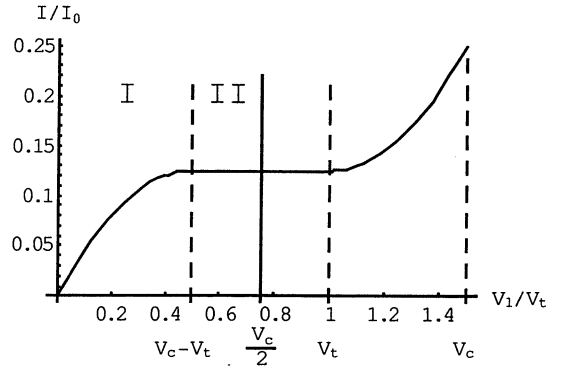


Figure C.3: Symmetric load.

Figure C.4: $I_{sl}(V)$ for case I, $V_c = 1.6V_t$.

and approaches V_c , while V_2 starts from V_c and approaches 0 V. The next delay cell starts to switch when $V_1 = V_2 = V_c/2$.

In order to calculate the delay time Δt we look at a single symmetric load connected to a capacitance C and a current source I_0 as shown in Figure C.3. At time $t = 0$ the voltage at the capacitance $V = 0$. We now want to know how long it takes to charge the capacitance to $V_c/2$. Applying Kirchhoff's laws results in the differential equation

$$C \frac{dV}{dt} + I_{sl}(V, V_c) = I_0, \quad (C.1)$$

with $I_{sl}(V)$ being the current through the symmetric load as a function of the control voltage V_c and the voltage V at the capacitance. Unfortunately, as a consequence of the different MOS transistor operating regions, several cases have to be considered in order to describe $I_{sl}(V, V_c)$.

Case 1: $V_t < V_c < 2V_t$

Figure C.4 shows the case that the control voltage is less than two times the threshold voltage. In region I, where $V < (V_c - V_t)$, transistor M2 is in the triode region and transistor M1 is off:

$$I_{sl,I} = \beta[(V_c - V_t)V - 1/2V^2],$$

while in region II, where $V_c - V_t < V < V_c/2$, M2 is in current-source mode. Since M1 only starts to conduct after V has passed $V_c/2$ it does not have to be considered.

In region I, eq.(C.1) becomes

$$C \frac{dV}{dt} + \beta[(V_c - V_t)V - 1/2V^2] = \beta(V_c - V_t)^2, \quad V(t=0) = 0, \quad (C.2)$$

with solution

$$V(t) = (V_c - V_t)[1 - \tan(\frac{\pi}{4} - t \frac{\beta(V_c - V_t)}{2C})] \quad (C.3)$$

Solving for $V(t_1) = V_c - V_t$ gives the time t_1 it takes $V(t)$ to reach $V_c - V_t$,

$$t_1 = \frac{C}{\beta} \left[\frac{\pi}{2} \frac{1}{(V_c - V_t)} \right]. \quad (\text{C.4})$$

In region II, the corresponding differential equation is

$$C \frac{dV}{dt} + \frac{\beta}{2} (V_c - V_t)^2 = \beta (V_c - V_t)^2, \quad V(t=0) = V_c - V_t \quad (\text{C.5})$$

with solution

$$V(t) = (V_c - V_t) + \frac{\beta (V_c - V_t)^2}{2C}. \quad (\text{C.6})$$

Now, solving for $V(t_2) = V_c/2$ results in

$$t_2(V_c) = \frac{C}{\beta} \left[\frac{2V_t - V_c}{(V_c - V_t)^2} \right] \quad (\text{C.7})$$

The overall time $\Delta t_I = t_1 + t_2$ to reach $V_c/2$ is

$$\Delta t_I(V_c) = \frac{C}{\beta} \left[\frac{\pi}{2} \frac{1}{V_c - V_t} + \frac{2V_t - V_c}{(V_c - V_t)^2} \right] \quad (\text{C.8})$$

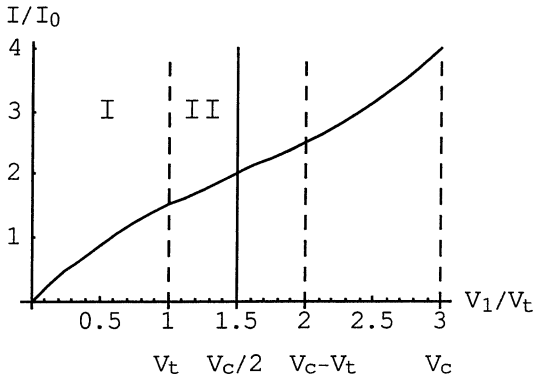


Figure C.5: $I_{sl}(V)$ for case II, $V_c = 1.6V_t$.

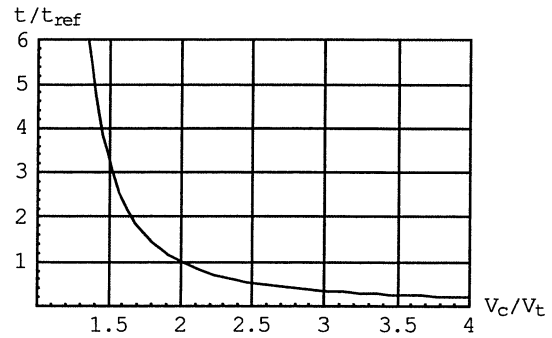


Figure C.6: Δt as a function of V_c .

Case 2: $V_c \geq 2V_t$

In the second case, when V_c exceeds $2V_t$, transistor M1 starts to conduct at $V > V_t$. Again, two regions have to be defined as shown in Fig. C.5. In region I, where $V_c < V_t$, transistor M1 is off, and M2 is in the triode region. In region II, M2 is still in the triode region, but M1 starts to conduct. Therefore, in region I, the differential equation is again given by (C.2). Now eq. (C.3) is solved for $V(t_1) = V_t$, resulting in

$$t_1(V_c) = \frac{C}{\beta} \left[\frac{\frac{\pi}{2} - \arccos \sqrt{\frac{(V_c - V_t)^2}{(V_c - V_t)^2 + (V_c - 2V_t)^2}}}{V_c - V_t} \right]. \quad (\text{C.9})$$

In region II, the total current from M1 and M2 is given by

$$I_{sl} = \beta[(V_c - 2V_t)V + \frac{1}{2}V_t^2].$$

It is to remark that now there is a perfectly linear relationship between V and I_{sl} in this region. The differential equation is given by

$$C \frac{dV}{dt} + \frac{\beta}{2}[(V_c - 2V_t)V + \frac{1}{2}V_t^2] = (V_c - V_t)^2, \quad V(t=0) = V_t \quad (C.10)$$

with solution

$$V(t) = V_t + \frac{(V_c - V_t)^2 + (V_c - 2V_t)^2}{2(V_c - 2V_t)} \left[1 - \exp \left(1 + \frac{(V_c - 2V_t)^2}{(V_c - V_t)^2} \right) \right] \quad (C.11)$$

Solving for $V(t_2) = V_c/2$ results in

$$t_2(V_c) = \frac{C}{\beta} \left[\frac{1}{(V_c - 2V_t)} \log \left(1 + \frac{(V_c - 2V_t)^2}{(V_c - V_t)^2} \right) \right]. \quad (C.12)$$

The overall time $\Delta t_{II} = t_1 + t_2$ to reach $V_c/2$ is

$$\Delta t_{II}(V_c) = \frac{C}{\beta} \left[\frac{\frac{\pi}{2} - \arccos \sqrt{\frac{(V_c - V_t)^2}{(V_c - V_t)^2 + (V_c - 2V_t)^2}}}{V_c - V_t} + \frac{\log \left(1 + \frac{(V_c - 2V_t)^2}{(V_c - V_t)^2} \right)}{V_c - 2V_t} \right] \quad (C.13)$$

The overall solution, graphically shown in Fig.C.6, is now given by

$$\Delta t(V_c) = \begin{cases} \infty & \text{if } V_c < V_t, \\ \frac{C}{\beta} \left[\frac{\pi}{2} \frac{1}{V_c - V_t} + \frac{2V_t - V_c}{(V_c - V_t)^2} \right] & \text{if } V_t < V_c < 2V_t, \\ \frac{C}{\beta} \left[\frac{\frac{\pi}{2} - \arccos \sqrt{\frac{(V_c - V_t)^2}{(V_c - V_t)^2 + (V_c - 2V_t)^2}}}{V_c - V_t} + \frac{\log \left(1 + \frac{(V_c - 2V_t)^2}{(V_c - V_t)^2} \right)}{V_c - 2V_t} \right] & \text{if } V_c \geq 2V_t. \end{cases} \quad (C.14)$$

Appendix D

VCO Noise Analysis

In order to estimate the effect of noise in a ring VCO, we will use a procedure similar to [HAJI-98a], but instead of deriving an expression for phase noise in the frequency domain, we will calculate the expected jitter in the time-domain. The voltage signal coming out of the oscillator is given by

$$V_{VCO}(t) = f(\omega_0 t + \phi(t)), \quad (\text{D.1})$$

in which $f(\cdot)$ is a cyclic function with period 2π , ω_0 is the angular frequency, and $\phi(t)$ is a zero-mean random process describing the phase fluctuations. Let t_n denote the time instance for which the phase is a multiple of 2π

$$t_n = \frac{2\pi \cdot n - \phi(t_n)}{\omega_0}. \quad (\text{D.2})$$

Hence $\phi_n(t_n)$ is the phase deviation (from 2π) of cycle n caused by noise. The cycle jitter is commonly measured by the variance of the phase deviation

$$\sigma_\phi^2 = E[\phi(t_n)^2] \quad (\text{D.3})$$

The cycle-to-cycle jitter is measured as the variance of the *difference* in phase [HERZ-98]¹² of two consecutive cycles

$$\sigma_{\Delta\phi}^2 = E[(\phi(t_{n+1}) - \phi(t_n))^2] \quad (\text{D.4})$$

Figure D.1 displays the noise sources in one differential delay cell, which are assumed to be statistically independent. The total variance of the cycle phase variation can therefore

¹It is also possible to specify cycle-to-cycle jitter as the variance of the difference in cycle *time*. We prefer the notation using phase, however, since it allows an easy comparison between oscillators running at different frequencies.

²Some authors [WEIG-94] also call cycle-to-cycle jitter, what in our terminology, which is the one found in [HERZ-98], is called cycle jitter.

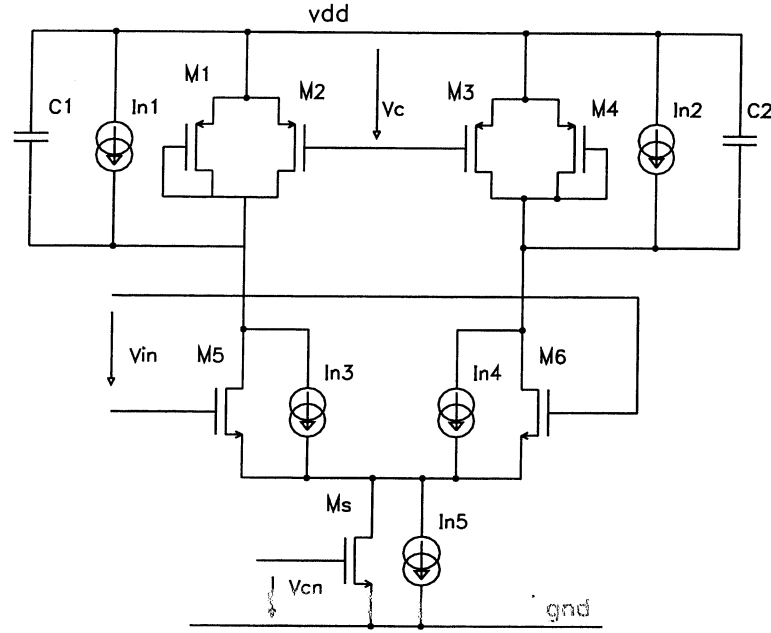


Figure D.1: Oscillator delay stage with noise sources.

be calculated by summing up the contributions from all the current sources in the ring oscillator

$$\sigma_{\phi, total}^2 = \sum_{n=1}^N \sigma_{\phi, n}^2. \quad (D.5)$$

As shown in the figure, there are three different types of noise sources in each differential oscillator cell, which are the noise sources connected to the load transistors (I_{n1}, I_{n2}), the switching transistors (I_{n3}, I_{n4}), and the current source transistor (I_{n5}).

First Order Analysis

In a first order model, the phase change per cycle caused by a noise current $i_n(t)$ is proportional to the total injected charge per cycle

$$\phi = \frac{1}{q_{max}} \int_0^T \Gamma_0 \cdot i_n(t) dt, \quad (D.6)$$

where q_{max} denotes the maximum charge stored in a delay cell during one cycle

$$q_{max} = \Delta V \cdot C_o, \quad (D.7)$$

with voltage swing ΔV and C_o the capacitance of a half delay cell. The factor Γ_0 in (D.6) describes the relation between excess phase ϕ and injected charge Δq (normalized by q_{max}).

$$\Gamma_0 = \frac{\phi}{\Delta q / q_{max}}. \quad (D.8)$$

It is to note that the definition of q_{max} according to (D.7) is arbitrary, since it is cancels out when (D.8) is substituted in (D.6). On the other side, the value of q_{max} is related to the current in the differential cell I_0 and the cycle time T_0 via

$$T_0 = N \frac{C\Delta V}{I_0}, \quad (D.9)$$

and hence $q_{max} = (T_0 I_0)/N$.

Since the device noise current is a stationary random process, the integration in (D.6) can be interpreted as a linear filter applied on the random process $i_n(t)$

$$\phi(t) = i_n(t) * h(t), \quad (D.10)$$

with $h(t)$ being a rectangular pulse of width T and height Γ_0/q_{max} , and "*" denoting the convolution operator. Sampling $\phi(t)$ at times kT then results in the random variable ϕ_k , describing the cycle jitter. If the random process $i_n(t)$ is white, then the cycle jitter can be expresses as

$$\sigma_\phi^2 = (\sigma_i^2/df) \cdot E_h \quad (D.11)$$

with σ_i^2/df defined as the power spectral density of the white noise current [A^2/Hz] and E_h denoting the "energy" of the filter function $h(t)$

$$\begin{aligned} E_h &= \int_{-\infty}^{\infty} |h(t)|^2 df \\ &= T \cdot \frac{\Gamma_0^2}{q_{max}^2} \end{aligned} \quad (D.12)$$

Time-Variant Model

In the first order model Γ_0 in (D.8) is defined as a constant and the noise current $i_n(t)$ is assumed to be a wide-sense stationary random process with constant standard deviation σ_i . A constant Γ_0 means that a charge Δq injected in a node of the oscillator always results in a phase jump of $\Gamma_0 \cdot \Delta q/q_{max}$, independent of the current state of the node. Since the oscillator is a non-linear time-variant circuit, however, the effective phase deviation caused by Δq depends on the time of its injection. It is intuitively clear that a charge injected just before the moment of switching the differential pair causes a greater phase deviation than after switching. The dependency of the phase change due to an injected charge on the moment of injection can be measured by a method described in [HAJI-98a]. Small current pulses are injected at known phase angles, and the resulting phase shift at the output of the oscillator is measured. The resulting *Impulse Sensitivity Function* (ISF) displays the variation of $\Gamma(\omega_0 t)$ within a clock period of the oscillator. For example, the curve marked " Γ_{load} " in Figure D.2 (page 102) displays the ISF for the load transistors.

Another refinement of the first order model takes the amplitude modulation of the noise-sources into account. The noise current source $i_n(t)$ is modulated with a cyclic function $\alpha(\omega_0 t)$, which is normalized in order to have a maximum value of 1.

$$i_n(t) = i_{n,max}(t) \cdot \alpha(\omega_0 t) \quad (D.13)$$

Rewriting (D.6) for the case of time-varying $\Gamma(t)$ and $i_n(t)$ results in

$$\phi = \frac{1}{q_{max}} \int_0^T i_{n,max}(t) \cdot \Gamma(\omega_0 t) \cdot \alpha(\omega_0 t) dt, \quad (D.14)$$

The impulse response function $h(t)$ of the corresponding linear filter applied to the stationary random process $i_{n,max}(t)$ is defined as

$$h(t) = \frac{1}{q_{max}} \text{rect}(t - T/2, T) \cdot \Gamma(\omega_0 t) \alpha(t), \quad (D.15)$$

with energy

$$E_h = \frac{1}{q_{max}^2} \int_0^T \Gamma(\omega_0 t)^2 \alpha(\omega_0 t)^2 dt. \quad (D.16)$$

By combining the effects of the impulse sensitivity function and the source amplitude modulation into a single function

$$\Gamma_{eff}(\xi) = \Gamma(\xi) \cdot \alpha(\xi) \quad (D.17)$$

and substituting ξ for $\omega_0 t$, a value $\overline{\Gamma_{eff}^2}$, independent of the cycle time T , can be defined as

$$\overline{\Gamma_{eff}^2} = \frac{1}{2\pi} \int_0^{2\pi} \Gamma_{eff}(\xi)^2 d\xi. \quad (D.18)$$

The variance of cycle jitter for white noise is then given by

$$\sigma_\phi^2 = \frac{T}{q_{max}^2} \cdot \overline{\Gamma_{eff}^2} \cdot (\sigma_{i,max}^2 / df), \quad (D.19)$$

where $\sigma_{i,max}^2 / df$ is the power spectral density of the maximum noise current $i_{n,max}$.

Cycle-to-Cycle Jitter for White Noise

Using (D.4) the cycle-to-cycle jitter calculates to

$$\sigma_{\Delta\phi}^2 = E[\phi(t_{n+1})^2] + E[\phi(t_n)^2] - 2E[\phi(t_{n+1})\phi(t_n)]. \quad (D.20)$$

Since for white noise $\phi(t_{n+1})$ is independent from $\phi(t_n)$, and $\phi(t_n)$ is a zero-mean random process, the last term of (D.20) is zero. Hence, the cycle-to-cycle jitter is two times the cycle jitter

$$\sigma_{\Delta\phi}^2 = 2 \cdot \sigma_\phi^2 \quad (D.21)$$

Device	$\overline{\Gamma_{eff}^2}$	$g_{m,max}[mS]$	# Sources	$\sigma_\phi[10^{-3} \cdot rad]$
Load	0.227	0.56	8	0.51
Switch	0.025	0.45	8	0.15
I-source	0.526	1.60	4	0.93
Total				1.07

Table D.1: Actual cycle-to-cycle jitter due to thermal noise of the components for $I_0 = 200\mu A$.

Thermal Noise

Thermal noise is present in every transistor as white noise with power spectral density

$$\sigma_i^2 = 4kT \cdot g_{m,eq} \cdot df/2, \quad (D.22)$$

where k is Boltzmann's constant, T the temperature in Kelvin, and $g_{m,eq}$ the equivalent channel conductance, which, depending on the mode of operation of the transistor is given by

$$g_{m,eq} = \begin{cases} \frac{2}{3}g_m & \text{(in saturation and strong inversion)} \\ 1/R_{lin} & \text{(linear region),} \end{cases} \quad (D.23)$$

where g_m is the channel transconductance in saturation, and R_{lin} is the equivalent resistance of a MOS transistor in the linear region given by

$$R_{lin} = \frac{1}{\beta(V_{gs} - V_T)}. \quad (D.24)$$

The amplitude modulation function $\alpha_{white}(\xi)$ then results in

$$\alpha_{white}(\xi) = \frac{g_{m,eq}(\xi)}{g_{m,max}}. \quad (D.25)$$

Figures D.2-D.4 display the impulse sensitivity function $\Gamma(\xi)$ together with the current modulation function $\alpha_{white}(\xi)$ and the resulting $\Gamma_{eff}(\xi)$ for the different noise sources in the oscillator. Since the current of the current source transistor (M_s in Figure D.1) is always constant, no modulation of the noise current amplitude happens in this case. Table D.1 displays the actual distribution of jitter caused by thermal noise. For a nominal oscillator current of $I_0 = 200\mu A$ the total jitter only amounts to $\sigma_\phi = 1.07rad$, which corresponds to an rms jitter value of 2.1 ps at a frequency of 80 MHz. It is remarkable that the biggest contribution stems from the current source transistor, which is neglected in the analysis of a similar oscillator cell in [HAJI-98b]. It is however clear that a noise current in the current sources must be taken into account, because a deviation in I_0 in (D.9) has a direct influence on the cycle time.

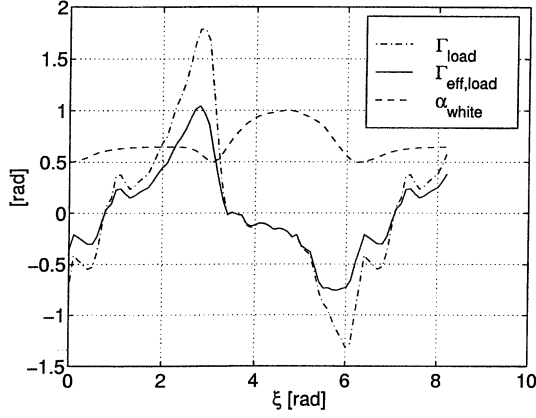


Figure D.2: $\Gamma(\xi)$, $\Gamma_{eff}(\xi)$ and $\alpha(\xi)$ for the symmetrical loads and thermal noise.

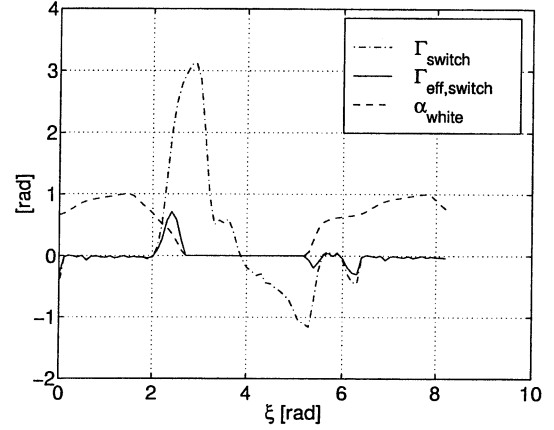


Figure D.3: $\Gamma(\xi)$, $\Gamma_{eff}(\xi)$ and $\alpha(\xi)$ for the switch transistors and thermal noise.

1/f-Noise

The $1/f$ (=flicker)-noise sources in CMOS transistors have a power spectrum which is modeled in SPICE simulations as

$$\sigma_i^2(f) = KF \cdot \frac{I^{AF}}{C_{ox} \cdot L_{eff}^2} \cdot \frac{df}{f}, \quad (D.26)$$

with transistor noise model parameters KF and AF , oxide capacitance per area C_{ox} and effective transistor length L_{eff} . It is impossible to calculate the cycle jitter variance σ_ϕ^2 by an integration of the filtered power spectral density since the integral does not converge. The cycle jitter due to $1/f$ -noise therefore is infinite. Since flicker noise is concentrated at low frequencies, however, it causes only slow variations of the VCO frequency which are filtered out in a phase locked loop. It is possible to calculate the amount of cycle-to-cycle jitter caused by flicker noise

$$\sigma_{\Delta\phi}^2 = E[(\phi_{n+1} - \phi_n)^2]. \quad (D.27)$$

We define a random process $\Delta\phi(t)$ by

$$\Delta\phi(t) = \frac{1}{q_{max}} \int_0^T i_{n,max}(t) \cdot \Gamma_{eff}(\omega_0 t) dt - \frac{1}{q_{max}} \int_T^{2T} i_{n,max}(t) \cdot \Gamma_{eff}(\omega_0 t) dt, \quad (D.28)$$

in which $\Gamma_{eff}(\omega_0 t) = \Gamma(\omega_0 t) \cdot \alpha(\omega_0 t)$ takes the amplitude modulation of the flicker noise current according to (D.26) into account, with $\alpha_{1/f}(\omega_0 t)$ given by

$$\alpha_{1/f}(\omega_0 t) = \frac{i_n^{AF}(\omega_0 t)}{i_{n,max}^{AF}}. \quad (D.29)$$

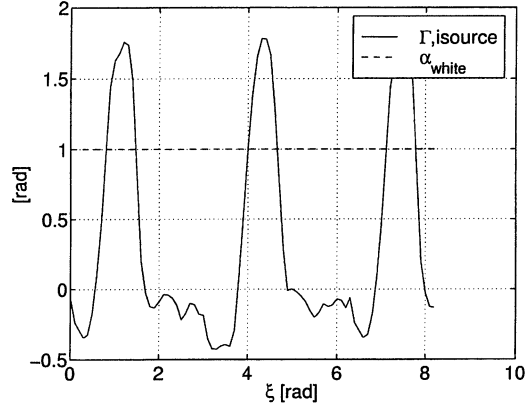


Figure D.4: $\Gamma(\xi) = \Gamma_{eff}(\xi)$ for the current source.

Combining the two integral terms of (D.28) and substituting t by $\xi = t\omega_0$ results in the convolution integral

$$\Delta\phi(t) = \int_0^{4\pi} \hat{i}_n(\xi) \frac{1}{q_{max} \cdot \omega_0} h(\xi) d\xi, \quad (D.30)$$

with $h(\xi)$ defined as

$$h(\xi) = [\text{rect}(\xi - \pi, \pi) - \text{rect}(\xi - 3\pi, \pi)] \cdot \Gamma_{eff}(\xi), \quad (D.31)$$

and $\hat{i}_n(\xi)$ being a time-scaled version of the random process $i_n(t)$

$$\hat{i}_n(\xi) = i_n(\xi/\omega_0), \quad (D.32)$$

with power spectrum density $\hat{X}_i(\omega) = (1/\omega_0)X_i(\omega/\omega_0)$. Since $X_i(\omega)$ has a $1/f$ spectrum given by $X_i(\omega) = k/\omega$ with constant k , it thus follows that

$$\hat{X}_i(\omega) = X_i(\omega). \quad (D.33)$$

The variance of the cycle-to-cycle jitter, $\sigma_{\Delta\phi}^2$ is then given by

$$\sigma_{\Delta\phi}^2 = \sigma_{i,max}^2 \cdot \frac{1}{\omega_0^2 \cdot q_{max}^2} \cdot \overline{\Delta\Gamma_{eff}^2}, \quad (D.34)$$

where $\overline{\Delta\Gamma_{eff}^2}$ is a frequency-independent constant which includes the effects caused by the cyclic modulation of current amplitude and impulse sensitivity and is given by

$$\overline{\Delta\Gamma_{eff}^2} = \frac{1}{2\pi} \int_{-\infty}^{\infty} |H(j\omega)|^2 \cdot \frac{2\pi}{\omega} d\omega \quad (D.35)$$

with $H(j\omega)$ being the Fourier transform of $h(\xi)$. Hence, with the knowledge of $\Gamma_{eff}(\xi)$, $H(j\omega)$ and thus $\overline{\Delta\Gamma_{eff}^2}$ can be derived numerically. Substituting the expression for $\sigma_{i,max}^2$ from (D.26) then results in

$$\sigma_{\Delta\phi}^2 = \frac{1}{2}KF \cdot \frac{I_{max}^{AF}}{C_{ox}L_{eff}^2} \cdot \frac{1}{\omega_0^2 \cdot q_{max}^2} \cdot \overline{\Delta\Gamma_{eff}^2}, \quad (D.36)$$

where the factor $1/2$ stems from the definition of (D.26) as the *one*-sided power spectral density function.

Figures D.5 and D.6 display the impulse sensitivity function $\Gamma(\xi)$ together with the noise current modulation function $\alpha_{1/f}(\xi)$ and the resulting $\Gamma_{eff}(\xi)$ for the switch transistor and the current source in the oscillator.

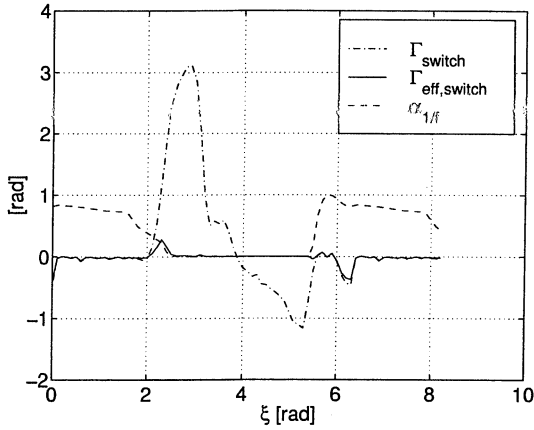


Figure D.5: $\Gamma(\xi)$, $\Gamma_{eff}(\xi)$ and $\alpha_{1/f}(\xi)$ for the symmetrical loads and $1/f$ -noise.

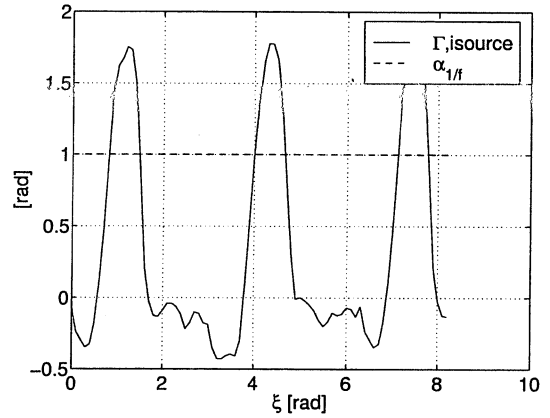


Figure D.6: $\Gamma(\xi)$, $\Gamma_{eff}(\xi)$ and $\alpha_{1/f}(\xi)$ for the switch transistors and $1/f$ -noise.

Table D.2 contains the resulting values for $\sigma_{\Delta\phi}$ of the actual circuit. It is to note that only the NMOS transistors were considered for calculating $1/f$ -noise, because KF of the PMOS devices, used in the resistor loads, is two orders of magnitude below the value for NMOS transistors. The standard deviation of cycle-to-cycle jitter amounts to 55.910^{-6} rad or 0.11 ps, which is more than a factor of 25 below the standard deviation stemming from thermal noise, given by $\sigma_{\Delta\phi} = \sqrt{2}\sigma_{\phi}$. This slow variations caused by $1/f$ noise is corrected by the control loop and will therefore not affect the cycle-to-cycle jitter properties of the oscillator.

Device	$\overline{\Delta\Gamma_{eff}^2}$	$\sigma_i[nA/\sqrt{Hz}]$	# Sources	$\sigma_{\Delta\phi}[10^{-6} \cdot rad]$
Switch	0.91	3.97	8	51.1
I-source	2.06	3.64	4	22.1
Total				55.9

Table D.2: Actual variance of cycle-to-cycle phase difference due to $1/f$ noise of the components for $I_0 = 200\mu A$.

Appendix E

Stability Limit in Bang-Bang Phase-Locked Loops

In this chapter, we derive an expression for the maximum jump in (input or oscillator) frequency that a second-order PLL with a bang-bang phase detector can accept without losing lock.

After each cycle, the bang-bang phase detector makes a new binary decision and, consequently, a positive or negative charge pump current flows through the loop filter during the whole oscillator period. The proportional part of the loop response, stemming from the current flowing in the loop filter resistor, gives rise to a constant and immediate change ΔT_p of the loop cycle time T , whereas the change in cycle time caused by the integral part grows linearly with time.

A jump of the power supply voltage leads to a change in the VCO frequency Δf , equivalent to the case that the frequency of the input signal jumps by Δf . For the subsequent analysis, we will thus assume a perfect VCO and a jump of the input frequency.

Fig. E.1 shows how the PLL responds to a jump in frequency: Before the jump, the decision of the phase-detector will constantly toggle between *early* and *late*. The VCO is then constantly switched between two frequencies.

After a jump in frequency, the loop tries to catch the input signal running away in phase, by maintaining a constant *late*-decision. The VCO frequency thereby rises linearly with time, the VCO excess phase quadratically. Ultimately, the curves of VCO phase and input signal phase cross. During this process, the phase deviation reaches a maximum value, which must be smaller than the maximum phase deviation, which the phase detector can accept without losing lock.

The input excess phase after a frequency jump of Δf is given by

$$\Theta_{inp} = n \cdot \Delta\Theta_{cycle}, \quad (\text{E.1})$$

with n denoting the cycle index after the jump, and $\Delta\Theta_{cycle}$ the change in phase per cycle in [rad], given by

$$\Delta\Theta_{cycle} = \frac{\Delta f}{f_0} \cdot 2\pi \quad (\text{E.2})$$

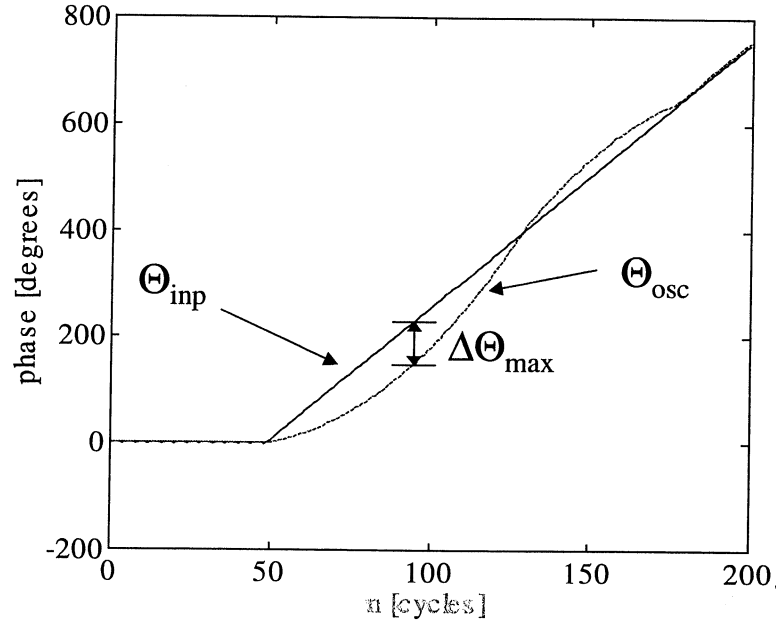


Figure E.1: Response of a bang-bang PLL to a frequency jump.

where f_0 denotes the reference frequency in [Hz]. The excess phase of the VCO after the frequency jump is given by

$$\Theta_{vco} = n \cdot [\Theta_p + \Theta_i/2] + \sum_{k=1}^{n-1} k \cdot \Theta_i, \quad (\text{E.3})$$

Θ_p and Θ_i denoting the change in phase caused by the proportional and integral part of the loop response

$$\Theta_p = 2\pi \frac{\Delta t_p}{T_0} \quad (\text{E.4})$$

$$\Theta_i = 2\pi \frac{\Delta t_i}{T_0} \quad (\text{E.5})$$

The phase difference $\Delta\Theta$ then follows from subtracting (E.3) from (E.1)

$$\Delta\Theta(n) = n \cdot [\Theta_{inp} - \Theta_p] - n^2 \frac{\Theta_i}{2}, \quad (\text{E.6})$$

which has a maximum value at $n = (\Theta_{inp} - \Theta_p)/\Theta_i$, given by

$$\Delta\Theta_{max} = \frac{(\Theta_{inp} - \Theta_p)^2}{2\Theta_i} \quad (\text{E.7})$$

Solving for Θ_{inp} results in

$$\Theta_{inp,max} = \Theta_p + \sqrt{2 \cdot \Theta_{max} \cdot \Theta_i}, \quad (\text{E.8})$$

which corresponds to a maximum deviation in frequency of

$$\Delta f_{max} = \Theta_{inp,max} \cdot \frac{f_0}{2\pi} \quad (\text{E.9})$$

Hence, the higher the values of Θ_p and Θ_i , the higher is the acceptable frequency deviation. As, on the other side, Θ_p and Θ_i should be small for low jitter, there is a tradeoff between jitter and stability. Thus, low jitter can only be achieved if the VCO frequency does not change too much with a variation on the supply voltage.

Appendix F

Transfer Function of Current-Biasing Circuit

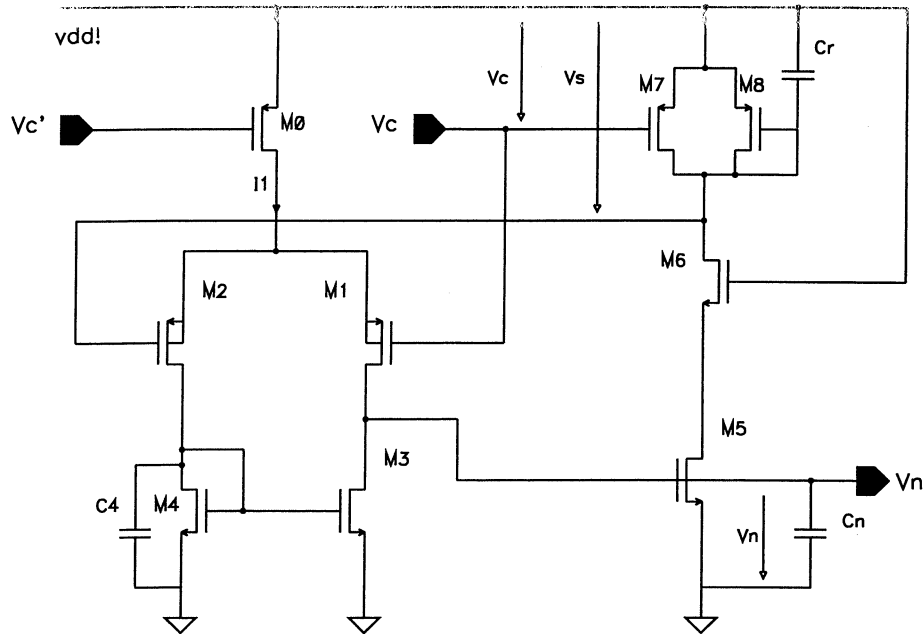


Figure F.1: Replica current biasing circuit with differential amplifier to regulate the voltage swing.

In order to study the stability of the feedback loop in the current biasing circuit, shown on Fig. F.1, we will derive the transfer function of the circuit. Following the analysis in [LAKE-94], the differential amplifier is modeled as a two pole system, having one dominant pole at the output, and one non-dominant pole at the drain of $M4$.

$$f_d = \frac{1}{2\pi R_o C_o}, \quad (F.1)$$

$$f_{nd} = \frac{g_{m4}}{2\pi C_4}, \quad (F.2)$$

with R_o being the output resistance of the differential amplifier, and C_o , C_4 the overall capacitance at the output and on the drain of M4, respectively. R_o results from the output resistances of M1 and M3

$$R_o = r_{ds1} \parallel r_{ds3}. \quad (F.3)$$

Using a simple model, the output resistances of M1 and M3 are defined by the Early-voltages per gate length, V_n and V_p

$$r_{ds1} = \frac{V_p L_1}{(I_1/2)}, \quad (F.4)$$

$$r_{ds3} = \frac{V_n L_3}{(I_1/2)}. \quad (F.5)$$

Hence, R_o can be written as

$$R_o = \frac{V_e}{I_1/2}. \quad (F.6)$$

The output capacitance C_o is determined by the gate capacitance of the five current sources (four in the VCO, one (M5) in the replica cell), resulting in a total capacitance of $3pF$. The capacitance on the node defining the non-dominant pole is given by

$$C_4 = C_{GD2} + C_{DB2} + C_{GS3} + C_{GB3} + C_{GD3} + C_{GS4} + C_{GB4} + C_{DB4},$$

which results in a total capacitance of $60fF$, hence being much smaller than C_o . The small-signal conductance g_{m4} at the non-dominant pole is given by

$$g_{m4} = \sqrt{2 \frac{I_1}{2} K_n \frac{W_4}{L_4}}, \quad (F.7)$$

where I_1 is the bias current of the amplifier, and K_n is the NMOS transconductance parameter in $[A/V^2]$. Note that I_1 is derived as a fraction of the VCO current I_0 ,

$$I_1 = \gamma I_0. \quad (F.8)$$

Hence the location of the poles and zeros of the amplifier are a function of the VCO current, which itself is a function of the VCO frequency. The transfer function of the differential amplifier can now be written as

$$V_n(s) = (V_c(s) - V_s(s)) \frac{A_0(1 + s/\omega_{z1})}{(1 + s/\omega_{p1})(1 + s/\omega_{p2})}, \quad (F.9)$$

with

$$A_0 = 2V_e \sqrt{\frac{2K_p(W_1/L_1)}{\gamma I_0}}, \quad (\text{F.10})$$

$$\omega_{p1} = \frac{1}{C_o} \frac{\gamma I_0/2}{V_e}, \quad (\text{F.11})$$

$$\omega_{p2} = \frac{1}{C_4} \sqrt{\gamma I_0 K_n(W_4/L_4)}, \quad (\text{F.12})$$

$$\omega_{z1} = 2 \cdot \omega_{p2}. \quad (\text{F.13})$$

Here we have used the fact that the nondominant pole acts on only half the signal, which is the same as having a pole at that frequency and a zero at twice that frequency, both operating on the full signal [LAKE-94].

The replica-bias cell constitutes the feedback path of the loop. The transfer function is given by

$$V_s(s) = -V_c(s) \frac{1}{(1 + s/\omega_{p3})} + V_n(s) \frac{\alpha}{(1 + s/\omega_{p3})}, \quad (\text{F.14})$$

with one pole ω_{p3} given by

$$\omega_{p3} = \frac{1}{C_r} \sqrt{I_0 K_p(W_7/L_7)}, \quad (\text{F.15})$$

and DC gain α given by

$$\alpha = \sqrt{\frac{K_n(W_5/L_5)}{K_p(W_6/L_6)}}. \quad (\text{F.16})$$

Combining (F.9) and (F.14) results in the closed loop transfer function

$$H(s) = \frac{V_s(s)}{V_c(s)}, \quad (\text{F.17})$$

given by

$$H(s) = \frac{\alpha A_0(1 + s/\omega_{z1}) - (1 + s/\omega_{p1})(1 + s/\omega_{p2})}{(1 + s/\omega_{p1})(1 + s/\omega_{p2})(1 + s/\omega_{p3}) + \alpha A_0(1 + s/\omega_{z1})}. \quad (\text{F.18})$$

The overall system is third-order, hence, there is a potential instability for high loop gains αA_0 . Figure F.2 shows the position of the poles when varying the loop gain. For very small gains, the positions of the poles correspond to their positions in the open-loop case. Increasing the gain causes poles ω_{p1} , ω_{p3} to become coincident and then to become complex and conjugate. With sufficiently large αA_0 , the complex conjugate poles cross the Imaginary Axis into the right-half plane.

The gain value for the poles to cross the Imaginary axis can be approximated by

$$A_{max} = \frac{2(\omega_{p2} + \omega_{p3})\omega_{z1}}{(\omega_{p2} - \omega_{p3})\omega_{p1}}, \quad (\text{F.19})$$

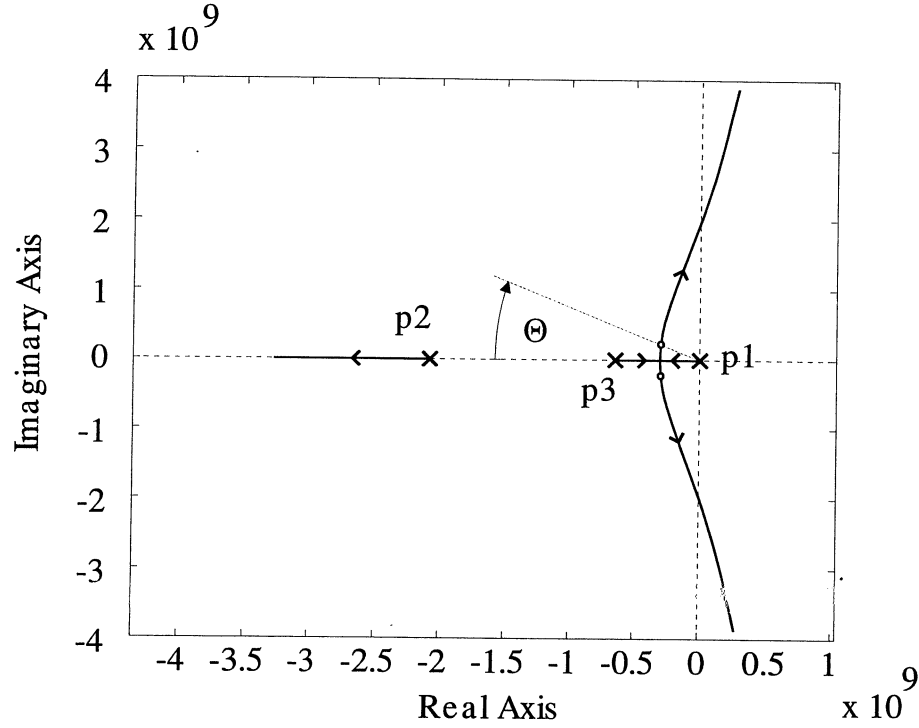


Figure F.2: Root locus plot of the feedback loop. The positions of the open-loop poles $\omega_{p1}, \omega_{p2}, \omega_{p3}$ were chosen for $I_0 = 200\mu A$.

which is a function of the I_0 of the form

$$A_{max} = k_1 / \sqrt{I_0}, \quad (F.20)$$

with k_1 being a constant which can easily be calculated by using (F.11)-(F.13). The actual loop gain αA_0 can also be written in the form of (F.20)

$$\alpha A_0 = k_2 / \sqrt{I_0}, \quad (F.21)$$

where k_2 can be calculated from (F.10) and (F.16). The loop gain αA_0 must be much smaller than A_{max} to guarantee stability. This condition can be written

$$\frac{A_{max}}{\alpha A_0} \gg 1, \quad (F.22)$$

$$\frac{(\omega_{p2} + \omega_{p3})2\omega_{p2}C_o}{(\omega_{p2} - \omega_{p3})g_{m1}} \gg 1. \quad (F.23)$$

Since all the product terms are of the form $k\sqrt{I_0}$, the gain margin $A_{max}/\alpha A_0$ does not depend on the actual value of I_0 . It follows from Fig. F.2 that, since the the pole at ω_{p2}

	$I_0 = 200\mu A$	$I_0 = 2\mu A$
GBW	$16.8 \cdot 10^6$	$1.68 \cdot 10^6$
ω_{p1}	$1.17 \cdot 10^6$	$11.7 \cdot 10^3$
ω_{p2}	$2.07 \cdot 10^9$	$0.21 \cdot 10^9$
ω_{p3}	$650 \cdot 10^6$	$64.7 \cdot 10^6$
ω_{z1}	$4.14 \cdot 10^9$	$0.41 \cdot 10^9$
αA_0	191.7	1917
$A_{max}/(\alpha A_0)$	35.35	35.35
ζ	0.8	0.8

Table F.1: Actual values of control loop parameters.

is located at a considerable distance from the imaginary axis, the system is essentially a two pole system, with poles defined by ω_{p1} and ω_{p3} . For such system the damping constant ζ is defined as

$$\zeta = \cos \Theta, \quad (\text{F.24})$$

where Θ is the angle of the polar angle of the complex pole location. The gain of the amplifier was now adjusted by changing γ and W_1/L_1 such that the damping factor ζ was at least $1/\sqrt{2}$ in order to achieve a reasonable stable system and a fast response. MATLAB simulations showed that ζ was nearly independent of I_0 . Using the actual device parameters, shown in Table F.1, then resulted in $G_0/(\alpha A_0)$ of 35.36 for the nominal case, allowing a large enough gain margin to assure stability.

Appendix G

Layouts

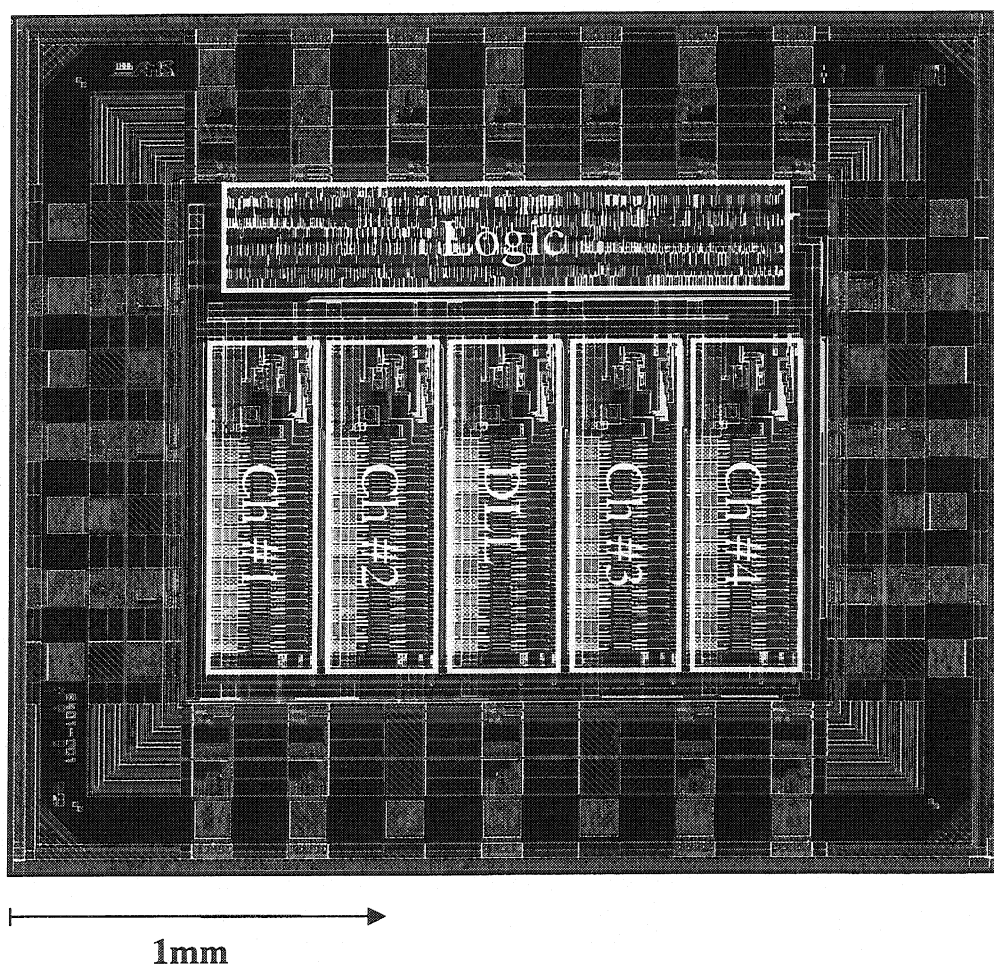


Figure G.1: Layout of the delay-generation ASIC (standard $0.8\mu m$ technology). The delay-locked loop (DLL) in the center is surrounded by slave-delaylines with identical layout.

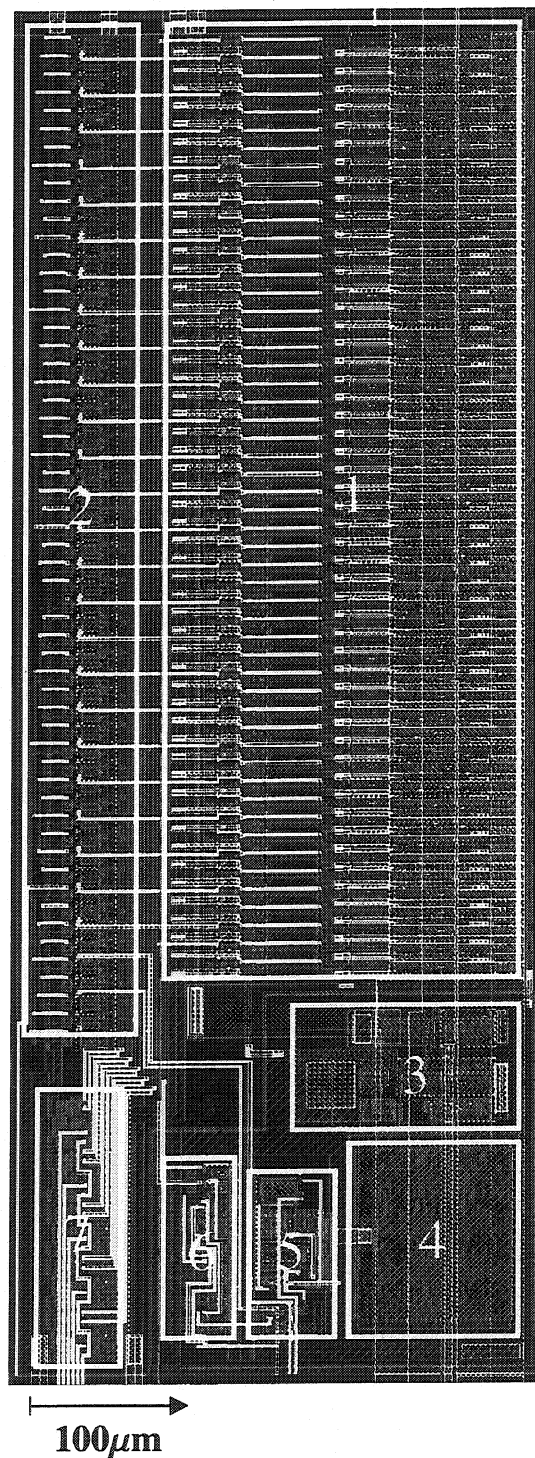


Figure G.2: Layout of the delay-locked loop. Delayline (1) with current-starved inverter cells, multiplexer (2), V_c/V_{cnp} -converter circuit (3), loop filter capacitance (4), charge pump (5), phase detector (6), 5-bit delay register (7).

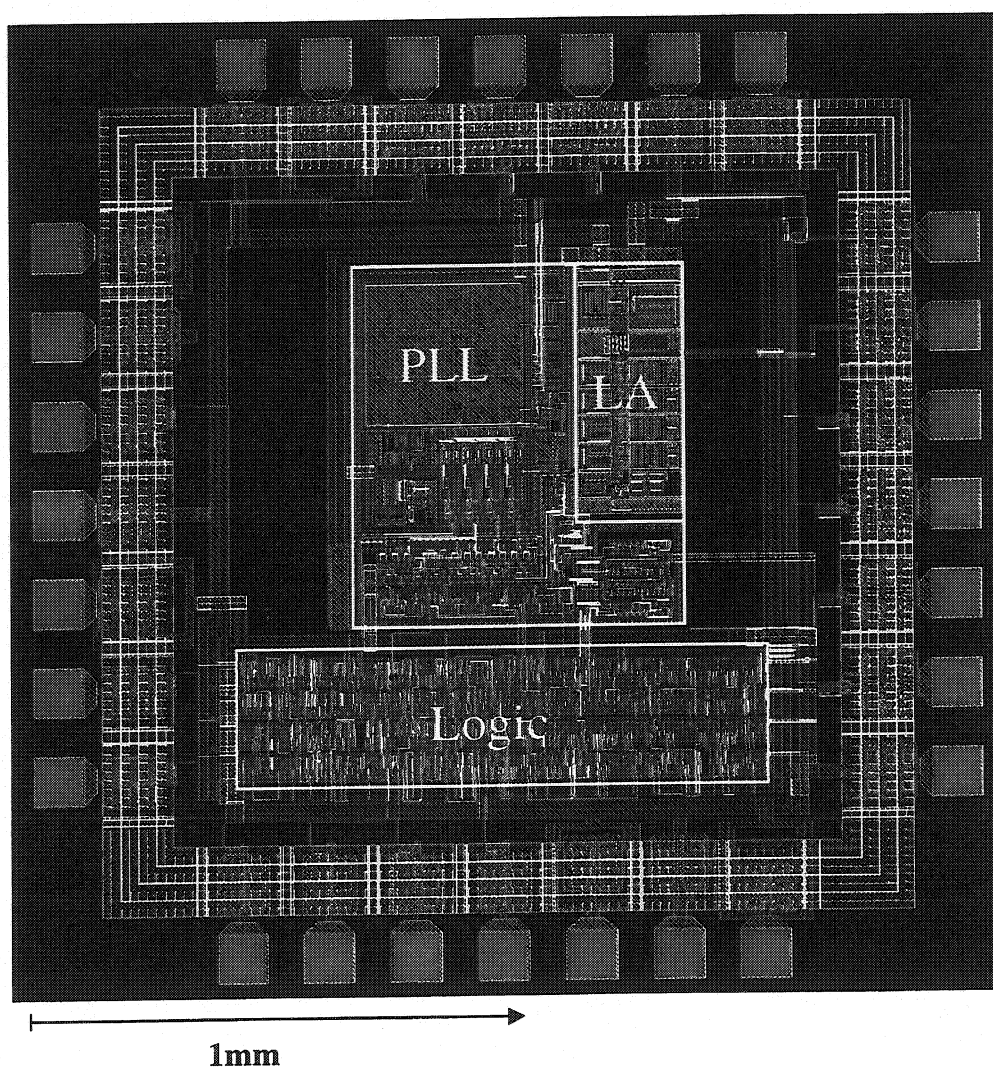


Figure G.3: Layout of the radiation-hard clock-and data recovery circuit. ($0.8\mu\text{m}$ DMILL technology.) The circuit consists of a Phase-locked loop (PLL) and a Limiting Amplifier (LA).

Decoupling Cap.

2 Clock phase shifters

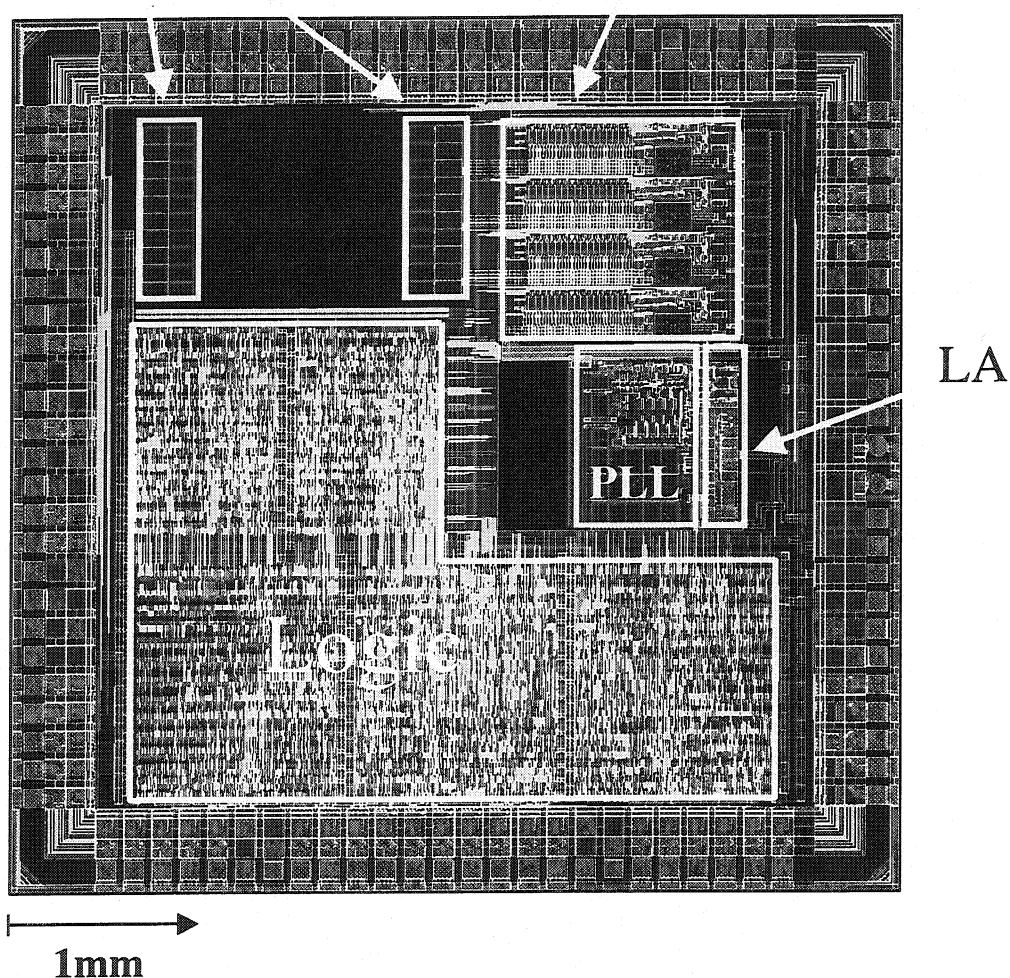


Figure G.4: Layout of the Timing, Trigger and Control Receiver (TTCrx) ASIC. (Non-radiation-hard $0.8\mu\text{m}$ technology.) The 2 clock-phase shifters comprising 4 delay-locked loops (DLL) are shown in the upper right corner, the clock-and data recovery part (PLL and Limiting Amplifier) is situated right below.

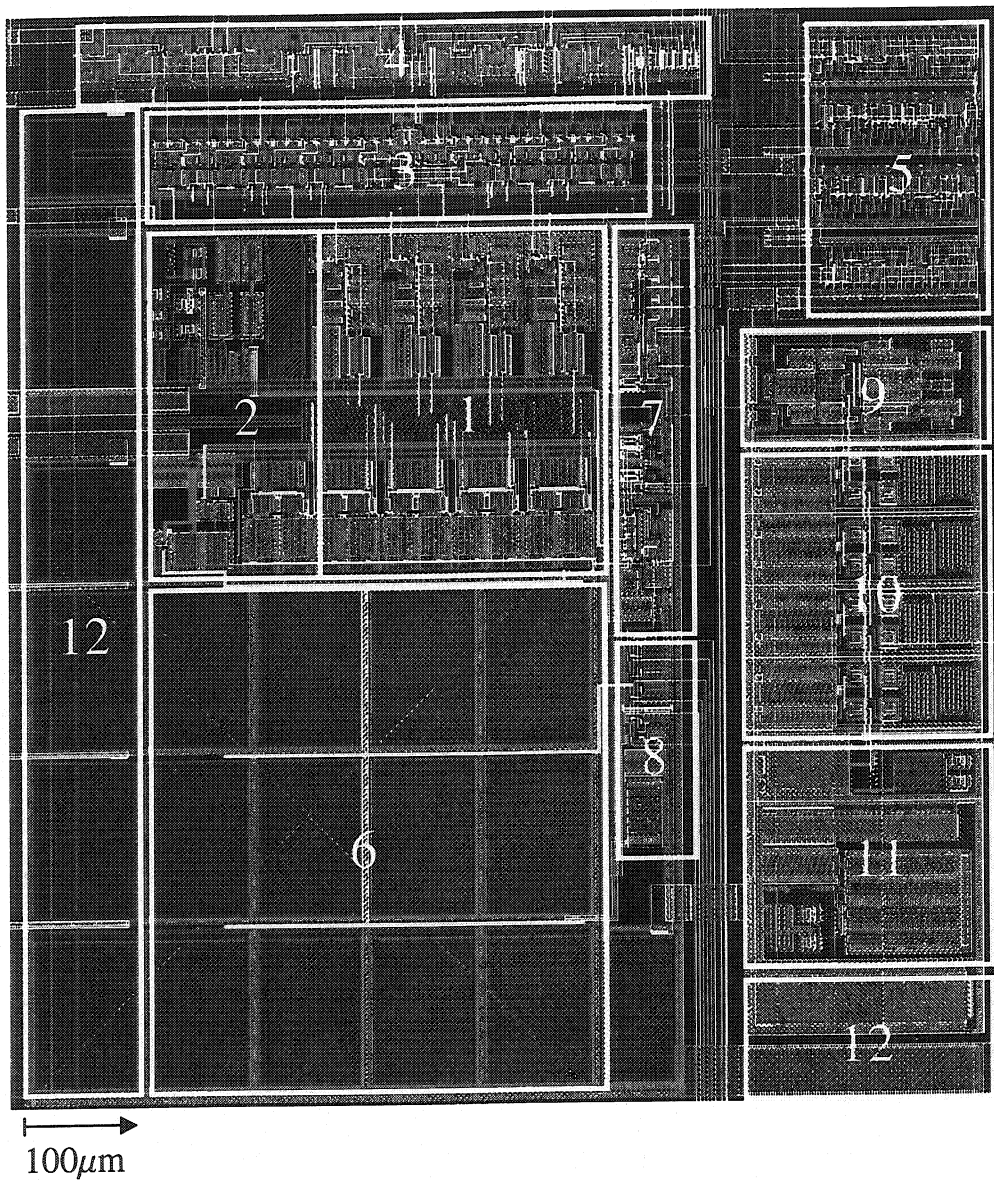


Figure G.5: Layout of the clock-and data recovery circuit. Voltage-controlled oscillator (1), replica current biasing circuit (2), phase-detector frontend (3), phase detector state-machine (4), frequency detector (5), loop filter (6), charge pump (7), $V_c - V_t$ extraction circuit (8), Limiting Amplifier (LA) differential-to-CMOS level converter (9), 4 LA gain stages (10), LA bias (11), decoupling capacitances (12).

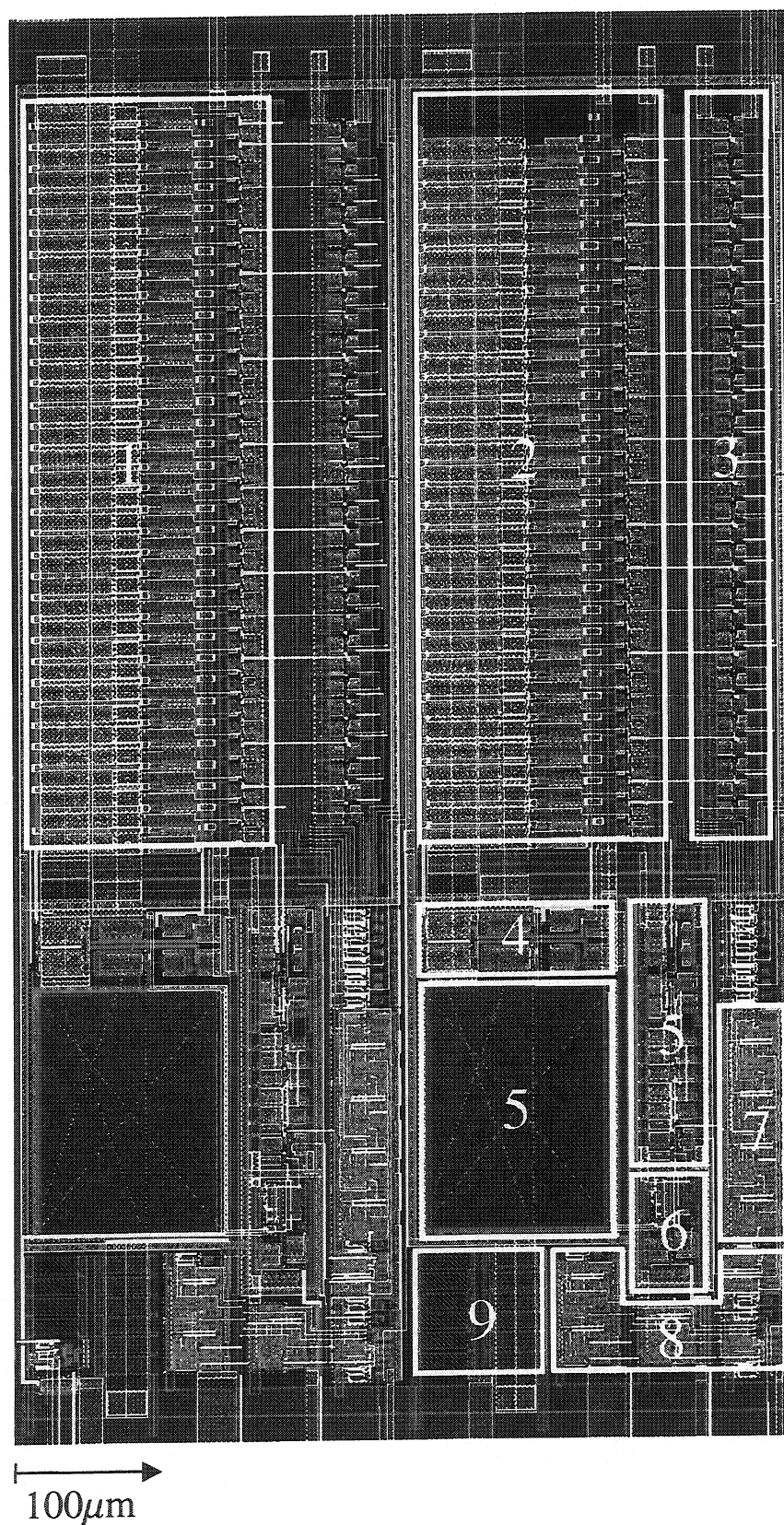


Figure G.6: Layout of high-resolution clock phase shifter. 16-stage delayline (1), 15-stage delayline (2), multiplexer (3), V_c/V_{cnp} -converter (4), Loop filter capacitance (5), charge pump (6), delay register (7), initialisation logic (8), decoupling capacitances (9).

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Vita

Thomas Toifl was born in Hollabrunn, Austria, in 1970. He won a first prize at the Austrian Young Scientist Award competition at the age of sixteen. In 1989 he started his studies of Electrical Engineering at the Vienna University of Technology, Austria, specialising in the field of Telecommunications Engineering. In 1993 he won a scholarship for a one year exchange program with the University of Illinois at Urbana-Champaign. There he became interested in Image Processing and Computer Vision after taking classes from Prof. Thomas Huang and Prof. Michael Orchard. Back in Austria, he received a Kurt Gödel Scholarship, which allowed him to spend seven months with the Image Processing department of the Ecole Supérieure des Télécommunications (ENST), Paris, France. Supervised by Prof. Henri Maître, he there wrote his master's thesis about color perception in fine art paintings. In December 1995, he received his "Diplom-Ingenieur" (M.S.) degree with highest honors (grade point average in both state examinations 5.0/5.0). During his studies he also held internship positions at IBM, Vienna, Austria, and Deutsche Aerospace (DASA), München, Germany.

After graduation, he decided to specialise in the field of chip design. In July 1996, he joined the microelectronics group of the European Laboratory for Particle Physics (CERN), Geneva, Switzerland, and entered the Ph.D. program at the Vienna University of Technology with thesis supervisors Prof. Franz Seifert and Prof. Christian Fabjan. At CERN, he got involved in the development of mixed digital-analog circuits for the synchronisation of particle detectors, which resulted in this work.

In the future, he intends to pursue a combined career in industry and academic research.

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