

Pixel-Strip Modules for the CMS Tracker Phase-2 Upgrade

From DAQ test system development to module
assembly and qualification

DISSERTATION

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*For my dear friend and colleague
Nicolas Tonon (1993 - 2021)
who left us too soon*

Abstract

The Large Hadron Collider (LHC) will undergo a major “High Luminosity” upgrade with the goal of delivering a peak instantaneous luminosity of $5 - 7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ by 2029. In order for the CMS experiment to cope with the higher radiation levels and data rates, the current CMS Silicon Tracker will be replaced. In particular, the outer part of the Tracker, referred to as the Outer Tracker, will introduce a new module concept, made of two vertically stacked silicon sensors. It will exploit the strong magnetic field inside the CMS detector to perform an on-module transverse momentum (p_T) discrimination, detecting high p_T particles locally and sending the corresponding information, referred to as *stubs*, to the CMS Level-1 Trigger system.

This thesis focuses on one of the two foreseen module designs, namely the Pixel-Strip (PS) module. The module is made of a $10 \times 5 \text{ cm}^2$ strip sensor, with 2.5 cm long strips and 100 μm pitch, stacked on top of a macro pixel sensor with $1467 \times 100 \mu\text{m}$ macro pixels bump-bonded to macro pixel ASICs. The latter are of particular importance as they implement the logic for the on-module p_T discrimination. The sensor stack is surrounded by peripheral front-end, readout and power hybrid circuits. The front-end hybrids host the strip sensor ASICs and a data concentration ASIC. The readout hybrid handles the control of the front-end ASICs and the bi-directional optical data communication with the back-end system. Finally, the power hybrid ensures power distribution to all the front-end electronic components.

The presented work describes the latest developments with respect to three main aspects: the PS module assembly, the module production test systems, and the PS module qualification. On the one hand, the module assembly relies on a semi-automated procedure capable of fulfilling the high precision requirements of the sensor-to-sensor alignment. On the other hand, the development of the production test systems is driven by the core principle of versatility, flexibility and high throughput such that they are able to support the qualification of the wide range of hybrid circuits and module types. As far as performance studies are concerned, the preliminary laboratory qualification of the latest assembled prototype PS modules demonstrates the electrical integrity of the readout chain but still yields a relatively high electronic noise affecting the strip sensor. Nevertheless, test-beam qualification of a prototype module shows excellent performance with cluster efficiencies above 99% for the strip sensor and 98% for the pixel sensor. Finally, the test-beam qualification demonstrates the p_T discrimination capabilities of the module, yielding stub efficiencies above 98%.

Zusammenfassung

Der Large Hadron Collider (LHC) wird einer umfassenden "High Luminosity"-Aufrüstung unterzogen, um bis 2029 eine maximale instantane Luminosität von $5 - 7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ zu erreichen. Damit das CMS-Experiment mit der höheren Strahlenbelastung und Datenrate stand hält, wird der derzeitige CMS-Silizium-Spurdetektor ersetzt. Insbesondere im äußeren Teil des Spurdetektors, dem so genannten Outer Tracker, wird ein neues Modulkonzept eingeführt, das aus zwei vertikal gestapelten Siliziumsensoren besteht. Hierzu wird das starke Magnetfeld im Inneren des CMS-Detektors ausgenutzt, um Teilchen mit hohem Transversalimpuls bereits auf dem Modul zu erkennen. Die entsprechenden Informationen, die als *stubs* bezeichnet werden, werden an das CMS Level-1-Trigger-System übermittelt.

Diese Arbeit konzentriert sich auf eines der beiden vorgesehenen Moduldesigns, nämlich das Pixel-Strip (PS) Modul. Das Modul besteht aus einem $10 \times 5 \text{ cm}^2$ Streifensensor mit 2,5 cm langen Streifen und 100 μm Streifenabstand, der einem Abstand von wenigen Millimetern auf einen Makropixelsensor mit $1467 \times 100 \mu\text{m}$ Makropixeln geklebt ist. Die Makropixel sind mit kleinen Lotkugeln mit dem Auslesechip verbunden. Diese sind von besonderer Bedeutung, da sie die Logik für die Impulsmessung auf dem Modul implementieren. Die beiden Sensoren sind von peripheren Front-End-, Auslese- und Leistungshybridschaltungen umgeben. Die Front-End-Hybridschaltungen tragen die Streifensensor ASICs und eine Datenkonzentration ASIC. Der Auslesehybrid übernimmt die Steuerung der Front-End-ASICs und die bidirektionale optische Datenkommunikation mit dem Back-End-System. Der Stromversorgungs-Hybrid schließlich sorgt für die Spannungsversorgung aller elektronischen Komponenten des Moduls.

Die vorliegende Arbeit beschreibt die neuesten Entwicklungen in Bezug auf drei Hauptaspekte: die Modulmontage, die Testsysteme für die Modulproduktion und die Modulqualifizierung. Die Modulmontage beruht auf einem halbautomatischen Verfahren, das die hohen Präzisionsanforderungen der Sensor-zu-Sensor-Ausrichtung erfüllen kann. Die Entwicklung der Produktionstestsysteme wird durch das Kernprinzip der Vielseitigkeit, der Flexibilität und des hohen Durchsatzes vorangetrieben, so dass sie die Qualifizierung einer breiten Palette von Hybridschaltungen und Modultypen unterstützen können. Was die Leistungsstudien anbelangt, so hat die vorläufige Laborqualifizierung der neuesten Prototyp-Module die elektrische Integrität der Auslekette gezeigt, aber immer noch ein relativ hohes elektronisches Rauschen ergeben, das den Streifensensor beeinträchtigt. Dennoch zeigt die Teststrahlqualifizierung eines Prototypmoduls eine hervorragende Leistung mit Cluster-Effizienzen über 99% für den Streifensensor und 98% für den Pixelsensor. Schließlich demonstriert die Teststrahlqualifizierung die Fähigkeit des Moduls Teilchen anhand ihres Transversalimpulses zu unterscheiden, wobei Stub-Effizienzen von über 98% erzielt werden.

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CHAPTER 1

INTRODUCTION

Starting from 2029, the Large Hadron Collider (LHC) at CERN will enter the last phase of its era with the so-called High Luminosity (HL-LHC) phase where major improvements to the accelerators are foreseen. These will bring the collider performance to unprecedented levels of instantaneous luminosity, with an expected peak reaching $5 \text{ to } 7 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ at a center mass energy of 14 TeV. The HL-LHC era will then span over 10 years and reach in the ultimate scenario luminosities of 4000 fb^{-1} with the main objective of improving studies of known particle physics processes but also extending the potential for the discovery of processes beyond the Standard Model. Chapter 2 provides a global overview of the LHC research focus and the prospects of the upcoming HL-LHC era.

As a result of the increase in luminosity, the four main experiments located around the LHC, namely ATLAS, CMS, ALICE and LHCb will have to face a very challenging experimental environment that includes a higher number of overlapping collisions (pileup), a harsher radiation environment and higher data rates. Therefore, in order to cope with these unprecedented experimental conditions, the CMS experiment will undergo major improvements of all the detector subsystems, in particular the Silicon Tracker, in a so-called Phase-2 Upgrade. As described in Chapter 4, the new Tracker will feature a substantial increase in the number of readout channels, an improved granularity and spatial resolution, and a better pseudo-rapidity coverage. In addition, in order to improve the pileup mitigation, the outer part of the Tracker, or what is referred to as the Outer Tracker, will directly contribute to the CMS Level-1 Trigger. This will be achieved by the introduction of a novel concept of on-module transverse momentum (p_T) discrimination that will ex-

exploit the strong magnetic field inside the CMS detector to select only high p_T particles. Outer Tracker modules will be able to generate trigger primitives corresponding to the high p_T particles and forward them to the Level-1 Trigger where they will be used for the reconstruction of the particle trajectories and contribute to the trigger decision. While the Outer Tracker will introduce two types of modules implementing this novel concept, this thesis mainly focuses on one of them, namely the Pixel-Strip (PS) module.

An introduction to the basic principles of silicon tracking detectors is given in Chapter 4 and a detailed description of the PS module design is presented in Chapter 5. The remaining chapters focus on three core aspects related to the PS module and to which I have actively contributed: the module assembly procedure, the module production test systems, and the module qualification. In Chapter 6 the semi-automated assembly procedure developed at the Deutsches Elektronen-Synchrotron (DESY) laboratory is described. It was extensively used in the context of this thesis in order to build the very first PS prototype modules. In addition, Chapter 7 introduces the various test systems developed for the purpose of qualifying the Outer Tracker modules and to which I have extensively contributed, with a focus on the developments dedicated to the PS module. In particular, I have been one of the main developers of the μ DTC firmware and the Ph2ACF software needed for the module qualification during both the prototyping and production phases. Finally, the qualification of the individual PS module components and the early prototype modules assembled at DESY are discussed in Chapters 8 and 9. It provides the latest qualification procedures developed for the PS module hybrid circuits and the fully functional modules, complemented by performance studies both in the laboratory and during test-beam campaigns. My work mainly focused on the development of test procedures dedicated to the ROH circuit characterization, the PS module laboratory qualification and the test-beam performance studies. This thesis therefore provides the first global overview of the various efforts deployed to bring the PS module from its conceptual design to the production, qualification and performance studies of its early prototypes.

CHAPTER 2

PARTICLE PHYSICS AT THE LHC

2.1 Standard Model of Particle Physics

Particle physics is at the heart of our understanding of the universe and the Standard Model (SM) is the most successful particle physics theory so far. It describes the elementary particles in the universe as well as their interactions and provides a unified mathematical description of three out of four of nature's fundamental forces: the electromagnetic force, the weak force, and the strong force. The description of the electromagnetic and weak forces can be unified under the electroweak model, while the strong force is described by Quantum Chromodynamics (QCD). A further unification of the electroweak and the strong forces could take place at a higher energy range than is currently accessible.

Another building block of this model is a theory combining quantum mechanics and special relativity, called Quantum Field Theory (QFT). The latter describes fundamental matter interaction by the exchange of field quanta. Through an interplay of nature's fundamental symmetries, each fundamental interaction is mediated by corresponding field quanta or what are referred to as bosons of the SM. However, due to the high number of free parameters in the SM and its inability to answer some open questions particle physicists face today, understanding the Universe is bound to face either further model extensions or undergo a radical paradigm shift. Up to the present day, the SM has been validated by all current experimental data and represents one of the triumphs of modern physics. The theoretical and experimental foundations of this model are described in great details in [1, 2].

The elementary particles and the mediators of the fundamental forces described by the SM are depicted in Figure 2.1. Two groups of particles can be distinguished: *fermions* and *bosons*. The fermions, divided into two categories, namely *quarks* and *leptons*, are considered the fundamental constituents of matter. The bosons correspond either to the force mediators or carriers referred to as gauge bosons, or the Higgs boson that gives mass to the particles. The mediator of the gravitational force, the graviton, remains hypothetical and undescribed by the SM.

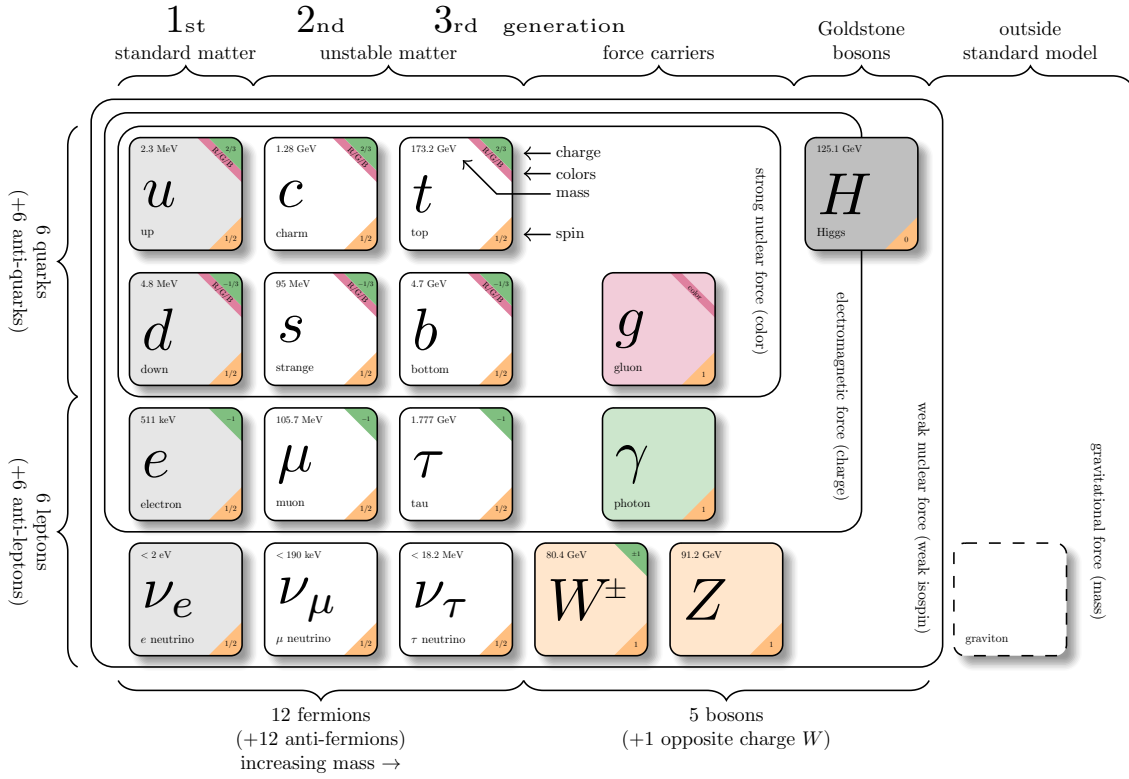


Figure 2.1: The Standard Model of particle physics' elementary particles and mediators of the fundamental interactions [3]. Each of the three first columns represents one generation of elementary particles, with the first one forming the constituents of the known universe. The fourth column represents the force carriers, namely the gluons (red), the photon (green) and the W and Z bosons (orange). The Higgs boson is indicated in the fifth column in dark grey. Finally, the graviton remains undescribed by the Standard Model.

Fermions

Fermions are divided into two categories: quarks and leptons, each containing six elements with a spin of $1/2$. In the group of quarks, the *up*, *charm* and *top* quarks have a fractional electrical charge of $2/3$ while the *down*, *strange* and *bottom* quarks have a fractional electrical charge of $-1/3$. In addition, through the theory of QCD, all quarks are assigned an additional quantum number called *color*, with three possible colors or anti-colors [4]. Due to the confinement principle, quarks cannot be observed isolated but only in bound states, called hadrons, which are colorless. Hadrons are composite particles made of two or more quarks held together by the strong interaction. An example of a hadron is the proton which consists of two up-quarks and one down-quark (uud). The group of leptons consists of the *electron* (e), the *muon* (μ), the *tau* (τ) and their corresponding *neutrinos* (ν_e, ν_μ, ν_τ). These leptons hold an integer electrical charge of -1 (e, μ, τ) or 0 (neutrinos), and no color.

Quarks and leptons are further grouped into three generations. The up quark, down quark, electron and electron neutrino are known collectively as the first generation. They represent the building blocks of the known universe. The two remaining generations, which are essentially heavier copies of the first generation, are only observed at higher energy scales, such as those reached in particle colliders.

Finally, to each of the listed fermions, there exist an anti-fermion (anti-particle), a particle with equal mass but opposite charge. These anti-fermions can form bound states made of anti-quarks. An example of these bound states is the anti-proton which is made of two anti-up quarks and one anti-down quark. ($\bar{u}\bar{u}\bar{d}$).

Bosons

In the group of gauge bosons, the gluon is the mediator of the strong interaction. It is massless, has color and only interacts with colored particles, hence it couples to quarks and to other gluons (self-coupling). The photon is the mediator of the electromagnetic interaction. It is massless, has no charge and couples to all charged particles as described by the Quantum Electrodynamics (QED) theory [5]. Finally, the $W^\pm$ bosons and the Z boson are the mediators of the weak interaction. They both have mass, couple to all fermions and can manifest self-coupling as well.

The Higgs boson is not a mediator of any fundamental interaction but is at the origin of the W and Z bosons masses. In addition, it couples to all massive particles with a coupling strength being proportional to the particle's mass and hence defining it. It was predicted in 1964 by Robert Brout and François Englert, Peter Higgs, and Gerald Guralnik, Carl Richard Hagen, and Tom Kibble through the elaboration of the spontaneous symmetry breaking mechanism [6–8]. The three independent publications, through different approaches, brought a solution to the standing problem of mass in local gauge theories. The Higgs boson was further discovered in 2012 by the CMS and ATLAS experiments at the LHC [9, 10] and earned François Englert and Peter Higgs the 2013 Nobel Prize in physics.

Despite all the success of the Standard Model, it still remains incapable of describing or explaining some aspects of nature's laws. While three fundamental interactions are well integrated into the model, gravitation still is not. Furthermore, there remain open questions concerning the contradiction between the theoretically predicted massless neutrinos, and the current experimental observations of neutrino oscillations that reveal a non-zero mass. Also, if the particles in the SM account for all the observed matter in the universe, they do not explain the existence of dark matter and dark energy that are observed to influence the dynamics of galaxies and the expansion of the universe, respectively. Such open questions yield a large amount of additional or alternative theoretical models.

The most famous model extension to the current SM is Supersymmetry [11]. At the core of it, the supersymmetric model predicts a partner particle for each particle of the SM, and thus solves major unresolved problems such as the hierarchy problem [12]. However no experimental observation was yet made to validate this model. Nevertheless, particle colliders, such as the Large Hadron Collider (LHC) at CERN, remain the most promising experimental endeavours for new discoveries.

2.2 The Large Hadron Collider

Operated by the European Organisation for Nuclear Research (CERN), the Large Hadron Collider (LHC) is the largest and most powerful particle accelerator in the world. It is also the largest scientific instrument ever built by mankind and is located 100 meters beneath the French-Swiss border in the Geneva region. With a circumference of 27 kilometers, it was constructed in an underground tunnel initially excavated for the LHC's predecessor, the Large Electron Positron (LEP) collider. After the decision was taken in 1984 to build the accelerator, construction spanned over ten years, from 1998 until 2008 when operation began. However, it only lasted nine days before being prematurely stopped

due to a magnet quench which damaged many of the superconducting dipole magnets. A year later, the damage was repaired and operation was restarted in November 2009. The current collider uses a complex of accelerators, shown in Figure 2.2, to bring protons or heavy ions to ultimate target energies of 7 TeV or 2.76 TeV, respectively.

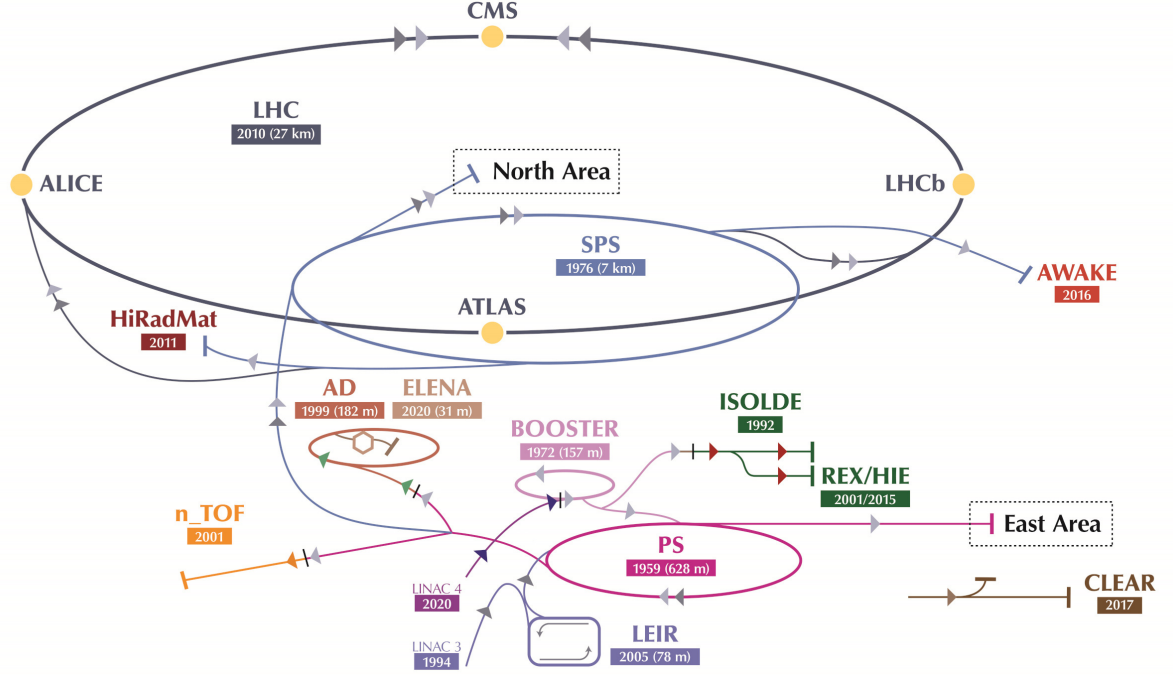


Figure 2.2: Schematic of the CERN accelerator complex. Particles undergo a series of accelerations performed at different stages of the complex, from the nucleon source, through linear accelerators and boosting rings, ending with the nominal energy reached in the LHC storage ring [13].

In the case of protons, the Linear accelerator 4 (LINAC4) is the source of proton beams. It accelerates protons up to an energy of 160 MeV prior to injection into the Proton Synchrotron Booster (BOOSTER). During injection from LINAC4 to the BOOSTER, the anions are stripped of their electrons, leaving only protons. Inside the BOOSTER, protons are accelerated to 2 GeV and injected into the Proton Synchrotron (PS). In the PS, the energy is further increased to 26 GeV and the protons are forwarded to the Super Proton Synchrotron (SPS) where they are accelerated to an energy of 450 GeV. Finally, they are formed into two proton beams transferred to two separate beam pipes inside the LHC where protons are accelerated up to the current target energy of 6.8 TeV. This target energy is the result of many improvements and extensions that brought it from 4 TeV during the so-called LHC Run 1, up to 6.5 TeV during the Run 2, and finally 6.8 TeV during the ongoing Run 3.

In the case of heavy ions, they are extracted from a source of vaporised lead, go through the Linear accelerator 3 (LINAC3) before being accelerated in the Low Energy Ion Ring (LEIR). Finally, starting from the LEIR, the heavy ions follow the same path as previously described for the protons, going through the PS until the LHC storage ring, where the target energy of 2.76 TeV is reached.

For both protons and heavy ions, the two beams are circulating in opposite directions and accelerated to their target energy by a series of 16 superconducting radio frequency cavities. They are focused by 392 quadrupole magnets and kept in a circular trajectory by 1,232 superconducting dipole magnets, which produce a magnetic field of 8.33 Tesla. The whole LHC ring is kept at an operating temperature of 1.9 Kelvin using almost 100 tons of superfluid helium. This especially ensures the superconductivity of the niobium-titanium (Nb-Ti) magnets and thus achieves high magnetic fields necessary to keep the beams circulating at the nominal energy.

While the LHC hosts multiple experimental points all around the accelerator complex, the beams are brought into collision at four main interaction points around the accelerator, where four large experiments are located: CMS (Compact Muon Solenoid), ATLAS (A Toroidal LHC Apparatus), ALICE (A Large Ion Collider Experiment) and LHCb (Large Hadron Collider beauty). After reaching center mass of energy of 8 TeV during Run 1 and 13 TeV during Run 2, the current Run 3 operation provides a center mass of energy of 13.6 TeV. These collisions induce high energy proton-proton interactions which can lead to the production of new particles that can be detected and studied by the four experiments.

The CMS and ATLAS experiments, located at the collision points 5 (P5) and 1 (P1), respectively, are two multi-purpose experiments. They are designed and built independently to cover a broad range of physics processes and studies, with a focus on the Higgs boson that was discovered by the two collaborations in 2012, and search for new physics. On the other hand, ALICE and LHCb are specialized experiments which are designed to study particular physics processes. ALICE is optimized for the study of heavy ion collisions, with a focus on studies of the quark-gluon plasma, a state of matter obtained when heavy nuclei collide at high energy. LHCb is designed for the study of particles affected by the strong and weak forces, in particular quarks and leptons, with a focus on the b-quark.

In each of these experiments, the number of possible interactions per time and per area quantified by the cross section σ is defined by the *luminosity* $\mathcal{L}$, such as

$$\dot{N} = \mathcal{L} \cdot \sigma \quad (2.1)$$

where $\dot{N}$ is the number of observed events, $\mathcal{L}$ the luminosity and σ the process cross section. Therefore, luminosity is a number that quantifies the ability of an accelerator to produce a number of particle interactions and thus physics processes. The design luminosity of the LHC is $10^{34} \text{ cm}^{-2}\text{s}^{-1}$ which is necessary for the production and study of rare processes. It is achieved by dividing the proton beam into 2,808 bunches of 1.15×10^{11} protons in each bunch, colliding at a rate of 40 MHz [14]. For a Gaussian beam profile, the luminosity can be written as [15]:

$$\mathcal{L} = \frac{N_b^2 n f_t \gamma}{4\pi \epsilon_n \beta^*} \quad (2.2)$$

where N_b is the number of particles per bunch, n the number of bunches per beam, f_t the revolution frequency of a bunch, γ the relativistic factor, ϵ_n the normalised transverse emittance of the beam, and β^* the beta function at the collision point.

The luminosity can be achieved by optimizing these various operating parameters and its nominal value can even be exceeded. Table 2.1 summarizes the key LHC parameters in proton-proton and heavy-ion modes. At the end of the Run 2 in 2018, the LHC was capable of reaching a proton beam energy of 6.5 TeV, close to the designed 7 TeV, and a peak instantaneous luminosity of $2.1 \cdot 10^{34} \text{ cm}^{-2}\text{s}^{-1}$, that exceeds the design value by more than a factor of two. The latter was only possible thanks to major improvements to the LHC injection chain magnets. With the Run 3, the prospects were even greater with an objective to reach the design performance of the accelerator that was achieved by recording unprecedented collisions at a center of mass energy of 13.6 TeV.

Parameter	Symbol	Unit	p-p Injection	p-p Collision	HI Collision
Nucleon energy	E	[TeV]	0.45	7	2.76
Dipole field	B	[Tesla]	0.53	8.33	8.33
Peak luminosity	L	$[\text{cm}^{-2}\text{s}^{-1}]$	-	10^{34}	10^{27}
Number of bunches			2808		592
Nucleons per bunch	n		1.15×10^{11}		7×10^7
Beam current	I	[A]	0.582		
Beam energy	E_{beam}	[MJ]	23.3	362	

Table 2.1: LHC design parameters [14]

2.3 The Compact Muon Solenoid Experiment

The Compact Muon Solenoid (CMS), shown in Figure 2.3, is one of the four large experiments at the LHC. It is located at Point 5 of the LHC accelerator, in a cavern excavated 100 meters underground. As mentioned earlier, it is a multi-purpose experiment using a large and compact detector in comparison to the other multi-purpose experiment ATLAS, based on a much larger detector in overall volume. The two independent experiments, with same abilities but different detector designs, are meant for cross validation of potential new discoveries.

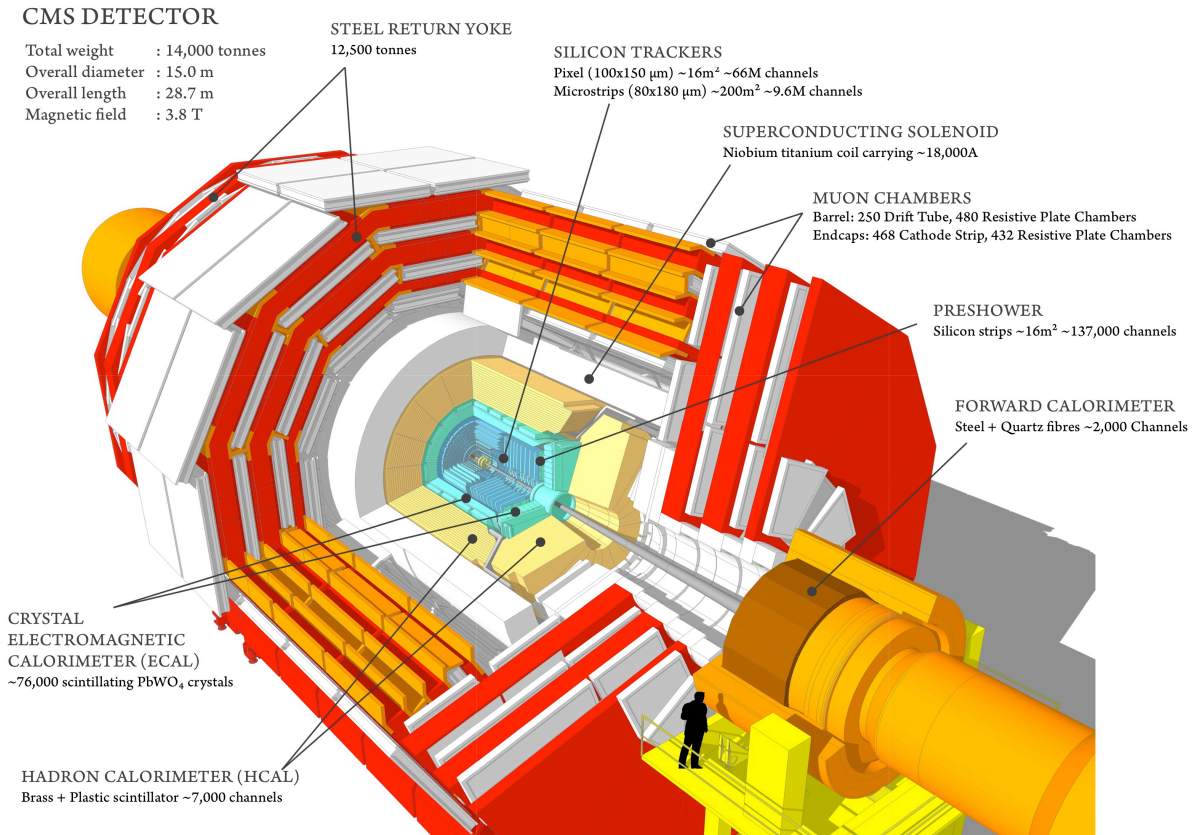


Figure 2.3: Sectional view of the CMS detector. From the inside to the outside, the detector consists of the silicon tracker, the electromagnetic calorimeter, the hadronic calorimeter, the solenoid and the muon chambers inside a steel return yoke. [16]

The CMS detector has a cylindrical shape, measures 21 meters in length, 15 meters in diameter and weighs about 14,000 tons, which makes it a very compact object - as the name suggests. One of the core parts of the detector is the powerful solenoid magnet capable of delivering a magnetic field of 3.8 T. The rest of the detector features several subsystems arranged in multiple layers around the collision point of the beams. Each

of the subsystems plays a role in the chain of particle detection and identification, from trajectory reconstruction to energy measurement. Besides the cylindrical parts of the detector, often called *barrels*, detector closure is achieved at both ends by means of so-called *endcaps*. This way, a large fraction of the 4π solid angle around the interaction point is covered to maximize the number of detected particles.

Figure 2.3 shows a sectional view of the CMS detector, all the subsystems and their corresponding detection technologies. The central part of the detector is made of the silicon pixel and strip tracker layers that allow the reconstruction of charged particles trajectories. Surrounding the tracker, the scintillator-based electromagnetic and hadronic calorimeters serve as instruments for the measurement of particles energy. The Niobium-Titanium superconducting solenoid delivers the magnetic field needed for the measurement of the momentum of charged particles. Finally, in the outermost part of the detector, muon chambers made of drift tubes, cathode strips, and resistive plates are dedicated to the detection of muons.

The CMS experiment is motivated by the large physics program pursued by the collaboration, with a special focus on Higgs physics and searches for new physics beyond the Standard Model. This program is supported by precise detector designs, as described in the following sections and strict specifications and performance requirements thoroughly described in [17]:

- Good muon identification and momentum resolution, good dimuon mass resolution ($\approx 1\%$ at $100 \text{ GeV}/c^2$) and unambiguous muon charge determination for momenta $< 1 \text{ TeV}/c$.
- Good charged particle momentum resolution and reconstruction efficiency in the tracker. Efficient triggering and offline tagging of τ leptons and b-jets.
- Good electromagnetic energy resolution, good diphoton and dielectron mass resolution ($\approx 1\%$ at $100 \text{ GeV}/c^2$), and good hermiticity.
- Good E_{miss}^T and dijet-mass resolution, requiring hadron calorimeters with a large geometric coverage ($|\eta| < 5$) and fine lateral segmentation ($\Delta\eta \times \Delta\phi < 0.1 \times 0.1$).

The CMS vertex reference coordinate system is defined such that the x-axis points towards the center of the LHC, the y-axis towards the top of the CMS detector, and thus the z axis points clockwise along the beam axis. In addition, to express angular coordinates with respect to the beam axis, the so-called *pseudo-rapidity* denoted by $\eta = -\ln(\tan(\theta/2))$

is used. The benefit of using pseudo-rapidity over the polar angle is that it is more closely related to the rapidity of the particle, where the difference in rapidity is a quantity that is invariant under longitudinal boosts (boosts along the beam axis) in a Lorentz frame. This makes the difference in pseudo-rapidity itself a Lorentz invariant quantity for highly energetic particles.

2.3.1 The Silicon Tracker

The silicon Tracker reconstructs the trajectories and measures the momentum of charged particles produced in the collisions. It must provide good spatial resolution and minimal material budget to minimize perturbations of the traversing particles. It is placed in the 3.8 T magnetic field to curve particle trajectories through the Lorentz force and the momentum can be measured via the formula [18]:

$$p[\text{GeV}] = 0.3 \, q \, B \, r \quad (2.3)$$

where B is the magnetic field density in Tesla, q the charge of the incident particle, and r the particle curvature radius in meters. The curvature follows a normal distribution, and its uncertainty can be estimated by [18] :

$$(\delta_\kappa)^2 = (\delta_{\kappa_{\text{res}}})^2 + (\delta_{\kappa_{\text{ms}}})^2 \quad (2.4)$$

where $\delta_{\kappa_{\text{res}}}$ is the contribution from the intrinsic measurement resolution, and $\delta_{\kappa_{\text{ms}}}$ the curvature uncertainty caused by multiple Coloumb scattering in the detector material. A more detailed description of silicon tracking detectors is given in Chapter 3.

The current CMS silicon tracker is a concentric arrangement of 18 barrel layers, complemented on both ends by 15 forward discs, for a total surface of 210 m². It extends from 4 cm to a radius of 110 cm from the interaction point and spans over a length of 540 cm symmetric around the interaction point, covering a pseudo-rapidity range up to $|\eta| < 2.5$. The innermost layers are designed as highly granular silicon pixel detectors and the outermost layers consist of silicon strip detectors. A cross section of the tracker layout is shown in Figure 2.4.

The Pixel Tracker

The pixel tracker is the closest to the interaction point. The very high particle flux in that region imposes very strict performance requirements on its design. It has to provide

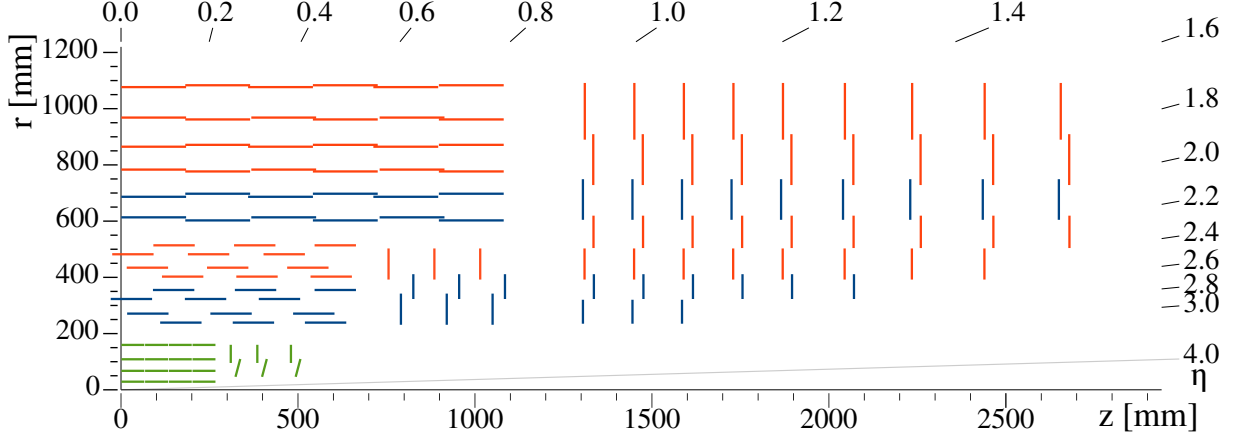


Figure 2.4: Schematic of a quarter of the silicon tracker layout in r-z view indicating the position of the pixel tracker (green) and the strip tracker (red and blue) [19].

high rate capability and radiation tolerance whilst providing high precision track reconstruction and vertex identification. In order to sustain the same level of performance, the initial tracker had to be replaced in the so-called Phase-1 upgrade. As of today, the pixel detector is made of four barrel layers (BPIX) of 54 cm length, located at radii of 2.9, 6.8, 10.9 and 16.0 cm, and three endcap disks (FPIX) at both ends extending in radius from 4.5 to 16.1 cm.

The pixel tracker modules consist of 270 μm and 286 μm thick silicon sensors, segmented into individual rectangular pixel cells of $100 \times 150 \mu\text{m}^2$ in size leading to a total of 66 million readout channels. Signal readout and processing is handled by the PSI46 ASIC [20]. Performance-wise, these pixelated modules produce 3D measurements along the paths of the charged particles with position resolutions between 10 and 20 μm [21].

Strip Tracker

The strip tracker surrounds the pixel detector and extends the overall tracker volume up to the designed 110 cm radius and 540 cm length. It is divided into four Tracker Inner and Outer Barrel layers (TIB, TOB), four Tracker Inner Disks (TID), and two Tracker Endcaps (TEC). In total 14 layers are deployed in the barrel and 12 in each endcap. In the outer region of the tracker, radiation and occupancy levels are considerably lower, therefore the granularity is decreased with a higher pitch.

The strip tracker modules consist of silicon sensors of 320 μm and 500 μm thickness, segmented into individual strips of 80 μm to 180 μm pitch, for a total of 9.3 million readout

channels [22]. To allow for easy mass production at relatively low cost, the strip tracker modules design features simple silicon sensor layouts that allow for cheap mass production, fully analog readout electronics and low-mass support and service infrastructure.

As far as performance is concerned, in the innermost layer, resolutions between 23 - 34 μm in the $r - \phi$ direction and 23 μm in the z direction are achieved. In the outermost layer, the wider strip pitch yields lower resolutions, between 35 - 53 μm in the $r - \phi$ direction and 52 μm in the z direction [17].

2.3.2 The Electromagnetic & Hadronic Calorimeters

The calorimeter detectors serve the purpose of particle energy measurement. They are made of high-density materials where incident primary particles induce a cascade of secondary particles with decaying energy. This process is referred to as *particle shower*. Two types of showers can be distinguished, electromagnetic showers, initiated by electrons and photons, and hadronic showers initiated by hadrons. Electromagnetic showers are the product of cascade energy losses by means of bremsstrahlung and electron-positron pair creation. The end-point of this process is the creation of low-energy photons in a scintillating material with an overall energy corresponding to the energy deposited by the primary particle. Hadronic showers are dominated by the strong force and are the product of pion creation and decay. However, they also yield a fraction of electromagnetic shower. Finally, in order to collect information about both the energy and the trajectory of the showering particles, calorimeters are usually segmented. This allows multiple particles and jets to be distinguished while being matched to particle trajectories recorded in the tracker system.

The Electromagnetic Calorimeter

The Electromagnetic Calorimeter (ECAL) covers pseudorapidities up to $|\eta| < 3$ and consists of one barrel layer (EB) and two endcap layers (ES, EE). 61,200 Lead-Tungstate crystals (PbWO_4) populate the barrel region, and 7,324 the endcap region. PbWO_4 was chosen for its very short radiation length ($X_0 = 0.89 \text{ cm}$) and Moliere radius (2.2 cm), its light emission speed (80% of the light is emitted within 25 ns) and its radiation hardness. The radiation length X_0 of a material is the mean length (in cm) to reduce the energy of an electron by the factor $1/e$, and the Moliere radius corresponds to the lateral spread of an electromagnetic shower in a material.

The crystals are $22 \times 22 \text{ mm}^2$ in the barrel region and $28.6 \times 28.6 \text{ mm}^2$ in the endcap region, with a length of 230 mm and 220 mm, respectively [17]. Within the EB and the EE, silicon avalanche photodiodes (APD) are used to detect the scintillation photons. It should be mentioned that in the endcap region, the ES plays the role of a pre-shower detector in front of the EE. It is made of two layers of silicon strip modules with 1.9 mm pitch, and mounted behind disks of lead at depths of $2X_0$ and $3X_0$. This adds extra material budget to sample the shower profile and yield an estimate of the energy deposit. Figure 2.5 shows a transverse section of a quarter of the CMS ECAL. The calorimeter energy resolution can be parametrized as a function of the incident particle energy as

$$\left(\frac{\sigma}{E}\right)^2 = \left(\frac{S}{\sqrt{E}}\right)^2 + \left(\frac{N}{E}\right)^2 + C^2 \quad (2.5)$$

where S is the stochastic term, N the noise and C a constant contribution. The measured energy resolution for electrons produced in Z boson decays in proton-proton collision data during Run 2 ranges from 2 to 5%, depending on electron pseudo-rapidity [23].

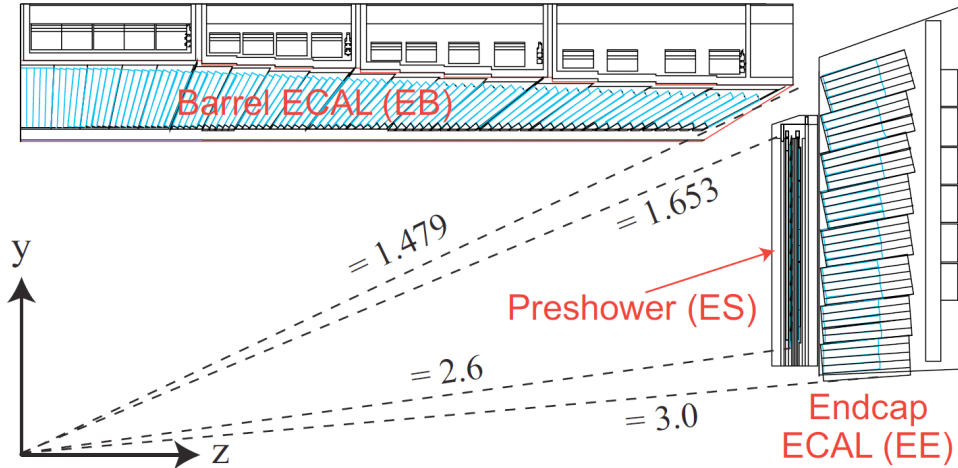


Figure 2.5: Transverse section through the Electromagnetic and Hadron Calorimeters indicating the geometrical configuration [24].

The Hadron Calorimeter

The Hadron Calorimeter (HCAL) is designed around the concept of sampling calorimetry. In this concept, alternating absorbing material, here brass plates, and scintillating material, here plastic scintillators, allow for the measurement of showers' secondary particles. Such a design ensures containment of the incident particles showers inside the calorimeter volume. It is divided into three sections, the hadron barrel (HB), the hadron outer (HO), the hadron endcap (HE) and the hadron forward (HF).

The HB, covers the $|\eta| < 1.4$ region. It is made of alternating layers of brass and plastic scintillators read out by Hybrid Photo-Detectors (HPD). The HE, covers the region $1.3 < |\eta| < 3$. It is made of the same material as the HB but the readout is achieved using Silicon Photomultipliers (SiPM). The HO, located between the solenoid magnet and the muon chambers, is made of plastic scintillators read out by Wavelength Shifter Tubes (WLF) and SiPMs. Finally, the HF, placed beyond the endcaps, covers the region up to $|\eta| < 5$. It is made of quartz fibers read out using Photomultiplier Tubes, while iron is used as an absorbing material. Figure 2.6 shows a transverse section of a quarter of the CMS HCAL. The energy resolution for the barrel layers was measured in test-beams to be [25]

$$\frac{\sigma}{E} = \frac{84.7\%}{\sqrt{E(\text{GeV})}} + 7.6\% \quad (2.6)$$

while for the HF the resolution was [26]

$$\frac{\sigma}{E} = \frac{280\%}{\sqrt{E(\text{GeV})}} + 11\% \quad (2.7)$$

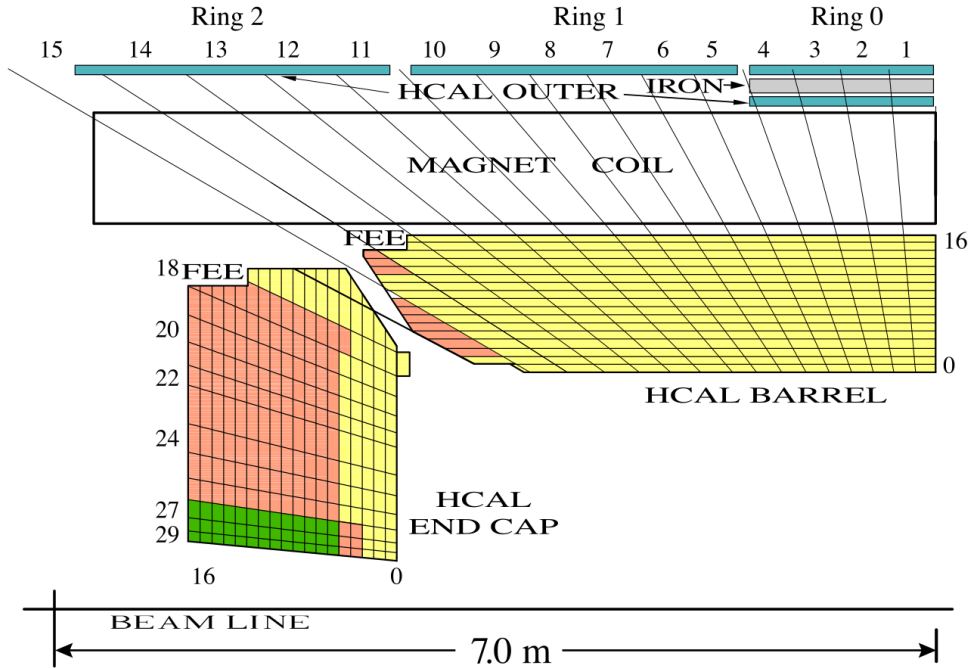


Figure 2.6: Transverse section through the hadron calorimeters indicating the geometrical configuration [27].

2.3.3 The Superconducting Solenoid

As already mentioned, the magnet system plays a decisive role in the overall performance of a particle detector, and more precisely in the momentum measurement. As one of the CMS design requirements is high muon momentum resolution for energies around 1 TeV, a strong field is needed. Consequently, the CMS detector features a superconducting solenoid coil made of Niobium-Titanium (Nb_3Ti) capable of generating a magnetic field of 3.8 T. Around the magnet coil, a large steel structure acts as both support for the magnet and return yoke for the magnetic field. With a total weight of 12,500 tons, the entire magnet structure accounts for the largest part of the experiment's weight. The solenoid geometry of the magnet leads to a magnetic field parallel to the beam axis.

2.3.4 The Muon System

The Muon System is arranged into three sections employing different technologies shown in Figure 2.7: the Drift Tube chambers (DT), the Cathod Strip Chambers (CSC), Resistive Plate Chambers (RPC) and triple-foil Gas Electron Multipliers (GEM).

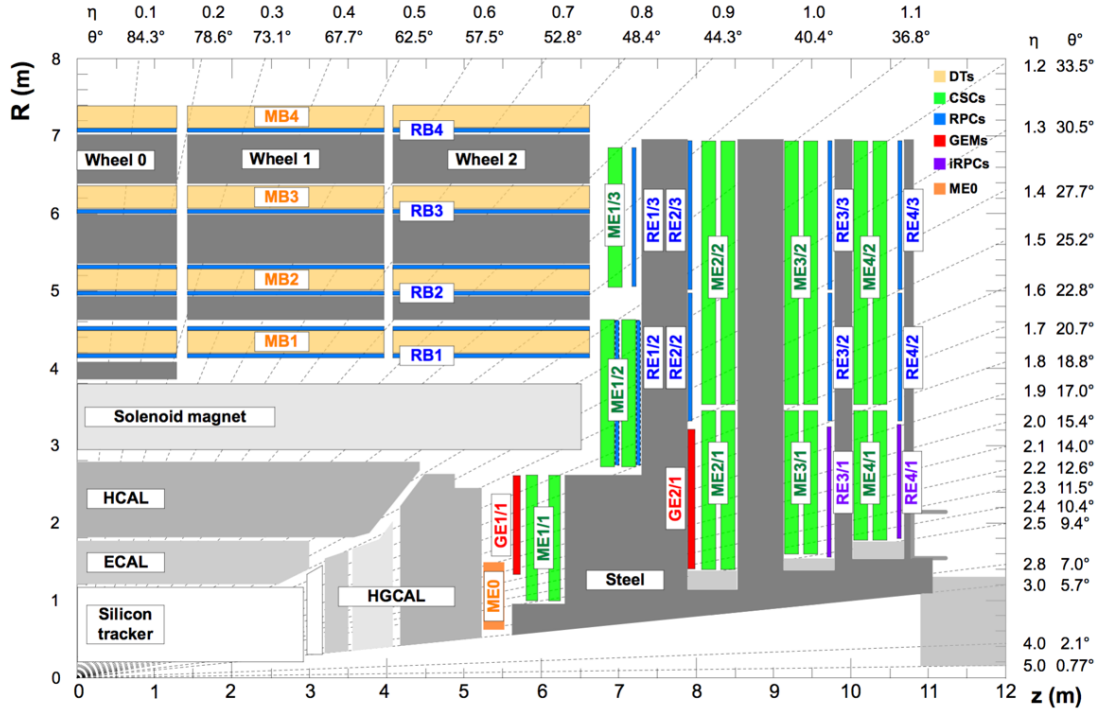


Figure 2.7: Transverse section of one quadrant of the CMS detector showing the present muon system [28].

Drift tube chambers are employed in the barrel region ($|\eta| < 1.2$) where the muon rate and residual magnetic field are low. They consist of 250 chambers organised in 4 layers (MB1,

MB2, MB3, MB4) inside the magnet support structure. With a maximum drift length of 2.0 cm the single point resolution is around 200 μm . In the forward region where the muon rate and magnetic field are high, 468 cathode strip chambers are deployed, covering a region up to $|\eta| < 2.4$. Each CSC is trapezoidal in shape and consists of 6 gas gaps with a plane of radial cathod strips and a plane of anode wires perpendicular to the cathod strips. The CSC information is used in the CMS Level-1 Trigger system and yields a spatial resolution of about 200 μm . Resistive plate chambers are used in both the barrel and endcap regions, covering the pseudo-rapidity region up to $|\eta| < 2.1$. They are arranged into 36 chambers mounted in each of the two rings in the endcap stations. They are operated in avalanche mode to ensure good operation at high rates. RPCs provide a fast response, good time resolution but a coarser position resolution compared to the DTs and CSCs. Finally, a recent upgrade of the muon system deployed GEMs in the region $1.6 < |\eta| < 2.4$. The objective is to limit the rate of background triggers while preserving high trigger efficiency for low transverse momentum muons.

2.3.5 The Trigger & Data Acquisition Systems

At design luminosity, the LHC is able to provide collisions at an interaction rate of 1 GHz. This represents an enormous amount of data requiring a fast and highly performant on-line data acquisition system. Since only a fraction of collision events per second may be stored to mass media, a trigger system providing a high rejection factor is required. This is achieved by means of a two-level trigger system capable of selecting only the most interesting physics events. Fortunately, with regards to the CMS physics program, these 'interesting' events are rare (< 1 Hz) and thus allow for an efficient signal collection while rejecting a large amount of background. The system is therefore divided into two large systems. On the one hand, the Level-1 Trigger (L1T) provides a first-level and fast rejection. On the other hand the High Level Trigger (HLT) provides a more elaborate rejection using advanced processing algorithms. Finally, the two trigger levels are complemented by a dedicated Data Acquisition (DAQ) system where data goes through different processing units before reaching the final storage space.

The Level-1 Trigger

The Level-1 Trigger (L1T) features a quick online decision based on basic reconstructed objects and whether they correspond to an interesting physics event. A Level-1 Accept (L1A) signal is generated if the collected information and the extracted trigger primitives from the ECAL, HCAL and Muon systems pass the L1 pre-defined selection requirements.

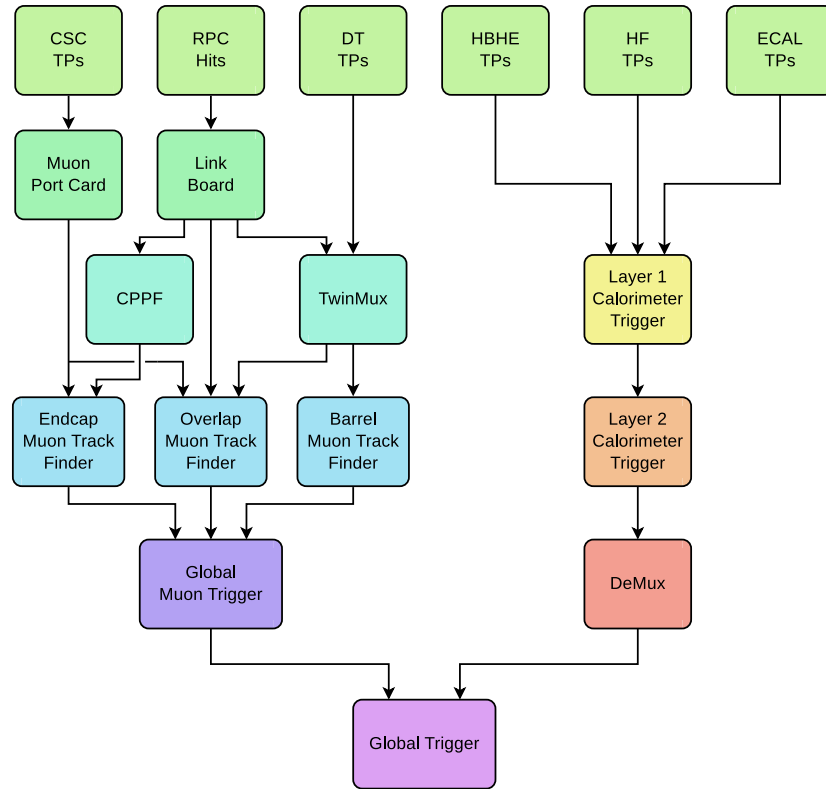


Figure 2.8: Control flow diagram of the Level-1 Trigger System during the CMS Run 2 [29].

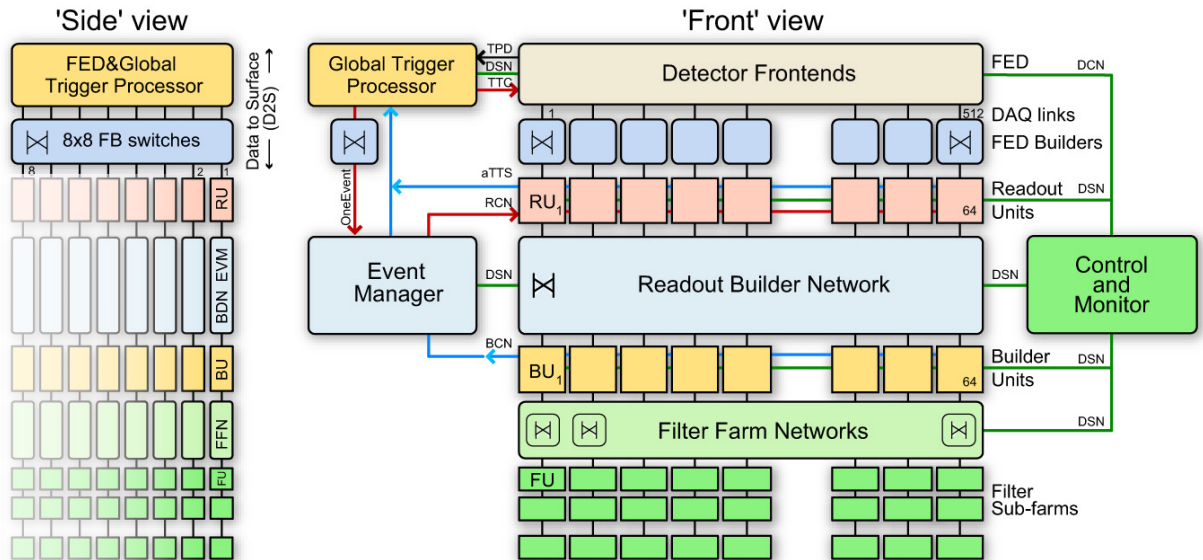


Figure 2.9: Overview of the CMS Trigger and Data Acquisition System. The right block depicts the various parts of the DAQ flow. The Reader Units (RU), the Builder Units (BU), the Filter Units (FU), the Detector Control Network (DCN), the DAQ Service Network (DSN) and the Run Control/Monitor System (RCMS). [30].

Regional trigger systems are deployed for every included detector region, and an L1 Global Trigger correlates multiple trigger algorithms to achieve a rejection factor of 400 [29]. For example, the trigger system selects on regional particles passing transverse energy (E_T) cuts. Figure 2.8 shows the flow diagram of the CMS Level-1 trigger during Run 2.

The calorimeter trigger consists of two layers: Layer-1 receives, calibrates and sorts the local energy deposits ("trigger primitives"). Layer-2 reconstructs and calibrates physics objects such as electrons, τ leptons and jets using the received trigger primitives. A demultiplexer board (DeMux) then reorders, serializes and formats the events for the Global Trigger.

The core of the muon trigger is made of the muon track finders (MTF) which reconstruct the muon trajectories in the barrel, overlap and endcap regions. The reconstructed muon objects are then collected by the Global Trigger which further executes every available and deployed trigger algorithm.

The trigger logic is fully implemented in hardware using Field Programmable Gate Arrays (FPGA) and high speed multi-Gigabit optical links, allowing for a high rejection rate. The initial rate is reduced to 100 kHz corresponding to an L1 trigger latency of 3.9 μ s. During this latency, all data from subdetectors are buffered in front-end pipelines and are sent to the central DAQ system only if the event is accepted by the L1T and an L1A signal is issued.

The High-Level Trigger & DAQ

The High Level Trigger (HLT) is a parallel computing system that receives data from the various detectors and systems such as the L1T, in real time. It deploys various software based algorithms used to reduce the data rate through the selection of highly interesting events based on their physics content. As shown in Figure 2.9, on the way to the central DAQ system, 512 Reader Units (RU) allow for event fragment buffering prior to merging by the RU builder or Readout Builder Network (RBN). The latter is capable of operating at transfer rates up to 800 Gbs. A total of 1.5 MB of fragments is then transferred to the Filter Units (FU) for event reconstruction through the High Level Trigger (HLT). These are highly flexible systems built around advanced reconstruction and decision algorithms deployed on a large Central Processing Unit (CPU) farm. Unlike the L1T, the HLT benefits from a larger allocated processing time of ≥ 40 ms per event, hence allowing for more complex algorithms.

Event data from the Filter Farm Networks is collected by the Computing Services for storage. In addition, monitoring data is collected and processed. The Event Manager acts as an interface to the RU, Builder Units (BU) and the Global Trigger Processor (GTP) to control the event flow through the DAQ system. The control and monitoring of the whole detector is performed by the Run Control and Monitor System (RCMS) which interfaces the full DAQ and Detector Control systems.

2.4 The High Luminosity Upgrade

A major upgrade of the Large Hadron Collider is foreseen for the years 2026-2029, for the so-called High Luminosity phase (HL-LHC). During that phase, the LHC is expected to achieve a peak instantaneous luminosity of 5 to $7 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ at a center mass energy of 14 TeV. The HL-LHC era is expected to span over 10 years and reach, in the ultimate scenario, integrated luminosities up to 4000 fb^{-1} [31]. The overall objective is to study known mechanisms in greater details, such as the Higgs boson, and extend the potential for physics discoveries beyond the Standard Model. In particular, the HL-LHC will allow the CMS experiment to achieve unprecedented levels of precision in the measurements of the Higgs boson couplings to fermions (Yukawa couplings), including the coupling to muons which has a branching fraction of only $\approx 10^{-4}$. Figure 2.10 shows the expected improvement of the precision in the measurement of the Higgs couplings from Run 1 (a) to the HL-LHC (b). In addition, the improved experimental conditions and higher luminosity will allow measurements of the Higgs boson self-coupling, a crucial aspect of the Higgs physics, as it is central for the understanding of the Higgs field. Finally, the discovery potential for many processes beyond the Standard Model will increase as the studies will be able to reach higher masses.

To reach these goals, major improvements to the accelerator complex are foreseen which will challenge the various experiments with harsher experimental conditions. The increase in luminosity will lead to substantial increases in particle density, data rates, radiation levels, and pileup (number of overlapping collisions in one bunch crossing) that will reach up to 200. To cope with that, the experiments will need to upgrade their respective detectors and systems to provide all the data bandwidth, radiation hardness and trigger capabilities required for the best performance, all supported by technologies pushed beyond their present limits. Figure 2.11 shows the current schedule for the remaining LHC physics program and the foreseen HL-LHC upgrade and operation.

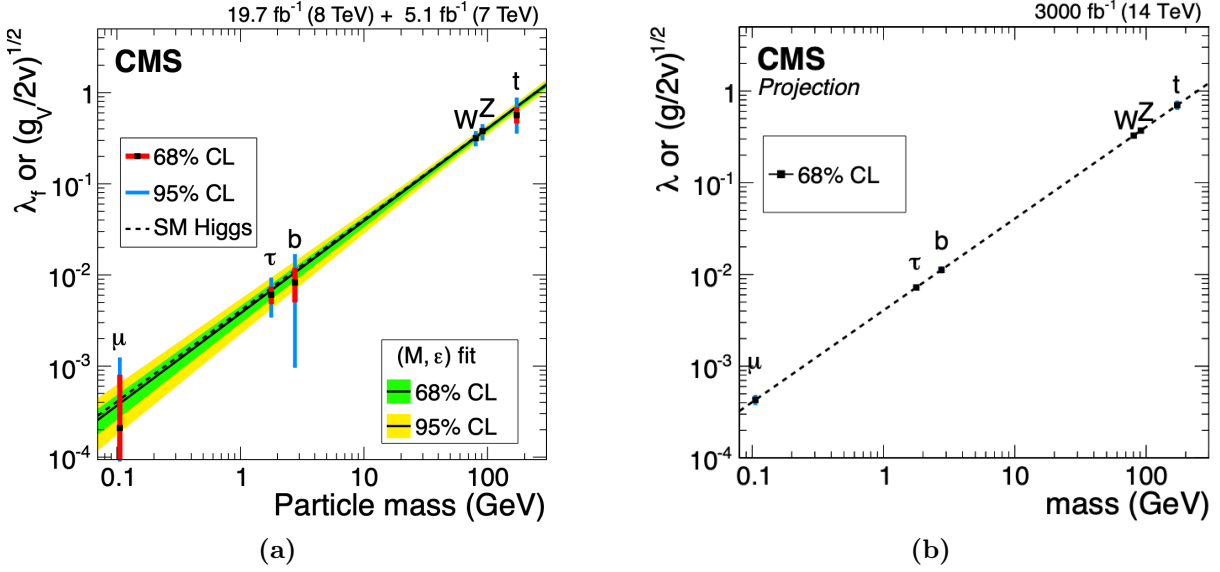


Figure 2.10: Higgs couplings to fermions (Yukawa couplings, λ_f), or bosons ($(g_V/2v)^{1/2}$) measured using Run 1 data (a) [32] and projection for the uncertainties, assuming standard model couplings, for an integrated luminosity of 3000fb⁻¹ (b) [33], as a function of the particle mass.

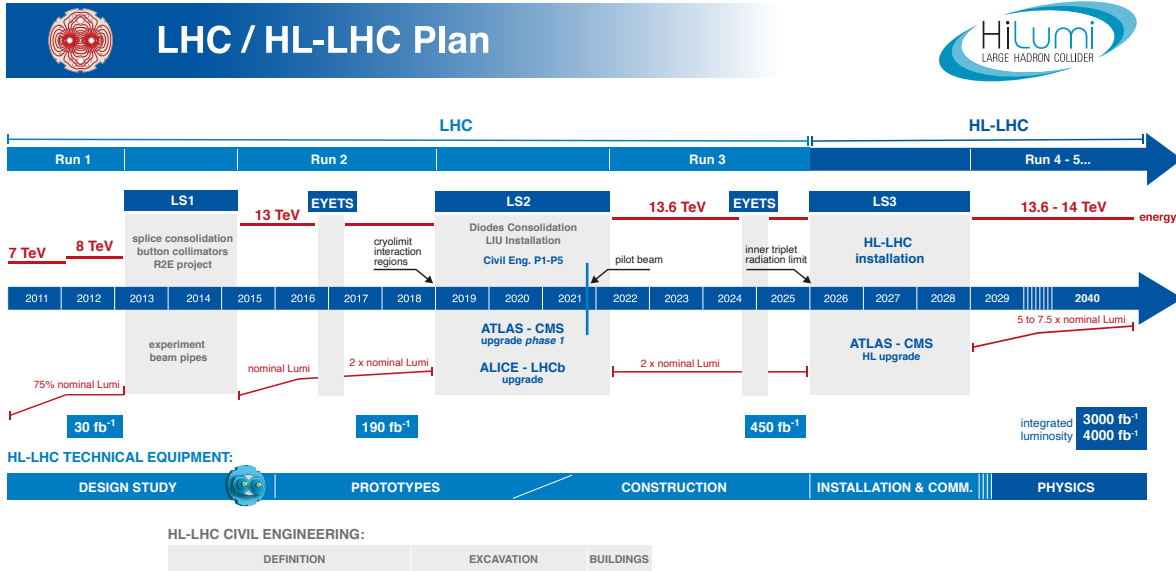


Figure 2.11: Overview of the LHC baseline plan for the next decade and beyond showing target energies and luminosities (red lines) as well as the various construction and installation phases for the HL-LHC [34].

2.4.1 Large Hadron Collider Upgrade

To achieve the design goals of the HL-LHC, several adjustments to the beam parameters will be necessary. These include increasing the number of particles per bunch, improving beam focusing capabilities to reduce the beam size, increasing the number of bunches in the storage ring and making sure that the overlap of the bunches at the interaction point is maximal. Such targeted improvements rely on a combination of cutting edge Nb-Ti and Nb₃Sn superconducting magnets, superconducting radio-frequency cavities (*crab cavities*) for beam rotation, as well as high-power superconducting links with zero energy dissipation. In addition, vacuum, cryogenics and machine protection will require novel concepts for beam control and modelling. Finally, major improvements are foreseen as well at different stages of the overall accelerator complex infrastructure.

2.4.2 CMS Phase-2 Upgrade

The HL-LHC luminosity increase will put the CMS experiment into a very challenging experimental environment. The higher pileup (up to 200) will require systems with improved granularity, resolution and pileup mitigation capabilities. A higher number of collisions also means a harsher radiation environment, reaching a 1 MeV neutron equivalent fluence of $2.3^{16} \text{ n}_{\text{eq}}/\text{cm}^2$ in the innermost regions of the Tracker, and a larger amount of data to be processed. Therefore radiation hardness improvements will be brought to the various CMS subsystems, and novel data acquisition and trigger concepts will be introduced.

The Endcap Calorimeter will feature high granularity (HGCAL) sections based on interleaved absorption and detection layers mixing silicon sensors and scintillators at lower and higher radii, respectively. This new system will allow measurement of the 3D topology of energy deposits in particle showers, as well as precise timing of the order of 30 ps down to low transverse momenta [35, 36].

CMS will also introduce an additional hermetic subsystem, the MIP Timing Detector (MTD), that will allow for precise Time of Flight (ToF) measurement with ≈ 30 ps precision. Such measurement is a powerful means of resolving spatially adjacent collisions during the same bunch crossing, effectively reducing the pileup by a factor of 5. The barrel and endcap regions of the MTD will be made of LYSO crystals with Silicon Photo-Multiplier (SiPM) readout and Low Gain Avalanche Diodes (LGAD) readout, respectively [37].

Finally, the new Silicon Tracker will play a crucial role in coping with the large amount of collision data. It will feature a substantial increase in the number of channels, an improved spatial resolution, and better pseudo-rapidity coverage. It will therefore allow for a better track and vertex reconstruction. Moreover, to improve the pileup mitigation and trigger selection, the outer part of the tracker will directly contribute to the Level-1 trigger. A novel concept of on-module transverse momentum (p_T) discrimination will be deployed in the Outer Tracker and will exploit the strong magnetic field inside the detector to select only high p_T tracks. The Outer Tracker primitives that correspond to these high p_T tracks will be forwarded to the Level-1 Trigger where they will be used in the Level-1 track reconstruction and directly contribute to the trigger decision [38]. This novel concept will allow to sustain the target 750 KHz trigger rate foreseen by the experiment.

This thesis mainly focuses on the upgrade of the CMS Tracker, in particular the Outer Tracker. It provides an overview of its major improvements and introduces the key concept of p_T discrimination to be used. In addition, the design and implementation of the aforementioned concept into corresponding tracker modules is described for one of the two chosen designs, the Pixel-Strip (PS) module that will be thoroughly discussed. It will uncover the details of the mechanical and electronic designs, the mechanical assembly procedure and all aspects of the qualification process both in laboratory and under beam exposure.

CHAPTER 3

SILICON TRACKING DETECTORS

The detection of particles and the measurement of their corresponding properties is at the heart of every particle physics experiment. As previously described in the case of the CMS experiment, multiple particle detectors are employed to study particles produced in high-energy collisions. However, the concepts and technologies used to detect these particles depend on the nature of their interaction with matter and the property to be extracted. In the case of tracking detectors, they are designed to provide information for the determination of charged particle trajectories and the inference of their basic properties such as momentum and electrical charge. Moreover, pileup mitigation is of utmost importance, especially in a high luminosity environment where hundreds of simultaneously occurring interactions need to be distinguished. Therefore, the material, design and instrumentation of tracking detectors have to be carefully chosen to maximize tracking efficiency and spatial resolution performance.

As of today, the technology favored by the CMS experiment is silicon semiconductor detectors. They are based on a solid-state ionization bulk where incident charged particles generate drifting electron-hole pairs which induce a small current on incorporated electrodes. The position sensitivity is achieved by segmenting the bulk and electrode structures in an either pixel-like or strip-like configuration. The induced current is then amplified and processed by a dedicated readout electronics circuit in order to produce a signal corresponding to the traversing particle. Silicon, with a much lower ionization energy of 3.62 eV compared to alternative materials, allow for a sufficiently large signal to be created in a relatively short amount of time, typically $O(10\text{ ns})$. Such fast readout is

of special interest at LHC experiments where collisions happen every 25 ns. In addition, the use of silicon allows for synergies with the micro-electronics industry and access to state of the art and high quality fabrication processes. This chapter provides an overview of the basics of silicon-based tracking detectors.

3.1 Particle Detection

Particle detection can be explained through two fundamental principles. First, the interaction of charged particles with matter, in particular silicon, describes the physics processes and mechanisms that govern energy deposition. The implementation of optimal silicon sensor structures is crucial to allow for an energy deposition with minimal electronic noise disturbance while providing good position sensitivity. Finally, signal formation covers the mechanisms through which deposited energy in silicon structures can be converted into an electronic signal and further be processed.

3.1.1 Charged Particle-Matter Interaction

As they pass through matter, charged particles lose kinetic energy by *excitation* of bound electrons and by *ionization* of atoms along the way. Excitation leads to low-energy photons emitted following the de-excitation of an atom. It is particularly useful for particle detectors capable of recording the emitted photons. Ionization is a scattering process in which incident particles transfer sufficient energy to atomic electrons to be liberated from the atom. For a single charged particle traversing a certain medium, the ionization energy loss per unit length traversed is given by the Bethe-Bloch formula [39]:

$$-\frac{dE}{dx} = 4\pi N_A r_e^2 m_e c^2 z^2 \frac{Z}{A} \frac{1}{\beta^2} \left(\ln \frac{2m_e c^2 \gamma^2 \beta^2}{I} - \beta^2 - \frac{\delta}{2} \right) \quad (3.1)$$

where z is the electrical charge of the incident particle, Z , A the atomic weight and atomic number of the absorber, m_e the electron mass, r_e the classical electron radius, N_A the Avogadro number, I the mean excitation energy, β the relativistic beta, and δ the *density* effect parameter.

The energy loss described by Equation (3.1) only accounts for energy losses due to ionization and excitation. At higher incidence energies, larger contribution from radiation losses, so-called Bremsstrahlung, need to be accounted for. Figure 3.1 shows the differential energy loss for muons for various incidence particle momentum regimes. In the Bethe regime, between 5 MeV/c and 5 GeV/c, the Minimum ionization represents the minimum

deposited energy in the absorbing material, and a particle of that energy is called a Minimum Ionizing Particle (MIP). MIPs are therefore very often used for particle detectors calibration as they yield the minimum energy possibly deposited in the detector.

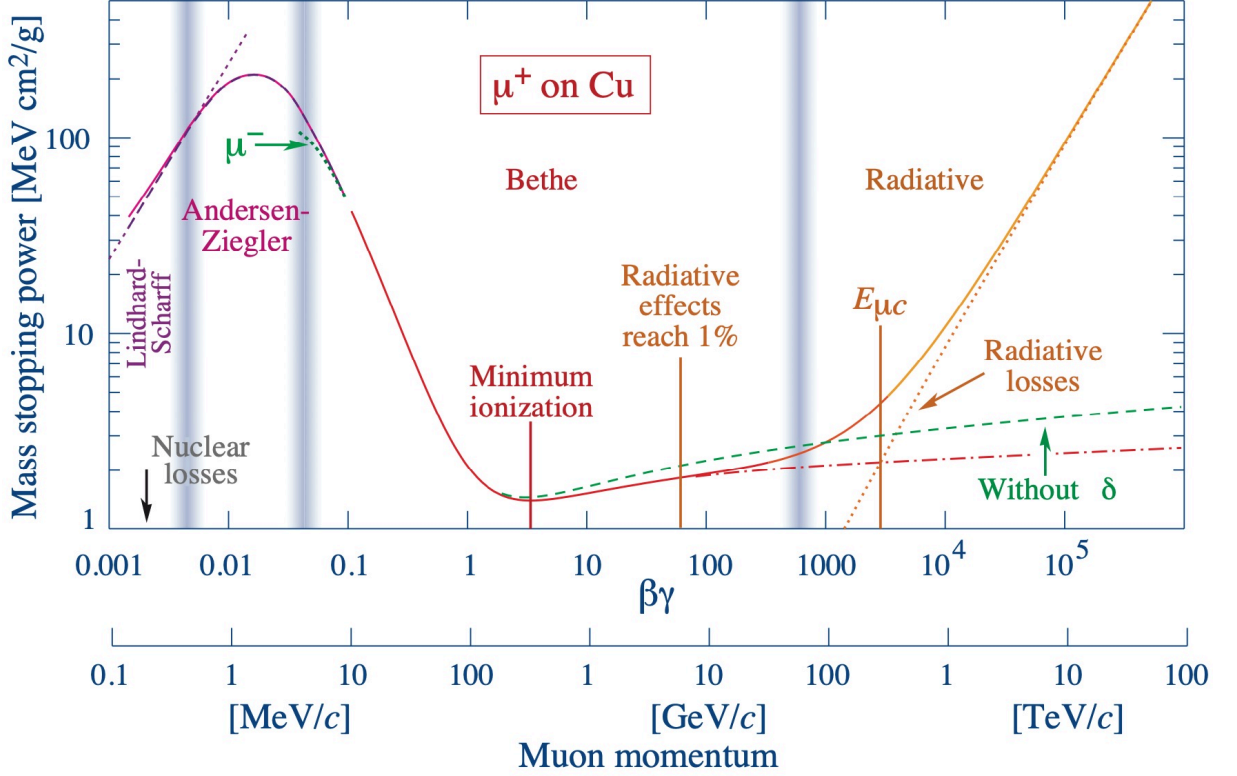


Figure 3.1: Differential energy loss of muons in copper as a function of the incident particle energy [40]. It is calculated using the Bethe-Bloch formula, indicating minimum ionization and including the multiple corrections at low and high incidence momentum.

While the Bethe-Bloch formula yields the average energy loss of charged particles traversing a certain volume of matter, the effective energy loss is subject to strong fluctuations around that average. These fluctuations are parametrized by the Landau-Vavilov distribution, or what is commonly referred to as the Landau distribution. Its probability density function can be written as

$$p(x) = \frac{1}{\pi} \int_0^\infty e^{-t \log t - xt} \sin(\pi t) dt \quad (3.2)$$

The probability density function is defined by a characteristic function that reads

$$\phi(t; \mu, c) = e^{it\mu - |ct| \left(1 + \frac{2i}{\pi} \log(|t|)\right)} \quad (3.3)$$

with μ being the Most Probable Value (MPV) and c a scale parameter.

Figure 3.2 shows an example of a Landau distribution with arbitrary scale. The distribution resembles an asymmetric Gaussian distribution but features a tail towards higher energy losses. This large tail is mainly induced by the account, in the Landau parametrization, of *delta* electrons which are atomic shell electrons that are liberated from the atom and carry sufficient momentum to cause further ionization in the material.

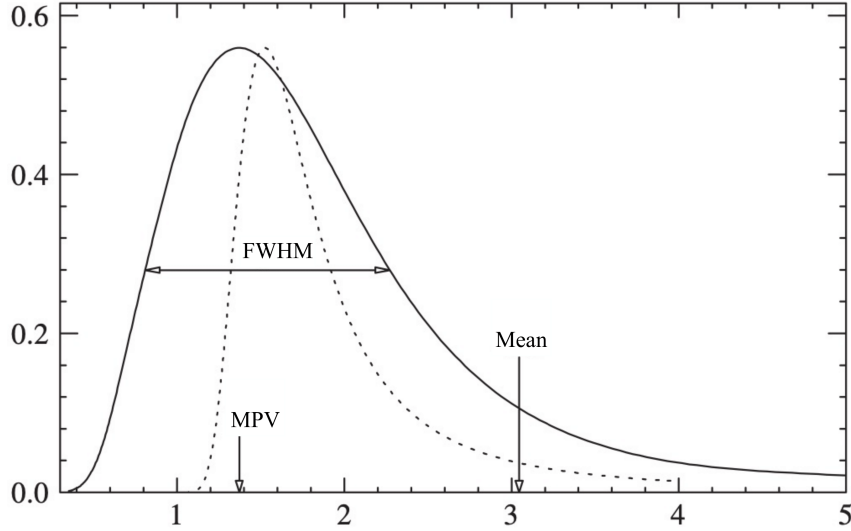


Figure 3.2: Landau distribution (solid line) with arbitrary scales. indicating the Full-Width-Half-Maximum (FWHM), the mean value and the Most Probable Value (MPV). Modified from [41].

The average energy loss by ionization and excitation effectively corresponds to a number of electron-ion pairs generated along the track of the incident particle. Primary ionization and secondary ionization caused by the previously mentioned delta electrons account for the *total ionization*. The total ionization n_T can be computed from the total energy loss in the detector and is expressed as [39]

$$n_T = \frac{\Delta E}{W} \quad (3.4)$$

where ΔE is the total energy loss and W the average energy required to form an electron-ion pair in the traversed material. W of a material is constant for relativistic particles and slightly increases for non-relativistic incident particles. In solid-state detectors such as silicon detectors, the low $W = 3.62$ eV yields a number of created electron-ion pairs that is much larger compared to that in other materials such as Diamond ($W = 13.1$ eV), or gases ($W \approx 30$ eV). Therefore, solid-state detectors, in particular silicon, show a much smaller statistical fluctuation in the number of produced charge carriers for a given energy

loss. For an average of N charge carriers produced, one would naively expect a statistical fluctuation according to Poisson statistics of the order of $\sqrt{N}$. However, the latter happens to be smaller by a factor $\sqrt{F}$ referred to as the *Fano factor* with a value of 0.115 for silicon. This factor is a material-dependent correction applied to the statistical fluctuations of charge carrier generation for a well-defined energy loss and which should be distinguished from the very large fluctuations of the energy loss (Landau fluctuations).

3.1.2 Silicon Sensors

Most tracking detectors employ silicon as sensor material. The latter belongs to the category of semiconductors, exhibiting certain electrical properties that make it suitable to be used as active sensing material. The electrical properties of semiconductors are described by the *band model of solids*. The model states that the discrete electron energy levels of individual atoms within a crystal are merged forming energy bands. The Pauli exclusion principle further imposes that each band only contains a finite number of electrons. The probability density of encountering an electron with a given energy is defined as

$$f(E) = \frac{1}{e^{(E-E_F)/k_B T} + 1} \quad (3.5)$$

with k_B the Boltzmann constant, T the temperature and E_F the Fermi level defined as

$$f(E = E_F) = \frac{1}{2} \quad (3.6)$$

Therefore, some low energy bands are fully filled with electrons while the high energy bands are empty. The lowest partially filled band is called the *conduction band* while the highest fully filled band is referred to as the *valence band*. The gap between the top of the valence band (E_V) and the bottom of the conduction band (E_C) is known as the *forbidden band*, the *energy gap* or more commonly the *bandgap* ($E_G = E_C - E_V$). Figure 3.3 shows the energy band configurations for conductors, semiconductors and insulators.

In the case of conductors, the conduction band is partially filled and due to the free available energy states within the band electrons can move freely within the crystal lattice. This occurs if the conduction band extends below the Fermi energy E_F or if the conduction and valence bands overlap. In the case of insulators, the opposite applies. The Fermi level lies above the valence band with the energy gap being too large for electrons to be excited into the conduction band. Finally, as far as semiconductors are concerned, they behave just as insulators at very low temperatures. However, the very narrow band gap

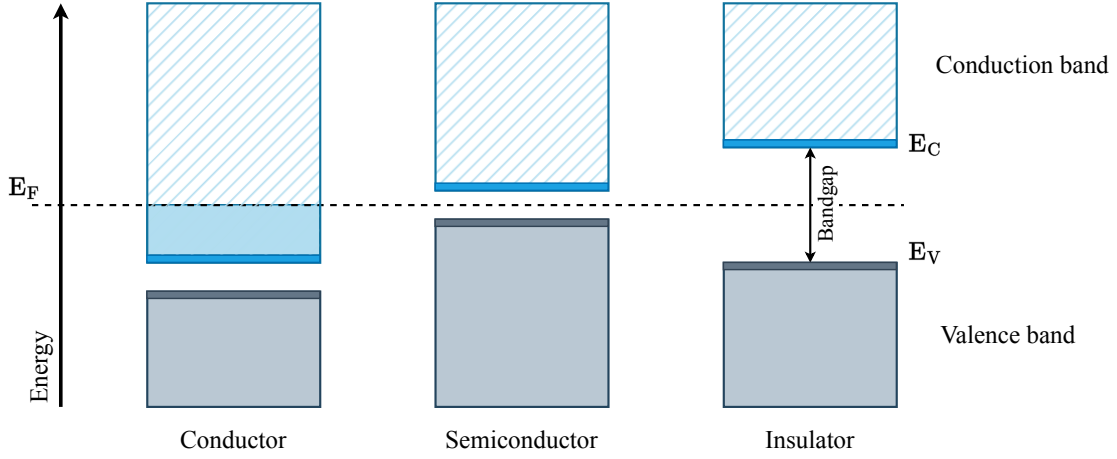


Figure 3.3: Energy band configuration for conductors, semiconductors and insulators. Conductors contain free charge carriers even at very low temperatures. However, semiconductors and insulators have Fermi levels below the conduction band, defining the band gap $E_G = E_c - E_v$.

allows for thermally excited electrons to reach the conduction band. These electrons are usually referred to as intrinsic charge carriers, and the corresponding material is referred to as *intrinsic* semiconductor.

In silicon, the band gap is $E_G = 1.12$ eV, yielding an intrinsically low probability of thermal excitation. However, an external excitation with comparatively low energy is possible, hence giving it high potential for the detection of excitations caused by energy deposits from traversing particles. It should be mentioned that due to a more complex band structure in silicon, an energy deposition of $E_e = 3.6$ eV is required to excite an electron from the valence band to the conduction band. This ionization process, while contributing to electrical conduction, also leaves silicon atoms with missing electrons in the valence band referred to as *holes* which can also act as charge carriers.

Extrinsic Semiconductors

By introducing impurity atoms in semiconductors like silicon, their conduction properties can be selectively altered. This process, known as *doping*, consists of replacing a silicon atom with an impurity element and a doped semiconductor is referred to as *extrinsic*. If the impurity belongs to a group-V element, such as arsenic, a loosely bound electron is added to the valence band. A *donor level* that is just under but very close to the conduction band is then formed and the quasi-free electron can easily be excited into the conduction band. Silicon material of this type is referred to as *n-type* silicon. However,

if the impurity element belongs to a group-III element, such as boron, one of the silicon bonds remains incomplete and an *acceptor level* above the valence band is formed. This newly introduced level then tries to attract one electron from a neighbouring silicon atom creating a hole in the valence band. Silicon material of this type is referred to as *p-type* silicon. Figure 3.4 shows a schematic representation of the n-type and p-type silicon, indicating the additional loose electron for the former and the incomplete bond for the latter.

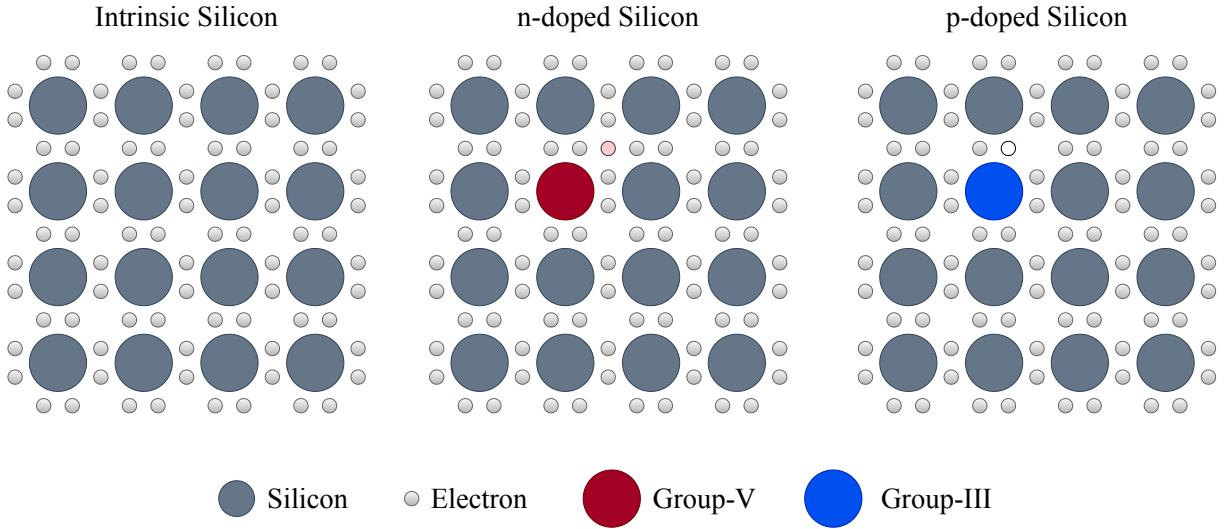


Figure 3.4: Schematic representation of intrinsic and extrinsic silicon. For the n-doped (n-type) silicon, a donor atom adds a loosely bound electron to the silicon valence band. For the p-doped (p-type) silicon, an acceptor introduces an incomplete bond right above the valence band.

PN-Junction

When it comes to detecting traversing particles, the expected number of generated charge carriers is of the order of $O(10^4)$. However, the intrinsic silicon noise arising from free charge carriers dominates the expected signal thus the amount of free charge carriers must be reduced. This can be achieved by forming a junction made of p-doped and n-doped silicon material and referred to as a *pn-junction*.

In the p-doped part, holes are the dominant charge carriers and the Fermi level is very close to the valence band. In the p-doped part, the situation is reversed such that the majority carriers are electrons and the Fermi level is near the conduction band. The strong concentration gradient of the two charge carriers at the interface between the p-doped

and n-doped parts leads to a diffusion current. The latter corresponds to electrons of the n-doped region diffusing into the p-doped region of the crystal, and the other way round for holes. At the interface, recombination of electrons and holes takes place leading to a zone free of charge carriers referred to as the *depletion zone*. However, despite the absence of free charge carriers in the depletion region, the remaining ionized atomic cores give rise to a region no longer neutral but featuring a *space charge* (SCR) as shown in Figure 3.5.

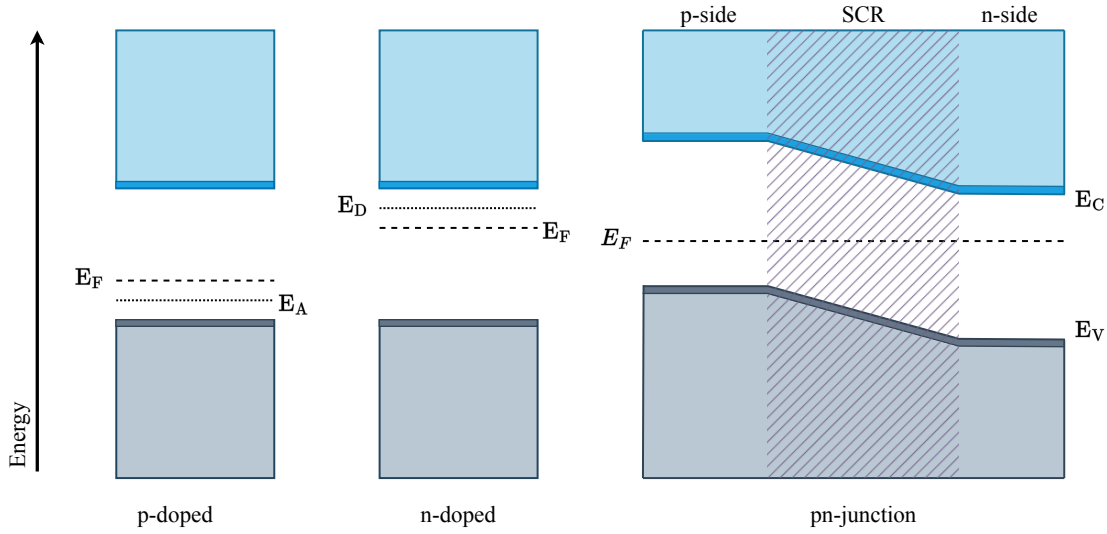


Figure 3.5: Band structure and energy levels of n-doped and p-doped silicon. The acceptor (E_A , left) and donor (E_D , center) energy levels introduced by the dopant alter the Fermi energy E_F of the material. When joining them (right) a common Fermi level develops and a space-charge region (SCR) forms.

The space-charge region is a product of the electric field induced by the diffusion and recombination currents between the differently doped regions. It is of particular importance as the electric field prevents further diffusion and depletes the space-charge region of free carriers. The built-in voltage between the pn-junction boundaries can be derived from the expression of the corresponding electrostatic potential

$$\Phi(x) = \begin{cases} -\frac{N_A}{2\epsilon_r\epsilon_0}(x + d_p)^2, & -d_p < x < 0 \quad (\text{p-doped region}) \\ \frac{N_D}{2\epsilon_r\epsilon_0}(x + d_n)^2, & 0 < x < d_n \quad (\text{n-doped region}) \end{cases} \quad (3.7)$$

where d_n and d_p are the n-doped and p-doped SCR boundaries, respectively. N_A and N_D correspond to the individual doping concentrations, typically of the order of 10^{12-15} atoms

per cubic centimeter, with the effective doping concentration given by $N_{\text{eff}} = N_D - N_A$. The built-in voltage is therefore

$$U_{\text{bi}} = \frac{1}{2\epsilon_r\epsilon_0} \cdot |N_{\text{eff}}| \cdot d^2 \quad (3.8)$$

where d is the total thickness of the depleted SCR. The size of the SCR can be further modified with the application of an additional external voltage U_{bias} which can be derived from Equation 3.8. The SCR thickness is therefore given by

$$d(U_{\text{bias}}) = \sqrt{\frac{2\epsilon_r\epsilon_0}{|N_{\text{eff}}|} \cdot (U_{\text{bias}} - U_{\text{bi}})} \quad (3.9)$$

Depending on the polarity of the applied voltage, the thickness of the depleted region can be increased or decreased. Reducing the SCR is referred to as *forward biasing* while increasing it is referred to as *reverse biasing* and is the usual mode of operation of silicon detectors. The voltage at which the SCR covers the totality of the sensor thickness is called the depletion voltage U_{dep} and is given by

$$U_{\text{dep}} = \frac{|N_{\text{eff}}| \cdot D^2}{2\epsilon_r\epsilon_0} \quad (3.10)$$

where D is the total sensor thickness. A typical range for the depletion voltage of silicon sensors used in particle physics experiments is around 50 to 500 V. Furthermore, as the SCR acts as a capacitor, the sensor capacitance can be calculated from the thickness of the depleted region

$$C = A_{\text{pn}} \frac{\epsilon_r\epsilon_0}{d(U_{\text{bias}})} \propto \begin{cases} \sqrt{\frac{\epsilon_r\epsilon_0|N_{\text{eff}}|}{2 \cdot U_{\text{bias}}}} & \text{for } U_{\text{bias}} \leq U_{\text{dep}} \\ \frac{\epsilon_0\epsilon_r}{D} & \text{for } U_{\text{bias}} > U_{\text{dep}} \end{cases} \quad (3.11)$$

where A_{pn} corresponds to the surface of the pn-junction. The sensor capacitance, being directly related to the sensor thickness at full depletion, is usually used to measure the effective full depletion voltage U_{dep} of the sensor.

Sensor Segmentation

The large majority of present silicon sensors are realized in so-called planar structures. In practice, the silicon wafer, which corresponds to the sensor bulk, is typically produced using the Float Zone (FZ) process which enables production of silicon ingots with spe-

cific resistivity. Other production techniques such as the Czochralski (Cz) or Magnetic Czochralski (MCz) process can also be used as they provide some additional advantages with regards to radiation hardness. Further in the process chain, the silicon bulk is structured with a photolithographic process and then treated by etching, implantation and material deposition. In order to create a position sensitive device, the bulk surface can be segmented in one or two dimensions, such as for example *Strip sensors* or *Pixel sensors*. This way the sensor volume where the charge carriers were generated can be identified and the position of the traversing particle can be deduced.

The segmentation is achieved by implanting the surface of the n-doped or p-doped silicon bulk with strips or pixels of a certain geometry. The most simple example of such segmentation is the so-called p-in-n sensor shown in Figure 3.6 (a). It yields a typical configuration where p^+ -doped implants are locally incorporated in the surface of the bulk, while the opposite side is evenly doped with donors (n^+) across the entire surface forming the so-called backplane. In this context, p^+ and n^+ doping is referred to as *high* or *heavy* doping. It corresponds to doping levels that exceed the order of one per ten thousands atoms. Such a design leads to the creation of a pn-junction between the bulk and the implants. As a result, when a particle traverses the sensor bulk and charge carriers are generated, holes drift towards the implant where they are collected, while electrons drift towards the backplane. An isolation layer, usually SiO_2 , is added to the sensor implant on top of which a metalization layer serves as a capacitive coupling to the implant. Finally, sensor biasing is made possible by connecting every implant to a bias ring via a poly-silicon resistor to evenly distribute the bias voltage.

One other possible segmentation scheme is used in so-called n-in-n sensors which use an n^+ implant, an n-type bulk and a p^+ backplane. However, if the structure is the same, an additional doped region is included between the n^+ implants. This addition can be achieved via the *p-spray* or *p-stop* technique which purpose is to reshape the electrical field close to the sensor surface in order to prevent electrons accumulation.

The segmentation parameters such as the distance between implants, commonly referred to as the sensor *pitch*, are driven by various considerations. Since the charge collected by every implant needs to be read out and processed separately, space requirements for readout electronics integration can be sometimes imposed. Moreover, aspired granularity and position resolution play a crucial role in the sensor design choices.

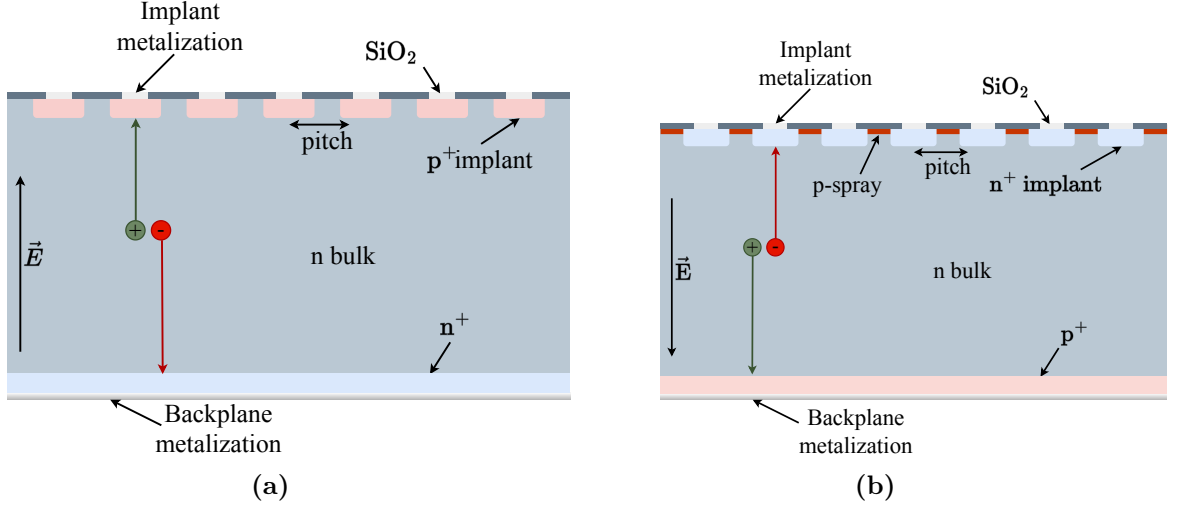


Figure 3.6: Sensor segmentation for p-in-n sensors (a) and n-in-n sensor (b), indicating the bulk type, the position of the implants and backplane metalizations. It also shows the direction of the electric field and the direction towards which each charge carrier moves.

3.1.3 Signal Formation

Signal formation inside silicon sensors is the mechanism by which the charge carriers generated by a traversing particle induce a signal that can be collected and processed. First, the traversing particle deposits energy in the sensor bulk and charge carriers, namely electron-hole pairs, are created. These charge carriers are then separated by the electric field generated by the reverse biasing. Electron and holes move in opposite direction towards either the implant or backplane metalization, depending on the sensor doping type. The moving charges induce an accumulation of charge on the electrode surface, and the induced charge can be recorded as a current or voltage signal.

As far as signal induction is concerned, it is important to note that what matters the most is not so much the effective "collection" of charges but rather their movement towards the electrode implants. The charge movement is initiated by the externally applied electric field (bias voltage) and the process of signal induction mechanism is described by the Shokley-Ramo Theorem [42, 43]. The latter states that the current induced at the electrode is due to changes of the electrostatic flux lines that end on the electrode, rather than the amount of charge received by the electrode.

The relevant observable is the total integrated charge Q , induced by the drifting charge

carriers. The charge collection efficiency (CCE) defines the ratio between the total induced charge Q and the initially deposited charge Q_0 .

$$\text{CCE} = \frac{Q}{Q_0} \quad (3.12)$$

Many factors affect the CCE, among them is the electric field shape inside the sensor volume and the implant geometry. It should be mentioned that CCE is of particular importance as it has a direct influence on the detection performance. Typically, the CCE for fully depleted silicon sensors is very high, often greater than 99.9%. However, it can significantly vary depending on the operating conditions such as temperature and radiation damage.

3.2 Signal Processing

The signal induced by the traversing particle is typically in the range of tens of thousands of electrons, 18.000 electrons for 300 μm silicon sensor, within a collection time of few nanoseconds (typically between 10 and 100 ns). The signal processing is performed by a dedicated Front-End (FE) electronic circuit. Figure 3.7 shows a simplified circuit diagram of a front-end electronics chain. The sensor is represented by a capacitance C_{det} and the connection between the sensor implant and the front-end input corresponds to the wire bond or bump pad. Along the chain, the signal charge is first converted into a voltage by a Charge Sensitive Amplifier (CSA). The output voltage is then discriminated and digitized. The processing chain results in a digital information which is encoded into a comprehensive data format describing for example position, time and amplitude, that can be used for a more elaborate data processing.

Signal Amplification

Signal amplification is achieved using a Charge Sensitive Amplifier (CSA). With a capacitive feedback C_f , the amplifier acts as an integrator of the input current. At its output, it generates a voltage step proportional to the signal charge. However, the sensor capacitance C_d also affects the gain g :

$$V_{\text{out}} = g \cdot Q \quad g = g_{\text{ideal}} \cdot \frac{1}{1 + \frac{1}{A} + \frac{C_d}{C_f A}} \quad (3.13)$$

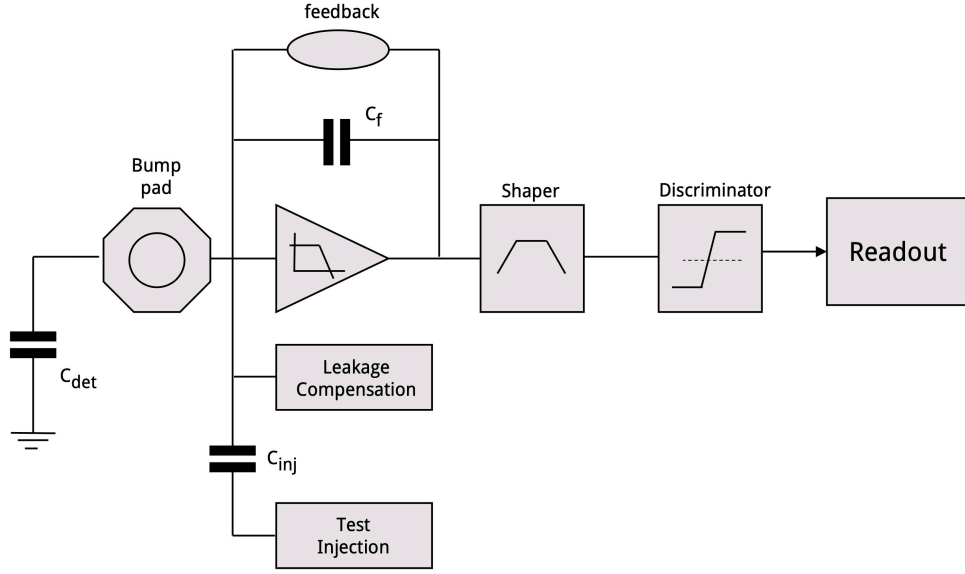


Figure 3.7: Processing chain of a general front-end circuit [44].

where Q is the integrated charge, A the open loop gain, and $g_{\text{ideal}} = 1/C_f$ the ideal closed loop gain. The amplifier is complemented by a feedback circuit required to define the DC operation point of the charge sensitive amplification. It also clears the input node and the feedback capacitor C_f from signal charge so that the amplifier output voltage returns to its initial value. Finally, to sink a significant fraction of the sensor leakage current, a leakage compensation circuit is included at the amplifier input.

Test Charge Injection

The charge injection feature allows the qualification of the front-end electronics without relying on sensor availability or on exposure to traversing particles. Such verification is made possible by including a test charge injection circuit which applies a known voltage step to a well-defined calibration capacitor C_{inj} . This allows for a controlled injection of known charges into the preamplifier, thus emulating a charge injection from a particle traversing the sensor volume. Such a feature is of particular importance for the calibration of the front-end electronics and the validation of operation, even in the early stages of the prototyping when for example the sensors are not yet available.

Signal Shaping

Pulse shaping consists in filtering the amplifier voltage step to generate a pulse that returns to the baseline after a finite time. The first objective is to limit the bandwidth and thus the electronic noise. The second objective is to constrain the pulse width to distinguish

between successive pulse signals. In reality, these two objectives are conflicting and shaper design considerations lead to compromises that depend on the application. For detectors at the LHC, the required timing precision is 25 ns, which corresponds to the 40 MHz bunch crossing. This imposes, for example, that the rising time of the shaped signal is below 25 ns.

Signal Discrimination

To distinguish real signals, generated by traversing particles, from the noise caused by electronic fluctuations described later in Section 3.2.1, the principle of discrimination is often used. From the analogue signal, a discriminator generates a rectangular output pulse (digital signal), usually in a logic standard, if an input signal exceeds a defined (voltage) threshold. This way noise signals with amplitudes below the threshold are filtered out. The threshold value in silicon detectors is usually optimized to maximize the signal detection, bringing it low enough so that low particle signals such as those generated by MIPs can be detected, and high enough for noise signals to be discriminated. Figure 3.8 shows an illustration of the signal discrimination principle.

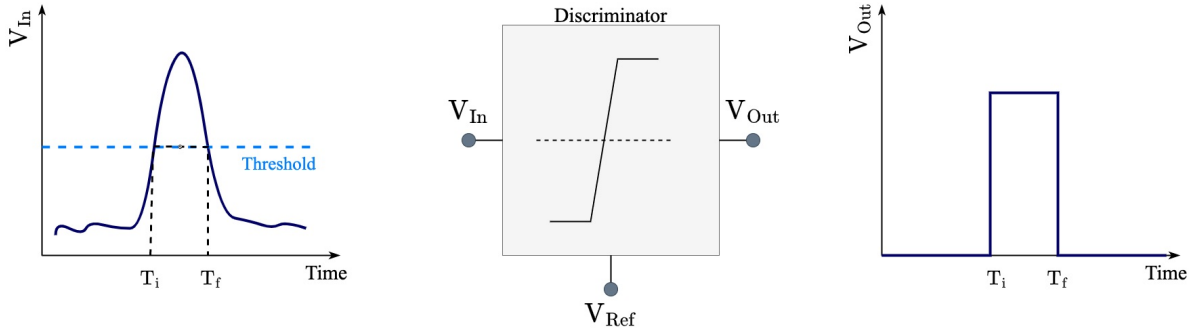


Figure 3.8: Illustration of the signal discrimination principle. A digital signal V_{Out} is produced if the analogue input signal V_{In} exceeds a defined voltage threshold V_{Ref} .

Readout

The signal processing chain ends with the readout stage where further processing of the discriminated signal is performed and application-specific digital logic is applied. Usually, the digital logic performs more advanced processing of relevant quantities. In particle physics, some examples of such quantities are the position of the incident particle in the sensor, the time at which it was detected or the corresponding signal amplitude. Moreover, in particular for the detectors at LHC, the logic circuit provides a trigger system that can

select only a fraction of the recorded events for readout, thus reducing the volume of data to transmit to the back-end system. This is usually implemented using on-chip data buffers to account for the significant delay the trigger signal needs to arrive. Finally, the selected data is transmitted to the dedicated back-end system where further processing, such as particle track reconstruction or momentum measurement, are performed.

3.2.1 Electronic Noise

During operation of silicon sensors, the number of electron-hole pairs generated by a traversing particle is subject to statistical fluctuations originating from multiple sources. This is referred to as *noise*. Four main contributions add up quadratically to form the so-called *equivalent noise charge* Q_n :

- **Leakage current:** Also referred to as *shot noise*, it is produced by the sensor leakage current I_L and scales with the temperature and the signal peaking time t_p of the readout electronics according to

$$Q_{I_L} = \frac{e}{2} \sqrt{\frac{I_L \cdot t_p}{q_e}} \quad (3.14)$$

where e corresponds to the Euler number and q_e to the electron charge.

- **Capacitance:** C_d constitutes the dominant contribution and is written

$$Q_{C_d} = a + b \cdot C_d \quad (3.15)$$

For example, in the case of a silicon strip sensor, the capacitance is mainly defined by the length of the sensor implant. The parameters a and b are characteristics of the readout electronics.

- **Parallel thermal noise:** It originates from the bias resistance current and scales with temperature according to

$$Q_{R_p} = \frac{e}{q_e} \sqrt{\frac{k_B T \cdot t_p}{2R_p}} \quad (3.16)$$

where R_p is the bias resistance and k_B the Boltzmann constant.

- **Serial thermal noise:** It is characterized by the resistance of the sensor implant

R_S and scales with the temperature according to

$$Q_{R_S} = C_d \cdot \frac{e}{q_e} \sqrt{\frac{k_B T \cdot R_S}{6t_p}} \quad (3.17)$$

Among all the aforementioned sources, the dominant ones are the sensor capacitance and the thermal noise. The former can be mitigated by optimizing the sensor design while the latter requires cooling of the sensor during operation. Finally, further noise minimization to guarantee a good signal-to-noise ratio can be achieved via various techniques such as shielding the silicon sensor from external interferences and optimizing the readout electronics.

3.3 Particle Tracking

Particle tracking is the process of reconstructing the trajectory of charged particles in a particle tracking detector. Tracking detectors are usually linear or cylindrical structures of multiple tracking layers. Traversing particles interact with the sensor material in each layer, leaving a precise record of their passage which is recorded by the integrated front-end electronics. The presence of a magnetic field further allows the momentum of the charged particle to be directly deduced from the reconstructed curvature of the trajectory.

In general, signals generated by the traversing particle in neighbouring sensor channels, are first grouped into so-called hit clusters, where the word *hit* refers to the record left by a traversing particle in the sensor. Track finding based on association of detector hit clusters from different tracking layers believed to originate from the same track is performed. Finally a track fitting is performed to fit the trajectory curve to the associated hit clusters and thus extract the corresponding momentum. Figure 3.9 shows a simplified example of a clustering mechanism (a), and a transverse sketch of particle tracking inside a tracking detector within a solenoidal magnetic field (b).

Hit Clustering

In most cases, the charge deposited inside the sensor volume is located underneath several adjacent sensor implants and thus shared among various readout channels. This charge sharing is driven either by charge diffusion, deflection due to the presence of a magnetic field (Lorentz drift), or because the particle traverses the sensor at an angle. Hit clustering is therefore the process with which the adjacent triggered pixels or strips are grouped.

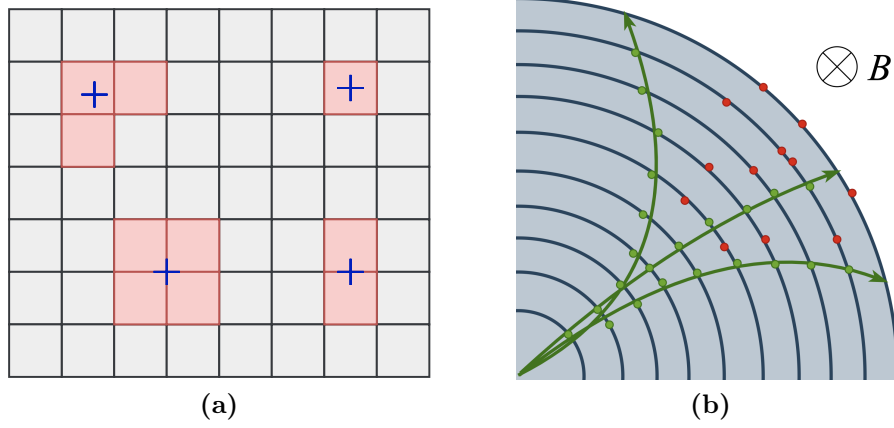


Figure 3.9: Simplified representation of a clustering mechanism (a) and track reconstruction inside of a tracking detector in the presence of a solenoidal magnetic field (b). Neighbouring hits are merged, and the positioning of the corresponding incident particle is computed. A trajectory curve fitting is performed on the associated hit clusters in each layer (green dots).

The main objective is to determine cluster centers that can be transformed from local on-sensor coordinates to a global reference frame where the track reconstruction can be performed. Depending on the charge sharing topology, different algorithms can be applied which are described in [45]. The η algorithm, the Head-Tail algorithm, and the center of gravity (CoG) algorithm are among the many developed. In the η algorithm, neighbouring entries (hits for example) are searched for in time and amplitude around a seed cluster, and are included if they fulfill certain threshold criteria. In the Head-Tail algorithm, in addition to the merging of the adjacent hits, the resulting cluster is divided into two parts, the *head* which contains the high amplitude, energy or momentum entries and the *tail* which contains the low amplitude, energy or momentum entries. This process is further performed until no more splitting can be performed. The Head-Tail algorithm is particularly useful when identifying hadronic jets, which are sprays of particles that are produced when quarks and gluons fragment into other particles. Finally the CoG algorithm, the most commonly used, is a simplified version of the η algorithm, using the same clustering approach but without including timing information. It is shown in a simplified version in Figure 3.9 (a).

Clustering is of particular interest as it ensures that all the charge generated in the sensor volume by the traversing particle is included, thus allowing to improve the position resolution. However, in the case of a binary readout where signal detection is subject to

a discrimination threshold some low amount of charge generated by the particle remains undetected and thus impact the position resolution.

Track Reconstruction

Track reconstruction is performed on the basis of hit cluster positions in the global frame of reference and a suitable track model. In order to account for multiple scattering effects induced by the material along the particle track, more elaborate models and tracking algorithms are necessary. They often focus on different performance features, for example scalability and speed, or optimal track resolution. An overview of the various approaches is given in [46]. The most commonly used approaches are the General Broken Lines (GBL) algorithm [47] used for example in test-beams as discussed in Chapter 9, and the Kalman filter algorithm used by the CMS experiment. In particular, the GBL algorithm, which will be referred to later in the thesis, models the trajectory of the particle using line segments with adjustable parameters that describe the particle's direction and position at each of them. It begins by selecting a set of hits to form an initial track candidate that is iteratively refined to minimize the difference between the predicted and measured hit positions. In addition to the standard line parameters, the GBL algorithm also takes into account corrections for multiple scattering and energy loss. The fit parameters are determined using a χ^2 minimization of the various contributions from the hit cluster positions and the multiple scatterers. Finally the best fitted track is extracted and can be used to deduce a measure of the particle momentum and charge.

CHAPTER 4

OUTER TRACKER PHASE-2 UPGRADE

The present CMS tracker was designed for high efficiency operation at an instantaneous luminosity of $1.0 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$, an average pileup of 20-30 collisions per bunch crossing, and up to an integrated luminosity of 500 fb^{-1} . However, due to the significant radiation damage, the performance is expected to degrade. In the innermost layer of the tracker, a hadron fluence of $3.6 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$ (measured in units of 1 MeV neutron equivalent) is foreseen after collecting an integrated luminosity of 500 fb^{-1} . The accumulated radiation damage will therefore lead to the deterioration of the pixel charge collection efficiency and resolution, and the strip tracker sensor properties. With regards to this performance degradation, the present CMS strip and pixel tracker subdetectors will have to be replaced for the High Luminosity LHC phase. The tracker will undergo major improvements consisting of novel concepts and design modifications in the context of the so-called Phase-2 Upgrade. The objective is to fulfill well defined requirements to meet the target tracker performance and achieve the overall CMS physics goals. Figure 4.2 shows examples of expected performance of the Phase-2 detector. In Figure 4.2(a), simulations of the expected tracking performance for muons and $t\bar{t}$ tracks as a function of the pseudo-rapidity are shown. High tracking efficiency is expected across the entire pseudo-rapidity range. Figure 4.2(b) shows the fit to the di-muon invariant mass distribution for $H \rightarrow \mu^+\mu^-$. The Phase 2 detector achieves 65% better invariant mass resolution thanks the lower material budget and improved spatial resolution of the tracker. More details to the expected performance are given in [38].

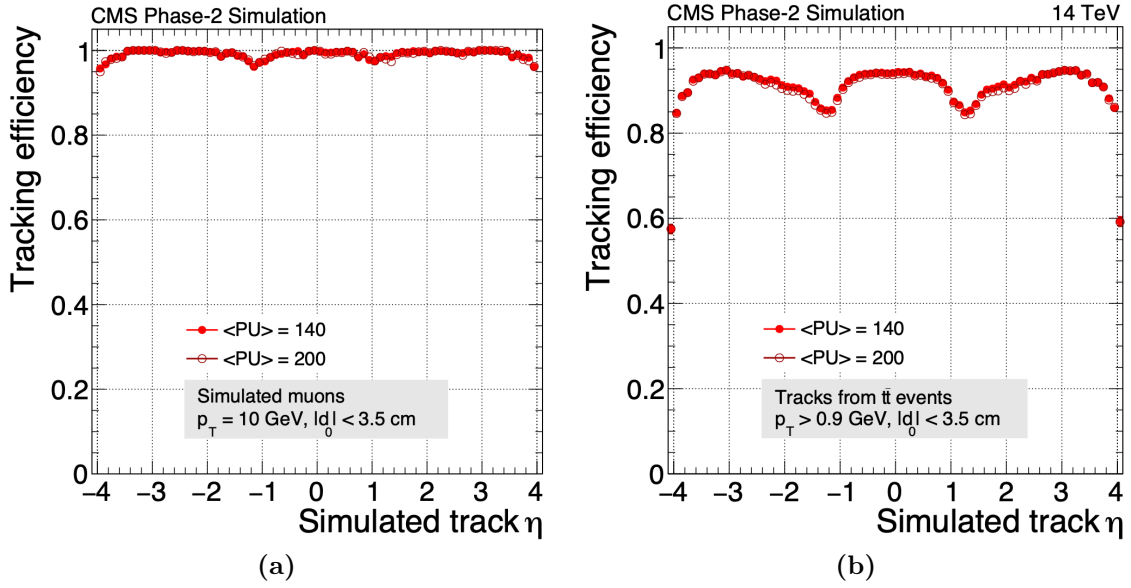


Figure 4.1: Tracking efficiency as a function of the pseudo-rapidity for single muons (a) with $p_T = 10$ GeV and tracks from $t\bar{t}$ events (b) with $p_T > 0.9$ GeV. Full circles correspond to a simulated pileup of 140 and open circles to a pileup of 200. The efficiency is shown for tracks produced within a radius of 3.5 cm from the center of luminous region. The results yield an efficiency close to 100% the entire range of pseudo-rapidity for muons, and around 90% for $t\bar{t}$ tracks in the central region [38].

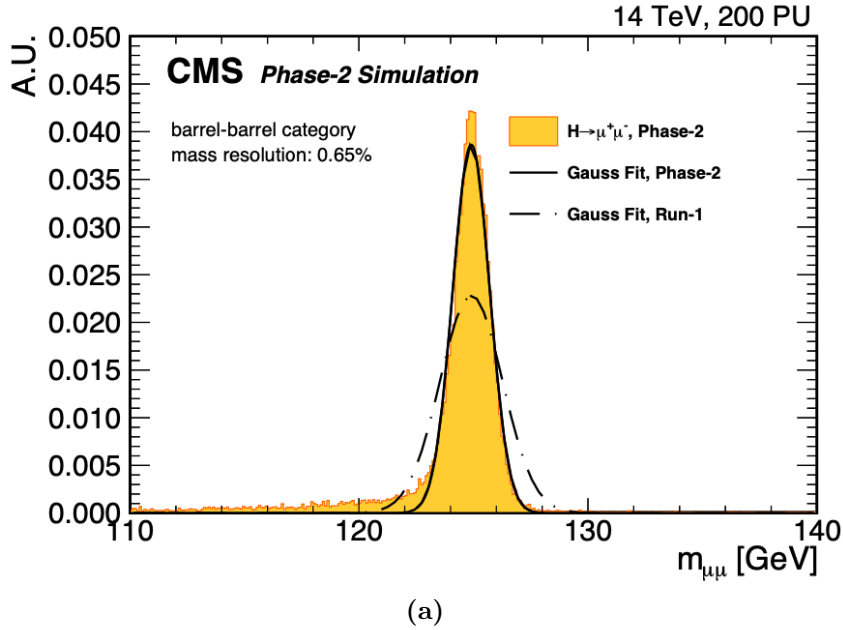


Figure 4.2: The di-muon invariant mass distribution for $H \rightarrow \mu^+\mu^-$ decays for muons in the central region, simulated with the Phase-2 detector [38].

In order to ensure the aforementioned performance, the Phase-2 tracker consists of an Inner Tracker (IT) region made of silicon pixel modules and an Outer Tracker (OT) region based on modules made of combinations of strip and macro-pixel silicon sensors. The main requirements for the tracker upgrade can be summarized as follows [38]:

- Extended tracking acceptance to provide efficient tracking up to about $|\eta| = 4$
- Reduced material budget for the benefit of calorimetry performance and overall event reconstruction in CMS
- Radiation tolerance and full efficiency up to a targeted integrated luminosity of 3000 fb^{-1} , without any maintenance intervention for the Outer Tracker
- Increased granularity with a target readout channel occupancy below the percent level (permille level) in the Outer Tracker (Inner Tracker) to ensure efficient tracking with a high level of pileup
- Contribution to the Level-1 trigger to cope with the rate increase and use tracking information in the L1 event selection
- Improved two-track separation to improve track finding performance in highly energetic jets
- Robust pattern recognition to enable fast and efficient track finding, notably at the High Level Trigger

This chapter focuses on the upgrade of the Outer Tracker and provides an overview of the foreseen detector design, from the corresponding silicon modules (a module referring to an assembly of silicon sensors and their corresponding front-end readout electronics) to the mechanical structures, services and layout. The chapter also introduces the novel concept of transverse momentum discrimination and provides a brief description of the corresponding silicon module designs. Two module designs are foreseen, the Strip-Strip (2S) module and the Pixel-Strip (PS) module. Chapter 5 will later provide a detailed description of the PS module.

4.1 Silicon Modules

As mentioned in the tracker requirements, the contribution to the CMS Level-1 Trigger (L1T) system is of particular importance in order to cope with the increasing data rate foreseen during the HL-LHC phase. As previously mentioned, the L1T acts as a first

filtering or discriminating stage where only collision events with interesting physics signatures are selected while rejecting the uninteresting ones. Those uninteresting events are very often characterized by a very low momentum particles composition. Therefore, one possible way to achieve the contribution to the CMS Level-1 trigger is by introducing tracker modules featuring a particle momentum discrimination logic that can act on the transmitted data upstream of the triggering system. A new concept offering on-board momentum discrimination and capable of rejecting low momentum particles is therefore introduced and implemented in the Outer Tracker.

4.1.1 Transverse Momentum Discrimination

The implementation of the on-board transverse momentum (p_T) discrimination relies on two key ingredients: a strong magnetic field and a stack of two closely spaced silicon sensors read out by common front-end electronics. A schematic representation of the concept is shown in Figure 4.3.

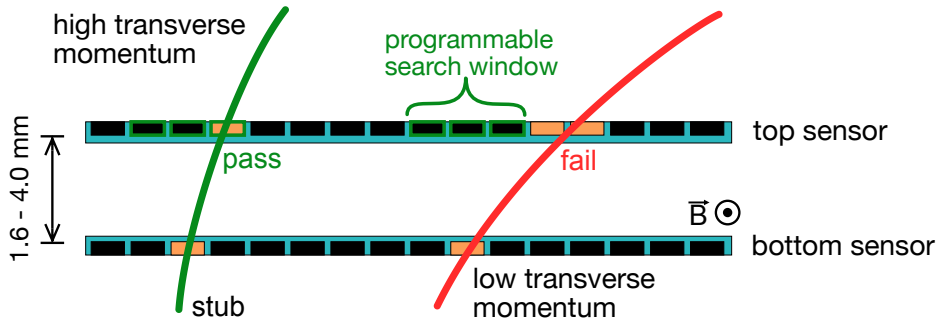


Figure 4.3: Illustration of the transverse momentum discrimination concept. Signals in each of the closely spaced top and bottom sensors are shown in orange. Correlation of the signals within a programmable search window enables rejection of low transverse momentum particles or the creation of stubs. Channels in green represent the programmable search window to create stubs. Shown in red is a low p_T rejected particle. [48]

In the presence of a strong magnetic field, 3.8 T in the case of CMS, and due to the Lorentz force, charged particles are bent in a plane transverse to the direction of the beam. The radius of curvature depends on the particle p_T where high p_T particles yield a smaller bending radius compared to low p_T particles. As the charged particle passes through the module, it generates signals (hits) in the bottom and top sensors of the stack with a spatial displacement that depends on the particle's p_T . Hits are processed by the common front-end electronics and the one from the bottom sensor (*seed layer*) is then

matched, within a programmable search window, to the one in the top sensor (*correlation layer*). If the two hits happen to be within the programmable search window, they are combined to form a short track segment or what is referred to as a *stub*. Otherwise, no stub is produced. In CMS the search window will be set to a defined rejection p_T threshold of 2 GeV, and the stubs generated will be the Outer Tracker's contribution to the Level-1 Trigger.

4.1.2 Module Designs

In the Outer Tracker, the p_T discrimination concept is implemented in two module types: Strip-Strip (2S) modules and Pixel-Strip (PS) modules. 3D models of a PS module (a) and a 2S module (b) are shown in Figure 4.4.

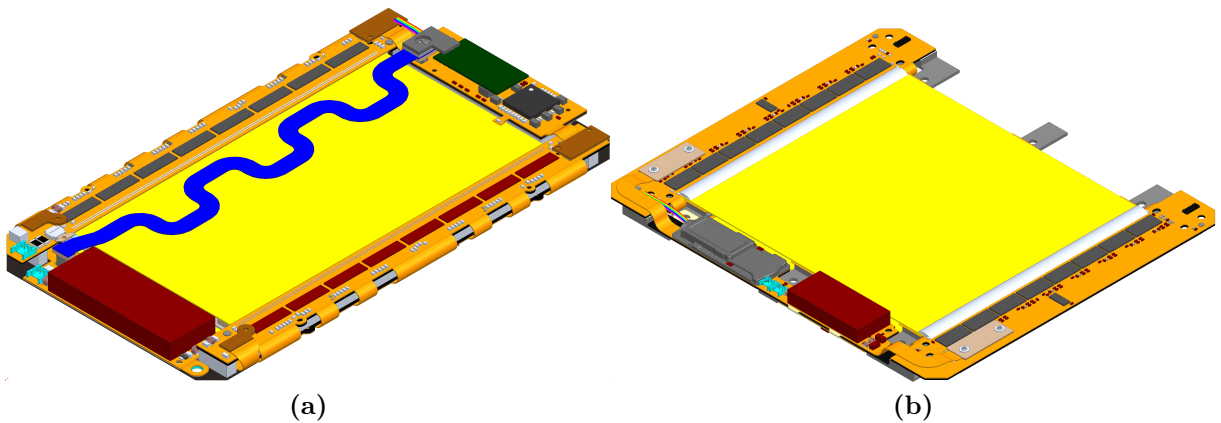


Figure 4.4: 3D models of a PS module (a) and a 2S module (b). The PS module consists of a macro-pixel sensor and a strip sensor, while the 2S module is made of two strip sensors. The model also shows in orange the front-end and service hybrids around the sensor assembly in yellow. Each of the module flavours is made in different spacing variants. [48]

Both the 2S and PS modules consist of a stack of two silicon sensors made in n-on-p technology using high resistive float zone silicon, separated by dedicated spacers. In the 2S module, the separation is done using Aluminum Carbon-Fiber (Al-CF) bridges, while in the PS module Aluminium-Nitride (Al-N) spacers are used. As far as the vertical spacing between the top and the bottom sensor is concerned, different spacing variants are foreseen in order to ensure a consistent p_T discrimination regardless of the position of the module inside the detector. The 2S module comes in two spacing variants: 1.8 mm and 4.0 mm, while the PS module comes in three: 1.6 mm, 2.6 mm and 4.0 mm. Table 4.1.2

summarizes the number of modules per type and variants foreseen for the Outer Tracker detector. Each of the collaborating CMS institutes will be in charge of assembling one or more module types and flavours. For example, at the Deutsches Elektronen Synchrotron (DESY) laboratory, more than 1120 of 4.0 mm PS modules will be assembled.

Table 4.1: Number of modules in the Outer Tracker, by module type and variant.

Module type	Spacing variant	Total per variant	Total per type
2S	1.8 mm	7256	7680
	4.0 mm	424	
PS	1.6 mm	826	5616
	2.6 mm	1462	
	4.0 mm	3328	

The 2S module is made of a stack of two $\sim 10 \text{ cm} \times 10 \text{ cm}$ strip sensors providing two rows of 1016 strips each with a pitch of $90 \text{ }\mu\text{m}$ and the PS module consists of a stack of a macro-pixel sensor (PS-p) on the bottom and a strip sensor (PS-s) on the top. The PS-p provides a 32×960 matrix of $\sim 1.5 \text{ mm}$ long macro-pixel implants with a pitch of $100 \text{ }\mu\text{m}$. The PS-s consists of 960 rows of $\sim 2.5 \text{ cm}$ long strip implants with a pitch of $100 \text{ }\mu\text{m}$. Both the PS-p and PS-s sensors active area are approximately $5 \times 10 \text{ cm}^2$. The reduced size and higher granularity of the PS module is motivated by the higher track density in the inner regions of the Outer Tracker where they will be placed, keeping the occupancy at acceptable levels. The $90 \text{ }\mu\text{m}$ and $100 \text{ }\mu\text{m}$ pitch sizes will allow excellent performance in terms of resolution while respecting limits imposed on the line and bump densities of the front-end readout electronics.

As far as the front-end electronics is concerned, the 2S and PS sensor stack is surrounded by three and four hybrid circuits (or hybrids), respectively. Both modules are equipped with two Front-End Hybrids (FEH). The FEHs host the front-end readout Application Specific Integrated Circuits (ASICs) that connect to the sensor and provide the analogue and digital circuits used to read out the sensors and process the data, in particular to perform the p_T discrimination. The FEHs are complemented by a Service Hybrid (SEH) in charge of the power distribution and optical data transmission. In the case of the PS module, due to its smaller geometry, the SEH is split into two separate hybrids, namely

the Power Hybrid (POH) and the Readout Hybrid (ROH) for power and optical data transmission, respectively. In this thesis, the focus will be set on the PS module and a detailed description of its corresponding hybrid designs and ASIC components is given in Chapter 5.

4.2 Layout & Mechanics

Figure 4.5 shows a schematic layout of a quarter of the Phase-2 tracker with the interaction point located at coordinates (0,0) and the beam pipe positioned along the z axis. It consists of a multi-layer barrel region with an endcap section on each side.

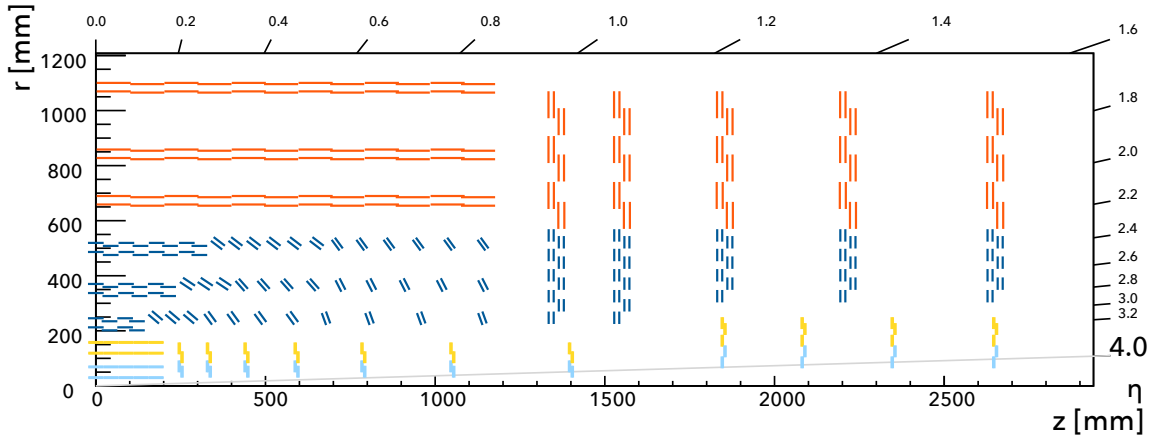


Figure 4.5: Schematics of a quarter of the tracker layout in r - z view indicating the position of the Inner Tracker (yellow and cyan segments), and the three sections of the Outer Tracker, namely the TBPS (flat and tilted blue segments), TB2S (flat red segments) and TEDD (blue and red vertical segments). [48]

The Inner Tracker (IT) occupies a total length of around 5 m for a total diameter of 0.5 m, ensuring coverage up to $|\eta| < 2.4$. The Outer Tracker is positioned around the Inner Tracker and is arranged into three sections: the Tracker Barrel Pixel-Strip (TBPS), the Tracker Barrel Strip-Strip (TB2S) and the Tracker Endcap Double-Discs (TEDD). Its total length is similar to the IT and its radius extends to around 1.2 m. The TBPS and TB2S regions are made of three concentric *barrel* layers covering the region $|z| < 1200$ mm. The former is populated with PS modules, while the latter is populated with 2S modules. They are complemented by the TEDD region which is made of five *endcap* double-discs in the region $1200 < |z| < 2700$ mm. It is populated with PS modules in the inner rings and 2S modules in the outer ones.

4.2.1 Tracker Barrel PS

The Tracker Barrel PS (TBPS) is entirely equipped with 2872 PS modules distributed over three concentric layers, each divided into three sections as shown in Figure 4.6. The central section features horizontal modules supported by flat plank structures in a so-called *barrel* arrangement. The end sections feature tilted modules disposed at an angle ranging from 47 to 74 degrees and supported by conical rings. In this configuration, TBPS provides increased barrel hermiticity with respect to particles emerging from the luminous region.

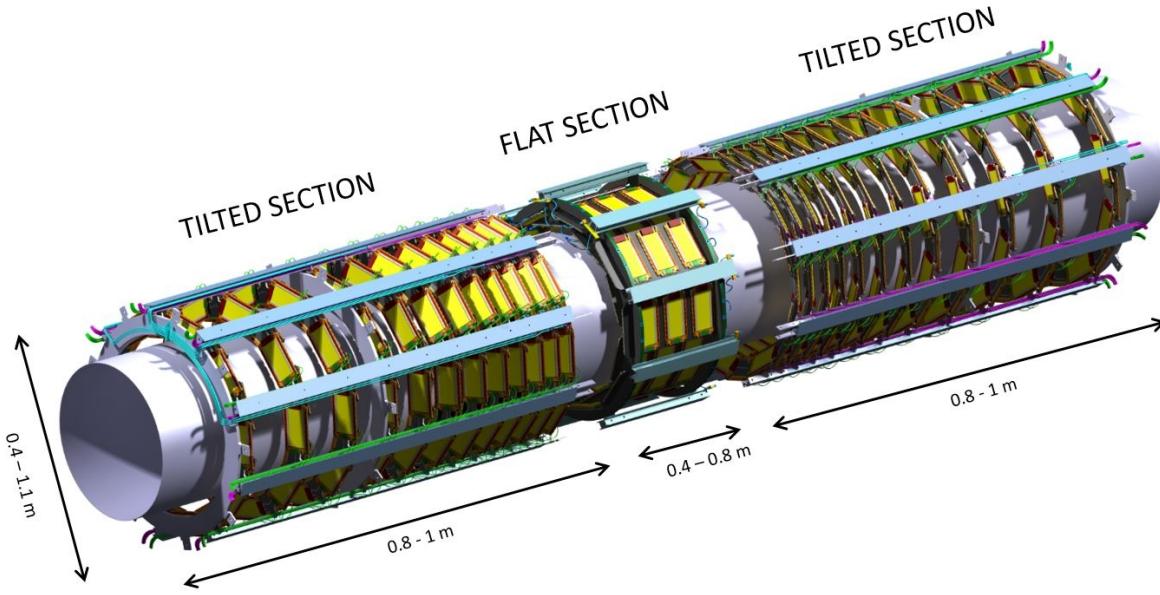


Figure 4.6: 3D CAD drawing of the first layer of the TPBS, indicating the flat and tilted sections [38].

The flat and tilted sections are mechanically joined using longitudinal I-beams. These I-beams also provide routing paths for cooling and cabling. The central planks are made of a foam core hosted between two Carbon fiber skins with a U-shaped cooling pipe embedded into the Carbon foam and located in the mid-plane of the plank. Small metallic inserts are embedded into the plank structure and allow the fixation of modules. The thermal connection between the plank surface and the modules is ensured through a phase-change thermal interface material. In the tilted section, the modules are placed on ring structures made of a sandwich of Carbon foam and CFRP with a circular cooling pipe running through the ring mid-plane. To attach the modules, high-conductivity Carbon fiber laminated cooling plates are used. The connection between the cooling plates and the cooling pipe is ensured by small Al-CF fibers composite pieces, and the thermal contact to the modules is achieved via a phase-change thermal interface material.

4.2.2 Tracker Barrel 2S

The Tracker Barrel 2S (TB2S) is entirely equipped with 4464 2S modules distributed over 372 ladders each containing 12 modules. A wheel consisting of four vertical discs joined by cylinders in the inner and outer radii acts as a support to the ladders. Figure 4.7 shows a 3D view of the inner-most layer as installed in the support wheel.

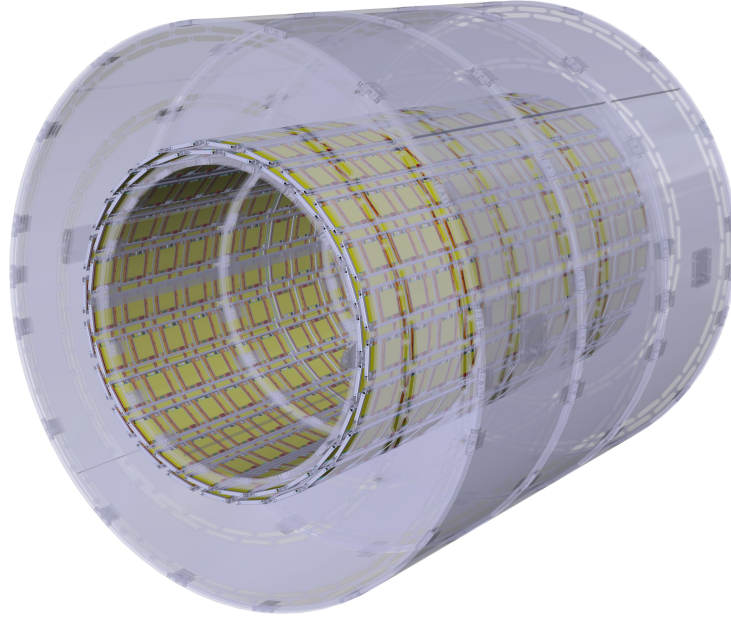


Figure 4.7: 3D CAD drawing of the first later of the TB2S as installed in the support wheel [38].

The TB2S ladders consist of two parallel CFRP C-shaped profiles supported by several orthogonal cross pieces also made of CFRP. Machined inserts made of aluminium are used for module fixation on the C-shaped profiles. They also provide a connection to the U-shaped cooling pipe covering the full perimeter of the ladder. Finally, cable routing is supported on the periphery along the modules and inside the C-profiles.

4.2.3 Tracker Endcap Double Discs

The Tracker Endcap Double Discs (TEDD), as the name suggests, is made of a total of 10 CFRP double-discs, five in each endcap, equipped with a mix of 2S and PS modules arranged in concentric rings. 2S modules are placed in the outer rings while PS modules are placed in the inner ones. In practice, for assembly reasons, each disk is split into two so-called *dees*, and two dees are assembled to form one disk. Figure 4.8 shows a simplified 3D view of the two identical TEDD units forming the two Outer Tracker endcap. The global mechanic structures and services are not shown.

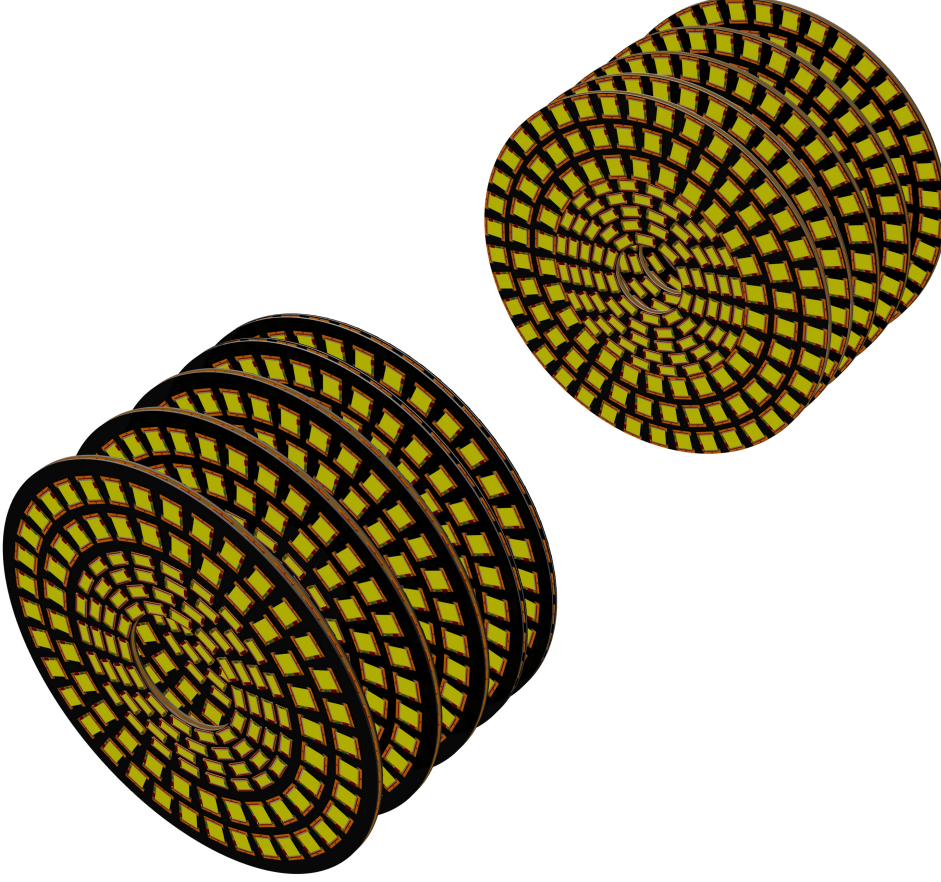


Figure 4.8: 3D CAD drawing of the two TEDD units each made of five double-discs and populated with 2S and PS modules [38].

The cooling pipes distributed over six cooling circuits run inside each Dee structure and pass in a *zig-zag* fashion along the module rings, intersecting every module cooling contact. The cooling contacts are realized differently for 2S and PS modules. For 2S modules, they consist of aluminium inserts. For PS modules, carbon foam blocks are embedded inside the Dee, underneath the PS module positions, to provide thermal connection between the dee skin and the cooling pipe. Finally, the cable routing is achieved radially outwards, above and between the modules to the outer periphery of each dee, but the final scheme is still to be defined.

4.3 Back-End Systems

As far as detector control and data readout is concerned, the Outer Tracker data flow consists of two separate data paths: the *Stub* data path, and the *Level-1* or *L1* data path. Figure 4.9 shows a schematic diagram of the data flow between the front-end modules

and the back-end systems. The Stub data path corresponds to the correlation primitives generated by the p_T discriminating logic. They are transmitted to the Readout system at the bunch crossing frequency of 40 MHz. The collected stub data is processed and forwarded to the back-end Track Finder (TF) system where it is used to reconstruct so-called Level-1 particle tracks. Finally, these tracks are transmitted to the Level-1 trigger system where they contribute to the Level-1 trigger decision. On the other hand, the L1 path is only used upon reception of a Level-1 Accept signal from the Level-1 trigger system. The path is dedicated to the full event data corresponding to the complete event hit information. This data is transmitted to the back-end Readout system and transferred to the central CMS DAQ system at up to a unprecedented nominal trigger rate of 750 KHz.

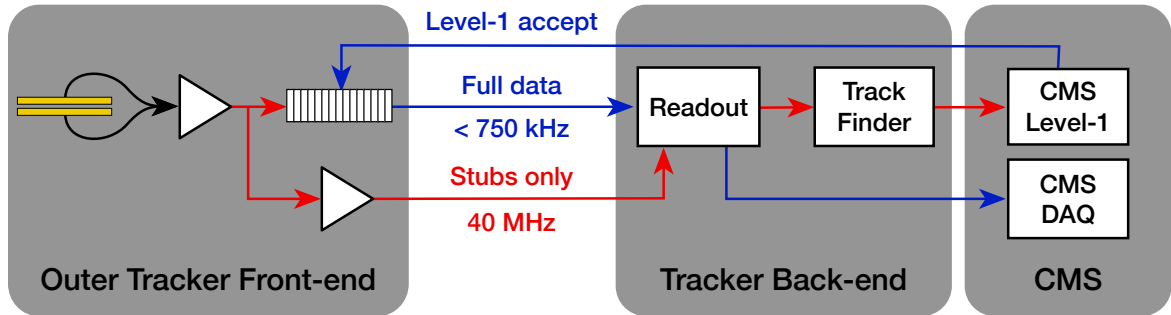


Figure 4.9: Schematic diagram of the front-end to back-end data flow. Red arrows represent the Stub data path, whereas blue arrows represent the Level-1 data path which corresponds to the full event data path.

4.3.1 Data Trigger & Control System

The Outer Tracker back-end control and readout is based on the Data Trigger and Control (DTC) system. It acts as an interface between the front-end modules and the central CMS control system. It consists of several custom boards based on the CERN Serenity [49] carrier card with each controlling and reading out up to 72 front-end modules. Each optical fiber pair associated to a front-end module supports a data rate up to 10 Gbps in the upstream (from the front-end to the back-end), and 2.5 Gbps in the downstream (from the back-end to the front-end). As a result, the expected aggregate maximum data rates per DTC board are 720 Gbps in the upstream and 180 Gbps in the downstream. The DTC boards are still under development but the current version is based on two Kintex

ultrascale Field Programmable Gate Arrays (FPGA) dedicated to the control and readout of the front-end modules, and a single CPU to interface the other back-end systems. In particular, the DAQ and Level-1 Track Finding systems will be linked to the DTC system through additional links operating at 25 Gbps. Figure 4.10 shows a simple diagram of the DTC system, indicating the corresponding data flow.

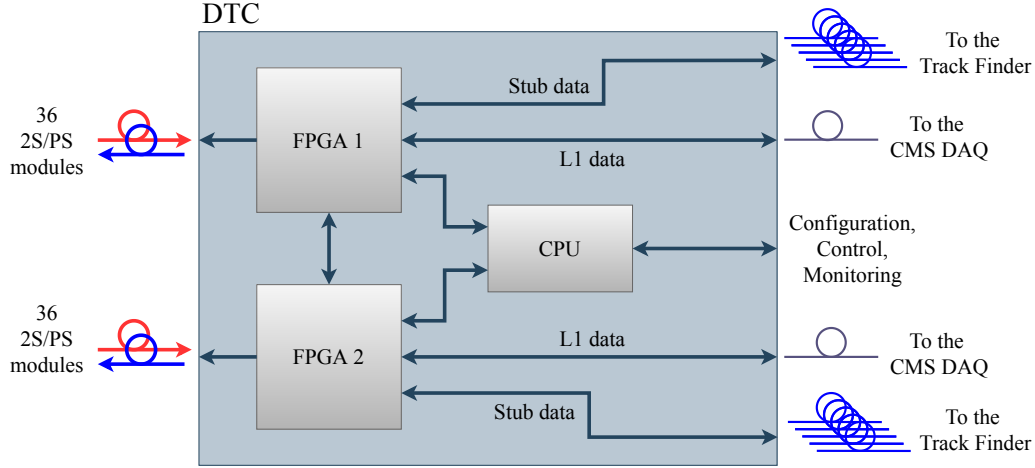


Figure 4.10: Simplified diagram of the DTC system.

4.3.2 Level-1 Track Finding System

The Level-1 Track Finding (TF) system is in charge of the reconstruction of particle tracks using the stub data transmitted at the bunch crossing frequency. The corresponding track finding algorithms will be deployed on powerful FPGA hosted on custom boards based on the CERN Apollo platform [50], where Stub data is received over multi-gigabit data links from the DTC system. The reconstructed tracks will then be used as an input to the Level-1 Trigger.

The Outer Tracker module designs and readout have been optimized to support discrimination of particles with $p_T < 2$ GeV and thus L1 tracking for particles with $p_T > 2$ GeV. However, tracking at Level-1 is a challenging task. In the highest pileup scenario of 200 events, about 15 000 stubs are expected to be produced at each bunch crossing. Level-1 tracks will need approximately 5 μ s to be reconstructed. Therefore, to transmit the stub data, reconstruct the tracks and deliver the Level-1 Accept trigger signal while remaining in the L1 trigger latency budget of 12.5 μ s, a sector-based strategy will be employed. Figure 4.11 shows a simplified diagram of the sector-based approach used for track finding, indicating the stub data flow. The outer tracker will be divided into nine sectors or

so-called *nonants* of modules read out by 24 DTC systems. The Track Finder is made of multiple FPGA-based computing units referred to as Track Finding Processors (TFPs). Tracks are reconstructed from single processing nonants rotated by 20° in ϕ with respect to the detector nonants in order to allow duplication and thus reducing track truncation. Within a single bunch crossing, tracks shall be reconstructed by a single TFP within 450 ns. However, the 40 MHz processing rate will be maintained thanks to a time multiplexing technique where track finding is distributed over 18 TFPs. Therefore, the required 450 ns processing time, distributed over the 18 TFPs, will allow an effective processing time of 25 ns per bunch crossing, matching the system requirements. Finally, as already mentioned earlier, the TFPs will transfer the reconstructed track to the Level-1 Trigger system.

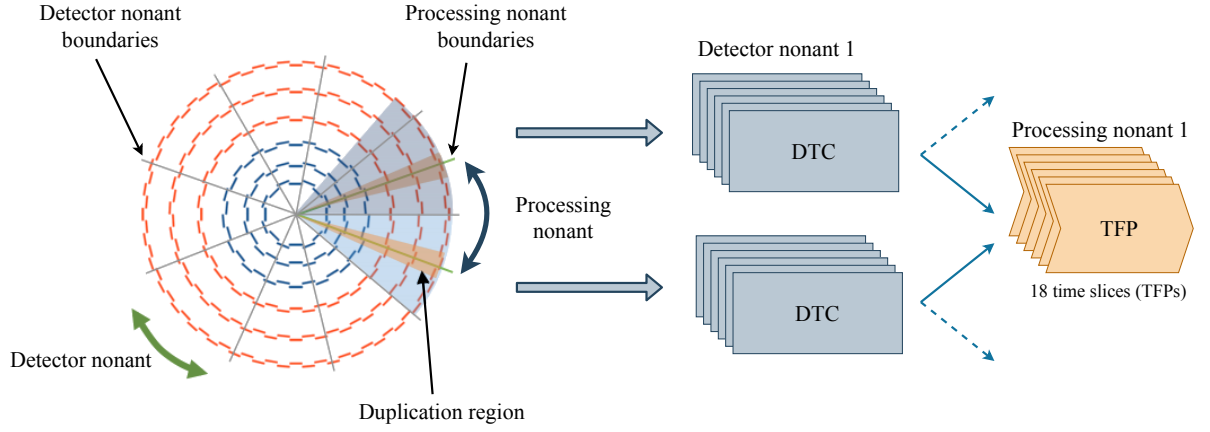


Figure 4.11: Baseline system architecture using DTCs in two neighbouring detector octants to time-multiplex and duplicate stub data across processing octant boundaries before transmission to the Track Finding Processors (TFPs) [51].

To achieve such long-term goals, a big effort was invested in the design of the Outer Tracker modules. The next chapter will mainly focus on the design of the PS module. It will provide a detailed overview of the multiple choices made for each of the silicon sensors, the front-end electronics and the mechanical components. Finally, the remaining chapters will uncover the PS module implementation aspects, going from the module assembly to the module qualification and a description of the systems developed for each of them.

CHAPTER 5

PIXEL-STRIP MODULE DESIGN

The Pixel-Strip (PS) module is one of the two types of modules introduced in the Phase-2 upgrade of the CMS Outer Tracker. It consists of a so-called *bare module* corresponding to a stack of two silicon sensors placed on a support plate and surrounded by dedicated hybrid electronic circuits. The sensor stack is made of a silicon strip sensor (PS-s) and a silicon macro-pixel sensor (PS-p). On the PS-p sensor, sixteen Macro-Pixel ASICs (MPAs) are bump bonded resulting in an assembly referred to as the Macro-Pixel Sub-Assembly (MaPSA). The separation between the PS-s and the MaPSA is defined by Aluminium-Nitride (Al-N) spacers, and the sensor stack support plate, referred to as *base plate*, is made of Carbon Fiber Reinforced Polymer (CFRP) with Aluminium inserts dedicated to the integration on the detector support structures. The bare module is complemented by four hybrid electronic circuits, or simply *hybrids*, to compose a single PS module: two Front-End Hybrids (FEH), one Readout Hybrid (ROH) and one Power Hybrid (POH). Each of the two FEH connect to the eight MPAs hosted on one side of the MaPSA and hosts eight Short Strip ASICs (SSAs) in charge of the strip sensor readout. In addition, one Concentrator Integrated Circuit (CIC) reduces and aggregates data received from the eight corresponding MPAs. As far as data transmission and control is concerned, the ROH hosts the CERN low-power Gigabit Transceiver (lpGBT) ASIC in charge of controlling MPAs and SSAs, and packing data received from the CIC hosted on each FEH. The lpGBT is complemented by a Versatile Link Transceiver Plus (VTRx+) module used for the bidirectional optical data transmission between the module and the back-end system. Finally, to provide power to the whole front-end electronic components, the POH integrates two CERN bPOL chips used for DC-DC conversion and power distribution. A

power cable is bridging the POH to the ROH to compensate for eventual voltage drops across the module. Figure 5.1 shows an exploded view of a PS module, showing the bare module and the hybrid circuits.

The overall PS module design is driven by the requirements of the CMS Tracker Phase-2 upgrade. As described in Chapter 4, the CMS tracker must fulfill the needs of a higher radiation tolerance, increased granularity, reduced material budget, and most importantly the contribution to the CMS Level-1 trigger system. As far as the Outer Tracker is concerned, radiation tolerance and increased granularity are ensured by a decisive choice of both strip and macro-pixel silicon sensors. The reduced material budget is achieved by the design of light-weight electronics and mechanical components. Finally, the contribution to the Level-1 trigger is guaranteed by the implementation of the on-board p_T discrimination logic described in Section 4.1.1. In this sense, every single component of the PS module is subject to a crucial interplay between requirements and design choices. This chapter provides a detailed description of the PS module, motivating and uncovering the most important aspects of the design.

5.1 Silicon Sensors

The main driving aspect of the PS module silicon sensors design is radiation hardness. The foreseen high luminosity environment calls for a decisive choice of sensor material and properties to ensure an efficient operation of the detector over its lifetime. An R&D campaign conducted over 10 years concluded that silicon strip and macro-pixel sensors made in n-on-p technology using high resistive float zone silicon are the best candidates for the Outer Tracker modules. Such sensors should provide the needed performance over their full projected lifetime of 10 years at the highest estimated fluences, ensuring sufficient signal-to-noise ratio for minimum ionizing particles at manageable operating conditions [52, 53].

Two types of sensors are foreseen for the PS module: an AC-coupled strip sensor (PS-s) and a DC-coupled macro-pixel sensor (PS-p). Both sensors are fabricated on 6" wafers either in pre-thinned p-type float zone wafers or thinned p-type wafers with a target bulk and backside implant thicknesses both depending on the wafer type. They include robust contact pads compatible with ultrasonic aluminium wire wedge bonding to withstand probing during the quality assurance phase. In addition, high voltage stability and low current operation is achieved by dedicated guard rings and appropriate p^+ edge implants

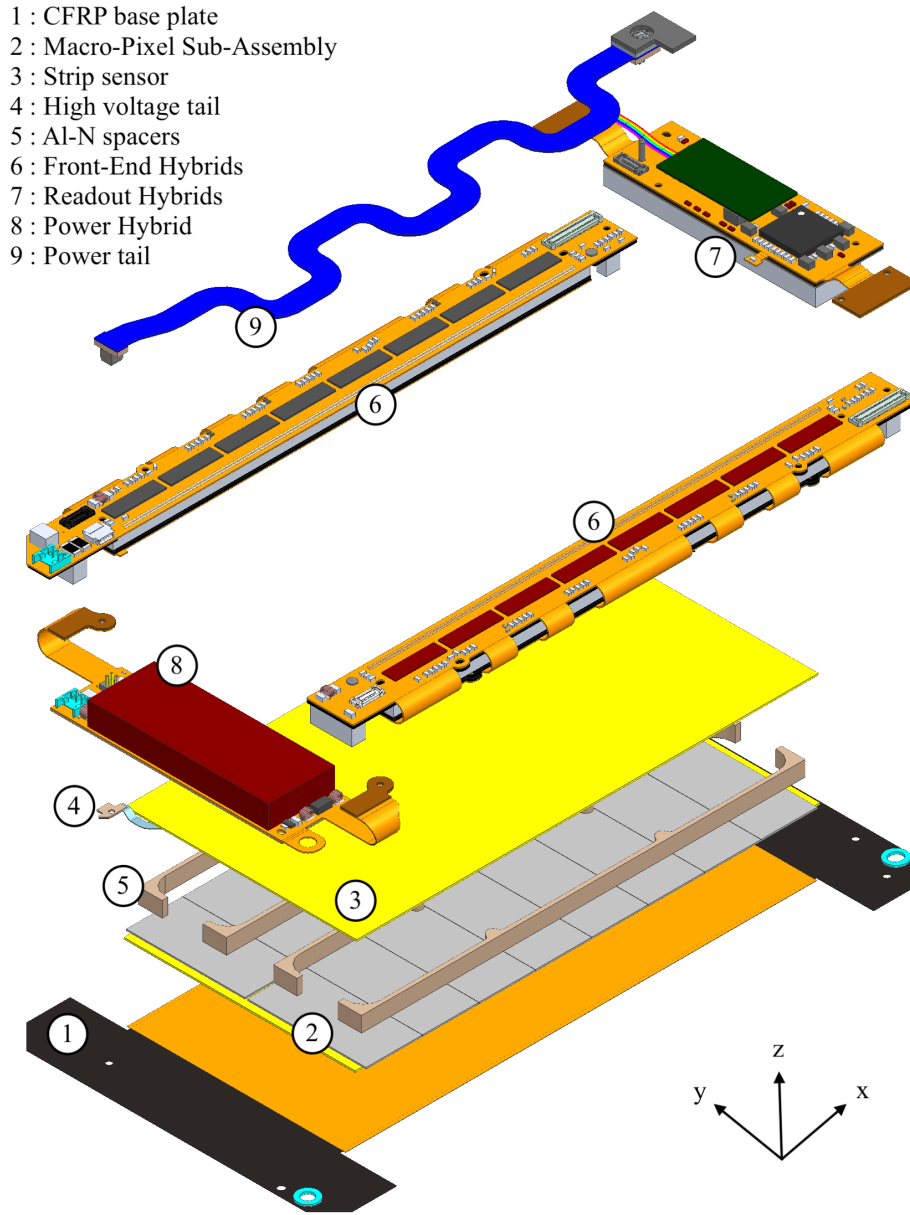


Figure 5.1: Exploded view of a PS module. The reinforced carbon fiber baseplate is shown in black, covered by an isolating kapton sheet shown in orange. The silicon sensors are shown in yellow with the macro-pixel sensor being hidden underneath the set of sixteen Macro-Pixel ASICs shown in grey. The eight Short Strip ASICs are shown in grey and red on each of the Front-End Hybrids. On the Readout Hybrid, the lpGBT ASIC is shown in black while the VTRx+ module is shown in green. The bPOL chips are hidden below the POH shield shown in red. Finally, the power tail connecting the POH to the ROH is shown in blue. [48]

to protect the sensor's active area during dicing. Finally, the backside p^+ implant is covered with a uniform aluminium metallization of wire bondable quality with good ohmic contact to the bulk of the sensor. Figure 5.2 shows a corner of the PS-s and PS-p designs.

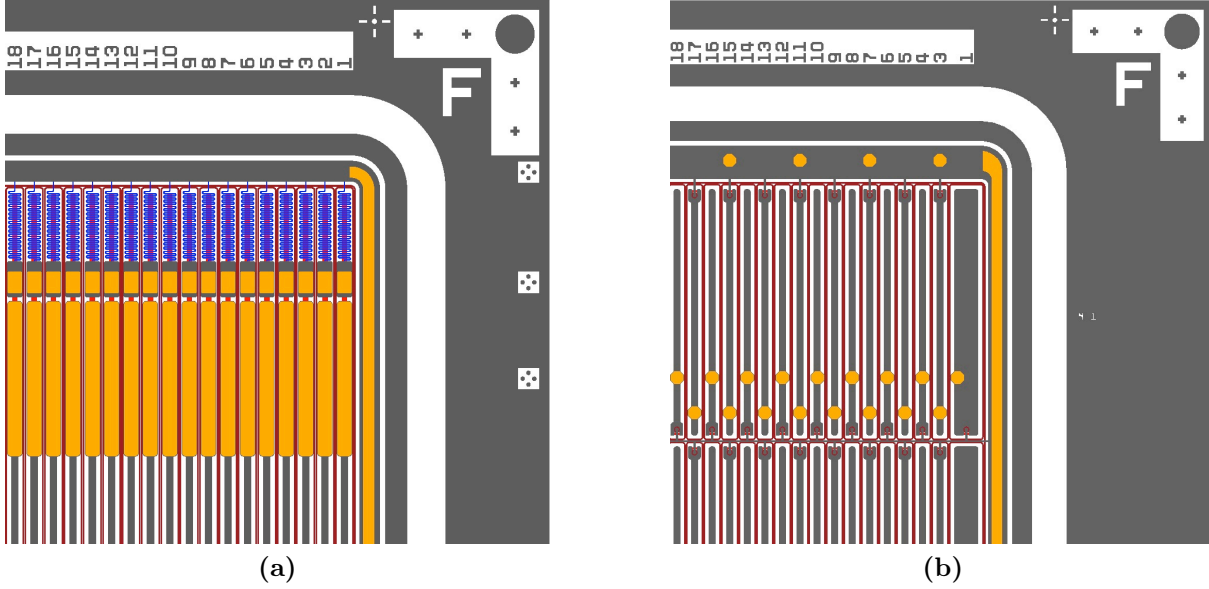


Figure 5.2: Corner of a PS-s sensor (a) and a PS-p sensor (b). L-shaped and F-shaped alignment patterns are placed at each corner. Dark grey areas are covered with aluminium, orange areas represent openings in the passivation (contact pads and bias ring) and red areas are p-stop implants. The biasing of each channel is accommodated by poly-silicon resistors (blue) for strip sensors and by punch-through structures for the macro-pixels.

5.1.1 Common Periphery

The PS-s and PS-p sensors share a set of common bias, guard and edge ring layout properties. A bias ring with $75\ \mu\text{m}$ implant width and asymmetric overhangs surrounds the active area. It provides a large opening in the passivation for wirebonding while accommodating the contacts to the polysilicon bias resistor in the PS-s. High voltage stability and electric field shaping is achieved through a single floating guard ring with an asymmetric overhang and corner openings in the metallization. Finally, a large and highly doped p-type implant protects the edge of the sensors and provides alignment marks used for the relative sensor-to-sensor alignment while assembling the PS bare module as will be discussed in Chapter 6.

5.1.2 Active Strip Area

The PS-s sensor, shown as (3) in Figure 5.1, has an active thickness of $290\text{ }\mu\text{m}$ for a total surface of $98.14 \times 49.16\text{ mm}^2$. It provides 920 AC-coupled strips on each of its long sides. The strip length is 23.472 mm and the AC pads are at least $62\text{ }\mu\text{m}$ wide to ensure reliable wirebonds. The strip pitch is $100\text{ }\mu\text{m}$ with a width-to-pitch ratio of 0.25. The latter is particularly important as it affects the high voltage stability and defines the interstrip capacitance which represents an important source of electronic noise for the readout chips. Finally, the strip implants are connected to the global biasing scheme using polysilicon bias resistors.

5.1.3 Active Macro-Pixel Area

Similarly, the PS-p sensor has an active thickness of $290\text{ }\mu\text{m}$ for a total surface of $98.74 \times 49.16\text{ mm}^2$. It provides a macro-pixel matrix of dimension 32×960 DC-coupled cells. The macro-pixel length is $1467\text{ }\mu\text{m}$ with a pitch of $100\text{ }\mu\text{m}$ with the exception of wide edge cells which yield a $200\text{ }\mu\text{m}$ pitch. The width-to-pitch ratio is 0.25 for the normal cells and 0.625 for the wide edge cells. Finally, Punch Through Structures (PTS) are used to connect each individual pixel to the global bias grid.

5.2 Front-End Electronics

As mentioned in the previous section, the PS-s sensor is segmented into 1920 strips and the PS-p sensor into 32 rows of 960 macro-pixels. This results in a large amount of data to be processed by the front-end electronics. This is done via a complex front-end system architecture, described in the chapter introduction, that starts with the individual strip and pixel readout and ends with the transmission of the aggregated data to the back-end system over the optical link. The pixel readout as well as the p_T discrimination logic is handled by the set of MPA chips bump bonded onto the PS-p sensor, forming the so-called MaPSA. The strip readout of each side is handled by SSA chips hosted on two FEH positioned along the wirebond pads of the PS-s sensor. In addition, each FEH hosts a CIC chip in charge of aggregating data received by the eight corresponding MPA chips. The aggregation of data coming from each side, left and right, of the module is further performed by the lpGBT chip, before being transmitted over the optical link to the back-end system. Figure 5.3 shows a simplified diagram of the data flow on the PS module, indicating how each of the L1 and stub data flows across the various chips and processing blocks until the back-end system.

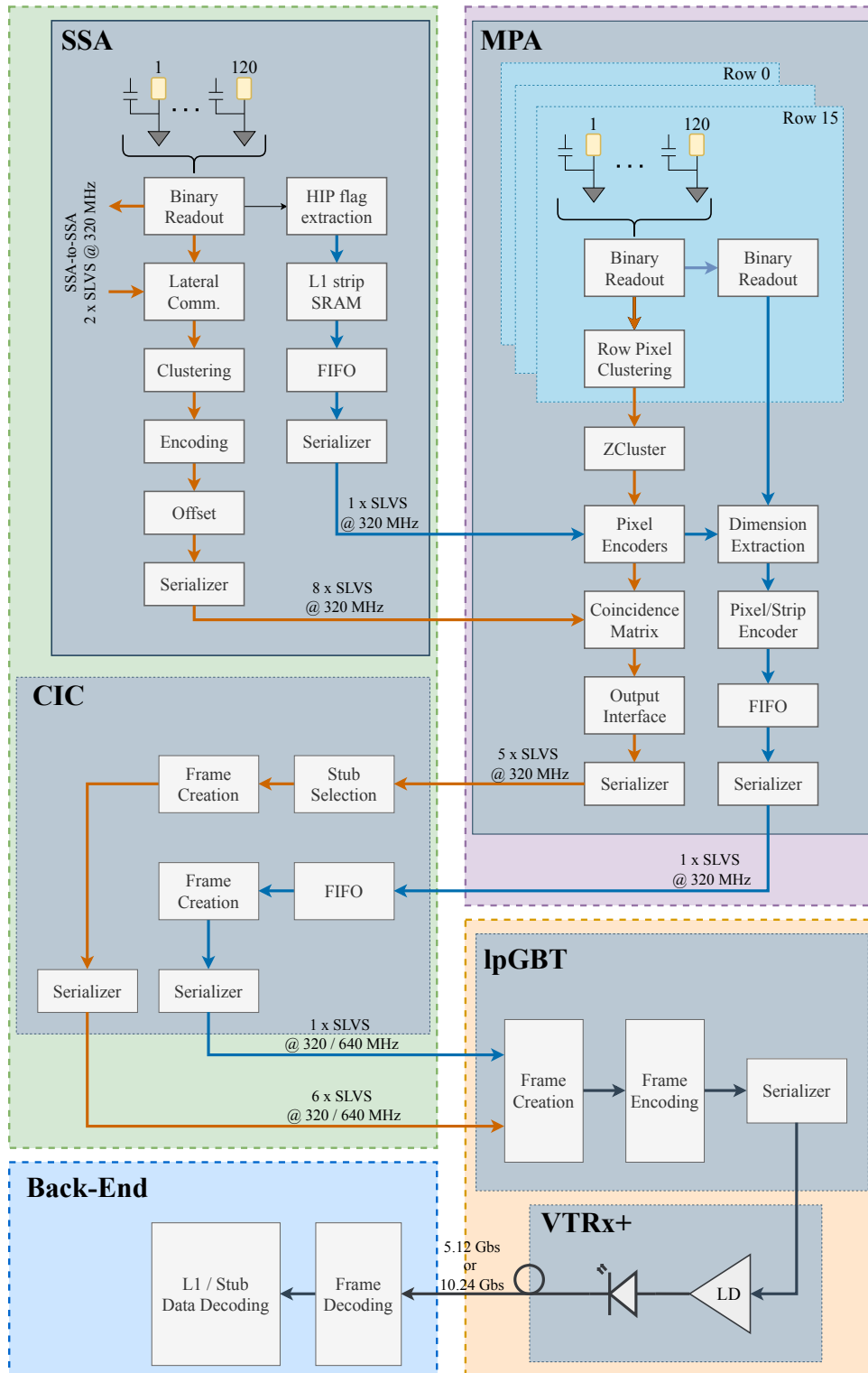


Figure 5.3: Simplified PS module data flow diagram, indicating how each of the L1 (blue arrows) and the stub (orange arrows) data flows across the module, between the MaPSA (purple box), the FEH (green box) and the ROH (orange box), until the back-end system.

5.2.1 Macro-Pixel Sub-Assembly

The Macro-Pixel Sub-Assembly (MaPSA), shown as (2) in Figure 5.1, is the association of a PS-p macro-pixel sensor with 16 MPAs. The latter are bump-bonded to the sensor and arranged in two rows of eight. Each MPA chip reads out 1920 pixels arranged in 16 rows and 120 columns. To isolate the MPAs from the sensor high voltage, a thin strip of kapton tape is installed between the edge of the PS-p sensor and the edge of the MPA wire bond pads.

Macro-Pixel ASIC

As mentioned before, the Macro-Pixel ASIC (MPA) is a binary readout chip dedicated to the readout of the PS-p sensor. Figure 5.4 shows a top level block diagram of a single MPA. In addition, the MPA implements the p_T discrimination logic in order to correlate signals from the PS-s and PS-p sensors and generate the corresponding stubs.

Each MPA is connected to a 16×120 pixel matrix and is composed of an analogue pixel region of $12.2 \text{ mm} \times 23.47 \text{ mm}$ and a digital periphery logic of about 2 mm that resides on the edge of the chip. Besides service blocks such as Inter Integrated Circuit (I²C) chip configuration interfaces, charge injection test circuits, and advanced clock distribution trees, the periphery logic provides blocks for event processing at the bunch crossing frequency. First in the periphery is the pixel digital circuit which serves as an interface between the analogue front-end and the digital processing logic. Three acquisition modes are implemented to digitalize the analogue pulse signal: the *Edge* sensitive mode, the *Level* sensitive mode and the 15-bit ripple counter mode. The Edge sensitive mode is based on an edge detector that generates a single bunch-crossing digital pulse, synchronous with the 40 MHz clock, when the pulse signal exceeds a defined threshold. For the Level sensitive mode, the digital output in contrast to the previous mode depends on the duration of the analogue pulse signal and remains high as long as the discriminator output stays high. Finally, the 15-bit ripple counter mode is an asynchronous counting mode based on an external shutter signal controlled through fast command signals. It allows to asynchronously count the number of pulses detected by the analogue circuit within a time window defined by the shutter control. The corresponding counters can either be accessed using the I²C interface or can be sent asynchronously over the stub data path every eight bunch crossings, replacing the stub data by the counter values. This feature is particularly useful for calibration purposes as it is uncomparably faster than the I²C readout and allows the readout of all counters in less than 500 μs .

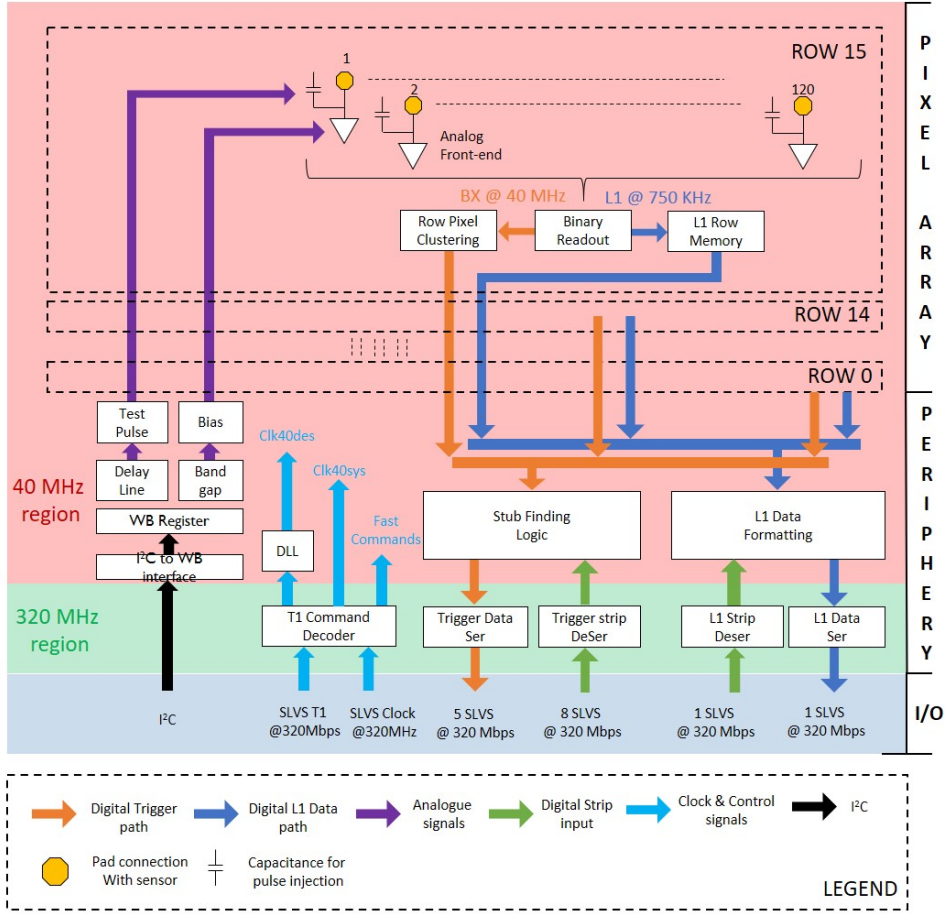


Figure 5.4: Macro-Pixel ASIC top level block diagram [54].

At its core, the MPA digital processing logic can be divided into three functional blocks: strip data deserialization, L1 data formatting and stub finding. In the first block, the hit data received from the SSA over a total of 9 SLVS lines operating at a rate of 320 Mbps is deserialized and branched into the L1 formatting and the stub finding blocks. The L1 formatting and the stub finding blocks operate in parallel. The first one stores hit information from both pixel and strip sensors without any data reduction. Upon reception of a Level-1 trigger signal, it reduces the pixel and strip hit information into a format, shown in Figure 5.5(a). The L1 data frame includes a fixed header and a payload of variable length that only includes the pixel and strip hit cluster positions and widths. It is further serialized on a single SLVS line at a rate of 320 Mbps towards the CIC. On the other hand, the stub finding logic receives, synchronously with the 40 MHz bunch crossing frequency, the same hit information as the L1 data formatting block. Using both pixel and strip hit data, it applies the stub finding logic, looks for coincidences between the top and bottom sensors within a programmable coincidence window, and eventually generates the corresponding stub information. A stub is summarized with the particle incidence

coordinates (seed) and the bending angle (bend) in the $r - \phi$ plane of the particle. The stub finding algorithm only selects stub information that fulfill the requirement of a given bending threshold and serializes them over five SLVS lines at a rate of 320 Mbps towards the CIC in the format shown in Figure 5.5(b). The stub data packet transmitted contains the stub found in two consecutive bunch crossings, indicating the number of stubs detected in each of them. Finally, the logic also provides more configurable selection criteria, such as setting a limit on the size of the clusters to be processed or applying an offset to the stub correlation window. This allows to accommodate for large signal clusters or non-trivial geometrical orientations of the modules, respectively.

Header							Payload								T
Start sequence		Error	L1 ID		Nb Sclust	Nb Pclusr	List of Sclust				List of Pclust				
							Sclust address	Width	MIP		Pclust address	Width	Z info		
Start sequence: 18 bits at '1'		0	0	0		0				*****				*****	
19 bits		2 bits	9 bits	1	5 bits	5 bits	1	7 bits	3 bits	1		7 bits	3 bits	4 bits	

(a)

MPA trigger data						
word 2	B5 ⁰	Z5 ³	Z5 ²	Z5 ¹	Z5 ⁰	b7
	S5 ²	S5 ¹	S5 ⁰	B5 ²	B5 ¹	b6
	S5 ⁷	S5 ⁶	S5 ⁵	S5 ⁴	S5 ³	b5
	B4 ⁰	Z4 ³	Z4 ²	Z4 ¹	Z4 ⁰	b4
	S4 ²	S4 ¹	S4 ⁰	B4 ²	B4 ¹	b3
	S4 ⁷	S4 ⁶	S4 ⁵	S4 ⁴	S4 ³	b2
	B3 ⁰	Z3 ³	Z3 ²	Z3 ¹	Z3 ⁰	b1
word 1	S ₂	S3 ¹	S3 ⁰	B3 ²	B3 ¹	b0
	S3 ⁶	S3 ⁵	S3 ⁴	S3 ³	S3 ²	b7
	Z2 ³	Z2 ²	Z2 ¹	Z2 ⁰	S3 ⁷	b6
	S2 ¹	S2 ⁰	B2 ²	B2 ¹	B2 ⁰	b5
	S2 ⁶	S2 ⁵	S2 ⁴	S2 ³	S2 ²	b4
	Z1 ³	Z1 ²	Z1 ¹	Z1 ⁰	S2 ⁷	b3
	S1 ¹	S1 ⁰	B1 ²	B1 ¹	B1 ⁰	b2
	S1 ⁶	S1 ⁵	S1 ⁴	S1 ³	S1 ²	b1
	S ₁	N ²	N ¹	N ⁰	S1 ⁷	b0
	line 1	line 2	line 3	line 4	line 5	

S_x : synchronisation bit (S₁ always '1', S₂ always '0'),

N^y : bit y of stubs number in the 1st bunch crossing

SX^y : bit y of Stub address on 8bits,

BX^y : bit y of Bend info on 3bits,

ZX^y : bit y of Z info on 4 bits

→ up to 5 stubs / 2 bunch crossings

(b)

Figure 5.5: MPA L1 data path data format (a) and stub data output format over two bunch crossings on 5 parallel lines (b) [54].

5.2.2 Front-End Hybrids

The Front-End Hybrids (FEH), shown as (6) in Figure 5.1, are flexible electronic circuits laminated onto CFRP stiffeners and folded around spacers, except for the 1.6 mm module variant where no spacer is used. Every single PS module is made of two FEH hosting eight SSAs and a single CIC each. Individual SSAs provide 120 input channels which connect to the PS-s via dedicated wire bonds to collect and process the corresponding signals. Moreover, data lines from each SSA are routed from the top side of the hybrid circuit to the bottom side and connected via wirebonds to their paired MPAs where the p_T discrimination logic is implemented. Also, in order to cover the interface between SSAs, lateral communication is included such that neighbouring SSAs can exchange hit data, thus avoiding inefficiencies in the stub finding logic for particles crossing the inter-chip region. As far as MPA data transmission is concerned, the FEH provides, on the bottom side, connections to the MPAs via wire bonds, and corresponding data lines are routed to the CIC. In addition, for hybrid circuit qualification purposes as discussed in Chapter 8, underneath the PS-s wirebond pads, a so-called *antenna* pad is integrated and purposed for the SSA analogue traces testing. It is capacitively coupled to each wirebond pad and allows the injection of a small amount of charge that can be used to detect shorts and opens among the input traces of the SSA. Finally, each FEH provides two grounding spring contacts on the bottom side dedicated to the grounding of the front-end electronics to the module carrier plates or the detector support structures. It should be mentioned that, while both FEH provide common low voltage power circuitry, only one of them provides a high voltage bias circuit necessary for the PS-s and PS-p biasing.

Short Strip ASIC

As previously mentioned, the Short Strip ASIC (SSA) is a binary readout chip dedicated to the readout of the PS-s sensor. Figure 5.6 shows a top level block diagram of a single SSA. It provides, at the bunch crossing frequency, encoded strip signal information to its paired MPA to be used in the p_T discrimination logic. Each SSA connects to 120 strips and the strip signals are discriminated in the analogue circuit via a double threshold binary system. The lower threshold, or detection threshold, provides sensitivity to particles with energy deposits down to $1/4$ of a MIP. The higher threshold, around 1.5 MIP, distinguishes signals generated by High Ionizing Particles (HIPs). An edge sensitive circuit is used to digitalize and sample the discriminator pulses at the bunch crossing frequency, and the corresponding sampling clock phase can be adjusted with a precision of 200 ps. This guarantees no dead cycles in case of consecutive particle hits caused by

pileup. In addition, similarly to the MPA, the digital sampling can be selected among three modes: *Edge* sensitive mode, *Level* sensitive mode, and 15-bit ripple counter mode that operate in exactly the same way as described previously, with the ripple counter information being accessible either asynchronously via the stub data path or the I²C interface.

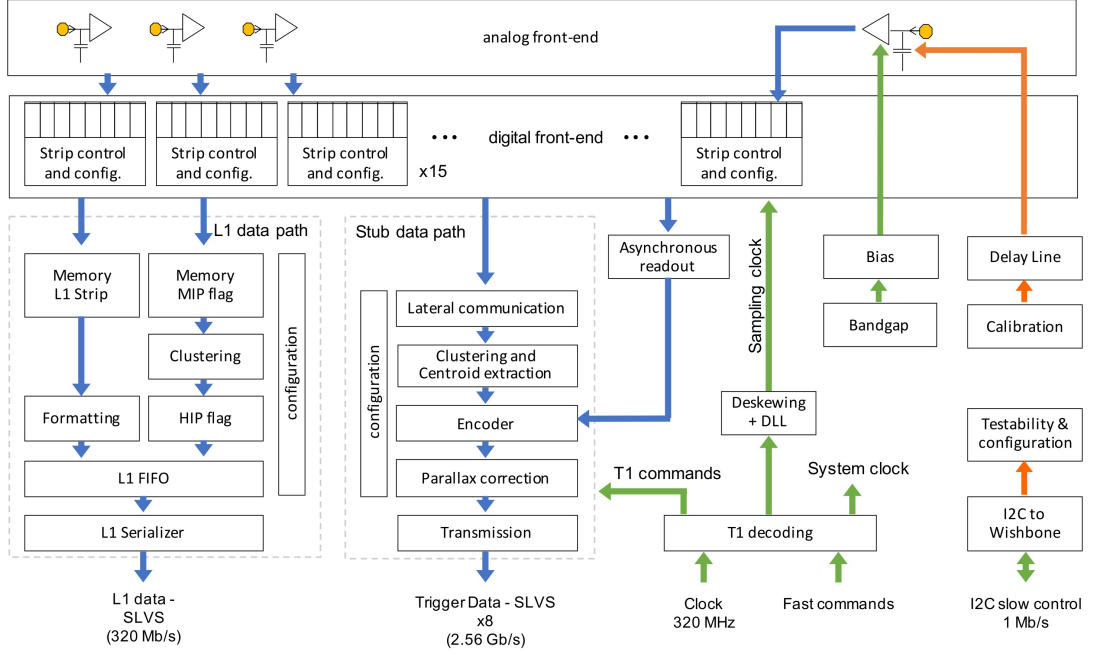


Figure 5.6: Short Strip ASIC top level block diagram. Revised from [55].

Internally, the digitized hit information follows two data paths: the stub data path and the L1 data path. In the stub data path, the hit data is encoded into clusters with corresponding coordinates and is sent to the paired MPA at the 40 MHz bunch crossing frequency over eight SLVS lines at a rate of 320 Mbps according to the format shown in Figure 5.7(b). Each line transmits sequentially the coordinate expressed on 7 bits followed by the half strip coordinate bit, giving a resolution of half strip. In the L1 data path, hit data is stored internally and only transmitted upon reception of a Level-1 trigger signal over a single SLVS line at a rate of 320 Mbps in the format shown in Figure 5.7(a). The data packet has a fixed length and includes a fixed header, L1 and bunch crossing counters to ensure synchronization with the MPA, and the sequence of 120 strip hits complemented by a flag for the HIP information. Finally, similarly to the MPA chip, the SSA provides service blocks which cover I²C chip configuration interfaces, charge injection test circuits and advanced clock distribution trees.

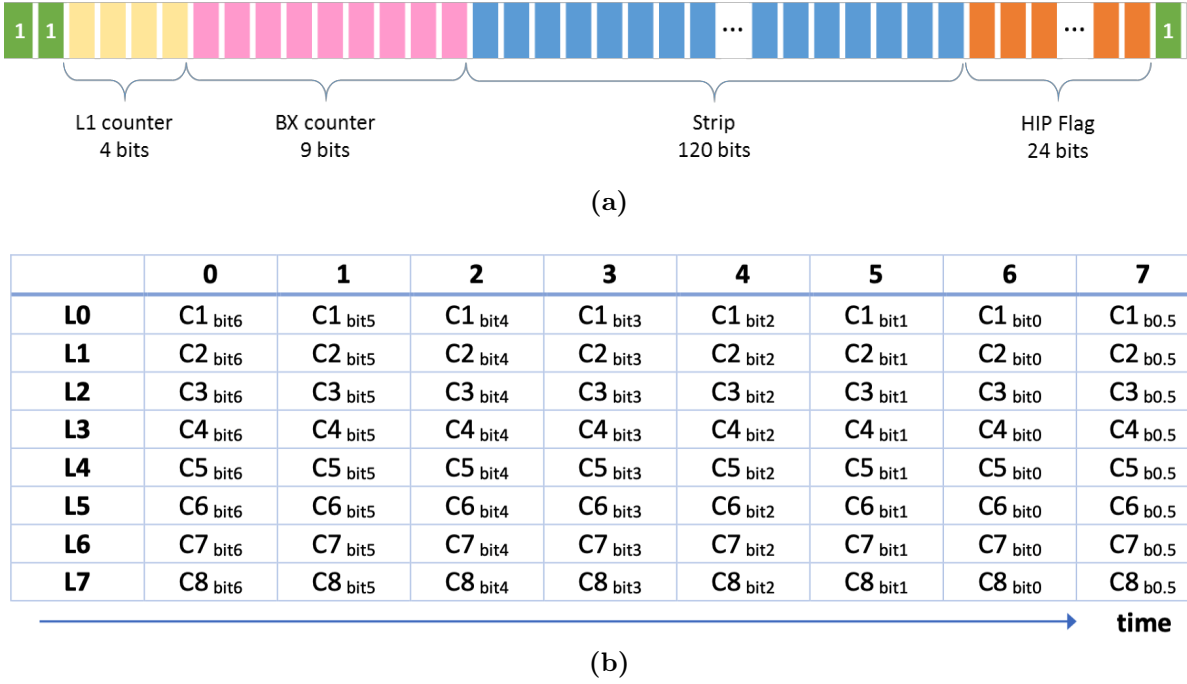


Figure 5.7: SSA L1 data path data format (a) and stub data output format over two bunch crossings on 5 parallel lines (b) [55].

Concentrator Integrated Circuit

The Concentrator Integrated Circuit (CIC) is a front-end data aggregator hosted on each FEH with the main purpose of handling, compression and eventually truncation of L1 and stub data transmitted by the MPAs. Figure 5.8 shows a top level block diagram of a single CIC.

The chip architecture features two independent data paths: the trigger (stub) data path and the L1 data path. The input to the trigger data path consists of five SLVS lines per MPA while the input to the L1 data path is a single SLVS line per MPA, resulting in a total of 48 lines per module side. All six data lines operate at a rate of 320 Mbps and in both cases, the trigger and L1 data lines are aligned to the 40 MHz sampling clock in order to ensure an optimal data sampling. In the trigger path, stub data received from the MPAs is deserialized, decoded and filtered such that only stubs corresponding to high p_T particles are further transmitted. A stub data frame is then created and further transmitted to the lpGBT over five SLVS lines following the format shown in Figure 5.9(b). On the L1 path, hit data is decoded and buffered until a Level-1 trigger signal is received. Upon reception of a trigger signal, a hit data frame is created and further transmitted to the lpGBT over a single SLVS line following the format shown in Figure 5.9(a). The

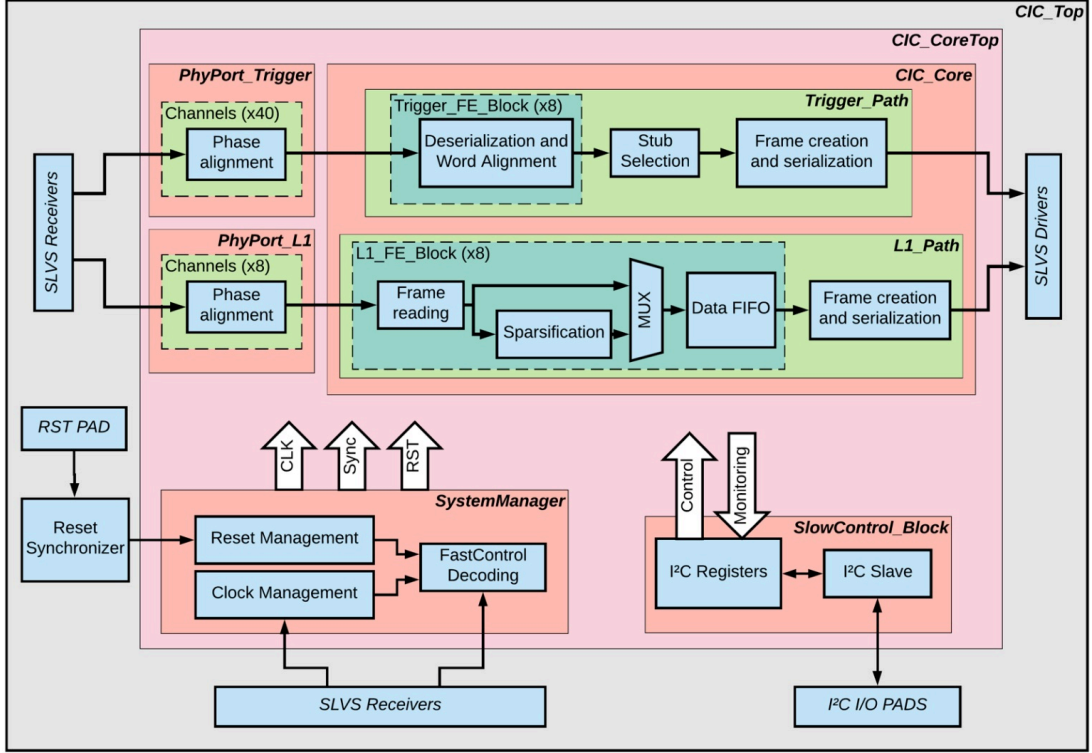


Figure 5.8: Concentrator Integrated Circuit top level block diagram [56].

output format of L1 and stub data is standardized such that the subsequent processing is simplified. It should be mentioned that the CIC output lines can operate at a rate of either 320 Mbps or 640 Mbps depending on the module configuration. In particular, the 640 Mbps bandwidth is crucial for the modules located in regions yielding very high hit occupancies. Finally, the data paths are complemented by two service blocks, namely the System Manager and the Slow Control where the former handles fast command signals decoding, reset and clock distribution while the latter provides the I²C interface.

5.2.3 Read-Out Hybrid

The Readout Hybrid (ROH), shown as (7) on Figure 5.1, is a flexible electronic circuit laminated onto CFRP stiffeners and complemented by an Al-N spacer placed on the bottom side. The circuit integrates the low-power Gigabit Transceiver (lpGBT) ASIC for data aggregation and serialization and a pluggable Versatile Link Plus (VTRx+) opto-transceiver module for optical data communication. In addition, a temperature sensor is located on a tail to be placed in contact with the PS-s sensor. The ROH is electrically connected to both FEH via micro-connectors that act as an interface for CIC data, clock and reset lines as well as low voltage power distribution.

Header										Payload									
Start sequence		Error/Status bits					L1 ID	Nb ScIust		Nb Pclusr		List of ScIust				List of Pclust			
Start sequence: 27 bits at '1'		0	MPA 8	MPA 7	MPA 6	MPA 5	MPA 4	MPA 3	MPA 2	MPA 1	CIC					Chip ID	Pclust address	Width	Z info
28 bits		9 bits					9 bits	7 bits	1	7 bits	1	3 bits	7 bits	3 bits	1	3 bits	7 bits	3 bits	4 bits

(a)

CIC PS trigger output (5G FEC5)											
L1	L2	L3	L4	L5	L6						
C	Status					BX1					
Status				BCID							
BCID											
BCID				Nb Stubs							
Nb Stubs				O1 ²	O1 ¹						
O1 ⁰	A1 ²	A1 ¹	A1 ⁰	S1 ⁷	S1 ⁶						
S1 ⁵	S1 ⁴	S1 ³	S1 ²	S1 ¹	S1 ⁰						
B1 ²	B1 ¹	B1 ⁰	Z1 ³	Z1 ²	Z1 ¹						
...					...	...					
B15 ²	B15 ¹	B15 ⁰	Z15 ³	Z15 ²	Z15 ¹	BX8					
Z15 ⁰	O16 ²	O16 ¹	O16 ⁰	A16 ²	A16 ¹						
A16 ⁰	S16 ⁷	S16 ⁶	S16 ⁵	S16 ⁴	S16 ³						
S16 ²	S16 ¹	S16 ⁰	B16 ²	B16 ¹	B16 ⁰						
Z16 ³	Z16 ²	Z16 ¹	Z16 ⁰	0	0						
0	0	0	0	0	0						
0	0	0	0	0	0						
0	0	0	0	0	0						
C	Status					BX9					
Status				BCID							
BCID											
BCID				Nb Stubs							
Nb Stubs				O1 ²	O1 ¹						
O1 ⁰	A1 ²	A1 ¹	A1 ⁰	S1 ⁷	S1 ⁶						
S1 ⁵	S1 ⁴	S1 ³	S1 ²	S1 ¹	S1 ⁰						
B1 ²	B1 ¹	B1 ⁰	Z1 ³	Z1 ²	Z1 ¹						

Definitions	
C	CIC conf. : MPA or CBC
Status	Status bits
BCID	Bunch clock ID
Nb Stubs	Number of stubs in block
Ox ^Y	BX offset for stub X (bit Y)
Ax ^Y	Chip ID for stub X (bit Y)
Sx ^Y	Stub address for stub X (bit Y)
Bx ^Y	Bend info for stub X (bit Y)

(b)

Figure 5.9: L1 Data path data format (a) and stub data output format over two bunch crossings on 5 parallel lines (b) [55].

Low-power Gigabit Transceiver

The low-power Gigabit Transceiver (lpGBT) is a radiation tolerant ASIC that implements multipurpose high speed bidirectional optical links. Figure 5.10(a) shows the ASIC architecture and top level block diagram. It supports 2.56 Gbps links on the downlink (from the back-end system to the module) and 5.12 or 10.24 Gbps links on the uplink (from the module to the back-end system). The two uplink data rates correspond to the previously mentioned possible CIC output data rates of 320 Mbps and 640 Mbps, respectively. The lpGBT connects to the CICs on each FEH through Electrical Ports or Links (ePorts or eLinks). The latter use the CERN Low Power Signaling (CLPS) [57] which features programmable signal amplitudes, data rates and power consumptions. Each ePort features

three transmission lines: Receiving ePorts (ePortRx), Transmitting ePorts (ePortTx) and Clock ePorts (ePortClk). Data from the CIC to the lpGBT (uplink), namely L1 and stub data, are transmitted on six dedicated ePortRx lines. Data from the lpGBT to all the front-end chips (downlink), such as fast command signals, are transmitted on a single dedicated ePortTx lines, one for the CIC and a common one for MPAs and SSAs. Finally the clock signals required by all the front-end chips are transmitted on single dedicated ePortClk lines, one for the CIC and one for the SSAs. The stub and L1 data transmitted over the ePortRx corresponding to each MPA are first subject to a phase alignment in order to ensure an optimal sampling of the data before being deserialized and aggregated into a large data frame which is further encoded and transmitted over the optical link to the back-end system via the VTRx+. The fast command signals, which are transmitted from the back-end system to the module over the optical link, are extracted from the deserialized and decoded downlink data frame, and transmitted to the front-end chips. The lpGBT downlink data frame has a fixed 64 bits structure and is divided into a header and multiple data fields used for the chip control and for the transmission of fast commands. On the other hand, the uplink data frame has a structure of variable length that depends on the lpGBT communication settings such as the data rate. It is divided into a fixed header, an IC field, and data fields dedicated to the L1 and stub data. Finally, besides the data paths, the lpGBT provides a set of configuration, control and monitoring blocks that cover functionalities such as I²C configuration interfaces that connect to each front-end chip, general purpose programmable input or output ports (GPIOs) used for the control of the reset lines, and Analogue-to-Digital Converters (ADCs) to monitor voltage levels inside the lpGBT or read out external components such as the ROH temperature sensor.

Versatile Link Transceiver Plus

The Versatile Link Transceiver Plus (VTRx+) is a radiation tolerant optical link module providing high speed data transmission for readout and control. Figure 5.10(b) shows an example system including the VTRx+. The module is based on radiation-hard Laser Diode Driver (LDD) and Transimpedance Amplifier (TIA) ASICs as well as commercial Vertical-Cavity Surface-Emitting Lasers (VCSEL) and p-in-n photodiode (PD) components [58]. The VTRx+ connects to the back-end system via an optical fiber. It is designed to operate together with the previously described lpGBT, but other types of data transmitters can be supported. In the case of the lpGBT pairing, the target operating data rates on the uplink and downlink are set by the latter.

5.2.4 Power Hybrid

The Power Hybrid (POH), shown as (8) in Figure 5.1, is a flexible electronic circuit laminated onto glass-reinforced epoxy laminate material (FR4). It handles power distribution for all the PS module electronic components. Figure 5.11 shows a sketch of the powering scheme used in the PS module.

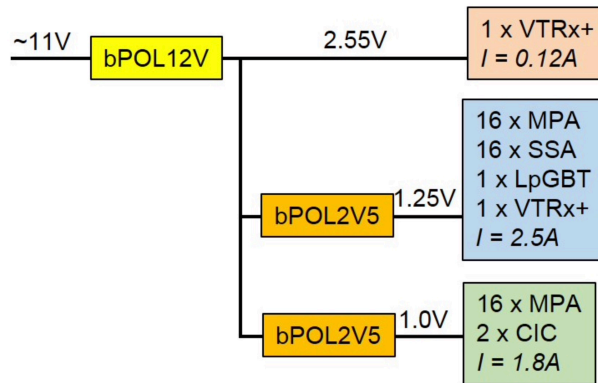


Figure 5.11: Sketch of the cascaded DC-DC conversion scheme used in the PS Readout Hybrid, showing the nominal voltages and currents during operation [38].

It is based on cascaded DC-DC conversion stages that produce a set of local supply voltages from an input 11 V supply line. Each conversion stage is based on the CERN buck Point-Of-Load (bPOL) DC-DC converters which are single phase synchronous buck converters designed for flawless functionality in a harsh radiation and magnetic field environment. In the case of the PS module, three set of voltages need to be provided: 1.25 V for the SSA, the lpGBT and the analogue part of the MPA, 1.0 V for the digital part of the MPA and the CIC, and 2.55 V for the VTRx+. In the first conversion stage, a bPOL12V converts the 11 V input into a 2.55 V output fed to the VTRx+ and to the second conversion stage. The second stage is divided into two parts that both employ a bPOL2V5 converter due to the larger currents to be supplied. They convert the 2.55 V input into the required 1.25 V and 1.0 V outputs. The bPOL converters are complemented with a set of air-core inductors as energy storage element, passive filter components and an electro-magnetic shield. The electro-magnetic shield is of particular importance as it protects the silicon sensors and the front-end electronic components from stray electromagnetic radiation caused by the switching DC-DC converters.

5.3 Module Mechanics

The mechanical design of the modules is largely driven by the objective of making it compact and self-contained such as the power conversion, front-end electronics and optical data transmission are all on-board and not shared with other modules. The use of Al-N material for the four spacers between the MaPSA and the PS-s sensor (shown as (5) in Figure 5.1) as well as for the front-end hybrid fold ensures good heat conduction from the sensor and hybrids, and very low stress on the glue joints between sensors, spacers and CFRP parts. This is due to the high thermal conductivity and low coefficient of thermal expansion (CTE) of the material. The good thermal performance of the PS module is also ensured by the use of high modulus and therefore high thermal conductivity CFRP material for each of the hybrid stiffeners and the 200 μm module base plate. In addition, the use of glue layers as thin as possible permit low thermal impedance and provides solid structural strength. For the sensor to hybrid connection, pitch adapters are avoided with the use of direct wirebonding, simplified by a bond pad pitch on the hybrid matching the one on the sensor. The risk of wirebond damage due to handling or resonant vibrations is mitigated through encapsulation. In addition, a robust connection between the adjacent hybrids is ensured with high reliability connectors. High voltage (HV) isolation between the MaPSA and the base plate is guaranteed by the use of a Kapton MT polyimide film. This shall provide reliable barrier up to the eventual maximum sensor voltage of 800 V that is considered. Finally, the HV bias connection to the PS-s sensor uses a small flex circuit glued to the back of the bare sensor. It is wirebonded to the sensor backplane on one end, and connected to the FEH providing the HV bias circuit on the other end. On the other hand, the PS-p sensor bias connection is done via a direct wirebonding of the sensor backplane to the FEH.

As far as thermal performance is concerned, the main module components, namely the sensors, the spacers, the carbon fiber stiffeners and the base plate, are chosen such that their coefficient of thermal expansion are well matched: 3 ppm/ $^{\circ}\text{C}$ for silicon, 4 ppm/ $^{\circ}\text{C}$ for Al-N, and 0 ppm/ $^{\circ}\text{C}$ for carbon fiber. This allows for minimal differential expansion, of the order of few microns, between the baseplate and the PS-p sensor, the sensor spacers and the PS-s, and the hybrid spacers and the stiffener. Finally, a crucial thermal performance consideration is the module thermal runaway. The thermal runaway is defined as a self-reinforcing thermal reaction that occurs in a system, leading to an uncontrolled temperature increase (ie: a situation in which insufficient cooling power leads the module into a temperature rise in a positive feedback loop since the leakage current increases exponentially with temperature). This happens when the coolant temperature is increased. In

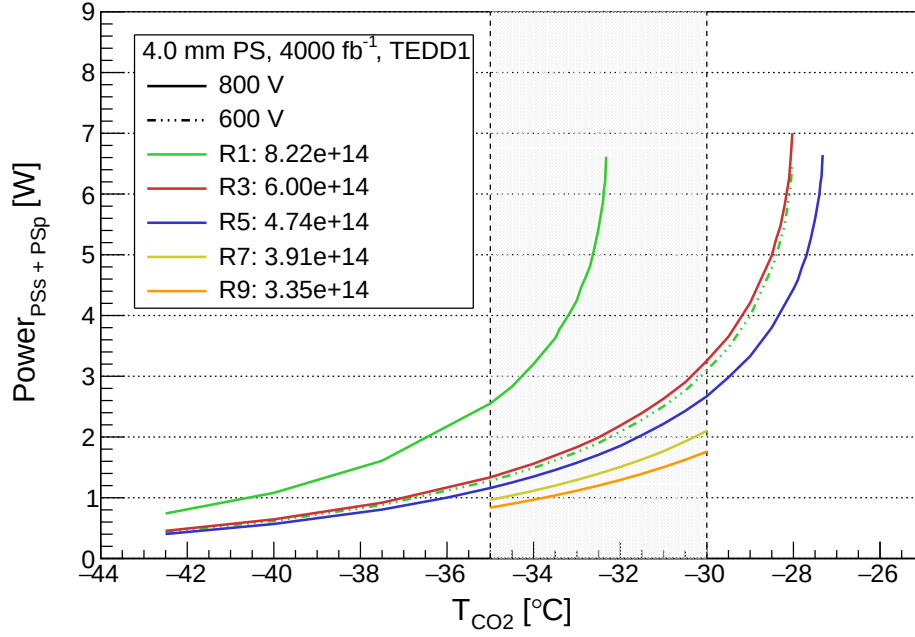


Figure 5.12: Expected thermal runaway turn-on temperatures for a PS module located on the TEDD1 structure on each of rings 1, 3, 5, 7 and 9 at expected nominal head loads after 4000 fb⁻¹ of integrated luminosity and biased at 800V [48].

the case of the Outer Tracker modules, this corresponds to the increase of leakage current due to the increase of the coolant temperature, which leads to the increase of the module heat load. Figure 5.12 shows the thermal runaway turn-on temperatures for PS modules placed on the first endcap double disk, referred to as the TEDD1 structure, operated at 800 V bias voltage, and irradiated at the maximum considered fluence after 4000 fb⁻¹ of integrated luminosity. The study is using Finite Element Analyses (FEA) such that only features relevant for the studies of the thermal performance are included in the module model in addition to simplifications of the cooling structures. When referring to the thermal performance of the module, it must be mentioned that it is tightly complemented by the thermal performance of the support and cooling structures. The thermal runaway is estimated using front-end power consumptions extracted from prototypes and simulation, whereas the sensor power consumption is calculated from the projected worst case fluence for a particular module variant, here the 4.0 mm PS module in the TEDD region. The shaded region indicates the expected coolant temperature range across the multiple TEDD cooling sectors, with the lowest temperature of -35 °C expected on Ring 1 (R1). The figure shows that even for the worst case, namely R1, the thermal runaway is expected to occur with enough operation margin at temperatures at least 3 °C above the expected coolant temperature. For the remaining TEDD rings, the thermal runaway is not to be

expected within the entire coolant temperature range.

With such a complex design loaded with strict precision and performance requirements, the assembly of a PS module is certainly not a straightforward endeavour. The next chapter will focus on one of the module assembly approaches pursued by the collaboration for this matter. It is based on a custom semi-automated assembly procedure developed by DESY in order to guarantee a high precision assembly while reducing the amount of human manipulation.

CHAPTER 6

PIXEL-STRIP MODULE ASSEMBLY

The module assembly is a crucial step of the overall detector construction. In particular, to implement the p_T discrimination concept introduced in Chapter 5, the PS module sensor-to-sensor alignment must be achieved with high precision. The translational and rotational alignments of the strip sensor with respect to the pixel sensor are subject to strict requirements, described later, for which a custom assembly setup and procedure were developed by the DESY group. The module assembly is divided into two phases: the bare module assembly and the functional module assembly. In the first phase, the bare module only including a MaPSA and a PS-s sensor stacked on top of a CFRP base plate is produced. In the second, the four hybrid circuits (FEHs, ROH, POH) are attached to the bare module before proceeding with the wirebonding of MPAs and SSAs, and encapsulation of the wirebonds.

The bare module assembly relies on a semi-automated system that integrates high-precision motion stages, a microscope camera and vacuum handling tools. The system is controlled via a custom software featuring high resolution image acquisition, pattern recognition and manipulation of the individual components using the motion stages and vacuum tools. Besides the automated steps, the bare module assembly still requires intermediate manual interventions, justifying the reference to the system as semi-automated. This system has the objective of reinforcing reliability and high quality output thus minimising human intervention during the assembly. As a result, high precision and throughput can be achieved. In the fully functional module assembly, hybrid circuits are glued to the bare module using fixture, or what is commonly referred to as *jiggs*. Finally, the wirebond-

ing of the MaPSA and the PS-s to the front-end hybrids is performed using ultra-sonic wire bonding with Aluminium wires that are further protected with a dedicated encapsulant. This chapter provides a detailed description of each assembly phase with a focus on the semi-automated bare module assembly. Contributions of the authors mainly include involvements in using the system for the assembly of fully functional prototype modules.

6.1 Precision Requirements

As described in Section 4.1.1, the p_T discrimination relies on the correlation of particle hits in the top and bottom sensors within a programmable search window centered around a straight trajectory. However, due to the sensor separation and thus their position at different radii, a straight trajectory does not cross the same channel number in the two sensors. This is illustrated in Figure 6.1. Such an offset needs to be accounted for in the stub finding logic, through a programmable parameter, the so-called *window offset* in the case of the MPA. As the SSA and MPA chips implement binary readout, the precision with which the window offset can be tuned cannot be better than half the sensor pitch, thus bringing an intrinsic limitation to the p_T measurement.

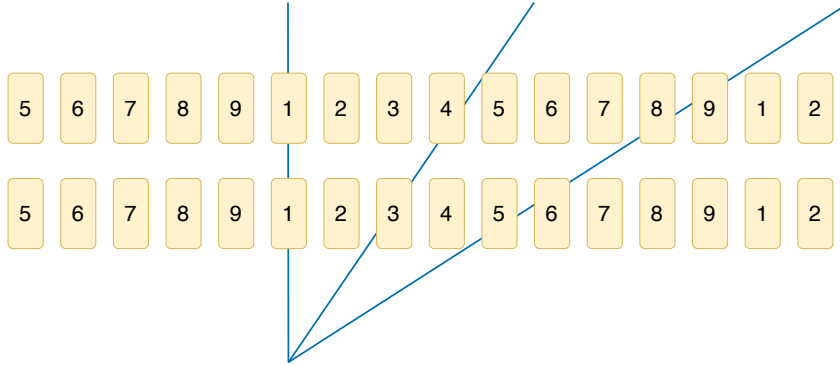


Figure 6.1: Illustration showing that straight trajectories do in general not cross the same channel number in the two sensors of a p_T module.

In the PS module, the PS-s is employed as the window layer. The offset is programmable up to eight strips, in steps of a half strip. The maximum expected offset depends on the Outer Tracker region. In the TBPS, the maximum offset is needed in the first layer and amounts to about 6 strips. For PS modules on the TEDD, the maximum is expected in the first disk and amounts to about 1.5 strips. In addition to mitigating differences resulting from the position inside the detector, the offset parameter is also able to absorb any lateral shift of the sensors with respect to each other with a half strip resolution.

However, a tilt (t) of one sensor with respect to each other introduces a variation of the offset along the strip which cannot be corrected in the stub finding logic. As a result, given the half pitch precision of the offset correction, the tilt between the sensors must be significantly smaller than half the pitch ($p/2$). With the pitch being $100\text{ }\mu\text{m}$ for each of the PS-p and PS-s sensors, a target of $t < 20\text{ }\mu\text{m}$ is set for the assembly precision, which translates into an angular tilt tolerance of $\theta < 800\text{ }\mu\text{rad}$. In addition, the tolerances for the lateral shifts along the x- and y-axes are defined as $\Delta x < 50\text{ }\mu\text{m}$ and $\Delta y < 100\text{ }\mu\text{m}$.

6.2 Bare Module Assembly

As mentioned earlier, the bare module assembly consists of gluing together the MaPSA and the PS-s sensor on top of a base plate covered with a Kapton isolator. It makes use of the semi-automated setup that handles all of the crucial sensor-to-sensor alignment steps. The procedure starts by gluing the MaPSA to the CFRP base plate. Afterwards, the PS-s is glued to the four spacers. Finally, the first half sub-assembly made of the PS-s and the spacers is glued on top of the other half made of the MaPSA and the base plate. A bare module is then obtained and metrology measurements are performed to ensure that the sensor-to-sensor alignments are well within the angular and lateral tolerances.

6.2.1 Setup

The bare module assembly setup consists of the main semi-automated system in addition to auxiliary tools used at various stages of the assembly procedure. These tools include two aluminium jiggs used for the preparation of the CFRP baseplate, and a set of stainless-steel blocks used to dispense glue onto the spacers. As far as jiggs are concerned, the first one is used to glue the aluminium inserts onto the CFRP base plate, while the second one is used to glue the isolation kapton foil on the surface of the base plate. The semi-automated system is a multi-function system providing three core features: motion, handling and vision. The system is mounted on a vibration-damping table with a stainless-steel surface featuring a grid of mounting holes. Figure 6.2 shows a 3D CAD view of the system.

The motion system performs translational and rotational movements of the assembly components and consists of motorized stages, namely a multi-axis translation stage and a rotation stage. The multi-axis translation stage allows movements along the x, y and z axes with a precision of $4\text{ }\mu\text{m}$ while the rotation stage allows rotations around the z axis and is capable of achieving a rotation precision of $175\text{ }\mu\text{rad}$ [59–62].

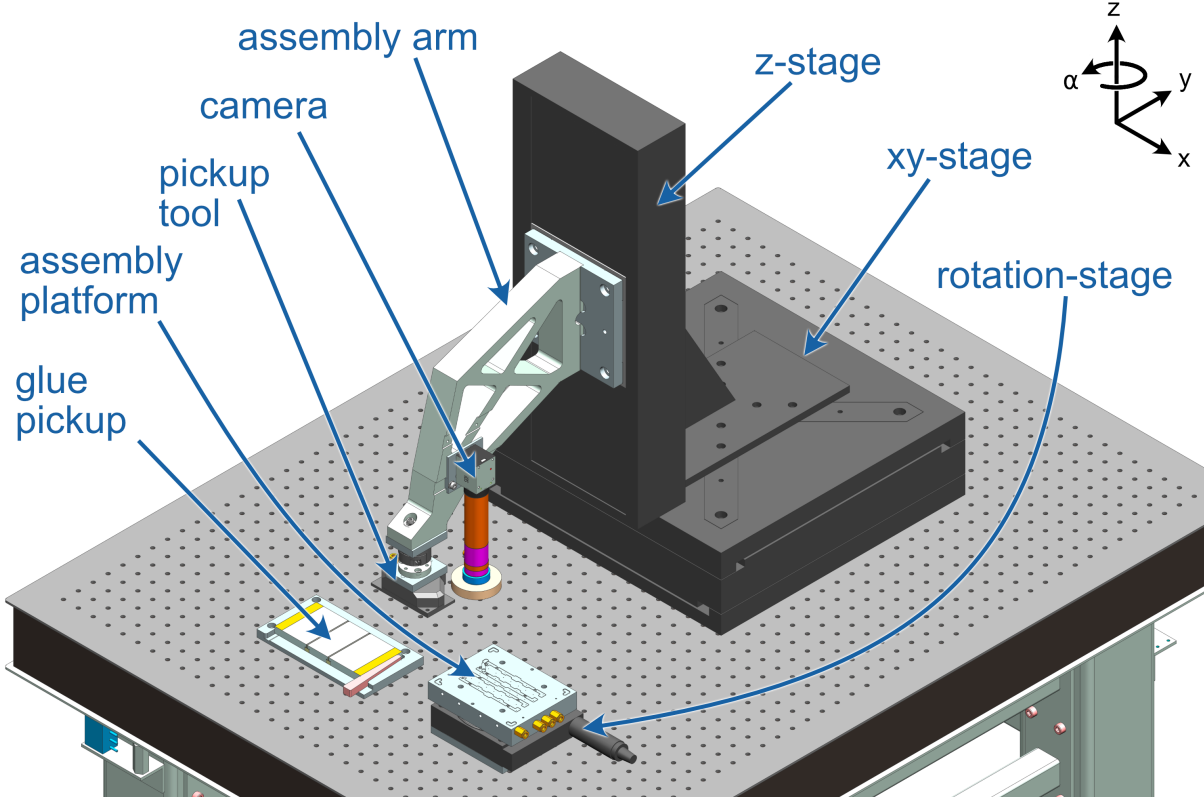


Figure 6.2: CAD model of the semi-automated assembly system. The motion function is fulfilled by the XYZ and rotation stages, the handling function by the assembly platform, arm and pickup tool, and the vision function by the camera. The glue pickup is used for glue dispensing as explained in the text. [48]

The handling system ensures accuracy and safety during the manipulation of the module components. It consists of two parts: an aluminium assembly platform designed to hold and fix the individual components during the assembly sequence and a pickup tool used to manipulate and position them. Both units rely on vacuum suction as a means to hold the components in place. Each individual vacuum line is controlled by electromagnetic valves connected to a USB relay card itself controlled from a computer. The assembly platform is directly mounted on top of the rotation stage and is designed to hold the various module components. Figure 6.3 shows an image of the assembly platform. In addition to the vacuum lines, it features on its surface pin holes used for the CFRP base plate fixation, grooves and stops for spacer positioning, a groove to host the PS-s High Voltage (HV) tail, and some reference markers. The rotational movement of this platform is crucial to achieve the target angular alignment of sensors with respect to each other. Finally, the pickup tool is made of an ESD plastic block [63] and features an array of vacuum holes on the bottom surface providing vacuum suction capabilities. It is attached

to the assembly arm using a ball-joint that can be adjusted such that the bottom side of the pickup tool doesn't yield any vertical tilt with respect to the assembly platform.

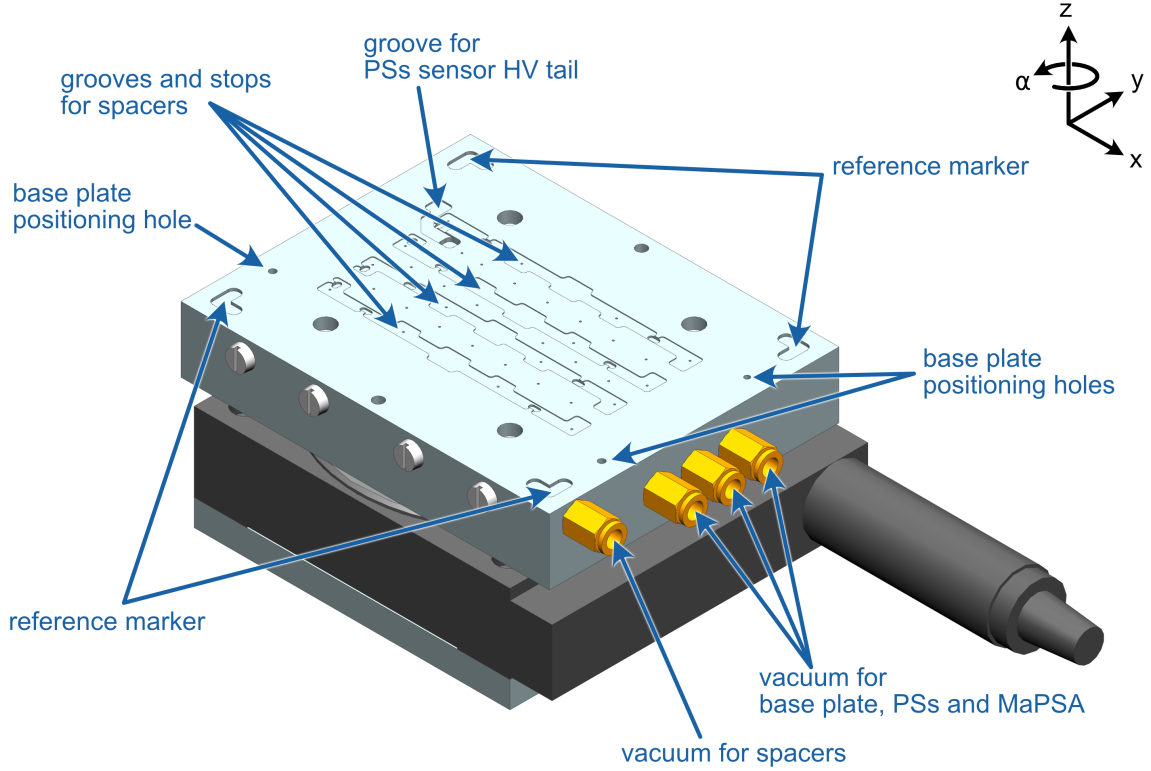


Figure 6.3: CAD model of the assembly platform. The rotation platform is indicated in black. The vacuum channels are shown in gold. The platform itself is shown in blue with the indicated features for the module components. [48]

The vision system provides high resolution image acquisition using a camera equipped with a low-power ring light and complemented by a microscope lense. This ensures proper light conditions and high quality images. The images are processed using a pattern recognition algorithm and real-time orientation of the sensors can be inferred. The latter are crucial to correct the position of the assembly platform and ensure proper alignment of the components.

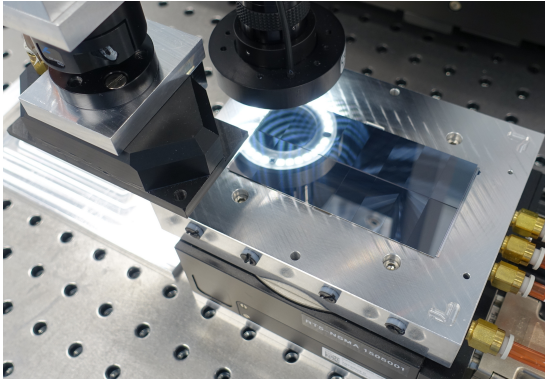
The entire semi-automated system is controlled using a custom software application written in C++, offering a Graphical User Interface based on the Qt framework [64] and image processing modules exploiting the openCV library [65]. The GUI provides control over the motion stage movements, the vacuum lines and the pickup arm. In addition, the software application features multiple functionalities that cover image acquisition

with color-to-gray and gray-to-black-and-white conversions, pattern recognition using the openCV functions, and custom alignment algorithms that are used during the setup calibration and the assembly sequence.

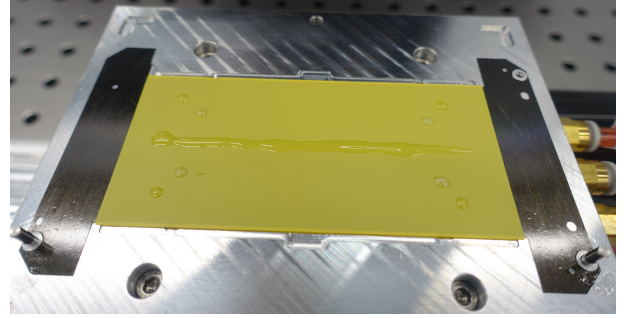
As far as the use of the semi-automated system is concerned, various calibrations must be performed before proceeding with the bare module assembly. These calibrations are crucial to achieve the target precision and must be performed every time a modification is made to the setup. First, the ball joint mechanism must be adjusted to mitigate any eventual vertical tilt that could affect the manipulation of the individual components. Second, the camera angle must be measured to ensure a reliable correspondance between the acquired images and the resulting stage movements. Third, the assembly platform orientation must be corrected to guarantee a well centered position of the individual components. Finally, the focus and pickup heights must be measured to ensure an optimal contact with the individual components placed on the assembly platform.

6.2.2 Procedure

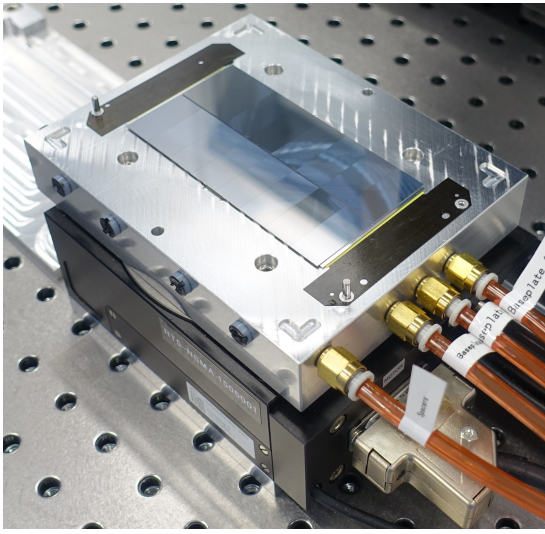
As mentioned earlier, the assembly procedure consists of three steps: gluing the MaPSA to the CFRP baseplate, gluing the Al-N spacers to the PS-s sensor, and finally attaching the PS-s and spacer sub-assembly to the MaPSA and base plate subassembly. Each step uses a combination of fast and slow curing epoxy glues. The main epoxy glue used is the Polytec EP 601-LV [66], a low viscosity two-component epoxy adhesive with a minimum curing time of 16 hours at 23°C, referred to as *slow glue*. Its main advantage is to allow for a low bond line thickness which facilitates heat dissipation in the through-plane direction. However, with regards to its long curing time, and to ensure the target assembly throughput, the use of slow glue is complemented by the use of Loctite EA 3430 [67]. The latter is a fast-curing medium-viscosity two-component epoxy with a curing time of the order of seven minutes and referred to as *fast glue*. It should be noted that 99% of the surface area when gluing the PS-s and spacers to the MaPSA and base plate is covered in slow glue and thus the overall properties of the assembled bare module glue layers correspond to those of the slow glue. As far as manipulation is concerned, individual components such as sensors, spacers and base plate are manipulated on the assembly platform using vacuum pens, tweezers and hands while each step of the assembly is performed using the semi-automated system via the control GUI. Figure 6.4 shows pictures of the different steps of the bare module assembly sequence.



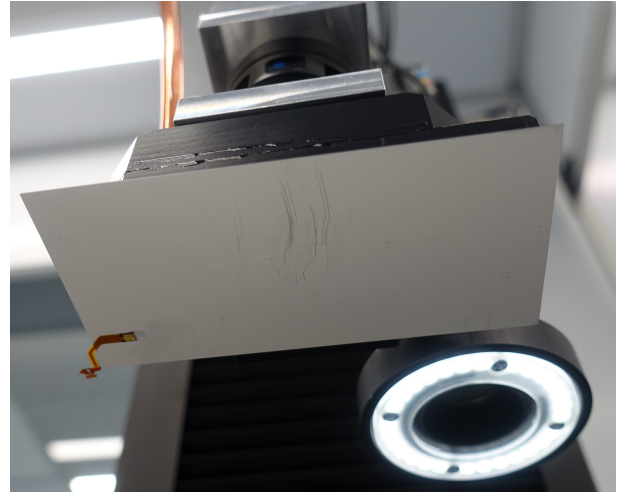
(a)



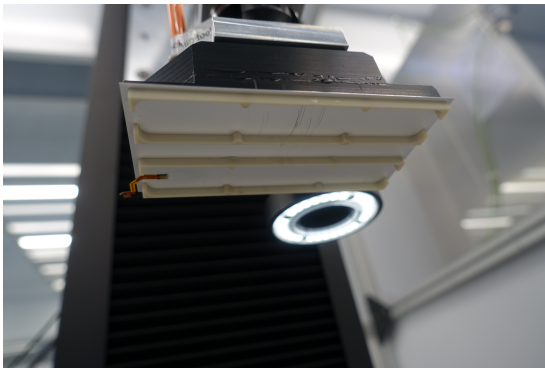
(b)



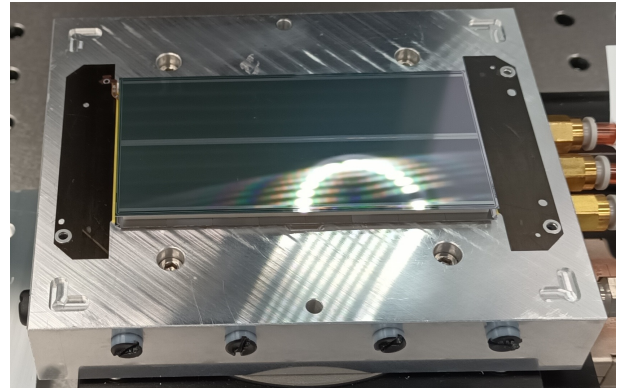
(c)



(d)



(e)



(f)

Figure 6.4: Pictures from different steps of the bare module assembly sequence. Picture (a) shows the pickup of the MaPSA sub-assembly, picture (b) the CFRP baseplate with dispensed glue, and picture (c) the gluing of the MaPSA to the baseplate. Picture (d) shows the pickup of the PS-s sensor, picture (e) the PS-s with attached spacers, and picture (f) the final bare module obtained from gluing the two aforementioned sub-assemblies.

MaPSA to baseplate gluing

First the MaPSA is placed on the assembly platform and fixed by vacuum as shown in Figure 6.4(a). An alignment routine is then performed. In the latter, the pattern recognition algorithm is iteratively used on the two opposite sensor fiducial markers along the long edge of the sensor such that the rotation of the assembly platform is corrected until the measured rotation between the fiducial markers becomes smaller than the tolerance of the rotation stage. Once that is achieved, the pickup tool is lowered onto the MaPSA and the sub-assembly is picked up by successively switching on and off the pickup tool and assembly platform vacuums, respectively. Next, as shown in Figure 6.4(b), slow glue is dispensed on the baseplate surface using a 3-axis automatic dispensing robot and a small amount of fast glue pattern is dispensed manually. The baseplate is then placed and fixed onto the assembly platform using vacuum and alignment pins. The latter are removed once the vacuum is engaged. Finally, as shown in Figure 6.4(c), the MaPSA is lowered onto the base plate and the position is held for 20 min until curing of the fast glue. The PS-p and base plate sub-assembly is then put aside.

Spacers to PS-s gluing

In this step the PS-s sensor is first placed on the assembly platform and fixed by vacuum as shown in Figure 6.4(d). The same alignment and pickup routines used for the MaPSA are used, and the PS-s sensor is picked up. Fast and slow glue are dispensed on the glue stainless steel blocks where the four spacers are dipped on one side before being placed on the assembly platform with the glue facing up. Vacuum is then engaged below the spacers to hold them in place, the PS-s sensor is lowered until contact is made and the position is held for 20 min until curing of the fast glue. The spacers vacuum is then disabled and the sub-assembly is picked up as shown in Figure 6.4(e).

PS-s-spacers to MaPSA-baseplate gluing

The MaPSA and base plate sub-assembly is brought back onto the assembly platform, fixed using vacuum and alignment pins, and the alignment routine is performed. Layers of slow and fast glue are dispensed on the glue stainless steel blocks and the latter are positioned on a dedicated glue pickup platform integrated to the assembly table. The PS-s and spacers sub-assembly is moved above the pickup blocks, and lowered such that the bottom side of the spacers is dipped into glue for approximately one second. Afterwards the PS-s and spacers sub-assembly is lifted, brought back on top of the MaPSA and baseplate sub-assembly then lowered onto the assembly platform until contact is made

between the two sub-assemblies. The position is then again held for 20 min until curing of the fast glue. This step completes the assembly sequence, and a bare module as shown in Figure 6.4(f) is produced. The bare module is transferred onto a dedicated curing plate and stored in a dry air cabinet until the slow glue is fully cured.

6.2.3 Metrology

Following the assembly and curing of the epoxy glue, every assembled bare module is subject to a metrology evaluation in order to verify that the lateral and angular alignment of the sensors are within the specified tolerances. Figure 6.5 shows metrology results from the last five bare modules assembled at DESY.

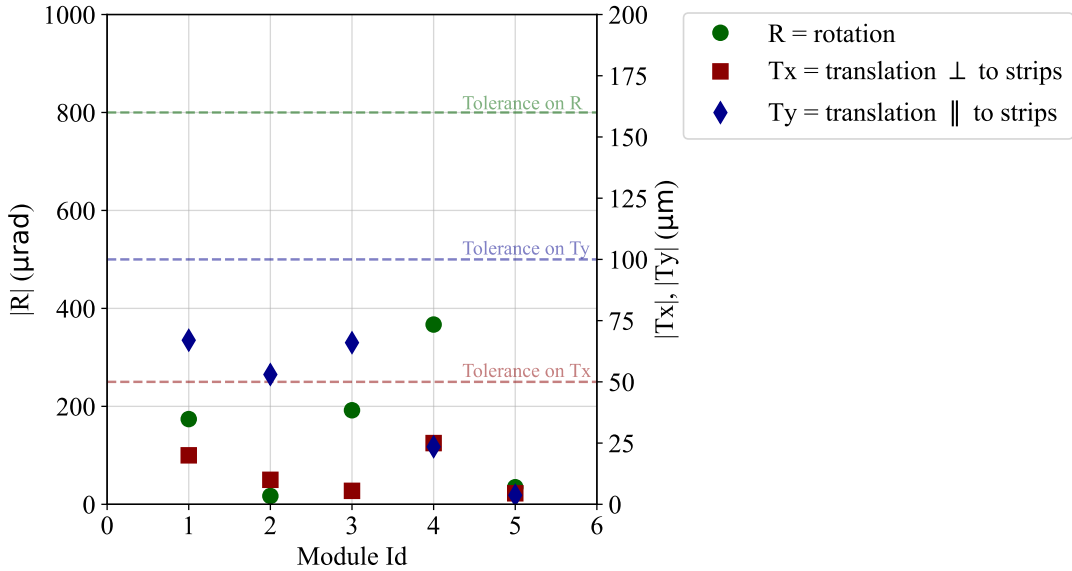


Figure 6.5: Metrology results from the bare modules assembled at DESY.

As mentioned before, these tolerances must be respected as they are crucial to ensure the best performance of the signal correlation and p_T discrimination logic for which the module is purposed. The metrology procedure relies on the use of the sensor fiducial markers and a metrology system, referred to as the *smart scope*, providing advanced vision and measurement features [68]. It is a high capacity benchtop multisensor measurement system capable of running camera-based automated routines and perform high precision measurements. Based on the four fiducial markers on each sensor, the metrology system builds virtual planes corresponding to each sensor using their respective fiducial markers. This is only possible thanks to the fact that the PS-p sensor is slightly larger than the PS-s sensor, thus allowing the fiducial markers from each sensor to be exposed. From the virtual planes, translational and rotational displacement can be inferred, and the success

of the bare module assembly can be assessed. So far at DESY, as Figure 6.5 shows, all the assembled bare modules were well within the specified tolerances.

6.3 Hybrid Circuits Gluing

Next in the assembly chain is the hybrid circuits gluing. It consists of attaching each of the Power Hybrid (POH), the Front-End Hybrids (FEH) and the Readout Hybrid (ROH) to the assembled bare module. It makes use of a custom gluing jig where the bare module is positioned and fixed with alignment pins. In addition, gluing blocks on which a well defined layer of slow glue is dispensed are used such that the bottom side of the hybrid is dipped into the glue before being placed on the jig.

The first hybrid to be attached is the POH. The bottom of the hybrid circuit is dipped into the gluing block and glued to the base plate on its dedicated position using an alignment pin. Next, the FEH are attached. The latter are equipped with Al-N feet on each end of the circuit that are used as gluing contacts. Both feet are dipped into the layer of glue and the hybrids are placed, using alignment pins, on their dedicated position such that the feet are glued to the corners of the base plate. Finally, the ROH, equipped with a spacer on the bottom part, is dipped into a layer of glue and placed on its dedicated position such that the spacer is glued to the base plate. Finally, to avoid any perturbation of the curing process, finger pushers integrated to the gluing jig are engaged on top of each hybrid to ensure a stable fixation until the glue is fully cured. Once the glue is cured, each hybrid connector is attached to its mated hybrid, and the fully assembled module is ready to proceed further in the assembly chain.

6.4 Wirebonding & Encapsulation

The last step of the module assembly procedure is wirebonding of the MaPSA and the PS-s sensor to the two FEHs, as well as their corresponding encapsulation. Wirebonding is performed using a dedicated system that uses an ultra-sonic aluminium wedge bonding technique. The connection consists of aluminium wires connecting on one side the PS-s sensor to the SSA bond pads on the top side of the FEH, and on the other side the MPAs to their corresponding bond pads on the bottom side of the FEH. Finally, the PS-p and PS-s sensor guard rings, as well as the PS-p sensor backplane are wirebonded to the ground pad and the HV circuit pad on the FEH, respectively. Wirebonds are further protected using a layer of SYLGARD 186 Silicone Elastomer [69] encapsulant dispensed

using the same automatic dispenser used for glue dispensing. The encapsulation step results in a fully assembled PS module, or what is referred to as the *functional* module. Figure 6.6 shows a picture of a functional module with a VTRx+ module attached and mounted on a dedicated module carrier plate.

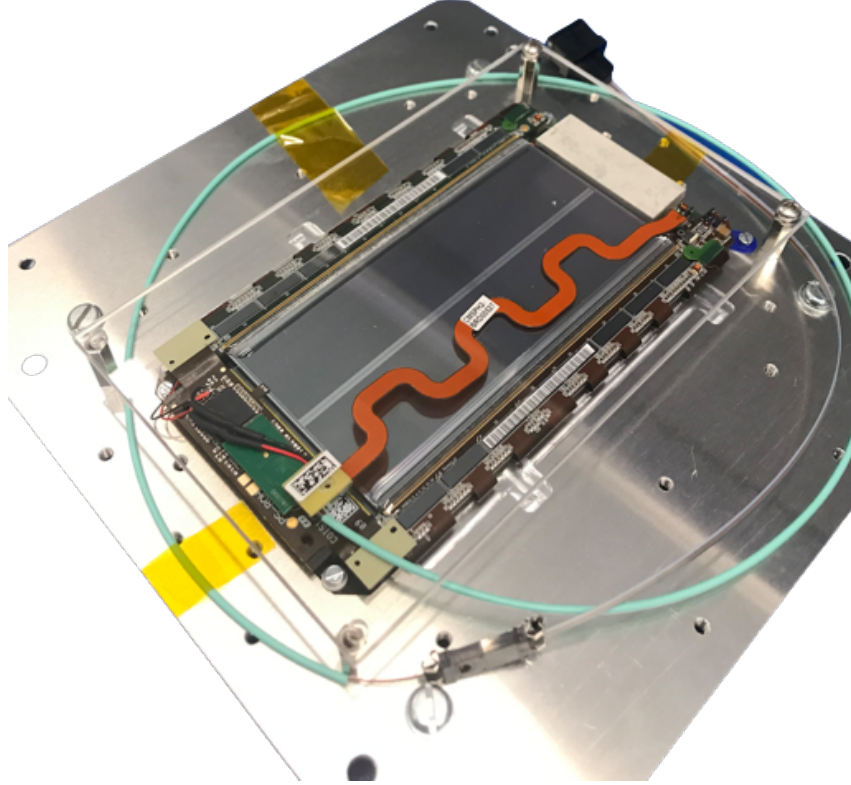


Figure 6.6: Picture of an assembled functional module, with the VTRx+ optical module attached and placed on a dedicated module carrier plate. Since the ROH used for this module didn't host a connector for the power tail, the latter is directly soldered to the hybrid circuit via two short wires.

It must be mentioned that prior to the distribution of the individual components to the module assembly centers, each of them is subject to a series of qualification tests. This ensures that only high quality mechanical components, functional sensors and hybrid circuits are used for the assembly. Finally, the assembled modules are also extensively tested to assess the performance and functionality of the sensors and the readout chain. The next chapters will focus on discussing a subset of the systems and the preliminary qualification tests developed for this purpose.

CHAPTER 7

MODULES PRODUCTION TEST SYSTEMS

Characterization and qualification of individual module components and fully assembled modules is a major part of the Outer Tracker project. Not only does it steer the R&D phase of the project but it is of central importance for the success of the production and detector integration phases. The Outer Tracker is supposed to operate for ten to fifteen years without any foreseen replacement. Therefore, every single component and assembled module needs to undergo a thorough qualification to ensure the expected longevity and performance. Figure 7.1 shows a diagram describing the quality control (QC) flow of individual components and assembled modules. For individual components, such as the silicon sensors or the front-end ASICs, the QC is already performed following the production at the vendors. Components are then delivered to distribution centers where they undergo additional QC. The components meeting the quality requirements are further distributed to the modules assembly centers where modules are produced and qualified. Finally, the modules passing the qualification tests are distributed to the integration centers where they are integrated into the large Outer Tracker structures.

Thousands of front-end chips, hybrid circuits, and assembled modules are foreseen to be produced. This creates the requirement of dedicated test systems to support both the prototyping and the production phases. These systems need to cover a large number of different devices and support both 2S and PS modules. For the hybrid circuits qualification, a crate-based test system featuring a multiplexed backplane interface and a set of test

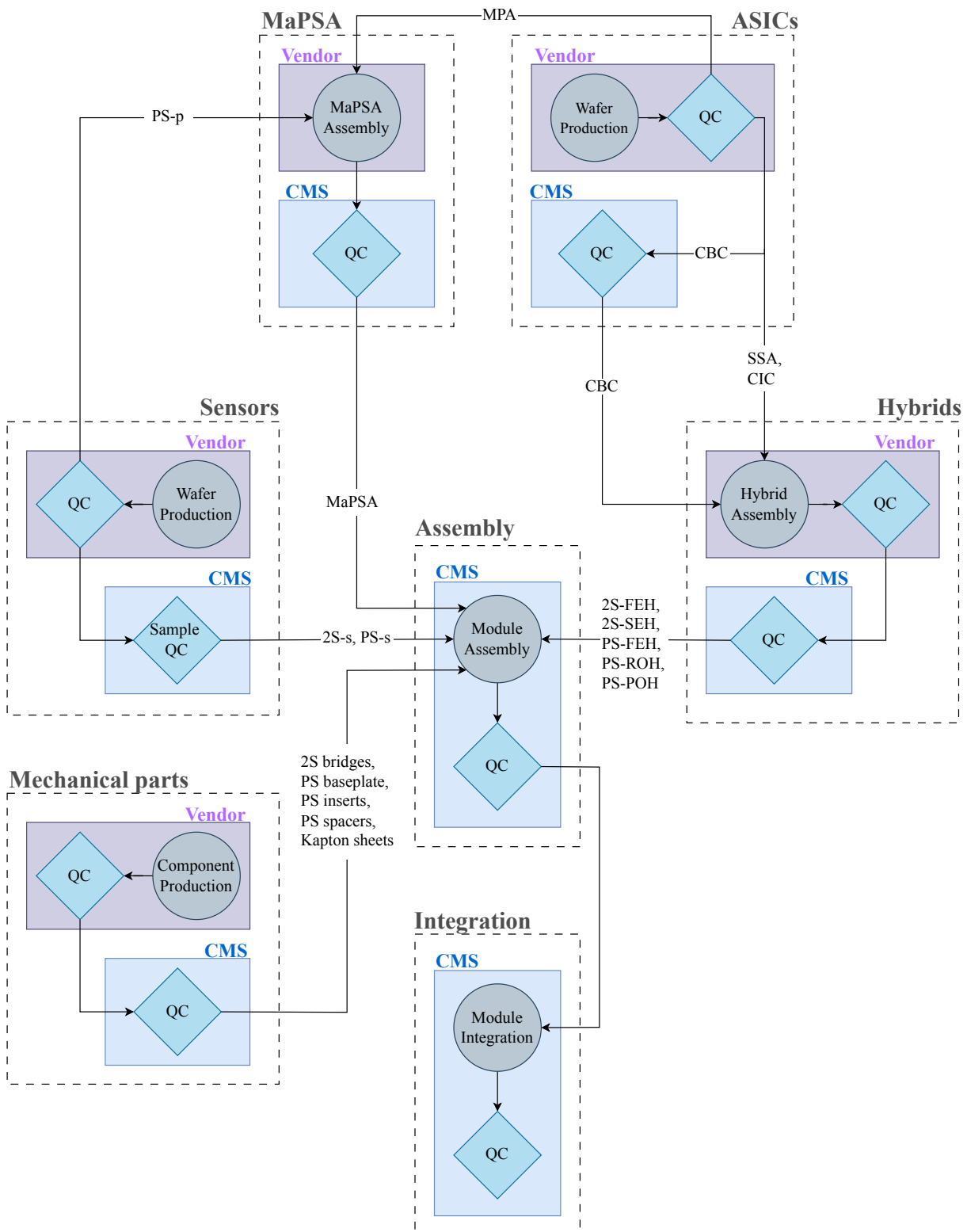


Figure 7.1: Diagram showing the quality control flow of individual components and assembled modules, starting from the component assembly at the vendors, down to the modules assembly centers and finally the detector integration centers.

cards hosting individual hybrid circuits was developed. The system is used for electrical testing of individual hybrid circuits and allows for a high throughput testing during production. For individual module testing, a custom and multi-feature module test station was developed. It provides a hermetic environment and a set of interface connectors to supply all kinds of services needed by the module. For the control and data readout, the DTC system was introduced in Chapter 4 as the one foreseen for the control and readout of the Outer Tracker. However, since the DTC system is still under development, the so-called micro-DAQ, Trigger and Control (μ DTC) system was chosen as an alternative to fulfill the needs of the prototyping and production phases. The μ DTC system is based on the FC7 board [70], a Field Programmable Gate Array (FPGA)-based circuit board complemented by a flexible FPGA program (firmware) to fulfill the needs of components and modules testing. Finally, the μ DTC system is complemented by control and test procedures developed within the so-called Phase-2 Acquisition and Control (Ph2ACF) software framework. The latter is a generic C++ software framework dedicated to the control and readout of the final CMS Tracker detector but is also used as the main development environment for prototyping and production test procedures. This chapter gives a detailed description of the various test systems, uncovering the corresponding hardware, firmware and software architectures and designs. Contributions from the author include major extensions to the μ DTC firmware and the Ph2ACF software framework, as one of the main developers, in order to support the hybrid test system control and the optical control and readout of assembled modules equipped with the lpGBT chip.

7.1 Hybrids Test System

The hybrid test system was designed to fulfill the large-scale and high throughput production of the 2S and PS hybrid circuits. It is a crate-based system with the main purpose of providing an interface between a control and readout system, in this case the FC7 board that will be described later, and the hybrid circuits. The objective is to perform quick electrical and functional tests of the hybrid circuits, be it at room temperature or during thermal cycling. The test system consists of a standard 3U size 19-inch sub-rack in compliance with the IEC 60297-3-101 standard, hosting three active multiplexing backplane modules. Each of the backplane modules can support up to four test cards on which hybrid circuits can be mounted. The control and readout interface between the FC7 board and the test system is ensured by two 3 meter Low-Pin Count (LPC) HDR cables. These cables allow the control of the multiplexing backplane and the selection of a test card, and provide an interface for the LVDS data signals from the hybrid circuit to the control and

readout system. Figure 7.2 shows a 3D model of the test-system crate populated with a simplified model of hybrid test cards.

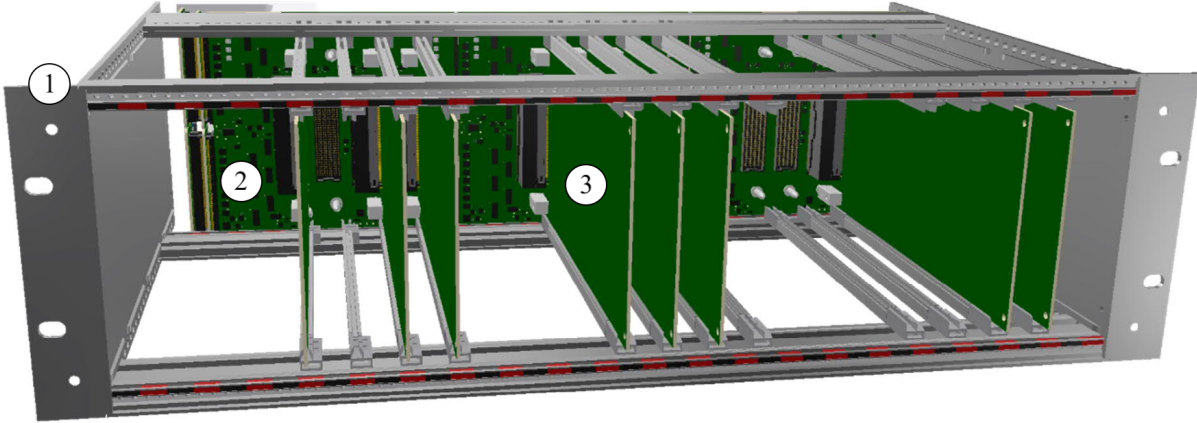


Figure 7.2: 3D model of the hybrid production test system indicating the crate structure (1), the multiplexing backplane (2) and the blank hybrid test cards (3) connected to their corresponding backplane module.

7.1.1 Multiplexing Backplane

The backplane modules are designed in conformity with the requirements of versatility, modularity and high-throughput production testing. Each backplane module can host four different hybrid circuit test cards. With such a design, up to twelve test cards can be inserted and the same number of hybrid circuits can be tested at once. However, the control and readout of all test cards in parallel is very resource intensive. Therefore, the backplane module was designed to multiplex the test cards and allow selection, control and readout of a single test card, and thus hybrid circuit, at a time. This selection process is achieved using 12-channel analogue multiplexers. To ensure proper transmission of the data signals through the backplane, LVDS buffers that act as an interface for the high speed LVDS data signals routed between the hybrid circuit and the FC7 board are included. Finally, the control of the multiplexing circuit is achieved via a low-pin count HDR cable that connects the first backplane module to the FC7 while providing access to the other backplane modules. Figure 7.3 shows a simplified model of the backplane modules and HDR cables, as well as the test card multiplexing circuit.

In the multiplexing circuit, a level-1 signal is used to select the backplane while level-2 and level-3 signals are used to select the test card slot. The selection results in the distribution of power to the selected test card. This way only a single card is powered

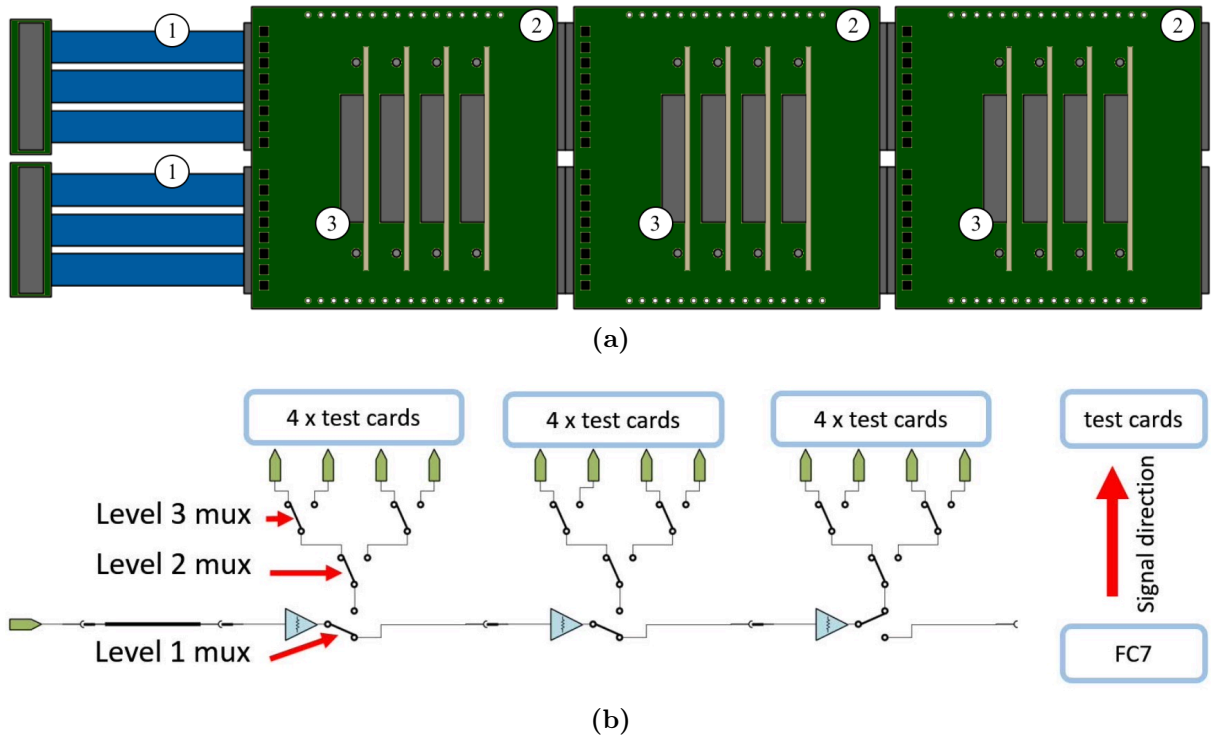


Figure 7.3: Simplified model of the multiplexing backplane (a) and a schematic of the multiplexing circuit (b). The backplane model indicates the HDR connection cables (1), the individual backplane modules (2), and the connection slots dedicated to the hybrid circuit test cards (3).

and all its corresponding data signals are multiplexed to the FC7 through the backplane interface. The multiplexing signals can also be used to detect the available backplanes and test cards which are assigned a unique identifier.

7.1.2 Hybrids Test Cards

The hybrid test cards are designed to host individual hybrid circuits and provide all the necessary control and test features required for a functional qualification. The test cards mechanical design is unified such that they all share the same geometry for the card outline and the backplane connector placement. This way, compatibility with the previously described crate and backplanes is ensured. The core difference resides in the electronic design which is adapted to the hybrid circuit for which the test card is developed. Each Outer Tracker hybrid circuit requires a dedicated test card design but this section will only focus on the electronic design of test cards for the PS hybrid circuits, highlighting the main design components and all the set of interfaces and test features the card provides. In the case of the PS module, three main test cards were designed: the PS-FEH test card,

the PS-ROH test card and the PS-POH test card. Finally, an additional PS-FEH test card specifically dedicated to the PS-FEH High Voltage (HV) circuit testing was designed but will not be covered in this section.

Pixel-Strip Front-End Hybrid Test Card

The PS FEH Test Card is used for the functional qualification of individual PS FEH circuits. Figure 7.4 shows a top view of the test card, with the hybrid circuit hidden underneath a socket shown as (2) that provides connection pressure against the test card.

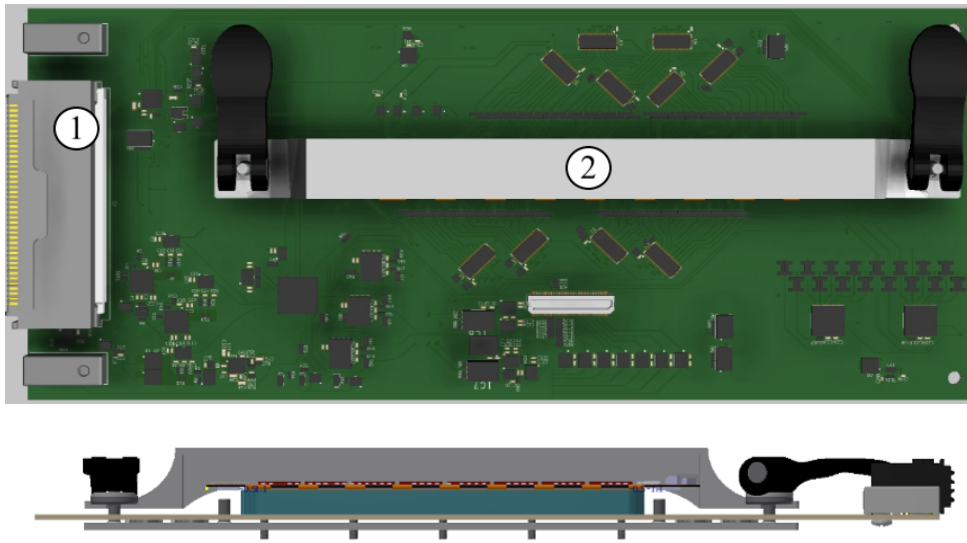


Figure 7.4: Top view of the PS FEH hybrid test card (top) and a side view of the socket fixture between the hybrid and the test card. In the top view, (1) indicates the backplane connector while (2) corresponds to the socket underneath which the hybrid is hidden.

The socket provides probe pins pressed against CIC and SSA input and output signal probe pads that act as a signal interface for transmission or readout of CIC and SSA data. This feature is of particular importance as the SSA output and CIC input signals are in principle routed to the MPAs which are not available at the FEH testing level. In addition, access to the CIC output signals as well as to the reset, clock and fast command signals is provided through a flexible cable attached on both end-connectors of the hybrid (not shown in the figure). The flexible cable is complemented by LVDS to SLVS translation circuits used to feed the signals to the FC7 board. As far as power is concerned, Low-Dropout (LDO) regulators are included to supply the necessary voltages to the circuit, and Analogue-Digital Converters (ADCs) provide measurement access to most of the test card power supply lines. Control and monitoring features on the test

card are implemented using a Serial Peripheral Interface (SPI) accessible via a Universal Serial Bus (USB) interface multiplexed between all the test card slots. Finally, to test the connection between the SSA inputs and the sensor wirebond pads, an antenna circuit is integrated to the test card and can be controlled to inject a small charge through the capacitively coupled antenna circuit underneath the wirebond pads on the hybrid. This is of particular importance in order to identify broken or shorted signal traces in the circuit.

Pixel-Strip Readout Hybrid Test Card

The PS ROH test card, as shown in Figure 7.5, is dedicated to the qualification of ROH circuits. The figure shows a top view of the test card, equipped with the corresponding hybrid. An additional power cable is included in order to study effect of the power tail shown in Figure 5.1, on the ROH functionalities.

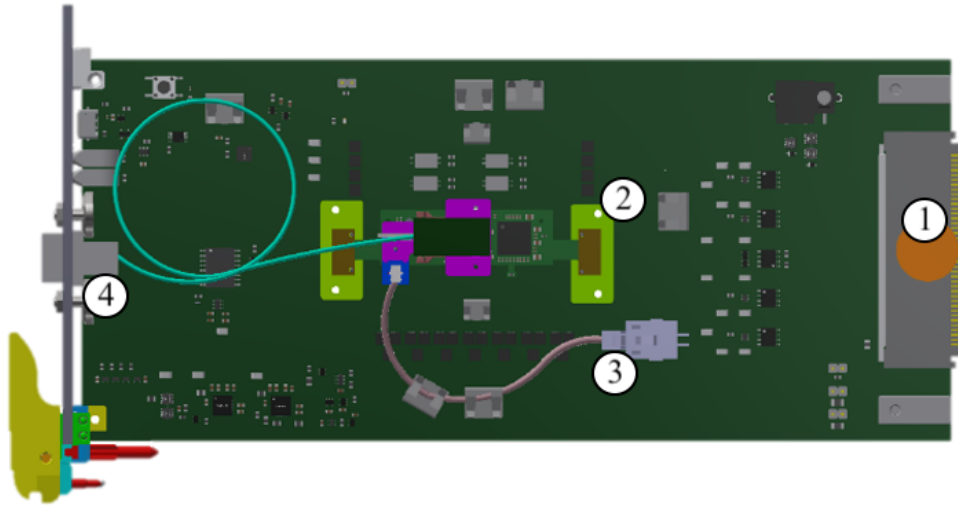


Figure 7.5: Top view of the PS readout hybrid test card. (1) indicates the backplane connector, (2) the connected ROH, (3) the power cable dedicated to the PS module power tail studies, and (4) the MPO interface for the optical fiber.

The hybrid is connected to the test card via two connectors on the hybrid circuit tails. These connectors act as an interface to all the power, control, and data lines. They provide access to the set of power distribution lines, I²C control interface with the lpGBT, the CIC output data lines as well as the reset, clock and fast command signal lines. A set of signal translation circuits ensure proper conversion from LVDS to SLVS, and vice versa. LDO regulators are used to supply the necessary voltages to the circuit, and measurement of most of the power supply lines is provided via dedicated ADCs. Control and monitoring of the test card features is provided through an USB-to-SPI communication

interface. The test card also integrates a fusing circuit to perform the fusing of lpGBT configuration registers. The fusing process consists of burning configuration fuses on the ASIC to permanently fix the register configuration value. It is of particular interest if some critical registers, not expected to be modified during operation, need to be configured and protected from potential modification due to radiation effects. Finally, since the ROH, with the presence of the lpGBT, is intended to ensure optical data transmission and control of the module, an Multi-fiber Push On (MPO) connector is mounted on the test card front-panel to allow for an additional optical connection with the back-end system. The latter is needed to fully test both electrical and optical functionalities of the ROH.

Pixel-Strip Power Hybrid Test Card

The functional qualification of the POH circuit is performed using the POH test card shown in Figure 7.6. The top view figure shows the test card, equipped with the corresponding hybrid hosted underneath a metal fixture and placed on top of a heat sink. The metal fixture ensures that enough pressure is applied for the hybrid to stay fixed on the test card. The heat sink is used as a heat dissipator. Flexible cables are used to connect the hybrid tail connectors to the test card and act as an interface to the hybrid power output lines which can be measured using dedicated ADCs. Finally, a micro-controller is integrated and provides all the control, test and monitoring features of the test card.

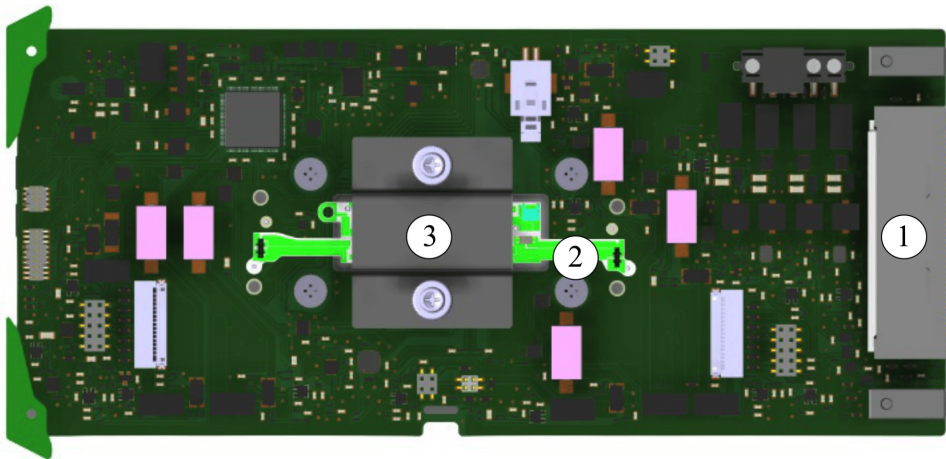


Figure 7.6: Top view of the PS power hybrid test card. (1) indicated the backplane connector, (2) the connected POH, and (3) the metal fixture to stably hold the hybrid on the test card.

7.2 Single Module Test System

The single module test system [71] was developed at Karlsruhe Institute of Technology (KIT) and is designed to host fully assembled 2S or PS modules allowing the full characterization of the sensors and readout chain. It was developed for the purpose of unifying the module test environment across all the module assembly centers. It provides an environment which minimizes the risk of damaging a module and allows for a full automation of the test procedure.

Figure 7.7 shows a picture of the test system with its corresponding integrated devices. It consists of an aluminium box which acts as Faraday cage and guarantees a dark environment by shielding the module from electromagnetic disturbance and light. Inside the box, the module carrier plate is hosted on four corner plates made of electrically conductive polyethylene and connected to the box frame. This, at the condition of which the box is placed on an electrostatic discharge safe table or mat, avoids charge accumulation at the corner plates and preserves the module from electrostatic discharges.

The module is held in place by lateral spring pushers that press the module carrier plate against pins on the backside. To ensure that the module is operated in a dry environment required for the best sensor performance, a 6 mm opening diameter tube pass-through is provided on the back of the box and can be connected to a dry air supply. The latter is also used for cooling since passive cooling using dry air was chosen for the operation of the module inside the box. Therefore, dry air outlets are provided and directed towards the components where most of the heat is generated, in particular the shielded DC-DC converters. To monitor the environmental conditions, a temperature and humidity sensor is integrated to the box. A connector back-panel provides a set of USB-A and power input connectors that are used for the Arduino [72] device and the supply of both low voltage and high voltage. The back-panel is complemented by a light-tight feed-through for the optical fiber. To guarantee operational safety, a magnetic reed relay is integrated to the box corpus and lid to interrupt the high voltage line until the box is fully closed.

Finally, the test box integrates the so-called Karlsruhe Infrared Array (KIRA) system. The latter consists of an array of LEDs that allows for charge injection in both the top and bottoms sensors, and thus a full qualification of the module's readout chain. However, due to the shielding presence of the carbon fiber base plate in the case of the PS module, the system will only be used for the qualification of 2S modules.

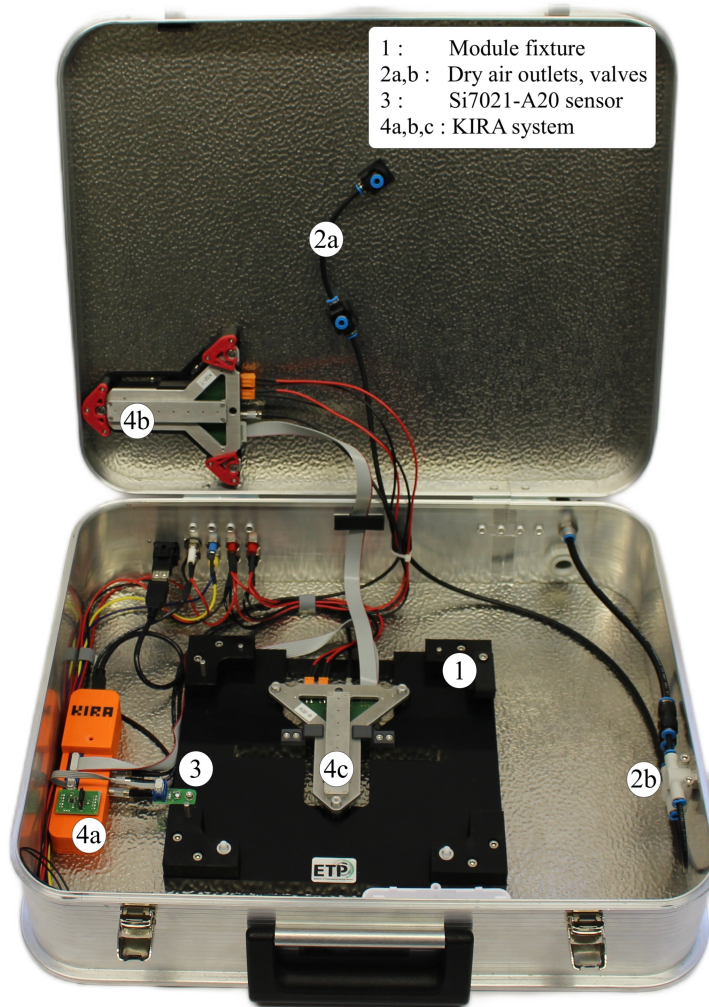


Figure 7.7: Picture of a module test station, indicating the fixture (1) hosting the module carrier plate, the dry air supply valves and outlets (2), the KIRA trigger generator (4a) and the KIRA boards (4b, 4c). Modified from [71].

7.3 Data Acquisition & Control Systems

Data acquisition and control is central in the module qualification. It is divided into three core parts: the hardware system, the firmware program and the software framework. The hardware system is based on the FC7 board hosting an FPGA and various peripherals such as external memories and FPGA Mezzanine interfaces. The firmware with which the FC7 FPGA is programmed is the so-called μ DTC firmware. It is a highly flexible and versatile firmware purposed for readout and control of the front-end ASICs, either electrically in the case of individual hybrid circuits, or optically in a fully assembled module. In addition, the firmware supports the control of the tests systems, in particular the multiplexing feature of the hybrid test system. Finally, the control and data readout is integrated to the tracker software framework, the Phase-2 Acquisition and Control Framework (Ph2ACF), in principle dedicated to final tracker control and readout, but also used for hybrid circuits and assembled modules qualification during both the prototyping and production phases. Each of these parts will be described in details in this section.

7.3.1 FC7 Board

The FC7 board is a flexible Advanced Mezzanine Card (AMC) [73] compatible with the micro-Telecommunications Computing Architecture (μ TCA) [74] form factor and used for generic data acquisition and control applications built around the Xilinx Kintex-7 FPGA [75] and the FPGA Mezzanine Card (FMC) Standard [76]. It supports a large array of configurable I/O as well as Multi-Gigabit Transceivers (MGT) operating at up to 10 Gbps.

Figure 7.8 shows the top side of an FC7 board. The FPGA is the key component of the FC7. It is a type of integrated circuit that provides a set of I/O Banks and Configurable Logic Blocks (CLB) that implement the user logic. CLBs are all connected through a highly-flexible configurable interconnect system of wires and Switch Matrices that allow dynamic reprogramming of the deployed logic. The simplest structure of a Configurable Logic Block includes an arrangement of three basic blocks: Look-Up Tables (LUTs), Flip-Flops (FFs) and Multiplexers. Look-Up Tables are configurable truth tables that implement the combinational logical functions, Multiplexers are used for selection logic, and Flip-Flops store the outputs of LUTs and are used for synchronous operation. Figure 7.9 shows a block diagram of a simplified FPGA architecture and CLB structure. Most of the FPGAs used for complex applications requiring advanced signal processing use more complex CLB structures with additional blocks for an improved performance.

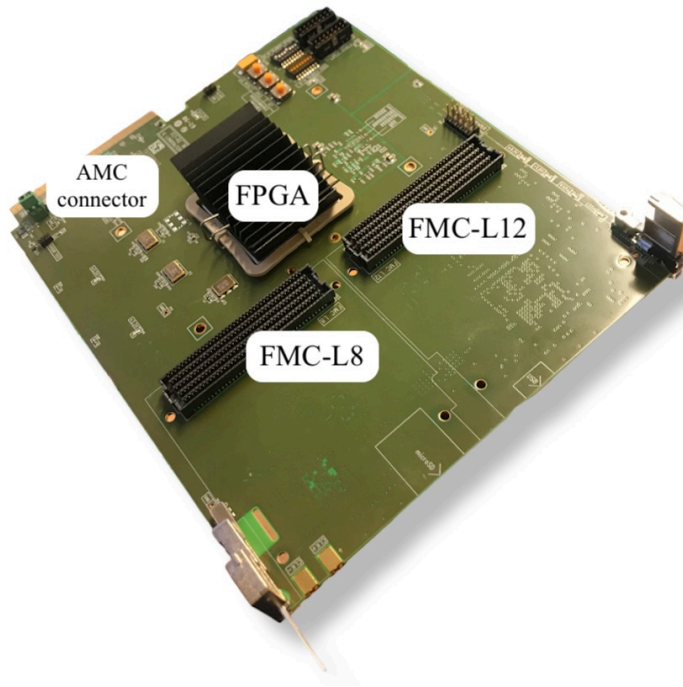


Figure 7.8: Picture of an FC7 AMC, indicating the backplane AMC connector, the FPGA and the two FPGA mezzanine card connectors used as external interfaces.

In the case of the Kintex-7 FPGA which was released in 2010 and which is used on the FC7, 65.150 CLBs are available with each containing four Look-Up Tables and eight Flip-Flops. In addition, it also provides 30.060 kB of Random Access Memory (RAM) blocks distributed across the chip and used for intermediate data storage. All these resources allow the user to implement a custom processing logic by developing a so-called FPGA firmware. Even though the market offers more powerful FPGA, such as those from the Xilinx Virtex Ultrascale+ series, the Outer Tracker DAQ system for the prototyping and productions phases doesn't require such processing power and thus relies on the already available FC7 board and the Kintex-7 FPGA.

In addition to the FPGA, the FC7 provides a set of complementary components and features. A card edge AMC connector ensures compatibility with μ TCA-based infrastructures but can also be used for bench-top usage. It provides high-speed connectivity and supports a wide range of data transfer protocols to the backplane. Two FPGA Mezzanine Card (FMC) connectors are included as a flexible access to the FPGA I/O. They consist of two-pin Samtec SEARAY sockets [77] fully compatible with Low Pin Count (LPC) FMCs but also support access to high-speed serial lines as defined by the High Pin Count (HPC) FMC pinout. These connectors can host, for example, FMC cards with

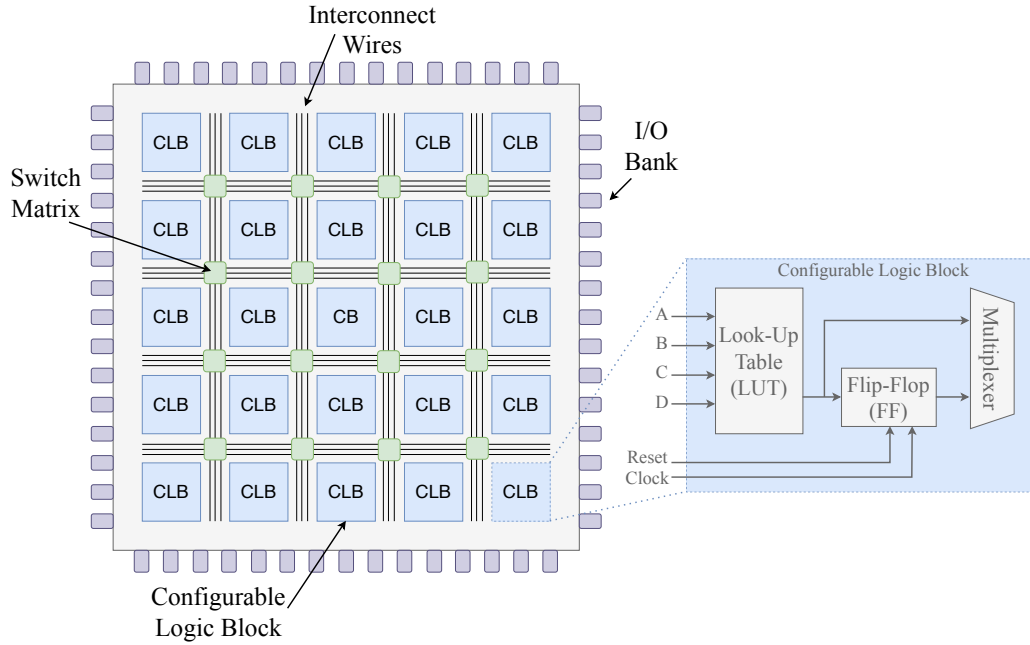


Figure 7.9: Block diagram of a simplified FPGA architecture and Configurable Logic Block structure.

optical transceivers (ie: SFP+) in the case optical data readout, or FMC cards with High Dynamic Range (HDR) cable connectors in the case of electrical control and data readout. As far as external memory is concerned, a 4 Gb Double Data Rate 3 (DDR3) memory is included and can support data transfer rates of up to 30 Gbps. For advanced clock distribution, the FC7 integrates an ASIC used for high precision control of the frequency and phase of the clocks provided to various processing blocks in the user firmware. Finally, a μ Secure Digital (μ SD) slot is provided to host a memory card on which multiple FPGA firmware versions, dedicated to different purposes or systems, can be stored.

7.3.2 Micro-Data Trigger & Control Firmware

The μ DTC firmware is an FPGA program dedicated to the control and readout of the Outer Tracker front-end objects (hybrid circuits, assembled modules) and systems (hybrid test system), as well as the control of the FC7 peripheral devices. The program is a structure of processing blocks supporting all the necessary features required by the various components and systems. Figure 7.10 shows a block diagram representing the structure of the μ DTC firmware used on the FC7 board.

The firmware can be divided into two core blocks: the System Core and the User Core. The System Core is a basic system firmware block which is provided by the FC7 designers

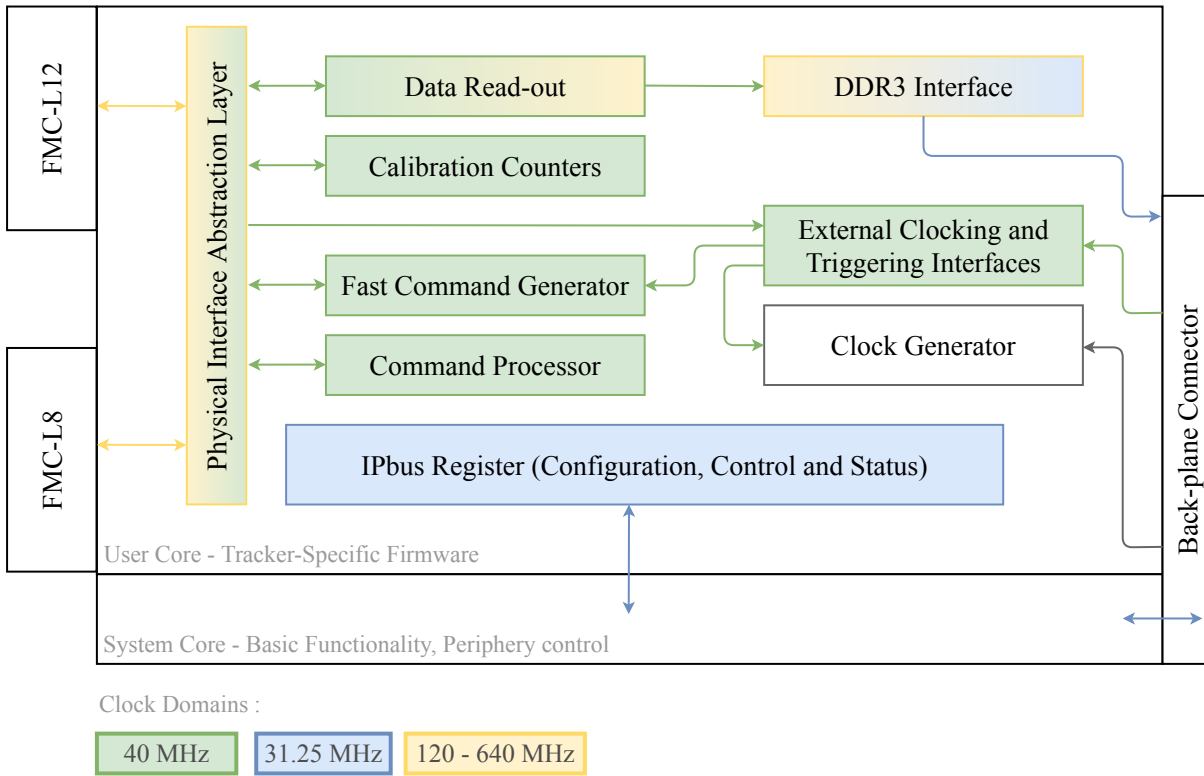


Figure 7.10: Top-level block diagram of the μ DTC firmware where color coding represents different clock domains and gradient colors clock domain crossings.

and which implements the basic features of the FC7. These include the control of peripheral devices, the μ TCA compatibility and the FC7 communication protocol. It does not require any change by the user but only needs to be complemented with a user-specific firmware block to extend the functionalities of the FC7 to custom user applications. As shown in the figure, this complement is provided by the User Core firmware. The latter is driven by the strong requirement of supporting the control and readout of all the various Outer Tracker front-end chips regardless of the test system used. The test systems described in Sections 7.1 and 7.2, rely on different control and readout interfaces. In the hybrid test system the communication with the front-end chips mostly relies on an electrical interface while in the single module test system it relies on an optical interface. For this purpose, the User Core firmware is designed around a configurable Physical Abstraction Interface Layer (PIAL) that allows for the firmware to be adapted to each of the aforementioned use cases. This PIAL layer, which takes care of the signal pin assignment and all the low-level hardware interfacing, also acts as an abstraction interface to all the generic and common firmware blocks responsible for the control, readout and triggering. This design approach provides high flexibility to the system and allows an easy integration

of any new firmware block regardless of the used communication interface. This section provides an overview of the most important blocks of the μ DTC firmware User Core.

IPbus Registers

The IPbus protocol [78] is a simple communication protocol based on data packet transfer between a control computer and an FPGA-based Telecommunications Computing Architecture (TCA) compatible device. It relies on a tightly-integrated software and firmware suit which can be used to develop high performance and reliable control systems. The protocol is transactional and relies on the exchange of 32 bit wide word packets on a dedicated bus offering 32 bit address space and 32 bit data transfer. In the case of the FC7, the implementation of the protocol is integrated to the System Core. Only the IPbus registers are part of the User Core. The communication between the FC7 and the control computer is built around System Core implementation of the IPbus protocol and a set of modifiable 32 bit registers, individually assigned to specific firmware blocks, and accessible to the user through the IPbus software interface. These registers are divided into three categories: Configuration, Control and Status registers. They allow for dynamic configuration, control and monitoring of each individual processing block of the User Core firmware.

Clock Generator

The Clock Generator block is in charge of generating and distributing all the necessary set of clock frequencies required by the firmware synchronous processing blocks. It requires the provision of a reference clock signal from which all the other clock signals are derived. In practice, the reference clock can either be provided internally from the FC7 on-board oscillator or externally through the backplane connector or FMC-L8 connector. Dedicated IPbus registers are provided such that the clock source can be dynamically programmed. Typically, for devices dedicated to LHC operation, the reference clock frequency corresponds to the bunch crossing frequency of 40 MHz. It is therefore used as a basic frequency for most of the μ DTC firmware processing logic. However, certain firmware blocks require different clock frequencies, higher or lower depending on the use case, and the 40 MHz clock is used to derive frequencies ranging from 5 MHz to 640 MHz.

Fast Command Generator

To ensure synchronization of the detector modules during data taking, as well as deliver trigger signals, the module front-end uses so-called *fast commands*. They are generated at

40 MHz and passed to the Physical Interface Abstraction Layer where they are forwarded to the front-end chips at 320 MHz. The front-end operation defines three categories of fast commands: Reset, Calibration Pulse and Level-1 Accept. The reset signals are used to synchronize the front-end chips by resetting the corresponding buffers, counters and state machines. The Calibration Pulse signal is used to trigger the front-end injection circuit to release a configurable charge into selected front-end channels. Finally, the Level-1 Accept signal is used to trigger the readout of the full event data from the front-end chips. As far as the trigger signal is concerned, the Fast Command Generator can either provide them from an external source or generate them internally according to a certain trigger scheme. The trigger schemes correspond to a designed sequence of fast command signals. In the basic trigger scheme, or *random* trigger scheme, Level-1 Accept trigger signals are generated at a frequency ranging from 1 KHz to 1 MHz with the possibility to generate triggers by introducing configurable delays between the Calibration Pulse and the Level-1 Accept signal. In addition, a so-called *antenna* trigger scheme is provided to control the shutter of the antenna circuit on the FEH test card used in the context of FEH circuit qualification. For the case of PS front-end chips, a *fast counters* trigger scheme is dedicated to the control of the SSA and MPA shutter used in the case of the asynchronous counter readout mode. Finally, a *stub* trigger scheme is provided and offers the possibility to generate trigger signals based on the stub information received from the front-end chips, such that a trigger signal is generated if one or multiple stubs are detected.

Command Processor

The Command Processor is in charge of the so-called front-end *slow control* which corresponds to the control and configuration of the front-end chips. Figure 7.11 shows a flow diagram of the Command Processor. While the previous version was centered around an implementation of the Inter-Integrated Circuit (I²C) protocol used for the front-end communication, the latest version is designed to ease the integration of more protocols and functionalities. The Core of the processor consists of two *Arbitrators* which act as managers distributing user-defined tasks to be performed by a set of so-called *Workers*. These workers must be implemented by the user and can be purposed for any use case. For example, in the case of the module control and configuration, a worker dedicated to the control and configuration of the front-end chips via the lpGBT was developed. In addition, to allow for multi-command transactions, a queueing mechanism is implemented using FIFO buffers which also act as clock domain crossing circuits moving data from the 31.25 MHz IPbus clock domain to the User Core 40 MHz clock domain and vice-versa.

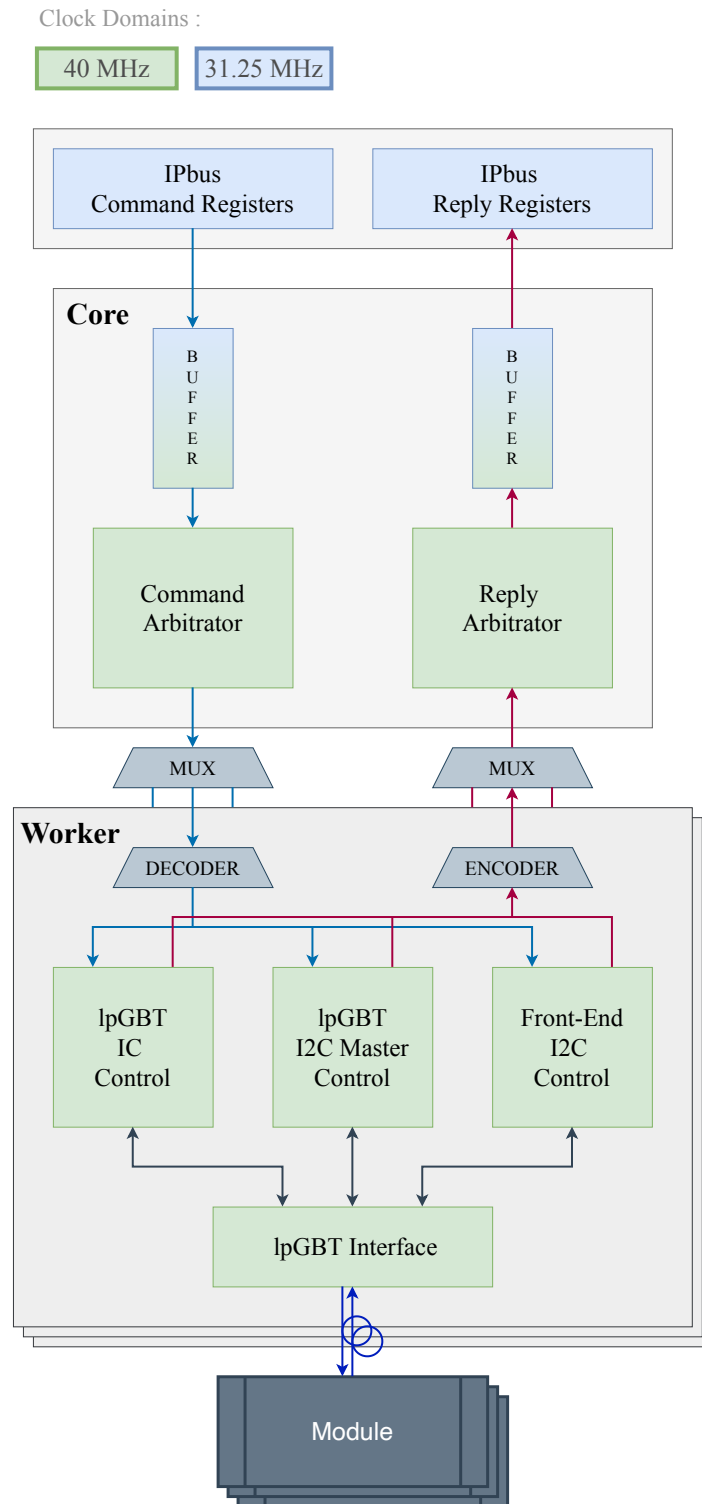


Figure 7.11: Process flow diagram of the command processor. It consists of two Arbitrators (Command and Reply) that act as managers distributing user-defined tasks to a set of Workers in charge of performing them. For Outer Tracker modules, a Worker exclusively dedicated for the control and configuration of the front-end chips via the lpGBT was developed.

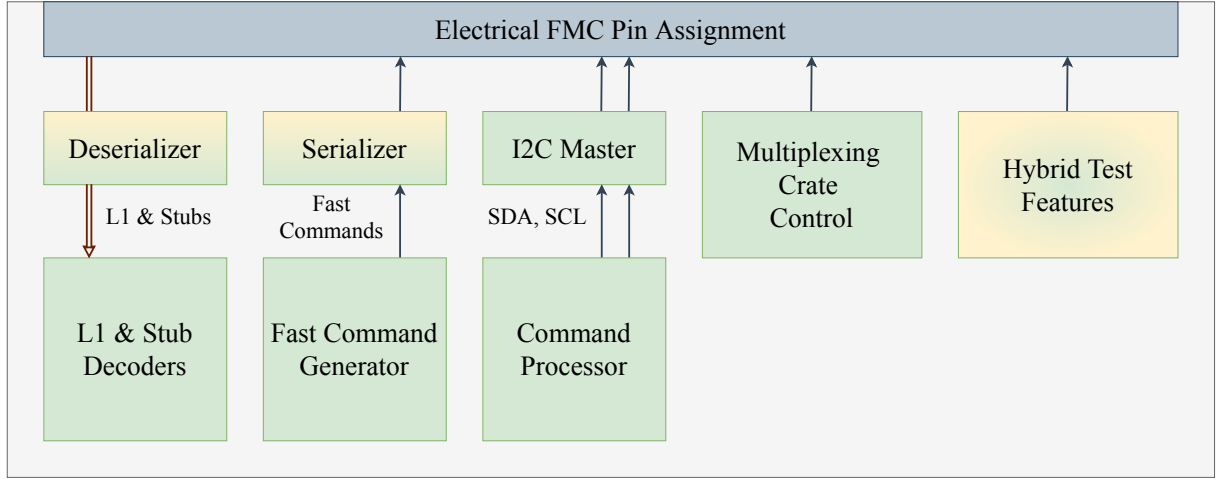
Finally, the control and status monitoring of the command processor is achieved through 32bit word commands and replies handled via dedicated registers integrated to the IPbus interface. The benchmark studies performed on the new processor design yield a considerable improvement offering control and configuration speed 16 times faster than the previous design.

In practice, in order for a command to be properly processed, it needs to encode the Worker's identification number, the identifier of the function to be performed and any set of arguments needed by the function. The command is therefore distributed to its corresponding Worker by the Command Arbitrator, and the user can monitor the progress of the task via dedicated IPbus registers. Once the task is finished, a task report is forwarded by the Worker to the reply Arbitrator and can be collected by the user through the IPbus interface. Such a design, driven by the concepts of queueing, Arbitrators and Workers, allows to reduce the load on the IPbus interface and provides the possibility to move software algorithms to the FPGA. This is of particular interest as in some cases slow control procedures can be very time consuming if mostly handled at the software level. The first Worker to be integrated to the Command Processor is the so-called *lpGBT Worker*. It provides an implementation of the lpGBT IC control protocol on which the configuration and control of the lpGBT is based. In addition, it provides an implementation of the lpGBT I²C Masters control. Finally, based on the aforementioned I²C Masters control, the front-end chip configuration protocol is implemented and allows the control and configuration of all the front-end chips. This Worker, coupled to the multi-command capabilities, provides a fast access to the front-end configuration registers, mostly benefiting the MPA configuration where more than ten thousand registers need to be accessed during configuration.

Physical Interface Abstraction Layer

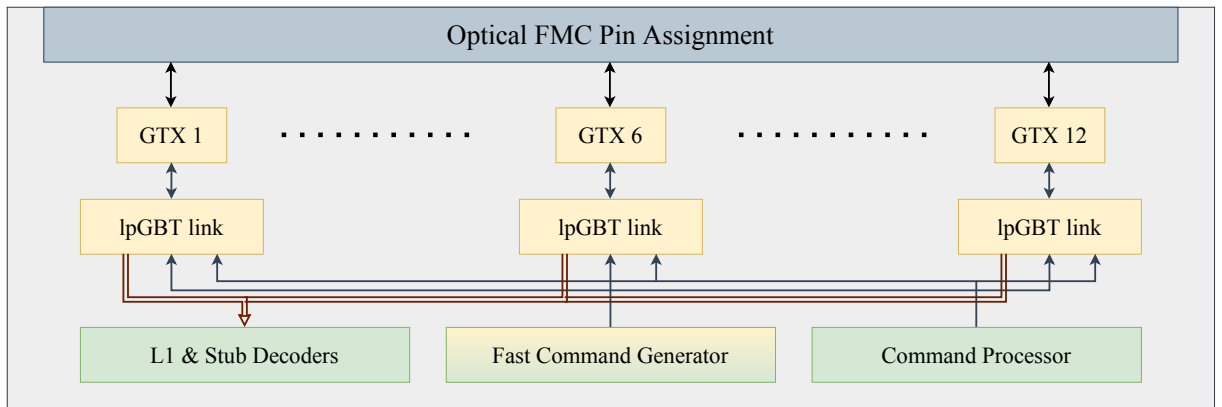
The Physical Interface Abstraction Layer (PIAL) is a highly flexible block that provides low-level adaptation of the firmware for all the front-end chips and communication interfaces that need to be supported. In total, five front-end chip types (CBC, SSA, MPA, CIC, lpGBT) and two communication interfaces (Electrical, Optical) need to be supported. This flexible support corresponds to the various test systems used for each of the front-end ASIC, MaPSA, hybrid circuits and assembled modules qualification. Simplified structural diagrams of both the electrical and optical implementation of the PIAL are shown in Figure 7.12.

Clock Domains :



(a)

Clock Domains :



(b)

Figure 7.12: Simplified block diagram of the electrical (a) and optical (b) implementations of the Physical Interface Abstraction Layer. The electrical implementation is based on a direct connection between the FPGA and the front-end data and control signals. In the optical implementation, the communication with the front-end chips is achieved via the lpGBT chip.

In the case of the electrical implementation shown in Figure 7.12(a), the FPGA has a direct access to the control and data lines from the front-end chips. Therefore, the PIAL provides data serializers (OSERDES) and deserializers (ISERDES) using 8 bit blocks to ensure the transition between the 40 MHz and the 320 MHz clock domains. In particular, they are used for the deserialization of the incoming 320 MHz front-end data, or the serialization of the outgoing 320 MHz fast command signals received from the Fast Command Generator. It should be mentioned that in order to ensure a proper deserialization of the data, the serializers and deserializers are complemented with a phase tuning block used to achieve an optimal sampling of the data. It relies on a constant data pattern sent by the front-end chips and used as a reference to find the phase at which the data bit is sampled in the middle, away from the bit transition. In addition, configuration and control of the front-end chips is ensured by an I²C Master block integrated to the Command Processor. Finally, the PIAL provides a multiplexing crate control block dedicated to the control of the multiplexing backplane featured by the hybrid test system crate, complemented by a set of hybrid circuit test features such as data generators, clock testers and fast command checkers that are described in Section 8.1.

In the case of the optical implementation, the FPGA doesn't have direct access to the front-end chip control and data lines. The link between the FPGA and the front-end chips is established optically via the lpGBT chip. On the FPGA side, in the case of multiple PS modules for example, the optical communication with each individual lpGBT is achieved using multiple instantiations of Xilinx GTX transceivers [79] which connect to the SFP+ optical transceivers corresponding to each optical link. The latter also ensure the proper serialization and deserialization of the data streams. The communication then relies on an FPGA implementation of the lpGBT protocol that abstracts the decoding and encoding of the uplink and downlink data streams, namely the lpGBT data frames, respectively. It acts as an interface for the transmission of slow control and fast command signals, and for the extraction of the L1 and stub data of each connected module. In the latest version of the PIAL, up to 12 GTX transceivers can be instantiated thus allowing the control and readout of up to 12 modules at a time.

Finally, to ensure a full abstraction of the incoming and outgoing data, both the electrical and optical implementations provide data decoders that are used to decode L1 and stub data extracted from the deserialized data stream, and form generic chip-agnostic event data which are forwarded to the data readout block described in the next section.

Data Readout

The Data Readout block is where all the data processing, aggregation and event creation is performed. Figure 7.13 shows the flow diagram of the block. It receives and buffers the deserialized L1 and stub data streams from the Physical Interface Abstraction Layer data decoders. A configurable data delay is included on the stub data path to allow matching of the asynchronous L1 data to the synchronous stub data. This delay is needed as the L1 data and stub data are received by the back-end system asynchronously. Therefore the stub data needs to be delayed in order to be matched to its corresponding L1 data. The buffered data is then collected by a Data Processing Manager and combined into a single event by dedicated Data Packing Nodes. In addition, instead of packing data sequentially, the packing is performed in a parallel fashion and at a clock frequency higher than the nominal one. This way the system is capable of sustaining the maximum 750 KHz data readout rate. In practice, the packing is implemented using a 160 MHz clock frequency, offering a processing speed gain of a factor of four compared to a processing at the nominal 40 MHz frequency. The gain is further improved by using a time-multiplexing technique that consists of instantiating multiple data packing nodes capable of processing events in parallel, thus further reducing the effective processing time. Finally, the data is complemented with general information about the event, aggregated into an event structure with a generic format and forwarded to the DDR3 packing block where it is written into the DDR3 memory and can be accessed through the IPbus interface.

Resource Utilization

The FPGA resources deployed by the aforementioned firmware is a central aspect of the design. The logic must be implemented such that the available resources are not exceeded and that logic congestions affecting the resource placement on the FPGA is avoided. Therefore, resource utilization measurements of all the set of firmware implementations supporting the various test systems were conducted. They are of particular importance as they allow to identify the most resource intensive firmware blocks and thus guide the type of design optimization to be performed. Table 7.1 shows the resource utilization of the common μ DTC firmware blocks in the case of the implementation expected to use the highest amount of resources, namely the optical implementation for 12 PS modules. The table indicates the percentage of logic elements deployed with respect to the total available resources. Here, logic elements are referred to as a *Slices* which, in the jargon of the Xilinx FPGA, correspond to a logic block containing four LUTs, eight FFs as well as multiplexers, such that two slices form a single CLB.

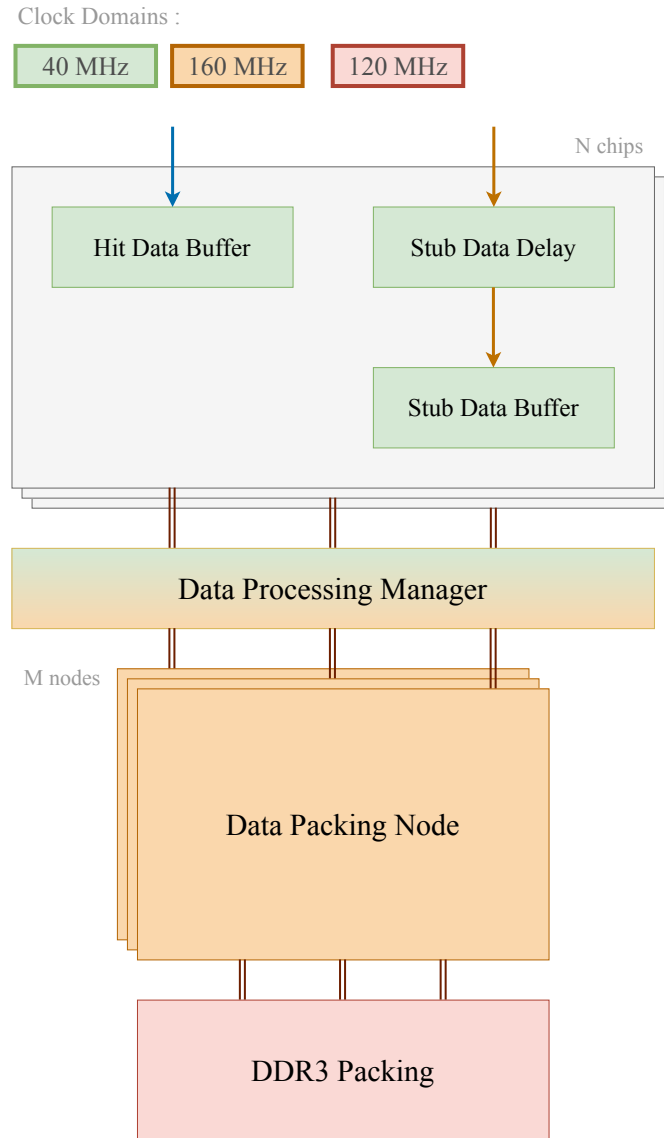


Figure 7.13: Flow diagram of the data readout block. The hit and stub data are received from the PIAL decoders. Data is then processed, aggregated and framed in dedicated Data Packing Nodes. Finally, the event is forwarded to the DDR3 Packing module before being written to the DDR3 memory.

Table 7.1: Resource utilization for the common μ DTC firmware blocks in the case of the multi-module optical readout implementation.

Firmware Block	Resource Utilization (%)			
	Slices			RAM
	LUTs	FFs	MUXs	
System Core	1.66	1.16	0.13	0.02
IPbus Registers	10.95	15.27	17.75	0.06
Fast Command Generator	0.93	0.38	0.19	0.23
Command Processor	4.47	2.26	0.08	3.83
PIAL	36.24	27.18	0.78	0
Data Readout	11.24	6.54	3.79	47.01

As mentioned earlier, the optical implementation for 12 modules is the most resource intensive and is taken as a baseline for the upper limit studies of the resource utilization. From the table, the observed high percentage of resources used in the PIAL and the Data Readout path is justified by all the processing logic needed to receive and decode the data from the front-end chips. On the other hand, the comparable amount of resources deployed in the IPbus Registers block is unjustified and yields the need of further optimization of the implementation. The high volume of resources deployed for the IPbus registers might lead to congestion and thus difficulties to place additional logic if the firmware happens to be extended with more resource intensive data processing. Finally, the Fast Command Generator and the Command Processor don't yield a significant resource utilization. It should be also mentioned that the electrical implementation deploys five times less resources for the Command Processor and the Fast Command Generators blocks. This is mainly due to the support of fewer front-end chips as only a single chip or hybrid circuit can be read out, in addition to the fact that the new design of the Command Processor is exclusively deployed for the optical implementation.

Figure 7.14 shows the inclusive resource utilization for the firmware implementations dedicated to the PS module test systems. The obtained results allow to conclude that the available resources on the FC7 are sufficient to implement the control and readout of all the Outer Tracker systems, with the multi-module readout being the most resource intensive. The resource utilization for the PS-POH system is not shown as, in practice, the firmware is only used for the multiplexing backplane control and no front-end control

or readout is taking place. As of today, in the case of the optical implementation, up to 12 modules can be controlled and read out simultaneously. However, by means of further resource optimization, in particular of the RAM usage and with the help of some constrained logic placement (floor planning), it remains possible to increase the number up to the target case of 16 modules. This is of particular importance since the number of available FC7 boards is limited and such an improvement would benefit larger tests systems where more than 12 modules need to be tested.

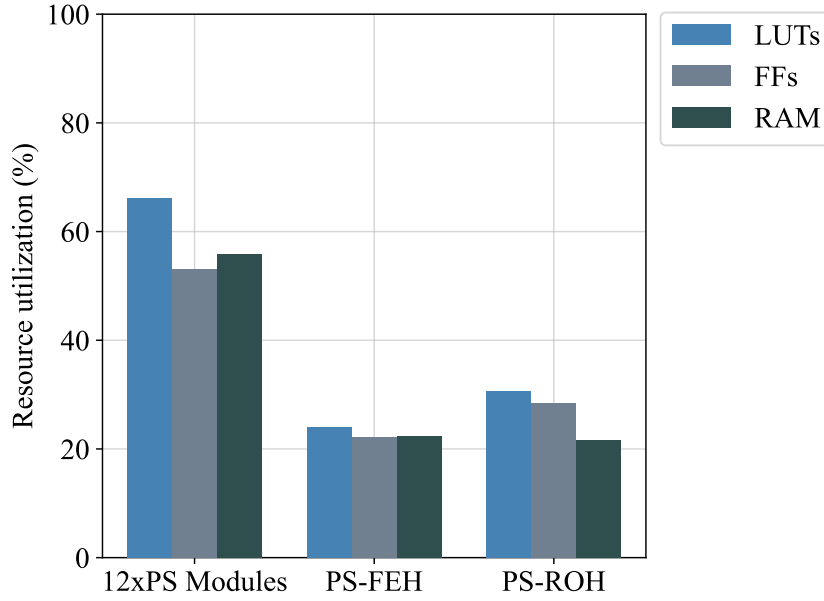


Figure 7.14: Total resource utilization for the μ DTC firmware implementations dedicated to the PS module test systems. The 12 Modules Test System corresponds to the optical implementation, while the PS FEH and PS ROH Test Systems both correspond to the electrical implementation.

7.3.3 Phase-2 Acquisition & Control Software

The Phase-2 Acquisition and Control (Ph2ACF) software is a software framework written in C++ and developed for the control and readout of the CMS Phase-2 Tracker detector. In addition, the framework is also used for the development of control and test routines needed during the prototyping and production phases of both the Inner Tracker and the Outer Tracker modules. It provides at its core a middleware Application Programming Interface (API) providing a description of the controlled system in addition to interface classes to access each individual front-end and back-end component.

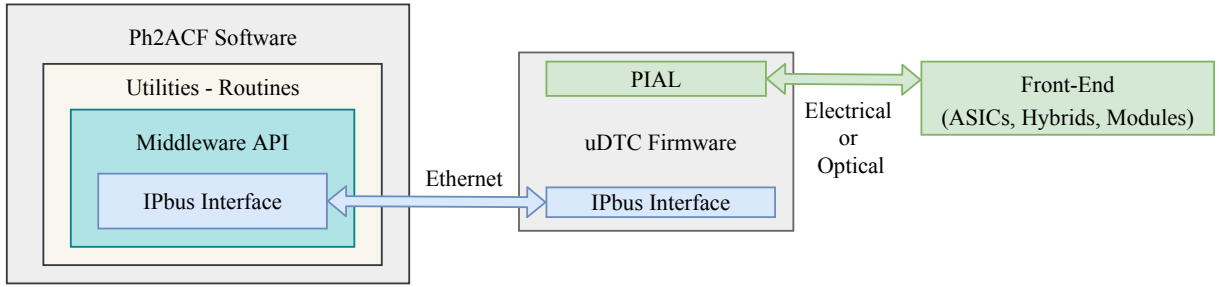


Figure 7.15: Block diagram showing the internal structure of the Ph2ACF software and how it links to the μ DTC firmware and the front-end objects.

Figure 7.15 shows a top-level diagram indicating the global structure of the Ph2ACF framework and how it relates to the μ DTC firmware and the front-end components. The middleware API layer is a hierarchical set of classes corresponding to the various system components. It consists of five core categories of classes: the Hardware Descriptors, the Containers, the Hardware Interfaces, the File Parser and the System Controller. Figure 7.16 shows a simplified diagram indicating the class hierarchy and relations in Ph2ACF.

Hardware Descriptors: The Hardware Descriptors, shown in grey in Figure 7.16, correspond to a set of classes representing each electronic component of the detector system. For example, in the case of the Outer Tracker system, these correspond to classes representing the FC7 board (*BeBoard*), the module (*OpticalGroup*), the hybrid circuits (*Hybrid*) and their corresponding front-end chips (ie: CIC, SSA, MPA and lpGBT described by the *Chip* and *OT_Chip* classes). They hold component-specific attributes and functions giving access to description information such as identification numbers or configuration registers.

Containers: Shown in yellow in Figure 7.16, they are tree structures corresponding to each component type in the system and arranged in a structure exactly similar to the system hierarchy. They consist of containers holding multiple instantiations of Hardware Descriptors such that the entire system is described. The top layer of the hierarchy structure is the *DetectorContainer* while the bottom layer are *ChipContainers*. In between, containers corresponding to the back-end board (*BoardContainer*), optical groups or modules (*OpticalGroupContainer*) and hybrids (*HybridContainer*) can be found.

Hardware Interfaces: The interface classes provide functional access to the system components. Each class provides a set of functions and routines used to configure, control

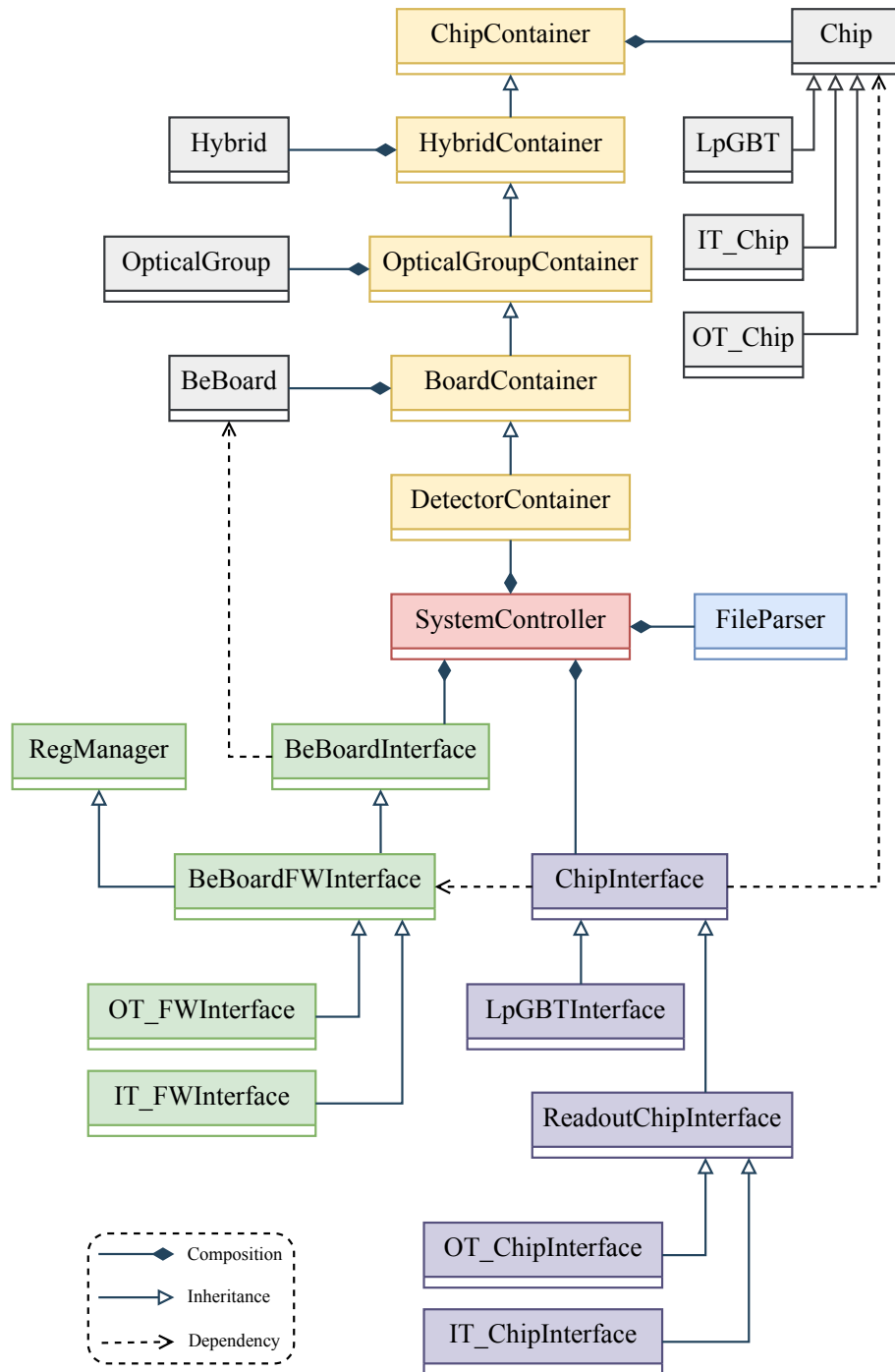


Figure 7.16: Simplified diagram showing the Ph2ACF Middleware API class hierarchy. Hardware Descriptors are depicted in grey, Container in yellow, Hardware Interfaces in green and purple, the File Parser in blue and the central System controller in red.

and read out the corresponding component. As shown in green and purple in Figure 7.16, they are divided into two categories: Back-End Interfaces (*BeBoardInterface*) and Chip Interfaces (*ChipInterface*). Back-End Interfaces can support the control and data readout of any type of back-end system through a dedicated Firmware Interface implementation. In the case of the FC7 board, depending on whether it is operated with the Outer Tracker μ DTC firmware or the Inner Tracker one, a suitable interface can be used. In both cases, the link to the board is achieved via the *RegManager* class which provides a software implementation of the IPbus communication protocol. On the other hand, Chip Interfaces implement the control of the individual front-end chips via an interface that relies on both the chip Hardware Descriptors and the Back-End Interfaces such that the descriptors provide the necessary chip information while the interface provides access to the physical chip.

File Parser: The instantiation of the system tree structure and the corresponding component interfaces is subject to a description of the system provided in a corresponding configuration file. The latter is parsed by the so-called *FileParser*, shown in blue in Figure 7.16 at run time such that the software hierarchical structure is created by the *SystemController* described below.

System Controller: The System Controller, shown in red in Figure 7.16, is the central part of the class hierarchy. It holds references to each of the File Parser, the Containers, the Hardware Descriptors and the Hardware Interfaces. In addition, as mentioned before, using the parsed information from the configuration file, it is in charge of the instantiation of the software hierarchical structure of the system and the assignment of the proper hardware descriptors and interfaces to each container layer.

Apart from the core middleware API which mostly acts as an interface to the system components, the framework provides a set of classes to perform all sorts of qualification tests. These classes, referred to as *Tools*, inherit the system description and interfaces from the System Controller and implement various application-specific test routines. In the case of the Outer Tracker systems for example, tools dedicated to each of the hybrid circuits and the fully assembled modules qualification, both in the laboratory and during test-beam campaigns as described in Chapters 8 and 9, respectively, are provided. In particular they allow the control of the various test systems, the electrical qualification of the hybrid circuits, as well as the front-end calibration and electronic noise characterization.

The Ph2ACF framework also allows controlling external devices, such as power supplies

and oscilloscopes. This feature is of particular interest for routine automation purposes where parameters from external devices need to be modified in the course of the test. The interface between the framework and the external devices relies on a network connection between an *External Device Interface* incorporated in the framework and an *External Device Controller* providing a direct access to the device. This way, commands can be sent from Ph2ACF to the device controller and further dispatched to their corresponding device via any kind of control interface.

In addition, the framework exploits multi-threading, thus allowing for parallel processes to be running simultaneously. This is of particular interest in cases where a calibration routine needs to be ran while monitoring data such as temperature and power from the front-end electronics if performed. As far as data processing is concerned, the multi-threading approach mainly benefits the Inner Tracker for which the complexity of the data exceeds that of the Outer Tracker.

Finally, in order to make the system control as easy as possible, Graphical User Interfaces (GUIs) are provided for each of the Inner Tracker modules, Outer Tracker modules, and Outer Tracker hybrid circuits qualification. All GUIs are based on the *Qt-python* package and are entirely decoupled from the Ph2ACF Middleware API in terms of code dependency as they communicate with Ph2ACF through so-called *named pipes*. The latter are a type of Inter-Process Communication (IPC) mechanism that allows processes to exchange data through dedicated communication channels. These GUIs will be crucial for the detector production phase where systems will be operated by non-experts such that all the framework complexity and process flows will be abstracted to the users.

The next chapter will focus on how all these hardware, firmware and software systems are employed for the purpose of qualifying both individual components and fully assembled modules. It will mainly cover the qualification of PS hybrid circuits and single prototype modules, describing the preliminary set of the tests developed for this purpose and setting the road for the foreseen production phase.

CHAPTER 8

PIXEL-STRIP MODULE LABORATORY QUALIFICATION

During the production phase of the Outer Tracker, thousands of pixel and strip sensors, front-end chips, hybrid circuits and assembled modules will have to go through a thorough qualification process. The objective is to perform a set of functional tests to characterize each individual component, act on potential issues, and ensure that only those of the highest quality are provided for the final detector integration. In particular, these tests need to cover the mechanical and electrical verification of the hybrid circuits and sensors, the control and readout functionalities of the front-end chips, and the performance of the assembled modules. All qualification results will be stored on a central data base that will be used to track every individual component throughout the production phase. For the individual components, namely the sensors, the front-end chips and the hybrid circuits, the qualification will be performed at the vendor and will be complemented by sample testing at participating institutes. Following reception of the individual components at module assembly centers or reception of the fully assembled modules at integration centers, each assembled module will undergo a series of quality control tests starting with qualification at room temperature, followed by thermal cycling tests or what is referred to as *burn-in* tests, and ending with integration tests on final mechanical structures such as TEDD Dees.

As of today, qualification of the strip and pixel sensors is the most mature among all while that of the hybrid circuits, the MaPSAs and the assembled modules is still being defined. This chapter provides an overview of a subset of the PS module and hybrid

circuits qualification tests developed in the context of this thesis. It mainly focuses on the pre-assembly functional tests of the PS hybrid circuits, and the post-assembly functional tests of fully assembled modules both in laboratory and in test-beam campaigns. The latter are of particular importance as they allow the qualification of modules under beam exposure and are an occasion to exercise the functional operation while studying the sensors and readout chain performance, in particular the p_T discrimination implementation. Contributions from the author include the development of firmware blocks and software tools for the qualification of the hybrid circuits, in particular the ROH, and development of software tools for the qualification of assembled PS modules both in laboratory and in test-beam campaigns.

8.1 Hybrids Qualification

Prior to distribution to the module assembly centers, every hybrid circuit is subject to extensive functional testing both at the vendors and at institutes such as CERN. As already mentioned and described in Section 7.1, the use of the hybrid test systems allows sequential testing of up to twelve hybrids. Each hybrid is mounted onto its corresponding test card and plugged into its dedicated multiplexing backplane slot inside the test crate. The crate control, card selection and test procedures are all performed from a dedicated computer using the Ph2ACF software framework, and the test results are summarized in a corresponding output file. While in practice the system is operated using Ph2ACF terminal commands, the framework also offers the possibility to abstract the operational aspects to the user through a Graphical User Interface (GUI). The latter allows the control of the test system and procedures, and the upload of the corresponding results to the data base. Each list of qualification tests is divided into multiple categories that target different functionalities of the circuit. As far as test results are concerned, they are divided into two categories: *Pass/Fail* and *Status Check* results. The *Pass/Fail* category is dedicated to the most critical features of the hybrid circuit. In this sense, considering the test as successful is subject to very strict requirements that shall either be passed or not. On the other hand, features which are no less important but can produce more elaborate outputs are qualified using the *Status Check* category. In the latter, a more detailed output is produced which can be in the form of a list of values or figures.

Figure 8.1 shows a generalized flow diagram of a hybrid circuit test. First, the crate backplane slot corresponding to the test card with the hybrid circuit to be tested is selected. Following the selection, the hybrid is powered and the front-end chips configured.

Finally, the hybrid-specific test sequence is launched and the corresponding results are verified by experts before being uploaded to the data base. This section provides an overview of the tests implemented for each PS hybrid circuit, giving a detailed description of the most important ones.

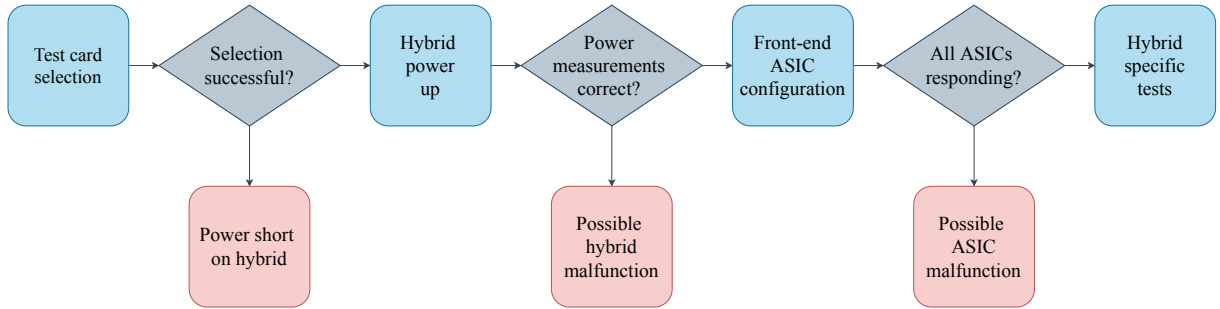


Figure 8.1: Generalized flow diagram of a hybrid circuit test [80]. First, the test card hosting the hybrid circuit to be tested is selected. The hybrid circuit is then powered, the front-end chips, if present, are configured and the test sequence is launched. The final results are uploaded to a central data base.

8.1.1 Front-End Hybrid Tests

In the case of the front-end hybrid circuits, it is critical to look for potential failures on the power, control and data communication lines of the SSA and CIC front-end chips. On the one hand, power verification measurements performed on the test card ensure that enough power is provided to the hybrid circuit prior to the functional tests. On the other hand, the data communication validation covers the verification of the data transmission on the SSA data output lines, and the CIC input and output data lines. In addition, the SSA input wirebonding pads are tested for shorts and opens using the antenna feature described in Section 7.1.2. Finally, for the control path validation, the chip configuration over I²C and the transmission of clock, reset and fast command signals are tested. Figure 8.2 shows a block diagram indicating the main electrical paths tested on each hybrid circuit and a set of preliminary functional tests is listed in Table 8.1.

The I²C communication and the ASIC configuration tests establish the communication with the front-end chips while bringing them to an operation readiness state. Data alignment procedures then ensure a correct sampling and decoding of the L1 and stub data on each of the CIC input and output data lines. These are described in details for the case of an assembled module in Section 8.2.3. Finally, threshold equalization, noise measurement and hybrid connectivity tests are performed. In practice, the threshold equalization

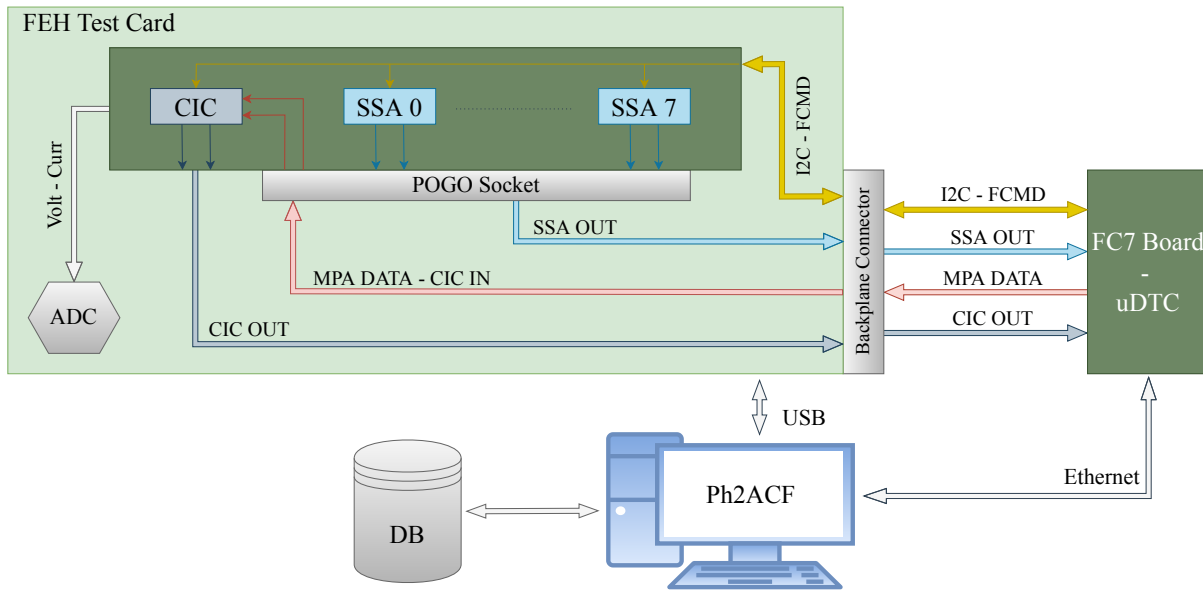


Figure 8.2: Block diagram of the PS Front-End Hybrid test. The validation of each hybrid circuits mainly focuses on the verification of the SSA and CIC control and data communication.

and the noise measurement, which are described in detail in Sections 8.2.4 and 8.2.5, are needed to equalize the analogue signal threshold across the SSA front-end readout channels and measure the corresponding electronic noise. The latter is particularly needed for the hybrid connectivity tests used to verify the integrity of the hybrid signal traces and the quality of the data transmission which will be the focus of this section.

SSA OUT: It is dedicated to the verification of the data transmission on the SSA output data lines. In an assembled PS module, the SSA output data lines are connected to dedicated MPA input channels. However, in the context of hybrid circuit qualification, the MPA chip is absent. The FC7 is therefore used as a replacement. The SSA SLVS output lines are connected to the FC7 FPGA inputs via the HDR cable and the μ DTC firmware PIAL block provides features used for the reception and validation of the transmitted SSA data. In practice, a subset of the SSA chips are sequentially selected and programmed to generate data according to a fixed data pattern (ie: 11001010). The data pattern is then serialized at 320 Mbps on the SSA output L1 and stub data lines. At the FC7 inputs, the data pattern is recovered and compared to the transmitted one. A data line is then reported to be failing if the recovered data pattern doesn't match the transmitted one.

CIC IN-OUT: This test allows the verification of the data transmission on the CIC input and output data lines. In an assembled PS module, the CIC data lines are connected to

Table 8.1: Preliminary list of front-end hybrid functional tests indicating the category, the test and the result type. "PASS/FAIL" corresponding to binary success or failure result, while "STATUS CHECK" corresponds to a more elaborate report.

Test category	Test step	Result type
Power verification	Test cards voltages	PASS/FAIL
	Hybrid voltages	PASS/FAIL
I ² C communication	CIC write/read	PASS/FAIL
	SSA write/read	STATUS CHECK
ASIC configuration	CIC / SSA configuration	STATUS CHECK
	CIC start-up	PASS/FAIL
Data alignment	MPA-CIC data alignment	STATUS CHECK
	CIC-BE data alignment	PASS/FAIL
Threshold/Noise measurement	Threshold equalization	STATUS CHECK
	Noise measurement	STATUS CHECK
Hybrid connectivity	Short finding	STATUS CHECK
	Open finding	STATUS CHECK
	CIC IN-OUT	STATUS CHECK
	SSA OUT	STATUS CHECK

dedicated MPA output and lpGBT input channels. However, dedicated μ DTC firmware data generation features allow to use the FC7 as an MPA data generator and an lpGBT data receiver. The MPA data generator firmware block is first programmed to generate data according to a fixed data pattern. From the FC7, data is then serialized on the corresponding CIC L1 and stub input lines at 320 Mbps. In the CIC, the data is directly forwarded to the corresponding output lines, completely bypassing the CIC internal logic. Finally, the CIC output data pattern is recovered back by the FC7 and compared to the transmitted one. A data line is then reported to be failing if the recovered data pattern doesn't match the transmitted one.

Open finding: The Open finding test is used to detect open (broken) SSA analogue input traces on the hybrid circuit. It makes use of the antenna feature on the hybrid test card and the capacitively coupled antenna trace on the hybrid circuit. As described

in Section 7.1.2, the antenna trace is positioned below the wirebond pads dedicated to the PS-s sensor and allows the injection of a charge at the level of the pad compared to the chip injection circuit which allows to inject charge at the input of the pre-amplifier. To detect the open traces, the SSA chips are first configured such that their input signal threshold is closely above the measured electronic noise level. The way the latter is measured is described in Section 8.2.5. The antenna circuit is then triggered such that enough charge is injected to generate a hit in a subset of pre-selected channels. The procedure is repeated to cover all the available channels, and a channel is then reported as being open if no hit is recorded following the charge injection.

Short finding: The Short finding test is used to detect shorted SSA analogue input traces on the hybrid circuit. Similarly to the Open Finding test, it makes use of the antenna feature, and the SSA threshold configuration prior to charge injection remains the same. For the test, a charge is injected in a subset of non-contiguous pre-selected channels and, instead of looking for recorded hits in the channels where charge was injected, hits are rather looked for in the neighbouring channels. The procedure is repeated until all available channels are tested. A line is then reported to be shorted if a hit is recorded on the neighbouring channel where no charge was injected.

8.1.2 Read-Out Hybrid Tests

For the read-out hybrid circuit, the functional qualification revolves around the validation of the lpGBT functionalities, in particular those related to the data communication and the front-end chip control. The verification of the data communication lines covers the transmission at the lpGBT input and output data lines and the corresponding bidirectional optical transmission to the FC7 board via the VTRx+. It includes the validation of the L1 and stub data transmission, as well as the transmission of the clock, reset and fast command signals. In addition, the most relevant lpGBT control blocks, such as the I²C Masters and the ADCs, are extensively tested.

It should be noted that for the ROH tests, two FC7 boards are used. The first board is referred to as the *Electrical* FC7. It provides control of the hybrid test system, generates data on the lpGBT data input lines, and provides electrical test features such as fast command signals recovery or clock signal tests described in the following paragraphs. The second board is referred to as the *Optical* FC7. It is dedicated to the optical control and configuration of the lpGBT chip, as well as the bidirectional optical data transmission. Both FC7s are controlled from the same computer using the Ph2ACF software from

where the test procedures are launched. Figure 8.3 shows a block diagram indicating the main power, control and data transmission lines verified for each hybrid circuit and the preliminary set of functional tests is listed in Table 8.2.

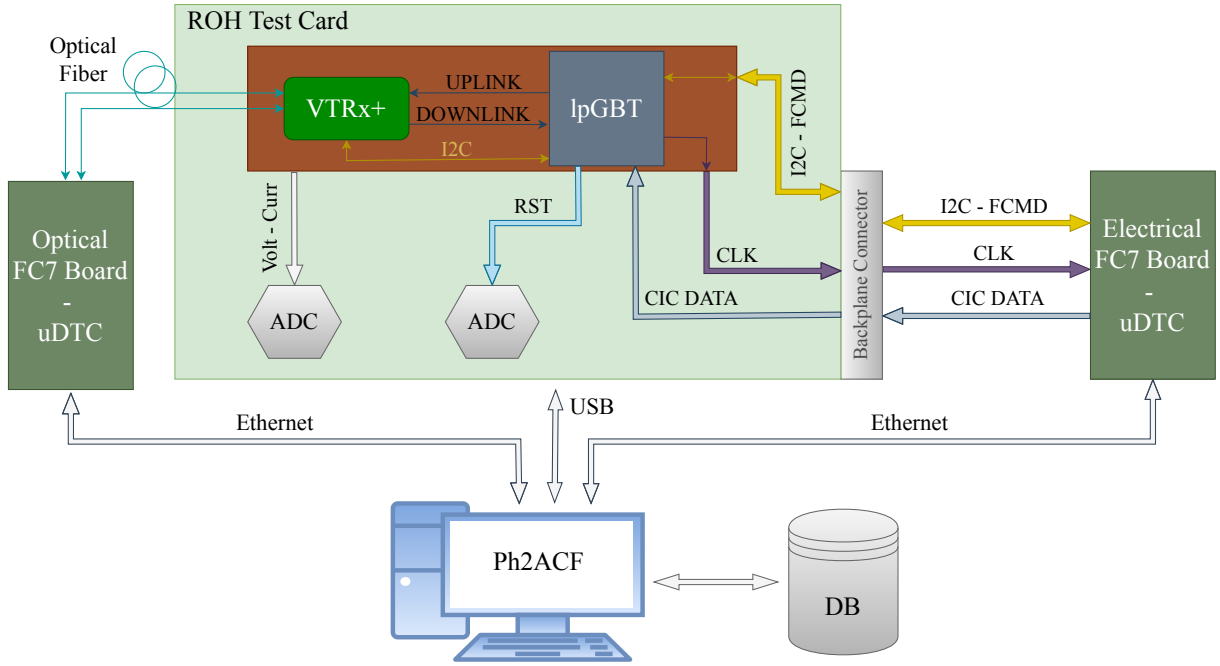


Figure 8.3: Block diagram of the PS Read-Out Hybrid test. The validation of each hybrid circuit mainly focuses on the verification of the lpGBT control and data communication verified. Two FC7 boards are used: the Electrical FC7 provides the crate control and hybrid electrical test features, while the Optical FC7 is dedicated to the bi-directional lpGBT data communication.

First, power verification is performed on both the hybrid circuit and the corresponding test card to ensure that the supplied voltages are within the specified operational ranges. The optical communication, which is described in detail for the case of an assembled PS module in Section 8.2.3, is then established and the lpGBT chip is configured. To ensure a proper sampling and decoding of the data transmitted on the lpGBT input lines, a tuning of the lpGBT sampling phase, also described for the case of an assembled PS module in Section 8.2.3, is performed by using the FC7 board as a CIC data generator. In addition, the functionality of some lpGBT blocks, in particular the I²C Masters and the eye opening monitor feature, are tested. Finally, the hybrid connectivity is verified by inspecting the transmission quality of the reset, clock, fast commands, and data signals. Descriptions in this section will mainly focus on the functionality and hybrid connectivity tests.

Table 8.2: Preliminary list of read-out hybrid functional tests indicating the category, the test and the result type. "PASS/FAIL" corresponding to binary success or failure result, while "STATUS CHECK" corresponds to a more elaborate report.

Test category	Test step	Result type
Power verification	Test cards voltages	PASS/FAIL
	Hybrid voltages/currents	PASS/FAIL
	Hybrid loaded voltages/currents	STATUS CHECK
Optical communication	Optical link lock	PASS/FAIL
	lpGBT configuration	STATUS CHECK
Data alignment	CIC-lpGBT phase alignment	PASS/FAIL
Functionality tests	I ² C Masters	STATUS CHECK
	Eye opening	STATUS CHECK
Hybrid connectivity	Reset	STATUS CHECK
	Clocks	STATUS CHECK
	Fast commands	STATUS CHECK
	Data IN-OUT	STATUS CHECK

Eye Opening: The Eye Opening test is used to verify the quality of the 2.56 Gbps downlink high speed input data fed to the lpGBT by measuring the corresponding eye diagram. The latter is a commonly used technique in digital communication systems to evaluate the quality of the transmitted signal. The measurement involves plotting a graph of the voltage or current waveform of a bit stream over time, such that bit transitions can be captured. To do so, the lpGBT provides a so-called *Eye Opening Monitor* [57] test feature that allows to make an on-chip eye diagram measurement of the high speed data.

Figure 8.4 shows the architecture of the Eye Opening Monitor feature (top left), the eye diagram measurement working principle (bottom left) and an example result of a measured eye diagram. In practice, the high speed data signal is a differential signal defined by its common mode voltage (VCM), ideally around 0 V, and its differential amplitude, typically 1.2 V. Therefore, in order to capture the differential signal, two parameters are provided by the lpGBT which need to be scanned in order to obtain an image of the eye diagram: a reference static voltage (V_{of}) and a phase interpolated sampling clock (clkPi). On the one

hand, the V_{of} voltage is used as a reference voltage to which the high speed data signal level is compared using a differential comparator such that the output of the comparator is toggled if V_{of} is within the high speed data signal voltage limits. In particular, a static '1' is produced if the V_{of} is above the limit, and a static '0' is produced if it is below. On the other hand the $clkPi$ sampling clock is used to sample the output of the differential comparator that is then fed to a 16bit counter. Finally, the eye diagram measurement is performed, following the working principle mentioned earlier, by scanning V_{of} (y-axis) and $clkPi$ (x-axis) while recording the number of counts (z axis) over a defined measurement duration. An eye diagram image can therefore be obtained, providing a direct visualization of the high speed data bit transition and allowing an assessment of the high speed data signal quality. On the example diagram, the eye opening in yellow corresponds to the space between the two voltage levels, upper and lower, of the digital signal that are used to represent a binary value of 1 and 0. The opening yields signal levels well within the expected voltage range. It is in particular crucial to assess how well the binary values are represented by the transmitted signal. Finally, the signal jitter that corresponds to the fluctuation of the bit transition slope around its ideal value is very low and thus allowing for good signal transitions between the binary values of 1 and 0.

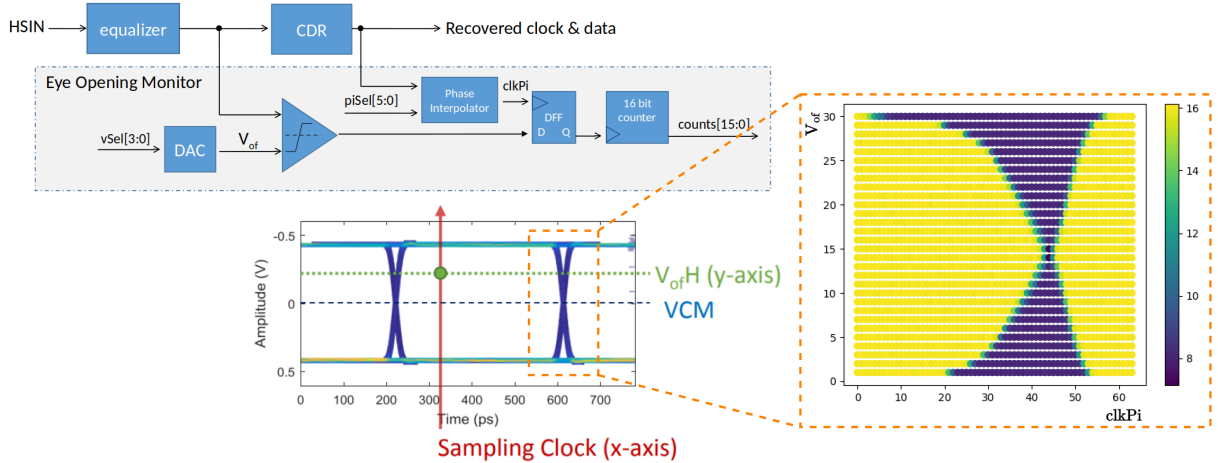


Figure 8.4: Eye Opening Monitor architecture (top left) and working principle diagram (bottom left). A static reference voltage V_{of} and a sampling clock $clkPi$ are scanned in order to obtain an eye diagram image as shown on the right [57].

Data IN-OUT: The DATA IN-OUT test is dedicated to the verification of the entire data path between the lpGBT and the FC7 board. It allows the validation of the electrical data transmission on the lpGBT input (ePortRx) and output data lines, and the uplink optical transmission of the same data via the VTRx+ module to the back-end system.

In an assembled PS module, the lpGBT input data lines are connected to CIC output channels. However, in the context of the ROH testing where no CIC chip is available, the FC7 is used as a CIC data generator. The μ DTC firmware provides a CIC data generator that can generate data at either 320 Mbps or 640 Mbps according to a fixed data pattern.

In practice, the electrical FC7 is programmed to generate data from the configured data pattern. The data is then serialized on the corresponding lpGBT L1 and stub data lines (ePortRx) at either 320 or 640 Mbps. At the lpGBT input, the data is received and the lpGBT Phase Aligner block is used to find the best phase for an optimal sampling of the data. Data from all input lines are then aggregated, encoded and serialized on the lpGBT output data lines to the VTRx+. The data is finally transmitted over the optical fiber to the optical FC7 board where it is recovered and decoded to extract data corresponding to each lpGBT input lines. A data line is reported to be failing if the recovered data pattern doesn't match the transmitted one.

Clocks: The lpGBT clock lines are crucial as they provide the reference clock needed for the front-end chips logic operation and the clocks test is used for their validation. To perform the test, the lpGBT Phase-Shifter circuit is programmed to output the 320 or 640 MHz differential clock signals on the corresponding clock output lines (eClocks). At the electrical FC7 where the signals are received, the μ DTC firmware features a clock test block used to compare the received clock to an internally generated reference one. To do so, a signal edge counting is used to compare the received clocks to the reference ones. The number of clock edges over a duration of 750 μ s is extracted from both the received signals and the reference ones. A clock output line is reported to be failing if the difference between its corresponding edge count and the reference edge count exceeds a 5 counts tolerance, equivalent to a clock frequency difference larger than 0.01%.

Fast commands: Fast command signals are central for the control and synchronization of the front-end chips. The fast commands test is therefore used for the verification of the transmission of fast command signals on the corresponding lpGBT output lines. It allows the validation of the fast command signals transmission path from the optical FC7 board to the front-end chips over the corresponding downlink data lines (ePortTx). The optical FC7 is configured to constantly send a fast command pattern in the form of *11000001* on the lpGBT downlink. The fast commands are then forwarded by the lpGBT on the corresponding downlink electrical links (ePortTx) which are connected to the electrical FC7. Finally, the fast commands are received by the FC7 and compared to the generated

ones. A fast command output line is reported to be failing if the recovered fast command pattern doesn't match the generated one.

Reset: Reset signals are of particular importance as they allow a reinitialization of certain front-end logic blocks. The reset test is therefore used for the verification of the lpGBT reset output lines. In the system, each of these lines are connected on one end to a configurable lpGBT GPIOs port that can act either as an input or as an output, and can either be at a voltage considered as high (1.2 V) or low (0 V). On the other end, the lines are connected to a test card ADC input that allows measurement of the GPIOs voltage level. For the verification, the reset lines are successively set to the high and low configurations. The voltage levels for each configuration are then measured and compared to the corresponding expected voltage levels. A reset line is reported to be failing if the difference between the measured voltage and the expected voltage exceeds an 8% tolerance corresponding to an absolute difference of 100 mV.

I²C Masters: As described in Chapter 5, the front-end chip register configuration uses the I²C protocol where the I²C Masters are integrated to the lpGBT chip and each front-end chip acts as an I²C Slave with a corresponding address. The I²C Masters test is therefore used for the functional verification of the lpGBT I²C Masters control and communication with the front-end chips. To cover the absence of front-end chips which act as I²C Slaves, the I²C data (SDA) and clock (SCL) lines are routed from the lpGBT to the electrical FC7 where the μ DTC firmware provides emulated I²C Slaves with a dedicated I²C protocol implementation and corresponding configurable registers. To perform the test, the lpGBT I²C Masters are controlled to initiate a configurable number of I²C transactions with the emulated Slaves. The report from each transaction is recorded, and an I²C Master is declared to be failing if at least one of the I²C transactions fails.

8.1.3 Power Hybrid Tests

The power hybrid validation is dedicated to the verification of the power distribution performance of the integrated bPOL DCDC converters. The objective is to ensure that an optimal power distribution of the 2.55 V, 1.25 V and 1.05 V supplies can be achieved over the whole range of input supply voltage and at all expected load conditions. On the test card, the load conditions are reproduced using configurable Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) complemented by resistors in series. The load value can therefore be configured and the corresponding output voltages and currents measured using test card ADCs. Figure 8.3 shows a block diagram indicating the main power lines

tested for each hybrid circuit and a preliminary set of functional tests is listed in Table 8.3.

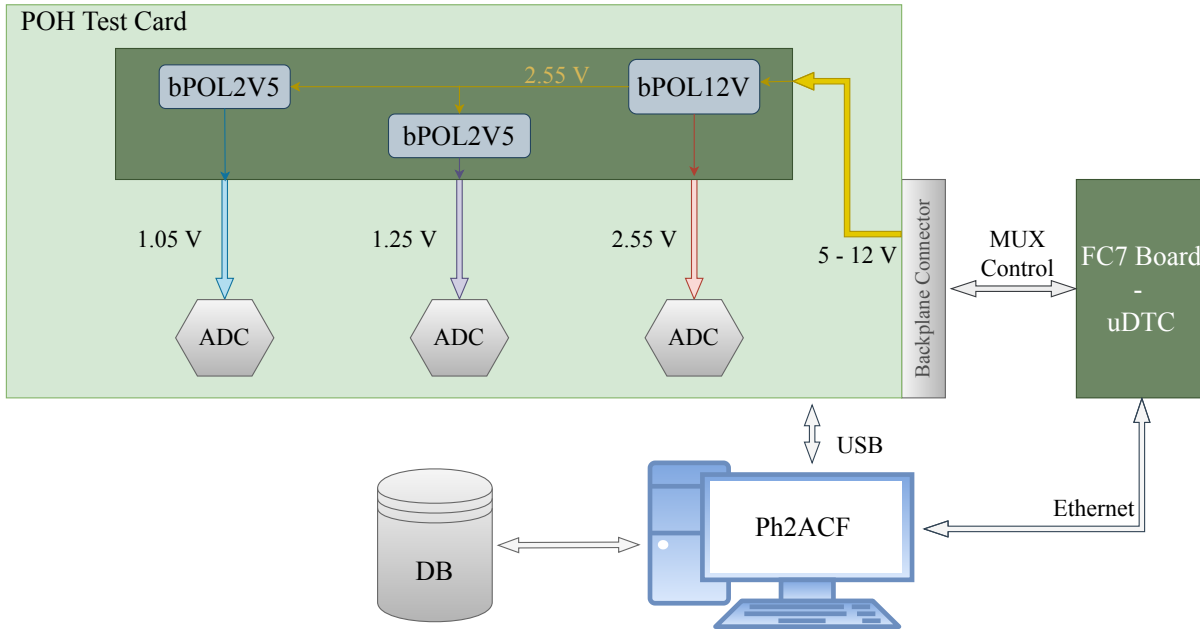


Figure 8.5: Block diagram of the PS Power Hybrid test. The validation of each hybrid circuit mainly focuses on the verification of the bPOL DCDC converters power distribution performance.

Table 8.3: Preliminary list of power hybrid functional tests indicating the category, the test and the result type. "PASS/FAIL" corresponding to binary success or failure result, while "STATUS CHECK" corresponds to a more elaborate report.

Test category	Test step	Result type
Power verification	Test cards voltages	PASS/FAIL
DC-DC characterization	Efficiency	STATUS CHECK
	Output ripple	STATUS CHECK

The output voltages of each power line are measured at minimum, medium and maximum load conditions. The minimum condition corresponds to the situation where no load is configured on the line while the maximum condition corresponds to a load of 80 mA for the 2.55 V line, 2.7 A for the 1.25 V line and 2.9 A for the 1.05 V line. It should be noted that since the 2.55 V line is also loaded by the two downstream bPOL2V5, its actual maximum load is achieved when both the 1.25 V and 1.05 V lines are at maximum load.

Efficiency: The output efficiency, denoted as $\eta = P_{\text{out}}/P_{\text{in}}$, is characteristic of the hybrid power transfer performance. It consists of measuring the ratio between the output power and the input power including each individual power line at low, medium and maximum load. The DC-DC conversion is considered to perform well if its corresponding efficiency is beyond 60%.

Output ripple: The bPOL DC-DC converters voltage control loops can be subject to strong oscillations and thus create ripples on the output voltage. They correspond to residual variations of the DC voltage and are therefore measured at each output voltage line under the different load conditions to ensure a stable DC output voltage. The quantitative criteria to define tolerances on the ripple characteristic of the output voltage are not yet defined, and the assessment for each POH is simply performed by comparing the output voltage curve to a reference curve.

8.2 Module Qualification

Following the validation of the various hybrid circuits, the latter, together with PS-sensors, MaPSAs and mechanical parts are distributed to module assembly centers and assembled into fully functional modules as described in Chapter 6. Each assembled module is then subjected to a series of qualification tests performed in the laboratory and using the single module test system described in Section 7.2. Figure 8.6 shows a block diagram of the test setup.

The module is placed inside the test box and connected to low and high voltage power supplies while the control and readout of the module is done via the FC7 board and the Ph2ACF software framework. While the list of qualification tests for the production phase is still being defined, a minimal set of functional tests was developed, mostly targeting the preliminary validation of prototype modules and covering power integrity verification, I-V characterization, module configuration and startup validation, threshold equalization and electronic noise measurements.

8.2.1 Power Integrity Measurement

Power integrity measurements refer to the testing and evaluation of the electrical performance of the module with respect to the power distribution. They help to assess the quality of the power supply to all the electronic components on the module, making sure that they all operate within specified voltage and current limits defined to provide reliable

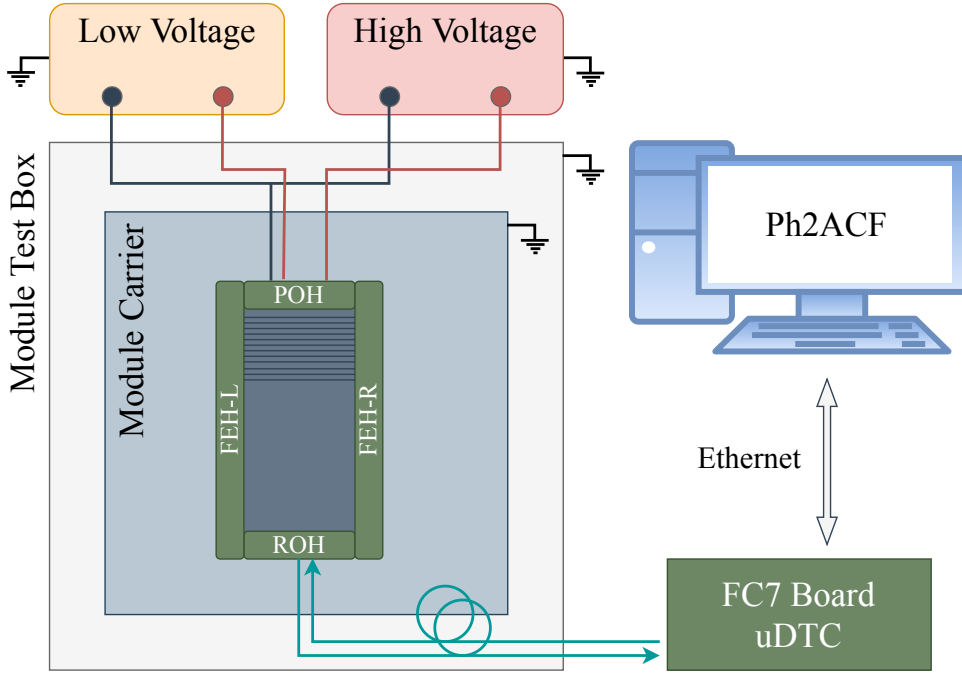


Figure 8.6: Block diagram of the PS module test setup. The module, mounted on its dedicated carrier plate, is placed inside the test box and connected to low and high voltage supplies. The control and data readout is performed using the FC7 board and the Ph2ACF software framework.

performance. They are performed manually using a multimeter and consist of probing a set of resistors and coupling capacitors on each hybrid circuit. These resistors and capacitors correspond to the various input power circuits that supply the lpGBT, VTRx+, CIC, SSA and MPA chips. Figure 8.7 shows all the power integrity measurement contact points on a PS module.

Each of the measurements consist of measuring the voltage between the points indicated by their corresponding arrows. They are performed at minimum and maximum power consumption, with and without the power tail connected. The minimum consumption corresponds to the module startup step, when low voltage is provided but the front-end chips are not yet configured. On the other hand, in theory, the maximum power consumption corresponds to the state where the front-end chips are fully configured and the module is at maximum activity. This is achieved when the module is at 50% of hit occupancy, which corresponds to the situation where half of the front-end channels, randomly distributed, are triggered at each readout clock cycle. This level is of particular interest as it corresponds to the level where the signal yields the strongest fluctuation. This level can be reached by positioning the front-end signal threshold close to the signal baseline

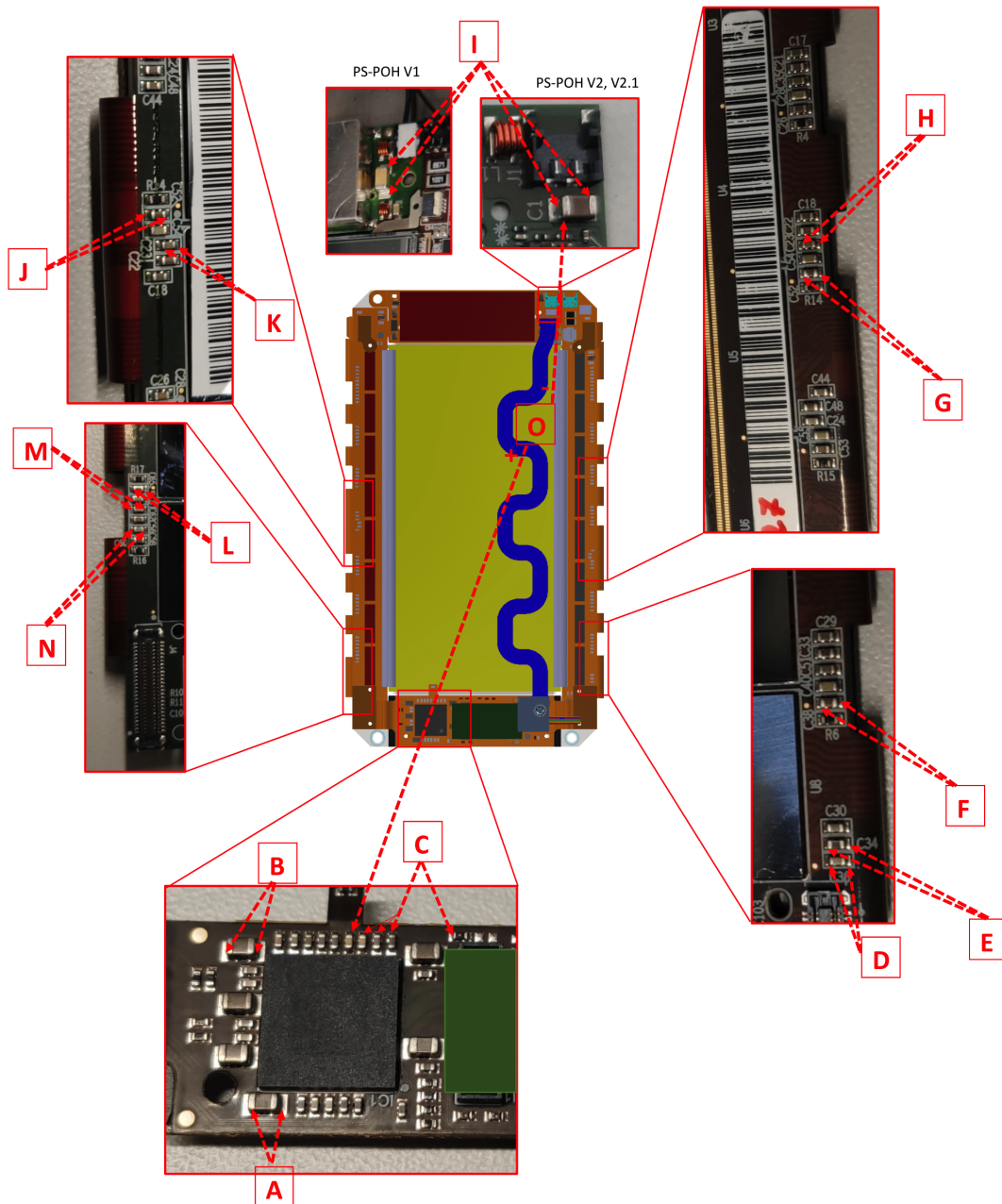


Figure 8.7: Mapping of all the power integrity measurement contact points on the PS module. Each zoomed image indicates the resistors and coupling capacitors to be manually probed with a multimeter. The measurements cover the 1.0 V, 1.25 V and 2.5 V voltage levels at various components on the FEH and ROH.

Table 8.4: Power integrity measurement results from a PS prototype module assembled at DESY. Each column corresponds to different measurement conditions combining minimum or maximum activity and connected or unconnected power tail (PT).

Measurement	Min Activity		Max Activity	
	PT	no PT	PT	no PT
Input Current [mA]	446	444	1020	1010
A: 1V25, ROH: C17 [V]	1.265	1.245	1.241	1.204
B: 1V25, ROH: C14 [V]	1.265	1.245	1.242	1.204
C: 2V5, ROH: R3, GND [V]	2.528	2.523	2.503	2.492
D: 1V25, FEHL: C36 [V]	1.265	1.252	1.237	1.213
E: 1V0, FEHL: C34 [V]	1.044	1.041	0.997	0.99
F: 1V25, FEHL: C38 [V]	1.255	1.253	1.240	1.237
G: 1V25, FEHL: C52 [V]	1.258	1.257	1.245	1.243
H: 1V25, FEHL: C23 [V]	1.268	1.261	1.246	1.230
I: 10V, POH: C1 [V]	9.89	9.87	9.97	9.96
J: 1V25, FEHR: C52 [V]	1.250	1.247	1.234	1.228
K: 1V25, FEHR: C23 [V]	1.262	1.256	1.226	1.215
L: 1V25, FEHR: C65 [V]	1.247	1.244	1.229	1.223
M: 1V25, FEHR: C65 [V]	1.261	1.251	1.227	1.208
N: 1V0, FEHR: C58 [V]	1.045	1.040	1.005	0.997

or amplitude, such that an occupancy of 50% is measured. Table 8.4 shows the results obtained from measurements performed on an early prototype module. The first column indicates the measurement, the reference voltage, the corresponding hybrid circuit and the component to be probed on the hybrid circuit. FEHR and FEHL correspond to the right and left front-end hybrid circuits on Figure 8.7, respectively. The four columns on the right correspond to different measurement conditions namely, minimum activity with power tail (Min Activity PT), minimum activity without power tail (Min Activity no PT), maximum activity with power tail (Max Activity PT) and maximum activity without power tail (Max Activity no PT).

In the measurements of the 1.05 V, 1.25 V and 2.55 V voltage levels (A-N) a slight decrease caused by the resistive losses on the path to the load can be observed when moving from the minimum activity to the maximum activity, both when the power tail is used and when it is not. However, these losses do not affect the operation of the module as the measurement points are well within the specified $\pm 8\%$ tolerance range around their nominal value. In addition, no substantial difference is observed when using the power tail, neither in the minimum activity case nor in the maximum one. It should be noted that since these power integrity measurements are delicate and timely ($> 1h$) to perform on a module, they are only invoked for the early prototype modules, and will be as well for the first production modules, in particular when dealing with functional issues.

8.2.2 I-V Characterization

The I-V characterization is the process of measuring the current (I) as a function of the bias voltage (V) applied to the silicon sensors. It allows the characterization of the silicon sensors electrical properties, in particular its leakage current and breakdown voltage. These electrical properties are of particular importance as they have a significant impact on the sensor performance and signal quality. Figure 8.8(a) shows the pre-assembly I-V measurements performed on the individual PS-p and PS-s sensors, and the post-assembly measurements performed on the corresponding assembled prototype module. In the pre-assembly stage, each of the individual PS-p and PS-s sensors is measured using a needle-based method and a dedicated probe station setup. In the post-assembly stage, a direct access to the individual sensors is no longer possible and the measurement directly relies on the current reading from the high voltage power supply and consists of an inclusive reading of the joint current of the two sensors.

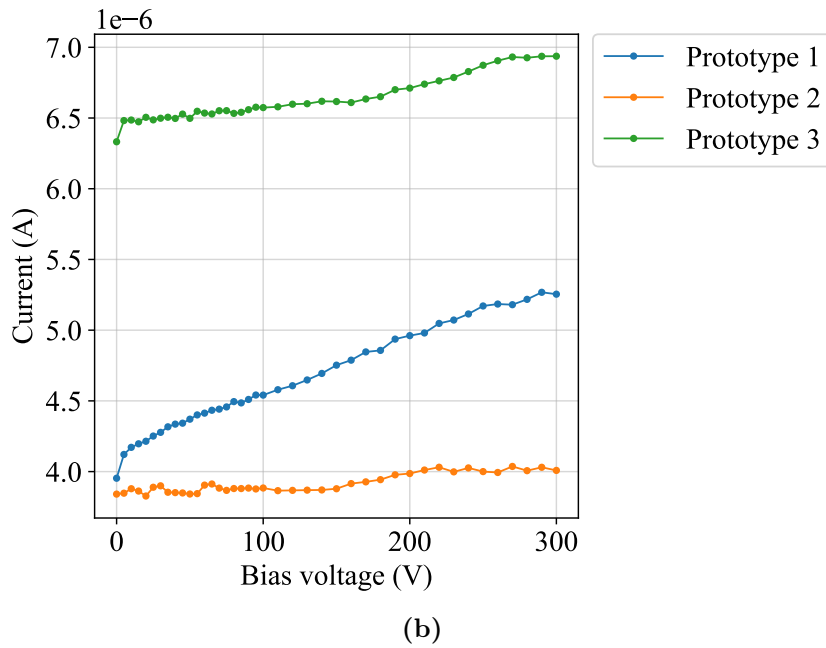
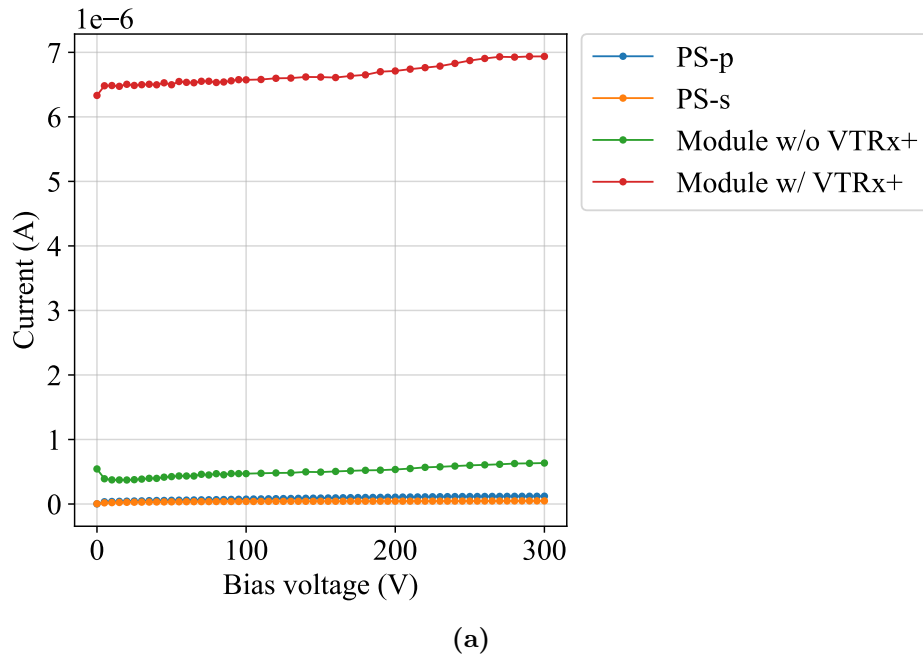


Figure 8.8: (a) I-V measurement results from the latest 4.0 mm PS prototype module showing the measurement of the individual sensors and the fully assembled module. The impact of the VTRx+ emitted light is also shown. (b) I-V measurement results of the last three 4.0 mm PS prototype modules assembled at DESY.

Figure 8.8(b) shows measurements performed on three prototype modules assembled at DESY. They are performed up to the nominal bias voltage of 300 V. The pre-assembly measurements of the individual PS-p and PS-s sensors yield a leakage current around 100 nA and 50 nA, respectively, and no sensor breakdown is observed. However, the post-assembly measurement where the VTRx+ is connected yields a leakage current higher than the one measured in the situation where the VTRx+ is disconnected by approximately 6 μ A. Further investigation showed that this drastic increase is related to the light emissions of the VTRx+ module which, as an optoelectronic transceiver, generates infrared light at a wavelength of 850 nm when biased. However, the transparent plastic cover used in the design of the VTRx+ is not enough to shield the emitted light which ends up leaking mostly towards the PS-s sensor. As this light can act as a noise source for the sensor, a shielding cover for the VTRx+ will be incorporated to the final PS module design. Finally, the results obtained across the assembled prototype modules yield values below the maximum expected 10 μ A at full depletion voltage, with variations mainly due to differences of the environmental conditions during the measurement. During production, these environmental conditions will be more strictly monitored and controlled to ensure consistency throughout the production timeline.

8.2.3 Start-Up Sequence

The module startup sequence refers to the set of control and configuration procedures performed on the front-end chips and the back-end FC7 board to bring the system into an operation readiness state. The steps can be divided into three categories: optical link establishment, front-end data alignment and back-end data alignment. The optical link establishment consists in achieving a stable optical communication with the lpGBT chip. The front-end and back-end data alignments address the preparation of the full data transmission chain from the front-end chips to the back-end FC7 board, ensuring that the transmitted signals are correctly sampled and the corresponding data packets correctly retrieved. Each step is described below.

Optical link lock: To ensure that a reliable optical data communication is achieved between the lpGBT chip and the FC7 back-end board, so-called *link lock* must be achieved such that at both ends the received data stream is properly decoded. In practice, the serialized data frame transmitted by the lpGBT (uplink) and by the FC7 board (downlink) are received and fed to a frame aligner block. A *frame-lock* acquisition sequence is then launched in order to find the frame boundaries and acquire frame synchronization. In practice, the frame lock acquisition operates as follows: for each received frame, the

frame header validity is checked using the four bits in the header position. If a defined number of consecutive frames contains valid headers, the link is considered *locked*. Otherwise, the frame is shifted by one bit and the header search procedure is repeated until the valid header is found. The optical link is therefore said to be *locked* if both the lpGBT and the FC7 board achieve a downlink and uplink link lock, respectively.

CIC-lpGBT data alignment: This test addresses the adjustment of the phases of the data signals between the CIC outputs and the lpGBT inputs to ensure that data is synchronized and thus correctly sampled. To achieve this, the lpGBT provides a phase-aligner circuit for each of the input ePortRx to guarantee that the data received is sampled by the lpGBT internal clock in the middle of the eye-diagram. First, the CIC is configured to output data according to a fixed data pattern, instead of the data frame described in Section 5.2.2, where transitions between zeros and ones are well balanced (ie 11101010). This is referred to as a DC-balanced pattern. The lpGBT phase-aligner is then configured to operate in so-called *Initial Training* mode where the sampling phase is scanned to determine the best phase to be configured. The ePortRx channel is asserted to be *locked*, or properly aligned, if a pre-defined number of 64 correct bit transitions is detected.

Back-end data alignment: Besides the front-end alignment, the L1 and Stub data encoded in the CIC data frames described in Section 5.2.2 and transmitted to the back-end FC7 board need to be properly received and decoded. Therefore data alignment in the back-end is needed. This is achieved using a so-called *word alignment* procedure that allows the proper synchronization of pre-defined data words (packets) within the transmitted L1 and stub CIC data frames. The data frame boundaries can therefore be determined with respect to the pre-defined words, and the subsequent data correctly retrieved. In practice, the CIC is configured to output data according to a fixed data pattern, or so-called *synchronization pattern*, on each of its L1 and stub data lines. The data frames received by the FC7 board are then subjected to iterative bit shifts, searching for the corresponding synchronization pattern. The L1 or stub line is therefore said to be aligned or tuned if the correct synchronization pattern is found.

MPA-CIC data alignment: Finally, to synchronize the signals of the six data lines between each MPA and the CIC inputs and ensure a correct decoding of the corresponding data, phase and word alignments at the CIC are needed. The CIC phase alignment block uses a simplified version of the lpGBT phase-aligner, and operates following the same procedure. Each MPA is configured to output data according to a fixed DC-balanced

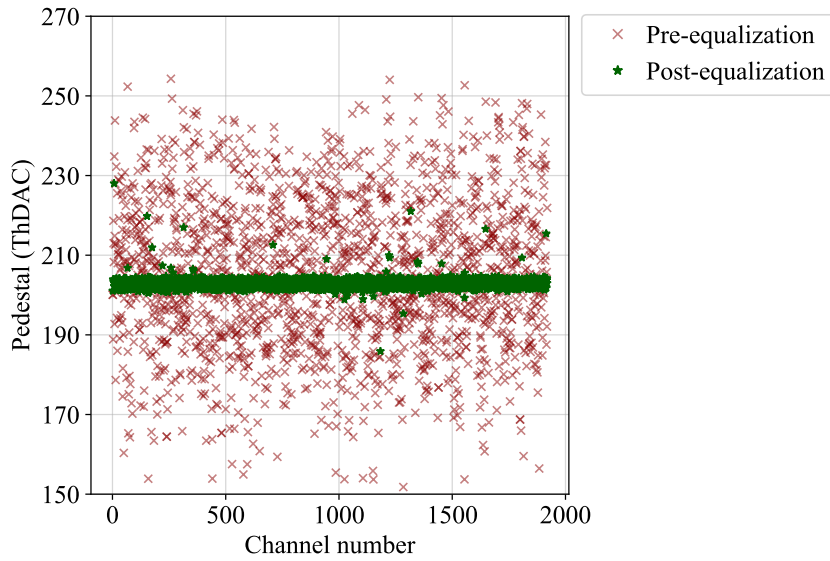
data pattern and the phase-aligner of each CIC input line performs a search of the best data sampling phase. The channel is then reported to be *locked* when the best sampling phase is found. On the other hand, the CIC word alignment block is dedicated to the synchronization of the MPA 16 bits stub data described in Section 5.2.1, first with the 40 MHz sampling clock then with the 20 MHz one. The objective is to locate the synchronization bits in each of the 16 bit data blocks in order to determine the word boundaries and correctly retrieve the stub data. In practice, the MPA chips are configured to output data according to a pre-defined fixed data pattern on each of the five stub data lines fed to the CIC. The CIC then performs iterative bit shifts, searching for the corresponding synchronization bit included in the data words. Each stub line is said to be aligned if the synchronization pattern is found and properly aligned to each of the 40 MHz and 20 MHz sampling clocks.

8.2.4 Threshold Equalization

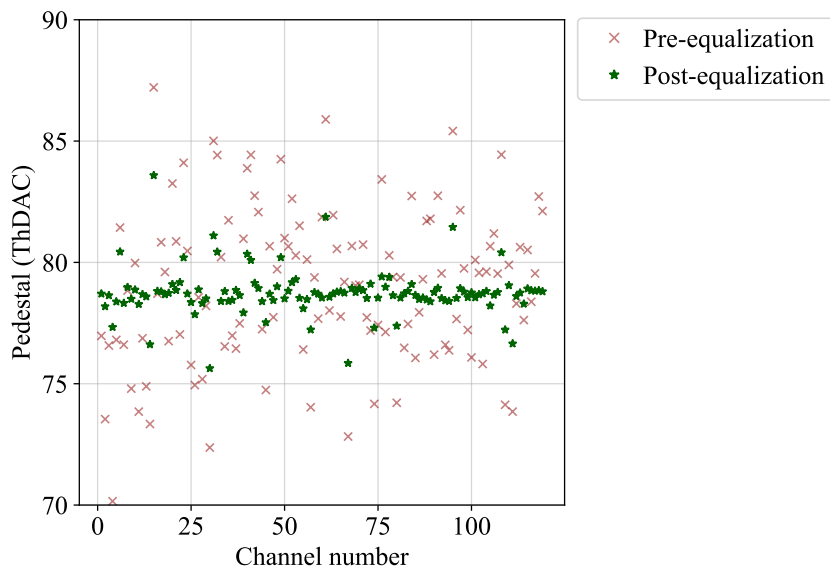
The threshold equalization is a calibration procedure that aims to adjust the signal threshold with respect to the signal baseline of the analogue front-end readout channels. In particular, it ensures that for every individual channel, the distance between the signal baseline, also referred to as *pedestal*, and the signal threshold is equalized. It is of particular importance for two main reasons. On the one hand, the pedestal values can vary between the front-end readout channels due to process variations. On the other hand, in each of the MPA and SSA chips, the signal threshold value is shared among all the front-end channels. Therefore, the equalization ensures that during operation the relative position of the signal threshold with respect to the signal baseline for each front-end channel is equal across the front-end chip, guaranteeing a homogenous signal detection.

The threshold equalization of the MPA and SSA chips is achieved by fine tuning the so-called *trimming* voltage used to locally shift the position of the signal threshold. In each front-end chip, the signal threshold is configured via an 8 bit DAC (ThDAC), while the equalization is controlled via a per-pixel and per-strip 5 bit DAC (TrimDAC) to compensate for the discriminators offset spread. In practice, the threshold equalization procedure can be performed either with signal injection or without. In the case of the MPA and SSA chips, it is performed with signal injection and uses the MPA and SSA asynchronous readout feature.

The procedure can be divided in two steps: First, a target signal threshold relative to which all front-end channels are equalized is defined and configured at the level of the pulse



(a)



(b)

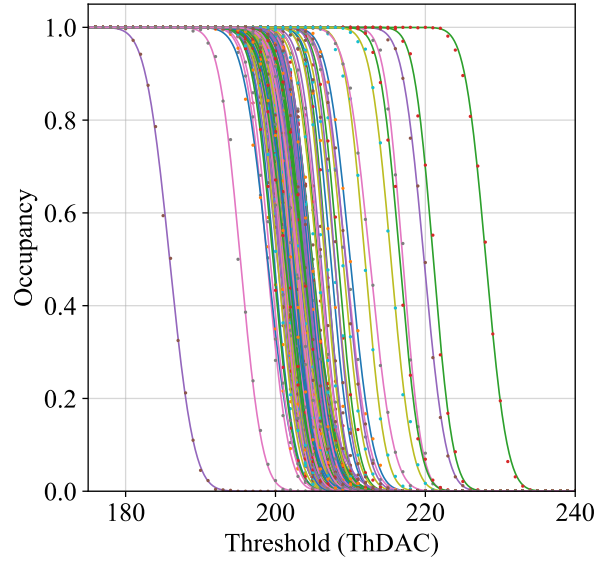
Figure 8.9: Threshold equalization results for a single MPA (a) and SSA (b) chip showing the pre-equalization and post-equalization pedestals for each front-end channel. The y-axis corresponds to the pedestal in digital units (ThDAC) and the x-axis corresponds to the channel number. The difference in the y scale is caused by differences in the analogue circuits between the MPA and SSA chips that yield different analogue to digital conversion factors for the ThDAC setting.

amplitude where the hit occupancy is approximately 50%. This approach is particular in the sense that the definition of the pedestal is modified from being the signal baseline to being the signal amplitude and thus the signal threshold tuned with respect to the latter. Second, the trimming voltage of each individual front-end channel is adjusted such that the signal threshold is shifted with respect to the pedestal until all channels yield the same 50% hit occupancy in response to the same injected charge. Figure 8.9 shows a distribution of pedestals for MPA and SSA chips before and after the threshold equalization procedure performed with a pulse amplitude of 77 CalDAC units where a single unit corresponds to 220 e^- for MPAs and 243 e^- for SSAs. Therefore a 77 CalDAC amplitude corresponds to approximately 1 MIP for both MPAs and SSAs. It should be noted that a certain number of front-end channels can fail the equalization procedure. This is mainly due to the fact that for those front-end channels the offset needed to equalize their corresponding signal threshold exceeds the maximum offset that can be configured on the trimming configuration register. However, the "trimmability" of a channel strongly depends on the target signal threshold and the amplitude of the injected signal. Currently, broader studies not covered by this thesis are ongoing in order to optimize the procedure with the objective of finding the optimal target signal threshold and injected signal amplitude to minimize the number of untrimmable pixels and strips. In addition, the current implementation of the procedure still requires a considerable amount of time ($\approx 15\text{ min}$) to be performed, in particular for the MPAs. This is mainly due to the fact that the MPA and SSA asynchronous counters are read out via the I²C interface instead of the fast readout interface. Work targeting migration to the faster readout interface is ongoing.

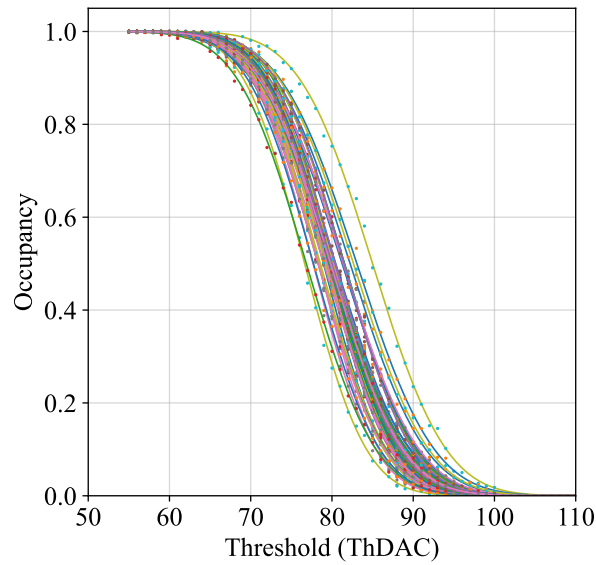
8.2.5 Noise Measurement

Noise measurement follows the threshold equalization and refers to the measurement of electrical fluctuations in the output of the detected signal. The fluctuations can arise from various sources as described in Section 3.2.1. Therefore the noise is a key measure of the quality and performance of each individual front-end channel and is used to optimize the design and operation of the module. In particular, determining the noise level is crucial for the choice of an optimal signal threshold that maximizes the cluster detection efficiency, as described in Section 9.3.1, during module operation.

In the case of binary readout chips, such as the MPA and SSA chips, noise is measured by performing a so-called *S-Curve measurement*. The latter consists of scanning the signal threshold for each readout channel while measuring the corresponding hit occupancy.



(a)



(b)

Figure 8.10: S-Curve measurements for all channels of single MPA (a) and SSA (b) chips. The outliers correspond to readout channels where the threshold equalization procedure failed.

Similarly to the threshold equalization, the procedure can either be performed with signal injection or without. In the case of the MPA and SSA chips, it is performed with signal injection. At very high thresholds, no signal pulse is detected and the hit occupancy for each front-end channel is at zero. By decreasing the signal threshold towards the range of the signal pulse the hit occupancy rises to 100% leading to the so-called *S-Curve*. The latter allows to capture in its slope the signal fluctuations at the pedestal and thus provide the means to infer the corresponding electronic noise. Figure 8.10 shows superimposed S-Curves from all the MPA (a) and SSA (b) front-end channels on a single chip.

Assuming a Gaussian distributed noise, the S-Curve can be fitted using an error function

$$f(x) = \frac{1}{2} \operatorname{erf} \left(\frac{x - \mu}{\sqrt{2}\sigma} \right) \quad (8.1)$$

where μ corresponds to the pedestal position and the width σ corresponds to the front-end channel noise.

In practice, the noise measurement is performed at multiple steps of the assembly: before the module assembly (pre-assembly) independently on the MaPSA and on the so-called *hybrid skeleton* which corresponds to connected hybrid circuits without any attached sensors, before the wirebonds encapsulation (pre-encapsulation) and after the wirebonds encapsulation (post-encapsulation). This allows the monitoring of the electrical properties of the module and the detection of potential damage. Figure 8.11 shows the noise performance at each of the aforementioned steps for a 4.0 mm PS prototype module equipped with the latest available versions of MPA and SSA chips at the time, namely MPA2.0 and SSA2.0, respectively. The noise is expressed in ThDAC digital units and a single unit corresponds to 94 e^- for MPA and 250 e^- for SSA. The measurement yields a consistent MPA noise level of 2.5 ThDAC or 225 e^- across the different assembly steps. On the other hand, the increase in the SSA noise level between the pre-assembly skeleton test and the post assembly module test is due to the addition of the PS-s sensor and thus extra capacitance at the input of the front-end channels. In the post-assembly steps, the SSA noise level, around 6.5 ThDAC or 1625 e^- is much higher than the maximum 800 e^- noise level allowed. The same observation was made on the other prototype modules assembled at DESY and other institutes. However no definite noise requirement is defined yet as it strongly relies on performance studies of irradiated modules. Figure 8.12 shows the noise measurement results from all the PS prototype modules assembled at DESY. The MPA noise levels appear to be consistent across the modules, however inconsistent variations

are observed in the SSA noise.

While environmental conditions can be considered as a potential cause for the inconsistencies, the previously mentioned high SSA noise indicates a more systematic problem. Investigations on the matter were conducted by the hybrid circuit designers and showed potential design weaknesses that can lead to such higher noise levels [81]. Two potential sources of noise are considered: First, the DC-DC converters switching currents at frequencies of 2.5 MHz and 4 MHz can generate a common mode (CM) voltage difference on the ground paths of the left and right sides of the module, as well as between the HV circuit ground and the front-end analogue circuits. This leads to currents flowing through the sensors, thus contributing with additional noise at the front-end analogue circuits. Second, a low impedance loop exists between the PS-p and PS-s sensors and the front-end chips. The latter can be sensitive to the time-varying magnetic field escaping through the printed circuit board of the PS POH and can result in a very small electromotive force capable of generating large noise currents which flow into the front-end analogue circuits. However, this only forms a vulnerability as the loop is less exposed to the magnetic fields generated on the module. Therefore, with regards to the aforementioned findings, the next version of hybrid circuits will come with adequate design changes to the HV and GND paths to mitigate these potential noise sources. However, improvements to the hybrid circuits design were introduced in order to meet the target noise performance. The latter is defined such that the hit detection efficiency can be maintained above 99% after irradiation at a level of $1 \times 10^{15} \text{ n}_{\text{eq}}\text{cm}^{-2}$ after 4000 fb^{-1} . The expected seed signal after the aforementioned radiation dose is expected to be around $9000 \text{ e}^- \text{ MPV}$. To maintain the hit efficiency with such a signal seed, the signal threshold should be about $1/3$ of the MPV, thus 3000 e^- . Therefore, in the case a foreseen $4\text{-}5 \times \sigma$ signal threshold, the noise level must be maximum around 800 e^- . However, even if this target noise performance is not met yet, the first prototype modules assembled and tested in laboratory remain usable for further qualification of the modules functionalities. In particular in test-beam campaigns as discussed in the next chapter.

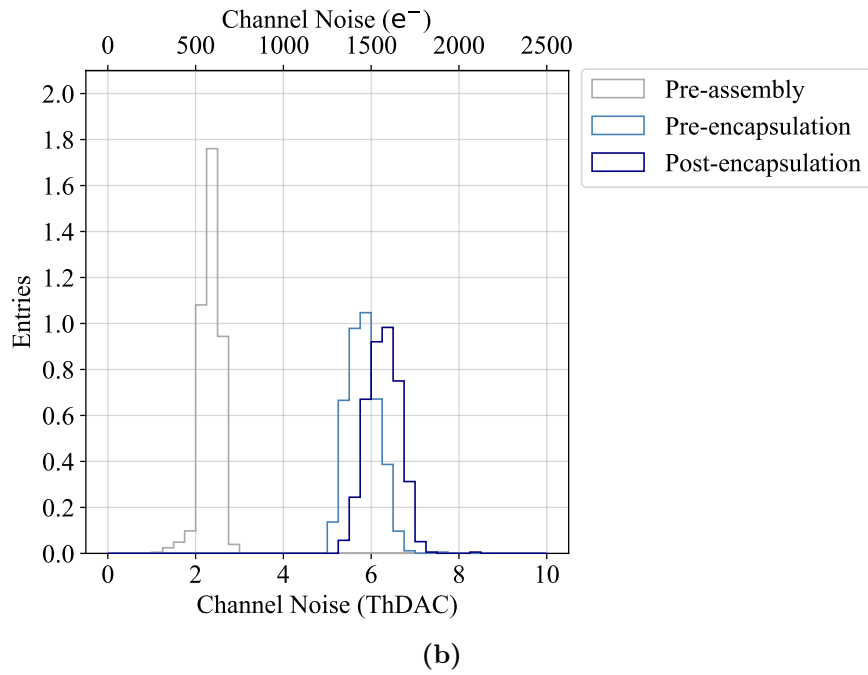
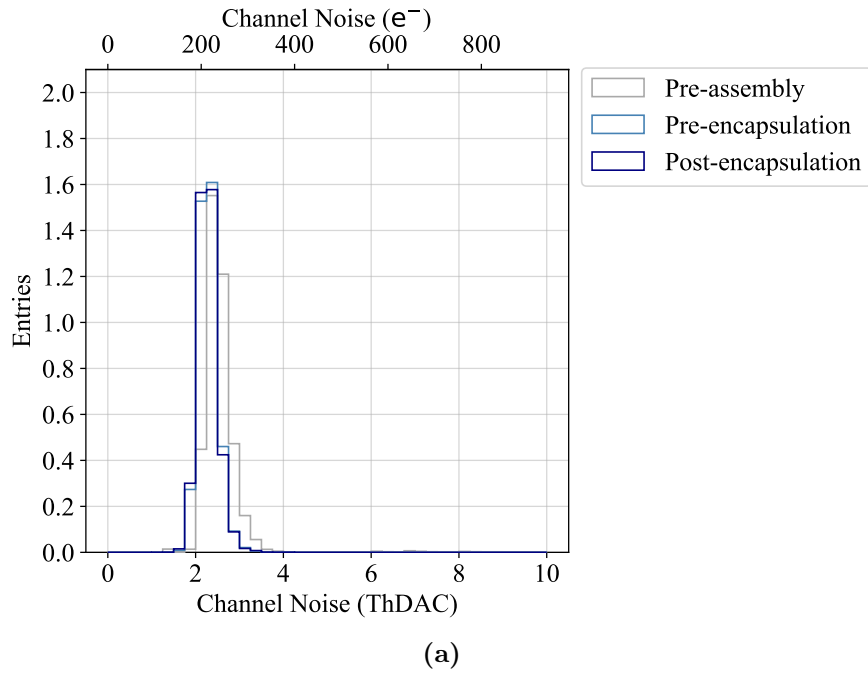
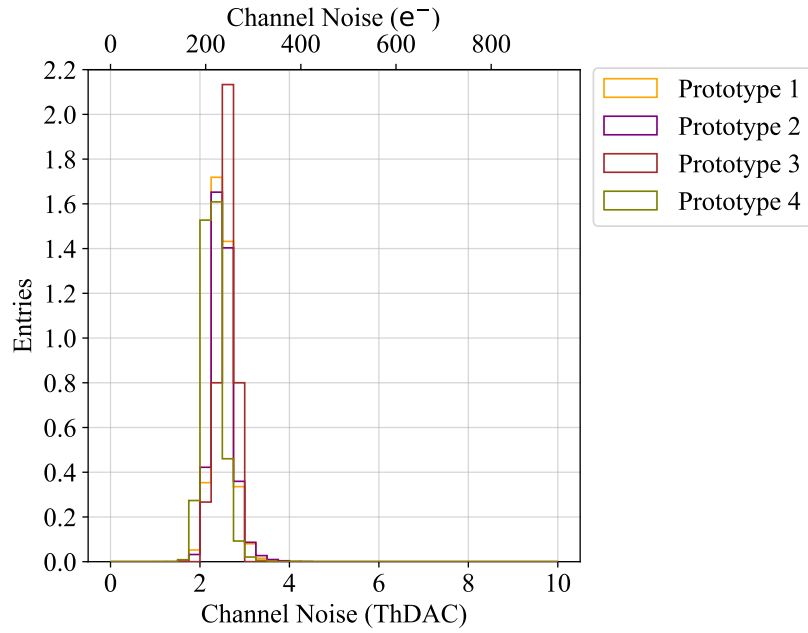
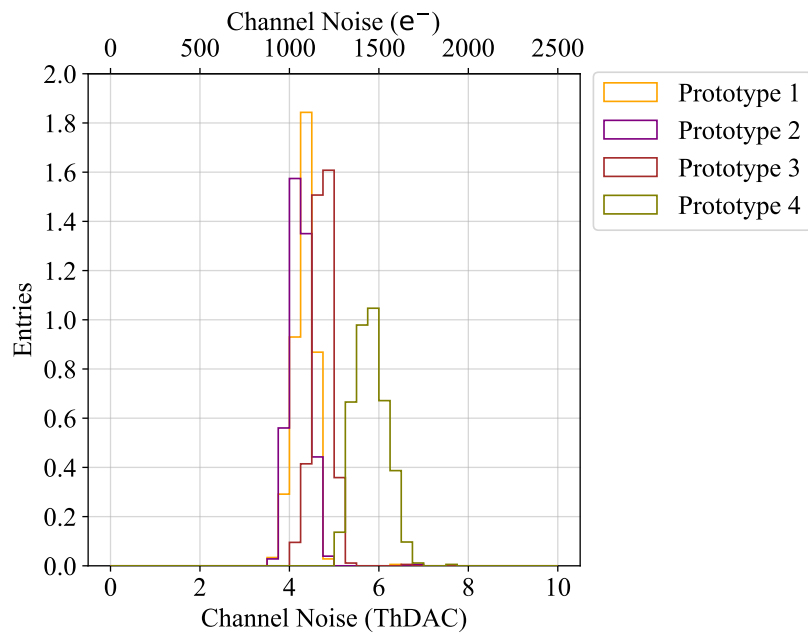


Figure 8.11: Noise measurement of a 4.0 mm PS prototype module at each stage of the assembly, namely: pre-assembly (skeleton, MaPSA), pre-encapsulation, and post-encapsulation. (a) shows the MPA noise while (b) corresponds to the SSA noise. The x-axis corresponds to the noise in ThDAC unit and the upper scale indicates the equivalent charge in e^- .



(a)



(b)

Figure 8.12: Noise measurement of PS prototype modules assembled at DESY. The x-axis corresponds to the noise in ThDAC unit and the upper scale indicates the equivalent charge in e^- .

CHAPTER 9

PIXEL-STRIP MODULE TEST-BEAM QUALIFICATION

As part of the qualification chain, validating the PS module design under beam exposure is of central importance. As a complement of the laboratory qualification described in the previous chapter, it is a great opportunity to further validate the operational aspects of the module as well as the corresponding functional performances. For this purpose, several test-beam facilities offering different testing environments are accessible to the community. In practice, the module is integrated to the corresponding test infrastructure and is exposed to a particle beam defined by certain characteristics and parameters that differ between the facilities. In addition, the facilities usually provide a so-called *beam telescope* to reconstruct particle tracks used to assess the detection efficiency of the device under test (DUT). Finally, a data acquisition system to which the user systems need to be integrated is often included and allows for a common control and operation of the test-beam setup.

The measurements presented in this chapter have been performed at the DESY-II Test-Beam Facility [82]. In the case of the PS module, the objective of these test-beam campaigns is to validate the full readout chain and study the module performance, in particular the particle detection efficiency, spatial resolution, and the p_T discrimination performance. This chapter provides a detailed description of the DESY-II Test-Beam facility and setup in the context of PS module test-beam campaigns, and presents the corresponding performance studies conducted in the scope of this thesis.

9.1 Test-Beam Infrastructure & Setup

DESY (Deutsches Elektronen-Synchrotron) operates a test-beam facility that offers three independent beam lines with electron or positron particles with selectable momenta from 1-6 GeV/c. The beam lines are served by the DESY-II synchrotron [83], which typically provides electron beams with an oscillating energy from 0.45 – 6.3 GeV and operates as an injector to the PETRA-III synchrotron light source [84]. In addition, each of the beam lines provides, in the experimental area, a so-called *beam telescope* that can be used during the offline data analysis to reconstruct particle tracks created by the beam to which the device under test is exposed. These tracks can further be used to study the performance of the device under test.

9.1.1 Beam Generation

The test beams are generated from the primary DESY-II beam via two fold conversion as shown in Figure 9.1. A carbon fiber target is placed on the primary beam orbit and used to generate Bremsstrahlung photons. These photons are subsequently converted into electron-positron pairs in a Cu or Al secondary target. Downstream of the generated electron-positron pairs, a spectrometer dipole magnet allows the selection of either electrons or positrons, and enables to only select particles within a certain momentum range. Finally, a primary collimator made of tungsten jaws complemented by a secondary collimator made of lead further limit the momentum acceptance and the size of the beam that is provided to the test-beam experimental area.

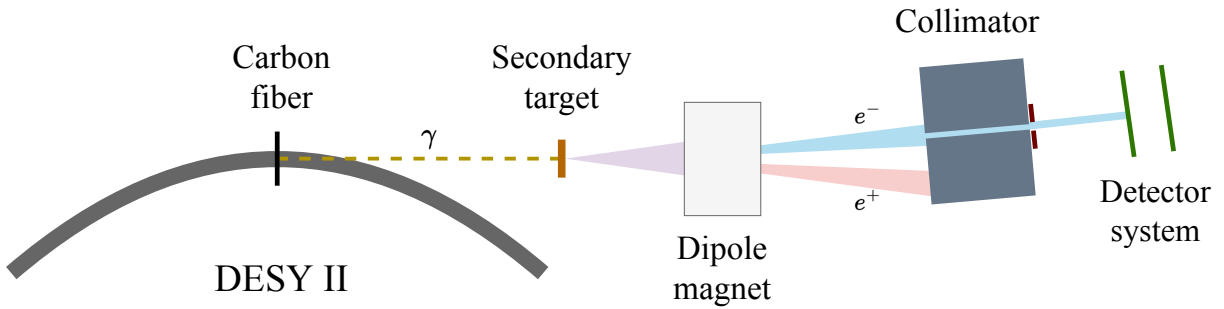


Figure 9.1: Schematic diagram of the test-beam generation at the DESY-II synchrotron. Bremsstrahlung is emitted from the beam in the DESY II synchrotron when hitting a fiber target and is converted into electron-positron pairs at a secondary target. Finally, a dipole magnet allows for a selection of the beam momentum within the available spectrum of up to 6 GeV/c.

9.1.2 Beam Telescopes

The DESY-II Test-Beam facility is equipped with EUDET-type beam telescopes [85] which allow for offline reconstruction of beam particle tracks. Each beam telescope is composed of two telescope arms each made of three planes. This configuration allows the integration of a device under test such that it is covered by three planes on the upstream and three on the downstream sides. Each plane consists of a MIMOSA26 (M26) monolithic active silicon pixel sensor [86]. The sensor is $50\text{ }\mu\text{m}$ thick and provides a pixel matrix of 1152 columns and 576 rows with a pixel pitch of $18.4 \times 18.4\text{ }\mu\text{m}^2$. This results in an active area of $21.2 \times 10.6\text{ mm}^2$. The pixel readout is based on a rolling shutter and line-by-line buffering, while the digitization provides binary pixel information that is zero-suppressed prior to streaming, resulting in an integration time of $115.2\text{ }\mu\text{s}$ per frame. Each MIMOSA sensor is covered by a $25\text{ }\mu\text{m}$ thick Kapton foil on each side, keeping the material budget as low as possible to achieve a high track resolution. The intrinsic resolution of a sensor was measured to be $3.24 \pm 0.09\text{ }\mu\text{m}$ [85]. Figure 9.2 shows a sketch of a EUDET-type beam telescope with an integrated DUT.

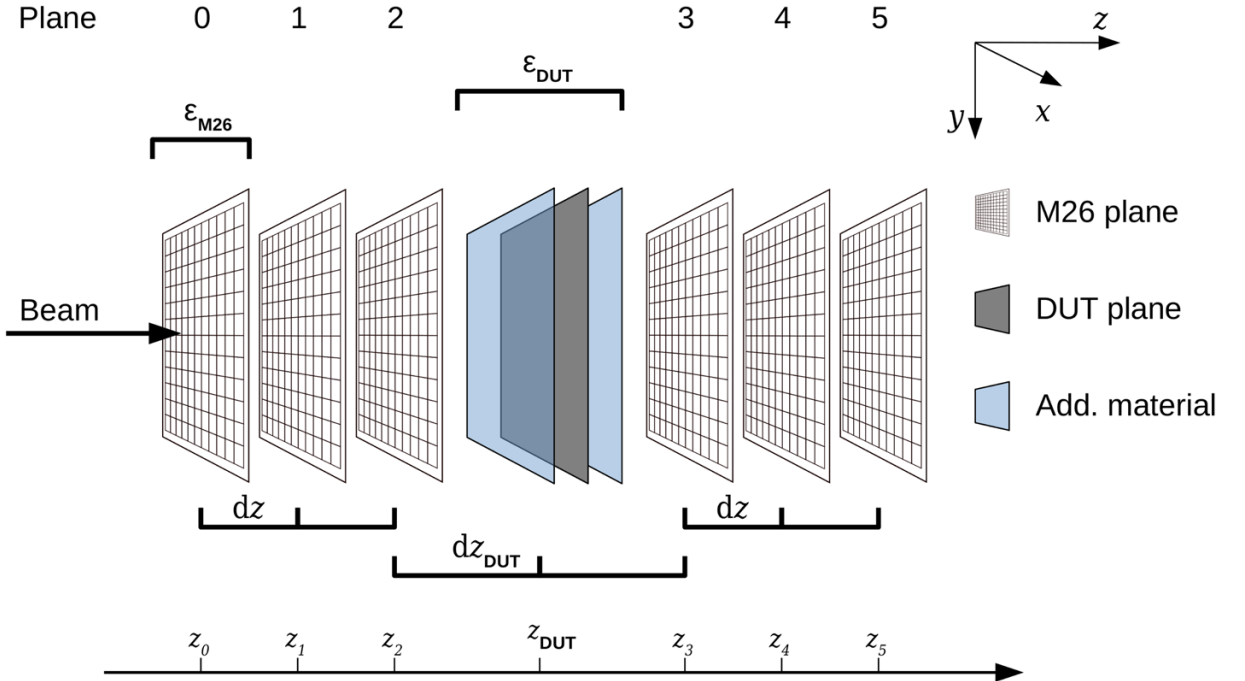


Figure 9.2: Sketch of the EUDET-type beam telescope configuration, its important parameters, and an integrated device under test (DUT). The MIMOSA26 (M26) planes 0 to 2 and planes 3 to 5 are referred to as upstream and downstream planes, respectively. The DUT plane corresponds to the sensing layer of the device while the additional material corresponds to any type of material surrounding the device [85].

9.1.3 Timing Reference Plane

Due to the long integration time ($115.2\ \mu\text{s}$) of the MIMOSA26, the number of reconstructed telescope tracks can be higher than one per event as shown in Figure 9.3. However, as explained in Section 9.1.6, only a single track triggers the readout of the DUT, and the latter, usually with $O(\text{ns})$ integration time, only records clusters from the triggering track. Therefore, in order to measure quantities such as the cluster efficiency (see Section 9.3.4), the telescope can be complemented by an additional timing layer with $O(\text{ns})$ integration time. The timing layer is used in the offline analysis in order to only select the tracks that triggered the readout, thus matching them to the corresponding clusters in the DUT.

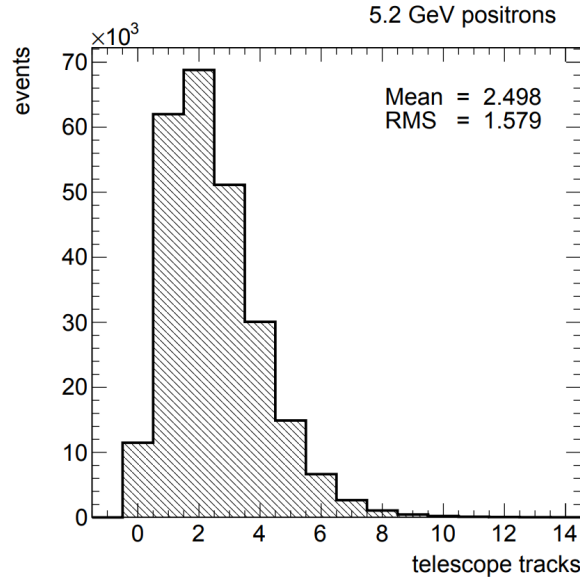


Figure 9.3: Track multiplicity in the Datura beam telescope within a single read-out frame of the MIMOSA26 sensors at a particle energy of 5.2 GeV[87].

For the results presented in the following sections, a CMS Phase-1 BPIX module, described in detail in [88], was used as a timing reference plane. It consists of a planar silicon sensor with a size of $18.6 \times 66.6\ \text{mm}^2$ (active area of $16.2 \times 64.8\ \text{mm}^2$), bump-bonded to an array of 2×8 PSI46dig readout chips [89]. Each readout chip is segmented into 4160 readout channels, and the pixel size is $100 \times 150\ \mu\text{m}^2$. The readout chips are read out via a high-density interconnect (HDI) flex circuit to which they are glued and wirebonded. Finally the module is further connected to a Digital Test Board (DTB), a compact FPGA-based data acquisition system that connects via USB to the control computer.

9.1.4 Trigger Logic Unit

The trigger logic deployed during beam tests is based on the AIDA Trigger Logic Unit (TLU) [90]. It is a flexible and easily configurable unit that provides trigger and control signals to devices used in test-beams and integrated in a beam telescope. It can operate with a sustained particle rate of 1 MHz and with instantaneous rates up to 20 MHz. In addition, it provides a timing resolution of 1.5 ns. Figure 9.4 shows a sketch of the front panel of an AIDA TLU.

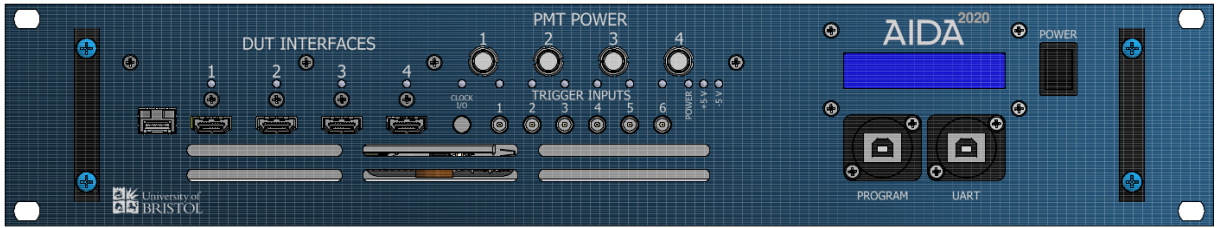


Figure 9.4: Sketch of the front view of an AIDA TLU [90]. Four HDMI and LEMO ports serve as an interface to the devices under tests and to the trigger scintillators, respectively.

Each device under test of the test-beam setup can be connected to the TLU via High-Definition Multimedia Interface (HDMI) ports. These ports are used to distribute the trigger, synchronization and system clock signals. In addition, the unit provides input ports for asynchronous trigger signals from external sources, such as beam scintillators. In the case of the DESY test-beam facility, two crossed scintillators coupled to silicon photomultipliers are positioned on the upstream and downstream parts of the telescope. They are used to generate a local trigger signal upon traversal of a particle. These signals can then be used by the TLU in any logical combination to generate and distribute a global trigger signal to the devices.

To synchronize all the devices under test, the TLU implements a special feature, so-called *handshake*, that allows each device to send signals back to the unit to indicate that they are busy. This allows to stop issuing any further trigger signals until all the devices de-assert the busy state. The TLU implements various handshake protocols depending on the type of device connected and the selected mode of operation. In the case of the PS module operation, the EUDET mode, also referred to as *trigger handshake mode* is used. Figure 9.5 shows a diagram describing how the handshake takes place.

The TLU asserts the TRIGGER line upon generation of a valid trigger signal. The device then asserts the BUSY line upon reception of the TRIGGER signal. The TRIGGER signal

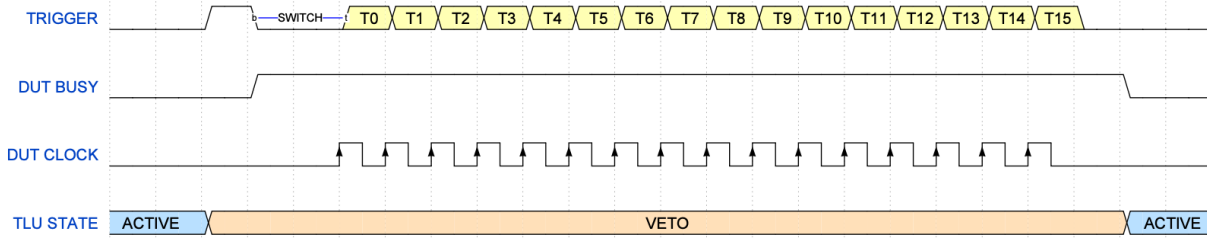


Figure 9.5: Signal diagram of the EUDET handshake mode. The TLU stops issuing any further trigger until the handshake protocol is terminated [90].

is de-asserted by the TLU as soon as it acknowledges the device to be busy, and the signal is switched to an output shift register containing the trigger number. No further trigger signal is issued to any device as long as the BUSY line of one of them is active. The device should then issue 16 clock pulses in order to retrieve the 15 bits of the trigger number. Finally, the device de-asserts the BUSY line when the trigger number is collected and the device is ready to accept a new trigger signal. This process takes place for the collection of every single event during data taking, and ensures that all devices are synchronized and their corresponding events are matched to the same trigger signal.

9.1.5 EUDAQ2 Software

The control of the integrated devices and the data collection during test-beams is performed using the EUDAQ2 software [91]. It is a framework written in C++ that features a modular and cross-platform architecture that serves as data acquisition software for the EUDET-type beam telescopes while providing a unified interface suitable for the integration of many different detector types, for example the PS module. Figure 9.6 shows a schematic overview of the EUDAQ2 software and the corresponding information flow.

A typical EUDAQ2 setup consists of several run-time instances with different roles communicating via Ethernet network, namely: a *Run Control*, multiple *Producers*, a single or multiple *Data Collectors*, a *Log Collector* and a *Monitor*.

Run Control: The central component of the EUDAQ2 system is the *Run Control* to which all the other modules connect. It provides all the necessary control of each of the various modules and connected devices, in particular the configuration, launch and termination of data collection during operation. It is provided as a Graphical User Interface (GUI) and is the main interaction point for the user with the framework.

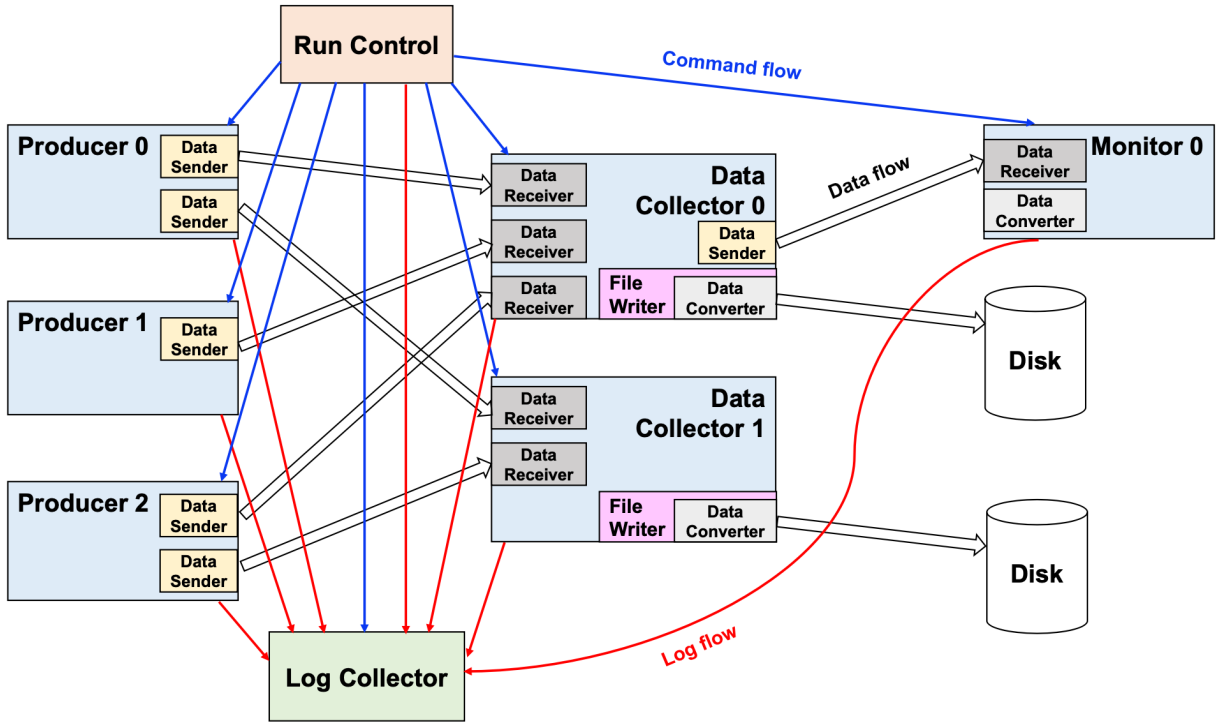


Figure 9.6: Schematic view of the EUDAQ2 architecture [91].

Log Collector: The *Log Collector* centralizes all the logging information received from the multiple devices and framework processes. It receives information from every individual device, displays them in one unified window and stores them in a dedicated file along with the recorded data files for later reference.

Producers: The control and readout of each individual detector is achieved via so-called *Producers*. These correspond to user-implemented classes written in C++ or python that are integrated to the EUDAQ2 architecture. In practice, the Producers need to implement a defined set of commands which are invoked upon start or configuration from the Run Control. For example, in the scope of this thesis, a Producer dedicated to the control and readout of a PS module was implemented for the need of the corresponding test-beam campaigns. It provides all the necessary functions to configure and read out the module, extract the L1 and stub data, and store them in a EUDAQ2-compatible format.

Data Collector: Data collected from each of the included detectors are gathered and merged all together by one or several *Data Collector* nodes. The merging process is performed online during data acquisition and ensures that data from the various detectors are attributed to the same trigger. No processing or conversion is performed prior to

storage. The raw detector data as delivered by the individual producers are stored in a dedicated EUDAQ2 raw event and can be converted to another format either online or offline, thus providing extensive offline processing freedom.

Monitor: To ensure data quality during data acquisition, the online *Monitor* is available. It connects to the Data Collector and accesses a fraction of the stored data, fully decodes it and builds control plots such as hit maps or correlation plots as shown in Section 9.1.6. This way, the user can ensure during data taking that all the devices are synchronized, well within the geometrical trigger acceptance, and functioning properly.

9.1.6 Integration & Data Acquisition

Starting from the individual components described earlier, the PS module test-beam setup is made of a EUDET-type beam telescope, complemented by two sets of crossed scintillators used for the trigger system and placed both upstream and downstream of the telescope. The whole structure is mounted on a large translation stage used to align the system with respect to the particle beam. The CMS Phase-1 BPIX module is included as a timing reference plane and placed in the downstream part right before the last telescope plane. Finally, the PS module is placed in the center of the beam telescope.

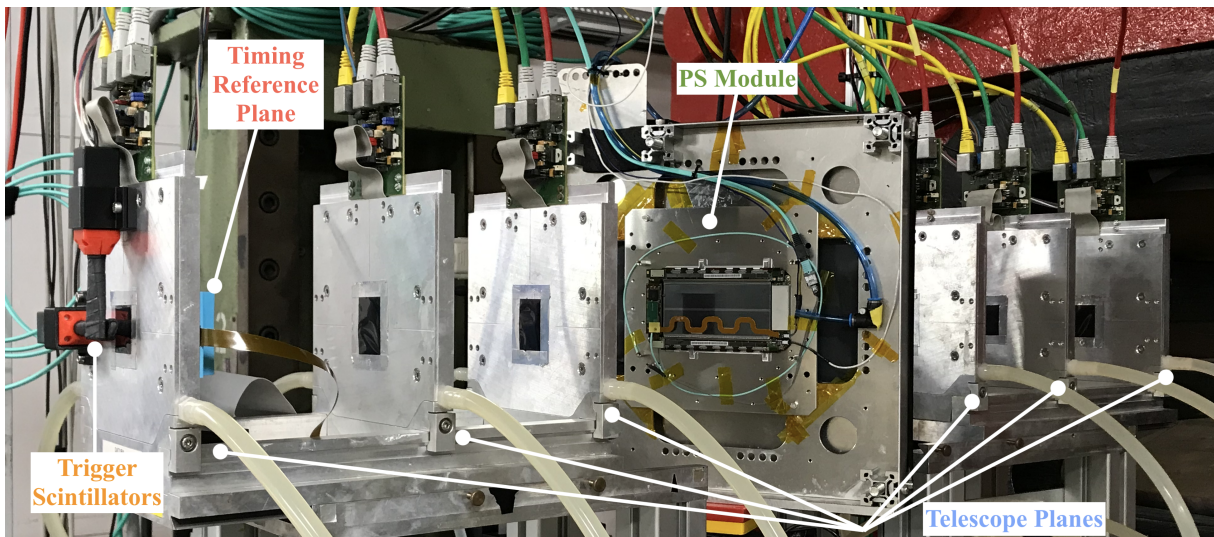


Figure 9.7: Picture of a PS module test-beam setup, indicating the six telescope planes, the trigger scintillators (only the downstream is shown), the timing reference plane and the integrated PS module. The PS module is placed at the center of the beam telescope, between three upstream and three downstream telescope planes.

Figure 9.7 shows a picture of the PS module test-beam setup, indicating the position of each of the six beam telescope planes, the crossed trigger scintillators (the upstream ones are hidden), the timing reference plane and the PS module. The PS module is integrated to the test-beam setup by means of a dedicated aluminium box. The module, placed on its carrier plate, is attached to the box plate via plastic screws to isolate it from the potential environment noise pickups. It is oriented such that the pixel sensor, or the bottom side of the module, is the closest to the upstream part of the beam telescope. A feed-through opening sealed with a foam block is provided at the top of the box to allow the routing of the power cables, optical fiber and dry air tube used for passive cooling of the DC-DC converters on the POH. The box is placed in the middle of the beam telescope and is mounted onto dedicated motion stages: a rotation stage is used to rotate the module around the axis parallel to the strips (y-axis) while a translation stage is used to translate the module along the axis perpendicular to the strips (x-axis), as defined in Figure 9.2.

Figure 9.8 shows the data acquisition scheme of the PS module test-beam. Each of the beam telescope, timing reference plane and PS module are connected to their corresponding data acquisition systems, namely the National Instruments (NI) system, the Digital Test Board (DTB) and the FC7 board, respectively. The data acquisition systems are connected to the AIDA TLU. The NI system and the FC7 board operate in EUDET handshake mode while the DTB is not using any handshake mode. Finally, the trigger scintillators provide their corresponding signals as inputs to the TLU via LEMO cables.

The data acquisition is triggered by the passing of a particle through the two sets of crossed scintillators. Upon reception of the four scintillators signals, the TLU uses an AND logic gate to generate a trigger signal which is distributed to all the integrated devices. This way, the data acquisition is only triggered if a coincidence is recorded across the four scintillators. The handshake protocol then takes place, and no further trigger signal is issued unless all devices have finished the acquisition. The data corresponding to the trigger is collected by the EUDAQ framework, stored onto disk, and data quality control plots are displayed on the monitoring window. This flow is repeated for every event across the whole duration of the data collection.

In the case of the PS module, to ensure the correct acquisition of the data, two additional settings need to be configured: the trigger (L1A) latency and the stub latency. The trigger latency corresponds to the time delay between the time when a particle is detected by the readout chips and the arrival of the trigger signal. It is configured at the

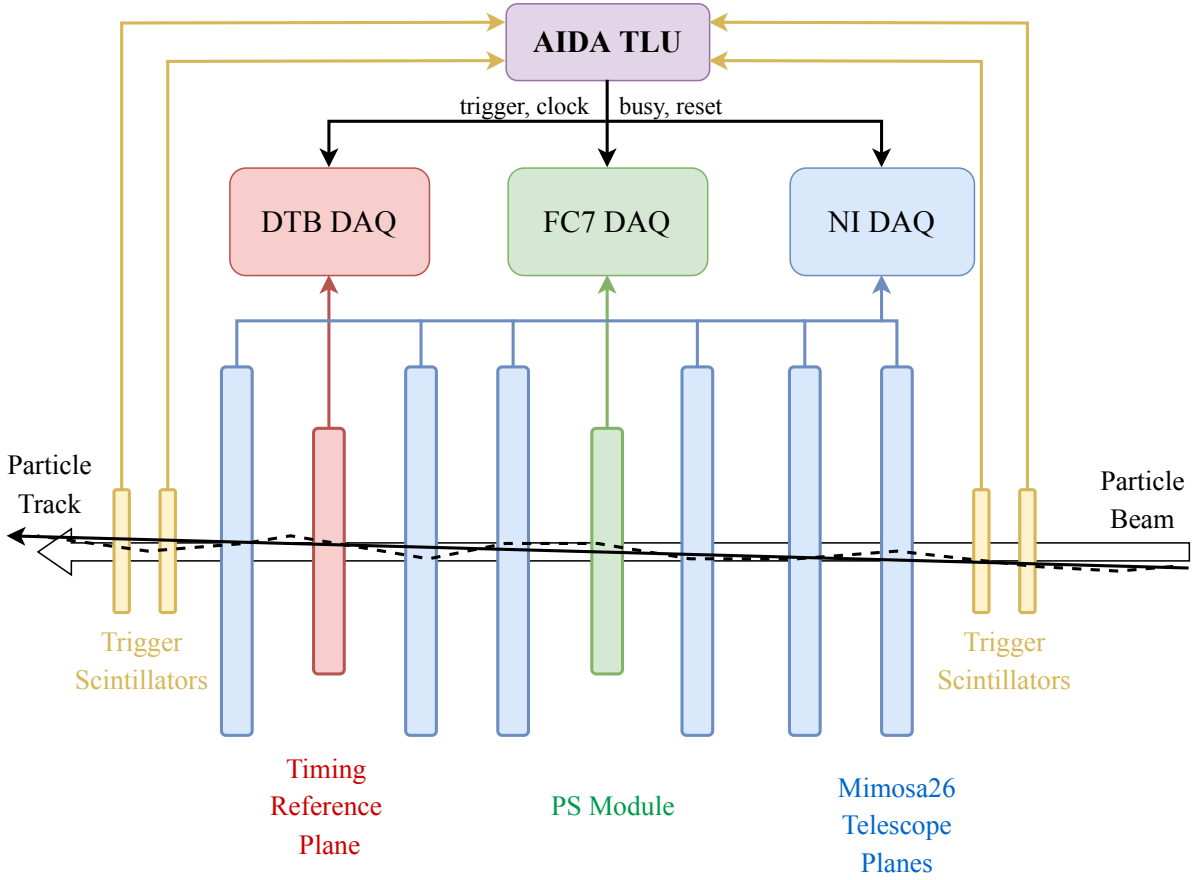


Figure 9.8: Schematic view of the data acquisition scheme during a PS module test-beam. Each device is connected to its corresponding data acquisition system. The trigger scintillators provide signals upon traversal of a particle, and the TLU distributes a trigger signal to the devices if a coincidence is recorded.

level of the front-end chips and is fine tuned such that from all the L1 data stored in the front-end readout buffers, the ones transmitted to the back-end system correspond to the received trigger signal. On the other hand, the stub latency is a setting that needs to be configured at the level of the back-end system as the L1 and stub data are transmitted asynchronously with respect to each other and over independent data paths. This leads to a difference between their corresponding arrival times. Therefore, the stub latency is fine tuned such that the stub data is properly matched to its corresponding L1 data in the back-end system.

To do so, the L1 and stub latencies are successively scanned in steps of 25 ns (corresponding to the bunch crossing clock cycle) while recording the number of L1 hits and stub entries. The L1 and stub latency values are chosen such that both their corresponding

number of entries are maximized. Figure 9.9 shows test-beam L1 latency scan distributions for both MPA and SSA chips measured in *edge* sensitive sampling mode. The one bunch crossing cycle difference between the MPA and SSA is due to design differences of the on-chip bunch crossing counters.

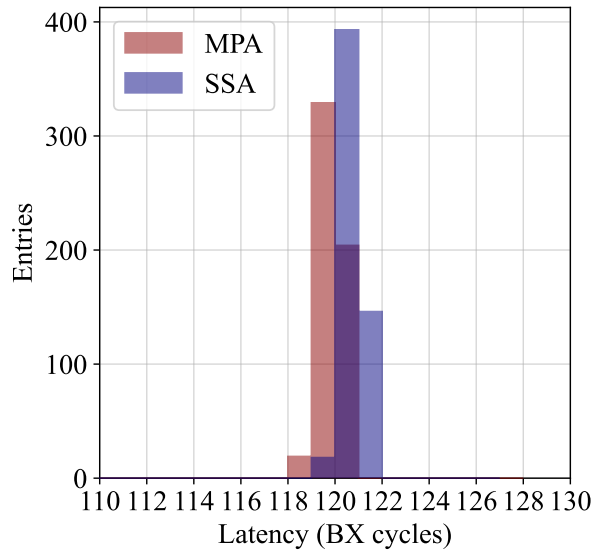
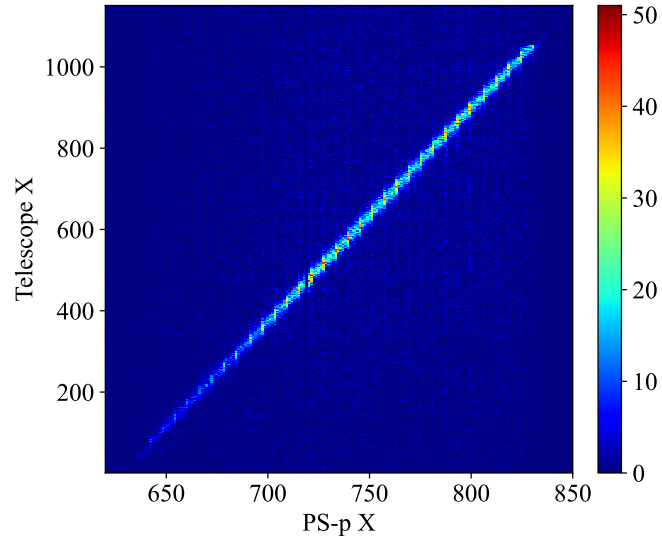
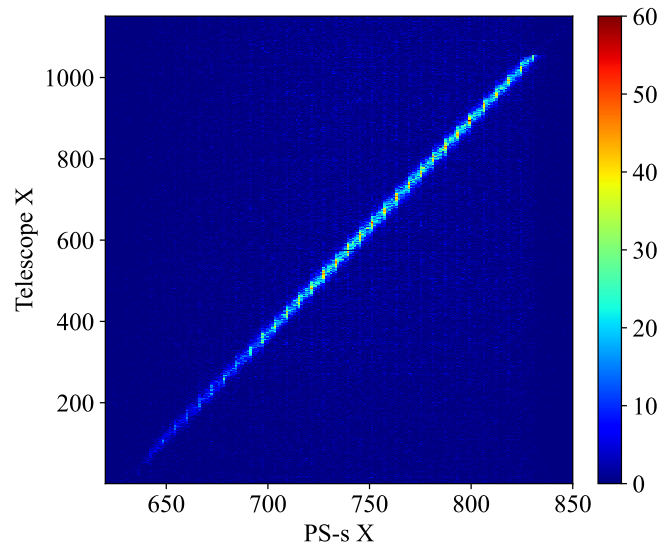


Figure 9.9: L1 Latency distributions for MPA and SSA chips. The latencies were measured in *edge* sensitive sampling mode. The difference between optimal MPA and SSA latencies is due to design differences in the respective bunch crossing counters.

Once the L1 and stub latencies are properly configured, data taking can take place. It is of particular importance to ensure that the various devices are running synchronously. To do so, hit correlation plots are constantly monitored during the course of the data collection. They correspond to scatter plots where each axis represents the hit entries along the corresponding detector direction, and can be built from combinations of different axes and detectors. Figure 9.10 shows two plots correlating the PS-p and PS-s sensor hits along the x-axis with the beam telescope hits along the same axis. The strongly correlated hits indicate that the two detectors are measuring the same traversing particle and thus are running synchronously. Such a plot is provided for every combinations of axis and devices and allows a continuous verification of the synchronous data taking.



(a)



(b)

Figure 9.10: Correlation plots along the x-axis of the PS-p (a) and PS-s (b) sensors with respect to the beam telescope. The strong correlation indicates that the PS module data is taken synchronously with respect to the beam telescope data.

9.2 Offline Track Reconstruction

In order to study the performance of the device under test from test-beam data, particle tracks need to be reconstructed. To do so, the Corryvreckan analysis framework [92] is employed. It is a versatile and highly modular framework designed to reconstruct and analyze test-beam and laboratory data, with a broad range of supported detectors and readout schemes. In particular, in the case of test-beam data, it provides a set of independent modules to perform geometrical alignment of the detectors, reconstruction of beam telescope tracks, and analysis of selected devices under test. Figure 9.11 shows a flow chart of a typical Corryvreckan test-beam analysis chain.

In the case of the presented flow, EUDAQ2 raw data is decoded and processed to extract the hit and timing information. The extracted data is then used to perform hit clustering, build cluster correlations, reconstruct beam telescope tracks and associate them with the hit clusters in the DUT and timing reference plane. This flow is typically used for each step of the overall analysis strategy, from the initial alignment of the beam telescope, timing reference plane and PS module, to the final PS module performance analysis. This section provides a detailed overview of the PS module test-beam data analysis flow.

9.2.1 Event Building

In the Event Building step, the EUDAQ2 raw data is decoded in order to extract pixel, strip and timing information from all the detectors. It is performed using the so-called *EventLoaderEUDAQ2* module which is instantiated for each detector. This step results in the preparation of data chunks, or so-called events that include data from each detector and that are identified by a commonly associated trigger number. These events are held by the Corryvreckan framework throughout the processing.

9.2.2 Hit Clustering

To perform the hit clustering, the closest-neighbour search algorithm is used for all the pixels or strip hits from the same detector plane. In principle the cluster position is calculated using a charge-weighted centre-of-gravity algorithm if charge information is available. However, for binary hit information such as that of the SSAs and MPAs, the cluster position is calculated as the arithmetic mean.

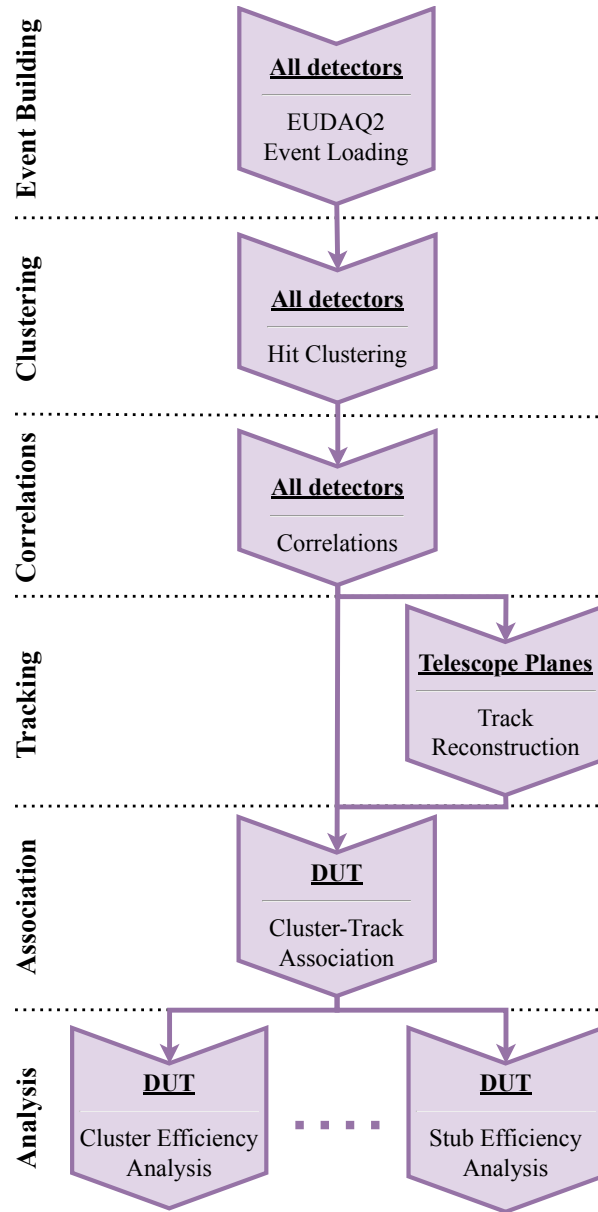


Figure 9.11: Flow chart of a typical Corryvreckan test-beam analysis chain. The steps targeting "All detectors" correspond to multiple instantiations of a single Corryvreckan module for different detectors and the offset modules operate on a subset of detectors. Modified from [92].

9.2.3 Track Reconstruction

In Corryvreckan, the procedure of finding track candidates is coupled to the actual track fitting routine. The former is realized in dedicated modules that have access to the different track fitting models, such that a track candidate is constructed, a fit performed, and the result reported back to the track finding module. For the PS data analysis, the *Tracking4D* module is used. It starts from the two first planes in the upstream part of the beam telescope to build a first track segment and subsequently adds more clusters from the remaining planes if they are within a configurable spatial and time window. As far as track modeling is concerned, the reconstruction makes use of the General Broken Line (GBL) model, which was briefly described in Section 3.3. The latter is of particular importance as it accounts for kinks at every individual detector plane caused by multiple Coulomb scattering along the track path.

9.2.4 Track-Cluster Association

In the association step, reconstructed beam telescope tracks are associated to clusters in one or more of the integrated detectors. Also multiple clusters from the same detector can be associated with a track. In Corryvreckan, the access is given to either all of the associated clusters per detector or only to the closest in space. In practice, the closest clusters in space are chosen such that they yield a distance between their position and the track position that is within a configurable window. For the present analysis only the closest associated clusters are used.

9.2.5 Alignment

In order to ensure a high precision in track reconstruction, the relative position of each of the telescope planes, the timing reference plane and the PS module must be aligned with respect to each other. Corryvreckan provides tools to perform a two-step alignment procedure [93]. Each step produces an updated geometry description of the setup that can be reused as an input for the subsequent alignment step as well as the final analysis.

In the first step, or *pre-alignment*, correlations are calculated between all detectors and a reference plane, usually the first beam telescope plane. These correlations are iteratively calculated and the detector positions corrected in the global x and y coordinates such that their corresponding residuals are centered around zero. The pre-alignment results in a coarse correction of each detector position that allows, with loose association criterias,

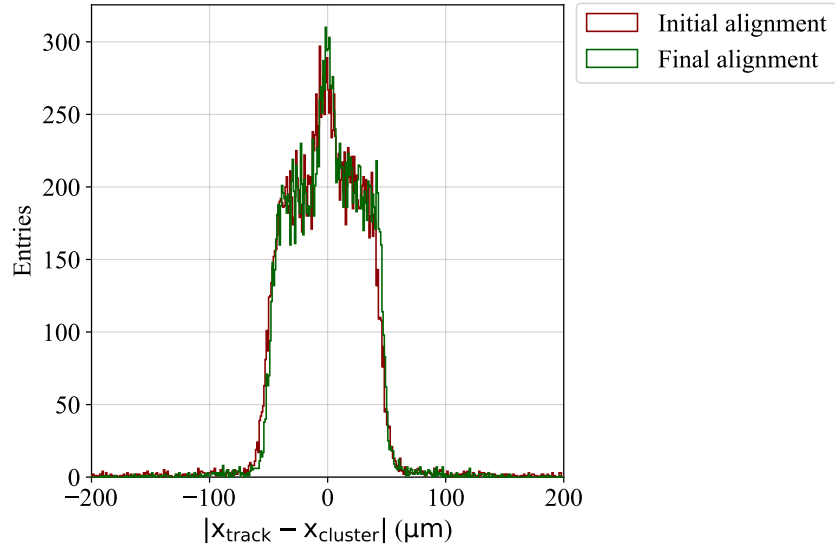
for a preliminary reconstruction of tracks needed for the second alignment step.

The second step corresponds to the final alignment of the detectors using finer global position corrections. The preliminary tracks reconstructed using the pre-alignment geometry are used as input. The framework provides different modules to perform the track fitting, but the one used for the PS data analysis relies on an iterative refit of individual tracks and minimization of the sum of the track χ^2 values using the Minuit2 [94] minimization tool. At each iteration, the tracks are reconstructed, fitted and the corresponding x and y residuals are calculated. Multiple alignment iterations are therefore required in order to converge towards a χ^2 minimum, thus ensuring that the residual distributions yield the minimum width and are well centered around zero. This way corrections to the global position of each detector can be extracted and included into a final geometry description that can be used in the final analysis.

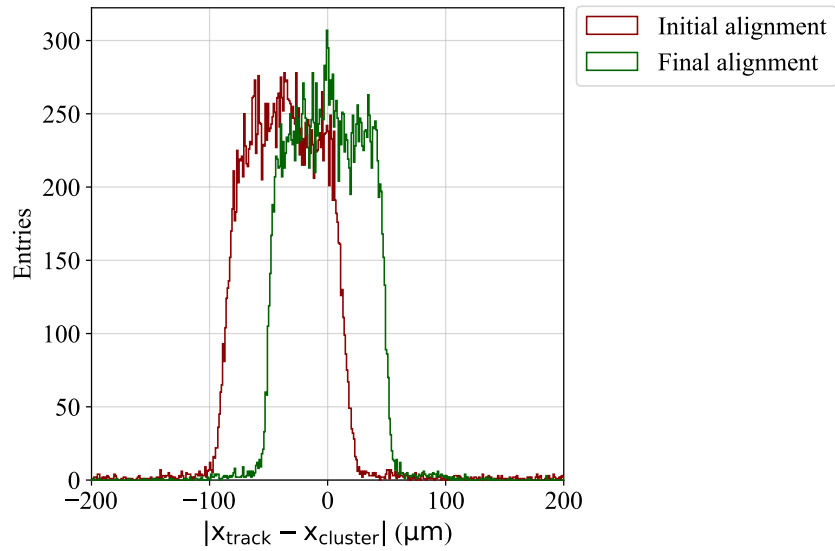
As far as PS module test-beam data is concerned, in addition to the beam telescope and timing reference planes, each of the PS-s and PS-p sensors need to be aligned independently. This is due to the fact that the PS-s and PS-p sensors are processed as two independent detector planes in both EUDAQ2 and Corryvreckan frameworks. Figure 9.12 shows an example result from the initial and final alignment steps performed using data collected at perpendicular beam incidence. It shows the residuals along the x-axis for the PS-p (a) and PS-s (b) sensors. After the final iteration step the distributions are well centered around zero, yielding a minimum width corresponding to the sensor pitch, as expected. The absence of difference between the initial and final alignment steps in the case of the PS-p sensor is mainly due to the fact that the coarse corrections applied by the pre-alignment procedure already lead to a good alignment. Finally, the peak at the center of the residuals distributions from both sensors corresponds to clusters made of more than one pixel or strip.

9.2.6 Analysis

The performance analysis of each detector is provided in a modular way as well. Individual Corryvreckan modules are available to assess for example the detection efficiency (*AnalysisEfficiency*) or the spatial resolution (*AnalysisDUT*) of the device under test. In addition, a module fully dedicated to the analysis of the stub detection performance was developed in the context of this thesis. All these modules can be invoked all together, independently and sequentially within the same analysis flow. The corresponding results from the PS module data are presented in the following section.



(a)



(b)

Figure 9.12: PS-p (a) and PS-s (b) sensors residual distributions along the x-axis at initial and final alignment steps. The residuals are corrected such that they are centered around zero, yielding the narrowest distribution. The peak at the center of the distributions corresponds to clusters made of more than one pixel or strip.

9.3 Performance Studies

The performance results presented in this section correspond to the data collected at the DESY-II Test-Beam Facility using a 4.0 mm PS prototype module with MPA2.0 and SSA2.0 front-end chips as shown in Figure 9.7. During the test-beam campaign the module was exposed to a 4 GeV electron beam and multiple measurement programs were pursued. The studies presented in this section focus on the assessment of the PS module cluster detection and stub efficiencies as a function of front-end signal threshold, sensor bias voltage and rotation angle. The latter is of particular importance as it allows to emulate the bending of particles in a magnetic field and thus validate the functionality of the p_T discrimination logic.

9.3.1 Definitions

In order to study the performance of the PS module, quantities that correspond either to parameters of the collected data or to the data selection criteria need to be defined.

Cluster & Stub Efficiencies

The cluster and stub efficiencies are quantities that assess the performance of the module in detecting traversing particles and forming their corresponding stub primitives, respectively. The efficiency analysis relies on the association of particle tracks and corresponding hit clusters in the DUT, here the PS module. However, as mentioned earlier, due to the long integration time of the beam telescope readout system, the multiplicity of the reconstructed tracks is often higher than one. Therefore, to only select particle tracks that shall be detected within the 25 ns time resolution of the PS module readout, information from the BPIX timing reference plane is used. In practice, the PS module efficiency studies are performed only with particle tracks that yield a corresponding cluster in the timing reference plane. A fiducial window is defined around the track impact point at the reference plane such that a matching cluster is declared only if the corresponding residuals fall within the window boundaries. The fiducial window for this analysis was chosen such that it corresponds to two times the BPIX pixel pitch along both the x- and y-axes, which results in the following selection cut criteria

$$|x_{\text{track}}^{\text{ref}} - x_{\text{cluster}}^{\text{ref}}| \leq 300 \text{ } \mu\text{m} \quad ; \quad |y_{\text{cut}}^{\text{ref}} - y_{\text{cluster}}^{\text{ref}}| \leq 200 \text{ } \mu\text{m}$$

On the other hand, each selected track is used to interpolate its corresponding impact point at both the PS-p and PS-s sensors and compare it to the detected clusters and

stubs. A cluster or stub is considered efficient if its corresponding residuals are within a fiducial window. Figure 9.13 shows a sketch of the corresponding definition. For the PS-p sensor the fiducial area is defined to be twice the pitch size along both the x- and y-axes. However, for the PS-s sensor, while the window is defined similarly to the PS-p along the x-axis, the selection cut along the y-axis is in practice irrelevant due to the large strip size. As far as stubs are concerned, their position corresponds to the position of the cluster in the seed layer, namely the PS-p sensor. Therefore, the selection cuts used for the PS-p clusters are used for stubs as well.

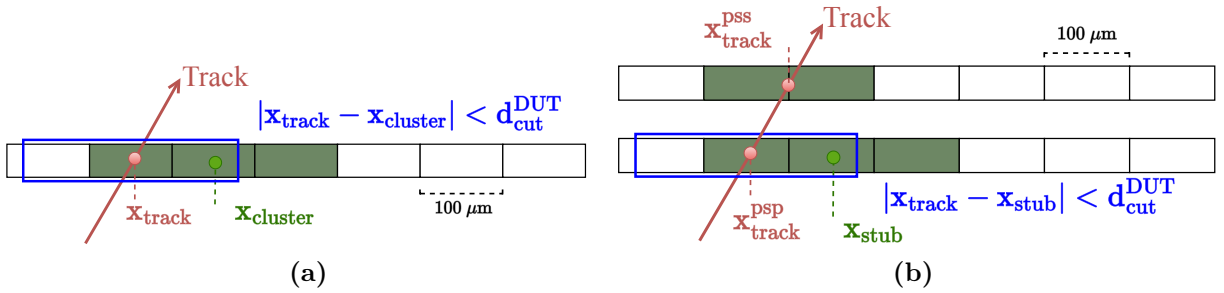


Figure 9.13: Illustration of the definition of PS-p and PS-s cluster efficiencies as well as the stub efficiency along the x-axis used for the test-beam analysis. (a) A cluster is considered efficient if its residual along the x $|x_{\text{track}} - x_{\text{cluster}}|$ is smaller than the selection cut $d_{\text{cut}}^{\text{DUT}}$. (b) A stub formation is considered to be efficient if the residual of the corresponding PS-p cluster (seed) is smaller than $d_{\text{cut}}^{\text{DUT}}$. The same principle applies along the y-axis.

The selection cut criteria for each of the PS-p, PS-s and stubs correspond to

$$|x_{\text{track}}^{\text{psp}} - x_{\text{cluster}}^{\text{psp}}| \leq 200 \mu\text{m} \quad ; \quad |y_{\text{track}}^{\text{psp}} - y_{\text{cluster}}^{\text{psp}}| \leq 3000 \mu\text{m}$$

$$|x_{\text{track}}^{\text{pss}} - x_{\text{cluster}}^{\text{pss}}| \leq 200 \mu\text{m} \quad ; \quad |y_{\text{track}}^{\text{pss}} - y_{\text{cluster}}^{\text{pss}}| \leq 25000 \mu\text{m}$$

$$|x_{\text{track}}^{\text{psp}} - x_{\text{stub}}^{\text{psp}}| \leq 200 \mu\text{m} \quad ; \quad |y_{\text{track}}^{\text{psp}} - y_{\text{stub}}^{\text{psp}}| \leq 3000 \mu\text{m}$$

Each of the cluster and stub efficiencies can then be calculated by counting the number of tracks with an associated cluster in the timing reference plane (REF), and the number of PS clusters and stubs associated to the selected tracks and fulfilling the corresponding residual cuts. The efficiency can therefore be written as

$$\epsilon_{\text{clusters/stubs}} = \frac{n_{\text{efficient clusters/stubs}}}{n_{\text{ref tracks}}} = \frac{\text{telescope tracks} \in \text{DUT}_{\text{clusters/stubs}} \cap \text{REF}}{\text{telescope tracks} \in \text{REF}} \quad (9.1)$$

The statistical uncertainty for the cluster and stub efficiencies is given by the standard deviation of the mean of a binomial distribution given by

$$\sigma_{\epsilon_i} = \sqrt{\frac{\epsilon_i(1 - \epsilon_i)}{n_{\text{ref tracks}}}} \quad (9.2)$$

TDC

During the operation of the detector at the LHC, the accelerator clock is shared among all the subdetectors in order to synchronize the signal readout with the particle arrival time, allowing for an optimal sampling of the charge pulse. However, in the DESY-II Test Beam Facility, the PS module readout and the accelerator clocks are asynchronous. This leads to particle arrival times randomly distributed with respect to the MPA and SSA sampling clock cycles. Therefore, the corresponding charge pulse is not consistently sampled at the maximum, resulting in a phase dependency of the cluster detection and stub efficiencies. This effect is compensated in the μ DTC firmware by sampling the trigger arrival time with a 320 MHz clock and recording the phase difference with respect to the internal 40 MHz nominal clock. The difference is then encoded via a Time-to-Digital Converter (TDC) and saved as a TDC phase.

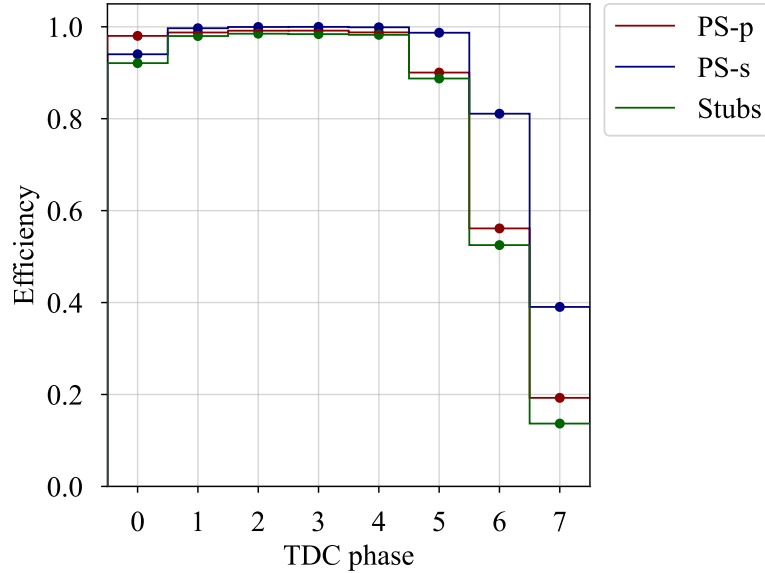


Figure 9.14: PS module efficiencies dependency on the trigger arrival time with respect to the 40 MHz system clock, or TDC phase, due to the asynchronous accelerator and system clocks.

Figure 9.14 shows a distribution of the PS-p, PS-s and stub efficiencies as a function of the TDC phase. In order to extract meaningful efficiency results with respect to the module

operation at the LHC, a cut on the TDC phase is applied such that only the most efficient TDC phases (1, 2, 3, 4) are considered for the analysis.

Channel Masking

During the test-beam campaign, functional failures of the startup sequence on the left FEH were observed. Therefore it was disabled during the data taking, and the beam was oriented towards the right side of the module only. In addition, following the campaign, the preliminary analysis uncovered additional issues affecting the stubs mostly located at the edges of the MPA chips. These issues were understood to be related to a mis-configuration of the stub correlation window. The latter was configured to be ± 8 strips, while the stub finding logic in the MPA was designed to operate with a stub window up to ± 4 strips. Therefore, the affected channel regions are masked during the analysis in order to prevent any undesired effect on the cluster detection and stub efficiencies. This is performed using a dedicated channel masking module in Corryvreckan in which the set of channels to be masked can be provided through a dedicated configuration file. Finally, in order to avoid any artificial inefficiencies, all the reconstructed tracks located close to the masked channels are discarded from the analysis.

Measurement Program

The campaign targeted the commissioning of the latest DAQ developments and the preliminary assessment of the prototype module performance. The measurement program included data collection as a function of the sensor bias voltage, the front-end signal threshold and the particle incidence angle. Finally, the data was analyzed following the campaign, and multiple studies were performed to evaluate the module performance, focusing on cluster size and resolution studies, cluster and stub detection efficiencies, and p_T discrimination performance.

9.3.2 Cluster Size

Cluster size measurements are of particular importance as they provide insightful information about the spatial resolution of the module. In addition, cluster size distributions are a good means of inferring the rotational misalignment of the module on the rotation stage with respect to the beam and correct for it. The cluster size corresponds to the projection of the generated charges inside the sensor bulk on the implant pixels/strips surface. For

an ideal point like implant, the cluster size is defined by the geometrical relation

$$s(\theta) = s_0 + \frac{d_0}{p} \cdot |\tan(\theta - \theta_0)| \quad (9.3)$$

where s_0 is the cluster size at perpendicular beam incidence (zero track angle), d_0 the sensor thickness, p the sensor pitch and θ the track incidence angle. θ_0 represents the potential angular offset between the orientation of the module and the track incidence angle that corresponds to the physical misalignment of the module on the rotation stage. However, for non-ideal sensors, the charge sharing among neighbouring strips depends on multiple parameters. On the one hand, it strongly depends on the sensor design parameters, namely the geometry, the implant structure and the electric field shape. On the other hand, in the case of binary readout such as in the PS module, the signal threshold used for the discrimination affects the charge distribution and thus the cluster size. Therefore the d_0/p factor is replaced by a parameter α that shall account for all the aforementioned effects and the parametrization of the cluster size distribution is finally given by

$$s(\theta) = \frac{1}{\sqrt{2\pi\sigma^2}} \cdot \int_{-\infty}^{+\infty} [s_0 + \alpha|\tan(t - \theta_0)|] \cdot e^{-\frac{(t - \theta)^2}{2\sigma^2}} dt \quad (9.4)$$

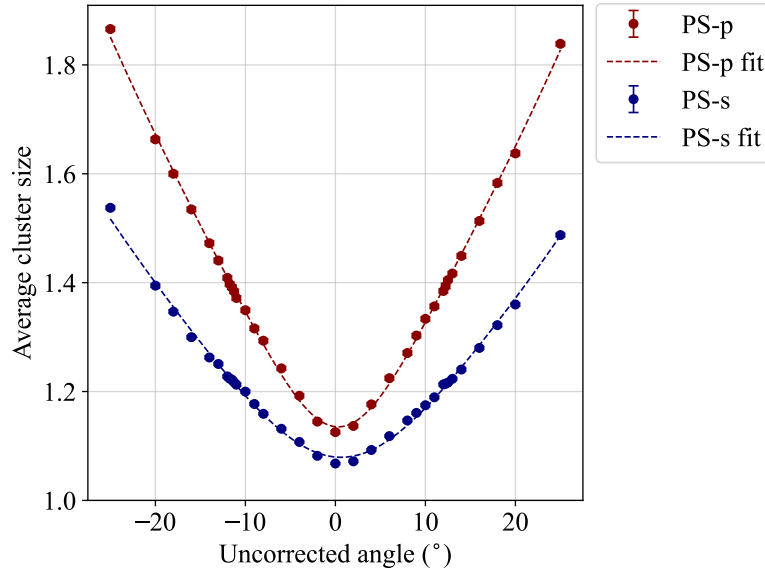


Figure 9.15: Cluster size as a function of the uncorrected rotation angle. The sensor bias voltage is set to 300 V for both the PS-p and PS-s sensors, and the front-end signal threshold is set to an absolute value of 90 ThDAC and 50 ThDAC for the MPA and SSA chips, respectively.

Figure 9.19 shows the distribution of cluster size as a function of the module rotation angle (track incidence angle) for both PS-p and PS-s sensors. The distribution only considers clusters matched to telescope tracks with a corresponding cluster in the timing reference plane. At perpendicular angle, where the charge sharing is minimal, the cluster size is measured to be 1.12 for PS-p and 1.07 for PS-s clusters. However, the larger the rotation angle, the larger is the track incidence angle correspondingly, thus charge sharing and cluster sizes are increased. The average angular offset is extracted by fitting Equation 9.4 to both PS-p and PS-s distributions and yields an angle of $0.32^\circ \pm 0.03^\circ$ for the PS-p sensor and $0.63^\circ \pm 0.06^\circ$ for the PS-s sensor. The difference between the two values is mainly due to the spacing between the two sensors that leads to the PS-s sensor seeing an incidence angle slightly larger than the PS-p sensor. The average of the two values is taken as a correction and applied to all the rotation angles in the analysis.

9.3.3 Resolution

Resolution measurements are crucial to assess the performance of the module in accurately determining the position of the traversing particle. It is a measure of how well the module can localize the point of interaction of the particle within the sensor volume. It depends on several module design and operation parameters, such as the sensor geometry, the sensor pitch or the signal-to-noise ratio. In the presented results, each of the PS-p and PS-s resolutions are extracted using the corresponding cluster-track residual distributions. The standard deviation or root mean square (RMS) of the distributions is defined as the measured resolution σ_{meas} . The latter includes both the sensor intrinsic resolution σ_{int} and the pointing resolution of the telescope σ_{tel} . Assuming that the intrinsic and telescope resolutions are uncorrelated, σ_{int} can be written as

$$\sigma_{\text{int}} = \sqrt{\sigma_{\text{meas}}^2 - \sigma_{\text{tel}}^2} \quad (9.5)$$

The pointing resolution of the telescope depends on the telescope geometry and position of the DUT, and is calculated using the GBL Track Resolution Calculator [95]. For the measurements with high statistics performed at perpendicular beam incidence, the calculation of the pointing resolution of the telescope at the DUT position results in $\sigma_{\text{tel}} = 3.54 \mu\text{m}$.

Both the PS sensors and the telescope resolutions are dominated by systematic uncertainties related to the dependency on the residual cut, the estimation of the material budget or the particle energy. In the present analysis, these systematic uncertainties are not taken into consideration and only the RMS is taken in first approximation. Table 9.1

shows the extracted intrinsic resolution along both x- and y-axes for the PS-p sensor, and only along the x-axis for the PS-s sensor. Keeping in mind the considered approximations, the extracted values remain close to the expected binary resolution $p/\sqrt{12}$ of each sensor, where p is the corresponding sensor pitch.

Table 9.1: Expected ($p/\sqrt{12}$) and measured intrinsic resolutions at perpendicular beam incidence, for both PS-p and PS-s sensors

Resolution	Expected	Measured
$\sigma_{\text{PS p,x}}[\mu\text{m}]$	28.9	33.5
$\sigma_{\text{PS p,y}}[\mu\text{m}]$	423.5	425.3
$\sigma_{\text{PS s,x}}[\mu\text{m}]$	28.9	32.7

Besides the optimization of the module operation parameters (ie: signal threshold, bias voltage, beam energy) and the precise determination of the corresponding systematic uncertainties, the spatial resolution can be improved by increasing the incidence angle of the traversing particles. When a particle traverses the sensor at a shallow angle, the generated charge is shared among multiple pixels or strips leading to more precise determination of the impact position. In the case of binary readout, this improvement strongly depends on the applied signal threshold such that an optimal combination between the signal threshold and the incidence angle can be found in order to maximize the charge sharing. For the presented results, the signal threshold was fixed at an absolute value of 90 ThDAC for the MPA chips and 50 ThDAC for the SSA chips such that the cluster efficiency is maximized as discussed later in Section 9.3.4. In addition, the distance between the upstream and downstream parts of the telescope was increased in order to allow the rotation of the module on the stage. This change of configuration degrades the telescope resolution that was extracted to be $\sim 9 \mu\text{m}$. Figure 9.16 shows the resolution along the x-axis as function of the beam incidence angle for both PS-p and PS-s sensors. The strongly fluctuating distributions are most likely due to two reasons: First, the lack of statistics which is exacerbated by the additional TDC selection applied to the collected data. Second, to a poor track reconstruction caused by the widely open beam telescope arrangement required to allow the rotation of the module. In order to be able to rotate the module, the distance between the upstream and downstream beam telescope planes needs to be increased, thus leading to a non-optimal geometry of the beam telescope resulting in reconstructed tracks of less quality than in the case where the distance between the individual planes in the upstream and downstream parts of the telescope is small.

Nevertheless, the distributions show a measured minimum around $\pm 15^\circ$ that maximizes the resolution of both sensors, yielding a resolution at the level of the expected one.

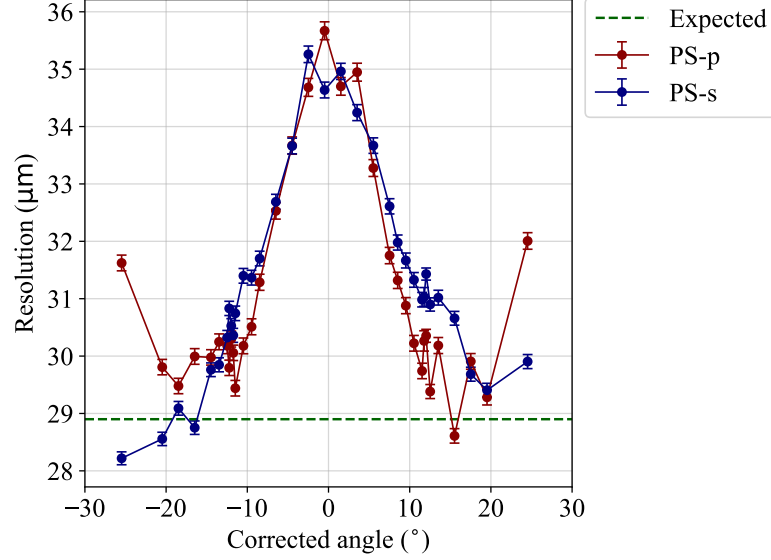


Figure 9.16: Resolution along the x-axis as a function of the corrected rotation angle. The sensor bias voltage is set to 300 V for both the PS-p and PS-s sensors, and the front-end signal threshold is set to an absolute value of 90 ThDAC and 50 ThDAC for the MPA and SSA chips, respectively.

9.3.4 Cluster & Stub Detection Efficiencies

To study the cluster and stub detection efficiencies, the module was positioned perpendicularly to the electron beam direction. This way the particle travelling distance inside the silicon sensors is reduced and the generated signal charge is minimal. The study investigates the effect of two main operation parameters on the detection efficiencies, namely the sensor bias voltage and the signal threshold. Cluster and stub efficiencies are calculated as a function of the aforementioned parameters over defined corresponding ranges. The stub correlation window was set to ± 8 strips with no configured offset. This section describes each study and discusses the obtained results.

Bias Voltage Dependency

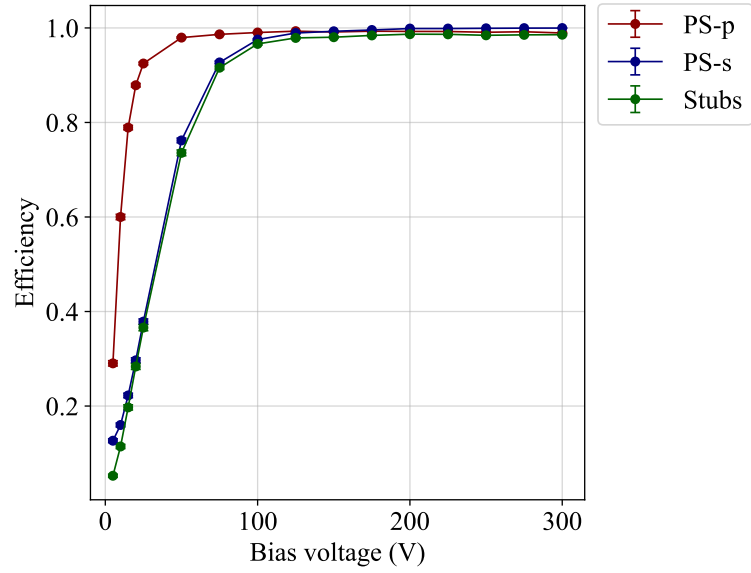
The bias voltage dependency study allows the determination of the optimal operation point of the sensor bias voltage. In the study, the signal threshold was set to an absolute value of 90 ThDAC and 50 ThDAC for the MPA and SSA chips, respectively. The latter

is chosen according to the post-assembly channel noise extracted prior to the data taking and presented in Section 8.2.5 such that it is located 5σ away from the pedestal. The bias voltage, which is commonly distributed to both the PS-p and PS-s sensors, is then varied between 0 V and 300 V while the corresponding cluster and stub efficiencies are calculated at each step. Figure 9.17 shows the evolution of the cluster and stub efficiencies as a function of the sensor bias voltage and a zoomed view of the high efficiency region is provided.

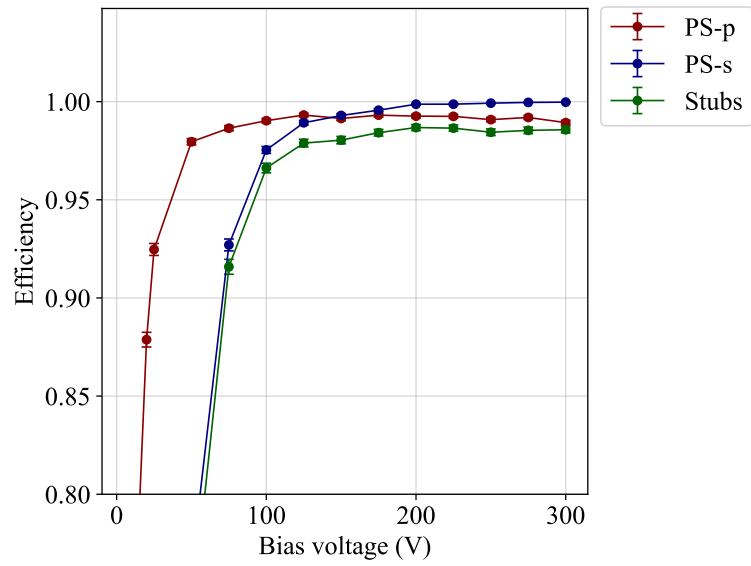
The efficiency increases following the high voltage ramp up until reaching a plateau. This increase corresponds to the progressive enlargement of the space charge region that leads to the increase of the generated signal charge in the sensor bulk. The turning point towards the plateau marks the minimum operating voltage that ensures a signal charge significantly larger than the configured signal threshold. The minimum operating voltage is shown to be around 50 V for the PS-p sensor and 100 V for the PS-s sensor. Beyond the optimal operation voltage, the efficiencies reach a plateau corresponding to above 99% for PS-p and PS-s clusters and above 98% for stubs. The slightly reduced PS-p efficiency compared to the PS-s is known to be caused by the Punch Through Structure (PTS) and the bias grid as described in Section 5.1 and investigated in [96]. Moreover, as the stub efficiency depends on the joint PS-p and PS-s efficiencies, its evolution is closely bound to the fastest decreasing efficiency, in this case the PS-s cluster efficiency. Finally, at nominal bias voltage, the stub efficiency appears to be slightly lower than the expected product of the PS-p and PS-s cluster efficiencies. This inefficiency is induced by randomly located missing and spurious stubs caused by the misconfiguration of the stub window described in Section 9.3.1.

Signal Threshold Dependency

Similarly to the bias voltage dependency, the signal threshold dependency concerns the determination of the optimal signal threshold at which the module should be operated. On the one hand a threshold that is too high leads to undetected small signal pulses and thus a reduced detection efficiency. On the other hand, a threshold that is too low leads to noise hits, distortions in the detection efficiency and a considerable effect on the p_T discrimination and tracking performance. In this study, the sensor bias voltage was set to 300 V. The signal threshold was then varied for both MPA and SSA chips in the ranges between 90 ThDAC and 250 ThDAC, and between 50 ThDAC and 250 ThDAC, respectively.

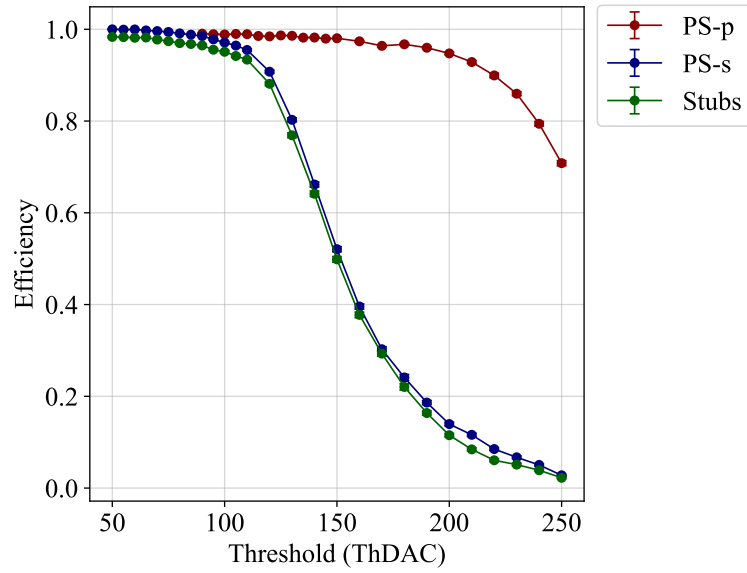


(a)

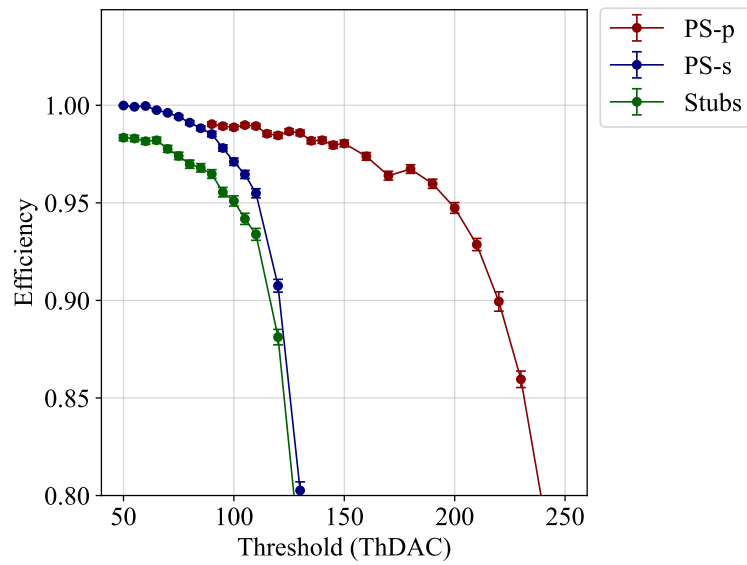


(b)

Figure 9.17: Cluster and stub efficiencies as a function of the sensor bias voltage (a), with a zoomed version on the high efficiency region (b). The front-end signal threshold is set to an absolute value of 90 ThDAC and 50 ThDAC for the MPA and SSA chips, respectively.



(a)



(b)

Figure 9.18: Cluster and stub efficiencies as a function of the front-end signal threshold (a), with a zoomed version on the high efficiency region (b). The sensor bias voltage is set to 300V for both the PS-p and PS-s sensors.

Figure 9.18 shows the evolution of the cluster and stub efficiencies as a function of the signal threshold as well as a zoomed view on the high efficiency region. At the lowest measured threshold, the result yields PS-p and PS-s cluster efficiencies above 99% and a stub efficiency above 98%. Due to the different position of the signal baseline as well as the different signal shapes in each of the MPA and SSA chips, the relative position of the signal threshold differs. As a result, the efficiency drop appears at different signal thresholds for each chip. The lower signal baseline and the higher relative threshold in the SSA lead to a PS-s efficiency drop at a lower threshold compared to that of the PS-p. The efficiency further decreases until reaching its minimum at a threshold of 250 ThDAC.

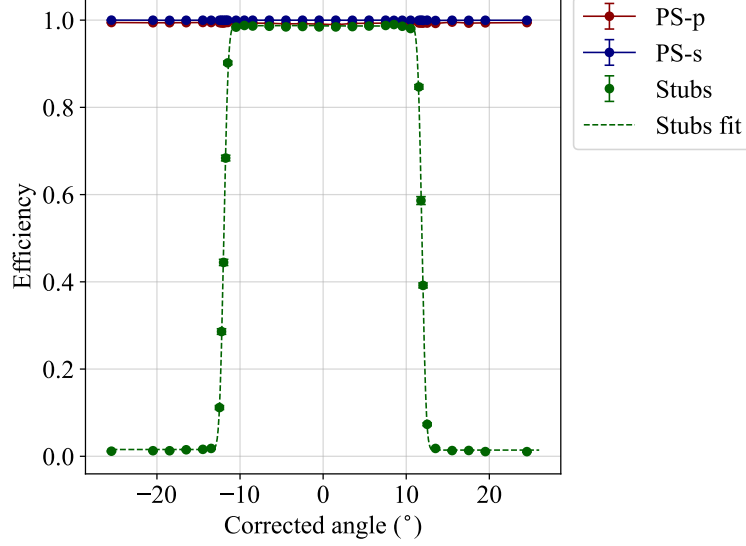
9.3.5 Transverse Momentum Discrimination Performance

To study the momentum discrimination performance, the module is rotated around the y-axis to emulate signals of particle trajectories bent by the magnetic field inside the CMS detector. In addition the module is operated at the nominal bias voltage of 300 V and signal thresholds of 90 ThDAC and 50 ThDAC for MPA and SSA chips, respectively. Figure 9.19 shows the cluster and stub efficiencies as a function of the corrected rotation angles.

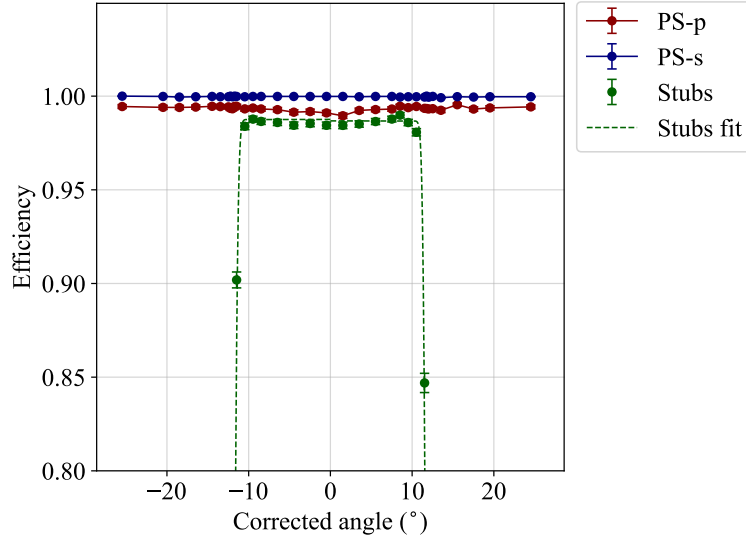
As far as cluster detection is concerned, the measurements yield a corresponding efficiency stable above 99% across the whole range of module rotation angles for both the PS-p and PS-s sensors. On the other hand, the stub efficiency remains constant at a level above 98% until reaching angles around $\pm 12^\circ$. At these angles a sharp drop of the stub efficiency is observed, reaching approximately 1%. In practice, increasing the module rotation angle leads to the creation of PS-p and PS-s clusters with an increasing spatial offset between their corresponding cluster centers. Therefore, when the spatial offset exceeds the programmed stub correlation window of ± 8 strips, no valid stubs are formed anymore leading to a decrease of the stub efficiency. The residual 1% efficiency beyond the turn-on angles is mostly dominated by spurious stubs caused by the stub window-related issue described in Section 9.3.1. This stub efficiency behaviour corresponds to the so-called *stub turn-on characteristic* and can be modelled by an error function of the form

$$f(\theta, p_0, p_1, p_2, p_3) = 1 - \frac{1}{2} \left(p_0 + p_1 \cdot \operatorname{erf} \left(\frac{\theta - p_2}{p_3} \right) \right) \quad (9.6)$$

where p_0 is an adjustment parameter to shift the error function towards the fitted stub efficiency and p_1 a scaling factor. On the other hand p_2 and p_3 correspond to the turn-on point and the turn-on width. Each of the positive and negative angles are fitted separately



(a)



(b)

Figure 9.19: Cluster and stub efficiencies as a function of the angular orientation of the module (a), with a zoomed version on the high efficiency region (b). The sensor bias voltage is set to 300 V for both the PS-p and PS-s sensors, and the front-end signal threshold to 90 ThDAC and 50 ThDAC for the MPA and SSA chips, respectively.

and the corresponding fit parameters are extracted as

$$p_2^{>0} = 11.90 \quad ; \quad p_2^{\leq 0} = -11.94$$

where the comparable values stand as a confirmation of the applied angle correction.

As the module rotation corresponds to an emulation of the bend of particle trajectories, the rotation angle can be converted to an equivalent transverse momentum. The latter can be chosen such that it corresponds to different PS module locations in the tracker barrel layer inside the CMS detector. The equivalent transverse momentum can be calculated by taking into account the CMS magnetic field of $B = 3.8$ T, the radial position of the module and using the equation

$$p_T[\text{GeV}] \approx \frac{0.57 \cdot R[\text{m}]}{\sin(\theta)} \quad (9.7)$$

For example, for a PS module positioned in the outer layer of the TBPS region at $R = 52.45$ cm, the configured ± 8 strips stub window would lead to a transverse momentum discrimination threshold of $p_T = 1.43$ GeV. However, while the ± 8 strips stub window proves the p_T discrimination capabilities of the PS module, the Outer Tracker layout and the PS module stub finding logic designs were made such that at most a stub window of ± 4 strips is used. In addition, the choice strongly depends on both the module spacing and the module location inside the detector. Such variability is driven by the objective of, assuming optimal threshold and bias settings to maximize the PS-s and PS-p efficiencies, reaching the target 2 GeV p_T discrimination in all regions covered by the Outer Tracker. Therefore the aforementioned results provide a direct evidence of the capabilities of a PS modules to implement the foreseen p_T discrimination feature. However, they only represent a first step in the understanding of the operational requirements of a PS module and the optimal settings needed for the best performance. In particular, many front-end ASICs settings are still to be investigate in order to ensure that all the expected chip functionalities are validated and the target performances met, especially for irradiated modules. But this already goes beyond the scope of this thesis.

CHAPTER 10

SUMMARY & CONCLUSIONS

With the prospects of the High-Luminosity LHC and the CMS detector Phase-2 upgrade, this thesis provided a description of the development efforts to which I have extensively contributed and that were deployed by the collaboration to drive the Outer Tracker PS module from its conceptual design to the actual production, qualification and performance studies of its early prototypes. It describes the latest design of the module, providing an overview of the individual components and focusing on the silicon sensors, the front-end ASICs and the hybrid circuits. The semi-automated module assembly procedure developed by DESY was introduced and shown to fulfill the precision requirements of the sensor-to-sensor lateral and angular alignments that play a decisive role in the p_T discrimination mechanism. Nevertheless, only few prototype modules have been built so far, and the repeatability of the achieved results is still to be further confirmed and validated. Truth is that even if the assembly system and the procedure are well advanced, further improvements are still needed. In particular, with the prospects of the module production throughput of four bare modules per day, the current time needed to assemble a single bare module is way below the target two hours. Therefore, I believe that the execution of each assembly step must be extensively exercised and timed in order to better understand the various bottlenecks and limitations of the procedure. This shall allow the most realistic estimation of the target time to foresee for a single bare module assembly. In particular, exercises involving the sequential assembly of multiple modules must be carried out with the objective of evaluating the feasibility of the target production throughput. Finally, as the availability of components is identified as one of the main bottlenecks preventing the extensive practice of the procedure, alternative assembly solutions must be investigated

in order to allow for enough preparation prior to the start of the modules production regardless of the immediate availability of components.

The thesis also uncovered the various test systems developed in order to support the qualification of the hybrid circuits and the fully assembled modules. These systems are targeting both the prototyping and the production phases. On the one hand, the hybrids test system was designed in a highly versatile and flexible fashion to fulfill the support of all the different Outer Tracker hybrid circuits. It provides a common multiplexing system capable of hosting up to twelve hybrid circuit test cards. These test cards, six in total if we include the hybrid circuits from both Outer Tracker module types, are designed according to a similar mechanical structure but with a different electronic design to fulfill the qualification requirements of each individual circuit. As of today, the entire volume of test card components for the production phase was produced, and the assembly and the functional verification of each individual test card is ongoing. And with the imminently starting hybrids production, the next milestone to reach is the setup and commissioning of the test systems both at the production companies and at the collaborating institutes involved in the hybrids quality control activities. On the other hand, the single module test system was designed to fulfill the requirement of a unified module qualification environment across the different assembly and integration centers. It consists of a multi-function test station where single modules can be placed, controlled and fully tested. Multiple units were already assembled and delivered to the interested institutes, including DESY. Therefore, each institute must ensure, prior to the launch of the module production phase, the full commissioning of the system and the corresponding software control tools.

As far as data acquisition and control is concerned, a reduced version of the final Outer Tracker DTC system, referred to as the μ DTC system was developed. It targets the needs of both the prototyping and the production phases. It relies on the FPGA-based FC7 board complemented by a dedicated FPGA firmware. The latter is designed such that all types of Outer Tracker test systems, electronic components and functional modules can be supported. The firmware was therefore designed with the core principle of versatility and flexibility, providing multiple functionalities ranging from the control of the hybrids test system, to the optical control and readout of fully functional modules. As of today, the firmware development is in a very well advanced state with a stable support for the hybrid circuits and the single module qualification. However, with the prospects of tests such as burn-in tests where up to ten modules are subjected to thermal cycling or integration tests where multiple modules are tested on various final detector mechanical

structures, finalization of the multi-module readout is of high importance. In particular, I believe that improvements of the synchronous readout and the finalization of the MPA and SSA fast counters readout must be a priority. The former is crucial as it ensures a maximum FC7 module occupancy while the latter is decisive to overcome the present time bottlenecks faced in the qualification of PS modules. In addition, investigations on a possible increase of the multi-module support from the current twelve modules to the ultimate target of sixteen modules must be carried out. On the software side, the Ph2ACF framework is currently chosen as a baseline to support both the hybrids and modules prototyping and production phases, as well as the final Tracker detector operation. The framework already provides a well advanced support of all the available systems and module components. However, the current status of the framework suffers, especially when it comes to the Outer Tracker parts, from structural vulnerabilities that lead to difficulties for external users and new developers to contribute to the development effort. Therefore, efforts must be invested into the redesign of certain hardware and firmware interfaces such that they are brought to a more user-friendly state, abstracting enough the complexity of the electronics and complemented by extensive documentation. This shall ease further developments, in particular when it comes to the implementation of crucial test procedures for the production phase.

Finally, the thesis provided an extensive overview of the developments and activities related to the qualification of individual hybrid circuits and PS prototype modules assembled at DESY. A preliminary set of qualification tests was defined and implemented for each hybrid circuit with the objective of validating their functionality. As of today, the tests procedures for all the hybrid circuit types are in a well advanced state and hundreds of prototype hybrid circuits have been successfully qualified and distributed to the module assembly centers. However, the currently deployed list of tests is still to be finalized and complemented with a list of precise grading criteria that shall apply throughout the imminently starting production phase. In addition, active work is ongoing in order to finalize and validate all the test procedures, including the streamlined results reporting from the test stations to the central data base. Alongside the hybrid circuits qualification, results from the early PS prototype module qualification activities at DESY were presented. They covered qualification of modules both in the laboratory and during test-beam campaigns. The laboratory qualification activities not only focused on the noise performance studies but also covered the development of configuration procedures needed for the modules readout chain to be brought to an operation readiness state. Results showed good I-V characteristics, excellent MPA noise performance, but the SSA were

discovered to yield noise levels higher than expected. Investigations led to the discovery of design vulnerabilities on the Front-End Hybrid circuits that can act as electronic noise sources. The latter were addressed by the hybrids designers in order to ensure a complete mitigation of the vulnerability and guarantee a noise performance at the expected level. These design modification will be introduced in the next version of the hybrid circuits and the performance validation must be of the highest importance prior to the launch of the production phase. In addition, all these performance tests must be complemented by two categories of tests that I believe must be the priority: extensive and systematic validation of the readout chain, and integration tests on prototype mechanical structures. On the one hand, the readout chain validation is of utmost importance as it will pave the path not only to a better understanding of the functional and operational aspects of the module but also to a broad range of developments that will irrigate the Ph2ACF framework. On the other hand, integration tests will be crucial to validate the module functionalities and performance on the foreseen final mechanical supports. Nevertheless, some of the assembled prototype modules were still able to be further qualified during test-beam campaigns organized at the DESY-II Test-Beam Facility. There, the functional performance of a PS module equipped with the latest front-end ASICs available at that time was evaluated. Results yield excellent hit detection efficiencies, exceeding 99% for the strip sensor and 98% for the pixel sensor. In addition, the functionality of the p_T discrimination mechanism was validated, yielding a stub efficiency exceeding 98% and demonstrating the expected efficiency drops beyond the boundaries of the programmable correlation window. Nevertheless, while these preliminary results offer a first validation of the readout chain and the module functionalities, many more studies must be carried out in order to cover all the functional aspects of the module. These studies include investigations of the various front-end ASICs configurations (ie: correlation window offset), efficiency studies of the interchip region to validate the chip lateral communication, efficiency studies at the center of the sensor where the split between the two independent hybrids occurs, and a reiteration of all the aforementioned studies for irradiated PS prototype modules.

In summary, with the approaching production phase, the Outer Tracker group is on the verge of entering a decisive chapter of the project. However, through all the various developments and contributions, the commitment and collaborative effort deployed in the context of this thesis, the path was further paved towards success. Nevertheless, I believe that an endeavour as big as building a Tracker will rely on three key aspects: creativity, communication and commitment.

ACRONYMS

μ DTC	micro Data Trigger & Control. 87, 95, 97, 99, 105, 107–109, 111, 116, 117, 122, 123, 160, 174
μ TCA	micro Telecommunications Computing Architecture. 95, 96, 98, 174
2S	Strip-Strip. 43–47, 49, 50, 85, 87, 93, 174
ADC	Analogue Digital Converter. 67, 90–92, 118, 123, 174
ALICE	A Large Ion Collider Experiment. 6, 174
AMC	Advanced Mezzanine Card. 95, 96, 174
APD	Avalanche Photodiode. 13, 174
API	Application Programming Interface. 108–112, 174
ASIC	Application Specific Integrated Circuit. 46, 47, 55, 57, 61–64, 66, 68, 85, 92, 95, 97, 102, 115, 117, 174

ATLAS	A Toroidal LHC Apparatus. 4, 6, 8, 174
BOOSTER	Proton Sychrotron Booster. 5, 174
BPIX	Barrel Pixel. 11, 144, 148, 158, 174
bPOL	buck Point-Of-Load. 55, 57, 68, 123–125, 174
BU	Builder Unit. 17, 19, 174
CBC	CMS Binary Chip. 102, 174
CCE	Charge Collection Efficiency. 33, 34, 174
CERN	European Organisation for Nuclear Research. 4, 5, 51, 52, 55, 66, 68, 114, 174
CFRP	Carbon Fiber Reinforced Polymer. 55, 63, 66, 68, 69, 73, 75, 76, 78, 79, 174
CIC	Concenrator Integrated Circuit. 55, 59, 62, 63, 65, 66, 68, 90, 91, 102, 109, 115–117, 119, 120, 122, 126, 132, 133, 174
CLB	Configurable Logic Block. 95, 96, 105, 174
CLPS	CERN Low Power Signaling. 66, 174
CMS	Compact Muon Solenoid. 4, 6, 8–10, 13–19, 21–23, 40, 41, 43–46, 51, 55, 56, 87, 108, 144, 148, 169, 174
CoG	Center of Gravity. 38, 39, 174
CPU	Central Processing Unit. 18, 52, 174
CSA	Charge Sensitive Amplifier. 34, 174

CSC	Cathod Strip Chamber. 15, 16, 174
CTE	Coefficient of Thermal Expansion. 69, 174
Cz	Czochralski. 32, 174
DAC	Digital Analogue Conversion. 133, 174
DAQ	Data Acquisition. 16–19, 51, 52, 87, 96, 161, 174
DDR3	Double Data Rate 3. 97, 105, 106, 174
DT	Drift Tube chamber. 15, 16, 174
DTB	Digital Test Board. 144, 149, 174
DTC	Data Trigger & Control. 51–53, 87, 98, 174
DUT	Device Under Test. 141, 143, 144, 153, 158, 159, 163, 174
EB	ECAL Barrel. 12, 174
ECAL	Electromagnetic Calorimeter. 12, 13, 18, 174
EE	ECAL Endcap. 12, 13, 174
ES	ECAL Preshower. 12, 13, 174
ESD	Electrostatic Discharge. 77, 174
FE	Front-End. 34, 174
FEH	Front-End Hybrid. 46, 55, 59, 60, 63, 65, 66, 70, 73, 82, 89, 90, 100, 108, 127, 160, 174
FF	Flip-Flop. 95, 105, 107, 174

FMC	FPGA Mezzanine Card. 95–97, 99, 174
FPGA	Field Programmable Gate Array. 18, 51–53, 87, 95–97, 99, 102–105, 116, 144, 174
FPIX	Forward Pixel. 11, 174
FU	Filter Unit. 17, 18, 174
FWHM	Full Width Half Maximum. 26, 174
FZ	Float Zone. 31, 174
GBL	General Broken Lines. 40, 155, 163, 174
GEM	Gas Electron Multiplier. 15, 16, 174
GND	Ground. 127–129, 138, 174
GPIO	General Purpose Input Output. 67, 123, 174
GTP	Global Trigger Processor. 19, 174
GUI	Graphical User Interface. 77, 78, 112, 114, 146, 174
HB	HCAL Barrel. 13, 14, 174
HCAL	Hadronic Calorimeter. 13, 14, 18, 174
HDMI	High Definition Multimedia Interface. 145, 174
HDR	High Dynamic Range. 87–89, 97, 116, 174
HE	HCAL Endcap. 13, 14, 174
HF	HCAL Forward. 13, 14, 174

HGCAL	High Granularity Calorimeter. 21, 174
HIP	High Ionizing Particles. 64, 174
HL-LHC	High Luminosity LHC. 19–21, 41, 43, 174
HLT	High Level Trigger. 16, 18, 174
HO	HCAL Outer. 13, 14, 174
HPC	High Pin Count. 96, 174
HPD	Hybrid Photo Detector. 14, 174
HV	High Voltage. 69, 70, 76, 82, 90, 138, 174
IPC	Inter Process Communication. 112, 174
IT	Inner Tracker. 43, 47, 174
L1A	Level-1 Accept. 16, 18, 149, 174
L1T	Level-1 Trigger. 16, 18, 43, 45, 174
LDD	Laser Diode Driver. 68, 174
LDO	Low Dropout. 90, 91, 174
LEIR	Large Energy Ion Ring. 6, 174
LEP	Large Electron Positron. 4, 174
LGAD	Low Gain Avalanche Diode. 21, 174
LHC	Large Hadron Collider. 4–9, 16, 19, 20, 24, 36, 99, 159, 160, 174

LHCb	Large Hadron Collider beauty. 6, 174
LINAC3	Linear Accelerator 3. 6, 174
LINAC4	Linear Accelerator 4. 5, 174
LPC	Low Pin Count. 87, 96, 174
lpGBT	low-power Gigabit Transceiver. 55, 57, 59, 65–68, 87, 91, 92, 100–104, 109, 117–123, 126, 131, 132, 174
LUT	Look-Up Table. 95, 105, 107, 174
LVDS	Low Voltage Differential Signaling. 87, 88, 90, 91, 174
MaPSA	Macro Pixel Sub-Assembly. 55, 59–61, 69, 73–75, 78–80, 82, 102, 113, 125, 137, 139, 174
MCz	Magnetic Czochralski. 32, 174
MGT	Multi-Gigabit Transceiver. 95, 96, 174
MIP	Minimum Ionizing Particle. 21, 25, 64, 135, 174
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor. 123, 174
MPA	Macro Pixel ASIC. 55, 59, 61–66, 68, 74, 82, 90, 100, 102, 109, 116, 117, 126, 132–137, 139, 150, 151, 153, 160, 161, 163–167, 169, 170, 174
MPO	Multi-fiber Push On. 91, 92, 174
MPV	Most Probable Value. 26, 138, 174
MTD	MIP Timing Detector. 21, 174

MTF	Muon Track Finder. 18, 174
MUX	Multiplexer. 107, 174
NI	National Instruments. 149, 174
OT	Outer Tracker. 43, 109, 174
PD	Photodiode. 68, 174
Ph2ACF	Phase 2 Acquisition and Control Framework. 87, 95, 108–112, 114, 118, 125, 126, 174
PIAL	Physical Interface Abstraction Layer. 98, 102, 104, 106, 107, 116, 174
POH	Power Hybrid. 47, 55, 57, 68, 73, 82, 90, 92, 107, 125, 127–129, 138, 149, 174
PS	Pixel-Strip. 22, 43–50, 53, 55–61, 63, 66, 68–71, 73–76, 78, 80–83, 85, 87, 89–93, 100, 104, 105, 107, 108, 112–116, 118, 119, 122, 124–131, 137–141, 144–153, 155–160, 162–165, 167–171, 174
PSI46	Paul Scherrer Institut 46. 11, 174
PTS	Punch Through Structure. 59, 167, 174
QC	Quality Control. 85, 174
QCD	Quantum Chromodynamics. 1, 174
QED	Quantum Electrodynamics. 3, 174
QFT	Quantum Field Theory. 1, 174
RAM	Random Access Memory. 96, 107, 108, 174

RBN	Readout Building Network. 18, 174
RCMS	Run Control and Monitoring System. 17, 19, 174
ROH	Readout Hybrid. 47, 55, 57, 60, 66, 67, 73, 82, 83, 90–92, 108, 114, 118, 122, 127–129, 174
RPC	Resistive Plate Chamber. 15, 16, 174
RU	Reader Unit. 17–19, 174
SCR	Space Charge Region. 30, 31, 174
SEH	Service Hybrid. 46, 174
SFP+	Small Form-factor Pluggable Plus. 104, 174
SiPM	Silicon Photomultiplier. 14, 21, 174
SLVS	Scalable Low Voltage Signaling. 62–65, 90, 91, 116, 174
SM	Standard Model. 1, 2, 4, 174
SPI	Serial Peripheral Interface. 91, 174
SPS	Super Proton Synchrotron. 5, 174
SSA	Short Strip ASIC. 55, 59, 62–64, 66, 68, 74, 82, 90, 91, 100, 102, 109, 115–118, 126, 133–137, 139, 150, 151, 153, 160, 163–167, 169, 170, 174
TB2S	Tracker Barrel Strip-Strip. 47, 49, 174
TBPS	Tracker Barrel Pixel-Strip. 47, 48, 74, 171, 174

TCA	Telecommunications Computing Architecture. 99, 174, 190
TDC	Time Digital Converter. 160, 164, 174
TEC	Tracker Endcaps. 11, 174
TEDD	Tracker Endcap Double Discs. 47, 49, 50, 71, 74, 113, 174
TF	Track Finder. 51, 52, 174
TFP	Track Finding Processor. 53, 174
ThDAC	Threshold Digital Analogue Conversion. 133, 134, 137, 139, 140, 163–167, 169, 170, 174
TIA	Transimpedance Amplifier. 68, 174
TIB	Tracker Inner Barrel. 11, 174
TID	Tracker Inner Disks. 11, 174
TLU	Trigger Logic Unit. 144–146, 149, 150, 174
TOB	Tracker Outer Barrel. 11, 174
ToF	Time of Flight. 21, 174
USB	Universal Serial Bus. 76, 91, 93, 144, 174
VCSEL	Vertical-Cavity Surface-Emitting Lasers. 68, 174
VTRx+	Versatile Link Transceiver Plus. 55, 57, 66–68, 83, 118, 121, 122, 126, 130, 131, 174
WLF	Wavelength Shifter Tube. 14, 174

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