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## **PhD Thesis**

### **COMPLEX INTEGRATED CIRCUITS IN THE RADIATION ENVIRONMENT AT THE LHCb HIGH ENERGY PHYSICS EXPERIMENT AND EXTRAPOLATION TO THE CASE OF SPACE-BASED EXPERIMENTS**

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# Abstract

The work presented in this thesis was done in the context of the Phase Ia upgrade program of the LHCb-RICH subdetectors from CERN. During the second Large Hadron Collider (LHC) long shutdown, which is foreseen for 2019 - 2020, the LHCb detector is upgraded to carry out data readout at higher speeds, synchronously with the LHC bunch crossing rate of 40 MHz. This involves a complete redesign of the LHCb readout architecture as well as its sub-detector electronics. The LHCb-RICH on-detector electronics will embed new sensors, multi-anode photomultiplier tubes (MaPMTs) and new front-end electronics with radiation hard ASICs - the CLARO integrated circuits. The MaPMT analog signals read by the CLARO and converted in to digital triggers will be fed into commercial-grade SRAM-based Field Programable Gate Arrays (FPGAs). The latter have an antifuse FPGA technology as a backup solution. Due to the fact, that these types of FPGA are known to be susceptible to radiation-induced failures, it is imperious to test these devices in equivalent radiation environments before they are used in their target application. Hence, an intense campaign was organized in order to test and qualify these devices in a radiation environment using beams with different particles species: mixed fields (high neutron and hadron fluence), protons, ions and X-rays. The FPGAs can malfunction in various ways when are used in radiation environments. Some failures are pure software either within the configuration memory and/or in the user design circuitry and they manifest as bit-flips that may affect the overall functionality of the device. Pure hardware failures are more difficult to mitigate and they manifest as either induced high current states in the FPGA, where sometimes an increased current consumption through ionizing radiation. Dedicated experimental setups for each of the tested FPGAs, were designed to ensure a proper testing and to fully evaluate the radiation response. To help with the reduction of the error rates, several mitigation techniques were employed and their efficiencies were measured. The entire preparation process for radiation testing as well as the results and the extrapolation of the results to the LHCb-RICH case are presented exhaustively in this thesis.

Besides the FPGAs, the SPACIROC2 - a dedicated Application Specific Integrated Circuit (ASIC) for space applications and other High Energy Physics experiments (HEP) - was tested in different particle beams to establish its radiation tolerance limits. As in case of the FPGAs, a complete dedicated experimental setup was designed for the radiation testing of the SPACIROC2 ASIC. The radiation testing results are presented in this thesis.





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Respectfully,  
Vlad-Mihai PLACINTA

A handwritten signature in purple ink, appearing to read 'VMA', with a stylized flourish extending from the end.

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# List of abbreviations

ADC – Analog-to-Digital Converter

ALICE – A Large Ion Collider

Ar – Argon

ASCII – American Standard Code for Information Interchange

ASIC – Application Specific Integrated Circuit

ATLAS – A Toroidal LHC Apparatus

AWAKE – Advanced WAKEfield Experiment

AWG – Arbitrary Waveform Generator

B – Particle containing Bottom Quark

BiCMOS – Bipolar Complementary MOSFET

BJT – Bipolar Junction Transistor

BRAM – Block RAM

C-Cell – Combinational Cell

CERN – European Organization for Nuclear Research

CHARM – CERN High Energy Accelerator Mixed Field Facility

CL – Confidence Level

CLARO – A Radiation-Hard ASIC Designed for High Rate Photon Counting

CME – Coronal Mass Ejections

CMS – Compact Muon Solenoid  
CMOS – Complementary MOSFET  
CRC – Cyclic Redundancy Check  
CO<sub>2</sub> – Carbon Dioxide  
COMPASS – Common Muon and Proton Apparatus for Structure and Spectroscopy  
COTS – Commercial-of-the Shelf  
CP – Charged Particle  
CRAM – Configuration RAM  
DAC – Digital-to-Analog Converter  
DAQ – Data Acquisition  
DCS – Detector Control System  
DD – Displacement damage  
DSP – Digital Signal Processing  
DUT – Device Under Test  
EC-H – Elementary Cell type H  
EC-R – Elementary Cell type R  
ECC – Error Checking and Correction  
ECS – Experiment Control System  
FE – Front-end  
FF – Flip-Flop  
FPGA – Field Programmable Gate Array  
FSM – Finite State Machine  
FSU – Fast Shaper Unipolar  
GBTx – Gigabit Transceiver  
GBT-SCA – GigaBit Transceiver – Slow Control Adapter  
GCR – Galactic Cosmic Rays  
GND – Ground  
GPIO – General-purpose Input/Output  
GUI – Graphical User Interface

H – Hydrogen Atoms

HEP – High Energy Physics

HfO<sub>2</sub> – Hafnium Dioxide

HBT – Heterojunction Bipolar Transistor

HKMG – High K Metal Gate

HL-LHC – High Luminosity Large Hadron Collider

HLT – High Level Trigger

HP – High Performance

HR – High Range

HPD – Hybrid Photodetector

I2C – Inter Integrated Circuit

ICAP – Internal Configuration Access Port

IRRAD – The CERN Proton Irradiation Facility

ISS – International Space Station

IT – Inner Tracker

JEM-EUSO – Joint Experiment Missions for Extreme Universe Space Observatory

JTAG – Joint Test Action Group

K – Kaon

L0 – Level 0

L1 – Level 1

LEIR – Low Energy Ion Ring

LET – Linear Energy Transfer

LHC – Large Hadron Collider

LHCb – Large Hadron Collider beauty

Linac – Linear accelerator

LUT – Look-up Table

LVDS – Low Voltage Differential Signaling

LS2 – Long Shutdown 2

MaPMT – Multi-Anode Photomultiplier Tube

MAROC3 – Multi-Anode ReadOut Chip

MBU – Multi Bit Upset

NA61/SHINE – SPS Heavy Ion and Neutrino Experiment

NA62 – NA62 Experiment

NIEL – Non-Ionizing Energy Loss

NMOS – N-channel MOSFET

NP – New Physics

O – Oxygen Atoms

OT – Outer Tracker

PCB – Printed Circuit Board

PDM – Photodetection Module

PDMD-B-H – Photodetection Module Digital Board Type H

PDMD-B-R – Photodetection Module Digital Board Type R

PMOS – P-channel MOSFET

PS – Proton Synchrotron

PSB – Proton Synchrotron Booster

QCD – Quantum chromodynamics

QE – Quantum Efficiency

R-Cell – Register Cell

RAM – Random Access Memory

RHBD – Radiation Hard by Design

RTD – Resistance Temperature Detectors

SAA – South Atlantic Anomaly

SCR – Silicon Controlled Rectifier

SE – Single Ended

SECCDED – Single Error Correction Double Error Detection

SEE – Single Event Effects

SEL – Single Event Latch-up

SEP – Solar Energetic Particle

SBU – Single Bit Upset

SES – Single Event Snapback

SEU – Single Event Upset

Si – Silicon

SiGe – Silicon Germanium Technology

SiO<sub>2</sub> – Silicon Dioxide

SM – Standard Model

SNR – Signal to Noise Ratio

SPACIROC – Spatial Photomultiplier Array Counting and Integrating Readout Chip

SPI – Serial Peripheral Interface

SPS – Super Proton Synchrotron

SRAM – Static Random-Access Memory

ST– Silicon Tracker

STI – Shallow Trench Isolation

S-TFC – Super Timing and Fast Control

TAP – Test Access Port

TCP/IP – Transmission Control Protocol/Internet Protocol

TID – Total Ionizing dose

TT – Tracker Trigger/Tracker Turicensis

TSMC – Taiwan Semiconductor Manufacturing Company

UART – Universal Asynchronous Receiver-Transmitter

UHECR – Ultra-High Energy Cosmic Rays

VELO – Vertex Locator

VFS – Very Fast Shaper

$V_g$  – Gate Voltage

VHDCI – Very High Density Cable Interconnect

VTRX – Versatile Transceiver

VTTX – Versatile Twin Transmitter

WWW – World Wide Web

# Chapter 1

## Introduction

Ground nuclear engineering, accelerator experiments as well as aero-space experiments are continuously demanding very reliable and cutting-edge technologies. These experiments are operating in harsh environments with a broad range of ionizing and non-ionizing radiation among other sources of perturbation like: high magnetic fields and large temperature fluctuations.

The first radiation effects in electronic devices were observed while the nuclear bomb was tested, causing various anomalies and malfunctions of the nearby equipment [1]. They appear following the interaction of radiation with the semiconductor layers of an electronic device as a result of either one of the two mechanisms: ionization or atomic displacement [2]. The study of radiation effects in electronic devices for various radiation environments [3] is a very broad and intensely studied topic in the modern science.

Many research groups [4]–[8] are designing, testing and qualifying custom integrated circuits, ASICs, to optimize them for their experiments and to harden them in order to operate in radiation environments. However, the costs and the time needed to design and qualify such integrated circuits are large to enormous, and for small experiments this is not a viable solution. For decades, people are investigating and testing various commercial-off-the-shelf (COTS) components in radiation environments to gauge the device reliability in their end-applications, instead of using a custom radiation hardened by design (RHBD) circuit especially due to the cost issues. In spite of their smaller price, the commercial-grade devices are designed for use in consumer electronics, and sometimes in high performance ground applications, leaving their radiation hardness under question. Such devices, if considered to be used out of their safe operating environments, have to operate with very low or negligible error rates. Therefore, there is a huge interest in testing and qualifying device radiation hardness as well as designing and implementing error-mitigation techniques for commercial-grade semiconductor devices when used in such environments. Radiation environments where the electronic devices may experience radiation damage are: high-energy physics and accelerator experiments [9], nuclear

power plants [10], space [11], atmospheric [12] and unusual terrestrial natural [13] environments. In this thesis the testing methodology as well as the results of radiation testing of three complex integrated circuits proposed to operate in high energy physics and space experiments will be presented.

*Experiments operating in space environments* [14] can be affected by various cosmic particles that includes protons, X-rays/gamma-rays, electrons, and heavy ions. There are two main sources of space radiation which can cause electronics to fail: particles trapped by planetary magnetospheres in so-called belts and transient radiation. Transient radiation is mainly either due to solar events [15] such as flares and coronal mass ejections (CME) [16] or galactic cosmic ray particles (GCR) [17]. The solar events produce alpha particles, electrons, energetic protons and heavy ions, which are orders of magnitude higher than the GCR fluxes.

Radiation belts may be present around any planetary body that has its magnetosphere strong enough to be able to capture particles before they can enter the atmosphere. Usually their type consists of particles from the solar winds and the low-energy GCRs. Toroidal shaped and concentrated regions of trapped electrons and protons by the Earth's magnetic field were first seen by Van Allen's team in 1958, hence the name of Van Allen Belts [18]. There are two categories of belts which are present around Earth: inner and outer belts. The inner belt which ranges from 1200 km to 6000 km altitude is populated with protons with energies of  $\sim 10$  MeV and electrons with energies between 1 MeV and 5 MeV [19]. On the other hand, the outer belt present at an altitude between 13000 km and 60000 km has a majority population made of electrons with energies between 10 MeV and 100 MeV [19]. However, the outer belt particle population is strongly influenced by the solar activity. Due to the fact, that the Earth's magnetic field is tilted by 11 degrees with respect to its rotation axis, this induces some asymmetries of the inner radiation belt alignment with respect to the Earth surface. These are translated in reductions of the inner belt altitude to 200-800 km in specific locations on Earth. The South Atlantic Anomaly (SAA) [20] is a such localized region and is located over the South America in the vicinity of the coast of Brazil being spread over a larger part of South America. This means that the particle fluxes in the SAA are significantly higher than in other places of Earth's orbit for the same altitude, but lower than at higher altitudes within the belt. However, orbital experiments and commercial satellites have to take into account when they are orbiting over the SAA, because it can generate serious problems with the reliability of their electronic systems.

Solar radiation is the most intense radiation flux in the solar system. It is produced via nuclear fusion, by converting hydrogen in to helium at the sun core, with the Sun emitting more than  $60 \text{ MW/m}^2$  [19]. Solar radiation can be due to either solar winds, solar flares or CMEs. Solar energetic particles (SEPs) [21], protons, electrons and heavy ions accelerated during CMEs-induced shock waves or solar flares are major concerns for space experiments. The fluxes can be much higher than usual during such events and particle maximum energy can be in the range of 1 GeV.

Cosmic rays like GCRs, are highly energetic particles that are originating usually outside of our solar system. They consist mostly of protons and have a low flux level of  $\sim 4$  protons/cm<sup>2</sup>/s but with a broad range of energies up to many GeV [22], with extreme galactic cosmic rays reaching  $10^{20}$  eV.



*High energy physics (HEP) experiments* such as those at CERN, arranged around the Large Hadron Collider (LHC) accelerator, rely on using reliable COTS components to operate and take valid collision data. The LHC radiation environment is very complex, with mixed radiation fields and very intense radiation level environment being caused by high energy particle collisions at 14 TeV and mostly neutron flux from the LHC beam itself. To have an idea on what to expect from the LHC radiation environment, various Monte Carlo simulations have been carried out using dedicated simulators like FLUKA [23]. Based on the simulation results, a complex radiation monitor has been designed to monitor the LHC radiation background, the RadMon system [24]. The electronics are exposed to high hadron fluxes with a broad range of energy spectra between a few meV up to hundreds of GeV [25]. Due to the fact that not all the electronics used in high energy physics experiments are RHBD, researchers have been investigating commercial-grade components in order to establish if they can be used in such LHC radiation-harsh environments [26].

The novelty of this PhD thesis stay in the irradiation campaign carried out to measure the radiation tolerance of one ASIC and 2 FPGA technologies, using custom experimental setups followed by a compressive data analysis. Each device and its experimental setup will be presented in detail. Advanced hardware design combined with various software programs, such as graphical user interfaces (GUI), were used to monitor, control and characterize the device under test (DUT) offline as well as during irradiation. The analysis, testing results, the extrapolation to a given radiation environment along with the conclusions are given at the end of each chapter, which is presenting the radiation campaign carried out for each DUT.

## 1.1 PhD Thesis Domain

The evolution of HEP experiments and their detection systems has taken the advantage of the technology advances in order to meet the requirements of high-energy particle collisions – LHC operates at large luminosity of  $10^{34}$  proton-proton pair per  $\text{cm}^2$  per second, and typical LHC-physics event having several thousand or reconstructed particles or more. Therefore, to engage in new research directions novel solid-state detectors had to be designed to allow a better reconstruction and identification of the particles resulting from collisions. To read out the data, the electronics have to operate flawlessly or with very low error rates. This involves state of the art systems, which have to be custom designed for their target application. With more luminosity accumulated during the runs, the more electronics and sensors are exposed to high radiation levels. These requirements pose design challenges on the electronics development as well as on the software programs intended to run in such harsh environments.

CERN's LHC accelerator [27] is the most advanced and powerful particle accelerator in the world on which 4 large experiments are searching for new physics and new states of matter by analyzing the data from particle collisions: ATLAS, ALICE, CMS and LHCb. Here, as a result of particle collision, the experiments are taking large amounts of data, while some of it is filtered with various trigger systems, and stored on the computer farms to be processed and analyzed.

In a similar way are the astrophysics/space experiments used to study among others the ultra-high energetic cosmic rays, e.g. JEM-EUSO mission [28] onboard at the ISS. However, besides the radiation environment, here it is also taken seriously into account the limited power budget and high temperature fluctuations.

The majority of experiments have a large ratio of their readout systems designed around commercial-grade electronic devices due to the limited financial budget. Therefore, there is a huge interest among researchers to test and qualify such commercial devices if these withstand various radiation levels, as well as to develop error-mitigation techniques to minimize the radiation impact in their systems.

Testing and qualifying commercial-grade electronic devices for use in radiation environments is a very complex task and involves knowledge of semiconductor physics, designing the data acquisition system to control and monitor the device under test, the analysis of the test data and the extrapolation of the results to a specific radiation environment – with uncertainty estimation and propagation.

Radiation hard by design devices designed for a specific target application are an ideal solution for the success of the experiment, however the R&D, the design together with the manufacturing process of the wafers are very expensive and a time-consuming process. Hence, the commercial-grade electronic devices are potentially viable solutions to be instead of RHBD device, due to their lower price and accessibility.

## 1.2 PhD Thesis Purpose

Following the second long shutdown (LS2), during 2019 - 2020, of the LHC accelerator the LHCb detector [29] will be upgraded and redesigned to work with a higher luminosity and to read out data 30 - 40 times faster than its previous detector, in the so called LHCb Upgrade phase Ia [30]. The LHCb entire electronics system is designed to withstand higher radiation levels while fulfilling the new operational requirements.

This PhD thesis is focused on reliability testing and investigation of radiation effects in 3 complex electronic devices: an ASIC and 2 FPGAs. Various irradiation tests with different particle beams and testing procedures for each device under test are presented in this thesis as well as the data analysis, testing results and the conclusions.

The ASIC, namely SPACIROC2, is a front-end ASIC proposed to read out MaPMTs in the JEM-EUSO mission. This ASIC has a very similar architecture with the MAROC3 ASIC and was proposed to be the back-up solution of the front-end ASIC in the LHCb RICH sub-detectors. Several irradiation tests were carried out using protons, ions and X-Ray beams in various scenarios and by monitoring a large number of parameters. Due to close connection of MAROC3, CLARO and SPACIROC2 ASICs design, it was investigated and estimated the SPACIROC2 reliability in LHCb radiation environment, as a possible choice for Ia, Ib and second (II) LHCb Upgrade phases – the device could be used in various systems from calorimeters to RICH systems.

The first tested FPGA is an SRAM-based device from Xilinx KINTEX-7 family that was chosen to be used in the digital readout system of the LHCb-RICH sub-detectors. Since this

device is a commercial device, a very intensive irradiation campaign was organized to test the reliability of this device in a given radiation environment with the results extrapolated to the LHCb-RICH environment. Since it is a very complex device, it was used different firmware versions to tests its specific resources, along with a custom data acquisition system, which was designed to power, monitor and control the device before, during and after the irradiation runs.

The other FPGA which was tested is an antifuse device from Axcelerator family being manufactured by Microsemi (now Microchip). This device was considered as a back-up solution for the KINTEX-7 device for use in the LHCb-RICH sub-detectors. However, due to its excellent radiation resilience this device is considered a viable solution for the future LHCb Upgrade, Upgrade phase II [31], as higher radiation levels are expected as a consequence of an increase in the total integrated luminosity during operation.

The only way to establish the radiation tolerance of electronic devices in such environments is by exposing them to radiation, like an accelerated particle beam (e.g. protons, ions, X-Rays) and monitoring their response before, during and after the irradiation procedure. Then, based on the data that was collected, the device response to radiation can be established, and, further its most probable or limiting behavior in LHCb-RICH environment can be computed/extrapolated.

The entire experimental setups involving the hardware and data acquisition systems, the irradiation tests and the data analysis as well as several error-mitigation techniques are extensively described in this thesis for each device which was tested. Furthermore, based on the results and the extrapolations, the device reliability in the LHCb-RICH environment is presented and conclusions are reached.

## 1.3 PhD Thesis Content

This PhD thesis is structured in 6 chapters and are described below briefly in the following paragraphs.

First chapter provides to the reader the purpose and motivation of this work along with an introduction to the harsh environments with radiation background and specially concentrated to the high energy physics experiments from CERN. Moreover, the LHCb experiment and its RICH subdetectors are presented as well as the LHCb upgrade program phase Ia.

The second chapter describes the radiation interaction with matter and provides a better understanding of how the radiation may cause failures into the electronics devices. The radiation effects are classified as either hardware or software and each of them are explained in detail along with their mechanisms of appearance. Several error-mitigation techniques are presented as well as how to analyze and extrapolate the data resulted from the irradiation tests.

The third chapter presents the radiation testing of the SPACIROC2 device with different particle beam: protons, ions and X-Rays. The data acquisition system, and the testing procedures are largely described in this chapter. Testing results and the conclusions are given at the end of the chapter.

The fourth chapter presents the radiation testing of the SRAM-based FPGA from KINTEX-7 family with different particle beam: protons, ions, X-Rays and mixed fields. The testing

routines, the data acquisition system and the setup, and the firmware versions are described in detail. Conclusions are reached based on the irradiation results and extrapolated to the LHCb-RICH environment.

The fifth chapter presents the radiation testing of the Axcelerator antifuse FPGA with proton and X-ray particle beams. The test bench along with its data acquisition system and the testing procedure are described in this chapter. Based on the results, conclusions are reached and the extrapolation is done for the LHCb-RICH environment. Also, a parametrization of the TID-induced increase of its leakage current using a mathematical model is presented.

The last chapter provides the overall conclusions of the test beam results, the original contributions as well as the conference/workshop/school participations and the scientific papers published by the author and which are relevant to this PhD thesis. The plans for future are also outlined following the next phase of the LHCb Upgrade, the phase II beyond 2030, for which the LHCb R&D have started since 2017.

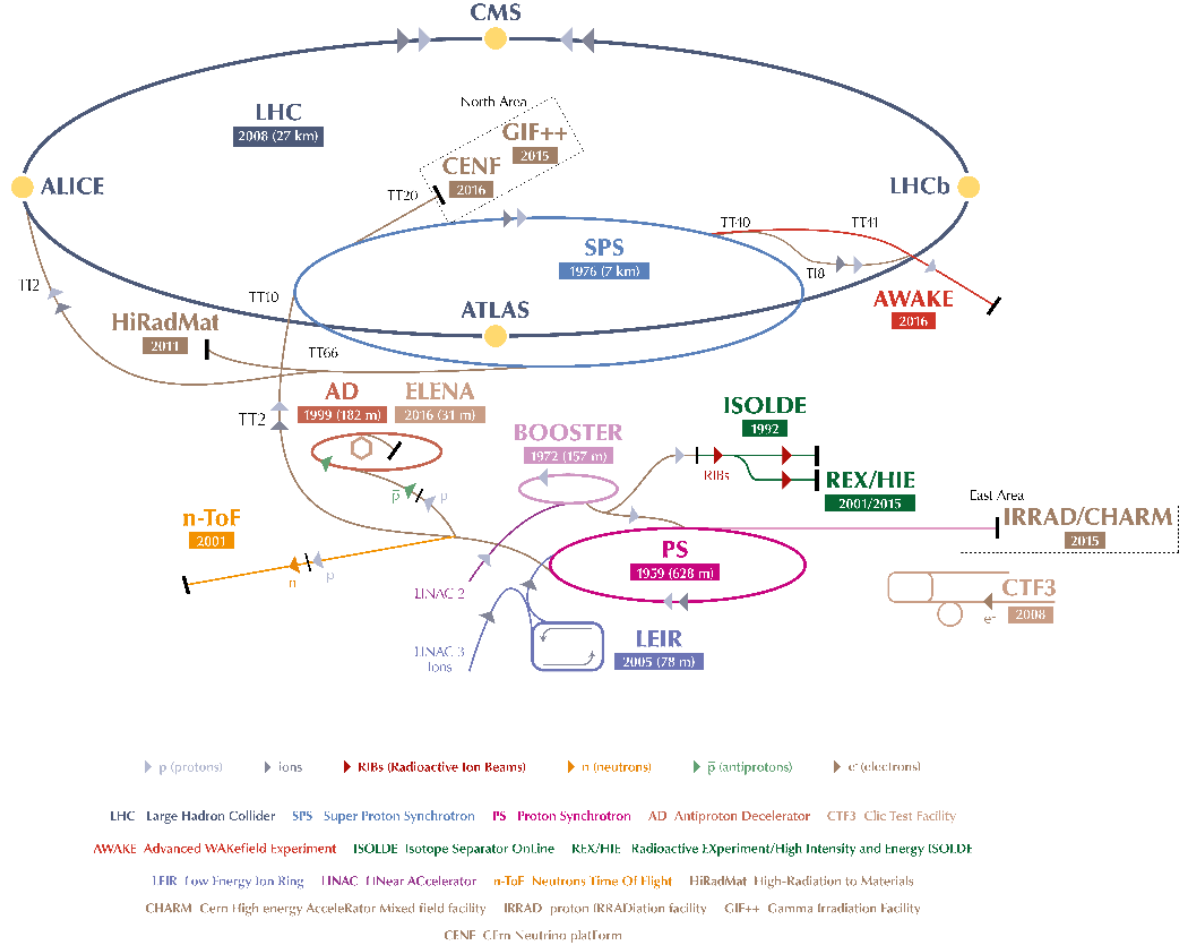
## 1.4 CERN and Its Accelerator Complex

CERN is the acronym for European Organization for Nuclear Research and is the biggest research center in particle physics and nuclear engineering in the world. Being located in the vicinity of Geneva city, the CERN campus is spread across the borders between France and Switzerland. It has been officially founded in 1953 initially with 12 member states, and now has 23 member states including Romania [32]. Its research topics covers both engineering and physics.

Various technologies have been invented at CERN during the past decades from which people are benefiting nowadays: the word wide internet (WWW) [33], capacitive touch screen [34], and one of the most recent is the Medipix3 ASIC [35] used to drive the first color X-Ray machine [36].

Under the CERN campus is hidden its accelerator complex, see fig. 1.1, one of the most impressive engineering constructions in the world. It is used to accelerate particles up to a certain kinetic energy and then they are collided inside various detectors to search for new physics and understand better the matter, as well as other exotic physics topics.

It's all starting with a canister of hydrogen gas, from where hydrogen atoms are stripped of their electrons to produce protons by using an electric field. The first starting point for the protons is the linear accelerator 2 (Linac 2) [37]. This type of accelerators is using radiofrequency cavities [38] with charge in several cylindrical conductors. In this way, the protons are passing through the empty space of such conductors, which are alternately charged either positive or negative. This is causing the particles to accelerate up to a certain energy. When the particles have reached the end of the accelerator, they will have an energy of 50 MeV and a 5% higher mass (in lab frame).



**Fig. 1.1** CERN Accelerator Complex [39]

The beam of particles is then injected into the Proton Synchrotron Booster (PSB) [40]. This accelerator is composed of four superimposed synchrotron rings designed to receive the proton beam from Linac 2 at 50 MeV. At this stage, the protons are accelerated up to an energy of 1.4 GeV, and are prepared for injection in the Proton Synchrotron (PS) machine [41]. The PS is an important component in CERN accelerator chain having a circumference of 628 meters. With this machine the particle beam is accelerated up 25 GeV. Additionally, several exit points for tests and experiments are presented at this stage intended for testing and evaluation of various detector components (e.g. electronics, mechanics etc.) in a radiation environment: CHARM [42] and IRRAD [43] facilities.

To have a higher energy, up to 450 GeV, the particle beam is injected from PS into the Super Proton Synchrotron (SPS) machine [44]. The SPS is the second-largest accelerator from the accelerator chain and it has a circumference of approximately 7 kilometers. Several small experiments are getting beams from SPS beam pipes: NA61/SHINE [45], NA62 [46], COMPASS [47] and AWAKE [48]. However, its main purpose is to provide high energy particle beams to be injected in the LHC accelerator.

The LHC machine [27] is the largest accelerator from the accelerator chain and is used to further accelerate the particle beams from SPS up to a projected 7 TeV kinetic energy. With its circumference of 27 kilometers, the LHC has two beams with one running clockwise and the other one in the opposite direction. When the two beams have reached their maximum energy,

they are crossed for collision inside four detector caverns. The colliding protons in LHC experiments have a total energy of 13 TeV in the center of mass, with projected energy for RUN 3 of 13.5 – 14 TeV.

As in any other accelerator, in the LHC the particles are circulating in a vacuum environment and their direction is controlled with various types of electromagnets designed around NbTi superconductors. These are cooled down to 1.9 K (-271.3 °C).

The LHC cryogenics system is considered to be the most extreme cooling system from Earth. It takes around 120 tons of helium and 40 MW of power to cool down and keep the electromagnets at 1.9 K (about 1 degree lower than the intergalactic space, at 2.7 K).

Being the largest and most powerful accelerator from the world, the LHC has been designed to run at a  $10^{34} \text{ cm}^{-2}\text{s}^{-1}$  luminosity. The luminosity is an important parameter of an accelerator and multiplied by the quantum probability of an interaction between the protons (cross-sections) gives the number of collisions at the beam crossing point in a given amount of time for which the luminosity is defined. The instantaneous luminosity is given as per  $\text{cm}^2$  and per second. The maximum LHC beam intensity is dependent on the accelerator filling of 2808 particle bunches, with each of them running at a fraction of 0,999999991 % of the light speed. The LHC time interval between the bunches is 25 ns, hence LHC collisions have a frequency of 40 MHz. This frequency is intended to be used to synchronize the readout electronics inside the detectors.

Ion beams can be also accelerated in the CERN accelerator chain and collided inside the LHC detector caverns when it is required by the experiments. Lead ions are produced at the beginning of Linac 3 [49] and then are redirected to be accelerated in the Low Energy Ion Ring (LEIR) [50]. From LEIR, the lead particle beams are following the same path to reach the maximum energy as in the case of protons.

The CERN accelerator complex will have major upgrades in the next years starting with the replacement of Linac 2 by the Linac 4. The Linac 4 [51] is designed to boost negative ions of hydrogen to higher energies and is scheduled to be the source of proton beams after the LS2. The protons are obtained by stripping the ions of their two electrons during injection to PSB.

Another major upgrade is the upgrade program of the LHC, the so-called HL-LHC [52]. The upgrade will take place during LS3 and is scheduled to begin operation starting with 2027. Its luminosity will be increased by a factor of 10 of current LHC design parameters. During 2015-2018 the LHC experiments reached a total integrated luminosity of  $160 \text{ fb}^{-1}$  [53] and with the new HL-LHC it is expected to reach  $250 \text{ fb}^{-1}$  per year [52] for a 10-year period of operation. With more luminosity accumulated, more data is recorded allowing experiments to discover and observe rare processes in physics.

The accelerated particles are brought to collision in the caverns of four main detectors positioned on the LHC: ALICE, ATLAS, CMS and LHCb. A Large Ion Collider Experiment (ALICE) [54] describes a general-purpose and heavy-ion detector which is focused on quantum chromodynamics (QCD) studies [55]. A Toroidal LHC Apparatus (ATLAS) [56] and the Compact Muon Solenoid (CMS) [57] are dedicated particle physics experiments designed to perform experimental tests of Higgs mechanism [58] as well as supersymmetry searches [59]. The Large Hadron Collider beauty (LHCb) [29] is described in extenso in section 1.5.

## 1.5 The LHCb Experiment and Collaboration

### 1.5.1 Physics Objectives within LHCb Collaboration

The Standard Model (SM) [60] of particle physics represents a theory which is classifying all known elementary particles as well as the interactions of three out of four known fundamental forces in universe: the weak, the strong and the electromagnetic (and not the gravitational force). Its current state dates back to around mid-1970s from when it had an increased validation and gained addition complexity with the experimental discoveries of: quarks, top quarks (1995), the tau neutrino (2000) as well as the Higgs boson (2012). The SM includes several categories of elementary particles, which are differentiated by different characteristics – or quantum number – like their color charge, electrical charge, flavor, weak charge, lepton and baryon numbers, helicity/chirality, spin and parity. The color charge is a property related to the strong interaction of particles, whereas the weak and charge describe the strength of electro-weak interaction.

There are 2 main categories of elementary particles within the SM: fermions and bosons. The fermions are half-integer-spin particles classified by the way of how they interact. Every fermion has an associated antiparticle, which has the same mass, but with the opposite charge. Therefore, the fermions are subclassified in quarks and leptons with their associated antiparticles: antiquarks and antileptons. There are three generation of quarks with their antiquarks: up and down, charm and strange, and top and bottom. These are particles with color charge and participate in strong interactions. The phenomenon of color confinement bounds the quarks in hadrons, which can include either by three valence quarks defining the baryons or by a valence quark and its antiquark which is a system known as a meson. The protons and neutrons are the lightest baryons. The leptons are fermions which do not carry color charge and are composed from six particles: electron, electron neutrino, muon, muon neutrino, tau and tau neutrino. The electron, muon and tau are interacting electromagnetically and by weak force, while the three neutrinos interact only through weak force which makes them very difficult to be detected at GeV and MeV energies.

The bosons are defined as fully-integer-spin particles and subclassified in gauge and scalar bosons. The gauge bosons are seen as force carriers (or messenger particle) which are mediating the weak and strong nuclear as well as electromagnetic fundamental interactions between other particles. The gauge bosons are composed from photons, W and Z bosons, and eight types of gluons, all vector bosons. The Higgs boson is a massive scalar boson with no intrinsic spin introduced and theorized by Peter Higgs in 1964 [58]. It is a unique elementary particle which is required to explain why other elementary particle such as photons have no mass while others like the W and Z bosons are very massive. Due to the fact that the Higgs boson is itself a very massive elementary particle and it is decaying almost immediately after it was created. It can be observed only with a very-high energy particle accelerator due to the large mass (above 100 GeV) and the interaction modes of its decay state. In 2012 the ATLAS

and CMS experiments at the LHC commonly reported the discovery of the Higgs boson [61], [62].

Although the SM is the top among theories describing the particle physics, the SM is not complete [63] as physics is known only at scales reached by experimental observatories. Over the last decades, the theoretical physicists have proposed various forms of New Physics (NP) which are beyond the SM. There are several incompletely known aspects within the particle physics and cosmology which are not yet explained such as: gravity, dark matter, dark energy, neutrino mass, matter-antimatter asymmetry, etc. Therefore, several experiments have been built to search for various NP beyond the SM.

LHCb is a specialized b and c-physics experiment designed to carry indirect signals of NP by studying very rare decays of bottom (beauty) and charm quarks together with doing other precise SM measurements like precise CP-violation measurements. By doing such studies, it may help to also understand the matter-antimatter asymmetry in the Universe. Over the last decade, the validity of the SM was confirmed with precision measurements carried out at various B factories. However, the challenge of future b-experiments is to extend the range of measured decays and reach channels that are generally suppressed by the SM as well as to improve the required sensitivity to NP. Therefore, the LHCb will extend its b-physics studies to detect decays of heavier b hadrons, such as strange or charm, which will be produced by the LHC, and improve the precision for some key decay channels. In this way it will compete with the direct searches of the NP at the LHC, by measuring important parameters of the NP flavor structure with the help of a dedicated detector, special optimized for this kind of task. [64]

The LHC is the most generous source of  $b\bar{b}$  pairs, having a cross-section of  $\sim 500 \mu\text{b}$  at an energy of 14 TeV [29]. The dominant mechanism for  $b\bar{b}$  production at the LHC machine is via gluon fusion. Following this process, the center of mass energy of the newly produced  $b\bar{b}$  pair is boosted along the path of the gluon with the higher momentum, hence both newly b hadrons are produced in the same direction, either forward or backward. Therefore, the layout of the LHCb detector is designed as a single arm forward spectrometer with a pseudo-rapidity range of  $1.9 < \eta < 4.9$  [64]. Within this range, there is a high geometric efficiency to detect all decay particles corresponding to a b hadron and the decay particle from its accompanying b hadron is ensured.

The LHCb detector must be capable to exploit the high number of b-hadrons of  $(7 \text{ to } 8) \cdot 10^{12}$  b-hadrons (for Upgrade luminosity of  $50 \text{ fb}^{-1}$ ). By all means it requires a very efficient and flexible trigger system. The trigger system has to be able sense both hadronic and leptonic final states. A particle identification system is mandatory for hadron detection and separation as well as for flavor tagging needed for CP violation studies. In addition, very good vertex and momentum resolution are mandatory requirements for a good time resolution needed to carry out studies to the rapidly oscillating  $B_s$  and anti- $B_s$  meson system as well as to ensure a good mass resolution, which is required for the reduction of combinatorial background. In addition, a high-bandwidth data acquisition system is needed to optimize the data taking and to process the information.

During RUN 2 the LHCb luminosity was low compared with the LHC nominal luminosity of about  $10^{34} \text{ cm}^{-2}\text{s}^{-1}$ . Hence for a luminosity of about  $4 \cdot 10^{32} \text{ cm}^{-2}\text{s}^{-1}$  the expected  $b\bar{b}$  pairs number was of about  $2 \cdot 10^{12}$  in  $10^7 \text{ s}$ . The rate of events containing at least two particles of interest within LHCb acceptance is of about  $\sim 10 \text{ MHz}$ . Within these events, the rate of b quarks

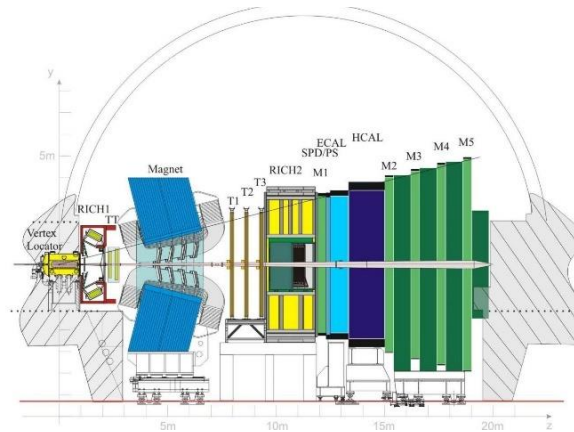


events was of about 100 kHz, while for  $c$  quarks events was much higher of about 600 kHz. However, the rate of events which are of interest for LHCb has a very low rate of a few kHz of that, ultimately, only a few are important in given analysis. Hence the need to have a very efficient and highly efficient trigger. A hardware trigger was employed to filter the candidate events to a rate of 1 MHz. Although, it leads to observation of many new insights in physics, many critical measurements were statistically limited due to the modest luminosity combined with a low trigger rate of about 1 MHz.

Starting with RUN 3, the LHCb experiment will run with an increased luminosity by a factor of five, of  $2 \cdot 10^{33} \text{ cm}^{-2}\text{s}^{-1}$ . All its sub-detectors will be upgraded to manage higher particle density by using novel sensors with finer granularity combined with new electronics readout chains. To meet the new requirements with the luminosity change, a new trigger system will be adopted. In this way the hardware trigger that imposed the reduction of the events to 1 MHz, will be removed and the full detector will be read out at the full LHC bunching rate of 40 MHz. By removing this limitation, the trigger efficiency of hadronic decays is expected to increase by a factor of 2 (with an overall gain of 10 for most key decay channels). The data will be fed to a software-based trigger system, allowing for more complex pattern recognition algorithms as well as more flexible decisions.

### 1.5.2 The LHCb Detector

The LHCb detector is a forward single-arm spectrometer which uses an array of sub-systems to detect particles that are produced and emitted in the forward direction as result of proton-proton or nucleus-nucleus collisions: the spectrometer magnet system, the tracking and particle identification sub-detectors, as well as the trigger and online systems. Its layout, shown in fig. 1.2, shows an angular coverage from between 10 mrad and 300 mrad in the bending plane, while a 10 - 250 mrad coverage is ensured for non-bending plane.



**Fig. 1.2** The general layout of the LHCb detector [29]

The spectrometer magnet system containing a dipole magnet is used to measure the momentum of charged particles, covering a forward acceptance of  $\pm 250$  mrad vertically and  $\pm 300$  mrad horizontally. Usually particles are travelling in straight lines, however the presence of a magnetic field causes the paths to curve, and positive and negative particles are moving in

opposite directions. It weighs 1800 tons (about 1600 tones the yoke and coils) and is generating a 3.6 Tm magnetic field to spread horizontally the charged particles.

The *LHCb tracking system* [65] contains a vertex locator system (VELO) together with two tracking detectors: the Outer Tracker (OT) and the Silicon Tracker (ST).

The VELO system [66] is used to perform precise measurements of track coordinates and is located close to interaction region. The measurements are used to identify displaced secondary vertices being a distinctive detail of b and c-hadron decays. Its system consists of a series of silicon microstrip [67] modules placed along the beam direction, with each of them providing measurements for  $r$  or  $\Phi$  coordinates of a particle.

The OT system [68] covers the T1-T3 stations, which are located downstream of the dipole magnet. It is a drift-time detector and is using straw-tube drift chambers [69] as detectors for tracking the charged particles and to measure their momentum over a large acceptance area. To guarantee a fast drift time, below 50 ns, a mixture of Ar (70%) and CO<sub>2</sub> (30%) is used as a counting gas. Also, it provides enough drift-coordinate resolution, of 200  $\mu\text{m}$ .

The ST system [70] is composed of boxes close to the beam-pipe in the T1-T3 stations called the Inner Tracker (IT) [71] and the Tracker Turicensis (TT) [53]. The TT is located upstream of the dipole. It is used to get a first estimate of the momentum, and it is also important for the trigger system. Being located downstream of the dipole magnet, the IT provides a coverage of 120 cm wide and 40 cm high cross shaped area in the center of the T1-T3 stations, close to the beam pipe. Both are using silicon microstrip sensors which gives an overall pitch of 200  $\mu\text{m}$ .

The *particle identification system* [29] is built up with two Ring Imaging Cherenkov sub-detectors (RICH), a calorimeter system and a muon detection system. Particle identification is a mandatory requirement for the LHCb experiment.

The main task of a calorimetry system [72] is to allow particle identification and to measure the electromagnetic, light lepton (electron and positron) and hadronic particle energies. It stops electromagnetic and hadronic particles as they pass through its detection layers, and in the same time the amount of energy is measured. In LHCb there are two main types of calorimeters used: electromagnetic and hadronic. The electromagnetic calorimeter is used to detect and measure the energy of electromagnetic and light lepton particles, such as electrons/positrons and photons. The other one is used to detect and measure the energy of multiple particles like: protons, neutrons and other particles containing quarks, i.e. hadrons.

The muon detection system [73] is a mandatory requirement for the LHCb experiment due to the fact that muons are present in the final stages of many b meson decays. Being located at the far end of the detector, the muon detection system is composed of five rectangular stations (M1-M5), mounted along the beam axis. It provides muon triggering and muon identification needed to trigger the data recording as well as particle identification to be used for offline analysis.

Two RICH sub-detectors [74] are providing particle identification over the full momentum range of 1-150 GeV/c, within 10-300 mrad angular acceptance. RICH 1 is placed upstream and it provides a coverage for the low momentum range of  $\sim 1$ -60 GeV/c, while the RICH 2 being placed downstream it covers the high momentum range of  $\sim 15$ -100 GeV/c. The RICH sub-detectors are described in section 1.5.3.

The LHCb trigger system [75] has a very important role in selecting true-signal events and rejecting uninteresting-tagged events as well as filtering the background noise. The architecture of the LHCb trigger system as of 2015-2018 is structured in a two-stage system: the level 0 trigger (L0) and high-level trigger (HLT). The role of the L0 trigger is to decrease the rate of observable interactions from 40 MHz down to 1 MHz, which is to be read out by the LHCb readout architecture. The HLT is also composed from two stages and being implemented in software it runs in about 29000 cores on the event filter farm. It is used mainly for partial and full event reconstruction including selection of signal candidates.

The online system [76] is in place to ensure the transfer of data from the sensors and their front-end electronics to permanent storage as well as to provide the infrastructure to operate the whole LHCb experiment. It is mainly responsible with the configuration and monitoring of all sub-detectors and sub-systems and to synchronize them with the LHC clock.

Due to limitations imposed by the L0 trigger stage by setting the maximum read out rate of 1 MHz to LHCb farm, the LHCb detector will be redesigned and upgraded to work at a 40 MHz readout rate. The first upgrade phase, Phase Ia, will take place during LS2, as shown in fig. 1.3, and its whole readout electronics will be based on a trigger-less architecture. In this way by using a software trigger, the online-farm event processing rate can be up to 40 MHz, as it is the LHC bunch rate.



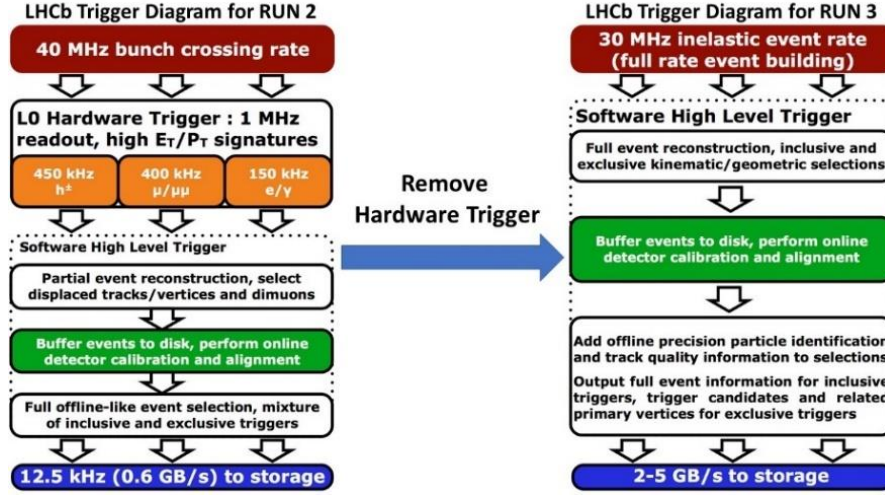
**Fig. 1.3** LHC and LHCb schedule

Every sub-detector will be redesigned to fulfill the 40 MHz LHCb readout rate (in conjunction with 5 times higher instantaneous luminosity) by including new sensors and front-end electronics. With more luminosity required for RUN 3, after the upgrade Phase Ia, the radiation environments in the vicinity of each sub-detector and sub-system are harsher, with 10 times increase in the expected fluxes and fluences. Hence, efforts have been made to design, test and qualify radiation-hard and radiation-tolerant sensors along with their front-end readout electronics.

The upgraded LHCb tracking system [77] will be compatible with higher data recording rate and faster readout speeds. This is done by a new Upstream Tracker (UT) [78] installed in the place of the former TT station upstream the dipole magnet. The T1-T3 stations located downstream will be replaced by a new scintillating fibre (SciFI) tracker [79].

The particle identification system will be also upgraded [80] to cope with the new requirements for 40 MHz readout rate. New readout electronics and sensors for muon detection [81] and the calorimeter [82] systems as well as for the RICH sub-detectors [83] are designed and qualified to be integrated in the upgraded LHCb readout. The new upgraded RICH sub-detectors are described in detail in section 1.5.3.

Due to the need to maximize the physics output of the LHCb experiment, a new high trigger architecture with higher signal efficiency was designed to fulfill the requirements for a full readout at 40 MHz and is prepared for RUN 3 [84]. This is done by the removal of the L0 trigger stage and the deployment of a software trigger, using also commercial-off-the-shelf hardware, as it can be seen in the diagrams presented in fig. 1.4. The data is acquired using trigger-less readout hardware architectures at a full rate of 40 MHz, hence the system will be able to reconstruct and temporary record events in every LHC bunch crossing [85].



**Fig. 1.4** The LHCb trigger diagram used for RUN 2 (left side) and the proposed diagram for RUN 3 (right side) [86]

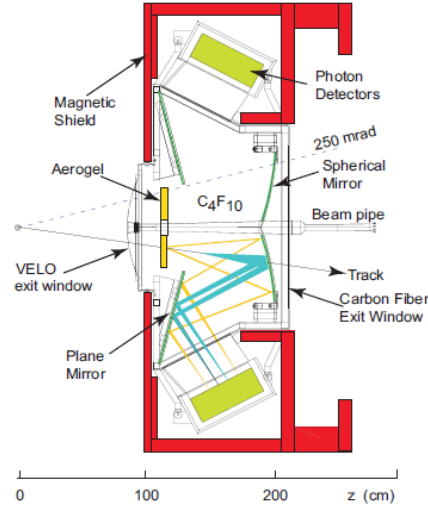
With the help of a new online system, data is sent from every sub-detector via optical links to the DAQ system for filtering, event-building and processing. After processing, the data is saved in dedicated storage facilities with a rate between 2 and 5 GB/s [87]. The new online system will accommodate also the control protocols and timing for all sub-detectors [88], [89].

### 1.5.3 The RICH Sub-Detectors Past and Future Architectures

The RICH sub-detectors [90] are a key component in the LHCb detector as part of the particle identification system. There are two RICH sub-detectors in the LHCb layout used to measure and detect Cherenkov radiation [91]. RICH 1 is placed upstream while RICH 2 is placed downstream with respect to the magnet position, see the fig. 1.3. The choice of their position in the layout is due to the need to cover the full momentum range as its spectra is softer at large polar angles and harder at small polar angles. Both RICH sub-detectors are focusing the Cherenkov light by using a configuration of flat and spherical mirrors to reflect the light out of spectrometer acceptance. To detect the Cherenkov photons in a wavelength range of 200-600 nm, Hybrid Photon Detectors (HPDs) are used [92].

*RICH 1* is in place to sense the charged particles with low momentum range  $\sim 1\text{-}60\text{ GeV}/c$  in a wide acceptance enough to ensure a full coverage of the LHCb acceptance of  $\pm 25\text{ mrad}$  to  $\pm 300\text{ mrad}$  horizontally and  $\pm 250\text{ mrad}$  vertically. This is ensured by using fluorobutane ( $\text{C}_4\text{F}_{10}$ ) as gas radiator. RICH 1 is located upstream of the magnet, being placed between VELO

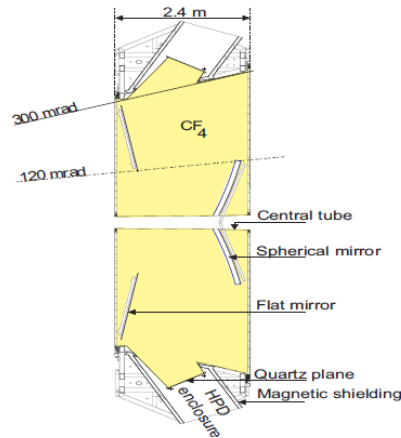
and the TT sub-detectors. Its optical layout is placed vertical with respect to the interaction point as shown in the schematic diagram from fig. 1.5.



**Fig. 1.5** RICH 1 schematic diagram [29]

The RICH 1 performances and parameters have been modeled with the help of various simulators. Charged particles trajectories, resulted from the interaction point are directed through RICH 1 radiators. The generation of Cherenkov photos is usually uniform following the track in the gas radiators. To be detected by the HPDs, the Cherenkov light is reflected and focalized with an optical system made with flat and spherical mirrors. On the top and bottom sides of the beam pipe there are two spherical mirrors made from carbon fiber reinforced polymer (CFRP) used to send and focus the photons resulted from the gas radiators to the plane mirrors. The flat mirrors placed vertically on both sides of the beam pipe redirect the focalized photons to the HPD plane and the photon signal events are recorded. This layout configuration was needed in order to avoid the loss of efficiency in HPDs due to high magnetic fields in the area. For this purpose, the HPD planes are shielded with magnetic shield boxes, to ensure a magnetic field less than 3 mT for good operation of the HPDs. The RICH 1 sub-detector has a total weight of 16 tons, mostly due to the magnetic shielding enclosures.

*RICH 2* sub-detector is located between the last tracking station, T3, and the first muon detection station, downstream of the magnet. Its layout schematic is presented in fig. 1.6. It contains a CF4 radiator and it provides particle identification with a coverage of momentum from 15 to  $\geq 100$  GeV/c in a low polar angular acceptance:  $\pm 120$  mrad horizontally and  $\pm 100$  mrad vertically. Being located at approximately 9.5 m from the interaction point, its structure is aligned vertically with the HPD planes placed on the left and right side of the beamline to fulfill some mechanical constrains. The photodetection system is similar with the one present in RICH 1 and the optics system is composed from 2 flat mirrors and 2 spherical mirrors. It has a total weight of 30 tons, with 12 tones only from the magnetic shield.



**Fig. 1.6** RICH 2 schematic diagram [29]

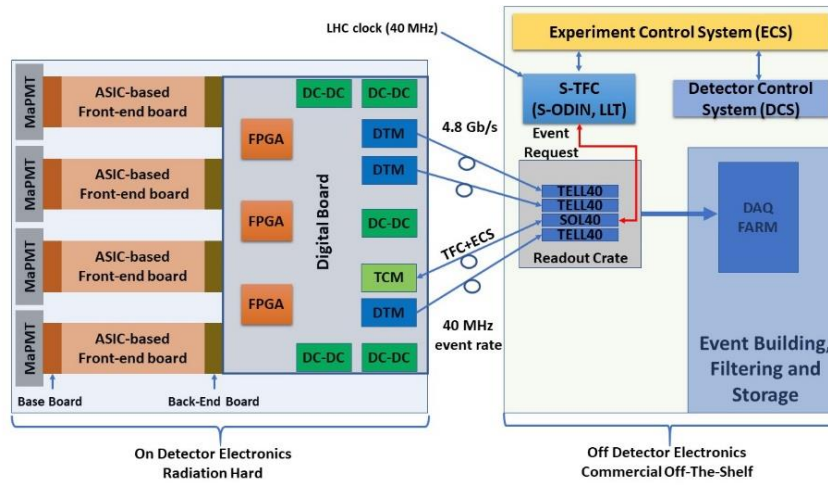
The *LHCb-RICH* photodetection system is made up with HPDs as photo detectors to collect and detect particle-emitted Cherenkov photons and to measure their spatial position for ring pattern recognition. The HPD is a vacuum photon detector developed by the LHCb in collaboration with industry. A Cherenkov photon excites the HPD photocathode and is converted in photoelectron which is accelerated by an applied high voltage field from 10 to 20 kV on a reverse-biased silicon detector. While the photoelectron energy is dissipated in the silicon wafer, electron-hole pairs are built with an average yield of one for each of 3.6 eV deposited energy. Well-designed readout hardware that interconnects to the HPD silicon detectors ensures very good efficiency for single photon detection.

To meet one of the most important RICH requirements in terms of high speed, 1 ns timing resolution (time alignment) and 25 ns readout clock to L0-trigger boards, an *LHCb-RICH* electronics system has been designed to read out the data from HPDs. The readout system is divided in two regions: Level-0 (L0) and Level-1 (L1). The L0 electronics are located near the HPD and are used to read out and synchronize the data from HPDs at a maximum rate of 40 MHz. The data from L0 is sent at 1 MHz rate to off-detector electronics, to the L1 electronics region, via optical data transmission links. The L1 electronics have been designed for data compression as well as protocol conversion to industry Gbit Ethernet protocol to be able to be interfaced with the DAQ network. Here, the data is processed and sent to the computer farm for storage.

Due to the need to operate faster, to get more data with higher granularity and efficiency, *new and upgraded LHCb-RICH sub-detectors* [93] are currently completely redesigned to cope with a new 40 MHz trigger-less readout architecture for RUN 3. The main concept remains the same for both RICH sub-detectors, but with major modifications to RICH 1 in terms of geometrical and optical arrangement. The RICH 1 will embed new mirrors as well as new the photon detectors. These are needed to widen the image area of the Cherenkov rings and implicitly to reduce the photon occupancy. Due to the fact that the HPDs have their readout embedded, the photon detectors are replaced with commercial multi-anode photomultiplier tubes – MaPMTs - with external readout hardware, due to their excellent capabilities into detecting single photons in the near UV spectrum as well as for low noise, fast time response and high pixel granularity.



A simplified new LHCb-RICH readout architecture is shown in fig. 1.7 and it comprises from two regions: on-detector and off-detector electronics. The on-detector region contains the MaPMTs, the front-end boards, digital boards, communication plugin adapters and interconnection boards. Since they need to operate in a harsh environment with radiation background, it is imperative to be radiation-hard or tolerant in the LHCb-RICH radiation environment. Meanwhile, the off-detector region contains commercial-grade electronics and is placed at a safe distance from the radiation levels behind a concrete shield wall or on surface. It is used to readout and control the RICH sub-detectors, to supervise the environment parameters and the cooling system, and to pre-process the data. It is mainly composed from the following systems: a readout crate, detector control system (DCS), experiment control system (ECS), timing and fast control system (S-TFC) and the online computing farm for event building, filtering and storage (DAQ farm).



**Fig. 1.7** LHCb-RICH readout architecture for RUN 3

The R13742, referred as R-type MaPMT in the following, are one square inch MaPMTs with 64 pixels arranged as  $8 \times 8$ , with a pixel size of  $\sim 3 \times 3 \text{ mm}^2$  from Hamamatsu selected to be used in RICH 1 and in the central region of RICH 2. Another type of MaPMT, R13743, also referred as H-type MaPMT in the following, will be used in the outer region of RICH 2 due to lower occupancy. The H-type is 4 square inch  $8 \times 8$  pixels MaPMT with a pixel size of  $\sim 6 \times 6 \text{ mm}^2$ . These MaPMTs are custom versions of the commercial Hamamatsu models R11265 [94] and H12700 [95] but with dedicated features and specifications.

The R-type and H-type MaPMTs have their entrance windows made of UV-glass which has a good transmittance in the UV spectrum. Their photocathodes are made of super-bialkali material which has the high quantum efficiency (QE) in the near UV spectrum. The QE is a very important parameter in the LHCb-RICH case as it describes the cathode photoemission. It is given in percentage and it relates to the ratio of the number of emitted photoelectrons to the number of photons transmitted through the MaPMT window.

When Cherenkov photons are transmitted through the UV-glass of the MaPMT the photocathode is excited and it releases photoelectrons. The photoelectrons are accelerated using an electric field and directed to the first dynode (electrode). Here it takes place the first stage of electron multiplication by secondary emission. This operation of electron

multiplication is repeated at each of the MaPMT dynodes, with the final charge being collected by the designated anode. The MaPMTs proposed to be used in the LHCb-RICH have a gain of  $10^6$  in normal operating conditions, hence for one Cherenkov photon transmitted through the window a charge of  $1 \text{ Me}^-$  is collected. The R-type MaPMT has 12-stage dynodes, while the H-type has 10-stage dynodes. Due to the fact that each of the MaPMTs have 64 independent pixels (channels), the gain can vary between every pixel as each of them have its own dynodes chain. The QE and the gain of each MaPMT may vary with the high voltage applied across the cathode, typically  $\sim 1000 \text{ V}$ , and this will require fine-tuning of the high voltage. Also, depending on the gain and the noise values, the MaPMTs will be mapped to fit in specific regions where similar gains are required. Both types of MaPMT have been intensively tested using various scenarios to be qualified as good to be used in the LHCb-RICH photodetection system [96], [97], [97]–[100].

The LHCb-RICH photodetection system [101] is made with about 3000 MaPMTs arranged in modules called Elementary Cells (ECs). Since there are two types of MaPMTs used, two types of EC are presented in the LHCb-RICH system: EC-R and EC-H.

Each EC-R is composed from four R13742 MaPMTs plugged in a baseboard that provides bias and connection of the anodes to the front-end (FE) boards. An EC-H type has only one R12743 MaPMT which is connected to a dedicated baseboard to be interfaced with the FE boards.

To read out the MaPMT analog signals, custom FE boards have been designed to carry out this task. The main component on the FE boards is the CLARO ASIC [102] which is a dedicated radiation-hard digitization chip, specially designed for the LHCb-RICH application. It has 8 channels and is designed in  $0.35 \mu\text{m}$  CMOS technology.

Each channel inside the CLARO ASIC has a charge sensitive input preamplifier followed by a fast discriminator. The discriminator is used to generate trigger signals when the MaPMT charge is higher than a given threshold which can be set by an embedded DAC. The ASIC is able process the next pulse with arrival in less than  $25 \text{ ns}$  as the next LHC bunches collide. Hence, this feature enables to do a full  $40 \text{ MHz}$  readout. Its power consumption is about  $1 \text{ mW}$  per channel, which make it excellent as there is no need to have a dedicated cooling system for the FE boards.

The CLARO can be configured to set different parameters of its internal blocks like: different gain values of the preamplifier and 64 DAC threshold values. These settings allow to tune the configuration in order to obtain the best signal to noise ratio (SNR) and detection uniformity. Each FE board hosts 8 CLAROs, which in fact means that each EC-R will have 4 FE boards, one for each R-type MaPMT, while the EC-H will embed only 2 FE boards, to read out one H-type MaPMT. The CLARO ASIC has been intensively tested in radiation environments by exposing the dice to various beams of species: protons, ions, mixed field, neutrons and X-rays [103], [104].

To read out the CLARO triggers a custom board has been designed, the Photo-Detector Module Digital Board (PDMDB). Being shown in fig. 1.8, it provides the interface between the FE boards and the upgraded LHCb readout architecture. Two versions of PDMDBs have been designed to match with the two types of EC: PDMDB-R and PDMDB-H. PDMDB-R will be coupled with the EC-R while the PDMDB-H with the EC-H.

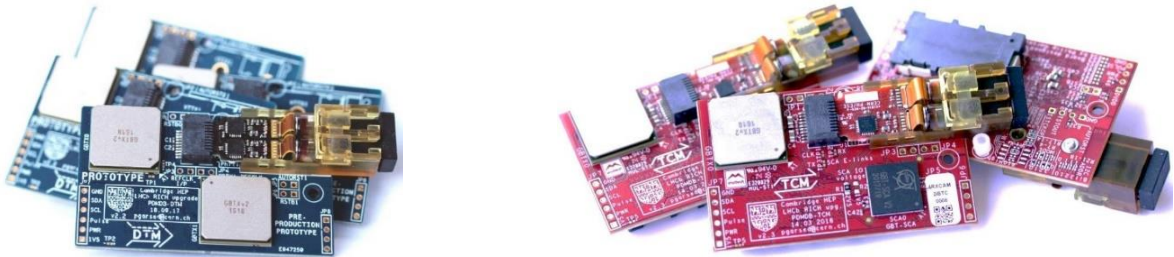




**Fig. 1.8** The PDMDB-R fully assembled [105]

Commercial-grade FPGAs, XC7K70T from Xilinx KINTEX-7 family [106], are used to synchronously read out the CLARO output triggers at a rate of 40 MHz. Besides latching the triggers, the FPGA performs some minimal processing and phase alignment of the data. The overall LHCb-RICH firmware occupancy for each FPGAs is  $\sim 1\%$ , however its I/Os pin usage ratio is close to 80% of total I/O pins. Each PDMDB reads 512 CLARO triggers, which are distributed across 3 FPGAs for the PDMDB-R and 2 FPGAs for the PDMDB-H.

To fanout the data from the PDMDBs to the LHCb readout infrastructure on the off-detector side, optical links are used. Each PDMDB requires 6 half-duplex links of 4.8 Gbit/s each to transmit the MaPMT-trigger data stream, and one full-duplex link of 4.8 Gbit/s to be used to communicate with the off-detector electronics for monitoring, control and synchronization. For this purpose, dedicated plugin modules have been designed and are shown in fig. 1.9: the data transmission module (DTM) and timing and control module (TCM).



**Fig. 1.9** The PDMDB plugins modules: DTM plugin (left) TCM plugin (right) [105]

The DTM plugin embeds two radiation-hard gigabit interface link ASICs (GBTx) developed by CERN [107] to carry out the data transmission from FPGA to the LHCb readout infrastructure. Data is converted from electrical in optical signals by using dual half duplex versatile links, VTTX [108], with one GBTx from each transmitter. There is one DTM per FPGA inside a PDMDB, hence 2 DTMs are used for a PDMDB-H and 3 DTMs for a PDMDB-R.

The TCM plugin is the master link interface and it embeds a full duplex link using the versatile transceiver, VTRX. Two ASICs are present on this plugin, the GBTx used to transmit

data, and a radiation-hard slow control adapter ASIC, the GBT-SCA [109]. The GBT-SCA is a dedicated chip with the purpose to distribute various control signals to the front-end electronics and to carry out monitoring operations of environmental parameters, e.g. temperature. It provides the timing and the synchronization of the whole on-detector readout infrastructure. It provides various general-purpose interfaces like: SPI, I2C, ADC, DAC, GPIO, and JTAG. One TCM is used per each PDMDB.

Five radiation hard DC-DC converters, FEAST2.1 [110], are used to power the PDMDB and its plugin modules by providing voltages between 1 V and 2.5 V.

One PDMDB-H or 2 adjacent PDMDB-R together with either EC-R or EC-H form a LHCb-RICH photodetection module (PDM). Each PDM has its own high voltage channel and they can completely communicate with the LHCb readout. Moreover, depending on the MaPMT gains and SNR the PDM can be placed in dedicated areas of the RICH sub-detectors, and various optimizations can be applied to reduce the noise (high voltage tuning, CLARO gain control etc.). The PDMs are assembled on columns, and each column has 6 PDMs. In tab. 1.1 the complete LHCb-RICH inventory is given. Around 1272 FPGAs are to be used, and due to the fact that these devices are commercial-grade, the radiation impact has to be studied.

**Tab. 1.1** *LHCb-RICH inventory*

|        | <b>Columns</b> | <b>EC-R</b> | <b>EC-H</b> | <b>PDMDB-R</b> | <b>PDMDB-H</b> | <b>FPGA</b> |
|--------|----------------|-------------|-------------|----------------|----------------|-------------|
| RICH 1 | 22             | 480         | 0           | 264            | 0              | 792         |
| RICH 2 | 24             | 192         | 384         | 96             | 96             | 480         |

The readout crate, located off-detector behind the concrete radiation wall, is used to read out the data from detector through optical links [89]. It has dedicated hardware, TELL40 [111], [112], and is the interface between the on-detector hardware and the online network. To ensure control and various monitoring tasks as well as timing and synchronization of the on-detector hardware, dedicated boards are to be used, SOL40 [88]. The SOL40 boards are tied to the S-TFC system which embeds the readout supervisor (S-ODIN) responsible for controlling the entire readout infrastructure by distributing timing and various calibration commands.

Another system infrastructure, the DCS, is used to monitor various non critical parameters that can affect the sub-detector performance: temperatures, humidity, pressure, and other signals [113].

The LHCb farm or the High Level Trigger and online farm [114] is a network-based system where the events are filtered for noise and then based on the data, real events are build. It has an aggregated bandwidth of  $\sim 32$  Tb/s. Then the data is passed to the online storage which serves as a temporary buffer as the data will be saved permanently on tapes. The whole LHCb readout is supervised and controlled by the ECS [115].

# Chapter 2

## Radiation Damage in Semiconductor Devices

### 2.1 Introduction on Radiation Effects in Electronic Devices

To understand better a radiation environment and to characterize its impact on electronic devices, some basic definitions need to be included first. Hence, according to international standards [116] the following items are used to describe briefly the proprieties of a particle beam:

- **Particle Flux  $\Phi$** : describes the particle number which are crossing a unit surface in a unit of time. It is expressed as: **particles / (cm<sup>2</sup> · s)**.
- **Particle fluence  $\Phi$** : represents the total number of particles crossing a unit surface in a given amount of time and is expressed as: **particles/cm<sup>2</sup>**.
- **Particle Energy E**: also known as kinetic energy and is given in **eV** (electron Volt).
- **Particle Species**: it refers to the type of particles used: electrons, protons, neutrons, ions or photons.

Several parameters are used to describe how the energy of a charged particle is transferred to a material [117] and few of them are describes below:

- **Radiation Absorbed Dose D**: represents the total amount of energy absorbed by an irradiated material in unit mass (kg or g) It is given in **Gray** (Gy), however the **rad** is used mostly by literature and its conversion to Gy is given in equation 2.1.
- **Dose rate  $\dot{D}$** : describes the time derivative of radiation absorbed dose and is expressed in **Gy/s** or **rad/s**.

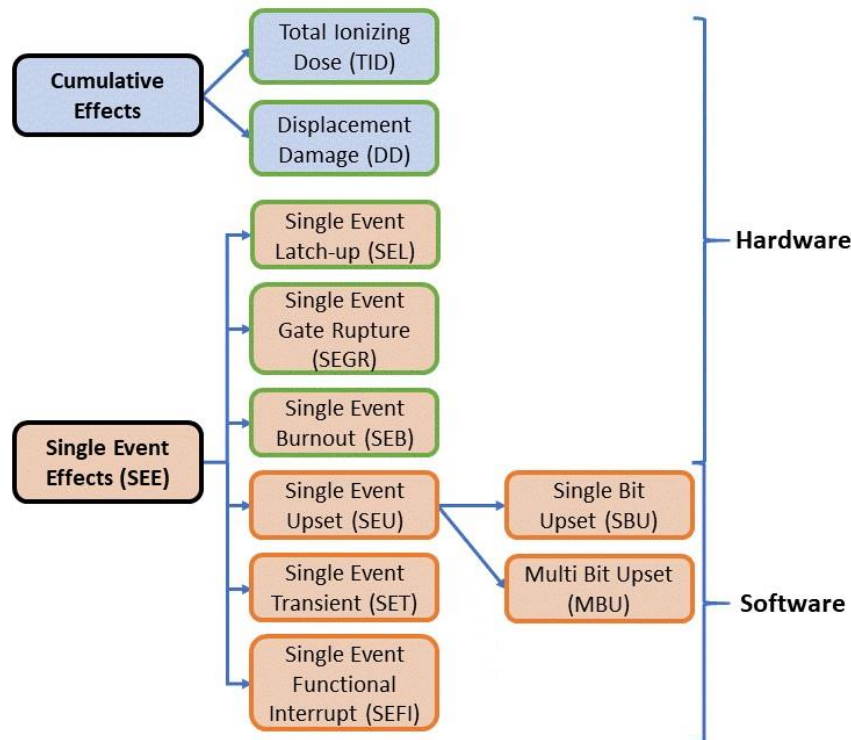
- **Linear Energy Transfer LET:** also known as the stopping power, is the amount of energy lost by a charged particle through ionization process in a material. It is expressed in **MeV · cm<sup>2</sup>/g**. (by division with material density)
- **The dose equivalent Dq:** is the product of radiation absorbed dose multiplied by a quality factor **q** and is expressed in **Sievert (Sv)**. This parameter gives a better measurement of the biological effect in a specific tissue due to the fact that q is chosen depending on particle species and their energy.

$$1 \text{ rad} = 10^{-2} \text{ Gy} = 10^{-2} \text{ J/Kg} \quad (2.1)$$

Depending on particle mass, its energy, charging state and the material, there are three ways on how a charged particle can interact with matter:

- by interaction with shell electrons of a target atom causing that atom to be ionized.
- by collision with the nucleus of a target atom, and if sufficient energy is provided atom is displaced and it becomes a recoil ion. In this case displacement damage will occur or at high recoil energy an ionization shower and secondary displacements.
- by triggering a nuclear reaction in a target nucleus, in this case the nucleus is split and energetic fragments are emitted, again with ionization shower.

Two general types of defects in semiconductor devices are triggered by radiation: *ionization* and *displacement damage*. Following these defects, the electrical parameters of the devices are modified which may cause either parametric or functional failure. These defects are classified in cumulative and single event effects (SEEs) and are presented in fig. 2.1. Depending on the nature of their occurrence, they can be subclassified as either hardware and software defects.



**Fig. 2.1** Classification of radiation effects in semiconductor devices

## 2.2 Cumulative Effects in Solid-State Devices

Cumulative effects [118] are due to accumulation of charges or defects into semiconductor layers during the entire exposure time of a given electronic device to a radiation environment. They are classified in two categories: Total Ionizing Dose (TID) and Displacement Damage (DD) effects.

TID damage is usually triggered by a charged particle such as protons/hadrons or photons which can produce ionization through their energy loss in that material. DD is the result of the interaction of matter mainly with neutral particles, e.g. slow neutrons, leading to displacement of atoms from their lattice, displacement damage could be induced by high energy hadrons too, though the ionization effects usually are more destructive in these cases.

### 2.2.1 Total Ionizing Dose

When electronic devices are exposed to an ionizing radiation source, they accumulate part of the deposited energy in form of induced localized charges and the total amount of radiation dose which was accumulated during the whole exposure is known as TID and is usually correlated with the material which was exposed: Si, SiO<sub>2</sub> etc. Most of TID energy is released by recombination, low frequency electromagnetic radiation and heat, but some is converted in localized electric changes of the semiconductor.

The performance of electronic devices may be degraded by the dose accumulated in the oxide dielectric layers, which usually are SiO<sub>2</sub> or HfO<sub>2</sub> (as gate dielectric) in modern CMOS electronics [119]. Through ionization, electron-hole (e-h) pairs are generated, and they can be separated using a local electric field. Trapped holes in the insulator layer or acceptors/donors at the Si-SiO<sub>2</sub> interface are both the reason for the production of the localized charges. These two defects, trapped holes and interface states, lead to aging and bad behavior of the electronic devices.

TID effects in electronic devices are different for different technologies. Bipolar technologies manifest increasings of leakage currents and gain degradation [120]. CMOS technologies are more affected by TID and are manifesting various failures like: decrease of transconductance, increased noise, increase in leakage currents and threshold voltage shifts [121].

In this thesis, the *TID-induced leakage current* is defined as a global excess of the current consumption in the integrated circuits under radiation exposure. This is in agreement with the literature [122].

*TID effects in CMOS technology* are described starting with the generation of e-h pairs in the gate dielectric oxide layer of a MOS structure. If a MOS structure is irradiated with a homogeneous dose, the number of e-h pairs,  $N_{eh}$ , generated in the SiO<sub>2</sub> layer can be calculated by using the equation 2.2:

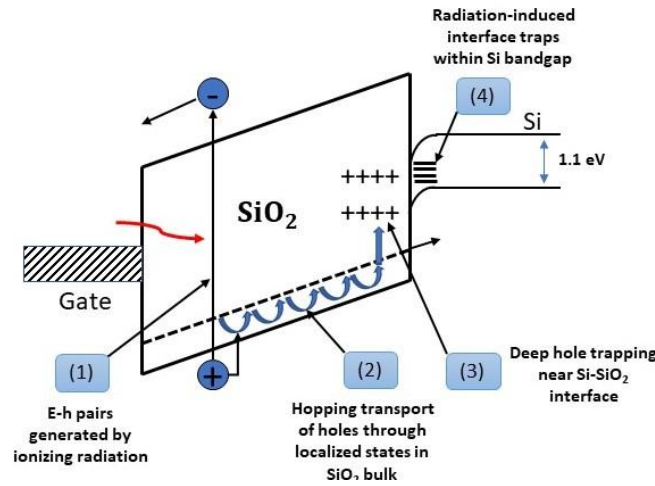
$$N_{eh} = \frac{Q_{eh}}{e} = A \cdot d_{ox} \cdot g_o(\text{SiO}_2) \cdot D \quad (2.2)$$

where,

- ❖  $Q_{eh}$  – charge generated of electrons and holes;
- ❖  $e$  – electron elementary charge,  $e = 1.6 \cdot 10^{-19} \text{ C}$  ;
- ❖  $A$  – gate surface;
- ❖  $d_{ox}$  – insulator thickness;
- ❖  $g_o(\text{SiO}_2)$  – regeneration rate in  $\text{SiO}_2$ ;
- ❖  $D$  – radiation absorbed dose.

The energy needed to generate e-h pairs is known as ionization energy ( $E_{ion}$ ), and its value depends on the material: 3.6 eV for Si, 18 eV for  $\text{SiO}_2$  [123], 4.8 eV for GaAs and 2.8 eV for Ge [117].

Both NMOS and PMOS devices are affected by TID, however the NMOS devices show significant more TID damage than the PMOS devices. This is due to the fact that the gate of a NMOS device is positively biased (to enable the conductive channel), which cause the holes to be guided to the Si-SiO<sub>2</sub> interface, leading to positive hole traps into the oxide. On the other hand, the gate of a PMOS device is negatively biased (to enable the conductive channel), which leads to only a minor hole population into the oxide [117]. In the following, the basic TID mechanism in NMOS device is described. Therefore, fig. 2.2 presents the energy band diagram of an irradiated NMOS device in four physical processes.



**Fig. 2.2** Energy band diagram of an irradiated NMOS device illustrating major physical processes (adapted after [122])

A sensible area of a NMOS device to radiation is its oxide insulator layer. When a charged particle passes through the gate oxide, free e-h pairs are generated by the deposited energy of the incident particle, as illustrated in the first process from fig. 2.2. It takes a picosecond or less for the electrons to be evacuated from the oxide due to their higher mobility than holes in the  $\text{SiO}_2$  [124]. Within that first picosecond, a fraction of holes and electrons will recombine, depending on the type and the species of the incident particle. The remaining holes, which

escaped recombination, may – in certain conditions – remain near their point of generation and they contribute to a negative shift of the threshold gate voltage ( $V_{th}$ ).

The transportation of holes to the Si-SiO<sub>2</sub> interface via hopping transport, shown as the second process in fig. 2.2, is a dispersive process which leads to short-term recovery of the  $V_{th}$ . However, this process usually takes place over decades (log) in time, and is very dependent on temperature, applied field, oxide thickness and to some extent the oxide manufacturing process [122].

*Deep hole trapping* near the Si-SiO<sub>2</sub> interface (third process from fig. 2.2) arise due to the presence of sites with O vacancies (or excess Si) within the amorphous SiO<sub>2</sub> [122]. This leads to weak Si-Si bounds, with each Si atom being back-bonded with three O atoms. As the holes are moving to the Si-SiO<sub>2</sub> interface, some of them are trapped and lead to a relaxation of the lattice due to a broken Si-Si bond. As a consequence, additional positive charge is built within the SiO<sub>2</sub> which contribute to an additional negative voltage shift of  $V_{th}$  [122]. These traps are spread all over the SiO<sub>2</sub> volume, and their concentration is varying with the SiO<sub>2</sub> manufacturing process.

The free holes which are not trapped in the SiO<sub>2</sub> can step to the Si-SiO<sub>2</sub> interface, see forth process in fig. 2.3. As a consequence of the transition to the crystalline material, dangling (incomplete) atomic bonds are present here which manifest as energy levels within the band-gap. Depending on the Fermi-level, they trap either electrons in case of NMOS devices (p-type Si) or holes in case of PMOS devices (n-type Si) [122]. Although, usually the dangling bonds are passivated by using H atoms, the radiation-induced free holes can react with the H and thus the dangling bonds are re-activated [122]. Such effects are commonly known as *radiation-induced interface traps* and results in a negative space charge for a NMOS transistor due to electron traps [122].

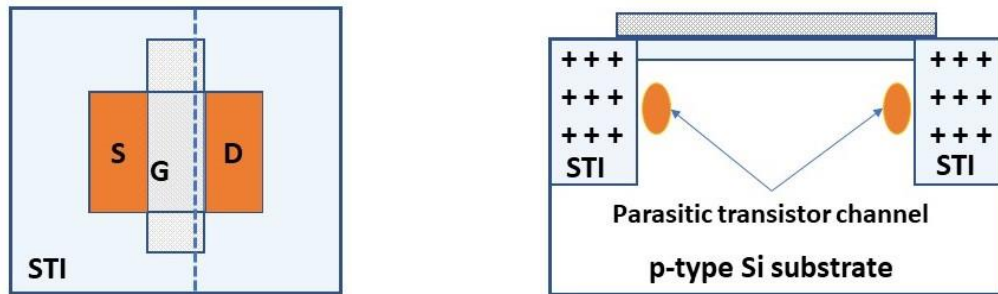
Besides shifts in the  $V_{th}$ , the following electrical parameters of a MOS device may be affected as result of ionizing radiation: increase in leakage current (e.g. gate and drain current under radiation exposure), decrease in transconductance. However, CMOS devices may manifest in addition at least one of the following symptoms: additional propagation delay times, reduction of output voltage and maximum output current [117].

Driven by Moore's law, the aggressive downscaling of MOS technology has shrunk the gate dielectric to ensure higher speed operation and lower power consumption. Nevertheless, with the ultra-scaled SiO<sub>2</sub> as gate dielectric the devices have been proven to have a very good radiation resilience [125]. To cope with the low power requirements of modern electronic devices, the technology nodes beyond 45 nm have introduced the use of high-k dielectrics such as hafnium oxide (HfO<sub>2</sub>) [126]. By using thicker materials without compromising the general rules of constant field scaling the gate leakage current is reduced. Hence, the gate leakage current will be neglected in the next chapters due to the fact that the investigated circuits were manufactured with sub-350  $\mu\text{m}$ .

On the other hand, TID effects may still be visible in the insulator oxides and guard rings used to isolate two neighboring transistors in a CMOS structure, as they still have large thickness up to a few hundreds of nanometers, which makes them prone to charge formation [127]. Two methods exist to isolate the two neighboring transistors in a CMOS structure: local oxidation of silicon (LOCOS) and shallow trench isolation (STI) oxide. The LOCOS isolation was used in technologies down to 250 nm [128], and it was replaced by STI to reduce the

leakage currents in advanced technology nodes. Therefore, deep-submicron CMOS technologies use STI insulator oxides for electrical isolation between transistors in the nowadays integrated circuits [125].

TID effects in STI oxides of a CMOS structure are a well-known problem related to the radiation hardness of an electronic device, and their mechanism of appearance is similar with the one described above for the gate dielectric oxide. The point of origin for the increase of leakage current is the parasitic transistor channel along STI, in which a transistor is embedded as shown in the left side of fig. 2.3. With the appearance of TID-induced positive charges in the STI, an inversion layer is created within the STI, which leads to additional drain-to-source leakage paths [129] as shown in the right side of fig. 2.3. Such leakage paths are described as the channels of two parasitic transistors, due to their similar layout with a transistor. However, the only difference is the fact that the electric field required to enable the transistor channel comes from the space charge in the STI, instead of a gate potential.



**Fig. 2.3** Top view of a NMOS transistor showing its terminals and the STI (left side) and the cross-section of NMOS transistor along the dashed line from the left side showing the parasitic transistor channel with orange (right side) (adapted after [129])

The space charge in STI is always positive for both PMOS and NMOS devices. This means that for NMOS devices the radiation-induced electric fields generated by the negative space charge within the Si-SiO<sub>2</sub> interface and the positive space charge within the STI are compensating each other. However, in the PMOS case, these two electric fields are cumulated due to their positive charge [129].

The TID-induced increase of the leakage current due to STI effects is only visible in NMOS devices. This is due to the fact that the parasitic transistor channels within a PMOS device are closed by the TID-induced positive space charge in STI [130].

The intra-device increase of the drain leakage current as a result of TID-induced effects within STI is a well-known effect and is considered one of the major problems in NMOS transistors when are exposed to high TID [131]. Such effect may cause large increase of the static power dissipation in a device [132]. The probability of TID-induced effects in STI is reduced with the aggressive downscaling of the technology.

Deep-submicron CMOS technologies, e.g. 28 nm CMOS technology, have excellent TID radiation resilience as they show insignificant TID effects up to tens of Mrad (Si) [133].

*TID effects in bipolar technology* are the same as in the MOS devices, however they manifest in a different way. Positive trapped charges in the insulation oxides and the accumulation of interface states at Si-SiO<sub>2</sub> interface combined with various factors of emitter



bias, polarity, base doping density, emitter technology and dose rate can lead to gain degradation as well as inversions in the Si layer under a very thick oxide. Depending on the technological characteristics, the inversion channel can be created in various places: surface, sidewall and on the substrate [134]. The substrate inversion leads to the opening of a channel between two buried layers leading to an increase in the leakage current, while the sidewall inversion may lead to a very low-resistance path (short-circuit) between emitter and collector for NPN transistors.

The gain degradation in bipolar transistors, especially for NPN transistors, is the general TID effect and it has been intensively studied. It has been established that is due to the increased recombination in the emitter-base depletion region [135]. This is mainly due to accumulation of interface states in the base surface and due to positive charge buildup in the vicinity of the emitter-base junction. This results in an increase of the base current with the collector current being constant, hence the overall gain is lower.

In general, even at very high doses and depending on the technology node, the TID effects are not permanent effects as the trapped holes may be removed during or post irradiation through a annealing process in a given amount of time [136]. Such annealing is a physical process which removes the trapped holes and restore the device to normal operation in given amount of time, depending on the TID, dose rate and temperature.

In general the annealing process gives a very strong exponential function of time. Therefore, the hole traps near the Si-SiO<sub>2</sub> interface will be neutralized in a very short time, but the ones trapped far away from the Si-SiO<sub>2</sub> interface will take much more time to be neutralized. The slope of the annealing curve may decrease with time, if the spatial density of traps within a distance into oxide is decreasing.

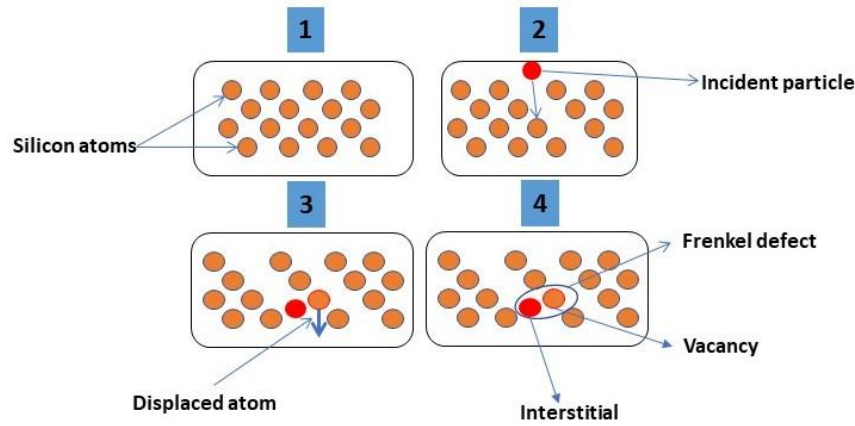
Under normal bias conditions modern technologies shown very visible room-temperature annealing, making this very accessible to perform such operations on the irradiated devices.

## 2.2.2 Displacement Damage

The non-ionizing energy loss (NIEL) in Si cause dislodges of the atoms from their structure, leading to degradation of the electrical characteristics of semiconductor devices due to displacement damage.

The displacement damage process is shown in fig. 2.4 and it is explained using the following steps:

- 1: usually a silicon structure has equally spaced atoms;
- 2: an incident particle enters in the structure;
- 3: there is a probability that an atom to be dislodged as a consequence of a particle elastic collision;
- 4: Frenkel defects [137] may be created consisting of a vacancy and an interstitial defect.



**Fig. 2.4** Displacement damage process (adapted after [138])

To form Frenkel defects, a minimum energy depending on the target material is required: 35 +/- 5 eV for diamond, 27.5 eV for Ge, 21 eV for Si and 7-11 eV for GaAs [139].

Three important mechanisms are following after radiation-induced displacement damage in semiconductor materials:

- Modification of donor or acceptor density;
- Charge trapping close to the band edges;
- Creation of min-gap states, which enables the transition of electrons from the valence to the conduction band.

Lattice defects are influenced by the fluence of particles which travels through the atomic structure and the DD effects are gradually amplified. Depending of particle type and their energy, each of them may induce DD with a relative weight and a rough comparison for several types of particles is shown in table 2.1:

**Tab. 2.1** Various particles and their relative displacement damage [130]

| Particle        | Proton | Proton | Neutron | Electron | Electron |
|-----------------|--------|--------|---------|----------|----------|
| Energy          | 1 GeV  | 80 MeV | 1 MeV   | 1 MeV    | 1 GeV    |
| Relative Damage | 1      | 2      | 2       | 0.01     | 0.1      |

The displacement damage is a gradual effect and is usually given as the number of 1 MeV equivalent neutrons per given area, **1 MeV neq./cm<sup>2</sup>**. However, it is proportional to the NEIL, which can be calculated with the equation 2.3, and it is expressed in **MeV · cm<sup>2</sup>/g** [140].

$$\text{NIEL} = N/A \cdot [(\sigma_e \cdot T_e) + (\sigma_i \cdot T_i)] \quad (2.3)$$

where:

- ❖  $N/A$  – material density ( $N$  – Avogadro's number,  $A$  – atomic mass);
- ❖  $\sigma_e$  – elastic cross-section value;
- ❖  $T_e$  – elastic effective average recoil energy;
- ❖  $\sigma_i$  – inelastic cross-section value;
- ❖  $T_i$  – inelastic effective average recoil energy;

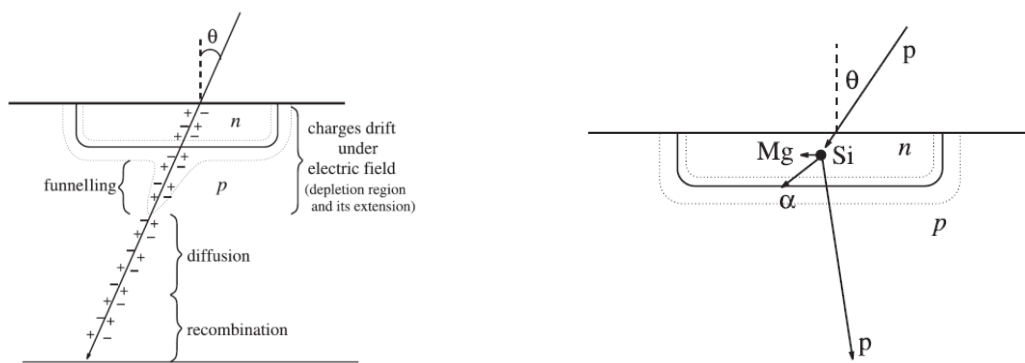
The bipolar technology is known to be highly affected by displacement damage and these devices can manifest gain degradation. The gain degradation in bipolar devices is due to increased recombination of minority carriers in the base region [141]. Optoelectronic devices are known to be susceptible to displacement damage [142]. In particular, optocouplers have a high sensitivity to displacement damage, and as a consequence, the degradation of current transfer ratio (CTR) was seen to be the most affected parameter [143]–[145]. Defects in CMOS technology due to displacement damage are negligible as the MOS properties are not significantly affected by the minority carrier lifetime [146].

## 2.3 Single Event Effects

### 2.3.1 Single Event Effects – Physical Mechanisms

Single event effects (SEEs) are due to the path of a single high energetic and high- $Z$  ( $Z > 2$ ) particle passing through the device semiconductor layers while depositing its energy through ionization.

Usually heavy ions can trigger SEEs by direct ionization and e-h pairs are generated along the track of the particle within a sensitive area of the microelectronic device, as shown in the left side of fig. 2.5. Protons and neutrons may trigger SEEs by nuclear interactions (inelastic and elastic scattering or spallation) with the atoms, i.e. nuclei, within the semiconductor device resulting in production of a large spectra of light particles (protons, deuterons, light nuclei) and heavy recoil nuclei. The majority of the recoil ions are much heavier than the original incident hadron/particle, therefore, they have much large ionization potential (proportional with  $Z^2$ ). As a consequence, the recoil ions may generate e-h pairs along their path (indirect ionization). The basic mechanism of indirect ionization is shown in the right side of fig. 2.5.



**Fig. 2.5** SEE mechanisms due to direct ionization (left side) and due to indirect ionization by creation of several possible states or recoiling ions (right side) [147]

Following ionization process, either direct or indirect, a very localized charge is deposited into the semiconductor material, and if higher than a given threshold value, known as the critical charge ( $Q_c$ ) [148], then the SEE probability of production is high. The critical charge is

generated by particle energy deposition in a critical volume within the device. The region where the charge collection mechanism takes place is known as the sensitive volume and is described as an rectangular parallelepiped (RPP approximation) [147].

Each particle, depending on its energy, type, Z-charge, and mass, can deposit an energy into the sensitive volume of the target material which is known as linear energy transfer (LET) or the stopping power. LET is expressed in **MeV · cm<sup>2</sup>/mg** and can be calculated by using equation 2.4:

$$\text{LET (x)} = \frac{1}{\rho} \cdot \frac{dE}{dx} \quad (2.4)$$

where:

- ❖  $\rho$  – target material density;
- ❖  $dE$  – energy loss of the particle;
- ❖  $dx$  – the depth of the particle through the target material.

The LET can be also expressed in terms of values of electrical charge generated per unit path length. This is based on the fact that usually it takes an average of 3.6 eV for a single particle to generate e-h pairs into a Si layer. Hence, in silicon devices, an LET of 1 MeV · cm<sup>2</sup>/mg corresponds by approximation to a charge deposition of 10 fC/μm [149].

Due to technology downscaling and large integration of high logic density the SEE probability in such devices is higher. The critical charge threshold had abruptly decreased with the size-reduction of technology, giving high probability for even low energy particles to deposit enough energy to trigger a SEE. An approximation of the critical charge value for a given technology node can be calculated with the equation 2.5 introduced by Petersen [150]:

$$Q_c = 0.0023 \cdot t^2 \quad (2.5)$$

where the  $Q_c$  is expressed in pC and  $t$  is the technology node given in μm. As an example, some  $Q_c$  values have been calculated for various technology sizes: 230 fC for 10 μm, 2.3 fC for 1 μm, 0.28 fC for 0.35 μm, 0.05 fC for 0.15 μm and 0.0018 fC for 28 nm.

The effects caused by SEE depend on the energy of the particle and the characteristics of the device: semiconductor material, thickness, geometry, technology node and the package thickness.

Depending on how they may be affecting the integrated circuits the SEEs can produce the functional failures: Single Event Transient, Single Event Upset, Single Event Latch-up, Single Event Gate Rupture and Single Event Burnout.

### 2.3.2 Single Event Transient

Transient effects may occur due to single particle strike into the semiconductor layer and they manifest as a temporary perturbation which can be propagated forward in the circuit leading to malfunctions of the devices. These are known as single event transients (SETs) and are present

as a glitch or a parasitic-induced pulse. They are described by the shape, width and amplitude [151].

In digital circuits they are mostly induced into the combinational logic in which they may be propagated through and up to the input of a latch. Minimum four criteria have to be met by a radiation-induced transient pulse in order to have an error [152]:

- the particle strike must deposit enough charge to generate a transient pulse strong enough to propagate;
- the availability of an open path to a storage element through a path of logic elements;
- the SET should have sufficient amplitude and width to be able to change the logic state of the latching element;
- the transient pulse must be present on the latching edge of the clock.

The number of logic elements in a combinational logic chain which can be traversed by a SET is directly dependent with its width as well as the technology of the device [153]. As the transient width is wider, the more logic elements can traverse, and the probability to arrive at the input of a storage element is higher.

With the downscaling of the technology, the device operation frequency becomes higher, giving more latching clock edges to shift-in a transient pulse, hence increasing the overall error rate. In this way the SET pulses can induce overtime multiple errors and malfunctions of the electronic devices. Efforts are made to simulate [151] and to mitigate the impact of SETs in complex electronic circuits [154].

In analog circuits, the SETs are identified as glitches or as very short variations of the output voltages from various components like: operational amplifiers [155], comparators [156] or voltage references [157].

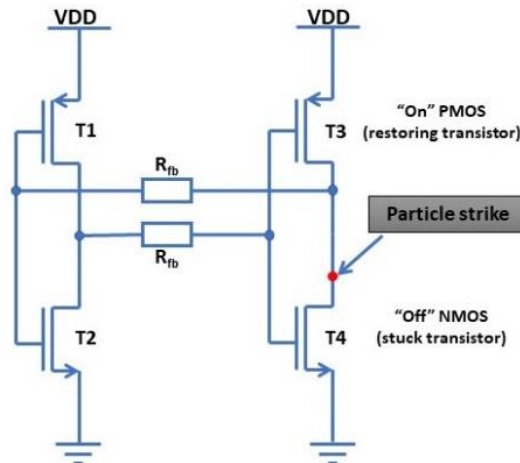
### 2.3.3 Single Event Upset

Localized charge depositions into the semiconductor layer due to the particle strikes may lead to software errors like bit-flips in digital circuits. The bit changes are possible in memory cells, Flip-Flops (FF), look-up tables (LUT) or other digital logic resources. These are known as single event upsets (SEUs) and are non-destructive and permanent radiation-induced effects – permanent in sense that they are latched till the resource is reset by rewriting of configuration or of device memory resource. Depending on the number of bit-flips induced by a single high energetic particle, SEUs are subclassified as: single bit upset (SBU) and multi bit upset (MBU). Several types of memories are known to be very susceptible to radiation-induced SEUs: static random-access memory (SRAM), dynamic random-access memory (DRAM) etc.

SRAM technology is a broadly used type of memory, especially in complex devices like FPGAs, ASICs or basic memory cells. Its basic structure is shown in fig. 2.6 and is composed from two CMOS inverters and 2 additional transistors used for read/write operations which are not shown.

If a sensitive SRAM location is hit by a particle, which is usually the reversed-biased drain junction of the NMOS transistor in the off state, e.g. T4 in fig. 2.6, charge collection in that transistor leads to a transient current [158]. As the current flows in T4, the T3 transistor will

source current as an attempt to neutralize the particle-induced current. However, the current flow through T3 leads to a voltage drop induced at its drain. This voltage drop is actually the mechanism for SEU in SRAM cells, as it is similar with the write signal, causing the wrong value to be stored in the memory cell. There are four possible locations on which a particle strike may induce a SEU in the SRAM cells, namely the drain terminals of the four transistors.



**Fig. 2.6** SEU mechanism in SRAM cells (adapted after [159])

DRAM cells describe a one transistor-design, which stores charge as binary information in a capacitor. Due to the fact that the information storage is passive, the radiation-induced upset in DRAM cell is persistent until is corrected by the external circuitry [160]. SEUs in the DRAM cells, are not all the time caused by radiation induced bit-flips, but sometimes degradation of the stored charge results in a signal level which is no longer readable and it is enough to cause a bad interpretation/read of the stored bit.

An energetic particle may deposit a large amount of charge into a semiconductor device enough to cause a cluster of upsets in the vicinity of the charge collection region, hence the MBUs are induced in this way. This happens if the incident ion or deflected ion or collision produced ion crosses multiple active regions on the device at oblique or tangential angle.

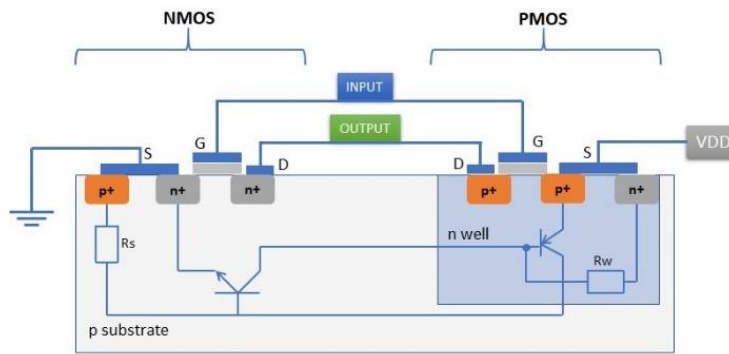
### 2.3.4 Single Event Functional Interrupt

Another software SEE, is the single event functional interrupt, SEFI. SEFI manifests as a temporary non-functionality of a device, which keeps the device in an unknown state till the an external operation is performed: either power cycle or reconfiguration [161]. In modern complex circuits such as micro-controllers or FPGAs, they may manifest as: restart/reset while is operating, complete freezing, partially or fully data loss of the program/configuration [162].

SEFI may induce high current states in FPGAs due to the corruption of the configuration memory that affects the internal FPGA control registers [9]. Other type of SEFI seen in FPGAs can cause their operation to partially freeze [163]. However, all SEFIs can be fully recovered by either an external reset, a power cycle or a full reconfiguration of the device.

### 2.3.5 Single Event Latch-up

Single event latch-ups (SELs) are hardware defects which are described as high current states due to low resistant paths between the power lines in CMOS electronic devices as a consequence of particle strike [164]. In a CMOS inverter, there are inherited two parasitic bipolar transistors, as shown in fig. 2.7, which in normal operating conditions they act as PMOS and NMOS transistors. In this way, this two-transistor configuration forms a p-n-p-n structure which is known as thyristor or silicon-controlled rectifier (SCR).

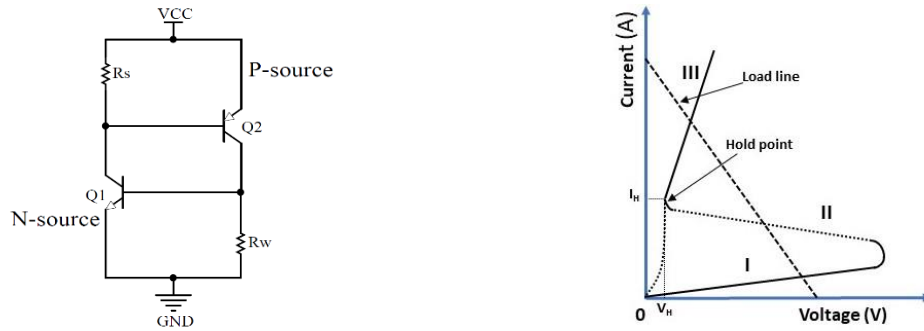


**Fig. 2.7** Cross-section of a CMOS inverter showing the parasitic bipolar transistors in a thyristor like structure (adapted after [165])

The two-transistor system, which is an equivalent thyristor like structure, shown in the left side of fig. 2.8, and represents the usual latch-up in CMOS circuits. The current-voltage characteristics of a latchable structure are shown in right side of fig. 2.8. Two independent regions are shown and which are describing the behavior of a latch-up. Region I, describes the normal operation of all devices, prior to latch-up occurrence. When a particle strikes the CMOS structure, and assuming the deposited charge is high enough, it can turn-on either one of the parasitic transistors, resulting rapidly in a transition to high current states, as described in region III. The load line is highlighting the power supply output capabilities.

The holding voltage ( $V_H$ ) and the holding current ( $I_H$ ) are two key parameters in the latch-up characteristics. They describe the minimum conditions needed to sustain a latch-up. Once the latch-up has been enabled, it will sustain as much as circuit conditions are consistent with the voltage and current holding requirements.

There are only two ways to restore a latch-up from a device, once activated: complete power cycle and lowering of the power supply voltage below the holding voltage. Usually the power cycle of the entire device is the easiest way, however people have been investigating methods to bypass the complete power cycle, by reducing the voltage in the power rails below the holding voltage. The holding voltage varies with the technology downscaling, and its minimum value is approximately 0.8 V. If the devices are operating under or around the minimum latch-up voltage holding value, then the latch-up will not be activated [165].



**Fig. 2.8** Equivalent structure of thyristor composed from two bipolar transistors (left side) and its current-voltage characteristics (adapted after [165])

High temperature dependence has been reported in radiation-induced latch-up, as its probability is higher by a factor of about 2.7 at high temperatures, 125 °C, than at the room temperature of 24 °C for the same LET delivered to the device [166]. This is due to two mechanisms in the bipolar transistors: the decrease of the forward bias voltage ( $V_{BE}$ ) by approximately 2mV/°C and the increasing in the well resistance due to elevated temperatures. The increase of the well resistance is the dominant factor.

SELs are not the only ones which are causing high-current states in electronic devices. Two additional failures, single event snapback (SES) and second breakdown, can be present in either CMOS or bipolar devices and neither of them requires a p-n-p-n structure. They may occur even in latch-up immune technologies.

*Snapback* is a failure which can be triggered in a NMOS transistor structure. It is due reduction of the avalanche breakdown voltage in the parasitic bipolar transistor inherent in the NMOS. This results in high current states through the transistor which, unlike the latch-up, it can be removed by changing the gate voltage without a power cycle of the device [167].

*Second breakdown* can be triggered in bipolar technologies, being caused by localized heating in the filamentary structure, mesoplasma, of a reverse-biased junction. Inhomogeneities in the silicon leads to mesoplasma and cause very high and localized currents to flow in that region. Once is formed, a high-current condition inside the bipolar structure is created due to abrupt reduction of the breakdown voltage even in normal operating/bias conditions.

### 2.3.6 Single Event Gate Rupture and Single Event Burnout

Two destructive and permanent radiation-induced SEEs can be triggered by a particle strike: single event gate rupture (SEGR) and single event burnout (SEB).

*Single event gate ruptures* are catastrophic failures affecting power MOSFETs when they are in the “off” state [168]. These failures are due to a heavy and energetic ion strike in the neck region of a MOSFET while is under positive drain-to-source bias (NMOS). Following the path of the ion, e-h pairs are generated and they are separated due to the  $V_{DS}$  which is affecting the substrate field. This results in an temporary increase of the oxide field near the strike region due to charge build-up at the Si-SiO<sub>2</sub> interface, and it usually last for a few picoseconds [169]. Oxide breakdown occurs when the increased oxide field is larger than the critical oxide



breakdown, hence a permanent short-circuit through the oxide results. SEGR are detected by measurements of high current increase in the gate and drain terminals, and are usually seen in power MOSFETs [170].

*Single event burnout* is another destructive and permanent failure which is affecting power devices (MOS and BJT transistors, diodes) while they are in the “off” state. In a MOSFET device, SEB is triggered by the transient current which is generated by the heavy ion strike, and resulting in the activation of the parasitic bipolar transistor inside the MOS structure. This will cause a regenerative feedback mechanism leading to an increase of the collector current and finally to secondary breakdown [171]. SEB in BJT transistors has been identified to have the same mechanism as the failures seen in the parasitic bipolar inherent in the MOSTFET transistors [172].

The SEB mechanism in power diodes is different from the power MOSFET transistors, as they do not have the inherent BJT. However, it has been seen that the SEB in power diodes is due to strong avalanche charge carrier multiplication triggered by ion strike and resulting in rapid increase of the current within a few nanoseconds. Then, due to thermal breakdown the SEB occurs [173].

### 2.3.7 SEE Measurement Procedures

The sensitivity of electronic devices to any type of radiation-induced SEEs (SET, SEU, SEL, SEGR, SEB) is calculated by using the measurement of cross-section,  $\sigma$ , as function of LET for ions, and as a function of energy for protons and neutrons [147]. In this way, by knowing how many particles have passed through the semiconductor layers of the device and by counting the number of SEEs, the probability of SEE occurrence by a given particle strike can be calculated by using the equation 2.6 for ions and 2.7 for protons and neutrons. The result, gives the number of failures divided by the number of particles per  $\text{cm}^2$  which are causing SEEs, and is described as the cross-section of the device under test.

$$\sigma(\text{LET}) = N_{\text{failures}} / \Phi [\text{cm}^2] \quad (2.6)$$

$$\sigma(E) = N_{\text{failures}} / \Phi [\text{cm}^2] \quad (2.7)$$

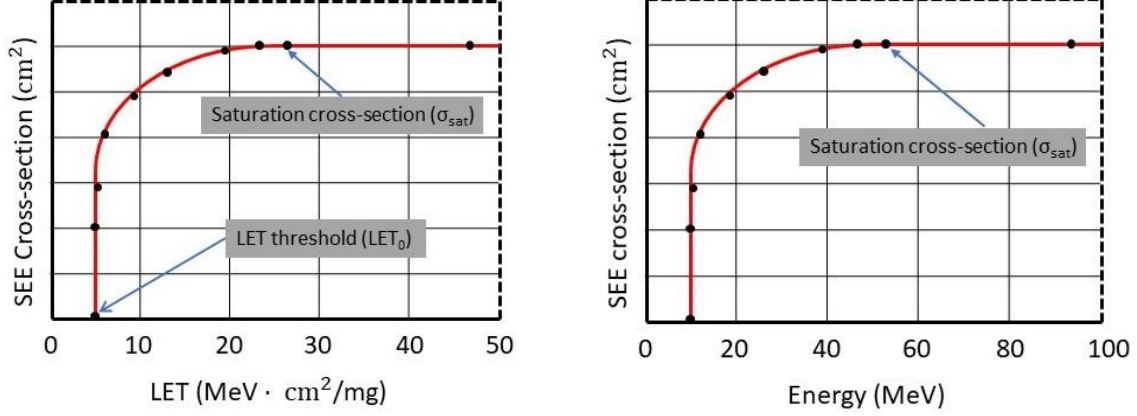
where,  $N_{\text{failures}}$  is the total number of failures recorded in the device during exposure at a given total incident particle fluence  $\Phi$  per device surface. When the device is irradiated with ions, the inclination angle  $\theta$  of the ion beam can change the total effective LET deposited into device, and also the beam facilities give the fluence for a surface transverse to the beam, and to compute the effective particle fluence on the device surface is required to multiply the facility value with cosine of angle  $\theta$ .

In some cases, the SEE cross-sections can be given as per device or per bit for memories. In this case, the equations 2.8 and 2.9 are used to calculate the corresponded cross-section values.

$$\sigma(\text{per device}) = N_{\text{failures}} / (N_{\text{devices}} \cdot \Phi) \quad (2.8)$$

$$\sigma(\text{per bit}) = N_{\text{failures}} / (N_{\text{bits}} \cdot \Phi) \quad (2.9)$$

For different values of LET for ions and energy for protons and neutrons the cross-section values can be plotted as a Weibull distribution, see fig. 2.9.



**Fig. 2.9** Typical cross-section curves for ions as a function of LET (left side) and for protons/neutrons as a function of particle energy (right side) (adapted after [147])

With more induced SEEs in individual sensitive volumes within the circuit as a consequence of the LET increase, the Weibull distribution can be imagined as a cumulative distribution. The LET<sub>0</sub> describes the threshold from where the device starts to manifest SEEs for a minimum ion fluence of 10<sup>7</sup> ions/cm<sup>2</sup> [174]. The saturation cross-section, σ<sub>sat</sub>, describes the maximum number SEEs over the whole sensitive area inside the device.

The protons and neutrons may induce SEEs into a silicon device via nuclear reactions with the material (indirect ionization) only if the charge deposited following recoil ion propagation exceeds SEE threshold LET of the device under test, which is below 15 MeV · cm<sup>2</sup>/mg in some devices [175]. However, the highest LET induced by protons via indirect ionization is about 34 MeV · cm<sup>2</sup>/mg in modern semiconductor materials [176]. Therefore, if an electronic device has the SEE threshold LET above 34 MeV · cm<sup>2</sup>/mg, the proton SEE testing is expected to yield no SEE.

According to the ESA/ESCC radiation testing guidelines [177], when testing for SEE several requirements have to be met:

- ❖ in case of proton SEE tests, protons beam with the energy in range of 20 to 200 MeV with an adjustable flux from 10<sup>5</sup> protons/cm<sup>2</sup>/s to minimum 10<sup>8</sup> protons/cm<sup>2</sup>/s needs to be used.
- ❖ for heavy ion SEE tests, the ions have to be capable to have a penetration depth of at least 40 μm in silicon while ensuring an adjustable flux from 10 ions/cm<sup>2</sup>/s to a minimum of 10<sup>5</sup> ions/cm<sup>2</sup>/s. The possibility to rotate the x axis of the device under test with respect to the beam is desirable in order to increase the effective LET.

The reliability of electronic devices to various types of radiation-induced effects must be addressed for each new device which may be considered for safety-critical applications operating in radiation environments. Further, testing strategies, monitoring solutions as well as measurement techniques have to be adopted to record any relevant information and parameters

of the electronic device under test while it is placed in a particle beam. This implies complex automatic and custom designed test benches to satisfy the monitoring and control requirements of the electronic device intended to be tested. Therefore, various testing methods and techniques have been standardized over the time by experienced researchers and these are the main starting points when an irradiation campaign is prepared to test and qualify an electronic device. Most important standards are: JESD89A [116], JESD57A [174], JESD234 [178], ASTM F1192 – 11 (2018) [179], ESA/SCC 25100 [177], MIL-STD750-1 [180], MIL-STD-883F [181], NASA/DTRA [182].

## 2.4 Error Mitigation Techniques

Harsh environments with radiation background may cause too many failures in electronic devices leading to mission and/or experiment failure and cancelation. To be able to operate sensors and electronics in such environments people have been investigating various radiation-hardening techniques in order to mitigate or minimize the radiation-induced effects in electronic devices. The radiation-hardening techniques are classified in two categories: physical level and logical level radiation hardening.

### 2.4.1 Technological Solutions for Radiation-Hardening

Physical radiation-hardening processes are using various physical approaches such as: increasing the spacing between transistors, insulating substrates, adopting radiation-tolerant devices, shielding the wafers etc.

The usage of insulating substrates instead of a semiconductor one, increases the radiation hardness of electronic devices. Usually, two types of insulators are used: silicon on insulator (SOI) and silicon on sapphire (SOS). By using the SOI technique, a layer of silicon-insulator-silicon substrate is adopted to replace the conventional silicon substrate. This will improve the device performance by means of reducing the device parasitic capacitance due to the fact that the silicon junction is located above the electrical insulator. Therefore, the most important benefits of using SOI technology are: low parasitic capacitance and resistance to SELs due to complete isolation of p- and n-well structures [183]. SOS is a hetero-epitaxial process from SOI family used to manufacture electronic devices and consist of a thin silicon layer grown on top of a sapphire wafer. The usage of sapphire enhances the radiation tolerance of electronic devices, due to its excellent electrical insulation properties which prevents any radiation-induced stray currents to be propagated in the circuit. It is mainly used in aerospace and military; however, its fabrication process is complex and expensive. Although the usage of SOI increase the immunity to SEE, TID-induced increase of leakage currents may still be present [184].

To mitigate the electronic devices against SEL, usually, designers adopt some layout techniques to reduce the probability of activating the SCR structure in the CMOS structure. One can be done by increasing the spacing between the PMOS and the NMOS transistors

resulting in a decrease of the gain for at least one of the parasitic bipolar. However, this may add a drawback to the overall layout as the increase in the spacing comes with the reduction of the component density. Another way to act against the parasitic SCR structure is to decrease the bias of the parasitic transistor by increasing the well and the substrate doping concentrations. This will result in an increase of  $R_w$  and  $R_s$  reducing the bias current of the parasitic transistors. [185]

Shielding the device dice with depleted Boron that is the isotope Boron-11, may be a solution to increase the radiation tolerance of semiconductor devices. Borophosphosilicate glass, (BPSG) is used as a passivation layer to shield the semiconductor dice [186].

## 2.4.2 Radiation Hardening at Logic Level

Radiation hardening at the logic level adopts various techniques to minimize the radiation impact on the functionality of the device such as: redundant structures, watchdog timers and memory-error correcting procedures. Redundant structures may be implemented to reduce the error rates in logical elements and to enhance the system reliability. The most common technique is the usage of triple modular redundancy (TMR) which involves the triplication of the critical areas in the user logic. Hence, by using a majority voter, some errors may be masked in such way, ensuring a good functionality of the device [187]. However, the main drawback of such technique is the fact that it is using three time more logic resources.

A watchdog timer scheme can be implemented to monitor the normal operation of a device such as a processor and to perform a hardware reset if some sequence is not executed [188].

In general, complex devices such as processors, FPGAs, system-on-chips (SOCs) or microcontrollers as well as RAM devices embed various protection algorithms against software errors by using error correcting codes (ECC) either provided as they are by the vendors or by using customized versions developed by the users themselves [189].

## 2.5 Particularities of the Radiation Environment in LHCb-RICH

In some respects, the radiation environment at the LHC is different than the environment for space applications. Due to proton-proton or ion-ion collisions in the LHC detector caverns, a mixed and complex radiation field is generated and is consisting of various particles like: charged and neutral hadrons (light ions, protons, neutrons, kaons and pions), electrons, photons and muons. This mixed field will affect the life-time and the functionality of the electronic devices operating in the LHC environment as well in its experiment sites.

The LHC radiation environment relevant to establish the reliability of the electronic devices is described by three factors:

- ❖ the expected TID;
- ❖ the expected high energy hadrons (HEH) fluence;
- ❖ the expected 1 MeV equivalent neutrons fluence.

The high energy hadrons are defined as all hadrons which have kinetic energy equal or above 20 MeV. Only the charged hadrons above 20 MeV are considered to be effective in inducing SEEs into electronic devices as they have about similar nuclear interaction cross-sections. With the decrease of the energy, below 20 MeV, the nuclear interaction cross-section decreases abruptly and, in some cases, the charged hadron might not be able to penetrate the device package to hit the semiconductor area. As there are various shielding structures made of concrete/lead/iron present in the LHC tunnel a significant thermal neutron fluence is expected.

With the starting of the RUN 3, the LHCb-RICH sub-detectors will operate at higher frequencies in order to acquire more data from ultra-high energy particle collisions. During RUN 3 it is expected to reach  $50 \text{ fb}^{-1}$  total integrated luminosity at the level of LHCb detector, over its approximately 7000 h of operation. Therefore, to estimate the expected radiation environment in RICH 1 and RICH 2 regions, various simulations and models have been studied using dedicated programs like FLUKA. Following the simulations presented here [190] it has been established that the worst case scenario values are in the RICH 1 region, as is much closer to the interaction point than RICH 2. In table 2.2 are given the expected radiation levels, including a safety factor of 2, for the RICH 1 region as well as the approximate dose rate in 7000 h of operation.

**Tab. 2.2** *Worse case-scenario radiation levels at the RICH 1 region [191]*

| <b>Region</b> | <b>TID<br/>[krad]</b> | <b>Hadrons (HEH):<br/>&gt; 20 MeV [cm<sup>-2</sup>]</b> | <b>Neutrons:<br/>1 MeV <math>n_{eq}</math> [cm<sup>-2</sup>]</b> | <b>Dose rate<br/>[rad/s]</b> |
|---------------|-----------------------|---------------------------------------------------------|------------------------------------------------------------------|------------------------------|
| <b>RICH 1</b> | 200                   | $1.2 \cdot 10^{12}$                                     | $3 \cdot 10^{12}$                                                | 0.008                        |

The presence of HEH in the LHCb radiation environment may induce, via nuclear reactions with the silicon material from electronic devices, a maximum LET of around  $15 \text{ MeV} \cdot \text{cm}^2/\text{mg}$  [175]. Therefore, the Si-based devices need to have the SEE threshold LET above  $15 \text{ MeV} \cdot \text{cm}^2/\text{mg}$ , especially for potentially destructive SEEs like SELs. In some cases, a device with the SEU threshold LET below  $15 \text{ MeV} \cdot \text{cm}^2/\text{mg}$  may be accepted if the SEU rate is low and errors can be mitigated without complicating the overall design of the system.

Based on these numbers, all the electronics, sensors, optic devices, and mechanical structures must be resilient to such radiation levels, in order to ensure good functionality with very low error rates during the operational runs. The most sensible part in the whole LHCb-RICH readout electronics chain is the commercial-grade SRAM-based FPGA. It is the main core of the PDMDB, with its main purpose to read out the trigger signals from the front-end boards. The reliability of this FPGA has been a key topic in the preparation of the LHCb-RICH Upgrade Phase Ia program. It was intensively tested in various radiation environments to simulate and extrapolate its behavior to the expected LHCb-RICH radiation levels. Therefore, its response to radiation is presented in chapter 4.

In order to have a backup solution for the SRAM-based FPGA in case its resilience to LHCb-RICH radiation environment is questionable, another FPGA technology, has been also tested and its behavior is presented in chapter 5.



## Chapter 3

# Characterization of the SPACIROC2 ASIC Under Radiation Exposure

The **S**patial **P**hotomultiplier **A**rray **C**ounting and **I**ntegrating **R**eadout **C**hip (SPACIROC) [192] family is a mixed signal and full readout front-end ASIC family designed to fulfill the needs of compatibility with photomultiplier tubes, being optimized for 64-channel MaPMTs. Most of its analog blocks are inherent from the third generation of **M**ulti-**A**node **R**ead**O**ut **C**hip (MAROC) family [193], a family initially proposed to be used also as front-end readout on the LHCb-RICH [80].

The SPACIROC family was designed to meet the requirements of the **J**oint **E**xperiment **M**issions for **E**xtrême **U**niverse **S**pace **O**bservatory (JEM-EUSO) in terms of photodetector front-end readout. The JEM-EUSO space-based mission [28] is a 5-years experiment onboard at the ISS with the purpose of detecting and measuring Ultra-High Energy Cosmic Rays (UHECRs) by using the Earth's atmosphere as a calorimeter together with a fluorescence telescope. It will be the first experiment which takes data from both hemispheres ensuring in this way a full-sky coverage, due to the ISS trajectory orbit. The data taking will be on the dark side of the Earth and will consist in the detection of UV photons emitted from the extensive air showers caused by UHECRs with energy above  $10^{18}$  eV [194]. By detecting, analyzing and reconstructing UHECR events, it can lead to a better understanding of the Universe as well as to evidence of new fundamental physics and new astronomy which could be found and studied.

To detect UV photons, the JEM-EUSO uses a fluorescence telescope with a focal surface consisting of approximately 5000 64-channel MaPMTs, R11265-030-M64 type [94], summing up together approximately 300 k pixels to be read out [195]. The MaPMTs are arranged in groups of four in ECs, and then each group of nine ECs forms PDMs. All the PDMs are arranged in a detection plane with a focal surface of  $4.4 \text{ m}^2$ .

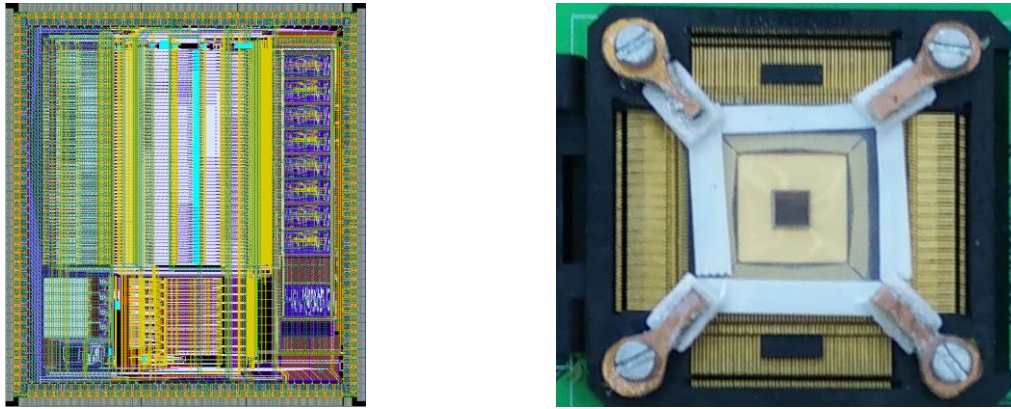
The MaPMT readout is implemented with the third generation of the SPACIROC ASIC family [196], a custom 64-channel and radiation hard chip, one for each MaPMT. The ASICs

are expected to accumulate a TID of 30 krad over the whole 5-years operation [197]. SEE may be triggered inside the chip either by protons up to a LET of  $15 \text{ MeV} \cdot \text{cm}^2/\text{mg}$  or by ions from cosmic rays which can have an LET between  $0.01 \text{ MeV} \cdot \text{cm}^2/\text{mg}$  and  $40 \text{ MeV} \cdot \text{cm}^2/\text{mg}$  [149].

Therefore, in this chapter a complete reliability analysis will be presented and the results will be extrapolated to the JEM-EUSO as well as LHCb-RICH radiation environments.

### 3.1 SPACIROC2 ASIC Description

The SPACIROC2 ASIC has been designed by Omega MICRO group [198] in close collaboration with JEM-EUSO group. It was fabricated in a  $0.35 \mu\text{m}$  SiGe BiCMOS technology node with an active area of almost  $19 \text{ mm}^2$  ( $4.6 \text{ mm} \times 4.1 \text{ mm}$ ). Its layout as well as a photo of the ASIC in its naked package can be seen in fig. 3.1.



**Fig. 3.1** SPACIROC2 layout (left side) [199] and a photo of its die in a naked package (right side)

SPACIROC2 has 64 inputs with negative polarity compliant with MaPMT readout requirements. Assuming that the MaPMT gain is  $10^6$ , then there is an average charge of 160 fC needed to have one detected photoelectron (1 p.e.). The main features of the SPACIROC2 are listed below:

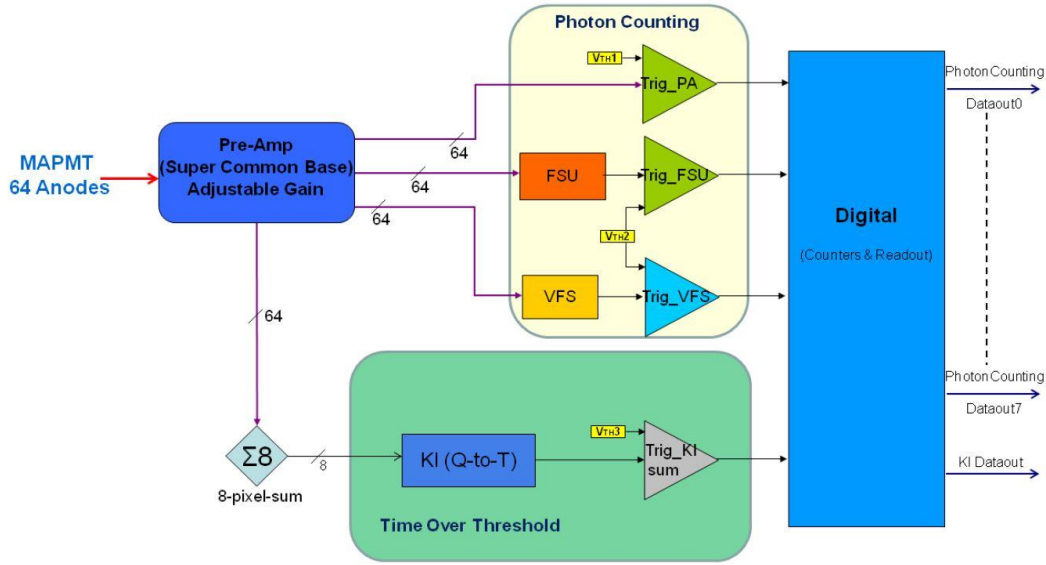
- ❖ 64-channel preamplifier, with 8-bit gain control for each channel;
- ❖ 64-channel photon counting;
- ❖ Charge to time (Q-to-T) converter on 8 internal blocks with multiplexed inputs;
- ❖ 100 % trigger efficiency for a measured charge higher than 50 fC ( $\sim 1/3$  p.e.);
- ❖ Q-to-T converter range: 2 pC – 200 pC (12.5 p.e – 1250 p.e.);
- ❖ Double pulse separation of 10 ns;
- ❖ Power consumption of  $\sim 1\text{mW}/\text{channel}$ ;
- ❖ Increased tolerance against radiation-induced SELs and SEUs at the hardware level.

The general architecture of SPACIROC2 ASIC, shown in fig. 3.2, embeds the following functional sections: the super common base preamplifier, the photon counting block, the Q-to-T converter and the digital block.



The 64 analog signals corresponding to the MaPMT channels are fed into the wideband current preamplifiers and, if needed, the non-uniformity of each signal can be corrected with the programmable gain. Due to its super common base structure, a low impedance of  $\sim 100 \Omega$  as well as a low quiescent current are ensured. These features are important to minimize the crosstalk as well as power consumption. The 64 outputs from the preamplifier are distributed to the photon counting block and Q-to-T converter.

Due to the fact that the SPACIROC2 is a prototype ASIC to the final version, the photon counting block has three individual and different types of discrimination used to generate the photon triggered signals: Trig\_PA, Trig\_FSU and Trig\_VFS. The Trig\_PA discriminator takes the signal directly from the preamplifiers (PA) and due its simple architecture it has the lowest power consumption, with respect to the other two trigger generation blocks. The Trig\_FSU discriminator takes the signal from a fast shaper unipolar (FSU) block which is a low-noise charge sensitive amplifier with adjustable gain and shaping time. The Trig\_VFS discriminator contains a very fast shaper (VFS) block, and it has more gain and shaping time than the TRIG\_FSU. The performances of all three-trigger generation blocks were evaluated either in laboratory and/or during irradiation tests, in order to choose the best trigger generation solution for the final version of the ASIC. Two 10-bit DACs are used to set the trigger thresholds. One is shared between TRIG\_FSU and TRIG\_VFS and one is used for TRIG\_PA.



**Fig. 3.2** SPACIROC2 general architecture [199]

The Q-to-T converter offers charge measurements within a range of 12.5 - 1250 p.e. and its principle is based on Time Over Threshold (TOT) technique. Each 8 neighbouring channels are summed and fed to the input of the TOT block, inside Q-to-T converter. The TOT output is discriminated over a given threshold set by an additional 10-bit DAC.

With respect to the MAROC3 ASIC, the digital block of SPACIROC2 has a more complex circuitry which embeds: 8-bit Gray counters, two state machines, four 10-bit DACs, multiplexors and logic gates, plus 9 serial data outputs. The photon-counting and Q-to-T converter sections are controlled by these two state machines. All the readout and data

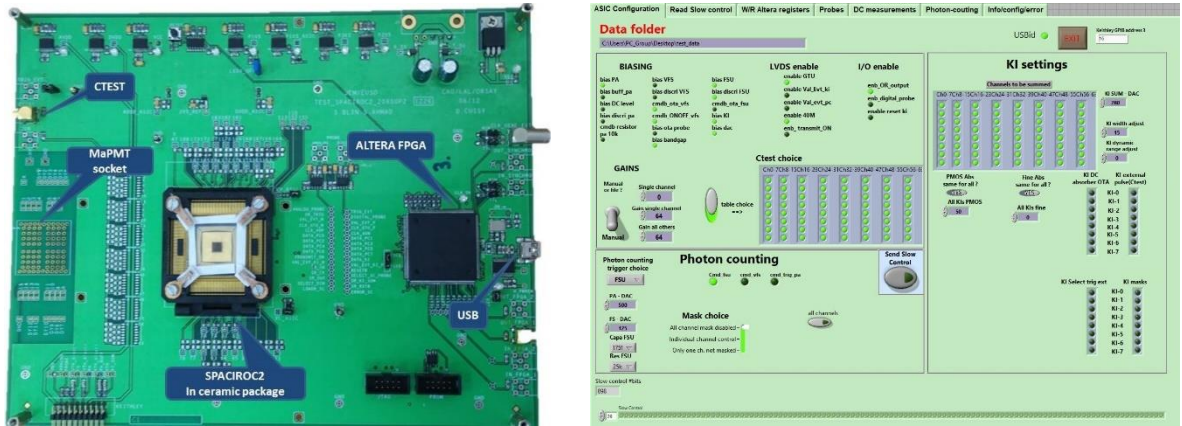
acquisition are done within a well-defined time interval of 2.5  $\mu\text{s}$ , defined as Gate Time Unit (GTU).

The SPACIROC2 ASIC is controlled by 897 bits organized as slow control parameters. To mitigate against radiation induced SEUs, each bit from the slow control routine has implemented a triple modular redundancy with a majority voter [200]. In this way some of the SEUs which may be induced are masked, hence the overall SEU rate is reduced.

The SPACIROC2 analog layout has been designed to be tolerant against SELs by using two mitigation techniques [200]. One was by increasing physically the distance of the inherent bipolar parasitic transistors due to a larger space between the PMOS and NMOS transistors. In this way the positive feedback gains will be reduced, hence the SEL probability will be lower. Another technique was applied and consists in enlarging the power supply contacts of each substrate, and ensuring in this way a reduction of the resistivity, respectively, preventing in this way the bias of the parasitic transistors by increasing the resistance of the parasitic feedback resistors.

This strategy of prevention against SELs has not been applied to the digital layout, due to design constraints. However, some external mitigation was ensured by adding a 50  $\Omega$  current limiting resistor in series with the digital power supply rail.

To evaluate and characterize the SPACIROC2 ASIC performances, a test board designed by the Omega group was fully assembled within our group from IFIN-HH, see the left side of fig. 3.3. The ASIC comes in ceramic package with the top lid being detachable. The test board is configured by using a LabVIEW graphical user interface (GUI) provided by the Omega group and is shown in the right side of fig. 3.3. An FPGA is used to pass the configuration to the ASIC as well as to perform the readout.

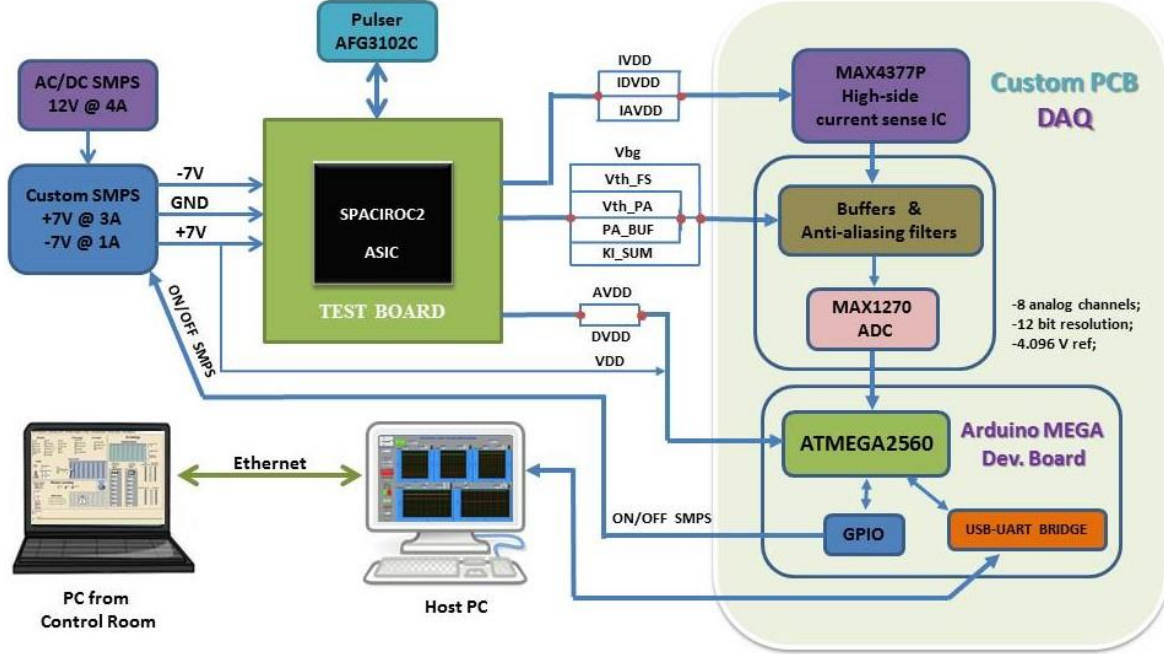


**Fig. 3.3** SPACIROC2 test board (left side) and its LabVIEW GUI for configuration (right side) [198]

## 3.2 Experimental Setup and Testing Routines

An experimental setup in compliance with the radiation testing standards has been proposed and designed to power, monitor and characterize the SPACIROC2 ASIC – named the DUT from now on within this chapter – while performing laboratory tests as well as under ionizing

radiation conditions [201]. Its architecture is shown in fig. 3.4, and the entire work was carried out within the *Laboratory for Radiation and Aging Effects in Electronic Devices* (LaRA EED) from IFIN-HH [202].



**Fig. 3.4** The experimental setup architecture designed to characterize the SPACIROC2 -self citation [201]

The experimental setup is completely automatic and is composed from the following sections: power supply block, the DAQ system, the DUT test board, an arbitrary wave generator (AWG) as a pulser, and two computers.

The DUT test board was designed by the DUT design team, and it was implemented the design of the PCBs with very minor modifications in IFIN-HH. The DUT was placed on a socket, ensuring an easy replacement of the DUT when needed.

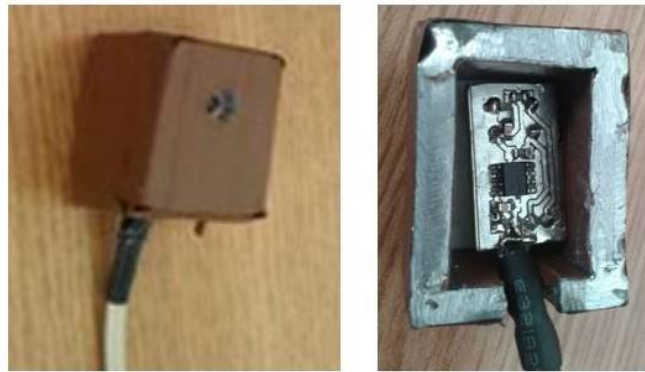
An AWG was used to generate a test pulse to be injected in the test board in order to simulate a 1 p.e. signal needed for trigger efficiency measurements. All the connections concerning the power, monitoring and control signals to the DAQ system were made with multicore and screened cables, to prevent any background noise for small amplitude signals.

The power supply block ensures the power requirements for powering the DUT test board by providing two independent voltages of +7 V at a current of 3 A and -7 V at a current of 1 A with respect to the ground (GND). These power supplies are switching mode and they can be enabled/disabled together by the user at a given condition.

The DAQ system is designed around a commercial development board which embeds the ATMEGA2560 8-bit microcontroller [203]. The whole control and operation routines are made around this microcontroller which is responsible for various tasks like: power management, communication with host PC and controlling the DAQ board. The DAQ board was designed to monitor up to 24 analog input channels from which 16 are 10-bit capable and are embedded in the ATMEGA2560 and the rest of 8 are external channels with 12-bit resolution provided

by an external high-speed ADC, MAX1270 [204]. The external channels are used to monitor low amplitude and important signals while the others are for monitoring less important voltages and/or with higher amplitudes. Up to 12 analog inputs are used to monitor the DUT power activity, and all of them before being digitized pass through a signal conditioning block consisting of voltage buffers and anti-aliasing filters. For current measurements, high-side current shunt amplifiers, MAX4377 [205], are used to convert the current flow through a shunt resistor into a voltage.

The DUT die temperature was monitored by using a non-contact temperature sensor, MLX90614 [206], which is used since its naked die package allows direct infrared measurement. The sensor was placed in a 5 mm Lead shield, as it can be seen in fig. 3.5.



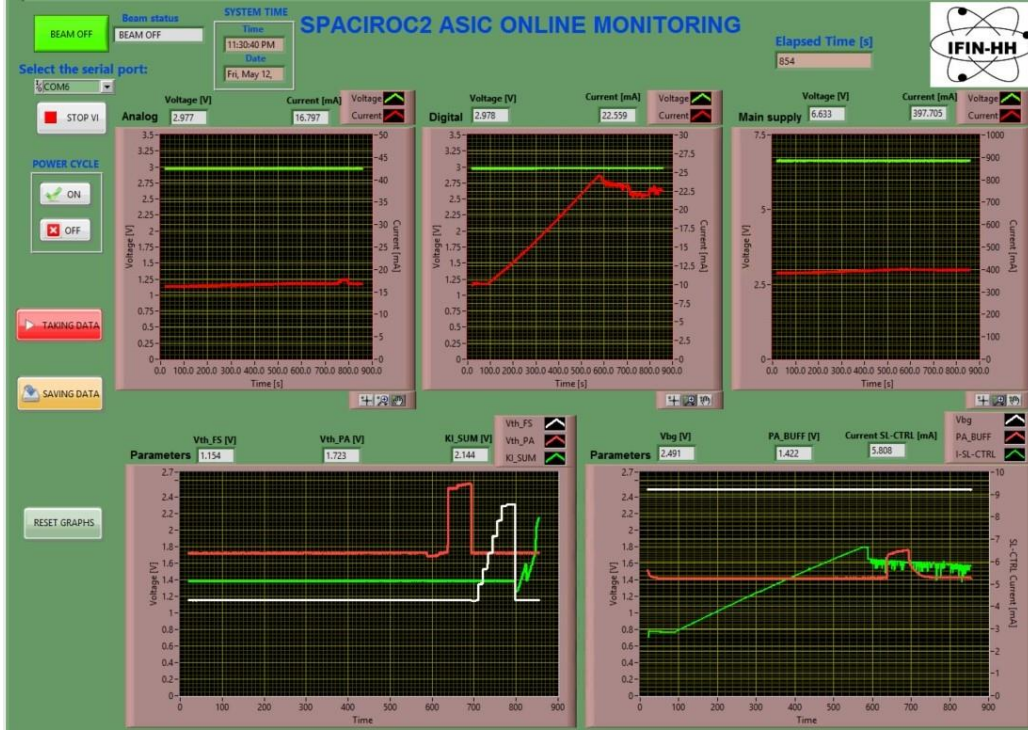
**Fig. 3.5** *MLX90614 and its 5 mm lead case to monitor the SPACIROC2 die temperature -self citation [201]*

The DAQ system is connected through an UART communication to the host PC where a LabVIEW GUI, shown in fig. 3.6, runs and ensures full control of the experimental setup. The measured data is plotted on graphs and saved in ASCII files for later analysis. The sampling rate is 50 ms. Another PC located in the control room is used to control the host PC located inside the experimental area during irradiation tests.

The top graphs from GUI are displaying the power consumption of analog and digital power rails together with the main test board power consumption. The bottom plots are dedicated to various internal parameters of interest which describes to functionality of the device. The user can perform at any time a power-cycling procedure of the device. Each new data saved in the ASCII file contains a time stamp and a flag indicating whether the particle beam was “on” or “off”. This allows a consistent and coherent analysis of the saved data to extract the SEE rates and cross-sections together with a parametrization of the cumulative effects.

The monitoring strategy as well as the testing routines before, during and irradiation were established together with the DUT design team. In this way a compressive set of electrical parameters and characteristics of the DUT were collected. Therefore, based on data collected while the device was irradiated as well as after the irradiation, the cumulative effects measurements and SEE rates were highlighted in user display and recorded on the hard-disk.





**Fig. 3.6** The LabVIEW GUI designed to control and monitor the experimental setup

The cumulative effects in a  $0.35\ \mu\text{m}$  SiGe BiCMOS device are parametrized through measurements of a cumulative drain leakage currents induced in the NMOS transistors [207]. Since the analog core of the DUT has a majority of heterojunction bipolar transistors (HBT), the TID-induced leakage currents are expected to be lower compared to the DUT digital core as the HBTs show good TID resilience compared with the NMOS transistors [207]. However, the increase in leakage currents may combine with partial or full functional failures of other internal blocks due to TID-induced voltage shifts, e.g. in the DACs output voltage. These can be mitigated following an annealing process after irradiation with the DUT being biased and configured as in normal operation.

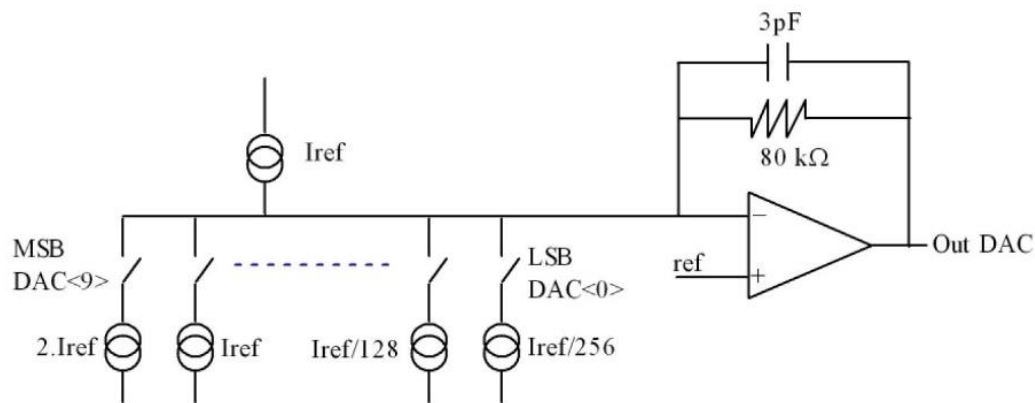
The detection of SEE is a more complex process as it involves multiple parameters to be monitored and checked simultaneously. To detect radiation-induced SELs the power consumption on the DUT analog and digital cores is monitored. Also, as part of the digital core, the power consumption on the slow control configuration section is monitored separately. Therefore, if during irradiation an abrupt increase in current is detected, and if this increasing is not corrected by a complete reconfiguration of the DUT, then the next step is to perform a power cycle of the DUT. If the device recovers after a power cycle, e.g. the current increase disappeared, then a radiation-induced SEL was induced in the DUT. However, if the DUT is not recovering after these steps and the current increase is still present, there is a probability that the device has a permanent SEE which has to be further investigated. The increase of power consumption within the DUT rise its power dissipation and can be correlated with die temperature measurements.

By doing a readback operation of the slow control configuration registers, the SEU rate is counted. The presence of the SEUs in the slow control registers may put the DUT in an unknown state which can cause damage to its internal blocks as well as its external components

on the test board. However, the SEUs in the slow control configuration registers can be mitigated by a full reconfiguration of the DUT without the need of a power cycle.

Due to the fact that the TID may induce functional failures in various key blocks of the DUT, a compressive analysis of the internal DAC parameters variation will be carried after each irradiation step to establish if DAC linearity was preserved and to check its response to various digital input codes.

To understand better how the DACs may be affected by TID, a better view of its structure is required. In fig. 3.7 is given the basic architecture of a 10-bit transimpedance DAC which is embedded in the SPACIROC ASIC. There are 10 NMOS current mirrors which inject currents into the transimpedance amplifier to be converted into voltage, i.e. into the DAC output voltage. Since the NMOS transistors from the current technology node, 0.35  $\mu\text{m}$  SiGe BiCMOS, are very sensitive to TID, any induced leakage currents as well as combined with some gate-to-source voltage shifts of the NMOS current mirrors may affect the reference current corresponding to a bit of data and can be a major contributor of failures in such DACs. The transimpedance amplifier may be also a source contributor to DAC failures as it can generate an offset voltage at its inputs which can in turn be translated as a voltage shift to DACs output voltage over the whole range with respect to its baseline values. The corresponding NMOS current mirrors of the lowest significance bits – those with the very small current ratios – are the first to induce visible radiation-induced effects, hence the minimum output voltage of the DAC may be positive shifted as a consequence of TID.



**Fig. 3.7** SPACIROC2 internal DACs architecture [200]

The trigger efficiency for Trig\_FSU trigger generation block was measured by injecting a known charge into the DUT analog blocks with the pulser. Then by sweeping the DAC2 values over its entire range, the signal is discriminated by the Trig\_FSU and depending on the input signal amplitude it will generate trigger signals if the threshold condition is satisfied. The plot is known as S-curves and it shows the cumulative distribution function of the probability for a given number of channels to generate a trigger. The tests were done by injecting the minimum charge which should generate 100 % trigger efficiency, i.e. 50 fC corresponding to 1/3 p.e. Based on the results after each irradiation step as well as by comparing with the reference data taken before, anomalies in the trigger efficiency measurements were highlighted. These anomalies include: negative threshold shifts or decreasing of the trigger efficiency. The failures

recorded into the trigger efficiency are strongly correlated with the failures observed in the DACs, as these fail to provide a requested threshold to the trigger generation blocks.

In table 3.1 are given the parameters and tests which were monitored before, after and during irradiation. However, some parameters were not monitored at the beginning of the irradiation campaign but were introduced later in the next irradiation sessions. The DAQ system monitors the DUT parameters with a resolution of 1 mV for voltage signals respectively 0.01 mA for current signals.

**Tab. 3.1** *The list of parameters which were measured before, during and after irradiation of the DUT*

| Before and after irradiation                                             | During irradiation                                                       |
|--------------------------------------------------------------------------|--------------------------------------------------------------------------|
| Power consumption on the main power rail                                 | Power consumption on the main power rail                                 |
| Power consumption on the analog power supply                             | Power consumption on the analog power supply                             |
| Power consumption on the digital power supply                            | Power consumption on the digital power supply                            |
| Power consumption on the slow control section (part of the digital core) | Power consumption on the slow control section (part of the digital core) |
| Internal voltage reference (Vbandgap)                                    | Internal voltage reference (Vbandgap)                                    |
| DAC1 voltage output (Vth_Trig_PA)                                        | DAC1 voltage output (Vth_Trig_PA)                                        |
| DAC2 voltage output (Vth_Trig_FS)                                        | DAC2 voltage output (Vth_Trig_FS)                                        |
| DAC3 voltage output (Vth_Trig_Ki_Sum)                                    | DAC3 voltage output (Vth_Trig_Ki_Sum)                                    |
| Preamplifier analog probe (PA_BUFF)                                      | Preamplifier analog probe (PA_BUFF)                                      |
| Die temperature                                                          | Die temperature                                                          |
| DAC analysis                                                             | Slow control registers readback                                          |
| Trigger Efficiency for Trig_FSU                                          |                                                                          |
| Slow control registers readback                                          |                                                                          |

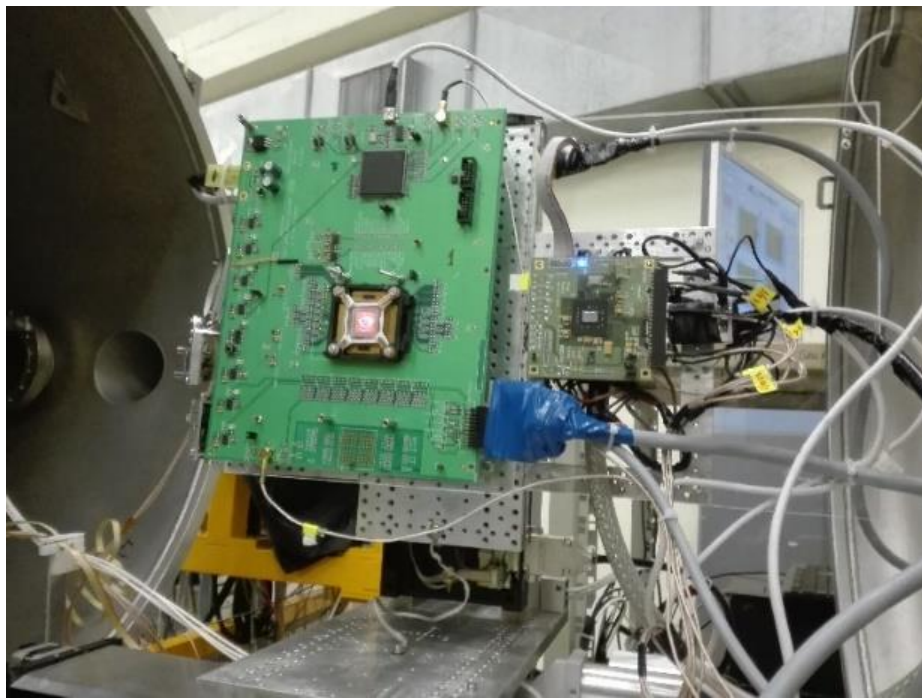
### 3.3 Test Beam Results and Analysis

The SPACIROC2 ASIC was tested in radiation by using ions, protons and X-rays particle beams from the following facilities:

- ❖ Ions at SIRAD [208] facility from Legnaro National Laboratories in Italy;
- ❖ 200 MeV protons at the proton irradiation facility (PIF) [209] at the Paul Scherer Institute in Switzerland;
- ❖ 35 MeV protons at the 2.88 GeV Cooler Synchrotron COSY-Jülich [210] at Juelich Research Center in Germany;
- ❖ 50 keV X-rays at the X-ray radiation facility [211] from Padova University in Italy.

### 3.3.1 Ion Irradiation

The ion irradiation was carried out in a vacuum chamber to reduce the ion energy loss in the air and to protect the beam-pipe vacuum. Inside the vacuum chamber the test board was installed on a dedicated sample holder with all of its connectors regarding - power, control and monitoring - being linked the DAQ system through vacuum pass-through connectors as shown in fig. 3.8. The sample holder has the ability to rotate the test board with respect to the beam up to  $50^\circ$  on the X-axis in order to increase the effective LET. Several tests were performed before starting the irradiation to get the baseline data as well as to check the connectivity of the whole setup.



**Fig. 3.8** The DUT test board mounted on the sample holder inside the vacuum chamber

Two DUT test boards were tested in various runs with  $^{16}\text{O}$  and  $^{20}\text{Si}$  ion beams having 108 MeV respectively 157 MeV kinetic energy per particle and using different particle fluencies. The base LET for  $^{16}\text{O}$  is  $(2.85 \pm 0.29) \text{ MeV} \cdot \text{cm}^2/\text{mg}$  and  $(8.59 \pm 0.86) \text{ MeV} \cdot \text{cm}^2/\text{mg}$  for  $^{20}\text{Si}$ , however by tilting the device to  $20^\circ$ ,  $40^\circ$  and  $50^\circ$  it was possible to increase the effective LET. In total, 10 runs were carried out on two test boards with various effective LET values and the particularities for each run are given in table 3.2.

Due to the fact that the DUT placed on a test board, TB1, had an  $\sim 100 \mu\text{m}$  thick plastic foil on top of the DUT die as a protective layer, the effective LET was higher than the one delivered by the particle beam, as the foil slowed down the ions resulting in an increase of the LET. Hence only the TB3 results are presented in this chapter.

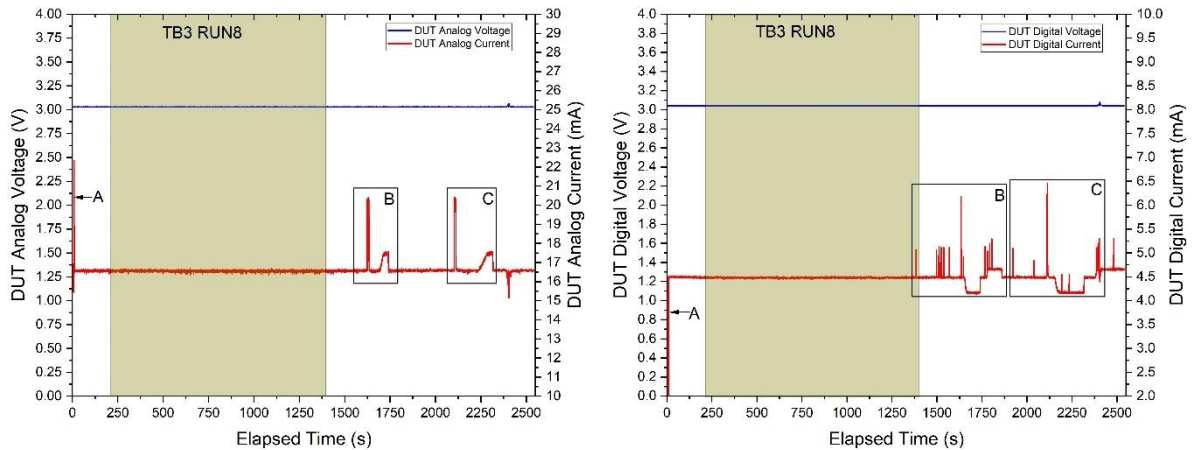


**Tab. 3.2** The DUT ion irradiation runs

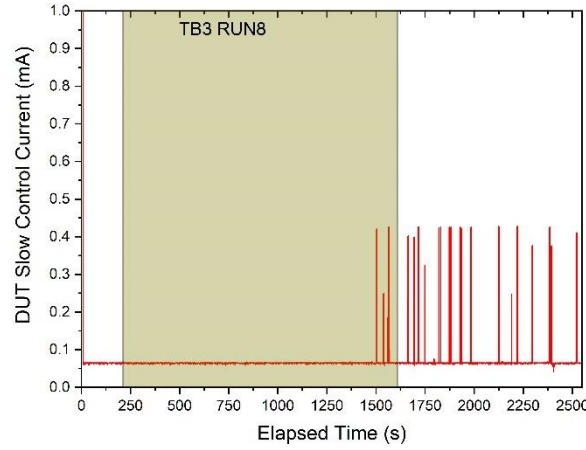
| Run Nr. | Test Board | Ion Species      | Angle (°) | Effective LET (MeV · cm <sup>2</sup> /mg) | Fluence (20% error) (ions/cm <sup>2</sup> ) |
|---------|------------|------------------|-----------|-------------------------------------------|---------------------------------------------|
| 1       | TB1        | <sup>16</sup> O  | 0         | 2.85 +/- 0.29                             | (1+/-0.2) · 10 <sup>5</sup>                 |
| 2       | TB1        | <sup>16</sup> O  | 0         | 2.85 +/- 0.29                             | (1+/-0.2) · 10 <sup>6</sup>                 |
| 3       | TB1        | <sup>16</sup> O  | 0         | 2.85 +/- 0.29                             | (1+/-0.2) · 10 <sup>7</sup>                 |
| 4       | TB1        | <sup>16</sup> O  | 40        | 3.7 +/- 0.37                              | (1+/-0.2) · 10 <sup>7</sup>                 |
| 5       | TB1        | <sup>16</sup> O  | 20        | 3.03 +/- 0.3                              | (1+/-0.2) · 10 <sup>7</sup>                 |
| 6       | TB3        | <sup>16</sup> O  | 40        | 3.7 +/- 0.37                              | (1+/-0.2) · 10 <sup>7</sup>                 |
| 7       | TB3        | <sup>16</sup> O  | 20        | 3.03 +/- 0.3                              | (1.5+/-0.3) · 10 <sup>7</sup>               |
| 8       | TB3        | <sup>16</sup> O  | 50        | 4.45 +/- 0.45                             | (1.5+/-0.3) · 10 <sup>7</sup>               |
| 9       | TB3        | <sup>20</sup> Si | 0         | 8.59 +/- 0.86                             | (1.265+/-0.25) · 10 <sup>6</sup>            |
| 10      | TB3        | <sup>20</sup> Si | 40        | 11.15 +/- 1.1                             | (1.1+/-0.22) · 10 <sup>6</sup>              |

At an LET of (4.45 +/- 0.45) MeV · cm<sup>2</sup>/mg done with <sup>16</sup>O ions and with the device tilted at 50° - 8<sup>th</sup> irradiation run - no radiation-induced events were observed. No SEUs were seen, this may be due either the very good efficiency of the hardware TMR structure implemented in the slow control configuration registers or the SEU threshold LET is higher. After this run, the DUT functionality was completely normal.

In the following figures are presented the measurements of the DUT electrical parameters during and after the 8<sup>th</sup> irradiation run. In fig. 3.9 are given the measurements of the power consumption on both analog and digital power rails connected to the DUT. Also, the individual monitoring of the power consumption on the slow control section part of the digital block is shown in fig. 3.10.

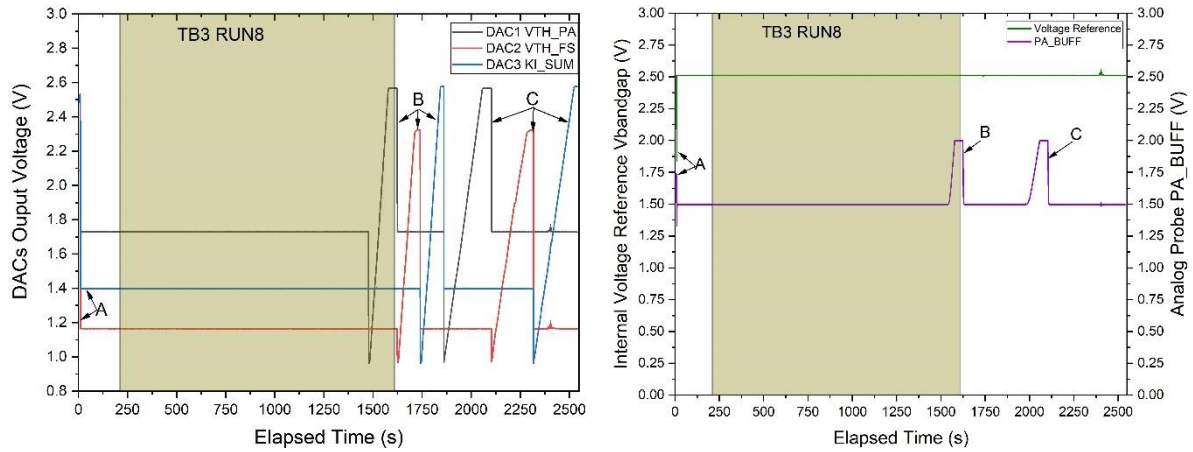


**Fig. 3.9** DUT power consumption on the analog (left side) and digital (right side) blocks during 8<sup>th</sup> irradiation run



**Fig. 3.10** DUT power consumption on the slow control section part of the digital block during 8<sup>th</sup> irradiation run

The output voltages of the internal DACs were monitored during the irradiation run and their measurements can be seen in the left side of fig. 3.11. In the right side of fig. 3.11 the internal voltage reference together with the preamplifier analog measurements as additionally signals to the DUT functionality were monitored.

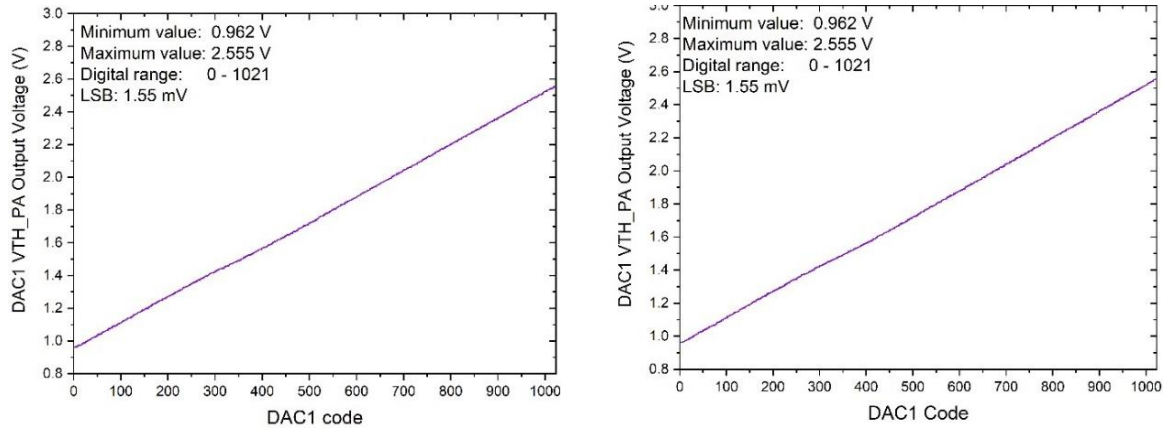


**Fig. 3.11** Measurements of DUT output voltages corresponding to its three internal DACs (right side) and internal voltage reference together with the preamplifier analog probe (right side) during 8<sup>th</sup> irradiation run

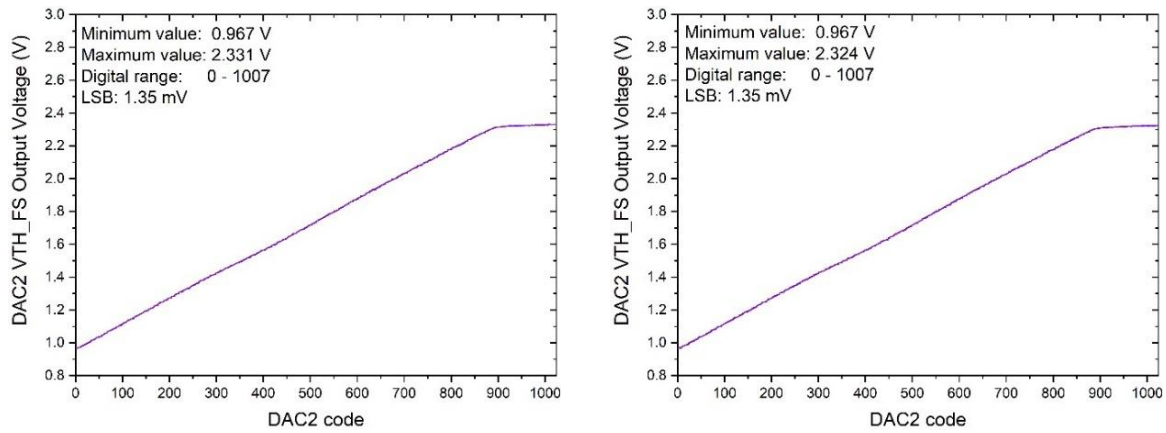
To understand better these figures, several events were highlighted on the plots and which are correlated with various states of the DUT as described below:

- ❖ **State A:** this state describes the DUT in an unconfigured state after the power-up. During this state the DUT is placed in an unknown state with most of its internal blocks unconfigured, hence the high and unstable power consumption. After configuration the DUT stays in a stable state being ready for operation.
- ❖ **State B:** this state is correlated with the DAC analysis measurements either for one or for all DACs (the DUT is configured).
- ❖ **State C:** this state is correlated with the trigger efficiency measurements (the DUT is configured).

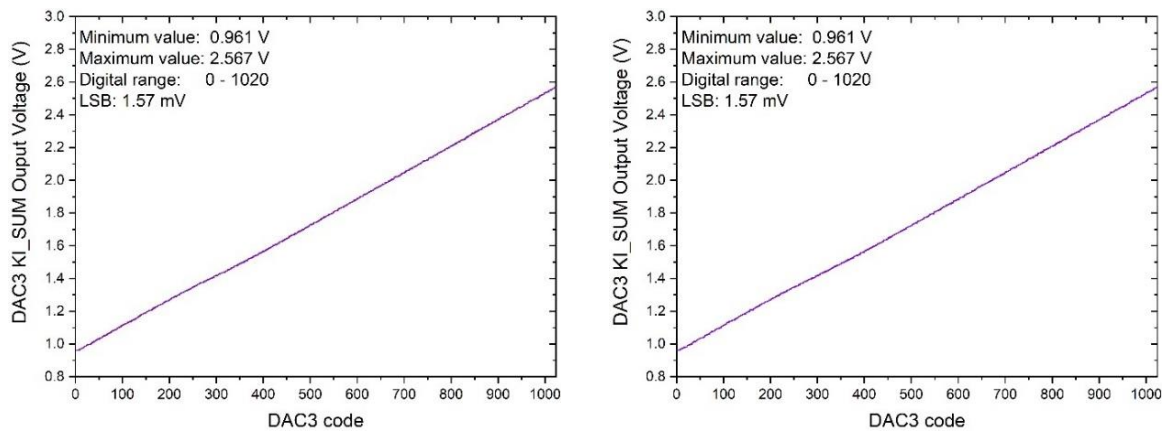
The linearity of each internal DAC was measured after the irradiation run and it was compared with the measurements done before and no errors were seen. The measurements are given in fig. 3.12 for DAC1, in fig. 3.13 for DAC2 and in fig. 3.14 for DAC3.



**Fig. 3.12** DUT DAC1 linearity measurements before irradiation (left side) and after the 8<sup>th</sup> irradiation run (right side)

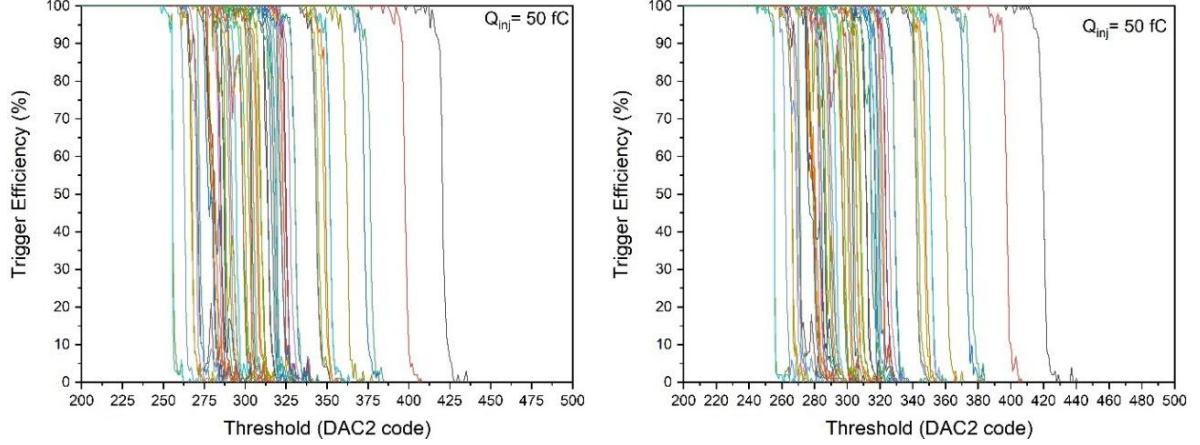


**Fig. 3.13** DUT DAC2 linearity measurements before irradiation (left side) and after the 8<sup>th</sup> irradiation run (right side)



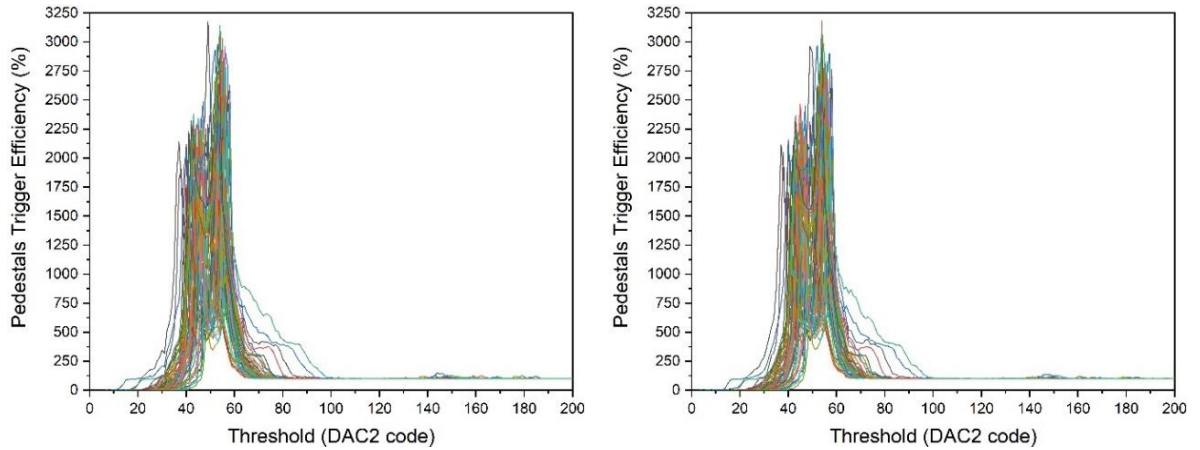
**Fig. 3.14** DUT DAC3 linearity measurements before irradiation (left side) and after the 8<sup>th</sup> irradiation run (right side)

The trigger efficiency was measured by sweeping the DAC2 values over its entire range and by injecting a 50 fC charge corresponding to 1/3 p.e. In fig. 3.15 the S-curves measurements are shown before and after the irradiation run, with only the Trig\_FSU trigger generation block used during this check. No failures were observed as the DAC2 range on which the S-curves were detected was constant in both cases.



**Fig. 3.15** DUT Trig\_FSU trigger efficiency measurements for all 64 channels with 50 fC input charge before (left side) and after 8<sup>th</sup> irradiation run (right side)

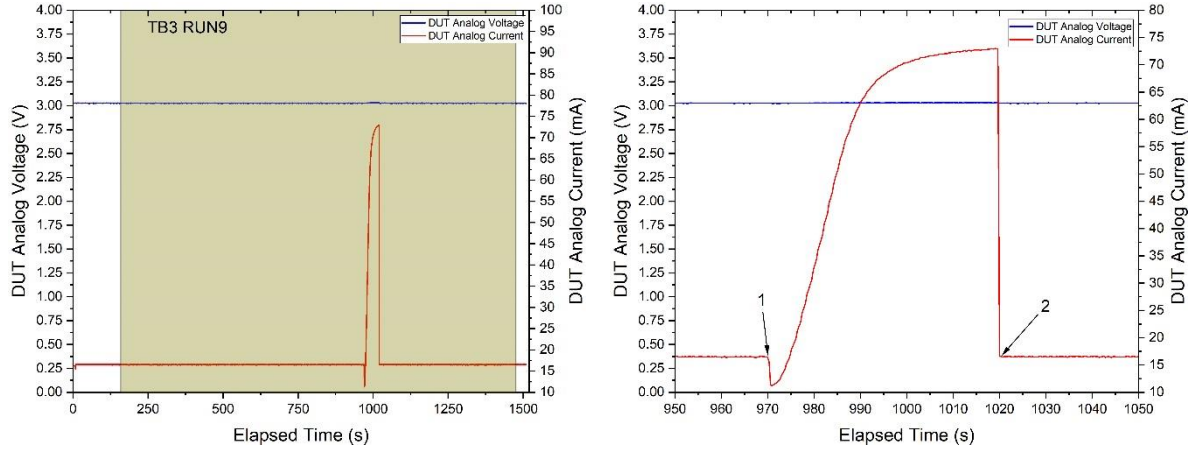
Another type of measurements which were carried out are the pedestal measurements. These measurements show the false trigger rates when the DAC threshold value is low (close to GND level), and lower than the noise present at the input of the discriminator. The pedestals trigger rate is decreasing as the DAC threshold is increasing and hence exceeding the noise amplitude. The resulting plots are given in fig. 3.16 and no failures were observed.



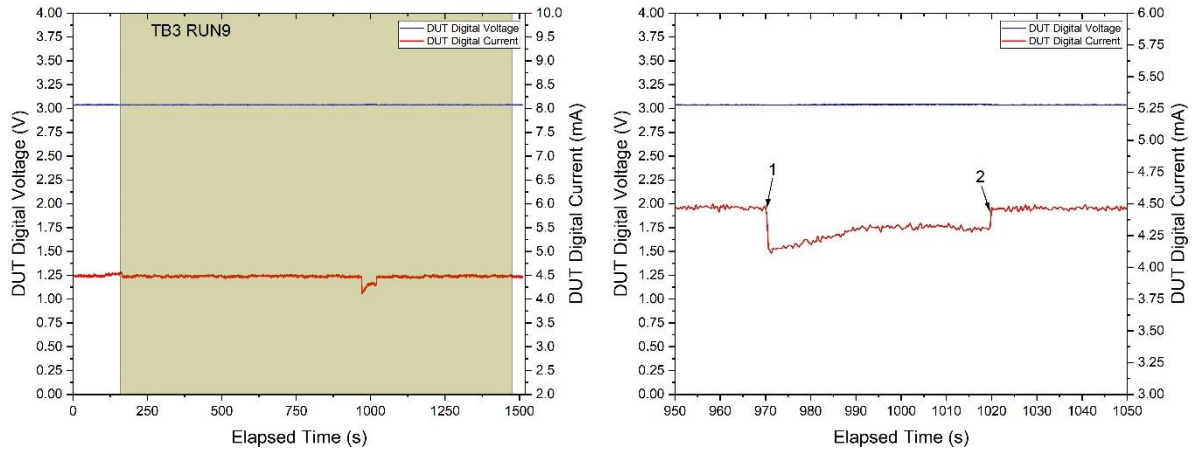
**Fig. 3.16** DUT Trig\_FSU trigger rate measurements with pedestal on all 64 channels before (left side) and after the 8<sup>th</sup> irradiation run (right side)

By increasing the LET to  $(8.59 \pm 0.86) \text{ MeV} \cdot \text{cm}^2/\text{mg}$  using  $^{20}\text{Si}$  ions beam, two radiation-induced SEUs into the slow control configuration registers were observed during the 9<sup>th</sup> irradiation run.

The first SEU has led to a current increasing into DUT power consumption and was mapped to be the 205<sup>th</sup> bit within the slow control configuration register being flipped from 1 to 0. According to the DUT datasheet [212], the 205<sup>th</sup> bit is a bit from the DUT biasing control category and this particular bit is responsible for controlling the biasing for the preamplifier blocks. Hence, an additional bias was injected in the preamplifier blocks and a current increase with a multiplicative factor of 4 more than its baseline value was induced into the analog core of the DUT, as it can be seen in left side of fig. 3.17. In the right side of fig. 3.17 a zoom-in on the current increase is shown, and it can be seen that before the increase there is a sudden decrease of the current (dip). However, due to the same SEU the current in the digital block had a slight decrease, as it is shown in fig. 3.18.



**Fig. 3.17** DUT power consumption on the analog block over the whole irradiation run (left side) and a zoom-in on the current increase induced by a SEU in the slow control configuration registers (right side) during 9<sup>th</sup> irradiation run, the “1” is the SEU event time and “2” is the moment of reconfiguration of device

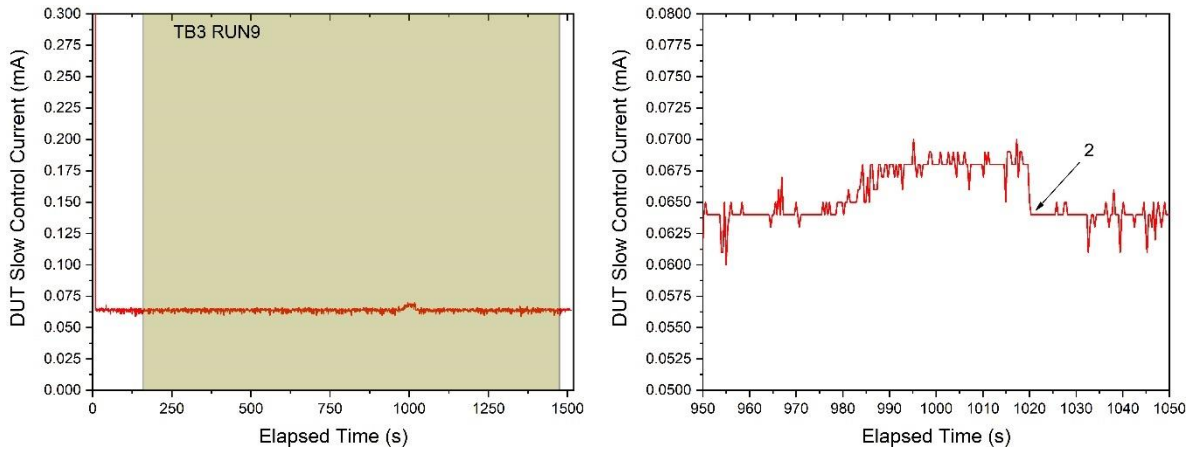


**Fig. 3.18** DUT power consumption on the digital block over the whole irradiation run (left side) and a zoom-in on the current spike induced by a SEU in the slow control configuration registers (right side) during 9<sup>th</sup> irradiation run

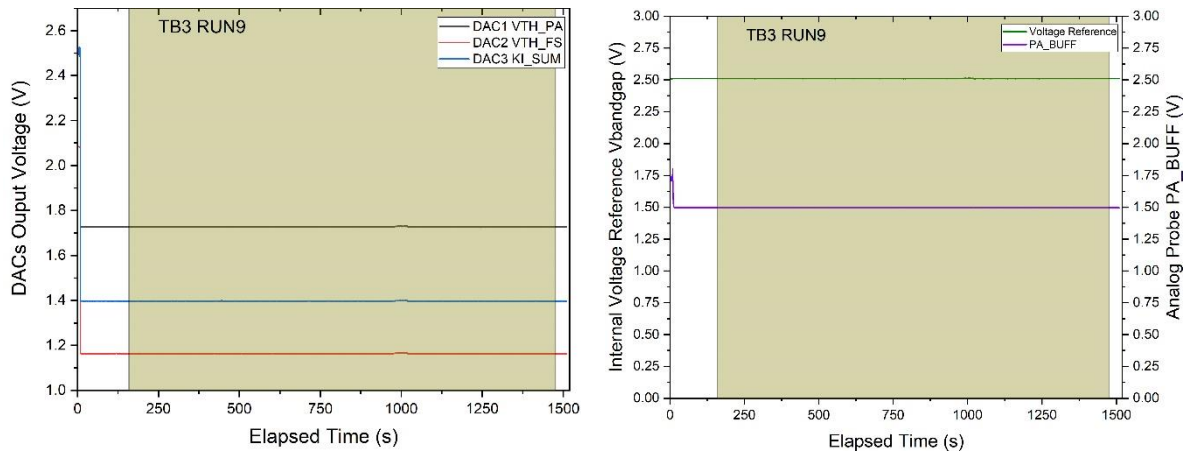


A small increase was observed also in the slow control current consumption as a consequence of the same SEU, see fig. 3.19. However, the induced current increase within the DUT was mitigated by a full reconfiguration of the DUT which flipped the 205<sup>th</sup> bit back to its initial status, 0. No changes were observed in the DAC output voltages as well as in the internal voltage reference respectively in the preamplifier analog probe, see fig. 3.20.

The effect of the first SEU to the DUT functionality is correlated in most of the measurements as it can be observed by the states “1” and “2” from fig. 3.17, fig. 3.18 and fig. 3.19. The effect of this SEU on the DUT power consumption within the analog core is similar with the DUT state “A” after power-up and before being configured, as the current consumption on the analog core is rising up to a given value and it stays there till the DUT is configured.



**Fig. 3.19** DUT power consumption on the slow control section part of the digital block over the whole irradiation run (left side) and a zoom-in on the current increase induced by a SEU in the slow control configuration registers (right side) during 9<sup>th</sup> irradiation run



**Fig. 3.20** Measurements of DUT output voltages corresponding to its three internal DACs (right side) and internal voltage reference together with the preamplifier analog probe (right side) during 9<sup>th</sup> irradiation run

The second SEU which was observed during the 9<sup>th</sup> irradiation run did not affect the power consumption of the DUT, however its location was in a control byte used to configure the gain

of the preamplifier for the 46<sup>th</sup> channel. This SEU may affect the trigger efficiency of 46<sup>th</sup> channel, however it was also mitigated by a full reconfiguration of the DUT. The table 3.3 shows the SEU locations within the slow control configuration registers as well as their default state before SEU occurrence.

**Tab. 3.3** Summary of radiation-induced SEU in the slow control registers during 9<sup>th</sup> irradiation run and their mapping

| Slow control bit | Initial state | Observations                                                                                                 |
|------------------|---------------|--------------------------------------------------------------------------------------------------------------|
| 205              | 1             | bias switching control for the preamplifier                                                                  |
| 432              | 0             | GAIN46[5] => the 5 <sup>th</sup> bit of the gain value byte for the preamplifier on 46 <sup>th</sup> channel |

Another run - 10<sup>th</sup> irradiation run - was carried out on the same DUT with a higher effective LET of (11.15 +/- 1.1) MeV · cm<sup>2</sup>/mg by using <sup>20</sup>Si ions with the DUT tilted at 40°. During this run, six radiation-induced SEUs were observed with no major effects to the DUT functionality. The majority of the SEUs were affecting the gain of the preamplifiers, see table 3.4 for a summary of all bits flipped/changed in the slow control configuration registers. However, all of them were mitigated by a full reconfiguration of the DUT.

During the 10<sup>th</sup> run, no effects were seen in the DUT power consumption or in the other parameters as well as in its DAC linearity and trigger efficiency measurements, as the affected bits were mostly preamplifier bits and generally used for controlling the trigger rates.

The irradiation with ions proved the fact that the DUT shown no SELs up to (11.15 +/- 1.1) MeV · cm<sup>2</sup>/mg. However, the SEU threshold was measured to be between (4.45 +/- 0.45) MeV · cm<sup>2</sup>/mg and (8.59 +/- 0.86) MeV · cm<sup>2</sup>/mg. Two cross-section values were calculated for the SEUs observed during the 9<sup>th</sup> and 10<sup>th</sup> runs. Since the number of SEUs was low for a given fluence, the cross-section values for each LET values are given as lower and upper limits with a 95% confidence level (CL). The values are given in table 3.5 and have included also the fluence error of 20 %.

**Tab. 3.4** Summary of radiation-induced SEU in the slow control registers during 10<sup>th</sup> irradiation run and their mapping

| Slow control bit | Initial state | Observations                                                                                                 |
|------------------|---------------|--------------------------------------------------------------------------------------------------------------|
| 115              | 0             | KI1:sc5DCAbs_Pmos_160u – internal configuration for KI_SUM block                                             |
| 315              | 0             | GAIN57[2] => the 2 <sup>nd</sup> bit of the gain value byte for the preamplifier on 57 <sup>th</sup> channel |
| 416              | 0             | GAIN47[1] => the 1 <sup>st</sup> bit of the gain value byte for the preamplifier on 47 <sup>th</sup> channel |
| 423              | 0             | GAIN46[4] => the 4 <sup>th</sup> bit of the gain value byte for the preamplifier on 46 <sup>th</sup> channel |
| 489              | 0             | cmd_Ctest_ch40 => external pulser test enable for 40 <sup>th</sup> channel                                   |
| 776              | 0             | GAIN11[1] => the 1 <sup>st</sup> bit of the gain value byte for the preamplifier on 11 <sup>th</sup> channel |

**Tab. 3.5** DUT SEU cross-section limit values for the slow control configuration registers

| SEUs | Fluence<br>(ions/cm <sup>2</sup> ) | Effective LET<br>(MeV · cm <sup>2</sup> /mg) | Lower limit of<br>cross-section<br>(cm <sup>2</sup> /device) | Upper limit of<br>cross-section<br>(cm <sup>2</sup> /device) |
|------|------------------------------------|----------------------------------------------|--------------------------------------------------------------|--------------------------------------------------------------|
| 2    | $(1.265 \pm 0.25) \cdot 10^6$      | 8.59 $\pm$ 0.86                              | $0.13 \cdot 10^{-6}$                                         | $9.5 \cdot 10^{-6}$                                          |
| 6    | $(1.1 \pm 0.22) \cdot 10^6$        | 11.15 $\pm$ 1.1                              | $1.4 \cdot 10^{-6}$                                          | $20 \cdot 10^{-6}$                                           |

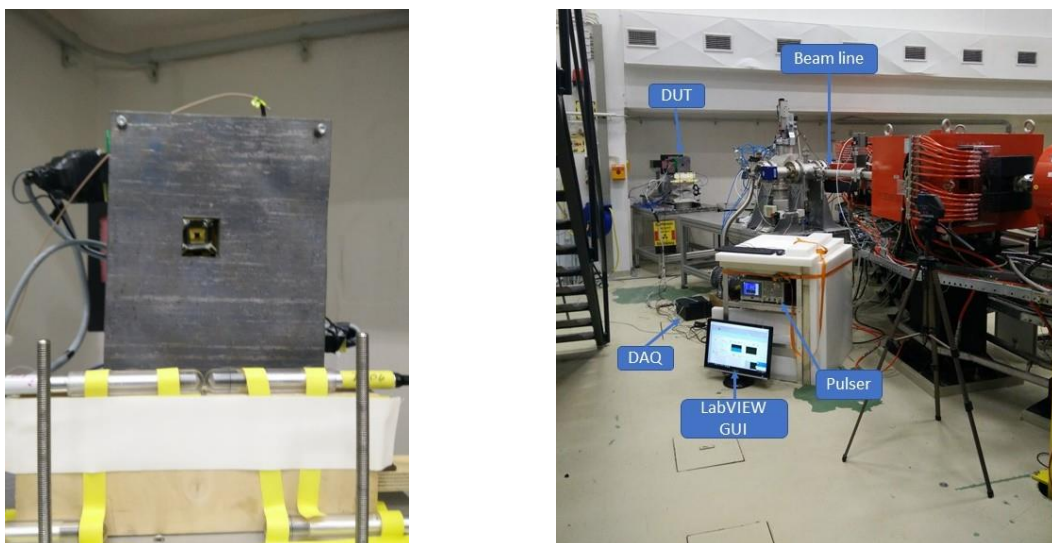
### 3.3.2 35 MeV Proton Irradiation

One DUT test board was tested at the 2.88 GeV Cooler Synchrotron COSY-Jülich with 35 MeV protons beam at different dose rates and up to  $(150 \pm 7.5)$  krad (Si) TID. The summary of the proton runs done on the DUT test board are given below, in table 3.6.

**Tab. 3.6** The 35 MeV proton irradiation runs

| Run<br>Nr. | Test<br>Board | Time<br>(s) | Dose<br>(krad) | Dose rate<br>(rad/s) | Fluence (5% error)<br>(protons/cm <sup>2</sup> ) |
|------------|---------------|-------------|----------------|----------------------|--------------------------------------------------|
| 1          | TB1           | 253         | $(50 \pm 2.5)$ | 197.6                | $(2.3 \pm 0.11) \cdot 10^{11}$                   |
| 2          | TB1           | 477.3       | $(50 \pm 2.5)$ | 104.7                | $(2.3 \pm 0.11) \cdot 10^{11}$                   |
| 3          | TB1           | 490.7       | $(50 \pm 2.5)$ | 101.9                | $(2.3 \pm 0.11) \cdot 10^{11}$                   |

The DUT test board was mounted on a sample holder in front of the beam line and its experimental setup, including the DAQ system, was placed at a few meters away, as it is shown in the right side of fig. 3.21. A 10 mm Lead mask was used to ensure a radiation shielding of the additional electronics from the DUT test board and leaving an open window to expose only the DUT die, see the left side of the fig. 3.21. The whole experimental setup was monitored from the control room at a very far and safe distance from the experimental area. Tests were carried out before irradiation, to establish a baseline of the DUT parameters.



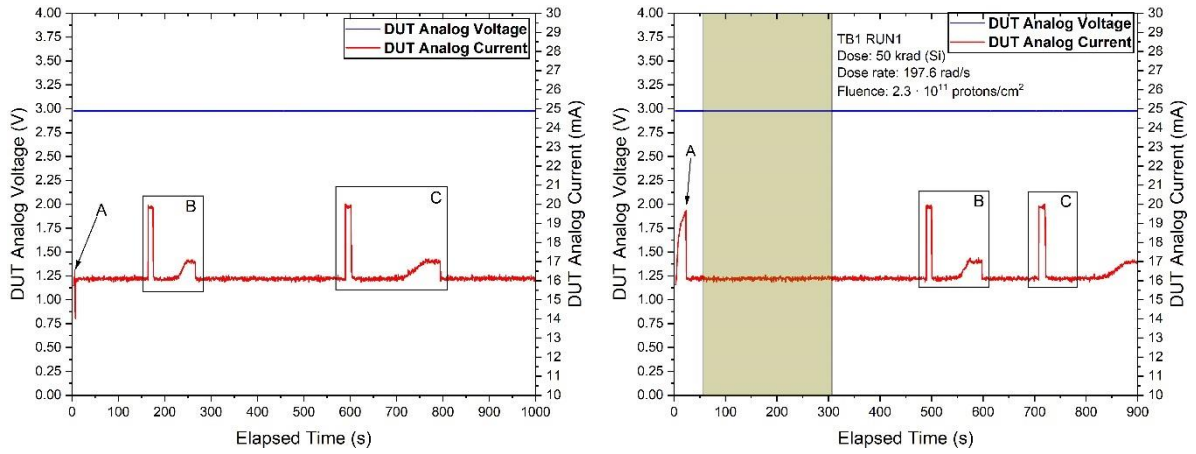
**Fig. 3.21** DUT test board (left side) and its experimental setup installed in the experimental area at the Juelich cyclotron (right side)



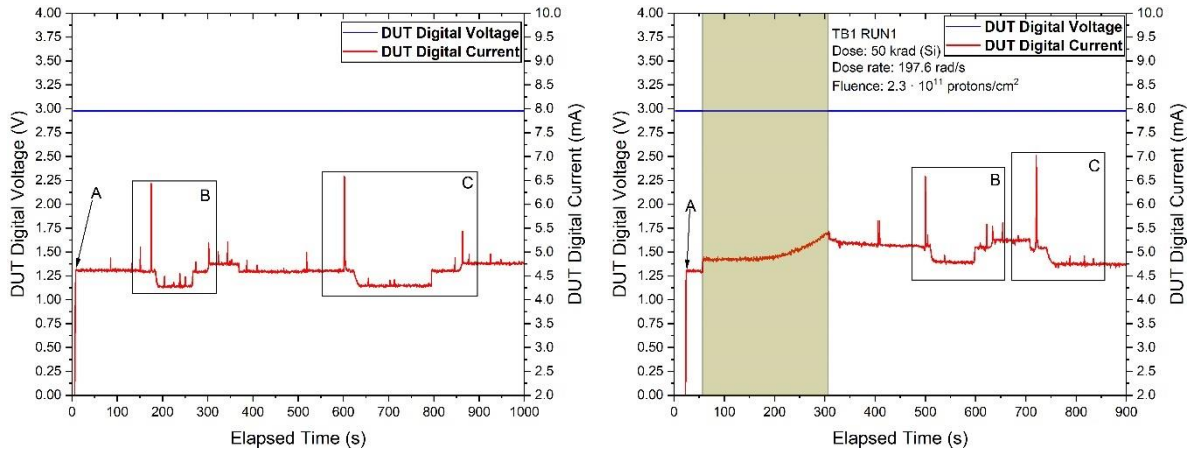
The same functional states described in section 3.3.1 are present on the DUT parameters which highlights the present state of the DUT and are correlated in all the measurements: powered and unconfigured state “A”, DAC linearity tests state “B” and trigger efficiency tests state “C”.

With the first run, 50 krad (Si) TID were delivered to the DUT and it was observed that the digital core manifested a small increase of the leakage current of about 0.5 mA with respect to its baseline value as more dose was accumulating, hence more positive charge traps into its oxide. On the slow control section, the current increase was 7 times above its baseline. However, the TID-induced increase of the leakage current started to decrease after the beam was stopped, and the room-temperature annealing process started to be visible.

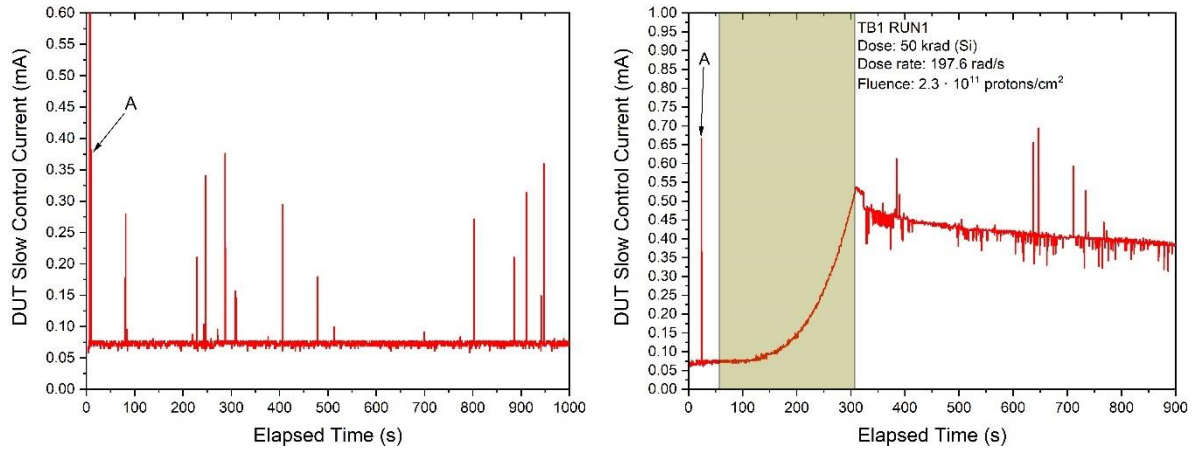
The power measurements on the analog and digital blocks before and during the irradiation run are given in fig. 3.22 and fig. 3.23, respectively in fig. 3.24 for the slow control section.



**Fig. 3.22** DUT power consumption on the analog block before irradiation (left side), during 1<sup>st</sup> irradiation run (right side), and after the irradiation

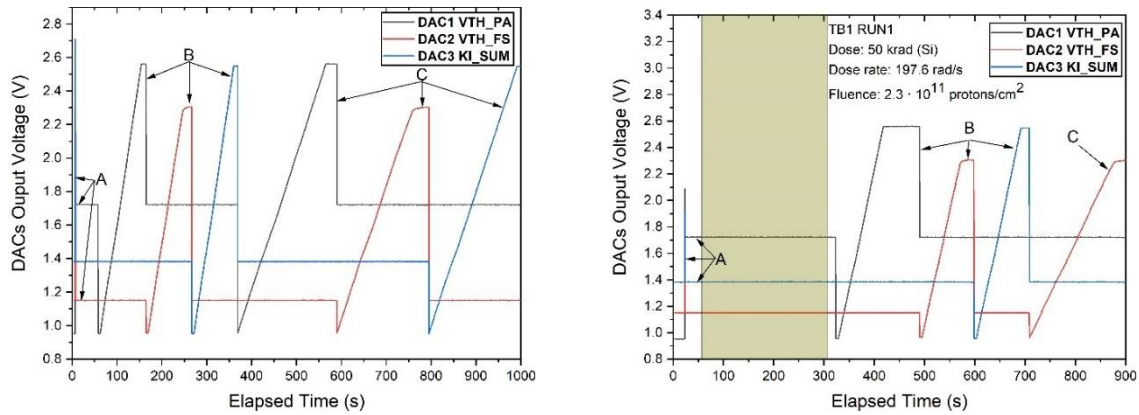


**Fig. 3.23** DUT power consumption on the digital block before irradiation (left side) during the 1<sup>st</sup> irradiation run (right side), and after the irradiation

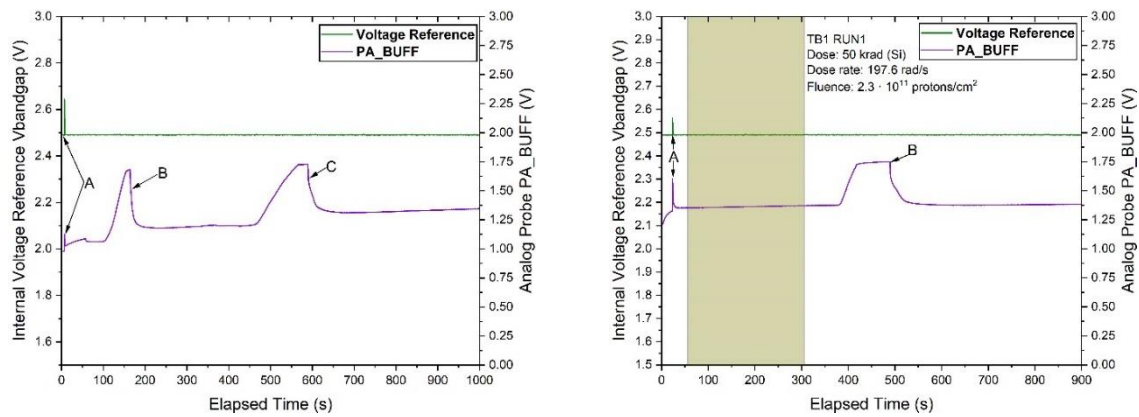


**Fig. 3.24** DUT power consumption on the slow control section part of the digital block before irradiation (left side) during the 1<sup>st</sup> irradiation run (right side), and after the irradiation

No TID effects were observed in the measurements of the DAC output voltages as well as in the analog preamplifier probe and in the DUT internal voltage reference, see fig. 3.25 and fig. 3.26.

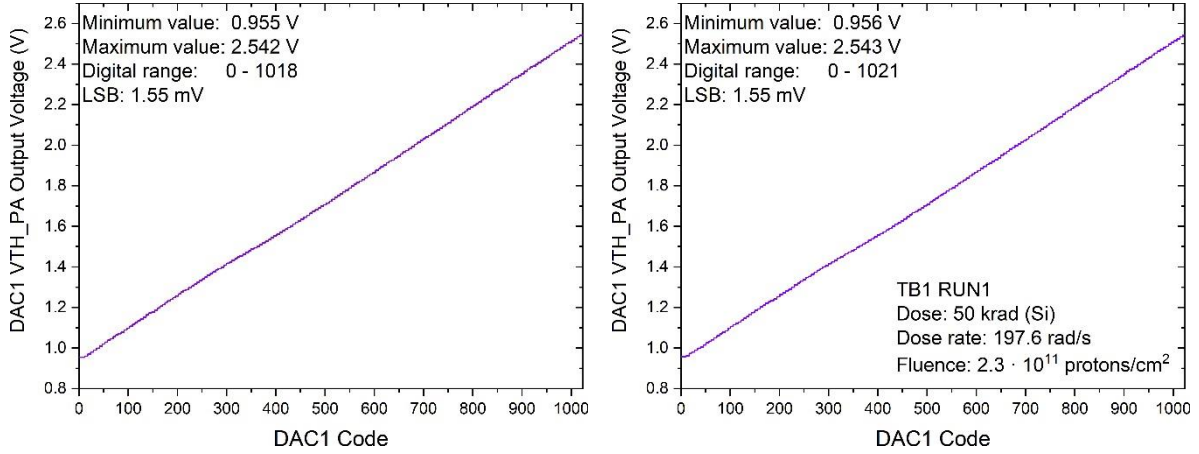


**Fig. 3.25** Measurements of DUT output voltages corresponding to its three internal DACs before irradiation (left side) during the 1<sup>st</sup> irradiation run (right side)

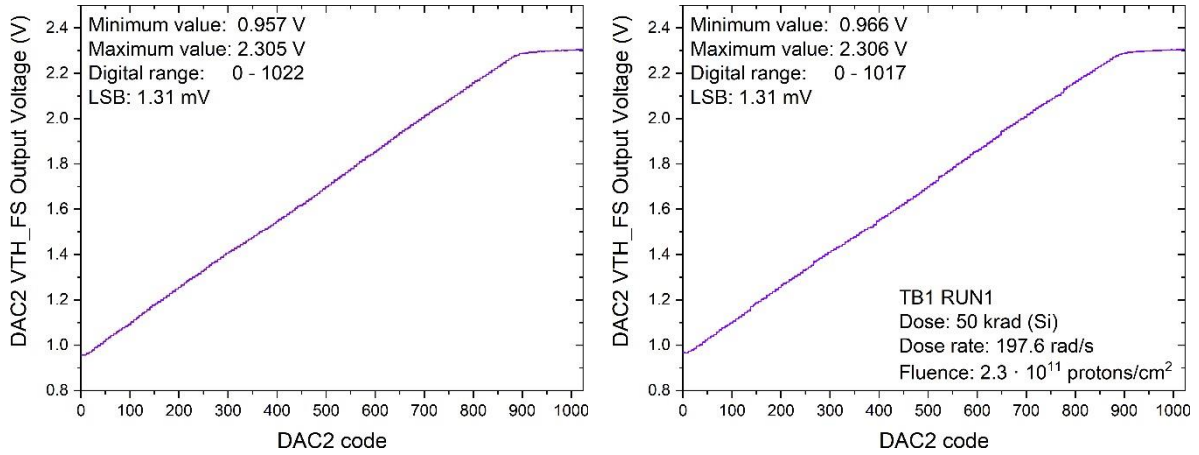


**Fig. 3.26** Measurements of the internal voltage reference together with the preamplifier analog probe before irradiation (left side) during the 1<sup>st</sup> irradiation run (right side)

The linearity of the DACs was generally stable after 50 krad (Si). No significant effects were observed in the DAC1 functionality, as is shown in fig. 3.27. However, fig. 3.28 and fig. 3.29 highlights the fact the DAC2 and DAC3 shown a small radiation-induced voltage offset of their minimum values (when the DAC code is 0) of 9 mV for DAC2, respectively 6 mV for DAC3. This may be due to TID-induced additional increase of the leakage current in the NMOS current mirrors, corresponding to the lowest significant bits, which shifted the DAC minimum value as well as induced some imperfections on the DAC linearity along the entire range.

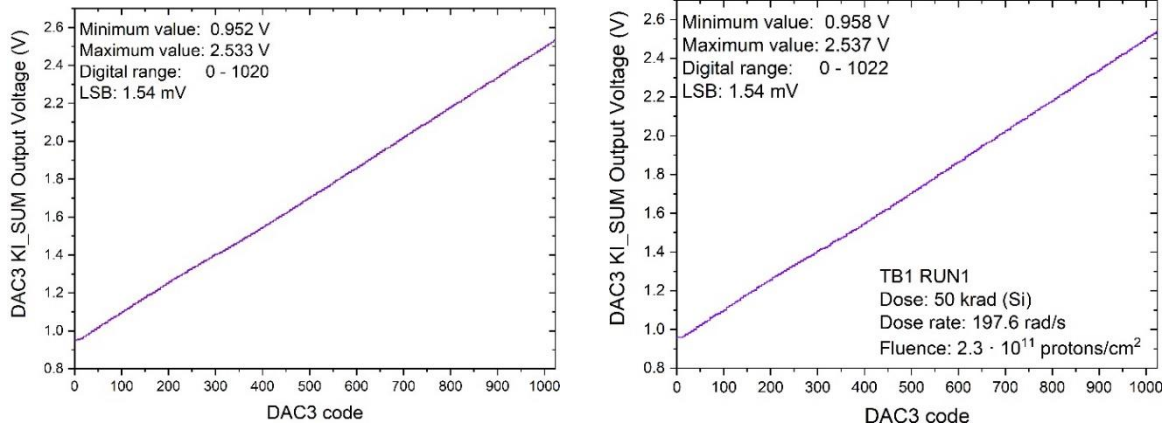


**Fig. 3.27** DUT DAC1 linearity measurements before irradiation (left side) and after the 1<sup>st</sup> irradiation run (right side)

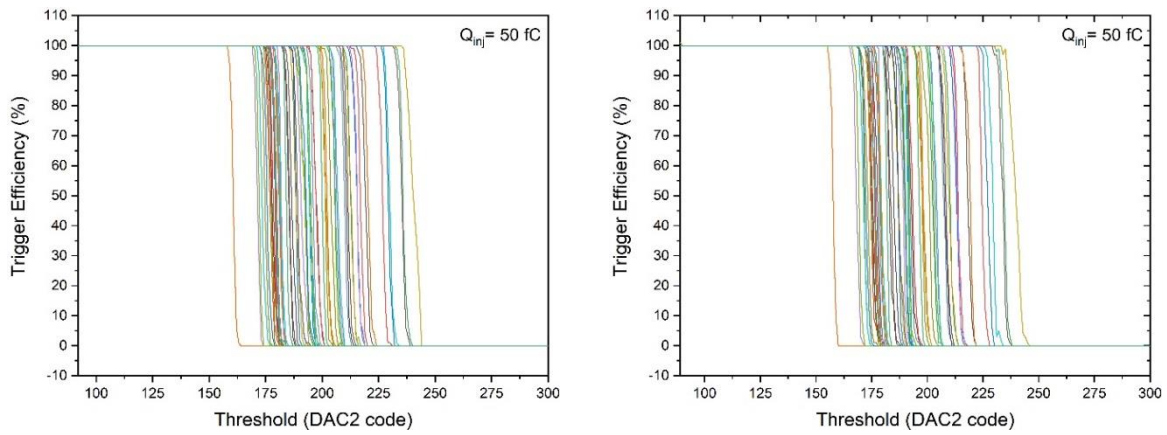


**Fig. 3.28** DUT DAC2 linearity measurements before irradiation (left side) and after the 1<sup>st</sup> irradiation run (right side)

The positive offset in the minimum voltage of the DAC2 output had an impact on the trigger efficiency measurements for the Trig\_FSU trigger generation block. As it may be seen in the right side of fig. 3.30, the threshold for 100 % trigger efficiency decreased with a few DAC units with respect to the measurements done before irradiation and given in the left side of fig. 3.30.

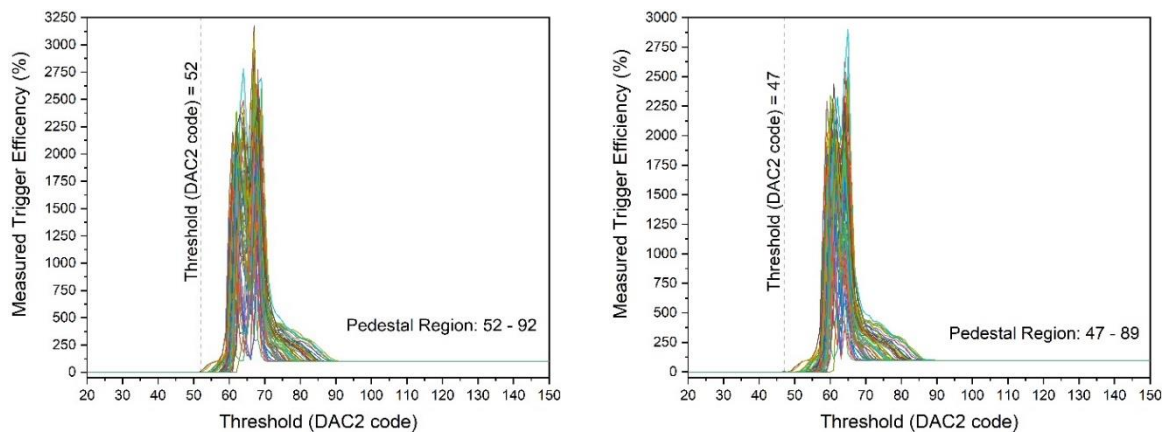


**Fig. 3.29** DUT DAC3 linearity measurements before irradiation (left side) and after the 1<sup>st</sup> irradiation run (right side)



**Fig. 3.30** DUT Trig\_FSU trigger efficiency measurements for all 64 channels with 50 fC input charge before irradiation (left side) and after the 1<sup>st</sup> irradiation run (right side)

As in case of the trigger efficiency measurements, the same negative threshold shift was observed in the pedestals measurements as a consequence of a positive shift in the DAC2 output, see fig. 3.31.

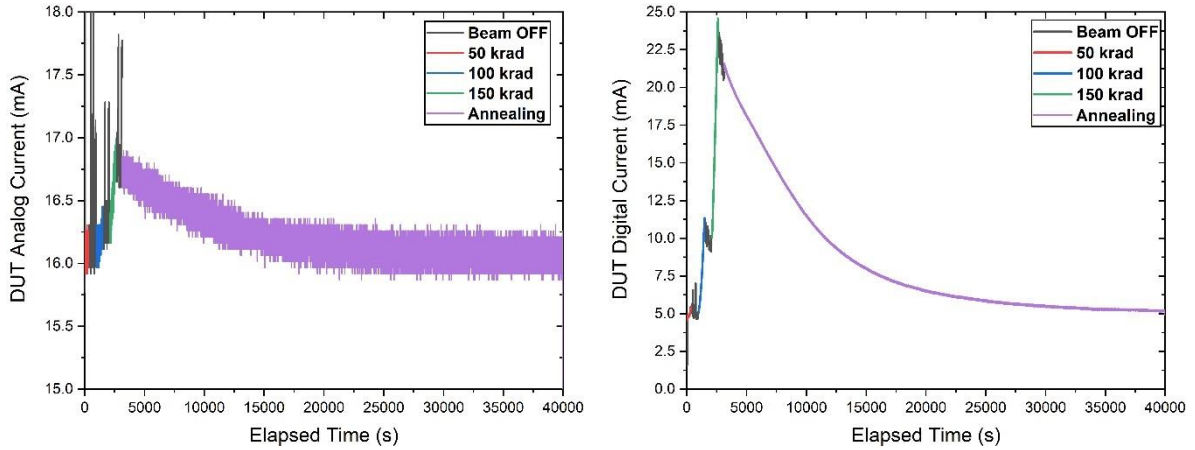


**Fig. 3.31** DUT Trig\_FSU pedestal trigger rate measurements on all 64 channels before irradiation (left side) and after the 1<sup>st</sup> irradiation run (right side)

With more dose accumulating into the DUT oxide insulation layers the global TID-induced leakage currents are initially increasing linearly with the dose (to first approximation). Between runs, when the beam is stopped and the DUT internal blocks are tested, the rapid annealing process at room temperature is visible.

After 50 krad (Si) the analog core starts to manifest visible, however small, TID-induced increase of the leakage current, having up to 1 mA increase between 50 krad (Si) and 150 krad (Si) with respect to its baseline value. It was completely mitigated through a 10 h room-temperature annealing process, as it can be seen in the left side of fig. 3.32.

The digital core starts to manifest TID-induced increase of its leakage current at lower doses, this effect being highly dependent on the dose rate. After 100 krad (Si) the current into the digital core was increased by a factor of 2, and by a factor of 5 after 150 krad (Si). However, it was almost completely mitigated through a 10 h room-temperature annealing process. The evolution of the current increase in the digital core with respect to the total accumulated dose (assuming the dose rates are constant during runs) and its annealing curve are given in the right side of fig. 3.32.

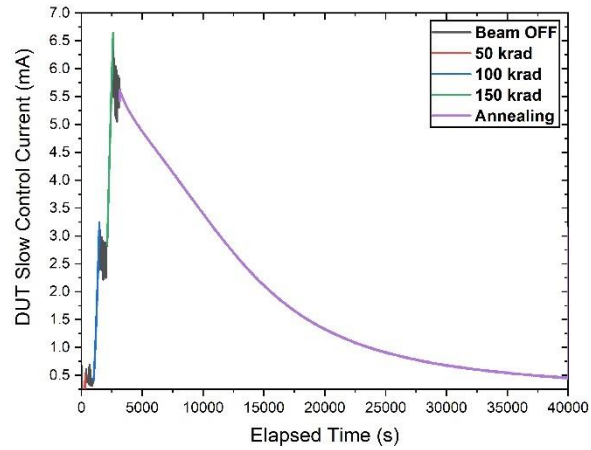


**Fig. 3.32** DUT power consumption on the analog block (left side) and digital block (right side) after three runs of 50 krad (Si) each, plus room-temperature annealing measurements

The same current increase rate is present in the slow control section part of the digital core, which does not contribute to the digital core current increase, though, its evolution with the dose together with its annealing curve are shown in fig. 3.33. (assuming the dose rate is constant)

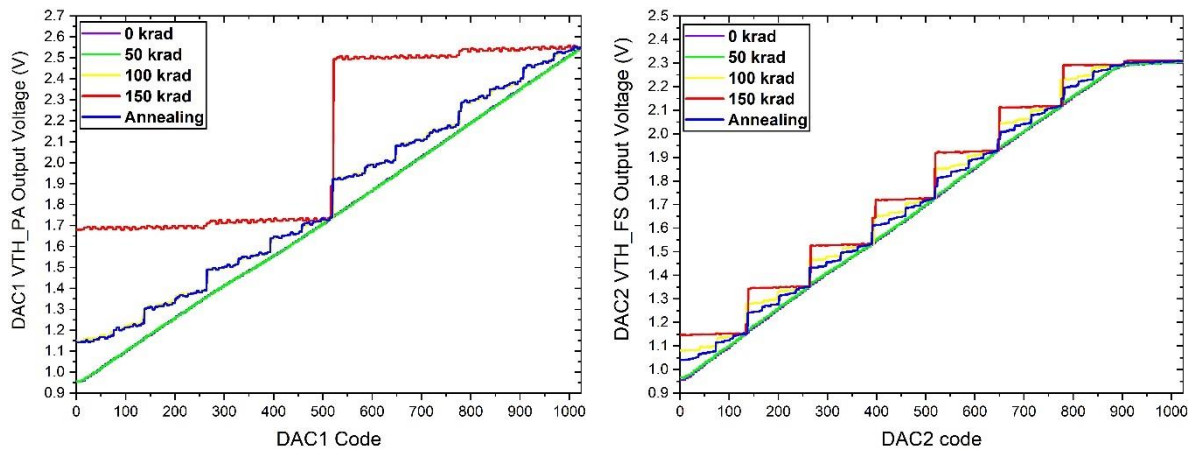
At higher doses, the embedded DACs start to manifest positive voltage shifts of their minimum values, when their digital code is 0. Effects due TID, were observed in DAC1, DAC2 and DAC3, where after 150) krad (Si) they have completely lost their monotonicity, hence their linearity. By looking at the DAC1 evolution with dose (left side of fig. 3.34) it can be seen that at TID over 50 krad (Si) start to manifest signs of non-linearity and a complete loss of its majority bits after 150 krad (Si). The same apply to other DACs, however DAC2 seem to be less affected than the other DACs. From fig. 3.25 it can be seen that the DAC1 and DAC3 are set to have an output voltage higher than the DAC2 when were irradiated, however there is no indication that this configuration may have an impact.



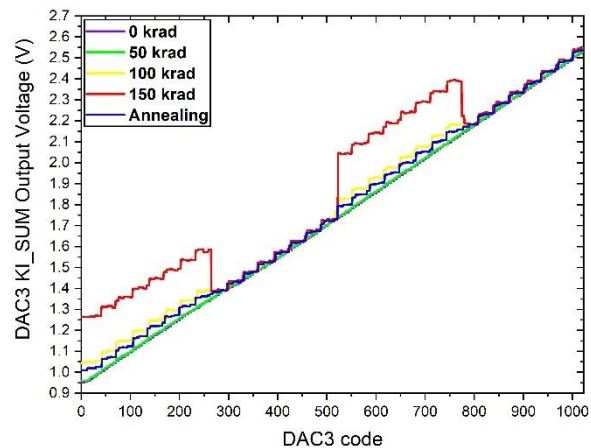


**Fig. 3.33** DUT power consumption on the slow control section, part of the digital block, after three runs of 50 krad (Si) each, plus room-temperature annealing measurements

All three DACs seem to have partially regained their linearity after a 10 h room-temperature annealing, and their linearity measurements before, during irradiation and after annealing are given in fig. 3.34 for DAC1 and DAC2 and in fig. 3.35 for DAC3.

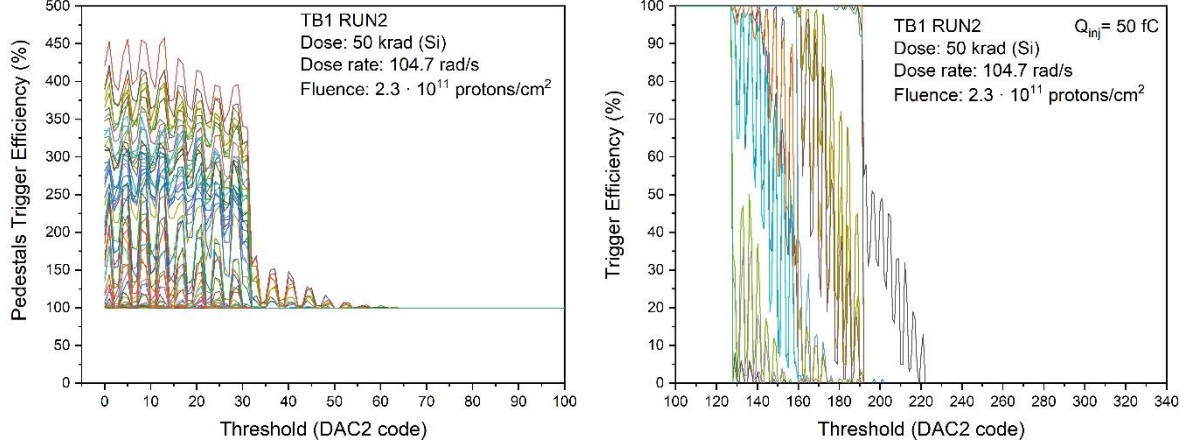


**Fig. 3.34** DUT DAC1 linearity (left side) and DAC2 linearity measurements after three runs of 50 krad (Si) and after annealing



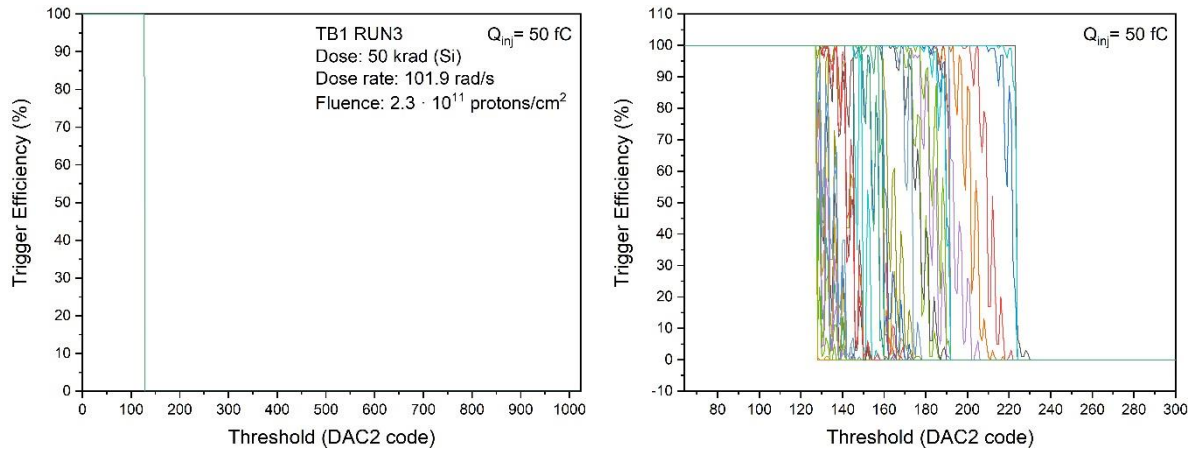
**Fig. 3.35** DUT DAC3 linearity measurements after three runs of 50 krad (Si) and after annealing

Failures were observed in the Trig\_FSU trigger generation block, as after 100 krad (Si) the trigger efficiency curves had shifted to a lower DAC threshold as well as some of the channels were manifesting functional failures. The pedestal trigger rate decreased drastically on all 64 channels mainly due to the fact that the DAC output voltage had a positive shift over the normal threshold where usually the pedestal trigger rates have the high rate. The pedestals together with the trigger efficiency measurements are given in fig. 3.36.



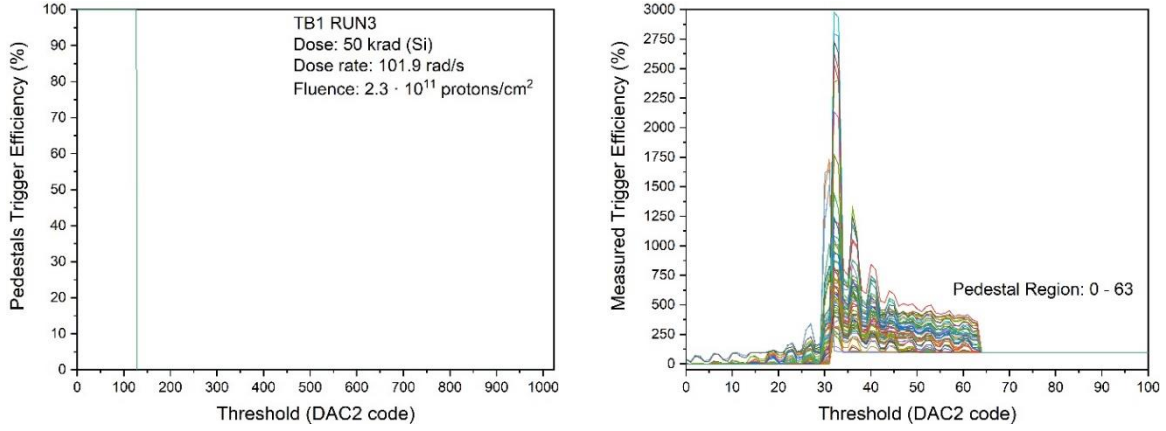
**Fig. 3.36** DUT Trig\_FSU pedestals (left side) and trigger efficiency with 50 fC input charge (right side) measurements for all 64 channels after the 2<sup>nd</sup> irradiation run

As more dose was accumulating, the Trig\_FSU block showed full functional failure of not being able to generate triggers anymore. However, after a 10 h room temperature annealing process, and with the DUT recovering from TID, in the same manner with the DACs, the Trig\_FSU block is already partially recovered. In fig. 3.37 are shown the trigger efficiency measurements after 150 krad (Si) in the left side and after annealing in the right side. It can be seen, that there is still a shift in the DAC2 threshold with respect to the baseline measurements (see left side of fig. 3.30). However, all the channels seem to almost completely recovered.



**Fig. 3.37** DUT Trig\_FSU trigger efficiency measurements on all 64 channels after 150 krad (Si) (left side) and after annealing (right side)

In the same manner were acting also the pedestal measurements, which showed partial improvements and having a lower DAC threshold value compared with the baseline measurements before irradiation, see fig. 3.38.



**Fig. 3.38** DUT pedestal trigger rate measurements on all 64 channels after 150 krad (Si) (left side) and after annealing (right side)

The DUT recovered completely after a few days of annealing in unbiased off-state mode, with no permanent or residual failures observed, compared with the state before irradiation (this is realistic as LHCb and JEM-EUSO experiments are expected to follow the same power-down cycles). No SEEs were observed during irradiation with 35 MeV protons. However, an upper limit of SEU cross-section within the slow control registers was calculated with a 95% CL to be  $1.53 \cdot 10^{-11}$  cm<sup>2</sup>/device. The only predominant effect being the TID-induced increase of leakage currents of the CMOS structures within the digital core. Also, the observed functional failures in the analog blocks, mainly due to TID-induced voltage shifts lead to completely losses of trigger efficiency but only at these large TID rates delivered by proton beam.

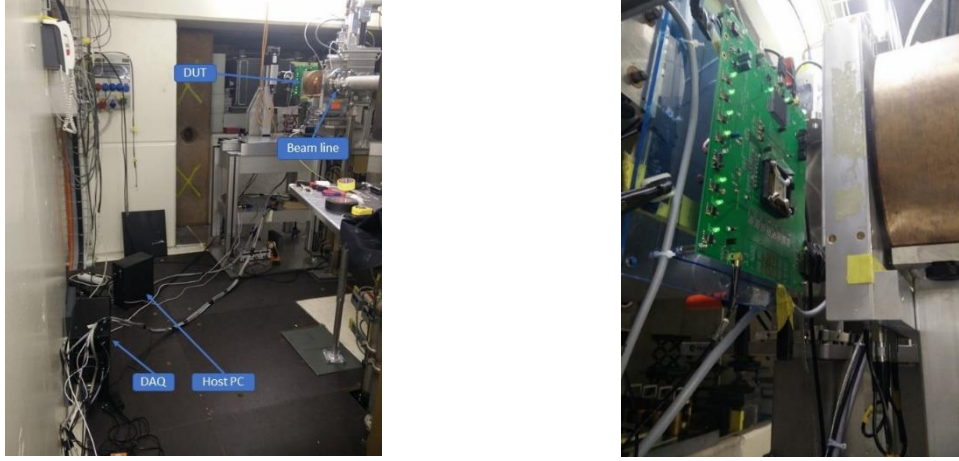
### 3.3.3 200 MeV Proton Irradiation

The SPACIROC2 test board was tested for the first time in beam with 200 MeV protons at the Proton Irradiation Facility (PIF) [209] from Paul Scherrer Institute in Switzerland. Three test boards were tested in different scenarios to establish the DUT tolerance to proton-induced TID and SEE effects up to about 100 krad (Si) and with a fluence up to about  $(2 \pm 0.3) \cdot 10^{12}$  protons/cm<sup>2</sup>.

The DUT test board was mounted on a sample holder in front of the beam line window, while the beam was extracted in air. Its experimental DAQ setup was placed in the vicinity of the beam line at a few meters away, as it can be seen in fig. 3.39. The entire experimental setup was controlled by the host PC which was accessed remotely from the control room, at a very far away and safe distance via Ethernet, behind 10 m reinforced concrete block wall and several meters away from the wall. Several tests were carried out with the test boards to establish a baseline of measurements before placing the DUT under proton beam. Due to the fact that at

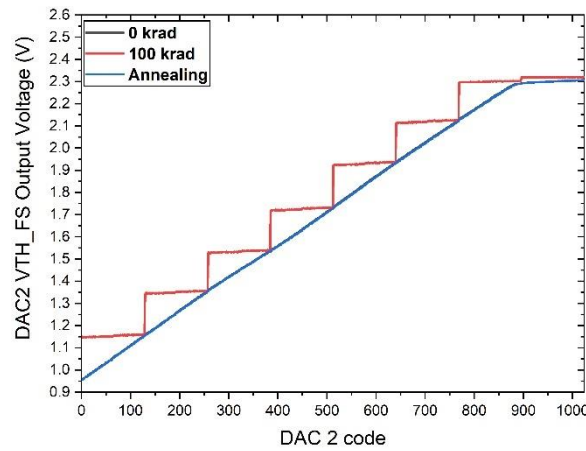


that time a readback procedure of the DUT slow control configuration registers was not implemented, the SEU rates were not extracted for these runs. A more compressive analysis of the DUT test data with 200 MeV protons is given in the PhD thesis of my colleague [213], hence only a few key results from one test board will be presented below in this section, which are independent of the previous work.



**Fig. 3.39** DUT test board mounted on the sample holder at PIF (right side) and its experimental setup placed in the vicinity of the PIF beam line (left side)

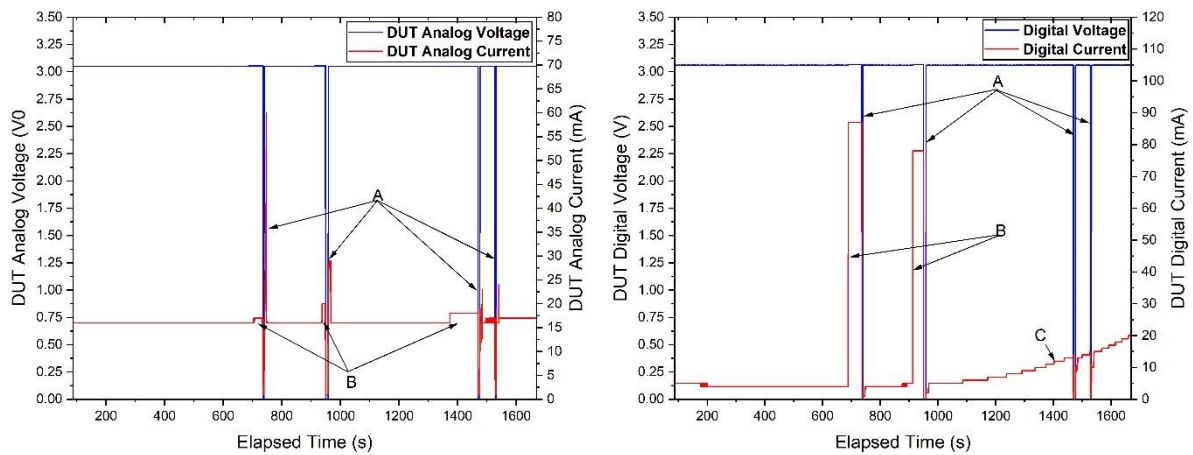
One test board was tested in a single run up to a TID of 100 krad (Si) and with a dose rate of about 63 rads/s, which resulted in a total fluence of  $(1.7 \pm 0.26) \cdot 10^{12}$  protons/cm<sup>2</sup>. It was observed that after 100 krad (Si) the DUT manifested full functional failure, highlighted by the DAC2 non-linearity and as well as by observed changes in the trigger efficiency and pedestal measurements. As it can be seen in fig. 3.40, the DAC2 showed a positive shift of its minimum voltage value, of about 200 mV which affected the trigger efficiency measurements by decreasing the trigger rate to 0 and a step-like response in its linearity due to the loss of at least 3 bits. Also, from fig. 3.40 it can be seen that the maximum value was higher than its baseline value, which may indicate a failure in the transimpedance amplifier inherent in the DAC block.



**Fig. 3.40** DUT DAC2 linearity measurements before, after a TID of 100 krad (Si), and after one week of unbiased annealing

The DUT recovered completely after about one week of unbiased (off-state) annealing at room temperature. The DAC2 has regained its linearity, as well as the trigger efficiency measurements were the same with baseline values before irradiation.

Proton-induced TID and SEEs were observed during this run in both analog and digital current consumption, and are shown in fig. 3.41. SEEs were highlighted as abrupt increased current states in both analog and digital power rails, annotated with “B”. The events annotated with “A” are power cycles of the DUT as rewriting its configuration registers would not mitigate the “B” events. Since there was no way at that time, to distinguish the SEEs from SEU or SEL, the events were classified generally as SEE. With “C”, events or changes in the digital core current are highlighting the TID effects as increased leakage currents which were not mitigated by a power cycle of the DUT. However, these TID effects were completely removed after a week of unbiased and room-temperature annealing.



**Fig. 3.41** Proton-induced TID and SEEs in the DUT analog (left side) and digital (right side) cores during the irradiation run

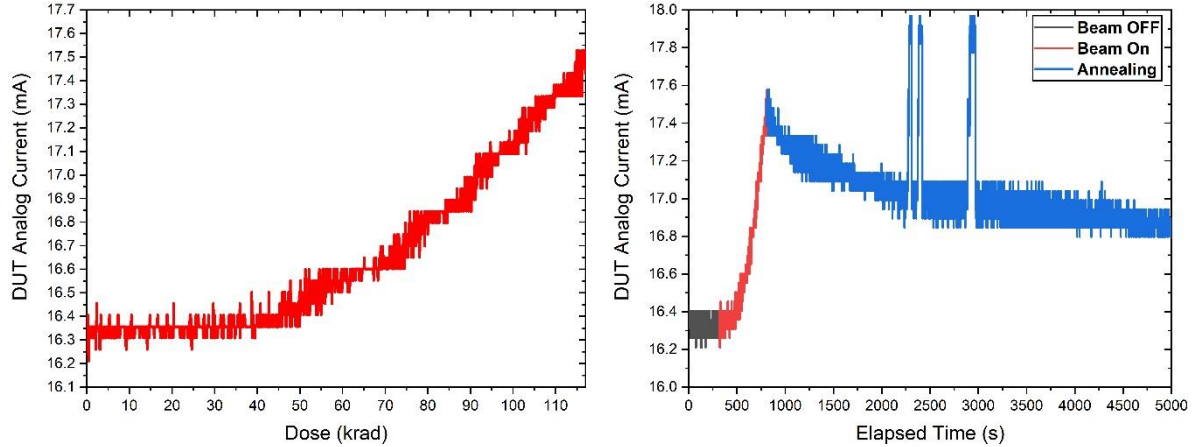
Other two test boards were tested up to 100 krad (Si) but with runs in 10 krad each to establish the threshold on which the DUT starts to manifest functional failure. Hence, according to the measurements presented here [213], the TID threshold is between 80 and 100 krad (Si).

Since there is no way to know exactly the SEU number in the DUT slow control configuration registers, a lower limit of the SEE cross-section in the DUT was calculated based on the “B” events observed in fig. 3.41. Hence, for three SEEs observed after a fluence of  $(1.7 \pm 0.26) \cdot 10^{12}$  protons/cm<sup>2</sup>, the lower limit of the SEE cross-section with a CL of 95% was calculated to be  $1.76^{+3.4}_{-1.4} \cdot 10^{-12}$  cm<sup>2</sup>/device.

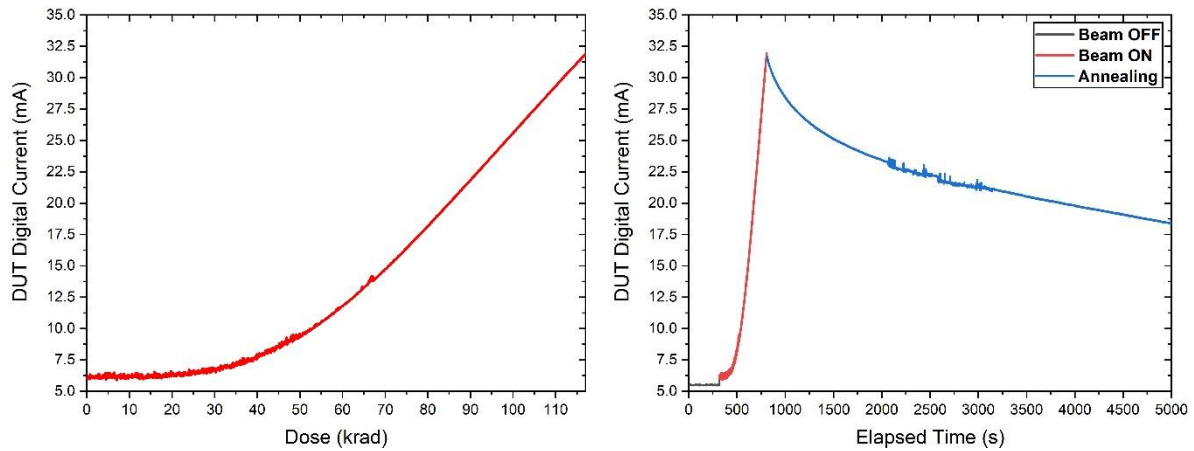
### 3.3.4 X-Rays Irradiation

A single run of about 117 krad (Si) and with a dose rate of 330 rad/s was carried out with 50 keV X-Rays beam on one DUT test board at the X-Ray facility [211] from University of Padova in Italy. The DUT was mounted on a sample holder inside the X-Ray machine and before starting the beam, reference measurements were carried out to establish a baseline.

The X-Rays irradiation run highlighted the TID effects as increased leakage currents with more dose accumulating in the DUT which were already confirmed by the proton irradiation runs. Therefore, the current evolution with the dose and their annealing curves is given in fig. 3.42 for the analog core and in fig. 3.43 for the digital core. Although, the annealing was not done completely, the currents seem to restore with time to their baseline values as the room-temperature annealing takes place.

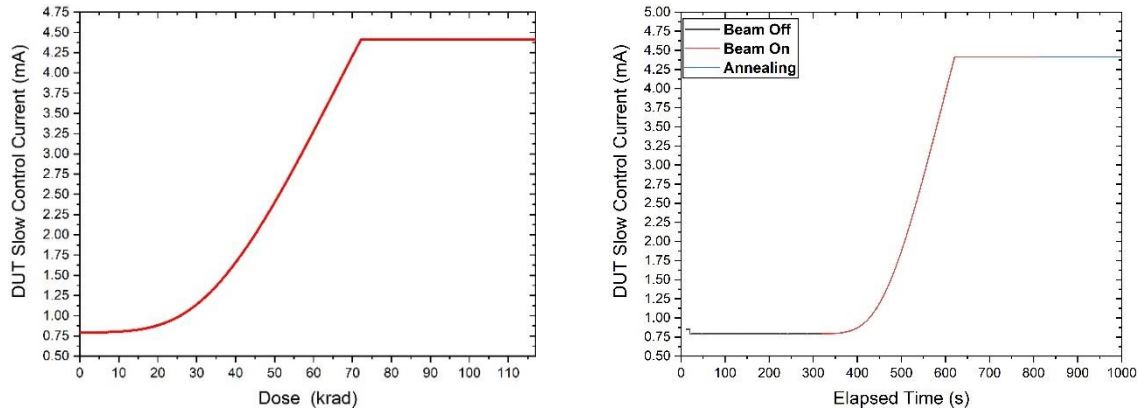


**Fig. 3.42** The evolution of the DUT analog current consumption with the dose (left side) and its annealing curve (right side), with 3 reconfiguration of DUT during S-curve testing and linearity testing



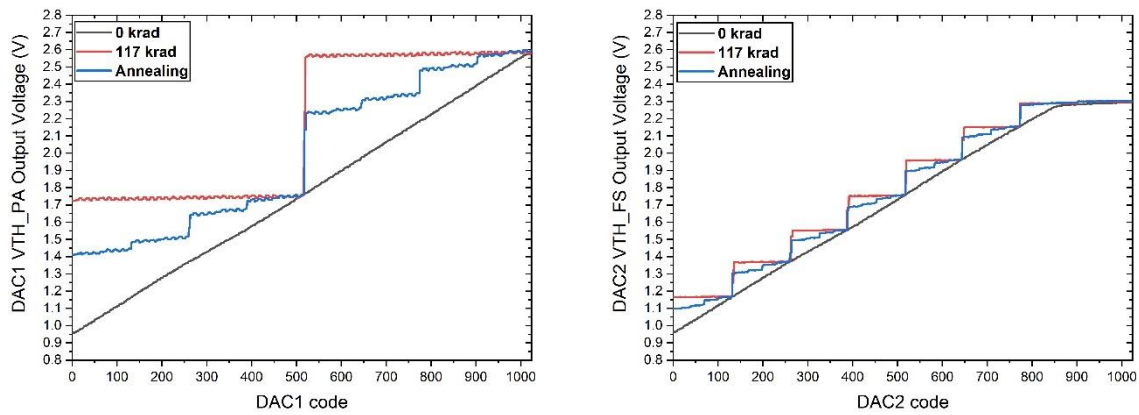
**Fig. 3.43** The evolution of the DUT digital current consumption with the dose (left side) and its annealing curve (right side), with 3 reconfiguration of DUT during S-curve testing and linearity testing

The same pattern was observed in the slow control current consumption, part of the digital current, as it can be seen in fig. 3.44. However, due to a hardware limitation in the DAQ, the slow control current reached the saturation value of the DAQ system and any value above this saturation limit was not measured.

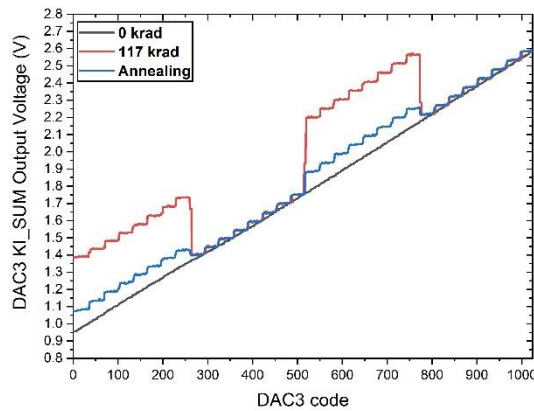


**Fig. 3.44** The evolution of the DUT slow control current consumption with the dose (left side) and its annealing curve (right side)

Similar failures with the ones induced by protons were seen in the DACs, as the DUT showed the same TID response with X-rays as in case of proton TID measurements. The DAC1, DAC2 and DAC3 responses to X-Rays irradiation are shown in fig. 3.45 respectively fig. 3.46 with measurements done before, after irradiation and after about one hour of room-temperature annealing. As it can be seen, the DACs did not recover completely as the annealing period was short, yet the room-temperature annealing is still proven to be extremely fast acting.

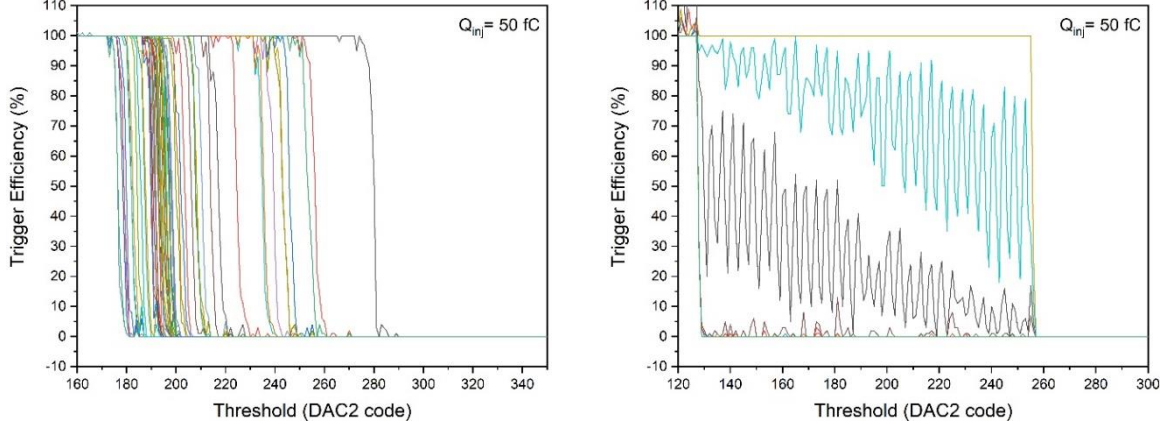


**Fig. 3.45** DUT DAC1 (left side) and DAC2 (right side) linearity measurements before and after 117 krad (Si) irradiation and after annealing

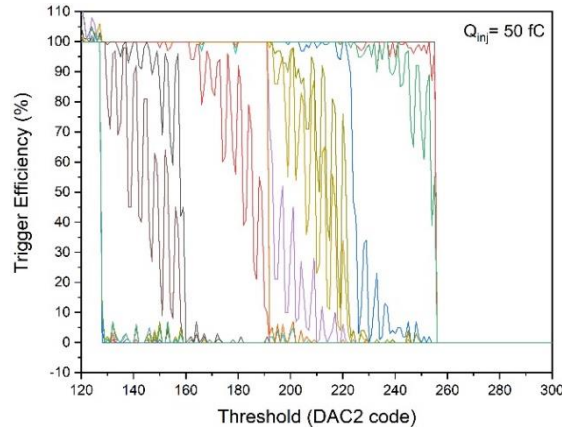


**Fig. 3.46** DUT DAC3 linearity measurements before and after 117 krad (Si) irradiation and after annealing

The failures were propagated through the trigger generation block, confirming the already seen proton-induced TID effects. Therefore, fig. 3.47 shows the trigger efficiency measurements before and after the irradiation run. However, they manifest improvements after about 1 h of room-temperature annealing, as it can be seen in fig. 3.48.



**Fig. 3.47** DUT Trig\_FSU trigger efficiency measurements on all 64 channels before (left side) after 117 krad (Si) irradiation (right side)



**Fig. 3.48** DUT Trig\_FSU trigger efficiency measurements on all 64 after annealing

### 3.4 Conclusions

This chapter presented the irradiation campaign done to evaluate the reliability of the 2<sup>nd</sup> generation of SPACIROC family in a radiation environment. Therefore, the SPACIROC2 ASIC has been evaluated for TID and SEEs with various particle beams: ion, protons and X-rays.

The DUT will operate with very low error rates in the JEM-EUSO radiation environment as it will be expected up to 2000 errors over the full 5-years mission (worst case scenario). Due to the very low dose rate any increase of the leakage currents will be mitigated almost instantly due to rapid annealing. However, in terms of SEEs more tests are needed in order to have a complete view of the DUT reliability, as the LET in space may reach a value up to 40 MeV ·

$\text{cm}^2/\text{mg}$ , and this means that the SEL rates for high value LETs need to be parametrized. Yet, due to very low probability of events with recoil ions having stopping power in Si above  $12 \text{ MeV} \cdot \text{cm}^2/\text{mg}$ , the SPACIROC2 is safe to use in JEM-EUSO environment even for systems with 5000 PMT devices due to the very low rates of SEU and much lower rates of SEL (if any), which translate in per-mile system efficiency degradation over the entire operation time.

Due to the low dose rate expected in the LHCb-RICH radiation environment for the RUN 3, of about  $0.008 \text{ rad/s}$ , the DUT will definitely survive the TID of  $200 \text{ krad (Si)}$ , as the rapid annealing at room temperature will prevent the cumulative TID effects. The main concern remains the SEEs, as the current irradiation tests did not reach the maximum expected LET of  $15 \text{ MeV} \cdot \text{cm}^2/\text{mg}$ . Therefore, more testing has to be done in order to establish a proper extrapolation, yet it is already clear that SEL rates will be very low, if any. Also, the expected SEU rates will be low with per-mile effect or lower on the PID efficiency of RICH.

# Chapter 4

## Characterization of the KINTEX-7 FPGA Under Radiation Exposure

With the introduction of the reconfigurable devices, especially FPGAs, there were made remarkable achievements in the development of high-performance computing systems. These rely on the reconfigurability of such devices to define custom logic architectures in order to fulfill the needs of an end-user application. FPGAs are programmable logic devices which embeds a large variety of hard logic resources such as: user Flip-Flops (FF), Look-up Tables (LUTs), embedded block RAM (BRAM), high-speed serial transceivers, phase-locked loops (PLL), digital signal processing (DSP) resources, multipliers, clock management blocks etc. The user can implement/create sections of circuitry which can run in parallel ensuring a high-speed response of the system. Modern FPGAs embeds hard processors enabling users to benefit from more versatility and more high performance of a such device, known as System on Chip (SoC).

The FPGAs are becoming a common and very accessible choice to be used in harsh environments with radiation background, and to replace ASICs in aero-space and high energy physics experiments. Being able to reconfigure a system is a very valuable asset as the functionality of a readout system can be upgraded without the redesign of the readout electronics. There are at least six main advantages which enables the user to benefit from choosing the FPGAs over ASICs in such applications:

- ❖ lower price as there is no R&D and manufacturing of a new ASIC for a target application, and low non-recurring engineering costs (NRE);
- ❖ high-logic density;
- ❖ in-flight full reconfigurability, allowing the user to change dynamically the configuration;
- ❖ short-design cycle;
- ❖ possibility to implement partial reconfigurability and self-correcting mechanisms.



The sensitivity to radiation of commercial-grade FPGAs is largely known by the communities, and people have been investigating them and developed methods to reduce the impact of radiation-induced failures into their end-user applications. The main concern is the integrity of the configuration memory (CRAM) used to store the FPGA configuration bits. The FPGA configuration memory is used to define the user FPGA circuit, and it can be as large as more than 100 Mb [214] for large FPGAs. SEU in the configuration memory may lead to changes in the FPGA circuits ultimately leading to functional failures of the systems.

It is well known and described by the literature that all commercial-grade FPGA technologies are sensitive in various ways to TID and SEEs. There are three FPGA types commonly used in radiation environments either in space or accelerator experiments: flash-based, SRAM-based and antifuse. Being different technologies, each of them have distinct advantages and drawbacks with respect to the response to radiation, and the best compromise has to be chosen depending on the end-user application and its experiment environment. However, all FPGAs types depending on their technology node may manifest increase of the leakage currents due to TID.

*The Antifuse FPGAs* are one-time programmable devices which are using fuses to permanently configure the state of each FPGA configuration bit. Such devices are nonvolatile and the configuration is retained even when they are unpowered. Although is a huge drawback as the FPGA configuration cannot be changed once the fuses have been spiked/zapped, the antifuse FPGAs are known to be immune to SEUs in the configuration memory [215]. The main concern in terms of radiation induced SEE failures, are the SEUs and SETs within the user logic resources (FF, LUTs, BRAM etc).

*The flash-based FPGAs* are using internal flash memories cells as a primary resource to store the FPGA configuration bits. The states in a flash memory, are stored by using an electrically isolated floating gate. This feature makes these devices to be nonvolatile with respect to a power cycle, however unlike antifuse FPGAs, they can be reconfigured for a limited number of times. The configuration memory of a flash-based FPGA is known to be immune to radiation-induced SEUs [216]. As like in the antifuse FPGA case, the primary concern for radiation-induced SEEs are the SEUs and SETs within the user logic resources. However, the flash memory cells are known to be very sensible to TID, due to failures of the internal voltage charge pump used for high-voltage erasing and writing operations as well as the degradation of the threshold voltage. They translate as failures in the programming circuits, and were observed at low TID, of 30 krad (Si) [217].

*The SRAM-based FPGAs* are using static memory cells to store the FPGA configuration bits. Due to the fact that these static memory cells require power to maintain the configuration sequence, they are volatile and the state of the FPGA configuration bits is lost when the power is off. The SRAM-based FPGAs can be reconfigured an unlimited number of times, which turns them in excellent solutions in certain cases. The primary concern for such FPGAs is the reliability of the configuration memory against radiation-induced SEUs. The SRAM cells are very sensible to SEUs, therefore the presence of SEUs in the configuration memory is the most common failure of these FPGAs. Compared with the case of the other FPGA types, concerns regarding radiation-induced SEE within the user logic resources are generally more stringent. Although, modern SRAM-based FPGAs implemented with tens on nanometers technologies have been proved to be very resilient against TID effects, even at high TID over 1 Mrad [218].



This chapter will present the experimental setup and the irradiation campaign carried out on a SRAM-based FPGA proposed to be used in the LHCb-RICH radiation environment. Although, most of the results were confirmed with the ones available in the literature, several new resources were tested as well as new testing methodologies and mitigation techniques were investigated. Based on the obtained testing results, several conclusions are reached and the results are extrapolated to the expected radiation environment during the **LHCb-RICH Upgrade Phase Ia**.

## 4.1 Device Under Test

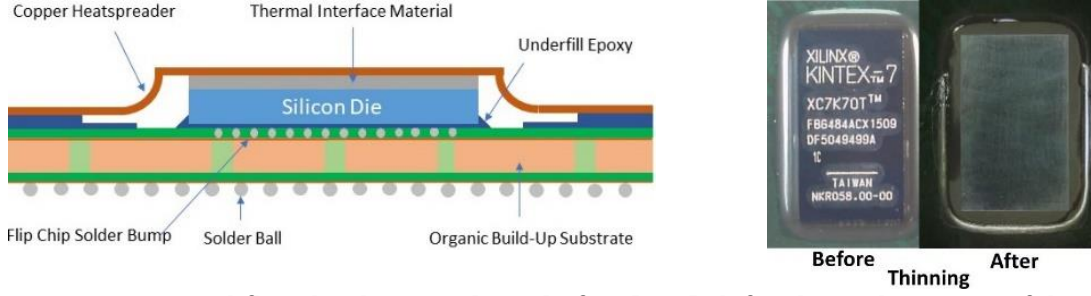
The smallest device from Xilinx KINTEX-7 family, **XC7K70T**, was chosen as the main active component on the LHCb-RICH PDMDBs, which read out the CLARO output triggers (see section 1.5.3). It has sufficient high-speed I/O pins to provide the required connectivity to the single-ended (SE) CMOS 2.5 V CLARO signals as well as the LVDS and SE CMOS 1.5 V signals to the GBTX ASIC.

The Xilinx 7-series family, which includes the XC7K70T, is the first FPGA family manufactured by using the advanced TSMC's high performance and low power (HPL) CMOS process which embeds a 28 nm high-k metal gate (HKMG) technology node [219]. To cover a broad range of user connectivity, it comes with two types of I/O banks: high performance (HP) and high range (HR). In table 4.1 are given the main features for the XC7K70T extracted from its datasheet [106]:

**Tab. 4.1** XC7K70T main features, see [106]

|                         |           |
|-------------------------|-----------|
| <b>CRAM size (bits)</b> | 18884576  |
| <b>BRAM size (bits)</b> | 4860000   |
| <b>Maximum I/O pins</b> | 300       |
| <b>I/O Banks</b>        | 6         |
| <b>Logic Cells</b>      | 65600     |
| <b>DSP Slices</b>       | 240       |
| <b>Logic Slices</b>     | 10250     |
| <b>Maximum FFs</b>      | 82000     |
| <b>Maximum LUTs</b>     | 41000     |
| <b>Packaging</b>        | Flip-Chip |

The XC7K70T, addressed as DUT from now on, came packaged as flip-chip device with its die wired on the bottom side as it is shown in the left side of fig. 4.1. Therefore, in compliance with the radiation testing standards [174], the thermal interface material and its substrate from the top side of the package was thinned from about 250 to about 60  $\mu\text{m}$  in order to allow the ion beams to reach to the device active layer. Five samples were thinned and pictures of the package for one FPGA sample before and after the thinning operation is shown in the right side of fig. 4.1.



**Fig. 4.1** Typical flip-chip layout adapted after [220] (left side) and pictures of the FPGA package before and after the thinning operation (right side)

Although the XC7K70T-FBG676 (part number) device was chosen for the LHCb-RICH PDMDBs, in order to simplify the design of the hardware for the irradiation campaign the XC7K70T-FBG484 (part number) device was used. Since they have the same die, the only difference between these two packages is the number of I/Os which are bounded out from the package, as the FBG676 has more I/O pins than the FGB484. Therefore, a complex and custom experimental setup to power, monitor and control the DUT was designed for this purpose. Various firmware versions were designed to evaluate the SEE reliability of multiple general-purpose resources such as FFs, CRAM, BRAM and I/O blocks. Also, the susceptibility of the DUT to radiation-induced SEL as well as to TID cumulative effects was measured.

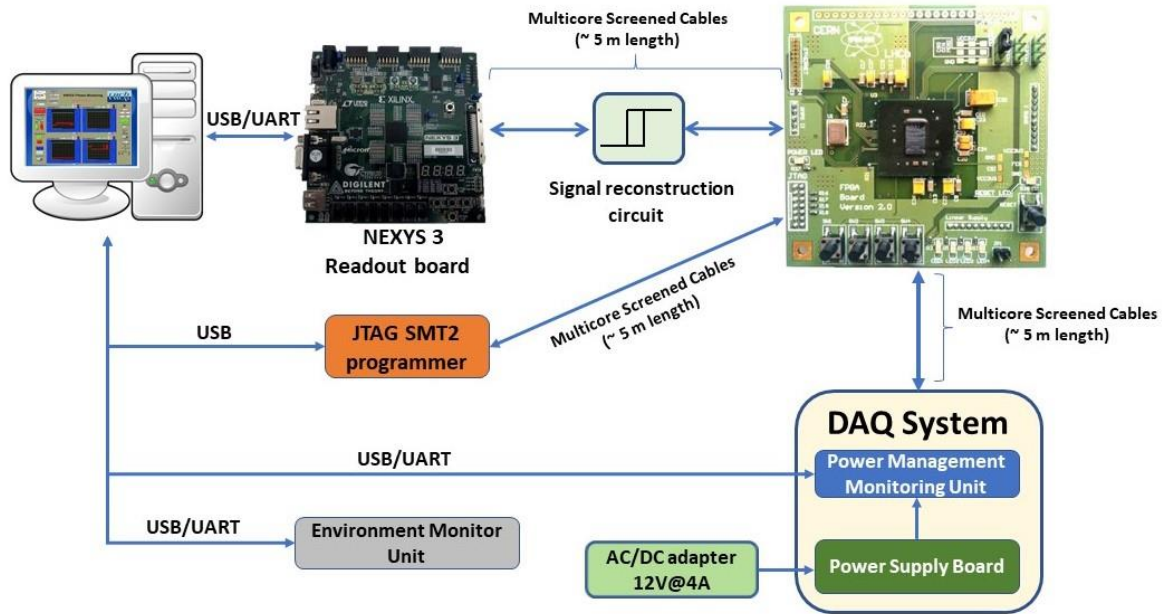
## 4.2 Experimental Setup

The general layout of the DUT experimental setup, shown in fig. 4.2, was designed within LaRA EED laboratory [202] to test and evaluate the DUT, and is composed of four main components: the DUT test board, the power supply board, the DAQ system and the readout board. It was designed to comply with the radiation testing constraints as well as to be easy to adapt for various irradiation environments and facilities, e.g., device placed either in vacuum chambers for irradiation with heavy ion beams or outside on a mechanical support with the proton-beam or X-ray beam extracted in air [221]. Due radiation protection constraints all the DAQ-units, with incoming/outgoing connections to the DUT test boards were placed at a safe distance of at least 5 meters. This ensured resilience of the experimental setup against any stray radiation from the DUT test board (backscattering) or from the beam itself, as the irradiation of the DAQ system had low probability and low intensity in this configuration.

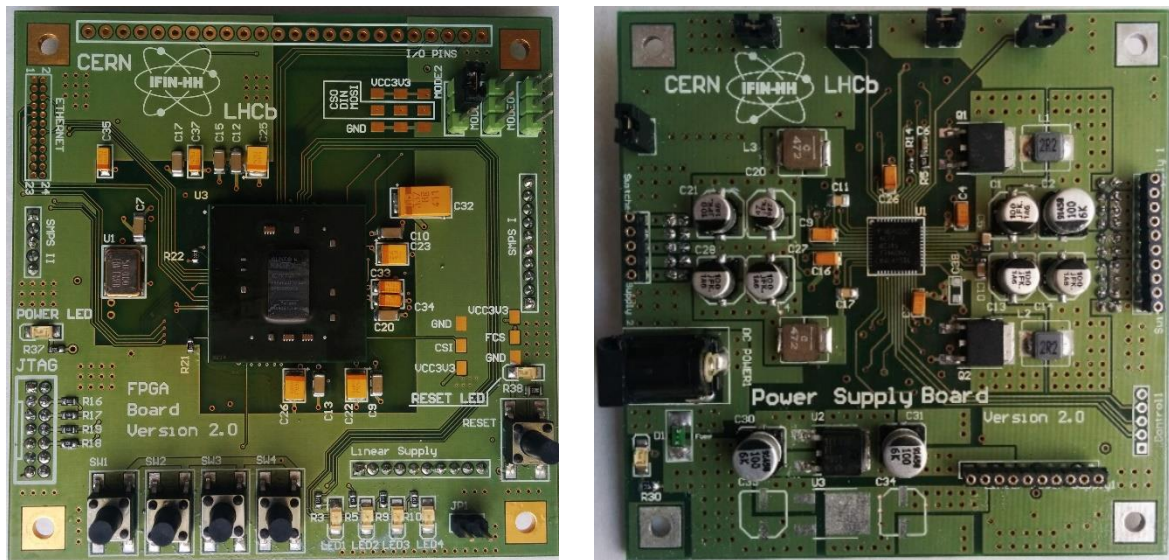
*The DUT test board*, shown in the left side of fig. 4.3, was designed as simple as possible to ensure the full functionality of the DUT with minimum external components. No external memory to store the configuration was used. Therefore, the DUT was set to operate in JTAG mode and the only way to write its configuration was via the JTAG port. Due to the obvious radiation constraints, this operation mode will be also used in its target application, the LHCb-RICH readout. Optional components such as push-buttons and LEDs were routed out just for debugging purposes. To run the DUT logic, two clocking possibilities were provided: an onboard 100 MHz SE clock and the possibility to receive an external clock from the readout board. Depending on the firmware design they can be used either independently or

simultaneously to run the logic. The layout of the DUT test board was 80 mm x 80 mm and it was designed using an 8-layer PCB.

The power to the DUT was delivered via dedicated power connectors which were linked using multicore screened cables to the power supply board, shown in the right side of the fig. 4.3. To compensate for the voltage drops on the long cables, the power supply feedback connections on the most important power rails were moved at the end of the cables, near the DUT.



**Fig. 4.2** The general layout of the DUT experimental setup



**Fig. 4.3** DUT test board (left side) and its power supply board (right side)

The power supply board was designed around ADP5050 [222] integrated circuit. This circuit is a dedicated solution to power complex integrated circuits such as the FPGAs. It is a

switching mode power supply controller and it embeds the following features which were extended to the power supply board:

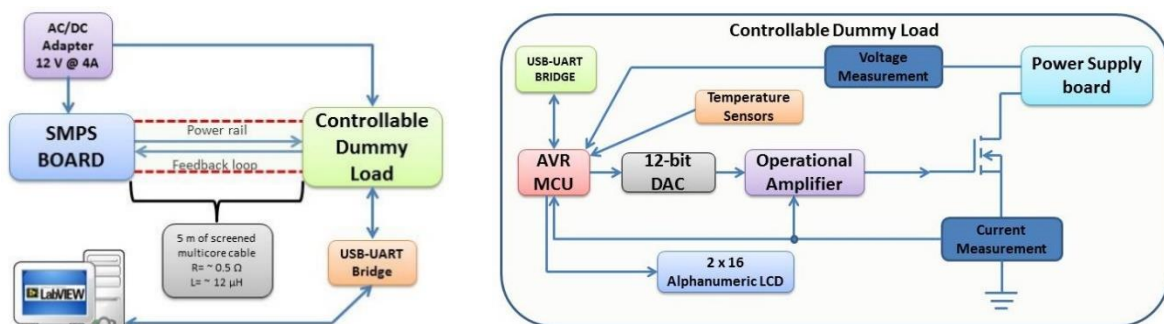
- ❖ wide input voltage range: 12 V was used at the nominal voltage in this setup;
- ❖ overheating and overcurrent protections;
- ❖ independent soft start and enable functions for each power supply channel;
- ❖ high efficiency: 2 high current converters have synchronous rectifier capabilities;
- ❖ optional digital control via I2C;

Due to the fact that the ADP5050 only facilitate up to four high current switching mode converters, two more external power supplies were additionally added on the board. A summary of the all power rails provided by the power supply board to the DUT are given in table 4.2.

**Tab. 4.2** The power supply rails and their connection to the DUT test board

| Power Rail    | DUT Connection                                                |
|---------------|---------------------------------------------------------------|
| 1 V @ 4 A     | VCCINT (core) and VCCBRAM (BRAM)                              |
| 1.5 V @ 4 A   | VCCIO for BANK14 and BANK34                                   |
| 1.8 V @ 1.2 A | VCCAUX and VCCIO for BANK33 and BANK16                        |
| 1 V @ 1.2 A   | MGTAVCC (internal transceivers)                               |
| 3.3 V @ 1 A   | VCCO (JTAG and configuration) and VCCIO for BANK14 and BANK15 |
| 1.8 V @ 1 A   | VCCxADC (internal ADC block)                                  |
| 1.2 V @ 0.2 A | MGTAVTT (internal transceivers)                               |

The power supply quality is a very important step to ensure the functionality of DUT without errors or failures. In this way, a custom electronic load was designed to test and stress the power supply board and its power rails and to measure its output quality [223]. The test bench used to test the power supply board is shown in the left side of fig. 4.4 and the general architecture of the electronic load used to simulate high current events is given in the right side of fig. 4.4.



**Fig. 4.4** The power supply test bench (left side) and the architecture of the electronic load (right side) -self citation [223]

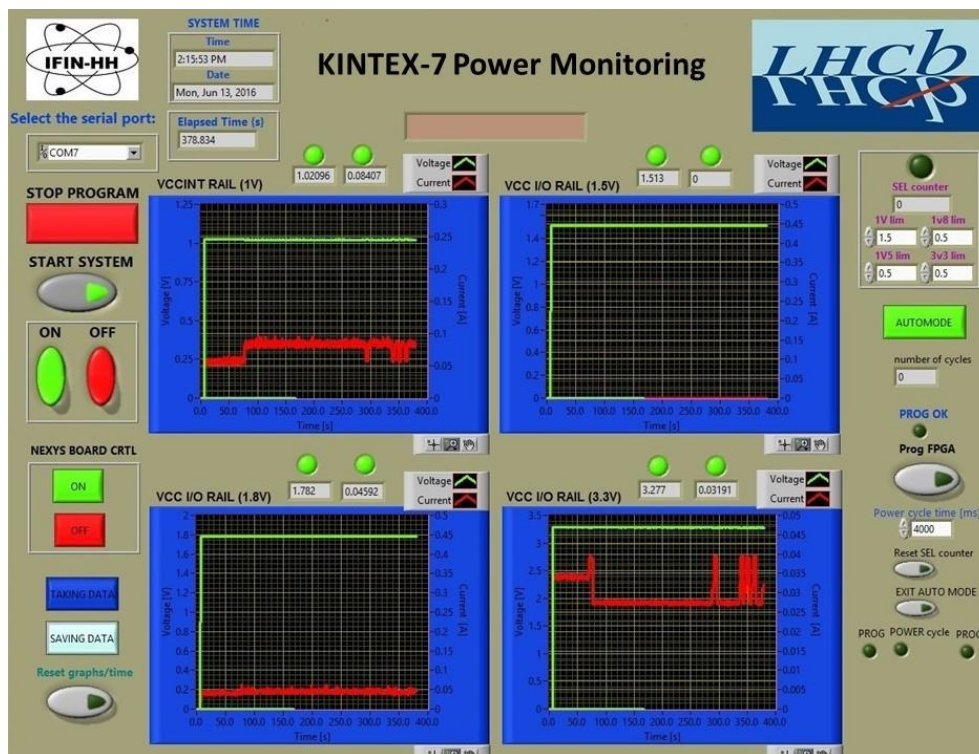
The DUT core power rail, VCCINT, is a very sensible power rail, which if it is not stable it may produce damage to the DUT. According to its datasheet, it should not exceed 1.1 V as



it may trigger the internal overvoltage protection diodes, which may lead to a permanent short circuit inside the DUT. On the opposite side, if this voltage rail has an amplitude less than 0.87 V, for a long enough period of time, it may trigger a reset condition within the DUT. Therefore, this power rail was intensively tested by inducing high-current states within the electronic load to simulate SEL-like events. Another important parameter which was tested, was the transient response of the power supplies. Radiation may induce high and abrupt current states, e.g. from 0.1 A to 2 A, therefore the power supply needs to have a fast-transient response time to compensate the output voltage when such high currents occur.

Overall, all the power lines responded well to high current states induced by the electronic load and the measured values were in the limits provided by the vendor.

The custom DAQ system has four power rails highlighted with green in table 4.2. These were monitored due to their important role in powering key internal blocks of the DUT. The power monitoring was done with high-side current sense amplifiers, on which the current flow through a shunt resistor is converted into a voltage. The resulted voltage is filtered through a low-pass RC filter before is fed into the ADC block of an 8-bit microcontroller. The microcontroller acquires the data with a resolution of 1 mV and equivalent to 1 mA, respectively, and sends it, on user request, via an UART communication to a LabVIEW GUI at every 50 ms. The LabVIEW GUI shown in fig. 4.5 is used to communicate to the DAQ system and to ensure the power management and power monitoring of the DUT. The user can perform power cycle of the DUT as well as to save the data in ASCII files for a later offline analysis. Several additional functions were implemented to facilitate the testing of dedicated events such as: SELs.



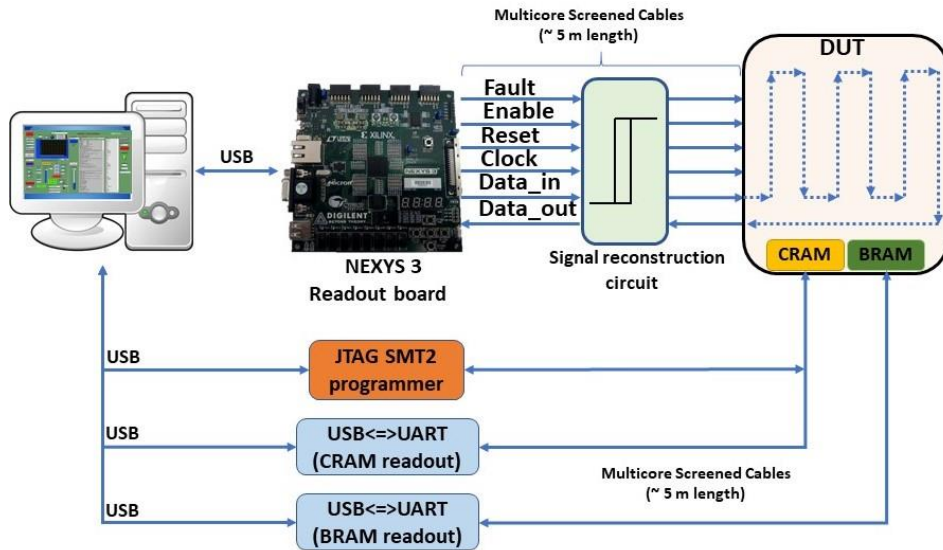
**Fig. 4.5** The LabVIEW GUI designed to power and monitor the DUT as well as to control the DAQ system

A dedicated system was used to monitor the environment parameters such as the temperature and the humidity in the vicinity of the DUT while was tested [224]. Such information is needed to provide a better understanding on how the DUT is affected by radiation as well as to parametrize and correlate its radiation response.

An important part of the experimental setup was the NEXYS3 commercial readout board [225] proposed as readout and control board of the firmware inside the DUT as well as to extract the SEUs rates. Its functionality and its role will be described in the section 4.3.

### 4.3 FPGA Firmware for Radiation Testing

To evaluate the DUT reliability – and to count radiation-induced SEEs, focusing on counting SEUs, SETs and SEFIs to determine their cross-sections –, dedicated firmware architectures were designed to test key resources of the DUT. Therefore, tests were carried out to measure the SEU rates in CRAM, BRAM, user FFs, and I/O blocks. The NEXYS3 readout board was used: to control the DUT logic circuitry during testing of only the FFs resources, and for laboratory tests. To monitor the CRAM and BRAM integrity, two external USB-UART connections were used to read out the data from these two types of memories. A simplified scheme of the connections to the DUT is shown in fig. 4.6, and displays the connections used in case of each testing firmware.



**Fig. 4.6** The simplified DUT firmware readout and control architecture

The device reliability, in context of radiation-induced SEUs affecting certain logic architecture running within the DUT, was established by counting and monitoring the effects of the SEU errors through various logic chains created within the DUT. It all starts from the readout board which sends a 32-bit length bitstream of serial data (data\_in) together with a clock signal to the DUT test board. Inside the DUT, depending on the firmware version, a path of user FFs is created within the device and if the certain conditions are met, the bitstream is shifted through the whole chain of logic resources. Then the shifted bitstream of data is sent

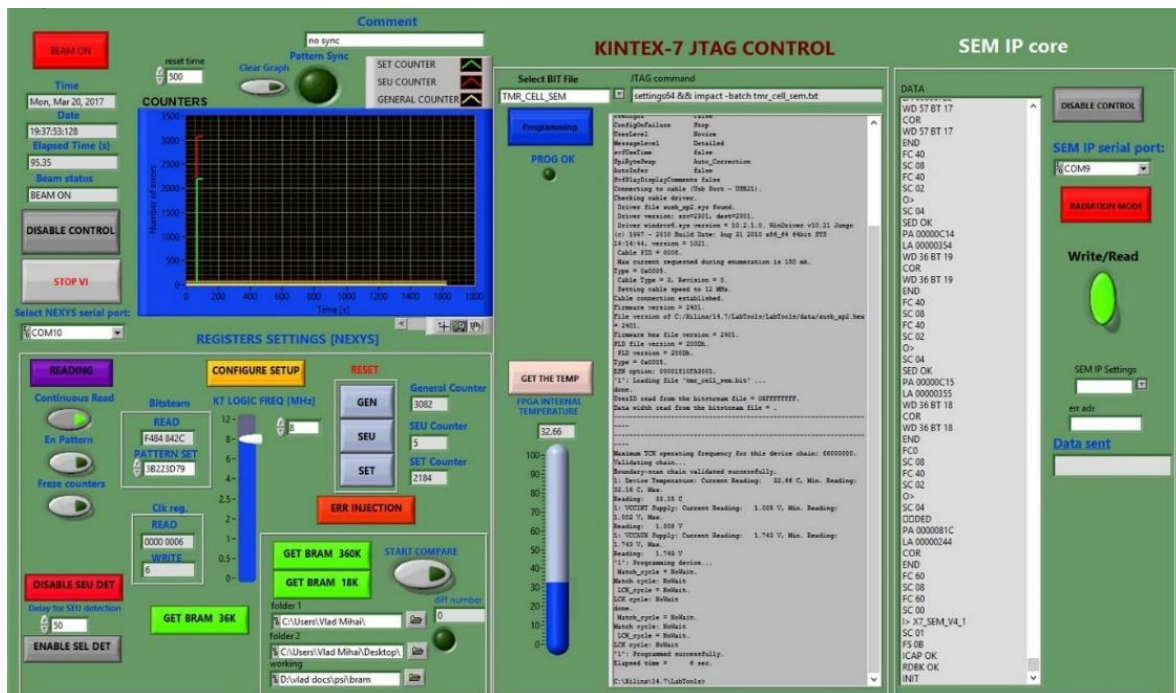
back to the readout board (data\_out). The readout board takes back the bitstream data and compares it against the initial bitstream data. If there are differences between the data, then a mismatching failure will be highlighted and saved in a SEU counter register. The process is started again if all conditions are met.

The readout board is controlled and monitored using an additional LabVIEW GUI presented in fig. 4.7. From this GUI the user can set the bitstream pattern sent to the DUT as well as the external clock frequency. This GUI is synchronized with the other GUI used for power management, and it has additional features, like: BRAM and CRAM monitoring and DUT JTAG control.

The BRAM and CRAM monitoring are done without the need of the readout board by reading out the status data from dedicated firmware through USB-UART connections from the DUT test board. In some cases, both operations can be done in the same firmware.

The JTAG control section is used to reconfigure the DUT when is necessary, as well as to read out some parameters like: the device ID and its internal temperature. Such parameters are needed to perform checks of the JTAG core, especially to its test access point (TAP) controller. The DUT reconfiguration can be automatically triggered when a user defined condition is met such as the corruption of the CRAM or the DUT logic has a high SEU rate.

A validated SEU within the DUT logic or BRAM is flagged “true” when the CRAM is simultaneously SEU free. Therefore, integrity of the CRAM is mandatory, and to be monitored all the time, when checking the integrity of other DUT resources. This allows to separate any errors seen in the logic by the corruption of CRAM, from the SEU in other resources.



**Fig. 4.7** The LabVIEW GUI designed to control the DUT firmware functionality, as well as to perform CRAM monitoring and reconfiguration

Several firmware versions were proposed and designed in order to create a path within the DUT by using FFs and LUTs resources. Each firmware has a unique configuration, and all of

them were tested against radiation-induced SEUs. Each firmware architecture is described in section 4.3.2.

Careful attention was given to ensure the CRAM integrity in the DUT, as several mitigation techniques were tested and are described in section 4.3.1.

### 4.3.1 Solutions for Mitigating Errors within FPGA Configuration Memory

The SRAM cells are very susceptible to radiation-induced SEUs, and a very important step is to ensure the CRAM integrity when testing other resources of the DUT. SEUs in the CRAM, depending from case to case, may change the user circuitry and errors/failures may be induced in critical areas within the devices which makes end-user application to fail or unstable. In some cases, the corruption of the CRAM may lead to SEFIs, placing the DUT in an unknown state such as: high-current states, hardware reset, operational freeze etc.

To define and configure a user logic circuit, this DUT uses 18884576 bits of CRAM. A configuration frame represents the smallest unit of configuration within such a device. The CRAM bits are arranged in 5843 configuration frames and each of them is composed from 101 32-bit words [226]. The central location of each frame, consisting of 50<sup>th</sup> word, contains the Error Checking and Correction (ECC) information used to provide single-bit error correction as well as to detect double-bit errors (SECODED).

The CRAM frames can be accessed either internally from a user design via the Internal Configuration Access Port (ICAP) [226], or externally through the following configuration modes: JTAG, Master SelectMAP, Slave SelectMAP, Master Serial, Slave Serial, Master Serial Peripheral Interface (SPI) and Master Byte Peripheral Interface (BPI). The easiest way to access the CRAM is in the JTAG mode, as it requires few connections to the DUT, while the fastest way to reconfigure the DUT is by using the 32-bit SelectMap parallel interface. However, due to the fact that JTAG protocol is a serial connection it is the slowest reconfiguration interface, as its clock frequency can go up to 66 MHz. Faster reconfiguration times can be archived by using the SelectMAP interface with clock frequencies up to 100 MHz.

Due to the fact that the CRAM resource is the largest resource within the device, it makes it potentially the most vulnerable to radiation-induced SEUs. In this way, by accessing the CRAM resource several mitigation approaches can be implemented to scrub the memory frame for errors: blind scrubbing, readback scrubbing, internal scrubbing and hybrid scrubbing [227].

*The blind scrubbing* is the simplest procedure to correct the SEUs within the configuration memory. It is done by a full reconfiguration of the device with a golden bitstream regardless any information about the SEU presence within the CRAM. This procedure can be set to be done regularly, at various time intervals defined by the user. Although, is a very simple mitigation technique, it adds dead times to the functionality of the system while the DUT is being reconfigured. In some cases, this method has been found to cause high current states within the device, while is irradiated [228]. This is due to the fact that the configuration memory is placed in the write mode while the DUT is being configured and a SEU strike in the configuration logic may cause bad/corrupted data to be written in the CRAM frames.

*The readback scrubbing* is a way mitigate the SEUs within CRAM by performing a readback operation of the configuration frames. The readback frames are compared with



reference frames, and only the SEU-affected frames are written to the device. This procedure is considered to be more robust against SEUs within the configuration logic itself than a bling scrubbing procedure. This is due to the fact that during readback scrubbing the configuration logic is placed in read mode, and only the affected frame is set to write [229]. In this way, any SEU strike within the configuration logic interface will not cause bad/corrupted data to be written into the whole CRAM.

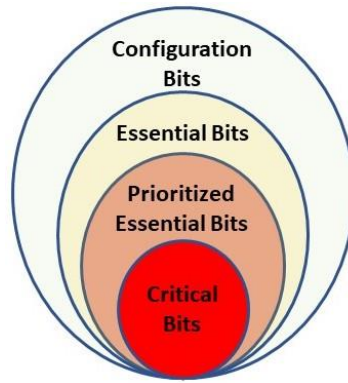
*The internal scrubbing* use dedicated logic to detect, classify and correct SEUs within the configuration memory. Such dedicated logic is the Soft Error Mitigation (SEM) IP Core from Xilinx [230]. The SEM core is a dedicated solution provided to help with detection and mitigation of radiation induced SEUs as well as to simulate such events into the user designs by performing error injection into CRAM frames. Generally, it has two main components: individual frame ECC and full-device Cyclic Redundancy Check (CRC). The frame ECC is able to detect all single-bit errors within a CRAM frame, and in some cases some multi-bit errors. The SEM is mainly used to detect errors within the CRAM frames, however the error correction feature within the SEM core is optional and it can be done by using one of the following operation modes:

- ❖ Repair mode: is based on the ECC algorithm and supports correction of single-bit errors within a CRAM frame;
- ❖ Enhanced repair mode: is using both ECC and CRC algorithms and supports single bit and adjacent double-bit error within a CRAM frame;
- ❖ Replace mode: supports correction of arbitrary number of errors within the CRAM frames by replacing the frames with reference data from an external storage;

*The hybrid scrubbing* solutions use the combined advantages of internal and external scrubbers. Therefore, in most of the hybrid scrubbers, the SEM core is used together with an external interface to access the CRAM frames. An example of a hybrid scrubber configuration is the use of the SEM core with an external JTAG-based readback scrubber [231]. The SEM is used to detect and correct all single-bit SEUs within a frame. The FPGA communicates with the external scrubber through the JTAG interface and based on the information provided by the internal scrubber it performs the reconfiguration of the frames with multi-bit errors or full reconfiguration of the device.

Not all the radiation-induced SEUs within the CRAM have a real impact on the user logic design. Therefore, to evaluate the impact of the CRAM SEUs with respect to an user logic design, the notion of essential bits [232] was induced by Xilinx.

Generally, depending on the user logic design, CRAM bits are classified as: non-essential and essential bits. If an essential-bit is flipped by an SEU, it may cause changes in the design circuitry. Depending on their role into a circuit, they can be reduced to prioritized essential bits. Further, the essential bits can be classified into: non-critical and critical bits, which if flipped may cause errors within the design circuitry that affects the “useful” output of the device (“useful” being most of time subjective as the definition is user-dependent). The relation between the CRAM bits and the critical bits is shown in fig. 4.8.



**Fig. 4.8** Relation between configuration bits and critical bits within the CRAM for Xilinx 7-series FPGAs (adapted after [232])

Only the designer itself can establish how an essential bit can impact its design circuitry when is hit by an SEU. To understand better how an essential bit may be categorized as a critical bit into a design, let us see what impact have the radiation-induced bit flips on a basic two-input NAND gate. The two-input NAND gate truth table is shown in table 4.3, and with the SEU changing the state of the input B, the output state is changed from its correct value only 50 % of the time. Due to the fact that the NAND gate is symmetric, the same ratio is found if the input A is affected by SEU. Therefore, to first approximation, the essential/critical bits ratio is 50%. In this way, the designer may categorize the essential bits which are prone to change functionality of its design circuitry as critical bits. This assumes the A and B feed is static and not dynamic, as if the feed changes over time an intermittent critical error will be introduced.

**Tab. 4.3** SEU impact on a two input NAND gate [227]

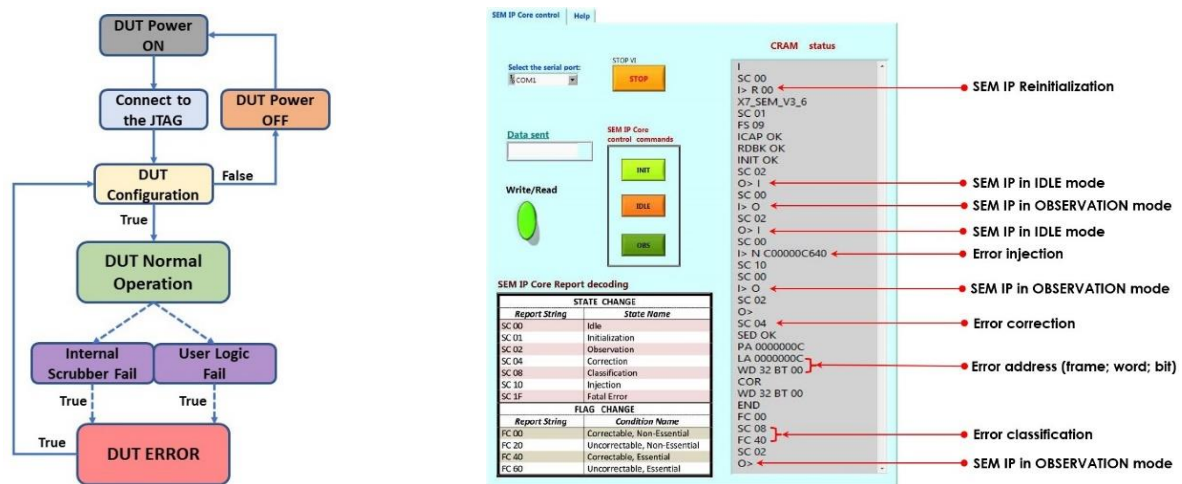
| A | B | Out | SEU B | SEU OUT  | Impact?    |
|---|---|-----|-------|----------|------------|
| 0 | 0 | 1   | 1     | 1        | No         |
| 0 | 1 | 1   | 0     | 1        | No         |
| 1 | 0 | 1   | 1     | <b>0</b> | <b>Yes</b> |
| 1 | 1 | 0   | 0     | <b>1</b> | <b>Yes</b> |

To ensure the CRAM integrity within the DUT while is irradiated, a hybrid scrubbing architecture was implemented to monitor, detect and correct the radiation-induced SEUs. Its basic architecture is shown in the left side of fig. 4.9 and is composed from the SEM core as internal scrubber and an external JTAG-based blind scrubber. The internal scrubber is mainly used to detect and correct the single-bit errors within each CRAM frame. By reading out the SEM status, uncorrectable multi-bit errors as well total failures within the SEM core logic are detected and the full reconfiguration of the DUT is triggered. The management of the implemented hybrid scrubber is done by the LabVIEW GUI presented in fig. 4.7. Generally the blind scrubbing is triggered by two conditions:

- ❖ *when internal scrubbing is used*: the failures within the internal scrubber triggers the full reconfiguration of the DUT;

- ❖ *no internal scrubbing used*: the failures within the user-designed circuitry triggers the full reconfiguration of the DUT;

Due to the fact that the internal scrubber is instantiated within the SRAM cells (configuration memory) and DUT logic resources, its resilience to radiation-induced SEUs is questionable. If its logic core is hit by a SEU it can lead to failure as well as to the case where the DUT is placed in an unknown state. Therefore, to study the susceptibility of the SEM core, a DUT firmware with only the SEM core instantiated in the user logic was used. A LabVIEW GUI, shown in the right side of fig. 4.9 was designed to test the SEM core. By injecting SEUs into the CRAM, it was observed that a fraction of them cause global failures of the SEM core, and the DUT had to be reconfigured. A very small fraction of the injected SEUs caused high current states within the DUT core power rail, which were corrected by a full reconfiguration.



**Fig. 4.9** The DUT hybrid scrubbing architecture (left side) and the LabVIEW GUI designed to monitor and validate the SEM core as internal scrubber (right side)

The error correction rate of the SEM core when is used as internal scrubber is highly dependent on the error rate. It takes 610  $\mu$ s to correct each single-bit errors when running the ICAP interface within this DUT at its maximum frequency of 100 MHz. Therefore, large error rates can compromise the SEM logic, as some errors cannot be corrected in time (this is valid for some high-Z ion beam tests with about 1kHz error rates or even higher).

Carefully-selected design has to be chosen when taking into account the usage of the SEM core as internal scrubber in environments where high error rates are expected. Its malfunction can lead to failures within the design circuitry. By using the Xilinx Vivado environment, the essential bits for a design with only the SEM core (configured in one of its two operation modes) were extracted and are given in table 4.4. It is approximated through error injection that the SEM core logic has 45.9 % critical/essential bits ratio, where critical bit flipping may trigger a failure within the SEM logic [227].

**Tab. 4.4** Summary of essential and critical bits for the SEM core within the DUT

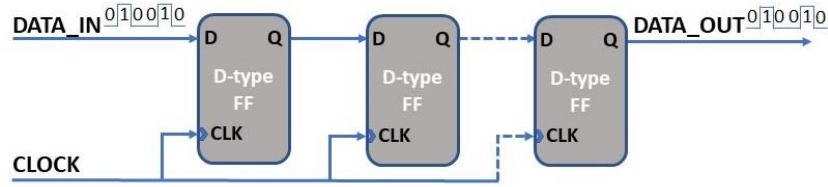
| Firmware      | Essential bits (all CRAM) | Critical bits (45.9%) |
|---------------|---------------------------|-----------------------|
| SEM-rep. mode | 91118 (0.48%)             | 49295                 |
| SEM-enh. mode | 154474 (0.82%)            | 83570                 |

### 4.3.2 Solutions to Test and Mitigate Errors for Dedicated Logic Resources

Several firmware versions were designed to test logic resources like the FFs, BRAM and the I/Os. For some of them the SEM core internal scrubber was used to ensure the error mitigation as well as to test the CRAM itself and to extract the SEU rates within the CRAM while the DUT was being irradiated.

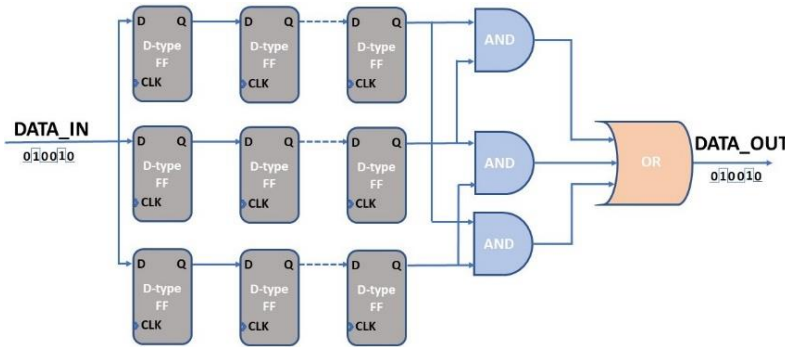
The SEU rates within the user FFs were measured by using four firmware configurations with the FFs arranged in single chain and in various TMR configurations.

A single chain of FFs configuration is a general architecture of the FFs arranged in a shift chain without any redundancy. Its architecture is shown in fig. 4.10. While the data (data\_in) is shifted into the DUT FFs chain, if a single FF from the chain is affected by SEU, then its output data (data\_out) will be corrupted. In this way, the readout board will detect the corrupted data, and a SEU is counted. The VHDL code written to create this circuit is available in annex A1.



**Fig. 4.10** Single chain of FFs architecture

A way to reduce the SEU error rates within the FFs is by using three individual and identical FFs chains coupled with a majority voter implemented with one LUT. In this way, a basic TMR architecture is designed. Although, it will generally reduce a bit the error rates within the FFs, there is a small chance that the voter itself may be affected by a SEU hit.



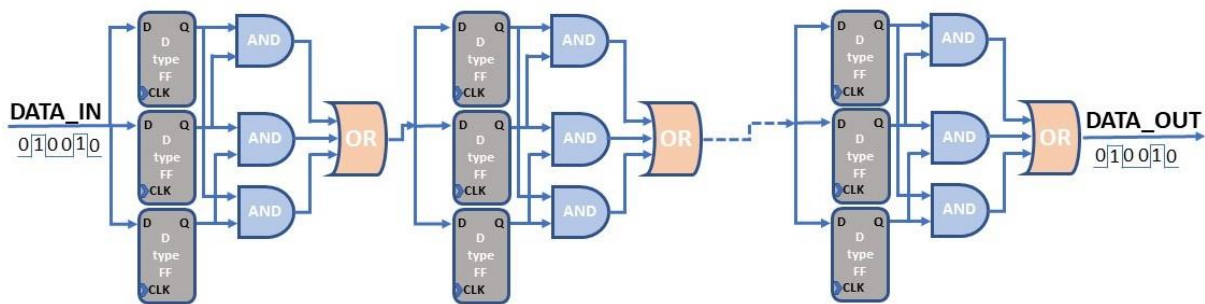
**Fig. 4.11** Basic TMR architecture

The basic TMR architecture uses three times more FFs and a LUT for the TMR majority voter. According to its truth table given in table 4.5, if only one chain of FFs is corrupted by SEUs then the output data available at the output of the majority voter will still be valid. However, if two or all chains are corrupted by SEUs then the output data is no longer valid.

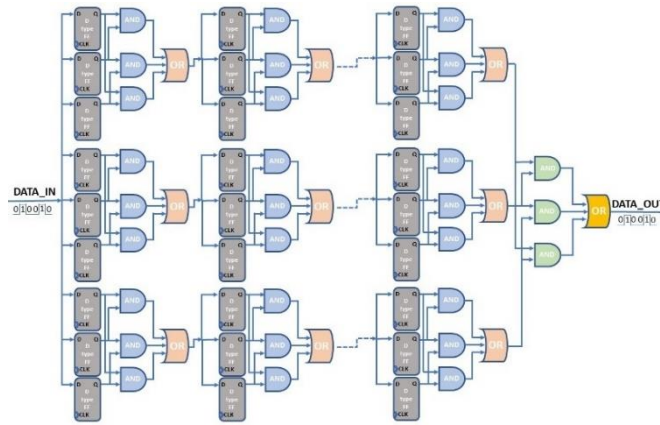
**Tab. 4.5** TMR majority voter truth table

| Chain A | Chain B | Chain C | TMR voter output |
|---------|---------|---------|------------------|
| 0       | 0       | 0       | 0                |
| 0       | 0       | 1       | 0                |
| 0       | 1       | 0       | 0                |
| 0       | 1       | 1       | 1                |
| 1       | 0       | 0       | 0                |
| 1       | 0       | 1       | 1                |
| 1       | 1       | 0       | 1                |
| 1       | 1       | 1       | 1                |

The TMR majority voter can be implemented further at individual FF level, ensuring redundancy of each 3 FF cell [233]. Shown in fig. 4.12, this architecture may enhance the design reliability, however, unlike the basic TMR, it requires one LUT for each redundant FF structure. Therefore, the overall resource usage within the DUT increases. If two FFs from the same redundant FF structure are affected by SEU or the TMR voter itself is corrupted, the output data is no longer valid. The VHDL code used to implement the FF level TMR architecture is available in annex A2.

**Fig. 4.12** FF level TMR architecture (adapted after [233])

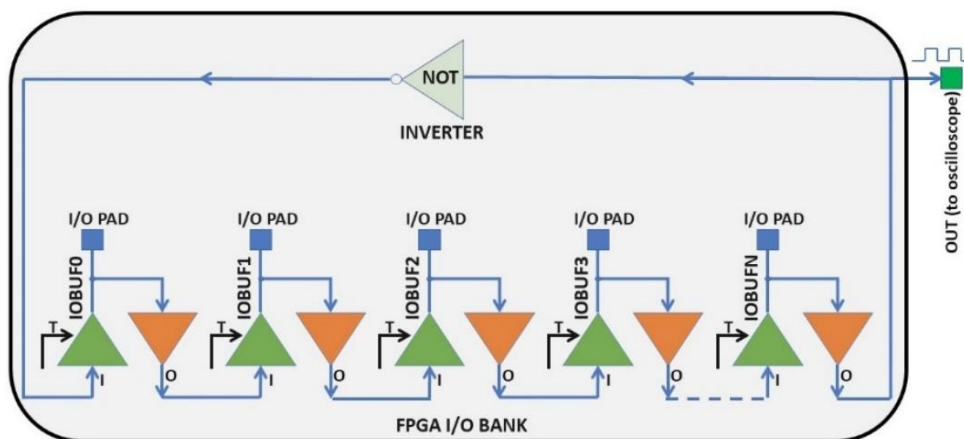
Another architecture was proposed by combining the basic TMR and FF level architectures to further enhance the design reliability. Its architecture is shown in fig. 4.13 and the VHDL code used to implement it is available in annex A3. The extended TMR architecture in some cases may introduce an increased reliability to a design, however it uses up to 9 times more FF resources than a single FF chain. The main vulnerable area is the general TMR majority voter as in the case of the basic TMR architecture.



**Fig. 4.13** Extended TMR architecture

The embedded BRAM resources were also tested to establish their resilience to radiation-induced SEUs. The BRAM was instantiated with hard-coded constant values and its content was downloaded after the irradiation run via an UART communication. Several firmware versions were designed with different usage of BRAM resources: 18 Kb, 36 Kb and 360 Kb. The SEM core was embedded within all BRAM firmware versions to ensure the integrity of the CRAM.

A special attention was dedicated to test the I/O block reliability against radiation-induced SEUs. Therefore, a custom firmware embedding 4 ring oscillator (RO) architectures was designed within the I/O banks of the DUT. Such structure was designed by using only the I/O buffers primitives set as delay elements in which the signal is shifted through the I/O blocks chain. The output signal of the last I/O block is inverted by using a logic inverter gate and its output is connected to the first delay element. Therefore, the architecture presented in fig. 4.14 meets the requirements to generate a full self-oscillation while using only one LUT to implement the logic inverter as additional logic resource. The VHDL code used to implement the RO structures within the DUT is available in annex A4.



**Fig. 4.14** The single inverter ring oscillator architecture within the DUT I/O blocks -self citation [234]

In order to evaluate and operate the I/Os under various conditions, each RO structure was designed by using a different configuration. Therefore, they were designed within different



type of I/O bank – either high range (HP) or high performance (HP) - and with a different usage of I/O pins. Each buffer within the I/O pins is set to have the following proprieties: “slew rate = slow”, “drive strength = 12 mA”, and “I/O standard = “LVCMOS15 or LVCMOS18”. Hence, depending on the configuration and based on the internal propagation delay paths each RO structure has a fixed oscillation frequency. The particularities of each RO structure are given in table 4.6.

**Tab. 4.6** Resource utilization for each RO structure within the DUT [235]

| Name | DUT I/O Bank | I/O Usage | RO VCC [V] | RO Freq. [MHz] |
|------|--------------|-----------|------------|----------------|
| RO1  | 13 (HR)      | 50        | 1.5        | ~4.1           |
| RO2  | 15 & 16 (HR) | 85        | 1.5 & 1.8  | ~1.6           |
| RO3  | 33 (HP)      | 49        | 1.8        | ~4.1           |
| RO4  | 34 (HP)      | 18        | 1.5        | ~11            |

Fig. 4.15 presents an oscilloscope snapshot with the RO waveforms where from top to the bottom side they are labelled as follows: RO2 (yellow), RO1 (blue), RO3 (purple) and RO4 (green). The RO waveforms and its parameters (amplitude, frequency and duty cycle) were acquired continuously during the whole operation of the DUT, including during the irradiation. Each of the RO parameters are measured are saved in ASCII files to be used for later analysis.



**Fig. 4.15** Oscilloscope screenshot illustrating the waveforms for all 4 RO structures within the DUT-self citation [234]

Three types of failures within the RO structure were defined and are classifying the errors within the I/O blocks: frequency and duty cycle shifts and complete loss of the oscillation. Such failures can be either due to the corruption of the CRAM by a radiation-induced SEU or by a radiation-induced local charge deposition within a I/O block area. Although, the CRAM usage is very low for this type for firmware structure, its corruption can lead to modifications of the user-designed circuitry as well as to modifications of at least one of the I/O attributes within a

RO structure such as: slew rate, I/O direction, I/O standard or drive strength. Once they are triggered, these changes may perturb the oscillation of a RO structure.

A failure complete loss of oscillation is most likely due to the corruption of the CRAM causing the disruption of the RO oscillation, as the design circuitry is changed. Usually, the RO signal will be blocked in a random state either at GND level (0 V) or at a given voltage amplitude established by the I/O bank voltage supply. To have a such failure, at least one of the following scenarios has to be met: either the output buffer from an I/O block within the RO is disabled by its 3-state T pin value (logic “high”), a parasitic connection within the RO is induced, or the operation of the LUT-based inverter is affected.

The frequency shift failures may be caused by changes within the DUT design circuitry or a change in value of at least one of the I/O parameters (drive strength, I/O standard or slew rate). As the DUT circuitry may be affected by radiation, some additional parasitic circuits may be induced and can interfere with to the RO circuit nodes. Such modifications may lead to positive/negative shifts of the RO oscillation frequency.

Failures related to duty cycle shifts may appear only during a half of the RO oscillation period. Such failures may be caused either due to the corruption of the CRAM (most probable) or by a direct hit of a charged particle into a I/O block area leading to a transient effect (e.g. voltage glitch) to be propagated and latched in an Upset within the RO structure. Generally, the RO duty cycle is close to the 50 % value, and assuming a level of variation of  $\pm 2$  %, any values outside this range, while the other RO parameters (amplitude and frequency) remain within their nominal values, are classified as duty cycle shifts.

In table 4.17 are given the DUT firmware versions which were used to test its resources to radiation-induced SEEs. From the table it can be seen that with each mitigation layer added to the logic FFs, the more resources are added within the DUT leading to increase of its essential bit ratio, hence its susceptibility to radiation-induced SEUs. The I/O block RO firmware has a very low usage of essential bits; therefore, the expected error rates may be lower with respect to the other resources.

**Tab. 4.7** DUT firmware architectures and their essential bit numbers (percent of total CRAM) with SEM IP core instantiated in enhanced repair mode

| Firmware Version       | Essential bits   | User Logic Resources                   |
|------------------------|------------------|----------------------------------------|
| Single chain           | 293058 (1.55 %)  | 5500 FFs (6.71 %);                     |
| Single chain + SEM enh | 452823 (2.4 %)   | 5500 FFs (6.71 %);                     |
| Basic TMR              | 1013097 (5.36 %) | 18000 FFs (21.96 %); 1 LUT             |
| FF level TMR           | 1097910 (5.81 %) | 16005 FFs (19.52 %); 5335 LUTs (13 %)  |
| FF level TMR + SEM enh | 1267960 (6.71 %) | 16005 FFs (19.52 %); 5335 LUTs (13 %)  |
| Extended TMR           | 1092465 (5.78%)  | 16200 FFs (19.8 %); 5400 LUTs (13.2 %) |
| Extended TMR+SEM enh   | 1289981 (6.8 %)  | 16200 FFs (19.8 %); 5400 LUTs (13.2 %) |
| BRAM 18 Kb + SEM enh   | 164024 (0.87%)   | 18 Kb BRAM                             |
| BRAM 36 Kb + SEM enh   | 165092 (0.87%)   | 36 Kb BRAM                             |
| BRAM 360 Kb + SEM enh  | 187400 (1 %)     | 360 Kb BRAM                            |
| I/O rings              | 36688 (0.19 %)   | 202 I/Os (71 %)                        |
| I/O rings + SEM enh    | 188458 (1 %)     | 202 I/Os (71 %)                        |

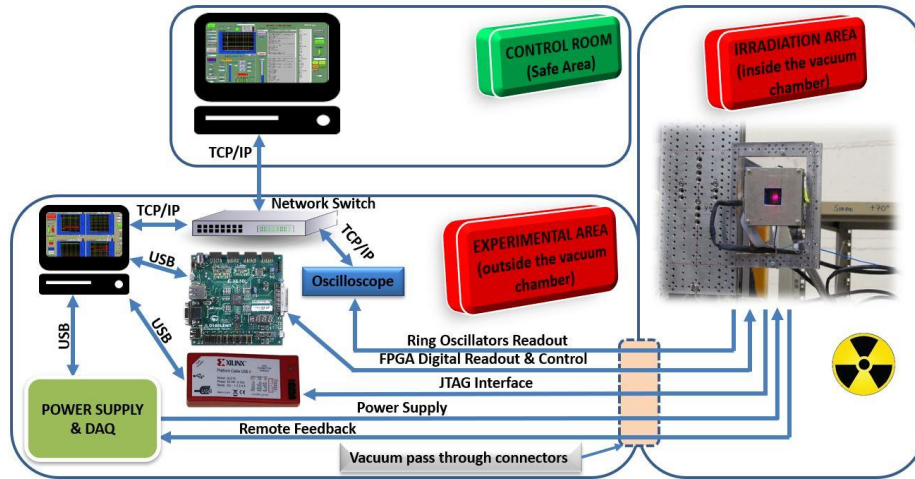


## 4.4 Test Beam Results and Analysis

The Kintex-7 FPGA was tested with various particle beams by using protons, ions, X-Rays and a mixed field of radiation particles. The following facilities were used to establish the DUT reliability in a radiation environment:

- ❖ Ions at SIRAD facility [208] from Legnaro National Laboratories in Italy;
- ❖ Ions at Heavy Ion Facility (HIF) [236] from Université Catholique de Louvain in Belgium;
- ❖ 200 MeV protons at the proton irradiation facility (PIF) [209] from Paul Scherer Institute in Switzerland;
- ❖ 35 MeV protons at the 2.88 GeV Cooler Synchrotron COSY-Jülich [210] from Juelich Research Center in Germany;
- ❖ 50 keV X-rays at the X-ray radiation facility [211] from Padova University in Italy.
- ❖ Mixed field of irradiation at the CHARM facility [42] from CERN.

Based on the architecture presented in fig. 4.2, a general irradiation setup was put together, shown in fig. 4.16. Only the DUT test board was installed in the front of the beam while its connections to the DAQ system and to the readout board were linked through 5 m screened cables. The ion-beam irradiation was carried out in a vacuum chamber to reduce the ion energy loss in the air and the beam window, and protect the beam vacuum. Therefore, the test board connections were linked to outside through vacuum pass connectors. The same setup was easily adapted for the irradiations carried out in air like those with protons or X-Rays.



**Fig. 4.16** The general layout of DUT irradiation setup

Due to the need to establish the DUT response to radiation on the LHCb-RICH application board, or the RICH PDMDB, it was decided within the LHCb-RICH group to have a more complex run at the CHARM facility from CERN. To cope with the CHARM facility

requirements, a more complex irradiation setup was implemented to carry out this irradiation and it will be presented in detail in section 4.4.4.

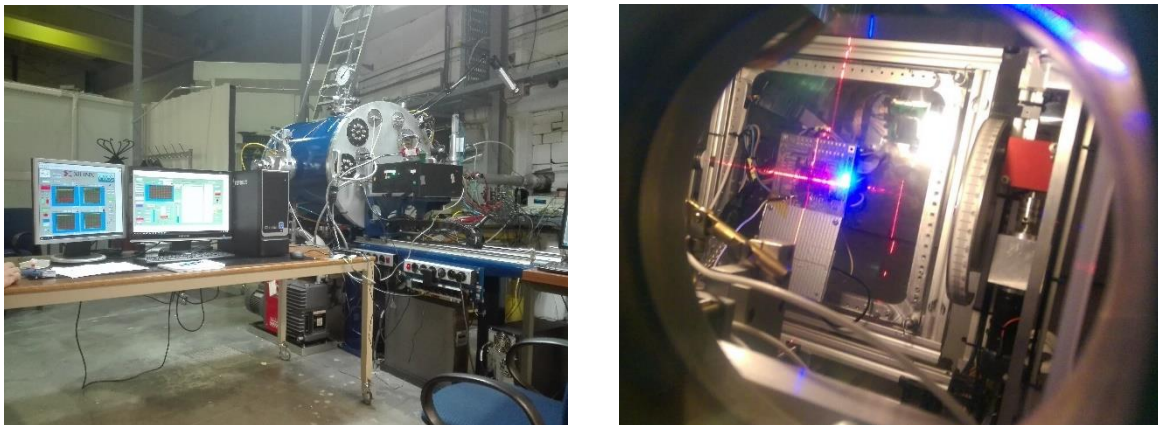
#### 4.4.1 Ion Irradiation

The HIF from UCL provided ion beams within a broad range of LET from  $(1.3 \pm 0.26)$  MeV  $\cdot$  cm<sup>2</sup>/mg to  $(32.4 \pm 6.48)$  MeV  $\cdot$  cm<sup>2</sup>/mg. Several irradiation runs were carried out at different LET values to study the SEEs and to determine the threshold for SELs within the DUT as well as to measure the SEU rates in CRAM and user logic. The most important ion irradiation runs done at HIF are summarized in table 4.8. Due to the fact that the DUTs were thinned to 60  $\mu$ m substrate thickness in order to allow the ions to penetrate to the dice active layers, an additional source of error concerning the LET uncertainty was introduced to have a better view of the effective LET within the DUT.

**Tab. 4.8** Ion beam irradiation runs at the HIF from UCL

| RUN/<br>Sample | Ion              | Energy<br>(MeV) | Flux<br>ions/cm <sup>2</sup> /s | Fluence<br>ions/cm <sup>2</sup> (5 % error) | Effective LET<br>(MeV $\cdot$ cm <sup>2</sup> /mg) |
|----------------|------------------|-----------------|---------------------------------|---------------------------------------------|----------------------------------------------------|
| 1/S1           | <sup>22</sup> Ne | 238             | 10 <sup>4</sup>                 | $(1.4 \pm 0.07) \cdot 10^7$                 | 3.3 $\pm$ 0.66                                     |
| 2/S1           | <sup>22</sup> Ne | 238             | 10 <sup>3</sup>                 | $(1.4 \pm 0.07) \cdot 10^7$                 | 3.3 $\pm$ 0.66                                     |
| 3/S1           | <sup>40</sup> Ar | 379             | 10 <sup>3</sup>                 | $(1 \pm 0.05) \cdot 10^6$                   | 10 $\pm$ 2                                         |
| 4/S1           | <sup>84</sup> Kr | 769             | 10 <sup>3</sup>                 | $(9.1 \pm 0.46) \cdot 10^5$                 | 32.4 $\pm$ 6.48                                    |
| 5/S1           | <sup>58</sup> Ni | 582             | 10 <sup>3</sup>                 | $(1 \pm 0.05) \cdot 10^6$                   | 20.4 $\pm$ 4.08                                    |
| 6/S1           | <sup>40</sup> Ar | 379             | $5 \cdot 10^3$                  | $(1.8 \pm 0.1) \cdot 10^6$                  | 15.6 $\pm$ 3.12                                    |
| 7/S5           | <sup>13</sup> C  | 131             | $5 \cdot 10^3$                  | $(3.2 \pm 0.16) \cdot 10^5$                 | 1.3 $\pm$ 0.26                                     |

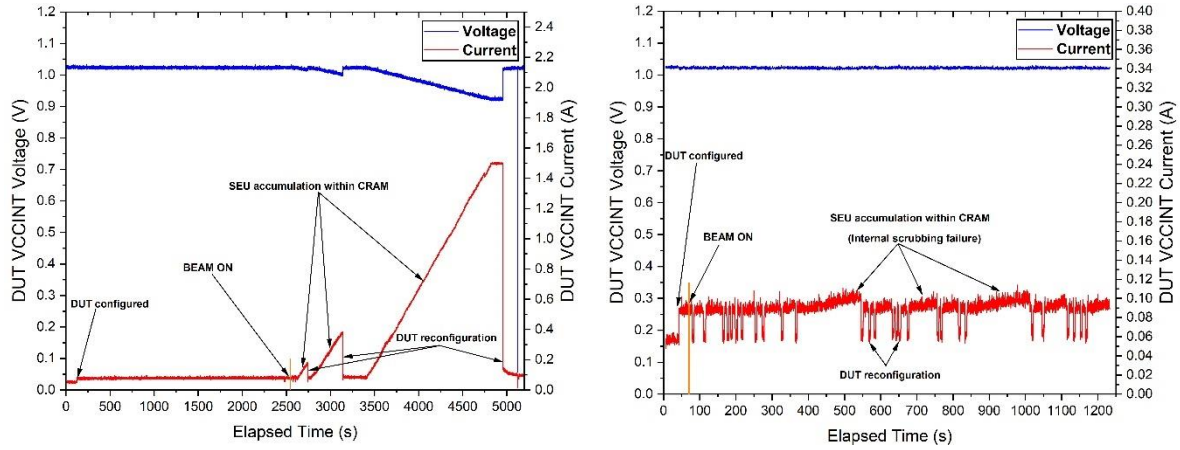
The DUT irradiation setup was installed in the vicinity of the vacuum chamber as it can be seen in the left side of fig. 4.17. Whereas, inside the vacuum chamber the DUT is aligned with respect to the beam line, see the right side of fig 4.17. The vacuum chamber contains any harmful radiation and no special safety measures are required for this ion experiment.



**Fig. 4.17** The HIF vacuum irradiation chamber with the placement of the DUT irradiation setup in its vicinity (left side) and the laser alignment of the DUT inside the vacuum chamber (right side)

A first run with  $^{22}\text{Ne}$  beam at an LET of  $(3.3 \pm 0.66) \text{ MeV} \cdot \text{cm}^2/\text{mg}$  and with a high flux value was applied to the DUT up to a fluence of  $(1.4 \pm 0.07) \cdot 10^7 \text{ ions/cm}^2$ . Inside the DUT was running only the single chain of FFs firmware without the internal scrubber to mitigate the SEUs within the CRAM. As a consequence of the SEU accumulation into the CRAM, additional parasitic circuits were created within the DUT and which contributed to a linear increase of the power consumption on the VCCINT (core) power rail. The evolution of the VCCINT power consumption while the DUT was irradiated is given in the left side of fig. 4.18. However, the SEUs within the CRAM were mitigated by a full reconfiguration of the DUT. Due to the increase of the VCCINT power consumption its internal die temperature was increased up to  $50^\circ\text{C}$ .

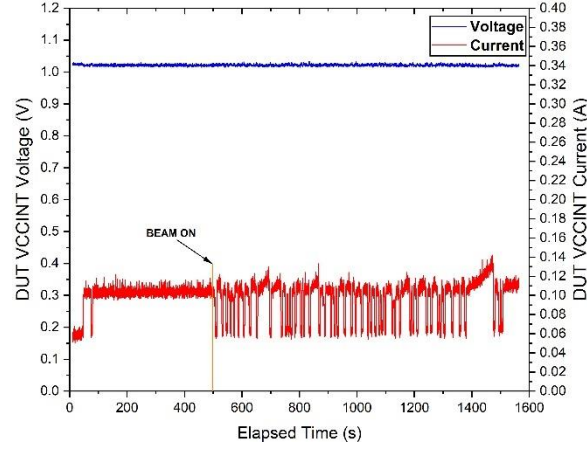
It was clear the fact that the SEU rates were high and without the scrubbing of the CRAM, the DUT cannot operate even at this low LET value. A second  $^{22}\text{Ne}$  run with a 10 times lower flux and with the same target fluence was delivered to the DUT while it was running the basic TMR firmware together with the CRAM internal scrubber.



**Fig. 4.18** The evolution of the VCCINT power consumption while the DUT was irradiated during 1<sup>st</sup> (left side) and the 2<sup>nd</sup> (right side) irradiation runs

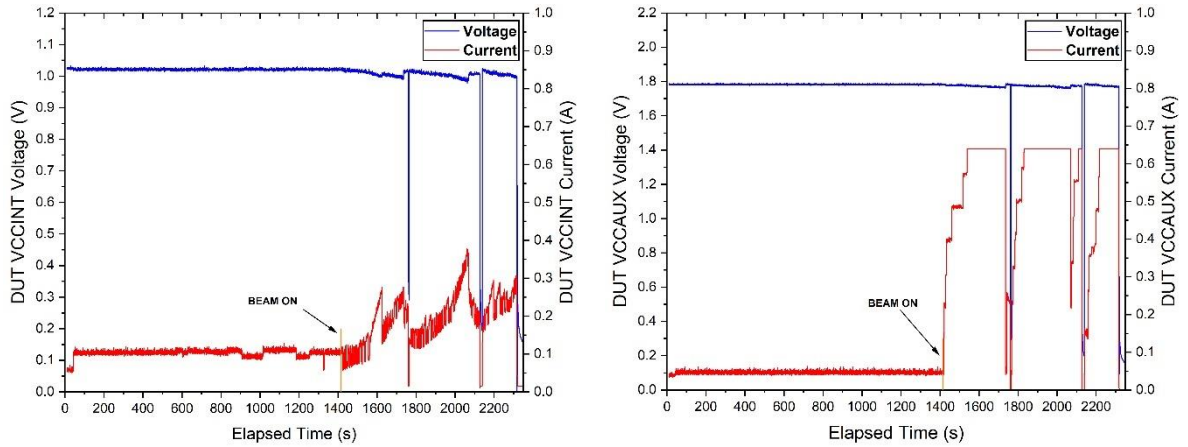
From the right-side graph of fig. 4.18 it can be seen an improvement within the power consumption of the DUT as the internal scrubbing was mitigating most of the ion-induced SEUs within the CRAM. Due to the still-high error rates within the CRAM the error correction time was increased compared with respect to pre-irradiation estimate. This together with SEM-configuration corruption leads to failure of mitigation procedure. Failures of the internal scrubber are highlighted by increasing of the VCCINT power consumption as more unmitigated errors were accumulated. However, again, a full reconfiguration of the DUT mitigated all failures. The SEU error rates within the TMR basic architecture firmware were high as the DUT was reconfigured several times to be able to restart the user logic.

When moving to a higher LET of  $(10 \pm 2) \text{ MeV} \cdot \text{cm}^2/\text{mg}$ , obtained with  $^{40}\text{Ar}$  beam, the error rates within the CRAM and its firmware were even higher as the DUT had to be reconfigured multiple times to restart its operation. The evolution of the VCCINT power consumption during the 3<sup>rd</sup> irradiation run is given in fig. 4.19, and the same failures with the internal scrubber are highlighted by increasings of the VCCINT power consumption. This time the full reconfiguration was used intensively.



**Fig. 4.19** The evolution of the VCCINT power consumption while the DUT was irradiated during the 3<sup>rd</sup> irradiation run

Since no SEL was observed up to an LET of  $(10 \pm 2) \text{ MeV} \cdot \text{cm}^2/\text{mg}$ , a decision was made to move to a very high LET of  $(32.4 \pm 6.48) \text{ MeV} \cdot \text{cm}^2/\text{mg}$ , by using  $^{84}\text{Kr}$  ions. During the 4<sup>th</sup> irradiation run a fluence of  $(9.1 \pm 0.46) \cdot 10^5$  was delivered to the DUT. Large error rates were observed in the CRAM as well as in its firmware, causing the internal scrubbing to fail very fast and leading to an increase of the power consumption within VCCINT power rail with more errors being induced within the CRAM, as it can be seen in the left side of fig. 4.20. Most of the continuous increase in power consumption on the device is due to the rise of the temperature, which in turn is generated by the SEE in another resource of the device, see next paragraph.



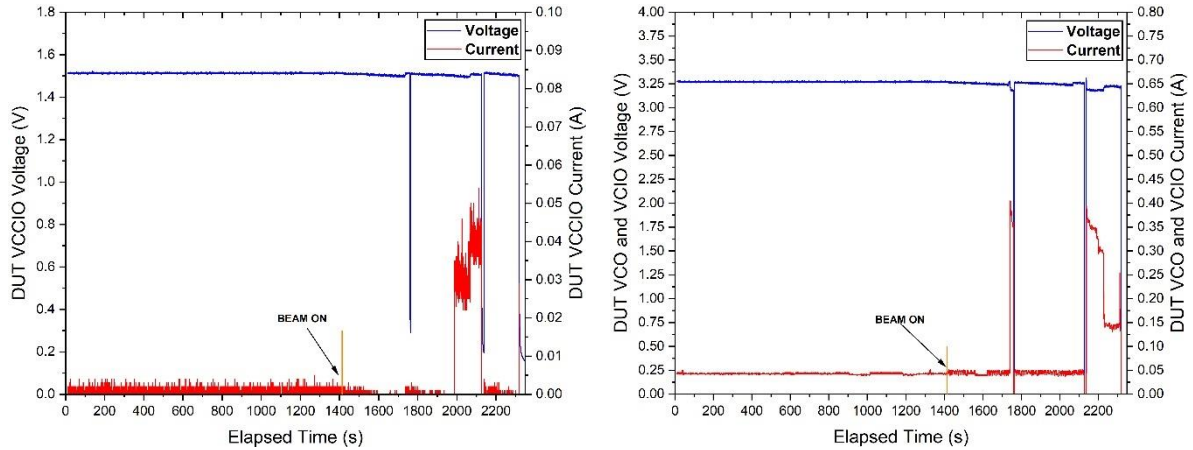
**Fig. 4.20** The evolution of the VCCINT (left side) and VCCAUX (right side) power consumption while the DUT was irradiated during the 4<sup>th</sup> irradiation run

SELs were first observed in the VCCAUX power rails, highlighted as steps of about 100 mA. These events are known in the literature as micro-latchups [237] and it has been established that are due the presence of SEE in the HR I/O banks within the 7-series Xilinx devices, SEE with a threshold LET value smaller than  $40 \text{ MeV} \cdot \text{cm}^2/\text{mg}$  [238]. As it can be seen in the right side of fig. 4.20 the micro-latchup events were only mitigated by a power cycle of the DUT, with full reconfiguration of the CRAM being ineffective without power cycle.



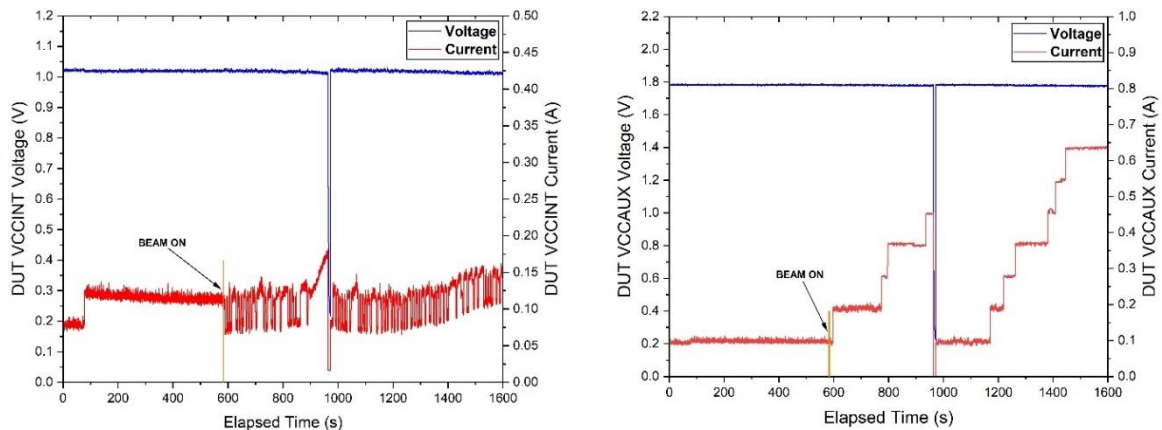
Similar micro-latchup events were observed in other power rails which were used to power other HR I/O banks within the device. The events can be seen in the fig. 4.21 and were corrected as in the case of the VCCAUX ones, by a power cycle of the DUT.

During this run the micro-latchups events caused high power consumption within the DUT, leading to a severe increase of its internal die temperature to a peak value of 79 °C (compared with its baseline value of about 35 °C).



**Fig. 4.21** The evolution of the VCCIO (left side) and VCCO (right side) power consumption while the DUT was irradiated during the 4<sup>th</sup> irradiation run

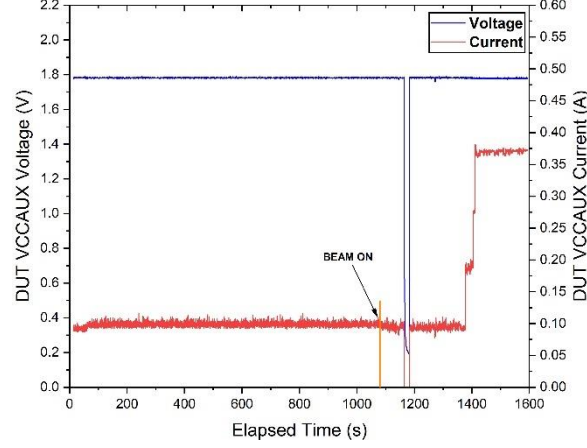
Due to the fact that the SELs were observed at a LET of  $(32.4 \pm 6.48) \text{ MeV} \cdot \text{cm}^2/\text{mg}$ , it was decided to lower the LET value in order to establish the threshold LET value for SEL. Therefore, a 5<sup>th</sup> irradiation run done with  $^{58}\text{Ni}$  beam having a LET value of  $(20.4 \pm 4.08) \text{ MeV} \cdot \text{cm}^2/\text{mg}$  was carried out. During this run, the DUT has received a total fluence up to  $(1 \pm 0.05) \cdot 10^6 \text{ ions/cm}^2$  with an average flux of  $10^3 \text{ ions/cm}^2/\text{s}$ . The same failures of the internal scrubber as well as within the DUT firmware were observed during this run, and are highlighted in the VCCINT power consumption given in the left side plot of fig. 4.22.



**Fig. 4.22** The evolution of the VCCINT (left side) and VCCAUX (right side) power consumption while the DUT was irradiated during the 5<sup>th</sup> irradiation run

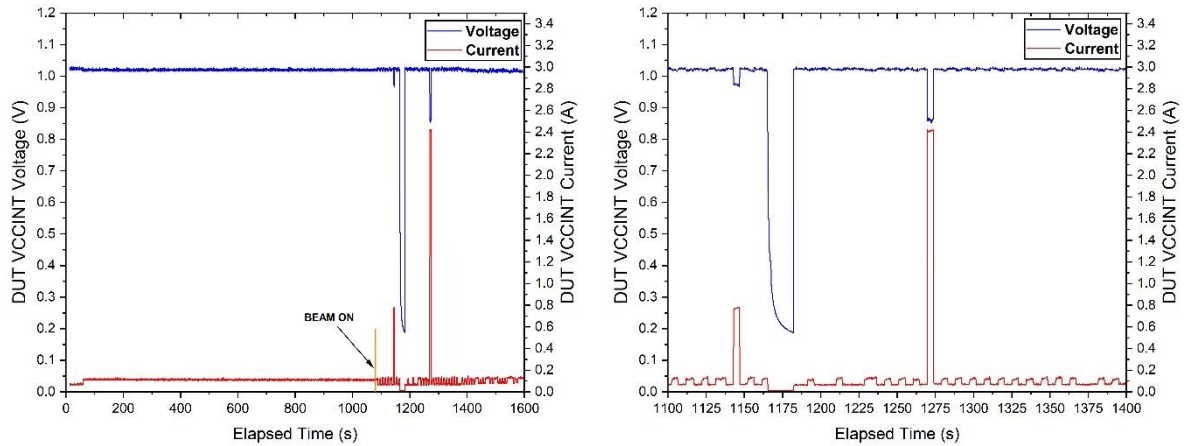
The same micro-latchup events were observed at this LET value, as it can be seen in the right plot of fig. 4.22. Hence, it means that the threshold LET for such micro-latchups is below

this value. Therefore, another irradiation run with a lower LET value of  $(15.6 \pm 3.12) \text{ MeV} \cdot \text{cm}^2/\text{mg}$  obtained with  $^{40}\text{Ar}$  beam and with the DUT tilted at  $50^\circ$  was carried out. The micro-latchup events appeared within the VCCAUX power rail, as it can be seen in the fig. 4.23, suggesting that the threshold LET is around this value, fact which was similar with the literature [237].



**Fig. 4.23** The evolution of the VCCAUX power consumption highlighting the micro-latchups events while the DUT was irradiated during the 6<sup>th</sup> irradiation run

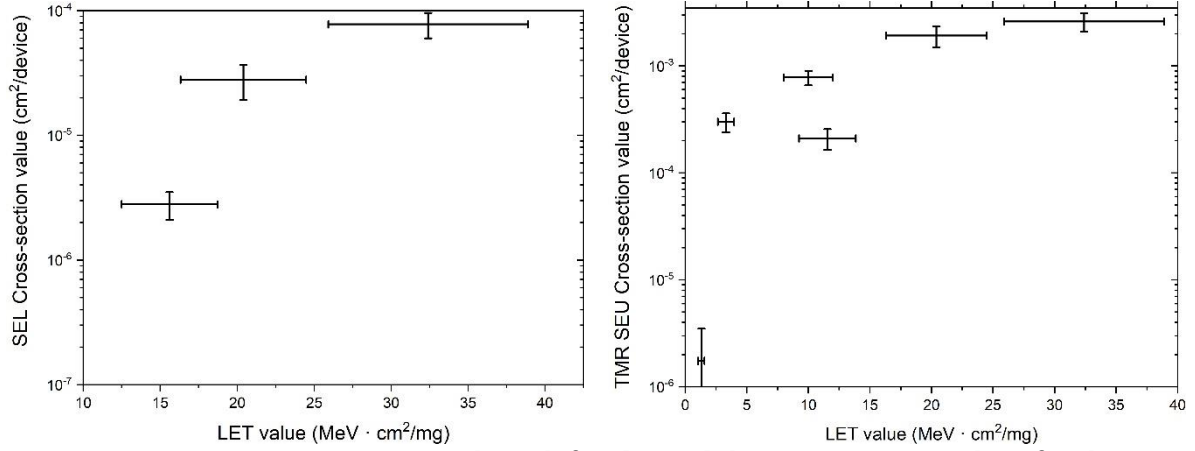
High current states were observed within the VCCINT power rail when the DUT is being reconfigured under beam, causing the current to abruptly increase up to 20 times as it is shown in fig. 4.24. Such events are referred in literature as “Scrub SEFIs” because they are due to writing multiple frames into the wrong memory location when a blind scrubber is used. Hence, they are triggered either by a SEU in the Frame Address Register (FAR) or by a SET on the clock line connected to the boundary scan registers used to feed the configuration SRAM cells [228]. However, these events were mitigated with a second full reconfiguration of the DUT.



**Fig. 4.24** High current states highlighted within the VCCINT power rail and a zoom-in of these events (right side) while the DUT was irradiated during the 6<sup>th</sup> irradiation run

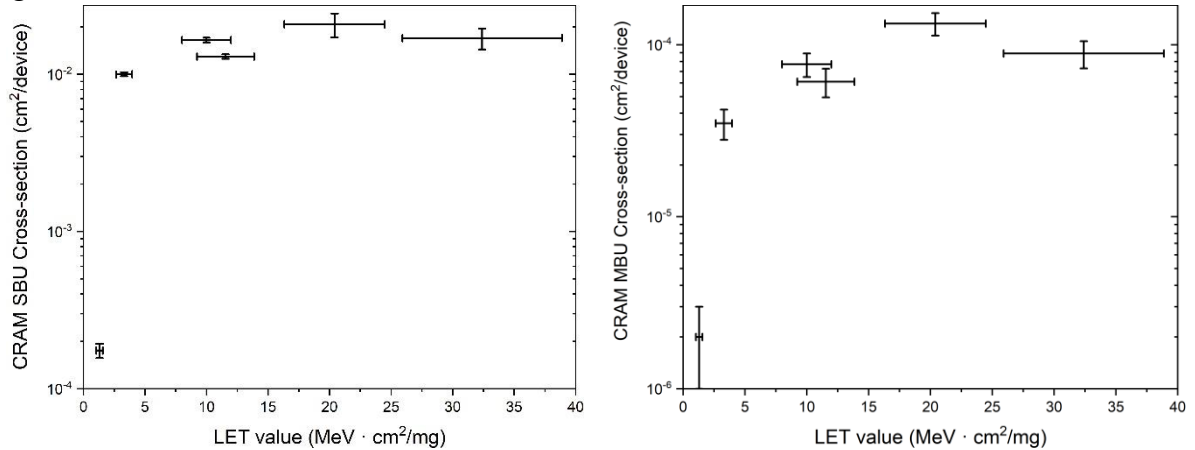
Based on the micro-latchups events observed during the irradiation runs, their cross-section have been calculated to be:  $(2.8 \pm 0.7) \cdot 10^{-6} \text{ cm}^2/\text{device}$  for an LET of  $(15.6 \pm 3.12) \text{ MeV} \cdot \text{cm}^2/\text{mg}$ ,  $(28 \pm 8.8) \cdot 10^{-6} \text{ cm}^2/\text{device}$  for an LET of  $20.4 \text{ MeV} \cdot \text{cm}^2/\text{mg}$  and  $(78 \pm 18) \cdot 10^{-6}$

$6 \text{ cm}^2/\text{device}$  for an LET of  $32.4 \text{ MeV} \cdot \text{cm}^2/\text{mg}$ . These results are plotted on the left graph of fig. 4.25. In the right plot of fig. 4.25, cross-section values are given for the user-logic failures within the basic TMR firmware. As it was expected the error rate within the logic are higher as the LET increases.



**Fig. 4.25** DUT SEL cross-section values (left side) and the cross-section values for the SEU affecting the basic TMR logic user architecture (right side) as a function of LET

The threshold LET for SEUs within the CRAM was measured to be less than a LET of  $(1.3 \pm 0.26) \text{ MeV} \cdot \text{cm}^2/\text{mg}$  [9]. By analyzing the data provided by reading out the internal scrubber status, the DUT cross-section values for single-bit and multi-bit SEUs within the CRAM were calculated. Therefore, the single-bit SEU cross-section values were found to be between  $(1.75 \pm 0.18) \cdot 10^{-4} \text{ cm}^2/\text{device}$  for an LET of  $(1.3 \pm 0.26) \text{ MeV} \cdot \text{cm}^2/\text{mg}$  and  $(170 \pm 26) \cdot 10^{-4} \text{ cm}^2/\text{device}$  for an LET of  $(32.4 \pm 6.48) \text{ MeV} \cdot \text{cm}^2/\text{mg}$ . The multi-bit SEU cross-section values were found to be between  $(0.018 \pm 0.018) \cdot 10^{-4} \text{ cm}^2/\text{device}$  for an LET of  $(1.3 \pm 0.26) \text{ MeV} \cdot \text{cm}^2/\text{mg}$  and  $(26 \pm 5) \cdot 10^{-4} \text{ cm}^2/\text{device}$  for an LET of  $(32.4 \pm 6.48) \text{ MeV} \cdot \text{cm}^2/\text{mg}$ . All single-bit and multi-bit SEU cross-section measurements for a given LET value are given in fig. 4.26.

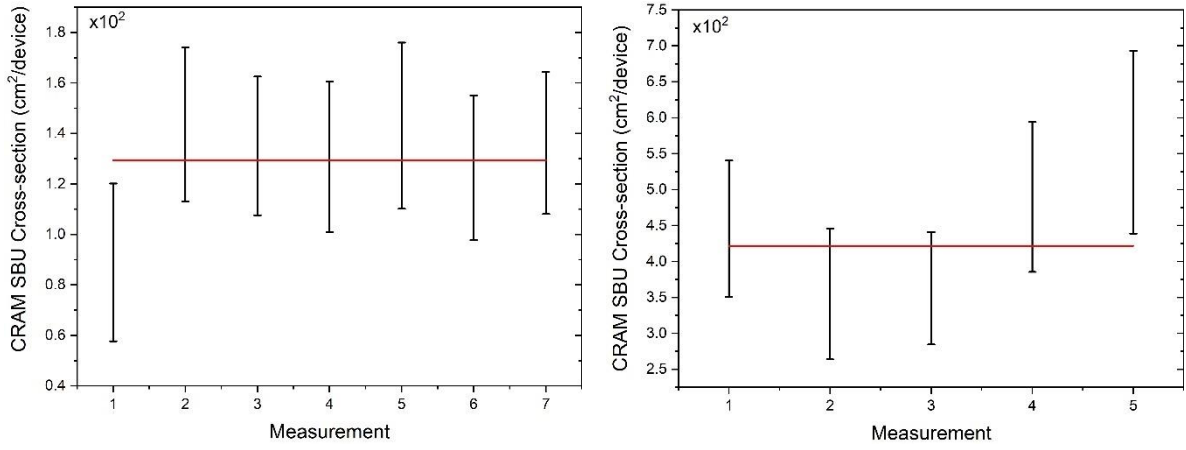


**Fig. 4.26** DUT CRAM single-bit SEU cross-section values (left side) and multi-bit SEU cross-section values (right side) as a function of LET

Additional ion irradiation runs were carried out at the SIRAD facility from Italy, where the DUT was irradiated with two ion species:  $^{16}\text{O}$  for an LET of  $(3.8 \pm 0.38) \text{ MeV} \cdot \text{cm}^2/\text{mg}$  and

$^{28}\text{Si}$  for an LET of  $(13.35 \pm 1.36) \text{ MeV}\cdot\text{cm}^2/\text{mg}$ . Multiple runs were performed on the DUT to test several resources like: CRAM, BRAM, and the I/O blocks.

The CRAM-SEU cross-section was determined by analyzing the status of the internal scrubber while the DUT was irradiated. With the increase of the LET as well as the ion flux, the correction rate of the internal scrubber was highly affected, as already confirmed by the tests done at the HIF from UCL. The average values for SEU cross-section were calculated to be  $(68.5 \pm 5.94) \cdot 10^{-11} \text{ cm}^2/\text{bit}$  for an LET of  $(3.8 \pm 0.38) \text{ MeV}\cdot\text{cm}^2/\text{mg}$  and  $(22.3 \pm 2.26) \cdot 10^{-10} \text{ cm}^2/\text{bit}$  for an LET of  $(13.35 \pm 1.36) \text{ MeV}\cdot\text{cm}^2/\text{mg}$  [239]. These values can be multiplied by the CRAM size of 18884576 bits to get the values per device:  $(1.29 \pm 0.12) \cdot 10^{-2} \text{ cm}^2/\text{device}$  for an LET of  $(3.8 \pm 0.38) \text{ MeV}\cdot\text{cm}^2/\text{mg}$  and  $(4.2 \pm 0.42) \cdot 10^{-2} \text{ cm}^2/\text{device}$  for an LET of  $(13.35 \pm 1.36) \text{ MeV}\cdot\text{cm}^2/\text{mg}$ . Multiple measurements showing the agreement of the CRAM SEU cross-section measurements for each LET value are given in fig. 4.27. Also, the obtained values are close with similar measurements given in literature [237].



**Fig. 4.27** CRAM SEU cross-section measurements for LET values of  $(3.8 \pm 0.38) \text{ MeV}\cdot\text{cm}^2/\text{mg}$  (left side) and  $(13.35 \pm 1.36) \text{ MeV}\cdot\text{cm}^2/\text{mg}$  (right side) –self citation [239]

Two firmware versions, BRAM18 and BRAM36, were used to evaluate the resilience of the BRAM resources against SEUs. The internal scrubber status was monitored to ensure the CRAM integrity as well as the BRAM logic integrity. Therefore, the BRAM SEU cross-section values were found to be  $0.42^{+0.39}_{-0.23} \cdot 10^{-8} \text{ cm}^2/\text{bit}$  for an LET of  $(3.78 \pm 0.38) \text{ MeV}\cdot\text{cm}^2/\text{mg}$  and  $4.8^{+9.8}_{-3.5} \cdot 10^{-8} \text{ cm}^2/\text{bit}$  for an LET of  $(13.35 \pm 1.36) \text{ MeV}\cdot\text{cm}^2/\text{mg}$  [239]. Both measurements are in agreement to some extent to the ones provided by other measurements in the literature [237]. The error is large due to the few BRAM errors recorded before the CRAM configuration fails, as the probability of failure per bit is comparable between BRAM and CRAM.

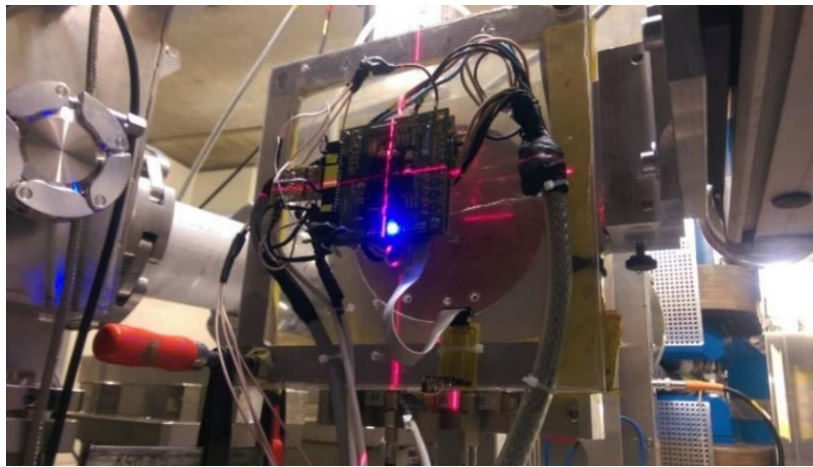
A set of five measurements was carried out to establish the FFs resilience against SEUs using the  $^{16}\text{O}$  beam. The average SEU cross-section value within a basic TMR firmware architecture was found to be  $(38 \pm 5.7) \cdot 10^{-10} \text{ cm}^2/\text{FF}$  for an LET of  $(3.8 \pm 0.38) \text{ MeV}\cdot\text{cm}^2/\text{mg}$  [239]. Usually the measurements of the logic-SEU rates within the user logic is highly dominated by the CRAM integrity, therefore slow correction times as well as failures of the internal scrubber are directly affecting the measurements of SEU rates within the FFs chain logic.



A low number of failures within the I/O blocks RO structures were observed when the DUT was exposed to a low flux of  $^{28}\text{Si}$  beam, 100 ions/cm<sup>2</sup>/s. Even though, the overall usage of the essential bits within the DUT was 1 % with the internal scrubber included, duty cycle shifts and complete loss of oscillation failures were seen. Therefore, for a fluence up to  $(5 \pm 1.25) \cdot 10^5$  ions/cm<sup>2</sup> and a CL of 95% the I/O blocks failure cross-section values were found to be  $0.6_{-0.47}^{+1.15} \cdot 10^{-5}$  cm<sup>2</sup>/device for complete loss of oscillation and  $1.6_{-0.91}^{+1.55} \cdot 10^{-5}$  cm<sup>2</sup>/device duty cycle shifts at an LET of  $(13.35 \pm 1.36)$  MeV·cm<sup>2</sup>/mg [235]. The I/O blocks resilience proved to be good compared with the CRAM for the same LET, however the main reason might be the low flux values as well as the very low usage of the essential bits within the I/O test firmware, which in realistic case might be higher for LHCb-RICH PDMDDB case.

#### 4.4.2 Proton Irradiation

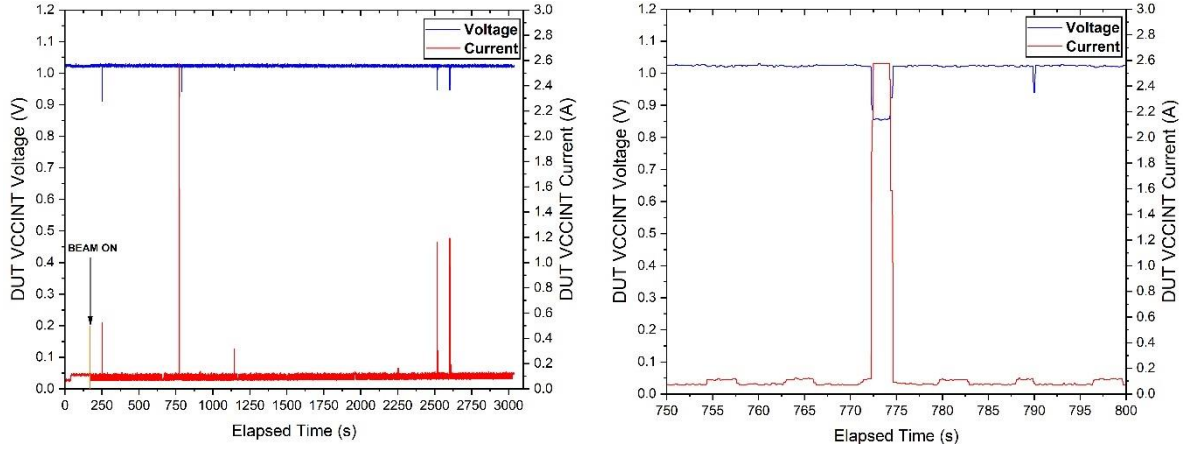
Using the PIF, proton irradiation facility, [209] from Paul Scherrer Institute, three DUT test boards were tested for TID and SEEs with a beam of 200 MeV per proton. Each DUT was irradiated up to  $(500 \pm 75)$  krad (Si) TID with flux values between  $10^7$  protons/cm<sup>2</sup>/s and  $10^9$  protons/cm<sup>2</sup>/s summing up a total fluence of up to  $(8.6 \pm 1.3) \cdot 10^{12}$  protons/cm<sup>2</sup>. The DUTs were irradiated with the beam extracted in the air and in fig 4. 28 is shown the placement of the DUT test boards on the PIF sample holder.



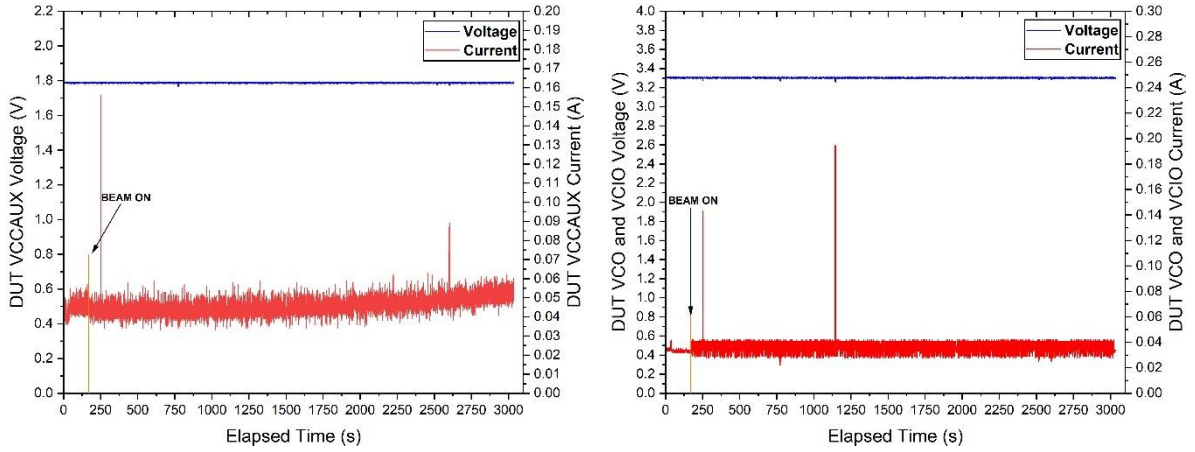
**Fig. 4.28** The placement of the DUT test board on the PIF sample holder and its laser alignment with respect to the beam

Large error rates within the CRAM were observed even at low flux values of about  $10^7$  protons/cm<sup>2</sup>/s, causing the internal scrubber to fail rapidly. As a consequence, the blind scrubber was activated immediately the internal scrubber fails to reconfigure the DUT and to restart operation. However, the large error rates were slowing down the internal scrubber, as its correction time was increasing with the number of errors. Usually the DUT was reconfigured at an average rate of 50 s, this being dependent on the nature of the errors within the internal scrubber logic.

At higher flux values of about  $10^9$  protons/cm<sup>2</sup>/s besides the large error rates within the CRAM, the so called “Scrub SEFIs” were observed as a consequence of the blind scrubbing procedure. Such events are highlighted in the VCCINT power consumption given in fig. 4.29, and they caused the DUT to sink up to 25 times more current than core current baseline value. Similar events were observed also in the VCCAUX and VCO power rails but with a smaller magnitude with respect to their baseline values, see fig. 4.30. However, a full reconfiguration of the DUT mitigated all these effects.

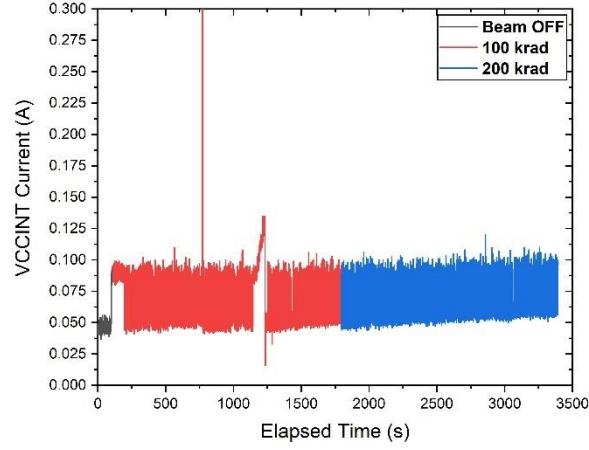


**Fig. 4.29** High current states highlighted within the VCCINT power rail and a zoom-in of these events (right side) while the DUT was irradiated with high flux values of about  $10^9$  protons/cm<sup>2</sup>/s



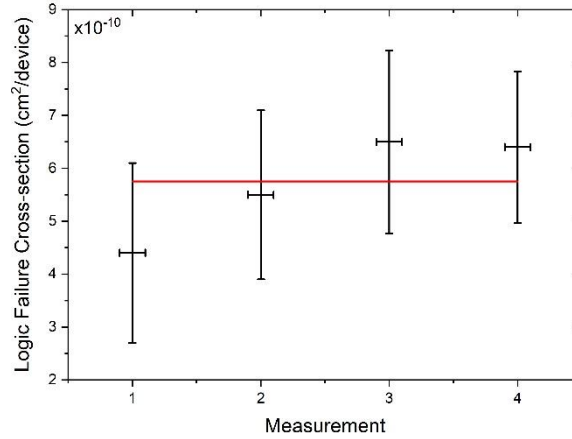
**Fig. 4.30** High current states highlighted within the VCCAUX (left side) and VCO (right side) power rails while the DUT was irradiated with high flux values of about  $10^9$  protons/cm<sup>2</sup>/s

As expected, due to its modern technology node (low gate size at 28 nm technology node, makes the charge accumulation less probable, though relatively large TID effects were seen in X-Rays tests at high dose rates of 160 rad/s), no significant TID effects were seen in any DUT while were irradiated up to (500 +/- 75) krad (Si) even at high flux rates of about  $10^9$  protons/cm<sup>2</sup>/s (about 60 rads/s). In fig. 4.31 is shown the trend of the current within the VCCINT power rail to confirm the low value TID effects on the DUT up to a TID of (200 +/- 30) krad (Si) – 200 krad is the TID expected during the **LHCb RICH upgrade phase Ia**.



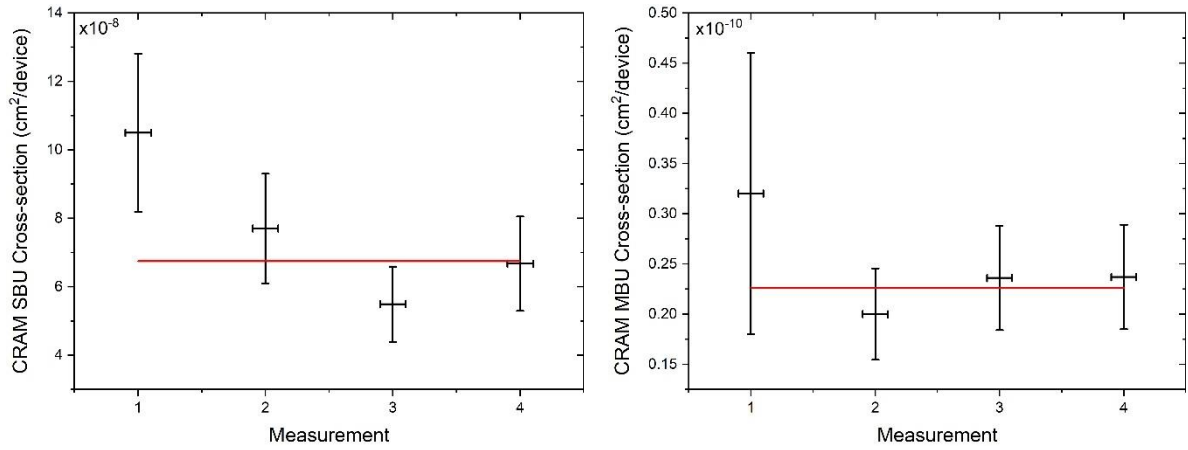
**Fig. 4.31** VCCINT current variation as a function of TID up to a total of  $(200 \pm 30)$  krad (Si), two runs at constant dose rate

However, the main drawback is the large error rates within CRAM which made it very hard to extract the user logic errors rates even on logic architectures with very low usage of essential bits. The average cross-section values for logic failures of the DUT firmware was found to be  $(5.7 \pm 1.6) \cdot 10^{-10} \text{ cm}^2/\text{device}$ , and other measurements are given in fig. 4.32. Therefore, a faster CRAM error-mitigation technique is required in order to keep up with such high errors rates.



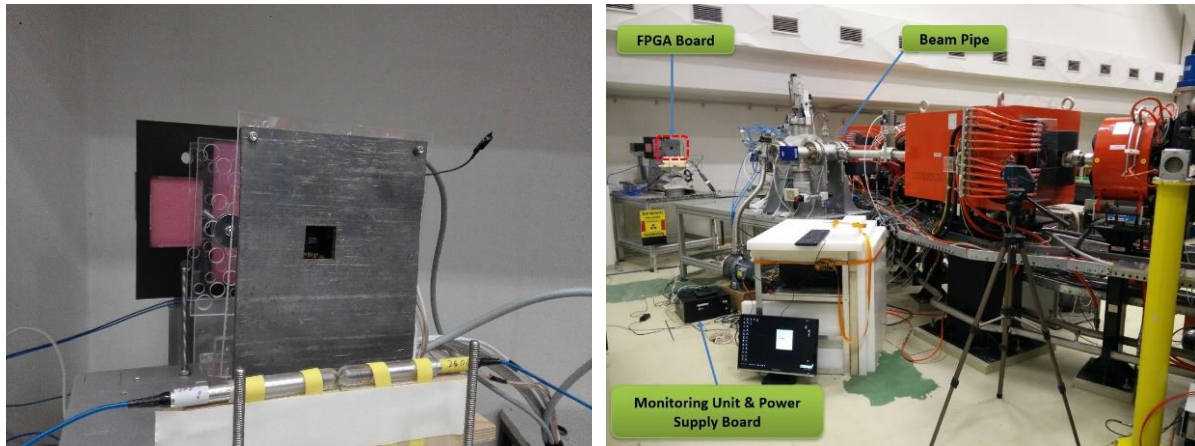
**Fig. 4.32** Logic failure cross-section measurements for 200 MeV proton beam

By analyzing the status report of the internal scrubber, several measurements of the CRAM single-bit and multi-bit cross-section values were carried out. The average values were found to be  $(7.6 \pm 1.6) \cdot 10^{-8} \text{ cm}^2/\text{device}$  for single-bit errors respectively  $(0.25 \pm 0.07) \cdot 10^{-10} \text{ cm}^2/\text{device}$  for multi-bit errors. By dividing the cross-section value to the CRAM size of 18884576, it is obtained a value of  $(4.02 \pm 0.84) \cdot 10^{-15} \text{ cm}^2/\text{bit}$  for single-bit errors. The single-bit cross-section value is close to the value of  $(5.7 \pm 0.58) \cdot 10^{-15} \text{ cm}^2/\text{bit}$  obtained with 180 MeV protons by other independent measurements [240]. More measurements done with 200 MeV protons beam are given in fig. 4.33.



**Fig. 4.33** CRAM single-bit (left side) and multi-bit (right side) error cross-section values measured with 200 MeV proton beam –self citation [241]

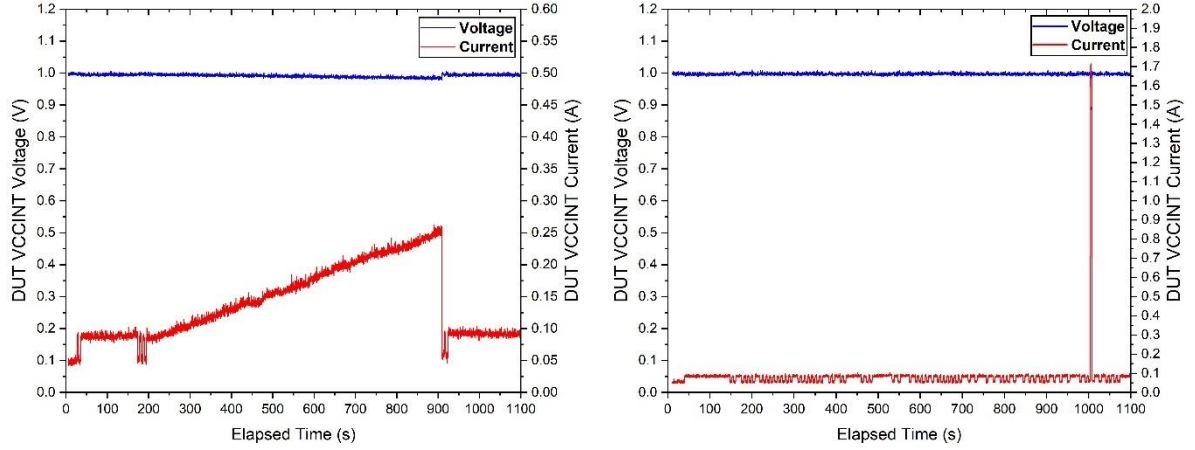
By using the cyclotron pre-accelerator JULIC - 2.88 GeV Cooler Synchrotron COSY- in Jülich [210], three DUTs were irradiated with 35 MeV protons. The energy loss within the full DUT package was calculated to be about  $(1.68 \pm 0.2)$  MeV. Two DUTs were tested with up to  $(250 \pm 18)$  krad (Si) TID, and another sample was tested with up to  $(500 \pm 35)$  krad (Si) TID. The DUT resources (CRAM, BRAM, FFs and I/Os) were tested with dose rate values between  $(30 \pm 2)$  rad/s and  $(67 \pm 4)$  rad/s. The proton beam was extracted in air and the DUT was placed on sample holder in front of the beam line surrounded by the a lead mask to protect the rest of the test board, see the left side of fig. 4.33. The irradiation setup, shown in the right side of fig. 4.33, was installed in the vicinity of the beam line at a few meters away, far from beam impact point. The operation the DUT irradiation setup as well as the monitoring were done from a safe distance and from behind the concrete wall in the control room by an ethernet link connection to the radiation-room PC.



**Fig. 4.34** The DUT test board (left side) and its irradiation setup placed on the experimental area at the COSY-Jülich facility (right side)

As in case of 200 MeV proton tests, no significant TID effects (compared with the temperature effects induced by the SEU-induced changes in device power consumption) were seen within the DUT electrical parameters. The integrity of the CRAM still remains a major

issue with these SRAM-based type. The corruption of the CRAM lead to the creation of parasitic circuits within the DUT which contribute to the gradual increase of the power consumption on the VCCINT power rail, as it can be seen in the left side of fig. 4.35, in absence of error-mitigation procedure. These effects were removed by a full reconfiguration of the DUT. However, in some cases the reconfiguration of the DUT while is irradiated may lead to “Scrub-SEFI” events highlighted as abrupt high current states within the VCCINT power rail. Such events, shown in the right side of fig. 4.35, were corrected by a full reconfiguration of the DUT.



**Fig. 4.35** Events observed within the VCCINT due to the corruption of the CRAM, in two distinct irradiation runs without (left side) and with blind scrubbing (right side)

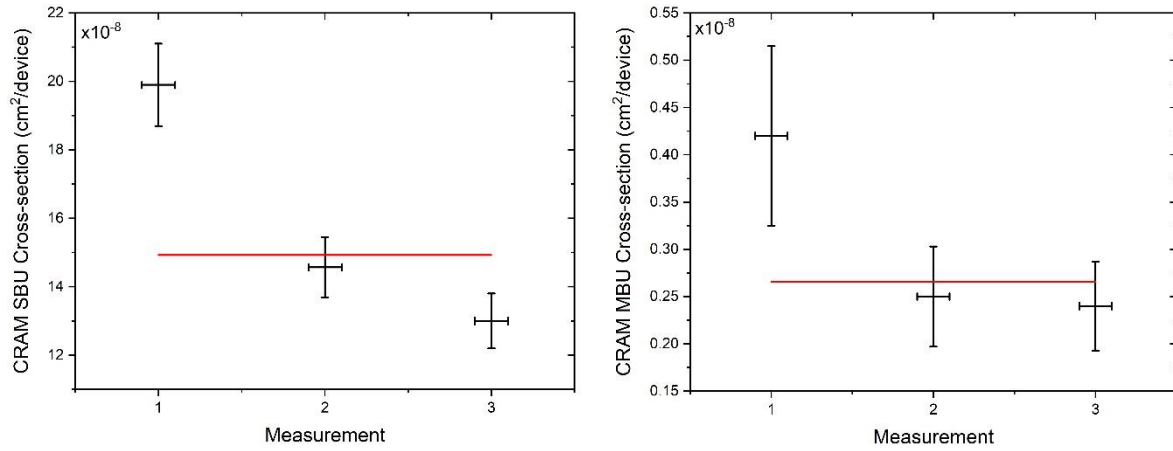
Several measurements were carried out to establish the CRAM single-bit and multi-bit cross-section values, by monitoring the reliability and the status report of internal scrubber. Therefore, the average cross-section values were found to be  $(15.82 \pm 0.96) \cdot 10^{-8} \text{ cm}^2/\text{device}$  for single-bit and  $(0.3 \pm 0.06) \cdot 10^{-8} \text{ cm}^2/\text{device}$  for multi-bit SEUs. By dividing these values by the CRAM size of 18884576, the single-bit cross-section value was obtained to be  $(8.37 \pm 0.5) \cdot 10^{-15} \text{ cm}^2/\text{bit}$ , which is by a factor of about two with other independent measurements done at a similar proton energy [242]. This large difference is probably due to the fast fluctuation in JULIC flux values by 30% or larger, though the TID value is given at 5 -10 % accuracy the beam at nA values is rather instable, but a parametrization of the beam flux is being developed and it should decrease the flux uncertainty, there might be a small bias 20-30 % in the reference data, too, when comparing to other experiments.

The error within the user logic, were measured using the FFs, configured either in single chain or in TMR architectures. For a single chain of FFs the cross-section value was found to be  $(9 \pm 0.07) \cdot 10^{-13} \text{ cm}^2/\text{device}$ ,  $(1.6 \pm 0.01) \cdot 10^{-12} \text{ cm}^2/\text{device}$  for the basic TMR architecture,  $(9.7 \pm 0.07) \cdot 10^{-13} \text{ cm}^2/\text{device}$  for the FF level TMR architecture and

$(8.2 \pm 0.06) \cdot 10^{-13} \text{ cm}^2/\text{device}$  for the extended TMR architecture. As it was expected, TMR architecture improves the overall design resilience against SEUs. However, the use of TMR architecture introduces new drawbacks as more resources are needed to have the same “effective logic”, hence the overall higher essential and critical bits number are increasing the probability of failures. Between the TMR architecture, in some cases the FF level and the

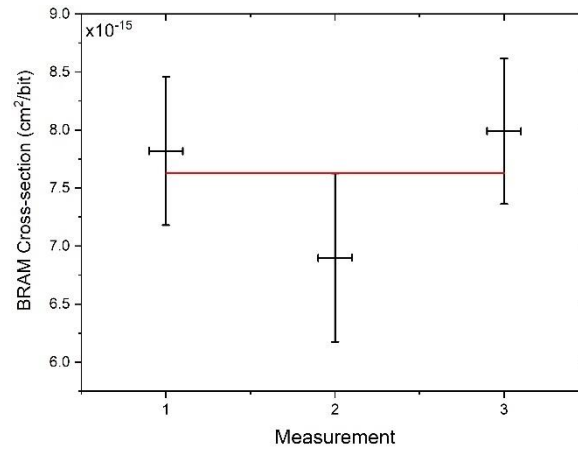


extended TMR architecture may be approached, as they show improvements with respect to a single chain architecture, however these are not so much efficient if the error rate is high.



**Fig. 4.36** CRAM single-bit (left side) and multi-bit (right side) error cross-section values measured with 35 MeV protons beam – self citation [243]

Several measurements of the BRAM resilience were carried out, by using a 360 Kb of BRAM to write before and read after irradiation. Therefore, the average cross-section value was measured to be  $(7.57 \pm 0.4) \cdot 10^{-15} \text{ cm}^2/\text{bit}$  [9]. This value was found to be close with other independent measurements done at similar proton beam energy [242]. More BRAM cross-section measurements are given in fig. 4.37.



**Fig. 4.37** BRAM error cross-section values measured with 35 MeV protons beam

The testing of the I/O blocks resilience was done by using the RO structures without the internal scrubber. In this firmware, the number of essential bits within this I/O RO firmware is 36688 representing 0.19 % from the CRAM. Three DUT samples were tested with a dose rate of  $(30 \pm 2) \text{ rad/s}$  up to a TID of  $(50 \pm 4) \text{ krad (Si)}$  each. The total fluence within a DUT was of about  $(2.3 \pm 0.16) \cdot 10^{11} \text{ protons/cm}^2$ . Failures within the RO structures were observed, and their cross-sections were calculated and given in table 4.9.

**Tab. 4.9** Failures with complete loss of oscillation in all four RO within a sample and their cross-section values calculated with classical CL of 68 % (95 %) [234]

| Sample | Number of failures                                                     | Fluence (protons/cm <sup>2</sup> ) | Cross-section (cm <sup>2</sup> /device)                                                                              |
|--------|------------------------------------------------------------------------|------------------------------------|----------------------------------------------------------------------------------------------------------------------|
| 1      | 3 <sup>+2.9</sup> <sub>-1.6</sub> (3 <sup>+5.8</sup> <sub>-2.4</sub> ) | (2.3 +/- 0.16) · 10 <sup>11</sup>  | 1.25 <sup>+1.2</sup> <sub>-0.7</sub> · 10 <sup>-11</sup> (1.25 <sup>+2.4</sup> <sub>-1</sub> · 10 <sup>-11</sup> )   |
| 2      | 4 <sup>+3.2</sup> <sub>-1.9</sub> (4 <sup>+6.3</sup> <sub>-2.9</sub> ) | (2.3 +/- 0.16) · 10 <sup>11</sup>  | 1.66 <sup>+1.3</sup> <sub>-0.8</sub> · 10 <sup>-11</sup> (1.66 <sup>+2.6</sup> <sub>-1.2</sub> · 10 <sup>-11</sup> ) |
| 3      | 9 <sup>+4.1</sup> <sub>-3</sub> (9 <sup>+8.1</sup> <sub>-4.9</sub> )   | (2.3 +/- 0.16) · 10 <sup>11</sup>  | 3.75 <sup>+1.7</sup> <sub>-1.2</sub> · 10 <sup>-11</sup> (3.75 <sup>+3.4</sup> <sub>-2</sub> · 10 <sup>-11</sup> )   |
| Total  | 16 <sup>+5.1</sup> <sub>-4</sub> (16 <sup>+10</sup> <sub>-6.9</sub> )  | (6.9 +/- 0.5) · 10 <sup>11</sup>   | 2.22 <sup>+0.7</sup> <sub>-0.5</sub> · 10 <sup>-11</sup> (2.22 <sup>+1.4</sup> <sub>-1</sub> · 10 <sup>-11</sup> )   |

Assuming the fact that all RO failures given in the table 4.9 are due to the corruption of the CRAM, the number of critical bits can be calculated by using the following equation:

$$N_{\text{crit}} = (\sigma_A \cdot N_{\text{CRAM}}) / \sigma_{\text{CRAM}} \quad (4.1)$$

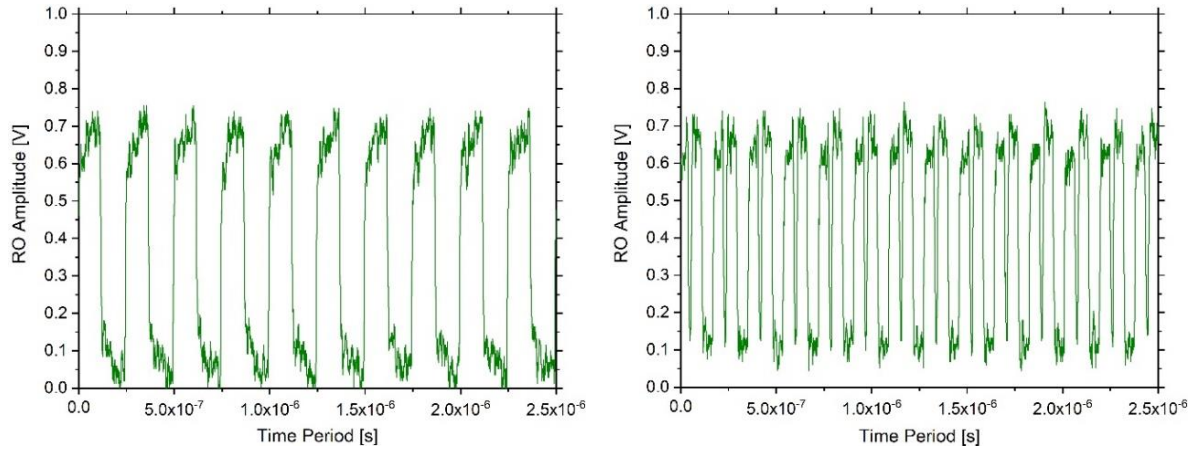
where  $N_{\text{CRAM}}$  is the number of bits within the CRAM,  $\sigma_A$  the RO failure cross-section, and  $\sigma_{\text{CRAM}}$  is the average SEU CRAM cross-section value. Therefore, by using the  $(15.82 \pm 0.96) \cdot 10^{-8} \text{ cm}^2/\text{device}$  for  $\sigma_{\text{CRAM}}$  the number of critical bits within the RO architecture was found to be about 2644 bits representing 0.014 % from the CRAM size and 7.2 % from the essential bits number.

No duty cycle shifts were observed in any of the tested DUTs within an acceptance level of  $50 \pm 2 \%$ . However, an upper limit of cross-section value for duty cycle failures within all DUTs and with a 95 % CL was calculated to be  $1.53 \cdot 10^{11} \text{ cm}^2/\text{DUT}$  for a fluence of  $(6.9 \pm 0.5) \cdot 10^{11} \text{ protons/cm}^2$  [234].

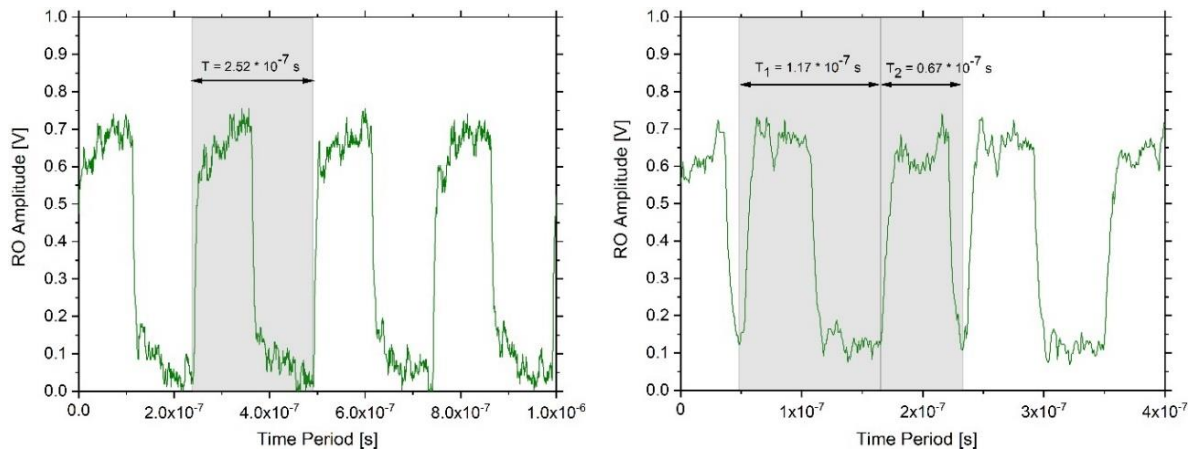
Radiation-induced frequency failures within the RO structures were observed as positive/negative frequency shifts larger than 10 %. Therefore,  $7^{+7.5}_{-4.2}$  (95% CL) events were observed within all three DUTs for a total fluence of  $(6.9 \pm 0.5) \cdot 10^{11} \text{ protons/cm}^2$ . The cross-section value was calculated to be  $0.97^{+1}_{-0.6} \cdot 10^{-11} \text{ cm}^2/\text{DUT}$  for 95% CL. In the left side of fig. 4.38 is given the baseline waveform of the RO3 structure within the DUT having a nominal frequency of about 4.1 MHz. Due to the fact that the RO output waveforms were monitored as simple as possible and via long cables with an oscilloscope, their edges are noisy, but the waveform measurement is good enough to be analyzed. However, in the right side of fig. 4.38 it can be seen an RO radiation-induced frequency failure.

A zoom-in on the time axis for both waveforms, see fig. 4.39, highlights the fact that the radiation-free RO waveform has a typical time period of  $2.52 \cdot 10^{-7} \text{ s}$  which in fact corresponds to its typical oscillation frequency of about 4.1 MHz. However, assuming that the waveform from the right side of fig. 4.39 is composed by 2 signals, we have: a signal with a period  $T_1 = 1.17 \cdot 10^{-7} \text{ s}$  and a frequency of about 0.85 MHz and another signal with a period  $T_2 = 0.67 \cdot 10^{-7} \text{ s}$  and a frequency of about 1.49 MHz. These values highlight a negative RO frequency shift, showing the fact that the RO circuitry was affected, and is no longer operating with its nominal parameters. However, such failures are mitigated by a full reconfiguration of the DUT.





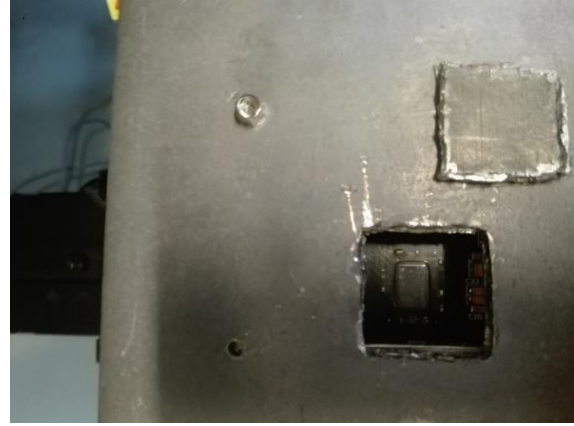
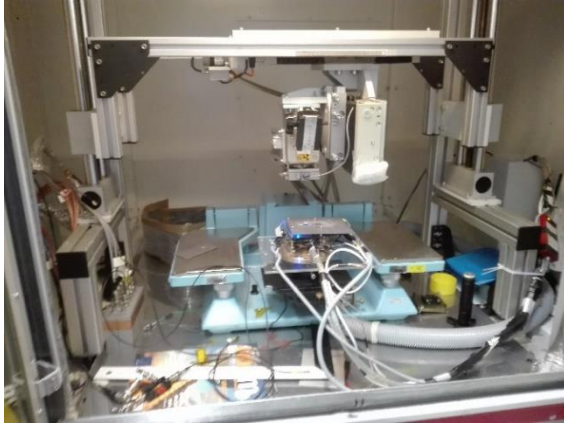
**Fig. 4.38** RO3 waveform information, before (left side) and while the DUT is exposed to the 35 MeV protons (right side)



**Fig. 4.39** Zoom in on the RO3 waveform information, before (left side) and while the DUT is exposed to the 35 MeV protons (right side)

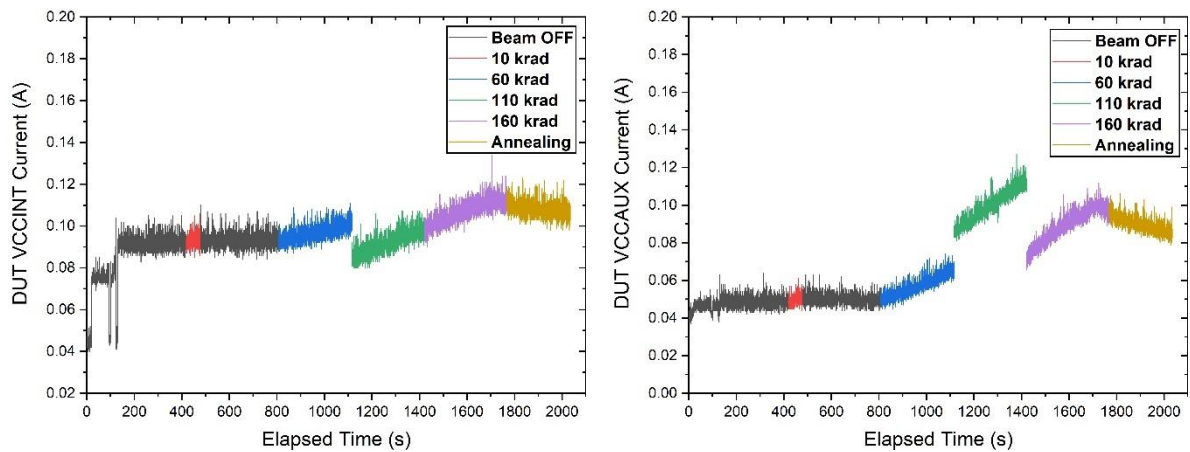
### 4.4.3 X-Ray Irradiation

To confirm the very small TID effects observed with protons tests, two DUTs were irradiated with 50 keV X-rays beam provided by the X-ray facility from University of Padova [211]. The DUTs were mounted inside the X-ray irradiation chamber as it can be seen in fig. 4.40. Each DUT was irradiated with an average dose rate of  $(166 \pm 33)$  rad/s in three runs of  $(50 \pm 10)$  krad (Si) each, summing up a TID of  $(160 \pm 32)$  krad (Si). As expected no CRAM corruption or logic failures were seen, as usually the X-ray photons do not have enough energy to deposit and to trigger SEEs. However, they can induce TID effects, therefore the X-rays beam test is used to confirm, and in some cases, to differentiate the TID effects from SEEs or DD which may be induced by protons beams.



**Fig. 4.40** The placement of the DUT test board inside the X-ray irradiation chamber

Fig. 4.41 shows the overall TID effects within the DUTs power rails: VCCINT and VCCAUX. The discontinuity of the plots is due to different firmware versions used for testing which had a direct effect to the nominal power consumption. It can be seen that the overall variation of the power consumption as a consequences of the TID is about 10 % for the VCCINT power rail, and of about 50 % for the VCCAUX power rail. However, the room-temperature annealing process is visible already even only after a few minutes.



**Fig. 4.41** X-ray TID effects within the DUT VCCINT (left side) and VCCAUX (right side) power rails with multiple irradiation runs

The large dose rates of these runs make the TID effects more visible as the room-temperature annealing is not balancing-out the induced parasitic charges in device insulator layers like is at least partially happening for proton-beam runs. A more compressive study of TID effects in these chips is in progress.

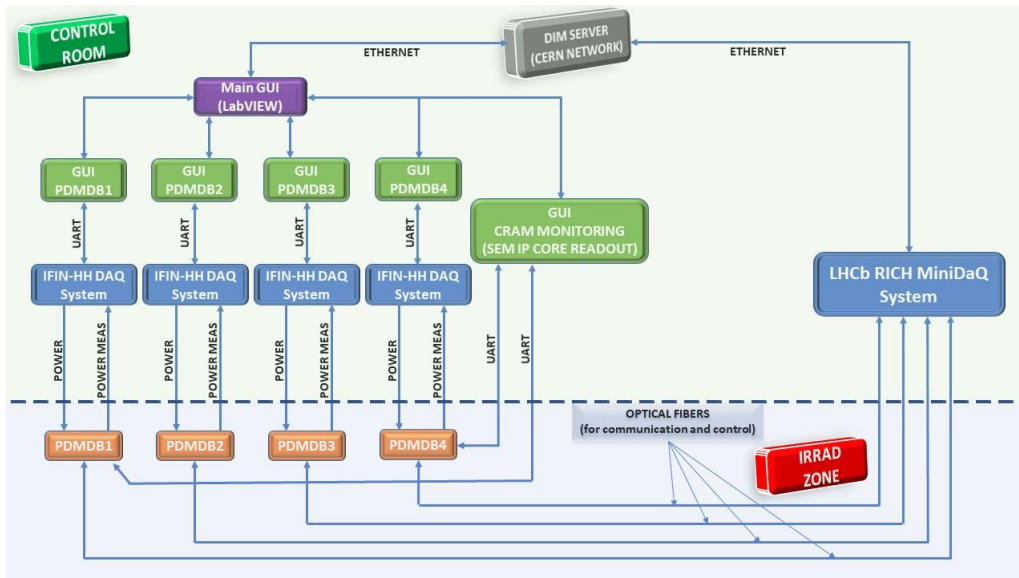
#### 4.4.4 Mixed Field Irradiation

To have a very close idea on how the radiation environment will be on the LHCb detector, it was decided within the LHCb collaboration to use CHARM facility [42] from CERN to test the reliability of the PDMDB design together with the KINTEX-7 FPGAs. The CHARM

facility is a dedicated radiation test facility used mainly to test and qualify electronic components and systems for LHC/CERN/HEP applications and for space experiments. Its radiation mixed field of HEH and neutrons is generated by striking a metallic target, either aluminum or copper, with a 24 GeV/c proton beam extracted from the CERN Proton Synchrotron (PS) accelerator. There are 13 test positions available for users to test their electronic systems. Additionally, movable iron or concrete blocks can be used to create a shield between the target and the electronics placed in different test areas. This allows the user to modulate the resulted mixed-field spectra to a required radiation field.

Our collaboration got the chance to be a secondary user of an LHC-test slot at the CHARM facility. Therefore, a configuration with a copper target without shielding and with the PDMDBs rack placed on the position 10 was available for use. The position is chosen as it has radiation environment close to LHC tunnel environment, hence, a bit below our requirements, though the test was proven in the end relevant from both quantitative and qualitative point of view.

A very complex and dedicated irradiation setup was put together in close collaboration with the LHCb-RICH group to test four PDMDBs. The PDMDB were in the final design stage, however, they had only one FPGA from a total of 3 possible per PDMDB. The KINTEX-7 FPGAs are the only active components which are commercial, while all the active components are radiation-hard by design as it was described in section 1.5.3. The system shown in fig. 4.42 is composed from two main sub-systems: the DAQ systems and LHCb-RICH miniDAQ system. LHCb-RICH miniDAQ system is an infrastructure adopted to validate the development of the front-end electronics within the LHCb experiment [244]. It is used to monitor the data and to configure the entire electronics chain via optical fibers.



**Fig. 4.42** The PDMDB irradiation setup used for testing at the CHARM facility

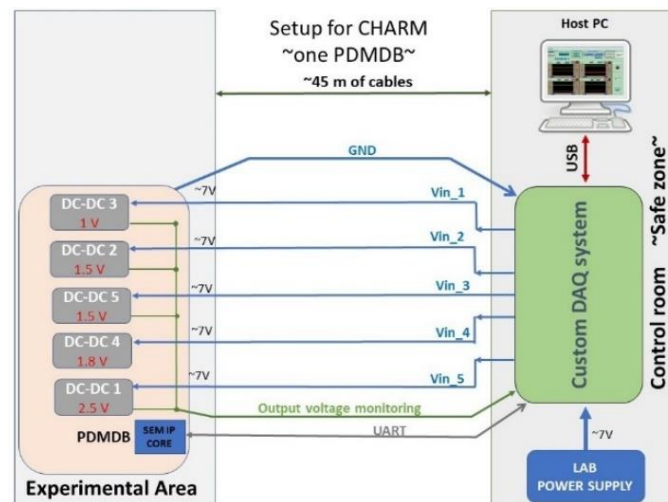
Four DAQ systems were designed to power and monitor the power consumption of the PMDB as well as the CRAM integrity by reading out the internal scrubber within the PDMDB firmware. Due to radiation safety and constraints, besides the PDMDBs, there were no additional electronic system placed in the experimental area. Therefore, the DAQ systems and

the LHCb-RICH miniDAQ systems were placed in the control room. About 45 - 50 m length on each power/monitoring cable or fiber were needed to fulfil the connection requirements between the patch panels from the experimental area and the tested devices (PDMDBs) plus, additionally, from experimental area to the panels from the control room.

The simplified architecture of one DAQ is given in fig. 4.43 showing the power and monitoring connections to one PDMDB. The PDMDB architecture described in section 1.5.3 has 5 DC-DC radiation-hard converters to convert the input voltage of about 7 V to several voltages: 1 V, 1.5 V, 1.8 V and 2.5 V.

Due to the PDMDB design, it was not possible to design a radiation hard current monitoring circuitry to monitor the power consumption on all the DC-DC converters outputs. Hence, a different approach was proposed to estimate the output current of each DC-DC converter. By measuring the input power and the output voltage and knowing the approximate efficiency ( $\eta$ ) from its datasheet, it was possible to compute the approximate output current values by using the power conversion efficiency equation:

$$I_{out} = (V_{in} \cdot I_{in} \cdot \eta) / V_{out} \quad (4.2)$$



**Fig. 4.43** The simplified DAQ architecture for one PDMDB proposed for testing at the CHARM facility

Within the DAQ system, the main voltage of about 7 V provided by a bench power supply is divided in 5 lanes, one for each PDMDB DC-DC converter. Each power lane is individually controlled and monitored to get the input power values needed to compute efficiency equation. Each output voltage corresponding to the PDMDB DC-DC converters is monitored by the DAQ. In this way, a rough estimate of the FPGA power consumption was obtained. Additional circuitry was added on the DAQ board to provide the UART interface to the SEM IP core, used as internal CRAM scrubber. Due to the long length of the cables the maximum workable baud rate within 45 m of cables was 4800 bauds.

A complex LabVIEW GUI readout system composed from one master GUI and 5 slave GUIs was designed to readout and control the operation of the PDMDBs as well as to communicate to the LHCb-RICH miniDAQ system. Four independent slave GUIs were used to control each DAQ system connected to one PDMDB, in order to monitor its power



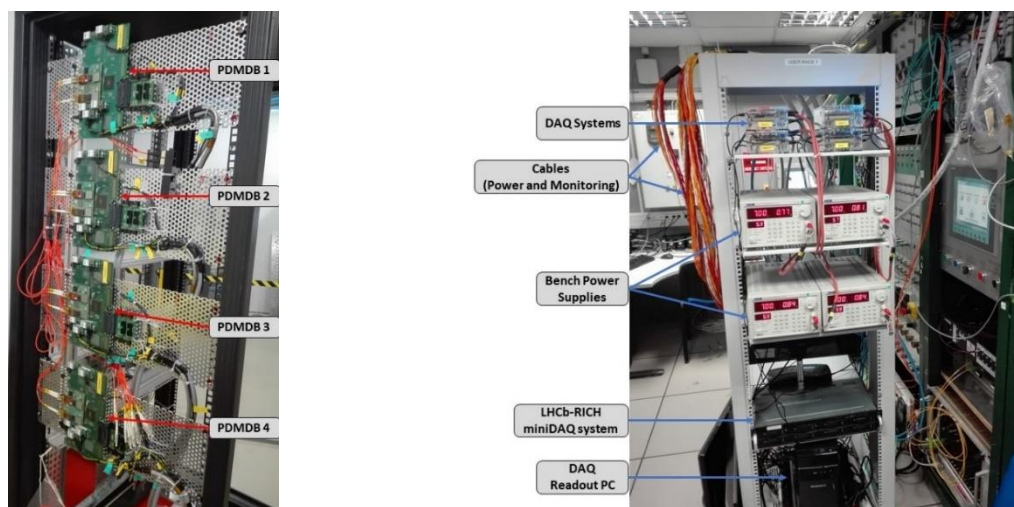
consumption, see the left side of fig. 4.44. One slave GUI, shown in the right side of fig. 4.44, was used to read out the status of the internal scrubber from the PDMDBs. Within each slave GUI the data is saved in ASCII files for later analyses. The master GUI was used to synchronize the data from all slave GUIs and to communicate with the LHCb-RICH miniDAQ GUI via CERN distributed information management system (DIM) [245].

From the LHCb-RICH miniDAQ GUI, each FPGA from the PDMDB was configured and firmware status was read out via optical fibers. By reading out the firmware-stored data, corresponding to each FPGA within a PDMDB, the logic error rates are counted by comparing the FPGA-output stream to the baseline stream.

All four PDMDBs were mounted on a test rack, shown in the right side of fig. 4.45, to be placed by a robot in the position 10 of CHARM experimental area. A dedicated rack was reserved in the control room to host the bench power supplies together with the DAQ and the LHCb-RICH miniDAQ systems, as shown in the right side of fig. 4.45.



**Fig. 4.44** LabVIEW GUIs: to control the DAQ for one PDMDB (left side) and to readout the internal scrubber status (right side)



**Fig. 4.45** The racks containing the four PDMDBs to be placed in the CHARM irradiation area (left side) and the DAQ systems located in the control room (right side)

As the PDMDB did not have any input trigger signals from the front-end boards, a hard-coded emulating pattern was used in the buffer described previously. Therefore, the information pattern was shifted out through the FPGA logic and it was read out by the LHCb-RICH miniDAQ. Then the obtained value is compared against its hard-coded value to count differences and increment an error counter.

Two PDMDBs, PDMDB 1 and PDMDB 4, had the FPGA firmware with the internal scrubber to monitor the CRAM integrity as well as to correct the single-bit errors. This was required to measure the SEU cross-section within the CRAM, as well as to see error-mitigation impact on the user-logic circuitry. The other two PDMDBs from the middle were running with only their basic firmware, without internal scrubbing. From table 4.10 it can be seen that the approximate usage of essential bits within the LHCb-RICH FPGA firmware is close to 1 %, and increases to 1.8 % when the internal scrubber is used. Each PDMDB had independent FPGA reconfiguration via the JTAG interface provided by the radiation hard GBT-SCA circuit embedded on the TCM adapter boards of the PDMDB. The FPGA reconfiguration was set to be triggered by the following scenarios: logic failures, high current consumption and failures of the internal scrubber.

**Tab. 4.10** Essential bits usage of the LHCb-RICH FPGA firmware used during CHARM tests

| Firmware        | Essential bits used (bits) | CRAM size (bits) |
|-----------------|----------------------------|------------------|
| LHCb_RICH       | 191861 (1 %)               | 18884576         |
| LHCb_RICH + SEM | 346335 (1.8 %)             | 18884576         |

The PDMDB rack was exposed in two runs of one week each having a TID of 34.27 krad (Si) and up to a fluence of  $0.65 \cdot 10^{12}$  HEH/cm<sup>2</sup>, out of which close to 70 % are high energy neutrons. In table 4.11 are given the detailed numbers of the radiation exposure during the CHARM irradiation runs.

**Tab. 4.11** Summary of the PDMDB rack radiation exposure during the CHARM tests

|                                       | RUN I                | RUN II               |
|---------------------------------------|----------------------|----------------------|
| PDMDB rack inside                     | 14:40 02-August 2017 | 17:08 09-August 2017 |
| PDMDB rack removed                    | 15:42 07-August 2017 | 09:21 15-August 2017 |
| TID (krad)                            | 14.37                | 19.9                 |
| 1 MeV eq. fluence (cm <sup>-2</sup> ) | $1.4 \cdot 10^{12}$  | $1.94 \cdot 10^{12}$ |
| HEH fluence (cm <sup>-2</sup> )       | $4.47 \cdot 10^{11}$ | $6.18 \cdot 10^{11}$ |
| Total protons on target               | $1.2 \cdot 10^{16}$  | $1.66 \cdot 10^{16}$ |

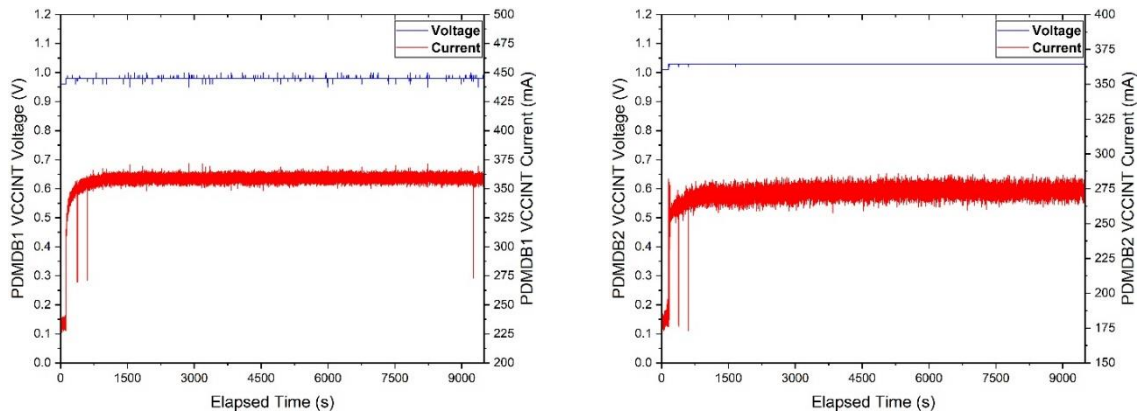
With the beginning of the irradiation runs, SEUs within the CRAM started to be visible either in the user logic or in the status report of the internal scrubber. However, no SEL events or high current states within the FPGA nor in the whole PDMDB were observed. The only observed current increase was due to the corruption of the CRAM combined with the failures of the internal scrubber logic (accumulated SEUs generate a time-linear power increase as was for proton and ion test). As the SEUs were accumulating within the CRAM, parasitic circuitry

is created which increases the dynamic power consumption within the VCCINT power rail. However, they were corrected by a reconfiguration the DUT.

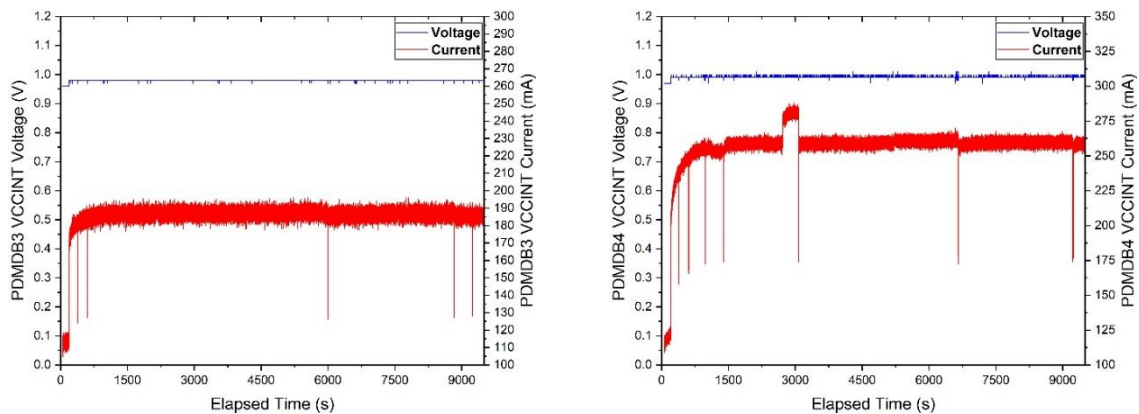
A sample showing the evolution of the VCCINT power consumption for each PDMDB within a 3 hours period is given in fig. 4.46 respectively in fig. 4.47. The current drops (with red) from each plot represents the reconfiguration of the DUT due to either logic failures and/or to excessive CRAM corruption, with the latter when the accumulated SEUs make the core current significantly different with respect to its base-value.

In the left side of fig. 4.47 it can be observed a small increase of the VCCINT power consumption due to accumulation of the SEUs within the CRAM. Since the PDMDB 3 did not have the internal scrubber, the errors kept accumulating. However, they were corrected by a reconfiguration of the FPGA.

In the right side of fig. 4.47 it can be observed failures of the internal scrubber, which led to accumulating more errors within the CRAM and finally to the increase of the power consumption. As in the case of the other PDMDBs, the increase of the power consumption was corrected by reconfiguring the FPGA.



**Fig. 4.46** A 3 hours sample of the DUT power consumption on the VCCINT power rail within the PDMDB 1 – with internal scrubbing – (left side) and PDMDB 2 – no internal scrubbing – (right side) while irradiated at CHARM

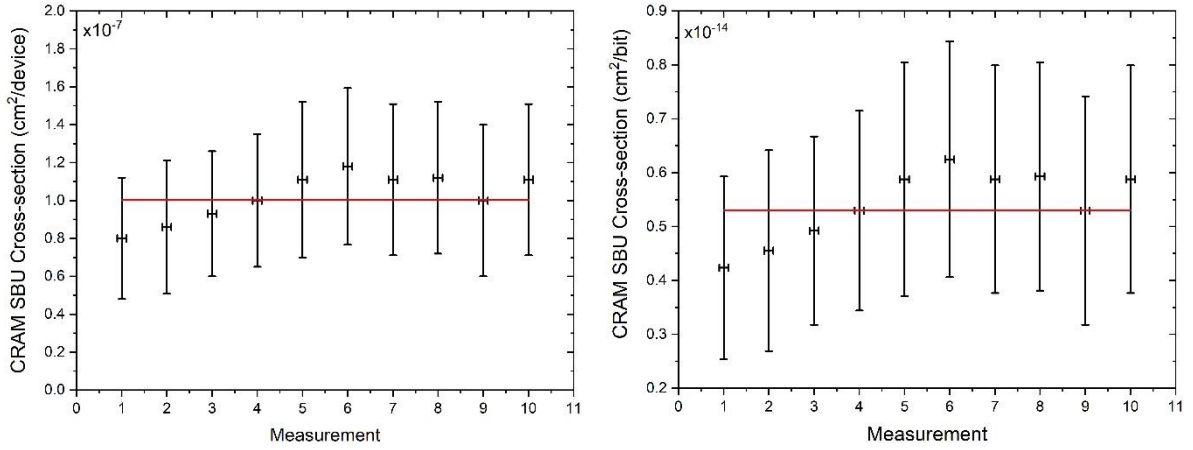


**Fig. 4.47** A three hours sample of the DUT power consumption on the VCCINT power rail within the PDMDB 3 – no internal scrubbing – (left side) and PDMDB 4 – with internal scrubbing – (right side) while irradiated at CHARM

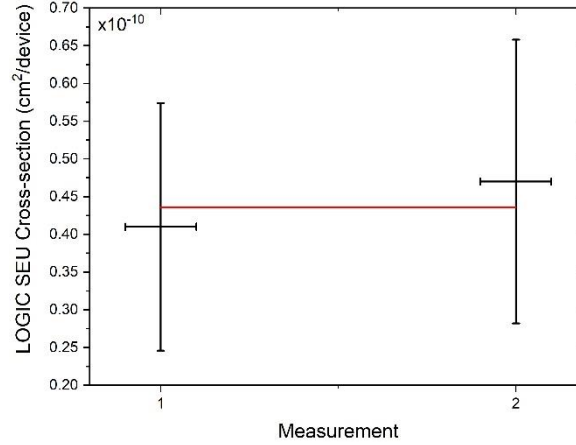


Multiple measurements of the CRAM SEU cross-section values were carried out, and the average value was found to be  $(1.02 \pm 0.37) \cdot 10^{-7} \text{ cm}^2/\text{device}$  respectively  $(0.54 \pm 0.2) \cdot 10^{-14} \text{ cm}^2/\text{bit}$ . More measurements are given in fig. 4.48.

Two measurements of the logic SEU cross-section, shown in fig. 4.49, were carried out for the LHCb-RICH firmware and an average value was found to be  $(0.44 \pm 0.17) \cdot 10^{-10} \text{ cm}^2/\text{device}$ . The logic SEU rates measurements are dominated by effect of SEUs within the CRAM, therefore is very hard to completely separate these types of SEUs. Actually, the logic SEU cross-section is just the product of the critic-bit number and the CRAM cross-section per device by number of CRAM bits on device. However, a better and faster CRAM mitigation technique should reduce the SEU rates within both CRAM and logic resources.



**Fig. 4.48** Multiple measurements of CRAM single-bit error cross-sections given per device (left side) and per bit (right side) for position 10 at CHARM [243]



**Fig. 4.49** Measurements of logic SEU cross-section values given per device for position 10 at CHARM [243]

#### 4.4.5 Extrapolation of the Results to the LHCb-RICH environment

For the extrapolation to the expected LHCb-RICH environment during the RUN 3 a 7000 hours operational time was considered. The worse-case scenario values (which include a safety factor

of 2) are in the RICH 1 region where for the electronics, and it should expect: 200 krad (Si) TID and  $1.2 \cdot 10^{12}$  HEH/cm<sup>2</sup> [191]. According to table 1.1, both RICH sub-detectors require 1272 FPGAs to be used. Therefore, as an additional safety factor, the error rates will be extrapolated to the RICH 1 environment for all FPGAs.

Assuming the average CRAM single-bit cross-section value measured during the CHARM tests and normalized with a safety factor of 2 to account for any differences between the CHARM and the LHCb-RICH radiation environments a cross-section value ( $\sigma_{\text{CHARM}}$ ) of  $(2.04 \pm 0.74) \cdot 10^{-7}$  cm<sup>2</sup>/device was obtained. For an expected fluence ( $\Phi_{\text{RICH}}$ ) of  $1.2 \cdot 10^{12}$  HEH/cm<sup>2</sup> corresponding to an operation time (t) of 7000 hours, the average number of CRAM SEUs ( $N_{\text{SEU}}$ ) within all 1272 FPGAs can be estimated by using the following equation:

$$N_{\text{SEU}} = (\sigma_{\text{CHARM}} \cdot \Phi_{\text{RICH}} \cdot N_{\text{FPGA}}) / t \quad (4.3)$$

From equation 4.3 a number of about 44400 SEU/h in all FPGAs is obtained. However, as it was observed during the test beams most of these SEU will not affect the user logic circuitry, but a very small fraction of them may still hit critical areas. Some of them will lead to creation of parasitic circuits which will contribute to the power consumption. Therefore, a fast reconfiguration of the DUT is required to minimize the dead times within its operation.

Though no SELs were observed while the DUT was irradiated with protons and at CHARM facility, the PDMDBs have the prepared to mitigate and detect micro-SELs or “Scrub-SEFIs” highlighted as high current states within the DUT. The “Scrub-SEFIs” may appear during the reconfiguration of a particular FPGA while a SEU is induced in its configuration logic.

To be able to estimate the number of logic failures besides the fluence and the logic failure cross-section, the number of critical bits within the final firmware has to be taken into account. To account the uncertainty in the estimation of number of critical bits within the final firmware design as well as to compensate the logic failure cross-section obtained at CHARM to the expected LHCb-RICH environment, a safety factor of 4 was used. Therefore, by using equation 4.4 and assuming the  $\sigma_{\text{Logic}}$  as the logic failure cross-section of  $(0.44 \pm 0.17) \cdot 10^{-10}$  cm<sup>2</sup>/device measured during CHARM tests, the estimated number of logic failures ( $N_{\text{L}}$ ) was calculated to be of about 28 logic failures/hour.

$$N_{\text{L}} = (\sigma_{\text{Logic}} \cdot \Phi_{\text{RICH}} \cdot N_{\text{FPGA}} \cdot 4) / t \quad (4.4)$$

This logic failure rate is equivalent with an average of about 100-channel failures or 1.5 fully-defective MaPMTs, this based on the observed output patterns at CHARM. Hence, during and 8-hour operational run it gets close to 800 channel failures, which represents about 0.4% from all 196608 MaPMT channels.

The TID effects will not pose a problem, as the DUT was tolerant up to 1 Mrad (Si). The expected dose rate in the LHCb-RICH environment during RUN 3 will be of 3 orders of magnitude less than the dose rates used in the test beams.

It was concluded that the KINTEX-7 FPGA is so far adequate to be used within the PDMDB of LHCb-RICH sub-detectors during RUN 3. The above error rates per hour seem manageable, if careful attention is given to the reconfiguration and FPGA-firmware reliability

and size. And, also, the SEL or scrub-SEFI events have to be mitigated upon detection in RICH electronics.

## 4.5 Conclusions

Following the Long Shutdown 2 of the LHC, the LHCb single arm forward spectrometer will be upgraded to operate at higher luminosity and with a higher trigger rate. The LHCb-RICH sub-detectors were redesigned to allow operation for higher HEH fluence – close to  $10^{12} \text{ cm}^{-2}$  and higher TID values of 200 krad (Si). The RICH MaPMT photon hit rates will be read out with custom digital hardware (PDMDBs) which embeds the commercial grade KINTEX-7 FPGA. These FPGAs are widely used in high energy physics experiments due to their lower price and high logic density. However, the main concern remains their reliability in a radiation environment.

A compressive irradiation campaign spread over a 4-year period was carried out in order to establish the reliability of the KINTEX-7 FPGA in a radiation environment, and in particular focused on the expected radiation environment in the LHCb-RICH during RUN 3 and possible RUN 4 with expected cumulative luminosity of  $50 \text{ fb}^{-1}$ . Several test beams with different particle species were used: ions at the HIF from Louvain Cyclotron Resource Centre in Belgium and at the SIRAD facility from Legnaro National Laboratories in Italy; 35 MeV protons at the Juelich Research Center in Germany and 200 MeV protons provided by proton irradiation facility at the Paul Scherrer Institute in Switzerland; and 50 keV X-Ray beam at the X-ray facility from University of Padova in Italy.

The KINTEX-7 has an excellent resilience against TID effects at least till up to about 1 Mrad (Si). The only notable TID effects were observed as small current increasings within the VCCINT and the VCCAUX power rails when irradiated with X-rays up to a TID of  $(160 \pm 32)$  krad (Si) done with a high dose rate of  $(166 \pm 33)$  rad/s. However, the room-temperature annealing effects started to be visible very early after the device irradiation.

The main concern remains the integrity of the CRAM, as its SRAM-based structure is very sensible to SEUs. Large SEU numbers within the CRAM lead to the activation of the parasitic circuits within the DUT which contributed to increase within the power consumption of the DUT, which is mostly visible on the VCCINT and VCCAUX power rail. These effects were mitigated with a full reconfiguration of the DUT done with a hybrid scrubbing procedure.

The hybrid scrubber architecture proposed to monitor and mitigate the SEUs within the CRAM is composed from the SEM IP core as internal scrubber together with an JTAG-based blind scrubber. However, this architecture proved to not be very reliable at high error rates, and three general conclusions/drawbacks were drawn on this scrubbing architecture:

- ❖ the internal scrubber logic itself has a large number of critical bits, which if affected may perturb the operation of the entire DUT user circuitry;
- ❖ the frame single-bit error correction time within the internal scrubber is very dependent with the error rates, as it takes a longer time to correct a single-bit error at high error rates;

- ❖ the blind scrubbing of the DUT while is irradiated proved to be not very reliable, as in some cases caused high current states within the VCCINT power rail, due the corruption of the DUT configuration logic.

All the radiation-induced SEU within the CRAM and the user logic were mitigated by a full reconfiguration of the DUT. Therefore, ensuring a SEU-free CRAM shall be the main concern when proposing such device to be used in a radiation environment similar with the one expected at LHCb-RICH, or other radiation environments.

## Chapter 5

# Characterization of the Axcelerator FPGA Under Radiation Exposure

The antifuse technology is an old FPGA technology designed to operate in radiation environments, especially in space experiments. As described in the introduction of chapter 4, they are one-time programmable devices as a consequence of their antifuse technology. Such FPGAs have the CRAM immune to radiation-induced SEUs. In some cases, this feature is a major drawback as the designer cannot upgrade or change its design circuitry. Therefore, the device has to be replaced with an unprogrammed/unfused device. Another major drawback is related to its performance and its density of logic resources as well as its power consumption and voltage compatibility with modern electronics, as most commercial antifuse FPGAs belong to older technology with larger technology node.

When such types of FPGAs are proposed to operate in radiation environments, the following concerns have to be addressed: TID-induced increase of the power consumption and SEE effects within the logic resources (RAM, FFs, LUTs etc.), especially the non-antifuse resources.

This chapter will present the experimental setup and the irradiation campaign carried out on a antifuse FPGA proposed to be a backup solution of the KINTEX-7 FPGA at the LHCb-RICH experiment. Several testing methodologies as well as a new DAQ system solution will be presented. The test beam results will be extrapolated to the LHCb-RICH environment phase Ia case as well as phase Ib case.

*The Axcelerator FPGA family* from Microsemi (now Microchip) are antifuse FPGAs designed with the advanced 0.15  $\mu\text{m}$  CMOS antifuse process [246]. The AX250-FG484 device was chosen to be evaluated in a radiation environment. Although low, compared with the KINTEX-7 FPGA, its I/O and logic resources are more than enough for LHCb-RICH application and they are given in table 5.1. From table 5.1 it can be observed that the AX250 device has 1408 register cells (R-cells), which is the vendor alias for sequential logic, i.e. FFs.

Therefore, the number of FFs available in this device is about 58 times lower if compared to the modern KINTEX-7 device. The same apply to the combinational cells (C-cells), which represents the vendor alias for a 3-input LUT, and their number is about 14 times lower than the modern KINTEX-7 device.

**Tab. 5.1** AX250 FPGA resources extracted from its datasheet [246]

|                            |        |
|----------------------------|--------|
| <b>Typical Gates</b>       | 154000 |
| <b>RAM size (bits)</b>     | 55296  |
| <b>Register Cells</b>      | 1408   |
| <b>Combinational Cells</b> | 2816   |
| <b>I/O Banks</b>           | 8      |
| <b>Maximum I/O pins</b>    | 248    |

## 5.1 Experimental Setup

To test the reliability of the AX250 device – from now on referred as DUT – under ionizing radiation, a custom experimental setup has been proposed to power, monitor and control the DUT all the time – that is before, during and after the irradiation tests. It was designed in compliance with available radiation test standards [4], [177]–[179], [181] as well as based on the past experience gained by designing experimental setups for other devices [201], [221].

The experimental setup architecture is given in fig. 5.1, and is mainly composed of: a custom DUT test board and an FPGA-based DAQ system. The DAQ system is used also to ensure the power management of the DUT as well as to control and to read out the DUT logic circuitry. The connections between each component are made with screened cables of at least 5 meters length and, for the high-speed data and clock signals a HDMI cable was used to ensure a proper signal integrity. Plugin adapters were designed to facilitate remote communication and control of the DUT via the DAQ system and to allow testing the DUT I/O pins.

To detect SELs or high current states, marked by current increasings within the DUT power rails, the DAQ was configured to detect any abrupt current changes and to trigger a power-down procedure (e.g. power off or power cycle) when is required and to log the event.

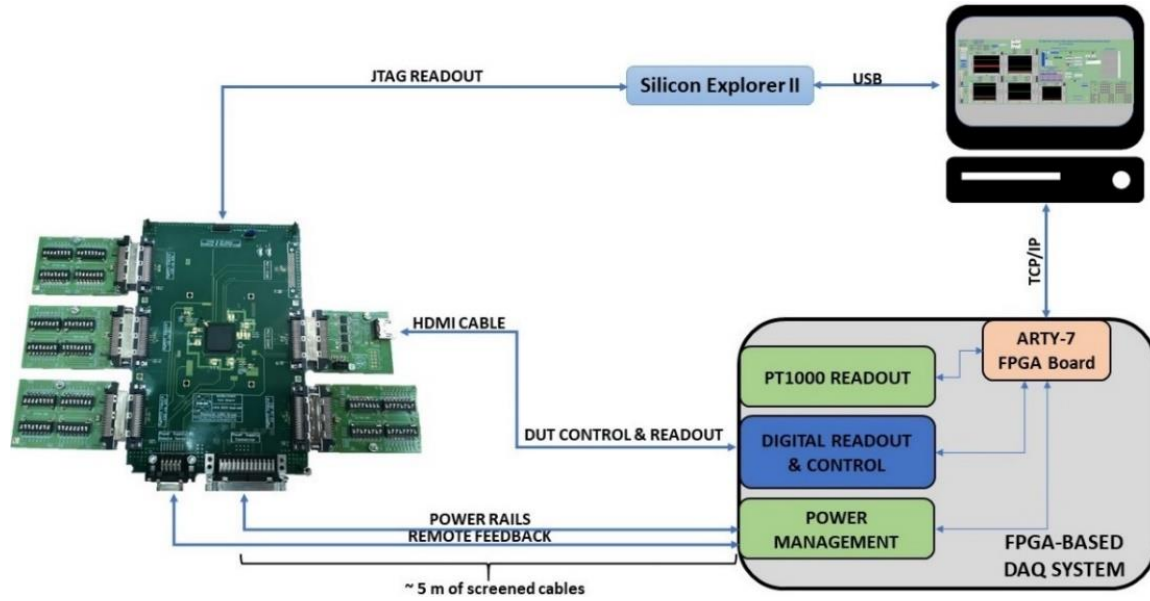
The detection of software errors, more focused on SEUs, is based on the following routine:

- ❖ A custom configurable pattern (reference pattern) is sent from the DAQ system to the DUT test board while the DAQ clock signal is allowing the FPGA to run the logic. (assuming for this firmware it use an test-board-external-clock)
- ❖ Then the pattern is shifted within a custom logic path of FFs created inside the DUT with a dedicated firmware.
- ❖ The output bit-stream containing the shifted data is sent back to the DAQ system to be compared with the reference pattern.
- ❖ Inside the DAQ, the data are analyzed and if detected, the SEUs are counted.

SEFIs are errors when usually the DUT is in a reset state and that can be detected by monitoring its power consumption and its output data.

I/O failures are detected by reading over a large number of I/O pins the same output data, which was generated in a specific pattern and then the information is sent to the DAQ to be

compared to this reference data-pattern. All the data and controls from/to DUT test board are operated in the same way, using serial links.



**Fig. 5.1** Experimental setup architecture proposed for monitoring and control of the DUT

The temperature monitoring during and after the irradiation runs is important, due to temperature dependence of DUT power consumption. The cumulative effects, as well as the annealing process non-linear parametrization are temperature dependent. The cumulative TID effects are inducing an increase of power consumption in the device, which rises the device temperature, which in turn influences the TID-induced effects, therefore adding non-linearity to the parametrization problem besides the non-linearity due to beam fluctuations and competing charge relaxation processes. Temperature monitoring of the experimental area and of the DUT package was implemented by using two platinum resistance temperature detectors (RTDs), PT1000, connected to the DAQ system over 5 meters of screened cables. These RTD sensors are known to be resilient to radiation [247], as they are used in applications with radiation environments [29].

A LabVIEW-based GUI was designed to control the operation of the experimental setup through TCP/IP intranet connection. From the GUI, the user has: the ability to control each power rail voltage, to select a clock frequency for running the DUT logic, and to perform tests by simulating radiation induced effects in the DUT. All the data concerning the DUT operation before, during and after irradiation are saved in ASCII files at a given user- configurable sampling rate.

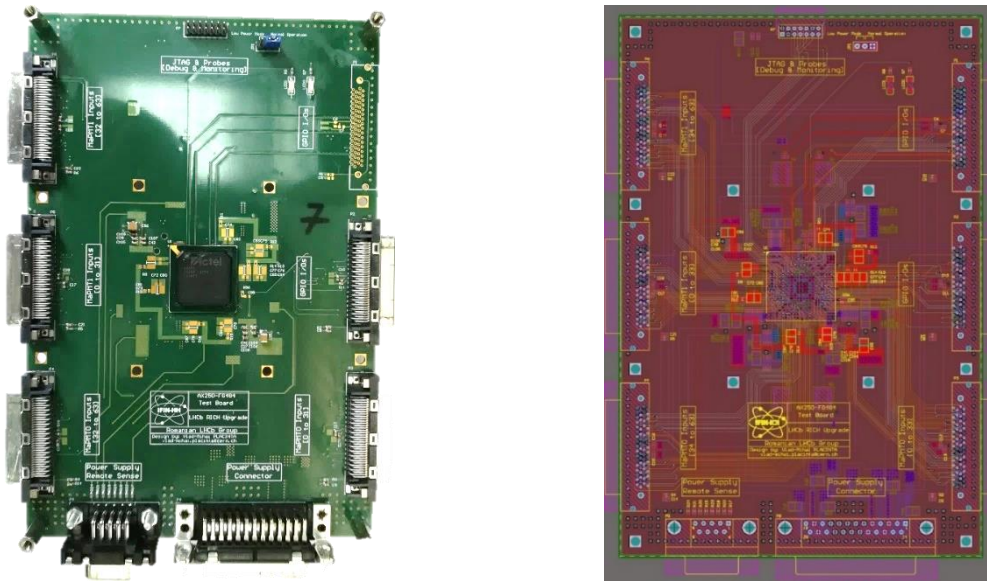
The DUT test board, shown in fig. 5.2, was designed on a 8-layer PCB around the AX250-FGG484 device, ensuring an operation with close to full FPGA functionality and with a minimum number of components on the board. More than 60% of the I/O pins were routed out from the DUT package to be used for control and testing. Very-high-density cable interconnect (VHDCI) 68-pin connectors were used to pass all the I/O pins to outside the DUT-board to the plugin adapters.



Since due to radiation constraints the power supply was placed on the DAQ system outside of the test board, a power connector was foreseen on the DUT test board. Another connector was used to ensure remote feedback to the power supplies in order to compensate the voltage drop over the cables as well as to maintain a stable voltage to the DUT.

The JTAG interface along with four probe pins were routed out, and were used to debug and to monitor various signals from the DUT logic circuitry.

On the board, there are no other active components within a 15 cm radius to the DUT. This was needed in order to ensure a protection against failures of other integrated circuits which are used in the communication with the DUT but are not intended to be irradiated. A carefully designed layout was implemented, in order to ensure a proper operation of the DUT under these conditions. The schematic diagram of the DUT test board is available in annex A5.



**Fig. 5.2** The DUT test board (left side) and its layout (right side)

The DAQ system, shown in fig. 5.3, is a key component of the experimental setup due to its role of controlling and monitoring the DUT activity. It includes 2 parts: a commercial FPGA development board, and a custom acquisition and control board. The commercial FPGA development board was chosen to be the Arty A7 board [248] due its lower price, as well as its considerable resources. The acquisition and control board, which can be seen in fig. 5.4, was designed on a 6-layer PCB with all the features needed to control and read out the DUT as well as to ensure the power management.

The DUT is powered with 7 independent rails over at least 5 meters of multi-core screened cable. The power supply is designed around 2 integrated circuits with 4 buck regulators each, i.e. the ADP5050 device [222]. The design takes into account the fact that the DUT has to be powered over a long cable. To eliminate the voltage drops on the cables as well as to secure a good transient response and the stability of each power rail, a remote feedback technique was implemented. This technique was implemented with unity gain differential amplifiers, which were used to measure the voltage across each power rail supplying the DUT. In this way, the amplifier outputs the voltage to the ADP5050 feedback network, allowing the controller to adjust the voltage and stabilize it to a desired value, thus the voltage drops on the cables are

cancelled. To test the reliability of the power supplies and to simulate various radiation-induced scenarios a custom electronic load was designed and used for this purpose [249].



**Fig. 5.3** The DAQ system composed from the commercial FPGA board connected to the acquisition and control board

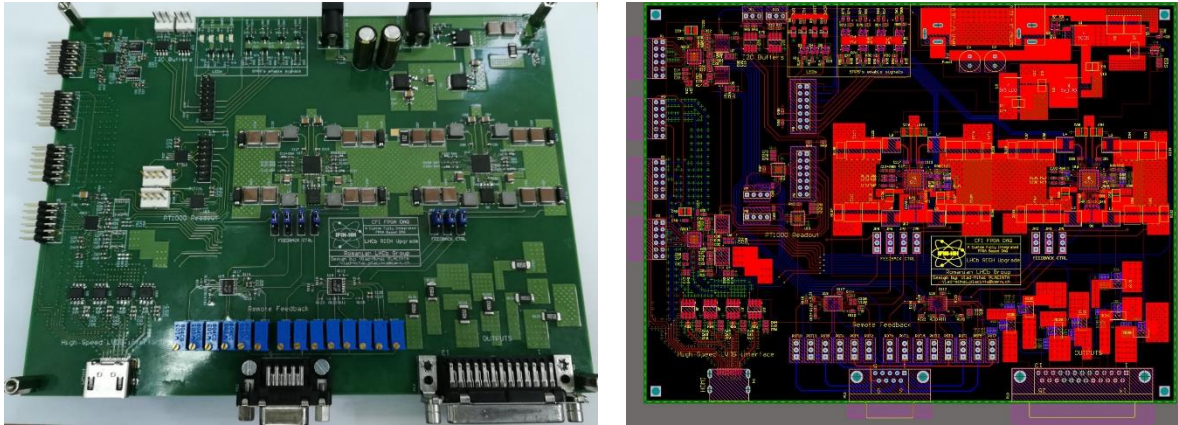
The DUT power consumption is monitored using two 16-bit 8-channel high-speed ADC units, LTC2374-16 devices [250]. One ADC is used for voltage sensing and the other one for current sensing. The current sensing is done using low resistance shunt resistors, 50 m $\Omega$ , together with high-side current shunt amplifier circuits. It allows a current-to-voltage conversion ready to be sent to the ADC inputs.

To implement the PT1000 temperature readout, MAX31865 RTD-to-digital integrated [251] were used to ensure a very good measurement resolution of 0.01  $^{\circ}\text{C}$ . The sensors are connected in a 4-wire configuration to the DAQ system providing a good noise reduction.

High speed LVDS to SE conversions and the reverse conversions are both done on the DAQ board to convert the clock and data signals which are incoming or outgoing with respect to DUT board, with these signals passing through a HDMI cable. After conversion, the outgoing signals are sent to the commercial FPGA board. The LVDS connections were preferred due to radiation and facility constraints as well as taking into account that LVDS has better noise immunity than SE, especially for long cables with high-speed signals.

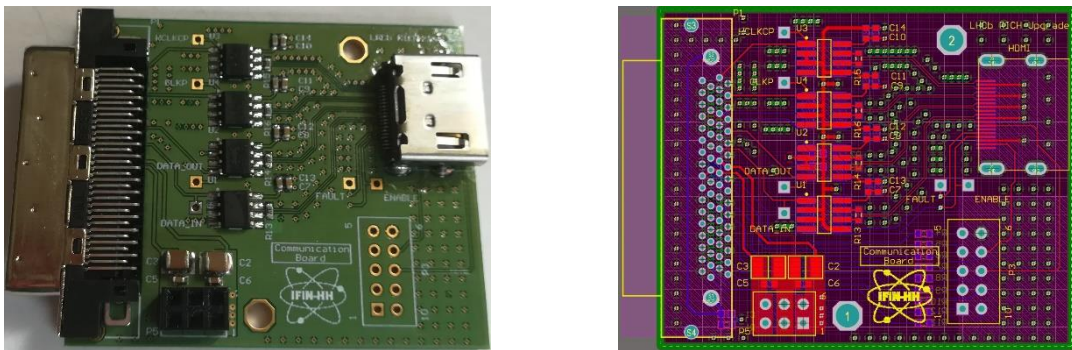
Additional functions were implemented to allow the DAQ system to power cycle and to control each power rail individually. Protections for overcurrent and overvoltage were implemented.

Finally, the DAQ system was configured to power and monitor the DUT with 7 voltage rails between 1.5 V and 3.3 V, with each rail used for various logic blocks inside DUT. The power on each of voltage rail is monitored with a resolution of 62.5  $\mu\text{V}$  and 62.5  $\mu\text{A}$ . The schematic diagram for the DAQ system is available in annex A6.



**Fig. 5.4** The acquisition and control board (left side) and its layout (right side)

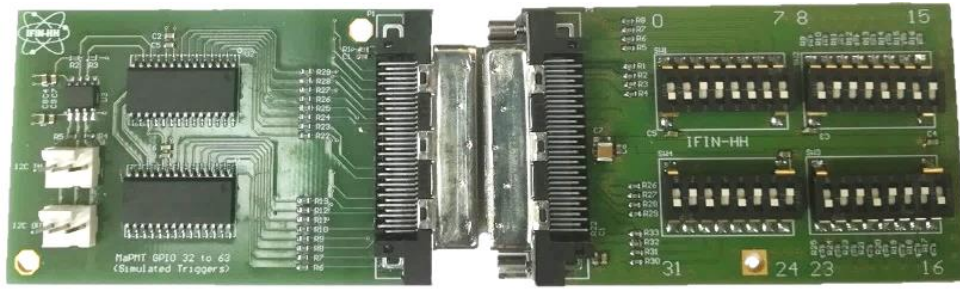
The communication and control plugin-board adapter, shown in fig. 5.5, was required in order facilitate the remote communication and control of the DUT firmware and to read out its status. It was designed as a standalone board to ensure a protection against any indirect irradiation which can occur while the DUT is being irradiated. High-speed signals like clocks and data are converted from SE to LVDS and then driven through the HDMI cable to the DAQ system. Additionally, a few low-speed and general purpose I/Os were routed out for auxiliary signals and to ensure a better control of the DUT logic. The schematic diagram for the communication and control plugin-board is available in annex A7.



**Fig. 5.5** The communication and control plugin adapter (left side) and its layout (right side)

Due to fact that the DUT will be used to read out hundreds of external trigger signals through its I/O pins in its target LHCb-RICH application, a solution to test the I/O pins and device configuration reliability was needed. Two solutions were proposed, both implying to generate outside the test board a specific pattern and to read it continuously with 128 of the I/O pins while the device is being irradiated. The first method uses static switches to simulate a pattern. It is the simplest way to inject static signals into the I/O pins of the DUT. However this solution has the drawback of not being able to change the pattern dynamically. To allow the pattern to be changed dynamically a second solution has been proposed which replaced the switches with 16-bit I<sup>2</sup>C I/O expanders connected to the DAQ system. The pattern can be changed any time by the user from the GUI. In fig. 5.6 both dynamic and static I/O plugin boards are shown.





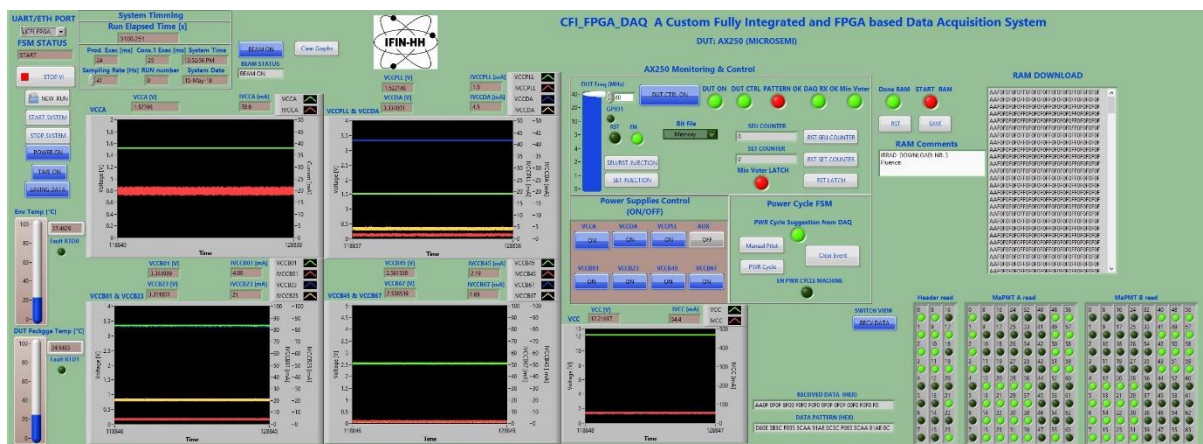
**Fig. 5.6** Dynamic (left side) and static (right side) I/O plugin boards

A complex GUI was designed using LabVIEW software to control the DAQ system and to read out the DUT data and its electrical parameters using either an UART or TCP/IP interface. It was designed using a finite state machine (FSM) architecture which allows fast control and high acquisition rates. The GUI front panel is shown in fig. 5.6 and it is mainly organized as follows: the acquisition block, the power supply control block, the DUT control block, and the timing control block.

The acquisition block oversees all the acquisition. This is done by reading out the data containing all the measurements supplied by the DAQ. Besides the acquisition, this block is plotting in real time the DUT power consumption per each rail on a set of graphs, all at user request. Measurement data are saved in ASCII files for later analysis.

The power control block is responsible for controlling the power flow on the DUT. Each of the power rails - including the main rail which is supplying the DAQ system - can be controlled by the user from the GUI. Overcurrent and overvoltage protection circuits are implemented and the user can configure and enable them at any time. A specific power sequencing can be implemented on each of the DUT power rails to allow a proper start-up of the DUT. This operation is required in complex integrated circuits like FPGAs, where multiple power rails with different voltages are used.

The timing block is ensuring the low latency times in the entire system and it is responsible for configuring the system timing as well as the acquisition rate from DAQ, which is upper-limited to 1 KHz.



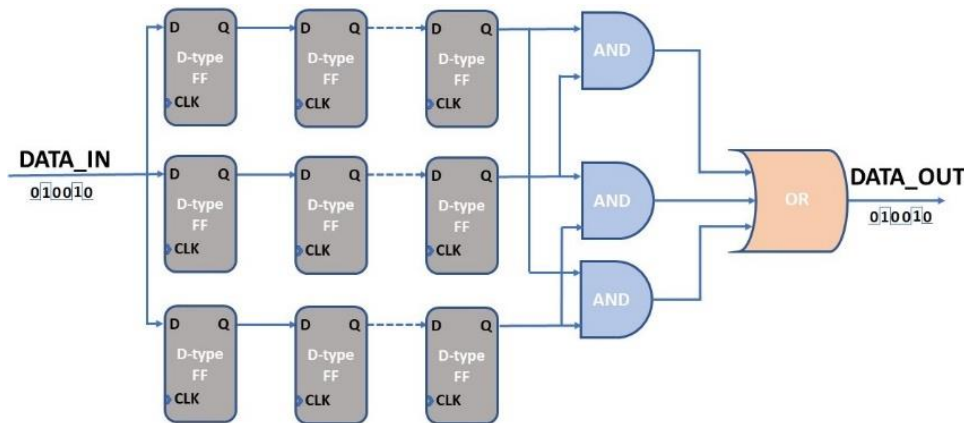
**Fig. 5.7** The LabVIEW-based GUI designed to communicate with the DAQ system

## 5.2 Proposed FPGA Firmware for Radiation Testing

For a given radiation environment, a very important step when evaluating the reliability of an FPGA is its firmware. Due to the fact that the CRAM corruption within the AX250 device is not such a concern as it was in the case of the KINTEX-7 device, the attention was directed to its logic resources. Therefore, two firmware versions were proposed to allow testing individual resources like: the user FFs and the embedded RAM. Additionally, a more complex and realistic firmware version was implemented to emulate the LHCb firmware of the Upgraded LHCb-RICH subdetectors. Each firmware implementation was controlled by the DAQ system through the communication and control board attached to the DUT test board, whereas the DUT readout being passed to DAQ system the same way. Basically, each firmware architecture, share more or less the same control signals. The DAQ system is providing: a 40 MHz SE clock to run the DUT logic, software reset and enable signals to control the logic.

Unlike the TMR firmware which basically is just a path of FFs and LUTs created within the DUT, the other two firmware versions required a transmitting logic core to be able to send the data at user/DAQ request. Therefore, a custom UART core with a baud rate of 1 Mbaud which was customized to have a throughput of 152 bits of data per transmission frame - was designed within each firmware version. Although this logic core may fail itself due to radiation, several fail-safe signals and controls were added to check that core is working as expected.

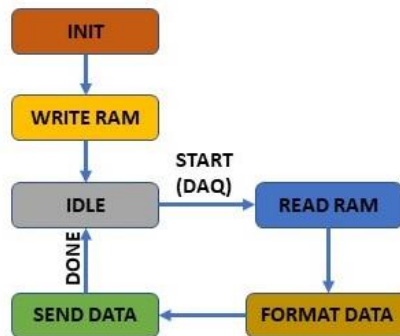
*The basic TMR architecture* was applied to the DUT FFs to form a logic structure path such as the one provided schematically in fig. 5.8 and which was also used on the KINTEX-7 tests. An additional feature to this particular firmware version was a minority voter in parallel with the majority voter to detect when a single chain of FFs is affected. The minority voter applies XOR logic to all three FFs chains and if any of them are different than the others 2 then its output will be “1”. In this way the DAQ will sense this state change. The VHDL code used to implement this firmware structure is available in annex A8.



**Fig. 5.8** Basic TMR architecture

To test the embedded RAM resources, a dedicated firmware was used within an FSM to write hard-coded values to the RAM bits. The RAM is written with a 36-bit hard-coded pattern

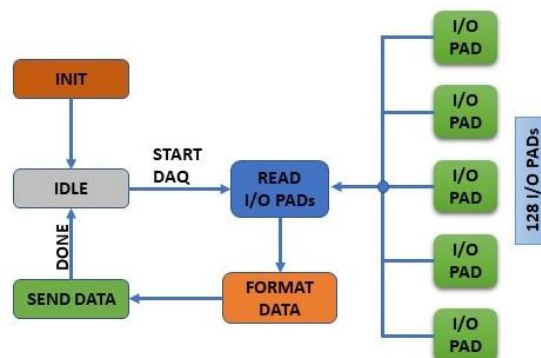
within each RAM address. The data from 4 RAM addresses concatenated with an 8-bit header form a 152-bit data frame. Then, at user request, the RAM content is read and downloaded frame by frame to be compared with a reference data stored within the DAQ system, and, the SEU rates are computed. The general structure of the FSM is given in fig. 5.9 and the VHDL code used to implement this firmware is available in annex A9.



**Fig. 5.9** The general FSM structure within the RAM-readout firmware

A more compressive and realistic firmware was designed to emulate the firmware version proposed to be used with the LHCb-RICH PDMDBs during the LHCb upgrade phase Ia. For this firmware configuration, the additional static I/O plugin adapters were used to generate a static signal pattern, by pulling “low” or “high” the state of 128 DUT input pins. Within this firmware, at user request the state of the 128 input pins is read out at a 40 MHz rate. The data is concatenated with a 24-bit header to form a frame of 152-bit length. Then by using the custom UART core, the data is sent out to the DAQ system. Inside the DAQ, the data is compared with the reference pattern, and if any, the logic failure rates are computed from failure counts. Its FSM architecture is given in fig. 5.10 and the VHDL code used to design this firmware is available in annex A10.

While exposed to radiation, there is a chance that the FSM itself will be affected in a way that cannot be recovered by a software reset. Therefore, if such event occurs, in order to ensure a clean reset of the firmware, a power cycle of the DUT is required, and the dead-time is measured to correct the SEE rate values. In table 5.2 a summary of logic resource usage per each firmware version is given.



**Fig . 5.10** The general FSM structure within the LHCb-RICH like firmware

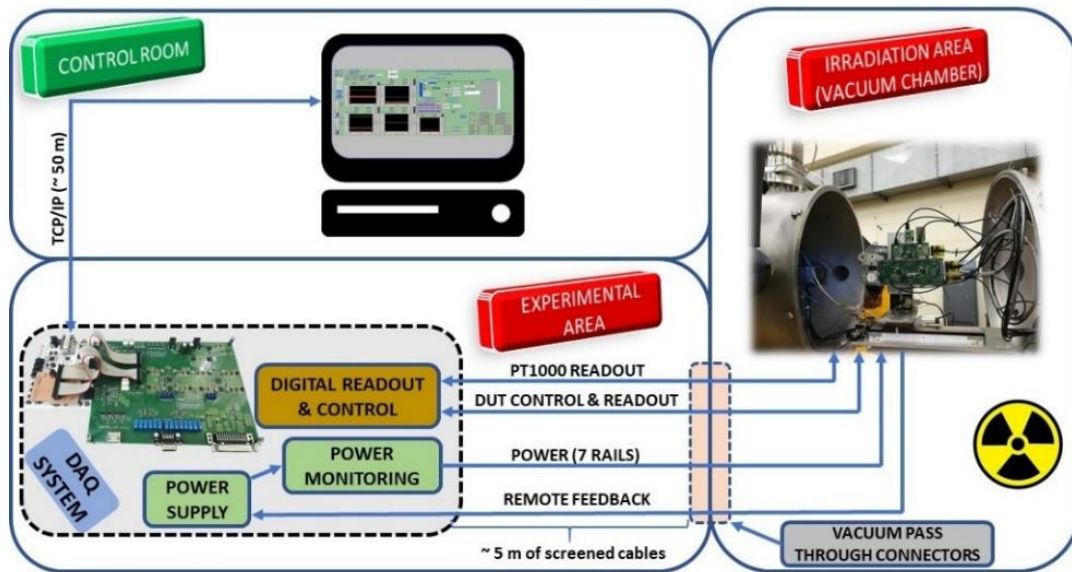
**Tab. 5.2** Logic resources usage within the AX250 for all firmware versions

| Firmware           | R-Cells    | C-Cells    | RAM Blocks | I/O Cells |
|--------------------|------------|------------|------------|-----------|
| Basic TMR          | 846 (60 %) | 2          | 0          | 5         |
| RAM Readout        | 418 (30 %) | 846 (30 %) | 8 (66 %)   | 7         |
| LHCb-RICH firmware | 326 (23 %) | 124 (2 %)  | 0          | 135       |

### 5.3 Test Beam Results and Analysis

The AX-250 device was tested with 24 MeV protons beams at the SIRAD facility [208] from Legnaro National Laboratories in Italy. Additionally, an X-rays test beam was carried out at the X-ray radiation facility [211] from Padova University in Italy. After each test beam a compressive room-temperature annealing study was carried.

As in case of the KINTEX-7 device, a general irradiation setup was put together, shown in fig. 5.11, with its sketch based on the architecture presented in fig. 5.1. In this way, only the DUT test board was placed in the front of the beam while its connections to the DAQ system were done through 5 m screened cables. The proton irradiation was carried out in a vacuum chamber in a similar way with the ion irradiation runs done for KINTEX-7. Therefore, vacuum pass-through connectors were used to connect the screened cables between the DUT test board and the DAQ system. The same setup was easily adapted for irradiations carried out in air.

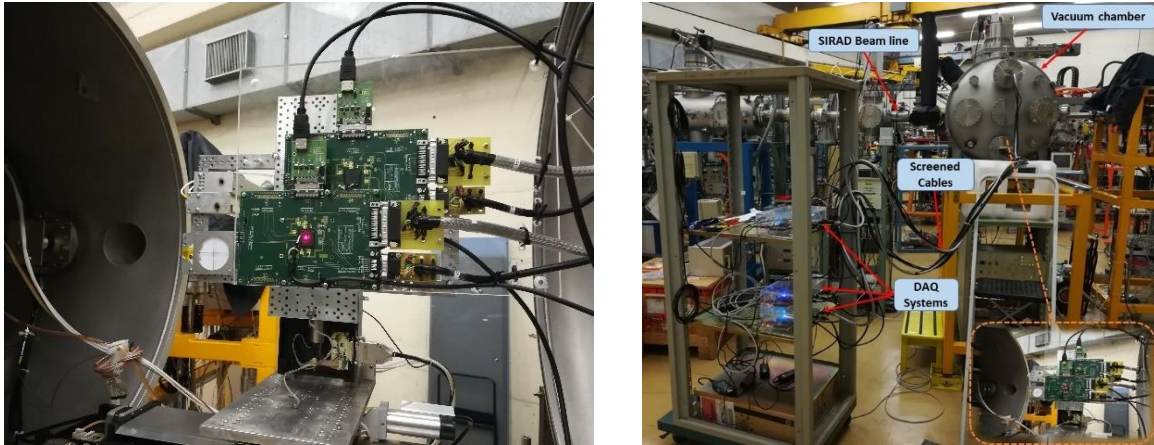
**Fig. 5.11** The general layout of the DUT irradiation setup

#### 5.3.1 Proton Irradiation

The SIRAD facility provided 24 MeV protons beam with flux values between  $10^8$  and  $10^9$  protons/cm<sup>2</sup>/s and the DUTs were exposed to a fluence of about  $(2.5 \pm 0.5) \cdot 10^{13}$  protons/cm<sup>2</sup>. The energy loss within the DUT package was estimated to be around  $(3.71 \pm 0.7)$  MeV.

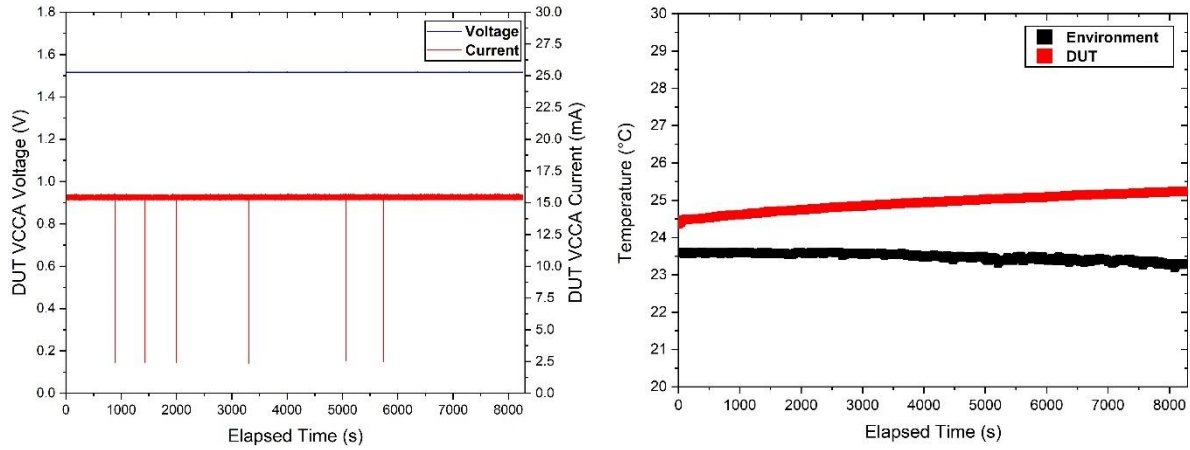


The proton irradiation was split in 2 days and 5 DUT test boards were tested with measurements of TID effects and SEEs within its dedicated logic resources. Between each irradiation day, a pause of a several days was scheduled to allow time for the deactivation of the vacuum chamber before replacing the DUT test boards and for annealing measurement. Fig. 5.12 shows the DUT test boards mounted on the sampled holder inside the vacuum chamber and the rack containing the DAQ systems connected via screened cables. The position of each DUT was determined and stored by using the laser alignment with each DUT moving on the X and Y axis. The environmental temperature probe was tied to the DAQ rack at about 2 meters elevation with respect to the floor. The package temperature probes were mounted in the corner of each DUT package.

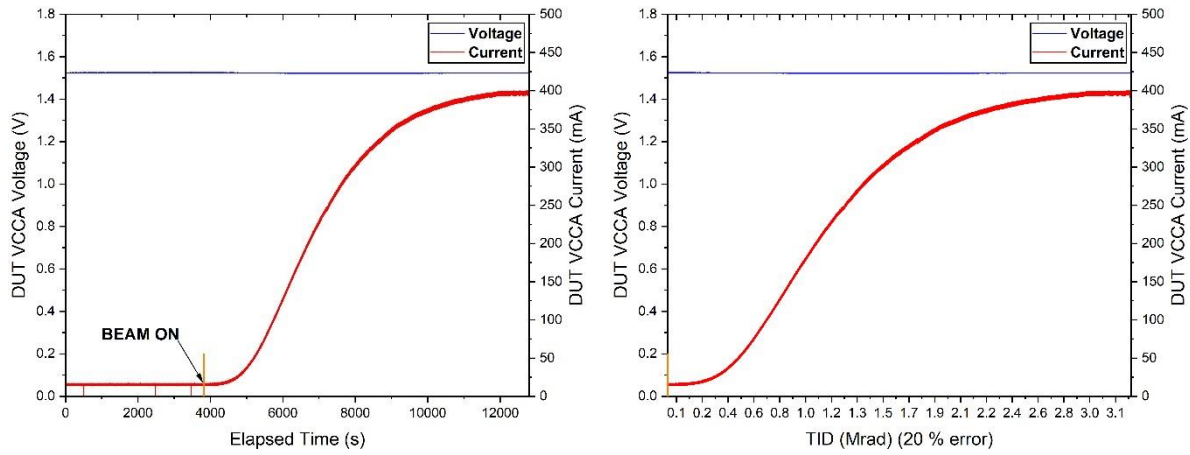


**Fig. 5.12** The DUT test boards mounted on the sample holder within the SIRAD vacuum chamber (left side) and a close-up of the irradiation setup placed in the vicinity (right side)

The first day of irradiation started with only 2 test boards mounted inside the vacuum chamber. Each of these test boards had the basic TMR logic running at 40 Mhz. A first run with a dose rate of  $(155 \pm 31)$  rads/s was applied to one DUT summing up a fluence of  $(9.4 \pm 1.9) \cdot 10^{11}$  protons/cm<sup>2</sup> which corresponds to a TID of  $(320 \pm 64)$  krad (Si). No TID induced effects were observed up to this TID, nor SEEs within the TMR logic. The evolution of the DUT core power consumption, as well its package temperature during this run can be seen in fig. 5.13. However, at a high TID of  $(3.2 \pm 0.64)$  Mrad (in Si and cumulated value between both runs) delivered with a dose rate of  $(363 \pm 73)$  rads/s, TID-induced increase of the leakage current within the DUT power consumption starts to be visible after  $(640 \pm 128)$  krad (Si). Although, all power rails supplying the DUT had some increase in power consumption, the most visible was observed on its core-power rail, VCCA. Fig. 5.14 shows the evolution of the DUT core current as function of time as well as function of TID (with TID being almost proportional to time). As expected, an increase in the power consumption means an increase of power dissipation, hence the DUT package temperature increased up to about 38 °C while the environmental temperature remained close to 23 °C, see fig. 5.15.

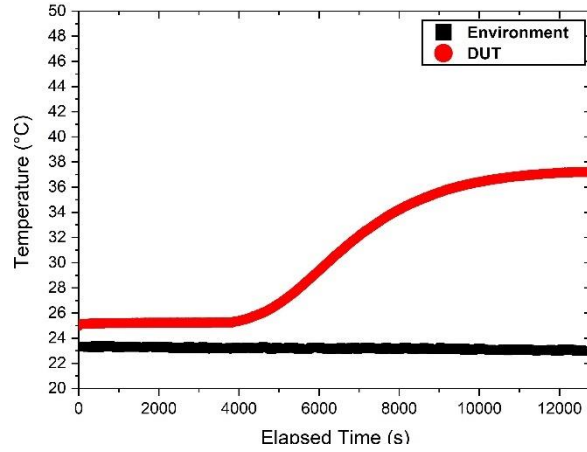


**Fig. 5.13** The evolution of DUT core current (left side) and its package temperature (right side) during a run of  $(320 \pm 64)$  krad (Si) done with a dose rate of  $(155 \pm 31)$  rad/s

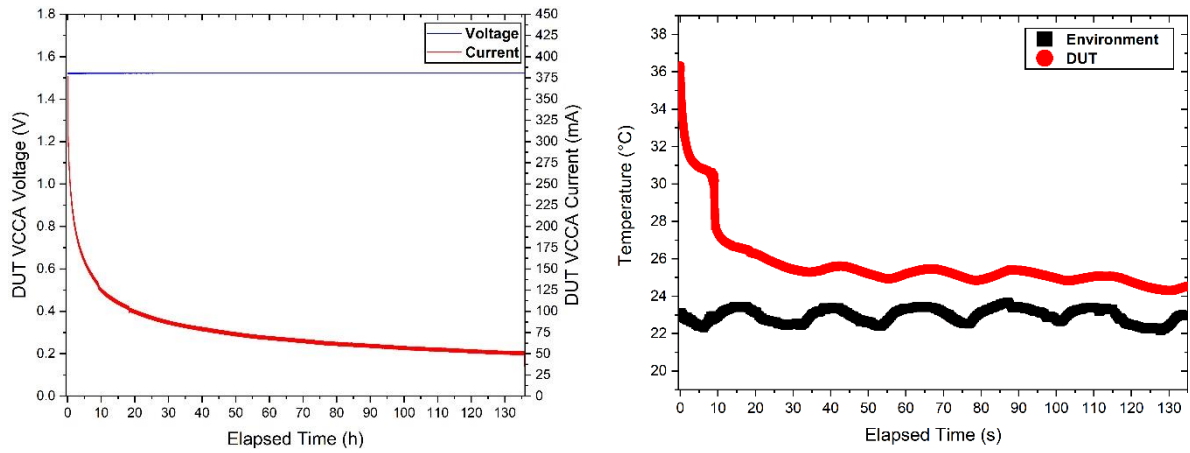


**Fig. 5.14** The evolution of DUT core current as a function of time (left side) and TID (right side) during a run of  $(3.2 \pm 0.64)$  Mrad (Si) done with a dose rate of  $(363 \pm 73)$  rad/s

A strong room-temperature annealing, prompted by hole relaxation, was observed as the DUT core current started to decrease in absence of beam. Within the first 5 hours the current decreased by a factor of 2. This is due to the fast relaxation of the hole traps near the Si-SiO<sub>2</sub> interface. However, the evolution of the current drop rate of the annealing curve indicate the presence of other populations of hole traps located at farther distance from the Si-SiO<sub>2</sub> interface within the oxide, within much larger relaxation times. Therefore, with the DUT placed under normal laboratory conditions, the core current decreased from about 375 mA to about 50 mA in about 135 hours of annealing at room temperature. As a consequence of the overall power decrease, its package temperature, too. Fig. 5.16 shows the annealing curve and its temperature variation during 135 h of measurements. The average environmental temperature was of about 23 °C, with  $\pm 1$  °C variations correlated to the day/night operations.

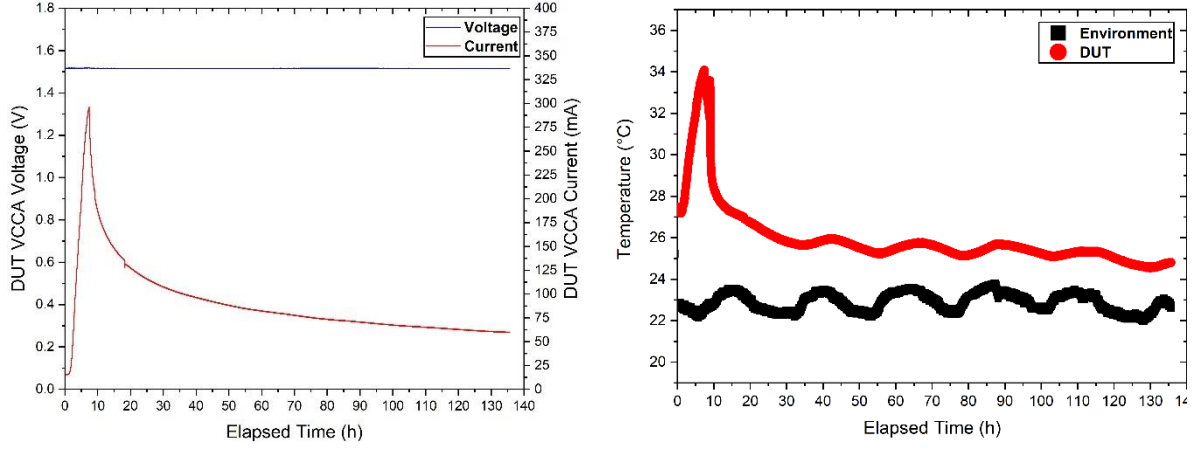


**Fig. 5.15** The DUT package and environmental temperature measurements when exposed up to  $(3.2 \pm 0.64)$  Mrad (Si) and with a dose rate of  $(363 \pm 73)$  rad/s



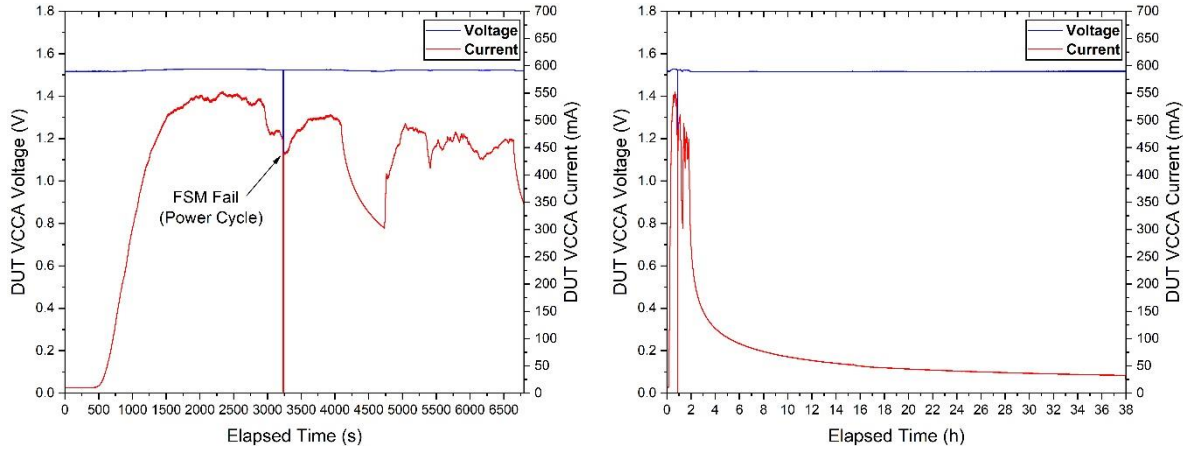
**Fig. 5.16** The annealing curve of the DUT (Si) (left side) and its temperature conditions (right side) after it was irradiated up to  $(3.2 \pm 0.64)$  Mrad and with a dose rate of  $(363 \pm 73)$  rads/s

Within the first irradiation day, another run of  $(2.7 \pm 0.3)$  Mrad (Si) corresponding to a fluence of  $(0.85 \pm 0.09) \cdot 10^{13}$  protons/cm<sup>2</sup> was carried out on second DUT. However, the average dose rate was by a factor of 3 lower than the previous run,  $(123 \pm 25)$  rads/s. Therefore, as it can be seen in the left side of fig. 5.17, the slope of the current increase is strongly dependent on the flux value, when compared to the results seen in fig. 5.14. However, the annealing current drop rate was observed to be similar with the one seen on the previous DUT irradiated with a higher dose rate. In the same manner, in the right side of fig. 5.17 it can be observed the evolution of its package temperature and its variation with the day/night activities within the experimental area.



**Fig. 5.17** The evolution of DUT core current (left side) and its package temperature (right side) during a run of  $(3.2 \pm 0.64)$  Mrad (Si) done with a dose rate of  $(123 \pm 25)$  rad/s and combined with over 100 h of room-temperature annealing

On the second day of irradiation, a run with a very high dose rate of  $(1248 \pm 250)$  rad/s was carried out on a DUT which had the LHCb-RICH-like firmware running inside. A very high early increase of the leakage current was observed followed by a saturation and slight decrease of the core up to a dose of  $(8 \pm 2)$  Mrad (Si), see fig. 5.18. However, as in the previous cases, the room-temperature annealing and charge relaxation is very visible in absence of beam. On the left side of fig. 5.18 it may also be seen the variations of the core power consumptions with the instability of the beam followed by almost 2 days of annealing.

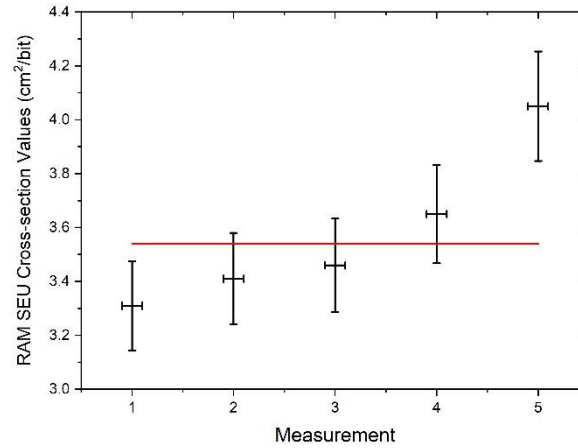


**Fig. 5.18** The evolution of DUT core current (left side) together with its 36 h room-temperature annealing curve (right side) during a run of  $(8 \pm 2)$  Mrad (Si) done with a dose rate of  $(1248 \pm 250)$  rad/s

During this run, 3 failures were observed: one logical error within the FSM which was only recovered by a hardware reset (power cycle), and 2 SEUs within the data frame coming from the DUT. Therefore, by summing up these errors a value of  $3^{+3.4}_{-1.4}$  for a 95 % CL it obtained, and the upper limit of logic error cross-section was calculated to be  $(2.56 \pm 0.51) \cdot 10^{-13}$  cm<sup>2</sup>/device for a fluence of  $(2.5 \pm 0.5) \cdot 10^{13}$  protons/cm<sup>2</sup>. This cross-section corresponds to

extreme circumstances of dose rate (1 krad/s) hence it should be counted more as an upper limit on SEU rate than as an actual measurement of the SEU cross-section.

Several measurements of SEU rates within the embedded RAM resources were carried out with  $((24 \pm 0.5) - 3.7)$  MeV protons beam. The average value of SEU cross-section was measured to be  $(3.57 \pm 0.18) \cdot 10^{-14} \text{ cm}^2/\text{bit}$ . The value is similar with other independent measurements available in literature [252]. In fig. 5.19 are given more measurements of the SEU rates within the RAM resources.

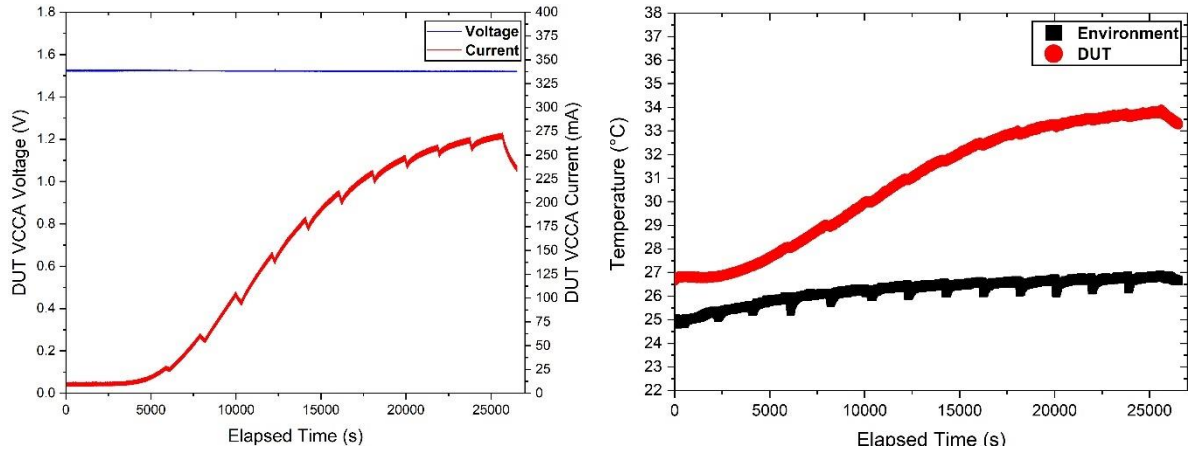


**Fig. 5.19** SEU cross-section measurements within the embedded RAM resources for a proton energy of  $(24 \pm 0.5)$  MeV at package surface

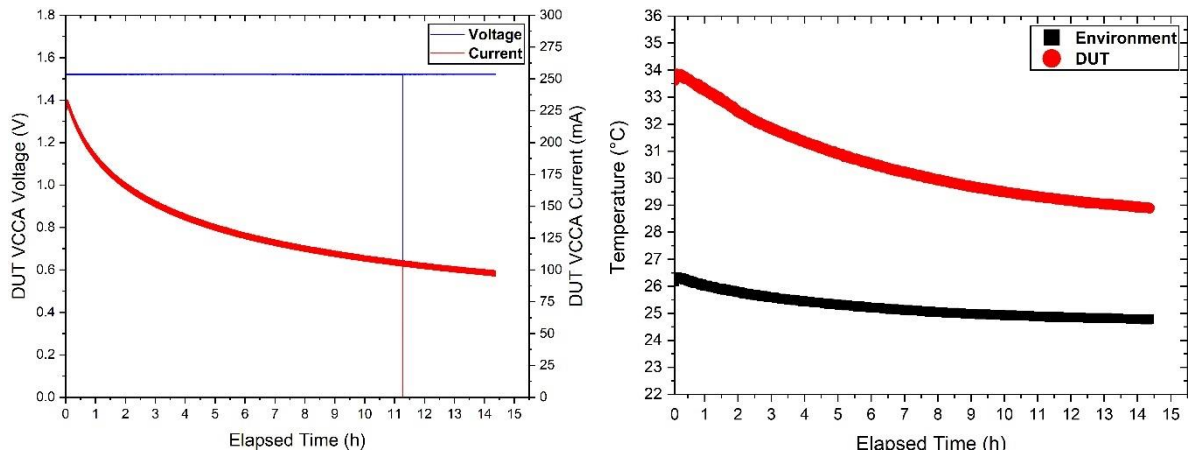
### 5.3.2 X-Ray Irradiation

Two new DUT test boards were tested with 50 KeV X-rays beam provided by the University of Padova, to confirm the TID effects observed with protons beam. The DUTs were exposed with an average dose rate of  $(100 \pm 20)$  rad/s in several irradiation steps, till up to a TID of  $(2.3 \pm 0.46)$  (Si) Mrad per each device. As expected, no errors were observed within the DUT logic. However, the same TID-induced increase of leakage currents was present with the same magnitude within the DUT core power consumption, as it can be seen in the left side of fig. 5.20. From the right side of fig. 5.20, the same package temperature dependence with the power consumption can be observed for an environmental temperature close to 26 °C. It follows the same room-temperature annealing rate, which was already observed during protons beam, see fig. 5.21.





**Fig. 5.20** The evolution of DUT core current (left side) and its package temperature (right side) during a run of  $(2.3 \pm 0.46)$  Mrad (Si) done with a dose rate of  $(100 \pm 20)$  rad/s done in steps with X-Rays beam



**Fig. 5.21** The annealing curve of the DUT (left side) and its temperature conditions (right side) after it was irradiated with X-rays up to  $(2.3 \pm 0.46)$  Mrad (Si) done in steps with a dose rate of  $(100 \pm 20)$  rad/s

## 5.4 Model Parametrization of TID-Induced Increased Leakage Current

The increase of current consumption within a CMOS structure during exposure to ionizing radiation is a well-known and studied problem. As described in section 2.2.1, such increase could be induced through the activation of a parasitic transistor channel within the STI/LOCOS of the NMOS transistor in a CMOS structure. This leads to additional intra-device drain current added to the overall CMOS current consumption.

Several physics-based modelling approaches are available in literature to predict the leakage current values within a device when irradiated up to certain TID [253]. However, due to the fact that the AX250 is a commercial-grade device, its layout parameters related to its

0.15  $\mu\text{m}$  technology node were not available. This is usually a general rule for all commercial-grade devices.

In literature the current measurements on CMOS devices after irradiation are parametrized on the assumption of radiation-induced parasitic transistors in STI/LOCOS. The present parametrization follows and expand the model outlined in [130] in parametrizing the measurement data on core current with assumption of induced parasitic transistors within the STI substrate of a NMOS transistor inherent in the AX250 device.

As the reference model suggested, the TID-induced current consumption can be described by using the transfer characteristics of both the actual NMOS transistor and the parasitic one. The following equations show the simplified transfer characteristics of any NMOS transistor when is operated in saturation:

$$I_D \sim 0 \quad \text{for } V_{GS} < V_{thr} \quad (5.1)$$

$$I_D \sim c' \cdot (V_{gs} - V_{thr})^2 \quad \text{for } V_{GS} \geq V_{thr} \quad (5.2)$$

where  $I_D$  is drain current,  $V_{thr}$  is the threshold voltage and  $V_{GS}$  the gate-to-source voltage. The  $c'$ -parameter is a proportionally constant which contains all the technological aspects, regarding the lengths, widths, oxide capacitance, the mobility of the minority carriers within the channel of the transistor etc. The sub-threshold currents are neglected in this model.

Due to the fact that the electric field within the parasitic transistor channel originates from the effective space charge in the STI, and assuming an electric field proportional with the effective space charge, the gate-to-source voltage of the parasitic transistor is replaced by the effective number of charges along the STI wall in the oxide layers,  $N_{eff}$ . In the same manner the threshold voltage is given by the threshold number of charges  $N_{thr}$ . Therefore, the equations 5.1 and 5.2 are converted in equations 5.3 and 5.4 to describe the transfer characteristics of the parasitic transistor and its drain current  $I_{Dp}$ :

$$I_{Dp} = 0 \quad \text{for } N_{eff} < N_{thr} \quad (5.3)$$

$$I_{Dp} = c \cdot (N_{eff} - N_{thr})^2 \quad \text{for } N_{eff} \geq N_{thr} \quad (5.4)$$

where  $c$ -parameter is equivalent with the  $c'$ -parameter from equation 5.2 that contains all the technological parameters related to the induced parasitic channel into the STI.

Assuming the fact that the  $N_{thr}$  is constant in time, with temperature and with the accumulated dose, then a TID-induced increase in current consumption can be described with a parametrization of the TID-induced number of effective charges  $N_{eff}$ . Further, the drain current of the parasitic transistor when is operating at saturation has an approximated quadratic dependence on gate-to-source voltage, and implicitly this additional parasitic current considered as drain current within a parasitic transistor channel has a purely-quadratic charge dependence. Hence, the global drain current  $I_{Dt}$  that includes the drain currents for both the actual NMOS transistor and the parasitic one can be approximated by the following simplified equations:

$$I_{Dt} = I_0 \quad \text{for } N_{eff} < N_{thr} \quad (5.5)$$



$$I_{Dt} = c \cdot (N_{\text{eff}} - N_{\text{thr}})^2 + I_0 \quad \text{for } N_{\text{eff}} \geq N_{\text{thr}} \quad (5.6)$$

where  $I_0$  is the baseline value of the drain current either in on or off state.

From [130], it can be generalized the exponentially-decaying deep oxide hole-traps and interface trap model by considering several layers with different trap concentrations and different decay/annealing time. Given the fact that the full decay law of hole-traps in oxide involve a convolution of an exponential decay function with a space-distribution function of trapped charges relative to the Si-SiO<sub>2</sub> interface (i.e. deepness of charge position within oxide), it can be approximated this by taking a 6-layer approximation for the decay law of all traps in oxide. Hence, in equation 5.7 is given the parametrization for the core-current  $I(t)$  measurements done in the Legnaro-Laboratory experiment on one AX250 FPGA:

$$\begin{aligned} I &= I_0 & \text{for } 0 < t < 3000 \\ I &= \left\{ \sum_{i=1}^6 c_i \cdot d_{\text{Legnaro}} \cdot \tau_i \cdot [1 - \exp(-\frac{26000}{\tau_i})] - 3.82 \right\}^2 + I_0 & \text{for } 3000 < t < 26000 \\ I &= \left\{ \sum_{i=1}^6 c_i \cdot d_{\text{Legnaro}} \cdot \tau_i \cdot [1 - \exp(-\frac{26000}{\tau_i})] \cdot \exp(-\frac{t-26000}{\tau_i}) - 3.82 \right\}^2 + \\ &+ I_0 & \text{for } 26000 < t < 26300000 \end{aligned} \quad (5.7)$$

The baseline current ( $I_0$ ) is 15.4 mA and the measured current begins a sharp rise after 3000 seconds during irradiation phase. After 26000 seconds (7.2 hours) of irradiation at a dose rate ( $d_{\text{Legnaro}}$ ) of about 116 rad/s, the beam was off and it was measured the room-temperature annealing parameters during a time span of about 4.5 to 5 days. The 5-decay model fit, shown in fig. 5.22, and done with equation 5.8 allowed to extract the c-times and d-parameters, except for the very long-lived charge population in 6<sup>th</sup> layer,  $\tau_6$  being found from the analysis of Padova X-ray data and the offline measurements done in Bucharest at 86 days after irradiation. This X-ray data analysis gave a  $\tau_6$  estimate of 304 days with 30 % uncertainty, plus a constraint on lower limit much in excess of 100 days.

$$\begin{aligned} I &= [p_0 \cdot \exp(-\frac{t_0}{p_1}) + p_2 \cdot \exp(-\frac{t_0}{p_3}) + p_4 \cdot \exp(-\frac{t_0}{p_5}) + p_6 \cdot \exp(-\frac{t_0}{p_7}) + \\ &+ p_8 \cdot \exp(-\frac{t_0}{p_9}) + p_{10} + (p_{11} \cdot T)]^2 + I_0 \end{aligned} \quad (5.8)$$

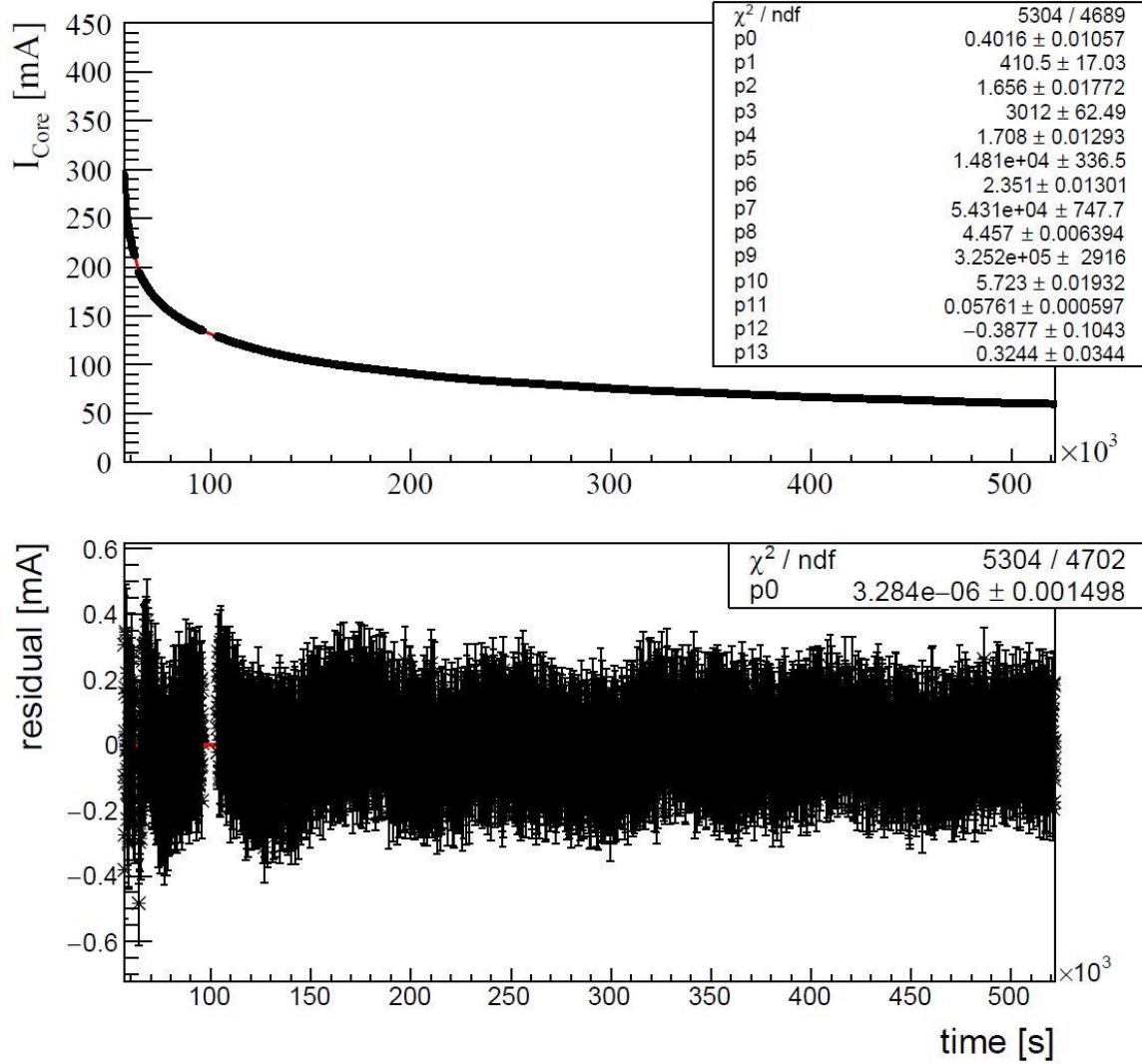
The value of charge threshold  $N_{\text{thr}}$  needed to activate the parasitic transistors in the NMOS technology is estimated to be 3.82 given in arbitrary units due to the lack of knowledge on c-parameter in the formula – this value depend on the technological fabrication process of the device. The c-parameter could be extracted from the fit, but as their exact values are not relevant for the present objective of extrapolating to LHCb case, the number was kept in arbitrary units. Therefore, the number of effective charges  $N_{\text{eff}}$  can be expressed as the sum of 6 charge populations in the oxide:

$$N_{\text{eff}} = \sum_{i=1}^6 c_i \cdot d_{\text{Legnaro}} \cdot \tau_i \cdot [1 - \exp(-\frac{t}{\tau_i})] \quad (5.9)$$

during irradiation with  $t = 0$  at the start of irradiation procedure. The equation of the induced effective number of charges during the room-temperature annealing process is:

$$N_{\text{eff}} = \sum_{i=1}^6 c_i \cdot d_{\text{Legnaro}} \cdot \tau_i \cdot [1 - \exp(-\frac{t_0}{\tau_i})] \cdot \exp(-\frac{t_0 - t}{\tau_i}) \quad (5.10)$$

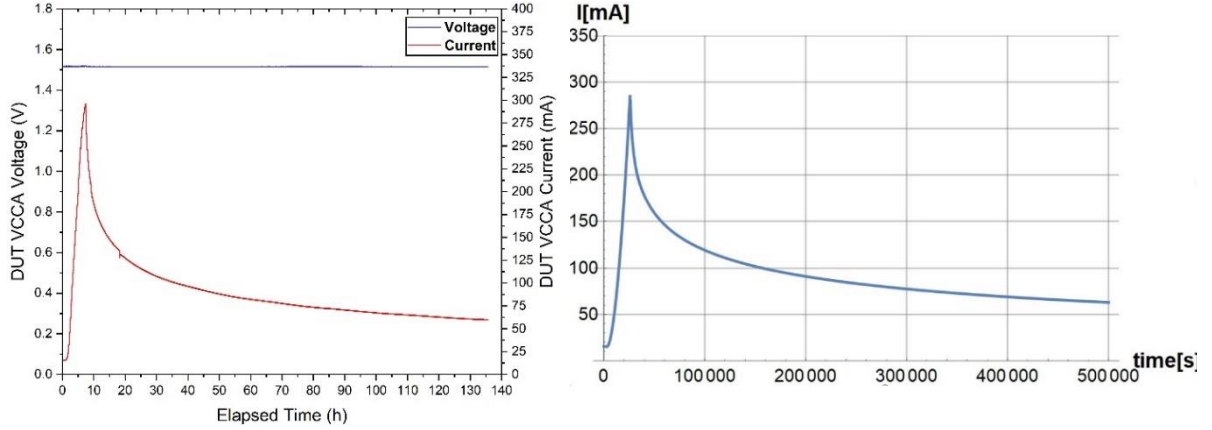
here  $t_0$  is the end of irradiation phase and numerically is 26000 s for the example herein.



**Fig. 5.22** Five exponential fit done with equation 5.8 on the annealing measurements showing the annealing time for different hole-trap populations:  $p_1$  ( $\tau_1$ ),  $p_3$  ( $\tau_2$ ),  $p_5$  ( $\tau_3$ ),  $p_7$  ( $\tau_4$ ) and  $p_9$  ( $\tau_5$ )

The parametrization is displayed in fig. 5.23 and was done by using equation 5.7. It corresponds to 6 decay parameters, 6 amplitudes and a constant y-shift with the base-line of the current consumption within the AX250. The annealing times vary over a broad range from

410 seconds to 304 days. The actual values from the data fits are:  $\tau_1 = 410$  s,  $\tau_2 = 3 \cdot 10^3$  s,  $\tau_3 = 15 \cdot 10^3$  s,  $\tau_4 = 54 \cdot 10^3$  s,  $\tau_5 = 32 \cdot 10^4$  s, and  $\tau_6 = 26.3 \cdot 10^6$  s. The amplitude terms “ $c_i \cdot d_i$ ” corresponding to each of these 6 decay laws are: 0.001, 0.00056, 0.00013, 0.00011, 0.00018, 0.00038 in arbitrary units. The c-constants depend on width of the oxide layer and on trap concentration for that layer. More exactly, it depends on chemical Si–Si bound-system concentration within oxide and on any other oxide defect which might be turned into a hole trap.



**Fig. 5.23** AX250 measured core current during irradiation (left side) and the parametrized model function for the 6 oxide-trap populations model, with 6 decay parameters, the data used in parametrization correspond to a AX250 device irradiated with 3 Mrad TID, at a dose rate of 116 rad/s. The annealing curve after 26000 seconds varies from a fast 410 second decay time to an almost constant decay exponential slope for 300 days relaxation time.

To extrapolate the parametrization of core current from Legnaro experiment to the actual LHCb experiment it is needed to change the TID values from 3 Mrads to 1.4 Mrads (estimated value of the TID form LHCb 2<sup>nd</sup> Upgrade phase after 2031, with an LHC beam luminosity of 350 fb<sup>-1</sup>), and then to change dose rate  $d_{\text{Legnaro}}$  of 116 rad/s to  $d_{\text{LHCb}}$  value of 0.056 rad/s. The total effective/operation time of the 2<sup>nd</sup> Upgrade phase could be taken as 7000 hours or about  $25 \cdot 10^6$  s seconds. The number of effective charge in LHCb environment will vary with time over 7000 hours according to the following formula:

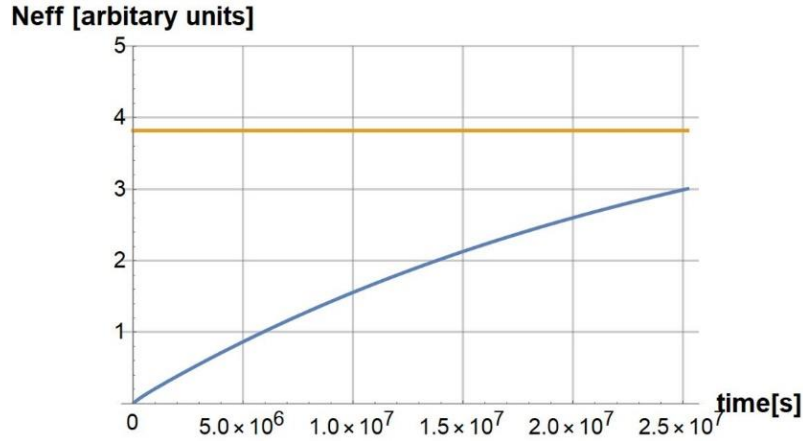
$$N_{\text{eff}} = \sum_{i=1}^6 c_i \cdot d_{\text{LHCb}} \cdot \tau_i \cdot [1 - \exp(-\frac{t}{\tau_i})] \quad (5.12)$$

which numerically is written as:

$$\begin{aligned} N_{\text{eff}} = & 48.2759 \cdot 10^{-5} \cdot \{ [0.41 \cdot (1 - e^{-2.43902 \cdot 10^{-3} \cdot t})] + [1.68 \cdot (1 - e^{-3.33333 \cdot 10^{-4} \cdot t})] + \\ & + [1.95 \cdot (1 - e^{-t/15000})] + [5.94 \cdot (1 - e^{-1.85185 \cdot 10^{-5} \cdot t})] + [57.6 \cdot (1 - e^{-3.125 \cdot 10^{-6} \cdot t})] + \\ & + [9994 \cdot (1 - e^{-3.80228 \cdot 10^{-8} \cdot t})] \} \end{aligned} \quad (5.13)$$

If the value of  $N_{\text{eff}}$  is smaller than the threshold value  $N_{\text{thr}}$  then the core current will remain unchanged to its base-line value of 15.4 mA in the measured device, as the parasitic transistor will never be activated since the charge deposit at any time does not exceed the critical

threshold value. In fig. 5.24 it is plotted the estimated value of  $N_{eff}$  over 2<sup>nd</sup> phase LHCb Upgrade, versus the constant threshold value. It can be noticed that at no moment the effective charge approaches the threshold value, hence the device will exhibit none of the TID cumulative effects with current rise. For values of TID much higher than LHCb TID values it could be expected a maximum of 6 % increase in core current above a value of 10 Mrad TID. Compare the last value with the 1.4 - 1.6 Mrad TID expected over the full LHCb lifetime, 2010 to beyond 2035. Though it is expected large errors on the fit value quoted in this section, by taking into account the hard-constraints on the real TID parameters it should be expected the conclusion (constant device current over LHCb lifetime) is accurate for LHCb experiment and LHCb environment during all Upgrade phases.



**Fig. 5.24** The  $N_{eff}$  increase (with blue) for 0.056 rad/s and the  $N_{thr}$  (with dark-yellow) fixed value obtained from Legnaro data analysis on 3<sup>rd</sup> board measurements, for 7000 hours

## 5.5 Conclusions

The AX250 proved to have excellent radiation resilience against proton-induced SEUs, following the 24 MeV proton beam tests done at high fluence values of up to  $(2.5 \pm 0.5) \cdot 10^{13}$  protons/cm<sup>2</sup> in one sample. The basic TMR architecture had 100 % efficiency with no errors observed. However, 3 errors were observed with a more complex firmware architecture which was designed to be similar with the firmware version proposed to be used within the LHCb-RICH PDMDBs. These errors appeared only in the most extreme run at 1 krad/s dose rate, and could be at least partially due to temperature and TID cumulative effects which induce favorable conditions for SEE production. All 3 errors were recovered successfully.

The embedded RAM was observed to be very sensible to radiation-induced SEUs and an average value of the cross-section was measured to be  $(3.57 \pm 0.18) \cdot 10^{-14}$  cm<sup>2</sup>/bit. However, it seems to be by a factor of 20 higher when compared with the value measured for KINTEX-7 device with 35 MeV protons,  $(7.57 \pm 0.4) \cdot 10^{-15}$  cm<sup>2</sup>/bit.

In terms of TID, the DUT survived with no permanent operational failures up to a dose of  $(8 \pm 2)$  Mrad (Si) and for a very high dose rate of  $(1248 \pm 312)$  rad/s. High TID-induced increase of the leakage currents were observed, more visible with its core power rail, after a

TID of (640 +/- 128) krad (Si). The fast changes within the core power consumption are very dependent with the beam flux, as the annealing effects are visible immediately in absence of beam. The DUT seem to recover in matter of few weeks, except for a very long-lived component which account for about less than 10 % of maximum leakage current.

The DUT is an excellent choice be used in applications operating in radiation environments, however a few tradeoffs have to be taken into account regarding the DUT when designing the application:

- ❖ one time programmable;
- ❖ logic resource density is lower compared with latest generation devices;
- ❖ its power consumption is higher due to its older technology;
- ❖ additional circuitry may be needed when interfacing with very low voltage devices;

Assuming 7000 h of operation, the Axcelerator FPGA is suitable to be used within the PDMDBs during the **LHCb-RICH Upgrade Phase Ia**, as the expected TID is 200 krad (Si) and with a very low dose rate of 0.008 rad/s. Due to the very low dose rate, the TID effects will not be visible as the annealing effects are very strong. However, the tradeoff of its logic resource density and its power consumption as well as its antifuse CRAM have to be taken into account. The same applies when it is considered the expected radiation environment during the **LHCb-RICH Upgrade Phase Ib and II**, where the expected radiation levels are a factor of 10 higher.

# Chapter 6

## Conclusions and Original Contributions

Within this PhD thesis, the reliability of 3 complex integrated circuits, one ASIC and two FPGA technologies, was investigated in several radiation environments. The found operational parameters were extrapolated to their target applications. The results presented in this thesis had a high impact on choosing the KINTEX-7 FPGA as the main component within the LHCb-RICH PDMDBs, but with reduced firmware resource allocation from close to 20 % to much lower than 1 % of CRAM (actually close to 1 per-mile of CRAM being critical bit numbers in worst-case scenario). The gained expertise provided very useful information which helped the collaboration to improve its PDMDB design, by adding SEL and high-current SEU detection and mitigation tools. Moreover, the antifuse FPGA proved to be very resilient to radiation, making it an excellent candidate for the future upgrade programs in much harsher environments. In the next section a summary of the main conclusions are given for each tested integrated circuit.

### 6.1 Summary of Results

*The third chapter* is dedicated to the SPACIROC2 ASIC evaluation. The Spatial Photomultiplier Array Counting and Integrating Readout Chip (SPACIROC) family are front-end and radiation hard ASICs designed to meet the readout requirements for 64-channel photomultiplier tubes, e.g. MaPMTs. It has been intended as photodetector readout chip for the space-based JEM-EUSO cosmic ray observatory onboard at the ISS. The second generation of SPACIROC chip was a prototype to evaluate the performances of various internal blocks

before a final version. A set of irradiation tests was organized to establish the reliability of the SPACIROC2 in a radiation environment similar to the ISS environment or to a typical CERN accelerator experiment. The SEE rates and TID effects were measured by using particle beams like: ions, protons and X-Rays. To monitor its radiation response a custom experimental setup was proposed and designed in accordance with the various radiation testing standards as well as with the facility and its safety radiation constraints. Several radiation-induced failures were observed and the results were extrapolated to the JEM-EUSO and LHCb-RICH radiation environments. In conclusion, this integrated circuit may operate in such environment if proper safety measures are implemented within its target application at JEM-EUSO.

*The fourth chapter* presents a complex set of irradiation tests carried out on the Xilinx KINTEX-7 FPGA. This SRAM-based FPGA is a commercial-grade circuit and it was proposed for the digital readout within the LHCb-RICH program during upgrade Phase I. A comprehensive experimental setup, including a custom DAQ system, was designed to monitor this FPGA while is being exposed to radiation. Several firmware architectures, some of which included error mitigation techniques, were developed to test in radiation circuit-internal logic resources like: CRAM, BRAM, user FFs, and I/O blocks. Its radiation response was measured by using several particle beams such as: ions, protons, X-Rays, and a mixed field of radiation. The results were extrapolated to its main target application, and concluded with agreeing of using this FPGA within the LHCb-RICH application with the caveat that its CRAM is very sensible to radiation-induced SEUs, and thus, recommending a very sparse usage of CRAM at level of 1 per-mile, and, SEL or SEU-high-current error mitigation tools on the PDMDB RICH system to prevent system aging due to high current states.

*The fifth chapter* describes the irradiation campaign carried out on the Microsemi (now Microchip) Axcelerator FPGA device. This is an antifuse FPGA and it was proposed as a backup solution for the KINTEX-7 FPGA in the LHCb-RICH application. By using the past experience gained by testing the KINTEX-7 and the SPACIROC2/MAROC3 devices, a very fast and performant DAQ system was designed to ensure remote operation, besides data acquisition like: power management, monitoring and firmware control. As in case of the KINTEX-7 FPGA, several firmware versions were developed to test key resources like: BRAM, FFs and the IO blocks. The tests beam done with protons and X-Rays revealed an excellent radiation resilience of the FPGA, with very low error rates within its logic resources and configuration. Although, high TID-induced increases of the leakage currents were observed at very high and unrealistic dose rates, when extrapolated to the harshest LHCb-RICH environments this device will never show any of these effects. The RAM resources are prone to SEUs, though the memory corruption is easily mitigated in this FPGA due to configuration immunity which makes it possible to implement algorithms to check the data integrity. A possible LHCb-RICH application could also avoid altogether the usage of volatile resources.

Overall, with the aggressive downscaling of the technology, the observed TID effects were small within the 28 nm KINTEX-7 FPGA. In other technologies such as the 0.15  $\mu\text{m}$  antifuse FPGA as well as the 0.35  $\mu\text{m}$  BiCMOS SPACIROC2 ASIC the TID effects were more visible due to the effect of hole traps accumulation within the device insulator oxides.



## 6.2 Original Contributions

I am employed since August 2014 by Horia Hulubei National Institute for R&D in Physics and Nuclear Engineering (IFIN-HH) and since then I am an Associate Electronics Engineer and PhD student (with LHCb author rights due to specific contribution) to the LHCb collaboration at CERN respectively in the Romanian LHCb group. From the beginning I was directly involved in activities related to the upgrade program of the LHCb-RICH sub-detectors. During my PhD thesis I participated at various R&D activities focused on the development of hardware and software solutions related to the LHCb-RICH PDMDBs as well as to design test prototype systems to carry out quality assurance tests on the PDMDBs and their plugin modules.

Within the Romanian LHCb Group, besides the LHCb related activities, I was involved in various capacities in irradiation tests done for various integrated circuits, which were proposed to operate in radiation environments. Part of original contributions are repeated at each tested integrated circuit and consequently they are grouped in "General original contributions". Then, specific original contributions for each tested integrated circuit are presented.

### *General original contributions*

- ❖ Major contributions into establishing the irradiation testing strategy for each tested integrated circuit (e.g. irradiation setup proposal, irradiation strategy etc.);
- ❖ For each tested integrated circuit, a compressive irradiation setup was designed and implemented following strict rules in terms of radiation and facility constrains;
- ❖ Each irradiation setup was connected to dedicated LabVIEW GUIs; these GUIs were developed in this PhD thesis for each irradiation setup, allowing close monitoring and full control of the circuit under test as well as data saving for later analysis;
- ❖ Each irradiation setup, had a DAQ system that was controlled by either a micro-controller or an FPGA, hence besides the hardware design of each DAQ system, I wrote the firmware for each of them either in C or VHDL language;
- ❖ One key component within the irradiation setups was the power supply boards, which had to be tested in advance by simulating radiation-induced high current states. Therefore, custom active electronic loads were designed to establish the reliability of the power supplies before they were used in the irradiation tests; [A5, C4]
- ❖ Important contributions into proposing several testing methodologies to detect and measure various radiation-induced effects within the tested integrated circuits, and which were largely described in this PhD thesis; (e.g. latch-up detection, SEU detection and mitigation in all three circuits)
- ❖ Several contributions were brought to mitigate or to reduce the impact of radiation-induced effects within the tested integrated circuits; (e.g. the hybrid scrubber architecture to detect and correct SEUs within the CRAM for the KINTEX-7 FPGA and presented in section 4.3.1)
- ❖ Multiple software scripts were designed, mainly by using Python language and LabVIEW, to analyze the post irradiation data and to extract the cross-section values

for different experiments in order to explain the circuits behavior in a particular radiation environment.

Beside these, a lot of work was carried out at the irradiation facilities in terms of irradiation setup arrangement as well as data taking and full supervision of the circuit under test.

*Original contributions within the SPACIROC2 ASIC evaluation:*

- ❖ The symmetrical power supply board, the DAQ system and its associated LabVIEW GUI were designed in order to ensure individual power monitoring of the ASIC on both analog and digital cores as well as to monitor various internal signals; [A4]
- ❖ The DAQ system was configured to cope with the monitoring requirements via its LabVIEW GUI and the latter to save the data in ASCII files for later analysis;
- ❖ Full software integration was ensured in order to be able to communicate with the ASIC registers via the DAQ system to detect and correct the radiation-induced SEUs;
- ❖ After each irradiation, laborious data analysis was carried out based on the measured data, and the circuit behavior under ionizing irradiation was established and presented in section 4.4.

*Original contributions within the KINTEX-7 FPGA evaluation:*

- ❖ Several contributions were brought to the hardware part of the irradiation setup containing the FPGA test board, the power supply board and its associated DAQ system; [C3]
- ❖ The FPGA test board was designed in accordance with various radiation constraints with the FPGA as the only active component on the board, and in the same time it ensured a full functionality with minimum components;
- ❖ Several FPGA firmware architectures were proposed to test and mitigate radiation-induced failures within several critical resources of the KINTEX-7 FPGA under radiation exposure and the VHDL code for few of them can be seen in annex A1-A4; [C1]
- ❖ A complex power management and DAQ architecture of the LHCb-PDMDBs that embeds the KINTEX-7 FPGAs was proposed when were irradiated into the mixed field of radiation at the CHARM facility from CERN. The FPGAs were powered and monitored over about 50 meters of cables, via a custom DAQ system. Four DAQ systems were tied to individual LabVIEW GUIs in order to allow remote control and monitoring of the FPGA following the facility requirements in term of radiation constraints (details in section 4.4.4);
- ❖ Laborious data analysis was carried after each irradiation test beam in order to extract the error rates and to conclude the FPGA behavior under ionizing radiation exposure. (details in section 4.4)
- ❖ Several irradiation results were published and presented at various international conferences. [A1-A2, C1-C2]

*Original contributions specific to the Axcelerator FPGA evaluation:*

- ❖ The monitoring and testing strategy of the Axcelerator FPGA under radiation exposure was proposed;
- ❖ A new and more complex irradiation setup was designed (hardware and software contributions);
- ❖ Multiple boards were designed using Altium Designer that were required to ensure the functionality of the irradiation setup: FPGA test board, FPGA DAQ board, the communication plugin boards and the I/O plugin boards; (for schematic diagrams see annex A5-A7)
- ❖ Every board that was part of the irradiation setup was assembled completely manually as follows: 9 FPGA test boards, 3 DAQ boards, 5 communication boards and 12 I/O plugin boards;
- ❖ Several firmware architectures were proposed to test and mitigate radiation-induced failures within several critical resources of the Axcelerator FPGA and their VHDL code can be seen in annex A8-A10;
- ❖ Due to the fact that the antifuse FPGAs are one time programmable, careful simulation and testing of the firmware architectures on other FPGA platforms was carried out before programming the antifuse device;
- ❖ Compressive data analysis was performed based on the measured data during irradiation and the FPGA behavior under a specific source of radiation was extracted and presented in section 5.3.

To summarize, over 10 articles and conference proceedings related to this PhD thesis were published. More than 20 presentations were held at various international conferences and workshops, as well as within the LHCb collaboration. The complete list of communication and papers can be found in section 6.3.

A much more completed and upgraded version of the irradiation setup presented in section 5.1, is proposed to be patented. This new system is a scalable and dedicated system designed to carry out full monitoring and control of various integrated circuits when are exposed to ionizing radiation.

Finally, in close collaboration with Dr. Stephen Wotton and Dr. Philip Garsed from University of Cambridge I was involved in the implementation of a complex testing system to carry out the production testing and the quality assurance of the PDMDB plugin modules, DTM and TCM presented in section 1.5.3. I personally tested around 1500 of such modules and reported the results to the LHCb Collaboration. Some pictures during the mass testing process are available in annex A11.

## 6.3 List of Papers and Conference Participations

### 6.3.1 Published Papers Related to this PhD Thesis Topic

#### A. Published papers in ISI indexed journals with UPB affiliation

**A1. V. M. Placinta**, L. N. Cojocariu, and C. Ravariu, *Proton-induced radiation effects in the I/O blocks of an SRAM-based FPGA*, **Journal of Instrumentation**, vol. 14, no. 10, pp. T10001–T10001, Oct. 2019, WOS:000501798500001, IF = 1.452 (2019), Q3, ISSN: 1748-0221, doi: 10.1088/1748-0221/14/10/T10001.

**A2.** L. N. Cojocariu and **V. M. Placinta**, *Ion Beam Irradiation Effects in KINTEX-7 FPGA Resources*, **Romanian Journal of Physics**, vol. 61, no. 901, p. 10, IF = 1.197 (2018), Q3, ISSN: 1221-146X.

**A3.** M. K. Baszczyk,..., **V. M. Placinta**,.... et al., *Test of the photon detection system for the LHCb RICH Upgrade in a charged particle beam*, **Journal of Instrumentation**, vol. 12, no. 01, pp. P01012–P01012, Jan. 2017, WOS:000395769600012, IF 1.220 (2016), Q3, ISSN: 1748-0221, doi: 10.1088/1748-0221/12/01/P01012. (6 citations)

**A4. V. M. Placinta**, L. N. Cojocariu, and C. Ravariu, *Test Bench Design for Radiation Tolerance of Two ASICs*, **Romanian Journal of Physics**, vol. 62, no. 903, p. 12, 2017, WOS:00040577260012, IF = 1.758 (2016), Q2, ISSN: 1221-146X. (4 citations)

**A.5. V.-M. Placinta**, F. Babarada, C. Ravariu, and L. G. Alecu, *Digitally Controlled Electronic Load for Testing Power Supplies Reliability*, **Rev. Roum. Sci. Techn.–Électrotechn. et Énerg**, vol. 64, no. 2, pp. 131–136, 2019, IF = 0.76 (2019), Q4.

**A6.** C. Ravariu, D. E. Mihaiescu, A. Morosan and **V. M. Placinta**, *New steps for advancing the Nothing On Insulator Triode 3nm gap and preliminary expanded technology*, **Romanian Journal of Information Science and Technology**, vol. 23, no. 2, p. 13, 2020, WOS:000532321500002.

In the next papers (section B), a selection of 12 papers are given with the author names in alphabetical order. Given my status as a PhD student and with my thesis topic related to the LHCb upgrade program, I have been included in the LHCb collaboration author list, which gave me the opportunity to be co-author on more than 170 high-impact papers related to the LHCb physics program.

B. Selection of published papers in ISI journals related to the LHCb collaboration with IFIN-HH affiliation

- B1.** R. Aaij, C. A. Beteta, T. Ackernley,..., **V. Placinta**, et al., *First Observation of Excited  $\Omega_b^-$  States*, **Physics Review Letters**, 124, 082002, February 2020, IF = 8.385 (2019), Q1, doi: 10.1103/PhysRevLett.124.082002
- B2.** R. Aaij, C. A. Beteta, T. Ackernley,..., **V. Placinta**, et al., *Measurement of the  $B_c^-$  meson production fraction and asymmetry in 7 and 13 TeV pp collisions*, **Physical Review D**, 100, 112006, December 2019, IF = 4.833 (2019), Q1, doi: 10.1103/PhysRevD.100.112006
- B3.** R. Aaij, C. A. Beteta, T. Ackernley,..., **V. Placinta**, et al., *Measurement of Charged Hadron Production in Z-Tagged Jets in Proton-Proton Collisions at  $\sqrt{s} = 8$  TeV*, **Physics Review Letters**, 123, 232001, December 2019, IF = 8.385 (2019), Q1, doi: 10.1103/PhysRevLett.123.232001
- B4.** R. Aaij, C. A. Beteta, T. Ackernley,..., **V. Placinta**, et al., *Observation of CP Violation in Charm Decays*, **Physics Review Letters**, 122, 211803, 2019, IF = 8.385 (2019), Q1, doi: 10.1103/PhysRevLett.122.211803
- B5.** R. Aaij, C. A. Beteta, M. Adinolfi,..., **V. Placinta**, et al., *Search for beautiful tetraquarks in the  $Y(1S)\mu^+\mu^-$  invariant-mass spectrum*, **Journal of High Energy Physics**, 86, 2018, WOS:000447516300002, IF = 5.833 (2018), Q1, ISSN: 1029-8479, doi: 10.1007/JHEP10(2018)086
- B6.** R. Aaij, C. A. Beteta, M. Adinolfi,..., **V. Placinta**, et al., *Search for lepton-flavour-violating decays of Higgs-like bosons*, **European Physical Journal C**, 78, 12, December 2018, WOS:000453066200003, IF = 4.843 (2018), Q1, ISSN: 1434-6044, doi: 10.1140/epjc/s10052-018-6386-8
- B7.** R. Aaij, C. A. Beteta, M. Adinolfi,..., **V. Placinta**, et al., *Measurement of Antiproton Production in p-He Collisions at root S-NN=110 GeV*, **Physics Review Letters**, 121, 22, November 2018, WOS:000451582500005, IF = 8.385 (2018), Q1, ISSN: 0031-9007, doi: 10.1103/PhysRevLett.121.222001
- B8.** R. Aaij, C. A. Beteta, T. Ackernley,..., **V. Placinta**, et al., *Search for weakly decaying b-flavored pentaquarks*, **Physical Review D**, 97, 3, 032010, February 2018, WOS:000425304300001, IF = 4.368 (2018), Q1, ISSN: 2470-0010, doi: 10.1103/PhysRevD.97.032010
- B9.** R. Aaij, C. A. Beteta, T. Ackernley,..., **V. Placinta**, et al., *Search for Dark Photons Produced in 13 TeV pp Collisions*, **Physics Review Letters**, 120, 6, 061801, February 2020, WOS:000424507800010, IF = 9.227 (2018), Q1, ISSN: 0031-9007, doi: 10.1103/PhysRevLett.120.061801
- B10.** R. Aaij, B. Adeva, M. Adinolfi, ..., **V. Placinta**, et al., *Bose-Einstein correlations of same-sign charged pions in the forward region in pp collisions at root s=7 TeV*, **Journal**

**of High Energy Physics**, 12, 025, December 2017, WOS:000417757900003, IF = 5.541 (2017), Q1, ISSN: 1029-8479, doi: 10.1007/Jhep12(2017)025.

**B11.** R. Aaij, B. Adeva, M. Adinolfi, ..., **V. Placinta**, et al., *Search for lepton-flavour-violating decays of Higgs-like bosons*, **European Physical Journal C**, 77, 12, 812, November 2017, WOS:000417101000002, IF = 5.172 (2017), Q1, ISSN: 1434-6044, doi: 10.1140/epjc/s10052-017-5178-x

**B12.** R. Aaij, B. Adeva, M. Adinolfi, ..., **V. Placinta**, et al., *Measurement of the  $J/\psi$  pair production cross-section in  $pp$  collisions at  $\sqrt{s} = 13$  TeV*, **Journal of High Energy Physics**, 10, 068, October 2017, WOS:000412907800015, IF = 5.541 (2017), Q1, ISSN: 1029-8479, doi: 10.1007/Jhep10(2017)068.

C. Published papers in conference proceedings indexed in ISI or IEEE with UPB affiliation

**C1. V.-M. Placinta** and L. N. Cojocariu, *Radiation Hardness Studies and Evaluation of SRAM-Based FPGAs for High Energy Physics Experiments*, in **Proceedings of Topical Workshop on Electronics for Particle Physics - PoS(TWEPP-17)**, Santa Cruz, California, Mar. 2018, p. 085, doi: 10.22323/1.313.0085.

**C2. V. M. Placinta**, L. N. Cojocariu, and C. Ravariu, *I/O Blocks Reliability for an SRAM-Based FPGA When Exposed to Ionizing Radiation*, in **Proceedings of 2018 International Semiconductor Conference (CAS)**, Sinaia Romania, Oct. 2018, WOS:000514386700038, ISBN: 978-1-5386-4482-9, doi: 10.1109/SMICND.2018.8539743

**C3.** L. N. Cojocariu, **V. M. Placinta**, and L. Dumitru, *Monitoring system for testing the radiation hardness of a KINTEX-7 FPGA*, in **Proceedings of 9TH INTERNATIONAL PHYSICS CONFERENCE OF THE BALKAN PHYSICAL UNION (BPU-9)**, Istanbul, Turkey, 2016, p. 140009, doi: 10.1063/1.4944199.

**C4. V. M. Placinta**, L. N. Cojocariu, and C. Ravariu, *Evaluating the switching mode power supplies used in radiation hardness tests of integrated circuits*, in **Proceedings of 2017 International Semiconductor Conference (CAS)**, Sinaia, Oct. 2017, pp. 305–308, WOS:000425844500068, ISBN: 978-1-5090-3985-2, doi: 10.1109/SMICND.2017.8101232.

**C5.** M. Serbanescu, **V. M. Placinta**, O. E. Hutanu, and C. Ravariu, *Smart, low power, wearable multi-sensor data acquisition system for environmental monitoring*, in **Proceedings of 2017 10th International Symposium on Advanced Topics in Electrical Engineering (ATEE)**, Bucharest, Romania, 2017, pp. 118–123, WOS:000403399400024, ISBN: 978-1-50-0-5160-1, doi: 10.1109/ATEE.2017.7905059.

**C6.** C. Ravariu, C. Parvulescu, and **V. M. Placinta**, *Technology and Optimizations for the NOI-Nano-Triode*, in **Proceedings of 2019 International Semiconductor Conference (CAS)**, Sinaia, Romania, Oct. 2019, pp. 75–78, WOS:000514295300014, ISBN:978-1-7281-1888-8, doi: 10.1109/SMICND.2019.8923917.

*List of scientific research reports:*

- 1. Introduction Nuclear Engineering and the R&D within CERN High Energy Experiments**
- 2. Radiation-Induced Failure within the Semiconductor Electronics Devices**
- 3. Test Bench Design for Radiation Tolerance of Two ASICs**
- 4. Radiation Hardness Studies and Evaluation of SRAM-Based FPGAs for High Energy Physics Experiments**
- 5. Data Analysis and Investigation of Proton Induced Radiation Effects in 0.15  $\mu\text{m}$  CMOS Antifuse FPGA**

Without the financial support from Romanian funding agencies supporting the materials and expenses of this work I would not been able to complete these studies and popularize the result and gain the necessary experience. Hence, I am grateful to Ministry of National Education and Research and Institute of Atomic Physics (IFA) for providing the funding under the following grants:

- ❖ IDEI PN-II-ID-PCE-2011-3-0749 (2012 - 2016);
- ❖ contract/project IFA "Capacitati" LHCb 3/3.12.2012 (2012 - 2015);
- ❖ IFA projects and contracts PN-III 5.2 Romania-CERN LHCb 7/16.03.2016 (2016 - 2019) and LHCb 9/16.03.2020 (2020 - 2021);
- ❖ PN-III-P4-IDPCE-2016-0480 (2017 - 2019);
- ❖ national project “Nucleu” PN 19 06 01 04 (2019 - 2021), as well as other institutional IFIN-HH projects.

### **6.3.2 Presentations Held at International Conferences, Workshops, Symposiums and within the LHCb Collaboration at CERN**

- 1. V. M. Placinta**, L. N. Cojocariu and Florin Maciuc, *Radiation Hardness Tests Done on KINTEX-7 FPGA for High Energy Physics Experiments*, **Topical Workshop on Electronics for Particle Physics 2019**, University of Santiago de Compostela, Santiago de Compostela, Spain, September 2<sup>nd</sup> – 6<sup>th</sup> 2019, available at: [TWEPP 2019](#) (poster)



2. **V. M. Placinta**, L. N. Cojocariu and Florin Maciuc, *Radiation Hardness Tests Done on KINTEX-7 FPGA for High Energy Physics Experiments*, **19th International Balkan Workshop on Applied Physics and Materials Science (IBWAP 2019)**, University of Santiago de Compostela, Ovidius University of Constanta, Constanta, Romania, July 16<sup>th</sup> – 19<sup>th</sup> 2019. available at: [link](#) (poster)
3. **V. M. Placinta**, L. N. Cojocariu and Florin Maciuc, *Investigation of Proton-Induced Radiation Effects in 0.15  $\mu\text{m}$  Antifuse FPGA*, **Topical Workshop on Electronics for Particle Physics 2018**, KU Leuven, Antwerp, Belgium, September 17<sup>th</sup> – 24<sup>th</sup> 2018, available at: [TWEPP 2018](#) (presentation)
4. **V. M. Placinta**, L. N. Cojocariu, *Radiation Hardness of Field Programmable Gate Arrays in LHC Experiments*, **SAD -ETI symposium**, Bucharest, Romania, July 2018 (presentation + poster)
5. **V. M. Placinta**, L. N. Cojocariu, *Radiation Hardness of Field Programmable Gate Arrays in LHC Experiments*, **Third Barcelona Techno Week – Course on semiconductor detectors**, Barcelona, Spain, July 2017 (poster)
6. **V. M. Placinta** and L. N. Cojocariu, *Radiation Hardness Studies and Evaluation of SRAM-Based FPGAs for High Energy Physics Experiments*, **Topical Workshop on Electronics for Particle Physics 2017**, Santa Cruz Institute of Particle Physics (SCIPP), California, USA, September 11<sup>th</sup> – 14<sup>th</sup> 2017, available at: [TWEPP 2017](#) (presentation + conference proceeding)
7. **V. M. Placinta**, *First Results on KINTEX-7 FPGA testing in mixed field radiation at CHARM facility*, **Topical Workshop on Electronics for Particle Physics 2017**, Santa Cruz Institute of Particle Physics (SCIPP), California, USA, September 11<sup>th</sup> – 14<sup>th</sup> 2017, available at: [TWEPP 2017](#) (presentation)
8. **V. M. Placinta** and L. N. Cojocariu, *Test Bench Design for Evaluating the Performance of Multi-anode Photomultiplier Tubes*, **17th International Balkan Workshop on Applied Physics and Material Science**, Ovidius University of Constanta, Constanta, Romania, July 11<sup>th</sup> – 14<sup>th</sup> 2017. (presentation)
9. **V. M. Placinta** and L. N. Cojocariu, *Test Bench for ASIC radiation hardness evaluation*, **Workshop on Sensors and High Energy Physics (SHEP 2016)**, Stefan Cel Mare University of Suceava, Suceava, Romania, October 21<sup>st</sup> – 22<sup>nd</sup> 2016, available at: [SHEP 2016](#) (presentation)
10. **V. M. Placinta**, L. N. Cojocariu, et al, *Kintex-7 Irradiation, Test Bench and Results*, **Topical Workshop on Electronics for Particle Physics 2016**, Karlsruhe Institute of Technology (KIT), Karlsruhe, Germany, September 26<sup>th</sup> – 30<sup>th</sup> 2016, available at: [TWEPP 2016](#) (presentation)

11. **Vlad-Mihai Placinta** and Stephen Wotton, *PT1000 Temperature Readings Through GBT-SCA ADC Lines*, **General RICH Meeting**, 12<sup>th</sup> of November 2019, available at: [link](#) (private communication)
12. **Vlad-Mihai Placinta** and Stephen Wotton, *Update on SCA-ADC Temperature Readings and Calibration*, **RICH Upgrade – Integration and Commissioning**, 1<sup>st</sup> of November 2019, available at: [link](#) (private communication)
13. **Vlad-Mihai Placinta** and Stephen Wotton, *Update on SCA-ADC Temperature Calibration*, **RICH Upgrade – Integration and Commissioning**, 25<sup>th</sup> of October 2019, available at: [link](#) (private communication)
14. **Vlad-Mihai Placinta**, Floris Keizer and Stephen Wotton, *Temperature Reading through GBT-SCA ADC lines*, **RICH ECS meeting**, 10<sup>th</sup> of October 2019, available at: [link](#) (private communication)
15. **Vlad-Mihai PLACINTA**, *Summary of the PDMDB module testing*, **RICH upgrade PDMDB testing progress meeting**, 15<sup>th</sup> of March 2019, available at: [link](#) (private communication)
16. **Vlad-Mihai PLACINTA**, *Summary of Modules testing*, **RICH upgrade PDMDB testing progress meeting**, 7<sup>th</sup> of March 2019, available at: [link](#) (private communication)
17. **Vlad-Mihai PLACINTA**, *Antifuse FPGA Irradiation Setup*, **LHCb RICH Upgrade meeting**, 5<sup>th</sup> of June 2018, available at: [link](#) (private communication)
18. **Vlad-Mihai PLACINTA**, *Antifuse FPGA Irradiation Campaign Status*, **LHCb RICH Upgrade meeting**, 26<sup>th</sup> of February 2018, available at: [link](#) (private communication)
19. **Vlad-Mihai PLACINTA**, *Updates regarding the DAQ system proposed for PDMDB monitoring*, **LHCb RICH Upgrade mini-meeting**, 12<sup>th</sup> of April 2017, available at: [link](#) (private communication)
20. **Vlad-Mihai PLACINTA**, *First measurements of the I/O signals in KINTEX-7 FPGA in proton beam*, **Mini-meeting on irradiation for RICH Upgrade**, 24<sup>th</sup> of November 2017, available at: [link](#) (private communication)

### 6.3.4 Participation at International Schools and Courses

- ❖ *GRIDS 2019 – Graduate Instrumentation and Detector School*, organized by **TRIUMF facility within University of British Columbia**, June 10<sup>th</sup> – 21<sup>th</sup> 2019, Vancouver British Columbia, Canada. (website available at: [link](#))  
*Activities and disciplines*: DAQ electronics, FPGA workshops, interaction of radiation with matter, radiation detection, physical mechanisms for collecting energy deposited by radiation, low background detectors, scintillating detectors etc.
- ❖ *Third Barcelona Techno Week – Course on semiconductor detectors*, organized by **Institute of Cosmos Sciences within Barcelona University**, July 2<sup>nd</sup> – 6<sup>th</sup> 2018, Barcelona, Spain. (website available at: [link](#))  
*Activities and disciplines*: interaction of radiation with matter, semiconductor radiation detectors, CMOS technology, pulse processing electronics, sensor design and interconnects, application of radiation detectors, light detection in semiconductor devices etc.
- ❖ *SERESSA 2017 – The 13th International School on the Effects of Radiation on Embedded Systems for Space Applications*, organized by **Spectrum Aerospace with Technical University of Munich**, October 23<sup>rd</sup> - 26<sup>th</sup> 2017, Munich, Germany. (website available at: [link](#))  
*Activities and disciplines*: radiation environments, spacecraft anomalies, single-event effects (SEEs), total dose effects (TID), radiation effects in power systems, radiation effects in solar cells, architecture hardening in analog and digital circuits and in memories, software hardening in FPGAs, radiation testing and laser testing and remote testing experiments.
- ❖ *ESIPAP 2017 – European School of Instrumentation in Particle & Astroparticle Physics*, organized by **European Scientific Institute (ESI)**, February 20<sup>th</sup> to March 17<sup>th</sup> 2017, Archamps, France. (website available at: [link](#))  
*Activities and disciplines*: detector technologies, signal processing and electronics, gravitation wave detection, data handling technologies, trigger and data acquisition, and ultracold neutrons production and detection.
- ❖ *ISOTDAQ 2016 – International School of Trigger & Data Acquisition*, organized by **Weizman Institute of Science**, January 24<sup>th</sup> to February 2<sup>nd</sup> 2016, Rehovot – Tel Aviv, Israel. (website available at: [link](#))  
*Activities and disciplines*: introduction to detector readout, introduction to data acquisition, introduction to trigger, DAQ hardware, microcontrollers, trigger hardware, LabVIEW, modular electronics, waveform digitizing and signal processing, introduction to FPGAs, advanced FPGA programming, design and implementation of

a monitoring system, and introduction to the design of full-custom front-end & data transmission ASICs.

## 6.4 Future Perspectives

During my PhD program, I have gained a massive experience in developing high performance FPGA-based DAQ systems intended to power, control and to read out complex integrated circuits in radiation environments. The enormous knowledge involving the interaction of radiation with matter, more directed to semiconductor electronic devices, have proved to be very useful into preparation of complex systems operating in a harsh environments with radiation background.

Starting with 2021, the LHCb detector will be able to take collision data at a full LHC bunching rate of 40 MHz by using a novel hardware architecture combined with a full software trigger. The newly LHCb detector is scheduled to run for about 4 years on which is expecting to reach to more than  $25 \text{ fb}^{-1}$  integrated luminosity. Our group already proved its excellent knowledge into electronics, as I was involved in detector assembly, testing and commissioning of various RICH assemblies at CERN as well as in hardware design and evaluation during the R & D period. Therefore, I will continue to get involved in data taking shifts as well as maintenance tasks once the LHCb detector is up and running.

On the other hand, the discussions for the next upgrade phase planned after 2025 has enabled us to get involved into preparation of the radiation testing as well as in hardware design of various boards required during the next upgrade, phase Ib. As the radiation environment is expected to be at least 10 times harsher than its previous upgrade, the KINTeX-7 FPGA in its current configuration cannot operate. Therefore, alternatives to this FPGA have to be searched and evaluated for the new radiation environment. The Antifuse FPGA has excellent radiation resilience and it may work in the new radiation environment. However, its old technology attracts many drawbacks in terms of its performances which are very hard to accept.

I will continue the radiation testing program for new high density and high performance FPGAs, as well as other ASICs and integrated circuits proposed to operate in harsh environments with radiation background such as the space and the accelerator experiments.



# Annexes

## A.1 VHDL Code for Single Chain of FF Architecture (KINTEX-7 FPGA)

```
-- Company: IFIN-HH
-- Engineer: VLAD MIHAI PLACINTA
--
-- Create Date: 02/08/2017 02:36:15 AM
-- Design Name:
-- Module Name: top_single_chain - Behavioral
-- Project Name: Single chain FF
-- Target Devices: XC7K70T-FBG484
-- Tool Versions: Vivado
-----

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity top_single_chain is

    Port (
        clk_sys : in STD_LOGIC;
        data_input: in STD_LOGIC;
        data_output: out STD_LOGIC);

end top_single_chain;

architecture Behavioral of top_single_chain is

    component cell is
        generic ( fd_cells: integer:= 5498); --7% occupancy FF
        port (
            clk_tmr: in STD_LOGIC;
            data_in: in STD_LOGIC;
            data_out: out STD_LOGIC
        );
    end component;

begin

    main_cell: cell
    port map(
        clk_tmr => clk_sys,
        data_in => data_input,
        data_out => data_output);

end Behavioral;
```

-----CELL COMPONENT-----

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity cell is
  generic ( fd_cells: integer:= 5498); -- for 6.71% occupancy

  Port ( data_in : in STD_LOGIC;
        clk_tmr : in STD_LOGIC;
        data_out : out STD_LOGIC);
end cell;

architecture Behavioral of cell is
  signal link: STD_LOGIC_VECTOR(fd_cells downto 0);

  component FD_cell is
    Port ( C : in STD_LOGIC;
          D : in STD_LOGIC;
          Q : out STD_LOGIC);
  end component;

  begin

  start:FD_cell
  port map ( C=>clk_tmr,
            D=>data_in,
            Q=>link(0));

  eend:FD_cell
  port map ( C=>clk_tmr,
            D=>link(fd_cells),
            Q=>data_out);

  basic:
  for i in 1 to fd_cells generate
  begin
  basic_m:FD_cell
  port map ( C=>clk_tmr,
            D=>link(i-1),
            Q=>link(i));
  end generate basic;

  end Behavioral;
```

-----FD\_CELL COMPONENT-----

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
Library UNISIM;
use UNISIM.vcomponents.all;

entity FD_cell is
  Port ( C : in STD_LOGIC;
        D : in STD_LOGIC;
        Q : out STD_LOGIC);
end FD_cell;
```



```

architecture Behavioral of FD_cell is
signal Q1 : STD_LOGIC;

begin
--D-type Xilinx FF primitive
FDRE_1: FDRE
generic map (
INIT => '0') -- Initial value of register ('0' or '1')
port map (
Q => Q, -- Data output
C => C, -- Clock input
CE => '1', -- Clock enable input
R => '0', -- Synchronous reset input
D => D -- Data input
);

end Behavioral;

```

## A.2 VHDL Code for FF Level TMR Architecture (KINTEX-7 FPGA)

```
-- Company: IFIN-HH
-- Engineer: VLAD MIHAI PLACINTA
-- Create Date: 02/08/2017 02:36:15 AM
-- Module Name: tmr_cell - Behavioral
-- Project Name: TMR Cell Level
-- Target Devices: XC7K70T-FBG484
-- Tool Versions: Vivado

-----

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity tmr_cell is
    generic ( fd_cells: integer:= 5333); --8000 for 30% occupancy/ 5333 for 20%

    Port ( data_in : in STD_LOGIC;
          clk_tmr : in STD_LOGIC;
          data_out : out STD_LOGIC);
end tmr_cell;

architecture Behavioral of tmr_cell is
    signal link: STD_LOGIC_VECTOR(fd_cells downto 0);

    component FD_cell is
        Port ( C : in STD_LOGIC;
              D : in STD_LOGIC;
              Q : out STD_LOGIC);
    end component;

    begin

    start:FD_cell
    port map ( C=>clk_tmr,
              D=>data_in,
              Q=>link(0));

    eend:FD_cell
    port map ( C=>clk_tmr,
              D=>link(fd_cells),
              Q=>data_out);

    basic:
    for i in 1 to fd_cells generate
    begin
    basic_m:FD_cell
    port map ( C=>clk_tmr,
              D=>link(i-1),
              Q=>link(i));
    end generate basic;
end generate basic;
```

```

end Behavioral;
-----TMR FD_CELL COMPONENT-----
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
Library UNISIM;
use UNISIM.vcomponents.all;

entity FD_cell is
    Port ( C : in STD_LOGIC;
          D : in STD_LOGIC;
          Q : out STD_LOGIC);
end FD_cell;

architecture Behavioral of FD_cell is
    signal Q1, Q2, Q3 : STD_LOGIC;

begin
    FDRE_1: FDRE
    generic map (
        INIT => '0') -- Initial value of register ('0' or '1')
    port map (
        Q => Q1, -- Data output
        C => C, -- Clock input
        CE => '1', -- Clock enable input
        R => '0', -- Synchronous reset input
        D => D -- Data input);

    FDRE_2: FDRE
    generic map (
        INIT => '0') -- Initial value of register ('0' or '1')
    port map (
        Q => Q2, -- Data output
        C => C, -- Clock input
        CE => '1', -- Clock enable input
        R => '0', -- Synchronous reset input
        D => D -- Data input);

    FDRE_3: FDRE
    generic map (
        INIT => '0') -- Initial value of register ('0' or '1')
    port map (
        Q => Q3, -- Data output
        C => C, -- Clock input
        CE => '1', -- Clock enable input
        R => '0', -- Synchronous reset input
        D => D -- Data input);

    Q <= (Q1 AND Q2) OR (Q2 AND Q3) OR (Q1 AND Q3);    -- TMR Voter

end Behavioral;

```

## A.3 VHDL Code for Extended Cell Level TMR Architecture (KINTEX-7 FPGA)

```
-- Company: IFIN-HH
-- Engineer: VLAD MIHAI PLACINTA
-- Create Date: 02/08/2017 02:36:15 AM
-- Module Name: extended_tmr_cell - Behavioral
-- Project Name: Extended TMR Cell Level
-- Target Devices: XC7K70T-FBG484
-- Tool Versions: Vivado

-----

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity extended_tmr_cell is

    Port ( clk_sys : in STD_LOGIC;
          data_input: in STD_LOGIC;
          data_output: out STD_LOGIC);
end extended_tmr_cell;

architecture Behavioral of extended_tmr_cell is

    component tmr_cell is
        generic ( fd_cells: integer:= 1800); --8000 for 30% occupancy --5500 for 60% --1800 for 20%
        port (
            clk_tmr: in STD_LOGIC;
            data_in: in STD_LOGIC;
            data_out: out STD_LOGIC
        );
    end component;

begin

    main_tmr_cell: tmr_cell
    port map(
        clk_tmr => clk_sys,
        data_in => data_input,
        data_out => data_output);

end Behavioral;

-----TMR_CELL COMPONENT-----

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity tmr_cell is
    generic ( fd_cells: integer:= 1800);

    Port ( data_in : in STD_LOGIC;
          clk_tmr : in STD_LOGIC;
          data_out : out STD_LOGIC);
end tmr_cell;
```

```

architecture Behavioral of tmr_cell is
signal link_chain1: STD_LOGIC_VECTOR(fd_cells downto 0);
signal link_chain2: STD_LOGIC_VECTOR(fd_cells downto 0);
signal link_chain3: STD_LOGIC_VECTOR(fd_cells downto 0);

component FD_cell is
  Port ( C : in STD_LOGIC;
        D : in STD_LOGIC;
        Q : out STD_LOGIC);
end component;

begin

chain1:          --chain 1 instantiation
for i in 1 to fd_cells generate
begin
basic_m:FD_cell
port map ( C=>clk_tmr,
          D=>link_chain1(i-1),
          Q=>link_chain1(i));
end generate chain1;

chain2:          --chain 2 instantiation
for i in 1 to fd_cells generate
begin
basic_m:FD_cell
port map ( C=>clk_tmr,
          D=>link_chain2(i-1),
          Q=>link_chain2(i));
end generate chain2;

chain3:          --chain 3 instantiation
for i in 1 to fd_cells generate
begin
basic_m:FD_cell
port map ( C=>clk_tmr,
          D=>link_chain3(i-1),
          Q=>link_chain3(i));
end generate chain3;

data_out <= (link_chain1(fd_cells) AND link_chain2(fd_cells)) OR (link_chain2(fd_cells) AND
link_chain3(fd_cells)) OR (link_chain1(fd_cells) AND link_chain3(fd_cells)); -- TMR Voter
link_chain1(0)<= data_in;
link_chain2(0)<= data_in;
link_chain3(0)<= data_in;
end Behavioral;
----- TMR FD_CELL COMPONENT-----

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
Library UNISIM;
use UNISIM.vcomponents.all;

entity FD_cell is
  Port ( C : in STD_LOGIC;
        D : in STD_LOGIC;
        Q : out STD_LOGIC);
end FD_cell;

architecture Behavioral of FD_cell is

```

```

signal Q1, Q2, Q3 : STD_LOGIC;

begin
  FDRE_1: FDRE
  generic map (
    INIT => '0') -- Initial value of register ('0' or '1')
  port map (
    Q => Q1, -- Data output
    C => C, -- Clock input
    CE => '1', -- Clock enable input
    R => '0', -- Synchronous reset input
    D => D -- Data input);

  FDRE_2: FDRE
  generic map (
    INIT => '0') -- Initial value of register ('0' or '1')
  port map (
    Q => Q2, -- Data output
    C => C, -- Clock input
    CE => '1', -- Clock enable input
    R => '0', -- Synchronous reset input
    D => D -- Data input);

  FDRE_3: FDRE
  generic map (
    INIT => '0') -- Initial value of register ('0' or '1')
  port map (
    Q => Q3, -- Data output
    C => C, -- Clock input
    CE => '1', -- Clock enable input
    R => '0', -- Synchronous reset input
    D => D -- Data input);

  Q <= (Q1 AND Q2) OR (Q2 AND Q3) OR (Q1 AND Q3); -- TMR Voter

end Behavioral;

```

## A.4 VHDL Code for I/O block Ring Oscillator Architecture (KINTEX-7 FPGA)

```
-- Company: IFIN-HH
-- Engineer: VLAD MIHAI PLACINTA
-- Create Date: 02/08/2017 02:36:15 AM
-- Module Name: ring_osc - Behavioral
-- Project Name: IO RING OSCILLATOR
-- Target Devices: XC7K70T-FBG484
-- Tool Versions: Vivado
-----
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
library unisim; -- for xilinx IOBUF
use unisim.vcomponents.all;
use ieee.std_logic_signed.all;

entity ring_osc is
    --number of each pins and number IOBUF instantiation
    generic ( n_13 : integer:=49;
              n_1516: integer:=84;
              n_33 : integer:=48;
              n_34 : integer:=17 );
    port (
        pins13 : inout std_logic_vector (0 to n_13);      --hardware pins for bank 13
        pins1516 : inout std_logic_vector (0 to n_1516); --hardware pins for banks 15 & 16
        pins33 : inout std_logic_vector (0 to n_33);      --hardware pins for bank33
        pins34 : inout std_logic_vector (0 to n_34));      --hardware pins for bank34
end entity ring_osc;

architecture io_ring of ring_osc is
    --bank 13 signals
    signal data_in13 : std_logic_vector (0 to n_13+10);
    signal data_in1516 : std_logic_vector (0 to n_1516+10);
    signal data_in33 : std_logic_vector (0 to n_33+10);
    signal data_in34 : std_logic_vector (0 to n_34+10);

    component inverter is
        Port ( data_in : in STD_LOGIC;
              data_out : out STD_LOGIC);
    end component;

begin

    --bank13 i/o buff instantiation
    start_IOBUF_Inst_13: IOBUF generic map ( DRIVE => 12, IOSTANDARD => "DEFAULT", SLEW =>
    "SLOW") port map ( O => data_in13(1), IO => pins13(n_13), I => data_in13(n_13+2), T => '0');

    IOBUF_bank13_1:
    for i in 0 to n_13-1 generate --nr total-2
    begin
        IOBUFi_inst : IOBUF
        generic map ( DRIVE => 12, IOSTANDARD => "DEFAULT", SLEW => "SLOW")
```



```

port map ( O => data_in13(i+2), IO => pins13(i), I => data_in13(i+1), T => '0');
end generate IOBUF_bank13_1;
inverter13_1: inverter port map ( data_out=> data_in13(n_13+2), data_in=> data_in13(n_13+1));

--bank15&16 i/o buff instantiation
start_IOBUF_Inst_1516: IOBUF generic map ( DRIVE => 12, IOSTANDARD => "DEFAULT", SLEW =>
"SLOW") port map ( O => data_in1516(1), IO => pins1516(n_1516), I => data_in1516(n_1516+2), T => '0');

IOBUF_bank1516:
for i in 0 to n_1516-1 generate --nr total-2
begin
IOBUFi_inst : IOBUF
generic map ( DRIVE => 12, IOSTANDARD => "DEFAULT", SLEW => "SLOW")
port map ( O => data_in1516(i+2), IO => pins1516(i), I => data_in1516(i+1), T => '0');
end generate IOBUF_bank1516;
inverter1516: inverter port map ( data_out=> data_in1516(n_1516+2), data_in=> data_in1516(n_1516+1));

--bank33 i/o buff instantiation
start_IOBUF_Inst_33: IOBUF generic map ( DRIVE => 12, IOSTANDARD => "DEFAULT", SLEW =>
"SLOW") port map ( O => data_in33(1), IO => pins33(n_33), I => data_in33(n_33+2), T => '0');

IOBUF_bank33:
for i in 0 to n_33-1 generate --nr total-2
begin
IOBUFi_inst : IOBUF
generic map ( DRIVE => 12, IOSTANDARD => "DEFAULT", SLEW => "SLOW")
port map ( O => data_in33(i+2), IO => pins33(i), I => data_in33(i+1), T => '0');
end generate IOBUF_bank33;
inverter33: inverter port map ( data_out=> data_in33(n_33+2), data_in=> data_in33(n_33+1));

--bank34 i/o buff instantiation
start_IOBUF_Inst_34: IOBUF generic map ( DRIVE => 12, IOSTANDARD => "DEFAULT", SLEW =>
"SLOW") port map ( O => data_in34(1), IO => pins34(n_34), I => data_in34(n_34+2), T => '0');

IOBUF_bank34:
for i in 0 to n_34-1 generate --nr total-2
begin
IOBUFi_inst : IOBUF
generic map ( DRIVE => 12, IOSTANDARD => "DEFAULT", SLEW => "SLOW")
port map ( O => data_in34(i+2), IO => pins34(i), I => data_in34(i+1), T => '0');
end generate IOBUF_bank34;
inverter34: inverter port map ( data_out=> data_in34(n_34+2), data_in=> data_in34(n_34+1));

end architecture io_ring;

-----INVERTER COMPONENT-----
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

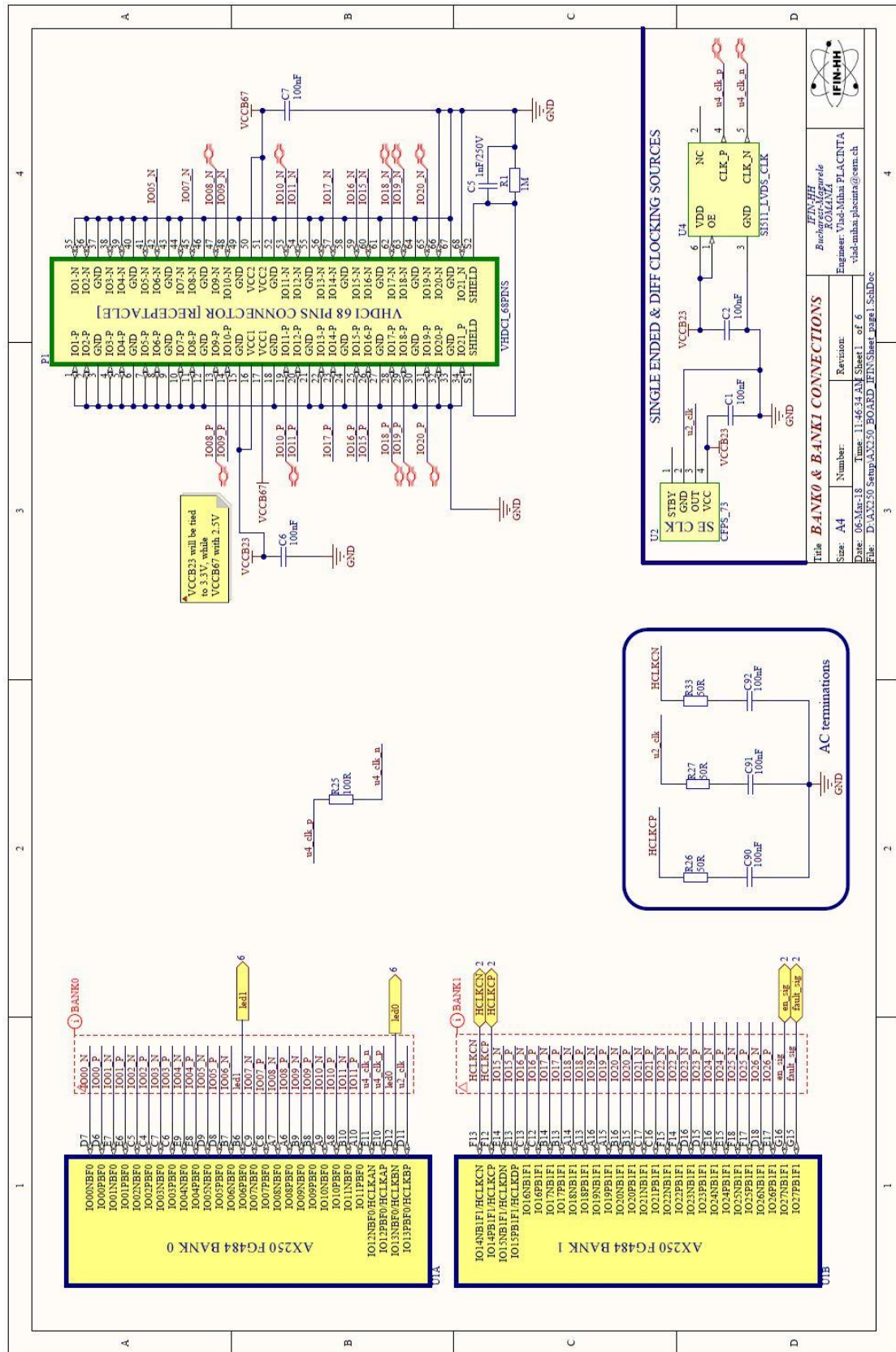
entity inverter is
    Port ( data_in : in STD_LOGIC;
          data_out : out STD_LOGIC);
end inverter;
architecture Behavioral of inverter is
begin

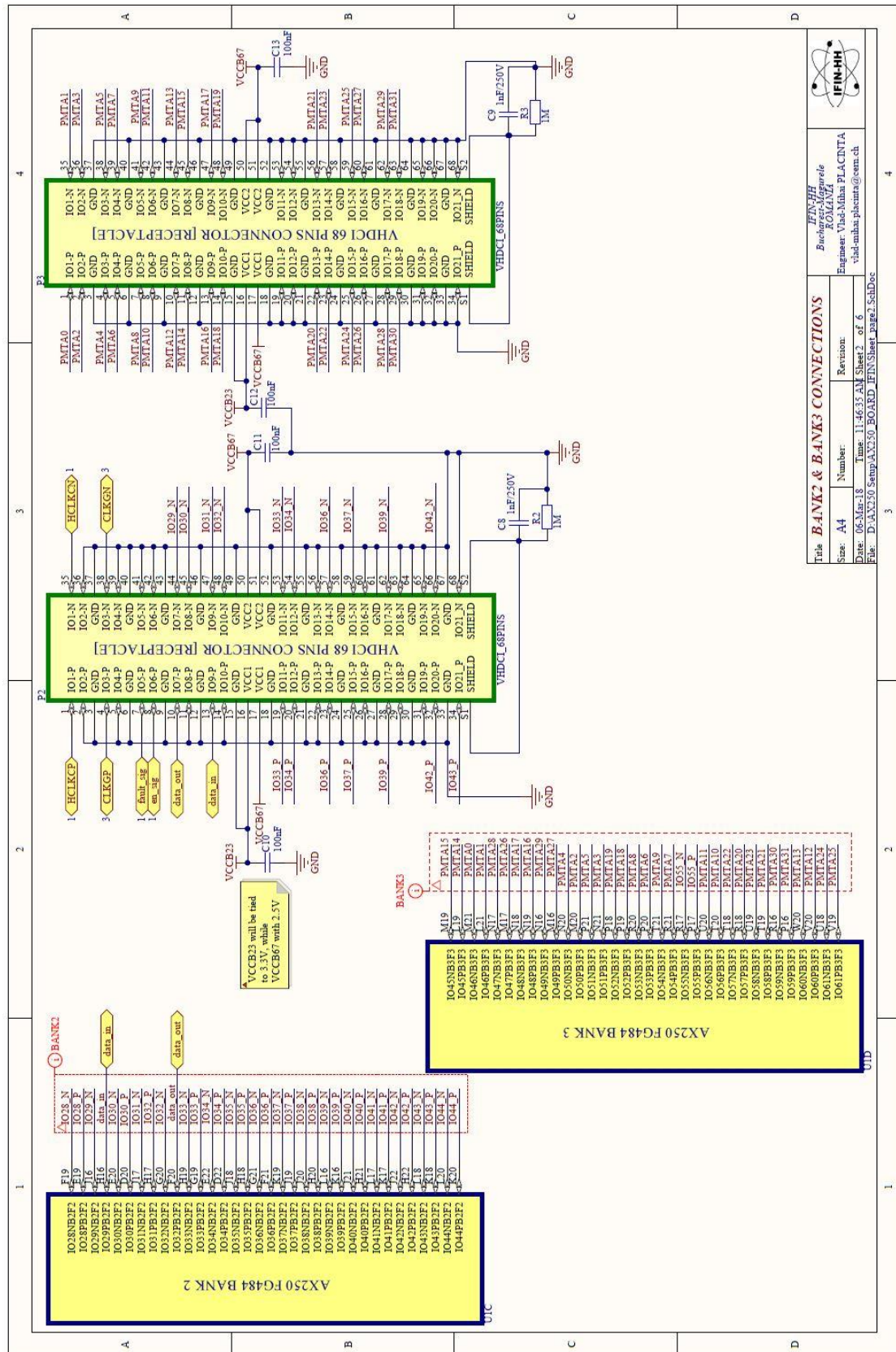
data_out<= NOT data_in;

end Behavioral;

```

## A.5 Schematic Diagram of the AX250 antifuse FPGA





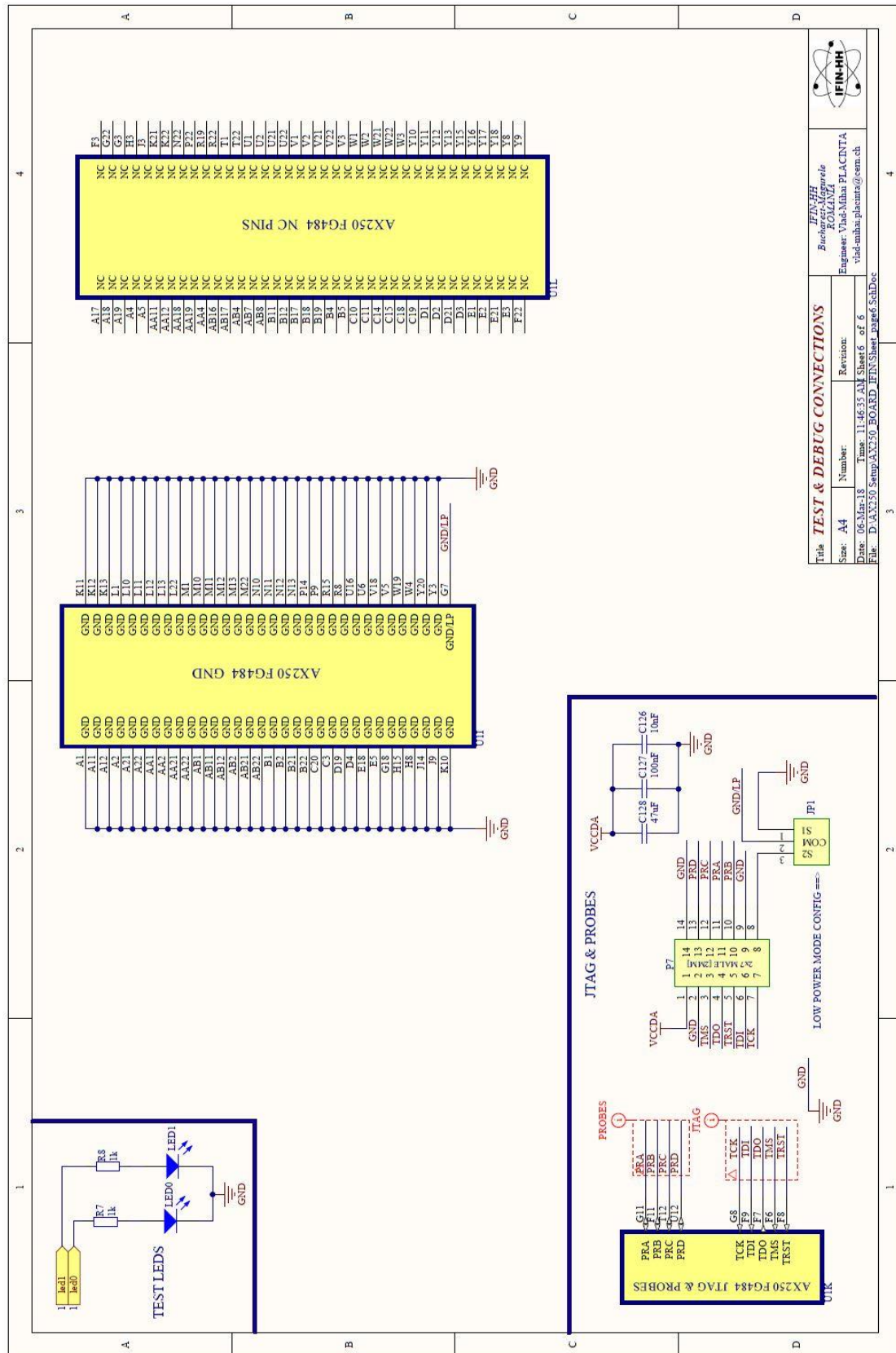






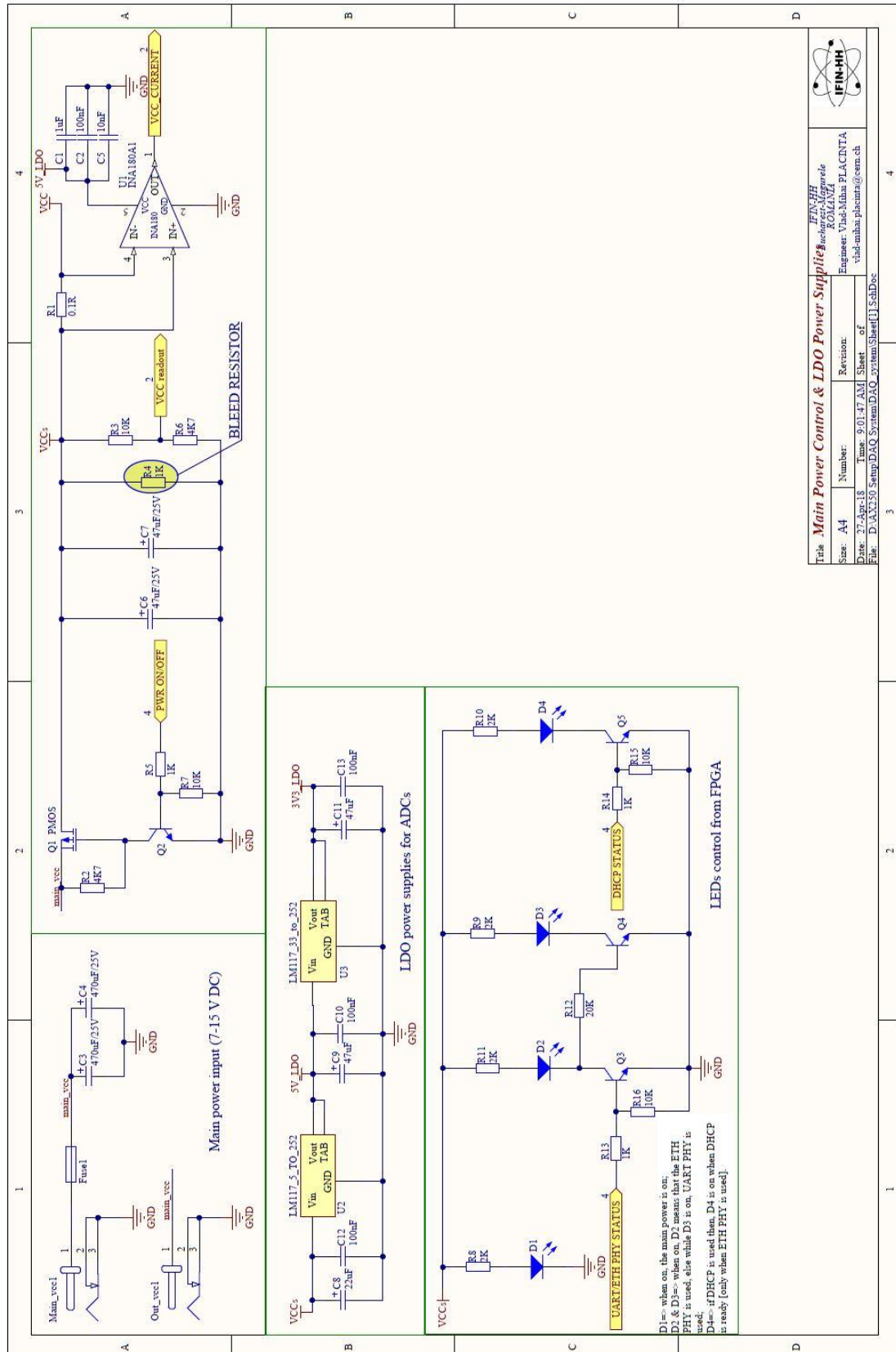


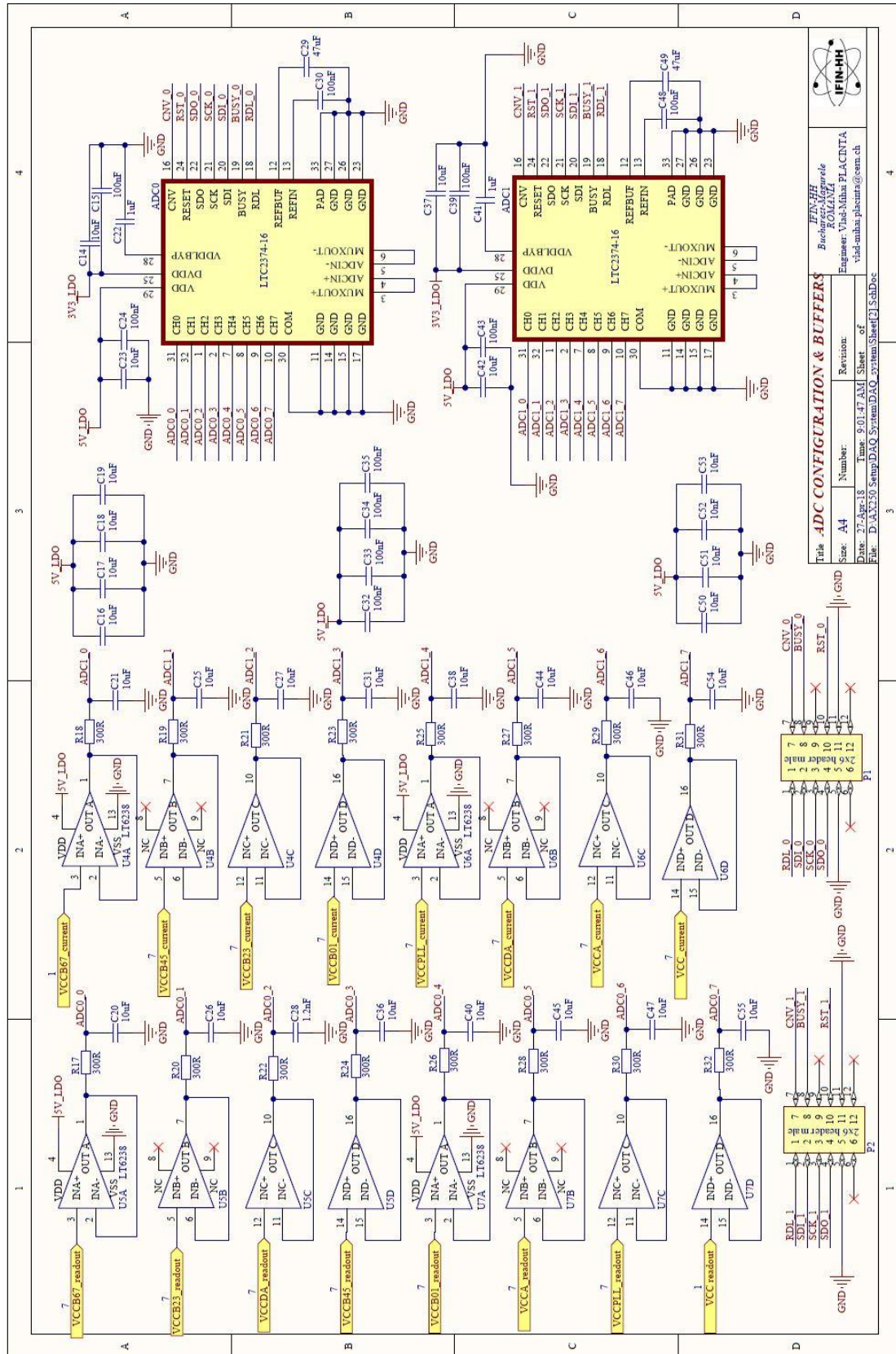


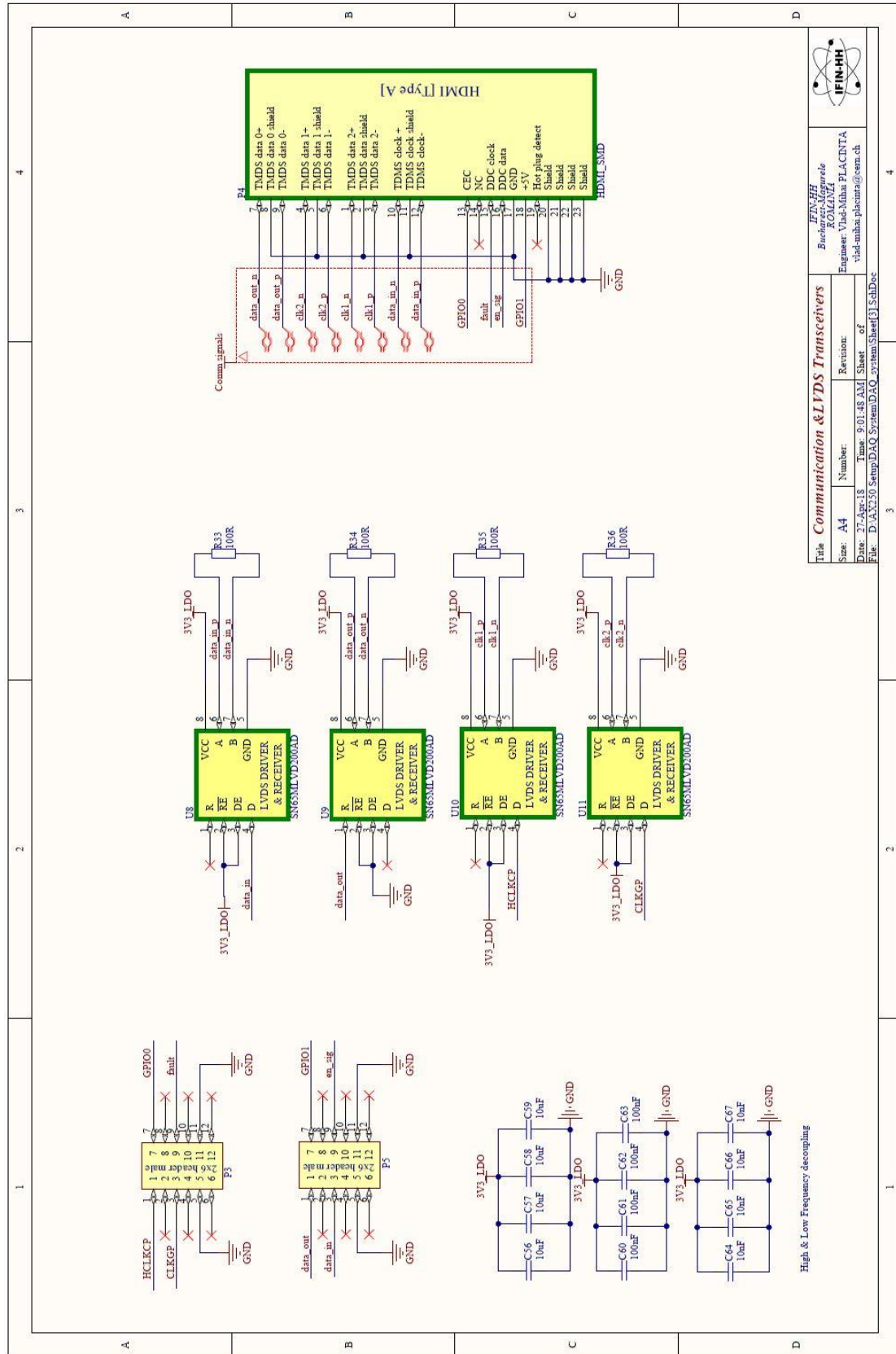




## A.6 Schematic Diagram of the DAQ System

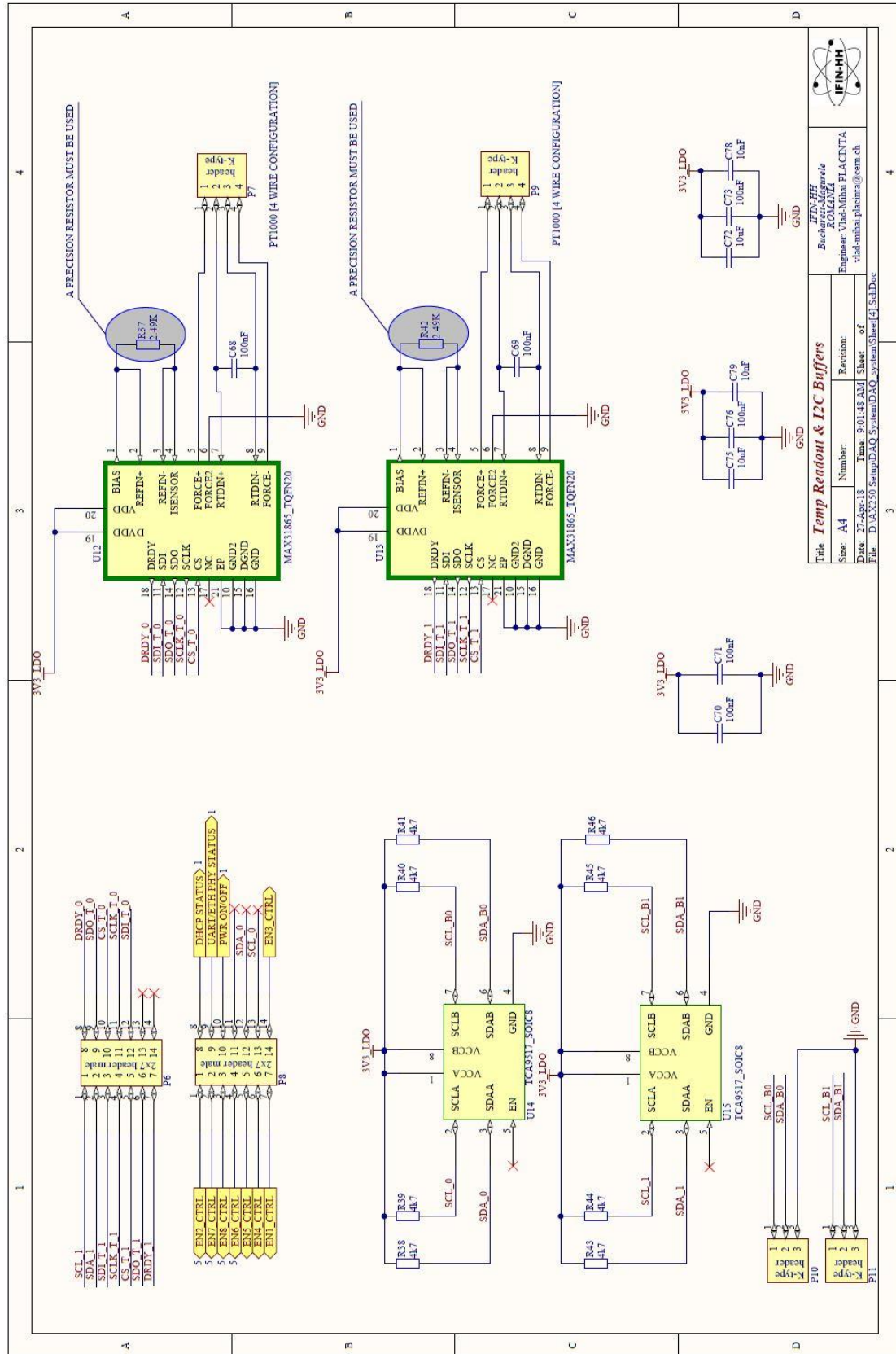






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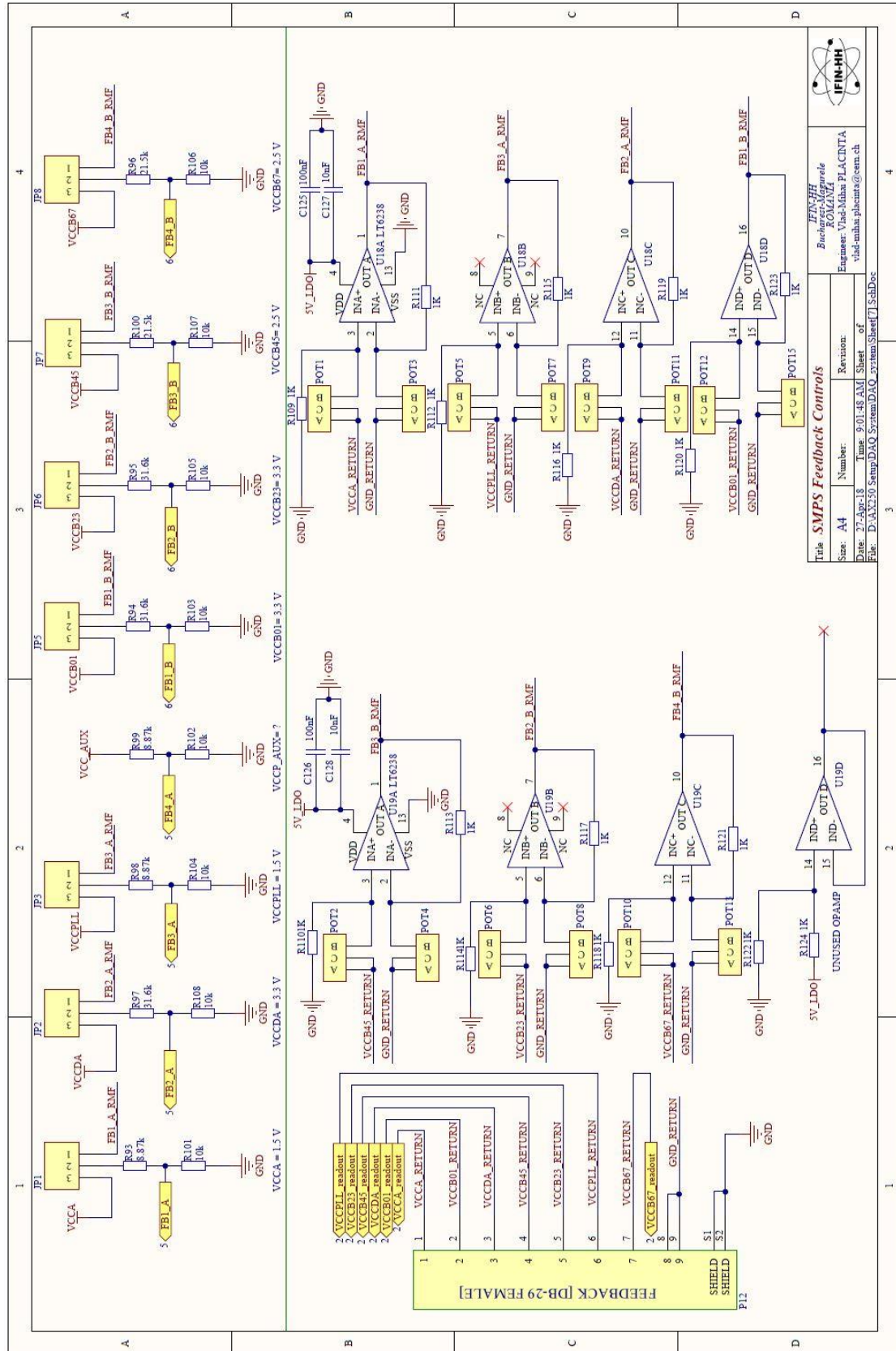
| Title: Communication & LVDS Transceivers |                  |                                                          |          |
|------------------------------------------|------------------|----------------------------------------------------------|----------|
| Size: A4                                 | Number:          | Revision:                                                | Sheet of |
| Date: 27-Apr-18                          | Time: 9:01:48 AM | File: D:\X250 Setup\DAQ System\DAQ_System_Sheet(3).5dDoc |          |



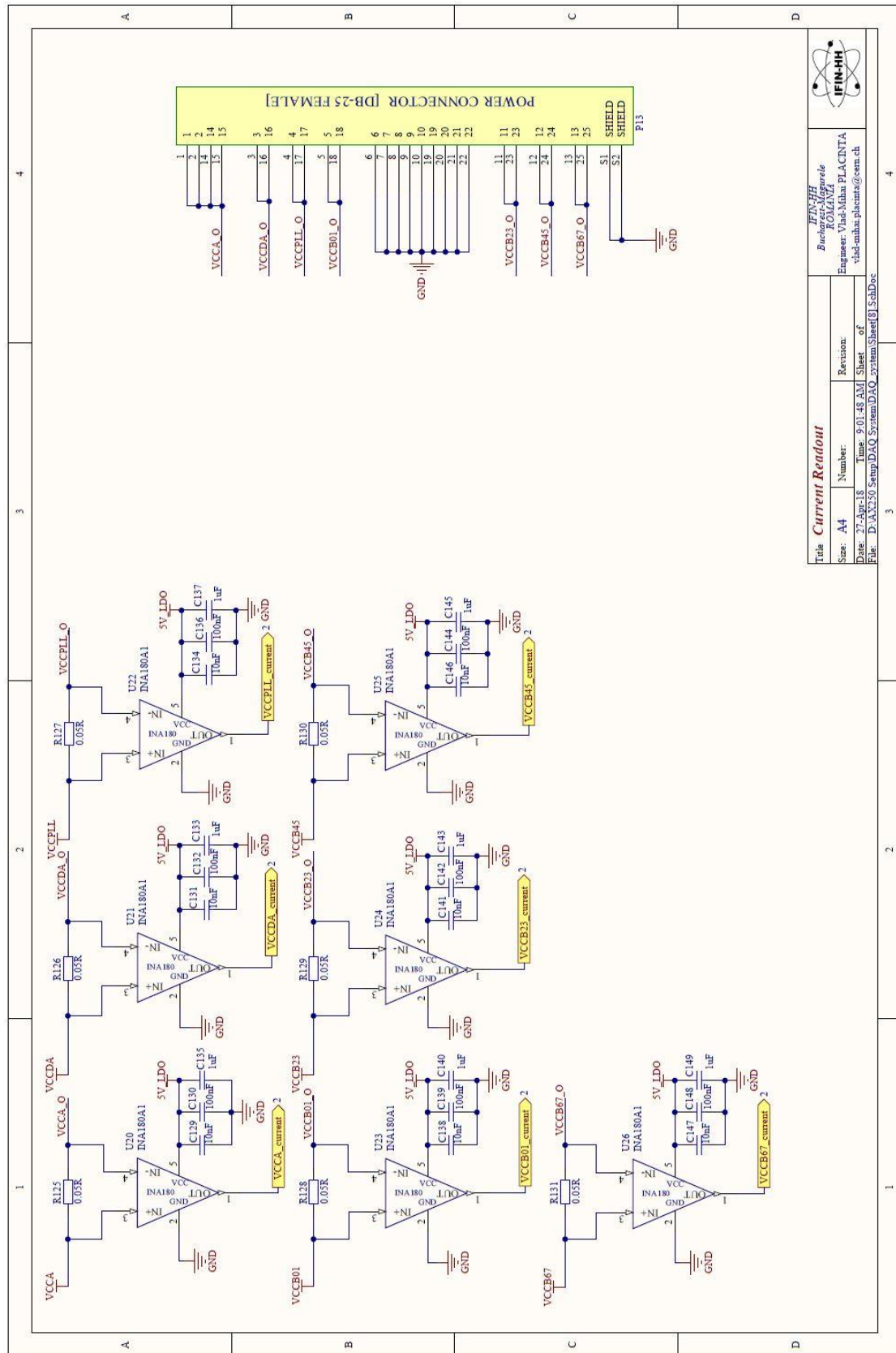












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Title: **Current Readout**

Size: A4

Number:

Revision:

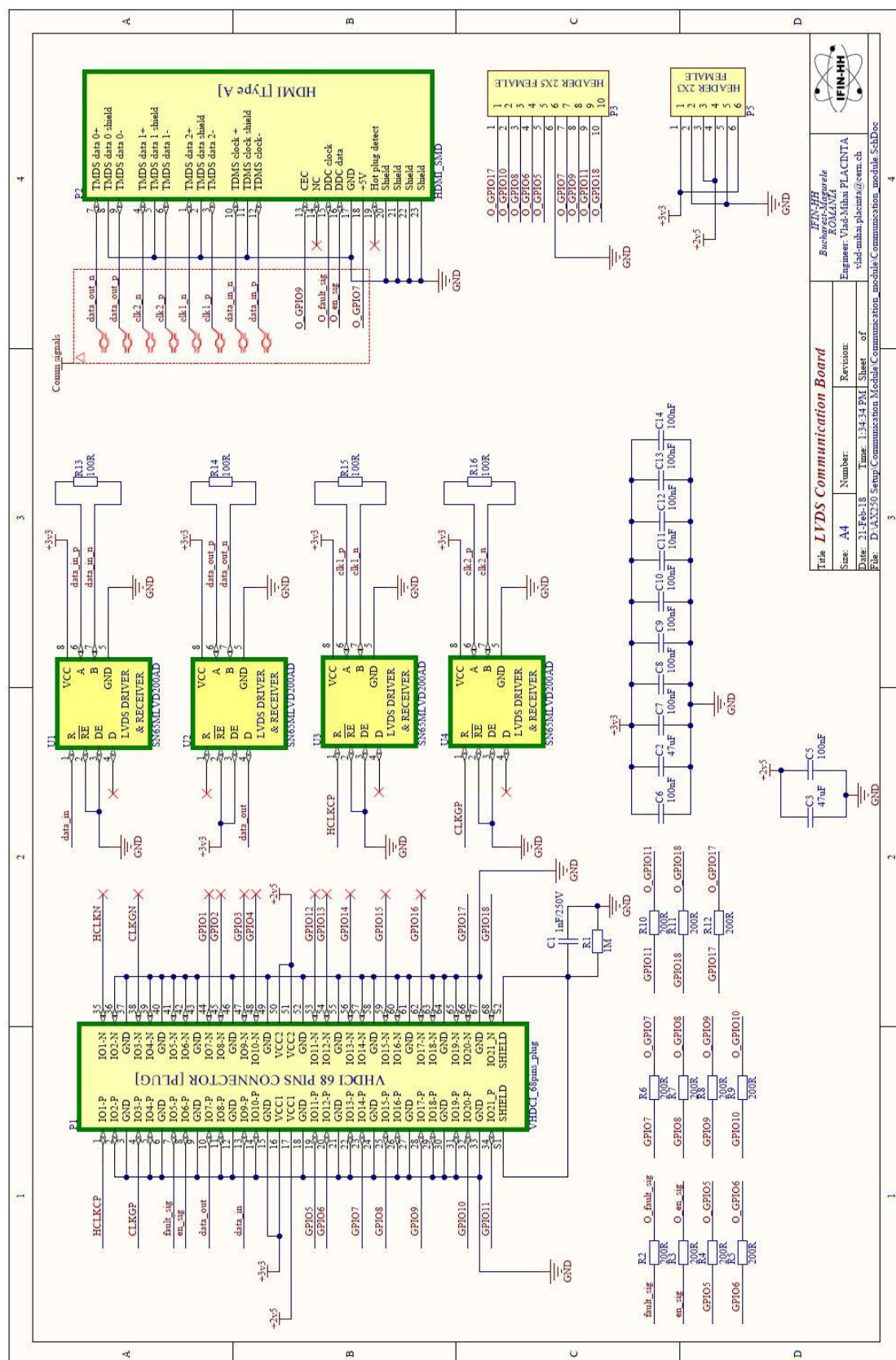
Date: 27-Apr-18

Time: 9:01:48 AM

Sheet of

File: D:\AX350 Setup\DAQ System\DAQ\_3774m\Sheet[5].SchDoc

## A.7 Schematic Diagram of the Communication Board



## A.8 VHDL Code for Basic TMR Architecture (Axcelerator FPGA)

```
-----  
-- Company: IFIN-HH  
-- Engineer: VLAD MIHAI PLACINTA  
-- Module Name: top_ax250_tmr - Behavioral  
-- Project Name: TMR FF  
-- Target Devices: AX250-FGG484  
-- Tool Versions: LIBERO IDE  
-----  
  
library IEEE;  
use IEEE.STD_LOGIC_1164.ALL;  
library Axcelerator;  
use Axcelerator.all;  
  
entity top_ax250_tmr is  
    Port (sys_clk : in STD_LOGIC;    --system clk in 40 MHz  
          LED0   : out STD_LOGIC;    --power on flag  
          fault_lane: out STD_LOGIC;  
          data_in  : in STD_LOGIC;    --data_input  
          data_out : out STD_LOGIC);  --data_output  
  
end top_ax250_tmr;  
  
architecture Behavioral of top_ax250_tmr is  
    constant R_cell_nr: integer:=846;    --846 for ~ 60% R cells usage  
    signal data_lane0: STD_LOGIC:= '0';    --lane0 from TMR  
    signal data_lane1: STD_LOGIC:= '0';    --lane1 from TMR  
    signal data_lane2: STD_LOGIC:= '0';    --lane2 from TMR  
  
    component tmr_lane is  
        generic (fd_nr: integer:=R_cell_nr/3);  
        Port ( clk      : in STD_LOGIC;  
              d_in      : in STD_LOGIC;  
              d_out      : out STD_LOGIC);  
    end component;  
  
    begin  
  
    Lane0:tmr_lane  
        port map (clk=> sys_clk,  
                 d_in=>data_in,  
                 d_out=>data_lane0);  
  
    Lane1:tmr_lane  
        port map (clk=> sys_clk,  
                 d_in=>data_in,  
                 d_out=>data_lane1);  
  
    Lane2:tmr_lane  
        port map (clk=> sys_clk,
```

```

        d_in=>data_in,
        d_out=>data_lane2);

data_out <= (data_lane0 AND data_lane1) OR (data_lane1 AND data_lane2) OR (data_lane0 AND
data_lane2); -- TMR Voter

fault_lane<=(data_lane0 XOR data_lane1) OR (data_lane1 XOR data_lane2) OR (data_lane0 XOR
data_lane2); --minority voter

---static signals declarations
LED0<='1';

end Behavioral;

-----TMR LANE COMPONENT-----

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
library Axcelerator;
use Axcelerator.all;

entity tmr_lane is
    generic (fd_nr: integer:=282);
    Port ( clk      : in STD_LOGIC;
          d_in      : in STD_LOGIC;
          d_out      : out STD_LOGIC);
end tmr_lane;
architecture Behavioral of tmr_lane is
    signal fd_link: std_logic_vector (fd_nr+1 downto 0) := (others => '0');

    --FFD instantiation-----
    component DF1 is

    port (D  : in std_logic; --data input
          clk : in std_logic; --clock input
          Q  : out std_logic); --data output

    end component;

    -----
begin

    lane:
    for i in 1 to fd_nr generate
    begin

        D_FF:DF1
        port map (clk=>clk,
                  D=> fd_link(i),
                  Q =>fd_link(i+1));

    end generate lane;

    fd_link(1)<=d_in;
    d_out<=fd_link(fd_nr+1);

end Behavioral;

```

## A.9 VHDL Code for Embedded RAM Readout Firmware (Axcelerator FPGA)

```
-----  
-- Company: IFIN-HH  
-- Engineer: VLAD MIHAI PLACINTA  
-- Module Name: top_bram_ax250 - Behavioral  
-- Project Name: Embedded RAM readout firmware  
-- Target Devices: AX250-FGG484  
-- Tool Versions: LIBERO IDE  
-----  
  
library IEEE;  
use IEEE.STD_LOGIC_1164.ALL;  
library Axcelerator;  
use Axcelerator.all;  
USE ieee.std_logic_arith.all;  
USE ieee.std_logic_unsigned.all;  
  
entity top_bram_ax250 is  
Port (sys_clk : in STD_LOGIC;    --system clk in 40 MHz  
      rst      : in STD_LOGIC;    -- rst signal  
      LED0      : out STD_LOGIC;   --power on flag  
      LED1      : out STD_LOGIC;   --tx on flag  
      en_tx     : in STD_LOGIC;    -- en tx signal  
      done_tx   : out STD_LOGIC;   --en tx signal  
      data_out  : out STD_LOGIC);  --data_output  
  
end top_bram_ax250;  
architecture Behavioral of top_bram_ax250 is  
  
  --tx setup--  
  constant clk_freq : integer :=40_000_000;  
  constant baud_rate : integer :=1_000_000;  
  constant os_rate   : integer :=16;  
  constant d_width   : integer :=152;  
  constant tx_lengh  : integer :=19;  
  
  -----tx machine setup-----  
  type tx_machine is(idle, transmit, wait_till_next);  
  signal tx_state :tx_machine;  
  signal baud_rate_pulse :STD_LOGIC := '0';  
  signal over_s_pulse   :STD_LOGIC := '0';  
  signal tx_enable      :STD_LOGIC := '0';  
  signal tx_done        :STD_LOGIC := '0';  
  signal tx_buffer      :STD_LOGIC_VECTOR(d_width+1 downto 0) := (OTHERS => '1');  
  
  signal delay_counter: integer range 0 to 3000000:= 0;  
  
  -----SRAM declarations-----  
  
  signal data_to_write : STD_LOGIC_VECTOR (35 downto 0):=(others => '0');
```

```

signal data_to_read : STD_LOGIC_VECTOR (35 downto 0):=(others => '0');
signal data_r       : STD_LOGIC_VECTOR (143 downto 0):=(others => '0');
constant data_wr0   : STD_LOGIC_VECTOR (35 downto 0):= x"F0F0F0F0F";    --dummmmy data
constant data_wr1   : STD_LOGIC_VECTOR (35 downto 0):= x"0F0F0F0F0";    --dummmmy data
constant header     : STD_LOGIC_VECTOR (7  downto 0):= x"AA";          --dummy pattern
signal address_r    : std_logic_vector (10 downto 0):=(others => '0');
signal address_w    : std_logic_vector (10 downto 0):=(others => '0');
signal WE           : STD_LOGIC := '0';
signal wr_ram       : STD_LOGIC := '0';
signal counter_sec  : integer range 0 to 4 :=0;

-----ram machine setup-----
type ram_machine is(idle, write, read, transmit);
signal ram_state :ram_machine;

--RAM BLOCK-----
component sync_ram is
  port (
    clock : in std_logic;
    we    : in std_logic;
    address_r : in std_logic_vector (10 downto 0);
    address_w : in std_logic_vector (10 downto 0);
    datain : in std_logic_vector;
    dataout : out std_logic_vector
  );
end component;

begin

SRAM_inst: sync_ram

port map ( datain => data_to_write,
           dataout => data_to_read,
           address_r => address_r,
           address_w => address_w,
           we      => WE,
           clock   => sys_clk);

--generate baud rate and oversampling rate
process(rst, sys_clk)
variable cnt_baud:integer range 0 to clk_freq/baud_rate-1 := 0;
variable count_os:integer range 0 to clk_freq/baud_rate/os_rate-1 := 0;
begin
if(rst = '1') then
baud_rate_pulse <= '0';
over_s_pulse <= '0';
cnt_baud := 0;
count_os := 0;
elsif(rising_edge(sys_clk)) THEN
--create baud enable pulse
if(cnt_baud < clk_freq/baud_rate-1) then
:= cnt_baud + 1;
baud_rate_pulse <= '0';
else
cnt_baud := 0;
baud_rate_pulse <= '1';
count_os := 0;
end if;

--create oversampling enable pulse

```

```

if(count_os < clk_freq/ baud_rate/os_rate-1) then
count_os := count_os + 1;
over_s_pulse <= '0';
else
count_os := 0;
over_s_pulse <= '1';

end if;
end if;
end process;

--transmit state machine
process(rst, sys_clk)
variable tx_count :integer range 0 to d_width+3 := 0;
begin
if(rst = '1') then
tx_count := 0;
data_out <= '1';
delay_counter<=0;
tx_done <= '0';
tx_state <= idle;
elsif(rising_edge(sys_clk)) then
case tx_state is
when idle =>
if(tx_enable = '1') then
tx_buffer(d_width+1 downto 0) <= header & data_r & '0' & '1';
tx_count := 0;
tx_state <= transmit;
else
tx_done <= '0';
tx_state <= idle;
end if;

when transmit =>
if(baud_rate_pulse = '1') then

tx_count := tx_count + 1;
tx_buffer <= '1' & tx_buffer(d_width+1 downto 1);
end if;
if(tx_count < d_width+3) then
tx_state <= transmit;
else
tx_done <= '1';
tx_state<=wait_till_next;
end if;

when wait_till_next =>
if (delay_counter = 40000) then
tx_done <= '0';
delay_counter<=0;
tx_state <= idle;
else
delay_counter<=delay_counter+1;
tx_state<=wait_till_next;
end if;

when others => tx_state <= idle;
end case;
data_out <= tx_buffer(0);
end if;

```



```

end process;
----ram state machine -----
process(rst, sys_clk)
begin
if(rst = '1') then
WE<= '0';
data_to_write<= (others => '0');
address_r <= (others => '0');
address_w <= (others => '0');
wr_ram <= '0';
ram_state <= idle;
elsif(rising_edge(sys_clk)) then
case ram_state is
when idle =>
WE<= '0';
if (en_tx = '1') then
ram_state <= write;
end if;

when write =>
if(wr_ram = '0') then
WE<= '1';
if ( address_w > "0111111111") then -- if the addresses are reached > 1023
address_w <= (others => '0'); -- reset the counter
wr_ram <= '1';
ram_state <= idle; -- go to idle
else
if (address_w < "00111110100") then --if its lower than 200 low first dummy data
data_to_write<=data_wr0;
else
data_to_write<=data_wr1;
end if;
address_w <= address_w + 1;
end if;
ram_state<= write;
else
WE<= '0';
ram_state<=read;
end if;

when read =>
if ( address_r > "0111111111") then -- if the addresses are reached > 349
address_r <= (others => '0');
ram_state <= idle;
else
data_r (35 + counter_sec * 36 downto counter_sec * 36) <= data_to_read;
if (counter_sec = 3 ) then
counter_sec<=0;
ram_state<=transmit;
end if;
address_r<= address_r+1;
counter_sec<=counter_sec+1;
end if;

when transmit =>
tx_enable<='1';
if (tx_done = '1') then
tx_enable<= '0';
ram_state <= idle;
end if;

```

```

when others => ram_state <= idle;

end case;
end if;
end process;

---static signals declarations
--LED0<= '1'; --power on flag
LED0<= '1'; --power on flag
LED1<= en_tx; --tx on flag
done_tx<=tx_done;

end Behavioral;

-----RAM Declaration COMPONENT-----

library IEEE;
use IEEE.STD_LOGIC_1164.all;
use IEEE.Numeric_Std.all;

entity sync_ram is
port (
    clock : in std_logic;
    we : in std_logic;
    address_r : in std_logic_vector (10 downto 0);
    address_w : in std_logic_vector (10 downto 0);
    datain : in std_logic_vector (35 downto 0);
    dataout : out std_logic_vector (35 downto 0));
end entity sync_ram;

architecture RTL of sync_ram is

constant ram_size: integer:= 1023;

type ram_type is array (0 to ram_size) of std_logic_vector(35 downto 0);
signal ram : ram_type;
signal read_address : std_logic_vector(10 downto 0);

attribute syn_ramstyle : string;
attribute syn_ramstyle of ram : signal is "block_ram";

begin

    RamProc: process(clock) is

    begin
    if rising_edge(clock) then
    if we = '1' then
    ram(to_integer(unsigned(address_w))) <= datain;
    end if;
    read_address <= address_r;
    end if;
    end process RamProc;

    dataout <= ram(to_integer(unsigned(read_address)));

end architecture RTL;

```

## A.10 VHDL Code for LHCb-RICH like Firmware (Axcelerator FPGA)

```
-----
-- Company: IFIN-HH
-- Engineer: VLAD MIHAI PLACINTA
-- Module Name: lhcb_rich_ax250 - Behavioral
-- Project Name: LHCb RICH like firmware
-- Target Devices: AX250-FGG484
-- Tool Versions: LIBERO IDE
-----

library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity lhcb_rich_ax250 is
    Port (sys_clk : in STD_LOGIC;    --system clk in 40 MHz
          rst     : in STD_LOGIC;    -- rst signal
          LED0    : out STD_LOGIC;   --power on flag
          LED1    : out STD_LOGIC;   --tx on flag
          en_tx   : in STD_LOGIC;    -- en tx signal
          done_tx : out STD_LOGIC;    -- en tx signal
          MaPMTA0 : in STD_LOGIC_VECTOR (31 downto 0); --first half of MAPMT A
          MaPMTA1 : in STD_LOGIC_VECTOR (63 downto 32); --second half of MAPMT A
          MaPMTB0 : in STD_LOGIC_VECTOR (31 downto 0); --first half of MAPMT B
          MaPMTB1 : in STD_LOGIC_VECTOR (63 downto 32); --second half of MAPMT B
          data_out: out STD_LOGIC);   --data_output

end lhcb_rich_ax250;
architecture Behavioral of lhcb_rich_ax250 is

    signal data_frame : STD_LOGIC_VECTOR (151 downto 0):=(others => '0'); -- data frame to be send to
    DAQ
    constant frame_header : STD_LOGIC_VECTOR (23 downto 0):=x"D66E5B";    -- frame header

    --tx setup--
    constant clk_freq : integer :=40_000_000;
    constant baud_rate : integer :=1_000_000;
    constant os_rate : integer :=16;
    constant d_width : integer :=152;
    constant tx_length : integer :=19;

    -----tx machine setup-----
    type tx_machine is(idle, transmit, wait_till_next);
    signal tx_state :tx_machine;
    signal baud_rate_pulse : STD_LOGIC := '0';
    signal over_s_pulse : STD_LOGIC := '0';
    signal tx_buffer : STD_LOGIC_VECTOR(d_width+1 downto 0) := (OTHERS => '1');
    signal delay_counter: integer range 0 to 3000000:= 0;

begin
```

```

--generate baud rate and oversampling rate
process(rst, sys_clk)
variable cnt_baud:integer range 0 to clk_freq/baud_rate-1 := 0;
variable count_os:integer range 0 to clk_freq/baud_rate/os_rate-1 := 0;
begin
if(rst = '1') then
baud_rate_pulse <= '0';
over_s_pulse <= '0';
cnt_baud := 0;
count_os := 0;
elsif(rising_edge(sys_clk)) THEN
--create baud enable pulse
if(cnt_baud < clk_freq/baud_rate-1) then
cnt_baud := cnt_baud + 1;
baud_rate_pulse <= '0';
else
cnt_baud := 0;
baud_rate_pulse <= '1';
count_os := 0;
end if;
--create oversampling enable pulse
if(count_os < clk_freq/baud_rate/os_rate-1) then
count_os := count_os + 1;
over_s_pulse <= '0';
else
count_os := 0;
over_s_pulse <= '1';
end if;
end if;
end process;

--transmit state machine
process(rst, sys_clk)
variable tx_count :integer range 0 to d_width+3 := 0;
begin
if(rst = '1') then
tx_count := 0;
data_out <= '1';
delay_counter<=0;
done_tx <= '0';
tx_state <= idle;
elsif(rising_edge(sys_clk)) then
case tx_state is

when idle =>
if(en_tx = '1') then
tx_buffer(d_width+1 downto 0) <= data_frame & '0' & '1';
tx_count := 0;
tx_state <= transmit;
else
done_tx <= '0';
tx_state <= idle;
end if;

when transmit =>
if(baud_rate_pulse = '1') then

tx_count := tx_count + 1;
tx_buffer <= '1' & tx_buffer(d_width+1 downto 1);

```

```

end if;
if(tx_count < d_width+3) then
tx_state <= transmit;
else
done_tx <= '1';
tx_state<=wait_till_next;
end if;

when wait_till_next =>
if (delay_counter = 40000) then    --generate an 1 ms between transactions
done_tx <= '0';
delay_counter<=0;
tx_state <= idle;
else
delay_counter<=delay_counter+1;
tx_state<=wait_till_next;
end if;

when others =>
tx_state <= idle;

end case;
data_out <= tx_buffer(0);    --output last bit in transmit transaction buffer
end if;
end process;

---to pack the data-----
process(sys_clk, rst)
begin

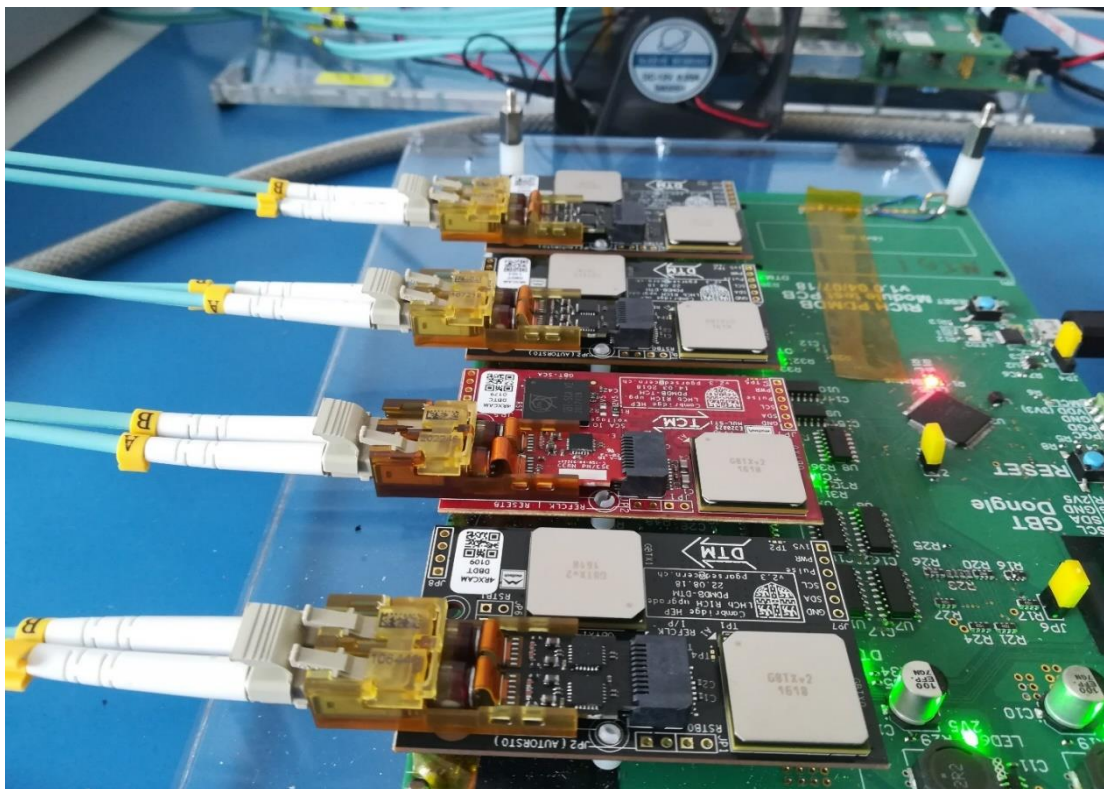
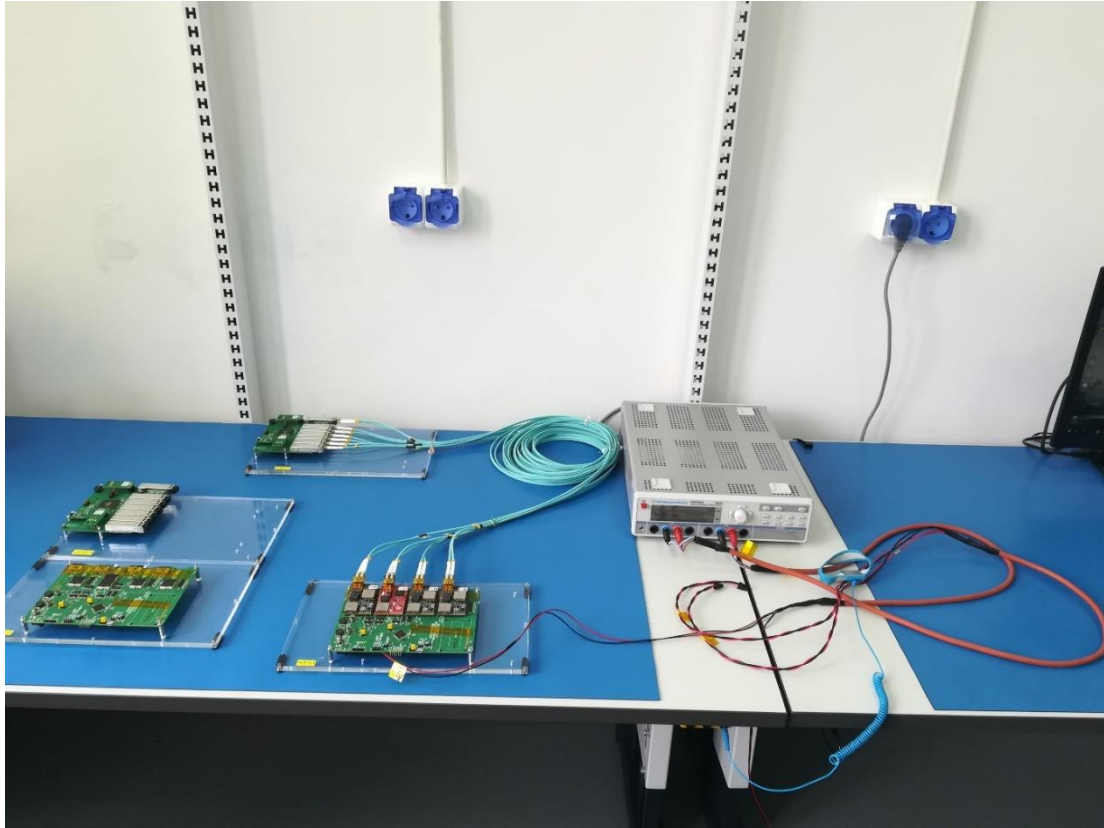
if (rst = '1') then
data_frame<= (others => '0');
elsif (rising_edge(sys_clk)) then
data_frame<= frame_header & MAPMTA1 & MAPMTA0 & MAPMTB1 & MAPMTB0;    --data to be
packed at 40 MHz
end if;
end process;

---static signals declarations
LED0<= '1'; --power on flag
LED1<= en_tx; --tx on flag

end Behavioral;

```

## A.11 Photos During the Production Testing and Quality Assurance of the PDMDB Plugin Modules



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