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**Design and development of the Level-1 Data Driver Card
(L1DDC) for the New Small Wheel upgrade of the ATLAS
experiment at CERN**

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Design and development of the Level-1 Data Driver Card (L1DDC) for the New Small Wheel upgrade of the ATLAS experiment at CERN

PhD THESIS

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Abstract

ATLAS is one of the four main experiments located in the Large Hardon Collider at CERN. During Long Shutdown 2 (2019-2020) the innermost muon stations of ATLAS called the Small Wheels will be replaced by the New Small Wheel upgrade project. This upgrade is motivated by the high particle flux (up to 15 kHz/cm^2), the high radiation during Run-3 (2021-2023) and ultimate luminosity of $7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ expected in High-Luminosity Large Hadron Collider (after 2026). The number of interactions per bunch-crossing (every 25 ns) will be increased up to 140, resulting in a dramatically large amount of produced data. The New Small Wheel is a set of precision tracking and trigger detectors able to work at high rates with excellent real-time spatial and time resolution. The new detectors consist of the resistive Micromegas and the small-strip Thin Gap Chambers. Furthermore, a radiation dose up to 1700 Gy (innermost radius) and a magnetic field up to 0.4 T in the end cap region, create a hostile environment for the front-end electronics. To read out the large number of electronic channels (~ 2.1 million for the Micromegas and ~ 332 thousand for the sTGC) and in order to survive in such a harsh environment new electronics must be fabricated and installed. In addition, correction mechanisms for Single Event Upsets (this is a change of state caused by a high-energy particle strike to a micro-electronic device) must be implemented to assure the integrity of the transmitted data. The whole readout and trigger architecture of the NSW was redesigned including the fabrication of new electronic boards and Application Specific Integrated Circuits compatible even with the Run-4 data rates.

The aim of this dissertation was the research and development of the Level-1 Data Driver Card which is part of the data acquisition system for both detector technologies and consists of radiation tolerant components. The development of the cards included a series of prototypes and their extensive testing independently, and as part of the final system as well. A major and extensive study to make these cards compatible even with the future (and demanding) upgrades of the experiment was performed. Up to now, eight different versions of these cards have been manufactured and tested. The latest prototypes, after their debugging, are the reference cards for mass production of 1056 Level-1 Data Driver Cards. Additionally for the needs of the experiment and for a more complete control and testing of the cards and the final system, a series of Front-Ends, a Low Voltage distributor and a series of auxiliary cards were designed and fabricated.

Furthermore for the testing procedure of the boards different pieces of firmware were developed using the Very High Speed Integrated Circuit Hardware Description Language. This development includes communication of the control system with the Level-1 Data Driver Card through optical link, the programming of the Application Specific Integrated Circuits on the Level-1 Data Driver Card card, the acquisition of environmental variables (voltage levels and

temperatures) and their evaluation by a personal computer through the Ethernet interface and UDP/IP protocols. In order to validate the final system, a low-level code was also developed, tested and debugged to configure the Venetis MicroMegas Application Specific Integrated Circuit (on the Front-Ends) to collect data from the detectors and transfer them via the UDP/IP protocol to a computer for storage and subsequent evaluation.

Preface

Purpose of this dissertation is mainly to design and produce the Level-1 Data Driver Card for the needs of the New Small Wheel upgrade of the ATLAS experiment at CERN. The design rules, the components and materials that were selected and the tests performed are described in detail. The nature of the New Small Wheel detectors (micromegas and small-strip Thin Gap Chamber) along with the expected high data rates led to three different Level-1 Data Driver Cards that were finalized and verified after a series of prototypes.

- Chapter 1: The ATLAS experiment and the future upgrades of the Large Hardon Collider are described in detail. The high luminosity expected in the future runs ($7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$) has a deep impact on the New Small Wheel data rates. To handle the new high rates, the current trigger architecture is redesigned and will be gradually deployed. The operation principle of the new detectors (micromegas and small-strip Thin Gap Chambers) is also mentioned.
- Chapter 2: Presents in detail the architecture of the data acquisition and trigger paths for both micromegas and sTGC detectors. A series of custom made boards and Application Specific Integrated Circuits were designed. Moreover the connectivity of the on-detector electronics, the grounding policy and the protocols being used are also described. A common board for the readout path of both detector technologies was developed. This prototype comprises a radiation tolerant Application Specific Integrated Circuits fabricated at CERN but also a commercial Field Programmable Gate Array and many additional features. Main purpose of the board is to provide a synchronous clock to all on-detector electronics, read out the detector data, monitor environmental variables (temperature, current and voltage levels) and to configure all the Application Specific Integrated Circuits and Field Programmable Gate Arrays. The specifications, design selections, communication protocols and results of various tests are presented. The impact of the high readout data rate expected in the future runs, due to the updated trigger scheme of the New Small Wheel is also examined. Additional chips, cables and fibers were used but also the power distribution and cooling architectures were revised.
- Chapter 3: Due to the different characteristics and data rates of both detector technologies different Level-1 Data Driver Cards were eventually fabricated. The harsh environment in the detector area which is imposed by the radiation and magnetic field made the design challenging. All materials must comply with CERN regulations and should also be radiation and magnetic tolerant. Furthermore, high quality clocks should be provided to the Front-End electronics for the reliable high speed data transmission. This chapter describes in detail the roadmap of the Level-1 Data Driver Card for the small-strip Thin Gap Chambers through a series of prototypes, design preferences, schematics, tests and errors identified.

- Chapter 4: The micromegas Level-1 Data Driver Card is part of the data acquisition of the micromegas detectors. This board comprises the same components with the Level-1 Data Driver Card for the small-strip Thin Gap Chambers but due to the higher data rates of the micromegas detector uses a different configuration. A detailed description of the prototype and production boards along with the test results are presented.
- Chapter 5: The rim Level-1 Data Driver Card is part of the trigger chain of the small-strip Thin Gap Chambers. Although it does not handle trigger data is used for configuration, clock distribution and for reading out any additional data. Moreover, it distributes a low jitter clock to the demanding 7-family Field Programmable Gate Array transceivers for the creation of the high speed links. A series of tests were performed and prototype boards were developed to verify the proper clock distribution. The design preferences, the issues identified and the test results are also described in this chapter.
- Chapter 6: Describes the position of the various Level-1 Data Driver Cards on both types of detectors (micromegas and small-strip Thin Gap Chambers). Due to the limited available space of the detectors the placement became challenging. The interface with the other on-detector electronics, cable lengths and cooling preferences are presented. In total 1184 Level-1 Data Driver Card boards (including pre-production and 10% overage) will be produced. Thus, in order to test them extensively and to avoid any human errors, a fully automated system should be deployed. Four testing sites in different universities are already allocated and equipped with the appropriate tools for the testing of the boards. This chapter describes in detail the overall testing procedure, the firmware that was developed and the information needed to be stored in the database. The signal integrity of the transmitted data through long cables and especial for high speed signals is examined. The technique to cope with the cable attenuation was to boost the signals by using additional chips (repeaters). A series of tests performed in order to validate the link stability and data integrity. The outcome of the tests are also presented.
- Chapter 7: In this Chapter the conclusions are presented.
- Appendix: To validate the boards as part of the overall architecture a number of Front-Ends, mezzanines and adapters boards were developed. Moreover for the Level-1 Data Driver Card validation and for the Front-End data acquisition two different firmwares (low level code in Very High Speed Integrated Circuit Hardware Description Language) were developed, debugged and tested. This chapter describes in detail the boards that were designed and fabricated but also the firmware that was deployed.

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The true sign of intelligence is not knowledge but imagination.

Research is to see what everybody else has seen, and to think what nobody else has
thought.

Albert Einstein, 1879-1955

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The ATLAS experiment and the New Small Wheel Upgrade project

The ATLAS [1] along with CMS, LHCb and ALICE is one of the four main experiments located at the Large Hardon Collider (LHC) at CERN. LHC is the largest and most powerful particle collider in the world. In this circular machine which is 27 km long and 100 m below ground protons are accelerated close to the speed of light. Protons collide in four different places in the LHC where the four main experiments are located. When the LHC runs at full energy and intensity, about 600 million proton-proton collisions take place every second inside the vast ATLAS detector.

The future upgrades of the LHC will lead to an average instantaneous luminosity of $5 - 7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$. During Run-1 (2011-2012) the average instantaneous luminosity in the LHC was 0.75 times that of the nominal one ($10^{34} \text{ cm}^{-2}\text{s}^{-1}$) and a centre-of-mass energy of 7 – 8 TeV. After a two-year shut-down, LHC restarted (Run-2, 2015-2018) to deliver proton-proton collisions with the nominal luminosity ($1 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$) and a centre-of-mass energy of 13 TeV. In Run-3 (2021-2023), after the Phase 1 upgrade, the instantaneous luminosity will be increased to $2.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ and in the future upgrades of Phase 2 and Run-4,5..(2026-2038) to $5 - 7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ with a centre-of-mass energy of 14 TeV. The LHC plan is presented in Figure 1.1.

A major upgrade of the experiments is required to cope with these new conditions and to fully exploit the HL-LHC physics potential [2]. ATLAS is a general-purpose particle physics experiment consisting of different subsystems. As illustrated in Figure 1.2, ATLAS has a height of 25 m, a length of 44 m and weighs 7000 tons. In the center of ATLAS, where the beams collide, the pixel detector, the tracker and the Liquid Argon (LAr) electromagnetic/(hadronic end-cap and forward) calorimeters are located. Around the LAr the tile calorimeters are located and in the outer part the muon systems. The muon spectrometer, made up of 4,000 individual muon chambers using four different technologies by 48 institutions in 23 production sites around the world, identifies and measures the momenta of muons. The Small Wheels are placed between the toroid magnets and the tile calorimeters and consist of three different types of detectors: the Monitor Drift Tubes (MDT), the TGCs and the Cathode Strip Chambers (CSC).

During Run-3 the mean number of interactions per bunch-crossing (every 25 ns) will be increased up to 140, resulting in a dramatically large amount of produced data.



Figure 1.1: The LHC plan.

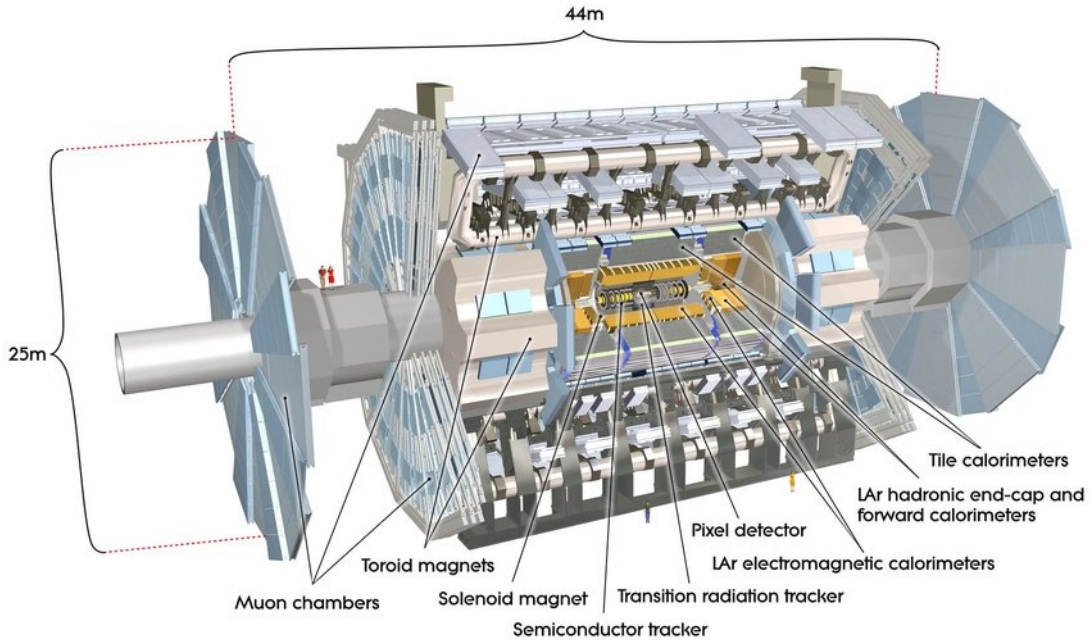


Figure 1.2: The ATLAS detector and its subsystems.

In the ATLAS experiment the present muon Small Wheels will be replaced by the New Small Wheel (NSW) [3, 4]. The NSW is a set of precision tracking and trigger detectors able to work at high rates with excellent real-time spatial and time (≈ 10 ns) resolution. The new detectors consist of the resistive micromegas and the Small-strip Thin Gap Chambers (sTGC). Each of the two wheels consist of sixteen sectors, eight large called Large Modules (LM) and eight small called Small Modules (SM), with a diameter of about 10 m, as presented in Figure 1.3(a). Each sector has four wedges (four planes of the same detector technology) with a configuration of sTGC-Micromegas-Micromegas-sTGC as is illustrated in Figure 1.3(b). The planes are divided into two parts, the

LM1/SM1 consisting of five PCBs (with 1024 readout strips per PCB) and the SM1/SM2 consisting of three PCBs. NSW is designed to detect muons in the pseudorapidity region $1.3 < |\eta| < 2.7$ and can handle particle rates up to 15 KHz/cm^2 . It is worth mentioning the huge number of readout channels which rises up to two million for the Micromegas and up to 330 thousands for the sTGC detectors.

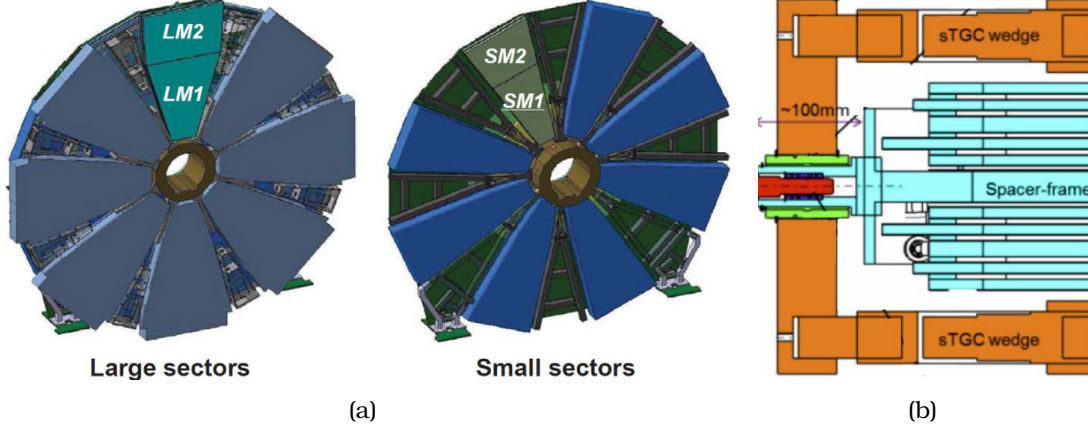


Figure 1.3: (a) NSW layout, (b) Cross-section of a sector.

Currently in ATLAS, more than 90% of the Endcap-Muon (EM) triggers are fake. This is due to background, low energy particles generated in the materials between the SW and the EM and have an angle similar to that of real p_T muons [5]. NSW will be part of the Level-1 trigger decision minimizing the fake triggers by reconstructing high quality (σ_θ of about 1 mrad) Interaction Point (IP) pointing segments providing also efficient and precise tracking for the expected rate of 15 kHz/cm^2 . For $|\eta| > 1$ triggers are dominated from Big Wheel fake triggers (L1 MU11 shaded areas) as shown on the left of Figure 1.4.

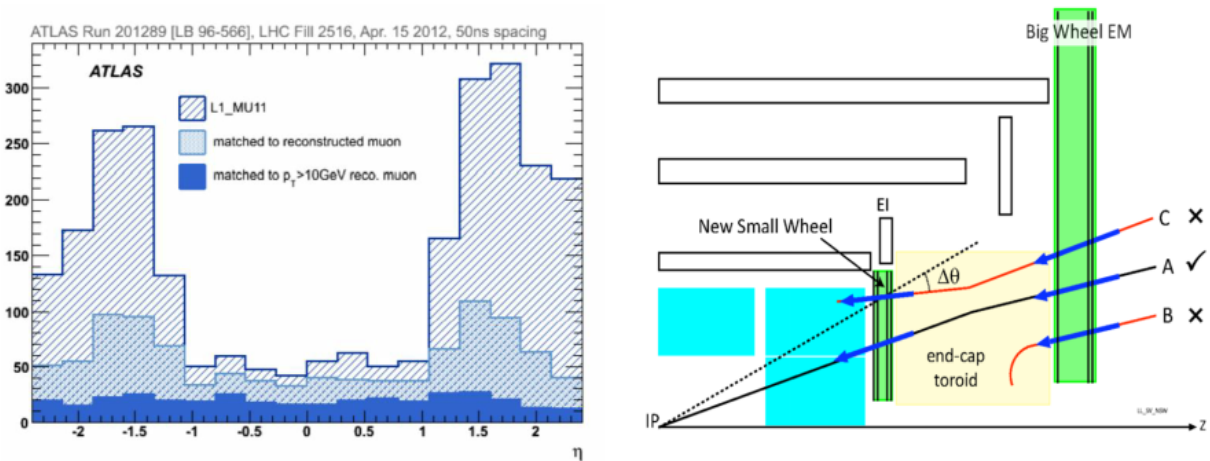


Figure 1.4: Left: η distribution of level-1 muon triggers ($p_T > 10 \text{ GeV}$). NSW as part of the trigger logic, rejects B and C tracks.

1.1 The ATLAS trigger scheme

In the ATLAS experiment the trigger system is responsible for deciding whether or not to record a given collision event [6]. The trigger system is complicated and involves different subsystems. To meet Phase 1 and Phase 2 requirements the trigger system will be upgraded and new electronics will be developed.

The ATLAS trigger system is designed to reduce the event rate from the LHC bunch crossing frequency of 40 MHz to about 1 kHz for permanent storage. The trigger architecture for Run 3 uses a trigger system which consists of a custom hardware-based Level-1 (L1) trigger and a computer-based High-Level trigger (HLT) [7]. The L1 trigger system uses custom electronics to determine the regions of interest (RoI) from the calorimeter and muon spectrometer signals, searching for signatures such as large electromagnetic energy deposits or high- p_T muon tracks. The L1 trigger is capable of reducing the event rate of 40 MHz to 100 kHz with a latency of 2.5 μ s. The HLT then runs trigger algorithms with near-offline reconstruction quality on either the RoIs or the full event information with an off-the-shelf CPU farm. This technique reduces further the event rate from 100 kHz to about 1 kHz with an average latency of 0.3 s

The main new trigger components for Run 3 are the electron Feature EXtractor (eFEX), jet Feature EXtractor (jFEX), global Feature EXtractor (gFEX) processors, the Level-1 Muon Trigger sector logic for the endcap, a NSW trigger processor for muon reconstruction in the endcap region, the inclusion of Tile Calorimeter information in the muon trigger, an improved Muon Central Trigger Processor Interface (MUCTPI) capable of providing precision muon inputs to the Level-1 Topological Processor (L1Topo) and an upgraded version of L1Topo. The overall ATLAS Trigger and Data Acquisition System (TDAQ) Phase 1 upgrade architecture is presented in Figure 1.5.

After a L1A is issued, the DAQ system is responsible for the transport and assembly of the event data all the way from the sub-detector RODs to the logging to disk. While the readout path remains unchanged for most systems, the new and upgraded subdetector systems, such as the Muon NSW, L1Calo and the LAr calorimeter, deploy a Front-End Link eXchange FELIX-based readout system [8], the first element of the DAQ system receiving front-end detector data and routing it using commodity multi-gigabit network to further processing. The data are passed and buffered in the Read Out System (ROS), until requested by the HLT farm, where they are assembled into events (event building) and ultimately recorded to disk once accepted by the HLT. Finally, the HLT system exploits the capabilities of the FTK, which is designed to provide charged particle track reconstruction within 100 μ s of every event accepted by the Level-1 Trigger.

The Phase 2 baseline trigger architecture is based on a single Level-0 hardware trigger with a detector readout rate of 1 MHz (with a maximum latency of 10 μ s) and a decision formed using calorimeter and muon information. In addition, each system and sub-system is designed to be able to handle a dual-level hardware-based trigger architecture. This two-level hardware trigger design specifies a Level-0 trigger rate of 2-4 MHz and 10 μ s latency, followed by a Level-1 trigger rate of 600–800 kHz and latency up to 35 μ s.

After the Phase 2 upgrade and during Run 3 the Level-0 trigger decision will be formed by the Level-0 Calorimeter Trigger (LOCalo), the Level-0 Muon Trigger (LOMuon),

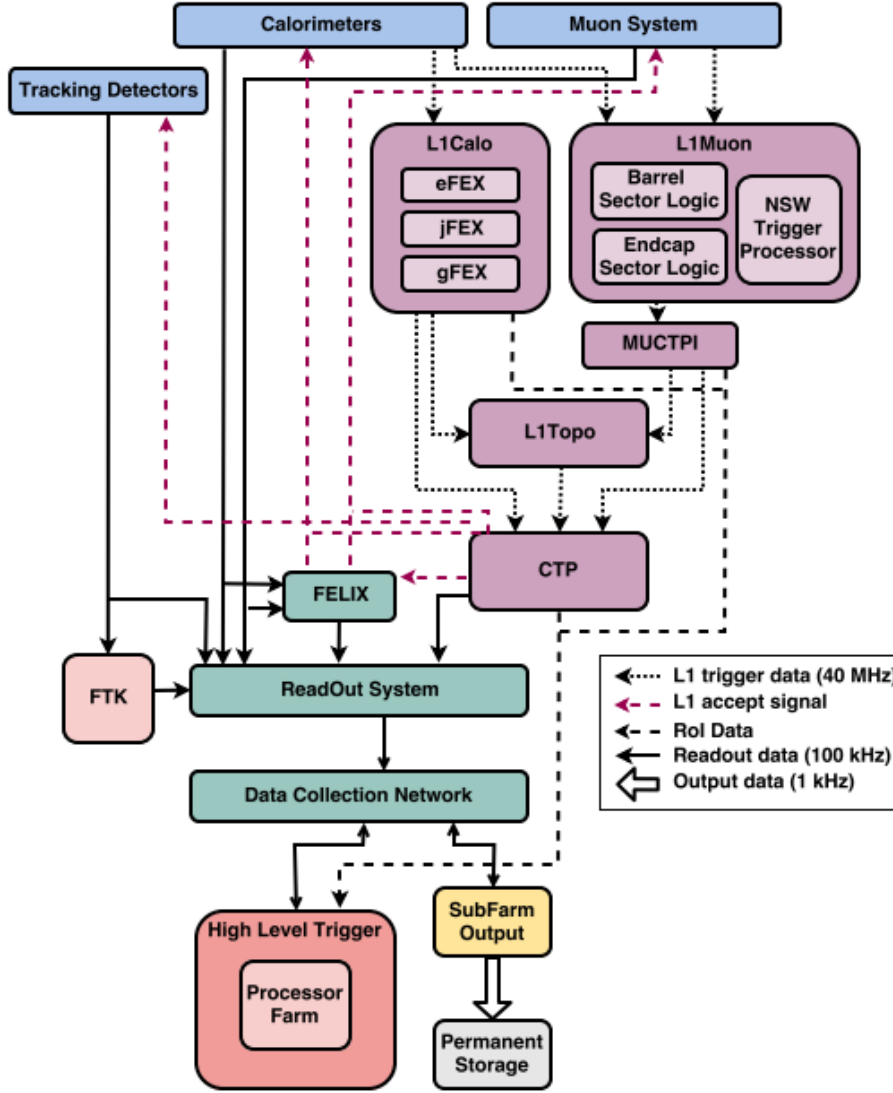


Figure 1.5: TDAQ Phase 1 upgrade architecture.

the Global Trigger and the Central Trigger sub-systems [9]. The L0Calo sub-system is composed of the Phase-I eFEX, jFEX, gFEX complemented by a new forward Feature EXtractor (fFEX) component to reconstruct forward jets and electrons, matching the pseudo-rapidity coverage of the new tracker system. The L0Muon sub-system comprises the Barrel and Endcap Sector Logic processors, the NSW Trigger Processor, and the MDT Trigger Processor.

For the reconstruction of muon candidates in the barrel Resistive Plate Chambers (RPCs) the new L0Muon sub-system will use upgraded Barrel Sector logic. On the other hand, for the endcap Thin Gap Chambers (TGCs) and NSW detectors upgraded Endcap Sector Logic and New Small Wheel (NSW) Trigger Processors will be used. In addition, Monitored Drift Tube (MDT) information will be used in new dedicated processors to improve robustness and efficiency of the Muon Trigger, its p_T resolution and selectivity. The MUCTPI component interfaces the L0Muon sub-system with the CTP.

The Global Trigger will replace and extend Topological Processor that will be used in

Run 2, by accessing full-granularity calorimeter information to refine the trigger objects calculated by L0Calo, perform offline-like algorithms, executes topological algorithms and calculate event-level quantities before applying topological selections. The CTP forms triggers based on combinations of inputs or conditions received from the Global Trigger and other sources. The final trigger decision is made by the Central Trigger Processor (CTP), which can apply flexible pre-scale factors and introduces deadtime when necessary to avoid saturation in the front-end and readout systems. The CTP transmits also the Trigger, Timing and Control system network to start the readout process on the detectors.

The Level-0 trigger decision is transmitted to all detectors and trigger processors. After the trigger reception by the detector, the detector and trigger data are transmitted to the Data Acquisition system at 1 MHz through the Readout and the Dataflow sub-systems. The Readout system contains the FELIX and Data Handler, and the Dataflow subsystem contains the Event Builder, Storage Handler, and Event Aggregator. These sub-systems are based on commodity PC servers and standard networking infrastructure. The Readout sub-system converts the detector front-end protocol data into standard network packets by using custom made electronics cards. The Event Filter (EF) system consists of a CPU-based processing farm and a Hardware-based Tracking for the Trigger co-processor. The main function of the EF system is to refine the trigger objects in order to get down to the final output rate. The baseline option for the installation of all the Level-0 Trigger modular electronics, the DAQ Readout components (FELIX and the Data Handlers) and the HTT electronics in the main underground electronics cavern, USA15. The Dataflow and EF servers will be installed in the surface-level counting room, SDX1. A high-level functional description of the architecture consisting of the three main systems: the Level-0 Trigger System (purple color), the Data Acquisition (DAQ) System (including Readout and Dataflow - green and yellow color respectively), and the Event Filter System (red color) is presented in Figure 1.6.

1.2 The micromegas detectors

The Micromegas detector is a gaseous detector invented by Georges Charpak and Ioannis Giomataris. It consists of two asymmetric regions, the amplification region (128 μm , 40 – 45 kV/cm) and the Conversion/Drift region (5 mm, 0.6 kV/cm) as shown in Figure 1.7. For the NSW micromegas detectors, the two regions are filled with a gas mixture of ArCO₂ (93:7 %) and are separated by a thin metallic mesh called micromesh. The readout strips of the detector are covered by an insulator and a layer of resistive strips to protect the detector from discharges.

Charged particles traversing the drift area ionize the gas and the electrons produced drift towards the mesh. Most of the electrons pass through the mesh and enter the amplification region where the avalanche effect takes place. In this case the electrons reach enough energy to produce new ion/electron pairs that will also ionize the gas. Sparks may damage the detector and readout electronics and/or lead to large dead times as a result of High Voltage (HV) breakdown [10]. The ions produced are moving towards the cathode. The charge is amplified and the induced signal is read out by charge amplifiers located on the front-end boards. Micromegas detectors can be used

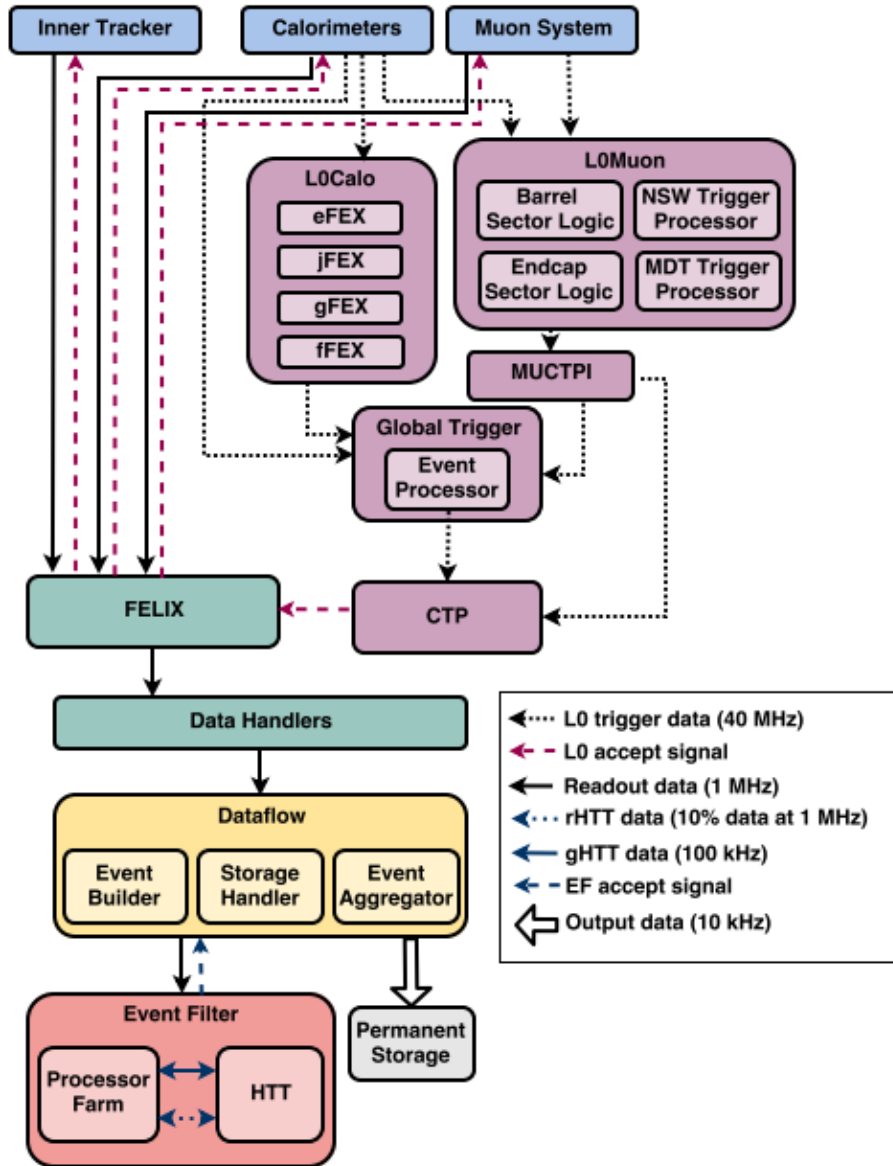


Figure 1.6: TDAQ Phase 2 upgrade architecture.

in high particle fluxes due to the fast evacuation of the positive ions (about 100 ns) immediately above the readout electrode.

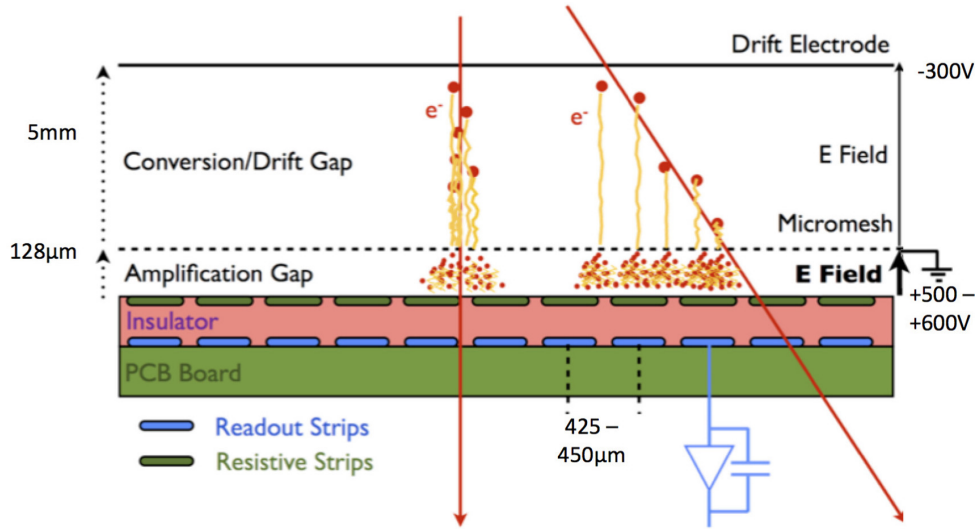


Figure 1.7: Operation principle of the Micromegas detector.

1.3 The sTGC detectors

The sTGC [11] are also gaseous detectors and consist of gold plated tungsten wires and strips and pads both from copper. The wires have a diameter of $50\text{ }\mu\text{m}$ and the potential applied is about 2.9 kV . They have a pitch of 1.8 mm and are placed between two graphite-epoxy cathode planes each at a distance of 1.4 mm from the wires. The cathode planes are made of graphite-epoxy mixture and have a surface resistivity of typically $100\text{--}200\text{ k}\Omega/\text{sq}$. On the outer side of the cathodes, the precision strips (perpendicular to the wires) and the pads are placed, both acting as readout electrodes. Strips have a 3.2 mm pitch (much smaller than the current ATLAS TGC), providing improved angular resolution. Pads have a much larger pitch, of about 80 mm , and are used to identify muon tracks roughly pointing to the interaction point by producing a 3-out-of-4 coincidence, as well as to define a region of interest for which the strips and wires are read out. The chamber is filled with a gas mixture of 55% CO_2 and 45% n-pentane, which has an electron drift velocity of about $3\text{ cm}/\mu\text{s}$ under an electric field of $2.9\text{ kV}/\text{cm}$.

1.4 NSW overall electronics design and specifications

In this section the overall data acquisition and trigger scheme for both detector technologies is described in great detail. An overview representation of the NSW electronics complex is shown in Figure 1.10. The electronics can be divided in two categories, the on-detector electronics located on the detector (harsh radiation and magnetic field environment) and the off-detector electronics located in USA15 (area a few meters away from the detector), consisting of commercial electronics. In this scheme there are three distinct paths: the readout path (common for both micromegas and sTGC), the trigger path for micromegas and the trigger path for sTGC detectors. Due to the different characteristics of both detector technologies (micromegas and sTGCs) three different types of Front-End boards (FE) with various numbers of Front-End Application Specific

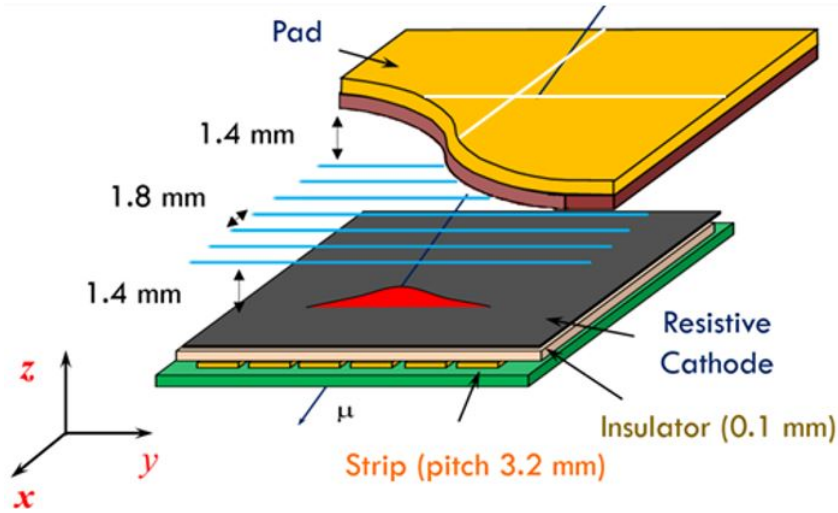


Figure 1.8: *sTGC detector operational principle.*

Integrated Circuit (ASICs) will be fabricated: one for the micromegas which is called MicroMegas Front-End (MMFE8) (the "8" indicates the number of front-end chips), and two for the sTGC, the strip FE (sFE) and pad and wires FE (pFE) boards. Due to the high number of readout strips for micromegas and sTGC detectors, 4096 MMFE8, 768 sFE and 768 pFE will be fabricated.

The readout path consists of the FE, Level-1 Data Driver Card (L1DDC) [12] and the FELIX boards. The trigger path for the micromegas comprises the MMFE8, the Address in Real Time Data Driver Card ADDC [13] board and the trigger processor. Finally, a more complicated scheme for the sTGC includes the pad and wire FE (pFEB), strip FE (sFEB), PAD trigger, Router, L1DDC and trigger processor. The trigger algorithms will be implemented in conventional FPGAs housed in Advance Telecommunication Computing Architecture (ATCA) crates. The output of the trigger processor will be sent to the new sector logic boards, to be combined with the Big Wheel trigger and therefore define the final Level-1 trigger signal.

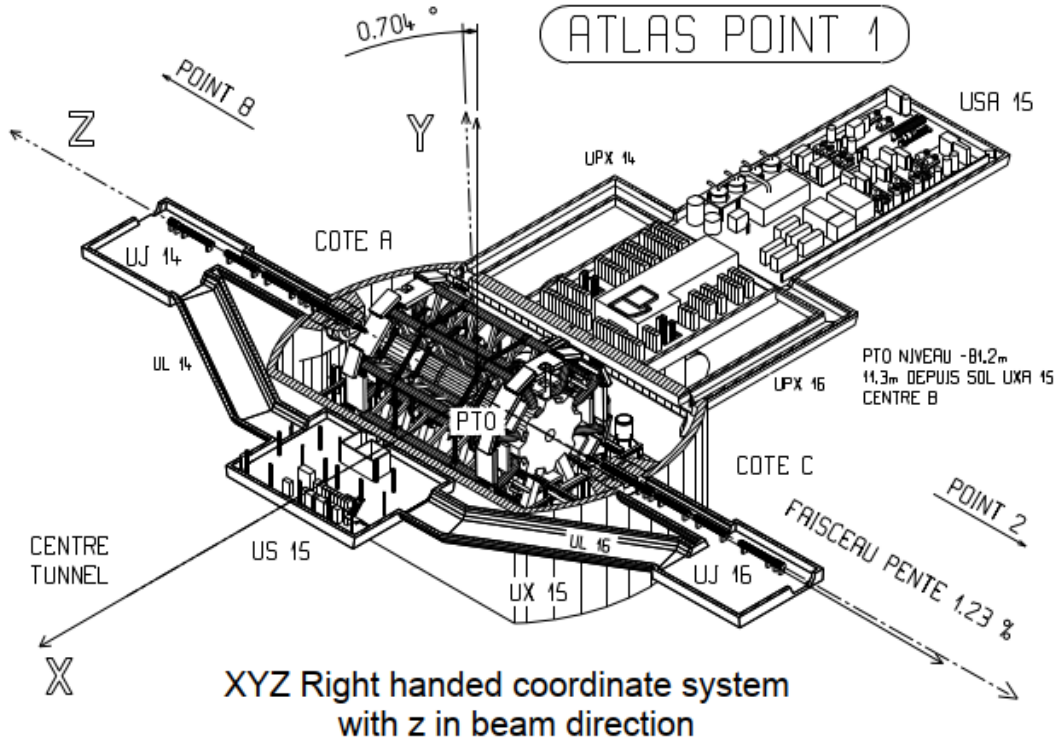


Figure 1.9: The ATLAS detector and USA15 area.

In order to overcome the constraints of bandwidth, latency and radiation tolerance, the front-end electronics will include four new ASICs specifically designed for the NSW: the Trigger Data Serializer (TDS), Address in Real Time (ART) [14], Venetios MicroMegas(VMM) [15] and Read Out Controller (ROC) [16]. The VMM is the front-end ASIC that receives the analogue signals from the detector. Discriminators and Analog to Digital Converters (ADCs) for every channel send data to both the trigger and readout paths. The former is prompt and the latter is buffered awaiting a trigger signal. The TDS and ART are designed to transmit trigger data, while the ROC transmits data to the readout path.

The data from the ROC are received by a Gigabit Transceiver Link (GBT) and sent via optical fiber to a general purpose network with a high-availability interface, called FELIX. All hits in the VMM ASIC are stored until the arrival of a trigger and then only hits in the Bunch Crossing (BC) close to the triggering BC are selected for transfer to the ROC. The ROC will aggregate data from up to eight VMMs and send it either unfiltered (after Phase 1 of the ATLAS detector upgrade) or filter it based on a Level-1 trigger (after Phase 2). For Phase 2 and the originally planned two-level trigger the ROC buffers the Level-0 accepted (LOA) events until a Level-1 Accept (L1A) trigger is initiated and then data are transmitted to the FELIX through the GBTX [17] and L1DDC. The single-level trigger readout passes all events to the ROC and is serially transmitted directly downstream.

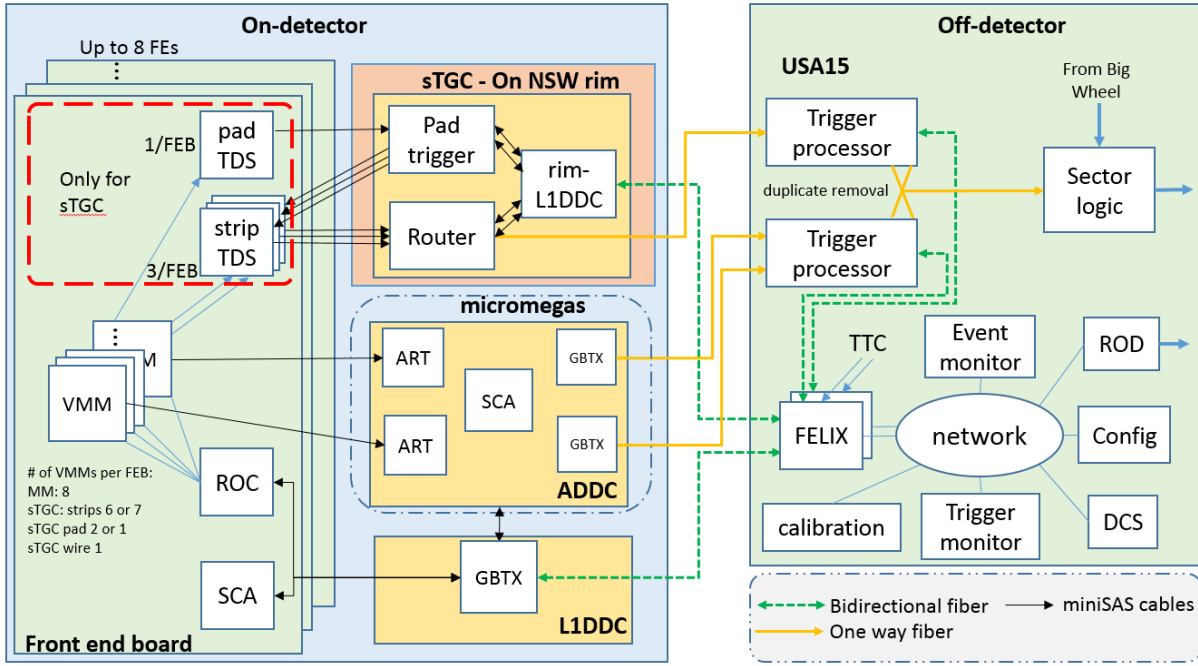


Figure 1.10: Overview representation of the NSW micromegas electronics system.

1.4.1 Data acquisition

The main front-end ASIC is the 64-channel VMM, a common front-end ASIC for both the micromegas and sTGC detector technologies, which provides amplitude and timing measurements and direct output of trigger primitives as well as Level-0 trigger buffering [18]. The ROC ASIC collects the data from multiple VMMs and transmits them through serial links at 320 Mb/s each to the GigaBit Transceiver (GBTX) ASIC. The GBTX can be described as a high speed serializer/deserializer chip that can receive serial data from multiple FEs (the maximum number of FEs depends on the actual bandwidth as it is described in section 1.4.1) on one side and transmits them to a single fiber at 4.8 Gb/s. The data from the GBTX are transmitted to FELIX network interface and then finally to the Read Out Devices. The BC (a synchronous 40 MHz) clock, trigger and configuration data are transmitted from FELIX and through GBTX to all on-detector electronics boards. The board that houses the GBTX is the L1DDC. The FEs will house a number of VMMs (8 for the micromegas and up to six for the sTGC detectors) one ROC and one Slow Control Adapter (SCA) ASICs [19]. As it is described in section 1.4.1, the SCA integrates a number of interfaces and is used for configuring and monitoring all ASICs and boards of the NSW electronics housed on the detector.

VMM

Venetios MicroMegas (VMM) ASIC was designed at Brookhaven National Laboratory by Gianluigi de Geronimo and his microelectronics design group specifically for the Micromegas detectors. Later it was decided to use the VMM, also, for the sTGC detectors. The first version of the ASIC (VMM1) was fabricated in 2012. It was made up of 500k

MOSFET (8 k per channel) in an area of 50 mm^2 . It used a two-phase readout and did not contain any (ADCs). The VMM1 was tested under irradiation for Single Event Upset (SEU) and specifically on the response of the configuration registers. During these tests two VMM1s were exposed in a neutron irradiation environment using the TANDEM Van Der Graaff accelerator at NSCR Demokritos, Athens, Greece. During the tests a number of SEUs was measured at a measured cross section of $(4.1 \pm 0.8) \times 10^{-14} \text{ cm}^2/\text{bit}$ for each VMM. When extrapolating this value to the luminosity expected in Run 3, the occurrence is roughly six SEUs/min in all the read-out system comprising 40,000 VMMs installed during the Phase-I upgrade [20].

The second version of the chip (VMM2) was fabricated in 2014. This version integrates ADCs and had much higher functionality and complexity compared to VMM1. The density of the MOSFETs increased to 5 M MOSFETs (>80 k per channel) in an area of 115 mm^2 . The last version of the ASIC was the VMM3 which was fabricated in 2016 and was revised to VMM3a in 2018. It numbers 10 M MOSFETs (>160 k per channel) in an area of 130 mm^2 . Figure 1.11 shows the dies for the three versions of the VMM ASIC. The differential standard changed to Scalable Low Voltage Signaling (SLVS) for compatibility with the other ASICs of the NSW and SEU mechanisms were implemented for robustness. Dual Interlocked Cells (DICE) were used for the protection of the configuration register, and Triple Modular Redundancy (TMR) for the state machines and the Bunch Crossing ID (BCID) registers.

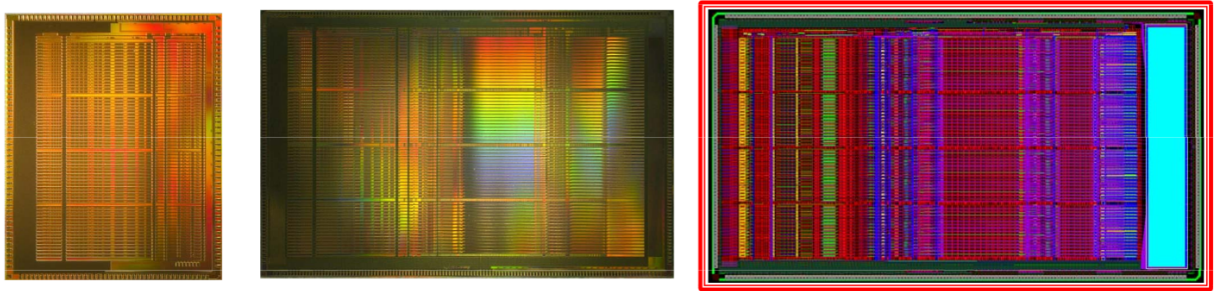


Figure 1.11: Left VMM1, center VMM2 and right VMM3 dies.

The VMM is a radiation tolerant ASIC fabricated in the 130 nm Global Foundries 8RF-DM process. It is a 400 Ball Grid Array (BGA) with 1 mm pitch and the device dimensions are $21 \text{ mm} \times 21 \text{ mm}$. The VMM uses a single power supply of 1.2 V and is composed of 64 front-end channels with highly configurable parameters. As shown in Figure 1.12, each channel has a low-noise Charge Amplifier (CA), a shaper with baseline stabilizer, a discriminator with trimmer and neighbor enabling logic, a peak and time detector and some extra logic.

The CA can operate in a wide range of input capacitances. It integrates a test capacitor and has adjustable gain, peaking time and polarity. The input MOSFET is a p-channel with a gate area of $L \times W = 180 \text{ nm} \times 10 \text{ mm}$ (200 fingers, $50 \text{ }\mu\text{m}$ each) biased at a drain current $I_D = 2 \text{ mA}$. The gain is adjustable to eight values (0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC). The adjustable polarity for processing either a positive or negative charge is optimized for a capacitance of 200 pF and a peaking time of 25 ns. The shaper is a third-order designed in delayed dissipative feedback and has adjustable peaking

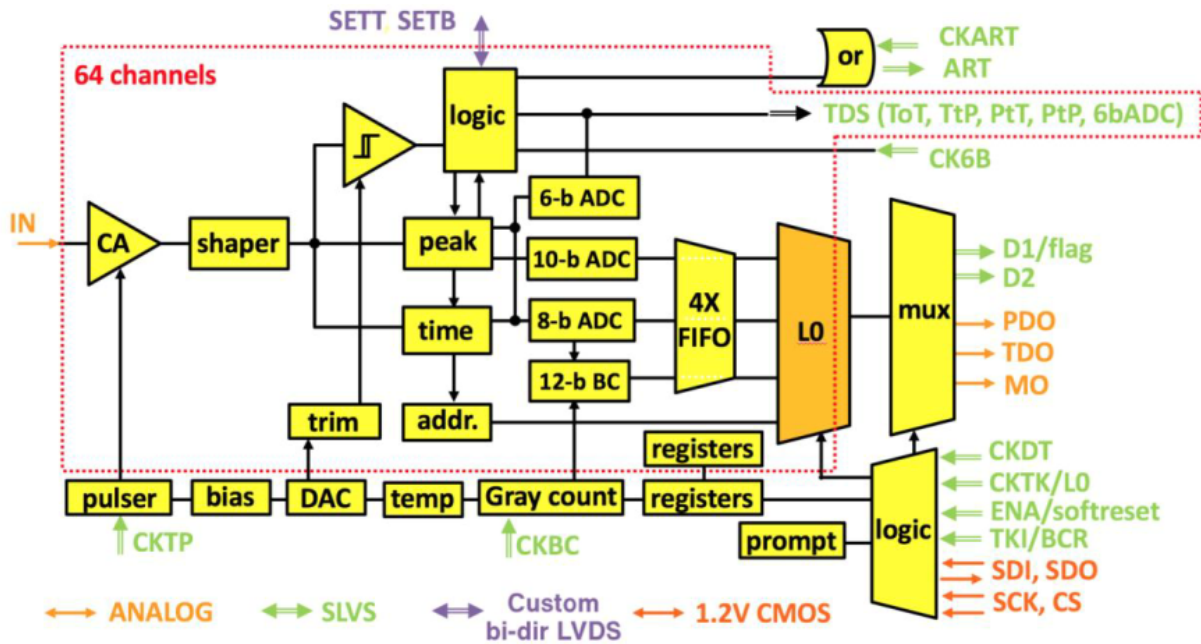


Figure 1.12: *The VMM3a architecture.*

time of four values (25, 50, 100 and 200 ns) and band-gap referenced baseline. The peak amplitude measured by the peak detector is stored in analogue memory. The time detector measures the peak timing using a Time-to-Amplitude Converter (TAC), a voltage ramp that starts at the time of the peak and stops at a clock cycle of the BC clock. Then, TAC value is stored in an analogue memory and the ramp duration is adjustable to four values of 60, 100, 200 and 400 ns. The peak and time detectors are followed by three low-power 6,8,10-bit ADCs. The VMM has two different modes of operation; the two phase analog mode and the continuous mode. On the two phase analog mode, data are stored while the VMM is in the acquisition mode and readout only after VMM is switched to the readout mode. After the readout is complete acquisition process is re-enabled. In the continuous mode the simultaneous read and write of data with a maximum rate of 4 MHz is possible. Moreover each channel has a dedicated digital output for Time-over-Threshold (ToT), Time-to-Peak (TtP), Peak-to-Threshold (PtT), Pulse-at-Peak (PtP) measurements, including also a 6-bit ADC. Some common features are the bias circuits, a temperature sensor, a test pulse generator, two 10-bit Digital to Analog Converters (DACs) for adjusting the threshold and test pulse amplitudes, a mixed-signal multiplexer, the control logic and the ART which consists of dedicated digital outputs (flag and address) for the first above-threshold event. The VMM has 64 parallel prompt data outputs from all channels with selectable format and three multiplexed outputs (Monitor Output-MO, Time Detector Output-TDO, Peak Detector output-PDO for analog amplitude and timing). The bottom side of the MMFE8 board is shown in Figure 1.13. On the upper part the eight VMMs are visible, on the lower part (center and left) the ROC and the SCA (center and right).

The bottom side of the sFEB board is shown in Figure 1.14(a) and the bottom side of the pFEB in 1.14(b). For the sFEB, on the lower center and upper right corner the three TDS ASICs are visible. The ROC ASIC is located at the center top-right and the

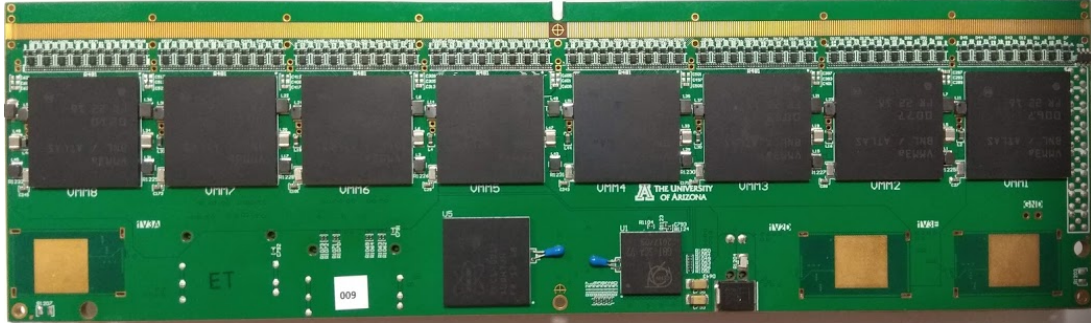
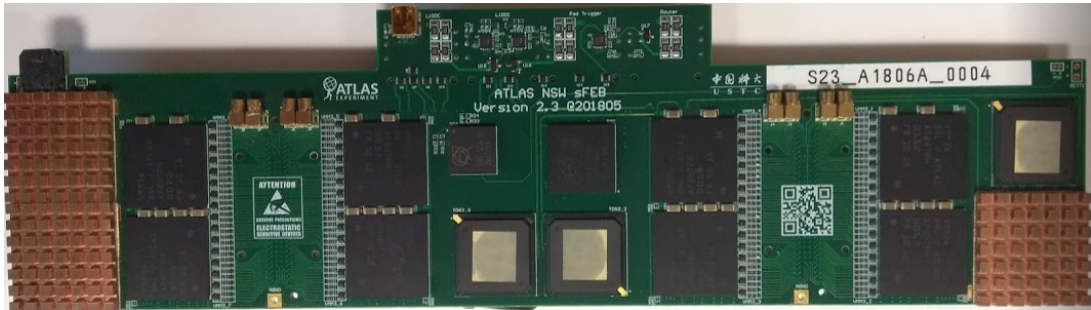


Figure 1.13: Bottom side of the MMFE8 board.

SCA at the center top-left side. The eight VMMs on the left and right of the board are also visible. For the pFEB, from left to right: the TDS ASIC, the three VMMs, the ROC and the GBT-SCA ASIC are shown.



(a)



(b)

Figure 1.14: On (a) the bottom side of the sFEB and on (b) the bottom side of the pFEB are illustrated.

ROC

The data from various number of VMMs (up to eight) are transmitted to the ROC ASIC that merges the incoming hits, reformats the data, adds headers and interfaces with the L1DDC. The data transfer from the VMMs to the ROC happens via two serial lines (even bits on one, odd bits on the other) running at 160 MHz with Double Data Rate (DDR) each, giving a total bandwidth of 640 Mb/s.

Input				RD = -1	RD = +1
	DEC	HEX	HGF EDCBA	abcdei fghj	abcdei fghj
K28.5 †	188	BC	101 11100	001111 1010	110000 0101

Figure 1.15: The K28.5 comma character.

The Readout Controller supplies the clock for this transfer. 8b/10b encoding is used with at least one comma character, K28.5 shown in Figure 1.15, is transmitted continuously between event data. The 8b/10b encoding reduces the effective bandwidth to 512 Mb/s. The block diagram of the ROC ASIC is shown in Figure 1.16.

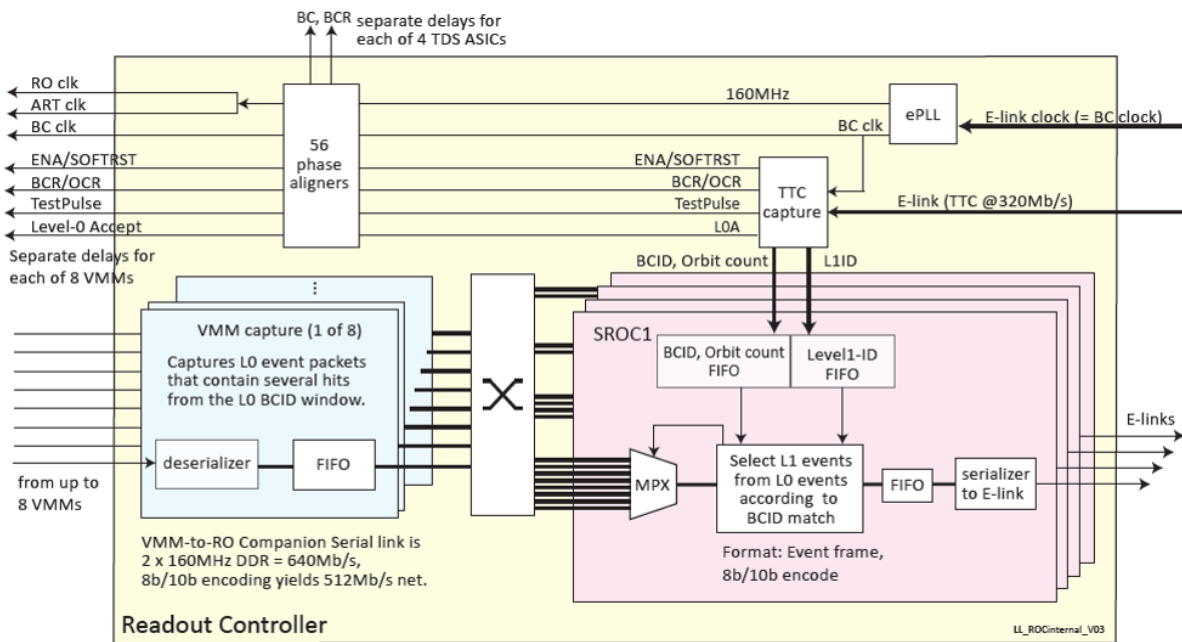


Figure 1.16: The ROC architecture.

The L0A selects the data to be sent to the ROC while the L1A is used by the ROC to select data for readout to FELIX. For single-level trigger readout (rate up to 1 MHz) both L0A and L1A are sent at the same BC. For a two-level trigger, the L0A rate can be up to 1 MHz but the L1A rate will be less. For the data transmission to the Gigabit Transceiver (GBTX) ASIC of the L1DDC, differential lines are used each running at 80, 160 or 320 Mbps using one lane, or 640 Mbps using two lanes. In order to have data rates greater than 640 MHz from one Readout Controller, as are needed at the inner radii of both detectors, several differential pairs must run in parallel. The ROC therefore has four independent sub-Readout Controllers, sROCs, each with a dedicated double-lane differential pair and configurable data rate, as shown in Figure 1.16. For flexibility, the ROC has a crossbar that allows routing up to eight VMMs to up to four different sROCs.

L1DDC and GBTX ASIC

The GBTX ASIC as part of the L1DDC board is described in great detail in this Section. The L1DDC is an intermediate board that implements a bidirectional link with the USA15 and especially with FELIX. The L1DDC is connected with eight MMFE8 and three s/pFEB boards and for the micromegas case also with the ADDC board. In total, 1024 L1DDC boards will be used for the upgrade of the NSW (512 for the micromegas detectors and 512 boards for the sTGC detectors).

Commercial Off The Shelf components (COTS) are typically not sufficiently radiation resistant and, in particular, quite susceptible to SEUs caused by energetic ($E > 20$ MeV) hadrons. For this reason the CERN microelectronics group has been developing a radiation hard chipset, the GigaBit Transceiver (GBT). This chipset consists of the GBTX ASIC, the versatile optical transceiver (VTRX) (which is formed by the Gigabit Laser Driver (GBLD) [21] and the GigaBit Transimpedance Amplifier (GBTIA) [22]) and the SCA.

The GBTX can be used to implement multi-purpose high speed (3.2 – 4.48 Gb/s user bandwidth) bidirectional optical links for high-energy physics experiments. It provides three "distinct" data paths for Timing, Trigger and Control (TTC) data, Data Acquisition (DAQ) and Slow Control (SC) information (monitoring and configuration data) to the FE electronics and the ADDC boards as shown in Figure 1.17.

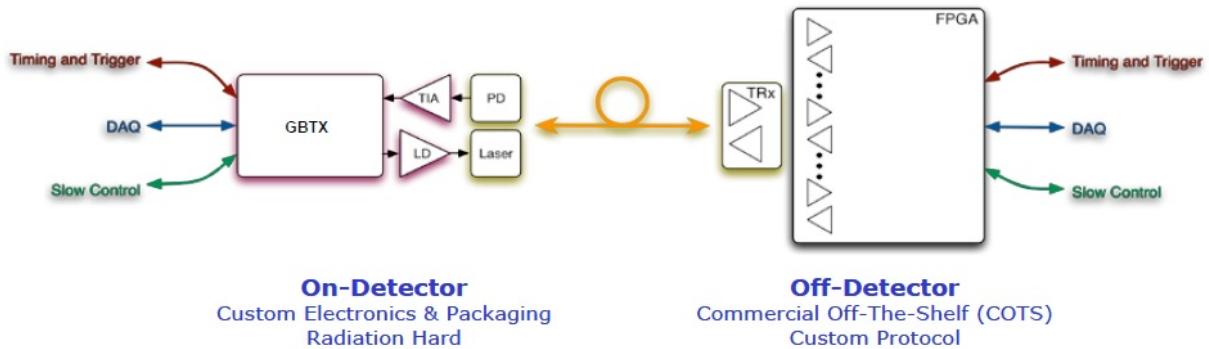


Figure 1.17: Overall functionality of the GBT chipset.

The GBTX ASIC is fabricated with the 130 nm technology. It utilizes a 400 pin BGA package with 0.8 mm pitch, a single power supply of 1.5 V and a maximum power consumption of 2.2 W. It can be viewed as multiplexing a number of serial links (up to 40) with 80, 160, or 320 Mb/s rates onto one fibre by transferring two, four or eight bits per serial link via an 80-bit word (optionally 112 bits when no forward error correction is used) every 25 ns, for an aggregate GBT bandwidth of 3.2 Gb/s.

The GBTX can be electrically interfaced with the on detector electronics using different topologies. One of these consists of interconnecting the GBTX and a FE device via duplex local Electrical serial links (E-Links). Each E-Link normally consists of three signal lines (differential pairs):

- Differential Clock line (dClk+/dClk-): Clock driven by GBTX to FE module. These clocks can be configured at 40, 80, 160 and 320 MHz.

- Differential Downlink data output (dOut+/dOut-): Data line from GBTX to the FE module.
- Differential Uplink data input (dIn+/dIn-): Data line from FE module to GBTX.

The E-Link data rates are programmable in a per group basis. Within a group, the input and output lanes can be set to work at different data rates and an unused group can be turned off to reduce the power consumption in the corresponding internal logic. As we will discuss in the next sections various data speeds are used in the L1DDC boards. The bit shift in/out order for the E-Link data inputs and outputs is MSB first. For each group the E-Link clock signals can be programmed independently to get any of the following frequencies: 40 MHz, 80 MHz, 160 MHz or 320 MHz. For the NSW the clock frequency that will be distributed to the FEs and ADDC boards will be 40 MHz (Bunch Crossing (BC) clock).

The general architecture of the GBTX ASIC and its main external connections are displayed in Figure 1.18. The GBTX is connected to the GBLD laser driver ASIC and to the GBTIA trans-impedance amplifier ASIC. The Clock and Data Recovery (CDR) circuit receives high speed serial data from the GBTIA. It recovers and generates an appropriate high speed clock to correctly sample the incoming data stream. The serial data is then de-serialized (that is converted to parallel form) and then DECODEd, with appropriate error corrections, and finally DeSCRAMbled (DSCR).

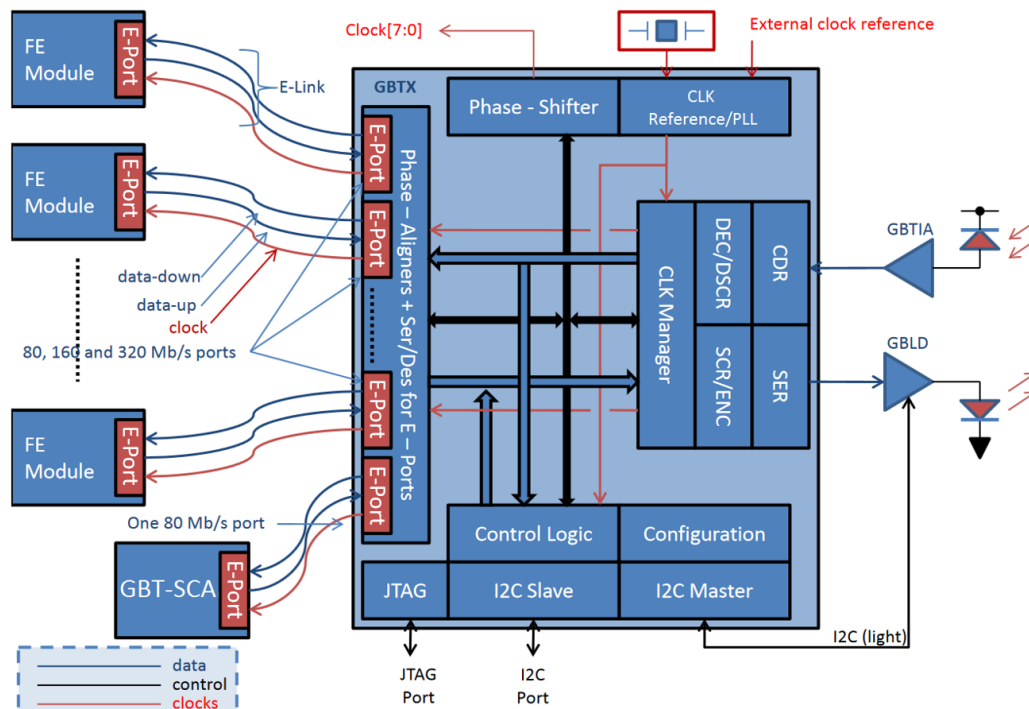


Figure 1.18: GBTX full functionality and connectivity with the FE boards & the rest of the DAQ system.

The GBTX is equipped with a standard I²C slave interface, and is accessed by an I²C master, transmitting data with the correct address. Access to the configuration

registers can be implemented also through the fiber. The GBTX contains a simplified I²C master that can be used to configure the GBLD. Seven registers in the GBTX are reserved for storing the values to write to the GBLD.

At this point is crucial to underline that the GBTX is completely transparent to the data being received/transmitted. This means that any custom or commercial protocol can be implemented for the communication between the FEs and the back-end system.

Phase delays between the FEs and GBTX depend on the system configuration, cable lengths and various delays in the FE circuits. It is thus necessary that GBTX provides a phase adjustment/alignment mechanism for adjusting the phases of the incoming data signals so that data is sampled reliably in the middle of the eye-opening. The phase alignment circuit has three different modes of operation: the training mode, the automatic mode and the static phase selection. Both training and automatic mode are not recommended for environments where SEUs are a concern.

- When in the static phase selection mode the user has to set, for each active input ePort, the required phase. Choosing the correct phase is critical for error free operation of the system where the GBTX is being used.
- The training mode is used when the user wants to have the chip guessing the optimum sampling phase but also wants to freeze phase tracking for the remaining of the data transmission operation. The training mode consists thus of two phases: the training phase where the user sets the train bit to "1" for each channel he wants to train, and the hold phase (freeze) where training of the channels is halted by setting the train bit to "0" for all channels. It is also mandatory to have data transitions on the input ePorts while the individual channels are being trained. Registers are triplicated for SEU protection, so to set a channel to be in the training mode three registers need to be written.
- In automatic mode the phase-aligner automatically selects the optimum phase for each channel and also automatically tracks any phase drift that might occur during system operation. However this phase tracking is limited to $\pm 3/8$ of the E-Link bit period. Under normal circumstances this range should be enough to compensate most system drifts. However, if the phase drift exceeds these values the phase-aligner needs to be reset to select a new optimum sampling value.

The GBTX is equipped with 366 electrical programmable fuses (eFuse) registers. eFuse is a technology invented by IBM which allows for the dynamic real-time re-programming of chips and ASICs. The eFuses use electrically programmable PMOS gate oxide anti-fuses to provide a flexible solution for performance tuning, memory repair and the updating of configuration and version data. On the GBTX each of the readable/write-able register has a corresponding E-fuse register. Upon powering on, the eFuse registers copy its values to the read/write registers.

FELIX

FELIX will be used as gateway between dedicated links connecting to detectors and trigger electronics, links providing timing and trigger information, and a commodity

network (Ethernet or Infiniband). Software running on server PCs connected to a commodity network - using COTS switches - will interact via FELIX with on-detector and trigger electronics for configuration, control, monitoring and calibration. Via FELIX event data to be read out will be passed to server PCs where software will build event fragments, which will be in turn passed on to the Read Out System (ROS), a subsystem of the ATLAS DAQ system that receives and buffers data from all sub-detectors and trigger systems. FELIX is basically a Peripheral Component Interconnect express (PCI-express) custom made board integrating a Xilinx Virtex-7 family FPGA and eight miniPODs. This means that FELIX is capable of interfacing with 48 bidirectional GBT links (twelve links for each miniPOD). Four mini Parallel Optical Device (miniPODs) (two RX and two TX) are connected to a 24 Multi-fiber Termination Push-on (MTP24) connector and then to a patch panel with Lucent Connector (LC) outlets. FELIX receives the TCC data from the TTCvx module via a Straight Tip (ST) fiber connector. In Figure 1.19 the Virtex-7 FPGA (center), the eight miniPODs (left and right of the FPGA), bottom the PCI express and left the MTP and ST connectors are visible.



Figure 1.19: *The Brookhaven National Laboratory BNL-712 PCI express board.*

SCA

To configure and monitor the VMM, TDS and ROC ASICs but also the FPGAs the GBT-Slow Control Adapter (GBT-SCA) ASIC will be used. The GBT-SCA ASIC is an integrated circuit built in a commercial 130 nm CMOS technology and is the part of the GBT chipset. It implements a point-to-multi point connection between one GBT optical link and several front end ASICs. The GBT-SCA is usually connected to a dedicated electrical port on the GBTX ASIC that provides 80 Mb/s of bidirectional data traffic. If needed, more than one GBT-SCA ASIC can be connected to a GBTX using a regular electrical port thus increasing the control and monitoring capabilities in the system. The GBT-SCA features several I/O ports to interface with the embedded front-end ASICs.

The GBT-SCA implements different interfaces like the Joint Test Action Group (JTAG), Serial Peripheral Interface (SPI) and the Inter-Integrated ("I²C") which allow the configuration of the ASICs while features an ADC for monitoring input signals. There are sixteen I²C buses, one JTAG controller port, four 8-bit wide parallel-ports, a memory

bus controller and an ADC to monitor up to eight external analogue signals, as shown in Figure 1.20. All these ports are accessible from the counting room electronics, via the GBT optical link system. Special design techniques are being employed to protect the operation of the GBT-SCA against radiation induced Single-Event-Upsets to a level that is compatible with phase-2 running.

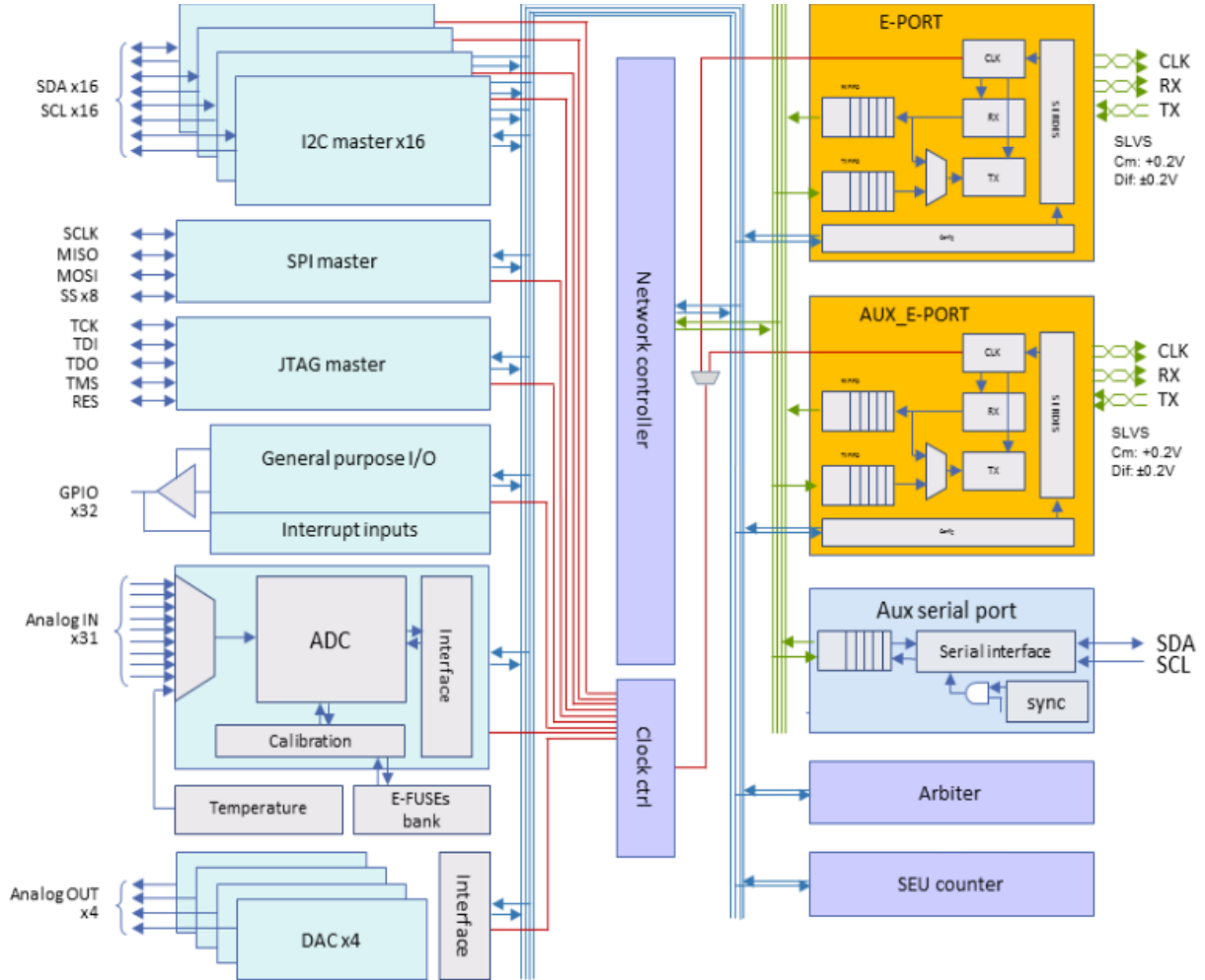


Figure 1.20: The SCA architecture.

The GBT communication is transparent to the slow control protocol. The GBT encodes slow control packets in the counting room, carries it on the optic fibers interlaced with the rest of the traffic, and it delivers the SCA packets unmodified to the GBT-SCA. All on-detector electronics have a SCA for on-board ASIC configuration and environmental monitoring.

1.4.2 micromegas trigger

For the micromegas case the FEs are also capable of driving the ART signals to a separate transmission line for every LHC bunch crossing of 25 ns. The ART signals of the eight FE boards are multiplexed into the ADDC board.

For the micromegas trigger path the responsible board is the ADDC which receives the ART data (the address of the strip of the first hit) from 64 VMMs (eight MMFE8s). A priority based hit selection is implemented in real time, and the selected data will be sent to trigger processors. The basic plan for the ADDC is to use two customized ART ASICs, see Figure 1.20 for a schematic diagram, to deserialize and align the 64 channels of ART data (32 channels for each ART) and complete the hit selection processing. After the hit selection processing is finished, the selected data from each ART ASIC will be sent to one corresponding GBTX. One Versatile Twin-Transmitter (VTTX) module with two fiber cables will be used to transmit the data to the micromegas trigger processor via the two GBTX chips of the ADDC board. A GBT-SCA ASIC will be used also for the configuration and monitoring the ART and GBTX ASICs. In total 512 ADDC boards will be used in the NSW.

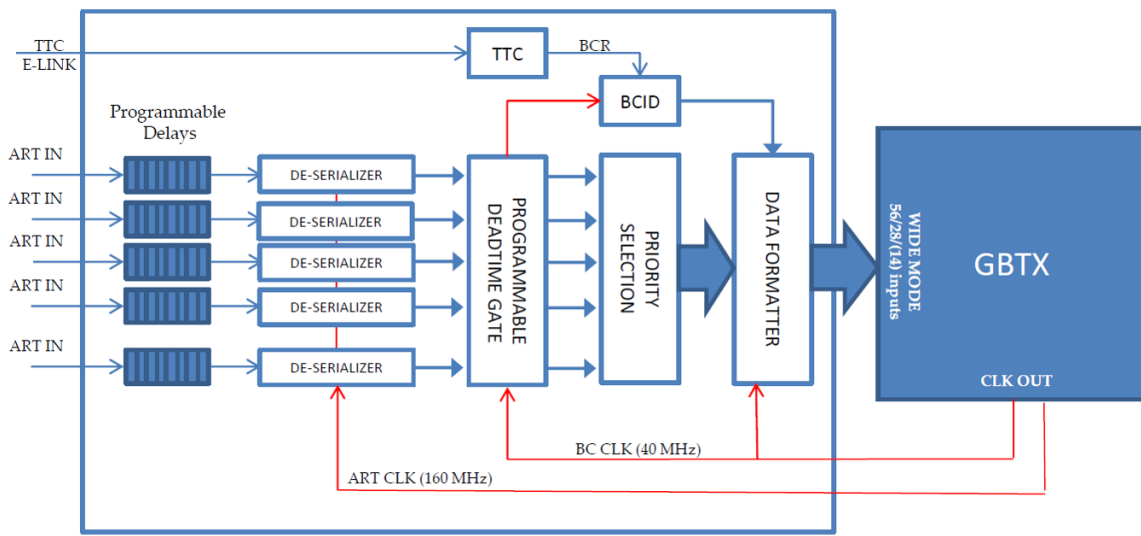


Figure 1.21: The ART architecture.

The NSW trigger signal is based on track segments produced online by the sTGC and micromegas chambers comprising the NSW detectors. These candidate track segments are input to the new sector logic that uses the information to corroborate trigger candidates from the Big Wheel TGC chambers. The sector logic sends Level-1 trigger candidates to the ATLAS Muon Central Trigger system. The trigger system for the end-cap muon detectors in ATLAS currently relies on the use of the middle layer and the reconstruction of projective segments pointing to the IP by the TGCs.

1.4.3 sTGC trigger

The NSW sTGC trigger system makes use of coincidences of detector Pads to identify regions where a muon candidate was detected. To reduce the amount of data sent to the off-detector trigger processors, only sTGC strip information coming from the regions selected by the pad trigger logic are transmitted off-detector. The TDS ASIC and Router electronics handle the serialization and subsequent routing of active trigger data signals from the front-end of the sTGC detectors to track-finding processors. The L1DDC placed

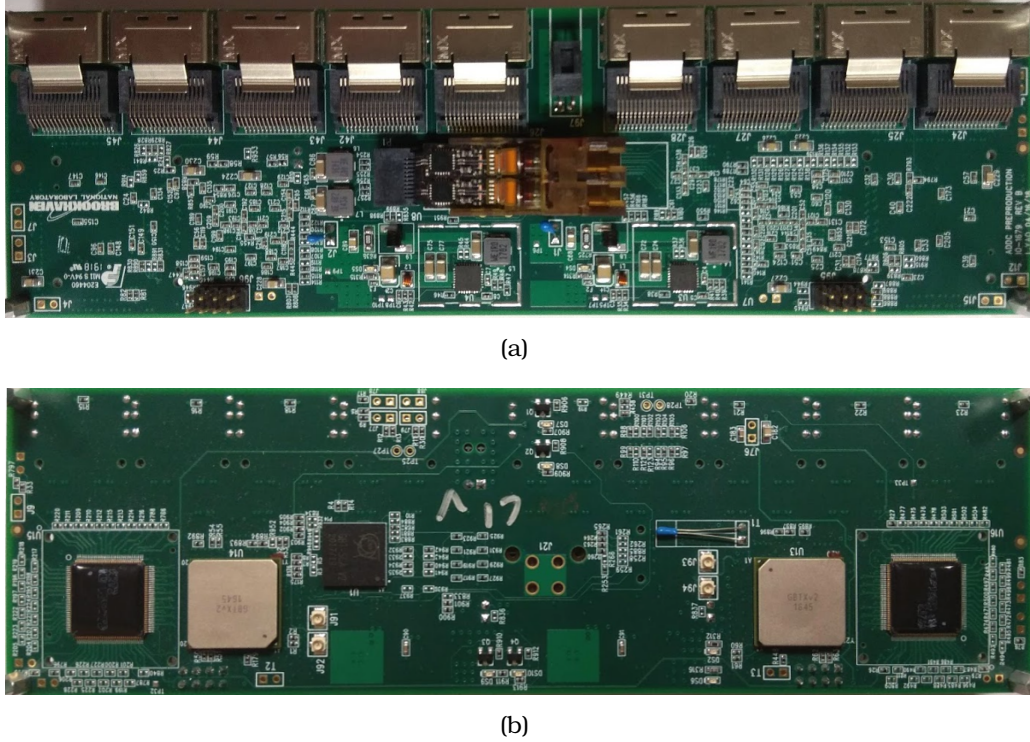


Figure 1.22: (a) Top side, (b) bottom of ADDC board.

on the rim of the wheels will be used to provide high quality clocks, configuration or additional data to the pad trigger and router boards but also to readout the Level-1 data.

TDS ASICs are placed on the FE for the sTGC detectors (one for the pFEB and three for the sFEB). The time-over-threshold from each channel of the VMM is sent to the pad TDS (pTDS) ASIC. This ASIC has 104 inputs that are divided into 13 groups with eight pads per group and there is a configurable local BC clock for each group. Timing is adjustable in steps of 3.125 ns within a range of 25 ns since different pads can have very different trace length. In case there is a pad fired, the pad TDS uses the leading edge of the pulse signal to sample the BC clock in the group it belongs to obtain the BCID for that pad. The sampled BCIDs are kept in the ring buffers. At the end of BC k , the TDS will check the ring buffer of each channel to check if there is a hit with a BCID equals to k . A channel is marked as "yes" as long as there is a match in the ring buffer, otherwise, a "no" will be recorded. All data except the header bits are scrambled to keep them DC-balanced, serialized and transmitted with a speed of 4.8 Gb/s. DC-balancing is achieved by using a self-synchronizing scrambler that "randomizes" the data pattern and guarantees a proper distribution of 0's and 1's in the data stream.

From the pTDS, pad signals are sent to the pad trigger logic, which looks for hit coincidences in a tower of logical Pads within one BC. A three out of four majority logic is used for both sTGC quadruplets to select a muon candidate. If a candidate track is identified, the pad trigger logic selects the band of strips in each layer (band-ID) associated with the triggered pads, and distributes the IDs of the bands to the sTDS. Each wheel is equipped with 16 Pad trigger logic boards on its rim, one per sector, for a

total of 32 boards. The rim is a few meters away of the interaction point; the radiation and magnetic fields are not so strong, which makes it possible to implement the PAD logic in commercial FPGAs.

The 6-bit charge information from 128 VMM channels is sent to the strip TDS (sTDS) ASIC. The design of the sTDS can be divided into three major parts: VMM interface, Preprocessor, and Serialization. The VMM interface reads in the VMM output data and stores it in ring buffers awaiting track road information from the pad trigger logic. The Preprocessor performs the BCID and pad trigger matching and selects strips within the pad road for transmission to the router. The Serialization part prepares the trigger data and serializes it for transmission to the on-rim router.

The sTDS then transmits the strip charges, BCID, band-ID, and ϕ -ID (total 120 bits) on twinax serial copper wires to the signal packet Router on the periphery of the wheel. The Routers remove NULL data and forward valid strip data to a limited number of optoelectronic outputs. The data are sent by fiber to track finding processors in USA15 where centroids and track segments are calculated and sent to sector logic to be combined with candidate tracks from the Big Wheel. Router boards will be placed on the rim inside commercial boxes along with PAD and RIM-L1DDC boards and will use also commercial FPGAs. Eight router boards will serve a NSW sector resulting in 256 router boards.

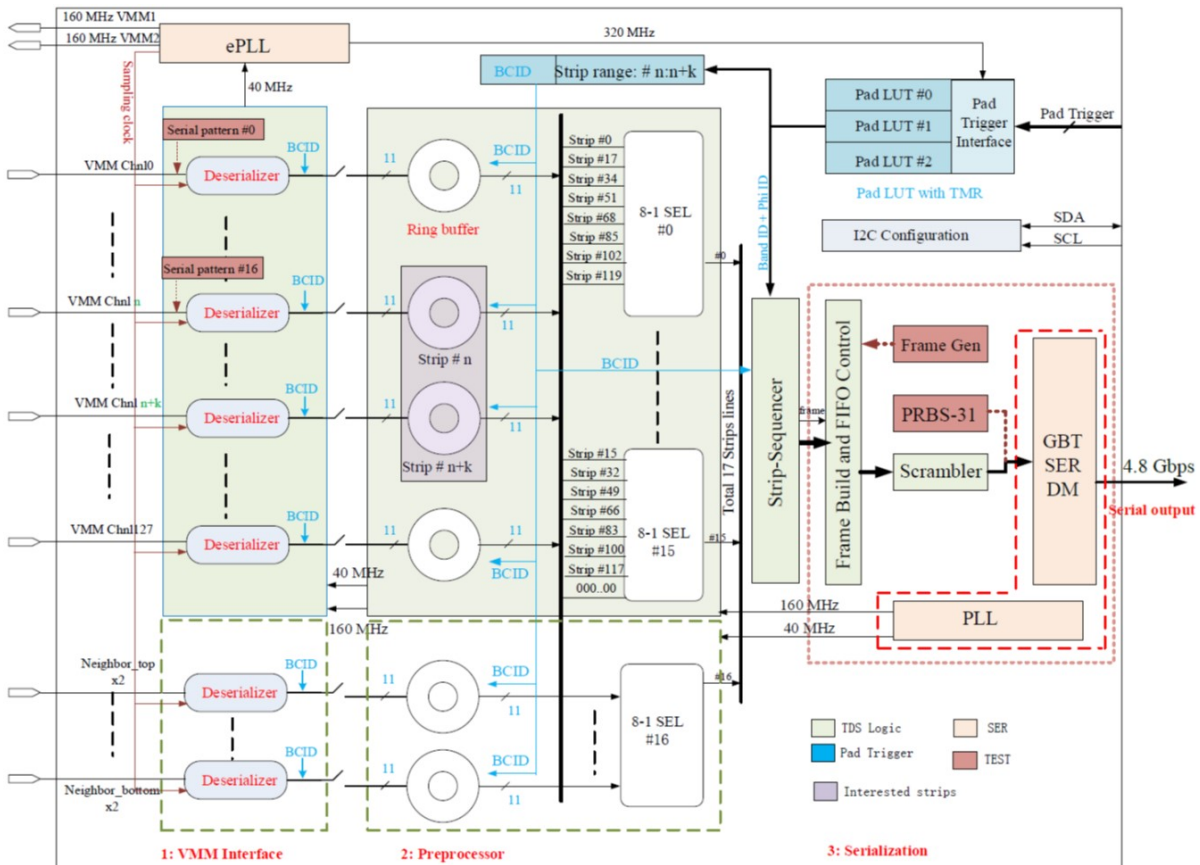


Figure 1.23: The TDS architecture.

For the trigger path of the micromegas detectors the ADDC will receive the ART

Table 1.1: *Signal attenuation on different frequencies and different cable lengths for the 3M twinax SL8800 Series.*

Frequency (GHz)	0.50	1.0	2.0	5.0	10.0	15.0	20.0
Tin Plating (dB/m)	-0.90	-1.4	-2.2	-4.0	-7.5	-10.9	-14.6
Silver Plating (dB/m)	-0.85	-1.2	-1.7	-3.2	-4.9	-6.8	-8.8

data from 64 VMMs (eight micromegas front-end boards). The first arrival hit address is selected in real time and the selected data will be sent to the trigger processors.

1.4.4 Connectivity and compatibility

E-Links use the 400 mV (SLVS-400) [23] standard, with signal amplitudes that are programmable to suit different requirements in terms of transmission distances, bit rate and power consumption. Especially GBTX uses the SLVS in the transmitting side and the SLVS or Low Voltage Differential Signaling (LVDS) standards in the receiving side. The LVDS signals use a differential voltage swing of ± 400 mV centred on 1.2 V. The SLVS standard is also differential but with a reduced voltage swing of ± 200 mV, centred on 0.2 V. For full compatibility with the other boards and in order to avoid using any extra ICs (eg. voltage translators) all ASICs use the same voltage levels (SLVS-400 standard).

The connectivity of the L1DDC board with the other on detector electronics (FE and ADDC boards) will be through the 3M 36 pins mini Serial Attached SCSI (Small Computer System Interface) (miniSAS) connectors and 3M custom made twinax cables. The small size of the connectors (8.47 mm height and 17.8 mm width) along with the highly routable cables is the reason for choosing them for the update of the NSW. These cables are flat, highly bendable and don't impose any distortion on the signal quality even after multiple bending. On the top of Figure 1.24 the dimensions of the twinax cable from 3M is presented. On bottom left the actual cable and the cross-section are depicted. These cables have four differential lines and four sidebands dedicated for single ended signals. On the bottom right the dimensions of the pcb miniSAS connector are presented.

Two different materials are used for coating the central copper wire of 3M cables, tin and silver. Moreover, custom cables should be produced, for cable lengths above 1 m. For low frequency signals (up to 320 MHz in our case) the signal attenuation is similar on both cables but for the high frequency data, e.g. at 4.8 Gb/s as it is in the STGC trigger chain, attenuation is becoming an issue. The attenuation of the cables with respect to the Frequency and cable length is shown in Table 1.1.

The miniSAS 36 position cable can accommodate up to five receiving and five transmitting differential pairs, as long as one receiving and one transmitting pin dedicated to sideband for single ended signal transmission as shown in Table 1.2. L1DDC and ADDC boards are close together and for that reason 1 m cables will be used. Due to the extremely high cost of the 10-pair twinax cables, it was decided that for the Phase-1 upgrade only eight pairs will be used. The eight pair version utilizes four transmitting

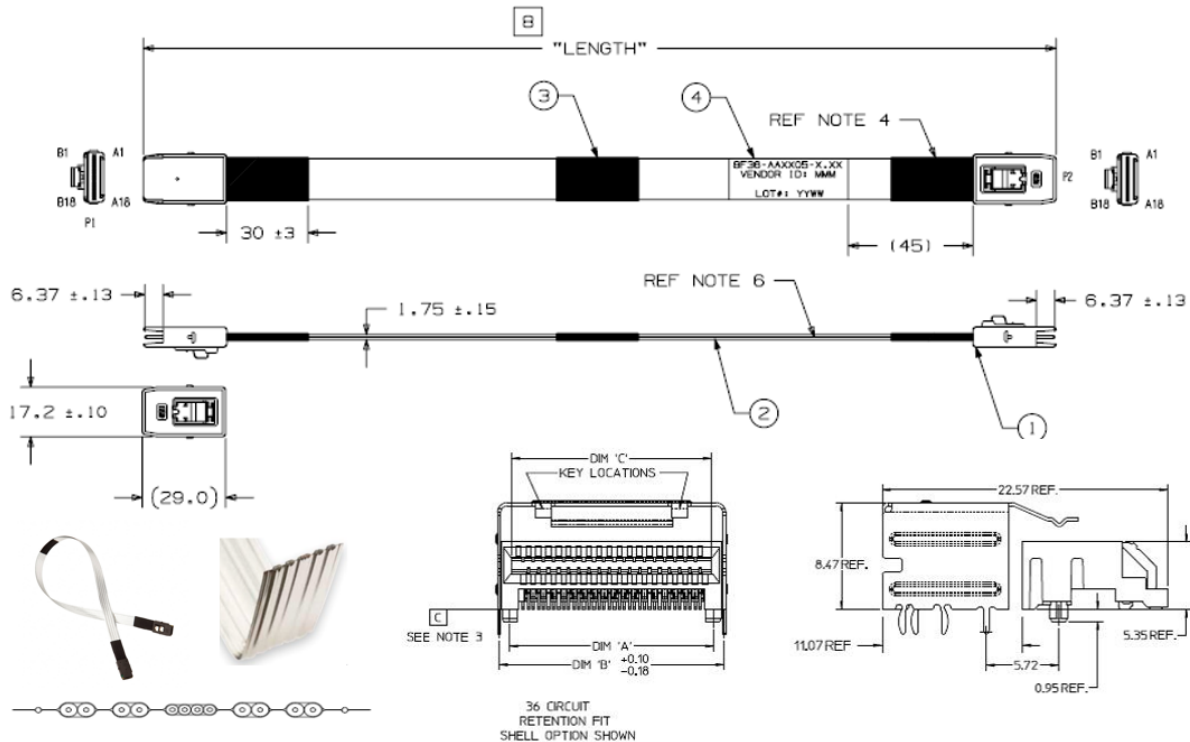


Figure 1.24: *Twinax and miniSAS dimensions.*

and four receiving differential pairs but also four transmitting and four receiving sidebands. For the eight pair version the A9-A11 and B9-B11 pins are sidebands. Since the rate in Phase-1 is relative low the 5th differential pair will not be used. Moreover, tests with four meter twinax cables have shown that sidebands can be used also for differential signal transmission at 320 Mb/s.

1.4.5 Grounding policy

The overall grounding scheme was designed in detail and carefully to avoid any ground loops and potential noise to the FE. For this reason the miniSAS shields should be connected to ground at only one end to prevent ground loops. No DC current should be flowing in the shield, so breaking this should have no negative effect on DC currents. The decision was to ground at the end without sensitive analog electronics so the shield will not act as an antenna bringing in noise to the FE ground. The connection of the shield to the FEs is made through a capacitor. The idea of the capacitor is to provide continuity of the "ground plane" for the AC signals in the twinax pairs. It was thought that any discontinuity of the ground as the signals cross the cable-to-FE board boundary would affect signal integrity. The unused lines cannot be left floating and are tied to ground at same end that the shield is grounded. Connecting them to ground via a capacitor could alter the twinax impedance since mirror currents can now flow in them parallel to the adjacent active twinax. These issues are mitigated by the fact that the twinax signals are well below 1 Gb/s, although a clock is transmitted whose jitter might be increased.

Table 1.2: Pinout of the 3M 36-pin ten-pair miniSAS connector

L1DDC				Front End			
P1		P2		P1		P2	
A1	GND	B1	GND	B1	GND	A1	GND
A2	Rx+	B2	Tx+	B2	Tx+	A2	Rx+
A3	RX-	B3	TX-	B3	TX-	A3	RX-
A4	GND	B4	GND	B4	GND	A4	GND
A5	Rx+	B5	Tx+	B5	Tx+	A5	Rx+
A6	RX-	B6	TX-	B6	TX-	A6	RX-
A7	GND	B7	GND	B7	GND	A7	GND
A8	sideband	B8	sideband	B8	sideband	A8	sideband
A9	GND	B9	GND	B9	GND	A9	GND
A10	Rx+	B10	Tx+	B10	Tx+	A10	Rx+
A11	RX-	B11	TX-	B11	TX-	A11	RX-
A12	GND	B12	GND	B12	GND	A12	GND
A13	Rx+	B13	Tx+	B13	Tx+	A13	Rx+
A14	RX-	B14	TX-	B14	TX-	A14	RX-
A15	GND	B15	GND	B15	GND	A15	GND
A16	Rx+	B16	Tx+	B16	Tx+	A16	Rx+
A17	RX-	B17	TX-	B17	TX-	A17	RX-
A18	GND	B18	GND	B18	GND	A18	GND

**Figure 1.25:** Grounding policy for the NSW electronics.

Below is presented in detail the connectivity that should be implemented for the NSW electronics. For the connection of the L1DDC with FEs, ADDC, PAD trigger and Router boards:

- Unused differential pairs and sidebands should be connected to ground on the L1DDC side and left open on the other boards.
- Ground pins and shields should be grounded on the L1DDC side and connected to ground via a capacitor on the other side.

For the connection of the ADDC, PAD trigger and Router with the FEs:

- Unused differential pairs and sidebands should be connected to ground on the ADDC/PAD trigger/Router side and left open on the FE side.

- Ground pins and shields should be grounded on the ADDC/PAD trigger/Router side and connected to ground via a capacitor on the FE side.

The ground scheme of the micromegas detectors is shown in Figure 1.26. The positive (+550 V) and negative (−300 V) potentials for the resistive strips and drift panels respectively are provided by the High Voltage (HV) Power Supply (PS) through a Resistor-Capacitor (RC) network for filtering. A typical value for the resistor is 100 k Ω and for the capacitor 100 nF. Both return lines (named as HV GND) utilize a resistor of $\sim 100 \Omega$ in series to avoid any ground loops (prevent current from the analog electronics to return through the HV return lines). The mesh and drift panels are connected to the analog ground (AGND) and through the holding screws are attached to the ATLAS safety ground (named SGND) at a single point. Spacer frame is also connected to the SGND. The readout electronics and specifically the input channels of the VMM are connected directly to the readout strips of the detector. MMFE8 board is half digital-analog board with the analog part connected to the analog ground of the detector (AGND). The digital part of the MMFE8 board is connected with the analog part of the board via eight single points. The digital ground is basically the return path of the LV power supply (DGND).

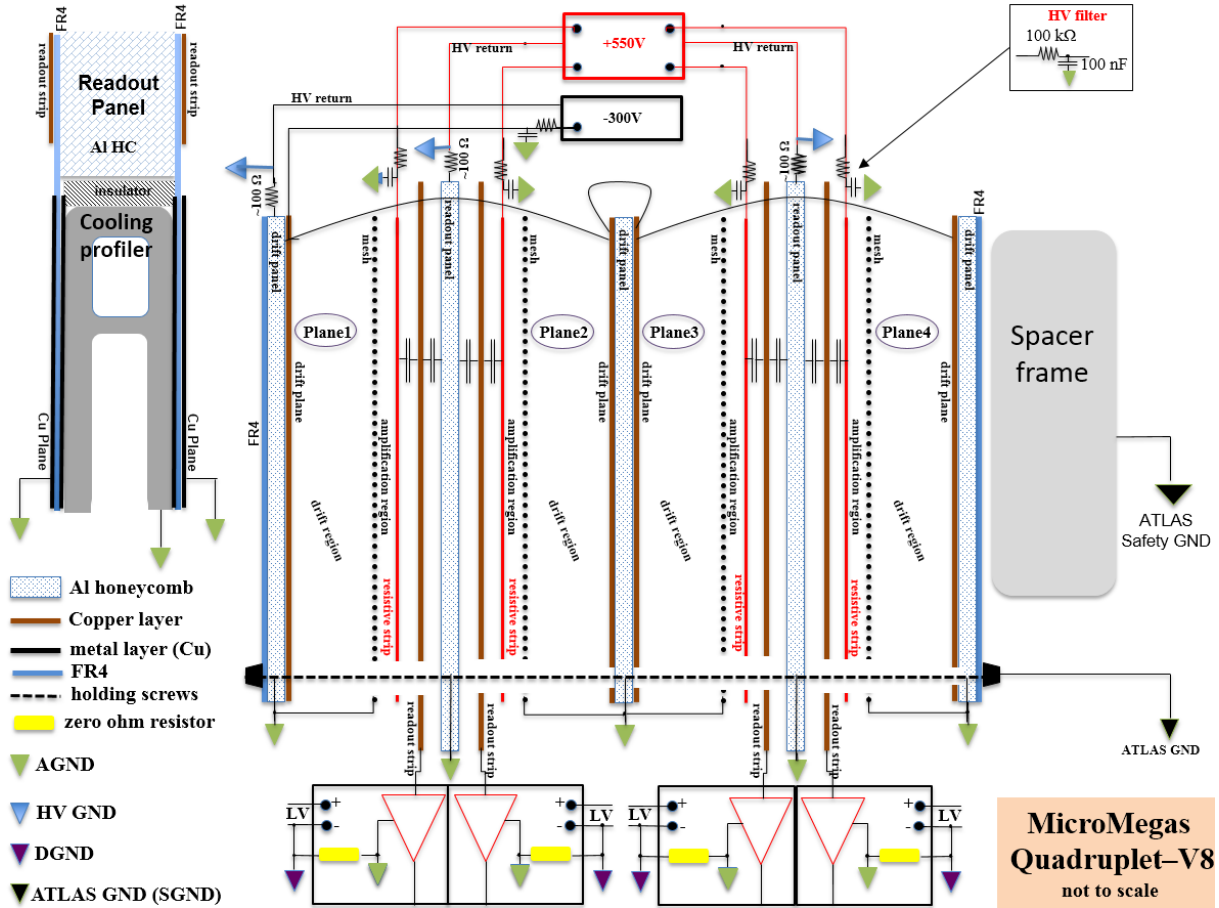


Figure 1.26: Grounding policy for the NSW electronics.

A HV power supply channel is powering on the LM1 or SM1 (five PCBs each). A splitter box is utilized to distribute the power to the PCBs (total ten lines, two per side

of the PCB). Jumpers are used to enable/disable the power to each PCB at the splitter box. The RC filtering ($100\text{ k}\Omega$ resistor and 100 nF capacitor) for the negative power supply and the 100Ω resistor for the return current of the Drift are located inside the splitter box as shown in Figure 1.27. The SM2/LM2 (six PCBs) are powered on with exactly the same topology by using a different HV channel.

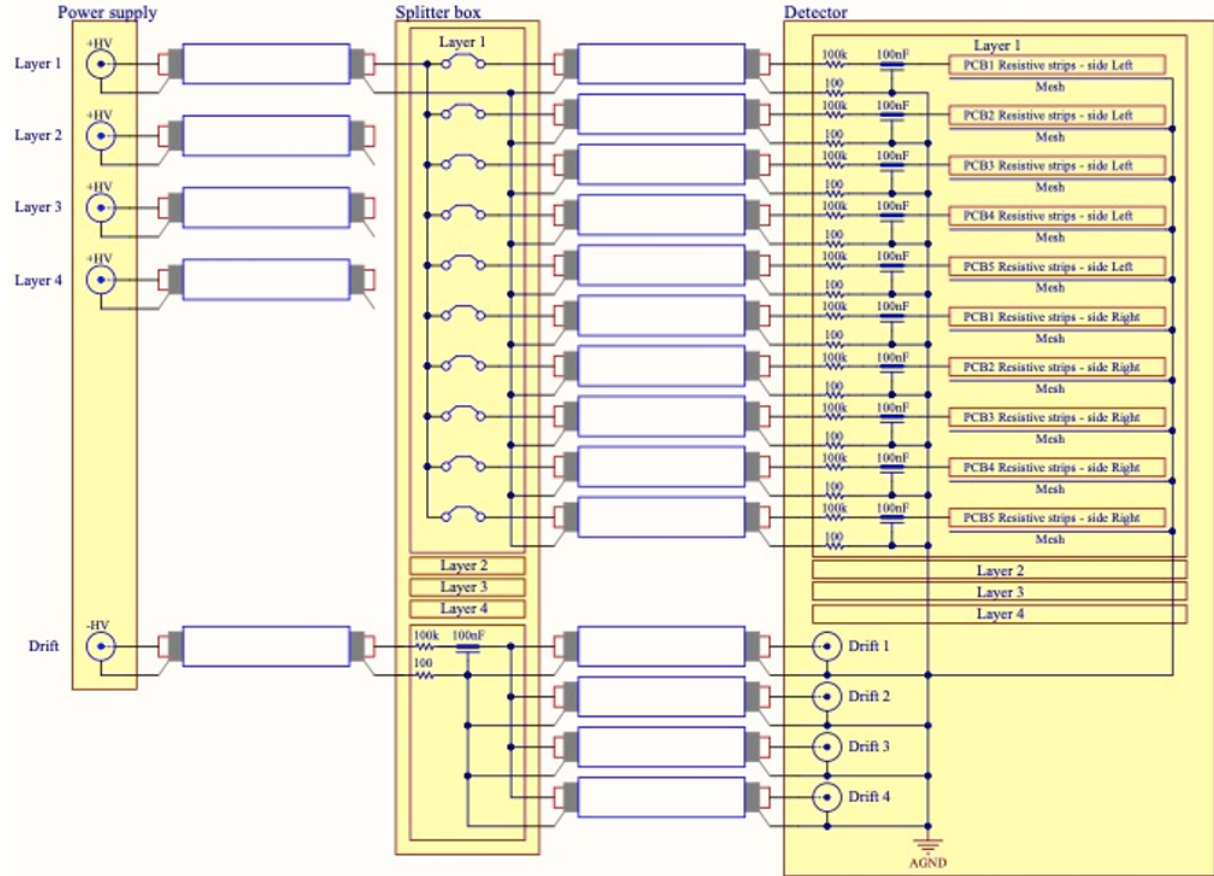


Figure 1.27: HV distribution diagram. Schematics by Givi Sekhniaidze.

1.4.6 Interface and communication protocols

In this subsection the interface of the L1DDC with the on and off detectors electronics is described. The connectivity, communication protocols and standards are also mentioned.

Interface with FELIX

The L1DDC board will be connected to FELIX, housed in the USA15, through the VTRX and/or VTTX optical transceiver/transmitter and multimode fibers. This link can perform bidirectional communication and delivers the Level-1/monitoring data to the USA15 but also sends the TTC/configuration data to the front-ends and ADDC boards. Basically the GBTX can implement three types of frame, the 8B/10B frame, the GBT frame and the wide frame. For the upgrade of the NSW, the GBT frame is

used. The 120-bit GBT frame format, sketched in Figure 1.28, is transmitted during a single LHC bunch crossing interval (25 ns), resulting in a line rate of 4.8 Gb/s. In the transmitter part the data to be transmitted are SCRambed (SCR), to obtain DC balance, and then encoded with a Forward Error Correction (FEC) code, before being serialized and sent to the GBLD laser driver.

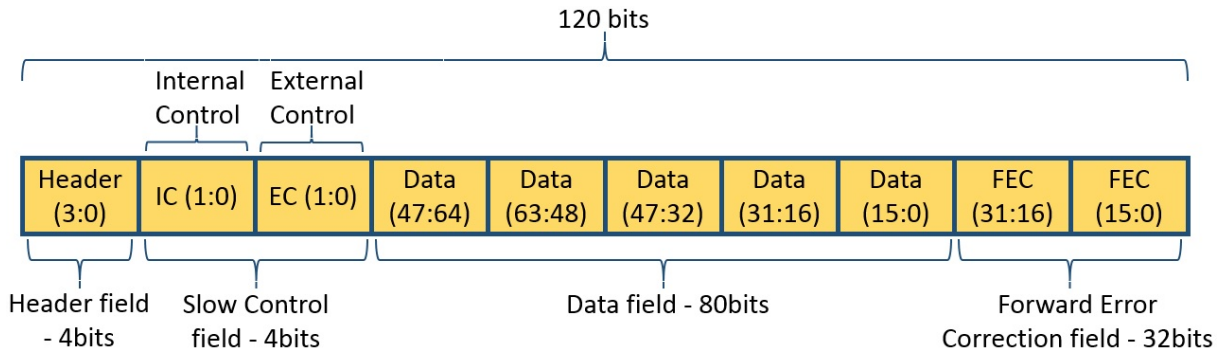


Figure 1.28: The GBT frame.

Four bits are used for the frame Header (H) and 32 are used for FEC. This leaves a total of 84 bits for data transmission corresponding to a user bandwidth of 3.36 Gb/s. Of the 84-bits, 4 are always reserved for Slow Control information (Internal Control (IC) and External Control (EC) fields), leaving 80-bits for user Data (D) transmission. The 'D' and EC fields use are not pre-assigned and can be used indistinguishably for Data Acquisition (DAQ), Timing Trigger & Control (TTC) and Experiment Control (EC) applications. DC-balance of the data being transmitted over the optical fibre is ensured by scrambling the data contained in the SC and D fields. The FEC code is built by interleaving two Reed-Solomon encoded words with 4-bit symbols, each capable of correcting a double symbol error. This, in practice, means that a sequence of up to 16 consecutive corrupted bits can be corrected. The 4-bit frame header is chosen to be DC balanced.

Interface with FE

The L1DDC board will communicate with the ROC and the SCA ASICs on the FE boards. The ROC ASIC collects the data from multiple VMMs and transmits them to the L1DDC. In Figure 1.3 the ROC output frame is illustrated. Before the frames are transmitted, they are encoded using the 8b/10b encoding. Different E-Links will be used for the communication with the ROC and SCA ASICs but over the same miniSAS cable.

On the other side ROC is responsible to collect the TTC data transmitted by the L1DDC board. Table 1.4 presents the format of the (aligned) TTC data word. Bit 0 is the reset for the Level-0 ID (not used in ROC) and Bit 1 is used to reset the SCA via the TTC path. The LOA (bit 2) is forwarded to the VMM chips and Bunch Crossing Reset (BCR) (bit 3) loads the configurable offset in the BCID counter. The Orbit Counter Reset (OCR) is also encoded on the BCR line. If the bit has a value of one for two consecutive bunch crossings, OCR will reset the orbit counter on the next rollover of the BCID counter. ECR (bit 4) resets the L1ID counter and Test Pulse (TP) (bit 5) is forwarded to

Table 1.3: ROC output frame format.

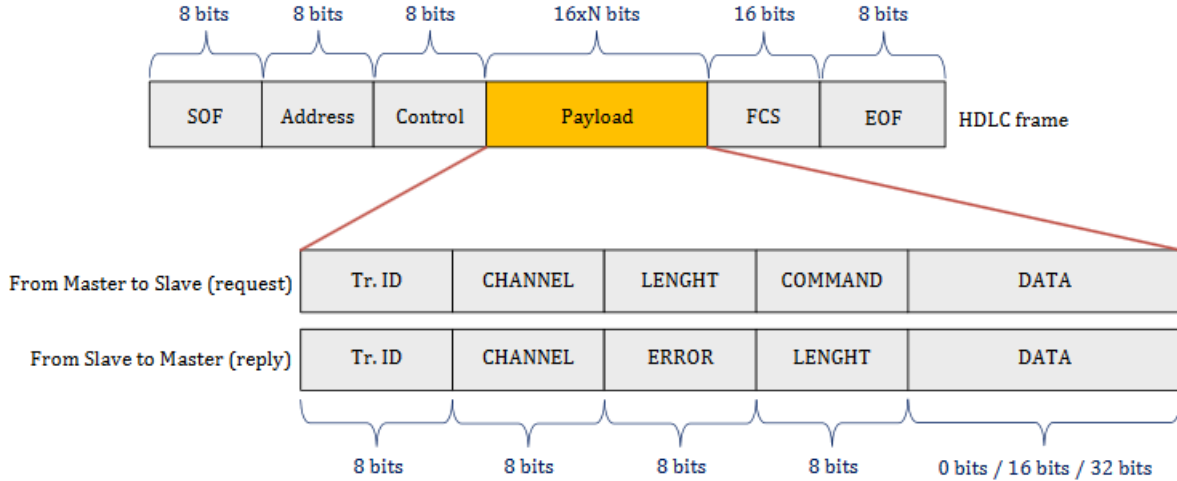
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39
null evnt hdr	SOP (8)								0	1	ROC ID (6)						Level-1 ID (8)								EOP (8)															
hit header	SOP (8)								0	0	orbit		BCID (12)										Level1 ID (16)																	
hit header no TDC	SOP (8)								1	0	orbit		BCID (12)										Level1 ID (16)																	
hit data	P	N	rel BCID (3)			VMMid (3)			Chan (6)						ADC (10)										TDC (8)															
hit data no TDC	P	N	rel BCID (3)			VMMid (3)			Chan (6)						ADC (10)																									
dummy hit data	P	0	3'b0			VMMid (3)			6'b0						11_1111_1111										8'b0															
dummy hit data no TDC	P	0	3'b0			VMMid (3)			6'b0						11_1111_1111																									
trailer opt A	E	TO	VMM missing data flags (8)								L0 ID (4)				Length (no hits) (10)										checksum (8)								EOP (8)							

Table 1.4: TTC data word format.

MSB=7	6	5	4	3	2	1	0
L1A	Soft Reset	Test Pulse	ECR	BCR+OCR	LOA	SCA reset	ECOR

the VMM chips. Bit 6 (Soft Reset) is a synchronous reset for the ROC logic. The L1A (bit 7) identifies a Level-0 trigger and its BCID by the L1A's fixed delay after the requested Level-0. This bit is used for incrementing the L1ID counter.

The SCA is responsible for controlling and monitoring the ASICs on the FE boards. The E-Link port on the SCA ASIC implements a packet oriented full duplex transmission protocol based on the HDLC standard (ISO/IEC 13239:2002) allowing full duplex communication with non-deterministic link latency. This protocol is transmitted inside the EC field (2 bits) of the GBT frame. The HDLC protocol is illustrated in Figure 1.29.

**Figure 1.29:** The HDLC frame.

Interface with ADDC

The interconnection of the L1DDC with the ADDC is done with the use of a 1 m twinax cable with miniSAS connectors on either end, in the same way with the FEs. The L1DDC will distribute two reference clocks at 40 MHz for the GBTXs of the ADDC

and two BCR signals for the ART ASICs. Then each GBTX will distribute the 40 MHz and generate a 160 MHz reference clock for its corresponding ART ASIC. A clock at 40 MHz for sampling the BCR signals is also necessary and is provided by the L1DDC. In Figure 1.30 the overall block diagram is presented. Moreover one E-Link will be used for the slow control data transmission to/from the ADDC board at 80 Mbps, using the HDLC standard. Then, the SCA of the ADDC board will be able to configure the on-board VTTX, ART and GBTX ASICs.

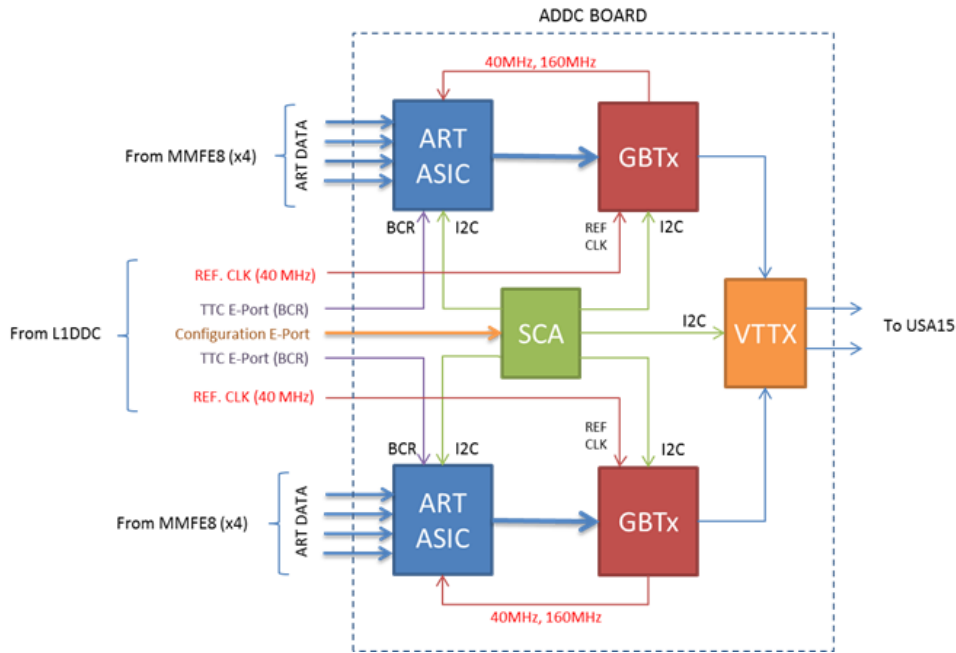


Figure 1.30: L1DDC to ADDC transmitting signals.

L1DDC Prototype-1 and Phase 2 data rates

In this chapter a brief description of the architecture and functionality of the L1DDC prototype-1 board is presented. Moreover, the results of the tests that were performed are also mentioned. The board was initially designed to be compatible with the Phase 1 upgrade and Run 3 data rates. Due to the limited accessibility it was requested that the L1DDC should be compatible even with the demanding high rates of the HL-LHC after Phase 2 and Run 4. New configuration and techniques were implemented but also additional ASICs were added to the initial board.

2.1 L1DDC Prototype-1 description

Initially a common board for both detectors technologies was planned to be used. The L1DDC Prototype-1 is a multifunction board containing not only the radiation tolerant GBT chipset but also a Xilinx's FPGA as an alternative solution in case of GBTX malfunction or failure during the operation [24]. Moreover it was able to verify the proper operation by comparing the data from the two alternative paths. The configuration of the GBTX can be implemented either by the FPGA or the DIP switches by using jumpers. In Figure 2.1 the full functionality of the L1DDC prototype-1 is shown.

Two additional data outputs, an SFP+ as an alternative optical path and an RJ45 connector for 1 Gb/s Ethernet were implemented for compatibility with any read out system. A second RJ45 connector is utilized for receiving the trigger, reset and clock signals from an external source (compatible with the custom made Clock and Trigger Fanout (CTF) modules). The GBTX ASIC provides eight SLVS clock (programmable in phase) outputs that can be used as local timing references in the FE electronics. These clocks are generated by the phase-shifter circuit, and are fully synchronous with one of the GBTX 40 MHz clocks, depending on the transceiver mode, (synchronous with LHC bunch crossing reference) and maintain with it a stable phase relationship. A SMA connector was also used for driving external signals to the FPGA. A SMA pair was used to provide an external reference clock to the GBTX ASIC if this is needed. There was no actual limitation in the dimensions of the prototype board which led to the final

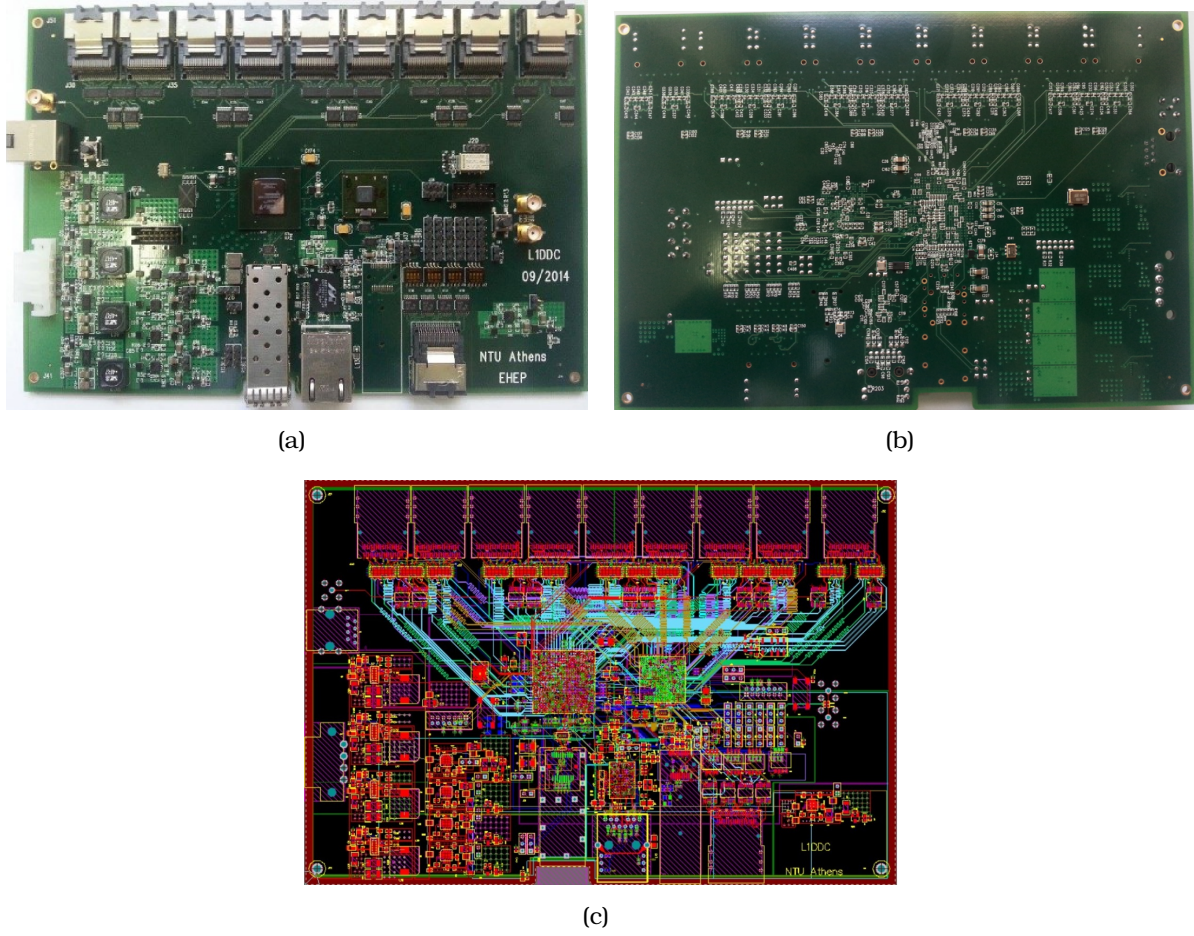


Figure 2.2: (a) Top side, (b) Bottom side and (c) layout of L1DDC prototype-1.

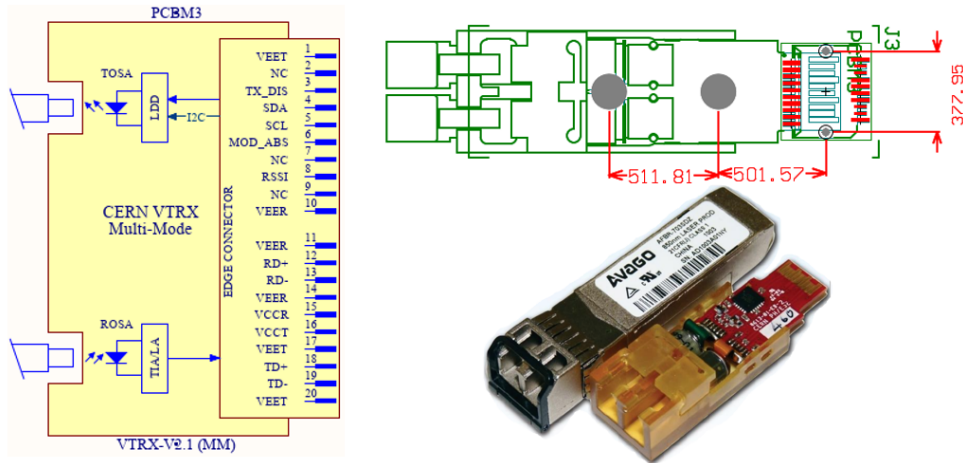


Figure 2.3: The VTRX optical transceiver. Pinout, dimensions and comparison with a commercial SFP+.

consumption of a commercial SFP+. The VTRX is the largest component that it will be placed on the L1DDC board with a width of 45.3 mm, length of 14.5 mm and height of

10 mm.

2.2 L1DDC Prototype-1 design

L1DDC was designed with a fourteen layer stack as it is shown in Figure 2.4. The selection between GBTX and FPGA, which has as result some non active signals, gave the opportunity to use some non isolated layers in the design. The board was designed using Mentor Graphics software version 9.2 and especially Pads Logic for the schematic, Pads Layout for the layout and Pads Router for routing the signals. A typical layout of the board is shown in Figure 2.2(c). The target for the differential impedance was 100Ω for the internal and external layers. The parameters (material height, dielectric constant, copper height) chosen, led to a very good approximation of the targeted impedance (97.48Ω minimum - 99.24Ω maximum). The placement of the GBTX and the FPGA was chosen to be in the middle of the board in order to minimize the routing length of the signals to the miniSAS connectors. On the other hand, this scheme has the penalty of the deviation in the routing lengths of the differential pairs from each miniSAS connector to the GBTX and the FPGA. For that reason all differential pairs were designed to have the same length. This led to a maximum routing length of 115.57 mm for the FPGA and 116.332 mm for the GBTX ASIC.

The GBTX ASIC uses a 400 pins BGA package with ball diameter of 0.5 mm and pitch 0.8 mm. This leaves very little space between the vias and it was difficult to fill with copper the power and ground planes underneath the BGA. For this purpose the vias were designed with a diameter size of 18 mils and drill size of 8 mils. The L1DDC is powered by a four pin power connector by Molex (Part Number 039303041) with mating cable connector the Molex (Part Number 39-01-4040). The LT8612 DC-DC converter by Linear Technology was used to step down the low voltage power to the appropriate levels. This DC-DC converter has a wide input voltage range of 3.4 V to 42 V, an output current of 6 A and a low drop-out (under all conditions) voltage of 250 mV at 3 A. The recommended PCB layout of the LT8612 for the top layer of the board provided by Linear Technology/Analog Devices was used as a guideline in the L1DDC board. In order to step down the outputs of the DC-DC converters, to the appropriate levels and to supply the analog part of the GBTX, the ADP1755 LDO by Analog Devices Inc. was used.

This LDO has a maximum output current of 1.2 A and the input voltage range is 1.6 V - 3.6 V. Moreover, it has a very low drop-out voltage, 105 mV at 1.2 A load and an adjustable output voltage option with soft start from 0.75 V to 3.3 V. For the GBTX the sensitive power rails for the Clock Manager and the Phase Shifters were driven by a separate LDO and the ground was split from the digital one. Later, tests performed by the GBTX group proved that by separating the ground planes can produce poor eye diagrams and it was recommended to use a common digital plain. This approach was implemented on all next prototypes of L1DDC boards.

Artix-7 has eight DC supply voltages (VCCINT, VCCAUX, VCCBRAM, VCCO, VCCBATT, VMGTAVTT, VMGTAVCC, VCCADC) and its DC characteristics are shown in table 2.1. Xilinx recommends the use of a power-on sequence (VCCINT, VCCBRAM, VCCAUX, and VCCO) to achieve minimum current draw and ensure that the I/Os

Stack Up					
PCB Stack Up				Impedance	
Layer	Type	Thickness (mil)		Differential	OHM
Top side solder mask		0.5 mils			
L1	Top	copper + plating	1.4 mils	4/4/4 mils - 100Ω +/- 10%	97.84Ω
		prepreg	4 mils		
L2		copper	0.7 mils		
		core	8 mils		
L3		copper	0.7 mils	4/4/4 mils - 100Ω +/- 10%	99.24Ω
		prepreg	8 mils		
L4		copper	0.7 mils		
		core	6 mils		
L5		copper	0.7 mils	4/4/4 mils - 100Ω +/- 10%	97.85Ω
		prepreg	5 mils		
L6		copper	0.7 mils	4/4/4 mils - 100Ω +/- 10%	97.85Ω
		core	6 mils		
L7		copper	0.7 mils		
		prepreg	4 mils		
L8		copper	0.7 mils		
		core	6 mils		
L9		copper	0.7 mils	4/4/4 mils - 100Ω +/- 10%	97.85Ω
		prepreg	5 mils		
L10		copper	0.7 mils	4/4/4 mils - 100Ω +/- 10%	97.85Ω
		core	6 mils		
L11		copper	0.7 mils		
		prepreg	8 mils		
L12		copper	0.7 mils	4/4/4 mils - 100Ω +/- 10%	99.24Ω
		core	8 mils		
L13		copper	0.7 mils		
		prepreg	4 mils		
L14	Bottom	copper + plating	1.4 mils		
Bottom side solder mask		0.5 mils		4/4/4 mils - 100Ω +/- 10%	97.84Ω
TOTAL			90.2 mils		
			2.2911 mm		

Figure 2.4: Stackup and differential impedance of L1DDC prototype-1.

Table 2.1: Artix-7 DC characteristics.

Symbol	Description	Min	Max	Units
FPGA Logic				
V _{CCINT}	Internal supply voltage	-0.5	1.1	V
V _{CCAUX}	Auxiliary supply voltage	-0.5	2.0	V
V _{CCBRAM}	Supply voltage for the block RAM memories	-0.5	1.1	V
V _{CCO}	Output drivers supply voltage for 3.3V HR I/O banks	-0.5	3.6	V
V _{REF}	Input reference voltage	-0.5	2.0	V
V _{IN} ⁽²⁾⁽³⁾⁽⁴⁾	I/O input voltage	-0.4	V _{CCO} + 0.55	V
	I/O input voltage (when V _{CCO} = 3.3V) for V _{REF} and differential I/O standards except TMD5_33 ⁽⁵⁾	-0.4	2.625	V
V _{CCBATT}	Key memory battery backup supply	-0.5	2.0	V
GTP Transceiver				
V _{MGTAVCC}	Analog supply voltage for the GTP transmitter and receiver circuits	-0.5	1.1	V
V _{MGTAVTT}	Analog supply voltage for the GTP transmitter and receiver termination circuits	-0.5	1.32	V
V _{MGTREFCLK}	Reference clock absolute input voltage	-0.5	1.32	V
V _{IN}	Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage	-0.5	1.26	V
I _{DCIN-FLOAT}	DC input current for receiver input pins DC coupled RX termination = floating	-	14	mA
I _{DCIN-MGTAVTT}	DC input current for receiver input pins DC coupled RX termination = V _{MGTAVTT}	-	12	mA

are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If V_{CCINT} and V_{CCBRAM}, V_{CCAUX} and V_{CCO} have the same recommended voltage levels, can be powered by the same supply and ramped simultaneously. The recommended power-on sequence to achieve minimum current draw

for the GTP transceivers is VCCINT, VMGTAVCC, VMGTAVTT OR VMGTAVCC, VCCINT, VMGTAVTT. Both VMGTAVCC and VCCINT can be ramped simultaneously. The power-on sequence that was used on the L1DDC prototype-1 is shown in Figure 2.5.

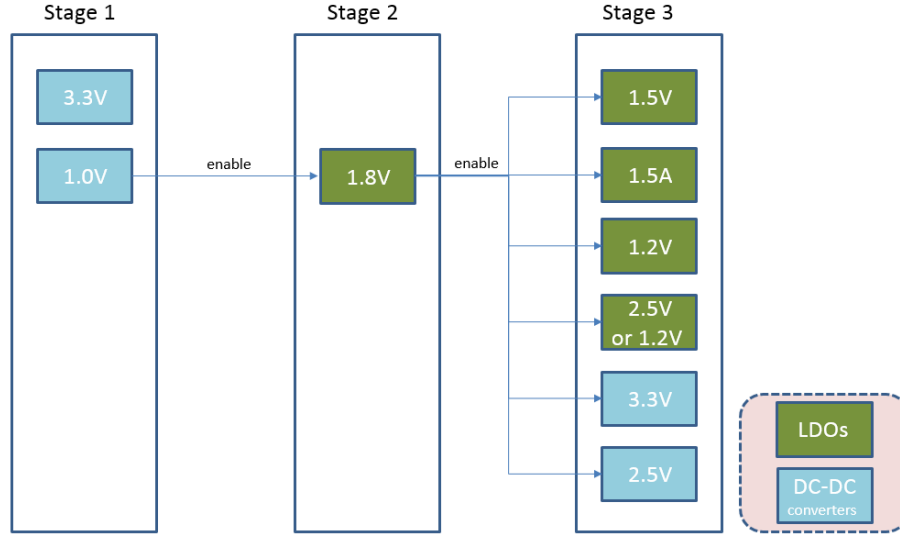


Figure 2.5: The power on sequence implemented in L1DDC prototype-1.

As mentioned in previous chapters the connectivity with the front-ends and the ADDC boards will be through miniSAS connectors and two E-links for every connection will be used. The pin assignment of the miniSAS connector for the front-ends is shown in Figure 2.6(a) and for the ADDC in Figure 2.6(b).

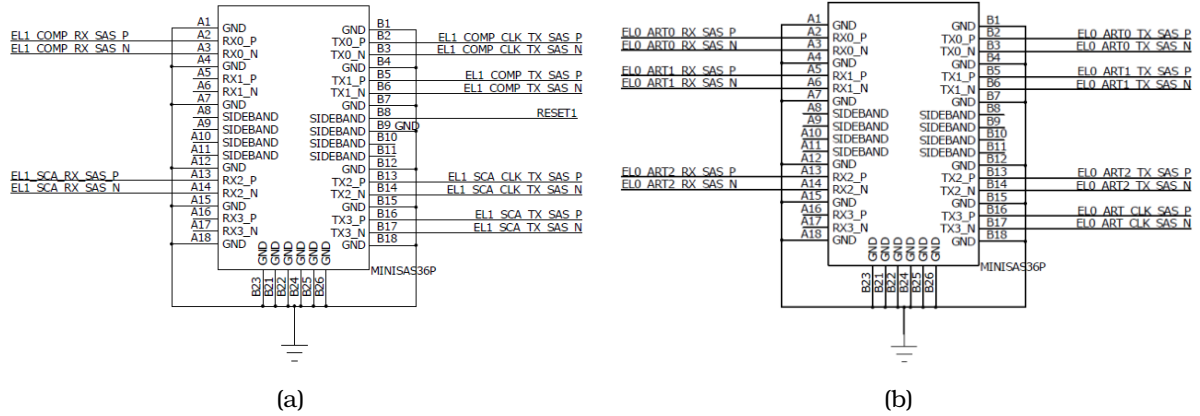


Figure 2.6: MiniSAS pinout. (a) connection to FEs, (b) connection to ADDC.

The selection between the FPGA and the GBTX is made through a NXP 3.3 V, four differential channel, 2:1 multiplexer/demultiplexer switch. The switch is controlled by the FPGA. The input signals from the E-links that are routed to the FPGA are translated into the LVDS standard through the Texas Instrument 2×2 LVDS CROSSPOINT SWITCH (Part No SN65LVDT122). This translator is designed for signaling rates up to 1.5 Gb/s and has a total jitter smaller than 65 ps.

On the DAQ side, the FPGA is connected to a SFP+ connector and to a RJ45 Ethernet connector. Also, the FPGA is connected with an extra pair of GTP transceivers to the custom VTRX for testing purposes or in case of failure of the GBTX. On the other hand the GBTX is connected to both the VTRX and the SFP+. With this schema there is an alternative route for GBTX in case of VTRX failure or for testing purposes. For that purpose the NXP (Part No CBTL02043A) two bidirectional differential channel, 2:1 multiplexer/demultiplexer was used. This multiplexer/demultiplexer is a high-speed signal switch for PCIe Gen3 8 Gb/s and has a high bandwidth of 10 GHz at -3 dB. It has also a low intra-pair skew of 5 ps typical and 35 ps maximum.

Two 200 MHz LVDS differential clocks from Silicon Laboratories Inc. (with Part Number: 510BBA200M000BAG) were used. The one is provided as a user clock and the other as a reference clock for the GBT transceivers. An extra 40 MHz single ended clock from Abracon Corporation (Part No ASV-40.000 MHz-EJ-T) can be provided as user clock. For the FPGA GTP Ethernet reference clock a 25 MHz Crystal (Part No ABM8-25.000 MHz-B2-T) was used in conjunction with a the Ethernet generator Integrated Circuit of IDT, Integrated Device Technology Inc (Part No 844021BG-01LF) which performs a multiplication of the input frequency by five times as shown in Figure 2.7. For the GBTX the reference clock is an external clock assigned to the chip via two SMA connectors. Micron SPI FLASH memory supports 54 MHz (MAX) clock frequency (supported for all protocols in DTR mode). The External Master Configuration Clock (EMCCLK) pin of the Artix7 FPGA was connected to a 50 MHz clock of AVX Corp/Kyocera Corp with Part No : KC2520B50.0000C10E00. This pin is an optional external clock input for running the configuration logic in a master mode (versus the internal configuration oscillator). In master modes the FPGA can optionally switch to EMCCLK as the clock source, instead of the internal oscillator, for driving the internal configuration engine.

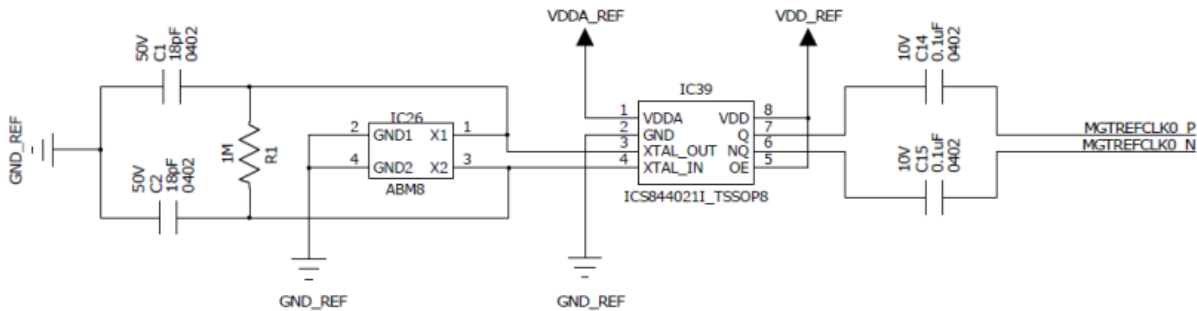


Figure 2.7: Generation of the 125 MHz reference clock for Ethernet communication.

At that time the Molex miniSAS connector (Part Number: 0757830132) was selected. The insulator material is a high temperature thermoplastic glass filled (UL 94V-0), the shell is nickel silver (C770) with thickness 0.250/0.254 and contact area of $0.38 \mu\text{m}$ minimum gold over $2.54 \mu\text{m}$ nickel. The solder foot area is $2.54\text{--}5.09 \mu\text{m}$ tin over $1.27 \mu\text{m}$ nickel. This connector was replaced by the 8AB36-2220-LJ from 3M at all versions of pre-production and production L1DDC boards. For the bypassing capacitors of the Artix-7 FPGA, the recommended values from Xilinx were used. The values for the FGG676 package and XC7A100T device are shown in Figure 2.8.

Package	Device	V _{CCINT}						V _{CCBRAM}				V _{CCAUX}			V _{CC0} Bank 0	V _{CC0} all other Banks (per Bank)		
		680 μ F	330 μ F	100 μ F	47 μ F	4.7 μ F	0.47 μ F	100 μ F	47 μ F	4.7 μ F	0.47 μ F	47 μ F	4.7 μ F	0.47 μ F	47 μ F	47 μ F or 100 μ F ⁽³⁾	4.7 μ F	0.47 μ F
FBG676 RB676	XC7A200T XQ7A200T	1	0	0	0	12	14	1	0	0	3	1	4	7	1	1	2	4
FGG676	XC7A75T	0	1	0	0	4	6	1	0	0	2	1	3	5	1	1	2	4
FGG676	XC7A100T	0	1	0	0	6	8	1	0	0	2	1	3	5	1	1	2	4
FPG1156	XC7A200T	1	0	0	0	12	14	1	0	0	3	1	5	9	1	1	2	4

Figure 2.8: Bypassing capacitors for the Artix-7 FPGA.

The connector selected for the SFP and VTRX optical modules is a standard SFP connector from TE Connectivity (Part No 1888247-1). The material of the housing is high temperature LCP rated with the UL 94V-0 (halogen free according to CERN regulations) and the contacts are phosphor bronze. There is a hard-wired selection for the SFP RS0 and SFP RS1 pins, as long as a selectable power of 2.5 V and 3.3 V for compatibility tests with the VTRX transceiver. Finally the signal SFP TX DISABLE can be set to ground through a hard-wired connector. There was also a concern about the incompatibility between the voltage levels of the 1.5 V GBTX ASIC and the 2.5 V VTRX module. For that reason the I²C voltage levels had to be converted and thus the Texas Instruments I²C voltage level translator was used (Part No PCA9306DCTR).

2.3 Prototype-1 testing

Generally, no critical errors were found on the design or layout of the board. At the time of the prototype-1 fabrication only one GBTX ASIC was available. For that reason only one board was extensively tested for the GBTX communication. Power measurements were performed on all power rails of the board. It was found out that the digital power supply of the GBTX has a voltage drop of about 800 mV. This was caused by the high DC-resistance (440 m Ω) of the decoupling inductor (Part No:MPI2520R1-100-R by ECS inc.) placed at the LDO output of the digital rail of GBTX. This drop didn't affect the functionality of the GBTX and the inductor was not replaced. GBTX configuration functionality was also verified by using either the FPGA or jumpers.

Signal integrity tests were performed on both optical and E-Link paths [25]. A ML605 Xilinx's evaluation board which was running the GBT-FPGA firmware [26] (a core that emulates the GBTX functionality) along with the E-Link blocks was used to generate the data for checking. To test the E-Links, a FPGA Mezzanine Card (FMC) with five uHDMI connectors and a personal computer were used. Finally a custom made miniSAS-to-uHDMI adapter board named Brookhaven Bucharest Arizona L1DDC Adapter (BBALA) was also fabricated. The block diagram of the testing setup is shown in Figure 2.9.

Error checking counters inside the ML605 were monitored via a regular PC running the ISE software and by using Integrated Logic Analyser (ILA) cores. This core can be used to monitor the internal FPGA signals of a design. A predefined pattern was used as the transmitting data at this version of the firmware. E-Links were tested

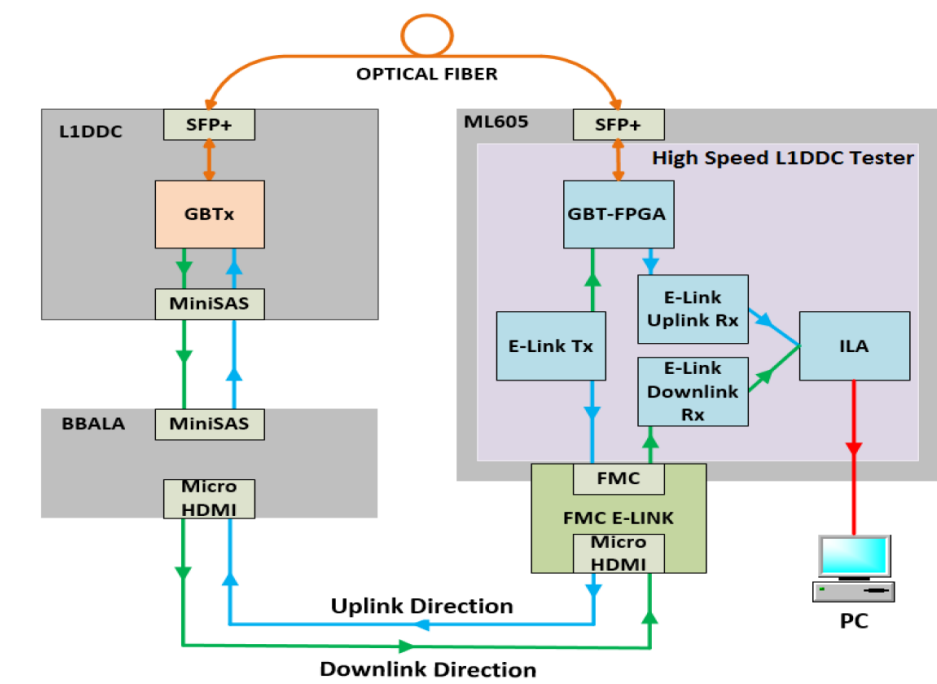


Figure 2.9: Block diagram for the testing procedure of the L1DDC prototype-1.

at their nominal rates (80 and 320 Mb/s). A typical output of the checked data (eight downlinks and four uplinks at 320 Mb/s) and the error counters (red color) is shown in Figure 2.10. Two E-Links showed a strange behaviour counting a lot of errors. These errors occurred systematically on the two Downlinks which are probably due to a malfunctioned multiplexer or poor soldering during to the assembly process. That was verified later with a second prototype-1 board were the GBTX was assembled.



Figure 2.10: E-Link testing of the L1DDC prototype-1 board.

Thermal measurements using the FLIR thermal camera were also performed. The anything-to-LVDS translators are the components that dissipate more heat on the board with a maximum temperature of 50°C on idle state as illustrated in Figure 2.11(a). For the bottom side of the board GBTX is the component that dissipates more heating with a maximum temperature of about 36.7°C as shown in Figure 2.11(b). During the thermal measurements no cooling was used.

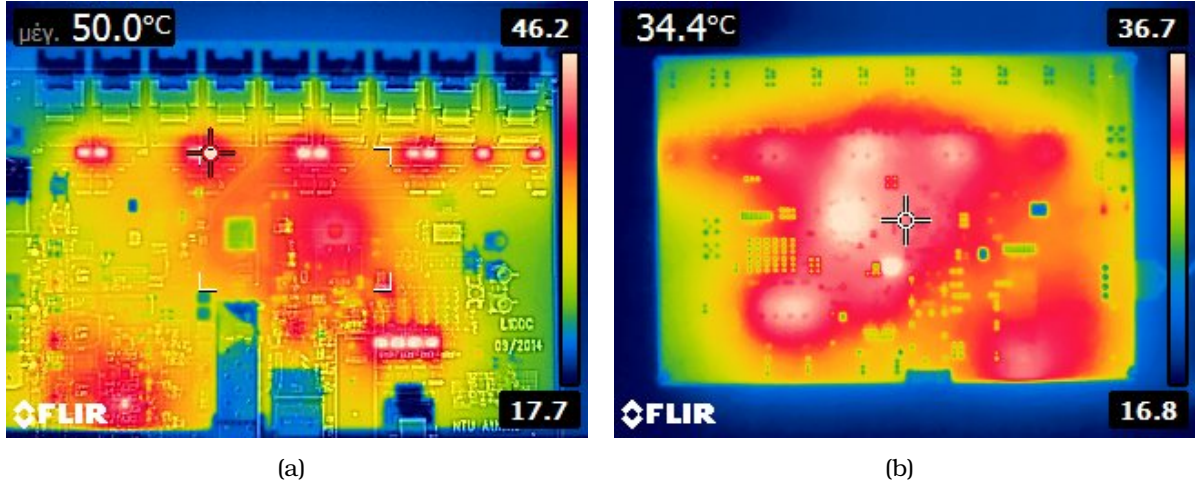


Figure 2.11: Thermal measurements, (a) top side, (b) bottom side.

2.4 Readout at 1 MHz

The original specification for the New Small Wheel readout required a Level-0 trigger rate of 1 MHz with up to $10\ \mu\text{s}$ fixed latency and a Level-1 trigger rate of 200 kHz. The latter was increased to 400 kHz, with up to $60\ \mu\text{s}$ variable latency for the Phase 2 luminosity. The current plan for Phase 2 is to start Run 4 with a single-level scheme at 1 MHz rate, which may evolve later to a two-level hardware trigger with up to 4 MHz at Level-0 and 800 kHz at Level-1. Due to the limited accessibility of the on-detector electronics, after the assembly of the Wheel, all NSW boards must be installed already at Phase 1 with the capability to meet the Phase 2 requirements [27]. The technique chosen was to buffer hit data in the VMM ASIC until a Level-0 trigger initiated transferring the hits within the associated BC window to the ROC ASIC and discarding those no longer needed. The ROC then buffers the Level-0 data until a Level-1 trigger initiates their transfer out over E-links to a GBTX ASIC on the L1DDC boards that drive the optical links to FELIX in USA15. Subsequently ATLAS TDAQ proposed that the NSW should be able to handle a 1 MHz [28] readout rate to FELIX. In this section, the required modifications to the L1DDC that are needed in order to handle the 1 MHz trigger rate, are discussed.

Background hits in the muon spectrometer originate from low-energy photons and neutrons, as well as from charged particles and dominate over the rate of muons originating from the IP. In the present ATLAS Muon System the highest background rate is observed in the Small Wheel region. Accurate measurements of the background

rates with the present detector where used to predict the background rates in the NSW detectors by applying scaling factors for luminosity and the LHC filling scheme. Monte-Carlo simulations are used for projecting to the situation after the Phase 1 upgrade, when the new shielding disk (NJD) in front of the NSW will replace the current JD.

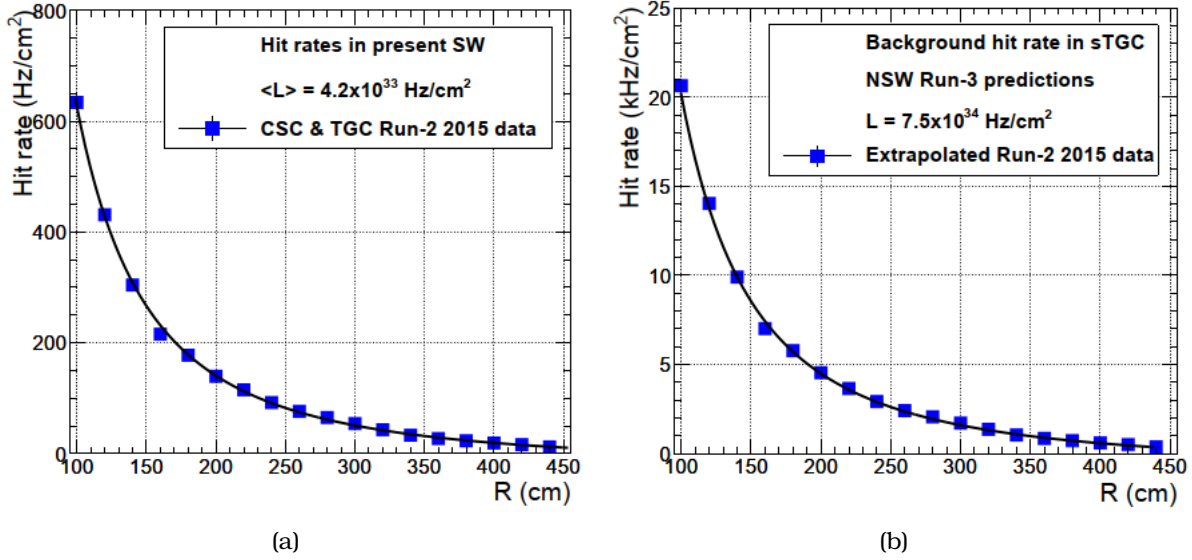


Figure 2.12: (a) SW background hit rates, (b) Extrapolated background hit rates for Run 3 [29].

Background hit rates for CSC and TGC in the present SW extracted from Run 2 ATLAS data are shown in Figure 2.12(a). For both technologies the hit rates have been corrected for detector efficiency. The CSC and TGC Run 2 hit rates have been measured in a run with 2232 bunches per beam and at a luminosity of $4.2 \times 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$. Rates for the HL-LHC are estimated by scaling to a luminosity of $7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$, correcting to the 2736 bunches expected in Run 4, and multiplying by a factor of two, which is the expected increase in rate due to the thinner NJD shielding. This estimated background hit rate as a function of radius is shown in Figure 2.12(b). The maximum expected charged particle rate is 21 kHz/cm^2 .

2.4.1 1MHz L1DDC

The initial plan for the 200 kHz Level-1 trigger was to use one GBTX in the L1DDC for both micromegas and sTGC. After increasing the L1 rate to 400 kHz, a second GBTX was added to handle the high rates for both detectors. In the current TDAQ scheme, the L1DDC must be compatible with readout at slightly below 1 MHz Level-1 rate. This requires two GBTX for the sTGC and three GBTX for the micromegas detectors. Moreover, due to the different FE board characteristics, different L1DDCs will be fabricated for micromegas and sTGC detectors. For the micromegas detectors eight FEs will be connected to one L1DDC board, whereas for the sTGC detectors three FEs will be connected to one L1DDC board. Furthermore, due to the different data rates on each FE, various numbers of E-Links with different bandwidths have to be used for the two detectors.

For the sTGC case, two GBTX are enough to handle the new high rates, as shown in Figure 2.13, where the red crosses indicate the 90% utilization of each E-Link. Bonding of E-links will be used to increase the actual bandwidth to 640 Mb/s for some of the links. The rates have been calculated assuming removal of the 8-bits TDC field of the hit information received from the VMM.

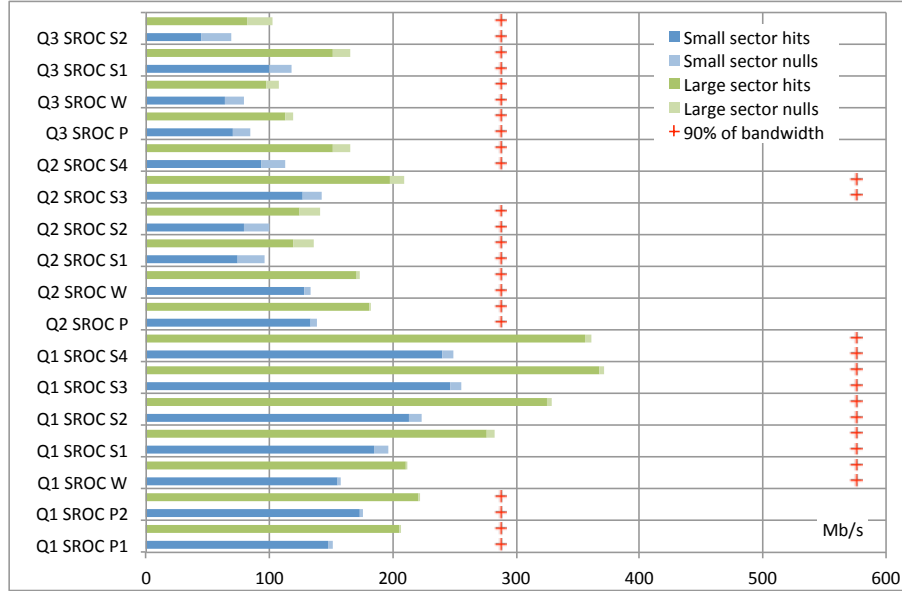


Figure 2.13: E-link rates in Mb/s for the Pad & Wires and Strip FEs of the sTGC for the 1 MHz common trigger.

The bank configuration of the sTGC-L1DDC is shown in Fig. 2.14. On the left side the configuration of the Strip FEs is illustrated. Two GBTX will be used in this case and a second miniSAS will be added for the inner strip FEs to provide the path for the extra differential pairs. On the right the configuration of the Pad & Wire FE boards is shown. The same type of L1DDC is used for strips and pad & wires. However, in order to reduce the cost, the second GBTX will not be mounted on the Pad & Wire board. The solid green lines represent the E-Links for the TTC, clock and Level-1 data (one per FE board), the dashed green lines the uni-directional E-Links for the Level-1 data (from the FEs to L1DDC) and the red lines the E-Links for the slow control data. The maximum readout rate was estimated at 1.478 Gb/s for the inner sFEB. Each L1DDC for the sTGC detectors can handle up to 5.12 Gb/s of level-1 data and a total bandwidth of 5.621 Tb/s can be achieved for the 512 boards. L1DDC interfaces with the back-end with four fibers per board (two for transmitting and two for receiving).

When adding a second GBTX on the L1DDC for the sTGC, an additional VTRX optical transceiver is also required. The configuration of the two ASICs can then be performed through the optical link by the IC field of the GBT frame. The I²C master channel of each GBTX is used for the configuration of the VTRX as shown on the left side of the Figure 2.15(a). For the micromegas case, even with two GBTX in the L1DDC and thus with doubled bandwidth, the rates are still high and as a consequence some E-Links have an unacceptable expected utilization of up to 96%. To reduce the E-Link utilization and to equalize the rates, a third GBTX was added to the L1DDC for the

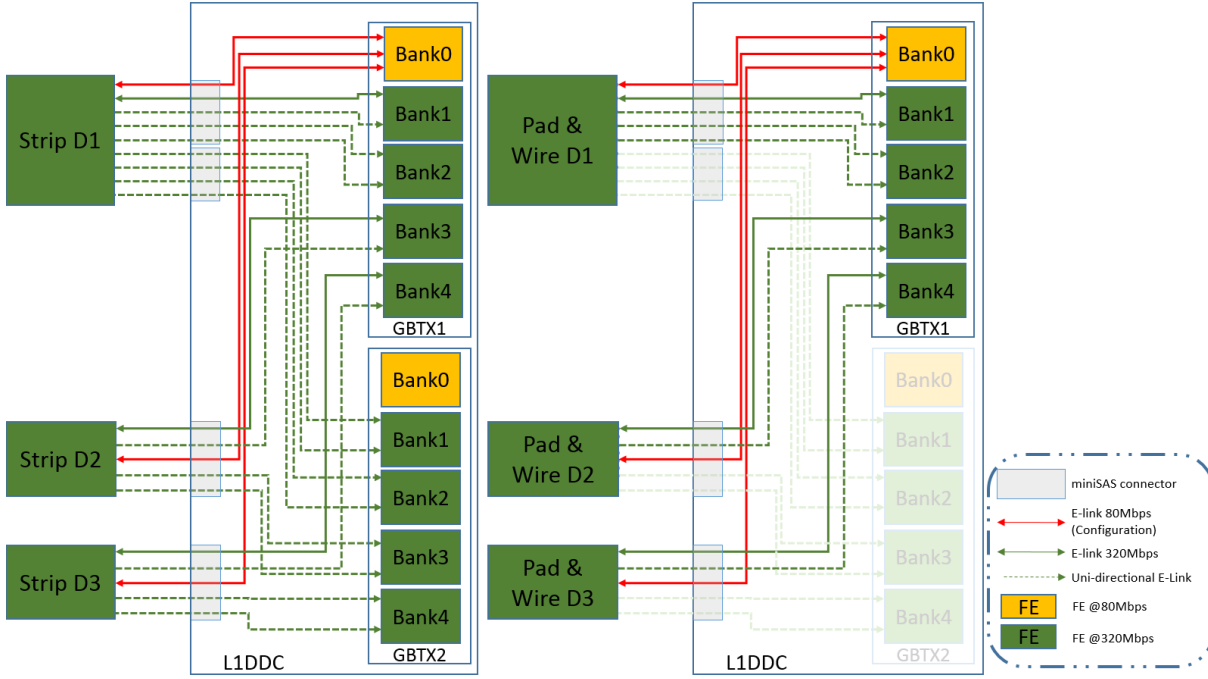


Figure 2.14: Bank configuration of the sTGC FE boards.

micromegas detectors. In order to leave the number of fibers unchanged but also due to the limited available space, a VTTX optical transmitter was added (use of one fiber pair) instead of two VTRX optical transceivers (use of two fiber pairs). To configure the two additional GBTX, an SCA ASIC was also added. With this scheme, the first GBTX is configured by the IC field of the GBT frame, and the GBLD of the VTRX transceiver is configured by the I²C master of this GBTX. Furthermore, the extra SC E-Link of the GBTX will be used to send the data to the SCA of the L1DDC. Two I²C masters of the SCA are used to configure the other two GBTXs and then these GBTXs will configure the two GBLDs of the VTTX optical transmitter as shown in Figure 2.15(b). With this configuration the L1DDC is capable of handling up to 8.720 Mb/s of level-1 data over 31 E-Links and a maximum rate of 4.46 Tb/s can be achieved by the 512 L1DDC boards. Each L1DDC utilizes only four fibers (one receiving and three transmitting) for the interface with the back-end.

The E-Link rates and 90% utilization limit of the micromegas for the three-GBTX configuration are shown in Fig. 2.16. The maximum E-Link utilization is 79.5% for the inner FEs. The utilization depends approximately linearly on the length of the time interval during which hits are accepted for a L0 accept. The length used is 5 BC, i.e. 125 ns. The maximum E-link utilization would become 92.5% which would be too tight and instead a length of 6 BC had to be used.

From the three GBTXs, one (GBTX1) is operating as a transceiver and the other two (GBTX2 and GBTX3) as transmitters only and thus their E-Link transmitting pairs and EC channels cannot be used. For this reason only GBTX1 will be used to provide data to the FEs. One bank (Bank 0) of GBTX1 is dedicated for SCA communication and runs only at 80 Mb/s.

In order to provide the configuration data to the SCA but also the two BCR signals for

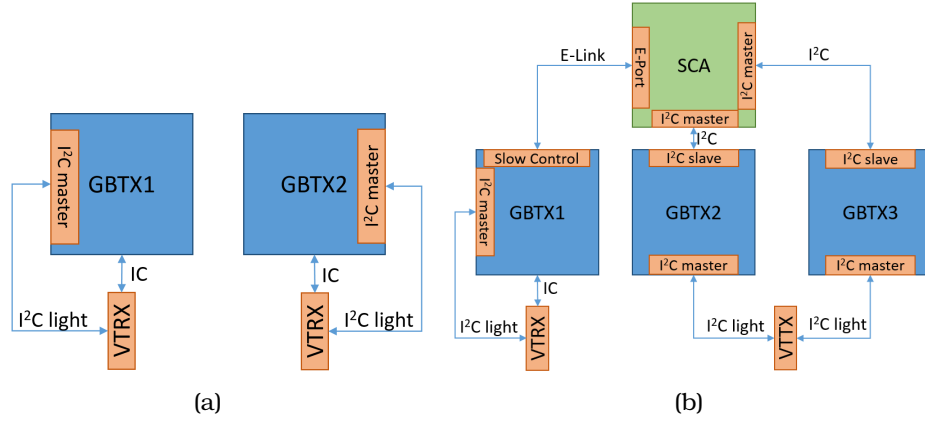


Figure 2.15: GBTX configuration (a) sTGC-L1DDC, (b) MM-L1DDC.

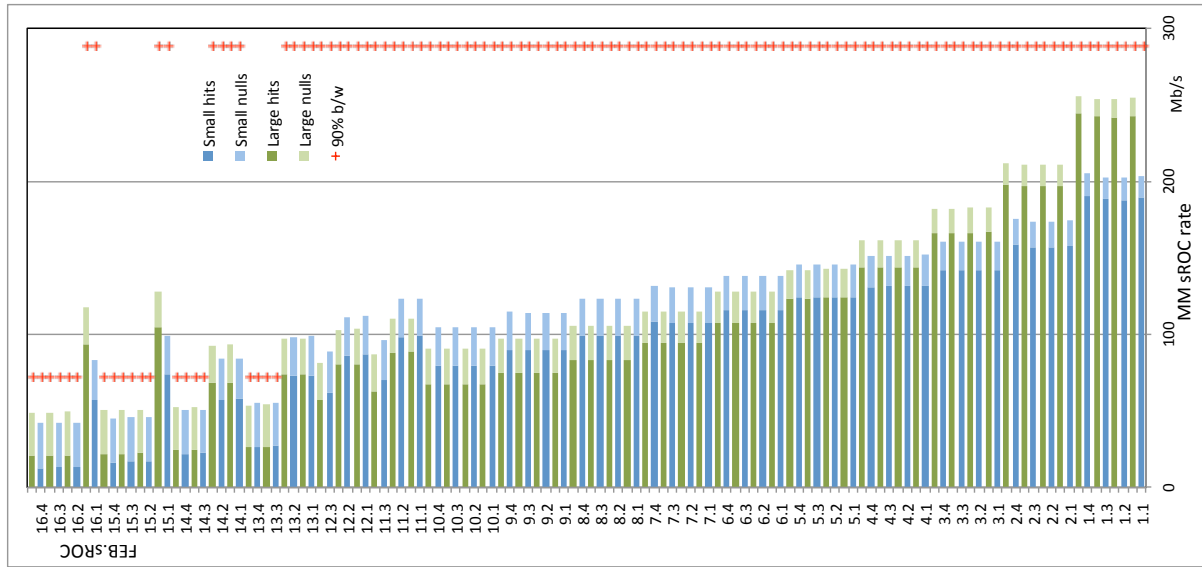


Figure 2.16: E-link rates for the micromegas detectors - three GBTX configuration.

the ART on the ADDC board, a second bank (Bank 1) of the GBTX1 is also configured to run at 80 Mb/s. The rest E-Links of bank 1 will be used to provide additional bandwidth to the outer FEs where the rate is relatively low. The rest of the banks are configured to run at the maximum speed of 320 Mb/s. With this configuration there are only six E-Links to provide the TTC information to the eight FEs at the rate of 320 Mb/s and thus 1:2 fan-out chips will be used for the outer FEs (9-16). The GBTX bank configuration of the MM-L1DDC is shown in Figure 2.17.

The solid green lines are E-Links for the TTC, clock, and level-1 data (one per FE board), the dashed green lines are uni-directional E-Links for the Level-1 data at 320 Mb/s (from the FEs to L1DDC), the yellow lines are level-1 data at 80 Mb/s, the red lines are E-Links for the configuration data at 80 Mb/s and the purple dashed lines indicate the TTC data at 320 Mb/s provided to the FEs through the fanout chips. For GBTX1 the output clock of every bank is set to 40 MHz.

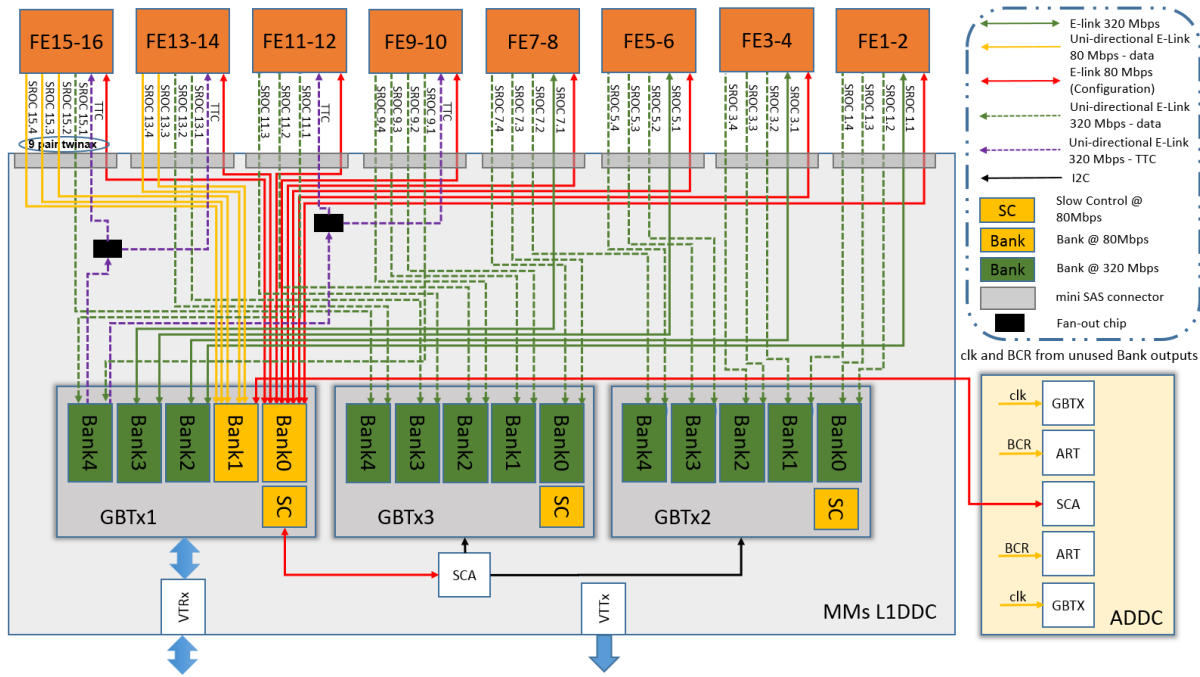


Figure 2.17: Bank configuration of the micromegas L1DDC.

E-links 11.1, 11.2, 13.1, 13.2 (or 12.1, 12.2, 14.1 and 14.2 for the even side) transfer the data from three VMMs, 15.1 (or 16.1) data from five VMMs, while the 80 Mb/s links transfer data from one VMM. All other E-links transfer data from two VMMs, the E-link rates have been minimized by appropriate pairing of the VMMs. Red marks indicate 90% E-Link utilization.

2.4.2 Impact of the 8-pair twinax cable on E-Link rates

The idea of using the custom 10-pair miniSAS cable from 3M was finally abandoned due to the extremely high cost of the cables. The one option is to use the sidebands for the transmission of the differential pairs but in long cables this maybe an issue. The second option is to give up the one differential pair but this of course affects the overall bandwidth. All E-Link output rates were recalculated using three sROCs instead of four as presented in Figure 2.18. A special configuration on the ROC crossbar was implemented to equalize the rates on the E-Links according to the eight VMMs data outputs.

As a result, the occupancy was increased and the safe margin was minimized. Especially for the micromegas case and Large Module (LM), by using the 8-pair twinax cable the inner FE occupancy exceeds the 100% as shown in Table 2.2 compared to 80.80% occupancy of the 10-pair one. For the sTGC case the maximum occupancy increased up to 65.57% on the LM with a safe margin of more than 30%.

For the Small Module (SM) where the rates are not so high the occupancy increased at a maximum of 83.89% for the micromegas detectors which still leaves a small safe margin of 12.53%. On the SM of the sTGC detectors the increase is relatively small (occupancy increased from 36.71% to 41.6% for the worst case) leaving a safe margin

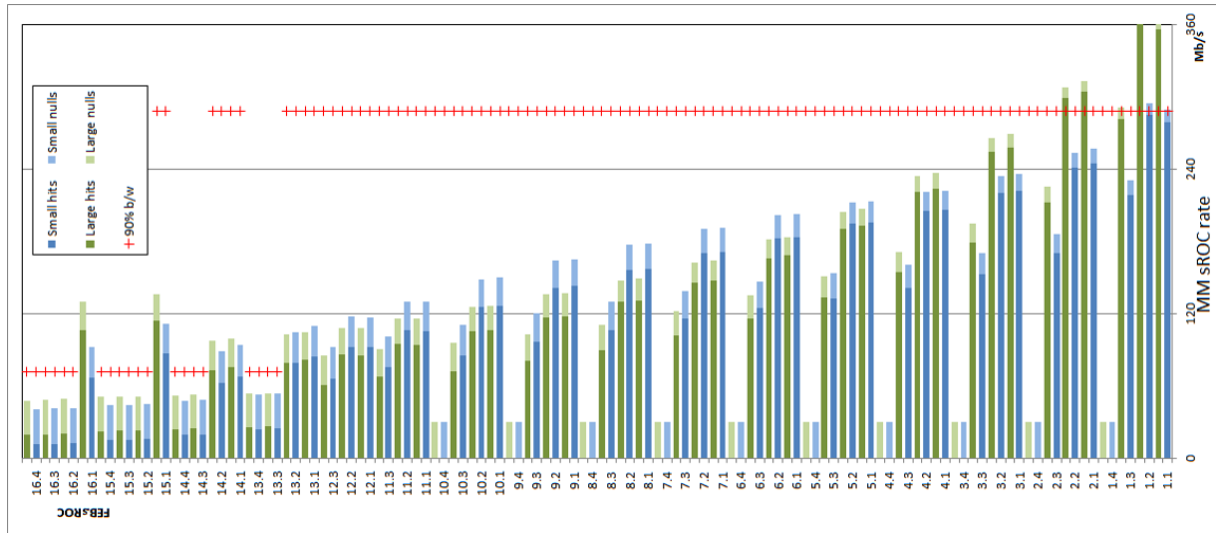


Figure 2.18: E-link rates for the micromegas detectors - three GBTX configuration and eight pair miniSAS.

Table 2.2: 8 vs 10 pair occupancy for LM.

LM									
total bandwidth			total	10 pair Occupancy		total	8 pair Occupancy		
sTGC									
	pads		strips		Pads	Strips		Pad	Strips
Q1	657.00		1403.40	2560	25.66%	54.82%	2240	29.33%	62.65%
Q2	366.70		629.50	1280	28.65%	49.18%	960	38.20%	65.57%
Q3	219.80		247.80	1280	17.17%	19.36%	960	22.90%	25.81%
MMs									
even		odd			even	odd		even	odd
MMFE2	839.70	MMFE1	1034.20	1280	65.60%	80.80%	960	87.47%	107.73%
MMFE4	614.60	MMFE3	710.20	1280	48.02%	55.48%	960	64.02%	73.98%
MMFE6	460.10	MMFE5	528.10	1280	35.95%	41.26%	960	47.93%	55.01%
MMFE8	356.70	MMFE7	402.60	1280	27.87%	31.45%	960	37.16%	41.94%
MMFE10	288.40	MMFE9	319.60	1280	22.53%	24.97%	960	30.04%	33.29%
MMFE12	232.30	MMFE11	256.50	960	24.20%	26.72%	960	24.20%	26.72%
MMFE14	197.10	MMFE13	213.30	800	24.64%	26.66%	720	27.38%	29.63%
MMFE16	166.00	MMFE15	182.50	560	29.64%	32.59%	480	34.58%	38.02%

of more than 50% as presented in Table 2.3.

Table 2.3: 8 vs 10 pair occupancy for SM.

SM									
				10 pair			8 pair		
total bandwidth				total	Occupancy		total	Occupancy	
sTGC									
	pads		strips		Pads	Strips		Pad	Strips
Q1	495.70		939.80	2560	19.36%	36.71%	2240	22.13%	41.96%
Q2	272.70		397.00	1280	21.30%	31.02%	960	28.41%	41.35%
Q3	142.10		153.80	1280	11.10%	12.02%	960	14.80%	16.02%
MMs									
even		odd			even	odd		even	odd
MMFE2	671.70	MMFE1	805.30	1280	52.48%	62.91%	960	69.97%	83.89%
MMFE4	561.40	MMFE3	606.00	1280	43.86%	47.34%	960	58.48%	63.13%
MMFE6	496.80	MMFE5	530.60	1280	38.81%	41.45%	960	51.75%	55.27%
MMFE8	422.90	MMFE7	461.50	1280	33.04%	36.05%	960	44.05%	48.07%
MMFE10	339.70	MMFE9	383.30	1280	26.54%	29.95%	960	35.39%	39.93%
MMFE12	251.40	MMFE11	287.00	960	26.19%	29.90%	960	26.19%	29.90%
MMFE14	169.60	MMFE13	213.40	800	21.20%	26.68%	720	23.56%	29.64%
MMFE16	102.80	MMFE15	133.20	560	18.36%	23.79%	480	21.42%	27.75%

sTGC L1DDC board

As was mentioned in Section 2.4 different L1DDC boards were fabricated for sTGC and Micromegas detectors for the 1 MHz readout rate. The board was designed according to the final specifications and for that reason all components that were not part of the final product were removed (FPGAs, SFPs, Multiplexers, voltage translators, SMA and RJ45 connectors etc) from the first prototype.

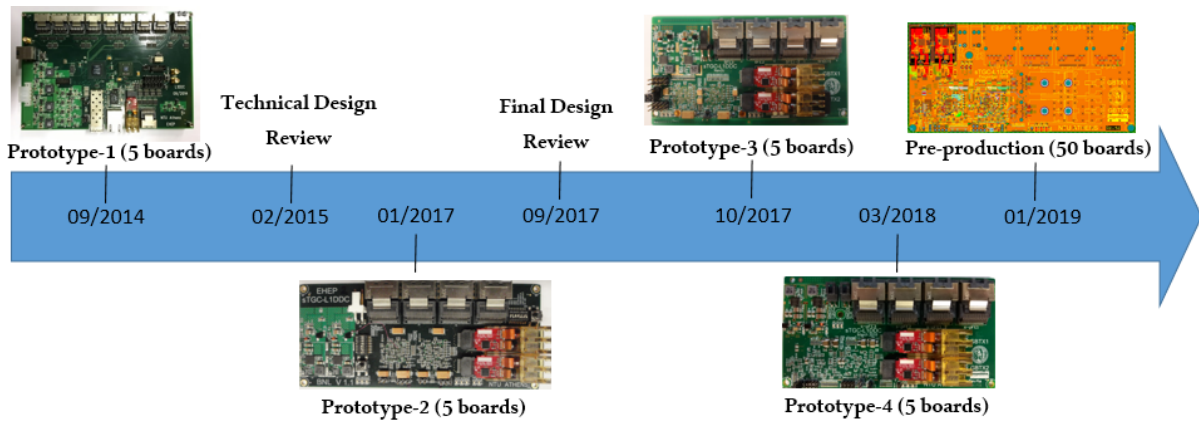


Figure 3.1: *sTGC-L1DDC roadmap.*

The roadmap of the sTGC-L1DDC board includes a series of four prototypes and two reviews as is presented in Figure 3.1. After the first prototype and the Technical Design Review which was held in February 2015, the green light was given by the reviewers and the production of five boards of the second prototype was launched. This prototype didn't meet the space requirements of the sTGC detectors and was modified. In the meantime, just before receiving the five new prototypes the Final Design Review took place in September 2017. After the positive outcome and few suggestions by the reviewers the design and fabrication of five more boards of the fourth prototype started in March 2018. This prototype is the reference point for the 50 pre-production boards which were submitted for fabrication in January 2019. We will describe in great detail the design rules, the modifications and the tests performed to all prototypes to verify the proper operation of the final boards.

3.1 Prototype-2 description

All electronic boards that will be placed on the detector should be radiation and magnetic tolerant. The expected total ionising dose in the NSW is $\sim 2 \times 10^{11} \text{ n/cm}^2/\text{yr}$ at the nominal luminosity $1 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. After the Phase 2 upgrade and during Run 4,5 the total ionising dose will be increased to $\sim 15 \times 10^{11} \text{ n/cm}^2/\text{yr}$ as the instantaneous luminosity will be $7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. Figure 3.2 shows the total ionising dose and neutron flux with respect to the radius from the interaction point.

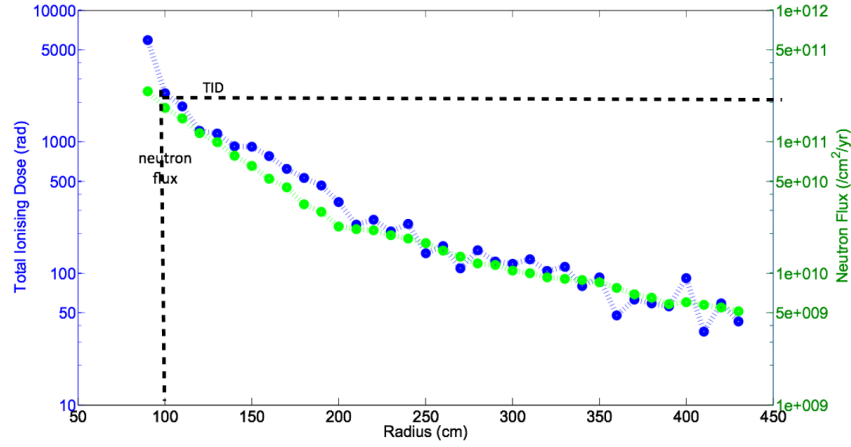


Figure 3.2: NSW Radiation. Total ionising dose and neutron flux $E > 20 \text{ MeV}$.

In the NSW, the maximum magnetic field induced by the end-cap and barrel toroids (4 T each) is expected to be about 0.6 T (on the outer edges of the wedge). Since the LM is closer to the toroid magnet the magnetic field is stronger comparing to SM. Figure 3.3(a) represents the maximum expected magnetic field of the LM and Figure 3.3(b) of the SM at a distance of 7900 mm and 7435 mm respectively. All versions of the L1DDC boards

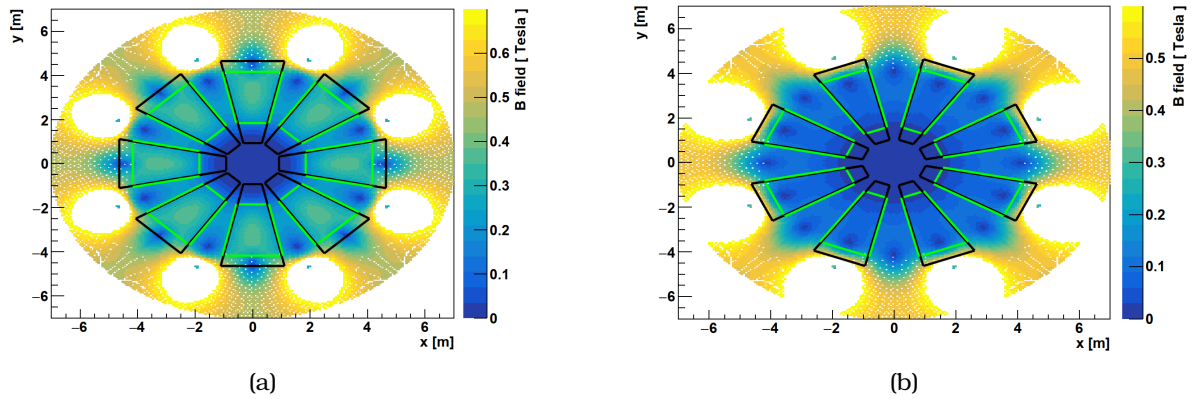


Figure 3.3: Total magnetic field for (a) large sector at 7900 mm and (b) small sector at 7435 mm from the interaction point.

require only two voltage levels of 1.5 V and 2.5 V. The crucial decision for the power

distribution was to select a commercial DC-DC converter and LDO that can survive under radiation and magnetic field. Radiation tests showed that commercial DC-DC converters have a relatively low tolerance under high radiation environments and magnetic fields. The LTM4619-A, LTM4619-B, LTM4628-A, LTM4628-B, LT8610 by Linear Technology, the ADP5052 and ADP1864 by Analog Devices, the TPS53319 by Texas Instruments and the ST1S41 by ST Microelectronics were tested under radiation by the University of Michigan and INFN Roma. All DC-DC converters failed after few days of operation and certain amount of radiation. The results are presented in Figure 3.4. Tests on LDOs showed a similar behaviour.

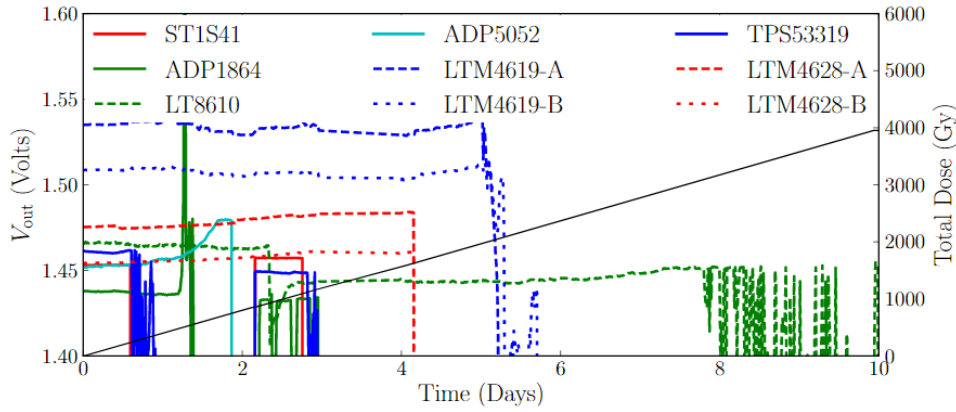


Figure 3.4: DC-DC converter output voltage under radiation [30].

Thus it was finally decided to use the CERN's FEAST [31] radiation tolerant buck converter. This converter is capable of continuous operation up to more than 200 Mrad (Si) total ionizing dose and an integrated particle fluence of 5×10^{14} n/cm² (1MeV-equivalent)[32]. It is also designed for operation in strong magnetic fields of more than 40,000 G and the switching frequency is selectable in the range of 1 to 3 MHz. The input voltage range is from 5 V to 12 V, has continuous 4 A load capability and achieves 76% efficiency. The package is a plastic Quad Flat No-Lead (QFN) 5.0 mm × 5.0 mm × 0.9 mm in size, with 32 pads and with an exposed pad to be soldered to the PCB for better thermal properties.

The shield that was used at that time was a commercial one by Harwin (part number: S02-20150300) with a thickness of 0.2 mm and the material is nickel silver. These shields provide excellent Radio-Frequency Interference (RFI) and Electro-Magnetic Interference (EMI) protection to sensitive circuitry at the PCB level. The dimensions of the shield are 20 mm × 15 mm. The selection of the material of the FEAST shield was crucial for the noise suppression but also to ensure that metal whisker [33] will not be generated. Metal Whiskers are hairlike protrusions that can grow on surfaces of many technologically important metals, for example, tin and zinc. These whiskers are grown under the presence of electric field and may cause short circuits across leads of electric equipment raising reliability concerns.

The maximum input current is equal to the output current divided by the conversion

Table 3.1: FEAST switching frequency options.

Resistance (kΩ)	270	200	180	160	130	100	82
Frequency (MHz)	1.03	1.35	1.48	1.65	1.99	2.51	2.98

ratio and the efficiency:

$$I_{in} = \frac{I_{out}}{Efficiency \times \frac{V_{in}}{V_{out}}}$$

To enable the device the available enable pin (En) should be asserted by applying a voltage above about 820 mV. FEAST2.1 has also an Over-Temperature Protection (OTP) functionality that monitors the on-chip junction temperature and disables the device when it reaches about 103°C (the OTP temperatures are not precisely measured since T is not measured on FEAST2.1 itself). The OTP has a hysteresis of about 30°C, hence the converter restarts (with Soft Start) when the junction temperature decreases below 73°C. In case of inefficient cooling, it is hence possible that the converter cycles between the disabled and enabled states at a frequency dependent on the load and cooling conditions.

The switching frequency of the converter can be adjusted with an external resistor, which provides the bias current to the embedded oscillator. While the usage at 1.5 MHz allows top efficiency, 1.8 MHz operation provides reduced conductive noise and is preferred as default configuration. The available options for the FEAST frequency according to the resistor value is presented in Table 3.1. FEAST has also a power good output pin that monitors the output voltage. Moreover, utilizes a lot of extra features as over-current and over-temperature protection, enable input, power good output, under-voltage lockup and selectable Power Transistor size (5/5th or 2/5th) for improved efficiency at small loads (<600 mA). Finally chip temperature can be monitored via a dedicated analog signal (PTAT).

The GBTX ASIC has a maximum power consumption of about 2237 mW when it works in full operation. The initial power estimation of the board using one GBTX and one VTRX is 5.47 W and is shown in Table 3.2. This table includes a 30% margin and 66% FEAST efficiency. For the second prototypes of the L1DDC boards and for the FEAST ASIC, the schematics and the layout suggested by the University of Michigan's (UM) were used. This layout ensures low output noise on the power rails but also less radiated noise. The schematics are shown in Figure 3.5, the recommended layout in Figure 3.6(a) and the layout implemented in sTGC-L1DDC in Figures 3.6(b) (top side) and 3.6(c) (bottom side). The output voltage level defined by R4 and R5 resistors according to the following equation:

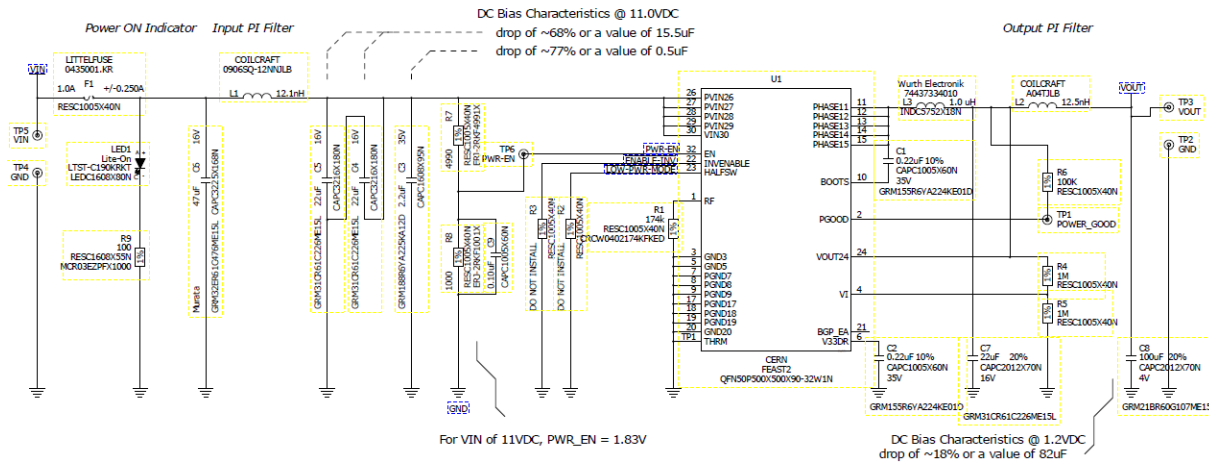
$$V_{out} = 0.6 \times (1 + \frac{R4}{R5})$$

A special anti-parallel placement of the capacitors for both input and output rails of the FEAST ASIC can reduce their distortion while it maintains the large capacitance value. In UM layout only the input anti-parallel capacitors are implemented. Moreover it was suggested by the FEAST designers that the power rails/traces should be at

Table 3.2: Power consumption of the NSW boards and ASICs.

	Power	1.2D	1.2A	1.5	2.5	MMFE	ADDC	L1DDC	Strip (5 VMM)	Strip (6 VMM)	Strip (7 VMM)	Pad + Wire (3 VMM)	Pad + Wire (2 VMM)
Device	Watts	Current @ Voltage				Qty. Per Board							
VMM	0.900	0.150	0.600			8			5	6	7	3	2
ROC	0.500	0.417				1			1	1	1	1	1
TDS	0.700		0.467						3	3	4	2	1
ART	0.500		0.333				2						
SCA @ 1.5V	0.250		0.167				1		1	1	1	1	1
SCA @ 1.2V	0.250	0.208				1							
GBTX	2.201		1.467				2	1					
GBTIA	0.250			0.100				1					
GBTLD	0.325			0.130			1	1					
Estimated Requirement						7.95	5.97	2.78	7.35	8.25	9.85	4.85	3.25
Margin @ 30%	0.30					2.39	1.79	0.83	2.21	2.48	2.96	1.46	0.98
FEAST @ 66%	0.66					5.32	4.00	1.86	4.92	5.53	6.60	3.25	2.18
Total Power						15.66	11.77	5.47	14.48	16.25	19.40	9.55	6.40
Board Count													
Board Count						4096	512	1024	128	384	256	256	512

the exact size of the filtering capacitors/inductors footprint for best filtering. A shield is used to minimize the radiated noise produced by the power inductor used on the FEAST circuitry. The selection and the placement of the shield is crucial to achieve the optimal performance. The anti-parallel capacitors, FEAST ASIC and the power inductor are placed inside the shield. The shield that was used at that time was a commercial one by Harwin with a thickness of 0.2 mm and the material is nickel silver.

**Figure 3.5:** Michigan's recommended schematics.

The board dimensions for the sTGC-L1DDC prototype-2 are 140 mm × 50 mm and the board height is approximately 15 mm. In total five sTGC-L1DDC prototype-2 boards were fabricated in January 2017. The top side of the L1DDC prototype-2 board is shown in Figure 3.9(a). The four miniSAS connectors (top center), the power connector (top left), the FEAST ASICs without the shield (left) and the VTRX optical transceivers (right) are visible. On the bottom side of the board, Figure 3.9(b) only the two GBTXs

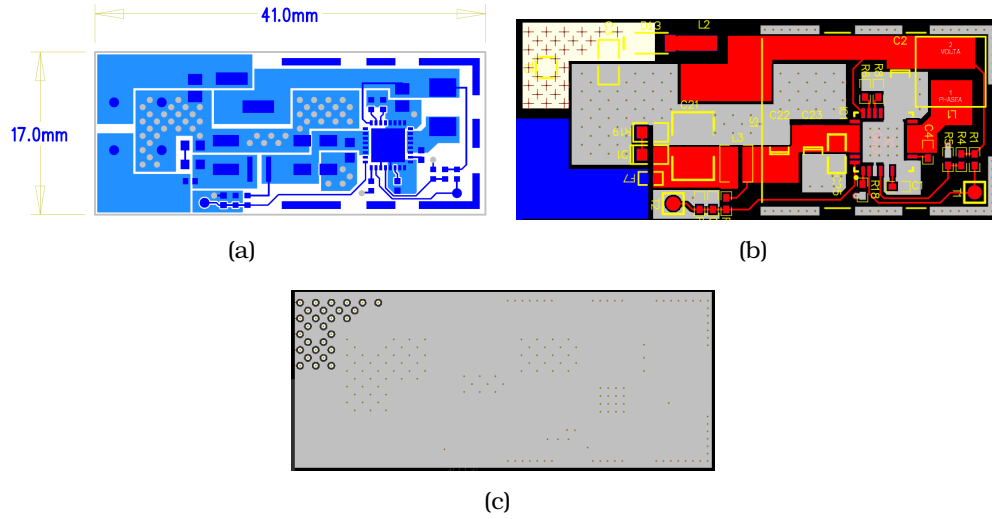


Figure 3.6: The FEAST layout that was used for the sTGC-L1DDC prototype-2.

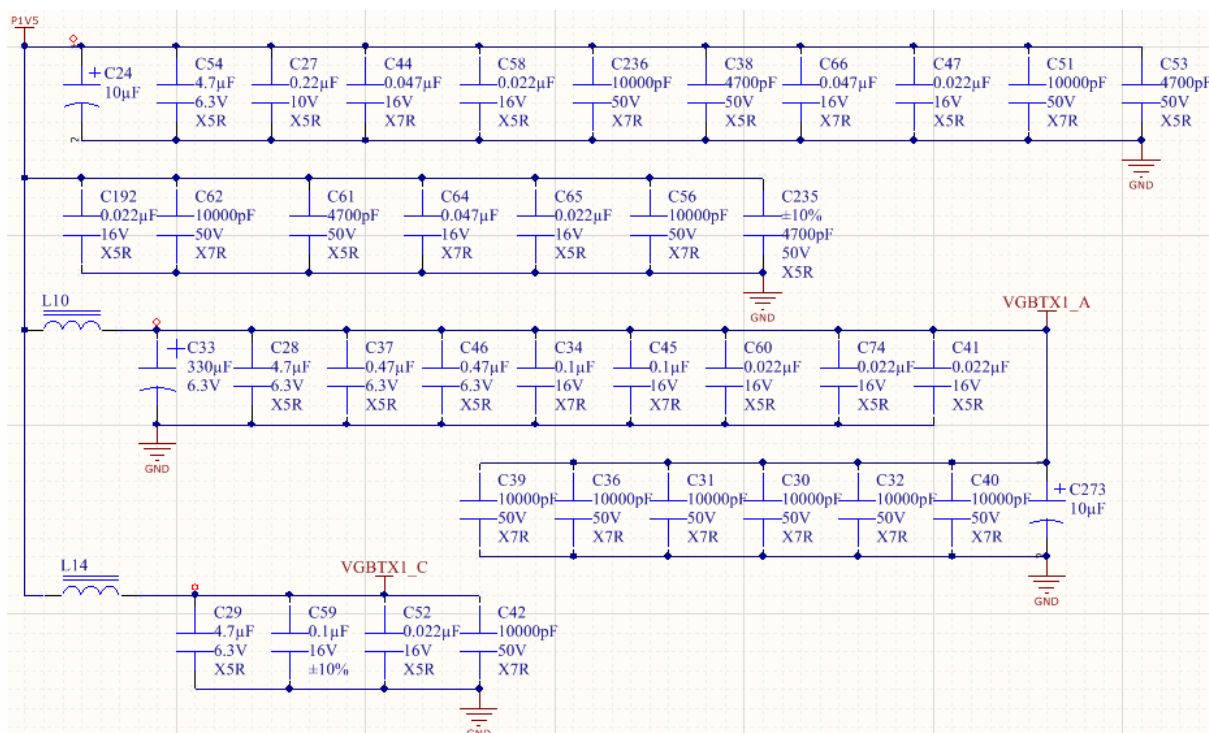
are placed. The layout of the board is illustrated in Figure 3.9(c).

Lyr	Type	Image	Foil	Thk (μm)	Family	Vendor
✓L1	Signal	Cu foil 18 μm	18μm 48		Copper Foil	Foil
		IT-180A 106 (71.5% RC)			IT-180A	ITEQ
		IT-180A 106 (71.5% RC)		94.6	IT-180A	ITEQ
✓L2	Power / Ground	IT-180A 0.150 mm 18/18	18μm 18	150	IT-180A	ITEQ
✓L3	Signal	IT-180A 2116 (53.0% RC)	18μm 18		IT-180A	ITEQ
		IT-180A 2116 (53.0% RC)		228.4	IT-180A	ITEQ
✓L4	Power / Ground	IT-180A 0.150 mm 18/18	18μm 18	150	IT-180A	ITEQ
✓L5	Signal	IT-180A 2116 (53.0% RC)	18μm 18		IT-180A	ITEQ
		IT-180A 2116 (53.0% RC)		228.4	IT-180A	ITEQ
✓L6	Power / Ground	IT-180A 0.360 mm 18/18	18μm 18	360	IT-180A	ITEQ
✓L7	Power / Ground	IT-180A 2116 (53.0% RC)	18μm 18		IT-180A	ITEQ
		IT-180A 2116 (53.0% RC)		228.4	IT-180A	ITEQ
✓L8	Signal	IT-180A 0.150 mm 18/18	18μm 18	150	IT-180A	ITEQ
✓L9	Power / Ground	IT-180A 2116 (53.0% RC)	18μm 18		IT-180A	ITEQ
		IT-180A 2116 (53.0% RC)		228.4	IT-180A	ITEQ
✓L10	Signal	IT-180A 0.150 mm 18/18	18μm 18	150	IT-180A	ITEQ
✓L11	Power / Ground	IT-180A 106 (71.5% RC)	18μm 18		IT-180A	ITEQ
		IT-180A 106 (71.5% RC)		94.6	IT-180A	ITEQ
✓L12	Signal	Cu foil 18 μm	18μm 48		Copper Foil	Foil

Figure 3.7: Stackup design for the sTGC-L1DDC prototype-II board.

The board was designed with twelve layers and the stackup is shown in Figure 3.7. All L1DDC versions and prototypes, except prototype-1, were designed using the ALTIUM software. The dimensions of the board were selected according to the sTGC detector requirements. As was already mentioned two GBTX ASICs were used for the

For the decoupling and bypassing capacitors the recommended scheme from the VLDB board provided by the GBT-FPGA group was used. This scheme utilizes LC filtering and bulk tantalum capacitors that provide lower effective series resistance (ESR) and inductance (ESL). The decoupling and bypassing diagram implemented in all L1DDC versions and prototypes is shown in Figure 3.8.



The differential pairs were designed with 4 mil width and 4 mil (101.6 μm) separation

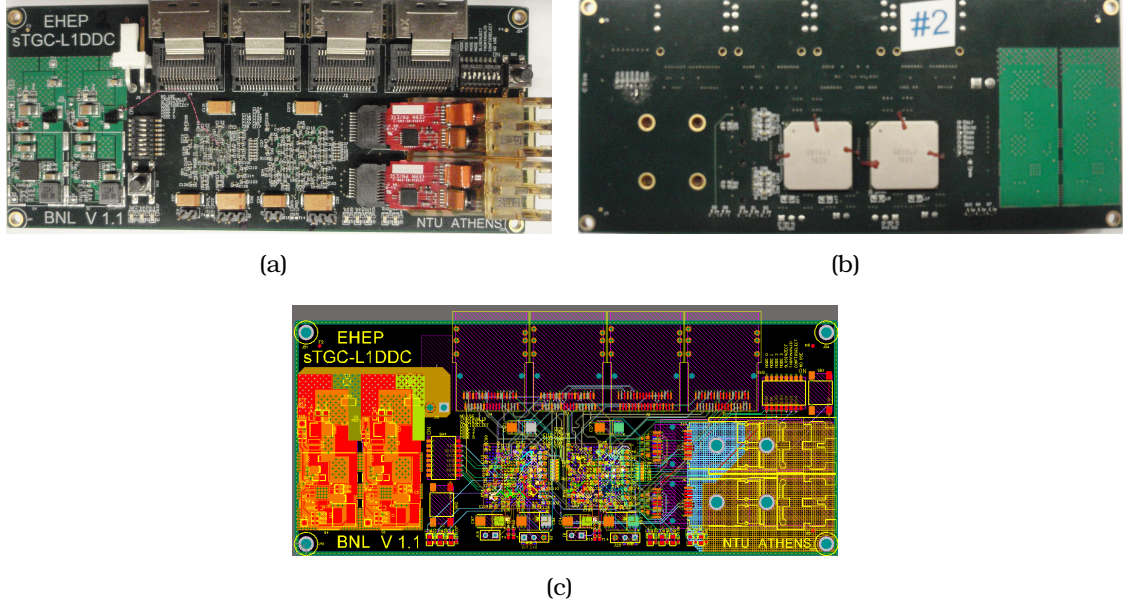


Figure 3.9: *sTGC-L1DDC Prototype-2.*(a) Top side, (b) bottom side and (c) layout.

for all layers. To avoid any phase differences in the transmitting pair and clock of each E-Link, length equalization of the differential pairs was implemented in all versions and prototypes of the L1DDC boards. Moreover to avoid any potential noise or jitter on the differential pairs introduced by vias due to impedance mismatches and reflections, the minimum possible number of vias was used (maximum two per line). Due to the limited available space caused by the 0.8 mm ball pitch of the GBTX ASIC, a separation of the differential signals should be implemented under the BGA. By rearranging the fanout vias of the BGA a separation with a maximum number of three vias was possible. This was succeeded by using common vias for the ground and power pins but also due to the unused signals of the GBTX. For the single ended signals 5 mil (127 μm) width was used for the outer layers and 6 mil (152.4 μm) for the internal ones.

A common ground for the digital and analogue pins of the GBTX was implemented according to the instructions of the GBTX designers. The unused pins of the miniSAS connector were left floating whereas the ground and shield pins were connected directly to ground. The pinout of the miniSAS is common for the three for s/pFEB and is illustrated in Figure 3.10(a). The pinout of the extra miniSAS connector used only by the inner sFEB due to the high rate as was mentioned in Section 2.4.1, is presented in Figure 3.10(b).

3.2 Prototype-2 testing

No major schematic or layout errors found on the sTGC-L1DDC prototype-2 and the boards are fully functional. A wrong value of the voltage divider network was identified and resistors were replaced. After the modification it was possible to configure the board either using the I²C dongle using a custom software or the IC channel. Power

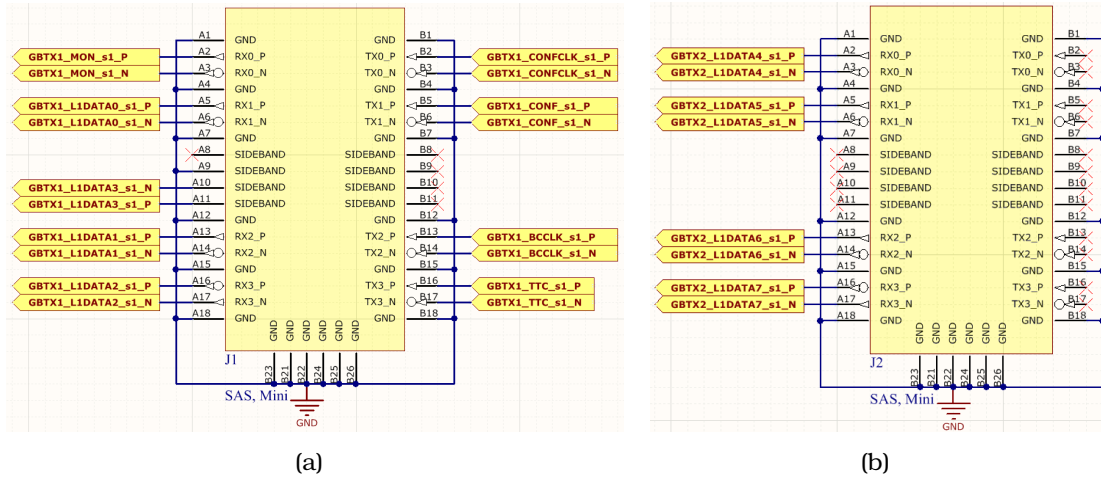


Figure 3.10: MiniSAS pinout of sTGC-L1DDC prototype-2. (a) common for all s/pFEBs and (b) extra connector of the inner sFEB.

distribution and noise measurements at the 1.5 V and 2.5 V output of the FEAST were also performed. In Figure 3.11 a screenshot of the FFT analysis for the 1.5 V FEAST output is illustrated. The RMS mean value of the noise is demonstrated to be 245.63 μV . However the switching frequency of the FEAST and it's harmonics are still visible. As it will be mentioned later in section 3.6, it was able to minimize the switching frequency and remove completely this component.

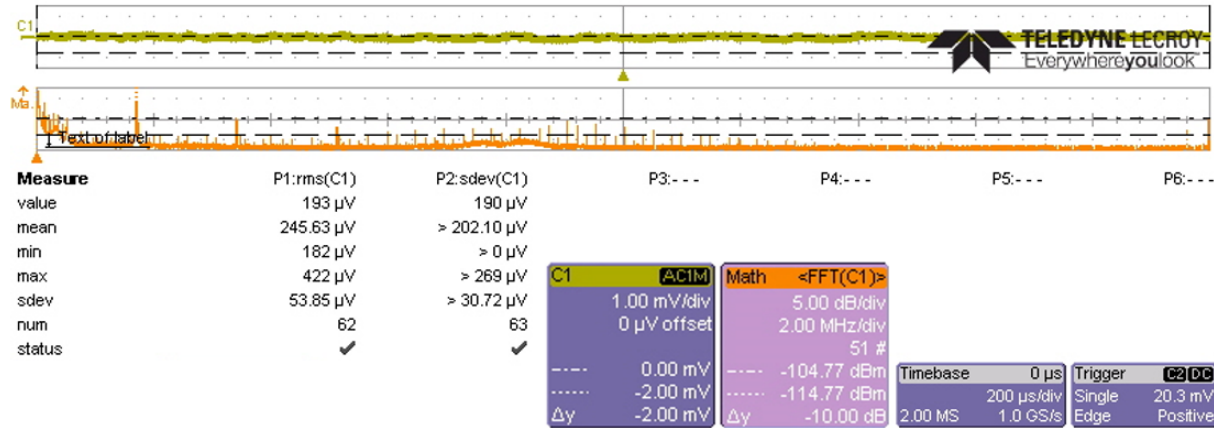


Figure 3.11: FFT of the 1.5 V FEAST output.

The boards were tested with both FELIX and evaluation boards and showed the expected behaviour. The jitter on all clock outputs of the L1DDC boards was measured by using the Keysight E5052B Phase Noise Analyzer. For the 40 MHz clocks the jitter measured at $\sim 8.6\text{ps}$ as shown in Figure 3.12. The jitter is calculated by the integrated bandwidth between 1 kHz and 20 MHz.

In more detail, the following tests were implemented:

- Power and noise measurements on the 1.5 V and 2.5 V FEAST outputs.

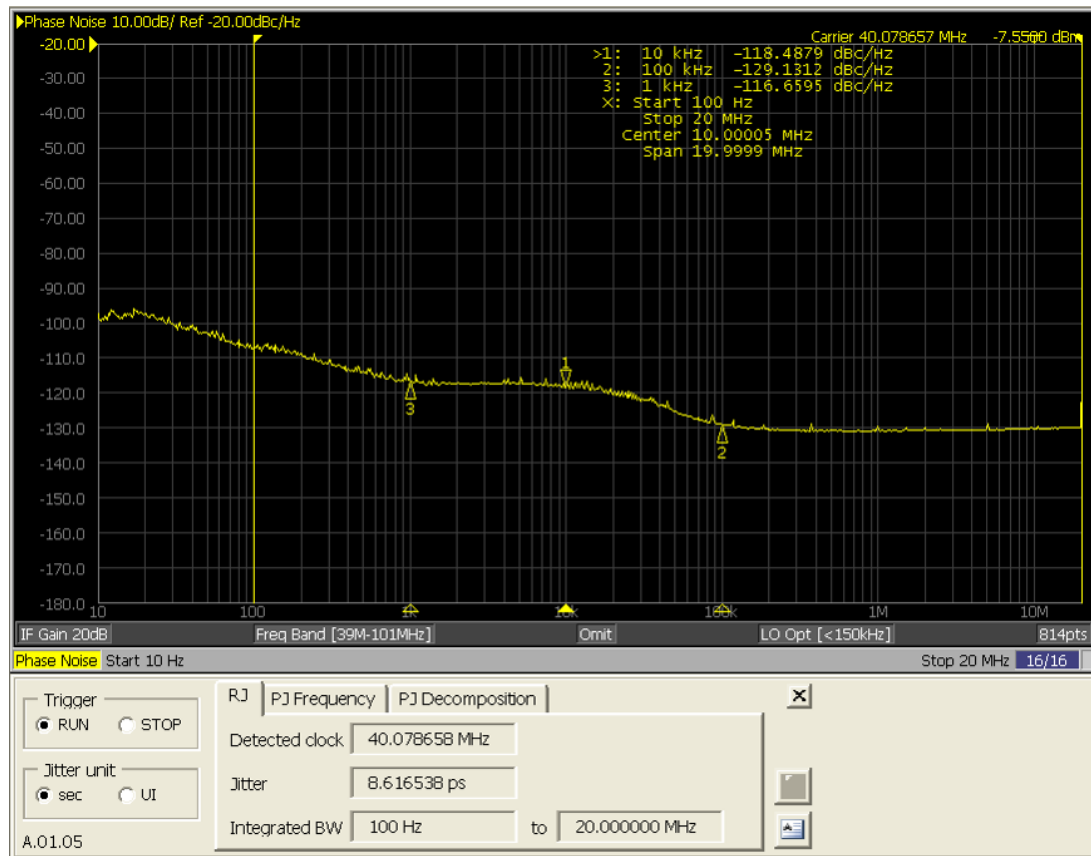


Figure 3.12: Jitter measurement on E-Link clocks at 40 MHz.

- Power and noise measurements on the GBTX input power rails.
- E-Link testing at 80, 160 and 320 Mb/s. A typical output of the tests for the E-Links at the 80 and 320 Mb/s is shown in Figure 3.13.
- GBTX internal loopback tests on the fiber side and by using FELIX and evaluation boards running the GBT-FPGA firmware, showed no errors.
- The I²C communication with the VTRX was successfully tested. All VTRX registers were configured from FELIX via the L1DDC and GBTX.

Moreover the following were achieved:

- Interface and level standards with the FEs were verified.
- SCA data were transmitted successfully to FEs from regular E-Links by using FELIX.
- TDS configuration on the pFE board was achieved with SCA data sent from FELIX via the L1DDC.

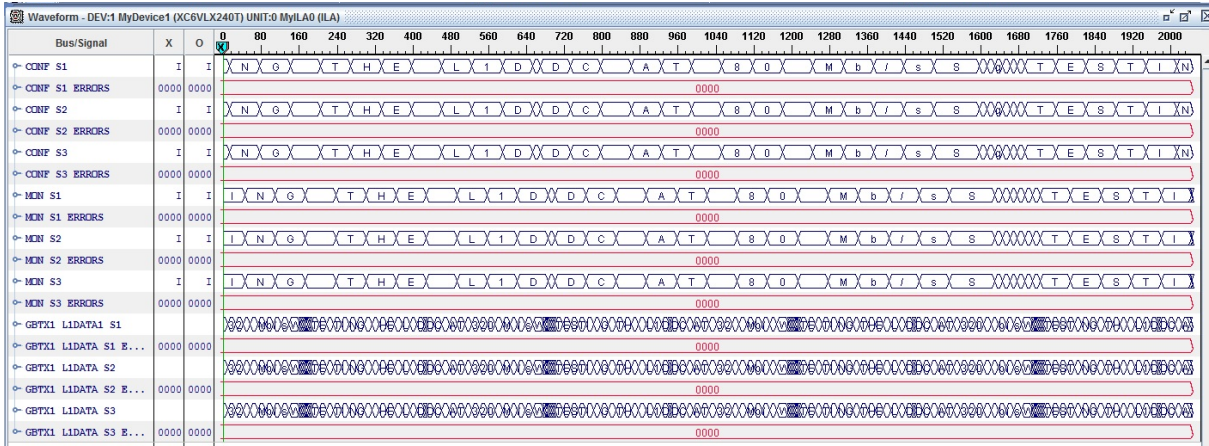


Figure 3.13: E-Link testing at 80 and 320 Mb/s on the sTGC-L1DDC board.

3.3 Prototype-3 description

The sTGC-L1DDC prototype-2 dimensions didn't satisfy the requirements of the sTGC detectors due to a conflict of the LC-LC fiber connector with the Low Voltage (LV) distributor box as shown in Figure 3.14.

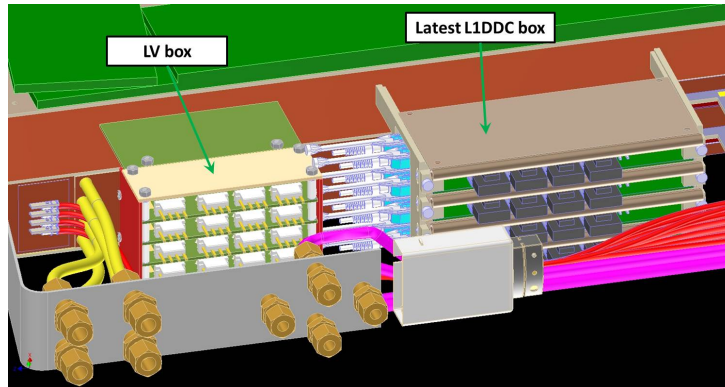


Figure 3.14: Conflict of the sTGC-L1DDC prototype-2 board with the LV boxes.

For that reason the sTGC-L1DDC layout and the board dimensions were modified. The board was designed again with twelve layers and the new stackup is shown in Figure 3.15.

Generally the following modifications were made to the sTGC-L1DDC prototype-3 compared to prototype-2:

- To avoid the conflicts the board dimensions changed from 140 mm × 60 mm to 125 mm × 60 mm. The two VTRXs were moved closer to the center of the board and the FEAST layout was redesigned.
- The FEAST layout was redesigned to reduce space and the modifications were done according to the FEAST-MP designers guidelines. This means that two 10 uF

Layer	Info	Thickness
TOP	=====	0.333+Plating
	PP IT-180A 3313	3.729(mil)
L2	=====	0.5 Oz
	Core IT-180A 0.11	4.331(mil)
L3	=====	0.5 Oz
	PP IT-180A 1080*2	5.443(mil)
L4	=====	0.5 Oz
	Core IT-180A 0.11	4.331(mil)
L5	=====	0.5 Oz
	PP IT-180A 1080*2	5.465(mil)
L6	=====	0.5 Oz
	Core IT-180A 0.51	20.078(mil)
L7	=====	0.5 Oz
	PP IT-180A 1080*2	5.443(mil)
L8	=====	0.5 Oz
	Core IT-180A 0.11	4.331(mil)
L9	=====	0.5 Oz
	PP IT-180A 1080*2	5.452(mil)
L10	=====	0.5 Oz
	Core IT-180A 0.11	4.331(mil)
L11	=====	0.5 Oz
	PP IT-180A 3313	3.729(mil)
BOT	=====	0.333+Plating

Figure 3.15: Stackup design for the sTGC-L1DDC prototype-III board.

anti-parallel capacitors were added (C2 and C7 in Figure 3.17(a)) on the output power and after the power inductor. The resistors for the voltage divider and the capacitor on the Enable pin were moved inside the shield. Finally, the GND pins (3,5,20) were isolated from PGND and were connected to the ground on the bottom layer through vias. The new layout is about 10 mm smaller comparing to previous one and is shown in Figure 3.17(b). This layout was used also for the second prototype of MM-L1DDC.

- VTRX Rx polarity found to be swapped and was corrected to this version.
- Ferrite beads for the filtering of the VTRX were completely removed as the FEAST outputs provides sufficient LC filtering.
- For the decoupling of the GBTX ferrite beads were replaced with ceramic inductors in order to avoid any potential noise coming from aircore inductors.
- All configuration pins are hardwired using resistors and some of them with a selectable option (using two resistors to GND or PWR).
- The eFuse programmability is available by adding external 3.3 V power on a two pin (2.54 mm) DIP header and using the I²C dongle.
- According to the GBTX specifications, it is very important for the reset signal (RESETB) to be released only after the supply voltage has reached at least 90% of its final value. The minimum duration of the reset pulse (RESETB = 0 V) is 1 μ s. For this reason the reset of the GBTX on the L1DDC is selectable by using a Resistor Capacitor (RC) network (connected to VDD) to provide a time delay, a push-button or the Power Good (PGOOD) signal of the FEAST.

- Differential pairs were designed with 88.9 μm (3.5 mil) width and 127 μm (5 mil) gap for all layers. This was demanded by the fabrication company in order to succeed the appropriate differential (100 Ohm) and single ended (50 Ohm) impedance. This led to a very good approximation of the final impedance varying from 99.593 Ω up to 100.013 Ω as shown in Table 3.3. To avoid any modifications and potential problems on the fabrication and the assembly process the same companies were used for all the current versions as well as for the next prototypes.
- Equalize the lengths for all the TX (at 87.249 mm) and all RX differential pairs (at 86.8172 mm).

Table 3.3: Impedance calculation for the twelve layer stackup.

Ctrl	Ref	Imp_type	Cust_req	Imp_req	FP_des	Imp_des	mask	H1	Er1	H2	Er2
L1	L2	Differential	3.5/5	100+/-10%	3.5/5	99.593	Yes	3.7 29	4.1 5		
L10	L9/L11	Differential	3.5/5	100+/-10%	3.4/5.1	99.985		4.3 31	4	6.0 52	3.95
L12	L11	Differential	3.5/5	100+/-10%	3.5/5	99.593	Yes	3.7 29	4.1 5		
L3	L2/L4	Differential	3.5/5	100+/-10%	3.4/5.1	99.965		4.3 31	4	6.0 43	3.95
L5	L4/L6	Differential	3.5/5	100+/-10%	3.4/5.1	100.013		4.3 31	4	6.0 65	3.95
L8	L7/L9	Differential	3.5/5	100+/-10%	3.4/5.1	99.965		4.3 31	4	6.0 43	3.95

The top side of sTGC-L1DDC prototype-3 is shown in Figure 3.16(a). The four miniSAS connectors (top), the power connector (top-left), the FEAST DC-DC converters (left) and the two VTRX (center-right) are visible. On the bottom side of the board, Figure 3.16(b) the two GBTX ASICs (bottom-right) and thermal pads of the FEASTs (top-right) are depicted. The layout of the board is shown in Figure 3.16(c). Five sTGC-L1DDC prototype-3 boards were submitted for fabrication in September 2017.

3.4 Prototype-3 testing

The five prototypes were extensively tested using the micro-DAQ system and an oscilloscope for the signal integrity of the data and the clock. The micro-DAQ, which is described in detail in section 6.2.1 is an independent system developed for testing the L1DDC boards and comprises the VC709 evaluation board from Xilinx, a custom (FMC) (the board is described in Section A.3.1) and a clock synthesizer. No errors were identified and the boards were fully functional. All boards were eFused successfully using the I²C dongle and the noise measurements performed on the FEAST output voltage and GBTX power rails. The Keysight E5052B phase noise analyser was used also to evaluate the jitter on the BC clocks. The clocks appear to have better performance compared to prototype-2 and the Random Jitter ranges from 5.6 ps up to 6.8 ps as shown in Figure 3.18.

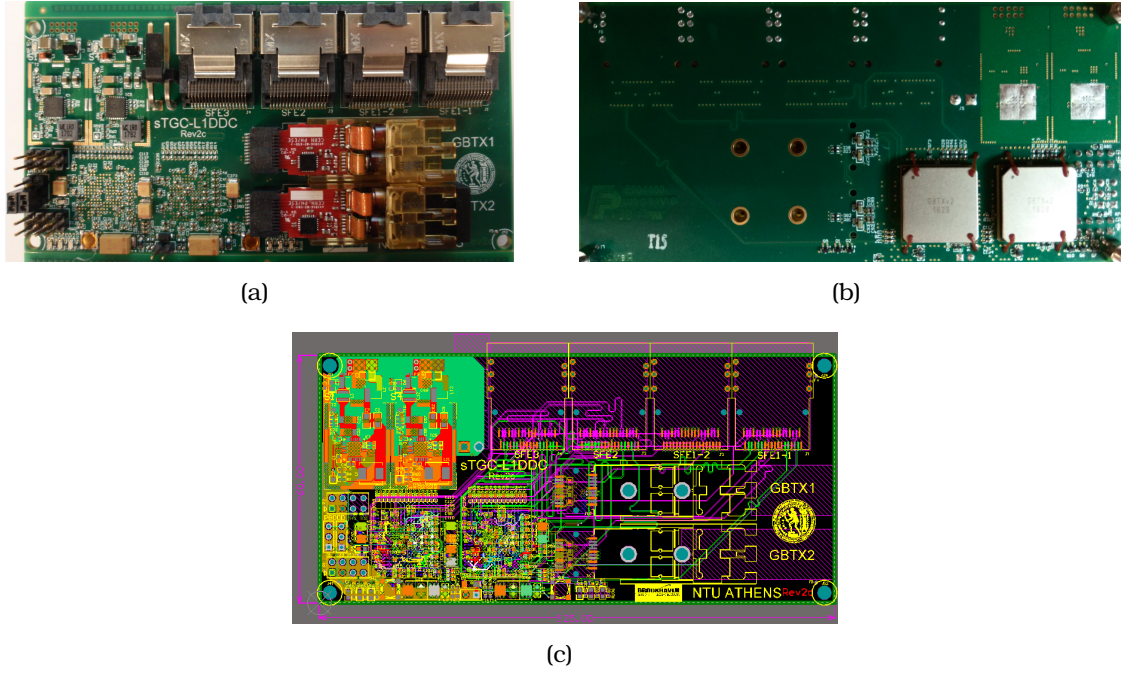


Figure 3.16: (a) top side, (b) bottom side and (c) layout of sTGC-L1DDC Prototype-3 board.

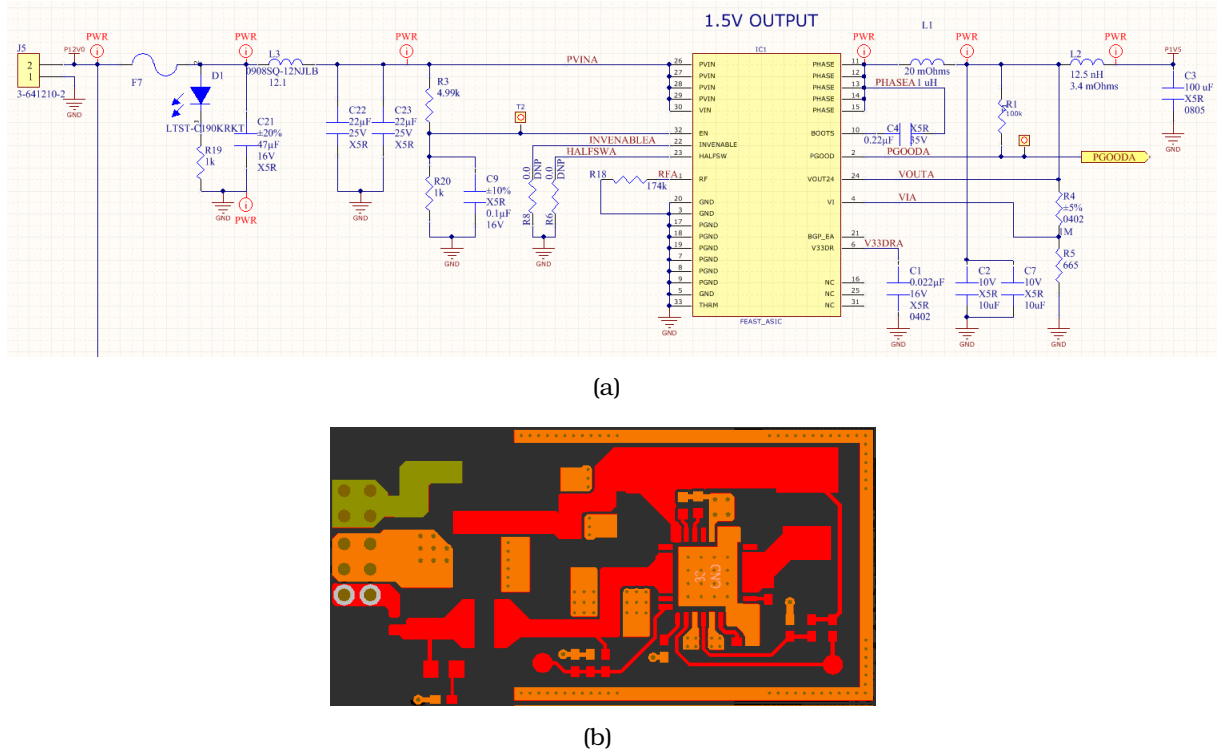


Figure 3.17: (a) Schematics and (b) layout of FEAST on L1DDC prototype-2 boards.

Moreover the boards were tested with the final trigger and readout chain during the various integration weeks with the final boards (Router, PAD trigger and pFEB/sFEB).

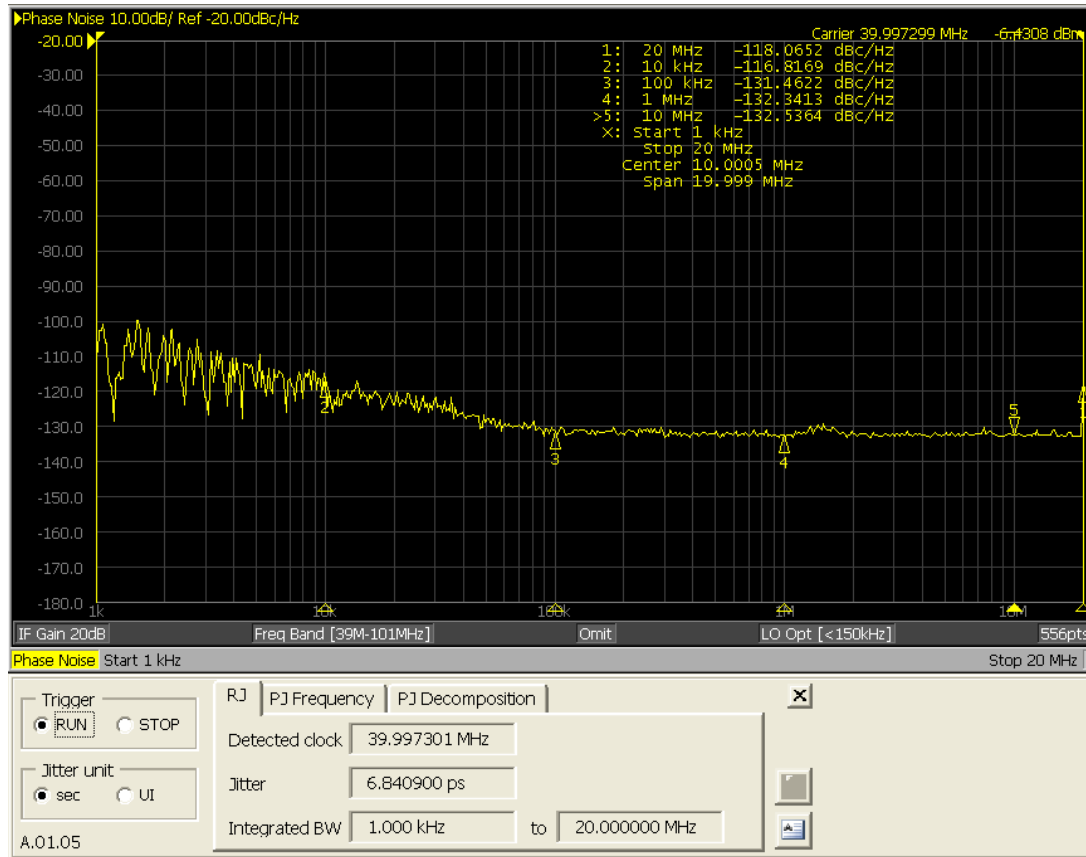


Figure 3.18: Jitter measurement on the 40 MHz E-Link clock.

3.5 Prototype-4 description

At that time it was requested to add a SCA ASIC on the board for environmental monitoring. For that reason two extra thermistors were added for measuring the temperature of the two GBTXs. Furthermore an extra power connector was added to power on the repeaters needed for the proper transmission of the data on the trigger path of the sTGC detectors as is described in Chapter 6.3. The Molex Nano-Fit PCB connector with part number 105313-1302 (mating with the cable connector - part number: 105307-1202) was selected due to its small size. This connector is rated up to 6.5 A and 250 V AC/DC and the material is Nylon Liquid Crystal Polymer (LCP) UL 94V-0 halogen free and compliant with CERN regulations. The pinout that was selected is shown in Figure 3.19(b) with the circuit one being the ground as indicated in the data-sheet (Figure 3.19(c)).

By adding the SCA and the extra power connector there was limited space for the FEAST layout. That was the reason that the layout of the FEAST was modified again. The new dimensions are 30.61 mm × 11.735 mm compared to the 31 mm × 15 mm that was before. To succeed this the test points were removed, 0201 components and new custom shields were used. The comparison between the old and the new FEAST layout is shown in Figure 3.20. New shields for the FEAST DC-DC converters were ordered by

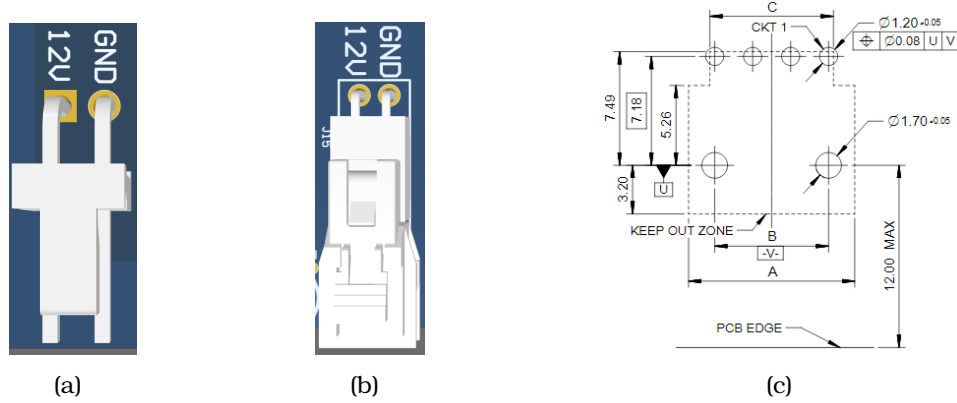


Figure 3.19: sTGC-L1DDC power connector pinout: (a) prototype-2 and prototype-3, (b) prototype-4 and pre-production, (c) Data-sheet pinout.

Orbel. The material is Nickel silver - Copper alloy 770 and the thickness of the shield is 0.381 mm. Chemistry Data: Alloy 770 Nickel Silvers (Copper, Nickel, Zinc) 55% Copper, 27% Zinc, 18% Nickel and the specifications are: ASTM B122, ASTM B151, QQ W321, SAE J461, UNS C77000. More details about the shield can be found at: [data sheet](#). Furthermore the PTAT signal for temperature monitoring of the FEAST ASIC was also connected to the ADC of the SCA.

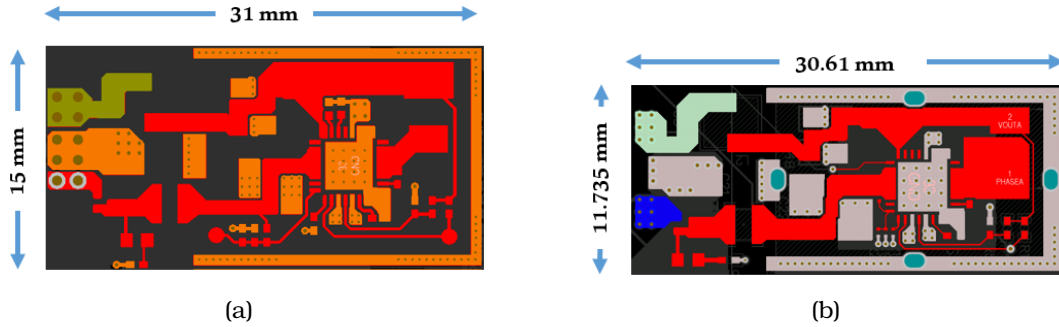


Figure 3.20: (a) FEAST layout that was used for prototype-3 Micromegas and sTGC boards. (b) Modified layout for the final boards.

The Molex miniSAS connector was replaced by the 8AB36-2220-LJ from 3M. The latter has better quality materials and is considered crucial for the signal integrity. The insulator material is again high temperature thermoplastic glass filled (UL 94V-0), the shell is stainless steel with wiping area of 0.76 μm Nickel, contacts are of 0.76 μm minimum gold over 2.54 μm nickel and solder tails of 2.54 μm . Due to the limited space the eight and three pin 2.54 mm DIP headers for the efusing and IC/I²C configuration of the GBTXs were replaced with DIP headers of 2 mm and 1.27 mm pitch respectively.

The output voltage driven by the DC-DC converter consists of AC components. Thus it is of a crucial need to remove those AC ripples for noise reduction and potential increment on the jitter of the output clock of the GBTX. To increase the efficiency of the GBTX power input filtering an extra capacitor was added to form a pi filter. The pi filter is basically an Inductor Capacitor (LC) filter with an additional capacitor at

the input. The construction arrangement of all the components resembles the shape of Greek letter Pi (Π). By performing that the output of the FEAST is directly applied to the input capacitor. The capacitor provides a low impedance to AC ripples present in the output voltage and high resistance to DC voltage. Therefore, most of the AC ripples get bypassed through the capacitor at the input stage only. The residual AC components which are still present are filtered when they pass through the inductor coil and through the capacitor connected parallel across the load. By this way, the efficiency of filtering increases multiple times. The ceramic inductors were replaced with shielded ones since the latter can provide much higher inductance at a similar footprint. The inductor selected for this purpose was the 74438324010 from Würth Electronics Inc. with 1 μ H, nominal current of 2.8 A and 60 mOhm DC resistance. The board utilizes twelve layers

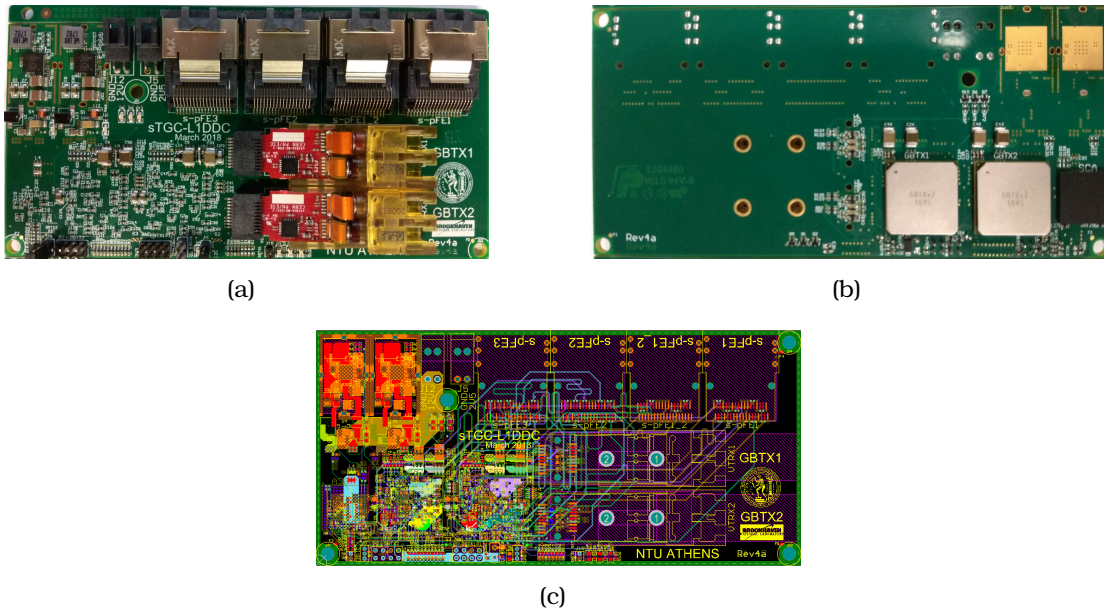


Figure 3.21: *sTGC-L1DDC Prototype-4 board, (a) top side, (b) bottom side and (c) layout.*

and no modifications were performed on the stackup compared to prototype-3. Same rules and settings for the differential pairs and the single ended signals were used. The sTGC-L1DDC prototype-4 is shown in Figures 3.21(a), 3.21(b) and the layout in Figure 3.21(c). Five sTGC-L1DDC prototype-4 boards were submitted for fabrication in September 2017.

Finally, it was also requested to change the bank of the BC clock and TTC data to simplify the FELIX firmware. This was the reason that both signals were moved from bank 1, channel 0 of the GBTX to bank 2, channel 0 as shown in Table 3.4.

3.6 Prototype-4 testing

All boards were eFused successfully by using the I²C dongle. Prototype-4 boards were tested again with the Agilent E5052B phase noise analyser to verify the jitter performance of the 40 MHz clock. On all boards the two out of the three output clocks

Table 3.4: GBTX bank configuration of sTGC-L1DDC boards. Orange color indicate the signals for prototype-2 and 3 (Bank 1, channel 0) that were moved to Bank 2, channel 0 in prototype-4 and pre-production boards.

		GBTX1			GBTX2		
		DIO	DIN	DCLK	DIO	DIN	DCLK
BANK0	0	SCA sFE1	SCA sFE1	SCA CLK			
	1	SCA sFE2	SCA sFE2	SCA CLK			
	2	SCA sFE3	SCA sFE3	SCA CLK			
	3						
	4						
	5						
	6						
	7						
BANK1	8	TTC sFE1	L1DATA0 sFE1	BCCLK sFE1		L1DATA4 sFE1	
	9						
	10						
	11						
	12		L1DATA1 sFE1			L1DATA5 sFE1	
	13						
	14						
	15						
BANK2	16	TTC sFE1	L1DATA2 sFE1	BCCLK sFE1		L1DATA6 sFE1	
	17						
	18						
	19						
	20		L1DATA3 sFE1			L1DATA7 sFE1	
	21						
	22						
	23						
BANK3	24	TTC sFE2	L1DATA0 sFE2	BCCLK sFE2		L1DATA2 sFE2	
	25						
	26						
	27						
	28		L1DATA1 sFE2			L1DATA3 sFE2	
	29						
	30						
	31						
BANK4	32	TTC sFE3	L1DATA0 sFE3	BCCLK sFE3		L1DATA2 sFE3	
	33						
	34						
	35						
	36		L1DATA1 sFE3			L1DATA3 sFE3	
	37						
	38						
	39						

had similar jitter (about 7 ps) comparable to sTGC-L1DDC prototype-3. The BC clock output of the bank two, channel zero appeared to have an extremely high jitter of about 70 ps as shown in Figure 3.22.

Using an oscilloscope to monitor the signal it appeared that there is a deformation on the positive edge of both pairs of the clock. This deformation is caused by enabling the training mode of another bank of the GBTX (bank 3, channel 0). By disabling the training mode that causes this effect the jitter is reduced to the same level of the other two output clocks. In Figure 3.23(a) the output clock of the Bank two, channel zero with the training mode of Bank three, Channel zero disabled is presented and in Figure 3.23(b) the same clock with the training mode enabled. The deformation is not a coupling effect or a malfunction on the board but is caused by the GBTX ASIC itself. The phase noise analyser interprets this waveform as a jitter. This issue identified is not crucial as in the final setup the manual mode will be used.

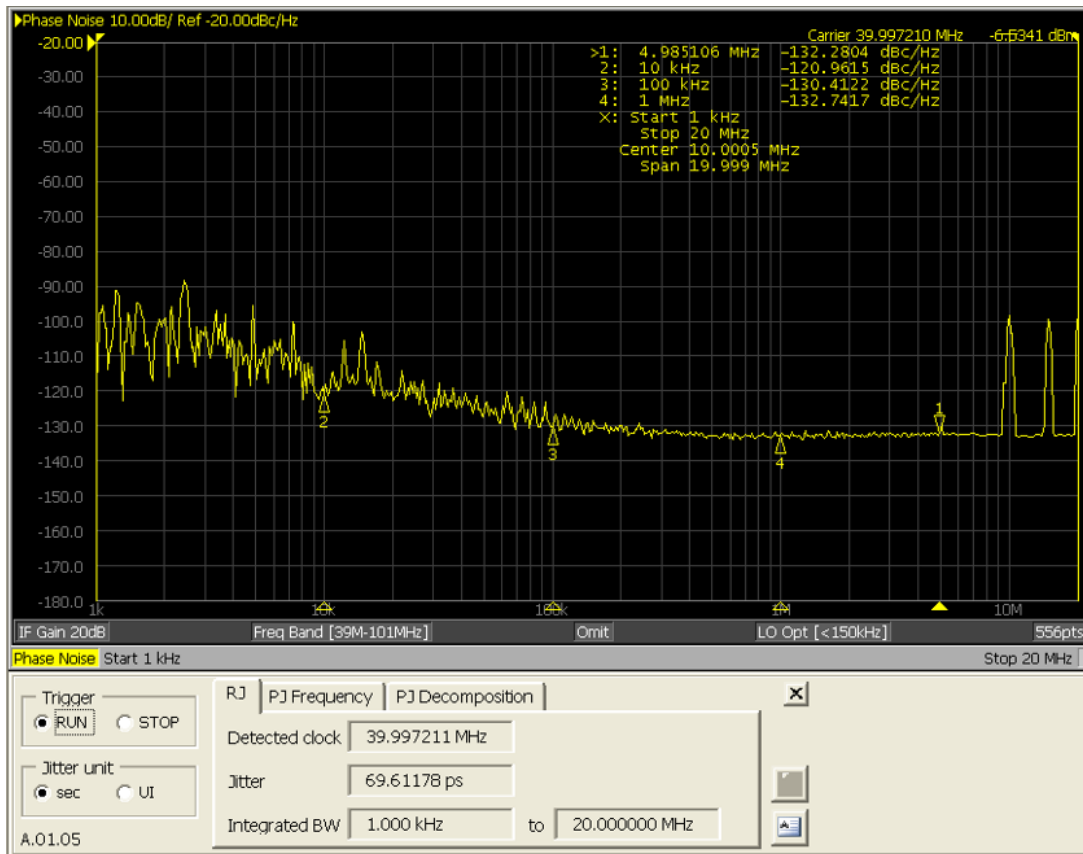


Figure 3.22: Extremely high jitter measured at the *STGC-L1DDC BC* clock.

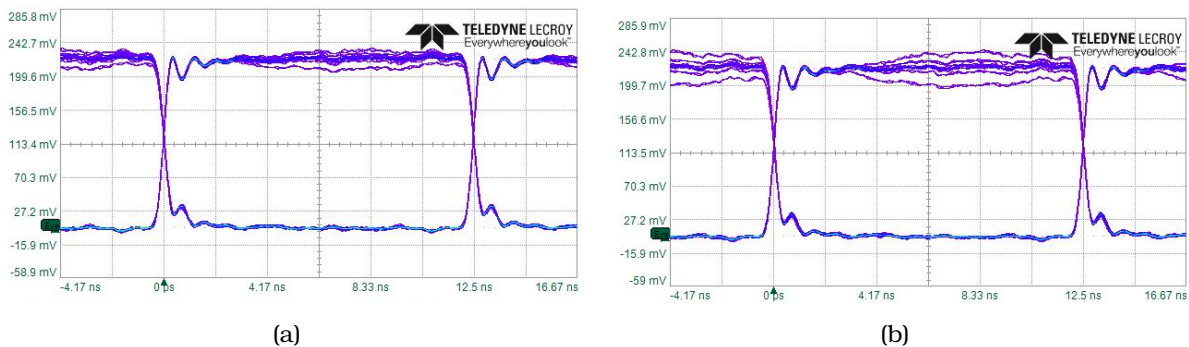


Figure 3.23: Deformation on the waveform for the 40 MHz *BC* clock (Group 2, channel 0) by enabling the training mode for group 3, channel 0.

A 10 μF 0805 capacitor by Yageo with a Self Resonant Frequency of about 1.5 MHz and extremely low ESR (about 2 m Ω at 800 kHz and less than 5 m Ω) for wide range of frequencies ($10 \text{ kHz} < f < 5 \text{ MHz}$) appeared to be ideal for filtering the FEAST DC-DC switching noise. The Impedance and Self Resonant Frequency (SRF) of the capacitor are shown in Figure 3.24(a).

Moreover, 220 μF bulk capacitors were used to overcome the voltage drops caused by the inductive effects of PCB traces (inherent inductance). The JMK325ABJ227MM-T

with 1210 footprint and ESR value smaller than 1 m Ω between 30 kHz and 200 kHz was selected. The ESR and SRF values of the 220 μ F capacitor are shown in Figure 3.24(b).

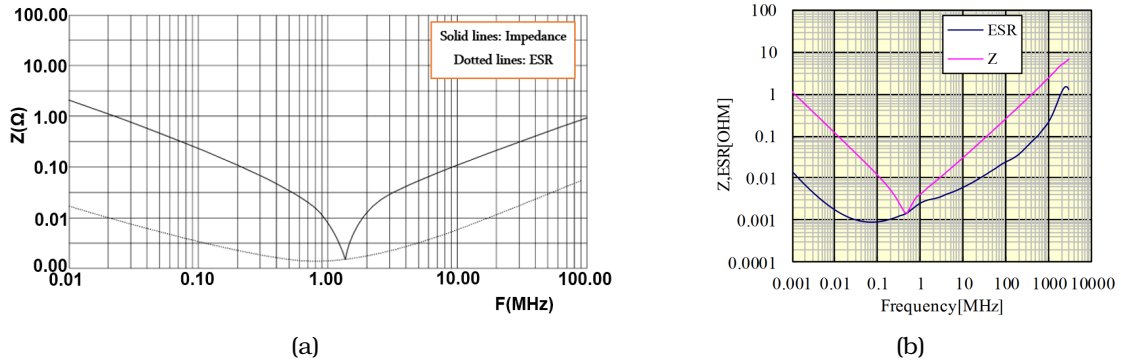
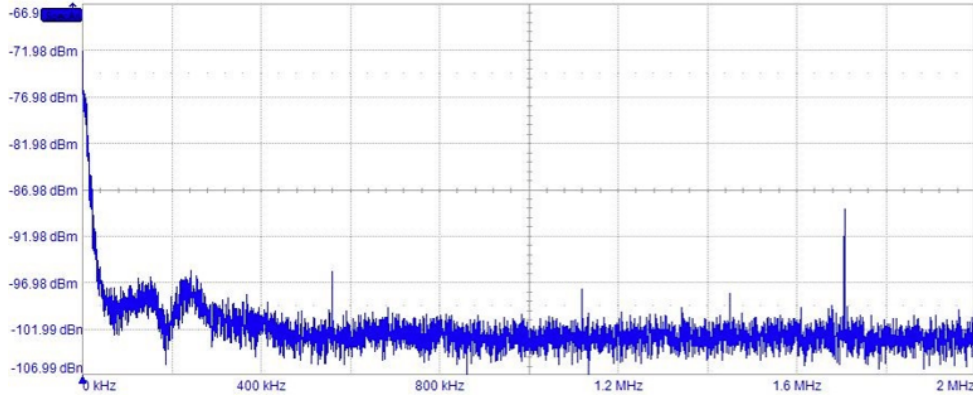


Figure 3.24: Impedance and ESR versus frequency characteristics for the (a) 10 μ F CC0805KRX5R5BB106 ceramic capacitor by Yageo and (b) 220 μ F JMK325ABJ227MM-T by Taiyo Yuden.

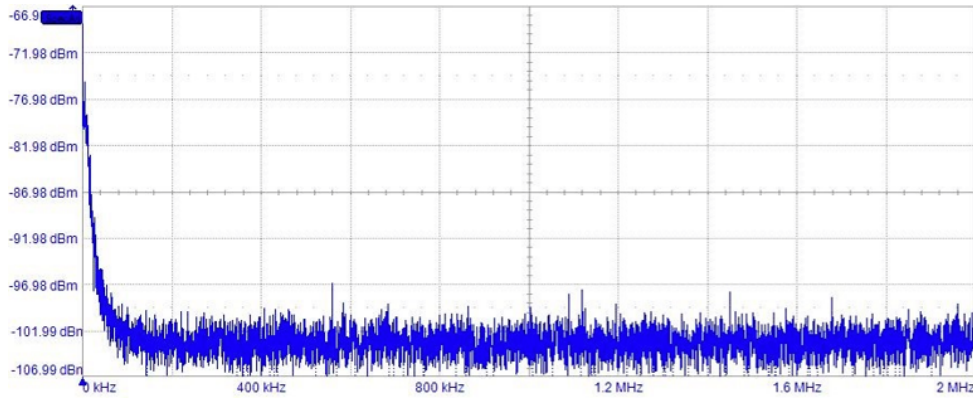
All power rails of the board were measured and analysed with FFT using an oscilloscope. On the 1.5 V FEAST output power, the spike on the FFT spectrum at 1.7 MHz as illustrated in Figure 3.25(a) is created due to the switching frequency of the FEAST ASIC. If we repeat the same measurement after the pi filtering and at the input power rails of the GBTX, we can see clearly that the component caused by the FEAST is completely removed and the rms value is 246 μ V as it is shown in Figure 3.25(b). Moreover low frequency noise appeared at the FEAST output is also removed by the filter. Since sTGC-L1DDC prototype-4, MM-L1DDC pre-production and RIM-L1DDC prototype-2 utilize the same filtering scheme, they show similar performance.

All data lines were tested with the micro-DAQ system and no errors appeared even after 24 hours of continuous operation. The SCA communication was verified by using both micro-DAQ and OpcUA server. Reconfiguration of the GBTX using the IC channel was also successful. The sTGC-L1DDC board was tested extensively with the final boards and FELIX. It was used to provide the 40 MHz reference clock for the ROC ASIC, to configure the FE ASICs (VMM, ROC, TDS) and for reading out the Level-1 data. Thermal measurements performed on the sTGC-L1DDC prototype-4 board using the FLIR E6 thermal camera. On the top side of the board the component that dissipates more heat is the VTRX with temperature of 62.4 $^{\circ}\text{C}$ as shown in Figure 3.26(a). On the bottom side is obvious that the GBTX and the FEAST DC-DC converters dissipate most of the heat with the GBTX temperature rising at 52.4 $^{\circ}\text{C}$ as shown in Figure 3.26(b). In the aforementioned measurements no cooling was used. The high temperature of the VTTX led to a new cooling scheme including also the top side of the board (areas above VTTX/VTRX and especially the GBLD ASICs).

The 74438324010 shielded inductor with 1 μ H and the ILHB0603ER600V ferrite bead with relatively small footprint showed good performance and proved to be ideal for the GBTX and VTRX filtering respectively. Up to this point it was not clear if and which ferrite beads or inductors can be affected by the magnetic field. The presence of the 0.4 T magnetic field has an impact in inductance reduction and thus a variety of

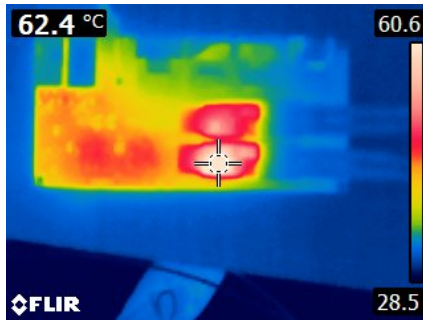


(a)

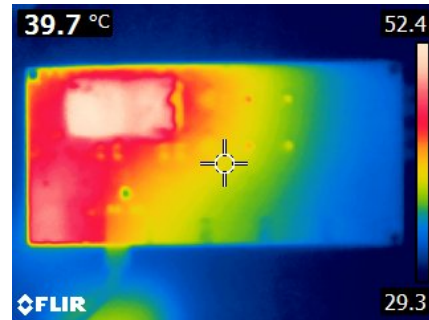


(b)

Figure 3.25: FFT analysis of the 1.5 V FEAST (a) direct output, (b) after the pi-filter.



(a)



(b)

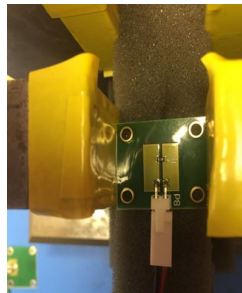
Figure 3.26: Thermal analysis of the sTGC-L1DDC prototype-4 board, (a) top side and (b) bottom side.

different components were tested by K. Johns et al. of the University of Arizona. The components that were tested are presented in Table 3.5. The ferrite beads showed significant reduction on their inductance and were replaced by the 74438313010. These shielded inductors appeared to have good performance under magnetic field and have a relative small footprint. For the purpose of this test various components were placed

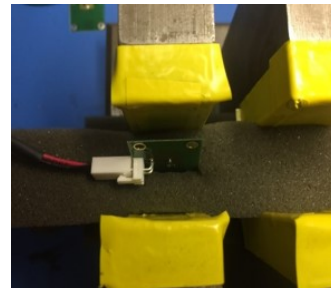
in parallel and perpendicular to the magnetic field as shown in Figures 3.27(a) and 3.27(b) respectively.

Table 3.5: Ferrite beads and inductors that were tested under magnetic field.

Part Number	Discription	Value	az b=0	az position1=0.4T	az position 2=0.4T
0908SQ-17NGLB	INDUCTOR AirCore 16.6nH 4.4A SMD	16.6nH	0.0213	0.0213	0.0212
74437334010	INDUCTOR POWER 1uH 5A3 2-SMD	1uH	0.9584	0.3046	0.8080
A04TGLB	IND_12n5H_4A0_0R0034_3G4Hz	12.5nH	0.0177	0.0182	0.0184
74404024022	2.2uH Shielded Wirewound Inductor 1.8A 80 mOhm Nonstandard _260MHz	2.2uH	2.1578	0.2356	0.2242
DFE252012P-1R0M=P2	FIXED IND 1uH 4.3A 42 MOHM SMD	1uH	0.9483	0.0529	0.1639
LQH2HPN1R5NJRL	FIXED IND 1.5uH 1.08A 90 MOHM	1.5uH	1.3363	0.1792	0.1684
MLZ2012M1R0HT000	Fixed Inductors 1 uH 20%	1uH	1.6650	-0.0561	-0.0470
ECS-MPI2520R1-1R5-R	Fixed Inductors 1.5uH +/-20% 2.9A -40C +105C	1.5uH	1.5113	0.3345	0.4931
ECS-MPI2520R0-1R5-R	Fixed Inductors 1.5uH +/-20% 2.4A -40C +105C	1.5uH	1.2648	0.2937	0.6562
ECS-MPI2520R1-3R3-R	Fixed Inductors 3.3uH +/-20% 1.8A -40C +105C	3.3uH	3.1112	0.6592	0.9408
ECS-MPI2520R1-1R0-R	Fixed Inductors 1.0uH +/-20% 3.7A -40C +105C	1.0uH	0.8091	0.1785	0.3002
ECS-MPI2520R1-2R2-R	Fixed Inductors 2.2uH +/-20% 2.3A -40C +105C	2.2uH	1.9869	0.4307	0.7851
IHLP2525CZER1R0M01	Fixed Inductors 1uH 20%	1uH	0.9502	0.3501	0.5249
ILHB0603ER600V	Ferrite Beads 60ohms 25%	0.25uH	0.3069	-0.0245	0.0066
74438343010	Fixed Inductors WE-MAPI SMD 2010 1.0uH 1.8A	1uH	0.9831	0.3550	0.5995
74438313010	Fixed Inductors WE-MAPI SMD 1610 1.0uH 1.4A 159mOhm	1uH	0.9740	0.3783	0.5985
74437334010	Fixed Inductors WE-LHMI Powr SMD5020 1uH 5.3A 20mOhm	1uH	0.9901	0.3118	0.6444
74437346100	Fixed Inductors WE-LHMI Powr SMD7030 10uH 3.0A 85mOhm	10uH	9.0692	2.8531	5.8242
ILHB0603ER121V	Ferrite Beads 120ohms 25%	0.404uH	0.4879	0.0157	0.0105
74438321010	Fixed Inductors WE-MAPI SMD 2506 1.0uH 1.25A 196mOhm	1uH	0.9860	0.2476	0.7403



(a)



(b)

Figure 3.27: Testing setup of inductors and ferrite beads. Position 1 (a) is parallel and position 2 (b) is perpendicular to the magnetic field.

Finally in order to select the proper pi-filter for minimizing the noise on the input power rails of the GBTX a set of tests were performed. The tests were motivated by the high unavailability and small variety of inductors/ferrite beads that show good behaviour under the magnetic field. For these tests different components were used to form the pi-filtering and in some cases the one capacitor was removed to see the effect of the LC filter. The seven different configurations implemented and the jitter of the output clocks measured on the same connector for different LC/pi-filters are shown in Figure 3.28. It is obvious that there is no significant change in the performance of the jitter for all clocks according to the plots.

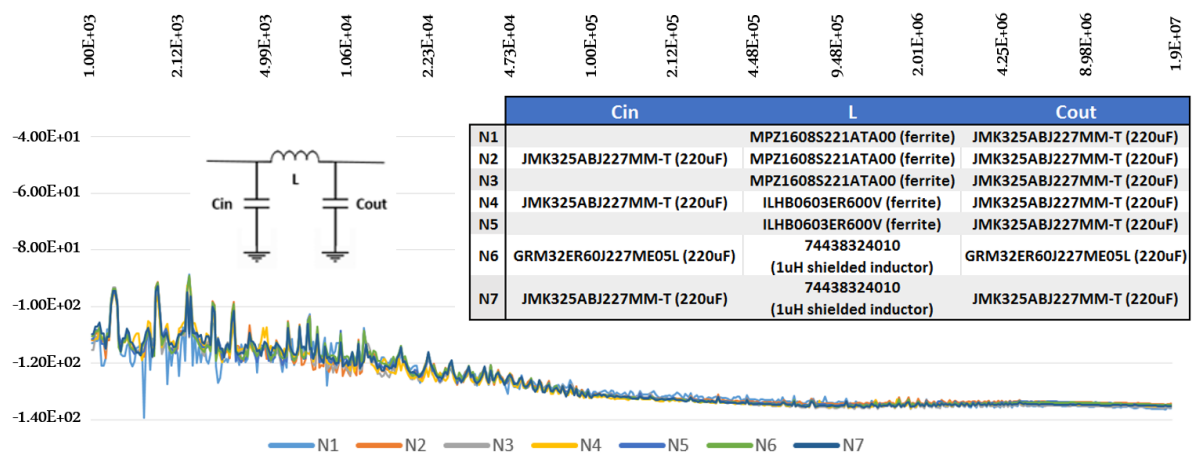


Figure 3.28: Output jitter for different filters.

3.7 Pre-Production

In January 2019 the pre-production of the 50 sTGC-L1DDC boards was launched. Minor modifications were made to the board. The top and bottom layers were poured with copper for better isolation of the internal layers. Sufficient stitching vias were placed to the bottom right area of the board as shown in Figure 3.29(c) for better connectivity of the ground pours. The copper areas of the power planes underneath the FEAST layout were replaced with ground areas to eliminate any potential induced noise to the power rails of the board. Top soldering opening was added to the FEAST shield for proper soldering as shown on the top left side of Figure ???. The bottom side of the board is illustrated in Figure 3.29(b). This can reduce the radiated EMI noise produced by the power inductor of the FEAST. The PCB material used is IT-180A (Glass Transition Temperature (Tg) - DSC 80°C and Decomposition Temperature (Td) 350°C). Finally ferrites for the VTRX filtering were replaced by shielded inductors (Part No:74438313010) from Wurth Electronics Inc. that were tested under magnetic field as described in the previous section.

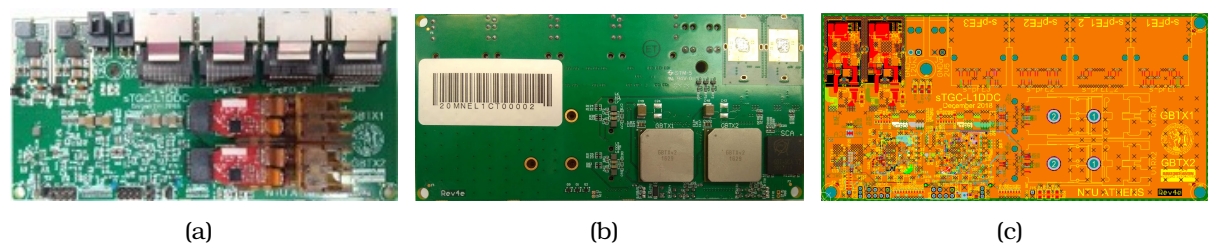


Figure 3.29: sTGC-L1DDC pre-production board, (a) top side, (b) bottom side and (c) layout.

Chapter 4

MM L1DDC board

In this Chapter the L1DDC prototype-2 board which was designed according to the MM detector requirements and ATLAS compliance rules is described. As was mentioned in section 2.4.1 different L1DDC boards were fabricated for sTGC and MM detectors for the 1 MHz readout rate.

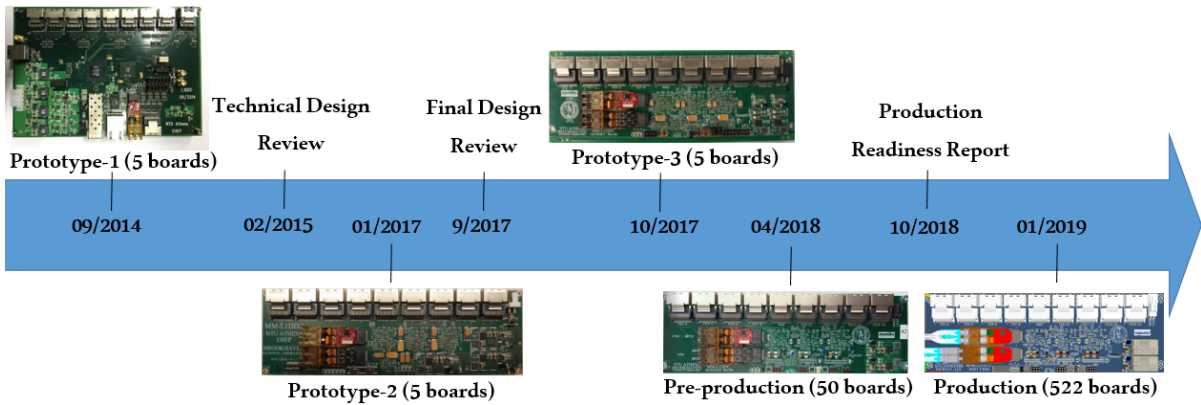


Figure 4.1: MM-L1DDC roadmap.

The roadmap for the production of the 522 boards comprised in total three prototypes and three reviews. After the first common prototype and the Technical Design Review in February 2015, five boards of the second prototype were designed and fabricated in January 2017. The Final Design Review was passed successfully in September 2017 and five boards of the third prototype fabricated in October 2017. This is also the reference board for the pre-production which was launched in April 2018 with 50 boards. No significant changes were made to pre-production boards and after exhaustive tests and the Production Readiness Report in October 2018 the production of the 522 boards started in January 2019. The design rules and requirements, modifications, issues identified and tests performed to all prototypes are presented in this chapter.

4.1 Prototype-2 board description

According to the micromegas detectors the available space for the placement of the boards is $200\text{ mm} \times 60\text{ mm}$. Thus the positioning holes for all on detector electronics in micromegas case were set to $55\text{ mm} \times 195\text{ mm}$ (2.5 mm from each edge of the boards). Due to the 1 MHz readout which has a significant impact on the design of the MM-L1DDC, the width of the board increased to 64 mm. This provided more flexibility on the component placement and routing.

The layout of the micromegas detector and hole distances are illustrated in Figure 4.2. In this figure the MM-L1DDC (not placed in the right position) is also shown for comparison. All boards must not exceed the detector envelope, which means that the board holes on the outer side (miniSAS side) must be placed at 2.5 mm from the edge. For the MM-L1DDC, the inner holes were placed at 6.5 mm from the edge to meet the detector requirements.

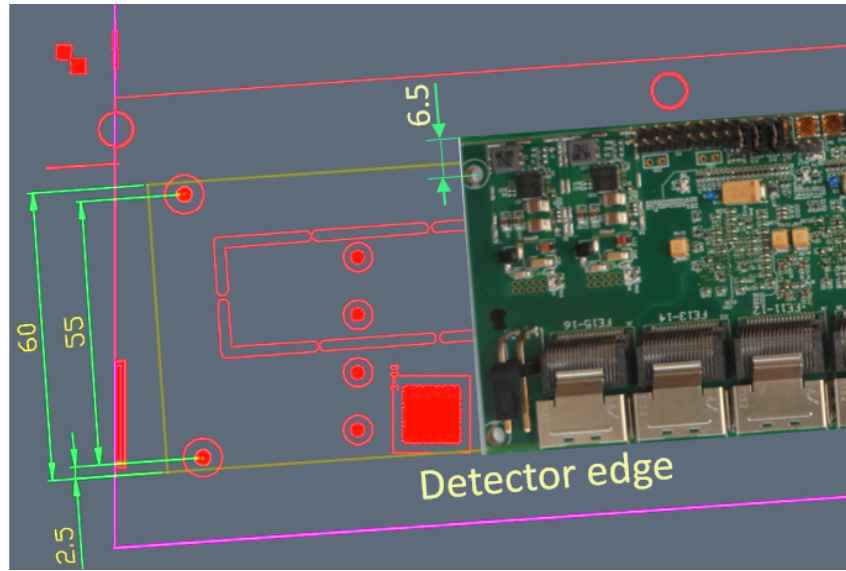


Figure 4.2: Micromegas layout for the positioning of the boards. Distances are in mm.

For the differential pairs $101.6\text{ }\mu\text{m}$ (4 mil) gap and $101.6\text{ }\mu\text{m}$ (4 mil) width were used. The PCB was designed with sixteen layers and the fabrication company modified the original stackup with a total width $< 2.5\text{ mm}$ to achieve the 100Ω and 50Ω impedance for the differential pairs and the single ended signals respectively. The new stackup shown in Figure 4.3, led to a total thickness of 2.6 mm. The overall height of the board is approximately 15.5 mm (10 mm for the VTRX, 2.6 mm for the PCB thickness and 3 mm for the GBTX ASIC on the bottom side) and a 4 mm spacer will be used to place the board on the micromegas chamber.

Five boards of MM-L1DDC prototype-2 were fabricated in January 2017. Concerning the power distribution scheme, the L1DDC requires two different voltage levels: 1.5 V for the GBTX ASICs and 2.5 V for the VTRX. Initial estimation on power consumption for the MM-L1DDC prototype-2 led to an additional FEAST DC-DC converter for the 1.5 V. The power consumption of the MM-L1DDC prototype-2 was estimated to be approximately 15 W. This calculation included the maximum power consumption of














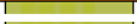














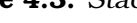

Lyr		Thick	Weight	Foil Type	Prepreg/Core Thickness	
1	s		0.0525	0.34	Standard	
0			0.0688			
2	s		0.1850	0.50	Standard	1x1080PV170 Panasonic R-1650V
3	s		0.1850	0.50	Standard	0.1500 Panasonic R-1650V
0			0.0618			1x1080PV170 Panasonic R-1650V
0			0.1167			1x2116PV170 Panasonic R-1650V
4	s		0.1850	0.50	Standard	0.1500 Panasonic R-1650V
5	s		0.1850	0.50	Standard	
0			0.0618			1x1080PV170 Panasonic R-1650V
0			0.1168			1x2116PV170 Panasonic R-1650V
6	s		0.1850	0.50	Standard	0.1500 Panasonic R-1650V
7	s		0.1850	0.50	Standard	
0			0.0618			1x1080PV170 Panasonic R-1650V
0			0.1168			1x2116PV170 Panasonic R-1650V
8	s		0.1850	0.50	Standard	0.1500 Panasonic R-1650V
9	s		0.1850	0.50	Standard	
0			0.1168			1x2116PV170 Panasonic R-1650V
0			0.0618			1x1080PV170 Panasonic R-1650V
10	s		0.1850	0.50	Standard	0.1500 Panasonic R-1650V
11	s		0.1850	0.50	Standard	
0			0.1168			1x2116PV170 Panasonic R-1650V
0			0.0618			1x1080PV170 Panasonic R-1650V
12	s		0.1850	0.50	Standard	0.1500 VT-901
13	s		0.1850	0.50	Standard	
0			0.1168			1x2116PV170 Panasonic R-1650V
0			0.0618			1x1080PV170 Panasonic R-1650V
14	s		0.1850	0.50	Standard	0.1500 Panasonic R-1650V
15	s		0.1850	0.50	Standard	
0			0.0688			1x1080PV170 Panasonic R-1650V
16	s		0.0525	0.34	Standard	

Figure 4.3: Stackup design for the MM-L1DDC prototype-II board.

the three GBTX, one GBTIA, three GBLD, one SCA, as long as two fanout chips. In this calculation a margin of 30% and 66% efficiency of the FEAST were added. The cooling of the FEAST will be through the bottom side of the board with the help of sufficient vias and copper islands. A common ground for the digital and analogue pins of the GBTX was used according to the GBTX designers instructions. In Figure 4.4(a) the top side of the MM-L1DDC prototype-2 board is illustrated. The miniSAS connectors (top), the power connector (top right), the FEAST ASIC without the shields (right) and the VTRX/VTTX optical transceivers/transmitters (left) are shown. On Figure 4.4(b) the bottom side of the board is presented. The three GBTX, the SCA and the fanout chips are the only components placed on the bottom side as depicted in the center of the board. Finally, the layout of the board with all layers enabled is shown in Figure 4.4(c).

Due to the lack of output E-Links at 320 Mb/s for the TTC data two 1:2 fanout chips from Microchip Technology (Part No: SY54011RMG) were used. This fanout chip has a maximum rate of 3.2 Gb/s with less than 300 ps propagation delay, less than 50 fs

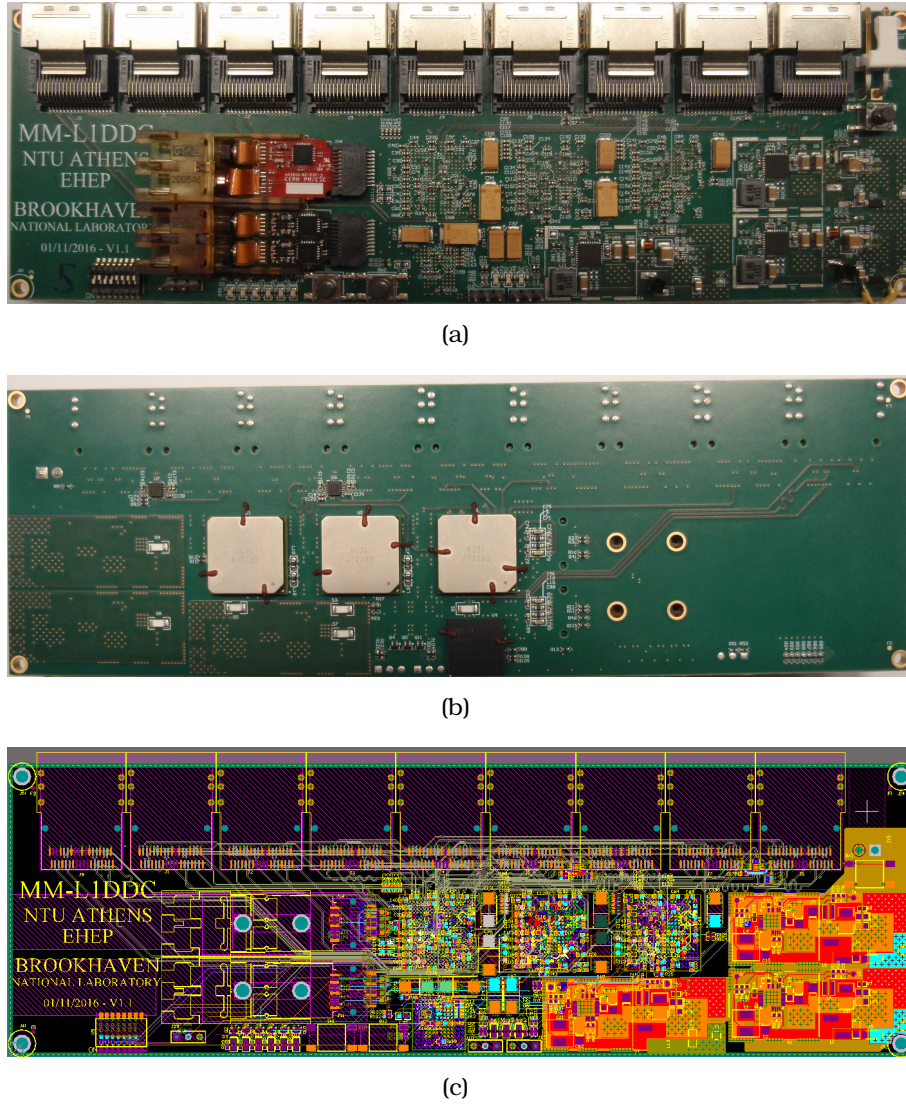


Figure 4.4: MM-L1DDC prototype-2, (a) top layer, (b) bottom layer, (c) layout.

additive phase jitter and less than 15 ps within-device skew. The input of the chip can be CML/LVDS and the output is CML. It needs two different power supplies the V_{cc} at 2.5 V and the V_{cco} at 1.2 V or 1.8 V for the output. Because there is no such voltage level on the L1DDC a voltage divider was used to provide the 1.2 V from the 1.5 V. The reason of selecting two 1:2 fanout chips instead of a 1:4 was to avoid dependencies on the VMMs. For example for a single VMM reset, only two VMMs will be affected and not four. The E-Link configuration implemented in MM-L1DDC prototype-2 is shown in Table 4.1.

Due to insufficient number of 320 Mb/s E-Links caused by the high input rate imposed by the 1 MHz readout, the pinout of the miniSAS is different for the various MMFE8s. All MMFE8s utilize nine differential pairs except the sixth MMFE8 (counting from the beam line) that has only eight pairs. Figure 4.5(a) illustrates the miniSAS pinout with the nine pairs, Figure 4.5(b) the eight pairs and Figure 4.5(c) the pinout for

Table 4.1: E-Link configuration for the prototype-2 (Rev2b) MM-L1DDC boards.

MM-L1DDC (Rev2b)

	GBTX1				GBTX2				GBTX3		
	DIO	DIN	DCLK		DIO	DIN	DCLK		DIO	DIN	DCLK
BANK0	0	SCA FE0 or FE1	SCA FE0 or FE1			L1DATA2 FE1 or FE2				L1DATA3 FE7 or FE8	
	1	SCA FE2 or FE3	SCA FE2 or FE3								
	2	SCA FE4 or FE5	SCA FE4 or FE5								
	3	SCA FE6 or FE7	SCA FE6 or FE7								
	4	SCA FE8 or FE9	SCA FE8 or FE9			L1DATA3 FE1 or FE2				L1DATA4 FE7 or FE8	
	5	SCA FE10 or FE11	SCA FE10 or FE11								
	6	SCA FE12 or FE13	SCA FE12 or FE13								
	7	SCA FE14 or FE15	SCA FE14 or FE15								
BANK1	8	SCA ADDC	SCA ADDC			L1DATA4 FE1 or FE2				L1DATA2 FE9 or FE10	
	9	BCR ADDC	L1DATA3 FE13 or 14								
	10	BCR ADDC	L1DATA3 FE13 or 14								
	11		L1DATA2 FE15 or 16								
	12		L1DATA3 FE15 or 16			L1DATA2 FE1 or FE2				L1DATA3 FE9 or FE10	
	13		L1DATA4 FE15 or 16								
	14										
	15										
BANK2	16	TTC FE1 or FE2	L1DATA1 FE0 or FE1			L1DATA3 FE3 or FE4				L1DATA4 FE9 or FE10	
	17										
	18										
	19										
	20	TTC FE3 or FE4	L1DATA1 FE2 or FE3			L1DATA4 FE3 or FE4				L1DATA2 FE11 or FE12	
	21										
	22										
	23										
BANK3	24	TTC FE5 or FE6	L1DATA1 FE4 or FE5			L1DATA2 FE5 or FE6				L1DATA3 FE11 or FE12	
	25										
	26										
	27										
	28	TTC FE7 or FE8	L1DATA1 FE6 or FE7			L1DATA3 FE5 or FE6				L1DATA1 FE13 or FE14	
	29										
	30										
	31										
BANK4	32	TTC FE9,11 or FE10,12	L1DATA1 FE8 or FE9			L1DATA4 FE5 or FE6				L1DATA2 FE13 or FE14	
	33										
	34										
	35										
	36	TTC FE13,15 or FE14,16	L1DATA1 FE10 or FE11			L1DATA2 FE7 or FE8				L1DATA1 FE15 or FE16	
	37										
	38										
	39										

the ADDC boards.

4.2 Prototype-2 testing

A design error was identified on the MM-L1DDC. The reference clock selection pin (REFCLKSELECT) was by mistake tied to power instead of ground for the first GBTX but was fixed with a board modification. Tests on power distribution and noise measurements were performed. The maximum power consumption of the board was measured at 9 W. Voltage levels were at the nominal values and the noise measured at the output of the FEASTs was ~ 12 mV p-p. Complementary tests were performed on the MM-L1DDC prototype-2 board with both FELIX and evaluation boards running the GBT-FPGA firmware. The following were achieved:

- E-Links were tested with no errors at 80, 160 and 320 Mb/s.
- GBTX internal and external loopback tests on the fiber side showed no errors.
- The VTRX I²C communication was successfully tested. A read/write operation to the seven VTRX registers was performed.
- The GBTX communication with the on-board SCA was successfully established.

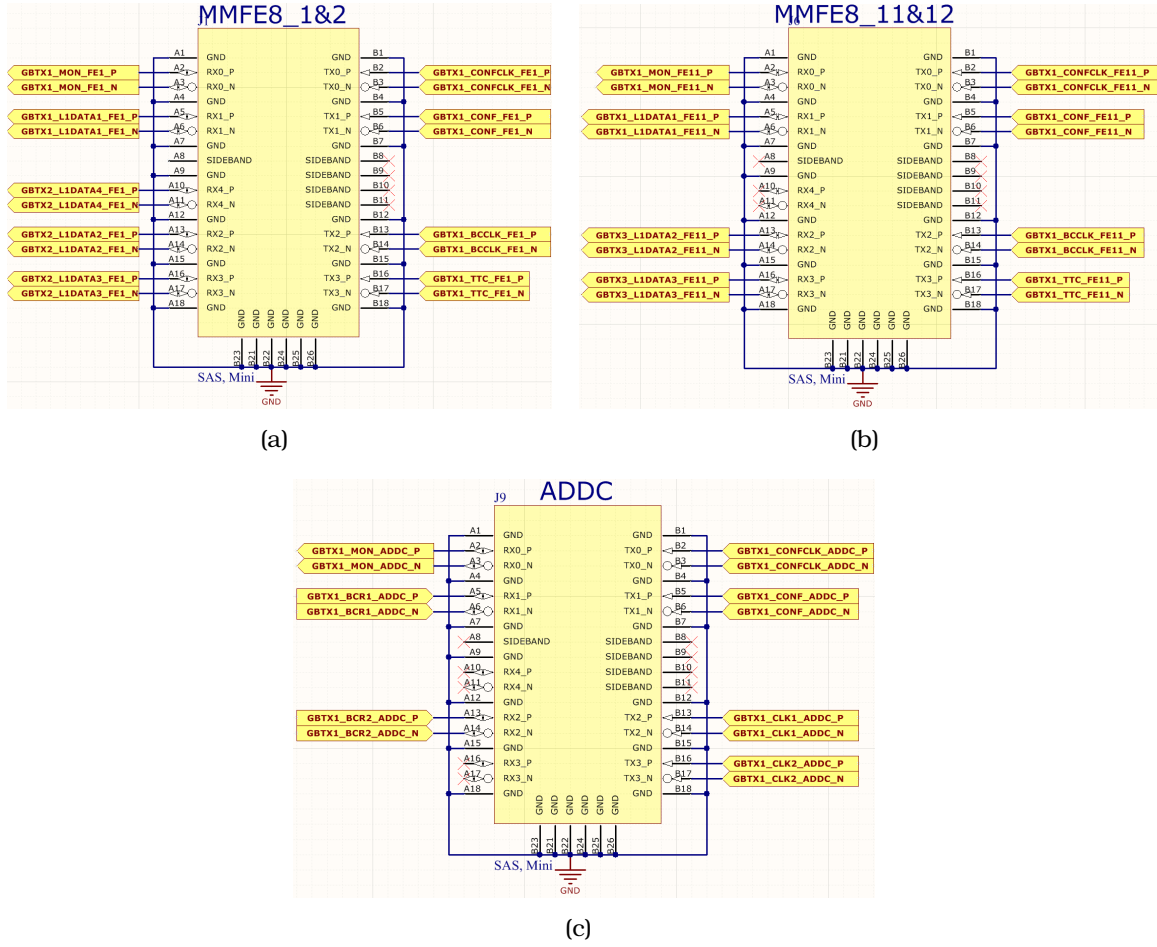


Figure 4.5: Pinout of the miniSAS for the MMFE8 and ADDC boards.

- GBTX configuration via the on-board SCA was verified. In this case data were sent from FELIX to GBTX2 and GBTX3 via the GBTX1 and SCA of the L1DDC.
- GBTX configuration via the IC channel was also tested and verified.
- Interface and level standards with the MMFE8 and ADDC boards were verified.
- Readout data from the FEs at 80 Mb/s.
- GBTX and ART ASIC configuration on the ADDC board was achieved with configuration data sent by the L1DDC.
- Clock distribution to the ADDC board to create the GBT link for the ART transmission.

4.3 Prototype-3 description

For the MM-L1DDC prototype-3 the board dimensions will remain the same with the previous prototype (200 m × 64 m).

Table 4.2: Stackup design for the MM-L1DDC prototype-III board.

Layer	Info			Thickness
TOP	=====			0.333+Plating
	PP	IT-180A	3313	3.618(mil)
L2	=====			1 Oz
	Core	IT-180A	0.13	5.118(mil)
L3	=====			0.5 Oz
	PP	IT-180A	106H+1080	4.740(mil)
L4	=====			1 Oz
	Core	IT-180A	0.13	5.118(mil)
L5	=====			0.5 Oz
	PP	IT-180A	106H+1080	4.775(mil)
L6	=====			1 Oz
	Core	IT-180A	0.13	5.118(mil)
L7	=====			0.5 Oz
	PP	IT-180A	106H+1080	4.744(mil)
L8	=====			1 Oz
	Core	IT-180A	0.13	5.118(mil)
L9	=====			1 Oz
	PP	IT-180A	106H+1080	4.770(mil)
L10	=====			0.5 Oz
	Core	IT-180A	0.13	5.118(mil)
L11	=====			1 Oz
	PP	IT-180A	106H+1080	4.736(mil)
L12	=====			0.5 Oz
	Core	IT-180A	0.13	5.118(mil)
L13	=====			1 Oz
	PP	IT-180A	106H+1080	4.773(mil)
L14	=====			0.5 Oz
	Core	IT-180A	0.13	5.118(mil)
L15	=====			1 Oz
	PP	IT-180A	3313	3.618(mil)
BOT	=====			0.333+Plating

After testing the MM-L1DDC prototype-2 the following corrections/modifications were made to prototype-3:

- For uniformity, the recommended FEAST-MP layout that was described in section 3.5 was also used for the MM-L1DDC.
- The GBTX has a maximum power consumption of 2,237 mW when it is configured to run in full operation (configured as a transceiver and using the phase shifter). In our case the phase shifter will not be used and the power consumption is lowered at the 2,001 mW. In addition, the power consumption of the GBTX when is configured as a transmitter is only 998 mW. Adding the 250 mW of the SCA we have a total of 4,247 mW for the 1.5 V. This means that 2.8 A are required in total and can be provided by a single FEAST. For this reason the additional 1.5 V FEAST was finally removed from the final design. In Table 4.3 the two red boxes indicate the power consumption of the GBTX when it operates as a transceiver (left red box) without the phase shifter and as a transmitter only (right red box).
- It was proven that the clocks inside a GBTX bank are completely independent in frequency with respect to the transmitting pairs but not independent from the number being active. This means that enabling two transmitting pairs in one bank at 320 Mb/s only two clocks at 40, 80, 160 or 320 MHz are available in the specific bank. For this reason the number of transmitting clocks were not enough to satisfy the micromegas scheme and two additional 1:2 fanout chips (Part Number: SY54011RMG) were added.

Table 4.3: Power consumption according to the GBTX mode of operation.

Mode:	TRX	TRX	TRX	TRX	Simple TX	Simple TX	Simple TX	Simple TX	Simple RX	Simple RX
E-Links:										
Data rate (Mb/s):	40	40	160	320	40	160	320	320	40	160
# Data outputs:	40	40	20	10	0	0	0	0	40	20
Clock outputs:	40	40	20	10	5	5	5	5	40	20
Data inputs:	40	40	20	10	40	20	10	0	0	0
EC-Channel:	Enabled	Enabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Enabled	Enabled
Phase-Shifter:										
State:	Enabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Enabled	Enabled
# Channels:	8	0	0	0	0	0	0	0	0	0
Circuit:	Power [mW]	Power [mW]	Power [mW]	Power [mW]	Power [mW]	Power [mW]	Power [mW]	Power [mW]	Power [mW]	Power [mW]
Transmitter:	456	456	456	456	456	456	456	456	0	0
Receiver:	330	330	330	330	0	0	0	0	330	330
Clock Manager:										
E-PLL:	83	83	83	83	42	42	42	42	42	42
XPLL:	100	100	100	100	100	100	100	100	100	100
Total:	183	183	183	183	142	142	142	142	142	142
Phase Shifter:										
PLL:	42	0	0	0	0	0	0	0	0	0
Channel:	128	0	0	0	0	0	0	0	0	0
SLVS-TX:	66	0	0	0	0	0	0	0	0	0
Total:	236	0	0	0	0	0	0	0	0	0
I/O:										
Data SLVS-Tx:	336	336	164	82	0	0	0	0	328	164
CLK SLVS-Tx:	336	336	164	82	41	41	41	41	328	164
Data SLVS-Rx:	27	27	13	7	26	13	7	0	0	0
Total:	699	699	341	171	67	54	48	41	656	328
CORE:										
Standard Cells:	305	305	305	305	305	305	305	305	305	305
Phase-Aligners:	28	28	14	7	28	14	7	0	0	0
Total:	333	333	319	312	333	319	312	305	305	305
Total Power [mW]:	2237	2001	1629	1452	998	971	958	944	1433	1105

- To meet all the requirements, MM-L1DDC PCB thickness should be less than 2.5 mm. Thus, for the outer layers the 101.6 μm (4 mil) width and 101.6 μm (4 mil) gap of the differential pairs were modified to 88.9 μm (3.5 mil) width and 127 μm (5 mil) gap respectively and for the inner layers to 88.9 μm (3.5 mils) width and 116.84 μm (4.6 mil) gap to succeed the appropriate stackup shown in Table 4.2. The board was designed again with sixteen layers. The total thickness of the board is 2.29 mm (90.157 mil). This stackup led to a very good approximation of the single ended and differential impedance of 50 Ω and 100 Ω respectively as shown in Table 4.4. All future prototypes and different versions of the L1DDC built with sixteen layers, utilize this stackup and properties.
- The miniSAS connector for the ADDC board was moved to the center to ensure that the 1 m twinax cable will be long enough for the interconnection of the boards.
- Ferrite beads for the decoupling and filtering of the VTRX, GBTX and SCA were replaced with ceramic inductors. The option of selecting air-core inductors with higher inductance was finally rejected as they can induce more noise to the board.
- All configuration pins were hardwired using resistors and some of them with a selectable option (using two resistors to GND or PWR).

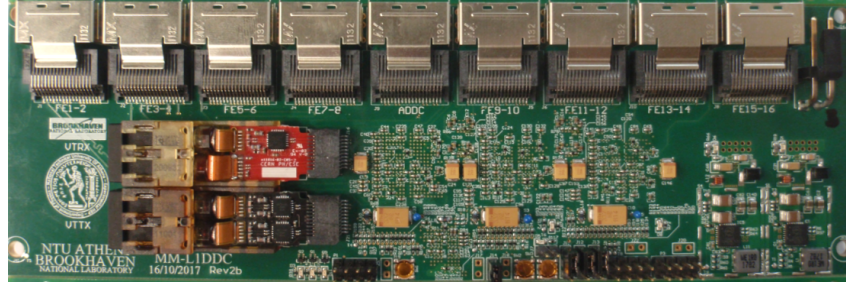
Table 4.4: Single ended and differential impedance for the sixteen layer stackup.

Ctrl	Ref	Imp_type	Cust_req	Imp_req	FP_des	Imp_des	mask	H1	Er1	H2	Ex2
L1	L2	Differential	3.5/5	100+/-10%	3.4/5.1	100.167	Yes	3.62	4.15		
L16	L15	Differential	3.5/6	100+/-10%	3.4/5.2	100.167	Yes	3.62	4.15		
L3	L2/L4	Differential	3.5/4.6	100+/-10%	3.3/4.8	100.707		5.12	4.25	5.34	3.76
L5	L4/L6	Differential	3.5/4.7	100+/-10%	3.3/4.9	100.814		5.12	4.25	5.38	3.76
L7	L6/L8	Differential	3.5/4.8	100+/-10%	3.3/4.10	100.719		5.12	4.25	5.34	3.76
L10	L9/L11	Differential	3.5/4.9	100+/-10%	3.3/4.11	100.799		5.12	4.25	5.37	3.76
L12	L11/L13	Differential	3.5/4.10	100+/-10%	3.3/4.12	100.695		5.12	4.25	5.34	3.76
L14	L13/L15	Differential	3.5/4.11	100+/-10%	3.3/4.13	100.808		5.12	4.25	5.37	3.76
L5	L4/L6	Single-Ended	5	50+/-10%	4.4	49.639		5.12	4.25	5.38	3.76
L7	L6/L8	Single-Ended	5	50+/-10%	4.4	49.552		5.12	4.25	5.34	3.76
L10	L9/L11	Single-Ended	5	50+/-10%	4.4	49.625		5.12	4.25	5.37	3.76
L12	L11/L13	Single-Ended	5	50+/-10%	4.4	49.530		5.12	4.25	5.34	3.76
L14	L13/L15	Single-Ended	5	50+/-10%	4.4	49.633		5.12	4.25	5.37	3.76

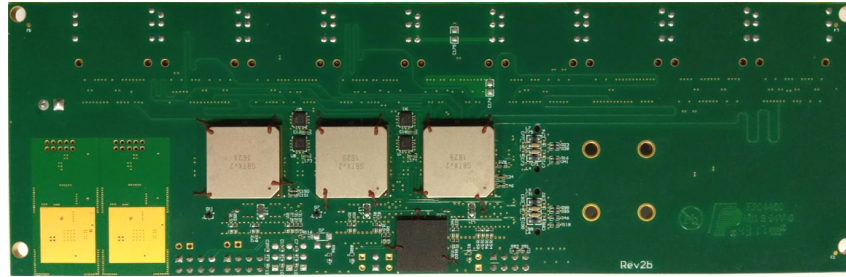
- The eFuse programmability is available by adding external 3.3 V power to a 2.54 mm DIP header and using a I²C dongle.
- The reset of the GBTX is selectable by an RC network (connected to VDD) to provide a time delay, a push-button or the PGOOD signal of the FEAST via DIP headers.
- The wrong polarity on the Rx of the VTRX that was identified in prototype-2, was corrected to the new version.
- Lengths for all the TX (at 103.632 mm) and all RX differential pairs (at 120.396 mm) were equalized.
- An extra clock for the Bunch Crossing Reset signal (BCR) was added to the miniSAS for the ADDC connection as was requested. The new Bank configuration for the GBTX1 of prototype-3 is shown in Figure 4.7(a).
- Moreover the unused differential pairs and single ended signals of the miniSAS connectors were tied to ground according to the ATLAS grounding policy that was described in Section 1.4.5.
- The temperature sensors used in prototype-2 were replaced. New product: Amphenol Advanced Sensors with Part No: DC95F502WN which will be common for all NSW boards.
- The power connector was replaced with the Molex Part No: 1718141002 which will be the same for FE and ADDC boards.

The top, bottom side and layout of MM-L1DDC prototype-3 are shown in Figures 4.6(a), 4.6(b) and 4.6(c) respectively. On the top side of the board the following components are visible: on the left the VTRX and VTTX optical transceiver/transmitter, on the top the nine miniSAS connectors, on the top right the power connector, on the

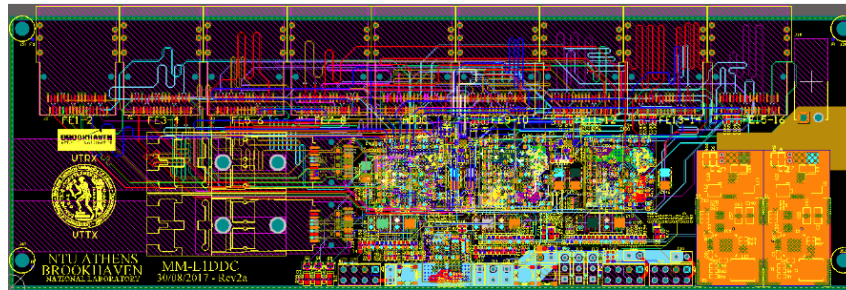
right the 2 FEAST DC-DC converters without the shields, center the decoupling capacitors along with the tantalum ones and center bottom the push-button switches for the reset and DIP headers for efusing and configuration. On the bottom side: on the left the FEAST openings for the heat transfer to the cooling channel, center the three GBTXs and bottom the SCA. The four fanout chips are also visible in between the GBTX ASICs. Five MM-L1DDC prototype-3 boards were submitted for fabrication in September 2017.



(a)



(b)



(c)

Figure 4.6: The top side (a), bottom side (b) and layout (c) of L1DDC Prototype-3.

4.4 Prototype-3 testing

The five boards were tested extensively using the micro-DAQ setup (described in section 6.2.1) and no errors were identified at that time. An oscilloscope was used to evaluate the link with eye diagrams and a phase noise analyser was used to measure the jitter. Since the FEAST layout, filtering/decoupling circuitry and bypassing capacitors are identical with sTGC-L1DDC the jitter performance presented in Section 3.4 was

similar. For the 160 MHz clock the jitter varies from 4.5 ps to 4.8 ps and for the 40 MHz clock from 6.0 ps to 6.7 ps and from 4.9 ps to 5.35 ps for the GBTX direct and fanout output signals respectively. The boards were tested also with FELIX and MMFE8 boards where a swapped polarity on one BC clock was identified. This caused errors on the reception of the TTC data on the MMFE8. The micro-DAQ has not the ability to check the phase of the BC clock making the identification of the problem impossible. Configuration of all ASICs on the FE boards was also achieved using FELIX. The L1DDC was tested also with the whole micromegas trigger chain. Trigger processor was able to align correctly the data coming from the ADDC boards with the BC 40 MHz clock provided by the L1DDC.

4.5 Pre-production description

After extensively testing the MM-L1DDC prototype-3 the pre-production phase of the 50 boards was launched. Some minor modifications had to be performed on the new version:

GBTX1			
	DIO	DIN	DCLK
BANK0	0 SCA FE1	SCA FE1	SCA CLK
	1 SCA FE3	SCA FE3	SCA CLK
	2 SCA FE5	SCA FE5	SCA CLK
	3 SCA FE7	SCA FE7	SCA CLK
	4 SCA FE9	SCA FE9	SCA CLK
	5 SCA FE11	SCA FE11	SCA CLK
	6 SCA FE13	SCA FE13	SCA CLK
	7 SCA FE15	SCA FE15	SCA CLK
BANK1	8 SCA ADDC	SCA ADDC	SCA CLK ADDC
	9 BCR ADDC	L1DATA3 FE13	GBTX1 CLK ADDC
	10 BCR ADDC	L1DATA4 FE13	GBTX2 CLK ADDC
	11	L1DATA2 FE15	GBTX2 REF CLK
	12	L1DATA3 FE15	GBTX3 REF CLK
	13	L1DATA4 FE15	
	14		
	15		
BANK2	16 TTC FE1	L1DATA1 FE1	BCCLK FE1
	17		BCCLK FE3
	18		
	19		
	20 TTC FE3	L1DATA1 FE3	BCCLK FE5
	21		
	22		BCCLK FE7
	23		
BANK3	24 TTC FE5	L1DATA1 FE5	BCCLK FE9
	25		
	26		
	27		
	28 TTC FE7	L1DATA1 FE7	BCCLK FE11
	29		
	30		
	31		
BANK4	32 TTC FE9/11	L1DATA1 FE9	BCCLK FE13
	33		
	34		
	35		
	36 TTC FE13/15	L1DATA1 FE11	BCCLK FE15
	37		
	38		
	39		

GBTX1			
	DIO	DIN	DCLK
BANK0	0 SCA FE1	SCA FE1	SCA CLK
	1 SCA FE3	SCA FE3	SCA CLK
	2 SCA FE5	SCA FE5	SCA CLK
	3 SCA FE7	SCA FE7	SCA CLK
	4 SCA FE9	SCA FE9	SCA CLK
	5 SCA FE11	SCA FE11	SCA CLK
	6 SCA FE13	SCA FE13	SCA CLK
	7 SCA FE15	SCA FE15	SCA CLK
BANK1	8 SCA ADDC	SCA ADDC	SCA CLK ADDC
	9 BCR ADDC	L1DATA3 FE13	GBTX1 CLK ADDC
	10 BCR ADDC	L1DATA4 FE13	GBTX2 CLK ADDC
	11	L1DATA2 FE15	GBTX2 REF CLK
	12	L1DATA3 FE15	GBTX3 REF CLK
	13	L1DATA4 FE15	BCR CLK ADDC
	14		
	15		
BANK2	16 TTC FE1	L1DATA1 FE1	BCCLK FE1
	17		
	18		
	19		
	20 TTC FE3	L1DATA1 FE3	BCCLK FE3
	21		
	22		
	23		
BANK3	24 TTC FE5	L1DATA1 FE5	BCCLK FE5
	25		
	26		
	27		
	28 TTC FE7	L1DATA1 FE7	BCCLK FE7
	29		
	30		
	31		
BANK4	32 TTC FE9/11	L1DATA1 FE9	BCCLK FE9/11
	33		
	34		
	35		
	36 TTC FE13/15	L1DATA1 FE11	BCCLK FE13/15
	37		
	38		
	39		

GBTX1			
	DIO	DIN	DCLK
BANK0	0 SCA FE1	SCA FE1	SCA CLK
	1 SCA FE3	SCA FE3	SCA CLK
	2 SCA FE5	SCA FE5	SCA CLK
	3 SCA FE7	SCA FE7	SCA CLK
	4 SCA FE9	SCA FE9	SCA CLK
	5 SCA FE11	SCA FE11	SCA CLK
	6 SCA FE13	SCA FE13	SCA CLK
	7 SCA FE15	SCA FE15	SCA CLK
BANK1	8 SCA ADDC	SCA ADDC	SCA CLK ADDC
	9 BCR ADDC	L1DATA3 FE13	GBTX1 CLK ADDC
	10 BCR ADDC	L1DATA4 FE13	GBTX2 CLK ADDC
	11	L1DATA2 FE15	GBTX2 REF CLK
	12	L1DATA3 FE15	GBTX3 REF CLK
	13	L1DATA4 FE15	BCR CLK ADDC
	14	L1DATA2 FE15	
	15		
BANK2	16 TTC FE1	L1DATA1 FE1	BCCLK FE1
	17		
	18		
	19		
	20 TTC FE3	L1DATA1 FE3	BCCLK FE3
	21		
	22		
	23		
BANK3	24 TTC FE5	L1DATA1 FE5	BCCLK FE5
	25		
	26		
	27		
	28 TTC FE7	L1DATA1 FE7	BCCLK FE7
	29		
	30		
	31		
BANK4	32 TTC FE9/11	L1DATA1 FE9	BCCLK FE9/11
	33		
	34		
	35		
	36 TTC FE13/15	L1DATA1 FE11	BCCLK FE13/15
	37		
	38		
	39		

(a)

(b)

(c)

Figure 4.7: GBTX1 E-Link configuration (a) Prototype-2, (b) Prototype-3, (c) pre-production and production boards.

- Tantalum capacitors were replaced by ceramic ones with the same value.
- All 2.54 mm DIP headers were replaced by 2 mm DIP headers.
- Ceramic inductors were also replaced by shielded ones with higher inductance (1 μ H) and extra filtering was added to minimize the noise at the input of the GBTX.
- The power connector replaced by the Molex Nano-Fit which is common with all on detector electronics (except rim electronics).
- The E-Link signals in Bank 2 were rearranged to simplify the routing and the new configuration is shown in Figure 4.7(c). The GBTX2 and GBTX3 configuration remained unchanged compared to prototype-2 Rev2b board and is presented in Table 4.1.
- The FEAST layout implemented in sTGC-L1DDC prototype-4, as described in Section 3.5, was also used for uniformity.

In total 50 boards were fabricated and assembled in September 2018.

4.6 Pre-production testing

The 50 boards were tested using the micro-DAQ for signal transmission integrity. All E-Links were tested at the nominal frequencies (80 Mb/s and 320 Mb/s) and no errors were observed. One board, after long time of operation, appear to have unstable connection and was losing the synchronization with the back-end. This board was marked as a faulty one and thus the yield was calculated to be 98%. All GBTXs were eFused with the training mode for the incoming data by using the I²C dongle. During the tests it was observed that GBTX, after powering on the board, failed to find automatically the proper phase for the 320 Mb/s incoming data. After resetting the DLLs on the unaligned E-Links the GBTX was able to find the correct phase and receive the data correctly. Since the latency of the cables and traces on the boards will be fixed in the final setup, the manual mode will be used on the final boards.

Phase noise measurements were performed for the output clocks and eye diagrams for the data lines. The eye of the direct GBTX TTC output is shown in Figure 4.8(a). The eye is wide open with a height of 412.1 mV and width of 2.991 ns. A typical eye for the TTC outputs after the fanout chips is shown in Figure 4.8(b). The transitions in this case are not so sharp but the eye is still open with a height of 420.2 mV and width of 2.906 ns.

The jitter of the direct clock outputs was measured to be between 6.15 ps and 7.33 ps. The clock outputs driven by the fanout chips appear to have a good performance with a jitter of 4.8 ps up to 5.5 ps. A typical jitter measurement of the fanout clocks for Front-end eight is illustrated in Figure 4.9. The Random Jitter value of 4.88 ps is calculated by the integrated bandwidth between 1 K and 20 MHz.

FELIX and OPCUA server were used to test the communication with the on board SCA. ADC values were read out successfully confirming the correct functionality of the

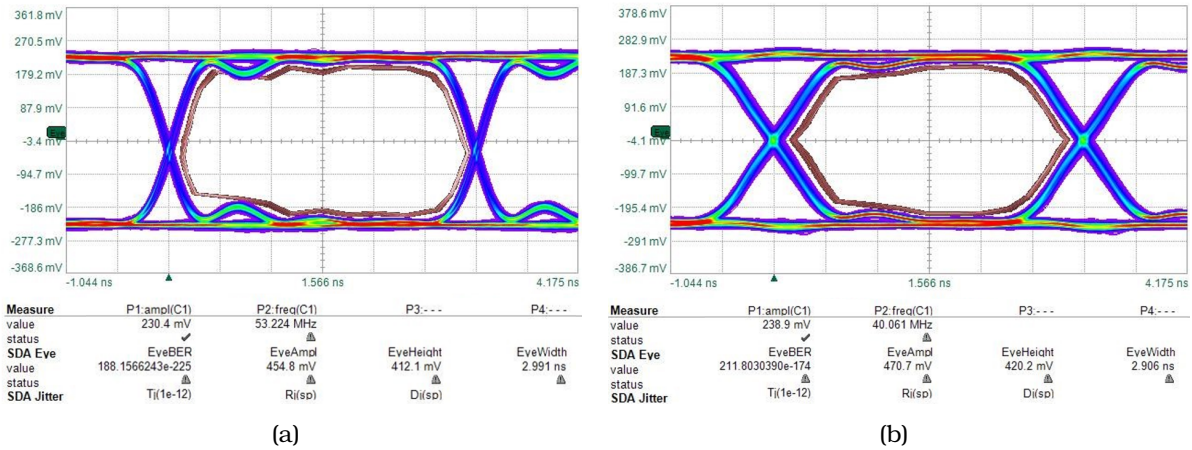


Figure 4.8: Eye diagrams for the 320 Mb/s E-Links, (a) direct GBTX output, (b) after the fanout buffer.

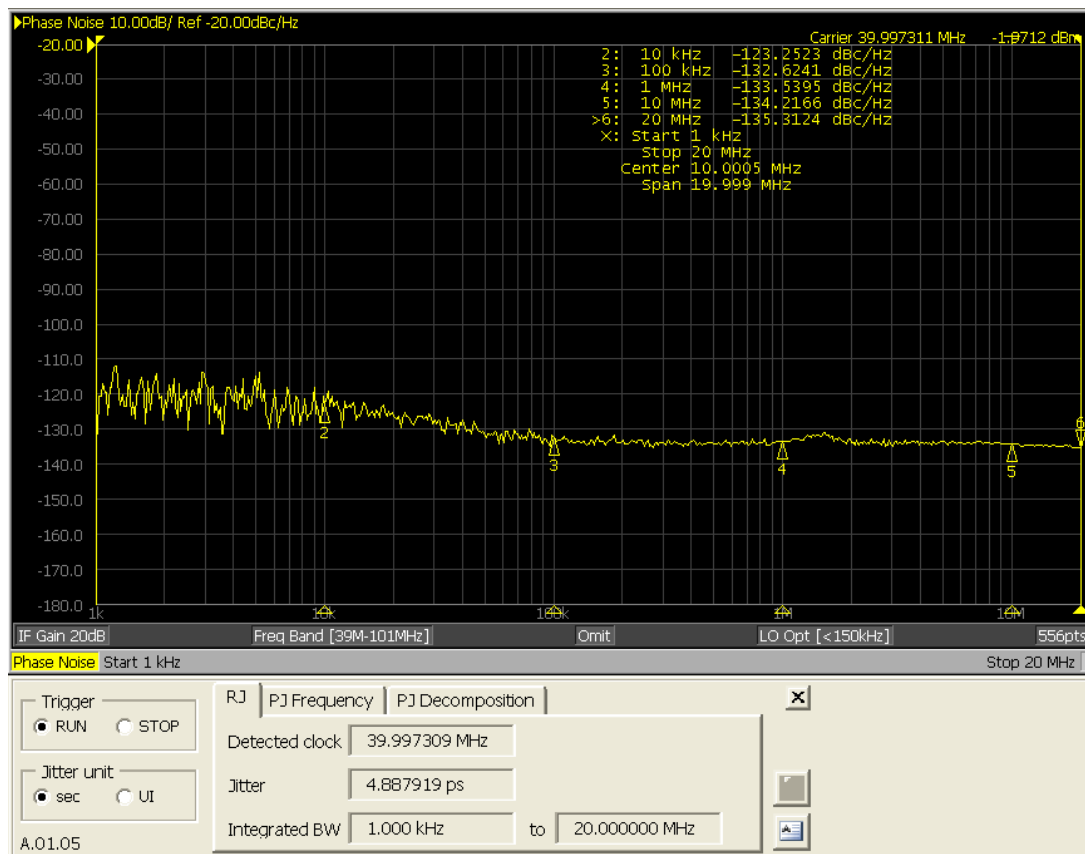


Figure 4.9: Random jitter of the fanout clocks.

board. Thermal analysis was also performed on the board. The maximum temperature is observed on the VTTX module and especially by the GBLD ASIC as shown in Figure 4.10(a). This temperature can rise up to 62.7°C (Figure 4.10(b)) without any cooling. This value was measured after operating the L1DDC board in full functionality

for two hours. It was obvious that this high temperature may affect the performance and the life expectancy of the ASIC and was decided to be cooled down. The 1.5 V and 2.5 V FEASTs can rise up to 57.5°C (Figure 4.10(c)) and 53.7°C (Figure 4.10(e)) respectively. By placing a small fan at the back of the board the temperature decreases significantly at 40.7°C (Figure 4.10(d)) for the 1.5 V and 37.4°C (Figure 4.10(f)) for the 2.5 V.

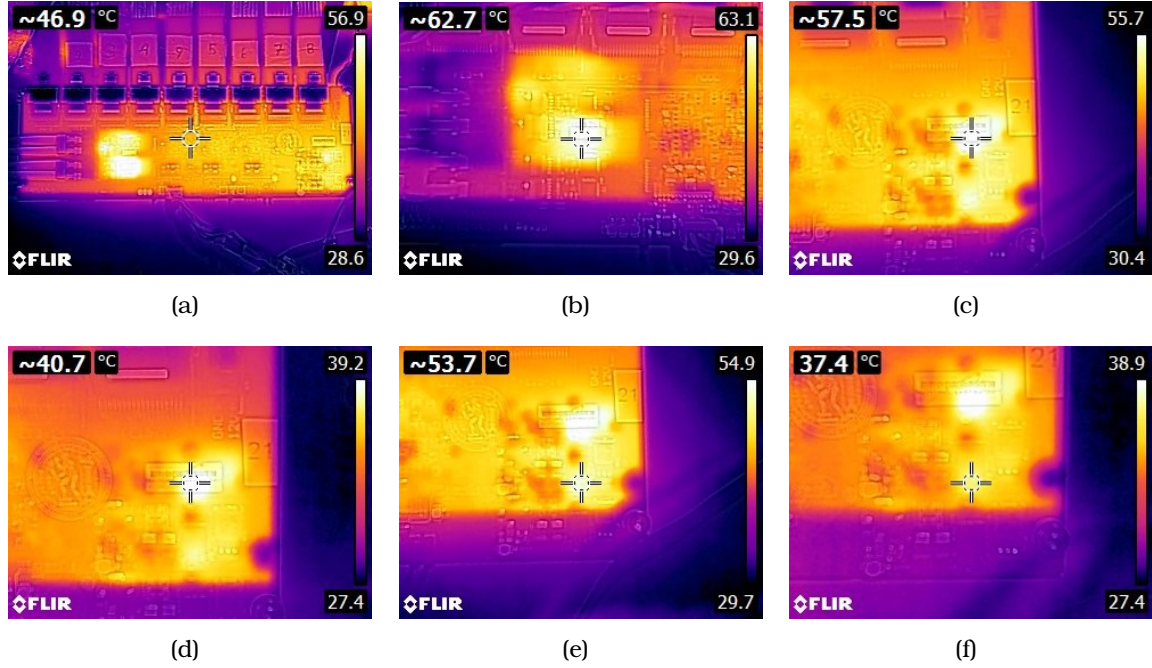


Figure 4.10: Thermal analysis of the MM-L1DDC board after two hours of continuous operation in full functionality. (a) top side, (b) VTTX, (c) 1.5 V FEAST without cooling, (d) 1.5 V FEAST with fan cooling, (e) 2.5 V FEAST without cooling and (f) 2.5 V FEAST with fan cooling.

Finally eight boards were randomly selected for the readout of eight MMFE8s. For that test FELIX BNL-712 was used to receive the data from all three optical links of each L1DDC board. The clock and TTC data were provided to FELIX by the TTCvi module. ROC and VMM configuration was succeeded by using the OPC Unified Architecture (OPCUA) server and simultaneous readout of the eight MMFE8s was achieved.

4.7 Production boards

The files for the 522 production boards were submitted in January 2019, where some minor modifications were implemented. According to the new LV distribution architecture that is described in detail in section A.2 the fuses for the over current protection should be removed and placed on the Low Voltage Distributor Board (LVDB). Moreover the ferrites for the noise suppression of the VTRX and VTTX modules were replaced with shielded inductors, by using different footprints. To provide sufficient cooling to the VTTX and VTRX through a thick metal plate from the bottom side of the boards a

cutout of $5.51\text{ mm} \times 13.99\text{ mm}$ was added close to VTTX as shown in Figure 4.11. Finally the DIP headers for the configuration selection of the two GBTXs were completely removed and the signals were tied to power through resistors. The Bank configuration for all GBTXs remained unchanged compared to the pre-production boards.



Figure 4.11: *Cutout implemented in production boards for the cooling of the VTTX and VTRX.*

RIM L1DDC board

The roadmap of the RIM-L1DDC comprises only two prototypes as presented in Figure 5.1. Three boards of the first prototype were designed and fabricated in January 2017. Four boards of the second prototype were produced in September 2018 and due to the limited available time for the tests until the Final Design Review (October 2018) some tests were pending. In this section the architecture and the functionality of the RIM-L1DDC board are presented. Especially there is a detailed description of the design choices that were made, rules that were followed and the components/materials that were used. Finally, the results of the tests that were performed are also mentioned.

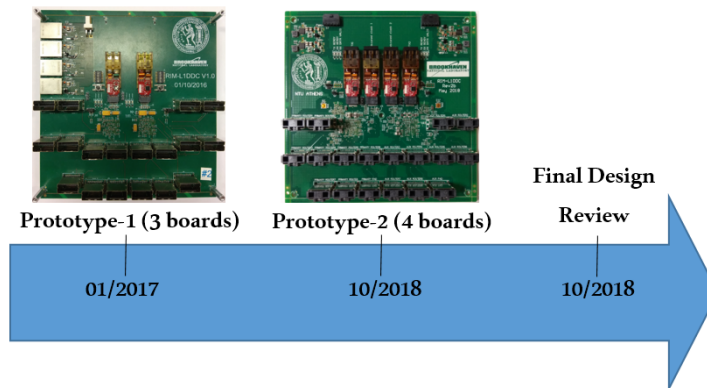


Figure 5.1: Roadmap of the RIM-L1DDC board.

5.1 Prototype-1 description

The RIM-L1DDC interfaces with on detector trigger electronics of the sTGC detectors (one PAD and eight router boards) on one side and with FELIX on the other side. In total 32 RIM-L1DDC will be used for the upgrade of NSW. One GBTX was enough to handle the bandwidth and the number of PAD and trigger boards. For the optical communication the VTRX optical transceiver was used. Moreover, for the power distribution the CERN's FEAST radiation tolerant DC-DC converter was selected. At that

time it was decided to provide the reference clock for the FPGA transceivers by the eight programmable in phase clocks of the GBTX. A 1:2 fanout was also used to provide the extra clock to the PAD and trigger boards (in total nine boards). This fanout was tested and survived under radiation.

The purpose of the RIM-L1DDC is to:

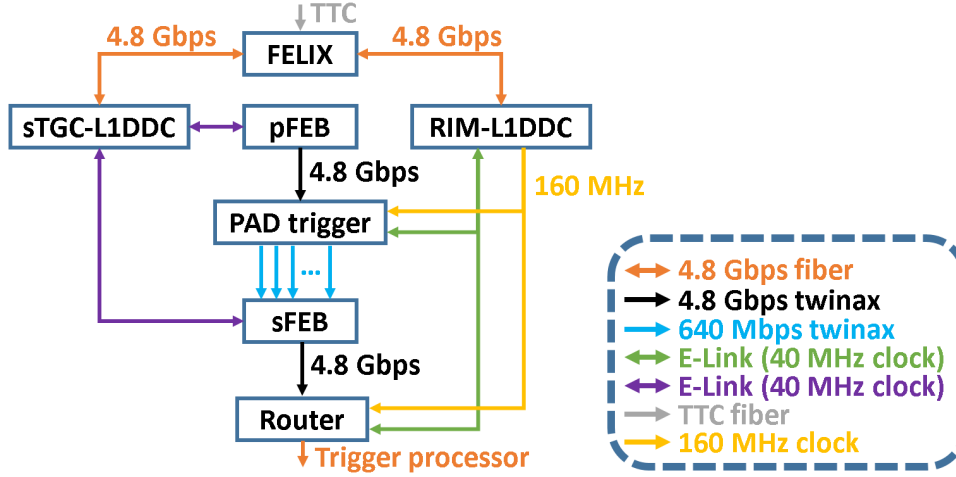
- Distribute a low jitter 160 MHz reference clock to the PAD and router boards. This clock is used by the Xilinx's 7 family FPGA transceivers to sample the 4.8 Gb/s TDS trigger data.
- Provide the 80 Mb/s configuration data and receive environmental variables (current, voltage levels and temperatures) to/from the SCA of the PAD trigger and Router boards.
- Receive Level-1 readout data from the FPGAs (eg which Pad hits have been received or which trigger has been sent).
- Provide the TTC data, auxiliary data at 80 Mb/s and a synchronous 40 MHz BC clock to the FPGAs.

The full sTGC trigger chain is shown in Figure 5.2. Both L1DDC boards (sTGC and RIM) are connected with FELIX. The sTGC-L1DDC will provide the 40 MHz clock to the ROC of the FEs. The ROC distributes the 40 MHz reference clock (traversing the ROC PLL) to the TDS ASICs. The latter uses the clock to generate the high speed serial links at 4.8 Gb/s and the data are transmitted to the PAD trigger board through twinax cables. The PAD board receives one link at 4.8 Gb/s from each pFEB board. In total 24 pFEBs are connected to one PAD trigger board (every four are merged into one miniSAS connector with the use of four-SATA to one miniSAS cables). PAD trigger transmits in total seven signals to the sFEB: a clock at 320 MHz, an enable signal, the D0 for the twelve bits of the BCID and four lines for the 13 bits of the band ϕ -ID. Each PAD trigger board interfaces with 24 sFEB boards. Finally each sFEB transmits three high speed serial links (one for each TDS ASIC) at 4.8 Gbps to the Router board. Three sFEB are connected to one router board so in total eight router boards are needed for each sector.

Link stability for the data transmission is related to the jitter of the reference clock being used. Both Router and PAD trigger boards integrate a Xilinx's 7 family FPGA (Kintex-7 for PAD and Artix-7 for Router). To achieve the proper and reliable data transmission, Xilinx provides a phase mask for the reference clocks which varies depending on the frequency of the clock and the PLL being used (CPLL vs QPLL). In Table 5.1 the phase noise for the Channel Phase Locked Loop (CPLL) and Quad Phase Locked Loop (QPLL) with respect to the frequency is presented.

GBTX output clock jitter was measured by the designers using a tester board. The RMS and Peak-to-Peak jitter of the E-Link clocks at different frequencies (40, 80, 160 and 320 MHz) and for the different modes of the GBTX (simplexRx, simplexTx and duplex) are presented in Table 5.2.

The one PAD trigger and eight router boards handle the trigger for a whole sTGC wedge (four planes). This means that in a case of a RIM-L1DDC failure the whole

Figure 5.2: *sTGC trigger chain.*Table 5.1: *Xilinx's phase noise mask for the CPLL and QPLL.*

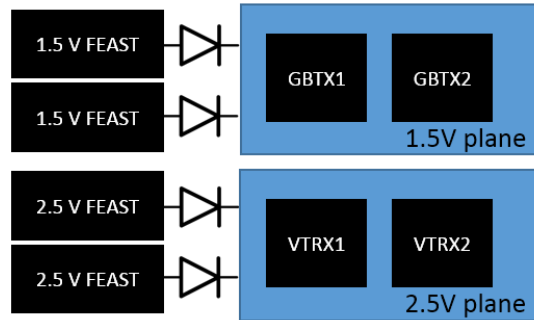
Reference clock frequency (MHz)	Phase Noise at Offset Frequency (dBc/Hz)					
	CPLL			QPLL		
	10 kHz	100 kHz	1 MHz	10 kHz	100 kHz	1 MHz
100.0	-126	-132	-136	-126	-130	-134
125.0	-123	-131	-135	-123	-129	-133
156.25	-121	-129	-133	-122	-127	-132
250.0	-119	-126	-132	-119	-126	-131
312.5	-116	-124	-131	-115	-124	-130
625.0	-110	-119	-127	-110	-116	-120

wedge is unusable. Thus, it was decided that the RIM-L1DDC should have a level of redundancy. All the components except the power connector and power cable were doubled using the same PCB with the ability to switch to the second circuitry in case of a fiber/GBTX/VTRX failure. The number of miniSAS connectors was doubled and the primary ones are connected to GBTX1 and auxiliary to GBTX2. Common planes for the 1.5 V and 2.5 V were used for the board. Each plane was powered up by two FEAST ASICs with a diode at the output for protection. The block diagram of the power for the board is shown in Figure 5.3.

The placement of the GBTX was chosen to be in the middle of the board in order to minimize the routing length of the signals to the miniSAS connectors. For the FEAST ASIC UM's recommended schematics and layout that are described in detail in section 3.1, were used. This layout ensures low output noise on the power rails but also less radiated noise. The traces of a differential pair were adjusted to have the same length with a deviation of $< 254 \mu\text{m}$ (10 mil). Moreover, the lengths of the two transmitting pairs (data and clock) of each E-Link were equalized to avoid phase differences and ensure the proper reception on the receiving side. Due to the limited number of E-Links available, the communication with the PAD trigger SCA is implemented by the

Table 5.2: GBTX jitter measurements.

GBTX mode	Frequency (MHz)	Jitter RMS (ps)	Jitter P-P (ps)
SimplexRx	40	7.20	60.52
	80	6.76	56.67
	160	5.90	45.56
	320	5.85	47.78
SimplexTx	40	6.02	47.78
	80	5.86	45.00
	160	5.58	49.44
	320	5.65	44.44
Duplex	40	7.25	58.89
	80	6.70	55.00
	160	5.88	47.22
	320	5.73	43.89

**Figure 5.3:** FEAST connectivity for the RIM-L1DDC prototype-1.

dedicated EC channel of the GBTX. The GBTX configuration of RIM-L1DDC prototype-1 is shown in Table 5.4. The red highlighted signals were added on the second prototype. For the miniSAS connectors the unused single ended pins were left floating and the ground/shield pins were grounded (connected on the ground planes of the board). The miniSAS schematic diagram for the router board is shown in Figure 5.4(a) and for the PAD trigger boards in Figure 5.4(b).

The board dimensions are 170 mm \times 170 mm so the board is able to fit inside the RIM crate (approximately 180 mm \times 180 mm). DIP switches were used for the selection of the MODE[3:0], the SLVSINJECT, TXDATAVALID and CONFIGSELECT configuration signals. The reset of the GBTXs is performed from push-button switches. The eFuse programmability was not added on this version of the board. RIM-L1DDC has no direct contact with the ground of the rim box. The only connection with the power is the +12 V and the return current. Three boards of the first prototype of the RIM-L1DDC were fabricated in October 2016. On the top side of the board shown in Figure 5.5(a), the miniSAS (bottom), the power connectors (top left), the FEAST ASICs (top left) and the VTRX optical transceivers (center-top) are illustrated. At the bottom side the two GBTXs and fanout chips (center) are visible as illustrated in Figure 5.5(b). Finally, the

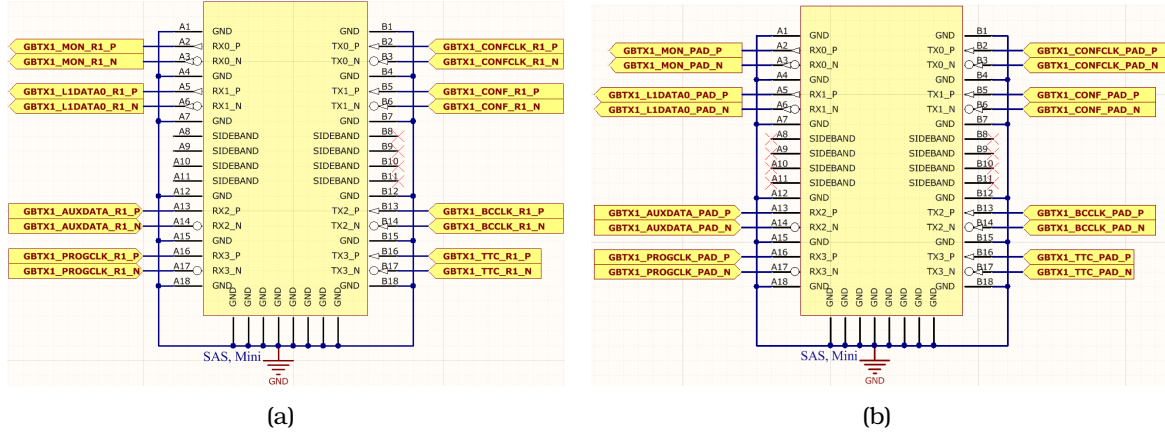


Figure 5.4: MiniSAS pinout of RIM-L1DDC prototype-1 for (a) Router and (b) PAD trigger board.

layout with all the layers enabled is presented in Figure 5.5(c). The board was designed with sixteen layers and uses the same setting with MM-L1DDC prototype-2 board as was described in section 4.1.

5.2 Prototype-1 testing

All three boards were extensively tested. Power and noise measurements, signal integrity tests, eye diagrams and jitter measurements were performed. Generally no significant errors were identified and the boards were fully operational and had the expected behaviour. To verify that the 160 MHz E-Link clock was good enough to feed the FPGA 7-family transceivers a set of Integrated Bit Error Rate Tester (IBERT) tests were performed. Data transmission at 8 Gb/s from a Xilinx's KC705 evaluation board to VC707 via SMA cables and with 160 MHz GBTX E-Link clocks was verified. In all cases Xilinx's IBERT IP core was used to generate 31 bit Pseudo Random Binary Sequence (PRBS) data. This sequence is generated by a 31 grade of the monic polynomial:

$$PRBS\ 31 = x^{31} + x^{28} + 1$$

Different GBTX E-Link clocks at 160 MHz were tested. FELIX was used as the back end for this test. In Figure 5.6(a) a typical result of the Bit Error Ratio for the link transmission using the 160 MHz RIM-L1DDC E-Link clocks is presented. After the transmission of 1.699E+13 bits no errors occurred and the Bit Error Ratio (BER) was 5.88E-14.

Jitter measurements were also performed at the RIM-L1DDC boards. For the measurements the Keysight E5052B Phase Noise Analyzer was used. For the 40 MHz clocks the jitter measured at ~ 8 ps and for the 160 MHz at ~ 4.1 ps as shown in Figure 5.7.

Tests were performed on both optical and E-Link paths at the nominal bandwidth and no errors occurred. For these tests the setup described in Section 2.3 and shown in Figure 2.9 was used. A typical output for the checked data at 80 Mb/s and 320 Mb/s showing the errors counter (red color) is shown in Figure 5.8. During the tests no errors occurred after the transmission of 2.7E+13 bits and the BER was 3.61E-14.

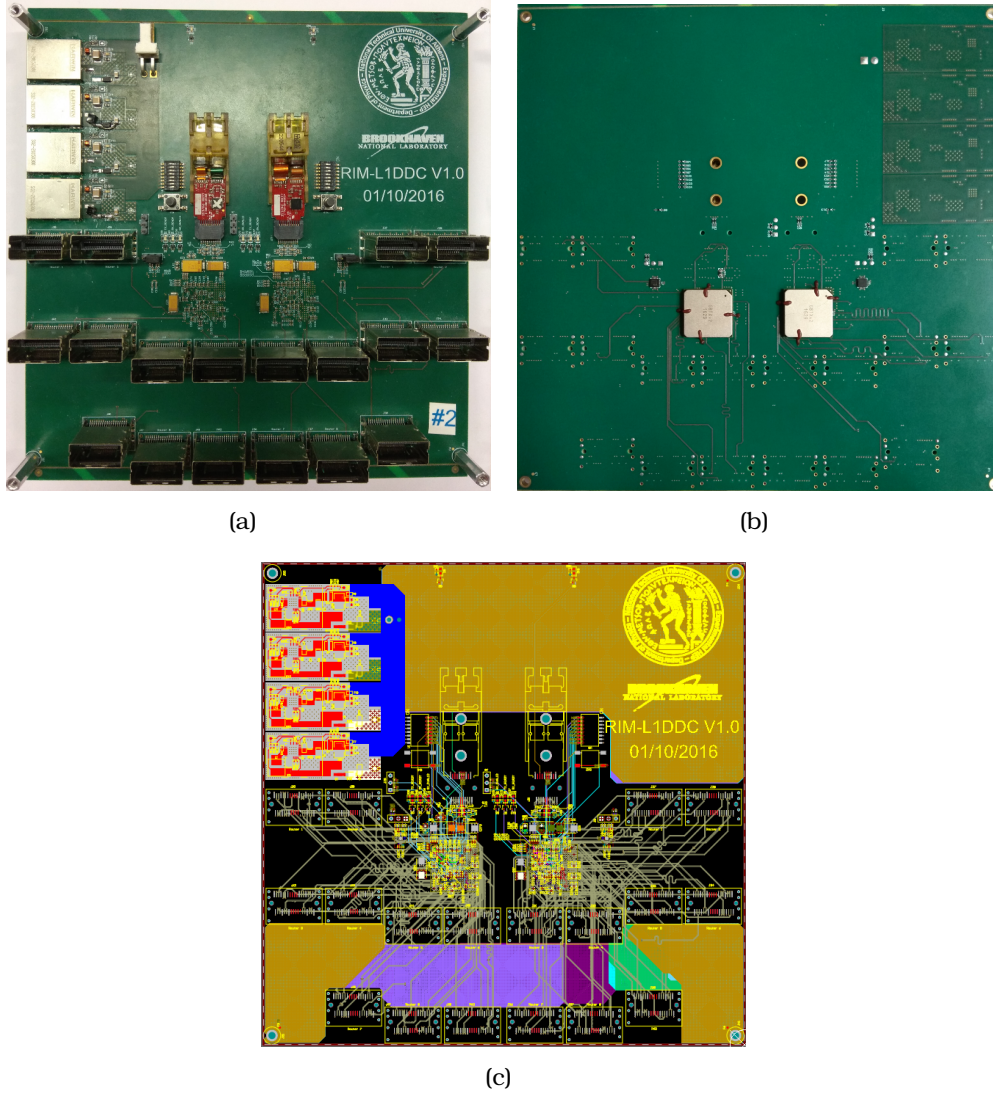


Figure 5.5: RIM-L1DDC Prototype-1. (a) Top side, (b) bottom side and (c) layout.

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DPE Enabled	Inject Error	TX Reset	RX Reset	RX PLL Status	TX PLL
Link Group 0 (4)																		
Link 0	MGT_X1Y0/TX	MGT_X1Y0/RX	8.016 Gbps	1.242E13	0E0	8.051E-14	Reset	Multiple	Multiple	1.67 dB (00111)	0.68 dB (00011)	1018 mV (1100)	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked
Link 1	MGT_X1Y1/TX	MGT_X1Y1/RX	No Link	1.242E13	6.458E12	5.199E-1	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV (1100)	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked
Link 2	MGT_X1Y2/TX	MGT_X1Y2/RX	No Link	1.242E13	6.204E12	5.003E-1	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV (1100)	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked
Link 3	MGT_X1Y3/TX	MGT_X1Y3/RX	No Link	1.242E13	7.453E12	6E-1	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV (1100)	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked

(a)

Figure 5.6: BER and errors for the 8 Gb/s data lines.

Noise measurements at the 1.5 V and 2.5 V output of the FEAST were also performed. The results are similar with the ones presented in Section 3.2 for the sTGC-L1DDC prototype-2.

Furthermore it was crucial to identify the jitter threshold that makes the high speed links unstable. White noise was added gradually to the 160 MHz input reference clock of the Router and high speed links were monitored for errors. Due to the sFEB unavail-

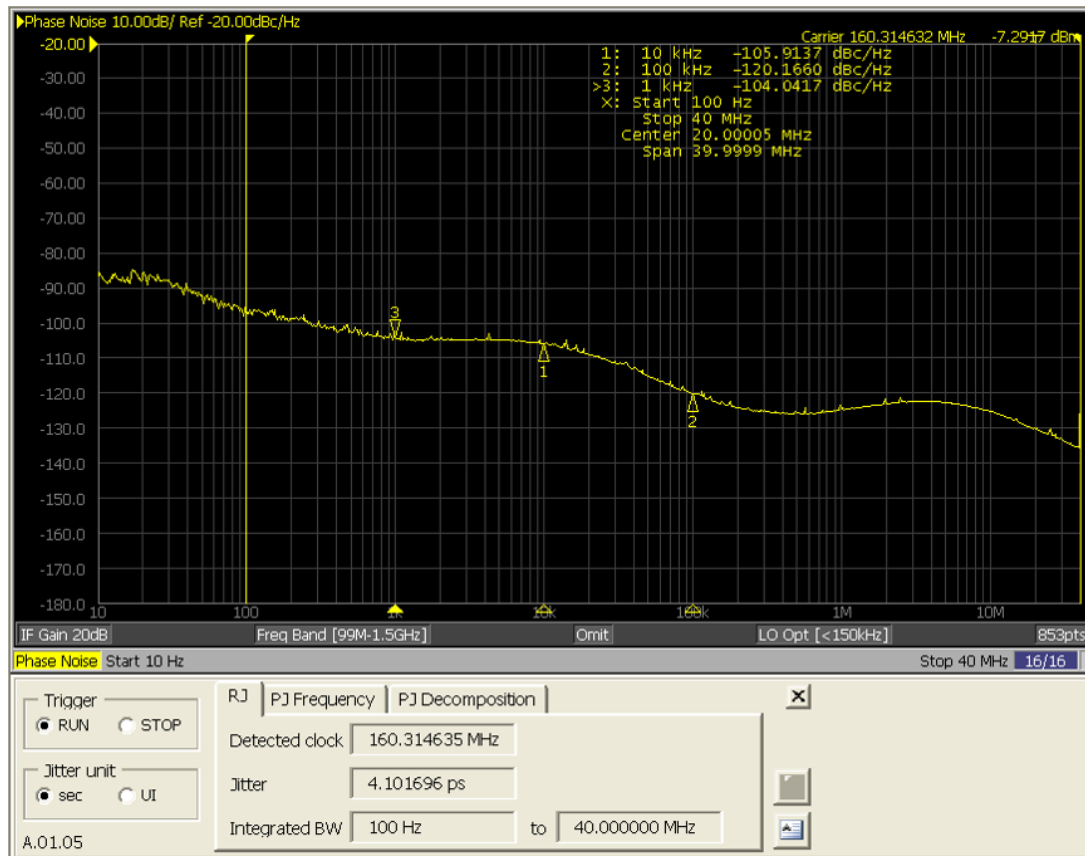


Figure 5.7: Jitter measurement on E-Link clocks at 160 MHz.

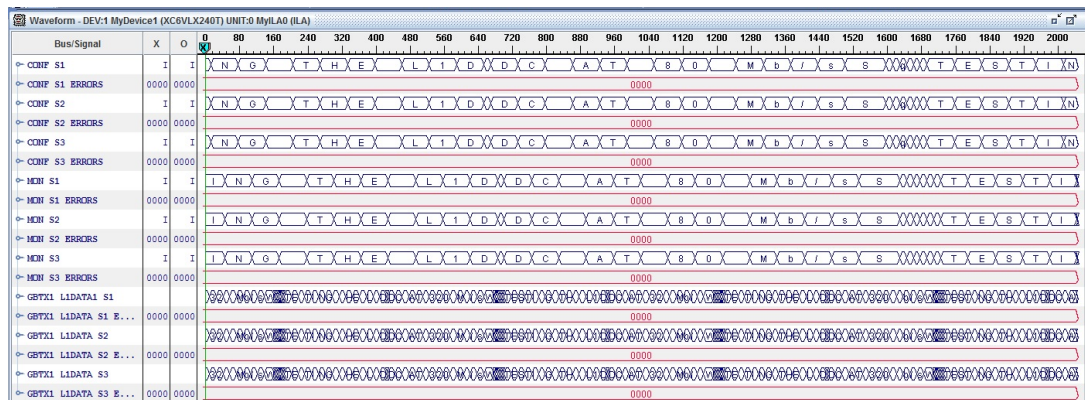


Figure 5.8: Example of E-Link testing at 80 and 320 Mb/s on the RIM-L1DDC board.

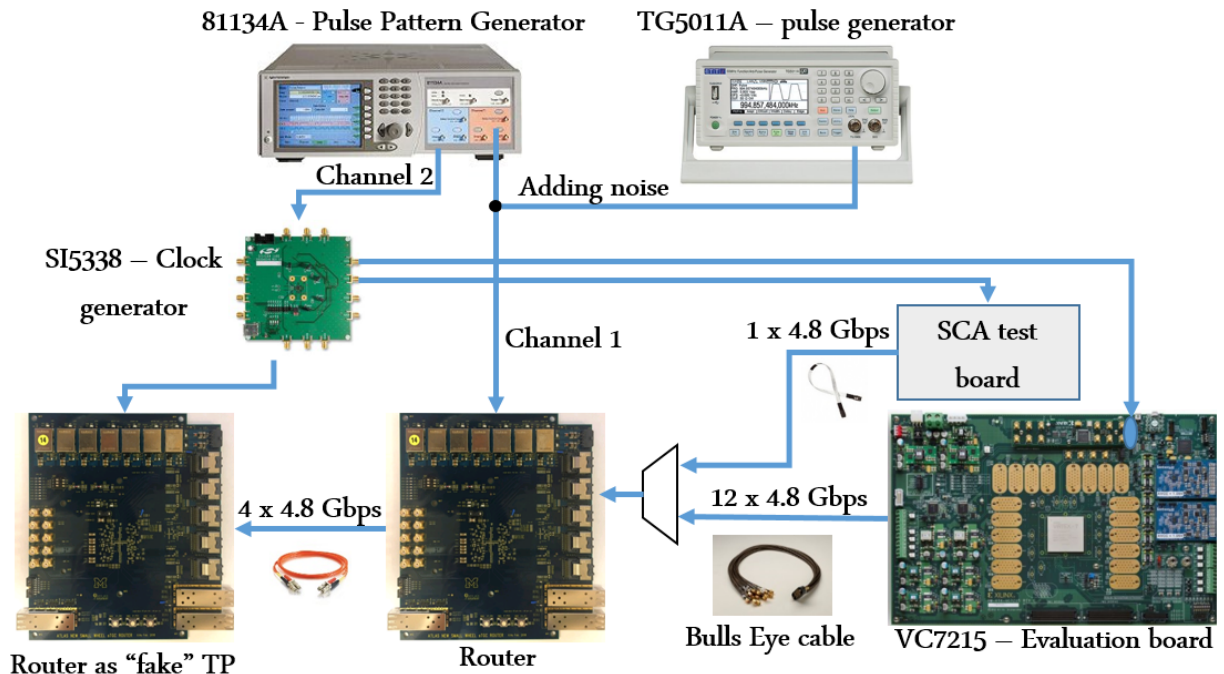
ability the SCA tester board was used. This board has a VMM, a SCA, a ROC and a TDS ASIC and emulates the FE boards. VMM data were transmitted by the TDS to the router, using a 3 m twinax cable and then to a second router (acting as a trigger processor) for evaluation. Since the SCA test board has one TDS, only one link at 4.8 Gb/s was monitored during the test. The 81134A Pulse Pattern Generator by Keysight was used as the clock source. This instrument features two output channels, with the one driven to the Router board and the second one to the SI5338 clock generator and dis-

Table 5.3: *Jitter for different values of white noise.*

Noise amplitude (mVp-p)	57	80	100	120	150	170	200
Phase noise jitter (ps)	7.55	7.75	8.21	8.67	9.52	10.08	11.06

tributed to the "fake" Trigger Processor and SCA test board. The SI5338 provides a very low output jitter for the 160 MHz clock, which was measured to be 730.47 fs. The second channel was connected also with the TG5011A pulse generator by Aim & Thurlby Thandar Instruments to add the Gaussian white noise. The whole setup is presented in Figure 5.9. Noise amplitude from 57 mVp-p up to 200 mVp-p was added to the 160 MHz clock of the Router and the resulting jitter is presented in Table 5.3. It proved that the link became unstable by adding noise more than 150 mV which corresponds to 9.52 ps. To validate the stability of more high speed links the SCA test board was replaced by the VC7215 evaluation board from Xilinx. The latter features twenty Samtec BullsEye connectors each one utilizing four GTH transceivers of 16.3 Gb/s. Adapter boards were used to convert the 0.5 m SMA cables (BullsEye) to miniSAS and twelve links in total were transmitted to Router. Noise was also increased gradually and the links started to fail at 200 mVp-p which corresponds to a jitter of 11.06 ps.

The different thresholds should be related to the highest attenuation of the signal when traversing the longest twinax cable. Finally the clock source was replaced by the RIM-L1DDC and the GBTX 160 MHz clock which showed no errors with a BER of $10E-14$ after 1.5 hours of operation.

**Figure 5.9:** *Setup for finding the phase mask threshold.*

5.3 Prototype-2 description

In this section the RIM-L1DDC prototype-2 board, which was totally redesigned compared to prototype-1, is described. The layout was changed in a way that there are two completely independent circuits housed on a single PCB. The ground and power planes were separated and two power connectors were used. A SCA was also added to switch off/on the PAD trigger and router boards. The SCA provides via the GPIO pins an enable/disable signal to the FEASTs of PAD trigger and router boards. The single ended (sidebands) wires of the twinax cables are used for the transmission of this signal. The miniSAS pinout for Router and PAD trigger boards is illustrated in Figure 5.11(a) and 5.11(b) respectively. Moreover, the SCA can also measure the environmental variables of the RIM-L1DDC itself.

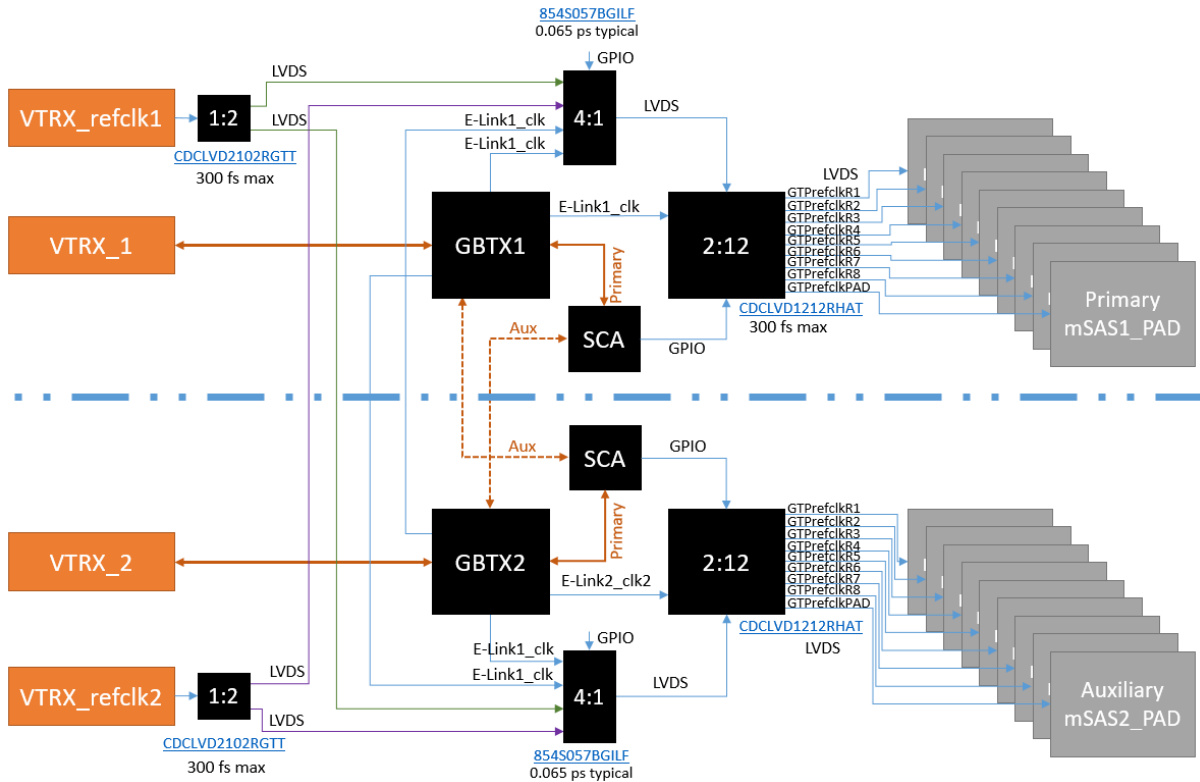


Figure 5.10: RIM-L1DDC prototype-2 block diagram.

Tests on RIM-L1DDC prototype-1 showed that the system can work stably but it can be marginal. Furthermore the jitter of the reference clock can be increased inside the RIM crate with all boards installed in it due to radiated noise. Thus, it was unclear if the GBTX's 160 MHz E-Link clock was good enough to be used as a reference clock for the Xilinx's 7-family FPGA transceivers. For that reason it was decided to provide a dedicated clock through an additional fiber to the RIM-L1DDC. To receive the dedicated clock an extra VTRX was added to the board. That clock is distributed to the Router and PAD trigger boards via low jitter fanouts. In order to have full redundancy three different fanout buffers are used: a 1:2, a 4:1 and 2:12. With this scheme the final output to the PAD and router boards (output of the 2:12 fanout buffer) can be either

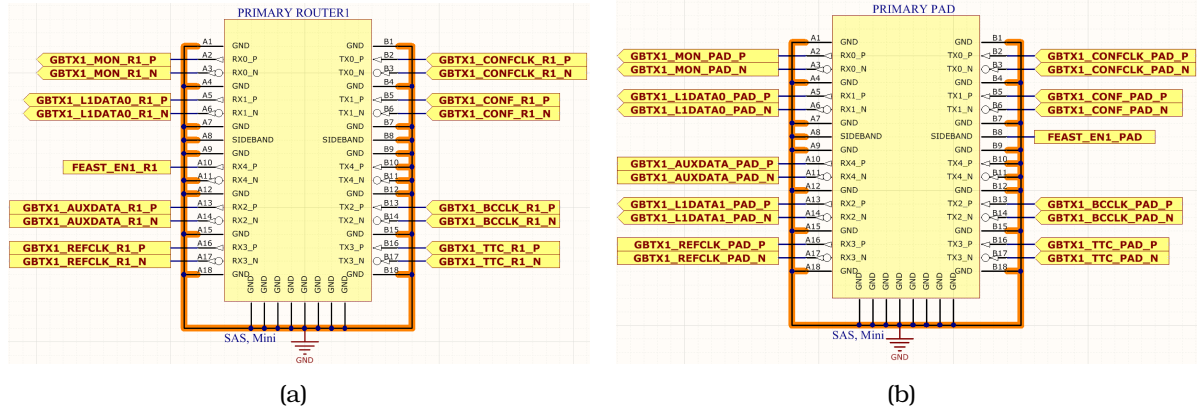


Figure 5.11: RIM-L1DDC prototype-2 miniSAS pinout for (a) Router and (b) PAD board.

the dedicated clock coming from the VTRX1 or VTRX2 (selectable via GBT-SCA GPIO), either the E-Link output of the GBTX1 or GBTX2. The block diagram showing the clock distribution of the RIM-L1DDC is shown in Figure 5.10.

Before the fabrication of the RIM-L1DDC the performance of the dedicated clock was verified with a fanout board. This board utilizes all the fanout buffers that are used on the RIM-L1DDC prototype-2. The tests were performed again using the E5052B phase noise analyser. As clock source the CDCE62005 clock synthesizer was used. The 160 MHz clock was fed to the fanout board via SMA cables and then to a VTRX optical transceiver. The same VTRX was used to receive back the clock over 110 m fiber (two fibers with length 30 m and two of 30 m coupled together with couplers were used). Then from the VTRX the clock was driven to the fanout network. Measurements showed that there was no significant jitter added either from the fiber neither from the fanouts. Four boards of the RIM-L1DDC prototype-2 board were received in August 2018. The top side of the board is shown in Figure 5.12(a), the bottom side in Figure 5.12(b) and the layout in Figure 5.12(c).

The board dimensions of the RIM-L1DDC prototype-2 remained unchanged (170 mm×170 mm). Length equalization of the differential pairs was done between TX pair and clock of every E-Link. A common ground for the digital and analogue pins of the GBTX was used according to the GBTX designers instructions. The power connector that was selected was the four position Molex Micro-Fit with part number: 0436500401 (mating with the cable connector with part number: 0436450408 and contacts with part number: 043030009). It is composed by a high temperature thermoplastic material and the flammability complies with the 94V-0 standard. For prototype-2 pins one/four are connected to GND and two/three to PWR as shown in Figure 5.13(b). The numbering is according to Molex's datasheet (Figure 5.13(d)). The pinout was finally modified to be compatible with the rest rim electronic boards (PAD trigger and Router) as shown in Figure 5.13(c).

For the distribution of the dedicated clock a custom board will be fabricated. The board will be placed in the USA15 and for that reason commercial electronics can be used. It can be a standard VME 6U that can be powered on by VMEbus on the NSW TTC VME crate. In total one RIM-L1DDC will be used for each sector resulting in a total of 32

Table 5.4: GBTX bank configuration for RIM-L1DDC. The signals highlighted with red color indicating the additional signals added in prototype-2.

RIM-L1DDC P2							
		GBTX1			GBTX2		
		DIO	DIN	DCLK	DIO	DIN	DCLK
BANK0	0	SCA Router1	SCA Router1	SCA CLK Router1	SCA Router1	SCA Router1	SCA CLK Router1
	1	SCA Router2	SCA Router2	SCA CLK Router2	SCA Router2	SCA Router2	SCA CLK Router2
	2	SCA Router3	SCA Router3	SCA CLK Router3	SCA Router3	SCA Router3	SCA CLK Router3
	3	SCA Router4	SCA Router4	SCA CLK Router4	SCA Router4	SCA Router4	SCA CLK Router4
	4	SCA Router5	SCA Router5	SCA CLK Router5	SCA Router5	SCA Router5	SCA CLK Router5
	5	SCA Router6	SCA Router6	SCA CLK Router6	SCA Router6	SCA Router6	SCA CLK Router6
	6	SCA Router7	SCA Router7	SCA CLK Router7	SCA Router7	SCA Router7	SCA CLK Router7
	7	SCA Router8	SCA Router8	SCA CLK Router8	SCA Router8	SCA Router8	SCA CLK Router8
BANK1	8	AUX Router1		GBTX1_REFCLK1	AUX Router1		GBTX1_REFCLK1
	9	AUX Router2			AUX Router2		
	10	AUX Router3		GBTX1_REFCLK3	AUX Router3		GBTX1_REFCLK3
	11	AUX Router4			AUX Router4		
	12	AUX Router5			AUX Router5		GBTX1_REFCLK2
	13	AUX Router6			AUX Router6		
	14	AUX Router7	SCA L1DDC aux	GBTX1_REFCLK2	AUX Router7	SCA L1DDC	
	15	AUX Router8	SCA L1DDC		AUX Router8	SCA L1DDC aux	
BANK2	16	TTC Router1	L1DATA0 Router1	BCCLK Router1	TTC Router1	L1DATA0 Router1	BCCLK Router1
	17	SCA L1DDC		SCA CLK L1DDC	SCA L1DDC		SCA CLK L1DDC
	18	TTC Router2	L1DATA0 Router2	BCCLK Router2	TTC Router2	L1DATA0 Router2	BCCLK Router2
	19	SCA L1DDC aux		SCA CLK L1DDC aux	SCA L1DDC aux		SCA CLK L1DDC aux
	20	TTC Router3	L1DATA0 Router3	BCCLK Router3	TTC Router3	L1DATA0 Router3	BCCLK Router3
	21						
	22	TTC Router4	L1DATA0 Router4	BCCLK Router4	TTC Router4	L1DATA0 Router4	BCCLK Router4
	23						
BANK3	24	TTC Router5	L1DATA0 Router5	BCCLK Router5	TTC Router5	L1DATA0 Router5	BCCLK Router5
	25						
	26	TTC Router6	L1DATA0 Router6	BCCLK Router6	TTC Router6	L1DATA0 Router6	BCCLK Router6
	27						
	28	TTC Router7	L1DATA0 Router7	BCCLK Router7	TTC Router7	L1DATA0 Router7	BCCLK Router7
	29						
	30	TTC Router8	L1DATA0 Router8	BCCLK Router8	TTC Router8	L1DATA0 Router8	BCCLK Router8
	31						
BANK4	32	TTC PAD	L1DATA0 PAD	BCCLK PAD	TTC PAD	L1DATA0 PAD	BCCLK PAD
	33						
	34						
	35						
	36	AUX PAD	L1DATA1 PAD		AUX PAD	L1DATA1 PAD	
	37						
	38						
	39						
EC		SCA PAD	SCA PAD	SCA CLK PAD	SCA PAD	SCA PAD	SCA CLK PAD

RIM-L1DDC boards (16 sectors/Wheel). Due to the redundancy, two dedicated clocks will be used per RIM-L1DDC. Two clock distribution boards will be used per wheel which correspond to 32 clock outputs per board. The clock input can be the TTCvx or the ALTI module. Then is distributed to four jitter cleaners (SI5345 from Silicon Labs) via a 1:4 fanout buffer. Twelve jitter cleaner outputs (each chip has ten outputs) can be grouped and driven to a miniPOD. Then with the use of MTP24-to-LC cables the reference clock is distributed to the RIM-L1DDC boards as shown in Figure 5.14.

The RIM-L1DDC prototype-2 board was designed again with 16 layers and the stackup is identical with the MM-L1DDC prototype-3 as presented in Figure ?? of

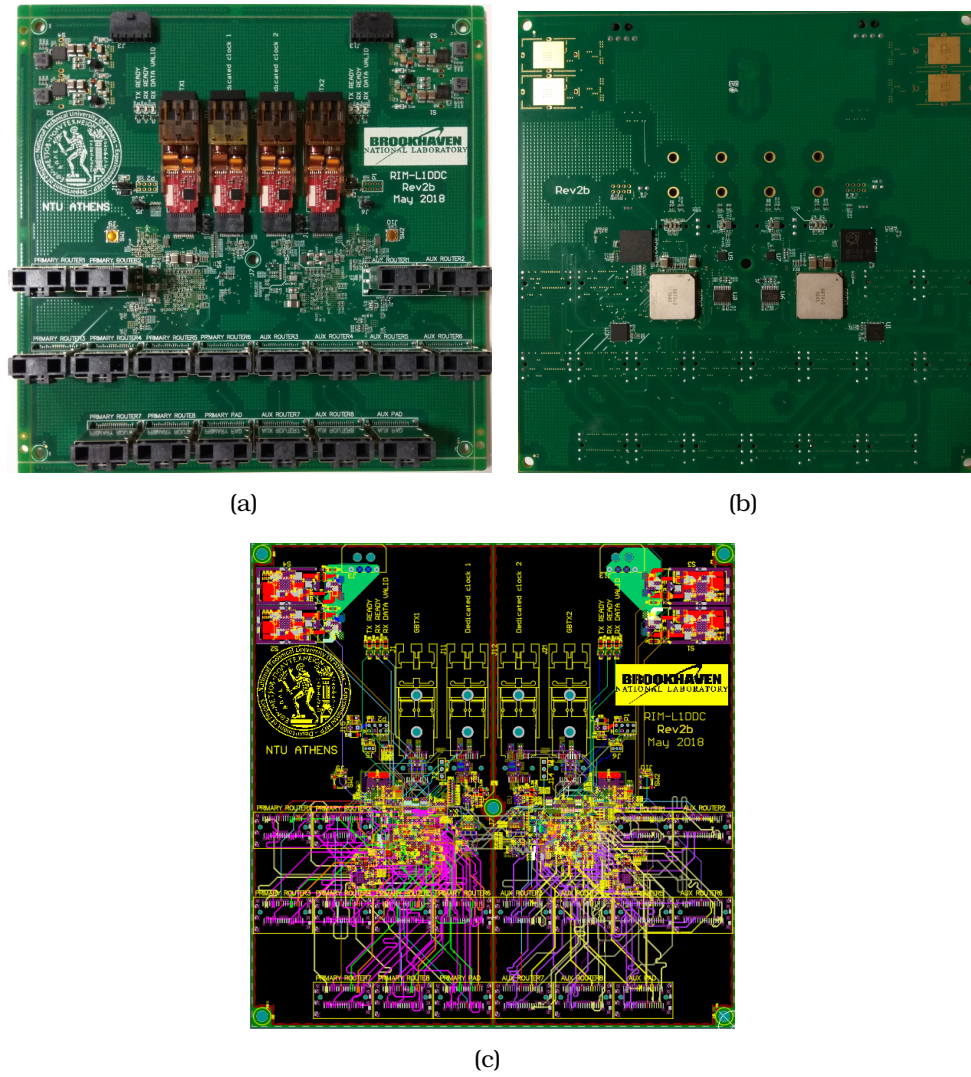


Figure 5.12: *RIM-L1DDC prototype-2.*

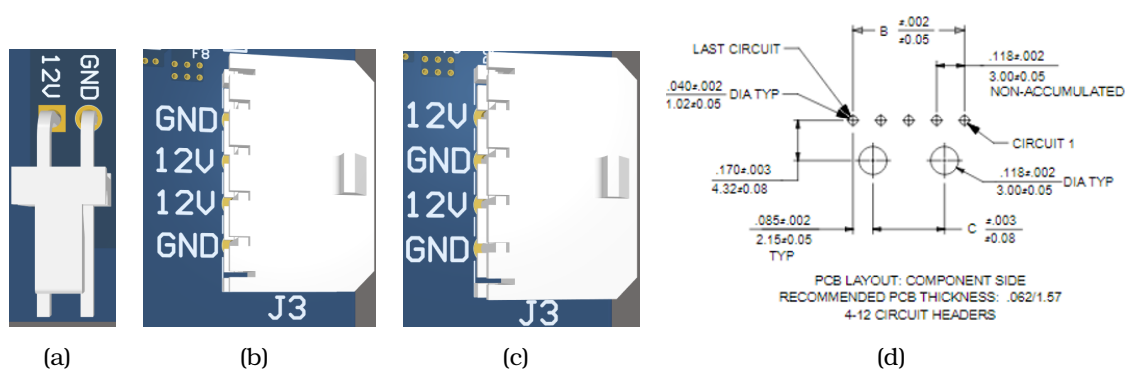


Figure 5.13: *RIM-L1DDC power connector pinout: (a) prototype-1, (b) prototype-2, (c) final, (d) Datasheet*

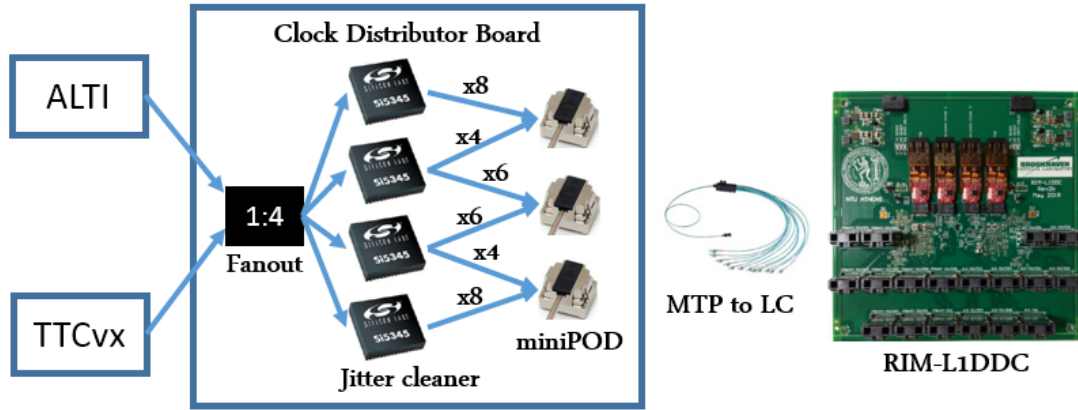


Figure 5.14: Clock distribution board concept.

Section 4.3.

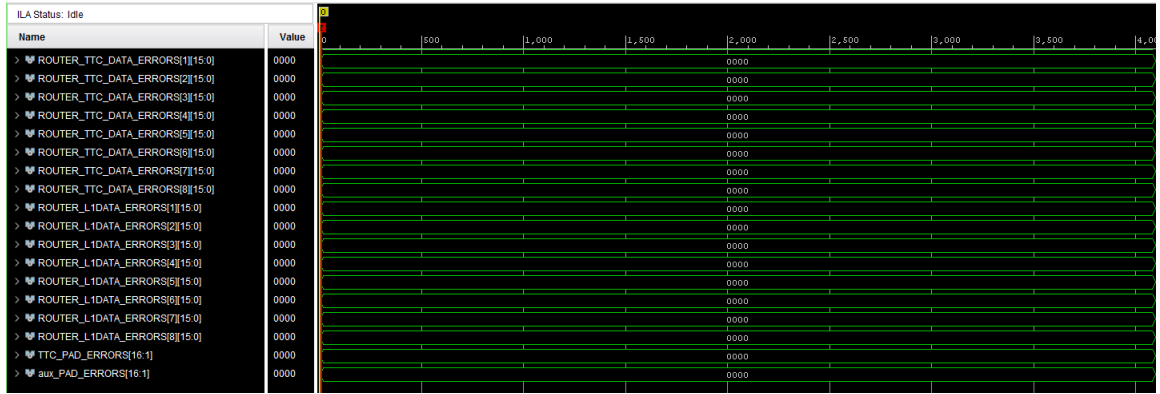
5.4 Prototype-2 tests

No schematic or layout errors found on the RIM-L1DDC prototype-2 and the boards are fully functional. An error occurred during the eFUSE programming and as a result one GBTX fails to lock and cannot establish the link with the back-end system. It seems that almost all registers have wrong values but GBTX can be functional after reprogramming it via the I²C dongle. The micro-DAQ system was used to verify the functionality of the RIM-L1DDC prototype-2. All E-Links were tested in the nominal rates. The GBTX was configured in training mode and the differential termination was enabled in all receiving E-Links. Figure 5.15(a) illustrates the TTC router data at 80 Mbps, router L1DATA at 160 Mbps, PAD TTC and auxiliary data at 320 Mbps being transmitted during the test. In Figure 5.15(b) the errors observed for the data being transmitted/received are shown. Generally zero errors appeared in all tests and the BER was 1.23E-15. Furthermore, all E-Link outputs were tested using an oscilloscope from Tektronix (DPO5054B). A typical output of the TTC for the PAD board at 320 Mbps is shown in Figure 5.16(a) and for the router at 80 Mbps in Figure 5.16(b).

The GBTX and the dedicated reference clocks at 160 MHz were measured at the fanout outputs by using the E5052B Phase noise analyser. The clock source was again the CDCE62005 clock synthesizer and as the back-end the VC709 running the GBT-FPGA firmware was used. An example of the GBTX reference clock for the Router board with a jitter of 4.09 ps is shown in Figure 5.17. To measure the jitter of the dedicated clock the setup presented in Figure 5.18 was implemented. The CDCE62005 clock synthesiser was used again to provide the clock, then with 0.5 m miniSAS cables the LVDS signal was transmitted to a custom made Fanout board. This board was used to convert the LVDS into optical signal, which subsequently was transmitted to the RIM-L1DDC through total 110 m fiber. Due to the lack of a direct 110 m fiber one 50 m and two 30 m fibers interconnected with LC-LC couplers were used. Finally the output clock from the RIM-L1DDC was driven to a custom made miniSAS-to-SMA bracket board (specifically designed for the testing setups and is described in detail in section A.3.2)

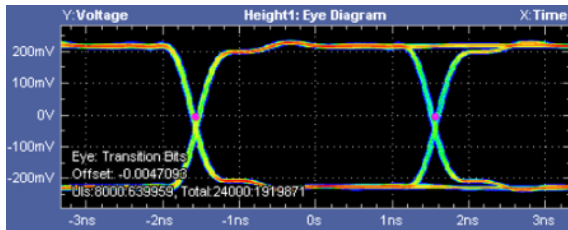


(a)

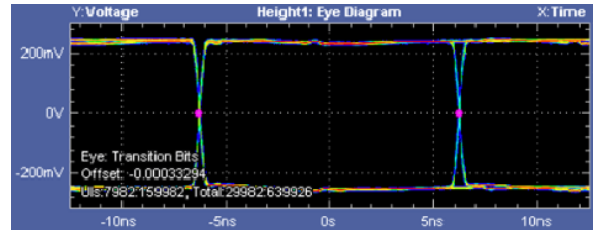


(b)

Figure 5.15: E-Link serial transmission and error testing of the RIM-L1DDC prototype-2.



(a)



(b)

Figure 5.16: Eye diagrams of the TTC link for the (a) PAD board at 320 Mb/s and (b) Router board at 80 Mb/s.

via a 0.5 m twinax cable from 3M and then to the phase noise analyser using 0.7 m SMA cable. Despite the complexity of the setup the jitter of the dedicated clock at 160 MHz measured to be at about 1.26 ps as shown in Figure 5.19.

The IC communication was also verified and all 365 registers were successfully written and read back via the fiber. The SCA communication was also tested and it was able to read all the values of the ADCs but also to enable and disable the GPIO signals. The GPIO signals were used to alternate between the GBTX and the dedicated clock using the fanout network. Finally the FEAST enabling/disabling feature was

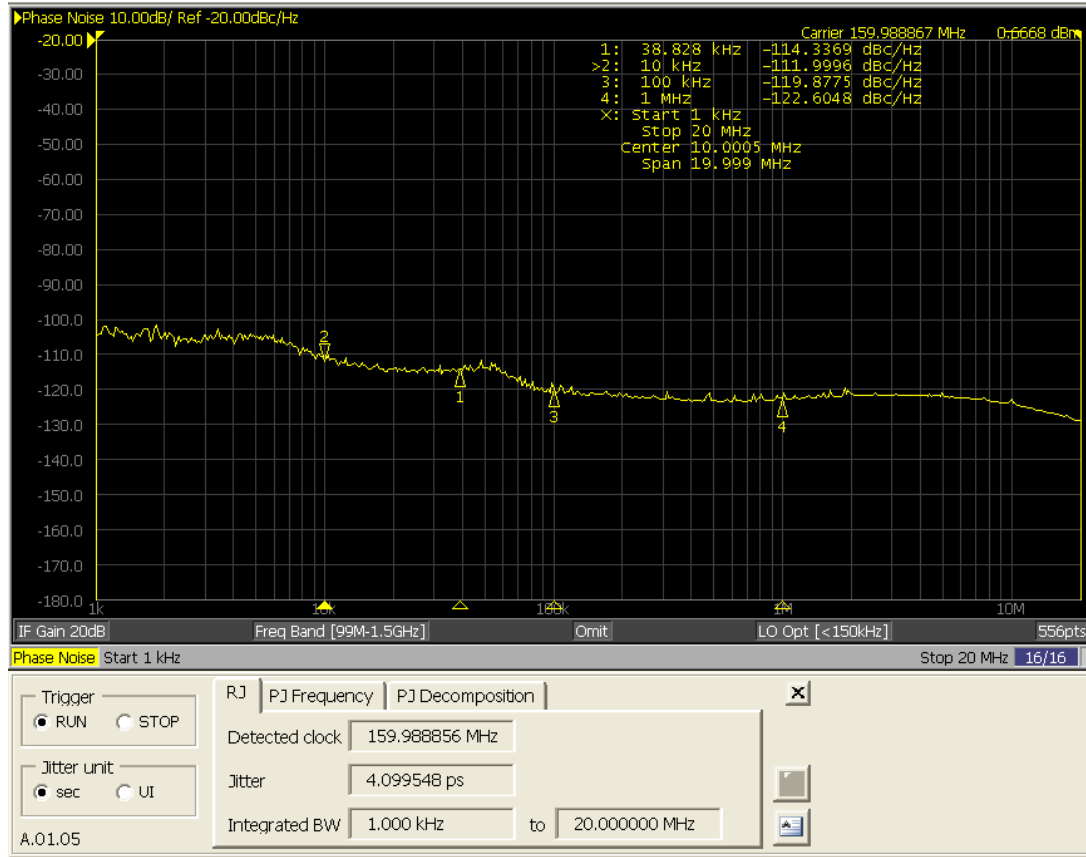


Figure 5.17: Jitter of the GBTX reference clock at 160 MHz.

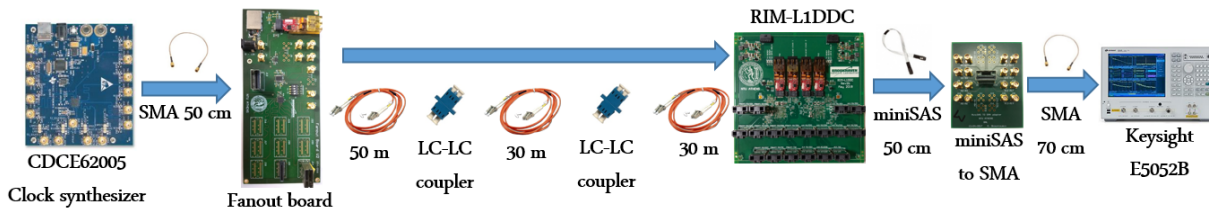


Figure 5.18: Evaluation of the dedicated clock. In total 110 m of fiber with two couplers were used.

verified by using the final prototypes of the PAD trigger and Router boards.

Xilinx provides the phase noise mask for the 156.25 MHz and not for the 160 MHz. A correction factor to the mask point according to the equation:

$$PhaseNoiseAt(X)MHz = PhaseNoiseAt(Y)MHz + 20 \times \log \frac{X}{Y}$$

was applied. The phase noise of the dedicated and GBTX E-Link clock at 160 MHz were compared with Xilinx's phase mask. Even though the dedicated clock appeared to have a much better performance compared to E-Link GBTX clock, is still above the mask as shown in Figure 5.20. Both clocks were extensively tested using the whole final trigger chain and showed perfect performance with no errors on the links. From the above we can conclude that the FPGA transceivers are relative robust to jitter and the phase

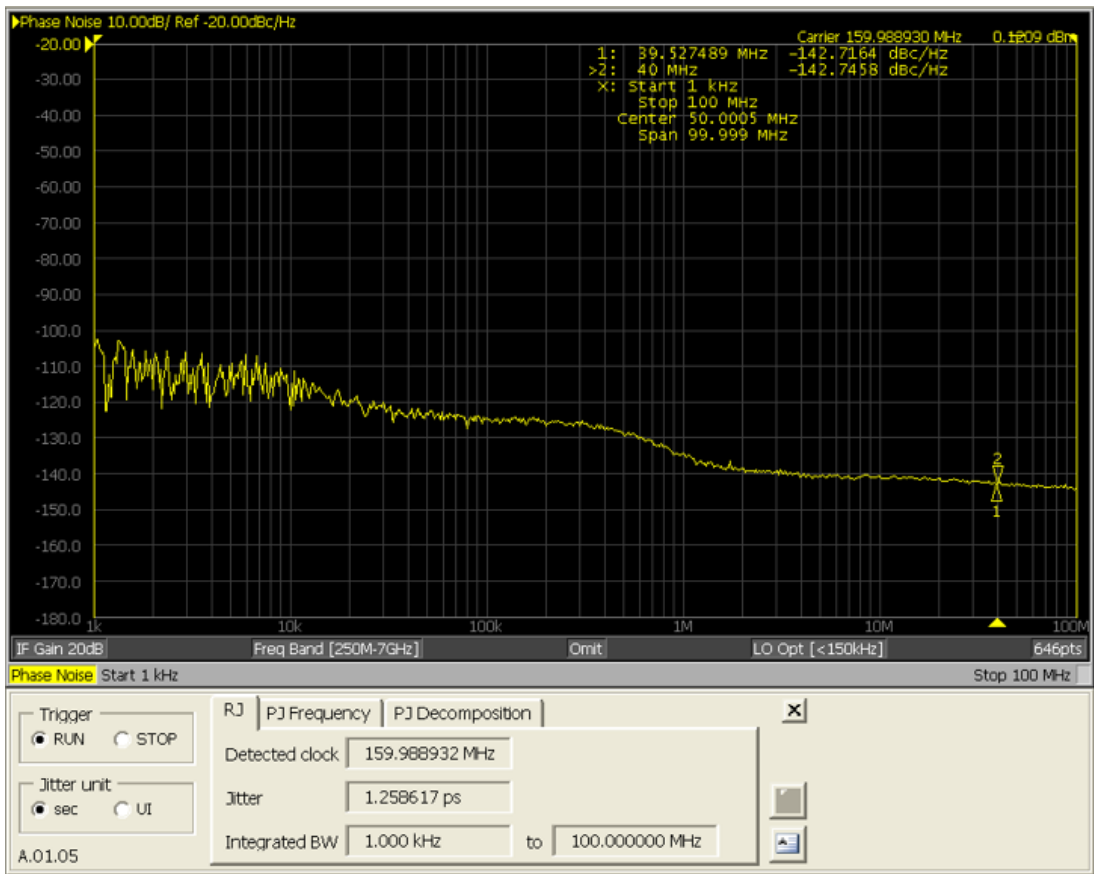


Figure 5.19: Jitter of the dedicated clock with 110 m fiber measured with the Keysight E5052B signal source analyzer. The jitter measured to be at 1.26 ps

mask is very strict.

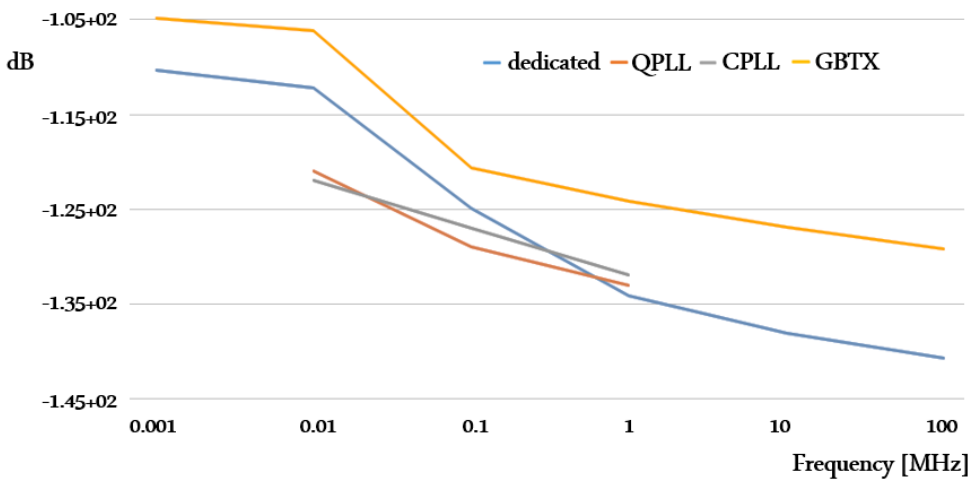


Figure 5.20: Jitter performance of the RIM-L1DDC compared to Xilinx's phase mask.

5.5 Evaluating with final setup

To evaluate the jitter performance of the dedicated clock the setup showed in Figure 5.21 was implemented. TTCvx module was providing the 40.079 MHz BC clock (TTL signal from a LEMO to SMA cable) to the SI5345 jitter cleaner evaluation board. It uses a fourth-generation DSPLL™ and MultiSynth™ technologies to enable any-frequency clock generation and jitter attenuation for applications requiring the highest level of jitter performance. This chip can be used for any-frequency clock generation and jitter attenuation for applications requiring the highest level of jitter performance. The DSPLL architecture by Silicon Labs, combines an analog low phase noise LC-VCO, a digital Phase Locked Loop (PLL) architecture, and cutting edge CMOS technology to provide a solution offering higher integration, smaller form factor, lower power, and more robust performance in comparison to conventional cascaded PLL devices. A PLL is a feedback circuit designed to allow the on board circuit to synchronize the phase of its own clock with an external timing signal. PLL circuits operate by comparing the phase of the external signal to the phase of a clock produced by a voltage controlled crystal oscillator (VCXO). The circuit then adjusts the phase of the oscillator's clock signal to match the phase of the reference signal. Thus, the original reference signal and the new signal are precisely in phase with each other.

The generated 160 MHz output clock via SMA cables is driven to the Fanout board which basically translates the LVDS differential to optical signal. The clock is transmitted to RIM-L1DDC and distributed to PAD board via the fanout network that was described in section 5.3. Four pFE boards were transmitting PRBS-31 data at 4.8 Gb/s (one link per pFEB) to one PAD trigger by using 1 m sata-to-miniSAS cable. The IB-ERT core was running on PAD trigger board checking for errors on each link. After transmitting 7.61×10^{10} bits on all four links, zero errors occurred and the BER ratio was 1.313×10^{-14} as shown in Figure 5.22. sTGC-L1DDC was used to provide the 40 MHz reference clock to the pFEB for the generation of the high speed data.

5.6 Radiation tests

Neutron irradiation tests of the GBTX and of the fanout chips that are used on the RIM-L1DDC boards were performed in May 2017 and June 2018, respectively. These tests took place at the 5.5 MV HV TN-11 TANDEM Van Der Graaff accelerator of NCSR "Demokritos" in Athens, Greece. In this facility neutrons can be produced through the reactions presented in Table 5.5. For the purposes of these tests, mono-energetic neutrons were produced via the $^3\text{H}(d,n)^4\text{He}$ reaction where a deuteron beam of 4 – 5.9 MeV impinged on a thin solid tritiated titanium target deposited on a copper backing. A molybdenum foil of 10 μm was set in front of the tritiated target for wear protection, while the target was cooled by using lateral heat conduction from the Al beam dump/target housing to the surrounding pressured cold air channel. The $^3\text{H}(d,n)^4\text{He}$ reaction using this setup under the aforementioned experimental conditions yielded neutrons of 19-24 MeV. The distance of the GBTX board from the target was not constant (from 14.4 up to 29.8 cm) and was depending on the test priority of the other boards. In Figure 5.23(a), the RIM-L1DDC board is visible on the left, as well as the

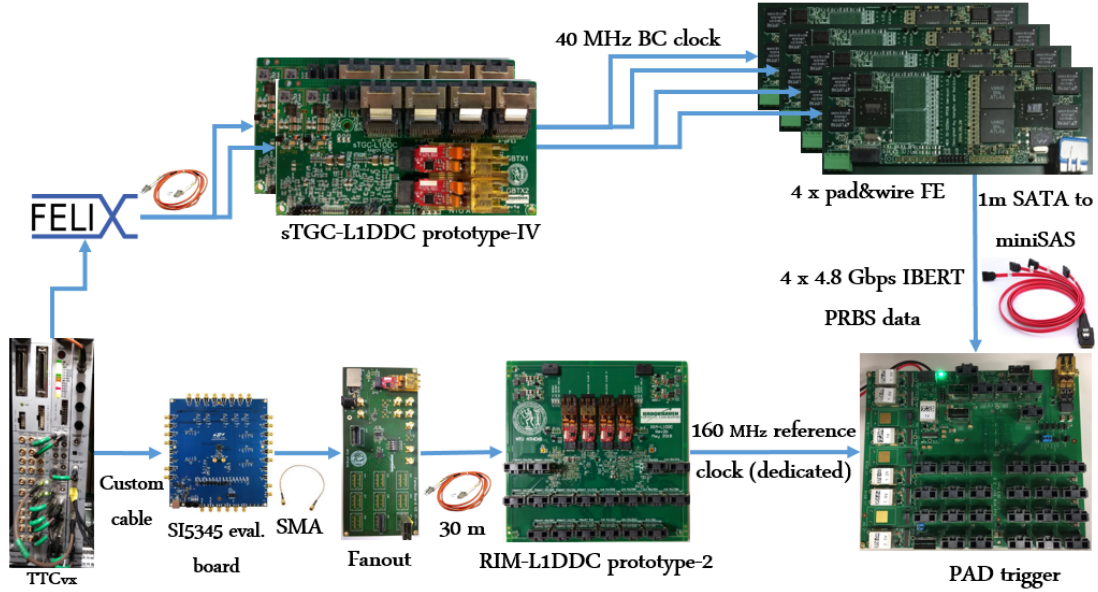


Figure 5.21: Setup for the validation of the dedicated clock.

Name	TX	RX	Status	Bits	Errors	BER
Ungrouped Links (0)						
Link Group 0 (24)						
Link 0	MGT_X0Y0/TX	MGT_X0Y0/RX	No Link	7.58E13	3.316E13	4.375E-1
Link 1	MGT_X0Y1/TX	MGT_X0Y1/RX	No Link	7.58E13	3.316E13	4.375E-1
Link 2	MGT_X0Y2/TX	MGT_X0Y2/RX	No Link	7.58E13	3.316E13	4.375E-1
Link 3	MGT_X0Y3/TX	MGT_X0Y3/RX	No Link	7.58E13	3.553E13	4.688E-1
Link 4	MGT_X0Y4/TX	MGT_X0Y4/RX	4.810 Gbps	7.617E13	0E0	1.313E-14
Link 5	MGT_X0Y5/TX	MGT_X0Y5/RX	4.810 Gbps	7.617E13	0E0	1.313E-14
Link 6	MGT_X0Y6/TX	MGT_X0Y6/RX	4.810 Gbps	7.617E13	0E0	1.313E-14
Link 7	MGT_X0Y7/TX	MGT_X0Y7/RX	4.809 Gbps	7.617E13	0E0	1.313E-14

Figure 5.22: IBERT test running on PAD trigger board.

target (on the center) and the beam pipe (on the right). The GBTX board was irradiated for a total of five days with various hours and fluence per day with a total dose of $4.99\text{E}+09\text{ n/cm}^2$ and total time of about 48 hours as shown in Table 5.6. For the purpose of the test a Xilinx ML605 evaluation board running the GBT-FPGA firmware was used. Prefixed data at 320 Mb/s from the evaluation board were sent to the GBTX and with external loopbacks (using 0.5 m twinax cables) data were sent back to the

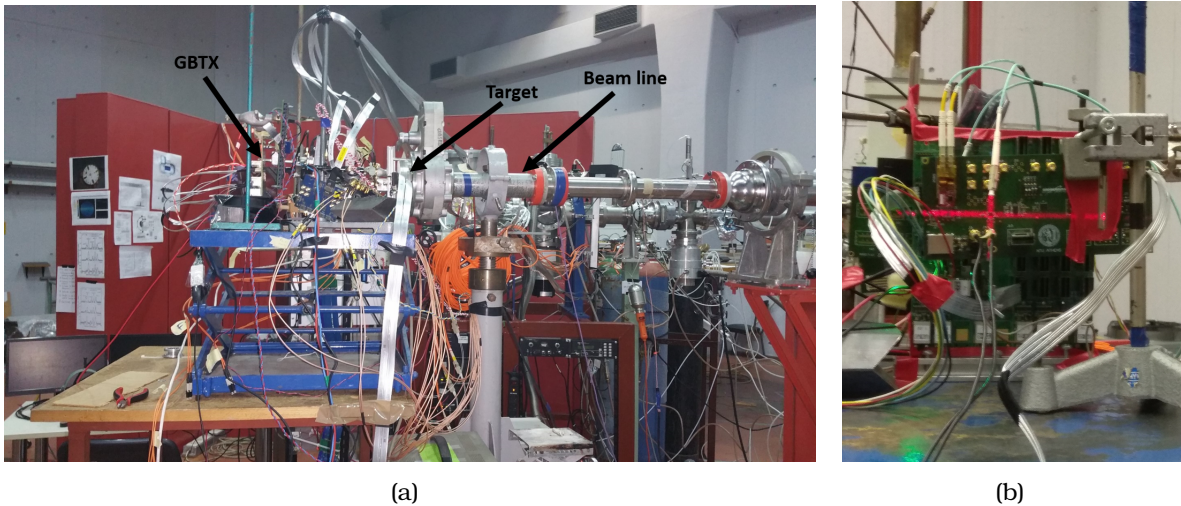
Table 5.5: Available reactions for neutron irradiation in the TANDEM accelerator at N.C.S.R Demokritos.

Nuclear Reaction	Proton or Deuteron Energy Range (MeV)	Neutron Energy Range (MeV)
$^7\text{Li}(p,n)^7\text{Be}$	1.9 to 8.4	0.1 to 6.7
$^2\text{H}(d,n)^3\text{He}$	0.8 to 8.4	3.9 to 11.5
$^3\text{H}(d,n)^4\text{He}$	0.8 to 8.4	16.4 to 25.7

Table 5.6: Distance of the GBTX from the target, fluence, time, neutrons and total dose.

DAY	Distance (cm)	Fluence (n/cm ² s)	Time (s)	Neutrons (n/cm ²)
1-2	29.8	5.26E+03	53280	3.36E+08
3	14.5	2.22E+04	39540	8.78E+08
4	16.7	1.67E+04	36180	6.04E+08
5	14.4	1.32E+05	8940	1.18E+09
Total			137940	3.00E+09

evaluation boards comparing the received and transmitted data. The required 120 MHz high quality reference clock for the ML605 transceivers was provided by the Texas Instrument clock synthesizer evaluation board (CDCE62005) as shown in Figure 5.24. The clock synthesizer and the ML605 board were placed outside the beam area and were connected with the GBTX board via a 60 m fiber. About 6 TB of user over the 28 TB of total data were transmitted during the test period and no errors were observed. The SEU correction register of the GBTX was monitored most of the time and no SEU errors were observed. Also no counts on FEC registers of the GBTX ASIC were observed.

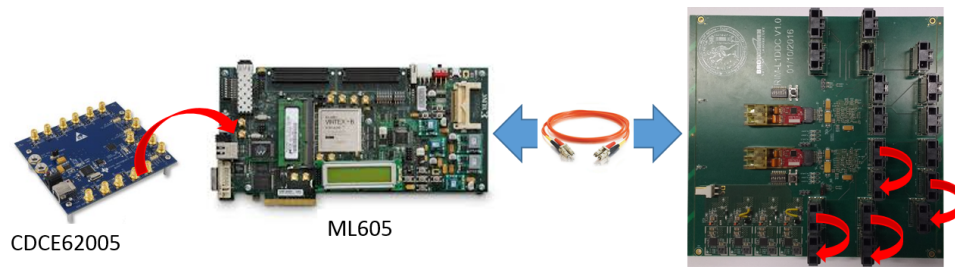
**Figure 5.23:** Setup at Demokritos: (a) RIM-L1DDC, (b) fanout board.

The 4:1 854S057BGILF fanout chip by IDT was also tested under radiation with the use of the fanout board. The Texas Instrument CDCE62005 clock synthesizer was providing the 160 MHz reference clock to the VTRX via SMA cables and then with a loopback, using a fiber, the clock was transmitted to the input of the fanout chip. The fanout outputs were driven to a Xilinx's VC709 evaluation board were feeding the PLLs and counters. The PLL locked signal was monitored and the counter was compared with a local one. In both cases zero errors were observed after 139200 seconds with maximum fluence of $4.6\text{E}+06 \text{ n/cm}^2$ and total dose of $6.45\text{E}+10 \text{ n/cm}^2$. The fanout board was placed in different distances under different fluence and time as is shown in Table 5.7. In figure 5.23(b) the board with the fanout chip centered at the beam line is

Table 5.7: Distance of the fanout board from the target, fluence, time, neutrons and total dose.

DAY	Distance (cm)	Fluence (n/cm ² s)	Time (s)	Neutrons (n/cm ²)
2	7.8	4.37E+04	38160	1.67E+09
3 run 1	7.8	3.64E+04	19560	7.12E+08
3 run 2	7.8	6.65E+04	12240	8.14E+08
3 run 3	7.8	6.86E+04	7200	4.94E+08
4	2.61	3.76E+05	36120	1.36E+10
5 run 1	8.6	3.6E+04	13800	4.97E+08
5 run 2	6.4	6.47E+04	1860	1.20E+08
5 run 3	6.4	1.31E+05	2760	3.62E+08
5 run 4	0.73	4.6E+06	10260	4.71E+10
Total			141960	6.54E+10

visible.

**Figure 5.24:** Testing scheme at Demokritos.

Services and testing procedure

6.1 Location of the L1DDC boards on detector and services routing

In this section the location and placement of the L1DDC boards as well as the routing services (miniSAS cables for the interconnection of the front-end, ADDC and L1DDC, fiber and power cables) will be described in detail.

6.1.1 sTGC board placement

On the sTGC detector, the L1DDC will be mounted on both detector edges, close to the outer rim. The L1DDC will serve the three strip or three pad & wire FEs of each sTGC plane. Four L1DDC boards will be placed in a sandwich scheme, as shown in Fig. 6.1. In this figure the cooling pipe which is attached to the cooling plates between the boards is also visible. FEAST will be cooled from the bottom side of the board with the use of a 10 mm × 10 mm exposed copper pad and sufficient vias. The copper plates will be attached to the ASICs and FEASTs pads with the use of bergquist thermal gap pads to compensate the height differences between the various components. The 3 mm GBTX is the highest component located at the bottom side of the board and by adding an additional 1 mm gap pad the copper cooling plate will be placed at 4 mm away from the surface of the board. Using a 4 mm gap pad will not be efficient and additional copper blocks will be placed for the FEAST and GBLD ASICs as shown on the right of Figure 6.1.

For the interconnection with the FE boards different cable lengths will be used. The various cable lengths and the number of cables according to the type of FE (pFEB or sFEB) are presented in Table 6.1. Each L1DDC utilizes two VTRX optical transceivers which means that in total 2048 fibers must be installed for the sTGC detectors.

6.1.2 Micromegas board placement

The front end electronics will be installed on the micromegas wedges radially along both sides of the plane. Especially, the L1DDC will be placed on the first and fourth plane

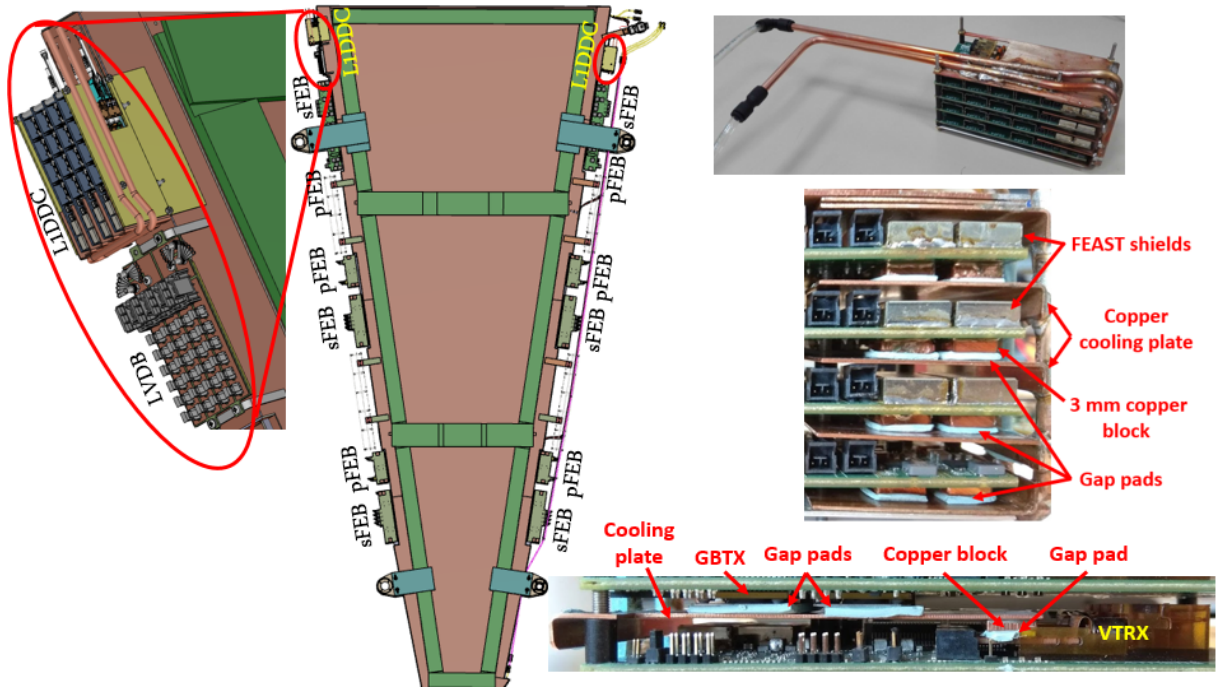


Figure 6.1: Placement of the L1DDC on an STGC wedge, right the four STGC-L1DDC packed inside the cooling box (the copper plates, gap pads and copper blocks are visible).

Table 6.1: Lengths and number of twinax cables for the interface of the STGC-L1DDC with pFEB and sFEB.

sFEB to L1DDC						
Quad	1 side	1 wedge	Total/sector	1 Wheel	2 Wheels	Length (m)
QL1	4	8	16	128	256	3.0
QL2	2	4	8	64	128	2.0
QL3	2	4	8	64	128	1.0
QS1	4	8	16	128	256	3.0
QS2	2	4	8	64	128	2.0
QS3	2	4	8	64	128	1.0
pFEB to L1DDC						
QL1	2	4	8	64	128	3.0
QL2	2	4	8	64	128	1.5
QL3	2	4	8	64	128	1.0
QS1	2	4	8	64	128	3.0
QS2	2	4	8	64	128	1.5
QS3	2	4	8	64	128	1.0

of each wedge (and especially in PCBs four and five) radially along both sides. Each L1DDC will serve eight micromegas FE boards on each edge of the detector (Fig. 6.2) and on the same plane. This means that in total eight L1DDC boards will be placed on a micromegas wedge. This provides a way of equalizing the load on both sides of

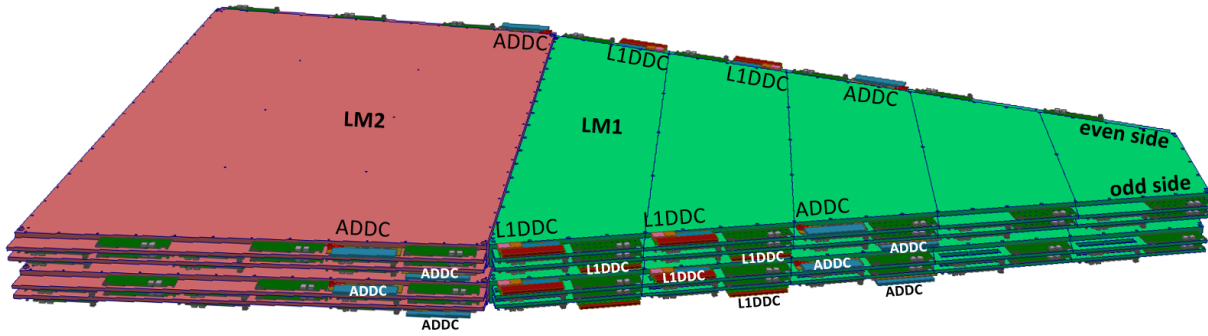


Figure 6.2: MMFE8/ADDC/L1DDC position on a micromegas sector.

the detector and the cable routing. The board will be mounted on the chamber with the use of 4 mm spacers as shown on the left of Figure 6.3. A non-conducting elastic thermal foam will be used to attach the ASICs to the cooling channel as shown on the right of Figure 6.3. In the upper part of both pictures, the L1DDC board mounted on a micromegas wedge is illustrated. On the top side of the L1DDC board the miniSAS connectors, the power connector and the VTRX/VTTX while on the bottom side the board the GBTX and the SCA ASICs are placed. These components are in thermal conduct with the cooling channel via an elastic thermal foam. Finally, on the bottom side of both pictures the FE board is also visible. Each MM-L1DDC utilizes one VTRX optical transceiver and a one VTTX optical transmitter which means that in total 2048 fibers must be installed for the micromegas detectors. For the power distribution a Low Voltage Distributor board, described in detail in Section A.2 was developed.

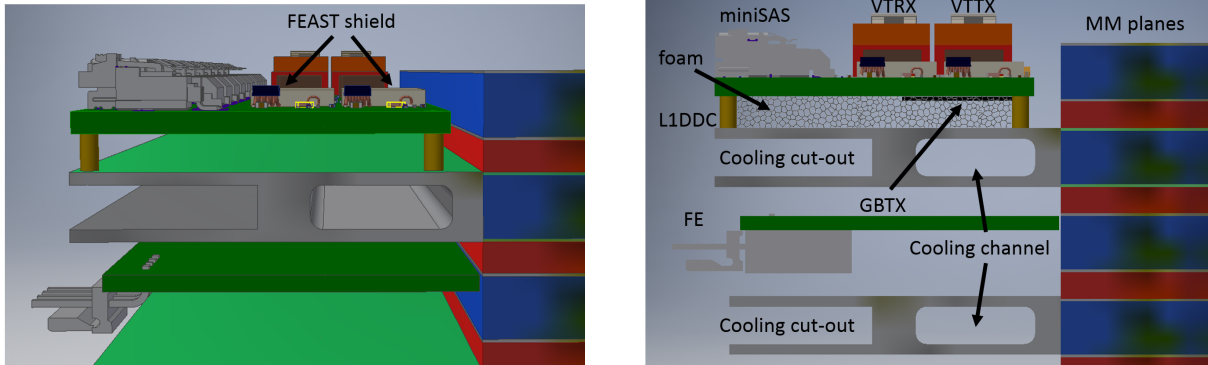


Figure 6.3: MM-L1DDC placement on the detector.

6.1.3 RIM board placement

The RIM-L1DDC along the PAD and Router boards will be placed inside a commercial crate called rim crate with the use of copper backplates. The bottom side of the boards, where all the components that dissipate heat are placed, will be attached to the copper plates. For better conductivity, non electrically conductive thermal foam will be placed between the chips and the plate. RIM-L1DDC will be mounted to the copper plates with the use of 4 mm spacers. On the bottom of the rim crate another copper plate is

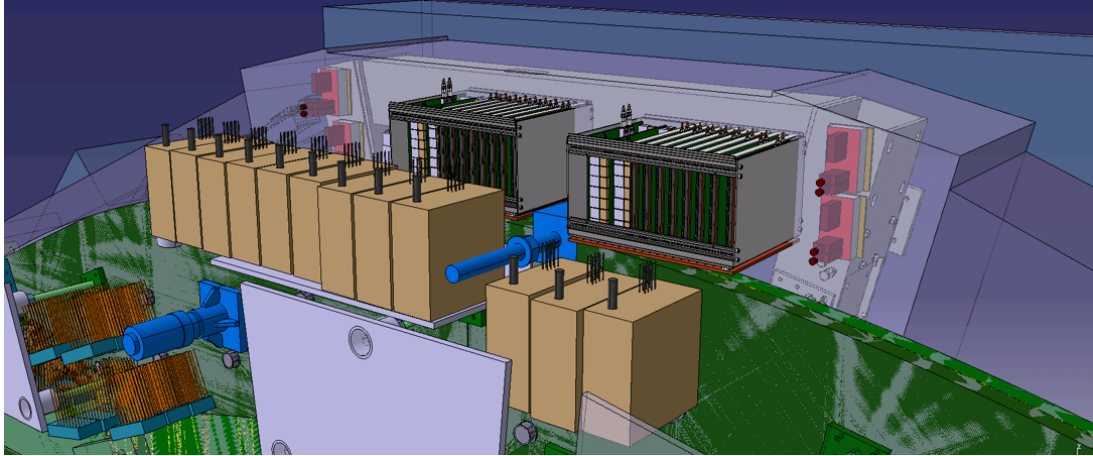


Figure 6.4: *RIM crates placed on the NSW.*

attached to the cooling channel. The rim crate will be mounted on the outer rim of the NSW and especially on the structure close to the large sector as shown in Figure 6.4. Due to the close proximity of the rim electronics inside the rim crate, 0.5 m twinax cables will be used for the interconnection of the boards. In total 32 RIM-L1DDC boards will be produced for the NSW upgrade. The two out of the four VTRXs of the RIM-L1DDC board are used only for the reception of the dedicated clocks. This means that in total 192 fibers (six per board) are needed in the NSW for the RIM-L1DDC.

6.2 L1DDC testing procedure

Due to the large number of L1DDC boards (1056 in total with 512 for the micromegas, 512 for the STGC and 32 for the trigger of the STGC detectors) that will be fabricated for the NSW a testing setup was deployed. The testing procedure is completely automated and all features of the board are checked at once to avoid any potential human errors. In this section we will describe in detail the whole testing process.

6.2.1 Procedures for the final L1DDC tests

For the final L1DDC board a set of tests must be performed in order to decide if the board is accepted for use. First of all power consumption, and thus the current, must be within a safe margin of $\pm 5\%$. The integrity of the data and clocks being transmitted from the L1DDC to the FE boards must also be verified. A FPGA Mezzanine Card (FMC) with nine miniSAS vertical connectors (described in Section A.3.1) is already designed to verify the E-Link communication. This miniSAS-FMC board, which is compatible with all versions of the L1DDC boards, is connected to Xilinx's VC709 evaluation board via a High Performance Connector (HPC). This evaluation board will generate the data with respect to the receiving clock for each E-Link, so both clock and data can be checked simultaneously. VC709 utilizes four optical connectors that can be used for the evaluation of the L1DDC optical links. Since the MM-L1DDC needs three receiving optical modules, VC709 proved to be ideal for these tests. The results

will be transmitted to a personal computer via Ethernet and UDP protocol and will be stored in the database. The CDCE62005 clock synthesizer provides a clean clock for the high speed lines of the 7-family FPGA transceivers.

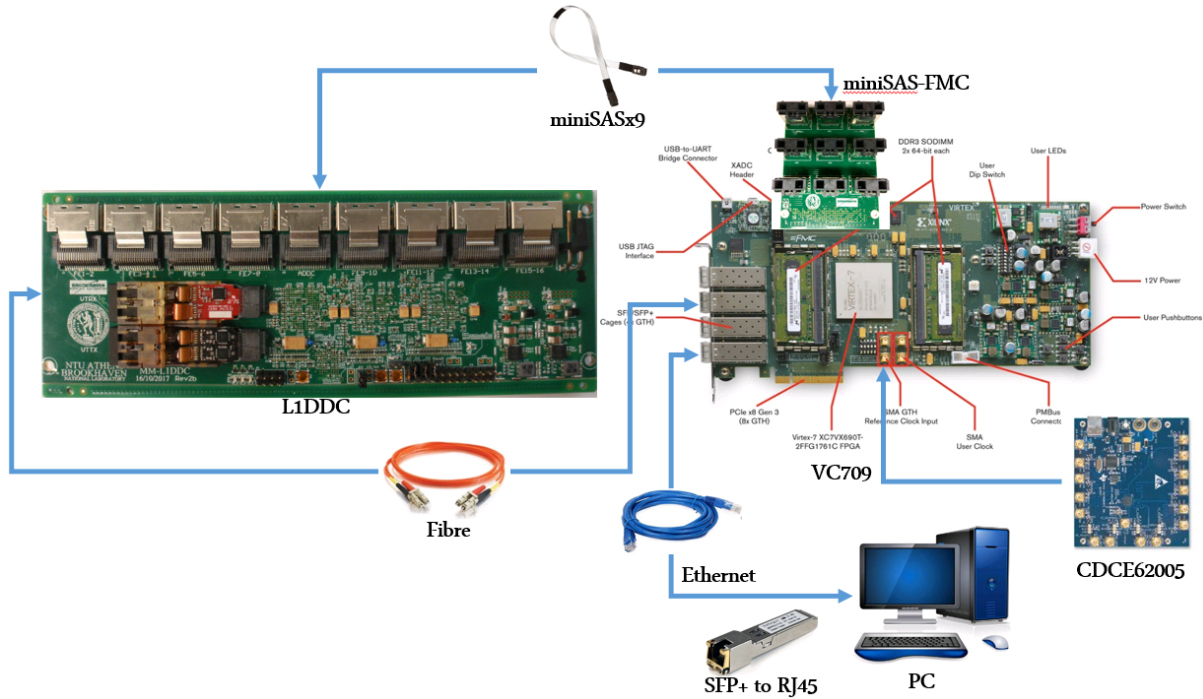


Figure 6.5: Typical setup for the testing of the final L1DDC boards.

A typical setup of the testing procedure is shown in Figure 6.5. Error checking can be performed in the firmware and if any errors occurred the specific board will be rejected. A few number of final L1DDC boards will be randomly selected to verify the reliability after long term operation. Finally some boards will be randomly selected for clock jitter measurements and data integrity tests by using a phase noise analyser and oscilloscope.

On the one path the PRBS data are fed to the GBT frame and are transmitted to the GBTX via the fiber and then via the serial lines back to the FPGA. On the other path the PRBS data are serialized and transmitted to the GBTX via the serial lines and then to FPGA via the fiber. In both cases data are received back to the FPGA and checked for errors. A PC is used to communicate with the VC709 using Ethernet and UDP packets.

Since the 10-pair cables are not available, all tests will be performed by using the 8-pair version. The serial communication with the L1DDC was verified with 0.5 m and 3 m twinax cables from 3M. During these tests differential data at 320 Mb/s were transmitted using the sideband (single ended lines) of the cables, without errors.

Three different testing setups equipped with the micro-DAQ will be allocated at the production sites. These sites are:

- National Technical University of Athens.
- Tomsk State University.

- National and Kapodistrian University of Athens, University of West Attica and University of Aegean.
- National Center for Scientific Research Demokritos.

In total 1084 L1DDC boards (522 MM-L1DDC, 522 sTGC-L1DDC and 40 RIM-L1DDC) should be tested. For an extensive test of one hour per board and assuming eight working hours per day, 34 days are needed in total for the four sites. One testing bench will be also available at CERN (BB5 building) for the final testing of the boards before the on-chamber integration. In case of problematic board detection, it will be send to the lab for detailed examination using the existing infrastructure.

A unique database for all NSW electronics is developed to store the board IDs, status and measurements. Each board will be marked with a fourteen alphanumeric identification number with the following format: 20MNEL1CM3000X. The code mapping is shown in Figure 6.6. For the board type CM is the L1DDC for the Micromegas, CT for the sTGC and CR for the RIM.

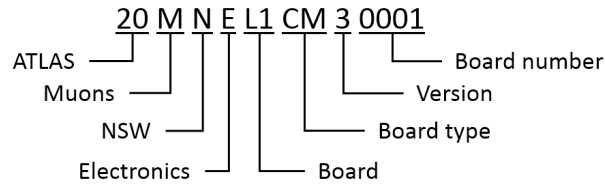


Figure 6.6: Board ID in the electronics database.

The variables that are selected to be stored in the database are:

- Board ID (according to the aforementioned format)
- Testing site that performed the measurements.
- Board version and board revision.
- If the board is functional.
- IDs for the GBTX1, GBTX2, GBTX3 and SCA ASICs
- If eFuse operation is implemented.
- Testing results including (SCA, I²C, and IC communication).
- Environmental variables (voltage levels for 1.5 V and 2.5 V FEAST outputs, FEAST/GBTX temperatures).
- Errors appeared in each E-Link (Tx, Rx and Clock) for all GBTXs.

6.2.2 Firmware development

As was described in the previous section for the massive tests of the L1DDC boards the micro-DAQ setup and firmware were deployed. The firmware was developed with the collaboration of the University of West Attica. The main blocks of the firmware are the GBT FPGA core, the Slow Control, the High Speed L1DDC Tester (HSLT) and the Ethernet are depicted in Figure 6.7. GBT-FPGA is a core provided by the GBT Group for the GBTX testing. This core sends and receives GBT frames to/from the GBTX. The GBT-FPGA firmware was migrated to the VC709 evaluation board and modified to have three fiber links.

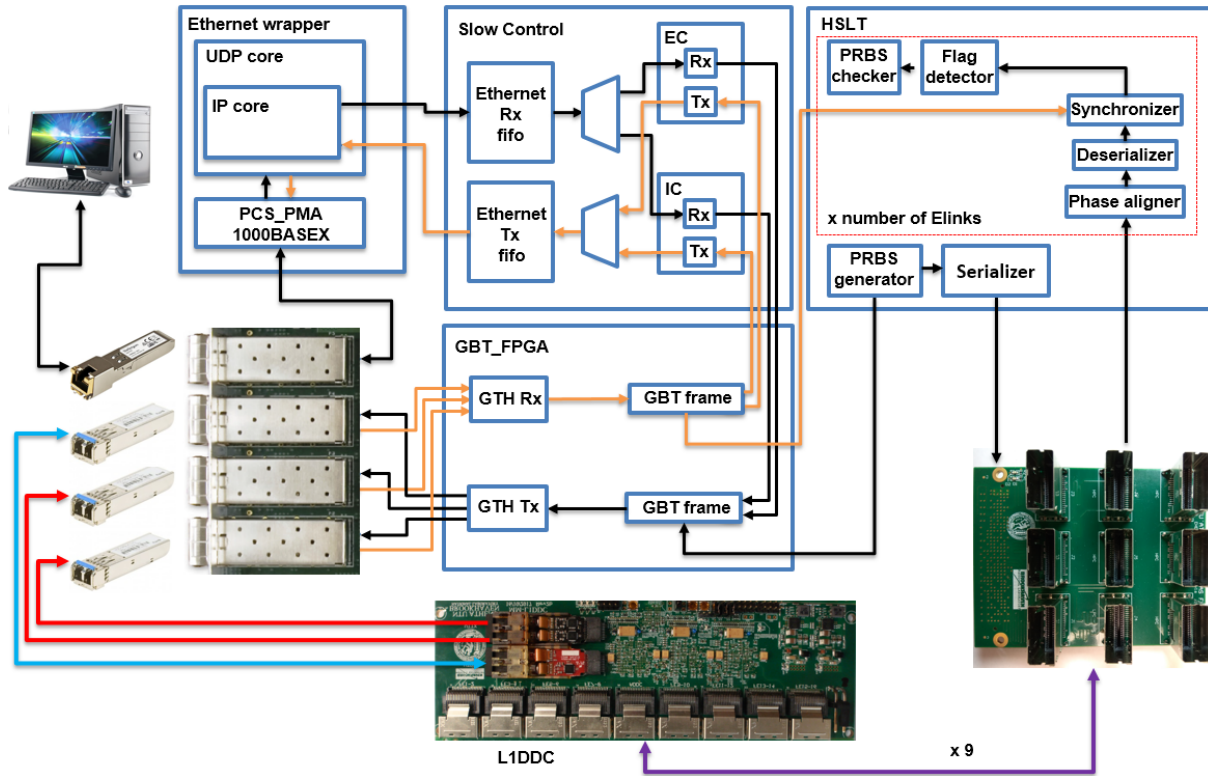


Figure 6.7: Micro-DAQ firmware block diagram. Contains the GBT-FPGA core, the Slow Control, the HSLT and the Ethernet wrapper.

For the transmission PRBS-7 data were used which is basically a seventh grade polynomial:

$$\text{PRBS7} = x^7 + x^6 + 1$$

These data are generated based on a deterministic algorithm that is difficult to predict and exhibits statistical behaviour similar to a truly random sequence. Moreover, generated data by the PRBS-7 sequence are similar to DC-balanced data required by the GBTX E-Link receivers for proper phase alignment. Thus, the PRBS generator and checker primitives provided by Xilinx were used. Data are encapsulated inside frames with Start Of Packet (SOP) and End Of Packet (EOP). The generated parallel data in various speeds (80, 160, 320 Mb/s) are fed to the GBT frame for optical transmission or to the deserializer and then to FMC-to-miniSAS for serial transmission. The GBT frame

is transmitted by the SFP+ of the VC709 evaluation board and received by the GBTX on the L1DDC side. GBTX distributes the incoming data to the corresponding E-Links and then via the FMC-to-miniSAS, data are received by the evaluation board.

For proper reception of the data a phase aligner circuitry is used. This circuitry is using the IDELAY2 by Xilinx which is a 31-tap, wraparound, delay primitive with a calibrated tap resolution. IDELAY allows incoming signals to be delayed on an individual input pin basis. The tap delay resolution is contiguously calibrated by the use of an IDELAYCTRL reference clock. A FSM is controlling the counter value of the primitive (CNTVALUEIN - 5 bit) from the FPGA logic for dynamically loadable tap value. With this configuration is ensured that the data are sampled in the middle of the eye diagram. Then data are deserialized and after the synchronizer are aligned properly as eight bit chunks. Then, the SOP and EOP can be identified while the PRBS data can be decapsulated. This procedure is implemented in the Flag Detector. Finally the payload is driven to the PRBS checker which identifies if there are any errors during the overall process. On the other direction, the serial data are received by the GBTX (miniSAS side), classified into the GBT frame and transmitted to the evaluation board via the optical link. The received parallel data for each E-Link are fed again to the Synchronizer and Flag detector and eventually to the PRBS checker for error detection. Multiple copies of the receiving chain inside the HSLT (Phase Aligner, Deserializer, Synchronizer, Flag detector and PRBS checker) are implemented depending on the number of active E-Links.

GBTX can receive SLVS/LVDS signals but transmits only SLVS. On the other hand the VC709 uses 1.8 V to power the banks for the FMC connector and for this reason the LVDS standard was used for the serial communication with the GBTX. With this standard and by enabling the internal termination of the FPGA was able to sample the incoming data correctly. VC709 does not have a RJ45 connector for Ethernet communication and for that reason the fourth SFP+ connector was used. A RJ45-to-SFP connector was utilized to interface with the `gig_Ethernet_PCS_PMA` IP core from Xilinx and the 1000-BASEX standard was implemented. The UDP/IP implementation is based on the open source code by `opencores.com`.

The Slow Control block is responsible for the GBT-SCA communication (EC) and the configuration of the GBTX (IC). VC709 firmware receives a UDP packet containing all the configuration data for the 366 read-write registers of the GBTX. For the IC configuration a write/read operation is implemented and the content of the 436 registers (366 read-write + 70 read only) is transmitted via Ethernet to a regular PC for evaluation. A similar operation is performed for the EC communication. The payload of the UDP containing the configuration data for the GBTX are encoded with the HDLC protocol and transmitted to the GBTX and finally to the on board GBT-SCA via the GBT frame and the optical link. The GBT-SCA on the L1DDC board uses the I²C interface to communicate with the two additional GBTXs as was described in section 2.4.1. Similar to the IC, a write/read operation of the GBTX registers is implemented and data are transmitted to the PC for comparison. Moreover a set of additional commands are transmitted in order to verify the proper functionality of the SCA, The ADCs are enabled and the environmental variables are sent to the software for monitoring. Finally, for the RIM-L1DDC the GPIOs should be enabled and checked.

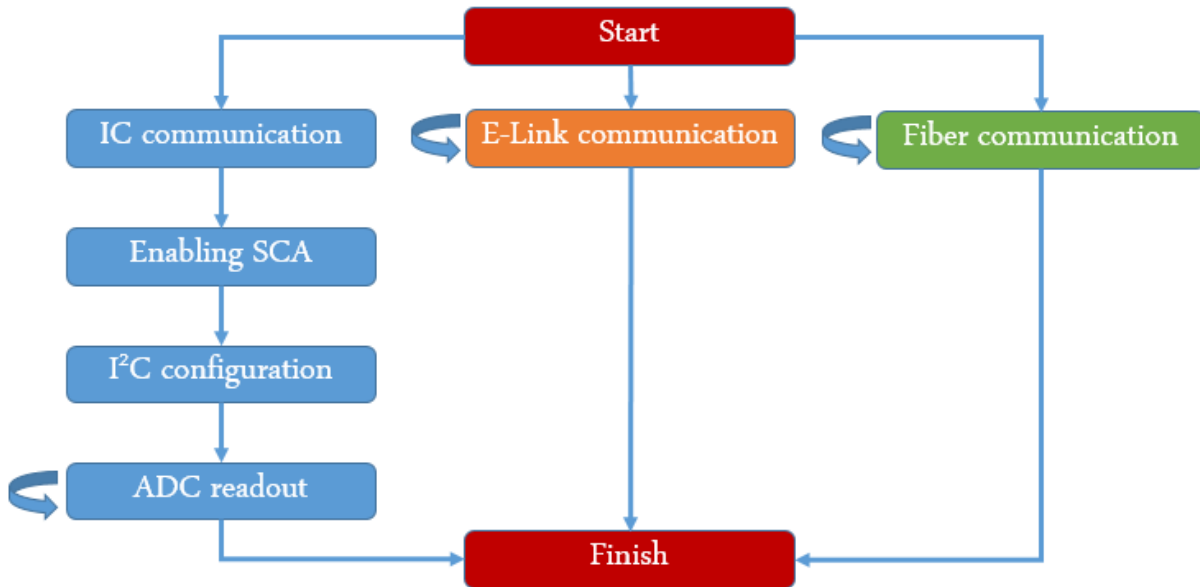


Figure 6.8: The FSM of the testing procedure.

The main FSM shown in Figure 6.8 controls all the steps of the testing process. After initiating the main FSM, the three distinct paths are enabled: the IC/EC communication, the serial and the optical transmission. The FSM will remain at the ADC readout, E-Link and fiber communication states to accumulate enough statistics for the evaluation of the board. The duration of the test can be specified by a drop-down menu at the GUI. A board is considered functional if all the steps are completed with no errors.

6.3 Use of repeaters

In this section we will describe the need of using repeaters to boost the signal over long meter cables (up to 6 m) for the sTGC triggering. The on-board repeaters of the PAD trigger and Router boards proved to be not sufficient for the long tin cables. The solution is to use additional repeaters in the middle of each cable length between the sFEB/pFEBs and the PAD trigger/Router. The measurements performed on both 4.8 Gb/s and 640 Mb/s and the results are presented.

6.3.1 Serial repeater

In Figure 6.9 is obvious that due to the attenuation of the 5 m tin twinax cable by 3M the eye is completely closed. The measurements performed with the DSA91204A Infiniium High Performance 12 GHz Oscilloscope. The maximum cable length for the high speed links in NSW is 6 m which implies that the direct signal transmission is unable. For the 4.8 Gb/s data transmission from pFEB to PAD trigger but also from sFEB to Router the serial repeater (Part Number: DS100BR410) by Texas Instruments is used. This chip is placed at the input lines of both PAD trigger and router boards.

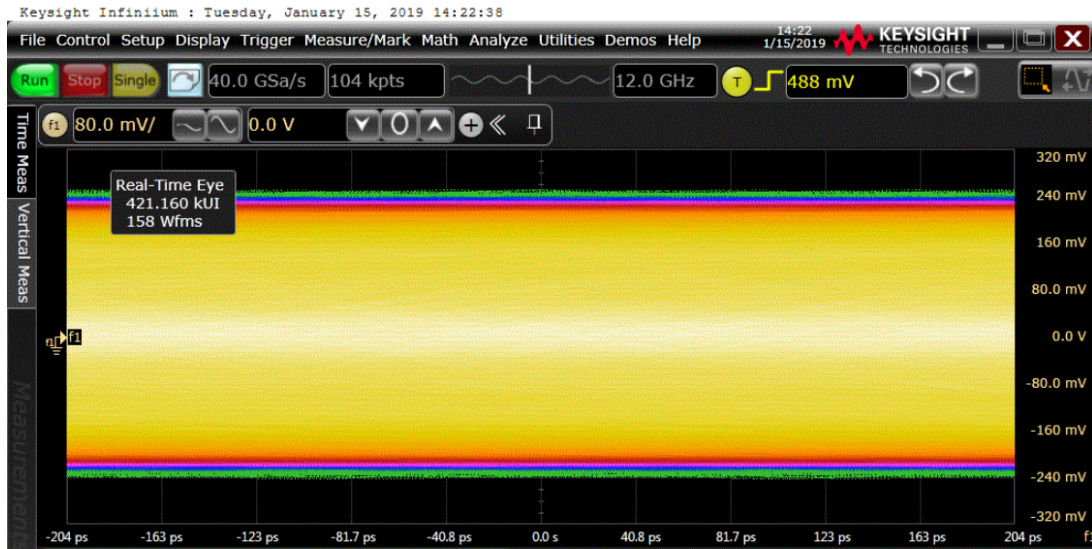


Figure 6.9: Eye diagram of the 4.8 Gb/s data from sFEB after 5 m of twinax cable.

Table 6.2: Boost/equalization pin mode configuration.

Inputs			SMBus Register Bits	Result at 5 GHz
BST2	BST1	BST1	[8:0]	
0	0	0	00000000	2.7 dB
0	0	1	00000001	7.3 dB
0	1	0	00000011	12.2 dB
0	1	1	00000111	16.6 dB
1	0	0	00001111	20.6 dB
1	0	1	00011111	24.8 dB
1	1	0	00101111	27.6 dB (default)
1	1	1	00011111	28.9 dB

It is an extremely low power, high performance quad-channel repeater for high-speed serial links with data rates up to 10.3125 Gb/s. A single supply operation at 2.5 V is needed using a 48-pin very thin Quad Flat No-lead (WQFN) package with 7 mm × 7 mm and 0.5 mm pitch. Moreover the device is capable of adjustable receive equalization and adjustable transmit de-emphasis on all channels to compensate for channel loss allowing maximum flexibility of physical placement within a system. The De-emphasis is controlled by one input signal with −9 dB if tied to Vdd, −6 dB if left open, −3 dB with a 20 kOhm to ground and 0 dB if tied to ground. The equalization boost settings are presented in Table 6.2.

The receiver's Continuous Time Linear Equalizer (CTLE) is capable of opening an input eye that is completely closed due to the Inter-Symbol Interference (ISI) induced by the interconnect medium such as backplane trace or cable. Finally the device has an adjustable output amplitude voltage level from 600 mV up to 1.2 V. The selection is made by only one input pin with the options: tie to Vdd (1.2 V), leave open (1.0 V), with



Figure 6.10: Eye diagram for 4.8 Gb/s data from sFEB with 8 m twinax cable and repeaters.

a 20 KOhm to ground (800 mV) and tie to ground (600 mV).

To test the signal integrity the transmitting data were monitored after 8 m silver cable and a repeater, which was emulating the on-board repeater of PAD trigger and Router boards. The signal was driven from the repeater to the oscilloscope by using an extra 0.5 m miniSAS cable, a miniSAS-to-SMA breaker board (described in Section A.3.2) and SMA cables. To achieve the optimal performance the repeater was configured with equalization boost of 28.9 dB, output amplitude of 1.2 V p-p and zero De-emphasis. The resulted eye is wide open and is presented in Figure 6.10. The mean value of the eye height is 474.6 mV and the width is 148.965 ps. Additional IBERT tests with the 8 m silver cable performed to evaluate the link between the sFEB and Router. The TDS ASIC is able to generate and transmit PRBS-31 data at 4.8 Gb/s. Running IBERT on Router managed to succeed a BER of $10E-15$ with zero errors. From the IBERT tests and eye diagrams is clear that for the 4.8 Gb/s link between PAD and router the on-board repeaters are adequate to drive the signal over the 8 m silver cables and no intermediate boosting is needed.

There was also the argument if by mounting the boards on the detector the noise will be increased and subsequently a higher jitter will affect the eye and the data transmission. The 40 MHz TDS reference clock for the high speed links is provided

Table 6.3: ROC register values that were tested.

Measurement	1	2	3	4	5	6	7	8	9	10	11	12
Register 6	99	99	99	99	99	99	99	99	99	9B	9B	9B
Register 7	88	22	28	2C	82	8C	C2	C8	CC	88	22	28
Jitter (ps)	8.21	8.21	8.19	8.18	8.01	8.03	8.01	8.09	8.08	7.87	7.96	7.86
Measurement	13	14	15	16	17	18	19	20	21	22	23	24
Register 6	9B	9B	9B	9B	9B	9B	9A	9A	9A	9A	9A	9A
Register 7	2C	82	8C	C2	C8	CC	88	22	28	2C	82	8C
Jitter (ps)	7.86	7.94	7.93	7.92	7.82	7.97	7.98	7.84	7.68	7.61	7.50	7.78
Measurement	25	26	27	28	29	30	31	32	33	34	35	36
Register 6	9A	9A	9A	98	98	98	98	98	98	98	98	98
Register 7	C2	C8	CC	88	22	28	2C	82	8C	C2	C8	CC
Jitter (ps)	17.72	7.96	7.98	7.9	10.34	9.84	10.09	10.17	11.14	10.32	10.22	10.25

Table 6.4: IBERT tests using the 8 m silver twinax cables.

Cable	Clock 40 MHz	Jitter (ps)	Ref. Clock 160 MHz	Jitter (ps)	Duration (h)	Errors	bits	BER
Cable1 (Lot 1723)	40	12	160	4	14	0	2.5E+14	3.4E-15
Cable2 (Lot 1738)	40	12	160	4	2	5	4.2E+13	1.2E-15
Cable2 (Lot 1738)	40	8	160	1.26	14	0	3.4E+14	2.9E-15
Cable3 (Lot 1738)	40	12	160	4	2	1	3.4E+13	2.9E-15

by the sTGC-L1DDC through the ROC. This clock is traversing the ROC PLL which is a classic Type-2, 3rd order loop PLL. Two registers are used to control the loop current but also the values of the loop resistor and capacitor. It was proved that by adjusting the values the output jitter varies from about 8.3 ps (0x9A for register 6 and 0x28 for register 7) up to 12.2 ps (0x98 for register six and 0xC2 for register seven). All measurements with the corresponding values and the resulted jitter are presented in Table 6.3. It appeared that even with the worst jitter there is no effect on the link stability by running IBERT tests and measuring the BER.

During the time of the tests only one 8 m silver cable was available. Later two additional 8 m silver cables received for testing. These cables belong to a different lot and appeared to have worse performance in terms of jitter. Tests repeated again with the worst jitter of 12 ps at the 40 MHz ROC clock and the 160 MHz GBTX clock with 4 ps jitter. The new cables showed errors (five and one) after two hours of operation with a BER of 1.2E-15 and 2.9E-15 respectively. The results are presented in Table 6.4. After these tests it was decided that the additional serial repeaters are necessary in order to have a safe margin.

6.3.2 LVDS repeater

Contrary to the high speed serial links, no repeater is used on the sFEB board for the 640 Mb/s lines and the signal is driven directly from the PAD's FPGA to the TDS inputs. Tests with actual data from PAD trigger to sFEB using 5 m tin cables and 8 m silver cables from sFEB to Xilinx's KC709 evaluation board acting as data checker showed no errors after continuous 12 hours of operation. Due to the long delivery time of the custom made 3M twinax cables (longer than 1 m) it was unable to perform tests with 6 m at that time. In Figure 6.11 the eye diagram after 5 m tin cable is presented. It is obvious that the signal degrades significantly with a eye height of 246.6 mV and width 1.362 ns.

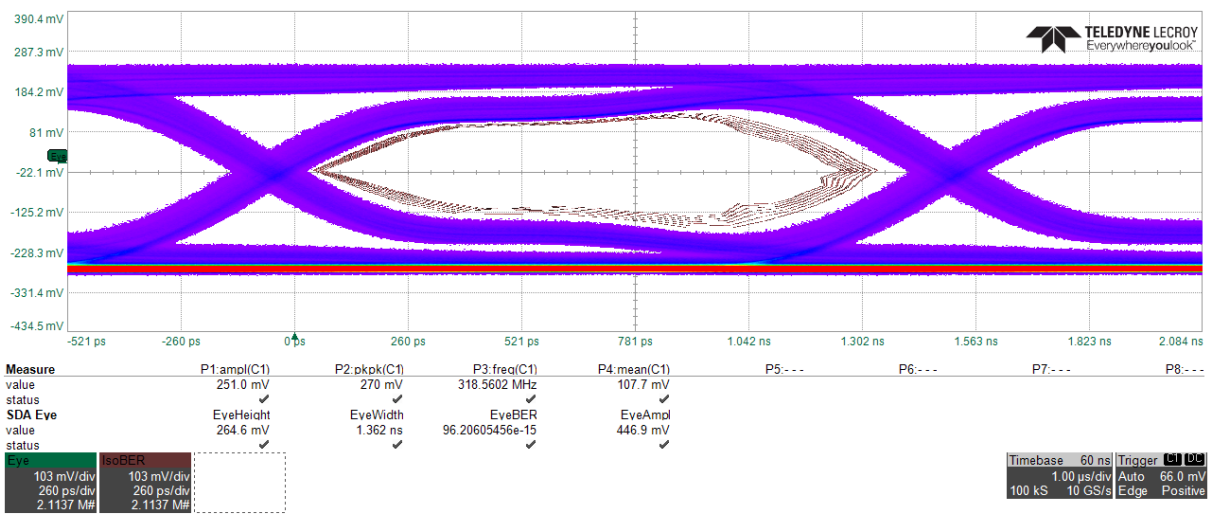
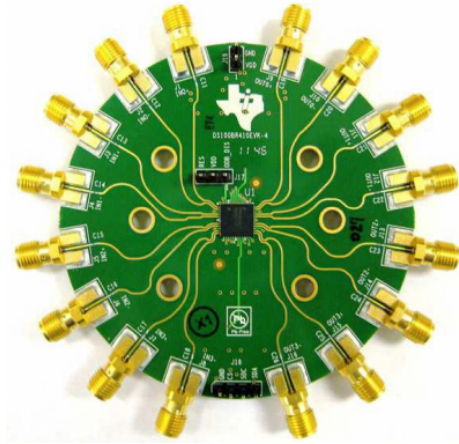


Figure 6.11: Eye diagram for 640 Mb/s data from PAD trigger with 5 m twinax cable.

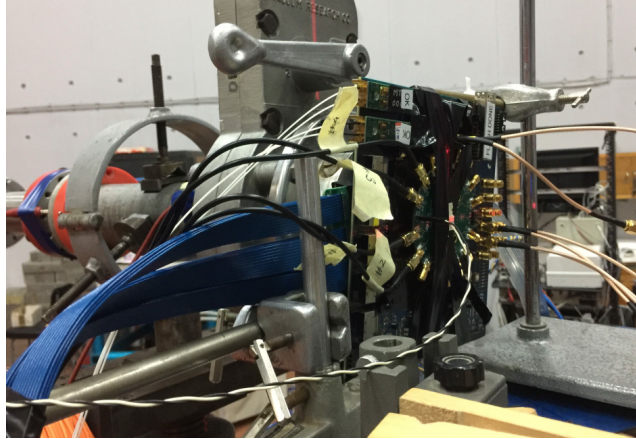
To boost the signal the SY58605 LVDS buffer by Micrel was added. This buffer has a single power supply of 2.5 V and provides less than 10 ps total jitter. It can process clock signals up to 2 GHz or data patterns up to 3.4 GHz. Input can be Current Mode Logic (CML), LVDS or Low Voltage Positive Emitter-Coupled Logic (LVPECL) and the output is 325 mV LVDS.

6.3.3 Repeater irradiation tests

The serial repeater device was tested under irradiation in Demokritos along with RIM-L1DDC (described in Chapter 5) by Riccardo Vari et al. from National Institute of Nuclear Physics (Istituto Nazionale di Fisica Nucleare - INFN) Roma. For the purpose of this test the DS100BR410EVK-4 evaluation board, shown in Figure 6.12(a) by Texas Instruments was used. PRBS data at 1.25 Gb/s generated by a Xilinx’s KC705 evaluation board were transmitted to the input channels of the repeater board and the outputs were driven back to KC705 for comparison. The KC705 board was placed 5 m away from the beam line and four 5 m SMA cables were used to transmit and receive the data from/to the repeater board. The board was placed in different distances away from the target with different fluence during the five day run as shown in Table 6.5. After 41.7 hours and a total dose of 3.15×10^{10} n/cm² no errors were monitored.



(a)



(b)

Figure 6.12: (a) Serial repeater evaluation board, (b) test beam setup.

Table 6.5: Distance of the LVDS repeater evaluation board from the target, fluence, time, neutrons and total dose.

DAY	Energy (MeV)	Distance (cm)	Fluence (n/cm ² s)	Time (s)	Neutrons (n/cm ²)
1-2	20.1	5.76	1.43E+05	50400	7.21E+09
3	20.1	4.50	2.26E+05	39540	8.94E+09
4	20.1	3.90	2.72E+05	34980	9.51E+09
5	24.0	4.97	1.11E+06	4260	4.73E+09
5	24.0	4.97	5.55E+04	20820	1.16E+09
Total				150000	3.155E+10

Conclusions

This dissertation presents the development of the three different versions of the Level-1 Data Driver Card for the micromegas and the sTGC detectors. These boards are part of the data acquisition for both detectors and will be used on the upgrade of the New Small Wheel of the ATLAS experiment at CERN. The current detectors and electronics of the Small Wheel are not able to cope with the high background hit rates and bandwidth that are expected in the future upgrades of the Large Hardon Collider. The whole readout and trigger paths for both detectors were completely redesigned. The new readout scheme is capable of reading out ~ 2.5 m channels from both detector technologies (~ 2.1 m for micromegas and ~ 300 k for the sTGC) and helped a lot the scalability of the final system.

The L1DDC board was initially designed for the non demanding Phase 1 upgrade with a single trigger rate of 100 kHz, centre-of-mass energy of 14 TeV and luminosity of $2.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. Due to the limited accessibility after the assembly of the New Small Wheel it was requested that the L1DDC should be able to handle a single trigger rate of 1 MHz which may evolve later to two-level trigger with up to 4 MHz at Level-0 and 800 KHz at Level-1 which are basically Phase 2 requirements. A detailed study for modifying the initial boards in order to be compatible even with the future upgrades of the LHC (Run 3 2021-2023 and Run 4 2026-2038) was performed. Extensive calculations showed that the extrapolated hit rates (maximum 21 kHz/cm²) of the New Small Wheel for Phase 2 and Run 3 will be increased about 31 times. These calculations are based on Run-2 Small Wheel data. The maximum bandwidth for the Level-1 data increased at 814.2 Mb/s and 1.478 Gb/s for the inner front-ends of the micromegas and sTGC detectors respectively. A new configuration was implemented to distribute equally the rates from the front-end ASICs to the four sub Read Out Controllers of the Read Out Controller ASIC and eventually to the E-Links. The maximum utilization of the E-Link for the new rates was estimated at 79.5% and 63.45% giving a sufficient margin for micromegas and sTGC detectors respectively. To support the new rates, additional components, GigaBit Transceiver ASICs, fibers connectors, differential pairs and cables were added but also the distribution and cooling schemes were revised. The optimum solution to balance between space and cost was identified. This option led also to the design of different boards for the sTGC and micromegas detectors. The L1DDC is capable of reading out up to 8.72 Gb/s of detector data and delivers them to

the back-end systems for further analysis. In total 4.46 Tb/s of produced Level-1 data will be handled by all L1DDC boards and the whole readout chain.

Reliability is one of the main concerns since after the integration of the New Small Wheel there is no accessibility for maintenance or replacement of the electronics/cables. All boards must work without failures for ten years of continuous operation. The component placement and the cooling design was also crucial since the increased temperature can reduce dramatically their life expectancy. Detector size constrains and special requirements for the placement, cooling and cable routing made the design of the boards challenging. In addition, the harsh environment inside the detector imposed the use of radiation and magnetic tolerant materials. Commercial components were tested under radiation in NCSR Demokritos's facility in Athens, Greece with maximum fluence of $4.6\text{E}+06\text{ n/cm}^2$ and total dose of $6.45\text{E}+10\text{ n/cm}^2$. These components had excellent behaviour under radiation and selected to be used on the L1DDC boards. Furthermore, all materials should comply with the CERN regulations and should be halogen free, which made the selection of the components more difficult. A custom made shield with specific thickness and alloy was produced to minimize the radiated noise by the DC-DC converter but also to avoid the growth of tin whiskers.

Noise appeared to be critical for the sTGC and RIM-L1DDC boards since can affect the output clock jitter and link stability for the transmitting trigger data. Specific layout rules were implemented to eliminate any potential noise that can increase the output clock jitter. Pi-filtering proved to be ideal and capable to remove completely the switching components of the DC-DC converter at the input of the ASICs. The inductors for the decoupling of the power planes were carefully selected and tested under a 0.4 T magnetic field in different angles. These tests showed that the 1 μH shielded inductors by Würth Electronics appear to have the smallest reduction on their inductance and used on all versions of the L1DDC boards. Bypassing capacitors with the appropriate Equivalent Series Resistance and Self Resonant Frequency values were selected. By implementing all the above, the clock output jitter was measured to be $\sim 4\text{ ps}$ for the 160 MHz and $\sim 6.4\text{ ps}$ for the 40 MHz clock. These values are similar to the specifications provided by the ASIC designers measured with a test board. The phase noise jitter of the GBTX 160 MHz clocks found to be above the phase noise mask for the 7-family FPGA transceivers which is provided by Xilinx. Extensive tests with the final setup and the actual boards showed that this clock can drive stable links at 4.8 Gb/s. Since it is not clear if the noise levels will remain the same after mounting the boards on the detector or inside the radiated area, an alternative scheme to provide a dedicated direct clock was designed and implemented. It was essential to prove that is possible to distribute a low jitter clock by bypassing completely the GBTX ASIC of the L1DDC. The new scheme comprises a jitter cleaner and a custom made board that transmits a clean clock over 100 m of multimode fiber. With the aforementioned setup the jitter was measured to be $\sim 1.2\text{ ps}$ after a 110 m fiber and the use of two couplers. Moreover, a series of tests performed to identify the phase noise mask of the 160 MHz clock that causes the link instabilities. The measurements showed clearly that the margin is at $\sim 10\text{ ps}$ which is far away from the output jitter of the L1DDC boards. All individual tests performed showed the proper behaviour and long time runs verified the reliability of the boards. Moreover extensive tests using the final prototypes and the whole readout/trigger chain,

proved the stability and proper functionality of the boards. After the green light from the reviewers during the Final Design and Production Readiness Reviews the 1056 boards are ready to launch the production.

To test and validate the various electronics and the detectors a series of boards were fabricated. These boards consist of front-ends, mezzanines, low voltage distributors, adapters and testers. The front-end boards utilize the same front-end ASIC that will be integrated in the New Small Wheel upgrade. Specific rules and recommendations provided by the designer of the ASIC were followed to minimize the noise at the input channels of the front-ends. The boards proved to have good performance and low noise even with the large sTGC chambers. Furthermore, they were used in test beams with small $10\text{ mm} \times 10\text{ mm}$ micromegas chambers and a readout of about 25 kHz per channel was achieved which corresponds to 100k events per spill or more. The boards were used mainly for the evaluation of the front-end ASIC and performance studies of the sTGC detectors but later were adapted to different experiments and setups in all over the world. Extensive tests proved that the sufficient channel input protection of the front-end ASIC is to employ steering diodes in a rail-to-rail configuration in parallel with a back-to-back Transient Voltage Suppressor diode with a Reverse Stand-Off Voltage of 3.3 V.

Bibliography

- [1] ATLAS Collaboration “*The ATLAS Experiment at the CERN Large Hadron Collider*,” Nuclear JINST 3 (2008) S08003.
- [2] ATLAS Collaboration, *Muon Spectrometer Phase-II Upgrade Technical Design Report*, Draft version 0.1, September 2017.
- [3] The ATLAS Collaboration, “*Technical Design Report*,” ATLAS note LHCC-2015-009, ATLAS-TDR-024-2015, (2015).
- [4] B. Lefebvre [ATLAS Muon Collaboration], “*Muon Spectrometer Phase-I Upgrade for the ATLAS Experiment: the New Small Wheel project*,” arXiv:1810.01394 [physics.ins-det].
- [5] K. Ntekas, *The ATLAS New Small Wheel Upgrade Project*,” JINST DOI: <https://doi.org/10.22323/1.213.0331> , 2015.
- [6] A. R. Martinez [ATLAS Collaboration], “*The Run-2 ATLAS Trigger System*,” J. Phys. Conf. Ser. **762** (2016) no.1, 012003. doi:10.1088/1742-6596/762/1/012003
- [7] F. Winklmeier, “*The ATLAS High Level Trigger Infrastructure, Performance and Future Developments*,” ATL-DAQ-PROC-2009-019, ATL-COM-DAQ-2009-053.
- [8] J. Anderson, A. Borga, H. Boterenbrood, H. Chen, K. Chen, G. Drake, D. Francis, B. Gorini, F. Lanni, G. Lehmann Miotto, L. Levinson, J. Narevicius, C. Plessl, A. Roich, S. Ryu, F. Schreuder, J. Schumacher, W. Vandelli, J. Vermeulen, J. Zhang, “*Level-1 Data Driver Card Design Review Report, FELIX: a High-Throughput Network Approach for Interfacing to Front End Electronics for ATLAS Upgrades*, May 2015.
- [9] The ATLAS Collaboration, “*Technical Design Report for the Phase-II Upgrade of the ATLAS Trigger and Data Acquisition System*,” CERN-LHCC-2017-020, ATLAS-TDR-029, (2018).
- [10] T. Alexopoulos, J. Burnens, R. de Oliveira, G. Glonti, O. Pizzirusso, V. Polychronakos, G. Sekhniaidze, G. Tsipolitis, J. Wotschack, “*A spark-resistant bulk-micromegas chamber for high-rate applications*,” , Nuclear Instruments and Methods in Physics Research A, (2011).

- [11] X. Zhao and C. Zhu, “Small-Strip Thin Gap Chambers (sTGC) for the Muon Spectrometer Upgrade of the ATLAS Experiment,” Springer Proc. Phys. **213** (2018) 129. doi:10.1007/978-981-13-1316-5_24
- [12] P. Gkoutoumis [ATLAS Muon Collaboration], “Level-1 Data Driver Card of the ATLAS New Small Wheel upgrade,” doi:10.1109/NSSMIC.2015.7581785
- [13] L. Yao, H. Chen, K. Chen, S. Tang and V. Polychronakos, “The Design and Testing of the Address in Real Time Data Driver Card for the Micromegas Detector of the ATLAS New Small Wheel Upgrade,” arXiv:1806.06912 [physics.ins-det].
- [14] L. Yao, H. Chen, K. Chen, S. Tang and V. Polychronakos, “The Design and Testing of the Address in Real Time Data Driver Card for the Micromegas Detector of the ATLAS New Small Wheel Upgrade,” arXiv:1806.06912 [physics.ins-det].
- [15] G. Iakovidis [ATLAS Muon Collaboration], “VMM - An ASIC for micropattern detectors,” EPJ Web Conf. **174** (2018) 07001. doi:10.1051/epjconf/201817407001
- [16] R. M. Coliban, S. Popa, T. Tulbure, D. Nicula, M. Ivanovici, S. Martoiu, L. Levinson and J. Vermeulen, “The Read Out Controller for the ATLAS New Small Wheel,” JINST **11** (2016) no.02, C02069. doi:10.1088/1748-0221/11/02/C02069
- [17] GBT Project, *GBTx Manual*, [Version 0.15](#).
- [18] *Component: VMM*, ATLAS NSW Electronics Specifications, **v3**, (2016).
- [19] A. Caratelli, S. Bonacini, K. Kloukinas, A. Marchioro, P. Moreira, R. De Oliveira and C. Paillard, “The GBT-SCA, a radiation tolerant ASIC for detector control and monitoring applications in HEP experiments,” JINST **10** (2015) no.03, C03034. doi:10.1088/1748-0221/10/03/C03034
- [20] T. Alexopoulos, G. Fanourakis, T. Geralis, M. Kokkoris, A. Kourkoumeli-Charalampidi, K. Papageorgiou and G. Tsiolitis, “Study of the VMM1 read-out chip in a neutron irradiation environment,” JINST **11** (2016) no.05, P05015. doi:10.1088/1748-0221/11/05/P05015
- [21] G. Mazza, A. Rivetti, P. Moreira, K. Wyllie, C. Soos, J. Troska and P. Gui, “A radiation tolerant 5 Gb/s Laser Driver in 130-nm CMOS technology,” JINST **7** (2012) C01052. doi:10.1088/1748-0221/7/01/C01052
- [22] M. Menouni, P. Gui and P. Moreira, “The GBTIA, a 5 Gbit/s Radiation-Hard Optical Receiver for the SLHC Upgrades,” doi:10.5170/CERN-2009-006.326
- [23] JEDEC STANDARD, *Scalable Low-Voltage Signaling for 400 mV (SLVS-400)*, JESD8-13, October 2001.
- [24] T. Alexopoulos, C. Bakalis, P. Gkoutoumis, G. Iakovidis, A. Koulouris, *Level-1 Data Driver Card Design Review Report*, Atlas note, Draft version 1.0.

- [25] I. P. Mesolongitis, A. Gkountis, E. D. K. Bitzaros, K. Zachariadou, P. Gkountoumis and T. Alexopoulos, “*Testing the Level-1 Data Driver Card for the New Small Wheel of the ATLAS detector*,” doi:10.1109/MOCAST.2017.7937667
- [26] M. Barros Marin, S. Baron, S. S. Feger, P. Leitaio, E. S. Lupu, C. Soos, P. Vichoudis and K. Wyllie, “*The GBT-FPGA core: features and challenges*,” JINST **10** (2015) no.03, C03021. doi:10.1088/1748-0221/10/03/C03021
- [27] T. Alexopoulos, P. Gkountoumis, G. Iakovidis, D. Lellouch, L. Levinson, S. Martoiu, V. Polychronakos, I. Ravinovich, J. Vermeulen, *Upgrading the New Small Wheel readout to handle a 1 MHz readout rate*, ATLAS note ATL-COM-MUON-2016-026, (2016).
- [28] P. Gkountoumis, “*Level-1 Data Driver Card of the ATLAS New Small Wheel upgrade compatible with the Phase II 1 MHz readout scheme*,” doi:10.1109/MOCAST.2016.7495115
- [29] The ATLAS Collaboration, “*Technical Design Report for the Phase-II Upgrade of the ATLAS Muon Spectrometer*,” CERN-LHCC-2017-017, ATLAS-TDR-026, (2017).
- [30] J. Ameel, D. Amidei, R. Edgar, M. Kravchenko, K. Sekhon, “*NSW LV Power - Radiation Testing Status*,” internal communication, (2014).
- [31] FEAST Datasheet, *Radiation tolerant 10 W Synchronous Step-Down Buck DC/DC converter*, rev1.0, (2014).
- [32] F. Faccio, S. Michelis, S. Orlandi, G. Blanchot, C. Fuentes, S. Sagginid and F. Ongarod “*Development of custom radiation-tolerant DCDCconverter ASICs*,” JINST **5** (2010) C11016
- [33] A.C. Vasko, G. R. Warrell, E. Parsai, V. G. Karpov, and Diana Shvydka, “*Evidence of rapid tin whisker growth under electron irradiation*,” Nucl. Instrum. Meth. [arXiv:1505.00822v2 [cond-mat.mtrl-sci]].
- [34] P. Gkountoumis, “*Prototype board development for the validation of the VMM ASICs for the new small wheel ATLAS upgrade project*,” doi:10.1109/MOCAST.2018.8376599
- [35] G. Iakovidis [ATLAS Muon Collaboration], “*VMM - An ASIC for micropattern detectors*,” EPJ Web Conf. **174** (2018) 07001. doi:10.1051/epjconf/201817407001
- [36] N. Atanov *et al.*, “*The Mu2e calorimeter: quality assurance of production crystals and SiPMs*,” Nucl. Instrum. Meth. doi:10.1016/j.nima.2018.10.085 [arXiv:1812.07921 [physics.ins-det]].
- [37] N. Atanov *et al.*, “*The Mu2e Calorimeter Final Technical Design Report*,” arXiv:1802.06341 [physics.ins-det].
- [38] I. Ravinovich and V. Smakhtin, “*Optimization of π -network & pull-up schemes for wires, pads and strips*,” internal communication, (2017).

- [39] K. Kurokawa, "*Power Waves and the Scattering Matrix*," vol. 13, no. 2, pp. 194-202, March 1965. doi: 10.1109/TMTT.1965.1125964

Additional boards that were designed and developed

A.1 Front-End boards

A variety of front-end boards utilizing the VMM ASIC were fabricated to readout data from a different type of detectors (MDTs, micromegas, sTGCs, CSCs and Gas Electron Multiplier-GEM) in different experiments. These boards are the MDT mezzanine, the MMFE1, the GPVMM and the mu2e. The majority of the components and functionalities are the same in all boards. The VMM ASIC requires four separate supplies for minimizing the contribution to Equivalent Noise Charge (ENC). These four power supplies are the:

- Vddp: Power for the charge amplifiers. The maximum current is 150 mA and the reference ground plane is the Vss.
- Vddad: Mixed analog-digital power. The maximum current is about 200 mA and the reference ground plane is the Vssad.
- Vdd: Power for all the other analog circuitry. The maximum current is 400 mA and the reference ground plane is the Vss.
- Vddd: Digital power including the SLVS drivers. The maximum current is 150 mA and the reference ground plane is the Vssd.

The maximum power consumption of the VMM is 1080 mW. For the power distribution a set of DC-DC converters and LDOs was used. The LT8612 Step-Down regulator has a wide input voltage range from 3.4 V up to 42 V and an output ripple of less than 10 mVp-p. The Vddp, Vdd, Vddad and the Vddd are powered by different LDOs. Five LEMO connectors provide access to: MO, PDO, TDO (described in Section 1.4.1), a LVTTTL output signal for the ART and a Transistor Transistor Logic (TTL) input signal for the trigger. The new version of the VMM (VMM3) integrates the SLVS standard which is not supported by the Artix-7 FPGA and thus Xilinx's DIFF_HSUL_12 differential standard was used. This standard provides the lower common mode voltage (0.6 V)

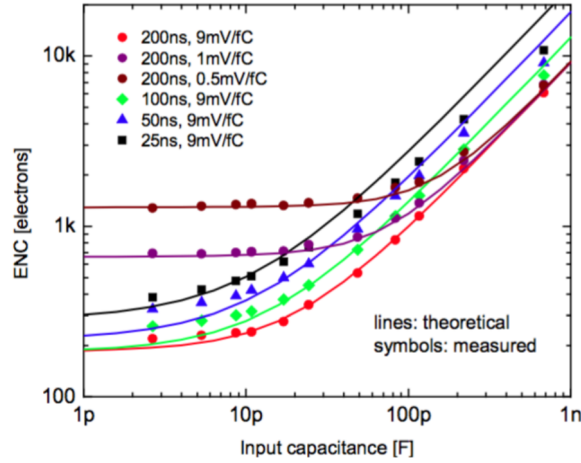


Figure A.1: Equivalent Noise Charge of the VMM for different capacitances.

comparing to all other standards and proved to be fully compatible with the SLVS. The FPGA banks which are interfacing with the VMM are powered on with the required 1.2 V. The FPGA is accessible through a standard JTAG connector for programming and monitoring. The configuration file for the FPGA is stored in a non-volatile 256 Mb quad SPI FLASH (Part Number: N25Q256A13EF840E) by Micron. The Quad SPI bus provides access to the read/write commands of the FLASH memory. For the Ethernet interface Marvell's 88E1111-B2-BAB1C000 Ethernet PHYSical layer (PHY) was used which achieves a 10/100/1000 Mbps Ethernet. Communication with the software is established by using the UDP/IP protocols and all configuration parameters for both VMM and FPGA are set by the corresponding Graphical User Interface (GUI). Finally a six position Dual In-line Package (DIP) switch and seven user Light Emitting Diodes (LED) provide extra flexibility to the user if needed.

Internal layers were mainly used to route the input signals to the VMM and the traces on the top-bottom layers were minimized. Moreover, those traces were shielded by the power planes for the input transistors on top and bottom layers. Cutouts in the analog ground planes adjacent to the VMM input signals were implemented to minimize the parasitic capacitance. In Figure A.2 the cutouts with green color and the tracks for the input channels are visible. Separation of at least 762 μm (30 mil) was used for the analog and digital ground planes and there is no overlapping between them.

For the readout of the boards a (GUI) called VMM Ethernet Readout Software (VERSO) was deployed. VERSO is based on the Qt independent platform and uses the Ethernet interface and UDP/IP protocols for the communication with the FE boards. With this software is possible to configure the VMM ASIC, set the FPGA parameters, readout and store the VMM data in ntuples for further analysis.

A.1.1 MDT mezzanine boards

The MDT boards (436 and 446) were developed and proposed to be used as the new readout scheme for the future upgrades of the MDT detectors. The difference between the two boards is the orientation of the connectors that are plugged on the detector (the

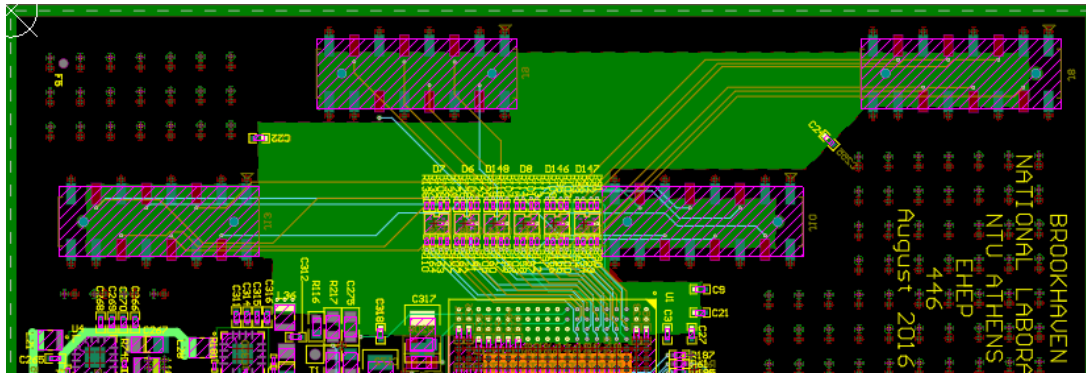


Figure A.2: *Input signals of the VMM ASIC on the MDT Mezzanine boards.*

connectors are actually mirrored). The part number of the connectors is the SSM-108-L-DV compatible with the MDT chambers. The dimensions of the boards are 110 mm \times 113 mm. The MDT 436 is presented in Figure A.3(a) and the 446 in Figure A.3(b). Each MDT mezzanine is connected to 24 MDT tubes and thus only 24 channels (0 to 23) are utilized at the VMM ASIC. Channel 24 is connected through a 1 pF capacitor and a voltage divider to a LEMO connector for the input trigger as shown in Figure A.4(a). The same input is connected to the 3.3 V Bank 14 of the FPGA through a voltage divider. The input was assumed to be TTL and the resistor values were calculated accordingly. An additional LEMO was used as alternative input for an external signal to channel 25 of the VMM.

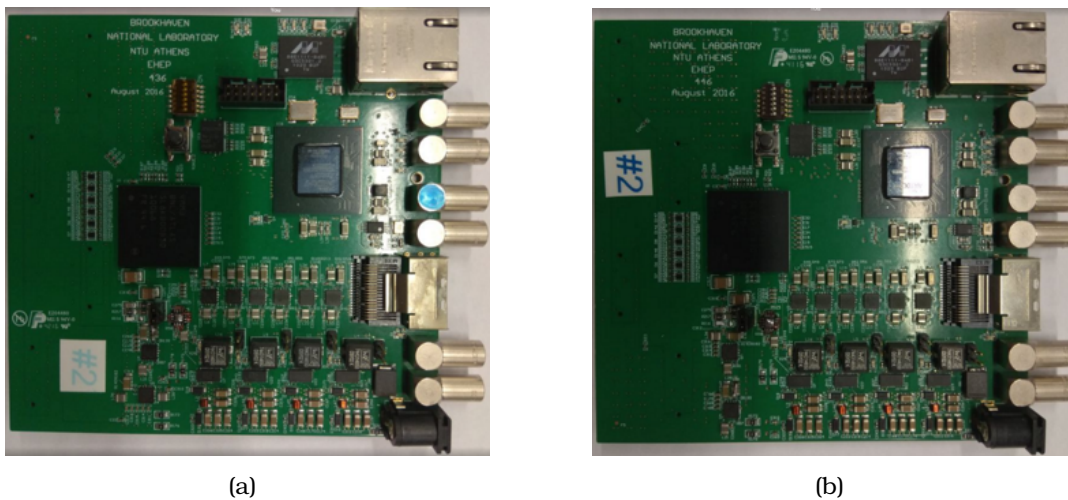


Figure A.3: The MDT (a) 436 board and (b) 446 board.

The Artix-7 FPGA by Xilinx was selected and a miniSAS connector was used as an alternative routing path for the data. The purpose of the Ethernet interface was basically for developing purposes and there was not any plan to be used in the final system. The main idea for scaling up the readout chain (by using multiple MDT mezzanines) was to use the GBTX ASIC and the whole GBT infrastructure.

The board was designed with eight layers and special layout rules were followed

in order to minimize the noise on the input channels of the ASIC. Analog and digital ground planes were split to avoid any digital noise interference with the sensitive analog electronics. Special consideration was given also to avoid any overlapping of digital and analog planes between the layers. The different ground planes were interconnected at a single point by using 0 Ohm resistors. For the VMM ASIC the via to pad technique was used and low Equivalent Series Resistance (ESR) bypassing capacitors were placed directly to the pads of the VMM.

The four power inputs of the VMM (Vdd, Vddp, Vdad and Vddd) were powered by different LDOs and decoupled by using shielded inductors. Moreover pi-filters were used at the outputs of the DC-DC converters and the LDOs in order to minimize any potential unwanted noise. A significant amount of bypassing capacitors with various capacitances, ESR and resonant frequencies were used in each power rail. Tantalum capacitors with a 1000 μ F capacitance were used to reduce instances of current spikes or starvation in the power supply rails acting as a storage. An Electro-Static Discharge (ESD) protection circuit was implemented at the input of each channel of the VMM. This circuitry includes the SP3004 diode array along with two 10 Ohm resistors as shown in Figure A.4(b).

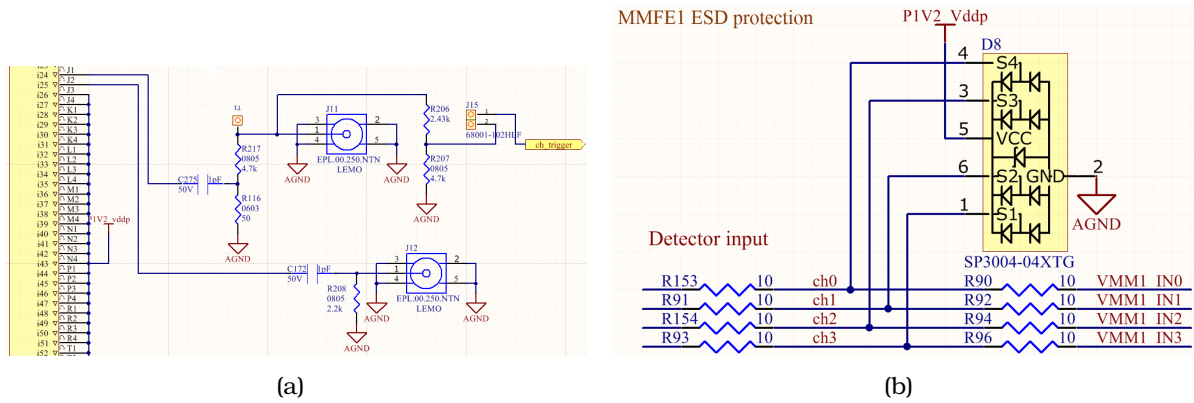


Figure A.4: (a) VMM input trigger scheme, (b) SP3004 protection circuit.

MDT mezzanine boards were tested with cosmic rays with an MDT-BIS chamber of 48 tubes in building 188 at CERN. The setup is presented on the left of Figure A.5. The two mezzanines (436 and 446) are mounted on the BIS chambers with 24 channels each. A power supply was used for powering the FEs and a fan for cooling. A scintillator was providing the trigger and the readout of the boards was implemented via Ethernet and a laptop running VERSO software. On the top-right of Figure A.5 the inputs channels of the VMM after internal pulsing is illustrated, with a number of damaged channels and with many events on channel 24 which was used as the trigger input. The number of hits for each channel is shown on bottom-left of Figure A.5 with the boards mounted on the chambers.

MDT Mezzanine and VMM3 were also used for efficiency studies of the full size sTGC prototype Module-1. The latter was found to be about 100 % efficient with cosmic and X-Rays at high rates.

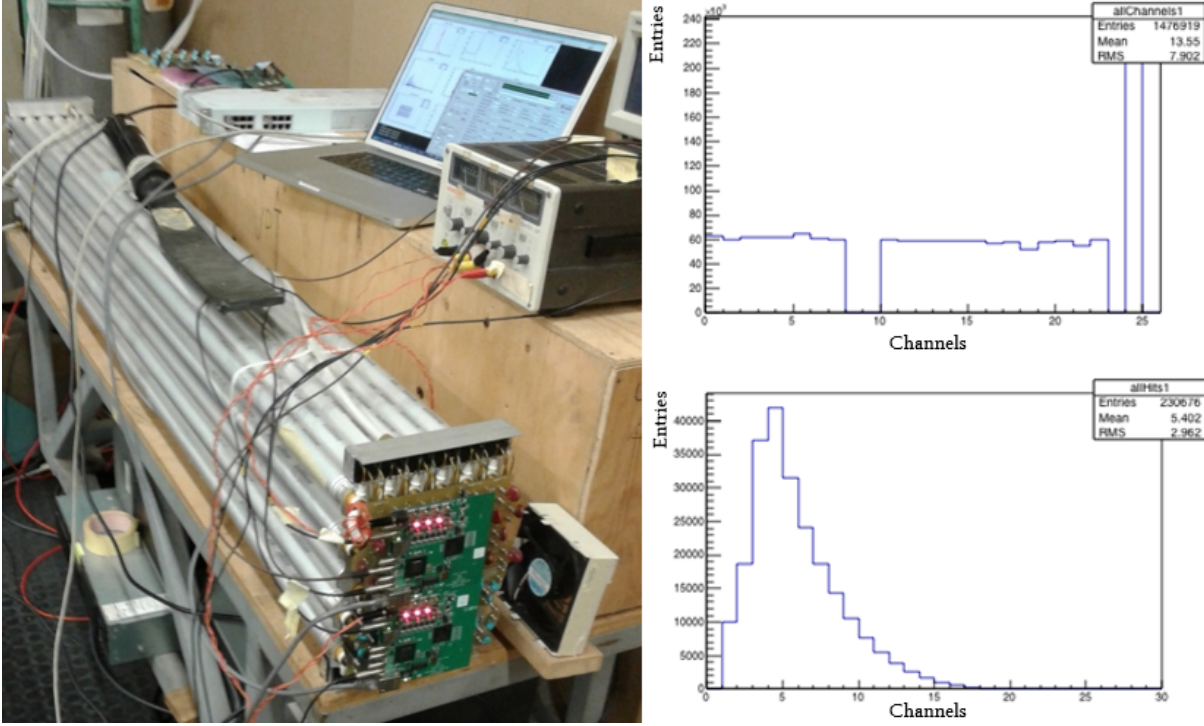


Figure A.5: Left: The MDT 436 and 446 boards mounted on a MDT-BIS chamber of 48 tubes. Right-top: VMM entries using TP and right-bottom: Number of hits.

A.1.2 MMFE1 board

To validate the functionality of VMM3 ASIC with small $10\text{ cm} \times 10\text{ cm}$ micromegas prototype chambers the MMFE1 board was fabricated. To eliminate the design/layout time and also to avoid any potential errors that can increase the debugging process of the board, the layout of the MDT boards were used as reference. In order the MMFE1 to be compatible with the micromegas chambers the the 130 pin Panasonic female connector (Part Number: AXK5SA3277YG) was selected. A second 32 Kb Electrically Erasable Programmable Read-Only Memory (EEPROM) with part number: CAT24C32WI-GT3 was used to store the media access control (MAC) and Internet Protocol (IP) address of the board. This gives the capability of the dynamic reconfiguration of the board which is useful if multiple boards are used over the same network. The access to the specific EEPROM is implemented through the I²C protocol. The power consumption of the board is about 6.5 W in full operation and the board dimensions are $117.73\text{ mm} \times 109.47\text{ mm}$. Later the SP3004 diodes and the protection circuitry of the MMFE1 proved to be inefficient to protect the channel inputs of the VMM. For that reason a more robust protection scheme was used on the new version of the board as it is described in the next section.

For additional noise suppression coming from the power supplies on the input LV line of the board, a common mode choke by TDK Corporation (part number: ACM9070-701-2PL-TL01) was used. This choke is useful for suppression of electromagnetic interference (EMI) and radio frequency interference (RFI) from power supply lines and for prevention of malfunctioning of power electronics device. It passes differential currents

(equal but opposite), while blocking common-mode currents. An extra uHDMI connector was used as alternative interface for the clock, trigger and reset signals. A mini Serial Attached Small Computer System Interface (SCSI) (miniSAS) connector is also used for interfacing with the L1DDC board. By using the L1DDC board it is possible to utilize the exact readout scheme that was designed for the upgrade of the NSW.

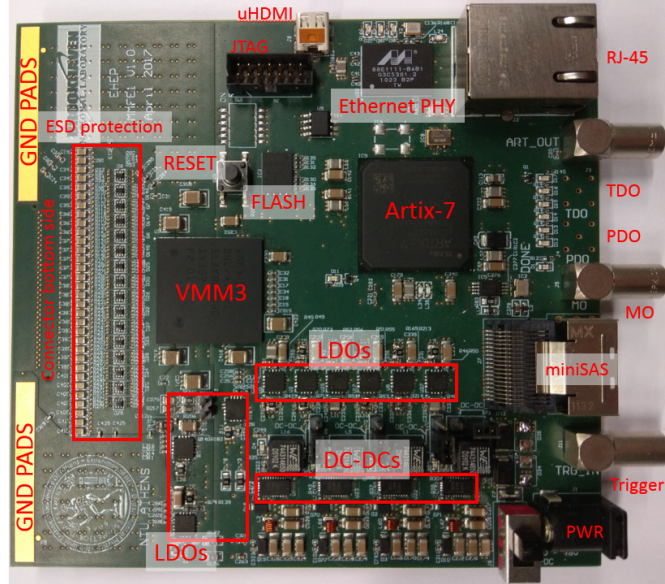


Figure A.6: The MMFE1 board.

The MMFE1 boards were tested with T and TLP ($10\text{ cm} \times 10\text{ cm}$) resistive strip micromegas prototype chambers with 1D readout at the CERN beam facilities. T chambers are prototype micromegas with strip width of $300\text{ }\mu\text{m}$ and strip pitch of $400\text{ }\mu\text{m}$. The TLP chamber is a T-type detector with a strip pitch of $400\text{ }\mu\text{m}$ and strip width of $320\text{ }\mu\text{m}$, split in two parts with different pillar shapes. Main goal was to evaluate VMM3 with the use of micromegas detectors and find any potential issues that need to be corrected before the submission of the next version of the ASIC. The coincidence from three scintillators was used to provide the trigger to the boards. The setup of the test beam is shown in Figure A.7. On the left side of the picture the MMFE1 boards mounted on the T and TLP detectors are visible along with the GEM telescope on the center and the Small Module prototype-0 (SM2) micromegas on the right.

By using the FPGAs internal XADC is possible to measure the baseline voltage and noise for each channel. Figure A.8(a) depicts the baseline and Figure A.8(b) the noise measurement for each channel of the VMM when the MMFE1 board was placed on the T chamber. The mean value of the baseline for the specific VMM was measured to be 170 mV and the mean value of the noise 1.456 mV . Three channels of the VMM ASIC showed much lower noise indicating probably a non-good connectivity to the detector.

A readout of about 25 kHz per channel was achieved which corresponds to 100 k events per spill or more. A typical beam profile taken by the T chamber is illustrated in Figure A.9(a). It is obvious that two channels (9 and 48 with no entries) were damaged while others (eg 46) showed higher noise. Cluster multiplicity is presented in Figure A.9(b) with the peak at three strips. For perpendicular to the detector plane

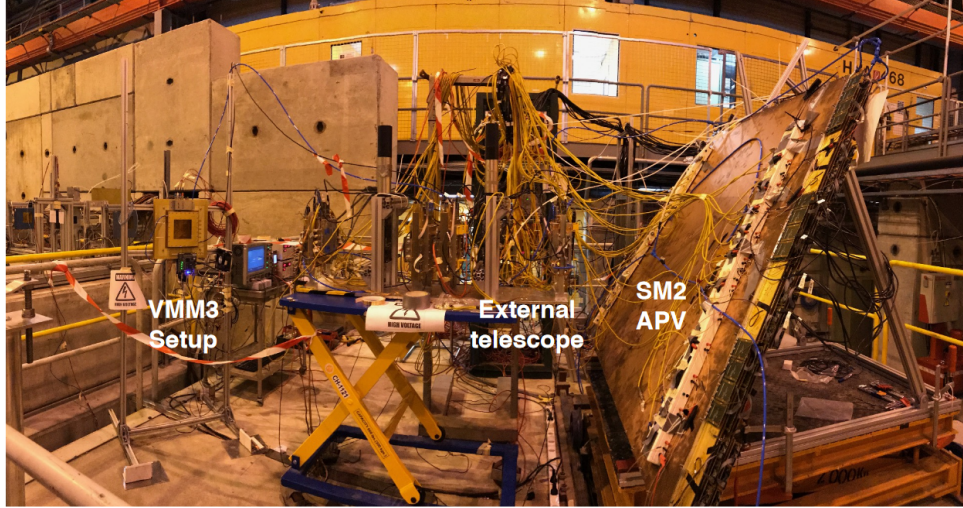


Figure A.7: Test beam setup.

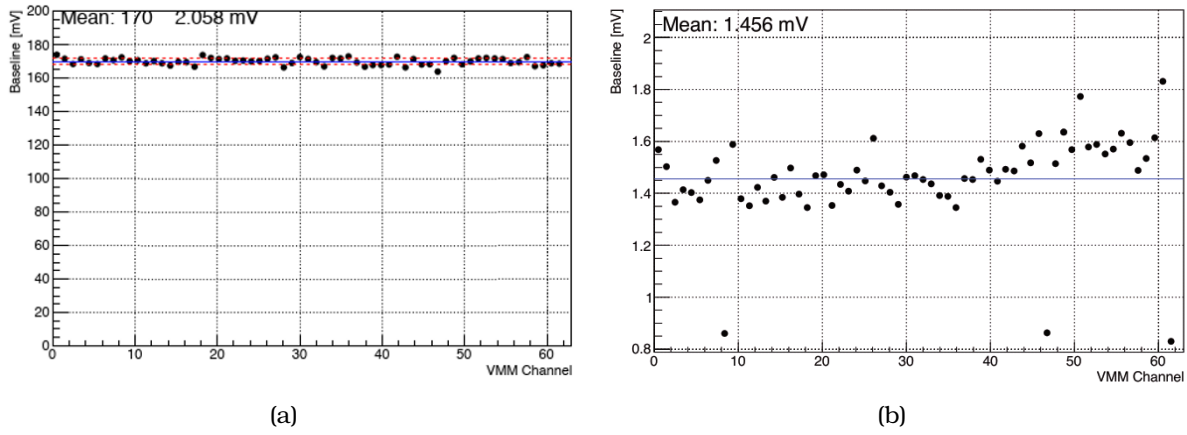


Figure A.8: VMM channel measurements with the MMFE1 plugged on the T chamber. (a) baseline scanning, (b) noise scanning.

tracks a spatial resolution has been measured at $64\ \mu\text{m}$, as shown in Figure A.9(c) and for inclined tracks (30°) at $108\ \mu\text{m}$, as shown in Figure A.9(d) [35].

A.1.3 MMFE1 wire bonded board

After the fabrication of the VMM3a ASIC a few issues were identified. Up to that time it was unclear if the issues were related to the packaging process, to the fabrication of the die itself or to the wafer position. To answer this question the MMFE1 board was modified to house the die instead the packaged VMM3a. Due to the small pitch of the wire bonded footprint and the high density of the board blind vias with diameter of $254\ \mu\text{m}$ (10 mil) and hole size of $127\ \mu\text{m}$ (5 mil) for layers one and two were used. Since the wire programming was already defined due to previous wire bonding process of other boards, only fourteen input channels were connected to the VMM. Moreover six direct outputs and the CK6B clock, necessary for the transmission of those signals,

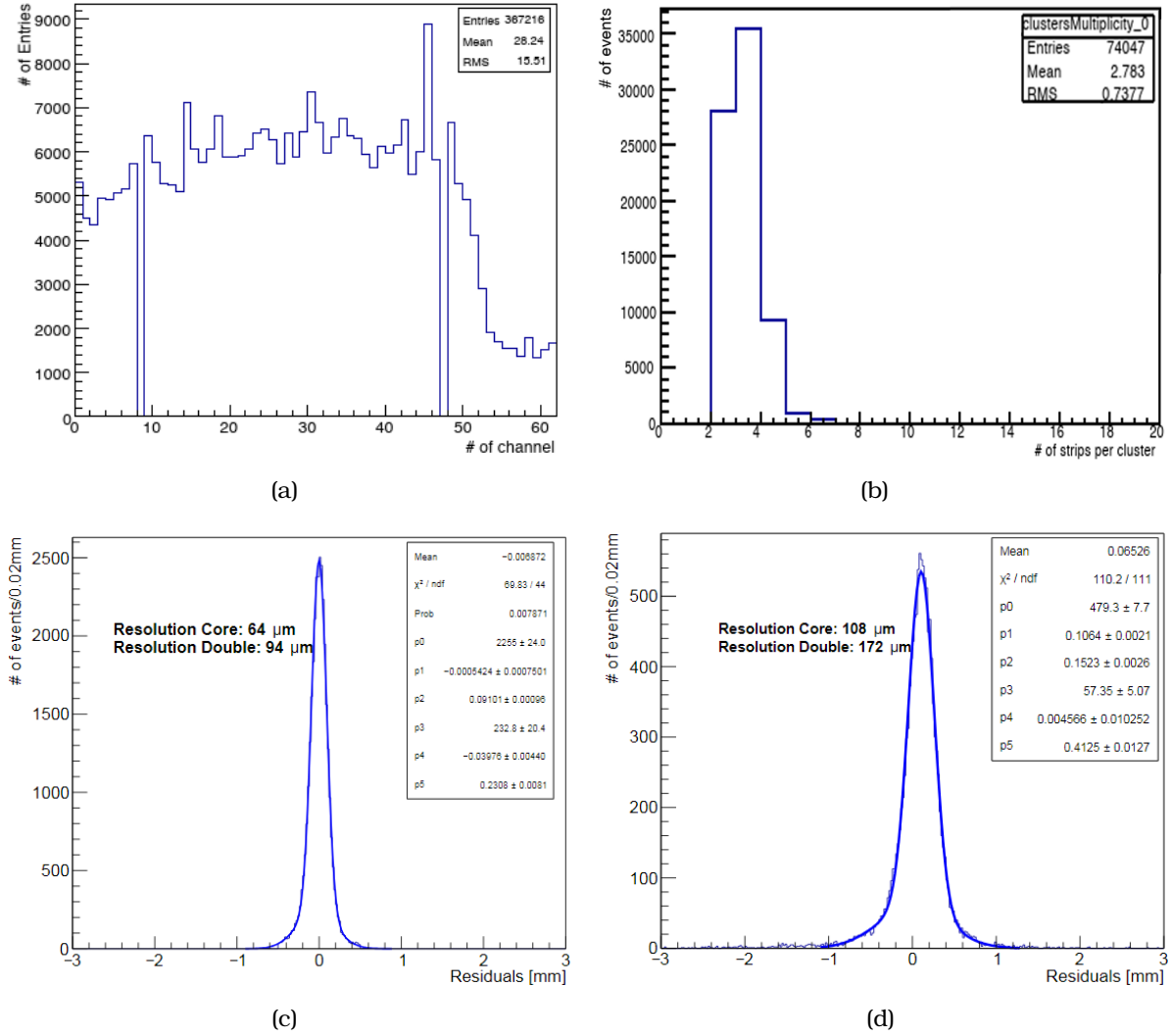


Figure A.9: (a) Beam profile, (b) Cluster multiplicity, (c) Residual distribution for perpendicular to the detector tracks and (d) Residual distribution for inclined tracks under (30°).

were connected to the FPGA. In total, ten wire bonded boards were designed, fabricated and assembled in May 2018. Due to the complexity, difficulty and limited available machinery for the wire bonding only three boards produced with the VMM die. The wire bonded process of the VMM dies took place in Brookhaven National Laboratory.

Some of the issues identified in VMM3 ASIC are:

- The missing codes of the 10-bit and 8-bit ADCs shown in Figure A.11(a).
- The equalization problem of the channel threshold range. Figure A.11(b) shows the dynamic range of the trimmers for each channel where it is obvious that a unique value for all channels cannot be defined.
- Some channels appeared to have high baseline in higher gains (eg Gain of 9 mV/fC and 12 mV/fC) as is clearly illustrated in Figure A.11(c).

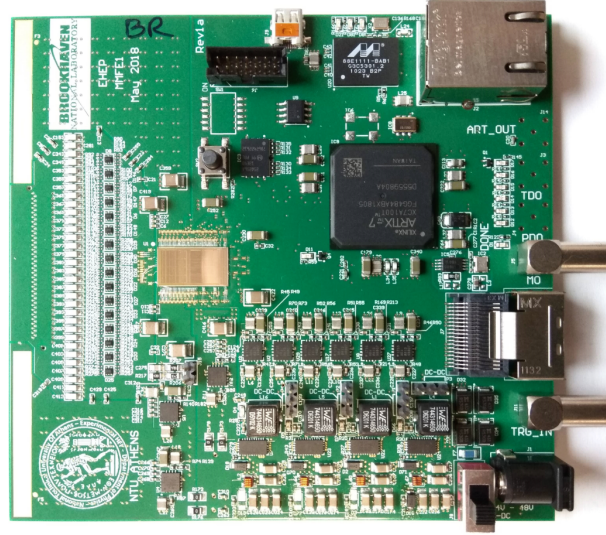


Figure A.10: *The wire bonded MMFE1 board.*

- Positive channel issue. It proved that VMM could not readout positive pulses when it was configured at positive polarity.

A.1.4 GPVMM board

A second board, more handy and robust to the chamber discharges, the GPVMM, was designed and fabricated. To keep the same low noise levels with the MMFE1 board, the same design, layout rules and stackup were used. Board was extended by a few millimetres (new dimensions: 132.84 mm × 117.35 mm) in order to house the new protection scheme. A more flexible, three row connector from TE Connectivity (part number: 9-1393644-1) with a standard 2.54 mm pitch was used to interface with various detector types. GPVMM board is shown in A.12. Additionally, due to the lack of space twelve direct outputs of the VMM were driven to a 1.27 mm DIP header. A diode network can be used as an alternative way to power on the MMFE1 and is possible to eliminate any noise introduced by the switching frequency of the DC-DC converters. In this case the input voltage must be 3.5 V and the selection is made by a two-point switch. Xilinx's XC7A100T-2FGG484C FPGA proved to be the ideal solution balancing cost and functionality as it is relatively inexpensive and has enough resources, fulfilling the requirements of the board.

These boards along with MDT Mezzanines were basically used for performance studies of the full size sTGC prototypes (Module-0) in Weizmann Institute of Science, in Israel by Ilia Ravinovich et al. Noise levels driven by MO output were measured for both pad and wires of the sTGC detectors and for different gains.

In Figure A.13 the noise measurements of the wires for 3 mV/fC gain and 200 pF wire capacitance are presented. The standard deviation of the distribution is proved to be proportional to the gain. In Figure A.14 the noise measurements of the pads for 3 mV/fC gain and 200 pF effective capacitance (after a pi-network) are presented. In this case, noise is not proportional to the gain and is close to the theoretical limit (2000 e)

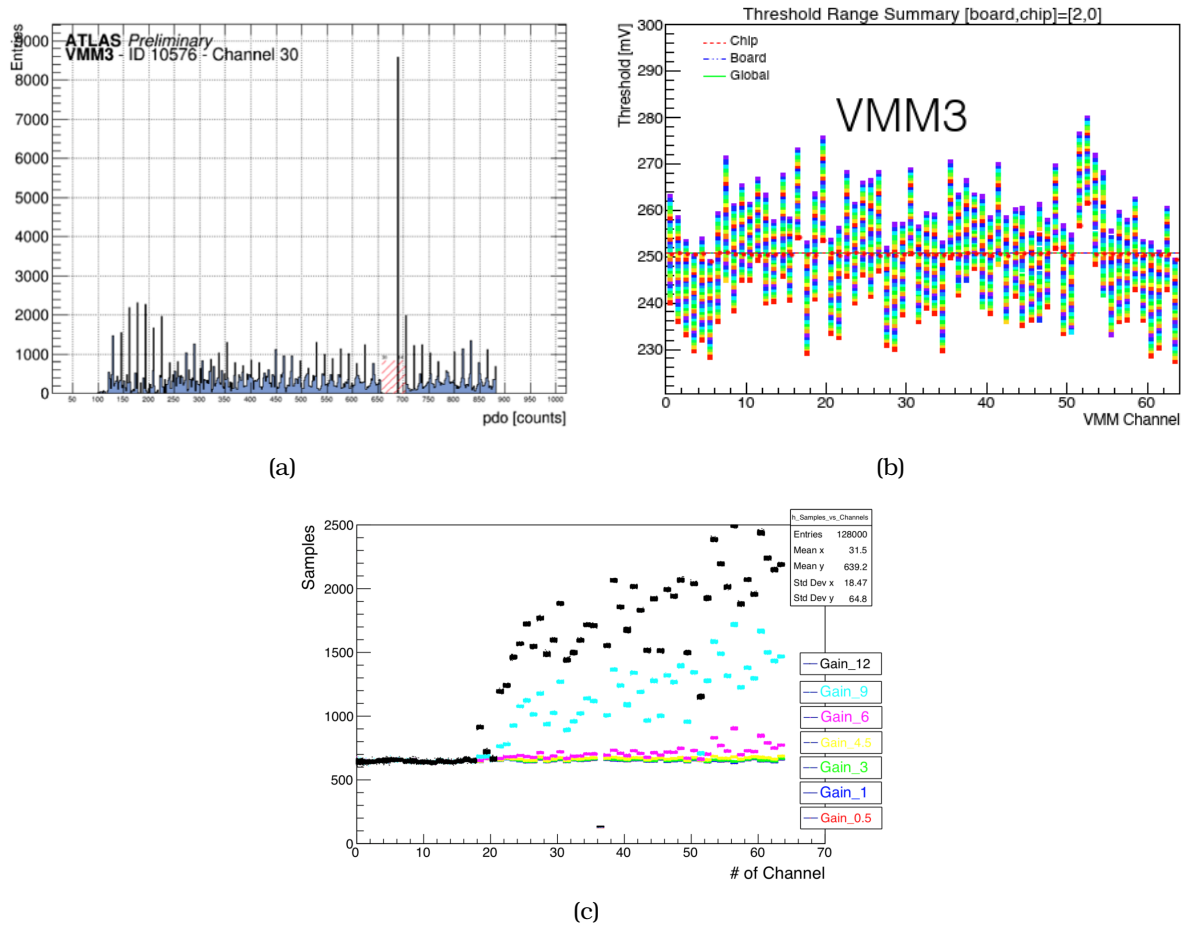


Figure A.11: (a)VMM missing codes, (b)Trimmer dynamic range, (c) High baseline issue.

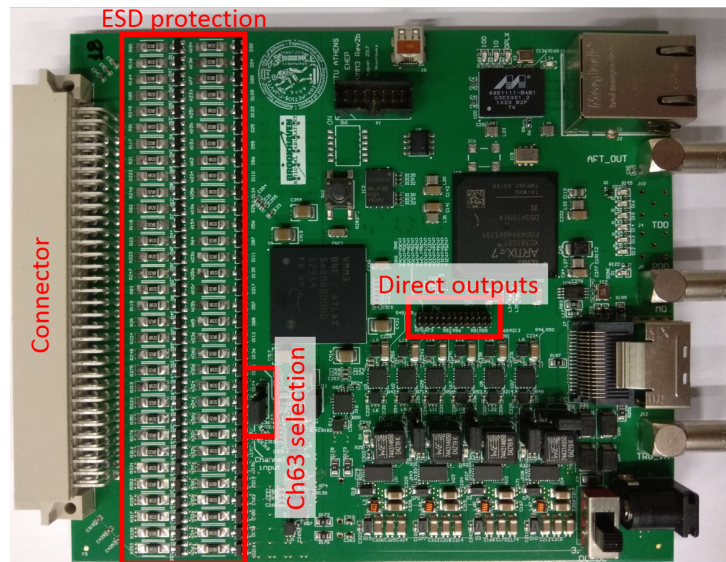


Figure A.12: The GPVMM board.

with 100 pF input capacitance.

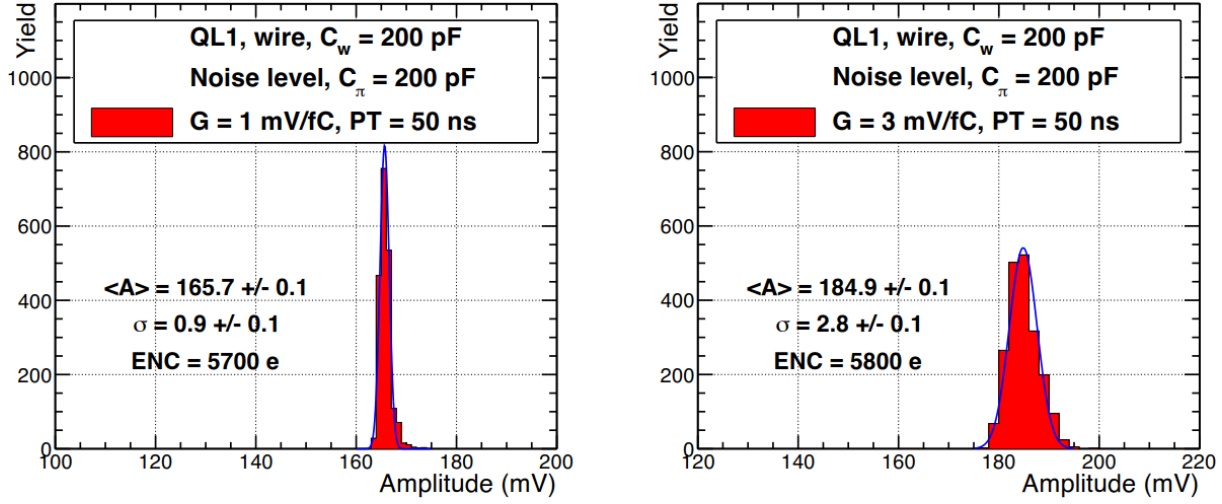


Figure A.13: Noise of the GPVMM board mounted on the sTGC detector [38].

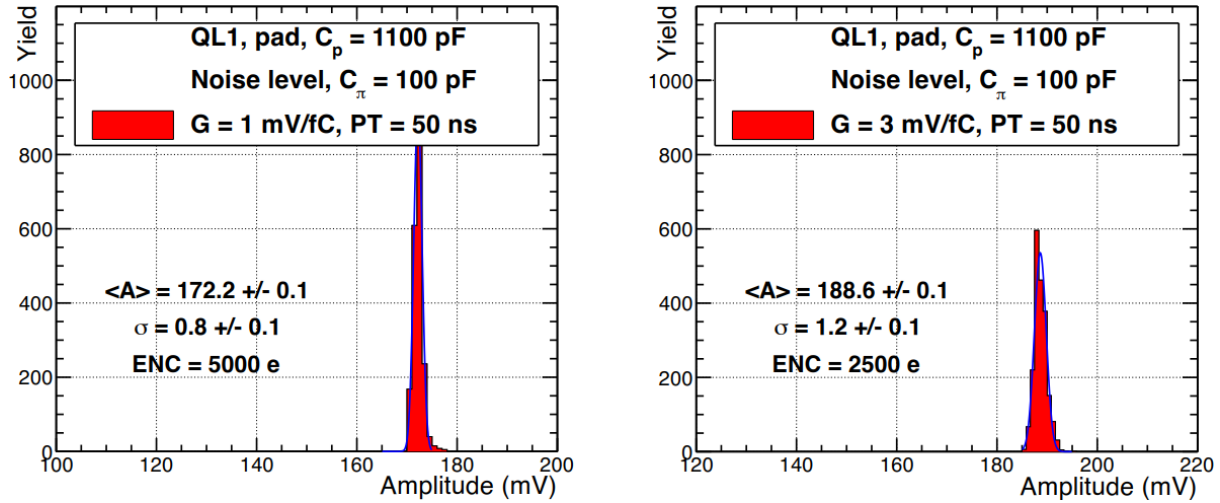


Figure A.14: Noise of the GPVMM board mounted on the sTGC detector [38].

Furthermore a series of tests for the protection of the input circuitry of the VMM showed that an additional Transient Voltage Suppression (TVS) diode should be used. The protection scheme of Figure A.15, derived from Cathode Strip Chambers (CSC) technology, was used in the GPVMM board. A pull-up resistor was also used for the bias of the input positive pulses.

Full size prototype Module-0 (QL1) chamber equipped with three GPVMM boards connected to nine wires groups, 16 pads and 30 strips through adapter boards.

A.1.5 mu2e board

This board was designed for the Muon-to-electron experiment [36, 37] in Fermilab. This experiment searches for the conversion of a muon to an electron in the field of

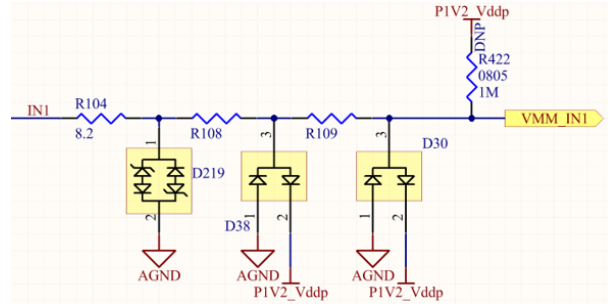


Figure A.15: GPVMM input protection diagram. *IN1* is the signal coming from the connector and *VMM_IN1* is the signal connected to the VMM.

an Aluminum atom improving by four orders of magnitude all previous sensitivities on this kind of Charged Lepton Flavor Violating process. The experiment consists of three super-conducting solenoids containing the production and the stopping target, the tracker and the electromagnetic calorimeter and an external system used to veto cosmic rays. The calorimeter helps the tracker in the identification of converted electrons (CE), building an efficient trigger and improving the track reconstruction efficiency.

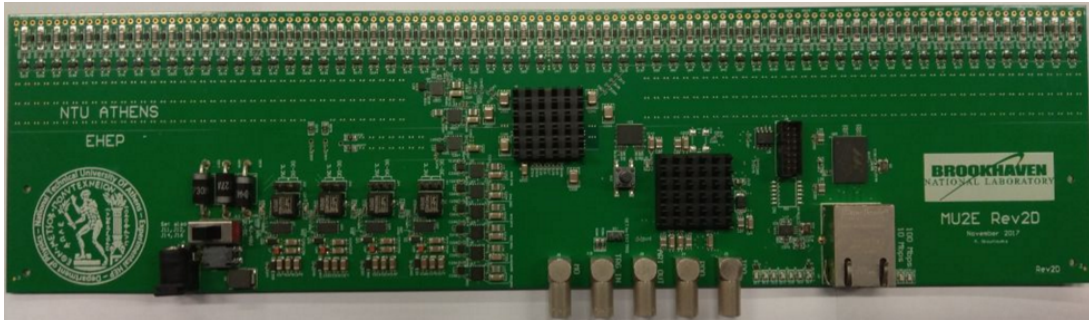


Figure A.16: The *mu2e* revision 2D FE board.

The board has 64 input channels using a 2.54 mm pitch DIP header. On the connector side there is also a ground pin in between channels. This is the reason why the board was forced to be 330.07 mm × 84.94 mm. The same stackup (eight layers) and rules of the MDT mezzanine board were used. To avoid damaging the VMM input channels the CSC protection scheme that was described in Section (A.1.4) was implemented. The *mu2e* Revision 2D board is presented in Figure A.16. On the top side of the board the 2.54 mm header and the protection scheme, on the left and bottom side, the power connector and the switch for the input selection are visible. Above the switch the diodes for the direct input and on the center-left the four DC-DC converters. On the center and top the VMM, center-right the Artix-7 FPGA and on bottom the five LEMO connectors. On the right the Ethernet PHY and the RJ45 connector are also visible.

Five boards of the first prototype (Version 1.0) were designed and fabricated in August 2016. The boards were extensively tested and were fully functional. A delamination problem was identified after the assembly process caused by the FR4 material selected by the fabrication company. On the next prototype (Rev2D) the High-Tg FR4 material was used. A few modifications performed on the second prototype:

- A second EPPROM for storing permanently the IP/MAC address of the board was added.
- Bulk tantalum capacitors were added for the VMM ASIC.
- The smaller grade Artix-7 FPGA (XC7A100T-2FGG484C) was used.
- The CSCs protection scheme for the input channels of the VMM was implemented.
- A direct diode network to bypass the DC-DC converters was also added. The selection is performed by an additional two-position switch.
- A fuse and common mode choke were integrated for protection and noise reduction respectively.
- The miniSAS connector was considered useless and was removed.

35 boards were fabricated in November 2017. All boards were functional and extensively tested.

A.1.6 FE firmware development

To test the functionality of the FE boards a firmware should be developed for the Artix-7 FPGA. The firmware was designed to be common for all FEs including MMFE8 boards. The configuration and the DAQ of the VMM implemented using a personal computer running VERSO software and Ethernet and UDP protocol. For the MMFE8 board the initial idea was to configure the eight VMMs with the same configuration. Thus the configuration data received by the FPGA were buffered to local registers and transmitted to one or more VMMs. Later it was decided to send individual packets for every VMM and the registers removed. This simplified the logic and reduced also the available resources. The selection of the number of VMMs to be configured was specified inside the UDP packet. VMM2 and VMM3 have different configuration protocols. The VMM2 configuration process utilizes five signals the Enable (ENA), Write Enable (WEN), Token CLock (CKTK), Data In (DI) and Data Out (DO). Configuration registers are only accessible when VMM is in configuration mode (ENA low and WEN high). In total 1616 bit should be transmitted on the DO line every falling edge of the CKTK clock. From the 1616 bits the 80 are used for configuration of the global registers and the rest for the channel registers (24-bit per channel). After implementing a full configuration, the written bits are available at the DO output for daisy chain configuration or for validation (bit corruption after SEUs). The configuration process for VMM2 is illustrated in Figure A.17.

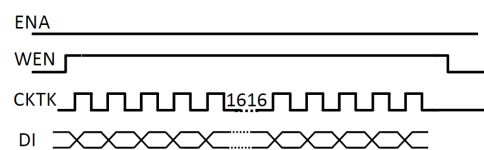


Figure A.17: VMM2 configuration diagram.

The configuration process was modified in VMM3 to be similar to Serial Peripheral Interface (SPI) protocol. This time the configuration mode is enabled by having the ENA signal low and the Chip Select (CS) low. When the VMM is in the configuration mode, the ASIC registers are accessible through the SPI clock SCK and data inputs SDI. The data transmitted are shifted at the falling edge of SCK in groups of 96-bits and latched when the CS is high. The first two bunches of 96 bits (192 bits) are used for the configuration registers and the rest eighteen (1536 bits) for the channel registers. This means that the total number of bits for the configuration registers increased to 1728. As in VMM2 data of the configuration registers are available at the SDO output lines for daisy-chain configuration or for validation. For multiple VMM configuration SDI, SDO and SCK lines are common but using individual chip select pins. Tri-stated logic is implemented and high impedance is used for the VMMs that are not selected. The timing diagram of the VMM3 configuration is shown in Figure A.18.

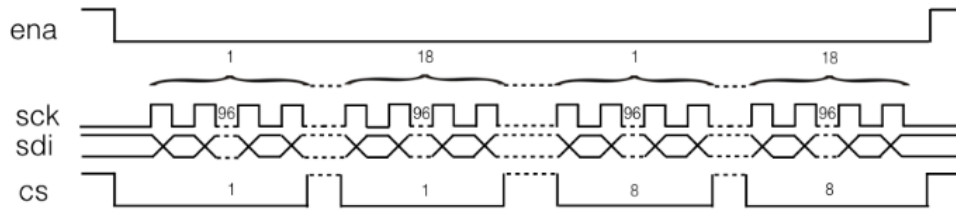


Figure A.18: VMM3 configuration diagram.

The communication with the Verso firmware is implemented by using Ethernet and UDP protocol as was described in section 6.2.2. The only difference is that instead of the 1000Base-x the Serial Gigabit Media Independent Interface (SGMII) was used, since the communication is implemented with an external PHY chip. A flow FSM was used to control the transitions of the different states of the firmware (IDLE, Configuration, DAQ). For the VMM readout the continuous mode was initially implemented. After the readout the data from one or multiple VMMs are transmitted to the FPGA where they are encapsulated in packets with the appropriate format and transmitted to GUI via Ethernet.

A.2 Low voltage distributor board

One main concern for the proper functionality of the micromegas on-detector electronics was the low voltage distribution and grounding. Thus, the Low Voltage Distributor Board (LVDB) was designed to power the MMFE8s, ADDC and L1DDC boards. The LVDB board has twelve two pin Nano-Fit connectors (two for powering the L1DDC and two the ADDC) and two five pin high current power connectors (molex, part number: 172310-1105) rated for 14 A per contact for receiving the power from the Intermediate Conversion Stage (ICS). Each ICS channel is capable of providing 16 A (maximum) via two pair shielded low voltage cables (16 AWG). The output voltage is adjustable depending on the drop of the cables with a possible value being the 10 V. Due to the different LV cable lengths of the FEs, ballast resistors were used for the equalization of the return currents and to avoid any ground loops. Since the digital electronics are less

sensitive to noise, no ballast resistors were used for the ADDC and L1DDC boards. The power from the LVDB will be distributed to the MMFE8/ADDC/L1DDC with a two pair cable of 0.13 mm^2 cross-section. One ICS channel/LVDB will power on the four upper MMFE8s of the first plane and the four upper MMFE8s of the second plane. Accordingly, a second LVDB will power on the upper eight MMFE8s of plane three and four. For the ADDC/L1DDC boards, the two pairs of an ICS channel will be split and driven to different LVDB boards. With this scheme, all L1DDCs and ADDCs of the one side of the quadruplet (four micromegas planes) will be powered on by one ICS channel. The ICS and LVDB distribution diagram for the micromegas detector is illustrated in Figure A.19. The shields from the ICS cables along with the shields of the on-detector electronics are tied to the ATLAS safety ground at the LVDB board with the use of 3.5 mm plated through holes. On the on-detector electronics side the shields of the low voltage cables are left floating.

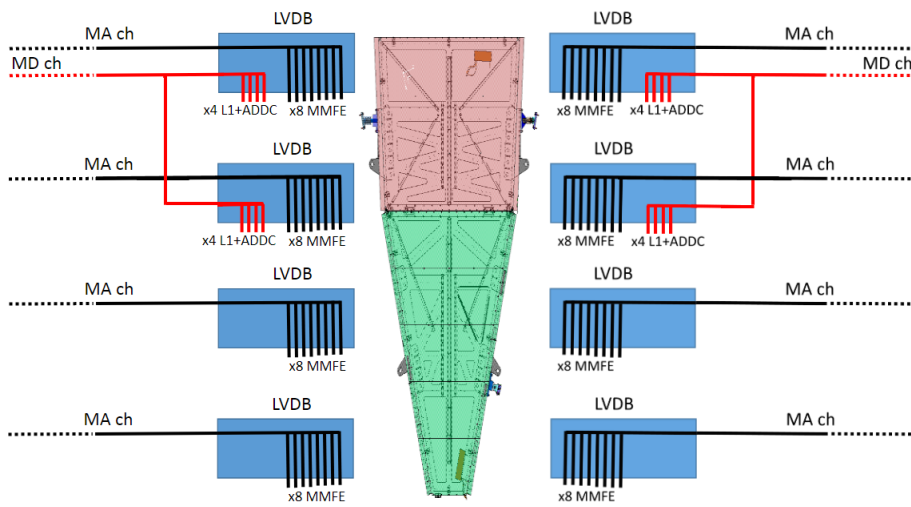


Figure A.19: ICS and LVDB distribution diagram.

Ten LVDB boards (Version 1.0) were designed and fabricated in October 2018. The top side of the board is illustrated in Figure A.20 where the Nano-Fit connectors for the four ADDC/L1DDC and eight MMFE8 boards are shown on the top left and top right respectively. In the middle the two five pin power connectors for the interconnection with the ICS channels and the plated holes for the cable shield, along with the ballast resistors are visible. The board was designed with two layers and the dimensions are $200 \text{ mm} \times 60 \text{ mm}$.

The LVDB boards will be placed on the first and fourth plane of each wedge and especially on the second and seventh micromegas PCB (outer and inner positions of the wedge). L1DDC and ADDC boards will be connected only to the outer LVDBs (PCB seven). This will minimize the length of the thin 0.13 mm^2 cables (from LVDB to on detector electronics) and subsequently the voltage drop. This cable corresponds to a American Wire Gauge (AWG) of 26 with about $134 \text{ m}\Omega$ per meter. The maximum current of the MMFE8s is about 1.15 A in full operation and thus the voltage drop of the cables is calculated at about 154 mV per meter. Since the resistance is calculated per wire, the drop is doubled per meter for both power and ground cables. With the

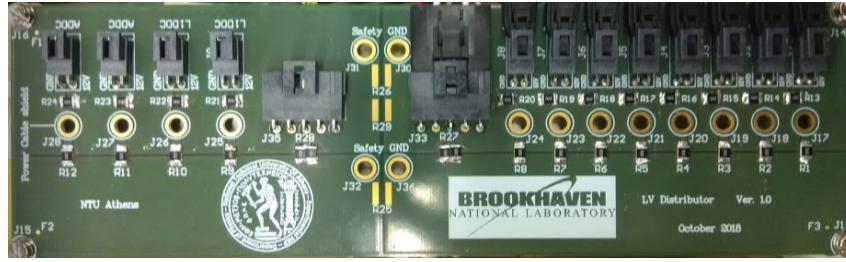


Figure A.20: The Low Voltage Distributor Revision 1 Board.

Table A.1: Low voltage drop that was measured on the LVDB and MMFE8 boards.

PS voltage	LVDB (6 m)	33 cm	45 cm	63 cm	82 cm	116 cm	124 cm
11 V	10.28 V	10.14 V	10.08 V	10.08 V	10.04 V	9.88 V	9.83 V
10 V	9.2 V	9.03 V	8.98 V	8.97 V	8.94 V	8.71 V	8.75 V

new configuration the maximum length was measured at about 1.2 m. All voltage levels and drops were measured at the input of the eight MMFE8 and LVDB boards. A 6 m 16 AWG cable was used to provide the power to LVDB from a commercial power supply and various lengths of the 0.13 mm² cable were used. During the measurements all MMFE8 boards were powered on and configured while they were consuming the maximum power consumption of 1.15 A. From the results presented in Table A.1 the maximum drop at 1.24 cm is 1.25 V.

The inrush current for the two ICS channels was measured using a current probe. For the eight MMFE8s the maximum value is 13.3 A as is shown on the left of Figure A.21 and for the four ADDCs and four L1DDC is 6.31 A as is shown on the right of Figure A.21. Both values are lower than the ICS 16 A capability.

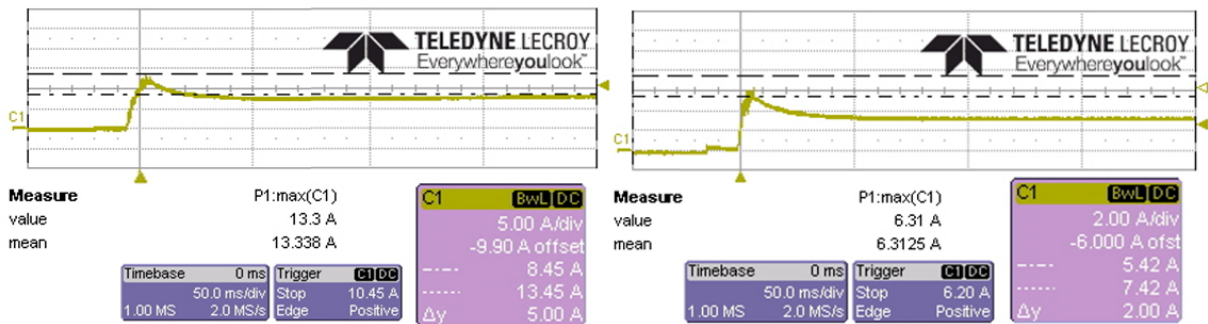


Figure A.21: Inrush current. Left: for the eight MMFE8 boards, Right: for the four ADDCs and four L1DDC boards.

In case of over-current due to a short on the cables or boards, the drawn current can reach the maximum limit of 16 A and the ICS will kill the specific channel. Up to this point ADDC and L1DDC utilize 1 A (Part No: 0435001.KR) and 3 A (Part No: 0435003.KR) fuses respectively for over-current protection of the FEASTs. On the other hand MMFE8 boards due to the limited space they don't use fuses. The overheating protection of the FEAST can prevent any further damages in case of a short on the

board. If the short is on the cables or at input circuit of the FEAST then high current will flow through the cables and there is a risk of fire. If the current consumption exceeds the ICS trip limit then the specific channel will be disabled. Thus all the MMFE8s connected to the specific channel will be powered off. To reduce the failure of multiple MMFE8s fuses will be used also for each MMFE8 on the LVDB board. Moreover, it was decided to replace all fuses located on the L1DDC and ADDC boards with a single one at the LVDB board. Resetable fuses seem to be ideal but since there is no proof that are radiation tolerant they were finally rejected.

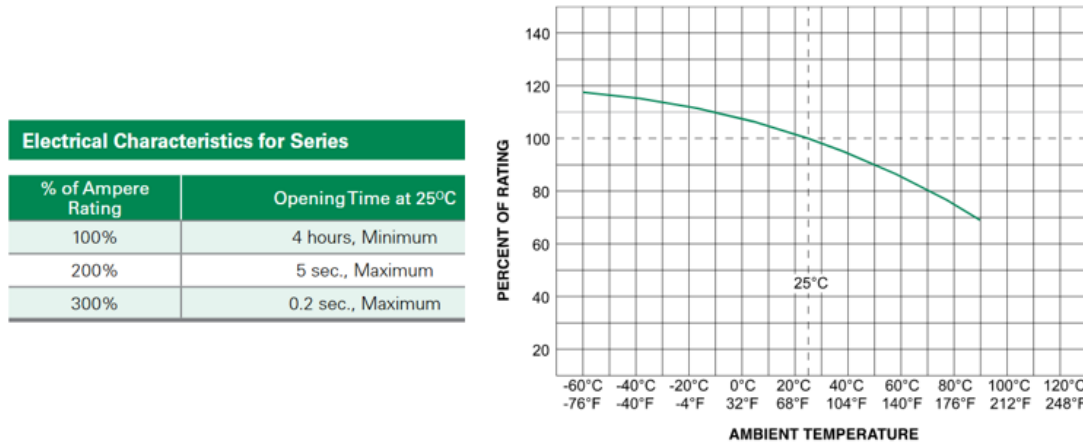


Figure A.22: Left: fuse electrical characteristics, right: Temperature rerating curve.

The fuse candidate for the LVDB is the 0467003.NRHF by LitteFuse with a current rating of 3 A, DC/AC voltage rating of 32 V and a 0603 footprint. This fuse was tested by the FEAST group under magnetic fields and radiation up to 100 Mrad. The electrical characteristics of the fuse are presented on the left and temperature rerating curve on the right Figure A.22. The specifications for the ICS to trip is less than 1 s for the overcurrent (> 16 A) and 0.1 s for the overvoltage. To prevent ICS from tripping the fuse must blow at less than 1 s which corresponds to 300% of ampere rating (9 A).

During the integration tests on the micromegas chamber it was proved that the usage of a plated hole to mount the shield of the voltage cable was impractical, especially for the LVDBs placed on the 4th plane. Thus, it was decided to replace the two pin molex nanofit connectors with three pin ones, where the third pin will be used for the shield wire. To reduce any potential noise coming from the ICS a common mode choke was placed at the input side of the MMFE8 boards. The only available commode mode choke with 18 A and relative small size (with height less than 10 mm which is the envelope constrain) is the PLT10HH450180PNL by Murata Electronics North America. This component has a current rating of 18 A, an extremely low DC Resistance of 1.8 m Ω and voltage rating (DC) of 300 V.



Figure A.23: A 2-port network.

The performance of this component is evaluated by the Insertion Loss (negative gain). For a generic multi-port network a_i is the incident and b_i the reflected "power wave" [39]. In our case which is a 2-port network (shown in Figure A.23) the complex linear gain is given by the:

$$G = S_{21} = \frac{b_2}{a_1}$$

where S_{21} is the forward voltage gain. The scalar linear gain (or linear gain magnitude) is given by

$$|G| = |S_{21}|$$

This value represents the gain magnitude (absolute value), the ratio of the output power-wave to the input power-wave, and it equals the square-root of the power gain. In case the two measurement ports use the same reference impedance, the insertion loss (IL) is the magnitude of the transmission coefficient $|S_{21}|$ expressed in decibels. It is thus given by:

$$g = -20 \times \log_{10}|S_{21}|$$

which is basically the extra loss produced by the introduction of the device under test (DUT) between the two reference planes of the measurement.

The S_{21} parameter of the PLT10HH450180PNL common mode choke is presented in Figure A.24(a). The loss in the range of 1 to 10 MHz (frequency range that MMFE8 and VMM are susceptible) is relatively low (-0.43 dB at 1 MHz and -5.42 dB at 10 MHz). Another option is to use a different common choke for each MMFE8 output line. Minimizing the current rating (1.15 A in full operation and ~ 1.6 A inrush current for the MMFE8) a huge variety of available common mode chokes was available. The part that was finally selected is the ACP3225-501-2P-T000 by TDK. This component has a current rating of 2 A, a DC Resistance 40 m Ω , a voltage rating (DC) of 60 V but also a very low price in large quantities. The S_{21} parameter of the ACP3225 common mode choke is presented in Figure A.24(b). This choke has a much better behaviour compared to PLT10HH450180PNL with -1.2 dB at 1 MHz and -14.12 dB at 10 MHz.

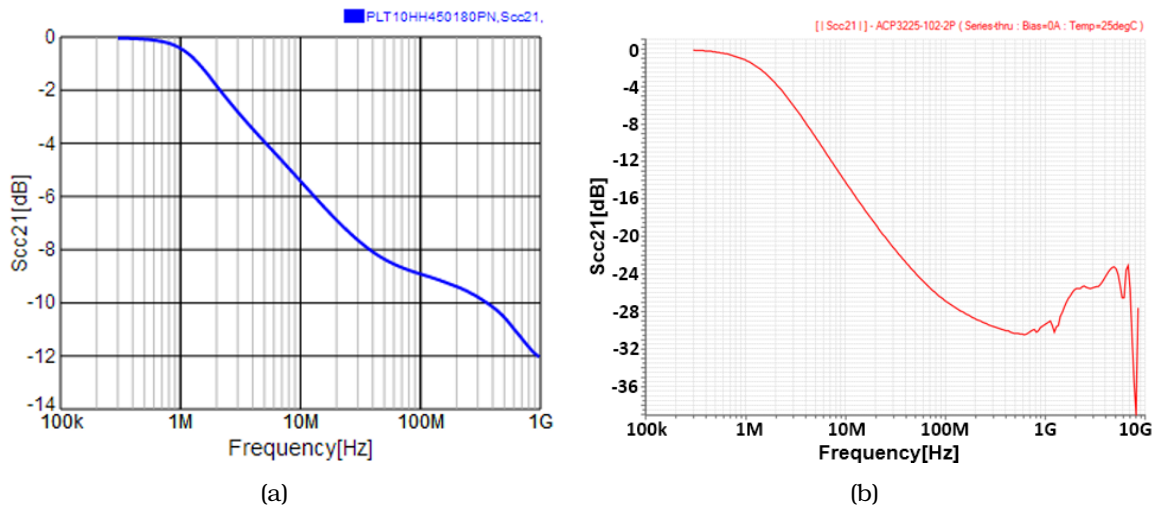


Figure A.24: The FMC miniSAS mezzanine.

A.3 Mezzanine and adapter boards

A.3.1 FMC to miniSAS mezzanine

To test and validate the L1DDC boards a proper setup had to be designed. All L1DDCs have a maximum of nine miniSAS connectors and three fibers. In order to be able

to test one L1DDC board at a time a FMC mezzanine, compatible with the VC709 evaluation board from Xilinx, was fabricated. This passive board has nine miniSAS connectors and the pinout is fully compatible with all versions of L1DDC boards. In total 81 differential pins are routed to this twelve layer mezzanine. The layer stackup is the same with sTGC-L1DDC and the two board were fabricated using the same PCB panel to reduce the overall price. All differential pairs are connected to an 1.8 V bank of the Virtex-7 FPGA. Ten mezzanine boards were designed and fabricated in total. No errors identified and all boards are fully functional and are used at the testing sites of the L1DDC board. The top side of the board is shown in Figure A.27(a) and the pinout that was used for all miniSAS connectors in Figure A.27(b).

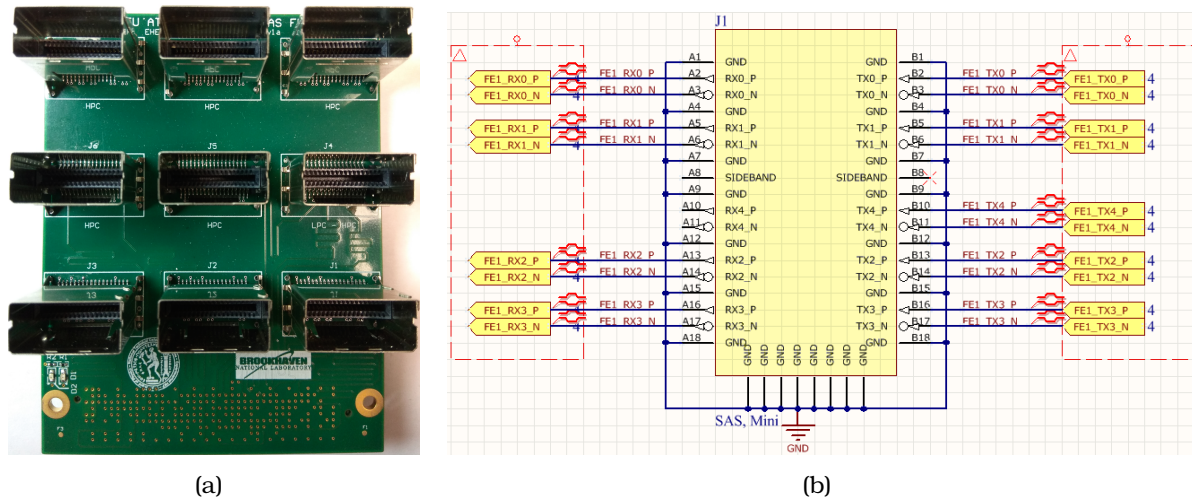


Figure A.27: The FMC miniSAS mezzanine.

A.3.2 miniSAS to SMA adapter

For the evaluation of the output signals of the L1DDC boards a conversion of the signals from miniSAS to SMA cables was required. For this reason was designed and fabricated the miniSAS-to-SMA adapter board. It is a simple board consisting of only two layers and has one miniSAS and 18 SMA connectors. All differential pairs and sidebands are utilized. The miniSAS-to-SMA board is illustrated in Figure A.28.

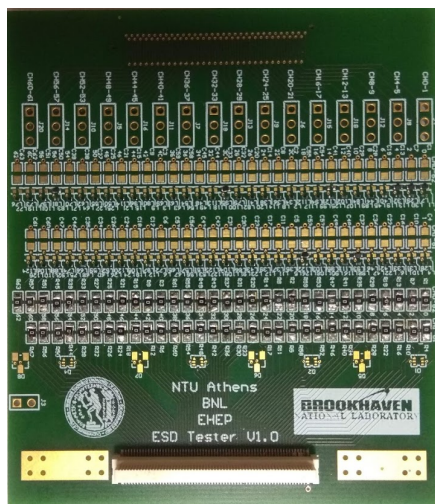
VMM tester

The protection scheme that was used initially for the MMFE1 board and all the FE boards of the NSW appeared to be inadequate to protect the input channels of the VMM. The alternative protection of the GPVMM boards is robust but consumes a lot of space on the board. To find the optimum solution the VMM tester board was developed. It utilizes a male Panasonic connector and multiple footprints (0201, 0402, 0805) as shown on the left of Figure A.29. This board was attached to the MMFE1 and gave the opportunity to test large number of protection diodes.

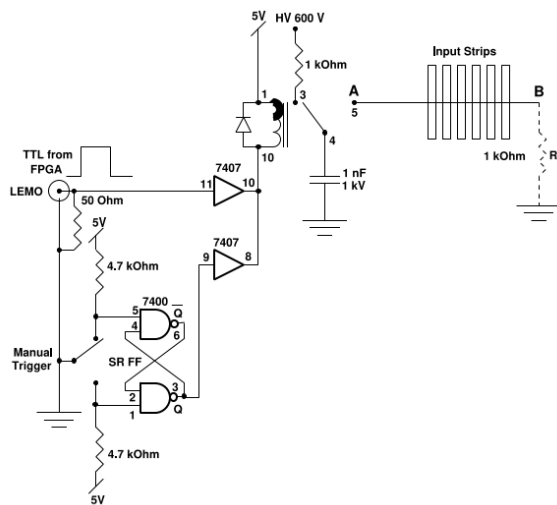


Figure A.28: miniSAS to SAM breaker board.

With the use of a simple circuit it was possible to charge and discharge a 1 nF, 1 kV capacitor at the input channel of the VMM, just before the protection scheme. To open and close the switch a push button is available but also a relay driven by an external signal for continuous operation. The schematic diagram of the circuit is shown on the right of Figure A.29. With the protection scheme of the MMFE1 was able to kill the channels, even with a single discharge. By adding a back to back TVS diode channels survived even after more than 30,000 discharges.



(a)



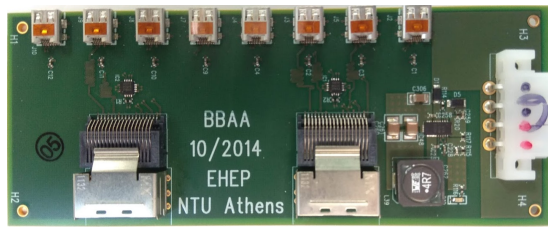
(b)

Figure A.29: (a) Protection diode tester board. (b) Schematic diagram of the discharge circuit.

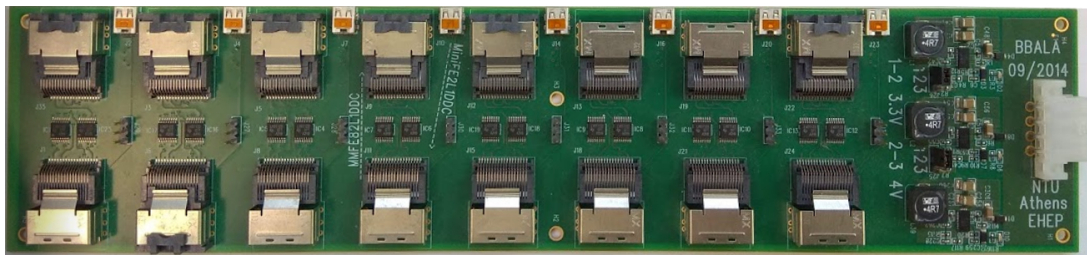
The 0201 uClamp 3311p protection diode by Semtech appeared to be ideal for this purpose. The uClamp is a Transient Voltage Suppressor (TVS) and is designed to protect sensitive semiconductor components from damage or upset due to electrostatic discharge (ESD), lightning, electrical fast transients (EFT), and cable discharge events (CDE).

Adapter boards

During the early period only small $10\text{ mm} \times 10\text{ mm}$ prototype micromegas chambers were available for data taking. The RD51 group at CERN developed a simple FE board called mini-2, which is compatible with those chambers. The board contains two VMM ASICs, a SPARTAN-6 FPGA by Xilinx and a few LDOs. It utilizes two micro-HDMI connector to receive the power at 3.3 V and to transmit the data. The one connector is used for the trigger data to ADDC and the other for the VMM data to L1DDC. To convert the signal from the micro-HDMI to miniSAS connectors, two boards were designed and fabricated: the Brookhaven Bucharest ADDC Adapter (BBAA) for the ADDC and the Brookhaven Bucharest Arizona L1DDC Adapter (BBALA) for the L1DDC. The BBALA



(a)



(b)

Figure A.30: Adapter boards:(a) BBAA for ADDC, (b) BBALA for L1DDC.

has micro-HDMI connectors and miniSAS from the one side (FR side) and the signals from both connectors are routed in the same miniSAS connector of the other side (L1DDC side). With this scheme both mini-2 and MMFE8 can interface with L1DDC but never using the same micro-HDMI/miniSAS pair. In total eight miniSAS and eight micro-HDMI connectors were used giving the opportunity to the L1DDC to interface with eight mini-2 FE boards.

It was also unclear if the FPGAs of both MMFE8 and mini-2 boards were capable of receiving correctly the SLVS signals that were transmitted by the GBTX ASIC of the L1DDC. For that reason CML to LVDS translators were used. This conversion is unidirectional with the direction of the miniSAS side to the miniSAS/micro-HDMI side. A three pin DPI header for every micro-HDMI connector gives the ability for external configuration of the mini-2 FEs through a standard I²C protocol. Finally the BBALA has a power distribution circuit in order to provide the power supply to mini-2 through the micro-HDMI connectors. The power is selectable between 3.3 V and 4 V in case there is a voltage drop caused by longer micro-HDMI cables (test beam option). To power on the board the LT8612 DC-DC converter, described in Section 2.2 was used.

BBAA aggregates the four trigger input signals (from eight VMMs) into one miniSAS connector. In total eight micro-HDMI connectors and two miniSAS were used on the BBAA board. CML to LVDS translators were also used for the transmitted signals of the ADDC board. The overall scheme is shown on the left of Figure A.31. Eight mini-2 are connected to one L1DDC board and one ADDC board. Red arrows indicate the trigger path, blue arrows the data path and orange the configuration data.

It was also essential to deploy a system that can communicate with the first prototypes of the L1DDC boards for testing purposes. A FMC board with five micro-HDMI connectors designed and fabricated at CERN was utilised. This FMC board was mounted on a ML605 evaluation board by Xilinx. To convert the signals from the micro-HDMI to miniSAS and to transmit data from ML605 to L1DDC and vice versa, the BBALA adapter board was also used. The setup is shown on the right of Figure A.31.

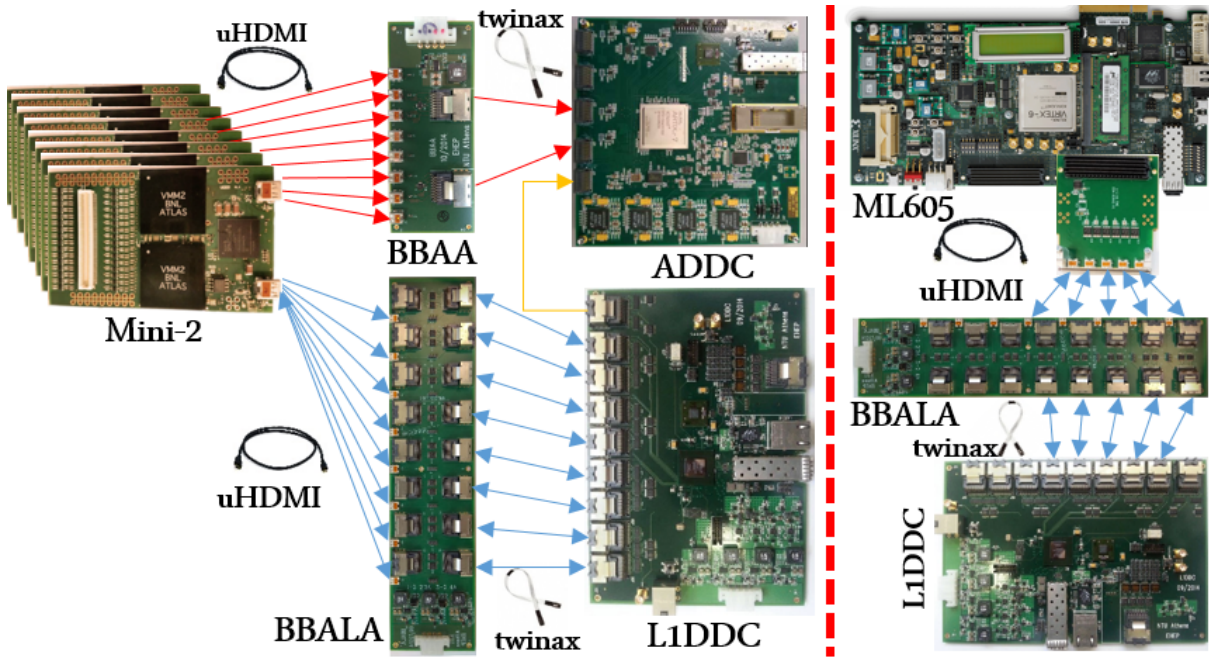


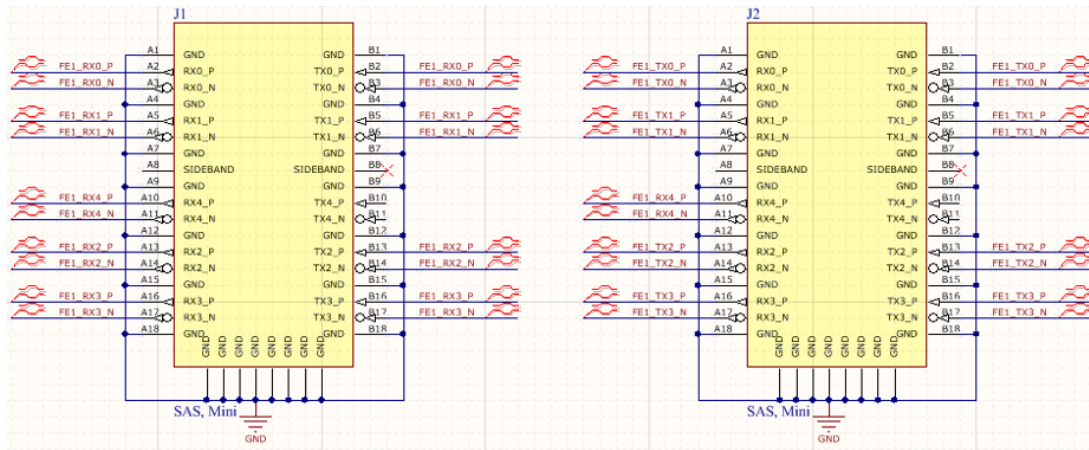
Figure A.31: Left: Old readout and trigger chain for micromegas detectors. Right: Initial testing setup for L1DDC prototype-1.

Twinax terminator

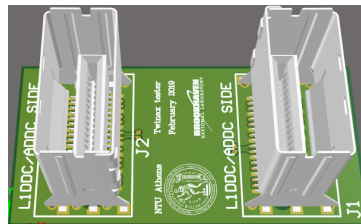
Before the integration of the micromegas chambers, all twinax cables are tested for continuity. Bending and stretching can damage the twinax cables during their placement inside the spacer frame. Thus, cables will be retested after the placement to verify the signal integrity. Cables can be easily tested by plugging both connectors on the FMC mezzanine (described in Section A.3.1) and using the micro-DAQ (described in Section 6.2.1). The only disadvantage of using this setup is that not all receiving pairs of the FMC are connected to the FPGA and the pair B10-B11 (on the FMC side) cannot be tested.

A simple board named twinax terminator that redirects the transmitting pairs to the receiving ones was designed and fabricated. The transmitting sideband pair of the

FMC miniSAS connectors is redirected back to the same transmitted pair of another miniSAS connector of the FMC with the use of a second miniSAS connector on the twinax terminator. By connecting two cables on the micro-DAQ side and the twinax terminator on the other side, all used differential pairs can be tested. The pinout of the two miniSAS connectors of the twinax terminator is presented in Figure A.32(a). Since the pins of the FMC miniSAS are connected to regular IO pins of the FPGA, the sidebands of the four miniSAS connectors can be configured as receivers and the rest as transmitters. With this configuration up to eight cables can be tested simultaneously. A 3D representation of the miniSAS terminator board is shown in Figure A.32(b). A typical testing setup including the micro-DAQ system, the twinax terminator and the micromegas chamber is presented in Figure A.33. Twinax terminator was used to test the first 136 twinax cables placed inside the spacer frame. SLVS signals were transmitted and received back in a total length of 6 m tin cables. All cables were functional and zero errors observed even for the differential pairs that are transmitted in the single ended wires (sidebands).



(a)



(b)

Figure A.32: miniSAS terminator:(a) pinout, (b) 3D representation.

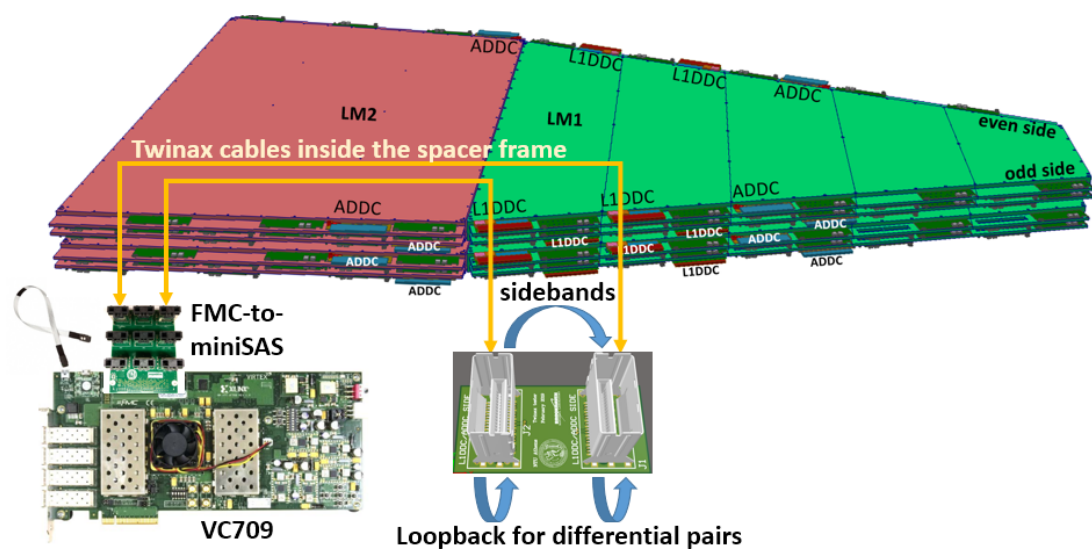


Figure A.33: Cable testing setup with twinax cables placed inside the spacer frame.

Presentations and publications

B.1 Publications in scientific journals

- **“Electronics design and system integration of the ATLAS New Small Wheels”**
P. Gkoutoumis.
JINST 12 C01088 (2017)

B.2 Publications in International Conferences’ Proceedings with referees

- **“Prototype board development for the validation of the VMM ASICs for the New Small Wheel ATLAS upgrade project”**
P. Gkoutoumis.
DOI: 10.1109/MOCAST.2018.8376599
- **“Level-1 Data Driver Card of the ATLAS New Small Wheel upgrade”**
P. Gkoutoumis.
DOI: 10.1109/NSSMIC.2015.7581785
- **“Level-1 data driver card of the ATLAS new small wheel upgrade compatible with the phase II 1 MHz readout scheme”**
P. Gkoutoumis.
DOI: 10.1109/MOCAST.2016.7495115
- **“Testing the Level-1 Data Driver Card for the New Small Wheel of the ATLAS detector”**
I. Messologitis et al.
DOI: 10.1109/MOCAST.2017.7937667
- **“Prototype board development for the validation of the VMM ASICs for the new small wheel ATLAS upgrade project”**

P. Gkoutoumis.

DOI: 10.1109/MOCAS.T.2018.8376599

B.3 Publications and presentations in international conferences

- **Muon/NSW WEEK**, 22 – 26 October 2018, CERN, Switzerland, Oral presentation: *Rim L1DDC and Direct low jitter clock.*
- **Topical Workshop on Electronics for Particle Physics (TWEPP)**, 17 – 21 September 2018, Antwerpen, Belgium, Poster presentation: *Level-1 Data Driver Card - A high bandwidth radiation tolerant aggregator board for detectors.*
- **International Conference on Modern Circuits and Systems Technologies (MOCAS.T)**, 7 – 9 May 2018, Thessaloniki, Greece, Oral presentation: *Prototype board development for the validation of the VMM ASICs for the New Small Wheel ATLAS upgrade project.*
- **ATLAS Week**, 19 – 23 February 2018, CERN, Poster presentation: *Prototype board development for the validation of the VMM ASICs for the New Small Wheel Upgrade project.*
- **ATLAS Week**, 19 – 23 February 2018, CERN, Poster presentation: *The MicroDAQ system, an FPGA-based readout scheme for testing the Micromegas Front-End and readout boards of the New Small Wheel Upgrade Project.*
- **ATLAS Week**, 19 – 23 February 2018, CERN, Poster presentation: *Prototype board development for the validation of the VMM ASICs for the New Small Wheel Upgrade project.*
- **ATLAS Week**, 8 – 12 October 2018, February 2018, Poster presentation: *Low jitter clock distribution for the sTGC trigger chain of the ATLAS NSW upgrade.*
- **Muon/NSW WEEK**, 6 – 10 November 2017, CERN, Switzerland, Oral presentation: *DAQ for reading out full wedges during integration.*
- **ATLAS Week**, 19 – 23 JUNE 2017, CERN, Poster presentation: *Level-1 Data Driver Card of the ATLAS New Small Wheel upgrade.*
- **ATLAS Week**, 19 – 23 JUNE 2017, CERN, Poster presentation: *Designing and testing of prototype boards for the validation of the VMM3 ASIC.*
- **ATLAS Week**, 19 – 23 JUNE 2017, CERN, Poster presentation: *A readout firmware for the micromegas prototype front-end board of the New Small Wheel upgrade.*
- **International Conference on Micro Pattern Gaseous Detectors (MPGD)**, 22 – 26 May 2017, Philadelphia, USA, Poster presentation: *LEVEL-1 DATA DRIVER CARD - A high bandwidth radiation tolerant aggregator board for detectors.*

- **IEEE NSS/MIC conference**, 29 October – 6 November 2016, Strasbourg, France, Poster presentation: *Level-1 Data Driver Card of the ATLAS New Small Wheel Upgrade Compatible with the Phase II 1 MHz Readout Scheme*.
- **14th Topical Seminar on Innovative Particle and Radiation Detectors (IPRD16)**, 3 – 6 October 2016, Siena, Italy, Oral presentation: *Electronics Design and System Integration of the ATLAS New Small Wheels*.
- **Muon/NSW Week**, 26 – 30 September 2016, Chios, Greece, CERN, conference participation.
- **HEP**, 12 – 14 May 2016, Thessaloniki, Greece, Oral presentation: *Level-1 Data Driver Card of the ATLAS New Small Wheel Upgrade Compatible with the Phase II 1 MHz Readout*.
- **International Conference on Modern Circuits and Systems Technologies (MO-CAST)**, 12 – 14 May 2016, Thessaloniki, Greece, Oral presentation: *Level-1 Data Driver Card of the ATLAS New Small Wheel Upgrade Compatible with the Phase II 1 MHz Readout*.
- **Muon/NSW WEEK**, 12 – 16 October 2015, Munich, Germany, Oral presentation: *L1DDC update, readout at 1 MHz L0*.
- **IEEE NSS/MIC conference**, 31 September – 7 October 2015, San Diego, USA, Poster presentation: *LEVEL-1 Data Driver Card (L1DDC) of the New Small Wheel ATLAS Experiment*.
- **ATLAS Week**, 15 – 19 June 2015, CERN, Poster presentation: *Level-1 Data Driver Card for the ATLAS New Small Wheel Upgrade*
- **International Conference on Modern Circuits and Systems Technologies (MO-CAST)**, 12 – 14 May 2016, Thessaloniki, Greece, Oral presentation: *Level-1 Data Driver Card of the ATLAS New Small Wheel Upgrade Compatible with the Phase II 1 MHz Readout*.

B.4 Internal publication in ATLAS experiment

- “Upgrading the New Small Wheel readout to handle a 1 MHz readout rate”
T. Alexopoulos *et al.*
ATL-COM-MUON-2016-026, CERN, Geneva (2016),

B.5 Total ATLAS publications

- According to the [INSPIRE](#) website, there are 208 co-sign publications of the ATLAS experiment in international scientific journals.

Abbreviations

ADC Analog to Digital Converter

ADDC Address in Real Time Data Driver Card

AGND Analog GrouND

ART Address in Real Time

ASIC Application Specific Integrated Circuit

ATCA Advance Telecommunication Computing Architecture

BC Bunch Crossings

BCID Bunch Crossing Identification Nuber

BCR Bunch Crossing Reset

BER Bit Error Ratio

BGA Ball Grid Array

BNL Brookhaven National Laboratory

CA Charge Amplifier

CDR Clock and Data Recovery

CML Current Mode Logic

COTS Commercial Off The Shelf

CPLL Channel Phase Locked Loop

CSC Cathode Strip Chambers

CTF Clock and Trigger Fanout

CTLE Continuous Time Linear Equalizer

CTP Central Trigger Processor

DAC Digital to Analog Converters

DAQ Data AcQuisition

DC Direct Current

DDR Double Data Rate

DGND Digital GrouND

DIP Dual In-line Package

DSCR DeSCRambled

EF Event Filter

eFEX electron Feature EXtractor

EMCCLK External Master Configuration Clock

EMI Electro-Magnetic Interference

ENC Equivalent Noise Charge

ESR Equivalent Series Resistance

FE Front-End

FEC Forward Error Correction

FELIX Front-End Link eXchange

FFT Fast Furrier Transform

FMC FPGA Mezzanine Card

GBLD GigaBit Laser Driver

GBTIA GigaBit TransImpedance Amplifier

GEM Gas Electron Multiplier

gFEX global Feature EXtractor

GUI Graphical User Interface

HDLC High-Level Data Link Control

HDMI High-Definition Multimedia Interface

HLT High-Level Trigger

HSLT High Speed L1DDC Tester

HV High Voltage

IBERT Integrated Bit Error Ratio Test

ILA Integrated Logic Analyser

IP Interaction Point

ISI Inter-Symbol Interference

jFEX jet Feature EXtractor

JTAG Join Test Action Group

LOA Level-0 accept

L1A Level-1 accept

L1DDC Level-1 Data Driver Card

LAr Liquid Argon

LC Inductor Capacitor

LCP Liquid Crystal Polymer

LDO Low Drop-Out

LHC Large Hardon Collider

LM Large Module

LV Low Voltage

LVDB Low Voltage Distributor Board

LVDS Low Voltage Differential Signaling

LVPECL Low Voltage Positive Emitter-Coupled Logic

MDT Monitored Drift Tube

miniSAS mini Serial Attached Small Computer System Interface

MO Monitor Output

MOSFET Metal-Oxide-semiconductor Field-Effect Transistor

MTP Multi-fiber Termination Push-on

mu2e Muon-to- Electron

NSW New Small Wheel

OCR Orbit Counter Reset

OPCUA OPC Unified Architecture

PCB Printed Circuit Board

PDO Peak Detector Output

PHY PHYsical

PLL Phase Locked Loop

PRBS Pseudo-Random Binary Sequence

PS Power Supply

PtP Pulse-at-Peak

PtT Peak-to-Threshold

PWR PoWeR

QPLL Quad Phase Locked Loop

RC Resistor Capacitor

RFI Radio-Frequency Interference

ROC Red Out Controller

ROS Read Out System

SC Slow Control

SCA Slow Control Adapter

SCR SCRambed

SEU Single Event Upset

SFP Small form-factor Pluggable

SGMII Serial Gigabit Media Independent Interface

SGND Safety GrouND

SLVS Scalable Low-Voltage Signalling

SM Small Module

SMA SubMiniature version A

SPI Serial Peripheral Interface

SRF Self Resonant Frequency

sROC sub-ReadOut Controllers

ST Straight Tip

sTDS strip Trigger Data Serializer

TAC Time-to-Amplitude Converter

TDO Time Detector Output

TDS Trigger Data Serializer

TMR Triple Modular Redundancy

ToT Time-over-Threshold

TP Test Pulse

TTC Timing Trigger and Control

TTL Transistor Transistor Logic

TtP Time-to-Peak

VCXO Voltage Controlled crystal Oscillator

VERSO VMM Ethernet Readout Software

VMM Venetis MicroMegas

VTRX Versatile TRasceiver

WQFN very thin Quad Flat No-lead

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