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Analog Front End Development for the Large Hadron Collider Interlock Beam Position Monitor Upgrade

Master Thesis

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Abstract

The interlock Beam Position Monitor (BPM) system in the Large Hadron Collider (LHC) is responsible for monitoring the particle beam position at the point of the beam dump kicker magnets and is part of the machine protection system. The current interlock BPM system has some limitations and because of this, an upgrade project has been initiated. This master thesis describes the development of the analog front end electronics of this system, consisting mainly of two parts: A delay line based microwave filter and a high isolation and highly balanced power combiner circuit.

The filter has been validated with real LHC beam measurements and is found to work as expected. More work however needs to be done to ensure the effect that the filter itself has on the beam measurements as the filter could introduce some ringing effects on the signal. The highly balanced high isolation power combiner has been tested through lab measurements and also shows promising results but long-term tests need to be conducted to ensure the reliability of the component as it will need to endure very high signal levels over long periods of time.

Acknowledgements

I would like to thank my supervisor Manfred Wendt who gave me the opportunity to work at CERN - it has truly been a great experience. I would also like to thank my colleagues in the former BI-QP (now BI-IQ/BP) section, especially Andrea Boccardi and Jan Pospisil who have helped and supported me with my work throughout the project.

Acronyms

ADC	Analog-to-Digital converter
ADS	Advanced Design System (software)
Balun	Balanced-to-Unbalanced transformer
BLM	Beam Loss Monitor
BPM	Beam Position Monitor
CERN	European Organization for Nuclear Research
CST	Computer Simulation Technology (software)
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
FPGA	Field Programmable Gate Array
HEP	High Energy Physics
LHC	Large Hadron Collider
PCB	Printed Circuit Board
PPB	Protons Per Bunch
RF	Radio Frequency
TEM	Transverse Electromagnetic
VNA	Vector Network Analyzer
WPD	Wilkinson Power Divider

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1 Introduction

1.1 CERN

The European Organization for Nuclear Research (CERN) hosts the world's largest laboratory for high energy physics (HEP), and is one of the global centers for accelerator-based physics research. Since its establishment in 1954, CERN has made several significant contributions to the global scientific and technological communities. CERN was founded primarily with the idea to help uniting the European countries after the devastating World War II, but now acts and operates more and more globally, supporting scientists in their work and allows the sharing of costs of the increasingly expensive high energy physics experiments [1].

Today CERN hosts the largest particle accelerator complex in the world, consisting out of eight accelerators and decelerators, shown in Fig. 1.1: LINAC, Booster, LEIR, PS, SPS, ELENA, AD and the Large Hadron Collider (LHC). With its circumference of 27 km, the LHC is in fact the largest machine ever built and allows the acceleration and collision of particles currently up to 13 TeV center-of-mass energy. It was thanks to the LHC that the Higgs boson was discovered in 2012, a discovery that was linked to a Nobel price award [2].

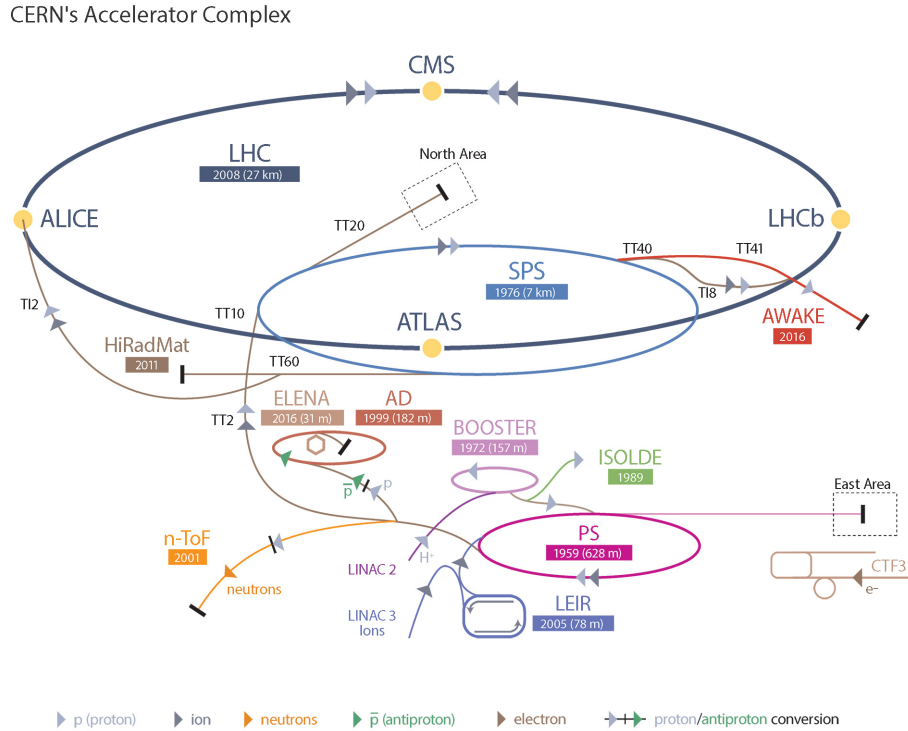


Figure 1.1: The CERN accelerator complex. Image: [3]

The study of subatomic matter and the related forces under well controlled conditions gives the motivation of accelerator-based particle physics. The particle collisions at high energies mimic a situation similar to that of the very early stage of

the universe and act like a microscope that allows physicists to have insight to the underlying physical laws of subatomic particles.

The field of high energy physics is however not only challenging for experimental physicists. A large infrastructure is required to successfully conduct high energy physics experiments: building, maintaining and improving machines of this complexity and scale requires contributions from many different types of engineers and other experts. At CERN there are for example professionals working with radiation protection, civil engineering, beam dynamics, software development and electronics design, just to mention a few typical disciplines.

1.2 Particle Beam Instrumentation

It is essential to monitor the parameters of the particle beam during operation in each of the accelerators, as well as the status of the machine. Typical beam parameters to monitor are:

- the *beam intensity*, given as number of particles in the beam,
- the *beam orbit*, based on beam position measurements at many locations along the accelerator,
- the *beam tune*, the oscillation frequency of the beam
- the transverse *beam emittance*, based on a measurement of the transverse beam profile (particle distribution) or beam size measurement ,
- the longitudinal bunch profile or bunch length ,
- beam or particle losses.

These measurements are vital to characterize and improve the performance of the accelerator, i. e. providing better beams for the experiments, but are also very important to ensure a reliable and safe operation of the accelerators.

Performing these kinds of measurements is an important field in accelerator research and development and is commonly referred to as beam instrumentation and diagnostics. The task for engineers and scientists working in beam instrumentation is to find ways to perform the outlined measurements, and to develop and maintain the required tools. The field of beam instrumentation incorporates a broad diversity spanning accelerator physics, detector technology, custom built electronics, mechanical engineering, vacuum technology, software engineering, to mention a few [4].

At CERN, the Beam Instrumentation (BI) group is responsible for all these systems and the beam position (BP) section is specifically responsible to monitor the beam orbit based on beam position measurements.

1.3 Beam position monitors

A beam position monitor (BPM) measures the transverse beam position with respect to the center of the vacuum chamber [5], i. e. returns the horizontal and vertical beam displacement in units of length, typically with a sub-millimeter resolution. Many BPMs are distributed along the accelerator, often near every quadrupole magnet and at other important locations, to measure the beam *trajectory*, which looks at the beam position over multiple turns, or the *orbit* which considers the beam position on a turn-by-turn rate.

Beside beam and machine characterization, BPMs are also used for machine protection purposes, which is the subject of this thesis that considers the interlock BPMs in the LHC. For this type of application the BPM data is used to monitor the beam position and for triggering a beam dump in the case that the beam is drifting too far from the center of the beam pipe, as this may cause severe damage to the machine. In the case of the LHC for example, the maximal particle drift that the interlock BPM system allows is ± 3.5 mm from the beam pipe symmetry axis. If any interlock BPMs report a value greater than this for a given number of bunches within a certain time frame, the beam is automatically dumped [6].

A general schematic of a typical beam position monitor is illustrated in Fig. 1.2. Here four pickup electrodes are arranged symmetrically along the horizontal and vertical axis of the cross section, which is a typical configuration. The electrodes interact electromagnetically with the charged particles in the beam pipe and each of them return a pulse-like signal, which is proportional to the bunch intensity and to the distance between beam and electrode, i.e. to the beam position. All four electrode signals are routed to the front-end electronics, which consist of a variety of signal processing elements, for example analog filters, amplifiers, power combiners etc., and is then digitized by an analog-to-digital converter (ADC). To extract the horizontal and vertical beam position information, add the correct scaling and useful timing information, the digital data is further processed and decimated, often by utilizing a field-programmable gate array (FPGA) [7]. The final beam position data is passed on to other systems, e.g. the LHC BPM data is used for an orbit feedback system.

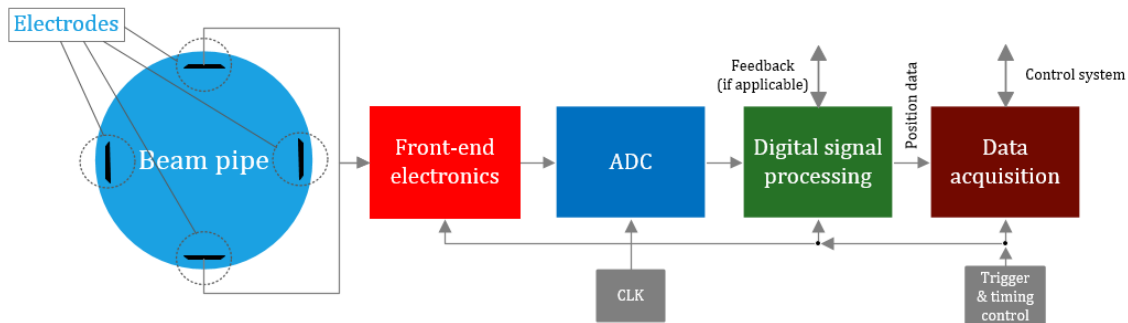


Figure 1.2: A general schematic of a modern BPM system.

The voltage signal from each BPM electrode, A , is proportional to the beam intensity I can in general be expressed as

$$A_{\pm}(x, t) = Ik(1 \pm x)p(t). \quad (1)$$

Here k is a parameter that accounts for the geometry of the electrode itself and $p(t)$ is the impulse response of the pickup. To extract the beam position along one axis, the sum and difference of two opposite electrodes are compared as

$$\text{BeamPosition} = \frac{A_+ - A_-}{A_+ + A_-}. \quad (2)$$

The concept and technical implementation of a BPM system can vary a lot, both in terms how the position signal is generated by the BPM pickup, as well as how the signal is processed in the read-out electronics. Historically, the BPM signal processing was performed entirely in analog technology - today there is however the possibility to process the data of each BPM digitally at very high rates, which has improved the performance of BPM systems substantially [4].

The signal generating part of the BPM, commonly referred to as the ‘pickup’, is the component that is physically installed in the beam pipe and directly interacts with the particle beam. Different types of BPM pickups are used, optimized for the particular application [4].

- Electrostatic or capacitive pick-ups, often referred to as ‘button’-BPMs.
- Electromagnetic ‘stripline’ couplers.
- Resonant cavity pick-ups.

Each of these pickup types has its own benefits in terms of costs, simplicity, frequency range, etc. Button and stripline pickups are broadband couplers, while the cavity BPM operates at a narrow-band resonance. The LHC interlock BPMs utilize the broadband stripline coupler as BPM electrodes.

1.4 Purpose of this thesis

The purpose of this thesis is to analyze and develop the analog front end in the new LHC interlock BPM system. It is also meant to serve as documentation for the hardware that was developed and as reference in the case of changes that may need to be made or for future developments.

2 The LHC interlock BPM system

2.1 System description



Figure 2.1: The LHC accelerator tunnel.

The LHC, as any other modern high energy particle accelerator, is equipped with a BPM system, primarily to measure and control the beam orbit close to the center of the vacuum chamber. Therefore ~ 1000 BPM pickups are distributed along the two LHC rings, with attached read-out electronics continuously monitoring the LHC beam orbit. The measured beam positions are fed into the orbit feedback, which compares them with the set-value, usually the center of the vacuum chamber, and in case of a deviation corrects the orbit by modifying the current of the appropriate steering magnet. This combination of BPMs and steering magnets in an automatic orbit feedback arrangement ensures the LHC beam being always on the nominal orbit, in particular during the energy ramp.

At nominal beam and machine parameters the total energy of each beam is around ~ 400 MJ - an energy level that has a very large damage potential. Because

of this, it is important that in the event of a *beam dump*, when for some reason a beam extraction is triggered, that the beam can be extracted in a way that does not damage the machine. When a beam dump is triggered, a fast switching magnet – a so-called *kicker* magnet – is enabled during the abort-gap, a $3\ \mu\text{s}$ particle free section within the circulating beam. This gap is necessary because of the rise time of the kicker magnet. The kicker redirects the entire beam trajectory into the dump line and extracts it from the LHC ring within a single turn. Finally, the beam collides at the end of that dump line into a dedicated beam dump which consists of a block of carbon which is shielded with steel and concrete for radiation protection purposes.

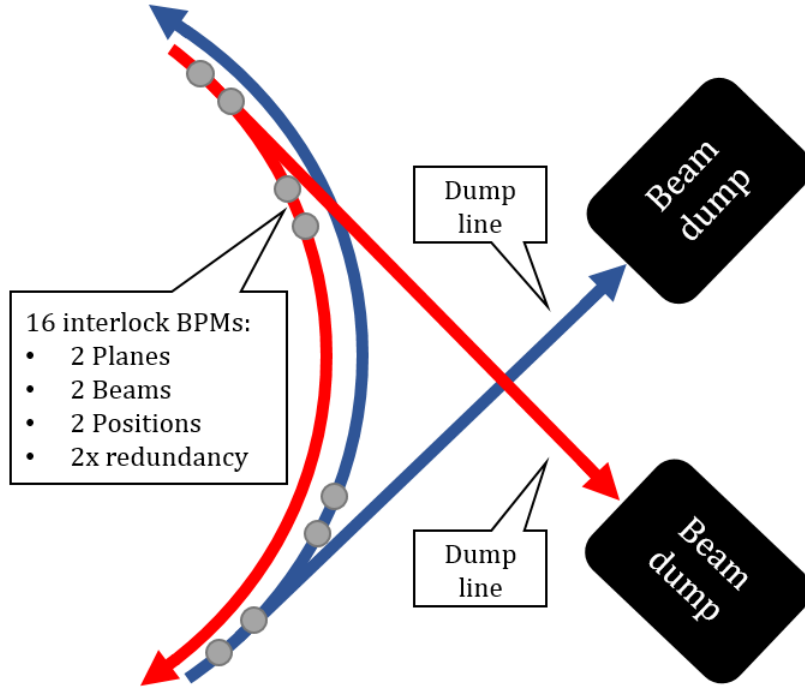


Figure 2.2: Conceptual illustration of the LHC beam dump.

This kicker magnet is always set to redirect the particles at a fixed angle. If the particle beam is outside a certain range within the beam pipe, it can not be guaranteed that the beam hits the dump core and the machine can be severely damaged. This is the motivation for the LHC interlock BPM system: The interlock BPM system is meant to ensure reliable beam extractions by measuring every single bunch in the machine individually to see that each of them are within the 3.5 mm radius that is required for safe extraction [8].

There are however some limitations of the current interlock BPM system, and to mitigate them an interlock BPM upgrade project was initiated. This thesis is focused on the development and prototyping of the analog mission critical sub-systems and components of the new system. In the following sections the shortcomings of the present interlock BPMs are briefly discussed, and the concept of the upgrade is presented.

2.2 System upgrade

2.2.1 Limitations of current system

The current LHC interlock BPM system is based on the hardware of general LHC BPM system, which was designed for a minimum bunch-to-bunch spacing of 25 ns. There is however an operation mode with a bunch spacing of 5 ns – the so called ‘doublet’ bunches, which the system ideally should be able to handle as well. These doublet bunches are used as a ‘scrubbing’ technique that is used for cleaning the beam pipe from residual electrons. If not removed, these electrons may form clouds that can lead to instabilities in the beam [9]. The difference of ‘standard’ singlet and ‘scrubbing’ doublet bunches are illustrated in Fig. 2.3.

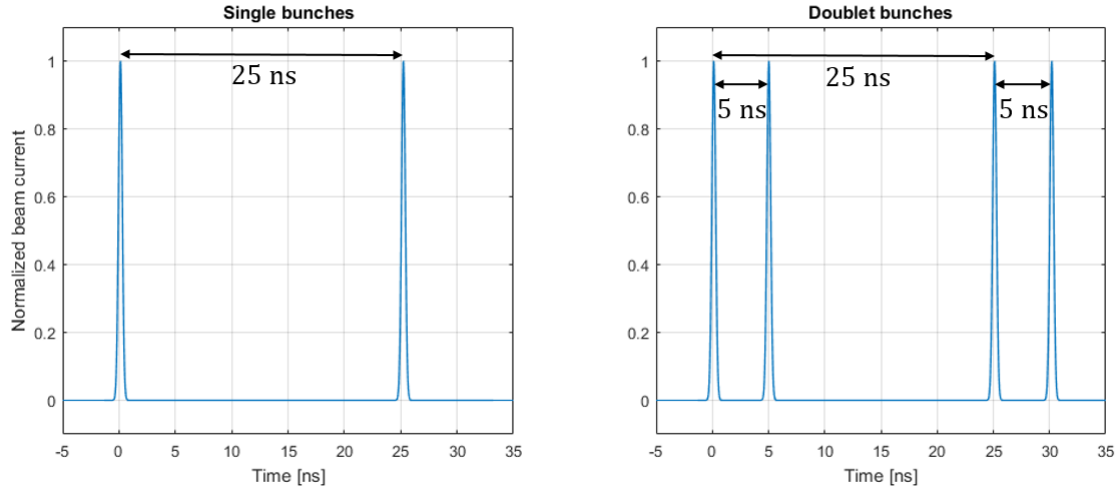


Figure 2.3: Conceptual illustration of single and doublet bunches in the accelerator beam.

Another issue with the current interlock BPM electronics is related to temperature drifts: The position measurements in the current system depend on the temperatures of the electronics. The aim is to remove this temperature dependency in the new system. The motivation of the system upgrade is based on these limitations and the new system is intended to solve these problems. At the same time the upgrade may also offer better performance as it will be based on ‘up-to-date’ technology.

2.2.2 New system proposal

In Fig. 2.4, the architecture of the proposed system upgrade is illustrated. The system works by the following principle:

1. A bunch passes the electrodes of a stripline pickup and excites voltage signals on each electrode which is proportional to the bunch intensity.
2. Two electrodes in a single plane (e.g. top and bottom) are combined to a single channel, where one of them is offset in time by 12.5 ns.
3. The signal is filtered through a delay line filter which repeats each bunch pulse four times to allow for sampling the signal more accurately.

4. The signal is attenuated or amplified, depending on the signal levels.
5. The signal is digitized by a high speed analog to digital converter.
6. The signal is processed in an FPGA and the reading is converted into a measurement of the position by using the ratio between the sum and difference between the amplitudes of two opposite electrodes.

The fact that the two BPM electrodes are combined to a single channel has two main benefits: The system will not suffer from temperature drifts as the signals from both electrodes are now subject to the very same temperatures and this should thus not impact the measurements. Additionally, only half the electronics is needed in comparison with the case where each electrode has its own processing chain.

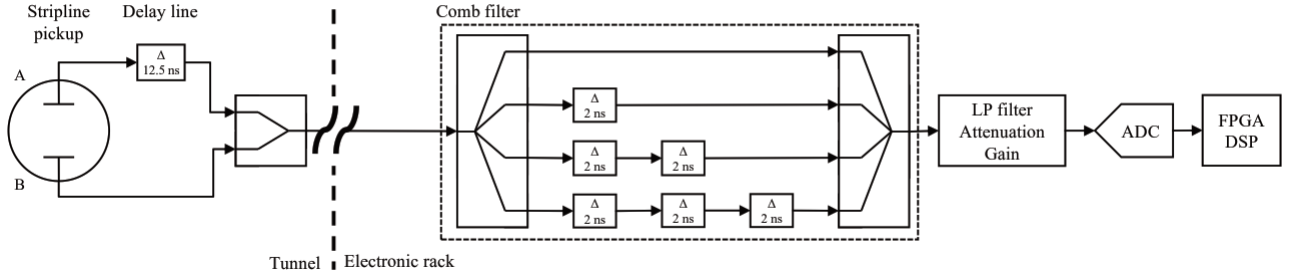


Figure 2.4: Full interlock BPM system illustration. Image: Jan Pospisil [10].

Any position measurement errors in the system are mainly due to noise in the signal chain. Studies made on the signal processing end of the system suggest that this error is proportional to $1/\sqrt{N}$, where N is the number of samples of the signal. This is demonstrated in Figs. 2.5-2.6, which illustrate the standard deviation of position measurement errors for different bunch intensities in the case of a single pulse and four copies of the same pulse. This is the motivation to the delay line filter and to creating multiple copies of the same signal.

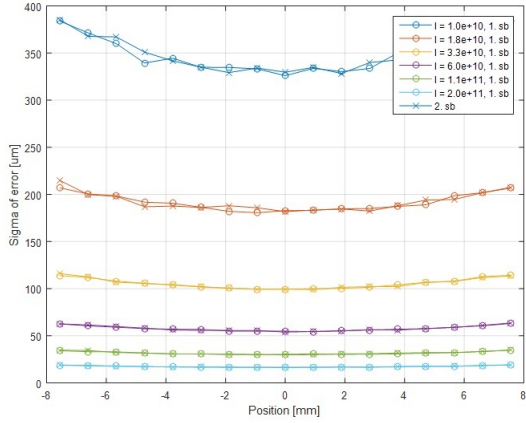


Figure 2.5: Simulation of the position measurement error for N samples. Image provided by Irene Degl’Innocenti.

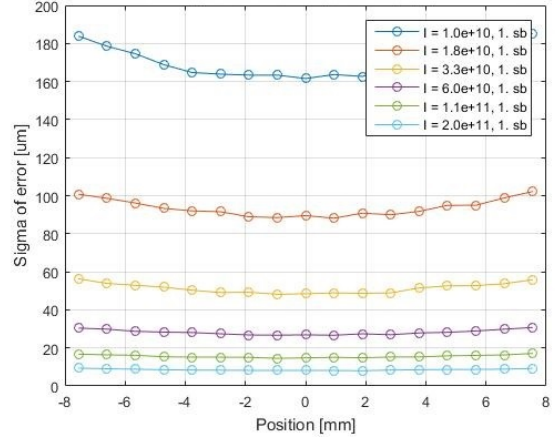


Figure 2.6: Simulation of the position measurement error for $4N$ samples. Image provided by Irene Degl’Innocenti.

2.2.3 Digital acquisition and signal processing

Following the analog-to-digital (ADC) stage, the signal is further processed, e.g. demodulation, decimation, time-stamping, calibration, etc., to finally report the beam position of every passing bunch, including a time stamp. Here, the digital acquisition is performed based on the commercial ADC board *Vadatech* FMC225. The maximum sampling rate is 4 GSa/s, but had to be reduced to 3.2 GSa/s, a limit set by the data link to the data processing unit. The ADC has a voltage range of 725 mV peak-peak and a resolution of 12 bits [11]. The data processing is performed on an *Altera* Arria V GX FPGA [10].

2.2.4 Algorithms

The beam position is calculated by normalizing the difference between two pickup signals in one plane with their sum,

$$\text{BeamPosition} = k(x, y) \frac{A_+ - A_-}{A_+ + A_-}, \quad (3)$$

where A_+ and A_- are the amplitudes of the sampled waveforms of the processed electrode signals and $k(x, y)$ is a non-linear calibration function that is defined by the geometry of the pickup. In our case for small beam displacements, this function can be considered linear, being approximately 0.79 dB/mm for the LHC stripline BPM type [10].

There are multiple ways to obtain the values for the signal amplitudes A_+ and A_- . Investigations made by J. Pospisil [10] demonstrated that for this system a root mean square (RMS) algorithm is a good compromise between complexity and performance, where the amplitudes are computed as

$$A = M \sqrt{\frac{1}{N} \sum_{i=1}^N s_i^2}, \quad (4)$$

where M is a calibration factor, N is the number of samples and s_i is the i :th waveform sample.

2.3 The stripline electrode

2.3.1 Introduction

The use of stripline electrodes is well established in the field of beam instrumentation and they are already well studied and documented [4], [5], [12]. This section is dedicated to summarizing and reproducing some general results about the characteristics of stripline electrodes that are significant for the rest of the thesis. The purpose of doing this is to give an understanding of the properties of the signals that are to be processed in the system. These properties are further important for the development work that has been done in this thesis.

The stripline electrode is a BPM probe that couples electromagnetically to the fields produced by the passing charged particles. They are typically installed in the configuration showed in Fig. 2.7, where each set of two opposite electrodes cover one longitudinal plane. By comparing the sum and difference in amplitude between a pair of opposite electrodes, it is possible to find the relative position along one axis in the cross section of the beam pipe. Combining this with an identical measurement along a perpendicular axis, it is possible to fully determine the relative position in the beam pipe. To convert the relative measurement into an actual displacement in a known unit of length, some kind of calibration function has to be used that can be determined empirically or through simulations.

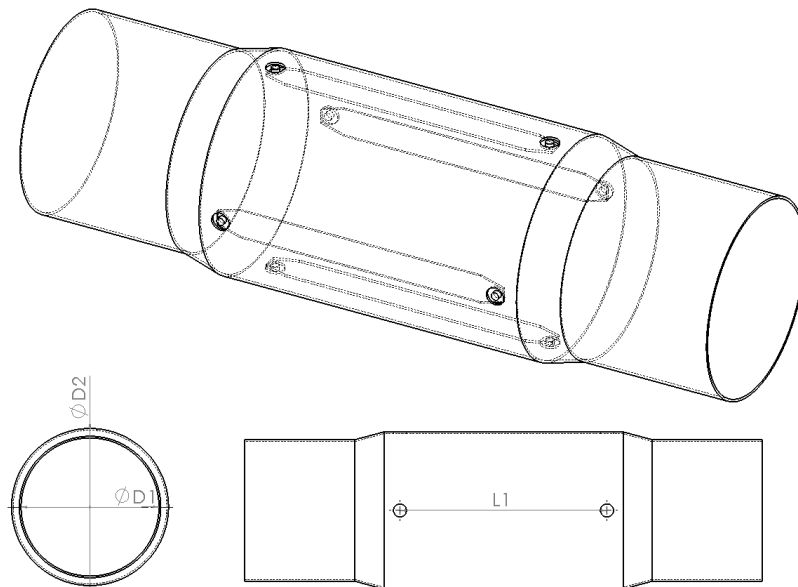


Figure 2.7: The LHC stripline electrodes and their installation in the LHC beam pipe. $D_1 = 80$ mm, $D_2 = 89$ mm, $L_1 = 120$ mm.

The stripline electrode essentially forms a microstrip transmission line with the wall of the beam pipe. A part of the field from the passing particles is coupled to this transmission line and causes a voltage wave to travel along it.

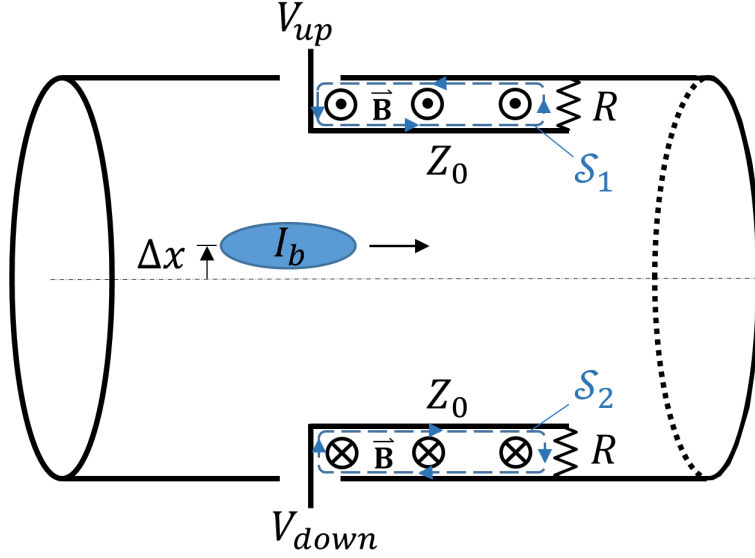


Figure 2.8: The principle of operation of the stripline electrode.

The phenomenon can be explained in multiple ways. One is that as the positively charged particle bunch approaches the stripline, it will repel positive charges (or attract negative ones) and thus cause a voltage wave to travel along it. Another way to see it is that a voltage is induced from the magnetic flux through the surfaces $\mathcal{S}_1$ or $\mathcal{S}_2$, where the voltage is equal to

$$V_{\text{up}} = -\frac{\partial \Phi}{\partial t} = -\frac{\partial}{\partial t} \iint_{\mathcal{S}_1} \mathbf{B}(\mathbf{r}, t) \cdot \hat{\varphi} \, dS, \quad (5)$$

where $\hat{\varphi}$ is the transverse unit vector.

2.3.2 Stripline signals

This section is dedicated to describing what the signal behaviour of the stripline is and what a typical signal might look like. This is to get an understanding of signal duration, voltage levels and bandwidth etc. which are important properties to consider when it comes to developing components in the signal chain that are to process the signals.

The magnitude and phase of the coupled signal will depend on the geometries of the beam pipe and the stripline, and we can say that there is a certain transfer impedance Z_T in the frequency domain that relates the beam current with the output voltage signal. In the frequency domain, the transfer impedance is defined by [13]

$$Z_T(\omega) = \frac{V_{\text{pu}}(\omega)}{I_b(\omega)}, \quad (6)$$

I_b being the beam current and V_{pu} the voltage signal from the pickup. If we assume a certain beam current and electrode geometry, we can approximate Z_T through simulations. In Fig. 2.9, we can see the instantaneous beam current from a CST particle studio simulation using a bunch intensity of 0.9×10^{11} protons, which is

close to nominal bunch charge in the LHC. The particle bunches are assumed to move at the speed of light and to be normal distributed along the trajectory with a standard deviation $\sigma = 50$ mm. A snapshot from the CST simulation is depicted in Fig. 2.10. The geometry of the electrode in the simulation is based on an actual stripline electrode in the LHC, the same as in Fig. 2.7.

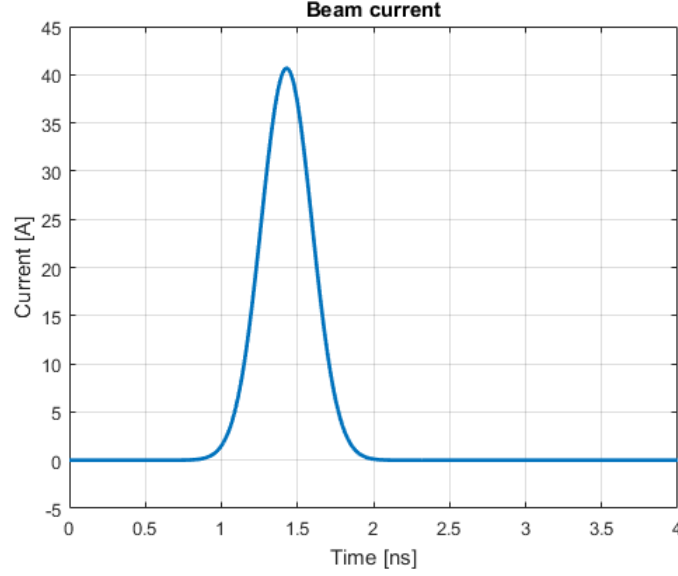


Figure 2.9: Single bunch current over time.

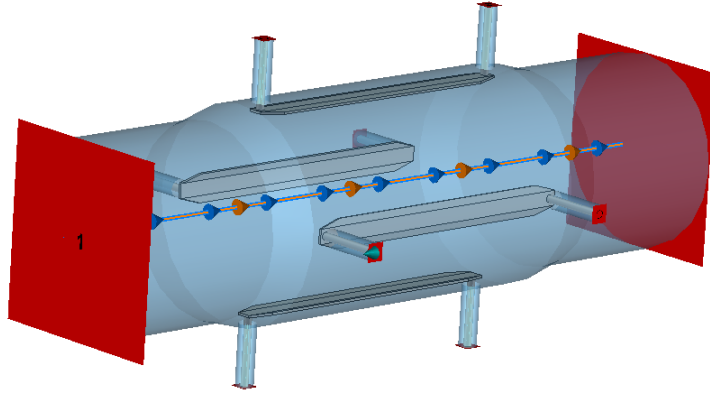


Figure 2.10: Snapshot of the CST simulation setup. Each of the four striplines have a voltage monitor on the output port and the particle path is defined by the line with blue and orange cones. The red areas correspond to waveguide ports which in this context act as open boundaries to prevent reflections.

Letting this current pulse pass by the striplines produces the voltage signal illustrated in Fig. 2.11. There is now a negative pulse right after the first positive one which is generated when the pulse passes the far end of the stripline. This can be explained with Eq. (5). When the pulse leaves the direct vicinity of the electrode, the

magnetic flux through the surfaces $\mathcal{S}_{1,2}$ decreases over time and thus creates a negative voltage. The signal amplitudes, which are proportional to the bunch intensity, may reach very high voltage levels for nominal bunches which makes it important to attenuate the signals heavily before connecting sensitive types of electronics.

The plot contains two sets of stripline signals, each belonging to the left and right electrodes, respectively. The left electrode has a higher signal level than the right due to a beam displacement to the left in the simulation. The difference in amplitudes between the two is related to the beam offset and is the basic principle that is used to measure beam position.

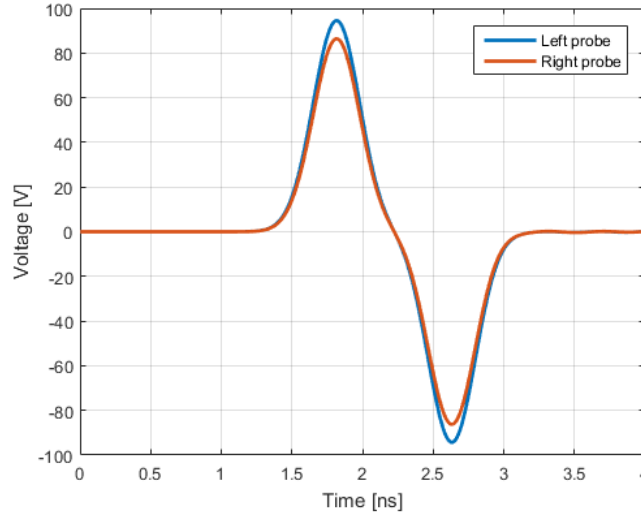


Figure 2.11: The simulated output voltage signals in two opposing electrodes caused by a passing particle bunch with intensity 0.9×10^{11} and displacement of 1 mm towards the left electrode.

A measurement of an actual LHC stripline pickup signal at a 60 GHz sample rate is illustrated in Fig. 2.12 together with a simulated signal with similar beam conditions. The signal was captured with an approximate 1.35×10^{11} bunch intensity and with a total attenuation of about 27.5 dB, partly from the 70 meter long signal cable but also from attenuators that were added when taking the measurement. The simulation was made with the same intensity, and was then processed through a model of the given cable together with the proper attenuation. This was done to see the effect of the cable and also to ensure that the simulations produce the proper signal levels.

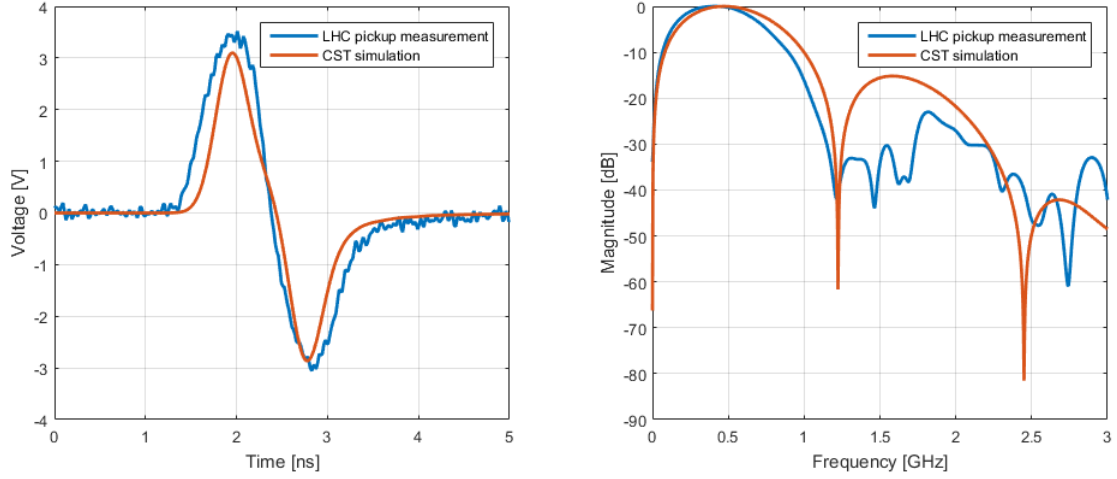


Figure 2.12: Comparison between CST simulated signal convoluted through cable and attenuator models and the real LHC pickup measurement in the time- and frequency-domains.

There is an agreement between the amplitudes of the simulated and measured signals and any deviations may be caused by small differences in the simulated and actual bunch intensities as well as differences between simulation and actual cables and attenuators. It can also be observed that a certain amplitude asymmetry between both signals' positive and negative parts has been introduced. This effect is not present in Fig. 2.11, which means that the cable must be the cause of this. Further it may be noted that in the frequency domain plots of the signals we find that they have very large bandwidths, stretching from just a few MHz up to the GHz range.

Given a certain beam current and its corresponding voltage signal, we can compute the transfer impedance, Eq. (6). In Fig. 2.13, the frequency domain quantities of V_{pu} , I_b and Z_T are illustrated.

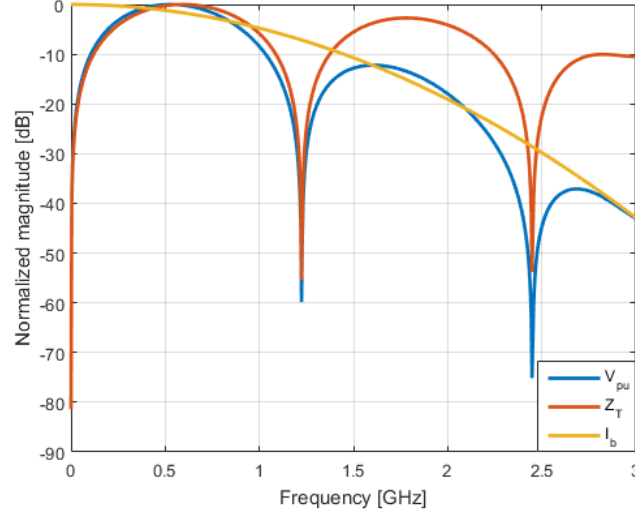


Figure 2.13: Frequency domain plot of the beam pulse (the input signal), the frequency response of the stripline pick-up and the output signal.

2.3.3 Analytic transfer impedance model

At this point, it is possible to create an analytic model for the transfer impedance. The idea with this model is to use it as a fast way of estimating the numerical results of the component power dissipation in Appendix C.

Idealizing $z_T(t)$ and considering the widths of the two pulses as infinitely thin and disregarding the noise, one could say that this signal can be approximated as [5], [13]

$$z_T(t) = c_1 \left(\delta(t - T_d + \frac{T_0}{2}) - \delta(t - T_d - \frac{T_0}{2}) \right), \quad (7)$$

where $\delta(t)$ is the Dirac pulse, T_d is the delay caused by the distance between the beam and the voltage measurement point and T_0 is the delay caused by the length of the stripline. c_1 is a real-valued proportionality constant. In the frequency domain, this impulse response translates to a transfer impedance

$$Z_T(\omega) = c_1 e^{-j\omega T_d} \left(e^{j\omega \frac{T_0}{2}} - e^{-j\omega \frac{T_0}{2}} \right), \quad (8)$$

where the following rules for transformation between time- and frequency-domain have been utilized:

$$x(t - T) \xrightarrow{\mathcal{F}} X(j\omega) e^{-j\omega T} \quad (9)$$

$$\delta(t) \xrightarrow{\mathcal{F}} 1 \quad (10)$$

A comparison between the computed and analytic expression for the transfer impedance is illustrated in Fig. 2.14. For lower frequencies, the agreement is excellent but as we reach higher frequencies, the deviation grows. This is because the pulses in the impulse response $z_T(t)$ are in fact not infinitesimally thin which means that they do not share the higher frequency components with the Dirac pulses.

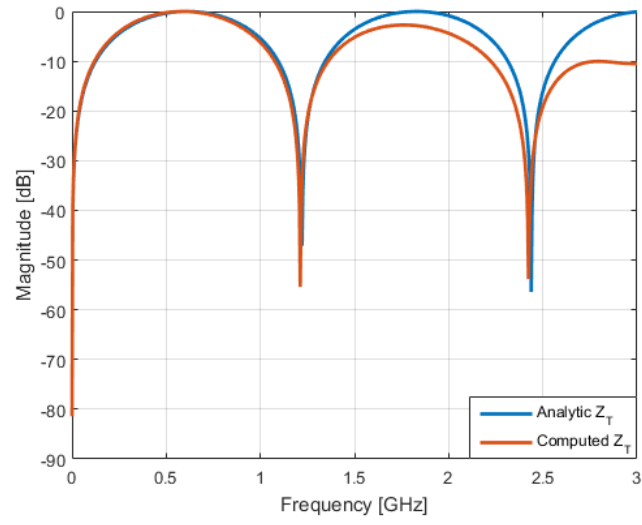


Figure 2.14: Comparison between computed and analytic transfer impedance Z_T . $T_0 = 1.64$ ns.

3 Delay line filter

3.1 Introduction

The pulses that are generated at the stripline electrodes for each passing bunch are relatively short in time. Their duration of about 2 ns in the context of the normal 25 ns cycle means that most of the signal that to be processed is only ‘silence’ or noise. This can be used as an advantage for improving the position measurements, as previously described in Section 2. In the proposed system architecture in Fig. 3.1, the signals from both electrodes in one plane (here top and bottom) are combined to one single channel using a 12.5 ns (half of the normal 25 ns LHC cycle) delay transmission line. The signals are then processed through this delay line based filter that will cause each pulse to be repeated four times.

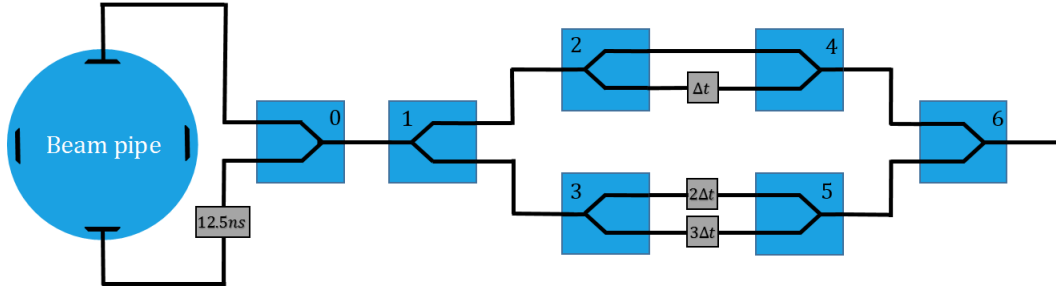


Figure 3.1: A detailed schematic of the delay line filter [10].

The signal splitting and combining in the filter is done using two-way RF splitters and combiners, numbered 1-6. The parameter Δt determines the separation between each repetition and needs to be large enough for each pulse not to overlap the next one.

In Fig. 3.2, a simplified response from beam current to filtered output signal is plotted in the time domain to demonstrate the filter’s function. Here, all delay lines produce a delay of 2 ns and are assumed to be completely lossless. Note that this entire cycle is contained within 25 ns and will under conditions with long bunch trains continually repeat itself with this periodicity.

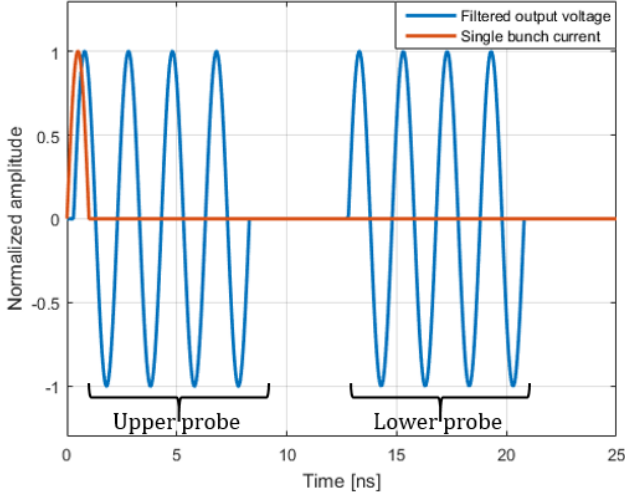


Figure 3.2: Idealized filter response from single bunch to filtered signal.

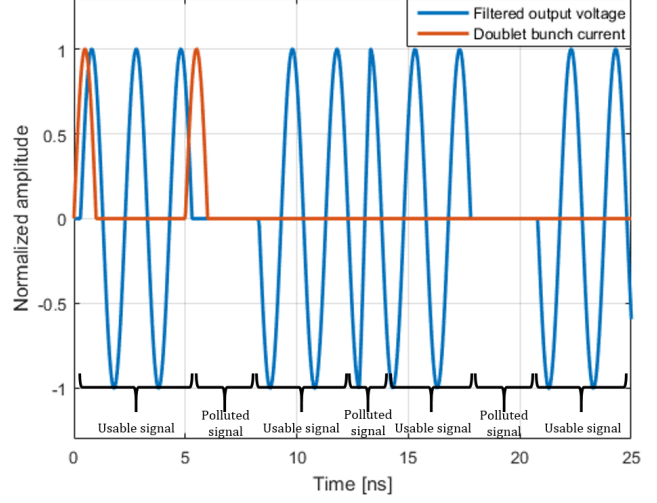


Figure 3.3: Idealized filter response from double bunch to filtered signal.

3.2 Signal theory modelling

As the entire filter only consists of passive splitting and combining elements and delay lines, it is straightforward to analyze it using basic signal processing theory. A theoretical model of the filter is very useful as it can be used as a reference for the performance of the manufactured filter.

We can describe each of the components separately in the frequency domain. The power dividers/combiners are considered as ideal, meaning that they have lossless power division and complete isolation when combining. This corresponds to an S-parameter matrix

$$S_{\text{div}} = \begin{bmatrix} 0 & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \\ \frac{1}{\sqrt{2}} & 0 & 0 \\ \frac{1}{\sqrt{2}} & 0 & 0 \end{bmatrix}. \quad (11)$$

If the delay lines are considered as lossless and without reflections, their S-matrix becomes

$$S_{\text{delay}} = \begin{bmatrix} 0 & e^{-j\omega T_d} \\ e^{-j\omega T_d} & 0 \end{bmatrix}, \quad (12)$$

where T_d is the time delay of the line.

The input signal at the common port of splitter number one (refer to Fig. 3.1) can be related to an output signal at the common port of combiner six by summing each of the four signal paths as follows:

$$H(\omega) = \frac{V_{\text{out}}}{V_{\text{in}}} = \frac{1}{4} \left(1 + e^{-j\omega T_d} + e^{-j2\omega T_d} + e^{-j3\omega T_d} \right). \quad (13)$$

Note that there is a decrease of the exponent in each of the four terms, which is caused by the additional length for each delay line.

This transfer function can now be translated to a time domain impulse response $h(t)$ using the following standard transform pairs:

$$x(t - T) \xrightarrow{\mathcal{F}} X(j\omega)e^{-j\omega T} \quad (14)$$

$$\delta(t) \xrightarrow{\mathcal{F}} 1 \quad (15)$$

$$h(t) = \frac{1}{4}[\delta(t) + \delta(t - T_d) + \delta(t - 2T_d) + \delta(t - 3T_d)], \quad (16)$$

where $\delta(t)$ is the Dirac pulse. The ideal frequency and time domain responses are plotted in Figs. 3.4 and 3.5.

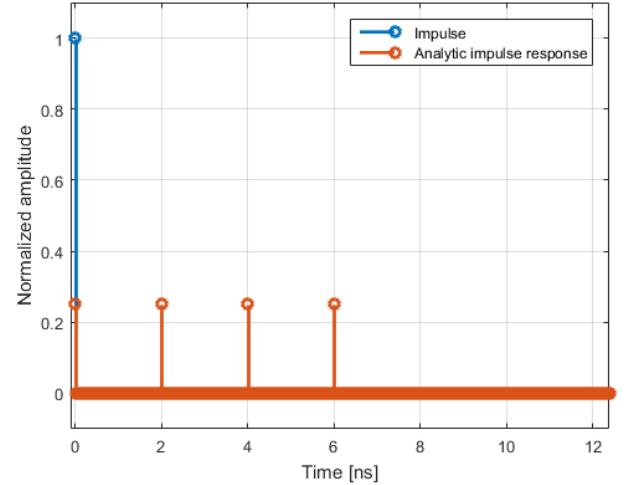
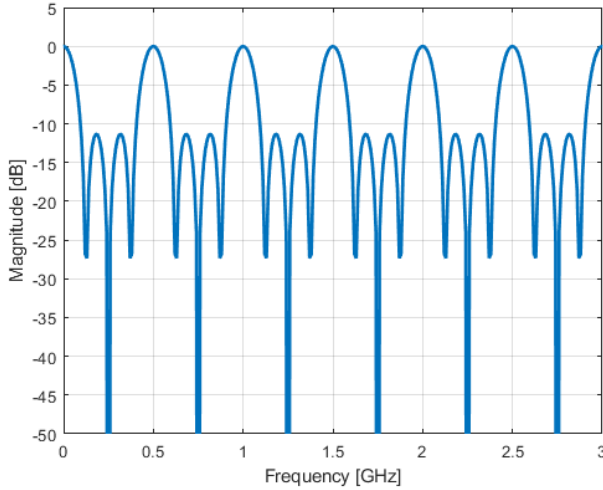


Figure 3.4: Ideal filter frequency response.

Figure 3.5: Ideal filter impulse response.

It is also important to include the losses and their dependency on frequency in the model. The losses can be described with an exponential function $f(\omega)$ that is multiplied with the ideal transfer function, Eq. (13), for obtaining the lossy and more realistic transfer function $H_{\text{lossy}}(\omega)$ [14].

$$H_{\text{lossy}}(\omega) = f(\omega) \left(\frac{1}{4} + \frac{1}{4}e^{-j\omega T_d} + \frac{1}{4}e^{-j2\omega T_d} + \frac{1}{4}e^{-j3\omega T_d} \right) \quad (17)$$

$$f(\omega) = Ae^{-\frac{\alpha}{2\pi}\omega}, \quad (18)$$

where A is the signal amplitude at zero frequency and α is the losses in Np/Hz.

3.3 Proof of concept

A simplified proof of concept design was developed for testing the viability of the filter. A short description of the development of this filter and the hardware used is presented in Appendix A. The filter was measured and tested in two different ways. First an S-parameter model was created and compared to the analytic model in Eq. (13). Secondly, the filter was installed in the LHC, where it was connected to a stripline BPM to capture the real signals.

In Fig. 3.6, the absolute value of the analytic and measured frequency response (S_{21}) is plotted. 15 dB have been subtracted from the analytic curve for simplifying the comparison. This big difference in magnitude is a result of not considering the losses in the analytic model. It is possible to see a slight decrease in gain of the constructed filter as the frequency increases. This is because both the cables and connectors decrease in performance for higher frequencies.

The corresponding time domain impulse response was computed from the VNA measurement and is depicted in Fig. 3.7. Note that the amplitude of the pulses decreases slightly for each pulse. This effect is mainly due to the losses in the delay lines. The spacing of each pulse is within 2 % of the goal of 2 ns, which was deemed sufficient for carrying out the digital signal processing part of the system.

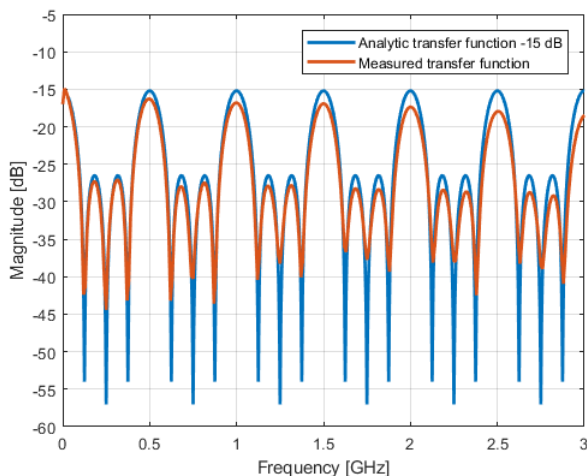


Figure 3.6: Prototype filter measured frequency response (S_{21}) compared with the analytic model.

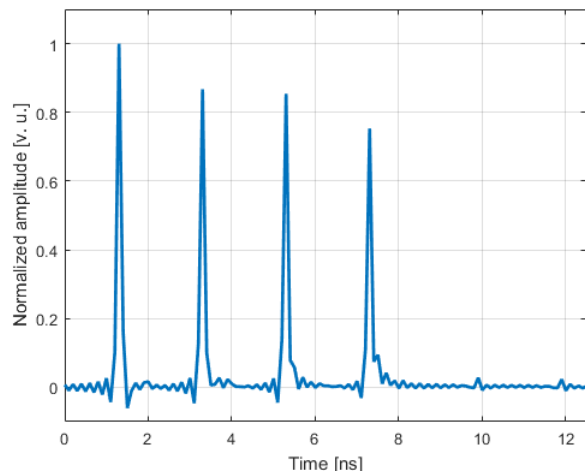


Figure 3.7: Computed impulse response from measured S-parameter.

Some time domain measurements were also made in the LHC using a LeCroy SDA 18000 oscilloscope at a 20 GHz sampling rate during the normal LHC 25 ns cycle and nominal bunch intensities. The results of this measurement are plotted in Fig. 3.8. This initial version of the filter is later used for the development of the software of the interlock system.

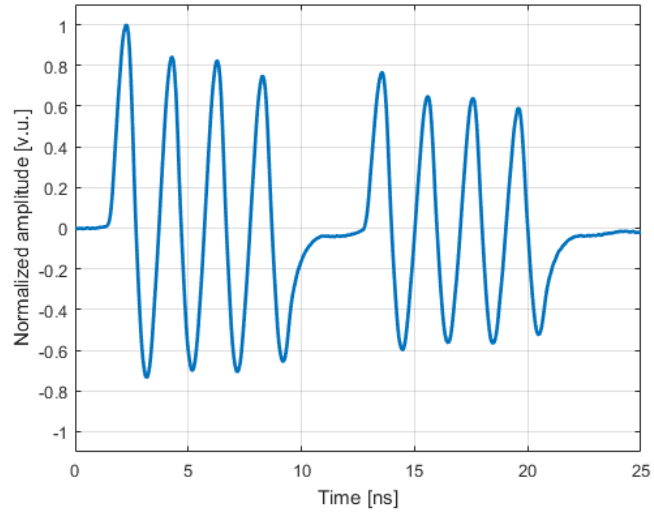


Figure 3.8: Time domain measurement from the LHC stripline pickup during the LHC25NS cycle.

3.4 PCB filter design

The final version of the filter needs to be implemented in a PCB configuration as it is a more reproducible way of building the circuit. The proof-of-concept design presented in the previous section, although fully functional, is largely made by hand which will lead to uncertainties in the production and is why a more reliable way of producing the filter is needed.

Apart from being implemented in a PCB configuration, the filter and its sub components should produce as little *ringing* as possible, which is essentially the most important property of the filter. A low filter ringing means that the impulse response of the physical filter should be as close as possible to the ideal model, Fig. 3.5, with no additional pulses following the original four. This is because any ringing in the signal would influence the beam position measurements. This section aims to explain the process of designing and integrating these elements into a final prototype of the PCB filter and to find designs that produce as little filter ringing as possible.

The key components for designing this type of filter are the combining and dividing elements. These elements are typically identical in their design, meaning that a single type of circuit is used for both splitting and combining a signal. To reduce the ringing in the filter, these components need to have two main properties:

- Low reflections at each input port.
- High isolation between ports 2 and 3, as defined in Fig. 3.9.

The low reflections are needed because otherwise signals can be reflected back and forth between each combining and diving element which will appear as ringing at the filter output. The isolation is important too since any reflected signals could otherwise reach between ports 2 and 3, which also would show as ringing at the output. These properties naturally also need to have bandwidths that match that of the input signal, Fig. 2.12, meaning that the components will need to have a very large bandwidth, ranging from just a few MHz up to more than 1 GHz.

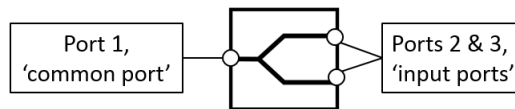


Figure 3.9: Schematic of a combining/dividing element with naming conventions used throughout the report for the different ports.

Another property that the components ideally should have is that they should be able to process the BPM signals without ever being too close to their power rating. Considering the signal levels in section 1.3 about stripline pick-ups and the signal generation, we can conclude that the input signals may reach very high amplitudes. Because of this, it is also important to investigate the power dissipation in the filter components, namely the power dividers, to ensure that the design can handle the

required power levels.

In the following section, some tests are conducted on a couple of commercially available power divider components to see whether they can meet the requirements and produce a well performing filter circuit. The comparison is made between a standard Wilkinson power divider and a commercial power divider from Marki Microwave called PBR0003 SMD. The two components are different in their operation and will first be evaluated based on how they affect the signal ringing in the context of the full filter and secondly their power handling capacity.

3.5 Review of available surface mount combiners

3.5.1 The Wilkinson power divider

The Wilkinson power divider (WPD) is a simple and low cost type of power splitting component that was invented by Ernest J. Wilkinson in 1960 [15]. Its main advantages are the high isolation that it can provide between the two input ports and that it typically has relatively low insertion losses. Additionally, it consists only of a single lumped element which makes it simple to manufacture.

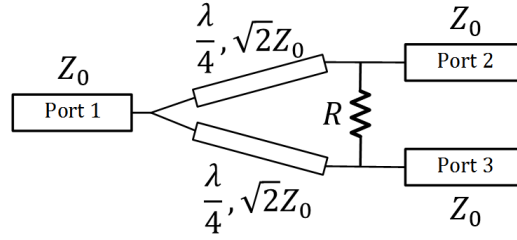


Figure 3.10: Schematic of the Wilkinson power divider.

The WPD makes use of quarter-wave transformers, visible in Fig. 3.10, in order to make the outputs have the same characteristic impedance as the common port. We can derive the input impedance of each of the two branches individually using the transmission line theory and demonstrate that the total input impedance remains a 50Ω load.

A short (low-loss) transmission line with characteristic impedance Z_1 that is terminated in a load Z_L has an input impedance

$$Z_{\text{in}}^{\text{branch}} = Z_1 \frac{Z_L + jZ_1 \tan(\beta l)}{Z_1 + jZ_L \tan(\beta l)} \quad (19)$$

where β is the phase constant and l the distance from the input [16]. Taking the limit $l = \frac{\lambda}{4}$, the impedance is reduced to

$$Z_{\text{in}}^{\text{branch}} = \frac{Z_1^2}{Z_L} \quad (20)$$

The characteristic impedance of each of the two branches Z_1 is equal to $\sqrt{2}Z_0$ and the load is $50\ \Omega$, which yields an input impedance of $100\ \Omega$. As we can consider the two branches to be connected in parallel, the total input impedance is

$$Z_{\text{in}}^{\text{tot}} = \frac{Z_{\text{in}}^{\text{branch}} Z_{\text{in}}^{\text{branch}}}{Z_{\text{in}}^{\text{branch}} + Z_{\text{in}}^{\text{branch}}} = 50\ \Omega \quad (21)$$

The resistor R that is connected between the two branches does not have any effect on the input impedance of the common port as a signal that is split will in theory have the exact same phase at both nodes where the resistor is connected, resulting in a zero voltage difference. The purpose of the resistor is instead to provide isolation between ports two and three. A signal that is inserted at for example port two will cause a certain phase difference over the resistor, which causes most of the power that goes through port three to be dissipated.

This principle of operation is however very dependent on the wavelength, making the WPD a fairly narrow-band component. A WPD in microstrip configuration was designed at 500 MHz through CST simulations to find the bandwidths and losses of this component. Its operation is illustrated in Fig. 3.11.

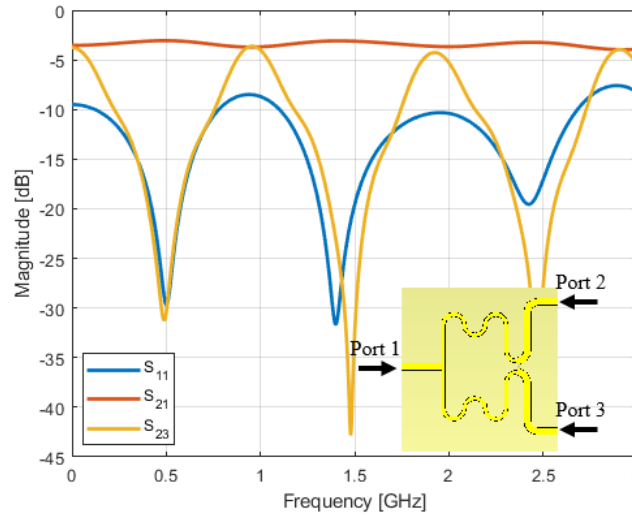


Figure 3.11: S-parameters of a simulated single stage Wilkinson power divider in a microstrip configuration designed at 500 MHz. The layout of the Wilkinson divider is illustrated in the bottom right inset.

The main advantage with the WPD is that it is very simple to design and that the resistor can be chosen arbitrarily, meaning that we can choose the maximal power dissipation by design. To increase the bandwidth, the WPD can instead be designed in multiple stages, where each stage has its own resonant frequency. This does however increase the size of the WPD significantly for each added stage.

3.5.2 The PBR0003 resistive divider

The PBR0003 SMD divider, the surface mount version of the PBR0003 used in the proof of concept design, is a commercial component that is supposed to have

extremely good isolation and splitting capacity over a very large bandwidth. The results illustrated in Fig. 3.12 demonstrate that this divider does both those things excellently and that the signal splitting ratio is almost completely flat from very low frequencies up to at least 3 GHz.

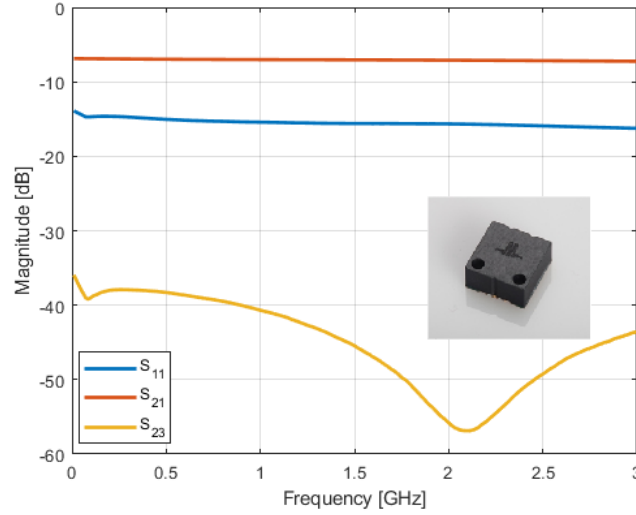


Figure 3.12: S-parameters of the PBR0003 surface mount component. The subset illustrates an image of the chip [17].

This circuit is based on a resistive splitter design that utilizes a balanced to unbalanced transformer to obtain its high bandwidth and isolation. An approximate model of the circuit is depicted in Fig. 3.13. All resistors are $50\ \Omega$.

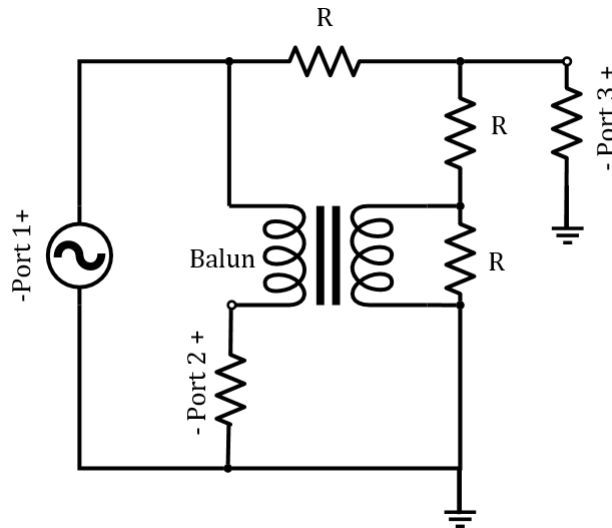


Figure 3.13: Schematic of a wideband power divider similar to PBR0003.

3.5.3 Filter ringing

The performance of each component in the filter is crucial for the digital data acquisition and measurement precision. To quantify this, we must focus on the ringing of the filter, which should be as small as possible for an optimal performance. If the ringing is too significant in duration and amplitude, it may cause the signal from one passing bunch to affect the measurement of the next one and thus produce inaccurate measurements.

To analyze the behaviour of the ringing, the circuit in Fig. 3.1 was simulated in the time domain using the S-parameter models of the power divider components in ADS. The commercial model is provided by the manufacturer and the WPD model was extracted from the CST simulation. These simulations assume reflection free transmission lines and only the ringing caused by the dividers themselves is considered. The used input signal is generated from CST simulations. Note that the input from only one single probe is used and that the second probe with the 12.5 ns delay line is omitted. Simulation results are presented in Figs. 3.14 and 3.15.

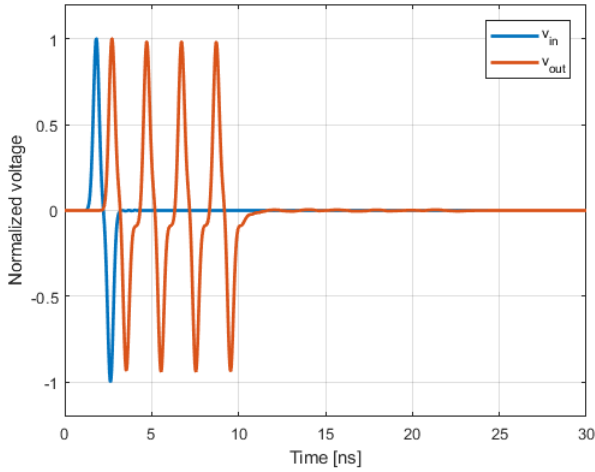


Figure 3.14: In- and output in full filter using PBR0003.

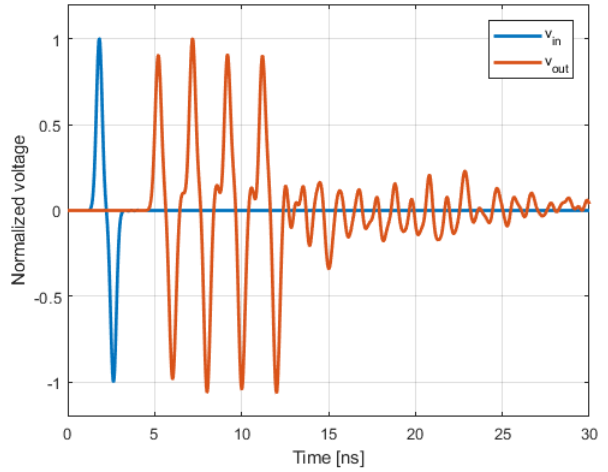


Figure 3.15: In- and output in full filter using WPD.

The tendency to cause ringing in the WPD based filter is very explicit. This can be explained by looking at the bandwidth of the input signal, Fig. 2.13, and comparing it to the bandwidth of the WPD, Fig. 3.11. The signal has for example a significant frequency component at 1 GHz, where at the same time the WPD has a peak in reflection and minimum isolation between ports 2 and 3. This means that signals will be reflected at dividers number two and three, specified in Fig. 3.1, and will leak between the input ports of divider number one and cause unwanted ringing at the output. For the PBR0003 divider which on the other hand practically operates independently of frequency over the interval of interest, there is a significantly smaller amount of ringing and thus an output signal that is more favorable.

3.5.4 Power handling

The LHC has several different modes of operation and the machine may be filled with particle bunches of different intensities. As the signal levels are proportional to the bunch intensities, the signals that are generated at the stripline electrode will thus vary in amplitude over a large range. The assumed absolute minimum and maximum particle bunch intensities are 1×10^9 and 3×10^{11} , respectively.

In Figs. 3.16 and 3.17, the pickup voltage is plotted versus time for both the highest and the lowest bunch intensities. We can see that the signal levels stretch from hundreds of millivolts to hundreds of volts - some three orders of magnitude difference. The signal shape itself does not change, given that the bunch shape remains the same for all intensities. It should also be noted that these simulations are made on perfectly centered beams and that any displacement of the beam will cause even higher signal levels on the electrodes.

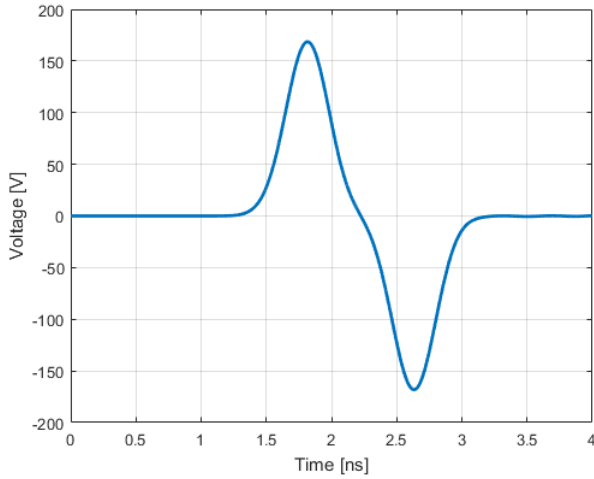


Figure 3.16: Simulated pickup voltage at the highest bunch intensity, 3×10^{11} protons per bunch.

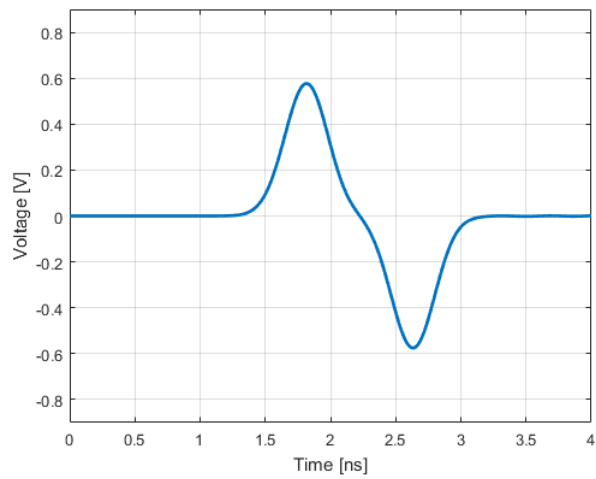


Figure 3.17: Simulated pickup voltage at the lowest bunch intensity, 1×10^9 protons per bunch.

These very extreme signal levels created a need for calculating the average power dissipation in the combiner components. There were some difficulties implementing these calculations using the ADS software, which led to the decision of writing a custom software that could do it instead. This software takes an arbitrary time domain signal, here the measured stripline BPM signals, and calculates the power dissipation in a three-port network, corresponding to the power combiners. An extensive description of the implementation of these calculations is in Appendix D.

Fig. 3.18 shows the dissipation in each of the two suggested components, PBR0003 and the WPD, versus the peak voltage of a measured stripline signal that has a periodicity of half the LHC 25 ns cycle. This is based on the system architecture which for a continuous train of particle bunches would send a new stripline pulse into the delay line filter every 12.5 ns. This models a ‘worst case’ scenario.

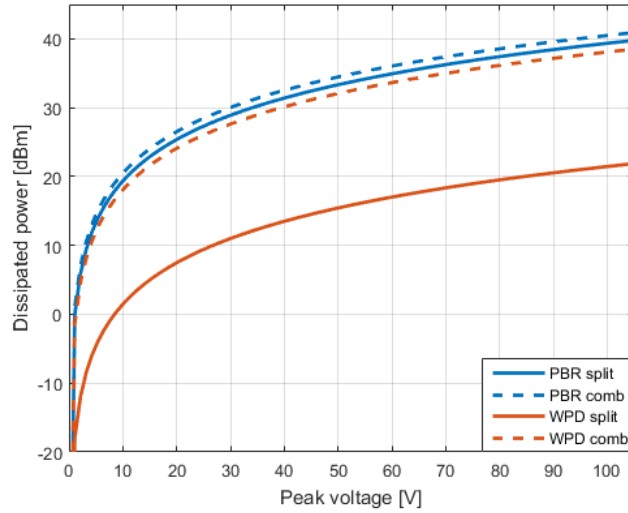


Figure 3.18: Power dissipation as function of peak voltage in the time domain simulations.

It is here found that the PBR0003 component reaches its power rating of 1 W (30 dBm) at around 30-40 V peak signal. The single lumped element in the Wilkinson divider, a $50\ \Omega$ resistor, can on the other hand be chosen to have a power rating much larger than 1 W.

3.5.5 Review of surface mount combiners

Based on the results from this section about two different power combiners, it was decided that none of the two options would satisfy the requirements of the delay line filter. The Wilkinson power divider has a too narrow bandwidth that causes ringing in the filter, and the PBR0003 has a power rating that is lower than required. This is a problem that could be solved by simply introducing attenuators before the filter in the signal chain, however, it would be a more convenient solution to ensure that the filter by itself could endure higher input signals.

This ultimately leads to the decision of developing a custom component with similar properties to the PBR0003, that could produce the lower ringing, but with a significantly higher power rating.

3.6 Design of a high isolation power combiner

3.6.1 Introduction

Because of the shortcomings of the components suggested in Section 3.4, it was decided to develop a customized power combiner component. The circuit that was used is depicted in Fig. 3.19 and is based on that of the PBR0003 circuit that was tested in the previous section. The circuit is a resistive type of combiner that uses a 1:1 balanced to unbalanced, or balun, transformer which helps to create a high isolation between ports two and three as required.

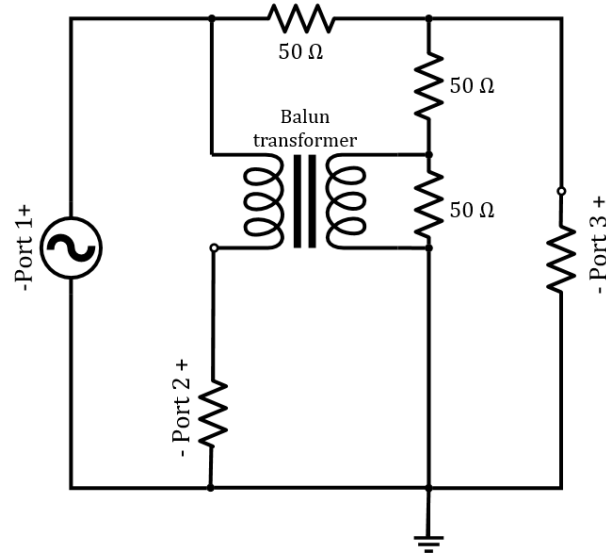


Figure 3.19: High isolation combiner circuit model.

To understand the operating principle of the isolation, it can be useful to look at the time domain response of the balun. In Fig. 3.20 a signal is inserted into node p_1 of the balun and the resulting output signals at nodes p_2 and p_3 are investigated. Note the 180° phase shift between nodes p_2 and p_3 . This is commonly referred to as a differential output.

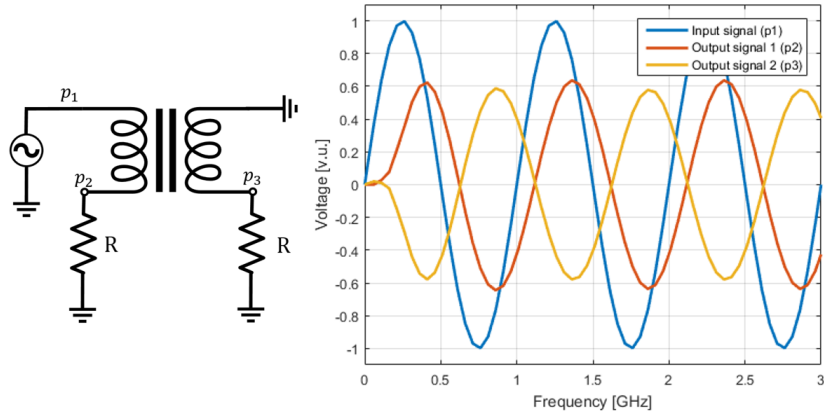


Figure 3.20: Time domain response of a 1:1 balun at 1 GHz. The figure to the left illustrates the balun and the configuration of its ports. $R=50\ \Omega$.

Building the full combiner circuit in Fig. 3.21, using the same balun transformer, we can find an intuitive way to see why the circuit isolates ports two and three from each other. Assuming an input signal on port two, based on the result in Fig. 3.20, there will be a 180° phase shift between nodes v_1 and v_2 . Given that each resistor has the same value ($50\ \Omega$), node v_3 or port three is forced to have zero voltage.

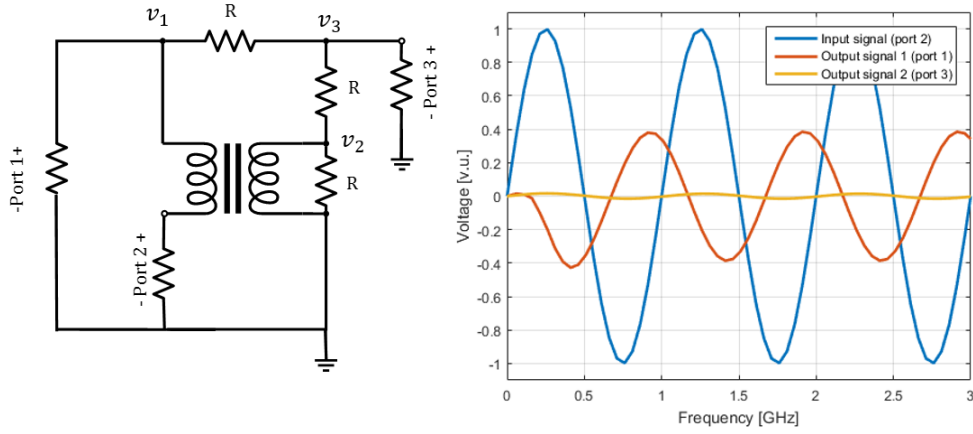


Figure 3.21: Time domain response of the full splitter showing the isolating effect of the balun. The figure to the left illustrates the full combiner circuit and the configuration of its ports. $R=50\ \Omega$

3.6.2 Balun

A number of surface mount baluns from different manufacturers are here briefly investigated by looking at their S-parameter models. The amplitude balance and phase difference between the outputs of each balun are compared to see which balun can produce the most ideal differential output over frequency (and thus the best performing isolation). An ideal behaviour refers to the balun's ability to produce a 180 degree phase shift at the same time as balancing the amplitudes of the differential outputs. These comparisons are plotted in Fig. 3.22, with the components being tested referenced in [18], [19] and [20]. The most ideal balun transforming behaviour was observed with the S-parameter model of a component called RFXF9503.

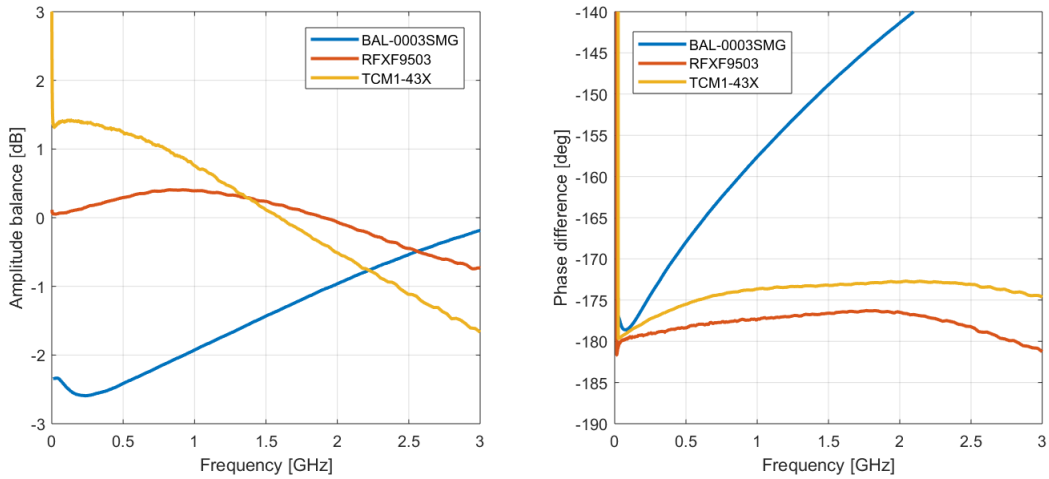


Figure 3.22: Comparisons of amplitude balance and differential output phase difference between different baluns.

3.6.3 Component power ratings

To estimate the requirements on power rating for each of the sub-components, the ADS simulation was run using ideal components. This means that the resistors were modelled as perfect $50\ \Omega$ loads for all frequencies and that the balun transformer had a perfect 1:1 transformation ratio without losses. The peak resistor dissipation as function of input voltage to the divider circuit is plotted in Fig. 3.23. This is the maximum dissipation regardless of which port the signal is inserted into. The simulation was again made using measured electrode signals assuming a 12.5 ns cycle. For the balun, the losses will in general be smaller. This component's only function is to transform the signal and most of the energy is transferred to its output ports. It should however still be confirmed that the component can handle the input signals. The maximum power dissipation in this component as function of input peak voltage to the divider circuit is illustrated in Fig. 3.24.

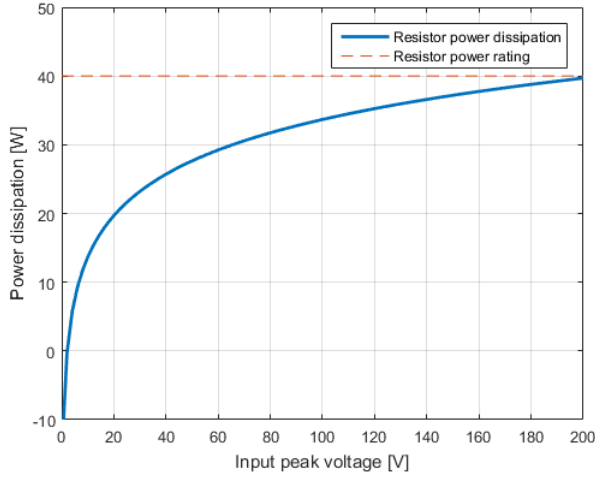


Figure 3.23: Losses in the individual resistors as function of the peak input voltage to the divider circuit using the input signal in Fig. 2.12.

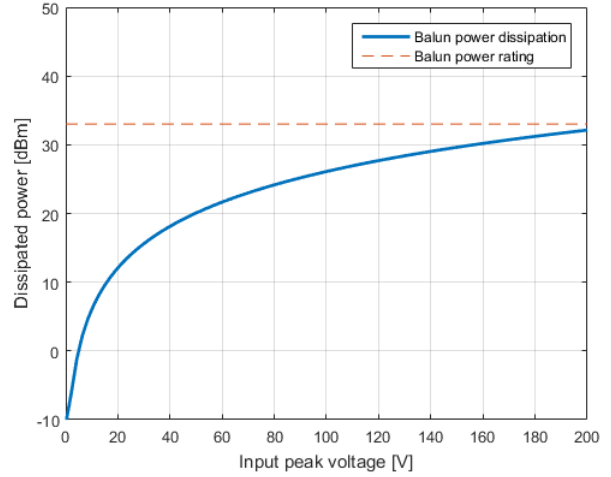


Figure 3.24: Losses in the RXF9503 balun as function of the peak input voltage to the divider circuit using the input signal in Fig. 2.12.

Each of the components reach their power rating around the point where a 200 Volt pickup signal with a 12.5 ns repetition rate is inserted into the circuit.

3.6.4 Layout design

The layout was generated with the intention of keeping the overall size of the circuit as small as possible. This is because to large distances between the component nodes may cause unwanted phase differences that could counteract the isolating effect. For prototyping purposes, it was decided that the initial version of the circuit would be developed in a microstrip configuration on a cheap FR4 substrate that could easily be manufactured in-house. One of the constructed power divider prototypes is depicted in Fig. 3.25.

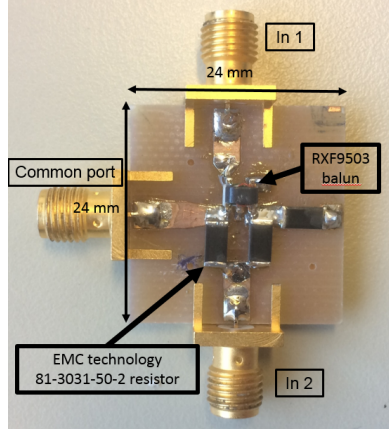


Figure 3.25: Manufactured power divider prototype.

3.6.5 Measurement results

In Figs. 3.26 and 3.27, the S-parameters of the simulated and measured circuit are plotted. There is some resemblance in the behaviour to that of the PBR0003 (Fig. 3.14), but the behaviour of the constructed component does not agree well with the simulations. The amplitude balance is worse than expected and presents a 3 dB difference at 2 GHz.

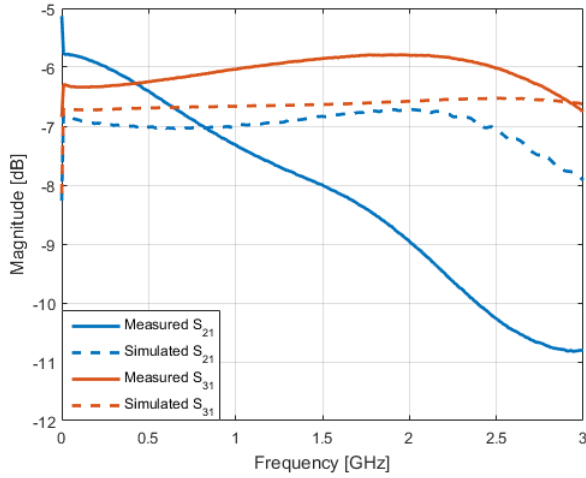


Figure 3.26: Combining/splitting (S_{21} and S_{31}) of the prototype power divider. Port 1 is the common port and ports 2 and 3 are the input ports.

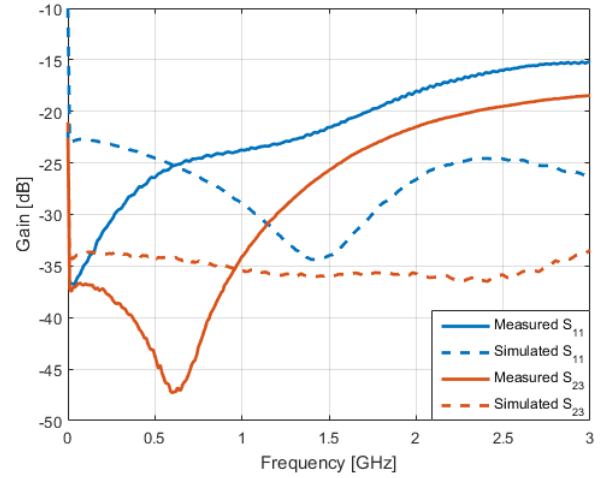


Figure 3.27: Isolation (S_{23}) and common port reflection (S_{11}) of the prototype divider. Port 1 is the common port and ports 2 and 3 are the input ports.

3.6.6 Simulated filter ringing

The full delay line filter was again put together in ADS using the S-parameter models of the combiners and ideal transmission line and was simulated in the time domain with a pickup signal generated in CST. This is the same simulation that was made in section 3.5.3. Assuming a sufficiently high power rating of the component, what was of special interest this time was to look at the ringing of the filter which had

been the problem with the Wilkinson power divider, Fig. 3.15. The results of this simulation are plotted in Fig. 3.28. The ringing is in this case slightly larger than in the case of the PBR0003, but also significantly smaller than the Wilkinson power divider of Figs. 3.14 and 3.15.

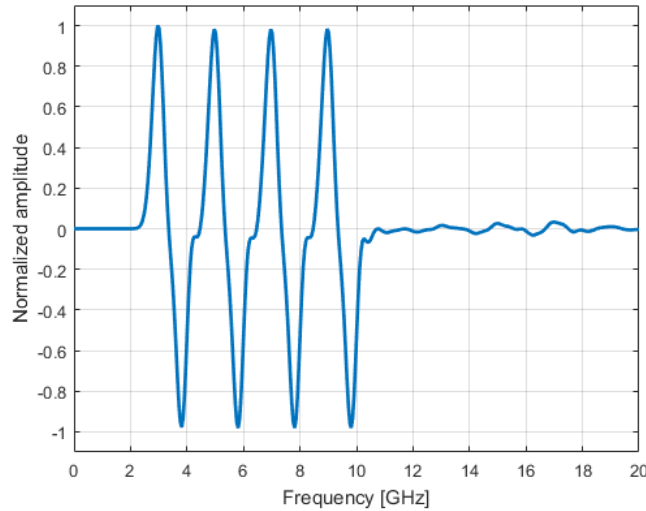


Figure 3.28: Simulated time domain filter output when using the measured prototypes and ideal transmission lines.

3.6.7 Power handling

In Fig. 3.29, I have plotted the results of the same power dissipation simulations on the complete component together with a power rating that was approximated with the ideal component ADS simulations. This graph suggests that the component can handle 200 V peak voltage of the 12.5 ns repeating stripline signal when used as a divider and 170 V when used as a combiner. These values should however be interpreted with some caution as the simulation is not completely accurate. Additionally, other parts of the component, such as solder joints, may break down before this point due to heating.

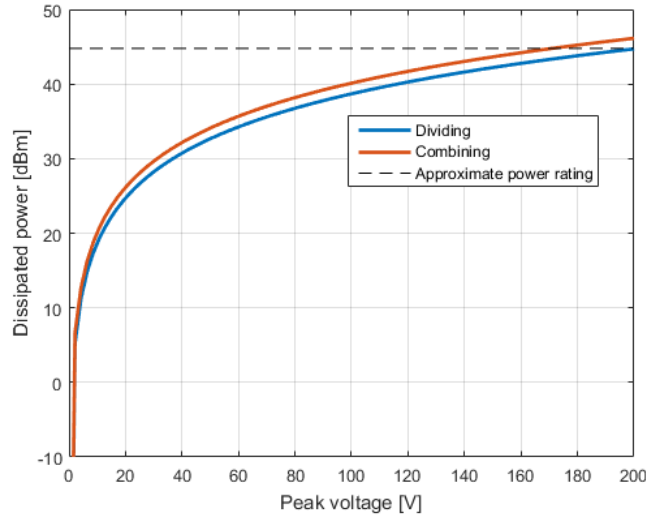


Figure 3.29: Total power dissipation in the prototype surface mount combiner circuit versus peak voltage of the 12.5 ns repeating stripline pulse.

3.6.8 Discussion on surface mount combiner

The goal to design a component that can handle higher input powers than the previously suggested ones was reached. The component is estimated to have a power rating of ~ 44.5 dBm (~ 30 W) in the dividing mode where the power rating is more crucial.

From a signal conditioning perspective the constructed circuit performs well for lower frequencies, especially around 500 MHz in the sense that the amplitude balance is very good and the isolation between ports two and three is very high. The circuit is however more dependent on frequency than anticipated and does not agree with the simulations, especially for higher frequencies. One important reason to this is the fact that the resistors that were assumed to be ideal in the simulations are in fact also dependent on frequency and cannot be assumed to be exactly $50\ \Omega$ over the entire interval. Their considerable size also may create phase differences that are not taken into account when using the ideal models. Typically, it would be a good option to find a component that has an S-parameter model provided by the manufacturer, but I was unfortunately unsuccessful in finding such a model. Additionally, another possible source of errors in the simulations may be that the S-parameter model for the balun that was provided by the manufacturer is not completely accurate. The amplitude balance of the circuit is however not critical in the context of the delay line filter, because the filter has a symmetrical ‘mirrored’ layout that causes any imbalances in the combiners to cancel out.

3.7 PCB filter layout

A significant part of the work behind designing the PCB layout is presented in Appendix F, where different details in the design are investigated to find optimal performance. In this section, I only present the conceptual approach for designing the layout.

There are multiple layout solutions for obtaining the architecture in Fig. 3.1, some of which are illustrated in Fig. 3.30. Layout (3) was deemed as unsuitable because it causes imbalance between the different pulses because of losses in the power combiners/splitters - the signals do not travel through the same number of elements and thus experience different losses. Layouts (1) and (2) balance the splitter/combiner losses and even compensates for imbalances between the different ports in each element because of the mirrored layouts. After some trial and error with trying to generate a layout from these two different options, it was decided that layout (2) would be the most compact and simple way to design the filter.

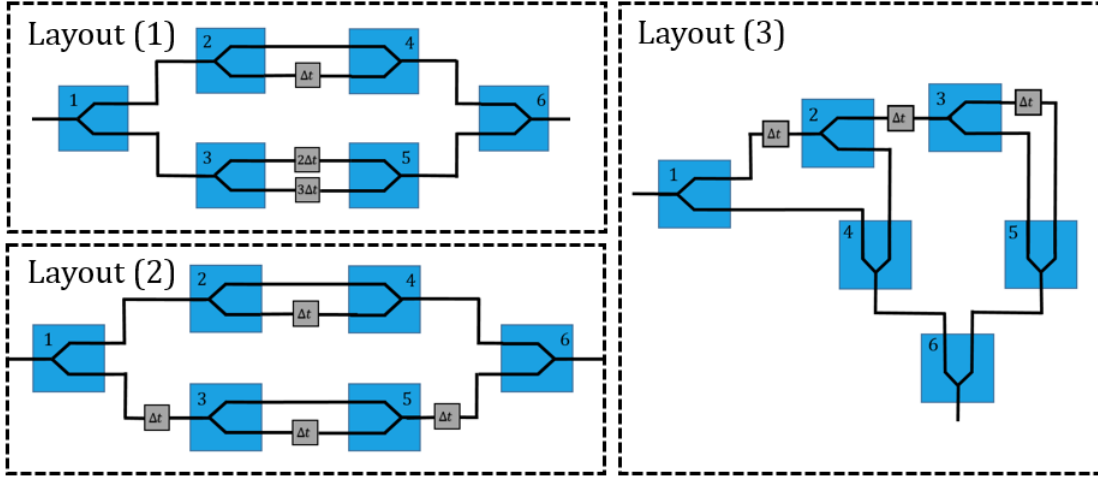


Figure 3.30: Different layout solutions for the FIR filter.

The physical layout was generated using Keysight ADS. To find the correct geometries for the delay lines, they were all isolated and electromagnetically simulated by themselves in CST MWS to ensure the correct signal delay. After assuming a number of approximations for the geometries of the delay lines, the layout was transferred to Altium Designer for generating the final gerber files to send for manufacturing. The layouts for the power dividing circuits were directly copied from the prototype design with some minor modifications. A screen capture from the layout design in Altium Designer is depicted in Fig. 3.31. A photo of the final prototype can be found in Appendix G.

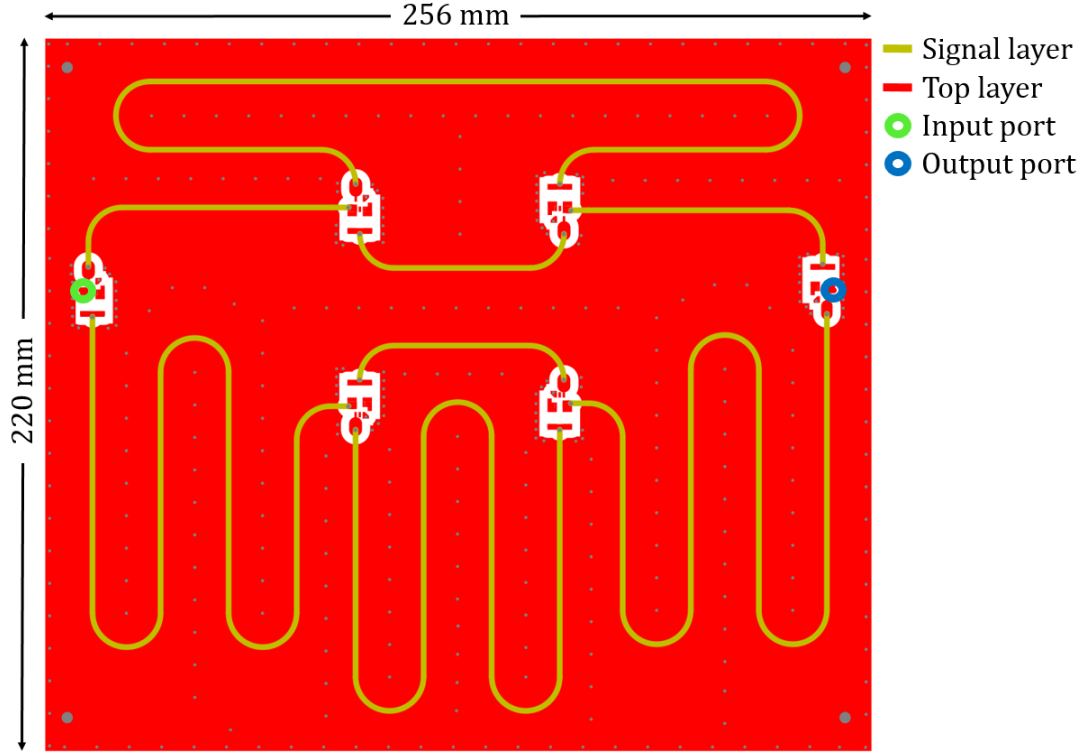


Figure 3.31: Delay line filter PCB layout. All cut out regions are for mounting the power divider components.

3.8 Results

3.8.1 PCB lab measurements

The PCB filter was tested with a VNA measurement to find its transfer function and impulse response, both illustrated in Figs. 3.32 and 3.33. The losses in the PCB combiners are this time very frequency dependent, so to simplify the comparison of the ideal and measured transfer functions, the losses in the ideal model presented in Eq. (18) were included. The loss coefficient was chosen to produce -3.6 dB/GHz.

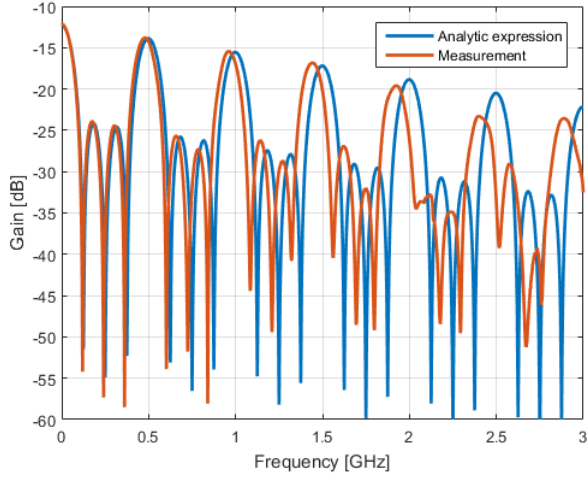


Figure 3.32: Measured PCB filter transfer function compared with the analytic model.

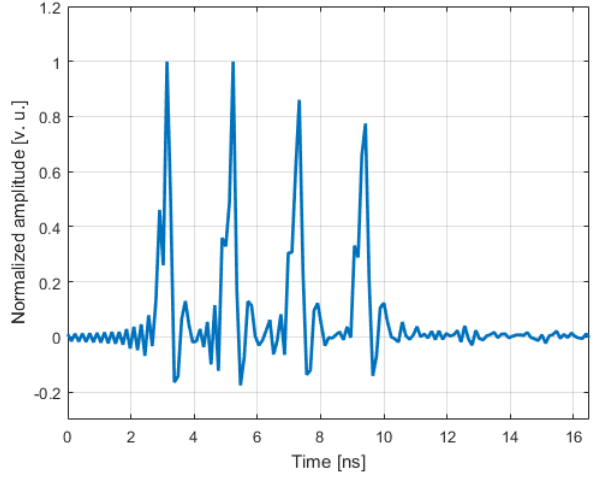


Figure 3.33: Impulse response of measured PCB filter.

3.8.2 PCB beam measurements

What is ultimately determining the performance of the filter is its tendency to produce ringing that is small in duration and magnitude. If the ringing is too strong, there will be signal interactions between different electrode signals as well as different bunches, which will cause errors in the measurements. To estimate the ringing, the filter was measured with a real beam in the LHC with single bunches during the LHC 25 ns cycle. The beam response was measured with 60 GS/s with a 1.35×10^{11} bunch intensity. A 70 meter long coaxial cable separated the oscilloscope and the filter. No additional attenuation was used. A moving average of the measurement results are plotted in Fig. 3.34. The averaging was used to remove some of the noise from the oscilloscope. The distance in time between each pulse is around 2.1 ns, which means that they are slightly off from the target of 2.0 ns.

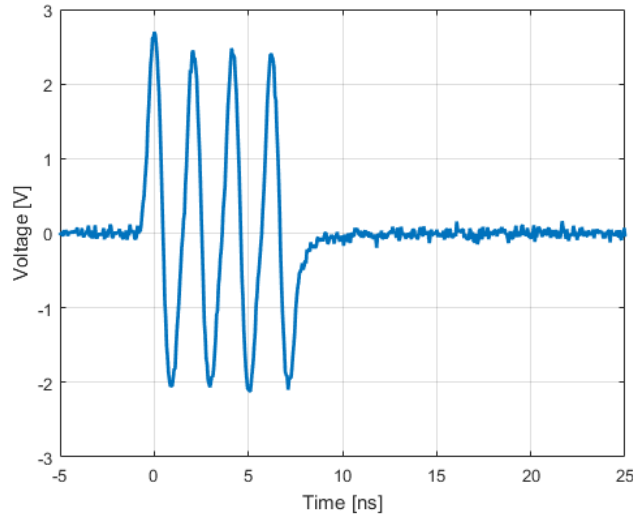


Figure 3.34: Moving average (3 points) of PCB delay line filter prototype beam measurement.

The oscilloscope used in the measurement in Fig. 3.34 introduces a significant amount of noise and it is not possible to distinguish any potential ringing from the noise floor of the measurement.

3.9 PCB delay line filter discussion

There is a clear agreement between measurement and model and the manufactured PCB behaves overall very similar to what was intended. The PCB is however slightly shifted in frequency, which is caused by the small error in the delay time. These small deviations in the electrical length of the transmission lines are likely caused by the fact that the PCB substrate has a dielectric constant that does not correspond exactly to that of the CST simulations as the material parameters are manufactured with some tolerances [21]. This is easily compensated by simply altering the lengths in the next iteration.

Additionally, the filter also behaves rather poorly for higher frequencies. This behaviour is likely caused mainly by the surface mount resistors that do not remain $50\ \Omega$ loads because of reactive effects. The same goes for the balun transformers, where the ferrite transformer core can not sustain its permeability over large frequencies [19].

The ringing of the filter was found to be so small that it was not detectable in the beam measurements. This does not imply that there is no ringing and that it will not affect the position measurements. This calls for further measurements and more analysis on the software side using the system ADC to assess more precisely how the ringing will affect the position measurements.

4 Amplitude balanced power combiner

4.1 Introduction

The analog front end system utilizes high isolation power dividers at two different points: Partially in the delay line based filter but also in the very first point after the electrodes in the analog signal chain, where a combining element is used to merge the signals from two electrodes in one plane into one single channel. The requirements on the combiners in the filter and the very first combiner in the signal chain are however different. Both components need to have very high isolation between the input ports and should also be able to handle very large input signals, but the very first combiner additionally should have a very even amplitude balance between the inputs. If the amplitudes of the two inputs of this component are unbalanced, it would be equivalent to emulating a beam position offset which naturally is an unwanted effect. Additionally, this type of property would lead to a decreased dynamic range of the system, as it would mean that the signals would reach outside the range of the ADC for lower bunch intensities. The PCB combiners that were developed for the delay line filter are highly unbalanced, however this does not really affect the performance of the filter. In this case the amplitude balance is however more important which is why a separate component has been developed for this purpose.

The circuit that is developed in this section is based on the very same circuit as the surface mount versions, Fig. 3.13, but has one major difference: It uses a different type of balun transformer. The amplitude balance in the circuit is effectively limited by the balun and the surface mount balun in the PCB combiners proved not to have a behaviour that was sufficient for a high amplitude balance. In this second version of this circuit, a balun that is based on coaxial cables is instead used, which produces a much better performance.

4.2 Casing design

This combiner was designed to be connected to the stripline electrodes directly in the LHC tunnel. For shielding purposes, it was suggested to make a metallic housing for the component that encloses all the components. This also offers the possibility to integrate SMA connectors directly onto the housing which is convenient from a connectivity point of view. The housing was designed in a way that would make it possible to make separate measurements on the balun by itself before assembling the entire circuit. A small PCB for simplifying the connections between the components was also developed.

It was decided to make the housing out of brass because of its high conductivity and the possibility to solder directly onto the material. In Appendix E, it is briefly investigated to see whether it is useful to use some kind of damping material inside the housing as it could act as an RF cavity, which however was concluded to not be necessary. A 3D model of the housing is depicted in Fig. 4.1, where a preliminary layout of its interior also is visible. The workshop schematics that were used to manufacture the parts are included in Appendix H. The final assembled combiner is depicted in Fig. 4.2.

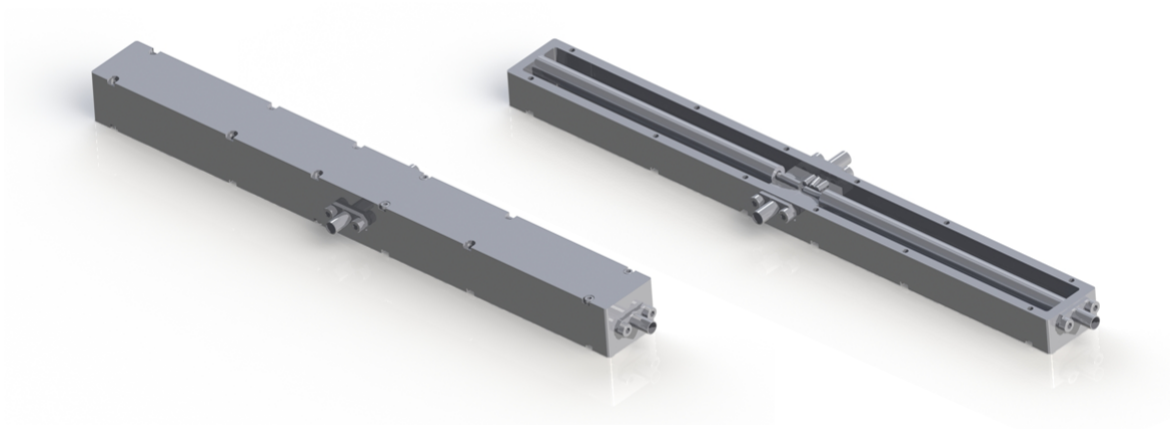


Figure 4.1: 3D model of the amplitude balanced combiner circuit.

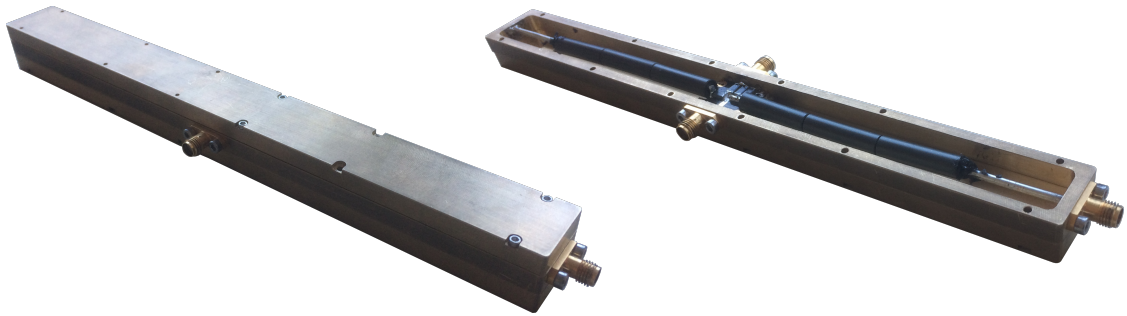


Figure 4.2: The constructed amplitude balanced combiner circuit.

4.3 Coaxial balun design

The balun used in the surface mount design does not appear to have a stable frequency response which causes an amplitude imbalance. Because of this, it was decided to design a custom balun with a better frequency response with the intention of making the input ports more balanced. A commonly used type of balun is the Marchand balun, which is known to have a wide bandwidth as well as very even phase and amplitude balance. The Marchand balun can be designed in planar configurations, but it will in this project be developed in a coaxial configuration for the simplicity of manufacturing the component by hand.

4.3.1 Coaxial balun theory

The function of the coaxial balun is exactly the same as the balun used in the previous design. The working principle is however different and it will be briefly explained in this section how it works.

In the top part of Fig. 4.3, the problem with going from the unbalanced characteristics of a coaxial cable to a balanced signal mode is illustrated. In a highly conducting material, the *skin depth* is very small. This means in practice that all electrons that flow on a conductor will be concentrated to its surface. In the coaxial

cable, this means that the electrons will be concentrated on the outer surface of the inner conductor, and the inner surface of the outer conductor. This causes the outer side of the outer conductor to act as a separate conducting path, making the 180° output ‘see’ a coaxial jacket connected in parallel with whatever load that is connected to it [22]. The so called Marchand balun solves this by connecting another, identical, piece of coaxial outer conductor to the 0° output, which balances the two ports. This is illustrated in the bottom part of Fig. 4.3.

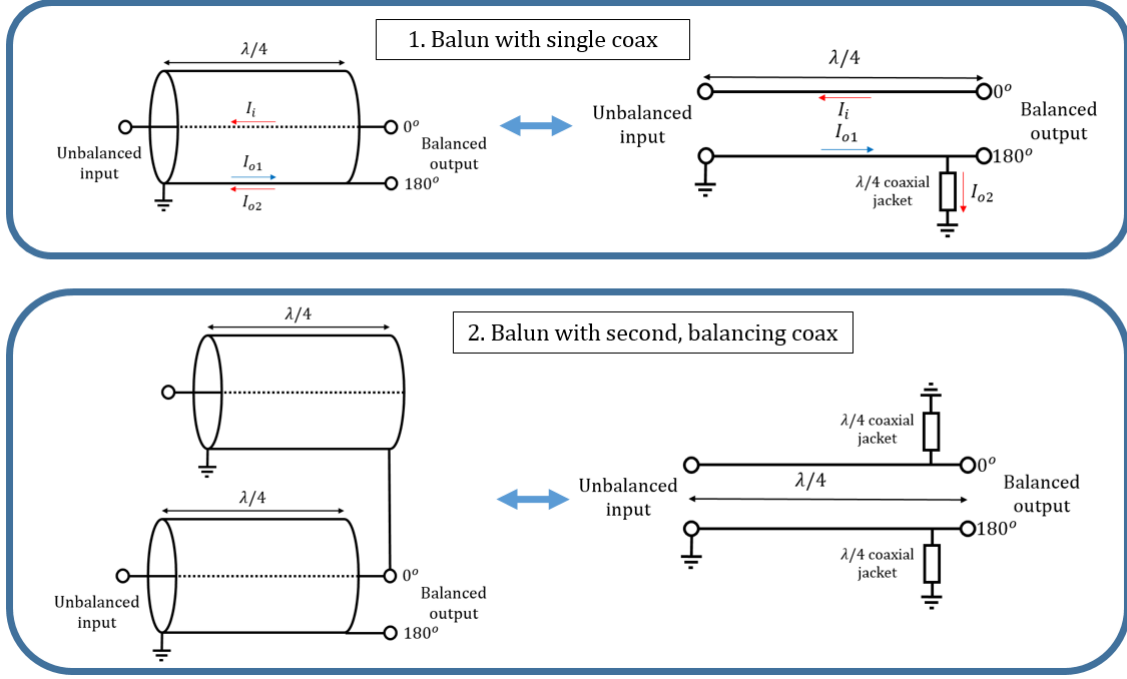


Figure 4.3: Conceptual illustrations of baluns with, and without, the second balancing coax.

To let currents escape on these outer conductors is however an unwanted effect as this still effectively acts as parallel impedances to ground on both the inner and outer conductor. Ideally these currents should be zero. This can be achieved by increasing these impedances to appear more like open circuits. One way to create such an effect is by loading the outer conductor with ferrite sleeves which makes this signal path highly inductive.

4.3.2 Balun measurements

To show the effects of the balancing coaxial cable and the ferrite sleeves, this section contains graphs that show the differences in the behaviour of the balun as each of these are added.

First the single coaxial cable balun was assembled and measured. The measurement setup and the S_{21} and S_{31} are illustrated in Fig. 4.4. This was followed by adding the second, balancing coax. The corresponding picture is found in Fig. 4.5. The slight frequency shift between ports two and three in Fig. 4.5 is due to small differences in length between the first and second coax.

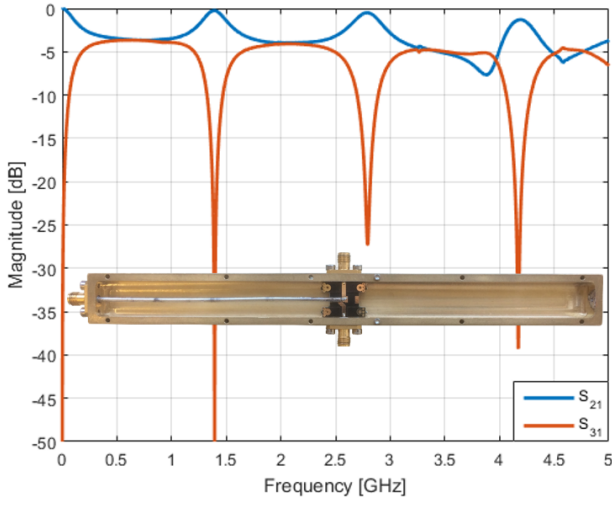


Figure 4.4: S_{21} and S_{31} of the single coax balun together with a picture of the setup. Port 1 is the common port.

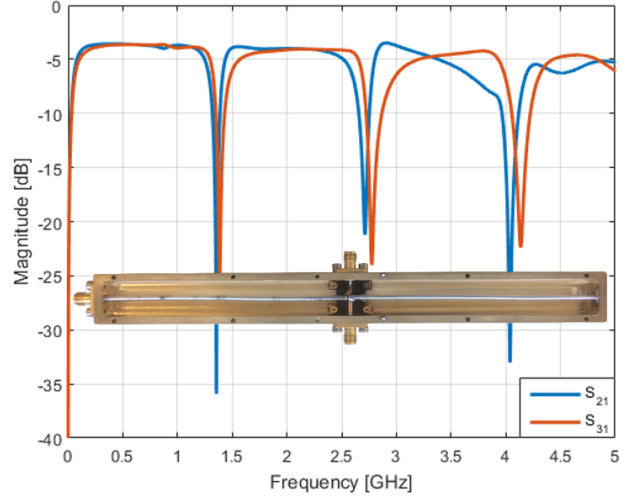


Figure 4.5: S_{21} and S_{31} of the balun when the second balancing coax is added, together with a picture of the setup. Port 1 is the common port.

A more typical way to measure the performance of a balun is to look at the differences between the S_{21} and S_{31} in terms of magnitude and phase. This difference that the balancing coaxial jacket makes can be observed in Fig. 4.6. It is clear that both the amplitude and the phase balance are improved by adding this component as both curves display a much more ‘flat’ behaviour when the part is added and are thus closer to an ideal balun. Note that I define the amplitude balance as

$$\text{Amplitude balance} = S_{21}[\text{dB}] - S_{31}[\text{dB}], \quad (22)$$

and the phase balance as

$$\text{Phase balance} = |\text{phase}(S_{21}) - \text{phase}(S_{31})|. \quad (23)$$

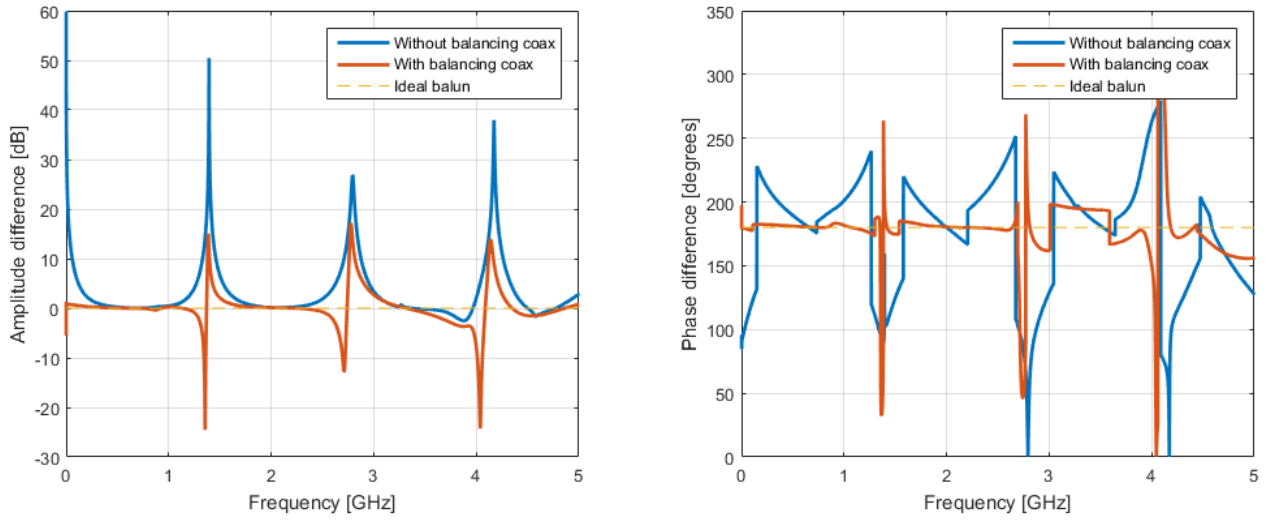


Figure 4.6: Amplitude and phase balance of the balun using a single coax, and with the balancing second coax. Note that an ideal balun has an amplitude difference of 0 dB and a phase difference of 180 degrees. Port 1 is the unbalanced port and ports 2 and 3 are the balanced ports.

The perfect differential output 500 MHz comes from how long the coaxial cables are chosen to be ($\lambda/4$). When the coaxial cables have exactly the length of a quarter wavelength, the outer layer of the coaxial jacket assumes an infinite impedance, and thus appearing identical to the 0° port. The reason to this can be explained with (19), where we again have a quarter-wavelength transmission line, which this time is terminated in a zero load. This causes the input impedance of the transmission line to assume an infinite value at exactly $\lambda/4$. At the same time, the opposite happens when the cables assume a half wavelength, meaning that the outer shield acts as a short at twice the center frequency.

To reduce the currents flowing on the outer side of the coaxial jackets for all frequencies, both coaxial cables were covered in ferrite beads. The behaviour of the circuit is extremely sensitive to the position of the beads, especially when they are moved close to the balanced outputs. One measurement of the ferrite covered marchand balun is illustrated in Fig. 4.7 together with the measurement setup.

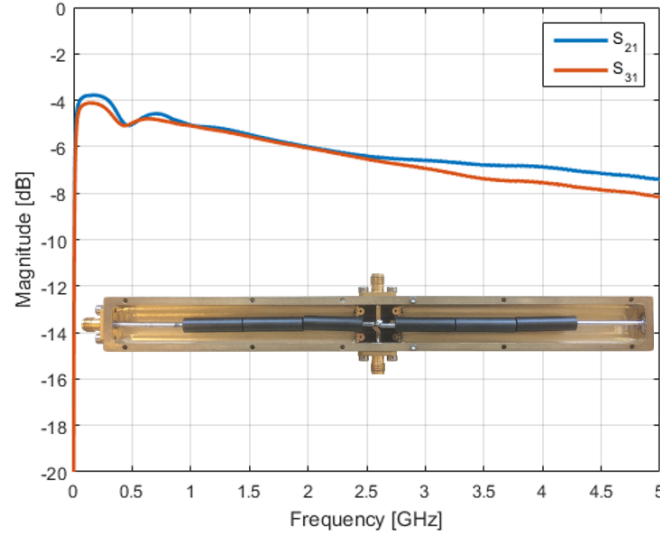


Figure 4.7: S_{21} and S_{31} of the balun when both coaxial cables are covered in ferrite beads.

A plot of the amplitude and phase balances in the same style as Figs. 4.4 and 4.5 is illustrated in Fig. 4.8. The amplitude balance has less than 1 dB difference and the phase is within 180 ± 4 degrees up to 5 GHz.

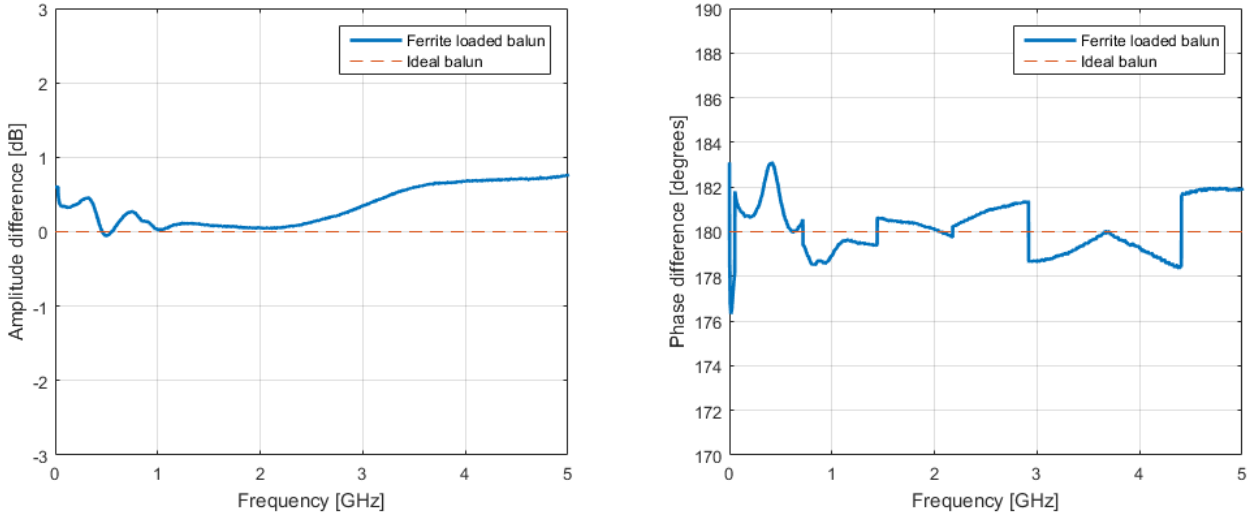


Figure 4.8: Amplitude and phase balance of the balun when covered with ferrite beads. Port 1 is the unbalanced port and ports 2 and 3 are the balanced ports. Note that the y-axes have significantly smaller scales than in Fig. 4.6.

4.4 Amplitude balanced combiner, simulations and measurements

Based on the very same combiner circuit as in the previous chapter, the full combiner was designed using the Marchand balun design. To make an estimate of the performance before assembly, the 3D-CAD model that was developed was imported into CST MWS for electromagnetic simulations.

No material parameters were available for the ferrite beads which lead to the decision of using material data from another ferrite under the assumption that they would be similar enough. No exact material data was available for the FR4 PCB substrate either and the resistors used in the circuit were again assumed to be ideal. A snapshot of the CST simulation 3D model is depicted in Fig. 4.10.

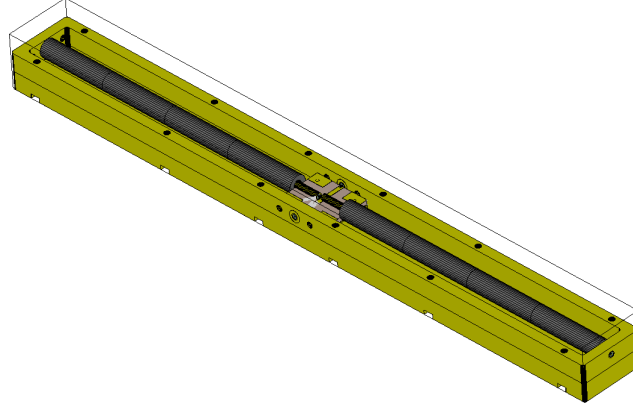


Figure 4.9: Snapshot of CST simulation of the balanced power combiner.

The full component was then assembled and tuned to the best possible result. The relevant results of the simulations and measurements are plotted in Fig. 4.10.

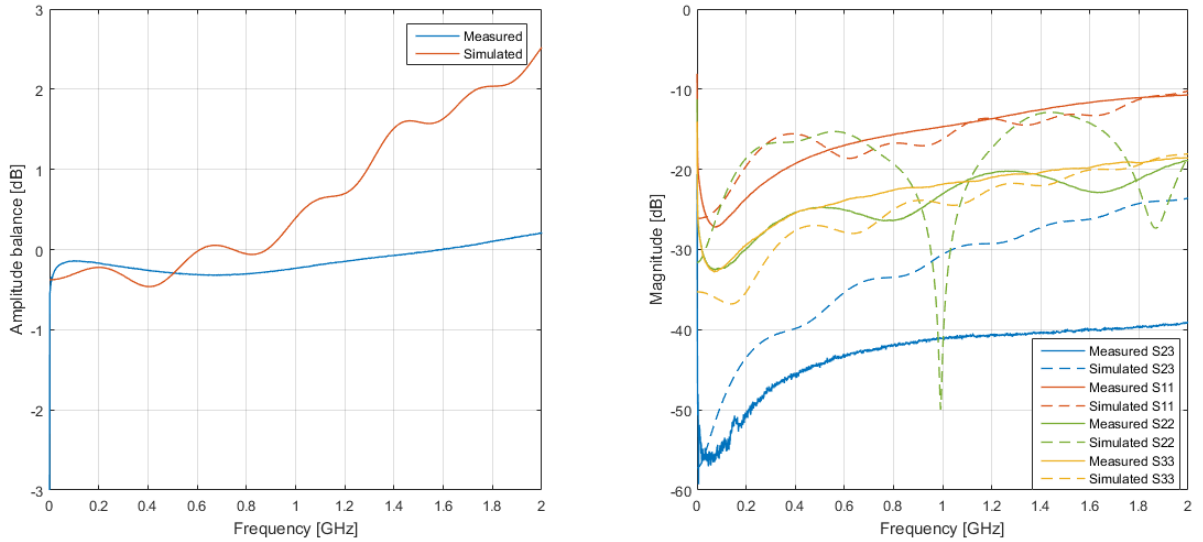


Figure 4.10: Simulation and measurement results of amplitude balance, reflections and isolation of balanced power combiner. Port 1 is the common port and ports 2 and 3 are the input ports.

The simulation has an overall good agreement with the measurement with the exception of the reflections at the second port. This is likely due to the uncertainties in the modelling of the different materials and also possibly due to the meshing of the very detailed 3D model.

The measured combiner component however behaves well and has an amplitude balance that is less than 0.4 dB difference from a few MHz up to two GHz.

4.4.1 Balanced combiner power dissipation

Finally, the power dissipation simulation was run on the balanced power combiner to find the accepted signal levels. The power rating is based on the assumption that the balun has very low losses. The results are plotted in Fig. 4.11.

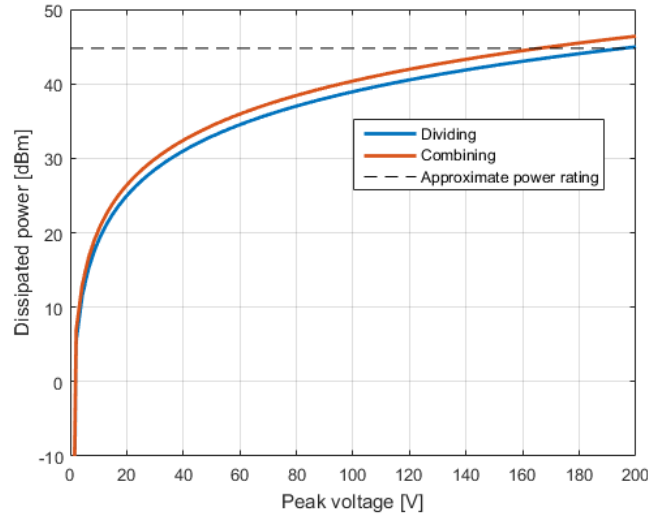


Figure 4.11: Total power dissipation in the balanced power combiner circuit versus peak voltage of the 12.5 ns repeating stripline pulse.

4.5 Amplitude balanced combiner discussion

The prototype amplitude balanced combiner shows results that may very well be sufficient for the final interlock BPM system. The measured divider that is presented in Fig. 4.10 has a difference in amplitudes that is smaller than 0.3 dB at the center frequency 500 MHz, which roughly corresponds to a 3.5 % difference in signal amplitude between the two ports. As one of the two channels is supposed to be delayed by 12.5 ns, this difference may well be reduced even further because of losses in this delay line.

The power dissipation in this component may be considered as more or less identical to the surface mount combiner and it should thus be able to handle input signals from bunches with intensities up to 3×10^{11} protons per bunch and a bunch standard deviation of 50 mm. This should however again be interpreted with caution as other parts of the component very well may break down due to heating. It is of high importance that this component is tested with real beam over a long period of time to check its reliability.

5 Analog signal chain

The full analog front end of the interlock BPM system needs to process the signals in a way that optimizes performance and accuracy on the digital side. This section investigates two key aspects that need to be considered when looking at the analog signal chain from a system perspective: Signal bandwidth and dynamic range of the signal levels.

5.1 Signal bandwidth

The fixed sampling rate of the ADC makes it undesirable to include frequencies above the *Nyquist* frequency, f_n , in the signal to be sampled. This frequency is exactly half of the sampling frequency, which in our case would be

$$f_n = \frac{f_s}{2} = 1.6 \text{ GHz.} \quad (24)$$

Any signals that exceed this frequency will be ‘folded’ in the frequency domain and recognized as frequencies lower than they actually are [23]. If these high frequencies are too large, it may affect the position measurements. In Fig. 5.1 there are time and frequency domain beam measurements of the filter. The frequency domain graph indicates that the signal already behaves in a very favorable way as most frequencies above 1 GHz are already heavily attenuated. This can be explained partly with the bunch shape and the response of the stripline electrode itself but also with the frequency response of the delay line filter as well as the low-pass characteristics that the long cable through which the measurement was taken has.

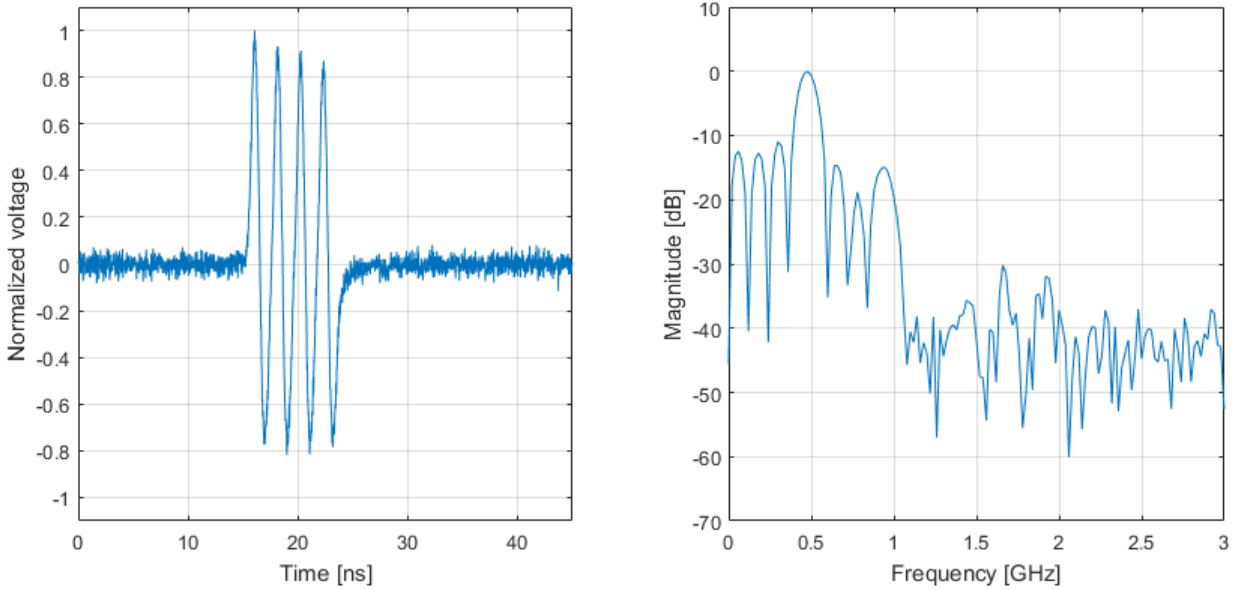


Figure 5.1: Time and frequency domain plots of a beam measurement of the filter.

5.2 Signal chain attenuation

The bunch intensities in the LHC have a wide dynamic range and the interlock BPM system should be able to operate with bunches from 1×10^9 up to 3×10^{11} charges per bunch. As the voltage signal from the electrodes scales linearly with the intensity, there is a need to be able to both actively amplify as well as attenuate the signal in order to use the most of the resolution of the 12 bit ADC. This section is dedicated to find the required levels of attenuation and gain and will be used as a basis for choosing the proper components.

In Fig. 5.2, a conceptual schematic of the analog signal path up to the point of the ADC is illustrated. Each passive component is labelled with an approximate attenuation level that can be used as a rule of thumb.

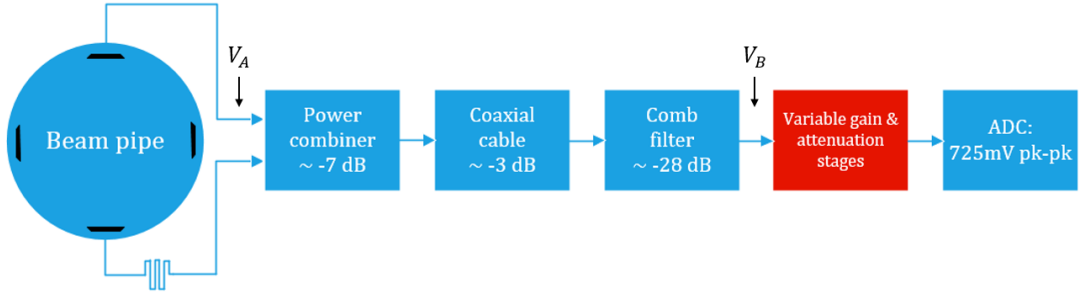


Figure 5.2: The analog signal signal chain of the interlock BPM system and the approximate attenuation levels of each component.

The approximate attenuation suggested in Fig. 5.2 is based on some assumptions and does not account for the frequency dependency in each component. To find the precise sizes of gain and attenuation stages, each of the passive components were modelled with their S-parameter models in ADS and the total attenuation could be found.

The coaxial cable was measured on-site with a VNA and later an ADS circuit model of said cable was implemented to simplify the simulations. The other two components - the initial power combiner and the delay line filter - already had S-parameter models available from previous measurements. The insertion losses from each of the three are illustrated in Fig. 5.3.

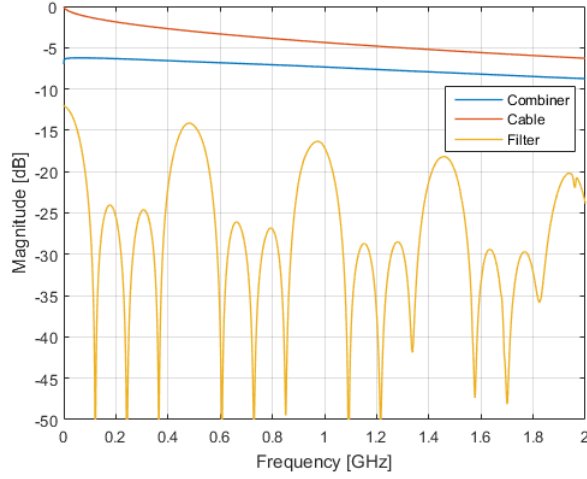


Figure 5.3: Transfer functions of the three main passive components in the analog signal chain.

5.3 Dynamic range of signal

5.3.1 Estimation

By using the same simulation as in section 2.3 about stripline electrodes, we can find the lowest and highest expected voltages at the starting point of the analog signal chain, V_A , defined in Fig. 5.2. By combining this with the approximate attenuation levels of each component, we can estimate the voltage ranges at the point after the delay line filter, V_B .

The lowest possible voltage from any of the electrodes occurs at a 1×10^9 bunch intensity and a displacement of 3.5 mm away from the electrode. The very highest possible voltage occurs at a 3×10^{11} bunch intensity and a displacement of 3.5 mm towards the electrode. The results are displayed in Tab. 5.1.

Intensity	Beam offset	V_A	V_B
1×10^9	-3.5 mm	0.5 V	0.0063 V
3×10^{11}	+3.5 mm	205 V	2.58 V

Table 5.1: Estimate of dynamic range of voltage levels.

5.3.2 Simulation

The S-parameter models of each passive component in the chain were used in an ADS simulation to get a more accurate picture of the signal range. The results are plotted in Fig. 5.4.

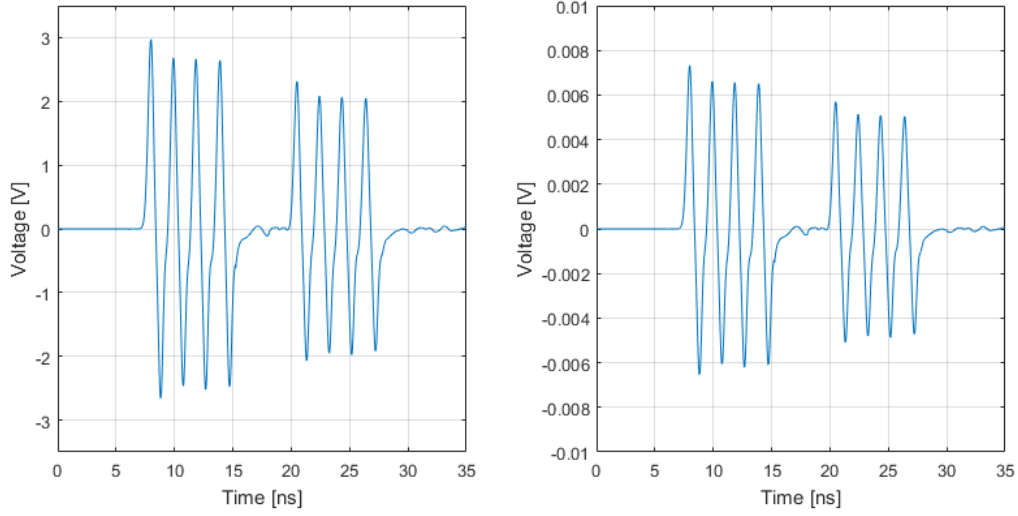


Figure 5.4: Simulated signals at the most extreme displacements of ± 3.5 mm. The left graph shows the output of the delay line filter at the very highest bunch intensity and the right one at the lowest.

5.4 Gain and attenuation stages

5.4.1 Amplification

The gain stage should ideally be able to amplify the lowest level signal up to the full 725 mV peak-peak range of the ADC. This corresponds to a gain of 57, which is 25 dB.

Additionally, the amplifier needs to have the capacity to produce the output power that is needed for the ADC. All signals propagate on $50\ \Omega$ transmission lines, which means that the maximum output power that would be required from the amplifier can be calculated as

$$\max(P_{\text{out}}) = \frac{V^2}{2Z_0} = \frac{\max(V_{\text{ADC}})^2}{100} = \frac{(0.725/2)^2}{100} \approx 0.0013\ \text{W} = 1.14\ \text{dBm}. \quad (25)$$

5.4.2 Attenuation

The attenuation stage should ideally be able to scale the highest level signal down to the full 725 mV peak-peak range of the ADC. This corresponds to a gain of 0.14, which is -17 dB.

6 Discussion, conclusions and outlook

Some of the essential hardware development of the new LHC interlock BPM system has with this thesis project been significantly advanced or finalized. The balanced power combiner and the delay line filter are two important components in the analog signal chain and they are now in a state where they can more or less be integrated into the system directly as long as the architecture does not change.

The balanced power combiner shows very promising results and the design is reliable and reproducible. What would be of interest and should be investigated in the future would be to see how the component wears down when used over long periods of time inside the LHC tunnel. Even though each sub-component through simulations has been confirmed to handle the input power from bunches with intensities up to some 3×10^{11} protons per bunch, it is difficult to say how other parts of the component wears down due to the heating that occurs. This kind of test would be critical to see if the component is suitable for the final interlock BPM system as this system has to operate without fault over long periods of time. It should naturally also be investigated exactly what the electrode signals look like when combined through this component with real beams, as simulations sometimes can be inadequate.

The results from delay line filter have also been successful and only some minor modifications to the delay lines may be necessary to achieve a more uniform and precise delay time between each pulse. There have been discussions about whether the two nanosecond delay is exactly what will be used in the final system and also whether the number of repeated pulses, four, could be reduced in order to improve the doublet bunch measurements as this would mean more samples that are not polluted (see section 3). This should be investigated on the software side: What there is to gain in terms of position measurements from such a modification in both the singlet- and doublet modes of operation? Some further work should also be made to see if the filter will have a detectable ringing when the signal is sampled with the system ADC instead of an external oscilloscope.

Appendices

A Filter proof of concept development

As a proof of concept and a first step towards the final design, a primitive prototype of the filter was developed using coaxial cables and ‘off the shelf’ commercial power combiners. The purpose of the prototype was also to be used as a tool for the development of the digital signal processing side of the new BPM system.

The power combiners used in this design are some high isolation power dividers called PBR0003 from Marki Microwave which come in a configuration with SMA connectors, depicted in Fig. A.1. Individual S-parameter models of each of the six dividers in the filter were created with an Agilent E5071C Vector Network Analyzer (VNA) in order to have accurate models of the phase curves, and thus the components’ influence on the signal delay, for simulations.



Figure A.1: The PBR0003 power divider in its SMA connector configuration. Image: [24]

The coaxial cables had to be cut and mounted to SMA connectors to be connected with the power dividers. The physical lengths of the cables that would produce the correct signal delay were determined using Eq. (26) [25], and were cut to the calculated length and tuned until the correct value was obtained.

$$L = \frac{\varphi}{2\pi} \lambda = \frac{c_0}{\sqrt{\epsilon_r} f_0} \frac{\varphi}{2\pi} \quad (26)$$

The prototype filter was assembled in a way that required as few cables to be manufactured as possible. A 3D model of the prototype filter is depicted in Fig. A.2.

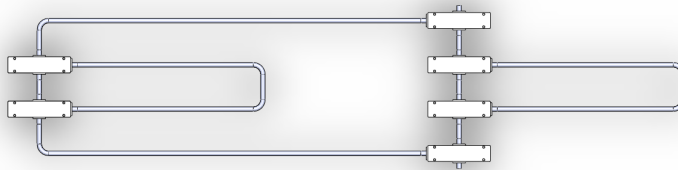


Figure A.2: 3D model of filter assembly.

B Power dissipation in a three port network

B.1 Introduction

This section is dedicated to calculating power dissipation given an S-parameter network and a certain time domain signal. This analysis is done in order to see how well the combining and dividing components presented in section 3.4 can handle the stripline electrode signals.

The power dissipation is investigated in both frequency- and time domain, and even though these two are completely analogous and should lead to the exact same results in theory, their implementation is somewhat different and error sources can appear in different places. The idea is to investigate both methods for some kind of redundancy and possibility to cross-check if each implementation is producing proper results.

As all calculations are made numerically there will be a certain amount of switching between analytic and discrete functions. For convenience I will keep the same names for both analytic and discrete representations of a single function, distinguishing them by the use of different brackets and their argument,

$$x(t) \rightarrow x[n], \quad (27)$$

where $x(t)$ is the analytic representation and $x[n]$ is the discrete representation and n is the n :th element in this data set. Additionally, I will also switch between frequency- and time domain representations of the same signals, where I will use the convention of using capital letters for frequency domain and small letters for time domain,

$$x(t) \xrightarrow{\mathcal{F}} X(\omega). \quad (28)$$

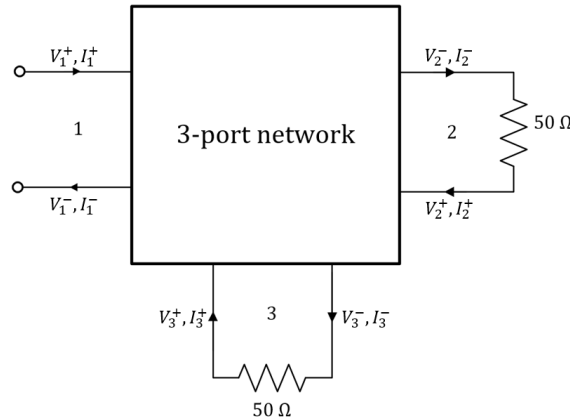


Figure B.1: A three port network with in- and outgoing current and voltage waves.

B.2 Frequency domain

The relations between all voltages on the connecting lines to our three port network may be expressed with the S-parameter matrix [26],

$$\begin{bmatrix} V_1^- \\ V_2^- \\ V_3^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \begin{bmatrix} V_1^+ \\ V_2^+ \\ V_3^+ \end{bmatrix}, \quad (29)$$

where the S-parameters are typically functions of frequency,

$$S_{ij} = S_{ij}(\omega). \quad (30)$$

In our case, the illustration in Fig. B.1, we know by definition that there are no reflections at ports two and three because of the matched terminations. Therefore,

$$V_2^+ = V_3^+ = 0 \quad (31)$$

$$I_2^+ = I_3^+ = 0. \quad (32)$$

We assume a known forward-going voltage wave on the transmission line that connects to port one, corresponding to the stripline electrode signal,

$$V_1(z) = V_1^+ e^{-jkz} + V_1^- e^{jkz} \quad (33)$$

$$I_1(z) = \frac{1}{Z_0} (V_1^+ e^{-jkz} - V_1^- e^{jkz}), \quad (34)$$

where Z_0 is the characteristic impedance of the line, which in our case is 50 Ω . The theory is all the same independently which port is used as input port and port number one is only used for the sake of the example.

Using equations (29) and (31), we can express the out-going voltages as

$$V_1^- = S_{11} V_1^+ \quad (35)$$

$$V_2^- = S_{21} V_1^+ \quad (36)$$

$$V_3^- = S_{31} V_1^+ \quad (37)$$

At this point we can define all the currents and voltages at each port using only the voltage input signal V_1^+ :

$$V_1(z) = V_1^+ (e^{-jkz} + S_{11} e^{jkz}) \quad (38)$$

$$I_1(z) = \frac{V_1^+}{Z_0} (e^{-jkz} - S_{11} e^{jkz}) \quad (39)$$

$$V_2(z) = V_1^+ S_{21} e^{jkz} \quad (40)$$

$$I_2(z) = \frac{V_1^+}{Z_0} S_{21} e^{jkz} \quad (41)$$

$$V_3(z) = V_1^+ S_{31} e^{jkz} \quad (42)$$

$$I_3(z) = \frac{V_1^+}{Z_0} S_{31} e^{jkz} \quad (43)$$

As we are interested in the average power, we can disregard the z -dependence and use $z = 0$ because a change in z will only correspond to a phase shift.

The time-averaged power travelling along a transmission line can be expressed as [27]

$$P = \frac{\operatorname{Re}\{V(z)I^*(z)\}}{2}. \quad (44)$$

Using this equation, we can express the average power at each of the ports:

$$P_1 = \operatorname{Re}\left\{\left(|V_1^+|^2(e^{-jk0} + |S_{11}|e^{+jk0}) \times (e^{-jk0} - |S_{11}|e^{+jk0})^*\right) \frac{1}{2Z_0}\right\} \quad (45)$$

$$= |V_1^+|^2 \left(1 - |S_{11}|^2\right) \frac{1}{2Z_0}. \quad (46)$$

Similarly for ports 2 and 3,

$$P_2 = |V_1^+|^2 \frac{|S_{21}|^2}{2Z_0} \quad (47)$$

$$P_3 = |V_1^+|^2 \frac{|S_{31}|^2}{2Z_0}. \quad (48)$$

The total power that is dissipated inside the three port network, P_d , is the power that is inserted into port 1 subtracted with the power that reaches (and escapes) through ports 2 and 3:

$$P_d = P_1 - P_2 - P_3. \quad (49)$$

This means that we can formulate the power dissipation as a function of frequency as the following

$$P_d(\omega) = \frac{|V_1^+(\omega)|^2}{2Z_0} \left(1 - |S_{11}(\omega)|^2 - |S_{21}(\omega)|^2 - |S_{31}(\omega)|^2\right), \quad (50)$$

with its corresponding discrete representation

$$P_d[n] = \frac{|V_1^+[n]|^2}{2Z_0} \left(1 - |S_{11}[n]|^2 - |S_{21}[n]|^2 - |S_{31}[n]|^2\right), \quad (51)$$

where it is assumed that each data set has the same distribution of points along the frequency axis.

Further, this expression may be written in the more general form

$$P_d(\omega) = \frac{|V_j^+(\omega)|^2}{2Z_0} \left(1 - \sum_{i=1}^N |S_{ij}(\omega)|^2 \right), \quad (52)$$

in the case where a signal is inserted into the j :th port of an N -port network.

The last step to implement Eq. (50) is to calculate the frequency domain representation $V_1^+(\omega)$ of the signal $v_1^+(t)$ that is at hand. This is done by using the Fourier transform [28]

$$V_1^+(\omega) = \int_{-\infty}^{+\infty} v_1^+(t) e^{-j\omega t} dt, \quad (53)$$

which in discrete form becomes

$$V_1^+[n] = \sum_{m=0}^{N-1} v_1^+[m] e^{-j\omega_n m}. \quad (54)$$

The Fourier transform is a standard operation and is implemented as a routine in many computational programming languages e.g. Matlab.

To finally determine the total power dissipation, we can derive an expression starting from the average power in the time domain using some arbitrary voltage signal $x[n]$,

$$P_{\text{avg}} = \frac{1}{N} \sum_{n=0}^{N-1} \frac{x^2[n]}{Z_0}, \quad (55)$$

and combine it with the discrete so called Parseval's relation which relates the signal and its transformation as [29]

$$\sum_{n=0}^{N-1} x^2[n] = \frac{1}{N} \sum_{k=0}^{N-1} |X[k]|^2, \quad (56)$$

which yields the total power dissipation

$$P_{\text{avg}} = \frac{1}{N^2} \sum_{n=0}^{N-1} P_d[n], \quad (57)$$

which corresponds to integrating the entire power spectral density.

An evaluation of the implementation of the frequency domain method is presented in Appendix D.

B.3 Time domain

Again assuming a certain set of discrete S-parameters $S_{ij}[n]$, we can inverse transform these functions to instead be represented as impulse responses $s_{ij}[n]$ in the

time domain. The inverse fourier transformation is defined as

$$s_{ij}(t) = \int_{-\infty}^{+\infty} S_{ij}(f) e^{j2\pi ft} df, \quad (58)$$

and in the discrete case

$$s_{ij}[n] = \frac{1}{N} \sum_{m=0}^{N-1} S_{ij} e^{j2\pi nm/N}. \quad (59)$$

The set of S-parameters for some component or circuit that is provided by a manufacturer is typically a single-sided spectrum, meaning that we only have the information for the positive frequencies. In order to obtain the proper real-valued time domain function when inverse transforming the set, it needs to be concatenated with its complex conjugated ‘mirror image’, corresponding to the negative frequency part. If we define

$$\underline{S}_{ij}[n] = S_{ij}^*[(N-1)-n], \quad (60)$$

where N is the number of points and $*$ represents complex conjugation, then the double-sided spectrum will be

$$\begin{bmatrix} S_{ij} \\ \underline{S}_{ij} \end{bmatrix} \rightarrow \begin{bmatrix} [S_{ij}] & [\underline{S}_{ij}] \end{bmatrix}. \quad (61)$$

Given the impulse responses, we can now perform what corresponds to Eqs. (35)-(37) in the time domain - a convolution:

$$v_i^-(t) = s_{i1}(t) \circledast v_1^+(t) = \int_{-\infty}^t s_{i1}(\tau) v_1^+(t - \tau) d\tau \quad (62)$$

$$v_i^-[n] = \sum_{m=0}^{N-1} s_{i1}[m] v_1^+[n - m]. \quad (63)$$

The convolution is also a standard routine in many programming languages and does not have to be implemented manually.

The instantaneous incident or reflected power at each of the ports is defined by

$$p_i^+[n] = \frac{(v_i^+)^2[n]}{Z_0} \quad (64)$$

$$p_i^-[n] = \frac{(v_i^-)^2[n]}{Z_0}. \quad (65)$$

Now to find the average power dissipation, we must calculate the mean of these data sets over our desired time interval with start- and end points N_1 and N_2 , respectively. I will define the mean as

$$\overline{p}_i = \frac{1}{N_2 - N_1} \sum_{n=N_1}^{N_2} p_i[n]. \quad (66)$$

We can now find the average power that is dissipated in the network analogously to the frequency domain expression, Eq. (49),

$$P_{avg} = \overline{p_1^+} - \overline{p_1^-} - \overline{p_2^-} - \overline{p_3^-}. \quad (67)$$

Just like the frequency domain method, this method has also been evaluated with a simple example in Appendix D and was found to work as expected.

C Implementation of power dissipation calculations and results

C.1 Introduction

In this section, the implementation of the theory from chapter B is presented with the computed results.

The input signal will be modeled in two different ways: First by assuming a simplified analytic signal and secondly by using an actual measured stripline pickup signal. For the measured pickup signal, both the frequency- and time domain methods are implemented for each of the two components that were presented in section 3.4 - the Wilkinson power divider and the PBR0003.

The filter will have two bottlenecks in terms of power consumption: The very first *splitting* element or one of the two first *combining* elements. The components are not necessarily symmetric in their operation and can have different levels of insertion loss depending on if they combine or split a signal. For example, in the case of the WPD, inserting a signal at the common port will in theory create a zero voltage difference over the resistor and thus create no dissipation. In the combining case, we will on the contrary *not* have this signal symmetry as there is only a signal coming in on *one* of the two input ports - the other one will be at zero voltage. This means that close to no power is dissipated in the delay line filter until the signal reaches the first combining element.

There is in principle no difference between calculating the power dissipation in the splitting and combining cases. It is only necessary to assume that one of ports two or three now is the input port instead of number one. Using port two as the input, Eq. (52) becomes

$$P_d(\omega) = \frac{|V_2^+(\omega)|^2}{2Z_0}(1 - |S_{12}(\omega)|^2 - |S_{22}(\omega)|^2 - |S_{32}(\omega)|^2), \quad (68)$$

and in the time domain, the corresponding Eq. (63) becomes

$$P_{tot} = \overline{p_2^+} - \overline{p_1^-} - \overline{p_2^-} - \overline{p_3^-}. \quad (69)$$

C.2 Analytic estimation

To get an idea of the order of magnitude of the power dissipation, a simplified analytic model was first implemented. Given a certain beam signal we can estimate the output voltage and thus the power dissipation using the analytic expressions for the stripline in section 1.3. We first assume a beam pulse with a sinusoidal shape that is similar (but not identical) to that from the simulation of the beam current,

$$i_b(t) = I_0 \sin(2\pi f_0 t) \times \left(u(t) - u\left(t - \frac{T_0}{2}\right) \right) \quad (70)$$

where $f_0 = 500$ MHz, $T_0 = 2$ ns, $u(t)$ is the Heaviside step function and I_0 is the current amplitude. What this is is essentially one single positive half period of a sine

wave. By performing the convolution between this signal and the impulse response of the stripline electrode, Eq. (7), we obtain the output voltage,

$$v(t) = z_T(t) \otimes i_b(t) = \int_{-\infty}^t z_T(\tau) i_b(t - \tau) d\tau = c_0 I_0 \sin(2\pi f_0 t) \times (u(t) - u(t - T_0)) \quad (71)$$

One of these cycles are illustrated in Fig. C.1.

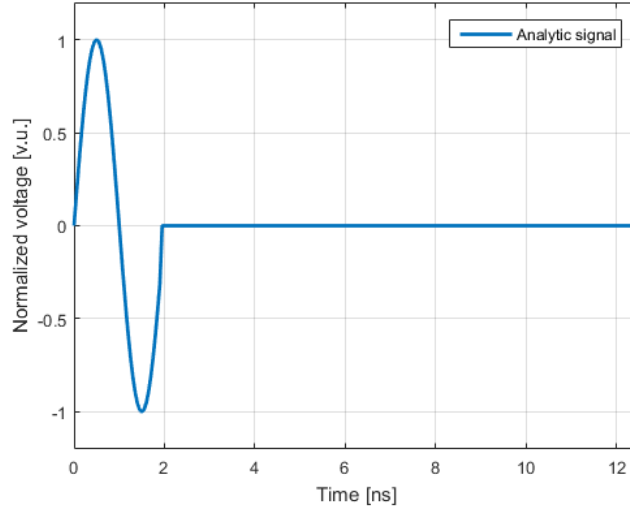


Figure C.1: Analytic input signal.

One way to approach the calculation of the power dissipation is to neglect the step functions in Eq. (71) and instead assume a continuous sine wave and multiply the power this signal would dissipate with the duty cycle T_0/T_p . The period $T_p = 12.5$ ns comes from the fact that the signal should repeat itself every 12.5 ns, see section 3. So, what I do is that I evaluate Eq. (50) at the desired frequency and multiply with this factor. This method is somewhat inaccurate because it assumes that the frequency spectrum is only non-zero for 500 MHz, which is in fact not true because of the abrupt discontinuity of the function at 2 ns - it is however only meant to be a simple initial model. In Fig. C.2, the power dissipation versus the input voltage is plotted. Note how small the dissipation in the splitting Wilkinson divider is - just as expected.

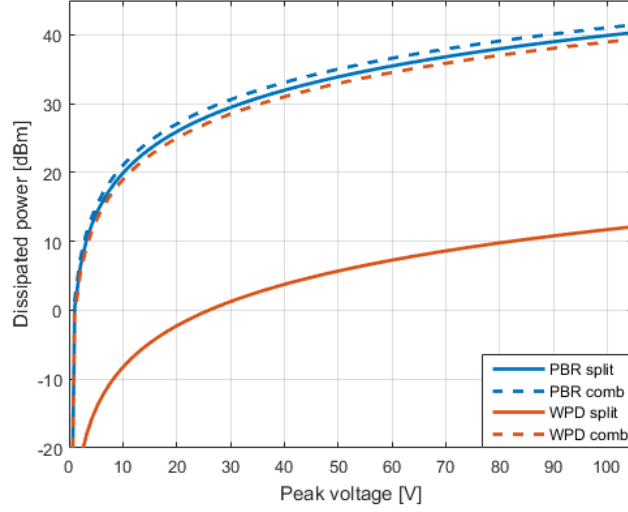


Figure C.2: Analytic input signal power dissipation.

C.3 Frequency domain simulation

In this section, the input signal that is used is instead the measured signal in Fig. 2.12. This should create a fairly realistic model of the power dissipation. For testing different voltage levels, the entire signal is simply scaled to the desired peak voltage.

In order to apply Eq. (50) and (68), we need to convert the time domain signal to a frequency domain one. However, to do the point-wise multiplication that we want to do between the input signal and our discrete sets of S-parameters, it is also necessary to make sure that we have the same distribution of samples along the frequency axis in each of these data sets. This can not be assumed to be the case and to solve this, it is necessary to re-sample either the signal or the S-parameter set, which can be done using for example built-in re-sampling functions in Matlab. In this case, the S-parameter data set was chosen to be re-sampled to the same rate as of the measured signal set.

In Fig. C.3, I have plotted the spectral density of the input signal. In other words, this is the average incoming power at each frequency on the feeding 50Ω transmission line.

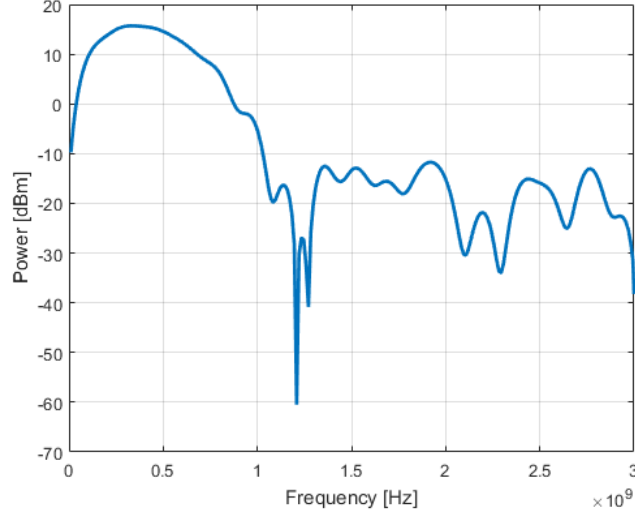


Figure C.3: Spectral density of the input signal when it is scaled to have a 30 V peak voltage.

Now by applying Eq. (50), we can find the spectral density $P_d(f)$ for the dissipation inside the three port network, which is illustrated in Fig. C.4.

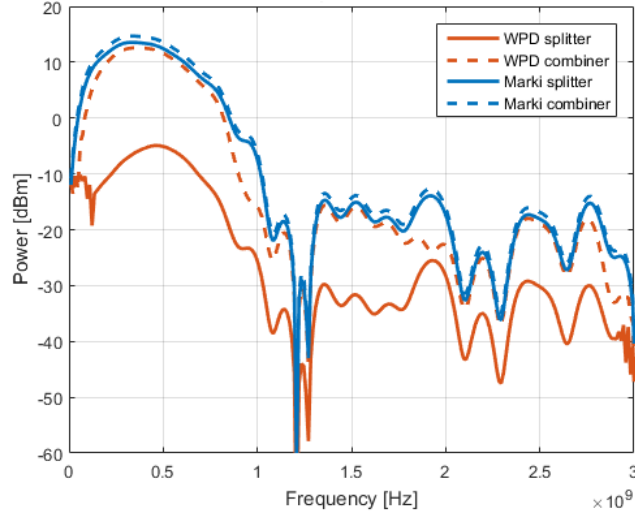


Figure C.4: Spectral density of the power dissipation for the same 30 V peak signal.

To find the total power dissipation, we need to integrate the spectral density over all frequencies, Eq. (57). The result of this integration as a function of peak voltage in the four different cases is illustrated in Fig. C.5. By comparing these results with Fig. C.2, we can conclude that the analytic model actually gives a good estimate of this more accurate, measurement based model.

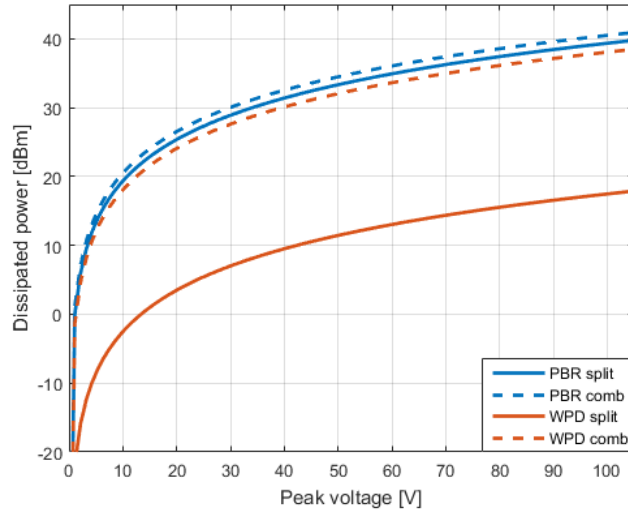


Figure C.5: Power dissipation as function of peak voltage in the frequency domain simulations.

C.4 Time domain simulation

For the time domain calculations, the same measured signal as the previous section was used for input.

Following the principles of Eqs. (58) - (61), we first calculate the time domain representation of the S-matrix - the corresponding impulse responses. In order to use the same measured input signal in Fig. 2.12, these impulse responses need to be re-sampled to the same rate of the measurement, or it is not possible to perform the convolution integral, Eq. (63).

As an example, in Fig. C.6 the convoluted signals are illustrated together with the input signal in the case when a signal is inserted into the common port of the PBR0003 divider. Here, the time shift of each convoluted signal is arbitrary relative to the input signal. This has no significance for further calculations as only the mean values are important.

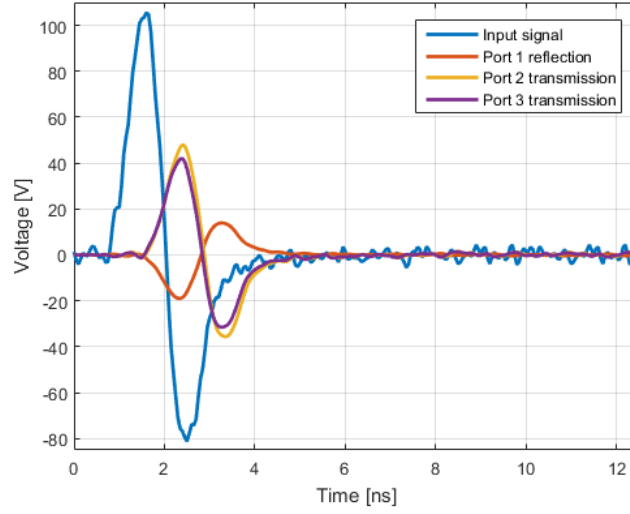


Figure C.6: Input voltage signal and the convoluted output signals in the splitting case of the PBR0003 divider.

To proceed, the instantaneous power waves that are inserted and leaving each respective port are calculated with Eqs. (64) - (65). These signals, Fig. C.7, are proportional to the square of the voltage waves and thus look similar to the absolute values of those in Fig. C.6.

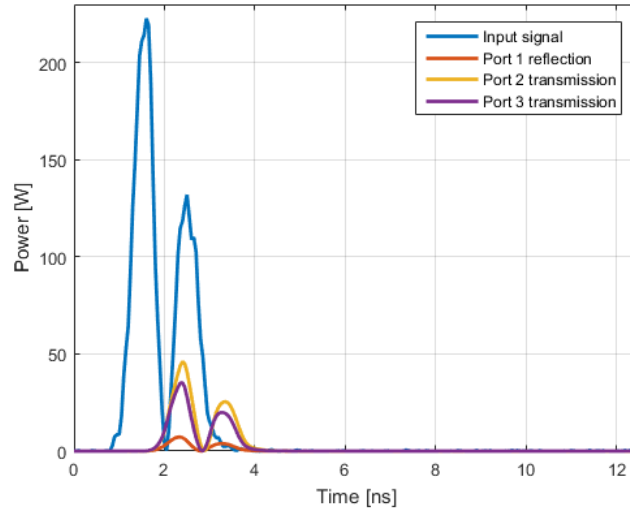


Figure C.7: Incoming power wave together with the reflected P_1 and the transmitted waves P_2 and P_3 in the splitting case of the PBR0003 divider.

Finally, Eqs. (66) and (67) are applied for calculating the mean power over the 12.5 ns time interval. The results are plotted in Fig. C.8. The curves correspond well with both those of the analytic estimation and the frequency domain simulation.

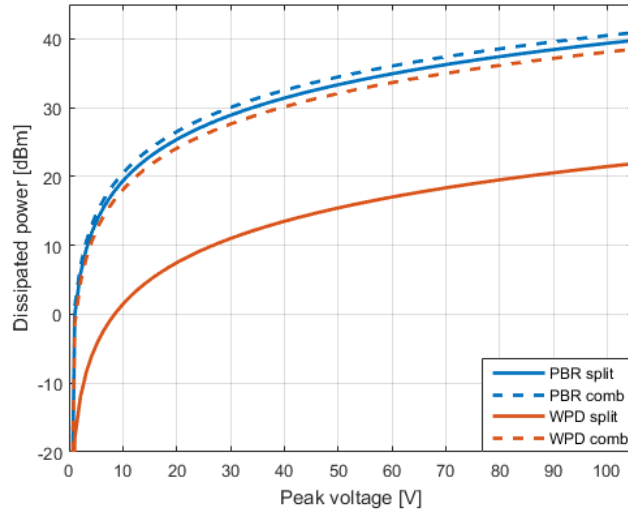


Figure C.8: Power dissipation as function of peak voltage in the time domain simulations.

C.5 Discussion about power dissipation results

The methods presented in Appendix B all produced similar results and when comparing the results to the reference simulation in Appendix D, it was indicated that the implementation was successful.

Looking at each of the curves that illustrate peak voltage versus power dissipation, it is evident that the PBR0003 circuit only can handle input voltages to a level of around 30 V, where it reaches its rated power of 30 dBm (1 W). This means that this component will not be a suitable choice as it may not be able to handle the signal levels that are required. The Wilkinson divider generally dissipates slightly less power and it is at the same time possible to actively design this component to handle higher power levels. This makes it the better option in terms of power handling capacity.

D Evaluation of methods for calculating power dissipation

In section B about power dissipation in a three port network, I present two different approaches for calculating the power dissipation given a certain set of S-parameters and a certain time domain signal. In this appendix, I want to show that my methods work as expected and that they produce reasonable results by comparing with results from commercial simulation software ADS. The reason to why this cross check was not done immediately in the power dissipation section was because the time domain solver in ADS does not seem to properly handle forward- and backward going power waves in some cases. This means that we cannot run a simulation where there are reflections going back into the probe that measures the power. To work around this issue, I have in this appendix set all values for S_{11} equal to zero and only considered the S_{21} and S_{31} .

The test is made by running a continuous 500 MHz sine wave with 1 V amplitude through the common port of a power splitter. In Fig. D.1, I have plotted the magnitudes of S-parameter set that I used in a linear scale.

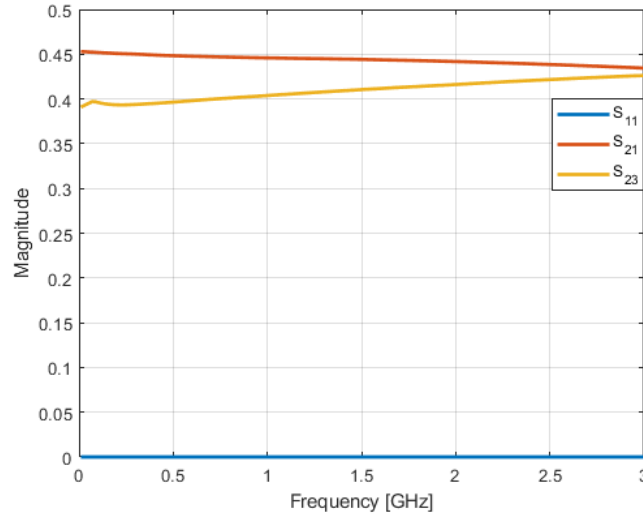


Figure D.1: PBR0003 scattering parameters - note that S_{11} has been set to zero.

As can be read from the graph, the parameters have the following magnitudes at 500 MHz:

$$S_{11}(f = 500 \text{ MHz}) = 0.000 \quad (72)$$

$$S_{21}(f = 500 \text{ MHz}) = 0.448 \quad (73)$$

$$S_{31}(f = 500 \text{ MHz}) = 0.396 \quad (74)$$

A quick calculation using Eq. (50) tells us that the total power dissipation in this case equals

$$P_{tot} = \frac{|V_1^+|^2}{2Z_0} \left(1 - |S_{11}|^2 - |S_{21}|^2 - |S_{31}|^2 \right) \approx 6.425 \text{ mW}. \quad (75)$$

The small deviations that can be seen between the different simulation results can be explained with the fact that each algorithm needs to re-sample signals in order to execute the calculations, which always will lead to a certain amount of deviation or error. All methods are within 2 % of the ADS simulation result.

D.1 ADS reference simulation

For reference, I ran a time domain simulation of the described setup in ADS. A screen capture of the simulation components is depicted in Fig. D.2.

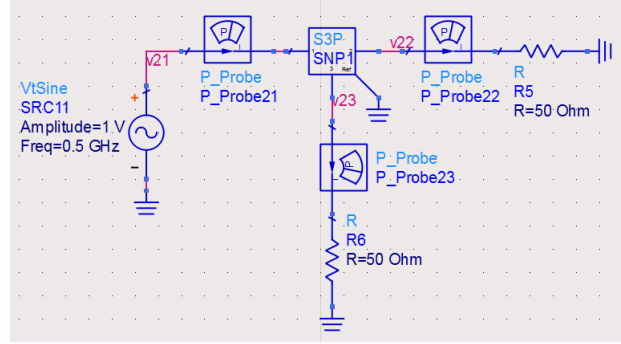


Figure D.2: ADS simulation setup.

The simulation produced the time domain power signals that are illustrated in Fig. D.3 and by taking the mean of this data as described in Eq. (66), a total power dissipation of 6.497 mW was calculated.

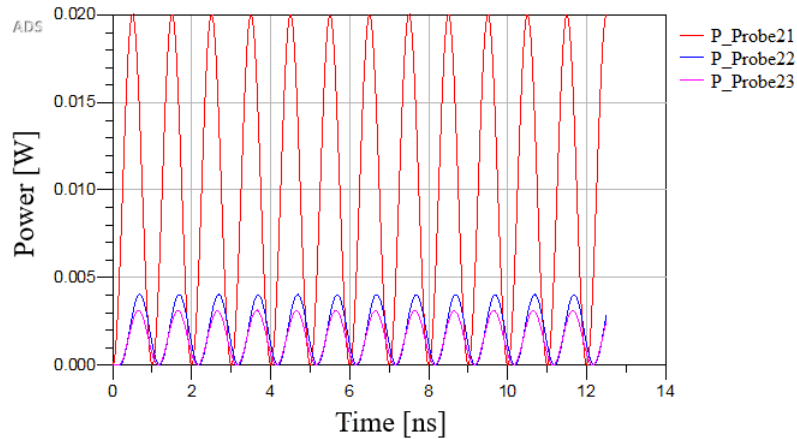


Figure D.3: Time domain power outputs for power probes 1-3, defined in the previous figure.

D.2 Frequency domain

Running this through my time domain implementation produces the power density spectrum illustrated in Fig. D.4.

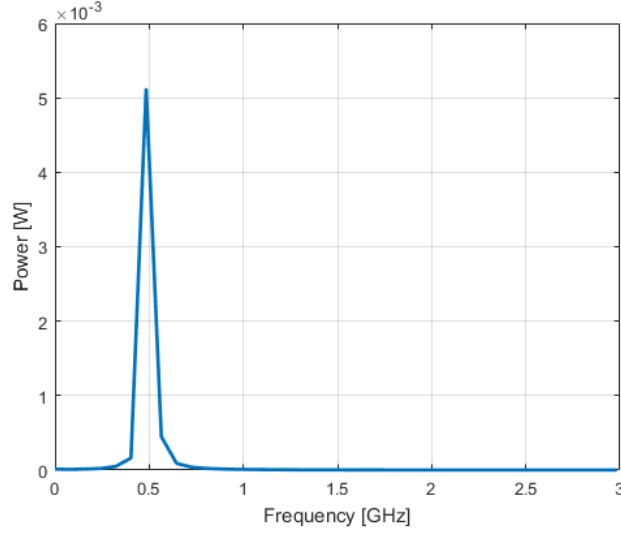


Figure D.4: Spectral density of power dissipation from 500 MHz sine wave through the common port of PBR0003.

Now taking the integral of this spectrum, in accordance with Eq. (57), produces a result of 6.382 mW.

D.3 Time domain

Running the same setup in my time domain implementation produces the out-going power waves P_1 to P_3 at each port that are illustrated in Fig. D.5.

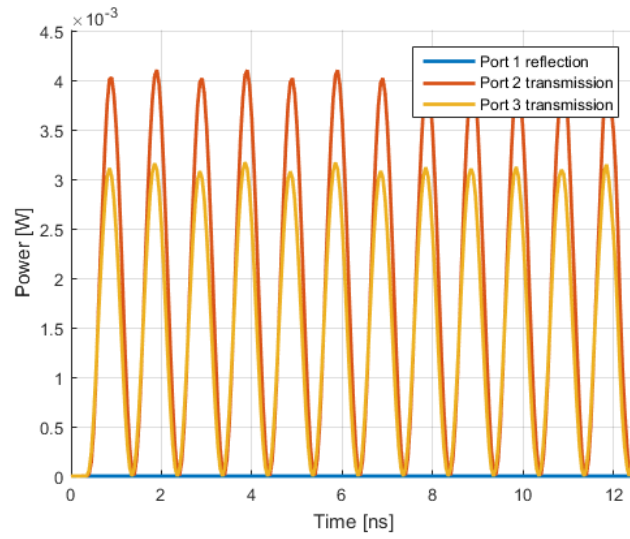


Figure D.5: Outgoing time domain power signals at ports 1-3.

Taking the mean of each of these signals and subtracting them from the incident power in accordance with Equations (64) - (66), the average power dissipation was calculated to be 6.368 mW.

E RF cavity resonant frequency

Using a closed, highly conducting metal casing for a microwave frequency circuit comes with the risk of exciting resonant cavity modes in the casing which may well interfere with the behaviour of the circuit. These resonant modes can be reduced and attenuated by introducing a damping material into the casing if necessary. In this section it is briefly investigated what the lowest possible frequency for such a resonant mode would be for the given geometry of the metal casing to see if a damping material could be useful.

We may consider a resonant cavity as a waveguide that has been closed by metallic plates in both directions. The complete electromagnetic fields of a waveguide mode in a perfect conductor can be written as [30]

$$\mathbf{E}_i(\mathbf{r}) = \mathbf{E}_{ti}(\boldsymbol{\rho})(a_i^+ e^{-jk_{zi}z} + a_i^- e^{+jk_{zi}z}) + E_{zi}(\boldsymbol{\rho})\hat{\mathbf{z}}(a_i^+ e^{-jk_{zi}z} - a_i^- e^{+jk_{zi}z}) \quad (76)$$

$$\mathbf{H}_i(\mathbf{r}) = \mathbf{H}_{ti}(\boldsymbol{\rho})(a_i^+ e^{-jk_{zi}z} + a_i^- e^{+jk_{zi}z}) + H_{zi}(\boldsymbol{\rho})\hat{\mathbf{z}}(a_i^+ e^{-jk_{zi}z} - a_i^- e^{+jk_{zi}z}), \quad (77)$$

where $\mathbf{E}_i$ is the electric field of the i :th resonant mode, with $\mathbf{E}_{ti}$ and E_{zi} being its transverse and longitudinal components. a_i^+ and a_i^- are the excitation coefficients and k_{zi} the longitudinal wave number of the i :th mode and $\mathbf{H}_i$ is the magnetic field.

We assume that the metallic plates are at the positions $z = 0$ and $z = d$. This means that the total transversal electric field must vanish on these surfaces:

$$\mathbf{E}_i \times \hat{\mathbf{z}}|_{z=0,d} = \mathbf{0}. \quad (78)$$

From this condition, at $z = 0$, it follows that

$$a_i^+ = -a_i^-, \quad (79)$$

which means that the transversal electric field is proportional to $e^{-jk_{zi}z} - e^{+jk_{zi}z} \propto \sin(k_{zi}z)$. At the other end of the waveguide, $z = d$, the condition becomes $\sin(k_{zi}d) = 0$, which implies that the longitudinal wave number takes the values

$$k_{zil} = \frac{l\pi}{d}, \quad l = 0, 1, 2, \dots \quad (80)$$

The entire wave number is given by

$$k_{il} = \sqrt{k_{ti}^2 + k_{zl}^2} \quad \begin{cases} \text{TM: } l = 0, 1, 2, \dots \\ \text{TE: } l = 1, 2, \dots \end{cases} \quad (81)$$

for TM and TE modes, respectively, whereas we can find the resonant frequencies from the relation $f = kv/2\pi$,

$$f_{il} = \frac{v}{2} \sqrt{\left(\frac{k_{ti}}{\pi}\right)^2 + \left(\frac{l}{d}\right)^2} \quad \begin{cases} \text{TM: } l = 0, 1, 2, \dots \\ \text{TE: } l = 1, 2, \dots \end{cases} \quad (82)$$

where $v = 1/\sqrt{\varepsilon\mu}$. If we assume that the metal casing is a perfectly rectangular geometry, we can use the transversal wave number of a rectangular waveguide:

$$k_{tmn} = \sqrt{\left(\frac{m\pi}{a}\right)^2 + \left(\frac{n\pi}{b}\right)^2} \begin{cases} \text{TM: } m, n = 1, 2, \dots \\ \text{TE: } m, n = 0, 1, 2, \dots \quad (m, n) \neq (0, 0) \end{cases} \quad (83)$$

where a and b are the width and height of the cross section, respectively. For the defined geometry,

$$a = 16 \text{ mm} \quad (84)$$

$$b = 12.5 \text{ mm} \quad (85)$$

$$d = 223 \text{ mm}, \quad (86)$$

which yields a lowest resonance frequency for a resonant cavity mode at approximately

$$f = 9.4 \text{ GHz} \quad (87)$$

for the TE mode with $(m, n, l) = (1, 0, 1)$. This is well outside the operating frequency of the component, which may make it unnecessary to include the damping material. It should also be noted that the ‘cavity’ is in fact filled with other metallic parts which will impose other boundary conditions on the resonances than the simplified ones assumed here. The calculated lowest frequency can however still be considered as a ‘worst case’ as any added metallic parts would decrease the physical space in which the resonances can form and thus increase the resonance frequencies.

F Printed circuit board design rules

F.1 Introduction

The final configuration of the delay line filter that will be installed in the upgraded interlock BPM system needs to be implemented using printed circuit board (PCB) technology to ensure its reproducibility.

It was decided at an early stage that it would be a good idea to design the filter in a stripline configuration. This is because a stripline transmission line is very well shielded from the outside as it has ground planes on both sides.

For optimal performance of an RF PCB design each component, transmission line, connection or transition need to be analyzed by the means of modelling and measurements. The design should to produce low reflections and ‘clean’ signals, as demonstrated in section 3.5.3 about signal ringing. This appendix is dedicated to finding some general guidelines that are useful for designing a layout that follows these criteria for the specific PCB setup.

All the investigations are made on a stripline transmission line setup that uses two layers of 1.52 mm Rogers RO4350B and a 0.1 mm thick Rogers RO4450F prepreg material which is used for adhering the two other substrates together. Material data is available in [21]. This setup was chosen based on previous experience within the department and that it was available for manufacturing.

F.2 Stripline characteristic impedance

The input impedances of the stripline electrodes are by design $50\ \Omega$. The characteristic impedance of any transmission line that is connected to this load must thus also be $50\ \Omega$ to be *matched*, that is, to minimize the reflections and to maximize the power transfer [31]. The characteristic impedance, often detoned Z_0 , is defined as the ratio between forward or backward going voltages and currents,

$$Z_0 = \frac{V^+}{I^+} = \frac{V^-}{I^-}, \quad (88)$$

or the square root of the ratio between inductance and capacitance per length of the line. The characteristic impedance is:

$$Z_0 = \sqrt{\frac{L_l}{C_l}}. \quad (89)$$

This impedance is dependent on the geometry of the transverse cross section of the transmission line. Three different methods for determining a geometry that produces the desired characteristic impedance were investigated. Using the characteristic impedance, the required boundary distance specified as d in Fig. F.1, could be determined.

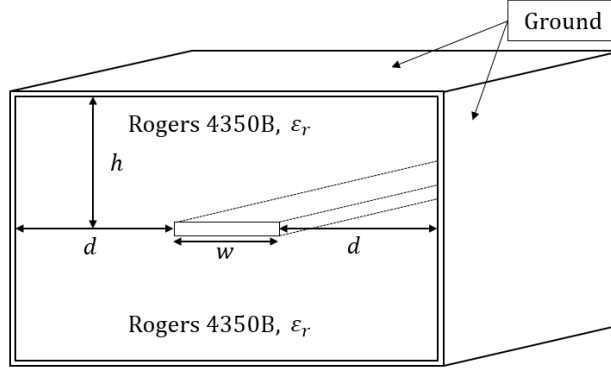


Figure F.1: Illustration of the stripline transmission line setup. $h = 1.52$ mm.

F.2.1 Analytic model

An analytic model for the characteristic impedance of a stripline transmission line is, as reported in [32],

$$Z_0 = \frac{\eta_0}{4\sqrt{\epsilon_r}} \left[\frac{1}{\frac{w/b}{1-t/b} + \frac{2}{\pi} \ln\left(\frac{1}{1-t/b} + \coth \frac{a\pi}{2b}\right)} \right], \quad (90)$$

where η_0 is the intrinsic wave impedance and t the thickness of the center conductor and

$$b = 2h \quad (91)$$

$$a = 2d + w \quad (92)$$

This method was implemented numerically and the parameters w and d were tuned until a solution was found. The results are displayed in Fig. F.4.

F.2.2 Electrostatic CST simulation

CST MWS is one of the most commonly used electromagnetic simulation softwares. Here the static solver was used to compute the total capacitance of a three dimensional geometry. By defining this geometry as a section of the transmission line with a certain length, we obtain the stripline capacitance per unit length, C_l , whereas the characteristic impedance can be computed using

$$Z_0 = \sqrt{\frac{L_l}{C_l}} = \frac{\sqrt{\mu_0 \epsilon_0 \epsilon_r}}{C_l} \quad (93)$$

where μ_0 and ϵ_0 are the permeability and permittivity of free space and ϵ_r is the relative permeability [32]. This method should be accurate for lower frequencies but because the dielectric constant of the materials varies slightly with frequency, [21], it may be less accurate when the frequency increases.

F.2.3 Time Domain CST simulation

In this case (and in all following CST simulations), CST's time domain solver was used, which essentially solves Maxwell's curl equations in a three dimensional space. The software automatically outputs the characteristic impedance of the line when using the time domain solver and when the line is excited using a waveguide port. Special care has to be given to making sure that the software uses a mesh grid that is fine enough to give accurate results. This can for example be tested by making several simulations with an increasingly dense mesh and see when the results start to converge. A snapshot of the simulation setup is depicted in Fig. F.2.

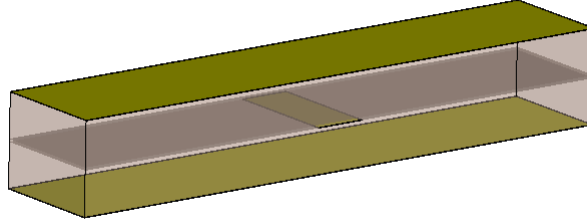


Figure F.2: Snapshot of time domain simulation for finding characteristic impedance.

F.2.4 PCB test

An additional test was made using real transmission lines. How well a transmission line is matched to a load can be measured by the reflection coefficient, Γ , which is defined by

$$\Gamma = \frac{Z - Z_0}{Z + Z_0}, \quad (94)$$

where Z is the actual impedance of the line and Z_0 again is the characteristic impedance. Γ is used to measure the ratio between the reflected and transmitted waves of a network and can also be defined as

$$\Gamma = S_{11} = \frac{V^-}{V^+}, \quad (95)$$

where V^- and V^+ are backward and forward going waves, respectively [33]. The test with real transmission lines was made on a PCB with five straight lines of equal length of 100 mm and varying trace width. Each line was measured separately and the reflection, S_{11} , was recorded for each of them. The widths were swept from 80 to 120 percent of a suggested trace width w_{50} that was determined from simulations. In Fig. F.3 the results of this test are illustrated.

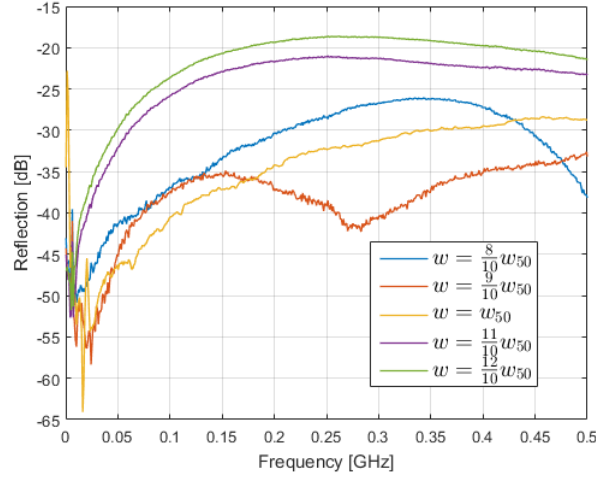


Figure F.3: Reflection measurements of striplines with varying widths.

For a transmission line that is matched to the load, the reflection should be as small as possible. The reflection, Eq. (94), is a function that has a minimum for $Z = Z_0$ and should thus increase for both $Z < Z_0$ and $Z > Z_0$. This behaviour can be observed in Fig. F.3 where the reflection is minimized for a trace width somewhere around $w = w_{50}$.

F.2.5 Characteristic impedance results and discussion

The trace width was varied in each of the three design methods until a characteristic impedance of 50Ω was obtained. It was found that a width of around 1.75 mm was required in all three cases. Further, it was found that the distance d , specified in Fig. F.1, needed to be around three times the trace width itself to ensure the proper characteristic impedance. This is illustrated in Fig. F.4. It should be noted that the analytic model assumes a homogeneous substrate material which is in fact not the case because of the thin layer of prepreg. The effect of this is however relatively small, which is obvious when comparing with the two simulated curves that do consider this.

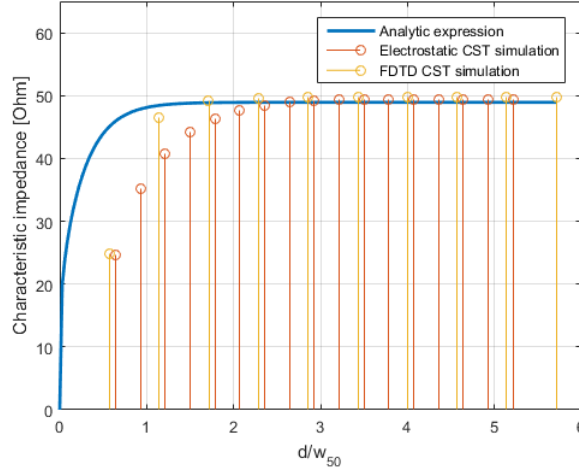


Figure F.4: Analytic and simulated impedance of the stripline transmission line as function of the distance d specified in Fig. F.1. $w_{50} = 1.75$ mm.

F.3 Stripline cross talk

Minimizing the size of a circuit board is always desirable because of production costs and often also because of limitations in size. This means that the components ideally should be squeezed together as closely as possible. In the case of an RF board, there must however be a trade off between the distance between two signal paths and the cross talk between them - that is, the level of signal that is coupled from one line to another. In this section, it is investigated how the isolation between two parallel stripline transmission lines depends on the distance between them.

Simulations were again made using the predefined stripline setup, and the distance between the two parallel transmission lines was varied to see the effect. In Fig. F.5 the geometry that was simulated is illustrated. The length of the two lines was chosen so that the coupling was maximized at 500 MHz. This is satisfied for a quarter wavelength.

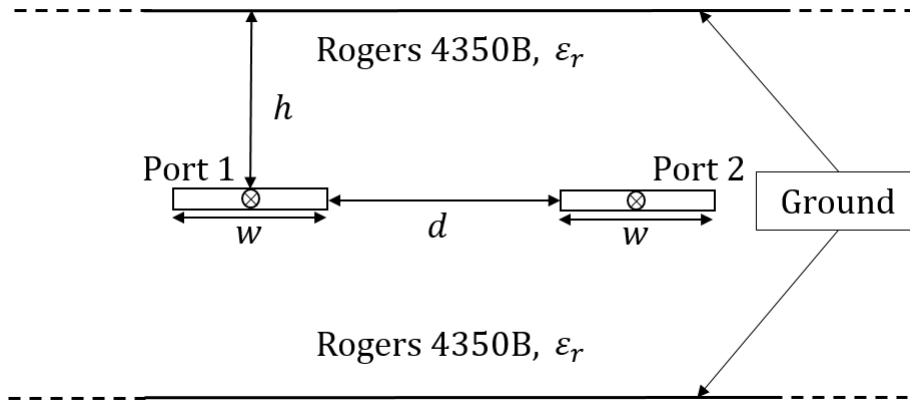


Figure F.5: Cross section of the geometrical setup for simulating crosstalk.

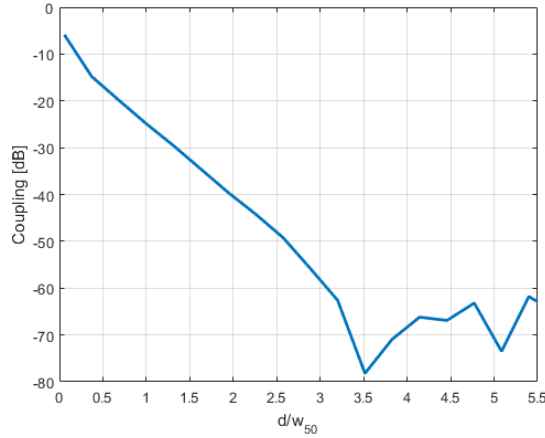


Figure F.6: The coupling ($|S_{21}|$) between two parallel $\lambda/4$ stripline transmission lines as a function of the distance between them at 500 MHz. $w_{50} = 1.75$ mm.

F.3.1 Cross talk discussion

The curve in Fig. F.6 shows the coupling between the two lines at 500 MHz as function of the distance between them. Somewhere close to three trace widths, the coupling is less than 0.1 % (-60 dB). A similar behaviour can be observed in Fig. F.4 in the section about characteristic impedance - at around three trace widths away, the characteristic impedance is practically no longer affected by the external geometry. Because of this, a distance of a of three trace widths was chosen as a minimum distance between two adjacent lines when designing the final layout. The fluctuations that can be observed above 3 mm are likely caused by accuracy limits of the simulation software. They can possibly be prevented to some extent by altering the simulation mesh. This was however deemed unnecessary as the relevant results already seemed to be present.

F.4 Stripline bending techniques

To limit the size of the PCB and for purely geometrical reasons such as the placement of connections to components the path of the transmission lines needs to be bent multiple times. If done incorrectly the bends may cause unwanted reflections and because of this, some investigations were made to find a bending method that was a good compromise between low reflections, size and geometrical simplicity. Two different geometries were investigated: A chamfered bend and a circular bend, illustrated in Fig. F.7. Each bend was isolated and simulated with CST Microwave Studio. Special care was given to making sure that the simulation results were valid, partly by looking at the excitation which is explained in each of the two following sub sections, and also by ensuring a fine enough simulation mesh.

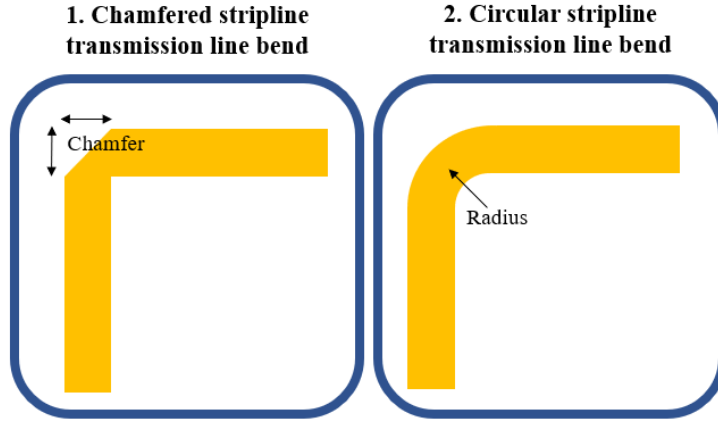


Figure F.7: Chamfered and circular stripline transmission line bend.

F.4.1 Chamfered bend

The amount of reflections in the transmission line was then investigated for different chamfer widths. Looking at Fig. F.8, it is possible to see that there is an optimal chamfer width that minimizes reflections somewhere between 2 mm and 3 mm. This is a well known result [34].

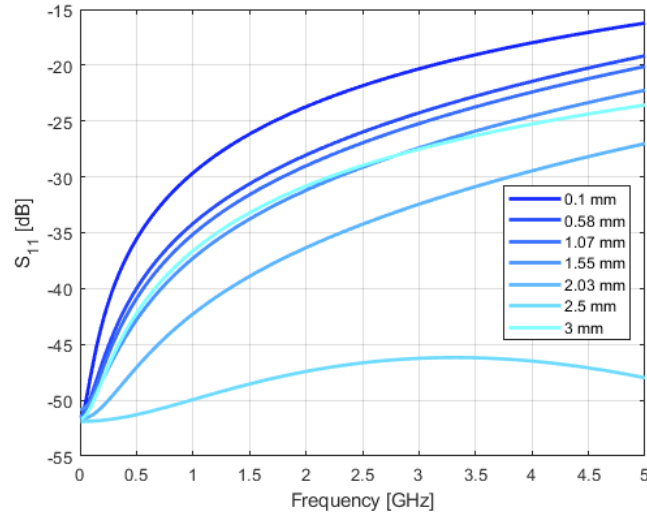


Figure F.8: Reflections in a chamfered bend for different chamfer widths. $w_{50} = 1.75$ mm.

F.4.2 Circular bend

The reflections were again simulated for circular bends with different radii and from the results in Fig. F.9, it is clear that the bigger the radius, the smaller the reflections. This result is intuitive as a bigger radius essentially approaches a straight transmission line which ideally produces no reflections.

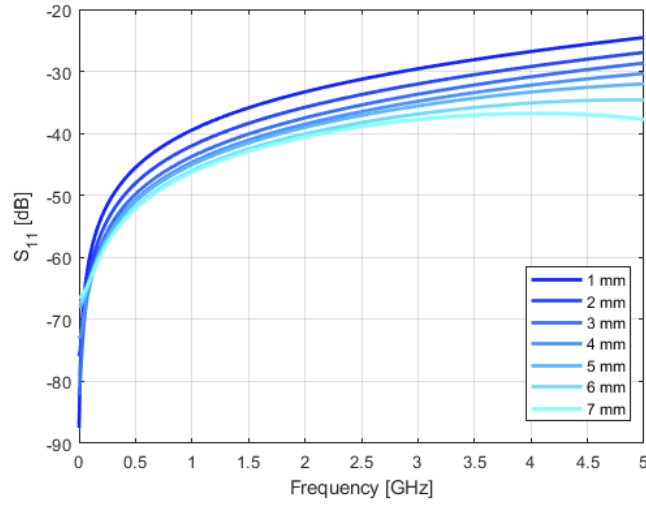


Figure F.9: Reflections in a circular bend for different bend radii. $w_{50} = 1.75$ mm.

F.4.3 Bending technique discussion

It should first be noted that although the simulations were made over 0-5 GHz, there is little interest in frequencies above around 1.6 GHz because of the signal bandwidth (see section 1.3) and the ADC sampling frequency. The most important interval to produce low reflections is around the center frequency of 500 MHz.

The results in Fig. F.8 show that when using a chamfered bend with a cut of approximately 2-3 mm, the bend is optimized to produce minimum reflections. It is however also a good option to use a circular bend with a bend radius that is large compared to the trace width, especially for lower frequencies. It is also more simple to describe the geometry of a circular bend with the modelling and simulation software that was used. Because of this, it was decided that the circular bend would serve the purpose best and that it should be used for all transmission line bends in the filter design. The largest circular radius that was tested was 7 mm, which means that the ratio between the trace width and the radius was $7/1.75 = 4$. This radius ensures less than -40 dB (1 %) reflections up until around 2 GHz. For some additional margin, all bends were designed to have a radius of at least five times the trace width.

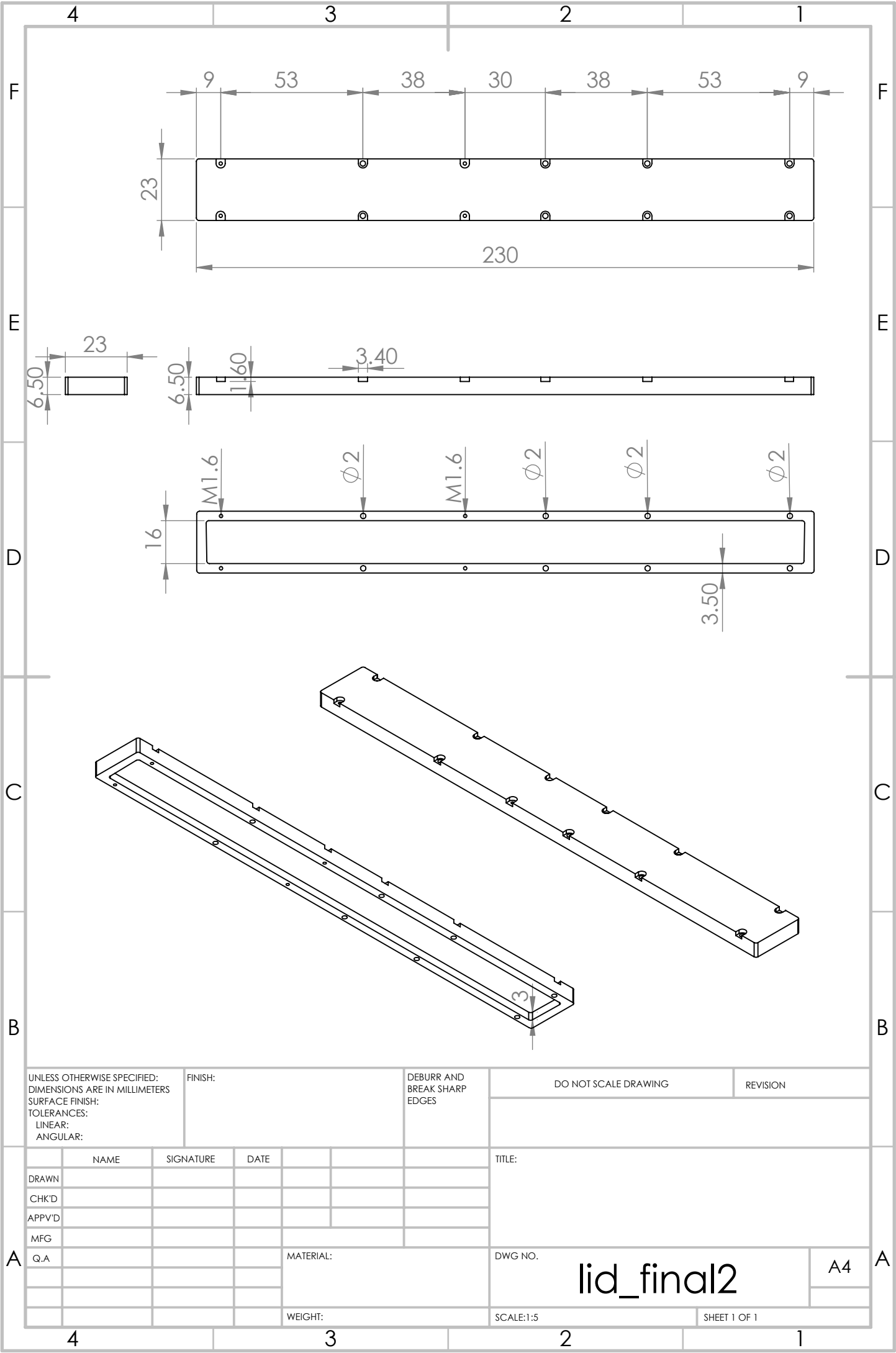
G PCB prototype photo



Figure G.1: Assembled prototype PCB.

H Balanced power combiner schematics

This appendix contains mechanical schematics of the balanced high power component.



UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN MILLIMETERS
SURFACE FINISH:
TOLERANCES:
LINEAR:
ANGULAR:

FINISH:

DEBURR AND
BREAK SHARP
EDGES

DO NOT SCALE DRAWING

REVISION

	NAME	SIGNATURE	DATE		
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CHK'D					
APPV'D					
MFG					
Q.A					

MATERIAL:

WEIGHT:

TITLE:

DWG NO.

SCALE:1:5

lid_final2

A4

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