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***Contributions to testing and characterization of
electronic devices with applications in
Large Hadron Collider (LHC) experiments***

- PhD Thesis -

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Sincerely,
Lucian-Nicolae COJOCARIU

Abstract

This work was done in the context of radiation hardness tests and qualification of the new read-out electronics chain for Ring Imaging Cherenkov sub-detectors part of the Large Hadron Collider beauty detector architecture. Precursory to the second-long shutdown of Large Hadron Collider, a challenging R&D campaign was focused on achieving reliable read-out electronic ready to be installed in the sub-detectors starting from 2018. An irradiation program was foreseen to investigate the radiation tolerance of dedicated integrated circuits designed for Cherenkov sub-detectors front-end board as well as commercial off-the-shelf components (COTS) considered for the digital architecture read-out electronics. The Romanian LHCb group was actively involved in RICH Upgrade Program evaluating the radiation hardness of MAROC3 ASIC along with an FPGA from KINTEX7 family. In December 2013, shortly after joining the group at Horia Hulubei National Institute for R&D in Physics and Nuclear Engineering, the author was responsible with the design and implementation of the automated test bench for online monitoring of circuits during the irradiation tests procedure.

Benefiting from a Summer School Program organized by European Organization for Nuclear Research in 2011, the author carried out the practical stage in the Micro Electronics Section testing and characterizing a 65 nm CMOS test chip. On this occasion, his interest expanded in the area of front-end electronics for detectors used in high energy physics experiments. They are by nature applications that require electronic devices capable to run in hostile environments with a hard radiation spectra, temperature fluctuation and magnetic field. Converging science and technology fields, the radiation hardness qualification procedure combines knowledge of radiation interaction with matter, nuclear and semiconductor physics, chip architecture and operation, circuit design, software, beam profiling plus high energy physics and nuclear instrumentation.

This thesis summarizes the work that has been done to evaluate the radiation tolerance of three integrated circuits, one is implemented in a 28 nm High K Metal Gate (HKMG) and the other two are in 0.35 μm SiGe technology node.

The first chapter provides an overview of the CERN accelerator infrastructure starting with a brief history of the organization and continuing with the physics program at the four main experiments on the LHC ring. A detailed description of the LHCb detector is given, especially of the RICH sub-detector upgrade program. The new photodetection system is presented together with the irradiation campaign for several integrated circuits.

The second chapter introduces the concepts of radiation effects in a semiconductor device with a brief overview of the domain terminology. The effects induced by radiation are depicted. Also, a summary of radiation hardening techniques is outlined.

The third chapter describes the MAROC3 chip architecture as well as the automated test benches designed and implemented for its radiation hardness qualification. Considered as a backup for the RICH photo-detection system front-end board, this integrated circuit is rad-hard by design and it was submitted for testing. Three samples have been irradiated using a 35 MeV proton beam. A dedicated section highlights the results of data analysis and interpretation.

The fourth chapter presents the SPACIROC2 chip architecture which serves as a blueprint for the next generation of the MAROC device family. This low power integrated circuit was designed for space applications to read out multi anode photomultiplier tubes on the Extreme Universe Space Observatory (JEM-EUSO). Inherited from MAROC3, the test bench was adapted for SPACIROC2 parameters online monitoring during irradiation tests. Its

radiation tolerance was investigated with a 200 MeV proton beam and the data recorded are presented as well as explained based on ASIC behaviour.

The fifth chapter is dedicated to the tolerance measuring and radiation hardness qualification of an FPGA from Xilinx KINTEX-7 family. It was proposed as the main component for the digital communication board of the RICH read-out chain. A test board was designed and implemented around the thinned dice of the device under test in agreement with radiation hardness constraints. Data monitoring is accomplished by means of an automated test bench assembled to run also for irradiation measurements within vacuum vessel. The device was tested under beams of heavy ions as well as proton and the results along with data analysis are presented in detail.

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List of abbreviations

ADC	Analog to Digital Converter
ALICE	A Large Ion Collider Experiment
ASCII	American Standard Code for Information Interchange
ASIC	Application Specific Integrated Circuit
ATLAS	A Toroidal Large Hadron Collider Apparatus
b quark	beauty quark
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BJT	Bipolar Transistors
BPSG	Borophosphosilicate Glass
BRAM	Block Random Access Memory
CDS	Control detector system
CERN	European Organization for Nuclear Research
CLB	Configuration Logic Bloc
CMOS	Complementary Metal–Oxide–Semiconductor
CMS	Compact Muon Solenoid
COTS	Commercial Off-The-Shelf
CP	Charged-Parity violation
CRAM	Configuration memory
CRC	Cyclic Redundancy Check
DAC	Digital to Analog Converter
DAQ	Data Acquisition
DCS	Detector Control System
DD	Displacement damage
DRAM	Dynamic Random Access Memory
DSP	Digital Signal Processor
DUT	Device under test
EC	Elementary Cell
ECAL	Electromagnetic Calorimeter shashlik type;
ECC	Error Correction code
ECR	Electron Cyclotron Resonance
EEPROM	Electrically Erasable Programmable Read-Only Memory
FF	Flip-flop

FPGA	Field Programmable Gate Array
GBT	Giga-Bit Transceivers
GOL	Gigabit Optical Link
GPIO	General-Purpose Input/Output
GUI	Graphical User Interface
HCAL	Hadronic Calorimeter
HEP	High Energy Physics
HIF	Heavy Ion Irradiation Facility
HKMG	High K Metal Gate
HL-LHC	High Luminosity Large Hadron Collider
HLT	High Level Trigger
HPD	Hybrid Photo Detector tube
I2C	Inter-Integrated Circuit interface
IC	Integrated Circuit
ICAP	Internal Configuration Access Port
IFIN-HH	Horia Hulubei National Institute for R&D in Physics and Nuclear Engineering
IT	Inner Tracker
JEM-EUSO	Japanese Experiment Module - Extreme Universe Space Observatory
JTAG	Joint Test Action Group interface
JULIC	Julich Isochronous Cyclotron
L0, L1	Level-0, Level-1
LDO	Low Drop Regulator
LEIR	Low Energy Ion Ring
LET	Linear Energy Transport
LHC	Large Hadron Collider
LHCb	Large Hadron Collider beauty
LHCC	Large Hadron Collider Committee
LEO	Low Earth Orbit
LLT	Low Level Trigger
LS2	Second Long Shutdown
LVDS	Low-Voltage Differential Signalling
M₁ - M₅	Muon station
MaPMT	Multi Anode Photomultiplier tube
MAROC	Multi Anode Read-Out Chip

MBU	Multibit Upset
MOS	Metal Oxide Semiconductor
MRAM	Magnetic Random Access Memory
n_{eq}	neutron equivalent
NIL	Non-Ionizing Energy Loss
OT	Outer Tracker
PCB	Printed Circuit Board
PDM	Photodetection Module
pe	photoelectron
PGA	Pin Grid Array
PID	Particle Identification System
PS	Proton Synchrotron
PS	Proton Synchrotron
PSB	Proton Synchrotron Booster
PSI	Paul Scherrer Institute
RF	Radio Frequency
RICH	Ring Imaging Cherenkov detector
SBU	Single Event Burnout
SC	Synchrocyclotron
SEE	Single Event Effect
SEFI	Single Event Function Interrupt
SEGR	Single Event Gate Rupture
SEL	Single Event Latchup
SEM IP	Soft Error Mitigation Core
SET	Single Event Transient
SEU	Single Event Upset
SiO₂	Silicon dioxide
SMPS	Switching Mode Power Supply
SPACIROC	Spatial Photomultiplier Array Counting and Integrating Readout Chip
SPD	Scintillator Pad Detector
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
T₁ - T₃	Tracking stations
TFC	Timing and Fast Control system

TID	Total Ionising Dose
TMR	Triple Modular Redundancy
TOTEM	Total Elastic and diffractive cross-section measurement experiment
TS	Tracking System
TT	Trigger Tracker
UART	Universal Asynchronous Receiver/Transmitter interface
USB	Universal Serial Bus interface
VCSEL	Vertical Cavity Surface Emitting Lasers
VELO	Vertex Locator system
VLSI	Very Large Scale of Integration

General introduction

Cutting edge applications in the area of wireless communications [1], broadband services [2], avionics, space stations and detectors for high-energy physics experiments [3, 4] rely on state of the art semiconductor device [5]. Following Moore's Law, the number of compact VLSI circuits obtained have increased as a result of the outstanding progress made in physics and production technology of semiconductor single crystals [6]. The semiconductor devices impairments [7] are driven by slight structural imperfections and insignificant concentration of impurities [8]. In harsh environments [9], especially those with ionizing radiation, damages occur in the electro-physical properties of semiconductors [10].

Over time, many research groups [11-15] carried out extensive studies meant to highlight the behaviour of electronic devices in the presence of ionizing radiations and the physical phenomena [16] occurring due to the semiconductor irradiation. The progress achieved by the physics of radiation-resistant semiconductors [17, 18] allows us to design reliable electronic devices [19] for extreme environments. Besides various radiation hardness tests made for qualification procedure, scientists invest a tremendous amount of work in developing software tools [20-26] intended to simulate electronic devices operating in environments with ionising radiation. The semiconductor devices lifecycle strongly depends on the spectrum of particles and energy distribution for each radiation environment [27]. Electronic devices experience radiation damages in environments like space [28], nuclear plants [29], high-energy physics experiments [30], including processing-induced radiation [31] and natural environment [32].

Space environments contain energetic particles [33] which can be found in the following main sources: electrons and protons trapped in the Van Allen belts [34, 35], heavy ions caught up in the magnetosphere [36], heavy ions and protons from solar flares [37], cosmic ray heavy ions and protons [38]. The radiation level for some of the listed sources is strongly correlated with the sun activity which has two cycles [39]. Typically, the cycles lasts on average 11 years with 7 years of solar maximum and 4 of solar minimum, but there have been reported cycles of 9 or 13 years [40]. The Van Allen belts consist of an inner belt [41] from 1000 to 6000 km and an outer belt starting from 13000 up to 60000 km [42]. In the inner radiation belt there are trapped protons with energies that exceed 100 MeV, also the high concentration of electrons with energy reach the range of hundreds of keV [43]. While for the outer belt, the radiation environment is given, mainly, by high-energetic electrons (0.1-10 MeV) [44]. In addition to this, the Van Allen belts have a small percentage of heavy ions like O^+ [45]. Regarding the inner radiation belt, it has an area known as South Atlantic Anomaly spread above the Earth surface in 0° to -50° latitude and between -90° to 40° degrees in longitude, situated to an altitude of 200-800 km [46]. This inner belt is dipping down at low altitude because the Van Allen radiation belts are symmetric to the Earth magnetic axis and offset with an angle of 11° of Earth rotation axis. The South Atlantic Anomaly taps and store charged particles originating from solar flare and coronal mass ejections as well as form cosmic-ray albedo neutron decay [46, 47]. This area consists mainly of electrons with energy range up to 10^2 keV and protons up to 10^2 MeV [48]. The South Atlantic Anomaly is a constant threat to the space systems running due to its dominant proton component which raises endless designing issues. The galactic cosmic ray particles have a low flux level and high energy starting from 10s of MeV up to 100s of GeV [49]. They originate from outside the solar system and include a wide range of heavy elements from atomic number 1 to 92. Consisting of around 85% protons, 14% alpha particles and 1% heavy ion [45], the galactic cosmic ray produce ionisation effects by passing through the semiconductor materials of

electronic devices. Solar flares occur especially during the solar maximum period and they can last for several hours or up to a few days generating heavy ions as well as protons with energies higher than 100 MeV [50].

Nuclear environment is characterised by very high doses and fluxes of neutrons and gamma particles [51, 52]. Special shielding for the reactor core and its environment is used to reduce the radiation level produced [53].

Processing-induced defects befall on semiconductor devices in fabrication phase which includes many processing steps that can lead to radiation-damages introduced by: the X-ray or e-beam lithography [54, 55], dry etching, ion beam milling, ion implantation, plasma enhanced chemical vapour deposition [56-58]. From the electro-physical properties of semiconductors viewpoint, the radiation damages that occur are much lower compared to the ones mentioned above. The Downscaling of electronic devices entails a higher vulnerability of the VLSI circuit at processing-induced radiations, especially in the case of ultra-thin gate dielectrics and spacer oxides [59].

Natural environment, beyond expectation, turned out to be a considerable radiation source inducing software errors in programmable device or perturbing data storage in memories [32]. Impurities contained by the device package, like thorium and uranium together with their daughter products, lead to the electronic device malfunction [60, 61]. The alpha particles are generated due to radioactive impurities which lead to software error in dynamic memories. Despite their low flux, the emitted alpha particles can be damaging for scaled down VLSI device [62]. Usually boron is used in the device fabrication process as p-type dopant in junction structures to enhance the flow properties and stress of SiO₂ layers [63]. This reactant has two isotopes, out of which the ¹⁰B one is instable and harmful, being exposed to thermal neutrons coming from cosmic rays. The ¹⁰B fusion process ends up by emitting alpha particles, gamma photons and ⁷Li nucleus [64, 65]. Studies of the Soft Errors Rate (SER) for non-BPSG integrated memory revealed results with one order of magnitude higher compared to similar SRAM devices implemented in 0.25 µm technologies using inter-metal layer of borophosphosilicate glass (BPSG), [66, 67].

Another radiation source is given by lead based isotopes found in the solder bumps of flip chip technologies [68, 69]. Therefore, the lead isotopes proved to be a source of radiation-induced failures for electronic devices even at the ground level, especially for those implemented beyond 100 nm fabrication technology [70]. Among the technical challenges faced with device downscaling, the soft errors in SRAM or DRAM memory caused by terrestrial low energy nucleon, muons and cosmic radiation become much higher with the increasing storage capacity [71-73]. Over the time various mitigation technique were developed to overcome soft errors induced by radiation, but still remain an open problem [74].

High-Energy Physics Experiments, particularly those carry on Large Hadron Collider (LHC) at CERN, demand electronic devices capable of reliable running into complex radiation field inside the collider tunnel as well as in the detectors experimental caverns (LHCb, ATLAS, CMS, ALICE and TOTEM) [75, 76]. Therefore, a hostile environment for electronic devices is caused by a huge particle rate with a high intensity coming mostly from the primary hadron-hadron interaction and also from LHC machine material activation. The mixt radiation field at LHC consists on hadrons with wide energy spectra from 0.025 eV (thermal neutrons) up to hundreds of GeV [77]. This represents a constant threat for the electronics embedded into CERN accelerator complex infrastructure [75]. Regarding the radiation tolerance of readout electronics for the LHC experiments, takes advantage of

valuable knowledge gained by the development of various space and defence applications for which the space agencies have databases with rad-hard electronic components. The radiation background on electronic devices in the LHC detectors is quite similar with the one from the Van Allen belt and this allow assessing the devices behaviour as well as semiconductor fabrication technology feasibility [78]. A comprehensive view of radiation background distribution for LHC has been achieved with particle transport code like FLUKA, GEANT4, GCALOR and MARS which are the Monte Carlo simulations [79-81]. The prediction results are cross-checked with the measured values provided by the online radiation monitoring system for the LHC machine and experimental caverns [82]. Over 400 radiation monitoring sensors, part of collider RADMON system, were installed in 2013 in the accelerator tunnel and adjacent shielded area [83]. The mixt-field radiation background inside LHC environment has two main sources. The first one is given by the proton-proton or lead-lead beams head-on collision inside detectors. Second one consists in distributed beam losses along the accelerator tunnel produced by interaction between protons and residual gas or materials surrounding the beam pipe [77].

In close proximity to the accelerated beams are elements such as beam screens collimators, beam dump (point losses), cryostats, magnets and cables. All these materials interacting with the proton beam from primary reaction lead to hadronic cascade consisting within secondary particles as proton, neutron, pion, kaon, electron and positrons. In their turn, some of this particles have enough energy to contribute to the production of tertiary particles, this phenomenon can continue on if resulting particle have enough energy [84]. Among hadronic cascade products are radioactive fragments of the nuclei that have a decay timescale ranging from a fraction of a second up to several days [85]. Consequently, remanent radiation [86] occurs and supply's the radiation background even when there are no circulating beams inside the tunnel. Studies were carried on as in [87] to evaluate the remanent dose in different material using Monte Carlo code FLUKA and the simulation results were benchmarked against measured ones from CERN-EU high-energy reference field facility. Experimental caverns and beam pipe tunnel mixt-field radiation environment raise reliability issues for electronics embedded in detector architecture. As example produced by colliding particle beams the hadrons (protons, pion, kaon) as well as neutrons may induce instantaneous effect by striking the sensitive volumes of the devices and upsetting their logic state or causing internal short-circuit, in worst case leading to a complete damage [88].

Particles like electrons, positrons and muons contribute to the cumulative radiation effects in electronics which experience an accelerated aging with the loss of performances [89]. Remanent radiation bring an important share to cumulative effects that influence the proprieties of device semiconductor layers and even induce bulk damages [90]. The main engineering constraint for the readout electronics and control systems in LHC accelerator complex is the radiation tolerance factor of semiconductor devices. Being used either Application Specific Integrated Circuits (ASIC) or selected and tested integrated circuits from Commercial Off-The-Shelf (COTS) device market [91]. The particle transport codes relaying on Monte Carlo simulation proved to be indispensable tools for mapping the complex radiation field in different region of LHC machine. Theirs outcome data represent a starting point in the environment parameterization and radiation hardness qualification requirements that need to be fulfilled by considered electronic devices meant to have a reliable operation. In the radiation hardness tests done to evaluate electronic devices radiation tolerance it is taking into account a safety factor at least three times higher than the value provided by simulation [92]. Over the time, several facilities were made at CERN to evaluate the semiconductor device radiation tolerance in mixt-field and the newest one is CHARM [93]. Radiation hardness assurance of electronics is mandatory for all electronic devices selected to be used in detectors architecture or other systems running in accelerator tunnel.

An Upgrade Programme is ongoing for the *Second Long Shutdown* (LS2) of LHC [94] which will start in 2018 and the goal is to improve the LHC detectors performances. Some sub-detectors of the LHCb machine will be upgraded as well as both Ring Imaging Cherenkov (RICH) system which will be rebuild to run at a beam bunch crossing rate of 25 ns [95]. Their photo-detection system will be redesigned using in the electronic readout architecture COTS devices and radiation-hard by design ASIC's. For this, it was foreseen an irradiation hardness qualification campaign to evaluate the radiation tolerance of electronic device intended to be used in the RICH readout. The Romanian LHCb group got involved in this irradiation campaign by caring out tests on a front-end ASIC MAROC3 and for a Field Programmable Gate Array (FPGA) from KINTEX-7 family of Xilinx.

In the following, it will be presented the work that has been done to evaluate the radiation tolerance of the devices mentioned above as well as the test benches specially developed for their online parameters monitoring during irradiation procedure. A third chip, SPACIROC2, was investigated since its radiation-hard design is the blueprint for the next generation of MAROC family. Irradiation tests were performed with mono-energetic beams and the data analysis results are given. Furthermore, for each chip the results are extrapolated to the LHCb detector nominal condition of radiation.

CHAPTER 1

LHCb at CERN

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1. LHCb at CERN

The European Organization for Nuclear Research houses a unique accelerator complex with four large experiments: ATLAS, CMS, LHCb and ALICE. A wide physics research program is ongoing, and detectors gather huge quantity of data from colliding protons or heavy ions. Exploiting the Large Hadron Collider capabilities at full potential and improving detectors data taking will be possible after the Third Long Shutdown in 2025. This chapter provides a brief history together with the description of accelerator infrastructure. In addition, an insight into the LHCb architecture is given. Finally, the new photodetection system of the two Ring Imaging Cherenkov sub-detectors will be presented in detail.

1.1 Introduction

Since mid-century, the European Organization for Nuclear Research contributes to pushing of the science boundaries considering the multiple technological breakthroughs and fundamental contributions in high energy physics experiments. Meant to align the European science at world class level, after the Second World War, the cornerstone for accelerator infrastructures occurred as a result of a few visionary scientists of that time like Niels Bohr, Raoul Dautry, Edoardo Amaldi, Lew Kowarski and Pierre Auger [96].

On the 9 December 1949, the French physicist Louis de Broglie addressed the European Cultural Conference, held in Lausanne, the first official proposal for achieving a European atomic physics laboratory. In December 1951, with the occasion of the UNESCO intergovernmental meeting, in Paris, the first resolution regarding the establishment of the European Council for Nuclear Research was adopted [97]. The acronym CERN (French: Conseil Européen pour la Recherche Nucléaire) appeared two months later, when an agreement was signed by eleven countries. The site of the CERN Laboratory was chosen in 1952 to be the city of Geneva. On 29 September 1954 twelve countries ratified the convention to settle CERN at the Meyrin site in Geneva, Switzerland and so earth excavation began only a few months later [97].

Marked by major projects, collaborations and scientific advances, the timeline of the CERN particle accelerators, associated with infrastructure required by a high-energy physics research, started in 1957 with the first accelerator built, a 600 MeV Synchrocyclotron (SC). This facility provided beams for experiments at CERN over 33 years. With the beam energy of 28 GeV, the Proton Synchrotron (PS) was in November 1959 the world's highest energy particle accelerator which continues to function until today [98]. A simple idea that revolutionized high energy physics experiments was colliding two proton beams head on. The project Intersecting Storage Rings has relied on this concept and lead to the construction of a new accelerator consisting from two intersecting rings feed with proton beam from the Proton Synchrotron. The world's first proton beams head on interactions were recorded at 27th January 1971. This scientific step leads to a new opportunity concerning the study of particle physics. In additions, this was the first accelerator that crossed the French-Swiss border [97].

The Large Hadron Collider (LHC) accomplishment would not be possible without valuable knowledge gained in over 13 years of Proton Synchrotron and expertise won from colliding beams head on. In average located at 100 m underground, this state of the art accelerator uses a circular tunnel with a 26.7 km circumference spanning between the Geneva International Airport and the Jura mountains in France [97].

In November 2009, two beams accelerated in the opposite direction with energy of 3.5 TeV were successfully circulated through the LHC ring. On 30 March 2010, for the first time two proton beams were collided at 3.5 TeV central-mass energy [98]. Furthermore, in 2012 data has been recorded for collision at 7 and 8 TeV leading to the Higgs boson finding [99, 100]. This discovery supports the Standard Model Theory [101] expounding the mechanism of interaction between matter building blocks ruled by four fundamental forces.

After the first Long Shutdown (LS1) ended in 2014, the LHC machine was upgraded to its nominal colliding energy of 14 TeV [102]. Currently, the CERN accelerator complex, schematically represented in figure 1-1, consist of six accelerators and one decelerator [103].

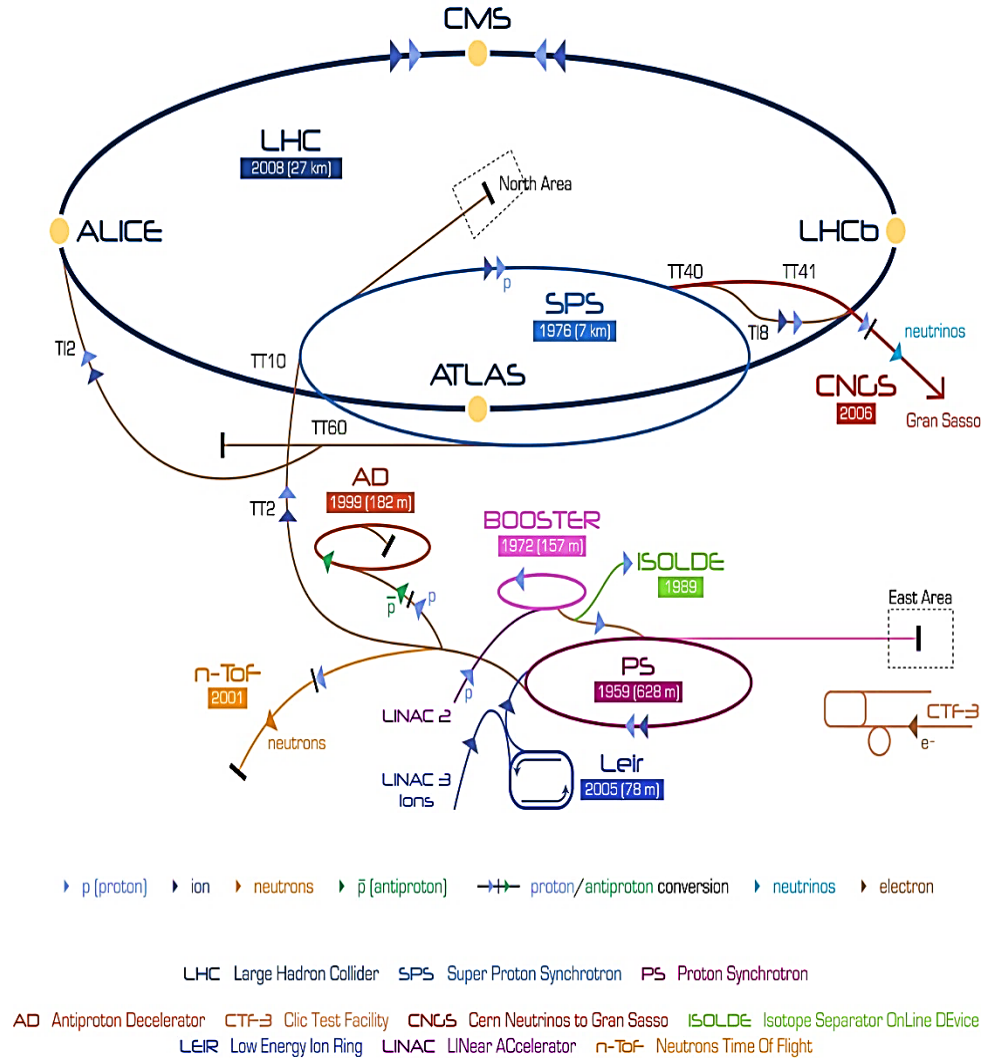


Figure 1-1 The CERN accelerators complex [106].

Finally, the protons are accelerated at a top energy of 6.5 TeV, which means 0.999999991 times the speed of light, began their journey through CERN's accelerator infrastructures by stripping away orbiting electrons of the hydrogen atoms [104]. A tank containing highly compressed H gas feeds with atoms, at a precise controlled rate, the Duoplasmatron source [105]. Resulted protons are accelerated initially by Linac2 accelerator up to 50 MeV, followed by the Proton Synchrotron Booster (PSB) which increases the proton beam energy up to 1.4 GeV [106]. After, the protons are accelerated at 25 GeV into the Proton Synchrotron (PS) and the beam is passed to the Super Proton Synchrotron it will reach even a higher energy of 450 GeV [103].

Also, lead ions are accelerated to allow hadronic particles production in collision at 1150 TeV centre-of-mass energy for the experiments conducted at CERN. The production of lead ions takes place into the Electron Cyclotron Resonance (ECR) source [105]. A sample of highly purified lead is heated at around 550 °C and an ingrowth lead vapour is ionized using an electron current. Produced with multiple charge states, the ions are accelerated into the Linac3 facility to energy per nucleon of 4.2 MeV/u. Subsequently a carbon foil is used to strip only the Pb^{54+} ion. The Low Energy Ion Ring (LEIR) accumulates and accelerates the Pb^{82+} beam to 4.2 MeV/u. Furthermore, the Proton Synchrotron increases the beam energy to 5.9 GeV/u. The beam is stripped a second time by a foil and the ions are transferred and accelerated into the Super Proton Synchrotron at 177 GeV/u [104].

The proton or ion beam energy is increased by each machine and passed to the next powerful one until arriving at the Large Hadron Collider (LHC). This amazing accelerator can accelerate two proton beams to a nominal energy of 7 TeV and lead ions to energy per nucleon of 2.76 TeV/u. In the LHC machine, the particles inside the vacuum tubes are manipulated using a complex system based on electromagnetic devices. Keeping the particles close to the circular orbits of the facility beam pipe is made possible by the dipole magnets while quadrupole magnets maintaining the beam focused. The electromagnetic resonators are used to accelerate allowing keeping the particles at constant energy by compensating the radiation energy loss. Three vacuum systems are utilized in the LHC machine, among them two for insulation of which one for the cryomagnets and the other for helium distribution line. The beams ultrahigh vacuum pressure goes down to 10^{-13} atmosphere in order to avoid collisions between accelerated hadrons with gas molecules inside the two beam pipes.

About 9600 magnets contribute at optimizing the beam trajectory. Inside the LHC machine a large variety of magnets are used such as dipoles, quadrupoles and even decapoles. The dipole magnets are superconducting electromagnets from niobium-titanium (NbTi), operating at 1.9 K to create a magnetic field of 8.7 T when 11700 A pass through them [104]. This high magnetic field allows the 7 TeV beams to be bended around the LHC 26.7 km ring, consisting of eight arcs and eight insertions. One arc has 154 dipole bending magnets. Concerning the insertion, it is made of a long straight section provided at each end with transition region named dispersion and suppressors. The insertion use can be for injection, beam cleaning, beam dumping and physics when beams are collided within detectors for experimental purposes. Depending on this, the straight section layout is linked to the insertion purpose. Between these two insertion points is a sector that represents the working units of the LHC.

Focusing the beams at an interaction point to the smallest size possible maximize the probability of colliding two protons head-on. Special magnets known as insertion quadrupoles are used to focus the beams at the collision points. In nominal operating conditions a proton beam in the LHC has 2808 bunches, each bunch containing around 10^{11} protons [104]. The time spacing between two consecutive bunches is 25 ns. In modern accelerators, the bunch structure is prompted by the radio frequency (RF) acceleration scheme. The accelerating cavity increases protons energy only when the RF field has a correct orientation at the moment when particles pass through the cavity. This occurs during an RF cycle at a precise specified moment. The LHC machine has eight superconducting cavities per beam operating at 4.5 K. One cavity can deliver an accelerating field of 5 MV/m and they are grouped in cryomodules of four units. Each beam goes through two cryomodules installed in a long straight section where the transverse inter-beam distance of the machine is 420 mm instead of 195 mm normal ones [104]. Therefore, ensuring a high luminosity, these cavities play an important role in maximizing the number of collisions by keeping the proton bunches tightly clustered together.

In particle physics the performance of an accelerator is quantified by the beam energy and the number of useful interactions known as events. A collider capacity to produce the require number of events is called luminosity. This represents the ratio between the numbers of interactions per second detected to the interaction cross-section. Therefore, the luminosity measurement unit is expressed in $\text{cm}^{-2}\text{s}^{-1}$. During the LHC run2, the experimental data was recorded for a nominal beam energy of 6.5 and luminosity of $4 \times 10^{32} \text{ cm}^{-2}\text{s}^{-1}$, while for 7 TeV the luminosity was $15 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ [107, 108].

There are four interaction points, on the two rings from the LHC machine accelerator, associated with four large experiments that have the following acronyms: ATLAS (A Toroidal Large Hadron Collider Apparatus), CMS (Compact Muon Solenoid), ALICE (A Large Ion Collider Experiment) and LHCb (Large Hadron Collider beauty).

Taking into account its weight of 7000 tons, a length of 46 m and with a height and width of 25 m makes ATLAS the heaviest detector ever build [109]. Being a general purpose detector as CMS, it is used to explore a wide range of physics, as Higgs boson, extra dimension and particles that may possible constitute dark matter [110]. The interaction point is located in the detector centre and the resulting charged particles have the paths bend, due to a huge magnet that creates an intense field which allows the measurement of their momentum. After the beams collide, the resulted particles are identified by recording their momentum trajectories and particle energy using six detecting subsystems arranged around the interaction point. Each protons bunch interaction implies the generations of a tremendous amount of data which is processed by an advance trigger system that decides to keep or not the event. In 2014 at the ATLAS experiment there were 174 institutions and 3000 scientists affiliated that bring their own contributions to it [110].

Although the CMS detector has the same physics program as ATLAS, the magnet system design is different as well as the technical solution of its implementation. This CMS experiment relays on a huge solenoid magnet around which the entire detector was built. The solenoid maximum magnetic field is 4 T. All the other mentioned detectors were built in their associate caverns, but the CMS detector was assembled at ground level in 15 sections and then lowered in his underground cavern. This unusual features led to the construction of a detector that is 15 m high, 21 m long and 15 m wide [111]. The CMS collaboration had in 2014 a number of 182 institutes affiliated involving a number of 4300 particle physicists [112].

ALICE is a detector for heavy-ions serving for the study of extreme energy densities and the physics for strongly interacting matter. This detector allows us to detect quark-gluon plasma which is a state of mater formed immediately after the Big Bang. Used for such studies, the detector weighs 669 tons with a height of 16 m, being in length of 26 m and 16 m wide [113, 114].

The LHCb experiment has as scientific purpose to study the differences between matter and antimatter by investigating the particle entitled “beauty quark” or simply “b quark”. From architecture stand point, the experimental data are taken with a series of sub detectors designed to record particles emitted forward relative to the collision point direction [115]. The experiment takes advantage of sophisticated tracking detectors which are movable and close to the beam in order to reconstruct the b quarks among other types of quarks. The detector has a weight of 5600 tons being 10 m high, 21 m long and 13 m width. In 2013 at the LHCb experiment were affiliated 66 institutes [115]. An upgrade program is ongoing for this detector and the final goal is to improve the trigger rate from 1 MHz up to 40 MHz. New electronics should be develop in order to cope with LHCb nominal conditions of radiation, temperature fluctuations and magnetic field [116].

1.2 Large Hadron Collider beauty experiment

The LHCb is an experiment at LHC with the purpose of searching the new physics by indirect evidence in the Charged-Parity (CP) violation [54] mechanism along with precise measurements of beauty and charm hadrons rare decays. A particularity in distinguishing these heavy flavour hadron from the background consists in their large lifetime, such as a 1.51 ps for B and a 0.41 ps for D^0 [117]. Such particles have a flight distance of a couple millimetres in most of the decay instances, as result of their large boost production in conjunction with lifetime.

Nowadays, the LHCb experiment takes advantages of the most copious source of B mesons in the world and contributes to the study of CP violation in B decay [118]. Observing the decay of such particle allows a deep perception into the matter structure and the forces governing the sub-atomic constituents. One year of data taking at LHCb, with luminosity of $2 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$, means around 10^{12} pair of bb will be produced in 10^7 s of the facility's total running time [119]. The first advantage of running the LHCb detector at this modest luminosity is motivated by the events occurring as result of single proton-proton interaction per bunch crossing. In consequence, the data are simpler to analyse compared to the situation where multiple primary proton-proton interactions are taking place. Beside this, at low luminosity the radiation damage is reduced in the sub-detectors front-end electronics operating close to the interaction point or beam pipe. Tuning the luminosity for LHCb detector is independent from other interaction points, which is possible by adjusting the beams focus at the interaction point.

In the LHCb detector the large numbers of b hadrons are exploited using a sophisticated trigger system based on requirements such as efficiency, flexibility and robustness. Reducing the B meson decay combinatorial background is conditioned by the invariant mass resolution as well as the excellent vertex and momentum resolution. Furthermore, the reconstruction of the B meson decay final states becomes possible with the reconstruction of electrons, muon accompanied by the protons, pions and kaons identification. All these are key channels for fulfilling the goals of the LHCb physics program. Ultimately, the tremendous quantity of data recorded demands an outstanding data processing capability relying on the detector data acquisition system connected through a high bandwidth data bus.

1.3 LHCb detector architecture

Heavy flavour physics program at the LHCb experiment investigate beauty (b) and anti-b hadrons, and therefore the slight differences between matter-antimatters. This hadronic pair production at high energies is predominantly in the forward or backward cone of the interaction point. The experiment takes advantage of a detector architecture acting as single-arm spectrometer with a forward angular acceptance starting from 10 mrad up to 300 mrad in the bending plane, while in the non-bending from 10 mrad to 250 mrad [120]. Located in Point 8 of the LHC, the LHCb detector has a geometry made of sub-detectors specialized in particles identification, trajectory reconstruction and momentum measurements. The LHCb detector cross-section view is presented in figure 1-2 assigning the right-handed coordinate system with a z axis along the beam pipe and the y axis along the vertical.

In the non-bending y-z plane is showed the warm diplo magnet, the beam pipe as well as the sub-detectors part of Tracking System (TS) and Particle Identification System. Detailed, the LHCb parts are:

- VELO – the Vertex Locator system, including a pile-up veto counter;

- TT – trigger tracker;
- T₁, T₂, T₃ – tracking station consisting of Outer Tracker (OT) and Inner Tracker (IT);
- RICH1, RICH2 – Ring Imaging Cherenkov sub-detectors;
- SPD, PS – Scintillator Pad Detector and Preshower;
- ECAL – Electromagnetic Calorimeter shashlik type;
- HCAL – Hadronic Calorimeter;
- M₁, M₂, M₃, M₄, M₅ – muon detection system.

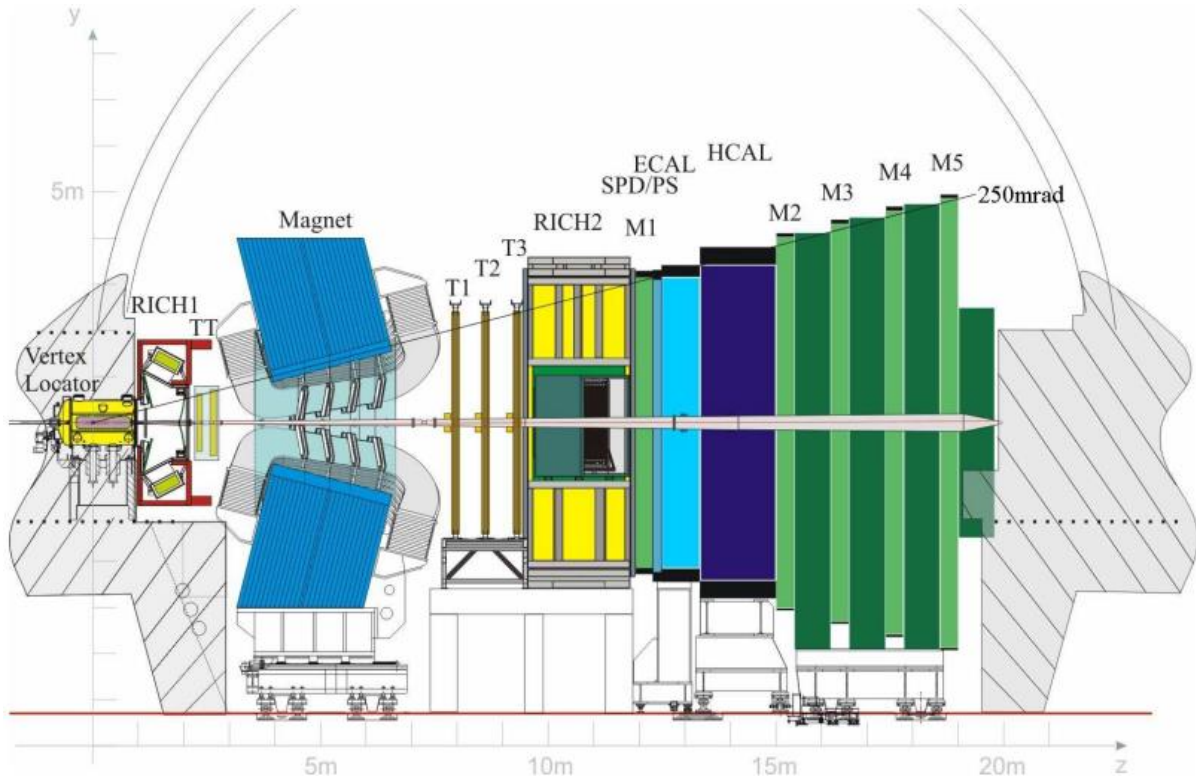


Figure 1-2 The cross-section of LHCb detector [21].

Many of the detector subsystems have been developed from design to be assembled in two halves that move out separately on horizontal. This constructive solution was chosen to ensure easy parts assembly and maintenance, allowing access to the beam pipe [119]. Another crucial aspect taken into account was the particles interaction with the detector material. The detection efficiency of photons and electrons is influenced by the LHCb machine material budget. Moreover, the pattern recognition together with the momentum resolution is diminished when pions and kaons undergo multiple scattering. Advanced software tools have been used to optimise the detector material budget based on realistic geometries for all the sub-detectors, including the vacuum vessel. The studies revealed that a particle with the tracking ending up right before RICH2 has crossed on average a detector thickness equivalent to 20% of an interaction length and 60% of a mediation length [121].

1.3.1 RICH sub-detectors and photodetection system

An essential key in the high-energy physics program at LHCb is the ability to provide particle identification for b hadron decays. The final state particles are pions, kaons and

protons, in case of these decays. Particle identification is carried out combining the particles velocity measurements with the momentum information, allowing further the mass calculation of individual particles [98, 122-127]. The tracking system measures the particles tracks curvatures in the magnetic field and, therefore, their momentum. For velocity measurements the Ring Imaging Cherenkov detectors (RICH) are used. Their principle of operation relies on the Cherenkov radiation.

The Cherenkov effect is given by charged particles that passes through dielectric material with a speed greater than the phase speed of light in the same medium and photons are emitted [128].

$$v_p > c_m = \frac{c}{n(\omega)} \quad (1.1)$$

Where:

- v_p - the speed of the particle through the dielectric material;
- c_m - the phase speed of light in the same medium;
- c - the speed of light in vacuum;
- $n(\omega)$ - the dielectric material refractive index expressed, in general, as a function of the frequency (ω) corresponding to the emitted photons.

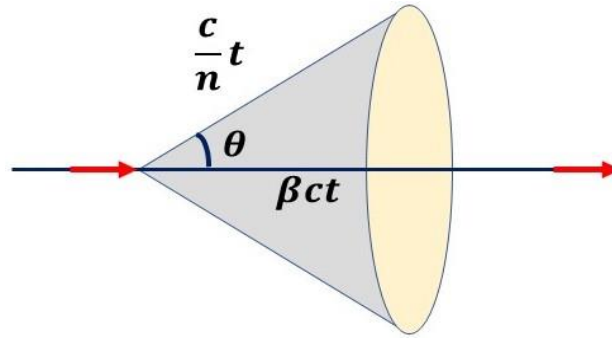


Figure 1-3 Cherenkov Light emitted in a cone (reproduce after ref. [128]).

The Cherenkov effect is sketch in figure 1-3, the charged particle goes through the radiator and determines the emission of light in a cone shape around their trajectory. The relation 1.2 refers to the azimuthal angle that is in fact the cone opening on which the light is emitted [128].

$$\cos \theta_c = \frac{1}{n(\omega)\beta} = \frac{\sqrt{(mc^2)^2 + p^2c^2}}{npc} \quad (2.2)$$

Where:

- θ_c - the azimuthal angle;
- β - the velocity given by the ration between v_p and c ;
- p - the particle momentum.

The particle velocity β is calculated knowing the refraction index and the azimuthal angle which is fixed for the Cherenkov emitted light.

The LHCb detector used in the particle identification system has a chain of two RICH sub-detectors to fully cover a momentum range from 1 GeV up to 150 GeV [129, 130]. RICH1 as well RICH2 rely on the same working principal, design and technology. When charged hadrons pass through radiator generate the Cerenkov photons emitted in a cone.

Further being focused with a spherical mirrors and reflected using flat mirrors on photodetectors planes situated beyond the LHCb acceptance [131]. Both sub-detectors are equipped individually with two planes of photodetectors. The RICH1 photodetection plans are placed above and below the beam pipe, while in the RICH2 are situated on the side of the beam pipe [123].

RICH1 is used for the identification of low momentum particles (1-60 GeV) and located close to the interaction point, thus in upstream of the dipole magnet between VELO and the TT tracking detector. A layout of RICH1 is presented in figure 1-4 with the vessel dimension of $2 \times 3 \times 1 \text{ m}^3$ [132]. A positive kaon identification is done above 2 GeV while a pion-kaon separation is done up to 10 GeV, achieved using a 5 cm of aerogel radiator with a 1.03 refractive index [132]. Further, to 60 GeV the pion-kaon separation is performed using a C_4F_{10} gas radiator extending 85 cm in the Z axis with a refractive index of 1.0014. Consequently, by being placed in the fringe field of the magnet, the RICH1 experiences a magnetic field of about 60 mT. A shielding box, made from a high magnetic permeability iron, surrounds the RICH1 architecture and lowers the magnetic field to 2.5 mT in order for the photon detectors to operate in compatible environment condition [133, 134]. After radiators, emitted in cone of light the photons are focused using a system consisting of two spherical mirrors and two flat mirrors [131]. The curvature for both spherical mirrors is 2.4 m while their structures of carbon fibre is coated with aluminium and a SiO_2 plus HfO_2 pair of layers to protect and optimised the reflective of Cherenkov light. Situated above and below the beam pipe, the flat mirrors are used to reflect the Cherenkov photons on the detectors planes [131].

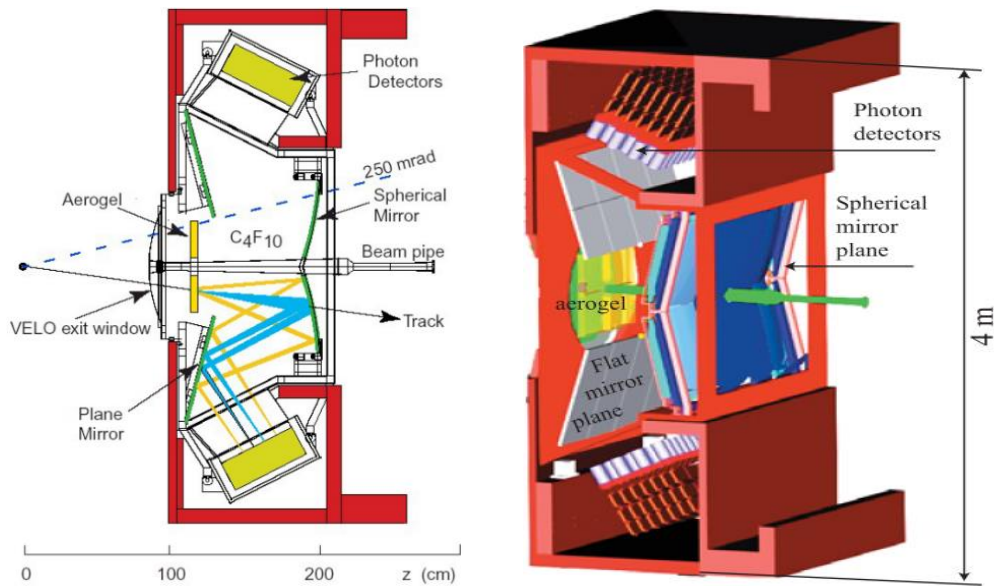


Figure 1-4 The RICH1 sub-detector architecture presented in cross section (on the left) and 3D (on the right) [116].

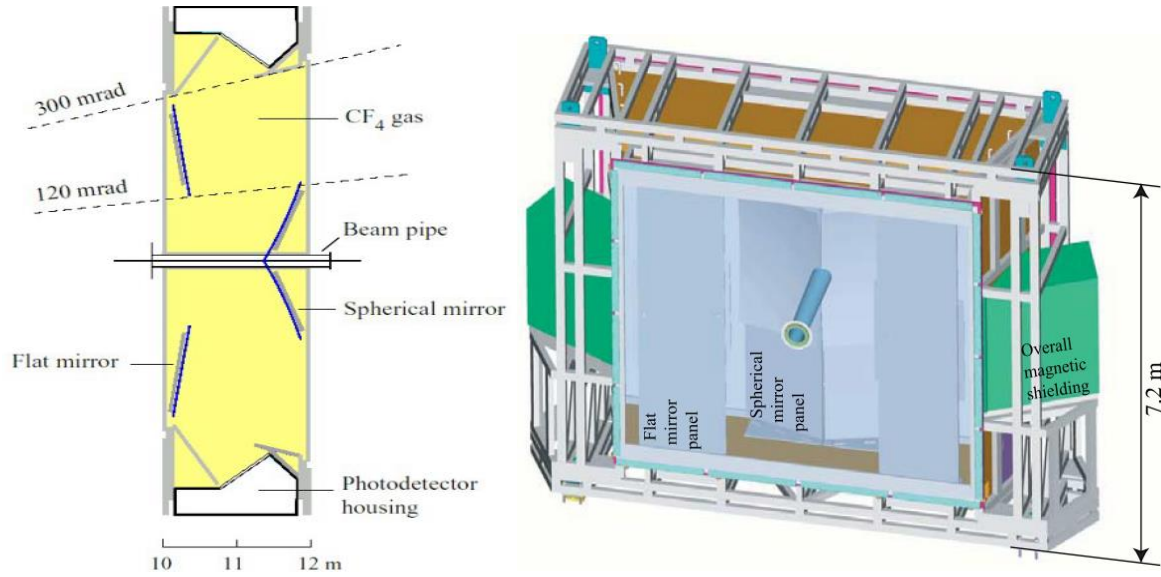


Figure 1-5 The RICH2 sub-detector architecture view from the top (on the left) and its 3D representation (on the right) [116].

The RICH2 sub-detector is placed downstream to dipole magnet with the sub-detector vessel of $7 \times 7 \times 2 \text{ m}^2$ embedding as single radiator the CF_4 gas having 1.005 refractive index [116]. The length of the gas radiator is 2 m and it provides a pion-kaon separation that covers a momentum range starting from 20 GeV up to 150 GeV. As in the previous case of the sub-detector, RICH2 has a shielding box that protects the photodetectors and diminishes the magnetic flux density less than 1 mT [133, 134]. The layout of RICH2 is presented in figure 1-5. The Cherenkov photons are reflected in photodetector planes, which are left and right of the beam pipe. Each one of the spherical mirrors has a curvature radius of 8.6 m [131].

The Cerenkov photons in the RICHs sub-detectors chain are collected using large areas of photodetectors planes working on LHCb nominal conditions. When the LHCb detector was in conceptual phase, no commercial photodetectors were available to fulfil the application requirements and to withstand in LHC environment. Due to this, a large R&D program was initiated resulting in the implementation of Hybrid Photo Detector tubes (HPD) [135]. Figure 1-6 presents the layout of an HPD tube.

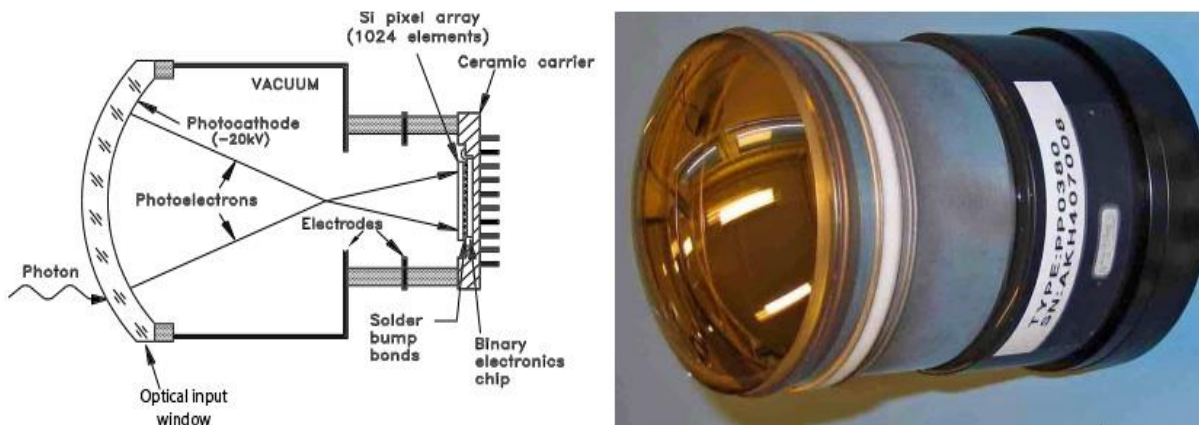


Figure 1-6 Constitutive elements of the HPD tube (left) and its physical implementation (right) [25].

The HPD are vacuum tubes that have a spherical entrance window of 7 mm thick quartz with thin S20 multi-alkali layer deposit to its inner curvature as photocathode. When an incident Cherenkov photon hits the tube photocathode, a photoelectron is released and accelerated towards Si pixel array sensors. Between 10 - 20 kV are applied typically at the electrodes to generate the intense electrical field inside the tube vacuum. Accelerated photoelectron dissipates its energy in the reverse-biased silicon detector with 1024 pixels leading to electron-hole pairs production. The silicon pixel array has 32 rows by 32 columns, each of the $500\text{ }\mu\text{m} \times 500\text{ }\mu\text{m}$ elements are bump-bonded to the binary readout chip. The entire semiconductor structure forms the flip-chip assembly which is mounted and wire-bounded to a ceramic carrier namely PGA (Pin Grid Array) [119], thus represents the anode part of HPD tube.

In both RICH sub-detectors, the photodetection planes consists of closed packed HPD tubes which are installed together with their readout electronics into magnetic shielded boxes. In total 196 HPD were used in RICH1 and 288 for RICH2. Figure 1-7 shows the HPD tubes integration into detector plane assembly along with a picture of one column fully equipped with electronics. The HPD tube overall has a diameter of 83 mm and in column assembly is surrounded by a 1 mm thick sheet of magnetic shield. Measurements have shown a decreasing in B field intensity from 5 mT to 2 mT in case of RICH1. A packing factor of 0.65 was achieved for all four photodetection planes taking to account the 75 mm active radius of HPD and tube to tube pitch of 89.5 mm for detector plane assembly [119].

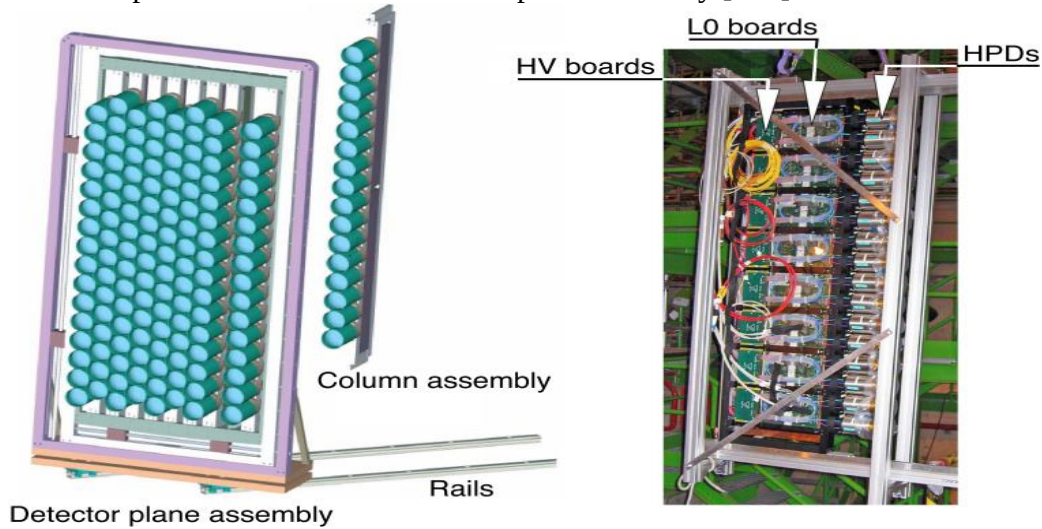


Figure 1-7 Layout of the detector plan assembly for RICH2 (left) and one column fully equipped (right) [119].

Data from HPDs are readout with the help of an electronic system consisting of front-end electronics embedded in so called L0 (Level-0) and the rest of this electronic acquisition chain into L1. Therefore, the L0 electronics use only radiation qualified devices because usually it is exposed to radiation. Instead, the L1 electronics operates in the counting house outside the LHCb detector cavern, behind the radiation-shield wall. Hence, the components of L1 electronics are not mandatory radiation tolerant. For each HPDs column assembly the L0 electronics consists of LHCPIX1, L0 boards followed by high voltage distribution (HV) boards. The anode assembly of the HPD tube is based on a readout chip named LHCPIX1 implemented with a $0.25\text{ }\mu\text{m}$ CMOS technology [136].



Figure 1-8 The RICH sub-detectors L0 board [119].

Signals are amplified, shaped and discriminated by the chip. During the L0 trigger latency period the recorded hits are stored in a buffer and then readout. The HPDs data outputs are transferred to the L0 boards implemented around antifuse gate array ACTEL AX1000. These boards are used as interfaces between the HPDs, Experiment Control System (ECS), Timing and Fast Control system (TFC) and, finally, the data transmission system [119]. Before passing data coming from HPDs to the data transmission system, the ACTEL AX1000 device was configured to add headers with event information and data integrity. A picture with L0 board is given in figure 1-8.

Data are transferred from L0 boards to L1 electronics inside the counting room via optical links. Over 484 optical fibres are used to send in total 500 Gbit/s of aggregate output data from the RICH photon detectors running at 1MHz trigger rate. Each L0 board is equipped with two fibre optic connectors, one per HPD, and the data transmission is provided by the Gigabit Optical Link (GOL) chips in conjunction with Vertical Cavity Surface Emitting Lasers (VCSEL) [119].

A custom data transmission protocol was adopted to send data from L0 to L1 electronics. Adapting this protocol to the industry-standard Gbit Ethernet protocol is done by the L1 electronics which ensure a compatibility with the LHCb detector DAQ network. In the first phase, the incoming serialised optical data on each fiber optic channels is converted into electrical signals processed by FPGAs. After the data are deserialised, the FPGAs execute a zero-suppression algorithm to all the streams of data in parallel. The zero-suppressed data are buffered and further multiplexed in the so called multi-HPD event packets. Finally, the multi-HPD event packets are again multiplexed to obtain the multi-event packets transferred over Gbit Ethernet protocol to the DAQ network.

The operating conditions of both LHCb Cherenkov sub-detectors are supervised by the RICH Detector Control System (DCS) that allows features as: power supply control and monitoring; gas purity monitoring; environment parameter monitoring; adjusting the magnetic distortion; monitoring the RICH1 and RICH2 laser alignment system [137]. All these CDS capabilities ensure the RICH sub-detector integration into LHCb detector control system.

1.3.2 Trigger system

In the LHC time there are 25 ns between two successive proton or lead ions bunches, therefore the collisions rate for the two opposite accelerated beams is 40 MHz. The LHCb detector can be readout entirely at a rate of 1 MHz, while operating at an average luminosity

of $4 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$ lower than LHC can deliver [119]. The data stored for future offline analysis are selected using a trigger system [138] that reduces the events rate to 4 - 5 kHz, corresponding to the writing speed into the LHCb storage. Thus, the LHCb trigger system purpose is to decide in a very short time if an event can be accepted or rejected. A detailed view of the trigger system architecture is given in figure 1-9. This selection of the potentially interesting events for physics analysis is made by the hardware and software components of the trigger system.

The hardware part is the first trigger stage known as Level-0 (L0) trigger whose custom electronics run synchronously with the 40 MHz bunch crossing frequency of LHC. The L0 trigger searches for typical signatures of the heavy B meson decays using the pile-up system, the calorimeters trigger and the muon trigger. The decision unit oversees all these subsystems. When threshold conditions are fulfilled for any of the three L0 trigger subsystems, then an event is selected for the High Level Trigger (HLT) processing. The pile-up system measures the radial positions of the tracks allowing distinguishing crossings with single and multiple interactions. Photons, electrons or hadrons with large transverse momentum are identified by calorimeters, while for each event the tracks of the two muons with highest transverse momentum are reconstructed by muon stations. The L0 decision unit gathers all the information which concludes to the final decision upon event rejection. In terms of L0 trigger output rate for hadrons this is 450 kHz, preceded by muons with a 400 kHz and a 150 kHz for photons or electrons.

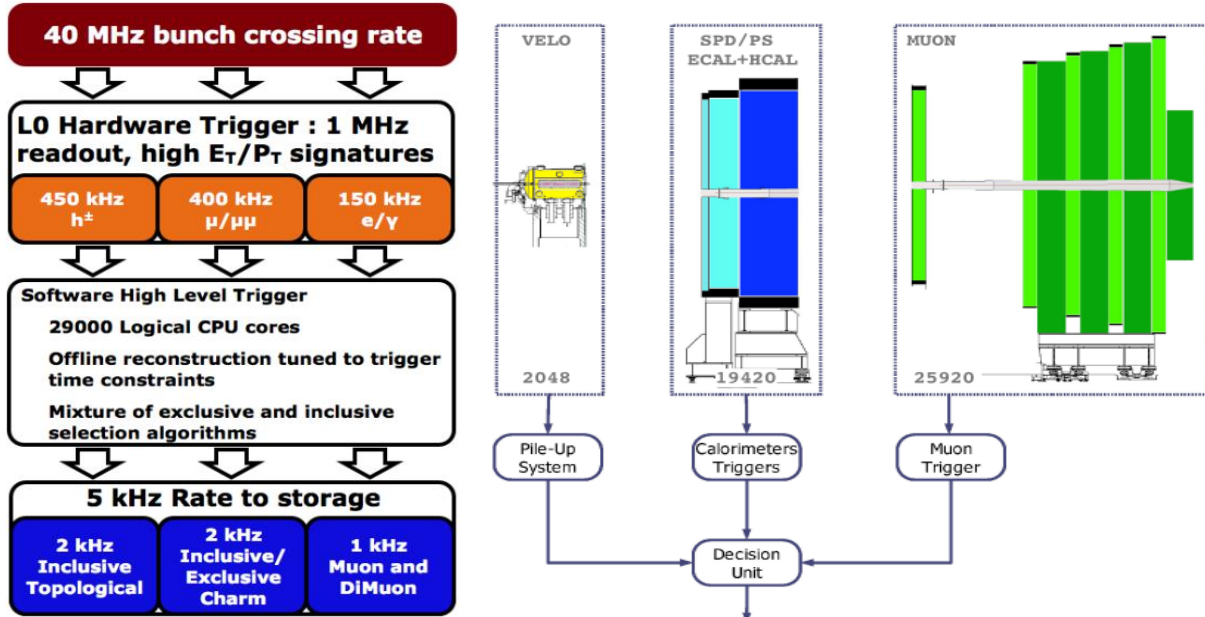


Figure 1-9 The trigger system scheme [139] for LHCb detector (left) and the L0 trigger [119] layout (right).

Second trigger system component is a C++ application running asynchronously on Event Filter Farm (EFF) relying on 29000 CPU cores [119, 139]. The High Level Trigger (HLT) is organised in two components namely HLT1 and HLT2. The bulk of events delivered at 1 MHz rate by the L0 trigger, will undergo selection algorithms subsequently in HLT1, then in HLT2. The L0 decision is confirmed or reject by HLT1 which accomplishes a partial event reconstruction fairly closed to the object that enabled L0 trigger. Reduction is done in HLT2 designed to allow full event reconstruction. Finally, the data associated to the events passing HLT2 are stored for later physics analysis. By design the HLT is a software

application which is very flexible and continues to be improved based on knowledge gained from real data.

1.3.3 The RICH Upgrade Program

The LHC is a unique research infrastructure being the largest and most advanced particle accelerator infrastructure built up to now. This amazing machine was putted into service in 2009 and since then provides proton-proton collision initially at 900 GeV and after 4 operation years ramped up to 8 TeV at bunch crossing rate of 25 ns, while the first heavy-ions collisions took place in 2010 at 2.75 TeV centre of mass energy. The peak instantaneous luminosity milestone of $7.7 \times 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$ was achieved in 2012 with LHC, this value is closest to the design one of $10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ [94]. Even so, the LHC worked at half its nominal energy and its vast physics potential will be fully exploited within the next years after finishing an upgrade period.

The High Luminosity LHC (HL-LHC) project currently ongoing has as main purpose to extend and improve the physics program at the LHC beyond 2022. This program has become the top priority of the European Strategy for Particle Physics [140] given the scientific achievements and technological breakthroughs driven by the numerous experiments conducted at CERN. The LHC upgrade will lead to an increase of collision energy, luminosity and data delivered by the four major experiments. Regarding the luminosity, it will be increased by a factor of 10 and this will raise new engineering challenges that will need to be overcome, especially by the readout electronics which will run in an intense radiation environment. The LHC roadmap towards HC-LHC is presented in figure 1-10.

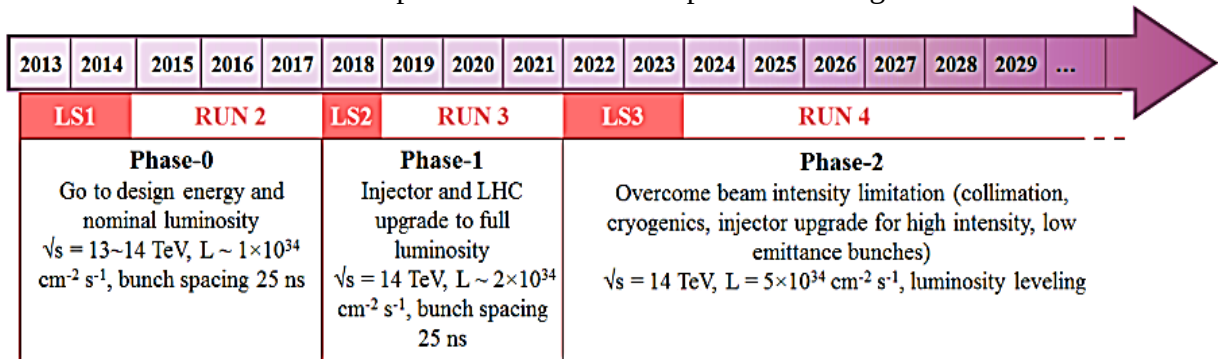


Figure 1-10 The timeline for LHC roadmap [94].

The HL-LHC machine will become operable in the end of the following three evolution phases:

- *Phase-0*: marked by first long shutdown (LS1) in which the centre of mass energy for proton-proton collision is increased to 13-14 TeV and has a peak luminosity of $10^{34} \text{ cm}^{-2} \text{ s}^{-1}$. Also the ATLAS, CMS, LHCb and ALICE experiments underwent some adjustments required by the new LHC machine operating conditions [94].
- *Phase-1*: starts with second long shutdown (LS2) period followed by data taking in RUN3 at nominal LHC design energy and $2 - 3 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ peak luminosity. Within this phase all four detectors will be improved and upgraded to take advantage of the luminosity reached [94].

- *Phase-2*: begins with LS3 during which the LHC infrastructure will be upgraded to deliver a peak luminosity of $5 - 7 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$. The ATLAS, as well as CMS experiment will require upgrades and replacement of their detectors motivated by the lifetime end of some important parts as inner tracking systems [94].

During RUN1 (2010-2012) and RUN2, the LHCb experimental apparatus has proved its robustness and excellent performance in collecting data even operating at $4 \times 10^{32} \text{ cm}^{-2} \text{ s}^{-1}$ luminosity, which is twice more than the detector design one [141]. The present detector readout and trigger system are limited in exploiting higher luminosity value. Moreover, in the future the LHCb detector must cope with luminosity ten times higher. In consequence, the current LHCb detector cannot fully benefit from the present and future LHC machine capability due to the “bottleneck” caused by reading out some sub-detectors at 1 MHz and storing the event information at 5 kHz after processing the bulk of collected data. The first level trigger (L0) of LHCb detector is implemented in hardware fact leading to data bandwidth limitation.

As a main objective for RUN3 is the upgrade of detector in order to gather data more efficiently by reading out all its sub-detectors at a LHC bunch crossing frequency of 40 MHz and taking advantage of $2 \times 10^{33} \text{ cm}^{-2}\text{s}^{-1}$ instantaneous luminosity during a period up to 10 years. The program of the LHCb Upgrade was documented initially in so called “Letter of Intent” [142] and detailed in the “Framework Technical Design Report” [143]. Also, for each subdetector improved or redesign dedicated technical design reports were made such as: LHCb Trigger and Online Upgrade Technical Design Report [144], LHCb VELO Upgrade Technical Design Report [145], LHCb Tracker Upgrade Technical Design Report [146] and LHCb PID Upgrade Technical Design Report [116]. The production together with the quality control for new subsystems is planned between 2015-2017, while the installation and commissioning are foreseen in 2018/2019 in terms of the upgrade programme schedule.

The new data acquisition architecture proposed for LHCb Upgrade requires re-design to the sub-detectors front-end electronics in order to transfer data at 40 MHz. General schematic for the future detector front-end electronic system consists on signal preamplifiers, analogue to digital converters (ADCs), data zero suppression, derandomising buffer and Giga-Bit optical links [147]. Also, complete event readout at bunch crossing frequency strongly depends on the trigger strategy. For the LHCb Upgrade the solution adopted envisages on one side replacing the L0 hardware based trigger system with a new one relaying more on a flexible software-based trigger system [144, 147-149]. This turning point in the trigger system architecture takes advantage of the flexible and scalable design benefiting from software upgrade, upgradable computing power available in Computer Farm, all-software approach running on inexpensive COTS hardware. Figure 1-11 presents a schematic view of new LHCb trigger system.

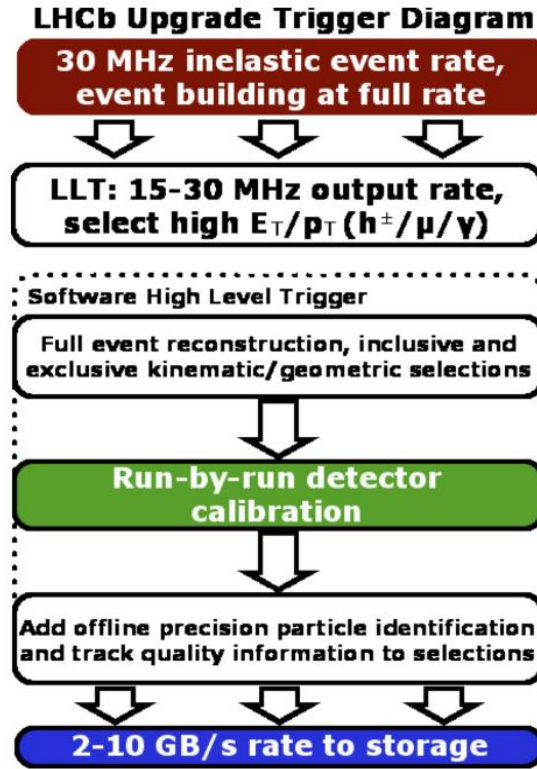


Figure 1-11 The full-software trigger architecture proposed for LHCb Upgrade [141].

Concerning the software-based trigger system architecture, it is divided in the Low-Level Trigger (LLT) and the High Level Trigger (HLT). The LLT is a software and hardware trigger sharing similar functionality with L0 and the following features: accommodates event data to HLT capabilities; improves the selected sample quality with interesting events; protects against fluctuation in occupancy which overcome the full readout. The LLT role will be gradually minimized with increasing of the CPU farm resources. On the other hand, the HLT is in charge with a flexible event filtering governed by a software algorithm running on the LHCb CPU farm. Finally, the HLT will tape the event information at 20-100 kHz rate. This flexible trigger platform also allows run by run detector calibration.

The LHCb sub-detectors upgrade entail design challenges due to the higher data rate required, increased level of radiation causing sub-systems performance degradation and higher track multiplicity. Moreover, all this affect, especially, the silicon detectors having the readout chip integrated within the sensors.

1.3.4 RICH new photodetection system

Scheduled to start in 2018 the RICH Upgrade Program envisage the redesign of photodetection system [150-152]. The Cherenkov photon detection will be implemented using a commercial baseline solution with Multi Anode Photo Multiplier Tubes (MaPMT) [153]. All semiconductor devices part of the MaPMTs readout, either from front-end boards or digital boards, must withstand to mixt-radiation field inside LHCb detector. Our group is in charge with the radiation hardness qualification of the MAROC3 chip considered as backup ASIC for the front-end board. While for the digital board, we evaluate the main IC at ionizing radiation which is an FPGA from KINTEX-7 family.

Regarding the MaPMT work principle, the photo-detector relies on an external photoelectric effect taking place into a vacuum tube. The MaPMT consists of an input window, a photocathode for a photoelectric conversion, focusing electrodes that accelerate and focus the electrons on dynode where they multiplied through a secondary electron emission. Further, the process is repeated at each dynode till the last one where all the emitted electrons are collected by anode [154]. Figure 1-12 presents a detailed view of all constructive elements built in the photomultiplier enclosure.

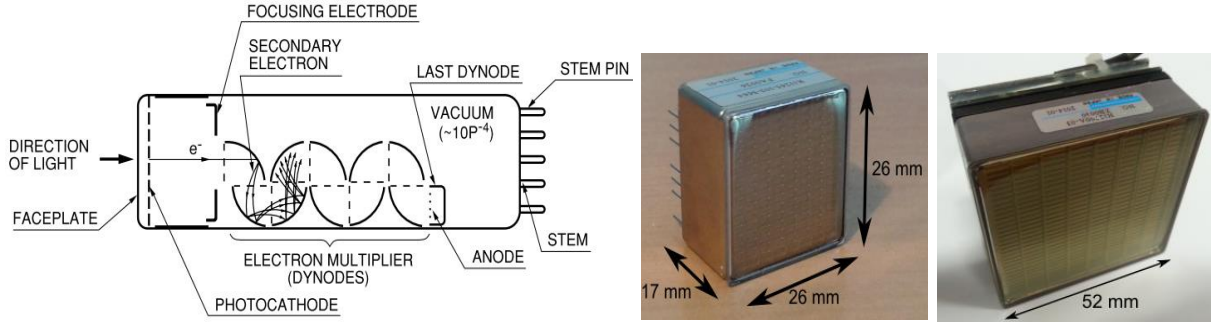
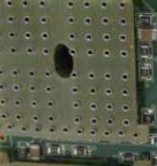


Figure 1-12 Constructive elements of a photomultiplier tube [154] (left side), Hamamatsu R11265 MaPMT and H12700 (right side) [155, 156].

An photodetection plane of 1.6 m^2 for RICH1 and 2.1 m^2 for RICH2 will be covered in total with 4480 MaPMT [116]. Two types of MaPMT were considered, both with an ultraviolet borosilicate entrance window, super bi-alkali photo-cathode and electrons multiplication in 12 stages. For RICH1 and the central part of RICH2 a R11265 will be used. This device has an effective area of $23 \times 23 \text{ mm}$ summing 64 pixels arranged in an 8×8 array, each pixel occupying approximately $2.9 \times 2.9 \text{ mm}^2$ [157]. In the case of RICH2, the photodetection plane outer region, where lower granularity is required, the H12700 MaPMT type will be used. This one has an area four times greater than R11265 with the pixel size of 2.1 times bigger. Both MaPMT types are optimised for single photon detection with quantum gain of 10^6 biased at 1 kV DC voltage.

The photodetection planes, occupied by MaPMTs, will benefit from read-out electronics running with 40 MHz LHC clock. A preliminary version of its general architecture for the read-out system is presented in figure 1-13. The front-end boards, populated with CLARO, process the signals out coming from MaPMT by performing analogue pulse shaping, amplification and digitisation, channels to channels gain correction. MAROC3 ASIC was considered as backup for the front-end board, but this chip has a couple of drawbacks such as longer peaking time than CLARO and it is not radiation hard tested. On the other hand, the MAROC3 has 64 input channels, so one chip can fully read a MaPMT, and in addition it can perform a charge measurement. One digital board is serving 4 MaPMTs. Around the digital board with FPGAs resides DC-to-DC converters, GBT-SCA chip, giga-bit transceivers (GBT) [158] chips and optical links to TELL 40 readout cards [116]. The GBT-SCA chip was specially developed for High Energy Physics Experiments allowing the front electronics control by sending Slow Control signals, delivering reference clock together with trigger decisions and detector control [159]. Among this integrated circuit built in features are: DACs, ADCs, general-purpose IO, and interface GBT data transmission protocol to SPI, I2C and JTAG standard.



Read-out electronics will be embedded in the so-called elementary cell (EC) which is an aluminium structure with cooling bars housing the following:

- Subsequent, 2x2 ECs are grouped into one photon detection module (PDM), see figure 1-15. Also, 4 x 4 MaPMT tubes are shielding against LHCb dipole magnet B field, as material mu-metal is foreseen to be used in shielding ECs.

Regarding the bandwidth requirements by example one PDM to forward data at TELL40 module, in case of the PDM situated in regions with high occupancy it is estimated at 40 Gb/s, excluding header information and zero-suppression not used for those zones. For low occupancy regions, where zero-suppression is applied, the bandwidth would be up to 3 Gb/s [116].

1.3.5 LHCb detector radiation environment

The operation of accelerators and detectors in high energy physics experiments induce radiation background leading to a harsh environment not only for human safety, but also for electronics. Over time, software application were used to characterize and quantify the radiation background inside the LHC accelerator complex, such as MARS IHEP, GCALOR, FLUKA and GIANT4 [79]. Information about the radiation dose, particle species and their fluxes are very useful for:

- knowing detectors constructive elements activation, therefore radiation level in case of maintenance services;
- determining during beam operation the radiation exposure of personnel working not far away from the experimental hall;
- requirements in term of radiation tolerance for the electronics meant to run in such hostile environment.

Early studies found in literature [90, 161-163] were focused in characterising the LHCb machine radiation background in its cavern. The biggest contribution for the background is brought by protons interacting with the detector constructive elements. This process sparks secondary particles that do not originate from the primary beam head-on interaction. A more recent study [164] highlights, ranked by each contribution, the sources that generate the LHCb detector radiation background as:

- beam head-on collisions;
- contributions of proton beam inelastic and elastic interactions with residual gas nuclei taking place into LHC long straight section (around 600 m long) beam pipe nearby the LHCb cavern;
- elastic and diffractive interactions occurring in whole LHC 26.7 km ring;
- transverse beam halo as a consequence of betatron located at IR7 [165] with fixed cleaning inefficiency;
- off-momentum beam halo generates by a betatron at IR3 on the LHC ring;
- small part of diffractive and elastic interactions which possibly reach LHCb experimental hall, originating from surrounding higher luminosity experiments.

Other considerations regarding radiation background in LHCb detector are settled by its position closed to the beam 2 injection point in LHC and ATLAS experiment proximity, while less relevant is the cross-talk induce by CMS interaction point take into account its lack of proximity location [164]. All sources mentioned give birth to mixed-field radiation environment in the LHCb experimental area featured by various particles species and wide energy spectra.

Particles like protons, neutrons, electrons, positrons gammas, charged hadrons (pions, kaons, excluding protons) compose this mixt-field common to all experiments on LHC. As example, the principal source of neutrons for the LHCb experiment is the inner part of detector calorimeter system (ECAL and HCAL). In this region occurs the interactions between primary particles and calorimeters materials leading to a strong flow of neutrons that rise due to the hadronic showers [161]. The neutron fluency decreases with the distance to source, hadronic showers being absorbed by calorimeter material and other materials from detectors regarding system location. The dipole magnet situated between the muon system downstream and VELO, represent a second source of neutrons. This time the neutrons background affects the inner part of M4 and M5 muon stations, while rest M1-M3 stations are protected by the muon shields [161].

The primary interaction is the main source of charged hadrons spreading from VELO to calorimeter systems, where the pions represent most charged hadrons. These high energetic particles are almost fully stopped by the muon shield. Other particles such as electrons and positrons come up in electromagnetic showers into calorimeters as well as along the beam line [161].

The electronic devices are susceptible particularly to the damages induced by neutrons with kinetic energy exceeding 0.1 MeV, also thermal neutrons with an energy of 0.025 eV represent a threat for semiconductor [161, 166]. High energetic charged hadrons produce a very strong local ionization in the silicon lattice. Protons at low energies provoke silicon lattice displacement damages through non-ionizing energy loss (NIL). Electrons and positions contribute to the total ionizing dose and, nevertheless, they have negligible damage effect [161].

The research and development activities ongoing to fulfil the HL-LHC project milestones envisage an upgrade program for all four main experiments. In the case of LHCb detector, some of its sub-detectors will undergo an upgrade phase in order to become fully compatible with the LHC clock and luminosity value. A higher luminosity implies higher radiation background and new engineering challenges in designing radiation tolerant electronic equipment. An irradiation campaign was foreseen to evaluate the radiation hardness for the newly implemented ASIC and COTS devices. Concerning RICH sub-detectors upgrade, every electronic device, mostly the semiconductor based ones of and elementary cell, must be radiation hard [116]. Parameterization is made with FLUKA software for the new radiation background generated by significant luminosity increase, plus modification in LHCb machine architecture. The value estimated for radiation level in the inner region near beam pipe is approximately 1 Mrad/year. Looking in to photodetection system of RICH1 and RICH2, the low and high radiation regions are presented in table 1-1 [116].

Table 1-1 Radiation level per year around photodetection system electronic components (after ref. [116])

	RICH1		RICH2	
	Low region	High region	Low region	High region
Neutrons: 1 MeV n_{eq}/cm^2 ($\times 10^{11}$)	4	6	1	2
Ionising radiation [krad]	7	42	1.5	4

Extensive radiation qualification tests are in progress to fully characterize the following chips: CLARO, MAROC3 and KINTEX-7 FPGA. The Romanian LHCb Group is actively

involved in testing of the last two chips mentioned. The radiation hardness tests goal is to determine if they are reliable for the harsh condition considering the above values for background and safety factors of two might be considered due to the numbers of MaPMT and IC times statistical fluctuation.

1.4 Conclusions

CERN is the leading particle physics laboratory in the world, housing cutting edge accelerator complex and particle detectors. This unique research center is dedicated to the study of matter basic constituents, fundamental particles, probing the universe fundamental structure. Its timeline is full of outstanding scientific discoveries and technological breakthroughs. Extending the discovery potential after 2020 in the hope of New Physics studies requires an upgrade program accomplishment with LHC luminosity increasing by a factor of 10.

Future HL-LHC scientific instruments would accommodate a higher collisions number, accurate measurements of new particles and it will enable the observation of rare processes presently under the sensitivity threshold. Being the main priority of EU Strategy Report for High Energy Physics, this project envisages a laborious upgrade program for LHC injectors (LIU) as well as to the four most important detectors. The letter of intent for HL-LHCb was just submitted to LHCC Steering Comity of CERN.

The LHCb detector is part of this upgrade program. In the LHC second long shutdown beginning in 2018, the LHCb machine architecture will undergo modifications, which imply removing a few sub-detectors, while others will be completely redesigned, and some will have the readout electronics improved. Both RICH sub-detectors will be equipped with a new photodetection system based on MaPMT and the readout electronics will run compatible with LHC clock of 40 MHz. Each electronic device must be certified as tolerant in mixt-field radiation environment predicted for LHCb machine.

Preliminary to the 2018 upgrade phase, a radiation qualification campaign was foreseen to validate the new developed ASIC's and COTS components for the LHCb RICH sub-detectors redesign. The members of LHCb Romania Group bring their contribution testing the radiation hardness of a KINTEX-7 FPGA considered the main semiconductor device upon digital board, MAROC3 ASIC backup solution for a front-end board and SPACIROC2 ASIC as blueprint for future generations of MAROC radiation hard by design.

The upgraded LHCb detector will benefit from a full-software trigger system architecture with all subsystems running at 40 MHz acquisition rate. New research topics in particles physics will be open through these improvements and also by taking advantage of an increase in luminosity.

CHAPTER 2

Radiation effects in semiconductor devices

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2. Radiation effects in semiconductor devices

In LHC experiments proton bunches collide head-on at every 25 ns leaving behind a harsh radiation environment. High energy physics detectors, avionics, space probes, military applications demand radiation tolerant electronics meant to have a reliable operation in environments with radiation. Various types of radiation induced effects can occur in a device semiconductor lattice, thus depending on the type of particle passing through and its kinetic energy. These effects are classified in two groups. First one, represented by cumulative effects, which appear gradually because of accumulated radiation dose in time. Second group, Single-Event Effects (SEE), can be triggered by just a single highly ionizing particle producing a very large local charge deposit in semiconductor layers.

A comprehensive view upon each radiation effect depicted in figure 2-1 it will be presented in detail over present chapter.

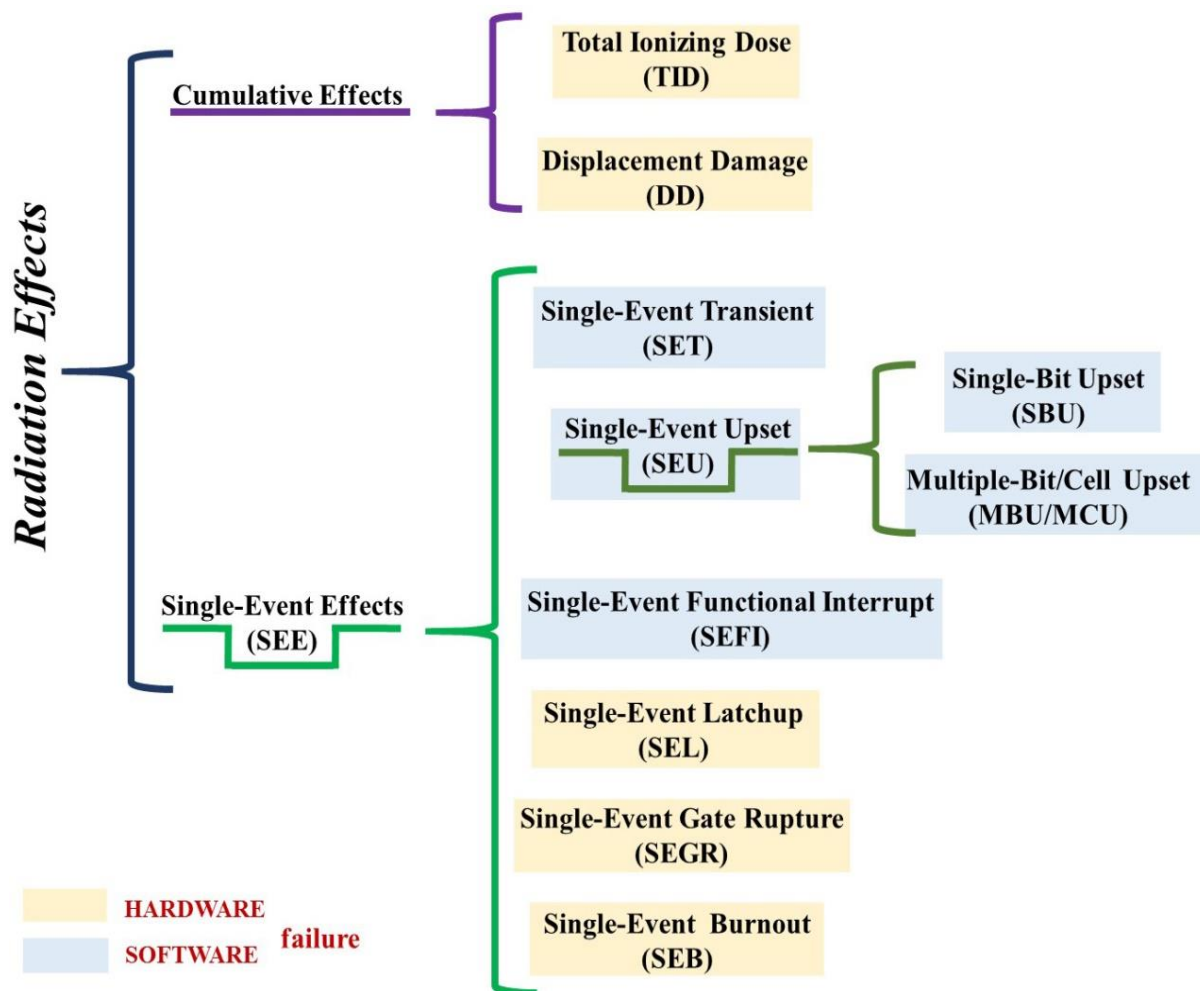


Figure 2-1 Radiation-induced effects into semiconductor devices.

2.1 Relevant definitions and units for domain

Exposed to radiation the semiconductor-based devices are susceptible to a wide range of induced radiation effects, especially in mixt-field. The radiation environment parameterisation makes possible the extrapolation of the device behaviour based on the irradiation tests previously performed. It allows prediction of errors rate and pinpoints the most threatening radiation induced effects upon certain devices. Further there is a list with: definitions and units specific to this domain, characterisation of various particles sources, particles properties, as well as interaction between particles and matter.

The definitions associated to particle proprieties are the following:

- **Flux $\dot{\Phi}$** represents the number of incident particles passing through a unit of area in a unit of time and it is expressed in $\text{cm}^{-2}\text{s}^{-1}$ [167, 168]. From this parameter, other two are derived to better describe the realistic scenario when particles are distributed in an energy spectrum. The integral flux $\dot{\Phi}(> E)$ is the total flux of particles exceeding a given energy E threshold. While the differential flux $\dot{\Phi}(E)$ for a given energy E value it is the variation of flux with energy. The mathematical relation between them is presented in 2.1 formula [167].

$$\dot{\Phi}(> E) = \int_E^{\infty} \dot{\Phi}(E) \cdot dE \quad (2.1)$$

- **Fluence Φ** constitute the total number of particles crossing or hit during a time interval the unit area, therefore expressed in $\text{particles}/\text{cm}^2$. Also, the difference among the differential, integral and solid-angle-resolved fluence is stated in references [167, 168].
- **Energy E** of a particle is measured in eV or often multiples of eV. Thus, 1 eV is defined as kinetic energy gained or lost by a single electron in 1 V electrostatic potential. Beside this, an alternative definition often used for kinetic energy of a particle is energy per nucleon stated in MeV/amu, term amu meaning the atomic mass unit [167].
- **Energy fluence Ψ** express the energy dE on cross-sectional area, noted dA , of a sphere and its unit is Jm^{-2} [168].
- **Species** refers to the proprieties differentiating particles such as mass, charge and energy. In contrast, the photons (UV, X-ray, gamma) may differ in energy [167].

Further are given, definition and units describing particle and matter interactions and the mechanisms of transferring the energy form an energetic particle to the absorbing material:

- **Exposure** is the quantity of ionization charges induced by a radiation species per unit mass of standard atmosphere. Its unit is Coulomb/Kg or the analogue unit Roentgen being $2.56 \times 10^{-4} \text{ C/Kg}$ [167].
- **Absorbed dose D** for the irradiated material is the energy absorbed per unit of mass. Therefore, a dose of 1 Joule per kilogram means a Gray (Gy). Frequently used unit is the rad corresponding to 10^{-2} Gy [167, 168]. Accurate is to be specified the nature of the irradiated material because of dependency between absorbed dose and material of interest, for instance rad (Si) or Gy (SiGe). The situation of high-energy charged particles penetrating the exposed material ends up with their energy dissipated through ionization phenomena. This allows cross-utilization for the term dose and ionizing dose, but not for neutrons and low energy ions.

- **Non-ionizing energy loss (NIEL)** is physical process driven by the energy loss of particles through a material resulting in permanent atomic displacement. The NEIL ions could interact with nuclei and not with atomic electrons. This interaction could be elastic or inelastic, for inelastic interaction resulting residuals nuclei, protons and neutrons (nucleons).
- **Dose equivalent H** was introduced to quantify the radiation-absorbed dose for human tissue which has a different response at various ionizing radiations, that way a qualifying and weighting factor was introduced. The dose equivalent can be written as $H=qD$ and measured in Sievert (Sv), alternative older unit is rem and correspond to 1 rad. The q factor numeric value is: 1 for electrons and gammas, 10 for protons and neutrons, up to 20 for alphas originating from radionuclides [167].
- **Dose rate** define the radiation quantity absorbed by the target material per unit of time [168].
- **Linear Energy Transfer (LET)** is a parameter used to define the amount of energy transferred per unit path length [169]. On the other side, the **electronic stopping power** depicts the energy losses by ionization phenomena when a charged particle passing through a material [167]. The measurement unit for LET is MeV/ μm , while for the stopping power is normalised to the absorbing material absorbing mass being expressed in MeV $\cdot\text{cm}^2/\text{mg}$. The Bethe-Bloch equation is at the basis of energy loss calculation trough ionization phenomena. Referring to semiconductor devices, the LET represents the most important parameter used in radiation qualification study of single-event effects (SEE) being defined in various ways by the literature of domain. The time table below summarises commonly used LET definitions [170].

Table 2-1 Radiation level per year for photodetection system electronic components (based on ref. [167])

No.	Definition	Unit
1.	Energy deposited per unit path length	MeV/ μm
2.	Mass stopping power	MeV cm^2/mg
3.	Linear charge deposition	pC/ μm
4.	Electron-hole pairs per unit path length	μm^{-1}
5.	Effective LET θ – angle of incidence for the particle	$\text{LET}_{\text{EFF}}=\text{LET}/\cos(\theta)$

Neutrons and heavy charge ions produce displacement damage in semiconductor device lattice. If the particle striking the target atom, from crystal structure, transfers enough energy above the atom displacement energy, it results in displacement of the target atom and the so-called recoil atom/nucleus is released from lattice node. Moreover, a cascade of displacements is possible to be triggered if the recoil atom has energy twice higher than displacement damage energy and another recoil atom is released which might perpetuate the mechanism.

Neutrons with energy spectra from 0.1 to 14 MeV are the main cause of displacement phenomena [167]. Usually, the damage due to the displacements induced by energetic particles into device is normalised to **1 MeV equivalent neutron** fluence, which would

produce deposition of the same amount of non-ionising energy leading at equivalent damage to the material crystal structure [171].

2.2 Cumulative effects

Understanding how energetic particles interact with matter is needed to allow parameterisation the mechanisms describing various radiation effects which are occurring into semiconductor devices. The cumulative effects represent one of the two mains categories of radiation effects occurring in devices. It manifests itself as an accelerated aging of the device performances or through malfunction and even failure. All this is consequence of total ionising dose and displacement damage.

Table 2-2 Cumulative effects (after ref. [167])

Particle species	Energy range	Type of interaction	Primary effects in Si and SiO ₂	Secondary effects in Si and SiO ₂
Electron	Low energy	Inelastic scattering	TID	DD
	Medium energy	Elastic scattering		
	High energy (>a few MeV)	Bremsstrahlung		
Protons and Ions	Low and medium energy	Inelastic and Elastic scattering	DD and TID	
	High energy protons, deuterons, alphas (>a few MeV)	Nuclear reaction Bremsstrahlung		
Photons	Low energy (<1 MeV)	Photoelectric effect	TID	DD
	Medium energy	Compton effect		
	High energy (>10MeV)	Pair production		
Neutrons	Low energy	Capture and nuclear reaction	DD	TID (by recoil atoms)
	High energy	Elastic scattering		

It is important to state first the process by which the energetic particles interact with matter and take in to account their species, energy and the target material nature. Essentially, there are the following mechanisms [167]:

- interaction between energetic particle with the electrons shell of an atom from target material crystalline structure, therefor this case ends in target atom ionization;
- energetic particle colliding with the target atom nucleus, when the energy transmitted exceeds the target atom displacement energy threshold, this it will lead to a recoil atom and displacement damage, moreover this might further trigger displacement cascade phenomena;
- energetic particle inducing in the target nucleus a nuclear reaction leading to the emission of energetic fragments, avalanche phenomena might appear hadronic shower.

The total ionising dose (TID) effect is triggered by highly energetic particle such as electrons with kinetic energy of few MeV, protons and ions or other charged hadrons. Also, ionisation by recoil particles must be considered as contributing to TID. On the other side, displacement damage (DD) is produced mainly by neutral particles, as example neutrons, leading mostly to an avalanche of displacements.

Material exposed to radiations can suffer transient or permanent degradation because of TID and DD effects, which depends on target material nature (semiconductor), temperature and local electric field. In table 2-2 there is a summary of particle inducing either by TID or DD depending on particle species and energy spectrum. The information is presented making the terms agreement that elastic scattering refers to target nuclei scattering and inelastic scattering designate shell electrons scattering, hence the terminology applies only for the below table.

The Bremsstrahlung is an interaction which leads to a continuous electromagnetic spectrum generated when electrons decelerate into target material. Nuclear reaction determines the emission of fragments when high energetic particle excite or splits the target atom. Out coming fragments might cause further DD and TID effects.

2.2.1 Displacement Damage

The mechanism of cumulative effects generation and their types depend on energy deposition within semiconductor layers. Belonging to this radiation-induced event class it is the term Non-Ionization Energy-Loss (NIEL) process that refers to the interactions categories ending through:

- atomic displacements when incoming particle strikes an atom/nucleus from semiconductor lattice and the energy transferred exceed the displacement energy threshold of the knock-on atom;
- lattice vibration caused by energy dissipation as consequence of the collision between incoming particle and knock-on atom from lattice which remains in position the previous collision type also produces vibrations.

The biggest contribution to devices bulk degradation by NIEL process it is brought by atoms displacement known as displacement damage (DD) effect. However, the energy loss through non-ionization mechanism is much lower than energy deposit due to ionization phenomena that also contribute to the cumulative effects. For a given high energy particle and target material, the NIEL is expressed as:

$$NIEL = \frac{N}{A}(\sigma_e T_e + \sigma_i T_i) \quad (2.2)$$

Where:

- A/N – the material atomic mass (A – gram atomic weight, N – Avogadro number);
- σ_e – the cross-section value for an elastic interaction with nucleus;
- T_e – the energy transferred in such elastic collision;
- σ_i – the cross-section value for an inelastic interaction with nucleus;
- T_i – the energy transferred in such inelastic collision.

The measurement unit for NIEL is typically expressed $\text{MeV cm}^2/\text{g}$. NIEL calculation proved to be a useful tool in estimating the electronic device behaviour in environments with radiation. However, for NIEL estimation careful attention should be paid to its limitation and assumption [172], hinge upon particle species and energy, also the nature of target material.

In case of protons, the inelastic part of NIEL contribution rises above 7 MeV and dominates from 100 MeV when the inelastic interactions reach 90% of total NIEL. In the opposite, for the electrons NIEL increases with the energy. Early studies of displacement damage induced in semiconductor were carried out on germanium [173, 174] and later in silicon [175]. The Very-Large Scale Integration (VLSI) device incorporate, beside Si and Ge, a lot of other elements from periodic table that have further implication in the generation process of displacement damage effect. Research in this area is still ongoing to properly explain the DD effect mechanism in semiconductor devices, therefore gaining a better prediction of the device behaviour in radiation environment without the need of costly radiation qualification tests. Basic mechanisms leading to DD effect can be explained considering an intrinsic semiconductor lattice, see figure 2-2.

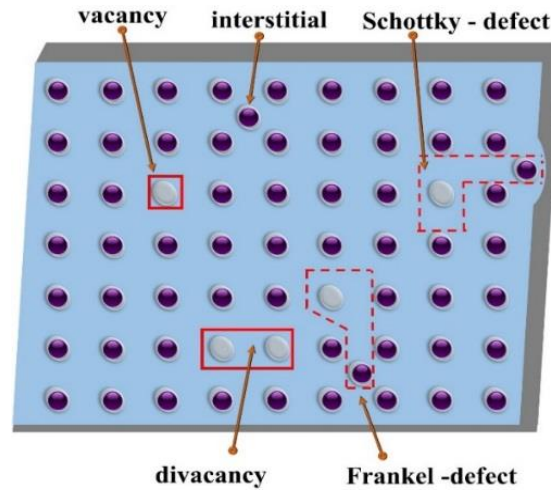


Figure 2-2 The 3D illustration for the basic defects in intrinsic structure (reproduced from ref. [167]).

Recoiling atom position in lattice becomes vacancy and the displaced atom occupies an interstitial position in lattice. Other resting alternatives conduct to Frankel defect consisting within vacancy-interstitial combination and Schottky defect where the displaced atom will position at the surface. At room temperature the primary point defects, which are either interstitials or vacancies, tend to cluster in more stable configuration [176]. As example the di-vacancy and di-interstitial defects in crystalline structure are generated through defect points migration. Practically a primary vacancy is occupied by a neighbouring atom which in turn leaves the initial node unoccupied, therefore vacancies migration in lattice occurs. These vacancies can cluster and give rise to a microscopic void [167]. Among morphological modification must be specified the edge and screw dislocation radiation-induced into intrinsic crystal.

The extrinsic semiconductors have widened number of secondary defects on account of doping atoms and impurities getting involved in defect-impurities pairs. In this case, primary point defects are adjacent to doping or impurities atoms. Two most commune defect-impurities complexes in silicon are so called E-center and A-center. The E-center defect refers to impurities complex arrangement amidst vacancy and elements from column 15 of the periodic table as phosphor, arsenic and bismuth, while A-center is vacancy-oxygen complex [167]. Moreover, extrinsic defects have also a tendency to cluster and persuade into

precipitates, striation, even bubble filled up with gas atoms [167]. Electrical and optical proprieties of semiconductor materials are influenced by secondary defects arising from the primary displacement defects. The displacement defects formation rate depends on target material, species and energy of incident particles, dose and dose rate, etc. Regarding particle species, the principally displacement damage source are the neutrons since they interact directly with the target atom nuclei. A single neutron with energy above 1 MeV can trigger a cascade effect by dislocating the primary knock-on atom from Si lattice which will have enough energy to displace many Si atoms, hereupon give birth to a disorder region.

Originating from primary points defects, the secondary defects influence the semiconductors electrical proprieties by introducing a new energy level (E_T) over or below the Fermi level. The influence of E_T level on carriers mobility can be explain within the following hypothesis:

- secondary defects behave as generation centre when the E_T level is nearby mid-gap and the free carrier concentration is lower than equilibrium one in depleted region;
- the E_T level is close to mid-gap and the minority carriers are in surplus, then the secondary defects act as recombination centre leading to minority lifetime decreasing;
- the defects can carry as trapping centre when E_T level is close to valence or conduction band, hereupon the carries are get caught temporarily and released again in the conduction band.

The defects density plays an important role in above mechanism along with semiconductor dopants. Among all, the trapping centres [177] have even severe implication as: the reduction of semiconductor conductivity through decreasing free carriers concentration; the permanently step down of majority carrier concentration as effect of deeper energy levels introduction in the band, also the trapping levels located close to the band centre could turn the p and n type silicon in intrinsic [167]. Thereby, the displacement damage effect deteriorates the semiconductor devices behaviour and electrical performance. The carriers recombination lifetime for semiconductor is a material parameter which is most sensible to displacement damage. Also, affected by DD are the carriers generation lifetime, the concentration of majority carrier as well as carrier mobility.

Bipolar technology is affected by displacement damage effect especially the devices which are lightly-doped such as particle detectors or high voltage devices and the electronic components in which the minority carrier lifetime is a parameter critical for their functioning like in solar cells. The bipolar transistor has the common emitter DC-current gain, known as h_{FE} , influenced by displacement damage [178]. Experimental studies proved a better radiation tolerance of high-frequency transistors comparing with those operating at low frequency. It is recommended the bipolar transistor usage where in the characteristic range were $h_{FE}(I_c)$ is almost flat.

The MOS transistors operating principle stands in majority carrier currents flowing into gate channel underneath lattice surface. Apparently, they are immune to displacement damage, but device downscaling in conjunction with DD mechanisms of substrate resistivity decreasing and carrier mobility reduction leads to device malfunction. The dominant effect induced by displacement damage upon MOS technology is the increasing of net surface states density [179].

2.2.2 Total Ionising Dose

High energetic particles are losing energy in target material partial through NIEL and mostly through ionization phenomena. Current section is dedicated to ionization effects

induced by radiation in MOS devices. Unlike displacement damage, the ionization affects these devices in a more distinct way influencing both substrate and insulating layer proprieties. The MOS integrated circuits exposed to radiation are sensitive to ionization phenomena because charge could build up into insulator interface like SiO_2 . In the following it will be presented the complex way in which this phenomenon degrades the MOS device performance.

The amount of energy transferred to target semiconductor material volume through ionization phenomena is called ionizing dose and the entire energy quantity absorbed by material during full exposure is also known as Total Ionizing Dose (TID). In semiconductor material exposed to high-energy ionizing radiation the electron-hole pairs are generated, mechanism followed by recombination of most pairs produced. The remaining pairs give rise to a photocurrent that threatens the device electrical characteristics while the ionisation is sustain and once off it will not leave permanent effects [167]. The electron-hole pairs released by ionisation into silicon dioxide, which remain not recombined, give rise to electrically active defect centres, therefore influencing the MOS device structure electrical parameters [180]. Exemplifying on MOS transistor with the gate positive charge, part of the electron-hole pairs produced by ionization starts to recombine. Escaping fraction of electron-hole pairs, named the electron-hole yield, rapidly drift after irradiation. As is shown in figure 2-3, the electrons drift in picoseconds to the gate positively biased while the holes drift on the way to Si/SiO_2 interface.

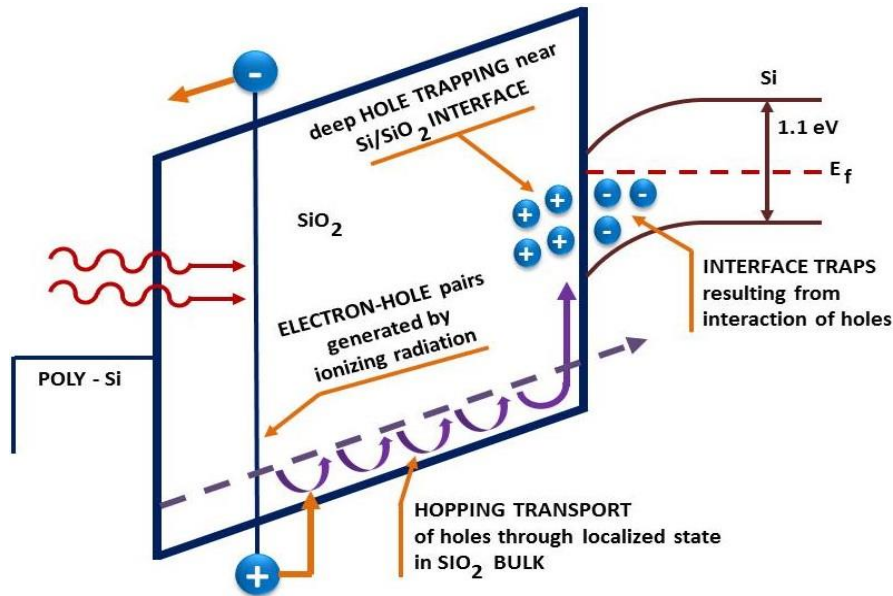


Figure 2-3 Illustration of the band diagram for positive gate bias MOS device in which the charge generation process is triggered by ionising radiation (reproduced from ref. [181]).

Further on, the holes steady advance towards Si/SiO_2 interface ends up entailing a localized state in the oxide as they get nearer to the interface, part of the holes will be trapped, and the positive oxide-trap charge is formed. For n-channel MOS the interface traps are negatively charged. High number of oxide-trapped charges can cluster and cause leaking current. Another contribution to the interface traps is added by hydrogen ions likely released as holes into oxide. The hydrogen ions can drift to Si/SiO_2 interface and react to form interface traps [182]. Clustered in large concentration the interface traps formed in N-MOS transistor leads to the decreasing of carriers mobility and it rise the threshold voltage. In consequence, the transistors drive capability and its timing parameters are compromised.

The charge build-up mechanism in SiO₂ [183] and interface state can be summarised step-by-step, some of upcoming processes could occur in parallel:

- the electron-hole pairs generation;
- the recombination of pairs immediately after generation and the electron-hole yield;
- the migration in SiO₂ layer of the electrons and holes;
- the generation of oxide-trapped charges at Si/SiO₂ interface;
- the interface states generation;
- the annealing of oxide-trapped charges and interface states, process which is temperature and time dependent.

Apart from dose non-equilibrium deposition in case of the low energy X-rays passing through a structure made of thin layers, like MOS, and inhomogeneous ionization induced by heavy ions with high stopping power, the electron-hole production via homogeneously irradiation can be calculated based on formula 2.3 [167].

$$N_{eh} = A \cdot d_{ox} \cdot g_0(\text{SiO}_2) \cdot D \quad (2.3)$$

Where:

- A – transistor gate area expressed in cm²;
- d_{ox} – insulator thickness in cm;
- $g_0(\text{SiO}_2)$ – pair generation rate for SiO₂ is $8.2 \cdot 10^{14}$ per Gy·cm³;
- D – absorbed dose in Gy.

Same of the electron-hole pairs generated by irradiation recombine immediately after they form. The rest, which escape initially recombination, contribute to the value of fractional yield parameter. This parameter depends on electric field value in the oxide, incident particle species and temperature. Multiple studies have been made to highlight the fraction yield value versus the electric field in oxide for different particle species, a relevant one is given in reference [184].

Two recombination processes can be distinguished, and they depend on the density of electron-hole pairs created per unit path length in semiconductor layers by ionizing particle species. These processes are named geminate recombination and columnar recombination. In the case of geminate recombination the electron-hole pairs density is low, thus the recombined pairs are those barely generated [185]. This recombination is peculiar for an irradiation with electrons and high energy photons. The geminate recombination is strongly linked to the temperature in the presence of near-zero field, on other hand is weak when fields are high [167]. For columnar recombination, the electron-hole pairs density is higher, and the very recent generated carriers can recombine with any other carriers. This recombination type is broadly valid for all energies when the irradiation is made with alpha particles, ions and protons.

Regarding carries transport in SiO₂ at room temperature and zero-field, the electrons mobility is 20 cm²/V·s while for the holes is $1.6 \cdot 10^{-5}$ cm²/ V·s, besides all two strongly temperature dependent [167]. Once thermalization processes ends up, the electrons drift within picoseconds from the oxide and the hole practically stay near generation point. Because of very low holes mobility value their drift motion may take seconds as well as hours. To describe holes drift various models were developed, one is the stochastic transport model called Continuous Time Random Walk (CTRW) [186, 187]. The model agrees with experimental results because takes in to account the temporary capture of hols in shallow

traps plus the polaron hopping process which contributes to localized states. The polaron [188] designates the conjunction between hole and its strain field. Onward, the holes can migrate towards the Si/SiO₂ or gate/SiO₂ interface in the presence of an electric field and their movement give rise to distortion in the SiO₂ lattice local potential field, hence the hole is followed by the distortions. The holes transport over SiO₂ layer is made through the mechanism called polaron hopping [187, 189].

Nearby Si/SiO₂ interface the oxygen can undergo an out-diffusion plus the disordered transition region between semiconductor and oxide layers leads to a high number of oxide vacancy [190]. Considering a positive biased gate, the holes will drift to Si/SiO₂ interface and some fraction of them becomes trapped by oxide vacancies that behave as trapping centres, which the rests recombine with electrons supplied by the semiconductor. Further implication of this process is reflected in device threshold-voltage shift [191]. Also, it is possible that some trapped holes to recombine with electrons. [192]. The electrons traps with insignificant cross-section can be found in SiO₂ layer, but their contribution is neglected [193].

Another process occurring in post-irradiation time is the generation of interface states [194]. Unlike holes trapping, this process is more complex considering its dependence on temperature, time and field. Its build up mechanism is explained by several models. One supported by the bulk of experiments envisage the reaction between positively charged hydrogen H⁺ and the defects localised at Si/SiO₂ interface [195]. The interface traps can have neutral, positive or negative charge [196].

As example the interface-trap charge is neutral at mid-gap because in case of n-channel transistors they compensate with oxide-trapped charge while for p-channel transistors those two add together [196, 197]. When the interface traps are in the lower position of mid-gap, then they are positively charged. In third situation, the interface traps are in the upper position of the mid-gap they are negatively charged. In contrast with oxide-traps, at room temperature the interface traps do not anneal and they have important implication in environments with low dose rate like space [198]. The interface traps affect the threshold voltage and timing parameters of MOS devices.

Annealing of the oxide-trap charges is a process conditioned by time, temperature and the bias voltage. Two mechanisms behind oxide traps neutralisation are:

- the tunnelling effect of electrons into oxide traps from silicon;
- the thermal emission of electrons originating from the oxide valance band within oxide traps.

These two mechanisms where combined in a single mode by McWhorther, et all [198]. The oxide traps must be closely to the Si/SiO₂ interface so that the electrons tunnels from Si in a relatively short time scale. Otherwise, the tunnelling front on SiO₂ evolves at rate of 0.2-0.4 1nm/decade of time [199]. The oxide traps neutralisation mechanism through electron tunnelling has a rate dependent on device fabrication technique [200]. Instead, the thermal emission mechanism is varying exponentially with temperature but not dependent of oxide traps spatial position [198]. Recovery of the oxide charge can be done by reversing the bias [201].

The MOS devices susceptibility on effects induced by ionization phenomena stands in their operating principle of gate controlled currents. A list of post-irradiation effects includes: shift in the threshold voltage; an increase in drain-source leakage current and reduction of breakdown voltage.

2.3 Single Event Effects family

The second category of radiation-induced effects, that of Single Event Effects (SEE), it is triggered by charge deposition into a sensitive volume of the semiconductor devices when a single incoming particle causes the generation of electron-hole pairs along its path. If the charge deposited is above the device sensitive volume critical charge (Q_c), then the SEE occurs. The Q_c represents the minimum charge for a device which leads to the changes of its state. This parameter is settled as result of energy deposition in a critical volume related with the device sensitive volume. Hence, this sensitive volume delimits only the charge collection region. In case of SEE, the charge deposition is governed by the direct ionization and the indirect ionization phenomena, both sketched for a MOS structure in figure 2-8.

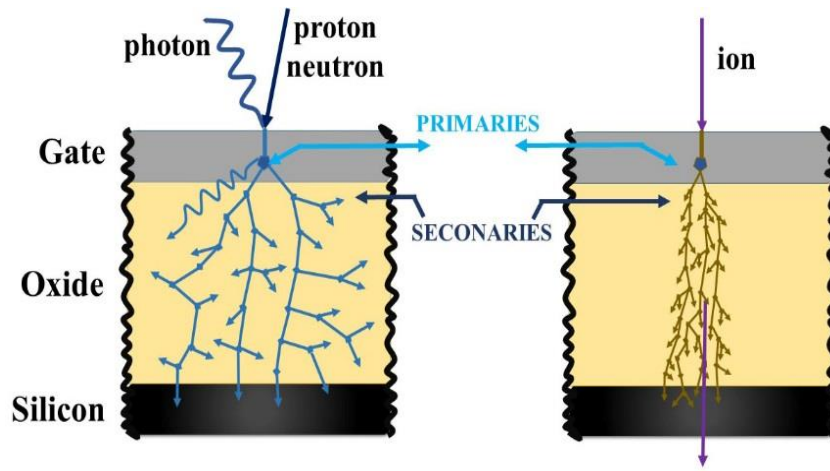


Figure 2-4 Cascades of charges resulting from indirect ionization phenomena caused by light particles or from direct ionization produced by heavy ion (reproduced from ref. [202]).

Single charge particle with atomic number $Z \geq 2$, species of heavy or light ion, produce direct ionization along its path and triggers an engrossment cascades of mobile carriers through device sensitive volume. On the contrary, light particles as high energy protons, neutrons and high-energy photons give rise to indirect ionization phenomena through elastic/inelastic interaction, scattering or spallation.

Thereupon, incoming light particle collision with device lattice atoms can result in production of heavy recoil nuclei and deuterons, light nuclei, α -particles or protons. Following primary interaction, these reactions have the probability to occur conditioned by a specific energy threshold. In table 2-3 are highlighted few of those reactions along with the energy thresholds when the target material is silicon.

As can be observed, most of the reaction products are heavier than primary incoming particle which triggers the event. Also, they do not propagate far from impact point and tend to be forward scattered in the direction of primary particle [203]. Moreover, this recoiling nuclei and ions have likely higher ionization capability, i.e. indirect ionization. Either way, charge deposition due to the direct ionization or indirect ionization may lead to temporary or permanent functional failure of semiconductor device.

Table 2-3 Reactions within Si induced by photons, protons and neutrons (based on ref. [176])

Species	Reaction	Energy threshold (MeV)
neutron	$n + {}^{28}\text{Si} \rightarrow n + {}^{28}\text{Si}$	0.00
	$n + {}^{28}\text{Si} \rightarrow \alpha + {}^{25}\text{Mg}$	2.75
	$n + {}^{28}\text{Si} \rightarrow \alpha + \alpha + {}^{21}\text{Ne}$	12.99
	$n + {}^{28}\text{Si} \rightarrow n + {}^{12}\text{C} + {}^{16}\text{O}$	16.70
proton	$p + {}^{28}\text{Si} \rightarrow p + {}^{28}\text{Si}$	0.00
	$p + {}^{28}\text{Si} \rightarrow \alpha + {}^{25}\text{Al}$	7.99
	$p + {}^{28}\text{Si} \rightarrow p + {}^{12}\text{C} + {}^{16}\text{O}$	16.70
	$p + {}^{28}\text{Si} \rightarrow n + p + {}^{27}\text{Si}$	17.80
gamma	$\gamma + {}^{28}\text{Si} \rightarrow n + {}^{27}\text{Al}$	16.97
	$\gamma + {}^{28}\text{Si} \rightarrow \alpha + {}^{24}\text{Mg}$	17.10
	$\gamma + {}^{28}\text{Si} \rightarrow n + n + {}^{27}\text{Si}$	30.50

SEE's could be classified in three categories based on their temporary or permanent nature. Those which cause a temporary disruption of the device known as upset are: Single Event Transient (SET), Single Event Upset (SEU); Multi-Bit Upset (MBU); Single Event Functional Interrupt (SEFI). Another type of temporary effect that could lead to permanent damage is Single Event Latchup (SEL). Third category is those of permanent damage comprising Single Event Gate Rupture (SEGR) and Single Event Burnout (SEB) [204]. After the charge collection mechanism description, a detailed view of each SEE will be done in the following.

2.3.1 Charge collection and transport mechanism

The direct ionization phenomena induce by heavy charged particles is the primary charge deposition mechanism. When high-energy ion passes through device semiconductor layers it loss energy along the trajectory by excitation and ionization of encountered material atoms. The total path length covered by a particle till comes to rest within semiconductor lattice it is known as particle range. Correlation between particle energy loss and electron-hole pairs generation is dependent on to the stopping power or more exactly on the linear energy transfer (LET). The energy deposited per unit path length depends on particle species energy and mass plus target material density. Formula 2.4 is used to compute the amount energy loss (dE) per unit path length (dx) normalised to the material density (ρ) is:

$$LET(x) = \frac{1}{\rho} \frac{dE}{dx} \quad (2.4)$$

The LET expressed in $\text{MeV cm}^2 \text{mg}^{-1}$ for various ions species and energy have been tabulated [205, 206]. Also, dedicated software tools have been developed , as the TRIM and SRIM, to determine the stopping power and range of ions [207]. The dependence of stopping

power versus penetration depth of particle it is a curve of interest showing the energy transferred over the particle range. Exemplifying, the energy transfer variation over the path of chlorine ion accelerated at 210 MeV which travel into silicon is presented in figure 2-5.

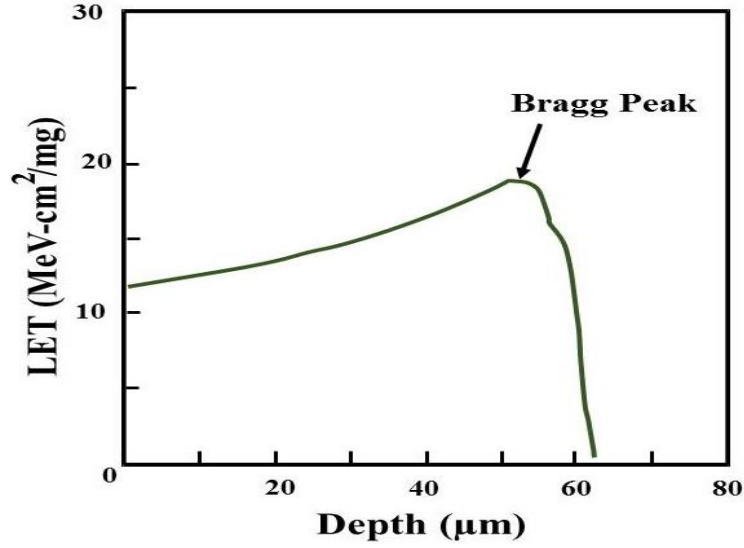


Figure 2-5 The LET as function of depth in silicon for 210 MeV chlorine ion (reproduced from ref. [202]).

Maximum LET region on the curve it is called the Bragg peak corresponding to the range where the ion is near end path reaching an energy comparable to 1 MeV/nucleon [202, 208]. The Bragg peak shifts with the ion energy and increase in amplitude with atomic number Z . Likewise, the LET value is related to the charge deposition per unit path length for a specific particle considering that is necessary a certain energy quantity for electron-hole pairs generation in given material. With the help of formula 2.4 the charge creation along an incremental length into semiconductor material by an ion is calculated, but must also considered the LET variation with penetration depth [28].

$$dQ = L(x) \cdot dX = \frac{LET(x) \cdot \rho \cdot 1.6 \cdot 10^{-5}}{G} \cdot dX \quad (2.4)$$

Where:

- dQ [pC] – differential charge ionized on the incremental length;
- $L(x)$ [pC/μm] – linear charge deposition (for Si is $1.035 \cdot 10^{-5} \cdot LET$ measured in MeV/(mg/cm²);
- $d(X)$ [μm] – differential/incremental length;
- $LET(x)$ – linear energy transfer at incremental point upon particle range;
- ρ [g/cm³] – target material density;
- G [eV] – the electron-hole pair generation energy of the target material (for Si is 3.6 eV).

The charge collection mechanism was extensively studied theoretically and experimentally. High-speed oscilloscopes in conjunction with ion micro-beams and lasers were used to measure the charge-collection transient in Si [209, 210]. Modern equipment allows time and position measurement of integrated charge collection induced in integrated

circuits using ion microbeams and lasers method [211-214]. The charge collection was also intensively studied with the help of software simulation tools [25, 215].

When strikes the semiconductor layers, a high energetic ion loses its energy through ionization and leaves along the path a dense plasma track of electron-hole pairs. There are three mechanisms that govern the charge deposit process and those are: depletion-region drift collection, field-assisted funnelling collection and diffusion collection [28].

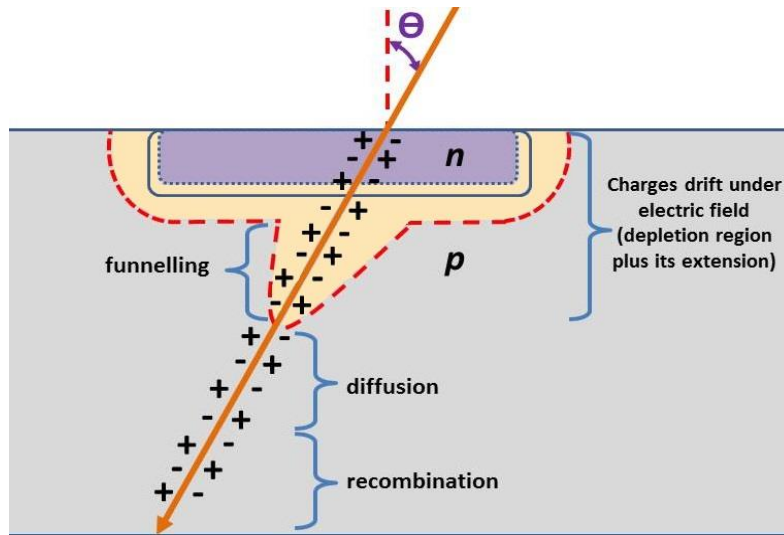


Figure 2-6 Direct ionization triggered by heavy ion in p/n revers biased junction exhibits funnelling, drift, diffusion and recombination (reproduced from ref. [176]).

From ion interaction point of view with semiconductor device, the most sensitive regions are the p/n junction reversed biased because of the high field present in junction depletion region which efficiently channels the induced charge over the drift process. Figure 2-6 represents a conceptual sketch of an ion striking at incident θ angle the revers biased p/n junction.

The electrostatic potential of revers biased p/n junction suffers a transient disturbance, known as field funnel [216]. Further, the highly-dense free carrier track along the ion path collapse the junction electric field due to the established charge track well conductive nature. At the struck node, the charge collection is improved by the funnelling effect considering the junction electric field extending depth within p substrate. Thus, the electron-hole pairs generated can be collected at some distance outside of the nominal depletion region through drift process. The electron-hole pairs away of any electric field influence may recombine close to the generation point or could be transported by diffusion. Once the concentration of free carriers diminishes and the carriers equilibrium is re-established, then the funnel vanishes.

Collected at the corresponding junction points, the electrons in n-region and the holes in p-region give rise to so called single-event (SE) current made up of a prompt and a delayed component, see figure 2-7. The prompt component of SE current spanning around 500 ps it is related to the charge collection over drift process in the junction nominal depletion region plus funnel region [28, 176]. The delayed component over 1ns in duration it is assigned to the carrier diffusion up to funnel or depletion edge where they are collected by junction electric field. Sometimes the delayed component can last 1 μ s or even longer, to a large extent in lightly doped substrates [215]. Probability exist that charge collection to occur even when ions near misses the depletion region but the carrier diffuses to it, leading to funnelling effect [217].

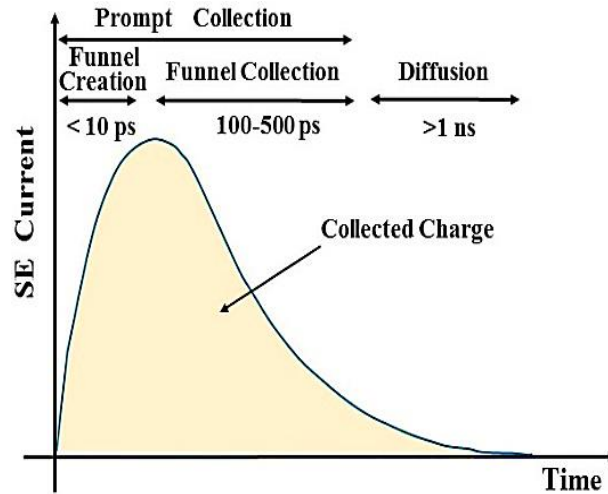


Figure 2-7 The single-event current flow versus time at a junction and charge collection (reproduced from ref. [28]).

The single-event current flow must be overcome in cutting edge integrated circuits implemented in sub-micron technologies, where the period of normal circuit signals becomes comparable with the parasite single-event transient pulse. Given their very dense geometry embedding over ten billion transistors per chip, another phenomenon was found to take place due to a single ion strike. The ion shunt collection occurs when an ion track goes through two proximal junctions [218, 219]. Considering a semiconductor structure of n^+p - n layers which can be struck by an ion it could lead to a current conduit between the two n regions. The connection between the two regions as a result of the plasma track left behind by a passing ion is named ion shunt [220]. This process increases the current flow on semiconductor layers over a very short period till the plasma track collapses. Semiconductor fabrication technologies as CMOS on thin epitaxial layers or the bipolar one are very susceptible to this effect [221].

For submicron semiconductor devices, another charge collection mechanism was discovered with the help of 3D alpha particle simulation. Afterwards experimentally confirmed, the alpha particle source-drain penetration effect (ALPEN) [222] manifests itself through channel electrostatic potential disturbance in MOS transistors induced by a single particle traversing at a near-grazing angle of incidence both source and drain. Occurring promptly after the particle strike, a short-lived source-drain conduction current is induced as a result of the disturbance in channel potential, thereupon mimicking the MOS transistor ON state. Later this direct channel conduction was observed in $0.3\ \mu\text{m}$ MOSFET, even at various angles of incidence [223]. This mechanism constitutes a big problem for deep submicron devices from SEU vulnerability standpoint.

Further implication of ion strikes, funnelling, charge collection and SE pulse will be addressed in the next section where non-destructive or destructive single-event effects will be presented in detail.

2.3.2 Single Event Transient

Charge collection within device sensitive volume becomes the root of single event upsets when an energetic particle strikes into a critical node of its semiconductor structure. This class of non-destructive radiation induced effects manifests as a transient or new stable state during device normal operation mode. Since its postulation, the Single Event Transient

(SET) was predicted to cause very serious reliability issues in upcoming dense integrated circuits [224]. The SET is a fleeting disturbance in voltage or current following immediately after the particle strikes within semiconductor lattice. At the signal level the SET phenomenon is modelled in the simplistic way as sum of two exponential functions.

Either affecting the digital and analog integrated circuits, the susceptibility to SET is conditioned by circuit technology, design, and on clock frequency [225-227]. Shrinking transistor size in today state of the art submicron devices and new materials added in the fabrication process have risen new challenges related to the immunity against SET. In this context, the probability increases as a single particle becomes likely to hit two adjacent transistors affecting their drain junctions, thus inducing multiple event transients. The struck transistors feed-back which is known as pulse quenching [228]. Charge sharing among neighbouring cell can perturb the circuit running. Given the fact that charge multi-collection is possible to take place in the same time scale, the outcoming downstream SET pulse may be shortened and even dim due to simultaneous perturbation of circuit by multi-event [229].

Classified as digital or analog, the SET is characterised by following proprieties: pulse width, amplitude and shape. The SET critical width is defined as minimum transient pulse width necessary for this phenomena to be propagate through an infinitely long chain of inverters [230]. If the transient width is well below critical width, then the SET pulse will vanish only passing over few logical gates because their transistors would not have the speed required to respond to the transient. In literature it is considered that a SET pulse with the width at half of the critical one would end in the first gate [231]. In contrast, SET pulse having width values exceeding critical threshold would propagate infinitely. With the CMOS downscaling, the critical transient width decreases, and this means narrower SET shape signal under 10 ps which propagates trough submicron integrated circuits. Beside technology dependence, the SET span and further propagation is also conditioned by particle LET [232]. Therefore, SETs induced by ions with higher LET are more likely to propagate.

Initially highlighted in the digital circuits [233, 234], the SET phenomenon induce errors either in combinatorial or sequential logic elements. Energetic particles can strike aside from combinatorial logic elements also clock, data and global control lines. Effects seen as signal disturbance might be further interpreted as valid signal. The SET propagating through subsequent circuitry can change the logic state of an element if encounter in its path a latch or other memory elements. This means SET becomes SEU due to latch. Several criteria must be satisfied for a SET to end up in a circuit error [233]. They are the following:

- a particle striking the semiconductor device must give rise to a transient pulse that can propagate through circuitry;
- it is mandatory to be an open logic path over which the SET propagate and reach a latch or other memory element;
- the SET must have enough amplitude and width to trigger a change in the state of the latch or memory element;
- for sequential logic the SET precondition is to arrive within transition time interval during the clock edge when data latching is enabled.

The SET pulse capture as valid data has a probability increasing linearly with the device operating frequency [235]. Therefore, the total error rate induced by energetic particle upon a device exposed to radiation is given by the sum of clock dependent SET error rate and the single event upset (SET) rate which is clock independent [230]. The simplest way to grasp how a SET can led at SEU it is to consider a chain of non-latching logic elements feeding at the end a register input. Depending on transient pulse position in relation to the clock edge

responsible for writing and triggering the data into register there are several scenarios drawn in figure 2-13.

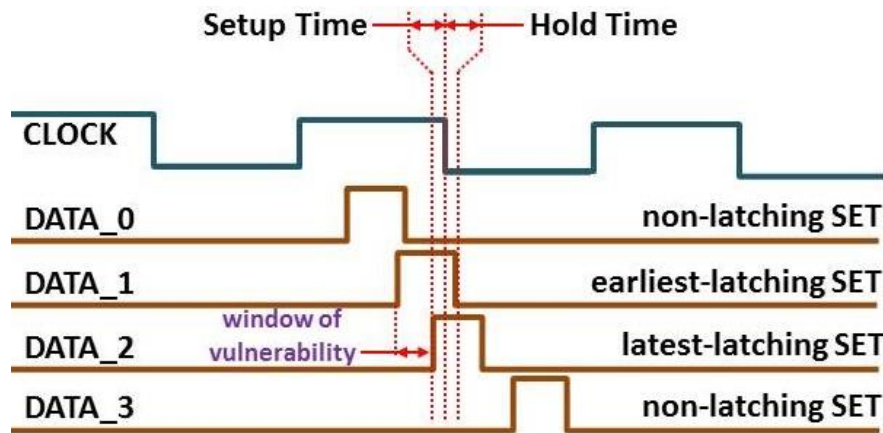


Figure 2-8 Time frame circumstances in which a SET is latched as error (reproduced from ref. [230]).

The window of vulnerability is the time interval when input data is validated to be latched into register or others memory elements. If the transient pulse overlaps with the window of vulnerability interval, then the SET is latched as valid data. Also, it is obvious that the probability of latching SET to occur is close related to circuit driven clock frequency. Moreover, in present days the circuit timings have become similar with the charge deposition-collection time interval and the paradigm of clock cycle lasting less than SET turns to be an unavoidable one. Further implication of the SET propagation includes production of SEE as SEU, MBU and SEFI. Earlier the SET were considered insignificant in digital circuit error rate since the phenomenon was dissembled by logical, electrical and latching windows [236, 237]. In fact, the SET gets observable after propagating to the output pads or caught in synchronous latches, but not at generation site.

Due to the incertitude about the time when a SET is generated in integrated circuits and the little information on its origin in the dice, it is very challenging to isolate the chip region predisposed to transient. In general, the SETs are observed in a time interval over which the system clock could pass many cycles and travelled through multiple circuit nodes. Induced by single energetic particle in a circuit node, just one SET might propagate on multiple paths and induce in the end as multiple upsets [230]. The propagation tree paths of a SET in the device logic elements is characterized by transient width and the number of passageways along elementary logic cells. The term assigned to this propagation of SET within logics trees is named propagation induced pulse broadening (PIPB) [238]. A circuit node sensitivity to SET is dependent on operating voltage, nodal capacitance, interconnections resistance, transistors layout (gate length and width). The integrated circuits downscaling entails low power devices with low operating voltage and nodal capacitance, thus more susceptible to SET because they require less charge deposition and collection to give rise at a transient voltage or current pulse.

Regarding the analog and mix signal integrated circuits, a selection of built in elements prone to SET include: low and high voltage elements, high frequency elements, feedback loops, cross coupling, nodes with low value of current drive restoring and high gain stages [239]. Commonly, the SET occurring in analog part of a device is observed as a glitch in expected output voltage level. Studies on this topic reported data characterising the SET in correlation with various parameters of analog integrated circuits such as supply voltage or signals amplitude versus its width [240-242]. Often the initial transient signal may be

amplified and widen in analog circuit, therefore resulting a transient pulse with high amplitude and duration [243]. Optoelectronic device and sensors plus data transfer systems over optic fiber are predispose to SETs, especially the photodetectors [244, 245]. These relative complex systems embeds numerous electronic components which in their turn contribute to SETs rate [239].

The SETs tend to have large contribution to error rate in the modern faster and denser submicron semiconductor devices. Otherwise, in the literature has been prognosticated that SET will become endemic for digital nanometric integrated circuits [246]. Besides software simulation tools developed to study and analyse this phenomenon, also mitigation techniques at system, device layout and software level are under continuously development to better overcome the negative impact of SET.

2.3.3 Single Event Upset and Multi Bit Upset

The single-event effects are produced by high energetic particles striking sensitive regions within device semiconductor layers that lead to changes in logical state or transient disruptions latch as valid signals in digital devices. All those produce soft errors in data storages and malfunctions in programmable devices due to faults induced by radiation in configuration memory, program counter or instruction registers.

The Single Event Upset (SEU) [247] refers to change of state in logic elements, actually a bit flip, which can results either through direct or indirect ionization when a single energetic particle strikes a semiconductor based memory device. This phenomenon was initially forecasted in a paper assessing microelectronics scaling trends towards minimum volume of semiconductor device state that will be restricted to 10 μm on a side because of the SEU induced by terrestrial cosmic rays [224]. Subsequent, the SEU had been observed first time in the electronics on-board of communication satellites [248] and shortly after in terrestrial microelectronics as a consequence radioactive contaminants contained in ceramic package [62, 249]. Nowadays, downscaling to submicron scale makes the semiconductor device more prone to SEU. The single-event vulnerability has been outlined by the SEMATECH National Industry Association Roadmap among the mainstream metrics for integrated circuit reliability [250]. The hardening and mitigation techniques are opened and core research topics in designing SEU tolerant devices. Further it will be explained the SEU mechanism in two of the fundamental memory circuits cells.

The information storage device based on Dynamic Random-Access Memory (DRAM) technology refers to low-cost and high-capacity memory semiconductor component in which binary information is represented by packets of charge stored passively. The physical design of storage structures encountered in DRAM includes various layouts from staked capacitor to buried trench capacitors. Since there is no active regeneration path for charge packet, a high energetic particle may strike and loose its energy through ionization into the sensitive volume of memory cell, resulting in cell logic state change that can be corrected only by an external circuit. The difference between logic state 1 and 0 is given by so called critical charge Q_{crit} that stand for minimal amount of charge required to be collected at a sensitive node for inducing a circuit upset.

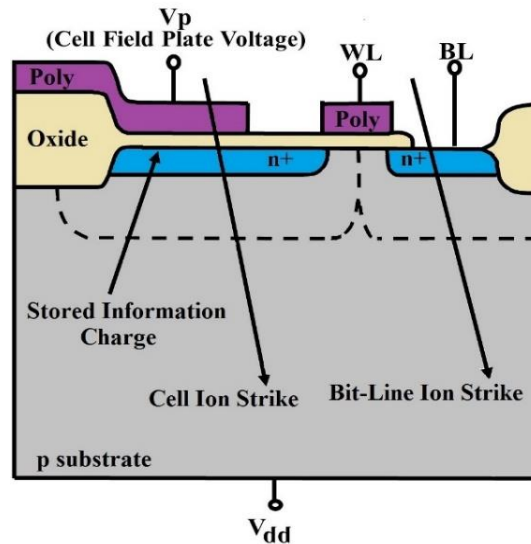


Figure 2-9 Physical layout of one-transistor DRAM cell outlining ions strikes in storage cell and bit-line (reproduced from ref. [251]).

A few mechanisms responsible for SEU occurrence in DRAM are pointed out in figure 2-10 and they are triggered by a particle striking the storage cell or bit line. A list of mechanisms leading to DRAM memory upset induced by ionizing radiation encompasses:

- charge collection as result of single event strike directly in storage capacitor or near it, plus the strike in the access transistor source are common soft error causes in DRAM arrays that are usually detected as 1 to 0 logic transitions [62];
- the ALPNET (alpha particle source-drain penetration effect) mechanism in DRAM leads to shunting charge into storage node, so by ion strike the transition from 0 to 1 it also possible [222];
- similar to ALPNET a phenomenon has been observed in trench type DRAM which occurs when two adjacent trench storage capacitors were crossed by a ionizing particle [223];
- during read cycle the bit-line is in floating mode and the DRAM cell is prone to charge collection in diffusion region, therefore a direct strike in access transistor drain or sense amplifier can result in an upset [252];
- the combined cell-bit line (CCB) failure mode [253] is a synergistic effect of charge collection over the bit-line and in storage cell, each contributing individually with less charge than Q_{crit} threshold, but under memory read operation together add and generate an error.

The DRAM susceptibility to SEU is strongly related to the storage cell technology [254]. The studies have revealed sever impact within soft error rate determined by various physical storage structure used in DRAM [255].

The Static Random Access Memory (SRAM) designates a high speed broad class of volatile storage device which hold 1 bit of information using two cross-coupled inverters implemented with four transistors, see figure 2-11. Another two access-transistors, not draw on schematic, are used to manage the memory cell read-write cycles.

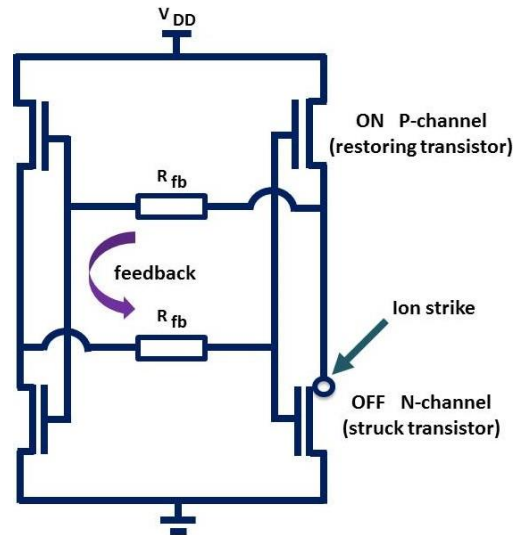


Figure 2-10 Sketch of SEU scenario in basic circuitry of a SRAM memory cell (reproduced from ref. [251]).

There are four sensitive nodes on SRAM circuitry, represented by the drains of each transistor that once struck by an ionizing particle can lead to SEU in the memory cell. Typically, the reverse-biased drain junction belonging to n-channel transistors biased in “off” state it is the most prone to be negatively affected by a particle strike, considering the charge collection that immediately gives rise to the transient current pulse [256, 257]. A balance attempt rises from the source current of the restoring transistor as a response to the transient current flow occurred in the struck transistor. Further, the current flow through “on” p-channel restoring transistor induces a voltage drop at its drain. This voltage transient is like a write pulse and it can trigger the latch of a wrong memory state. Therefore, the mechanism governing the SEU occurrence in an SRAM cell is due to the voltage transient [251].

Charge collection mechanism in the struck transistor is dramatically influenced by the physical layout of the SRAM cell, with the drain junction being located in the substrate or inside a well [256]. When it is situated outside the well, the charge is deposited in the reverse-biased drain by an incident ionizing particle deep in the substrate from where it can diffuse from the substrate to the drain junction [257]. For the inside-the-well alternative, the charge deposition deep within the substrate is prevented by the potential of the well-substrate junction. On the other hand, this technology is vulnerable to shunt and bipolar effects that may happen in a multilayer structure [258]. The upset process is initiated for an inside-the-well strike due to the initial drift current which lowers the struck node potential. The transient pulse occurrence influences the well potential, which is increased as a consequence of hole deposition in the p-well and collected at the p-well ties. The well potential increasing triggers the transistor source to inject electrons, initiating so-called inside-the-well [251, 259]. While the electrons collected by the substrate tie to (V_{DD}) do not contribute to the SEU mechanism, the ones collected by the n-drain induce a bipolar current adding to the initial photocurrent, leading to an upset in the SRAM cell [256].

The SEU can occur in an SRAM cell even if the LET of the particle which strikes the sensitive node is below the upset threshold. Despite low LET, the particle can induce a significant voltage transient at the struck drain. In this situation, the upset emergence is conditioned by the competition between the voltage transient over the opposite inverter and the cell recovery process [260]. Subsequently to a particle strike, an SRAM memory cell recovery time depends on strike location, particle LET, and technology aspects like the current drive of the restoring transistor, or minority carrier life time in the substrate [260, 261]. Regarding the feedback time, it is ascribed to the necessary time interval for the disturbed node voltage to feed back by way of cross-coupled

inverters and become latched as stable state, thereupon as SEU. The feedback time is related to the cell write time and calculated RC time constant in inverted pairs. A smaller RC time constant means faster SRAM cell response to voltage transient, so higher susceptibility for upsets to be induced by low LET particles [251].

Soft errors in both SRAM and DRAM or other semiconductor based storage technology can turn up in form of multiple upsets within memory cells due to a single high energetic particle strike [262, 263]. This type of error is called Single-Event Multiple Bit Upset (MBU) initially observed on board of space probes equipped with 1Kb RAMs [264] and confirmed latter by numerous ground-based testing. There are two classes of mechanisms leading to MBU occurrence [265]:

- the lateral strike where at grazing angle of incidence the impinging particle pass through multiple sensitive volumes across the device die [263];
- a high Z particle strike at other than near zero incidence angle may upset close cells either if its track diameter spans over their sensitive volume or the incoming charge from the track diffuses to sensitive regions [266].

Usually the MBU occurrence through the second mechanism is observed as a clustered of upsets on the memory cell array. Another important aspect is that MBU can be expected on a single memory word or in multiple words, but the single-word multiple-bit upsets (SMUs) is more damaging for the logic integrity [267].

Mitigation technique for MBU has been developed at the system level consisting in memory scrubbing procedure accomplished with cyclic redundancy check (CRC) and Hamming codes or simply rewriting entire information words. While from physical layout standpoint, most common method is memory cells interleaving of different memory words. Practically, the MBUs become rampant with semiconductor device downscaling trend, so for denser storage capacity.

2.3.4 Single Event Function Interrupt

Another non-destructive single event from general category of SEU it is so called Single Event Function Interrupt (SEFI) [268]. Otherwise observed long time ago [269], the SEFI phenomenon emerged with complex integrated circuits and manifested itself through a disruption of device operation after a sensitive volume of its architecture was strike by a single high energetic particle. As result of SEFI occurrence, changings in devices operation were reported for a wide range of devices including DRAM, EEPROM, DSP, microcontroller, microprocessor, SRAM based FPGA [270-273]. For instance, an upset into instruction register of a microprocessor is very likely to let the device in an unknown state or to lock-up the program execution [270]. In similar fashion, the FPGA cease to operate when particle strikes dedicated built-in memory bits belonging to the device control register or state elements, therefore SEFIs crop up.

Usually, the SEFI do not come along with high increase in device current consumption, which is the signature of other radiation-induced single events. The device normal operation is restored by doing power cycling and subsequent re-initialization after a SEFI. The probability for SEFI to occur is low, in fact the SEFI cross-section is relatively small comparing to SEU, but on the other hand it is hard to be localised taken in account that the upsets sensitive region of device where there is no direct access. Thus, a deep understanding of device architecture and functioning is necessary to identify the built-in elements predisposed to SEFI.

2.3.5 Single Event Latchup

Aggressive downscaling of semiconductor device persuade many impediments to be overcome such as latchup, which is a regenerative current flow condition triggered by two cross-coupled parasitic bipolar transistors forming a semiconductor controlled rectifier (SCR) into semiconductor with p/n/p/n structure. [274, 275]. In general, this thyristor structure is encountered in CMOS technologies where an n-channel transistor is coupled to a p-channel transistor like in SRAM cell. Figure 2-12 exemplify this in bulk CMOS technologies for a parasitic latchup circuitry consisting in a parasitic lateral NPN bipolar transistor having n-channel source as emitter, the base is p-substrate and the collector the n-well plus the parasitic vertical PNP bipolar transistor with p-channel source as emitter, the base in n-well and the collector in p-substrate. In addition to the complementary bipolar transistors (BJT) structure are parasitic wells and substrate resistances.

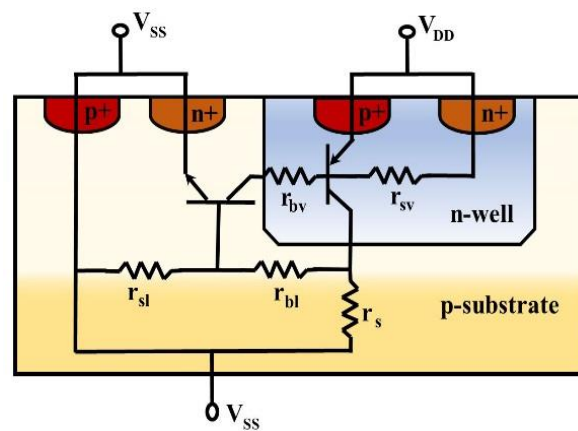


Figure 2-11 Layout of an CMOS inverter circuit along with the two parasitic bipolar transistors (reproduced from ref. [276]).

Normally the thyristor is in high-impedance off state but might be turned on by transient voltage as consequence of: device improper sequencing of power supply biases, transients over input/output lines or elevated temperature, all this leading to so called transient-induced latchup [277, 278]. Thus, high energetic particle can trigger-on this parasitic structure which further leads to a low resistance path between power supply rails resulting in the single event latchup (SEL) phenomenon. The mechanism of SEL triggering has not less than four main steps according to some literature sources [276] and these are:

- particle strike in the well substrate junction triggers a transient current, further creating a voltage drop within the well correlated with the well resistivity and depth, also considering the hit location from the well tie contact;
- the current flow in to the substrate would be amplified only when the voltage drop into well is sufficiently high to forward biasing the parasitic vertical BJT;
- current injected into the substrate causes a voltage drop within the substrate leading to the forward biasing the parasitic lateral BJT and the positive feedback is sparked by the collector current of lateral BJT feeding the base of vertical BJT;
- once the regenerative feedback is initiated, then current rises rapidly and the device step in latchup though the particle induced transient current.

Therefore, the latchup condition is only accomplished when one of the two parasitic BJTs is forward biased and the feedback loop is initiated. Typically, the vertical parasitic BJT is forward biased first when the particle strikes the sensitive volume because the lateral one requires more charge to be turned on in higher angles of incidence [279].

A first order requirement is to have the product of the two parasitic transistor betas greater than 1 as the latchup to be sustained [230]. Taking into consideration the parasitic thyristor current-voltage characteristic, to maintain the latchup condition it is necessary to have the device current higher than the holding current and the supply voltage higher than holding voltage. Moreover, the semiconductor device vulnerability to SEL is dependent on increasing of supply voltage and temperature [280]. To determine the SEL threshold for a device it is recommended to do the test under the worst case scenario of maximum operating voltage and temperature [168]. Also during exposure, it is important to tilt the device under test at a large number of angles with respect to the incident beam in order to reveal all latchup paths [168].

The detection of SEL occurrence is done by monitoring the device current consumption. A considerable increase in device current consumption is the distinctive signature for a SEL and after the device is power cycled it will disappear. In case it is not removed quickly, it may lead to device permanent failure through overheating and burnout, the metallization and bond wires unfastening [281, 282].

Another phenomenon observed in these large current flows (only in n-channel MOS transistors triggered by high energetic particle), it is the so called single event snapback (SES) [283, 284]. The regenerative current mechanism is kept up by a parasitic NPN transistor when a single energetic particle induces an avalanche multiplication in proximity of the n-channel MOS drain junction. Unlike the latchup, the SES do not need to occur in p/n/p/n/ semiconductor structure, require a much higher holding voltage and current and it vanish when the n-channel MOS transistor is turned on without doing a device power cycle [168]. Usually it is observed in the device internal bus drivers or output buffers.

2.3.6 Single Event Gate Rupture

In MOS transistors a localized breakdown can take place into dielectric material when a single energetic heavy-ion strikes the gate region triggering the destructive phenomenon known as single event gate rupture (SEGR) [285]. A permanent rupture of insulating gate dielectric is caused by this type of SEE when the following two conditions are satisfied:

- through dielectric material is initiated a high conductivity path by the heavy-ion strike;
- the device must hold enough energy to be immediately released along the plasma filament induced by the heavy-ion strike.

The SEGR formation mechanism requires that in the heavy-ion travels across the MOS capacitor that consist of gate conductor, dielectric material and silicon substrate, further it requires the forming of the highly conductive plasma path through dielectric over which the capacitor discharges [168]. Considering the second statement above fulfilled, the prompt discharge of MOS capacitor is accompanied by excessive heat release which can lead to the thermal runaway. All this makes the gate dielectric to melt and even evaporate and the conductive layers to overly.[286]. Initially the SEGR was observed in metal nitride oxide semiconductor (MNOS) dielectrics [287], next in power MOSFET's [288] and MOS transistors [286]. For instance, built-in transistors of SRAM and EEPROM storage devices are vulnerable to SEGR during write or clear operation favoured by the high oxide electric fields

condition. Extensive studies were carried on MOSFET transistors [289-291]. For example, in the structure of vertical power MOSFET the location prone to SEGR is the neck region strike by energetic particle through the gate oxide [292].

Failure threshold for MOS gate dielectric is dependent on several factors such as: heavy-ion LET and angle of incidence, device biased condition, particle path length and dielectric thickness and its critical electric field [293]. Susceptibility to SEGR increases with gate voltage, particle LET and its path length.

As the transistor layers become comparable in thickness with ion track diameter, the dependence law changes [294]. Investigation of very thin gate dielectric materials, under 5 nm, to SEGR susceptibility revealed a distinct behaviour comparing to the thicker oxides and rather than a hard breakdown, they suffer a soft breakdown leakage currents [295, 296]. In attempt to do more insights into SEGR phenomenon statistical and mathematical models for its prediction continue to be developed [297, 298].

2.3.7 Single Event Burnout

Second kind of SEE destructive failure mechanism encountered in power transistors operating in radiation environments it is the single event burnout (SEB) [299]. Observed both in power MOSFET and bipolar power transistors [293, 300], this phenomenon can be triggered by heavy ions, energetic neutrons [301] and protons [302]. By default, the power MOSFET transistor structure inherits a parasitic bipolar transistor and considering a n-channel MOSFET the basis of parasitic transistor is the anchored p-body, the emitter in n-source and the collector in n-type epitaxial region. When the device is in the 'ON' state, the parasitic bipolar transistor has the base shorted to emitter, while for the 'OFF' state those terminals become disconnected. Usually in 'OFF' state, this power device withstands high blocking voltage, but it is also vulnerable to SEB. For instance, if an heavy ion strikes the n-type power MOSFET being in 'OFF' state, then the transient current pulse might forward bias the emitter-base junction turning 'ON' the parasitic bipolar transistor and triggering a regenerative feedback mechanism, snap-back or 'second breakdown' [230]. Referring to the second breakdown, it is a high current condition combined with an abrupt drop in breakdown voltage, whilst the ion track created a plasma filament linking together the MOSFET source and drain through a low resistive path. This condition leads to prompt device damage if the current flow through device is not limited. On the other hand, the high fields present at the p-basis/n-type epitaxial region condition the avalanche multiplication [303]. This is the basic element for regenerative feedback which leads to the parasitic bipolar transistor collector current increasing to the point of junction overheating beyond ultimate burnout the device if no external current limitation or supply cut-off is applied.

A deeper understanding of SEB physical processes was achieved with the help of models and 2D or 3D numerical simulations [304-306]. A simple one was Current-Induced Avalanche (CIA) model used to describe the field and charge distribution with the increasing of current level in device [307]. Next model in line focused on regenerative feedback mechanism better parameterisation [308]. From experimental stand point, several solutions were found to perform non-destructive SEB tests on power devices. The easily available one is to attach a load resistor at the device under test drain for limiting the current flow [309]. Further, the SEB arising is detected as a current pulse at source terminal. Another technique allowing the measurement of charge collected during SEB is titled 'Energetic Particle-Induce Charge Spectroscopy' (EPICS) [310]. Otherwise, the p-channel MOSFETs are tolerant to SEB because the impact ionization coefficient for holes is well under the electrons one [308]. In other order, an increasing temperature is decreasing the impact ionization coefficient of

electrons, therefore the n-channel MOSFETs sensitivity to SEB diminishes [311]. Despite having identical SEB threshold in both static and dynamic regime, the same MOSFET has an SEB cross section higher in static bias rather than in dynamic regime [312]. Extra study investigated the MOSFET structure vulnerability dependence on ion strike position and track with the device [313]. Among the mitigation techniques against SEB must be mentioned the following: the resistance decrease for the base region of parasitic bipolar transistor, lowering the drain-source bias conditions, changes in doping level of different region of MOSEFET structure [307, 314]. The SEB phenomenon remains a core topic for research community addressing radiation induced effects and systems reliability in harsh environment with radiation background [291, 315-317].

2.4 Single event phenomena measurement

Semiconductor device reliability and behaviour in environments with radiation background it is extrapolated based on data obtained through numerical simulations and calibrated through costly irradiation campaigns. Monoenergetic beams of ions species, proton, neutron, alpha and X-ray available at different testing facilities are used to cover the requirements of a radiation hardness qualification study for a certain electronic device. Also rad-hard studies could be carried out in mixt radiation field, thought there are few facilities available, and one of these is CHAMR [318]. Test procedures for SEE need to be done in agreement with normative references like ASTM 1192 [319], ESA/SCC 25100 [320], JESD57 [321] and JESD234 [322].

The electronic device sensitivity to different kinds of SEE is estimated from cross section (σ). For a given particle, the probability to induce a certain type of SEE can be calculated by counting how many times the event occurs when the number of particles impinging the device active area is known. Thereupon, σ represents the number of events divided to the number of particle per chip area expressed in cm^2 that induce the upsets. The effective cross section is calculated according to formula 2.5 [323, 324].

$$\sigma_{(LET_{eff})} = \frac{N_{events}}{\Phi_{eff} \cdot t \cdot \cos(\theta)} \quad (2.5)$$

$$LET_{eff} = \frac{LET_0}{\cos(\theta)} \quad (2.6)$$

$$\Phi_{eff} = \Phi_0 \cdot \cos(\theta) \quad (2.7)$$

Where:

- N_{events} – the number of upsets;
- θ – tilt angle;
- t – exposure time;
- Φ_0 – beam flux on normal direction perpendicular to device surface;
- LET_0 – linear energy transfer at normal angle of incidence on device.

Formula 2.5, respectively 2.6 were introduced to correct the effective value for the LET and flux when the device is tilted with respect to the normal direction. The cross section can be expressed per device or per bit if the events are SEU. Also, for heavy ions the cross section is measured as function of their LET, while for protons and neutrons as function of their incident energy because they induce SEE though indirect ionization mechanism where magnitude is strongly correlated to the incoming particle energy. Conceptual cross-section

curve versus ideal one are represented in figure 2-13. The LET threshold (LET_{th}) and the saturation cross section (σ_{SAT}) are defining parameters for the cross-section curve. Considering the SEU phenomenon, the LET_{th} stand for lowest value of the linear energy transfer that a heavy ion needs to deposit as higher amount of charge than critical charge in the sensitive volume, therefore necessary to induce upset in the most sensitive region of the chip. Contrariwise, the σ_{SAT} designate SEU occurrence over the total are of sensitive regions on this chip.

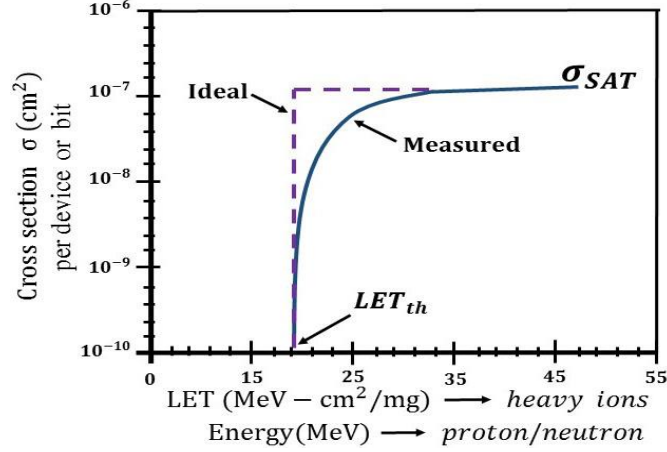


Figure 2-12 Ideal versus measured cross-section curve as function of LET or energy (reproduced from ref. [168]).

As expected, the cross-section curve for a device should be a step function with value for LET_{th} and σ_{SAT} well-defined. Nevertheless, the sensitive nodes across the device are not identical and the upset threshold vary, so the measured cross-section curve is no more a step function and the LET_{th} value is set by the most sensitive cell upon the chip. Commonly, the shape of measured cross-section curve for majority of devices is described by Weibull function [325]. The mathematical expression describing this function is given in formula 2.8 with the empirical fitting parameters W and s .

$$\sigma(LET_{eff}; \sigma_{SAT}; LET_{th}; s; W) = \begin{cases} \sigma_{SAT} \left(1 - \left[e^{-\frac{LET_{th} - LET_{eff}}{W}} \right]^s \right) & LET_{th} \geq LET_{eff} \\ 0 & LET_{th} < LET_{eff} \end{cases} \quad (2.7)$$

With the LET increasing more and more sensitive volume are upset, so the measured cross-section curve is in fact a cumulative distribution of cross-sections for all individual sensitive volumes over and within the device dice. According to the testing standards for SEE, the LET_{th} value required to produce a specific SEE it is identified selecting the ion type which induce just one event to a particle fluence of 10^7 ions cm^{-2} . While the semiconductor based device immunity to SEE it is defined for LET_{th} higher than $100 \text{ MeV cm}^2\text{mg}^{-1}$ [326].

2.5 Conclusions

Extensive semiconductor device downscaling governed by Moore's Law led to high-end integrated circuits embedding miscellaneous features. Nevertheless, unavoidable challenges continuously need to be overcome in this field. As example, once the commonly CMOS technology reached 45 nm and the gate oxide thickness approached 15 Å new material such high-k dielectric were introduced to ensure a low leakage current. On the other hand, outstanding performance of COTS devices makes them very attractive for safety-critical application meant to run in environments with radiation background. Transistor shrinking trend in conjunction with dense integrated circuit come along with downside from radiation tolerance stand point, especially for SEE phenomena. Decreasing the transistors size on chip, therefore reducing the sensitive volume and critical charge plus lowering the operating voltages, make the submicron technology more prone to SEE.

Throughout chapter a comprehensive view was given for each known radiation-induced phenomenon belonging either to cumulative or single event radiation induced effects. Both COTS and radiation-hardened devices are subject to radiation hardness qualification tests before their usage is validated in environments with specific radiation spectra as that of space and high energy particle accelerators like LHC. Also, it is important to distinguish during rad-hard tests among the numerous effects that might occur in the device under test as well as identifying peculiar effects for which the device is less tolerant. Constant attention and efforts are dedicated for increasing the semiconductor device immunity against radiation environments threats. Mitigation techniques at device, system and application level are developed. Moreover, steps were taken towards improving numerical simulation tools has been made. A better understanding of radiation induced phenomena is possible by their means. Regardless they are costly, time consuming and human power demanding, the radiation hardness qualification tests remain the only straightforward solution for devices radiation tolerance evaluation. Based on experimental data, the device behaviour can be extrapolated for different environments with specific radiation background.

CHAPTER 3

Multi Anode Read-Out Chip family

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3. Multi Anode Read-Out Chip family

The CNRS-IN2P3-Ecole Polytechnique microelectronics design centre or shortly the OmegaMICRO developed a wide range of front-end ASICs dedicated to detectors and sensors in the experimental field of astrophysics, particles and nuclear physics plus medical imaging [327]. One of them is the Multi Anode Read-Out Chip (MAROC) family developed for the MaPMT read-out or similar photodetector technology. The second generation of this ASIC family, MAROC2, was successfully used in the ATLAS luminometer [328]. While in the context of LHCb Upgrade Program, MAROC3 was a backup solution for the front-end read-out of the two RICH sub-detectors [116]. Because of the intense radiation field inside the LHCb detector, MAROC3 was included in the radiation hardness campaign of LHCb Upgrade program. The Romanian LHCb Group was in charge with the radiation tolerance study of MAROC3 [329]. Part of the work that has been done to test this chip under radiation will be presented in the current chapter.

3.1 The MAROC3 architecture

Being the third generation of a Multi Anode Read-Out Chip family designed by the OmegaMICRO, the MAROC3 chip was implemented in AMS BiCMOS SiGe 0.35 μm technology node with a power consumption of 3.5 mW/channel. This ASIC is dedicated to the read-out of 64 channels from a MaPMT [330]. In terms of design features MAROC3 was implemented to: correct channel to channel gain spread of MaPMT; generate 64 trigger signals corresponding to the 64 photomultiplier tube anodes; processes with essentially 100% trigger efficiency for input signal values starting from 50 fC (1/3 photo-electron equivalent) up to 1.6 pC. The channels cross talk is about 1% and the noise of 2 fC [331].

Block diagram of MAROC3 is represented in figure 3-1 [331]. Its architecture is based on a digital part with schematic delimited by the yellow rectangle in figure 3-1 that is used by each analog part of the 64 channels. The schematic of a single analog channel is marked in blue. Each analogic channel input has a low impedance preamplifier capable to correct the MaPMT gain spread. Further, the preamplifier output feeds with a signal on several chain with on path for the charge measurements and the other for the trigger generation [332].

Charge measurement is done by applying signal from the preamplifier output to the Slow Shaper which in turn feeds two Sample and Hold (S&H) buffers dedicated to the charge storing of a 2 pF capacitor. The charge digitization is carried out using the 12-bits Wilkinson ADC working with S&H buffers. The analog multiplexer allows access to the signal for each of the 64 channels that will be measured [330, 332-334].

Trigger generation in single photo-electron counting mode is accomplished either with the Unipolar Fast Shaper or the Bipolar Fast Shaper in conjunction with the discriminator which has the threshold set by DAC0. If the input charge is high, then the triggers are obtained using the Half Bipolar Fast Shaper followed by its dedicated discriminator that has the threshold set by DAC1 [330, 332, 334]. Both digital to analog converters have a resolution of 10 bits and their output is shared by all analogic channels. The chip can also deliver one trigger signal at a time through the built-in digital multiplexer. Beside the DACs and Wilkinson ADC, the digital part includes two OR gates used to perform logic operations upon the trigger signals delivered by discriminators. The MAROC3 has its own voltage reference named Vbandgap designed to be stable with variations of the temperature and the power supply voltage [330, 332, 334].

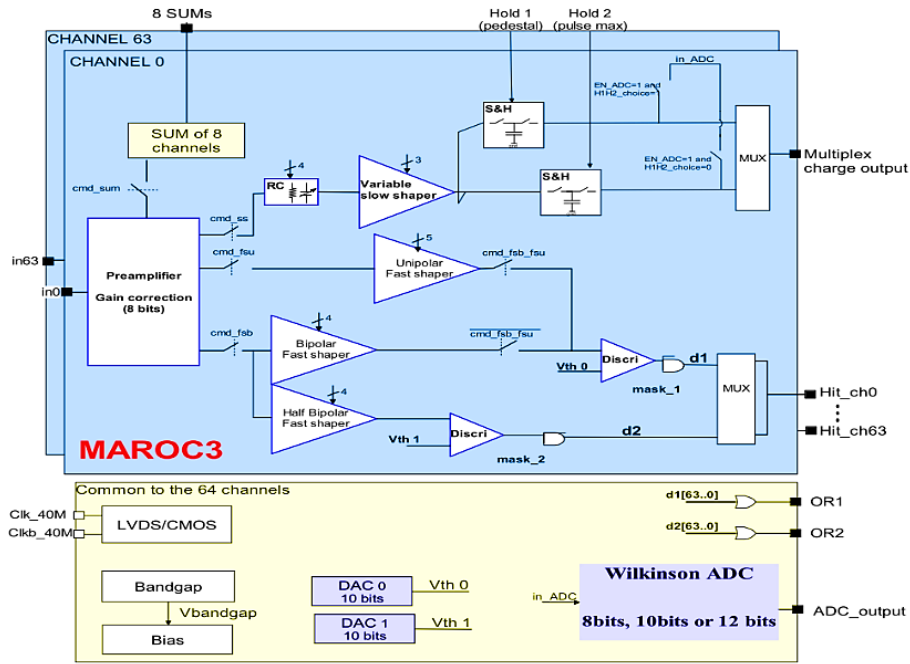


Figure 3-1 Layout of MAROC3 front-end ASIC architecture [331].

In absence of radiation, the characterization of the MAROC3 operational parameters has been performed by the chip design team. Presented in figure 3-2, there are two of the test boards available for this ASIC. The board with the socket was designed for MAROC2, but it was adapted for MAROC3, since both chips are almost pin to pin compatible. A dedicated version of board was designed and implemented also for MAROC3. Two versions of packaging are available for MAROC3, with one of them a ceramic package which has the upper lid removable such that the ASIC die can be exposed directly to beam.

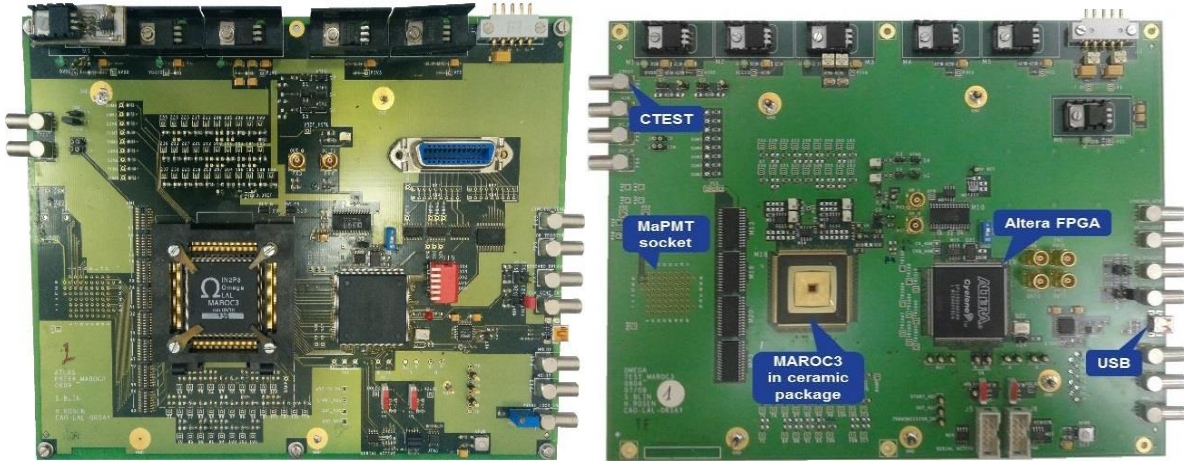


Figure 3-2 The MAROC3 prototype boards developed at CNRS-IN2P3-Ecole Polytechnique.

Depending on a single photo-electron counting or high input charge operation mode, the MAROC3 is configured from a LabVIEW Graphical User Interface (GUI) running on a PC, shown in figure 3-3 [335]. The configuration commands are sent from the PC over USB interface to the Altera FPGA which sets the MAROC3 running mode according with the instructions defined in GUI. Also, at users choice each input of the 64 preamplifiers can be

enabled or disabled through GUI, plus other ASIC predefined tests and measurements can be started.

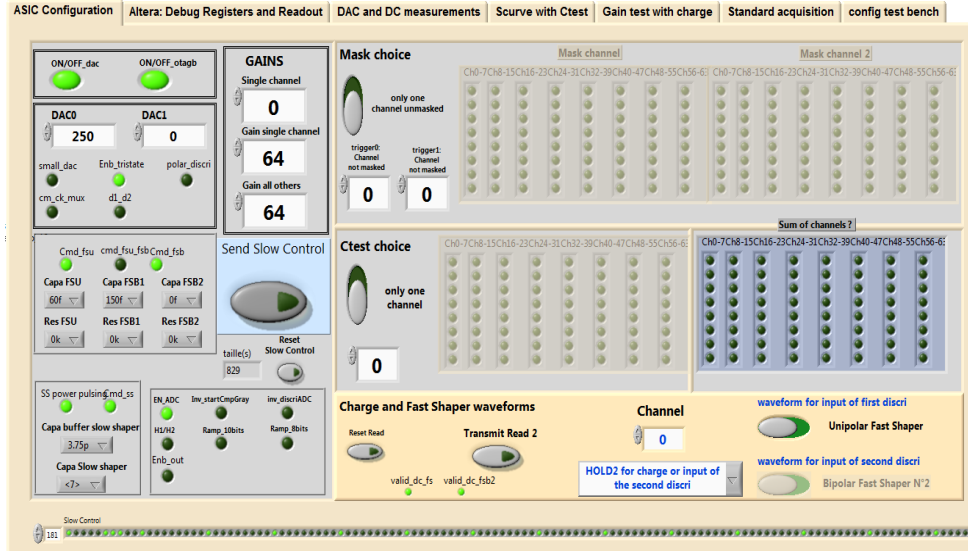


Figure 3-3 The LabVIEW graphical user interface implemented for MAROC3 board developed by the ASIC design team [331]

On the test board there is a LEMO connector, named C_{TEST} , associated to a chip pin with the same name. Internally MAROC3 has a 2 pF capacitor with one plate connected to the C_{TEST} pin and the second available for connection to each input of the 64 preamplifiers. This feature enables ASIC testing without explicitly attaching a MaPMT to its input channels. Hence, to test the board no light-tight enclosure is needed. Therefore, the signals from the MaPMT anodes are emulated with the help of a pulse generator. Pulses with fall time below 5 ns are injected to MAROC3 internal 2 pF capacitor. The Scurve test is carried out by adjusting the DACs threshold such that 100% trigger efficiency is ensured when at the input of the preamplifiers is applied a pulse similar to the one produce by a MaPMT anode when single photoelectron strike a pixel at 150 fC output. The setup used in the laboratory for the Scurve measurement is presented in figure 3-4, while in figure 3-5 is sketched the one for charge measurement.

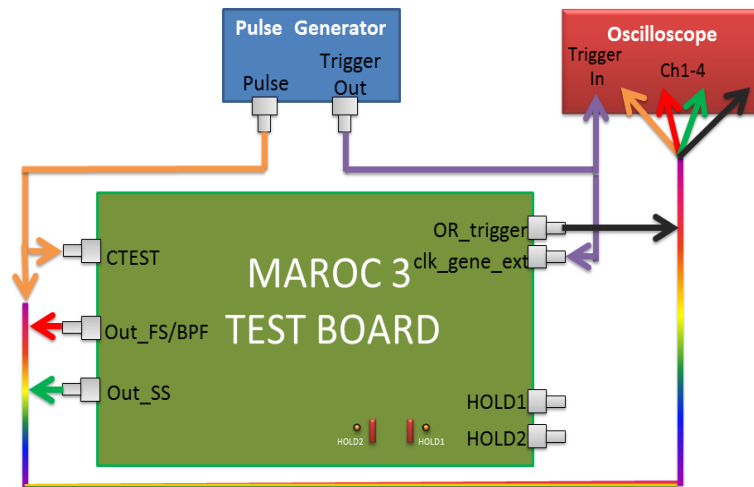


Figure 3-4 Experimental arrangement for Scurve measurements.

The Scurve measurement is made by injecting pulses with 5 ns fall time from the signal generator into the C_{TEST} LEMO connector, while the pulse generator trigger signal output is applied to synchronise the oscilloscope trigger with a counter inside an ATERA FPGA over clk_gen_ext LEMO connector. A burst of 100 pulses are injected into the chip through the C_{TEST} pin for each of the 1024 thresholds voltage values generated by DAC (10 bits). The discriminator output pulses are incremented by the counter inside the FPGA and the algorithm programmed in it calculates the efficiency for each DAC threshold. The Scurve measurement results are displayed on the GUI. For an input charge of 1 pC the waveform graph in figure 3-6 exemplify the signal response of both shaper outputs associated with the trigger signal. The efficiency curves for 150 fC input charge are plotted for all 64 channels in figure 3-7.

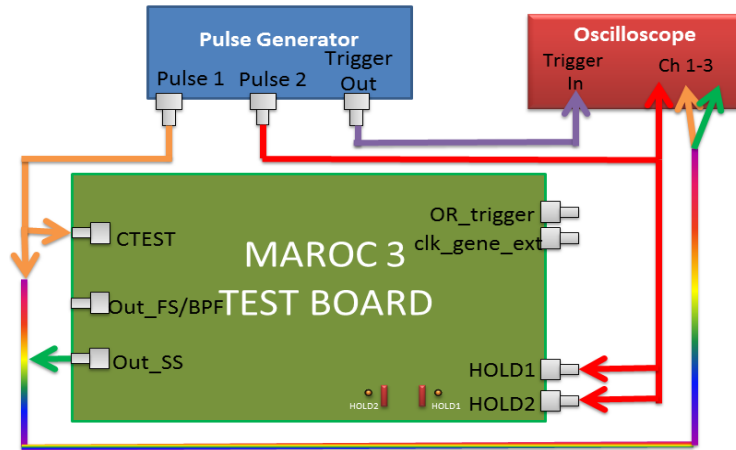


Figure 3-5 The setup for charge measurements.

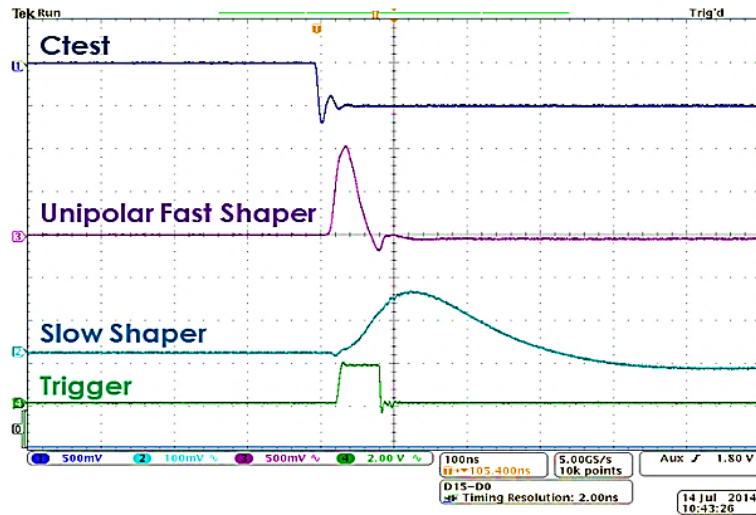


Figure 3-6 Slow Shaper/Fast Shaper and trigger signal for 1pC input charge.

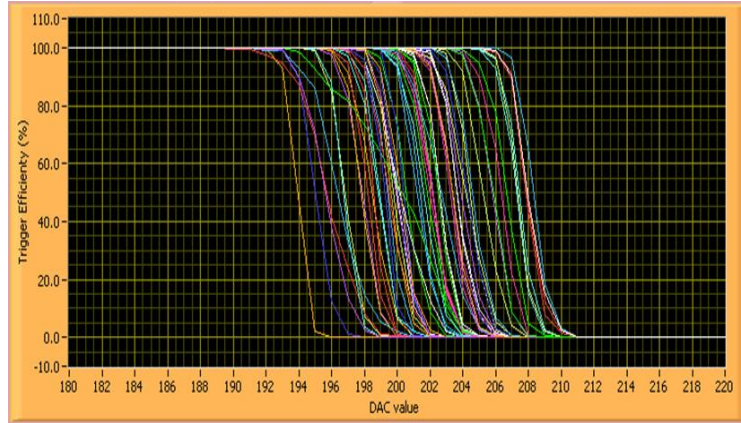


Figure 3-7 Trigger efficiency curves for 150 fC input charge.

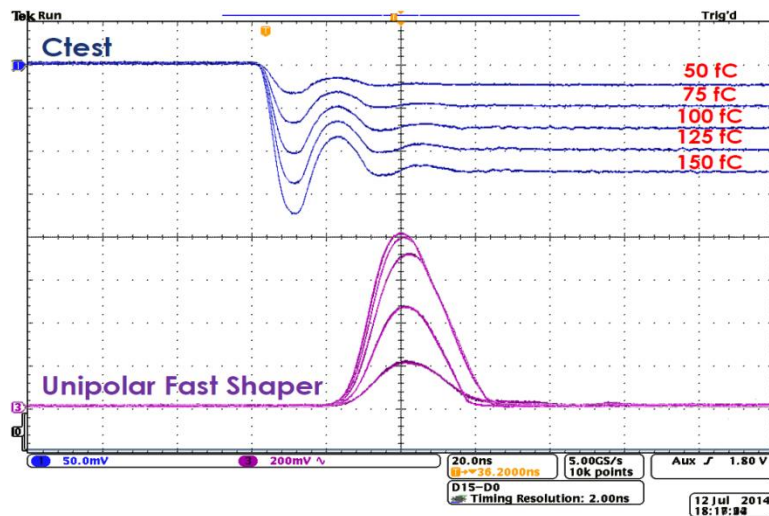


Figure 3-8 The Fast Shaper response for different input charge values.

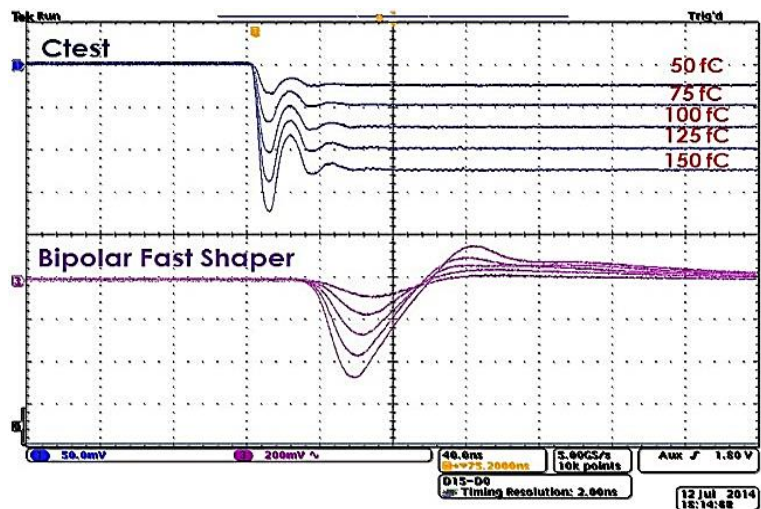


Figure 3-9 The Bipolar Fast Shaper response for different input charge values.

The signal response of the Fast Shaper at different input charge, see figure 3-8, it is faster compared to the response of the Bipolar Fast Shaper, which is dedicated to the sampling of the higher input charges, e.g. figure 3-9. Given the Fast Shaper response, the single photon

counting capability of the MAROC3 is optimal for a signal processing path which includes this shaper. Concerning the Scurves, the trigger efficiency of 100% is obtained for a 150 fC input charge when the DAC threshold voltage corresponds to a DAC register value below 190. Nevertheless, the Scurve change with the input charge, therefore the DAC register value has to be adjusted depending on an input charge value range of interest.

Using the setup diagram in figure 3-5, the charge measurement can be done by tuning the signals from pulse generator and those generated by the ASIC. This time the analog path of the Slow Shaper is used as feed to the Wilkinson ADC input. Again, the MaPMT output signals are emulated with the help of pulse generator, which also provides the signal required for both HOLD LEMO connectors. On the board, there are two switches named the HOLD1 and HOLD2 which must be turned on charge measurement mode. Tuning on is accomplished when the fall edge of HOLD signals is aligned with the Slow Shaper pulse peak, see image waveforms in figure 3-10.

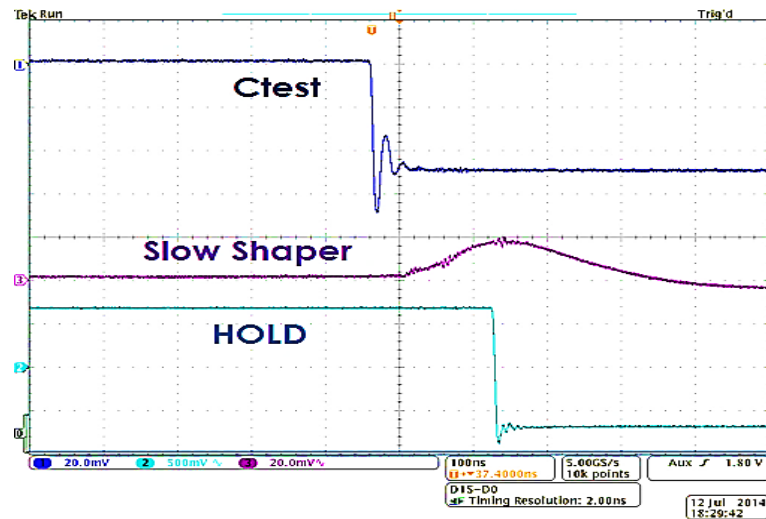


Figure 3-10 Signal tuning for charge measuring.

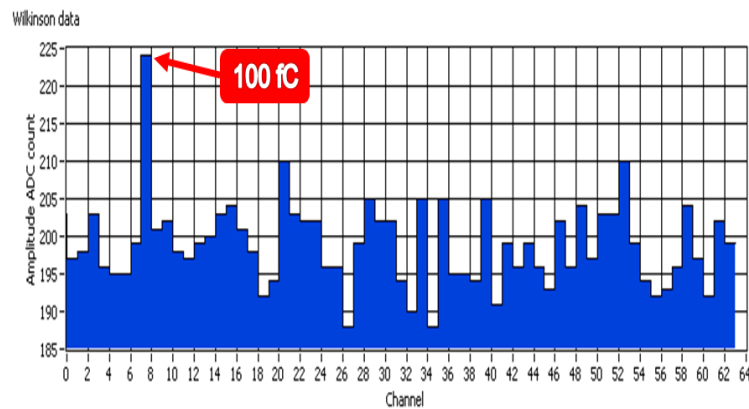


Figure 3-11 The result of charge measurement for channel 8.

The following results obtained in the laboratory were for an input charge of 100 fC injected in analog channel number 8 and the other channels were left without signal. The data displayed in the figure 3-11 highlights that the value of charge measured on channel 8 and it is significantly different compared to the noise background value of the MAROC3 built in Wilkinson ADC.

3.2 Test bench for the MAROC3 irradiation

Qualifying an integrated circuit as radiation hard demands a well-defined testing strategy focused on recording its activity in: normal running condition, under irradiation and post irradiation. All data collected are further analysed to spot any radiation effect that might occur in the device. In preparation for the MAROC3 radiation hardness qualification procedure the parameter nominated to be monitored were established jointly by the LHCB Romanian Group with the ASIC design team. The adopted procedures entail to monitor the MAROC3 parameters listed in table 3-1. After each irradiation dose, the parameters are checked again. There is one list of parameters to be monitored before and after each deposited radiation dose, and a second one that should be recorded online during the dose deposition. Offline analysis of each recorded parameter might highlight signatures of radiation induced effects. By correlating the monitored parameters evolution in time, it is possible to distinguish various types of effects and to isolate the functional parts of the chip where they occur.

Table 3-1 List of monitored parameters for the MAROC3 radiation hardness study

before /after irradiation	during irradiation
• DACs linearity and residuals	▪ Threshold voltage
• S curves for all channels	▪ Chip power consumption
• Chip power consumption	▪ ASIC internal voltage reference (Vbandgap)
• ASIC internal voltage reference (Vbandgap)	▪ DC voltage component of Slow/Fast Shaper
• DC voltage component of Slow/Fast Shaper	▪ Chip and PCB Temperature
• Chip and PCB Temperature	

The power consumption variation, particularly the current, can indicate an accelerated ageing of the chip as a cause of TID or DD usually accompanied by an increase in leakage current. Other severe effects, like SEL and catastrophic ones like SEG or SEB produce a extremely steep current increase. Only by power cycling the chip can it be check if those effects are permanent or not. Any increase in chip temperature independently of the environmental temperature is another perceptible indication of the power consumption variation, as the power dissipation increases considerably for the induced SEL.

Among various electrical parameters on the chip, it is possible to check if specific built-in functional blocks have a good operation by monitoring: internal voltage reference (Vbandgap), and electrical parameters of DACs, shapers and discriminators. The TID or DD effect upon the Vbandgap output voltage and the DC voltage component of the Slow/Fast Shaper are evident in changes of their voltage amplitude. Drastic variation in their output might be consequence of SEE, like latchup or upsets. The DAC linearity test is performed to prove that this mixt-signal circuitry does not lose its monotonicity, or that the expected voltage output from the same register value does not vary from dose to dose because of TID and DD. If a change in the threshold voltage appears then a SEE has occurred in the DAC analog part. The threshold voltage might likely have step transition and this can have as cause a SEU or MBU within the DACs registers, therefore the threshold voltage step

increase/decrease takes place and DAC output voltage is modified in accordance with the DAC register containing the upset bits.

Performed before the irradiation and after each deposited dose, the Scurve test allows asserting any modification on the trigger efficiency by maintaining the same input charge for all chip channels, usually the one corresponding to one photo-electron. A shift in the curve position indicates a change in the trigger efficiency as result of TID or DD in analog channels, or in DAC. Even some of the 64 curves might disappear and this points out a clear damage of those channels paths or to a SEU in registers. The Scurve variation with the dose is useful for chip calibration in Upgrade phase.

3.2.1 Hardware part of the test bench

The ASIC parameters variation offers indispensable information on its operation in the presence of radiation. Monitoring the parameters and gathering data during irradiation tests it is made by taking into account that the data acquisition (DAQ) system and other electronic equipment must be far away from the device under test (DUT), i.e. MAROC3 chip. Usually, the irradiation test with heavy ions beam is done in vacuum enclosure foreseen with vacuum-pass-through connectors. Therefore, all the wires connected to the DUT board are split in two and equipped with connectors matching the ones mounted on the vacuum vessel. Moreover, for irradiation tests with the beam extracted in air as in case of the protons or the neutron, all test bench electronics are placed in the experimental room as far as possible from the DUT board situated transversal the beam line. The users oversee and operate everything from the control room.

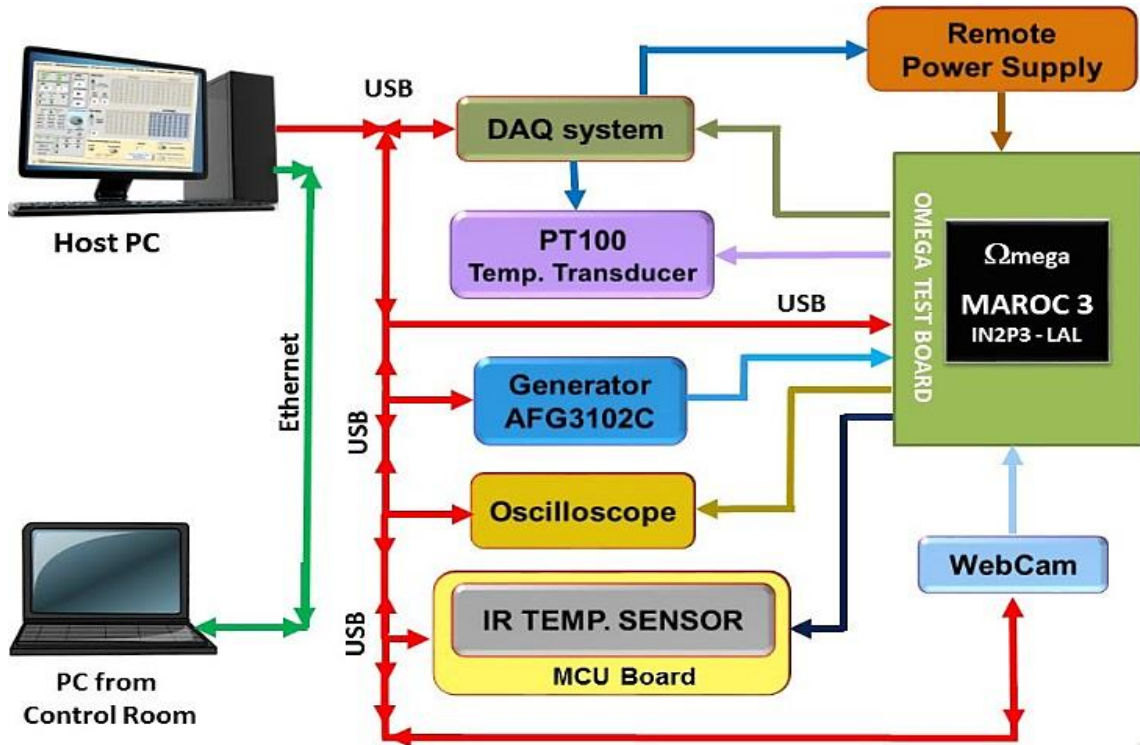


Figure 3-12 Test bench architecture for MAROC3 online monitoring.

I proposed and implemented an automatic test bench for the MAROC3 radiation hardness assessment appropriate for heavy ions, proton, neutron and X-ray irradiation testing,

but not for mixt-field typically of CHARM-like facility. The MAROC3 automatic test bench has the design layout presented in the figure 3-12. Each of the test bench equipment is connected to the host PC over USB interface. Further, the data are accessed by the user via Ethernet from the control room PC. The DUT board is powered through screened multicore cable a 5 m long from a remote-controlled power supply unit. This unit is custom-made and delivers ± 7 V and 2 A current on each of the rails. Other measurements performed with MAROC3 require a pulse generator and an oscilloscope as for Scurves test. The MaPMT signals are emulated with the help of an AFG3102 generator, which maintains a constant input charge for all 64 analog channels of the DUT. The signals are checked with the oscilloscope.

Shown in figure 3-13, our group designed and implemented the DAQ system considering the following requirements: noise suppression due to long data transfer cables and DAQ sampling technique using a signal conditioning block; extended number of analogue inputs and GPIO connections. The DAQ system features are: 24 analogue inputs of which 16 on 10-bit resolution and 8 on 12-bit resolution; 54 digital GPIO connectors; high-side current sense amplifiers; analogue voltage buffers and anti-aliasing filters. The processing unit of the DAQ system is built around a commercial Arduino Mega development board [336]. The 8 analogue inputs with 12-bit resolution are read through an external MAX1270 ADC [337] connected to the processing unit via a SPI interface, see schematic on Appendix B. The 12-bit resolution analogue inputs are assigned to monitored signals of low amplitude that might have also small variations during irradiation. Four inputs of the external ADC are dedicated to the high-side current sense amplifiers from MAX4377 series [338]. Requirement is that any small increase in current consumption be detected, as it could be a precursor of a high current consumption state, which would be caused by leakage current or SEL. Presented in Appendix B, the signal conditioning block has the voltage buffers implemented with an unity-gain stable operational amplifier MCP6424 followed by a network of RC anti-aliasing filters [339]. All analogue voltage inputs are connected to the signal conditioning block before signal gets to ADCs. Generally, the parameters less important for the DUT characterisation are sampled by the 10-bit built-in ADC of the processing unit. In this case the test board power supply monitoring is done with low resolution ADC.

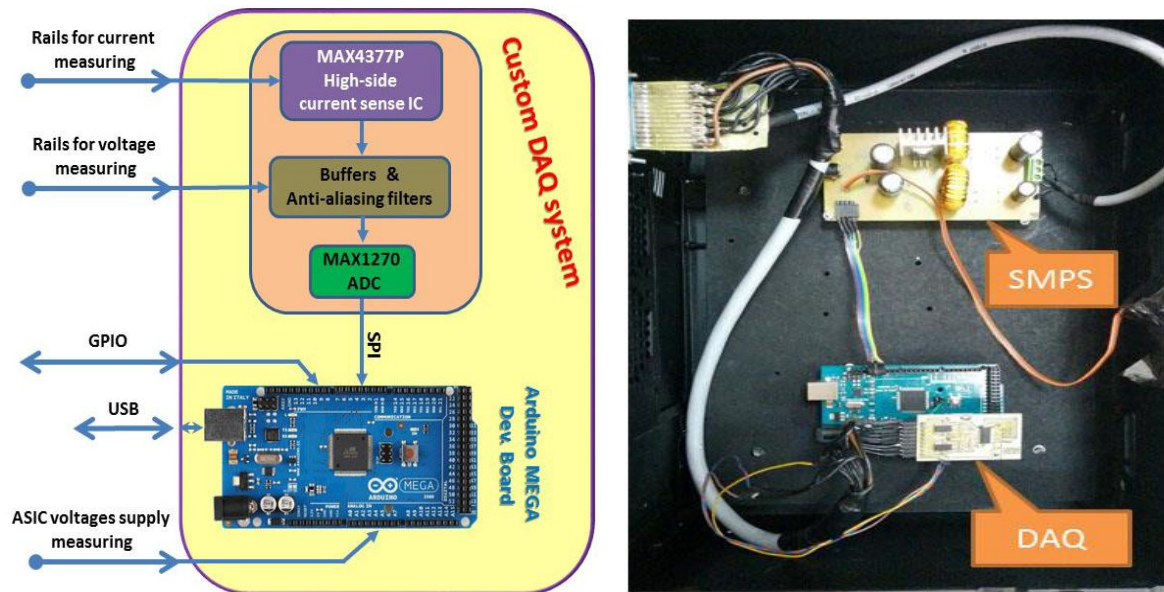


Figure 3-13 The data acquisition system architecture for ASIC irradiation (left side) and the monitoring unit housing DAQ plus SMPS (right side).

Further, I installed the SMPS along with the custom DAQ in a metallic black box which we call a monitoring unit, see right side of figure 3-13. All the input/output connections to the electronics inside the monitoring unit were accessible through a D-Sub connector with 25 pins fixed on the metallic box back side. The front side of the monitoring unit has a few status LEDs that indicate if the output voltage of SMPS is ON/OFF and if the DAQ system is on.

Over 5 m of screened multicore copper cable has been used to connect the DUT board with the DAQ system and the power supply. Another 5 m of USB cable is used for the data bus between the host PC and the monitoring unit. The complete setup was extensively tested in our laboratory. All three test boards were characterized before being irradiated and the values of the parameters recorded in laboratory were used as baseline for those measured during irradiation.

For the ASIC current consumption monitoring I implemented a small PCB which includes: the ASIC voltage regulator LM1086 and the current sense amplifier IC together with the shunt resistor R_1 , see left side of figure 3-14.

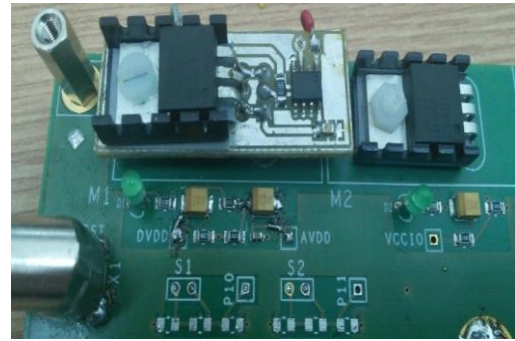
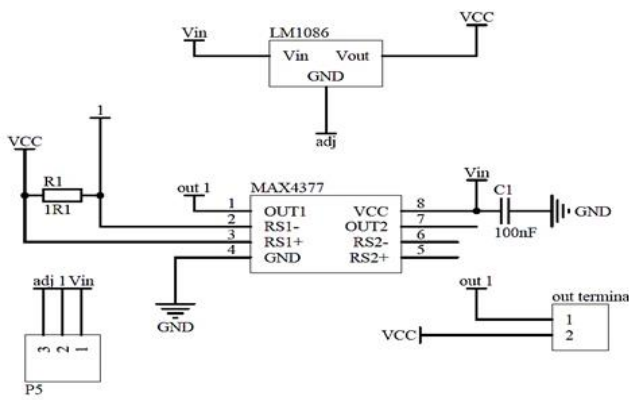


Figure 3-14 Schematic for the DUT current measurement (left side) and its PCB plugged in the MAROC3 test board (right side).

I have chosen the thermal monitoring of MAROC3 to be done with two types of sensors. First one is based on the PT100 transducer connected through an adapting circuit to the DAQ system and the second one is an infrared contactless sensor MLX90614 [340]. The contactless temperature sensor is readout over a I2C interface by a processing unit implemented with a ATMEGA328P microcontroller [341]. In figure 3-15 is presented the infrared contactless sensor along with the microcontroller processing unit, while the schematic is given in Appendix A.



Figure 3-15 The MLX90614 temperature sensor with ATMEGA328 processing unit.

The MLX90614 sensor plus the ATMEGA328 are powered from a USB port of the host PC. Again, 5 m of shielded cable was used to connect the temperature contactless sensor to the processing unit. A 3.3 V voltage regulator is soldered on the bottom side of sensor PCB. The MLX90614 sensor was enclosed in a 5 mm thick lead box with window, for shielding against the beam scattering or radiation background. The temperature values are sent by the microcontroller to the host PC over an UART to USB converter. This sensor was foreseen in the test bench mainly to measure the MAROC3 dice temperature, while the PT100 is attached to the test board PCB bottom layer right under the chip.

3.2.2 Software part of the test bench

The test bench hardware architecture is controlled and monitored by a software component consisting of a graphical user interface (GUI) developed by our group in LabVIEW and the ATmega328 software. At each 50 ms the electrical parameters and temperature values are sampled. A fast acquisition is essential for increasing the probability of observing rare events like SET or preventing possible permanent damage induced by SEL or SEU long term action. Further, the data is sent over USB to the host PC where it is stored in ASCII files and displayed by two GUI windows.

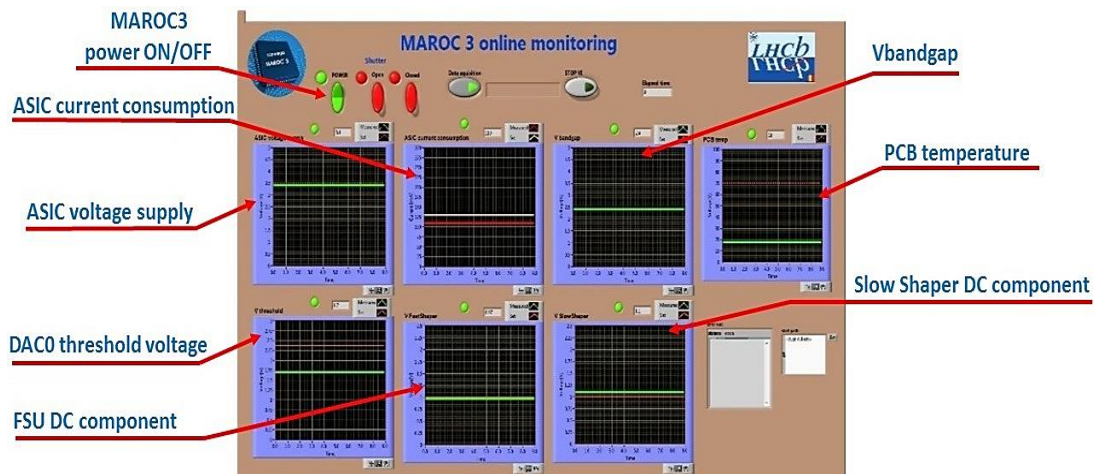


Figure 3-16 The graphical user interface associated to the DAQ system.

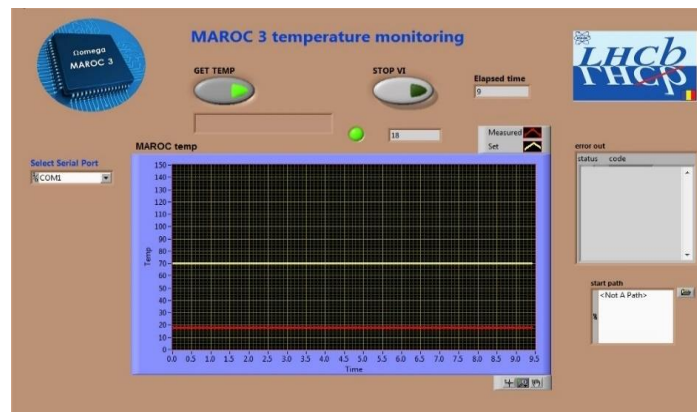


Figure 3-17 The GUI for contactless temperature sensor.

The first GUI is dedicated to the DAQ system which is presented in 3-16. Through this interface the user turn ON/OFF the power supply for the DUT and visualises the evolution in time for each monitored parameter. Moreover, a power cut-off routine is implemented to be initiated whenever a recorded parameter exceeds the user-defined threshold. A warning message will pop-up in the GUI and the power supply is cut automatically.

Figure 3-17 presents the interface developed in LabVIEW for the infrared contactless sensor MLX90614. This one was implemented to record the MAROC3 dice temperature continuously even when the DUT board is powered-down. The values are written in a separate ASCII file. Also, this second interface was foreseen to cut-off the power supply for the MAROC3 board, when the dice temperature exceeds 70 °C, though this threshold can also be modified by user. Both interfaces dump data in ASCII files and each data set recorded has a time stamp. All data gathered before, during and after irradiation procedure are essential for later analysis.

3.3. Irradiation test with 35 MeV proton beam

The MAROC3 radiation tolerance was investigated at low to medium proton energy beam using Julich Isochronous Cyclotron (JULIC) facility based in the Nuclear Physics Institute of the Research Centre Julich, Germany. Extracted in air through a 2 mm thick aluminium (Al) exit window, the beam has energy of 35 MeV at DUT surface, while in vacuum the proton beam has the energy of 45 MeV and a maximum flux of 6×10^{13} protons/s [342, 343]. Regarding the dosimetry, inside the beam line faraday cups are used to measure the proton current and the integral beam current is measured behind the Al exit window with an ionisation chamber, therefore the fluency is measured within 5% uncertainty. For beam profiling and position in front of the exit window a scintillating beam profile monitor is placed [343].

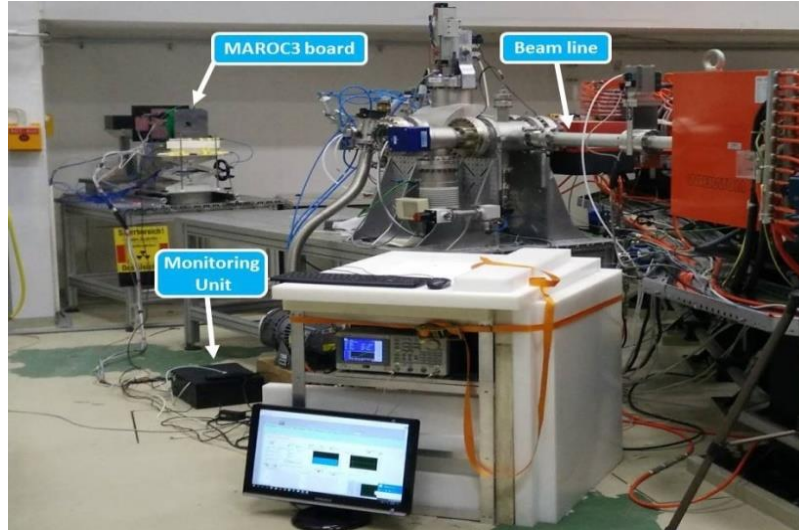


Figure 3-18 The MAROC3 test bench installed on JULIC beam line.

Mounted on a sample holder metallic support as in figure 3-18, the MAROC3 test board has in front a 5 mm lead mask to protect additional electronic device populating the PCB around the DUT. An aperture of $50 \times 50 \text{ mm}^2$ was left for exposing MAROC3 dice of 16 mm^2 ($4 \text{ mm} \times 4 \text{ mm}$) and almost all its package. The DUT dice alignment with the beam longitudinal axis was made using laser positioning system available on site. The monitoring

unit was placed 5 m away plus another 2 m for the other test bench equipment housed within a metallic frame surrounded by paraffin walls for radioprotection. From the control room everything was controlled and monitored via Ethernet. Subsequently three MAROC3 chips were irradiated in steps to determine when the device shows signs of malfunction or failure. In the table 3-2 is given the applied doses in Si and cumulated fluence for each tested device.

Table 3-2 Irradiation steps and cumulated fluence for MAROC3 testing at JULIC facility

Sample no.	Doses (krad)		Dose rate (rad/s)	Cumulated fluency (protons/cm ²)
1	dose 1	50	~ 26.5	9.226x10 ¹¹
	dose 2	50	~ 26.5	
	dose 3	100	~ 33.1	
2	dose 1	50	~ 35.5	9.226x10 ¹¹
	dose 2	50	~ 35.5	
	dose 3	100	~ 30.9	
3	dose 1	200	~ 172.8	1.845x10 ¹²
	dose 2	200	~ 169.6	

Two DUT sample have been irradiated up to 200 krad (Si) with 9.226x10¹¹ protons/cm² cumulated fluence. The third sample was exposed to 400 krad (Si) and cumulated fluence of 1.845x10¹² protons/cm², while the dose rate was increased to around 170 rad/s. From the LHCb radiation environment standpoint, 200 krad (Si) corresponds to 5 years of device running (50 fb⁻¹) including a safety factor of 2 for TID.

3.3.1 Data analysis and interpretation

Prior to the proton irradiation all three MAROC3 chips were characterised extensively in the laboratory and the electrical parameters recorded were kept as baseline. After test bench installation on JULIC beam line, each chip was again checked for several tens of seconds to record its parameters immediately before irradiation. The irradiation was initiated once the DUT board parameters have been cross-checked with the baseline values. After each deposited dose it was done a complete set of measurements is performed in compliance with the list of parameters listed in the table 3-1. The data analysis was done considering also the annealing process which was recorded without delay once the beam was stopped. In the following it will be presented the parameter variations in the presence of radiation for all three MAROC3 samples tested.

During irradiation with a cumulated dose of 200 krad (Si) it was observed an increase of the test board power consumption, seen in figure 3-19, when the TID exceeded 50 krad on the first MAROC3 sample irradiated. This rise is due to the increasing of power consumption on DUT analog rail presented in figure 3-20 as well as in digital rail shown in graph 3-21. Therefore, the leakage current rise within MAROC3 circuitry is correlated with TID value. At the beginning of each irradiation run the DUT was power cycled and configured, fact highlighted by the overlap in time between current spikes and supply voltages drops in the plots below.

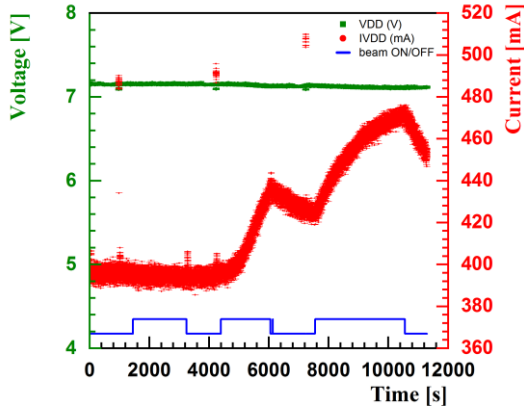


Figure 3-19 Sample 1 test board power consumption.

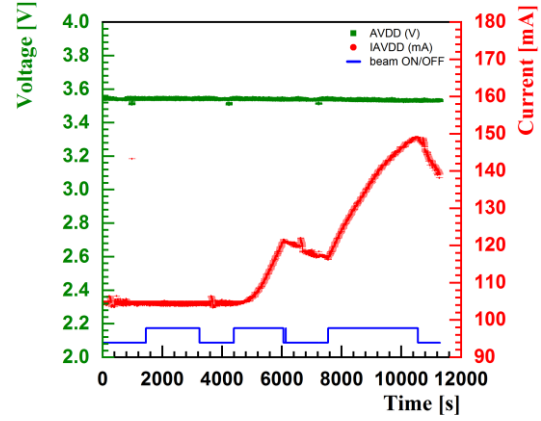


Figure 3-20 Sample 1 power consumption on analog rail.

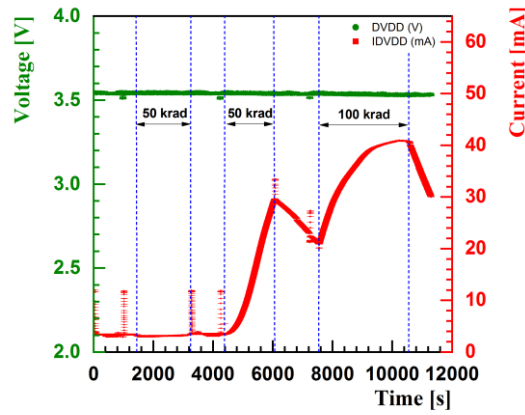


Figure 3-21 Sample 1 power consumption on digital rail.

After 100 krad (Si) the analog current has grown with 15.8% comparing the baseline value of 104.779 ± 0.055 mA, while on digital rail the variation was extreme at 765% considering 3.414 ± 0.055 mA in normal running condition. Also, a strong annealing was observed at the room temperature and the analog current decreased with 5 mA within around 24 minutes. In the same time span, for the digital current the annealing process led to a decrease with almost 8 mA. In the third irradiation run, after dose deposition of 200 krad (Si), on analog rail the current consumption rise against baseline was found to be 42.3% higher. On the digital rail the current consumption difference, when comparing with the normal running, was 37.26 mA. Thus, in extreme radiation condition with very high TID rates the MAROC3 analog and digital components are prone to TID effects given rise to high leakage current levels that are rapidly annealed by the annealing processes at room temperature.

Other parameters monitored during irradiation did not show notable variation with TID, these are internal voltage reference V_{bg} presented in figure 3-22, Fast Shaper DC component V_{FS} shown in figure 3-23, Slow Shaper DC component V_{SS} presented in figure 3-24. Before beam ON interval at the beginning of run 3, it can be seen that there was a shift in amplitude with respect to the baseline for the parameters mentioned above. This has happened after the DUT was power cycled and configured at the start of last irradiation run. After we perform some tests and reconfigure several times the device registers, these parameters returned to their baseline values and the beam was started. Possible cause of this behaviour might be a mismatch between Slow Control commands and chip configuration registers as result of 100 krad (Si) TID cumulated on the exposed device, which was solved most probably by the fast

annealing confirmed in other runs above 400 krad limit. These runs were not included in the analysis at this time,

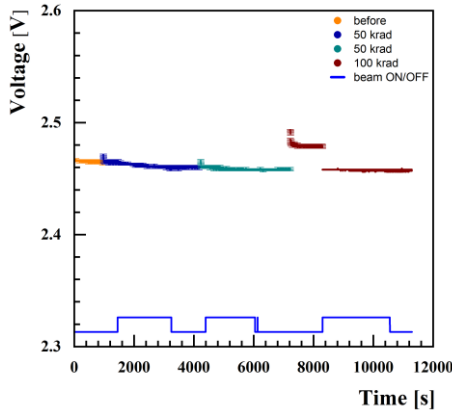


Figure 3-22 Sample 1 internal voltage reference V_{BG} .

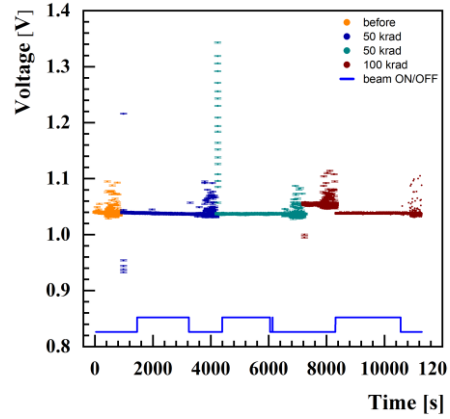


Figure 3-23 Sample 1 Fast Shaper DC component V_{FS} .

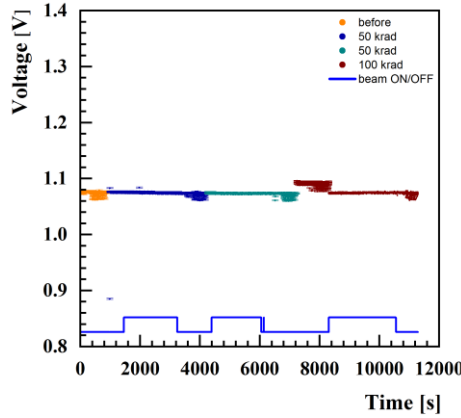


Figure 3-24 Sample 1 Slow Shaper DC component V_{SS} .

A closer introspection was carried on for the chip built-in DACs by monitoring their output voltages with ± 0.001 V precision. During irradiation no variation in voltage values was observed for both DAC. Linearity test was done after each dose and no relevant changes were observed to affect the DUT built-in DACs performance. Figure 3-25 presents the linearity curves for DAC0 as well as the residuals which are shown in figure 3-26 as difference between expected values and the measured output voltages. By fitting each linearity curve and comparing the results, it was found only a 1.38% variation within DAC0 linearity curve slope after 200 krad (Si). In case of DAC1 linearity curves presented in figure 2-27 it can be seen a plateau in the output voltage below configuration registers value of 500. This impairment was found to be an external feedback resistor used to adjust DAC1 range, and it is independent of radiation effects. Figure 2-28 with the residuals curves also outline the DAC1 linearity. For the curves slope value no variation were seen within working range of 500 to 1024.

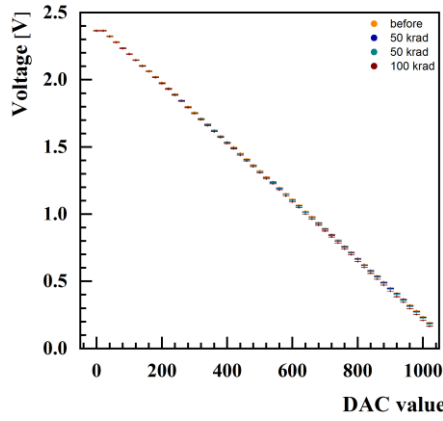


Figure 3-25 Sample 1 DAC0 linearity curves.

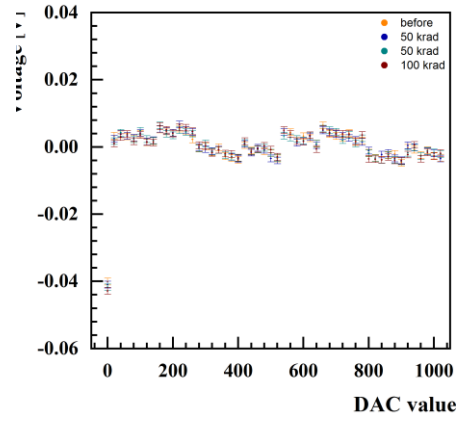


Figure 3-26 Sample 1 DAC0 residuals curves.

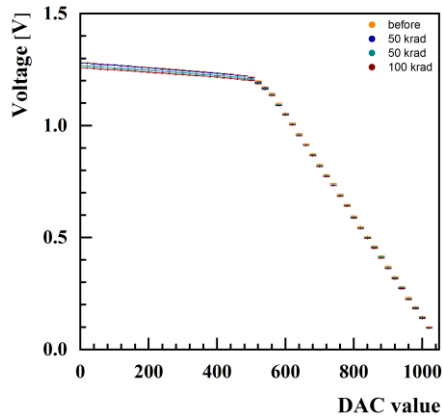


Figure 3-27 Sample 1 DAC1 linearity curves.

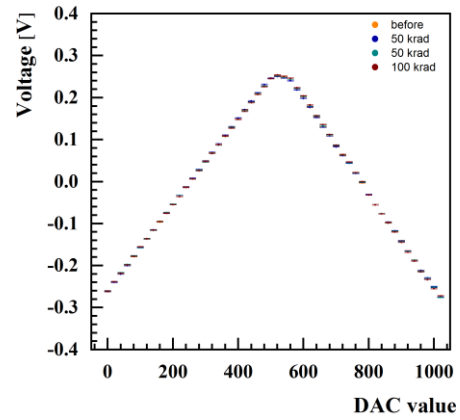


Figure 3-28 Sample 2 DAC1 residuals curves.

Second sample of MAROC3 chip was also irradiated to 200 krad (Si) TID maintaining almost constant dose rate for each run as in table 3-2, but the data taking was continued 8.55 hours after the beam was OFF. Figure 3-29 show the evolution of test board power consumption during DUT radiation hardness evaluation whereas the current rise is caused by the analog and digital current consumption increase. At the end of third dose when 200 krad (Si) accumulated on device, the analog current consumption grew with 36.7% from baseline value of 116.09333 ± 0.055 mA, see figure 3-30. Through annealing, the analog current consumption returned to the baseline value in 3 hours at the experimental room temperature around 20°C . A strong variation of the digital rail current consumption was recorded. Figure 2-31 highlights an increase by 187.5% compared to the baseline of 11.72 ± 0.055 mA for a cumulated dose of 200 krad (Si). In the digital part the annealing took place too, and the current came back to the baseline value after 3 hours.

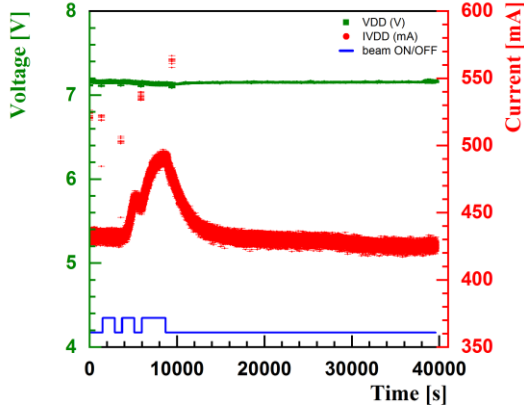


Figure 3-29 Sample 2 test board power consumption.

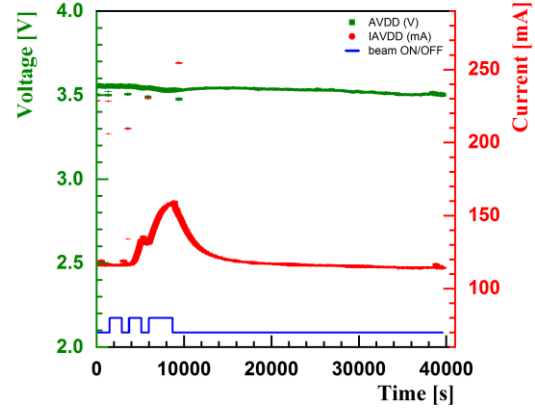


Figure 3-30 Sample 2 power consumption on analog rail.

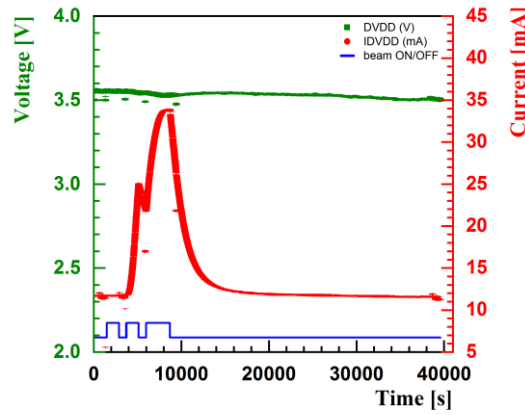


Figure 3-31 Sample 2 power consumption on digital rail.

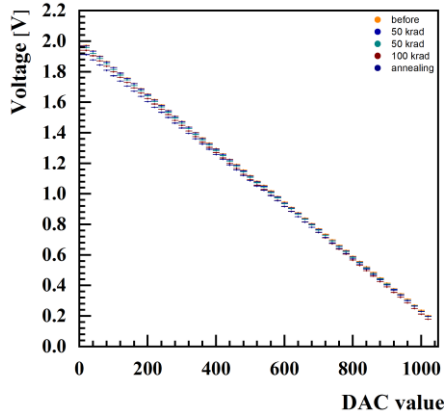


Figure 3-32 Sample 2 DAC0 linearity curves.

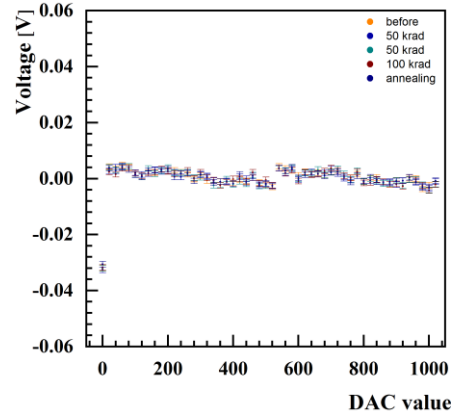


Figure 3-33 Sample 2 DAC0 residuals curves.

As in the previously tested sample, the embedded DACs performances under irradiation have been investigated after each deposited dose and after annealing period. In figure 3-32 are given the linearity curves for DAC0 and the plot with the corresponding residuals curves is given in figure 3-33. Analyzing the recorded data no relevant variations were found in the linearity curves slope. Also, DAC1 which has the linearity curves presented in figure 3-34 and

the residual curves in figure 3-25, it was proven to have a reliable operation up to a TID of 200 krad (Si).

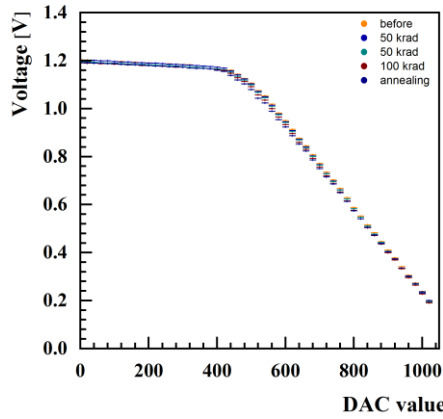


Figure 3-34 Sample 2 DAC1 linearity curves.

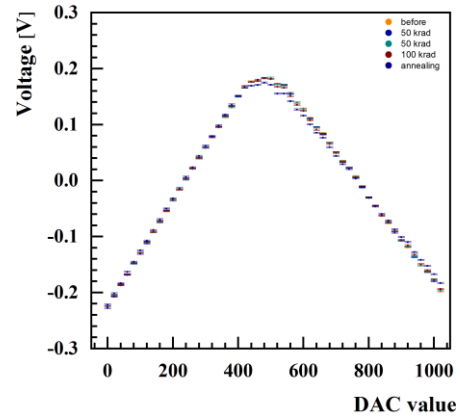


Figure 3-35 Sample 2 DAC2 residuals curves.

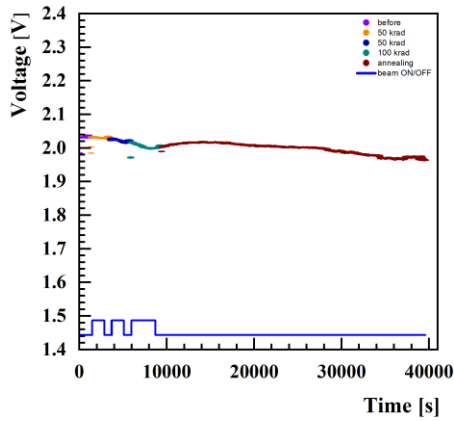


Figure 3-36 Sample 2 internal voltage reference V_{BG} .

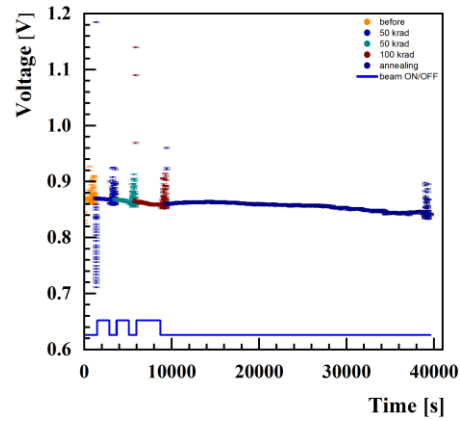


Figure 3-37 Sample 2 Fast Shaper DC component V_{FS} .

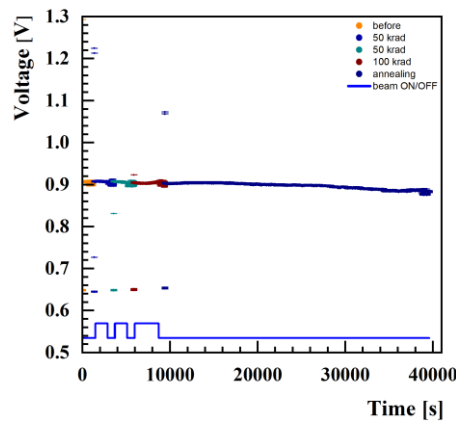


Figure 3-38 Sample 2 Slow Shaper DC component V_{SS} .

There were no significant changes with TID, but rather a modification with experimental room diurnal temperature changes. This is true for the parameters listed in the

following sequence: internal voltage reference V_{bg} presented in figure 3-36, Fast Shaper DC component V_{FS} shown in figure 3-37, Slow Shaper DC component V_{SS} presented in figure 3-38.

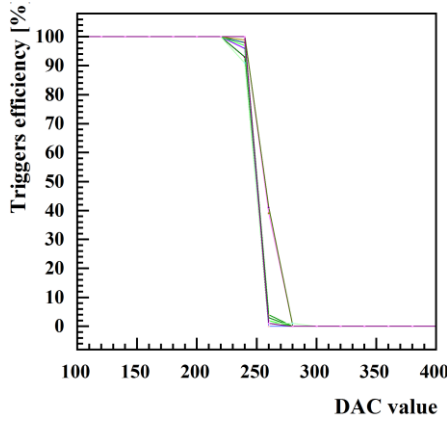


Figure 3-39 Sample 2 trigger efficiency curves before irradiation.

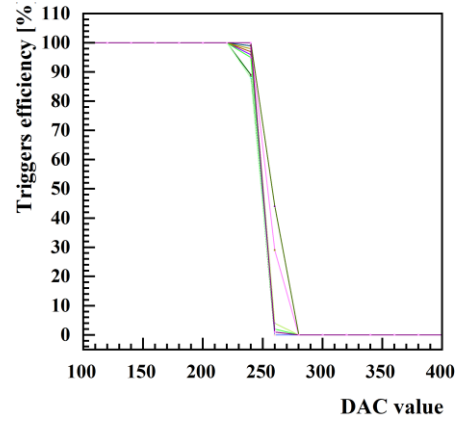


Figure 3-40 Sample 2 trigger efficiency curves after 50 krad (Si).

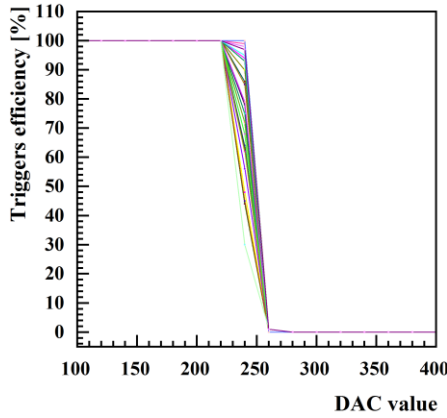


Figure 3-41 Sample 2 trigger efficiency curves after 100 krad (Si).

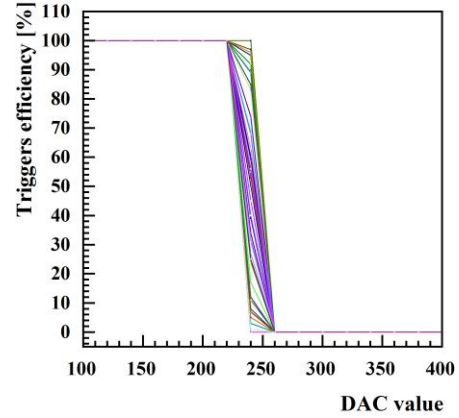


Figure 3-42 Sample 2 trigger efficiency curves after 200 krad (Si).

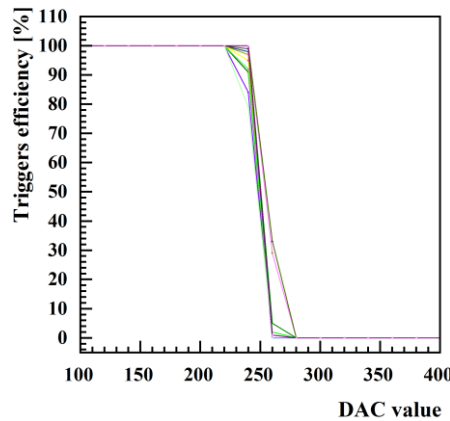


Figure 3-43 Sample 2 trigger efficiency curves annealing process

Trigger efficiency curve for each of the 64 chip input channels were also checked after each dose. The MaPMT signal was emulated with the pulse generator included in the test

bench architecture. Pulses with 5 ns rising edge were injected within 2 pF capacitor embedded in MAROC3 dice, therefore all 64 channels will have on the input a 50 fC charge. To perform this test the analog part of the chip works in conjunction with DAC0. For each efficiency curve of the trigger channels the DAC0 output is changed from 0 to the maximum. Figures 3-39 to 3-43 lay out the TID influence on the trigger efficiency curves. With the dose increase, the efficiency curves start to spread and slightly shift after 200 krad (Si) as in figure 3-42. This modification for the chip operation could be due DAC0 linearity slope insignificant variation with temperature plus TID charge deposition within analog circuitry of the MAROC3. After annealing, the triggers efficiency curves recovered, see figure 3-43, and overlap as before irradiation figure 3-39.

A different approach was used to study the radiation hardness for the third sample by an increased dose rate to around 170 rad/s, and with 400 krad (Si) dose cumulated within 2 runs. Considering MAROC3's resilience to 200 krad (Si), decision was made to apply this dose in a single run, further we continue the irradiation with a second dose of 200 krad (Si). Presented in figure 3-44, the board power consumption is influenced by the irradiated chip current consumption, as in case of the former two tested samples.

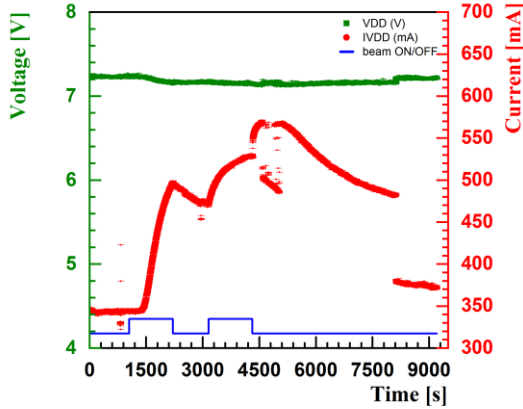


Figure 3-44 Sample 3 test board power consumption.

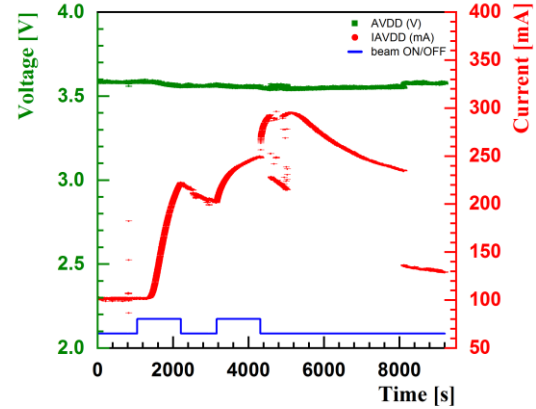


Figure 3-45 Sample 3 power consumption on analog rail.

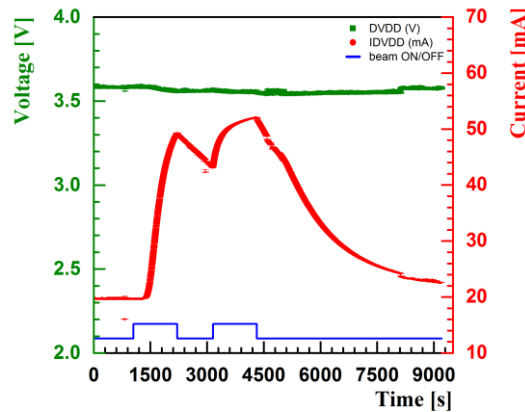


Figure 3-46 Sample 3 power consumption on digital rail.

First irradiation run of 200 krad (Si) had led to the rise in the chip analog rail current of 118.4% considering the baseline of 101.74 ± 0.055 mA, while for the second run the rise was 145.5%. Between the two consecutive runs it was an annealing time of 16 minutes and within

this period of time linearity and trigger efficiency tests were done, followed by reconfiguration. At the end of second run the analog current increased to peak value of 189.9% right after the beam was turned OFF. The linearity plus triggers efficiency test were launched but failed running. The DUT reconfiguration was tried but its functionality was frozen in unknown state. After 49.7 minutes, it was possible to resume the chip parameters test sequence done at the end of each run. The current consumption on the digital supply rail increased with 150.2% after the first run, while in the second run increased 163.6% considering the baseline of 19.7 ± 0.055 mA. For the third MAROC3 test board the baseline for the current consumption on digital rail is slightly higher comparing with other two because this board was adapted from MAROC2 to MAROC3, so the third sample evaluated does not have some electrical parameters as the prior two chips.

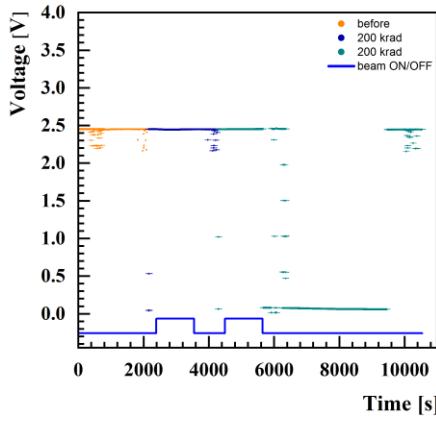


Figure 3-47 Sample 3 internal voltage reference V_{BG} .

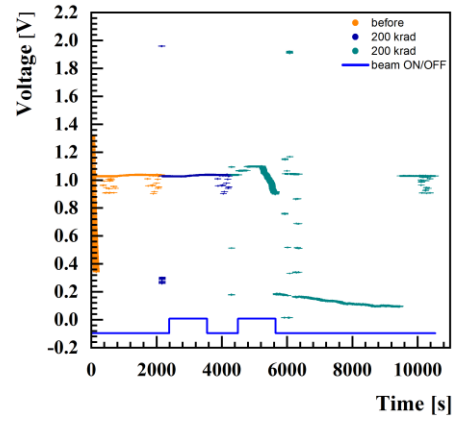


Figure 3-48 Sample 3 Fast Shaper DC component V_{FS} .

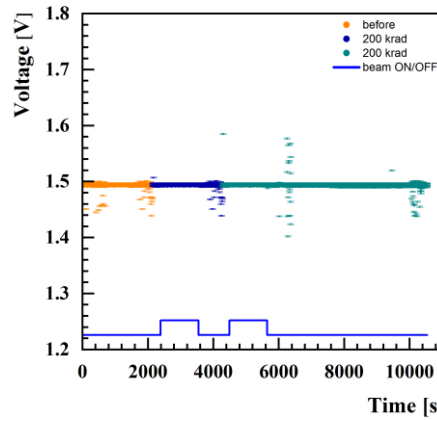


Figure 3-49 Sample 3 Slow Shaper DC component V_{SS} .

During 400 krad (Si) irradiation other parameters did not show notable variations, such as: internal voltage reference V_{bg} presented in figure 3-47, Fast Shaper DC component V_{FS} shown in figure 3-48, Slow Shaper DC component V_{SS} presented in figure 3-49. However the V_{BG} and V_{FS} parameters amplitude have fallen drastically after 400 krad (Si) within the time interval which overlaps the analog current consumption variation, see figure 3-45. Here the chip did not responded to configuration commands and its functionality was frozen until it was possible to reconfigure the chip, i.e. 49.7 minutes later. Through annealing and reconfiguration commands it was possible to recover MAROC3 functionality as the parameters in plots highlight.

Because the third test board was accommodated from MAROC2 chip version to MAROC3, both DACs ranges differ from previous ones. In normal condition the output voltage remains at the same value when DAC0 (DAC1) register value exceeds 920 (940) figure 3-50, (3-52). At the end of 1st run the DACs linearity was checked and analysis results indicate that there was only less than 1.5% modification in the linearity curves slope for both DACs relative to the baseline linearity curves. After 400 krad the linearity curve for DAC0 was stuck to a fix value. In case of DAC1 the registers incrementing from 0 to 1023 led to output voltage swinging between two fix values. The linearity test failed to run, as residuals plots show in figure 3-51 and 3-53. The linearity test was accomplished again once the chip reconfiguration was possible at 49.7 minutes after end of run 2. Slope modification was found to be 3.75% for DAC0 and 2.9% for DAC1 according to the baseline linearity curve. Also, the experimental room temperature changes and chip power dissipation might contribute to these changes in slope values.

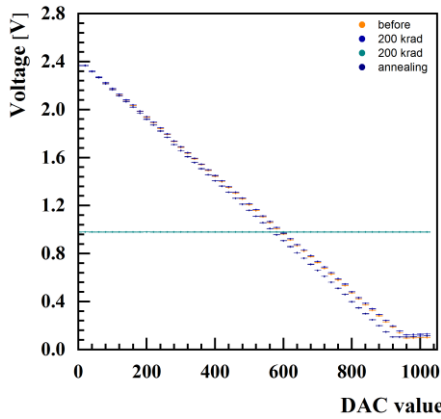


Figure 3-50 Sample 3 DAC0 linearity curves.

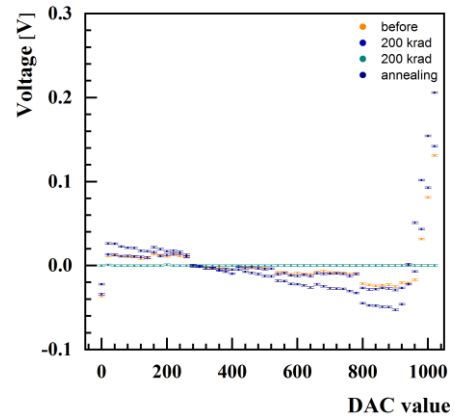


Figure 3-51 Sample 3 DAC0 residuals curves.

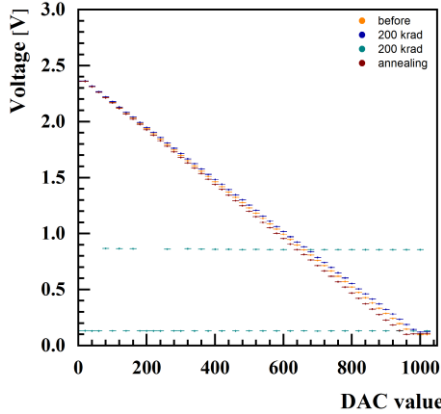


Figure 3-52 Sample 3 DAC1 linearity curves.

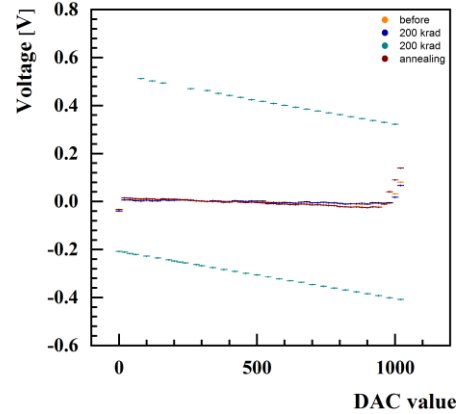


Figure 3-53 Sample 3 DAC1 residuals curves.

As it can be observed from all 3 samples, no sudden changes within the MAROC3 monitored parameters occurred during the beam was ON, therefore no clear sign of SEEs or especially SEL can be seen in the current consumption trend. The ASIC embedded DACs proved to be stable even to TID of 200 krad (Si). The S-curve graphs (trigger efficiency curves from figure 3-39 to 3-43) were determined before and after each applied dose of radiation. A fix charge of 50 fC was applied to all 64 analog channels of the MAROC3. The

results highlight, from dose to dose, influence of TID on the Scurves. Even so, the chip behaved well within the range considering the high dose applied.

3.4 Conclusions

The Romanian LHCb group accomplished the first successful irradiation test of an MAROC3 chip by evaluating its radiation tolerance against the TID with 35 MeV proton beam in May 2017 at JULIC facility located in the Nuclear Physics Institute of the Research Centre Julich, Germany. Further irradiation tests with protons and, also, heavy ions are foreseen. This first test with protons is the starting point of the irradiation campaign planned for the MAROC3.

Overall, the MAROC3 proved to be stable during beam irradiation with TID of 200 krad (Si). Beyond this TID threshold the ASIC radiation resilience must be carefully studied, considering that Slow Control commands do not reconfigure and the chip registers which seems to be stuck. However, the strong annealing process at room temperature overcomes the TID. In detectors for high energy physics application such as accelerators or space, the dose rate is much smaller than in accelerated irradiation tests. The chip power consumption rise would be negligible since the annealing process prevents the leakage current occurrence.

Still, a dedicated thermal study must be carried out to better understand how the chip parameters changes with the temperature. It is needed not only for the environment with considerable temperature fluctuation, but especially to quantify the impact of increasing in power dissipation on the dice, which in turn might influence MAROC3 normal running by: changes in DACs linearity curves slope or degrading triggers efficiency performance.

MAROC3 vulnerability to various SEE must be carefully checked. It is mandatory for the chip to be immune to SEL for heavy ions with LET below 15 MeV cm²/mg while the LET threshold is desirable to be as high as possible. Likewise, the chip tolerance to proton beams with energy above 100 MeV will be mandatory. Therefore, the possibility of permanent effects induced by protons and heavy ions must be investigated.

Close collaboration with the OmegaMICRO developer helped me to develop a viable monitoring strategy for the chip as well as a deeper understanding of its operation. In this context, I contribute to the proposal and implementation of the automated test bench for MAROC3 monitoring under irradiation. The test bench developed proved reliable over many hours of data taking. Other knowledge was passed to us by LHCb group involved in the testing of CLARO chip radiation tolerance. This chip also a MaPMT read-out ASIC.

CHAPTER 4

The Spatial Photomultiplier Array Counting and Integrating ReadOut Chip

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4. The Spatial Photomultiplier Array Counting and Integrating ReadOut Chip

The SPACIROC2 chip acronym stands for Spatial Photomultiplier Array Counting and Integrating Readout Chip. This is a front-end ASIC developed for the MaPMT read-out and its mainstream application is the Japanese Experiment Module (JEM) on the International Space Station (JEM-EUSO) space observatory. JEM is dedicated to the study of extremely high-energy cosmic rays [344, 345] using its wide-angle refractive telescope which operates in near ultra-violet wave-length region. More than 5000 MaPMT will be used in the telescope spherical-curved focal surface and the signal from each tube will be processed by SPACIROC2 [346-348]. Given the space environment unfriendly for electronics, the SPACIROC2 must undergo a radiation qualification procedure. I proposed and contribute to the implementation of an automatic test bench used for the ASIC radiation hardness qualification procedure, all this being possible with support from OmegaMICRO researchers. Throughout this chapter, a comprehensive view upon the work that has been done to evaluate the SPACIROC2 behaviour under radiation will be presented.

4.1 The SPACIROC2's architecture

Implemented within 0.35 μm SiGe BiCMOS technology at the Austria Micro System Company, the SPACIROC2 is a prototype ASIC with the following features: a low power consumption of 1mW per channel; 100% trigger efficiency for an input charge starting at 50 fC (1/3 photo-electron) with a 30 ns double pulse resolution; charge to time (Q-to-T) converter from 2 pC up to 400 pC; MaPMT gain spread correction with 64 channels input channels preamplifier that allows each individual channel gain adjustments on 8-bit resolution [349].

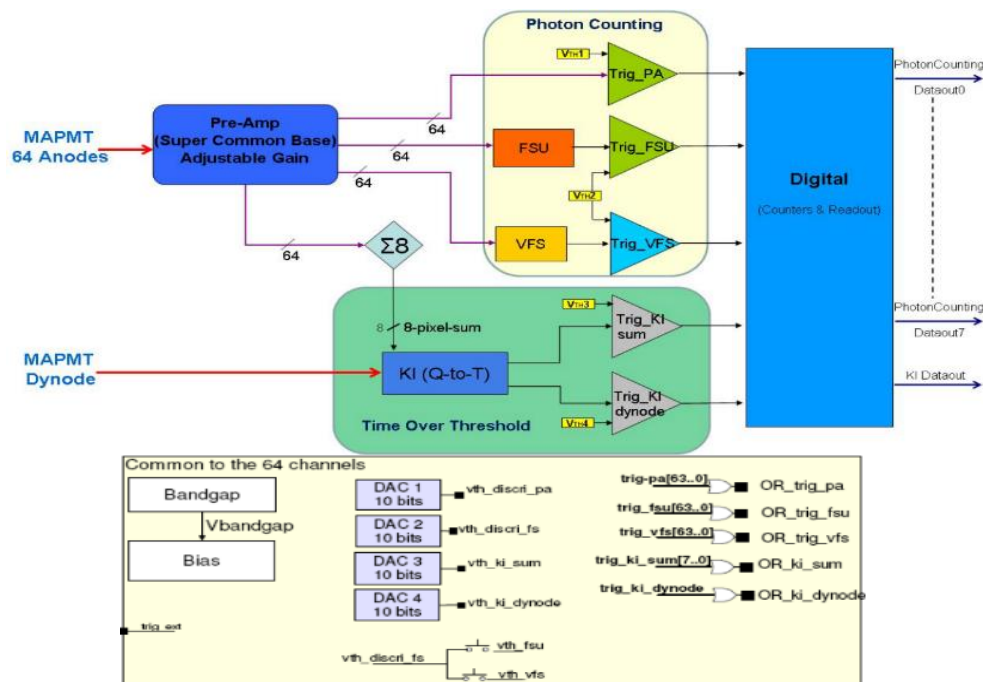


Figure 4-1 General architecture of SPACIROC2 chip [9].

Careful design was adopted to enhance the chip radiation tolerance, so that it can withstand cosmic ionizing particles flux [350, 351]. The general architecture of the SPACIROC2 is presented in figure 4-1 consisting of an analog and a digital part. The SPACIROC2 chip inherited from MAROC3 the Super Common Base Preamplifier with Adjustable Gain and the Unipolar Fast Shaper (FSU). The chip analog part embeds two blocks, one is named the Photon Counting, while the other is a Q-T Converter, and both are fed with signals from the adjustable gain preamplifier. In this version of SPACIROC, the 64 inputs Photon Counting block was implemented to have three discrimination paths for MaPMT signals in order to allow laboratory tests. The signal discrimination encompassing the Trig_PA comparator it is the simplest and low power path feed with signal directly from the preamplifier, so no shaper was use before. A 10-bit DAC (DAC1) is used to set the threshold for this discriminator. However, this solution is not efficient for input charges close to 1/3 photo-electrons. The other two signal discrimination paths benefit from shapers, while the threshold for the discriminators (Trig_FSU, Trig_VFS) is controlled by the DAC2. The single-photon counting capability of the SPACIROC2 is based on these discriminators supply with signals from the preamplifier through the pulse shapers. On each of the ASIC 64 channels, the outputs of Trig_PA, Trig_FSU and Trig_VFS discriminators are connected to 3 inputs AND gate. This makes possible to mask the trigger outputs further applied to a 4 to 1 multiplexer, the output of which goes at the digital counters [352]. Therefore, the user can mask individual or various combinations of SPACIROC2 channels.

Unlike MAROC3, the charge measurement is performed by SPACIROC2 using the Q-to-T Converter block. This is also called the KI module because it is based on a Time Over Threshold technique inherited from KI02/03 chip [346]. The Q-to-T converter allows to measure the charge available at the MaPMT anodes [352].

The digital part of the SPACIROC2 architecture consists in three modules being marked in figure 4-1 with a yellow rectangle common to all 64 analog channels. The digital part comprises of four DACs with 10-bit resolution, voltage reference Vbandgap and multiple-input OR logic gates. The other two digital modules are assigned to the Photon Counting and KI block. Each of them embeds Gray counters, registers and readout state machine. Data acquisition and readout from the digital architecture of the chip is made in a well-defined time slot called Gate Time Unit (GTU). One GTU cycle takes 2.5 μ s during which available data are loaded for sending and previously acquired ones are sent out via serial links to a processing unit implemented in a FPGA firmware [352].



Figure 4-2 The SPACIROC2 test board before and after assembling with the chip put on socket.

0 1



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The MaPMT signal is emulated for SPACIROC2 testing with a pulse generator that feeds with signal the LEMO connector on the ASIC test board, also called C_{TEST} , which is directly connected to the chip internal 2 pF capacitor as in case of MAROC3. However, the setup for performing these basic functionality tests is much easier than for MAROC3, see figure 4-4. The setup synchronisation signal is delivered by on board FPGA through a LEMO connector named Out_FPGA_1 and it is shared to the external test and measurements devices. Settings are made on the pulse generator to produce a square signal with a 5 ns falling edge that emulate the MaPMT output. This is triggered when the 400 kHz synchronisation signal is applied to its trigger input. The waveform of those signals is presented in figure 4-5 along with a FSU shaper response.

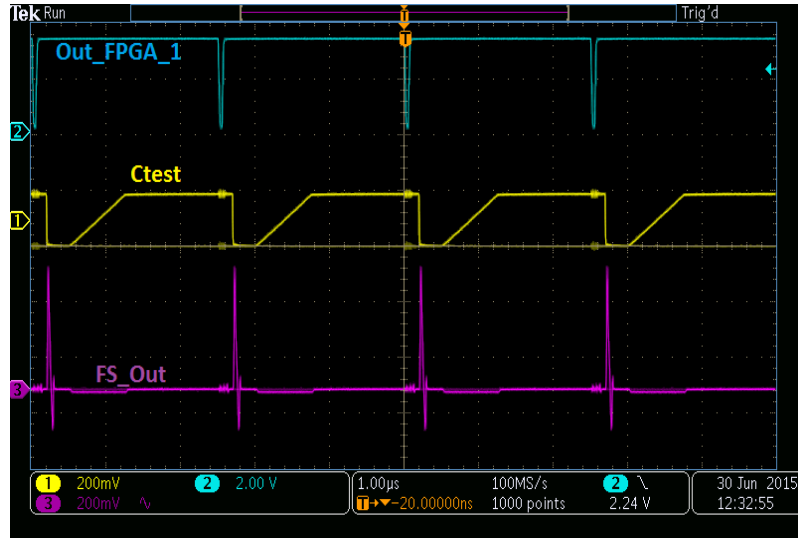


Figure 4-5 The waveform graph with synchronisation signal, pulse generator output and FSU response.



Figure 4-6 The signal response of FSU shaper to 300 fC input charge.



Figure 4-7 The signal response of VFS shaper to 300 fC input charge.

The next step was to check the FSU and the VFS shapers, see figure 4-6 and 4-7, feedbacks at the same input charge, i.e. roughly 2 photo-electrons. It can be seen in figure 4-6 that the FSU shaper has a better response considering the signal amplitude and the stiffness of the rising edge. So far, this recommends the path encompassing the FSU shaper as the most appropriate for testing the single-photon counting capabilities of SPACIROC2.

4.2 Automatic test bench for irradiation

Apart from its mainstream application, the JEM-EUSO cosmic ray's observatory, this SPACIROC prototype is also a blueprint for the next generation of MAROC, desired to be more radiation tolerant. This was the reason why SPACIROC2 chip was taken into consideration for radiation hardness qualification and a dedicated irradiation campaign is pursued. During the irradiation test a special attention is given to the digital part because of its complexity in contrast with MAROC3 chip architecture. Though, the layout part corresponding to digital block was optimised to fit within less area of the device silicon die. Several digital circuitries inside ASIC were implemented in Triple Modular Redundancy (TMR) as hardware mitigation technique.

The parameters to be monitored during tests were initially discussed with the SPACIROC design team, as in case of MAROC3. The list of these parameters to be monitored and measured before, during and after irradiation qualification test is given in table 4-1. The analogue and digital part have separate supply rails allowing for better distinguishing between the various radiations induced effects as they manifest in each electronic block. The list of parameters is quite extensive due to the digital part. Unfortunately, some of the parameters cannot even be monitored directly.

Any SEL development can be isolated for the analogue or the digital part, thus allowing pointing out which electronic block is more prone to exhibit a high current consumption state. The output voltages of all four DACs will be monitored as well as their level variations in time with respect to the initial set values. Investigating these dependences could help to deliberate whether SEEs occurs or TID cumulative effects perturb the semiconductor device operation. Nevertheless, all DACs registers were implemented in hardware TMR layout and it is less likely that a SEU or MBU could affect their configuration bits to cause a step change in the output voltages. The DAC2 linearity test will highlight if this mixed-signal circuitry is

susceptible to the cumulative effects caused by the TID or permanent damage induced by SEEs like SEGR. Any malfunction of the digital part in conjunction with the Photon Counting unit will manifest in the S-curve and pedestal deviation. Signs of cumulative structural defects could be uncovered if the Vbandgap or others parameters out coming from DUT undergoes variations in amplitude during irradiation. A useful approach is to establish if slight changes in parameter values correlate with environment temperature fluctuations, otherwise they could be caused by radiation cumulative effects.

Table 4-1 List of the monitored parameter for SPACIROC2

before /after irradiation	during irradiation
• Test board power consumption	▪ Test board power consumption
• ASIC analog part power consumption	▪ ASIC analog part power consumption
• ASIC digital part power consumption	▪ ASIC digital part power consumption
• DAC2 linearity	▪ Internal voltage references (Vbandgap)
• Internal voltage references (Vbandgap)	▪ DC voltage component of Analog Probe (PA_BUFF)
• DC voltage component of Analog Probe (PA_BUFF)	▪ DAC1 output (vth_discr_i_pa)
• DAC1 output (vth_discr_i_pa)	• DAC1 output (vth_discr_i_pa)
• DAC2 output voltage (vth_discr_fs)	• DAC2 output voltage (vth_discr_fs)
• DAC3 output voltage (vth_ki_sum)	• DAC3 output voltage (vth_ki_sum)
• Trigger efficiency (Scurves)	• Temperature
• Pedestals	
• Temperature	

Three test boards equipped with SPACIROC2 chips were carefully investigated from electrical parameters stand point and not only. On each board, multiple measurements were performed in the laboratory under normal conditions and the recorded parameters are considered as baseline during the irradiation tests.

4.2.1 Hardware part of the test bench

Similarities between the SPACIROC2 and MAROC3 chips make the automatic test bench for SPACIROC2 resemble the one for MAROC3, reusing most of the test and measurement instruments as the monitoring unit from figure 3-13 and even partially replicating the monitoring strategy. The hardware layout is shown in figure 4-8 and it was proposed by me. The innovative components of the test bench hardware are the data acquisition (DAQ) system and the remote-controlled switching mode power supply (SMPS) as parts of the monitoring unit presented in previous chapter. In-house designed by our group, the DAQ system was thought to meet the technical requirements of monitoring and continuously recording the parameters listed in table 4-1.

The test bench running principle is described in the following. The DUT test board is supplied with the bipolar voltage of ± 7 V. The power supply is controlled by the DAQ system which also measures the power consumption on each of the supply rails at every 50 ms. The SMPS is capable to deliver a maximum current of 2 A on both rails. The MaPMT signals are emulated by a pulse generator and delivered to the chip C_TEST input pin synchronously

with the test board output signal from Out_FPGA_1 LEMO. Also, the signals available on the test board measuring points can be checked using an oscilloscope. Inherited from the MAROC3 test bench, an infrared contactless sensor is used to record the dice or PCB temperature well as possible temperature fluctuations in the environment. If needed, live video streaming of the test bench can be provided during tests by means of a web camera. All test bench parts make available the sampled data via USB interface to a host PC placed in to the experimental room at safe distance, except the SMPS. The data are then forwarded over Ethernet to the control room PC where the test procedure is overseen.

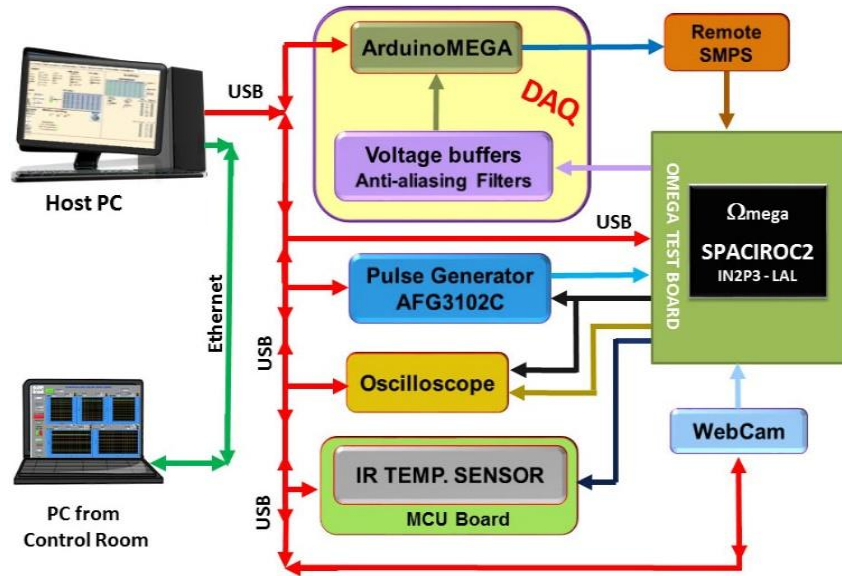


Figure 4-8 Layout of the automatic test bench for SPACIROC2 under irradiation.

The wiring diagram from SPACIROC2 to the DAQ system was done to accommodate the device under test requirements over 5 m screened multi-pair cables. Hence, the electrical parameters of the test board which are not crucial for the chip characterisation it will be sampled with 8-bit resolution ADC. On the other hand, the ASIC power consumption and embedded DACs output are sampled with 10-bit resolution ADC inputs of the DAQ.

4.2.2 Software part of the test bench

A software routine was developed for the processing unit implemented around ATMEGA260 microcontroller to enable it for reading out MAX1270 external ADC values over a SPI interface as well as its built-in ADC. The values measured for all analogue input channels are packed and sent over a USB interface every 50 ms. Another routine is dedicated to the SMPS control. The data received over USB by the host PC is in ASCII format containing a time stamp. It is displayed in real time by the LabVIEW GUI as seen in figure 4-9. In the left side panel of the GUI are the control buttons that allows stopping the interface, to switch ON/OFF the SMPS, to enable or inhibit data measurement and saving, to reset the information displayed by the graphs. Also, the red button called Beam OFF was foreseen within GUI to be actuated by the user when the beam is ON or OFF. This adds a useful flag in the ASCII file with recorded data for later analysis.

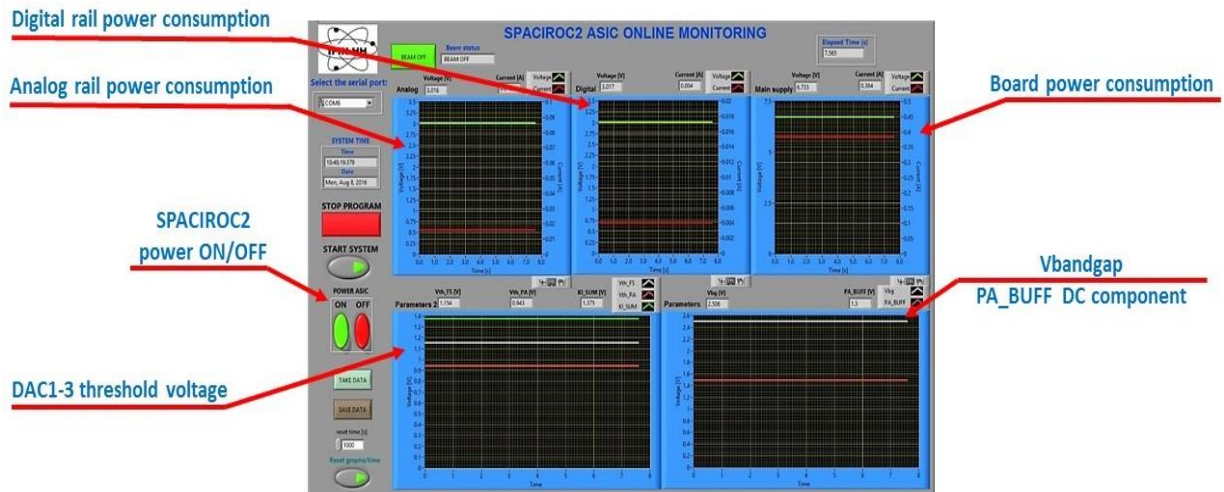


Figure 4-9 GUI used to control the SMPS and to monitor the SPACIROC2 parameters.

The user may define a threshold for each monitored parameter, so once exceeded a warning message will pop up. When such a warning appears, the user can decide to continue the monitoring or take immediate action to power off the DUT board. Data collected in the ASCII file is subjected to a detailed analysis and interpretation further on.

4.3 Irradiation test with 200 MeV proton beam

Irradiation campaign for SPACIROC2 started at the Proton Irradiation Facility (PIF) from Paul Scherrer Institute (PSI), Switzerland. In this facility the beam is delivered by a compact cyclotron named COMET capable to provide a proton beam with 250 MeV energy [353]. In case of SPACIROC2 the beam flux was $1.089 \cdot 10^9$ protons/cm²s. The DUT board was mounted on a metallic sampler holder in front of the beam exit window along with the test bench in the side as it can be seen in figure 4-10. Also, the oscilloscope and the pulse generator were installed 15 m away in the access corridor to the irradiation room, thus ensuring a higher degree of radiation protection for test and measurement devices. A laser alignment procedure was done to properly position the 18.86 mm² (4.6 mm x 4.1 mm) chip die with respect to the beam axis. This step was repeated for each DUT board tested.

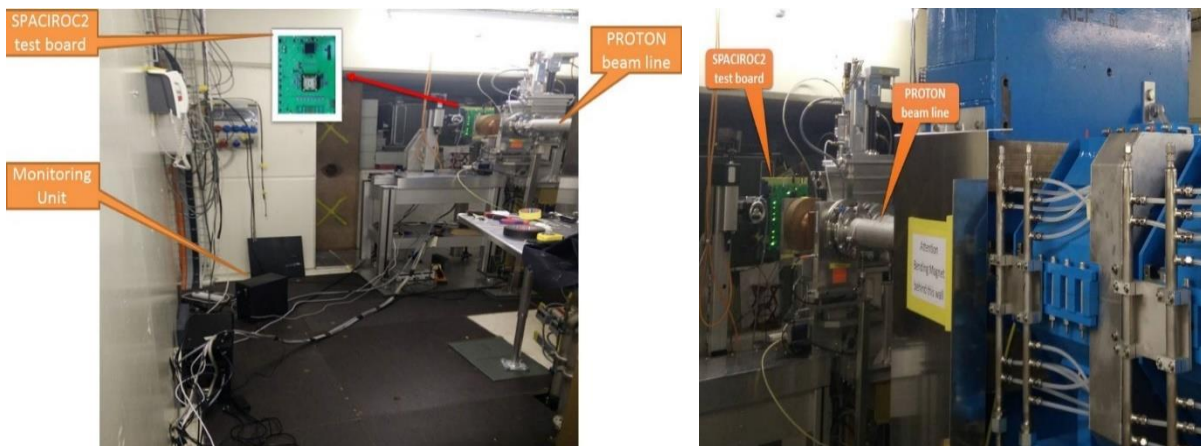


Figure 4-10 The SPACIROC2 test bench installed at PIF (left side) and the beam line in close view (right side).

The initial testing strategy was to deposit a 100 krad TID (Si) and depending on the chip behaviour the dose would be increased gradually up to the level of Mrad. If chip functionality would be lost below the 100 krad dose, a threshold scan for the radiation induced effect within this range must be pursued for the other two chips. The possibility has been exploited to look either for cumulative effects or SEE triggered by indirect ionization. This has been done by exposing the chip to protons at this high energy level. The JEM-EUSO space mission is planned to last almost up to 5 years and the cumulative dose estimated per year is 0.1 krad [351]. Thus, the cumulative effects induced by TID or DD will be harmful to on board electronics of the telescope. In contrast, at this beam energy it must envisage the SEE through the secondary ionization. Whereas a proton strikes an atom from the semiconductor lattice, further might trigger the emission of secondary atoms through various mechanisms as displacement, spallation and nuclear interaction. This secondary has higher LET comparing with the protons and it can further facilitate charge deposition. Once the critical charge threshold is exceeded then SEEs occur. These effects are potentiated by the percent, as well as the nature of materials used for the chip doping and metallization. Regarding the ASIC circuitry, among the TID test it is mandatory to investigate if its configuration registers are vulnerable to SEU/MBU. Considering the chip relative complex digital part and its possible high susceptibility to radiation induced events, the test procedure was designed to support the worst case scenario and the test bench was implemented to react to changes of key monitored parameters so, therefore to prevent the DUT permanent damage.

4.3.1 Data analysis and interpretation

The qualification of the SPACIROC2 chips started with a full test of each DUT after being installed on the beam line with the beam switched off. The values measured for ASICs parameters were checked against the baseline values recorded in laboratory, also considering the inside irradiation room temperature which fluctuated in the range of 30-36 °C. Initially the DUT irradiation procedure was thought to be made in step of 100 krad up to a cumulated dose of few Mrad. The evolution of monitored parameters of each irradiated DUT sample would be presented further.

The following plots highlight the first chip behaviour before and during the exposure to the 200 MeV proton beam up to a cumulated TID of 100 krad. Prior to irradiation the first chip tested had the power consumption very stable as it can be seen in figure 4-11, excepting the 0-15 s time interval where the chip received the configuration (Slow Control) commands. The first DUT board had the power consumption monitored even after the proton beam was turned off, see figure 4-12.

The first DUT board was power cycled six times out of which four times during irradiation, once right at the end of the irradiation and once more during the monitoring period after the beam was turned off. The board current consumption IVDD increases in two abrupt steps followed by a gradual growth towards the end of the irradiation. An overall effect of annealing at room temperature (about 35 °C) is seen after the last power cycle when parameter values seem to return to normal (no permanent effect is noticed). However, IVDD contains contributions from each power rail (analogue and digital) of the chip. A closer look at the analogue rail current consumption (in figure 4-13) reveals that its value increases in a single step almost at the end of the irradiation.

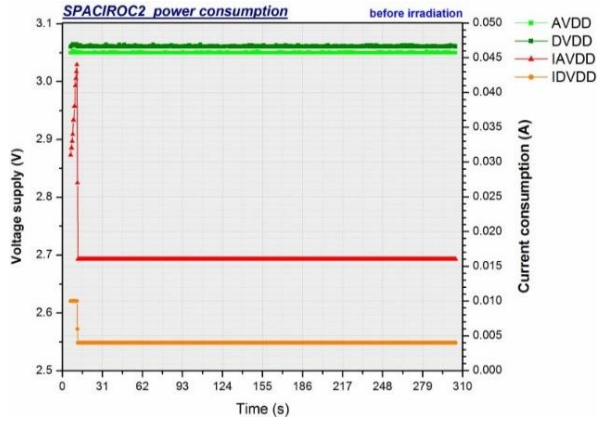


Figure 4-11 The power consumption of the first chip before irradiation.



Figure 4-12 Board power consumption during and right after irradiation.

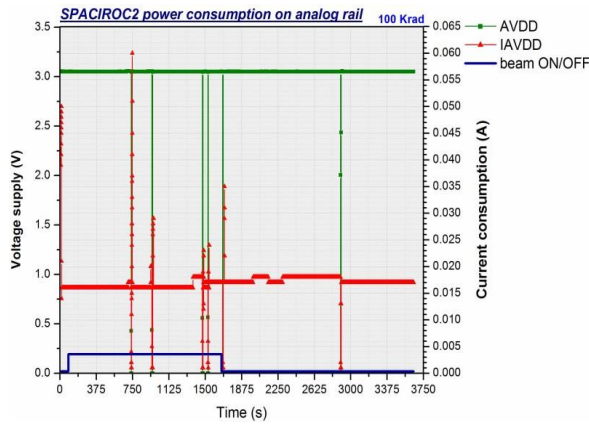


Figure 4-13 Analog power consumption during and right after irradiation.

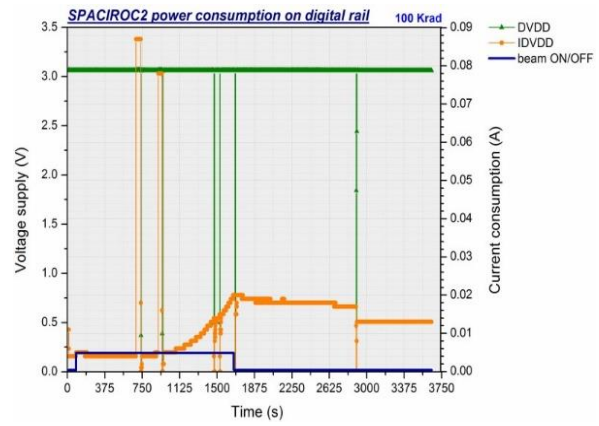


Figure 4-14 Digital rail power consumption during and right after irradiation.

Power cycling the board it was observed that the analogue current IAVDD remains to value higher than base line one of 16 mA, hence leakage current induced by TID. In contrast the current consumption on the digital rail jumped twice to high current states corresponding to two SELs which vanish after power cycling the board. Then IDVDD increases almost exponentially up to the end of the irradiation period. A zoom-in of this growth trend in figure 4-15 shows that IDVDD increases in almost equal steps. This effect could also be attributed to SEUs occurring in the chip configuration registers which might induce high power consumption due to misconfiguration of built-in circuitry. A clear answer is expected to be obtained during future irradiations when a configuration read-back procedure will be implemented to test for possible corruption of the configuration bits. However, the digital block did not recover when the board was power cycled twice towards the end of the irradiation period. The annealing process is clearer for the digital block of the chip as its current consumption returns to the base line value in steps after the beam was turned off. At the same time this process seems to be much slower as the digital current was found to return to its value before irradiation only when was checked again in the next day - see figure 4-16.

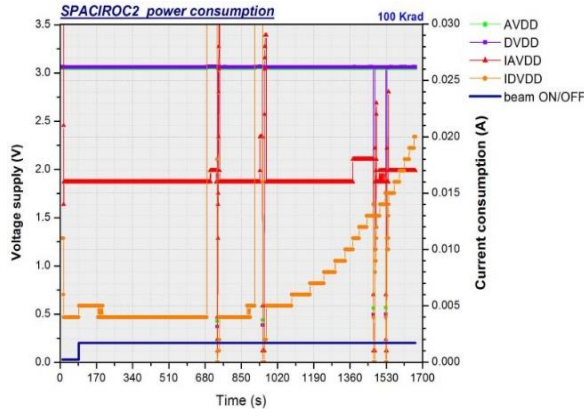


Figure 4-15 Zoom on current axis for the chip power consumption under irradiation.

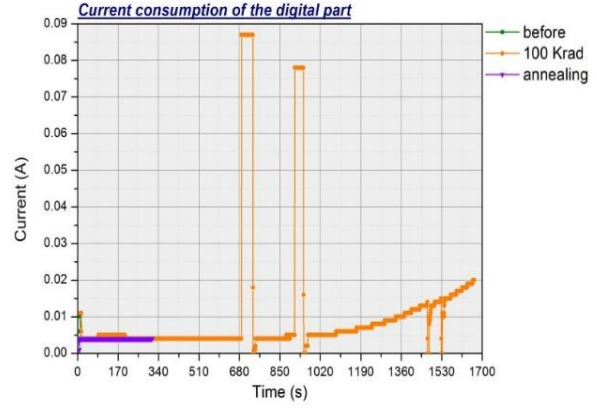


Figure 4-16 Digital current rail before, during irradiation and post-irradiation.

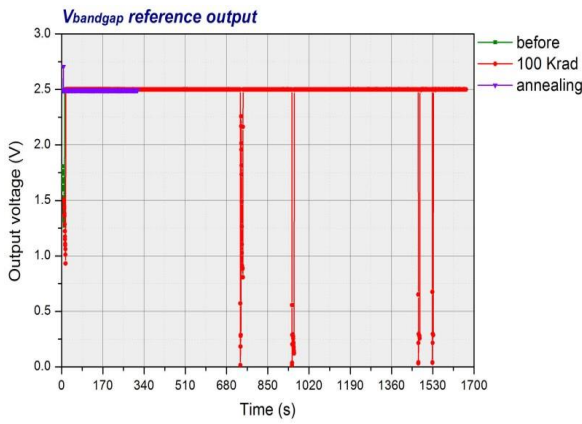


Figure 4-17 Output voltage of the chip internal voltage reference.

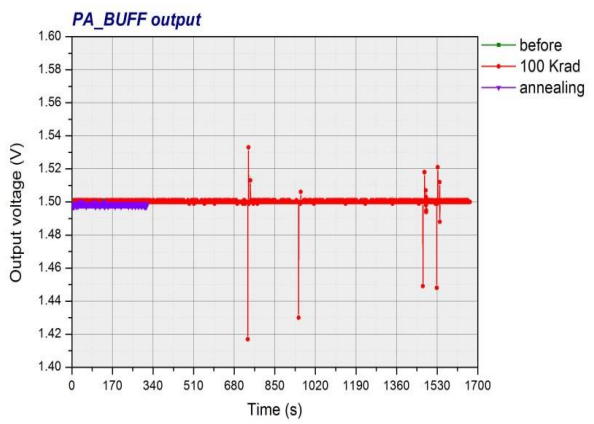


Figure 4-18 The DC voltage component of Analog Probe.

Other parameters like chip internal voltage reference (V_{bandgap}), DC voltage component of Analog Probe (PA_BUFF), DAC1 output, DAC3 output and DAC2 output did not show any significant variation during irradiation. The spikes in their distributions from figures 4-17 to 4-21 correspond to the board power cycling and SPACIROC2 reconfiguration. The amplitude of these jumps matches the values registered for this board before and one day after the irradiation test.

Despite the output voltage of DAC2 was stable during irradiation (figure 4-21), the smooth linearity curve lost its monotonicity and has step transitions as shown in figure 4-22. The DAC2 resolution is reduced from 10 to 3 bits as only the highest bits of the register appear to trigger a significant output voltage increase. This behaviour shows a clear effect of TID on the DAC response, also being reported in literature for other integrated circuits embedding DACs [354]. The linearity curve returns to normal after almost 24 hours of annealing at room temperature so this TID effect is not permanent. These effects indicate high vulnerability of the SPACIROC2 digital block to radiation.

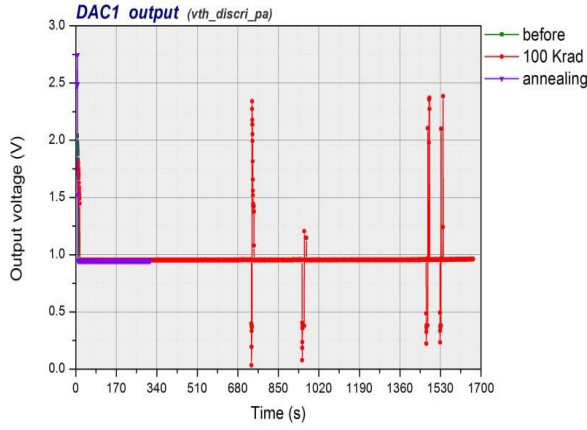


Figure 4-19 Output voltage of the DAC1.

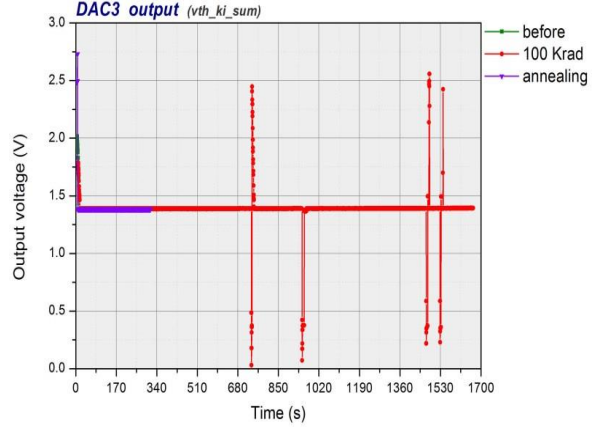


Figure 4-20 Output voltage of the DAC3.

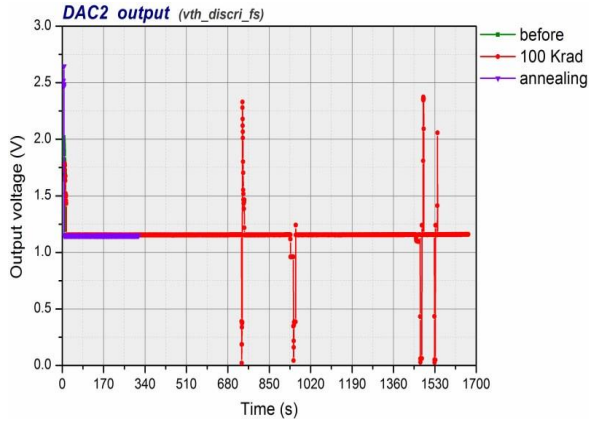


Figure 4-21 The DAC2 output voltage of the first irradiated chip.

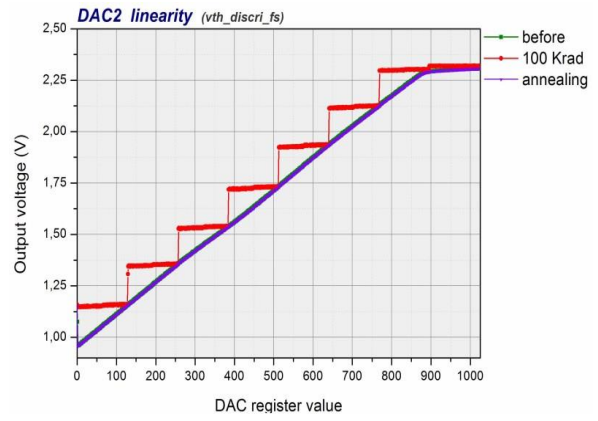


Figure 4-22 The DAC2 linearity test after 100Krad TID.

Furthermore, the trigger efficiency curves were investigated for an input charge of 150 fC injected on all 64 channels of the chip. Both the Scurves and the pedestal curves were measured. The pedestal corresponds to the trigger efficiency measurements when the threshold voltage vth_discr_fs is very close to the Trig_FSU discriminator input reference level. This allows a qualitative characterisation of the noise fluctuation during irradiation. The pedestal and efficiency curves are given in figure 4-23 and figure 4-24, before first chip was irradiated. After 100 krad TID deposition, no efficiency curves could be measured since the photon counting block did not run any more in conjunction with the digital part perturbed by radiation. It is likely that another circuitry inside the digital block could have failed, despite the DAC malfunction. After the 24 hours annealing period the efficiency curves were measured again as shown in figure 4-25 and 4-26. Both the pedestals and Scurves show negligible variations with respect to the efficiency curves recorded before irradiation, so the annealing process seems to remove any TID effects cause by the proton beam.

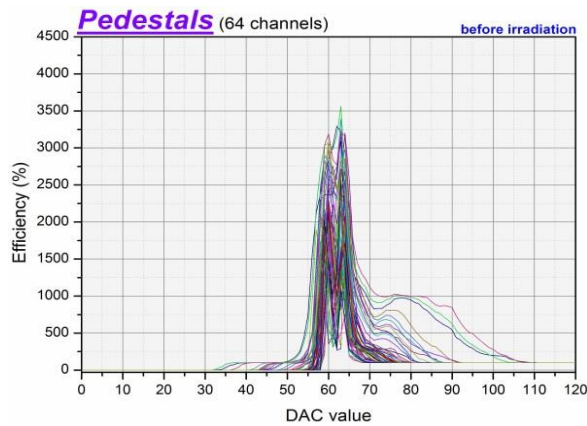


Figure 4-23 Pedestals curves of the first chip before irradiation.

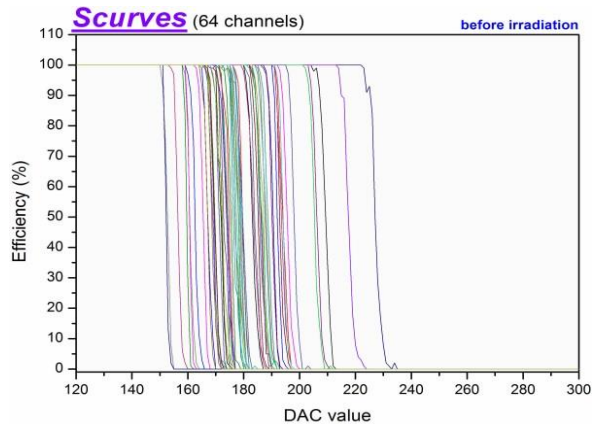


Figure 4-24 Efficiency curves of the first chip before irradiation.

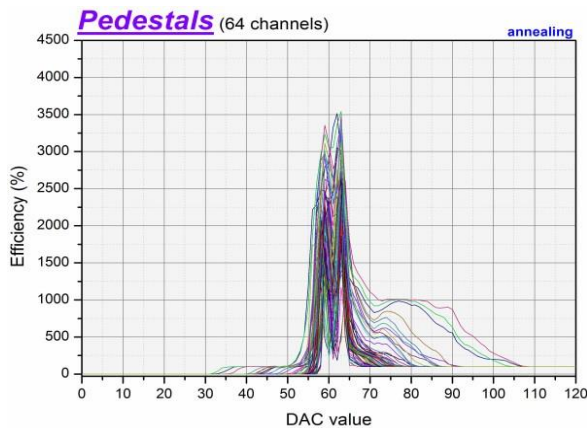


Figure 4-25 Pedestals curves of the first chip after annealing took place.

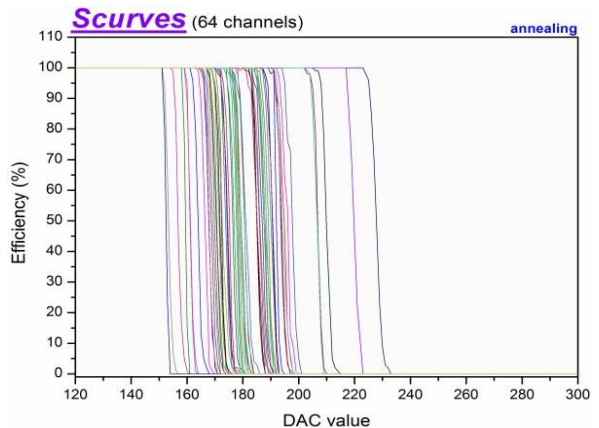


Figure 4-26 Efficiency curves of the first chip after annealing took place.

Considering the earlier results, for the second SPACIROC2 chip the irradiation procedure was reconsidered. With the purpose of determining the TID threshold where the chip ceased to run properly, the irradiation was pursued in steps of 10 krad up to 100 krad. The second chip analogue block current consumption is presented during the irradiation in figure 4-27. For the final TID of 101.414 krad a step increase is observed. When the digital rail current started to grow during last dose deposition, the DUT board was power cycled twice and the current on analogue rail increased with 6.6%. In both cases, the current maintained at the new level, so no recovery for the chip was observed. Again, a drastic increasing of the current on digital part was recorded as for the first irradiated SPACIROC2, but no SELs occurred. The digital current registered a step growth for TID of 59 krad and 60.014 krad, but subsequently the chip recovered without power cycling the board as one can see in figure 4-28. At 70.614 krad the digital current step jumped to a new stable value about 25% higher than the nominal. The next doses applied increase even higher the digital current level and at 101.414 krad the measured value was double respect to the baseline.

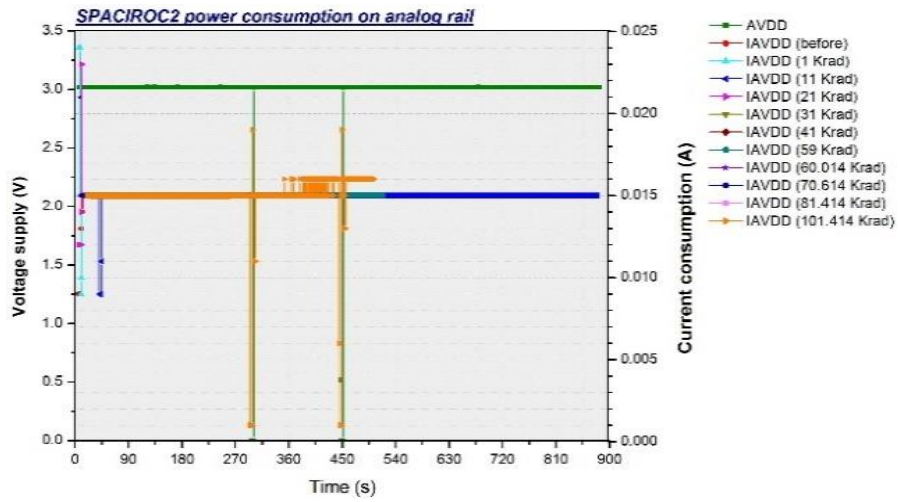


Figure 4-27 Analog current consumption for the second chip during irradiation.

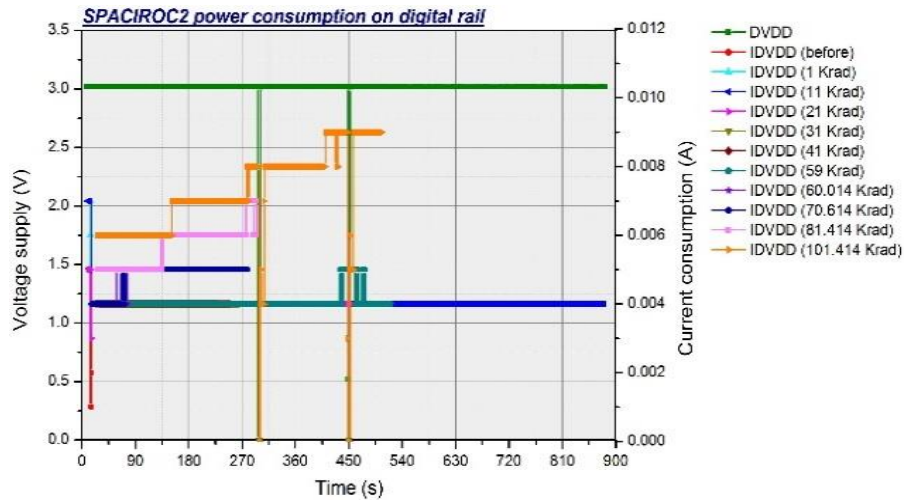


Figure 4-28 Digital current consumption for the second chip during irradiation.

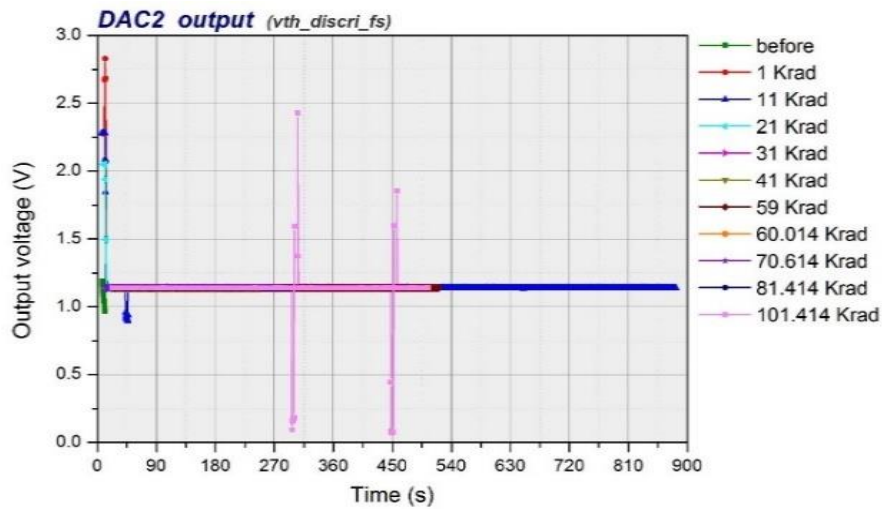


Figure 4-29 The DAC2 output voltage for the second chip under radiation.

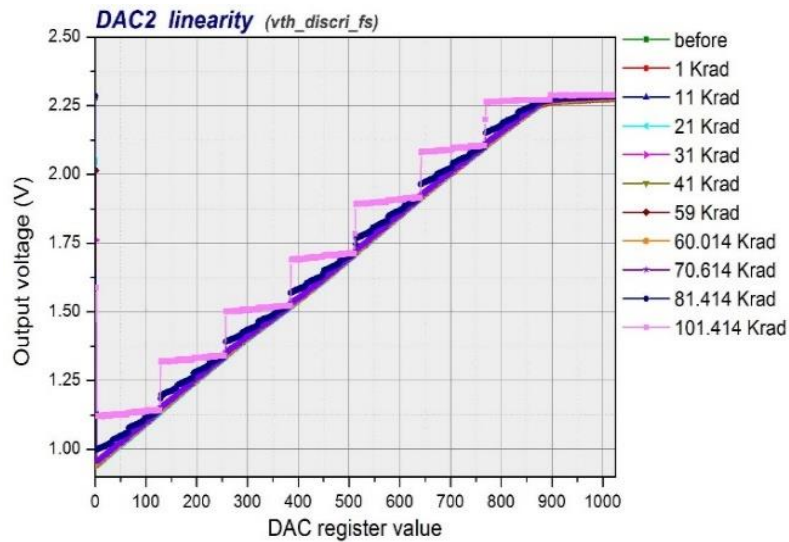


Figure 4-30 The DAC2 linearity test for second chip after each dose.

No changes in the output voltage for the DAC2 were observed during chip irradiation except the two pairs of up-down spikes corresponding to the board power cycles - see figure 4-29. The DAC2 linearity lost again its monotonicity at a TID about 70.614 krad. As it can be seen in figure 4-30, the DAC2 linearity deteriorates over this TID and for the final absorbed dose of 101.414 krad one gets the same drop in resolution, so only 3 (highest) out of 10 bits of the configuration register can be set.

Trigger efficiency curves have been determined in similar fashion as for the first tested chip by injecting a 150 fC input charge to all the 64 channels. The pedestal curves show significant variations when the 70.614 krad TID is exceeded. For instance, their shapes modify at 81.414 TID in figure 4-35 with respect to the base-line shown in figure 4-31.

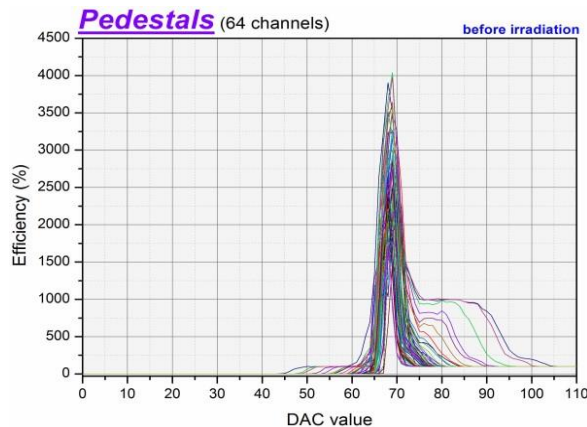


Figure 4-31 Pedestals curves of the second chip before irradiation.

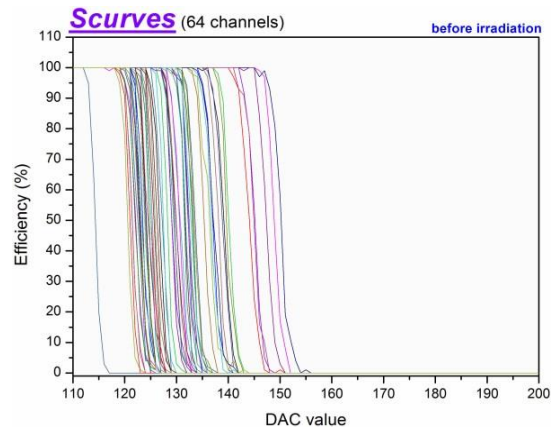


Figure 4-32 Efficiency curves of the second chip before irradiation.

As it can be seen in figure 4-34 the Scurve undergo a left shift at 70.614 krad TID in contrast with their baseline position in figure 4-32, due to the deterioration of the DAC2 linearity. This behaviour accentuates for larger TIDs, in figure 4-36 till the pedestal overruns the Scurve domain for the 101.414 krad TID as it can be seen in figure 4-37. It should be noted that contrary to the first chip behaviour, the efficiency curves are could still be registered at the largest TID and this fact is attributed to the policy of cutting-off the chip power after each deposited dose. Nevertheless, the digital block of the chip failed to run.

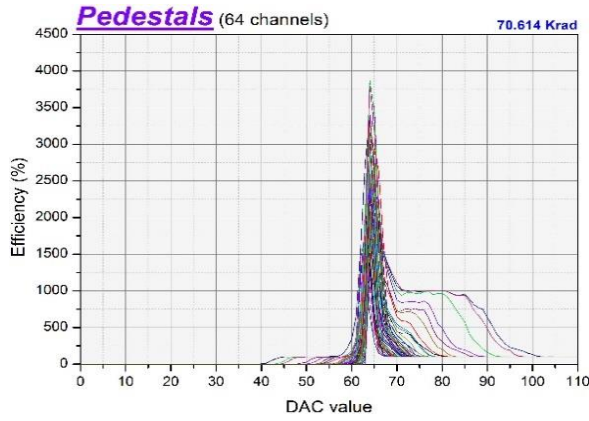


Figure 4-33 Pedestals curves of the second chip after 70.614 krad.

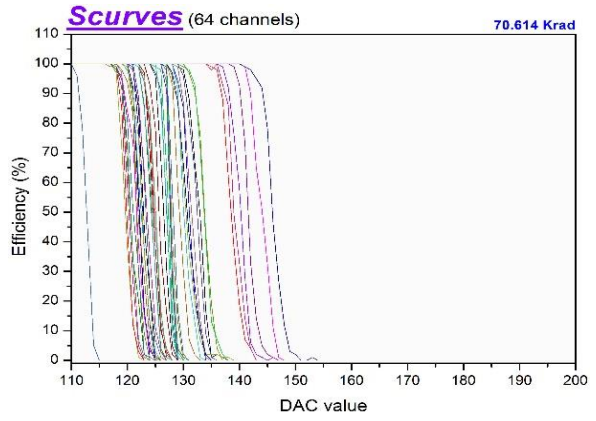


Figure 4-34 Efficiency curves of the second chip after 70.614 krad.

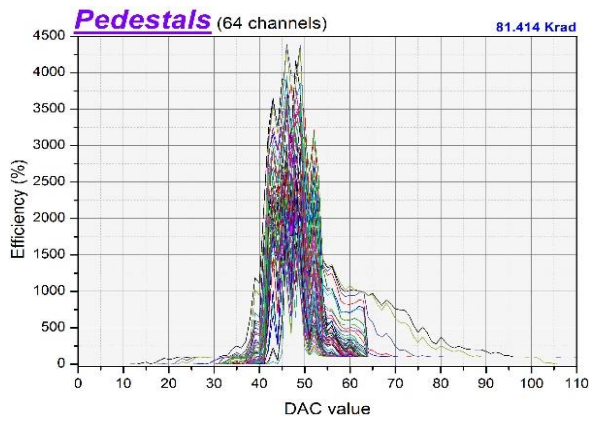


Figure 4-35 Pedestals curves of the second chip after 81.414 krad.

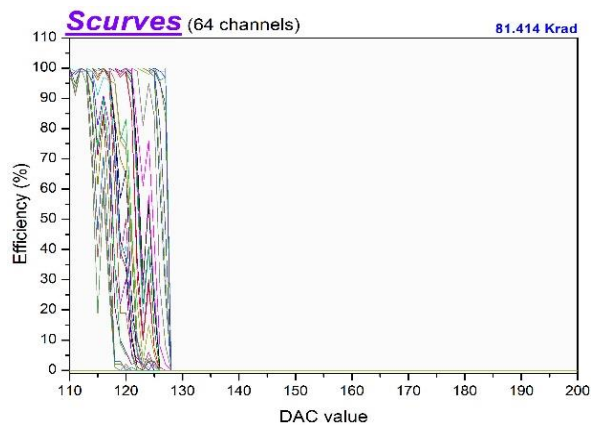


Figure 4-36 Efficiency curves of the second chip after 81.414 krad.

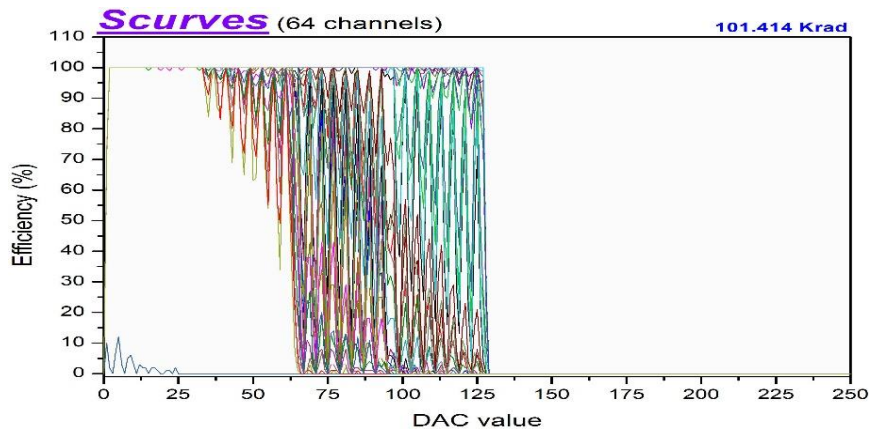


Figure 4-37 Pedestals and efficiency curves of the second chip after 101.414 krad TID.

In order to reconfirm the threshold TID from which the radiation induced effect begin to dominate, the third chip was irradiated in six steps up to total absorbed dose of 83.12 krad. As for the previous chips, step growths of both the digital and analogues currents were recorded. Moreover, as shown in figures 4-38 and 4-39, at the maximum TID the analogue current stabilized to a new value with 6.6% higher than the base line. After almost a day of annealing at room temperature (around 35 °C), the chip parameters returned to the values measured before irradiation.

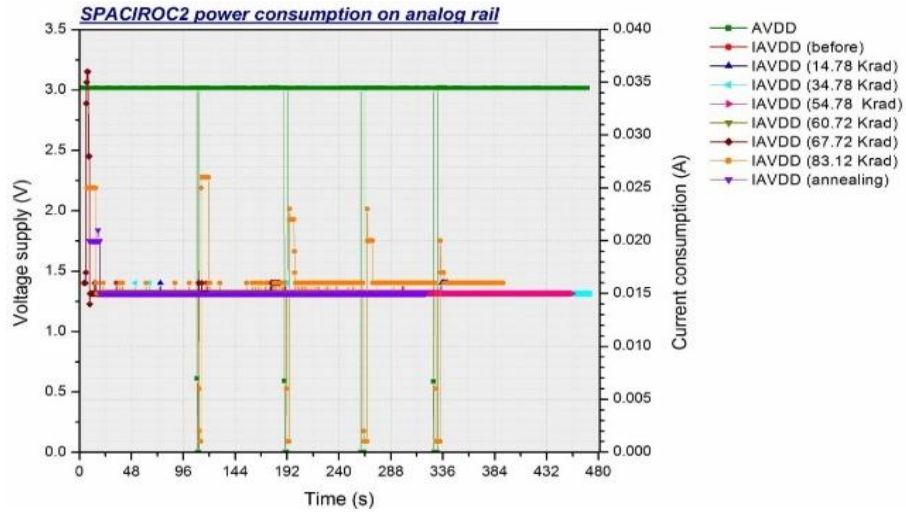


Figure 4-38 Analog current consumption for the third chip during irradiation.

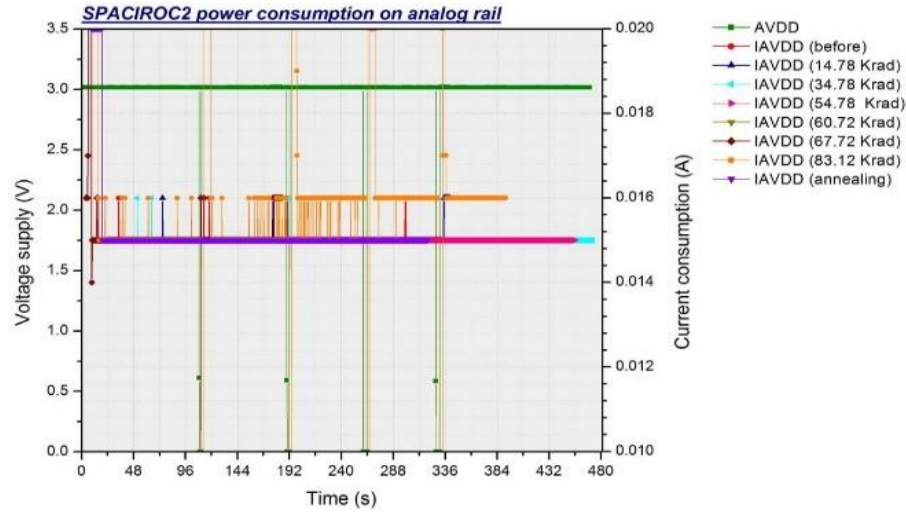


Figure 4-39 Zoom on analog current axis of the third chip under irradiation.

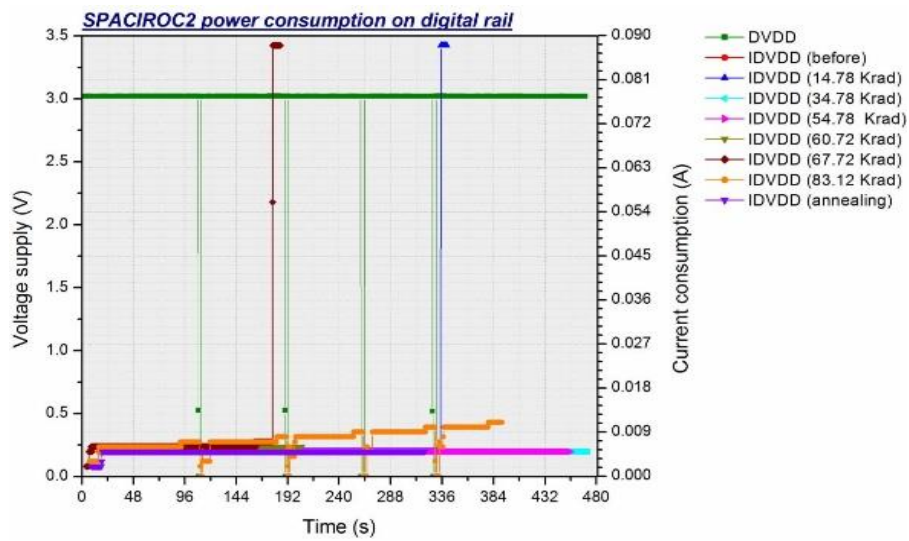


Figure 4-40 Digital current consumption for the third chip during irradiation.

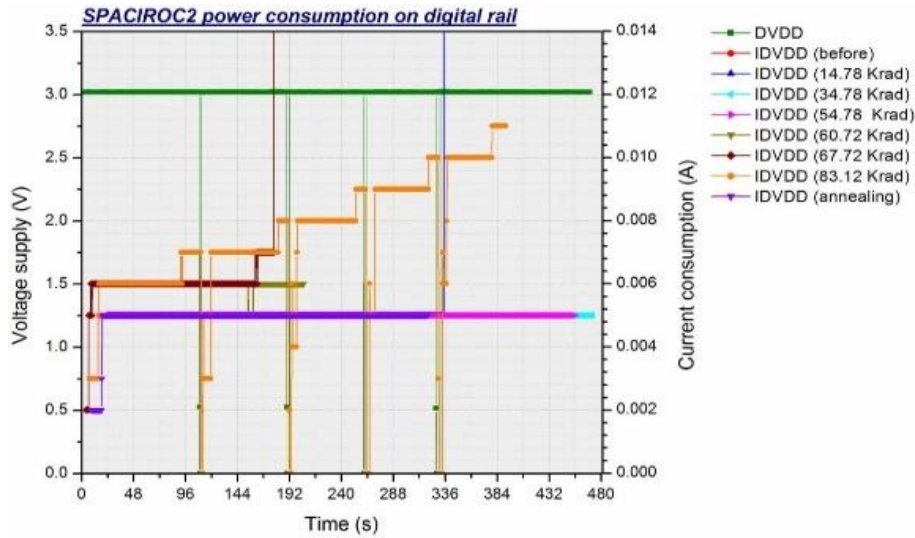


Figure 4-41 Zoom on digital current axis of the third chip under irradiation.

Two high current states of the digital block were registered as for the first chip. The SELs occurred at TIDs of 14.78 krad and 67.72 krad and the chip functionality was recovered with power cycles - see figure 4-40. The digital block current started to grow in steps at around 60.72 krad. During the last exposure to the proton beam, the board was power cycled four times, as shown in figure 4-41, but the current in the digital block did not return to its baseline value. Only after annealing at room temperature the TID effects disappeared and the current consumption on the chip digital rail returned to its reference level.

No voltage variation in the DAC2 output was observed before, during and one day after the irradiation. The up-down voltage spikes visible in figure 4-42 are caused by power cycling and reconfiguring the chip four times within the last dose deposition. As in the case of previous DUT samples irradiated, also for the third one the DAC2 lost its linearity when the TID exceeded 67.72 and 83.12 krad, see figure 4-43. Through annealing the DAC2 linearity curves were recovered.

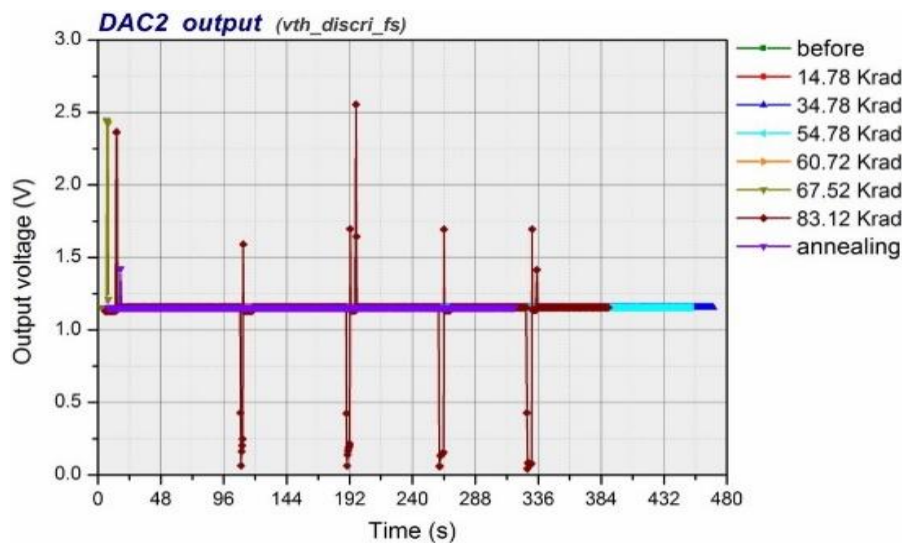


Figure 4-42 The DAC2 output voltage for the third chip under radiation.

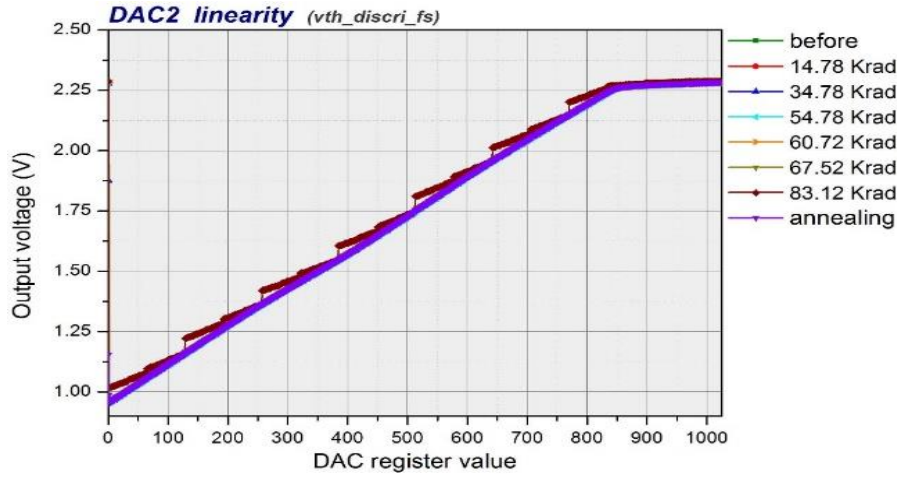


Figure 4-43 The DAC2 linearity test for third chip after each dose.

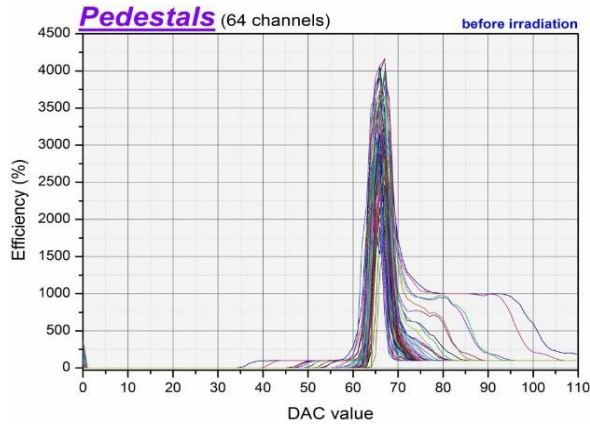


Figure 4-44 Pedestals curves of the third chip before irradiation.

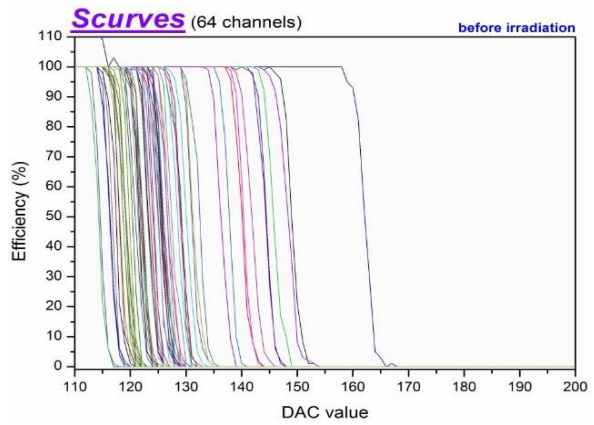


Figure 4-45 Efficiency curves of the third chip before irradiation.

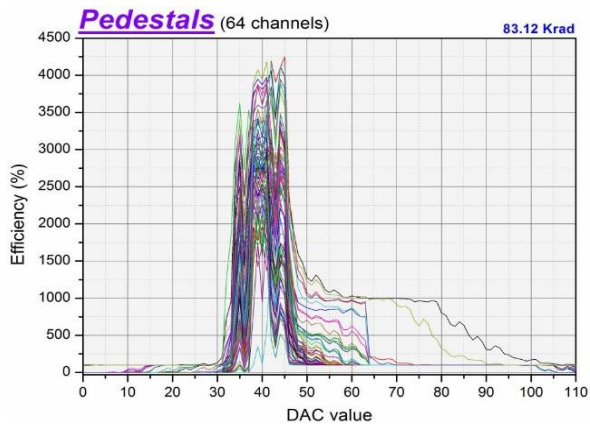


Figure 4-46 Pedestals curves of the third chip after 83.12 krad.

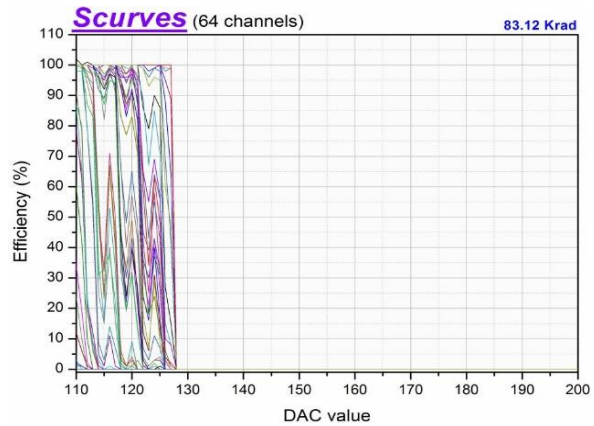


Figure 4-47 Efficiency curves of the third chip after 83.12 krad.

The same test conditions were kept for the trigger efficiency curve measurement. The behaviour described for the second irradiated chip was observed also for the third sample - see figures 4-44 through 4-47. The pedestal curves overran the Scurves during the deposition of the last dose up to the 83.12 krad TID corresponding to the loss of DAC2 response linearity - see figures 4-46 and 4-47. After annealing, the efficiency curves in figures 4-48 and 4-49

show negligible to no variations of their shapes and values measured before irradiation. Further in-depth analysis of the data was performed to check if any of the 64 channels failed to be measured during irradiation. Also, the variations for other parameters describing the efficiency curves were investigated.

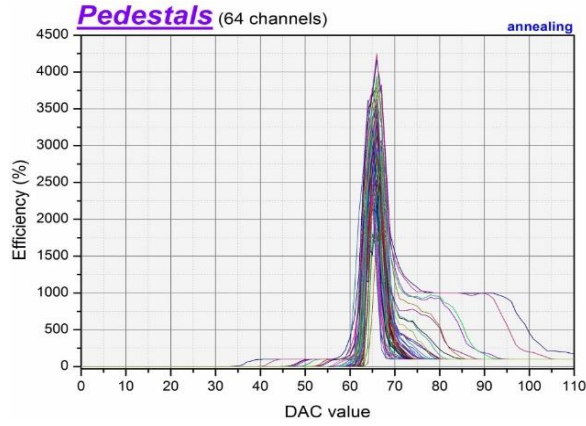


Figure 4-48 Pedestals curves of the third chip after annealing.

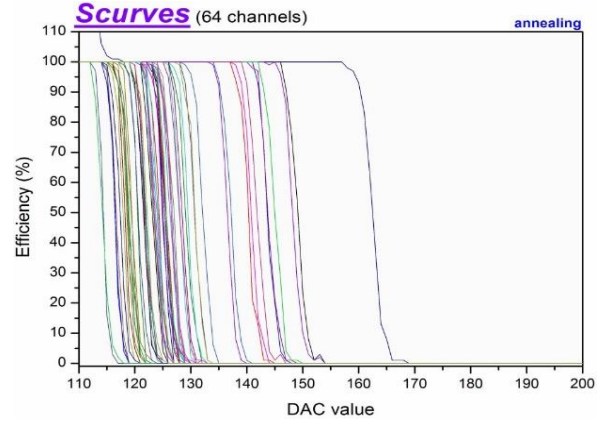


Figure 4-49 Efficiency curves of the third chip after annealing.

I did a close analysis for the trigger efficiency curve on each of the DUTs channels. For this purpose, a Python script was developed to check if the individual channels of the irradiated chip samples changed their position, form or slope from dose to dose. In Appendix C are presented the pedestal and Scurves for each channel of the second and third chip tested. As general observation, on either chip the pedestal curves and Scurves significantly shifts after 60 krad TID or equivalently the trigger efficiency is getting worse. In all channels investigated, the pedestals curves changed their form and position after the accumulated TID exceeded the above value. This change is exemplified in figure 4-50 and figure 4-52 where the chip recovers through annealing at room temperature. On the other hand, we found that the efficiency curves of few highlighted channels exhibited a severe degradation such as in figure 4-53. However, in most channels of the two chips, the Scurves shift their position at higher doses but recover through annealing, see figure 4-51.

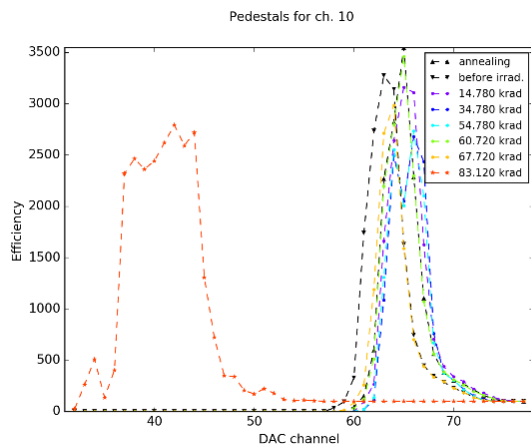


Figure 4-50 Pedestals curves changing from dose to dose corresponding to the channel 10 of third irradiated chip.

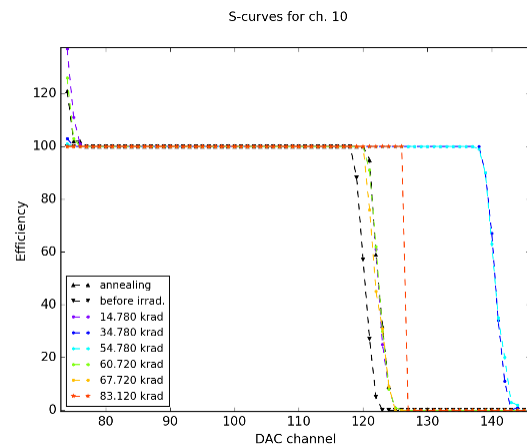


Figure 4-51 Efficiency curves shifting from dose to dose corresponding to the channel 10 of third irradiated chip.

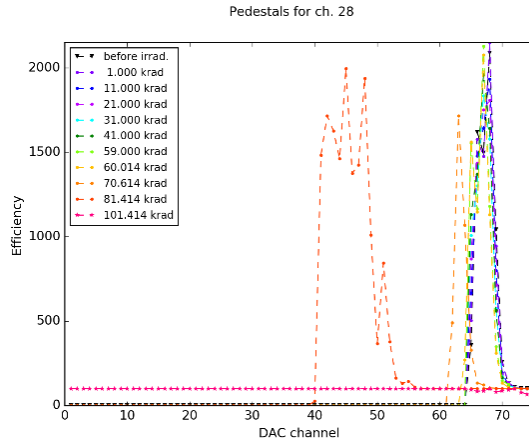


Figure 4-52 Pedestals curves changing from dose to dose corresponding to the channel 28 of second irradiated chip.

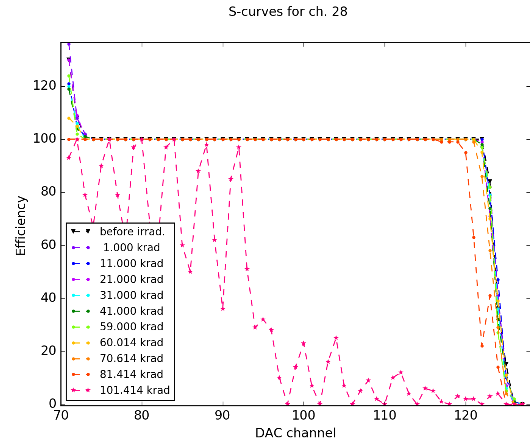


Figure 4-53 Efficiency curves shifting from dose to dose corresponding to the channel 28 of second irradiated chip.

In the upcoming irradiation tests, there are plans to investigate the TID impact on the trigger efficiency curves. Up to now, the main cause for these changes in efficiency curves was singled out in the DAC2 linearity problems at higher doses. Beside this, the SPACIROC2 immunity against the SEL phenomena will be carefully examined. So far a total of 4 SEL events were recorded for three tested SPACIROC2 ASICs with 200 MeV proton beam. The SEL cross-section computed based on measurement was found to be $0.78 \cdot 10^{-12} \text{ cm}^2$, but with 54% uncertainty. A heavy ions irradiation will allow us to precisely determine the SEL threshold for SPACIROC2 and to draw the corresponding Weibull curve for this phenomenon.

4.4 Conclusions

Expertise from the SPACIROC2 design team allowed me to better understand the chip operation and to propose a monitoring strategy. The test bench proved to be suitable for recoding the ASIC parameters during irradiation. It also fits the requirements for the next generation of these MaPMT readout chips.

Along with the group, I had the opportunity of performing the very first characterisation of SPACIROC2 in radiation. The results obtained during the irradiation using a 200 MeV proton beam it was subsequently discussed with the OmegaMicro working group, special attention being given to the digital block of the chip. Planned to take data for 4-5 years in the hostile environment of Low Earth Orbit (LEO), the electronics on board of JEM-EUSO space observatory will be exposed to about 0.1 krad TID per year. Considering that the proton beam had a flux of about 1.089×10^9 particles / cm^2s , the annealing is expected to overcome the radiation induced effects for the much lower particle rates registered in LEO environment. Therefore, the SPACIROC2 chip proves to be a viable technological choice since it can withstand up to 60 krad TID. On the other hand, this prototype version of SPACIROC was found not to satisfy the radiation hardness requirements imposed by experiments at the LHC where doses and particle rates would exceed the levels tolerated by the chip.

The relative complex digital part of SPACIROC2 proved to be prone to radiation effects causing malfunction. This block of the chip will be carefully investigated in future tests, for instance the linearity of all four built-in DACs will be measured. Also, the DACs linearity curves saturation at the end of output voltage range it will be fixed by modifying the

external bias resistor. The SELs associated with high current states on the digital supply rail which was observed for two out of three tested chips it is an important cause of concern. We postulate that these latch-ups probably appear from disturbances of the electronic structures produced by heavier secondary (Si, Ge or metallic) ions generated. Significant contribution to the high current states could also come from SEU/MBU affecting the chip configuration registers. For upcoming radiation hardness tests, a procedure was developed to readback the configuration registers which would then reveal when corruption due to SEU/MBU occurs. Both assumptions will be investigated during irradiation of the SPACIROC2 chips in beams of various heavy ion species. Thus, for this proton irradiation test the computed SEL cross-section is $0.78 \cdot 10^{-12} \text{ cm}^2$ with 54% uncertainty. In the cosmic environment, such heavy ions have LET values ranging from 0.01 to 40 MeV·cm²/mg. On this occasion, the chip vulnerability to catastrophic SEE will be explored.

CHAPTER 5

Field Programmable Gate Array for High Energy Physic Experiments

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5. Field Programmable Gate Array for High Energy Physics experiments

The FPGAs built-in pre-existing logic can be rerouted based on user configuration to cover a wide range of application because of their high-density and inherent flexibility. State of the art programmable gate array devices have embedded blocks with digital signal processing (DSP) capability, besides a high amount of logic resources. All these features make the FPGAs very attractive for critical safety applications. Where the radiation background represents a constant threat to their reliability, thus the usage of FPGAs needs to be considered with care. Nowadays, these COTS devices are increasingly preferred in electronics for high energy physics accelerators and their experiments given the high processing power and the application short-lead time [355]. The FPGAs fills a critical niche by being more and more used compared to ASIC. On the electronics market, there are various technologic and architecture solutions for programmable gate array device such as: SRAM-based FPGA, Flash-based FPGA, antifuse based FPGA and ultimately MRAM-based FPGA.

From the configuration stand point, the FPGA devices can be divided in two broad classes as reconfigurable or one time programmable – such as anti-fuse based FPGA. The first category allows in-system or on the flight programmability. However, this great asset could be turned into a disadvantage when the configuration memory is corrupted by a SEU or MBU leading to modification of the user-defined circuitry. The scrubbing and error mitigation techniques continue to be developed to overcome this drawback [356-358].

Among all technologies, the antifuse based FPGAs are considered to be most stable in the presence of radiation, as they are less sensitive to SEUs, though they could be affected by cumulative effects like DD and large TID [359]. For this type the configuration fuses are one-time programmable, so that they remain latched even the device is not powered. Generally, the configuration memory cells have smaller sizes as well as being SEU immune when compared to other FPGA types [360]. Even so, antifuse FPGAs are predisposed to destructive SEE caused by heavy ions - like SEGR due to the relatively low antifuse rupture threshold [361]. In radiation, the main concern for this FPGA technology are SETs and SEUs occurring within the customizable user logic elements such as flip-flops and memory.

The Flash-based FPGAs have the configuration stored in nonvolatile flash memory cells which can be programmed in-system. This type of FPGAs has the configuration memory in general immune to SEU [382, 389]. As previously stated, the flash FPGAs are vulnerable to SET and SEU when it comes to user block memory and flip-flops. Unfortunately, these flash FPGAs withstand only to a much lower TID compared to the SRAM versions [362].

Allowing reconfiguration for unlimited number of times, the SRAM-based FPGAs possess in general a denser built-in logic circuitry compared to the rest. The static configuration memory cells are volatile and require an external memory element for loading the configuration bitstream whenever the device is powered up. Moreover, it is possible to do a partial reconfiguration of the configuration memory elements as often as it is needed. In contrast, the top performances of SRAM FPGA could give rise to various radiation-induced issues, due to common causes. First, a large amount of configuration memory is vulnerable to SEU leading to an undesirable device behaviour that translates in changes of the internal user defined circuitry like: activating unwanted logic elements, upsets in the FPGA logic resources might also generate spikes in the internal currents on the device. Apart from these, the user-defined logic resources are susceptible to SEE. However, mitigation and scrubbing solutions at the device or system level have been developed to successfully use SRAM FPGA in critical safety applications with relatively large TID and radiation fluxes [357, 363-367].

Novel Magnetic RAM-based FPGA is a promising FPGA technology alternative for the electronics meant to run in environments with radiation background [368]. A fundamental element to the MRAM cell is the nanostructure made of two ferromagnetic layers intertwined by an insulating layer forming the magnetic tunnel junction (MTJ) [369]. The MRAM cells benefit from both Flash-type and SRAM-type advantages in term of low power consumption, high speed, non-volatile characteristic, plus a quasi-infinite endurance [370].

Except the MRAM FPGA that is still at prototype level, the other three FPGA technologies are widely used in high-radiation environments. In the following we will present the work that has been done for the radiation hardness assessment of an SRAM-based FPGA from KINTEX-7 family. This study was carried out in the context of the RICH-LHCb sub-detectors upgrade program.

5.1 *KINTEX-7 FPGA under test*

The design of a newly RICH photodetection system envisages new digital boards for photodetection elementary cells which will be implemented around a commercial base-line solution like SRAM FPGA. As a backup alternative, the antifuse FPGA is being considered. The Xilinx 7 series devices are available in four state-of-the-art FPGA families implemented in a 28 nm high-k metal gate (HKMG) technology. The KINTEX-7 FPGA family was selected as an attractive solution for the digital board carefully considering the cost-performance balance and the inputs/outputs number which matches those of the read-out electronic system from the upgraded elementary cell. In terms of features, this FPGA family has a multitude of heterogeneous resources like: embedded Digital Processing (DSP) units with performance reaching up to 2800 GMAC/s; ADCs; up to 478000 logic cells; high-speed multigigabit transceivers (GTX) with transfer rates up to 12.5 Gb/s; dual port block RAM (BRAM) memory; multi-gigabit serial input/output links with 800 Gb/s peak bandwidth [371].

From this KINTEX-7 family the FPGA packed dice number XC7K70T-1FBG676C was selected to be used for the digital board design, while for the radiation hardness qualification tests the XC7K70T-1FBG484C6 version was selected, the latter being equivalent with the former except for the dice-packing. Also, both devices embed an identical amount of logic resources while they differ in the I/O number of pins. Although these two FPGA types are low-end in the KINTEX-7 family, they have nevertheless generous resources: 5125 configuration logic blocs (CLBs), 56.6 k of logic elements, almost 5 Mb BRAM and up to 300 I/O pins. Both are graded as “no space-grade” products - they have no radiation-hardened design which is reserved for space and military applications - and are delivered in a flipped-chip package without a metallic heat-sink.

Usually, the heavy ions irradiation facilities operate multiple monoenergetic ion beams with a penetration depth in range of few 100s μm , but this value decreases with ion atomic mass. To ensure the flipped active semiconductor layers of the dice are fully penetrated, 6 samples of XC7K70T-1FBG484C6 have been sent to HIREX Company for partial substrate removal and chip-thinning operation. Each FPGA flip-chip was mechanically polished down to about 60 μm and the thinned dice was mapped with a resolution of $\pm 0.1 \mu\text{m}$ in grid of 15x16 points. The thickness measurements were carried out with an IR interferometer. Apart from this mapping, the thinned dice surface was carefully investigated for any potential cracks that would indicate the device damage. Thinning results are presented in table 5-1 for each of 5 FPGA dices.

Table 5-1 FPGA flipped dice thinning results report

<i>Before</i>	<i>After thinning</i>
	
Sample 1	25.0 – 59.5 μm
Sample 2	34.0 – 58.8 μm
Sample 3	43.1 – 66.9 μm
Sample 4	22.0 – 50.1 μm
Sample 5	38.9 – 57.2 μm

This FPGA dice thinning was mandatory for the heavy ion irradiation, while for high energy proton irradiation the FPGAs used are usually in standard package. Otherwise, the accelerated heavy ions would not reach the active layers of the DUT, being stopped in the passive layer, hence the SEE testing would not be possible. In the LHCb detector environment the particles have an energy spectrum which generally exceeds the GeV level. At this energy level ions, proton or pions will pass through the entire standard package thickness and much more. Other issues emerging with the FPGA thinning include careful manipulation of the DUT and its test board during the entire usage. In this purpose, custom plastic lids were made with a 3D printer and they were used to protect the DUT dices while the devices are not in the beam, or are in storage, or are being transported.

5.2 Automatic test bench for irradiation

The radiation hardness assessment of an FPGA is a complex process considering its enhanced architecture, relative to the much simpler ICs, like ASICs. Its tolerance to radiation must be determined individually for each type of built-in logic resource. Any reliability issues caused by an FPGA logic vulnerability to radiation induced effects must be uncovered and estimated quantitatively. When exposed to radiation it is desirable that in the proximity of the FPGA to have semiconductor devices as few as possible, so that the radiation tolerance measurement results for DUT would not be affected. The radiation hardness qualification of the DUT will be done based on the recorded data during irradiation, and the results will be extrapolated to the LHCb detector radiation environment, given different TID and particle species.

With support and expertise from RICH Upgrade working group, I put forward the test bench architecture presented in figure 5-1. Thus, the testing procedure was worked out in close collaborating with the Cambridge LHCb Group. Since the KINTEX-7 FPGA must withstand the effects of a mixt-radiation field within the LHCb detector, the irradiation campaign envisages testing with different types of beams like protons, species of heavy ions, alpha particles or other light ions and X-Ray.

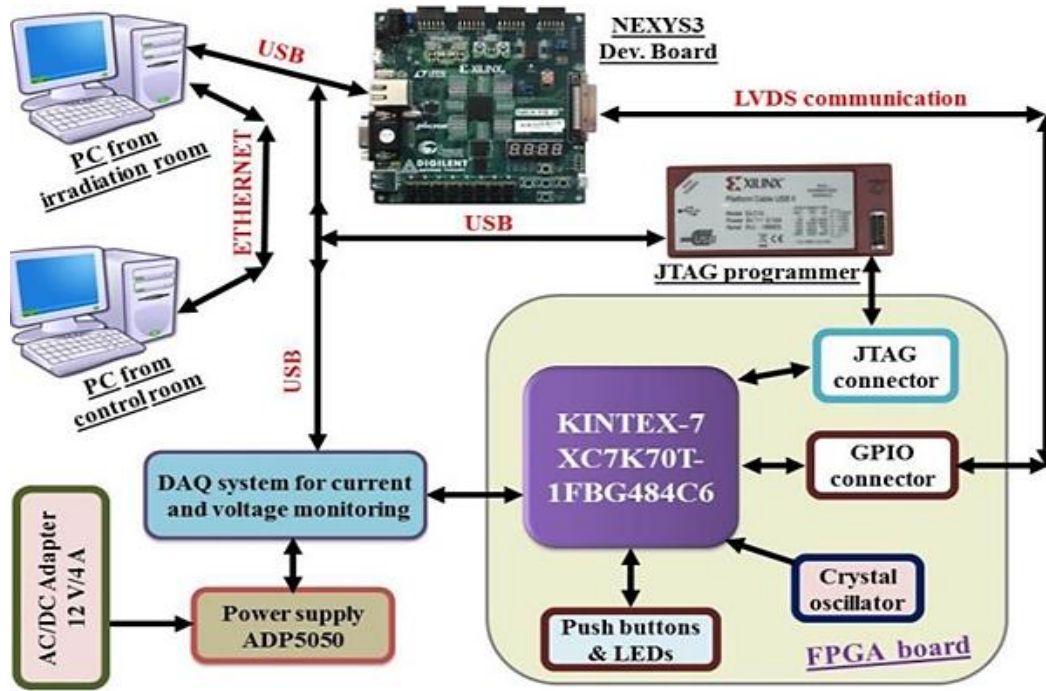


Figure 5-1 Test bench for a KINTEX-7 chip online monitoring under radiation [372].

The automatic test bench must accommodate all the demands associated with DUT irradiation, including testing in a vacuum enclosure. The test bench must deliver reliable data about the DUT operating parameters when it is exposed to radiation. Entire test architecture is developed around the KINTEX-7 chip which is mounted on the test board together with minimal chip-external electronic components such as: connectors, decoupling capacitors, crystal oscillator for system clock, push buttons and LEDs added just for a preliminary functionality test. These fulfil a set of minimal requirements for the FPGA basic operation.

The DUT reconfiguration is done through the standalone XILINX JTAG programmer connected over a ribbon cable at the FPGA board. The DUT power supply has four rails which are continuously monitored by the DAQ system as shown in figure 5-2. A commercial AC/DC adapter of 48 W is attached to the customised power supply board serving the FPGA test board. This is designed based on a ADP5050 integrated SMPS chip, see [373]. The supply rails from the power supply board pass through a DAQ system before connecting to the FPGA board. Feedback lines are foreseen for each of the FPGA supply rails. Any voltage drops across this supply screened cable multicore cable will be almost instantaneously compensated by the power supply board system. Further, the status of firmware written on the DUT is continuously checked with the help of a NEXYS3 development board housing a SPARTAN-6 FPGA. Screened ribbon cable is used for the LVDS (low-voltage differential signalling) data transfer between the commercial NEXYS3 board and the custom DUT board. All data are transmitted from NEXYS3, JTAG programmer and DAQ system to the host PC situated in the irradiation room, over USB links. Two LabVIEW GUIs have been developed to communicate with these devices and to gather the data in ASCII files for later analysis. The users will have access over Ethernet from a control room PC to the data gathered by the host PC.

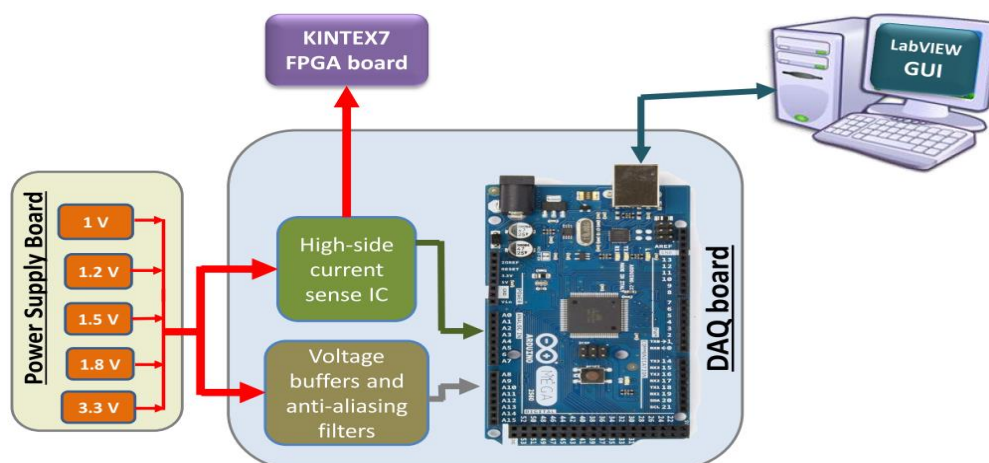


Figure 5-2 DAQ system architecture for DUT power consumption monitoring.

The following supply rails are connected to the DUT: 1 V for the FPGA core and BRAM; 1.5 V for I/O banks; 3.3 V required for FPGA JTAG block; 1.8 V for the high-performance I/O banks and for the configuration data storing elements. Any deviation in the DUT power consumption might be interpreted as a sign of radiation-induced effects, like SEL, which needs confirmation through various methods. Corroborating the FPGA power consumption with the FPGA configuration and the firmware status makes possible to distinguish among various effects that occur under irradiation. Monitoring the power consumption of the DUT is essential when the radiation could cause high-valued localized currents on the device that can lead to a thermal runaway.

The DAQ system architecture proposed and implemented is inherited from the MAROC3 test bench and onward adapted to fit the KINTEX-7 requirements. Its processing unit is a commercial baseline solution using the ArduinoMEGA development platform. A network of voltage buffers and anti-aliasing filters stops the sampling noise to overlap on the supply rails during current and voltage measurements. Built-in ADC of the processing unit digitises the voltages available at high-side current sense circuit outputs, plus those from supply rails. At every 50 ms the parameters are sampled and sent to the GUI running on the host PC where they are plotted and saved in an ASCII file. The power supply board used in conjunction with DAQ allows to cut-off the power supply of DUT and to perform a power cycling procedure whenever is needed.

5.2.1 Hardware part of the test bench

The FPGA under test has its test board schematics presented in Appendix D and the designed was made in compliance with radiation testing constrains. Besides the FPGA chip and the crystal oscillator for the system clock, there are no external semiconductor devices included on the DUT board. So, that the results from the radiation test would not be influenced by other semiconductor devices which are not radiation hardened. The capacitors and resistors populating the board ensure the minimal requirements for the FPGA to have at least a very basic operation mode. As in the digital board architecture for the RICH sub-detectors, an external flash memory was not used for storing the FPGA configuration - in other non-LHCb applications this memory stores the configuration even when the FPGA is not powered. The configuration bit stream is written via a JTAG interface to the FPGA whenever this is powered-on or needed by user. Our group designed entirely the test bench

schematic and did the PCB design. Figure 5-3 presents the 3D layout of a PCB and the test board assembled in the laboratory with a BGA rework station. Implemented in a commercial factory on 8 PCB layers, the FPGA board has 80x80 mm and it can be plugged in the SMPS board as a compact setup. During irradiation tests, the DUT will be powered through a 5 m shielded multicore copper cable. The LEDs and push buttons seen on the test board were only used to check preliminary the FPGA's functionality after a complete assembling. In total 9 KINTEX-7 test boards have been assembled by me, while 4 boards are implemented with a thinned FPGA dice.

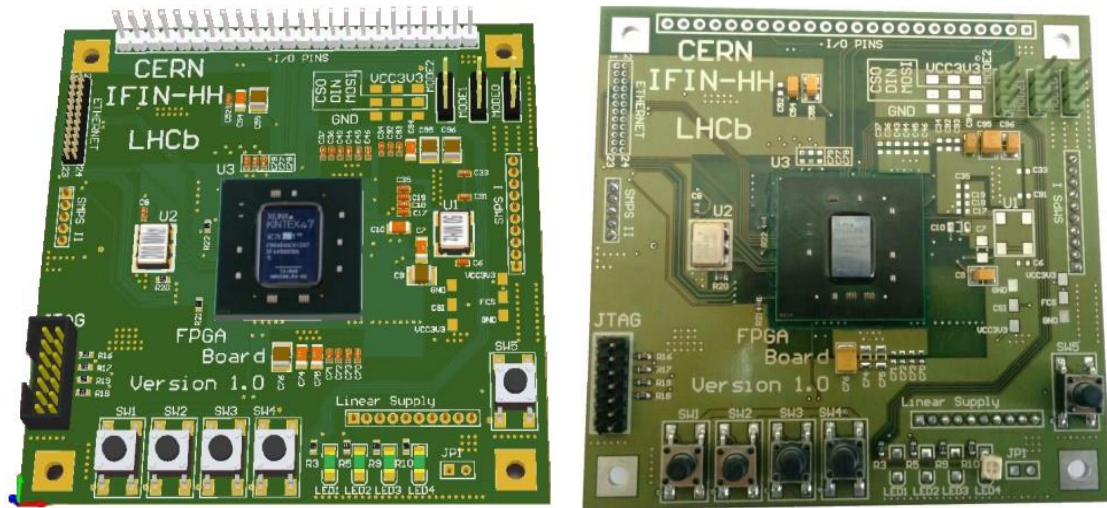


Figure 5-3 The 3D layout view of a PCB for the DUT on the left and the board fully assembled in the right side.

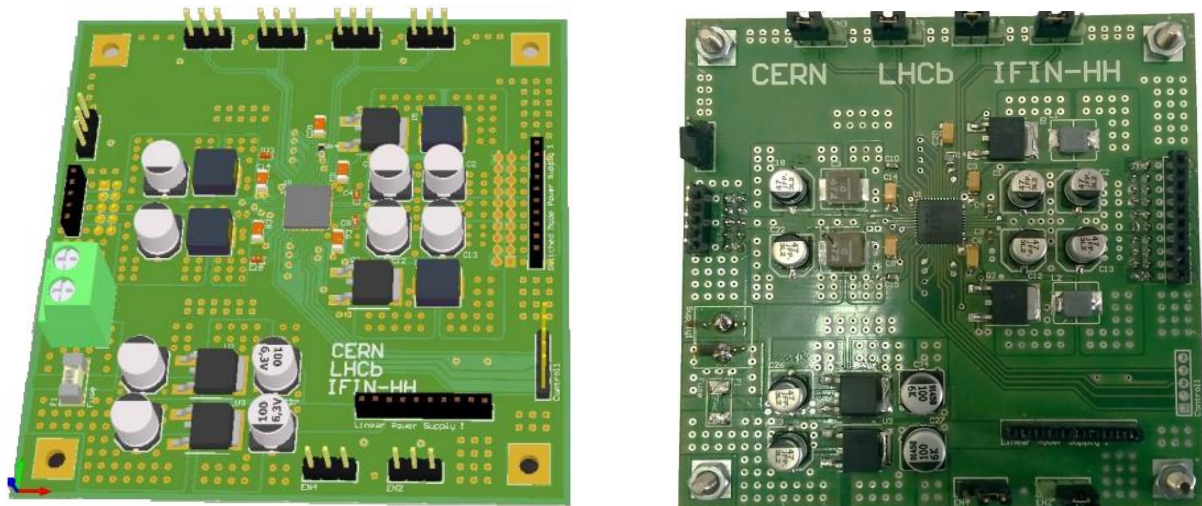


Figure 5-4 The power supply PCB layout in 3D view (left side) and its board fully assembled (right side).

The power supply for the DUT has been designed around the SMPS integrated circuit ADP5050 of the Analog Devices [401]. It is recommended as the most appropriate power supply solution for the KINTEX-7 family. The ADP5050 chip has the following features: wide input voltage ranges from 4.5 V to 15 V; $\pm 1.5\%$ output voltage accuracy over full temperature range; adjustable output voltage through I2C interface; overheat detection on junction temperature, five output voltage rails. The first two channels are programmable and drive up to 4 A current due to the sync buck regulators with low-side FET driver. Third and fourth

channel use also a sync buck regulator to provide currents up to 1.2 A. Channel five is a low drop regulator (LDO) providing 200 mA of current. Based on this chip our group designed the schematics available in Appendix E as well as the PCB and done their assembling “in house”. In figure 5-4 is presented the 3D layout of PCB, plus the practical implementation. As for FPGA test board, we kept the same dimension as for the power supply board, but in 4 PCB layers.

From design stage the output power delivered on the 4 rails by the ADP5050 chip was set through a network of feedback resistor to be: 1V and 3.5 A for the FPGA core plus BRAM; 1.5 V and 4 A for an I/O bank; 1.8 V and 1 A for the high-performance I/O; 3.3 V and 1A for third I/O bank plus JTAG block. The feedback point for each supply rail was attached to the other end of the screened multicore copper cable where the FPGA will be connected. In this way, we compensate any voltage drop across the 5 m length (or more) cable when sudden variations in current consumption occur in DUT. The power supply rail voltage values must be kept in a restricted range and should be very stable due to the FPGA’s complex internal architecture. In table 5-2 the accepted values are given for proper powering the KINTEX-7 chip. These values are provided by the Analog Device for the ADP5050 specification.

Table 5-2 The KINTEX-7 FPGA supplies voltage range provided by Analog Device

	Minimum	Nominal	Maximum
	voltage (V)		
FPGA core and BRAM	0.8	1	1.1
High performance I/O bank	1.14	1.5	3.46
IO bank supply at 1.8 V	1.14	1.7	3.46

Because the DUT will be powered over a long cable, our group made a setup to test each of the 6 power supply modules implemented. Therefore, it was check if their voltage outputs are in agreements with the values from table 5-2 while delivering only 75% of the nominal current value. Each of the three rails was connected through a 5 m cable to a calibrated active load system. On the case-package of the ADP5050 chip it was attached a temperature sensor with thermal paste. Further, the power consumption on supply rails has been monitored with a custom DAQ system implemented by the group, while system processing unit reads-out one wire digital temperature sensor [374]. The load on power rails was increased in steps to a value of 75% from the nominal value. Table 5-3 summarises the data gathered within ASCII file during a test.

Table 5-3 Linear fit values for KINTEX-7 FPGA supply voltages

	No. samples	Mean	Minimum	Median	Maximum
		voltage (V)			
FPGA core and BRAM	4081	0.95154	0.8013	0.9175	1.0337
High performance I/O bank	4081	1.43969	1.2415	1.4625	1.526
IO bank supply at 1.8V	4081	1.70182	1.5697	1.7165	1.7875

As it can be seen no values were detected which are outside of table 5-2's normal running ranges, even though the power supply board with the ADP5050 was loaded at 75% of its designed output power capability. A carefully analysis was carried on the FPGA core and BRAM rail data for all power supply modules implemented to be within a maximum/minimum rating. On the other hand, the FPGA under test does not have peripheral devices attached, so it will run with low power consumption. Anyway, the FPGA core power consumption will be the most significant contribution of all being closely correlated to the firmware choice and the implicit FPGA resource utilization. Here, radiation-induced high current states might increase the FPGA power consumption dramatically over at very short time span. Our tests proved that the power supply module can compensate high currents and the voltage drops across the long cables used.

Regarding the power dissipation on ADP5050 package, the chip data sheet states that it can run smoothly even at 75 °C without a thermal sink. Beyond this value the heat protection is activated triggering the chip to shut down. The data collected are given in the table 5-4 during the ADP5050 loading test.

Table 5-4 ADP5050 package temperature variation with the load level

Load	0%	10%	25%	50%	75%
Temperature (C ⁰)	27.37	29.06	32.75	37.25	48.81

Even if the power supply rails were loaded at 75% from the nominal value, the ADP5050 package is heated only up to a temperature of 48.81 C⁰ which is well below the maximum value recommended. Therefore, no thermal sink was or will be used for the SMPS chip.

I enclosed the entire setup used for the DUT monitoring in a metallic black box, see figure 5-5. The monitoring unit has on the front panel a few LEDs to indicate the status of: the power supply, the DAQ system and the Nexys3 development board. While on the back panel two D-sub 25 pins female connectors make available the output rails of the power supply module and the data I/O pins of the Nexys3 board. During irradiation tests, the monitoring unit will be placed 5 m away from the DUT and connected through another 5 m USB cable to the host PC.

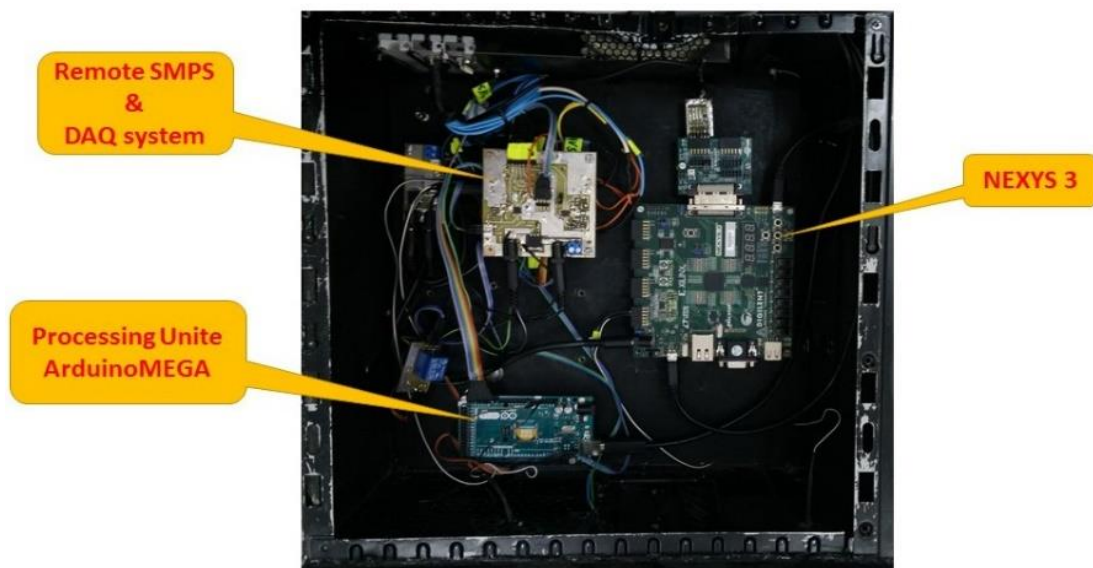


Figure 5-5 Monitoring and supply unit for KINTEX-7 FPGA under test.

The DAQ system has the voltage buffers and anti-aliasing filters plugged on top of the power supply board, while the processing unit with the ArduinoMEGA development kit is connected through a ribbon cable to the module. Regarding the circuitry of the voltage buffers and the anti-aliasing filters, it was inherited from the MAROC3 custom DAQ system.

5.2.2 Software part of the test bench

The processing unit of a DAQ system is controlled through a software routine written in C++. At every 50ms, data containing the power consumption values for each of the 4 FPGA supply rails are sent over a USB link to the host PC placed in the irradiation room. On these runs a GUI developed in LabVIEW handles the upcoming data and controls the power supply module state. In figure 5-6 is presented the interface that relies on a LabVIEW state machine, which saves data in ASCII files and it also plots the parameters variation on 4 graphs. It is implemented with various control buttons. The top left graph is used to display the power consumption of the core and BRAM memory, while the rest of the graphs indicate the power consumption variation on the diverse I/O banks. On the left side of the GUI are a few buttons that allow controlling the power supply for the DUT board and Nexys3 board, plus other functionalities associated to the data saving. In the GUI, the right side has features related to the SEL searches during testing. From there it is possible to set the upper limits on the current values which once exceeded increment a SEL counter and trigger automatically a DUT power cycling followed by a device configuration. The SEL testing menu makes use of several global variables from the second GUI interface.

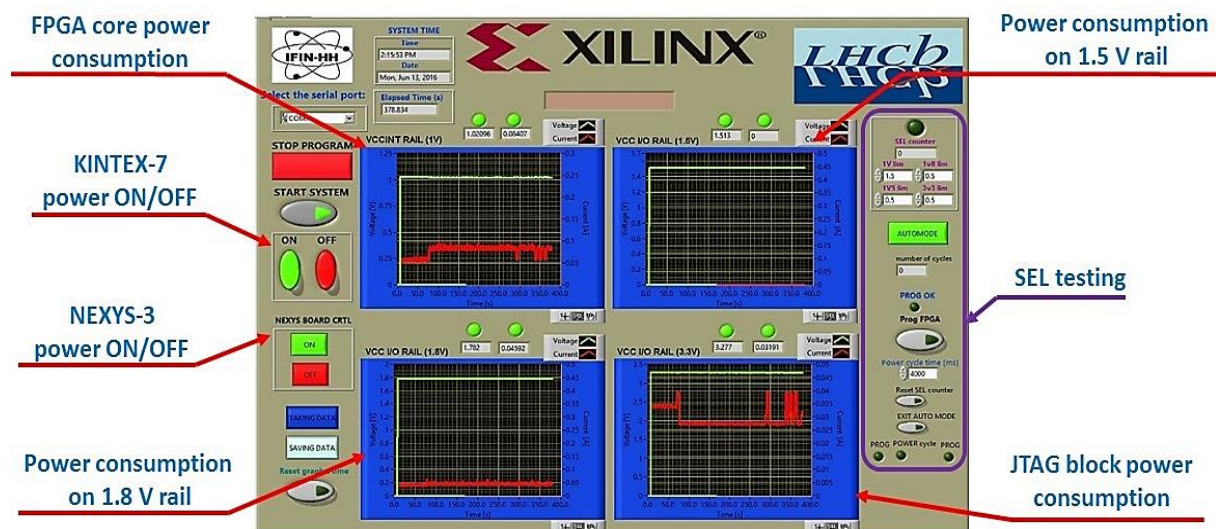


Figure 5-6 The GUI for the KINTEX-7 chip power consumption with online monitoring in real time.

Regarding the LabVIEW GUI presented in figure 5-7, here it is another state machine allowing the control of Nexys3, Xilinx JTAG programmer and Soft Error Mitigation (SEM) core instantiated on FPGA. As it can be seen, the LabVIEW GUI is divided in three sections. The left section is dedicated to the Nexys3 board. A known-pattern bit stream is sent to the firmware running on the Nexys3 board which in turn sends this pattern bit by bit to the KINTEX-7 input. The firmware running on KINTEX-7 circulates the bits through a chain of shift-registers. The output string is reinserted in the Nexys3 and compared with the reference. If those two mismatches, the error counters are incremented and the values plotted on the

graph. This test will allow during irradiation to check for SETs and certain SEUs in KINTEX-7 shift registers.

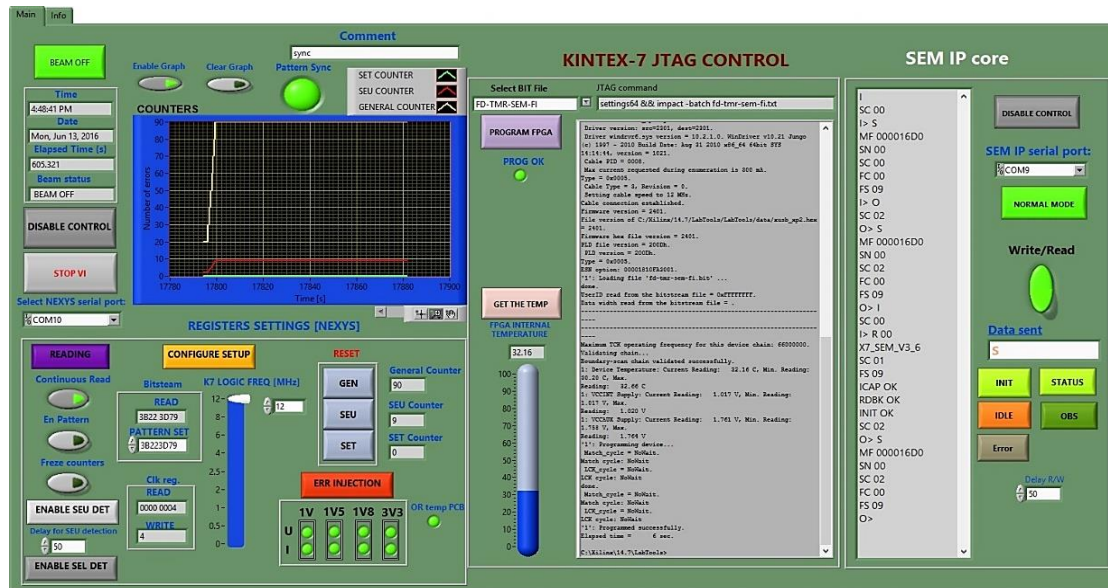


Figure 5-7 The DUT readout and control interface.

The central section of the LabVIEW GUI named “KINTEX-7 JTAG control” is used to configure the DUT using the list of firmware included in the attached menu. A text box is embedded to display the DUT configuration report at times when the device is reprogrammed or booted. The KINTEX-7 chip has a built-in thermal diode used to check the dice temperature and it is read out at the user’s request or after each re-programming procedure. Parts of the third subsection in this chapter, following next, are dedicated to the SEM IP core communication over the UART interface. This core is instantiated on the KINTEX-7 FPGA and reports any changes produced by the SEU phenomenon in the device configuration memory. More information about the SEM IP core will be presented later.

All data from this GUI are concatenated and saved within ASCII file. Also, the system time stamp is added, plus a flag for the beam state, if the beam was on or off. The state machine was implemented to handle all the incoming parameter values from both FPGA boards (DUT and Nexys3). The KINTEX-7 chip is automatically reprogrammed when the synchronization between the two FPGA boards is lost or when the SEM IP core tool crashes.

5.2.3 Firmware for FPGA evaluation in radiation

Investigating the radiation hardness of such complex devices as the SRAM based FPGAs relies heavily on the firmware. Thus, it is mandatory to quantify the rate of: SEU (Single Event Upset), SET (Single Event Transient) or SEFI (Single Event Function Interrupt) upsetting the FPGA logic fabric. As well it is important to pinpoint the potential vulnerability to the SEL which are triggered by particles with high LET. Therefore, the firmware architecture must be thought to cover and highlight all the types of SEE, except the destructive ones. Harmful TID and DD effects will be also investigated such as: degradation in the DUT performance manifested through the increasing in device power consumption, thus leakage currents, decreasing the retention capability of a built-in RAM memory or other aging effects.

From the beginning of the KINTEX-7 irradiation project, our group benefited from expertise of Dr. Stephen Wotton from the Cavendish Laboratory, University of Cambridge, affiliated to the LHCb experiment. Working under his supervision, at the Cavendish Laboratory and CERN, the visiting student Lukas Arnold from the “University of Applied Sciences and Arts Northwestern Switzerland”, implemented for us the first version of test firmware for the KINTEX-7 chip. Figure 5-8 presents the general architecture of the firmware meant to send data over a custom LVDS communication interface to the NEXYS3 FPGA readout board.

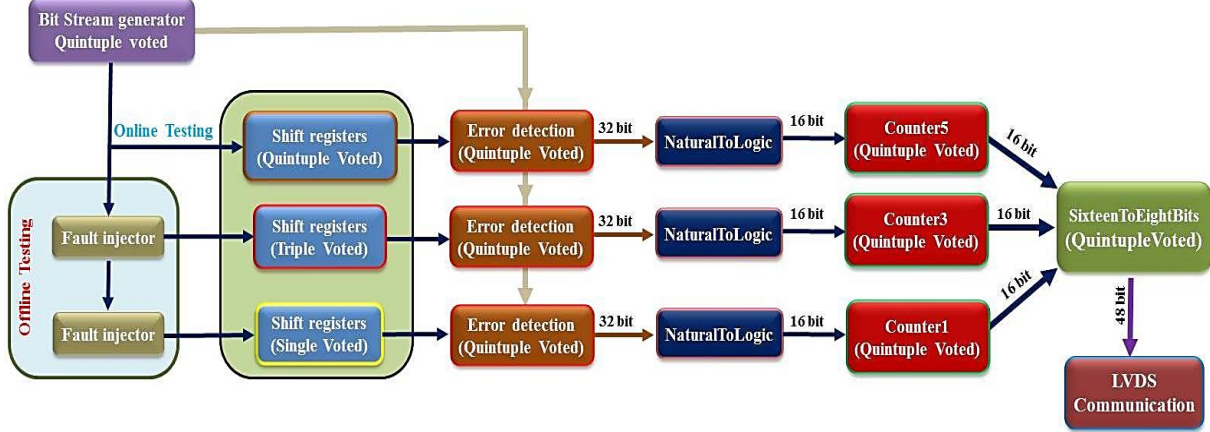


Figure 5-8 The first version of firmware layout for the DUT irradiation test without configuration memory scrubbing [372].

The main DUT logic resources tested in this version of firmware are the KINTEX-7 flip-flops. This firmware architecture was implemented to count the errors generated by specific events, such as SEUs or SET occurring in shift-registers chains implemented in single, triple and quintuple sub-chains with voting logic. Moreover, the efficiency of each type of voting logic will be evaluated in mitigating the radiation induced effects mentioned above. Such events are easily detected in large-dimension shift-register chains. At their input is injected a known bit stream pattern from the Bitstream generator logic bloc (also designed in quintuple voted redundancy scheme). Also, the Error Detection block will receive the same bit stream pattern, while the first input stream will have the bit string circulated through shift-register chains stacked with single or multiple redundancies.

The SEU phenomenon induces the bits flipping within memories, in registers and in other similar logic memory type structures. Furthermore, the SET event might be latched in sequential logic and generate a SEU. When these phenomena occur in the present architectures with shift-register chains, the error detection blocks should identify this by comparing their output with the output of the Bitstream generator. So, the counters will increment the number of errors detected on each single/multiple chain logic, while the incremented numbers of errors found are read by the NEXYS3 development board through the LVDS communication interface at every 4 ms. Other logic modules, like NaturalToLogic and SixteenToEightBits, are used to make the data string format to the communication interface requirements. Further over an USB link, the data readout by the NEXYS3 board is made available to the GUI which saves them in an ASCII file for later analysis. The firmware was implemented with a fault injector block to test the DUT offline, without irradiation, and to calibrate the system. At the user choice, a specific number of errors could be injected in the single and triple voted shift-register chain.

This version of firmware does not have embedded internal or external scrubbing or error mitigation solution for the FPGA configuration memory (CRAM). It is quite possible that accelerated beams of particles with high fluxes to compromise the CRAM before something

can be measured on the shift-registers chains. On the other hand, this allows us to see how the DUT behaves under radiation without having the CRAM being continuously checked and corrected through the configuration scrubbing.

Based on previous firmware architectures, our group adopted a straightforward solution to instantiate only those KINTEX-7 logic elements desired to be tested at a given time under radiation. Therefore, most of the blocks from the firmware architecture presented in figure 5-8 have been moved in to the NEXYS3 firmware. Hence, for the KINTEX-7 chip there have been developed a multitude of firmware versions that access a specific FPGA resource such as: flip-flops, SLR32 shift-registers, BRAM, CRAM, etc. Figure 5-9 shows the general architecture of a firmware for the FPGA test board within the irradiation test bench.

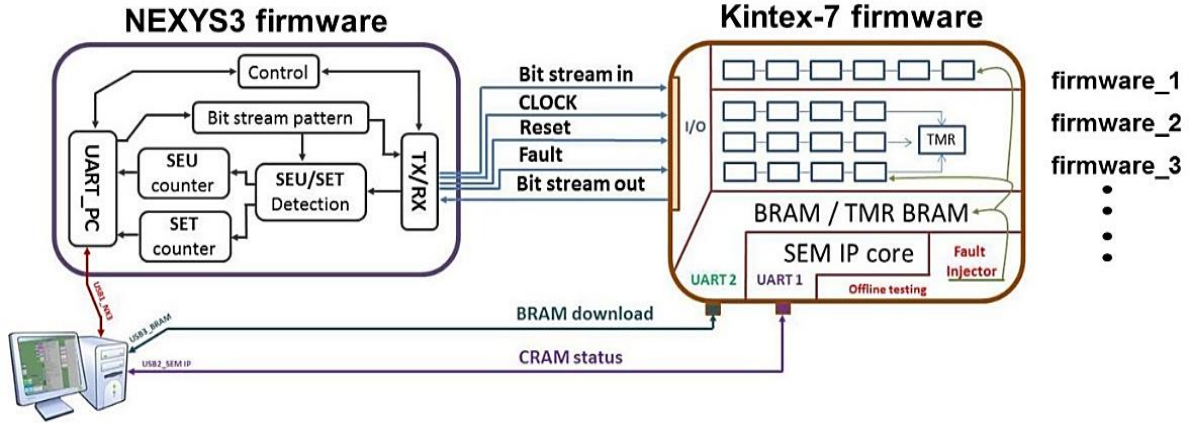


Figure 5-9 The firmware layouts for NEXUS3 and KINTEX-7 irradiation, including a SEM IP core for the CRAM’s scrubbing.

Evaluating the radiation tolerance of the flip-flops is crucial considering their indispensable use in implementing common sequential logic circuits, such as delay lines, counters, small memory buffers and state machines inside the FPGAs. Accounting this, dedicated versions of firmware have been implemented to measure radiation hardness of flip-flops inside the KINTEX-7 chip. As example, up to 40% of entire DUT’s flip-flops were connected in a long shift register chain receiving continuously a bit stream pattern and clock signal from the NEXYS3 board. The shift-register chain output is connected to the NEXYS3 board where the incoming bit streams are compared to the reference and if disagreement occurs, counters increments the values sent to the GUI which is running on the host PC. Depending on their error type, the errors detection block inside NEXYS3 classifies them as being SET or SEU. Improved firmware versions for testing the flip-flops have been implemented, many with a triple-modular-redundancy (TMR) solution mentioned in literature [403, 404]. In the same fashion, we have developed firmware versions to test the SLR32 resources found in the M slice of the KINTEX-7 chip. Single and TMR chains of shift-registers were implemented with an SLR32.

In total 4.86 Mb of BRAM are available in the DUT, and they could be utilised to perform traditional RAM functions [405]. This dense static memory is prone to radiation induced effects like SEUs or MBUs. To evaluate its radiation hardness a dedicated firmware has been developed for the KINTEX-7 FPGA, and it counts the upset rates when the device is exposed to radiation. The BRAM storage elements were instantiated on the device with a predefined pattern of bits. After each exposure to beam, the BRAM’s content is downloaded via an UART link to the host PC. The ASCII file generated at the end of this operation contains also the address of each bit string. After this, the data analysis is carried on using a Python script which compares the reference string of bits with those downloaded from the

DUT. At the end of the data processing it is known exactly how many bits are flipped and if there are clusters of bits changed within given pre-defined FPGA regions. Being the second large memory on the DUT, the BRAM can be used or not in the critical safety application.

In KINTEX-7 FPGA, the configuration memory (CRAM) is the largest memory which is embedded in the device [375]. Our DUT has in total 18884576 bits of CRAM used to customise the device logic function in the application by operation on the CLB units, which builds a “switching matrix” interconnecting and assigning pins for I/O blocks according to the user’s design. Considering the paramount dependence of FPGA running on CRAM, even a single bit flipped by radiation might have a severe and potentially very harmful effect on the device operation while in extreme cases could cause a failure in the entire system by burnout [376, 377]. The SEU occurrence in CRAM can lead to a mismatch in the FPGA logic fabric by changing the CLB function or switching the routing network topology [378-381]. Also, the I/O block operation may stop running in compliance to the firmware and the pins could change from input to output or vice versa. In addition slew rates of output signal could suffer significant changes [382].

Overall, for radiation-induced failures on the SRAM-based FPGAs mitigation solutions have been found and continue to be developed for improving FPGA reliability as key component of critical safety applications. Maintaining the CRAM integrity against the SEUs is essential for avoiding a wide range of radiation-induced malfunctions. This thing is usually done though CRAM configuration scrubbing and error mitigation [363, 367, 383, 384]. Practically, parts of the SRAM-based FPGA’s configuration memory can be partially or totally reconfigured for an unlimited number of times with a very fast pace [385, 386]. Existing alternatives either have additional electronics [387, 388] that read-out, check and rewrite the upset bits from the FPGA configuration memory. Other solutions are based on error mitigation core instantiated in the FPGA logic fabric [384].

On the digital boards of the Upgrade RICH detectors there will be no external flash memories to store the KINTEX-7 FPGAs configuration, so all the devices will be configured through a built in JTAG interface of GBT-SCA chips. Thus, the use of Soft Error Mitigation (SEM) Core from XILINX was considered as an internal scrubbing solution for the KINTEX-7 FPGA. The SEM IP core is free and a pre-verified solution to do internal scrubbing and error mitigation on CRAM [389]. This allows the SEU detection in the CRAM followed by a correction and error classification. Once instantiated within firmware design it can be configured to run in the next three modes:

- “repair” to correct just a single bit upset per CRAM frame without requiring an external flash memory;
- “enhanced-repair” for correcting two adjacent bits in the same frame, and as for previous mod it operates without any external memory;
- “replace” mode allows to overwrite entire frames from the CRAM by partially reprogramming the FPGA from an external flash memory containing the configuration bit string.

The FPGA configuration memory overwriting is possible through JTAG and SelectMAP interfaces, plus through the ICAP which is internally accessible. Thus, the SEM IP core uses ICAP primitive along with frame error correction (FRAM_ECC) and the readback cyclic redundancy check (CRC) to detect and restore bits affected by SEU. Moreover, the core can be put in an idle state and through its UART link or the SPI interface it allows injecting errors at specific CRAM bits addresses. So, the users have the possibility of simulating an SEU effect within implemented firmware in order to see how the device behaves. In terms of resource occupancy, the table 5-5 summarises the amount of logic resources required by the SEM IP core to run on DUT.

Other specification includes the core start-up latency, error detection latency and correction latency, but those depend on the FPGA system clock and resource occupancy by the firmware. Below in table 5-6 are listed the versions of firmware implemented to test the DUT under irradiation.

Table 5-5 The SEM IP core in repair mode and its resource occupancy on XC7K70T FPGA

	LUTs	Flip-flops	BRAM18	BRAM36
	number of logic elements			
DUT	41000	82000	270	135
SEM IP core	849	682	3	3

Table 5-6 Versions of firmware to access and test various logic resources during the radiation test

No	Versions of firmware for DUT
1.	Only SEM IP core configured in repair mode
2.	Shift-register chain with flip-flops (FF's) in single voted logic
3.	Shift-register chain with flip-flops (FF's) in single voted logic plus fault injector (FI)
4.	Shift-register chain with FF's in single voted logic plus SEM IP core
5.	Shift-register chain with FF's in TMR logic
6.	Shift-register chain with FF's in TMR logic plus fault injector FI block
7.	Shift-register chain with FF's in TMR logic plus SEM IP core
8.	Shift-register chain with SLR32 in single voted logic
9.	Shift-register chain with SLR32 in single voted logic plus FI block
10.	Shift-register chain with SLR32 in single voted logic plus SEM IP core
11.	Shift-register chain with SLR32 in TMR logic
12.	Shift-register chain with SLR32 in TMR logic plus FI block
13.	Shift-registers chain with SLR32 in TMR logic plus SEM IP core
14.	BRAM18 and BRAM32
15.	BRAM18 and BRAM32 plus SEM IP core

Foreseen to run on the KINTEX-7 FPGAs when these are mounted on the RICH front-end read-out digital boards, the final LHCb-RICH firmware will not exceed more than 50% or even lower usage for any of the device resources. Hence, the SEU cross-section per device is scalable with the SRAM-based FPGA resource occupancy. So, the evaluation firmware versions developed in the purpose of testing the DUT radiation tolerance will respect the upper limits of occupancy.

Previously mentioned, the firmware's embedding the SEM IP core has as collateral the benefit that it can allow the offline testing against the SEU without requiring additional complex hardware in order to purposely insert faults within CRAM. These offline tests may offer a good clue regarding the device behaviour when the CRAM bits are flipped by the SEU phenomena. On the other hand, it must be stated that SEM IP core does not access the bits of the device state or state registers, therefore it cannot mitigate the SEFI phenomena which is a SEU affecting the root of device.

I began the investigation of SEM IP core error correction and mitigation efficiency with offline tests using a relatively basic firmware on the DUT and by instantiating the core in repair mode. The firmware was implemented with the Vivado Design Suite software tool that also allows the generation of files filled with the design essential bits. Moreover, a script was developed to calculate the injection address of each essential bit based on the frame number, word number and position within the 32 bits of each word. Concerning the test bench for the data taking, we have used a setup almost identical with the one used for irradiation. The FPGA was powered over a 5 m screened cable and the DUT readout was done in the same manner through a multicore screened cable, while the programming of device was accomplished over a 1.5 m of cable using the XILINX JTAG programmer. All this setup was controlled with the help of LabVIEW GUI presented in figure 5-10 that has behind a LabVIEW state machine.



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parameters are saved also to an ASCII file with the system time stamp for each data entry. This is done for the recording containing the troublesome/un-correctable bit addresses.

The total number of essential bits extracted with Vivado for a firmware including only the SEM IP core in repair mode was 91118 bits, while the CRAM size has 18884576 bits for our DUT. For two weeks, the test bench had run continuously, and the errors have been injected one at the time. Thus, the core was turned to an idle state and the error was injected in CRAM. After the injection is confirmed the core is turned in observation mode where the error is identified, and the SEM IP tool tries to correct the flipped bit. Finally, based on the SEM IP report a decision is made either if the blind scrubbing is triggered or another error will be injected. Concerning the test report, it was found that 11 errors caused the built in JTAG controller to crash and almost 50% of the injected addresses were not correctable, which is understandable as the firmware include only the SEM IP core.

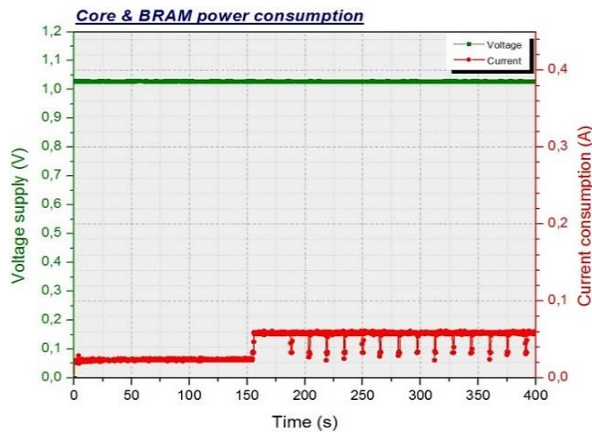


Figure 5-11 The DUT core current variation when blind scrubbing procedure is triggered - at 150 s the programming is finished.

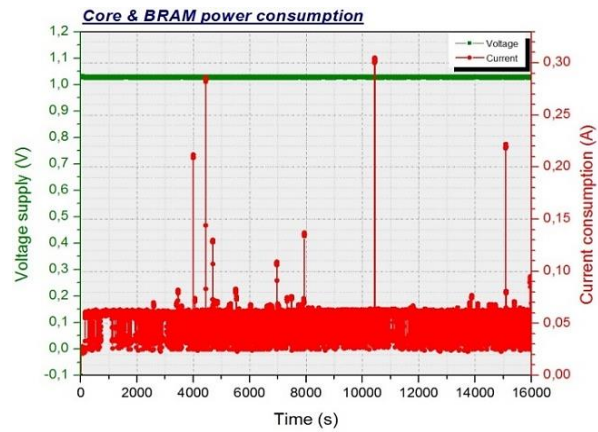


Figure 5-12 The DUT core current consumption for a much longer time spam.

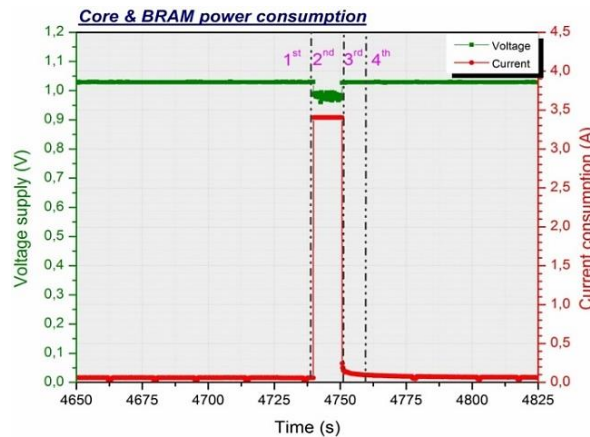


Figure 5-13 High current state in the DUT core during offline testing with SEM IP firmware.

A closer look to the power consumption of the DUT during offline test highlights that 26 errors caused the device power consumption to increase, by a FPGA core current sudden spike. Figure 5-11 presents the KINTEX-7 FPGA core and the BRAM power consumption at the beginning of online test. For 150 s the DUT has run without a loaded firmware, after this it was programmed, fact leading to the FPGA core current consumption increasing at 50 mA. The core current recorded value dips whenever the blind scrubbing procedure takes place, which leads to the CRAM being overwritten. If we look on at the larger time scale of the DUT

core current consumption within the offline test time span, as figure 5-12 presents, it can easily be spotted spikes with very large surges in the FPGA core current, that are several times higher in amplitude than the baseline value for the DUT core current of 50-60 mA.

These current spikes are caused by a corruption of the FPGA configuration memory in a few critical bits. A single bit flipped leads to a mismatch in the DUT logic resources, which enables a high current state very similar to some SEL effects found in literature but correctable by scrubbing. Beyond expectation, even severe cases of high current state for the FPGA core current consumption have been revealed by these simple tests. Figure 5-13 highlights such an event where on the FPGA core and the BRAM power consumption rails was measured a current flow value close to the maximum value of 3.5 A that the power modules are delivering.

As it can be seen, the DUT core current consumption was well behaved for the first interval of the graphic. At the first and second interval boundary takes place an error injection that instantaneously increases the current on the core supply rail up to almost 3.5 A. During the second interval spreading over 15.5 s the SEM IP goes from idle to observation mode and the error is corrected, so the flipped CRAM bit is put in its initial state. Between the second and the third interval the current rapidly decreases and a transitory current state is observed during the third graph interval. In the fourth interval, the FPGA recovers completely, except for a temperature effect. Clearly it could be seen that the power supply module compensated the sudden increase in power consumed during this event, as it was for the initial tests with active loads setup.

Keeping the CRAM integrity is mandatory considering the harmful effects that just one bit flipped can have, as permanent damage could be produced due for example to extreme temperature changes. Also, increasing the number of parameters being monitored - either electrical or the software ones for the DUT - is extremely helpful when the device is evaluated under irradiation. All this allows us to distinguish among the various SEE effects that might occur within a KINTEX-7 FPGA complex architecture. The other versions of firmware listed in table 5-6 have also been extensively tested in offline mode.

5.3 Heavy ions irradiation of KINTEX-7

Studies of the KINTEX-7 FPGA radiation hardness are carried out also by other research groups intending to use this family of devices in mainstream applications such as avionics, space experiments and large scale experiments in high-energy physics. A good study in this sense was made for the ATLAS Liquid Argon Calorimeter where a KINTEX 7K325 device is considered to be used [390]. In the literature, extensive studies on the XC7K325T-1FBG900C FPGA version can be found. Some were made with species of heavy ions to determine the susceptibility of various FPGA logic elements to SEE [391]. The XC7K325T FPGA was subjected to a proton irradiation with a 105 MeV energy, fluency 187.6×10^9 p/cm² and TID of 17 krad [392].

The KINTEX-7 FPGA should withstand within LHCb detector to a mixed-radiation environment broadly estimated up to 200 krad TID (Si), hadrons fluence 10^{12} /cm² with an energy spectra above 20 MeV, while the 1 MeV n_{eq} fluence is expected to be 10^{12} /cm² for almost 7000 h of LHC effective operation.

Our group took the task to evaluate the XC7K70T-1FBG484C6 radiation tolerance and to do a feasibility study concerning the device reliability within this harsh mixed-field radiation environment. We have started an irradiation campaign since 2015 for measuring the DUT radiation tolerance with protons and several species of heavy ions. The setup is presented in figure 5-14 and it can be used either for irradiation tests carried on with the beam extracted in

air or with the DUT placed in a vacuum vessel. Usually, the irradiation with heavy ions takes place in vacuum chambers where all the cables connected to the KINTEX-7 test board are foreseen with vacuum pass-through connectors.

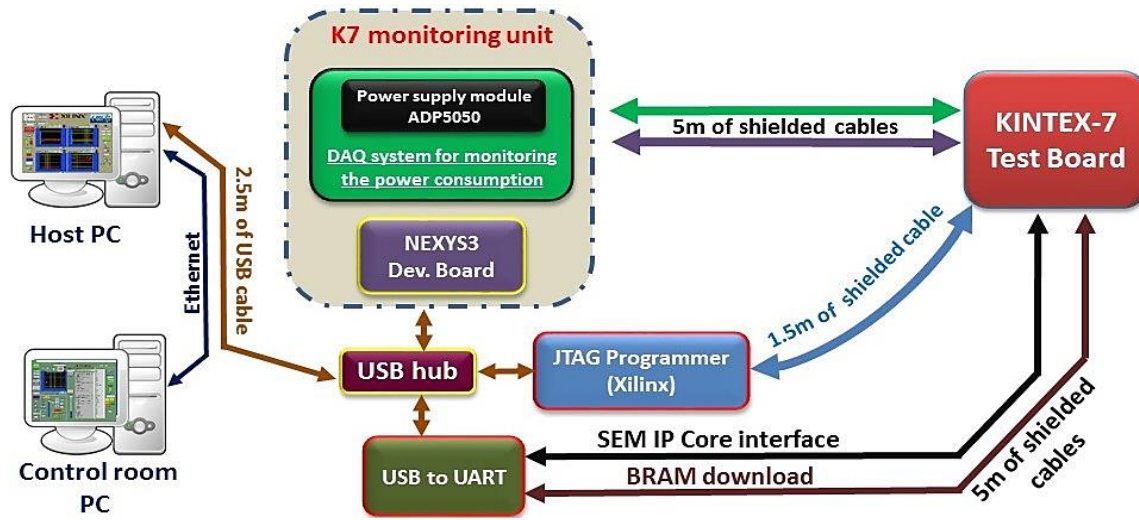


Figure 5-14 KINTEX-7 irradiation setup.

As it can be seen, all the electronics of the automatic test bench for the DUT monitoring is placed as far as possible from the beam, in general at 5 m away. Only the JTAG XILINX programmer adds some constraints being installed at 1.5 m from the FPGA. The main goal was to keep as short as possible the programming time of the DUT, because of the JTAG cable length, the DUT configuration is made at 12 MHz. All the hardware components of the test bench are connected to a USB hub, and further connected to the host PC over a 2.5 m of USB3.0 cable. This allows keeping all electronic equipment in a safe region of the irradiation room without influencing the measurement of the DUT radiation tolerance, especially for protons or neutrons beams. This setup should be drastically changed to allow radiation hardness tests in mixed radiation field like the one obtained by the CHARM facility at CERN, though this is planned in the second semester of 2017, hence for the moment we restrict ourselves to the case of direct DUT irradiation with particle beams.

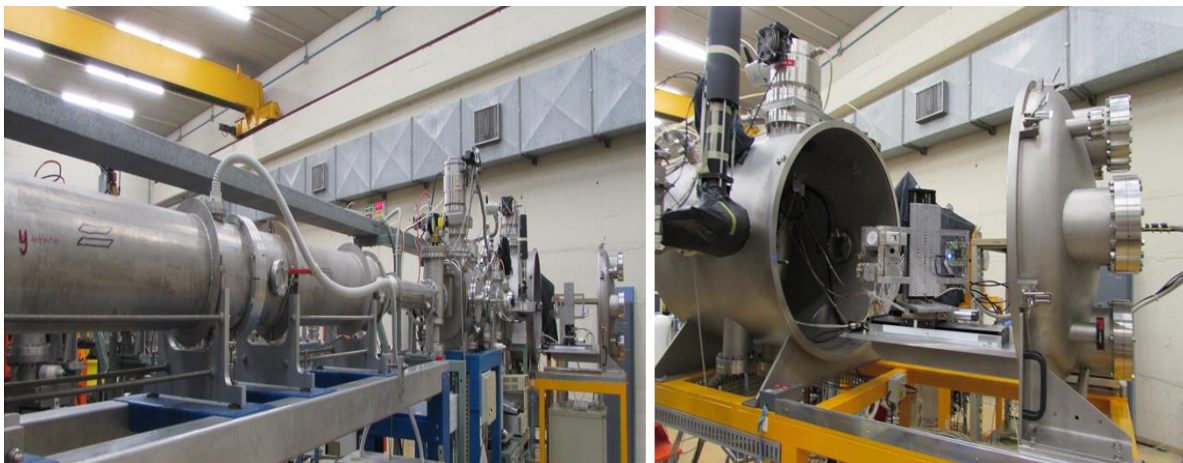


Figure 5-15 Legnaro Tandem-XTU accelerator beam pipe and the KINTEX-7 test board installed within the vacuum vessel.

The irradiation campaign on DUT has begun by accessing heavy ions irradiation facilities with the purpose of SEE testing. The first testing was undertaken at the SIRAD facility from INFN Legnaro National Laboratory, Padova, Italy [393-395]. The core machine of this irradiation facility is a 15 MeV Tandem-XTU electrostatic Van de Graaff accelerator providing a beam for studying both SEE and the cumulative radiation induced effects [396]. For this heavy-ion irradiation facility there are available a wide variety of ion species with a LET value spanning from 0.02 MeV cm²/mg and 4390 µm penetration depth to 81.7 MeV cm²/mg and 23.4 µm range in silicon [397]. Figure 5-15 presents the irradiation room at SIRAD with the beam line and vacuum vessel in open position giving access to the sample holder.

The DUT was installed on the metallic frame of the sample holder which can be controlled to move up or down and rotate $\pm 80^\circ$ on a vertical axis with a precision of 1° [397]. A laser system allows the DUT dice to be aligned on the beam. In our case the system position coordinates have been saved for 0° , 15° , 30° , 45° and 60° , the test board tilt angle with respect to the beam longitudinal axis. Inside the vacuum vessel there is a remote-control shutter and a system with Si diodes for beam profiling. The shutter has 330 ms switching time and it is operated from a control room to stop the beam in front of the DUT. The flux of ions in beam can be modified between 10^5 and 5×10^8 ions/cm²/s. After the setup installation and after its functionality is checked, the enclosure is latched and the turbomolecular pumps ensure a vacuum level of 10^{-5} mbar. This operation is followed by a beam profiling and if everything is fine then the test board is scrolled back in its irradiation position.

The second irradiation test was made possible through a AIDA2020 EU program, carried out at the Cyclotron Resource Center in Louvain-la-Neuve, Universite Catholique de Louvain Belgium (UCL) [398, 399]. From research infrastructure stand point, the UCL has a facility that allow heavy ions beam testing, light ions tests and neutron irradiations. The Heavy Ion Irradiation Facility (HIF) makes available a wide variety of ion species with LET ranging from 0.4 to 56 MeV cm²/mg and this only for the high penetration cocktail beam. In the purpose of SEE testing two heavy ion cocktails can be used either a high LET or a high penetration one [400]. Concerning the beam, it has a maximum diameter of 25 mm, and $\pm 10\%$ homogeneity, while the flux can be modified from a few ions/ cm²s to about 10^5 ions/cm²s. The beam profiling is made with a Passivated Implanted Planar Silicon (PIPS) detector. Irradiations take place in a cylindrical vacuum chamber that has the metallic sample holder actuated by electrical motors in x-y directions and it allows a tilt the probes at various angles.

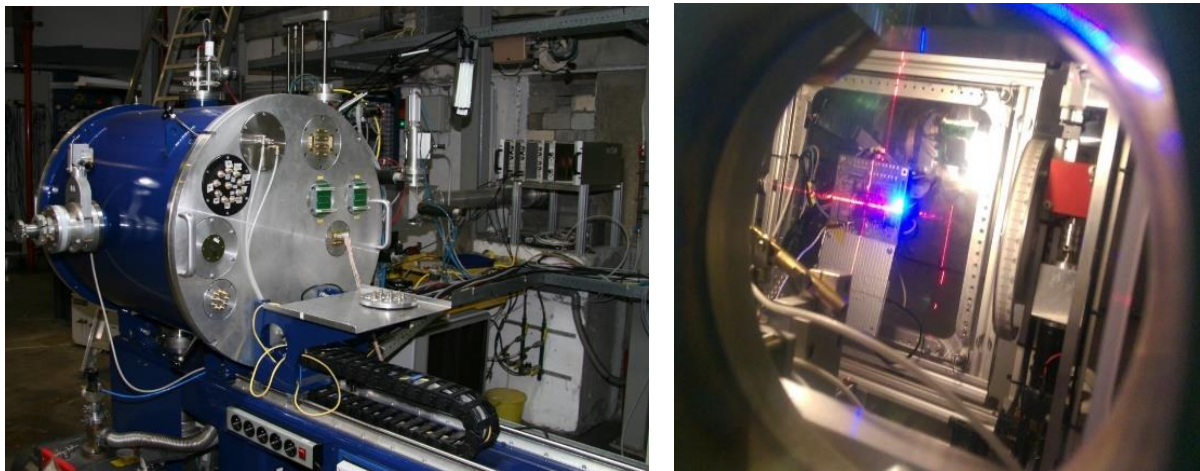


Figure 5-16 The HIF vacuum chamber in close position and the inside view during laser alignment of the DUT.

Laser alignment is assisted by a video camera used to place the DUT in front of the beam. Figure 5-16 presents the irradiation chambers plus the KINTEX-7 test board mounted on the sample holder and seen through a transparent aperture on the vessel metallic body.

Because the radiation background is very low near the vacuum chamber, the ion testing procedure of the DUT was done with the team in the irradiation room, hence only the host PC was used. As previously shown, once the alignment procedure ended the vacuum pump was turned on till the nominal pressure condition for heavy ion beam has been met.

5.3.1 Data analysis and interpretation

LNL tests with ions at SIRAD facility

The aim of the first irradiation test performed at SIRAD was to inquire how harmful are the effects induced by radiation on the FPGA when its CRAM has no scrubbing and error mitigation. For testing we have used only the firmware from figure 5-8 where shift-register chains are in a single, triple and quintuple voted logic. Two types of ions have been used during irradiation Oxygen ^{18}O at 108 MeV with the LET 3.197 MeV cm²/mg (TRIM estimate) and Florine ^{19}F at 122 MeV with the LET 3.67 MeV cm²/mg (LNL estimation for surface) or 3.899 MeV cm²/mg (TRIM estimate is given for bulk). The firmware was set to occupy just 40% of the FPGA logic resources. Once the vessel was closed, the vacuum pump was turned on and the online monitoring begun.

The power consumption of the FPGA core and the BRAM memory before the irradiation is presented in figure 5-17. In the plot of the first section the current consumption is around 25 mA and raised up to about 70 mA in the second section, where the FPGA is configured.

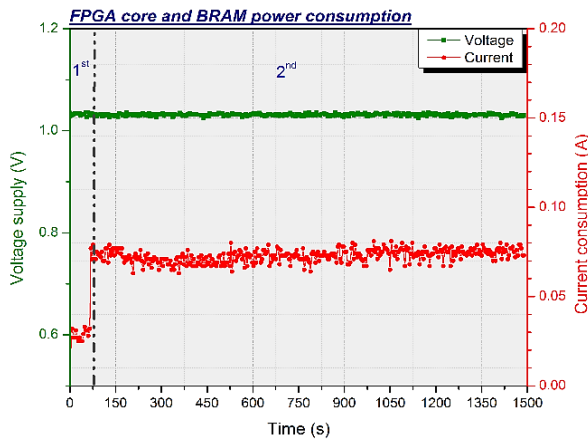


Figure 5-17 FPGA core and BRAM power consumption before irradiation.

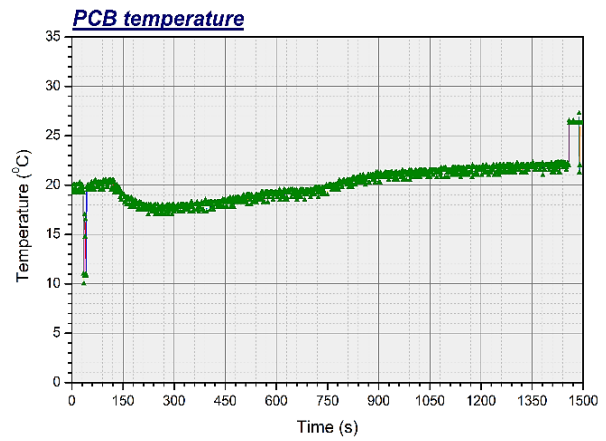


Figure 5-18 Vacuum vessel temperature before irradiation.

Further, the power consumption remained stable on all DUT supply rails. On the bottom layer of the FPGA board, right behind the dice, a K type thermocouple was attached to record the temperature inside the irradiation vacuum vessel. The recorded values are showed in figure 5-18. A rising trend in the temperature curve with time is observed, which is expected due to the poor heat dissipation in vacuum. The narrow peaks and dips on the curve occur due to the vacuum pump operation.

The DUT proved to be stable during the pump activation as the vacuum level was reaching the nominal pressure level for irradiation procedure to be carried out. Initially the

heavy ion beam flux was varied in a wide range. During this, it was observed that the configuration was failing rapidly in less than a few seconds even at low beam flux. Though this was expected to happen, it was not expected to be as quickly as measured. Irradiation with Oxygen and Fluorine ions at high beam fluxes highlighted a strong variation of the currents measured on the power rail which supplies the FPGA core and the BRAM. As example, one of the tests performed under a ^{18}O ion beam showed that the current increases gradually because of the accumulation of SEUs in the CRAM. So, unwanted and parasitic logic elements within the FPGA were introduced by the CRAM corruption. Figure 5-19 presents the current consumption of the FPGA core and its evolution during this test. Initially the FPGA is not configured, the first interval, after which the current consumption is raised to 55 mA in the second interval where the firmware was loaded and activated on the device. The third interval showed a continuous rising trend in the consumed current.

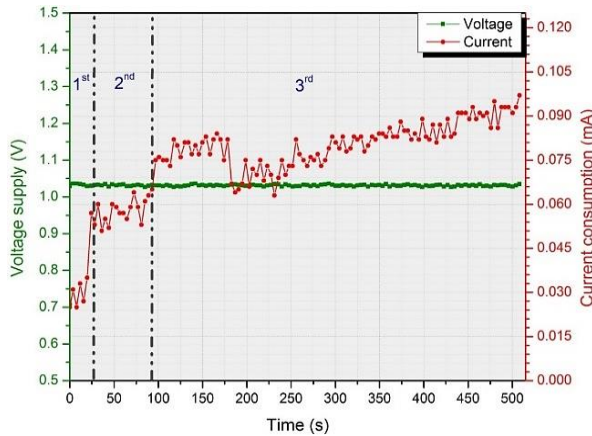


Figure 5-19 FPGA core and BRAM power consumption under irradiation, ^{18}O ions.

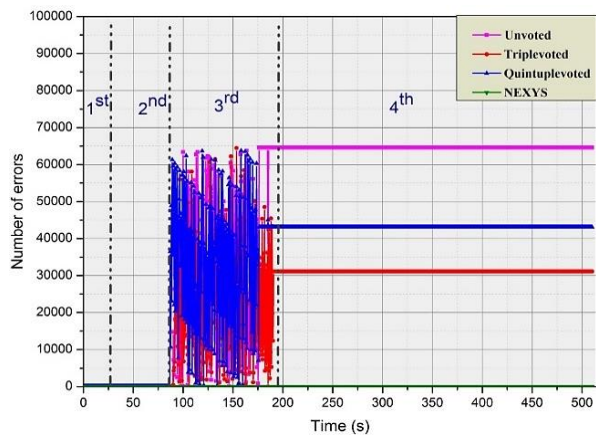


Figure 5-20 Number of errors incremented by ^{18}O ions upon shift-registers chains, qualitative argument only, as the y-axis is scaled arbitrary due to a bug in counters.

On the other hand, figure 5-20 shows the number of errors recorded for this test. Thus, in first interval the DUT was unconfigured, while in the second the firmware is written and the beam is on for a few seconds, but no errors were recorded for this brief period as the logic was being loaded. The third region outlines a high number of errors caused by SEUs or SETs in all the three shift-registers types, quite possible induced by the CRAM corruption which dominates the shift-register failures – reasoning considering that quintuple, triple and single voted decisions are equally probable to fail. After the current started to rise continuously, the error counters have frozen, becoming clearly that CRAM was severely compromised, so the configuration and the logic had failed. Multiple tests were carried out using the oxygen beam for different shift-register chains and logic size which proved the DUT's vulnerability to radiation, the measurements showing large SEU rates even at relatively low LET value.

Switching to the Fluorine beam with a slightly higher LET than Oxygen, it was observed for large fluxes the emergence of severe high current states induced on the FPGA core plus the BRAM system. Also, behaviour typically of SEFI phenomena was observed on the DUT. Figure 5-21 presents how the FPGA core and the BRAM current consumption doubles in less than 15 seconds and decreases quickly to the level were the device is unprogrammed. This time the firmware occupancy was close to 100%. If we look at the evolution of error number plotted in figure 5-22, it is obvious that the LVDS communication is lost close to 140 seconds of device running, when there is observed also a current variation

or dip, see figure 5.21. In this time, no information from the DUT firmware could be readout by the NEXY3. Therefore, the CRAM was badly affected by the accumulated SEUs. Also, the values incremented by the error counters are qualitative, as a bug was found for these first firmware versions.

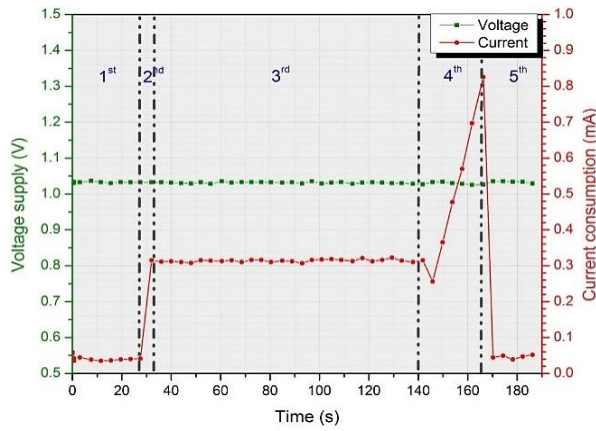


Figure 5-21 DUT unknown state revealed by a core current under ^{19}F ions action, SEFI.

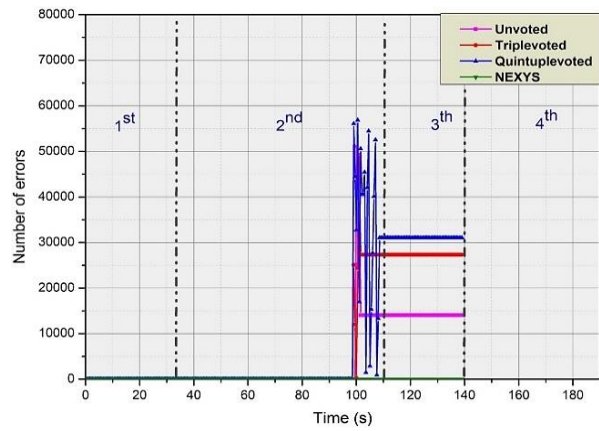


Figure 5-22 Number of errors incremented erratically till communication was lost.

Maintaining the same test condition as previously, the DUT was exposed a longer period to a ^{19}F ion beam and for several times was recorded the high current state time dependence presented in figure 5-23. After a short period of smooth running, see second graph interval, the CRAM is compromised by large accumulation of SEUs and the logic blocks inside the FPGA start to be turned on with almost constant rate.

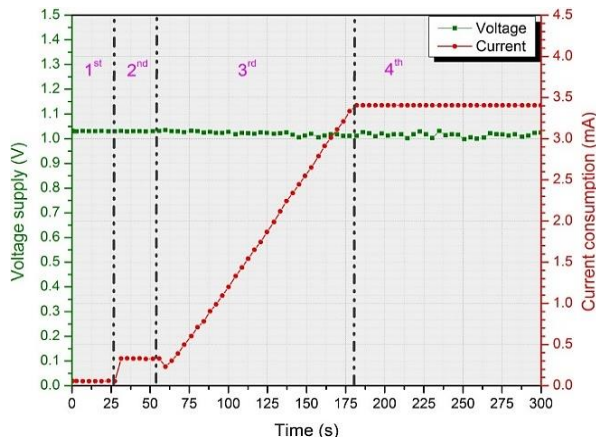


Figure 5-23 High current state on core and BRAM supply rail during a ^{19}F ions test, run away SEU accumulation.

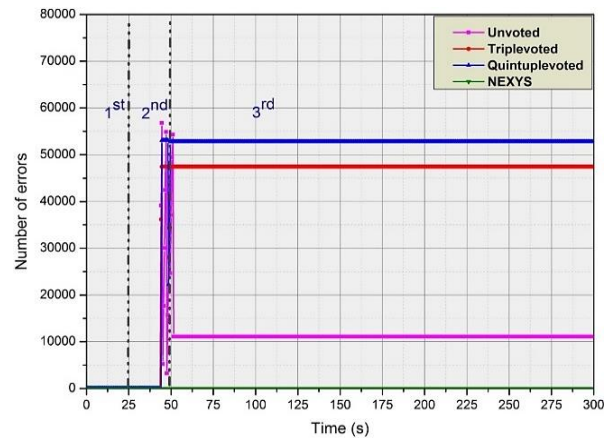


Figure 5-24 Number of errors incremented under a high current state.

The third interval shows how the core current increases gradually on an almost constant slope till it reaches a plateau in the fourth interval. Practically the current flow on the FPGA core and the BRAM power rails reached 3.5 A which is the maximum value delivered by the power supply module. The temperature on the DUT dice exceeded 75°C at which moment the power supply was cut-off. In the subsequent beam-off tests, no permanent damages were identified on the device, but this behaviour may lead to the FPGA thermal runaway if that high current state acted longer. It was possible to readout the errors number only in the second

interval of the graph presented in figure 5-24 while the firmware CRAM was not corrupted beyond use, and some degree of communication through the shift-register chains was still possible. After enough SEU were induced in CRAM, the counters were frozen to a fix value as the voter logic fails, so no trustworthy data was readout beyond this point.

The irradiation tests carried out at SIRAD facility have revealed the KINTEX-7 vulnerability to heavy ions even at low LET. Given that was a complete lack of CRAM scrubbing and error mitigation that could prevent the SEU effect, it is difficult to conclude only after this test at LNL, more testing being required. No clear sign of SEL was observed during the tests, only high current states induced by the CRAM failure by the SEUs were observed.

To measure the logic-failure induced by certain SEUs, the FPGA occupancy was kept below 2% for a relevant test while the beam flux was set to 100 ions per cm^2 per second. That allowed us to observe when the bit pattern was corrupted first time or when the FPGA configuration has failed (the two are impossible to separate for the firmware used at SIRAD). Figure 5-25 presents the SEU cross-section on logic-failure. Those values are computed per device versus LET. Compared with the results for the XC7K325T-1FBG900C chip available in literature [423], the SEU cross-section value measured for our DUT is given per device and not per bit.

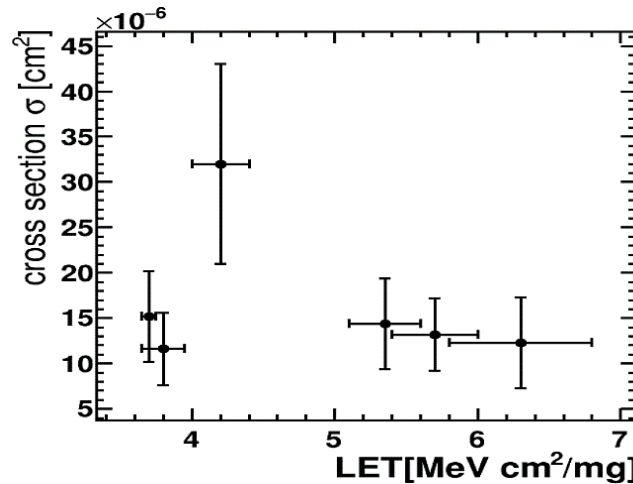


Figure 5-25 The SEU cross section for logic-failure measured at SIRAD.

Anyway, this value for the SEU cross-section might be considerably lower when the CRAM will be protected by a SEM IP core, as the logic might recover in the latter case. So, the CRAM failure will have less impact on the cross-section for non-recoverable logic failure events. The versions of firmware listed in table 5-6 will certainly allow a better DUT evaluation under irradiation.

Ion beam tests in Louvain at HIF facility

The KINTEX-7 radiation hardness assessment pursued at HIF focuses among other objectives on finding the threshold for the SEL. The devices considered in the RICH Upgrade Program are rejected if the SEL phenomenon is experienced for a LET threshold below 10 $\text{MeV cm}^2/\text{mg}$. This is about the LET of Silicon ions produced in elastic collision for light hadrons with lattice nuclei. The first test performed at this facility aimed also to confirm the FPGA core current increasing trend in slope induced by the multiple SEUs occurrence in CRAM. For this purpose, the DUT was programmed with a firmware consisting of flip-flops single voted shift-register chain without a SEM IP core. The FPGA resource occupancy was

set at 40% and the test board was not tilted with respect to the beam's longitudinal axis, while the ion beam had the following parameters: flux 10^4 ions/cm²/s, energy 238 MeV, ion species $^{22}\text{Ne}^{7+}$, LET 3.3 MeV cm²/mg. After a cumulated fluency of 1.43×10^7 ions/cm² on the DUT, its core current consumption increases three times and each time with the same slope. As it can be seen in figure 5-26, the core current recovers every time after the blind scrubbing procedure is triggered. The temperature measured by the FPGA built-in thermal diode was constantly around 30 °C while the test board was in the vacuum vessel without the device being irradiated. Figure 5-27 presents the temperature changes induced by these three current peaks arising in the FPGA core.

Like in the offline tests with the SEM IP in the laboratory, a similar core current step variation, due to a single flipped bit in the CRAM, was observed during a test with $^{40}\text{Ar}^{+12}$ ions, while the accumulated fluency on the device was 1.13×10^6 ions/cm². The DUT was configured with a firmware based on a simple TMR flip-flop shift-register chain plus the SEM IP core, and the board was tilted with 50° towards beam.

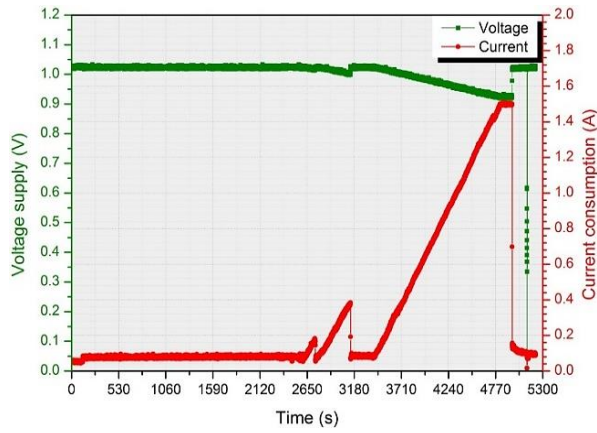


Figure 5-26 High current state induced in the FPGA core fore firmware without CRAM scrubbing.

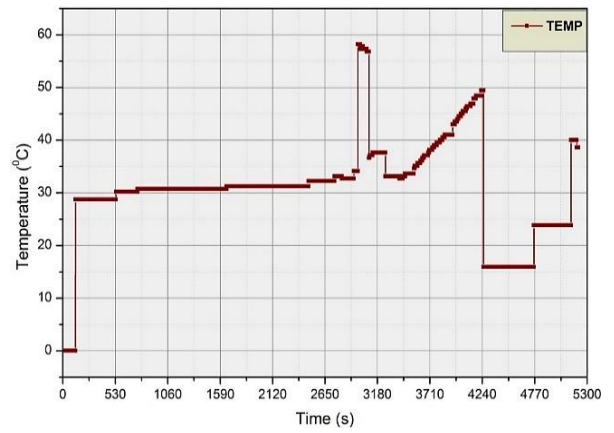


Figure 5-27 FPGA dice temperature during irradiation with $^{22}\text{Ne}^{7+}$ ions.

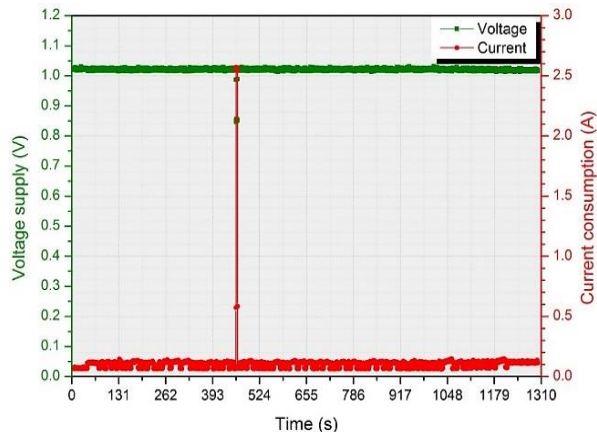


Figure 5-28 Core current increasing in steps as SEU occurred in CRAM.

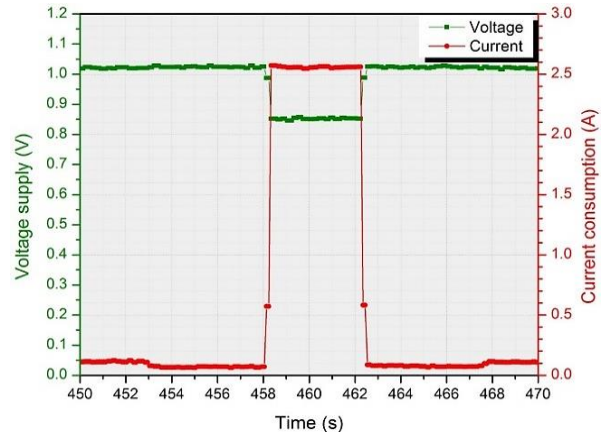


Figure 5-29 Zoom on time axis for the core current step increasing event.

The FPGA occupancy was kept at 40% and the beam parameters were: flux 10^3 ions/cm²/s, energy 379 MeV, LET 15.56 MeV cm²/mg. Figure 5-28 shows how the DUT current consumption has short current spike exceeding 2.5 A. Since the device recovered without blind scrubbing or power cycling, just with SEM IP core running, this event pointed

out a mismatch in the FPGA logic fabric due to the SEU affecting the CRAM. As it can be seen in figure 5-29 the high current step event lasted less than 5 s. Corroborating the data reported by the SEM IP core with the core current evolution and jump's time stamp, we have determined that the event was certainly a SEU in CRAM.

Keeping the same testing conditions, except for SEM IP which was set to “ENHANCED repair”, it was recorded a current jump with a signature corresponding to the micro latch-up events and the current was detected on 1.8V power rail as in literature. Cumulated fluency on DUT was $7.56 \cdot 10^5$ ions/cm². Figure 5-30 presents a current increasing in steps of approximately 100 mA, modifications which are not removable through a configuration scrubbing or blind scrubbing, but only by power cycling the device. The plots below highlight two power cycles applied, followed by device recovery. The Core and BRAM current consumption emphasize on figure 5-31 multiple dips and spikes associated to blind scrubbing when the error mitigation capability of the SEM IP core was offset by the large SEU rate and the logic was failing.

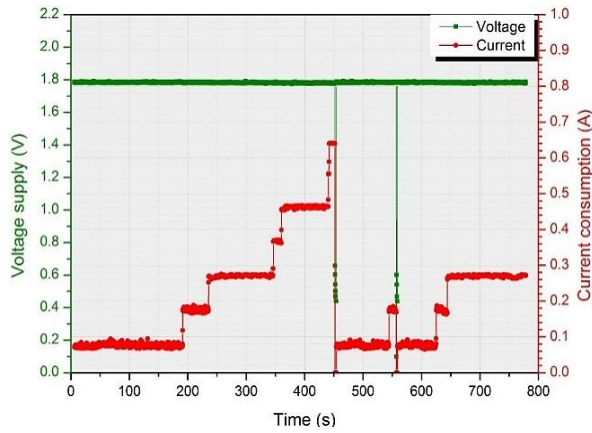


Figure 5-30 SEL induced by ions with a LET of 15.56 MeV cm²/mg in a 1.8 V power rail.

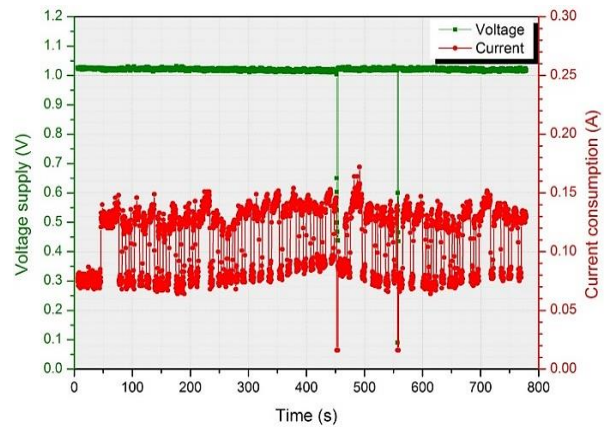


Figure 5-31 Core and BRAM current consumption under ⁴⁰Ar¹²⁺ ion irradiation.

Similar behaviour is described also in literature for another FPGA from the KINTEX-7 family [391]. It is argued that those current steps seen on the 1.8 V power rail did not represent a clear sign of a SEL since they disappear when the voltage is lowered to 1.2 V. However, from the RICH application standpoint. This event is considered a SEL because it requires a power cycling to be mitigated.

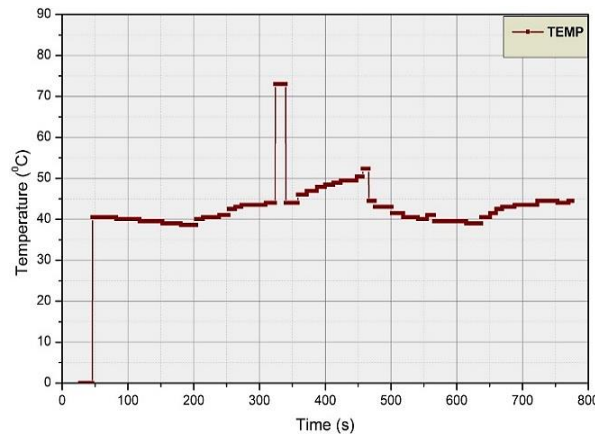


Figure 5-32 The DUT dice temperature during irradiation with ⁴⁰Ar¹²⁺.

Also, the need for a power cycle when the consumption rises following a SEL is determined by the increasing dice temperature as in figure 5-32. Hence, a considerable thermal stress on the device could occur and it is problematic especially when the irradiation takes place in vacuum as in test conditions with ion beams.

We continue to investigate the KINTEX-7 susceptibility to SEL using species of ions with a higher LET. Therefore, the next test was done using $^{58}\text{Ni}^{18+}$ ions at 582 MeV and LET of $20.4 \text{ MeV cm}^2/\text{mg}$. The beam flux was at $10^3 \text{ ions/cm}^2/\text{s}$, while the accumulated fluency on device was 1.06 times 10^6 ions/cm^2 . Concerning the firmware version, we have used the TMR flip-flop shift-register chain and the SEM IP core in repair mode, while the device occupancy remains at 40%. The test board was not tilted. As previously, current steps of 100 mA in amplitude have been recorded again on 1.8 V power rail, see figure 5-33. During this test, just one power cycle was applied to the DUT, as in figure 5-33, with the FPGA core and the BRAM power consumption monitored in figure 5-34. In the same time, it can be observed how the core current consumption base value shifts because of the DUT dice temperature increasing through power dissipation.

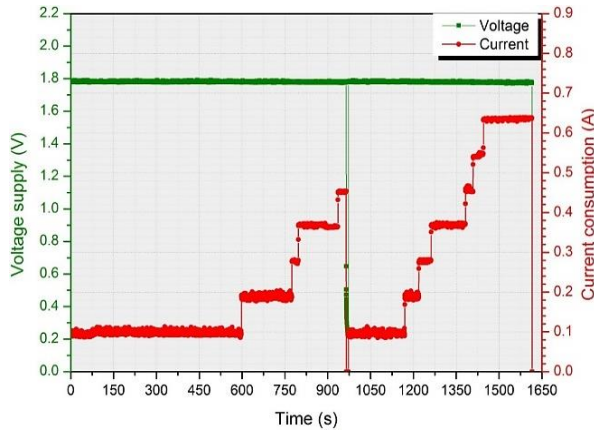


Figure 5-33 SEL induced by ions with a LET of $20.04 \text{ MeV cm}^2/\text{mg}$ in 1.8 V power rail.

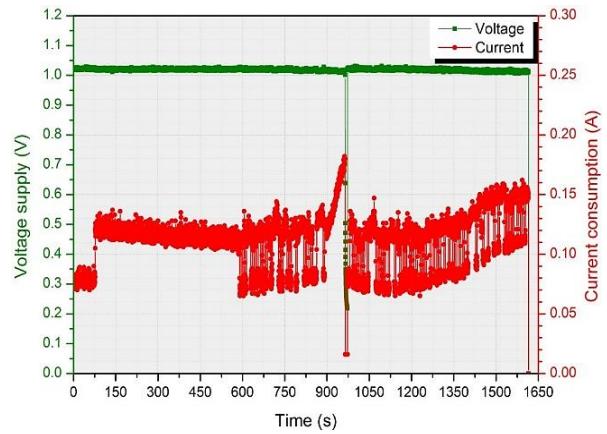


Figure 5-34 Core and BRAM current consumption under $^{58}\text{Ni}^{18}$ ion irradiation.

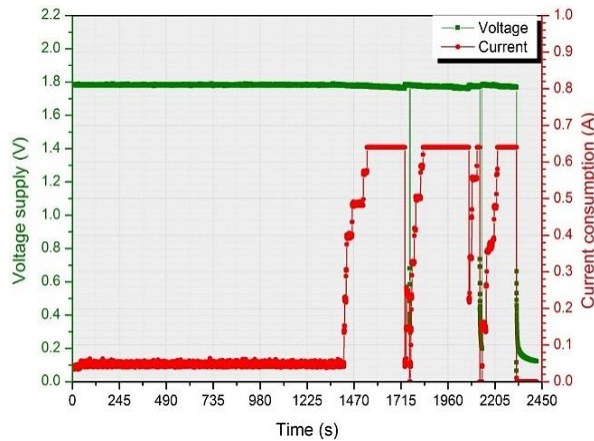


Figure 5-35 SEL induced by ions with a LET of $32.4 \text{ MeV cm}^2/\text{mg}$ in 1.8 V power rail.

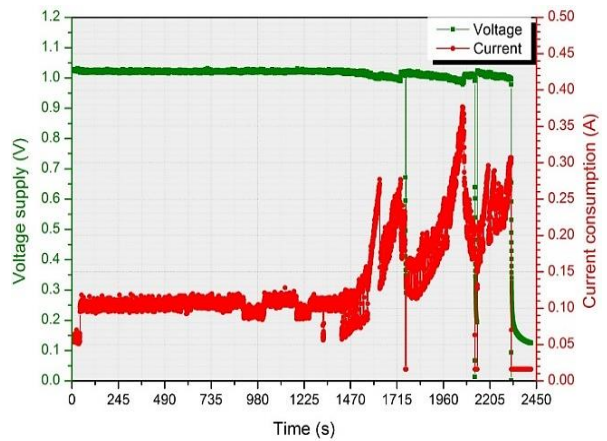


Figure 5-36 Core and BRAM current consumption under $^{84}\text{Kr}^{25+}$ ion irradiation.

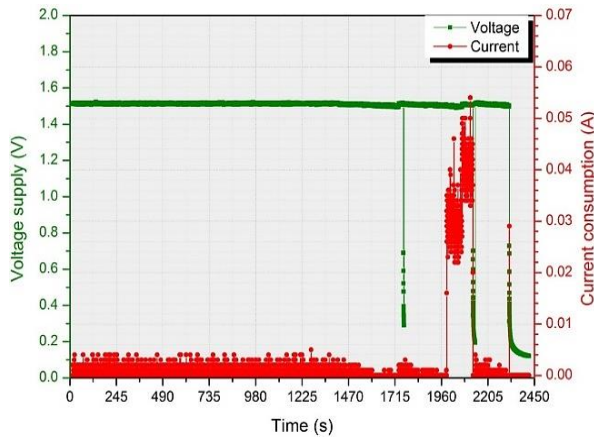


Figure 5-37 SEL induce by ions with LET of 32.4 MeV cm²/mg in 1.5 V power rail.

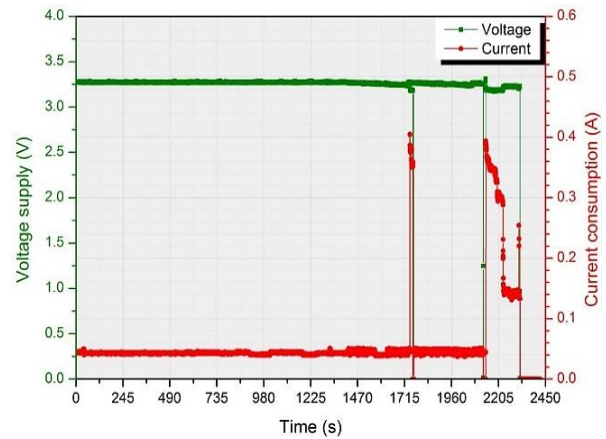


Figure 5-38 SEL induced by ions with LET of 32.4 MeV cm²/mg in 3.3 V power rail.

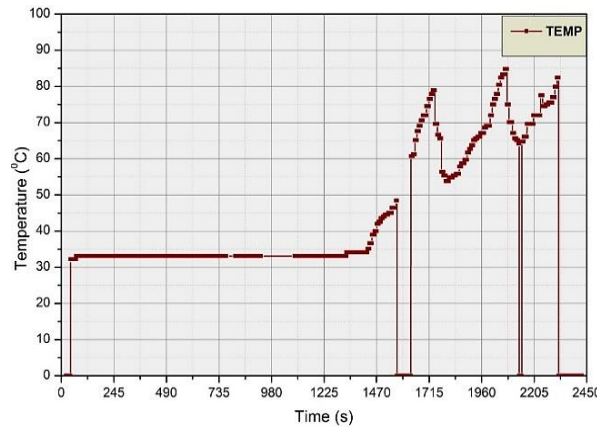


Figure 5-39 The DUT dice temperature during irradiation with ⁸⁴Kr²⁵⁺.

The final test was carried out with a 769 MeV beam of ⁸⁴Kr²⁵⁺ ions, species having a LET of 32.4 MeV cm²/mg. The beam flux was 10³ ions/cm²/s and the total fluency was 9.11 x 10⁵ ions/cm². No changes have been made on the firmware version or in the board positioning. This time several high current states have been recorded and this time not only in 1.8V power rail, figure 5-35, but also in 1.5 V power rail, figure 5-37, and 3.3 V power rail, figure 5-38. With these spikes of high-power consumption, the device had run at temperatures above 50°C as figure 5-39 shows.

The first power cycling was triggered to reconfirm the SEL on a 1.8V rail, while the second power cycling was made to confirm the SEL on a 1.5 V rail. Ultimately, the SEL on a 3.3 V rail supplying the JTAG built-in module and an I/O block was certified with the third power cycling. No sign of SEL was observed in the FPGA core and BRAM power rail as figure 5-36 presents. Due to the device overheating because of SELs on the other three power rails, the baseline current on the FPGA core and on the BRAM has increased with the temperature, even though the device was reconfigured.

After the last test, a trace of permanent damage was observed on the DUT. The FPGA in unconfigured state has a current consumption on 1.8 V supply rail double than before the irradiation. All these tests highlight the impact of various ion species on the KINTEX-7 power consumption. The SEL threshold was found for a LET of 15.56 MeV cm²/mg, which is the LET of Argon ion with the test board tilted at 50 degrees. Correlating data reported by a SEM IP core and the reprogramming log with the measured power consumption values, it allows the computation of micro latch-up cross-section per KINTEX-7 device presented in

figure 5-40. The cross-section corresponding to the micro latch-up threshold is not on the plot as two distinct-DUT results differ slightly – these results correspond to an Argon beam at LET of 15.56 MeV cm²/mg. A closer look is required to better understand this issue.

The logic inside the KINTEX-7 consisting in the TMR flip-flop shift-register chain was tested and the failure rate investigated too. The NEXYS3 readout board incremented continuously how often the bit string pattern was desynchronized, except the failures caused by the CRAM corruption. The 32 bits pattern was injected in the DUT along with the clock signal and shifts at 12 MHz rate, while the KINTEX-7 core was running at 50 MHz. Data gathered were analyzed and the resulting cross-section values versus the LET are shown in figure 5-41.

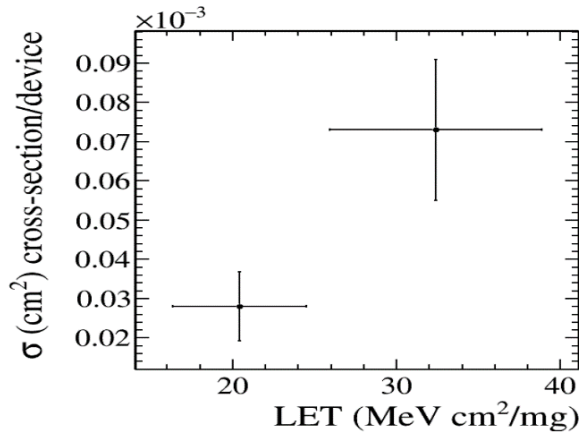


Figure 5-40 The cross-section for a micro latch-up (preliminary values).

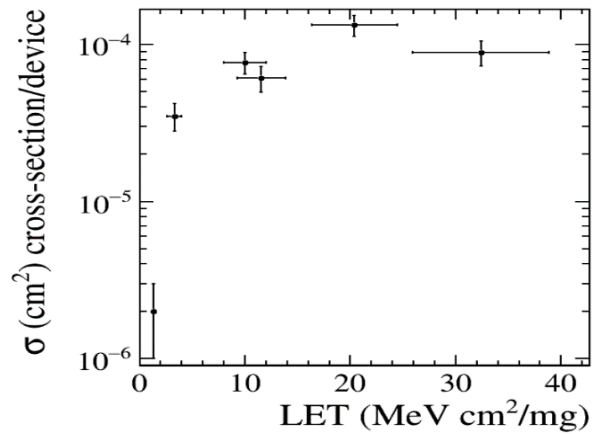


Figure 5-41 Cross-section for flip-flop TMR logic failure (preliminary values).

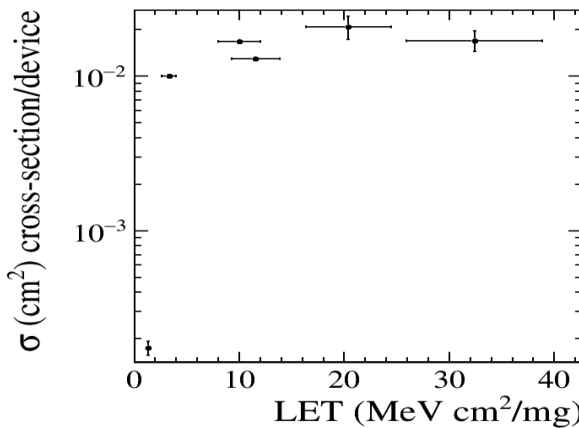


Figure 5-42 Cross-section for single-bit SEU in CRAM for heavy ion test.

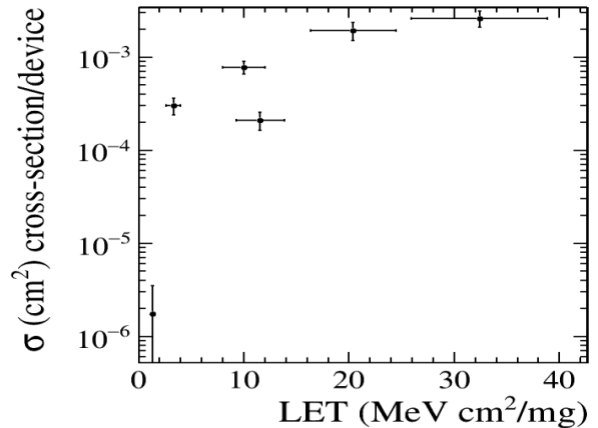


Figure 5-43 Cross-section for multi-bit SEU in CRAM for heavy ion test.

Through a SEM IP core report was possible to inspect the CRAM resilience against the SEU. The measurement was carried out with the SEM IP core configured in the “enhance repair” mode, so it was possible to correct a maximum two adjacent bits per memory configuration frame. In case of multiple bits upset per frame the configuration failed, and the blind scrubbing procedure was applied. Figure 5-42 shows the SEU cross-section for a CRAM when just a single bit per frame was upset and corrected, it is classified and reported by the SEM IP core. On the other hand, the configuration failure caused by multi-bit upset has

the SEU cross-section presented in figure 5-43. Evaluation to the SEE rate induced by species of heavy ions pursued at SIRAD and HIF focused on finding the LET threshold for SEL phenomenon occurrence. In addition, it was possible to check severe implication of the CRAM's integrity failure induced by a SEU. An unexpected high SEU rate was found to affect the CRAM integrity. Various approaches to ameliorate these issues are under consideration. However, the digital board design constraints impose limitation from the radiation tolerance stand point. Adding extra semiconductor devices around basic architecture is the B-case solution, while founding an efficient internal CRAM scrubbing and error mitigation solution is the suitable one at the moment.

5.4 Irradiation test with 200 MeV prtotons

A compulsory pass or fail test is the TID one with the threshold set at 200 krad in case of the RICH sub-detectors. Besides the cumulative effects that might compromise the KINTEX-7, also the radiation-induced single effects are measured through this test. For this purpose, we have accessed the proton-facility PIF at PSI where we have tested the SPACIROC2 chip, too. More details about this proton irradiation facility were given in previous chapter. The irradiation was carried out with a proton beam at 200 MeV energy and a flux ranging from 10^7 up to 10^9 particles/cm²/s. Three FPGA chips were irradiated subsequently each up to 500 krad TID-equivalent in Silicon with accumulated fluency per device at around 10^{10} and 10^{12} protons/cm². Even though, the dose has exceeded two and half times the nominal one, 200 krad expected for the in LHCb-RICH Upgrade phase worst case scenario, we have seen no Latch-Up and the device after reprogramming was recovering completely from SEUs. Moreover, no permanent effects were seen on the tested devices, any increase in currents or voltage fluctuation. Again, a high SEU rate in CRAM was recorded for the proton test, but at lower rate than for heavy ions irradiation, which is expected. Below cross-section values are determined based on four distinct measurements made on all the three FPGAs

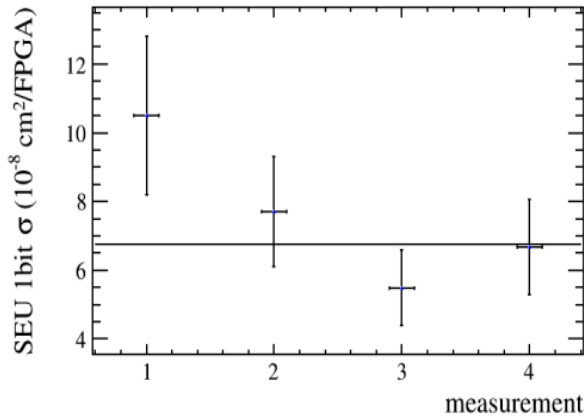


Figure 5-44 Cross-section for single-bit SEU in CRAM for proton irradiation.

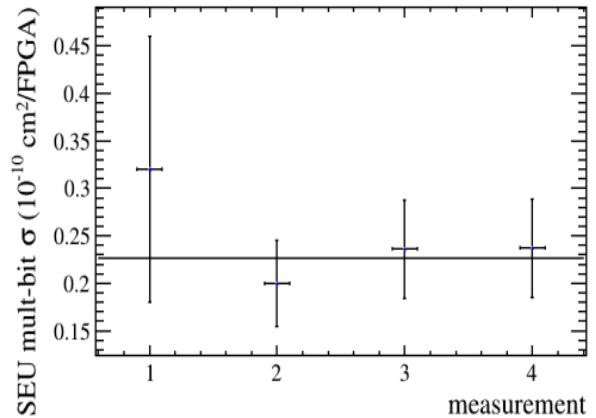


Figure 5-45 Cross-section for multi-bit SEU in CRAM for proton irradiation.

Computing the single bit SEU rate was possible as the SEM IP core classifies and reports them to user. Also, it was possible to measure the values for a SEU cross-section in CRAM, presented in figure 5-44. On the contrary, the figure 5-45 shows the SEU cross-section values for multi-bit upset which lead to SEM IP core configuration failure, due to impossibility to correct these upsets which freezes the SEM IP in idle state.

No destructive SEE has occurred during proton irradiation and no SEL current signature was observed. The high current states recorded during testing procedure have been induced by SEU in CRAM, further leading to FPGA logic resources mismatch. Nevertheless, those events were mitigated by a SEM IP core or blind scrubbing and not through power cycling. Post irradiation tests did not show any sign of cumulative effects that might compromise the KINTEX-7 device.

5.5 Conclusions

The radiation qualification study of our low-end KINTEX-7 FPGA is made from the perspective and constrains dictated by the expected mix-field radiation environment within the LHCb detector for 50 fb^{-1} integrated luminosity. An automatic test bench was design and implemented to record electrical and software parameters of DUT during the evaluation tests. The KINTEX-7 board design was kept as simple as possible. In this way, it was ensured that the radiation tolerance measurements are not compromised by the misbehaviour of other non-radiation hard semiconductor devices. Moreover, the test board follows the outlines of digital board requirements such as no external flash memory for the FPGA and device occupancy. Data are gathered in ASCII files for later analysis. The FPGA power consumption on the main four supply rails was measured at each 50 ms, while the SEM IP status report was continuously stored. Safety constrains on additional electronic equipment used for the FPGA monitoring pushed the setup to its limits. As example for proton testing, the monitoring unit was placed at 5 m away from DUT, while the sampled data was transmitted via another 5 m of USB cable to the host PC and further over Ethernet to the PC from the control room.

The heavy ions tests carried out cover a few crucial aspects regarding the KINTEX-7 tolerance against SEEs. More tests and beam time are required to finalise a complete study on this DUT, and it envisage radiation tolerance measurements of other important FPGA built-in logic elements like BRAM, SLR32 and I/O banks. So far, we confirmed what other literature sources present about micro latch-up occurrence at a LET right above $15 \text{ MeV cm}^2/\text{mg}$ for other not space grade KINTEX-7 FPGA. The CRAM study under heavy ions without error mitigation and without scrubbing solution allowed us to become aware about several effects that might occurs even when a single bit is flipped, and about the SEU cumulative effect in absence of blind scrubbing. The SEM IP core proved a good solution to do a quick and cost-effective investigation into the FPGA configuration and the potential corruption effects. Throughout its means, we had the chance to experience how the FPGA behaves when the CRAM is corrupted deliberately by injecting errors at specific memory location. Unfortunately, the build-in FPGA error mitigation and the scrubbing efficiency in repair or enhanced-repair mode are dropping fast to 0% when the beam has a very high flux, or the particles have a high LET. We took into consideration the use SEM IP core in replace mode with an external flash memory connected to it, this will allow us to have a much better CRAM error mitigation efficiency, though new test for flash memory radiation hardness should be done.

The proton irradiation test was a complete surprise since the KINTEX-7 withstood to 500 krad TID without notable failures due to cumulative effects (SEU rates are very high though). From what the literature mentioned, no other KINTEX-7 FPGA was irradiated to a so high TID level at that time. However, the unexpected rate of SEU induced by protons in CRAM remains a very big concern. There, the proton beam flux was used between 10^7 up to 10^9 particles/cm²/s. No kind of cumulative effects were observed in the accomplished tests in post irradiation phase.

Thorough study on KINTEX-7 radiation tolerance is ongoing to better understand how the device behaves and what might compromise its usage in the digital boards for RICH sub-detectors photodetection system. If it will be decided that it is feasible to run these FPGA with some degree of reliability in the LHCb mixt-radiation environment, then almost 2000 FPGAs will be acquired by LHCb for sub-detectors reconstruction in the LS2 of LHC – Upgrade Phase.

Conclusions, personal contributions and further developments

The LHCb-Romanian group offers its support towards building the new Upgraded LHCb detector. This is done by being actively involved in Research and Development (R&D) Program of LHCb with focus on the radiation hardness qualification campaign dedicated to the new semiconductor devices. These ICs are considered for the RICH sub-detectors photodetection read-out system. As member of the group my contribution has been so far to be actively involved in the context of radiation hardness studies of MAROC3 front-end ASIC and data analysis plus detailed investigation of a low-end FPGA from the KINTEX7 family in LHC conditions. The final goal of these tests was to extrapolate based on the gathered data if these devices can have a reliable operation in the nominal conditions of mixt-field radiation environment, temperature and magnetic field fluctuations estimated to be inside the LHCb detector for the Upgraded Phase (integrated luminosity 50 fb^{-1}).

Specially developed for the JEM-EUSO telescope, the SPACIROC2 is the second ASIC studied by our group, and the radiation hardness to ionizing radiations was mapped for ESA-ISS space-like conditions. This ASIC prototype version serves also as a blueprint of the next generation of MAROCs. The radiation hardness qualifications of these three devices depend heavily on the data collected during the irradiation tests. For each of them a list of quality-parameters was established for online monitoring. Using custom test benches presented in the previous chapters, these parameters are measured continuously and complementary to a set of offline parameters which are measured after and before irradiation. Among the contributions made to evaluate the radiation tolerance of the three chips, this present section seeks to highlight the experimental, practical and theoretical personal contributions.

I. Experimental contributions

I was successful in establishing well defined strategies to test the MAROC3, SPACIROC2 and KINTEX7 using different radiation sources. This was made possible mainly due to the collaboration with the LAL-OmegaMICRO chip design team and the other foreign group partners in LHCb. Since the testing boards provided by OmegaMICRO for MAROC3 and SPACIROC2 were not designed to be used in radiation environments, special precaution had to be taken regarding the test setup to allow exposing only the DUT to the beam. A lead mask has been made to protect additional devices residing on the board near the DUT. Thus, for the KINTEX-7 we designed the test board exclusively toward testing being exposed to radiation, so no extra material in front of the board was needed. My contributions to the irradiation test benches design and implementation along with the testing procedure as well as to the data analysis are summarized in the following paragraphs.

After studying the MAROC3 architecture and test board, in addition doing extensive tests in normal conditions without special radiation or magnetic field conditions, I proposed the test bench architecture for MAROC evaluation under radiation, see figure 3-12. In agreement with the ASIC design team I drafted the list of parameters to be monitored presented in the table 3-1. The design and implementation of the MAROC3 test bench as follows:

- Firstly, I sketch the layout of automatic test bench architecture around the in-house made DAQ system, see figure 3-13. This allowed to monitor online various parameters across the MAROC3 test board and to have a proper control over other parts of the test bench like the power supply for IC.

CONCLUSIONS

- On irradiation site the MAROC3 test board was powered using a custom-made remote power supply capable of delivering ± 7 V and 2 A current on each of the rails, see figure 3-13 right-side. Through the DAQ system its outputs can be switched ON/OFF in order to do power cycling for the ASIC when is needed.
- I took part to the monitoring unit assembly, presented in the figure 3-13. In addition, I have equipped the setup with all screened cables needed.
- To pinpoint eventual SEUs that might prove as destructive as SEL, I brought my contribution to the current measurement circuits for MAROC3, presented in figure 3-14.
- For monitoring the heat dissipation in the MAROC3 chip under irradiation, I selected two types of sensors to be used in the temperature monitoring strategy. We have used the PT100 transducer mainly to monitor any changes in temperature for the bottom part of the PCB underneath ASIC, while for the MAROC3 dice surface, it was used the MLX90614 infrared temperature contactless sensor and I shielded the implemented circuit in 5 mm thick lead case against beam halo scattering. I assembled the hardware part of the MXL90614 IR sensor including the processing unit base on ATEMGA326 microcontroller, see figure 3-15 and Appendix A.
- I proposed for the test bench to be used only screened cables required to interconnect the setup. Also, I studied and characterized the MAROC3's behaviour in normal condition of operations.
- Presented in the figure 3-16 it is the LabVIEW GUI used to control the test bench for MAROC3 to which I contributed. Through this GUI was possible to save within ASCII files the parameters recorded before and during the irradiation of each ASIC sample tested.
- Regarding the MAROC3 irradiation with 35 MeV proton beam, I was involved in the test bench installation on beam line as well as in the DUT monitoring over the testing period.
- I took part at the data analysis and I made the interpretation of all electrical parameters recoded during irradiation test and post irradiation.

SPACIROC2 inherited multiple elements from MAROC3's architecture. Because of theirs similarity, we just adapt the test bench wiring scheme to test board outputs to fulfil the monitoring requirements of SPACIROC2. My experimental contribution to SPACIROC2 chip radiation tolerance investigation is summarised below.

- The OmegaMICRO design team provided us the GERBER files for a PCB production and the SPACIROC2 test board schematic. I was in charge with sending the PCB to the foundry for manufacturing and after I assembled in the lab three SPACIROC2 test boards entirely, and test them to prove they were fully functional, see figure 4-2.
- Since the ASICs were mounted on the test boards via clamshell sockets, I have adapted it to the chip ceramic package to allow connections to the SPACIROC2 die. Further, using a microscope I have aligned each of the chip's pins with those of the socket.
- I had also a few contributions to the GUI development for the DAQ system presented in the figure 4-9 and solid contribution to the SPACIROC2 characterisation before the irradiation procedure.
- Again, I took part in the test bench installation on proton beam line at PSI Institute in Switzerland, as well as in the monitoring procedure.

CONCLUSIONS

- The measured data have been carefully analysed and I brought my contribution to the electrical parameter interpretation.

The KINTEX7 FPGA represents the main electronic device to be used on future digital boards for the RICH sub-detector chains, at least in the present design. Testing its radiation hardness implies to access various irradiation facilities, plus an increased human and financial resources due to the complexity of the hardware as well as that of the software/firmware. Our contribution was to design and implement entirely the KINTEX7 FPGA test bench and boards in agreement with the indications suggested by the LHCb collaboration experts. The KINTEX-7 test board was designed to accommodate a minimal number of electronic components needed by the FPGA to have at least a basic operation. The steps taken in the design and implementation of the test bench for the KINTEX7 radiation qualification were:

- To propose the architecture layouts for the FPGA test board, the power supply board, and the DAQ system. Each of these have been discussed in the LHCb Collaboration meetings and afterward approved for implementation.
- I had to supervise the schematic and the PCB design to all boards specially developed for the KINTEX-7 test bench presented in figure 5-1, Appendix D and Appendix E.
- After the PCB arrived from the factory, I completely assembled 9 FPGA test boards out of which 4 are with thinned FPGA chips, see figure 5-3. For this I have used an IR-infrared reworking/reballing station. Also, I assembled 4 power supply boards in the same way, see figure 5-4.
- The monitoring unit of the KINTEX-7 was implemented with my support, while the screened cables needed for setup were installed by me, see figure 5-5.
- When the setup was completed, I got involved in the device testing and I coordinated the firmware development. In addition, I suggested several improvements to the GUI design and functionality. Overall, I had to debug the hardware problems occurring during the setup implementation up to its final version.
- I provided expertise for the SEM IP core use and I took part in the offline tests carried out in the laboratory.
- Regarding, the irradiation tests pursued at SIRAD Legnaro, HIF Louvain and PSI, together with my colleagues I had to install on the beam lines the setup and I attended to the device monitoring.
- Finally, I got involved in the laborious data analysing procedure for the KINTEX-7 irradiation. The device behaviour had to be explained by corroborating the electrical and firmware parameters recorded during these irradiation tests.

The irradiation qualification tests remain the only straightforward solution to investigate the radiation resilience of an integrated circuit. Despite being costly, time consuming and work-power demanding the irradiation tests provides crucial data based on which the device behaviour can be extrapolated for a certain radiation environment during many years. Up to now, the data gathered over multiple tests tends to maintain the interest of using in the LHC radiation environment the KINTEX-7 chips, though other solutions are being investigated due to the large measured SEU rate in these devices. More tests must be performed on the MAROC3 to better understand its radiation tolerance. On the other hand, the SPACIROC2 passed at limit the TID test, while the heavy ions irradiation will clarify the chip's immunity against SEEs. The KINTEX-7 is a promising solution for the digital board especially after successfully passing the TID test. No destructive SEE effects occurred on it during heavy ion

testing. However, the high SEU rate in CRAM remains the main issue to be overcome through configuration scrubbing and error mitigation.

II. Theoretical contributions

Periodically I have done reports concerning the MAROC3, SPACIROC2 and KINTEX7 testing status to the LHCb collaborators and to the LAL-OmegaMICRO group from École Polytechnique of Palaiseau Paris, France. This allowed me to benefit from their expertise in the fields of rad-hard testing and the dedicated microelectronics which is used for high-energy physics experiments. Often, the encountered problems had solutions found during these meetings. A list of talks is summarised in the following:

1. ***Data analysis for the SPACIROC2 proton irradiation***, LHCb-Romania, September 21st 2016, IFIN-HH, Magurele, Romania, available at: <https://indico.cern.ch/event/570828/>
 - On this occasion, I discussed with the SPACIROC2 design team the preliminary result of chip irradiation at 200MeV protons. The ASIC's behaviour above 60Krad was interpreted closely.
2. ***Preliminary results of KINTEX-7 irradiation with heavy ions at Louvain***, RICH Upgrade Meeting, June 14th 2016, CERN, Geneva, Switzerland, available at: <https://indico.cern.ch/event/540695/>
 - I put forward the preliminary results outcoming from heavy ion irradiation at Louvain where the threshold LET for a micro latch-up (SEL) has been measured.
3. ***KINTEX-7 FPGA radiation hardness studies, test bench, firmware, error mitigation & scrubbing***, LHCb Upgrade Electronics, February 11th 2016, CERN, Geneva, Switzerland, available at: <https://indico.cern.ch/event/490512/>
 - In the current presentation, I outlined the preparation that has been done to test the KINTEX-7 under radiation by emphasis the firmware's developed, plus the internal CRAM scrubbing and mitigation solution with SEM IP.
4. ***Update on SPACIROC2 testing***, Omega MICRO designer team, November 19th 2015, Dahi-X Novation Center, Ecole Polytechnique, Paris, France.
 - Here I presented to the LAL-OmegaMICRO group the test bench and monitoring strategy for SPACIROC2 proton irradiation.
5. ***Status and perspectives for KINTEX-7 irradiation***, Mini-meeting on irradiations for RICH Upgrade, July 8th 2015, CERN, Geneva, Switzerland available at: <https://indico.cern.ch/event/406534/>
 - The irradiation plan along with the status of KINTEX-7 setup were presented in detail.
6. ***Update on KINTEX-7 irradiation setup***, RICH meeting, June 8th 2015, CERN, Geneva, Switzerland available at: <https://indico.cern.ch/event/399125/>
 - I presented the new features and improvements brought to the test bench architecture.

7. **First prototype of KINTEX7 module designed for irradiation tests**, RICH Upgrade Testbeam Meeting, April 1st 2015, CERN, Geneva, Switzerland available at: <https://indico.cern.ch/event/385716/>
 - On this occasion, I introduced the functional version of the KINTEX-7 basic test bench for radiation hardness evaluation.
8. **Characterization of the MAROC 3 before irradiation**, RICH Upgrade Testbeam Meeting, July 23th 2014, CERN, Geneva, Switzerland, available at: <https://indico.cern.ch/event/331717/>
 - In this presentation, I proposed a test bench architecture for online monitoring of the MAROC3 during the irradiation process along with the final list of parameters selected to be monitored, as well as the testing procedure.
9. **Multi Anode ReadOut Chip (pre-irradiation tests)**, RICH Upgrade Testbeam Meeting, June 11th 2014, CERN, Geneva, Switzerland, available at: <https://indico.cern.ch/event/324199/>
 - Here I made known a couple of issues that withstood against the MAROC3 characterisation in normal condition of running.

III. Results dissemination

The contributions added by the present thesis in the area of semiconductor devices radiation hardness qualification have been disseminated through journal publications and conferences. In the following are listed all the scientific contributions made.

A) Relevant papers for thesis topic:

- [1] V. M. Placinta, **L. N. Cojocariu**, and C. Ravariu, "Test bench design for radiation tolerance of two ASIC's," *Accepted for publication in Romanian Journal of Physics (RJP)*, 2017, ISI journal with impact factor 1.398;
 - The test bench architecture for measuring the radiation hardness of SPACIROC2 and MAROC3 has been published. Various cumulative and single event effects induce by radiation have been described along with the method to measured them.
- [2] M. K. Baszczyk, M. Benettoni, **L. Cojocariu** et al, "Test of the photon detection system for the LHCb RICH Upgrade in a charged particle beam," *Journal of Instrumentation*, vol. 12, pp. P01012-P01012, 2017, DOI: 10.1088/1748-0221/12/01/p01012, ISI journal with impact factor 1.310;
 - This paper presents the tests performed with a prototype version of an elementary cell within charged particle beam. The setup was based on Hamamatsu R11265 MaPMTs connected to the CLARO front-end boards.
- [3] **L. N. Cojocariu**, V. M. Placinta, and L. Dumitru, "Monitoring System for Testing the Radiation Hardness of a KINTEX-7 FPGA," *9th International Physics Conference of the Balkan Physical Union (Bpu-9)*, vol. 1722, p. 140009, 2016, DOI: 10.1063/1.4944199, (ISI Proceeding);

- The test bench architecture for the KINTEX-7 radiation tolerance measurement has been published along with the first version of firmware layout used at SIRAD testing in Legnaro. Also, the SEL and the SEU impact in logic has been simulated.
- [4] M. Prelipceanu, **L. Cojocariu**, A. Graur, and S. Schrader, "Analysis of thermally stimulated processes in new phenanthroline derivatives suitable for optoelectronic devices," *Journal of Physics: Conference Series*, vol. 585, p. 012011, 2015 DOI: 10.1088/1742-6596/585/1/012011, (ISI Proceeding);
- This study presents a compound material suitable for optoelectronic devices that could have an application also in high-energy physics.
- [5] R. Aaij, B. Adeva, **L. Cojocariu** et al, LHCb Collaboration, "Search for long-lived heavy charged particles using a ring imaging Cherenkov technique at LHCb," *European Physical Journal C*, vol. 75, Dec 2015, DOI: 10.1140/epjc/s10052-015-3809-7, ISI journal with impact factor 4.912;
- Here is published a detailed investigation on the RICH sub-detectors capability of distinguish from muons the heavy and slow-moving particles. The study is made for some proton-proton collisions at 7 TeV and 8 TeV centre of mass energy.
- [6] R. Aaij, B. Adeva, **L. Cojocariu** et al, LHCb Collaboration, "LHCb detector performance," *International Journal of Modern Physics A*, vol. 30, Mar 10 2015, DOI: 10.1142/s0217751x15300227, ISI journal with impact factor 2.373.
- Based on data gathered from 2010 to 2012, the current paper aimed to evaluate the LHCb machine performance by a closely approach on each sub-detector, including RICH. The results emphasise the LHCb detector role for introspecting matter and antimatter building blocks.

B) Conferences participation

1. **L.N. Cojocariu**, F. Maciuc, V.M. Placinta, "Experimental study on Soft Error Mitigation Core (SEM IP) efficiency", Workshop on Sensors and High Energy Physics (SHEP 2016), Stefan Cel Mare University of Suceava (USV), Suceava, Romania, 21 – 22 October 2016.
2. V.M. Placinta, **L.N. Cojocariu**, "Test bench for ASIC radiation hardness evaluation", Workshop on Sensors and High Energy Physics (SHEP 2016), Stefan Cel Mare University of Suceava (USV), Suceava, Romania, 21 – 22 October 2016.
3. **L.N. Cojocariu**, V.M. Placinta, "Designing and implementing test benches for radiation hardness qualifications of readout electronics from LHCb RICH photodectors", The 15th International Balkan Workshop on Applied Physics (IBWAP), July 2-4 2015, Ovidius University of Constanta, Romania, IBWAP Book of abstracts, pp. 103-104.
4. V.M. Placinta, **L.N. Cojocariu**, "Practical test bench used for testing Photomultiplier Tubes, type MaPMT", The 15th International Balkan Workshop on Applied Physics (IBWAP), July 2-4, 2015, Ovidius University of Constanta, Romania, IBWAP Book of abstracts, pp. 115.

Further developments

The mixed-field radiation environment raises reliability issues to be overcome by the semiconductor devices, especially for the COTS components, to be used within photodetection systems of both Upgrade RICH sub-detectors. Therefore, the radiation hardness tests play a decisive role in establishing whether the considered device might withstand to this intense radiation field without a considerable degree of damage for long periods of time, or without considerable deviation from nominal parameters. Testing the resilience against the radiation damaging effects is carried out with various species of high energy particles like protons, neutrons, heavy ions, X-ray and alpha particles. Being outlined in this thesis the testing results will be consolidated based on recorded data from upcoming irradiations. Time slots are already reserved at several irradiation facilities for better testing and understanding the behavior of MAROC3, SPACIROC2, as well as the KINTEX-7 FPGA under radiation.

For the MAROC3 chip, the final test will be made with a proton beam above 35 MeV, while the SPACIROC2 chip will part of an extensive irradiation campaign involving species of heavy ions, protons and X-ray. The final goal is to obtain the SEL and SEU cross-sections for SPACIROC2 function of LET and proton energy. On the other hand, subsequent irradiation tests on the KINTEX-7 will allow us to have a closer look on the FPGA constitutive blocks, such as BRAM and I/O banks.

Upcoming tests will let us conclude on the radiation tolerance of each chip. Moreover, the KINTEX-7 radiation resistance will be also investigated at CHARM. In this purpose a preliminary version of the digital board would be exposed to the facility mixed-field radiation environment. After this last test, a final decision will be made if this FPGA is suitable from radiation hardness stand point to be used for the digital boards in the new photodetection system readout of RICH sub-detectors. However, the high SEUs rate in CRAM remains a big concern for the FPGA firmware reliability. Preliminary estimations pointed out that the SEU rate in KINTEX-7 CRAM is very unlikely to be overcome through blind scrubbing via JTAG. Unfortunately, the JTAG interface of the GBT-SCA chip is meant to run at maximum 20 MHz, so reconfiguring such high number of FPGAs will take time. A solution is to lower the firmware occupancy on the CRAM through design optimisation.

Plans are made to test the backup solution for KINTEX-7 which is an antifuse based FPGA produced by the Microsemi Company. As main drawback, this type of FPGA is one time programmable, but more immune to SEE, thus the SEU and SEL threshold is defined at high LET. The open issues are their behaviour at TID above hundreds of krad. Irradiation tests must be done to check if the antifuse FPGA part number considered as backup for digital board it will withstand at least up to 200 krad TID. Our group will design and implement a complete test bench for the antifuse FPGA monitoring and characterisation during irradiation and post irradiation too. A custom test board for DUT will be assembled as well as a new power supply system to fit the device power requirements. Regarding the DAQ system, it will be based on blueprint one made for KINTEX-7 monitoring, but more versatile.

When the final design and production of the digital boards will be ready, we will be ready to get involved in the assembling and mass testing of the digital boards. Thereupon, a test bench that emulates the front-end and back-end electronics chain from RICH sub-detectors is desirable to be implemented. Maintaining the same test conditions, each digital board will be fully characterised from electrical, software and thermal stand point. Outcoming data shall be stored in a data base. Based on the collected parameters most probably a software routine will be implemented for the pass or fail test.

Finally, we will contribute to the RICH sub-detector assembling and commissioning, data taking and maintenance.

CONCLUSIONS

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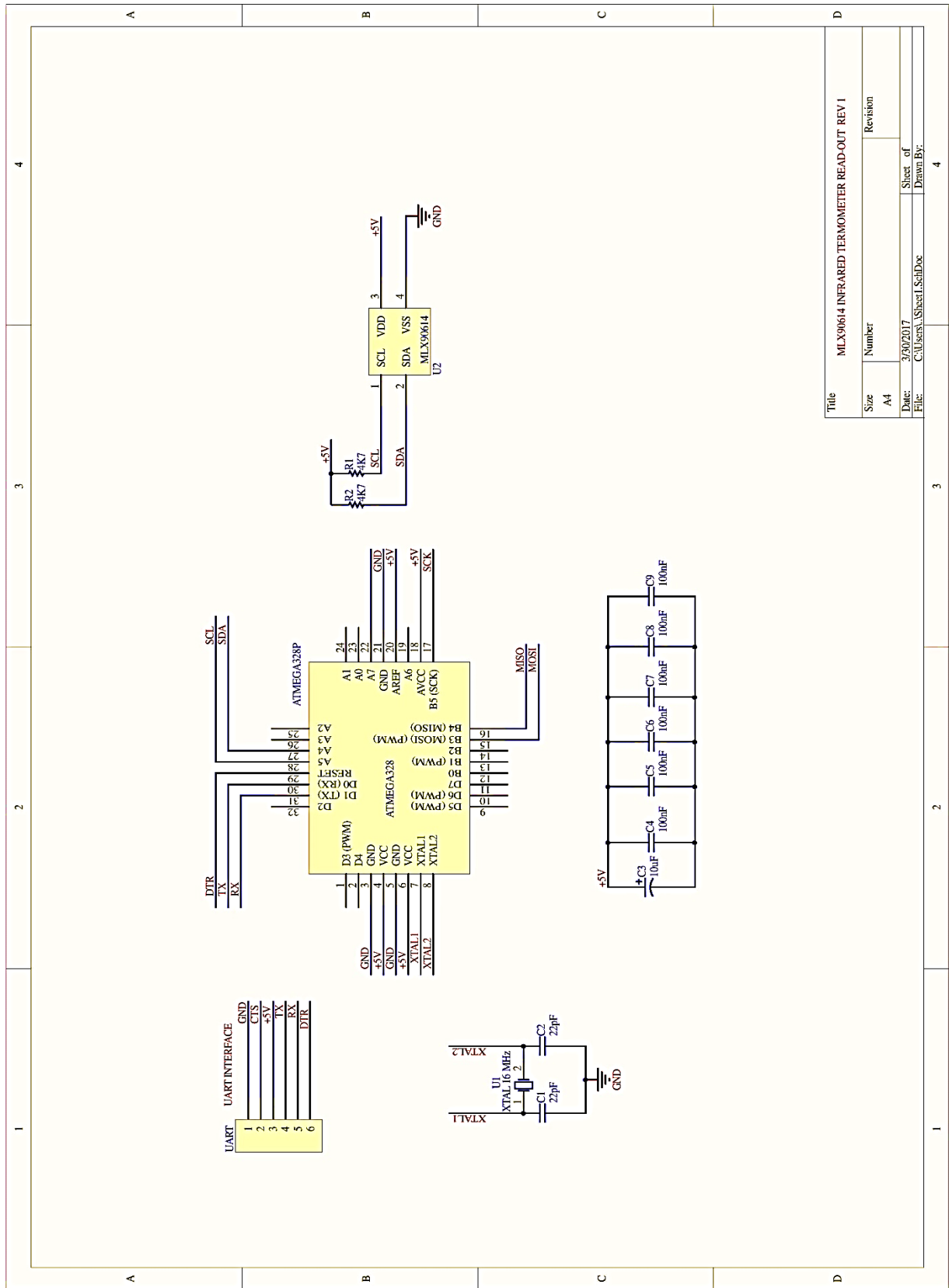
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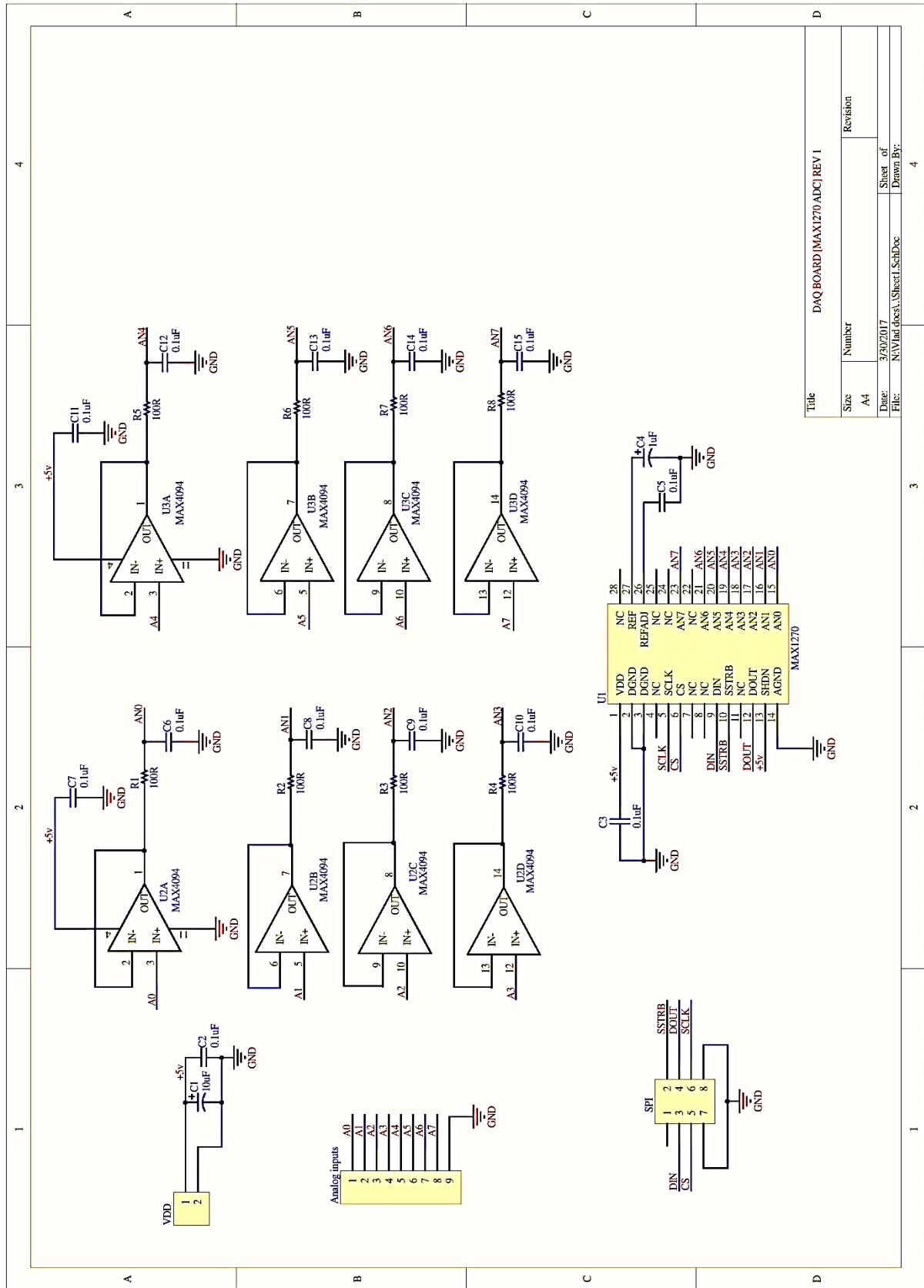
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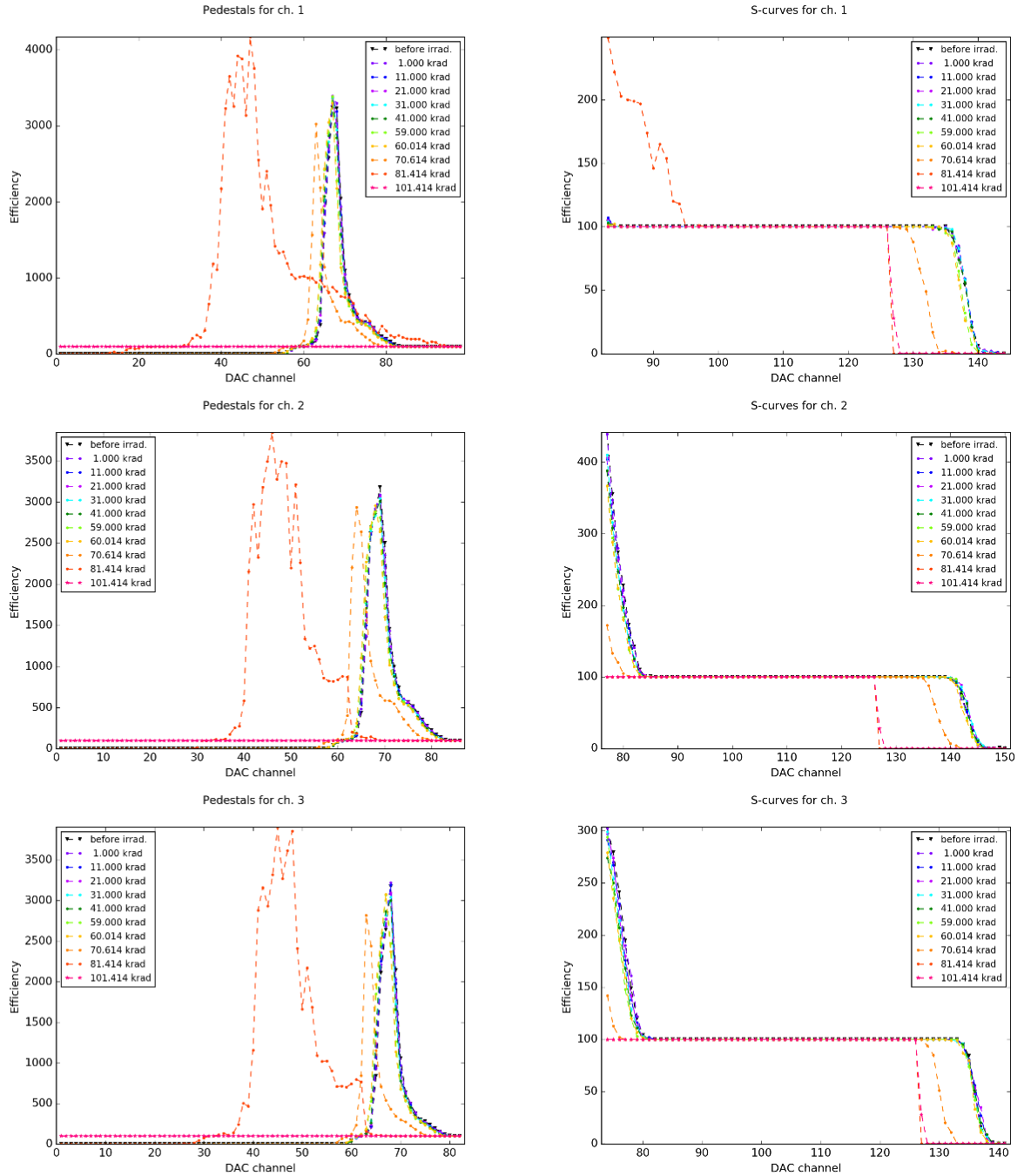
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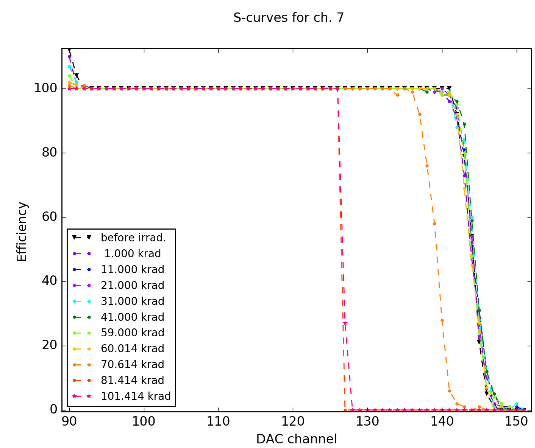
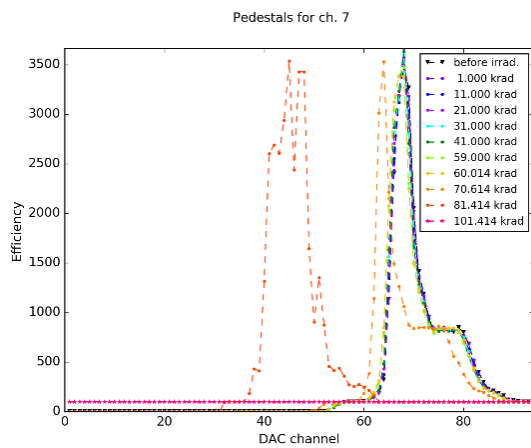
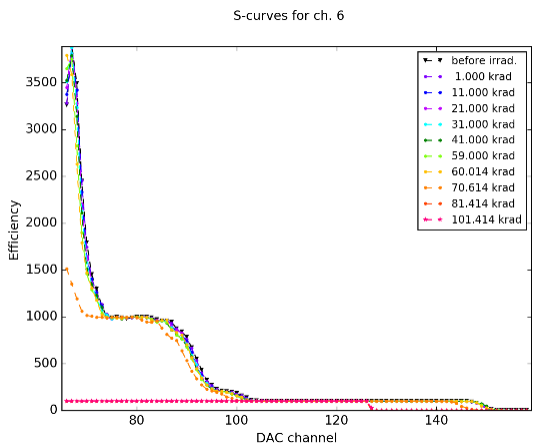
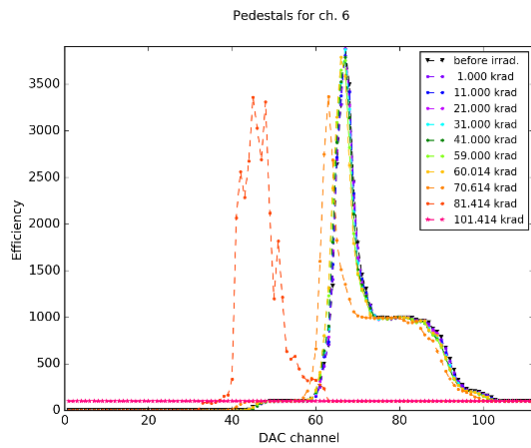
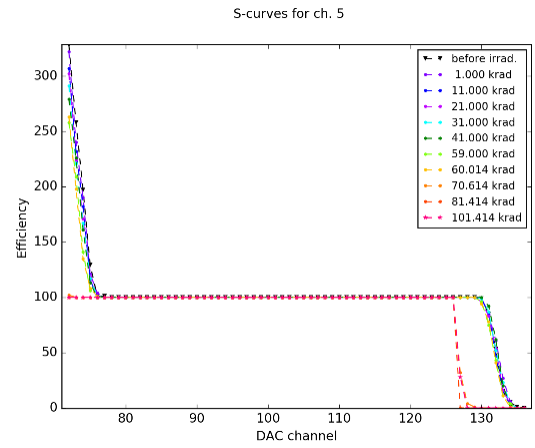
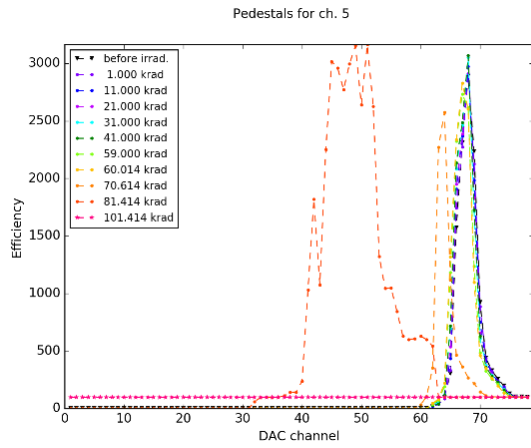
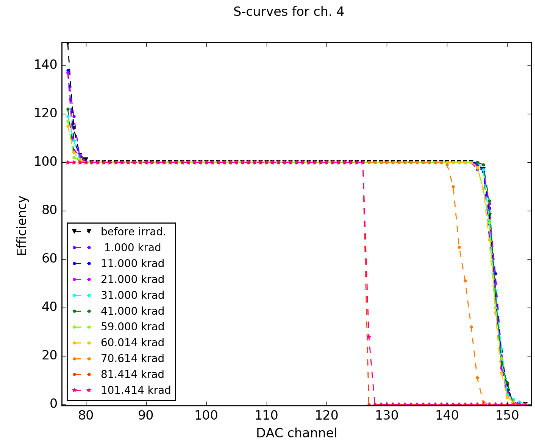
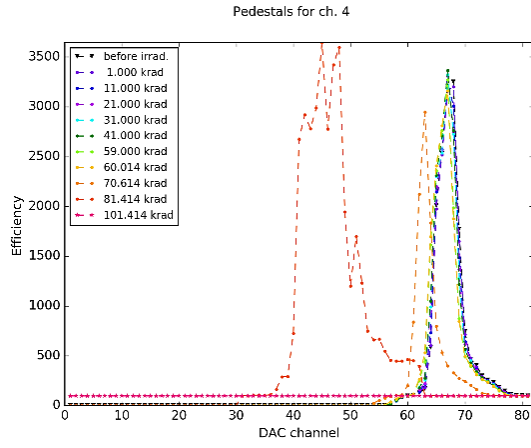
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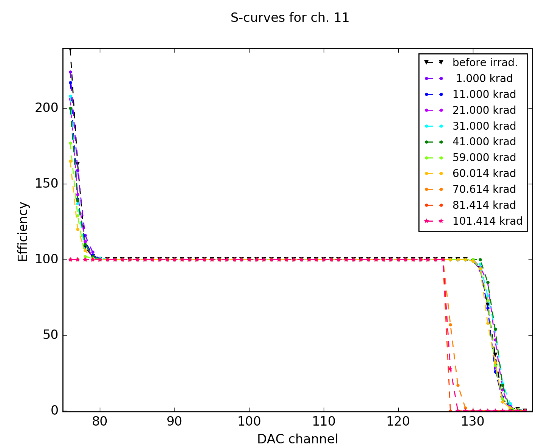
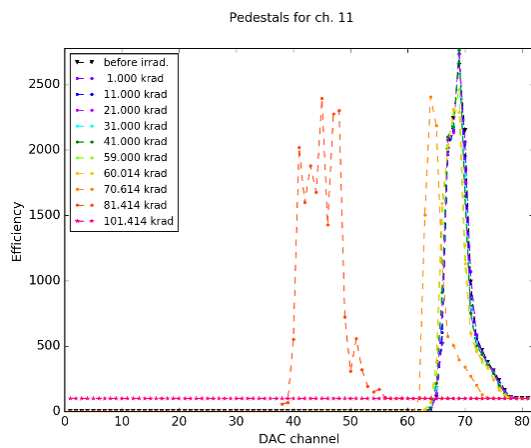
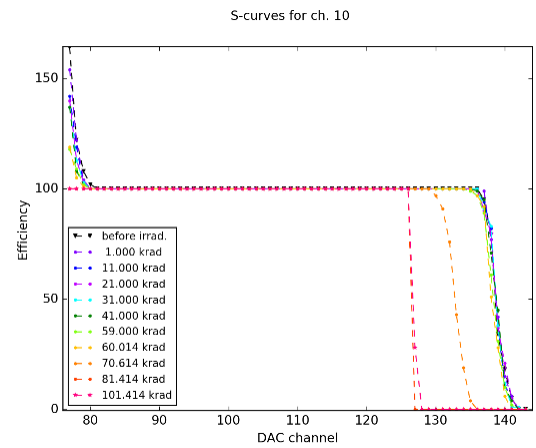
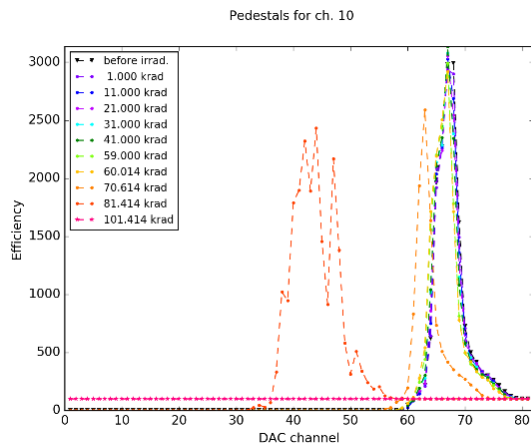
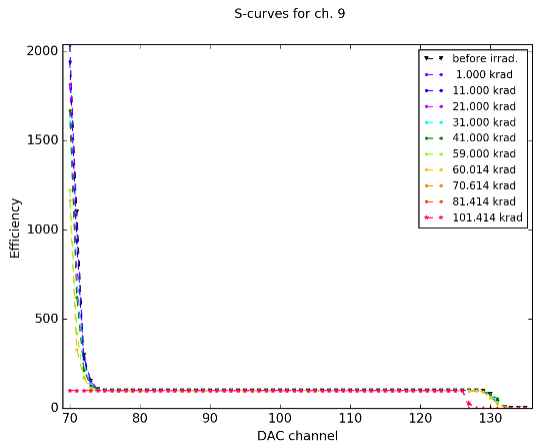
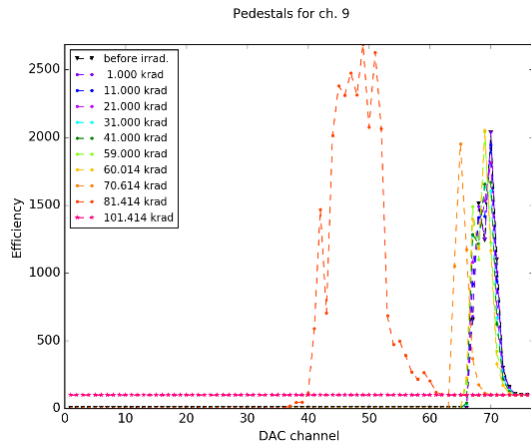
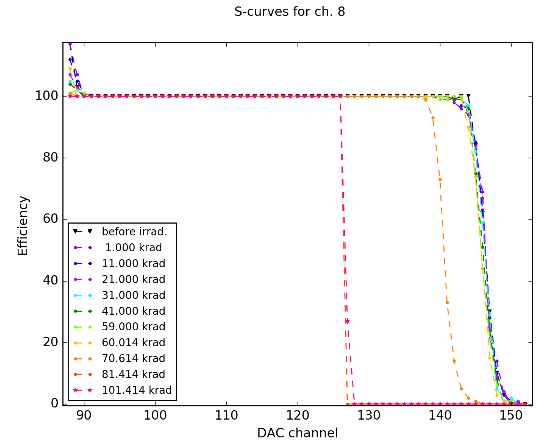
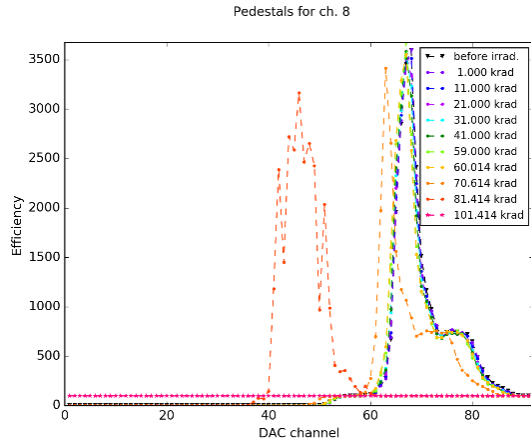


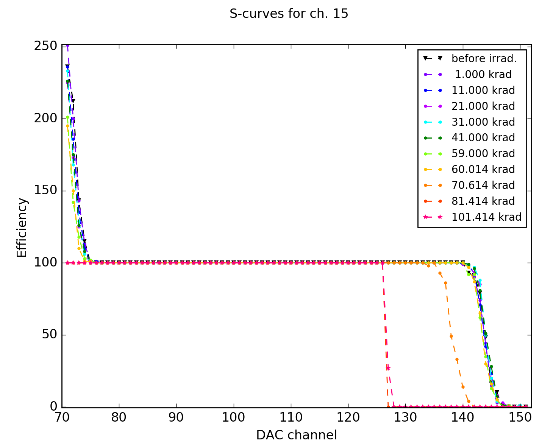
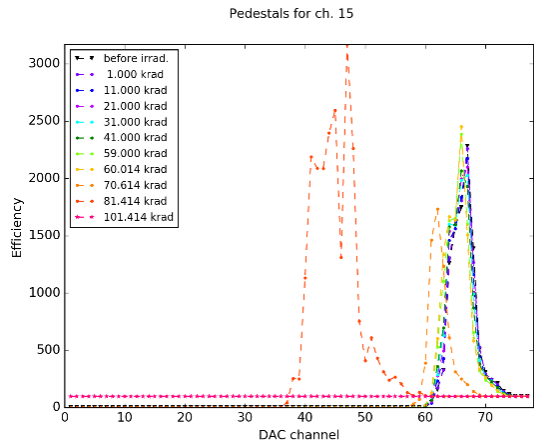
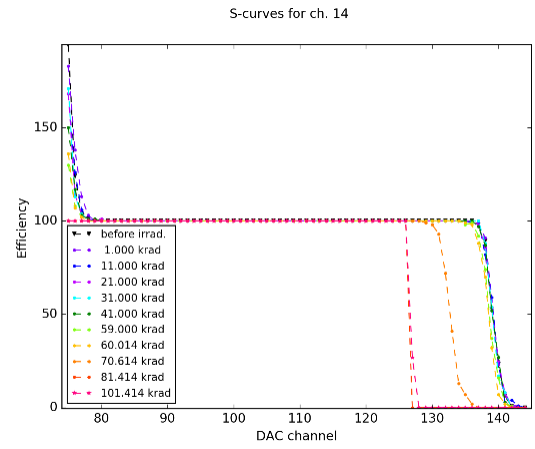
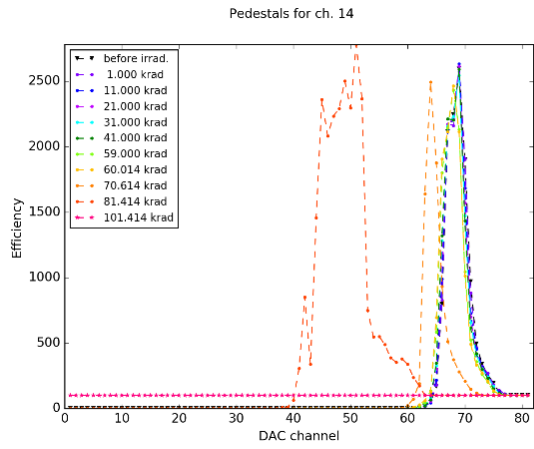
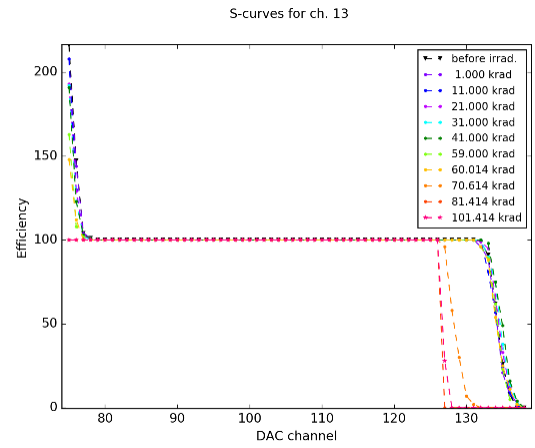
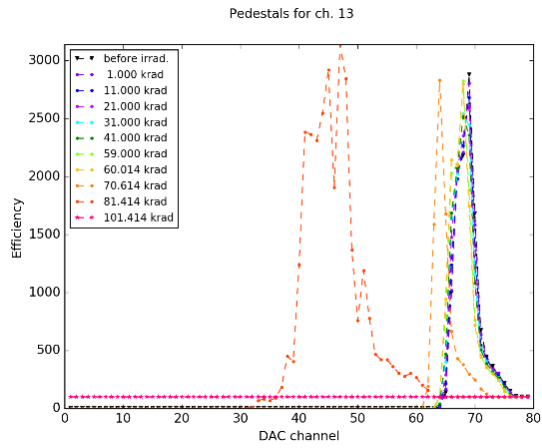
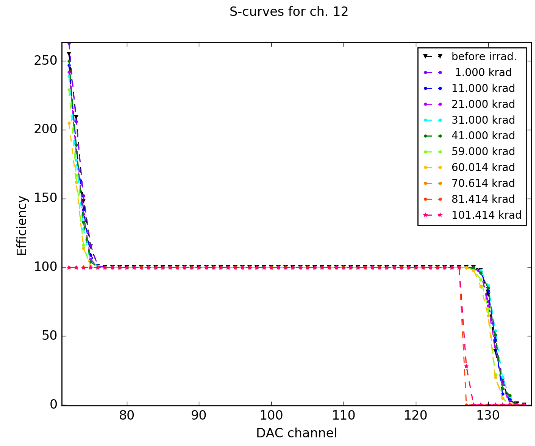
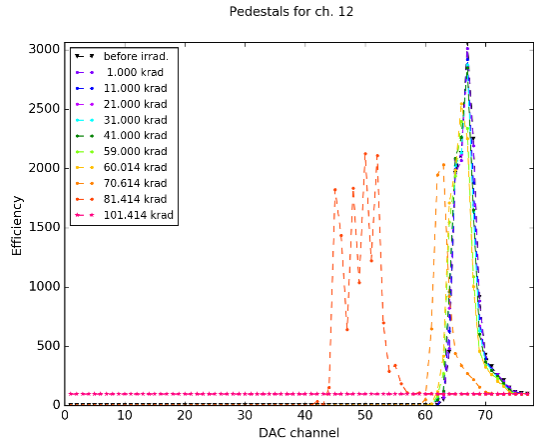
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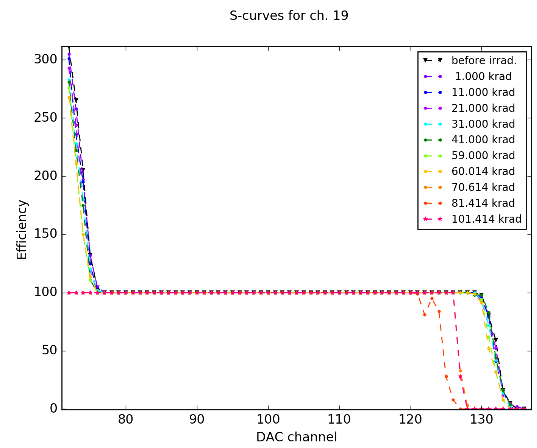
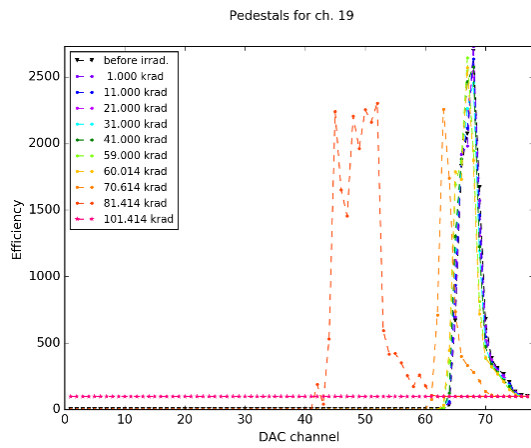
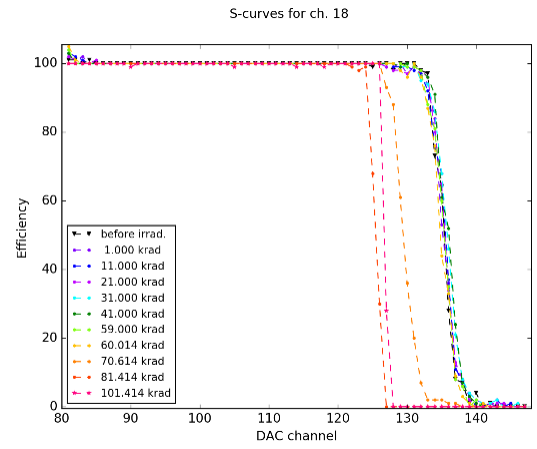
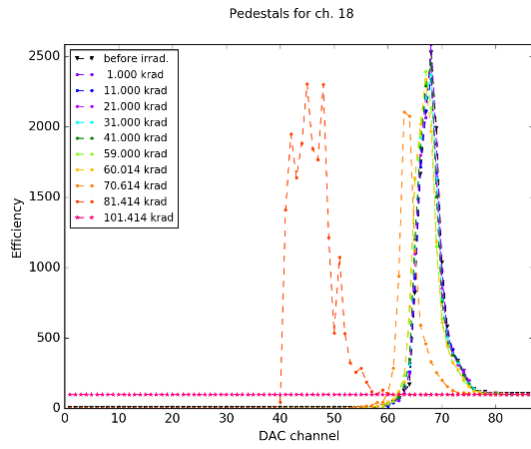
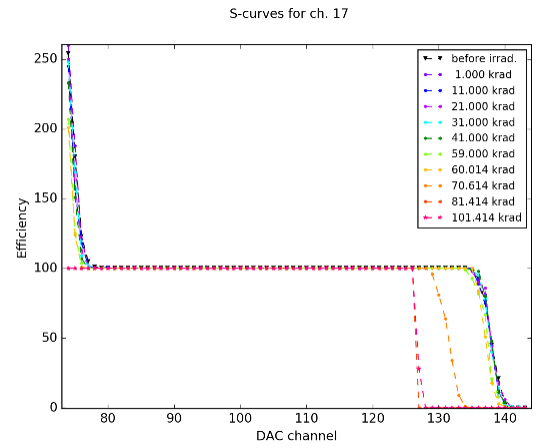
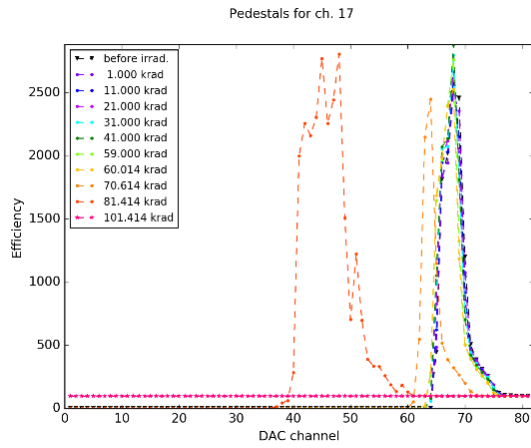
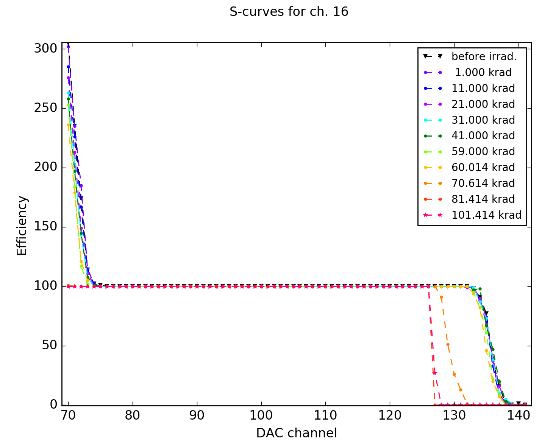
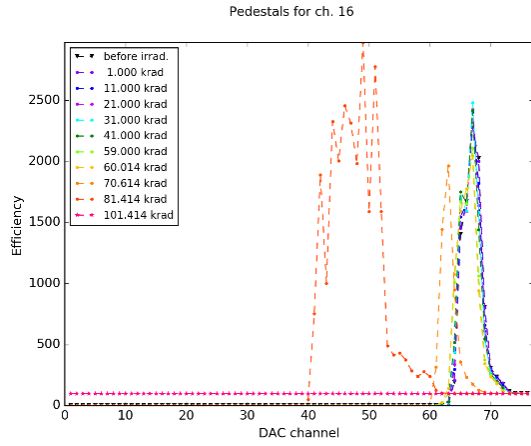
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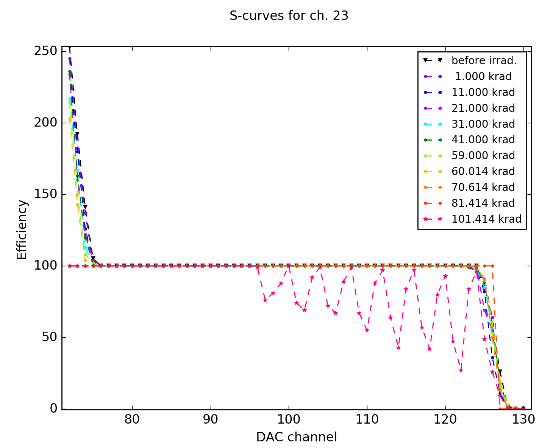
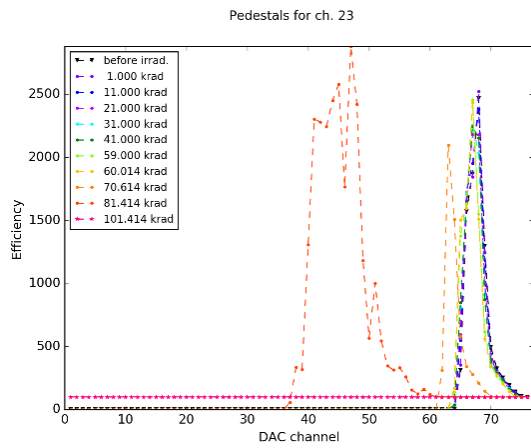
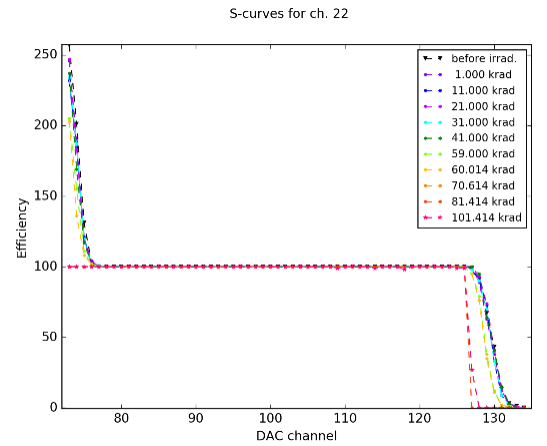
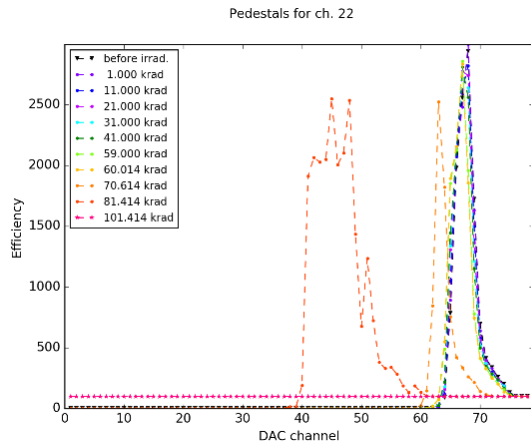
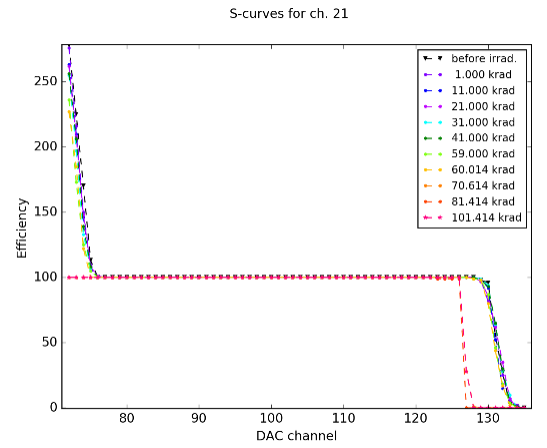
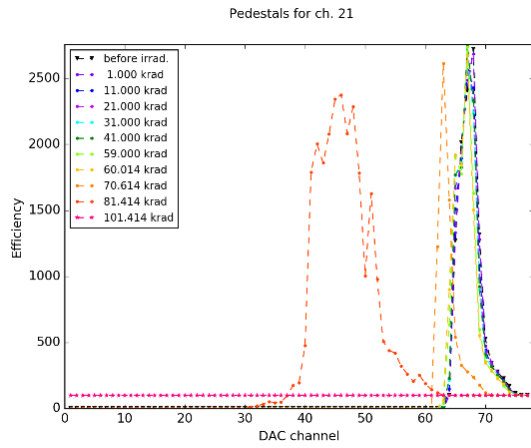
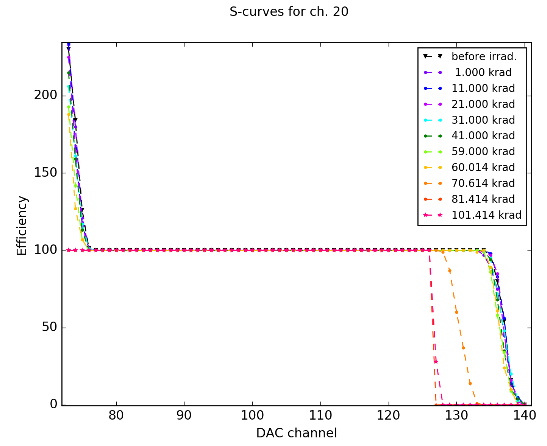
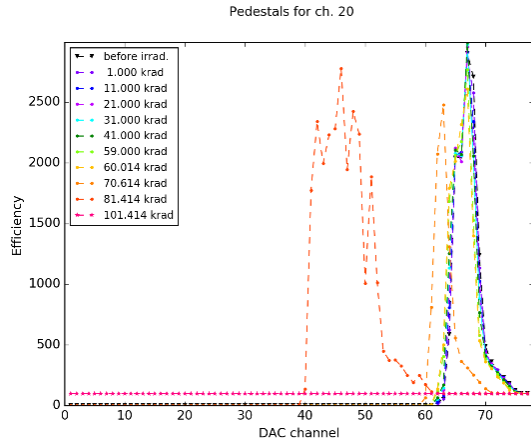


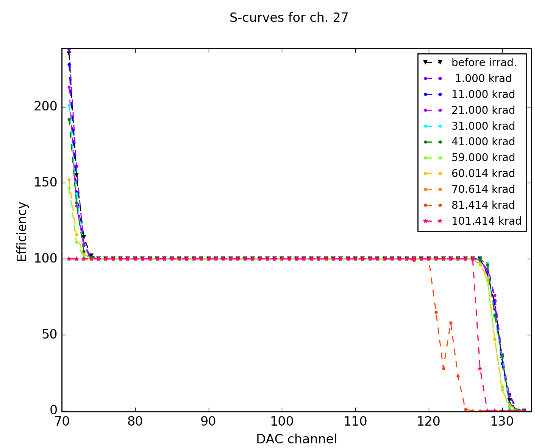
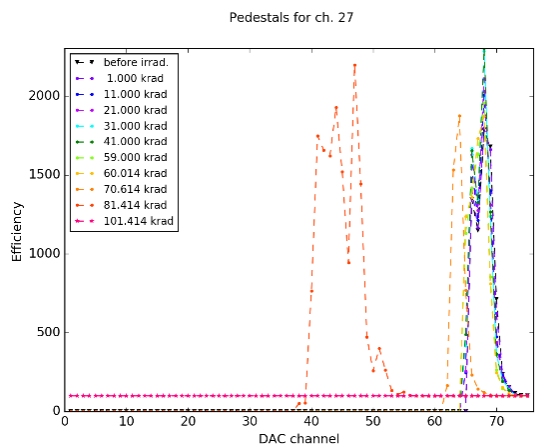
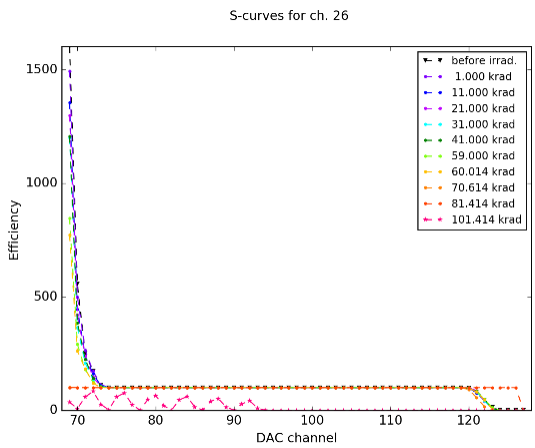
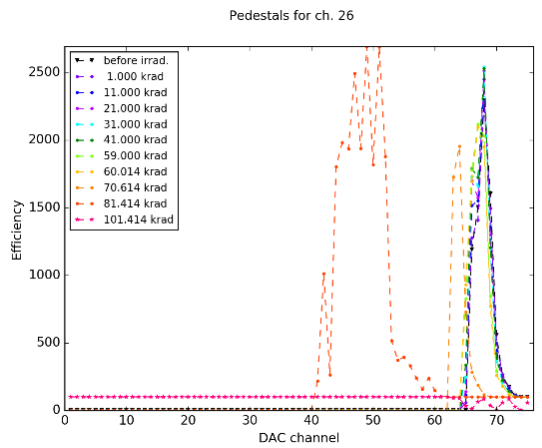
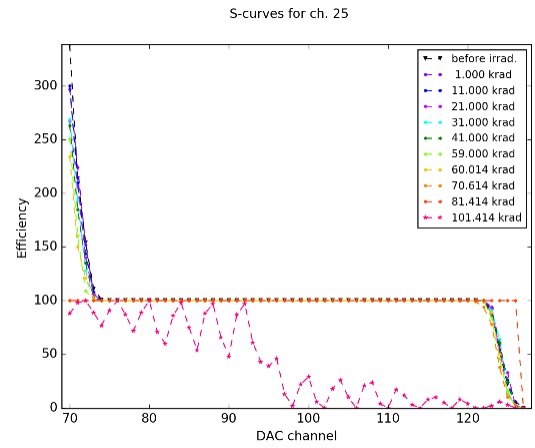
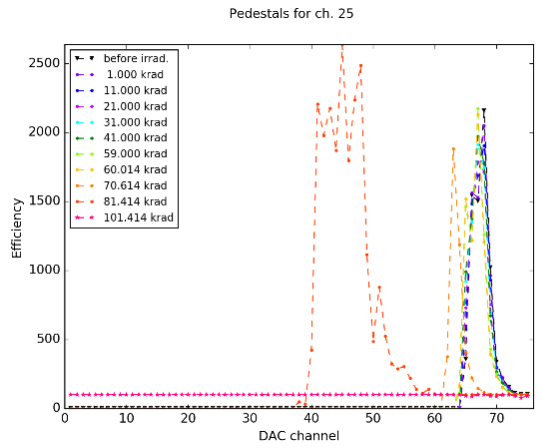
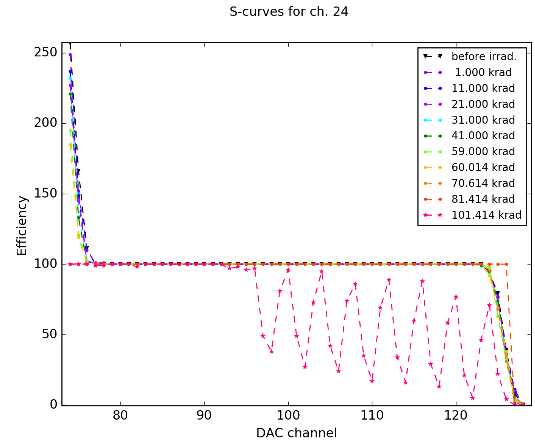
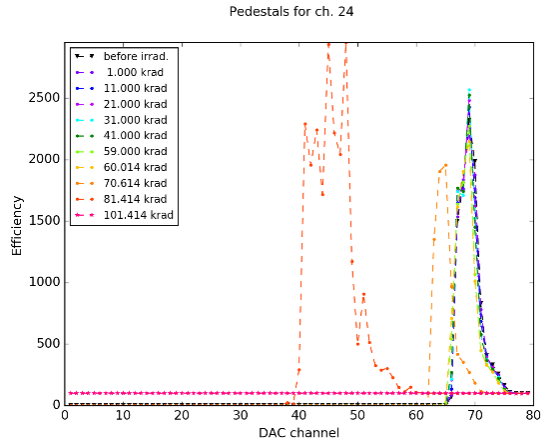


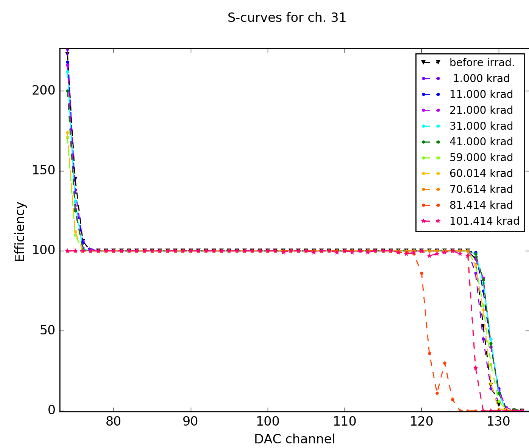
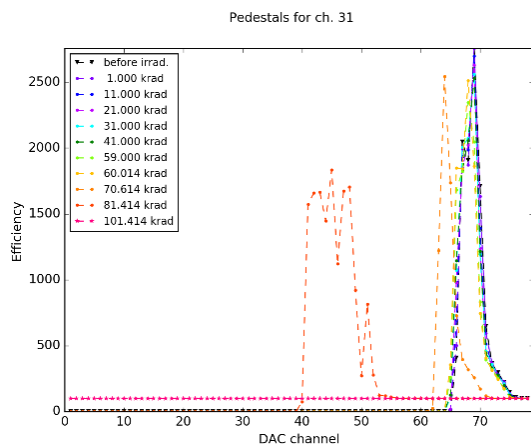
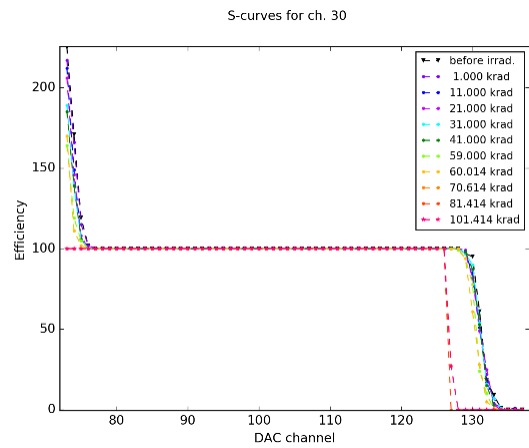
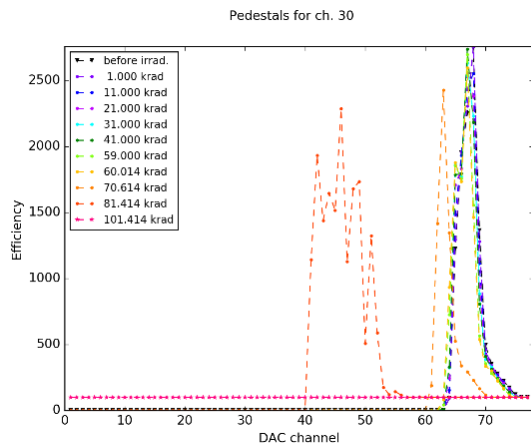
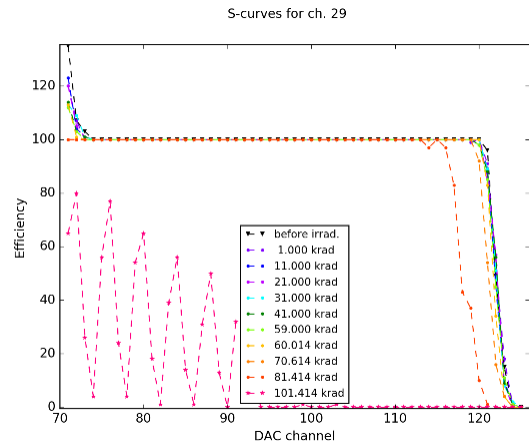
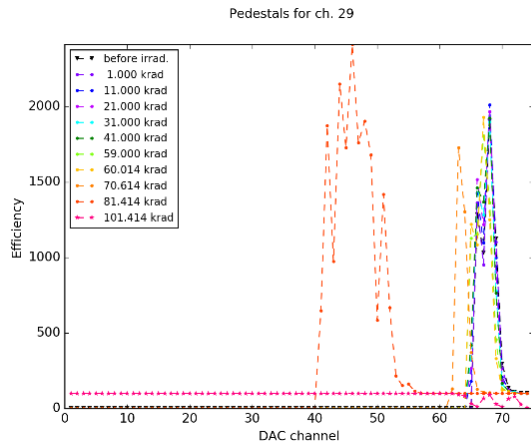
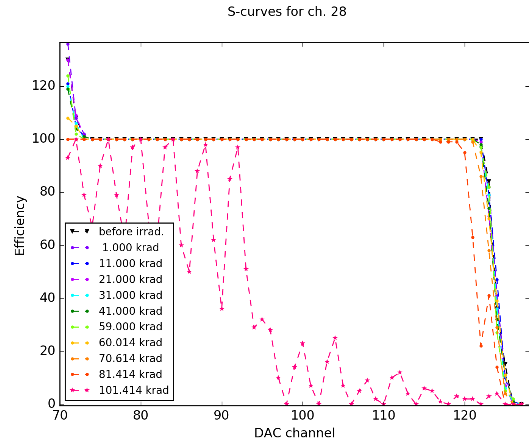
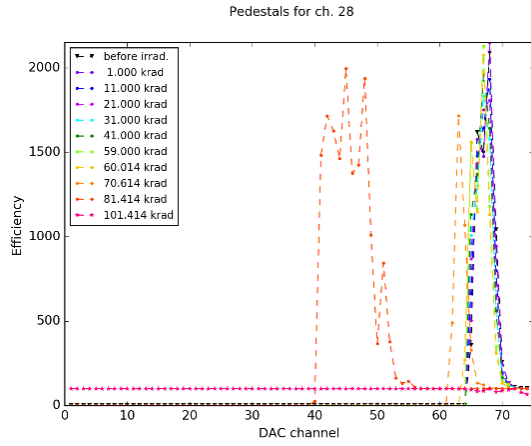


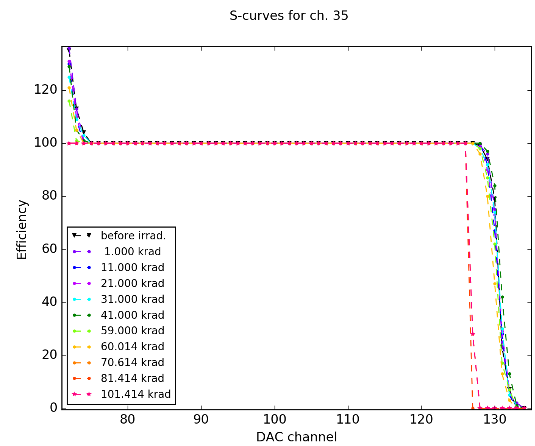
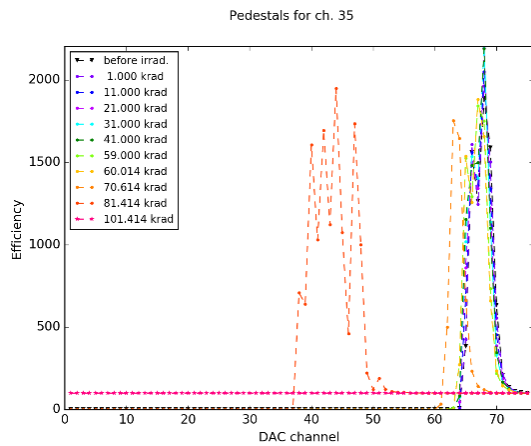
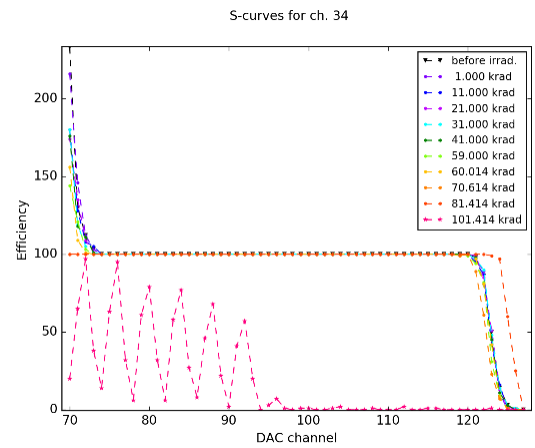
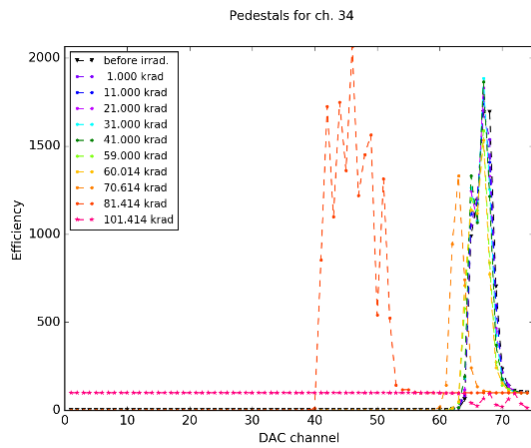
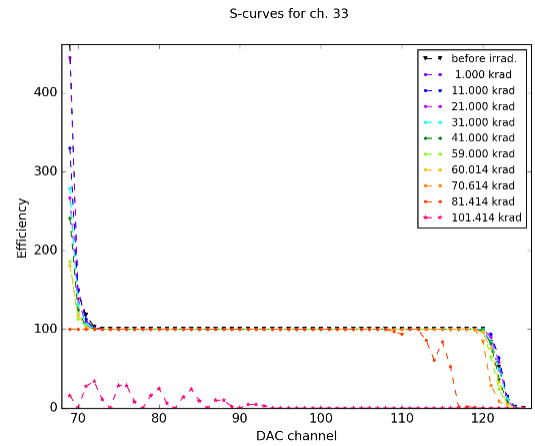
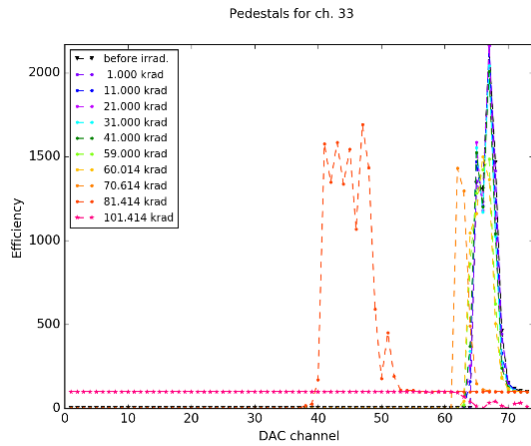
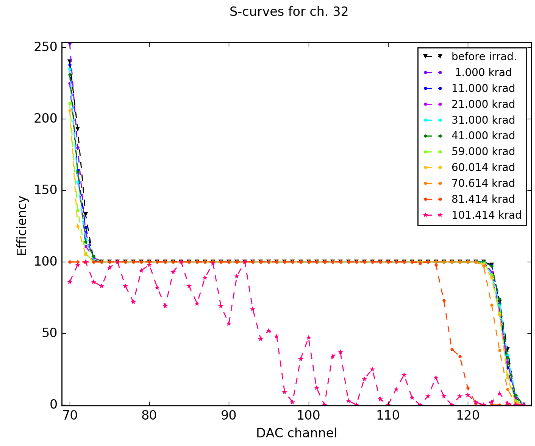
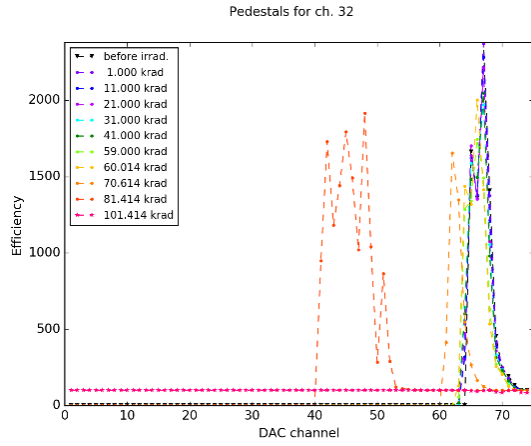


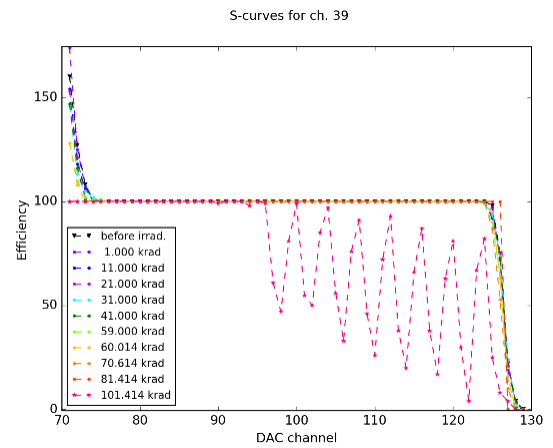
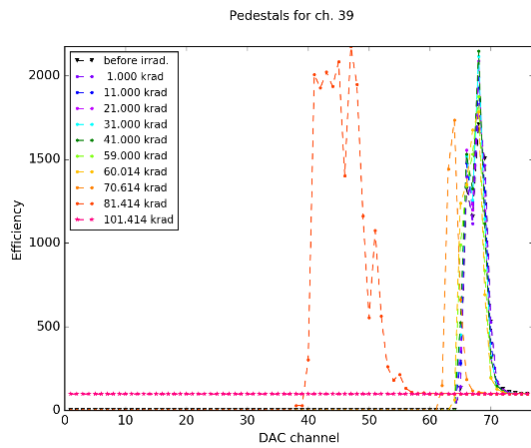
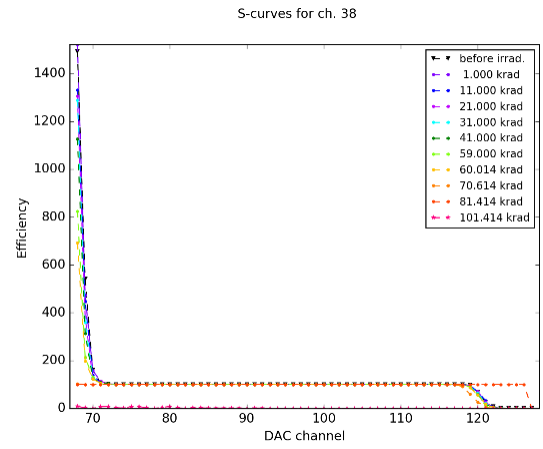
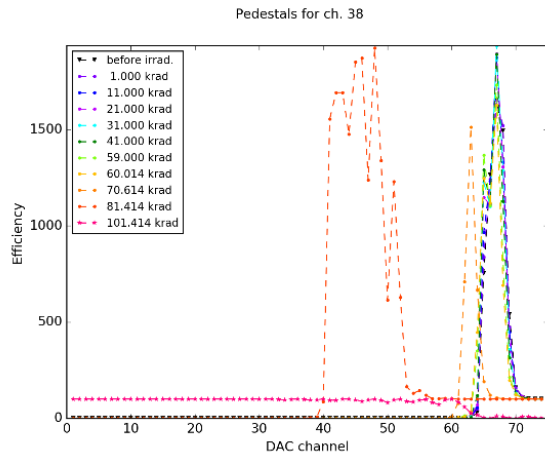
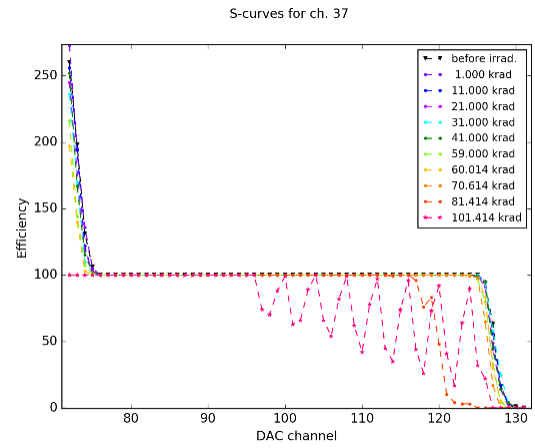
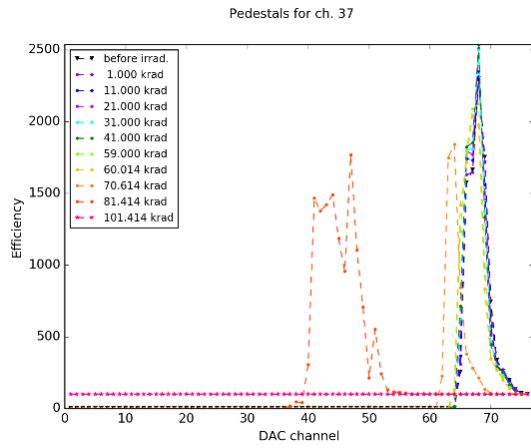
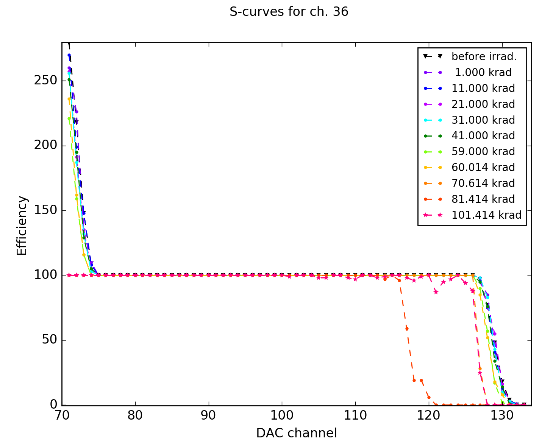
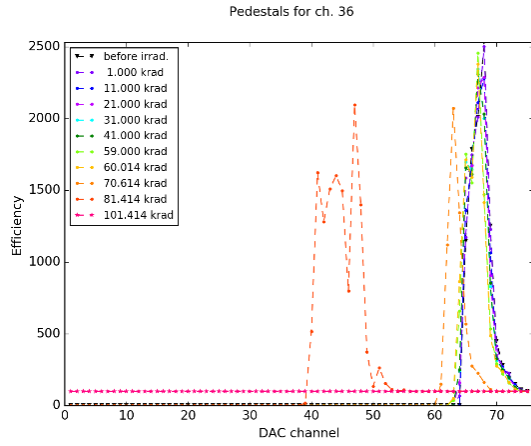


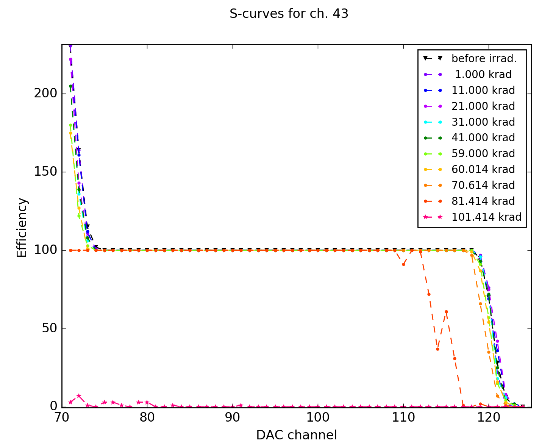
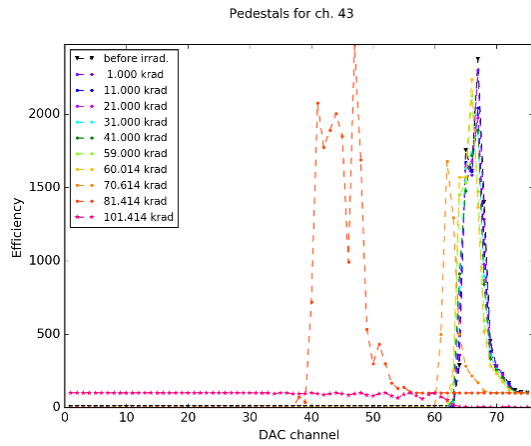
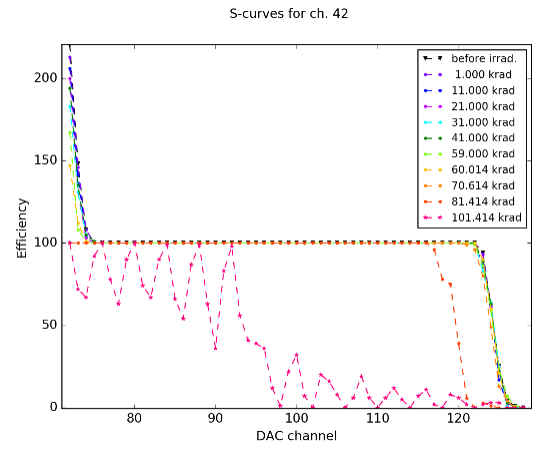
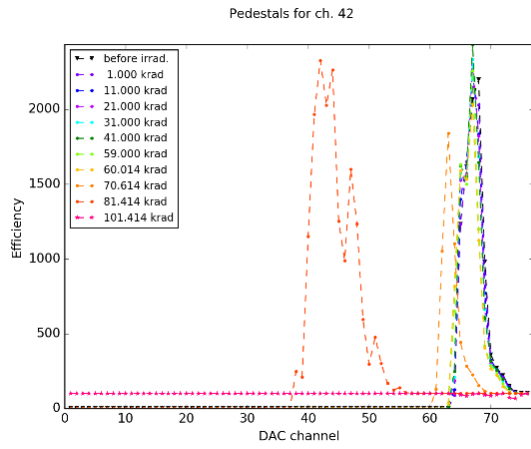
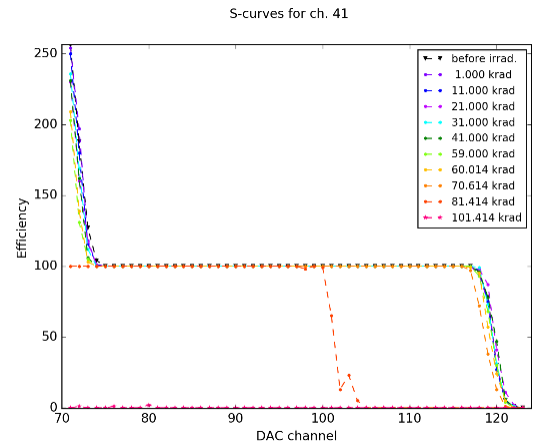
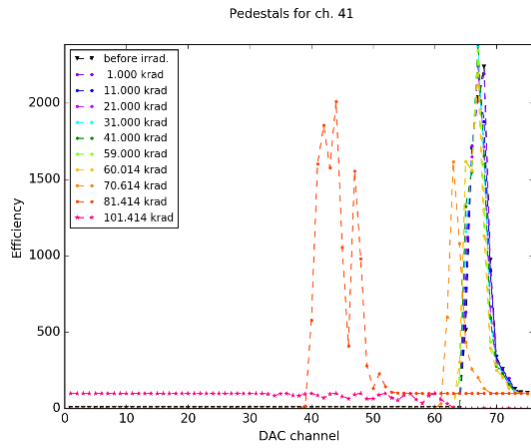
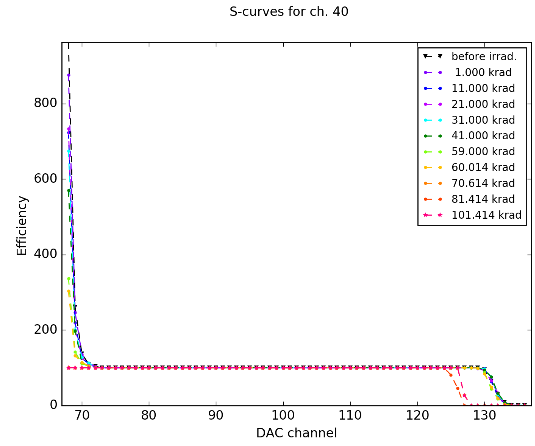
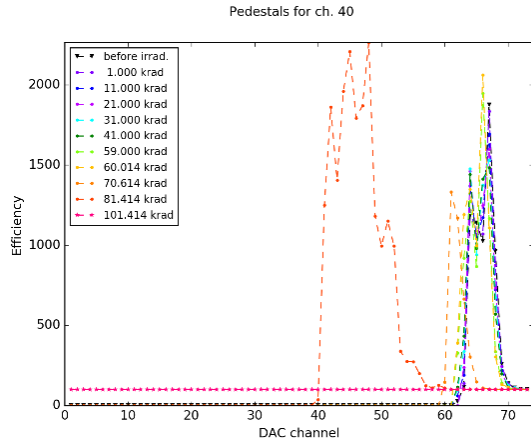


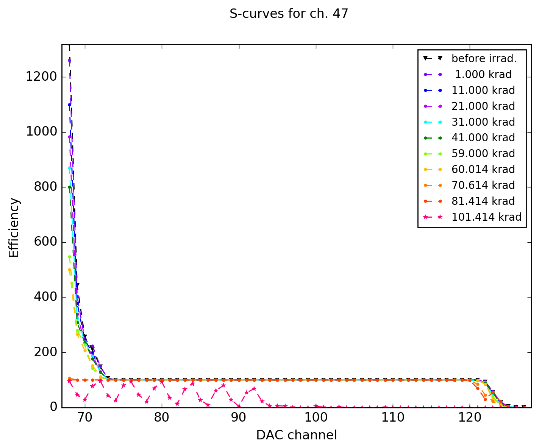
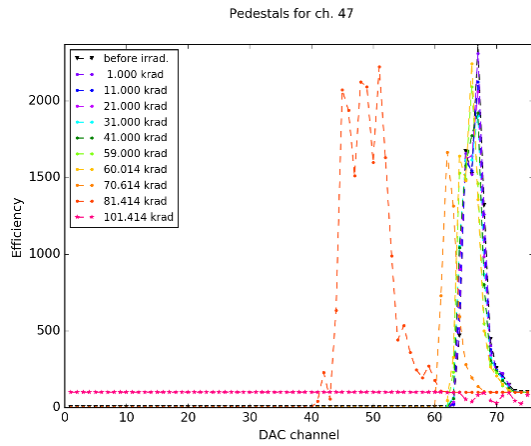
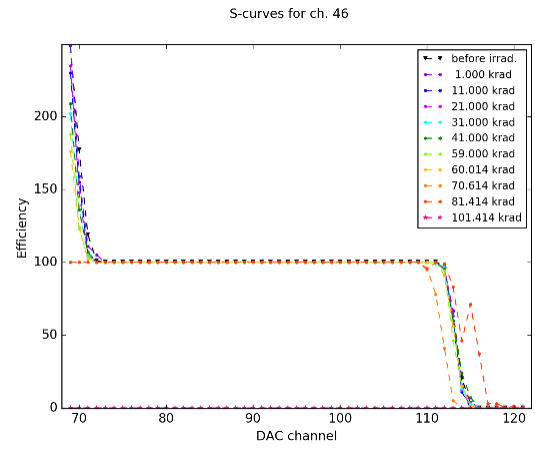
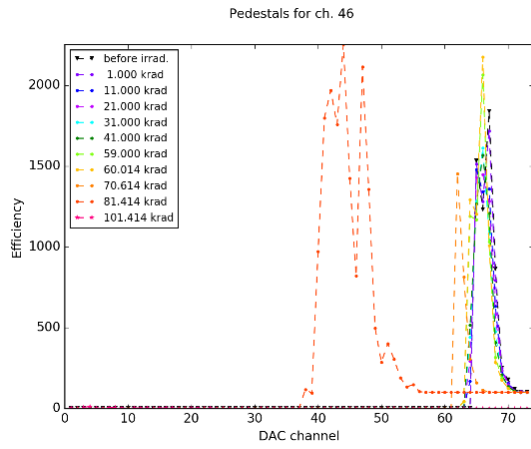
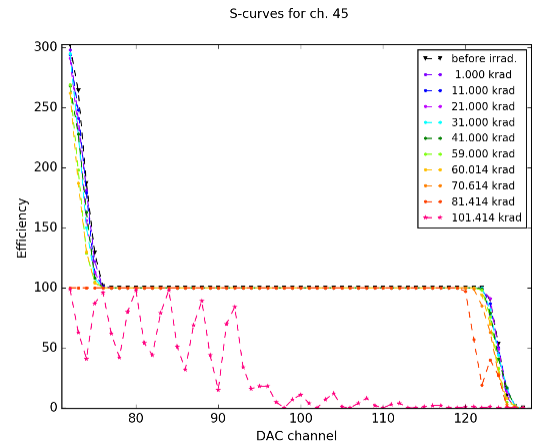
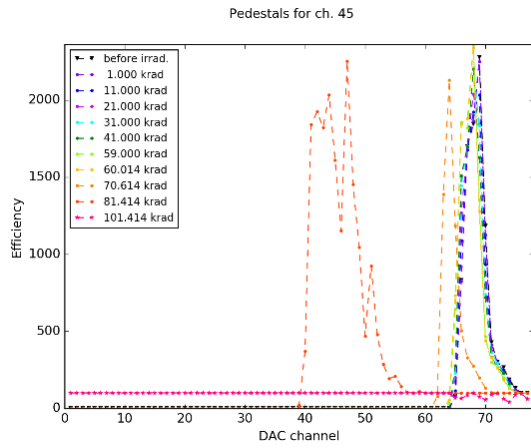
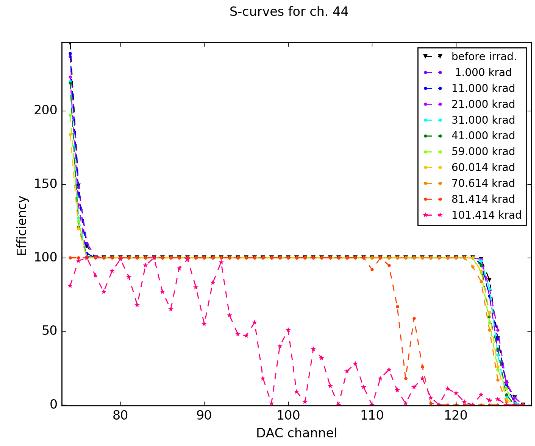
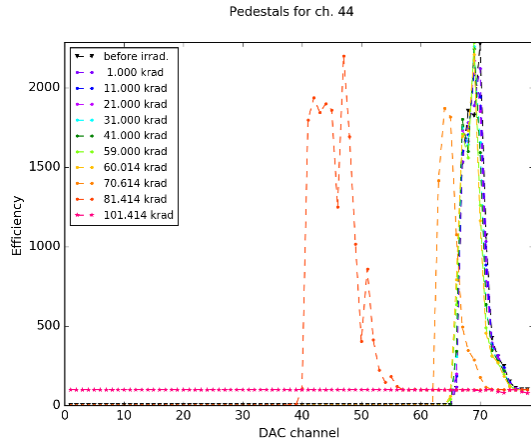


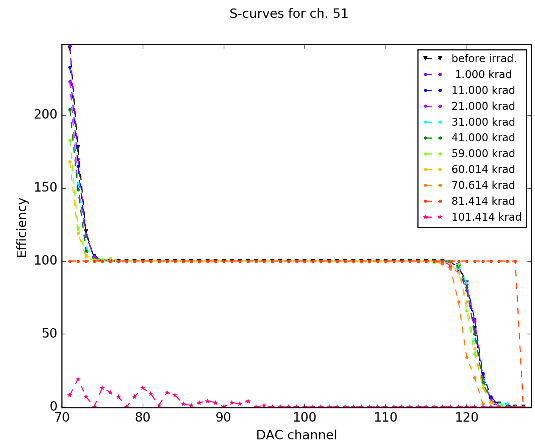
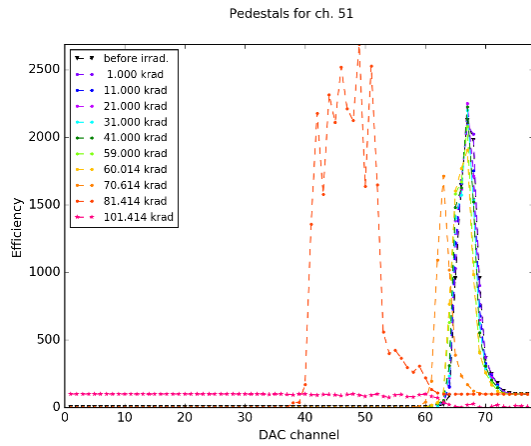
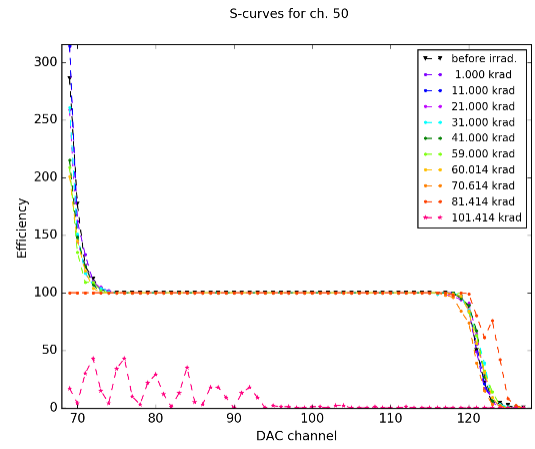
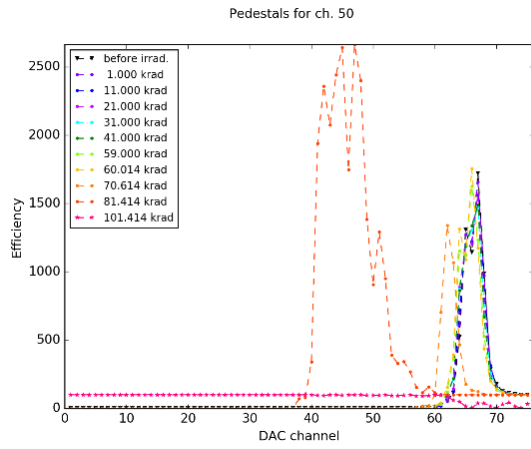
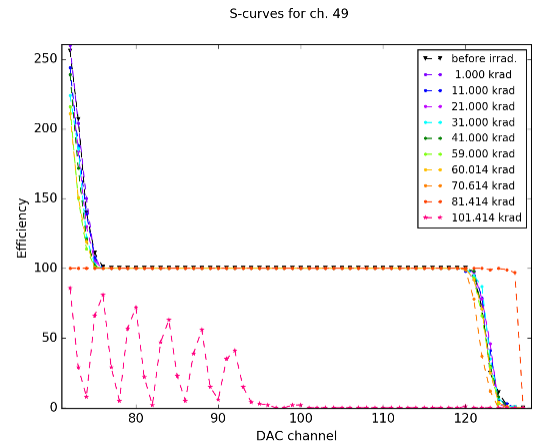
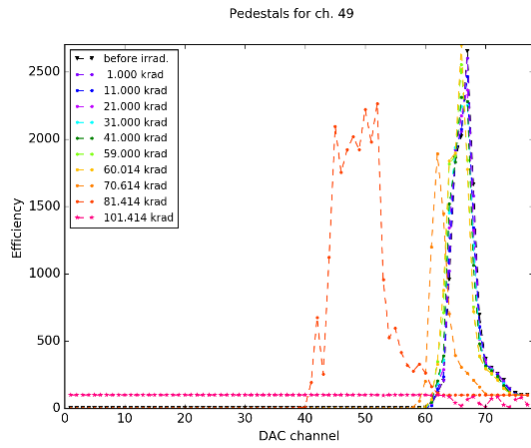
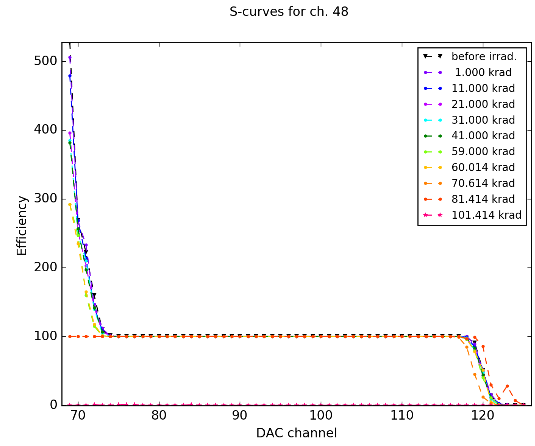
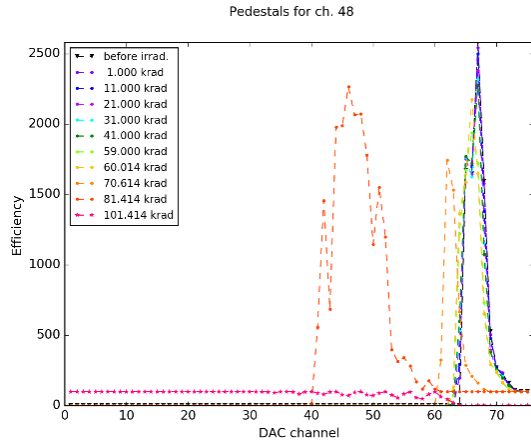


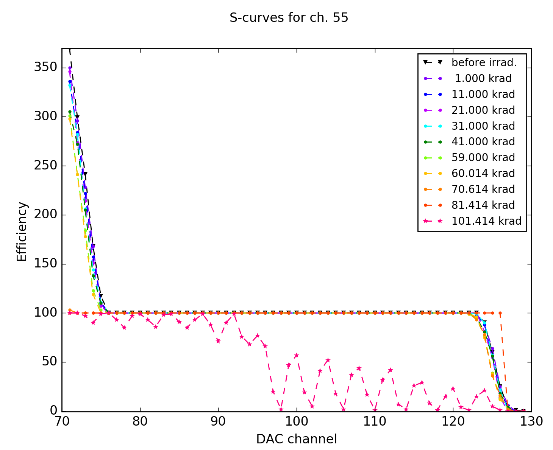
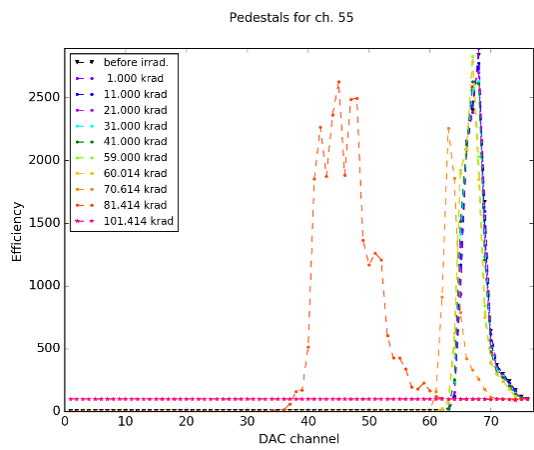
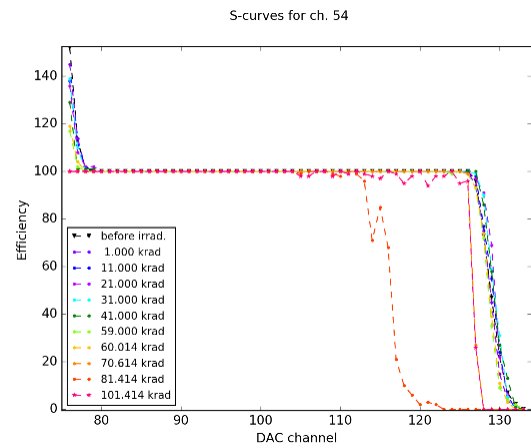
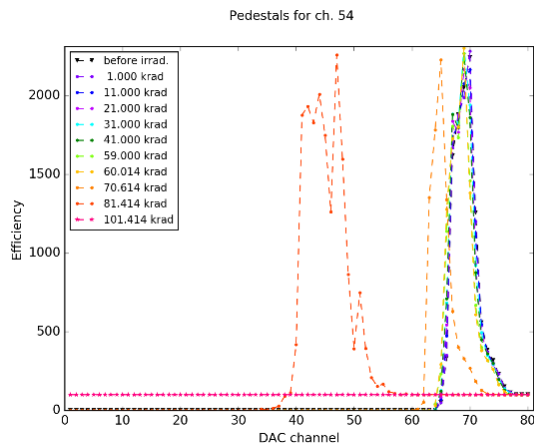
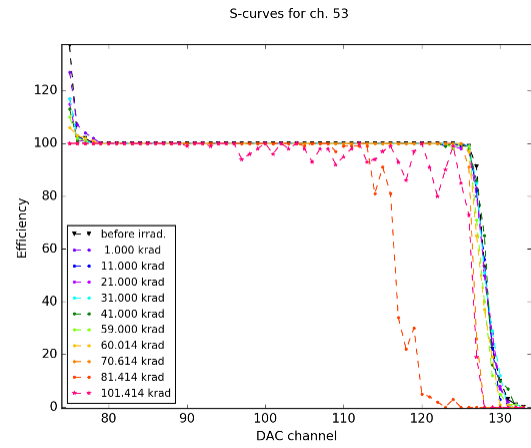
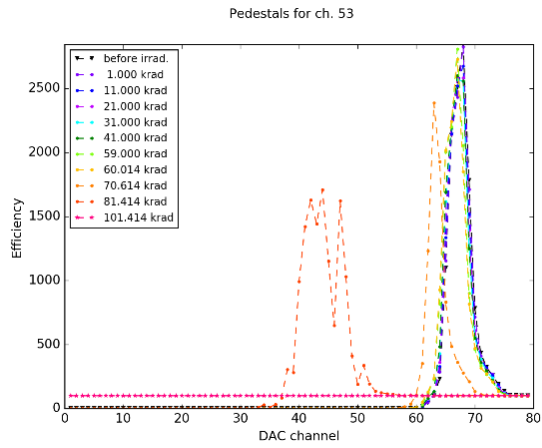
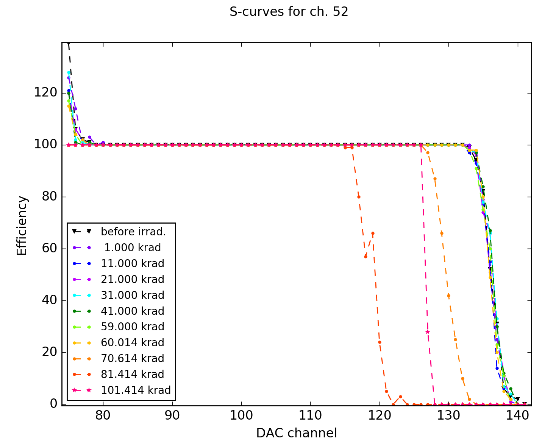
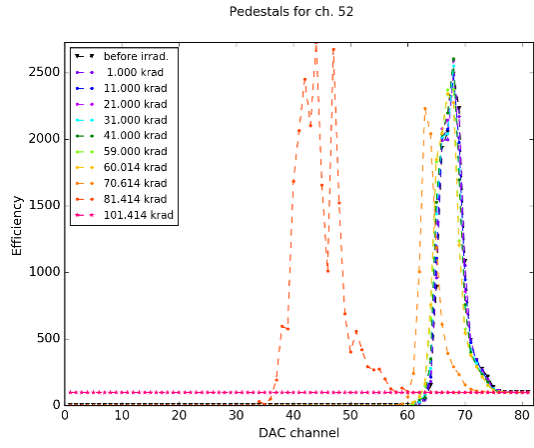


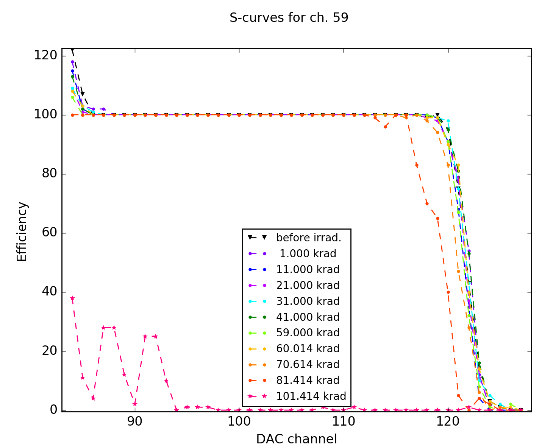
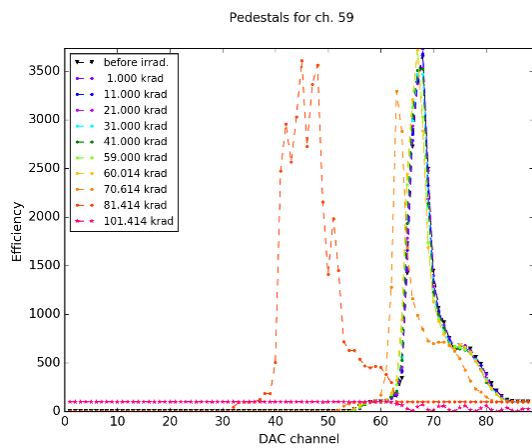
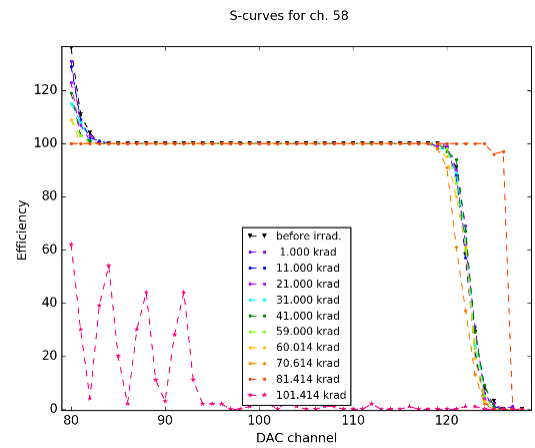
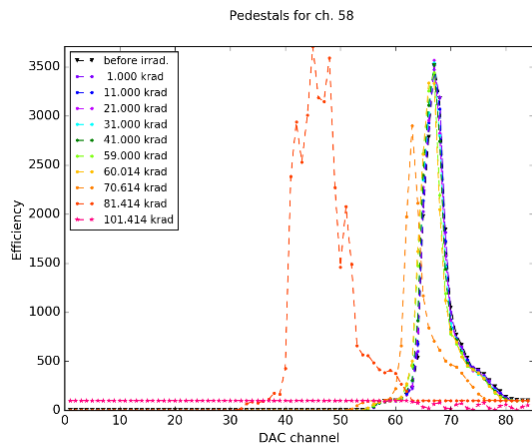
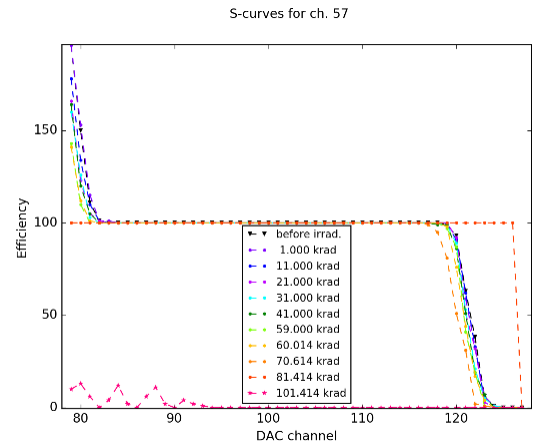
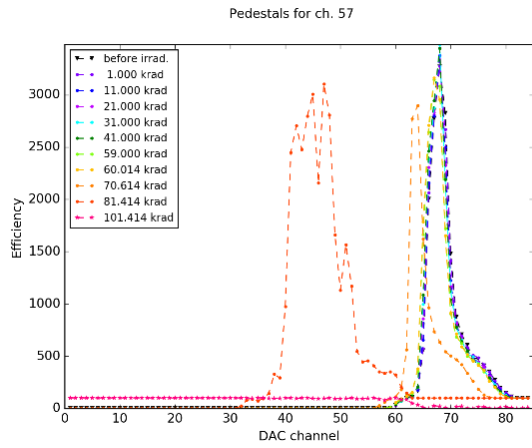
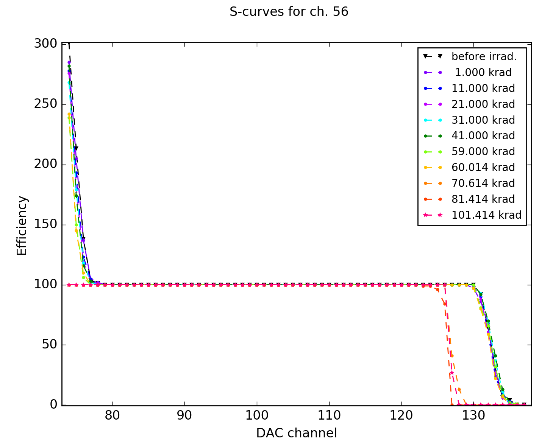
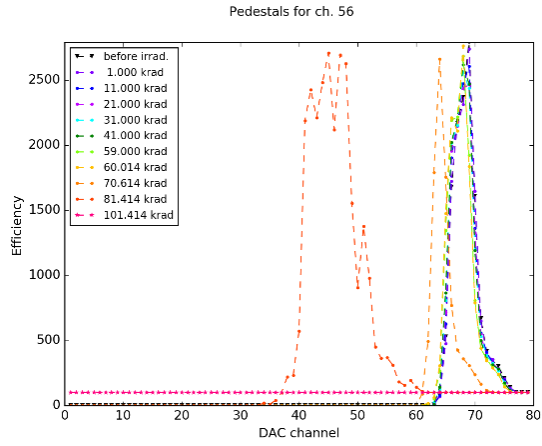


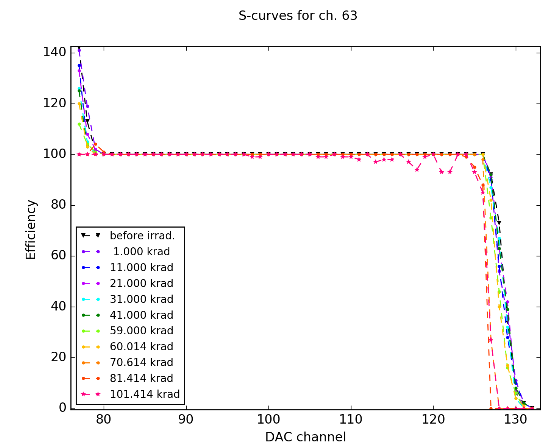
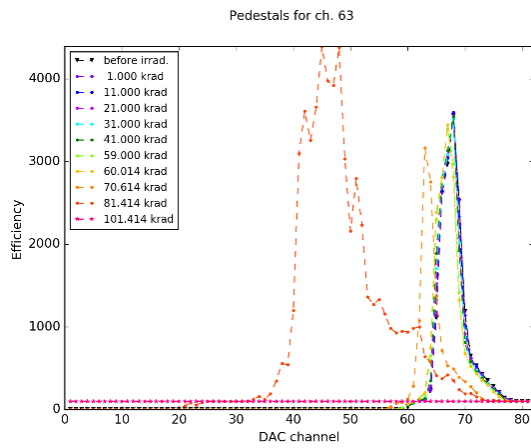
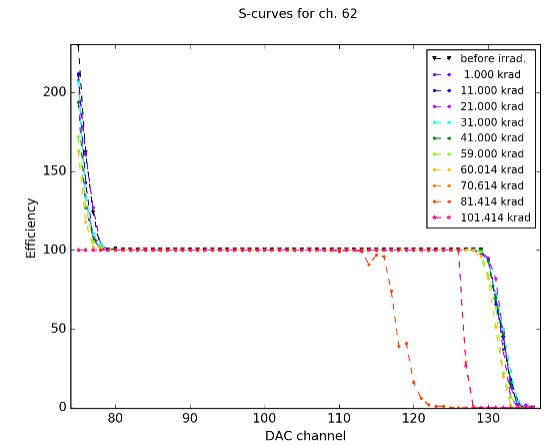
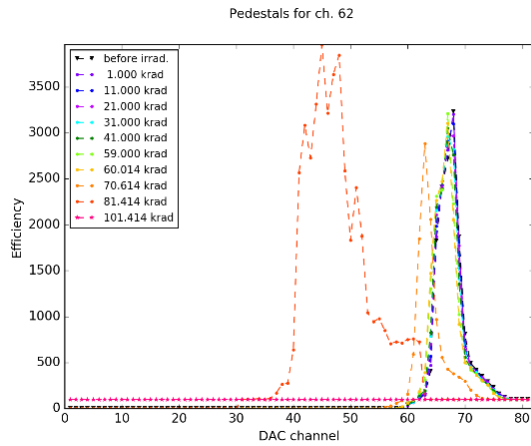
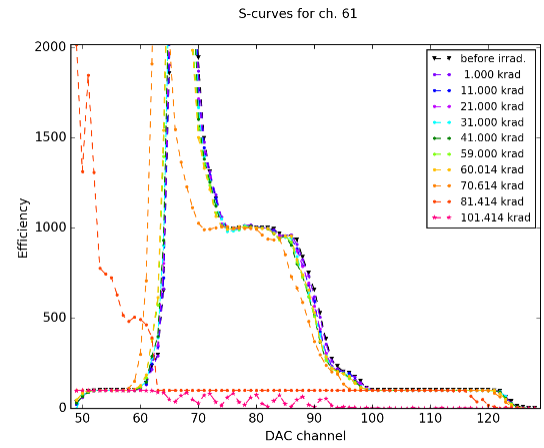
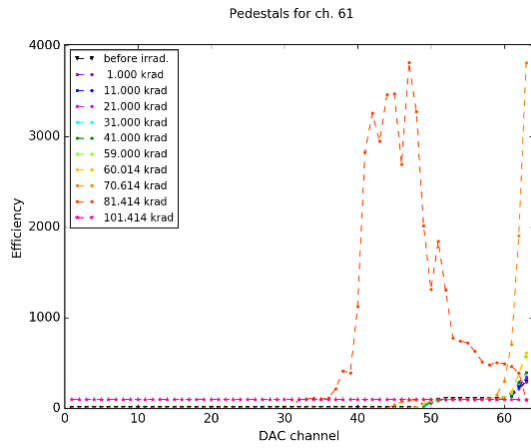
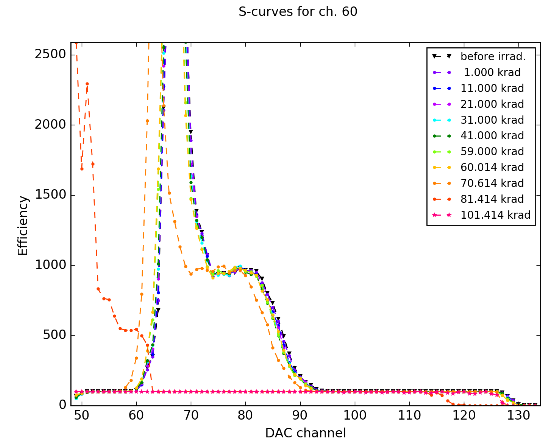
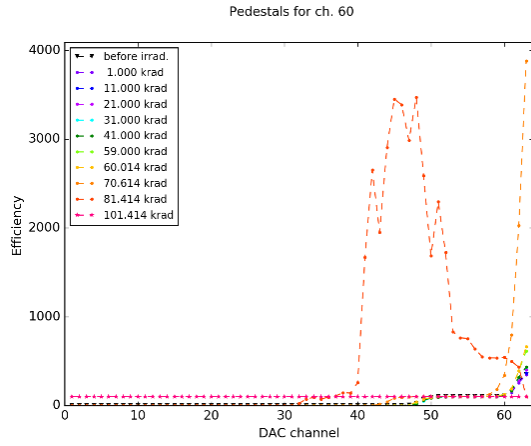


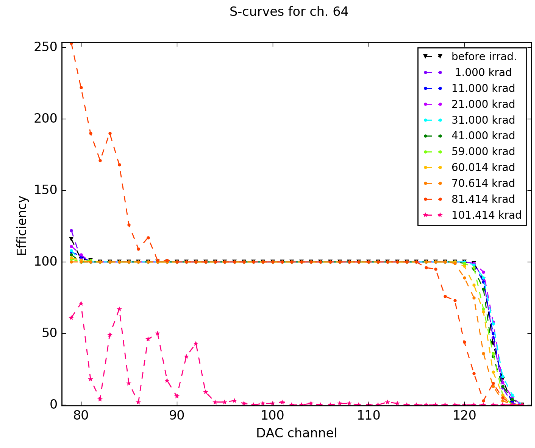
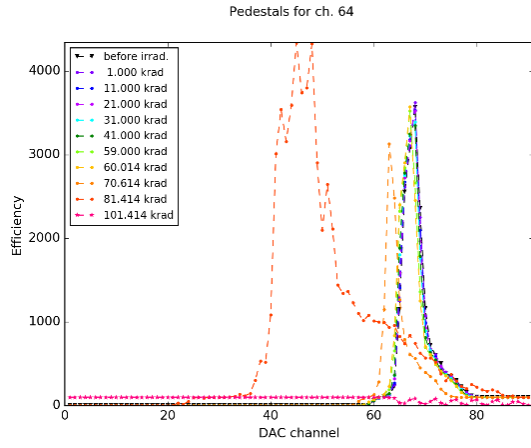




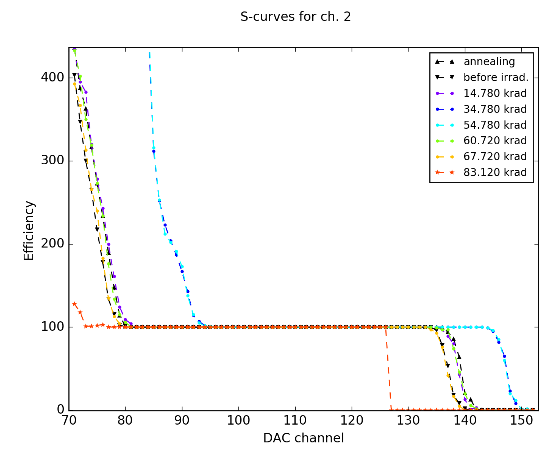
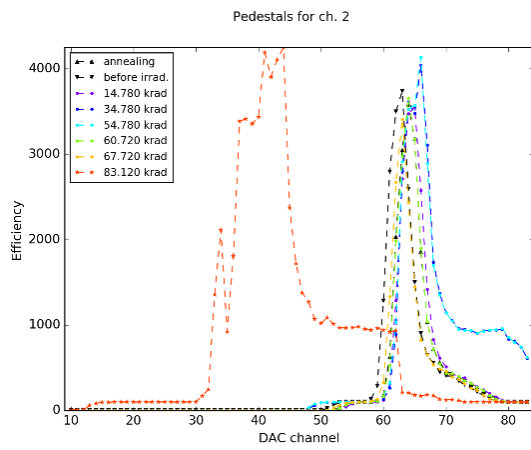
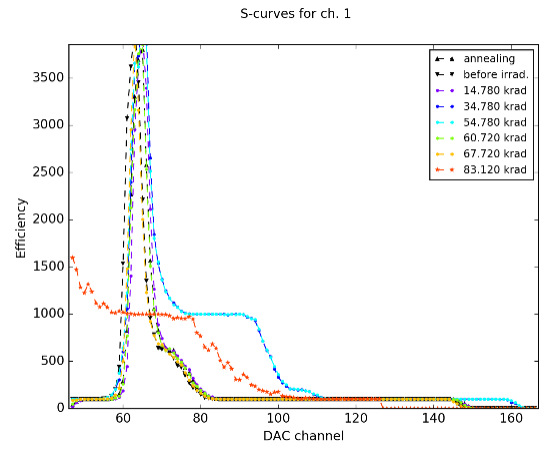
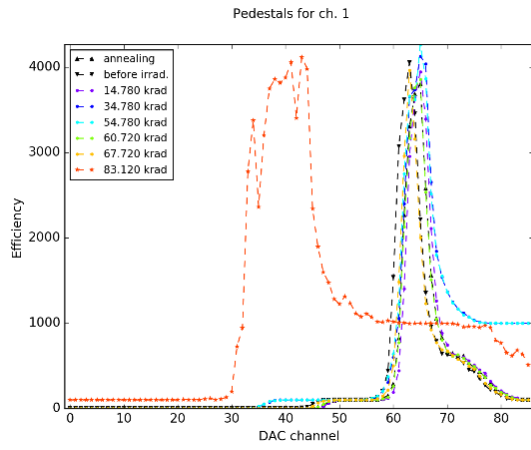


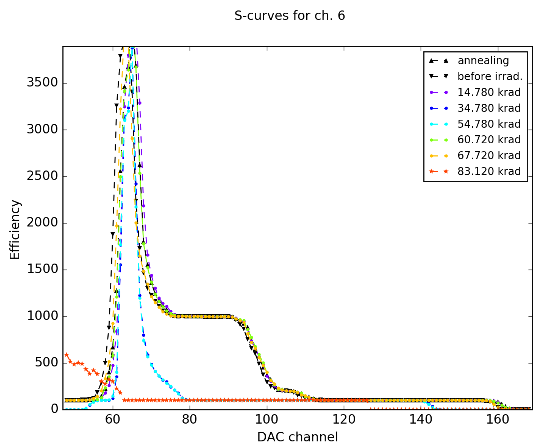
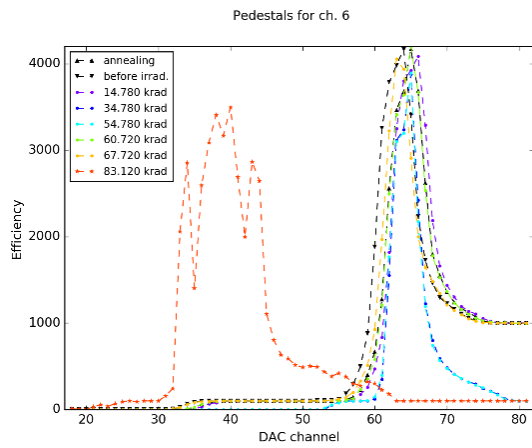
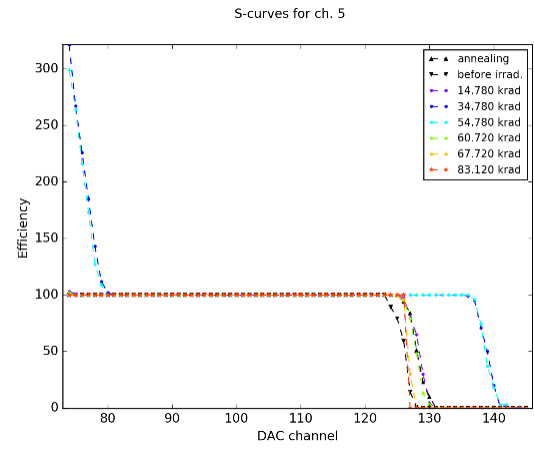
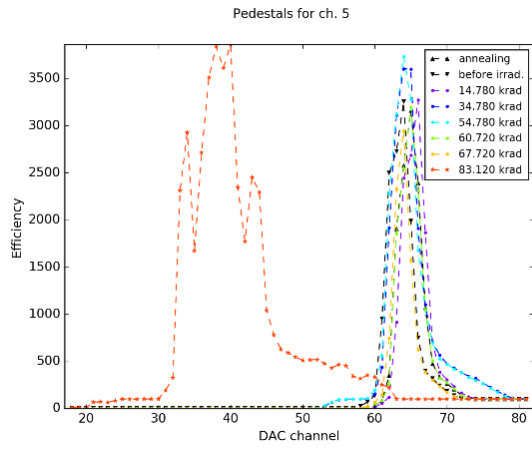
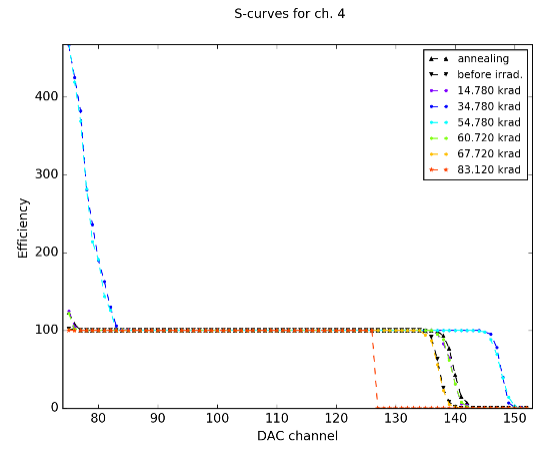
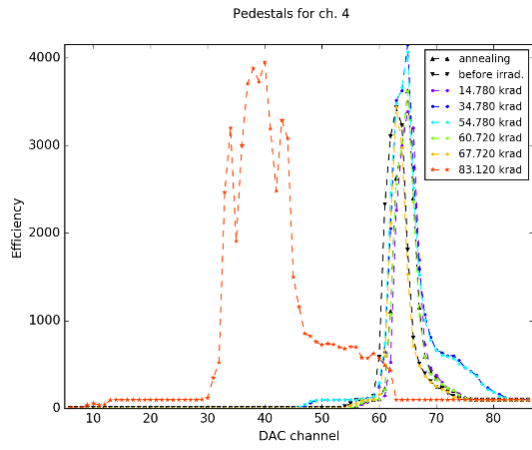
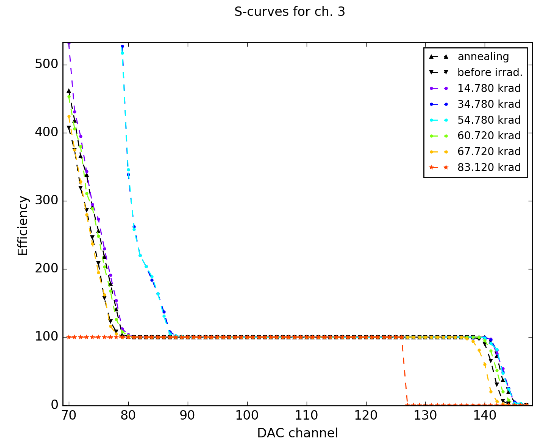
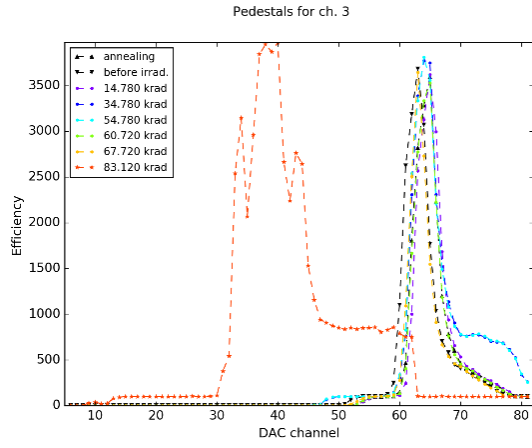


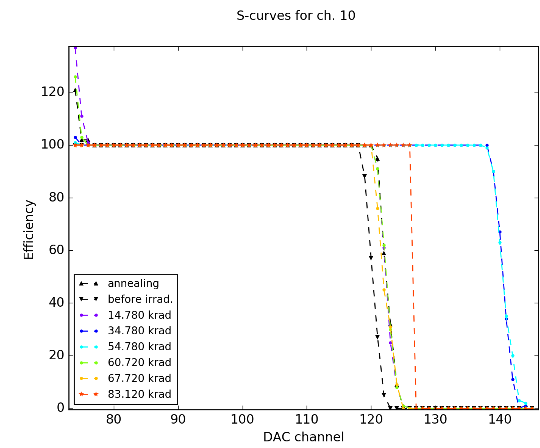
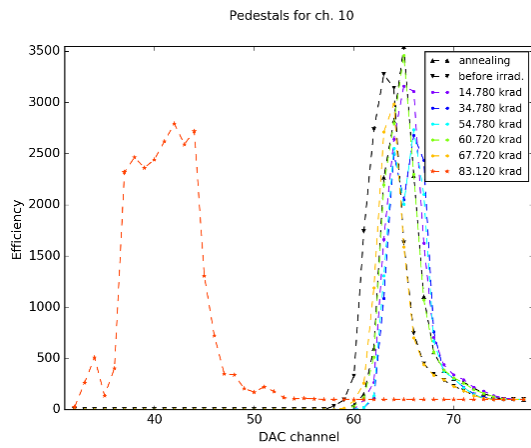
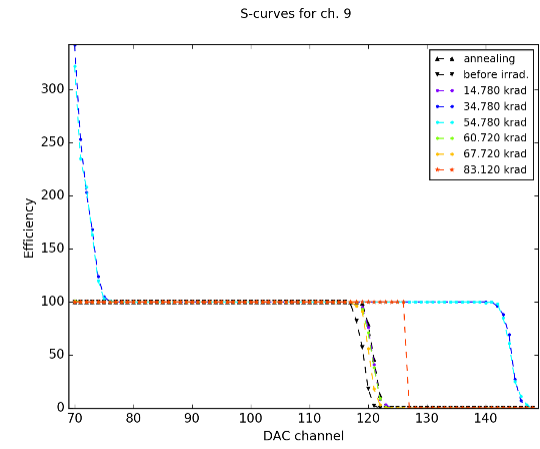
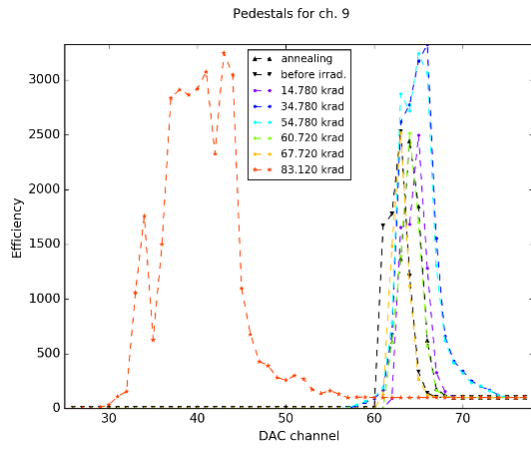
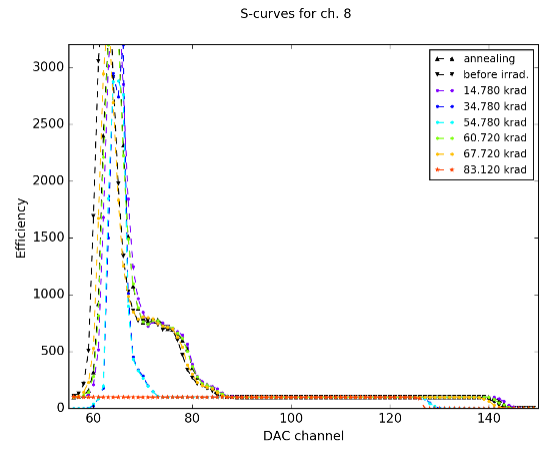
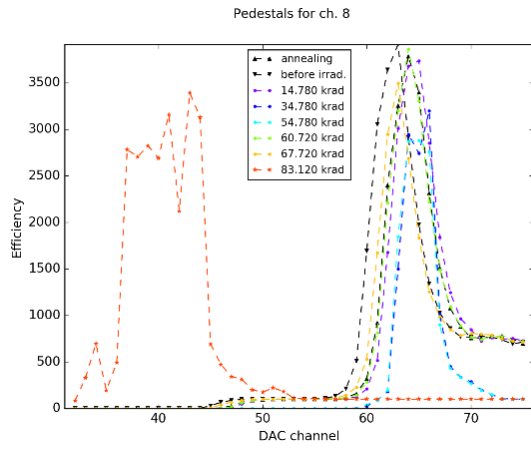
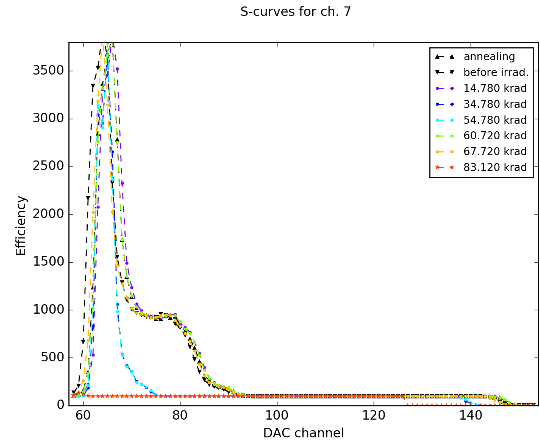
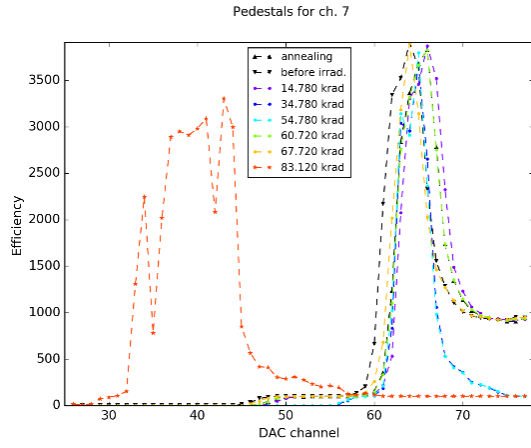


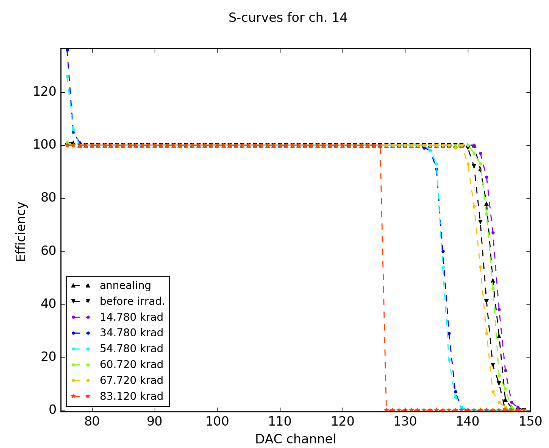
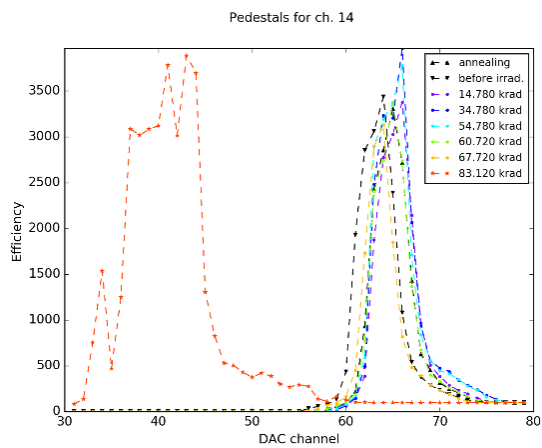
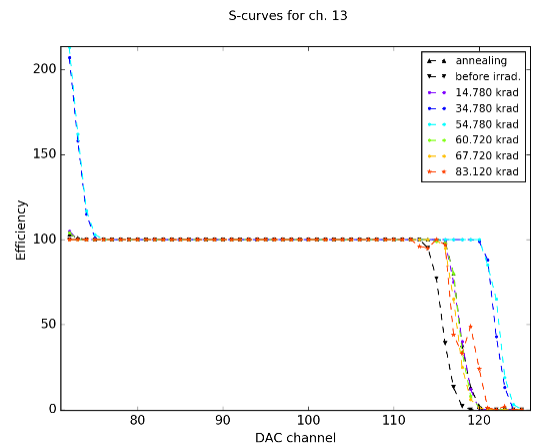
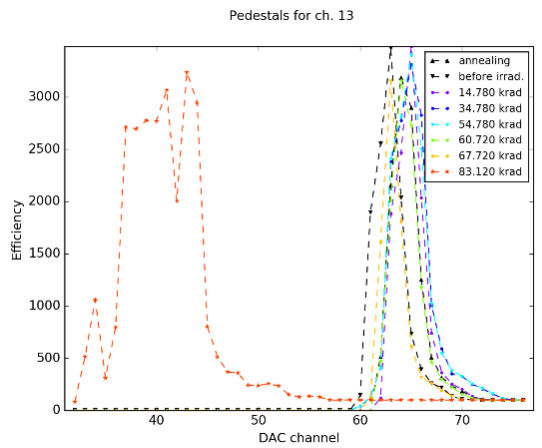
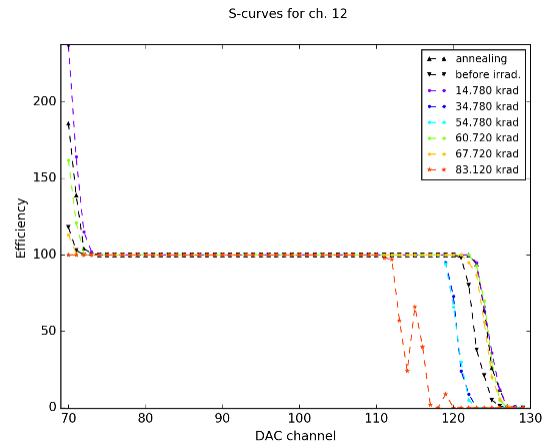
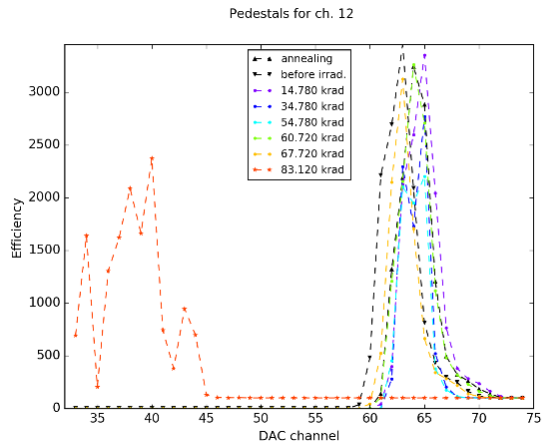
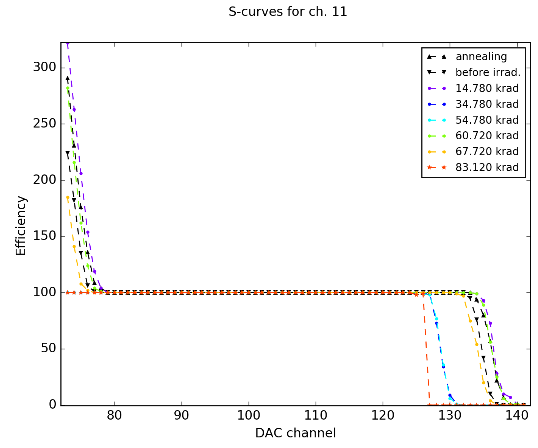
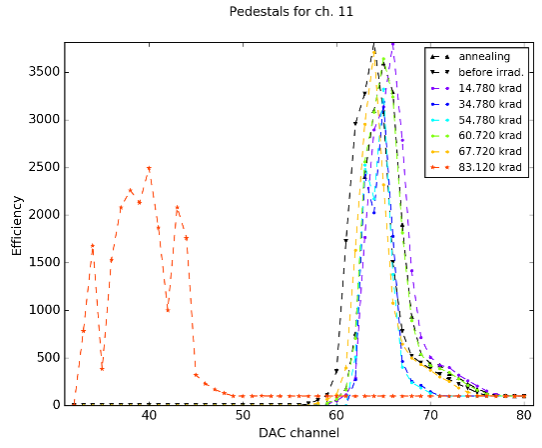


The trigger efficiency curves for the third irradiated SPACIROC2 chip.

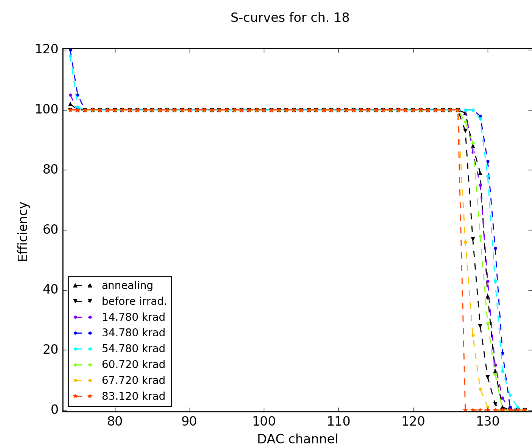
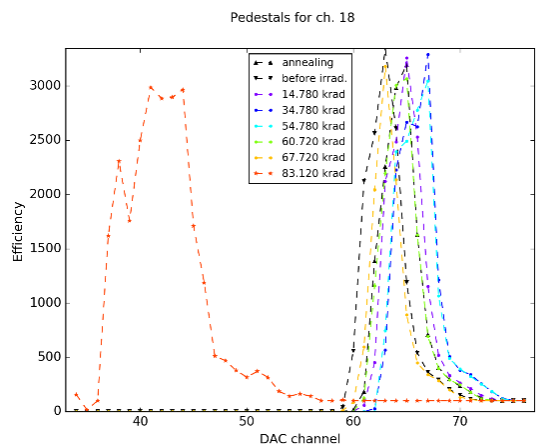
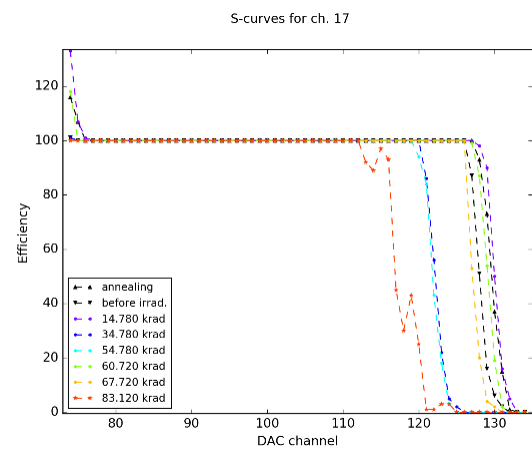
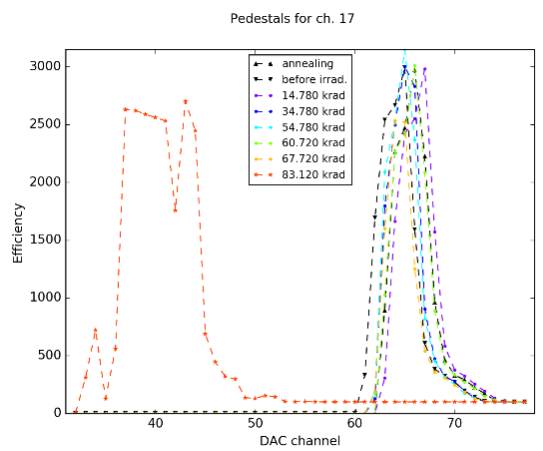
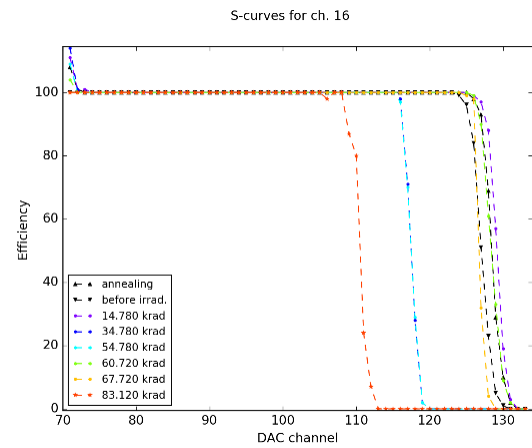
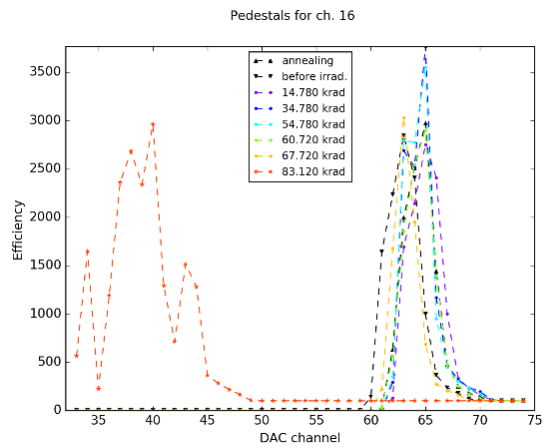
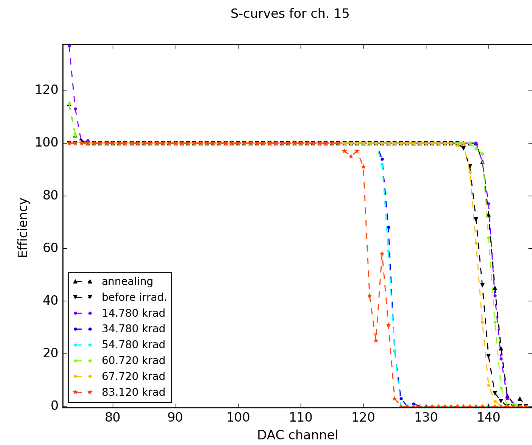
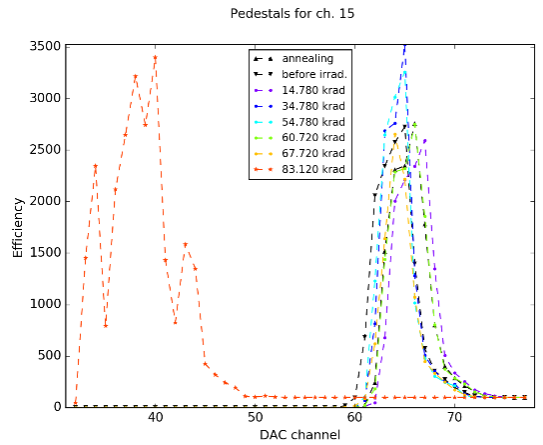


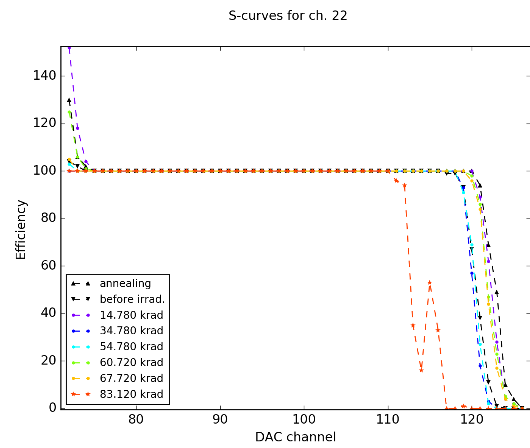
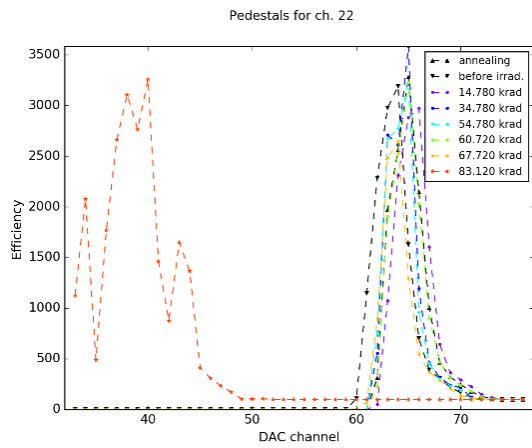
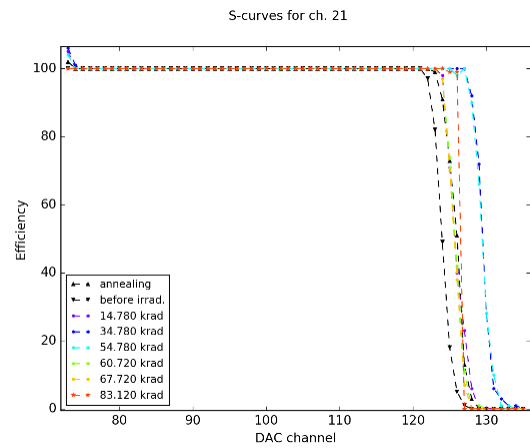
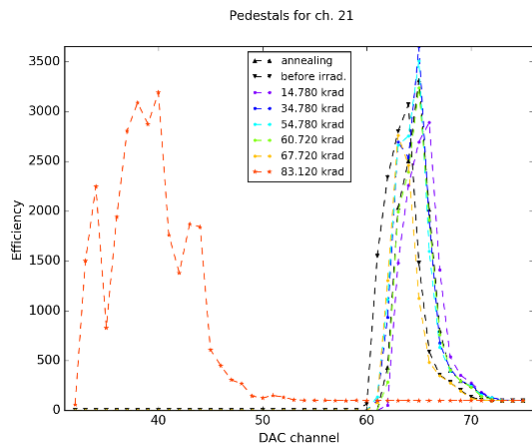
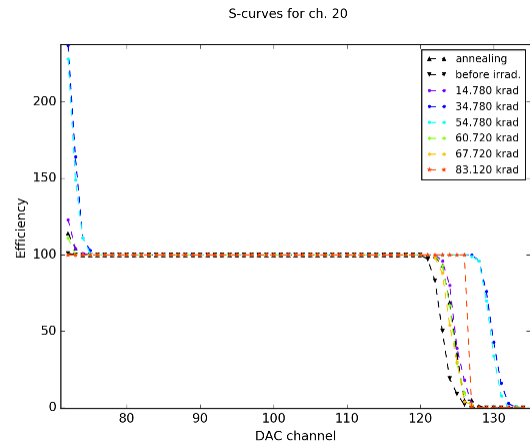
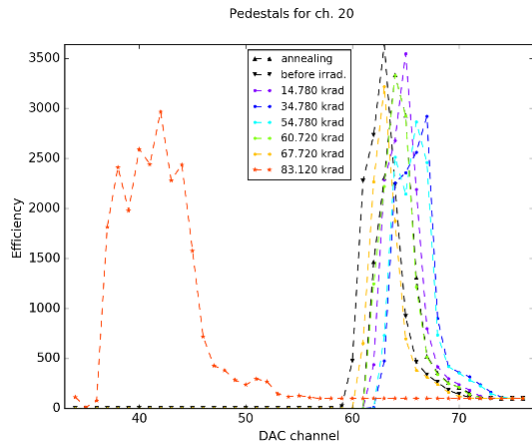
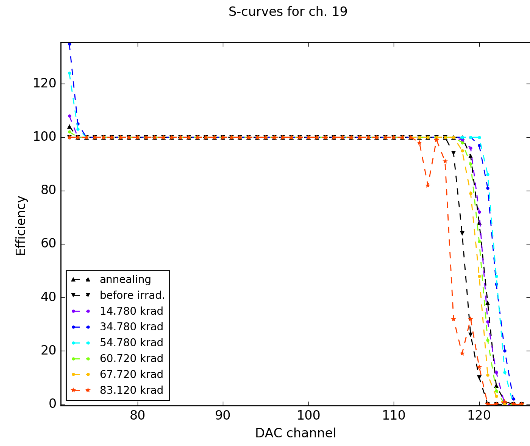
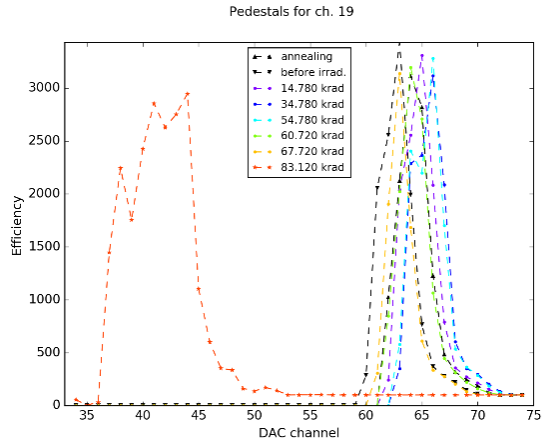


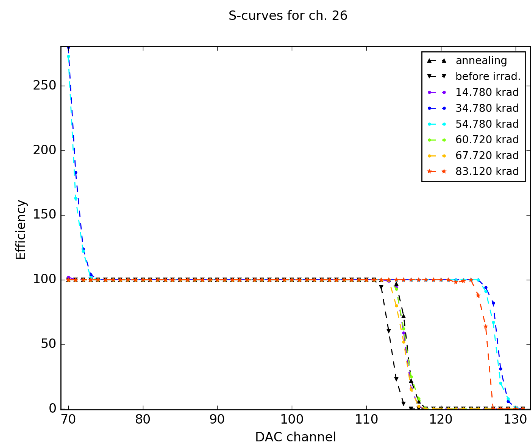
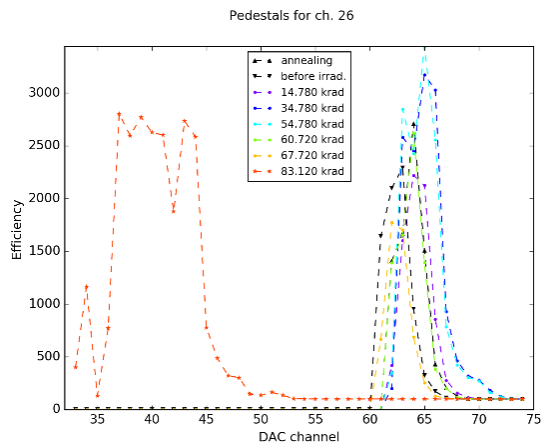
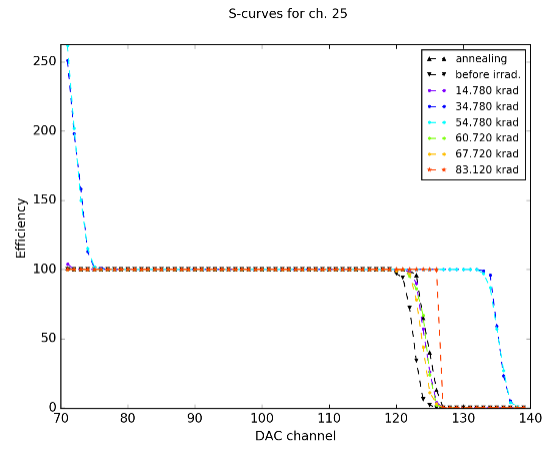
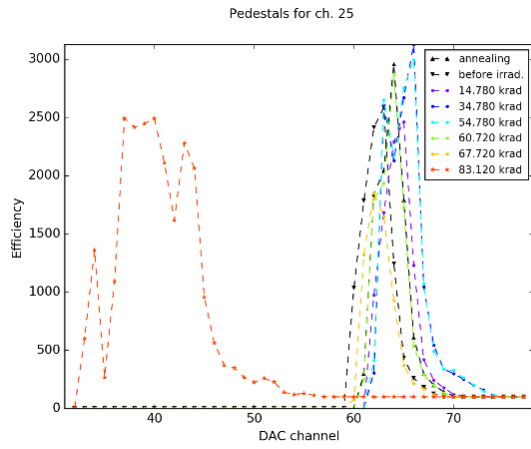
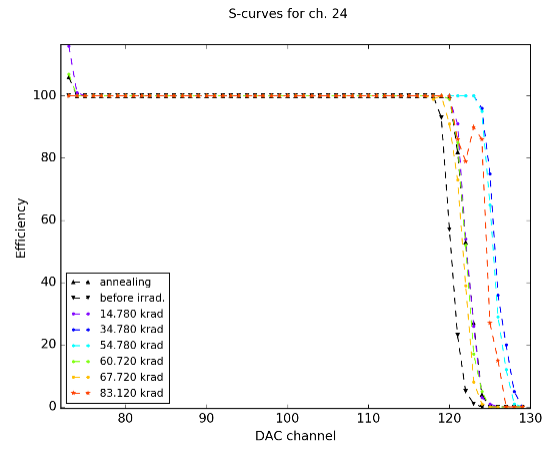
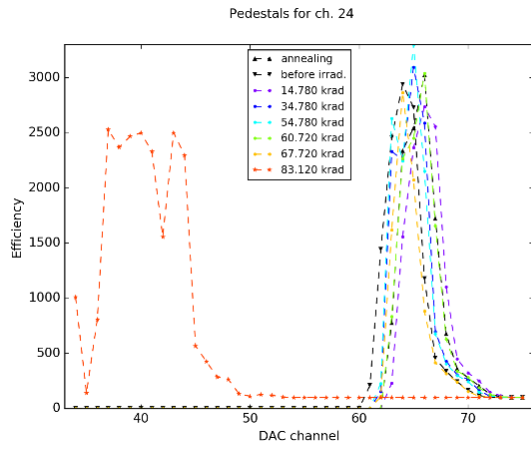
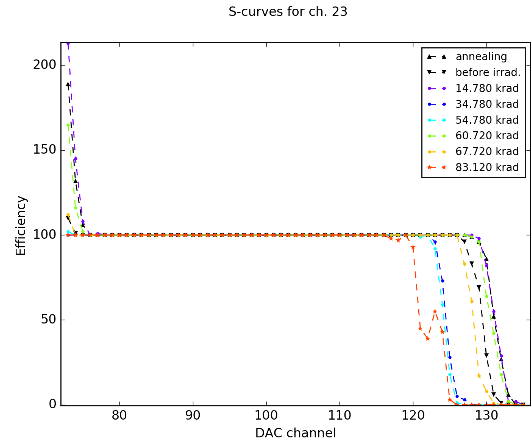
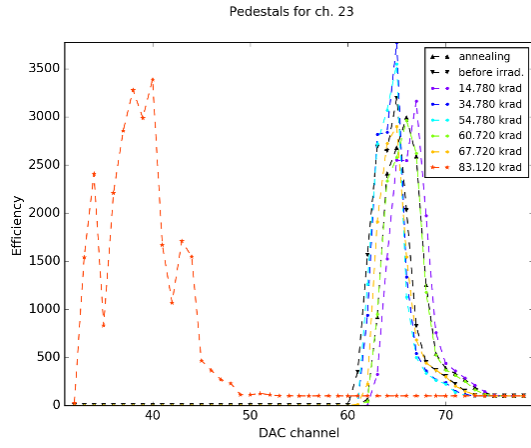


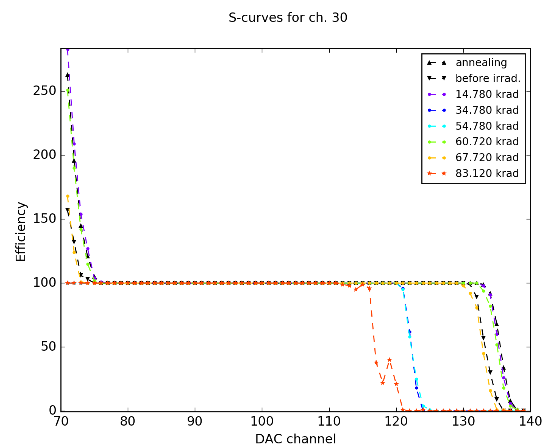
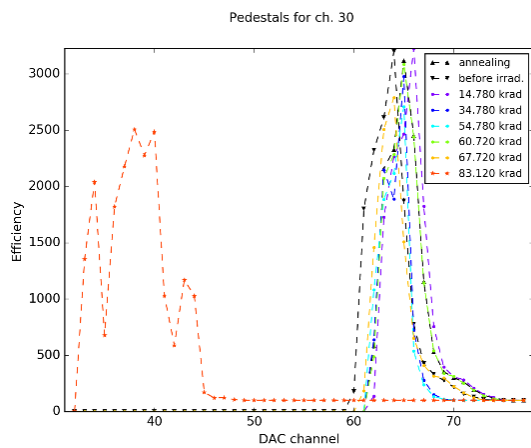
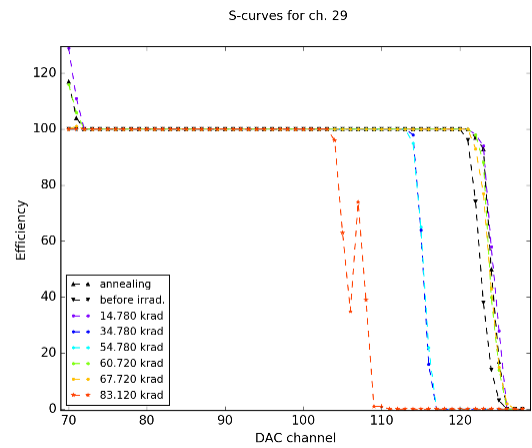
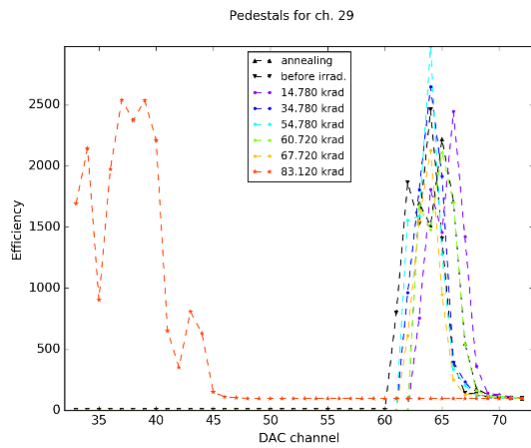
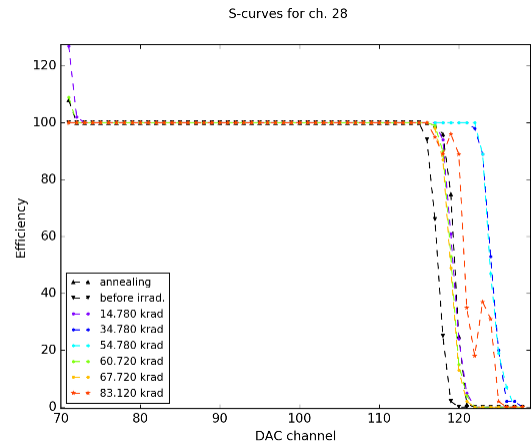
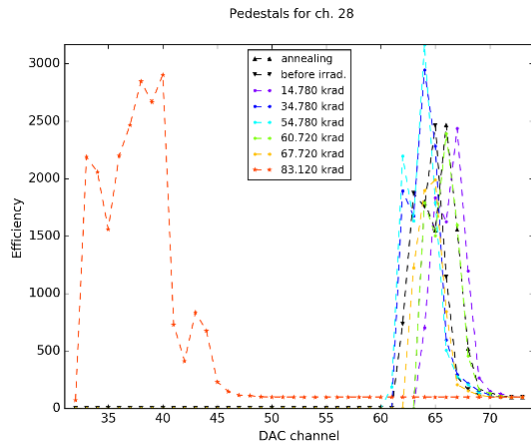
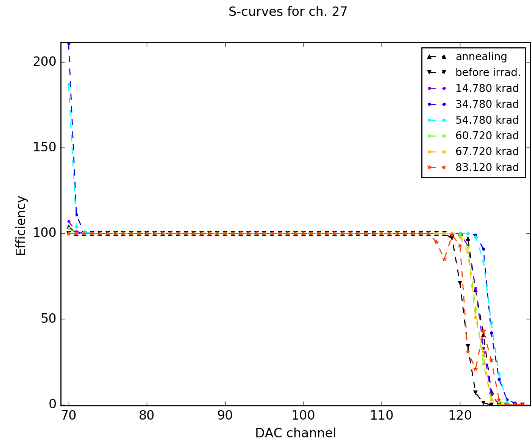
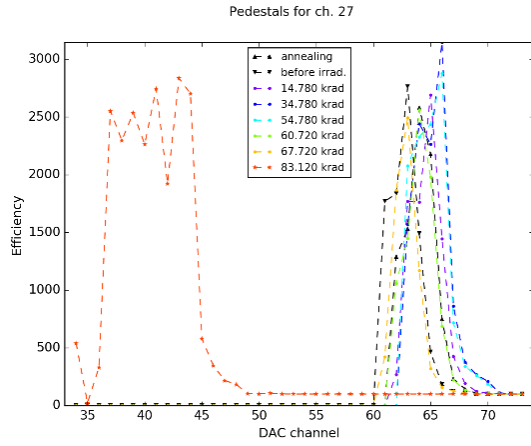


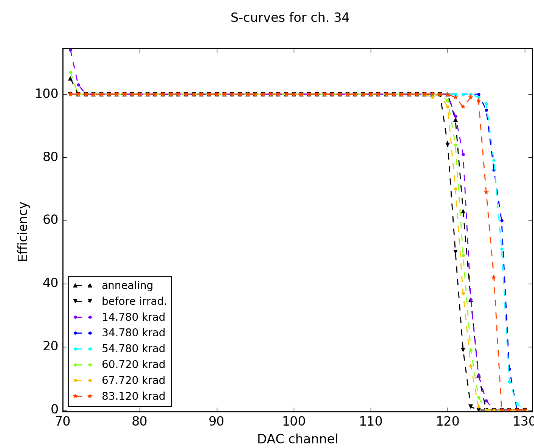
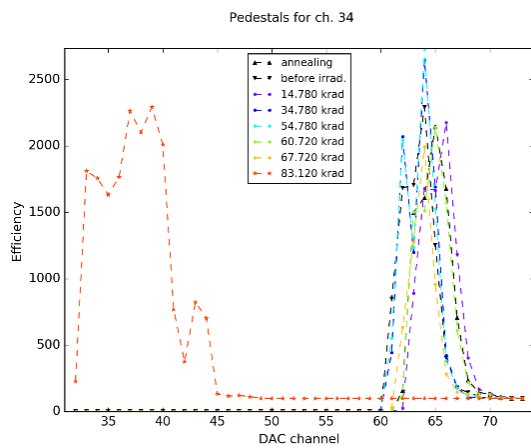
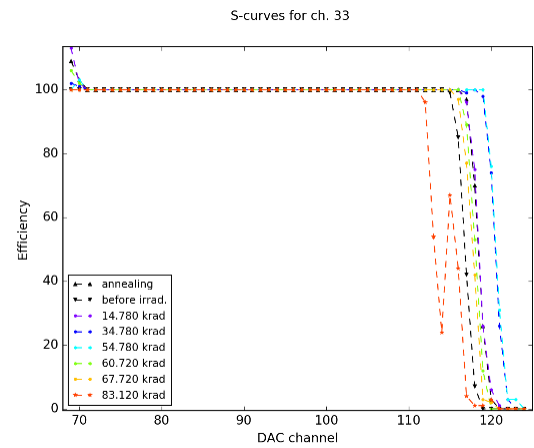
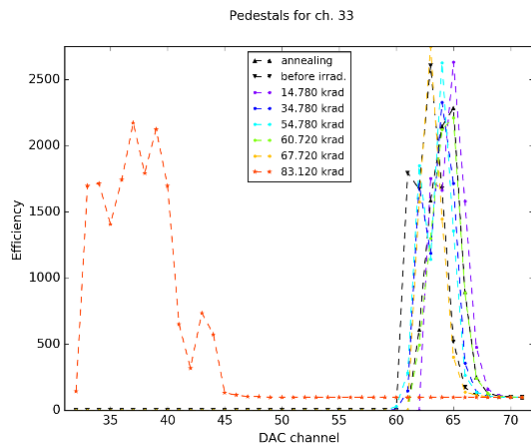
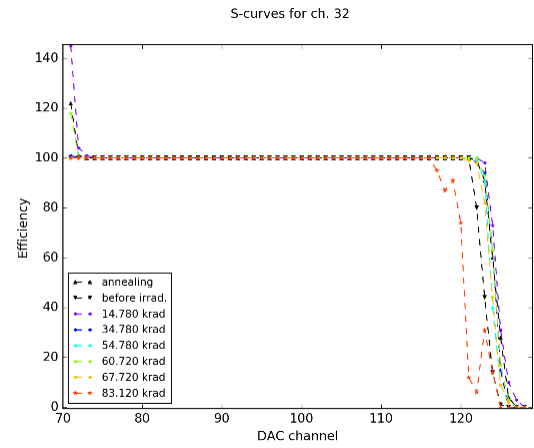
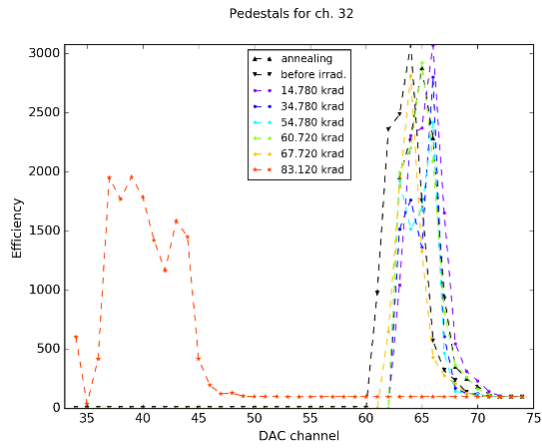
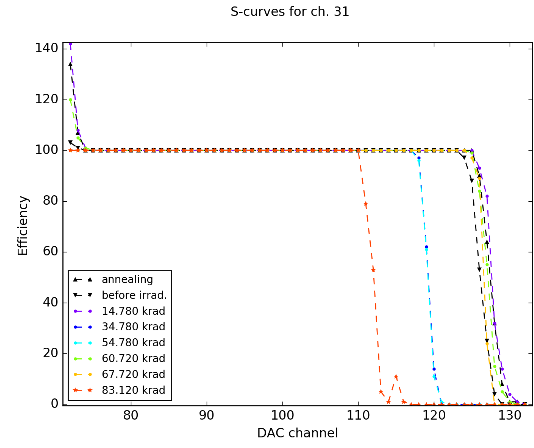
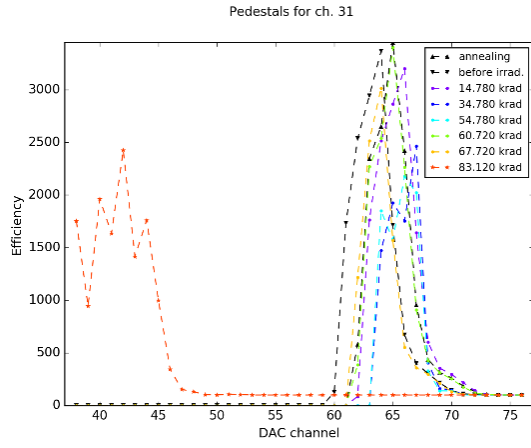
APPENDIX

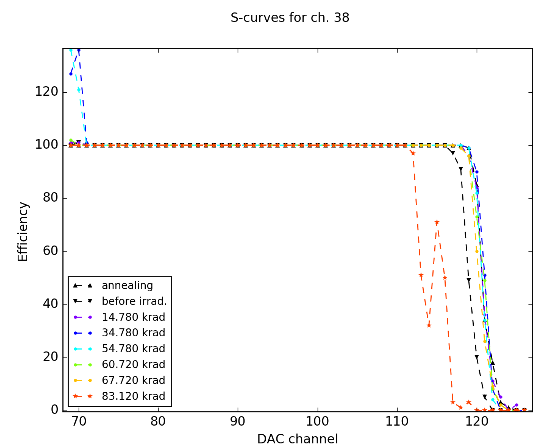
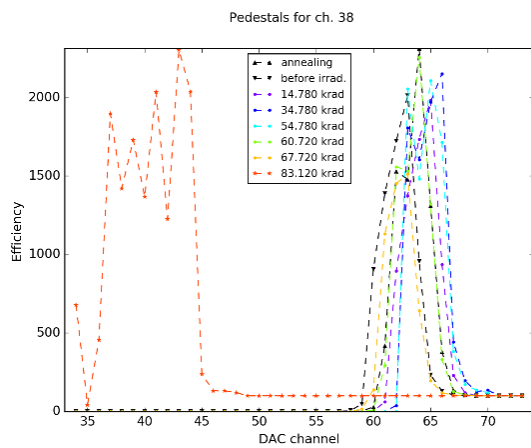
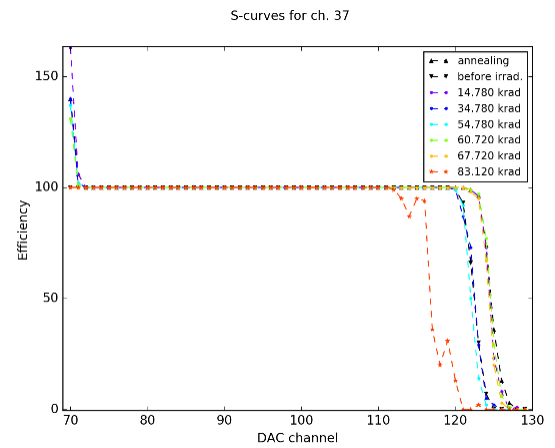
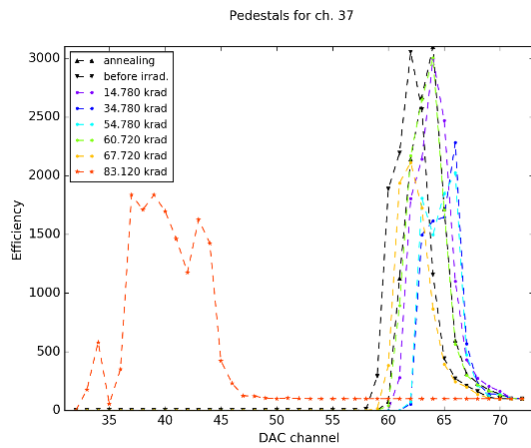
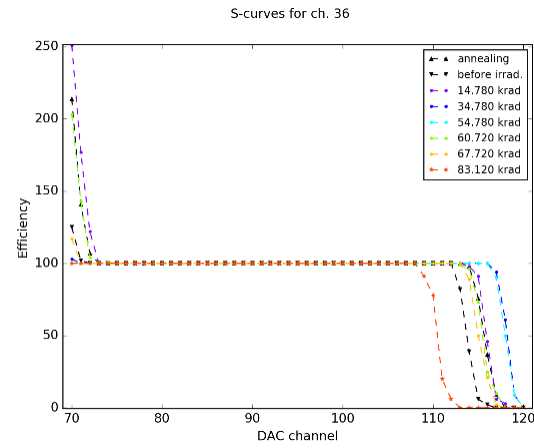
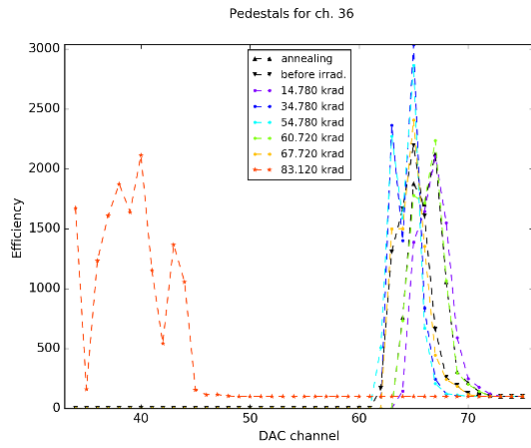
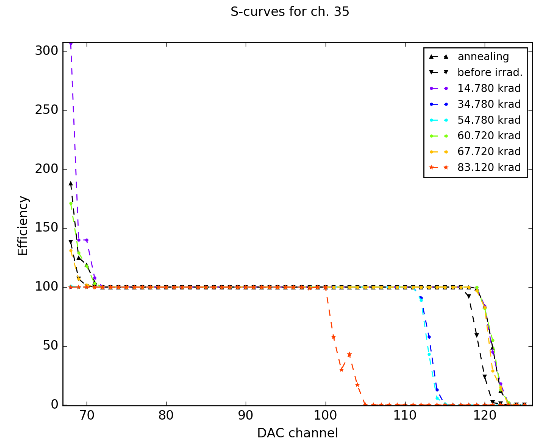
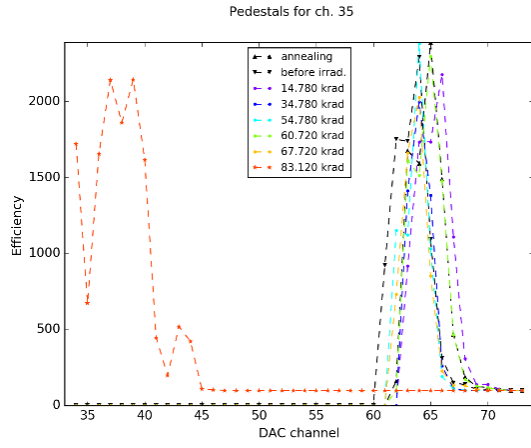


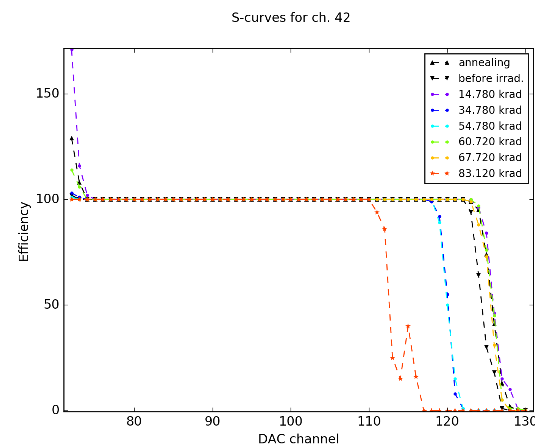
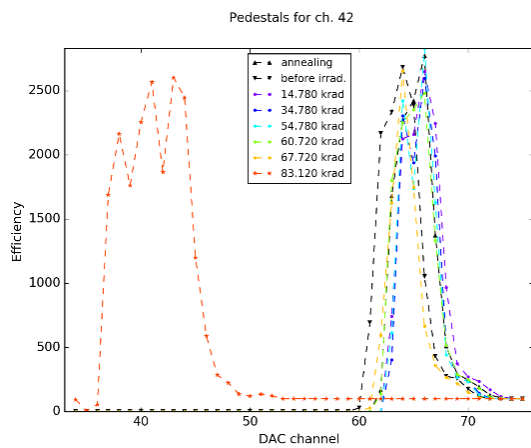
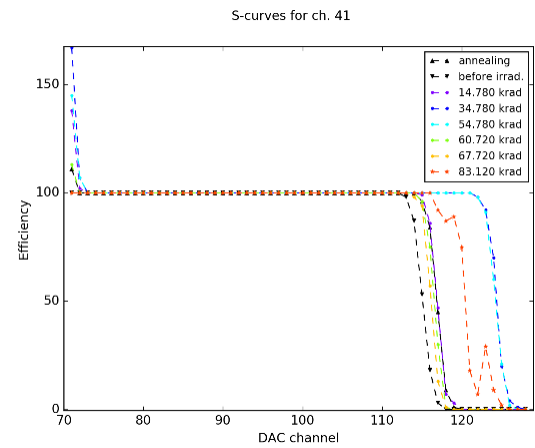
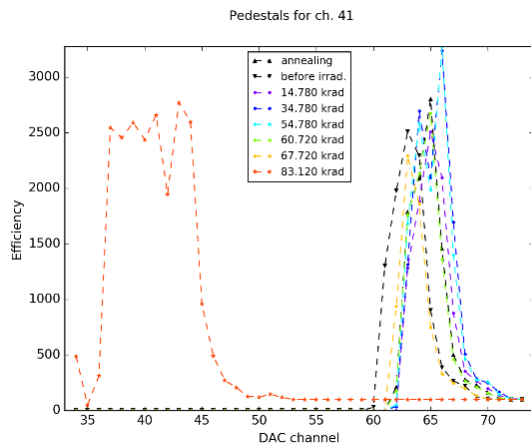
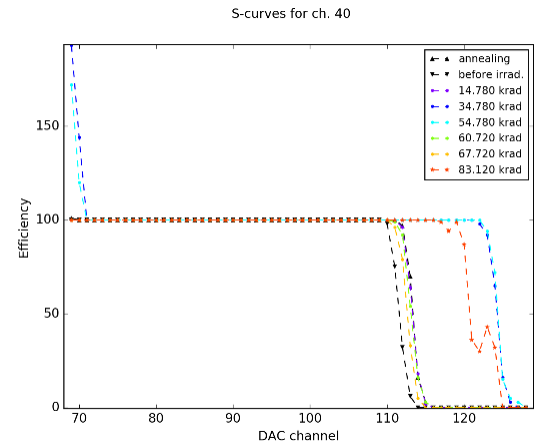
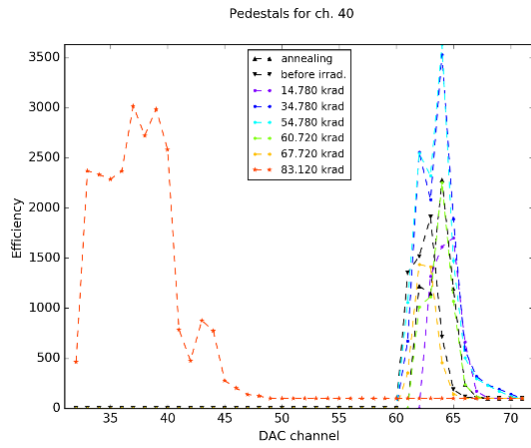
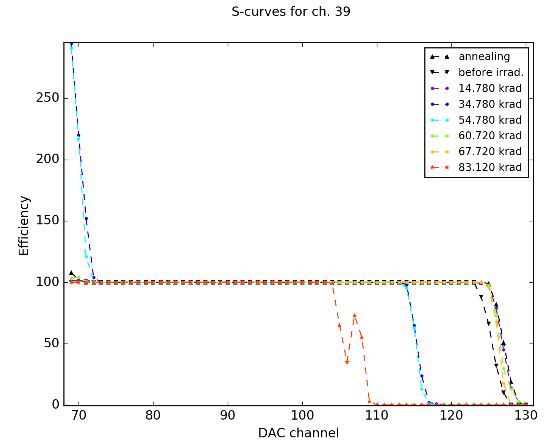
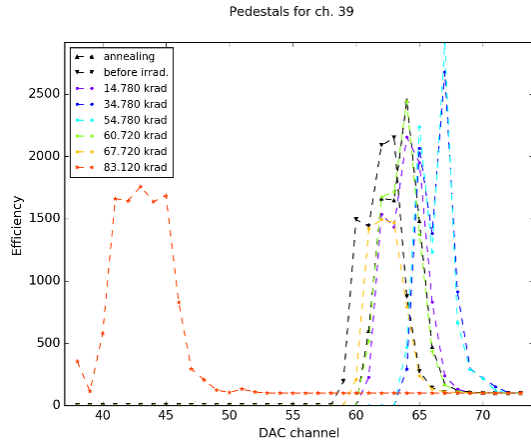


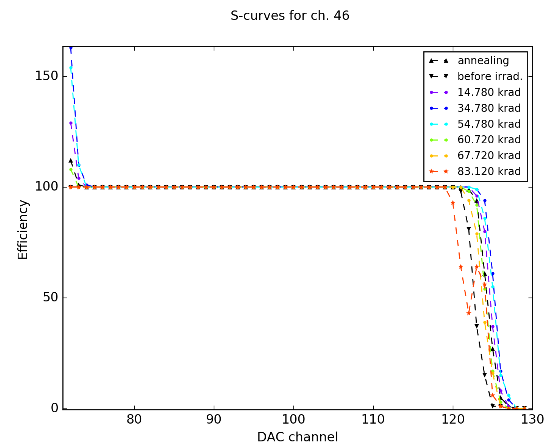
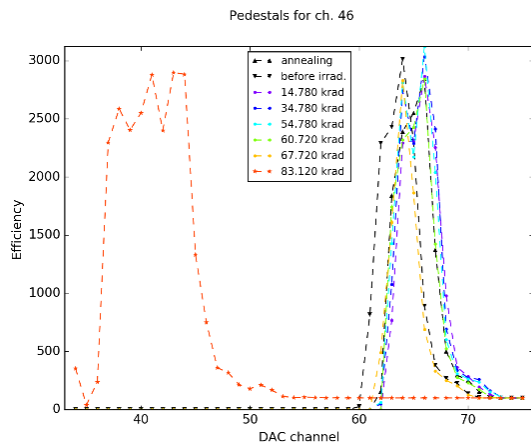
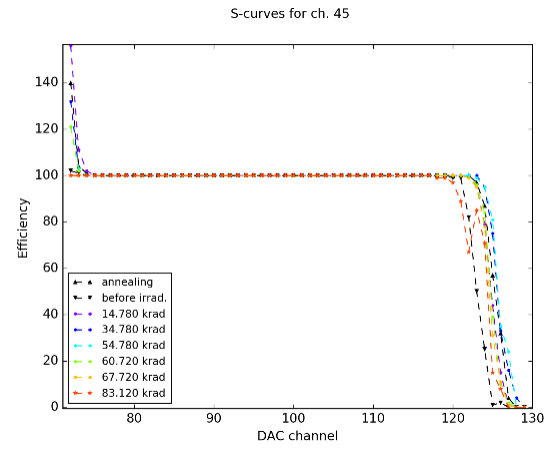
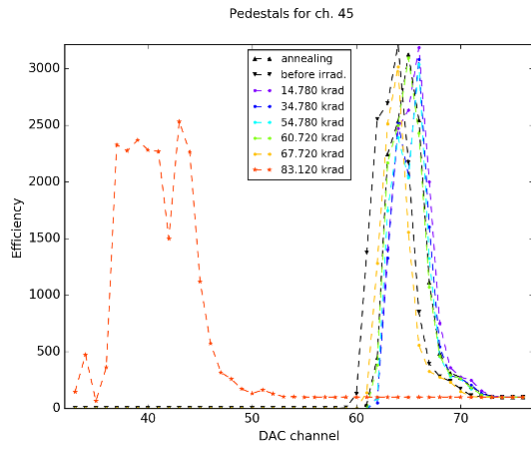
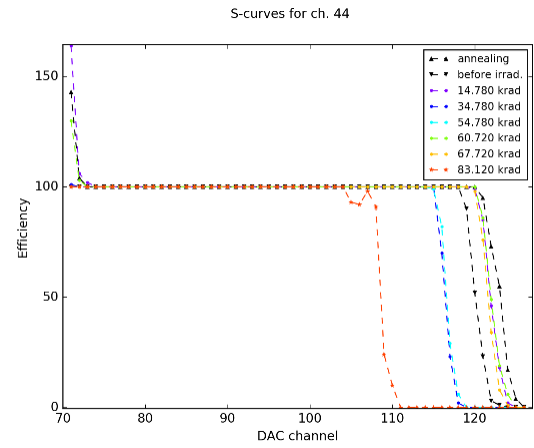
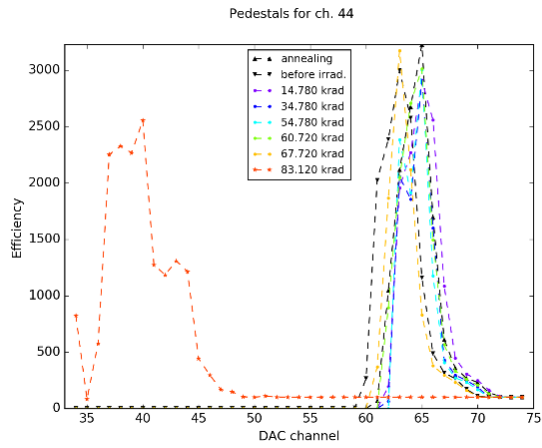
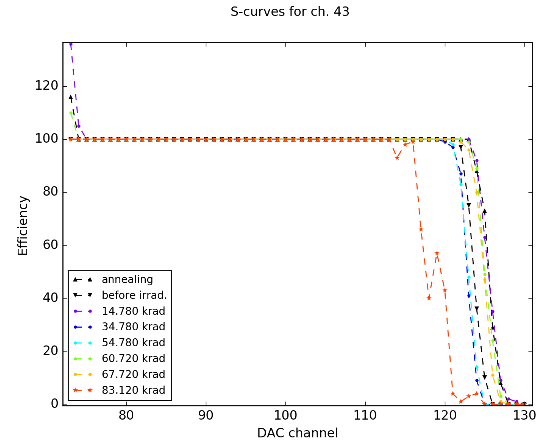
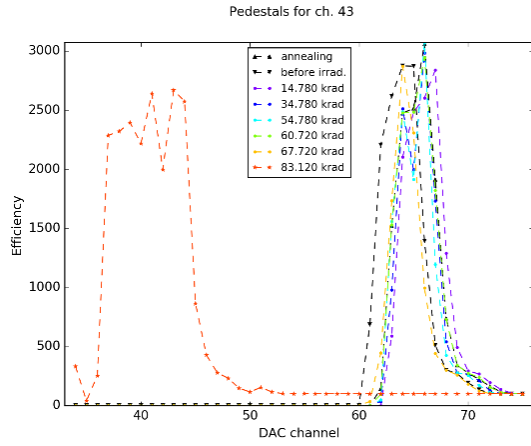


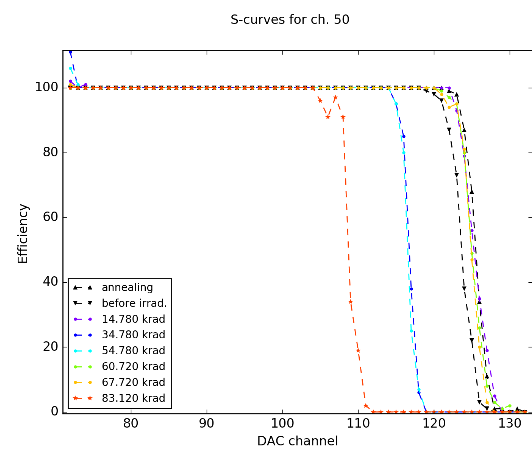
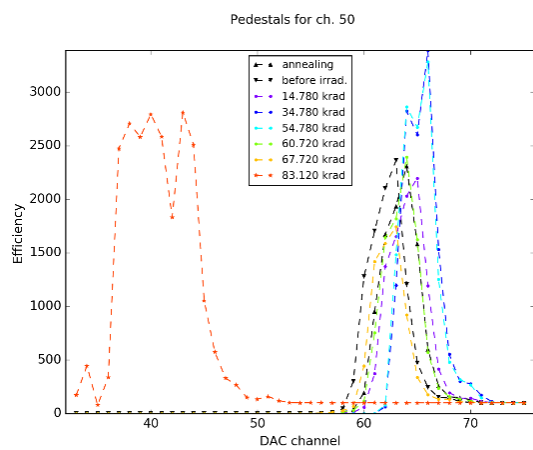
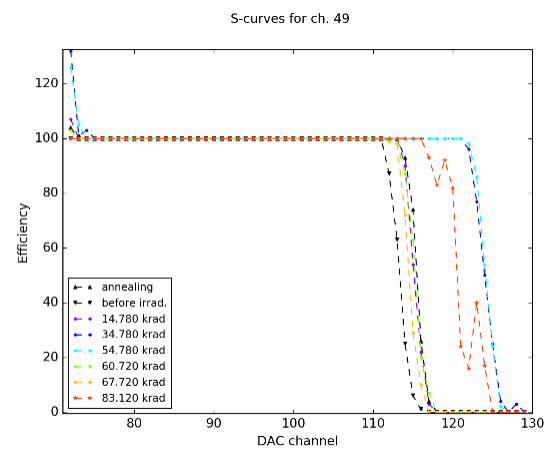
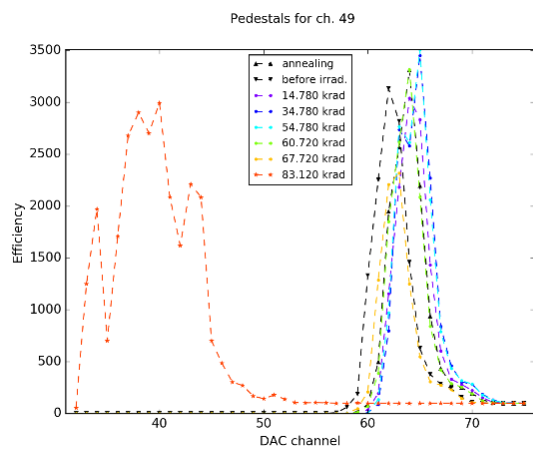
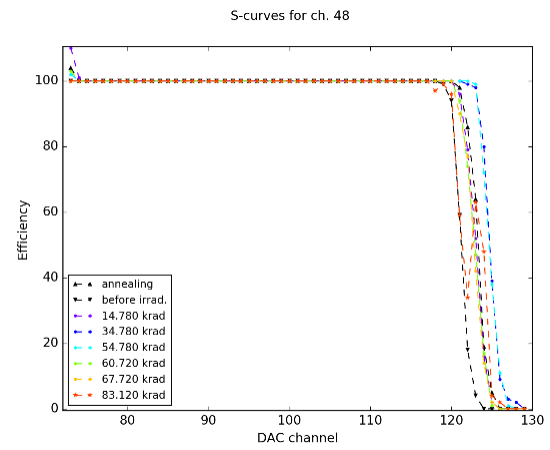
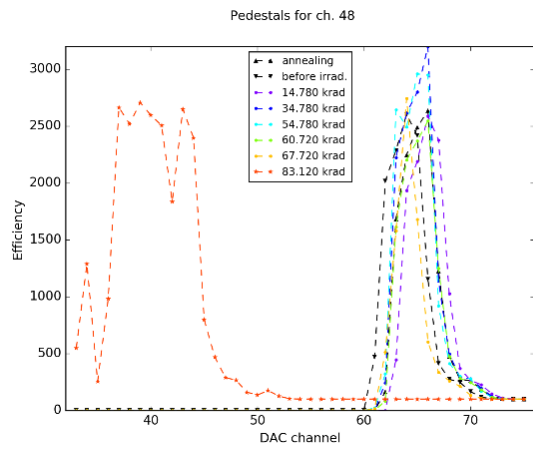
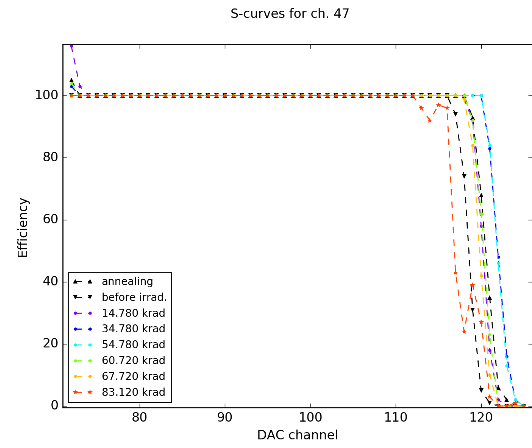
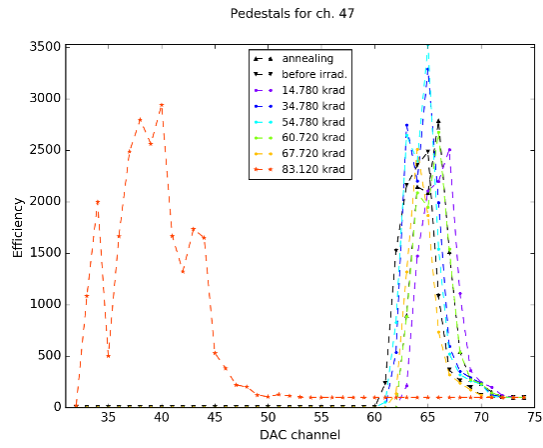


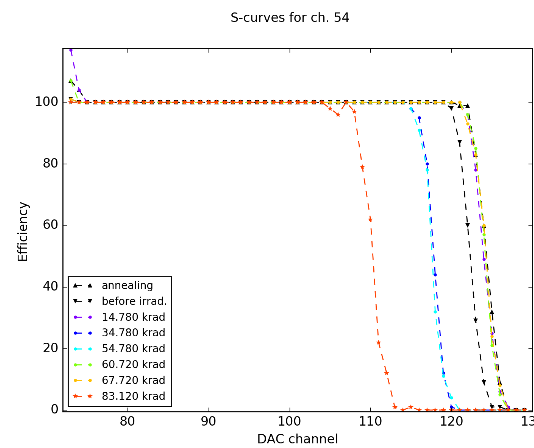
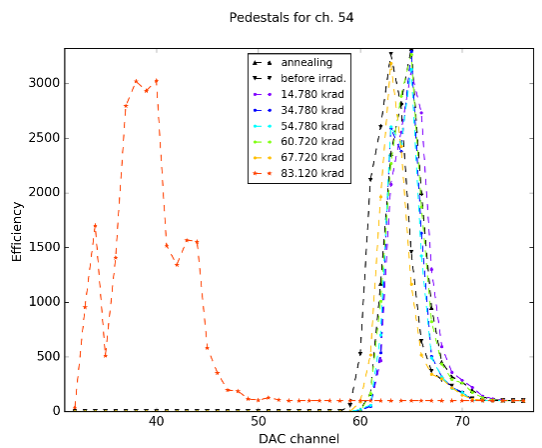
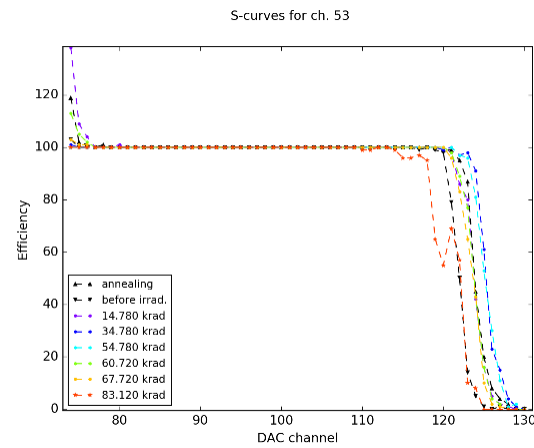
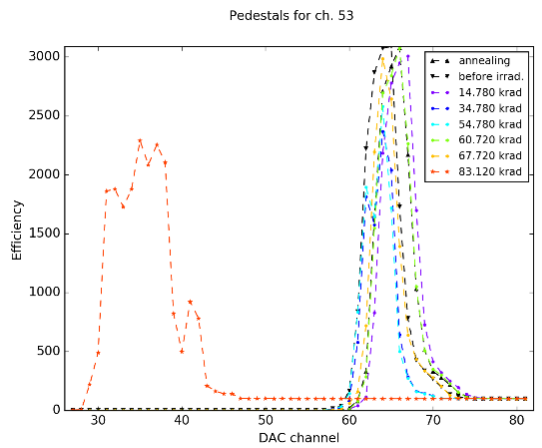
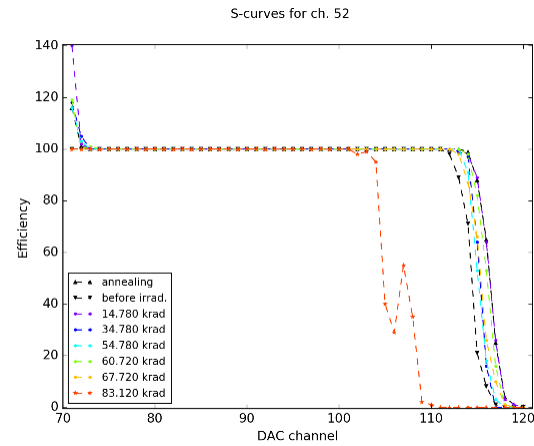
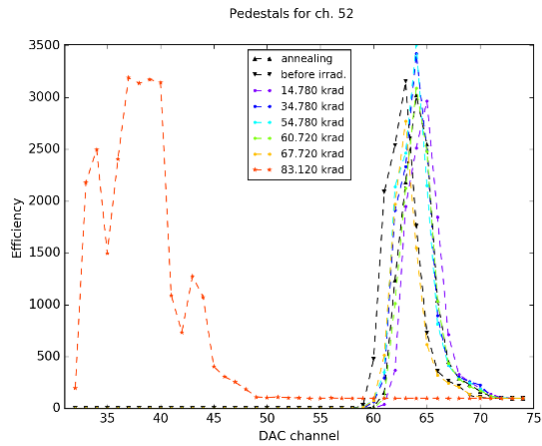
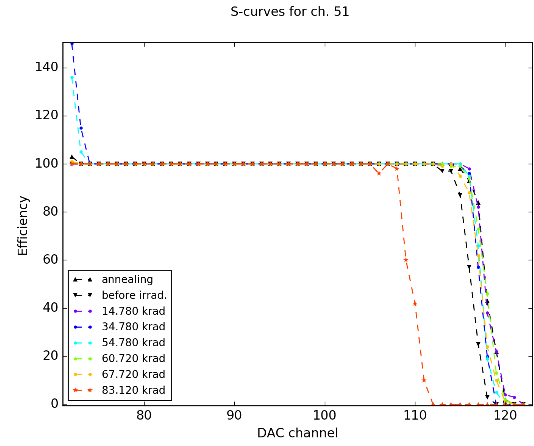
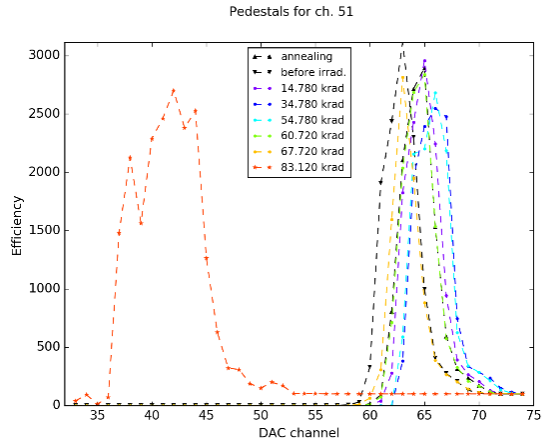


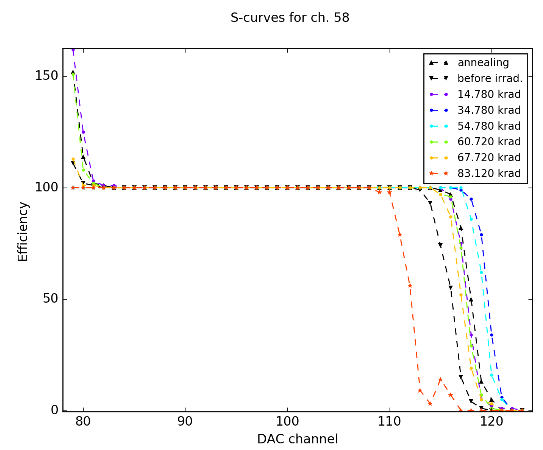
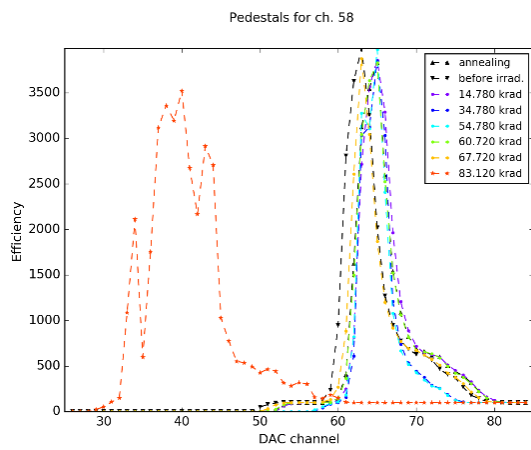
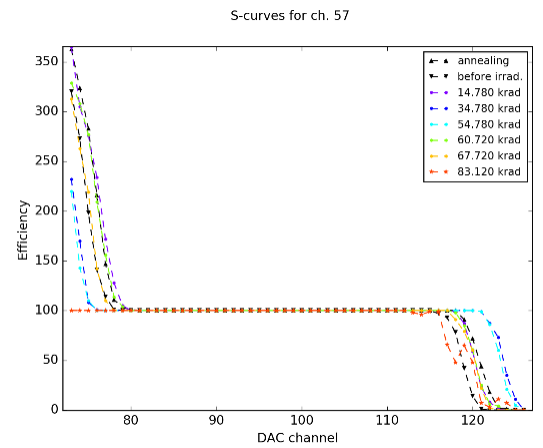
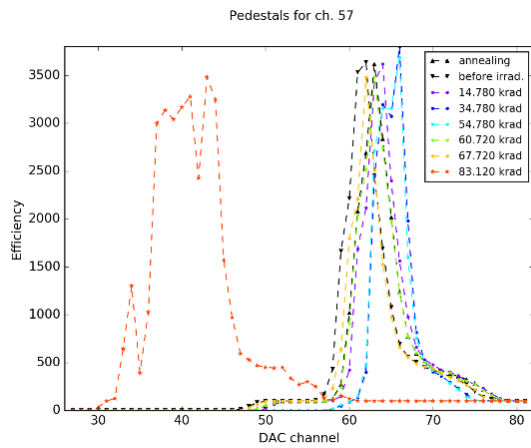
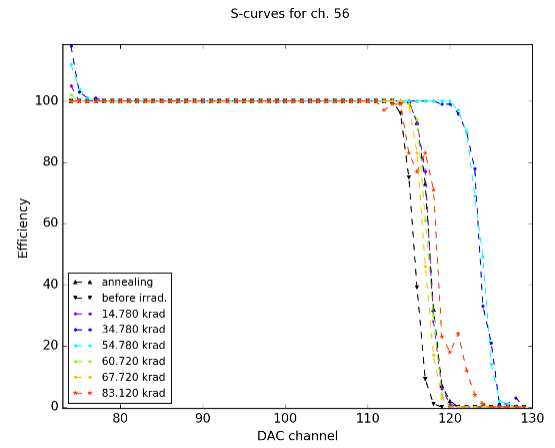
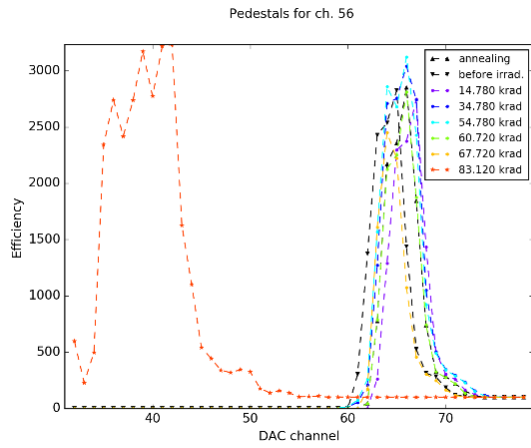
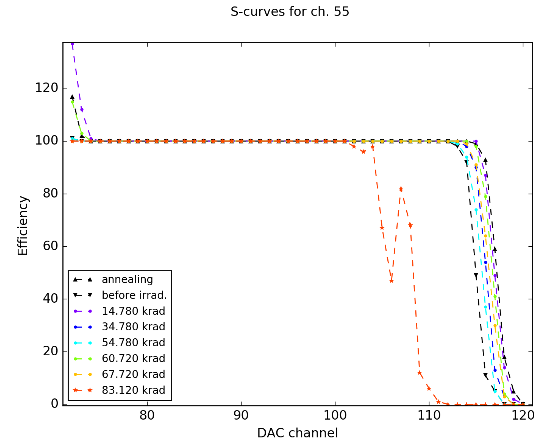
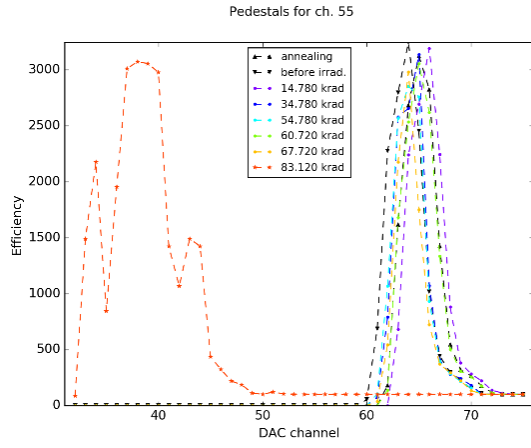


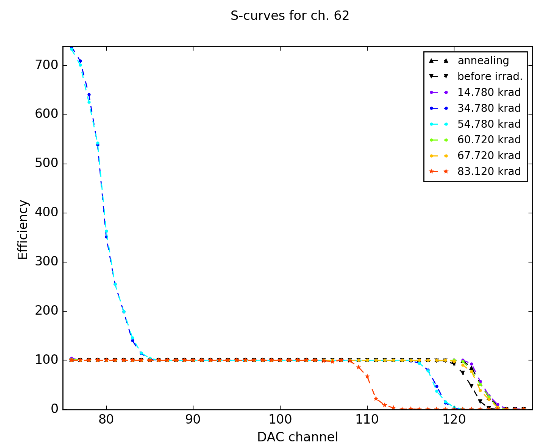
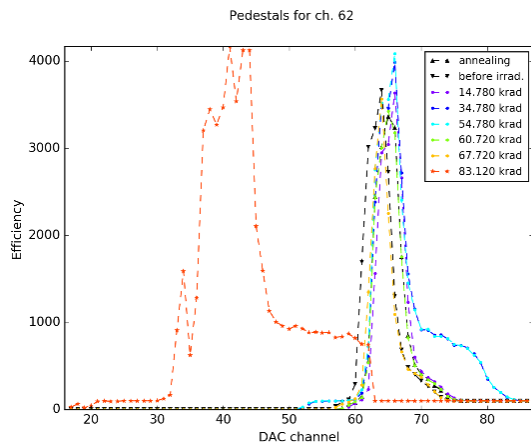
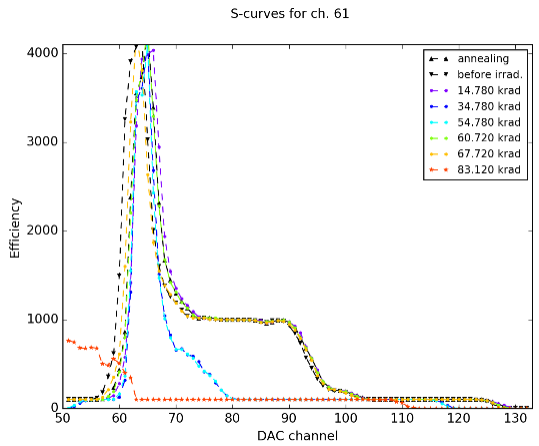
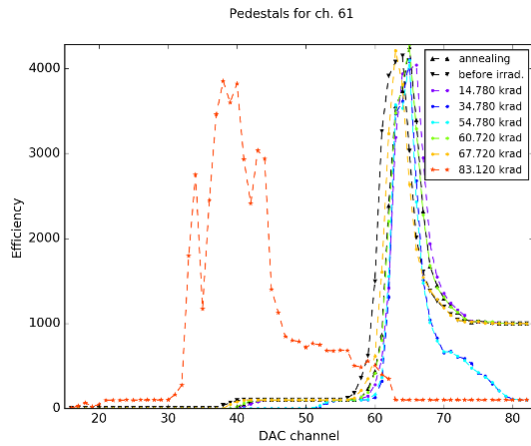
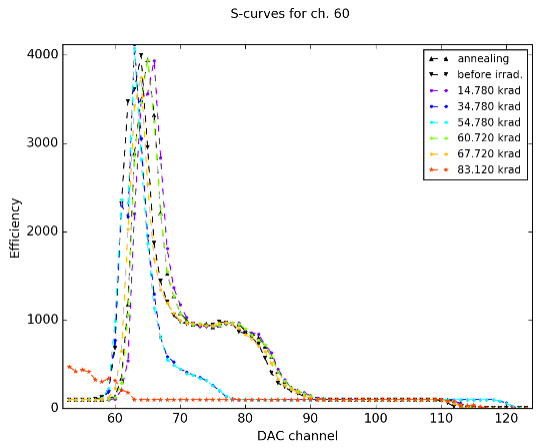
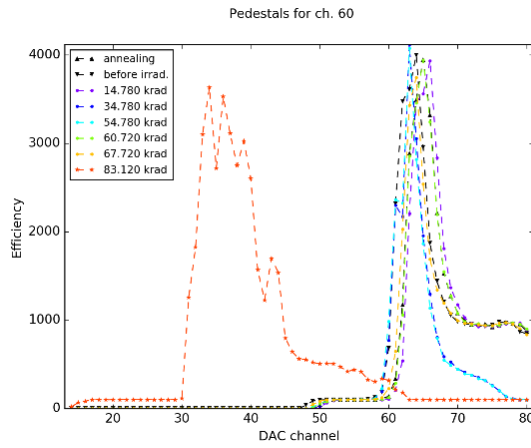
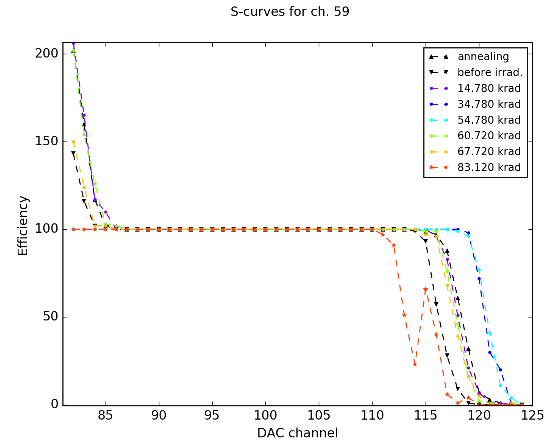
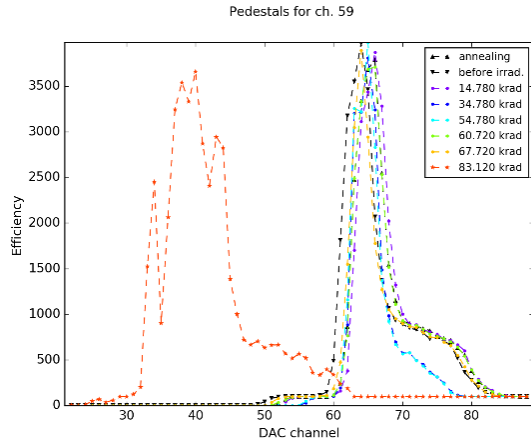


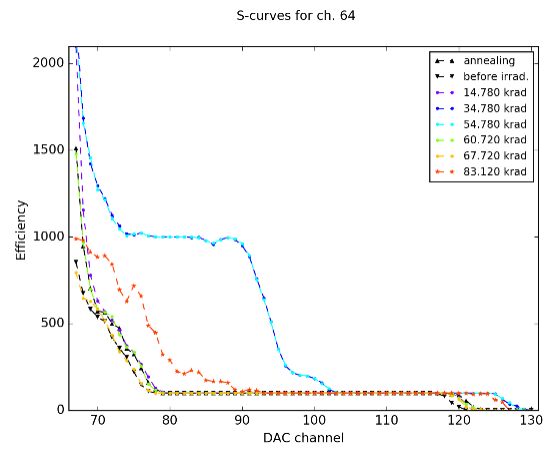
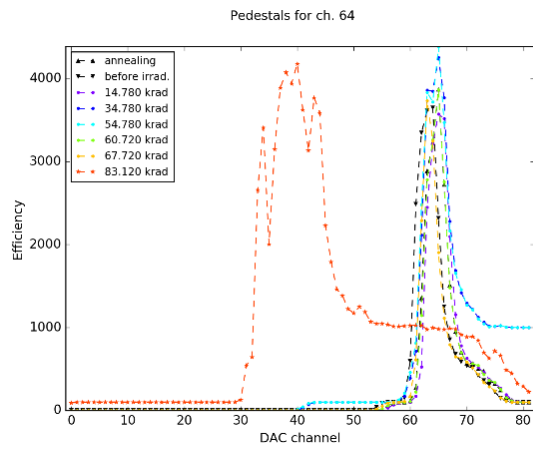
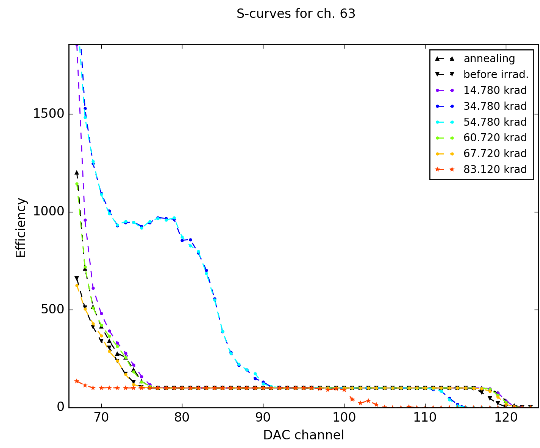
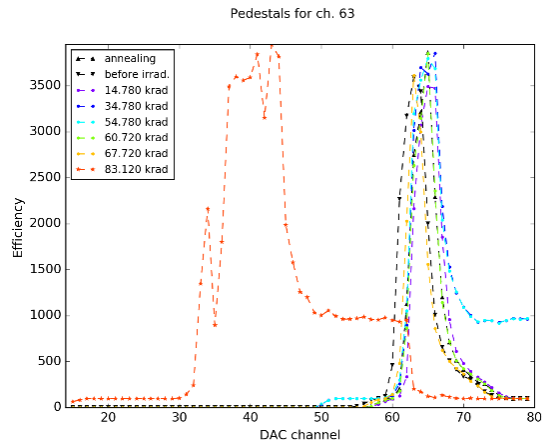




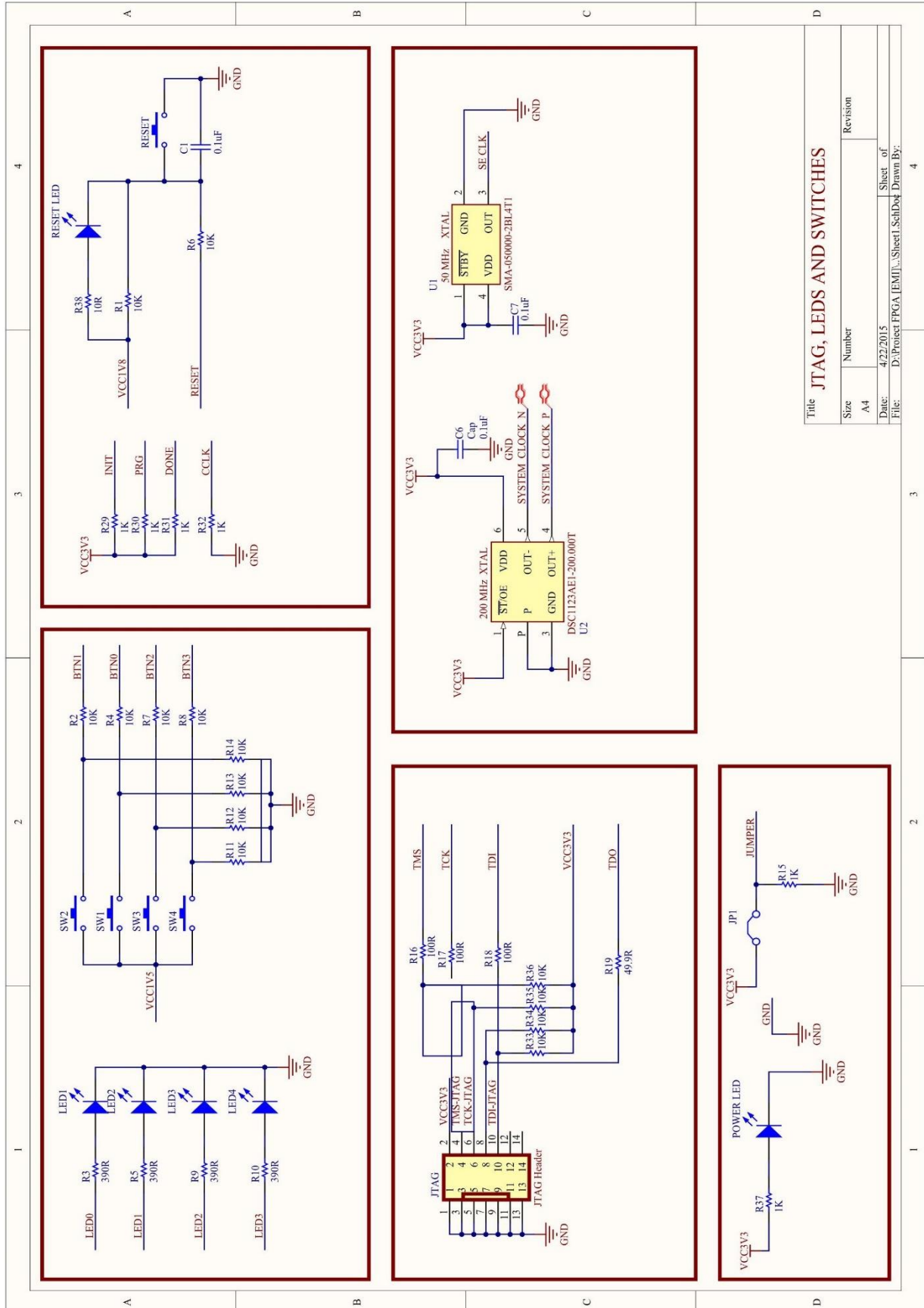




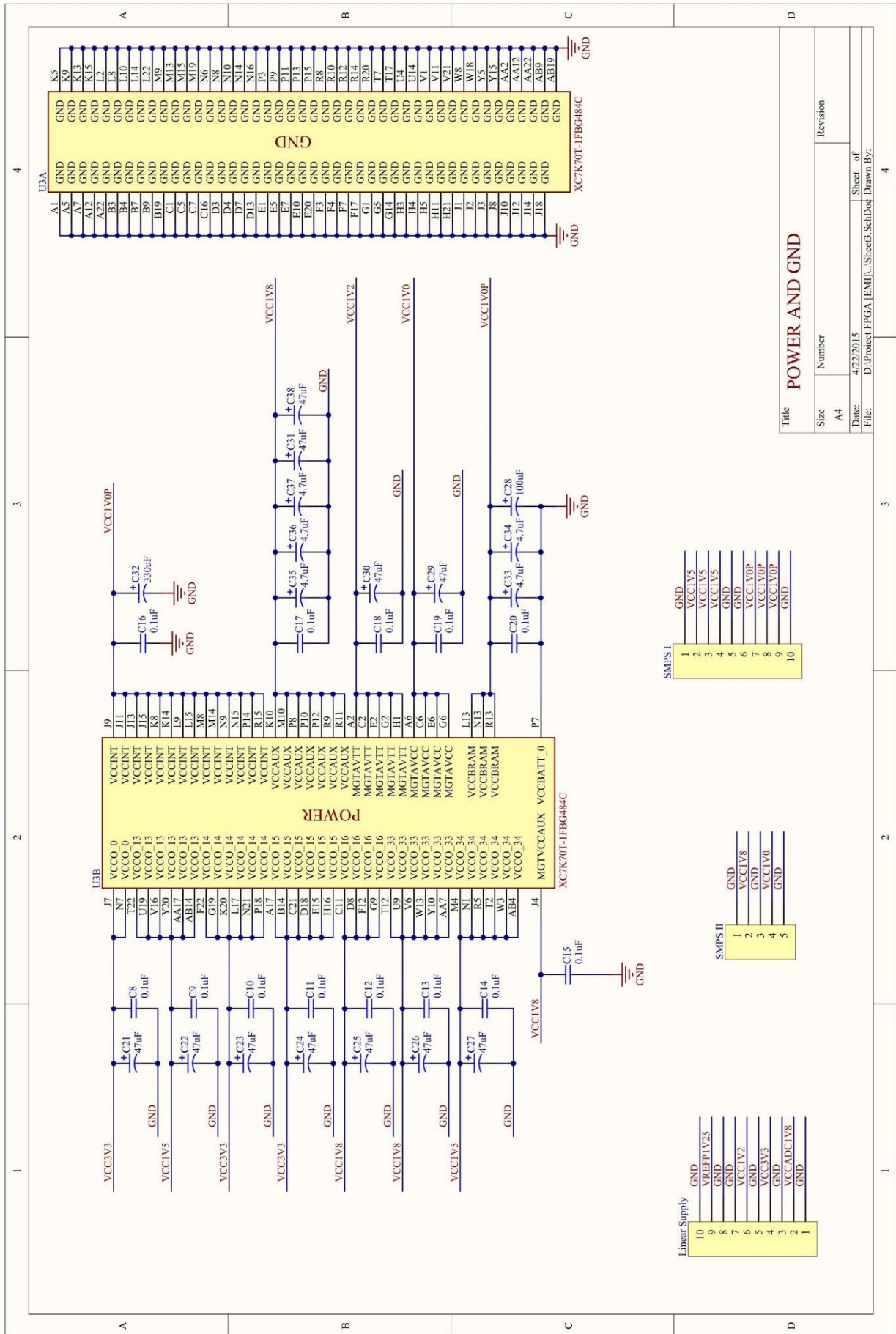


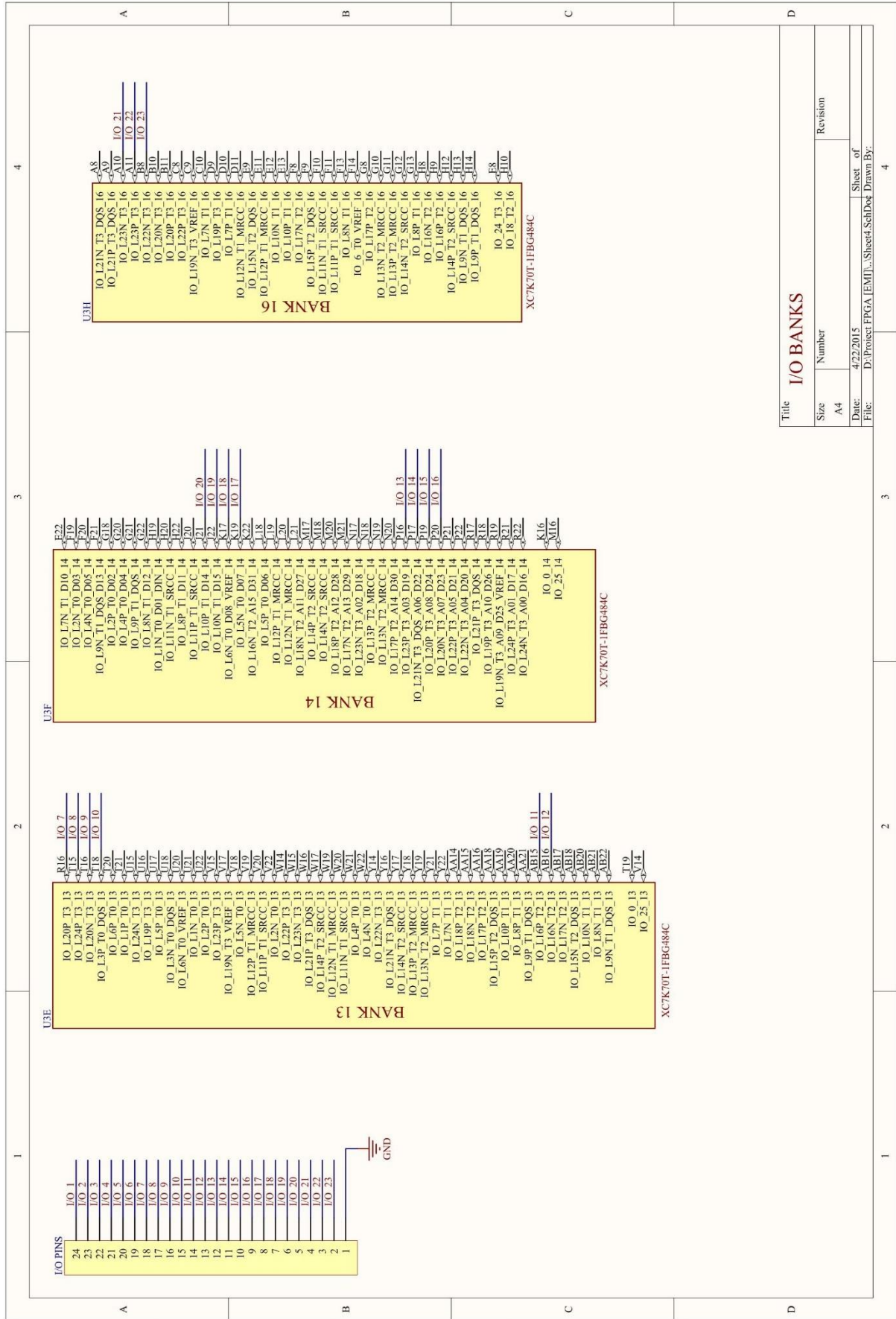


Appendix D



Title		JTAG, LEDs AND SWITCHES	
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Appendix E

