

Master-Thesis

**Design of an acquisition card mixed signals
analog/digital based on FPGA for CERN's
Beam Energy Tracking Systems**

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submitted by

B.Sc. B.Eng. Julien Alaric

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Professor Supervisor
Second Supervisor (CERN)

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Prof. Dr.-Ing. Elke Mackensen
M. Sc. Pieter Van Trappen

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Preface

This work treats about the "design of an acquisition card mixed signals analog/digital based on FPGA" and answer the question of "How can this system fulfil the new specifications of the Beam Energy Tracking System (BETS) by being compatible to other acquisition use-cases ?".

My personal major motivation for this work was to use and increase my theoretical and practical knowledge in electronic hardware development. Another important motivation was to enlarge my experience by working with hardware description languages. Finally, CERN's multicultural working environment was an incredible opportunity.

I would like to thank Prof. Dr.-Ing. Elke Mackensen of the Hochschule Offenburg for being available and for advising me for my report during this project. I also thank Ing. Nicolas Voumard and Ing. Pieter Van Trappen for trusting me for this project and to advise me during the whole project. I also thank Ing. Daniel Valuch and Martin Praznovsky for giving me access to their laboratory as well as advising me in analog to digital calibration methods. Finally, I thank the Baden-Württemberg scholarship which sponsored me to do this project at CERN.

Julien Alaric,
09/2023 at Ferney-Voltaire, France

Summary

Design of an acquisition card mixed signals analog/digital based on FPGA.

This project handles the design of the acquisition card of CERN's Beam Energy Tracking System (BETS). It is used for multiple purposes but mainly for the Large Hadron Collider Beam Dumping System (LBDS) and the Super Proton Synchrotron Beam Dumping System (SBDS).

In this work a new hardware and hardware description language (named gateware) design is done for the Beam Energy Acquisition (BEA) card. First, the state of the technology is done by describing the current system from 2004 as well as the new LBDS-BETS specification. Second, the electronic development is realized. It starts with the hardware architectures, the choice of the components and schematic as well as PCB design. Third, the gateware was developed. In this part, the drivers, communication IPs and signal processing IPs are simulated and tested as well. Last but not least, the tests and measurements for the new system are done and compared to the old one.

Abstract

Design of an acquisition card mixed signals analog/digital based on FPGA.

Dieses Projekt behandelt das Design von der Acquisitionskarte vom CERN's Beam Energy Tracking System (BETS). Es kann für viele verschiedene Anwendungen eingesetzt werden, hauptsächlich aber für das Large Hadron Collider Beam Dumping System (LBDS) und das Super Proton Synchrotron Beam Dumping System (SBDS).

Diese Arbeit ist eine neue Elektronik- und Hardware- Description Language (HDL oder Gateware)- Entwicklung des vorherigen Systems von 2004.

Zunächst wird der Stand der Technik vorgestellt, sowie die neue LBDS-BETS Spezifikation. Danach wird die Hardware-Entwicklung erklärt, von der Architektur und Auswahl der Komponenten bis zum PCB- Design. Anschließend wird die Hardware Description Language für die FPGA entwickelt, simuliert und getestet. Letzendlich werden Messungen und Tests für das neu entwickelte System durchgeführt und mit dem Vorherigen verglichen.

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Acronyms

ABT Accelerator Beam Transfer. 26

ACK acknowledge. 55

ADC Analog to Digital Converter. 6, 8–12, 14, 17–21, 24, 28, 38, 40, 41, 45, 47, 50, 54–58, 62–67, 69–71, XII–XIV

BEA Beam Energy Acquisition. 1, 4–6, 10, 11, 14, 15, 62, 63, 65–67, XIII, XV

BEC Beam Energy Controller. 5

BEI Beam Energy Interlock. 5

BEM Beam Energy Meter. 5, 10, 12, 15, 53, 68

BETS Beam Energy Tracking System. 1, 4, 5, 11, 15, 32, 71, XII

BTE Beam Transfer Electronics. 26

BW Bandwidth. 33

C2P Core to PIF. 47, 52

CERN Centre Européen de Recherche Nucléaire. 14, 26, 37, 41, 44, 58

CRC Cyclic Redundancy Check. 58

DAC Digital-to-Analog Converter. 55, 62, 66, 69, 70

DCCT Direct-Current-Current-Transformer. 1, 4–6, 12, 13, 19, 25, 31, 37, 38, 58, 69, 70

DNL Differential linearity error. 9

DSP Digital Signal Processing. 27, 61

EEPROM Electrically-erasable programmable read-only memory. 30, 42, 45, 50–52, 54–56, 70, XII, XIV

EMC ElectroMagnetic Compatibility. 37, XII

EPC Electrical Power Converter. 37

FF Flip-Flop. 27, 61

- FGC** Function Generator Controller. 13, 30, 36, XIV
- FIFO** First In First Out buffer. 59, 61
- FIR** Finite Impulse Response. 41, 55, 57, XIII
- FP** Front panel. 31
- FPGA** Field Programmable Gate Array. 14, 25–32, 37, 40, 49, 52, 56, 61, 70, VII
- FSE** Full-scale Error. 9
- Gitlab CI/CD** Gitlab Continuous Integration / Continuous Deployment. 42, 44
- GMT** General Machine Timing. 4
- GTP** Gigabit Transceiver Port. 27, 28, 32, 33, 37, 40, 58–61
- HDL** Hardware Description Language. 41
- HVD** High-Voltage Divider. 4
- INL** Integral linearity error. 9
- INT** Interrupt. 52
- IO** Input/Output. 41, 49, 50, XIV
- LBDS** LHC Beam Dumping System. 1, 4, 11, 64
- LHC** Large Hadron Collider. 1, 15
- LSB** Least Significant Bit. 49, 55, 64
- LUT** Look-Up-Table. 27, 61
- MM** Multi-mode. 15, 41
- MPE** Machine Protection and Electrical Integrity Group. 15, 41, 68
- MUX** Multiplexer. 6, 11, 19
- OE** Offset Error. 9
- OVS** Oversampling. 50, 66
- P2C** PIF to Core. 47, 52

- PIF** Parameterized Intellectual Property Function. 43
- PLL** Phase-Locked Loop. 33, 59
- PWRGD** Power Good. 52
- RAT** Remote Acquisition Transceiver card. 40, 61, 62, 66–68, 70, 71, XIII, XV
- RFS** Reserved for futur use. 58
- RSS** root-sum-square. 9, 67
- SBDS** SPS Beam Dumping System. 1, 4
- SBI** Simple Bus Interface. 42, 43, 46, 47, 50, 52, 55, 57, XII
- SFP** Small form-factor pluggable. 33, 34, XII, XIV
- SM** Single-mode. 15, 28, 37, 41, 60, VII, XIII
- SNIA** Storage Networking Industry Association. 33
- SPS** Super Proton Synchrotron. 1
- TCL** Tool Command Language. 44
- TCR** Temperature Coefficient of Resistance. 6
- TE** Technology Department. 41, 68
- UART** Universal Asynchronous Receiver Transmitter. 30, 40–42, 50, 51, 53–56, 68, XII, XIV
- UVVM** Universal VHDL Verification Methodology. 42–44, 52, 53, VII
- VHDL** VHSIC(Very High Speed Integrated Circuit) Hardware Description Language. 42, 44
- VM** Virtual Machine. 44

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List of symbols

Abbreviation	Unit	Designation
Δ	-	Variation range
ε	V	Root-sum-square error
E	V	Measurement error
E_{ppm}	ppm	Measurement error in ppm
OE	mV	Offset error
FSE	mV	Full-scale error
FR	V	Full-range
DNL	LSB	Differential Non Linearity error
INL	LSB	Integral Non Linearity error
TCR	$\frac{ppm}{^{\circ}C}$	Temperature coefficient of resistance
R	Ω	Resistance
L	H	Inductance in Henry
C	F	Capacitance in Farad
I	A	Current in Ampere
V	V	Voltage in Volt
f	Hz	Frequency in Hertz
D	%	Duty-cycle
SR	Hz	Sample rate
T	$^{\circ}C$	Temperature in degree celsius
Ex	18-bit code	Ideal code of given value
M	18-bit code	Measured code of given value
O	18-bit code	Offset code value
G	18-bit code	Gain code value
A_i	-	Matrix-coefficient
ρ	V	Non-linear error estimation
N	-	Polynomial degree
$poly$	-	Polynomial function

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1 Introduction

1.1. Motivation and problematic

The Beam Energy Tracking System (BETS) is from 2004 and was initially developed for the LHC Beam Dumping System (LBDS). The role of the LBDS is to safely dump the beam in case of emergency (internal or external root cause) or at the end of a physics run when the beam is not of sufficient quality. The Beam Energy Tracking System (BETS) is a safety critical system of the LBDS which surveys that the strength of each LBDS high voltage generator are within predefined tolerances with relation of the beam energy. To determine the beam energy, the BETS acquires currents from the LHC main bending magnets (ring bends) through Direct-Current-Current-Transformer (DCCT). In a synchrotron, the current flowing in the main bending magnet is directly proportional to the energy of the machine (saturation in the magnets must be considered).

The Beam Energy Tracking System (BETS) makes the acquisition of DCCT and other analog signals (voltage strength, currents or position) through the Beam Energy Acquisition (BEA) which is intended to acquire analog signals and digitize them to be sent over optic fibers to the centralized BETS chassis. The BEA cards are by design deported acquisitions cards which may be distant from the centralized BETS from few meters to nearly five kilometers.

BETS has been deployed over the years to numerous different systems in the LHC (injection kickers and LHC transfer lines collimators surveillance) and in the Super Proton Synchrotron (SPS) (SPS Beam Dumping System (SBDS), SPS extraction kickers and tune kickers surveillance).

Nowadays, the BETS is aging and components become obsolete. The renovation of this system takes into consideration new requirements for the LBDS as well as for other systems. Due to this, the BEA specification was changed and this card needs to be completely renewed to be compatible with multiple other systems. In this work, the new BEA card is redesigned from the hardware up to the gateway and tests.

How should this system be developed to fulfil the new BETS specifications by being also compatible for the other use-cases ?

1.2. Tasks of the project

In this project, the new BEA card from BETS needs to be developed and tested. To prepare the upcoming production of the BETS's new BEA cards, the following tasks are completed in the present work :

- Hardware development of the new BEA-card : architecture, choice of components

and schematic (routing done externally)

- Gateware development to meet all use cases : IP development, simulation and tests
- Automated tests and calibration development : development of post-production automated tests and, if necessary, calibration

In the next section, the detailed project steps and timeline will be described.

1.3. Project planning

Each of the previously described tasks is split steps as follows :

- Hardware development :
 - Research and proposition of possible architectures
 - Choice of the components
 - Schematic development with Altium Designer
 - PCB constrain definition and routing supervision
 - Prototype production supervision
 - Prototype hardware tests and hardware debug
- Gateware development :
 - Research and proposition of possible architectures
 - IP sources development
 - Components and complete gateware system simulation
 - Continuous integration testbenches
- Tests and measurements :
 - Development of automated hardware tests
 - Development of automated calibration (if required)
 - Post-production tests and calibration
 - Measurement of the system precision (old card and prototype)

At the beginning of the project an approximative timeline was realised. This timeline is described in the figure 1.1. The second figure 1.2 shows the real elapsed time for the different goals of the projects. Several delays were induced through missing project information and an uncertain specification during my internship (delays are shown through red arrows).

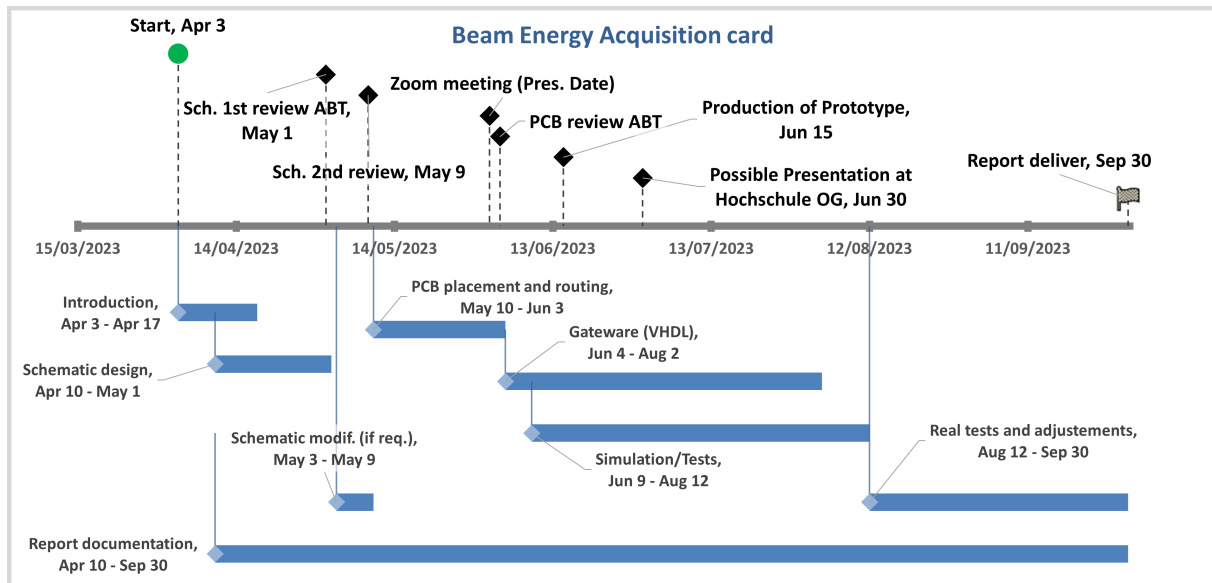


Figure 1.1: Planning estimation

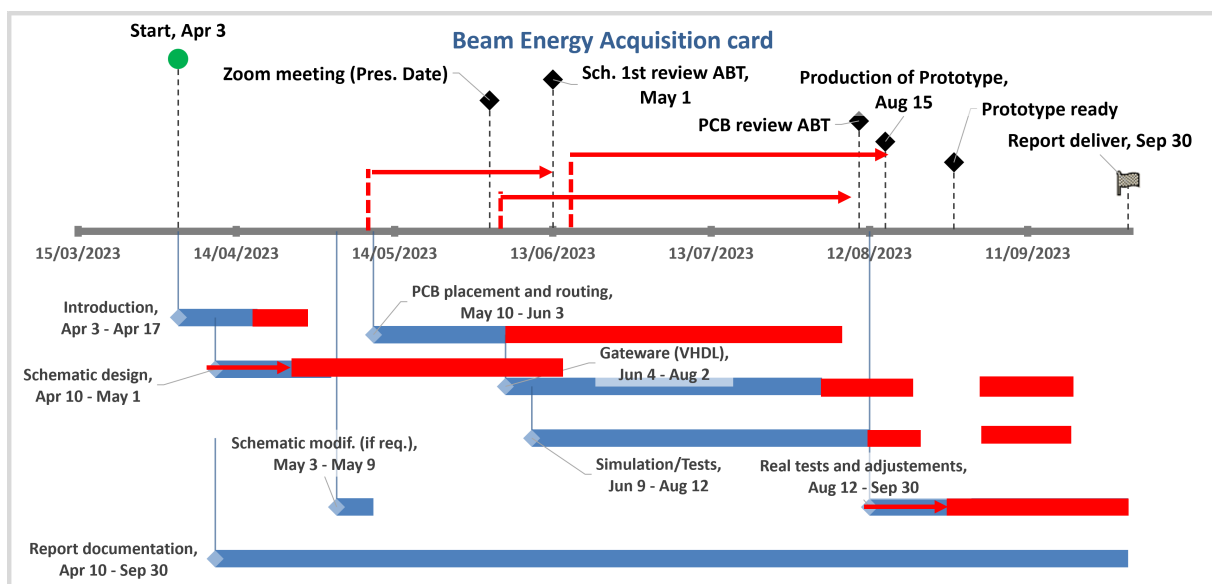


Figure 1.2: Real planning timeline

2 State of the technology

In this chapter the current BETS and BEA systems is presented. The current BEA card characteristics and previous choices for this system is explained. Finally, the purpose of a new design conception of this system is clarified and the possible solutions are shown.

2.1. The Beam Energy Tracking System

2.1.1. Overview

The BETS main functions are the following :

- Acquisition of the machine beam energy through measurements of main bending magnet current through DCCT
- Generation of the kick strength setting references for the LBDS and SBDS
- Continuous surveillance of the equipment parameters:
 - Kicker generators voltage strengths
 - Septum or quadrupole magnets currents
 - Collimators positions
- Generation of interlock when one of the parameter is not within predefined tolerances or on an internal fault is detected.
- Distribution of the beam energy over General Machine Timing (GMT) for other BETS systems all over the machine or any other user.

The figure 2.1 describes the context where the BETS is interacting. As shown in the diagram, the BETS receives the measured magnet flown currents information from the different Direct-Current-Current-Transformer, gets the state of the High-Voltage Divider through an "interlock" and controls the following kickers magnets. Its role is then to give the measured energy references to the "external clients" which represents the upstream systems, as well as giving the beam state with a beam permit signal to the Dump Request System.

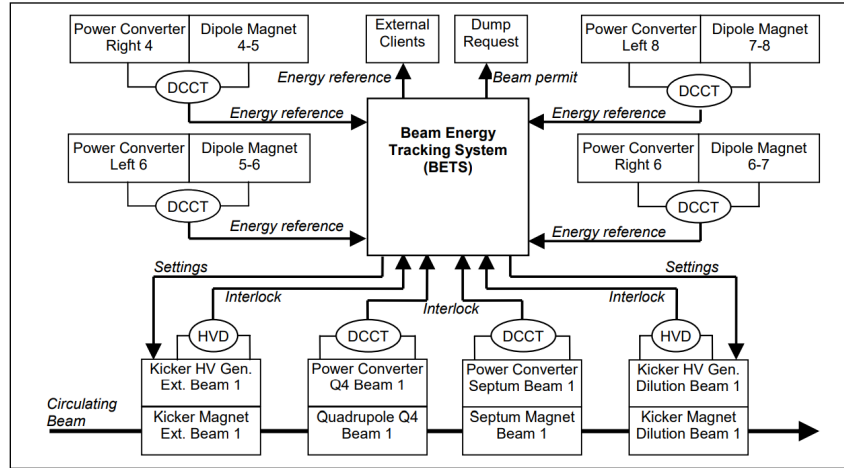


Figure 2.1: Beam Energy Tracking System context diagram [1]

2.1.2. Architecture

The BETS architecture can be described with the following block diagram, figure 2.2. It is made up of four different cards, the Beam Energy Acquisition, the Beam Energy Meter, the Beam Energy Interlock and the Beam Energy Controller.

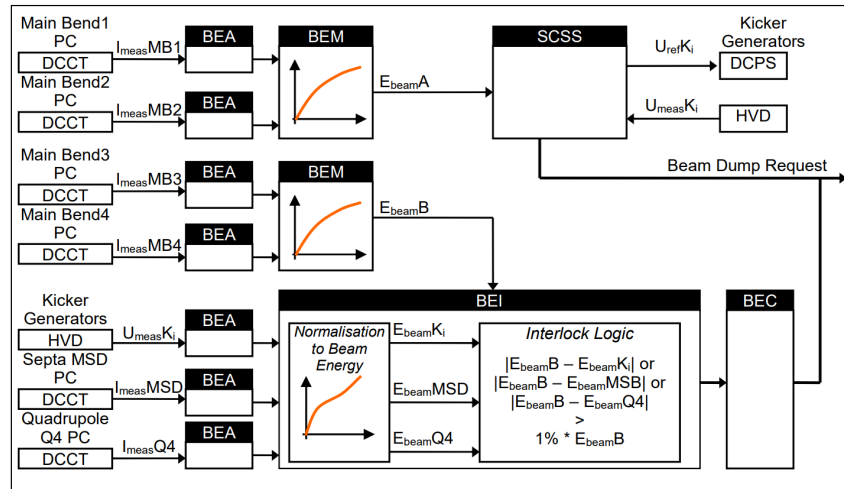


Figure 2.2: Beam Energy Tracking System architecture [1]

The beam energy reference signals are obtained through two independent and redundant BEM which are using BEA cards to acquire, digitise and process the DCCT voltages. The BEM centralizes the measurements acquired from the BEA cards through optic fiber point to point links. It then calculates a mean value of the different received measurements and uses a lookup-table to find the corresponding beam energy reference.

The BEA cards are required due to the long distances between each measurement point as the magnets where the measurements are done are separated by multiple kilometers.

2.2. Current Beam Energy Acquisition cards

The BEA basically does the acquisition of analog signals (from 0 V to 10 V) of two channels as well as two digital status signals. Those signals are coming from the DCCT, see 2.1.2. In order to have more stable resistance against ADC drifts the 0 V and 10 V references are also sampled here, and a single channel ADC is used in combination with a Multiplexer (MUX) to be able to switch between the analog inputs (See figure 2.3).

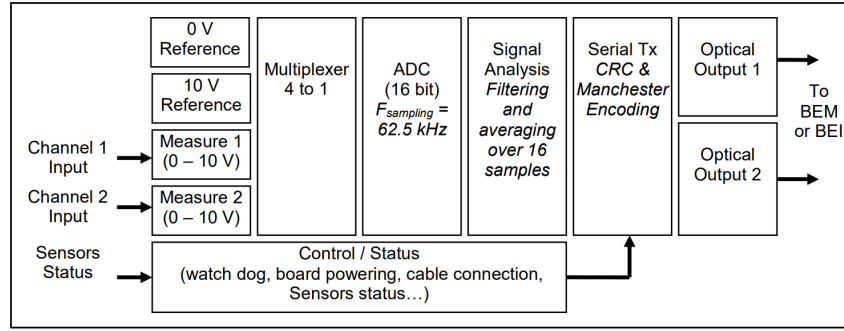


Figure 2.3: Block diagram of the BEA card [1]

2.2.1. Condition of operations

In this part, the conditions of operations are detailed. Those conditions are taken in account during the current BEA analysis as well as for the new design.

Temperature

The conditions of operations in terms of temperature are important to take into account within the framework of this project. Indeed, the calculation of the precision of the analog to digital part is highly dependent on the temperature variations mainly due to the Temperature Coefficient of Resistance (TCR).

The equation 2.1 defines the maximal operating temperature variation of the environment where the BEA is used and the equation 2.2 is the used equation to calculate the TCR deviation by the different manufacturers:

$$\Delta T = 40^{\circ}\text{C} - 10^{\circ}\text{C} = 30^{\circ}\text{C} \quad (2.1)$$

$$TCR = \frac{R2 - R1}{R1(T2 - T1)} \frac{\text{ppm}}{^{\circ}\text{C}} \quad (2.2)$$

In 2.2, R2 represents the resistance value at the temperature T2 and R1 the resistance value at the standard operating temperature (T1 = 25 °C). Finally, to calculate the resistance precision variation in the next sections we can use the equation 2.3 with 2.1.

$$\begin{aligned} R2 &= R1 \cdot TCR \cdot \Delta T + R1 \\ \Rightarrow \Delta R2 &= R1 \cdot TCR \cdot \Delta T = 30 \cdot R1 \cdot TCR [\Omega] \end{aligned} \quad (2.3)$$

2.2.2. Analog front-end

The analog front-end is constituted of a high impedance input as well as a first low pass filtering. Then, the differential input signal is converted to a single mode signal through a precise instrumentation amplifier. After this step, a Sallen-Key filtering is applied before being muxed to the buffered ADC input. See appendix BEA-3U, BEA-6U.

This front-end was modeled with LT-Spice in order to get the transfer function of this design. The schematic can be seen in figure 2.4.

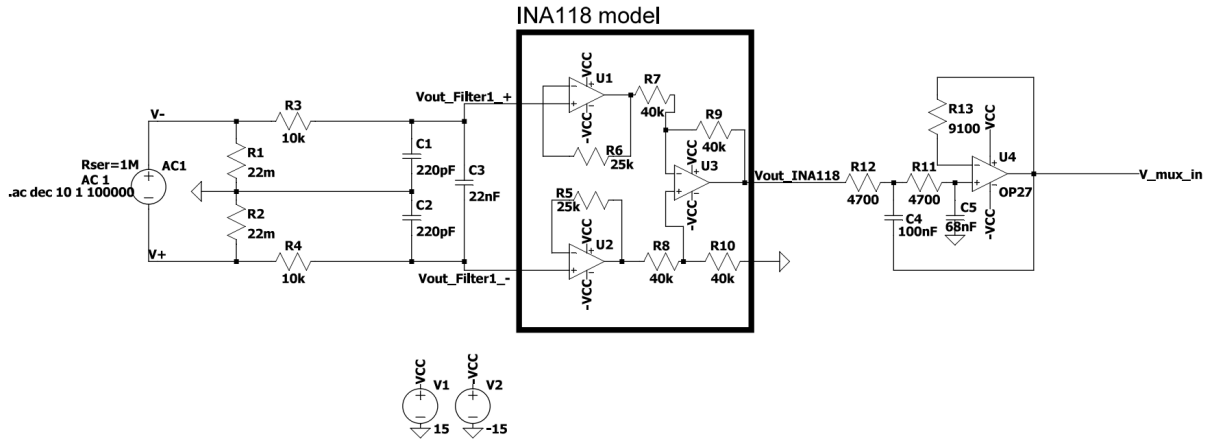


Figure 2.4: Filter schematic modeled in LT-Spice [2]

As shown in the schematic, the instrumentation amplifier INA118 was designed here with the simplified diagram described in its datasheet, see [7]. This simulation gives the following transfer function for the front-end, see figure 2.5.

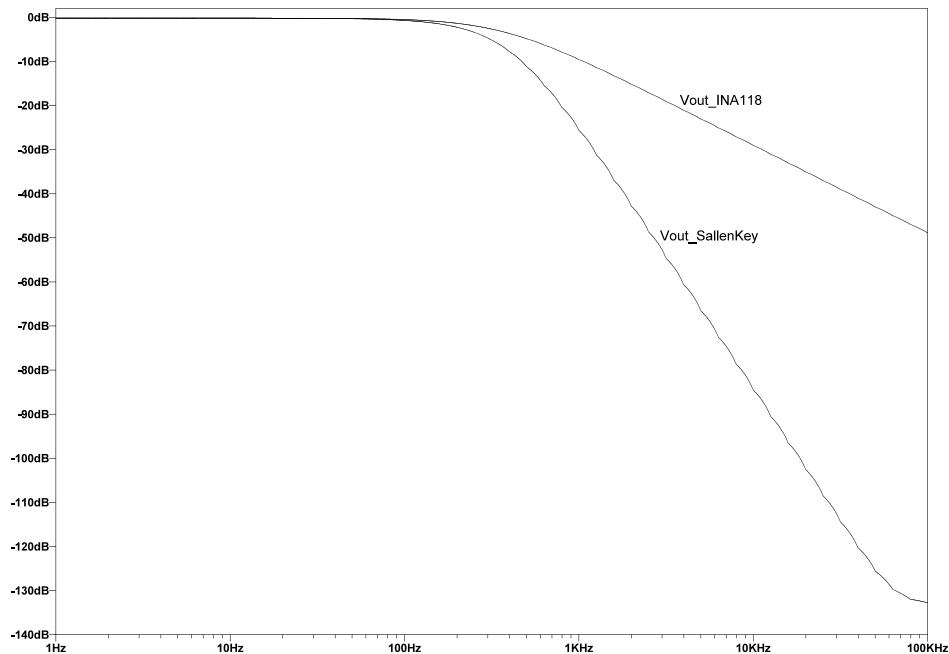


Figure 2.5: Transfer function of the modeled filter

After this filtering, the multiplexer used is the ADG444 [8]. This multiplexer has good switching characteristics and is able to switch between two channels in a maximum delay of 250 ns (4 MHz). The cross-talk between the different switches is from 100 dB and the off-isolation of 60 dB.

The problem of this inter-channel switching comes from the capacitance charge of the ADC which needs to be charged before having correct output values. Indeed, for the AD976, the input capacitance is from 22 pF with an input impedance of 23 k Ω . This results in a maximum capacitor charge time of 2.53 μ s, see equation 2.4.

$$\Delta_{ChargeADC} = R_{ADC} \cdot C_{ADC} \cdot 5 = 2.53 \mu s \quad (2.4)$$

By considering this charging time and that in each cycle the four inputs are sampled we can determine the maximum sample rate with the following equation 2.5.

$$SR_{ADC} = (\Delta_{ChargeADC} + \Delta_{switch}) \cdot 4 = 89.29 \approx 90 \text{ kHz} \quad (2.5)$$

Due to all this delays and required synchronised switching sequences, the complexity is highly increased and the 22.5 ks/s per channel (90 kHz for four channels) is quite impossible to reach.

Note : the reached stable acquisition sample rate for this card is of 4 ks/s per channel in practice.

Finally, we can summarize the analog front-end characteristics in table 2.1.

Characteristic	Value
3 dB Frequency	300 Hz
Steepness	60 dB/decade
INA118 max offset	50 μ V
INA118 drift	0.5 μ V/ $^{\circ}$ C
Max drift (eq. 2.1)	$\pm 7.5 \mu$ V
Estimated sample rate limit.	22 kHz/channel

Table 2.1: Characteristics of the analog front-end

Regarding this table, the precision of the front-end is largely sufficient to reach the 1 mV of precision. The big disadvantage is the maximum sample rate limitation due to the multiplexed single channel. Another negative point is the very low cut-off frequency of 300 Hz.

2.2.3. ADC

The chosen ADC was the AD976B from Analog Devices [4], the given characteristics of this ADC are given in the following table 2.2.

Sample rate	100 kHz
Input range	0 V to 10 V
Resolution	16 bits
Integral linearity error (INL)	± 2 LSB
Differential linearity error (DNL)	-1 LSB to 1.75 LSB
Full-scale Error (FSE)	± 0.25 %
Offset Error (OE)	± 10 mV

Table 2.2: Characteristics of the AD976B (see [4])

We can estimate the ADC precision and error variation with the previous table 2.2. For this system, the temperature drifts can be neglected as the temperature variation in the installation isn't high. The used method to estimate the ADC total error will be the root-sum-square (RSS) method, described in equation 2.6.

$$\varepsilon = \sqrt{E_1^2 + E_2^2 + E_3^2 + \dots + E_n^2} \quad (2.6)$$

The total error of the AD976B without any references for a gain and offset calibration would be :

$$\begin{aligned}
 DNL = 2.75 \text{ LSB} &\rightarrow DNL_{\%} = \frac{2.75}{2^{16}} \cdot 100 = 0.004\% \\
 INL = 4 \text{ LSB} &\rightarrow INL_{\%} = \frac{4}{2^{16}} \cdot 100 = \frac{1}{2^{14}} \cdot 100 = 0.006\% \\
 FSE &= \pm 0.25\% = 0.5\% \\
 OE &= \pm 10 \text{ mV} = 20 \text{ mV} = 0.1\%
 \end{aligned} \quad (2.7)$$

$$\varepsilon_{AD976B} = \sqrt{DNL^2 + INL^2 + FSE^2 + OE^2} = 0.51\% \rightarrow 102 \text{ mV} \quad (2.8)$$

In our case, as we have two reference voltages (that we consider as perfect references) the offset and gain error are corrected afterwards and can be neglected. The total error of the ADC is then equal to :

$$\varepsilon_{AD976B,calib} = \sqrt{DNL^2 + INL^2} = 0.007\% \rightarrow 1.4 \text{ mV} \quad (2.9)$$

We have to note that the 1.4 mV are only reached in case of a perfect 10 V reference channel and a right adjustment of the potentiometer **P1** (see appendix BEA-6U). In

addition to those conditions, due to the voltage divider applied on the external reference pin of the AD976B, the precision can be impacted by the operating temperature variation (100 ppm resistor precision). The summary of the BEAv1 ADC is described in the table 2.3.

Characteristic	Value
Sample rate	100 kHz
Number of channel	1
Best case ADC accuracy	1.4 mV
Reference temperature drift [9]	5 ppm/°C
Maximum reference voltage drift (eq. 2.3)	$\pm 50 \mu V$
Max reference resistor divider drift R72 and P1 (eq. 2.3)	$\pm 184.5 \Omega$
Max reference resistor divider drift R71 and P1 (eq. 2.3)	$\pm 61.5 \Omega$
Estimated maximum reference voltage divider drift (eq. 2.6)	$\pm 15.01 mV$

Table 2.3: Characteristics of the ADC and related circuitry

As exposed in table 2.3, this architecture could be outside from the requirements of 1 mV in certain cases. This is due to the choice of using the same reference voltage (10V) for the ADC (through an imprecise voltage divider) as for the offset and gain calibration channel. Finally, a wrong adjustment on the potentiometer P1 could drastically reduce the precision of measurement.

2.2.4. FPGA

The FPGA used for this design is a Spartan-3 from Xilinx [10], which is sufficient for this application but obsolete now. This FPGA was doing the following tasks on this architecture :

- Control of the ADC signals as well as a synchronised MUX switching
- Averaging the sampled values
- Sending the data through a multi-mode optic fiber data-link to the BEM
- Detect wrong on board voltages through supervisory circuits
- Display of detected errors on LEDs

2.2.5. Communication

For the communicating part, two multi-mode optic fiber transmitters were used to establish a redundant link. The transmitter used is the HFBR-1414TZ [11]. This transmitter

enables data link transmission up to 155 Mbaud/s which can be used with various encoding types.

On the FPGA a Manchester encoding at 1 MHz with a data-rate of 500 kbit/s was used. A higher data-rate was not used as it was not required with this sample rate (4 kS).

2.2.6. Main limitations and disadvantages

The main limitations and disadvantages of this card are the following:

- Sample rate limitation: the single channel ADC can reach 100 kS/s, but, due to the unique channel limit, a MUX was used to switch between both possible inputs as well as for the correction references channels. Indeed, the final maximum acquisition per channel with correction and MUX delay is only of 4 kS/s.
- ADC reference voltage calibration requirement: as shown in the appendix BEA-3U, a potentiometer is used to divide the reference source to reach a precise external reference for the ADC. This design requires a manual calibration for each card before their deployments.
- Data-rate of Manchester encoding over the multi-mode optic fiber links also limits the output sample rate of the BEA and needs to be increased in the new specification.
- Missing over and undervoltage protection and fuses. The supervisory circuits also needs to be used as on the current system.
- Obsolete components: this card was designed in 2006 which explains why many of those chosen components are now obsolete. A complete new design is required.
- Form factor : two different cards are used the 3U format and 6U format just for compatibility reasons between different experiments where this card is required. The card has two different designs and the idea would now be to use the same one for both systems by having an optional extension card to reduce the costs.

2.3. Purpose of a new Beam Energy Acquisition card

The Beam Energy Tracking System (BETS) was initially designed for the LHC Beam Dumping System (LBDS) without the focus to be deployed on other installations . The BETS has been adapted as far as it could be to fulfil the needs. However, the current BETS has weaknesses and limited functionalities.

The BEA card needs to be completely redesigned in order to meet the new requirements. A theoretical research work has to be done in order to find solutions to improve this system in term of hardware as well as gateway/software. The following weaknesses need to be redesigned completely in this work, see table 2.4.

Weakness	Cause	Req. nb.	Description
Sample rate	Architecture of A/D conversion	R1	New A/D architecture
Data-rate	Limited data-link	R2	New data-link architecture
Calibration	No calibration	R3	Calibration methods
Protections	Missing protection circuits	R4	Protect supply and inputs
Obsolescence	Obsolete components	R5	Use latest components
Form factor	Two production cards	R6	Unique card with extension

Table 2.4: Requirements of this research work

As shown in table 2.4, those requirements need a theoretical research work to be fulfilled. The results set as final objectives for each requirement within this project are defined in table 2.5.

Req. nb.	Description	Objective to reach
R1	New A/D architecture	100 kS/s per channel
R2	New data-link architecture	Full payload within the 100 kHz
R3	Calibration methods	Accuracy of 1 mV
R4	Protect supply and inputs	Diode, fuses and supervisory circuits
R5	Use latest components	Components available for the next 10 years
R6	Unique card with extension	Simple extension for one main card

Table 2.5: Requirements goal of this work

For the new card, a new specification is detailed in the next section based on those requirements, see 2.4.

2.4. New specification

The new specification is described by these different main points :

- **Control and processing unit** : this unit is responsible of the sequencing of the card operations. This means communication with the ADC, optical link with the BEM, and signal processing as well as calibration method.
- **Analog-Digital-Converter part** : this is the most important part to be renewed, it is responsible of the acquisition of the DCCT output voltages and other use-case voltages.
- **Communication** : those cards are situated close to the DCCTs measuring the magnet current (converted in analog voltages) and also to other systems. Once acquired through the ADC part, those values are required at multiple hundreds of meters or kilometers which requires the optical link.

- **Configuration and error detection** : this part describes the required configuration and error detection circuits.

Those four parts are described in figure 2.6.

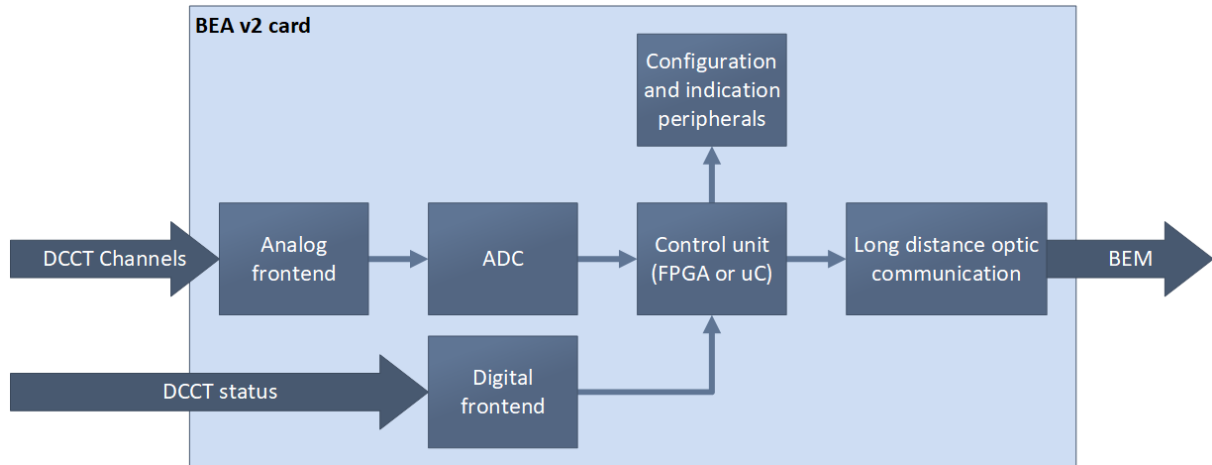


Figure 2.6: Block diagram for the new specification

This card will be connected as the previous one through a 3x32 pins connector, called FGC-2-Connector. The input and power supply pins are fixed as following, table 2.6. The supply provided through these pins must be protected through fuses to avoid disturbing the other systems connected to the same main supply in case of a short-circuit.

Card format	Row	Pin number	Signal name	Description
3U/6U	A/B/C	2	P15V0_in	Positive 15 V source
3U/6U	A/B/C	3	N15V0_in	Negative 15 V source
3U	A/B/C	5	P5V0_in	Positive 5 V source
6U	A/B/C	5	x	Has to be left floating
6U	A	10	DCCT_A_Status	Status signal DCCT
6U	B	10	DCCT_B_Status	Status signal DCCT
3U/6U	A	21	CH_3_N	Negative analog line channel 3
3U/6U	A	22	CH_2_N	Negative analog line channel 2
3U/6U	B	21	CH_3_P	Positive analog line channel 3
3U/6U	B	22	CH_2_P	Positive analog line channel 2
3U/6U	A	30	CH_1_N	Negative analog line channel 1
3U/6U	A	31	CH_0_N	Negative analog line channel 0
3U/6U	B	30	CH_1_P	Positive analog line channel 1
3U/6U	B	31	CH_0_P	Positive analog line channel 0

Table 2.6: FGC-2 connector pins

2.4.1. Control and processing unit

For this part, CERN usually use FPGAs due to the flexibility and speed advantage that they offer. Here, the choice is limited to the last 7-series FPGA from Xilinx [10], as it was defined since the beginning of the project for this new card. This is because this section (and many CERN sections) is used to work with Xilinx products and tools and the 7-series FPGAs are the newer on the market. One important point in the FPGA choice is that it has to be fully compatible to the communication aspect of our specification.

2.4.2. ADC

The analog to digital conversion is the BEA part which really needs to be improved between the old and new system due to the slow max sampling rate of the BEA v1 (4 kHz/ch) which is already used. The new BEA A/D conversion rate should reach at least 100 kHz/channel. The resolution required is 16 bits in the range 0 to 10V to match the resolution of the previous system as well as an accuracy of approximately 1 mV (reached with the reference signal sampling, assuming no temperature drifts). The number of sampling channels will here be increased to 4 to have the possibility to be compatible with other systems where the BEA will be used. Last but not least, a calibration method should be chosen here to always stay in the area of the 1 mV accuracy. The specification of the ADC is summarized in table 2.7.

Number of input channels	4 + reference channels
Sample rate	100 kHz/ch
Input range	-10 V to 10V
Resolution	16 bits from 0 V to 10V
Accuracy	approx. 1 mV

Table 2.7: ADC specification

2.4.3. Analog front-end

For the analog front-end, approximately the same front-end architecture should be used. As shown in the appendix BEA-3U, a high-impedance input is used with a differential to common mode conversion by using a high precision instrumentation amplifier. A low pass filtering with a very narrow cut-off frequency (-3 dB at around 3 kHz) is applied as the high frequency parts of the signals will introduce additional noise. Additionally, an over/under-voltage protection is required to avoid having more or less than 10 V/-10 V on the analog-inputs to protect the ADC. The given specification for the filtering, input impedance and signal mode are the following, table 2.8.

Front-end mode	Differential
Cut-off frequency	-40 dB at 50 kHz (half sampling freq.)
Input impedance	10 M Ω
OV/UV protection	10 V / -10 V

Table 2.8: Analog front-end specification

2.4.4. Optic fiber transmitters

For the communication part, optic fiber is used for most of the CERN applications as the distances between the different LHC points are of multiples km and to be more robust against the high electromagnetic noise which is present in the tunnel.

To be compatible with the current system as well as the BETSv2 and with other potential projects, both Single-mode (SM) and Multi-mode (MM) optic fiber transmitters are required. Indeed, MM optic fiber was chosen a few years ago because of the cheaper costs of the transmitters and cable. Now, with the massive use of single mode optic fiber for private and public sectors the costs drastically decreased.

The SM optic fiber should be introduced in the new BETS architecture. A redundant link will be established between the BEA and the BEM card. The BEA will also be able to receive data from the BEM as a half-duplex SM link. The table 2.9 describes the optic fiber requirements.

	Current used MM	Compatibility MM	New SM link
Range	< 1 km	< 1 km	< 10 km
Used throughput	500 kbit/s	25 Mbit/s	1.25 Gbit/s
Redundancy	not in BETSv1	Possible	Yes
Type of link	Simplex	Simplex	Duplex

Table 2.9: Optic fiber links in the current systems versus new specification

The new singlemode optic fiber link data-rate was fixed to 1.25 Gbit/s to be compatible to the receiver side from the new BEM which will be using the same data-rate as the external clients (typically MPE).

2.4.5. Configuration and error detection

As this board will be used on diverse projects the following configuration requirements are needed :

- Transmission frame architecture, single or multi-mode transmission as well as a partial channel selection should enable fast compatibility without changing the gateway through an hexadecimal switch.

- The 3U form factor must be able to be extended to a 6U form factor through a mechanical and electrical connector.

Additionally, LEDs must be used on the gateway as well as hardware part for critical error detection. Each different supply voltages on the board should be monitored through supervisory circuits generating an error linked to the communication and LEDs.

3 Electronic development

This chapter covers the electronic development part of the project. In this first section, the ADC calibration method will be detailed. The components in this section were chosen not only based on the new specification but also on their availability due to the current delivery delays (electronic components shortage).

3.1. ADC calibration methods

Before designing the hardware, the different calibration methods to reach the maximum precision of the ADC were studied. Indeed, different calibrations exist to correct two types of ADC-errors, the **linearity errors** and the **non linearity errors** described in the next subsections.

3.1.1. Linearity calibration (Offset and gain)

The linearity calibration is used to correct linearity drifts from the ADC, its internal or external reference voltage and the analog front-end linear deviations. The linear error can be described in two parts :

- Offset error : defines the deviation of the conversion transfer function from the ideal straight line at zero input voltage [12]. If the transition from the output value from 0 to 1 (raw converted value) does not occur at an input value of $1/2$ LSB then there is an offset error. This error needs to be corrected before doing any gain correction or further correction.
- Gain error : defines the deviation of the last output step from the ideal straight line after compensating the offset error [12]. At this step the 0 V point is calibrated and the linear deviation in the upper steps can be compensated by applying an additional gain correction.

To be able to do a proper correction, reference voltages are required here. Indeed, as this linear error can be described through a first order function, two known values need to be used at the input for being able to estimate the correction gain and offset at the output of the ADC.

In order to be able to calculate correctly our offset and gain correction values during the operation, one precise external reference with low temperature drift is required additionally to the ground measurement. This correction can easily be done on the device during run-time or only once (see 3.1.3).

The calibration algorithm used is described in the next chapter, see section 4.3.3.

3.1.2. Non linearity calibration

The non linearity calibration has a higher complexity. Indeed, non linearity errors are mostly due to the ADC imperfections. The two types of non linearity errors are the "Integral" and "Differential" errors. The integral non linearity error is defined as the maximum vertical difference between the actual and the perfect curve (y-axis). The differential non linearity error is defined as the maximum and minimum difference between the step width and the perfect LSB width (x-axis).

Normally, this correction should not be required in our case as the linear calibration should be sufficient to reach the specification precision.

To correct those, a look-up table could be used in order to correct each value with measured errors during a production-calibration process, however, this method requires a large amount of internal memory, in our case that would be around 590 kB. Another strategy would be to measure the errors and to calculate the polynomial function coefficients to reduce them. This last option was implemented in the next chapter, see section 4.3.3.

3.1.3. One-time and run-time calibration

Calibration methods can be used at different times. As a matter of fact, depending on the required precision, external hardware requirements and calculation time, these calibration methods should be performed during run-time or only one time at the power-up or production phase [13].

In our case, the two point calibration will be carried out cyclically at each measurements as the calculation requirements are low and the hardware will be present on the board. For the polynomial correction calibration, the goal would be to do a one time calibration during the production phase.

3.2. Hardware

This part is about the hardware development. It will describe what components were chosen and why, as well as the required circuits to match the requirements. This begins with the analog part of the card and continues with the digital part with the FPGA and power supply circuitry. Finally, the communication hardware is introduced.

3.2.1. Analog part

The analog part should be constituted of a first analog front-end including a filtering and buffering followed by the ADC. At this stage, we additionally need to sample two references in order to perform a two point gain and offset calibration. Three possible architectures were considered.

The first one would be to use a MUX and stay with quite the same architecture as shown in the old schematic from appendix BEA-3U and BEA-6U with a single channel ADC.

The second one would be to use an eight channel input ADC with four input channels coming from the DCCT and the additional references on the remaining channels (with two unused channels).

The last possible architecture would be to use six same single channel ADCs. The different architectures are represented in the following diagram 3.1.

The advantages and disadvantages of those architectures are listed in the following table 3.1.

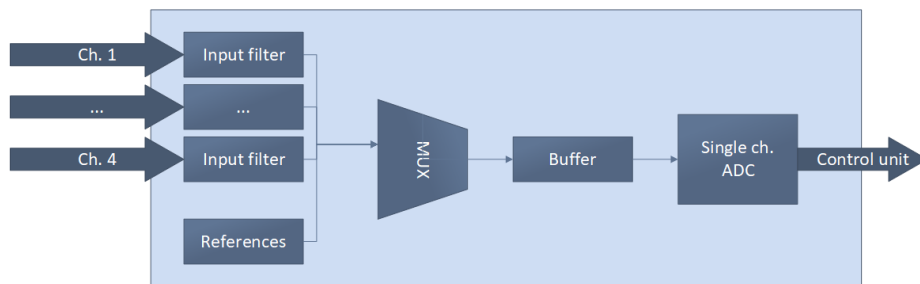
Architecture	3.1a	3.1b	3.1c
Cost	Low	High	Middle
Taken place	Low	High	Middle
Assumption	-	Same ADCs char.	Same channels char.
Advantages	No assumptions	Simple FPGA interface	Integrated switching
Disadvantages	Noise/Delay Uncertain sample rate	Space requirements	Complex interface

Table 3.1: Optic fiber links in the current systems versus new specification

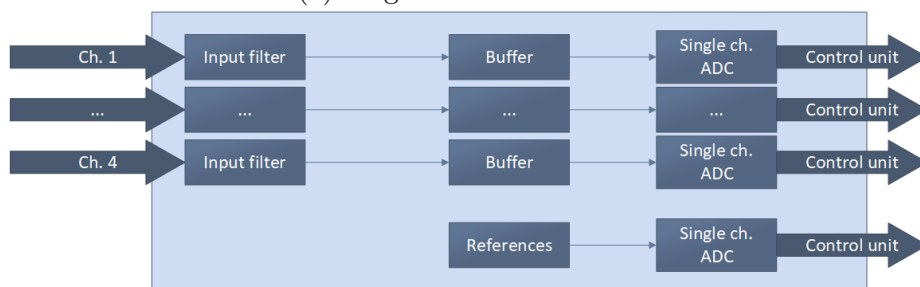
Due to limited space on the PCB, the choice 3.1b or 3.1c are privileged here. In the next section, the different possible and compatible ADC(s) with this system will be compared before doing the final architecture choice.

Analog-Digital-Converter

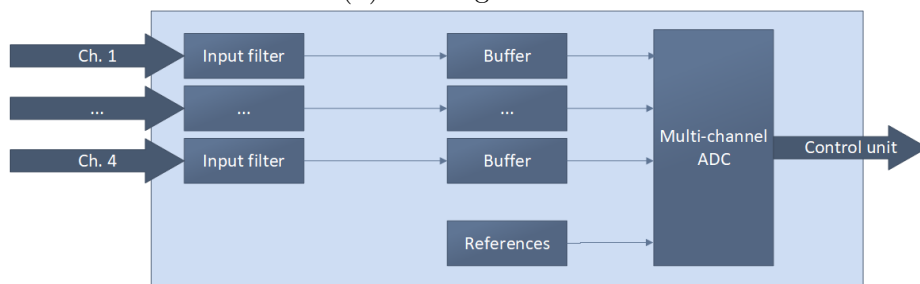
The ADCs from both vendors, Texas Instruments [14] and Analog Devices [15] were compared. As explained in the last section, ADCs with four or eight channels were privileged for the new architecture.



(a) Single ADC with MUX



(b) Six single ADCs



(c) Integrated 8-channel ADC

Figure 3.1: Considered ADC-architecture

The most interesting and available ones are presented in the given table 3.2. They all respond to the mentioned specification. The product life status/year of the ADCs are also important here as this card needs to be in operation as long as possible. The accuracy

ADC	Bits	Accuracy	Accuracy calib.	kHz/ch	Price	Avb.	Year
LTC2357	18	40.96 mV	571 μ V	350	45 €	>100	2017
LTC2335-18	18	40.96 mV	492 μ V	125(4ch)	48 €	>500	2016
AD7609/08	18	9.7 mV	1.1 mV	200	42 €	>1000	2019
ADS8694	18	10.3 mV	810 μ V	125(4ch)	21 €	>500	2015
ADS8698	18	10.3 mV	810 μ V	125(4ch)	17.5 €	>1000	2015

Table 3.2: Comparison of ADCs (Availability on Octopart [5])

before and after a two point gain and offset calibration were calculated with the same principle as in section 2.2.3.

The final choice was the AD7609 [16], this ADC is in a production state and pin to pin compatible with many others ADCs of the AD76-family. As it has 8 channels, the architecture presented in figure 3.1c was chosen.

This ADC has an internal 2.5 V reference which has a temperature deviation of ± 10 ppm/ $^{\circ}$ C (300 ppm absolute deviation with $\Delta T = 30$ $^{\circ}$ C). To increase the precision in dependence of the temperature variations of the ADC, an external voltage reference of 2.5 V is used here. The different possible references within ± 3 ppm are described in table 3.3. Due to

Reference IC	Precision [ppm/ $^{\circ}$ C]	Price	Avb. (Octopart 05/2023, [5])
LM4140ACM-2.5	± 3 ppm/ $^{\circ}$ C	3.5 €	>500
ADR4525BRZ	± 2 ppm/ $^{\circ}$ C	10 €	>500
ADR4525CRZ	± 1 ppm/ $^{\circ}$ C	18 €	<50
LT6657AHMS8-2.5	± 1.5 ppm/ $^{\circ}$ C	13 €	<30
LT6657BHMS8-2.5	± 3 ppm/ $^{\circ}$ C	8.5 €	<30

Table 3.3: Comparison of the possible external references

the huge price and availability difference, the external reference from Texas Instrument was chosen (LM4140ACM-2.5). In our case the temperature variation will not exceed 30 $^{\circ}$ C which means that we can have the following voltage deviation, see equation 3.1.

$$\Delta V_{REF} = 30 \cdot 2.5 \cdot \pm 3 \cdot 10^{-6} = \pm 225 [\mu\text{V}] \quad (3.1)$$

We know that the AD7609 [16] amplifies this reference value with a gain of 4 to reach the 10 V reference which is then used in the ADC to convert the channel values, this results in the following maximum deviation error, equation 3.2.

$$\varepsilon_{Ref} = \Delta V_{REF} \cdot 4 = \pm 900 [\mu\text{V}] \approx \pm 6 [\text{LSB}] \quad (3.2)$$

Analog front-end

As described in the specification, see 2.8, we require a differential front-end. A low pass filtering is then required to reach the -40 dB at the half sampling frequency. The high input impedance and RC-filtering was based on the previous schematic, see appendix BEA-3U and BEA-6U. The additional voltage protection was also added, see figure 3.2.

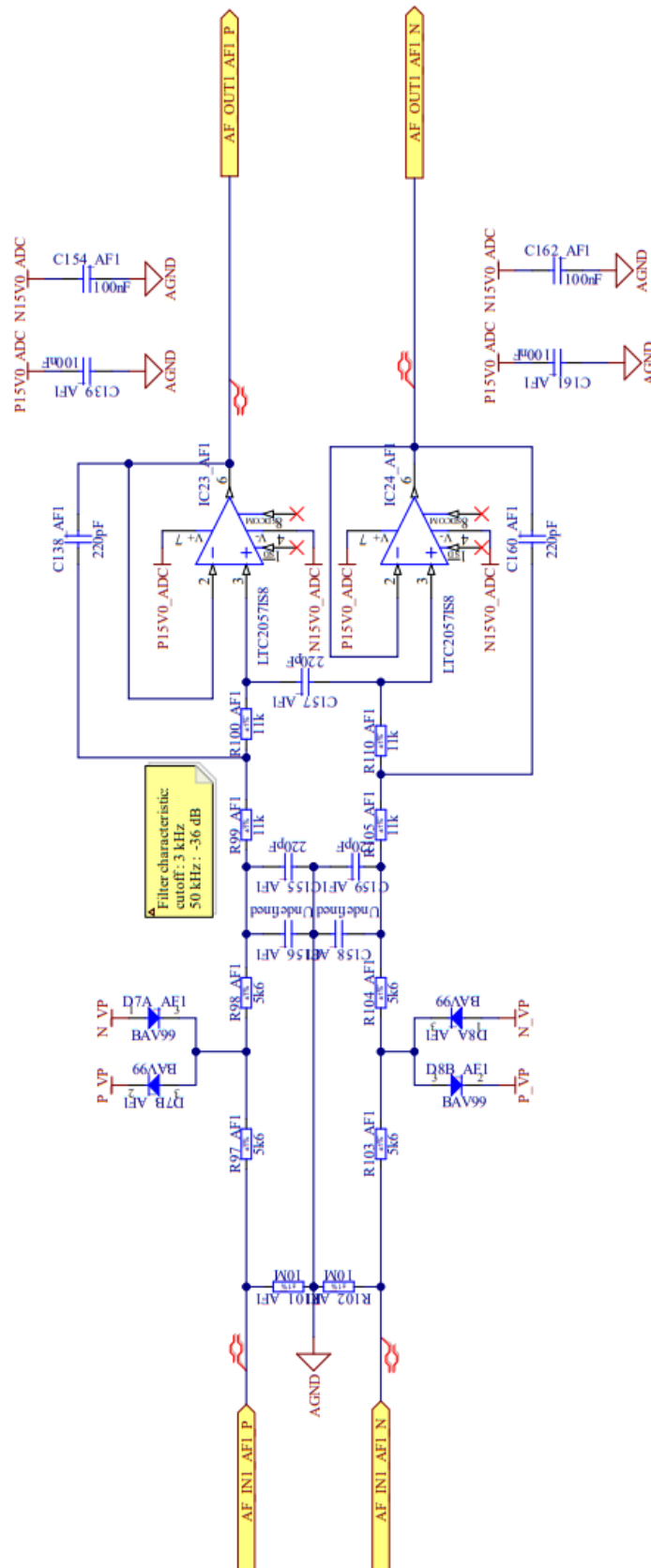


Figure 3.2: Analog front-end schematic

Two precision ($< 10 \mu\text{V}$ offset) operational amplifiers were used to add an additional Sallen-Key low-pass filtering. One disadvantage of the Sallen-Key filtering is that it adds a capacitive coupling between the ADC and the input signal. The complete schematic was then simulated on LTSpice [2] to get the total frequency response of the filter. The advantage of this architecture is also to have the possibility to use those amplifiers as simple buffers by removing C128 and C160. The LTSpice simulation is shown on figure 3.3.

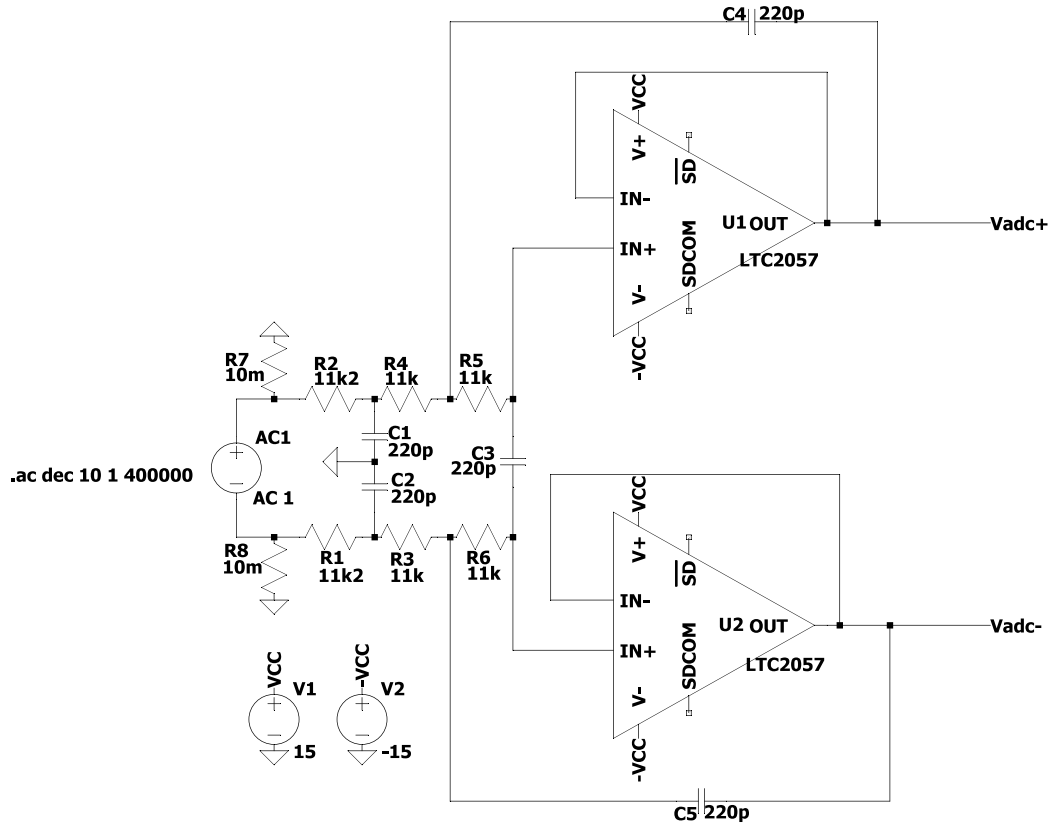


Figure 3.3: LTSpice schematic used to simulate the frontend

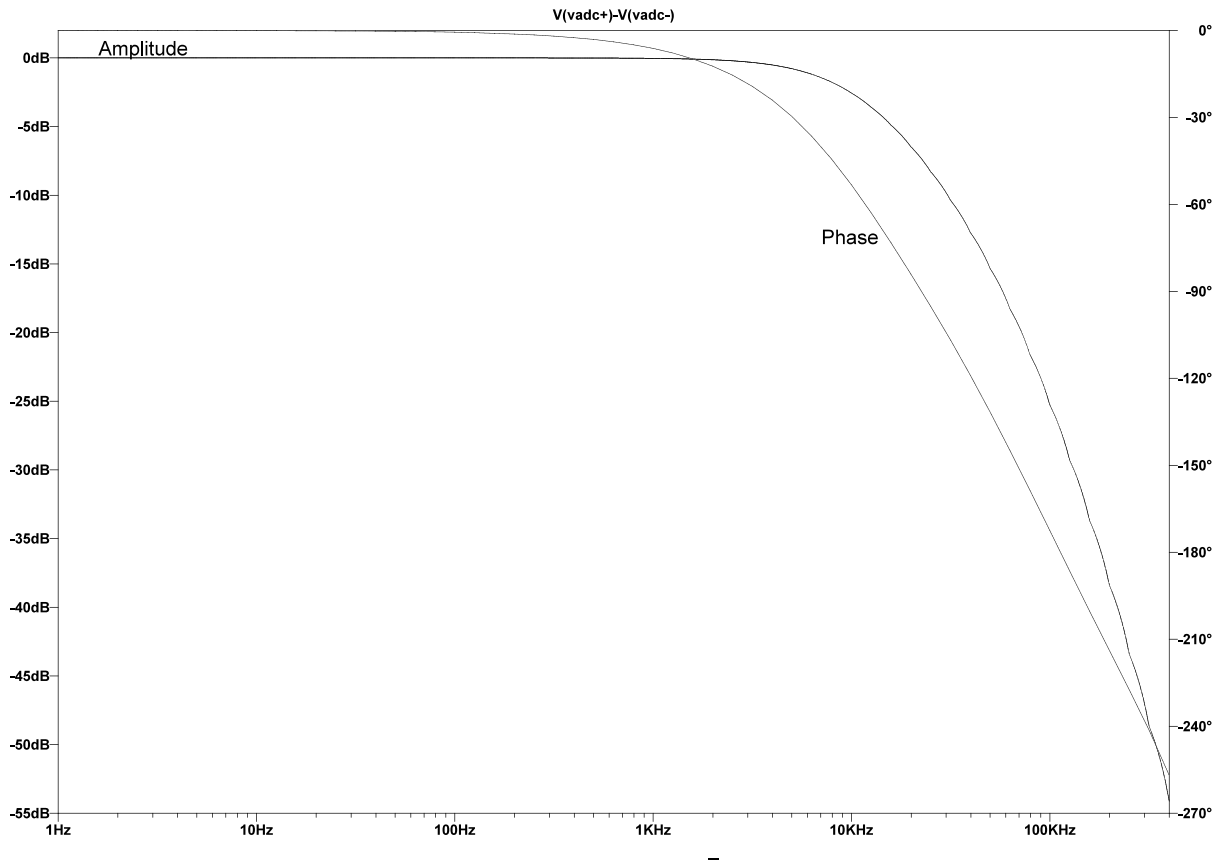


Figure 3.4: LTSpice simulation transfer function of the filter

External precise references

As explained in section 3.1, to reach the best precision an external reference is required to do the gain and offset error calculation.

3.2.2. Digital inputs

For the 5 V digital inputs coming from the DCCTs we just need an over- and under-voltage protection as well as a buffer converting the 5 V signals to the FPGA logic level of 3.3 V. The corresponding schematic is shown in figure 3.5.

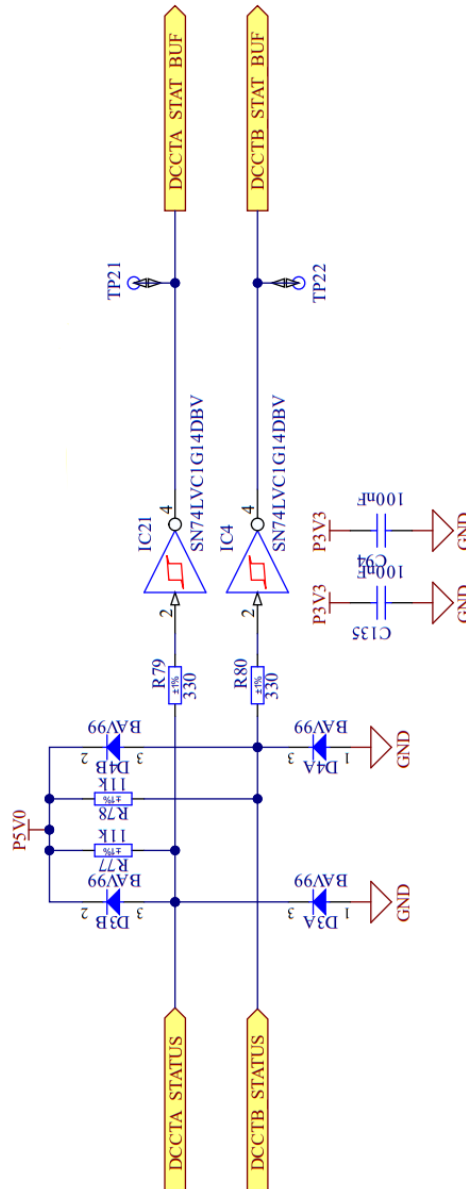


Figure 3.5: Analog front-end schematic

Those buffers and diodes were chosen as they are already used in the ABT-BTE section on many other cards.

3.2.3. FPGA

Two different FPGA were possible in the product catalog of already used FPGA by CERN. The first one was a Kintex Ultrascale which had much more DSP slices, logic cells and IOs which were not necessary for this application and the second one an Artix-7 based FPGA which is closer to our requirements.

The Artix-7 A35T belongs to the recent 7-Series FPGA from Xilinx [10]. The characteristics of this FPGA are the following, table 3.4.

Look-Up-Table (LUT)	20800
Flip-Flop (FF)	41600
Digital Signal Processing (DSP)	90
GTP Transceiver	4
GTP Receiver	4
User IOs	250

Table 3.4: Artix-7 A35T-FGG484 main characteristics

One disadvantage of such an FPGA is, in our case, the requirement of four different precise supply voltages. The power part design will be described in the section 3.2.4.

The used FPGA is the Artix-7 A35T from Xilinx [10]. The configuration circuitry of the FPGA was realized according to the documentation from Xilinx. A clock of 100 MHz was used. The designed configuration circuitry should be the following :

- Switching possibility between Master SPI and JTAG driven memory
- Default pull-up on IOs disabled
- Gateware reset on power-on

Additionally, on the power supply part, the voltages described in table 3.5 were used. Those voltages need to be within a recommended range which requires a minimal inductance and capacitance at the supply output, see section 3.2.4.

FPGA part	Core and GTP (1 V)	IOs (3.3 V)	Aux (1.8 V)	GTP (1.2 V)
Range	± 0.05 V and ± 0.03 V	-	± 0.09 V	± 0.03 V

Table 3.5: Supply voltages precision requirements for the different FPGA parts

In the next section, the different power supplies circuits design will be shown. In the chapter 4.3.6, the used logic cells, DSP slices and IOs on the latest gateware will be compared to the available one.

3.2.4. Power supplies

As described in table 2.6, the available input supplies are 5 V, 15 V as well as -15 V. We additionally need the following supply voltages, table 3.6. They are required to drive our FPGA core, auxilliary supply, IOs as well as the gigabit transceiver.

Voltage	Use-case	Derived from
3.3 V	FPGA IOs, ADC and SM	5 V
1.8 V	FPGA Aux supply	5 V
1.2 V	FPGA GTP	5 V
1.0 V	FPGA Core	5 V

Table 3.6: Supply voltages requirements

Power estimation

The total power consumption needs here to be estimated. For the FPGA-part a Xilinx-Tool [10], the Xilinx Power Estimator [17] in Excel was used. The output of this power estimator tool is given in the appendix Power estimation (XPE). For the other components, we assume that they are all working at their maximum current.

Another important factor is the power-on charging current of all the capacitors used on the PCB. The estimated consumption at startup (capacitor peak) and during operation is shown in table 3.7.

Voltage	Delay (ms)	Max power-on-peak	Maximum consumption	Available
15 V	0	30 mA	30 mA	-
-15 V	0	30 mA	30 mA	-
5 V	0	600 mA	0.8 A	-
3.3 V	6	215 mA	0.5 W + 0.4 W (SFP)	13.2 W
1.8 V	4	42 mA	0.7 W	2.16 W
1.0 V	2	640 mA	0.62 W	4 W
1.2 V	8	136 mA	0.12 W	1.44 W

Table 3.7: Maximum and peak consumption per voltage source

Note : the consumption of the 5 V includes the four derived voltages 3.3 V, 1.8 V, 1.0 V and 1.2 V which are separately estimated below.

To get those different supply voltages, an integrated solution was chosen, the ADP5051 [18]. This is a quad buck regulator with hardware programmable output voltages. It also has integrated supervisory circuits to monitor that the input voltage as well as the different output channels aren't below a given threshold. It also features an I2C-bus to configure those different thresholds as well as a temperature threshold. Those thresholds can be linked to available interrupts pins as well as an internal reset.

The corresponding schematic is shown in appendix Remote Acquisition Transceiver (RAT / BEAv2). Two external MOSFETs are required for the first two channel outputs (up to 4 A) and two internal MOSFETs are used for the two other channels 3 and 4 (up to

1.2 A).

The power-on sequence used was based on the FPGA requirements, section 3.2.3. Normally, none of the generated voltages consumption would reach 1.2 A, see table 3.7. The two upper channels were used for the 3.3 V (IOs, single mode transmitter) and 1.0 V (FPGA core) as those should use higher currents for a longer time than the other channels in our application.

Required capacitance and inductance per channel

Concerning the voltage ripple acceptance of the FPGA for those voltages, the formula mentioned in the data-sheet of the ADP5051 [18] was used to calculate the minimum required capacitance and inductance at the channel outputs, see equation 3.4 and 3.3.

$$L_{ch} = \frac{(V_{in} - V_{out}) \cdot D}{\Delta I_L \cdot f_{switch}} \quad (3.3)$$

$$C_{ch} = \frac{\Delta I_L}{8 \cdot \Delta V_C \cdot f_{switch}} \quad (3.4)$$

To use those equations the following values are required :

- ΔI_L which represents the inductance ripple current which is at approximately 30 % of the maximum channel current.
- ΔV_C which represents the channel output voltage ripple.
- f_{switch} which is the switching frequency configured through the R_{RT} resistor (600 kHz used here, configurable to up to 1.2 MHz).
- V_{in} which is the input voltage of the ADP5051, 5 V.
- V_{out} which is the output voltage of the corresponding channel.

The table 3.8 was filled using those formulas and based on the requirements given in the FPGA section, table 3.5.

Channel	1 V	3.3 V	1.8 V	1.2 V
Chosen tolerance (/10)	± 0.003 V	± 0.05 V	± 0.009 V	± 0.003 V
Required inductance	1.11 μ H	1.56 μ H	5.33 μ H	4.22 μ H
Used inductance	1.5 μ H	1.5 μ H	5 μ H	5 μ H
Required capacity	83.3 μ H	5 μ H	83.3 μ H	25 μ H
Standardized to used capacities	141 μ H	47 μ H	94 μ H	47 μ H
Max voltage ripple (ΔV_C)	0.0018 V	0.0053 V	0.0008 V	0.0016 V

Table 3.8: Required and used capacitance/inductance on each generated source

Fuses

To avoid disturbing the other cards which are using the same FGC-2 supplies in the case of a short-circuit or overload, fuses were added to the design. The fuses in table 3.9 were chosen with the power estimation in table 3.7.

	5 V	15 V	-15 V
Max consumption	max 0.8 A	max 30 mA	max 20 mA
Chosen fuse	1 A	100 mA	100 mA

Table 3.9: Chosen fuse protections

3.2.5. Peripherals

Some peripherals are additionally needed on our card to meet the specification requirements.

Hexadecimal selector

An hexadecimal selector is required to enable having up to sixteen different configurations without having to reflash the FPGA memory.

It enables us to change those main configurations in the gateway to be easily compatible with multiple systems :

- Multi-mode and single-mode frame architecture (3U, 6U)
- Sample rate configuration
- Oversampling configuration
- Calibration configuration

The different configuration parameters are described in the gateway section 4.3.1.

EEPROM memory

A small 2kbits EEPROM memory was added to the board. This memory was added to store calibration coefficients if a non-linearity or temperature based correction is required.

UART connector

The UART-connector was added, enabling a configuration communication between a computer and the FPGA. This serial communication will enable us to measure the non-linearity errors and store the corresponding coefficient in the EEPROM after the production phase. The connector pins placement was based on the FTDI USB to TTL connector, see [19].

Buttons

Two reset push buttons were added. One is resetting the supply voltage chip, by restarting the FPGA power-on sequence. The other one is a gateway reset which is internally linked to the different IPs from the FPGA.

Another user push button was added as a "not mounted" part.

LEDs

As described in the specification, section 2.4.5, LEDs are required on the front panel of this card. This enables easy identification of the card has an error in case of troubleshooting detection. Two states LEDs are used here which can be red, green or orange(both on). In each "Dialight LED" two LED pairs (top and bottom) are present. One LED pair was used for the supply voltage status and three others for different status signals internally generated by the FPGA. Those are described in the table 3.10.

Component	LED pair	Color	Name on FP	Description
LD1	Bot (A)	Green	Sup	Power on sequence is done
LD1	Bot (A)	Red	Sup	Supply is in reset state
LD1	Top (B)	Green	DCCT1	DCCT 1 status is ok
LD1	Top (B)	Red	DCCT1	DCCT 1 status is wrong
LD2	Bot (A)	Green	DCCT2	DCCT 2 status is ok
LD2	Bot (A)	Red	DCCT2	DCCT 2 status is wrong
LD2	Top (B)	Green	Thd	Board supervised thresholds are ok
LD2	Top (B)	Red	Thd	Board supervised thresholds are wrong

Table 3.10: Used LEDs and description

Supervisory circuits

Another important point which is mentionned in the specification section 2.4.5 is that each voltage source has to be monitored to be able to detect any supply default. Concerning the FPGA sources given by the ADP5051, an internal supervisory circuit monitors each channel and generates an error through I2C or through the linked interrupt. For the 5,15 and -15 V a dedicated chip was used, the LTC2909 [20]. This chip enables the under- and over-voltage monitoring through a resistor divider and a buffered output linked to the FPGA here, see appendix Remote Acquisition Transceiver (RAT / BEAv2), section "Power management". The over-/under-voltages thresholds are fixed 0.5 V upper and below from the optimal voltage.

3.2.6. Multi-mode transmitters

Two multi-mode transmitters are on the PCB to be fully compatible with the old BETS. The same HFBR-1414TZ [11] transmitters are used as no newer version exists and as they fulfill the BETS-requirements. This enables transmission rates up to 160 Mbaud if the controlling hardware meets those switching speed. To do so, as the FPGA works with a 3.3 V TTL output, the recommended NAND-Gate was used to convert the signal to 5 V by having a high enough output current. This NAND-gate is the 74ACT00SX [21] which is the newer version of the 74ACT00. It is fully compatible with a high frequency TTL-Input. The ACT version has a lower threshold input which enables to have the 3.3 V to 5 V conversion. The schematic between the 3.3 V TTL output and the optic output is shown in figure 3.6.

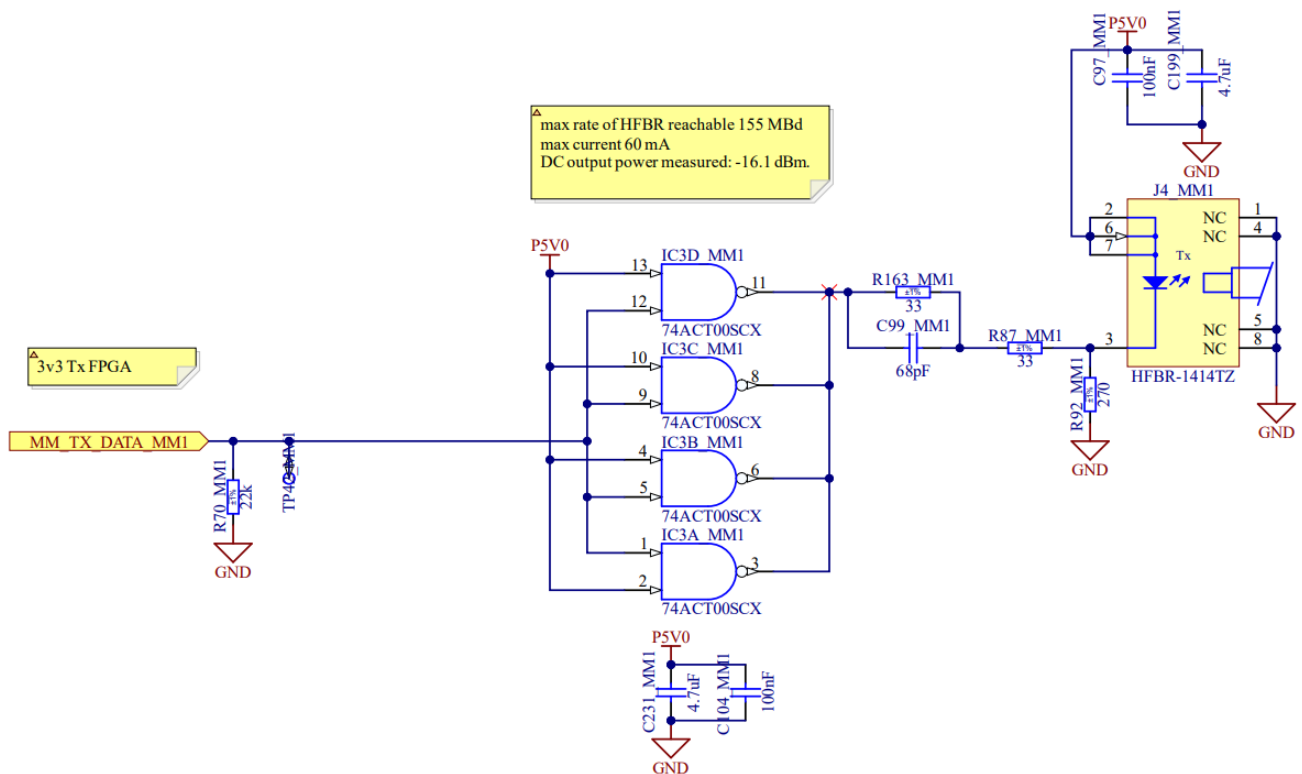


Figure 3.6: Multi-mode schematic

3.2.7. Single-mode transmitters

The single-mode transmitters are driven by the GTP-transceiver of the Artix-7. On the Artix-7 A35T, they can operate at up to 6.25 Gbit/s and four transmitters and receivers pairs are available. In our case, we only use two transceivers. The receivers are not required in this application but as those don't require any supplementary hardware, it was designed to be able to use them.

An additional 125 MHz clock with a differential pair output was required for the GTP

transceiver. Internally, those 125 MHz are then used by a PLL to get our precise GHz carrier signal.

Each clock, receiver and transmitter signal needs to be decoupled with a recommended decoupling capacitor of 100 nF to assure that no DC component comes to the GTP-transceiver, see 3.8. For the connector and cage (see figure 3.7), a fixed specification for all the different constructors was defined by the Storage Networking Industry Association (SNIA). This specification is available under the SNIA website [6].

The pins functions are described in table 3.11.

Pin name	Function	Description
VeeT	Transmitter GND	Transmitter ground
VeeR	Receiver GND	Receiver ground
VccR	Receiver Vcc	Receiver supply
VccT	Transmitter Vcc	Transmitter supply
TX_FAULT	Transmitter fault indication	Require a pull-up, high when fault
TX_DISABLE	Transmitter disable input	Require a pull-up, enable when low
MOD_DEF2	Module Definition 2	Require a pull-up Data line I2C for serial ID
MOD_DEF1	Module Definition 1	Require a pull-up Clock line I2C for serial ID
MOD_DEF0	Module presence	Grounded by the connector
RATE_SELECT	Select between full or reduced BW	Require a pull-up Low is reduced BW, high is full BW
LOS	Loss of signal	Require a pull-up Input power below sensitivity
TD+/-	Transmitter input differential pair	Recommended btw 500 and 2400 mV
RD+/-	Receiver input differential pair	Output btw 370 and 2000 mV

Table 3.11: SFP connector pins [6]

The schematic for both connectors and the corresponding GTPs was done with the specification [6] and the Xilinx GTP recommendations [10]. See figures 3.7 and 3.8.

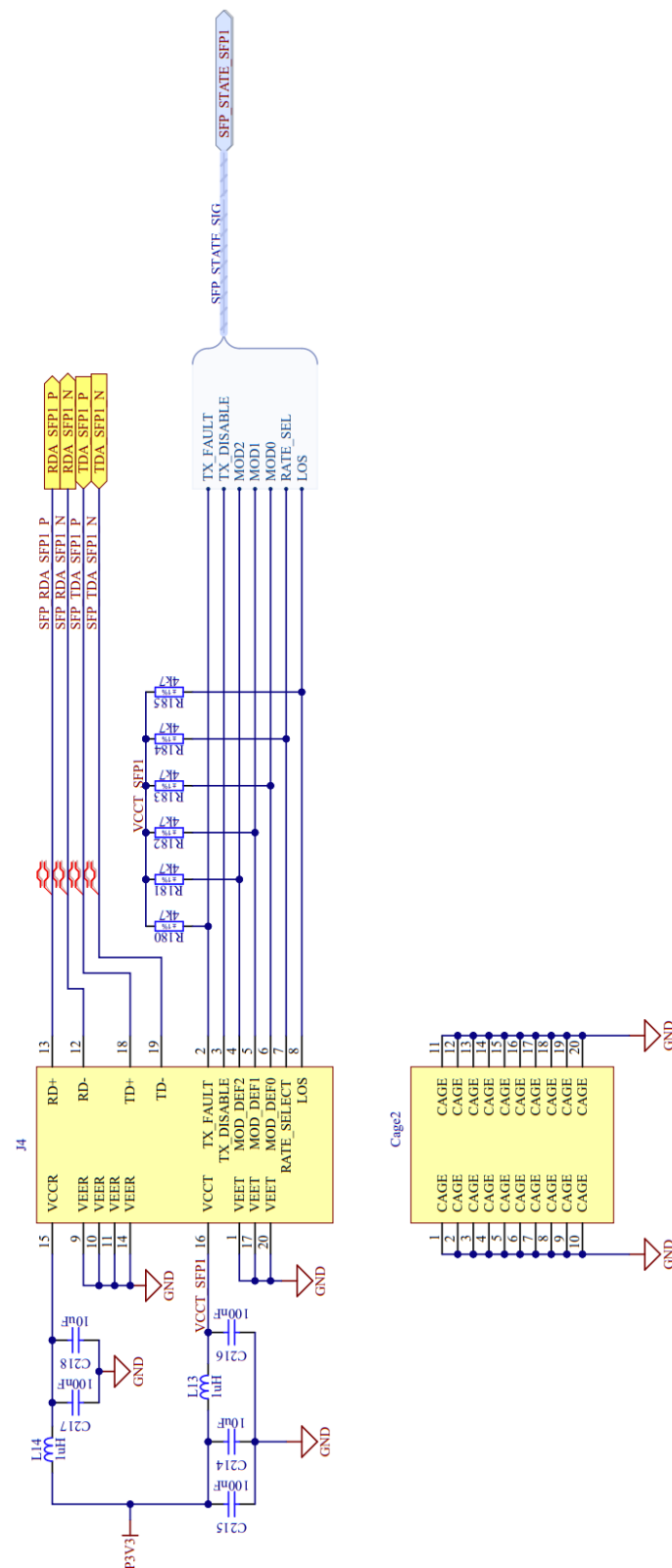


Figure 3.7: SFP cage and connector

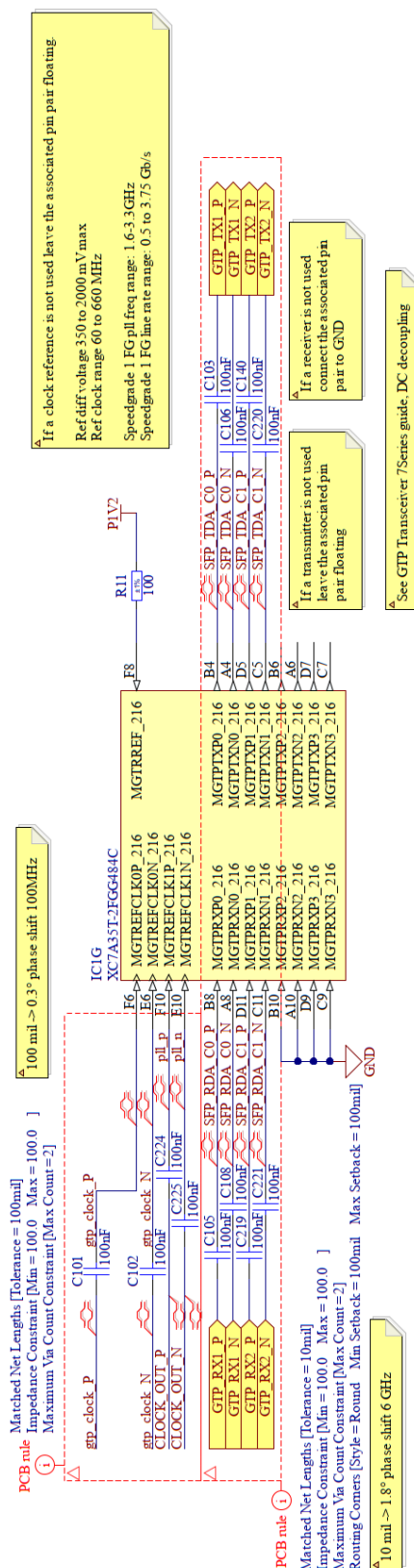


Figure 3.8: GTP transceivers schematic

3.2.8. Form factor extension (6U)

The form-factor extension enables the 3U developed card to be compatible with an extension to the 6U systems. The pins number given in table 2.6 must be respected. The 5 V power rail is not available on the 3U FGC-2 connector and must be accessed through the upper connector which is on the extension, see appendix Remote Acquisition Transceiver (RAT / BEAv2).

A connector was used in order to get those 5 V from the mechanical extension. Additionally, on the upper FGC-2 connector, a specific unique ID-chip is required on this system to identity the used card to the FGC-2 host.

3.3. PCB design

In this part, only the critical parts of the PCB design are mentioned. After the placement and design of the mechanical parts of the PCB, the routing was done with the author's supervision (PCB restrictions, dimensions, line impedance, line length, ...) by the specialised CERN Design Office in order to save time for the gateway and tests development. Indeed, components for 80 cards with additional spare parts (20) were ordered. Initially, two prototypes cards were produced before launching the series production.

The following most important routing restrictions were applied, see the next subsections.

3.3.1. Switching power supply shielding

The supply sources for the FPGA are given by the ADP5051 [18]. In fact, those are generated with two integrated and two external MOSFETs switching at a frequency defined by the resistor R_{RT} . This switching generates noise around this sub-MHz frequency and related harmonic frequencies which potentially could disturb the DCCTs precision. Due to that, the section in charge of them, in the EPC group, asked us to add a shielding which reduces the propagation of this potential sub-MHz noise up to their electronics.

An EMC-shield was chosen and placed above the power supply circuit as shown in the following figures 3.9.

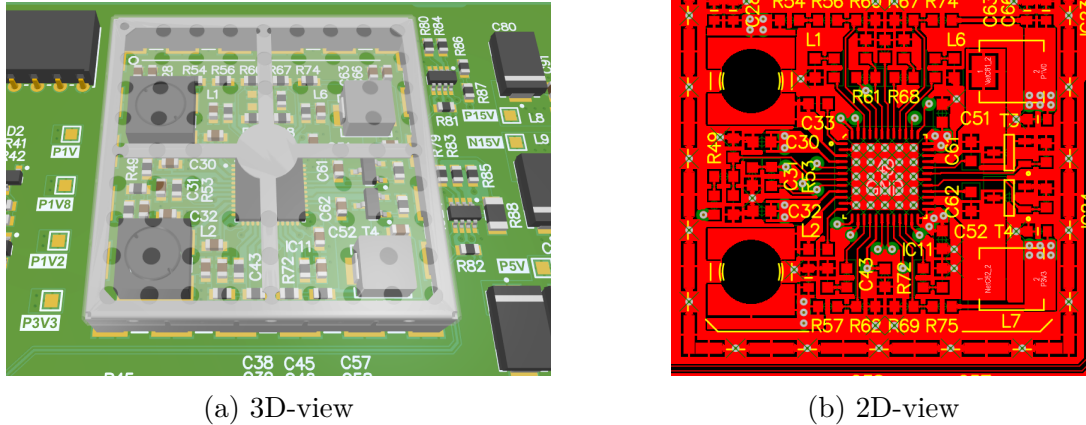


Figure 3.9: Power supply routing with the EMC shield

3.3.2. SM-differential pairs

Another critical point is the GHz part of our card for the SM differential lines between the GTP logic and the SM transmitter. The operating frequency for the transmission/reception pairs are at 1.25 GHz and 125 MHz for the clock pairs. The following points are important regarding those :

- Characteristic impedance : $100\ \Omega$ have to be respected for the differential clock

pairs, transmission and reception pairs.

- Length difference : the length difference between the lines in one pair should be as low as possible, < 10 mil or 0.254 mm for the transmission and reception pairs, < 100 mil or 2.54 mm for the clock pairs.
- Placement : the routing of those pairs should be as far as possible from the analog part as well as to the DCCT signals.

3.3.3. Analog front-end

The analog front-end requires a routing as differential pairs up to the ADC input. The lines impedance must also match $100\ \Omega$ here.

Concerning the ground, a cut between the digital ground and the analog ground of the PCB has been done and a filter added between the analog and digital supplies. This is to reduce the noise coming from the switching power supply frequencies and also the high frequency based transmitters into our analog measurements. This is shown in figure 3.10.

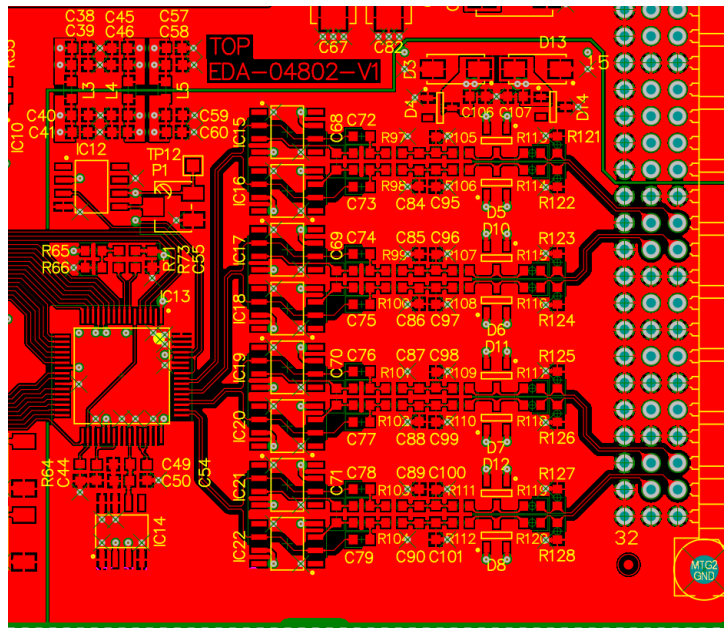


Figure 3.10: Ground plane separation

3.3.4. PCB front-panel

In addition to the PCB design, a front-panel was designed for both 3U and 6U cards. The front-panel of the 3U can be seen in figure 3.11.

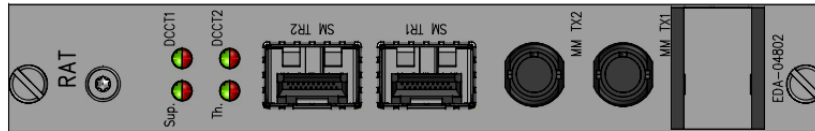


Figure 3.11: Front-panel 3U format

3.3.5. Final PCB

The final PCB is shown in figure 3.12 in the 3U format and in figure 3.13 in the 6U format.

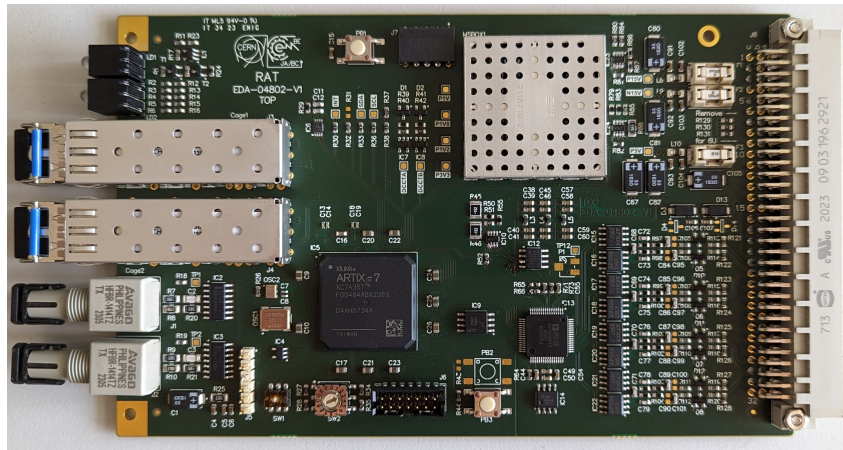


Figure 3.12: Top view picture 3U format (see 6)

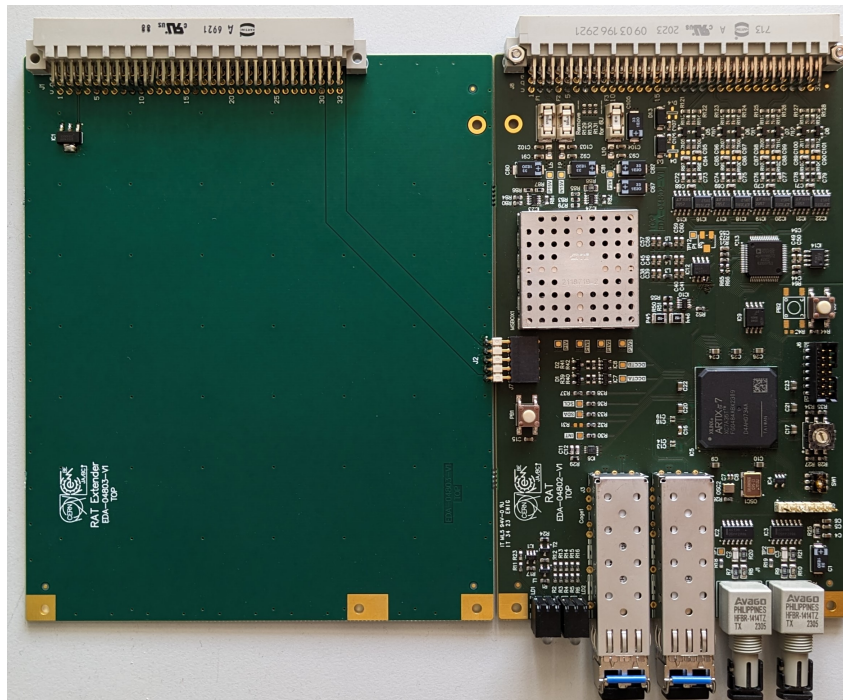


Figure 3.13: Top view picture 6U format (see 6)

3.4. Hardware testing of prototypes

After receiving both RAT first prototypes, few changes were done due to the listed errors in table 3.12.

Circuit	Error	V1.1 change
15 V supervisory	Over-voltage at 15.1 V too low	R87 changed to 75 k Ω (15.8 V now)
Supervisory circuit	SEL-pin should be open	SEL-pin open
UART	VCC-pin shortcut with external 3.3 V	VCC-pin left open on connector
10 V reference	11 k Ω resistor to ADC	Changed to 0 Ω resistor
Ref. temperature pin	connected to unused ADC ch.	Disconnected (induces ref. error)
Range SEL ADC	R66 is for the 10 to -10 V range	Mounted R66 / Not mounted R65

Table 3.12: Hardware corrections

The voltages generated by the ADP5051 regulator are correct and within the FPGA recommendation as shown in table 3.13.

FPGA part	Core and GTP (1 V)	IOs (3.3 V)	Aux (1.8 V)	GTP (1.2 V)
Recommended range	± 0.05 V and ± 0.03 V	-	± 0.09 V	± 0.03 V
Measured voltage	1.0058 V	3.279 V	1.7729 V	1.2003 V

Table 3.13: Supply voltages precision requirements and measured voltage

4 Gateware development

Having finished the hardware part, the "Gateware" which is a word initiated by CERN to mention HDL-derived logic, was developed in this part.

First, the requirements of the sequencer algorithm are described. Second, the used tools to achieve those through simulations and tests without having the hardware are presented. Finally, the gateware architecture and parts are explained in detail.

4.1. Requirements

The gateware part needs to fulfil the application specification which will be described in the next sub-section. The developed gateware must also be simulated entirely and tested as much as possible before the production deployment.

4.1.1. Application specification

Regarding the designed hardware and the project specification in section 2.4, the gateware has to fulfil the following aspects :

- ADC configuration and driver : driver of the ADC-IOs which implies the clock generation, configuration signals and conversion read steps accordingly to the datasheet.
- Calibration algorithm : two point gain and offset calibration and polynomial compensation algorithm to reach the specification precision.
- Filtering : FIR-filter to be compatible with lower frequencies applications.
- Production test communication (UART) : UART communication to read the version of the gateware, the status signals and the ADC corrected values.
- Optic fibers transmission MM and SM : framing IPs and configuration of the encoding IPs.
- Mode selection (hexadecimal selector) : mode selector package in order to enable/disable or configure the IPs through the hexadecimal switch.

A program in C++ or python script also needs to be developed in order to automate the tests after the production. The UART communication will be used to access the ADC measured values during this test and to store calibration values if necessary. The multi-mode optic fiber also needs to be tested by implementing a receiver. The single-mode will be tested in coordination with the Technology Department (TE) Machine Protection and Electrical Integrity Group (MPE) group which already has the corresponding receiver.

4.1.2. Simulation and testbenches specification

The other important point of the specification is that the gateware needs to be correctly tested through simulation testbenches. Indeed, each separate IP as well as the complete assembled gateware will be tested here. In the next sections, the used tools to fulfill this specification are described.

4.2. Used tools

The used tools for the gateware development are presented in this part. Firstly, the testbench simulation library UVVM will be presented. After this, the used simulators and last but not least, the continuous integration in the cloud with Gitlab Continuous Integration / Continuous Deployment (Gitlab CI/CD).

4.2.1. Test library: UVVM

The Universal VHDL Verification Methodology (UVVM) is a free and open source methodology and library for making very structured VHDL-based testbenches [22]. This library is fully compatible with the main VHDL simulators : ModelSim, Riviera-Pro, Questa Sim and GHDL.

It is constituted of a main utility library which contains many different procedures giving the possibility to verify the signal or bus states and changes with user defined time intervals as well as generating the simulation clocks. Additionally, the following sub-libraries of UVVM were used to test in detail the different bus and serial communications during the gateware development :

- Bitvis VIP Simple Bus Interface (SBI) : used to simulate a SBI master to test SBI-slaves
- Bitvis VIP I2C : used to simulate I2C-slave devices (EEPROM or ADP5051 supply)
- Bitvis VIP UART : used to simulate the computer side UART-communication

With the help of the UVVM-utility library as well as this sub-libraries the different entities were first separately tested before testing the IPs together.

In this work, the SBI communication was used to communicate from one IP to the other, as it is not a commonly used bus it is described shortly.

Simple Bus Interface (SBI)

The SBI is a simple bus interface which was defined in UVVM by Bitvis. It is using the following signals :

- CS : chip select line which is high when the SBI-slave is selected

- ADDR : address bus which is selecting the register to read
- WENA : write select, high when a register is written
- WDATA : write bus, used to write data to the register (width as required)
- RENA : read select, high when a register is read
- RDATA : read bus, used to read data from the register (width as required)

The signals listed are then used as presented in this timing diagram for write or read operations, figure 4.1.

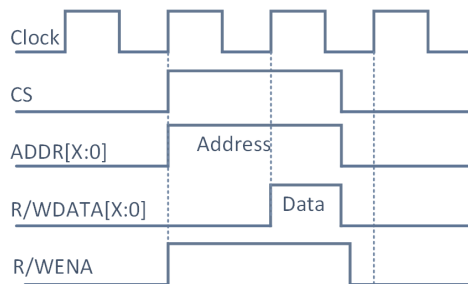


Figure 4.1: Timing diagram of SBI

As the IPs in our design are based on this bus communication, the same architecture was used for all IPs. They are composed of a "package" file which describes the SBI registers and required bus sizes. Then, two sides are developed, one is the Parameterized Intellectual Property Function (PIF)-interface which is in charge of responding to the SBI-master requests and the other is the "Core" which has the IP main state machine gateware and controls the other IP signals. Each IP was developed as shown in figure 4.2.

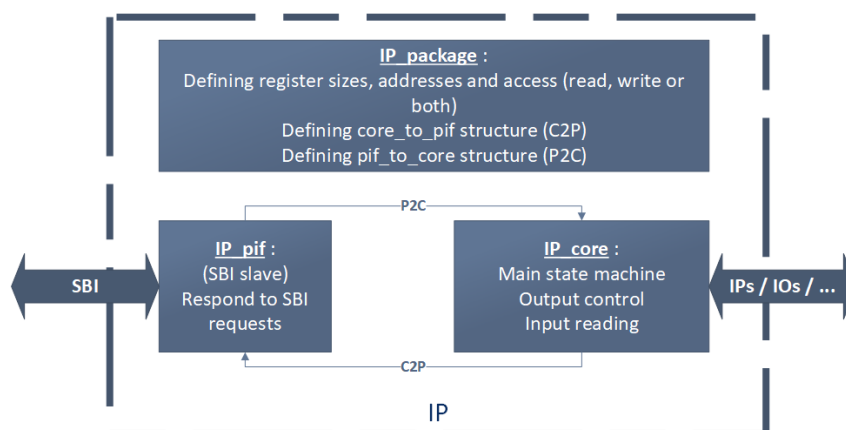


Figure 4.2: IP architecture of SBI-based IPs

The advantage of using this inter-IP communication is that the SBI test library from UVVM is fully compatible to those which simplifies the testbench development.

4.2.2. Simulator: GHDL and Modelsim

For this work, both simulator GHDL and Modelsim were used. Indeed, Modelsim was used locally to test the IPs during the development phase in pre- and post-synthesis. It was combined with Vivado and the pre-compiled UVVM libraries. One disadvantage of Modelsim is that the licence costs are high and in order to reduce the number of used licences, CERN prefers that we use GHDL or Riviera Pro which are free simulators.

GHDL was used remotely in Gitlab CI/CD in order to verify that all IPs were still passing all the testbenches after each committed change. This avoids the use of Modelsim licences in the Virtual Machine (VM).

GHDL is a free and open source simulator which enables compiling and executing VHDL. It supports for now all VHDL versions up to 2019 (partially 2008 and 2019) [23]. GHDL was not used locally with Vivado as it is not directly compatible with exported Xilinx IPs and can't do post synthesis simulations. However, it is largely sufficient for testing separate IPs of the design combined with the compatible UVVM library.

4.2.3. Automated synthesis and tests: Gitlab CI/CD

This project was developed by using the Gitlab Continuous Integration / Continuous Deployment (Gitlab CI/CD) tool. To do so, the Vivado project was exported as a TCL file in order to rebuild the project easily by just having the VHDL IP and testbench sources in the remote repository (without all configuration and temporary project files). For this, a Docker image with Vivado was used onto the VM and enables to launch a synthesis, implementation and bitstream generation at each push. The advantage of this method is that each version on Git has its own bitstream file and it is easily possible to get previous versions if any bug is encountered.

The testbenches were done with GHDL on another docker image. Here only the pre-synthesis simulations are done for the different project IPs. The waveforms are exported in order to be able to download them to verify the expected result. Figure 4.3 illustrates the used automated way of development.

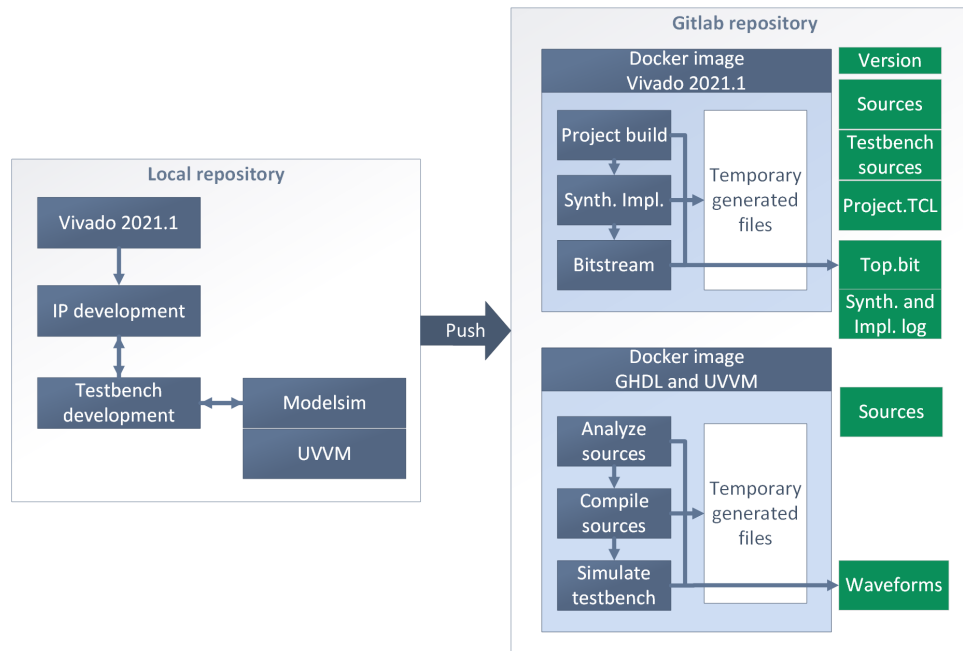


Figure 4.3: Local and remote architecture

4.3. Structure and architecture

During the gateway development, the first step was to design the whole drivers and to develop testbenches corresponding to their dedicated datasheet. Regarding our design the following drivers were required :

- Driver for the ADC (AD7609) with selection of sample frequency and oversampling
- Driver for the I2C-EEPROM
- Driver for the supply voltage (ADP5051) interrupt and reset configuration (using I2C)
- Driver for the supervisory circuits interrupts
- Driver for the UART-calibration communication
- Driver for the optic fibers

On top of those drivers, other IPs are needed to fulfil the application specification. These are the following IPs, they are required between the acquisition and the sent frame :

- Mode selection package based on the hexadecimal selector input
- Single mode encoder and framing IP
- Multi-mode encoder and framing IP
- Polynomial correction IP

- Memory interface (UART or Polynomial IP to EEPROM)
- FIR filtering IP

As explained in section 4.2.1, the SBI-architecture is adopted during the development for most of the IPs. The complete and final architecture can be seen in figure 4.4. The advantage of using this SBI-architecture is that an IP can be easily added or removed if (not) required.

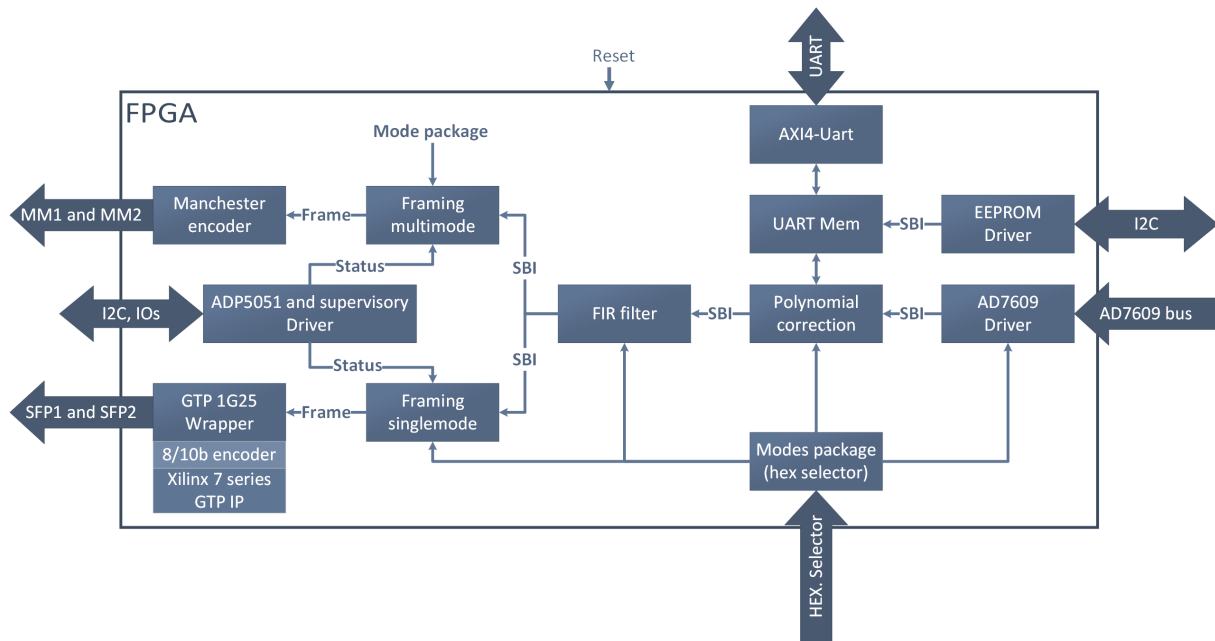


Figure 4.4: Global gateware architecture

In the next sub-sections, the different developed IPs are presented.

4.3.1. Mode selection package

The mode selection package is just composed of constant configuration arrays in order to switch easily between two configuration through the hexadecimal selector after a reset. With the hexadecimal selector up to 16 configurations are available. Indeed, as explained in the section 2.4, this card can be used for multi-purposes and that's why this different modes of operation are required.

For now, the different required modes are not completely defined but the following values can be changed, see table 4.1.

Parameter	Possible values	Description
Frequency	1 to 200 kHz	Sampling rate frequency
OVS	0 to 64	Oversampling configured on the ADC
Calibration	0 or 1	Enable or disable two point gain and offset calibration
Polynomial	0 or 1	Enable or disable polynomial correction
FIR	0 or 1	Enable or disable FIR

Table 4.1: Different possible modes of operation

4.3.2. Driver IPs and related testbenches

In this section the different drivers IP architecture and related testbenches are explained. The states machines are globally described as well with the states named as following S_NAME, with the additional mention _states for the simplified steps.

AD7609

The AD7609 driver controls the communication and conversion clock generation for the AD7609 ADC. To develop it, the datasheet requirements [16] are used. The following registers, see table 4.2, can be written (W) or read (R) through the SBI.

Register name	Structure	Description
RW-oversampling (8 bits)	P2C	Configure the oversampling
RW-frequency (8 bits)	P2C	Configure the sample rate frequency divider
RW-burst-state (1 bit)	P2C	Enable/Disable sampling
R-sample[1:8] (18 bits)	C2P	Sample values (channel 1 to 8)
R-NewSample (1 bit)	C2P	New sample available status
R-Error (2 bits)	C2P	Configuration error (oversampling/frequency)

Table 4.2: Different possible modes of operation

This registers are accessible during the configuration state after a reset. Once the configuration is done, the "burst-state" register has to be written in order to start the continuous sampling of the eight channels. The following state machine is used in the driver gateware, see figure 4.5.

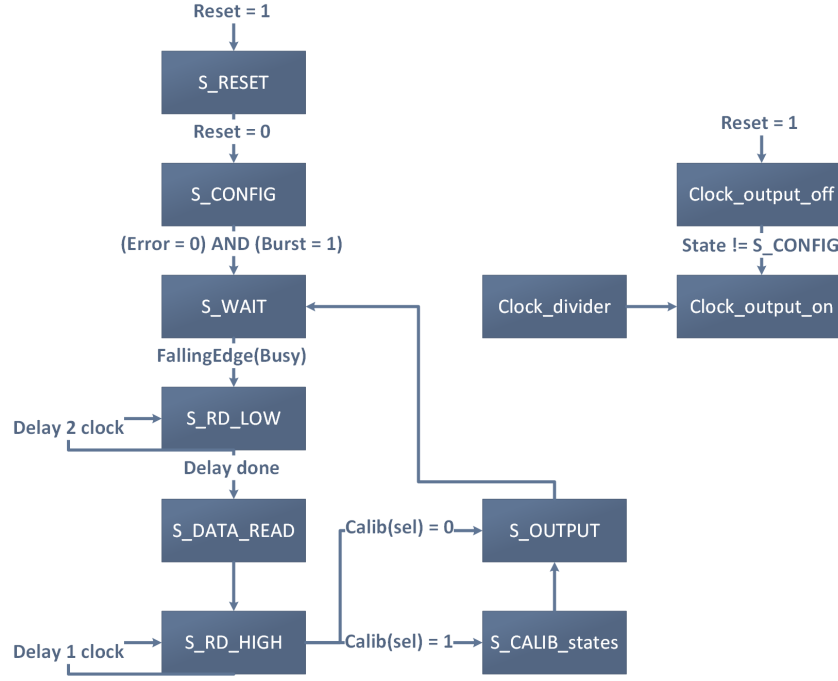


Figure 4.5: State AD7609 driver

As explained in section 4.3.1, the two point calibration can be set or not through the hexadecimal configuration selector. The used calibration algorithm is using both 10 V and -10 V channels to calculate the gain and offset voltage as following, see equation 4.1.

$$\begin{cases} G \cdot M_{P10V} + O = E_{P10V} \\ G \cdot M_{N10V} + O = E_{N10V} \end{cases} \quad (4.1)$$

$$\begin{cases} O = \frac{(M_{P10V} \cdot E_{N10V}) - (M_{N10V} \cdot E_{P10V})}{M_{P10V} - M_{N10V}} \\ G = \frac{(E_{P10V} - O)}{M_{P10V}} \end{cases}$$

In order to do this calculation with a fixed point, each resulted value is shifted by N bits (generic configurable) before the division. This gives the following resulting equation, eq. 4.2 (Bit-shift mathematically represented by 2^N).

$$\begin{cases} O = \frac{((M_{P10V} \cdot E_{N10V}) - (M_{N10V} \cdot E_{P10V})) \cdot 2^N}{M_{P10V} - M_{N10V}} \\ G = \frac{(E_{P10V} - O) \cdot 2^N}{M_{P10V}} \end{cases} \quad (4.2)$$

To estimate the required bit-shift to minimize precision losses, this calculation was first done with Excel. The error between a floating point calculation and the N-bit fixed point

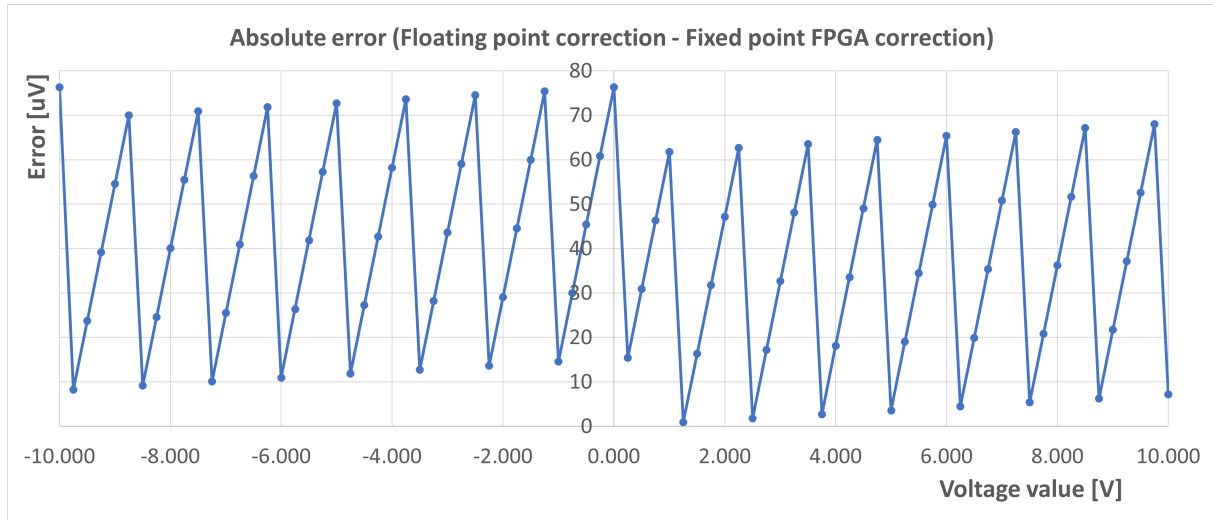


Figure 4.6: Fixed point error estimation compared to floating point

was then plotted for a simulated measured reference voltage. The precision increases with the bits. However, the number of bits is limited to 16, within the 200 kHz (max frequency of sampling) timing constrain of the FPGA sequential divider logic circuit. The error variation found with this calculation is illustrated on figure 4.6. The x-axis shows the simulated input voltage from -10 V to 10 V with the corresponding remaining error after the gain and offset compensation on the y-axis. The scale of the y-axis is represented in μV . The maximal LSB variation is then theoretically of $\pm 3 \text{ LSB}$ with an ideal 10 V and -10 V reference.

In addition to this linear correction, the polynomial correction, explained in section 4.3.3 is developed.

AD7609 testbench

Different tests were implemented for this IP. It tests the right operation of the controlled AD7609 IOs with the datasheet timing limitations, shown in table 4.4 corresponding to the diagramm 4.7. The global state machine and the registers values are tested as well. At the end, the calibration calculation timing and the output throughput rate stability was verified by injecting a simulated sinus at a 200 kHz sample rate (maximum sample rate). Table 4.3 illustrates in detail the tests.

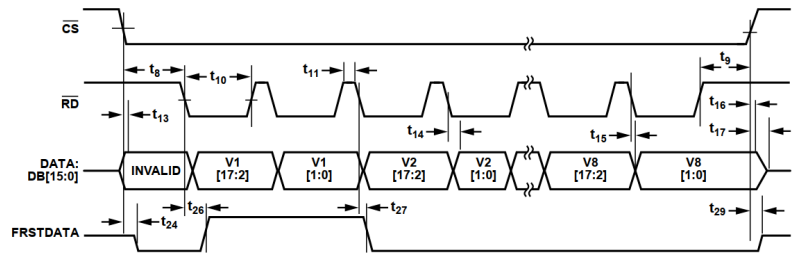
Figure 4. Parallel Mode Separate $\overline{CS}$ and $\overline{RD}$ Pulses

Figure 4.7: Conversion read operation AD7609

Test gp.	State	Nb.	Case	Expected
Init.	Reset	1.1	Reset ADC	Reset signal ADC to 1
	Config	1.2	SBI registers	Register to initial values
	Config	1.3	CONVST_A/B-clock	Stays high, no switching
	Config	1.4	CS and RD outputs	CS and RD stays high
Freq.	Config	2.1	Enable burst	Burst register is set to 1
	Sampling	2.2	Clock frequency	Verify freq./duty cyc. (200 kHz/50 %)
	Sampling	2.3	Changing freq.	Register change
	Sampling	2.4	Clock frequency	Freq./duty. cyc. to 100 kHz/50 %
	Sampling	2.5	Set burst reg. to 0	State change to config
OVS	Config	3.1	OVS to 2 (by 100 kHz)	Err. reg. to 0 and OVS-pins to "001"
	Config	3.2	OVS to 4 (by 100 kHz)	Err. reg. to 2 and OVS-pins unchanged
	Config	3.3	OVS to 3 (by 100 kHz)	Err. reg. to 1 and OVS-pins unchanged
	Config	3.4	Burst to 1 while errors	State and register unch.
	Sampling	3.5	Changing OVS	OVS register unch.
Sampling	Sampling	4.1	Simulating ADC sig.	Full read states cycle
	Sampling	4.2	Read sample value	SBI ch. values equals sim. values
	Sampling	4.3	New sample reg./int.	SBI reg. and int. goes to 1
	Sampling	4.4	Sinus of 20 Vpp	Calibrated output matching input

Table 4.3: Main tests of AD7609 IOs

Time nb. (see figure 4.7)	t8	t10	t11	t14
Min. time req. (3.3 V)	0 ns	24 ns	15 ns	24 ns

Table 4.4: Time limitations used for the AD7609 simulated component

EEPROM

The EEPROM uses a classical I2C communication. The driver uses the memory whether to read data after a reset or to store new values in the EEPROM through UART. To

determine the amount of bytes written on the last power-on cycle, a simple index is used. It is stored at the beginning of the memory.

We here have 2kbits of data followed by a fixed non-writable 48 bits ID. Figure 4.8 illustrates the architecture of our EEPROM driver.

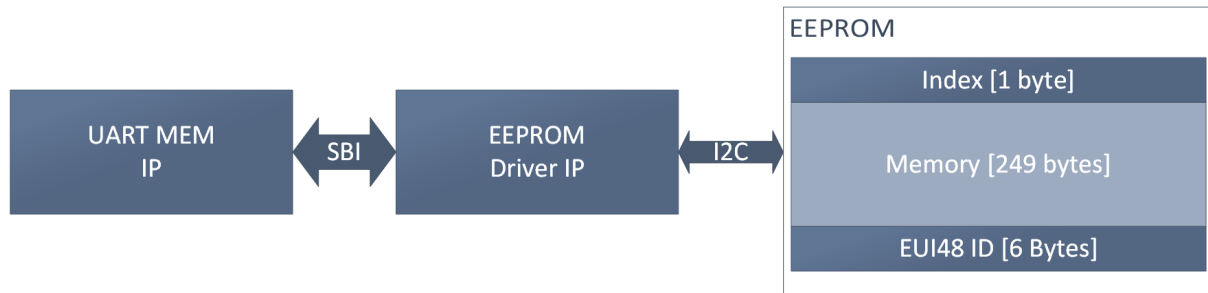


Figure 4.8: EEPROM gateware architecture

The used state machine is presented on figure 4.9. During the initialisation, the first byte of the EEPROM memory is read which contains the previous number of written bytes (if any). This is to verify if the memory is empty or not. If empty, the variable can be written through UART temporally in order to test them before doing a permanent EEPROM storage. Once the write operations are done and the coefficient are approuved, they can be saved to the EEPROM by writing the "save-register" through a given UART command (table 4.8).

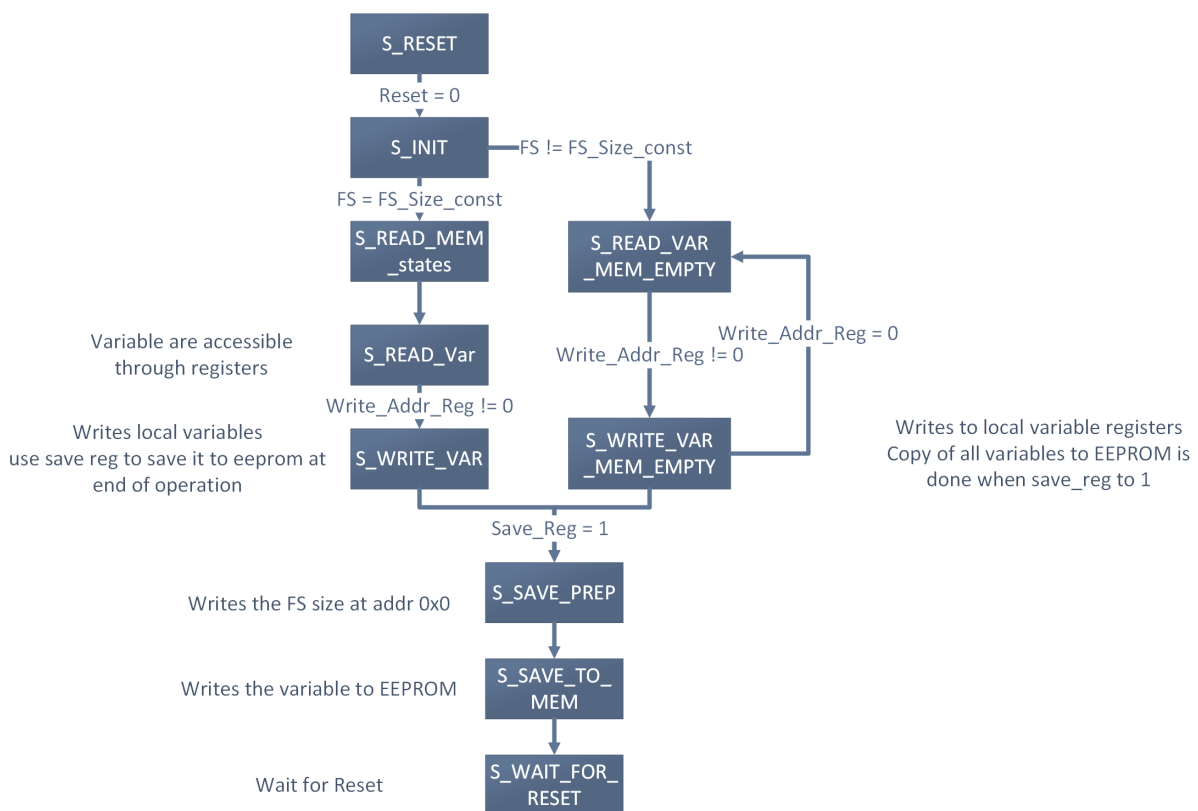


Figure 4.9: EEPROM gateware state machine

For now, twelve different variables are accessible through SBI which are 32-bits wide. The following registers are used to configure and use the EEPROM-Driver-IP, see table 4.5.

Register name	Structure	Description
W-Write-Address (8 bits)	P2C	Variable write address (1 to 8)
W-Write-value (32 bits)	P2C	Value to be written (write before address)
W-Save-Flag (1 bit)	P2C	Set to 1 to save local variable to EEPROM
R-Var-[1-12] (32 bits)	C2P	32-bits variable values
R-State (8 bits)	C2P	8-bits current state machine value

Table 4.5: Registers of the EEPROM-Driver-IP

EEPROM testbench

The EEPROM was simulated for this testbench as well with the UVVM-I2C library. The test-sequence is explained in table 4.6.

Test gp.	State	Nb.	Case	Expected
Init.	Reset	1.1	Reset	Reset state
	Init	1.2	I2C answer 0x0	State READ_VAR_EMPTY
	Init	1.3	I2C answer 0x20 and values	State READ_VAR_states
Read	Read_Var	2.1	Read variable SBI	Value answered in init.
	Write	2.2	Read_Var_Empty	SBI vars to 0
Write	Read_Var	3.1	Write addr. and values reg. SBI	Value of vars changed
	Read_Var	3.2	Write save reg. SBI	Value received in I2C

Table 4.6: Main tests of the EEPROM-IP

ADP5051

The ADP5051 [18] is the FPGA power supply which is switching the 5 V supply down to 3.3 V, 1.8 V, 1.2 V and 1.0 V. It has an I2C interface which is used to configure the interrupt output pin, the supply low voltage threshold detection, as well as the power good status pin correctly. After the configuration, the Interrupt (INT) and Power Good (PWRGD)-pins are used to monitor the status of the supply. The SBI will not be used here as no real interaction between the sequencer and the ADP driver are necessary.

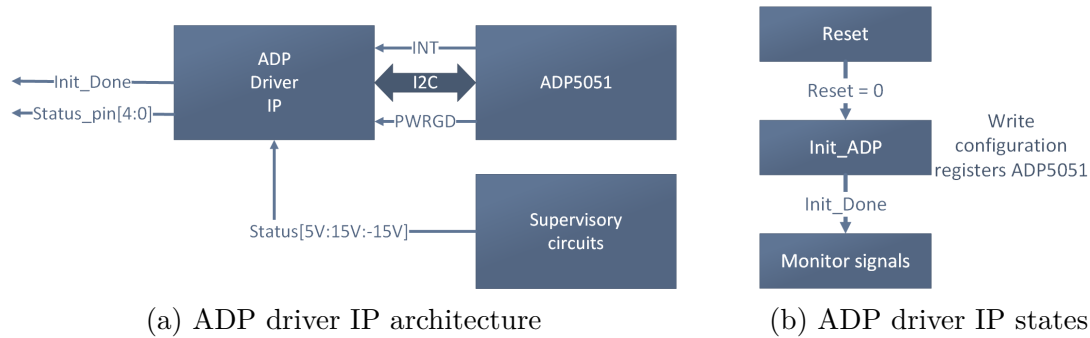


Figure 4.10: ADP5051 driver

The output signals are then used by the framing IP for the multimode and single mode transmitters. Even if a supply error is detected, the gateware should continue to operate normally and transmit the information to the BEM in order to generate an interlock if necessary.

ADP5051 testbench

The ADP5051 was simulated for this testbench with the UVVM-I2C library. The test-sequence is explained in table 4.7.

Test gp.	State	Nb.	Case	Expected
Init.	Reset	1.1	Reset	Reset state
	Init	1.2	Check if status starts low	All status low
	Init	1.3	Thresholds config.	I2C receive threshold config. frame
	Init	1.4	Power good config.	I2C receive power good config. frame
	Init	1.5	Interrupt config.	I2C receive interrupt config. frame
Run	Monitor	2.0	Interrupts ADP change	Change output status
	Monitor	2.1	Supervisory status change	Change output status

Table 4.7: Main tests of the ADP5051-IP

UART Mem IP

The UART memory IP is handling the UART requests coming from the calibration computer. It is using the AXI4-to-UART IP from Xilinx which enables to transmit and receive UART frames. The following UART requests can be handled by the IP, see table 4.8.

Request code	Request description
0xAA	Open UART communication has to be sent before using any command
0xBB	Set the 8 variables for the calibration IP
0x66	Save the 8 variables to EEPROM
0xCC	Get the 8 channels ADC values for the next sample
0xDD	Get the ADP and DCCT status bits
0xEE	Get the version of the gateware hardcoded in this IP

Table 4.8: Possible host side UART requests

The UART-mem IP state machine is described by the following state machine see figure 4.11.

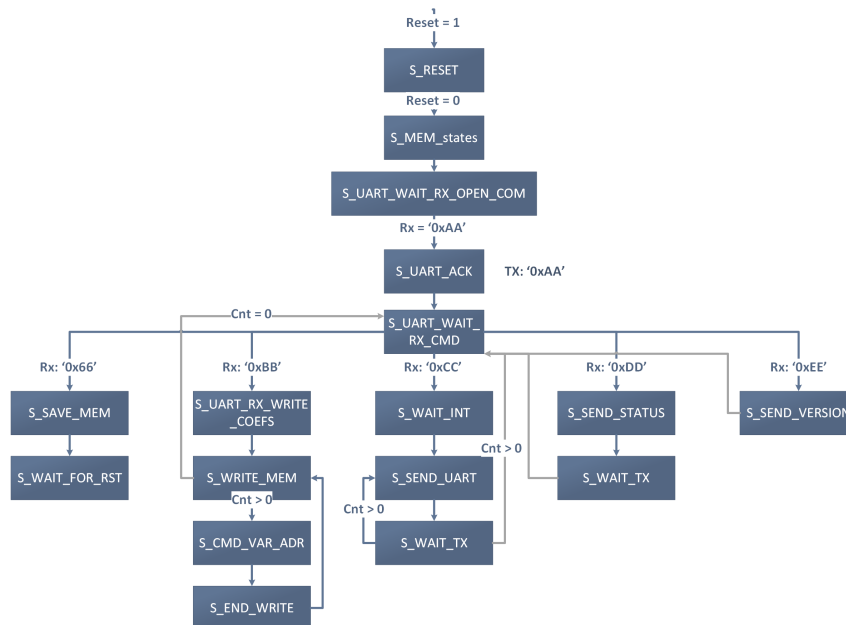


Figure 4.11: UART-Mem-IP state machine

UART testbench

The following shown testbench was realized for the UART-IP, table 4.9.

Test gp.	State	Nb.	Case	Expected
Init.	Reset	1.1	Reset	Reset state
Command	WAIT_OPEN_COM	2.1	Transmit "0xAA"	Receiving ACK "0xAA"
	WAIT_RX_CMD	2.1	TX "0xBB"+coefs	SBI coefs are correct
	WAIT_RX_CMD	2.2	TX "0x66"	Value are received in EEPROM
	WAIT_RX_CMD	2.3	TX "0xCC"	RX correct ch. values
	WAIT_RX_CMD	2.4	TX "0xDD"	RX correct status
	WAIT_RX_CMD	2.5	TX "0xEE"	RX correct version

Table 4.9: Main tests of the UART-IP

4.3.3. Digital signal processing IPs

Two different digital signal processing IPs are here. The first one is the polynomial correction IP which role is to compensate the additional ADC-errors. Then, a FIR-filter is used to have the possibility to digitally filter the signal for lower frequency applications.

Polynomial correction

Due to limited precision instruments and required memory (589.824 Bytes) no look-up table is used for this part. For the best accuracy, a precise 18 bits or 20 bits DAC would be required with a high precision multimeter.

Here, a polynomial calibration IP was developed by using the EEPROM memory. For this method which should improve slightly the accuracy, multiple solutions are presented in different papers. The first paper [24] explains different methods to estimate the non-linearity errors. Indeed, the approximation of the non-linearity errors was first calculated through a third degree polynomial function, then through a random function and finally with a combined method of the random and polynomial functions. The second paper [25] explains the random function based ADC non-linearity approximation most precisely.

In the present work, the third degree polynomial function error approximation method is used. The coefficients of this approximation can be stored and modified in the EEPROM memory. To calculate them, the following equations of [24] are used, equations 4.3.

$$\left(A_0 = 0 \quad A_1 = \frac{q \cdot x_n^2 \cdot INL}{(x_n^2 - x_L^2) \cdot x_L} \quad A_2 = 0 \quad A_3 = \frac{-q \cdot INL}{(x_n^2 - x_L^2) \cdot x_L} \right) \quad (4.3)$$

$$\rho = A_1 + 1.5 \cdot A_3 \cdot X_{sample}$$

In equation 4.3, A_i represents the coefficient of the third degree polynomial calculation, q the LSB of the ADC, INL the maximal integral non linearity of the ADC, x_L the input value where this maximal non-linearity is measured, and x_n the nominal full-scale

voltage of the ADC. This calculation is done in the polynomial correction IP using the state machine shown in figure 4.12.

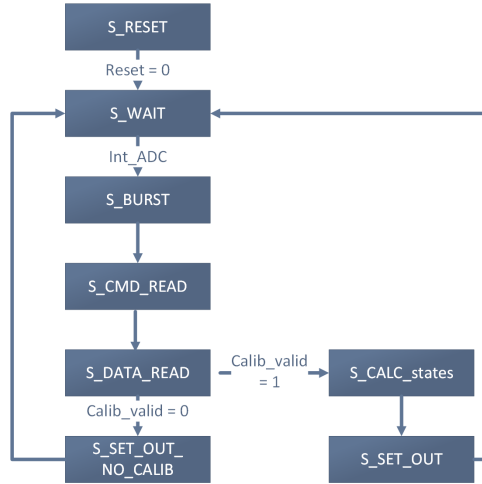


Figure 4.12: Polynomial correction state machine

After receiving the hardware and doing the error measurements, the best polynomial error correction was found by calculating the coefficients with the "polyfit" function from numpy-python (see [26]). It uses a curve fitting algorithm finding the required N-th coefficients (A_i) from the equation 4.4. Those coefficients are calculated and saved during the automated production setup, see section 5.3.

The second degree polynomial function is then used on the FPGA, see results in section 5.1.

$$poly(x, N) = \sum_{i=0}^{N-1} A_i \cdot x^i \quad (4.4)$$

$$E_x = M_{reference} \approx poly(M_{sample}, 2)$$

For this polynomial calculation, three 32-bits coefficients per channel are used. Fixed point values are used for this calculation and the coefficient must be given with the format 16.16 bits for the offset (A_0), 2.30 bits for the A_1 coefficient and 0.32 bits for the A_2 coefficient.

Polynomial correction testbench

For this IP, the top-IP of the polynomial correction was used which instantiates the following parts :

- AD7609-IP
- EEPROM-IP
- UART-IP

Then, each IP-function mentioned in the previous subsections are verified. The polynomial correction calculation was not tested in this testbench. The calculation steps were just verified in the Modelsim waveforms.

FIR filter

In order to use the card for lower frequencies without having higher frequency noise, a FIR filter is added between the polynomial correction and the optic fiber IP. Xilinx's FIR-filter is chosen, since it's coefficients and it's frequency response can be changed easily. This IP is communicating through an AXI-4-bus which is controlled by the implemented FIR-IP used with SBI. The architecture and state machine is described in figure 4.13. The FIR filter can be enabled or disabled through the hexadecimal selector selection table described in table 4.1.

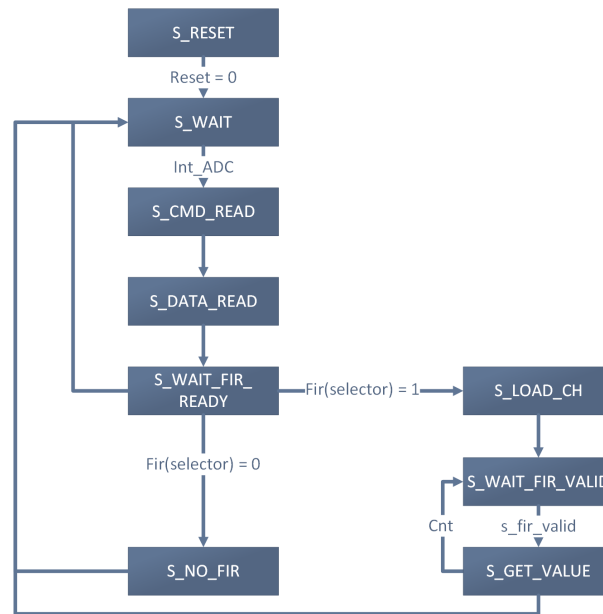


Figure 4.13: FIR states

FIR filter testbench

The FIR functions were verified through an impulse response test by replacing the ADC-SBI-values by an impulse to its max value.

4.3.4. Data transmission IPs

In this section, the data transmission IPs (encoding and framing) were developed/adjusted for the singlemode and multimode fiber optic.

Framing multimode/ singlemode

The optic fiber framing multimode IP has to convert the ADC 4-channel values as well as the status signals and interrupts into a given frame. Then this frame needs to be serialized by the manchester encoder IP (multimode) or by the singlemode GTP-wrapper. The frame used is described in table 4.10.

Mode	RFS	DCCT-status	Sup.Stat	RFS	Calib.Stat.	Channels[1:4]	CRC
(4 bits)	(2 bits)	(2 bits)	(5 bits)	(2 bits)	(1 bit)	(9 bytes)	(2 bytes)

Table 4.10: Frame payload architecture

As shown in the above table 4.10, the first byte is composed of the hexadecimal selector mode followed by the non-inverted DCCT-status signals (separated by a Reserved for futur use (RFS) unused bits). After, the supply status bits from the ADP5051 IP (see 4.3.2) are sent with the calibration status bit (1 if the polynomial correction IP is used). At the end of the frame, the four different calibrated channels are sent with a two bytes Cyclic Redundancy Check (CRC) to ensure that the payload is received correct.

In addition to this payload, a preamble and end symbol is sent by the manchester encoder with a length of 7.5 bits. Finally, the required carrier frequency to reach the maximum 200 kHz of the ADC or the normal operation of 100 kHz is described in table 4.11.

Requirements	200 kHz sampling rate	100 kHz sampling rate
Data-transmission rate	$\frac{14 \text{ bytes}}{5 \mu\text{s}} = 22.4 \text{ Mbit/s}$	$\frac{14 \text{ bytes}}{10 \mu\text{s}} = 11.2 \text{ Mbit/s}$
Carrier frequency	44.8 MHz	22.4 MHz
Receiver clock freq.	$\geq 179.2 \text{ MHz}$	$\geq 89.6 \text{ MHz}$

Table 4.11: Multimode optic fiber requirements

For the singlemode optic fiber, a start and end sequence of 2 bytes each are sent in addition to the payload (in table 4.10) at a data-rate of 1.25 Gbit/s. Due to the configuration, control and different output-rates of both transmitters types two different framing IP are used here.

Manchester encoder

The multimode optic fiber is used by CERN with the manchester encoding scheme and is standardized. The IP was not developed in this work. This encoding scheme uses the rising or falling edge transitions to encode the frame data. A low to high transition corresponds to a '0' and high to low to a '1'. The figure 4.14 describes the two different manchester codes (here G. E. Thomas).

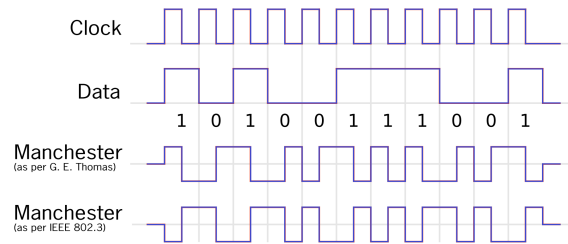


Figure 4.14: Manchester encoding scheme [3]

The major disadvantage of this encoding type that the coding rate is only half of the non-coded signal.

Manchester encoder testbench

The manchester encoder was tested as illustrated in table 4.12. To do so, a manchester decoder IP as well as a frame decoder were instantiated in the testbench to decode the frame.

Test gp.	State	Nb.	Case	Expected
Init.	Reset	1.1	Reset	Reset state
Transmit	-	2.1	Int. new sample	Frame is sended
	-	2.2	Frame received	Valid_decode is high
	-	2.3	Frame correct	Received frame data is correct

Table 4.12: Main tests of the frame and Manchester-IP

GTP 8b/10b encoder

The GTP transceivers on the Artix-7 are used for the single-mode data-link as explained in section 3.2.7. The IPs required for it are also given by Xilinx with an 8bit/10bit encoder. The datarate was fixed to 1.25 Gbit/s in order to be compatible with other already existing systems using such data-links.

The 8 data bits are here transmitted as an 10 bits symbol. To do so, the five first bits are converted to a 6 bits symbols and the 3 others to a 4 bits symbol. These conversions enables to have a DC-free signal and was defined by IBM, see [27]. The disadvantage is that this encoding scheme and datarate requires a high phase and frequency precision. The GTP hardware which includes a Phase-Locked Loop (PLL), enables to stay with a precise modulation carrier frequency.

As the GTP-transceiver uses its own clock (125 MHz), a First In First Out buffer (FIFO) was used between the GTP side and the framing part to reduce the timing issues due to the interclock pathes between those two clock domains logic (see section 4.3.5). The architecture is described in figure 4.15.

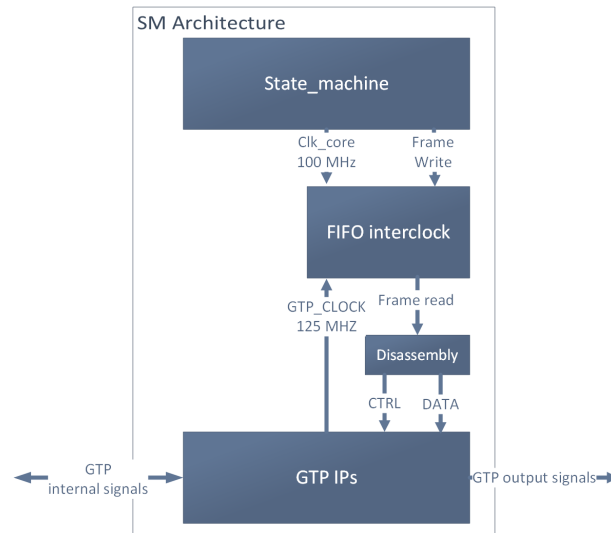


Figure 4.15: SM architecture

GTP 8b/10b encoder testbench

The GTP testbench was already implemented by Xilinx, the waveform was just verified in order to be sure that the expected frame is sended.

4.3.5. Encountered problems

Synthesis warning : "Inferring latch"

During the gateway development a main problem was encountered after the synthesis. In fact, many state machines outputs, signals and variables were synthesised as latches. This was due to the separated process architecture between the state transitions and the output changes **by not defining the output values for each state value**. The advantage of changing the output in process which is dependent on the state transitions is that the delay between the state and output transition is null.

Solutions : "Inferring latch"

Multiple solutions are possible, the first one is to group both processes together which shifts the outputs changes from one clock cycle. It then requires to change slightly your logic if you are reading input signals dependent on this output.

Another solution is to define a default value for this variable/signal or output in order to fill the non-used states values.

Timing summary : "Setup time constraints are not met"

After synthesising/implementing the design in Vivado, it is possible to have a "timing report summary". This reports enables to see if any signal logic path is slower than the

required time. In this case, the logic has to be changed or adapted.

Solution : timing summary

The solutions to resolve the timing summary issues depends on the encountered issue. Two issues were found, the first one was induced through a too long sequential 20 bits-fixed point division for the calibration which was not finished in the given available time. This was corrected by lowering the 20-bits to 16-bits fixed point which was enough for this calculation.

The second one was generated because of the "intra-clock paths" between the GTP domain and core logic domain. This happens when signals are used in two different clock domains which invite problems with metastability. It means that in some conditions the signal can be seen not as a '0' and not as a '1' generating faulty unpredictable behaviors. To avoid this, a synchronising circuit needs to be implemented by using at least two or three D-flipflops per bit between both clock domains. An asynchronous FIFO should be used for larger data exchanges (see [28]). This last solution was applied for the frame transmission from the core logic to the GTP-logic as shown in figure 4.15.

4.3.6. Used FPGA resources

Once the final gateware was developed, synthesised and validated on the RAT hardware, the percentage of resource usage on the used Artix 7 FPGA was measured with Vivado. The result compared to the available resources is shown in table 4.13.

	Available	Used	Percentage
LUT	20800	4923	23.7%
FF	41600	4861	11.7%
DSP	90	41	46%
GTP Transceiver	4	2	50%
GTP Receiver	4	2	50%
User IOs	250	68	27.2%

Table 4.13: Artix-7 A35T-FGG484 gateware used resources

5 Tests and measurements

In this chapter, ADC measurements of the BEA and RAT-card (BEAv2) are done. The accuracy and performance of both systems are then compared. Second, the data-links are tested in order to verify the good functioning of both single- and multi-mode optic fiber. Finally, the automated tests and calibration for the production are implemented.

5.1. ADC precision measurement and calibration

Once the RAT-card (or BEAv2) was received, the ADC-precision could be measured with the following setup, figure 5.1.

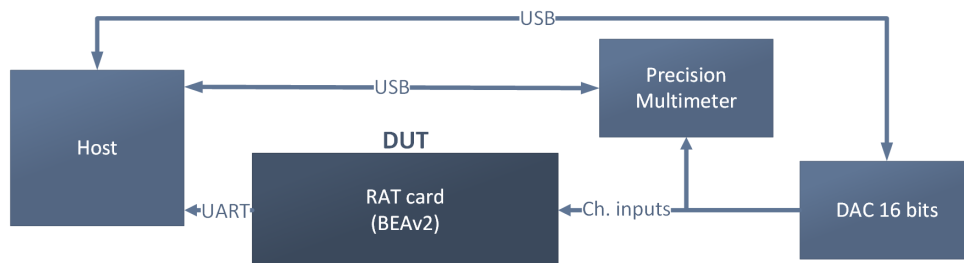


Figure 5.1: ADC precision measurements

The best way would be to use an 18 bits stable DAC with the same full-range as our ADC. Here, a 16 bits DAC with a full-scale range going from -12 to 12 V and programmable 1 mV steps from the "Keysight 34907A" module was used. A precise multimeter (5.5 digits) was used as the reference value, here the "RSDM 3055A".

The first step was to measure the ADC-error without any correction, this can be seen in figure 5.2.

The accuracy is linearly drifting to up to 10 mV. This could be derived from the LM-4140ACM reference of the AD7609 which was measured at 2.4984 mV. As the internal 10 V reference is generated with this voltage the total error should be of approximately 6.4 mV (4-gain) for a 10 V input voltage.

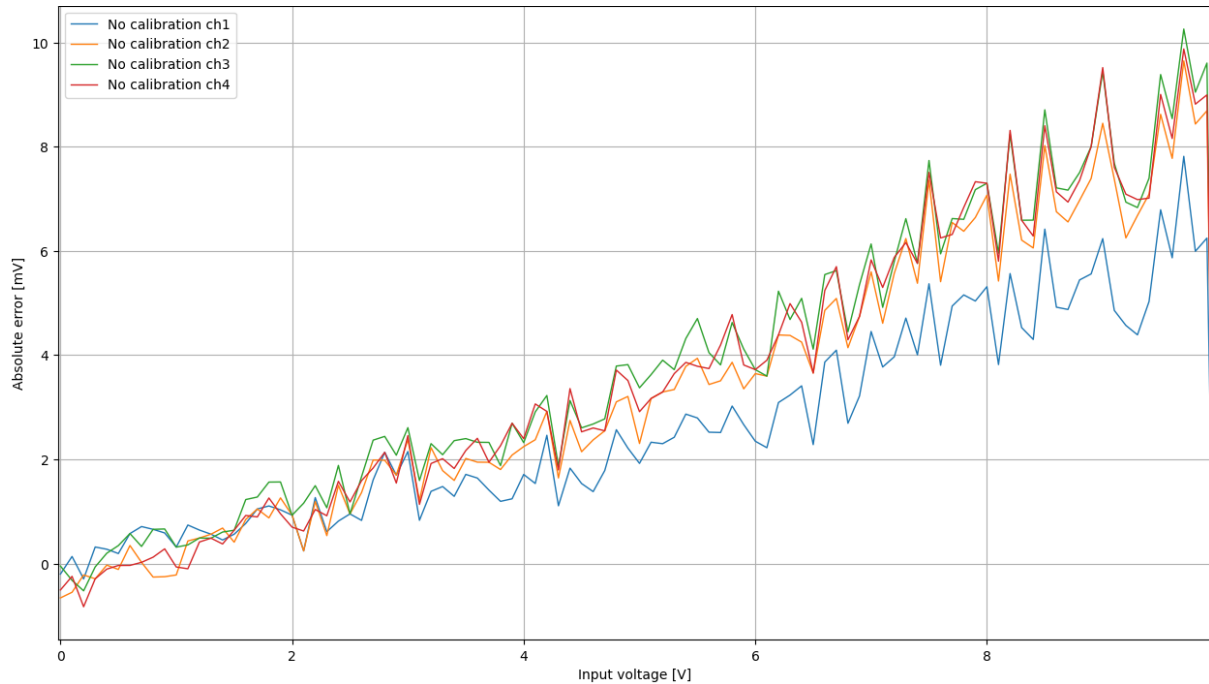


Figure 5.2: ADC errors without corrections

Then, the two point gain and offset calibration is realized. The accuracy of the four channels is shown in the figure 5.3. Here, we see that we are within 8.5 mV of accuracy for the full-range which don't reduces the linear error as much as expected. This is also due to the ADC-reference voltage which is lower than 2.5 V which means that the ADC reaches the maximal code of 10 V before the real 10 V voltage and saturates. Due to this, the gain and offset calculation result is incorrect. This problem was resolved in the precedent BEA design by using a potentiometer to trim the reference voltage.

The possible solutions to resolve this problem are following :

- Using another reference which has a better accuracy (difficult to find or very expensive)
- Trimming the reference with a potentiometer (Disadvantage for large quantities of production)
- Using the polynomial calibration (see next results)

After applying a second order polynomial correction on top of the two point gain and offset calibration, the errors were reduced, but noise is remaining, see figure 5.4. The accuracy is then of $\pm 500 \mu\text{V}$ until an input of 4 V and increases significantly to $\pm 1.4 \text{ mV}$ for an input voltage higher than 4 V (see figure 5.4).



Figure 5.3: ADC errors without the polynomial correction

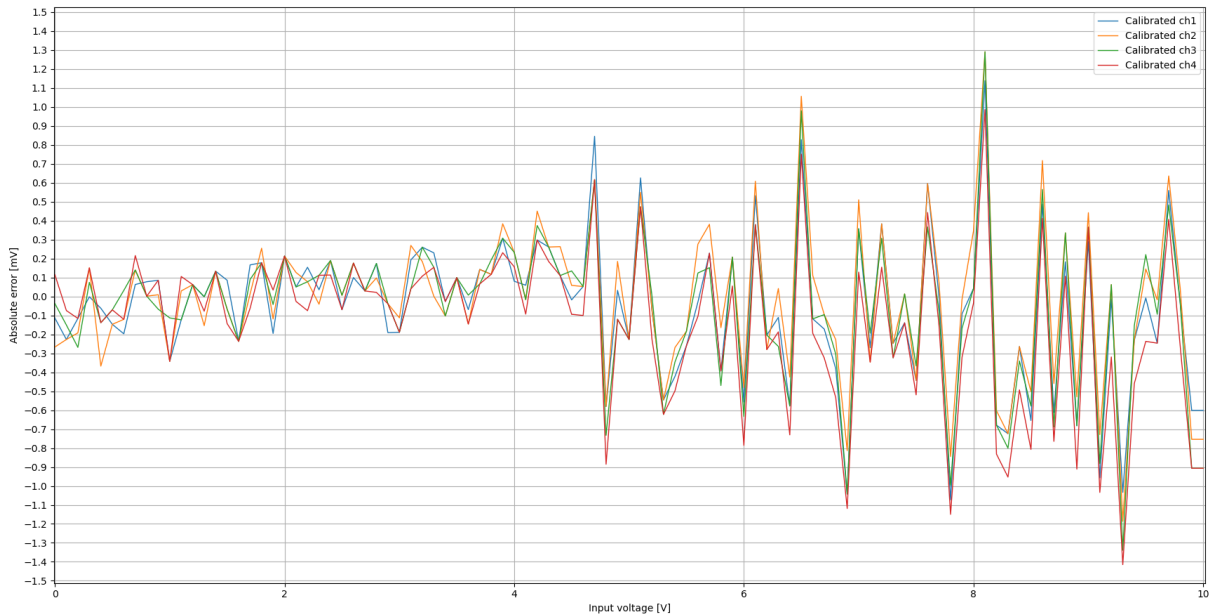


Figure 5.4: ADC errors with the polynomial correction

For the LBDS specific use-case which requires the best accuracy, the sampling rate can be reduced and the oversampling increased from 2 to 8. By configuring a lower sample rate (25 KHz) with an oversampling of 8, the noise is reduced on the absolute error curve as showed in figure 5.5 and 5.6. Indeed the accuracy of $\pm 400 \mu\text{V}$ ($\pm 5 \text{ LSB}$) is reached which is largely sufficient for this use-case.

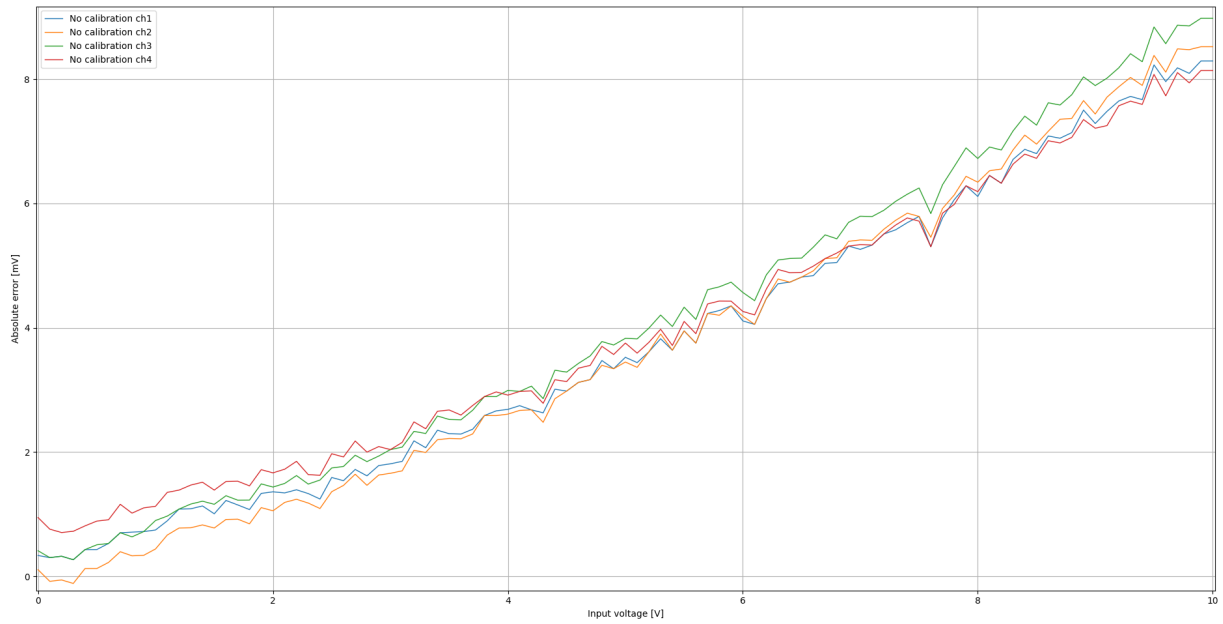


Figure 5.5: ADC errors with an oversampling of 8 without the polynomial calibration

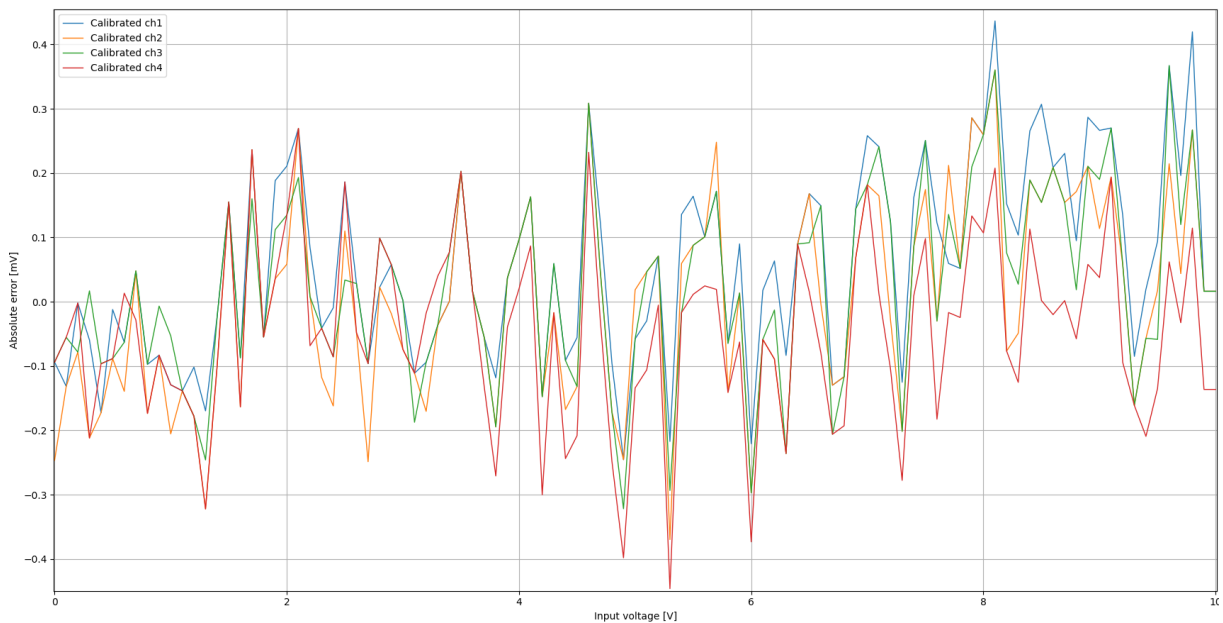


Figure 5.6: ADC errors with an oversampling of 8 with the polynomial calibration

In order to have a comparison point, previous measurements of the precision of a hardware calibrated BEAv1 card were used. This precision is shown in figure 5.7.

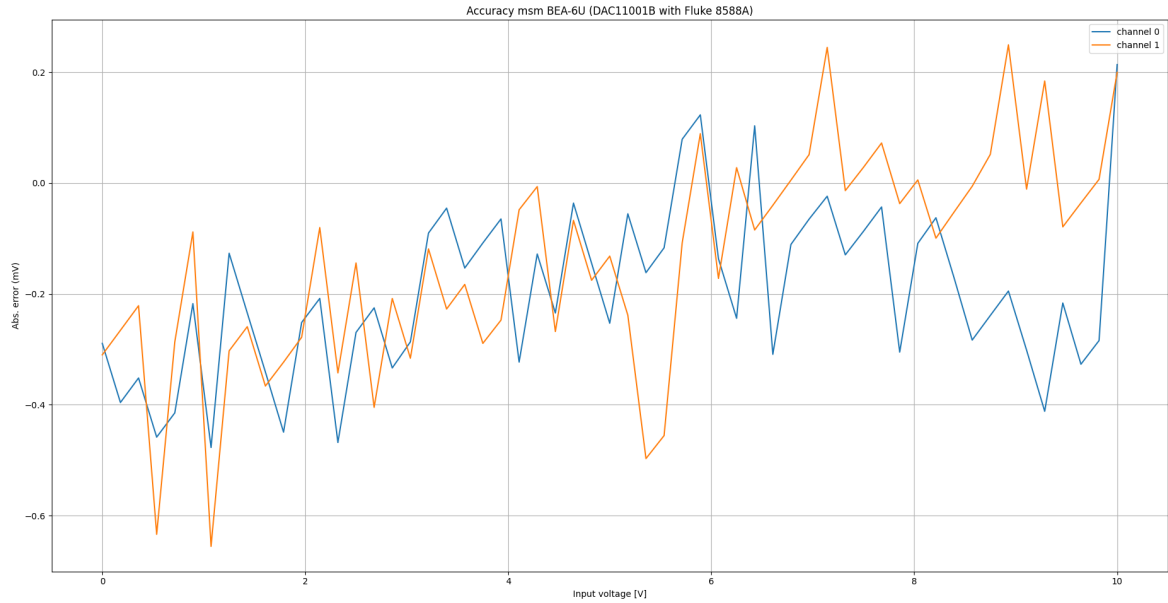


Figure 5.7: ADC errors of the BEAv1 card

Note : the measurements of the BEA accuracy were not done with the same setup as the one used for the RAT. This measurement was done at a fixed 23°C temperature with the "Fluke 8588A" multimeter and a precise 20 bits DAC "DAC11003B". This more reliable setup was not available at the end of this project for the RAT measurements.

The BEAv1 card has a non-symmetric error variation going from -0.6 mV up to 0.2 mV which corresponds to the symmetric $\pm 0.4\text{ mV}$ of figure 5.6.

To summarize, the second order polynomial calibration method works fine and increases highly the precision of the RAT in order to be within the required tolerance. The measured accuracy after and before calibration for both of this operation modes and the BEA are shown in table 5.1.

Card	SR (kHz)	OVS	Calibration	Absolute error (ppm)
BEA	4	-	Reference potentiometer	+20 to -60
RAT	25	8	Second order polynom	± 40
RAT	100	2	Second order polynom	± 140

Table 5.1: Comparison of RAT and BEA characteristics

As shown in table 5.1, the RAT reaches the same precision as the BEA at a reduced sample rate of 25 kHz. If this card is used at higher sampling rates, here 100 kHz, the absolute error increases by $\pm 100\text{ ppm}$. The main advantage of the RAT is that the calibration can be done automatically without any hardware adjustment (potentiometer).

The absolute error in (ppm) in table 5.1 is calculated with the following equation 5.1 with

E the error in Volt and FR the full-range in Volt.

$$E_{ppm} = \frac{E}{FR} \cdot 10^6 \quad (5.1)$$

Compared to the estimated RSS-error accuracy for a calibrated and non calibrated AD7609 in table 3.2, the reached accuracy is close to the estimated one. The theoretical and practical accuracy results are summarized in table 5.2.

Theoretical non calibrated accuracy	9.7 mV
Non calibrated accuracy (100 kHz)	10 mV
Theoretical calibrated accuracy	1.1 mV
Two point calibration accuracy (100 kHz)	8.5 mV
Polynomial calibration accuracy (100 kHz)	3 mV
Polynomial calibration accuracy (25 kHz)	800 μ V

Table 5.2: Calibration results compared to theoretical values

The final polynomial calibrated accuracy value is close and even better than the estimated theoretical calibration value. However, the two point gain and offset calibration technique does not decrease highly the non-calibrated theoretical accuracy. As explained before the cause is coming from the ADC-reference accuracy moving the saturation point of it. However, the channel independent polynomial calibration mostly resolves this issue.

5.2. Data-link test

In this section both optic fiber data-links are tested with the new RAT (or BEAv2).

5.2.1. Multimode optic fiber

The multi-mode optic fiber was tested before having the new card due to production delays. Indeed, the PYNC-Z2 from Xilinx (see [29]) was used (present and unused in the laboratory) with the same clock frequency of 100 MHz to test the transmissions IPs of the new implemented multi-mode data-link. For the optic fiber part, an evaluation board from Avago (see [30]) with the same transmitter used on the RAT-schematic (HFBR1414 [11]) and a receiver (AFBR2418 [31]) is utilized.

The architecture used is described in figure 5.8.

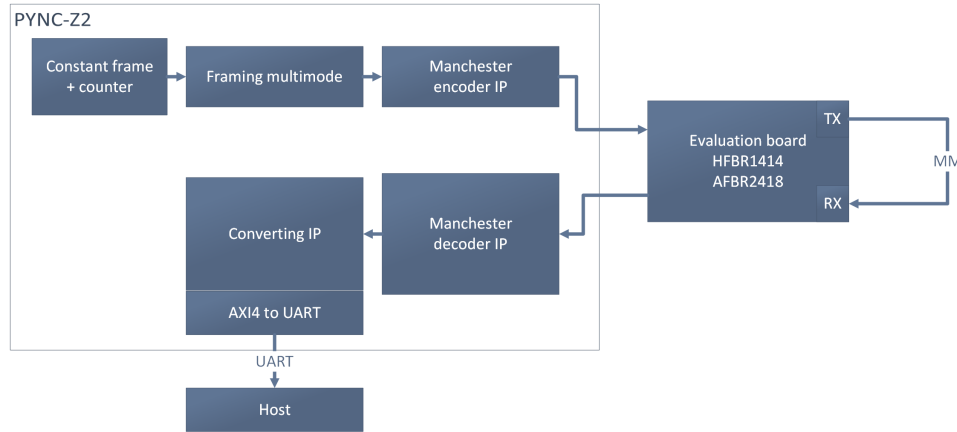


Figure 5.8: Block diagram multimode datalink tests

As described in section 4.3.4, the frame has a payload length of 11 bytes with an additional 2 bytes CRC. In table 4.11, we have seen that a bitrate of 12 MBit/s is required. In this test, a constant frame of 10 bytes with a one byte counter was sent with the maximum throughput. On the receiver side, the frame is decoded. If a frame counter value is missing the receiver error counter is incremented by one. The current received frame and error counter are accessible through UART.

This test has shown that the transmitter and receiver can operate without any issue at this data-rate.

Once the RAT was received, the same hardware was used to simulate the BEM and to check if the received frame is valid and to validate both transmitter circuits. Figure 5.9 illustrates the used hardware.

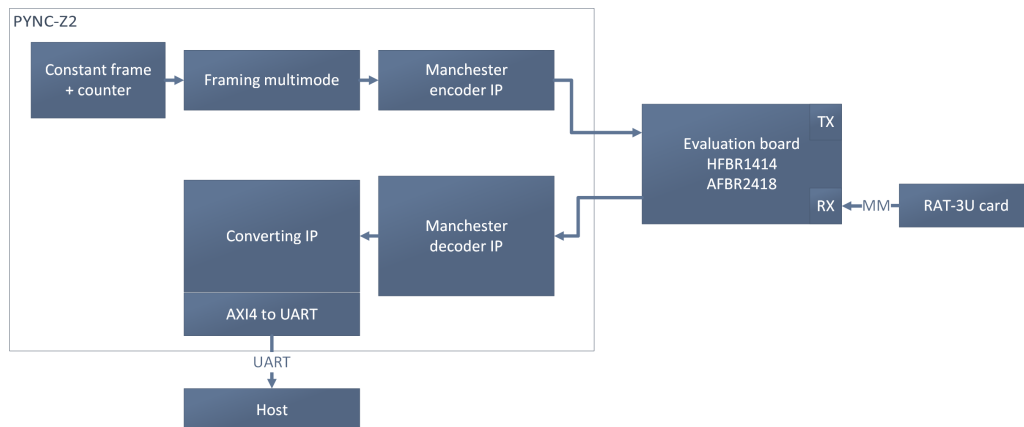


Figure 5.9: Block diagram multimode tests RAT

5.2.2. Singlemode optic fiber

The singlemode optic fiber was tested at the Technology Department (TE)-Machine Protection and Electrical Integrity Group (MPE) which is already using singlemode receivers

with the same characteristics. The frame was adapted to be compatible with their system. The singlemode frames were successfully received (tested during a 30 min slot) at the maximum 200 kHz-ADC frame rate on their receiver side and the hardware as well as the gateway validated.

5.3. Production automated tests

In order to test automatically the 80-production cards a python script was developed in combination with different instrumentation tools. The global hardware test environment is shown in figure 5.10.

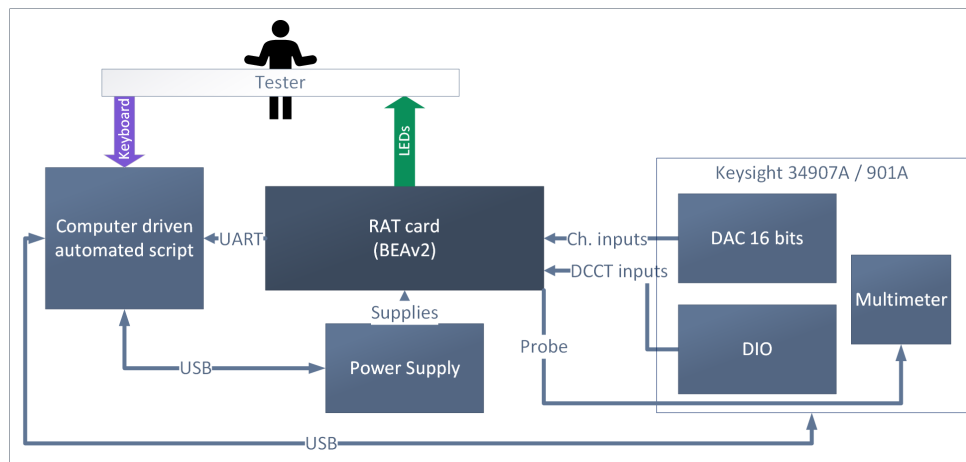


Figure 5.10: Automated production test environment

For the power supply a "Rhode & Schwarz NGE100" was used with a USB-VISA communication. This enables to automatically set the 5 V, 15 V and -15 V supply voltages, measure the consumption and test the supervisory circuits.

For testing the ADC and the DCCT, the "Keysight 34907A" and "Keysight 34901A" modules were used also with a USB-VISA communication. The 34907A module embedded a 16 bits DAC which is used to generate any voltage (with 1 mV steps) for the analog inputs. It also features a digital input output port (DIO) which is connected to the DCCT-inputs. The 34901A module is used as a multimeter to verify the different on board voltages.

As explained before, a python-script controls the described devices in order to do the following test-sequence, see table 5.3.

Test nb.	Test desc.	Actor	Sensor
1	Power supplies correct	Tester with measurement probe	KS34901A
2	LED green/red	LEDs	Tester
3	Status OK	UART read status	all 0
4	Supervisory circuits 15 V	15 V step-wise in-/decrease	UART read status
5	Supervisory circuits -15 V	-15 V step-wise in-/decrease	UART read status
6	Supervisory circuits 5 V	5 V step-wise in-/decrease	UART read status
7	DCCT inputs	0 then 1 input	UART read status
8	DCCT inputs	0 then 1 input	Tester with LEDs
9	ADC conversion	DAC generating ramp	UART read values
9	ADC conversion(calib)	DAC generating ramp	UART read values

Table 5.3: Production test sequence

During the test-sequence, the calibration values are calculated within the python-script (see section 5.1) and stored to the EEPROM-memory if approved.

This test sequence was used for both produced RAT 1.0 prototype cards and the hardware design from section 3 was validated. One test output file example can be seen in the appendix Automated tests - output. The FPGA-voltages are within the recommendations, the DCCT-status pins, the supervisory circuits, LEDs and ADC-channels as well as calibration are working.

6 Conclusion

At the end of this master thesis, the hardware design was successful and respected the specification. The card responds to the analog to digital acquisition requirements (channel, filter, resolution) and is compatible to both formats through its extension card. The optic fiber communication aspect is also fulfilled.

On the gateway side, the IPs and each components were simulated separately and together successfully before being validated on the hardware. The automated calibration is also functioning as wanted. Finally, the flexibility is reached through the configuration selector.

The accuracy measurements of both old and new systems are presented in the last chapter. The new system reaches a similar precision as the previous one with a 6-times higher sample rate. It can also be used at up to 200 kHz when a higher sample rate is necessary. At the end of this chapter, the automated test and calibration software to simplify the production is developed.

To conclude and answer the introduction(1) question, the Remote Acquisition Transceiver card (RAT) fulfills the new BETS specification by being compatible to the other use-cases (format, sample rate, precision flexibility).

During this project, new knowledge in hardware analog and digital electronic design was acquired. In addition, the development methodology for gateway was gained. Last, the ADC calibration techniques were also learned.

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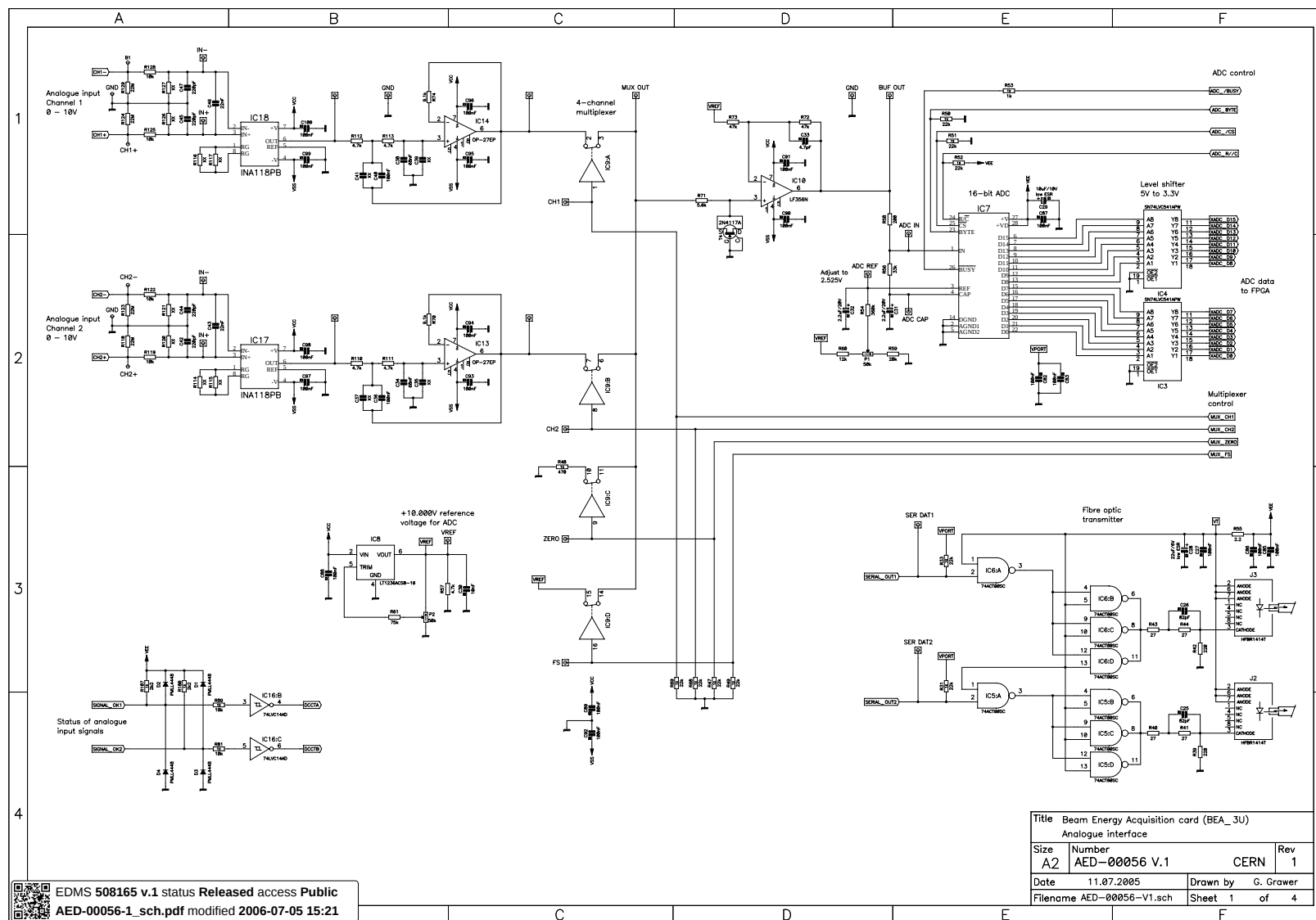
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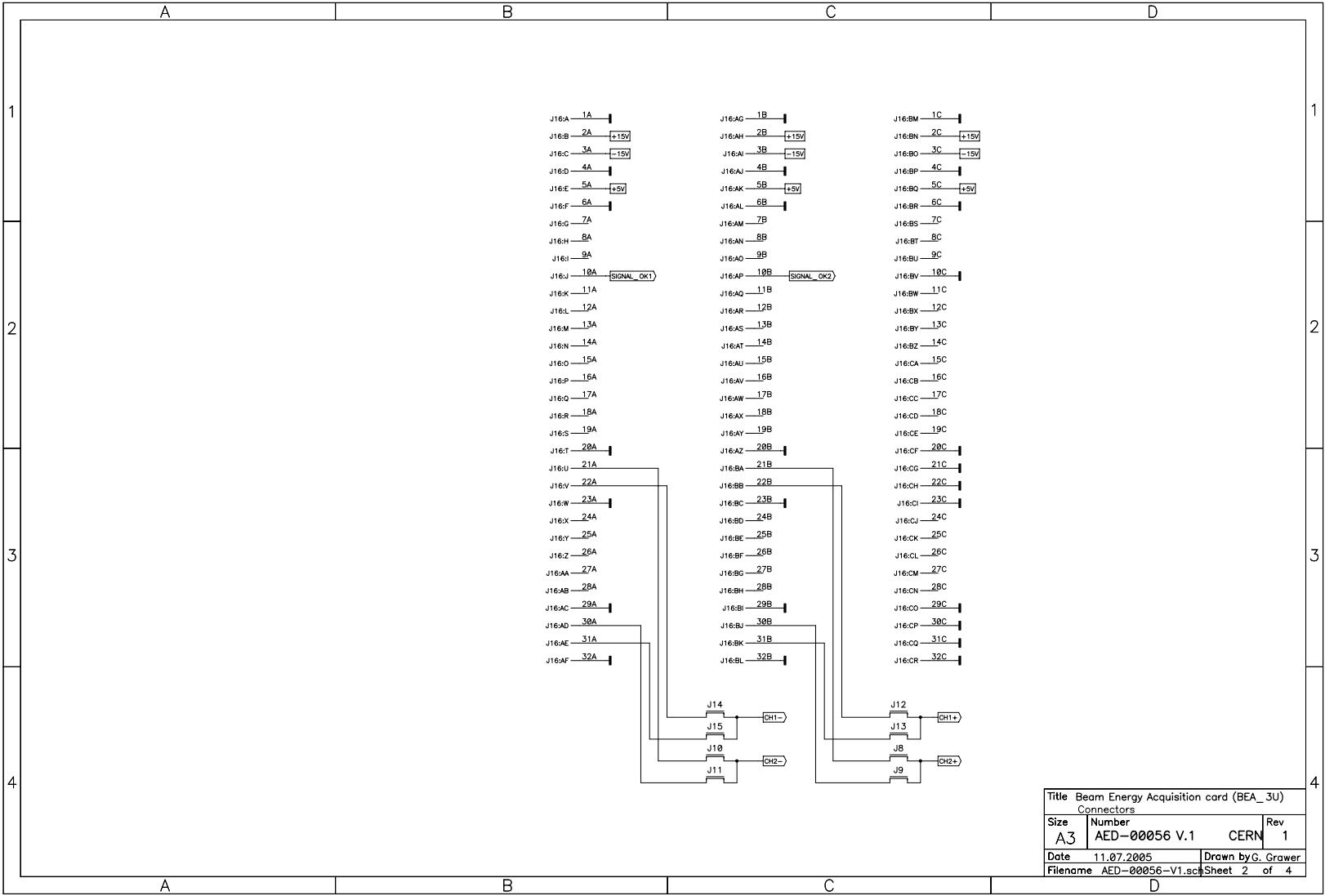
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Appendix

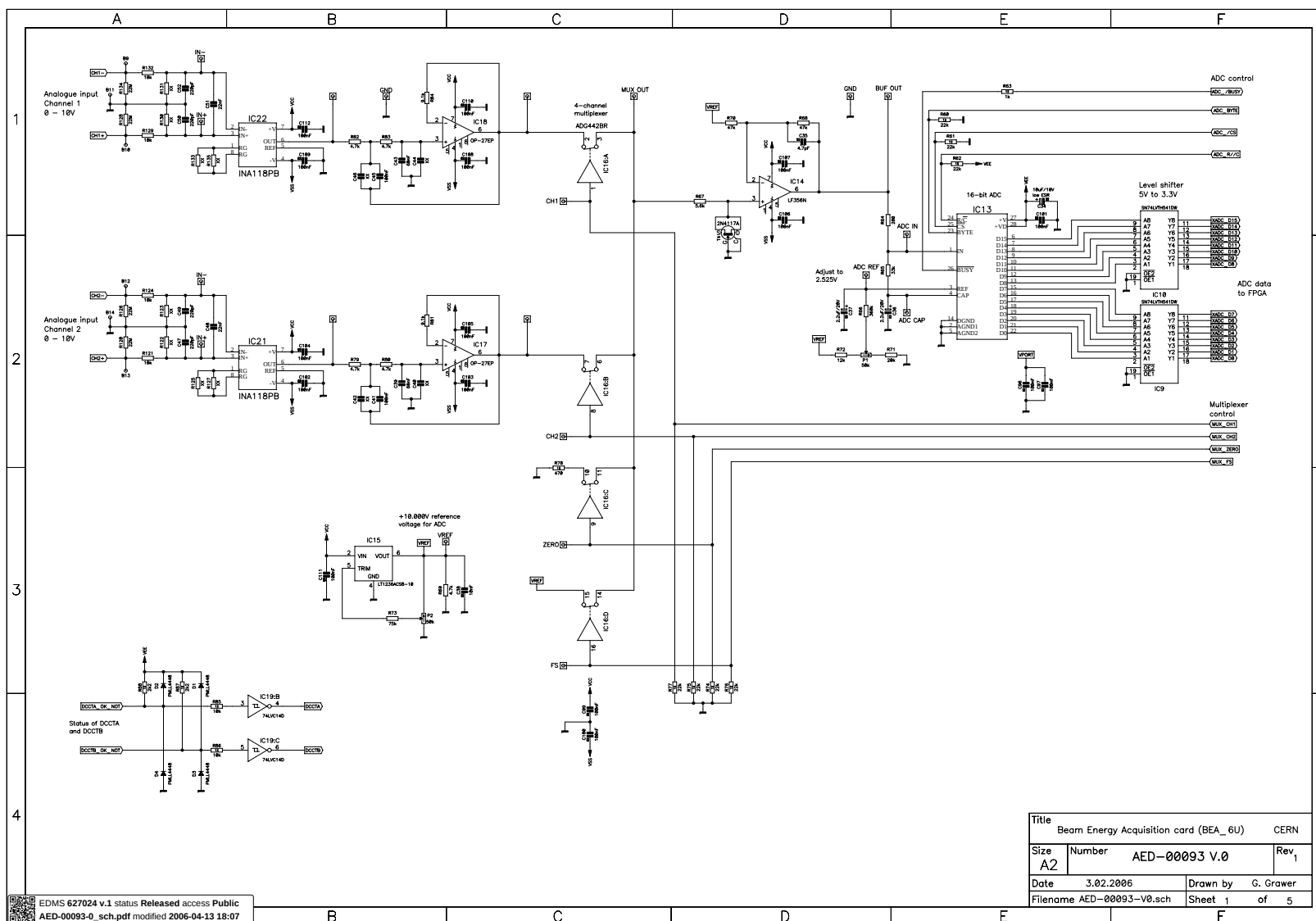
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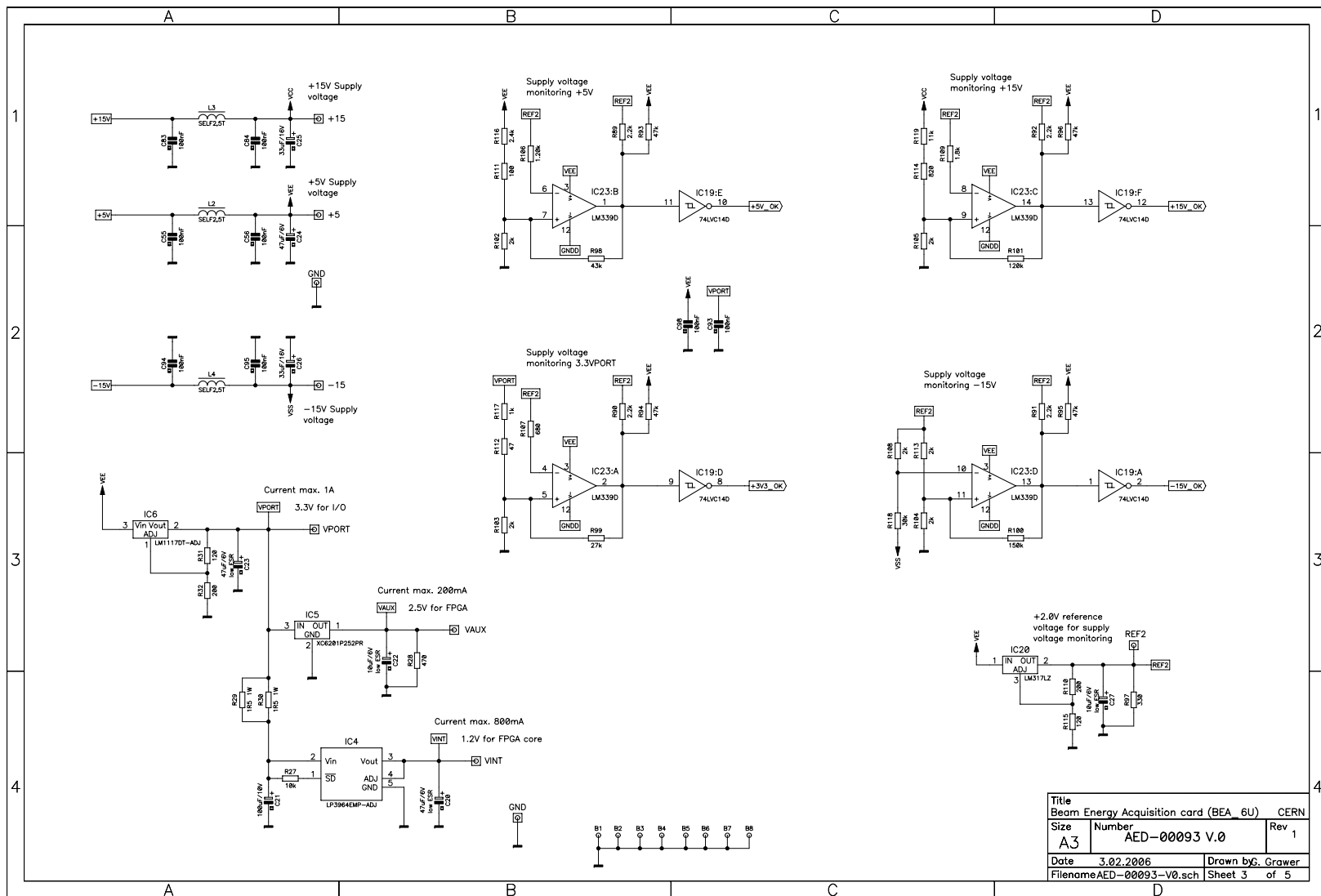


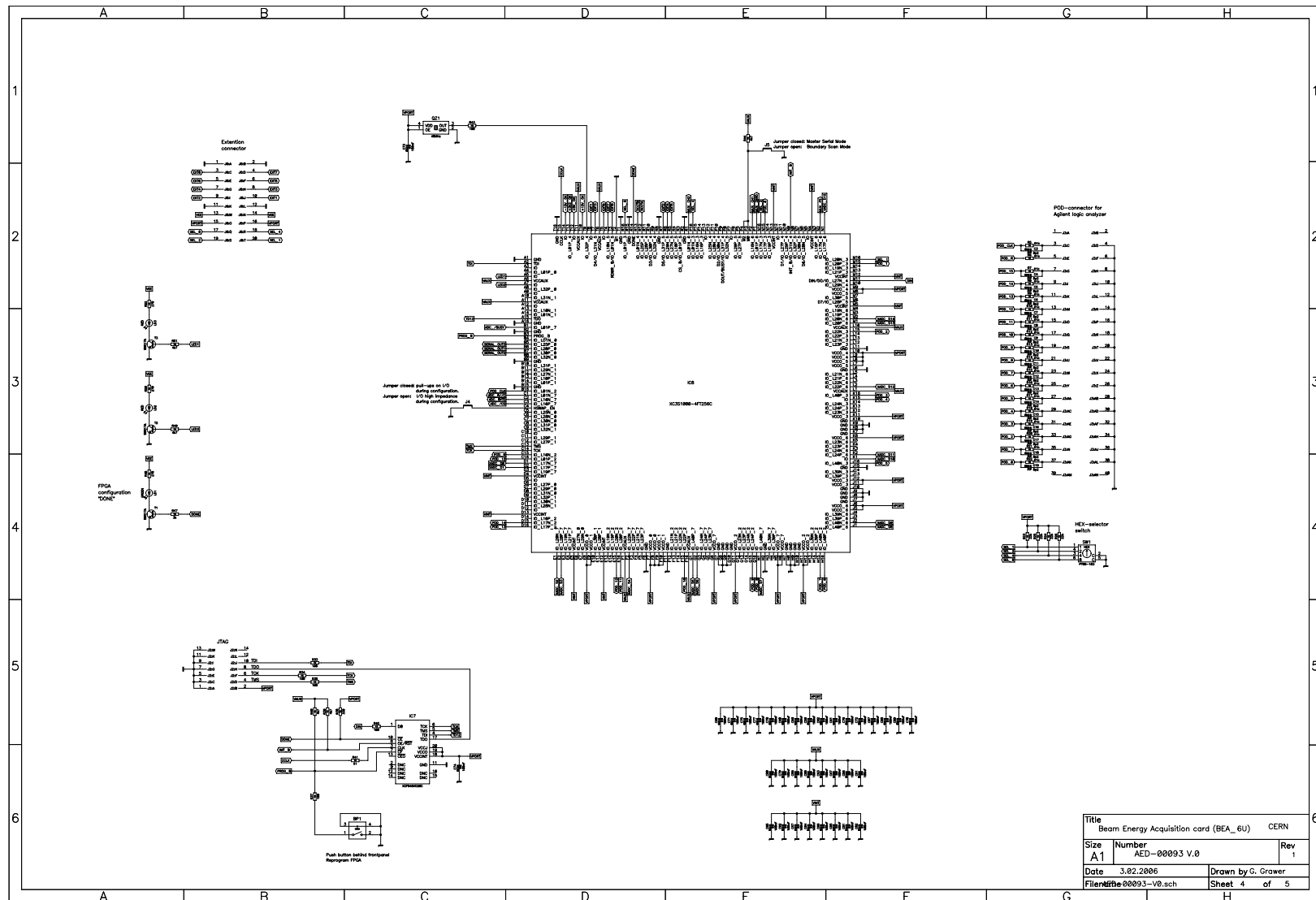


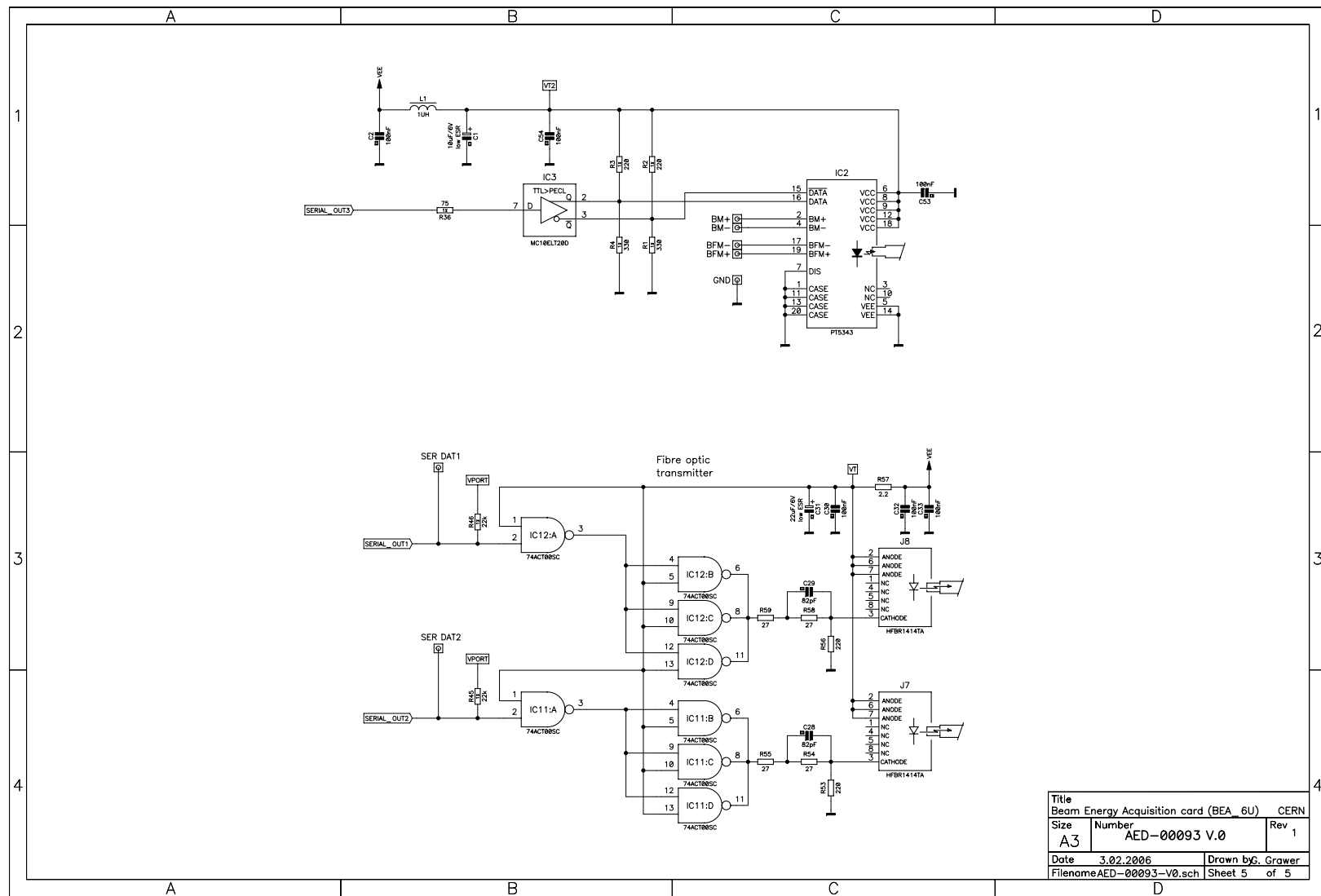
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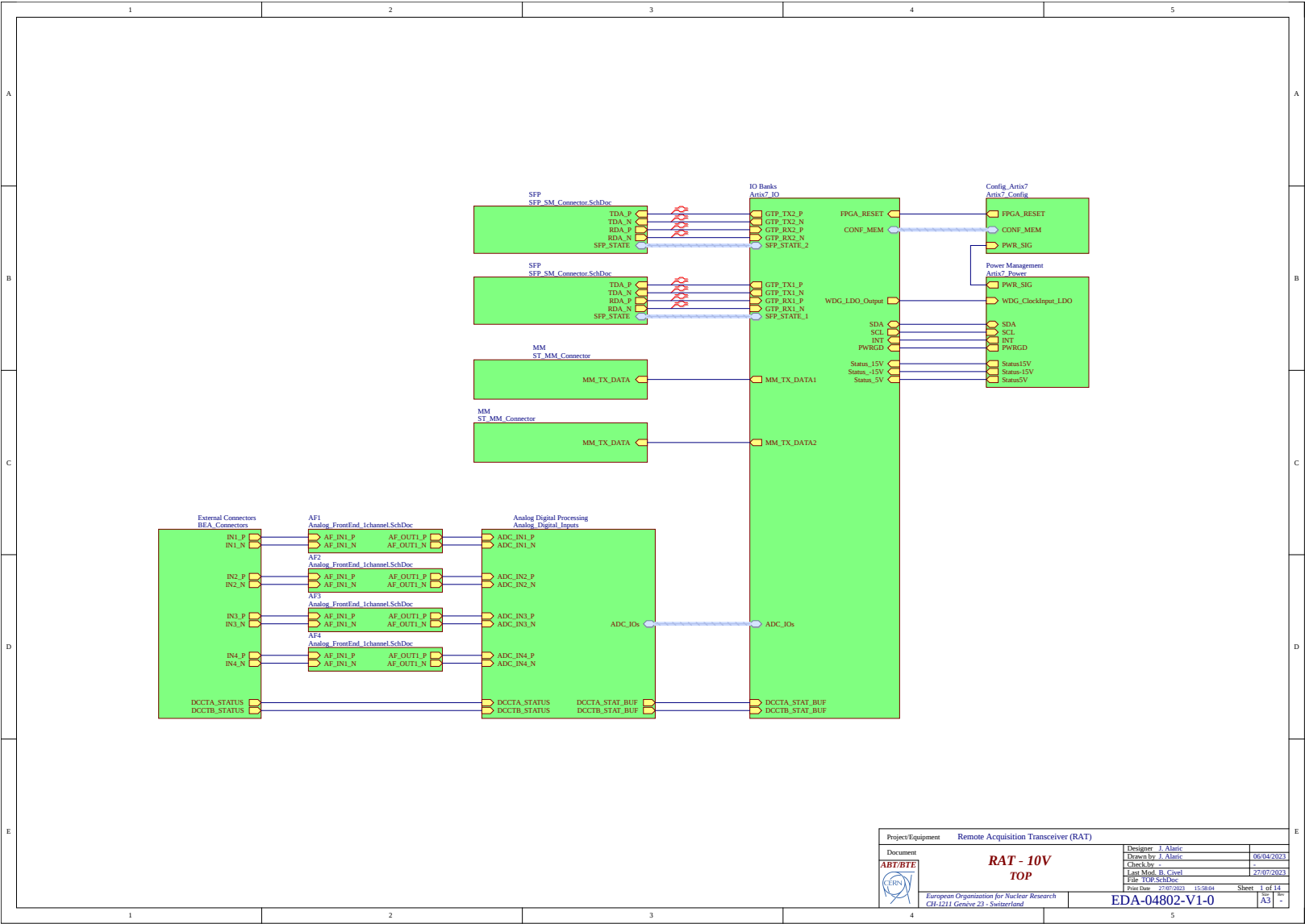


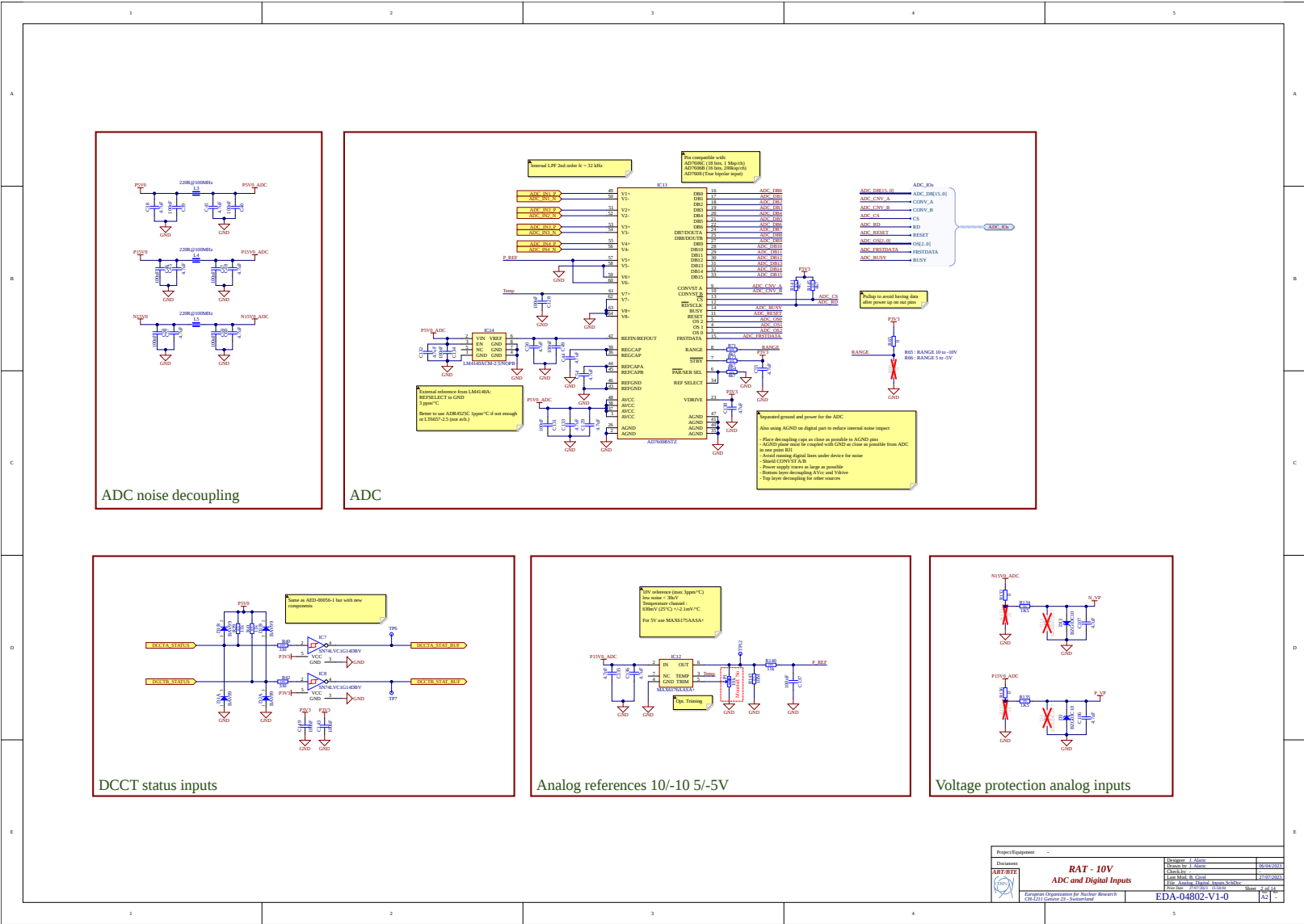


Power estimation (XPE)

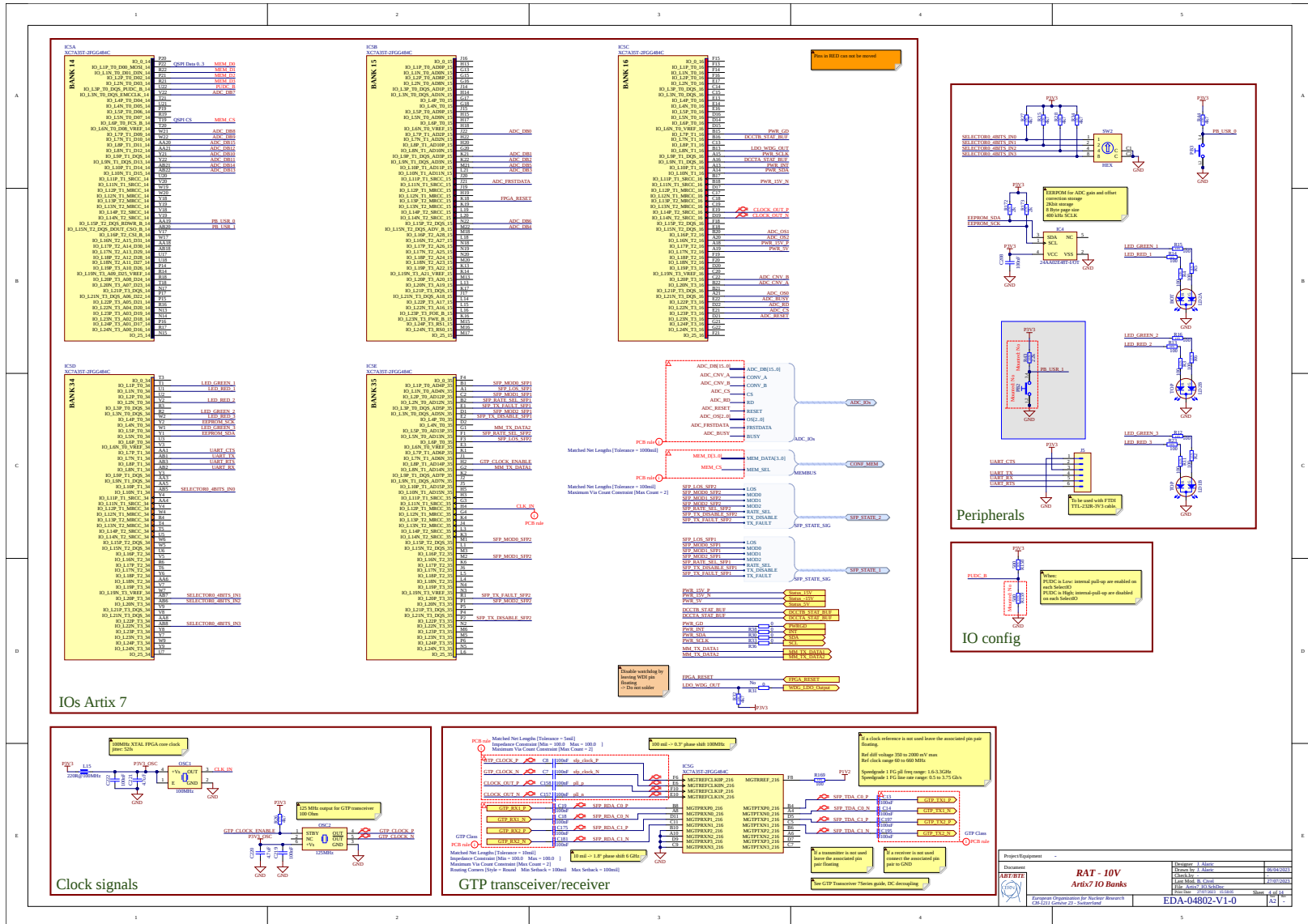


Remote Acquisition Transceiver (RAT / BEAv2)

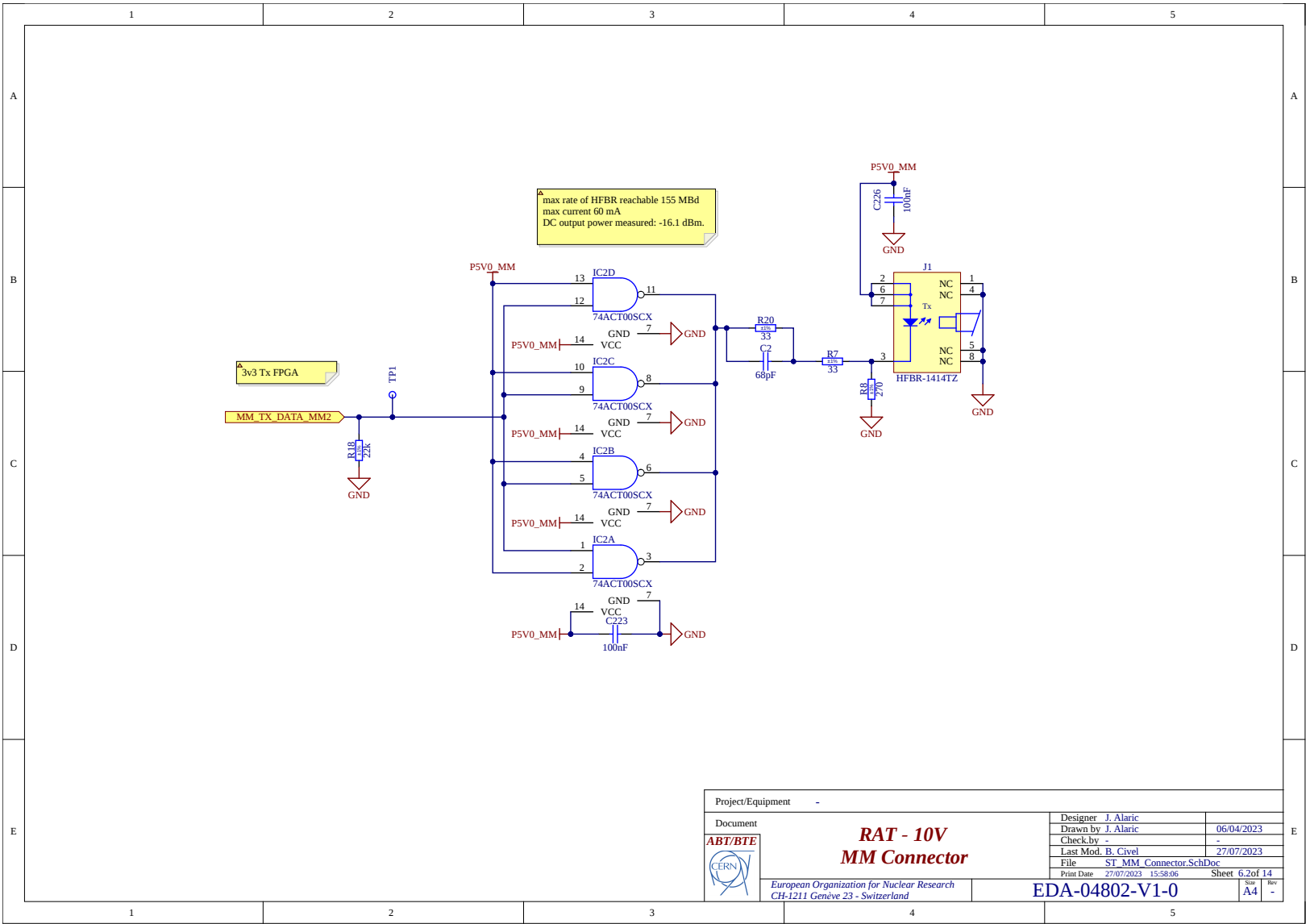


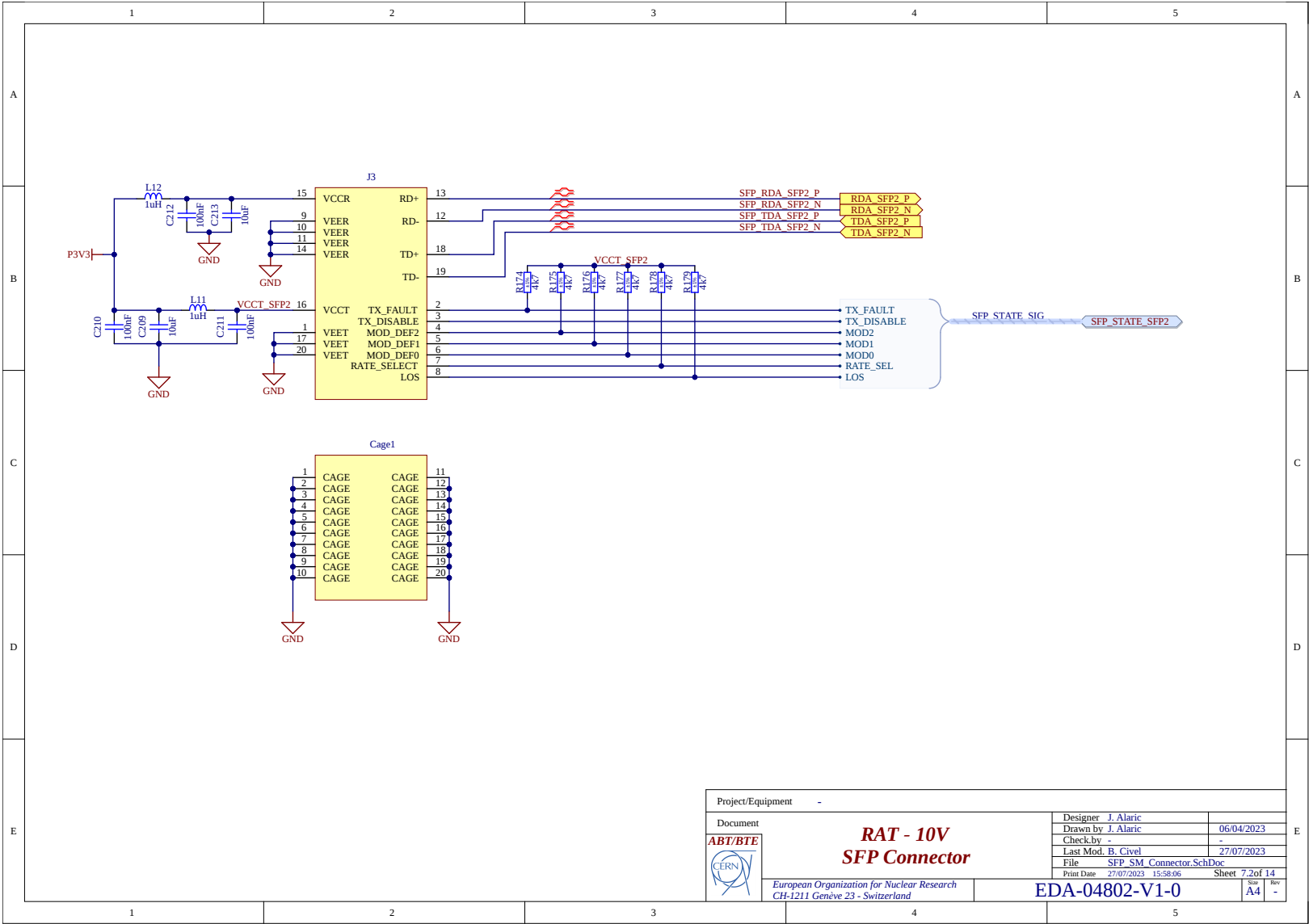




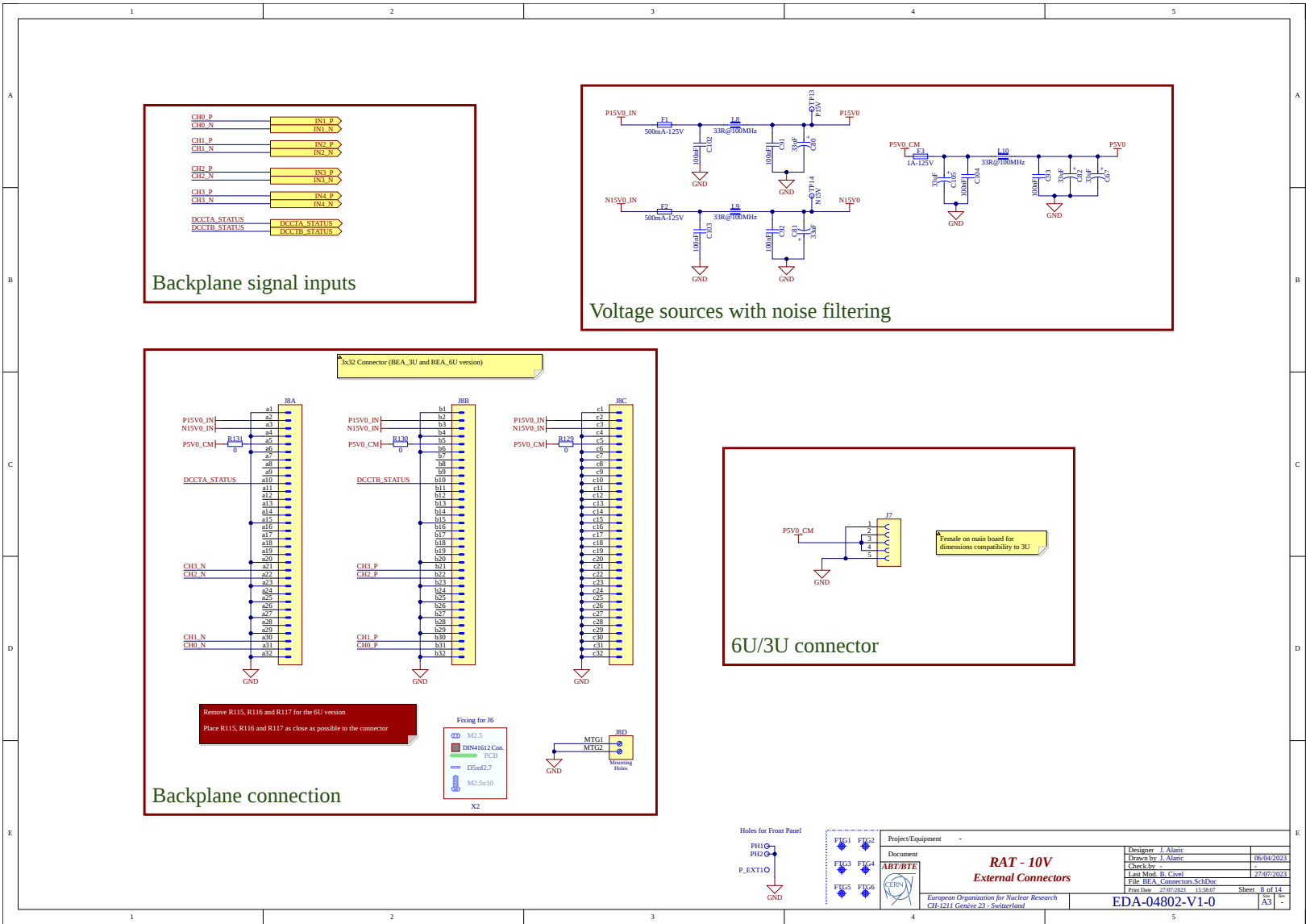


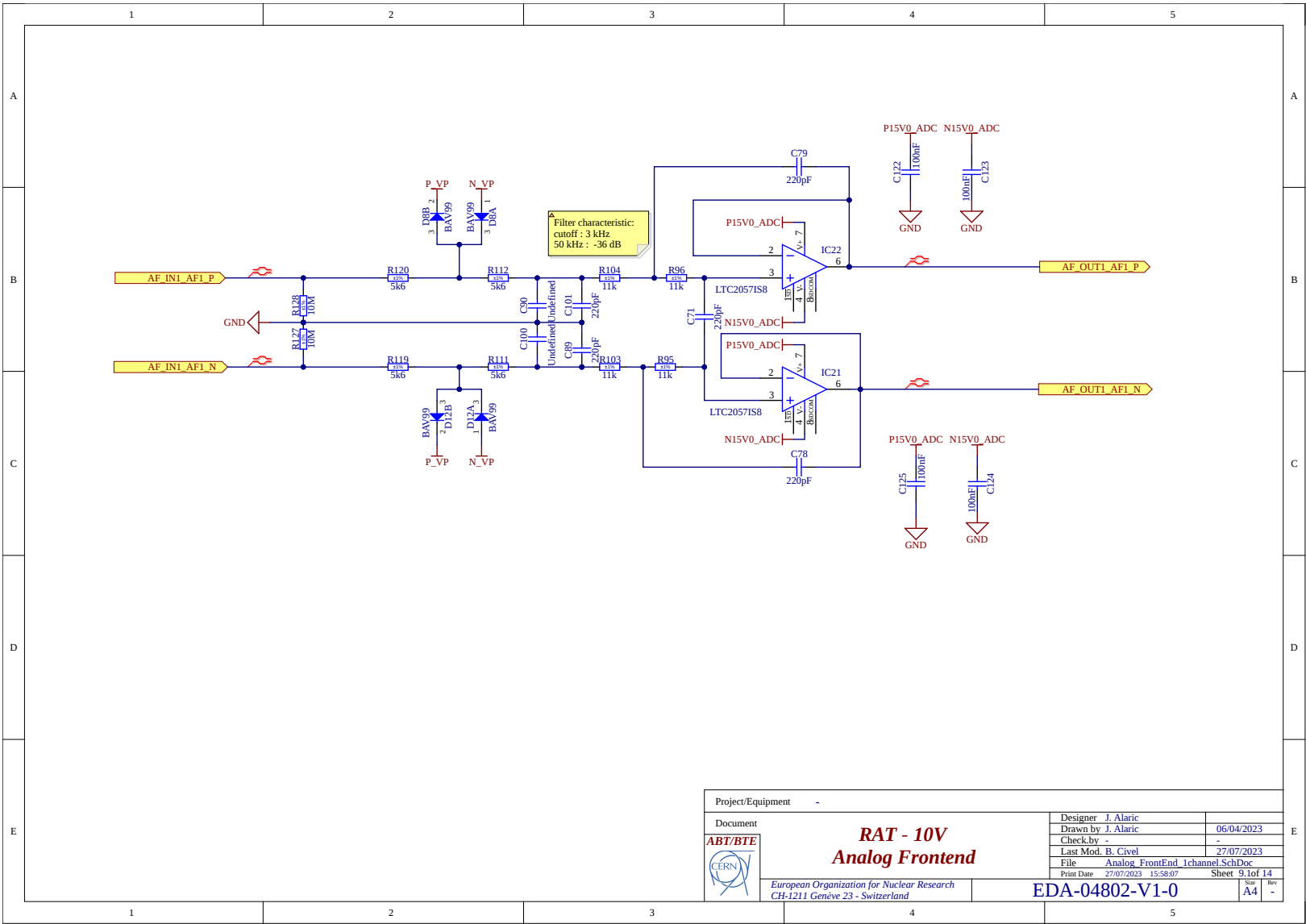


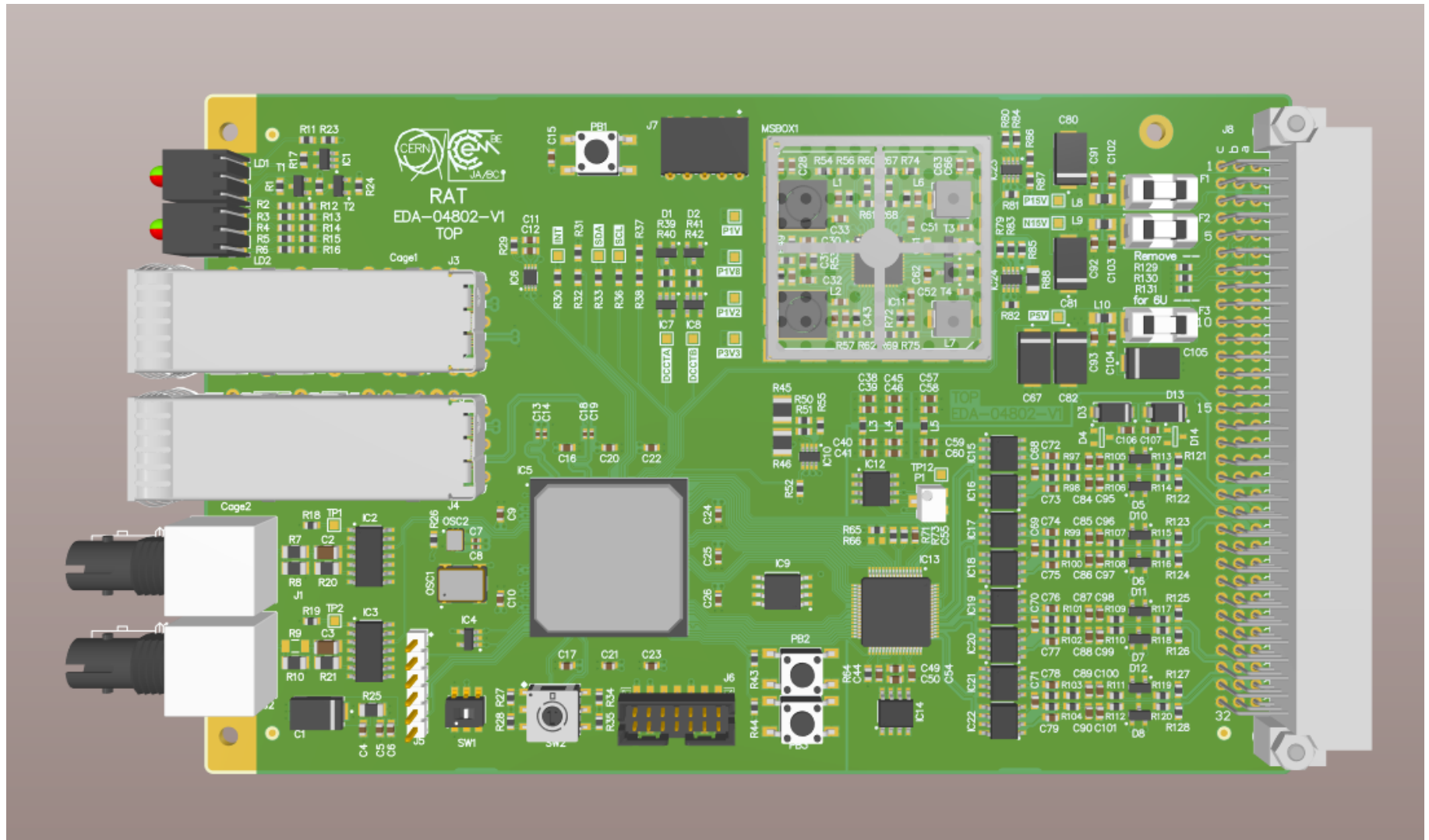


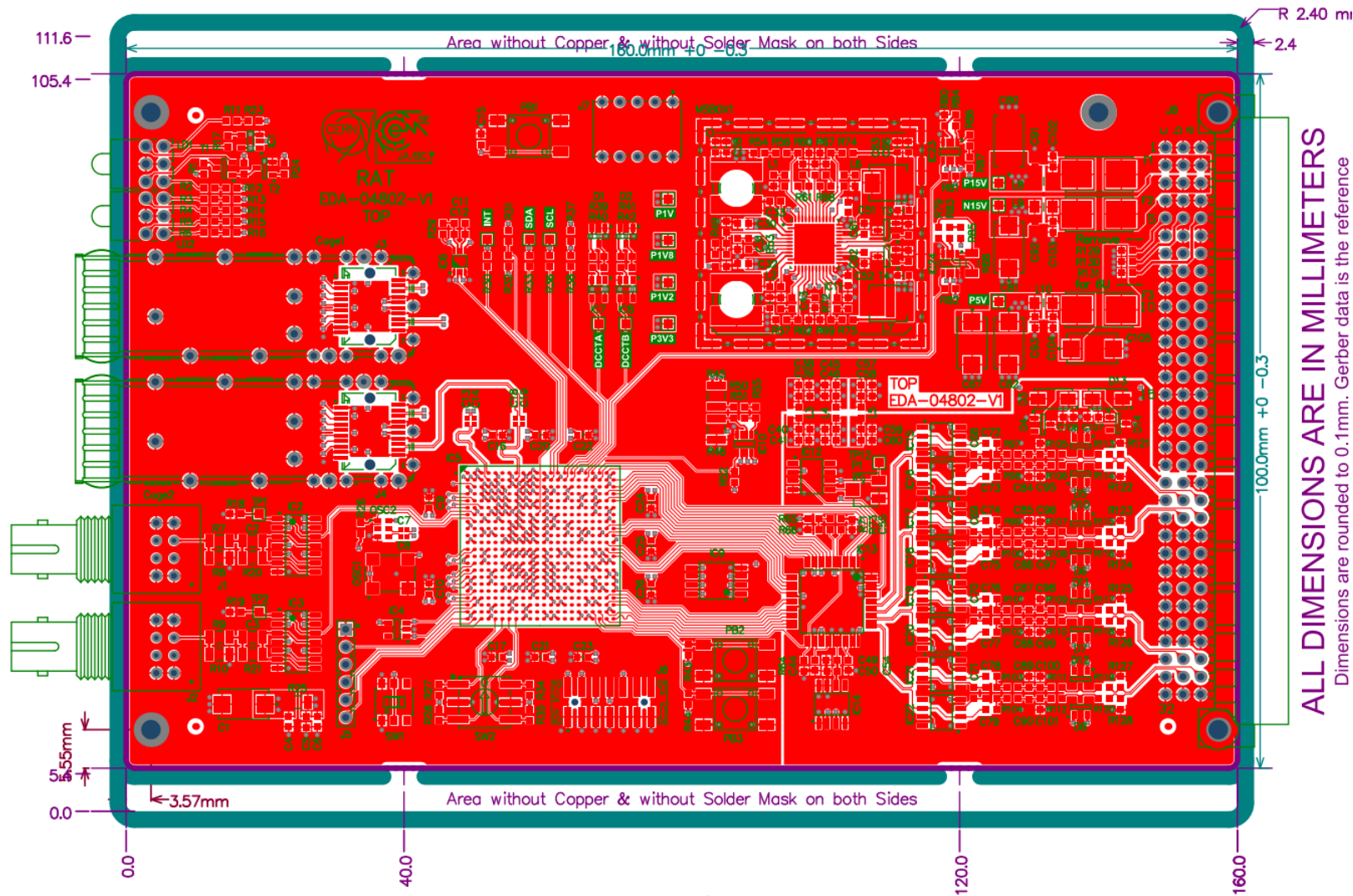


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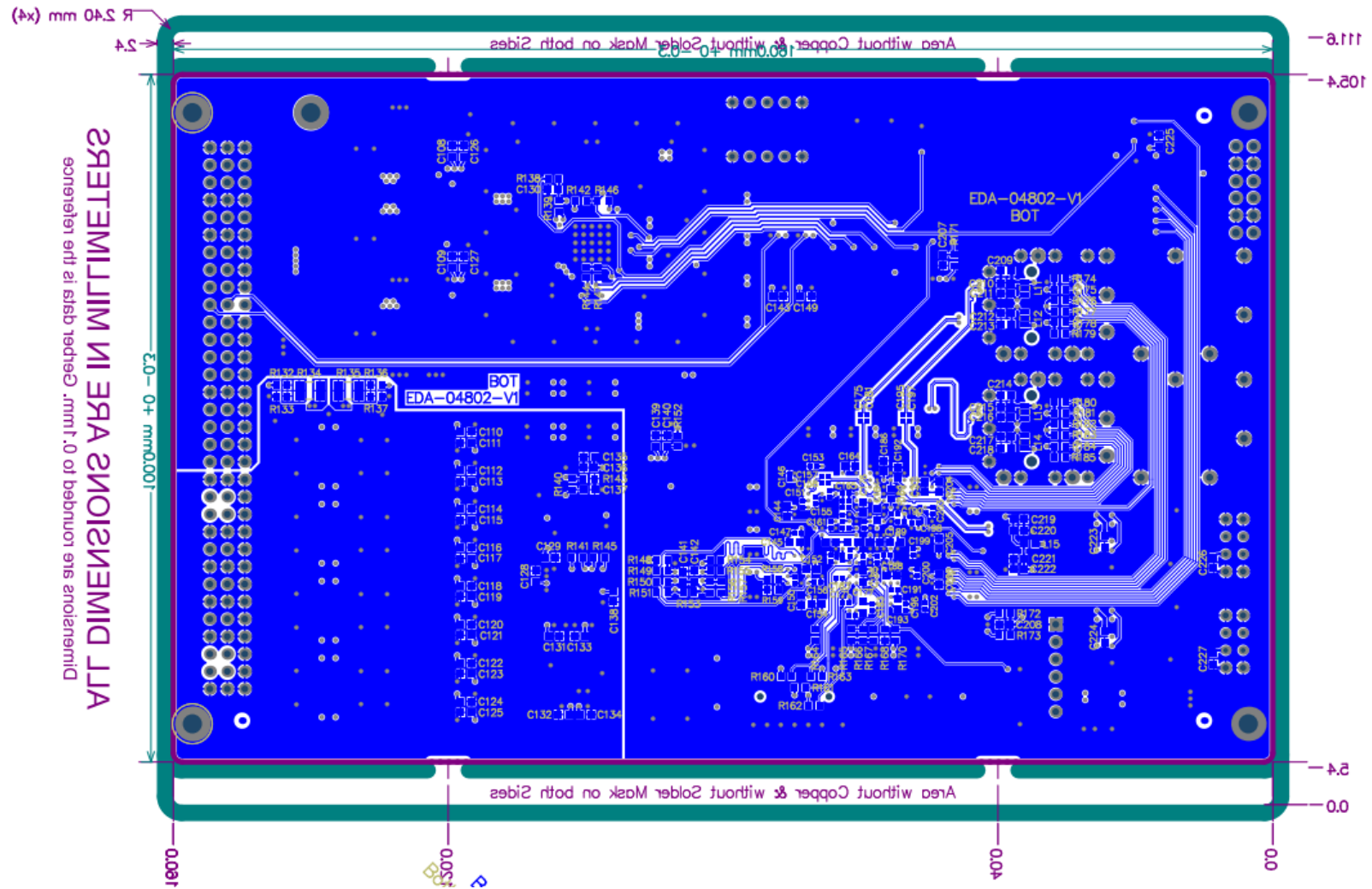


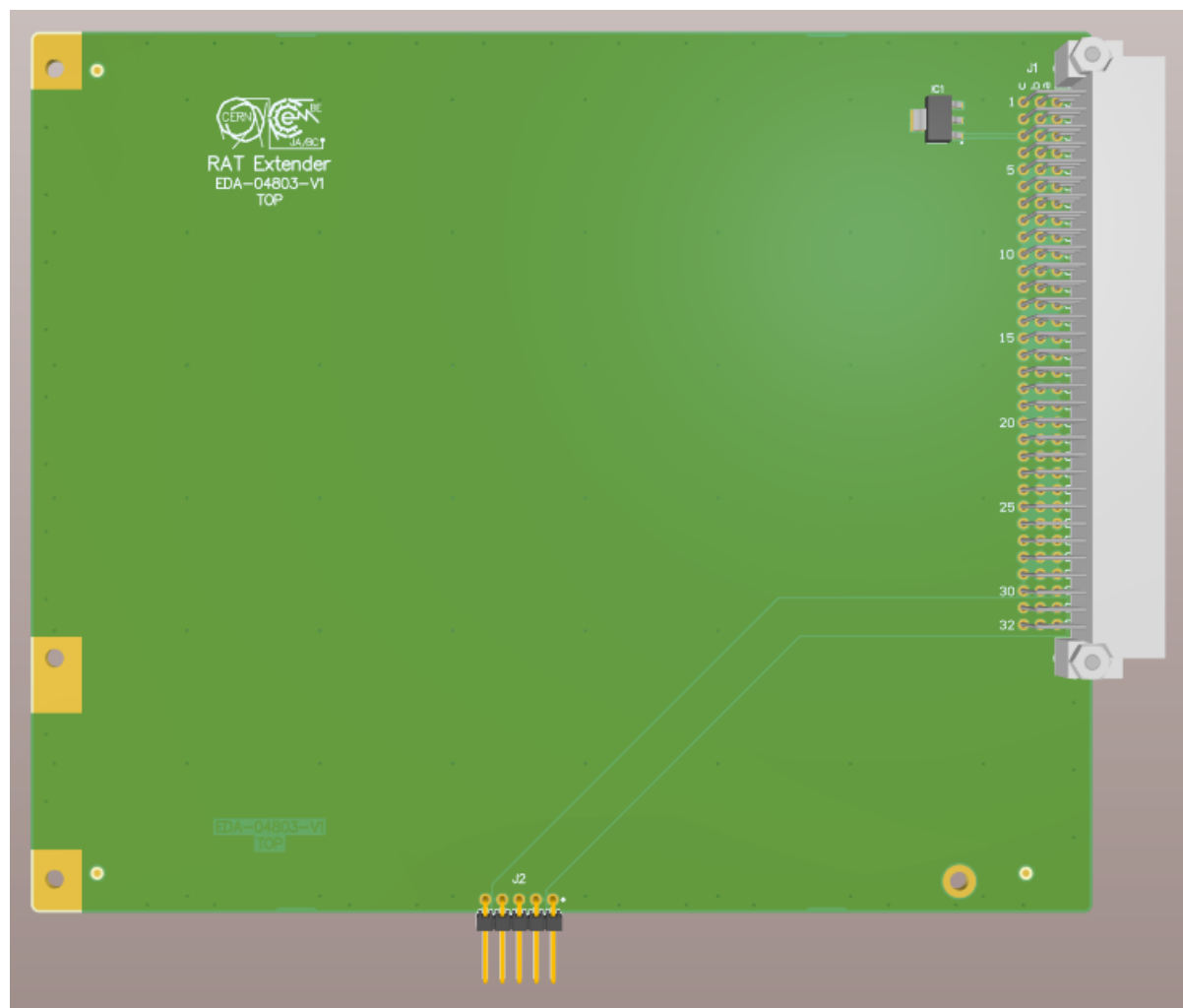


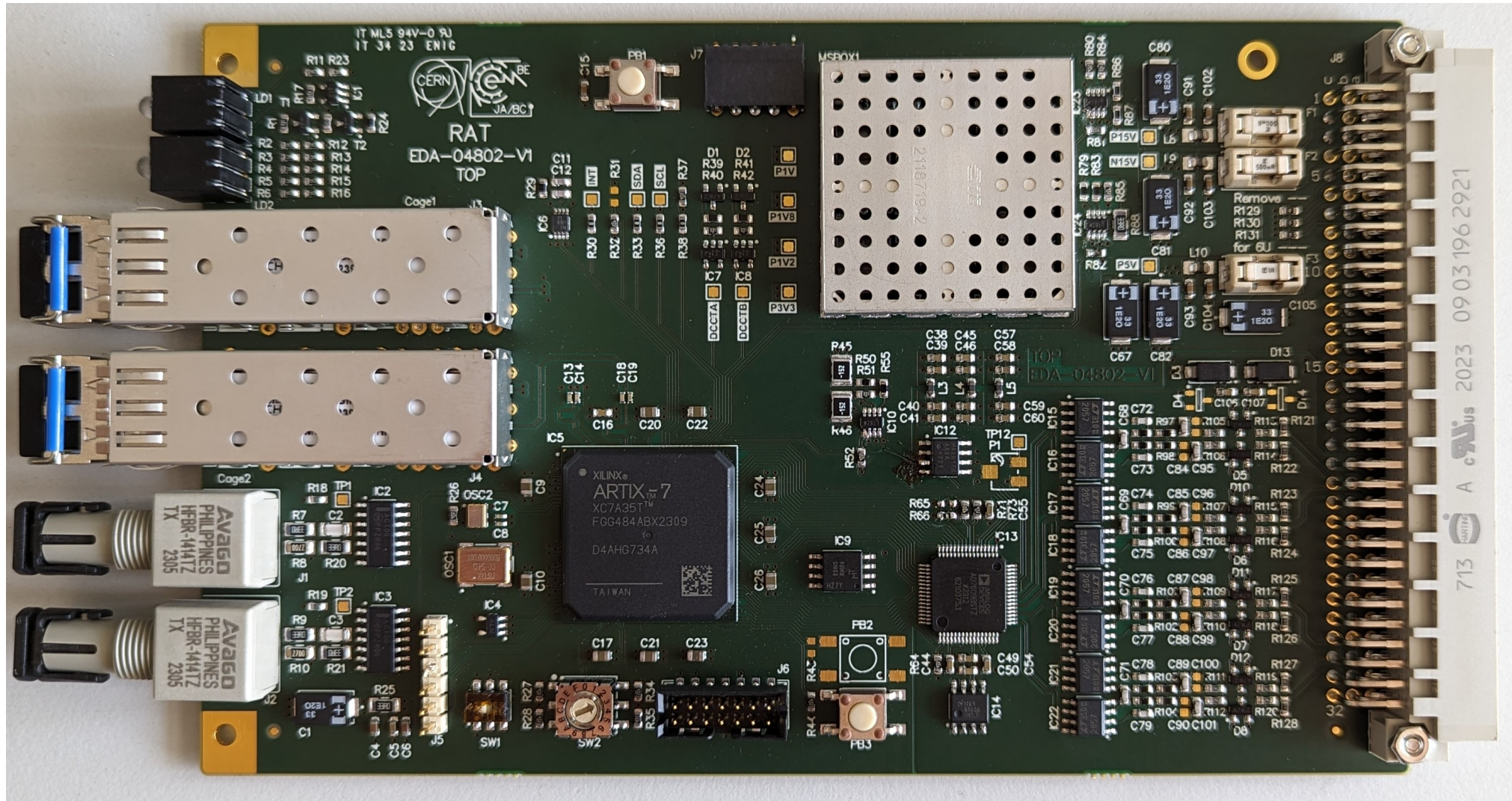


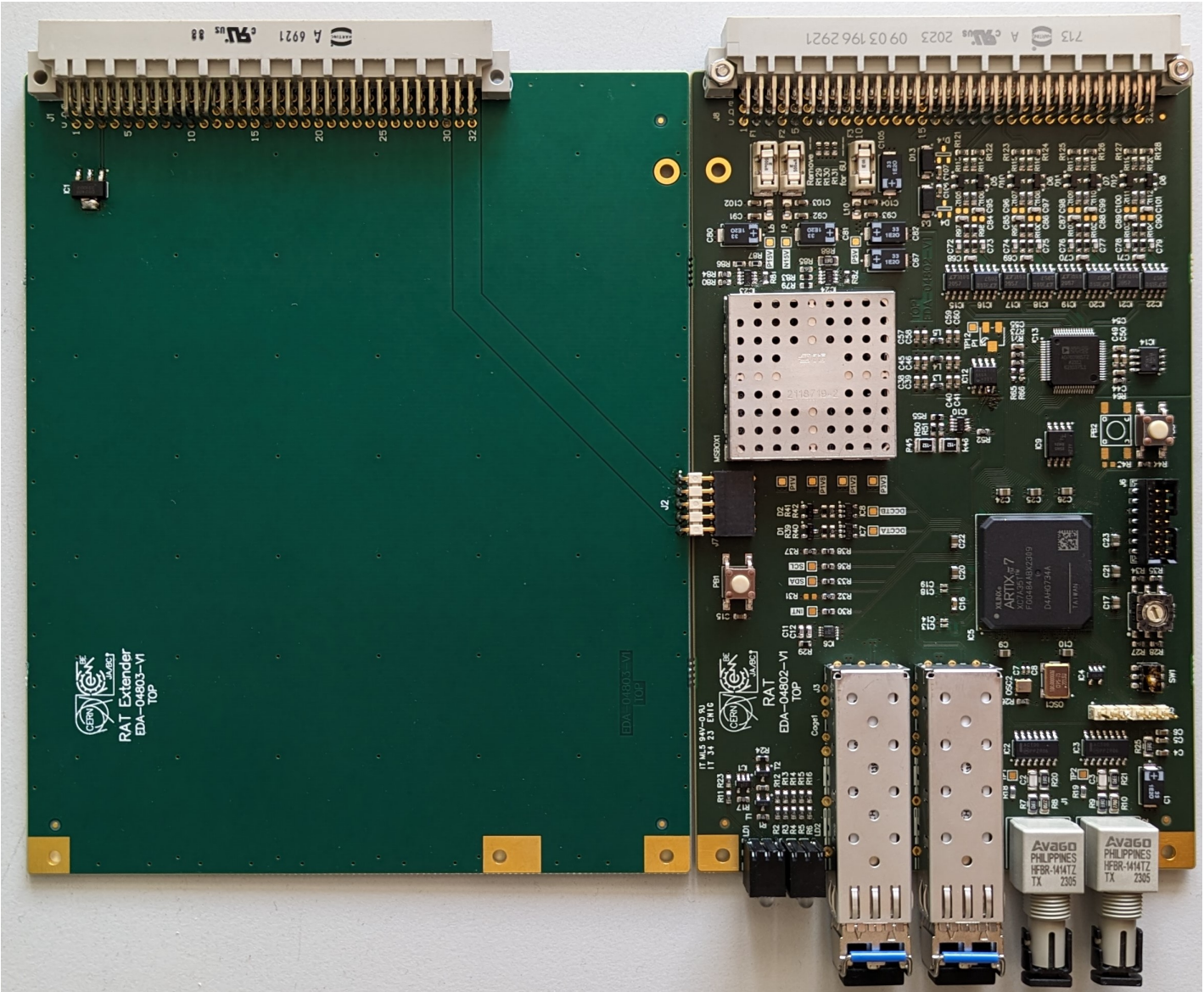


ALL DIMENSIONS ARE IN MILLIMETERS
Dimensions are rounded to 0.1mm. Gerber data is the reference









Automated tests - output

- RAT3U_NB-100000

- _____

- Production tag : 100000

- Test date : 21/09/2023 12:20:13

- On-board power supplies

- +1V : +1.006 V

- +1.8V : +1.772 V

- +1.2V : +1.200 V

- +3.3V : +3.279 V

- +15V : +14.979 V

- -15V : -15.023 V

- +5V : +4.922 V

- External power supplies

- +5V : +4.990 V / 275 mA

- +15V : +15.000 V / 13 mA

- -15V : -15.000 V / 12 mA

- ADC error msm no calibration:

- DAC : +0.000 V / Multimeter : -0.001 / ch0 : -0.0008 V / ch1 : -0.0011 V / ch2 : -0.0008 V / ch3 : -0.0002 V

- DAC : +0.100 V / Multimeter : +0.099 / ch0 : +0.0990 V / ch1 : +0.0985 V / ch2 : +0.0990 V / ch3 : +0.0993 V

- DAC : +0.200 V / Multimeter : +0.199 / ch0 : +0.1994 V / ch1 : +0.1990 V / ch2 : +0.1994 V / ch3 : +0.1999 V

- DAC : +0.300 V / Multimeter : +0.299 / ch0 : +0.2994 V / ch1 : +0.2989 V / ch2 : +0.2992 V / ch3 : +0.2997 V

- DAC : +0.400 V / Multimeter : +0.399 / ch0 : +0.3991 V / ch1 : +0.3988 V/ ch2 : +0.3992 V/ ch3 : +0.3996 V
 - DAC : +0.500 V / Multimeter : +0.499 / ch0 : +0.4994 V / ch1 : +0.4990 V/ ch2 : +0.4994 V/ ch3 : +0.4998 V
 - DAC : +0.600 V / Multimeter : +0.599 / ch0 : +0.5999 V / ch1 : +0.5994 V/ ch2 : +0.5999 V/ ch3 : +0.6004 V
 - DAC : +0.700 V / Multimeter : +0.699 / ch0 : +0.6997 V / ch1 : +0.6995 V/ ch2 : +0.6998 V/ ch3 : +0.7002 V
 - DAC : +0.800 V / Multimeter : +0.799 / ch0 : +0.7995 V / ch1 : +0.7992 V/ ch2 : +0.7995 V/ ch3 : +0.7999 V
 (truncated...)

CH1 : Calibration coefficient founded [FPGA format]: offset = -247871 order 1 : 1073344754 order 2 : -4

CH2 : Calibration coefficient founded [FPGA format]: offset = 80556 order 1 : 1073281649 order 2 : -4

CH3 : Calibration coefficient founded [FPGA format]: offset = -227145 order 1 : 1073270929 order 2 : -4

CH4 : Calibration coefficient founded [FPGA format]: offset = -607170 order 1 : 1073381523 order 2 : -4

CH1 : Calibration coefficient founded [Calculateds]: offset = -3.782210011699918 order 1 : 0.9996302000764675 order 2 : -3.60094348348774e-09

CH2 : Calibration coefficient founded [Calculated]: offset = 1.2291866516529693 order 1 : 0.9995714289144698 order 2 : -3.675281521753682e-09

CH3 : Calibration coefficient founded [Calculated]: offset = -3.4659592927752563 order 1 : 0.9995614449988375 order 2 : -3.598556176063633e-09

CH4 : Calibration coefficient founded [Calculated]: offset = -9.264685543656288 order 1 : 0.9996644437142405 order 2 : -3.428379892003526e-09

- ADC error msm calibrated:

- DAC : +0.000 V / Multimeter : -0.001 / ch0 : -0.0011 V / ch1 : -0.0012 V/ ch2 : -0.0010 V/ ch3 : -0.0008 V
 - DAC : +0.100 V / Multimeter : +0.099 / ch0 : +0.0986 V / ch1 : +0.0986 V/ ch2 : +0.0987 V/ ch3 : +0.0988 V
 - DAC : +0.200 V / Multimeter : +0.199 / ch0 : +0.1989 V / ch1 : +0.1988 V/ ch2 : +0.1987 V/ ch3 : +0.1989 V
 - DAC : +0.300 V / Multimeter : +0.299 / ch0 : +0.2991 V / ch1 : +0.2993 V/ ch2 : +0.2992 V/ ch3 : +0.2993 V
 - DAC : +0.400 V / Multimeter : +0.399 / ch0 : +0.3989 V / ch1 : +0.3986 V/ ch2 : +0.3988 V/ ch3 : +0.3988 V
 - DAC : +0.500 V / Multimeter : +0.499 / ch0 : +0.4990 V / ch1 : +0.4990 V/ ch2 : +0.4990 V/ ch3 : +0.4990 V
 - DAC : +0.600 V / Multimeter : +0.599 / ch0 : +0.5991 V / ch1 : +0.5991 V/ ch2 : +0.5993 V/ ch3 : +0.5991 V

(truncated...)

- DCCT status
- dccta : 0 ; dcctb : 0
- dccta : 1 ; dcctb : 1
- 15V supervisor : valid if $+15V > +14.20\text{ V}$ and $+15V < +15.80\text{ V}$

- -15V supervisor : valid if $-15V > -14.30\text{ V}$ and $-15V < -15.30\text{ V}$

- 5V supervisor : valid if $+5V > +4.60\text{ V}$ and $+5V < +5.70\text{ V}$