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Novel pixel CMOS sensors for radiation detection applications and sub-nanosecond timing measurements

By

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Declaration

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2025

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Abstract

The need for cost-effective, large-area sensors with improved timing resolution and low power consumption is currently growing across various fields of physics research and applications for the detection of high-energy charged particles and photons. Silicon detectors are extensively adopted, thanks to their adaptability and the rapid progress in the semiconductor industry. Among silicon detectors, Monolithic Active Pixel Sensors (MAPS) represent a cutting-edge technology in particle detection and imaging, combining high spatial resolution with cost-effectiveness and scalability. This thesis is focused on the simulation and characterisation of Complementary Metal-Oxide-Semiconductor (CMOS) pixel sensors for radiation detection and high resolution timing measurements. Among the different fields of applications, a particular focus is given to high-energy physics. In particular, this research work fits in the context of two distinct upgrades of A Large Ion Collider Experiment (ALICE) at the CERN LHC: the third generation Inner Tracking System (ITS3), where the Tower Partners Semiconductor Co. (TPSCo) 65 nm CMOS Image Sensor Process will be employed and ALICE 3, a proposal for the next-generation detector, designed as a follow-up to the present ALICE experiment in 2033.

Chapters 1, 2 and 3 provide an introduction covering the fundamental principles of silicon detectors, the aspects that influence their timing performance and the basics of charged particle tracking, with a particular focus on the above mentioned ALICE upgrades. An overview of several existing silicon-based technologies is subsequently provided.

A complete outline of the research approach is presented, aimed at predicting the performance of MAPS through simulations and then validating the results through test campaigns. For this reason, the first part of the research work, in Chapter 4, describes a combined approach of TCAD and Monte Carlo simulations, while the following part reports on the characterisation activities carried out on MAPS. The

activities have been accomplished in the framework of the Advanced Readout CMOS Architecture with Depleted Integrated sensor Arrays (ARCADIA) collaboration, a project funded by the Istituto Nazionale di Fisica Nucleare (INFN) that aims to develop Fully Depleted-MAPS, for which improved charge collection efficiency and timing performance are granted by a backside bias voltage for the complete sensor depletion. By importing the electric fields and weighting potentials extracted from TCAD in the Monte Carlo software, accurate simulations can be performed in an acceptable computing time. Both MAPS with small and large collection electrodes have been simulated and their timing performance extracted, demonstrating the impact of the weighting field uniformity, and therefore, of the sensor geometry, on the time resolution. A dedicated CMOS prototype, featuring a large collection electrode and integrated electronics, was produced in the LFoundry 110 nm CMOS commercial process to investigate the ARCADIA technology capabilities for fast timing applications, demonstrating sub-nanosecond timing performance. However, a larger collected charge or a higher power consumption were needed to improve the jitter.

To accomplish this goal, an innovative sensor concept was developed, as presented in Chapter 5, with the addition of a gain layer, allowing signal amplification by impact ionization. Experimental results on the first 110 nm CMOS avalanche detector prototype, demonstrated the presence of a gain between 2 and 3 and a time resolution around 230 ps. Following measurements with optimised working point led to a reduced and promising time resolution of approximately 150 ps.

Further investigation of the commercial technological nodes for High Energy Physics (HEP) applications was carried out through the validation of the 65 nm TPSCo CMOS imaging technology for the ALICE ITS3 upgrade, presented in Chapter 6. In particular, the Analog Pixel Test Structure with Operational Amplifier (APTS-OA) was characterised both in the laboratory and in test beam facilities. After the definition of the working point, optimised for the fast front-end response, an ^{55}Fe source was employed to calibrate the chip response using soft X-rays.

To assess the APTS-OA performance in terms of time resolution, spatial resolution, and detection efficiency with minimum ionizing particles, the chip was proficiently incorporated into a beam telescope. The modified pixel process demonstrated an impressive time resolution of 63 ps, a spatial resolution of $2\text{ }\mu\text{m}$ and a detection efficiency higher than 99%, with a substrate voltage of -4.8 V and a clusterisation threshold of $100\text{ }e^-$.

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Chapter 1

Fundamentals of silicon detectors

1.1 Introduction

Research in the field of particle physics has experienced, in the last decades, an increased employment of silicon detectors for timing and tracking applications. The reason behind this trend can be found in the great versatility of silicon detectors, the remarkable expansion of the semiconductor industry, and the advancement of its processing technologies.

From a historical point of view, the beginning of the solid state detectors era, and in particular, the one focused on silicon detectors, can be found around 70 years ago. Their success is due to the capability to efficiently detect radiation through electron-hole (e-h) pair generation, leading to an increased interest in their application to nuclear and particle physics. Unlike gas-based detectors, silicon detectors are small, solid, and require no high-voltage operation, making them attractive for miniaturisation and integration into experimental setups. The growth of the semiconductor industry, particularly with the development of transistors in the 1950s, led to improvements in silicon processing techniques, making the development of silicon detectors practical and reliable. Starting from 1955 to 1965, the development of silicon-based detectors began in many laboratories and institutes, including Oak Ridge National Laboratory in the U.S., the Chalk River Laboratories in Canada, the Atomic Energy Research Establishment of the United Kingdom and CEA, the Atomic Energy Commission of France. In 1960, an experiment at Brookhaven National Laboratory tested a silicon p-n junction detector for the first time with

high energy particles (750 MeV pions) [1]. In 1961 a single silicon substrate was segmented into multiple rectangular diodes, proving that by combining signals from different electrodes at varying times, the path of the ionizing particle could be reconstructed: the first pixel detector was born. Silicon strip-like sensors were produced for the first time and operated at -20°C at Karlsruhe in 1971 [2] and similar devices were employed in the same period at Argonne, Fermilab, and at the Department of Nuclear Medicine in Southampton [3]. 1969 saw the invention of Charge-Coupled Devices (CCD) thanks to Willard S. Boyle and George E. Smith, working at the Bell Laboratories, in New Jersey [4]. This invention set the beginning of the digital imaging revolution, since for the first time a light-sensitive silicon chip could store an image and then digitize it. The two physicists were awarded the Nobel Prize "for the invention of an imaging semiconductor circuit - the CCD sensor" in 2009.

Nowadays, silicon is a top choice material for particle detection, as the average energy required to produce e-h pairs is lower than the one required for gas, noble liquids or scintillators by an order of magnitude (3.6 eV for silicon and 20-40 V for non-semiconductor materials) [5]. Applications embrace a wide spectrum of possibilities, among which three can be considered as the driving ones: medical applications, space applications and high energy physics experiments. Indeed, the robustness of a semiconductor detector makes it well-suited for collider or satellite applications. Silicon detectors are easily adaptable to many fields of research, as they are light-weight and can be thinned down to a few tens of μm , but also in various high-tech systems, from portable phones to quantum technology [6]. Charged particle imaging is a widespread technique in many fields of science beyond high energy physics, like material science. For all the above-mentioned reasons, the scientific community expresses great interest in the development of spatially resolved silicon detectors that can provide also precise timing measurements. In this chapter, an introduction on the working principles of silicon detectors will be provided, representing a theoretical background for this work.

1.2 Silicon properties

Materials can be classified as insulators, conductors or semiconductors depending on their energy band structure. In insulators and semiconductors, the width of the *energy gap* E_g , separating the valence and the conduction band, determines how

easily electrons can move from the valence to the conduction band. Insulators feature a wide E_g and the Fermi level is placed in between them. As a result, even an increase in temperature is insufficient to excite electrons into the conduction band, leaving no carriers available for conduction. Conversely, conductors exhibit an overlap between the valence and conduction bands, with the Fermi level located within the conduction band. This overlap ensures the presence of free electrons in the conduction band, facilitating electrical conduction. Semiconductors fall between these two extremes, featuring a smaller energy gap than insulators. At 0 K the covalent bonds in the crystal lattice remain intact, preventing electron movement. However, as the temperature rises, thermal excitation enables electrons to jump from the filled valence band (at 0 K) to the conduction band, generating e-h pairs and enabling electrical conduction. Silicon belongs to the category of semiconductors and its most important properties are reported in App. A.1. It features an energy gap of 1.12 eV, a density of $\approx 2.33 \text{ g cm}^{-3}$ and it is the second most abundant element in the Earth's crust (about 28% by mass), after oxygen. Its low density makes it an ideal candidate for applications such as tracking in vertex detectors, where minimising material budget is crucial, while its abundance helps to reduce production costs, making it a cost-effective choice for large-scale detector fabrication. It behaves as an insulator at 0 K and, when the temperature rises, some electrons can be thermally excited and can transit to the conduction band, leaving a hole in the valence band. At the thermal equilibrium the e-h pairs formation is compensated by their recombination. At room temperature, the intrinsic concentration of free charge carriers is $n_i = 1.09 \cdot 10^{10} \text{ cm}^{-3}$, representing the number of electrons per unit volume in the conduction band. The well-known law of mass action tells that, for a given temperature, the product between the concentration of electrons n and holes p is constant [7]:

$$n \cdot p = n_i^2 \quad (1.1)$$

The electrical properties of silicon can be adjusted to fit specific requirements through doping, briefly described in the next paragraph.

1.2.1 Doping

The doping process consists in introducing additional atoms in the silicon crystal lattice. If the additional atom belongs to the V group (as Phosphorous (P), Arsenic

(As) or Antimony (Sb)), an energy state will be located in the energy gap, in proximity to the conduction band. From this energy state, electrons can easily jump into the conduction band, producing a positively charged atom. In this case, the silicon is called *n-doped* and N_D is the donor atom concentration. If the additional atom belongs to the III group (as Boron (B)), its energy level will be located a few meV above the valence band and, in this case, electrons can easily reach this state from the valence band. As a consequence, the atom becomes negatively charged and the silicon is called *p-doped*, while the acceptor atom concentration is indicated as N_A . Based on (1.1), if the donor concentration is N_D , the hole concentration p is given by: $p = n_i^2/N_D$. Similarly, in p-doped silicon, p is equal to the acceptor atom concentration N_A and the electron concentration can be computed as $n = n_i^2/N_A$. In n-doped silicon, electrons are the majority carriers, while holes are in p-doped silicon. In both cases, the ionised atoms are not involved in the current, as they remain fixed. An important quantity describing the electrical properties of semiconductors is the resistivity ρ , defined as:

$$\rho = \frac{1}{(nq\mu_n + pq\mu_p)} \quad (1.2)$$

where q is the elementary charge, μ is the mobility, n and p are the n-type and p-type doping concentrations, respectively. The mobilities of electrons and holes are:

$$\mu_e \sim 1350 \text{ cm}^2/(\text{V} \cdot \text{s}), \quad \mu_h \sim 480 \text{ cm}^2/(\text{V} \cdot \text{s}) \quad (1.3)$$

In intrinsic silicon $n = p = n_i$, resulting in a resistivity¹ $\rho \sim 230 \text{ k}\Omega \cdot \text{cm}$ at 300 K [8], and the number of carriers is orders of magnitude higher than the ones expected from a particle interaction with silicon. For this reason, the combination of silicon regions with different doping, namely a junction, is fundamental to build a region without free charge carriers, able to work as a particle detector.

1.2.2 p-n junction

To develop a region without free charges, one can put in contact a portion of silicon doped with donors (*n*-side) and one doped with acceptors (*p*-type), building a junction. The electrons and holes, free to move, will diffuse by thermal motion: electrons will leave the *n* region to reach the *p*, leaving behind their donor atoms that will turn

¹Typical values of resistivity for semiconductors lie in the range: $10^{-3} < \rho < 10^5 \text{ }\Omega \cdot \text{cm}$.

into positively fixed charged ions. The opposite happens for holes, that will leave the p-doped side to move to the n-side. This phenomenon generates a *space charge region*, called *depletion region*, where the dopant ionised atoms remain fixed and free carriers are not present anymore. A potential difference will then arise between the negatively charged p-side and the positively charged n-side. When this potential barrier becomes higher than the thermal energy needed for the charges to diffuse, the phenomenon stops and the result is a region empty of free charge carriers (in which the charge density $\rho \neq 0$, since fixed charges are no more compensated by free charges), surrounded by two conductive regions: the n and the p doped neutral regions. The potential across the p-n junction is called *built-in potential*, acting as a barrier for the diffusion of electrons towards the p-side and holes in the n-side. The concept is illustrated in Fig. 1.1.

From Poisson equation it is possible to calculate the extension of the depletion

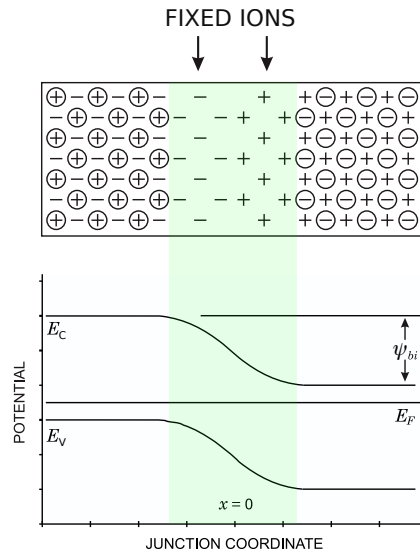


Fig. 1.1 P-n junction with fixed ionised atoms highlighted in green in the space charge region. Illustration of the built-in potential across the barrier. Image source [9].

region and the built-in potential:

$$\begin{cases} \frac{d^2 \psi}{dx^2} = -\frac{\rho}{\epsilon} = \frac{q}{\epsilon} N_A & -x_p \leq x \leq 0 \\ \frac{d^2 \psi}{dx^2} = -\frac{\rho}{\epsilon} = -\frac{q}{\epsilon} N_D & 0 \leq x \leq x_n \end{cases} \quad (1.4)$$

where Ψ is the potential as a function of the position and $\epsilon = \epsilon_0 \epsilon_r$ is the permittivity of silicon. The discussion and results presented in this paragraph hold in the abrupt

junction approximation. By integrating (1.4), the following expressions can be obtained for the potential in the p and n-side, respectively [7]:

$$\begin{cases} \psi = \frac{1}{2} \frac{qN_A}{\epsilon_0 \epsilon_r} x^2 + \frac{qN_A}{\epsilon_0 \epsilon_r} x x_p + \frac{1}{2} \frac{qN_A}{\epsilon_0 \epsilon_r} x_p^2 & -x_p \leq x \leq 0 \\ \psi = \frac{1}{2} \frac{qN_D}{\epsilon_0 \epsilon_r} x^2 + \frac{qN_D}{\epsilon_0 \epsilon_r} x x_n + \frac{1}{2} \frac{qN_A}{\epsilon_0 \epsilon_r} x_p^2 & 0 \leq x \leq x_n \end{cases} \quad (1.5)$$

Moving now to the electric field and imposing the continuity at the junction, one gets the condition

$$qN_A x_p = qN_D x_n \rightarrow \frac{N_A}{N_D} = \frac{x_n}{x_p}. \quad (1.6)$$

This means that the depletion region extends more in the less doped side of the junction. The two solutions of (1.5) join at $x = 0$, so the *built-in* potential can be computed as:

$$\psi_n - \psi_p = \psi_{BI} = \frac{1}{2} \frac{q}{\epsilon_0 \epsilon_r} (N_A x_p^2 + N_D x_n^2) \quad (1.7)$$

Solving now for x_n and x_p , the total width of the depletion zone can be calculated, which depends on the doping concentrations of both sides of the junction. In particular, one has:

$$d = x_n + x_p = \sqrt{\frac{2\epsilon_{Si}}{q} \frac{(N_A + N_D)}{N_A N_D} (\psi_{BI} + V_{BIAS})} \quad (1.8)$$

which allows to compute the total width of a p-n junction as a function of the doping levels and of the reverse bias voltage applied. Typically, one side of the junction is more doped than the other, for example it can be $N_A \gg N_D$ in the case of a junction between a p+ doped silicon and a n- one ². In this case the depletion region extends mainly in the n side, the less doped one. In fact one has $d \simeq x_n \simeq \sqrt{\frac{2\epsilon V}{e N_D}}$.

To maintain a neutral region across the junction, the number of ionized acceptor atoms in the p-side must balance that of ionized donor atoms in the n-side. Indicating A as the cross-sectional area of the junction and considering the origin of the x axis at the junction, it is possible to write:

$$(-qN_A)(-x_p A) = qN_D x_n A \quad (1.9)$$

²In this notation, the “+” indicates a strongly doped silicon region (e.g., p+), while “-” indicates a lightly doped one (e.g., n-).

which brings again to (1.6). The potential difference between the n-side and the p-side can also be written as [7]:

$$\psi_n - \psi_p = \phi_T \ln \frac{n_n}{n_p} \quad (1.10)$$

where $\phi_T = \frac{k_B T}{q}$ is called the thermal voltage, n_n and n_p are the electron concentration in the n-side and in the p-side, respectively. Since $n_n = N_D$ and $n_p = n_i^2 / N_A$, one has:

$$\psi_n - \psi_p = \psi_{BI} = \phi_T \ln \frac{N_A N_D}{n_i^2} \quad (1.11)$$

that expresses the *built-in potential* in another shape. For example, considering $T = 300$ K, for $N_A = 10^{16} \text{ cm}^{-3}$ and $N_D = 10^{12} \text{ cm}^{-3}$, $\psi_{BI} \sim 0.4$ V.

However, a simple p-n junction is not sufficient to build a silicon detector, as the number of thermally generated e-h pairs is orders of magnitude higher than the ones produced by the passage of a particle. This would result in a signal fully hidden by noise. In order to improve the Signal-To-Noise ratio (SNR), a first possibility is to cool down the detector, since $n_i \propto e^{\frac{-E_g}{2k_B T}}$, and a second is to apply an external reverse bias to the junction, in order to generate a depletion region without free carriers.

Forward and reverse bias

It's possible to apply an external voltage to the p-n junction operating it in *forward bias*, when a positive potential difference is applied between the p side and the n side. In this case, a strong current will flow as the electrons will move from the n region across the junction and this will reduce the net potential barrier. The second case is the reverse bias configuration, when a positive potential difference is applied between the n side and the p side. The external voltage will, in this case, enlarge the potential barrier across the junction and, as a consequence, the depleted region will extend. The free carriers will no more cross the junction and the system can now be used as a particle detector.

1.2.3 Leakage current

The desired current in a silicon detector is the one induced by the passage of a particle, but in a real detector there is always a current, called *leakage current*, even

if no particle is hitting it. Among the main causes there are: thermal generation of e-h pairs, both at the surface of the detector and in the depleted volume, the diffusion of free carriers from the undepleted volume towards the depletion region and the tunneling of carriers between states in the energy bandgap. The first two are the dominant contributions, while the latter usually plays a crucial role at cryogenic temperatures. The generation of charge carriers in the depleted volume is directly proportional to the volume of the depleted region and, for this reason, it is called *volume current*. In particular, considering the case of a junction with $N_A > N_D$, as discussed in 1.2.2, one has:

$$J_{vol} \sim e \frac{n_i}{\tau_g} d \sim e \frac{n_i}{\tau_g} \sqrt{\frac{2\epsilon V}{eN_D}} \quad (1.12)$$

where τ_g is the carrier generation lifetime³[10]. The temperature dependence is implicitly included in the intrinsic carriers concentration n_i :

$$n_i \propto T^{3/2} e^{\frac{-E_g}{2k_B T}}. \quad (1.13)$$

and therefore [11],

$$J_{vol} \propto T^2 e^{\frac{-E_g}{2k_B T}}. \quad (1.14)$$

This equation brings to the classical rule of thumb: the leakage current increases by a factor 2 every 7 degrees [12].

1.3 Energy deposition in silicon

In the following section, an overview of the energy deposition mechanisms relevant for this work will be described: energy loss of charged particles and photons absorption.

³ $\tau_g = \frac{1}{\sigma v_{th} N_t}$, with σ charge carrier cross-section ($\sim 10^{-15}$ cm²), v_{th} thermal velocity ($\sim 10^7$ cm/s) and N_t impurity-trap concentration

1.3.1 Charged particle interaction with matter

Particles crossing matter interact with the electrons and/or nuclei of the medium. This interaction can be weak, electromagnetic or strong, depending on the kind of particle and its effects can be exploited to detect it. In particular, the energy lost by the particle is converted into an electrical signal that can be exploited to measure the various observables of interest (position, energy, momentum etc).

In a material, a particle heavier than electron can collide with nuclei or atomic electrons. In the first case, a small amount of energy is transferred to the nucleus, while the particle undergoes a significative scattering. In the second case, the incident particle loses its energy on electrons, with a minimal deviation. The main way heavy charged particles (anything but e^-) lose energy when interacting with matter is through ionization. The mean rate of energy loss is given by the *Bethe-Bloch* formula for the *linear stopping power*:

$$\left\langle -\frac{dE}{dx} \right\rangle = K \frac{z^2}{\beta^2} \rho \frac{Z}{A} \left[\frac{1}{2} \ln \frac{2m_e c^2 \beta^2 \gamma^2 W_{\max}}{I^2} - \beta^2 - \frac{\delta(\beta\gamma)}{2} - \frac{C}{Z} \right] \quad (1.15)$$

In the formula: K is a constant value, independent from both the particle and the target, $K = 4\pi r_0^2 m_e c^2 N_{\text{Av}}$, with $r_0 = \frac{1}{4\pi\epsilon_0} \frac{e^2}{m_e c^2} = 2.8$ fm the electron classical radius and N_{Av} the Avogadro constant. β is the particle velocity in units of speed of light c , z is the particle charge in terms of unit charge, Z is the atomic number of the target material (14 for silicon), ρ and A the density and the atomic mass of the material, γ is the Lorentz factor $1/\sqrt{1-\beta^2}$, I is the mean excitation energy, $W_{\max} = \frac{2m_e c^2 \beta^2 \gamma^2}{1+2\gamma m_e/M+(m_e/M)^2}$ is the maximum energy transfer to an electron in a single collision. δ represents density effects correction and C a shell correction. In particular, $-\delta/2$ is a polarisation term that takes into account that the field polarises the medium and is characterized by a logarithmic dependence $\delta \sim 2\ln(\beta\gamma)$. The last term in square brackets is a shielding term exercised by more external electrons to more internal ones.

The quantity $-dE/dx$ is called *linear stopping power* and is measured in MeV/cm; however, it is quite common to compute the average differential energy loss per mass density, allowing to compare materials with different mass density:

$$\frac{dE}{d\tilde{x}} = \frac{1}{\rho} \frac{dE}{dx} \quad (1.16)$$

which is called *mass stopping power* and is expressed in $\frac{\text{MeV}}{\text{g/cm}^2}$. Eq. (1.15) is valid

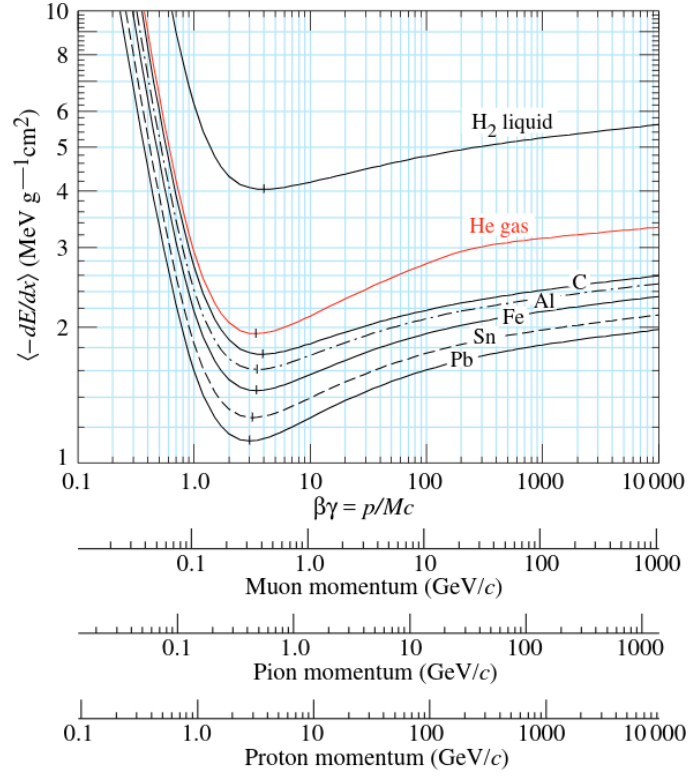


Fig. 1.2 Mean energy loss in liquid hydrogen, gaseous helium, carbon, aluminum, iron, tin, and lead. Radiative effects, relevant for muons and pions, are not included. Image source [13].

in the region $0.1 \leq \beta\gamma \leq 1000$ with an accuracy of a few percent. At $\beta\gamma \sim 0.1$ the projectile speed is comparable to atomic electron and at $\beta\gamma \sim 1000$ radiative effects begin to be important [13]. The mass stopping power in several materials is shown in Fig. 1.2. Except for hydrogen, particles with the same speed have similar energy loss in different materials, but it's possible to see a small decrease in the rate of energy loss with increasing Z of the material. Different regions of the *Bethe-Bloch* formula can be identified.

At non-relativistic energies, dE/dx is dominated by the factor $1/\beta^2$ and decreases with increasing velocity until a broad minimum is reached for $\beta \sim 0.96$ or $\beta\gamma \sim 3.5$ to 3 as Z goes from 7 to 100. The values of minimum ionization as a function of the material atomic number Z are shown in Fig. 1.3. Particles at the minimum dE/dx value are referred to as *Minimum Ionising Particles (MIPs)*. In practical cases, most relativistic particles (e.g., cosmic-ray muons or 120 GeV pions, as the ones that are used in this work to characterise the silicon detectors) can be considered MIPs. For

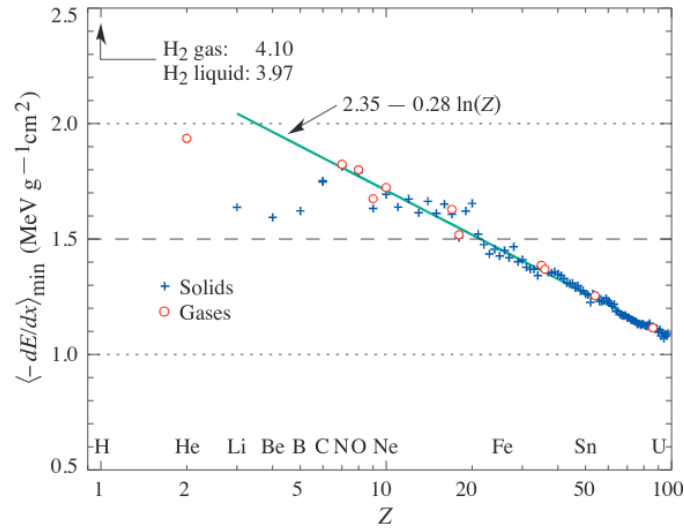


Fig. 1.3 Minimum of mass stopping power curve for different materials. Image source [13].

the specific case of silicon, the minimum energy loss normalised to the density of the traversed material is around $1.66 \frac{\text{MeV}}{\text{g/cm}^2}$ [13], corresponding to $\sim 3.8 \text{ MeV/cm}$. At larger energies, dE/dx rises again due to the logarithmic dependence of Eq. (1.15).

Energy loss fluctuations

For relativistic particles in silicon, the average distance between primary interactions is $\lambda = 0.212 \mu\text{m}$ [14]. One should remember that the loss of energy process is stochastic, as the number of collisions and the energy lost in every collision are not known a priori. In other words, the amount of energy lost by a particle is subject to statistical fluctuations. The probability density function of the energy loss (straggling function) depends on the thickness of the absorbing medium [8]: for sufficiently thick layers, in which the number of collisions is large, the energy loss probability density function is well described by the skewed Landau or Landau-Vavilov distribution [15]. While the stopping power expressed by Eq. 1.15 is independent of the thickness x , the most probable energy loss Δ_p scales as $x(a + \ln x)$ [16] and reaches a plateau, called Fermi plateau, for $\beta\gamma \geq 100$. The Landau distribution shows a Gaussian core and a long upper tail due to rare, but highly ionizing knock-on electrons or *delta rays*: secondary electrons with enough energy to further ionise, creating additional e-h pairs along their track, resulting in a large fraction of absorbed energy. It is important to keep in mind that the *Most Probable Value* (MPV) and the average value of the

distribution do not coincide. In particular, the former is significantly lower than the latter. Indeed, it is because of the very rare high-energy-transfer collisions, that the mean of the distribution is placed into the tail.

Very thin absorbers

For very thin sensor layers ($\leq 300 \mu\text{m}$ for silicon), as the ones presented in this thesis, the Landau model fails to describe the energy loss accurately. In fact, the ionisation energy loss fluctuations in very thin silicon sensors significantly deviate from the Landau distribution [17].

For thin sensors, the Bichsel straggling function better reproduces measured energy losses [16]. Both the ionisation (i.e. the number of e-h pairs produced in the detector) and the total energy loss of the particle are stochastic quantities and their probability density functions are called *straggling functions*. Tab. 1.1 reports the most probable

$t(\mu\text{m})$	$\Delta_p(\text{keV})$	r_p	$\Delta_p/t(\text{eV}/\mu\text{m})$	pairs/t
10	1.857	0.844	186	51
20	4.120	0.886	206	56
40	9.282	0.948	232	63
80	20.39	0.991	255	69
160	43.38	1.006	272	74
320	90.96	1.008	285	77
640	189.4	1.006	296	80
1280	393.2	1.002	307	83
2560	815.5	0.999	319	87

Table 1.1 Values of the most probable energy loss Δ_p of the energy-loss straggling functions $f(\Delta)$ as a function of thickness t of a silicon absorber for particles with $\beta\gamma > 500$. Ratio r_p of the Δ_p to the values of ${}_L\Delta_p$ computed with the Landau theory. Ratio Δ_p/t (eV/ μm) and ratio pairs/t. Data from [16].

energy loss for different sensor thicknesses by using the Bichsel functions and comparing it with the Landau model for $\beta\gamma \geq 500$. Fig. 1.4a shows the straggling functions in silicon for 500 MeV pions incident on thin silicon detectors. Fig. 1.4b displays the most probable energy loss scaled to the mean loss of a MIP, 388 eV/ μm , as a function of $\beta\gamma$.

Another model that is used to describe thin silicon devices is the Photoabsorption Ionization model (PAI) [18][14]. Fig. 1.5 shows the distributions of the number of e-h pairs deposited in a thickness of 50 μm (in blue) and 200 μm (in orange) of

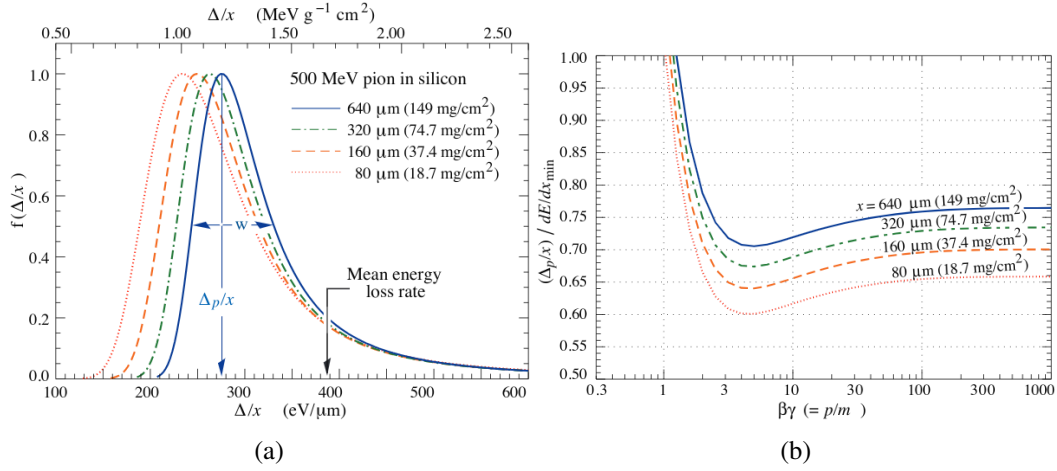


Fig. 1.4 Straggling functions in silicon for 500 MeV pions, normalised to unity at the most probable value. The width w is the full width at half maximum. Image source [13] (a). Most probable energy loss, scaled to the mean loss of a MIP, $388 \text{ eV}/\mu\text{m}$, as a function of $\beta\gamma$. Image source [13] (b).

silicon. The histograms show the results obtained with the PAI model, while the superimposed solid lines represent the Landau theory. Generally, the most probable number of e-h pairs from the Landau theory is underestimated with respect to the one from the PAI model and is given by:

$$n_{MP} \sim \frac{n_0 d}{\lambda} \left(0.2 + \ln \frac{d}{\lambda} \right) \quad (1.17)$$

where d is the silicon sensor thickness and $n_0 \sim 2.2$ electrons is a cutoff value of the cluster size distribution [14]. Eq. (1.17) leads to $n_{MP} \sim 2940$ e-h pairs, compared to $n_{MP} \sim 3160$ for PAI model in a $50 \mu\text{m}$ thick sensor (within 10% of the value from the Landau theory).

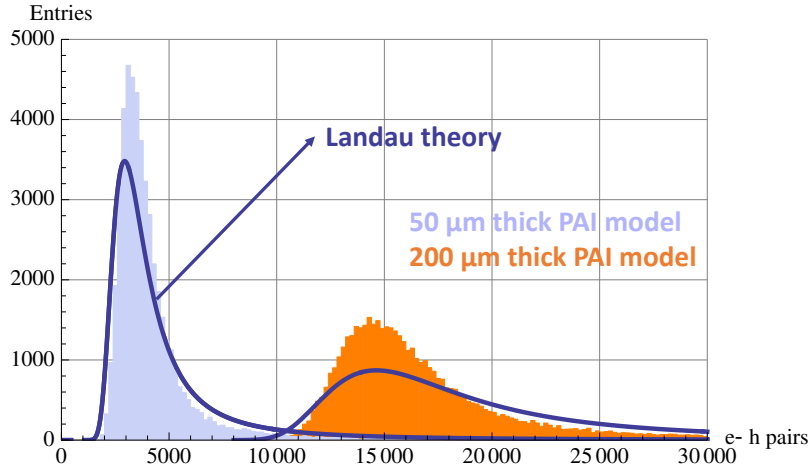


Fig. 1.5 Histograms showing the number of e-h pairs obtained with the PAI model for two sensor thicknesses with superimposed Landau theory (solid line). Image source [14].

1.3.2 Photon interaction with matter

Unlike charged particles, photon interaction with matter is governed by three main processes: photoelectric effect, Compton scattering and pair production. When photons cross matter their intensity is attenuated according to:

$$I(x) = I(0)e^{-\mu x} \quad (1.18)$$

where μ is the *absorption coefficient* defined as:

$$\mu = \sigma N_{Av} \rho / A \quad (1.19)$$

with ρ the specific mass of the medium, A the atomic weight, σ the total cross section. The photon *mean free path* is $\lambda = 1/\mu$.

Photoelectric effect, also known as photoelectric absorption, happens when the incoming photon is absorbed. All its energy is transferred to an atomic electron, which is ejected, as a consequence, from the atom and creates e-h pairs along its trajectory: $\gamma e^- \rightarrow e^-$. The energy of the outgoing electron is given by $E_e = h\nu - h\nu_0$, where $h\nu_0$ represents the binding energy of the electron.

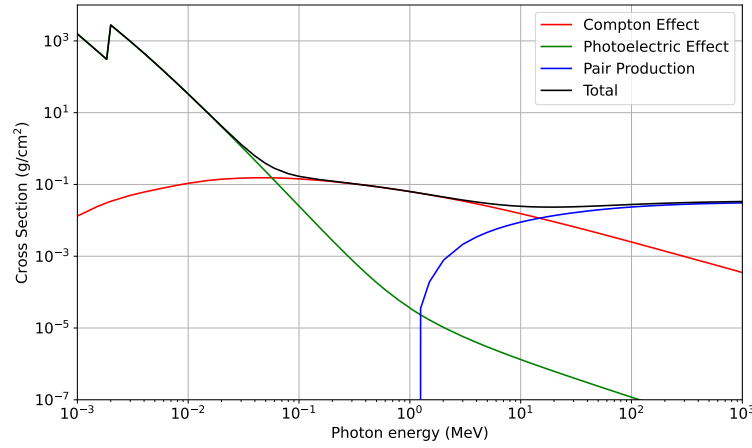


Fig. 1.6 Cross sections as a function of the photon energy in silicon [19].

Compton effect is an elastic collision occurring between a photon and an electron: $\gamma e^- \rightarrow \gamma e^-$. Atomic electrons are bounded electrons and if the incoming photon has an energy much higher than the electron binding energy, after the interaction, the electron can be considered as a free carrier.

Pair production is a process in which the incoming photon interacts with the electric field of a nucleus of a silicon atom and converts into an e^+e^- pair: $\gamma + Z \rightarrow Z + e^+ + e^-$, where Z is a generic atomic nucleus. The process has a threshold of $2m_e c^2 = 1.022$ MeV and therefore it occurs only at energies higher than this value.

Figure 1.6 points out the cross sections of the three described mechanisms of photon interaction with silicon, indicating in which energy range they are dominant. For photons energy below 10 keV, the interaction is governed by the Photoelectric effect. For energies in the range between 10 keV and 10 MeV, the Compton effect plays a major role and for energies higher than 10 MeV, the pair production becomes the prevalent phenomenon.

X-rays from ^{55}Fe

X rays are a frequent choice to characterise silicon detectors [20]. In particular, in this work, an ^{55}Fe source has been employed, which decays by electron capture to

^{55}Mn with an half-life of 2.737 years, represented by the following nuclear equation:



During the process, the hole left by the captured electron is filled by another electron from a more external shell. The difference between the two energy levels can bring to different processes: the emission of Auger electrons (e_A), emission of X-rays (X) and emission of γ -rays. Table 1.2 reports the details about the different emissions, their energy range and the probability computed per 100 disintegrations [21]. Both the Auger electrons and the γ -rays emissions are negligible for the purpose of this work and the only detected contribution comes from the X-rays. The $K_{\alpha 1}$ and $K_{\alpha 2}$ are often considered together as a single photon with 5.9 keV energy, as they are pretty similar. From the considerations done in Sec. 1.3.2, the interaction between such photons and silicon is mainly governed by the photoelectric effect (see Fig. 1.6). It is therefore the electron emitted from this process to be responsible for the generation of e-h pairs in the detector material. Keeping in mind that the range of an electron with an energy around 5-6 keV is lower than $1 \mu\text{m}$ [22], the charges will be generated in a very compact region of the detector volume. Remembering the mean energy of 3.6 eV required to generate an e-h pair in silicon, 5.9 and 6.5 keV photons will generate on average ~ 1640 and 1800 e-h pairs respectively.

Emission	Energy (keV)	Emissions per 100 disint.
e_{AL}	0.47 - 0.67	140.2
e_{AK}	4.95 - 6.53	60.1
XL	0.56 - 0.72	0.52
$XK_{\alpha 2}$	5.888	8.45
$XK_{\alpha 1}$	5.899	16.57
$XK_{\beta 1}$	6.490	3.40
$XK_{\beta 2}$	6.535	
γ	125.949	1.3×10^{-7}

Table 1.2 Emissions of electrons, X-rays and γ -rays from ^{55}Fe decay, per 100 disintegrations of the parent nuclide [21].

1.4 Signals in particle detectors

Signals in particle detectors are due to the motion of charge carriers generated by the impinging particles and the Ramo–Shockley theorem provides the basis for calculating the induced current signal, as it will be described in Sec. 1.4.2. The output pulse begins immediately after the carriers have started their motion to the collection diodes. Once the last carrier reaches its collecting electrode, the process of charge induction ends and the pulse is fully developed [23]. The time evolution of the signal is a relevant point to understand the timing properties of detectors and to observe effects due to the different particle impinging position on the sensor surface, as it will be explained more in more detail in Sec. 2.1.

1.4.1 Charge carriers motion

After the carrier pairs have been generated, they will start to move according to two different possible mechanisms: *diffusion* or *drift*. In the first case, the motion is due to a non-uniform concentration of charges in silicon or, in other words, to the existence of a gradient in the carrier concentration. As a consequence, charges move from the region with a higher to the one with a lower concentration. The diffusion mechanism obeys Fick's law [24], relating the diffusing physical quantity with the spatial derivative of its concentration. Let consider, for example, the case in which the density of electrons grows with increasing distance x in the sample and let us indicate $\nabla n = \frac{dn}{dx}$. The current density for electrons and holes has the following shape:

$$\mathbf{J}_n = qD_n \vec{\nabla} n \quad (1.21)$$

$$\mathbf{J}_p = qD_p \vec{\nabla} p \quad (1.22)$$

where n and p are the carrier concentrations and $D_{n/p}$ represents the diffusion constant of electrons/holes. It can be related to the mobility using Einstein relation:

$$D_{n/p} = \frac{k_B T}{q} \cdot \mu_{n/p} \quad (1.23)$$

where k_B is the Boltzmann constant, T is the absolute temperature and $\mu_{n/p}$ is the mobility of electrons (n) or holes (p).

On the other hand, the drift current is caused by the presence of electric fields and, as

a consequence, charges move following the field line directions. The current density is given by:

$$\mathbf{J} = \mathbf{J}_n + \mathbf{J}_p = nq\mathbf{v}_{n \text{ drift}} + pq\mathbf{v}_{p \text{ drift}} = (nq\mu_n + pq\mu_p)\mathbf{E} = \sigma\mathbf{E} \quad (1.24)$$

where $\mathbf{E}$ is the applied electric field. The *mobility* is linked to the drift velocity and the electric field magnitude by the relation:

$$\mathbf{v}_{\text{drift}} = \mu\mathbf{E}. \quad (1.25)$$

For a given material, the mobility is a function of $\mathbf{E}$ and the temperature⁴. For silicon at normal temperatures, the mobility is constant for $E < 10^3$ V/cm and the relation between velocity and $\mathbf{E}$ is linear. For 10^3 V/cm $< E < 10^4$ V/cm, μ varies as $E^{-1/2}$, while above 10^4 V/cm, μ goes as $1/E$, causing velocity saturation at a value about 10^7 cm/s [8]. The quantity $\sigma = (nq\mathbf{v}_{n \text{ drift}} + pq\mathbf{v}_{p \text{ drift}})$ is called *conductivity* and is the reciprocal of the resistivity ρ .

At this point, the two effects of drift and diffusion can be put together in the same mathematical relationship, the *Drift and Diffusion equations*, which express the total electron and hole current densities. In the three-dimensional case, one has:

$$\mathbf{J}_n = qn\mu_n\mathbf{E} + qD_n\vec{\nabla}n \quad (1.26)$$

$$\mathbf{J}_p = qp\mu_p\mathbf{E} - qD_p\vec{\nabla}p \quad (1.27)$$

1.4.2 The signal induction

In every particle detector, the induced current signal is provided by the Ramo–Shockley theorem [26][27]. The current induced on a grounded conducting electrode by a point charge q moving along a trajectory $\mathbf{x}(t)$, as illustrated in Fig. 1.7, can be computed in the following way: one removes the charge q from the setup, puts the electrode to voltage V_w , while keeping all other electrodes grounded. This will result in an electric field, the *weighting field*, in the volume between the electrodes [28]. At this

⁴The mobility decreases as temperature increases due to scattering with phonons [25].

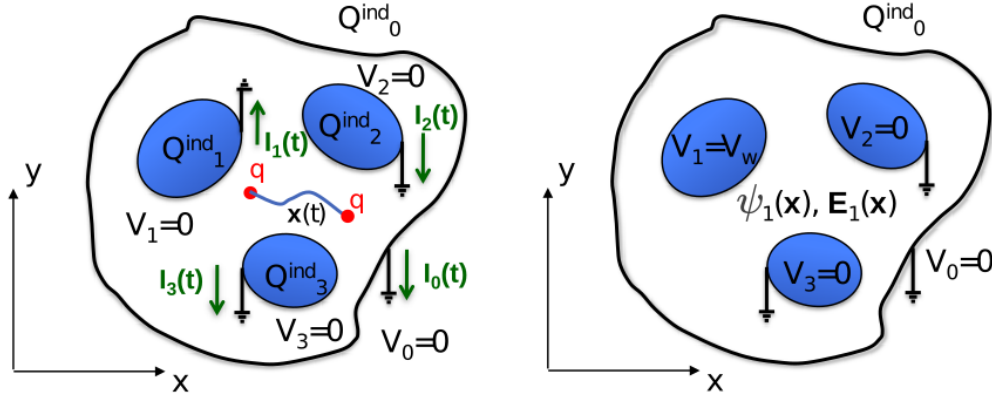


Fig. 1.7 Illustration of signal induction by a moving charge q on the electrode 1. Image source [28].

point, the instantaneous current induced on a given electrode n is equal to:

$$I_n^{ind}(t) = -\frac{dQ_n^{ind}(\mathbf{x}(t))}{dt} = \frac{q}{V_w} \nabla \psi_n(\mathbf{x}(t)) \dot{\mathbf{x}}(t) = -\frac{q}{V_w} \mathbf{E}_n(\mathbf{x}(t)) \cdot \vec{v}_{drift} \quad (1.28)$$

where $\mathbf{E}_n(\mathbf{x}(t))$ is the weighting field, given by $\mathbf{E}_n(\mathbf{x}) = -\nabla \psi_n(\mathbf{x})$ and $\psi_n(\mathbf{x})$ is the *weighting potential*.

Let's now consider the situation in which the point charge q is moving from $x_0 = x(t_0)$ to $x_1 = x(t_1)$. The total charge flowing between the electrode n and ground is independent of the path between x_0 and x_1 :

$$Q_n = \int_{t_0}^{t_1} I_n^{ind}(t) dt = -\frac{q}{V_w} \int_{t_0}^{t_1} \mathbf{E}_n(\mathbf{x}(t)) \dot{\mathbf{x}}(t) dt = \frac{q}{V_w} [\psi_n(\mathbf{x}_1) - \psi_n(\mathbf{x}_0)] \quad (1.29)$$

The induced charge on the electrode n is therefore given by the product of the carrier charge multiplied by the difference of the weighting potential at the beginning and at the end of the carrier path [23]. The weighting potential is not a real electric potential in the detector, but it represents a quantity that describes the coupling of the charge to a specific electrode and allows to compute the induced charge on the electrode of interest. Current signals on electrodes that don't collect any charge are therefore bipolar. From the above statement, it's possible to get the fundamental link between the observed signal and the induction process by the moving charges. Once the charge has actually arrived at the electrode, the signal is already concluded.

Chapter 2

Timing and tracking principles

In the near future, CERN will undertake a major upgrade called High Luminosity LHC (HL-LHC) [29], where the number of events per bunch crossing will be around 150-200, allowing the experiments to collect higher amounts of data. In this environment, it will become difficult to associate the detected particle with the parent collision, causing a degradation in the precision of the reconstruction process. To improve the event reconstruction, the timing information associated with each track could be exploited. This can be achieved by combining the data from the tracker with the information from a timing layer featuring an adequate time resolution. In this chapter, an overview of the general timing and tracking principles will be provided, together with an insight into the foreseen upgrades of the ALICE experiment at LHC, in which this work was conducted.

2.1 Time resolution of silicon detectors

In general, the term time resolution refers to the Least Significant Bit (LSB) in a time measuring circuit or device. As a result, any variation in a time interval that is shorter than the time resolution may not be detected, and two events occurring with a time distance shorter than the time resolution may not be distinguished time-wise. In particle physics applications, the time at which the particle crosses the detector has to be determined by the readout electronics. This has to be fed with an input signal induced on the sensing electrodes by the charge carriers' movement inside silicon, as described in 1.4.2. The recent increase in experiment event rate

capabilities resulted in the need for more and more sophisticated and accurate time measurements, requiring very short-duration signals. This allows the detection of particles from events happening within the time window of one beam crossing. Several effects play a role in time resolution, but the most significant components for a particle detection system, including the sensor and the read-out electronics, can be grouped in the following way [6][30]:

$$\sigma_t^2 = \sigma_{\text{Landau Noise}}^2 + \sigma_{\text{Time Walk}}^2 + \sigma_{\text{Distortion}}^2 + \sigma_{\text{Jitter}}^2 + \sigma_{\text{TDC}}^2 \quad (2.1)$$

In the following, the different elements will be briefly introduced.

Landau Noise

The Landau noise term is a fundamental limit due to the energy deposition process. It concerns the non-uniform energy deposition by the impinging charged particle and the fact that the number of e-h pairs can be different in every event. This effect can cause irregularity in the signal shape (Landau noise) and can also produce a difference in the total signal amplitude (leading to the time-walk effect), worsening the time resolution. A possible solution to overcome this effect is to employ thin sensors, in order to be less sensitive to signal fluctuations.

Time walk or time slewing

The *time walk* effect, also called *time slewing*, is caused by variations in the amplitude or rise time of different signals, leading to a difference in the time of threshold crossing, when applying a fixed threshold voltage V_{th} . In particular, signals with a larger amplitude cross the threshold earlier than smaller ones, as it's possible to see in Fig. 2.1a. In other words, with a leading edge discriminator (i.e. fixed applied threshold), smaller pulses result in a delayed discriminator output with respect to larger ones. Time walk can be expressed mathematically [6]:

$$\sigma_{\text{time walk}} = \left[\frac{V_{th}}{S/t_{rise}} \right]_{RMS} \quad (2.2)$$

in which S is the signal amplitude and t_{rise} is the signal rise time. It is therefore immediate to conclude that increasing the steepness of the signal (S/t_{rise}) can lower

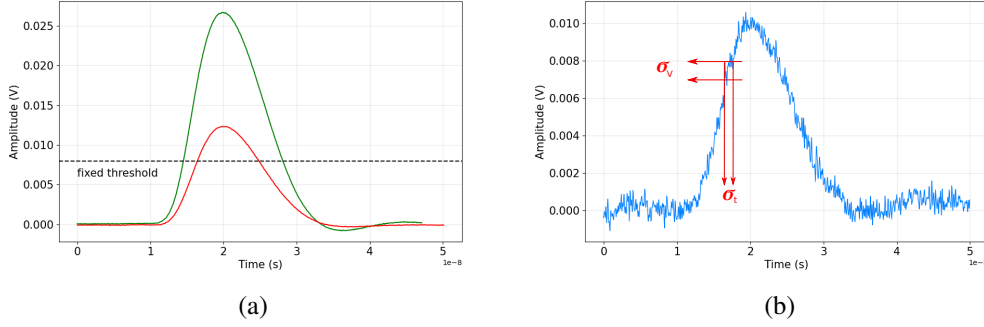


Fig. 2.1 Waveforms with different amplitudes showing the time-walk effect: the two waveforms cross the fixed threshold at different times, resulting in a delay in the time of arrival (a). Visualisation of the jitter effect on a waveform (b).

the time walk contribution. A secondary cause of time walk is given by the finite amount of charge needed to trigger the discriminator and the fact that a certain amount of charge must be integrated on a capacitor before producing a logic signal [8]. Among the different existing correction techniques to cope with this effect, one of the best known is the Constant Fraction Discriminator (CFD), which triggers at a fixed fraction of the input signal's amplitude. However, it has to be remarked that the CFD technique only suppresses time walk in case of a constant signal shape [7] [31].

Distortion

The distortion component is the effect caused by the non-uniformity of the weighting potential and the non-saturated drift velocity of charge carriers. The induced current signal can be computed as described in Eq. 1.28, clearly stating that the current induced by a charge carrier is proportional to its electric charge q , the drift velocity and the weighting field. In order to improve the sensor timing performance, some optimisations in the sensor design have to be considered. Focusing on the drift velocity and using the approximation for the velocity of the electrons and holes from the Canali model [32], one has for electrons and holes respectively:

$$v_e(E) = \frac{\mu_e E}{\left[1 + \left(\frac{\mu_e E}{v_{sat}^e}\right)^{\beta_e}\right]^{1/\beta_e}} \quad v_h(E) = \frac{\mu_h E}{\left[1 + \left(\frac{\mu_h E}{v_{sat}^h}\right)^{\beta_h}\right]^{1/\beta_h}} \quad (2.3)$$

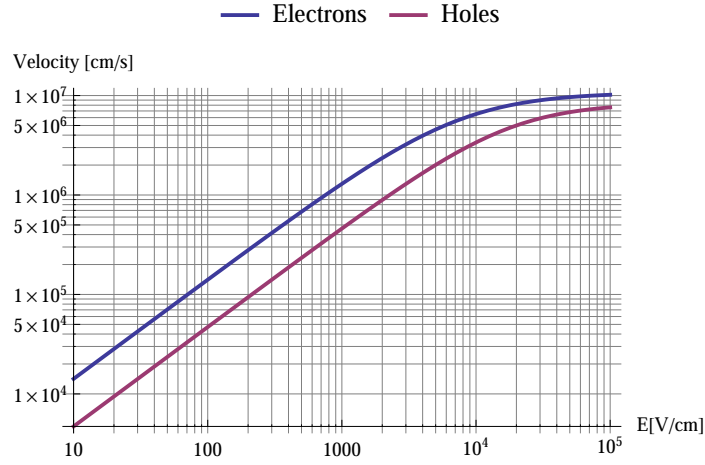


Fig. 2.2 Drift velocity of electrons and holes as a function of electric field. Image source [14].

where setting $\mu_e = 1417 \text{ cm}^2/(\text{Vs})$, $\mu_h = 471 \text{ cm}^2/(\text{Vs})$, $\beta_e = 1.109$, $\beta_h = 1.213$ and $v_{sat}^e = 1.07 \times 10^7 \text{ cm/s}$ and $v_{sat}^h = 0.837 \times 10^7 \text{ cm/s}$ at 300 K, the trend of the drift velocity as a function of the applied electric field can be obtained, as shown in Fig. 2.2 [14]. A key consideration is that to reach a good time resolution, an electric field high enough has to be generated at room temperature, to be sure to enter the drift velocity saturation regime. The easiest way to obtain uniform drift velocity is to have an electric field high enough everywhere in the active volume of the sensor, allowing the carriers to move always with saturated drift velocity [6]. Another crucial aspect regards the weighting potential, which enters into the computation of the induced current. To improve the time performance of a detector, it should not depend on the impinging position of the particle and, therefore, it has to be as uniform as possible along the pixel pitch. For these reasons, some geometrical optimisations have to be carried out, to generate a smooth electric and weighting field. Using the *Ramo-Schockley* theorem, it's possible to make an important observation on the maximum current from a simple pad-detector of thickness d [6]:

$$I_{max} \propto Nq \frac{1}{d} v_{\text{drift,sat}} = n_{e-h} q v_{\text{drift,sat}} \quad (2.4)$$

where $v_{\text{drift,sat}}$ indicates the saturated drift velocity and the weighting field has been approximated as $\propto 1/d$ for a simple pad geometry. From the above equation, it's clear to see the independence between the peak current and the thickness of the sensor.

Jitter

Jitter can be defined as the time uncertainty due to statistical fluctuations in the original detector signal or to the presence of noise from the electronics. The effect of jitter on a waveform can be observed in Fig. 2.1b. Many systems include a non-negligible level of electronic noise, producing uncertainty in the discriminator threshold crossing time of the analogue pulse. This crossing time will be randomly distributed around an average value and the sigma of the distribution of the comparator flipping times is related to the one of the noise affecting the input signal [7]. If one considers σ_V as the sigma of the noise affecting the analogue pulse and dV/dt as the slope of the signal when it crosses the discriminator threshold (i.e. the *slew rate*), the jitter can be defined as:

$$\sigma_{\text{jitter}} = \frac{\sigma_V}{dV/dt} \sim \frac{t_{\text{rise}}}{S/\sigma_V} \quad (2.5)$$

where in the last part of the equation, a linear input signal approximation has been considered with amplitude S and rise time t_{rise} . From (2.5) it's possible to state that to reduce the jitter component, one has to preserve the fastest possible rise of the signal. Keeping the noise and t_{rise} fixed, the jitter can be reduced with increasing signal amplitude.

TDC

The TDC (time-to-digital converter) term refers to the uncertainty associated with the digitization of the measured time. TDC digitizes the time information and records it in a time bin with a finite size. The TDC component is not linked to the sensor characteristics and it can be properly minimised from the electronic design [6].

2.2 Tracking with silicon detectors

Among the main challenging goals of silicon detectors in collider experiments there is the precise reconstruction of the particles' trajectories in the vicinity of the beam collision point. This is needed to reconstruct the charged particle tracks, determine the particles' decay vertices and study specific physics processes in HEP [33]. After the beam crossing, primary particles are produced and they decay so close to the

interaction point that the first tracking layer is still not reached. What is measured by the detector, in this case, are the hits due to the primary particles' decay, i.e. the secondary particles, whose tracks create a vertex displaced from the primary collision point. One aims at distinguishing the decay vertices of secondary particles from the primary vertex, in order to retrieve the desired information on the primary particle by reconstructing the trajectories of the secondaries. The vertex detector is the closest tracking system to the beam and it has to provide very precise position and direction information of the tracks produced in a collision, to detect them with large efficiency [34]. This detector has, as a consequence, the largest precision (smallest measurement errors) of all tracking systems. Vertex detectors are typically equipped with pixel sensors to achieve the required spatial resolution. A key parameter in this context is the particle's decay length:

$$\lambda_d = \beta c \tau_0 \gamma \quad (2.6)$$

where βc is the particle's velocity, τ_0 its mean lifetime and γ the Lorentz factor. It is necessary to reach a track resolution close to the interaction point smaller than the decay lengths of the particles to be measured [35]. For example, the Λ_c charm baryon has a decay length of only $60 \mu\text{m}$ and the D^0 meson $\sim 123 \mu\text{m}$. Moreover, since multiple interactions happen within a single bunch crossing (interactions pile-up), the vertex reconstruction is needed to discover which tracks originate from a given interaction or process.

2.2.1 Charged particle tracks position resolution

The main figure of merit to quantify the position resolution of a detector is the accuracy on the impact parameter d , defined as the distance of closest approach of the particle track to the beam collision position [33]. This accuracy, representing the pointing resolution, can be parametrised as:

$$\sigma_d^2 = \sigma_{\text{sp}}^2 + \sigma_{\text{ms}}^2 \quad (2.7)$$

where σ_{sp}^2 is the resolution of the geometrical reconstruction from the measured hits on the detector layers to the interaction point and σ_{ms}^2 is the uncertainty due to Coulomb multiple scattering. Considering the simple situation depicted in Fig. 2.3

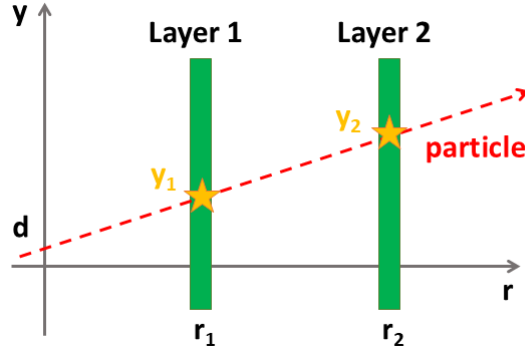


Fig. 2.3 Simple example of a tracking system with two detector layers.

with only two layers, the inner one at radius r_1 and the outer at radius r_2 , with a spatial resolution σ_1 and σ_2 , one can write d as:

$$d = \frac{y_2 - y_1}{r_2 - r_1} r + \frac{r_2 y_1 - r_1 y_2}{r_2 - r_1} \quad (2.8)$$

and considering $r = 0$ and r_1 and r_2 fixed, one can compute the spatial uncertainty σ_{sp} as [9]:

$$\sigma_{sp} = \sqrt{\left(\frac{r_2}{r_2 - r_1} \sigma_1\right)^2 + \left(\frac{r_1}{r_2 - r_1} \sigma_2\right)^2} \quad (2.9)$$

in which the position resolution at the inner radius is weighted by the outer radius, meaning that having a good spatial resolution at the inner radius is fundamental to end up with an accurate spatial resolution. If the two layers have an equal resolution σ , Eq. 2.9, can be rewritten as:

$$\sigma_{sp} = \sigma \sqrt{\left(\frac{1}{1 - r_1/r_2}\right)^2 + \left(\frac{1}{r_2/r_1 - 1}\right)^2}. \quad (2.10)$$

The above equation clearly indicates the relevance of the r_2/r_1 term, which has to be kept as high as possible to have a system with sufficiently small spatial resolution. As a consequence, it is desirable to measure the first hit position the closest possible to the interaction point.

As anticipated before, the σ_{ms}^2 term represents the uncertainty due to Coulomb multiple scattering¹, occurring in the beam pipe and the detector layers. Indeed, a

¹For hadronic projectiles, the strong interactions also contribute to multiple scattering.

charged particle traversing a medium undergoes deflections by many small-angle scatters and the total angular displacement of the particle direction can be modelled as a Gaussian distribution with rms θ_{RMS} [13]:

$$\theta_{RMS} = \frac{13.6\text{MeV}}{\beta c p} z \sqrt{\frac{x}{X_0}} \left[1 + 0.038 \ln \left(\frac{x z^2}{X_0 \beta^2} \right) \right] \quad (2.11)$$

where p , βc and z are the momentum, velocity and charge number of the incident particle and (x/X_0) is the thickness of the material in terms of radiation length X_0 . It's easy to understand that any material between the interaction and the detection point should be minimised and the first measurement should be performed at a radius as small as possible. The multiple scattering effect on the whole spatial resolution can be written as [33] $\sigma_{ms}^2 \propto r_1 \sqrt{x/X_0}/p$. In conclusion, to improve the pointing resolution it's essential to reduce the inner radius r_1 and the material budget (x/X_0) .

2.3 The ALICE experiment at LHC

ALICE [36] is an experiment located at the CERN Large Hadron Collider (LHC) dedicated to heavy-ion physics. It has been designed to investigate the properties of strongly interacting matter at extreme energy densities, where a deconfined phase of matter called *quark-gluon plasma* (QGP) forms, using proton–proton, proton–nucleus and nucleus–nucleus collisions.

ALICE's purpose is to recreate in the laboratory similar conditions to the ones immediately after the Big Bang, a few microseconds after the formation of the early Universe. In these extreme conditions, protons and neutrons "melt" and their components, the quarks, are no longer bound with the gluons. During the ongoing Run 3 (2022–2025), ALICE is studying Pb–Pb collisions up to an energy of $\sqrt{s_{NN}} = 5.36$ TeV and proton-proton (pp) collision up to $\sqrt{s} = 13.6$ TeV. In heavy-ion collisions at ultra-relativistic energies, the nuclear matter is heated and brought to temperature and density conditions well beyond those required for the formation of QGP and the same kind of medium that filled the very early Universe is generated for a fleeting instant. In general, during a heavy-ion collision, a short-lived, non-spherical hot *fireball* is created [37], whose dimensions and shape depend on the collision's centrality.

The goal is to study the QGP properties with this state of strongly-interacting matter,

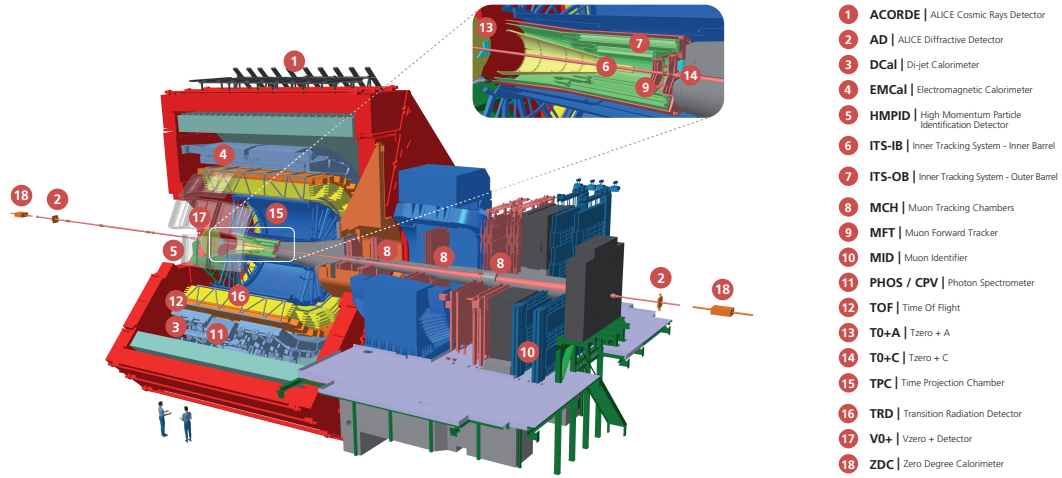


Fig. 2.4 The current ALICE detector at the CERN LHC during Run 3, 2022-2025.

completely different from the hadronic one we ordinarily find around us. The QGP is studied while it expands and cools down, observing how it progressively gives rise to the particles constituting the matter of today's universe. A picture of the current ALICE detector is shown in Fig. 2.4, in which all the components are highlighted. In particular, the Inner Tracking System 2 (ITS2) is devoted to tracking and the Time Of Flight (TOF) detector handles timing measurements.

The second generation Inner Tracking System (ITS2)

The ITS2 is the innermost detector surrounding the beampipe and it was installed during the LHC Long Shutdown 2 (LS2) in 2019-2021. The upgrade allowed ALICE to collect a large data sample at 50 kHz Pb–Pb collision rate during the ongoing Run 3 and to reach an increased vertexing capabilities, while maintaining the previous particle identification performance [38]. The ITS2 is the first large-area ($\sim 10 \text{ m}^2$) silicon tracker based on the CMOS MAPS technology operating at a collider (12.5×10^9 pixels). It is composed of seven cylindrical layers of MAPS called ALPIDE [39] [40] and the impact parameter resolution has been improved thanks to three main modifications with respect to the previous ITS, in agreement with considerations made in 2.2.1:

- the innermost detector layer was approached to the interaction point from 39 mm distance to 23 mm;

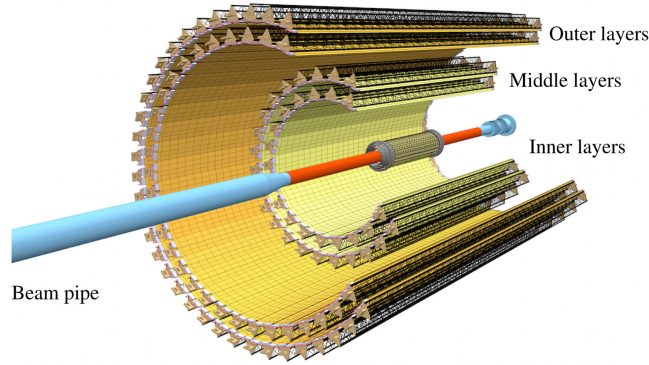


Fig. 2.5 ALICE ITS2 detector layout.

- the material budget of the inner layers has been reduced to 0.35% X_0 compared to 1.14% X_0 of the previous one;
- the pixel size has been reduced from $50 \mu\text{m} \times 425 \mu\text{m}$ to $29.24 \mu\text{m} \times 26.88 \mu\text{m}$.

The detector, represented in Fig. 2.5 is composed of an Inner Barrel (IB) with three inner layers and an Outer Barrel (OB) with four layers. This latter can be further divided into two middle layers and two outer layers.

The Time Of Flight (TOF)

The TOF detector measures the time it takes for each particle to travel from the vertex to the detector, allowing for precise determination of its speed. It was built in 2005-2006 for hadron identification in Pb-Pb collisions at intermediate transverse momentum p_T and is composed by Multigap Resistive Plate Chambers (MRPCs) placed at a radial distance between 3.7 m and 4.0 m from the beam line. It covers with a large cylindrical array of $\sim 141 \text{ m}^2$ of active area the region of $-0.9 < \eta < 0.9$, with η the pseudorapidity². The TOF allows to perform Particle IDentification (PID) and features a time resolution of 80 ps in pp and 68 ps in Pb-Pb. In the following section, it will be briefly illustrated how to perform PID via TOF measurements.

²pseudorapidity (η) is a spatial coordinate indicating the angle that the particle direction forms with respect to the beam axis. It is defined as $\eta = -\ln[\tan(\theta/2)]$, where θ represents the angle between the particle's momentum and the positive direction of the beam. In this case, it corresponds to $\pi/4 \leq \theta \leq 3\pi/4$.

2.3.1 Particle IDentification with TOF

The TOF measurement can be used to perform PID. In particular, the PID by mass determination is performed in the ALICE TOF. In order to identify any stable charged particle, it is necessary to determine its charge and its mass. The charge sign can be inferred from the curvature of the particle's track. Since the mass can not be measured directly, it has to be obtained from other variables, like the particle momentum p and the velocity β . The basic principle is to measure β by measuring the time interval Δt , called t for simplicity, employed by the particle to travel the distance L . Knowing the particle momentum p with a magnetic spectrometer measurement, it's possible to obtain the particle mass as $m = p/(c\beta\gamma)$, where γ is the relativistic Lorentz factor. Indeed, with fixed momentum and distance, the time of flight depends only on the particle's mass. For a given particle momentum, the time of flight t can be directly mapped to the particle mass m :

$$\begin{aligned}\frac{L}{t} &= \beta c = \frac{pc^2}{E} = c \frac{p}{\sqrt{p^2 + m^2 c^2}} \\ \frac{t}{L} &= \frac{1}{c} \sqrt{\frac{p^2 + m^2 c^2}{p^2}} = \frac{1}{c} \sqrt{1 + \frac{m^2 c^2}{p^2}} \\ m &= \frac{p}{c} \sqrt{\frac{c^2 t^2}{L^2} - 1}\end{aligned}\tag{2.12}$$

The following approximation can be used:

$$\text{for } \frac{m^2 c^2}{p^2} \ll 1 \rightarrow \sqrt{1 + \frac{m^2 c^2}{p^2}} \approx 1 + \frac{m^2 c^2}{2p^2}\tag{2.13}$$

It follows that for two particles with different masses but the same momentum, the difference between the two TOF measurements, after the particles travelled the same distance L will be:

$$\Delta t = t_1 - t_2 \simeq \frac{Lc}{2p^2} (m_1^2 - m_2^2)\tag{2.14}$$

From Eq. 2.12, the mass resolution can be computed as:

$$\left(\frac{\delta m}{m}\right)^2 = \left(\frac{\delta p}{p}\right)^2 + \left(\gamma^2 \frac{\delta L}{L}\right)^2 + \left(\gamma^2 \frac{\delta t}{t}\right)^2\tag{2.15}$$

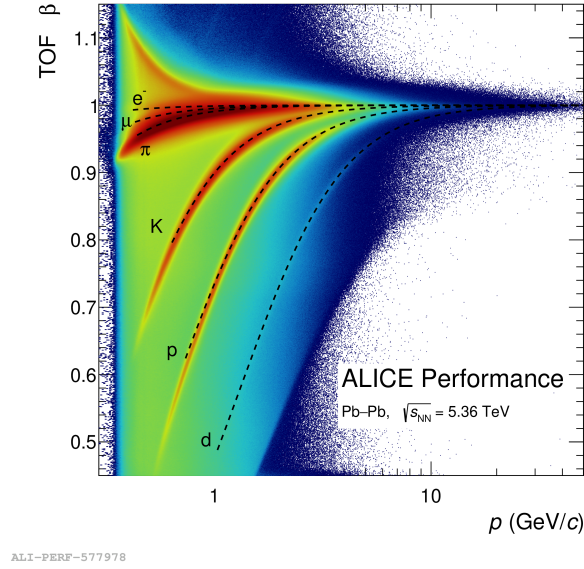


Fig. 2.6 Particle velocity β as a function of momentum, measured by the ALICE TOF for Pb-Pb collisions at 5.36 TeV in Run3.

and, as in most cases $\gamma \geq 1$, the mass resolution is predominantly affected by the accuracies in the time and length measurements, rather than by the accuracy of the momentum determination. The complete calculations can be found in App. A.2. The *separation power* can be used to quantify the usability of a technique, as it defines the significance of the detector response [41]. The TOF PID separation power, indicating the ability to distinguish different particles, is given by the number of standard deviations in the time-of-flight difference of two particles:

$$n_{\sigma TOF} = \frac{\Delta t}{\sigma_{TOF}} \quad (2.16)$$

where σ_{TOF} is the resolution of the TOF measurement. The better is the time resolution, the more accurate and reliable will be the TOF PID capability [42]. Fig. 2.6 shows the measured particle's β by the TOF, as a function of the momentum. The electron, muon, pion, kaon, proton and deuteron bands are well separated.

2.4 Future upgrades of the ALICE experiment

The research work presented in this thesis has been carried out in the framework of two future upgrades of the ALICE experiment, namely the ITS3 and ALICE 3. The following sections present an overview of the motivations driving the upgrades, providing the context to this research work.

2.4.1 The third generation Inner Tracking System (ITS3)

In order to reach the ALICE goal of advancing the understanding of the QGP, an improvement in the statistics and measurement at low- p_T of several heavy-flavour baryon and mesons species, the ALICE Collaboration foresees an upgrade of the above described ITS2 (Sec. 2.3). In particular, during the third LHC long shutdown (LS3, 2026-2028), the innermost three layers of the ITS2 will be substituted with a new vertex detector composed of bent and ultra-thin monolithic silicon sensors [43]. Such upgrade is called Inner Tracking System 3 (ITS3) and will give rise to a nearly massless detector based on wafer-scale silicon sensors with size of $10 \text{ cm} \times 26 \text{ cm}$, reaching a stunning material budget of $0.07\%X_0$ per layer [44]. Indeed, the sensors

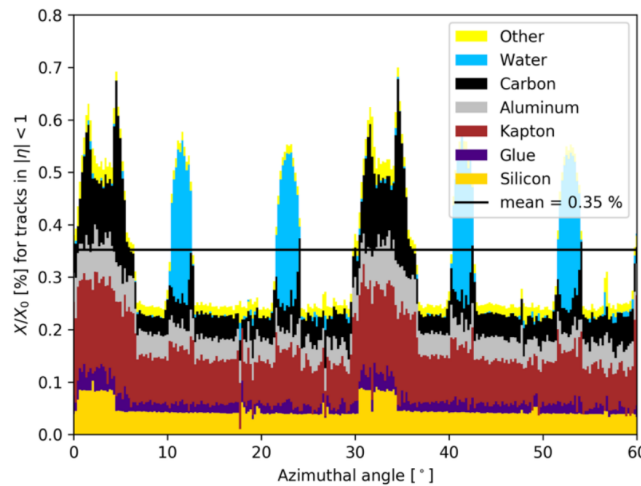


Fig. 2.7 Material budget components of the current ALICE ITS2 layer 0 as a function of the azimuthal angle. Figure from [43].

will be thinned down to less than $50 \mu\text{m}$ and curved into truly cylindrical detector layers, held in place with carbon foam and cooled by a forced airflow. No further

mechanical support (i.e. staves like in the previous ITS2) or electrical connection (circuit board) are necessary within the active area. This extraordinary reduction of the material budget can be inferred from Fig. 2.7, where the different materials included in one layer of the current ALICE ITS2 are shown. By removing materials like kapton and aluminum for circuit boards, water for cooling, carbon and glue for mechanical support, wafer-size stitched silicon sensors would result in a material budget of about 0.07%.

Stitching provides fabrication of pixel sensors of arbitrary dimensions, within the wafer constraints, enlarging the size of the mask that is used in the photo-lithographic process of chip manufacture. Here, parts of the mask are exposed in a periodic, aligned fashion to create a circuit that continues across several exposures [43] [44]. The ITS3 layout is made of three concentric cylindrical stitched detector layers, split into an upper and a lower half, as can be observed in Fig. 2.8.

Each half-layer is made of one single piece of silicon and the innermost layer will

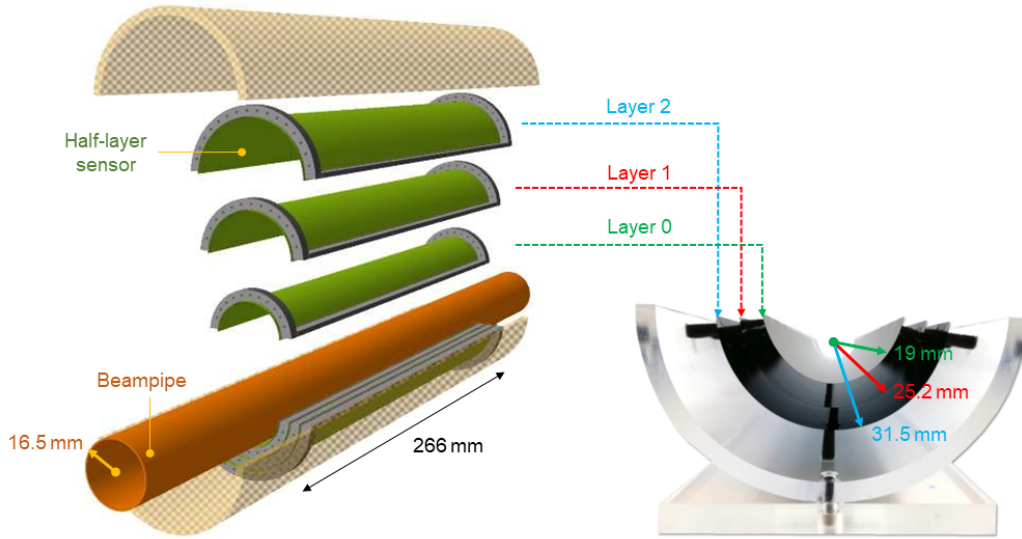


Fig. 2.8 Simplified ITS3 detector layout

be mounted around the beam pipe with a very small distance of 2.5 mm. The main features of the ITS3 are listed in Tab. 2.1. Both the lower material budget and the closeness to the interaction point (19 mm) will lead to a factor two improvement in pointing resolutions from very low p_T (~ 100 MeV/c) [45].

An idea of the improved performance of ITS3 with respect to the current ITS2 can be inferred from Fig. 2.9, showing the simulated impact parameter resolution for ITS2 and ITS3 detectors. For what concerns the technology employed for the ITS3

Table 2.1 ITS3 specifications

	Layer 0	Layer 1	Layer 2
Radial distance (mm)	19	25.2	31.5
Length (mm)	260	260	260
Sensors dimensions (mm ²)	266 × 58.7	266 × 78.3	266 × 97.8
Material budget (%X ₀ / layer)		0.07	
Sensor thickness (μm / layer)		≤ 50	
Pixel size (μm ²)		O(20 × 22.5)	
Power density (mW / cm ²)		40	
NIEL (1 MeV n _{eq} cm ⁻²)		10 ¹³	
TID (kGray)		10	

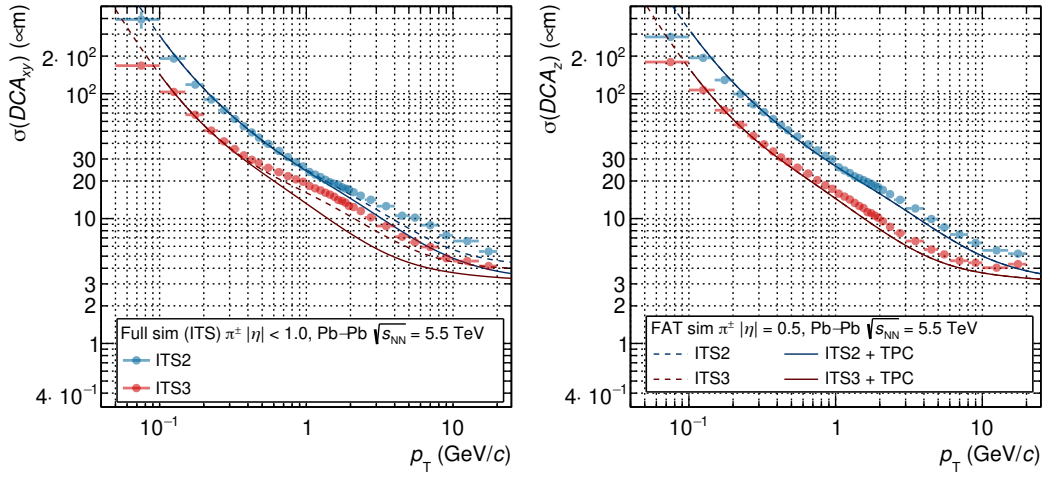


Fig. 2.9 Impact parameter resolution in the $r\phi$ (left) and longitudinal (right) direction as a function of the track p_T for ITS2 and ITS3 detectors. Image source [44].

upgrade, the TPSCo [46] 65 nm was chosen, benefiting from the smaller feature size with respect to the 180 nm employed in the ITS2 and larger wafers available (300 mm diameter instead of 200 mm). More detail on the sensor will be provided in Sec. 3.4.3. The work presented in this thesis fits into the first milestone of the R&D, in which the 65 nm technology has been validated for particle detection, as it will be demonstrated in Chapter 6.

2.4.2 The ALICE 3 upgrade

ALICE 3 is a proposal for a next-generation detector that could represent the successor of the present ALICE experiment [47]. It is part of the Phase IIb Upgrades of the LHC experiments during the fourth long shutdown (2033–2034). The following Runs 5 (2035–2038) and 6 (2040–2041) of LHC will allow to study more than five times the nucleon–nucleon luminosity available with Pb–Pb collisions in Runs 3 (2022–2025) and 4 (2029–2032), giving way to the ALICE 3 physics programme, in which particle identification will be essential. The proposed detector consists of a tracking system and multiple subdetector systems for particle identification, including silicon time-of-flight layers, a ring-imaging Cherenkov detector with high-resolution readout, a muon identification system and an electromagnetic calorimeter. A representation of the ALICE 3 detector concept is shown in Fig. 2.10. The schematic longitudinal

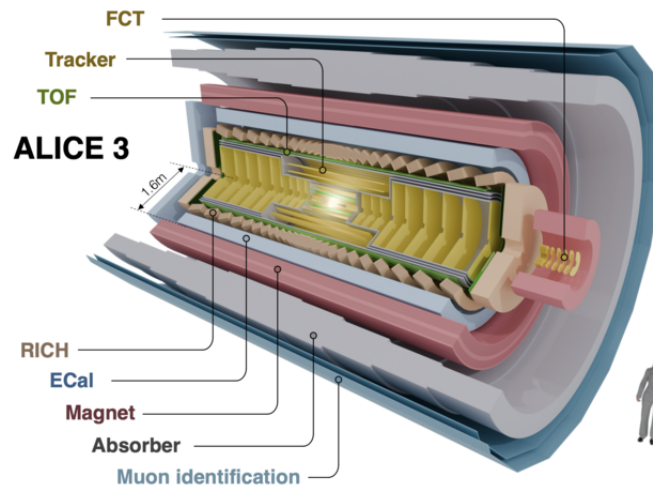
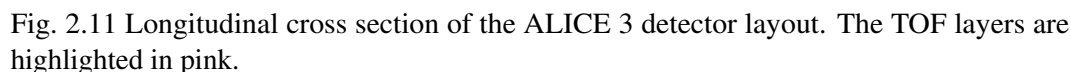


Fig. 2.10 Representation of the ALICE 3 detector proposal.

cross section of the reference detector is shown in Fig. 2.11.

The core of ALICE 3 is a large silicon tracker consisting of CMOS MAPS arranged



- an **Inner TOF** barrel located at $r = 19$ cm from the beam pipe, adjacent to the 6th tracker layer;
- an **Outer TOF** barrel located outside the last tracker layer at $r = 85$ cm;
- **Forward TOF disks** located at 375 cm on either side of the interaction point.

The technology that will be employed for the ALICE 3 TOF detector has not been selected yet. However, the R&D focuses on three sensor technologies: fully depleted CMOS sensors, Low Gain Avalanche Detectors (LGADs) and Single Photon Avalanche Diodes (SPADs) [47]. All of them will be outlined in the next chapter, but at this stage it's possible to say that the firsts could provide the required time resolution together with large-area scalability, profiting from the reduced production

Table 2.2 TOF system specifications

	Inner TOF	Outer TOF	TOF disks
Radius (m)	0.19	0.85	0.15 to 1
z range (m)	-0.62 to 0.62	-3.50 to 3.50	± 3.75
Granularity (mm ²)	1×1	5×5	1×1 to 5×5
Material budget (% X_0)	1 to 3	1 to 3	1 to 3
Power density (mW/cm ²)	50	50	50
Time resolution (ps)	20	20	20

expenses and the undemanding manufacturing process. An intense R&D is ongoing to evaluate the performance of the CMOS LGADs in which a thin gain layer has been introduced to reach the targeted timing resolution of 20 ps, while keeping a moderate power consumption. In Chapter 5, more details on the sensor and the ongoing tests will be provided. LGADs remain a promising choice to achieve the required time resolution as they represent an already consolidated technology. However, CMOS LGADs are now considered as a baseline solution while LGADs represent a backup option, since they are more costly ($\sim$ factor 1.6) and require dedicated readout electronics. On the other hand, SPADs built in CMOS technology could represent a possibility, but they suffer from dark count rate and fill-factor issues.

Chapter 3

Silicon detector technologies

In this chapter, an overview of some of the most important silicon detector technologies in the literature, employed in HEP, will be provided, with a particular focus on MAPS and their applications in Sec. 3.4 and following. In Sec. 3.5 silicon detector technologies optimised for time measurements will be presented.

3.1 Silicon Drift Detectors

In 1984 E. Gatti and P. Rehak introduced a new detector scheme based on the principle of sideward depletion [48]. The starting point consist of a high resistivity n-doped silicon wafer that can be fully depleted by implementing several p+ cathodes on both surfaces and a single n+ anode, positively biased with respect to the p+ electrodes. As the cathodes are far away from the anode, they are biased at progressively decreasing voltages, generating in this way a parabolic potential profile, called "gutter", trapping the electrons and driving them towards the anode, where they are collected. The key idea of this method is the possibility to fully deplete a thin, large area semiconductor wafer through a small contact located at the edge of the wafer.

Silicon Drift Detectors (SDD) derived from the principle of sideward depletion by adding, after a complete depletion of the semiconductor wafer, an electric field parallel to the wafer surface. This is achieved by a segmentation of either both or one of the p+ areas at the surfaces to form strip patterns and by adding a voltage gradient to the strip patterns. Charge carriers released within the depleted volume by the absorption of ionising radiation or by thermal generation, drift in the field towards

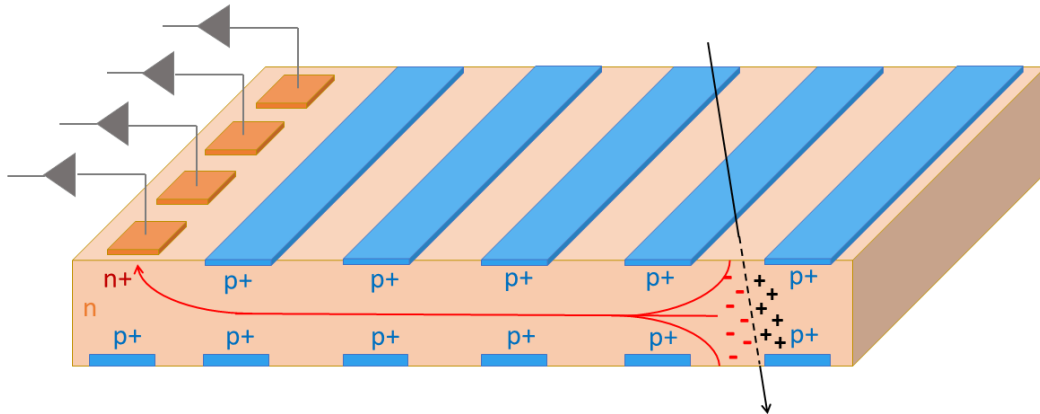


Fig. 3.1 Schematic cross section of a silicon drift detector. Electrons are guided by an electric field to the collecting anode, connected to an external amplifier.

the n^+ contact, which is connected to an amplifier. The main advantage of the SDD compared to a standard PIN-diode of the same size is the small anode capacitance which is independent of the active area of the device [49]. This feature translates in a shorter rise time and bigger amplitude of the output signal for a given amount of collected electrons, i.e. the signal is less subject to noise of subsequent electronic components [50]. The position in which the electron has been generated, i.e. the longitudinal position, is provided by the measurement of the time employed by the carrier to reach the anode. This latter is then pixelated, providing the transversal coordinate information. A schematic representation of a silicon drift detector is shown in Fig. 3.1.

Recent applications

Originally designed as position-sensitive detectors for particle tracking, SDD are nowadays regarded as state-of-the-art detectors for high resolution X-ray spectroscopy. New developments of SDDs by Fondazione Bruno Kessler (FBK) regarding their applications for X-ray spectroscopy have proved their performance in both cryogenic and room temperature, thanks to a minimization of the leakage current [51]. The leakage current reduction could be fully exploited in the ARDESIA (ARrays of DETectors for Synchrotron radIation Applications) project, started in January 2015 and funded by INFN with the aim of developing a versatile detector based on arrays of SDDs and low-noise electronics for synchrotron applications [52]. The goal is to perform X-ray absorption fine structure (XAFS) spectroscopy using

synchrotron radiation sources, in particular the X-ray beamline of LNF (Frascati National Laboratories, INFN, Frascati, Italy). The detector targets an energy range from 200 eV to 20 keV.

Another interesting application of SDDs has been spotted by the REDSOX group, a INAF (Italian National Institute for Astrophysics)-INFN-FBK collaboration which aims at developing large area SDDs with low noise electronics to be applied in spectroscopy and X-ray imaging [53]. In particular, the goals of the collaboration are: the development of high energy resolution SDDs for soft X-rays, the evolution of the SDD technology in collaboration with FBK CMM (Center for Material and Microsystems) in Trento, the development of large surface SDDs for X-ray astrophysics. The applications can be found in astrophysics X and γ , environmental monitoring, medical diagnostic.

Moreover, SSDs are exploited by the enhanced X-ray Timing and Polarimetry mission (eXTP) [54]. The mission is being developed by a large International Consortium, which includes institutions from China and 11 European countries, to explore the properties of matter and the propagation of light in the most extreme conditions found in the Universe and it will be an X-ray observatory. Three out of four detectors that will be included in the scientific payload will be equipped with SDD.

3.2 Silicon Strip Detectors

Silicon Strip detectors (SSDs) feature patterned implants, segmented into multiple strips with a very small pitch, i.e. the distance between two adjacent strips. Typical values for the pitch are lower than 50 μm and the lower the pitch, the better the spatial resolution. Each strip is connected to the readout electronics and signals are induced on a strip as a consequence of the passage of a particle in the active volume below the strip. These detectors are largely employed in particle physics experiments to measure particle trajectories with fine position resolution, for example in space applications. They feature a high spatial resolution, simpler readout and much lower power consumption per unit area compared to pixel detectors. The starting point for the use of silicon strip sensors in HEP experiments, can be set to 1960, when the Pisa group developed Si-strip sensor with 600 μm pitch [55]. Usually, p^+ (highly doped p-type silicon) strips are implanted on the n^- (lightly doped n-type silicon)

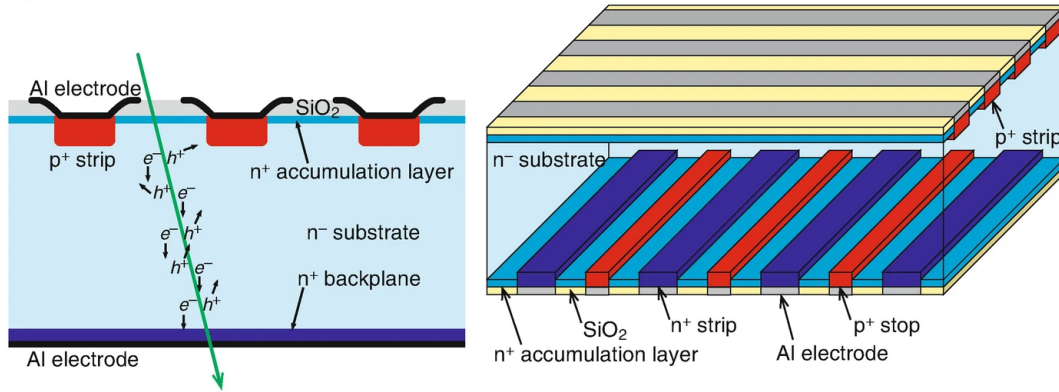


Fig. 3.2 Illustration of a silicon strip detector cross section (left), and double-sided silicon strip detector (right). Image source [5].

substrate, as displayed in Fig. 3.2 (left), because n^+ strips are difficult to isolate [5]. This difficulty originates from the formation of an electrons accumulation layer at the interface between the silicon and the silicon dioxide passivation layer on the surface of the device, which behaves as a conductive path.

Double-sided silicon strip detectors (DSSDs), as illustrated in Fig. 3.2 (right), are developed by placing n^+ strips orthogonal to p^+ strips on the opposite side of the detector. In this way, it's possible to get a two-dimensional position from a single device, lowering the number of needed detector layers and reducing multiple-Coulomb scattering, which improves the spatial resolution of the particle trajectory reconstruction (see Sec. 2.2.1). It has to be considered that strip-like devices have a quite high capacitance, that could be reduced only moving to a pixelated detector. SSDs are widely employed in satellite missions such as Fermi [56] (single-sided), AGILE [57] (single-sided), PAMELA [58] (double-sided), and AMS [59] (double-sided). The other main field of application of silicon strip detectors is the one of collider experiments, where strip sensors are regarded as a competitive alternative to pixel sensors, thanks to their simpler readout and lower power consumption. Several particle collider experiments have employed silicon hybrid strip sensors in the past years, for example the CMS experiment at CERN [60] assembled the largest silicon strip detector ever built. This technology is still taken into account to build new trackers, as in the case of the Phase-2 Upgrades of the CMS Outer Tracker [61] and of the ATLAS Inner Tracker (ITk) [62].

On the other side, some critical aspects in the use of strip detectors demotivate their employment for future applications [63]:

- microstrip are produced by dedicated facilities that are not so common, because of the high costs/profits ratio due to the the small market;
- microstrip technology is at the limit of its development as decreasing the strip pitch below $50\text{ }\mu\text{m}$ causes problems of capacitive coupling between the strips;
- for space applications, an on-board intelligence is needed to perform a real time supervision, increasing the demand for power consumption, readout speed and men power.

In particle tracking experiments in space, the transition towards a new technology based on pixel devices appears today an appealing option, as it solves some of the limitations characterising strip technologies, like the dependence of the spatial resolution on the pitch of the strips implanted on the silicon buffer or the accuracy in the reconstruction of the interaction point when the detector operates in environments with high radiation levels. The above stated arguments open the way to another flavor of silicon detectors, solving many of the mentioned issues: pixel detectors.

3.3 Silicon Pixel Detectors

Pixel detectors consist of a matrix of active silicon volumes, where the charge is generated, and sensing electrodes connected to the readout electronics. With respect to the above introduced microstrip detectors, pixel detectors provide a precise 2D-information, avoiding, in this way, the ambiguities in the impact position determination that could happen at high track densities. Moreover, they feature a lower leakage current, and consequently lower noise and better radiation tolerance, together with a lower capacitance, which again translates into lower noise.

From the electronic point of view, however, pixel detectors need many readout channels, one for each pixel in the matrix and this implies that a large number of signals have to be processed. For this reason, microstrip detectors are still largely employed in space applications for their simpler readout and much lower power density¹ with respect to pixel detectors.

Different silicon pixel detector technologies are briefly described in the following sections, trying to highlight benefits and drawbacks of each one.

¹Power consumption per unit area.

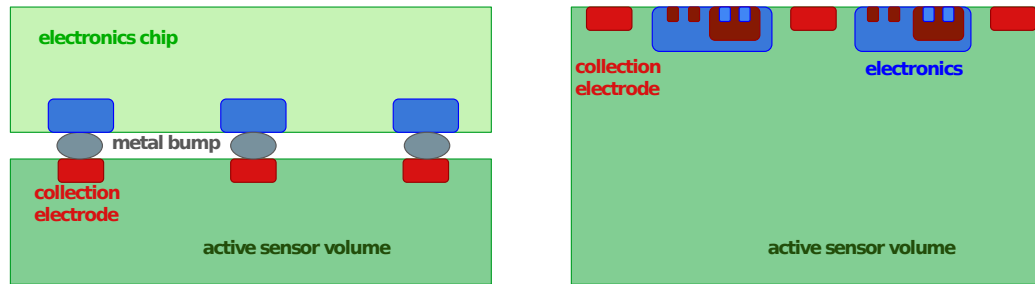


Fig. 3.3 Representation of a hybrid detector concept with bump bonding (left) and monolithic sensor concept (right).

3.3.1 Hybrid pixel detectors

In hybrid pixel detectors, the readout electronics (amplifiers, discriminators etc.) is implemented on a separate silicon volume with respect to the active one. The active volume and the chip are then interconnected typically through a procedure called external bump bonding or wire bonding. In this approach, a direct electrical connection (DC coupling) between sensor pads and the readout Application Specific Integrated Circuit (ASIC) is performed through small (around $20\text{ }\mu\text{m}$ diameter) solder metal balls or wire bonding. A schematic of a bump-bonded hybrid detector is shown in Fig. 3.3 (left), where the active sensor with its collection electrodes and the upper chip are depicted. Different assembly techniques are available and under study, like anisotropic conductive adhesives, replacing solder bumps with conductive micro-particles embedded in an epoxy layer, applied as either film or paste [64].

A relevant advantage of this detector flavour is the possibility to optimise both the sensor and the readout ASIC independently. On the other side, the structure is complex because of the interconnection between the two components, which translates into high costs of production and an increased overall material budget. All these difficulties were overcome with the introduction of monolithic detectors, described in detail in the next section.

3.4 Monolithic detectors

1990s saw the emergence of CMOS Image Sensor (IS) technologies, thanks to their ability to fabricate NMOS and PMOS transistors on the same substrate and the use of

a monolithic detector for particle physics, based on commercial CMOS processing, dates back to 1989 [65]. MAPS, regarded as the successor of the CCD [10], are pixellated sensors integrating the CMOS circuitry in doped wells separated from the collection electrode, as illustrated in Fig. 3.3 (right). Monolithic detectors lodge the electronics in the same silicon substrate that contains the active volume, avoiding the expensive and complex interconnections between the sensor and the readout chip. The possibility of joining detection volume and readout circuitry in the volume of a pixel allows the development of thinner sensors, beneficial for a better time resolution (2.1). A further advantage of monolithic CMOS technologies is the possibility of low-cost mass production using a commercial CMOS process [66][67]. The state of the art includes different options to integrate the CMOS logic in the sensor as it will be briefly described in the following.

3.4.1 SOI CMOS

Silicon-On-Insulator (SOI) monolithic sensors feature two different silicon layers separated by a SiO_2 buried oxide (BOX) layer. In particular, the upper thin low-resistivity layer hosts the readout electronics and a high-resistivity bottom wafer is used as the active volume. The key point of this technology is the possibility to employ differently doped silicon wafers for the substrate and the electronics [68] [69]. A schematic of a SOI structure can be observed in Fig.3.4. Among the main ad-

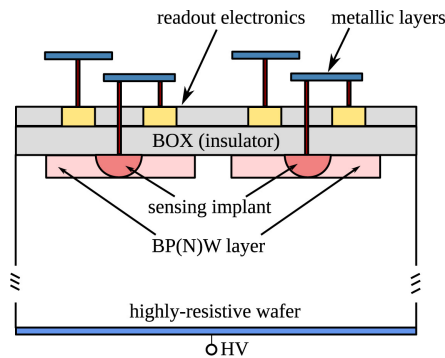


Fig. 3.4 Schematic cross section of the SOI concept. The Buried N(P)-Well (BN(P)W) is a layer dedicated to shielding the electronics from the sensors electric field. Image source [68].

vantages, a low capacitance can be obtained because of a small collection electrode design. The insulator layer reduces parasitic capacitances, allowing for a faster readout electronics with a lower power consumption. Thanks to the shielding of the

CMOS logic from the sensor active volume, a high bias voltage can be applied to the bulk in order to fully deplete the sensor.

The main problem with SOI is their weak radiation hardness, because of the accumulation of positive charge in the SiO₂ layer after the irradiation, causing a shift in the transistor working point and compromising their activity.

3.4.2 High Voltage CMOS

The high-voltage CMOS (HV CMOS) sensors are a concept of CMOS active pixel sensors developed to detect ionizing particles and with the goal of 100% fill-factor. The term "high-voltage" has to be intended as any voltage significantly higher than the standard supply voltage for a typical low-voltage CMOS chip [70]. Their peculiarity is that the pixel collection electrode is a deep n-well in which CMOS pixel electronics is implemented. In particular, PMOS transistors are implemented directly in the n-well and the NMOS are placed inside p-wells, included in the deep n-well themselves. The deep n-well is then implanted in a p-type substrate, constituting a pn junction. By biasing the substrate with a high negative voltage and by the use of a lowly doped substrate, a good depletion can be reached (one order of magnitude larger than that of a pn junction in a standard CMOS chip [70]). This technology combines the advantages of the standard low-voltage CMOS transistors, with a charge collection mainly by drift, thanks to the high electric field. The so called "floating logic structure" [70], allows the deployment of complex CMOS readout circuits inside the deep n-well, with signal amplification, threshold discrimination, time measurement, similarly to what is done in a hybrid detector. A graphical representation of four HV CMOS pixels is shown in Fig. 3.5.

The presence of a large collection electrode has several effects, like a more uniform electric field along the lateral size of the pixel, resulting in a homogenous response and short drift distances for the carriers generated in the substrate [71]. However, the homogenous electric field along the edge of the pixel, brings to a reduction of charge sharing and to the consequent worsening of the space resolution. In addition, HV CMOS feature a large sensor capacitance translating into a high analogue power consumption (see 3.4.4), as well as a large noise and a degradation of the timing measurement. HV CMOS sensors thinned down to 50 μm are employed for the Mu3e experiment vertex detector [72].

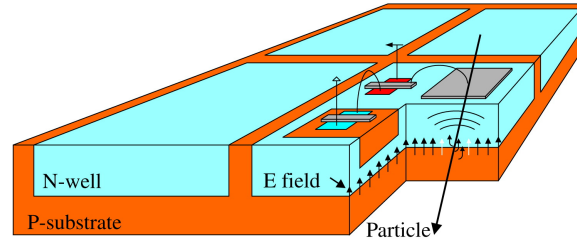


Fig. 3.5 Schematic representation of four HV CMOS pixels [70].

3.4.3 High Resistivity CMOS

To reduce the sensor capacitance, in High Resistivity (HR) CMOS sensors, full CMOS readout electronics is placed in a dedicated deep p-well, separated from the collection electrode. In this way, a small collection implant and therefore, a low capacitance, can be preserved with all the advantages of a fully monolithic design. HR CMOS technologies have been developed and deeply investigated in the context of the ALICE ITS2 upgrade [38], in which the TowerJazz 180 nm CMOS IS standard process has been adopted for the ALPIDE chip, briefly described in the next section. This process features a 25 μm thick, high resistivity epitaxial layer ($> 1 \text{ k}\Omega \text{ cm}$), grown on a low resistivity backside substrate, features deep p-wells with the aim of shielding the n-wells, in which the PMOS transistors are implemented, to compete with the collection electrode in the charge collection process. A schematical representation of a HR CMOS sensor cross section in TowerJazz 180 nm standard process is shown in Fig. 3.6 (left). The pn junctions originate between the collection electrode (n) and the epitaxial layer (p) and between the n implants of the NMOS transistors and the p-wells in which they are located. When the bias voltage needed to enlarge the depletion region is provided to the p-wells, a spherical shape depletion region starts to expand. Even with very high resistivity epitaxial layer, a complete lateral depletion is challenging to be achieved for the small collection electrode design, since the depletion needs to evolve from a narrow region around the collection electrode in a lateral direction under the p-wells. For this reason, in this standard process, a complete charge collection by drift is not possible, thus compromising the fast response of the sensor, due to the time difference between the hits in the central region and the ones in the corner. To overcome this problem, process modifications have been implemented in the 180 nm CMOS IS process, as described in the following.

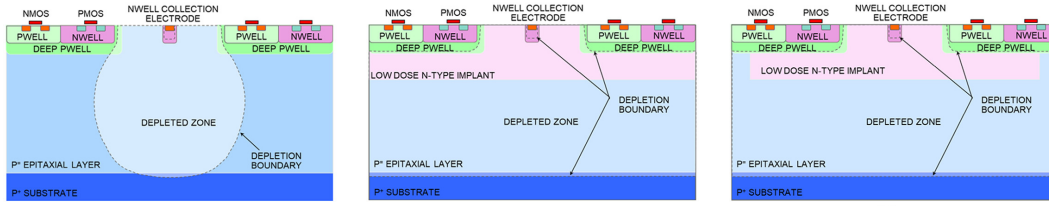


Fig. 3.6 Pixel cross section of different processes implemented in TowerJazz 180 nm CMOS IS process. Standard (left). Modified process with low dose n-type implant (center). Modified with gap process (right). Image source [73] [74].

Process modifications in the 180 nm CMOS IS technology

Fig. 3.6 (left) shows a standard process cross section, where the depletion region expands when increasing the reverse bias, but is still confined in a narrow volume around the collection electrode. As a consequence, charge carriers generated outside the balloon-shaped depletion region are collected by diffusion (with times in the order of 100 ns). To improve the speed of the charge collection and to get precise timing in the sub-nanosecond range, a more uniform drift field and depletion are required and represent the goals of the accurate design and test campaigns conducted in the past years in a joint effort among several groups and collaborations [75]. The work was indeed conducted in the framework of the ATTRACT project FASTPIX [73], the ALICE Collaboration [76], the Compact Linear Collider (CLIC) [75] detector development and the upgrade of the outer pixel layer of the Inner Tracker (ITk) of the ATLAS detector in view of the HL-LHC upgrade [77]. The driving idea is to give rise to a planar junction more in depth in the sensor and therefore separated from the collection electrode, avoiding the problem of non uniformity in the electric field which was dropping to zero in the pixel corners [75]. This goal is reached by adding a deep low dose n-doped layer, building a pn junction with the p-doped epitaxial layer, from which the depletion starts and extends over the full pixel area. This process modification, called *modified*, is shown in Fig. 3.6 (center) and allows to collect charges by drift without the need of particular layout or circuit modifications with respect to the *standard* process. The most critical parameter to be optimised was the dose of the deep n-type implant, as it should be low enough to allow full depletion, but at the same time high enough to avoid the punch-through to occur between the deep p-wells and the substrate [74]. Moreover, to improve the electric field strength in the pixel corner, further process modifications have followed, by introducing a gap in the n-doped layer at the pixel edges or adding an extra deep-p

implant [75]. The final goal was to generate a gradient in the doping profile, bend the electric field lines towards the collection electrode and reduce the charges drift path, improving the speed of the charge collection process. A cross section of the so called *modified with gap* process is shown in Fig. 3.6 (right).

3.4.4 The interplay of power consumption, SNR and capacitance

For the ITS3 and ALICE 3 TOF upgrades, the maximum allowed power densities are 40 mW/cm² and 50 mW/cm², respectively. The main contributions to the power consumption are represented by the analogue circuitry, the digital processing circuitry, the data transmission and the power consumption of the sensing diodes. The power consumption impacts on the design of the detector because it is directly proportional to the material budget². A system with high power consumption requires a power supply distribution system and cooling systems for heat dissipation. In particular, a passive or an active cooling could be employed: in the first case, material layers with a good thermal conductivity, able to collect and remove the heat are adopted, while in the second case a gas or a liquid flush removes the heat.

The digital power consumption depends on the design of the readout architecture of the detector and it can be limited adopting smart solutions. The analogue power consumption depends on the design of the sensor. The signal amplitude can be expressed as a voltage as $V = Q/C_{eq}$, where Q is the collected charge and C_{eq} is the equivalent pixel input capacitance. The Signal-to-Noise Ratio (SNR) is calculated as the ratio between the signal and the noise, both expressed in volts³. A large SNR is desired for timing measurements (see Sec. 2.1). Clearly, a lower capacitance improves the SNR and is therefore attractive for a low detection threshold and fast timing measurements. Indeed [78][79],

$$\frac{S}{N} \sim \frac{Q}{C_{eq}} \sqrt[m]{P} \quad 2 \leq m \leq 4 \quad (3.1)$$

²The detector thickness expressed in X_0 units, where X_0 is the radiation length. $X_0(\text{Si}) = 21.82 \text{ g/cm}^2$.

³The noise is expressed as an equivalent series voltage at the pixel input.

and, for a constant SNR, the analogue power consumption is linked to the charge and the capacitance by:

$$P_{\text{analogue}} \sim \left(\frac{Q}{C_{eq}} \right)^{-m} \quad 2 \leq m \leq 4 \quad (3.2)$$

which makes Q/C_{eq} the key parameter to reduce power consumption, as a factor 2 gain in Q/C_{eq} allows to reduce the power consumption by a factor 4 to 16. The relation shows a trade-off between the power consumption and the performances that one wants to achieve in terms of timing and tracking. In fact, the generated charge inside the detector, that should be maximised, depends on the incident particle properties and on the detector thickness. On the other hand, to obtain a good tracking performance and time resolution, the detector thickness must be small, in order to minimise X_0 . The input capacitance can be optimised during the sensor design, and it represents a key objective in the development of a detector devoted to timing measurements.

3.4.5 Applications of MAPS

MAPS represent a very attractive option for projects with large scale silicon trackers and stringent requirements on the material budget. MAPS have a wide range of use, from HEP experiments to space applications. Starting from HEP experiments, some relevant examples are presented in the following.

HEP experiments

- **The Ultimate-2 sensor (Mimosa28)**

The first application of the monolithic technology in HEP experiments is represented by the PiXeL detector (PXL) for the Heavy Flavor Tracker (HFT) of the Solenoidal Tracker at RHIC (STAR) experiment at the relativistic Heavy Ion Collider (RHIC), Brookhaven National Laboratory (BNL). The goal of the detector is to improve the spatial resolution and vertex reconstruction, performing heavy quarks measurements, and characterise the Quark-Gluon-Plasma generated in heavy ion collisions. It has been the first vertex detector fully equipped with MAPS to be operated in a collider experiment, covering a total silicon area of 0.16 m^2 [80] and holding a total of 356 million pixels.

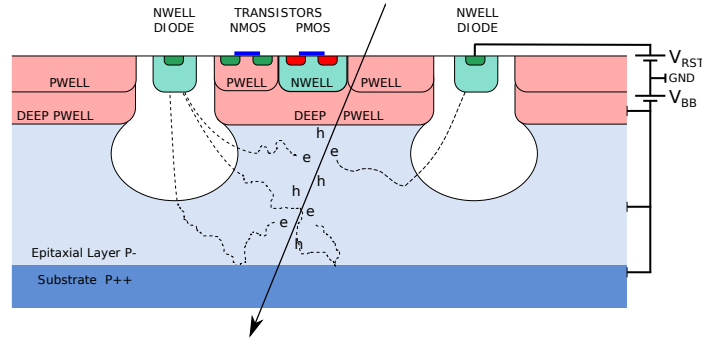


Fig. 3.7 Schematic cross-section of the ALPIDE chip. The white region represents the depleted area. Image source [82].

The Ultimate-2 sensor (also known as Mimosa28), developed in 2011, equips the PXL detector. Fabricated in the 0.35 μm twin-well technology and thinned down to 50 μm , it features a high-resistivity ($\geq 400 \Omega \text{ cm}$) epitaxial layer, a pixel pitch of 20.7 μm and 170 mW/cm^2 power consumption.

- **The ALPIDE chip** [81] is a 1.5 cm $\times$ 3 cm MAPS with 512 $\times$ 1024 pixels featuring a 29 μm $\times$ 27 μm pitch, read out in a binary hit/no-hit fashion, currently employed in the ITS2 of the ALICE experiment (see Sec. 2.3). The sensor is implemented in the standard TowerJazz 180 nm CMOS IS process (see Fig. 3.6 (left)) on a low resistivity ($\sim 10 \Omega \text{ cm}$) p-type substrate with high resistivity ($> 1 \text{ k}\Omega \text{ cm}$) p-type epitaxial layer. It offers the possibility to apply a reverse bias to the substrate ($< 10 \text{ V}$), in order to significantly improve the charge collection. The collection electrodes are n-well diodes with a diameter $\sim 2 \mu\text{m}$. Additional p-well and n-well implantations, at the top of the epitaxial layer, form the bulk of the NMOS and PMOS transistors, respectively, and are shielded by a deep p-well. Each pixel cell contains a sensing diode, a front-end amplifier and shaping stage, a discriminator and a digital section, while analogue biasing, control and readout are implemented in a peripheral region. A schematic cross section of the ALPIDE chip can be observed in Fig. 3.7. It demonstrated a detection efficiency above 99%, a fake hit rate better than $10^{-5} \text{ evt}^{-1} \text{ pixel}^{-1}$ and a spatial resolution around 5 μm over a large range of operational settings [39]. The power consumption is lower than 40 mW/cm^2 and the performance is not compromised after neutron irradiation to $10^{13} \text{ 1 MeV neq cm}^{-2}$.

- **The MALTA chip**

In the context of the ATLAS ITk upgrade Phase-II at the HL-LHC, a Depleted MAPS (DMAPS) called MALTA [83], based on 180 nm TowerJazz CMOS IS technology, has been designed to meet the radiation hardness requirements ($1.5 \times 10^{15} \text{ 1 MeV } n_{eq} \text{ cm}^{-2}$) of the outer barrel. The small pixel size ($36.4 \times 36.4 \text{ } \mu\text{m}^2$) provides high spatial resolution. It features a small collection electrode ($3.5 \text{ } \mu\text{m}$ diameter) providing a small capacitance ($\sim 2 \text{ fF}$), that combined with the front-end circuit, results in a total input capacitance lower than 5 fF. To cope with a degraded efficiency in the pixel corners after irradiation to $1.5 \times 10^{15} \text{ 1 MeV } n_{eq} \text{ cm}^{-2}$, the "MALTA-Czochralski (MALTA-Cz)" full size DMAPS sensor has been developed with the goal to improve the radiation hardness. The design of small electrode CMOS sensors with special implant geometries on high-resistivity Czochralski substrates, combines the benefit of a small collection electrode with the advantages of a thicker detection layer: the low pixel capacitance is maintained for low noise and low power performance. At the same time, the signal amplitude is significantly increased due to the larger ionisation charge in thicker depleted sensors. Beam and laboratory test results on unirradiated and irradiated sensors have shown excellent detection efficiency ($> 95\%$) after a dose of $2 \times 10^{15} \text{ 1 MeV } n_{eq} \text{ cm}^{-2}$. The time resolution of the sensor is measured to be 2 ns [84].

- **The CLIC Tracker Detector**

Another interesting application regards the Compact Linear Collider (CLIC): a proposed linear e^+e^- collider concept for post HL-LHC phase to work at energies of up to several teraelectronvolts (TeV). The CLIC Tracker Detector (CLICTD) is a monolithic pixelated chip produced in a 180 nm IS CMOS process built on a high-resistivity p-type epitaxial layer. The chip comprises a matrix of 16×128 pixels, each measuring $300 \times 30 \text{ } \mu\text{m}$ [85]. An intensive campaign of process optimisation and modification has been performed on this technology, as pointed out in Sec. 3.4.3 and different pixel layouts were manufactured through a process split on different wafers. Results satisfied the requirements with a spatial resolution down to $(4.6 \pm 0.2) \text{ } \mu\text{m}$ and a measured time resolution down to $(5.8 \pm 0.1) \text{ ns}$ after applying an offline time-walk correction using the pixel-charge information. The hit detection efficiency stays above 99.7% for thresholds of the order of several hundred of electrons [71] [86].

Space applications: the HEPD-02

Moving now to space applications, the Italian Limadou Collaboration has developed the second generation High-Energy Particle Detector (HEPD-02) of the China Seismo-Electromagnetic Satellite (CSES-02) mission. The mission is a collaboration between the Chinese National Space Administration (CNSA) and the Italian Space Agency (ASI), and has the goal to investigate the near-Earth electromagnetic, plasma and particle environment, for studying the seismo-associated disturbances in the ionosphere-magnetosphere transition zone. In particular, the mission aims to confirm the existence of possible temporal correlations between the occurrence of medium and large seismic events and the observation, in space, of electromagnetic perturbations, plasma variations and precipitation of particle bursts (PBs) with high energy charged particles from the inner Van Allen belt. HEPD has the aim to detect electrons with energies between 3–100 MeV, and protons, in a range of 30–200 MeV. It will discriminate anomalous events possibly induced by seismicity from the natural background, caused by geomagnetic, tropospheric and anthropogenic electromagnetic emissions [87]. The launch of CSES-02 satellite is foreseen in 2025 and it will hosts the first Space tracker equipped with MAPS, after decades where silicon microstrip detectors have been the leading technology. In particular, in the the Direction Detector (DD), the ALTAI sensors have been employed, developed in the context of the ALICE experiment, with a very similar performance to the ALPIDE, but with a non dual-use classification [88]. This choice will bring to remarkable benefits as the reduction of the material budget of the tracker, a high detection efficiency ($> 99\%$), low fake hit rate ($< 10^{-7} \text{ evt}^{-1} \text{ pixel}^{-1}$) and good spatial resolution ($\sim 5 \mu\text{m}$).

3.5 Silicon sensors optimised for time measurements

In HEP experiments charged particle tracks are reconstructed to study particular physics processes, as described in Chapter 2. In particular, CERN will upgrade the LHC in the 2020s to a HL-LHC [89]. Such upgrade will increase, after 2029, the instantaneous luminosity (rate of collisions) by a factor five to seven with respect to the original design value and the integrated luminosity (total number of collisions) by a factor ten. To cope with an increased event pile-up and radiation levels, significant detectors innovations are required. In order to separate piled-up tracks deriving

from primary or secondary vertexes originated in the same bunch-crossing, their time separation ($\sim$ tens of picoseconds) can be exploited, to associate hits to the proper track. For this reason, a timing layer with a time resolution ranging from 10 ps to 100 ps must be designed. In this way, the time information will help during the reconstruction phase, disentangling primary and secondary vertexes and, at the same time, minimising ghost tracks [90]. In the following, an overview of the main technologies currently employed or under study for timing applications will be exposed. It has to be highlighted that three of them (LGADs, SiPM⁴ and 3D trenches) are hybrid detectors and, therefore, need an external readout electronics.

3.5.1 Low-Gain Avalanche Detectors

A LGAD is a silicon sensor in which the avalanche mechanism, responsible for charge multiplication, takes place [91] [92]. The design starting point is a sensor with an n-doped collection electrode and a p-type high resistivity substrate, in which a p+ layer (Boron or Gallium doping), called gain layer, is diffused just below the sensing electrode. Typical values for the depth of the gain layer with respect to the n+ collection electrode range from a fraction of micron to a few microns and its thickness is around 0.5-1 μm . The aim is to generate a high electric field region localised below the collection electrode, which can activate the multiplication mechanism for the electrons, making them acquire enough kinetic energy to produce additional e-h pairs, in a process called 'impact ionisation'. Typically, 20–50 μm thick substrates are used for LGADs. The gain value is a function of the bias voltage polarizing the p-n junction inversely and increases as the bias voltage increases. A schematic representation of an LGAD cross-section can be observed in Fig. 3.8.

In order to isolate the electrodes avoiding short-circuits between the pixels, a boron layer surrounding the n-electrodes (*p-stop*) can be employed, as in Fig. 3.8, or a uniform layer (*p-spray*) over the entire surface can lead to the same effect. Another important feature of an LGAD is the way the termination implants are designed. At the border of the pixel, there is an additional deep, low dose, phosphorus implant, ohmically connected to the n+ collecting electrode. This implant is called the *junction termination edge (JTE)* (in orange in Fig. 3.8) and it has to mitigate the electric field at the border, causing the maximum electric field to develop in the region beneath the gain layer, as desired [93]. Currently, LGADs are produced by different facilities

⁴Silicon Photomultipliers

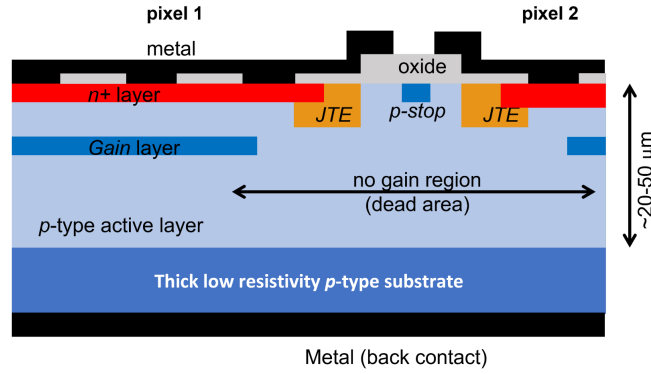


Fig. 3.8 Typical cross section of an LGAD. Image source [90].

like Brookhaven National Laboratory (BNL, Upton, NY, USA), Centro Nacional de Microelectrónica (CNM, Barcelona), Fondazione Bruno Kessler (FBK, Trento, Italy), Hamamatsu (Japan), IHEP-NDL (Beijing, China) and Micron (Lancing, UK). Dedicated amplifier boards for the readout have been produced by the University of California at Santa Cruz.

Charge multiplication

When the e-h pairs generated by the impinging particles drift through a region with a high electric field, around 300 kV/cm [30], they start to multiply. The gain of the avalanche process is defined as the ratio between the total number of e-h pairs collected with multiplication and in absence of multiplication ($G = N_{e,h}/N_{0\ e,h}$). The LGADs feature a moderate gain, between 10 and 30. The idea is indeed to have the lowest gain allowing to perform single particle time measurements with enough precision, avoiding, in this way, an excessive sensor noise and power consumption. The number of e-h pairs generated in the avalanche has an exponential dependency on the impact ionization coefficient $\alpha_{n,p}$ and on the path length x covered in the high electric field region [30]:

$$N_{e,h}(x) = N_{e,h}(0) e^{\alpha_{n,p} \cdot x} \quad (3.3)$$

After primary e-h pairs have been generated, they start to drift towards the collection electrodes (n+ for electrons and p+ for holes). When the electrons enter the gain layer, they are multiplied and create secondary e-h pairs. Since the multiplication happens very close to the cathode, secondary electrons are immediately collected.

On the other hand, secondary holes drift back towards the p+ contact, crossing almost entirely the substrate thickness before being collected, generating most of the signal, according to Shockley-Ramo theorem (see 1.4.2) [30]. A simulated typical signal of an LGAD with the separated contributions of primary and secondary (gain generated) electrons and holes, can be observed in Fig. 3.9a.

The key point of the working principle of an LGAD is a properly tuned electric field, allowing a controlled multiplication mechanism and, as a consequence, multiplication noise. This is achieved exploiting only electrons induced avalanche and not holes, avoiding electrical breakdown⁵. The n-type collection electrode is then connected to a fast read-out electronics by wire or bump bonding.

LGAD time resolution

The introduction of a gain layer allows to enhance the SNR of the sensor, decreasing the jitter contribution, but other key aspects must be considered to get the desired time resolution, as described in 2.1. The signal slew rate ($di/dt \sim dV/dt$) is linked to the sensor gain and its depleted (or active) thickness through the relation:

$$\frac{dV}{dt} \propto \frac{G}{d} \quad (3.4)$$

showing that decreasing the sensor active thickness and increasing the gain will generate signals with faster rising edge (i.e. a higher slew rate), improving the sensor timing performance. This fact is showed clearly in Fig. 3.9b, illustrating how the rise time of the signal can decrease by keeping a constant gain and just varying the sensor active thickness. At the same time, one has to keep in mind that a too high gain causes a worse SNR or a power consumption increase. The most important contribution to the timing performance of an LGAD is due to an intrinsic property of silicon, the Landau noise [6], representing the non-uniform charge deposition in the sensor. As described in 2.1, this effect is due to the non-uniform generation of charge along the track of the particle, which induces a variation of the signal shape. Thin substrates reduce the contribution of the Landau noise and recent results from test beam measurements have shown that LGAD with a thickness of 35 μm (FBK35) reach a time resolution of 22 ps at a bias voltage of 240 V and the 25 μm thick sensor

⁵The need of a small and controlled gain requires a stringent regulation in the doping level to a few percent and is therefore very challenging.

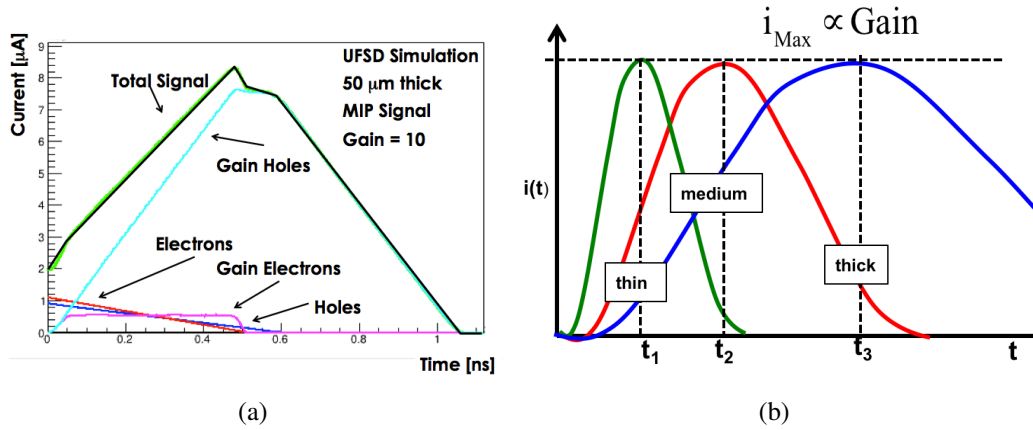


Fig. 3.9 Simulated signal of an LGAD with 50 μm thickness (a). Current signals for fixed gain and different sensor thicknesses (b). Images source [6].

(FBK25) showed a time resolution of 25 ps at a bias voltage of 120 V [94], while the 50 μm thick LGAD featured a ~ 30 ps time resolution. As shown in Fig. 3.8, the presence of the JTE and p-stops regions, introduced to avoid edge-breakdown phenomena, causes the appearance of a *dead area*, without gain. Typically, this region is $\sim 50\text{-}100$ μm wide and it causes a reduction of the fill factor (FF)⁶. In order to overcome this problem and minimise the gain losses because of sensor segmentation, technological solutions were proposed and they are briefly described in the following paragraphs.

Resistive AC-Coupled Silicon Detectors

A Resistive AC-Coupled Silicon Detector (RSD) or AC-LGAD is an optimised LGAD in which the gain layer is not segmented and covers the full sensor area [95][96]. It features a resistive n+ layer with a sheet resistance R_{sheet} ($\sim \text{k}\Omega$) where the charges propagate. The readout is performed via AC-coupling capacitors, inducing a signal on the metal pads and allowing a high segmentation. In particular, the AC-coupling is made via a thin dielectric film with a thickness ~ 100 nm between silicon and readout electronics [98]. In this technology, both the n-layer and the gain are uniformly distributed across the sensor surface, allowing for a 100% fill factor. Fig. 3.10 shows a cross section of a silicon AC-coupled LGAD. Two fundamental aspects that were properly optimised are the coupling oxide thickness and the n+ doping profile,

⁶the ratio between the sensor area with and without gain layer.

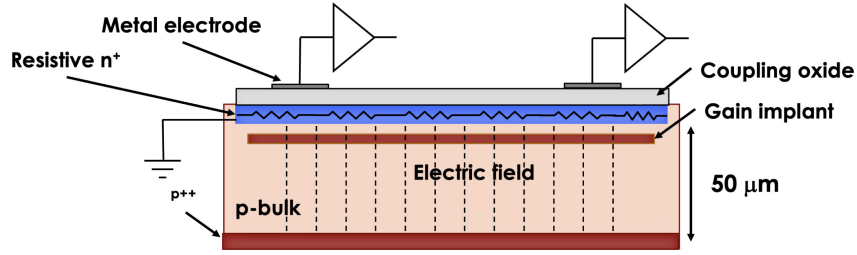


Fig. 3.10 Cross section of an AC-coupled LGAD with resistive n-type cathode and dielectric layer for the capacitive coupling the pads. Image source [97].

in order to guarantee a successful functioning of the device.

An important difference with respect to standard LGADs is the signal formation, as the charges are no more collected at the electrodes and signals are due to the capacitive coupling induced by the dielectric layer. In particular, the generated e-h pairs first produce a charge induction on the n+ resistive implant, in a similar way to standard LGADs; at this point the charges move toward ground in the n+ layer, but the AC metal pads, connected to the read-out electronics, offer to fast signals (about 1 ns for 50- μm thick sensors) a path to ground with a lower resistance than that provided by the resistive sheet [96]. These signals become therefore visible on the AC pads, charging the capacitors. Subsequently, the discharge of the pads is made possible through DC contacts. The resulting signal is bipolar, with a zero collected charge in total. The first RSD production (RSD1) was fabricated in 2019 by the Fondazione Bruno Kessler. Test beam measurements with 120 GeV/c protons demonstrated that RSDs with $\sim 200\ \mu\text{m}$ pitch can reach a timing resolution around 40 ps, similarly to standard LGADs, and that they can benefit from signal sharing among different pads to improve the spatial resolution below the one achievable with a binary readout [96]. Further in-beam measurements have followed on the second FBK RSD production (RSD2) and an array of seven 450 μm pitch pixels with cross-shaped electrodes was tested with a 5 GeV/c electron beam. The RSD were read out by a 16-channel ASIC with custom amplifier and a position resolution $\sim 14\ \mu\text{m}$ was measured, together with a temporal resolution of (49 ± 6) ps [97].

Trench-isolated LGADs (TI-LGADs)

To overcome the coarse segmentation typical of standard LGADs (500 μm - 1 mm), another proposed technological approach is the Deep Trench Isolation (DTI) technology [98] [99]. It consists in the introduction of narrow trenches ($\sim 1\ \mu\text{m}$ wide)

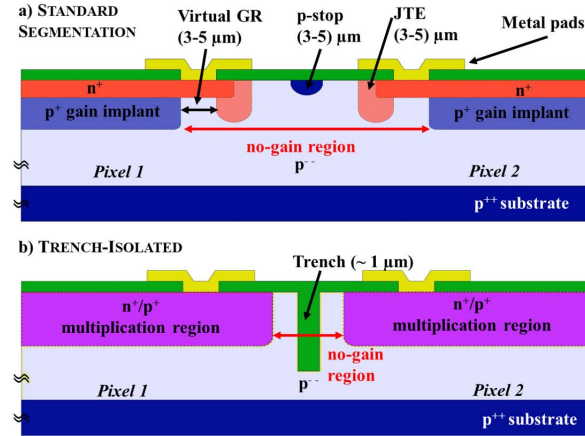


Fig. 3.11 Comparison between standard LGAD (top) and trench-isolated (TI) LGAD (bottom) cross section. Image source [99].

in the silicon substrate to guarantee electrical isolation between adjacent pixels. The trenches are filled with dielectric materials as silicon dioxide and there is no more need for p-stops and JTE at the edge. A schematic representation of the TI-LGAD concept is shown in Fig. 3.11, together with a comparison with the standard LGAD. In the latter, also the *virtual guard ring* (vGR) are highlighted: they consist in a gap between the JTE and the p+ gain implant and their role is to prevent early edge breakdown phenomena. In this case of standard FBK-LGAD, the no-gain region ranges between 31 and 66 μm [99], while in TI-LGADs the no-gain region is strongly suppressed to less than 6 μm . This allows for an improvement of the fill factor, that can be generally expressed as:

$$FF = \frac{(pitch - x_{ng})^2}{pitch^2} \quad (3.5)$$

where *pitch* is the pixel pitch and x_{ng} represents the no-gain region. Considering, for example, the case of an LGAD with a pitch of 250 μm , the FF improves from values around 50% to a FF larger than 90%.

3.5.2 Silicon Photomultipliers

A Silicon PhotoMultiplier (SiPM) is a solid-state photodetector that produces an analogue output signal in real time, when a photon is absorbed. SPADs have been used for photon detection and photon counting since many decades. The difference

between SPADs and SiPMs relies on how their readout circuitry is designed. In SPAD image sensors, the SPAD pixels are read out individually in order to generate an image. In SiPMs the individual pixels, or microcells, are a series combination of SPADs and a quenching resistor (RQ), connected in parallel into a single channel. As a consequence, the amplitude of the output signal will be proportional to the total number of fired pixels and therefore proportional to the photons number impinging on the pixel matrix. A SiPM contains a highly doped p-n junction of $0.5\text{--}2\ \mu\text{m}$ thickness, that make up the gain region and is biased above the breakdown voltage [100]. A cross section of a typical SiPM structure is shown in Fig. 3.12. All the microcells

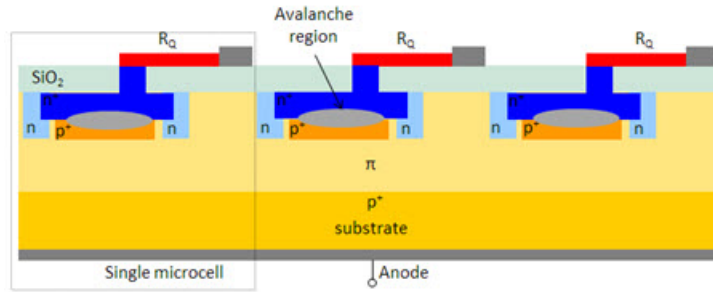


Fig. 3.12 Typical cross section of a SiPM. The gray oval represents the gain region. Picture from [101]

are connected in parallel and feature a size varying from $10\ \mu\text{m}$ to $100\ \mu\text{m}$, while the number of microcells per device ranges from several hundreds to several tens of thousands [101]. SiPMs work in the spectral region from UV to IR, peaking in the visible ($400\ \text{nm} - 500\ \text{nm}$). A SiPM is externally biased so that the voltage on each cell, called Avalanche PhotoDiode (APD), is above its breakdown voltage, making each APD to operate in Geiger mode. The difference between the biasing voltage and the breakdown voltage is known as overvoltage (OV) which represents the main adjustable parameter controlling the device operation. When a SiPM absorbs a photon, the generated charge carrier can trigger an avalanche in the gain region producing $10^5\text{--}10^6$ carriers. This number represents the SiPM gain. The role of the quenching resistor is to restore the APD back to the Geiger mode.

Recent studies have shown the capabilities of SiPMs to detect charged particles. As described in [102], the presence of a protection resin layer produces, via Cherenkov effect, a significant amount of photons at the passage of the charged particle. These photons, due to the small layer thickness, arrive on the SiPM surface with only few ps difference so essentially at the same time on the SiPM surface, generating a large

signal with many firing SPADs. In recent test beams, the timing resolutions were measured, indicating a value of about between 20 and 30 ps at 4 - 6 V of OV for MIPs at 10 GeV/c. Moreover, an improvement as a function of the number of firing SPADs was confirmed, reaching values below 20 ps for six or more fired SPADs [103].

3.5.3 3D silicon sensors

3D silicon sensors were introduced in 1997 [104] and are composed by three-dimensional electrodes penetrating into the silicon bulk, perpendicularly to the surface. The key point of this technology lies in the fact that the charge carriers are collected perpendicularly to the sensor thickness, making the deposited charge and the signal amplitude independent of the inter-electrode distance and electrode shape. In this way, a very short collection time can be achieved by simply reducing the inter-electrode spacing, without the drawback of lowering the signal amplitude. Among the explored configurations, in particular 3D columns and 3D trench, the most promising design is the parallel trench geometry [105] in terms of electric field and weighting potential uniformity, but also drift velocity saturation, both crucial ingredients for a good timing performance (see 2.1). A cross section of a 3D-trench sensor developed within the TIME and SPace real-time Operating Tracker collaboration is shown in Fig. 3.13 (left). The sensor has a n-in-p doping profile

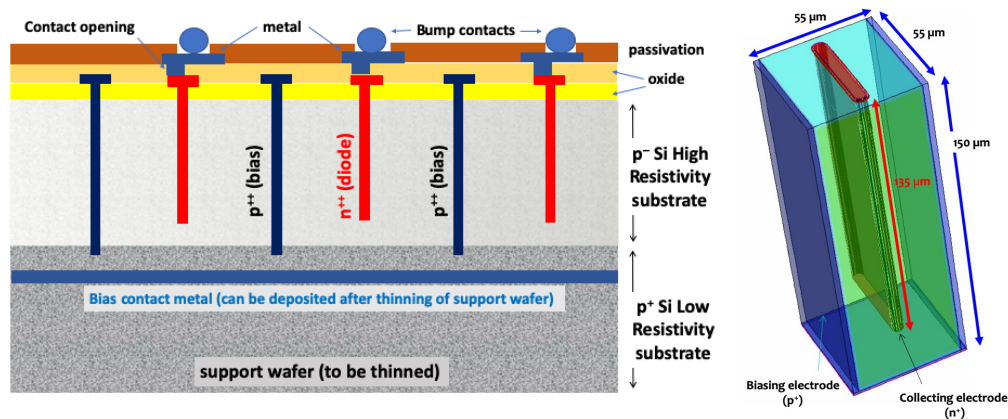


Fig. 3.13 Cross section of a 3D trench-sensor (left) and geometry of a 3D-trench pixel. Color scale: red for n++ doping, green for p- doping and blue for p++ doping. Images from [105].

and the depth of the sensitive volume is 150 μm , while the collecting electrode is

135 μm deep. A three-dimensional visualisation of the 3D-trench pixel is depicted in Fig. 3.13 (right). In this technology, however, the small inter-electrode distance of 15 μm causes an increase in the pixel capacitance, being equal to 110 fF.

The time resolution of 3D trench sensors was measured in a test beam with 270 MeV/c hadron beam. Each structure was attached to a printed circuit boards (PCB) containing the discrete-components front-end electronics, based on a two-stage signal amplification scheme. The measured time resolution was about 20 ps at room temperature and at a bias voltage of ~ -110 V, supplied from the backside contact. This result is however mainly due to the contribution of the electronic jitter of the front-end circuit, which has been estimated between 18 and 20 ps, while the intrinsic sensor time resolution is about 15 ps [105].

3.5.4 SiGe BiCMOS monolithic silicon pixel detector

The MONOLITH Horizon 2020 ERC Advanced project demonstrated that SiGe heterojunction bipolar transistor (HBT) electronics can be used to produce low noise, low power, and very fast frontend that could be integrated into a monolithic ASIC to produce a fully efficient detector with excellent time resolution. The Picosecond Avalanche Detector (PicoAD) features a fully depleted multi-junction with a continuous internal gain layer deep in the silicon sensor bulk. It separates a

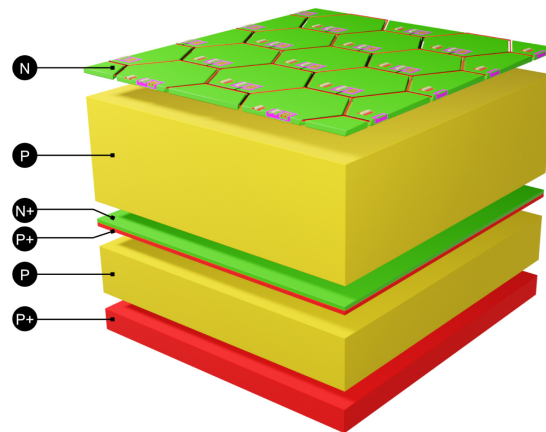


Fig. 3.14 PicoAD detector layout with the thin p+ - n+ junction constituting the continuous gain layer. Image source [106].

5 μm thick absorption region in which the primary electrons are generated from the 10 μm thick region where the electrons drift. Finally, it features a low resistivity p+

backside substrate. A schematic cross section of the PicoAD is shown in Fig. 3.14, where the different doping of the layers are highlighted. The two external pn junctions are reverse biased: the junction close to the top surface allows to isolate the pixels, while the one close to the bottom edge of the depletion region provides the electric field to generate and control the gain. The central, direct junction is isolated by the other two junctions, obtaining full depletion [107]. A prototype with hexagonal pixels having a side length of $65\ \mu\text{m}$ ($100\ \mu\text{m}$ pitch) and produced by IHP in the 130 nm SiGe BiCMOS technology was characterised with a beam of 180 GeV pions. At a bias voltage of 125 V, the detector provides full efficiency and an average time resolution of 17 ps, with 13 ps at the center of the pixel and 25 ps in the inter-pixel region, together with a power consumption of $2.7\ \text{W}/\text{cm}^2$ [107]. A time-walk correction has been applied.

Another monolithic silicon pixel matrix prototype without an internal gain layer was produced in 2022 in a commercial SG13G2 IHP 130 nm process and tested with a beam of 120 GeV/c pions. The sensor features a $50\ \mu\text{m}$ -thick epitaxial layer of $350\ \Omega\text{cm}$ resistivity and the high voltage is applied at the back of the sensor and on the top surface outside the guard ring. Moreover, several improvements have been applied in the electronics. The measured time resolution with time-walk correction is 20 ps at a bias voltage of 200 V and front-end power consumption of $2.7\ \text{W}/\text{cm}^2$ [108], together with a detection efficiency of 99.8% at a voltage threshold equal to seven times the voltage noise. In [109] it is shown, from laser measurements at a power density of $2.7\ \text{W}/\text{cm}^2$, an electronics jitter between 45 ps and 3 ps for laser pulses having amplitudes corresponding to 0.4 and 3.5 times the most probable value of the charge deposited by a MIP, respectively.

Table 3.1 provides a summary of the key characteristics of various chips as implemented in specific projects. The symbols σ_s and σ_t indicate the spatial and time resolution, respectively. Table 3.2 outlines some features of silicon detector technologies discussed in the chapter, without a particular link to any experiment. Both tables are not intended to be exhaustive, but they are meant to quickly identify essential information.

Project/Application	Technology	Power consumption (mW/cm ²)	Granularity	σ_s	σ_t
eXTP Spectroscopy Focusing Array	SDD	n.s.	hexagonal cells with 26.6 mm ² area	n.s.	10 μ s
Phase-2 CMS Outer Tracker	Silicon Strip Detector	< 100	90–100 μ m pitch with length 2.4–5 cm	~ 27 μ m	n.s.
AMS-02 Tracker	Silicon Strip Detector	~ 3	110 μ m readout pitch with length 29–62 cm	5–9 μ m	n.s.
STAR PXL (Mimosa28)	350 nm CMOS	170	squared pixels with 20.7 μ m pitch	4–6 μ m	n.s.
ALICE ITS2 (ALPIDE)	180 nm CMOS IS	< 40	29×27 μ m ²	~ 5 μ m	2–4 μ s
HEPD-02 (ALTAI)	180 nm CMOS IS	7 (clock off), 17 (clock on)	29×27 μ m ²	~ 5 μ m	2–4 μ s
CLIC Tracker (CLICTD)	180 nm CMOS IS	5.7 (matrix) + 49 mW (periphery)	300×30 μ m ²	4.6 μ m	5.8 ns
ATLAS ITk (MALTA)	180 nm CMOS IS	< 80	squared pixels with 36.4 μ m pitch	~ 5 μ m	2 ns

Table 3.1 The table summarizes the projects discussed in this chapter that currently use, or are planned to use, silicon detectors, highlighting their key performance parameters. In some cases, the name of the chip is included in parentheses after the project name. When a parameter is not specified, it is indicated as 'n.s.' (not specified). At present, the Phase-2 CMS Outer Tracker and the ATLAS ITk are foreseen to be installed during LHC LS3. The CLIC initial construction and commissioning are expected to start in 2026 [110].

Technology	Power consumption	Granularity	σ_s	σ_t
LGAD (25 μ m thick)	1–3 mW (sensor), 34 mW (amplifier board), 420 mW (minicircuit LEE39+ external amplifier)	$\sim 1 \times 1$ mm ²	$\sim$ mm	25–35 ps
Resistive AC-LGAD	10 mW/ch (FAST3 ASICs), sensor contribution negligible	450×450 μ m ²	14 μ m (3–5% pitch)	45 ps
SiPM	3.2 mW/ch (LiROC ASIC), sensor contribution negligible	1×1 mm ² with 10–100 μ m microcells	sub-mm ($\sim$ pitch/ $\sqrt{12}$)	20 ps for more than a few SPADs firing
130 nm SiGe BiCMOS	2.7 W/cm ²	100 μ m	n.s.	13–25 ps

Table 3.2 The table summarizes the performance of some silicon detector technologies discussed in this chapter. The contributions of the sensor and the readout electronics, employed in the measurements, to the overall power consumption are clearly specified. These technologies are not tied to a specific experiment but are suitable for a range of applications. When a parameter is not specified, it is indicated as 'n.s.' (not specified). References [111][112][97][113].

Chapter 4

TCAD and Monte Carlo simulations of Fully Depleted MAPS in the ARCADIA project

In order to simulate the performance of monolithic CMOS sensors, appropriate simulation tools are employed to study the signal formation and to help in the design optimisation of future prototypes.

In this chapter, simulation studies and results carried out in the framework of the ARCADIA project, funded by INFN, will be presented. The collaboration has three main lines on which the development focuses: space applications, medical applications, for which fast timing and low voltages are mandatory, and future colliders for HEP, demanding a high radiation hardness and an improved spatial resolution. The simulated sensors are Fully Depleted (FD) MAPS realised in 110 nm CMOS technology, representing an attractive option for particle tracking and timing applications, thanks to their low material budget and production costs. The adopted simulation flow will be illustrated on the Arcadia Main Demonstrator pixel sensor. A brief introduction to the employed simulation tools will be provided, followed by an illustration of the developed simulation chain that integrates the TCAD framework with Monte Carlo software. In particular, the first part of the chapter is devoted to a compact outline of the TCAD tool, which can be used for sensor modeling. In this context, a lightweight mesh has been introduced in the TCAD simulation of the Arcadia Main Demonstrator, in order to reduce the computing time, without compromising the accuracy of the results. Subsequently, the Allpix² tool will

be presented and its use will be motivated. The author developed an analysis framework to estimate the time resolution of the pixels and to study the cluster size under different geometrical and physical conditions. The proposed simulation approach enables the study of the sensor's intrinsic time resolution, incorporating both the Landau noise term and the distortion effect that influence the resulting time performance (see 2.1).

All the Monte Carlo simulations presented in this chapter and the next one have been carried out with the Open Computing Cluster for Advanced data Manipulation (OCCAM) cluster, managed in collaboration between the University of Torino and INFN Torino and funded by "Compagnia di San Paolo". The TCAD simulations have been performed thanks to the VPN Service of Politecnico di Torino.

4.1 Simulation tools

Technology Computer-Aided Design (TCAD)

A TCAD simulator is a numerical simulation tool supporting prototyping campaigns with simulations, giving the opportunity to simulate very complex geometries and to include a large number of effects. It simulates the electrical characteristics of semiconductor devices, as a response to external electrical, thermal, or optical boundary conditions imposed on the structure. Technology CAD simulators must describe two physical phenomena: the motion of electrical carriers and the generation of the electromagnetic field induced by such motion. The two phenomena are strongly entangled, since the presence of an electromagnetic field can affect carrier transport. For this reason, a TCAD simulator results from the coupling of carrier transport and electromagnetic models.

The software solves the Poisson-drift-diffusion (PDD) equations, describing the physics of the simulated device, using numerical methods on a spatial grid and the dynamic transitions are considered a series of quasi-stationary states. More details about the TCAD numerical solution of the charge transport model can be found in App. B.1. However, TCAD simulations are not a practical option when a high statistics is needed, due to the large computing time required for a single event. An integration with a Monte Carlo software is therefore highly advantageous in this context.

Allpix²

Allpix² [114][115] is an open-source software framework to conduct Monte Carlo simulations of silicon detectors. The framework builds upon other packages to perform tasks in the simulation chain, in particular, Geant4 [116] for the charge deposition by the particles crossing the sensors and ROOT [117]. In the Geant4 software, a collection of physics models is employed to handle the interactions of particles with matter across a very wide energy range. In particular, the FTFP_BERT_EMZ physics list was adopted and the Photon Absorption Ionisation Model (PAI) (see 1.3.1) was always employed in this work, to describe the energy loss distribution in thin sensors. The main advantage of the Allpix² framework is its ability to combine TCAD-simulated electric fields with a Geant4 simulation of the particles' interaction with matter, taking into account the stochastic nature of the initial energy deposition. Allpix² accounts for effects like Landau fluctuations in the energy deposition and the production of secondary particles such as delta rays. Subsequently, it employs a simplified charge transport algorithm, taking as input the electrostatic field map calculated by the TCAD simulation of the complex field configuration within the sensor [118]. One of the main differences between the two simulation tools is that TCAD considers local changes in the electric field and space charge region caused by charge movement. In contrast, in a Monte Carlo tool like Allpix², the electric field and weighting potential remain fixed after being imported. This fixed-field approach in Monte Carlo simulations helps to save computing time and power.

4.2 Simulation chain

The simulation chain in the Allpix² framework is arranged with configuration files and a set of modules implementing different simulation steps, executed sequentially for every event. A run consists of several sequential events, where a single event refers to an independent passage of one or multiple particles through the setup. The general simulation workflow is schematically represented in Fig. 4.1.



Fig. 4.1 Schematic illustration of the simulation flow adopted in this work, based on a combination of TCAD and Allpix². EF, EP and WP stand for electric field, electrostatic potential and weighting potential.

Import of the electric field and weighting potential from TCAD to Allpix²

Before the electric field distribution is imported from TCAD, it has to be properly converted from the TCAD adaptive mesh into a regularly spaced grid, allowing to speed up the following simulation steps. The *mesh converter* tool is employed to this purpose and the resulting electric field is replicated for all the pixels composing the matrix. A new regular mesh is generated by scanning the volume in regular x,y and z steps and then using a barycentric interpolation method to compute the electric field vector on the new point. The number of divisions employed in the new regular mesh can be set by the user. In order to establish the correct number of divisions, one has to keep in mind that a too fine mesh will lead to a considerable increase of the simulation time, while a too coarse one will probably result into an imprecise simulation, therefore a proper balance is required.

4.3 Arcadia Main Demonstrator: a FD-MAPS with small collection electrode

4.3.1 The sensor concept

FD-MAPS feature a high signal-to-noise ratio, low material budget and limited diffusion of the charge carriers generated by a particle crossing the active volume [119]. In fact, the charge is collected mainly through the drift mechanism, improving the speed and uniformity of response across the entire pixel matrix. The Main Demonstrator pixel sensor [120] has been developed in the framework of the ARCADIA collaboration, profiting from the work carried out in the predecessor Sensor with Embedded Electronics Development (SEED) project, aimed to develop an innovative

design for monolithic sensors using CMOS technology and realise a small scale prototype.

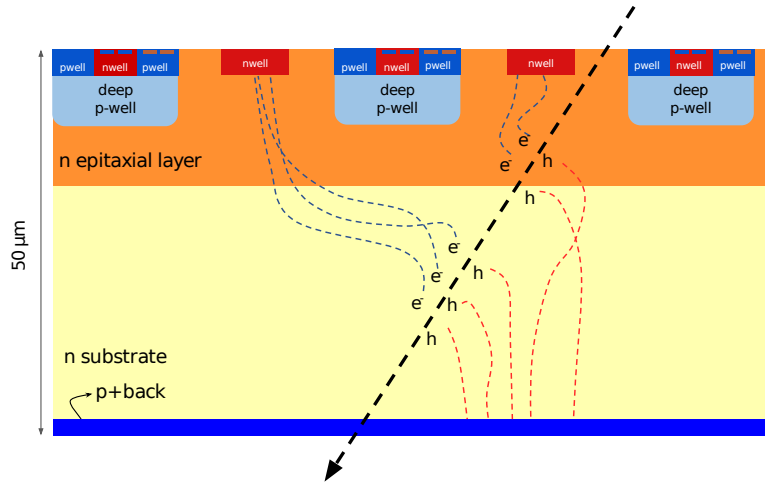


Fig. 4.2 Schematic cross section of the Arcadia Main Demonstrator sensor concept, for an active thickness of $50\ \mu\text{m}$. On the top side, the n-wells collecting the electrons are displayed in red, while the p+ backside electrode is shown in blue and is responsible for the collection of holes.

Figure 4.2 shows a simplified cross section of the Arcadia Main Demonstrator. The sensor concept features a small n-type collection diode located on the front side of the sensor and implanted on an n-doped silicon substrate (n-on-n). Electrons are collected at the n-well nodes, while holes are collected at the p+ electrode located at the bottom of the sensor. Specifically, this p+ boron-doped electrode forms a pn junction at the bottom, from which the sensor depletion starts. When sufficient negative voltage is applied, the sensor becomes fully depleted and the sensor nodes are electrically insulated. At low reverse voltages, the substrate remains partially depleted, resulting in resistive paths between pixels and causing current flow [121]. CMOS electronics is integrated into the n-wells (for pMOSFETs) and p-wells (for nMOSFETs), which are shielded by deep p-wells (in light blue in Fig. 4.2), avoiding charge collection competition between the sensing nodes and the n-wells containing the pMOSFET transistors. A low resistivity epitaxial layer is grown above the n-type substrate, enabling full depletion of both the substrate and the epitaxial layer at higher voltages. The goal of this layer is to provide a better control of the potential barrier under the deep p-well, delaying the voltage corresponding to the onset of punch-through. The punch-through phenomenon arises when the voltage applied to the backside electrode exceeds a specific value, denoted as V_{pt} , causing a hole current

to flow between the pwells/deep pwells on the front side and the p+ doped electrode at the sensor's bottom. From that point on, this current increases exponentially, and operating the sensor under conditions of significant punch-through current must be avoided, as it can lead to excessive power consumption [122].

The ARCADIA Main Demonstrator is designed in a modified 110 nm CMOS process, in collaboration with LFoundry. The chosen process node enables the integration of complex electronics directly within the pixel, while maintaining low prototyping and production costs [119]. This design allows to provide a high enough reverse bias voltage to the backside electrode and, simultaneously, low supply voltages (~ 1 V) to the front side of the sensor, where a readout electronics based on 1.2 V transistors can be employed [121]. The structure is assembled using two alternative approaches depending on the thickness of the active volume. For sensors thinner than $100\text{ }\mu\text{m}$, n-doped silicon layers are grown epitaxially on a p+ substrate, while for thicker sensors, exceeding $100\text{ }\mu\text{m}$, the production starts from a high-resistivity n-type substrate and the p+ region is added by backside implantation [120].

The ARCADIA Main Demonstrator chip

The Arcadia Main Demonstrator chip was designed and fabricated in the ARCADIA first engineering run in 2021. The chip is a matrix of 512×512 pixels arranged in double columns, covering an area of $1.28 \times 1.28\text{ cm}^2$. The demonstrator, developed for charged particles tracking, includes an event-driven readout architecture. The pixels contain both the analog and digital circuitry needed to amplify, discriminate, store, and transmit the address of the detected event. The prototype was tested in laboratory with cosmic rays and a ^{90}Sr β source showing a total power consumption of 10 mW/cm^2 at low event rates [123].

Further outcomes, not presented in this thesis, from the analysis of data collected during recent test beams will contribute to an exhaustive characterization of its performance in terms of cluster size, collection efficiency and spatial resolution. The following sections will present the simulations performed on this sensor to investigate its cluster size and evaluate its time resolution employing MIPs.

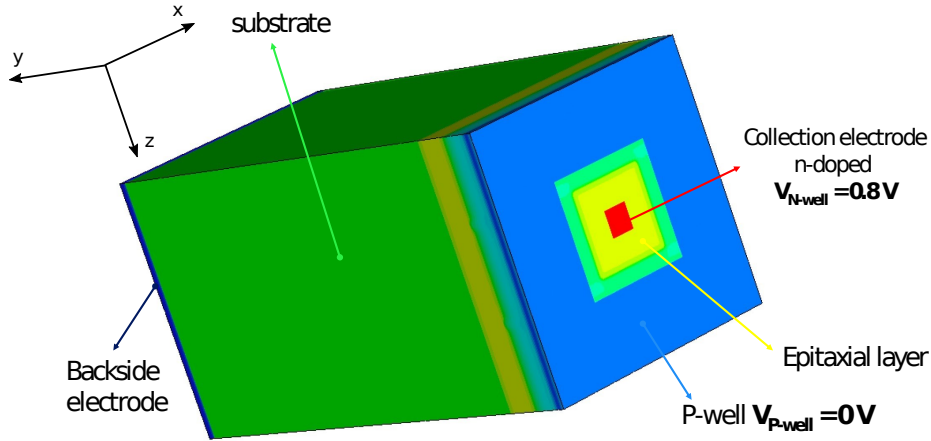


Fig. 4.3 TCAD 3D single pixel simulation domain. The color scale refers to the doping concentration. Image source [124].

4.3.2 TCAD simulations

As a first step, the pixel structure was simulated with three different sensor thicknesses, keeping the same fixed epitaxial layer. In TCAD simulation, a voltage of 0.8 V is applied to the collecting node contact ($V_{n\text{well}}$), while the CMOS electronics is operated at appropriately low bias voltages. Figure 4.3 shows a 3D TCAD simulation domain consisting of a single pixel with dimensions $(25 \times 25 \times 50) \mu\text{m}^3$.

Quasi stationary simulations were performed in which the voltages were gradually increased in tiny predefined steps to ensure simulation convergence. The solution to the Poisson equation is numerically computed in each point of the mesh shown in Fig. 4.4. This computation is carried out iteratively using the specified step size. Phenomena such as the development and local changes of the electric field and the depletion region, are determined at each step. The mesh adopted in this work has been properly tuned in order to be finer on the top and progressively become coarser while moving towards the bottom. The mesh definition is therefore a trade-off between simulation precision and computational time. Simulations with a SiO_2 layer on the sensor's top surface were performed to extract the I-V curves and the proper $|V_{\text{back}}|$ working point in a condition as similar as possible to the real one, since the silicon oxide layer could affect the electrical properties of the sensor [120]. From TCAD simulations of the layout shown in Fig. 4.3 with an active thickness (epitaxial plus substrate) of $100 \mu\text{m}$ [123], a capacitance of $\sim 3 \text{ fF}$ was estimated.

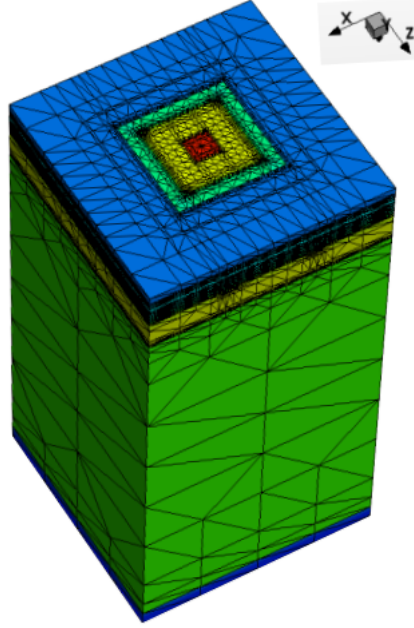


Fig. 4.4 TCAD 3D mesh on a single pixel simulation domain of the Arcadia Main Demonstrator with 50 μm thickness.

I-V simulations and power consumption investigation

As previously anticipated, the maximum voltage that can be applied to the backside electrode is limited by the punch-through. The onset of the punch-through can be estimated from the dip in the curve of the current flowing from the p-well located on the top side of the sensor, by performing a sweep of the voltage applied to the backside ($|V_{\text{back}}|$) [122], as shown in Fig. 4.5a for three different thicknesses: 50, 100 and 200 μm . The dip corresponds to the point of sign inversion from negative to positive current values in the shown absolute spectrum and indicates a delayed onset of punch-through for thicker sensors. Similarly, looking at the backside current in Fig. 4.5b, V_{pt} can be estimated as the knee of the I-V curve, where the current starts to increase. The estimated V_{pt} values are listed in Tab. 4.1.

The voltage $|V_{\text{back}}|$ to be applied as working point during TCAD simulations, has been evaluated as the voltage at which a power consumption per unit of area of 10 mW/cm^2 is reached, as this value is comparable with the electronics power consumption. The sensor power density has been computed as

$$V_{\text{pd}} = \frac{(I_{\text{pwell}} + I_{\text{nwell}}) \cdot V_{\text{back}}}{A} \quad (4.1)$$

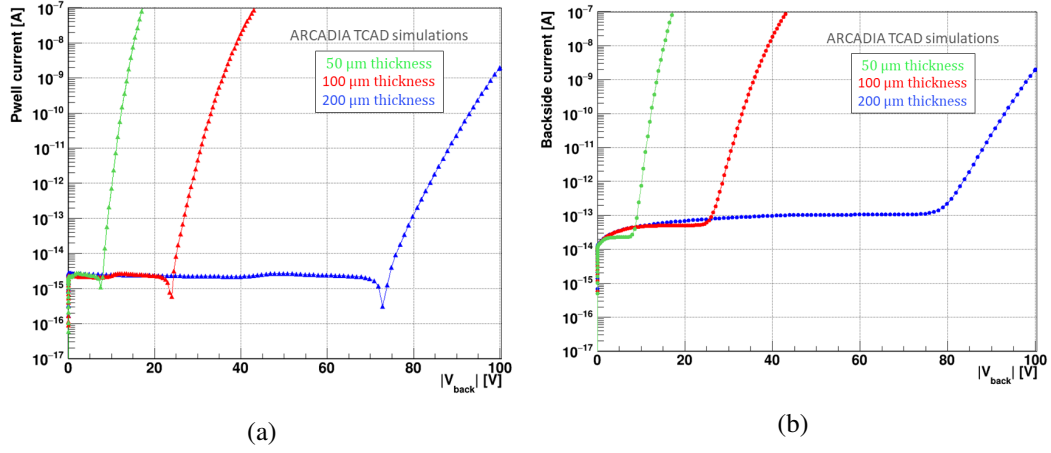


Fig. 4.5 Pwell current as function of backside voltage for three different thicknesses in different colors (a) and backside current as function of backside voltage for three different thicknesses in different colors (b).

Table 4.1 Voltage settings applied in 3D TCAD simulations.

Thickness (μm)	V _n (V)	V _{pt} (V)	V _{back} (V)
50	0.8	7.5	14.5
100	0.8	24	36.5
200	0.8	73	97

where I_{pwell} and I_{nwell} are the currents flowing at the top pwell and at the sensing node, respectively. A is the surface area of the pixel. Generally, the voltage found in this way is slightly higher than the V_{pt} , but still in an acceptable range. Fig. 4.6 shows the simulated power density as a function of $|V_{back}|$ and the agreed limit of 10 mW/cm² is highlighted. Table 4.1 summarises the voltage settings applied in TCAD quasi-stationary simulations to extract the electric field and electrostatic potential maps. These TCAD simulations were run neglecting the SiO₂ layer to save computing time, since it didn't affect the charge collection dynamics, the electric field and electrostatic potential maps needed for the subsequent Monte Carlo simulations.

As illustrated in 4.2, the electric field and electrostatic potential maps extracted from TCAD were imported in the successive step of the simulation chain: the Monte Carlo simulation.

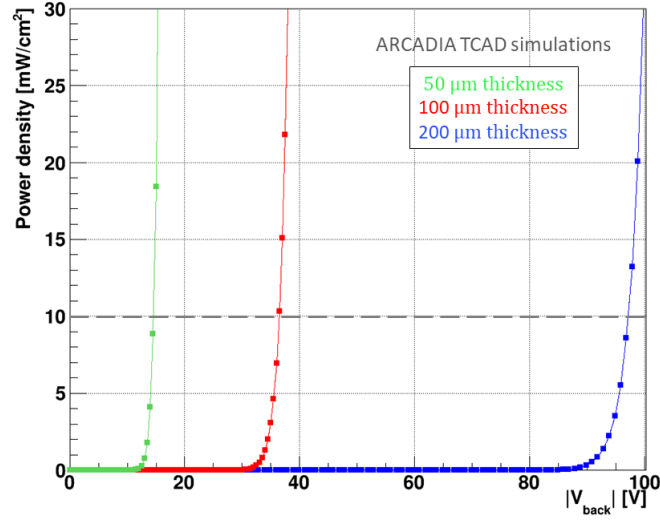


Fig. 4.6 Power consumption per unit of area. The gray dashed line indicates the limit of $10 \text{ mW}/\text{cm}^2$, comparable with the power consumption of the electronics.

4.3.3 Monte Carlo simulations

Fig. 4.7 (left) shows the electric field map of a 5×5 pixels simulation domain in which the electric field has been replicated for all the pixels that make up the matrix. On the right, the weighting potential map is illustrated, computed to simulate induced signals on neighbouring pixels [125]. The bin size in the regularly spaced grid

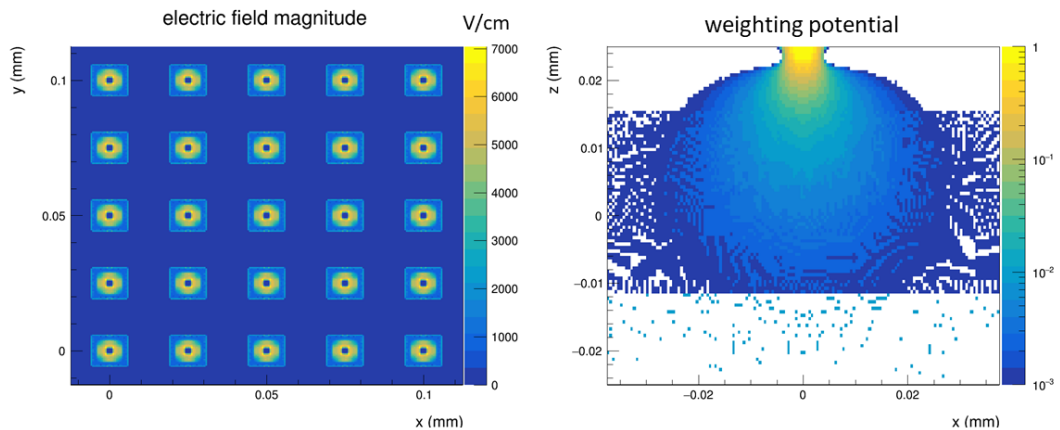


Fig. 4.7 Electric field map of a 5×5 simulation domain (left) and weighting potential map (right) with collection electrode in the center. Image source [124].

adopted in the Monte Carlo is $0.5 \mu\text{m}$ in each dimension, as a compromise between

accuracy and computing time. For the computation of the weighting potential the following approach was adopted. A 3×3 simulation domain was generated in TCAD, since the weighting potential at a distance of more than one pixel pitch normally is small enough to be neglected. The 3×3 simulated domain for the $200 \mu\text{m}$ thick sensor is displayed in Fig. 4.8. The weighting potential for the electrode of interest,

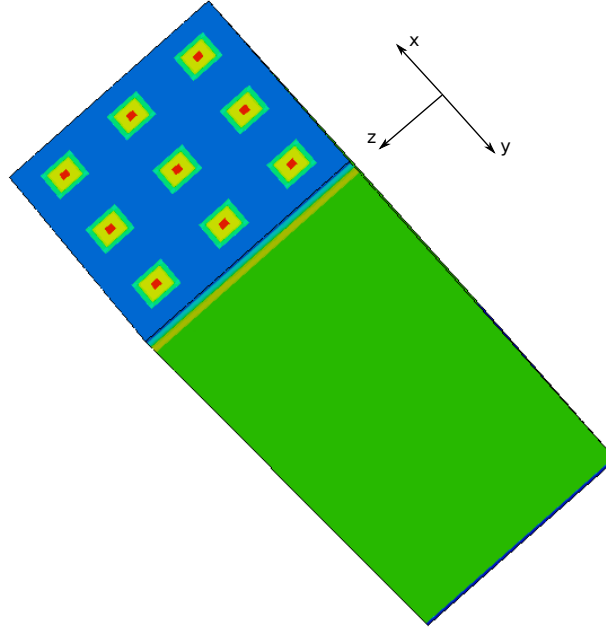


Fig. 4.8 TCAD 3×3 simulation domain for the $200 \mu\text{m}$ thick sensor, employed to extract the electrostatic potential maps and compute the weighting potential for the Monte Carlo simulation.

i.e. the readout electrode, can be computed by leaving all the electrodes at their bias voltages, adding a small voltage ΔV to the central one and then calculating the difference in the electrostatic potential [125]. Starting from these considerations, the subsequent procedure has been followed for a 3×3 pixel sub-matrix:

1. two TCAD simulations were run with a voltage applied to the central readout electrode equal to V_0 and $V_0 + \Delta V$, with $V_0 = 0.8 \text{ V}$ and $\Delta V = 0.01 \text{ V}$ (1% of the biasing voltage as rule of thumb);

2. the two electrostatic potential maps obtained have been subtracted and their difference normalised in order to obtain 1 at the electrode of interest and zero on all the others.

In Allpix², for each propagation step, the induced charge on electrode n is calculated via the Shockley-Ramo theorem (explained in detail in 1.4.2) as:

$$Q_n^{ind} = \int_{t_0}^{t_1} I_n^{ind} dt = q(\psi(x_1) - \psi(x_0)) \quad (4.2)$$

where ψ is the function describing the weighting potential displayed in Fig. 4.7 (right). Fig. 4.9 shows the 5×5 matrix collected charge for the three different sensor thicknesses. As expected, the MPV of the Landau fit to the distribution increases with increasing thickness and for a $50 \mu\text{m}$ thick device, a collected charge around 0.43 fC is expected.

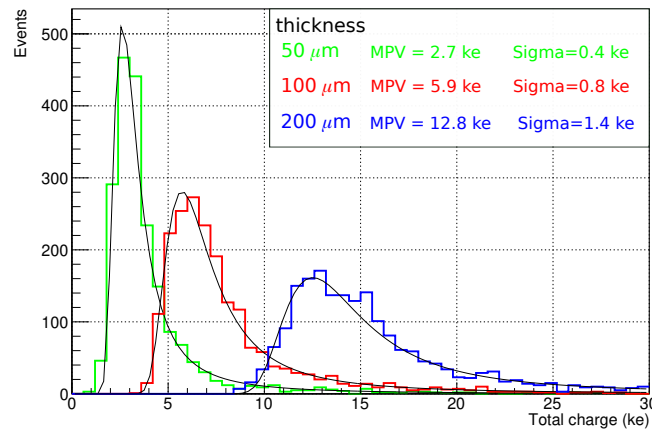


Fig. 4.9 Matrix collected charge for a 5×5 matrix of Arcadia Main Demonstrator pixels with superimposed Landau fit.

4.3.4 Cluster size results

The following simulations have been carried out by considering a source of μ^- with energy of 200 MeV, impinging uniformly on one pixel of a 21×21 simulation domain, both with perpendicular and tilted impact direction. One thousand events have been simulated in each configuration. After the charged particle crosses the active volume, it produces free charge carrier pairs by ionization, that may be shared

by several pixels. A group of adjacent pixels with a signal above a defined threshold is called a cluster.

The cluster size is defined as the number of pixels in a cluster, using a threshold of $200 e^-$. This threshold is chosen as a reasonable value to minimise the influence of readout electronic noise [119]. Starting from a perpendicular incidence configuration, the sensor was subsequently tilted at various angles ranging between 0 and 60 deg, and the cluster size distributions were analysed. Figure 4.10 illustrates the hitmaps, representing adjacent pixels in the matrix with signals above the threshold, obtained using two tilting techniques: double tilting along both the x and y axes, and single tilting along the y axis only, for different angles. These hitmaps provide a quick mapping depicting how the sensor tilting procedure influences charge collection and serve as the starting point for determining the cluster size distributions. As it can be observed, the hitmaps progressively enlarge as the tilting angle increases, indicating a first hint of increased charge sharing, as expected from geometry. In the following, the dependency of the cluster size from both geometrical and physical factors will be analysed. One thousand events have been simulated in each configuration. As a first study, the dependency of the cluster size from the tilting angle has been considered, as shown in Fig. 4.11 (left) for a sensor thickness of $100 \mu\text{m}$. As the angle increases, the average of the distribution shifts to higher cluster size. Additionally, an enlargement of the distribution can be noticed, due to a charge sharing which involves a progressively larger number of pixels.

A second analysed effect is the charge collection dependency on sensor thickness. Figure 4.11 (right) clearly demonstrates the trend of increasing average cluster size with sensor thickness at a fixed tilting angle of 20 degrees. This result can be attributed to the larger projection of particle tracks on the sensor surface as the thickness increases, as well as to the lateral diffusion of charge carriers during the charge collection process.

To summarise the cluster size studies conducted on the ARCADIA Main Demonstrator CMOS pixel sensor, Fig. 4.12 illustrates the trend of the cluster size as a function of the tilting angle, for a threshold set to $200 e^-$. Three thicknesses are considered and both the single (dashed line) and double tilting (solid line) simulation results are displayed. The shown cluster size is the average of the distribution of 1000 events simulated in that particular configuration. The error bars represent the

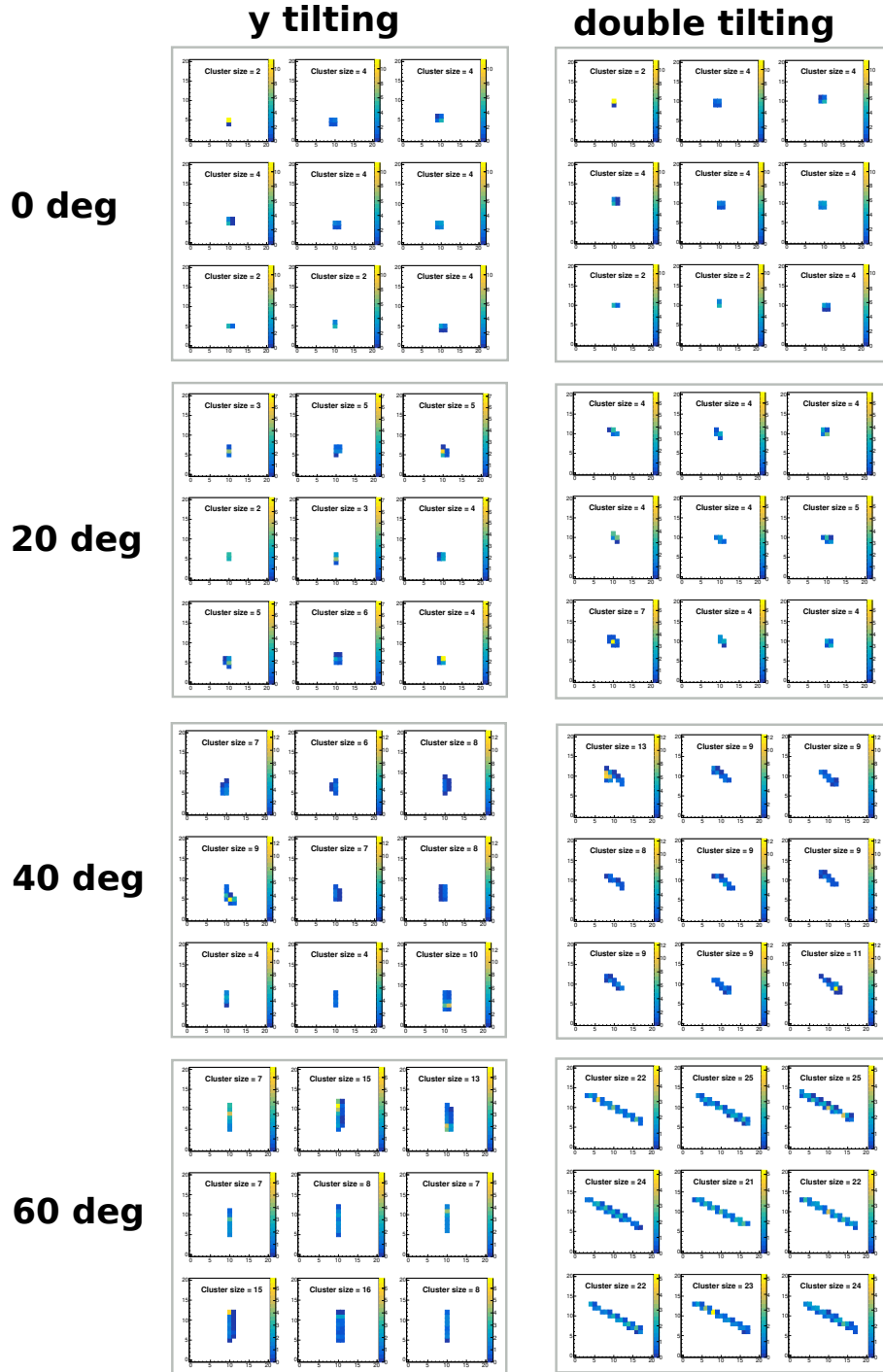


Fig. 4.10 Hitmaps obtained with a threshold of $200 e^-$ for a sensor thickness of $100 \mu\text{m}$. The first column shows the results from the y-tilted sensor, while the second column makes reference to double tilted sensor on both x and y axes. Different tilting angles are indicated on the left of each figure. Image source [124].

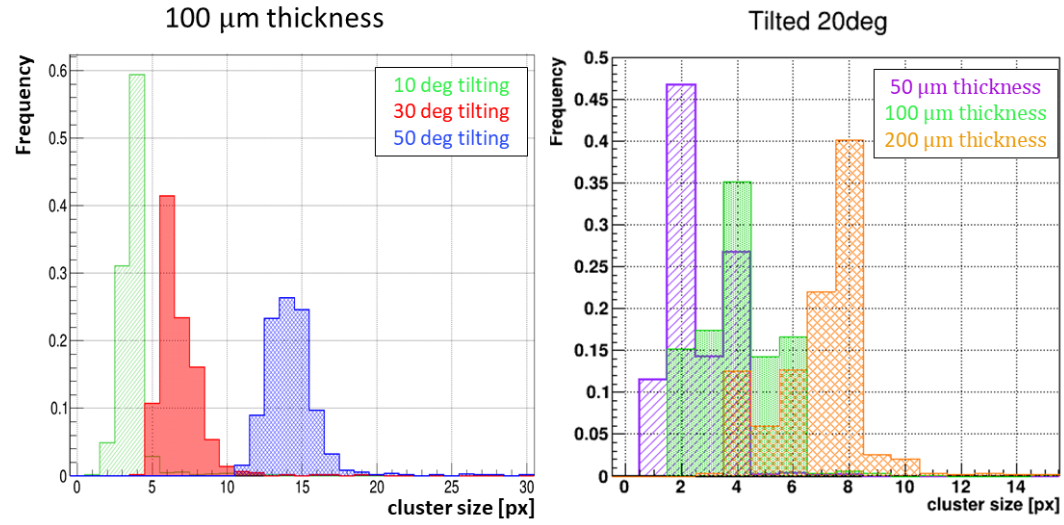


Fig. 4.11 Cluster size distributions for a sensor thickness of 100 μm for three different tilting angles. The plot makes reference to the double tilting procedure (left). Cluster size distributions for three different sensor thicknesses for a 20 deg double tilted sensor (right). Image source [124].

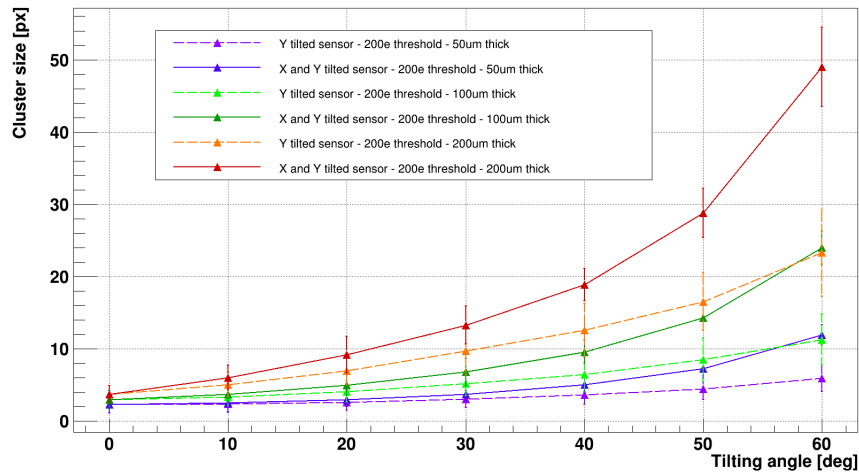


Fig. 4.12 Average cluster size as function of the tilting angle for three different sensor thicknesses with a fixed threshold of 200 e^- . The double tilting technique is shown in solid line, while the y-tilting is displayed in dashed line. Image source [124].

standard deviations of the cluster size distributions. The average cluster size obtained with a perpendicular impinging scenario, is a maximum of 4 pixels, while it increases with both the tilting angle and the thickness. At high tilting angles, the cluster size increase could mainly be justified by the geometrical configuration and a maximum value ~ 50 pixels is reached for a 200 μm thick sensor with a double tilting of

60 degree.

The above presented results, together with the computed charge collection efficiency (see App. B.2), offer some initial and significant insights into the tracking performance of the Arcadia Main Demonstrator pixel sensor with $25\ \mu\text{m}$ pitch, investigating its capabilities for radiation detection applications.

4.3.5 Time resolution

The sensor time resolution has been simulated by considering MIPs crossing the central pixel of a 5×5 matrix. In particular, a square source of 200 MeV muons was employed, with tracks impinging perpendicularly to the sensor surface and uniformly distributed across the pixel area (x,y initial coordinates randomly extracted from a uniform distribution over the pixel surface). For every event, the following procedure was adopted:

- the current signal was integrated to obtain the collected charge as a function of time;
- subsequently, the charge was normalised to the total amount of collected charge in that event;
- thresholds have been applied as constant fractions (hereafter called CFD) of the total collected charge, as shown in Fig. 4.13. It illustrates the normalised collected charge curves for a subset of the 2000 simulated events on a $50\ \mu\text{m}$ thick sensor. The same plot obtained for the $200\ \mu\text{m}$ thick sensor is shown in Fig. 4.14.

The time resolution has been evaluated by considering as an estimator the standard deviation of the crossing time distribution corresponding to each applied threshold. Comparing figures 4.13 and 4.14, it's already possible to guess some detail on the time resolution for the two sensor thicknesses. The collected charge curves of the "slow events", colored in red, look very similar for the two thicknesses and, for example, the slowest curves cross the 60% threshold around 10 ns in both cases. However, the $50\ \mu\text{m}$ thick sensor shows a fast population featuring steeper collected charge curves, as in this case the drift length is smaller.

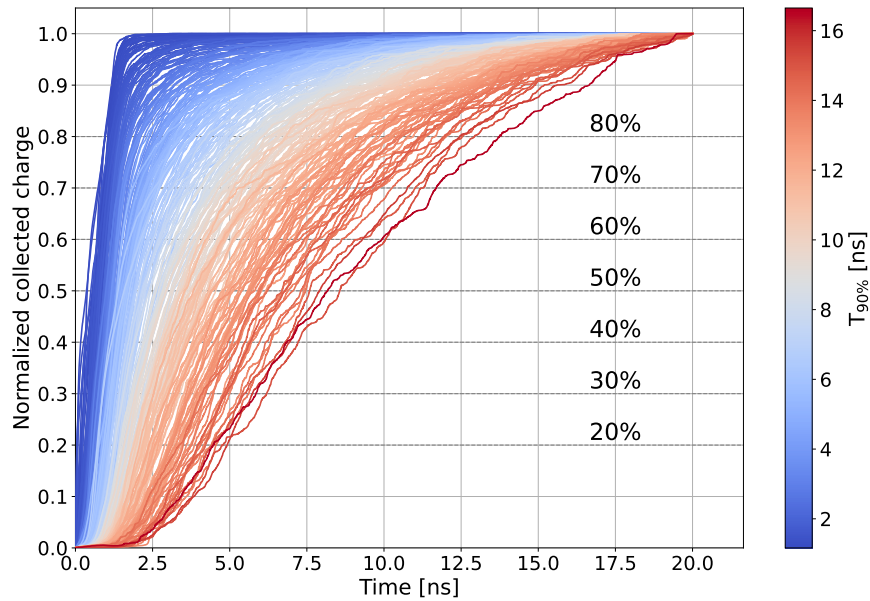


Fig. 4.13 Collected and normalized charge as a function of time for a subset of 300 out of 2000 simulated events on the 50 μm thick Arcadia Main Demonstrator. The color scale indicates the time at which the 90 % of the total charge is collected.

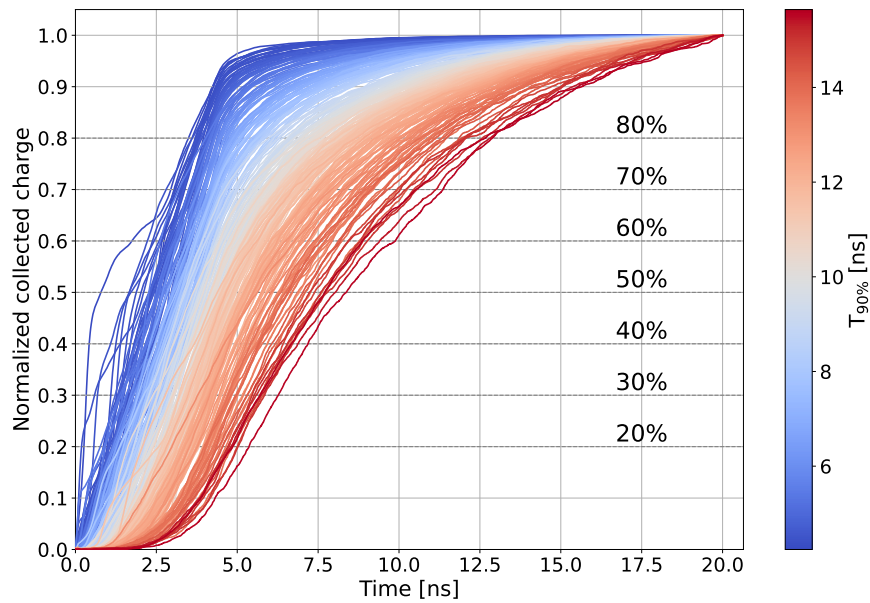


Fig. 4.14 Collected and normalized charge as a function of time for a subset of 300 out of 2000 simulated events on the 200 μm thick Arcadia Main Demonstrator. The color scale indicates the time at which the 90 % of the total charge is collected.

Fig. 4.15 (left) displays the time resolution for the three simulated sensor thicknesses, varying the applied constant fraction. As can be observed, the time resolution

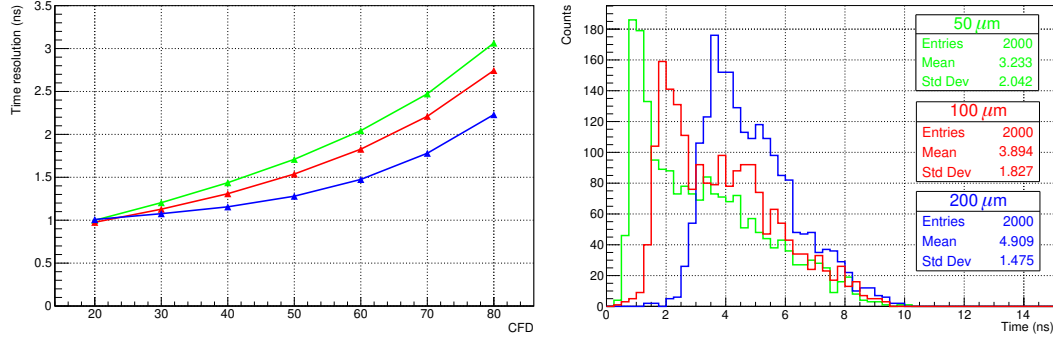


Fig. 4.15 Time resolution of the Arcadia Main Demonstrator with different thicknesses as a function of the fraction applied on the collected charge (left). Crossing time distribution at 60% of the total collected charge for the 50 μm , 100 μm and 200 μm thicknesses (right).

improves with the sensor thickness. This result can be understood by looking at the crossing time distributions, considering, as an example, the 60% threshold, in Fig. 4.15 (right). For the 50 μm thick sensor, the crossing time distribution at 60% shows a double population: a faster one, responsible for the first peak located at small crossing times and a second, broader, population, representing slower signals. On the other hand, the 200 μm thick sensor shows a narrower distribution, even if with a higher average crossing time. This effect is due to the difference in drift time of the generated e-h pairs in the detector volume. The slowest carriers are those generated at the interface between two or more pixels, and their drift time, in that case, is limited by the small lateral component of the electric field under the surface, which remains the same for different thicknesses. This determines the slow side of the distribution, which is thus not strongly dependent on the thickness. On the other hand, the fastest carriers are those generated at the center of the pixel and they are collected faster in the 50 μm thick sensor compared to the 200 μm . As a consequence, the fact that the fastest carriers for the 200 μm thick sensor are slower with respect to the 50 μm , helps to uniform the distribution, while the speed of the fastest carriers in the 50 μm thick sensor is counterproductive, as it increases the non-uniformity of the crossing time.

Illumination window scan

To better visualise the above-guessed effect of different carriers' drift time in the detector volume, Fig. 4.16a shows, for the $50\text{ }\mu\text{m}$ thick sensor, the crossing time distribution at 60% threshold, obtained by illuminating a progressively smaller area of the sensor surface, in order to suppress slow events and consider only the fast ones. As expected, the distribution gradually shrinks and the slow population of events is suppressed. For the smallest impinging area of $(5 \times 5)\text{ }\mu\text{m}^2$ a Gaussian fit is also superimposed to the crossing time distribution.

Fig. 4.16b illustrates the whole time resolution trend as a function of the applied threshold. For the $(5 \times 5)\text{ }\mu\text{m}^2$ illumination window, the sigma of a Gaussian fit to the crossing time distributions can also be employed as an estimator of the time resolution and its value is shown in light blue in Fig. 4.16b. Except for the last point with threshold 80%, using the standard deviation of the histogram overestimates by $\sim 10\%$ the time resolution obtained with the standard deviation of a Gaussian fit. This last estimator will be employed, when possible, in the following work.

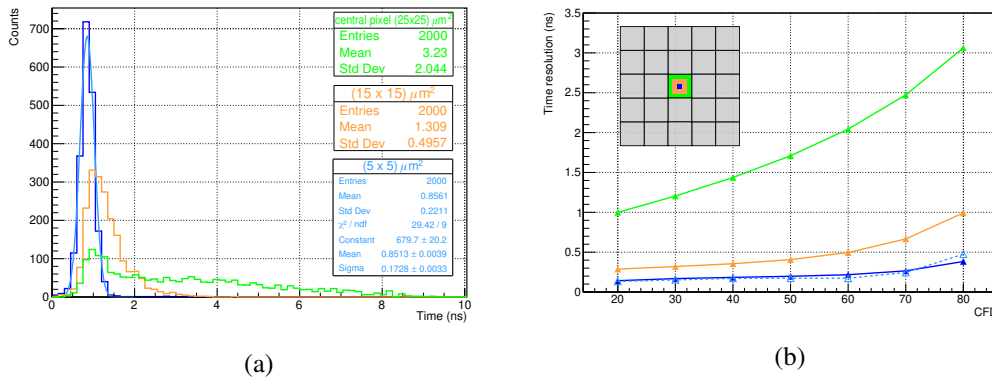


Fig. 4.16 Crossing time distributions at 60% of the total collected charge for the $50\text{ }\mu\text{m}$ thickness comparing the different illumination windows in different colours (a). Time resolution for the $50\text{ }\mu\text{m}$ thick sensor as a function of the threshold applied on the collected charge and for different illumination windows (b): central pixel in green, $(15 \times 15)\text{ }\mu\text{m}^2$ in orange, $(5 \times 5)\text{ }\mu\text{m}^2$ in blue with superimposed sigma from the Gaussian fit (light blue).

4.4 ARCADIA FD-MAPS with large collection electrode

In order to improve the time resolution of monolithic pixel sensors, the ARCADIA collaboration developed pad diodes with a large area collection electrode, covering $\sim 70\%$ of the surface area [126]. The pixel is a modification of the ARCADIA Main Demonstrator pixel and is therefore implemented in the same n-on-n process with a low resistivity epitaxial layer. A backside boron-doped region is implemented with backside lithography and allows a full depletion of the sensor volume.

In this chapter, the timing performance of pad diodes with pixel pitches ranging from $50\text{ }\mu\text{m}$ to $200\text{ }\mu\text{m}$ and different thicknesses will be presented and discussed in view of the possible applications. As described in [14], an optimal w/d ratio exists to optimise the time performance of a silicon detector, being w the width of the collection electrode and d the thickness. For this purpose, a systematic investigation of the field uniformity has been conducted with different geometries of the pads and the simulations have been carried out in collaboration with Greta Andrini ¹.

4.4.1 TCAD simulations

The adopted methodology is the same applied for the Main Demonstrator, combining a 3D TCAD simulation with the Monte Carlo software Allpix². Fig. 4.17 shows a single pixel TCAD simulation domain with a width and a thickness of $50\text{ }\mu\text{m}$. In this case the collection electrode is $(42 \times 42)\text{ }\mu\text{m}^2$ in area and was progressively increased together with the pixel pitch, in order to preserve the proportionality. The perimeter of the pixel features a $4\text{ }\mu\text{m}$ wide deep-p-well and, together with the ones of the neighbouring pixels, provides an $8\text{ }\mu\text{m}$ wide region that can potentially host the electronics. In order to find the optimal working point, I-V curves have been simulated varying the voltage applied to the backside electrode, as explained in 4.3.2 and shown in Fig. 4.18. From the aforementioned curves, the voltage corresponding to the punch-through onset was assessed. In all the simulations, the voltage applied to the p-well was always kept at 0 V. Again, the voltage applied in the simulation to the backside electrode has been estimated as the voltage at which a power consumption

¹Politecnico di Torino and INFN Torino.

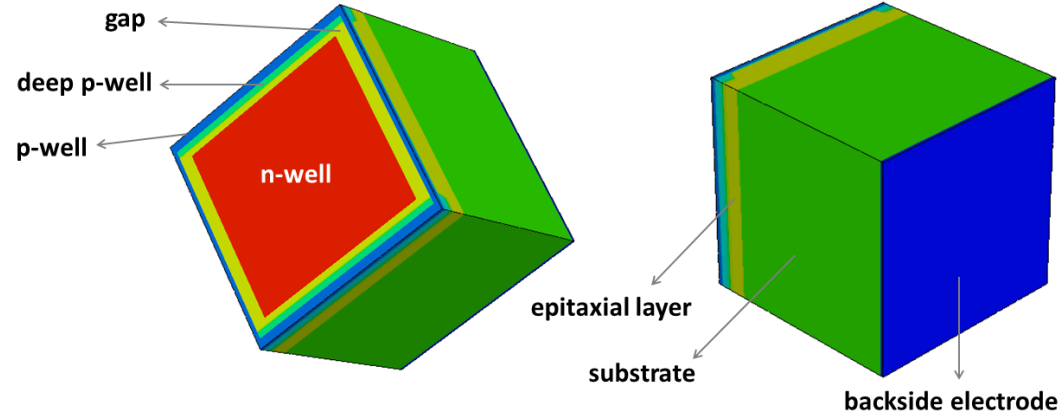


Fig. 4.17 3D TCAD simulation domain of a single pixel MAPS with large collection electrode. The dimensions are $50\ \mu\text{m}$ pitch, $50\ \mu\text{m}$ thickness and the collection electrode is $(42 \times 42)\ \mu\text{m}^2$.

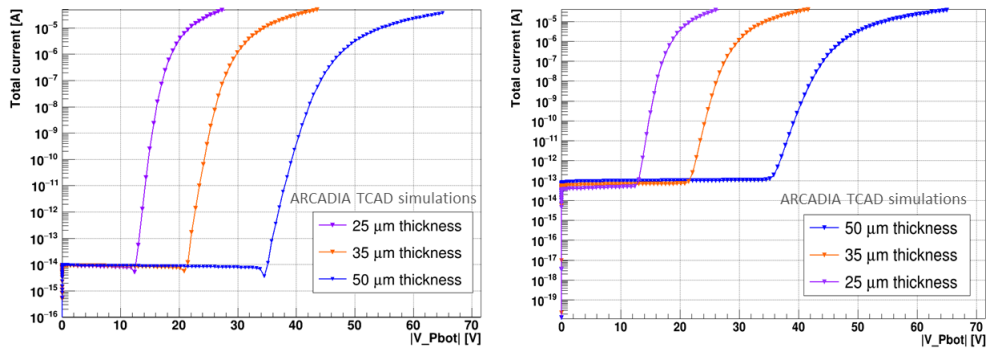


Fig. 4.18 Total current from the top p electrode (left) and from the bottom electrode (right) for the $50\ \mu\text{m}$ pitch pixel and different thicknesses. Image source [126].

per unit of area of $10\ \text{mW}/\text{cm}^2$ is reached, as shown in Fig. 4.19. The same study has been repeated also for the 100 , 150 and $200\ \mu\text{m}$ pitches.

Table 4.2 summarises the voltages at which the sensors have been operated during the simulations. In particular, the top electrode voltage V_n , the punch-through estimated voltage V_{pt} and the backside electrode voltage V_{back} . For all the pixel pitches, three thicknesses have been simulated: $50\ \mu\text{m}$, $35\ \mu\text{m}$ and $25\ \mu\text{m}$. The simulated sensor capacitance, representing the input capacitance for the front-end electronics, is $\approx 35\ \text{fF}$ for the $50\ \mu\text{m}$ pitch and ranges between 75 - $200\ \text{fF}$ for pixel pitches larger than $100\ \mu\text{m}$ [127].

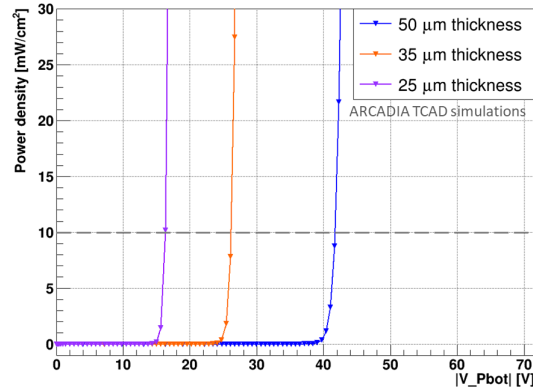


Fig. 4.19 Power density as a function of the voltage applied at the backside electrode for the 50 μm pitch pixel and different thicknesses.

Table 4.2 Voltage settings for the 50, 100, 150 and 200 μm pitch and different sensor thicknesses applied in 3D TCAD simulations.

Pixel pitch (μm)	Thickness (μm)	V_n (V)	V_{pt} (V)	$ V_{\text{back}} $ (V)
50	50	3.3	34.5	41.7
50	35	3.3	20.8	26.2
50	25	3.3	12.4	16.3
100	50	3.3	35.2	43
100	35	3.3	22.1	27.4
100	25	3.3	12.4	16.8
150	50	3.3	35.2	43.7
150	35	3.3	22.1	27.9
150	25	3.3	12.4	17.1
200	50	3.3	35.8	44.4
200	35	3.3	22.6	29.0
200	25	3.3	13.0	17.5

4.4.2 Investigation on the weighting potential uniformity

To evaluate the time performance of FD-MAPS with large collection electrode, some preliminary investigations on the weighting potential have been carried out. The applied procedure in the Monte Carlo simulations is the same adopted for the Main Demonstrator (see 4.3.3), starting from the extraction of the electrostatic potential maps from TCAD and the computation of the weighting potential. Fig. 4.20 shows the electrostatic potential and the weighting potential computed for a 3×3 matrix for the 50 μm pixel pitch and 50 μm thickness. A preliminary comparison with the

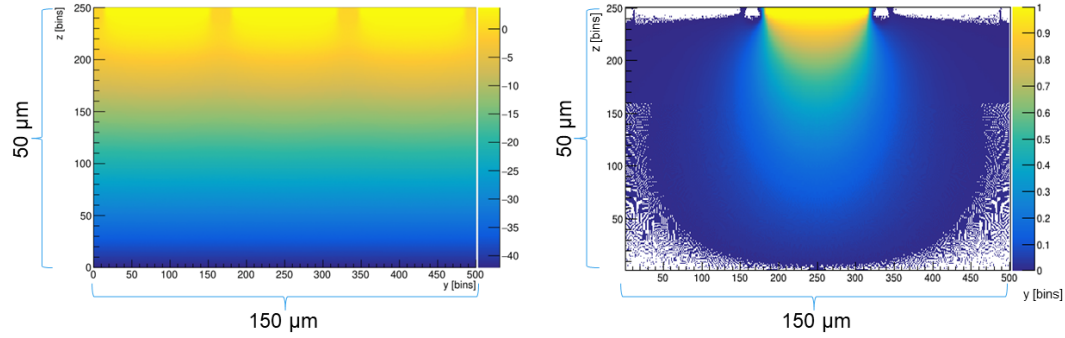


Fig. 4.20 Electrostatic potential (left) and weighting potential (right) 2D maps for a 3×3 sub-matrix. The sensor thickness and the pixel pitch are $50 \mu\text{m}$.

weighting potential calculated for the sensor with a small collecting electrode, shown in Fig. 4.7, clearly demonstrates the increased uniformity achieved by modifying the pixel geometry. This suggests a corresponding reduction in the distortion term affecting timing performance.

Comparing then the weighting potential profiles for three different pitches, keeping fixed the thickness at $50 \mu\text{m}$, it's possible to guess how the distortion component, presented in 2.1, can influence the time resolution in a different way, depending on the pixel pitch and, therefore, on the w/d ratio. From Fig. 4.21 it appears clearly that

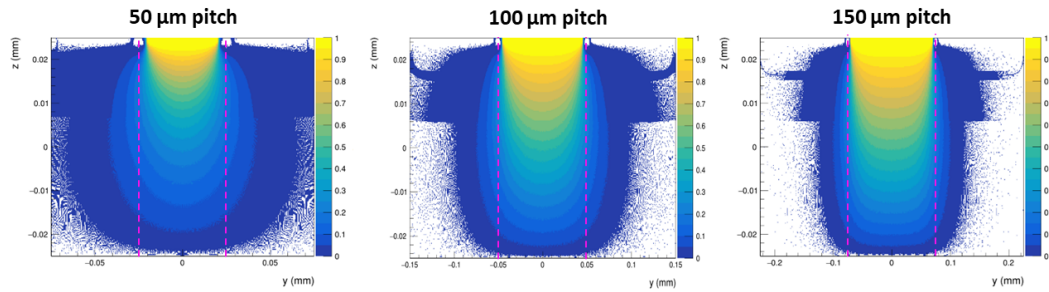


Fig. 4.21 Weighting potential profile for a 3×3 submatrix for pixel pitch 50, 100 and $150 \mu\text{m}$. The pink dashed lines represent the boundary of 1 single pixel, which allows to compare more easily the three profiles.

the $50 \mu\text{m}$ pitch exhibits a more spherical weighting potential profile on the backside, which turns into a more planar profile for larger pixel pitches. More quantitatively, one can compare the weighting potential profile along the sensor thickness for the three different pitches, as displayed in Fig. 4.22. The $50 \mu\text{m}$ pitch exhibits a non-linear profile with the thickness and it differs noticeably from the larger pixel pitches. This behaviour can be justified by edge effects, which are more visible in

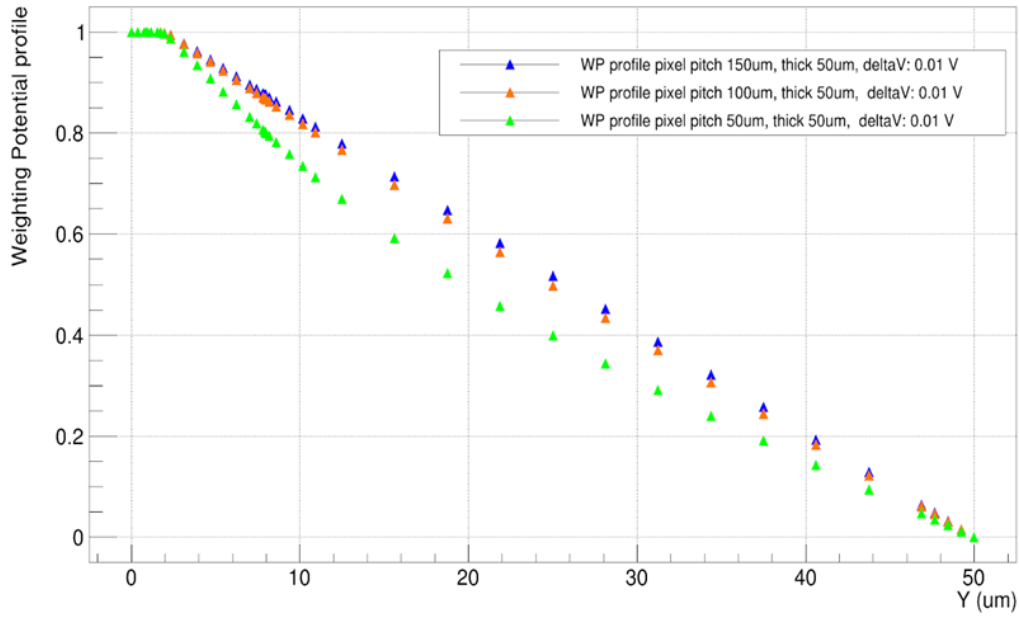


Fig. 4.22 Weighting Potential profile extracted along a vertical line in the center of the 3×3 simulation domain for 50, 100 and $150 \mu\text{m}$ pixel pitch in different colors. The y coordinate in TCAD represents the sensor thickness.

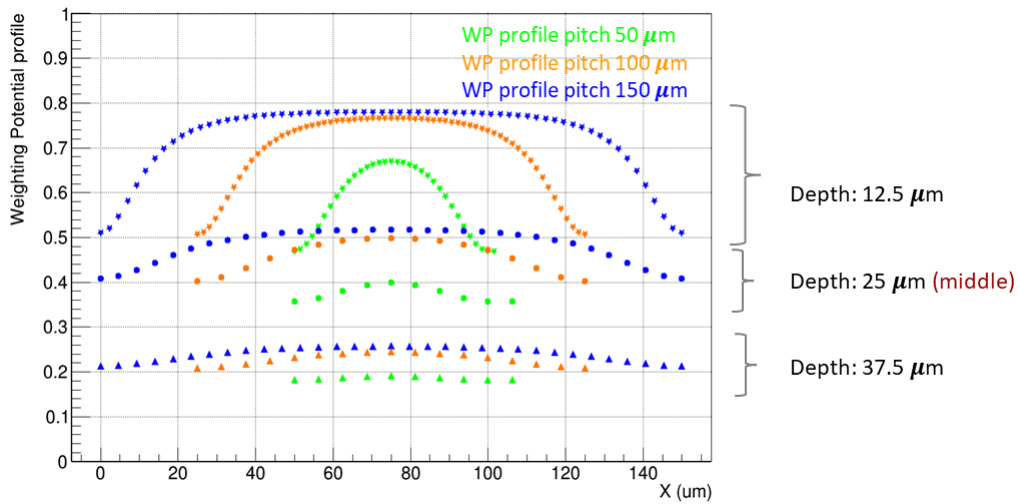


Fig. 4.23 Weighting potential investigation along the x transverse coordinate for 50, 100 and $150 \mu\text{m}$ pitch in different colors

small pixel pitches, where the border has a larger weight and progressively disappear moving to larger pitches. This will have an impact on the time resolution, as it will be shown in the following section. Fig. 4.23 illustrates the weighting potential

profile along the x coordinate (transverse coordinate in TCAD) computed at different sensor depth. For every depth, it's possible to notice the more roundish profile for the $50\ \mu\text{m}$ pixel pitch, that becomes progressively more planar moving to 100 and $150\ \mu\text{m}$ pitches. The uniformity of the weighting potential is a key element in the time resolution of silicon sensors, as it is expressed from the distortion term. From the studies presented above, it's already possible to state that larger pixel pitches will lead to an improved distortion component of the time resolution.

4.4.3 Time resolution

In order to estimate the time resolution, the approach described in 4.3.5 has been followed. Starting from the induced signal on the collection electrode, the collected charge as a function of time is computed and then normalised to the total collected charge in that particular event. After performing this procedure for every event, thresholds are applied. They correspond to fractions of the total normalised collected charge, as shown in Fig. 4.24a and 4.24b with an applied 60% threshold.

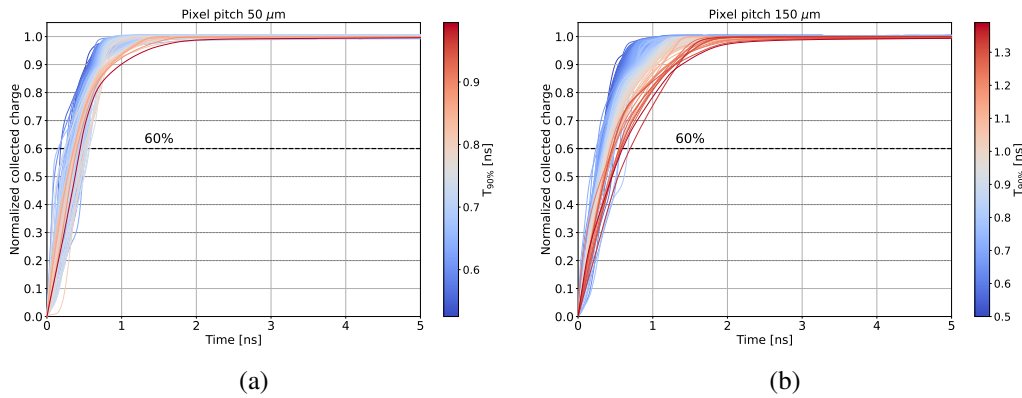


Fig. 4.24 Normalised collected charge curves as a function of time for a subset of 300 out of 10000 simulated events for the $50\ \mu\text{m}$ pitch (a) and $150\ \mu\text{m}$ pitch sensors (b) with applied threshold at 60% of the total collected charge. The thickness is $50\ \mu\text{m}$. The color scale indicates the time at which the 90 % of the total charge is collected.

Ten thousands events have been simulated for this study in every configuration (i.e for every pixel pitch and thickness). A Gaussian fit within a $(-3\sigma, +\sigma)$ interval has been performed on the crossing time distributions extracted at the different

applied thresholds ². The standard deviation σ of this fit provides the estimator for the time resolution, as displayed in Fig. 4.25 for the 60% threshold.

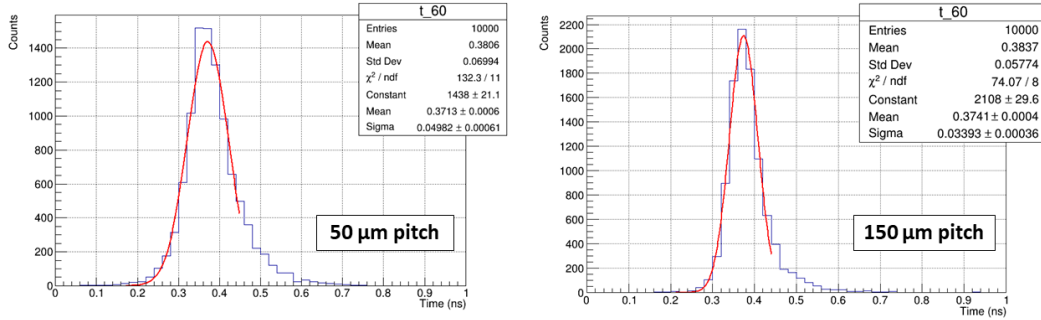


Fig. 4.25 Crossing time distributions for the 50 μm pitch (left) and 150 μm pitch (right) with applied threshold at 60% of the total collected charge. The thickness is 50 μm .

Fig. 4.26 summarises the results obtained from the simulation campaign of FD-MAPS in 110 nm CMOS process with large collection electrode, pixel pitch ranging from 50 μm to 200 μm and 25, 35 and 50 μm thicknesses. It's clear that for 25 μm thickness and below, sensors with pixel pitch $\geq 100 \mu\text{m}$ are suitable for optimal timing resolution. One can notice that around 70 or 80% of threshold, the time resolution for the 50 μm pitch improves and becomes lower than the one obtained for larger pixel pitches. This trend is confirmed by looking back at Fig. 4.24a, where it's easy to see a shrink, for the 50 μm pitch, in the collected charge curves for higher thresholds with respect to the 150 μm . The effect is limited to the final part of the charge collection and is therefore dominated by holes, which are slower than electrons. The cause of the detected effect lies in the weighting potential itself: a weighting field that drops to zero more rapidly when moving from the surface of the device to the back, as in the case of a 50 μm pitch (see Fig. 4.21), improves the timing resolution for very high CFD values and significantly worsens it for low CFD values. In other words, the tail of the signal, due to holes, has less influence if the weighting field at the back is significantly reduced. See also App. B.3 for more details.

Fig. 4.27 shows the time resolution as a function of the applied threshold by varying the sensor thickness, with a fixed pixel pitch of 50 μm . The time resolution strongly improves with decreasing thickness, reaching impressive values below 20 ps

²The crossing time distributions feature an asymmetric shape with a tail on the right, which can be explained by noting that a time measurement based on a constant amplitude fraction suppresses time walk only when the signal shape remains constant [7].

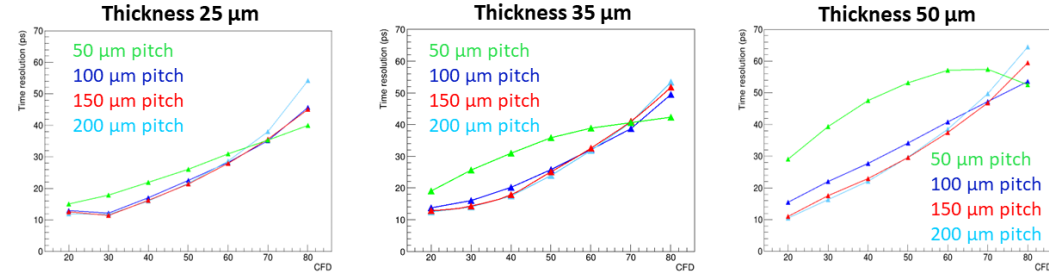


Fig. 4.26 Simulated time resolution of ARCADIA FD-MAPS with large collection electrode. Pixel pitches 50, 100, 150 and 200 μm and thicknesses 25, 35 and 50 μm.

for the 25 μm thick sensor. The lower time resolution with thinner sensors can be attributed to a smaller Landau contribution, due to the reduced number of generated charge carriers in the active sensor thickness.

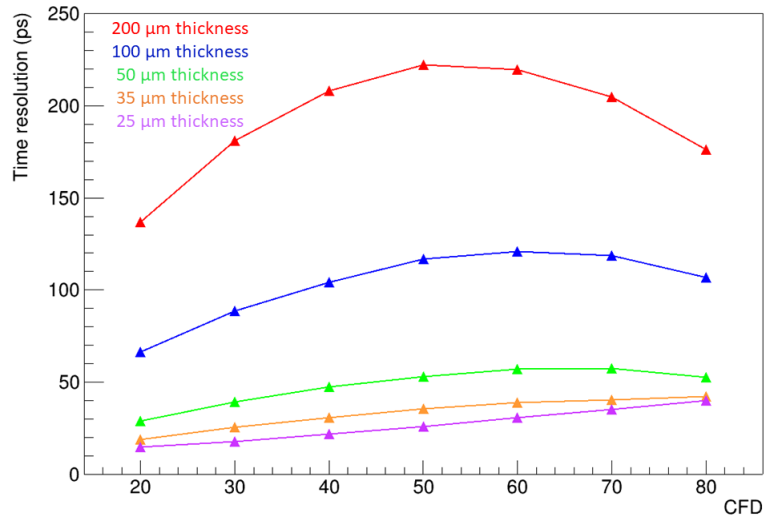


Fig. 4.27 Simulated time resolution of ARCADIA FD-MAPS with large collection electrode as a function of the applied threshold and for different thicknesses. Pixel pitch 50 μm.

4.4.4 The HERMES prototype in 110 nm CMOS process

Integrated electronics to readout the sensors has been designed by Stefano Durando³ and fabricated in the HERMES prototype [128] [129]. The active matrix is composed by 16×24 pixels. Each pixel is (50 × 50) μm² and the tested prototype features

³INFN Torino

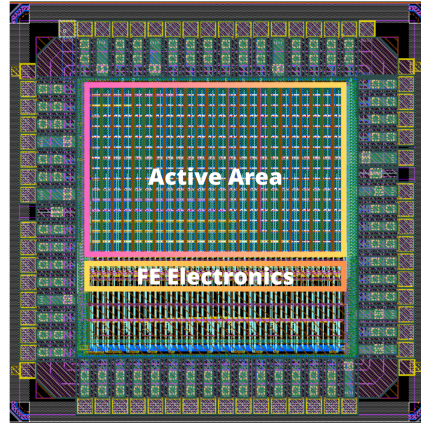


Fig. 4.28 HERMES prototype chip layout. The active area and the section of the chip hosting the front-end electronics are highlighted. The pixel pitch is $50\ \mu\text{m}$ [128].

a $48\ \mu\text{m}$ active thickness. The HERMES prototype is $(2 \times 2)\ \text{mm}^2$ large. Each HERMES channel comprises a Charge Sensitive Amplifier (CSA) that is DC coupled to the sensor electrode and is implemented with 3.3 V transistors. This choice was driven by the need to bias the collection node at a voltage larger than 1.2 V. Indeed, the bias to the collection node is provided by the amplifier feedback, which sets the voltage to $\sim 2.6\ \text{V}$. The preamplifier output is then AC coupled to a 1.2 V transistor discriminator. Every channel reads eight parallel pixels of the same column (one sub-column), resulting in a total detector capacitance of 280 fF. In this prototype, the channel has been developed in the column periphery, because of the amplifier size. For more details on the electronics see [128]. A picture of the chip layout is shown in Fig. 4.28.

Laboratory characterisation

The HERMES chip was characterised in laboratory and it was configured, controlled and readout with a Xilinx FPGA Board. The sensor with an active thickness of $48\ \mu\text{m}$ was tested with the Transient Current Technique (TCT) to investigate the electronics jitter. The laser spot was focused at the center of the pixel, neglecting in this way the distortion term of the time resolution in Eq. 2.1, due to the non-uniformity of the weighting field. With this measurements also the Landau term can be neglected and the electronics jitter component of the time resolution can be evaluated. Moreover, measurements with a ^{90}Sr source have been performed to extract the MPV of the amplitude distribution. In this way, the response to MIPs is evaluated by detecting

the e^- produced in the ^{90}Sr decay ⁴ and for the 48 μm thick sensor the measured MPV was (76.2 ± 0.6) mV (see App. B.4). From a proper matching with the CAD simulations, it was possible to retrieve the charge integrated at the sensor node, i.e. ~ 0.5 fC for a 48 μm thick sensor. The found result is in line with expectations from the Bichsel model (see 1.3.1), considering 65 e-h pairs deposited per μm , resulting in 3120 e^- in 48 μm active thickness.

Figure 4.29 shows the jitter as a function of the estimated injected charge by varying the intensity of the laser. The jitter component for this specific sensor thickness is around 900 ps (highlighted with a blue circle in the plot).

As a consequence, in this prototype, the time resolution is significantly dominated

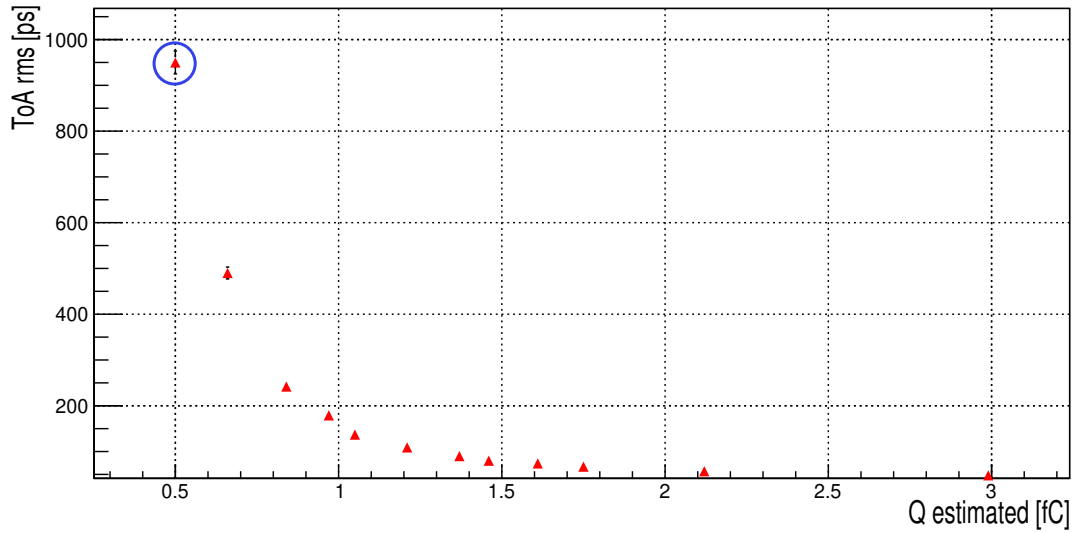


Fig. 4.29 Jitter measurement for the HERMES prototype with pixel pitch 50 μm and thickness 48 μm . Courtesy of S. Durando [128].

by the electronics jitter. To improve it, one has to address either the input charge or the amplification stage, which is directly linked to the power consumption.

To this end, one possible approach is to increase the sensor thickness, for example to 100 μm , in order to enhance the collected charge, improving the SNR ratio and, consequently, the time resolution. The MPV for a MIP in a 100 μm thick sensor is around 1.1 fC, resulting in a jitter contribution around 100 ps (see Fig. 4.29), together with a sensor time resolution component between 70 ps and 120 ps, depending on the

⁴The ^{90}Sr isotope undergoes a β^- decay with a 0.546 MeV energy distributed among the ^{90}Y isotope, an antineutrino and a detectable electron. The ^{90}Y again undergoes a β decay into ^{90}Zr , emitting electrons with a maximum energy of 2.28 MeV. Studying the detected electrons from the ^{90}Sr and ^{90}Y decays allows for the analysis of the sensor response to MIPs.

CFD considered (blue curve in Fig. 4.27). For this reason, the whole time resolution is not expected to be better than 100 ps with a 100 μm thick sensor.

Another approach to improve the time resolution of the chip involves the optimization of the amplification stage. In particular, increasing the transconductance of the input transistor can help to minimise the noise in the transistor channel. However, this improvement comes at the cost of increased power dissipation. The power consumption of the prototype is mainly due to the amplification stage, consuming 450 μA at 3.3 V power supply, bringing to a power consumption $\sim 1.4 \text{ mW/ch}$, remembering that one channel includes 8 pixels and therefore covers an area of $(50 \times 400) \mu\text{m}^2$. It is worth mentioning that the focus of the presented prototype was on assessing the overall timing performance, rather than on optimizing the power density. More details on the prototype characterisation measurements can be found in [128].

From the above stated considerations, it starts to become clear that to reduce the jitter component below 50 ps, a collected charge equal or higher than 3 fC is needed, together with a more performant preamplifier, employing 1.2 V transistors. The sensor must be optimised in order to be thin enough to reach a good timing performance (as expected from Fig. 4.27), but at the same time, collecting enough charge to reduce the jitter contribution. This target, combined with the need of a moderate power consumption, led to a new sensor concept with the addition of a gain layer, as already implemented in hybrid sensors as LGADs. The details on the new ARCADIA sensors with gain layer are presented in the next chapter.

Chapter 5

ARCADIA Fully Depleted CMOS sensors with gain layer

As delineated in 2.1, there are two main contributions to the time resolution of silicon pixel detectors. The first is the intrinsic timing performance of the sensor itself, depending on the geometry, on the uniformity of the weighting potential, and on the charge deposition mechanism. The second is represented by the jitter of the readout electronics, strongly dependent on the SNR. Since the electronics power consumption is limited in practical applications, the SNR has to be improved with an alternative approach. To reach this goal, several groups proposed to include a gain layer in CMOS sensors, for example in the the MONOLITH project, described in 3.5.4.

This chapter reports on a new CMOS sensor concept, developed in the framework of the ARCADIA collaboration, including an avalanche multiplication layer, able to amplify the signals generated by impinging charge particles. The devices presented in the following are also labelled as CMOS-LGADs and, thanks to their promising performance, combined with reduced production expenses, are now regarded as the baseline technology for the TOF detector of the ALICE 3 experiment (see 2.4.2).

The author performed the Monte Carlo simulations shown in the following, together with the consequent analysis. Moreover, the author personally participated in all the measurements here presented, giving a significant contribution in the data analysis of the test beam data published in [130]. All the work was carried out in collaboration with the ALICE 3 TOF working group.

5.1 The sensor concept

Starting from the promising results obtained from combined TCAD and Monte Carlo simulations of FD-MAPS with large area collection electrodes, presented in 4.4.3, the ARCADIA collaboration designed a backside-biased FD-MAPS with the addition of a gain layer implant underneath the collection electrode [131][132]. The sensors' design is based on a modified 110 nm CMOS process and aims to accomplish sub-nanosecond time resolution. The challenging requirements driving

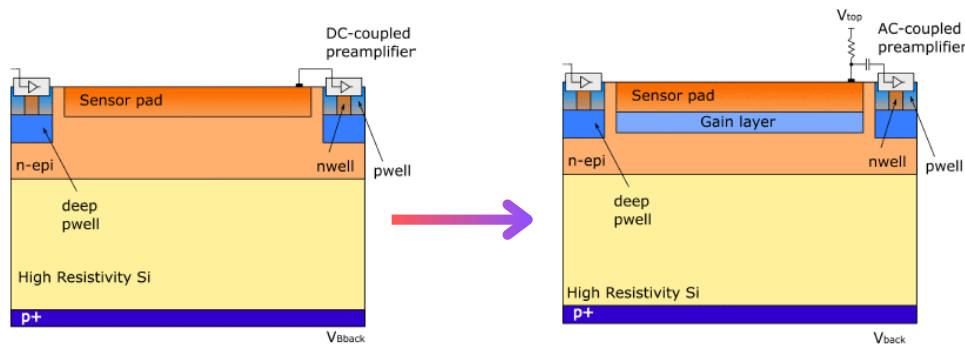


Fig. 5.1 Schematic cross section of a DC coupled pixel without gain (left) and an AC coupled pixel with gain (right). Image source [131].

the sensor and electronics design are the following:

- guarantee a fast charge collection, thanks to the uniform electric field shape and a uniform weighting potential;
- increase the SNR, collecting enough charge to reduce the jitter contribution (see Fig. 4.29);
- minimise the power consumption.

Fig. 5.1 illustrates the ARCADIA sensor concept with large collection electrode before and after the addition of the gain layer. The figure on the left shows a DC coupled sensor with large collection electrode and without gain layer, while on the right, an AC-coupled sensor with added gain implant, in blue, is outlined. The gain layer is made of a p+ implant and has the aim to generate a high electric field, enabling charge multiplication by impact ionization, as explained in 3.5.1 for LGADs. Indeed, thanks to the gain layer, a localised electric field peak in the order of 300-400 kV/cm, triggers the impact ionization in silicon [133]. The substrate

includes a high resistivity n-type epitaxial layer, on top of which a second, thin, n-type epitaxial layer is grown. These two volumes make up the active region of the sensor. They are grown on a p+ silicon wafer, constituting the p-n junction allowing the sensor's depletion.

Two voltages are applied to the sensor:

- a positive voltage, delivered to the front-side n-type electrode, responsible to manage the gain;
- a sufficiently negative voltage applied at the backside p+ electrode to deplete the whole sensor and enable the charge collection by drift.

The possibility to have a direct control of the gain and the signal dynamics by tuning the bias voltage applied to the collection electrode and to the backside implant, represents a major difference with respect to traditional LGADs. Indeed, LGADs feature one bias voltage only, applied to the sensor bulk, and responsible to inversely bias the p-n junction. In order to be able to bias the collection electrode at tens of volts and fully deplete the gain layer, the sensor nodes have to be AC coupled to the front-end preamplifier, as shown in Fig. 5.1 (right). A decoupling capacitor is therefore implemented together with a bias resistor, allowing to apply a sufficient high voltage at the top collection electrode and, at the same time, to deliver the proper voltage to the CMOS readout circuitry.

5.1.1 Junction termination layout

To evaluate the effect of the pixel termination layout on the charge collection dynamics, pixels with the same size but different layout of the implants at the pixel borders, labelled as A1 and A2, were designed. The two layouts are schematically represented in Fig. 5.2.

- In the **A1 layout**, shown on the left side, there is no free space between the deep p-wells and the gain layer implant. As a consequence, charges generated at the pixel periphery are multiplied, since the charge will be conveyed in the avalanche region. This effect is due to the presence of an almost continuous p-type implant at the pixel borders. This layout is expected to provide a higher average collected charge, thanks to charge multiplication across the entire matrix area.

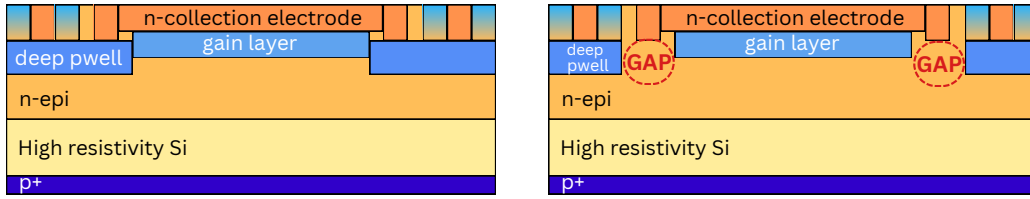


Fig. 5.2 Schematic cross section of pixels with layout A1 (left) and A2 (right)

- On the other side, in the **A2 layout**, a gap region, highlighted with red dashed circles, is preserved between the deep p wells and the gain layer, leading to an edge termination more similar to the one of standard LGADs. In this case, charges from the periphery are not multiplied, because of the gap between the two p-type implants. This causes the loss of the electrical continuity and leads to a direct path to the n-type collection electrodes for charges generated in the inter-pad regions. In this layout, a more uniform behavior in terms of multiplication inside the active area is foreseen, with the consequence of a decreased total multiplication volume, considering the whole pixel. Thanks to the possibility to distinguish between fast and slow signals, originating from the central or the edge area of the pixel, respectively, and selecting only the fast ones, a better time resolution is expected for this layout.

5.2 Monte Carlo simulations

Following the procedure described in the previous chapter, combined TCAD and Monte Carlo simulations have been performed on a structure with layout A2. The electric field map extracted from bidimensional TCAD simulations and the computed weighting potential have been used to conduct Monte Carlo simulations aimed at investigating the gain and assessing the intrinsic time resolution of the sensor.

5.2.1 ARCADIA engineering run 3 with nominal doping profiles

This set of simulations has been performed using the nominal doping profile of the gain implant, provided by the foundry. The simulation involves a domain with dimensions $250 \mu\text{m} \times 140 \mu\text{m}$ and a thickness of $48 \mu\text{m}$, as displayed in Fig. 5.4. The applied voltages are 45 V at the top collection electrode and -40 V at the backside

p-doped electrode. The electric field and the weighting potential are reported in Fig. 5.3, where the high electric field region is noticeable in the area corresponding to the gain layer implant. A finer mesh was adopted with respect to the previous sets of simulations without gain layer, in order to guarantee a sufficient sampling in the volume where multiplication occurs. In particular, a 20 nm uniformly spaced mesh was adopted.

In the Allpix² simulation, a 180 GeV pion beam (MIPs) was used as particle source

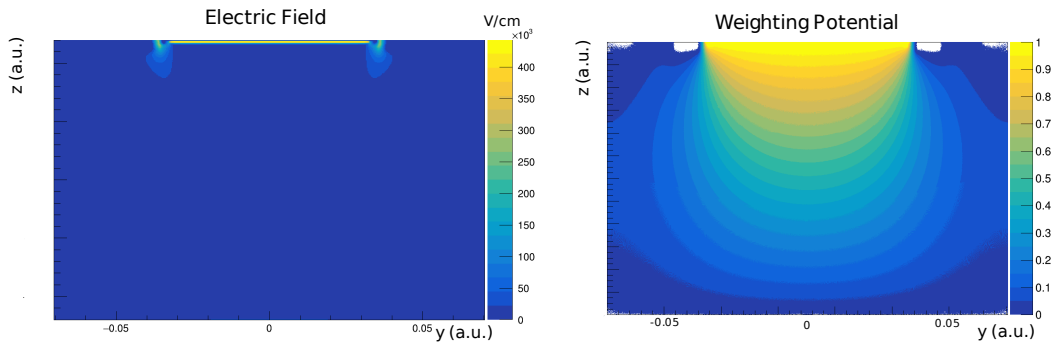


Fig. 5.3 Electric field (left) and weighting potential (right) of a single pixel simulated with layout A2.

and configured such that 1 particle crossing of the sensor corresponds to 1 event. For what concerns the carriers propagation, the Masetti-Canali [134] mobility model was employed¹. A time step of 0.5 ps was set as time granularity to calculate the induced charge. The adopted multiplication model is the Okuto-Crowell model [92]. Two sets of simulations have been carried out and the results are reported in the following.

Position scan

Different impinging positions of the pion beam were simulated, starting from the center of the pixel and moving gradually towards the border with a 10 μm step, as illustrated in Fig. 5.4. Pions impinge orthogonally to the sensor surface, with a beam-like source featuring a narrow size of 1 nm, in order to guarantee that the particles cross the pixel always in the same position. 1000 events have been simulated in each position.

Fig. 5.5a presents a comparison of the average waveforms for all the events impinging

¹the model is the same employed by the Synopsys Sentaurus TCAD software.

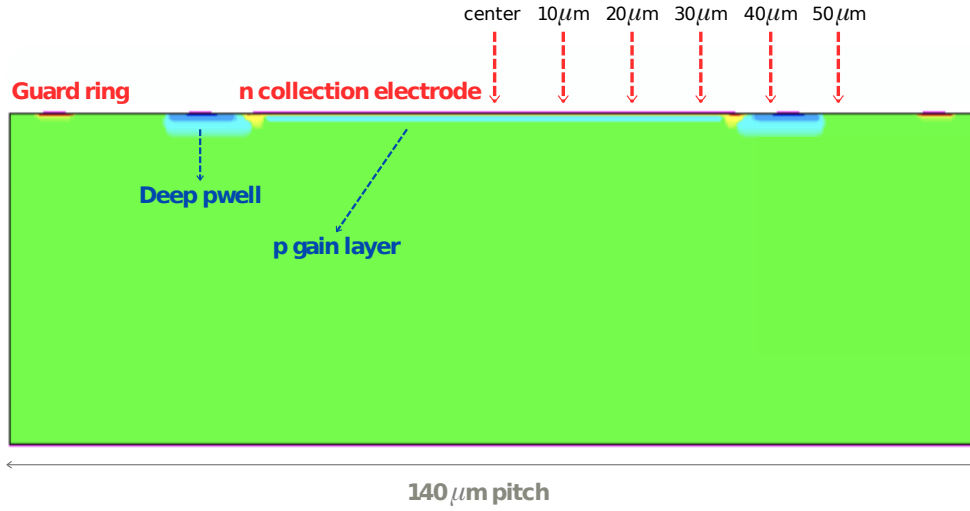


Fig. 5.4 Cross section of the TCAD simulated ARCADIA pixel with gain layer and layout A2. The different particles' impinging positions are indicated with dashed arrows. Courtesy of M. Mandurrino for the TCAD simulations.

in the pixel's center, with and without multiplication enabled. A clear difference is visible in the shape of the signal. The waveform without multiplication features a more triangular shape, while enabling the multiplication turns on the gain, thus enhancing the total collected charge. Fig. 5.5b shows the superimposed average waveforms for all the impinging positions with activated multiplication. They look significantly different based on the impact position. In particular, from the center until $\sim 30 \mu\text{m}$, the effect of the gain on the waveforms is clearly visible, while moving towards the pixel periphery brings to a reduction of the collected charge and to a different shape of the induced signal. In particular, the light blue and purple average waveforms in Fig. 5.5b, differ the most from the others, as they suffer the absence of gain. Indeed, in the reference system depicted in Fig. 5.4, the gain layer boundary is located around $27 \mu\text{m}$.

In correspondence of each impinging position, the gain can be evaluated as the ratio between the collected charge with and without multiplication. Fig. 5.6 (left) shows the collected charge distributions for the central impinging position with and without multiplication enabled, i.e. the corresponding comparison presented in Fig. 5.5a. From a Landau fit, the MPV of the collected charge was extracted. The gain vs position curve has been retrieved through a point-like calculation of the gain and is reported in Fig. 5.6 (right). The gain values have been normalised to the

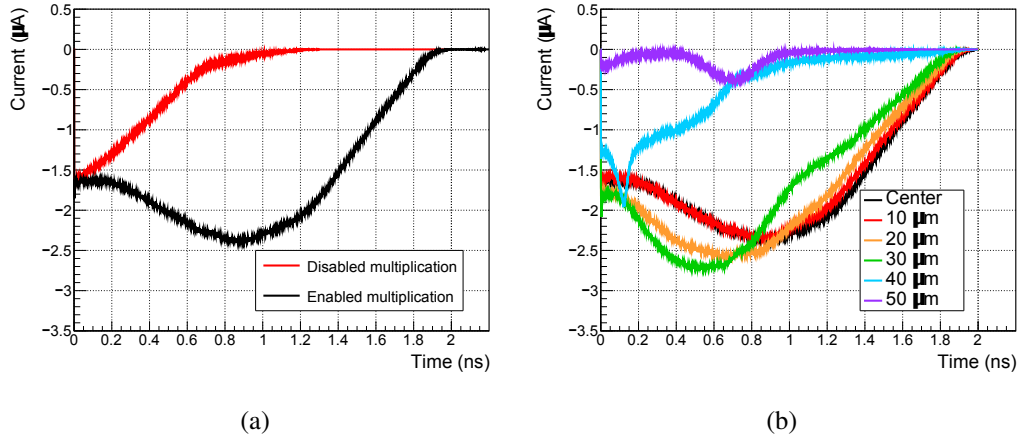


Fig. 5.5 Average waveforms of 1000 events with central impinging position comparing the effect of active/inactive multiplication (a). Average waveforms for different impinging position with active multiplication (b).

maximum, here called full gain. As can be observed, in the simulated A2 structure, the multiplication progressively decreases moving the particle's impinging position towards the edge, since the particle hits the sensor outside the multiplication region.

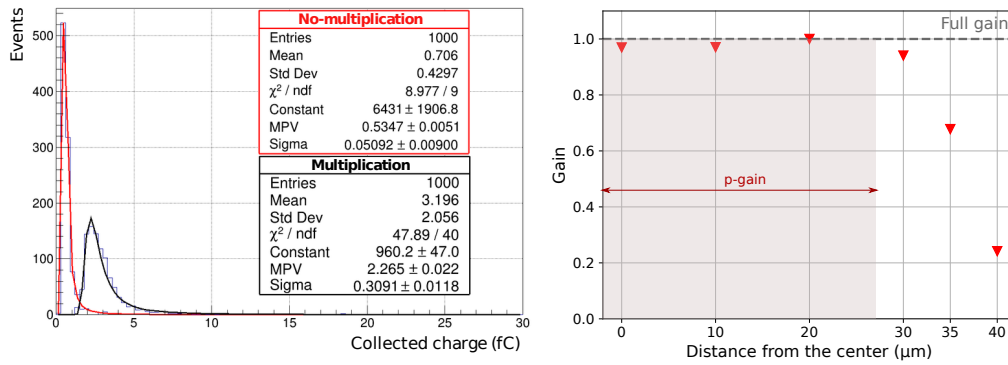


Fig. 5.6 Simulated collected charge distributions for the central impinging position with (black) and without (red) multiplication and superimposed Landau fit (left). Estimated gain for A2 structure layout as a function of the impinging position, normalised to the maximum value, called full gain (right).

The adopted procedure to estimate the time resolution is the same applied for the sensors without the gain layer in 4.3.5 and details are not repeated here. It has been evaluated by considering as an estimator the standard deviation of the crossing time

distributions, obtained by applying a constant fraction to the normalised collected charge curves. The results are reported in Fig. 5.7 as a function of the applied threshold and for the different impinging positions of the MIPs. As can be observed, as the impact distance from the pixel center increases, the time resolution deteriorates. Notably, when the impact position is $40\text{ }\mu\text{m}$ or more away from the center, the trend starts to deviate from the one observed in correspondence of the other positions. This is in line with the observations made on Fig. 5.6, unveiling a decrease of the gain after a distance $\sim 30\text{ }\mu\text{m}$ from the pixel center.

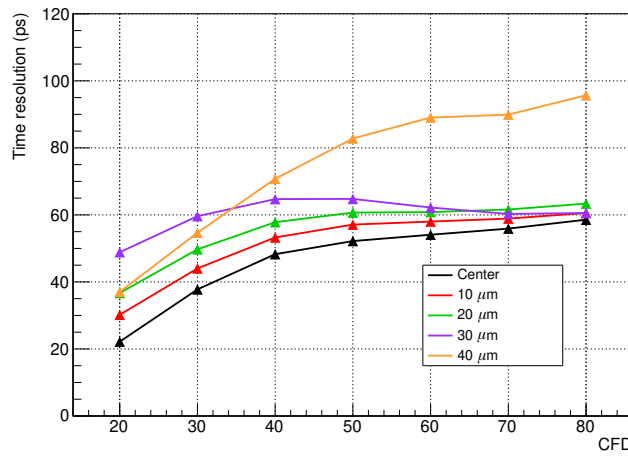


Fig. 5.7 Time resolution as a function of the CFD threshold applied and for different MIPs impinging position.

Random impinging position

A second simulation configuration involved the study of the time resolution when a pions beam impinges randomly, modelled as a square source with side length of $100\text{ }\mu\text{m}$, in the center of the pixel. Figure 5.8a shows the collected charge distribution of 10000 events. It features a double population, due to the pixel termination layout of the simulated A2 structure. Indeed, as explained in the previous section 5.1.1, when the particle crosses the edge of an A2 structure and the electrons are generated below the termination, the resulting signal is not multiplied. In order to exploit the potentiality of this structure and estimate the time resolution of the multiplied signals only, coming from charges that have been generated and collected in the central volume of the pixel, a cut has been applied at 1.25 fC , highlighted with a red line and leading to the distribution in Fig. 5.8b. The time resolution estimated considering

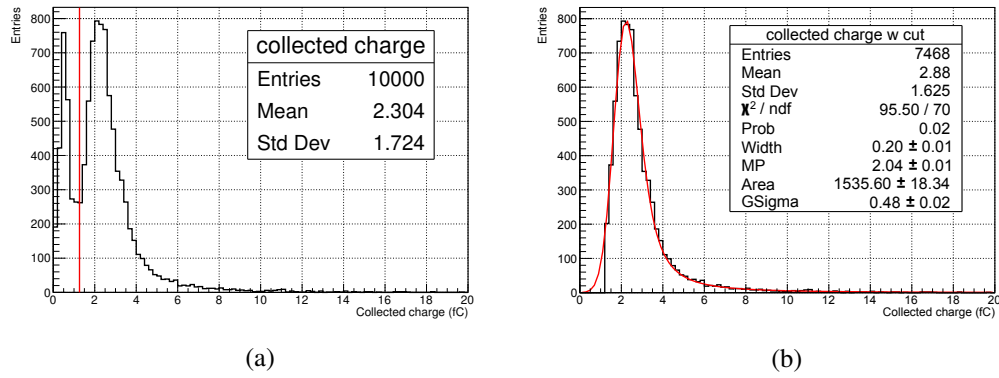


Fig. 5.8 Collected charge distribution of 10000 events with random impinging position in a square area of $100 \mu\text{m}$ side length (left) with highlighted applied cut in red at 1.25 fC to select multiplied signals. Collected charge distribution after the selection of multiplied events (right) with a superimposed fit of a Landau-Gaussian convolution.

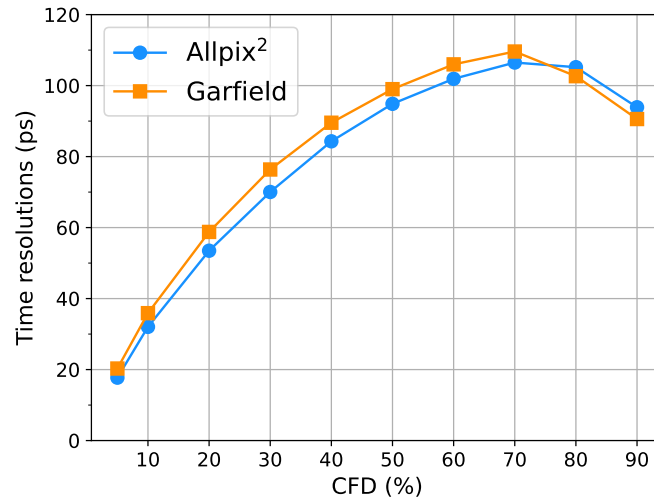


Fig. 5.9 Time resolution estimated on A2 structure of ARCADIA engineering run 3, with Allpix² and Garfield++. MIPs impinge randomly on a square area with side length of $100 \mu\text{m}$, in the center of the pixel. Courtesy of U. Follo for providing the Garfield++ results.

only the events in Fig. 5.8b is then shown in Fig. 5.9, where a comparison with the results obtained with the Monte Carlo tool Garfield++ is displayed. The simulations were executed in the same conditions and a coherent analysis was performed. The results show a good agreement, confirming the reliability of the followed method.

5.2.2 ARCADIA engineering run 3 with tuned doping profiles

In order to obtain a good matching between TCAD simulated C-V and measurements performed on the test structures belonging to the third ARCADIA engineering run (see Sec. 5.3), a fine tuning of the lateral spreading of the doping profiles was needed. The gain simulated using the tuned multiplication layer, based on the measured C-V, is in the range between 2 and 3, considerably lower than the desired one (10-30). The reason has been discovered and more details will be provided in the following sections, while hereafter, results from the Monte Carlo simulations with the tuned profiles are provided. The applied voltages are 45 V at the top collection electrode and -40 V at the backside p-doped electrode. The simulation involves 10000 events impinging randomly in a $(100 \times 100) \mu\text{m}^2$ area in the center of the pixel.

The average waveforms computed with both the Allpix² and Garfield++ tools exhibit an excellent agreement, as shown in Fig. 5.11a. As in the previous set of simulations, the adopted multiplication model is the Okuto-Crowell. Fig. 5.10 illustrates the effect of enabling the multiplication on the collected charge. The distributions are

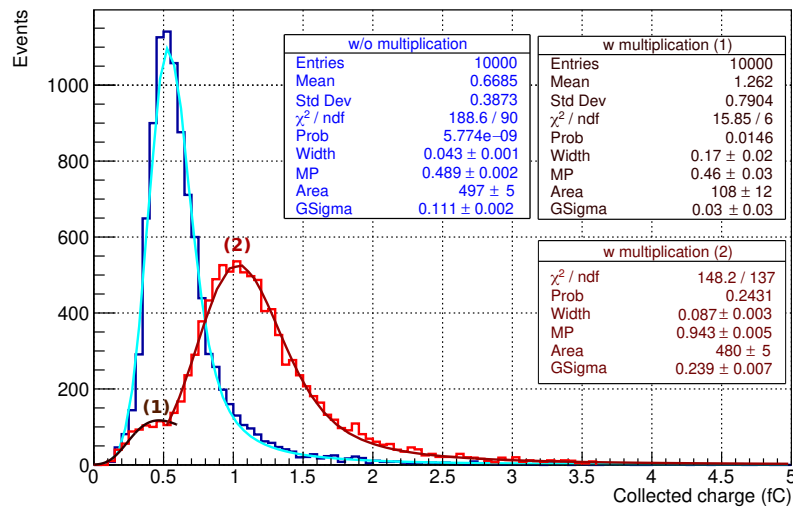


Fig. 5.10 Simulated collected charge without (blue) and with (red) multiplication enabled on ARCADIA run 3 structure, A2 layout. The distributions are fitted with a convolution of a Landau and Gaussian fit. The distribution with multiplication enabled features a main distribution, labelled with (2), and a shoulder located at small collected charges (1), attributed to not multiplied signals.

fitted with a convolution of a Landau and a Gaussian fit and the MPV shifts to higher values when the multiplication is enabled; however, a shoulder appears at lower

collected charges. Also this second population, indicated with (1) in Fig. 5.10, has been fitted with a convolution of a Landau and Gaussian fit. This shoulder can be explained by the A2 junction termination layout considered in this scenario, where charges collected from the pixel periphery are not multiplied, resulting in a secondary population. The simulated gain is estimated as the ratio between the MPV of the Landau distribution with and without multiplication model enabled. In this case, the gain is ~ 2 .

The time resolution was determined using the previously described approach, yielding to the trend shown in Fig. 5.11b, which demonstrates excellent consistency with the Garfield++ results within 10%. The presented simulation results have allowed

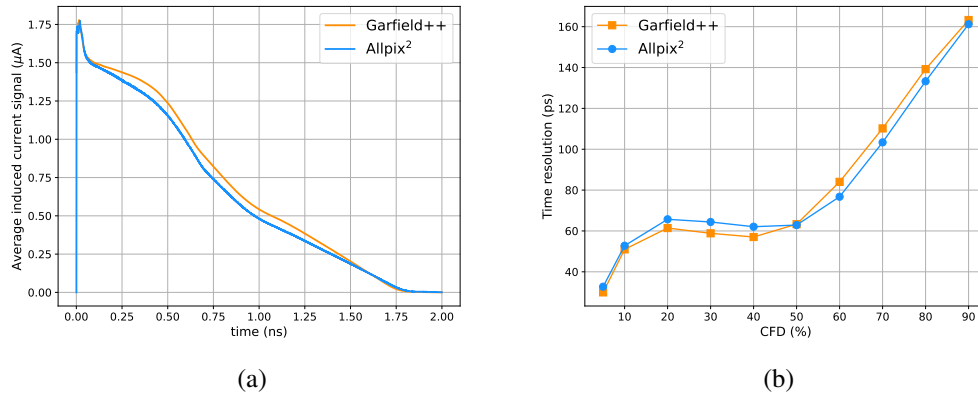


Fig. 5.11 Average induced signal of 10000 simulated events, impinging randomly on a $(100 \times 100) \mu\text{m}^2$ area in the center of the pixel (left). Simulated sensor time resolution as a function of the applied constant fraction on ARCADIA run 3 structure with A2 layout (right). Results obtained with Allpix² (blue) and Garfield++ (orange). Courtesy of U. Follo for providing the Garfield++ results.

to estimate, through the statistics provided by the Monte Carlo, the intrinsic time resolution expected from these new sensors with gain layer. Moreover, they have been a meaningful benchmark to validate the employed simulation process, showing a remarkable consistency between the results obtained with two different Monte Carlo simulation frameworks. Obviously, the simulations with the various gain splits and the test activities proceeded in parallel, in an interplay that was crucial in this first phase of R&D.

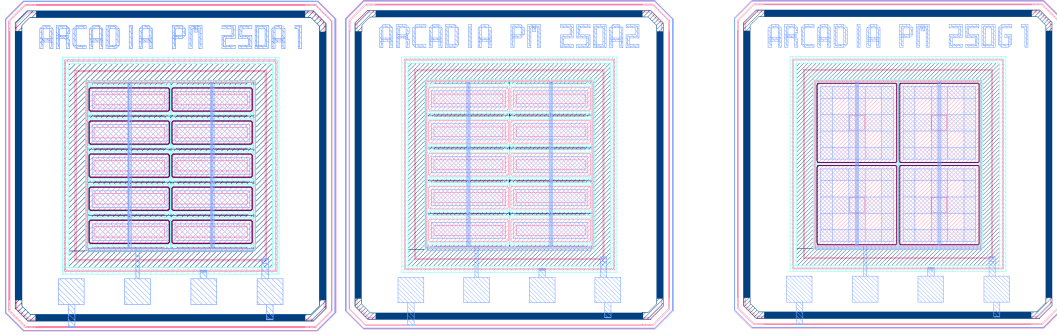


Fig. 5.12 A1, A2 and G1 passive pads fabricated in 110 nm CMOS technology. The active area is $250\ \mu\text{m} \times 70\ \mu\text{m}$ for A1 and A2 and $250\ \mu\text{m} \times 250\ \mu\text{m}$ for G1.

5.3 Characterisation of ARCADIA engineering run 3 passive structures

In April 2023, the first ARCADIA production with gain layer, i.e. the ARCADIA third engineering run, was received. It included passive test structures, i.e. sensors without the integrated electronics, together with active devices, where the CMOS readout electronics was implemented. This section focuses on the test campaign, conducted in collaboration with TIFPA (Trento), to characterise the passive test structures. The main goal of this initial test campaign was to demonstrate the feasibility of incorporating a gain layer into the sensor technology developed by the ARCADIA collaboration and to qualify the process. Several passive test structures were produced, differing in both the geometry and the border termination of the pads. Fig. 5.12 illustrates the ARCADIA 250A1, 250A2 and 250G1 test structures where the first two feature rectangular passive pads with the same geometry of the active pixels, with $250\ \mu\text{m} \times 70\ \mu\text{m}$ active area, while the G1 are square pads measuring $250\ \mu\text{m} \times 250\ \mu\text{m}$ with larger fill factor. The A1 and A2 pixel layouts are described in 5.1.1, while the G1 has the same layout as the A1, but features additional holes in the metal that can be employed for optical measurements [132].

5.3.1 $200\ \mu\text{m}$ active thickness

First tests were conducted on the $200\ \mu\text{m}$ active thickness sensors, studying and exploring the sensors' performance of this first production.

I-V

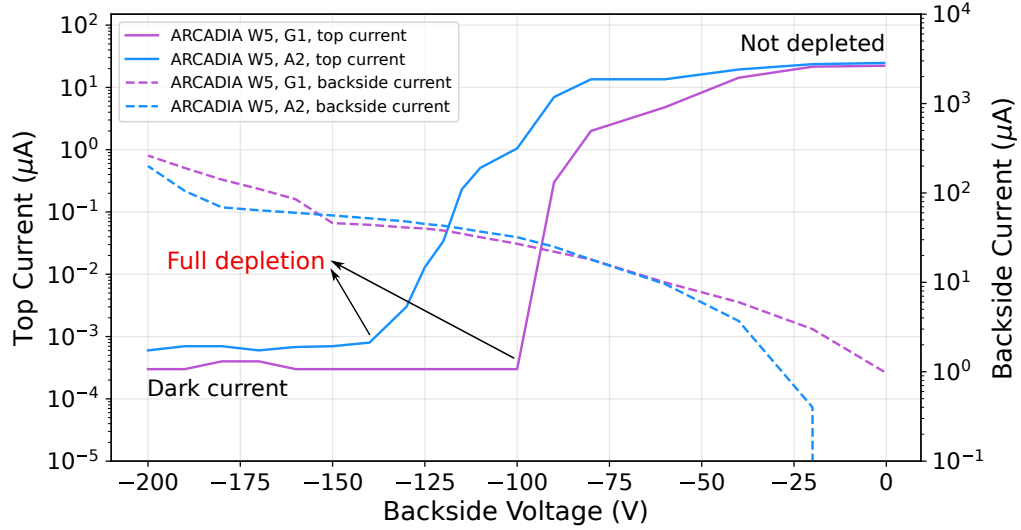


Fig. 5.13 I-V curve measured on G1 and A2 passive test structures fabricated in 110 nm CMOS technology. The continuous line indicates the top current, while the dashed line is employed for the backside current. The top voltage and the guard ring voltage were kept fixed during the measurement at 40 V and 8 V, respectively.

Current measurements were performed as a function of the voltage applied to the backside electrode. Fig. 5.13 illustrates two I-V curves measured on a G1 and a A2 structures. As can be observed, for low backside voltages, the sensors are not depleted and the current flowing from the n top electrode is of the order of tens of micro ampere. The full depletion is reached between -75 V and -100 V for the G1, where the I_{top} current undergoes a significant decrease. The A2 structure layout achieves full depletion for voltages above -100 V. The reason for the backside current increasing trend has been understood as a dark current (hundreds of μA) flowing between the backside electrode and the guard-ring, probably due to the damaged sensor volume close to the chip edge.

C-V

C-V measurements were performed at TIFPA, Trento, leaving the backside electrode floating and contacting the n-doped collection electrode and the p-well. The measurement is therefore aimed at extracting characteristics of the gain layer. C_{top} as

a function of the applied voltage is shown in Fig. 5.14 for the three test structures described before and for three different tested wafers. The knee observed in the

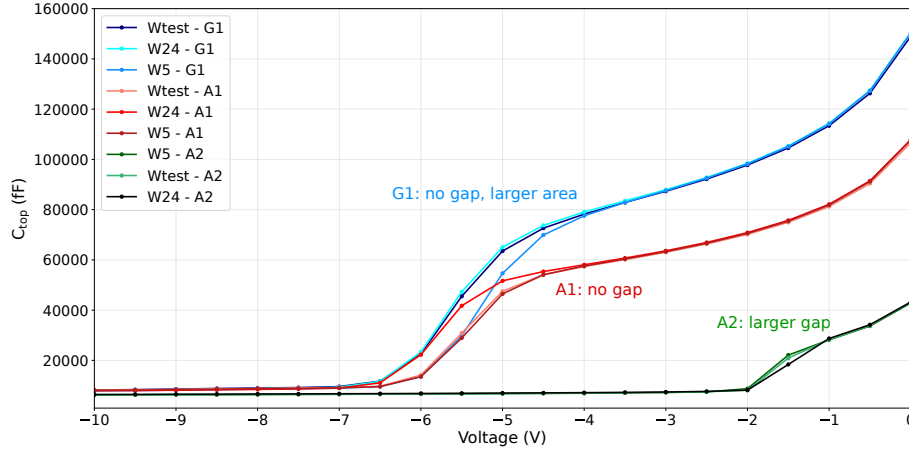


Fig. 5.14 C-V curves measured on the A1, A2 and G1 test structures. Different gap size translates into different depletion voltages of the gap regions.

C-V curves allows an estimation of the voltage required for the depletion of the gap between gain layer and deep p-wells. In particular, for the A1 and G1 structures, the capacitance remains high until 5-6 V, when it starts to decrease. This behavior is attributed to the proximity of the p-well to the gain layer, which isolates the gain layer and results in the observed higher capacitance. The A2 structure, on the other hand, features a gap between the deep p-well and the gain layer, causing the loss of electrical continuity at lower voltages ($\sim 1-2$ V). The measurements demonstrated that the narrower the gap between deep p-wells and p-gain, the higher the voltage needed to deplete the gain layer region.

5.3.2 48 μm active thickness

Successive measurements were performed on thinner passive test structure with 48 μm active thickness. Figure 5.15 and 5.16 display the current measured at the top electrode and the backside electrode respectively, as a function of the reverse bias voltage applied to the backside, for both the A1 and A2 layouts. During these measurements, the voltage at the top-side electrode was maintained at a constant value of 35 V and the guard ring was polarised at 3 V. For low bias voltage, the topside current is high and the sensor is not fully depleted. As the reverse bias voltage applied to the backside contact increases, the space charge region gradually

enlarges until the sensor is fully depleted. The depletion process can be observed in

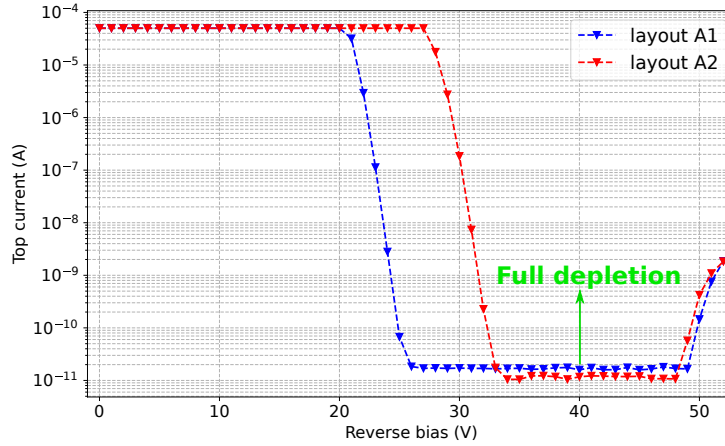


Fig. 5.15 Current measured at the top electrode of $48\ \mu\text{m}$ thick passive structures as a function of the negative voltage applied to the p^+ backside electrode, for the A1 and A2 layouts. The voltage applied at the collection electrode was fixed at 35 V and the guard ring was polarised at 3 V. Results presented in [135].

the steep decrease of the topside current in Fig. 5.15. At this point, the n-wells are isolated and no current is flowing, except the dark current. The distinct behavior of the A1 and A2 structures is attributed to their differing layouts, with the gap in the A2 design shifting the depletion point to higher V_{back} . With respect to the $200\ \mu\text{m}$ thick test structures (see Fig. 5.13), the depletion is reached at lower reverse bias voltages, as expected. The further increase of the top current visible around $-49\ \text{V}$ is due to the beginning of an edge breakdown, since also the current measured at the guard ring (shown in App. C.1) undergoes a significant increase in this voltage range.

From Fig. 5.16, the voltage range where the punch-through phenomenon begins can be identified. This occurs when the voltage applied to the backside electrode exceeds a certain threshold, leading to a hole current flowing between the deep p-well on the front side and the p^+ doped electrode at the bottom of the sensor. This current increases exponentially, and operating the sensor in a region with a high punch-through current should be avoided, as it results in excessive power consumption. For the measured structures, the punch-through starts after a backside bias voltage $\sim -40\ \text{V}$, as indicated in the plot. The constant current region around $-42\ \text{V}$, is due to the fact that the pwell reached the current limit set during the operation and this

reflects also in the backside current, since in this voltage range, the current flowing between the pwell and the backside electrode is the prevalent one.

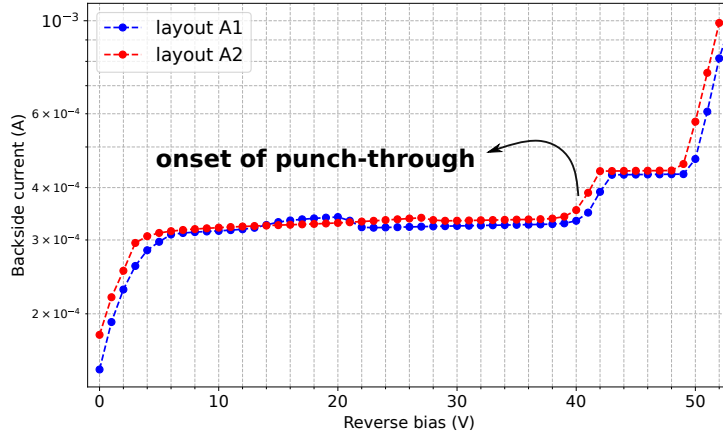


Fig. 5.16 Current measured at the backside electrode of $48 \mu\text{m}$ thick passive structures as a function of the negative voltage applied to the p+ backside electrode, for the A1 and A2 layouts. The voltage applied at the collection electrode was fixed at 35 V and the guard ring was polarised at 3 V. Results presented in [135].

Further measurements conducted on the passive test structures can be found in [132], while the next section is centred on the presentation and the characterisation of the first CMOS 110 nm prototype with gain layer and integrated electronics.

5.4 The Monolithic CMOS Avalanche Detector PIXelated (MADPix)

This section presents the Monolithic CMOS Avalanche Detector PIXelated (MAD-Pix): the first prototype of a monolithic sensor with internal gain and integrated electronics based on a commercial 110 nm CMOS process. The chip, included in the ARCADIA third engineering run, has been developed within the ALICE 3 TOF working group and the ARCADIA collaboration. The electronics of the chip is implemented in a LFoundry 110 nm node. The primary objective of the prototype discussed hereafter is to demonstrate the compatibility of the process with the gain layer. Results on the first characterisation tests have been recently published in [130] and details on the electronics can be found in [128].

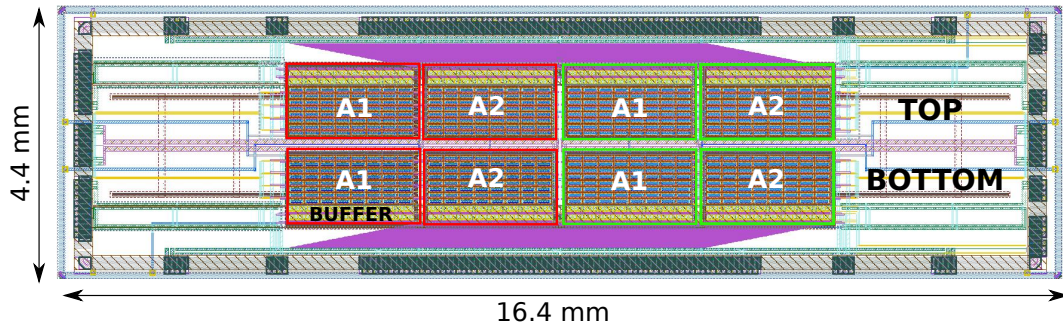


Fig. 5.17 MADPix chip layout, composed of two symmetrical regions: top and bottom. The four top and the four bottom matrices are made of 8×8 pixels. The four matrices in the same region differ for the pixel layout (A1 or A2) and for the coupling capacitors to the front-end electronics (red and green).

5.4.1 Chip layout

The chip is (16.4×4.4) mm² large and includes two symmetrical adjacent regions: *top* and *bottom*. Each region hosts four matrices composed by 64 pixels divided in 8 rows and 8 columns, for a total of 512 pixels. The layout is shown in Figure 5.17. The four neighbouring matrices differ for the pixel layout A1 or A2 (see 5.1.1) and for the coupling capacitance between the pixel and the amplifier, highlighted in different colors in Fig. 5.17. Indeed, a distinctive element of the engineered monolithic device, is the possibility to bias the collection electrode to a voltage above 20 V, in order to manage the gain. Hence, special care must be taken in connecting the sensor to the front-end electronics, which operates at a significantly lower voltage (1.2 V). The proposed solution involves AC coupling the pixel to the electronics ².

Pixel specifications

Monte Carlo simulations for pixels with large collection electrode and $50 \mu\text{m}$ thickness without internal gain layer, shown in 4.4.2, demonstrated that the weighting potential uniformity improves the sensor time resolution as it lowers the distortion component for square pixels with a pitch $\geq 100 \mu\text{m}$. The target pixel geometry was squared with $250 \mu\text{m}$ pitch, but because of density rules posed by the specific

²to deal with collection electrode voltages higher than 30 V and reach the desired gain, a fully custom capacitor is implemented in the matrices highlighted in green in Fig. 5.17, featuring an increased gap between the plates. However, only the matrices highlighted in red were characterized, as no breakdown occurred with the standard capacitor up to 50 V.

submission, the pixel size in this run was reduced to $250\ \mu\text{m} \times 100\ \mu\text{m}$. The ratio between the collecting electrode area and the total pixel area is around 67%. For timing measurement this ratio should be maximised, in order to lower the distortion contribution to the time resolution [14]. Future designs will feature expanded pixel geometries, exploring larger pitches up to 1 mm. The benefit of larger pixel sizes lies in an improved uniformity in the weighting potential and an enlargement in the absolute area of the deep-p-well per pixel.

Readout electronics

Each pixel features a front-end electronics, followed by an output buffer that drives the amplifier's output out of the chip. The 1.2 V front-end electronics is placed in a $(8 \times 250)\ \mu\text{m}^2$ deep-p-well, implemented in the long side dividing two adjacent pixels, $4\ \mu\text{m}$ in one pixel periphery and the other $4\ \mu\text{m}$ on the bottom neighbour. It is composed by a cascoded common source amplifier and a second cascoded branch, employed as a current source for the input transistor. The amplifier is followed by a differential buffer. Moreover, 3.3 V source follower buffers are placed outside the matrices and inside the external guard ring. A schematic diagram of the readout electronics is shown in App. C.2. The n-type external guard ring surrounds each matrix and, polarised to a positive voltage below 10 V, collects the electrons generated in the periphery of the chip and preserves a low dark current in the pixel. Because of size constraint, the chip is designed with only 64 analogue outputs per each region (top and bottom) hence the outputs of four 3.3 V buffers, one for each matrix, share the same output pad.

Power consumption

In comparison to the HERMES prototype amplifier (see 4.4.4), the use of 1.2 V front-end electronics offers a faster response with reduced power density. The in-pixel front-end power consumption is 0.18 mW per pixel, that corresponds to a power density of $7.2\ \text{mW}/\text{mm}^2$, remembering the pixel dimension of $(100 \times 250)\ \mu\text{m}^2$. Each output buffer stage, driving the analog output to the PAD, consumes a current of $500\ \mu\text{A}$, resulting in a power consumption of 1.65 mW per channel.

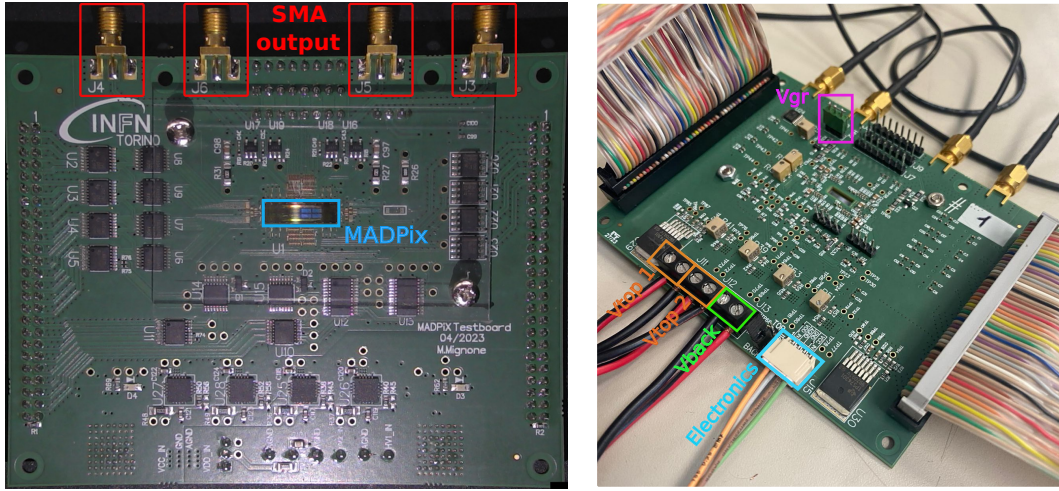


Fig. 5.18 Photo of the front side (left) and rear side (right) of the test board designed at INFN Torino by M. Mignone to characterise the chip. The MADPix chip is wire bonded and visible in the photo.

5.4.2 Operation and readout system

A custom PCB test board (TB), displayed in Fig. 5.18 was designed to test the MADPix chip. Its primary function is to configure all the bias currents and voltages required by the electronics. The top region of the TB hosts four analogue buffers, each one driving a $50\ \Omega$ impedance line, exiting the TB via SMA connectors that can be read out with an oscilloscope. An FPGA manages the board via two flat cables connected to the rear side of the TB and visible in Fig. 5.18 (right). Five voltages are provided to the test board:

- $V_{\text{top 1}}$ and $V_{\text{top 2}}$ provide the positive voltage to the collection electrode of the right-side and left-side of the chip, respectively;
- V_{back} is the negative voltage supplied to the back-side electrode and it is common for all the matrices;
- $V_{\text{electronics}}$ to deliver the required voltages to power the electronics ($\sim 4.5\ \text{V}$);
- V_{gr} represents the positive voltage to be applied to the guard-ring in the $[2.5, 10]\ \text{V}$ range.

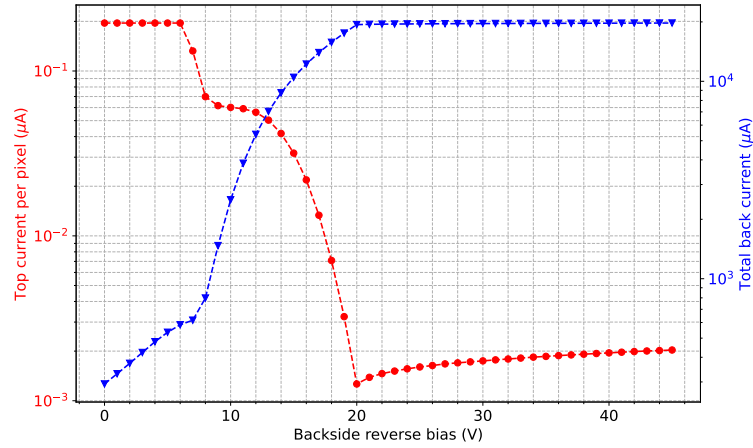


Fig. 5.19 Top current versus voltage curve per pixel (red) and backside total chip current as a function of the backside voltage in absolute value (blue).

5.4.3 I-V measurements

Electrical tests on the MADPix prototypes were carried out, in a similar way as for the passive test structures presented in 5.3.2. Fig. 5.19 shows the top current on the left-side axis and the backside current on the right-side axis, as a function of the reverse bias applied at the backside electrode. The first is defined as the current flowing from the n+ collection electrode to the n-type guard ring when the sensor is not yet depleted. As soon as the sensor starts to deplete, for a backside voltage ~ -10 V, this current reduces. The backside current, instead, represents the current flowing from the backside electrode. As previously mentioned, it allows an estimation of the voltage corresponding to the onset of the punch through. In that regime, the dominant backside current is due to the charge flow from the p+ backside electrode to the p-wells located on the front-side. The visible increase of the backside current around 10 V is due to a floating guard ring in the periphery of the matrix. The current further increases at backside voltages below -35 V, but the point of punch-through onset is not shown in the plot. The guard ring was biased at 8 V.

5.4.4 In-beam measurements and analysis results

Setup

To estimate MADPix time resolution, a test beam campaign was carried out at the Proton Synchrotron at CERN with a beam composed by a mixture of protons and pions with a momentum of 10 GeV/c. Two planes were employed for the measurements: the Device-Under-Test (DUT) and a $1 \times 1 \text{ mm}^2$ LGAD manufactured by FBK [136] with a thickness of $35 \mu\text{m}$, employed as trigger plane. The two planes are visible in Fig. 5.20 (left). The sensors were aligned through moving stages with micrometric precision and the telescope was kept at room temperature in a dark box. The outputs of three adjacent pixels of the DUT were read out and acquired together with the LGAD output. In particular, a LeCroy WaveRunner 9404M-MS oscilloscope with 20 GS/s sampling rate, 4 GHz of analogue bandwidth and 8-bit vertical resolution was used. The trigger was provided by the coincidences between one pixel of the DUT and the LGAD. A photo of the setup with the dark box and oscilloscope can be seen in Fig. 5.20 (right). The full waveforms of the

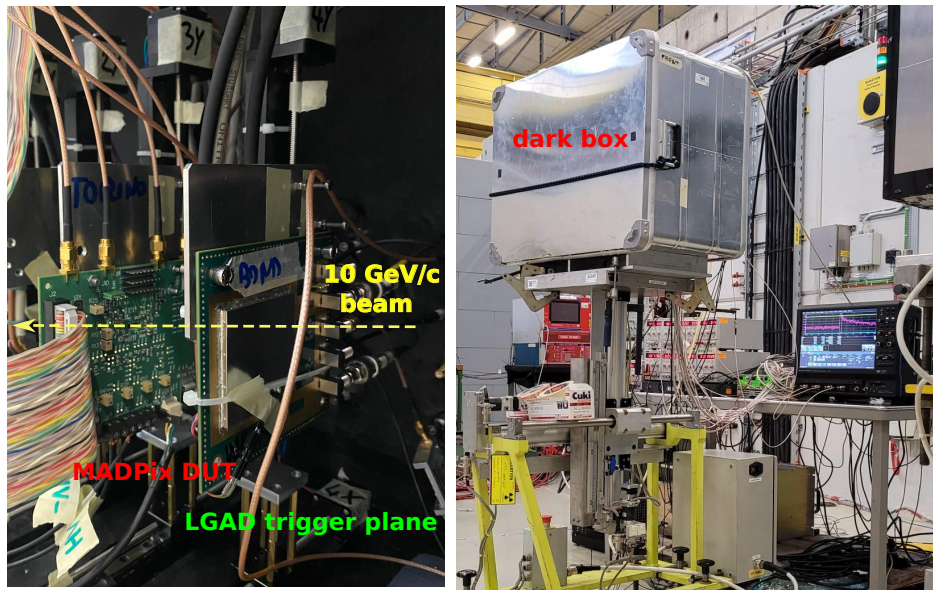


Fig. 5.20 Photo of the two planes of the telescope mounted on the moving stages inside the dark box (left) and setup installed at the Proton Synchrotron T10 beam line (right) in collaboration with INFN-Bologna.

LGAD and the DUT have been recorded and analysed offline.

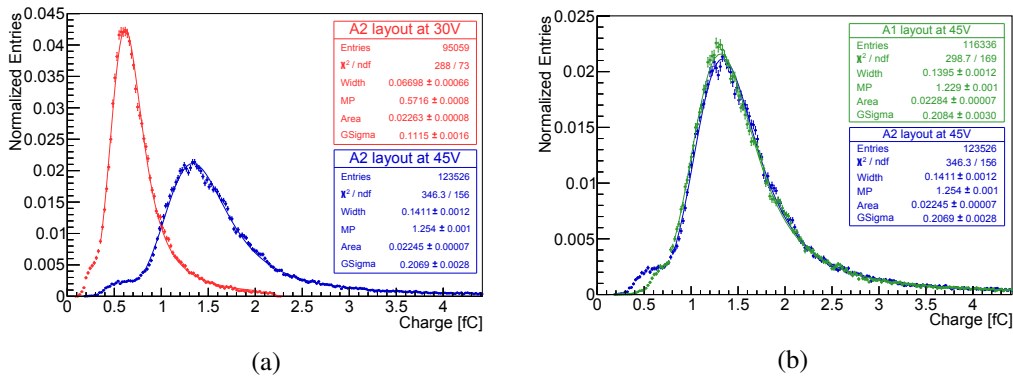


Fig. 5.21 Distribution of the signals integral for two different top bias voltages in the A2 structure: 30 V in red and 45 V in blue (a). Distribution of the signals integral for the two structure layouts at $V_{\text{top}} = 45$ V: A1 in green and A2 in blue (b). The backside voltage was fixed at -30 V. Image source [130].

Data analysis and results

In the following sections, the method and results from the analysis of the data collected during the test beam are presented. The time resolution of MADPix has been estimated by applying a fixed threshold algorithm with time walk correction and results are presented in [130]. For comparison, results with a constant fraction algorithm with time walk correction are reported in App. C.3.

Collected charge

The collected charge distributions are shown in Fig 5.21. The charge is evaluated as the maximum amplitude of the analogue signal divided by the electronics gain extracted through post-layout simulations. The distributions are fitted with a convolution of a Landau and a Gaussian functions. Figure 5.21a illustrates the charge distributions of an A2 structure with 30 V and 45 V collection electrode voltages. As observed, increasing the voltage results in a factor ~ 2.2 of increase in the MPV of the distribution, confirming the activation of the gain, consistent with the laser results [130]. Figure 5.21b compares the A1 and A2 collected charge distribution with 45 V applied to the collection electrode. The small mismatch between the shoulders at small charge values can be attributed to the different termination of the A1 and A2 layouts, since the A2 allows to distinguish multiplied and not multiplied events. This shoulder is excluded from the fit range.

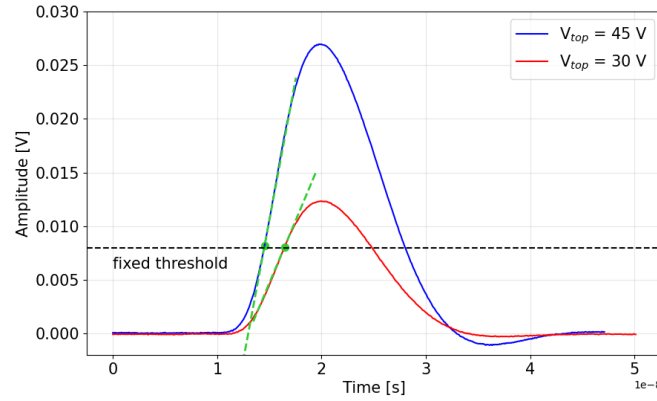


Fig. 5.22 Mean waveforms of 300 events acquired with a top voltage of 45 V (blue) and 30 V (red). A fixed threshold of 8 mV is shown as example, together with the slope in correspondence of the crossing time. The mean amplitudes of the two waveforms are 27 mV and 13 mV, with RMS of the signals' amplitude distributions of 10 mV and 5 mV, respectively. Image source [130].

Time resolution with fixed threshold algorithm

The Time of Arrival (TOA) of a particle is determined as the moment when the signal surpasses a specified threshold, as illustrated in Fig. 5.22.

The figure displays two average waveforms obtained with top voltages of 45 V and 30 V, respectively. For instance, a constant threshold of 8 mV is applied. The lowest applied threshold in the analysis was selected in order to be at least equal to $5 \sigma_{\text{noise}}$. Regarding the trigger plane, the TOA is calculated using the crossing time at 30% of the amplitude, based on the algorithm detailed in [94].

The above described method required a correction for the time-walk effect (see 2.1). For this purpose, the time differences between the TOA on the DUT (t_{DUT}) and on the LGAD (t_{trigger}) were plotted against the signal amplitude of the DUT ($DUT \text{ Amplitude}$), as illustrated in Fig. 5.23a. The resulting distribution was then fitted with the following function:

$$t_{DUT} - t_{\text{trigger}} = a + \frac{b}{(DUT \text{ Amplitude})} + \frac{c}{(DUT \text{ Amplitude})^2} \quad (5.1)$$

and the correction is applied by subtracting the value of the function in each amplitude bin from the measured data. Figure 5.23b shows the time difference distribution obtained with a threshold of 5 mV applied on DUT, before and after the time walk

correction. At this point, the corrected time difference distribution was fitted using an asymmetric q-Gaussian function to account for the tails. From the extracted sigma, the resolution of the reference LGAD was subtracted quadratically. The measured

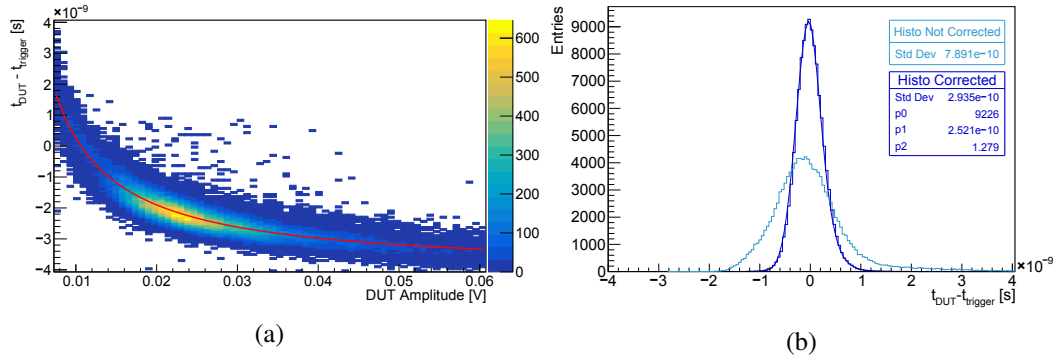


Fig. 5.23 Distribution of the time difference between the CMOS sensor (DUT) and the LGAD as a function of the DUT amplitude. In red the fit used to perform the time-walk correction (a). Time difference distributions between DUT and LGAD before (light blue) and after (dark blue) the time-walk correction (b). The fit used to extract the time resolution is superimposed to the second histogram, where p0 represents the normalization, p1 the sigma, and p2 the right heavy tail of the q-Gaussian. Image source [130].

time resolution obtained with the fixed threshold algorithm is shown in Figure 5.24 as a function of different applied thresholds.

Figure 5.24a highlights the difference in the response of an A2 test structure when the top voltage is increased from 30 V to 45 V. On average, an improvement of approximately 25% in timing performance is observed with a bias voltage of $V_{top} = 45$ V. At $V_{top} = 30$ V condition, the multiplication is strongly reduced, causing a lower average amplitude compared to the $V_{top} = 45$ V case. The time resolution at $V_{top} = 30$ V begins to worsen for thresholds larger than 6 mV, where the slope of the signal starts to decrease, as one can infer from Fig. 5.22. As a consequence a higher jitter contribution degrades the time resolution. On the other hand, for the 45 V, the slope of the signal is steep in this region, resulting in a more stable timing response.

In Figure 5.24b the time resolution measured on A1 and A2 structures, both with $V_{top} = 45$ V, is compared, showing a slightly better performance for the A1 version. This result could be due to the different junction termination layout and the increased multiplication volume in the A1. The lowest time resolution extracted with the fixed threshold algorithm and time walk correction is 234 ± 6 ps for the A1 and 244 ± 6 ps for the A2, with a threshold of 6 mV. From layout considerations, the best time resolution should be achieved with the flavour A2. However, due to the low gain

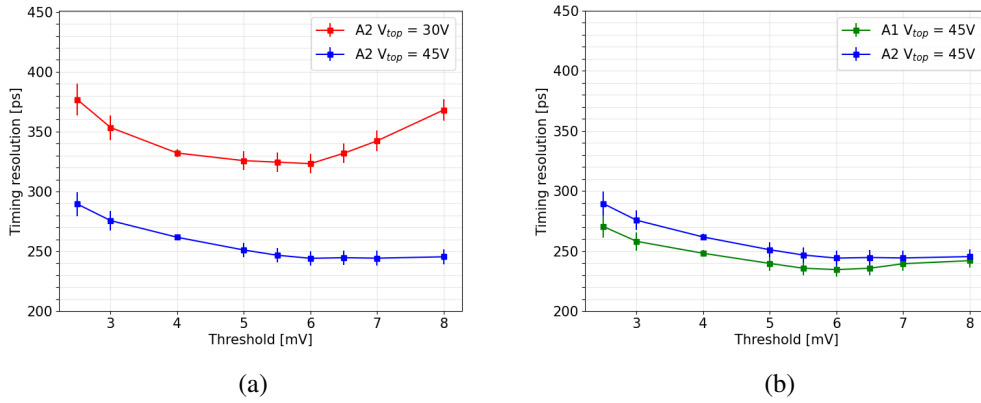


Fig. 5.24 Time resolution as a function of the applied threshold for an A2 structure at two different V_{top} voltages (a). Time resolution at $V_{top} = 45$ V for the two structures A1 and A2 (b). The backside polarization is set at -30 V. Image source [130].

measured in these structures, the discrimination of the particles impinging at the border from the ones under the collection electrode is not clear (Fig. 5.21b).

The error bars at 30 V in Fig. 5.24 have been computed as the standard deviation of the time resolution of four different pixels hosted on the same chip. The relative error has been propagated to the results obtained at 45 V. Similar results were obtained employing a constant fraction threshold algorithm and the results can be found in App. C.3.

Interpreting the results

The measured time resolution on the first prototype of CMOS-LGAD belonging to the ARCADIA third engineering run is about 230 ps for $V_{top} = 45$ V. This result is still far from the ALICE TOF requirement of 20 ps time resolution and cannot be explained with the jitter contribution, which is around 130 ps for a signal amplitude corresponding to 25 mV (MIP) [130].

The reason has been deeply investigated and understood through a numerical study based on TCAD simulations, summarised in Fig. 5.25, allowing to unveil an error during the fabrication process. Indeed, the energy of the ion implantation was set to a value 30% lower than the expected one, causing a shallow gain layer. The lateral ³C-V curves were employed to infer details on the gain layer, comparing experimental

³obtained with a ΔV applied between the deep-p-well and the n+ collection electrode on the top surface of the pixel.

and TCAD simulated curves. Fig. 5.25a shows that in order to match the measured and simulated C-V curves, a proper tuning of the p-gain profile was necessary. In particular, the gain implant had to be shifted towards the chip frontside, causing a reduced multiplication process and justifying the measured gain of 2.5. Fig. 5.25b

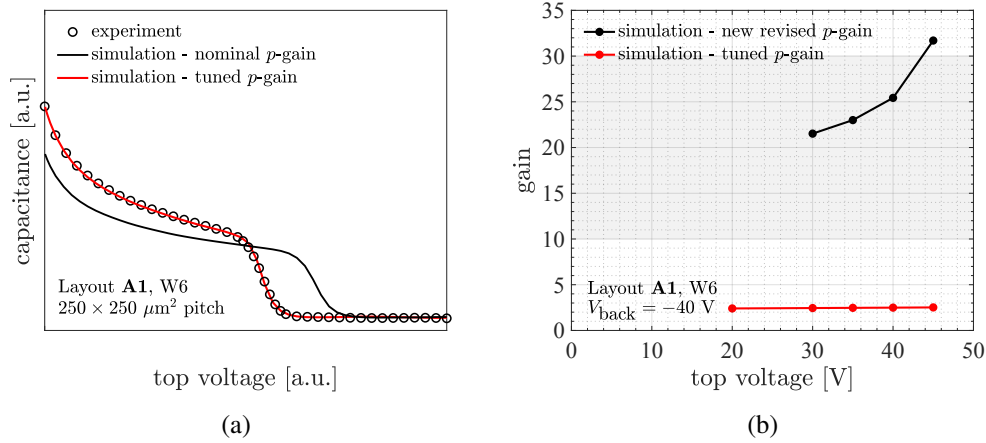


Fig. 5.25 Comparison of simulated and measured lateral C-V characteristics of a $250 \times 250 \mu\text{m}^2$ pitch test-structure with gain from the ARCADIA third engineering run (a). Gain curves simulated using the p -gain implant tuned on the measured C-V (red) and with the new profile submitted for the following short-loop run (black) (b). Image source [130].

exhibits the gain as a function of the top voltage, obtained with the found (tuned) gain implant, for a backside bias voltage of -40 V. The gain has been estimated in these TCAD simulations as the ratio between the integrated charge with and without the multiplication model enabled. The red points represent the gain obtained employing the tuned multiplication layer, based on the measured C-V. The black curve, instead, stands for the new revised gain profile, obtained employing the same maskset of the ARCADIA third engineering run, allowing to reach a gain ~ 10 -30.

Successive in-beam measurements conducted on the same structures but rising the bias voltage of the collection electrode until 60 V, have shown an enhanced time resolution better than 150 ps. These results are expected to be published this year. Moreover, tests are currently ongoing on new structures from the latest short-loop run (named run 3.2) with increased gain. The same masks have been exploited and a larger range of gain splits has been investigated, helping to obtain a good control of the process. Furthermore, on these structures, the problem of the high backside current observed in MADPix (see Fig. 5.19) from run 3, has been solved

by contacting the floating guard ring in the matrix periphery, thanks to a Focused Ion Beam (FIB) ⁴. After this correction, the backside current has been successfully reduced of more than one order of magnitude and the onset of the punch-through has been observed around $V_{\text{back}} -27$ V, with V_{top} at 45 V. Preliminary results obtained so far are encouraging and seem to prove the presence of the expected gain (5-13), with a reduction of the jitter contribution below 50 ps and a sub-100 ps time resolution.

⁴gallium ions have been employed, followed by a platinum deposition. The process has been carried out at INRIM, Torino.

Chapter 6

Validation of the 65 nm TPSCo CMOS imaging technology for the ALICE ITS3 upgrade

As already pointed out in 3.4.5 MAPS using commercial CMOS imaging technologies are already widely employed in HEP experiments. A collaboration between the ALICE experiment and the CERN Experimental Physics Department (EP) R&D was established to characterise and validate the 65 nm CMOS Image Sensor technology of Tower Partners Semiconductor Co. (TPSCo) [46] for future vertex and tracking detectors. In particular, the ITS3 upgrade (see 2.4.1) strongly benefits from this study, since the 65 nm technology was selected as a baseline for this third generation Inner Tracking System. As already shown in 3.4.3 for the 180 nm CMOS imaging technology [75, 74], also in the 65 nm process, the sensor optimisation has a relevant role. Indeed, four process splits were produced, gradually moving from the standard process to the most optimised [137] and the same three process variants shown in Fig. 3.6 were implemented in order to reduce the charge sharing and improve the charge collection performance.

This chapter illustrates the qualification of a pixel test structure, contributing to the validation of the technology in terms of pixel performance, particle detection and timing resolution. The author took part in the initial assembly of the setup, characterisation activities and participated in all the data acquisition and analyses presented in this chapter. During test beam campaigns, the author had a relevant responsibility in the alignment of the telescope planes, representing a challenging

task due to the very small dimensions of the test structures. She was responsible for the tracking analysis of the test beam data, crucial for the time resolution assessment and she was in charge of estimating the detector efficiency, the spatial resolution and the cluster size.

6.1 The Multi-Layer-Reticle (MLR1) submission

The Multi-Layer-Reticle (MLR1), shown in Fig. 6.1, was the first submission in the 65 nm TPSCo CMOS technology [137]. It was produced in summer 2021 with the aim of evaluating the charge collection performance of the targeted process that, up to that time, was mainly addressed to light detection applications and was never employed to detect charged particles.

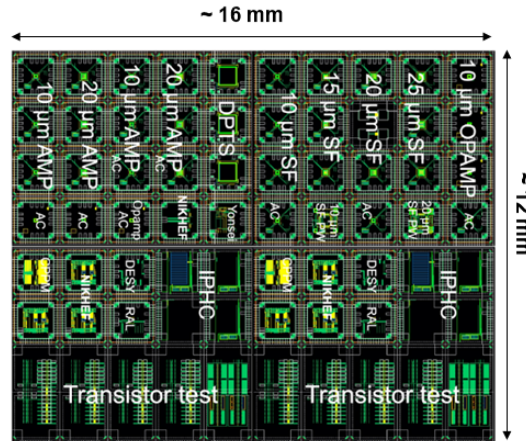


Fig. 6.1 Layout of the MLR1 submission in the TPSCo 65 nm ISC technology, containing a total of 70 test chips of $1.5 \text{ mm} \times 1.5 \text{ mm}$ or $3 \text{ mm} \times 1.5 \text{ mm}$. Modified picture from [137].

Four prototype chips implemented in the MLR1, $1.5 \times 1.5 \text{ mm}^2$ in area, are illustrated in Fig. 6.2. They are (starting from left):

- **APTS-SF**: Analogue Pixel Test Structure with a readout chain based on 4 source follower stages [138]; The chip is made of a 6×6 pixel matrix with direct analogue readout of the central 4×4 submatrix with the aim of testing the pixel cell, comparing process modifications and evaluating the radiation hardness. Several variants were produced with different combinations of pixel size and design and the pixel pitches varied between $10 \mu\text{m}$, $15 \mu\text{m}$, $20 \mu\text{m}$

and $25\ \mu\text{m}$. An intensive characterisation of this test structure was carried out both in laboratory and with in-beam measurements. The results are presented in [138]. A comparison between the APTS-SF and the APTS-OA prototypes will be shown subsequently in this work.

- **APTS-OA**: Analogue Pixel Test Structure with identical sensor and in-pixel front-end as in the APTS-SF, but with a fast operational amplifier as output stage [139];
- **DPTS**: Digital Pixel Test Structure; a matrix of 32×32 pixels with $15\ \mu\text{m}$ pitch in the modified-with-gap flavour. Each pixel is equipped with an amplifier and a discriminator, providing a time encoded digital readout with the purpose of testing the pixel digital front-end [140].
- **CE-65**: Circuit Exploratoire 65 contains a pixel matrix with analogue readout and was produced to explore the charge collection properties of the 65 nm TP-SCo process with a rolling shutter readout [141]. It is available in two different sizes (64×32 and 48×32 pixels, 15 and $25\ \mu\text{m}$ pixel pitch, respectively). Three different readout variants are implemented in the chip.

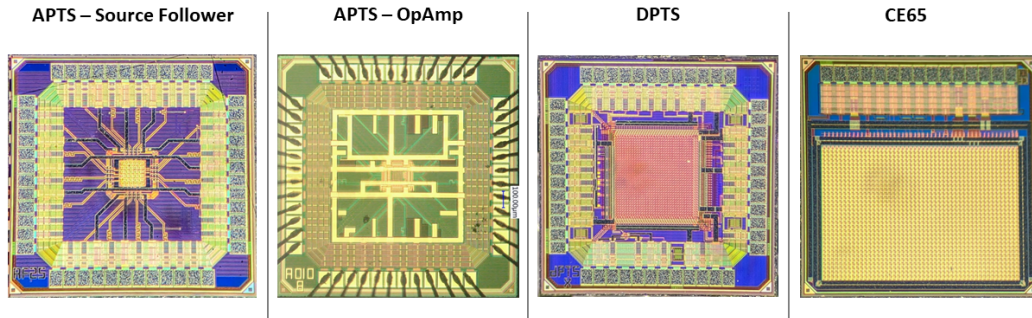
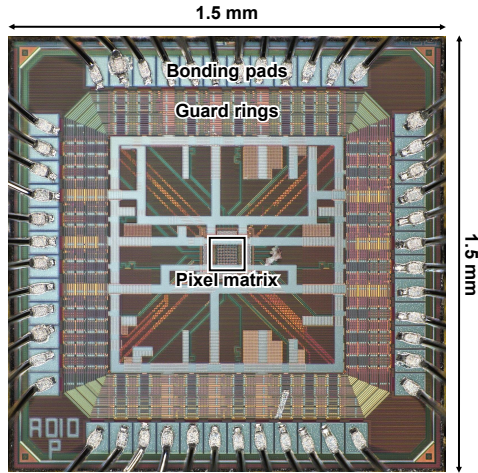


Fig. 6.2 Test structures belonging to the MLR1 submission. They measure $1.5\ \text{mm} \times 1.5\ \text{mm}$.

In order to validate the technology for HEP applications, extensive and challenging characterisation campaigns were carried out both in laboratory and in test beam facilities. In particular, the APTS-OA test structure has been first characterised in laboratory to find the best working point to operate it. Subsequently, intensive test campaigns with an ^{55}Fe source have been conducted to energy calibrate the chip response using soft X-rays and investigate the charge collection dynamics. Finally,



APTS-OA	
Die size	1.5 mm $\times$ 1.5 mm
Matrix	4 $\times$ 4
Readout	Direct analogue of central 4 $\times$ 4 pixels
Pitch	10 μ m
Process	Standard Modified Modified with gap

Table 6.1 Main characteristics of the APTS-OA.

Fig. 6.3 APTS-OA chip photo taken with a microscope.

the time resolution, detection efficiency and spatial resolution have been evaluated through in-beam measurements using MIPs. In the following sections, after a brief description of the APTS-OA chip, the most remarkable results are summarised, together with the followed methodology.

6.2 The APTS-OA test structure

As already mentioned, the APTS-OA is a (1.5×1.5) mm² chip consisting of a 4 $\times$ 4 pixel matrix with 10 μ m pitch and 16 analogue output channels. A picture of the chip obtained with a microscope is shown in Fig. 6.3. The sensor concept is n-on-p and it features an octagonal-shaped *n*-well collection electrode with 1.14 μ m diameter and a high-resistivity *p*-type epitaxial layer with a thickness ~ 10 μ m, grown on top of a low-resistivity *p*-doped substrate [138]. The sensor is labelled as AO10 and three different processes have been designed and produced, as detailed in 3.4.3: the standard (AO10), the modified with blanket implant (AO10B) and the modified with an implant with gap (AO10P), for simplicity called modified with gap [75][74]. Some relevant features of the APTS-OA are summarised in Tab. 6.1. In the following, some details about the analogue circuit of the APTS-OA are provided.

The analogue circuit

Figure 6.4 shows the front-end circuit of the APTS-OA. The sensor is represented by the diode and the pixel collection electrode (IN) is connected to an analogue front-end circuit working between 1.2 V (AVDD) and ground and buffering the signal to an output pad (BOARD). The circuit is partially implemented in each pixel with a first buffering stage composed by two source followers, a reset mechanism and the pulsing. The first PMOS follower buffers the IN signal to OUT1, while the second NMOS follower buffers it out to OUT2. These source followers are biased by two current sources: I_{biasp} and I_{biasn} . Afterwards, in the pixel peripheral circuit, a fast operational amplifier (OPAMP) drives the output stage. The circuit also provides a pulsing circuit which allows to inject charge at the input of the front-end exploiting an injection capacitance $C_{inj} = 242$ aF (nominal value), and a reset mechanism. The injected charge is managed by an external voltage (V_h), indicating the amplitude of the pulse applied to the injection capacitor C_{inj} and therefore regulating the injected charge.

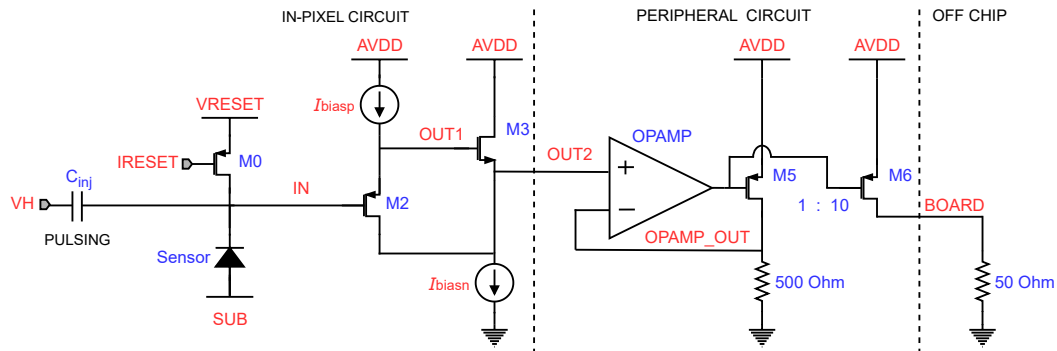


Fig. 6.4 APTS-OA front-end circuit with the circuitry inside the pixel (in the left part) and that located in the periphery of the matrix (in the right part). Figure from [139].

There are two main processes causing the discharge of the sensing node IN: the leakage current and the collection of charge generated by an impinging particle. Since a too large discharge may bring the IN node to a voltage outside the operational margin of the readout circuit, some mechanism must be applied to remain in stable conditions. Therefore, the crucial role of the PMOS transistor M0 needs to be stressed: when a particle crosses the sensor, the generated current induces a voltage drop on the input node (IN), turning on the reset transistor M0 which deliver a constant current I_{reset} . In this way, the sensing node is connected to the

reset potential V_{reset} and this phase is called reset mechanism. Without a hit, instead, the transistor has to compensate only for the leakage current of the sensor and to keep the collection electrode at a voltage close to V_{reset} . The I_{reset} current needs to be larger than the sensor leakage current, since it has to reset the electrode to its baseline in a time window of few microseconds.

The NMOS source follower output (OUT2) is then connected to a high-speed (1.9 GHz unity-gain bandwidth in post layout simulation) OPAMP, located at the matrix periphery and followed by an output stage driving a $50\ \Omega$ load (OFF CHIP). The signal coming from the inner 2×2 sub-matrix can be read-out with a fast, high bandwidth oscilloscope to get a precise timing information, while the external pixels can be readout with analogue to digital converters (ADCs).

The in-pixel and out-of-pixel power consumptions per pixel, estimated from the front-end biases, are $150\ \mu\text{W}$ and $3.1\ \text{mW}$ respectively. It is worth noticing that no signal shaping is performed at chip level, therefore the measured waveforms differ in shape depending on the collected charge.

6.3 Laboratory characterisation

6.3.1 Test setup

The setup employed to operate the APTS-OA was developed by a collaboration of different INFN Departments [142] and is shown in Fig. 6.5. It is composed by:

- a **data acquisition board (DAQ)** which was based on the ALPIDE DAQ board. It is powered at 5 V and connected to the PC via a USB 3.0 interface (mediated by Infineon's EZ-USB FX3), from which the power, pulsing and configurations are controlled. It hosts an FPGA (Altera Cyclone IV) and eight I/O LEMO connectors can be employed to apply back-bias voltage and operate the system in a telescope with trigger and busy chain. A PCIe connector allows to operate a proximity board.
- a **proximity board**, specifically developed for each test structure, with several roles:

- it houses the ADCs used to readout the peripheral pixels with a fixed sampling rate of **4 MS/s**, as the DAQ board only supports sensors with digital readout.
 - is responsible to deliver voltages and current biases to the front-end and the operational amplifier via two on-board 16-bit DACs which are then supplied via PCIe connector to the chip, where an ad hoc mirroring ratio is applied.
 - it hosts two voltage regulators, responsible to provide an output voltage of 3.3 V to the the proximity itself and 1.2 V to the chip.
- a **carrier board** on which the chip is glued and bonded through wire bonds. The carrier board features four high bandwidth SMA connectors to send the output of the four innermost pixels (highlighted in red in Fig. 6.5) to an oscilloscope, while the external pixels are readout via ADCs.
 - an **oscilloscope**: the Teledyne Lecroy, WaveMaster 813Zi-B was employed in this work, featuring a sampling rate of **40 GS/s** and a bandwidth of 13 GHz.
 - **PC with DAQ software**: the APTS-OA chip is connected to the PC running the DAQ software, which is responsible to configure the readout system, the bias currents and voltages and handle the data taking.

6.3.2 Working point optimisation

The response of the frond-end circuit was experimentally tested, via charge injection, in different configurations. Starting from the front-end nominal settings, several combinations were investigated looking for the fastest and more stable front-end response; this study allowed to establish the best working conditions, hereafter called operating point, for measuring timing resolution. First tests were carried out to characterise the chip in terms of signal amplitude, baseline and fall time. It is worth noticing that the signals feature a negative polarity. The following definitions are adopted in this stage of the work:

- **amplitude**: peak to peak amplitude of the signal;

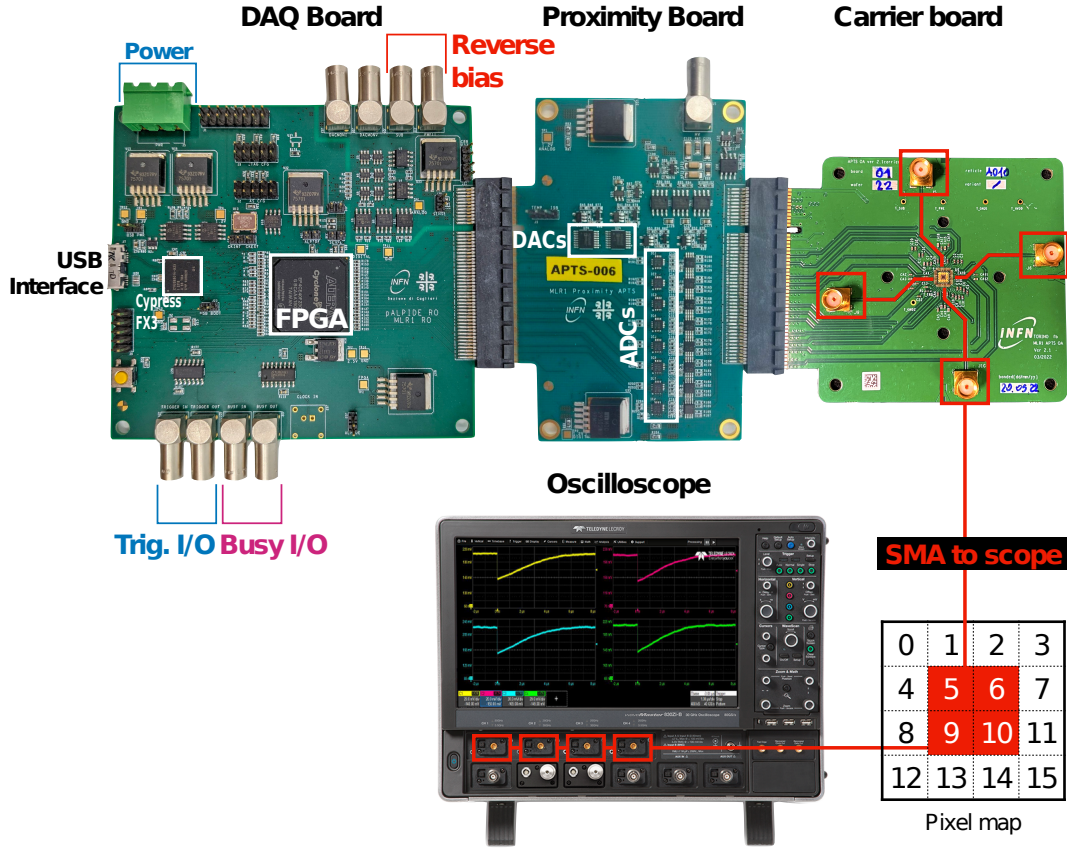


Fig. 6.5 Schematic representation of APTS-OA readout system. The DAQ board hosts the firmware, trigger, busy, and reverse bias connection. The proximity board hosts ADCs for external pixel readout, and on the carrier board the chip is glued and bonded. Image source [139].

- **baseline:** average of 100 samples of the waveform (corresponding to 2.5 ns) prior to the signal formation;
- **fall time:** time difference between the 10% and 90% of the signal amplitude;
- **slope:** $\Delta V/\Delta t$ ratio in the 10% - 90% range of the signal formation. It represents a key parameter as an increase of the slope translates into a reduced jitter and an improved timing performance (see Sec. 2.1).

A typical waveform from a test pulsing signal is represented in Fig. 6.6 showing its negative polarity, with a zoom on the falling edge of the signal on the right panel. The amplitude of the pulsing signal was fixed to $V_h = 1.2$ V. All the recommended operating conditions suggested by the designer group, listed in Tab. 6.2, were applied at first. All the currents hereafter reported are the ones applied to the chip and

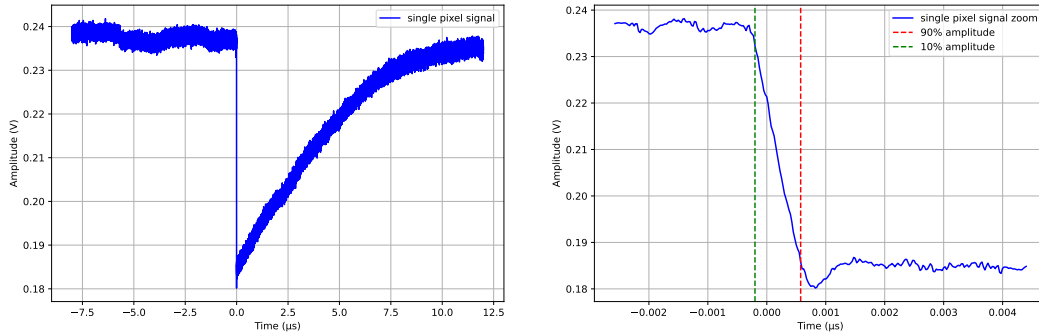


Fig. 6.6 Signal from one pixel (left) when pulsing the chip and zoom on the falling edge (right) showing the time interval used to define the fall time.

therefore corrected for the proper mirror ratio.

In all the measurements, when the chip was operated at different reverse biases, the same negative voltage referred to as V_{sub} , applied to the substrate, was applied also to the p-wells, V_{pwell} .

In-pixel		Out of pixel	
V_{reset}	200 mV	I_{bias3}	200 μA
I_{reset}	100 pA	I_{bias4}	2.5 mA
I_{biasn}	-200 μA	V_{casn}	750 mV
I_{biasp}	20 μA	V_{casp}	300 mV

Table 6.2 Nominal front-end circuit operating conditions. The mirror ratio to the front-end circuit has been already applied.

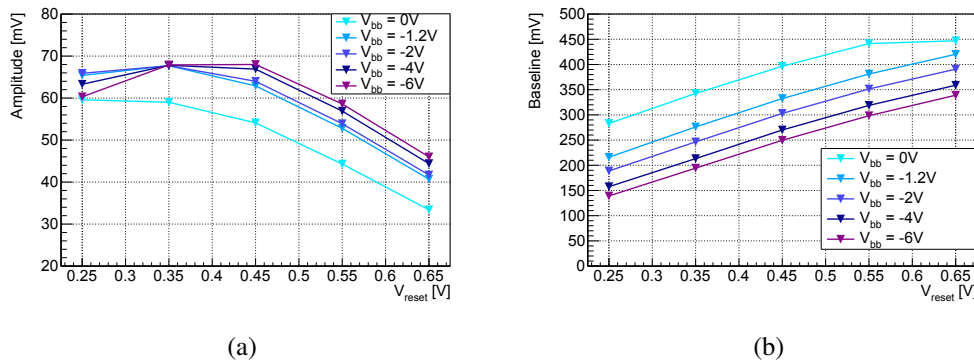


Fig. 6.7 Baseline (a) and amplitude (b) as a function of V_{reset} for different V_{bb} .

Effect of V_{sub} and V_{reset}

The front-end response to V_{reset} ¹ variations, was investigated as a first step. Figure 6.7a shows that as the reverse bias (V_{bb}) increases, the maximum of the amplitude is found at higher V_{reset} . For high values of V_{reset} , the amplitude drops as the front-end input stage of Fig. 6.4 is pushed against the AVDD power rail. Indeed, the effect of high, as well as very low, values of V_{reset} cause ultimately the output to saturate, either because the PMOS follower output goes against the AVDD, or the NMOS follower output approaches ground. This creates a minimum and a maximum voltage for V_{reset} , defining a range where the circuit can be operated normally without saturation effects.

Looking then at Fig. 6.7b, it's possible to observe that also the baseline is influenced by the reverse bias as the higher the V_{sub} , the lower the baseline. However, it is possible to adjust it by increasing V_{reset} , restoring a higher baseline. This is important because one ideally should place the working point in a linearity regime, trying to maximise the amplitude (keeping in mind the negative signal polarity), enhancing the SNR, and minimise the fall time, reducing the jitter. During these first assessment tests, it emerged that the circuit was squeezed between two limits: from Fig. 6.7b, the upper limit is reached around $V_{reset} \sim 0.55$ V with full baseline saturation already evident for the 0 V reverse bias, while, on the other hand, the amplitude already starts decreasing at 0.35 V, but only at that point one starts to create margin for gain using reverse bias.

A systematic optimisation of the operating point was therefore necessary because the NMOS transistors are in a p-well at voltage V_{sub} . Since this voltage can reach values beyond the range where the transistors were characterised, a model was used in the simulations to set the nominal working point, but was found in the end to deviate significantly from measurements [143]. As the reverse bias increases, the threshold voltage V_T of the NMOS transistors increases if their substrate is not connected to their source, which is the case for transistor M3 in Fig. 6.4. The increase in V_T of M3 due to the reverse bias causes the output of the NMOS follower (the source of M3) to approach the ground. In other words, an increase in reverse bias translates into a decrease in the margin of the circuit. From the above considerations, a systematic test campaign was carried out, deeply investigating the effects of the different biases of the front-end circuit, one by one. In particular, at first the bias

¹representing the voltage at the sensing node (see Fig. 6.4)

currents in the in-pixel follower branches were varied, in order to see the effect on the circuit performance. Thereafter, all the biases were changed together, with the aim of increasing the margin of the circuit without degrading its speed.

I_{biasp} and I_{biasn} investigation

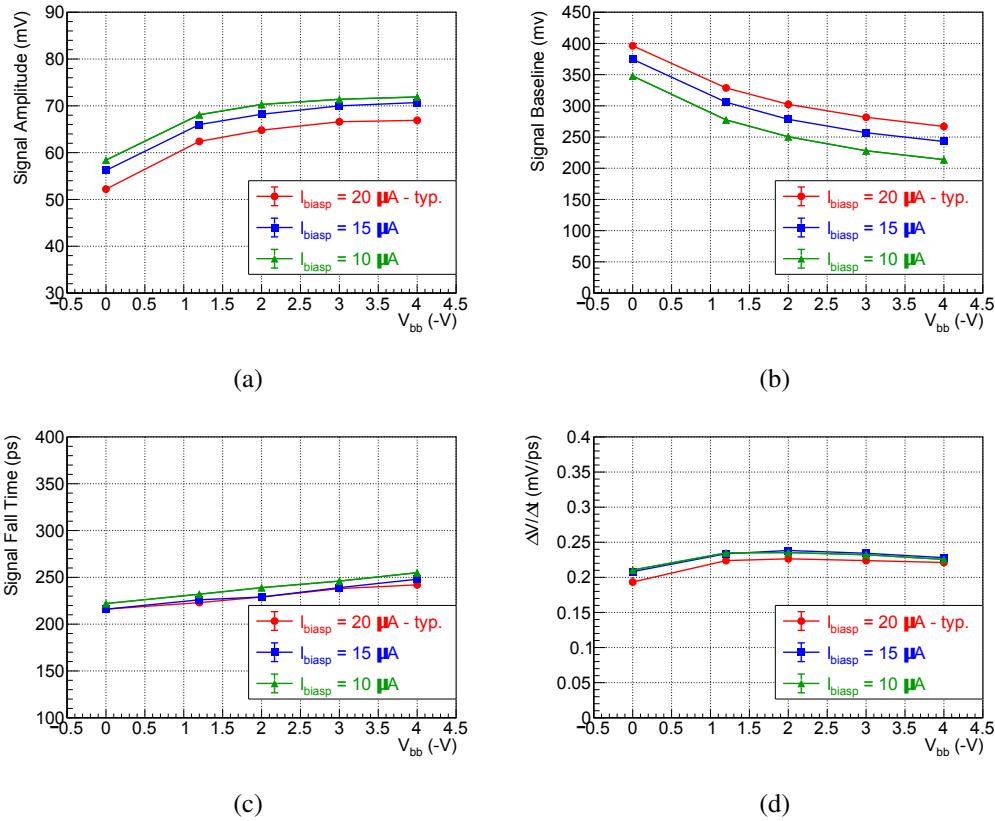


Fig. 6.8 Effect of the I_{biasp} current on the amplitude, baseline, fall time and slope of the signal. The red markers refer to the typical configuration (typ.). All the measurements have been performed by pulsing 500 times a pixel of the matrix, keeping V_{reset} fixed at 0.35 V, I_{biasn} at $-75 \mu\text{A}$ and all the other settings as the typical ones.

The effect of the I_{biasp} and I_{biasn} currents have been studied fixing V_{reset} at 0.35 V, since the amplitude is set around its maximum for all the V_{sub} , as can be seen in Fig. 6.7a. The following plots show the amplitude, baseline, fall time and slope as a function of the reverse bias for different I_{biasp} and I_{biasn} values, in order to deeply understand the interplay between the current settings of the two follower branches. Every data point is the average value of $N = 500$ pulses in that particular configura-

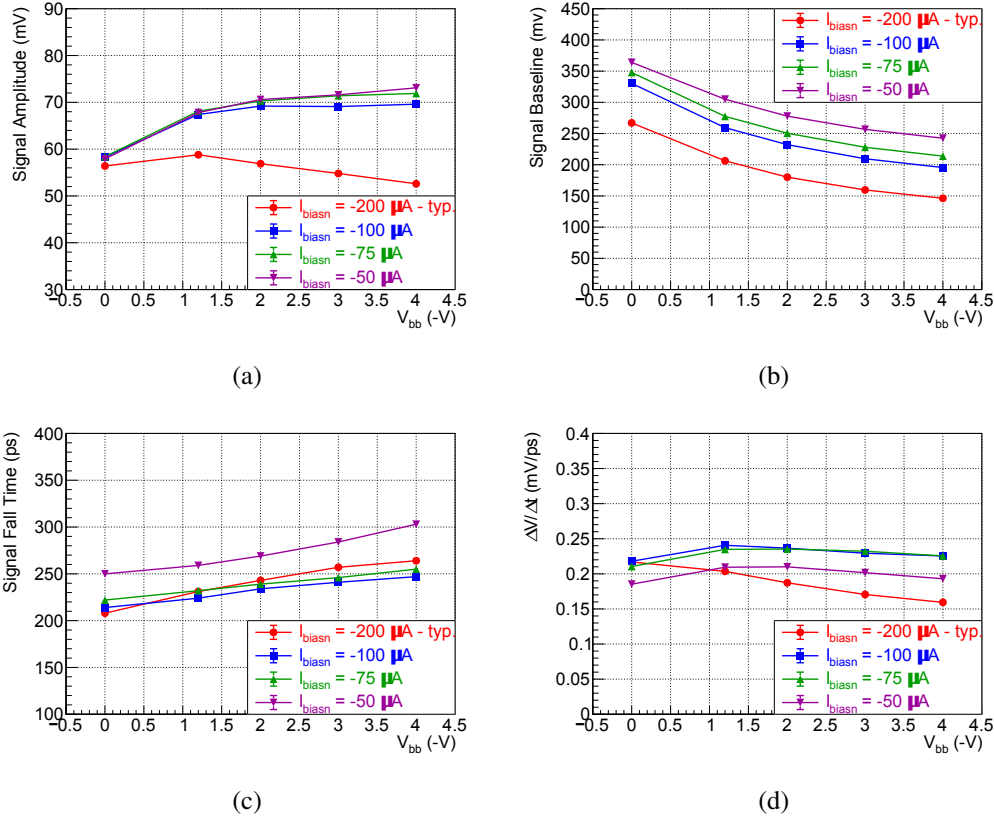


Fig. 6.9 Effect of the I_{biasn} current on the amplitude, baseline and fall time. The red markers refer to the typical configuration (typ.). All the measurements have been performed by pulsing 500 times a pixel of the matrix, keeping V_{reset} fixed at 0.35 V, I_{biasp} at $10 \mu A$ and all the other settings as the typical ones.

tion². In Fig. 6.8, it's possible to observe the effect of the I_{biasp} current, comparing its nominal value of $20 \mu A$ with two lower ones. Decreasing the I_{biasp} clearly improves the signal amplitude, accordingly to previous considerations in 6.3.2. Looking then at the fall time in Fig. 6.8c, only a small speed penalty can be observed with the $10 \mu A$ configuration, which can be considered negligible, also by looking at the slope in Fig. 6.8d, meaning that the time performance of the front-end circuit is not compromised by reducing this current. For the above illustrated reasons, the I_{biasp} $10 \mu A$ configuration was selected for further tests.

Fixing now I_{biasp} , a similar study was carried out to investigate the effect of the

²The error bars have been computed as $\frac{RMS}{\sqrt{N}}$. The error on the slope has been computed considering independent errors on the amplitude and fall time and applying the formula for the error propagation on a derived quantity.

I_{biasn} on the signal. From Fig. 6.9a, it's clear to see the benefit of reducing this current from its typical value of $-200 \mu\text{A}$. Indeed, it strongly enhances the amplitude when increasing the reverse bias, with an increase larger than 30% at $V_{\text{bb}} = -4 \text{ V}$, when compared to the nominal setting. At the same time, reducing this current produces a systematic increase of the baseline (Fig. 6.9b), giving in this way more margin to the circuit. Finally, the fall time is not degrading appreciably, except for the $-50 \mu\text{A}$ configuration. Looking at the slope in Fig. 6.9d, it's possible to observe its increase until the $-75 \mu\text{A}$ configuration, followed by a visible decrease for the $I_{\text{biasn}} = -50 \mu\text{A}$, meaning that a lower limit was reached with the $-75 \mu\text{A}$ and going beyond would have compromised the speed performance of the circuit. Even from these preliminary characterisations, it was already evident the need for a more exhaustive study, evaluating all the possible front-end parameter combinations, in order to find the best working point to operate the APTS-OA chip.

The adopted methodology

Starting from the acquired knowledge of the above presented studies, different combinations of the front-end parameters, listed in Tab. 6.2, were investigated, looking for the fastest response and the widest stability in the operational region of the circuit. In particular, a key objective was to achieve linearity in the front-end circuit transfer function $f_T = V_{\text{OUT}}(V_{\text{IN}})$. Non-linearity may arise due to saturation effects in the PMOS or NMOS source follower stages [35]. The differential DC gain g_j of the front-end circuit for a generic pixel j can be defined as the derivative of the output with respect to the input, or, in other words, as the derivative of its transfer function:

$$g_j = \frac{dV_{\text{OUT},j}}{dV_{\text{IN},j}} \quad (6.1)$$

where V_{IN} is the voltage applied at the collection electrode and V_{OUT} is the measured output voltage. Operatively, it can be measured by varying V_{reset} , changing in this way the applied voltage at the sensing node and measuring the output voltage V_{OUT} , which corresponds to the baseline. The workflow followed to optimise the chip front-end settings is here illustrated for a generic pixel j :

1. perform a *coarse scan* for the six front-end parameters (V_{casn} , V_{casp} , I_{biasn} , I_{biasp} , I_{bias3} , I_{bias4}) at all the reverse biases (from 0 V to -4.8 V with step of 1.2 V). For each parameter choose three values in the coarse range and execute:

- 100 pulses for all the 729 (3^6) combinations of voltages and current biases with V_{reset} ranged from 20 mV to 900 mV with 20 mV step;
 - measure the average fall time, amplitude and baseline in each configuration;
2. apply a matrix of cuts, aiming at:
 - reducing the fall time;
 - maximising amplitude and baseline;
 3. select the group of configurations with best derivative $\frac{dV_{\text{OUT}}}{dV_{\text{IN}}}$ (high DC gain and large plateau);
 4. make a refined study among the survived configurations and extract the optimal configuration.

More details about each of these step can be found in Appendix D.1. The following

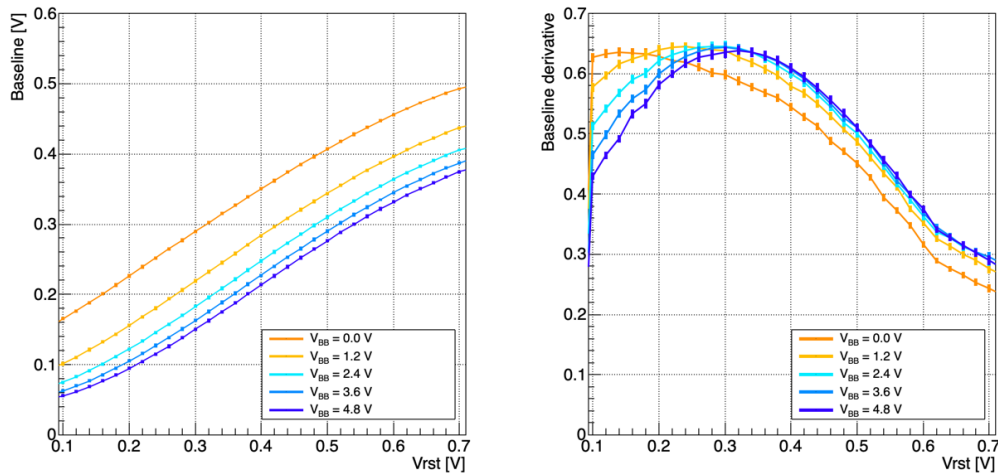


Fig. 6.10 Baseline (transfer function f_T , left panel) and baseline derivative (right) as a function of V_{reset} for different reverse biases. Modified process variant. Courtesy of U. Savino.

plots illustrate the quantities of interest as a function of V_{reset} after the best working configurations were obtained for the different reverse biases.

Fig. 6.10 (left) shows the baseline (V_{OUT}) of a pixel (pixel 5 chosen as reference) for five different reverse biases. It's immediate to recognise the offset between the curves, already encountered at the beginning of this study (see Fig. 6.7), in particular the baseline lowers when increasing in module the V_{sub} , here indicated as V_{bb} . This

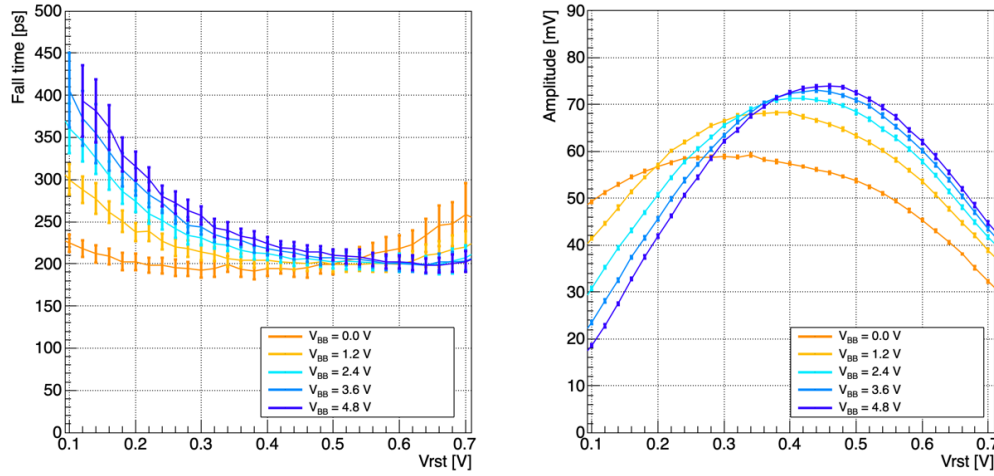


Fig. 6.11 Fall time (left) and amplitude (right) as a function of V_{reset} for different reverse biases. Modified process variant. Courtesy of U. Savino.

observed effect can be attributed again to the NMOS transistor M3, having the substrate connected to the p-well potential, which is therefore identical to V_{sub} . As a consequence, the characteristics of the NMOS transistor change, including an increase of the threshold voltage V_T with the reverse bias, as pointed out in 6.3.2, responsible for the different offsets after the NMOS source follower stage and visible in Fig. 6.10. Fig. 6.10 (right) shows the baseline derivative (i.e. the differential gain) of the front-end circuit as a function of V_{reset} , computed as the slope of a mobile fit over 5 points. It can be observed that the measured gain is consistently below unity for all the reverse biases. For each reverse bias, there is a range of V_{reset} where the gain remains approximately constant, forming a plateau. As V_{bb} increases, the width of this plateau decreases and shifts towards higher V_{reset} values. This observed effect can again be explained by the dependence of the threshold voltage of NMOS transistor from V_{bb} . All these observations have been carefully taken into account when choosing the V_{reset} operating point for each reverse bias, which ideally should be placed in a region of constant differential gain.

Fig. 6.11 (left) illustrates the fall time as a function of V_{reset} for different reverse biases. At low V_{reset} , in saturation regime, the circuit slows down, worsening the fall time. Fig. 6.11 (right) represents the signal amplitude. When the signal develops in the linear gain region, the amplitude reaches its maximum. An increase in V_{bb} leads to a decrease of the pixel input capacitance C_d , as it lowers the sensor capacitance

thanks to the depletion (see App. D.2), but also has an effect on the threshold voltage of the NMOS transistors, as already pointed out. A complicated interplay of these different effects contributes to the observed trend.

6.3.3 Measurements with the pulsing circuit

After the definition of the working point, the APTS-OA chips were characterised by analysing the response of different pixels when a specific amount of charge was injected through the pulsing circuit (see Fig. 6.4). The full matrix was pulsed varying the amplitude of the pulsing signal V_h from 0.3 V to 1.2 V with steps of 0.1 V. Fig. 6.12 shows the signal amplitude of the four central pixels (named J5, J6, J9 and J10) of a modified with gap process as a function of V_h for different V_{sub} . The expected linear trend can be observed together with an increased slope with reverse bias. This behavior can be attributed to the lower input capacitance due to the sensor depletion, as can be seen in App. D.2. The signal amplitudes measured on different

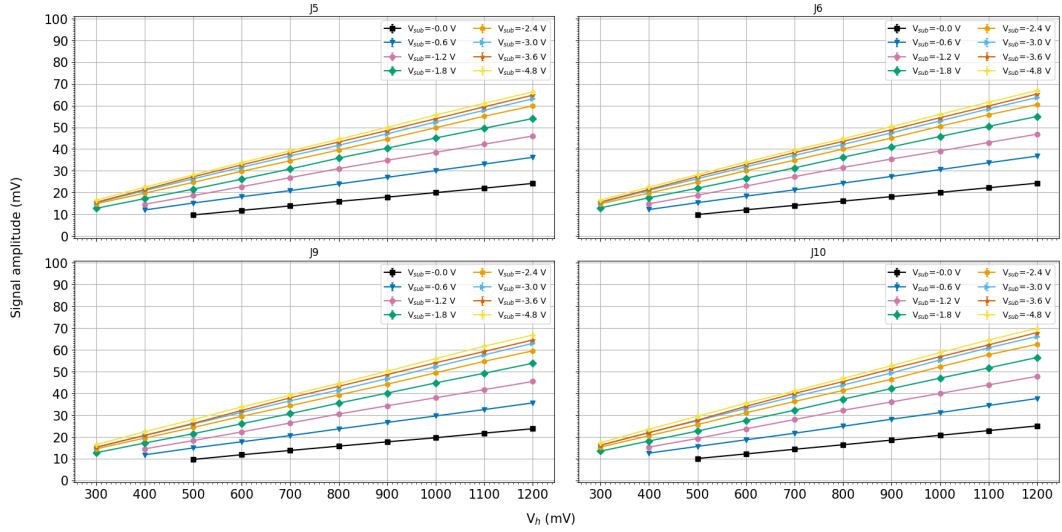


Fig. 6.12 Signal amplitude as a function of V_h for different reverse bias for the four central pixels of a AO10P chip.

pixels feature a pixel-to-pixel variation that can be quantified through a maximum dispersion percentage $\sim 5\%$. Fig. 6.13 represents the slope dV/dt computed by considering the usual interval 10% - 90% of the signal amplitude. An increase of the slope with the amplitude of the pulsing signal can be observed, together with an improved timing performance of the front-end with the reverse bias. Of course one

has to remember that the reverse bias is provided not only to the sensor substrate, but also to the p-wells in which the NMOS transistors are located. This means that a change in the V_{sub} has an effect on both the sensor capacitance C_d and on the electronics and in this study we are observing the combined effect of the two. The enhancement of the signal slope with V_h and V_{sub} brings to a decrease of the signal jitter (cfr. 2.1), which is desired to improve the timing performance.

The same characterisation results carried out on a AO10 standard process are

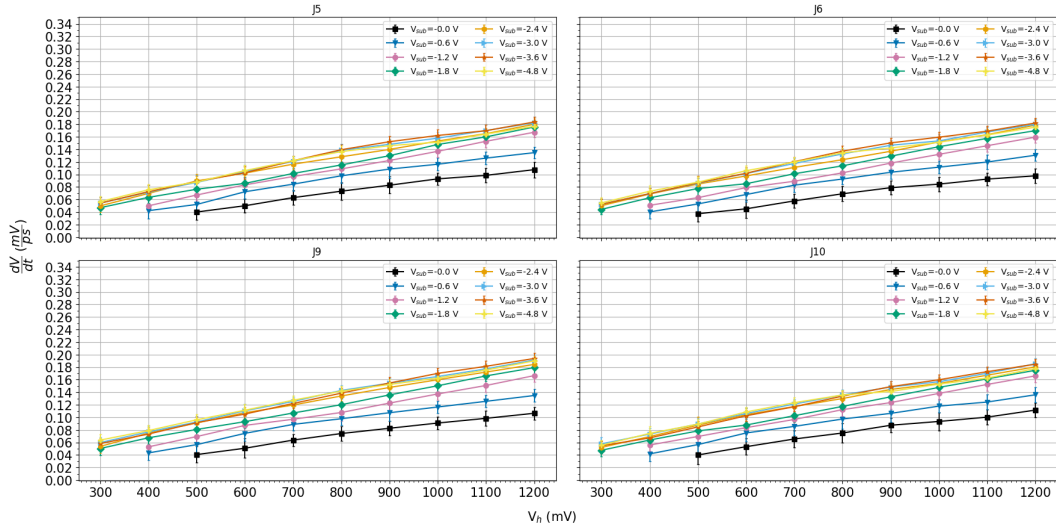


Fig. 6.13 Signal slope as a function of V_h for different reverse bias for the four central pixels of an AO10P chip.

reported in App. D.3, where it's possible to observe the lower effect of the reverse bias on both amplitude and signal slope.

Jitter measurements

The jitter contribution to the time resolution of the APTS-OA chip was estimated. Jitter was measured as the standard deviation of the distribution of the time difference Δt between the half height of two output pulse signals coming from different pixels on the same chip. In particular, in this study, pairwise jitter measurements were performed by pulsing the four internal pixels of an AO10P chip. The jitter of the individual pixels can therefore be retrieved mathematically through the relationships between the pixels. Specifically, if the jitter values between the pairs are assumed to

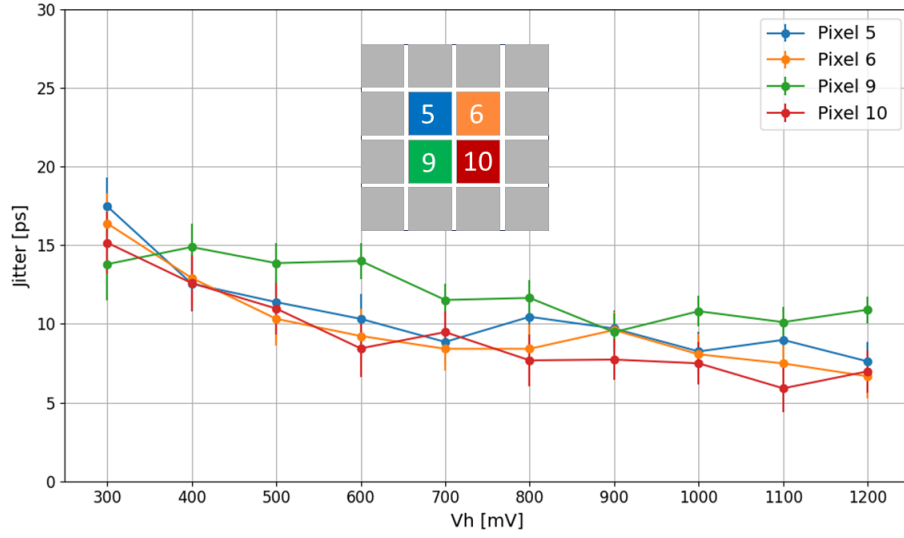


Fig. 6.14 Jitter of the four central pixels of a AO10P chip, measured at -4.8 V.

be a combination of the independent contributions of each pixel in the pair, one can write the pairwise jitter in terms of individual contributions:

$$\sigma_{1-2}^2 = \sigma_1^2 + \sigma_2^2, \quad \sigma_{1-3}^2 = \sigma_1^2 + \sigma_3^2, \quad \sigma_{1-4}^2 = \sigma_1^2 + \sigma_4^2, \quad \dots$$

For example, it's possible to compute σ_1^2 writing the following system of two equations:

$$\begin{cases} \sigma_2^2 = \sigma_{1-2}^2 - \sigma_1^2 \\ \sigma_3^2 = \sigma_{1-3}^2 - \sigma_1^2 \end{cases}$$

and substitute these expressions in the σ_{2-3}^2 one. In this way, one can solve for σ_1^2 :

$$\sigma_1^2 = \frac{\sigma_{1-2}^2 + \sigma_{1-3}^2 - \sigma_{2-3}^2}{2} \quad (6.2)$$

The same approach was adopted for the other pixels (see App. D.4).

The error for each jitter value can be estimated through the general error propagation formula for a function of several variables. Fig. 6.14 shows the computed jitter for the four central pixels of the matrix as a function of the amplitude of the pulsing signal. As can be observed, the jitter is not influenced by the position of the

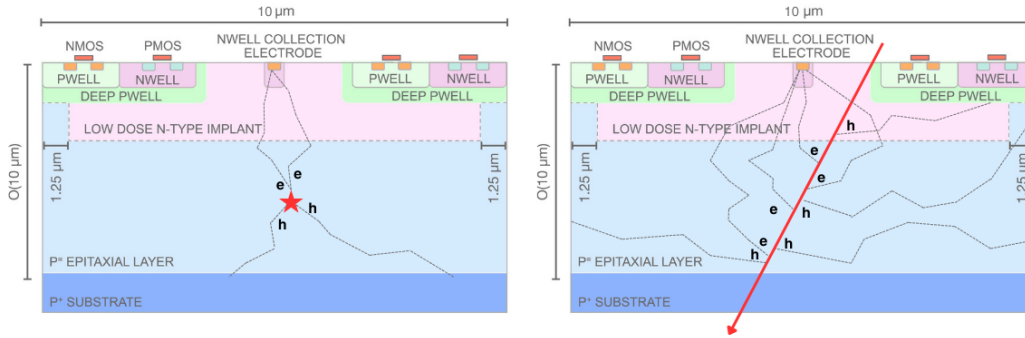


Fig. 6.15 Schematic representation of charge deposition by a photon (left) and by a MIP (right) in a modified with gap process cross section.

pixel and reaches a minimum value between 5 ps and 10 ps in the best case when V_h is 1.2 V.

6.4 Sensor response to X-rays

One of the main goal of the APTS-OA characterisation was the energy calibration through the study of the sensor response to a ^{55}Fe monochromatic source of soft X-rays. ^{55}Fe decays to ^{55}Mn by electron capture. ^{55}Mn from an excited state returns to its ground state by emitting photons in two emission modes with energies of 5.9 keV and 6.5 keV [144], as already described in detail in 1.3.2.

The attenuation lengths of such photons in silicon are $28\ \mu\text{m}$ and $37\ \mu\text{m}$ [19], respectively. Details about how photons and X-rays interact with silicon can be found in 1.3.2.

A point that must be stressed is that soft X-rays and MIPs are characterised by different energy losses and conversion processes: the former interact with silicon via photoelectric effect generating electron-hole pairs in a small point-like spatial region, while the latter generate e-h pairs almost uniformly along their track, in the crossed silicon volume. A sketch of the charge generation in a silicon sensor cross section can be observed in Fig. 6.15, where also the paths of electrons and holes are illustrated in a very simplified manner. The electrons are collected at the sensor nodes, located on the top side, while the holes are directed towards the substrate or the deep p-wells. The mean energy loss per unit of sensor thickness by charged particles in matter is described by the Bethe-Bloch formula (see Eq. (1.15)), but the most probable loss is much more relevant to detector calibration, since the tail is

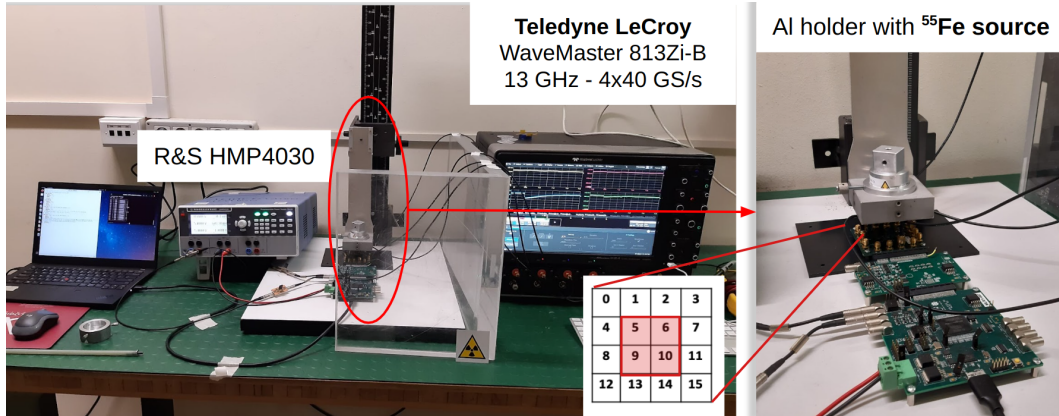


Fig. 6.16 Laboratory setup for measurements with the ^{55}Fe source equipped with PC, power supply, ^{55}Fe holder with carrier below (in the red circle), DAQ system, oscilloscope (left) and zoom on the holder with the source (right).

mainly due to a few high-loss events. The most probable loss is less than 70% of the mean for a typical silicon detector [145]. The most probable energy loss of a MIP is about 1.8 keV in a sensor of 10 μm active thickness [16] [146], lower than the energy of the X-rays from ^{55}Fe .

The following results concern test campaigns conducted with a ^{55}Fe source having a nominal activity of 37 MBq and an active diameter of 1 cm, illuminating the top side of an APTS-OA chip at a distance of approximately 2 cm. The source was placed in an aluminum holder produced ad hoc, in order to guarantee a proper stability during the measurements. The holder was equipped with a collimator having a diameter of 3 mm and a cover. A picture of the setup used in the measurements is reported in Fig. 6.16. The chip was operated with a reverse bias voltage of -4 V applied to the chip substrate and p-well. The four central pixels of the matrix were readout with the oscilloscope (Fig. 6.16, right), in order to be able to retrieve the time information from an offline analysis. The trigger was provided by a logic OR of the four central pixels of the matrix.

6.4.1 Methodology

The following definitions will be used in the discussion covering the next sections:

- **Seed pixel:** the pixel featuring the maximum signal amplitude in a cluster;

- **Seed signal:** the signal amplitude of the seed pixel;
- **Cluster signal:** the sum of the signals from the pixels within a cluster.

In this section the analysis methodology is described, starting from the gain correction applied to all the pixels and moving then to the energy calibration.

Gain correction

To calibrate the sensor response to X-rays, the well known nominal energies of the K_α and K_β peaks can be exploited. The general procedure is here presented using the data collected on the modified with gap sensor process, but it applies in the same way for all the processes. Before the energy calibration, a pixel-to-pixel equalisation procedure was applied, in order to merge the data collected from different pixels. The following approach was employed:

- the baseline derivative with respect to V_{reset} has been computed for each channel (see 6.3.2);
- events with cluster size 1 and fall time lower than 400 ps have been selected as reference signals for the energy calibration. The reason for this choice is a trade-off between the statistics and a clean distribution with clearly visible peaks. Fig. 6.17 shows a fall time vs amplitude plot for events with cluster size 1, in which a fast and a slow populations are highlighted. It has to be stressed that, since there is no shaping of the signal, the information in the plot is the result of the charge collection and of the front-end, which appears as an offset in the time. The fast component can be related to events where the X-ray has converted in a region close to the depletion region, below the collection electrode or, in general, in the shallow epitaxial layer. The charge collection is therefore dominated by drift because of the strong electric field, translating into a lower collection time. The slow component can be caused by events in which the X-ray converts in a more distant region from the electrode, where the field is lower and the charges are collected not only by drift, but also by diffusion. The single pixel cluster signal distributions of the four central pixels of the matrix are represented in Fig. 6.18 (not equalised), with superimposed Gaussian fits to the K_α (red) and K_β (blue).

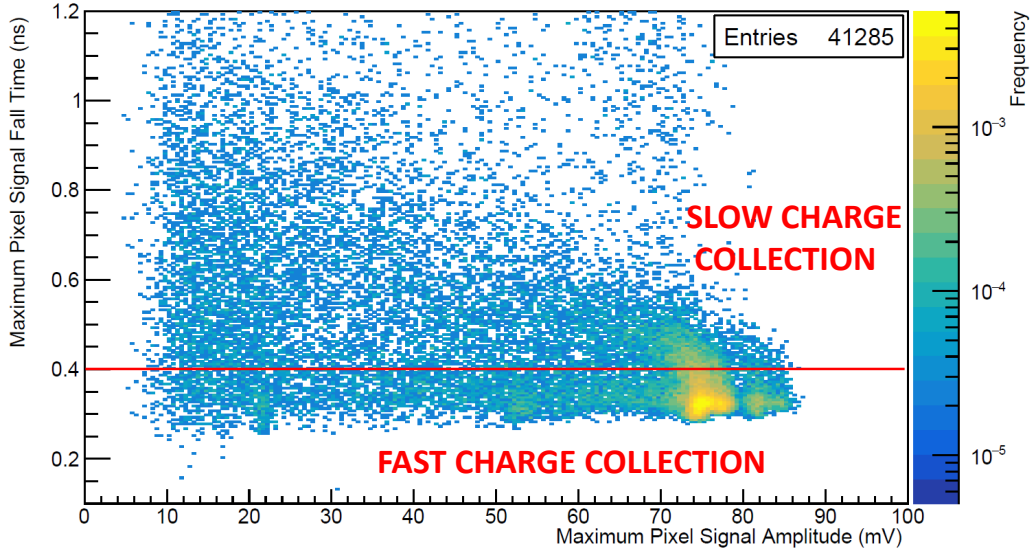


Fig. 6.17 Fall time vs amplitude for single pixel clusters of a modified with gap sensor process. The cut on the fall time at 400 ps is highlighted in red.

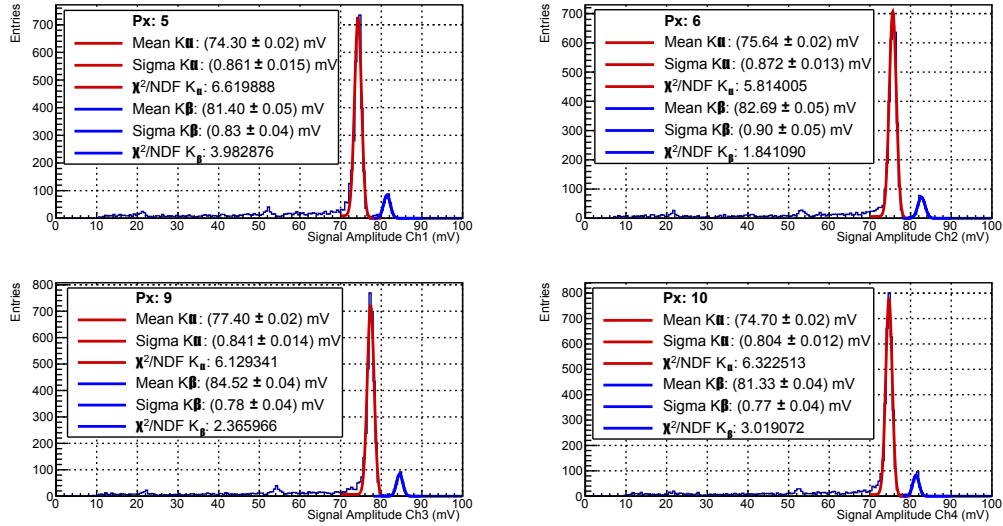


Fig. 6.18 Not equalised single pixel cluster signal distributions for the four central pixel of the AO10P chip.

- signals belonging to different pixels have been first equalised by applying a gain correction, i.e. dividing the raw signal amplitude of the pixel j for the derivative g_j corresponding to that pixel; Appendix D.5 shows the gain calibrated distributions corresponding to the four central pixels. The dispersion percentage among the K_α peaks decreases from 4% without the gain correction to 1.6% after the gain correction has been applied. This confirms that the correction mitigated the differences among pixels caused by the front-end.
- all the equalised pixel outputs can now be merged in one single distribution, where the K_α and K_β peaks are clearly visible. Fig. 6.19a represents the cluster signal distribution, obtained by summing all the signals within a cluster. The main peak in this distribution can be due to events in which the X-ray has converted in a region close to collection electrode (in the epitaxial layer) and all the generated charge is collected within the cluster. The tail located to smaller amplitudes can be due to an incomplete charge collection, happening for example when the X-ray is absorbed in the substrate and not all the charge is collected efficiently or some recombination occurred. Fig. 6.19b shows instead the resulting amplitude spectrum for the single pixel cluster signals with the cut on the fall time, asked to be lower than 400 ps; As it can be seen, the slow population attributed to charge sharing is strongly suppressed and also the Si- K_α and the Si- K_α -escape peaks start to become visible. The origin of these two peaks is described in App. D.6.

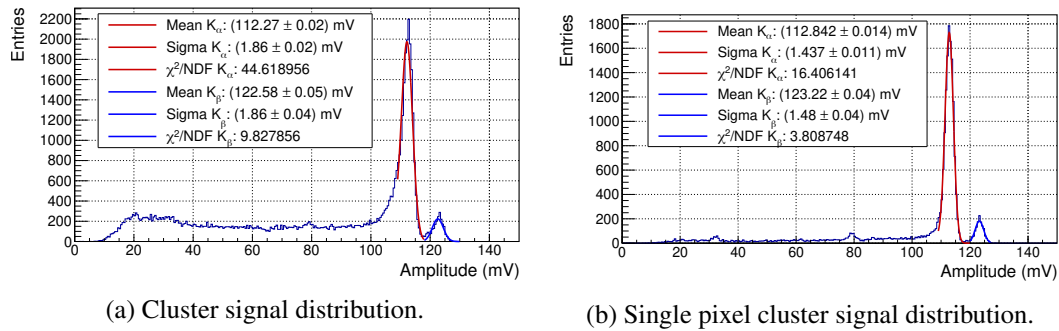


Fig. 6.19 Response of an A010 modified with gap process to X-rays from an ^{55}Fe source. Cluster signal distribution (left) and single pixel cluster signal distribution (right) with fall time < 400 ps. Superimposed Gaussian fit to the K_α (red) and K_β (blue) peaks.

From Fig. 6.19, it's possible to estimate the cluster Charge Collection Efficiency (CCE) as the ratio between the mean values of the Gaussian fit on the K_α peaks. In this case, the Cluster CCE is (0.9949 ± 0.0002) .

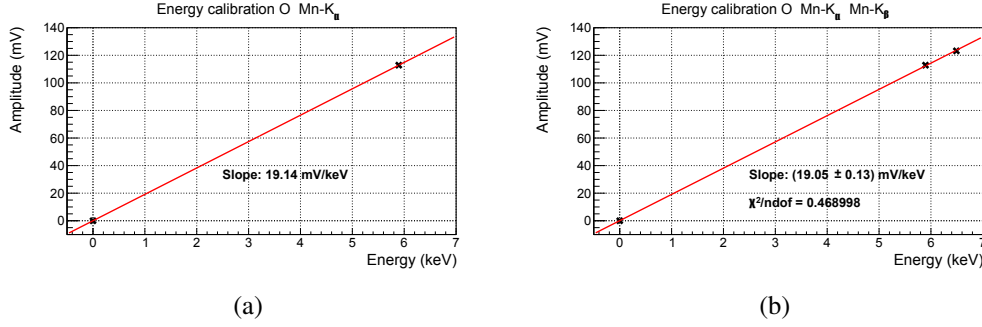


Fig. 6.20 Amplitude vs energy calibration line using the K_α peak and the (0,0) point (left) or the K_α , K_β and (0,0) (right).

Energy calibration

The energy calibration is performed exploiting the information of the peaks' position. Figure 6.20 illustrates the amplitude vs energy calibration line, obtained by considering a two or three points calibration. In the first case only the origin and the K_α peak have been considered³, while in the second case also the K_β peak was employed. A more precise calibration to low energy values could be obtained by adding the Si- K_α and the Si- K_α Escape peaks in the calibration line. Fig. 6.21a reports the single pixel cluster gain corrected amplitude distribution with superimposed fits to all the four peaks. The fit parameters are listed in Tab 6.3. Fig. 6.21b shows the resulting calibration line obtained with these four peaks. The slopes of the calibration lines achieved with the three different methods feature a negligible maximum difference around 1%, suggesting a consistency between the three calibration methods. The ratio of the energy over amplitude can be easily computed as⁴:

$$\frac{E \text{ (keV)}}{A \text{ (mV)}} = 0.0522 \frac{\text{keV}}{\text{mV}} \quad \mathbf{O, Mn-K}_\alpha$$

$$\frac{E \text{ (keV)}}{A \text{ (mV)}} = (0.0525 \pm 0.0004) \frac{\text{keV}}{\text{mV}} \quad \mathbf{O, Mn-K}_\alpha, \mathbf{Mn-K}_\beta$$

$$\frac{E \text{ (keV)}}{A \text{ (mV)}} = (0.0520 \pm 0.0005) \frac{\text{keV}}{\text{mV}} \quad \mathbf{Si-K}_\alpha, \mathbf{Si-K}_\alpha\text{-Esc}, \mathbf{Mn-K}_\alpha, \mathbf{Mn-K}_\beta$$

Since no relevant differences were observed in between the three calibration methods, the simplest one was adopted, i.e. the two points calibration. In conclusion,

³The energy of the K_α peak has been estimated as a weighted average of the $K_{\alpha 1}$ and $K_{\alpha 2}$ photon energies reported in Tab. 1.2

⁴The errors on the inverse of the slope have been computed with the propagation formula:
 $\Delta(\frac{1}{m}) = \frac{\Delta m}{m^2}$

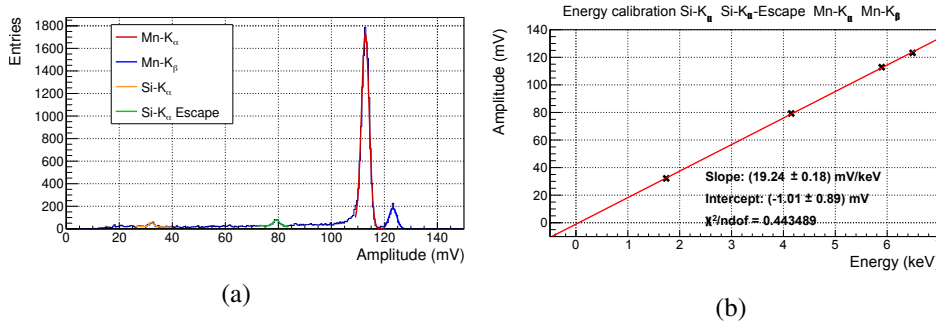


Fig. 6.21 Single pixel cluster distribution, after the gain correction has been applied with superimposed Gaussian fit to the Si-K α , Si-K α -Escape, Mn-K α and Mn-K β peaks (left). Calibration line obtained with four points (right).

Parameter	Value
Mean K α	(112.842 $\pm$ 0.014) mV
Sigma K α	(1.437 $\pm$ 0.011) mV
χ^2 /NDF K α	16.4
Mean K β	(123.22 $\pm$ 0.04) mV
Sigma K β	(1.48 $\pm$ 0.04) mV
χ^2 /NDF K β	3.8
Mean Si-K α	(32.18 $\pm$ 0.13) mV
Sigma Si-K α	(0.93 $\pm$ 0.12) mV
χ^2 /NDF Si-K α	1.7
Mean Si-K α Escape	(79.28 $\pm$ 0.11) mV
Sigma Si-K α Escape	(1.16 $\pm$ 0.13) mV
χ^2 /NDF Si-K α Escape	0.6

Table 6.3 Fit results corresponding to Fig. 6.21a and corresponding χ^2 /NDF values.

to energy calibrate every channel, first the correction with the proper gain factor has been applied and afterwards the energy calibration has been performed, ending up with the energy spectra as shown in Fig. 6.22 for the four pixels separately. The histograms show the events with cluster size 1 and fall time < 400 ps, as done in Fig. 6.18 for not calibrated data. The K α and K β peaks are fitted with a Gaussian function with a linear background. Appendix D.7 illustrates the cluster energy distribution, obtained from Fig. 6.19a after the energy calibration was completed.

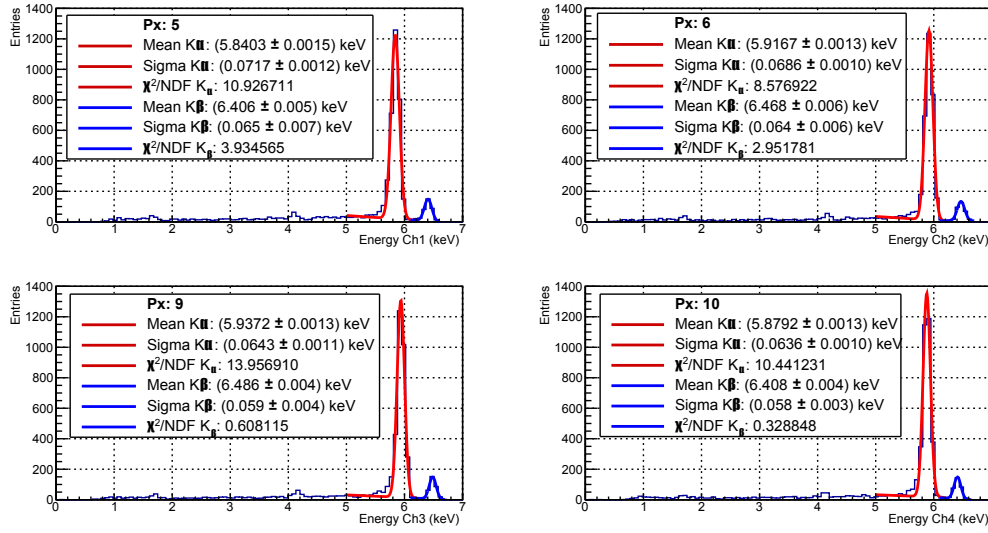


Fig. 6.22 ^{55}Fe energy distributions on the four central pixels, considering events with cluster size one and fall time lower than 400 ps.

6.4.2 Results

Figure 6.23 shows the maximum pixel energy distributions obtained for the standard and for the modified with gap sensor processes superimposed. A clear difference emerges between the two: the standard process, without the low dose n-type implant, shows a great charge sharing component, visible in the population of events with low amplitudes, while the modified with gap has a more pronounced K α peak and a decreased charge sharing component. Fig. 6.24 shows the 2×2 matrix energy distributions for the standard and modified with gap sensors. The same comparison can be performed also on the amplitude distributions, reported for the sake of completeness in App. D.8.

Selecting now events with cluster size 1, the energy spectrum obtained is shown in Fig. 6.25. In particular, the purple histogram includes all the events with cluster size 1. By applying a constraint on the charge collection time, it's possible to select fast events in which charge is collected quickly, corresponding to the green histogram. As a consequence, the peaks emerge clearly from the spectrum: the Mn-K α and Mn-K β peaks are resolved, as well as the Si-K α and the Si-K α escape peaks. Fig. 6.26 shows the fall time vs amplitude distribution on the standard sensor flavor (left) and the modified with gap one (right), for events with cluster size 1 (top row) and cluster size larger than 1 (bottom row). As can be observed, the modified with gap

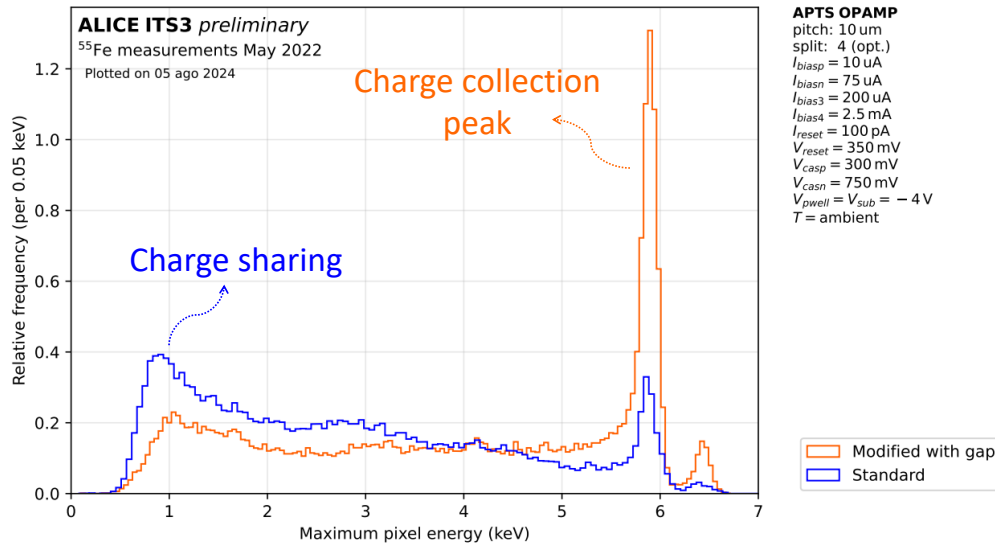


Fig. 6.23 Maximum pixel energy distribution for the standard (blue) and modified with gap (orange) sensor processes.

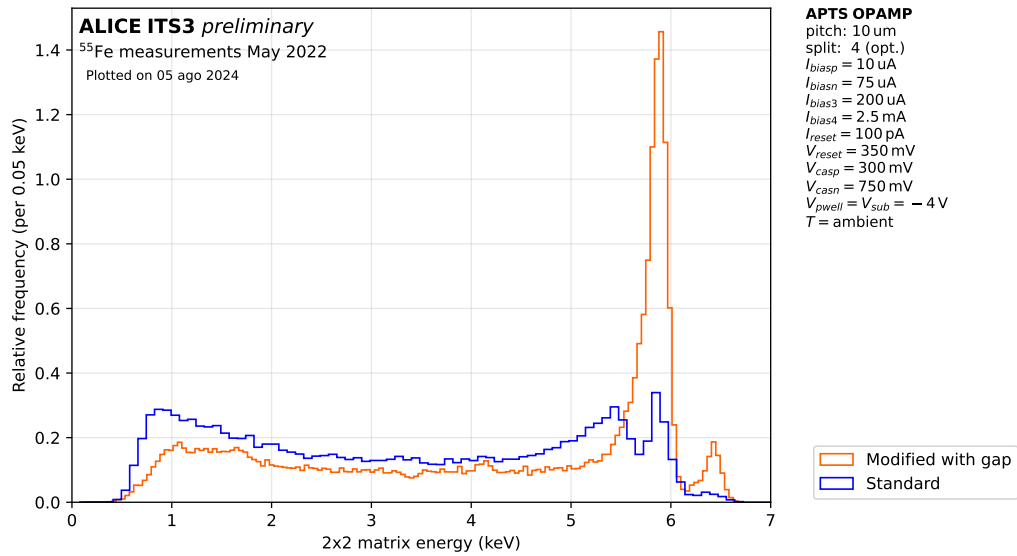


Fig. 6.24 2x2 matrix energy distribution for the standard (blue) and modified with gap (orange) sensor processes.

process suppresses slow events and it exhibits a larger fraction of events with high amplitude and low fall time. In particular, in the modified with gap sensor, the 80% of events with cluster size 1 lies in the region with a fall time lower than 1 ns, compared with the 20% of the standard process. This result is achieved thanks to

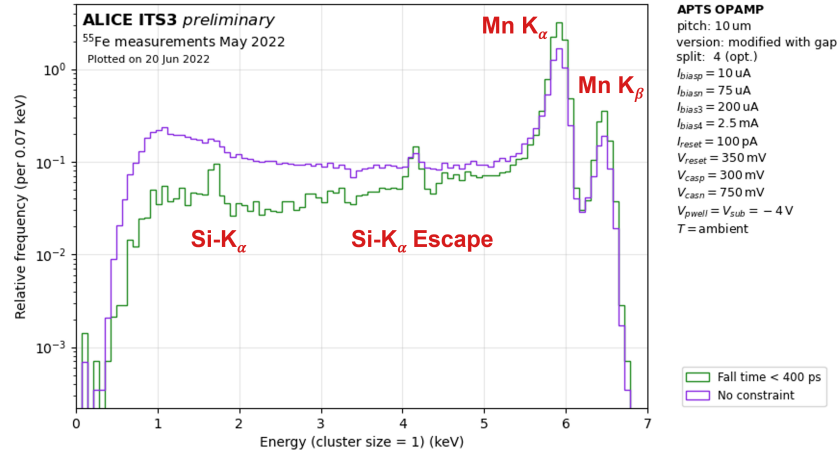


Fig. 6.25 ^{55}Fe energy spectrum measured on a modified with gap sensor process, considering events with cluster size one. In the green distribution only the events with fall time lower than 400 ps are selected, while in the purple one no cuts on the fall time are applied.

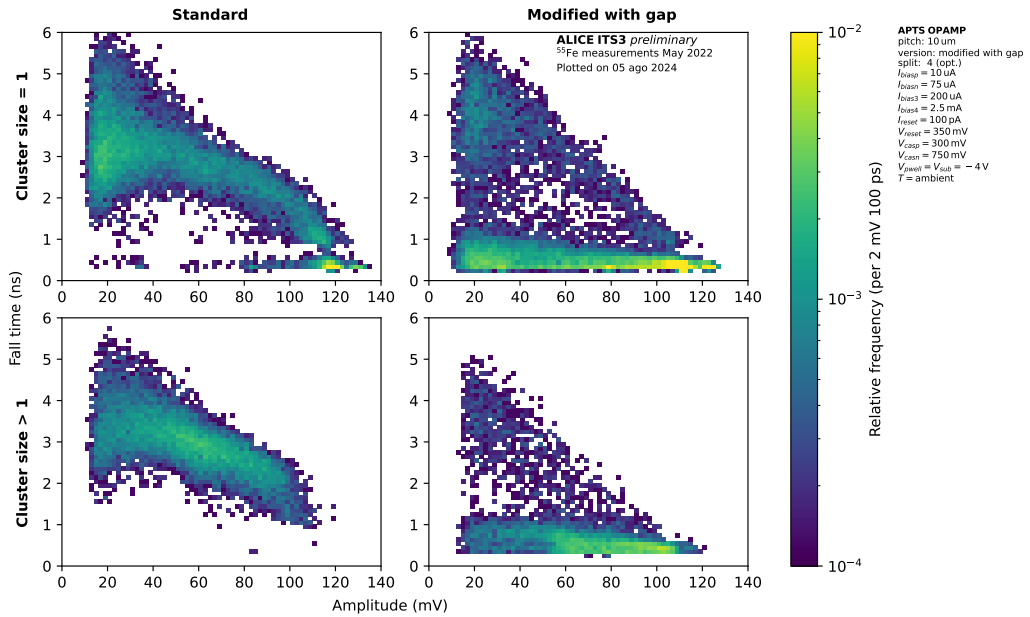


Fig. 6.26 Fall-time vs Amplitude distribution for standard flavor (left) and modified with gap flavor (right). In the first row, events with cluster size one and in the second row events with cluster size larger than one are displayed. The histograms are normalised to the total area.

the additional horizontal component of the electric field [75][74], that speeds up the charge collection process. Moreover, comparing the different cluster size, one can notice that even if there are some events with cluster size larger than one for the

modified with gap process, they are predominantly located in the low fall time region of the plot.

6.5 In-beam characterisation

6.5.1 Test beam setup

To evaluate the time resolution of the APTS-OA, in beam measurements have been performed at CERN-SPS H6 facility with a 120 GeV/c hadron beam. The test beam setup, a telescope made of nine planes, is illustrated in Fig. 6.27. The reference system is defined with the positive z-axis along the beam direction and with x- and y-axis defining the sensor planes. The telescope was composed by:

- **six ALPIDE planes** [39] operated at -3 V reverse substrate bias. Three planes are located upstream and three downstream, allowing track reconstruction.
- an **APTS-OA as DUT**, placed on xy moving stages to align it with micrometric precision.
- an **APTS-SF** [138] in a modified process and $15\text{ }\mu\text{m}$ pitch, as trigger plane for efficiency evaluation. Only the central 4 pixels of the APTS-SF were activated for the self-trigger, as they guarantee a trigger surface large enough to cover most of the APTS-OA DUT area and, in particular, the oscilloscope readout pixels that are relevant for the time information. The APTS-SF was operated with a -1.2 V reverse bias and all other biases at the optimal operating point, based on Ref. [138].
- a **LGAD** (produced by Fondazione Bruno Kessler) [94] as time reference, with an active area of 1 mm^2 and $25\text{ }\mu\text{m}$ active thickness, operated at -110 V bias voltage⁵ provided to the sensor bulk. The signal is amplified with an external circuit and readout with one oscilloscope channel.

A photo of the telescope inside the box is shown in Fig. 6.28 (left). A plastic scintillator detector equipped with a PMT, not depicted in the figure, was used to align the telescope to the beam. The APTS-OA data acquisition system employed

⁵the gain of the LGAD for this bias voltage is 17.

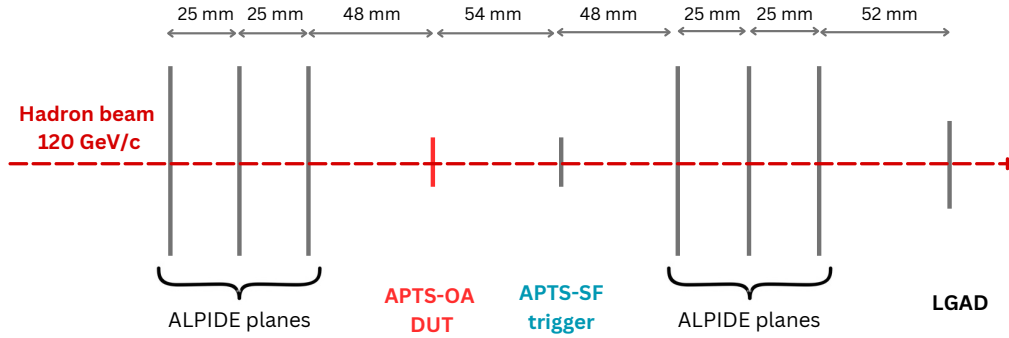


Fig. 6.27 Schematical representation of the telescope setup during test beam.

in the test beam is the same reported in Fig. 6.5. During the measurements 3 out of 4 central pixels have been read out with the oscilloscope, while the 12 external pixels plus one of the inner are read out via ADCs on the proximity board with a fixed sampling rate of 4 MHz.

6.5.2 Telescope physical alignment

To align the full telescope, a challenging step by step approach was followed:

1. Rough alignment of the box with respect to the beam:

for this first step a laser was employed, first placing it on the ground by following the beam line ⁶ and adjusting the horizontal position of the table on which the box was placed (see Fig. 6.28 (right)) and then placing the laser on a similar height to the beam and adjusting the vertical position of the table. For this first step the beam was off.

2. Check the beam profile on the ALPIDE planes:

this is pursued by switching on the beam and triggering on PMT, adjusting the table's position with greater precision compared to the previous step, in order to have the beam profile centered on the ALPIDEs (see Fig. 6.29a).

3. LGAD alignment:

trigger was changed to the oscilloscope channel where the LGAD was connected. The trigger surface was $1 \times 1 \text{ mm}^2$ and the tracks were observed on

⁶reference markers were already placed in the beam area.

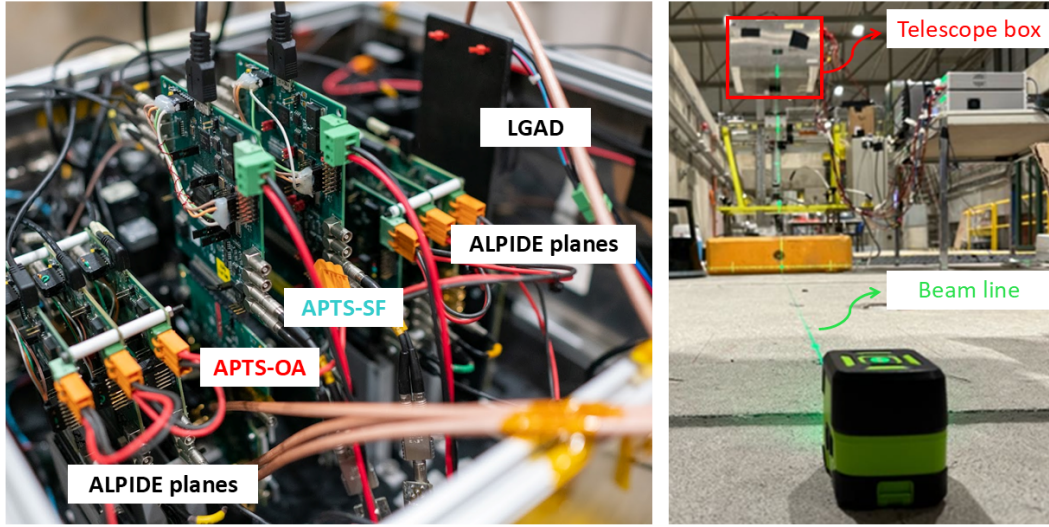


Fig. 6.28 Photo of the telescope inside the box (left) and adjustment of the telescope box in the horizontal direction with respect to the beam line through the laser spot (right).

the closest upstream ALPIDE plane with respect to the LGAD to be sure the LGAD was centered in the beam profile. Fig. 6.29b shows the halo of the LGAD on the six ALPIDE planes.

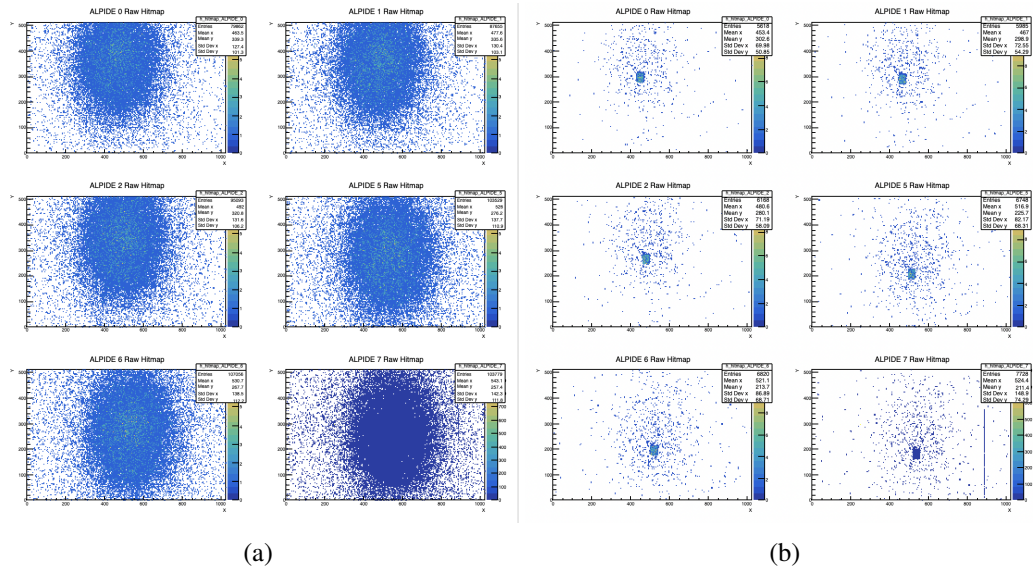


Fig. 6.29 Beam profile on the six ALPIDE planes obtained by triggering on the PMT (left). Track intercepts on the ALPIDE planes when triggering on the LGAD.

4. APTS-OA alignment:

the trigger logic was changed to trigger on the full APTS-OA matrix and to

see the projection of tracks on one ALPIDE plane. From Fig. 6.30 (center) it's possible to observe the superimposition of the LGAD and APTS-OA profile, allowing to see the position of the DUT with respect to the LGAD and check their alignment.

5. APTS-SF alignment:

switching the trigger to the four central pixels of the APTS-SF (area of $900 \mu\text{m}^2$), this plane was aligned until it was well overlapped to the APTS-OA (see Fig. 6.30 (right)).

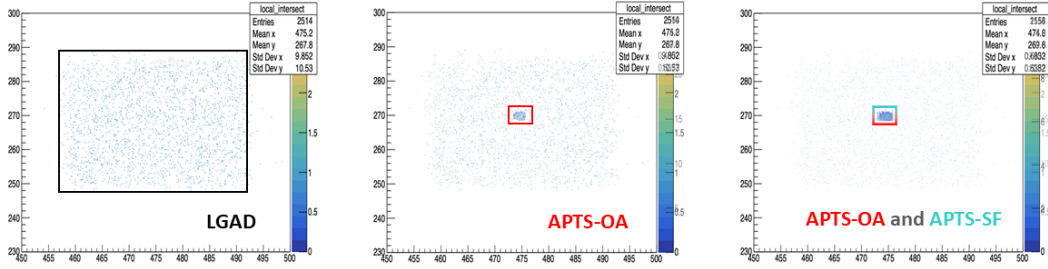


Fig. 6.30 Superimposed track intercepts on ALPIDE plane with trigger on LGAD (left), APTS-OA on LGAD (center) and APTS-SF plus APTS-OA on LGAD (right).

6.5.3 Data acquisition, conversion and processing

Once a proper alignment was achieved, stable data acquisition was started and synchronization among all the planes of the telescope was ensured through a trigger and busy chain. The data acquisition framework EUDAQ2 [147] has been employed to collect the test beam data, both for the ALPIDE planes, featuring a digital readout and for APTS, with analogue output signals. Two different pixel layouts have been characterized in the test beam: the modified and the modified with gap with V_{sub} ranging from -1.2 V to -4.8 V with steps of 1.2 V , in order to appreciate the effect of the progressive sensor depletion with the reverse bias. The operating points used during data acquisition are reported in App. D.11. The raw number of triggers acquired in each configuration is reported in Table 6.4.

The full signal waveforms read out with both the oscilloscope and ADC have been recorded, converted and analysed.

V_{sub}	Modified with gap	Modified
−1.2 V	290,000	15,000
−2.4 V	334,050	15,000
−3.6 V	15,000	20,000
−4.8 V	258,600	58,100

Table 6.4 Number of raw events collected in each configuration.

DUT data conversion and signal calibration

Signals were acquired via EUDAQ and had to be converted into a suitable format for executing the subsequent tracking analysis with the Corryvreckan framework [148]. In particular, data are stored in a native binary format, containing the raw data as they are read out by the various *data producers*. Each hardware that produces data has a specific *data producer* that has to initialise, configure, stop and start the hardware by receiving particular commands. APTS data are stored in EUDAQ *blocks* from which they are unpacked and converted in unit of electrons. This is achieved inside

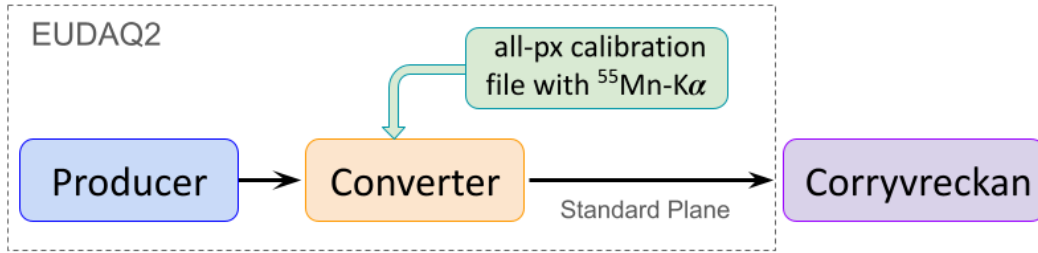


Fig. 6.31 General workflow to decode the acquired data.

the *data converter*, representing a bridge between EUDAQ and Corryvreckan and specifically developed for each detector type. Decoded pixel data are stored in an array of *StandardPlanes*, each representing one sensor plane of the telescope. Exploiting a calibration file, each *StandardPlane* contains the collected charge values from all the pixels of each sensor.

For APTS, this required a two-step process, in which signals were first converted from the binary format in which they were stored in EUDAQ into mV and then into a charge, expressed in electron units. For the specific case of the APTS-OA, since two different acquisition systems were employed, oscilloscope and ADC, two different decoding algorithms were applied. The general workflow is schematically shown in Fig. 6.31.

1. From binary format to mV

Oscilloscope

Each waveform contains 40000 data points ⁷ and they were converted first into int8 numbers and subsequently into mV, keeping in mind that the employed oscilloscope features 8 bits vertical resolution. This is the resolution of the ADC used to digitize the incoming signal that determines the number of discrete values that the oscilloscope can use to represent the amplitude of an input signal. The conversion factor from discrete units to mV has been computed as:

$$F_{\text{scope}} = \frac{20 \left(\frac{\text{mV}}{\text{div}} \right) \times 8 \text{div}}{256} = 0.625 \text{ mV/ADC} \quad (6.3)$$

being $2^8 = 256$ the total number of available discrete levels. The converted signal associated to the pixel j , readout via oscilloscope is hence computed as:

$$V_j = V_{j,\text{raw}} \times F_{\text{scope}}$$

ADC

The same approach was followed to decode the ADC readout pixels, with the conversion factor

$$F_{\text{ADC}} = \frac{2.5 \text{ V}}{2^{16}} = 38.1 \text{ } \mu\text{V/ADC}. \quad (6.4)$$

where 2.5 V is the internal reference voltage for the 16 bits ADC.

In conclusion, the signal associated to the pixel j , readout via ADC, is simply given by: $V_j = V_{j,\text{raw}} \times F_{\text{ADC}}$.

2. From mV to charge

In order to merge the results obtained from different pixels and different readout systems, a pixel by pixel calibration has been performed exploiting the acquisitions with the ^{55}Fe source, presented in 6.4.1. The mean of the $^{55}\text{Mn} - K_{\alpha}$ peak is then used to perform the conversion in electrons, using the same calibration method explained in Sec. 6.4.1. In conclusion, the following

⁷The oscilloscope acquisition window was 1 μs with a sampling period of 25 ps.

charge was associated to the pixel j :

$$Q_j = \frac{V_j \times Q_{\text{Mn-K}\alpha}}{V_{\text{Mn-K}\alpha,j}} \quad (6.5)$$

where V_j is the measured signal amplitude already converted in mV, as explained in the previous step, $Q_{\text{Mn-K}\alpha}$ is the charge generated by the $^{55}\text{Mn-K}\alpha$ photon ($\approx 1640 e^-$) and $V_{\text{Mn-K}\alpha,j}$ is the mean of the fit to the $^{55}\text{Mn-K}\alpha$ peak in the signal amplitude distribution for the specific pixel j .

Oscilloscope waveforms processing

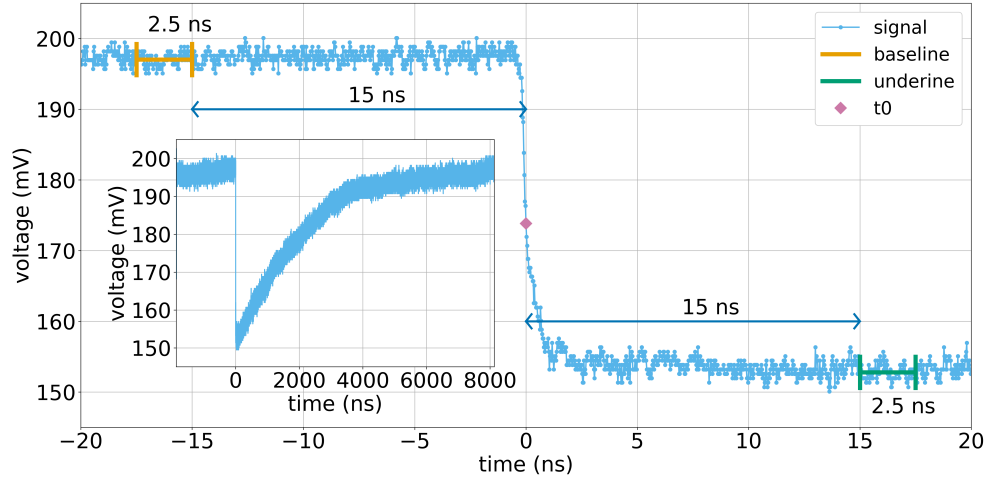


Fig. 6.32 Signal acquired with the oscilloscope with highlighted baseline, underline, t_0 and shift intervals of 15 ns before and after t_0 . The same signal is also shown in the box with a larger time scale, in order to appreciate the signal return to the baseline.

A typical signal recorded with the oscilloscope is shown in Fig. 6.32, where the relevant parameters have been highlighted. In particular, the following definitions have been employed in the analysis:

- the time zero (t_0), used to discriminate a signal, has been defined as the minimum of the signal's derivative [149];
- the baseline has been computed averaging 100 points, corresponding to a time interval of 2.5 ns, moving backwards of 15 ns from the t_0 ;

- the underline is defined, in a similar way, averaging 100 points after a delay of 15 ns from the t_0 ;
- the amplitude is given by the difference between the baseline and the underline.

ADC signals processing

For the external pixels and one of the 4 central ones, read out via DAQ board, the signal amplitude is computed as the difference between the baseline and the underline, the former defined as the signal value in correspondence of a fixed frame and the latter as the minimum itself, following the definition adopted in Ref. [138]. The reconstruction and analysis of data collected in test beam measurements is an elaborate multistage procedure, where two building blocks are the reconstruction and the analysis. In the following sections, the different steps that compose the reconstruction and analysis workflow will be introduced.

6.5.4 Data reconstruction

To reconstruct test beam data, the Corryvreckan framework [148] was employed. It is a modular tool based on several configuration files and an event loop, in which the different modules are sequentially executed. A schematic diagram of the general approach followed in the reconstruction phase is illustrated in Fig. 6.33.

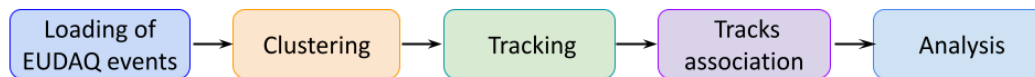


Fig. 6.33 Flowchart of the data reconstruction phase.

After the data, recorded by EUDAQ2 in a raw format, are read by Corryvreckan through a specific *converter*, as explained in 6.5.3, they are sorted into *events*, each one containing data from all the telescope planes. The proper allocation of data from all the detectors to the proper event is handled by EUDAQ2 and the Trigger Logic Unit (TLU) that was used during data taking to guarantee the correct synchronisation between the planes.

Clustering

Neighbouring pixel signals are joined to form a cluster. A clustering threshold of $100 e^-$ was applied to the DUT during the reconstruction phase to emulate the effect of a discriminator. Adjacent pixels with signal above such threshold are grouped into clusters and the threshold was chosen to be at least 4 times the RMS of the noise for all the working conditions, as it will be shown in 6.5.7. The position of a cluster on a plane is determined, for the DUT, as the charge weighted center-of-gravity, by considering the collected charge from all the pixels that make up the cluster.

Cluster position reconstruction

The spatial resolution evaluation benefits from the fully recorded analogue waveform and, in particular, from the precise signal amplitude estimation. The general procedure to estimate the DUT spatial resolution is to compute, for each track, the residuals Δx :

$$\Delta x = x_{\text{cluster}} - x_{\text{track}}. \quad (6.6)$$

To determine the position of the cluster, several *position finding algorithms* (PFA) exist, the more important and well known are:

- **Digital PFA**

It's the simplest algorithm since the cluster position is given by the position of the seed pixel in the cluster. In this case, the standard deviation of the residual distribution will be given by:

$$\sigma_{\text{DIG}} = \frac{\text{pixel pitch}}{\sqrt{12}} \quad (6.7)$$

- **Center of gravity (COG) PFA.**

It's based on the simple charge weighted mean position, obtained as expressed by the following equation:

$$x_{\text{cluster}} = \frac{\sum_i x_i Q_i}{\sum_i Q_i} \quad (6.8)$$

where x_i are the positions and Q_i the collected charges of each pixel in the cluster. However, this is not always expected to reproduce accurately the track position.

- **Non linear η PFA**

In the analysis presented in this work, the so-called η -algorithm [150, 151] has been applied to correct for the non-linear charge-sharing mechanism among the pixels. More details about the method will be provided in Sec. 6.5.9.

Track reconstruction

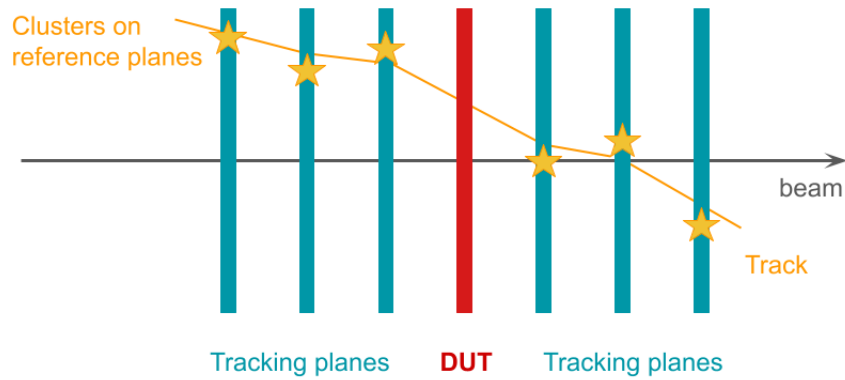


Fig. 6.34 Simple visualisation of the tracking algorithm on the reference planes, excluding the DUT. The stars represent the computed clusters' positions on the planes, while the yellow lines are the tracks between the planes.

The tracking is performed on six ALPIDE planes plus the trigger plane (APTS-SF), while the DUT has been excluded in order to obtain unbiased results.

For each event, particle tracks are reconstructed using the General Broken Line (GBL) [152] model to fit the cluster positions measured on the tracking planes, taking into account the multiple scattering⁸, mainly due to Coulomb interactions with the electrons in the atoms, leading to random changes in the particle direction with respect to the initial one and depending on the traversed material and the particle momentum. This chosen track fitting model allows therefore the tracks to change direction at the layers and kink angles to arise when crossing the detector planes. A

⁸The material budget of the sensor layers has to be defined in the first geometry file employed in Corryvreckan, in fraction of the radiation length (for silicon 21.82 g/cm² [145]). A value of 0.0005 was used in this work, corresponding to $\approx 50 \mu\text{m}$ of silicon.

simple visualisation of the tracking concept is shown in Fig. 6.34, where the tracking is performed only on the reference planes.

The track impinging angles have been evaluated by using the common *straight-line* track fitting method and including also the DUT in the tracking in order to retrieve the angle information on the DUT plane itself. Straight line tracks represent the simplest tracking algorithm and are accurate enough when multiple scattering can be neglected. Fig. 6.35 shows the track angle distributions with respect to the X/Y axis. By looking at the mean value and converting it in degree, one obtains $\langle\alpha_x\rangle = -0.0008$ deg and $\langle\alpha_y\rangle = 0.0004$ deg. Since in both directions the incident angles are lower than 0.001 degree, tracks can be considered always perpendicular to the DUT surface, as expected from the high beam momentum.

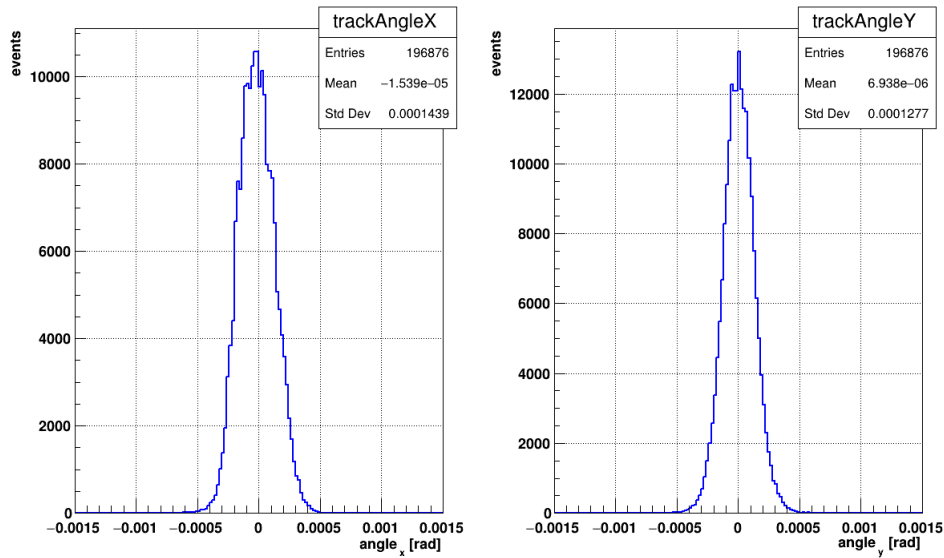


Fig. 6.35 Track angle distributions with respect to the x (left) and y (right) axis. Data collected on the modified with gap DUT at $V_{\text{sub}} -4.8\text{V}$. Applied clustering threshold of $100 e^-$.

Tracks association

The obtained tracks from the reference planes are interpolated to the position of the DUT. Tracks are associated to clusters if they impinge inside a user-defined association window, representing the maximum acceptable distance between the

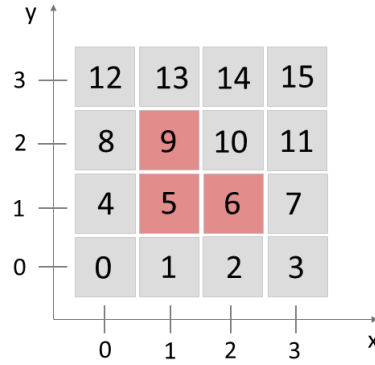


Fig. 6.36 Local coordinate system applied in Corryvreckan for every telescope plane and displayed here for the APTS-OA plane. Red pixels are the one readout via oscilloscope.

track intercept and the cluster position. This represents a paramount setting that has been carefully chosen, as it will be described in 6.5.8.

6.5.5 Telescope and DUT alignment

Software alignment of the different telescope planes is a crucial phase as it ensures a high quality of the tracks and a correct association between tracks and clusters. In particular, software alignment follows subsequent steps in which the different planes are shifted and rotated with respect to a chosen reference⁹ plane to increase the tracking quality [148]. Two different coordinate systems are provided: a global one, already explained in Sec. 6.5.1 and a local one for each sensor plane. This latter is a right-handed Cartesian system with the x and y axes defining the sensor plane and the origin placed in the center of the lower left pixel in the matrix (Fig. 6.36) The starting point is a geometry configuration file defining the detectors involved in the setup and their z position along the beam direction. Software alignment is not performed in z direction and is measured manually with an accuracy of ≈ 1 mm. The distances between the planes are shown in Fig. 6.27. In order to determine the precise x/y plane positions, a total of 8 alignment steps were executed in Corryvreckan:

1. Prealignment

The prealignment is performed on both the telescope and the DUT and it represents a starting point to help the subsequent alignment steps. In this

⁹when a detector has the "reference" role, it acts like an anchor for relative alignments and its position and orientation are used as comparison with the other telescope planes.

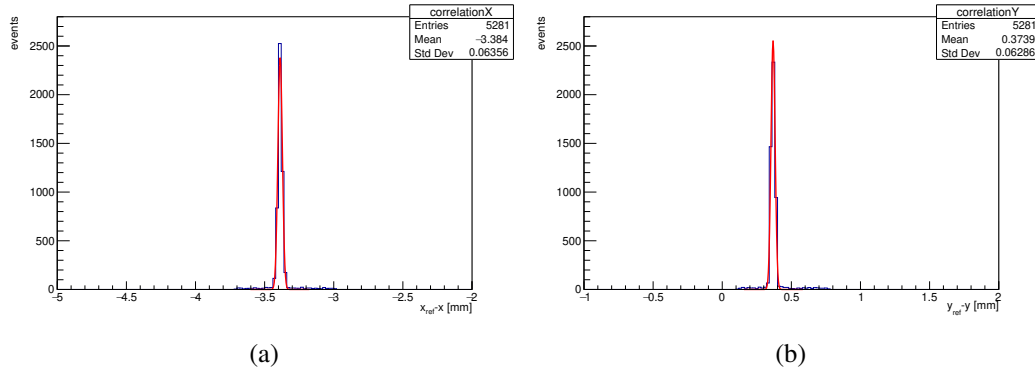


Fig. 6.37 Example of correlation histograms between the APTS-SF trigger plane and the ALPIDE reference plane during the prealignment phase.

module, the planes are aligned via x and y translational shifts determined by the mean of a Gaussian fit on 1D correlation histograms between each plane and the reference one. Example of correlation histograms are shown in Fig. 6.37a and 6.37b.

2. Telescope alignment

In this phase an alignment of the whole telescope but the DUT is performed, in which translation on the x-y plane and rotation with respect to the z-axis are allowed.

3. Trigger plane alignment

The APTS-SF used as trigger plane required a dedicated alignment procedure, in which it was considered as DUT and aligned through three iterations. In particular, it underwent translational and rotational alignment with respect to the usual ALPIDE reference plane and was aligned using tracks, through a minimisation of the unbiased residuals computed from the track intercept on this particular plane. In the three iterations the *spatial cut*, representing the maximum distance between cluster and track to allow for the association, was progressively reduced from a value ~ 4 pixel pitch down to the pixel pitch itself.

4. DUT alignment

The same three-steps procedure described above for the APTS-SF was performed for the APTS-OA DUT.

After the alignment was successfully completed, the analysis was performed, based on the criteria listed in Sec. 6.5.6.

6.5.6 Analysis strategy

To guarantee a clean data sample, the following selection criteria have been applied:

- a cluster is required on each tracking plane;
- only tracks with $\chi^2/\text{dof} < 5$, where dof stands for the number of degrees of freedom, have been considered¹⁰;
- only events with a single reconstructed track are selected, where an event has to be intended as a trigger provided by the APTS-SF (see Fig. 6.27);
- a Region Of Interest (ROI) is applied to select only the associated tracks crossing one of the three central pixels read out via the oscilloscope (pixels 5, 6 and 9 colored in red in Fig. 6.36), in order to avoid border effects.

With the above-mentioned selections, the number of reconstructed tracks associated with the DUT and used for the analysis discussed in the following are about 20% of the total acquired statistics reported in Table 6.4, for each configuration. In the next sections the main results will be presented.

6.5.7 Noise and SNR evaluation

A relevant quantity that needs to be evaluated is the chip noise, in order to select the proper clusterisation threshold to be applied in the analysis. For this purpose, an analysis of the single point noise was conducted and the noise distributions are reported in Fig. D.14 of App. D.9 and summarised in Fig. 6.38a. As a consequence, all the results shown in the following plots have been obtained by applying a clusterisation thresholds above 3 times the noise RMS, in order not to be biased by noise. To compute the SNR, the cluster charge distributions for the data samples with the highest statistics ($V_{\text{sub}} = V_{\text{pwell}} = -1.2, -2.4$ and -4.8 V) were fitted with a Landau-Gauss function in Fig. 6.39. The most probable values were used to calculate the SNR for the oscilloscope readout pixels, shown in Fig. 6.38b.

¹⁰Each track features a χ^2 defining the quality of the fitted trajectory.

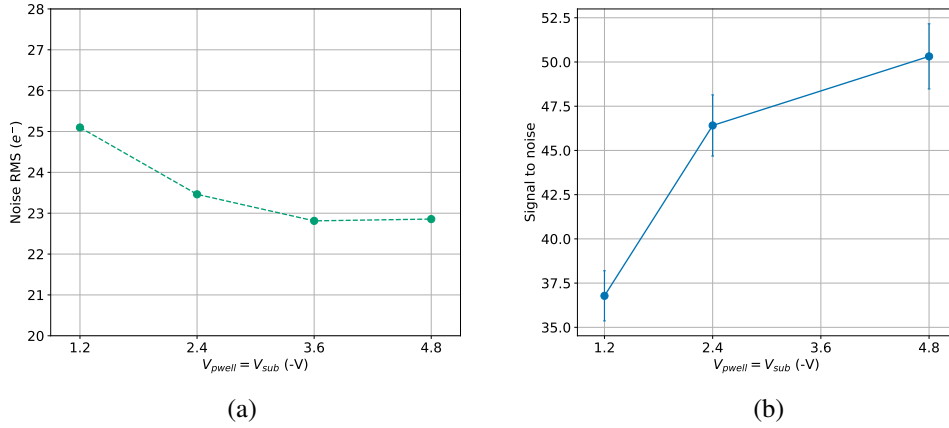


Fig. 6.38 Noise RMS computed on the APTS-OA matrix as a function of V_{sub} values (left). SNR as a function of V_{sub} values obtained on the oscilloscope readout pixels (right). Errors are statistical only. Image source [139].

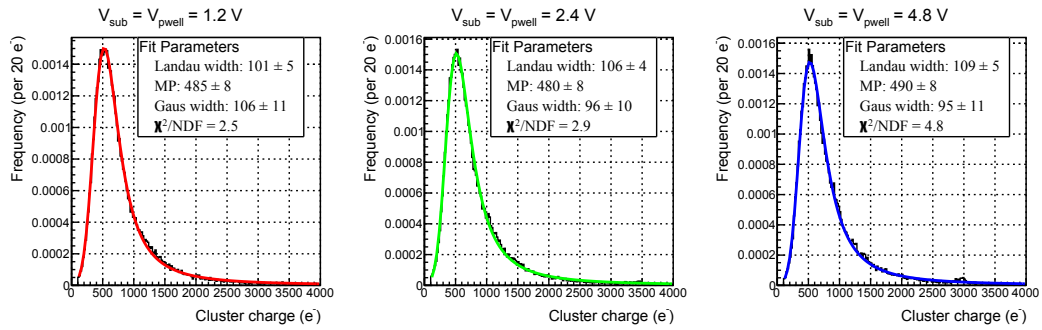


Fig. 6.39 Cluster charge distributions for data samples with the highest statistics ($V_{\text{sub}} = V_{\text{pwell}} = -1.2, -2.4$ and -4.8 V) with a Landau-Gauss fit. Only clusters associated to tracks are displayed and after the implementation of the analysis criteria described in 6.5.6. Data collected on the modified with gap process and with an applied clusterisation threshold of $100 e^-$.

6.5.8 Detection efficiency

The detection efficiency is computed as the ratio between the number of tracks providing an associated cluster in the DUT and the total number of tracks crossing the DUT ROI. The applied ROI includes only pixels 5, 6 and 9 shown in Fig. 6.36, in order to consistently quote the detection efficiency on the same three pixels for which the timing analysis is performed.

A crucial parameter to be defined for the efficiency analysis is the *association window*. A study was performed to select the proper association window radius and, as can

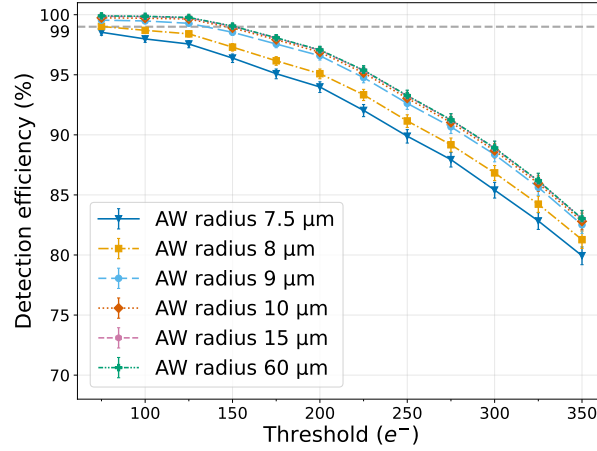


Fig. 6.40 Efficiency as a function of the threshold for a modified DUT at $V_{\text{sub}} = V_{\text{pwell}} = -1.2$ V, varying the association window (AW) radius. Image source [139].

be seen from Fig. 6.40, the detection efficiency increases as the association window is enlarged, since the number of associated tracks is getting bigger. However, no further changes are observed when increasing this parameter from $15 \mu\text{m}$ to $60 \mu\text{m}$ (the difference in efficiency between the aforementioned $15 \mu\text{m}$ and $60 \mu\text{m}$ radii is less than 0.05%) and therefore a choice of $15 \mu\text{m}$ would not have underestimated the efficiency.

For this reason, a $15 \mu\text{m}$ association radius was applied, meaning that to associate a cluster on the DUT to a track, this latter must impinge inside a circular area with a maximum radial distance of $15 \mu\text{m}$ from the cluster position.

Figure 6.41 shows the detection efficiency for the modified (left) and modified with gap (right) processes as a function of the clusterisation threshold, expressed in e^- charge, at different reverse bias voltages. The errors on the efficiency are statistical only ¹¹. As expected, a clear decreasing trend of the detection efficiency with the increasing threshold can be observed for both the modified and modified with gap processes. Moreover, for the modified with gap process, a dependence from the reverse substrate voltage V_{sub} can be noticed at high thresholds, where a higher V_{sub} translates into a higher detection efficiency. Both pixel processes feature an excellent detection efficiency higher than 99% up to a threshold of $150 e^-$, defining a wide operational window with the desired performance and the results are in agreement with [138]. Moreover, a high detection efficiency is a key requirement to

¹¹They have been computed using a Clopper-Pearson confidence interval of 1 sigma, corresponding to the central 68.3% of a binomial distribution [148].

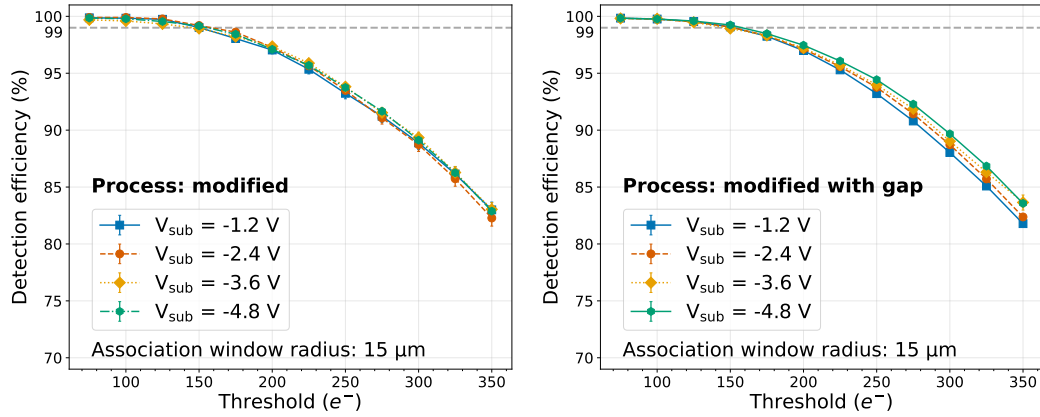


Fig. 6.41 Detection efficiency for the modified (left) and modified with gap (right) pixel processes as a function of the applied threshold and for different V_{sub} . The dashed line in both plots indicates the 99% detection efficiency. Image source [139].

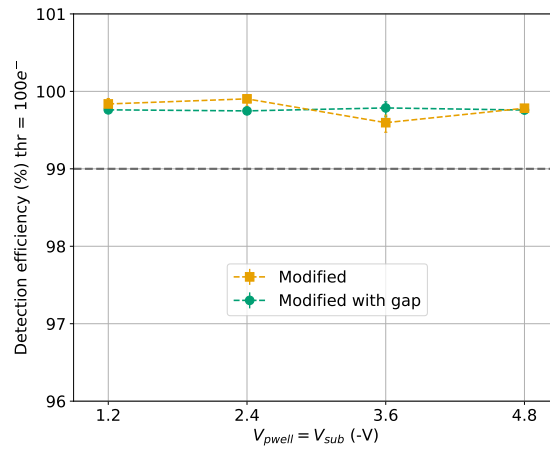


Fig. 6.42 Detection efficiency of the APTS-OA modified and modified with gap process at $100 e^-$ threshold at different $V_{sub} = V_{pwell}$ configurations. No significant difference can be spotted between the two pixel design variants. Image source [139].

avoid any bias in the time resolution measurement. Fig. 6.42 compares the detection efficiency of the two process variants at a threshold of $100 e^-$ and no significant differences can be found. No differences were observed enlarging the tracks selection ROI by adding an external crown of $5 \mu m$ (see Appendix D.15).

Thanks to the high statistics available, it was possible to perform an in-pixel efficiency study. Results obtained on the modified with gap process at $V_{sub} = 4.8 V$, are reported in Fig. 6.43 for $100 e^-$ threshold and Fig. 6.44 for $200 e^-$ threshold. The bin width was selected in order to reach a sufficient statistics in every bin (more than 2000

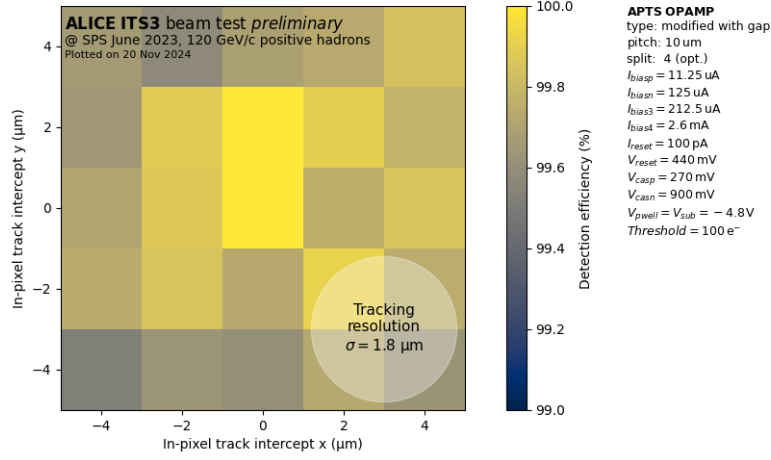


Fig. 6.43 In-pixel efficiency for the modified with gap pixel process at 100 e^- clustering threshold and $V_{sub} = -4.8 \text{ V}$.

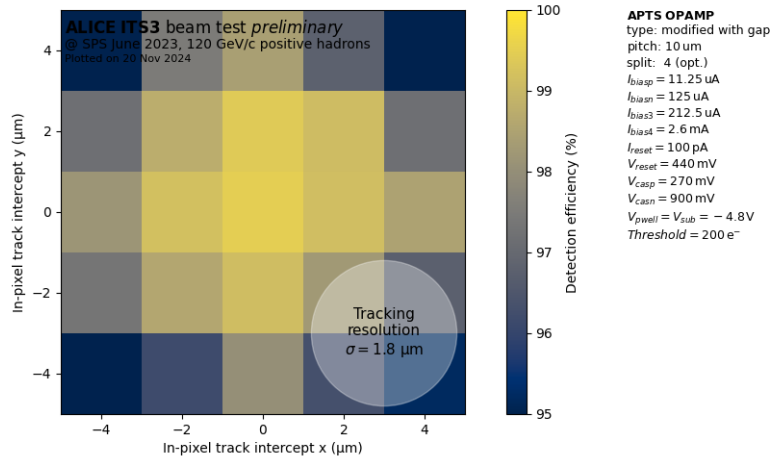


Fig. 6.44 In-pixel efficiency for the modified with gap pixel process at 200 e^- clustering threshold and $V_{sub} = -4.8 \text{ V}$.

events per bin are included in the following plots). Even though the color scales are different, it's worth noting that in the 100 e^- threshold case, an in-pixel detection efficiency higher than 99% is achieved in all the pixel area. If the threshold is increased up to 200 e^- , a decrease in the efficiency starts to become visible especially at the pixel edges and corners, where the probability of having events with cluster size larger than one is increased.

6.5.9 The η correction from telescope tracks

It's already well known that charge division for two pixel clusters is not linear [151]. Non-linear charge division results in a worse spatial resolution for two pixel clusters and the η -algorithm adopted in this work is a data-driven method for computing the cluster position which takes the non-linearities into account [138]. The adopted approach is implemented in Corryvreckan and compares the cluster position, computed with the COG algorithm (6.7), with the reconstructed track position from the telescope. In particular:

- the position of the track intercept is plotted against the weighted charge position of the associated cluster;
- the resulting profile is fitted with a N-order polynomial function; in this work, a third order polynomial function was chosen ¹² as displayed in Fig. 6.45 and the correction was computed for a clustering threshold of $75 e^-$ and for every V_{sub} separately.
- the determined η -correction functions f for x and y are applied to the clusters' positions by directly computing the corrected cluster position evaluating the function:

$$x_{\eta\text{-corrected}} = f(x_{\text{cluster}}) \quad (6.9)$$

The whole statistics was employed to compute the correction, since an improvement was observed in the stability of the fit parameters (see App. D.10). Fig. 6.46 (left) shows the cluster position on a local coordinate system where (0,0) is the center of the APTS-OA matrix and the color scale represents the events' frequency. The yellow small regions identify the cluster size 1 events, as the cluster position matches the pixel center and they are the more frequent events. Also events with cluster size 2 are visible, where the cluster position is in between two pixels and events with cluster size larger than two, recognisable in the events that make up the cloud-shaped populations. The track intercepts are displayed in Fig. 6.46 (center), where the applied ROI is well visible. Finally, the right plot depicts the difference between the cluster position and the track intercept for every events, resulting in a distribution centered around zero.

From the information of the track positions, it's possible to visualise the track

¹²as it is the lower order polynom that describes the trend.

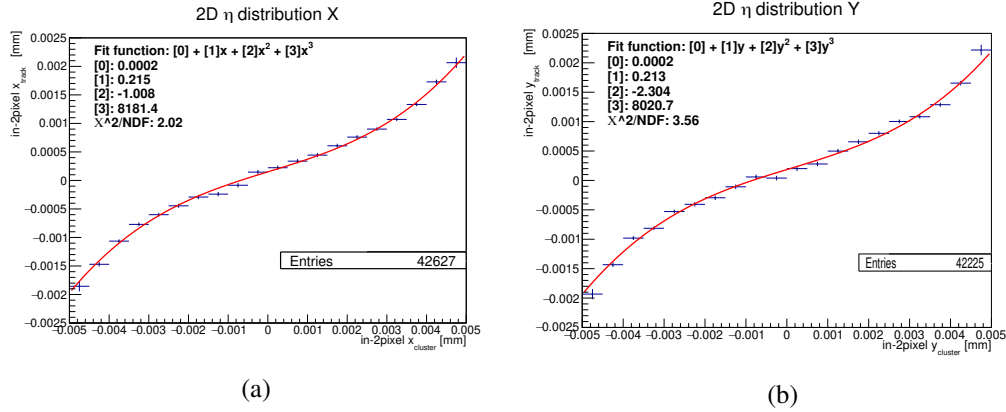


Fig. 6.45 TProfiles for x (left) and y (right) showing the track intercept position as a function of the cluster position with superimposed third order polynomial fit, providing the η -correction. Fit parameters are also displayed. Data from modified with gap DUT at $V_{\text{sub}} = -4.8$ V.

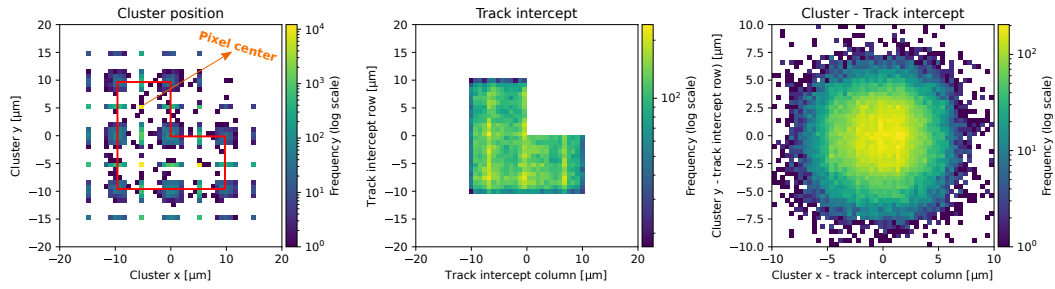


Fig. 6.46 Cluster position (left), associated tracks intercept with ROI applied (center) and difference between cluster and track position (right). Data on the AP10P at $V_{\text{sub}} -4.8$ V.

intercept on the DUT, selecting on the cluster size of the associated cluster. The three oscilloscope read out pixels are considered in Fig. 6.47, showing only events with cluster size 1 on the left plot, which are uniformly distributed across the three pixels area. On the other hand, tracks with associated cluster size 2 or 3, superimposed on Fig. 6.47 (right) are more localised in the proximity of the pixel boundaries, as expected. It's worth remarking that events with cluster size 1 represent the 64% of the total number of events, while cluster size 2 and 3 are only the 30 and 3% respectively. This effect can be justified by the high lateral electric field of the modified with gap process, leading to an increased probability of events with cluster size one.

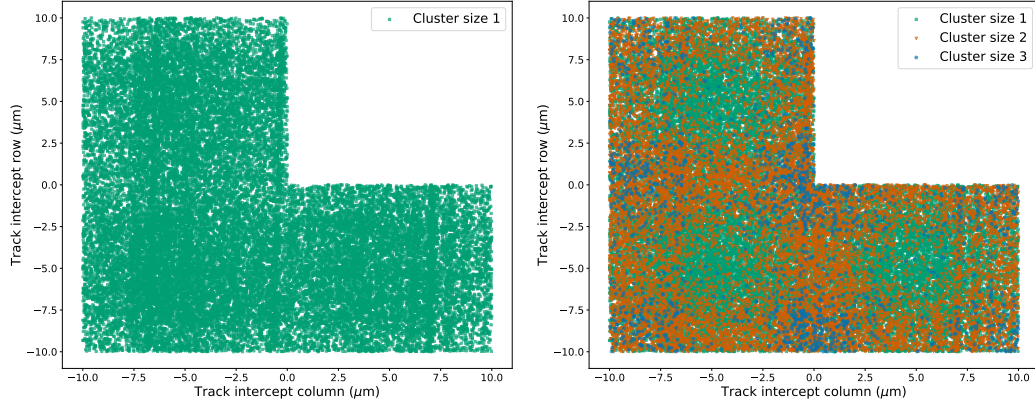


Fig. 6.47 Track intercept position on the DUT, selecting on the cluster size of the associated cluster. Only tracks crossing the three oscilloscope readout pixels have been considered, as they will be the ones employed for the estimation of the time resolution. Data from AO10P at $V_{sub} = -4.8$ V.

6.5.10 Spatial resolution and cluster size

In order to provide an exhaustive characterisation of the chip, spatial resolution and cluster size as a function of the applied threshold and for different applied V_{sub} are evaluated. Spatial resolution is derived from the unbiased¹³ spatial residuals distributions, obtained as in 6.6, after the η -algorithm was applied in both the x and y directions. The distributions of the modified with gap DUT at -4.8 V are reported in App. D.12, considering different clusterisation thresholds.

The spatial resolutions σ_x and σ_y in the x and y directions are computed by quadratically subtracting the estimated telescope tracking resolution $\sigma_{track} = (1.8 \pm 0.1) \mu m$ from the standard deviation of the residual distributions in the x and y direction, respectively. In formula:

$$\sigma_s = \sqrt{\sigma_{residuals}^2 - \sigma_{track}^2} \quad (6.10)$$

In the following, more details about the telescope pointing resolution estimation will be provided.

¹³The residuals are unbiased since the DUT was excluded from the tracking.

Tracking resolution estimation

The tracking resolution of the employed telescope has been computed following two different approaches:

- by using the telescope optimiser tool [153], a calculator where the GBL [152] model is employed, taking into account the multiple scattering in the telescope planes; as can be seen in App. D.14, the telescope optimizer tool provides 1.87 μm tracking resolution;
- by measuring it directly on the data, obtaining a valid cross check of the previous result. To this purpose, the following analysis was performed:
 - residual distributions were computed considering as cluster position and cluster signal only the seed pixel position of the cluster and the seed pixel signal, respectively;
 - no clustering threshold was set to avoid applying any selection on the signals.

In this way it was possible to retrieve the telescope tracking resolution considering the DUT with a purely binary readout, i.e the sensor resolution is given by the pixel pitch divided by $\sqrt{12}$. The tracking resolution can finally be estimated as:

$$\sigma_{\text{track}} = \sqrt{\sigma_{\text{residuals seed}}^2 - \left(\frac{10}{\sqrt{12}}\right)^2} \quad (6.11)$$

This study was performed on x and y separately and the residual distributions obtained on the modified DUT with the above mentioned approach and with different V_{sub} are reported in App. D.13. Fig. 6.48 shows the standard deviation as a function of V_{sub} , for x and y. In the end, the two tracking resolutions for x and y were found to be compatible within the errors, computed as the maximum semi-dispersion. Ultimately, the measured tracking resolution with this second method was $(1.8 \pm 0.1) \mu\text{m}$.

Since the tracking resolution obtained with the telescope optimiser tool was compatible with the measured one, a value of $\sigma_{\text{track}} = (1.8 \pm 0.1) \mu\text{m}$ was adopted in this work. The final position resolution is then defined as the arithmetic average between σ_x and σ_y and it will simply be referred to as spatial resolution. Indeed,

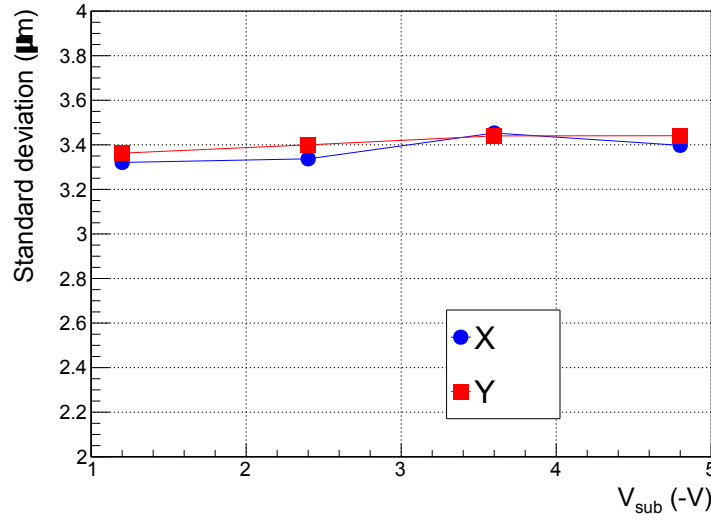


Fig. 6.48 Standard deviation of the residual distributions obtained for x (blue) and y (red) on the modified DUT by considering only the seed pixel of the cluster to define the cluster position and with a clustering threshold of $0 e^-$.

looking at the results in Fig. 6.49, obtained on the modified with gap DUT at $V_{\text{sub}} = -4.8 \text{ V}$, it's clear that the resolutions obtained on x and y are compatible within error bars. The effect of the η -correction can be observed on the spatial resolution

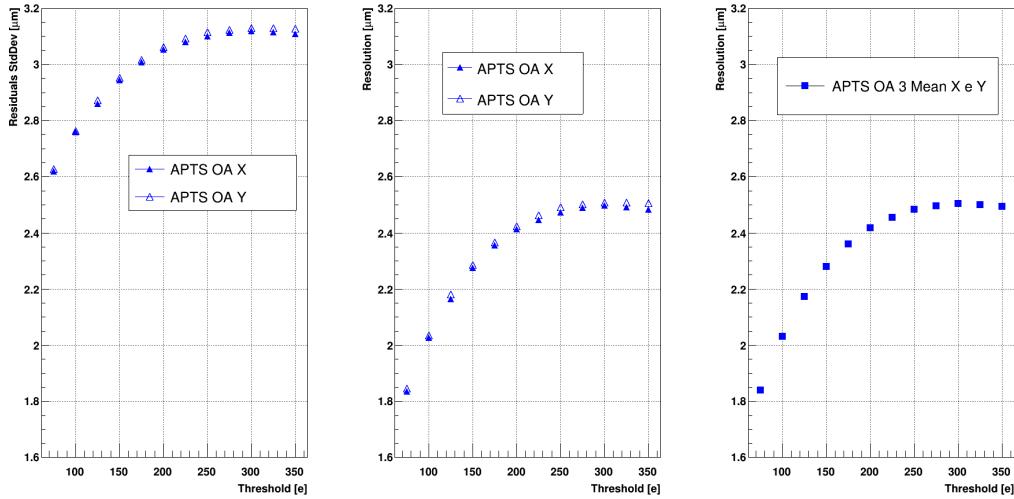


Fig. 6.49 Standard deviation of the residual distributions on x and y separately (left), spatial resolutions on x and y separately (center) and average of the two (right), obtained for the modified with gap DUT at $V_{\text{sub}} -4.8 \text{ V}$.

in Fig. 6.50, where its strong effect for low thresholds is apparent, while at high thresholds the effect is almost negligible, due to the majority of events with cluster size 1. Figure 6.51 shows the spatial resolution, on the left axis, and the average

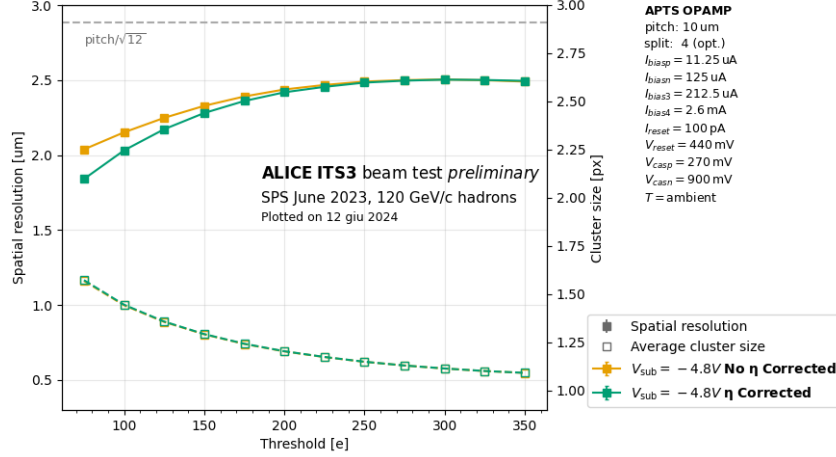


Fig. 6.50 Effect of the η -correction on the AO10P at $V_{\text{sub}} = -4.8\text{V}$

cluster size, on the right axis, as a function of the applied threshold. As for the efficiency, the threshold scan starts from $75 e^-$ for all the V_{sub} . The cluster size decreases with increasing threshold, as expected, degrading the spatial resolution since a less accurate determination of the cluster position can be obtained. The dashed gray line represents the spatial resolution that the chip would have in a case of a purely binary readout, i.e the pixel pitch divided by $\sqrt{12}$. As can be observed, the spatial resolution obtained with both the modified and the modified with gap processes, operated at different reverse bias voltages, is always lower than the pixel pitch divided by $\sqrt{12}$. Moreover, at low thresholds, it's possible to notice that for both the pixel variants the cluster size reduces with increasing reverse bias. This trend can be justified by the enhanced electric field, resulting in an increased probability of events with cluster size one. This V_{sub} dependence becomes undetectable for larger thresholds as the information from low amplitude signals is no more available. The errors on the spatial resolution has been computed as the quadratic sum of the uncertainty on the telescope tracking resolution and the error on the standard deviation of the residual distributions. The distributions shown in Fig. 6.52 for different V_{sub} values, help to visualise the cluster size reduction with increased reverse bias, as a consequence of the reduced charge sharing. They illustrate the cluster size distribution at $100 e^-$ threshold at different V_{sub} for the

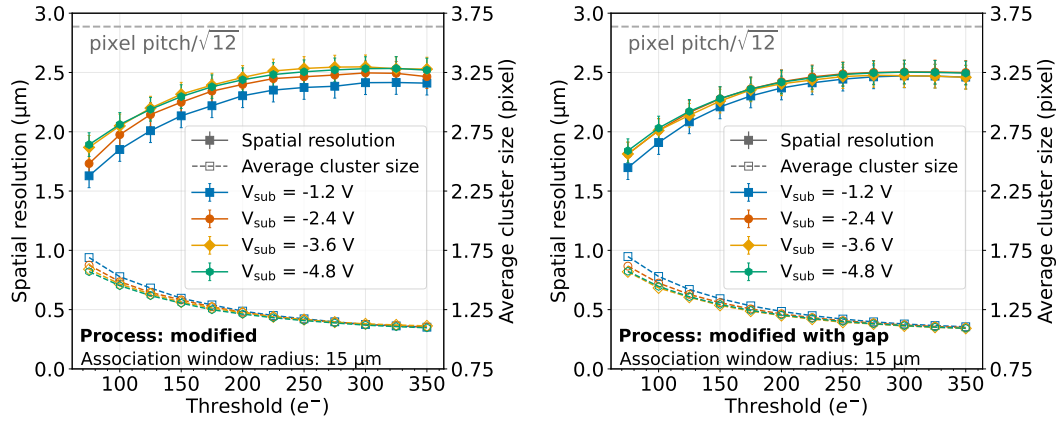


Fig. 6.51 Spatial resolution and cluster size as a function of the applied threshold for the modified (left) and modified with gap (right) structures, comparing different reverse substrate voltages in different colors. The grey dashed line represents the pixel pitch divided by $\sqrt{12}$. Image source [139].

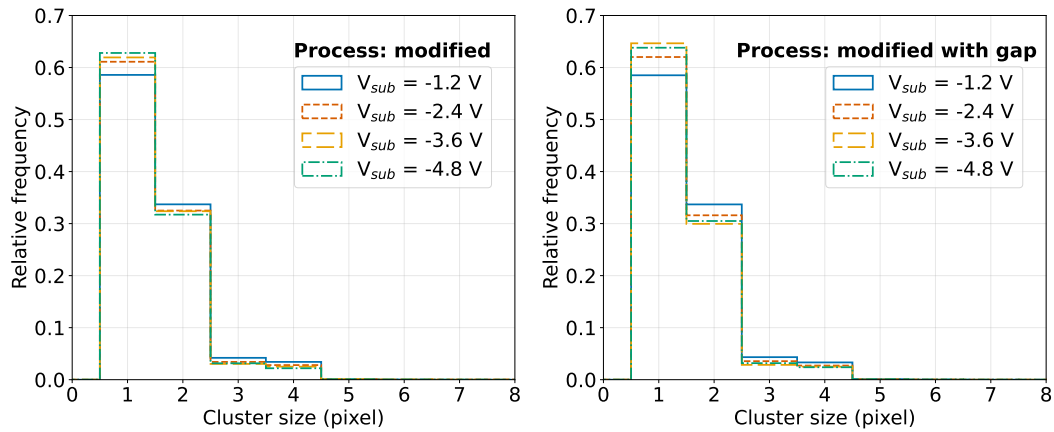


Fig. 6.52 Cluster size distribution of the APTS-OA modified and modified with gap DUT at $100 e^-$ threshold at different $V_{sub} = V_{pwell}$ configurations. Image source [139].

APTS-OA modified and modified with gap processes. Thanks to the high collected statistics, in-pixel studies can be performed. In particular, Fig. 6.53 shows the in-pixel cluster size for the AO10P at $V_{sub} = -4.8$ V at a threshold of $100 e^-$. As can be observed, the cluster size is always below 2, confirming the reduced charge sharing expected for this sensor. Appendix D.16 illustrates a comparison between the spatial resolution and cluster size of the APTS-OA and APTS-SF variants, both with a $10 \mu\text{m}$ pitch and a reverse bias $V_{sub} = -1.2$ V, showing an excellent agreement. In the following sections, the techniques employed to extract the time resolution of the APTS-OA prototype will be presented.

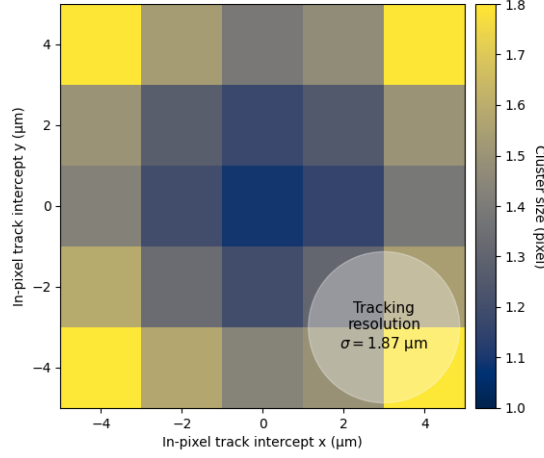


Fig. 6.53 In pixel cluster size obtained with a clustering threshold of $100 e^-$ for $V_{\text{sub}} -4.8\text{V}$.

6.5.11 Time resolution

The time resolution has been a key measurement of the test beam campaign, as it provides an estimation of the intrinsic timing performance of the sensors in this new technology. The APTS-OA time residuals have been computed as the difference between the time at which the APTS-OA DUT seed pixel signal reaches 10% of its amplitude and the time reference provided by the LGAD in the beam telescope (cf. Fig. 6.27). In particular, the reference time is defined as the time when the LGAD signal reaches the 40% of its amplitude. The threshold selection is based on the observation that, among the various amplitude fractions, the 10% level provided the most effective time walk compensation on the DUT. A similar strategy is applied to the LGAD signals [139].

The methodology of the constant fraction of the signal amplitude was chosen to mitigate time walk effects in the time resolution; the distribution of the time residuals is therefore defined as follows:

$$\Delta t = t_{10\%}^{\text{DUT}} - t_{40\%}^{\text{LGAD}} . \quad (6.12)$$

Since accurate timing information can be retrieved only from signals readout by the oscilloscope, only tracks associated to clusters having one of those 3 pixels as seed are used to determine the timing resolution. Quantitatively, around 85% of the events previously selected with tracking are used for the time resolution estimation, resulting in a number of available signals for the time resolution analysis equal to

17% of the number of recorded triggers reported in Tab. 6.4. The blue histogram of Fig. 6.54 shows the time residual distribution obtained on the modified with gap process at $V_{\text{sub}} = -4.8$ V. The LGAD time reference signals are delayed with respect to the DUT ones, because particles reached the LGAD after crossing the full telescope planes, resulting in negative time residuals (cf. Eq. 6.12). Finally, the LGAD time resolution $\sigma_{\text{LGAD}} = 30$ ps [154] is quadratically subtracted from the standard deviation of the time residuals to obtain the time resolution of the DUT σ_t :

$$\sigma_t = \sqrt{\sigma_{\Delta t}^2 - \sigma_{\text{LGAD}}^2} . \quad (6.13)$$

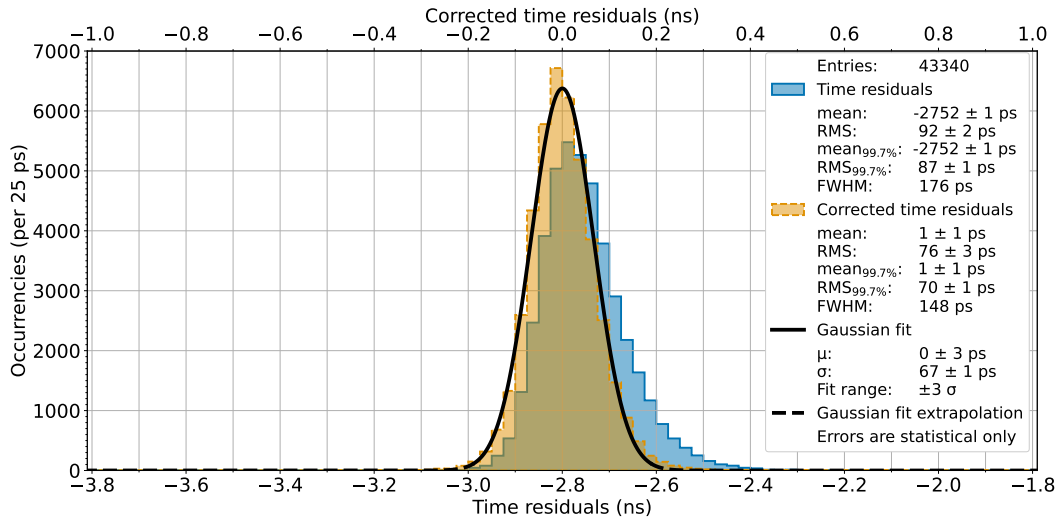


Fig. 6.54 Time residuals measured for the modified with gap process DUT operated at $V_{\text{sub}} = -4.8$ V, before (blue distribution, bottom horizontal axis) and after (orange distribution, top horizontal axis) time walk-like correction. The latter distribution is fitted with a Gaussian function on a range of $\pm 3\sigma$ (black solid line, dashed line for points outside the fit range). Image source [139].

Time-walk correction

Even though the employed analysis method aimed at reducing signal amplitude dependence of the measured signal times, a correction for residual time walk effect was needed. It can be explained by considering that no signal shaping is performed at chip level, therefore the measured waveforms differ in shape depending on the

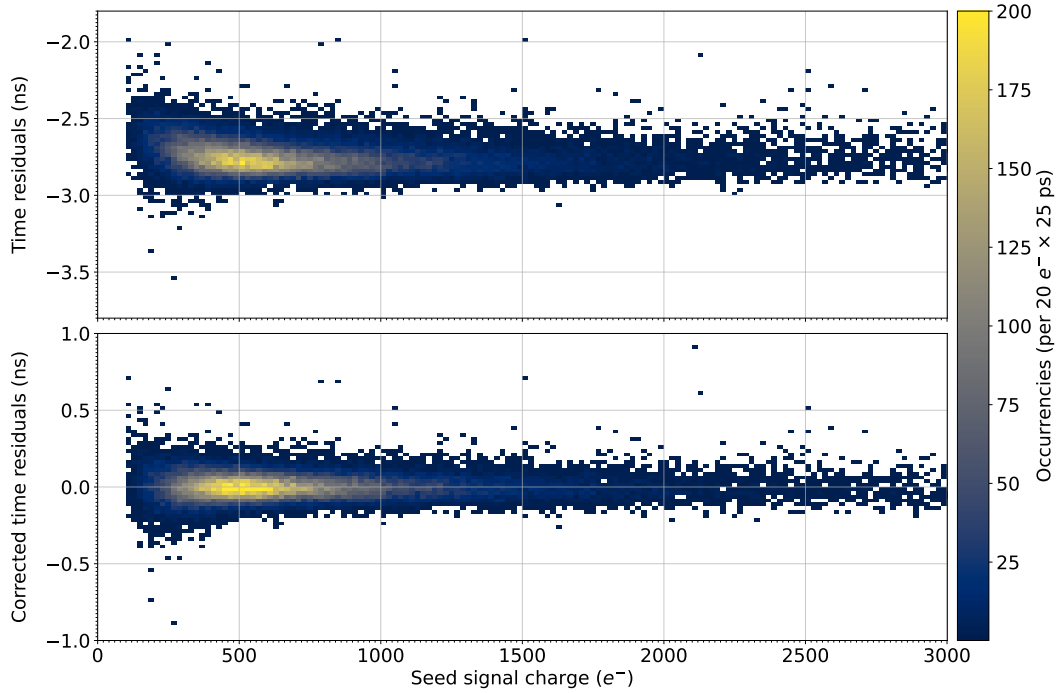


Fig. 6.55 Time residuals versus seed signal charge with no correction applied (top) and after the correction (bottom) for the DUT featuring modified with gap process operated at $V_{\text{sub}} = -4.8$ V. Image source [139].

collected charge and the in-pixel track hit position. Figure 6.55 (top) shows the dependence of the time residuals on the APTS-OA seed signal. In order to correct such dependence and restore the symmetry in the time resolution, a clustering threshold of $100 e^-$ was applied and the data divided in two groups: the first one including only single pixel clusters and the second involving events with cluster sizes larger than one. Each subset is further divided in two halves. For each dataset, the correlation between time residuals and seed pixel charge is represented with a 2D histogram and the average time residuals of each signal charge bin are interpolated with a quadratic function. To avoid introducing any bias, the time residuals of one half are corrected by using the function obtained from the other half, and vice versa. Figure 6.55 (bottom) shows the time residuals as a function of seed pixel charge after the correction discussed above. As expected, the dependence of the time residuals on the seed signal charge is mitigated and a symmetric shape is restored. Three estimators for the time residual distribution width have been computed and are reported in Fig. 6.54:

- the RMS of the entire data set;

- the RMS evaluated on the central 99.7 percentiles of the distribution;
- the standard deviation σ of a Gaussian fit within a 3σ interval for the corrected data sample.

The RMS of the corrected distribution (orange histogram) is $76 \text{ ps} \pm 3 \text{ ps}$ and is higher than the $\sigma = 67 \text{ ps} \pm 1 \text{ ps}$ of the Gaussian fit.

The fit is comparable with the $\text{RMS}_{99.7\%} = 70 \text{ ps} \pm 1 \text{ ps}$ and all the reported uncertainties are statistical only. Finally, the time resolution of the APTS-OA is calculated according to Eq. 6.13 by considering $\text{RMS}_{99.7\%}$ as the width of the time residual distribution. Since the time-walk correction needs a larger statistics to be effective, only the data taken with the modified with gap structure operated at $V_{\text{sub}} = -1.2$, -2.4 and -4.8 V have been corrected.

Time resolution dependence on the reverse bias

The dependence of the time resolution on the reverse substrate bias voltage V_{sub} , for both modified and modified with gap sensors, is shown in Fig. 6.56. For the data sets

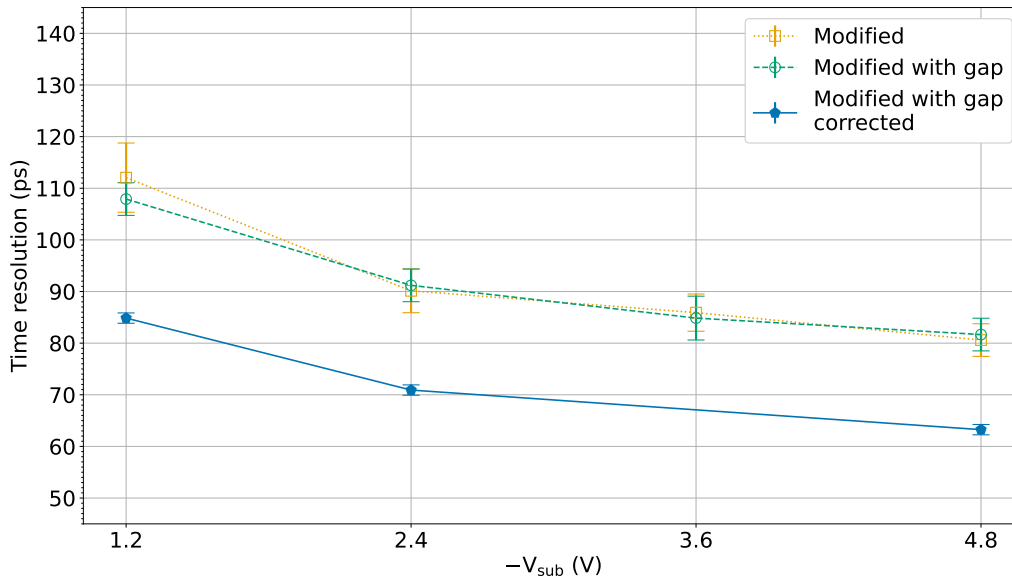


Fig. 6.56 Non-corrected (open symbols, orange dotted line and green dashed line) and corrected (full symbols, blue solid line) time resolution measured for modified and modified with gap DUT processes. A time walk-like correction is applied only to high statistical significance data sets, namely those measured with the modified with gap structure. Image source [139].

with larger statistics, the time resolution after time walk-like correction is also shown. While no substantial difference between the modified and modified with gap sensor processes can be spotted, an improvement in timing performance with increasing reverse bias is observed. In particular, a time resolution $\sigma_t = 63 \text{ ps} \pm 3 \text{ ps}$ and $\sigma_t = 82 \text{ ps} \pm 3 \text{ ps}$ at $V_{\text{sub}} = -4.8 \text{ V}$ for corrected and not corrected data, respectively.

In-pixel time resolution

Exploiting again the track positions information, the uniformity of the timing performance across the pixel surface can be investigated. In particular, this can be pursued through a correlation map of the time resolution with the in-pixel track position. Figure 6.57 shows the map of corrected time resolution of the modified with gap DUT operated at $V_{\text{sub}} = -4.8 \text{ V}$, considering all the hits from all the pixels folded into one pixel area and grouped per associated track position. As can be seen, the lowest time resolution $\sigma_t = 52 \text{ ps} \pm 4 \text{ ps}$ is measured for tracks impinging in the pixel center (position A), where the distance to the collection electrode is minimal and the electric field is maximum, while it deteriorates for tracks crossing the pixel edge ($\sigma_t = 58 \text{ ps} \pm 4 \text{ ps}$) and corner ($\sigma_t = 72 \text{ ps} \pm 4 \text{ ps}$), marked by the points B and C of Fig. 6.57, respectively. The reported uncertainties are statistical only.

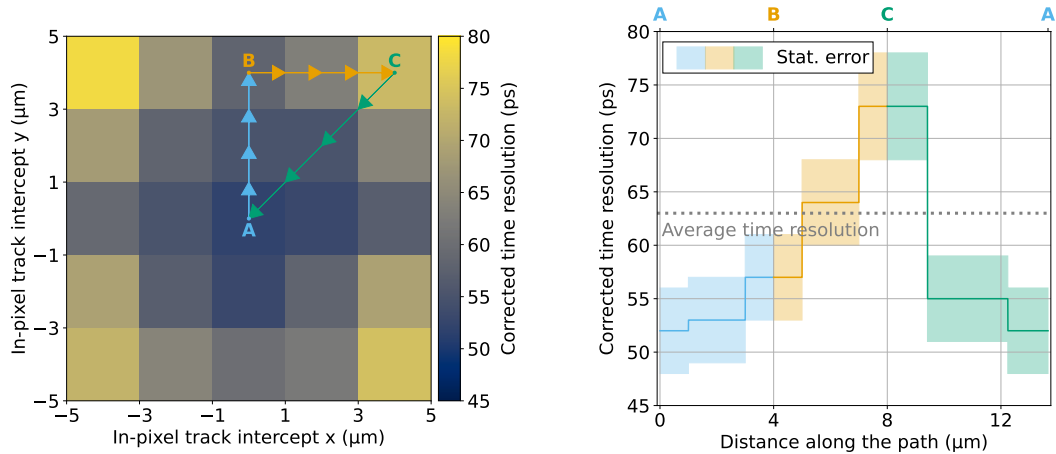


Fig. 6.57 Time-walk corrected in-pixel time resolution of the modified with gap AO10 chip operated at $V_{\text{sub}} = -4.8 \text{ V}$ (left). Time resolution in different positions: from the pixel center (A) to the edge (B) and the corner (C) (right). Image source [139].

Chapter 7

Conclusions

In the context of future detector upgrades in high energy particle physics experiments, MAPS are a promising option for next-generation, high-performance silicon vertex and tracking detectors, thanks to their reduced production costs and straightforward manufacturing process.

An intense R&D activity is carried out in the framework of the ARCADIA project at INFN to simulate and develop Fully Depleted Monolithic Active Pixel Sensors (FD-MAPS) in 110 nm CMOS technology, representing an attractive option for particle tracking and timing applications. In particular, they are suitable for the development of pixelated large-area Time Of Flight (TOF) detectors, as the one that will equip the ALICE 3 next-generation detector (2033–2034), the successor of the present ALICE experiment, for which a challenging time resolution of 20 ps RMS is required. Combining TCAD and Monte Carlo simulations represent a stable solution to get a realistic modeling of the detector response. Simulations of FD-MAPS with small collection electrode and 25 μm pitch enabled an exploration of their tracking capabilities and confirmed the suitability of these sensors for radiation detection applications. However, the simulated time resolution of approximately few ns, due to the difference in drift time of the generated e-h pairs in the detector volume, is not optimal for TOF applications with stringent requirements.

In order to improve the time resolution, the ARCADIA collaboration developed FD-MAPS with a large area collection electrode, covering $\sim 70\%$ of the pixel surface area. The timing performances of FD-MAPS in 110 nm CMOS process with pixel

pitch ranging from $50\text{ }\mu\text{m}$ to $200\text{ }\mu\text{m}$ and $25/35/50\text{ }\mu\text{m}$ thickness have been simulated. Sensors with pixel pitch $\geq 100\text{ }\mu\text{m}$ are suitable for optimal timing resolution, as the sensor intrinsic time resolution improves with larger pixel pitches, due to an enhanced uniformity of the weighting field. Integrated electronics has been designed and fabricated in a prototype developed in LFoundry 110 nm CIS process. However, tests conducted on the $48\text{ }\mu\text{m}$ thick device with a pitch of $50\text{ }\mu\text{m}$ demonstrated that the prototype will not achieve sub-100 ps time resolution, as the electronics jitter is the dominant contribution. To reduce the jitter component below 50 ps, a larger collected charge is needed, together with a more performant front-end electronics, keeping the power consumption under control.

To reach the target time resolution, a new sensor concept was developed within the ALICE 3 TOF Working Group, based on the previous experience gained in the ARCADIA collaboration. The sensor is a backside-biased FD-MAPS in a modified 110 nm CMOS process with the addition of a p-type gain layer implant underneath the collection electrode.

This new technology, also known as CMOS-LGAD, is regarded as a promising option for the future ALICE 3 TOF detector. The ARCADIA third engineering run hosted passive test structures and a prototype with AC-coupled readout electronics. This latter is a $16\text{ mm} \times 4\text{ mm}$ chip with 8 matrices of 64 pixels each and features a pixel size of $250\text{ }\mu\text{m} \times 100\text{ }\mu\text{m}$. The gain was measured both through optical characterisation of the passive test structures and in a beam test with MIPs, conducted on the prototype with integrated electronics. A gain of 2.5 was measured, lower than the initial target $\sim 10\text{-}30$. Moreover, a time resolution of 230 ps for $V_{\text{top}} = 45\text{ V}$ was assessed, due to a non optimal bias configuration and a large jitter caused by the low gain. A detailed numerical study based on TCAD simulations has followed and confirmed an error during the fabrication process, responsible for a shallow gain implant and, consequently, a lower multiplication factor. However, the measurements conducted on the first MAPS test structures with gain layer proved the remarkable feasibility of integrating a gain layer within the sensor technology developed in the ARCADIA project.

Subsequent in-beam measurements with optimised sensor biasing have led to a time resolution below 150 ps and even more promising results of sub-100 ps time resolutions on the new ARCADIA production will be exposed in future publications.

Additional exploration of commercial technological nodes for HEP applications was conducted by validating the 65 nm TPSCo CMOS imaging technology for the third generation ALICE Inner Tracking System (ITS3) at CERN, that will involve the replacement of the three inner-most layers of ALICE during LHC LS3 (2026-2029). The Multi Layer per Reticule (MLR1) has been the first submission to validate the Tower Partner Semiconductor Co. 65 nm technology, developed by the CERN Experimental Physics Department, together with the ALICE ITS3 upgrade project. In particular, the Analog Pixel Test Structure (APTS) allows a direct analogue readout of the pixels. Two different versions of the output buffer were designed: a source-follower (APTS-SF) and an operational amplifier (APTS-OA), the last devoted to measuring the time resolution. The APTS-OA was deeply characterised in laboratory and with in-beam measurements. The results obtained in this work proved that the charge collection performance benefits from the introduction of an additional n-doped low dose layer, as it was demonstrated for the 180 nm technology. The chip was successfully included in a beam telescope to measure its time resolution, spatial resolution and detection efficiency with MIPs. The modified pixel process with 10 μm pixel pitch features a notable time resolution of 63 ps, a detection efficiency larger than 99% and a spatial resolution of 2 μm at a substrate voltage V_{sub} of -4.8 V and 100 e^- threshold. The results not only underline the potential of the 65 nm CMOS imaging technology for HEP, but also highlight its applicability across a spectrum of disciplines requiring high resolution timing measurements, coupled with exceptional detection efficiency and spatial resolution. New results on irradiated APTS-OA chips will follow in short-term publications. This work will help the development of future technologies, pave the way for new applications, and drive advancements in fields beyond High Energy Physics.

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Appendices

The subsequent and final section of this thesis is dedicated to the appendices, which have been structured according to the corresponding chapters to ensure clarity and ease of reference. This material includes technical details and extended analyses which, if incorporated into the main body of the thesis, would have rendered the discussion overly dense and less accessible. Moreover, this section includes additional checks and studies carried out during the PhD research that, although relevant, have been placed in the appendices to maintain the readability and focus of the core chapters.

Appendix A

Silicon detectors

A.1 Silicon properties

Semiconductor	Si
atomic number (Z)	14
density ρ (g/cm ³)	2.328
dielectric constant ϵ	11.9
semiconductor type	indirect
bandgap E_G (eV)	1.12
intr. carrier density (cm ⁻³)	1.09×10^{10}
radiation length X_0 (cm)	9.36
average energy w_i for (e/h) creation (eV)	3.65
mobility (cm ² /Vs)	
electrons μ_n	1450
holes μ_h	500

Table A.1 Relevant properties of silicon. Data source [13].

A.2 Mass resolution in PID

$$m = \frac{p}{c} \sqrt{\frac{c^2 t^2}{L^2} - 1}$$

$$(\delta m)^2 = \left(\frac{\partial m}{\partial p} \right)^2 \delta p^2 + \left(\frac{\partial m}{\partial L} \right)^2 \delta L^2 + \left(\frac{\partial m}{\partial t} \right)^2 \delta t^2$$

$$\frac{\partial m}{\partial P} = \frac{1}{c} \sqrt{\frac{c^2 t^2}{L^2} - 1} = \frac{m}{p}$$

$$\frac{\partial m}{\partial L} = \frac{p c t^2}{L^3} \frac{1}{\sqrt{\frac{c^2 t^2}{L^2} - 1}}$$

$$\frac{\partial m}{\partial t} = \frac{p c t}{L^2} \frac{1}{\sqrt{\frac{c^2 t^2}{L^2} - 1}}$$

$$\left(\frac{\partial m}{\partial L} \right)^2 \cdot \frac{1}{m^2} = \frac{p^2 c^2 t^4}{L^6 \left[\frac{c^2 t^2}{L^2} - 1 \right]} \frac{c^2}{p^2 \left[\frac{c^2 t^2}{L^2} - 1 \right]} = \frac{c^4 t^4}{L^6} \frac{1}{\left[\frac{c^2 t^2}{L^2} - 1 \right]^2} = \frac{1}{L^2} \left[\frac{1}{\sqrt{1 - \beta^2}} \right]^4 = \frac{1}{L^2} \gamma^4$$

$$\left(\frac{\partial m}{\partial L} \right)^2 \frac{1}{m^2} \delta L^2 = \frac{\gamma^4}{L^2} \delta L^2 = \left[\gamma^2 \frac{\delta L}{L} \right]^2$$

$$\left(\frac{\partial m}{\partial t} \right)^2 \cdot \frac{1}{m^2} = \frac{p^2 c^2 t^2}{L^4 \left[\frac{c^2 t^2}{L^2} - 1 \right]} \frac{c^2}{p^2 \left[\frac{c^2 t^2}{L^2} - 1 \right]} = \frac{c^4 t^4}{L^4} \frac{1}{\left[\frac{c^2 t^2}{L^2} - 1 \right]^2} = \frac{1}{t^2} \left[\frac{1}{\sqrt{1 - \beta^2}} \right]^4 = \frac{1}{t^2} \gamma^4$$

$$\left(\frac{\partial m}{\partial t} \right)^2 \frac{1}{m^2} \delta t^2 = \frac{\gamma^4}{t^2} \delta t^2 = \left[\gamma^2 \frac{\delta t}{t} \right]^2$$

(A.1)

Appendix B

TCAD and Monte Carlo simulations

B.1 TCAD numerical solution of the Transport Model

Considering that the Poisson-drift-diffusion (PDD) mathematical model that describes the physics of semiconductors is characterised by systems of partial differential equations (PDEs), the software has to reduce the complexity of the calculation by:

1. discretizing of the problem in space and time;
2. solving systems of ordinary differential equations (ODEs) in place of PDEs.

A Finite Elements discretisation approach (FE) is followed by the software, but the details will not be provided in this work. Schematically, TCAD applies the following procedure for each mesh node:

- select a maximum number of iterations $\#_{\max}$ and a tolerance ϵ (maximum error of residuals);
- impose proper Initial Conditions (I.C.) and Boundary Conditions (B.C.);
- start from an initial guess φ'_0 for the electrostatic potential;
- the equilibrium solution φ_0 is obtained by solving only the Poisson equation with the I.C. and B.C.;

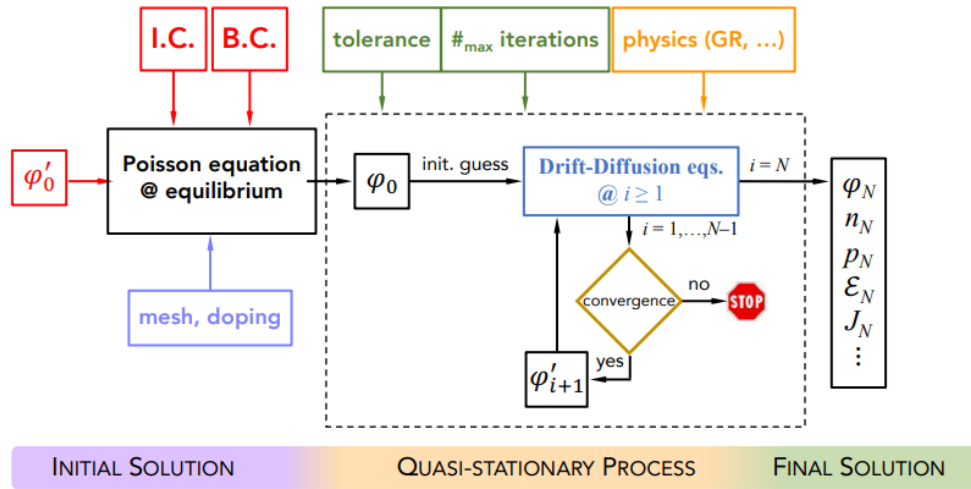


Fig. B.1 Schematical visualization of TCAD algorithm. Courtesy of M. Mandurrino.

- each step i of the ramp (e.g. voltage ramp) (with $i = 1, \dots, N$) is treated as a quasi-stationary state. The potential resulting from the Poisson solution at equilibrium φ_0 is used as initial guess for solving the DD equations at steps $i \geq 1$.

The TCAD procedure is shown schematically in Fig. B.1.

If the algorithm finds a solution in a finite number of iterations, the system converges. The non-convergence of the method may depend on several factors, like a too small minimum threshold value or a badly conditioned problem. Moreover, a key point is the choice of an appropriate mesh to guarantee the convergence of the calculation. An overly dense mesh may result in non-convergence due to insufficient computational power, whereas an excessively coarse mesh can lead to convergence problems because it fails to accurately define the device's physical parameters at critical points, where significant variations in electric field, electrostatic potential, and doping concentration occur.

B.2 Charge collection efficiency of the Arcadia Main Demonstrator FD-MAPS

In the context of simulating the performance of the Arcadia Main Demonstrator pixel sensor with $25\ \mu\text{m}$ pitch for radiation detection applications, the charge collection efficiency (CCE) can be found in [155]. A scan of a MIP impinging position was executed on the half diagonal of the central pixel of a 5×5 matrix. Five simulations on the half diagonal, as illustrated in Fig. B.2 (left), were carried out, moving the particle impact position from the center to the corner of the pixel. The CCE was computed as the ratio between the collected and the deposited charge. The collection

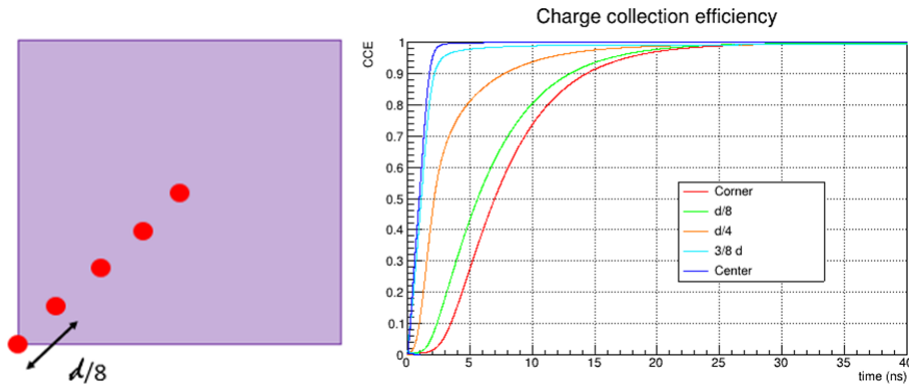


Fig. B.2 Graphical representation of the position scan on the half diagonal of the pixel (left) and charge collection efficiency as a function of time for the different impact positions (right). Image source [155].

diode is located at the center of each Arcadia Main Demonstrator pixel, and the time required for the charges to reach it depends on the particle impact position. As the impact shifts from the center toward the corner, the distance the charges must travel increases, leading to a longer drift time. Specifically, the total charge collection time ranges from a few nanoseconds for a central impact to approximately 15–20 ns for an impact at the corner.

B.3 Charge collection on ARCADIA FD-MAPS with large collection electrode

Fig. B.3 shows, in green, the average waveform of 100 simulated events where the MIPs were impinging always in the center of the pixel with pitch $150\ \mu\text{m}$. The contributions of electrons and holes to the total signal are displayed in blue and red, respectively. The last part of the signal is clearly due to holes, slower than electrons. When the particle hits at the corner among four pixels, charge sharing occurs. A

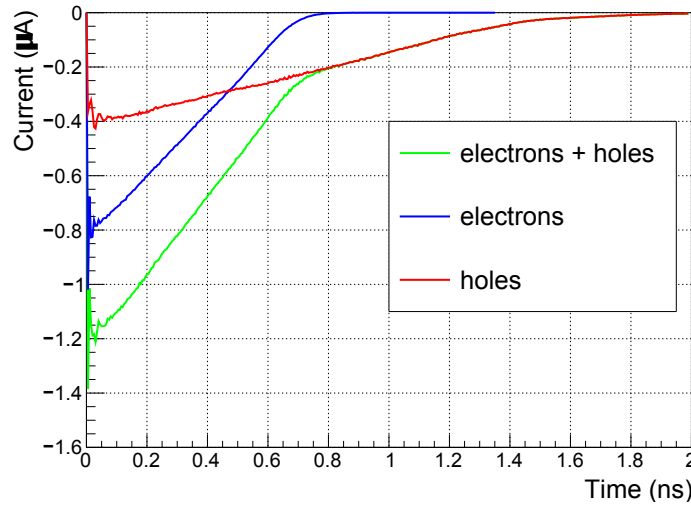


Fig. B.3 Average waveform of 100 events impinging at the center of the pixel with pitch $150\ \mu\text{m}$, in green. The contributions of electrons and holes to the total signal are highlighted in blue and red, respectively.

three-dimensional visualisation of charge sharing among four neighbouring pixels can be observed in Fig. B.4, where the motion of each group of charge carriers is represented by one line. In the plot, collected electrons are marked in blue colors, while collected holes are depicted in different shades of orange. The holes are collected mainly by the p-doped electrode located at the bottom of the sensor, at which a negative bias voltage is applied. Some holes are also collected by the p-wells, located near the n-wells at the top of the sensor.

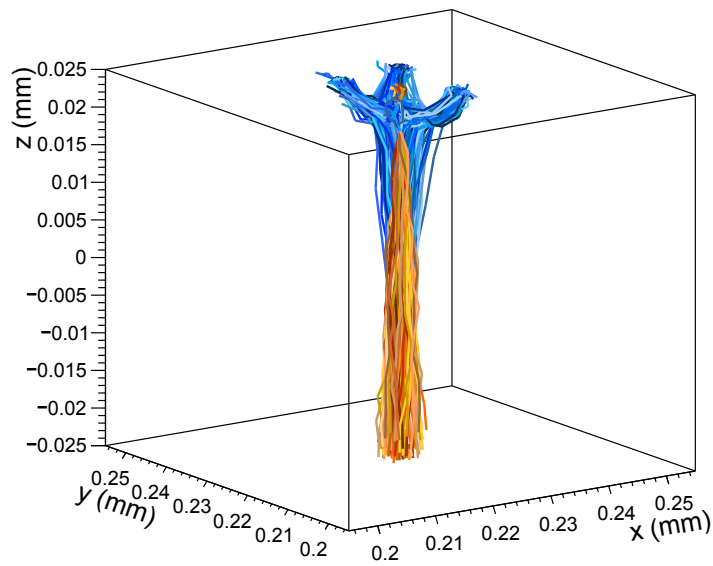


Fig. B.4 Three-dimensional visualisation of collected electrons and holes that have reached the implants. The particle is impinging at the corner among four pixels, causing charge sharing. Electrons are shown in blue and holes in orange.

B.4 Signals amplitude distribution on the HERMES chip

Fig. B.5 shows the distribution of the signals amplitude obtained on the HERMES chip with a ^{90}Sr radioactive source. The sensor has an active thickness of $48\text{ }\mu\text{m}$ and the measured MPV is $(76.2 \pm 0.6)\text{ mV}$

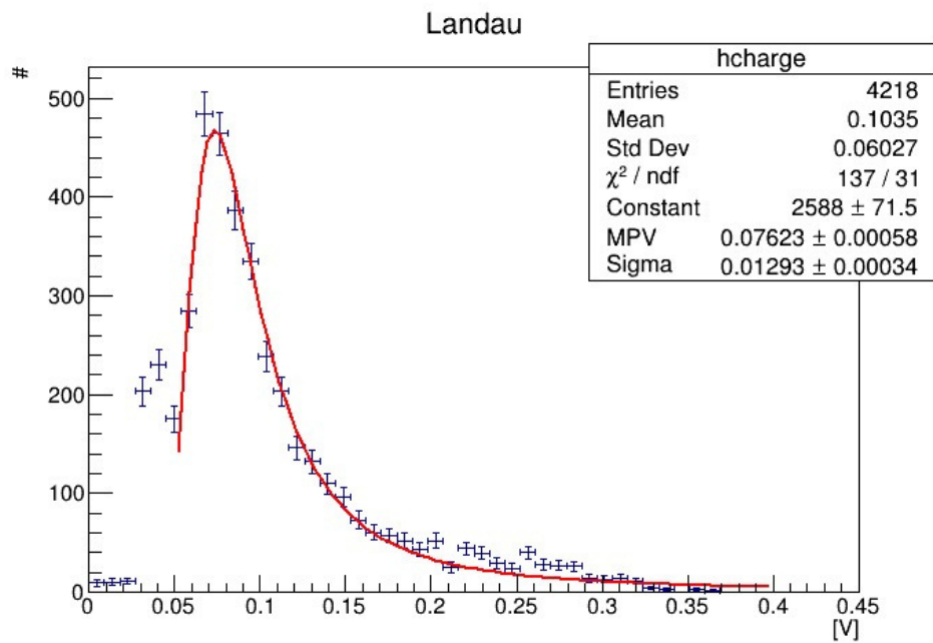


Fig. B.5 Signal amplitude distribution for the electrons from the ^{90}Sr decay. Superimposed Landau fit. Image source [128].

Appendix C

ARCADIA fully-depleted CMOS sensors with gain

C.1 Guard ring current measured on 48 μm thick passive test structures

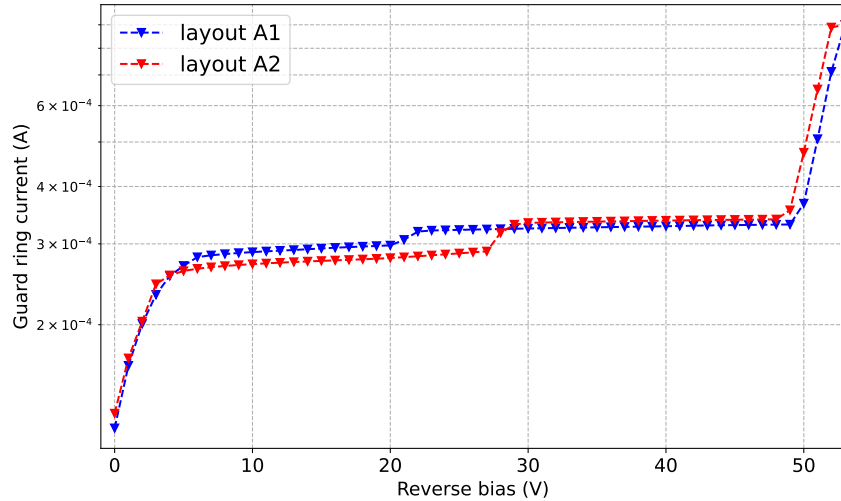


Fig. C.1 Current measured at the guard ring electrode of 48 μm thick passive structures as a function of the negative voltage applied to the p+ backside electrode, for the A1 and A2 layouts. The voltage applied at the collection electrode was fixed at 35 V and the guard ring was polarised at 3 V.

Fig. C.1 shows the current flowing at the guard ring of passive test structures with layout A1 and A2, measured at the probe station. An increase of the current can be observed around -49 V, due to an initial edge breakdown.

C.2 MADPix readout electronics

Fig. C.2 shows a schematic of MADPix in pixel front-end electronics followed by the output buffer located outside the matrices.

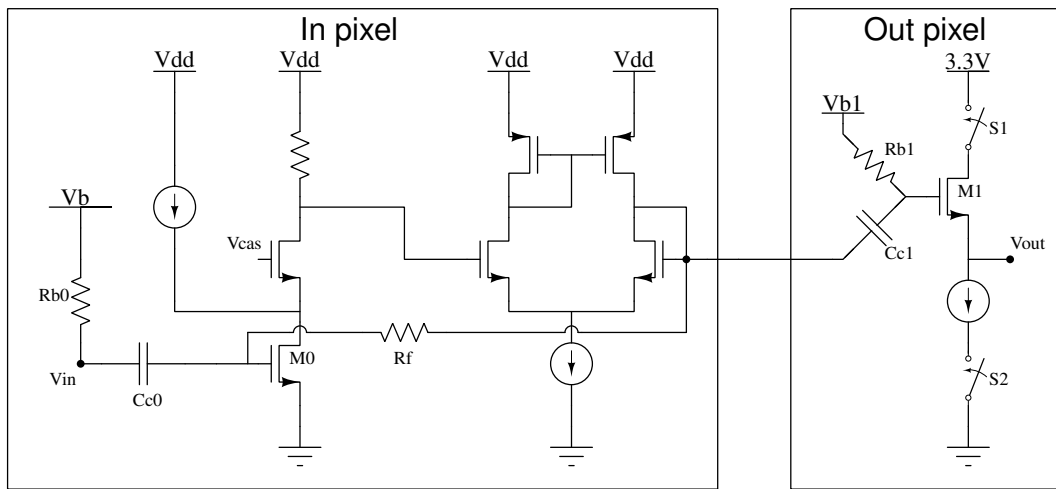


Fig. C.2 Schematic of the in pixel front-end electronics followed by the output buffer placed outside the matrices. Image source [130].

C.3 MADPix time resolution with constant fraction threshold algorithm

MADPix time resolution has been estimated also by applying a constant fraction threshold algorithm on the total signal amplitude and subsequent time walk correction. The time resolution has been estimated from the crossing time distributions, as described for the fixed threshold algorithm. The results for the measured time resolution as a function of the applied threshold are reported in Fig. C.3 for the A2 layout at V_{top} 30 V and 45 V. The time resolution worsens near the minimum and maximum thresholds, especially for the 30 V bias voltage, because in that regions the

signal features a lower slope, translating into a higher jitter. On the other hand, for $V_{top} = 45$ V, the slope of the signal remains constant over a wider range of applied thresholds, resulting in a more stable timing performance.

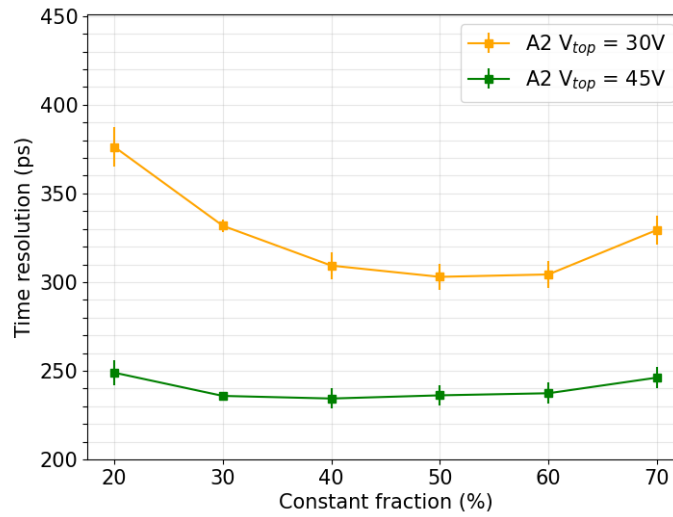


Fig. C.3 Time resolution of a 110 nm prototype with gain layer and integrated electronics as a function of the applied constant fraction threshold. The sensor has an A2 termination layout. Image source [135].

Appendix D

Validation of the 65 nm technology

D.1 Working point optimisation

The coarse scan

Starting from the coarse scan on the six front-end parameters, one can observe the trend of the quantity of interests (baseline, amplitude and fall time) as a function of that particular parameter, keeping all the other at their typical values. For example, Fig. D.1 shows the results obtained varying I_{biasp} for different reverse biases reported in different colors. Similar plots for the other five parameters are reported in the following. The green boxes highlight the regions in which the front-end features an improved performance. For example, it's easy to see that for $I_{\text{biasp}} \geq 11.25 \mu\text{A}$, the baseline has already reached the plateau and the same stands for the amplitude, while the fall time is already decreased and it starts to stabilise from that point on. This region can therefore be defined as a good starting range in which focusing and executing a more accurate study. To this purpose, for each parameter, it's possible to select three values lying in the proper window, ending up with the 729 possible configurations and thereafter apply the matrix of cuts. An example of the selected values for all the different biases in this study is reported in tab. D.1:

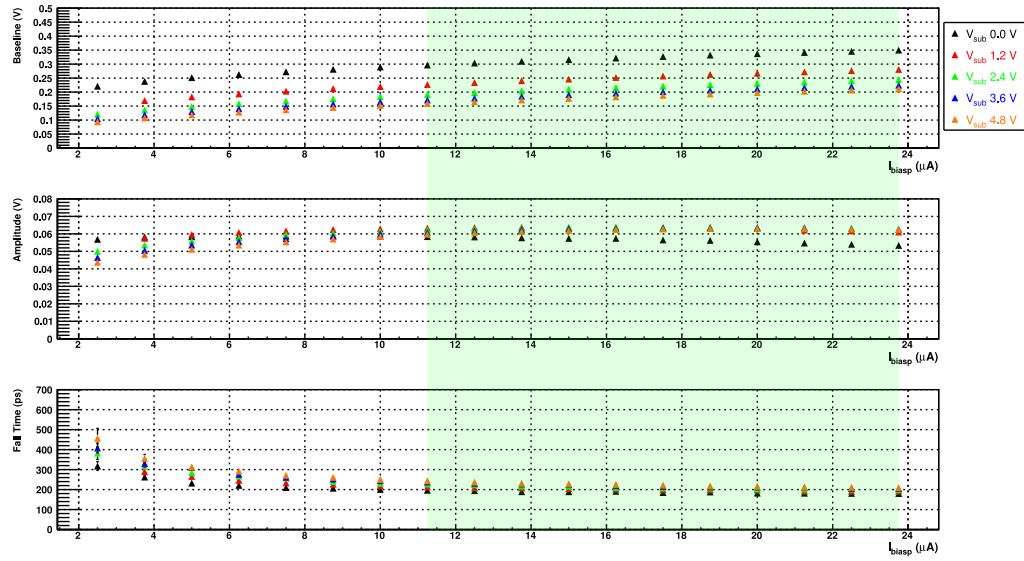


Fig. D.1 Baseline, amplitude and fall time as a function of I_{biasp} for different reverse biases in different colors.

Parameter	Typ. value	Tested values
V_{casn} (mV)	750	560 – 630 – 900
V_{casp} (mV)	300	140 – 270 – 400
I_{biasn} (uA)	200	62.5 – 125 – 187.5
I_{biasp} (uA)	20	11.25 – 17.5 – 23.75
I_{bias3} (uA)	200	112.5 – 162.5 – 212.5
I_{bias4} (mA)	2.5	1 – 1.8 – 2.6

Table D.1 Investigated parameters with their nominal settings (Typ.) and three selected values for the study. Reported values are corrected for the front-end mirror ratio.

Application of the cuts

The best configuration follows a selection based on the definition of the plateaux in the derivative, fall time and amplitude. In particular, the following criteria have been adopted:

- Derivative plateau: maximum of the derivative curve - 10% of the maximum;
- Fall time plateau: minimum of the fall time + 10% of the minimum;
- Amplitude plateau: maximum amplitude - 10% of the maximum;

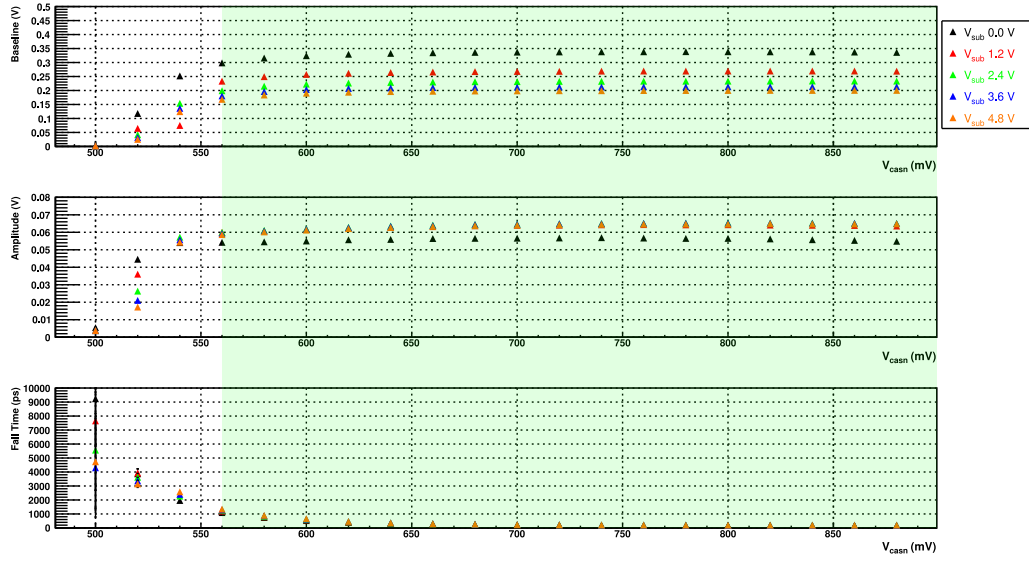


Fig. D.2 Baseline, amplitude and fall time as a function of V_{casn} for different reverse bias in different colors.

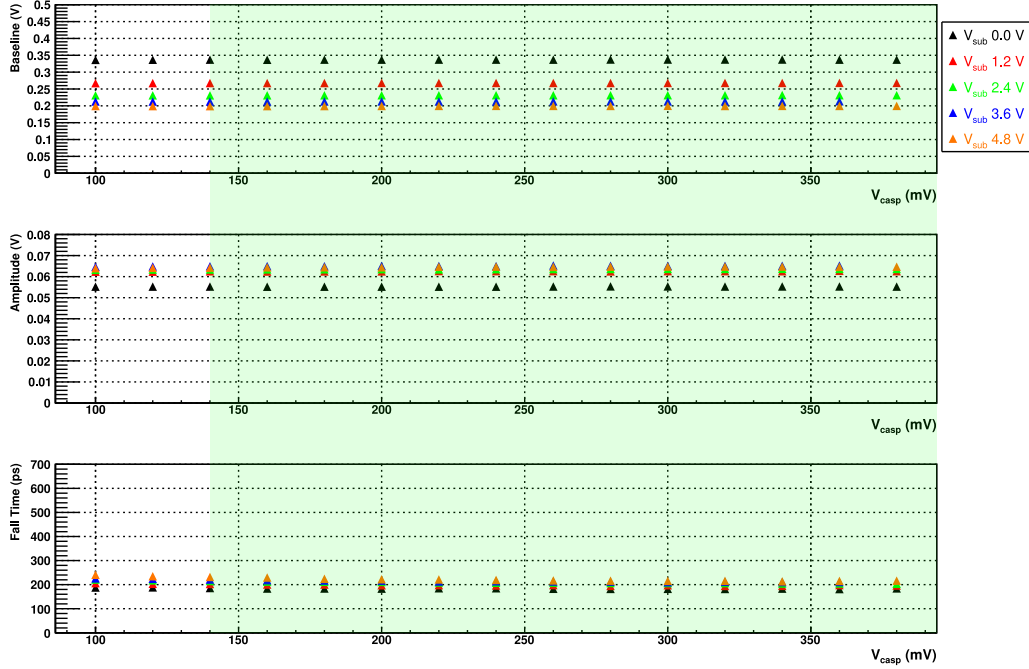


Fig. D.3 Baseline, amplitude and fall time as a function of V_{casp} for different reverse bias in different colors.

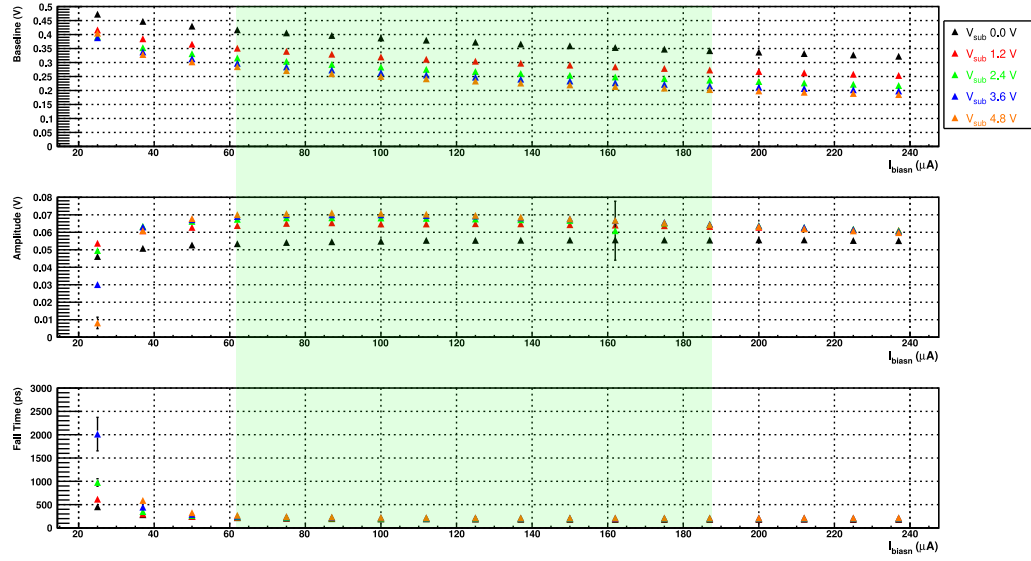


Fig. D.4 Baseline, amplitude and fall time as a function of I_{biasn} for different reverse bias in different colors.

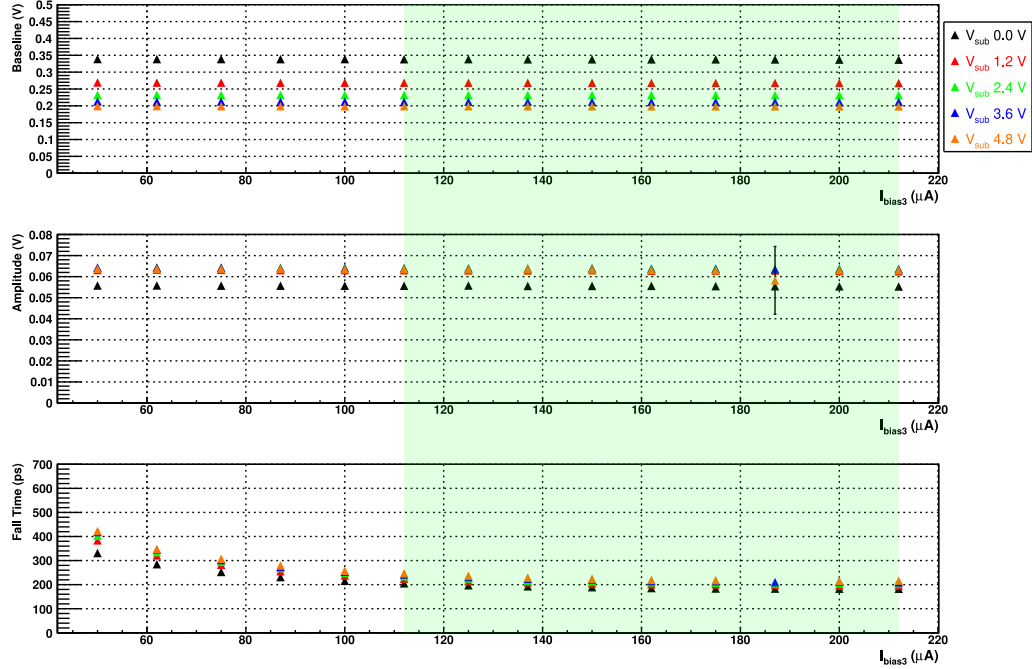


Fig. D.5 Baseline, amplitude and fall time as a function of I_{bias3} for different reverse bias in different colors.

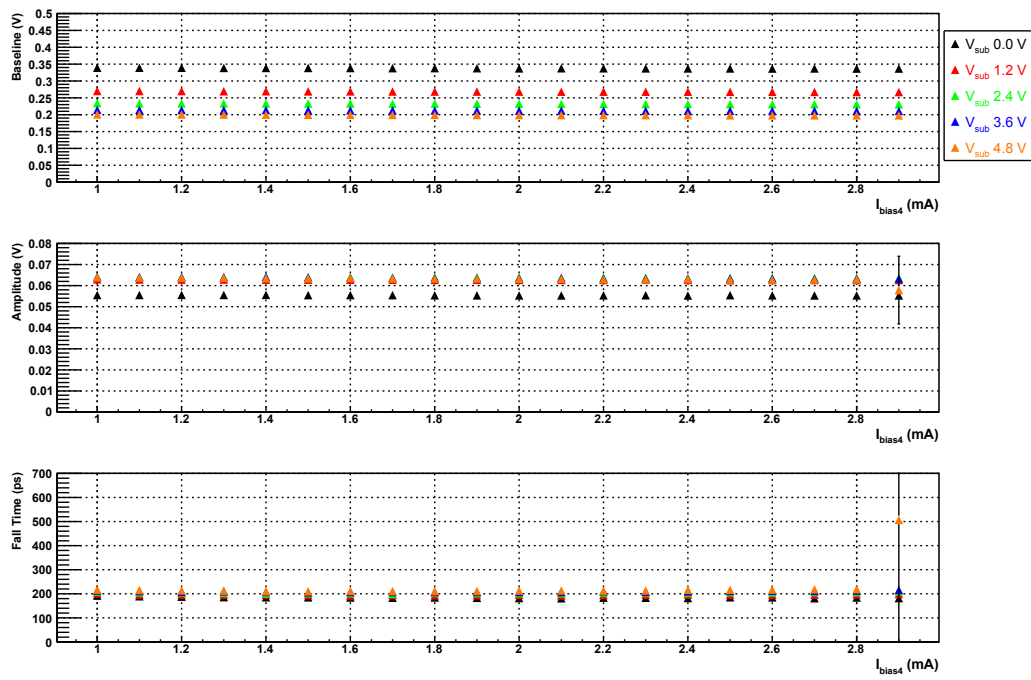


Fig. D.6 Baseline, amplitude and fall time as a function of I_{bias4} for different reverse bias in different colors.

D.2 Sensor capacitance as a function of reverse bias

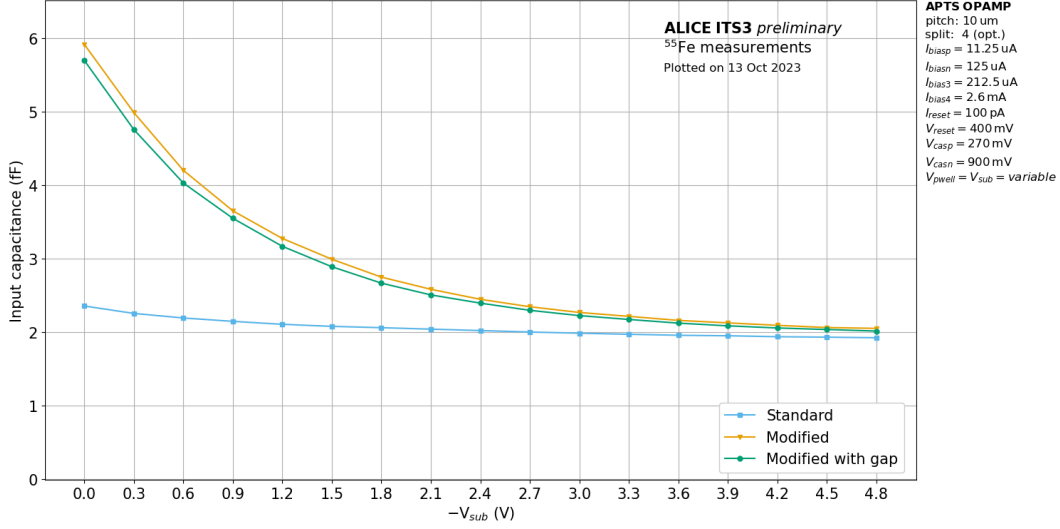


Fig. D.7 sensor input capacitance as function of V_{sub} for standard, modified and modified with gap processes.

Fig. D.7 compares the measured sensor capacitance of a standard, modified and modified with gap AO10 processes. The capacitance is retrieved by combining ^{55}Fe and test pulses measurement results. In the standard process, the depletion layer has a spherical shape and the capacitance can be written as:

$$C_{spherical} = 4\pi\epsilon \frac{R_1 R_2}{R_2 - R_1} \approx 4\pi\epsilon R_1 \quad (\text{D.1})$$

where R_1 is approximately the radius of the collection electrode ($\approx 0.5 \mu\text{m}$), responsible of the small capacitance on the full V_{sub} range. For what concerns the modified and modified with gap processes, they feature a planar junction from which the depletion starts and a depletion width having a stronger dependence from the reverse bias. For this reason, also the capacitance is affected by such dependence and shows a more pronounced trend with the reverse bias.

D.3 AO10 chip characterisation with pulsing circuit

The full matrix was pulsed varying the amplitude of the pulsing signal V_h from 0.3 V to 1.2 V with steps of 0.1 V. Fig. D.8 shows the signal amplitude of the four central pixels of the matrix (named J5, J6, J9 and J10) as a function of V_h for different V_{sub} .

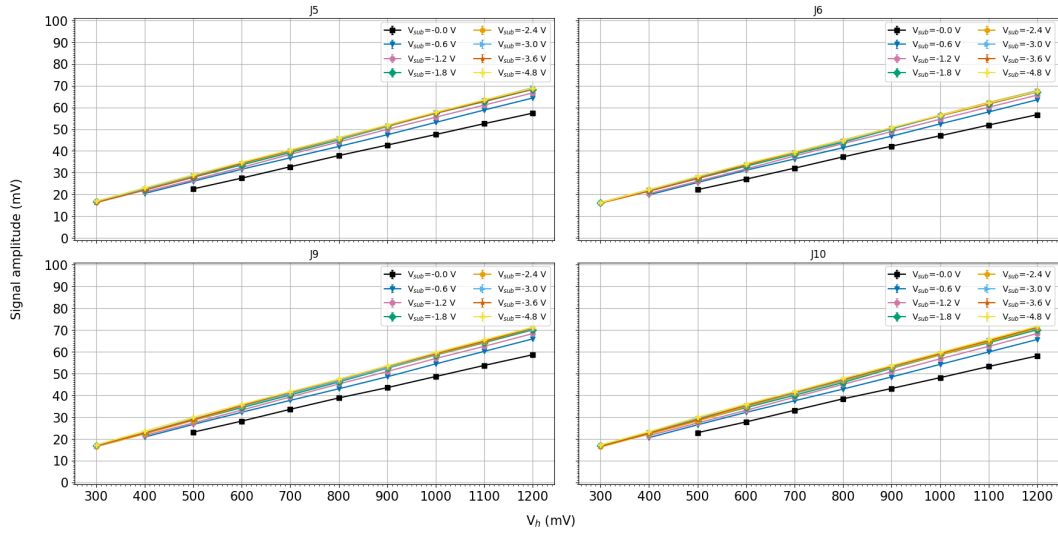


Fig. D.8 Signal amplitude as a function of V_h for different reverse bias for the four central pixels of a AO10 chip.

Fig. D.9 represents the slope dV/dt computed by considering the usual interval 10% - 90% of the signal amplitude. An increase of the slope with the amplitude of the pulsing signal can be observed.

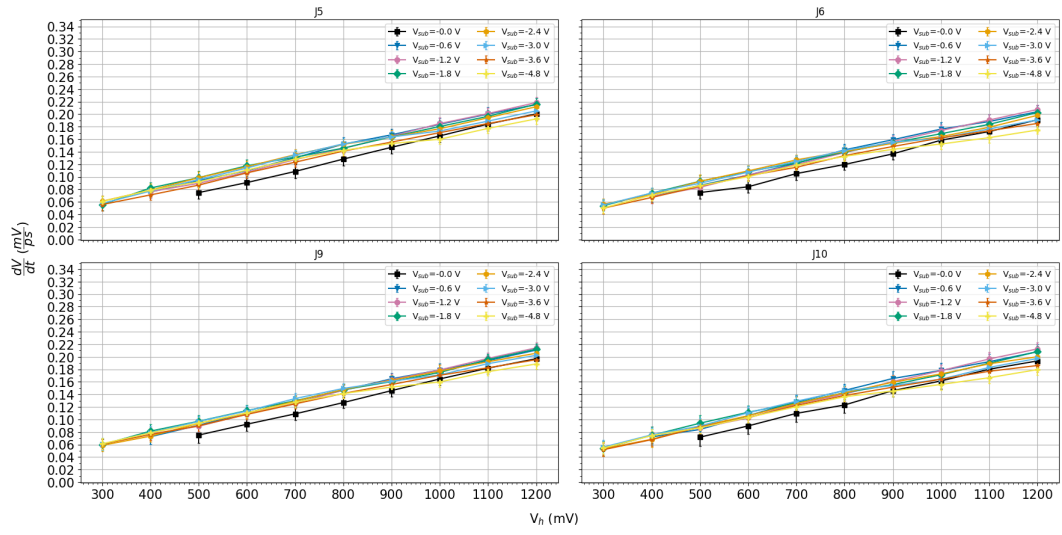


Fig. D.9 Signal slope as a function of V_h for different reverse bias for the four central pixels of a AO10 chip.

D.4 Jitter evaluation

Jitter has been computed for pixels 2, 3 and 4 as:

$$\sigma_2^2 = \frac{\sigma_{2-3}^2 + \sigma_{2-4}^2 - \sigma_{3-4}^2}{2} \quad (D.2)$$

$$\sigma_3^2 = \frac{\sigma_{1-3}^2 + \sigma_{3-4}^2 - \sigma_{1-4}^2}{2} \quad (D.3)$$

$$\sigma_4^2 = \frac{\sigma_{1-4}^2 + \sigma_{3-4}^2 - \sigma_{1-3}^2}{2} \quad (D.4)$$

D.5 Gain corrected signals APTS-OA

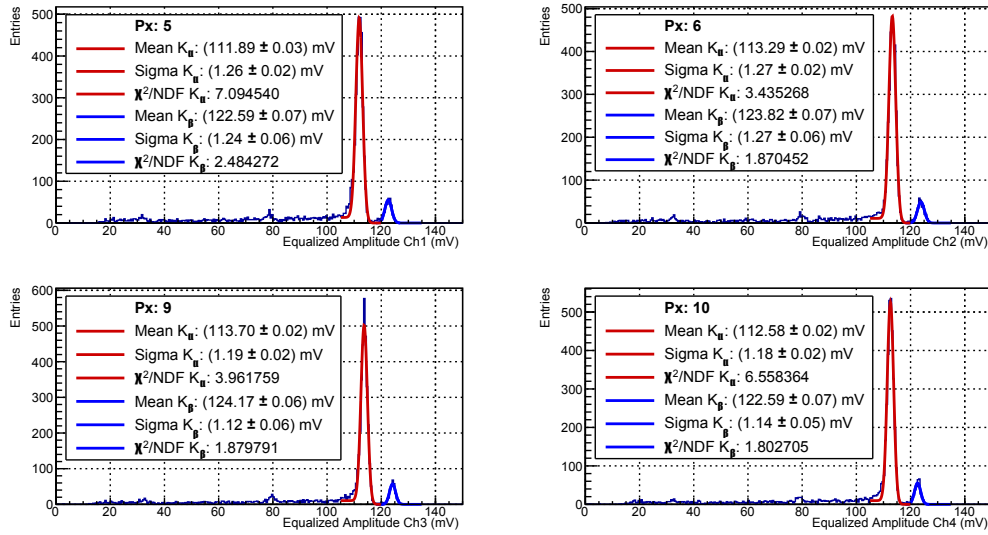


Fig. D.10 Gain corrected single pixel cluster signal distributions for the four central pixels of the modified with gap chip.

Fig. D.10 shows the gain corrected single pixel cluster signal distributions for the four central pixel of the matrix belonging to an AO10P test structure. After this correction the dispersion percentage among the K_{α} peak positions decreased to 1.6%.

D.6 Si-K $_{\alpha}$ and Si-K $_{\alpha}$ escape peaks

- The Si-K $_{\alpha}$ peak results from a statistical probability that some of the X-rays, emitted from the ^{55}Fe , interact with Si K-shell electrons in the detector. For X-rays with energy higher than the Si-K absorption edge, the photon can therefore knock-out some Si K-shell electrons in the detector, involving a process of secondary X-ray generation (Si-K $_{\alpha}$ X-ray at 1.74 keV) in the detector itself.
- The escape peak occurs when a Si X-ray escapes the detector, resulting in an artificial peak at an energy equal to the energy of the parent peak minus the energy of the generated Si X-ray (mainly the principal Si-K $_{\alpha}$ at 1.74 keV). The Si-K $_{\alpha}$ Escape peak will therefore have a residual energy of 4.1 keV.

D.7 Energy calibration APTS-OA

Cluster energy distribution, obtained as the energy calibrated spectra for all the pixels of every cluster configuration.

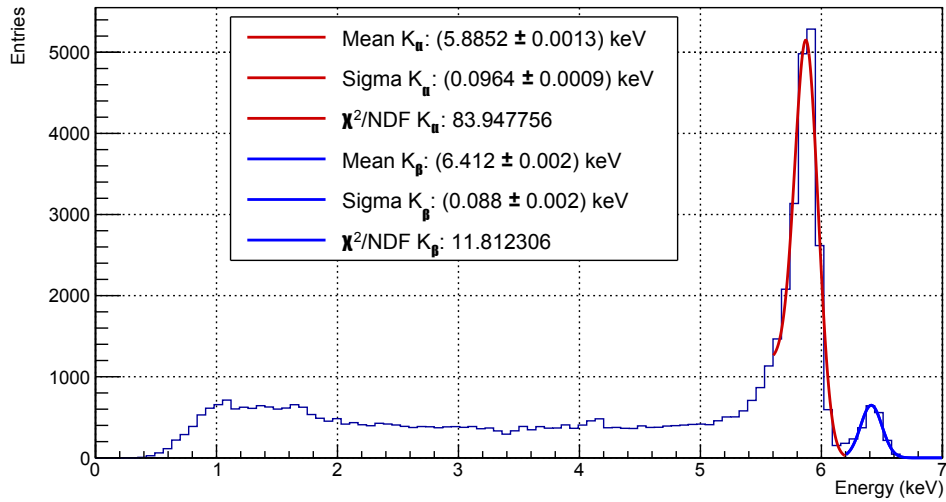


Fig. D.11 Cluster energy distribution.

D.8 Comparison between standard and modified with gap processes

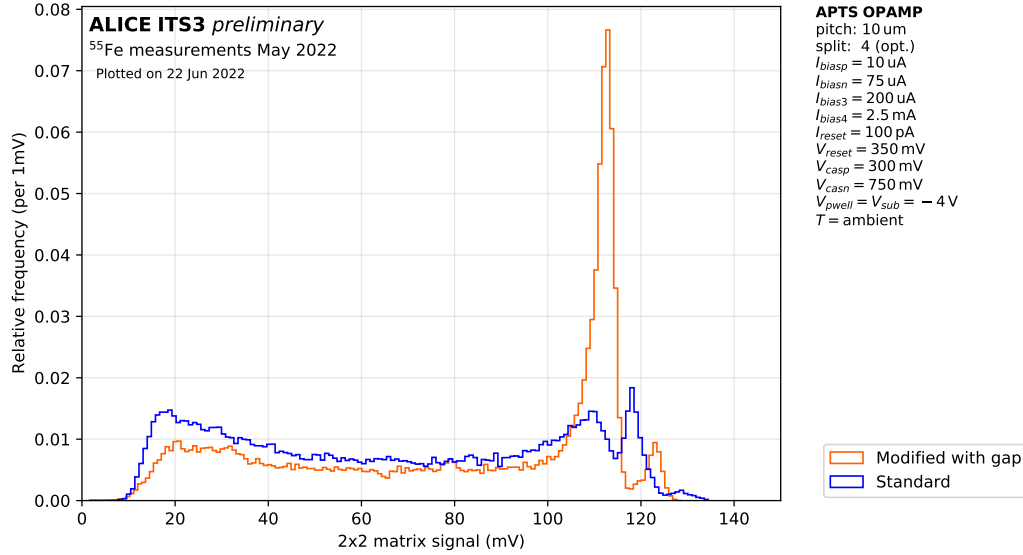


Fig. D.12 Comparison standard vs modified with gap 2x2 matrix signal amplitude.

Figure D.12 shows the 2x2 matrix signal amplitude distribution obtained for the standard and for the modified with gap sensor processes superimposed. A clear difference emerges between the two: the standard process shows a clearly visible component of charge sharing in the population of events with low amplitudes, while the modified with gap has a more pronounced K_{α} peak and a decreased charge sharing component. The same comparison is illustrated in Fig. D.13 between the maximum pixel signal amplitude distributions of the standard and the modified with gap processes. Furthermore, it's possible to notice a shift in the K_{α} peak position between the two sensor processes. The reason for the larger signals observed in the standard process is represented by a smaller input capacitance (see App. D.2).

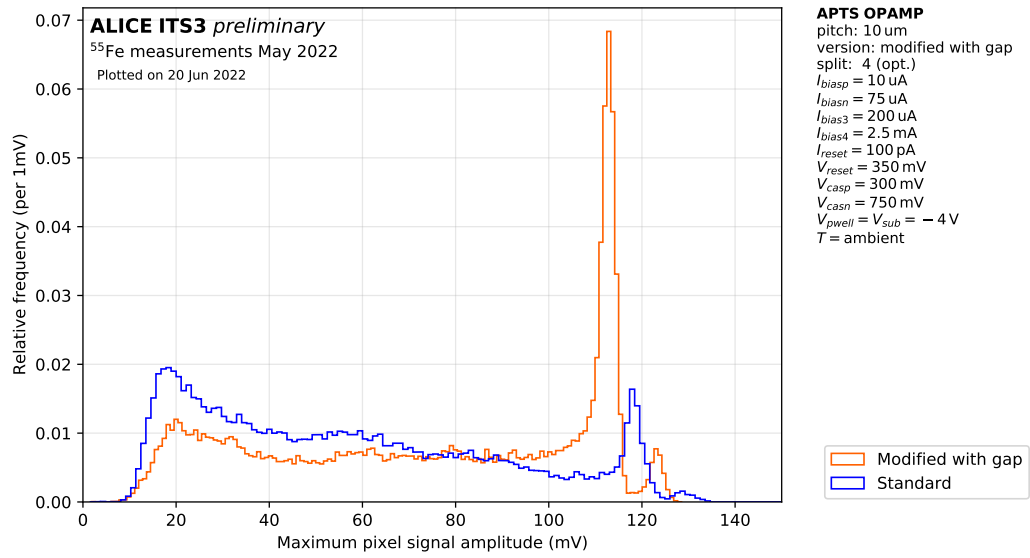


Fig. D.13 Maximum pixel signal amplitude for the standard and modified with gap processes in different colors.

D.9 Noise distributions

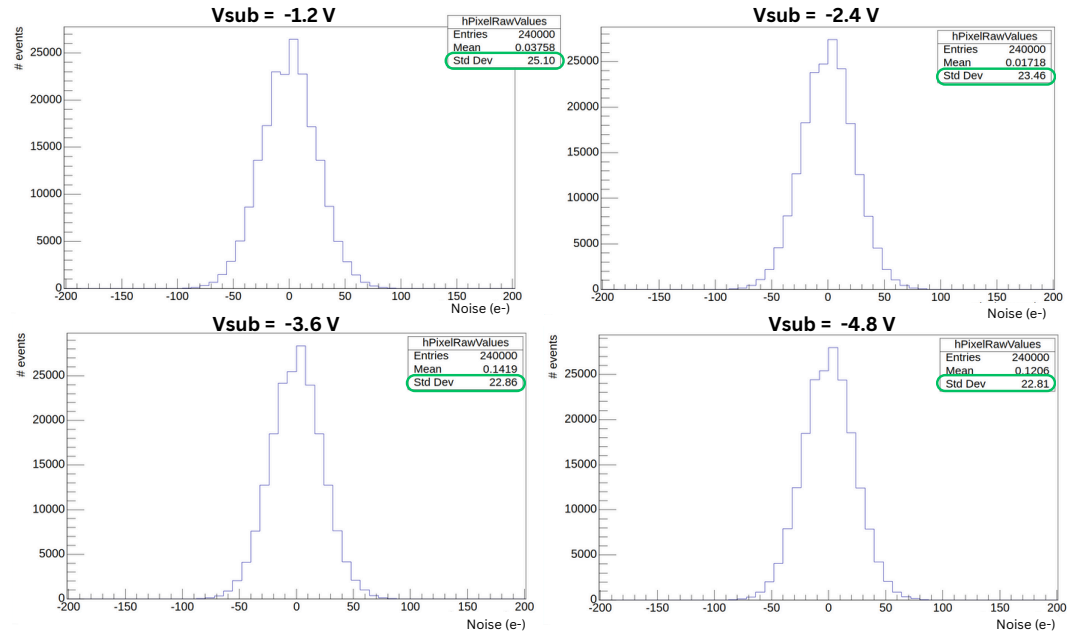


Fig. D.14 Noise distribution for different V_{sub} values.

Noise distributions reported in Fig. D.14 have been computed as noise on the single point, i.e. (underline - baseline) in a region where there is no signal.

D.10 η correction

The fit parameters from the third order polynomial function employed to fit the η distribution become more steady when a larger statistic is considered. Fig. D.15 illustrates this behavior for the x coordinate on the modified with gap DUT at $V_{sub} = -4.8$ V.

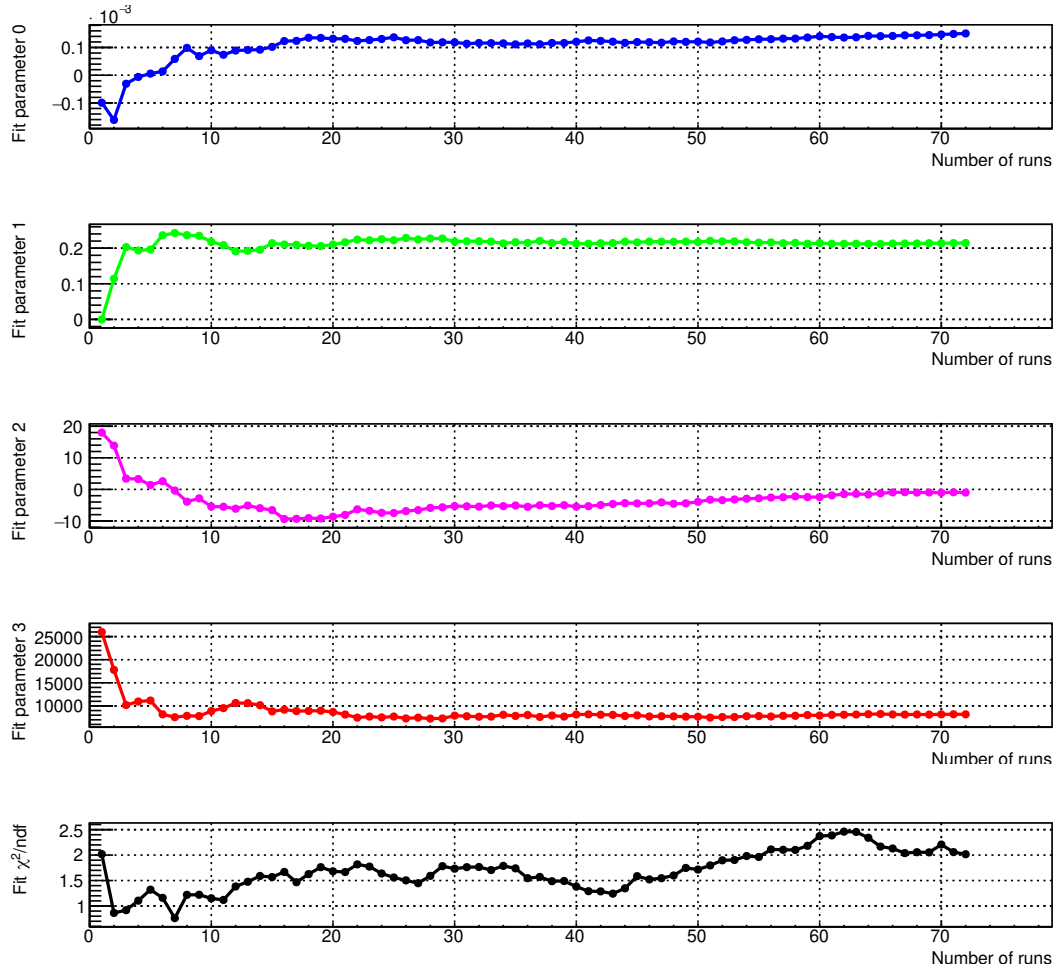


Fig. D.15 Fit parameters for the x coordinate η distributions showing a stabilisation with increased statistics.

D.11 Analog front-end settings

The operating point used for test beam measurements reported in this thesis is illustrated in the Table. 6.2. The currents I_{reset} , I_{biasn} , I_{biasp} are shown in Fig. 6.4 while the biasing currents for the operational amplifier I_{bias3} , I_{bias4} , V_{casn} , and V_{casp} are not depicted. Finally, the value of V_{reset} chosen depending on V_{sub} in order to operate in the most linear region of the front-end is reported in Table D.3.

In-pixel	
I_{reset}	100 pA
I_{biasn}	$-125 \mu\text{A}$
I_{biasp}	$11.25 \mu\text{A}$
Out of pixel	
I_{bias3}	$212.5 \mu\text{A}$
I_{bias4}	2.6 mA
V_{casn}	900 mV
V_{casp}	270 mV

Table D.2 The operating point used for the measurement. See the details in Fig. 6.4.

$V_{\text{sub}}(\text{V})$	-1.2	-2.4	-3.6	-4.8
$V_{\text{reset}}(\text{mV})$	380	420	440	440

Table D.3 V_{reset} settings at different V_{sub}

D.12 Spatial residual distributions on the modified with gap DUT

Fig. D.16 shows the residual distributions on the modified with gap DUT operated at $V_{\text{sub}} -4.8$ V, with different applied thresholds in different colors.

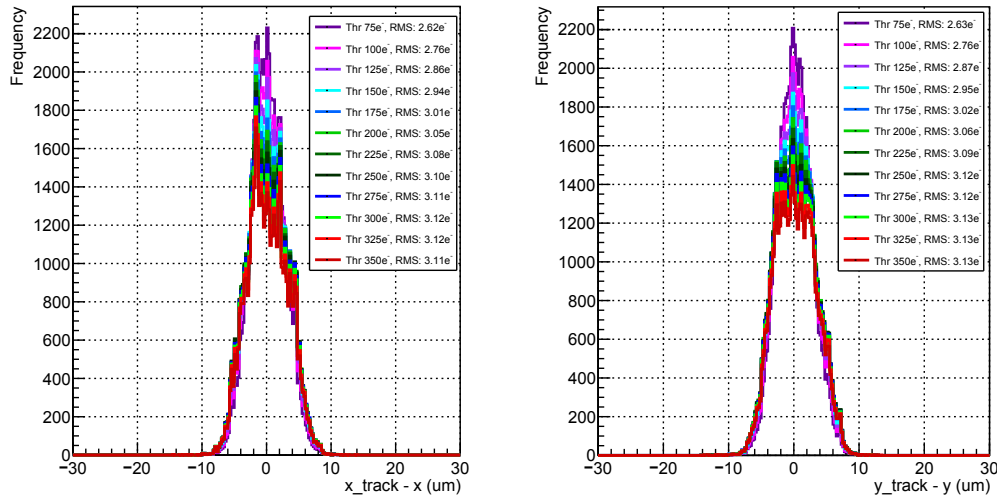


Fig. D.16 Residual distributions obtained for x (left) and y (right) on AO10P for $V_{\text{sub}} -4.8$ V with different applied thresholds in different colors.

D.13 Spatial residual distributions computed only with the seed pixel

Fig. D.16 shows the spatial residual distributions obtained on a modified DUT, considering only the seed pixel signal position. The aim was to cross check the telescope tracking resolution considering the DUT with a purely binary readout.

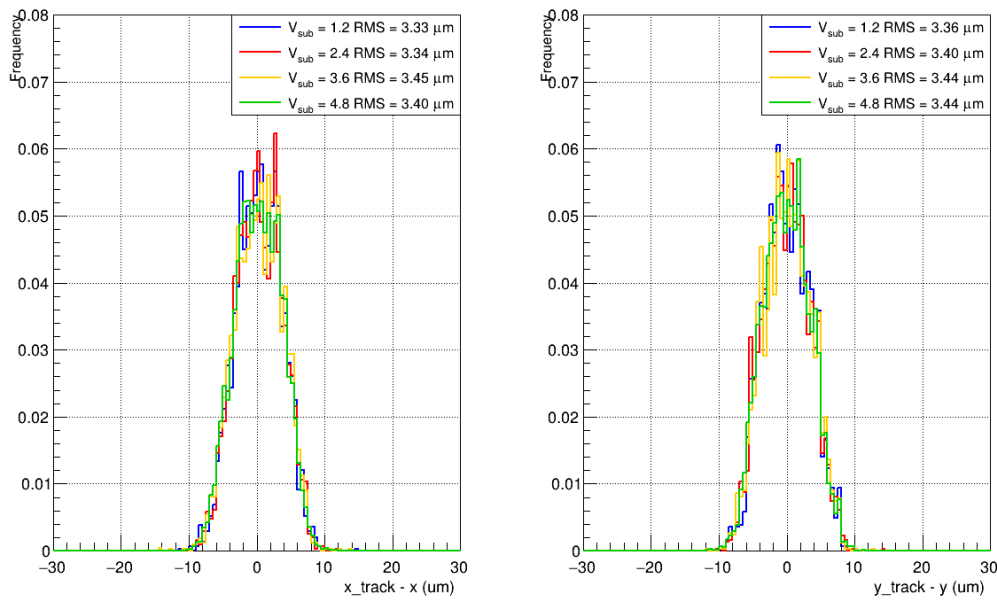


Fig. D.17 Residual distributions obtained for x (left) and y (right) on the modified DUT by considering only the seed pixel of the cluster to define the cluster position and with a clustering threshold of $0 e^-$.

D.14 Tracking resolution estimation

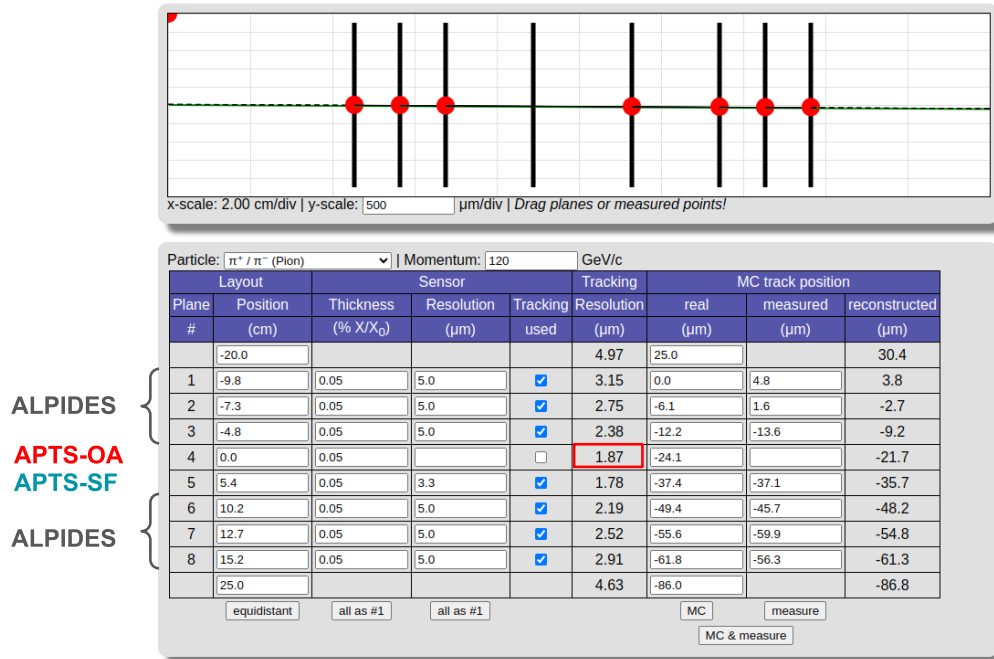


Fig. D.18 Telescope optimiser interface with estimated tracking resolution of 1.87 μm on the APTS-OA DUT. The spatial resolution used for the APTS-SF trigger plane is 3.3 μm

D.15 Detection efficiency with larger ROI

The detection efficiency has been computed by considering a strict selection of tracks impinging inside the three oscilloscope readout pixels. However, Fig. D.19 demonstrates that an enlarged ROI of half a pixel ($5\ \mu\text{m}$) wouldn't have changed the results.

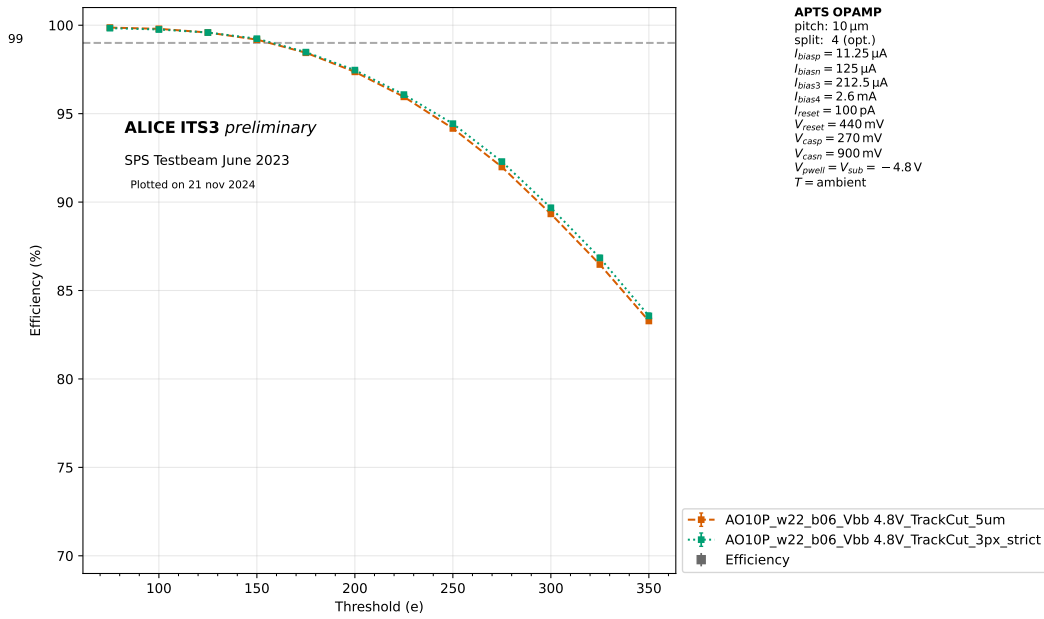


Fig. D.19 Detection efficiency on modified with gap DUT at $V_{sub} = -4.8\ \text{V}$ with two different selection on tracks. In green: the usual selection with tracks impinging inside the three oscilloscope readout pixels. In red: tracks impinging inside the three oscilloscope readout pixels plus an external crown of half a pixel.

D.16 Spatial resolution comparison with APTS-SF

Comparison of spatial resolution and cluster size between APTS-OA and APTS-SF as a function of the clustering threshold. Both APTS chips feature $10\ \mu\text{m}$ pixel pitch in modified with gap process and were operated at $V_{sub} = -1.2\ \text{V}$.

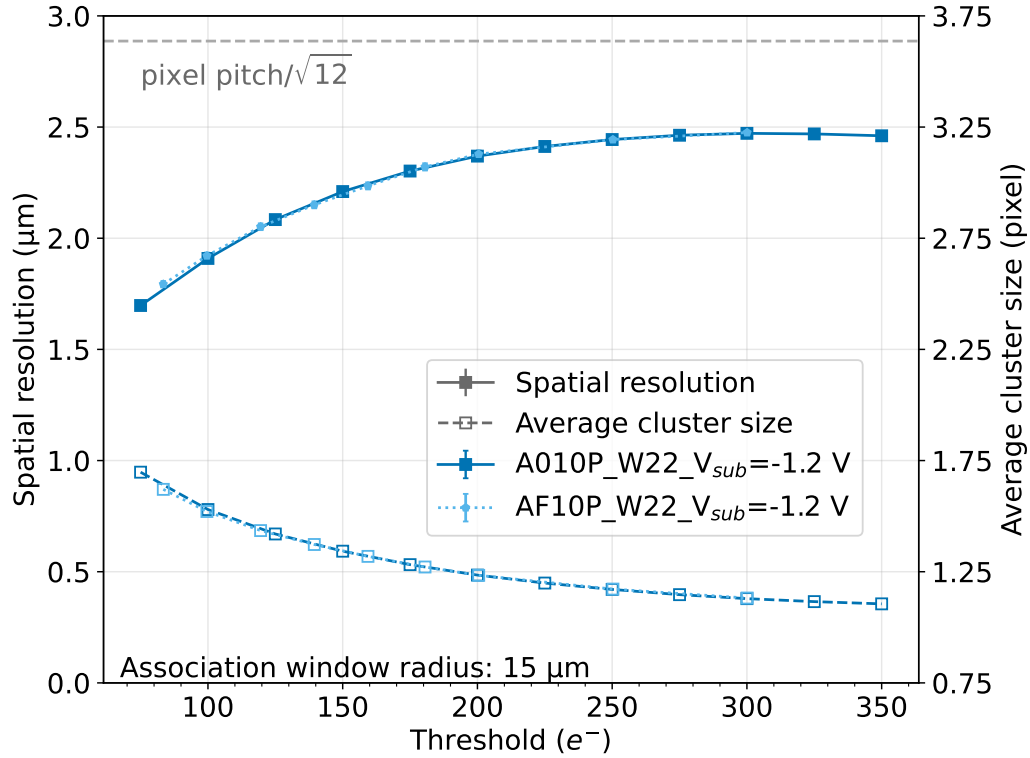


Fig. D.20 Spatial resolution and cluster size comparison between the APTS-OA and APTS-SF in a $10\ \mu\text{m}$ pitch, modified with gap process and $V_{sub} = -1.2\ \text{V}$ showing excellent agreement. Thanks to G. Alocco for providing the APTS-SF analysis' results.

Appendix E

List of Acronyms

- **ALICE**: A Large Ion Collider Experiment
- **APD**: Avalanche PhotoDiode
- **APTS-OA**: Analogue Pixel Test Structure with Operational Amplifier
- **ARCADIA**: Advanced Readout CMOS Architectures with Depleted Integrated Arrays
- **ASI**: Italian Space Agency
- **ASIC**: Application-Specific Integrated Circuit
- **CAD**: Computer-Aided Design
- **CCD**: Charge-Coupled Devices
- **CMOS**: Complementary Metal Oxide Semiconductor
- **CSES**: China Seismo-Electromagnetic Satellite
- **C-V**: Capacitance-Voltage
- **DAQ**: Data Acquisition
- **DUT**: Device Under Test
- **FD MAPS**: Fully Depleted Monolithic Active Pixel Sensors
- **FE**: Front-end
- **FF**: Fill Factor

- **FPGA:** Field-Programmable Gate Array
- **FWHM:** Full Width at Half Maximum
- **GBL:** General Broken Line
- **HEP:** High Energy Physics
- **HEPD:** High-Energy Particle Detector
- **HL-LHC:** High Luminosity LHC
- **HV:** High Voltage
- **ITS2:** Inner Tracking System 2
- **ITS3:** Inner Tracking System 3
- **I-V:** Current-Voltage
- **INFN:** Istituto Nazionale di Fisica Nucleare
- **LGAD:** Low-Gain Avalanche Detector
- **LS:** Long Shutdown
- **LSB:** Least Significant Bit
- **MAPS:** Monolithic Active Pixel Sensors
- **MIP:** Minimum Ionizing Particle
- **MLR1:** Multi Layer per Reticle
- **MOSFET:** Metal-Oxide-Semiconductor Field-Effect Transistor
- **MRPC:** Multigap Resistive Plate Chambers
- **OCCAM:** Open Computing Cluster for Advanced data Manipulation
- **PCB:** Printed Circuit Board
- **R&D:** Research and Development
- **RMS:** Root Mean Square
- **SiPM:** Silicon Photomultipliers
- **SNR:** Signal-to-Noise Ratio

- **SPAD**: Single Photon Avalanche Diode
- **TCAD**: Technology Computer-Aided Design
- **TCT**: Transient Current Technique
- **ToA**: Time of Arrival
- **TOF**: Time Of Flight

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