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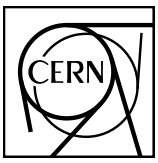

Study of signal discrimination for timing measurements

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Abstract

The timing detectors of the CMS-TOTEM Precision Proton Spectrometer (CT-PPS) are currently read out using discrete components, separated into three boards; the first board hosts the sensors and the amplifiers, the second one hosts the discriminators and the third is dedicated to the Time to Digital Converter (TDC) and to the interface with the data acquisition system (DAQ). This work proposes a new front-end electronics for the timing detector, with sensors, amplifiers and discriminators integrated on the same board. We simulated an updated version of the amplifier together with a discriminator designed using commercial components. We decided to use an LVDS buffer as a discriminator, because of its cost, availability, speed and lo w power consumption. As a proof of concept, we used the LVDS input of an FPGA to discriminate signals produced by a detector prototype, using a radioactive source.

1 Introduction

The TOTEM Experiment at CERN was designed to measure the total proton-proton cross-section and to study elastic scattering and diffractive processes. Some of the TOTEM detectors are placed inside Roman Pots, movable sections of the LHC beam pipe that can be inserted down to 1 mm from the beam; they are installed between 210 m and 220 m on both sides of the CMS interaction point. These detectors are used for both tracking and time of arrival measurements in the CMS-TOTEM Precision Proton Spectrometer (CT-PPS). In particular, the present front-end electronics of the timing detectors is organized into three boards. The first board, installed inside the Roman Pots, includes sensors and the amplifiers. The amplified signal is transferred to a NINO chip [1], used as a discriminator. High-Performance Time to Digital Converter (HPTDC) then processes the signal from the discriminator. Using three interconnected boards might cause problems due to damage of cables or connectors during operation and complicate the installation procedure. Moreover, the NINO chip is more than ten years old and needs to be replaced by a new component, but creating a new Application Specific Integrated Circuit (ASIC) would be expensive and complicated. Hence, we decided to create a discriminator using commercial components and integrate it on the board with the sensors. Furthermore, being this board inside the Roman Pot, the power consumption has to be optimized.

We propose a new front-end electronics for the timing detector where sensors, amplifiers and discriminators are integrated on the same board, as shown in figure 1. The final design should allow a time precision better than 50 ps with a power consumption below 150 mW.

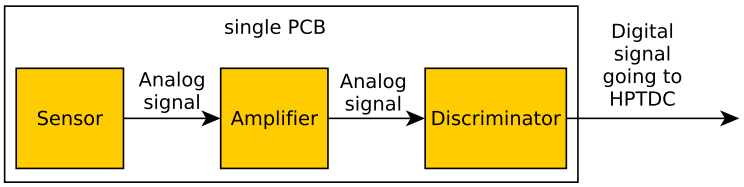

Figure 1: Block diagram of a detector channel. The former design of this part consisted of two boards; the first for the sensor and amplifier, the second for the discriminator.

2 The sensor

The most common solid-state sensors used in high-energy physics are made with silicon or diamond crystals. In particular, this work is based on Ultra Fast Silicon Detectors (UFSD), designed specifically for timing measurements. Thanks to a multiplication layer it is possible to have a thin sensor (fast charge collection) and to increase the output signal at the same time. The equivalent circuit of the sensor is shown in Fig. 2; the current generated at the passage of a Minimum Ionizing Particle (MIP) is on the order of tens of μA, the capacitance is usually few pF and the resistor is usually larger than hundreds of MΩ.

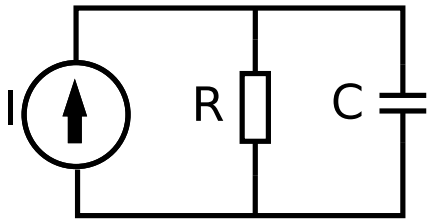

Figure 2: Equivalent model of an UFSD.

The signal generated by the sensor can be simulated using Weightfield2 [2] and is shown in figure 3.

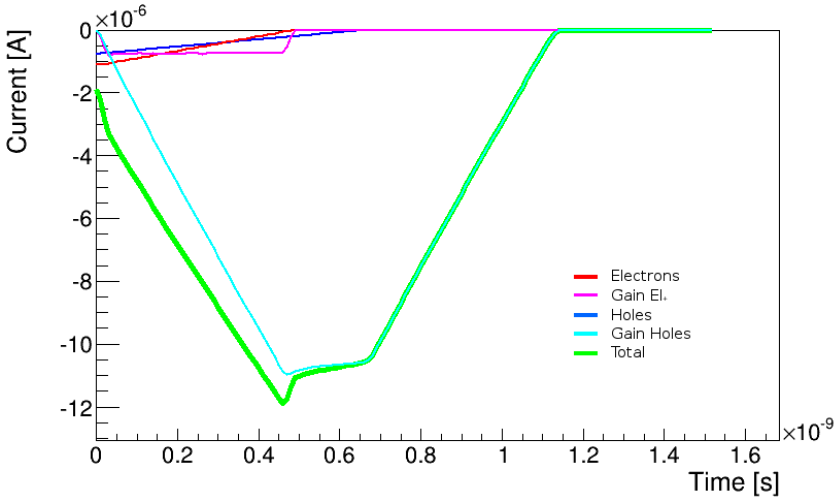

Figure 3: Current generated by the sensor simulated using Weightfield2.

The amplitude of the signal of the sensor depends on the energy released by the passage of the particle, and for UFSD, it also depends on the gain of the sensor. We used LTspice simulation software [3] to optimize the front-end electronics, configuring the current source to reproduce the signal generated by the sensor with different amplitudes, as shown in Fig. 4.

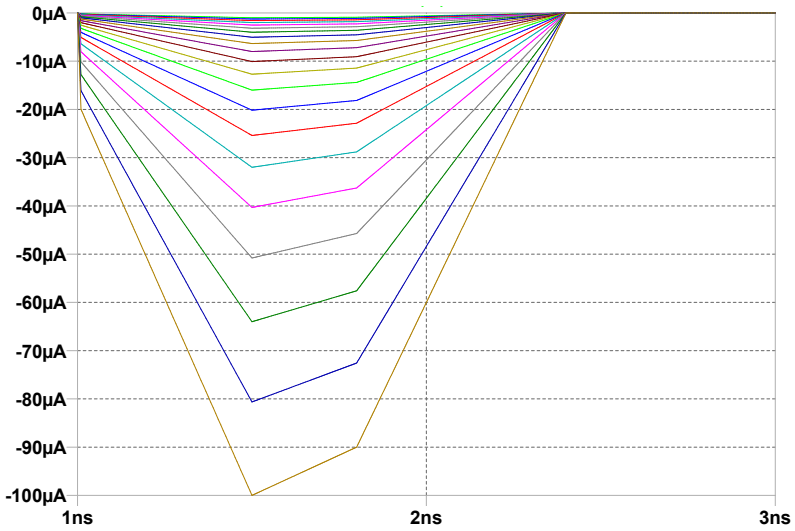

Figure 4: A signal with various amplitudes used to simulate the behavior of the electronics. This signal was used as input for the simulated amplifier.

3 Amplifier

The signal generated by the sensor has a low amplitude (tens of μA). Therefore, the signal needs to be amplified. The amplifier can be purchased as an integrated circuit; however, better performance can be obtained by designing a custom one using discrete components. Creating a custom amplifier has the advantage to be optimized for a specific application. The amplifier cannot be created using operational amplifiers because of their low bandwidth. Therefore, the amplifier was designed using transistors and passive components. A commonly used design, based on bipolar SiGe transistors [4], is suitable for this application. The values of the passive components such as resistors and capacitors as well as the number of stages were optimized.

The amplifier developed for this project is inverting and its output can be used as the input for a discriminator. The amplifier was designed to have an output amplitude of several hundreds of mV, SNR larger than 10 and time precision below 50 ps together with a power consumption lower than 150 mW per channel.

The time precision σ_t was simulated and computed using equation 1.

$$\sigma_t = \frac{\sigma_v}{\frac{dV}{dt}} \tag{1}$$

where σ_v is the RMS noise and dV/dt is the signal slope. More details on precise timing measurements are available in [5, Chapter 6.3].

The final design of the amplifier has a transimpedance gain V_{out}/I_{in} around 33000 and, in combination with a UFSD, can achieve an SNR higher than 100 and a time precision below 30 ps [6]. The simulated power consumption of a single channel is around 100 mW.

The output for different amplitudes of the input signal is shown in Fig. 5.

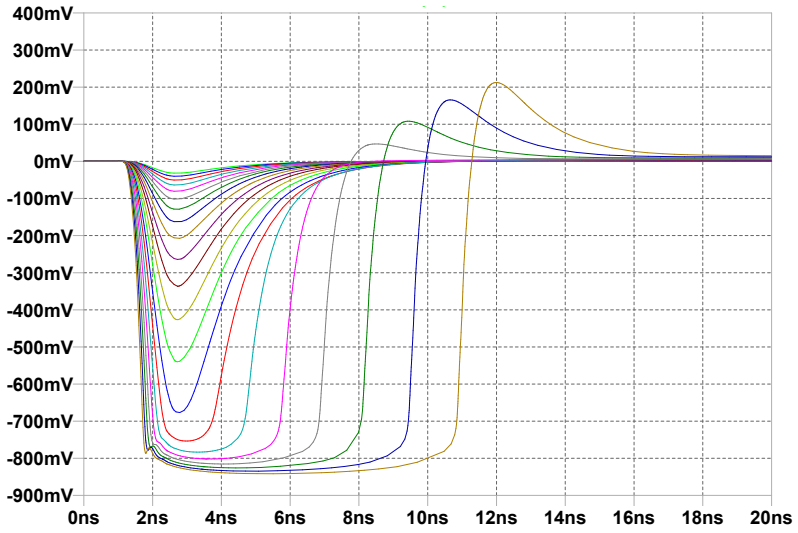

Figure 5: The output signal of the amplifier for various amplitudes of the input signal.

4 Discriminator

To use a Time to Digital Converter (TDC), the analog output of the amplifier needs to be discriminated. The solution presently implemented in CT-PPS uses a NINO chip on a dedicated board as a discriminator. In this work, we propose a fast, low power and low jitter discriminator that can be integrated on the same board as the amplifier, using commercially available components. This idea was also used in the PaDiWa board [7].

In particular, we looked for fast LVDS buffers produced by Texas Instruments and Linear Technology. However, Texas Instruments does not provide simulation models of their LVDS buffers, and components from Linear Technology are not fast enough. Despite that, we simulated the LTC6754 input comparator with LVDS compatible outputs to find out if the LVDS buffer will be usable as a discriminator. The positive input of the LTC6754 was connected to the amplifier's output shown in Fig. 5. The negative input was at a stable voltage of -0.1 V and served as the threshold voltage for the discriminator. The output signal of the LTC6754 is shown in Fig. 6 and it is a digital signal meeting the requirements in a frequency range limited by the LVDS buffer.

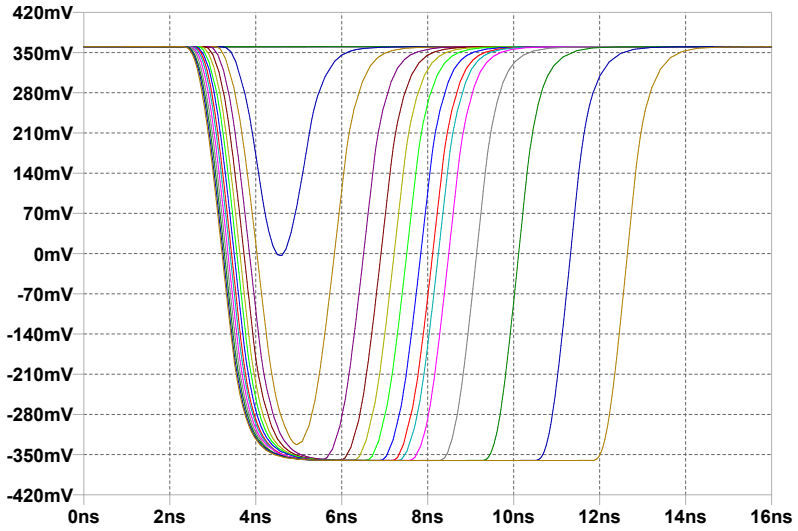

Figure 6: Simulated output of the LTC6754 LVDS buffer for different amplitudes of the input signal.

5 Experimental measurements

An experimental proof of concept was done using the LVDS inputs of an FPGA. In particular, we used a SmartFusion2 Advanced Development Kit from Microsemi Corporation. The maximum speed achievable for the LVDS buffer is 500 MHz for differential output and around 100 MHz for single-ended output. Using a signal generator, we proved that the LVDS buffer could be used as a fast discriminator with an adjustable absolute threshold down to 100 mV.

Measurements of arrival time with signals of different amplitudes are affected by a time walk [5]. This effect can be corrected by measuring the slope of the leading edge of the signal. Therefore, we used two buffers, as shown in Fig. 7, to discriminate the input signal at two different levels. The time difference between the output of the two discriminators depends on the slope.

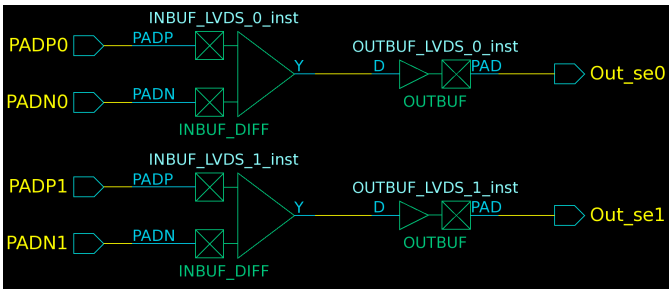

Figure 7: A graphical representation of the firmware implemented in the FPGA. The two different LVDS inputs are used to discriminate the input signal with two different thresholds to correct for the time walk.

The positive inputs of both LVDS buffers were connected to the signal generator. The length of the wires between the signal generator and the input pin had to be the same for both buffers to avoid different delays in the circuit. The negative inputs were connected to different DC voltage sources to set the thresholds. One of the thresholds was set slightly above the noise, while the second was set at a higher absolute voltage. The outputs of the two buffers were acquired with an oscilloscope, as shown in Fig. 8. We measured the dependence of the time difference between the output signals on the slope of the input signal, as shown in Fig. 9.

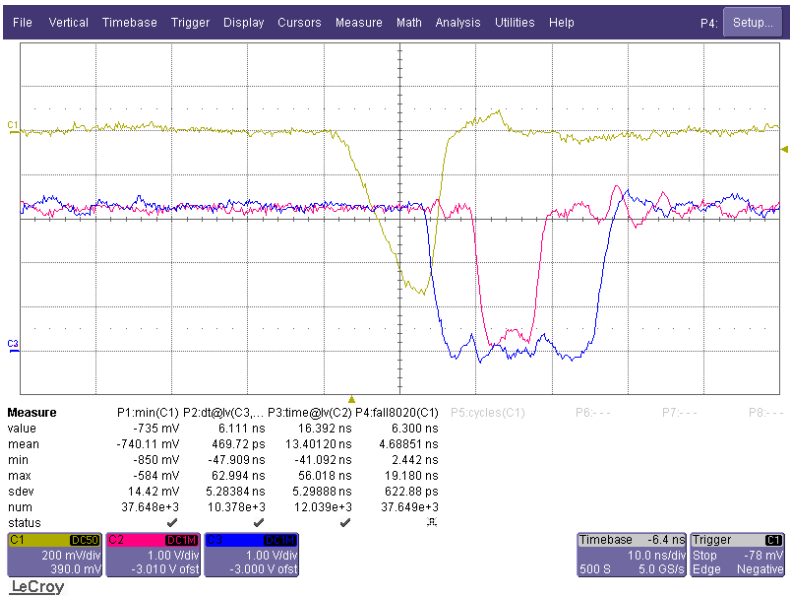

Figure 8: The input pulse is generated by a signal generator, and the two digital signals are the outputs of the discriminators with different thresholds. The blue signal corresponds to a threshold of 110 mV, the red signal to a threshold of 385 mV.

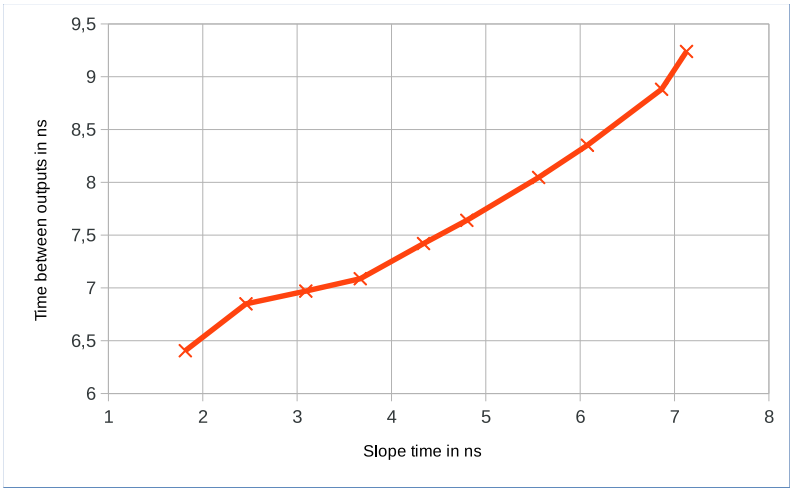

Figure 9: Dependence of the time difference between the output edges of the discriminators with a threshold of 106.7 mV and 419.2 mV on the input's slope.

A similar setup was tested using a Sr^{90} radioactive source, a UFSD and a read-out board, described in [6]. A picture of the setup is shown in Fig. 10. The output signal of this board was discriminated as described above; moreover, we used differential outputs of the buffers for their higher frequency. The LVDS buffers were producing fast digital signals dependent on the input pulse and the threshold. One measured sample is shown in Fig. 11.

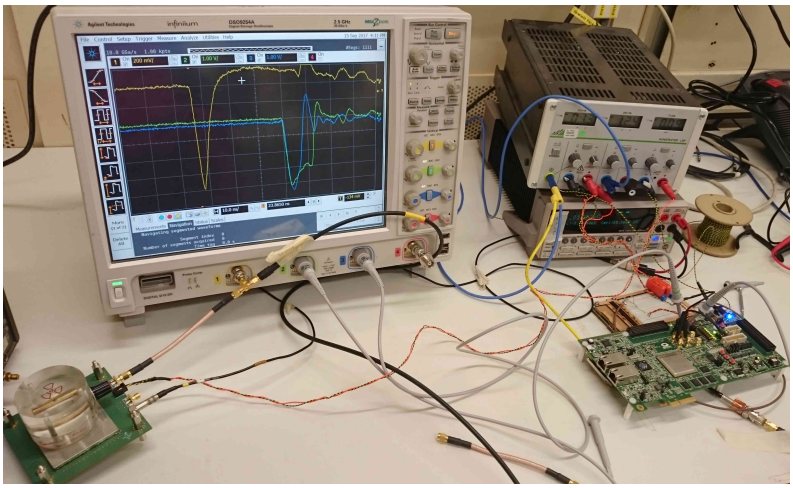

Figure 10: Picture of the experimental setup. The setup is using a Sr^{90} radioactive source, a UFSD with a read-out board and SmartFusion2 FPGA as the LVDS buffer.

We processed the acquired data using the ROOT data analysis framework. We removed the input signals shorter than 1 ns, caused by noise. As shown in Fig. 12, the Most Probable Value (MPV) of the amplitude distribution is not affected by this selection.

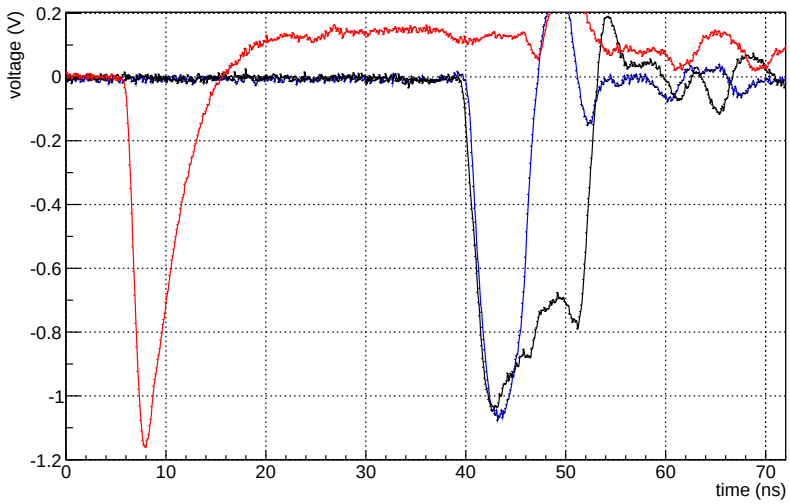

Figure 11: Example of the signal produced by the UFSD board and the digital output of the two discriminators. The black line corresponds to a threshold set to 189 mV, while the blue corresponds to a threshold set to 277 mV. We used differential outputs of the LVDS buffers for their higher frequency. However, the LVDS outputs of the discriminators were read out using single ended probes, therefore, some reflections due to the bad coupling are noticeable on the signals.

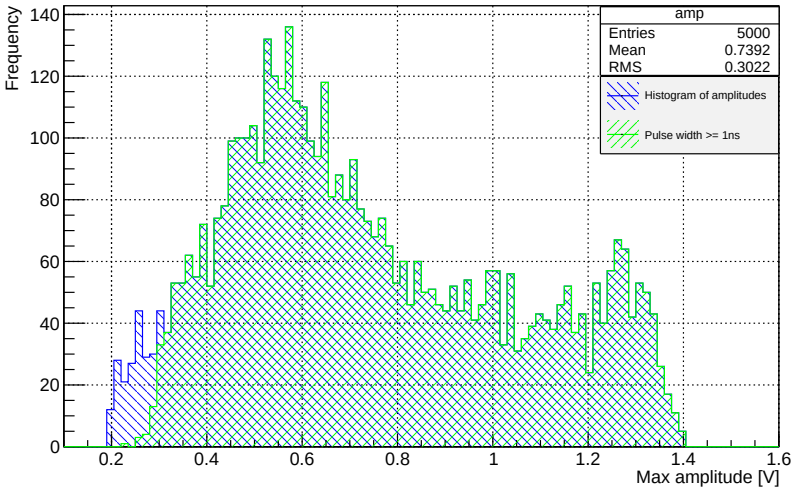

Figure 12: Histogram of the amplitudes of the input signals and the amplitudes of the pulses wider than 1 ns acquired during the tests.

We applied different software thresholds on the input signal to select pulses above a given threshold. We computed the efficiency of the discriminator using equation 2.

$$\eta = \frac{N_m \cdot 100}{N_c} \% \tag{2}$$

where N_m is number of discriminated pulses, N_c is number of pulses above the software threshold. The dependence between the efficiency and the threshold is in Fig. 13.

The lowest threshold for the experimental setup placed slightly above the noise was 189 mV, but the efficiency was below 80%. The discrimination efficiency at the 277 mV threshold was only slightly above 85%. The software threshold was 200 mV above the real threshold when the efficiency reached 100%. The difference between the real threshold and the software threshold may be due to using the

LVDS buffer as the discriminator. Therefore, for our setup with the SmartFusion2 FPGA we could discriminate signals with an efficiency of 100% for thresholds down to 500 mV.

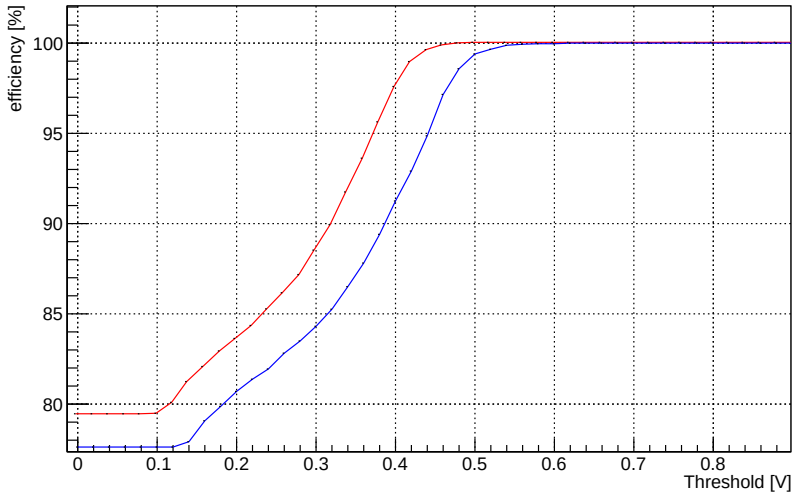

Figure 13: The efficiency of the discrimination at the different thresholds of the input signal. The red line represents the LVDS output with the threshold set to 277 mV, the blue line with the threshold set to 189 mV.

6 Conclusion

We proposed a new front-end electronics for timing detectors using solid state detectors. Present solutions, like the one implemented by the CT-PPS experiment, require an external digitizer (sampler or discriminator), while the proposed solution can be used to integrate a discriminator on the front-end board.

We described the sensor and simulated its behavior. With knowledge of the sensor's behavior, we designed an amplifier and investigated the usage of LVDS buffers as discriminators. The amplifier, made by bipolar SiGe transistors and passive components, was simulated with LTspice; its transimpedance gain V_{out}/I_{in} is around 33000 and the SNR expected for UFSDs is larger than 100, allowing a time precision below 30 ps. We used an LVDS buffer for the signal discrimination, moreover, using two identical buffers with two different thresholds it is possible to correct the time walk. The simulated power consumption of the final chain including the sensor, the amplifier and the discriminator was around 100 mW. To study the behavior of an LVDS buffer as a discriminator, we used the input drivers of an FPGA. We tested this discriminator with a pulse generator and, since the measurements worked as expected, we repeated the measurements using an existing board with a UFSD and an amplifier, exposed to a Sr^{90} source. In both cases, the LVDS driver was proven to be a good solution to discriminate analog signals with an amplitude of several hundreds of mV and with a pulse width down to 1 ns.

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References

[1] F. Anghinolfi, et al. "NINO, An ultra-fast, low-power, front-end amplifier discriminator for the Time-Of-Flight detector in ALICE experiment," *Nuclear Science Symposium Conference Record, IEEE.* Vol. 1, pp. 375–379, IEEE, 2003.

[2] F. Cenna, N. Cartiglia et al., "Weightfield2: A fast simulator for silicon and diamond solid state detector," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment,* 2015.

[3] LTspice: a high performance SPICE simulator. `http://www.linear.com/designtools/software/#LTspice`

[4] Nicola Minafra. "Development of a timing detector for the TOTEM experiment at the LHC", *Eur. Phys. J. Plus (2017)* 132: 402DOI: 10.1140/epjp/i2017-11707-2.

[5] Nicola Minafra. "Development of a timing detector for the TOTEM experiment at the LHC," PhD thesis, Bari, University of Bari A. Moro, Feb 2016. Presented 14 Mar 2016. `http://cds.cern.ch/record/2139815`

[6] N. Minafra, et al. "Test of Ultra Fast Silicon Detectors for Picosecond Time Measurements with a New Multipurpose Read-Out Board," *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment.* 2017.

[7] Neiser, A., et al. "TRB3: a 264 channel high precision TDC platform and its applications." *Journal of Instrumentation* 8.12 (2013): C12043.