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Noise Characterization of Silicon Strip Detectors

Comparison of Sensors with and without Integrated JFET Source-Follower

Settore scientifico-disciplinare:
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Dottorando
Gabriele Giacomini

Coordinatore del collegio docenti:
prof. Gaetano Senatore

Tutore e Relatore:
prof. Luciano Bosisio

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Riassunto

Il rumore è spesso il principale fattore che limita le prestazioni di un sistema di rivelazione. In questo lavoro si riporta un dettagliato studio dei contributi di rumore in diversi tipi di sensori al silicio a microstriscia.

Si sono investigati sia sensori con lettura a doppia faccia, fabbricati da tre differenti fornitori per l'esperimento ALICE presso lo LHC del CERN, sia rivelatori che includono, come primo stadio di condizionamento del segnale, un "Source-Follower" a JFET, integrato sullo stesso substrato del sensore. Questi ultimi sono stati progettati nel tentativo di migliorare le prestazioni del sistema quando sono richieste strisce molto lunghe, ottenute concatenando insieme vari sensori.

Dopo una descrizione dei sensori a microstriscia utilizzati, vengono illustrate e interpretate le misure di caratterizzazione statica eseguite su di essi (corrente e capacità verso tensione e/o frequenza). Come aiuto nell'interpretazione di alcune peculiari caratteristiche di queste misure si è fatto ricorso a simulazioni numeriche del dispositivo.

Sono poi descritti i modelli comunemente usati per esprimere il rumore del sistema rivelatore-amplificatore in funzione dei parametri che lo caratterizzano. Sono state considerate e confrontate due configurazioni del primo stadio di trattamento del segnale: il tradizionale amplificatore di carica e l'inseguitore di "source".

Segue la descrizione delle misure di rumore eseguite e dei relativi risultati. Sono state misurate curve della carica equivalente di rumore in ingresso, in funzione del tempo di picco del formatore, per diversi valori della corrente di buio. Quest'ultima è stata variata per fotogenerazione (illuminando il sensore con un LED) o, in alternativa, iniettandola direttamente nella striscia sotto esame per mezzo di una sorgente esterna di corrente (attraverso una resistenza di alto valore).
In tal modo è stato possibile verificare i modelli per il rumore su un ampio intervallo dei parametri, ed evidenziare chiaramente il contributo di rumore del meccanismo di punch-through, utilizzato per polarizzare le strisce.

Il rumore misurato con lettura del segnale tramite amplificatore di carica è generalmente in buon accordo con il modello comunemente usato, ma in qualche condizione operativa si sono trovati contributi inaspettati. Questi sono stati interpretati correlandoli con alcune caratteristiche particolari delle misure di capacità. Il rumore misurato sui rivelatori con Source-Follower integrato è in accordo con le predizioni del modello, quando per i parametri si usano i valori misurati.

Infine si confrontano le prestazioni dei due differenti approcci per la lettura del segnale.

Abstract

Noise is often the main factor limiting the performance of detector systems. In this work a detailed study of the noise contributions in different types of silicon microstrip sensors is carried on. We investigate three sensors with double-sided readout fabricated by different suppliers for the ALICE experiment at the CERN LHC, in addition to detectors including an integrated JFET Source-Follower as a first signal conditioning stage. The latter have been designed as an attempt at improving the performance when very long strips, obtained by gangling together several sensors, are required. After a description of the strip sensors and of their operation, the "static" characterization measurements performed on them (current and capacitance versus voltage and/or frequency) are illustrated and interpreted. Numerical device simulation has been employed as an aid in interpreting some of the measurement results. The commonly used models for expressing the noise of the detector-amplifier system in terms of its relevant parameters are then presented. Two configurations of the first signal processing stage are considered and confronted: the usual charge-sensitive amplifier and the Source-Follower. Next, the noise measurements performed and their results are illustrated. Curves of the equivalent input noise charge versus shaping time of the filtering amplifier, for several values of the leakage current, have been obtained. The leakage current has been varied by photogeneration, illuminating the sensor with a LED, or alternatively by injecting it into the strip from an external current source, through a high-value resistor. The noise measured with the strip sensors read-out by a charge-sensitive amplifier generally agrees well with the common model, but in some operating conditions unexpected contributions have been found. These have been interpreted by correlating them with some peculiar features of the capacitance-voltage measurements. The noise measured on the detectors with integrated JFET source-follower complies with the prediction of the model, using the measured values of the relevant parameters. Finally, the performances of the two different approaches are confronted.

Introduction

Since the pioneering work of Josef Kemmer on the fabrication of silicon detectors with the planar process [1], much progress has been made. Advancements in both detector and IC technologies opened the way to a varied array of silicon sensors, for many applications, in both science and industry. The power, flexibility and reliability of the technology allowed the introduction of various new kinds of detectors.

Among the first and most straightforward ones are strip detectors, in which the junction electrodes are shaped as long, narrow, parallel strips, allowing to determine with high spatial accuracy the coordinate orthogonal to the strip of the impact point of a detected particle.

Strip detectors have become a fundamental part of the inner tracking system of most high energy physics experiments. Because of their geometry, they cannot determine completely the position of the ionizing event, lacking information about the coordinate parallel to the strip. So, a signal from a further sensors, e.g. with strips at a different angle, is needed for a complete position determination. Anyway, they allow high spatial resolution, with a reduced number of read-out channels, compared with real 3D tracking devices as pixels. Strip detectors are commonly read out by Charge Sensitive Amplifiers (CSA), integrated into custom VLSI chips together with further amplification, shaping and a variety of other optional functions such as analog sample and hold with multiplexed read-out, ADC conversion, triggering, and more.

These chips are usually not commercial but are designed by the experiment team and fabricated by a foundry. The read-out chip is mounted as close as possible to the strips, in order to minimize stray connection capacitance. Every channel of the chip is bonded to a strip.

The advantage of the CSA configuration is that, as will be explained, the signal is independent on the parameters of the detector; it depends only on the well defined feedback capacitance. The detector capacitance, strip series resistance and leakage current affect only the level of noise.

For long strips, with a large capacitance, the option could be considered of subdividing the strip into shorter ones, individually connected to a simple first signal processing stage, integrated on the detector itself. Then, by means of thin cables, the signal is brought outside the tracking region, for further processing. An integrated Source Follower is a natural choice for this approach, since it has low output impedance, able to drive high capacitive loads, as presented by the long connections to the outer stages. A suitable fabrication technology had been developed at ITC-irst [1] (Trento) for the integration of n-channel JFETs on high resistivity silicon substrates, together with p-i-n detectors. The good static and dynamic characteristics of these JFETs had been demonstrated, but their suitability for the read-out of strip detectors had not yet been investigated.

One aim of this thesis, then, is to verify this point and, in particular, if it could give better noise performances with respect to a standard CSA read-out.

In chapter 1, the static characterization of the devices used throughout this work is presented. Two kind of strip detectors are considered: those designed for the ITS (Inner Tracking System) of the ALICE experiment at CERN and strips with

[1] Now, "FBK - irst".

integrated Source-Follower, developed under a "PRIN 2003" project. In the INFN-Trieste laboratory, the characterization and the quality acceptance tests of all microstrip detectors for the ALICE experiment have been made. On similar devices, we performed some additional tests; in particular, capacitance measurements opened the way to interpreting some peculiar features of the noise measurements. On detectors with SF, a characterization of the JFETs, constituting the source-follower stage, determined their parameters to be used in noise considerations.
In chapter 2, the noise as a physical quantity is introduced and the basic ideas of signal processing and noise analysis are presented for both the CSA and the SF configurations. Making some approximations, we derived the conditions for determining when one configuration is expected to be better than the other.
In chapter 3, the experimental set-up is described. The characteristics of the commercial single channel preamplification and filtering-shaping chain are presented, followed by the methods employed to generate signals with a conveniently high rate, as needed for an efficient noise determination.
Chapter 4 deals with noise measurements with the CSA read-out configuration. In order to fully characterize the signal processing, measurements with a simple diode detector have been made first. The measurements are based on noise scans versus peaking time, facilitated by the fact that the digital shaper allows selecting the shaping parameters within a wide range. Leakage and punch-through currents are varied too, checking their noise contributions. The same measurements are then performed on the strip detector, employing different methods for the polarization of the strips and investigating both sides of the detector (p and n strips). On these devices, the dependence on the bias voltage has been studied, leading to some unexpected results. These effects have been related to some features of the capacitance measurements described in chapter 1. A comparison with excess noise terms, found but not explained by other groups, is carried on.
Chapter 5 reports the noise scans made on structures with integrated SF. For these devices our set-up was not suitable to process the signals in an optimal way; however, we derived analytical expressions for both the signal and the noise under these conditions. As a result, signal and noise are discussed separately while the ENC, used in the CSA case, is not taken into account, since it does not give additional information. First pixels (devices with very extremely small area) and then strips are studied. A comparison with the theory discussed in chapter 2 is made.
Finally, in chapter 6, the experimental data are commented in the light of the theoretical expectations described in chapter 2, to answer the question that started our investigation:

SF or CSA?

Chapter 1

Static Characterization of Silicon Microstrip Detectors

1.1 ALICE Microstrip Sensors

The ALICE experiment at the Large Hadron Collider at CERN is designed for the detection of events generated by heavy ion collisions. In order to cope with the very high multiplicity of these events, the inner part of the tracking system is composed of six layers of silicon detectors with finely subdivided readout [2] [3]. The two outer layers, placed at average radii of 39 and 44 cm, are made up of strip detectors.

Given the low interaction rate during ion beam operation of the LHC and the relatively large radius of the strip layers, the expected radiation levels for 10 years of operation are very modest: a dose of 40 Gy and a hadron fluence of $4 \cdot 10^{11}$ cm^{-2} [3]. Such values do not pose demanding requirements on the radiation tolerance of the microstrip sensors.

The need for minimizing the material thickness forced the choice of double-sided sensors, while integrated AC-coupling capacitors are required for reliable operation of the detector system and simplification of the assembly process. The high expected track density (about 1 cm^{-2}) led to the adoption of a small-angle stereo geometry for the strips on opposite sides of the sensor, in order to limit the occurrence of ambiguities in track reconstruction.

The two strip layers are composed of 1698 sensors of a single type, for a total sensitive area of $\sim$5 m^2. The sensors have been provided by three different suppliers:

- Canberra Semiconductor NV, Lammerdries 25, B-2250 Olen, Belgium
- ITC-irst (now FBK-irst), Via Sommarive 18, I-38050 Trento, Italy
- SINTEF Electronics and Cybernetics, Blindern, N-0314 Oslo, Norway

All measurements reported in this work concerning the ALICE microstrip detectors have been performed on four test detectors (identical to the main ones except for a reduced number of strips, as described in Section 1.1.1). These will be referred to by the following abbreviations:

- AI , indicating a test sensor fabricated by ITC-irst.

- AE , indicating a test sensor fabricated by Canberra.

- AS1,AS2 indicating two test sensors fabricated by SINTEF. Of these, AS2 has been irradiated with low energy X-rays (20 keV), illuminating the p-side, to a dose of $\sim$130 Gy, to the purpose of increasing the positive oxide charge and prevent inversion of the interface [4].

1.1.1 Sensor Design and Specifications

The sensor has an overall size of 75 mm $\times$ 42 mm and a standard thickness of 300 μm [5]. The chosen stereo angle of 35 mrad between the two sides results from p-side strips forming an angle of +7.5 mrad with the short edge of the sensor and n-side strips forming a corresponding angle of -27.5 mrad.

The strips are about 40 mm long and placed at a pitch of 95 μm. At each end of a strip there are two bonding/probing pads on the upper (metal) electrode of the integrated capacitor ("AC pads"), and one smaller probing pad ("DC pad") connected to the lower electrode (implanted or diffused strip in the silicon substrate). The AC pad layout has reflection symmetry about the two detector axes and is identical on p and n sides, thus simplifying both testing and assembly.

On p-side, the strips are biased by punch-through from a surrounding bias ring [6] [7] [8]. Confronted with polysilicon resistors, this method of biasing is simpler to implement (no need for additional processing) and does not take room on the sensor layout. Furthermore, it avoids the thermal noise associated with a bias resistor, although it brings its own specific noise contributions, which are discussed in Sections 4.3 and 4.4.2. The main drawback of punch-through biasing is limited radiation tolerance, but this is not a concern for the ALICE strip detectors, given the very modest radiation levels they are expected to face.
A similar scheme has been adopted on n-side, where the strips are biased by injection of electrons toward the bias ring, across a potential barrier created by the insulation structure (p-stop or p-spray, depending on the supplier's choice).
A microscope picture of a corner on the n-side of the AI sensor is shown in Figure 1.1.

Outside of the bias ring, a guard ring is present and, on p-side, a number of floating rings are implemented in order to control the peak electric fields. The guard ring design and the details of strip design at the silicon level are defined by the suppliers of the sensors.

On the wafer, alongside the main detector, there is ample space for test structures. In addition to the standard devices for measuring properties of the substrate material and parameters of the fabrication process, a test detector has been included.

The test sensor is identical to the main one in all details of both the strips and the edge regions (bias rings, guard rings, scribe lines), the only difference being a reduced number of strips: 128 instead of 768. As a consequence, the overall size of the sensor is reduced to 14.2 mm $\times$ 42 mm. The small-angle stereo geometry allows designing a smaller detector with the same strip length of the large one, on both sides.

Because of the identical design, all properties of the sensors can be investigated on the test detectors, with obvious advantages in terms of availability (they are not needed for installation in the ALICE tracker) and a more compact size, facilitating

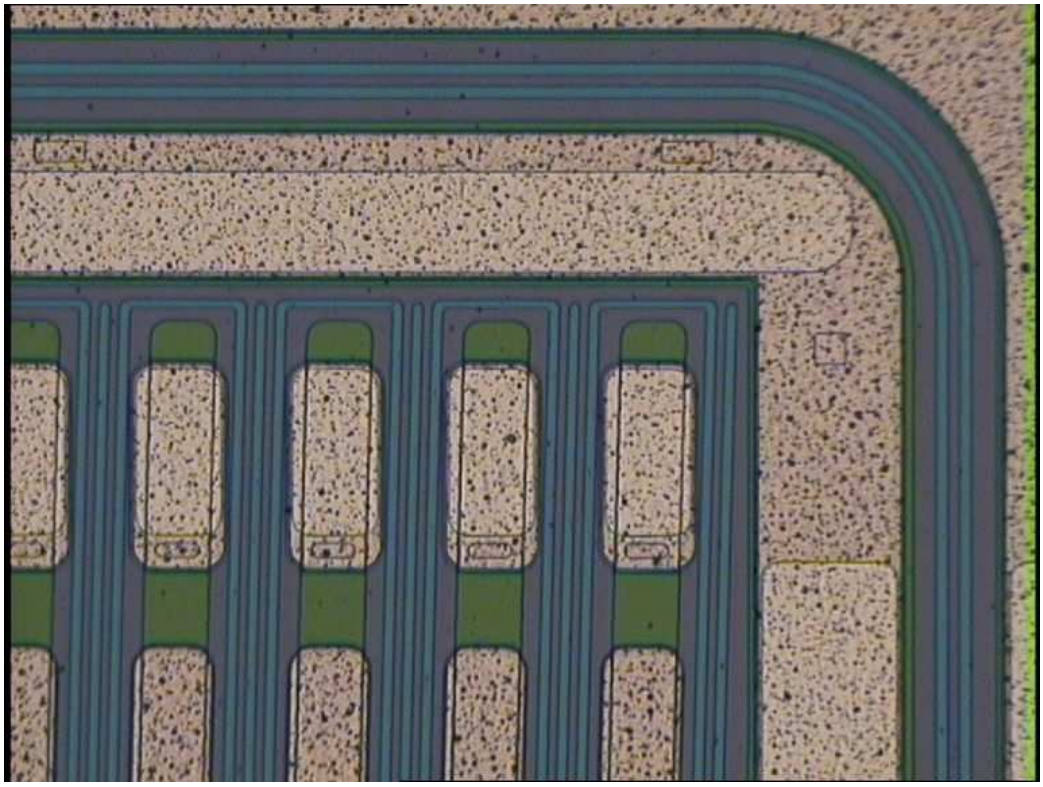

Figure 1.1: Microscope picture of a corner on the n-side of the AI sensor. The p-stop implants surrounding the n-type strips are clearly visible.

assembly and bonding.

According to the electrical specifications, a strip is classified as defective if either of the following happens [5]:

- the leakage current of the DC strip exceeds 20 nA;
- the effective insulation resistance of the DC strip is below 50 MΩ;
- the AC capacitor is broken;
- the metal AC strip is shorted to adjacent ones or to bias ring ("metal short");
- the metal AC strip is interrupted ("metal open").

The acceptance criterion requires the total number of defective strips on the two sides of a sensor to be less than 30, corresponding to about 2% of all strips.
The sensor must also comply with specifications on the maximum detector operating voltage, maximum total current and on the current stability in time. In addition, there are specifications on the values of the interstrip capacitance, the AC coupling capacitance, the metal strip resistance, the punch-through voltage drop and the differential punch-through resistance. These parameters are tested only on a sampling basis [5], since they are not related to random defects, but rather to design and processing aspects.

1.1.2 Acceptance Testing of Sensors

The acceptance testing and quality control of the microstrip sensors for the ALICE Inner Tracking System has been performed at the Trieste INFN laboratory.

A detailed description of the testing procedures adopted can be found in [5] and a summary of test results is given in [9]. Here we only recall the main steps of the routine acceptance test, performed on every sensor.
The n-side of the sensor is tested first, with the following sequence:

1) *AC Strip Scan*: Every strip capacitor is measured sequentially, with 20 V bias applied across it. Capacitance, dissipation factor and leakage current are measured simultaneously.

2) *I-V Measurement*: The currents of bias and guard rings on p-side (back-side) are measured, together with the current of one n-side strip, with the bias voltage reaching up to 100 V. The strip I-V characteristic allows a quick estimate of the insulation bias voltage, since parasitic currents due to instrument offset voltages dominate the measured strip current until good strip insulation is reached.

3) *Punch-Through Voltage Measurement*: The punch-through voltage drop between bias ring and strip is measured versus bias voltage, for two different strips.

4) *DC Strip Scan*: Leakage current and insulation resistance of every strip are measured.

Tests 1), 3) and 4) are then repeated on p-side (there is no need to redo the I-V measurement). The time required for the complete characterization of one (full-size) sensor is normally about two hours.

In the following we will be concerned only with measurements made on the four test sensors mentioned above, to the purpose of characterizing their properties in view of the noise measurements.
First, good quality sensors have been selected by performing the standard acceptance measurements.
The AI detector showed a low depletion voltage[1] of $\sim$15 V. The AE detector showed an even lower depletion voltage of just $\sim$8 V, while the AS detectors have higher depletion voltages, around 40 V.

After cutting from the wafer, the sensors have been glued upon fiberglass supports and bonded on both sides to gold-plated copper traces.
The assembly provides external access to:

- on each side, the bias ring and the guard ring;

- one (centrally located)strip per side; bonding provides independent access to its DC and AC pads;

- on each side, the AC pads of all the other strips, bonded together to a common line.

[1] the "depletion voltage" is defined here as the minimum bias voltage at which every n-side strip is insulated from the others, with an effective interstrip resistance exceeding 100 MΩ.

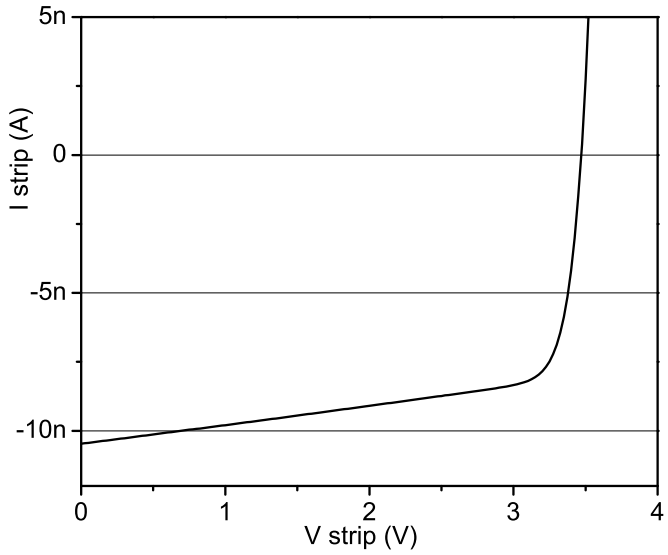

Figure 1.2: Punch-through I-V characteristic: while all others strips sit at their punch-trough voltage, the voltage of the single bonded strip is varied. Above a certain threshold ($\sim$3 V in this figure) a nearly exponential punch-through current starts flowing from the strip to the bias ring.

We describe in the following subsections a few additional measurements, not routinely made on the ALICE sensors, with particular attention to capacitance measurements, which are important for interpreting the noise data.

1.1.3 Punch-Through I-V Characteristic

During the standard acceptance tests, the punch-through voltage of a few sample strips has been measured versus the detector bias voltage. This measurement is performed by contacting the DC pad of the strip and reading out the voltage with a very high impedance "voltmeter" (an SMU channel of the HP4156A set in current-mode, at zero current).

To get more insight on the punch-through mechanism we can measure its I-V characteristic, for a given value of the bias voltage. This is done by varying the voltage applied to the DC pad of the strip, and measuring the current flowing into the DC pad itself from the external instrument (SMU channel in voltage-mode: forces voltage, measures current). The punch-through current, flowing from the strip to the bias ring, is then the sum of the leakage current with the externally measured current.

Figure 1.2 shows an example of such a measurement, for a p-side strip of sensor AS2 (the leakage current is higher than normal because of the surface generation caused by the X-ray irradiation). When the strip is at 0 V (the same voltage as the bias ring), it collects more than its "fair" share of leakage current, since the adjacent strips are at punch-through voltage (a few volt positive); this causes a deformation of the electric field in the silicon, with more field lines reaching the

strip, which then collects also a fraction of the leakage current normally flowing to the neighbouring strips. No punch-through current flows between the strip and the bias ring, because they are at the same voltage, hence the leakage current flows to the external instrument (reading a negative current because of the sign convention).
When a positive voltage is applied to the strip, the voltage difference with the adjacent ones is reduced, and the collected leakage current decreases (in absolute value): this is shown by the (almost linear) slope of the first part of the plot.
Finally, when the strip voltage becomes large enough to cause a significant punch-through current to the bias ring ($\sim$3 V in this case), the current measured by the instrument quickly goes to zero (the condition in which all the strip leakage current flows by punch-through), then reverses sign and grows with an approximately exponential dependence on the strip voltage.
At "large" current values (depending on geometry and substrate doping, about 10 nA are enough in this case) the punch-through current significantly deviates from the exponential behaviour, to become space-charge limited when the carrier density in the punch-through region becomes comparable with the substrate dopant density. The current then exhibits a power-law dependence on voltage [7] [10].

If one needs an accurate measure of the strip leakage current in its "normal" operating conditions (when it is biased by punch-through), the best procedure would be to extrapolate the linear part of the plot in Figure 1.2 to the punch-through voltage (the voltage at which zero current is measured).

1.1.4 Capacitance measurements

The only capacitances routinely measured on ALICE strip detectors are those of the integrated AC coupling capacitors, made up of a thin layer of SiO_2 between the implant and the metal. On a sampling basis, interstrip capacitances to first and second neighbors have also been measured [5]. For this work, a few more detailed measurements have been performed, taking advantage of the wire-bonded connections to the strips and bias ring on both sides of the sensors. In the following we illustrate, among these measurements, those that are most relevant for the interpretation of the noise characteristics of the sensors. The equipment and the procedures used for capacitance measurements are briefly described in Appendix A.

In the measurements, connections to the strip are made to the AC pads (i.e. to the metal strips) rather than the DC ones (i.e. to the implanted strips). On the one hand, the capacitances to be measured are at most on the order of 10 pF per strip, at least an order of magnitude less than the coupling capacitance, so that the difference in the measurement results introduced by adding the coupling capacitance in series is small. More importantly, it is actually the capacitances measured on AC pads that affect the performance characteristics of the detector readout (such as noise), because the front-end electronics is connected to the AC pads.

One of the most important detector parameters entering in noise calculations is the total capacitance between the charge collecting electrode (e.g. a strip) and all other electrodes that are kept at fixed voltage, i.e. at ground for what concerns the signal [11]. This can be measured, for example, by feeding the sinusoidal small-signal voltage v_{AC} (see Appendix A) to all the other electrodes and measuring the

induced AC current on the strip under study. It is instructive, however, to consider separately the various capacitances between the strip and the other electrodes.

Unless otherwise stated, the capacitance-voltage measurements (C-V characteristics) reported in the following are performed at 200 kHz frequency. This approximately corresponds to the shaping times (a few μs) used in the noise measurements; furthermore, the measured values do not significantly depend on frequency in a large interval around this point. Special features of the frequency-dependence of capacitance and dissipation factor are then investigated with measurements performed versus frequency (C-f characteristics), for different values of the bias voltage.

Consider first the capacitance between a strip and the opposite side (backside) of the sensor. Because the AC pads of all strips are wire bonded to just a few terminals, in our setup it is easy to measure the capacitance between all p-side strips and all n-side ones. Dividing the result by the number of strips we get a fairly accurate measurement of the capacitance between a single strip and all the others on the opposite side, i.e. the backside capacitance of a strip. Figure 1.3 reports the capacitance between all the p-side and all the n-side strips, measured versus bias voltage, for sensor AS1. The backside capacitance is plotted as C^{-2} (as is common practice) because for one-dimensional one-sided junctions the slope of the $C^{-2} - V$ plot is inversely proportional to the doping concentration [12]; for a uniformly doped substrate we then get a linear increase until the total depletion voltage is reached and the curve flattens out. In our case we expect deviations from the simple linear plot, because of two reasons: first, the junction is composed of many strips, so the geometry is not one-dimensional, and in addition there are interface charges in the interstrip gaps, altering the electrostatics of the problem; second, the actual bias voltage between p-side and n-side strips differs from the applied voltage because of the (non constant) punch-through voltage drops on both sides. Nevertheless, we observe that the plot in Figure 1.3 is still approximately linear. From the knee of the curve we can estimate that total depletion of the substrate is reached at a voltage of 41 V applied between the two bias rings (this includes the punch-through voltage drops).

For strip pitches smaller than the substrate thickness, the major contribution to the total capacitance of a strip usually comes from the interstrip capacitance, which is dominated by the capacitance to first neighbours. With our set-up, we can easily measure the capacitance of one strip towards all other strips on the same side. Figure 1.4 shows the interstrip capacitance versus bias voltage, measured on sensor AS1. In order to measure only the interstrip capacitance, the bias ring and the backside must be kept at signal ground. The figure also shows the capacitance measured when the backside is made floating for the AC signal, which has been obtained by supplying the bias voltage through a 1 MΩ resistor. In this latter case, the backside (including the undepleted part of the substrate at low bias voltages) is coupled to the AC signal by the backside capacitance of the n-1 strips connected to the HIGH terminal; in turn the backside is coupled to the strip under measure by the backside capacitance of that strip. It follows that the backside almost exactly follows the v_{AC} signal, so that we measure the sum of the interstrip and the strip-to-back capacitance. As a consequence, the measured capacitance increases at low bias voltages, where the capacitance to backside becomes important. Conversely, when the backside is grounded for the signal, the capacitance decreases at low bias voltage, because of the partial screening of the interstrip capacitance by the

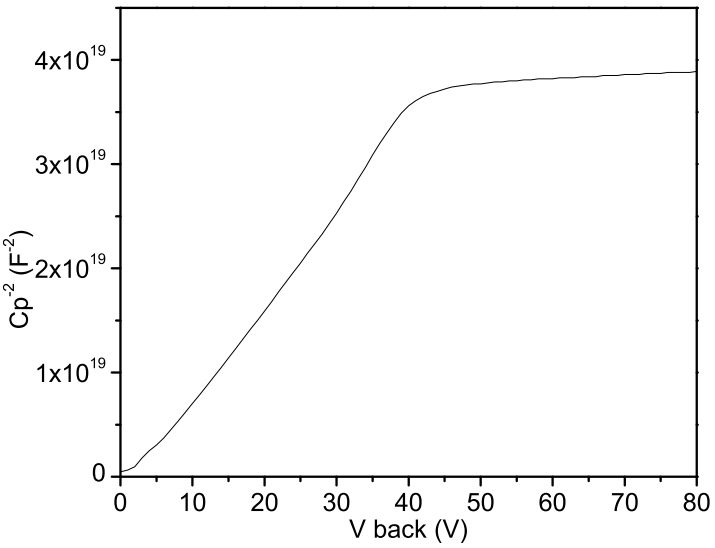

Figure 1.3: Detector AS1. Capacitance between all the p-side and all the n-side strips, measured as a function of the voltage applied between the two bias rings. The function C^{-2} is plotted.

undepleted bulk.

In order to measure the total capacitance of a (metal) strip towards all other electrodes, we connect the AC pad of a single strip to the LOW terminal, while the bias ring and the AC pads of all other strips on the same side are connected to the HIGH terminal. The bias ring and all AC pads on the opposite side are connected to HIGH through a large capacitor and to the bias voltage supply through a 1 MΩ resistor. Since the current flowing through the resistor is small (tens of nA), the corresponding voltage drop is negligible compared to the reverse bias voltage. In any case, it could be easily corrected for by measuring the bias supply current and subtracting the IR product from the applied voltage.
This configuration – with the metal strips at the same DC voltage of the corresponding bias ring, and the underlying implanted strips at their appropriate punch-through voltage – is the one applying during normal operation of the detector, when each strip is connected to a preamplifier, and the front-end electronics is floated at the detector bias voltage. An example of the measurement of this capacitance versus bias voltage is given in Figure 1.5, relative to an n-side strip of sensor AS1. The sharp increase of the measured capacitance and dissipation factor below 40 V reflects the fact that the n-side strips are not insulated below this voltage. Above the strip insulation voltage, the capacitance slowly decreases because of a slight lateral depletion of the electron accumulation channels present in between the p-stop implants that are used to insulate the strips.

The values of total strip capacitance and dissipation factor measured at 60 V bias for all four sensors are summarized in Table 1.1. The depletion voltages of the sensors are also indicated. The quoted C and D values refer to the particular strips (one per side on each sensor) that have been individually bonded to an

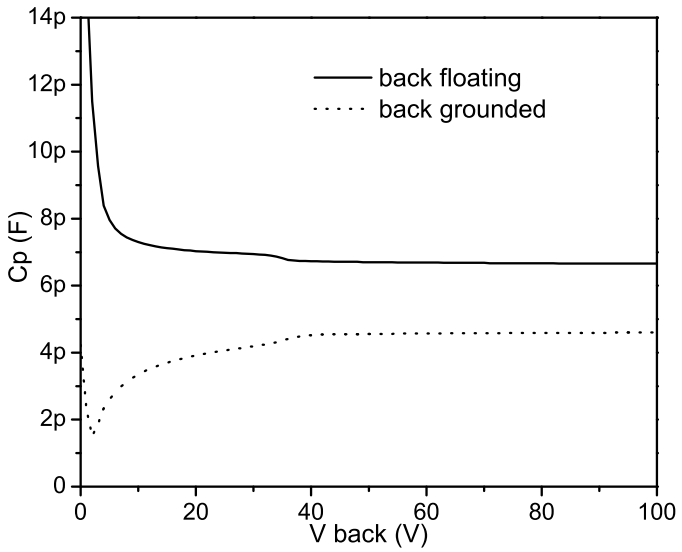

Figure 1.4: Detector AS1. Capacitance between one p-side AC strip and all the others ones, versus bias voltage. The figure shows curves obtained with the back-side grounded or floating for the AC signal. $f = 200$kHz

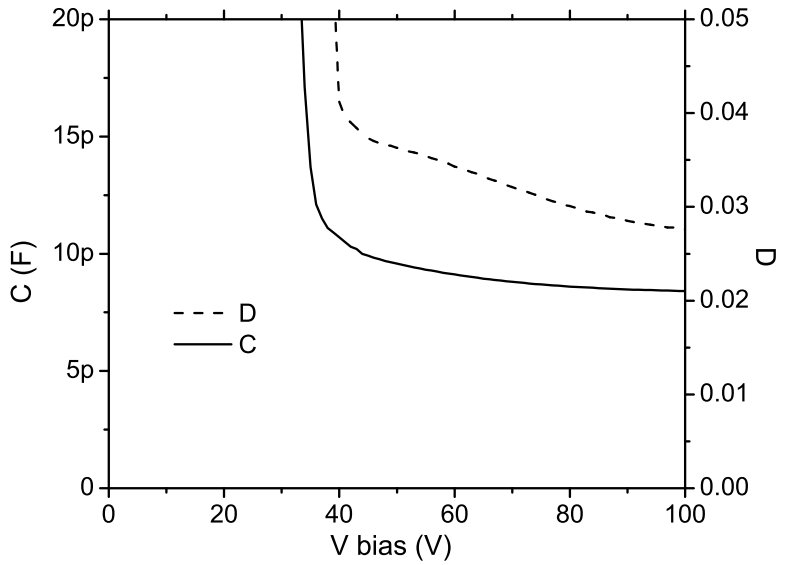

Figure 1.5: Total capacitance and dissipation factor for a single n-side strip of sensor AS1. It includes the capacitance toward the backside, the bias ring (negligible) and all others strips on the same side. $f = 200$ kHz

		Capacitance p-side (pF)	Capacitance n-side (pF)	$V_{\rm depl}$ (V)
CANBERRA	AE	10.2 (0.6 %)	12.2 (4.6 %)	8
ITC	AI	10.6 (0.6 %)	10.3 (1.0 %)	15
SINTEF	AS1	6.8 (0.7 %)	8.8 (3.4 %)	42
SINTEF irr.	AS2	6.8 (1.3 %)	8.3 (4.1 %)	40

Table 1.1: Total strip capacitance and dissipation factor (in parentheses) for the sensors studied, measured at 60 V bias and 200 kHz frequency. The depletion voltages of the sensors are also indicated. Sensor AS2 has been irradiated with 20 keV X-rays illuminating the p-side, at a dose of 130 Gy

external terminal. The same strips are used for the noise measurements, so that values reported can be appropriately used in models for noise analysis. However, the strip capacitance is subject to variations inside the same sensor and, to a larger extent, between sensors coming from different wafers and/or production lots. For this reason, when confronting different types of sensors the quoted capacitances can be taken as significant only with an uncertainty of 10%.
We observe that the n-side strips have larger capacitance than p-side ones, with the exception of the AI sensor, for which there is no difference. Furthermore, the irradiation with X-rays does not seem to have appreciably changed the capacitance of the AS sensors.

The dissipation factor is comfortably low ($< 5\%$), at least when depletion is reached, and this ensures that the capacitance is a well-determined parameter. In fact, the relative differences between the values obtained with series and parallel models are of order D^2.
However, the dependence of D on bias voltage, above total depletion, shows characteristic features, with some differences between the sensors studied. Figure 1.6 reports the measured D vs. V_{bias} curves of strips, for the AE and AI sensors (the ones with low depletion voltage).

On the n-side of detector AE the dissipation factor, after a very steep drop corresponding to the strip insulation voltage, remains almost constant at a relatively high value of 4.5%. The n-side of sensor AI shows a different pattern: after dropping sharply when the strip becomes insulated (16 V), D decreases gradually until, about 40 V above depletion, it suddenly changes to a constant value close to 1%.
On the p-side, there is no sharp drop in D at total depletion, since the p-strips are insulated from the n-type bulk at all bias voltages (the high value of D at very low bias, 0-1 V, is likely due to the large strip capacitance to the undepleted, highly resistive bulk). The p-side plot for the AE sensor shows a behavior similar to the n-side of the AI sensor: D smoothly decreases until it suddenly flattens at about 50 V bias. This characteristic of the dissipation factor is interesting because, in contrast to it, the capacitance (measured at the same frequency of 200 kHz) shows very little voltage dependence above total depletion.

These features, due to a resistive component of the admittance, are presumably related to surface effects, because after the substrate is depleted, changes in response to bias voltage variations can only take place in surface structures and layers. In fact, the backside capacitance measurements show constant dissipation

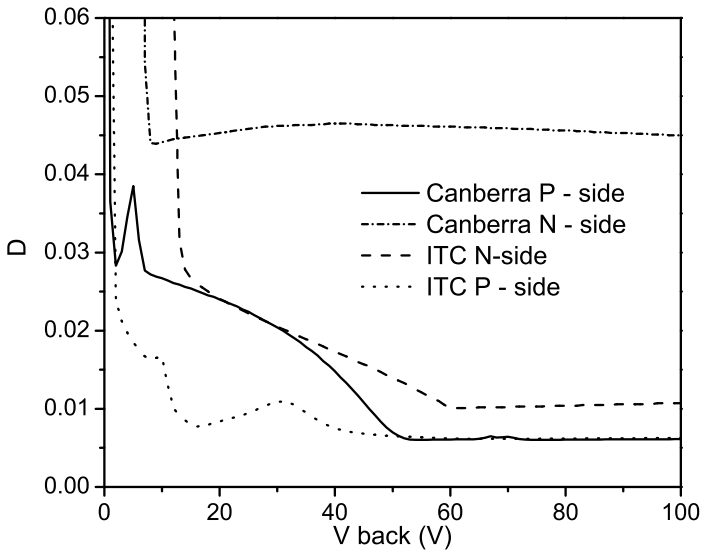

Figure 1.6: Dissipation factor versus bias voltage for p-side and n-side strips of sensors AE and AI. Notice the depletion voltage of the detector, clearly shown by the sharp fall of D for n-side strips. $f = 200$kHz

factors ($< 1\%$) above total depletion, practically independent on frequency.

In order to explain these features, the capacitance and dissipation factor have been studied in the frequency domain: a series of measurements versus frequency have been carried out, for different values of the bias voltage (above total depletion). The results of the measurements have been confronted with the predictions of a very simple model.
In the following subsections the situations for the sensors type AE and AI are considered separately.

AE-type sensor

At the surface of the AE detector, both on p and on n-side, the bias ring is separated from the strips and each strip from the others by a layer of opposite conductivity: on p-side an electron accumulation layer induced by the positive oxide charge and on n-side a p-spray layer, a low dose boron implant uniform across the wafer [13]. Then we expect the situation to be similar on the two sides. We verified that the measured interstrip capacitance is insensitive to whether or not the bias ring is connected to ground or to the HIGH terminal; this is true on both sides.

Consider measurements on n-side first, as reported in Figure 1.8. Looking at the curve for the dissipation factor D, we notice that a function of the type:

$$D \propto \frac{\omega\tau}{1 + (\omega\tau)^2} \tag{1.1}$$

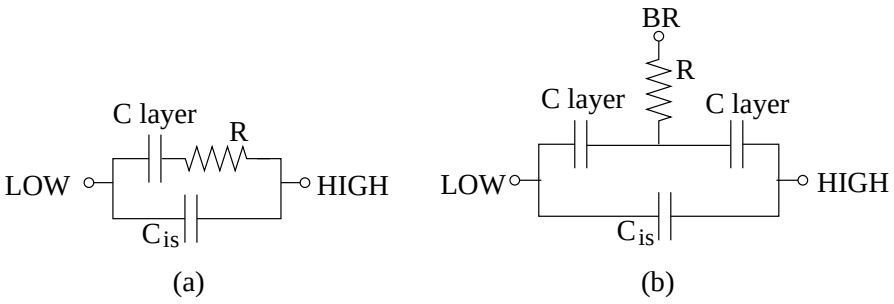

Figure 1.7: Simplified model of the interstrip impedance applying to: (a) AE sensor and p-side of AI sensor; (b) n-side of AI sensor.

with $\tau \sim (10\text{ kHz})^{-1}$, has a very similar frequency dependence.

An impedance made up by a capacitance in parallel with the series combination of a resistance and a capacitance, as shown in Figure 1.7(a), can account for this shape.

This schematic can be interpreted as follows: C_{is} is the "direct" interstrip capacitance (dominated by first neighbours, with a small contribution from other neighbours), C_{layer} is the capacitance of the strip versus the resistive layer (p-spray on n-side, electron accumulation channels on p-side) in series with the capacitance of this layer to all other strips, and R is the resistance of the resistive layer path linking the strip to all other strips. Obviously this is an extremely simplified model, with just three lumped elements replacing distributed capacitances and resistances in electrodes of complex geometry.

With some tedious calculations we obtain the values of D and $C_p = Im(Y)/\omega$ for the simple circuit of Figure 1.7(a):

$$D = \frac{Re(Y)}{Im(Y)} = \frac{\omega R(C_{layer} - C_{is} \oplus C_{layer})}{1 + (\omega R)^2 (C_{is} \oplus C_{layer}) C_{layer}} \tag{1.2}$$

$$C_p = \frac{Im(Y)}{\omega} = (C_{layer} + C_{is}) \frac{1 + (\omega R)^2 (C_{is} \oplus C_{layer}) C_{layer}}{1 + (\omega C_{layer} R)^2} \tag{1.3}$$

where the notation $C_{layer} \oplus C_{is}$ stands for the series combination of the two capacitances.

Consider now the p-side of sensor AE, where more interesting features appear.

The results of the model of Figure 1.7(a) are compared with the measured C-f and D-f curves in Figure 1.9. The values of C_{is} and C_{layer} (given in the caption) have been adjusted in order to reproduce the capacitance measured at low and high bias voltage in the low-frequency limit (when R can be neglected). Once this is done, the model can qualitatively reproduce the dependence of C and D on the bias voltage by varying the value of the layer resistance R. The flat C and D curves measured at high bias voltage (above $\sim$50 V) are obtained when $R \to \infty$ (indeed in Equations 1.2 and 1.3 C_p becomes independent of f and $D \to 0$ when $R \to \infty$). This is interpreted by assuming that the electron accumulation layer on p-side is interrupted at high bias voltage, suppressing the long-range capacitive coupling between strips. 3-D device simulations (Section 1.1.5) show that indeed in the narrow (6 μm) punch-through gap at the end of the strips the accumulation

layer is depleted due to the punch-through voltage difference between strips and bias ring, thus insulating the interstrip accumulation channels from each other. At lower bias voltages, when the accumulation layer is not interrupted, the low frequency capacitance shows the large contribution of the coupling C_{layer} to the resistive layer, while at high frequency this contribution is cut off by the series resistance R.

Going back to the n-side measurements (Figure 1.8), the fact that D is almost independent on the bias voltage can be related to the fact that the implanted p-spray layer, having a dopant density per unit surface much larger than the density of the accumulation electrons, is only marginally depleted at its edges, and never gets interrupted.

It can be seen that the model, despite its gross oversimplification of the real situation, is able to qualitatively reproduce the main features of the measurements.

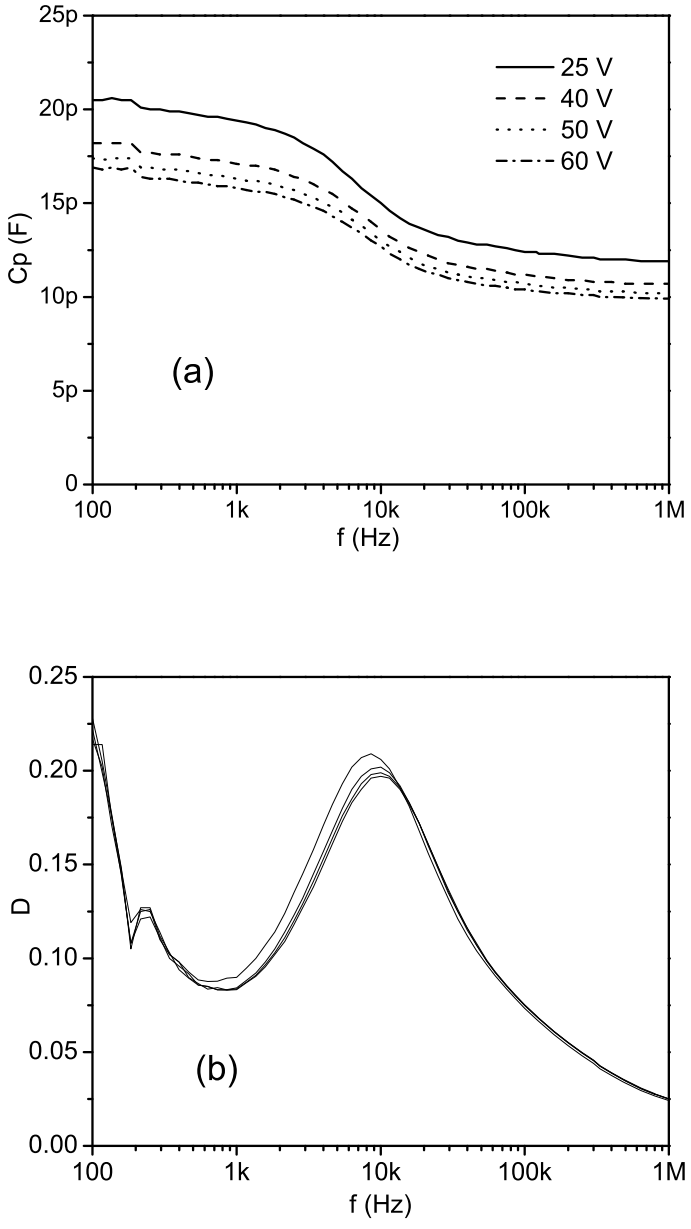

Figure 1.8: AE sensor, n-side. (a) Capacitance versus frequency of the single strip towards all other strips on the same side, for four values of the bias voltage (25, 40, 50 and 60 V). (b) Dissipation factor for the same measurement.

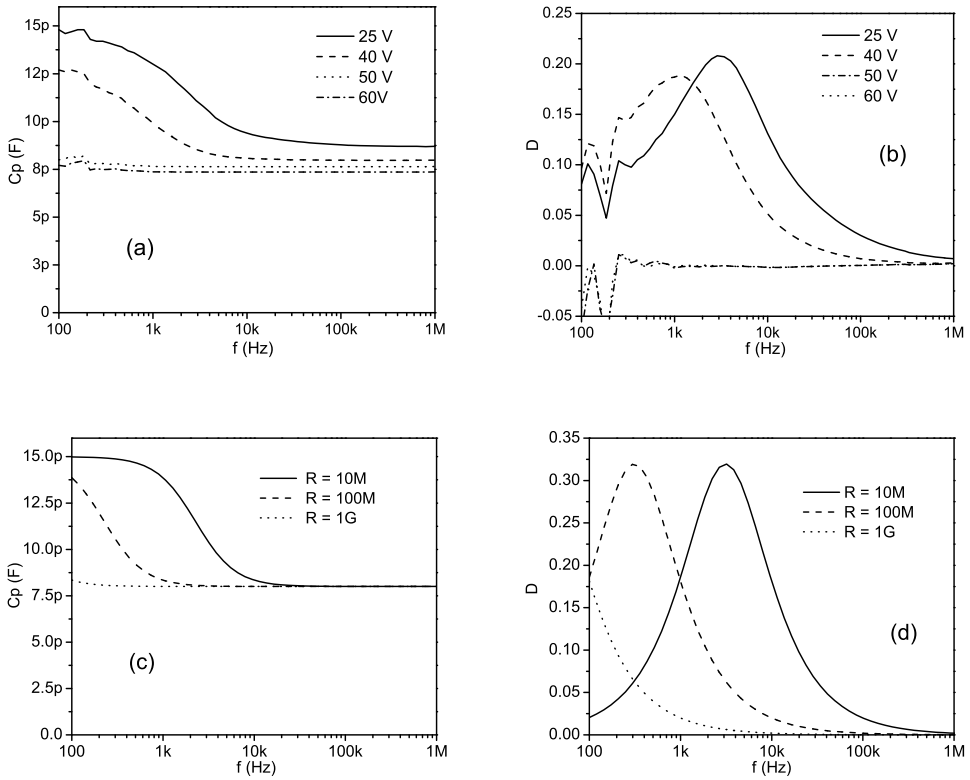

Figure 1.9: AE sensor, p-side. (a) Capacitance versus frequency of the single strip towards all other strips on the same side, for four values of the bias voltage (25, 40, 50 and 60 V). (b) Dissipation factor for the same measurement. (c) Capacitance calculated from the model of Figure 1.7a, with $C_{layer} = 7$ pF, $C_{is} = 8$ pF and three values of R (10 MΩ, 100 MΩ, 1 GΩ). (d) Dissipation factor calculated from the model, with the same parameter values.

AI-type sensor

On the p-side of the AI sensor (Figure 1.10), the capacitance is independent of frequency for every bias voltage applied, and the dissipation factor is always low ($< 1\%$). According to our previous model, this means that the accumulation channels in between the strips are not connected to each other at their ends, because the surface region between the bias ring and the strips is depleted even at the low bias of 25 V. This different situation with respect to the p-side of the AE sensor may be caused by the shorter punch-through gap (5 μm) and by a possibly smaller positive charge in the oxide.

On n-side, the strip insulation is obtained by surrounding the strips with a p-doped frame, called "p-stop". In addition, a p-stop strip is laid in between the p-stop frames, so that two adjacent n-side strips are separated by three p-stop implants (see Figure 1.1).
We can represent the situation actually occurring with the aid of the model in Figure 1.7(b), in which an electron accumulation layer between the p-stops is in *ohmic* contact with the n-type bias ring (in contrast to the previously discussed

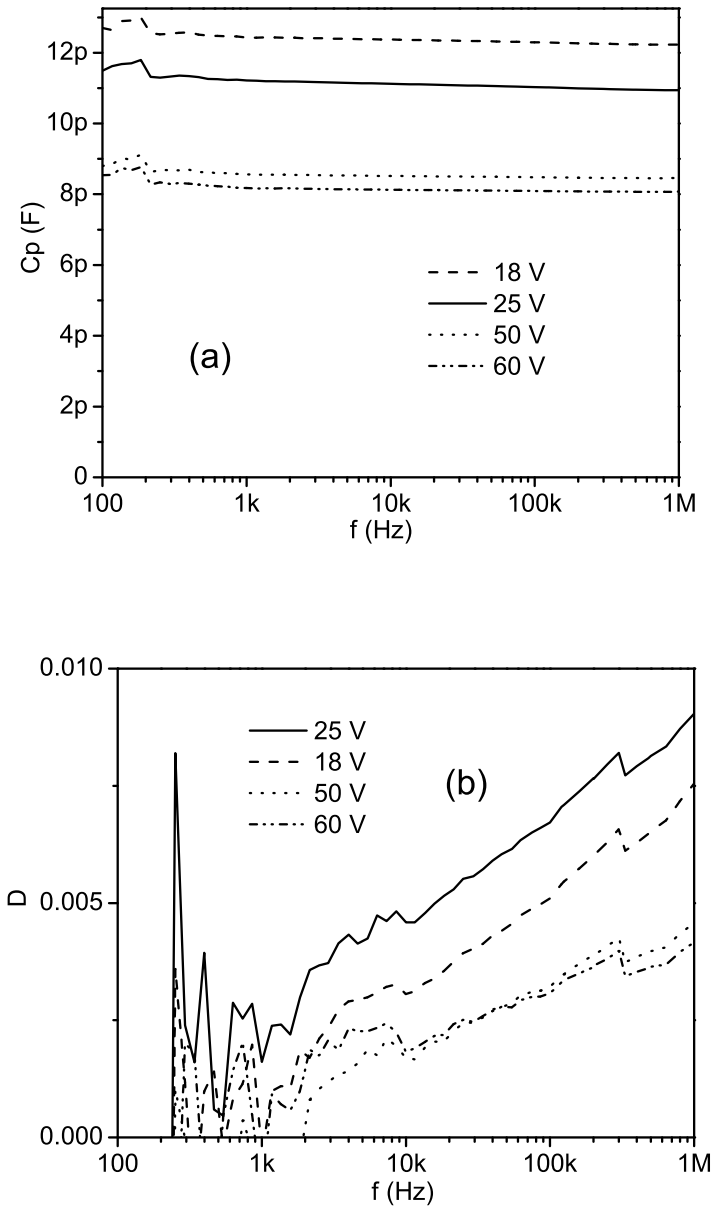

Figure 1.10: AI sensor, p-side. (a) Capacitance versus frequency of the single strip towards all other strips on the same side, for four values of the bias voltage (18, 25, 50 and 60 V). (b) Dissipation factor for the same measurement.

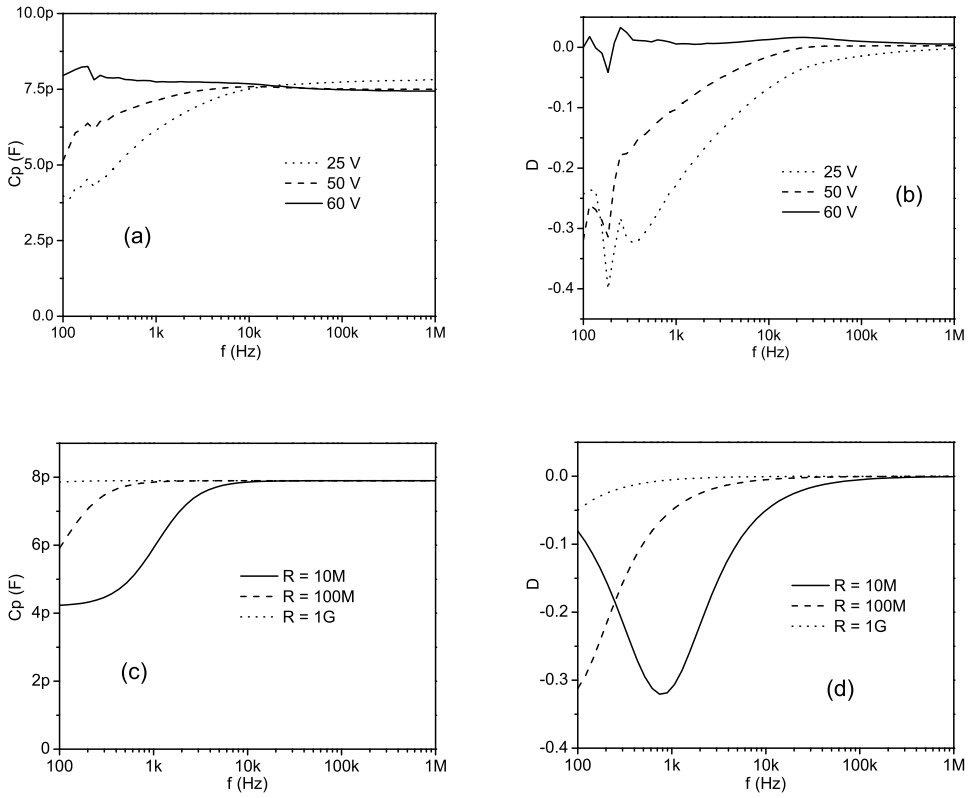

Figure 1.11: AI sensor, n-side. (a) Capacitance versus frequency of the single strip towards all other strips on the same side, for three values of the bias voltage (25, 50 and 60 V); the bias ring is at ground. (b) Dissipation factor for the same measurement. (c) Capacitance calculated from the model of Figure 1.7b, with $C_{layer} = 7.4$ pF, $C_{is} = 4.2$ pF and three values of R (10 MΩ, 100 MΩ, 1 GΩ). (d) Dissipation factor calculated from the model, with the same parameter values.

situations, where the resistive layer was junction-insulated from the bias ring). As before, there is an interstrip capacitance C_{is} between the strip and its neighbors, and a capacitance C_{layer} of the strip towards the resistive layer. This time there is no long-range coupling between the strips through the resistive layer, because the latter is tied to the bias ring at the strip ends. R represents, with the limits of a lumped-element model, the resistance of the accumulation channel up to the bias ring.

Consider first the case in which the bias ring is kept at ground, and we measure the capacitance between the single strip and all the other strips (the v_{AC} signal is applied to all the other strips) [2].
We then calculate the capacitance and dissipation factor in the parallel RC model

[2]The backside is at constant voltage V_{bias}, equivalent to ground for the signal.

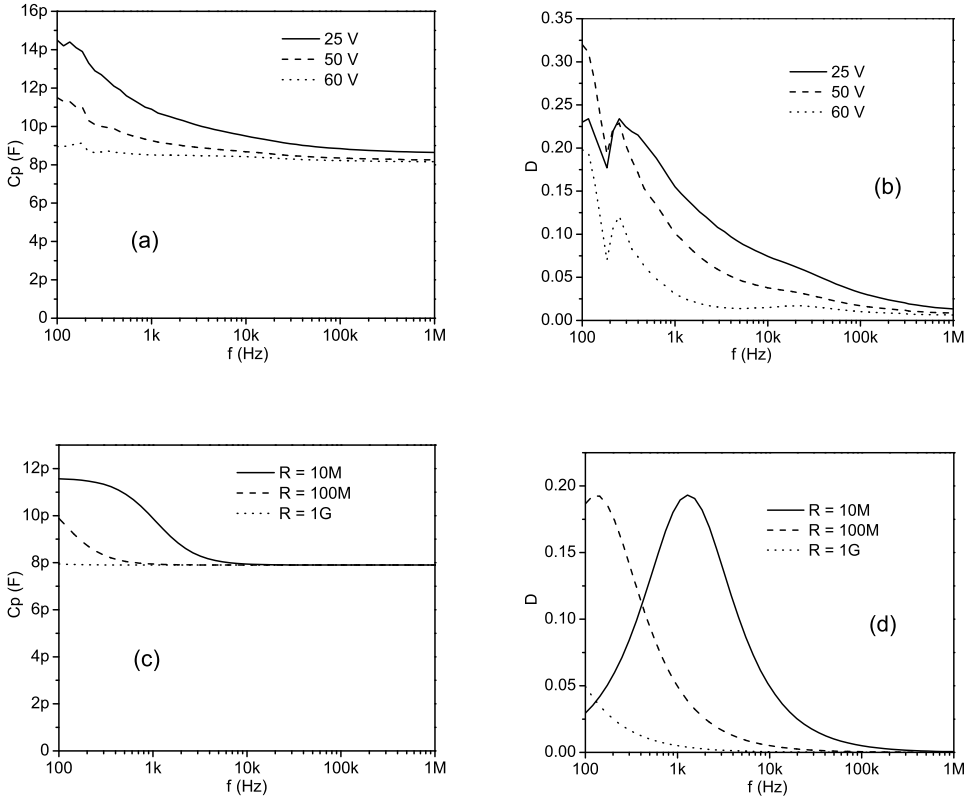

Figure 1.12: AI sensor, n-side. (a) Capacitance versus frequency of the single strip towards all other strips on the same side plus the bias ring, for three values of the bias voltage (25, 50 and 60 V); the bias ring is connected to the HIGH terminal. (b) Dissipation factor for the same measurement. (c) Capacitance calculated from the model of Figure 1.7b, with $C_{layer} = 7.4$ pF, $C_{is} = 4.2$ pF (same as in Figure 1.11) and three values of R (10 MΩ, 100 MΩ, 1 GΩ). (d) Dissipation factor calculated from the model, with the same parameter values.

of Figure 1.7(b), with the "BR" terminal at ground:

$$D = \frac{Re(Y)}{Im(Y)} = \frac{-\omega C_l^2 R}{C_{is} + 2(\omega C_l R)^2 (2C_{is} + C_l)} \tag{1.4}$$

$$C_p = \frac{Im(Y)}{\omega} = \frac{C_{is} + 2(\omega C_l R)^2 (2C_{is} + C_l)}{1 + (2\omega C_l R)^2} \tag{1.5}$$

Figure 1.11 shows the measured values of C_p and D versus frequency, for three different bias voltages. Also reported are the predictions of the model with three different values of the resistance R. The values of the two capacitances C_{is} and C_{layer} of the model have been adjusted in order to reproduce the measured capacitance in the high and low frequency limits. The measured C-f and D-f curves flatten out at high bias voltage (exceeding 60 V). As before for the p-side of the AE sensor, the model reproduces this behaviour when R goes to infinity: the interpretation is that as the bias voltage increases the electron layer at the ends of

the strips is depleted by the p-stops becoming more negative with respect to the bias ring, so that the accumulation channels in between the strips are eventually disconnected from the bias ring and from each other. Again, this view is supported by 3-D simulations, as reported in Section 1.1.5. At lower bias voltages, these accumulation channels are connected to the bias ring, which is kept at ground, so they act as an electrostatic shield in between the strips, depressing the measured interstrip capacitance; because of their high resistance, however, the shielding is only effective at low frequencies. As for the case of the AE sensor, the shapes of both the C_p and D curves qualitatively agree with a very simple three element model. The model also predicts the negative values for the dissipation factor observed at low frequencies for the two lower bias voltages.

A second measurement has been performed by connecting the bias ring to the HIGH terminal, so that the v_{AC} signal is fed both to the bias ring and to all the other strips. The results are shown in Figure 1.12, together with the predictions of the model for this setup:

$$D = \frac{Re(Y)}{Im(Y)} = \frac{\omega C_{layer}^2 R}{(C_{is} + C_{layer}) + 2(\omega C_{layer} R)^2 (2C_{is} + C_{layer})} \tag{1.6}$$

$$C_p = \frac{Im(Y)}{\omega} = \frac{(C_{is} + C_{layer}) + 2(\omega C_l R)^2 (2C_{is} + C_{layer})}{1 + (2\omega C_{layer} R)^2} \tag{1.7}$$

These are very similar to the previous equations, just note the opposite (now positive) sign of D and the replacement $C_{is} \rightarrow C_{is} + C_{layer}$ in the numerator of C_p and in the denominator of D.

As before we get a satisfactory qualitative agreement between the model and the measured data.

1.1.5 3D Numerical Device Simulations

What happens to the electron accumulation layer at the Si-SiO_2 interface can be guessed from the capacitance measurements reported above and from an intuitive picture of the situation, but it is worth looking for a confirmation with the help of device simulation. The task is complicated by the fact that the effects to be reproduced are intrinsically three-dimensional, so that a 3-D device simulator is required [3].

As with all 3-D simulations, the number of mesh points is a critical issue, and a careful selection of the region of interest must be made. This has been chosen as the strip-end region facing the bias ring, since there we expect the electron accumulation layer to be interrupted. In order to reduce as much as possible the number of mesh points, the backside has been taken unpatterned and the substrate mesh very rough. Taking advantage of the symmetry it has been sufficient to draw just one half of the interstrip region, 47.5 μm wide instead of the 95 μm pitch: Neumann boundary conditions are applied at the symmetry planes. The number of mesh vertices was on the order of 100k.

Two structures have been simulated, corresponding to the n and p sides of the AI detector, each one for six combinations of oxide charge density and substrate doping.

[3] ISE-TCAD 7.0 has been used. Each simulation took about 24 hours on a Pentium 4 single-processor machine.

$Q_{oxide}(q\,cm^{-2})$	$V_{depl}(V)$	p-side (V)	n-side (V)
$1\,10^{11}$	16	5	20
	50	5	50
$2.5\,10^{11}$	16	25	50
	50	25	85
$5\,10^{11}$	16	75	110
	50		140

Table 1.2: Summary of 3-D simulations. The first two columns report input parameters: the fixed oxide charge density (in units of elementary charges cm^{-2}) and the depletion voltage of the sensor (as a measure for the substrate doping). The last two columns show the results of the simulation for the minimum bias voltage at which the electron accumulation channels separate from each other.

The simulation increased the bias voltage (applied on the backside) in steps of 5 V, keeping the bias ring at ground; the strip, as in punch-through biased conditions, was left floating.
By looking at the values of carrier concentrations and potential at the Si-SiO_2 interface, we can verify that the electron accumulation layer actually depletes near the bias ring at reasonable values of bias voltage; the electron concentration in the interstrip channel, instead, remains practically constant.
The values of bias voltage for which the electron layer is depleted at strip ends are summarized in Table 1.2. Obviously, since the electron accumulation at the interface is induced by the positive oxide charge, the bias voltage for which the channel depletion occurs is strongly dependent on this concentration. On junction side (p-side), this voltage is practically independent of the doping concentration (within the resolution allowed by the 5 V steps), since the electric field peaks at the junction. On the ohmic side (n-side), the bias voltage at which the channel is depleted strongly depends on the substrate dopant concentration, because the electric field configuration on the n-side is influenced by the bias voltage only after the substrate is depleted.

From the capacitance measurements on the AI sensor we deduced that on p-side the channels were already insulated at 25 V bias, while on n-side this happened at about 60 V bias. The values reported in Table 1.2 agree well with these numbers, assuming an oxide charge density of $2.5 \cdot 10^{11}$ cm^{-2}, corresponding to an average value measured on the test structures of the ITC wafers.

An example of the simulation results is shown in Figure 1.13, showing the electrostatic potential at the interface in the strip-end region. At low voltage, the electron accumulation layer surrounds the strip and is therefore connected with the layers surrounding the adjacent strips. The interface is equipotential, since the electron layer is resistive and low currents flow through it. At high enough voltage, the accumulation layer is depleted in a small region between the p-stops at the strip end on n-side, and in the punch-through gap between strip and bias ring on p-side. On both sides, the electron accumulation channels in between the strips are then insulated from each other. The potential shows a discontinuity, sign that a continuous resistive path is absent.

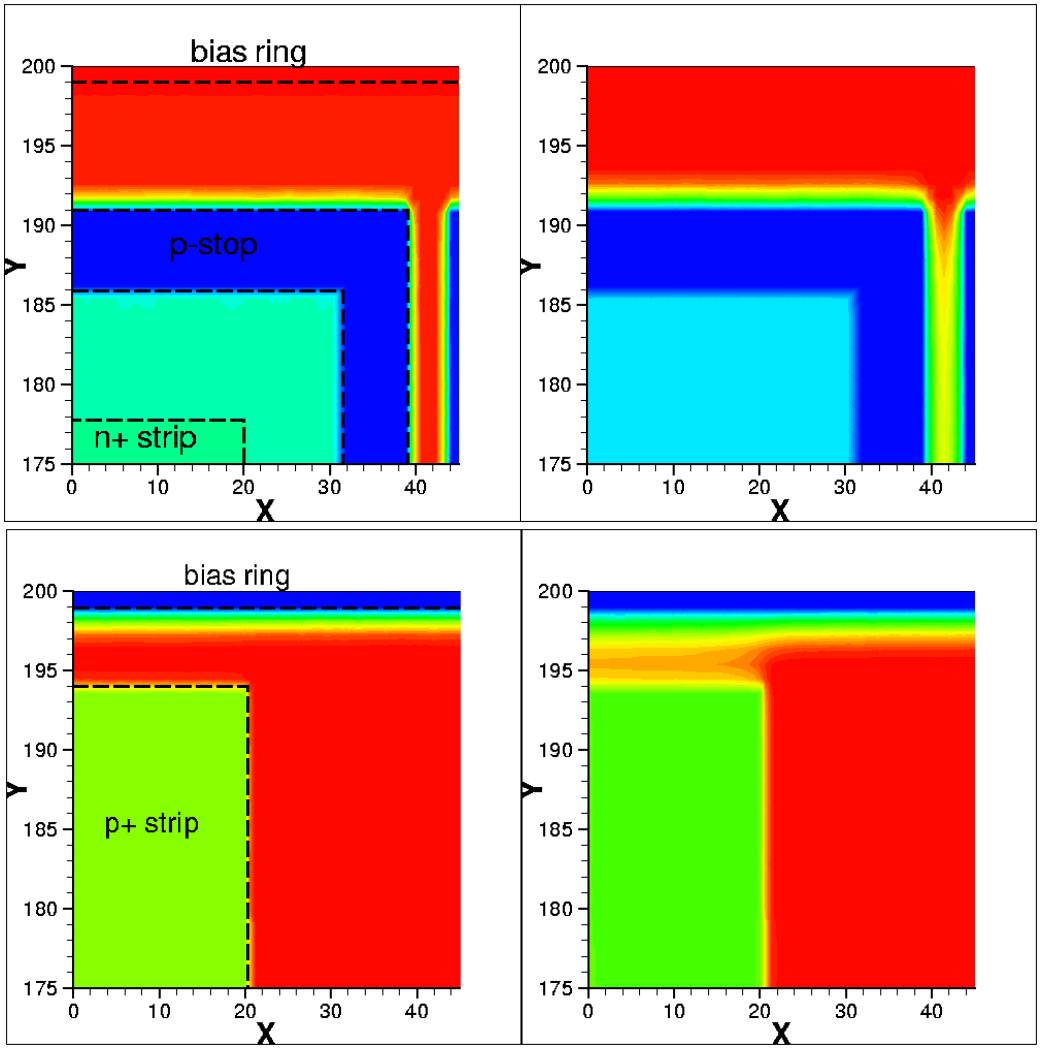

Figure 1.13: Simulated potential at the Si-SiO_2 interface. Upper two pictures: n-side of AI-type sensor at 40 V bias (left) and 60 V bias (right). Lower two pictures: p-side of AI-type sensor at 10 V bias (left) and 25 V bias (right). Positive oxide charge density is $2.5 \cdot 10^{11}$ cm^{-2}. Only 1/8 of the simulated strip length (vertical direction) is shown

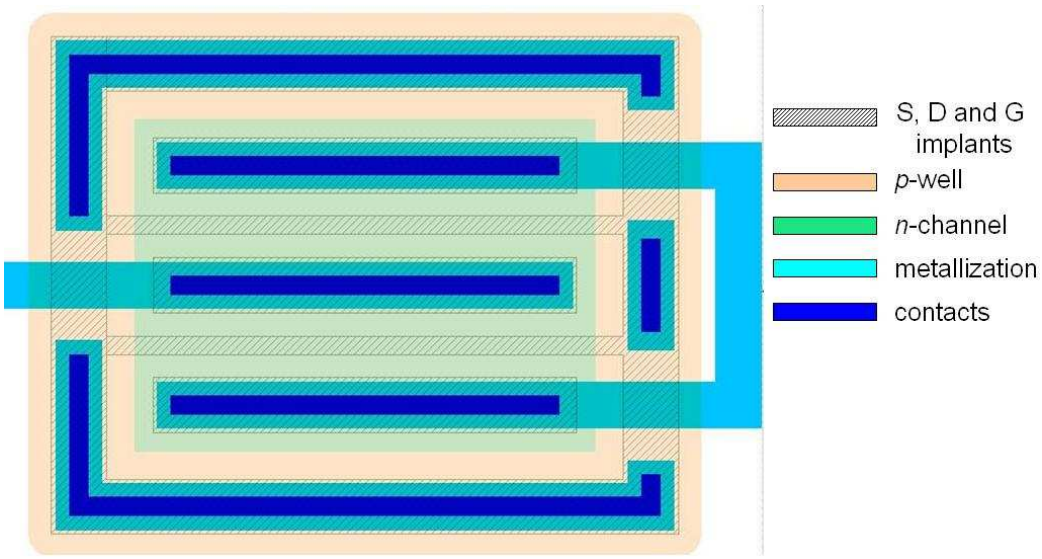

Figure 1.14: Layout of a triode-type JFET with a channel length of 4 μm and a width of 200 μm.

1.2 Microtrip Sensors with Integrated Source Follower

The second type of silicon strip detector considered in this study is a single-sided sensor with a JFET-based Source-Follower (SF) integrated at one end of each strip, as a first signal conditioning stage [14] [15]. They have been designed in an attempt at improving the signal-to-noise performance when very long strips, obtained by ganging together several sensors, are required. Then, by having a SF on each strip segment, the capacitance at the input could be limited to that of a single detector.
In a different situation, the integrated SF could allow to take better profit of the low capacitance of small detectors, by reducing the parasitic capacitance of connections.

Prototypes of these sensors have been fabricated by ITC-irst [4], making use of a technology they had developed for integrating, on high resistivity substrates, totally depleted detectors with JFETs, MOSFETs and BJTs [16] [17] [15].

In this process, the n-channel JFET is enclosed in a p-well, with the purpose of insulating the channel from the n-type high resistivity substrate, and allowing complete depletion of the latter by the applied bias voltage. In the JFETs used for the SF, adopting a triode configuration, the p-well is connected at the implant level with the gate, so it also acts as a bottom gate.
An example of the JFET layout is shown in Figure 1.14.

In a first implementation of the technology, although the JFETs showed good static characteristics, they exhibited higher white noise than could be attributed to channel thermal noise, as estimated from the measured transconductance. This excess noise has been traced down to a high gate series resistance, particularly in the bottom gate [15] [18], due to insufficient doping of the p-well. The doping profile of the p-well is shown by the curve on the left in Figure 1.15. Because of

[4]Now FBK-irst, "Fondazione Bruno Kessler".

the low doping, a drain voltage of only 3 V was sufficient to completely deplete the well at the drain end of the channel, leaving the undepleted portion of the well connected to the top gate only at the source end. This, together with the low conductivity of the well itself, caused a high series resistance in the bottom gate, responsible for the excess white noise observed.
Indeed, during the electrical characterization, it has been found that a few volts applied to the n^+ drain (or source), with all other terminals grounded, are enough to deplete the p-well, turning on a punch-through current from drain to substrate. (When a bias voltage is applied to the substrate, the punch-through current is suppressed, but the well depletion and the high series resistance in the bottom gate are still there.)

In order to address this issue, a new version of the technology has been developed, featuring a deeper and more doped p-well [19]: the new doping profile is shown by the right plot in Figure 1.15. The new JFETs have better noise performance, since their bottom gate is not depleted by the drain voltage and has lower series resistance.

Figure 1.16 shows, for the two processes, the electrostatic potential under the drain, plotted versus the first 5 μm of depth into the substrate, with different voltages applied to the drain, keeping all others terminals grounded. The plot is obtained from a numerical device simulation performed with the ISE-TCAD software [20]. As can be seen, in the case of the "old" p-well, for $V_D = 4$ V there is no potential barrier to electron injection from the substrate into the drain, leading to large current flow between these two terminals, as has been measured on real devices. With the new process, instead, the barrier to electron injection is still present.

1.2.1 Device Description

Two configurations of detectors with integrated Source-Follower have been investigated: isolated "pixels" (area 0.7 mm×0.8 mm) and single-sided microstrip sensors (strip pitch 100 μm, strip length 7 cm). The schematic of the devices is sketched in Figure 1.17. The SF transistor J_S has an active load, made with a second JFET J_C in current source configuration [21].

Pixels are biased by an integrated 3 MΩ polysilicon resistor[5]. They are of two types, called PIN1 and PIN2, differing by the size of the JFETs[6]:

- PIN1 : J_S 1000/4, J_C 400/4;

- PIN2 : J_S 400/4, J_C 200/4;

Figures 1.18 and 1.19 show microscope pictures of the Source-Follower region in the structure PIN2 and a detail of the J_S transistor.

The gate of J_S, directly connected to the pixel, is not externally accessible. However, since only the very small diode and gate leakage currents flow through the 3 MΩ resistor, the ohmic drop through the resistor is negligible, and the

[5]This is the DC-measured value of the resistance. However, at relatively high frequencies, the distributed capacitance of the resistor shunts to ground part of this resistance, resulting in a lower, frequency-dependent effective resistance.

[6]The notation e.g. 1000/4 stands for a channel width of 1000 μm and a channel length of 4 μm.

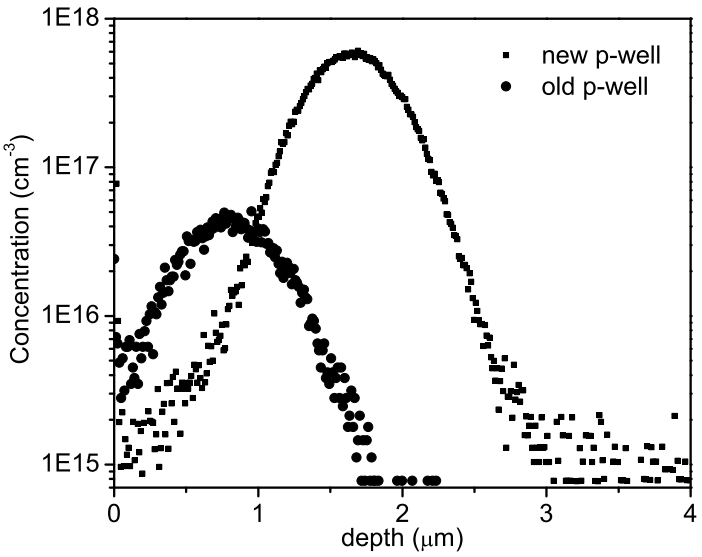

Figure 1.15: Doping profile of the p-well in the old and the new versions of the technology developed by ITC-irst [19] [18]. Data come from SIMS measurements.

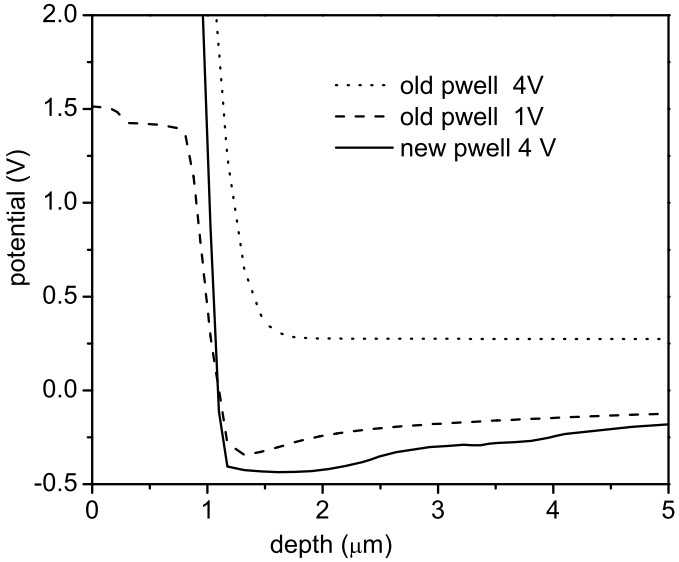

Figure 1.16: Electrostatic potential under the drain, plotted versus the first 5 μm of depth into the substrate, obtained from a 2-D simulation performed with ISE-TCAD. Curves refer to a JFET whose bottom gate is the "old" p-well, (at 1 and 4 V applied on drain) and for a JFET with the "new" p-well (at 4 V). Substrate, source and both top and bottom gates are at ground.

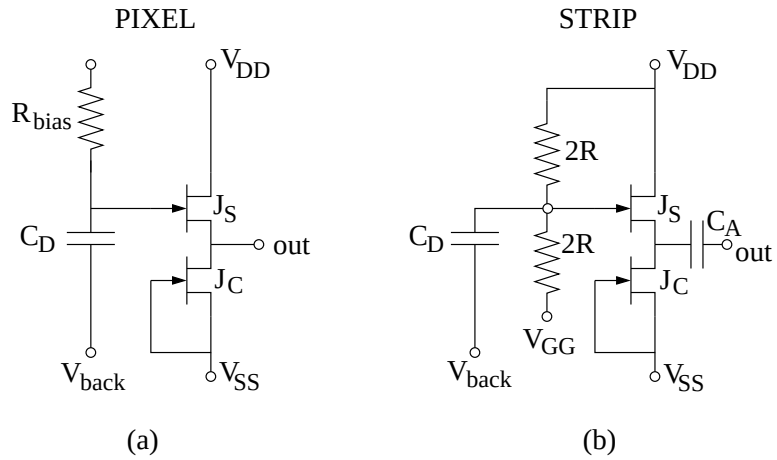

Figure 1.17: Schematics of the detectors with integrated JFETs: (a) pixel, (b) strip. Open circles represent the accessible terminals. The strip detector has 64 strips with individual output pads, while the V_{DD}, V_{SS} and V_{GG} terminals are in common between the 64 strips.

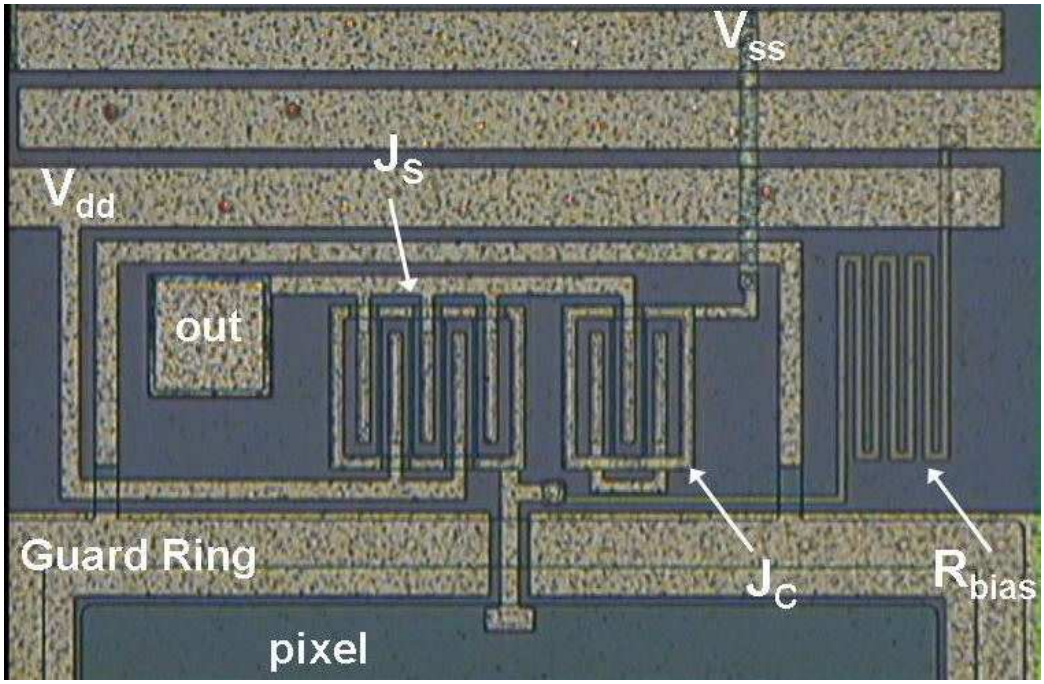

Figure 1.18: Picture of the Source-Follower of the PIN2 structure.

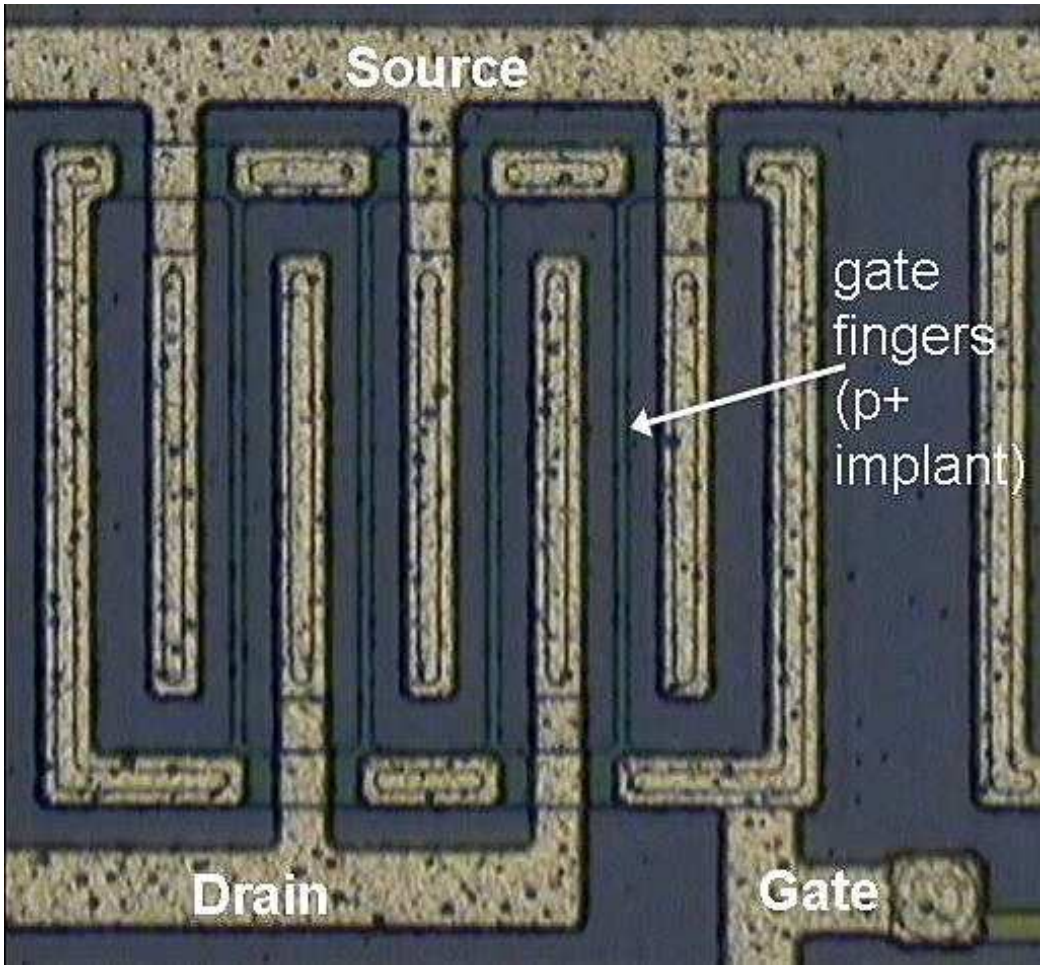

Figure 1.19: Detail of the 400/4 J_S FET in structure PIN2, showing the three source fingers, the two drain fingers and the gate surrounding them.

voltage applied to the V_{GG} terminal can be considered as applied to the gate[7]. Then, having a pad on both source and drain, full DC characterization of J_S is possible.

Coming to J_C, its gate is shortcircuited to the source, in order to act as a current source when biased into saturation. Then it is only possible to measure the output characteristics at $V_{GS} = 0$, showing the value of the saturation current, which defines the working point of J_S.
Unfortunately we get no information about the transconductance $g_{m,C}$, an important parameter entering in noise estimates[8].
For the 400/4 J_C in the structure PIN1 we can refer to J_S in PIN2, which is identical to it but has all terminals independently accessible.
For J_C in PIN2 (200/4) we have no match, so we must estimate its parameters from scaling rules: $g_{m,C}$ of PIN2 will be one half – to first approximation – of $g_{m,S}$.

It should be kept in mind, however, that an accurate determination of the parameters of the FET of interest from measurements made on another device (even if identical in design) is not always possible. In fact, on the same wafer there are test structures containing several JFET sizes (some of them are identical to the ones in our Source-Followers) and we noticed a little spreading of parameters between nominally identical devices.

The strips are biased via a $2R \,||\, 2R$ voltage divider, taking bias from the common lines V_{SS} and V_{GG}. Because of the low reverse leakage currents of gate and strip, every strip stays at the same voltage $(V_{DD} + V_{GG})/2$. The V_{DD} line too is common for all 64 strips of the sensor.
J_S is a 500/4 JFET, while J_C has the size 200/12. Both have a different geometry with respect to the devices in the pixel structures: the "fingers" composing the source and drain are only 50 μm long, instead of 100 μm.
The test structure includes a replica of J_S, but not of J_C. In the layout of the strip device, the node corresponding to the source of J_S and drain of J_C is not externally accessible through a pad (see Figure 1.17(b)). Direct measurements on the devices connected to one of the strips have been made after breaking the passivation layer in order to access with a probe the source of J_S.

1.2.2 DC Measurements

Among the several JFETs in test structures (all in triode configuration[9]), we tested the 1000/4 (J_S of PIN1), the 400/4 (J_S of PIN2 and J_C of PIN1), the 200/4, whose finger length is double of the previous two JFETs and then is slightly different from J_C of PIN2, and the 500/4 (J_S of the strip) whose finger length is one quarter that of the first two.

Some examples of the standard measurements made upon them are presented in Figures 1.20 to 1.23, referring to the 1000/4 test structure. From the output characteristics I_D versus V_{DS} (Figure 1.20), we obtain the output resistance of the JFET, i.e. the reciprocal of the output conductance $g_d = \mathrm{d}I_D/\mathrm{d}V_D$: in the

[7] In any case, a correction for the voltage drop could easily be performed by measuring the current drawn by the V_{GG} terminal.

[8] Subscripts S and C denote quantities referred to the JFETS J_S and J_C, respectively.

[9] The top and bottom gates are in contact.

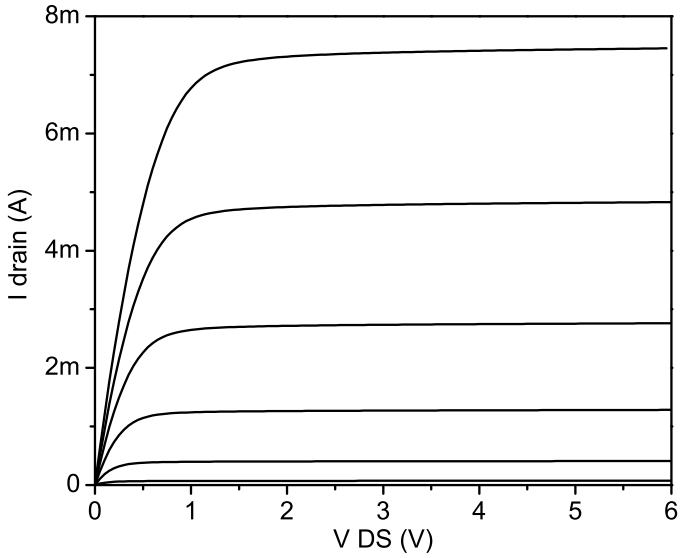

Figure 1.20: Output characteristic I_D-V_{DS} of the 1000/4 JFET test structure. V_{GS} = 0, -0.2, -0.4, ..., -1 V.

saturation region this resistance ranges, in the case of the 1000/4 device, from 41 kΩ at $V_{GS} = 0$ to 3.3 MΩ at $V_{GS} = -1$ V; similar values hold for the other JFETs.

In Figure 1.21 the input characteristic I_D versus V_{GS} is shown, for $V_{DS} = 2$ V (there is little dependence on V_{DS} as long as we stay in the saturation region). The drain current shows pinch off at $V_G \simeq -1.5$ V. The transconductance $g_m = \mathrm{d}I_D/\mathrm{d}V_G$, computed as incremental ratio of the measured points, follows the drain current.

Figures 1.22 shows gate current versus drain voltage. Note how the gate current increases rapidly for drain voltages in excess of 3 V. This at first would appear to be due to avalanche multiplication in the reverse biased gate-drain junction; however, the fact that the current is lower at $V_{GS} = -1$ V than at $V_{GS} = 0$ – despite the higher value of V_{GD} – shows that a different interpretation is needed. Further insight can be obtained from the "complementary" Figure 1.23, showing I_G versus V_G, for different values of V_{DS}: when the gate voltage becomes more negative, the gate-drain junction becomes more reverse biased, but the gate current decreases. Instead, the current increases at higher values of the drain-source voltage (controlling the field in the pinched-off region of the channel) and at more positive values of the gate voltage (increasing the channel current).
This indicates that the multiplication process is due to impact ionization by the electrons making up the channel current, in the high-field region near the drain [22]. The generated electrons flow to the drain, adding up to the channel current; however, their effect is hardly noticeable because the channel current is much larger than this contribution from impact ionization. The generated holes are collected on the gate, leading to a dramatic increase of the otherwise very small gate current (as shown by Figure 1.23). In any case, our operating voltage is $V_{DS} \simeq$2.5 V, in a

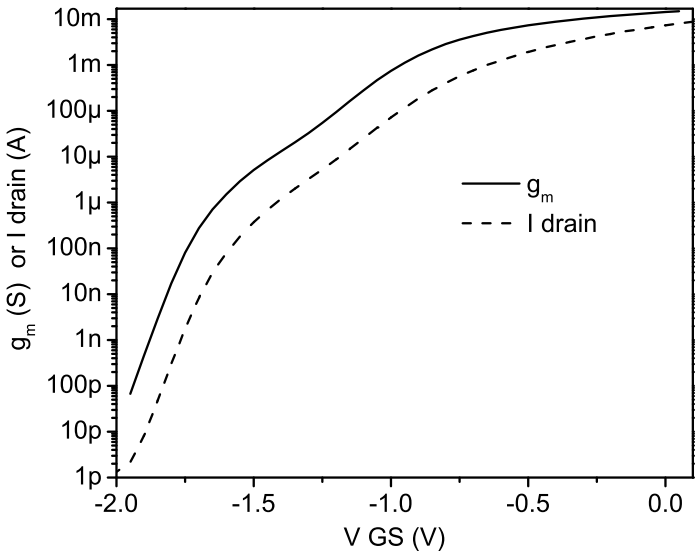

Figure 1.21: Input characteristic I_D-V_{GS} of the 1000/4 JFET test structure. I_D and g_m are plotted for $V_{DS} = 2$ V.

	200/4	400/4	500/4	1000/4
g_m @ $V_{GS} = 0V$	3.0	5.8	6.9	14.3
g_m @ $V_{GS} = -0.2V$	2.5	4.7	5.6	11.6
g_m @ $V_{GS} = -0.4V$	1.9	3.5	4.2	8.8
g_m @ $V_{GS} = -0.6V$	1.2	2.2	2.9	5.8

Table 1.3: Trasconductance g_m (in mS) of every measured test structure. V_{DS} =3 V.

region where the multiplication effects can be neglected even for the gate current.

Table 1.3 shows the g_m values measured on the test JFETs. It can be seen that they scale reasonably well with the channel width W. The scaling is less good for the 500/4 device, because it is made of 4 times shorter "fingers", leading to a larger influence of the "border effects".

In the source follower configuration, the current flowing into the channel of the JFET J_S is fixed by the saturation current of J_C, acting as a current source. This current defines the gate-source voltage of J_S.
Both JFETs are expected work in saturation; in order to reach this condition, the supply voltages V_{DD} and V_{SS} (Figure 1.17) must exceed some minimum values. Table 1.4 lists the operating point of the JFETs, as adopted for the noise measurements.

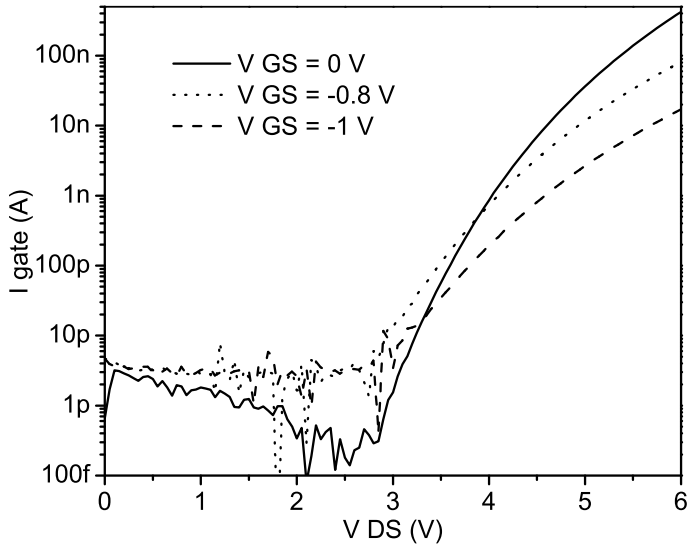

Figure 1.22: Gate current of the 1000/4 JFET versus V_{DS}, for different values of V_{GS}. I_G shows avalanche multiplication for $V_{DS} \gtrsim 3$ V.

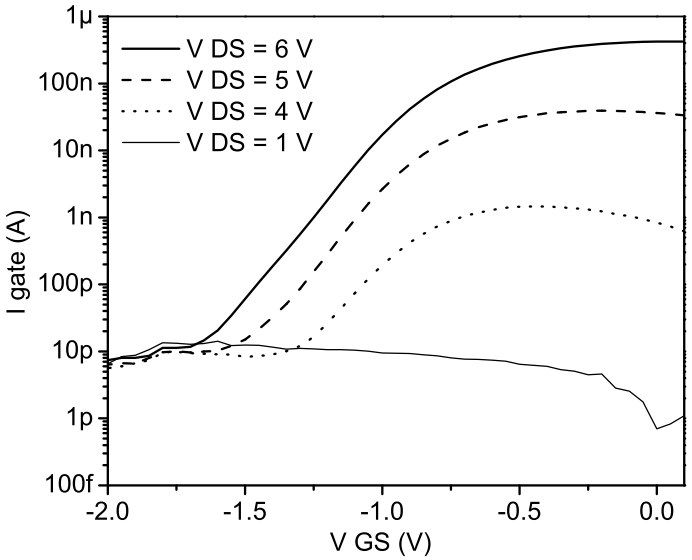

Figure 1.23: Gate current of the 1000/4 JFET versus V_{GS}, for different values of V_{DS}.

	PIN1	PIN2	STRIP
I_{drain} (mA)	4.34	1.41	0.285
V_{gate} of J_S (V)	0	0	1.5 (2)
V_{SS} (V)	-3	-3	0
V_{DD} (V)	3	3	3 (4)
V_{GS} of J_S (V)	-0.45	-0.34	0.77
V_{DS} of J_C (V)	3.45	3.34	2.27 (2.77)
V_{DS} of J_S (V)	2.55	2.66	0.73 (1.23)
g_m (mS)	10.7	4.62	1.7

Table 1.4: Operating points of the JFETs of the devices bonded and used as detectors.

	200/4	400/4	500/4	1000/4
C_{GD} @ $V_{SG} = 0$ V	1.44	1.57	2.34	4.36
C_{GD} @ $V_{SG} = 0.2$ V		1.55	2.34	4.28
C_{GD} @ $V_{SG} = 0.4$ V		1.53	2.31	4.17
C_{GD} @ $V_{SG} = 0.6$ V		1.52	2.29	4.09
C_{GD} @ $V_{SG} = 0.8$ V			2.28	4.05

Table 1.5: Gate-drain capacitance for $V_{drain} = 3V$. Gate to LOW. Source to SMU. $2.7\mu F$ connected from source to ground. Values in pF.

1.2.3 AC measurements

For noise measurements, the capacitance entering noise expressions is the one seen by the gate of the input transistor. In the source-follower configuration, the gate-source capacitance does not contribute: since V_{GS} is kept constant by the follower effect, this capacitance does not charge up. We then need to know only the gate-drain capacitance. The JFETs have been designed to have one more finger in the source than in the drain, so that the gate-drain capacitance is smaller.

We have measured the capacitance C_{GD} versus V_{DG} for several values of V_{GS}. The results for $V_{GD} = 3$ V are shown in Table 1.5. Because the gate is kept at 0 V by the LOW terminal of the LCR meter (see Appendix A), while the drain is connected to the HIGH terminal (supplying the v_{AC} signal and the V_{DG} bias), we must provide an additional DC voltage to the source and, at the same time, we must keep it at ground for what concerns the AC signal. The SMU we use as voltage source is not expected to give a good AC ground, so we connected a large value capacitor C_0 between source and ground (except in the measurements with the source at 0 V, when the source has been directly connected to ground). This capacitor in some conditions causes the SMU to oscillate (this is why Table 1.5 has white boxes).

The value of C_0 must be chosen large enough to make its impedance small compared with that of the channel; the channel resistance $1/g_d$ in Figure 1.20 has a minimum value of 100 Ω at $V_{GS} = V_{DS} = 0$. At the measurement frequency of 100 kHz, $(\omega C)^{-1} = 100\,\Omega$ when $C = 16$ nF, so that with the used capacitance $C_0 = 2.7\,\mu$F the source is kept efficiently at ground.

The gate capacitance has been measured to be frequency independent in a

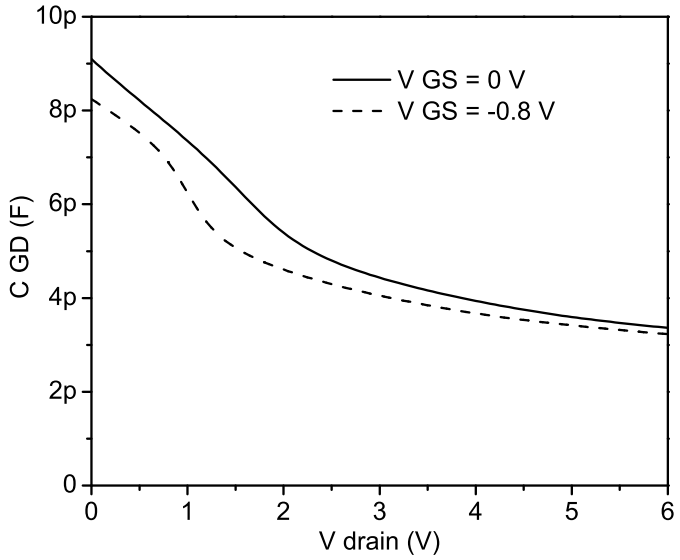

Figure 1.24: Gate-drain capacitance versus V_{DG} for a 1000/4 JFET, with $V_{GS} = 0$ and -0.8 V.

wide range of frequencies, as expected for a reverse biased junction as long as series resistance is not an issue. A relatively high frequency of 100 kHz has been chosen, to make the admittance of the 2.7 μF capacitance much larger than the conductance of the channel and to increase the accuracy of the measurement. Looking at Figure 1.24, we note that the capacitance increases more rapidly at low drain voltages, when the JFET is in its "linear" region: in this case the channel is in ohmic contact with the drain, so that a fraction of the gate-channel capacitance (the other end of the channel is kept at AC ground by the source) contributes to the gate-drain capacitance. In the saturation region the capacitance shows a modest dependence on V_{GD} and V_{GS}. The dissipation factor is low (below 1%) for $V_{GD} \lesssim 5$ V.

From Table 1.5 we see the capacitance approximately scales with the channel width for the 1000/4 and 400/4 JFETs, that have similar geometry. The 200/4 JFET has a different structure, with only one gate and one source finger, 200 μm long, and the perimeter of the gate running all around the drain is the same as for the 400/4 JFET: hence the very similar capacitance values. The 500/4 JFET, on the other hand, has a higher capacitance than expected from scaling; this can be easily explained by considering border effects, which in this structure are more important due to the shorter fingers, as noticed for the transconductance values.

Chapter 2

Models for Noise Analysis in Silicon Detectors

Often the most important feature limiting the performances of a system is its inherent level of noise. This is a measurable quantity and can be expressed in many ways. The signal to noise ratio indicates, for a specific type of event, the ratio between the signal (assumed to be noise-free) and the rms noise. Since most detectors rely on the measurement of the charge delivered by an ionization event [1], the most common parameter used to characterize the noise is the equivalent noise charge (ENC), defined as the input charge that produces at the output a signal amplitude equal to the rms noise.
It is the minimum charge detectable by the system, the one making the signal to noise ratio equal to 1. In any detector, minimizing the ENC could not be the only issue. As an example, consider a detector working at high rate: if the signals are processed too slowly, phenomena like pile-up may occur; consider also cases in which the charge needs time to be collected at the electrode: a longer signal helps collecting the total charge avoiding the so called ballistic deficit. Anyway, even it is meaningless to talk about the best detector, a best detector can be found for every application. Now, we present the theory underlining the philosophy of pulse processing. This argument has been discussed many times and long ago, it is a full understood issue and largely used: we do not have the purpose of presenting the details of the theory, we just present the underlying ideas. Since in this work we will use two type of preamplifiers (charge and voltage sensitive ones) we describe just these two, skipping the current sensitive one. First, a brief review of the noise sources we are dealing with is presented.

2.1 Noise Sources in Detector Systems

In any physical system, measurable quantities come with some sort of unavoidable superimposed fluctuations, due to the discrete nature of matter or the quantity itself or to the randomness of the constituting processes [23]. All these fluctuations take the name of "noise"; it is a statistical property of the system and can be estimated and measured. Obviously, it could be minimized, and often this is

[1] The charge produced by an ionization event is proportional to the energy deposited into the detector material. In Silicon, an average energy of 3.6 eV is required to create an electron/hole pair

the most important aim of the system designer.
Consider a process, no matter the quantity involved, represented by the real function of time $x(t)$. It spans from $-\infty$ to $+\infty$ and of such a process we want to calculate the Fourier transform. This may seem hopeless, because one condition for the existence of the transform function $X(\omega)$ is that $x(t)$ must be absolutely integrable, i.e.:

$$\int_{-\infty}^{\infty} \mathrm{d}t|x(t)| < \infty \tag{2.1}$$

but this condition does not hold, since $x(t)$ does not decay to zero at $\pm\infty$. $|x(t)|^2$ is related to the energy carried by the physical process and it is clear that the energy increases with time. However, our measurement times are never infinite and we are interested in statistical quantities independent of the time of observation. Calling T the observation time, we can define a new function from $x(t)$, coincident with $x(t)$ inside the window $\pm\frac{T}{2}$ and null outside:

$$x_T(t) = \begin{cases} x(t) & \text{if } -\frac{T}{2} < t < \frac{T}{2} \\ 0 & \text{outside} \end{cases} \tag{2.2}$$

The gated (or truncated) function $x_T(t)$ is now absolutely integrable, so that its Fourier Transform exists

$$X_T(\omega) = \int_{-\infty}^{\infty} \mathrm{d}t\, x_T(t) e^{-i\omega t} \tag{2.3}$$

and, by Parseval's theorem (or energy theorem):

$$\int_{-\infty}^{\infty} \mathrm{d}t|x_T(t)|^2 = \frac{1}{2\pi}\int_{-\infty}^{\infty} \mathrm{d}\omega|X_T(\omega)|^2 = \frac{1}{2\pi}\int_{0}^{\infty} \mathrm{d}\omega\, 2|X_T(\omega)|^2 \tag{2.4}$$

Since $x_T(t)$ is a real process, the module of its Fourier Transform $|X_T(\omega)|$ is an even function, allowing the integral $\int_{-\infty}^{\infty}\mathrm{d}\omega$ to become, as written, $\int_0^{\infty} 2\,\mathrm{d}\omega$. Both sides of the equation above represent the energy of the process [2] and are finite as long $T < \infty$. The quantity $2|X_T(\omega)|^2$ can then be interpreted as the energy spectral density of the process, which has units of energy/Hz.

Dividing both sides by the observation time T we get the average power in the *gated* process $x_T(t)$:

$$\frac{1}{T}\int_{\frac{-T}{2}}^{\frac{T}{2}} \mathrm{d}t|x(t)|^2 = \frac{1}{T}\int_{-\infty}^{\infty} \mathrm{d}t|x_T(t)|^2 = \frac{1}{2\pi}\int_{0}^{\infty} \mathrm{d}\omega\frac{2|X_T(\omega)|^2}{T} \tag{2.5}$$

For the stationary noise processes we are interested in, it is reasonable to assume the existence of the limit:

$$\lim_{T\to\infty}\frac{1}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} \mathrm{d}t|x(t)|^2 \tag{2.6}$$

which can then be taken to represent the average power of the *ungated* process $x(t)$. Then:

$$\lim_{T\to\infty}\frac{1}{T}\int_{-\frac{T}{2}}^{\frac{T}{2}} \mathrm{d}t|x(t)|^2 = \lim_{T\to\infty}\frac{1}{2\pi}\int_{0}^{\infty} \mathrm{d}\omega\frac{2|X_T(\omega)|^2}{T} = \tag{2.7}$$

[2] They are actually proportional to the energy, with a dimensioned proportionality constant that depends on the nature of the process considered. For brevity, this proportionality constant is usually understood, and the expression above is conventionally called the energy of the process.

$$\frac{1}{2\pi}\int_0^\infty \mathrm{d}\omega[\lim_{T\to\infty}\frac{2|X_T(\omega)|^2}{T}]$$

where we have assumed that the limit $T \to \infty$ and the integration over ω can be interchanged. It is then natural to define the power spectral density of the process $x(t)$ as:

$$\frac{\mathrm{d}x^2}{\mathrm{d}f} = \lim_{T\to\infty}\frac{2|X_T(\omega)|^2}{T} \tag{2.8}$$

The power spectral density just defined is referred to as the "unilateral" spectral density; often, as in [11], the "bilateral" power spectral density is used, where the factor 2 in the numerator of 2.8 is absent and the integral extends from $-\infty$ to $+\infty$.

If $x(t)$ is the input of a linear network[3], it is straightforward to determine the power spectral density at the output of the system due to the input $x(t)$. If $h(t)$ is the response of the system to a δ-like impulse, then the output corresponding to the input waveform $x(t)$ is given by the convolution product:

$$x_{out}(t) = \int_{-\infty}^{+\infty} \mathrm{d}t'\, x(t-t')h(t') \tag{2.9}$$

In the frequency domain, this translates into the simple product of the Fourier Transforms:

$$X_{out}(\omega) = X(\omega)H(\omega) \tag{2.10}$$

Noise spectral densities are proportional to the square of the modulus of the Fourier transforms. Then, taking the square of the modulus of the expression above, we get:

$$\frac{\mathrm{d}x_{out}^2}{\mathrm{d}f} = \frac{\mathrm{d}x^2}{\mathrm{d}f}|H(\omega)|^2 \tag{2.11}$$

Integration over all frequencies gives the rms value of the output quantity $x_{out}(t)$. These concepts are already sufficient to derive the contributions of some of the most relevant noise sources.

2.1.1 Shot Noise

We illustrate the characteristics of shot noise by considering the current associated with random emission of carriers over a potential barrier. Example of this kind of process are the thermionic emission of electrons from a cathode in vacuum tubes, or the emission of holes or electrons by the punch-through mechanism in semiconductor devices. Considering a time T, in which N emissions are observed, the current can be expressed in the time domain as:

$$i(t) = q\sum_{k=1}^{N} f(t-t_k) \tag{2.12}$$

where q is the electron charge, and $f(t-t_k)$ gives the time dependence of the current pulse produced by a carrier emitted at time t_k. Since the integral of this

[3] a linear network is one for which the superposition law applies: in our case the preamplifier-shaper chain can be approximated as linear, i.e. we assume the signal amplitudes are small enough for the small signal analysis to apply

pulse must be equal to q, we have: $\int_{-\infty}^{+\infty} \mathrm{d}t\, f(t) = 1$. The Fourier transform of such a process is:

$$I(\omega) = qF(\omega) \sum_{k=1}^{N} e^{i\omega t_k} \tag{2.13}$$

with the corresponding power spectrum:

$$\lim_{T\to\infty} q^2 \frac{2|F(\omega)|^2}{T} \sum_{k=1}^{N} \sum_{m=1}^{N} e^{i\omega(t_k - t_m)} \tag{2.14}$$

The summation can be decomposed into one considering the terms $k = m$ and another considering the terms $k \neq m$. The first gives just the number N of pulses in the interval T, the other accounts for the DC level of the current [23]. Neglecting the second term, we obtain the power spectral density:

$$\frac{\mathrm{d}i^2}{\mathrm{d}f} = \lim_{T\to\infty} q^2 2|F(\omega)|^2 \frac{K}{T} = 2q^2\nu|F(\omega)|^2 = 2qI|F(\omega)|^2 \tag{2.15}$$

where $\lim_{T\to\infty} q\frac{N}{T} = q\nu$ is the DC current. Notice that, in the case the pulses are extremely sharp, to be considered as delta pulses, the power spectrum assumes the well known expression:

$$\frac{\mathrm{d}i^2}{\mathrm{d}f} = 2qI \tag{2.16}$$

Since all frequency dependent terms are inside $|F(\omega)|^2$, the noise is white, i.e. frequency independent, at least in the range of frequencies for which the physical pulse can be considered as δ-like: $\omega << \Delta t^{-1}$, where Δt in the "duration" of the current pulse.
The leakage current thermally generated via SHR traps in a semiconductor device has the same spectral power density 2qI [23], because it results from the superposition of current pulses generated by randomly emitted carriers.

2.1.2 Thermal Noise

A resistor in thermal equilibrium with its surroundings shows a noise voltage at its terminals, i.e. the open circuit voltage has a value different from zero, due to the thermal motion of the electric charges in a conductor. This phenomenon was discovered by Johnson back in 1928 [24], and in the same year the expression for this noise was first derived by Nyquist [25], on the basis of the second law of the thermodynamics, considering the power exchanges between a couple of resistors in thermal equilibrium.
Nowadays, this noise is referred to as "Johnson" or "thermal" noise.
He found that the noise voltage power spectral density is flat ("white") and has the value:

$$\frac{\mathrm{d}v^2}{\mathrm{d}f} = 4kTR \tag{2.17}$$

Any physical resistor shows this kind of noise.
In the analysis of electronics devices, one often encounters "effective" resistances, not related to an ohmic conduction process and calculated from the slope of the current-voltage characteristic of the device. It is important to notice that no thermal noise is associated with these resistances [26].

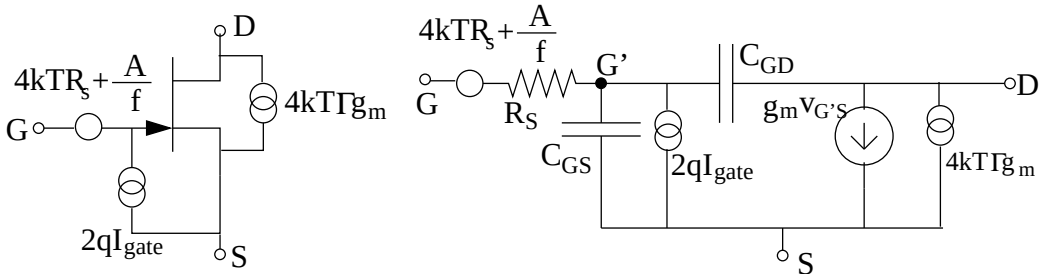

Figure 2.1: Location of the noise sources in a JFET. Also depicted is its relevant small signal model.

2.1.3 $\frac{1}{f}$ noise

While shot noise and Johnson noise are white noises, i.e. frequency independent, at least in the frequency range of interest in most physical cases, there are very common noise sources showing strong frequency dependence. The so called "flicker" noise comes with a power spectral density of $\frac{A_{1/f}}{f}$ and it is present in almost every electronic device. Trapping and detrapping processes, in which a carrier is trapped and released with a given time constant, generate a pure Lorentzian noise, having a power spectral density $\propto f^{-2}$. Very seldom a single time constant is involved, and with just a few values of time constants spread across a couple of decades, Lorentzian noise sums up to an almost perfect f^{-1} spectrum [26]. Usually, we refer to this kind of mechanism to explain flicker noise, related to some kind of imperfections of the material. It is clear that, in devices more affected by imperfections, the $1/f$ noise will be greater [27]. MOSFETs are particularly afflicted, being surface effect devices; JFETs are less sensitive, relying for their functioning on bulk effects.

2.1.4 Noise in JFETs

The noise sources in junction field-effect transistors are: leakage current of the gate, gate spreading resistance, thermal noise in the channel, flicker noise in the channel.
The gate leakage current is usually negligibly small in the JFETs used for spectroscopic applications. This current comes from carrier generation in a reverse biased junction. Its noise current spectral density is: $\frac{\mathrm{d}i^2}{\mathrm{d}f} = 2qI_{leakage}$.
Gate spreading resistance accounts for series resistance of the gate. Usually this noise contribution is small; its voltage spectral density is $\frac{\mathrm{d}v^2}{\mathrm{d}f} = 4kTR_{gate}$.
The resistance of the channel can be expressed in terms of the transconductance g_m as $(\Gamma g_m)^{-1}$, where the corrective factor Γ has a value of about 2/3 [8]. This gives at the drain a noise current with spectral density $\frac{\mathrm{d}i^2}{\mathrm{d}f} = 4kT\Gamma g_m$. Channel noise can be referred back to the gate via the transconductance, leading to a voltage spectral density $\frac{\mathrm{d}v^2}{\mathrm{d}f} = \frac{4kT\Gamma}{g_m}$. Summarizing, all noise sources in the JFET could be thought of as applied at the gate and described by an input noise voltage (Figure 2.1) .

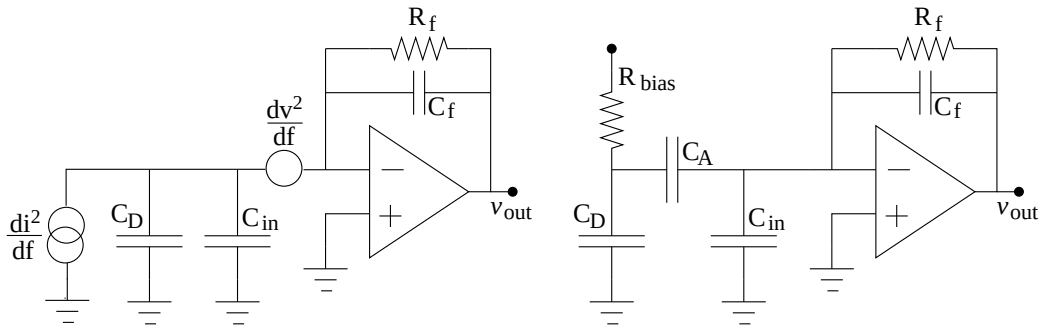

Figure 2.2: Fundamental elements of a Charge Sensitive Amplifier (CSA), the detector (represented by its capacitance) is DC-coupled (left) and AC-coupled (right) to the CSA. Also shown, the noise sources.

2.2 Charge Sensitive Amplifier Configuration

The CSA (Figure 2.2) can be seen as an operational amplifier (OPA) whose output is connected by a feedback capacitance to the inverting input, while the non-inverting input stays at some fixed potential, equivalent to ground for the small-signal analysis. The detector is connected to the inverting input. When a charge Q_0 is delivered by an ionization event, this charge does not accumulate on the detector capacitance, because the voltage across it is kept constant by the feedback loop, but flows to charge up the feedback capacitance C_f, giving at the output a step signal, whose amplitude is $-Q_0/C_f$. Since the input transistor is usually a JFET, providing very high input impedance, the feedback capacitance is the lowest impedance path to the signal.
The detector can be DC or AC coupled to the CSA. In the first case, the bias resistor, with its associated thermal noise, is absent, so that the overall noise performance is expected to be better. The leakage current flows directly through the feedback path, charging up the capacitance, exactly as the signal charge does. Thus the output voltage will increase with time, eventually reaching saturation. It is then necessary to provide a DC path for the current: the simplest way is placing a feedback resistor in parallel with the feedback capacitor. This resistor too contributes a noise current at the input of the CSA, but it can be easily made of larger value than the bias resistor when the latter needs to be integrated on the detector. The signal charge, initially stored on the feedback capacitor, is also discharged through the feedback resistor, causing the output to decay exponentially with time constant given by the product $R_f C_f$. An alternative solution, adopted in many practical cases, is the introduction in the feedback path of a reset transistor. The leakage current initially is integrated onto the feedback capacitance; to prevent saturation, at suitable times the reset transistor turns on and discharges the feedback capacitance through a low resistance path. This has the advantage of not introducing additional noise sources, if we can neglect the very low leakage current of the transistor in its OFF state. Furthermore, in integrated circuits, where space is a concern, a transistor is many times smaller than a resistor. This last kind of CSA is called a reset-type one.
In this work, only amplifiers with continuous draining of charge trough a feedback resistor will be considered. In detectors with many electrodes, such as strip or pix-

els, it is preferable to AC couple the sensor to the preamplifier, by interposing a large value capacitor between them. This will prevent high leakage currents originating in defective strips or pixels from affecting the working point of the front-end electronics. A bias resistor will also be required, in order to apply bias to the detector and provide a path for the leakage current. The coupling capacitance must be large enough to, on one hand, favourably compete with the detector and stray capacitances, and on the other hand, have an impedance, in the frequency range passed by the filter following the CSA stage, much lower than the bias resistor. Even with AC coupling, a feedback resistor in the CSA (or a reset transistor) will still be needed, in order to stabilize the input against stray charges and currents. However, this resistor can be taken of larger value than the bias resistor, so that its contribution to the noise will not be important. Consider now, the effect of the noise sources on the output of the CSA. Noise current sources at the input, indicated with the symbol $\frac{\mathrm{d}i^2}{\mathrm{d}f}$, charge up the feedback capacitance, giving an output noise voltage:

$$\frac{\mathrm{d}v^2_{out,i}}{\mathrm{d}f} = \frac{1}{\omega^2 C_f^2}\frac{\mathrm{d}i^2}{\mathrm{d}f} \tag{2.18}$$

Notice how the white spectral density of the current noise becomes strongly dependent on frequency. Noise voltage sources at the input ($\frac{\mathrm{d}v^2}{\mathrm{d}f}$) produce at the output a noise voltage which can be determined by considering the voltage divider given by the feedback and input capacitances. That voltage is then:

$$\frac{\mathrm{d}v^2_{out,v}}{\mathrm{d}f} = \frac{\mathrm{d}v^2}{\mathrm{d}f}\frac{(C_{in}+C_D+C_f)^2}{C_f^2} \tag{2.19}$$

where C_D is the capacitance of the detector, and C_{in} accounts for the input capacitance of the first JFET of the front-end electronics, as well as for the parasitic capacitance in the connection between detector and electronics.
These noise voltages, carrying informations on some of the relevant detector and front-end electronics features, come out from the CSA, which has low output impedance, and feed the following stage, the shaping amplifier. The latter performs a filtering in the frequency domain, with the purpose of enhancing the signal with respect to the noise. The shapers considered in our studies are time-invariant ones: that is their action does not depend explicitly on time.
If a step function enters the shaping circuit, it gives at the output a pulse of a defined "shape". In the frequency domain, if this shape has the Laplace Transform $F(s)$, then we have [11]:

$$F(s) = \frac{1}{s}T(s) \tag{2.20}$$

where $\frac{1}{s}$ is the Laplace Transform of the input step and $T(s)$ is the transfer function of the shaper, defined as the Laplace transform of the output pulse corresponding to a δ-pulse at the input [4]. With this definition, we can express the noise voltage

[4] In our definition, differing from the one reported in [11], the amplitude of output shape $f(t) = \mathscr{L}^{-1}(F(s))$ is normalized to unity. This has the advantage that the signal acquired by the amplification chain:

$$S = \frac{Q_0}{C_f} A\ MAX(\mathscr{L}^{-1}(F(s))) \tag{2.21}$$

with A the gain of the amplification stage, simplifies in: $S = \frac{Q_0}{C_f}A$

r.m.s. at the output of the shaping amplifier as:

$$\sigma_v^2 = \int_0^\infty \mathrm{d}\omega \, \frac{\mathrm{d}v_{out}^2}{\mathrm{d}f} |T(i\omega)|^2 = \tag{2.22}$$

$$\int_0^\infty \mathrm{d}\omega \, (\frac{\mathrm{d}i^2}{\mathrm{d}f} \frac{1}{\omega^2 C_f^2} + \frac{\mathrm{d}v^2}{\mathrm{d}f} \frac{(C_f + C_{in} + C_D)^2}{C_f^2}) |T(i\omega)|^2$$

where the contributions of both input noise current and input noise voltage have been considered. The signal to noise ratio is then:

$$\frac{S}{N} = \frac{Q_0/C_f}{\sqrt{\sigma_v^2}} = \frac{Q_0}{\sqrt{\int_0^\infty \mathrm{d}\omega \, (\frac{\mathrm{d}i^2}{\mathrm{d}f} \frac{1}{\omega^2} + \frac{\mathrm{d}v^2}{\mathrm{d}f} (C_f + C_{in} + C_D)^2) |T(i\omega)|^2}} \tag{2.23}$$

Notice that the C_f factors cancel each other. The ENC is the signal charge that makes $\frac{S}{N} = 1$. Expressed in coulomb, it is just the denominator; dividing it by the elementary charge q we get the more usual expression in terms of electrons. Then, summarizing, the contributions to the ENC of the various noise sources are found to be:

- current or parallel noise:

$$ENC_{parallel}^2 = \int_0^\infty \mathrm{d}\omega \, \frac{\mathrm{d}i^2}{\mathrm{d}f} \frac{|T(i\omega)|^2}{\omega^2} \tag{2.24}$$

- voltage or series noise, both white and flicker:

$$ENC_{series}^2 = \int_0^\infty \mathrm{d}\omega \, \frac{\mathrm{d}v^2}{\mathrm{d}f} (C_f + C_{in} + C_D)^2 |T(i\omega)|^2 \tag{2.25}$$

The above reported integration is often impracticable to perform analytically; with numerical techniques, however, it is easy to obtain an accurate result. Expressions derived for many types of shaping functions are available in literature [11].
Derivation of noise level can be carried on also in the time domain [28]. With this approach, the transfer function of the circuitry following the CSA is not used and the filtering action is replaced by the shaping one, then a frequency function is replaced by a time function. The calculation in the time domain begins considering the causality of noise process: during the processing of the signal, care should be taken of all noise events which occurred at previous times, whose effects last until measurement time.
Campbell theorem states that, at any time, the variance of a process is given by the sum of the squares of all preceding contributions at that time.
In our case, in particular, noise current is given by independently emitted charges, each one giving a step pulse at the output of the CSA which is then processed by the filtering stage: the "shaper". If a charge q is emitted at time t_0 and the shape transforms the step of magnitude $\frac{q}{C_f}$ at the output of CSA into a shape $\frac{q}{C_f} f(t - t_0)$, it gives a contribution to the measured signal at the measurement time t_m of:

$$v(t_m) = \frac{q}{C_f} f(t_m - t_0) \tag{2.26}$$

To calculate the variance of of the process, we must take into account all the noise events occurring at times $t_{0i} < t_m$ and sum up their square contributions at the time t_m. The variance of the process is then [28]:

$$\sigma_{v,i}^2 = \frac{q^2}{C_f^2}\Sigma_i f^2(t_m - t_{0i}) \tag{2.27}$$

and the symbol $\sigma_{v,i}^2$ stands for the variance of the output voltage, produced by noise current. Passing at the integration level, possible since the rate of arrival of the pulses is far greater than the times involved in any physical calculation:

$$\sigma_{v,i}^2 = \frac{q^2}{C_f^2} < n > \int_0^\infty \mathrm{d}t f^2(t) \tag{2.28}$$

Notice that the term $q^2 < n >= qI$ is one half of the shot noise. We can readily extend the concept and say that, limited for the current noise, whose pulses integrate onto the feedback capacitor, the noise at the output of the shaper is given by:

$$\sigma_{v,i}^2 = \frac{1}{C_f^2}\frac{1}{2}\frac{\mathrm{d}i^2}{\mathrm{d}f}\int_0^\infty \mathrm{d}t f^2(t) \tag{2.29}$$

If noise current, originated from δ pulses, produces steps at the output of the CSA, noise voltage, originated by δs too, transmits as it is at the output of the CSA; so there is an operation of derivation between them. If a δ gives a $f(t)$, a derivative of a δ, let's call it the doublet δ', gives the function $\delta' \otimes f(t) = f'(t)$. The noise contribution given by the voltage white noise is:

$$\sigma_{v,v}^2 = \frac{(C_{in} + C_f + C_D)^2}{C_f^2}\frac{1}{2}\frac{\mathrm{d}v^2}{\mathrm{d}f}\int_0^\infty dt f'^2(t) \tag{2.30}$$

and the symbol $\sigma_{v,v}^2$ stands for the variance of the output voltage, produced by voltage noise. Normalizing the shape at some fixed peculiar time, maybe the peaking time or some shaping time defining the curve, we can have an expression making explicit such times:

$$I_1 = \frac{1}{2}\int_0^\infty \mathrm{d}t\, f^2(t) = \tau a_1 \tag{2.31}$$

$$I_2 = \frac{1}{2}\int_0^\infty \mathrm{d}t\, f'^2(t) = \frac{a_2}{\tau} \tag{2.32}$$

if, of course, just one time is involved. Any shaper has its own numerical coefficients a_1, a_2; they have been tabulated for a large number of pulse response.
Unfortunately, calculation of ENC following the easier time domain is not trivial for a "coloured" noise spectral density, only white noise can be treated with this calculations. Then, in calculation of the 1/f noise contribution we must rely on frequency domain methods[5]. The $\frac{1}{f}$ noise comes from a voltage noise, as seen in Figure 2.1, and expressing it with the aid of the constant $A_{1/f}$:

$$\frac{\mathrm{d}v_{1/f}^2}{\mathrm{d}f} = \frac{A_{1/f}}{f} \tag{2.33}$$

[5]On the other hand, dealing with time variant shapers, only time domain approach is feasible.

To have the $\frac{1}{f}$ contribution to the total output noise v^2, just calculate the integral:

$$\sigma^2_{v,1/f} = \int_0^\infty \mathrm{d}\omega |T(i\omega)|^2 \frac{A_{1/f}}{f} \frac{(C_f + C_{in} + C_D)^2}{C_f^2} = \frac{(C_f + C_{in} + C_D)^2}{C_f^2} A_f \quad (2.34)$$

independent of the peaking time. It is a feature of the exact $\frac{1}{f}$ power noise spectral density, and does not depend on the filter involved. This comes out because the filtering action selects a passing band, whose lower and upper limit scale with the same factor, changing the peaking time of the shaper. Indeed, since $\int_{f_{down}}^{f_{up}} \mathrm{d}f \frac{1}{f} \sim \log \frac{f_{up}}{f_{down}}$, there are no frequency or time dependencies in the final results.
The total noise voltage can be expressed as:

$$\sigma_v^2 = \sigma_{v,i}^2 + \sigma_{v,v}^2 + \sigma_{v,\frac{1}{f}}^2 = \quad (2.35)$$

$$\frac{\mathrm{d}i^2}{\mathrm{d}f} \frac{1}{C_f^2} \tau a_1 + \frac{\mathrm{d}v^2}{\mathrm{d}f} \frac{(C_{in} + C_f + C_D)^2}{C_f^2} \frac{a_2}{\tau} + \frac{(C_f + C_{in} + C_D)^2}{C_f^2} A_f$$

Since the input signal is $\propto C_f^{-1}$, the ENC (expressed in number of electrons) takes the well known expression [28]:

$$ENC^2 = \frac{\mathrm{d}i^2}{\mathrm{d}f} \tau a_1 + \frac{\mathrm{d}v^2}{\mathrm{d}f} (C_f + C_{in} + C_D)^2 \frac{a_2}{\tau} + (C_f + C_{in} + C_D)^2 A_f \quad (2.36)$$

showing the three components, each having a different dependence on the peaking time τ, as shown in the example of Figure 2.3.

2.3 Source Follower Configuration

The configuration adopted for the readout employing a source-follower (SF) as first stage of signal processing is illustrated in Figure 2.4. The JFET J_C acts as a current source, setting the working point of J_S. The output of the SF is AC coupled by the capacitor C_A to an external charge-sensitive amplifier. The signal generator can be represented as a current source delivering a short pulse of current, typically shorter than a few tens of nanoseconds; in many cases this may be approximated by a δ-like pulse of current. The signal charge is integrated on the capacitance at the input of the SF rather than on the feedback capacitance of the CSA, and is then discharged through the RC equivalent circuit of the input node. R is the bias resistance, through which the leakage current flows. $C = C_D + C_{GD}$ is the total capacitance seen by input, with the important exclusion of the FET gate-source capacitance, which does not contribute because it is bootstrapped by source follower action (its two terminals have the same voltage). The small signal voltage at the gate of the JFET is then [29]:

$$v_{in}(t) = \frac{Q_0}{C_D + C_{GD}} e^{-\frac{t}{R(C_D + C_{GD})}} = \frac{Q_0}{C} e^{-\frac{t}{RC}} \quad (2.37)$$

with the Laplace Transform:

$$v_{in}(s) = Q_0 \frac{R}{1 + sR(C_D + C_{GD})} \quad (2.38)$$

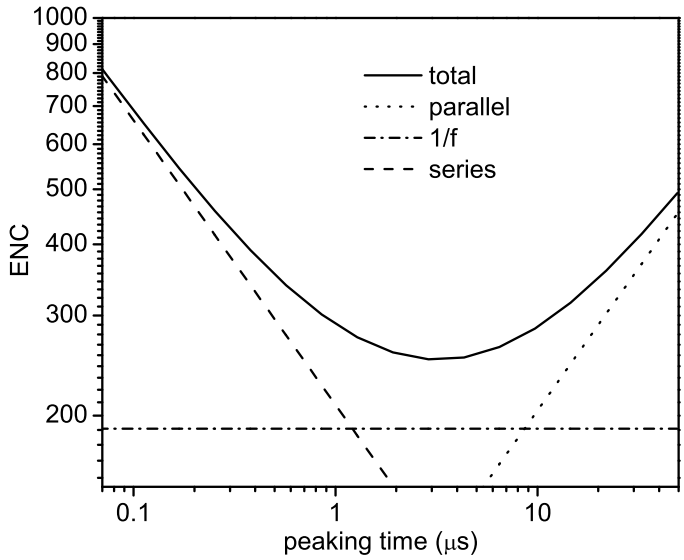

Figure 2.3: ENC (Equivalent Noise Charge in electrons r.m.s.) for a CSA followed by a triangular shaper, as a function of the shaper's peaking time. The parameters are: $a_1 = \frac{1}{3}$, $a_2 = 1$, $C_f + C_{in} + C_D = 10$ pF, $\frac{\mathrm{d}i^2}{\mathrm{d}f} = 2qI_{leakage}$ with $I_{leakage} = 1$ nA, $\frac{\mathrm{d}v^2}{\mathrm{d}f} = \frac{4kT\Gamma}{g_m}$ with $g_m = 13$ mS and $A_f = 10^{-12}\ V^2$.

The output voltage of the SF driving the capacitive load C_A can be expressed in the s domain as:

$$\frac{v_{in}(s)}{1 + \frac{g_S + g_C + sC_A}{g_{m,S}}} \tag{2.39}$$

Since the output conductances g_S, g_C of the two transistors are much smaller than the transconductance $g_{m,S}$ of J_S and in addition $sC_A << g_{m,S}$ (as will be discussed later), the output voltage of the SF closely follows the input. In the following, we will then assume that the output of the SF equals the input. The following stage of amplification is again a OPA in CSA configuration, but now the combination SF + CSA behaves as a voltage amplifier, giving at the output:

$$v_{out}(s) = -v_{in}(s)\frac{C_A}{C_f}\frac{sR_fC_f}{1 + sR_fC_f} = -Q_0R\frac{C_A}{C_f}\frac{sR_fC_f}{(1 + sRC)(1 + sR_fC_f)} \tag{2.40}$$

Transforming this back to the time domain:

$$v_{out}(t) = -\frac{Q_0}{C}\frac{C_A}{C_f}\frac{R_fC_fe^{-\frac{t}{RC}} - RCe^{-\frac{t}{R_fC_f}}}{R_fC_f - RC} \tag{2.41}$$

The output is the difference of two exponential falls, one with time constant RC and another with time constant R_fC_f. As mentioned in section above, it is difficult to integrate a very large value resistor on the detector, since this would increase to an intolerable extent the dead area, so it often comes out that $RC = R(C_D + C_{GD})$ is much smaller than the feedback time constant R_fC_f. The signal may then be

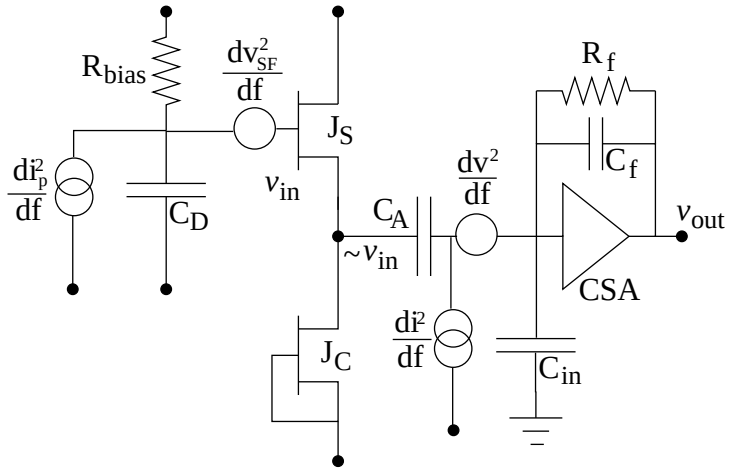

Figure 2.4: Schematics of a detector read-out by a Source Follower. Also shown, the noise sources.

approximated by a single exponential decay, with time constant set by the detector RC. If the shaping time is not much shorter than this time constant, a decrease in the pulse height occurs, with a consequent reduction in S/N.

With respect to the CSA configuration, the signal at the shaper's input is magnified by the factor $\frac{C_A}{C} = \frac{C_A}{C_D+C_{GD}}$, that could be made large choosing large values for the coupling capacitances C_A. The limit to the value of C_A comes from two considerations: first, the JFET J_S takes a time C_A/g_m to charge up C_A or, expressed in the frequency domain, the output impedance of the JFET (g_m^{-1}) must be by far smaller than $1/\omega C_A$; second, the value of the capacitor is limited by space constraints when it needs to be integrated on the silicon wafer. With respect to the CSA configuration, the signal at the shaper's input is, indeed, $\frac{C_A}{C_D+C_{GD}}$ times greater. The signal acquired is, considering unity gain of the shaper response:

$$S_{SF} = \frac{Q_0}{C_D + C_{GD}} \frac{C_A}{C_f} \tag{2.42}$$

Let's calculate the expected $\frac{\mathrm{d}v^2_{out}}{\mathrm{d}f}$ at the output of CSA, knowing the noise sources and the transfer function of the system. Just enumerate the noise sources [30]:

- $\frac{\mathrm{d}i_p^2}{\mathrm{d}f} = 2qI_L + 2qI_{gate} + \frac{4kT}{R}$ is the noise current at the input of the JFET J_S. It is made up by the leakage current of the detector, the leakage of the gate of the input JFET and the Johnson noise of the biasing resistor. As the signal does, it passes through the RC of the detector, giving by generalized Ohm law a small signal voltage at the gate of the FET. Then, at the output of the CSA:

$$\frac{\mathrm{d}v^2_{out,i_p}}{\mathrm{d}f} = \frac{\mathrm{d}i_p^2}{\mathrm{d}f}(\frac{C_A}{C_f})^2 \frac{R^2}{1 + (\omega R(C_D + C_{GD}))^2} \tag{2.43}$$

  Two case are worth distinguishing: at short shaping times compared with RC, that is at high frequency, the denominator of the expression above is proportional to ω^2, behaving as parallel noise:

$$\frac{\mathrm{d}v^2_{out,i_p}}{\mathrm{d}f} = \frac{di_p^2}{df}(\frac{C_A}{C_f})^2 \frac{1}{\omega^2(C_D + C_{GD})^2} \tag{2.44}$$

R_{Bias}	1M	$g_{m,S}$	5 mS
C_D	5 pF	$g_{m,C}$	1 mS
C_{GD}	2 pF	g_m	10 mS
C_{in}	15 pF	$A_{f,S}$	0
C_A	15 pF	A_f	$10^{-12}V^2$

Table 2.1: Unless differently specified, parameters entering noise expressions for the SF read-out, used to calculate the plots 2.5 through 2.8.

on the other hand, at long shaping times, or low frequencies, the ω^2 dependence disappears, as in the case of series noise:

$$\frac{\mathrm{d}v^2_{out,i_p}}{\mathrm{d}f} = \frac{\mathrm{d}i^2_p}{\mathrm{d}f}(\frac{C_A}{C_f})^2 R^2 \tag{2.45}$$

Notice how also this noise is amplified by the ratio $\frac{C_A}{C_f}$, exactly as the signal is.

- $\frac{\mathrm{d}v^2_{SF}}{\mathrm{d}f} = 4kTR_{Gate,S} + 4kT\frac{\Gamma}{g_{m,S}} + \frac{A_{\frac{1}{f},S}}{f} + 4kT\Gamma\frac{g_{m,C}}{g^2_{m,S}}$ is the series noise of the input devices (the two JFET of the source follower), comprehensive of the 1/f noise of the J_S, that is reproduced identical to the drain of J_C and gives a contribution:

$$\frac{\mathrm{d}v^2_{out,SF}}{\mathrm{d}f} = \frac{\mathrm{d}v^2_{SF}}{\mathrm{d}f}(\frac{C_A}{C_f})^2 \tag{2.46}$$

- $\frac{\mathrm{d}v^2}{\mathrm{d}f} = 4kTR_{Gate} + 4kT\frac{\Gamma}{g_m} + \frac{A_{1/f}}{f}$ is the series noise of the CSA amplifier, essentially the noise of input FET, referred to the gate of its input FET. It gives a contribution to the output:

$$\frac{\mathrm{d}v^2_{out,v}}{\mathrm{d}f} = \frac{\mathrm{d}v^2}{\mathrm{d}f}(\frac{C_A + C_{in} + C_f}{C_f})^2 \tag{2.47}$$

where C_{in} is the input capacitance of the input FET plus parasitic capacitance in the connections from C_A to CSA. Note that for applying the formula of the voltage divider the impedance must be at ground and C_A does not seem to be at; instead, since the input impedance of J_S is low, practically we can consider C_A at ground.

- $\frac{\mathrm{d}i^2}{\mathrm{d}f} = \frac{4kT}{R_f}$ is the parallel noise at the input of the CSA amplifier, essentially the noise of the feedback resistor. It contributes as:

$$\frac{\mathrm{d}v^2_{out,i}}{\mathrm{d}f} = \frac{\mathrm{d}i^2}{\mathrm{d}f}\frac{1}{(\omega C_f)^2} \tag{2.48}$$

- $\frac{\mathrm{d}v^2_{shaper}}{\mathrm{d}f}$: not always we can neglect the noise introduced by the shaper, we will see later a case when this really happens. Obviously, being at the output, it contributes as it is at the output.

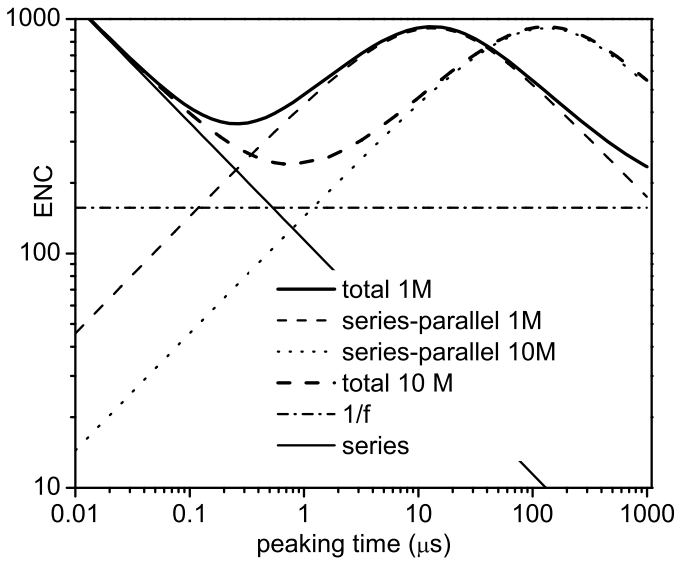

Figure 2.5: Model for the noise expected in a detector read-out by a SF; the parameters used are those listed in table 2.1. Series, 1/f and bias resistor noise contributions are shown, as well as their sum. Bias resistors of 1 MΩ and 10 MΩ are considered.

Next step, let's pass these noise spectral densities through the shaper:

$$\sigma_v^2 = \int_0^\infty \mathrm{d}\omega |T(i\omega)|^2 \frac{\mathrm{d}v_{out}^2}{\mathrm{d}f} \tag{2.49}$$

Many of these contributions may be calculated in the time domain, since they are originated from white noise and have expressions similar to the ones described in the CSA case. The most interesting part is the one with the peculiar denominator $1+\omega^2(R(C_D+C_{GD}))^2$, behaving as voltage or current noise depending on whether the shaping time is greater or smaller than the input time constant.
We can take advantage of the integral expression calculated for the CSA case, to find out the ENC contribution of each noise source, shown in Figure 2.5.

- $\frac{\mathrm{d}i_p^2}{\mathrm{d}f}$ is the noise coming from the "parallel" sources before the first amplification stage, the SF itself. The major contribution is easily given by the bias resistor. Let's consider the two limiting cases: at high frequency, this noise is a parallel one and:

$$ENC_{i_p,\omega\to\infty}^2 = (2qI_L + 2qI_{gate} + \frac{4kT}{R})a_1\tau \tag{2.50}$$

while at low frequency:

$$ENC_{i_p,\omega\to 0}^2 = (2qI_L + 2qI_{gate} + \frac{4kT}{R})(C_D + C_{GD})^2 R^2 \frac{a_2}{\tau} \tag{2.51}$$

Considering that usually we try to keep the shaping times small, in order to increase the acquisition rate, this noise is essentially parallel and the expression $ENC_{i_p,\omega\to\infty}^2$ holds. It turns out that the expression is identical to the

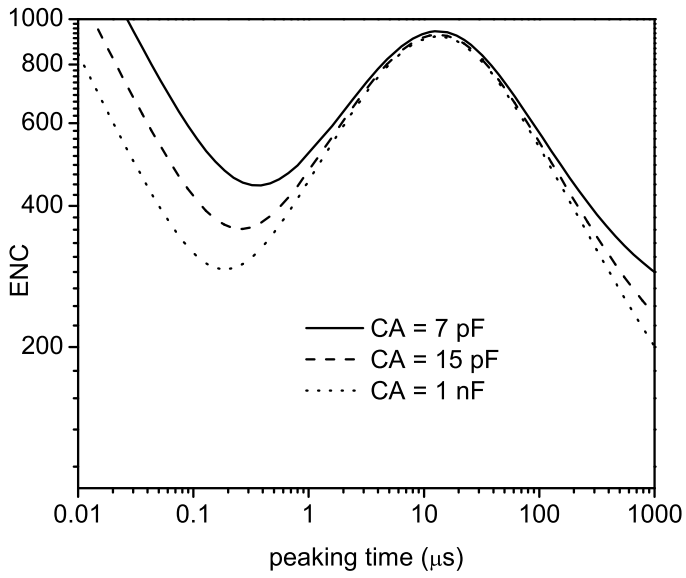

Figure 2.6: Effect of the coupling capacitance C_A on ENC: plots for $C_A = 7$ pF, 15 pF and 1 nF (practically infinite).

one for the CSA: the noise and the signal are indeed amplified by the same amount and the capacitances, different in the two cases, play no role.

In general, the complete expression is[6]:

$$ENC_{i_p}^2 = \frac{R^2}{\tau}\frac{\mathrm{d}i^2}{\mathrm{d}f}(1 + \frac{a}{2}(-3 - e^{-\frac{2}{a}} + 4e^{-\frac{1}{a}})) \tag{2.60}$$

with a = $\frac{R(C_D+C_{GD})}{\tau}$.

- $\frac{\mathrm{d}v_{SF}^2}{\mathrm{d}f}$ is the voltage noise coming from the two JFETs making the SF. Separating the white contribution from the 1/f one:

$$ENC_{v_{SF},white}^2 = \tag{2.61}$$

$$(4kTR_{Gate,S} + 4kT\frac{\Gamma}{g_{m,S}} + 4kT\Gamma\frac{g_{m,C}}{g_{m,S}^2})(C_D + C_{GD})^2\frac{a_2}{\tau}$$

$$ENC_{v_{SF},1/f}^2 = A_{f,S}(C_D + C_{GD})^2 \tag{2.62}$$

These contributions are not present in the CSA case.

- $\frac{\mathrm{d}v^2}{\mathrm{d}f}$ is the voltage noise coming from the external amplifier, configured as a CSA one but behaving as a voltage amplifier; again, separating the white from the 1/f noise

$$ENC_{v,white}^2 = \tag{2.63}$$

$$(4kTR_{Gate} + 4kT\frac{\Gamma}{g_m})(\frac{C_A + C_{in} + C_f}{C_A})^2\frac{(C_D + C_{GD})^2 a_2}{\tau}$$

[6] Unfortunately, to come to an exact and analytical solution, we must calculate by hand the integral:

$$ENC_{i_p}^2 = \frac{\mathrm{d}i^2}{\mathrm{d}f}\int_0^\infty \mathrm{d}\omega|T(\omega)|^2\frac{R^2}{1 + (\omega R(C_D + C_{GD}))^2} \tag{2.52}$$

Considering a triangular shaper, $|T(\omega)|^2 = \frac{2}{\pi(\omega\tau)^2}(1 - \cos(\omega\tau))^2$ and setting $a = \frac{R(C_D+C_{GD})}{\tau}$ and $x = \omega\tau$, the integral "simplifies" to the new one:

$$ENC_{i_p}^2 = \frac{\mathrm{d}i^2}{\mathrm{d}f}\frac{2R^2}{\pi\tau}\int_0^\infty \mathrm{d}x\frac{(1 - \cos x)^2}{x^2(1 + (xa)^2)} \tag{2.53}$$

The integral, let's call it "I", can be proficiently decomposed to:

$$I = \int_0^\infty \mathrm{d}x\frac{(1 - \cos x)^2}{x^2} - a^2\int_0^\infty \mathrm{d}x\frac{(1 - \cos x)^2}{1 + (ax)^2} \tag{2.54}$$

Solving with some mathematical methods or with the aid of an integral table, the integrals give:

$$\int_0^\infty \mathrm{d}x\frac{(1 - \cos x)^2}{x^2} = \frac{\pi}{2} \tag{2.55}$$

$$\int_0^\infty \mathrm{d}x\frac{1}{1 + (ax)^2} = \frac{\pi}{2a} \tag{2.56}$$

$$\int_0^\infty \mathrm{d}x\frac{\cos x}{1 + (ax)^2} = \frac{\pi}{2a}e^{-\frac{1}{a}} \tag{2.57}$$

$$\int_0^\infty \mathrm{d}x\frac{\cos^2 x}{1 + (ax)^2} = \frac{\pi}{4a}(1 + e^{-\frac{2}{a}}) \tag{2.58}$$

summing up to:

$$I = \frac{\pi}{2} + \frac{a\pi}{4}(-3 - e^{-\frac{2}{a}} + 4e^{-\frac{1}{a}}) \tag{2.59}$$

The contribution comes to its limiting value of

$$(4kTR_{Gate} + 4kT\frac{\Gamma}{g_m})\frac{(C_D + C_{GD})^2 a_2}{\tau} \tag{2.64}$$

increasing the coupling capacitance C_A, being Eq. 2.63 a monotonically decreasing function of this parameter, as can seen in Figure 2.6. Comparing with the expression for the CSA:

$$ENC^2_{v,CSA} = (4kTR_{Gate} + 4kT\frac{\Gamma}{g_m})\frac{(C_D + C_{in} + C_f)^2 a_2}{\tau} \tag{2.65}$$

we realize that deciding which one is greater depends strongly on the value of the capacitance involved. Large C_{in} make the SF better, and then making that configuration preferable when parasitic capacitance, due to long wire connection to the front-end amplifier, are not negligible. The same holds considering the pink noise of the same second amplification stage:

$$ENC^2_{v,1/f} = A_f(\frac{C_A + C_{in} + C_f}{C_A})^2(C_D + C_{GD})^2 \tag{2.66}$$

Deciding if it is better than CSA noise $(C_D + C_{in})^2 A_{\frac{1}{f},1}$ depends again on the capacitances.

- $\frac{\mathrm{d}i^2}{\mathrm{d}f}$ is the white noise coming from the Johnson noise of the feedback resistor R_f :

$$ENC^2_i = \frac{4kT}{R_f}\frac{(C_D + C_{GD})^2}{C_A} a_1 \tau \tag{2.67}$$

With C_A larger than the input capacitance, this ENC can be made smaller than the one in the CSA case.

At this point we must be able to compare the noise performances of the two types of detector-amplifier chains with some numerical results.

2.4 Theoretical comparison of CSA and SF

As seen in the above sections, the parameters to be managed are a lot; so we are led to make some approximation. Since this work is aimed to state the performances of detector for high energy physics, only short peaking times are of interest, so the noise $\frac{\mathrm{d}i_p}{\mathrm{d}f}$ can be seen as parallel. The detector are supposed to have a very large capacitance, deriving from gangling together several ones, and then the C_{GD} can be neglected. The same holds for C_f, that should be practically zero in every application. For good devices, series resistances of the JFET gate are small; 1/f noise can be neglected in first instance to simplify the overall calculations. $g_{m,C}$ of the current source is less than $g_{m,S}$, then also the noise coming from J_C, can be neglected.

Consider, then, only the contributions coming from the thermal noise of the channels of JFETs:

$$ENC^2_{CSA} = (C_D + C_{in})^2 4kT\frac{\Gamma}{g_m}\frac{a_2}{\tau} \tag{2.68}$$

$$ENC_{SF}^2 = C_D^2 4kT\Gamma((\frac{C_A + C_{in}}{C_A})^2 \frac{1}{g_m} + \frac{1}{g_{m,S}})\frac{a_2}{\tau} \tag{2.69}$$

We are searching the condition for which the SF is better than the CSA: $ENC_{CSA}^2 > ENC_{SF}^2$; this translates in a condition for the g_m:

$$g_{m,S} > \frac{g_m}{(1 + \frac{C_{in}}{C_D})^2 - (1 + \frac{C_{in}}{C_A})^2} \tag{2.70}$$

According to the expression above, when $C_A = C_D$ then $g_{m,S}$ should be infinite for the SF to be better than CSA, i.e. the J_S must be noise free. In the very case of $C_A < C_D$ the expression shows that every $g_{m,S} \geq 0$ make the SF better, but this is obviously due to a singularity of the function $g_{m,S}(C_A)$ for $C_A = C_D$. Then, the condition is that $C_A > C_D$; it can be shown that even neglecting the thermal noise in the channel of J_S, the very white voltage noise of the CSA makes the SF configuration worst if $C_A > C_D$. This because the signal is under amplified by the factor $\frac{C_A}{C_D} < 1$. In Figure 2.7, with all the parameters listed in table 2.1 and not just considering the noise coming from some JFETs, the plots shows how the SF works better than the CSA. The minimum $g_{m,S}$, according to the formula, is $\frac{g_m}{12} = 0.83$ mS. As expected, in the time range where series noise dominates, i.e. low shaping times, the SF configuration gives better noise performances than CSA. The region in which the superiority of the SF holds less is the one where the parallel noise of the bias resistance begins to dominate: this contribution, indeed, does not depend on both capacitances or transconductances. At very high peaking times, however too long to be practicable in whatever application, this bias resistance begins to contribute as series noise, making SF better and better with respect to the CSA.

The introduction of integrated JFETs into the detector substrate is, of course, a complication of the process, requiring additional dopant implantations; but large C_{in}, sum of the input capacitance of the first FET and of parasitic capacitances, may justify it. It is worth plotting the expected noise in function of this parameter for the two cases, at some fixed peaking time, possibly when series noise dominates - the other regions are not interesting. One typical result is plotted in Figure 2.8: for C_{in} smaller than 13 pF, the CSA is still better, then it worsens very rapidly with respect to the SF. In this case, indeed, the C_{in} enters in the noise expressions never alone, but weighted with the C_A, that must be made as high as possible, in the ratio $C_A + C_{in}/C_A$.

2.5 Technological consideration

The supposed supremacy of the SF on CSA depends on many parameters and the situation described above can be considered just as a first approximation. More, the SF needs some devices in the same silicon wafer of the detectors, compelling with them for the available space and/or producing some power dissipation. Let's consider some limitations.

R_{bias}

Large R_{bias} must be chosen to decrease its Johnson noise. To make a large resistor is always an issue, since bias resistors are made with polysilicon whose resistivity per square ρ_s is of the order of $10 - 20$ $k\Omega/\square$. It is common, as in the previous

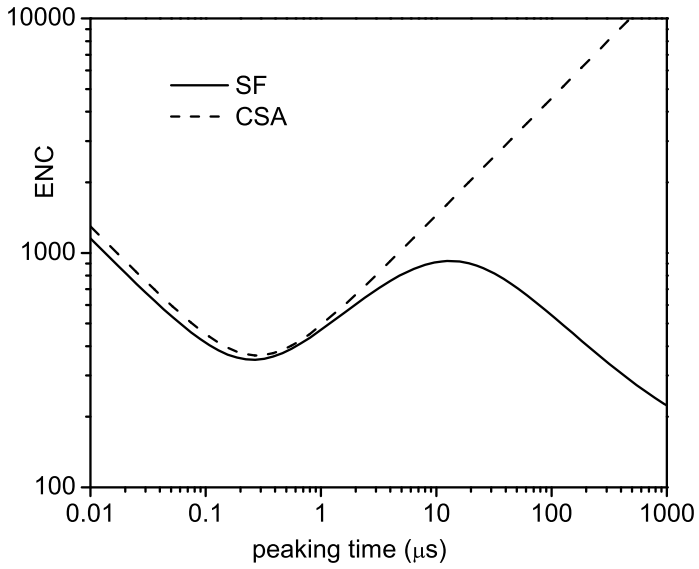

Figure 2.7: Comparison of the expected ENC for SF and CSA read-out versus peaking time, with the two configurations sharing the same parameters as listed in table 2.1.

examples of silicon strip detectors, have bias resistors in a snaky configuration, to increase their length. Anyway, the occupied surface is large and this fact puts a higher limit to their value. However, considering low peaking times, parallel noise coming from it may become low compared with the series sources of the channel thermal noises of the FETs; this can be the ultimate noise to cope with in SF.

C_A

Large capacitances, as C_A should be, require space. C_A are integrated on the wafer and are made of a thin layer of SiO_2 between an external metal and a polysilicon layer. The geometrical value, per unit area, is: ϵ_{SiO_2}/t_{ox}, holding, for an oxide thickness of 200 nm [7], 0.17 fF/μm^2. To have a "small" coupling capacitance of just 10 pF, the area needed is as large as 20k μm^2; having a pitch, in a strip detector, of 100 μm, in first approximation, considering complete area covering, we need capacitances 600 μm longer. It is not a negligible surface, and it comes in competition with the electrodes for charge collection.

JFET

It is possible to fabricate working JFET with the required characteristic of capacitance and trasconductance, having a small pitch too. A possible geometry is the interdigitated one, allowing high length/width ratios. In the plots above, we neglected the series contribution of the gate resistance, coming from the unmetallized regions of the gate implant, which could be even greater than the thermal

[7] the dielectric constant for the Silicon Oxide is 3.4 10^{-13} F/cm.

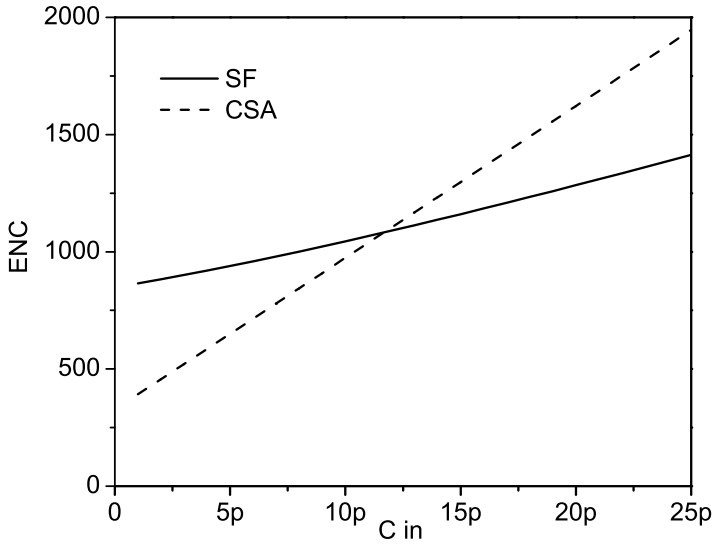

Figure 2.8: Comparison of the expected ENC for SF and CSA read-outs versus the input capacitance C_{in}, sum of the input capacitance of the CSA and of the parasitic capacitances. The peaking time is 100 ns, the other parameters are those listed in table 2.1.

noise of the channel.

Chapter 3

Experimental Set-up for Noise Measurements

3.1 Detector Assembly

After testing the electrical properties of the detectors, in order to select good quality devices and measure the static parameters relevant for noise measurements, they are glued upon custom made fiberglass supports. These are designed to allow connecting by wire bonds all relevant electrodes of the device to externally accessible terminals.
The detector support is mounted inside a mild steel shielding box which also contains the preamplifier, and is provided with BNC coaxial connectors for interfacing with the measuring instruments and voltage supplies. All connections inside the shielding box between the device terminals and the preamplifier or the BNC connectors to the external world are made with short wires provided by miniature pins, fitting into mating receptacles, so that the connections are quickly reconfigurable without soldering.

A photograph of the shielding box with two ALICE-type microstrip sensors inside is shown in Figure 3.1, while a schematic of the whole system is reported in Figure 3.2.

3.2 Preamplifier

The charge sensitive preamplifier used in this work is an Amptek Model A250 [1], equipped with an external input JFET type 2SK152 [2] and mounted on a dedicated evaluation board supplied by Amptek. The latter is a 4.5 cm×4.5 cm Teflon-insulated PCB holding the hybrid preamplifier, the input FET, a test input capacitor and power supply filtering. The preamplifier is placed in the same shielding box holding the sensors. The input lead is connected to the FET gate, which is kept at a voltage of +0.4 V by the feedback loop, while the source is at ground potential and the drain is kept at 3 V by the internal circuitry of the A250. The transconductance of the input FET has been measured to be high (13 mS) and its gate capacitance is matched to the strip capacitance of the ALICE detectors

[1] www.amptek.com/a250.html
[2] the datasheet can be found in www.interfet.com/pdf/DS_2SK113_P44.pdf

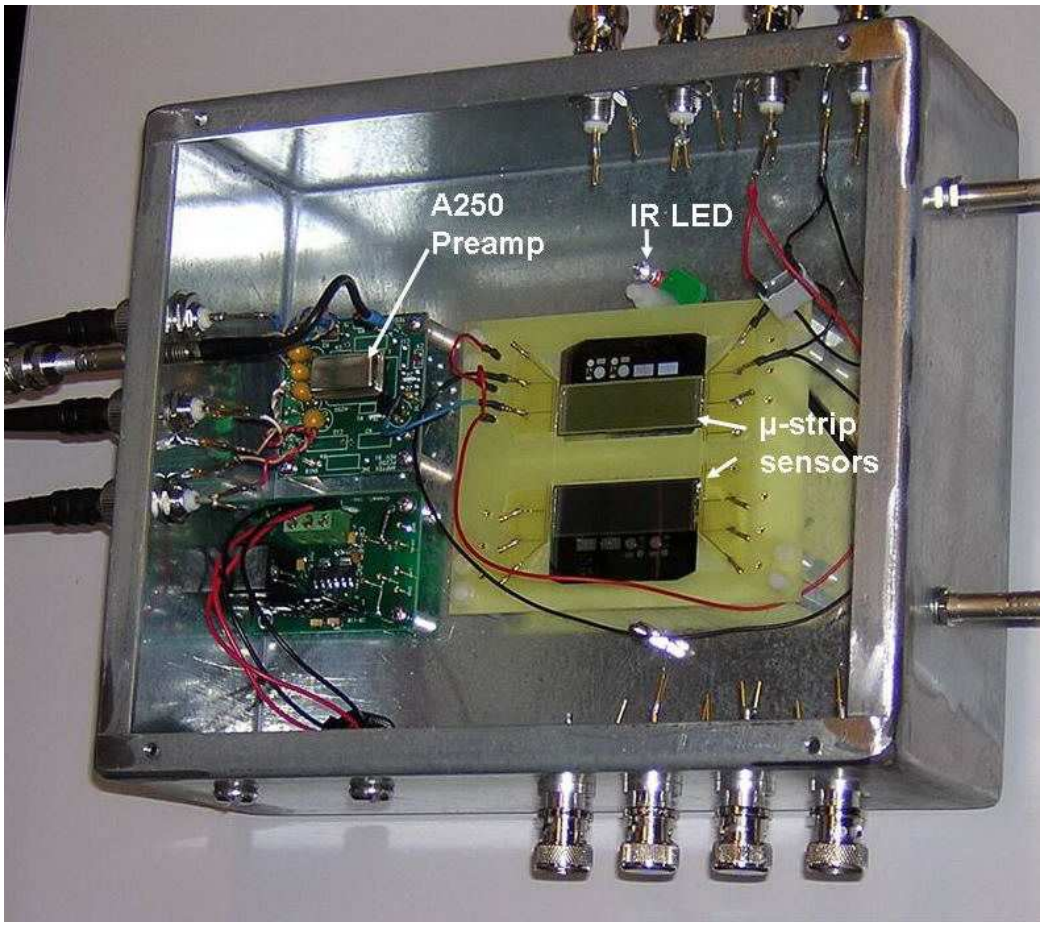

Figure 3.1: Picture of the shielding box, showing two ALICE-type test detectors assembled on a fiberglass support, the board hosting the Amptek A250 preamplifier and the wire connections between the components.

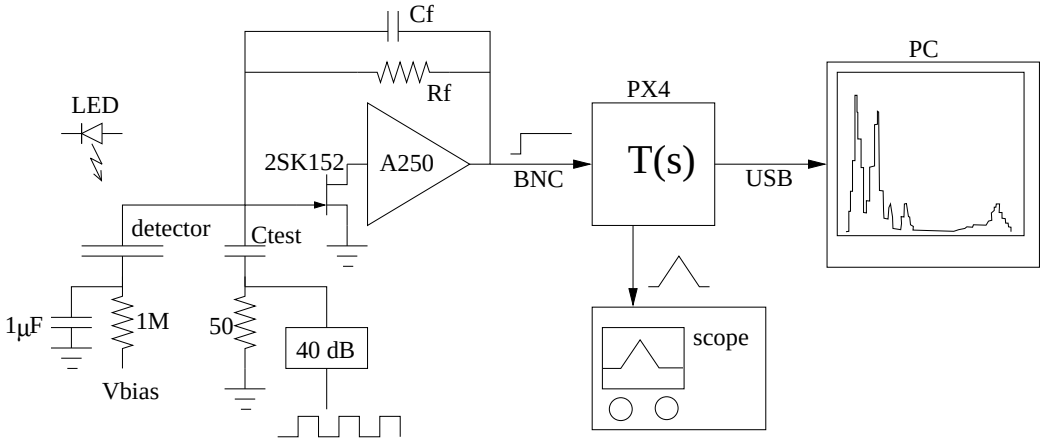

Figure 3.2: Experimental set-up for noise measurements: the standard readout chain composed of the charge sensitive preamplifier, the shaper and the acquisition system is shown. In this case the detector, represented by its capacitance, is DC coupled to the preamplifier.

($\sim$ 10 pF). The feedback resistance is easily measured by connecting an ohmmeter between JFET input and preamplifier output; its value is 300 MΩ, as specified.

The shape of the output signal should be a single exponential decay whose time constant is given by the product of the RC elements in the feedback loop; the specs give 300 MΩ and 1 pF, we observe instead a little undershoot and a dominant time constant of $\sim 400\,\mu$s. From this, a value of $\sim$1.3 pF can be deduced for the feedback capacitance C_f. The nominal value is 1 pF, the difference being likely due to parasitics in the PCB.

A test capacitance is provided on the board, with its 50 Ω termination; through accurate calibration with X-rays (see Section 3.4), its value has been found to be 2.28 pF.

By means of noise measurements made with open input (no detector connected), it is possible to extract some parameters of the amplifier which can then be used for the other noise measurements.
The input capacitance $C_{in} = C_{FET} + C_{test} + C_{parasitic}$ is $\sim$12 pF.
The equivalent series resistance of the FET gate is 60 Ω.
The coefficient of the $1/f$ noise, caused essentially by the series flicker noise voltage of input FET, is $A_f = 1.6 \cdot 10^{-12}\,\mathrm{V}^2$, for the shaper used. The gate leakage current is negligible; the transconductance is taken as measured (13 mS), while the parallel noise current contribution of the feedback resistor R_f can be represented by the thermal noise of a 200 MΩ resistance. The difference with the static measured value of 300 MΩ may be due to additional noise current sources in the preamplifier circuit.

3.3 Shaping and Acquisition System

The Amptek PX4 is a single channel digital shaper with triggering and data acquisition functions [3]. It takes at the input a step pulse followed by an exponential fall.

An analog prefilter section amplifies the signal, performs Pole-Zero cancellation and cuts down the decay constant of the signal to 3.2 μs. The output of the prefilter is sampled and digitized at 20 MHz rate by a flash ADC. Then the digital section performs the functions of trapezoidal shaping, triggering and acquisition of the peak value of the shaped signal. All PX4 settings are controlled via software. Data are sent to a PC and settings are imported through a USB interface.

A good Pole-Zero compensation of the input signal is required to get at the output of the filter the correct trapezoidal shape. Because for the Pole-Zero cancellation to be effective the decay time of the input signal must exceed 36 μs, this poses a restriction on the input signals that can be correctly processed by the PX4. This limitation will become important in the case of signals from detectors read out by a source follower (Chapter 5), and will require a modification of the relations developed in Chapter 2 for the determination of the equivalent noise charge.

The shaping is trapezoidal with peaking time and flat top width selectable via software. The peaking time ranges from 0.8 μs to 102 μs[4]. The flat top width range depends on the peaking time; in this work we tried to keep the flat top at the minimum value allowed by the PX4, since there is no risk of ballistic deficits

[3] www.amptek.com/px4.html

[4] A triangular shaper with peaking time τ gives approximately the same noise of a gaussian shaper with shaping time 2.2 times shorter.

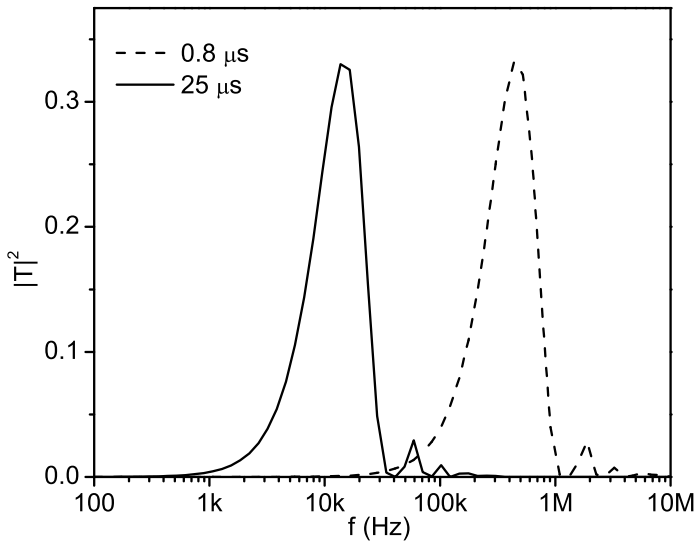

Figure 3.3: Plot of $|T(\omega)|^2$ for two triangular shapers with peaking times 0.8 μs and 25 μs. The filtering function peaks at $f \simeq 0.37/\tau$.

coming from slow charge collection inside the detector.

The Laplace Transform for a trapezoidal waveform in the time domain is:

$$F(s) = \frac{(-1 + e^{-s\tau})(-1 + e^{-s(FT+\tau)})}{\sqrt{2\pi}\,\tau\, s^2} \tag{3.1}$$

where τ is the peaking time of the trapezoid and FT the flat top width.

Since the trapezoid is the response of the system to an input step, whose Laplace Transform is s^{-1}, the transfer function of the shaper in the s domain is:

$$T(s) = sF(s) = \frac{(-1 + e^{-s\tau})(-1 + e^{-s(FT+\tau)})}{\sqrt{2\pi}\,\tau\, s} \tag{3.2}$$

or, in the real variable ω (the imaginary part of s):

$$|T(\omega)|^2 = 4\frac{(1 - \cos(\omega\tau))(1 - \cos(\omega(FT + \tau))}{2\pi(\omega\tau)^2} \tag{3.3}$$

Figure 3.3 shows a plot of the square of the modulus of the transfer function $T(\omega)$ of a triangular shaper, for two values of the peaking time τ.

From Equation 3.3 we can calculate the ω value corresponding to the peak of $T(\omega)$, for a triangular shaper (FT=0) with peaking time τ:

$$\omega_{peak} \simeq 2.3/\tau \quad \text{or} \quad f_{peak} \simeq 0.37/\tau \tag{3.4}$$

This relationship can be used to estimate the approximate frequency interval corresponding to a given range of peaking times, or vice versa.

By performing the integrals I_1 and I_2 defined by Equations 2.31 and 2.32, we can calculate the shaper coefficients for white parallel noise and for white series noise. Because two times are involved in the definition of the trapezoid, we expect both times to enter into the expressions for the noise coefficients. Indeed, in Equation 2.36 $a_1\tau$ gets replaced by $\frac{\tau}{3} + \frac{FT}{2}$, while $a_2 = 1$. The FT time does not enter in the noise expression for series noise[5]. Notice that the flat top only makes things worse, since it increases the shot noise component. This motivates our choice of setting FT to the lowest allowed value.

For the parameter A_f characterizing the $1/f$ noise, we rely on the values measured with open preamplifier input. In our shaped pulses, the flat top width (the minimum value allowed) does not increase proportionally to the peaking time: the ratio FT_{min}/τ decreases for longer peaking times. Indeed, the integral $\int \mathrm{d}\omega |T(\omega)|^2/\omega$ – which is proportional to the series $1/f$ noise – ranges from 0.53 (in the case of $\tau = 0.8$ μs and FT = 0.2 μs) to 0.46 (in the cases in which $\tau >>$ FT). For long peaking times, the flat top is short compared to τ: the trapezoidal shape looks like a triangular one and A_f can be taken as constant.

A DAC in the PX4 converts the digital shaped signal into an analog signal for visual inspection on a scope.

A high number of equal charge signals at the input result, on the screen of a PC, in a gaussian amplitude distribution whose standard deviation σ, calculated by the PX4 software, is proportional to the noise. Of course a preliminary calibration must be performed to set the gain of the whole amplification chain.

3.4 Signal Generation and Gain Calibration

In order to measure the absolute level of noise – usually expressed in terms of the Equivalent Noise Charge (ENC) at the amplifier input – we need to calibrate the overall gain of the preamplifier-shaper-ADC system, i.e. determine the output signal amplitude (or ADC channel number) corresponding to a given charge at the input. The best way to perform this calibration is by using monochromatic X-rays of suitable energy from a radioactive source to generate a precisely known charge signal inside the detector.

An ^{241}Am source is particularly suited for calibrating silicon detectors. It emits several monochromatic lines, the main ones having the energies shown in Table 3.1. The highest energy ($\simeq$ 60 keV) line is well separated from the others and it generates in silicon a charge of 59.5 keV/3.6 eV $\simeq$ 16.5 ke $\simeq$ 2.65 fC, or about 2/3 of the charge released by a m.i.p. traversing 300 μm of silicon. Unfortunately, as Table 3.1 shows, the detection efficiency for the 60 keV line in 300 μm of silicon is rather low and it could take time to acquire a spectrum with a sufficient statistics. Moreover, although photons of the low energy lines interact principally by photoelectric effect, as can be seen in figure 3.4, the Compton cross section for 60 keV photons becomes comparable with the photoelectric cross section. This produces a shoulder on the low-energy side of the 60 keV peak, reducing statistics in the peak and making the Gaussian fit less straightforward.

[5] As Equation 2.32 explicitly shows, parts of the waveform having zero time derivative (e.g. the flat top of a trapezoidal shape) do not contribute to that integral.

energy (keV)	emission fraction (%)	mass attenuation coefficient (cm^2/g)	linear attenuation coefficient (cm^{-1})	interaction probability (%)	interaction fraction (%)
13.9	13	12.1	28.2	57.1	7.42
17.6	20.2	6.5	15.1	36.5	7.37
21.0	5.20	3.87	9.01	23.7	1.2
26.3	2.40	2.11	4.91	13.7	0.33
33.2	0.12	1.07	2.49	7.20	0.01
59.5	35.7	0.321	0.75	2.22	0.79

Table 3.1: Interaction of the most intense Americium X-ray lines in 300 μm of Silicon. The mass attenuation coefficients are taken from Figure 3.4, the linear attenuation coefficient μ is the product of the mass attenuation in $cm^2\,g^{-1}$ with the density of Si ($\rho_{Si} = 2.33\ g\,cm^{-3}$). The "interaction probability" is $1 - e^{-\mu d}$, where d =300 μm. The "interaction fraction" is the product of the emission fraction of the line with its interaction probability.

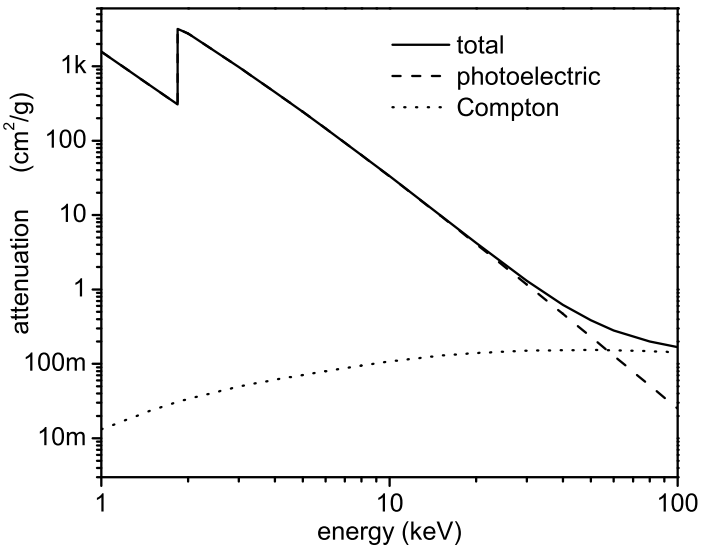

Figure 3.4: Mass attenuation coefficients in silicon of X-rays from 1 keV to 100 keV (range of Americium lines). Compton and photoelectric processes are shown, as well as their sum (from http://physics.nist.gov/PhysRefData/Xcom/html/xcom1.html).

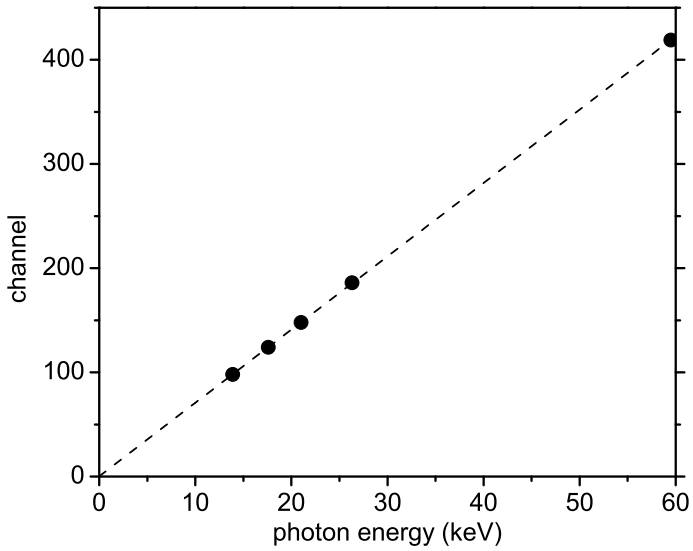

Figure 3.5: Peak position in channels of the most relevant Americium source of Table 3.1, taken from spectrum in Figure B.1. Also shown the fit to the points, giving a gain of 7.0 channel/keV and an offset of 0.3 channels, compatible with zero.

For some detectors, in particular those with narrow strips (with large perimeter/area ratio for the detecting elements), in a non negligible fraction of the events the charge can be spread over two adjacent electrodes, leading to higher background in the spectrum and more difficult fits, which need to be made only on the high-energy side of the peak.
By using a simple diode with a circular or square shape, having minimal perimeter/area ratio, it is possible to get cleaner Gaussian peaks, allowing to accurately determine the gain of the amplification chain.
Notice that we actually need two lines for this purpose, in order to find the zero of the energy scale, since there might be an offset level somewhere in the amplification chain or in the ADC conversion. Usually, the zero-energy channel can be determined by acquiring "events" with no signal in the detector, but with the PX4 this is not possible, since it cannot be triggered by an external signal. However, by using two of the Americium lines, or pulser-generated signals (see below), we verified that in all cases, no matter the detector used, zero input charge corresponds to channel number zero.
The data in Figure 3.5 show the linearity of the correlation of the channel number with the energy of the absorbed Am photons, according to the main peaks mentioned in Table 3.1. The actual measurements are reported in Appendix B, both for the single diode and for the different microstrip detectors.

The A250 preamplifier board provides a test capacitance, terminated with 50 Ω, which can be fed with a square wave of amplitude V_{square} to inject a known charge $Q_0 = C_{test}V_{square}$ into the amplifier input. For example, if the capacitance is 2 pF, pulsing it with a 2 mV square wave produces a charge injection of 4 fC, close

to the charge release of a m.i.p. in 300 μm of silicon. The waveform generator employed was not able to generate such small amplitudes (and even if it could, the noise level on such low amplitude would be significant). Therefore, a wave of much larger amplitude has been generated, and attenuated by 40 dB using a passive attenuator[6].

By comparing the positions of the 60 keV peak and of the peaks generated by injecting charge through the test capacitance, we can accurately determine the value of the test capacitance, including small parasitics in the PCB layout[7]. It is then possible to perform noise measurements using the pulser instead of the radioactive source.

Actually, using charge injection through the test capacitance is the correct way of measuring the *noise*. In contrast, when using signals generated in the detector by X-rays, we are actually measuring the *resolution* of the system, which includes fluctuations in the charge collected by the detector. These fluctuations may have several origins, including charge production statistics, carrier trapping (negligible in our detectors), Compton scattered X-rays, interaction of the X-ray in regions of low electric field, charge division between adjacent electrodes. These effects lead to broadening and distortion of the X-ray peaks; instead, the pulser-generated peaks are clean Gaussians, with no background.

The pulser method also has the very important advantage of allowing a much higher and adjustable data taking rate[8].

Of course fluctuations in the height of the pulser signal would contribute to the measured noise. These fluctuations have been minimized by generating a large signal and attenuating it. The fact that the peak width does not change by increasing the attenuation ratio gives confidence that the pulser signal fluctuations do not significantly contribute to the noise. It has also been verified that the pulser peaks are (slightly) narrower than the 60 keV Americium peak obtained with the simple diode (giving the lowest noise and the cleanest X-ray peaks). Finally, the fact that the noise measured with the diode agrees with the predictions of the model indicates that there are no significant noise contributions from the set-up.

Charge injection by pulsing the test capacitor on the A250 board is very practical but not always feasible. In detectors with integrated JFETs, this capacitor no longer provides access to detector, because of the presence of the Source Follower and the coupling capacitance in between.

So we must connect a different test capacitor directly to a pad on the sensor, when present, with the usual 50 Ω termination to ground [9].

If a contact pad is not present, as in the case of the small diode ("pixel") with integrated JFET, the only way to generate a high-rate signal in the detector is by optical pulses emitted e.g. by a LED. The amount of charge generated in the detector by the light pulse can be determined by comparison of the peak position with the position of the 60 keV X-ray peak.

As for the pulser, fluctuations in the intensity of light coming from the LED would

[6] Agilent 8495A, max attenuation 70 dB, frequency range: DC $\div$ 4 GHz.

[7] The A250 specifications give 2 pF with a tolerance of 10%; we measured 2.28 pF.

[8] Frequencies ranging from 100 Hz to 1 kHz were chosen in order to allow the preamplifier sufficient time for discharging the feedback RC.

[9] The 50 Ohm resistor correctly terminate the waveform, avoiding reflections that would introduce some spourious signals acting as additional noise. Its thermal noise, on the other hand, does not give an appreciable contribution to the parallel noise feeding into the CSA

contribute to the measured noise. Comparing measurements made on the photodiode with both methods shows that the LED light fluctuations are slightly worse than the pulser signal fluctuations.

The LED used should have a reverse recovery time [31] much shorter than the peaking times used, otherwise the tail in the light emission would cause the output signal height to depend on the peaking time because of the ballistic deficit effect.

3.5 DC Voltage and Current Supplies

The bias voltage of the detector is most conveniently applied to the "backside", leaving the "frontside (the one connected to the preamplifier) at ground potential. The local reference ground (or "common" potential) is provided by the shielding box, containing the detector and the preamplifier; the box is connected to the common terminal of the power supply. The voltage and current sources needed by our set-up are provided by the instrument HP4156C, intended for static characterization of semiconductor devices.

Noise on the bias supply line adds to the intrinsic detector noise: if a fluctuation Δv in the bias voltage occurs, a noise charge $\Delta Q_n = C_D \Delta v$ is injected into the preamplifier. It is then necessary to filter the bias voltage with an RC low-pass filter placed close to the detector, cutting off noise frequencies higher than $1/2\pi RC$. We used a filter with a long time constant of 10 s, realized with a 10 MΩ resistor and a 1 μF capacitor. The capacitor provides also the return path for the signal generated inside the detector.

Two more channels of the HP 4156C provide the positive and negative power supplies for the preamplifier. Filtering for these voltages is included in the preamplifier board.

A fourth SMU channel of the HP 4156C is used whenever we need a current source. For example, increasing the current of the devices is obtained through two methods: photogeneration by a LED or direct current injection through a large value resistor.

Driving a LED by a DC current we get a constant flow of light that can be used to photogenerate a constant leakage current in the detector. For this DC illumination we used an infrared led with slow response time. This helps in reducing noise, by averaging out fluctuations in the driving current.

A different method for increasing the current is by direct injection through a large value resistor, connected to the DC pad of the detector – when there is one[10]. This method can be used e.g. to increase (or decrease, or even reverse) the current flowing by punch-through to a bias ring, but it is not equivalent to a leakage current, because current injected through an ohmic contact does not carry shot noise (as verified in Section 4.3).

The current driving the LED has been filtered by an RC low-pass filter. After the filter, a large-value resistor has been used to inject the current into the detector. This resistor is necessary in order to decouple the detector from the large capacitive load of the filter and connections, plus the load of the current source itself (which is a good current source only in DC or at low frequencies).
This resistor contributes with its thermal noise to the total measured noise. The value of the resistor should then be taken large enough to make its thermal noise

[10]Every detector used is provided by a DC pad except the small diode with integrated JFET.

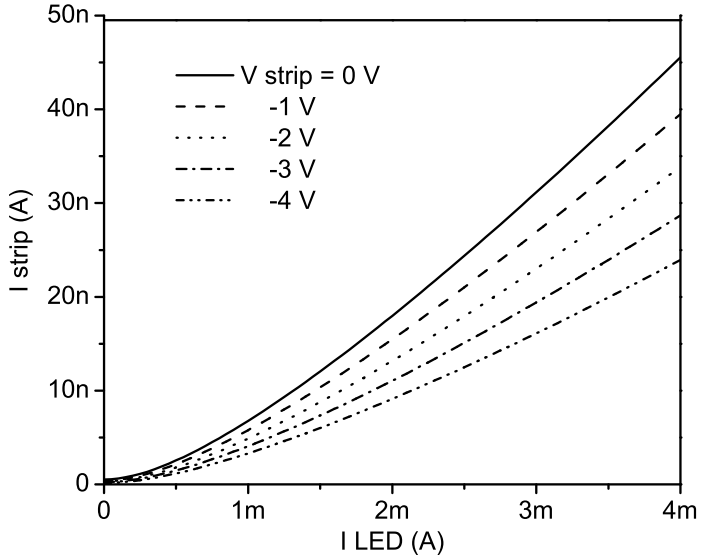

Figure 3.6: Photogenerated current drawn by the DC-connected strip on the n-side of AI sensor, plotted as a function of the current driving the IR LED, for several values of the strip voltage. The bias ring is at V=0 and a negative bias voltage (–50 V) is applied to the p-side.

negligible with respect to the other noise sources present. A 1 GΩ resistor has been used for this purpose.

3.6 Calibration of Photogenerated Current

In Section 3.4, we discussed the use of X-rays from an ^{241}Am source to calibrate the signal injected through a test capacitor, or generated by a pulsed LED.

A different calibration need arises when we use a constant ("DC") illumination to increase the leakage current of the detector by photogeneration. Being able to vary the leakage current in a controlled way over a large enough interval has proved to be very helpful for checking the predictions of the noise model, and allowed identifying an unexpected noise component that would not have been clearly visible at low currents (Section 4.4.2).

A LED[11] is mounted in a fixed position inside the shielding box and driven with a DC current, in order to shine a constant flow of light on the detector. The 850 nm photons have an absorption length of approximately 20 μm in silicon; the charge carriers photogenerated in the depleted region of the detector get collected by the electric field and contribute to the leakage current. They are subject to the same Poisson fluctuations as the thermally generated carriers, giving rise to shot noise. Metal layers on the detector absorb the light, shielding the underlying silicon. Therefore in strip detectors the photogeneration is only effective in the interstrip gaps, which are not covered by the metal. However, since the light is not

[11] Infrared AlGaAs LED type HERO HIRL5010, with peak emission at wavelength $\lambda_p = 850$ nm.

collimated, but is partially diffused inside the box, and since the photon absorption length is only a factor two shorter than the metal strip width, some carrier generation also occurs under the metal strips. The photodiode instead has a wide optical window, with a metal ring only around the edge, making photogeneration more uniform.

Since the LED current is in the range $1 \div 10$ mA and the bias needed by the AlGaAs LED is about 1 V, the power consumption reaches a maximum of 10 mW, and the heat load is not a concern.

The calibration is performed by varying the LED drive current and measuring the leakage current of the detector, kept in the same biasing conditions as for the noise measurement. This condition is important because the voltage difference between adjacent electrodes can have a strong influence on the sharing of the photogenerated current between them. When the noise has to be measured with DC-coupling of the sensor, it is straightforward to calibrate the current with the sensor kept at the appropriate bias: it is sufficient to set the voltage of the current-measuring SMU channel at the same voltage of the preamplifier input[12].
In case of AC coupling with bias provided by an external resistor, the voltage drop through this resistor is usually small, and can be evaluated and kept into account for the calibration.

The situation is more complicated when the bias to the detector element of interest (e.g. a strip) is provided by punch-through. Then we should measure the current collected by the strip when it sits at the appropriate punch-through voltage with respect to the bias ring: this will be the leakage current of the strip during the noise measurement. However, in this condition the instrument connected to the strip would measure zero current. In order to measure the current of the strip, its voltage difference with respect to the bias ring must be set to a value somewhat lower than the punch-through voltage – previously measured – so that the punch-through mechanism will be cut off, and the current will flow to the measuring instrument.

Because of the difference in biasing conditions, only an approximate determination of the current will then be possible.
For the photodiode the photogenerated current shows little dependence on the voltage difference between diode and guard ring.
By contrast, in the case of a strip detector the photogenerated current collected by a strip is strongly dependent on the potential applied to it (while the other strips stay at punch-through voltage), as can be seen in Figure 3.6.

This quite different behaviour depends on two factors.
First, the different perimeter/area ratio between the photodiode (having a square shape) and the strip. Both have approximately the same area (4 mm^2), but the strip has a perimeter $\sim$10 times longer. By varying the relative voltage between adjacent elements, we displace the boundary between their respective carrier collection regions, and this changes the sharing of the photogenerated current between the two elements. Thus we expect a larger current variation for the longer perimeter (not necessarily proportional, because it depends also on other factors like the width of the gap between the adjacent elements).
Second, the photodiode has a large optical window, so most of the photocurrent

[12] this has been measured to be -0.41 V at the supply of voltage of +-8 V

is generated far from the edges, while for the strip essentially all the photocurrent is generated in the edge region. As a consequence, even the *relative* variation of the photocurrent is larger for the strip.

In order to determine with good accuracy the photogenerated leakage current of a strip, the following method has been followed: for a given value of the LED drive current, the strip current is measured versus the strip voltage, varied from zero (the voltage of the bias ring) to the punch-through voltage. From the variation of the current in the pre-punch-through region, the current at punch-through voltage is then extrapolated.

Chapter 4

Noise Measurements on Microstrip Detectors read out by a Charge Sensitive Amplifier

This chapter summarizes systematic noise measurements performed on microstrip detectors equipped with a Charge Sensitive Amplifier (CSA), using the instrumentation described in Chapter 3. The measurement results are interpreted in terms of the noise concepts and parameterizations introduced in Chapter 2.
After validating the noise parameterization for the adopted CSA with a set of data obtained from a simple photodiode, the same method is applied to double-sided microstrip detectors from different manufacturers[1] leading to a detailed understanding of their properties and to the observation of some unexpected noise effects.

4.1 Noise parameterization

As described in Chapter 3, to characterize the noise performance of different detectors we adopted an amplification chain based on the Amptek A250 charge sensitive preamplifier and PX4 digital shaper.
The square of the modulus of the transfer function of the PX4, performing a trapezoidal shaping with peaking time τ and flat top width FT, is (see Equation 3.3):

$$|T(\omega)|^2 = \frac{4(1-\cos\omega\tau)^2(1-\cos\omega(\tau+FT))^2}{2\pi(\tau\omega)^2} \tag{4.1}$$

Given a noise current power spectral density $\frac{\mathrm{d}i^2}{\mathrm{d}f}$, generated by sources in parallel to the detector, and a noise voltage power spectral density $\frac{\mathrm{d}v^2}{\mathrm{d}f}$, generated by sources in series to the detector, the corresponding Equivalent Noise Charge (ENC), after integration over all frequencies, is:

$$ENC^2 = \frac{\mathrm{d}i^2}{\mathrm{d}f}(\frac{\tau}{3}+\frac{FT}{2}) + \frac{(C_{in}+C_D+C_f)^2}{\tau}\frac{\mathrm{d}v^2}{\mathrm{d}f} + (C_{in}+C_D+C_f)^2 A_f \tag{4.2}$$

[1] ITC-irst, Via Sommarive 18, I-38050 Trento, Italy;
SINTEF Electronics and Cybernetics, Blindern, N-0314 Oslo, Norway;
Canberra Semiconductors NV, Lammerdries 25, B-2250 Olen, Belgium.

as discussed in Chapter 2, where all the parameters appearing in 4.2 were defined. Accurate noise measurements on the amplifier chain not connected to a detector allowed to determine those parameters in the expression above that are related to the preamplifier, in particular:

- $R_S = 60\,\Omega$ is the series resistance of the input JFET;
- $A_f = 1.6\,10^{-12}\mathrm{V}^2$
- $C_{in} + C_f \sim 13$ pF
- $R_f = 200$ MΩ, although static measurements give a value of 300 MΩ, as reported by specs.

These values parameterize the parallel, series and flicker noise; the model assuming that the noise of the front-end electronics is dominated by the first input FET and the feedback resistor is only an approximation. However, the parameter values are reproducible and are the starting point for noise measurements on detectors read-out by a CSA.
As first step, Equation 4.2 has been tested, varying both the peaking time and the leakage current; agreement with the model also implies full functionality of the set-up. The noise measurements have been performed both on a simple photodiode and on ALICE-type detectors, for which the most significant static measurements have been reported in Chapter 1.

4.2 Preliminary measurements on a PhotoDiode

Our noise model has been initially validated by measurements performed on a photodiode.
On the same wafers containing the microstrip detectors many test devices are fabricated, including several diodes. As test structures, they are mainly used for the determination of the dopant density and carrier generation time in the high-purity substrate. A small area (2 mm $\times$ 2 mm) photodiode with guard ring has been cut from an ITC-supplied wafer, glued onto a fiberglass support and connected by wire-bonds. The metallization covers just the perimeter of the implant, in order to leave a wide optical window.
An RC low pass filter (470 M$\Omega \times 1\ \mu$F) is soldered close to the pad contacting the backside, in order to remove noise from the bias voltage applied to the diode. The noise measurements reported below are essentially scans of noise versus peaking time, performed for several values of the diode leakage currents. The latter has been photogenerated by illuminating the device with an IR LED, driven by an SMU operating in current mode.

4.2.1 DC-coupled measurements

A first set of measurements has been performed with DC coupling between photodiode and CSA: the terminal bonded to the p^+ implant of the junction diode is directly connected, through a short wire, to the gate of the input FET. DC coupling is possible because the low leakage current of the diode (tens of pA), flowing through the 300 MΩ feedback resistor, produces only a negligible voltage drop (order of 0.1 V). This is the less noisy configuration, since it does not include

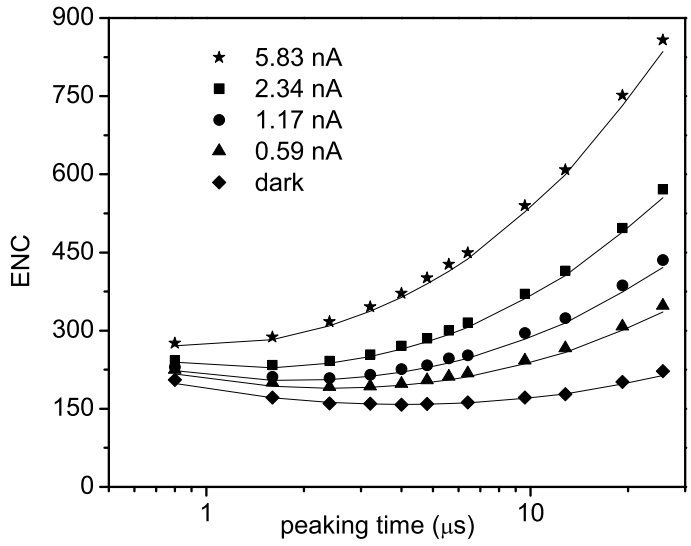

Figure 4.1: Equivalent Noise Charge versus peaking time, measured on the photodiode DC coupled to the CSA. Several values of leakage current are considered: dark ($\sim$ 10 pA), 0.59 nA, 1.17 nA, 2.34 nA and 5.83 nA, controlled by photogeneration from an IR LED. The points are the experimental values, while the solid lines are the curves obtained from 4.2, with the parameters values derived from DC measurements or noise measurements with open CSA input.

the parallel noise contribution from a bias resistor. The expected noise should follow Equation 4.2 that, including the explicit expressions for the power spectral densities, becomes the sum of the three following terms:

$$\mathrm{ENC}^2 = \sum \begin{cases} (\frac{\tau}{3} + \frac{FT}{2})(2qI_L + \frac{4kT}{R_f}) & \text{parallel white noise} \\ \frac{1}{\tau}(C_{in} + C_D + C_f)^2 4kT(\frac{\Gamma}{g_m} + R_S) & \text{series white noise} \\ (C_{in} + C_D + C_f)^2 A_f & \text{series flicker noise} \end{cases} \tag{4.3}$$

with the parameter values:

- $R_S = 60\ \Omega$ is the series resistance of the input FET (the series resistance in the diode itself is not important);
- $C_D = 3.2$ pF is the capacitance of the diode implant towards the backside and the guard ring, to be added to the previously estimated capacitance of the CSA ($C_{in} + C_f$);
- I_L is the diode leakage current, either thermally generated or photogenerated. This current is derived from a DC calibration, performed by measuring the diode current as a function of the LED driving current.

Figure 4.1 summarizes the noise measurements performed for several values of the diode leakage current. The continuous lines represent the noise curves predicted by the model, with the parameter values listed above. A good agreement with the model is obtained, confirming the reliability of the set-up.

4.2.2 AC-coupled measurements

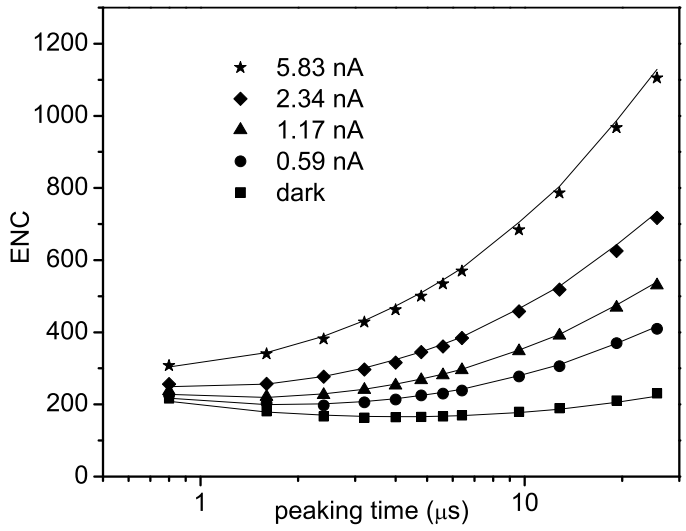

Figure 4.2: Noise measured with the photodiode AC-coupled to the CSA by a 2 nF external capacitor. The diode is biased by punch-through to the guard ring. The leakage currents have the same values as in the DC-coupled case. The continuous lines are obtained from the model, assuming a noise contribution from leakage current $\frac{\mathrm{d}i^2}{\mathrm{d}f} = 4qI_L$ (see text).

In order to measure the noise when the diode is biased by punch-through to the surrounding guard ring, a large value capacitor (2 nF) has been interposed between the diode and the CSA. The leakage current made of holes collected by the diode charges up the diode to a positive voltage, until a stationary state is reached in which an equal current of holes flows by the punch-through mechanism [6] [8] from the diode to the guard ring. With a 50 V bias applied to the backside contact and the bias ring at common, the diode sits at a voltage of $\sim$ 9 V. This punch-through voltage drop, slowly increasing with the leakage current, has been taken into account when performing the calibration of the diode current versus the IR LED drive current in AC biasing conditions.

The punch-through current is due to carriers (holes in this case) emitted over a potential barrier. As such, it is affected by Poisson fluctuations leading to a shot noise contribution. If fluctuations in the hole emission current from diode to bias ring are uncorrelated to fluctuations in the hole arrival current on the diode (a reasonable assumption for not too large currents), then the two shot noise contributions should add up in quadrature, leading to a leakage current contribution to parallel noise $\frac{\mathrm{d}i^2}{\mathrm{d}f} = 4qI_L$ instead of just $2qI_L$ (Figure 4.3). Then the effect of punch-through biasing would be an increase by a factor $\sqrt{2}$ of the shot noise (to be added in quadrature to the other noise sources). The measured noise values, reported in Figure 4.2, agree with this assumption.

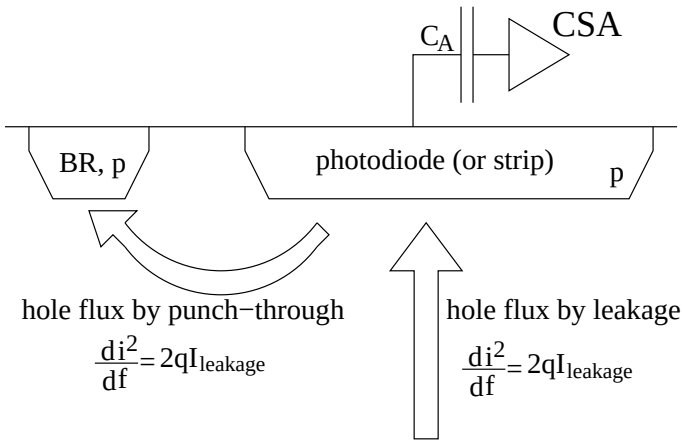

Figure 4.3: Model of different noise sources for the AC-connected detector. The punch-through current of holes flowing to the Bias Ring (BR) is equal to the leakage current and adds a further "shot noise" term to the overall noise.

4.3 Noise in Strip Detectors

In our set-up with single channel readout, for the strip detectors we expect to have the same types of noise sources as for the diode. The very different geometry would only be reflected in different values for the relevant parameters.
In the next paragraphs the main differences with respect to the simple diode and their consequences will be discussed.

The long and narrow implant of a strip has a large resistance (order of $10^5\Omega$). However, this resistance does not contribute to thermal noise, because it has strong capacitive coupling to the low-resistance metal strip connected to the amplifier (the upper electrode of the integrated AC-coupling capacitor). This capacitance is high enough to be the path of least impedance in the frequency range of interest for this study, so that the high resistance of the implanted strip is effectively shunted by the metal strip and the thermal noise contribution is set by the latter.

The resistance of the metal strips has been measured, and found to be in the interval $20-50\ \Omega$, depending on the side (p or n) of the sensor and on the supplier. It also varies between wafers, due to variations in metal thickness and line width. The strip series resistance R_S with the total strip capacitance C_D makes a low-pass filter, with 3dB cut at $f = \frac{2\pi}{R_S C_D}$. In our case $R_S C_D \sim 10$ pF $\cdot$ 100 $\Omega \sim 1$ ns, much shorter than our shaping times (and of any shaping time used with strip detectors), so the filtering is determined uniquely by the shaper.

In situations when several strips are bonded together in "daisy-chain", with just the last one connected to a preamplifier, the resulting electrode is quite long and the inductance of the strips must be taken into account when predicting the noise level. A strip must be represented with capacitive, inductive and resistive elements all connected in a passive distributed network ([26], pag 128). With the help of circuit simulations (using SPICE or similar programs) it is then possible to determine the minimum granularity (numbers of LRC elements per unit length) required for accurate predictions. When the transfer function of the shaper (the response to a δ-like pulse) peaks at high frequency (10 MHz, say), this kind of

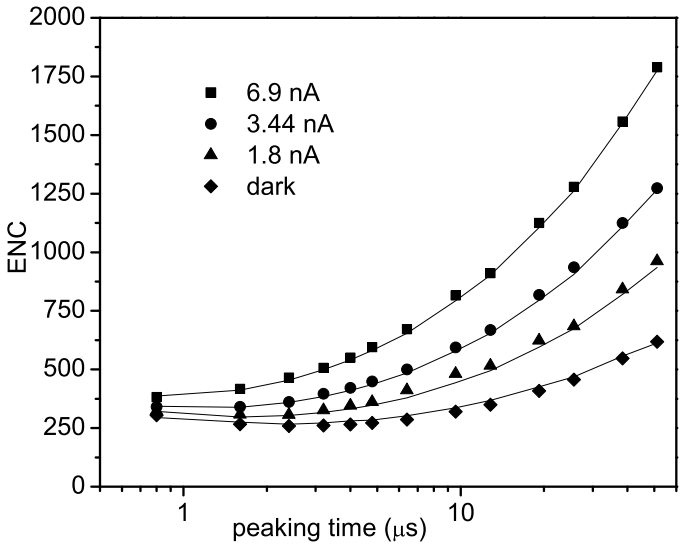

Figure 4.4: ENC versus peaking time for detector AE, p-side, at several values of photogenerated currents: 0.7 nA (dark), 1.8 nA, 3.44 nA and 6.9 nA. $V_{bias} = 40$ V. Strip biased by punch-through. The continuous lines are the predictions of the model, with $\sum C = 24$ pF, $R_S \sim 85\ \Omega$

analysis is necessary [32].
In the ALICE detector, the strips are only four centimeters long (to reduce occupancy in the very high multiplicity environment) and are read-out in a frequency range (shaping time 1-2 μs) where inductive effects are totally negligible. The strips can then be represented by a single capacitance and a resistance in series and noise analysis can rely on what has been developed for the simple diode.

In our set-up every metal strip, except the one under study, is bonded to a common line, which during noise measurements is connected to the "common" terminal (the local reference ground): in this way we reproduce the actual operation of the detector, where the metal strips are not floating, but are kept at local ground by the front end electronics.
However, during operation in the ALICE experiment, every strip is read out by a dedicated amplifier, whose input noise voltage is coupled to the adjacent strips by the interstrip capacitance. This induced noise adds in quadrature to the other noise sources of the strip. In our case, this noise contribution is absent (or very low), since the adjacent strips are directly connected to ground, with no noise source apart from the very small thermal noise due to the low resistance of the metal strip. Then again, the model used for the simple diode should be applicable.

The detector capacitance is the sum of the interstrip capacitance and the backside capacitance plus a contribution of capacitance towards the bias ring, which is negligible except at very low frequencies (see Chapter 1). As can be seen by plots reported in Chapter 1, in the frequency range of our noise measurements [2],

[2]From Equation 3.4 we deduce that the range of peaking times considered in this Chapter (0.8 to 25.6 μs) corresponds to a frequency interval of approximately 10-500 kHz.

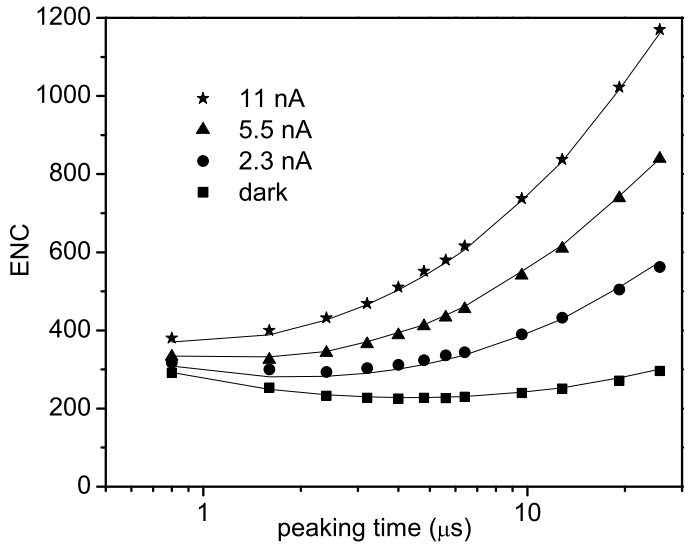

Figure 4.5: Detector AS1, p-side. Strip under measurement biased by external resistor (the punch-through mechanism is turned off). Photogenerated currents of 0.2 nA (dark) with $R_{bias} = 1$ GΩ, 2.3 nA with 470 MΩ, 5.5 nA with 200 MΩ and 11 nA with 100 MΩ. $V_{bias} = 70$ V. The continuous lines are the predictions of the model, with $\sum C = 23$ pF, $R_S = 70\,\Omega$

the strip capacitance can be considered frequency-independent (in our noise model the effect of capacitance changes smaller than 1 pF is not significant). As a consequence, when calculating from the model the noise versus peaking time curves, a single capacitance value has been used, independent of peaking time.

The results of noise measurements performed on the strip detectors generally agree well with the model predictions, with some exceptions described in the following sections.

As an example, Figure 4.4 shows the Equivalent Noise Charge versus peaking time measured on a p-side strip of detector AE, for different values of the strip leakage current, controlled by photogeneration. The continuous lines show the predictions of the model. The parameters characterizing the amplifier (including the $1/f$ noise coefficient A_f) have been taken from measurements performed without detector (Section 4.1). The total capacitance has been determined by adding the measured strip capacitance to the amplifier input capacitance. As done in the case of the photodiode, a shot noise contribution of the punch-through current has been added in quadrature to the other noise sources. The agreement between the measured data and the model is quite satisfactory, over a wide range of peaking times and leakage currents.

The punch-through contribution to noise can be further checked by exploiting the fact that, in addition to the pad on the metal line ("AC pad"), also the pad connected to the implant of the strip under measurement ("DC pad") has been bonded to an external terminal. It is then possible to apply different methods for

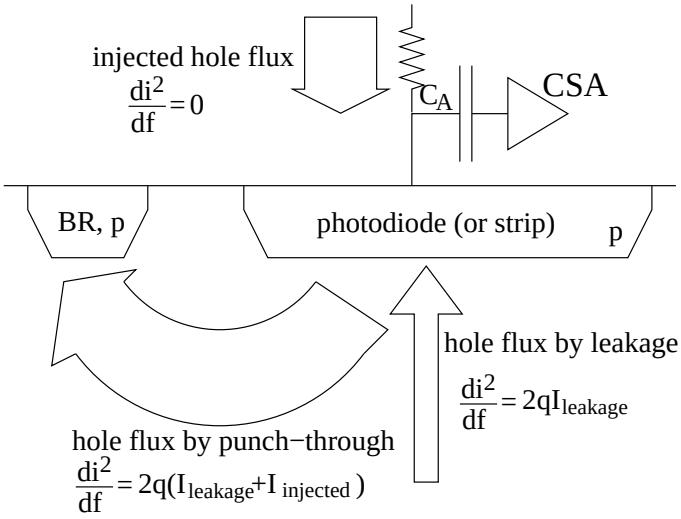

Figure 4.6: Carrier fluxes and noise contributions for the case of a positive injected current on p-side. Although current injected through an ohmic contact has no associated noise, it contributes to noise since it adds up to the punch-through current.

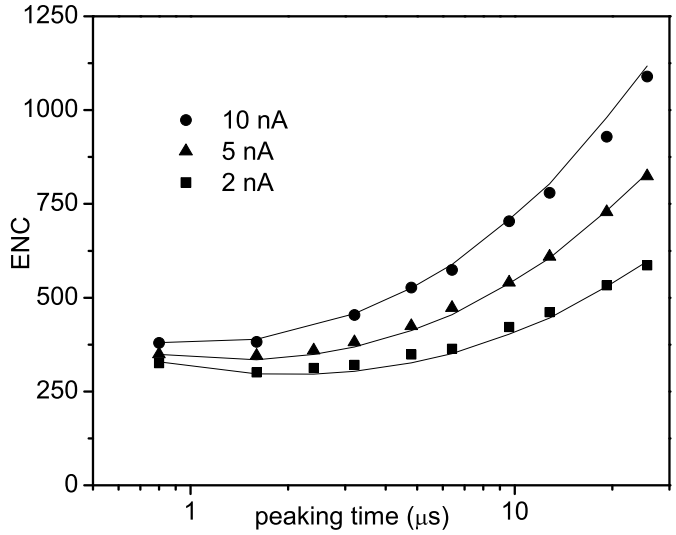

Figure 4.7: Detector AI, n-side. Strip biased by punch-through and current injected via a large resistor (1 GΩ). The injected currents (2, 5 and 10 nA) are negative: the electrons flow from the strip to the bias ring as in normal punch-through conditions. $V_{bias} = 60$ V. The continuous lines are the predictions of the model, with $\sum C = 24$ pF, $R_S = 80\,\Omega$

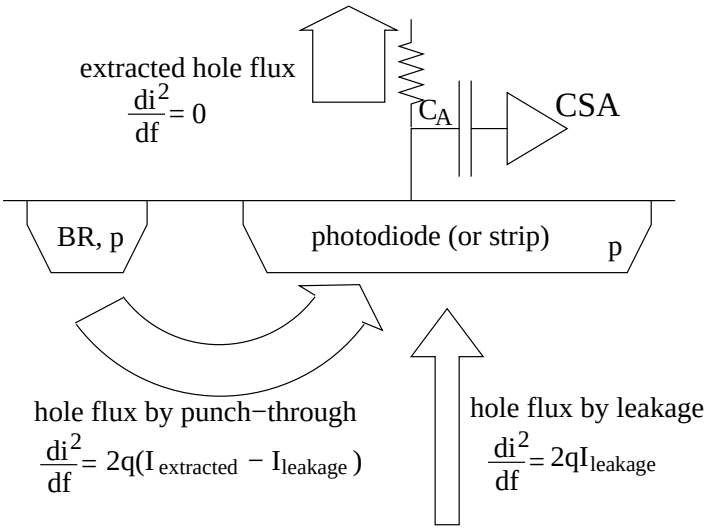

Figure 4.8: Carrier fluxes and noise contributions for the case of a negative injected current on p-side. The punch-trough current flows in reversed direction, as long as the extracted current is larger than the leakage current. The leakage current and punch-through current add up to give the extracted current.

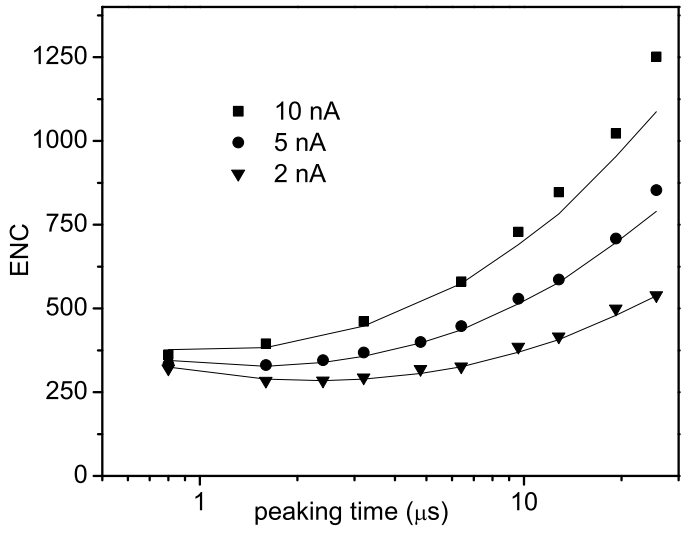

Figure 4.9: Detector AI, p-side. Current extraction (injection of a negative current) of 2, 5 and 10 nA. The leakage current and the punch-through current from the bias ring to the strip add up to give the current drained by the external current source. $V_{bias} = 60$ V. The continuous lines are the predictions of the model, with $\sum C = 24$ pF, $R_S = 80\,\Omega$

biasing methods, and to control the punch-through current independently of the leakage current.

For every detector, the following set-ups have been explored:

- Polarization via an external resistor R_{bias}, connected between the DC pad and the common terminal. Provided $R_{bias} I_L < V_{PT}$, the punch-through current is turned off, because the voltage drop between strip and bias ring is below the punch-through voltage, and the strip leakage current flows through the external resistor. The shot noise contribution of the punch-through current disappears, being replaced by the thermal noise of the bias resistor. The noise current spectral density then becomes:

$$\frac{\mathrm{d}i^2}{\mathrm{d}f} = 2qI_{PT} + 2qI_L = 4qI_L \;\rightarrow\; 2qI_L + \frac{4kT}{R_{bias}} \tag{4.4}$$

  As an example, Figure 4.5 shows a measurement performed on detector AS1, p-side. A good agreement with the predictions of the model is found.

- Current injection through the DC pad: this time the external resistor is not used to bias the strip (i.e. to set its voltage), but is connected to a current source; the strip voltage is again set by the punch-through mechanism, with a punch-through current given by the sum of the leakage current and the injected current. The value of R is taken very large (1 GΩ), in order to minimize its thermal noise contribution. The noise current spectral density (neglecting the small contribution from the 1 GΩ resistor) is then:

$$\frac{\mathrm{d}i^2}{\mathrm{d}f} = 2qI_L + 2q(I_L + I_{injected}) = 4qI_L + 2qI_{injected} \tag{4.5}$$

  The situation (referred to p-side) is depicted in Figure 4.6. In order to increase the flow of holes from the strip to the bias ring, the injected current must be positive. On the n-side, the symmetric situation requires a negative current injected through the DC pad (thus increasing the flow of electrons by punch-through from the strip to the bias ring). Figure 4.7 reports the results of a measurement performed on sensor AI, n-side.

- Current extraction from the DC pad: if the sign of the external current is reversed, we can make the carriers to flow by punch-through in the reverse direction (from the bias ring to the strip). The situation referred to p-side is illustrated in Figure 4.8. The noise contribution becomes:

$$\frac{\mathrm{d}i^2}{\mathrm{d}f} = 2qI_L + 2q(I_{extracted} - I_L) = 2qI_{extracted} \tag{4.6}$$

  since the punch-through current adds to the leakage current to satisfy the boundary condition set by the external current source[3]. Figure 4.9 shows the measurement made on sensor AI, p-side. Note that in this case we do not need to rely on an independent knowledge of the leakage current (which can vary with time, and requires a calibration when photogeneration is used) so that deriving the predictions of the model is both simpler and more accurate.

[3]This is true when the extracted current is larger than the leakage current; if not, part of the leakage current keeps flowing to the bias ring, and the noise contribution is: $2qI_L + 2q(I_L - I_{extracted}) = 4qI_L - 2qI_{extracted}$.

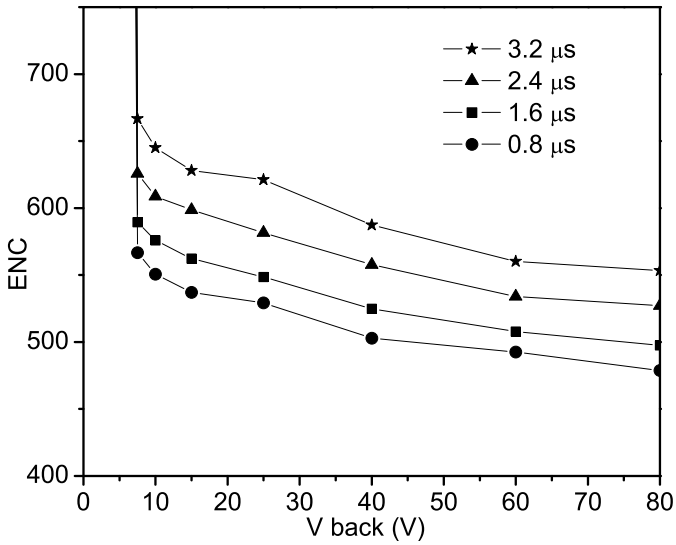

Figure 4.10: Noise versus bias voltage of AE n-side for peaking time of 0.8, 1.6, 2.4 and 3.2 μs.

For every setup, a good agreement between data and model is obtained, using for the detector capacitance a value very close to the one derived from the direct measurements reported in Chapter 1. A slight excess capacitance (1-2 pF) required in order to better reproduce the measurement results can be attributed to parasitics in the connection.

4.4 Unexpected noise components in strip detectors

Although in the situations illustrated so far the measured noise agrees with the predictions of the basic model of Section 4.1, in some instances significant deviations from the simple model have been observed. These are described in the next two subsections.

4.4.1 Noise due to resistive layers at the surface

In addition to the peaking time, the leakage current and the polarization method, we can vary one more parameter: the bias voltage. Increasing it, the noise is expected to decrease a bit, since the capacitance (slightly) does[4]; this is observed for the AS detectors and the p-side of the AI detector. Instead, new phenomena appear on the AE detector and the n-side of the AI detector, strictly related to what observed on the behaviour of the dissipation factor in the capacitance measurements (Section 1.1.4).

[4]In the dark, the small increase of the leakage current does not appreciably affects the noise at moderate shaping times, while the photogenerated currents are independent of bias voltage.

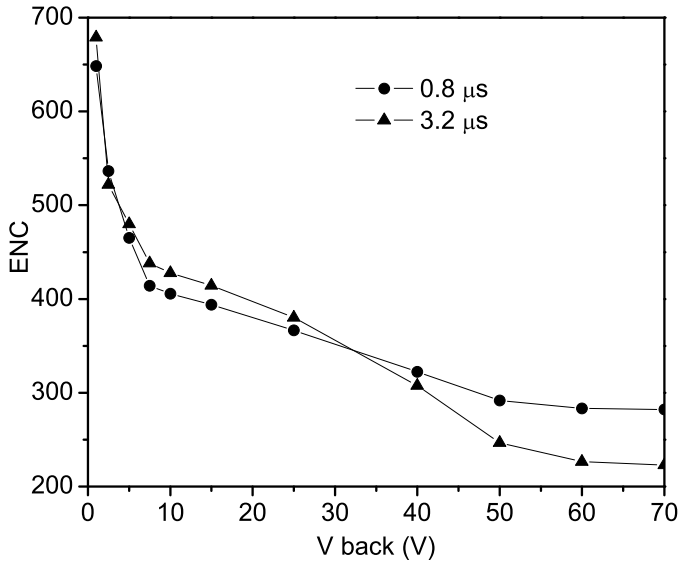

Figure 4.11: Noise versus bias voltage of AE p-side for peaking time of 0.8 and 3.2 μs.

The sensors AE and AI have very low depletion voltages (about 8 V and 15 V, respectively)[5]. The noise measurements reported in the previous section – performed at bias voltages well above the depletion voltage – agree with the simple model. However, in an intermediate voltage interval, an extra noise contribution appears. Furthermore, the n-side of detector AE (not shown in the previous section) shows a large excess noise at all bias voltages.

In Figures 4.10 through 4.13, we show the noise versus bias voltage for both sides of the AE and AI sensors, measured in the dark for different values of the peaking time.
The AS sensors have not been considered since their depletion voltage is much higher and the effects described in the following have not been observed.

Consider first the n-side of sensor AE, shown in Figure 4.10. Below depletion voltage the noise sharply increases, an obvious consequence of the fact that the n-side strips are no longer insulated. Above depletion, we observe a monotonic decrease of noise with increasing bias voltage, but the level of noise remains significantly higher (about a factor two) with respect to the p-side and to the other types of sensors, and also relative to the prediction of the model. Therefore, some noise source not considered in the model must be present. We can further note that at all bias voltages the excess noise is larger at longer peaking times.

On the p-side of the same detector (Figure 4.11), the noise shows an important decrease above depletion voltage, ending in a plateau beyond $\sim$ 50 V. From 10 to 50 V, at a peaking time of 3.2 μs the noise decreases by more than 150 e^-, and

[5] As previously noted, by "depletion voltage" we actually mean the bias voltage at which the interstrip resistance on n-side exceeds 100 MΩ.

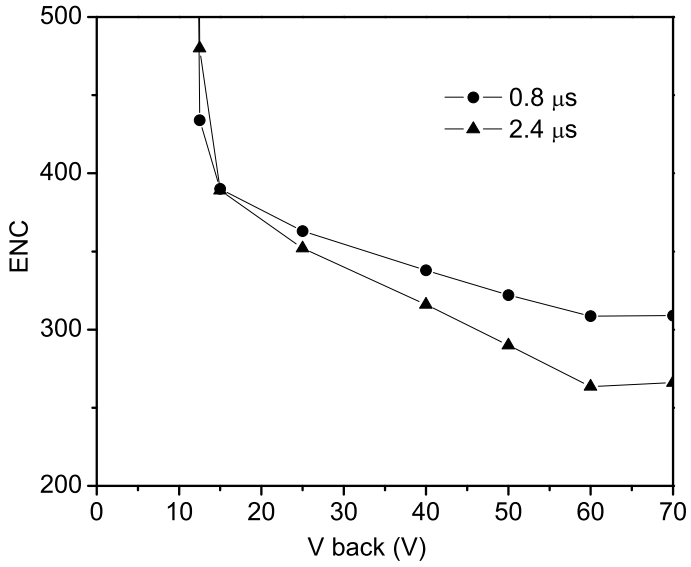

Figure 4.12: Noise versus bias voltage of AI n-side for peaking time of 0.8 and 2.4 μs.

by more than 100 at 0.8 μs. Below depletion voltage, the noise increases rapidly (because of the large backside capacitance and of the dissipative effects in the undepleted high resistivity bulk) but not as sharply as on the n-side, since the p-side strips are junction-insulated from the substrate.

While the noise values in the high-voltage plateau are compatible with the predictions of the basic model, the noise increase going to lower voltages cannot be explained by the modest increase in capacitance. Here again, the excess noise at low voltage is higher at longer peaking times, and must come from some additional noise source, not included in the basic model.

Similar considerations hold for the n-side of the AI detector (Figure 4.12, where the plateau is reached at ~ 60 V.

Finally, for the p-side of sensor AI (Figure 4.13), the noise increase going down in voltage is much less pronounced, and is compatible with the increase in capacitance.

Comparing these results with the curves of dissipation factor versus bias voltage reported in Figure 1.6, a striking similarity becomes apparent:

- For AE n-side both D and noise are much higher; D is about constant, while the noise decreases slowly with voltage.

- For AE p-side both D and noise decrease significantly with voltage, reaching a plateau beyond ~ 50 V.

- For AI n-side, both D and noise decrease significantly with voltage, reaching a plateau beyond ~ 60 V.

- AI p-side has low D and no excess noise, even at low voltage.

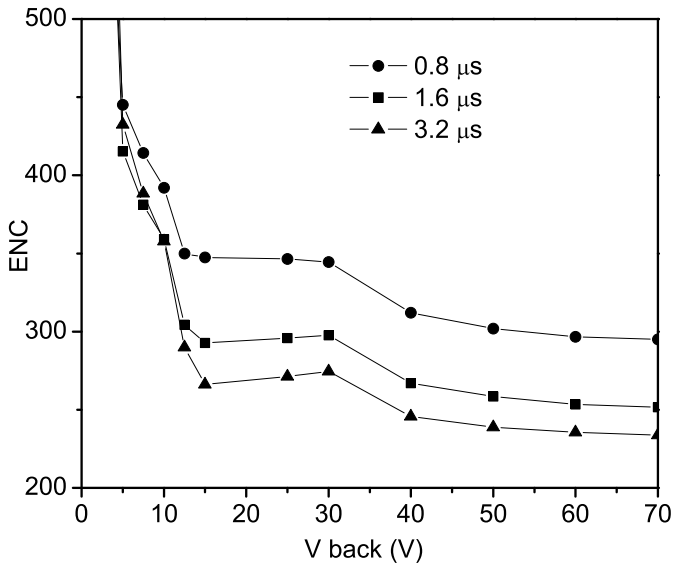

Figure 4.13: Noise versus bias voltage of AI p-side for peaking time of 0.8, 1.6 and 3.2 μs.

It is also interesting to consider the plots of the interstrip capacitance and dissipation factor versus frequency (Section 1.1.4), where both C and D reach a lower value, frequency independent, at a bias voltage corresponding to the voltage beyond which the excess noise disappears. These features have been attributed to the presence of a common resistive path surrounding all the strips, which at low voltages and low frequencies introduces a long-range capacitive coupling between the strips.

We are then naturally led to attribute the source of the excess noise to the presence of a resistive layer: accumulation electrons on AI n-side and AE p-side, p-spray implant on AE n-side.

In order to find out the spectral density of the excess noise, since we cannot directly measure the noise in the frequency domain, we rely on the measurements taken versus peaking time.
To begin with, we determine the excess noise by subtracting in quadrature the ENC value predicted by the basic model from the measured ENC value. In all cases, the result is a time dependence of the form:

$$\mathrm{ENC}_{\mathrm{res}}^2 \propto \sqrt{\tau} \;=\; qK_{res}\sqrt{\tau} \tag{4.7}$$

where the suffix "res" stands for "resistive layer", and the proportionality constant K_{res}, with units of C $\sqrt{\mathrm{Hz}}$, has the values reported in Table 4.1.

By increasing the detector current using photogeneration or direct injection, we verified that this excess noise is actually independent on both the leakage current and the punch-through current.

Since the excess noise comes from the detector, we find it natural to describe it in terms of a noise current. As we are going to verify in the following, the

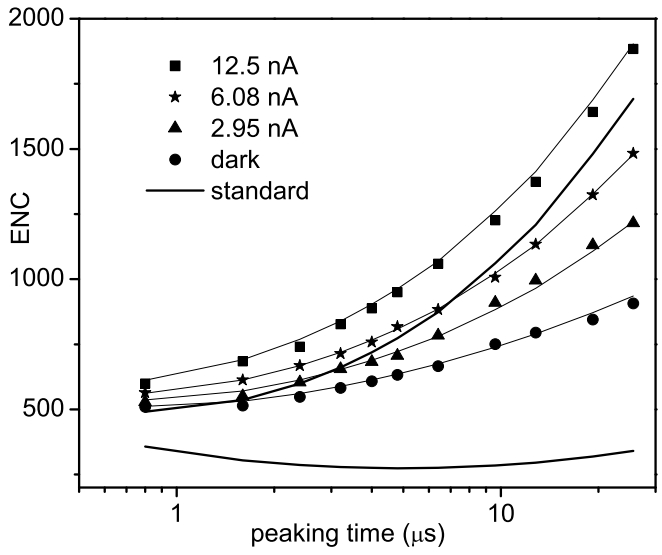

Figure 4.14: Detector AE, n-side. Punch-through biased, with photogenerated currents of 200 pA (dark), 1 nA, 2.95 nA, 6.08 nA and 12.5 nA. Independently of the bias applied (here 40 V), ENC^2 shows an extra term proportional to $\sqrt{\tau}$. The thin continuous lines are calculated from the model including this extra term. The two thick lines show the predictions of the basic model, for the dark and 12.5 nA currents.

	ITC n-side (25 V)	Canberra n-side (40 V)	Canberra p-side (25 V)
AC set-up	0.5	2.4	1

Table 4.1: Values of K_{res}, in units of 10^{-11} C $\sqrt{\mathrm{Hz}}$, for the three detectors showing excess noise of the type $ENC^2_{res} = qK_{res}\sqrt{\tau}$

noise current power spectral density generating, after triangular shaping, a noise $\mathrm{ENC}^2 \propto \sqrt{\tau}$ is proportional to $\sqrt{\omega}$. We parameterize it as:

$$\frac{\mathrm{d}i^2_{res}}{df} = qK'_{res}\sqrt{\omega} \tag{4.8}$$

By inserting this expression into Equation 2.24, giving the ENC corresponding to a noise current at the input of a CSA followed by a shaper with transfer function $T(\omega)$, and using the expression 4.1 for the transfer function of a trapezoidal shaper, we get:

$$\mathrm{ENC}^2_{res} = \int_0^\infty \mathrm{d}\omega \, \frac{|T(\omega)|^2}{\omega^2} \, qK'_{res}\sqrt{\omega} \; = \tag{4.9}$$

$$qK'_{res} \, \frac{4\sqrt{2}}{15\sqrt{\pi}} \, \frac{FT^{2.5} - 2\tau^{2.5} - 2(FT+\tau)^{2.5} + (FT+2\tau)^{2.5}}{\tau^2}$$

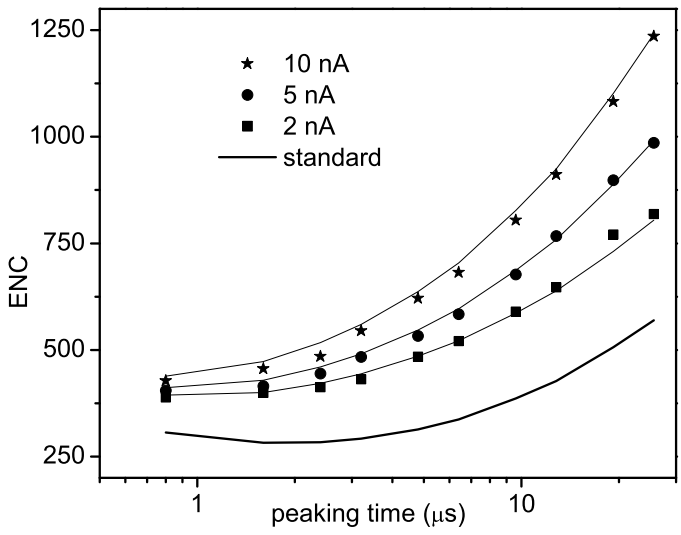

Figure 4.15: Detector AE, p-side, at low bias voltage (25 V). Injected positive currents of: 2 nA, 5 nA and 10 nA. The thin continuous lines are calculated from the model including the extra term $\mathrm{ENC}^2 \propto \sqrt{\tau}$. The thick line shows the prediction of the basic model for a 2 nA current. Other parameters are $\sum C =$ 23 pF, $R_S = 80\,\Omega$

In our case, the shaping is almost triangular, with $FT \sim 0$; then the expression simplifies to:

$$\mathrm{ENC}^2_{res} \simeq 0.35\, qK'_{res}\, \sqrt{\tau} \tag{4.10}$$

which coincides with 4.7 if we set $K'_{res} = K_{res}/0.35$.

Figures 4.14 through 4.16 plot the usual noise scans versus peaking time, for the three cases showing this kind of excess noise. The continuous lines represent the noise calculated with the modified model, including the term given by Equation 4.7 with the K_{res} values given in Table 4.1. Also shown by comparison are the noise curves (thicker lines) predicted by the basic model, for some values of the leakage currents.

During the assembly and then the commissioning of the ALICE Silicon Strip Detector, the noise of every strip has been monitored. The integrated front-end electronics connected to the sensors performs a semigaussian filtering with shaping time 1.8 μs. It was readily recognized that n-side of AE-type detectors has higher noise than the others. Furthermore, the noise on the p-side of AE-type detectors and on the n-side of AI-type detectors is still decreasing with bias voltage well beyond depletion, until a plateau is reached at high voltage.
This noise behaviour could not be justified in terms of capacitance variations, and no explanation for it has been found.

Figures 4.17 and 4.18 show two examples of such noise measurements, plotting the rms noise voltage at the shaper output for the 768 strips of the p-side of a

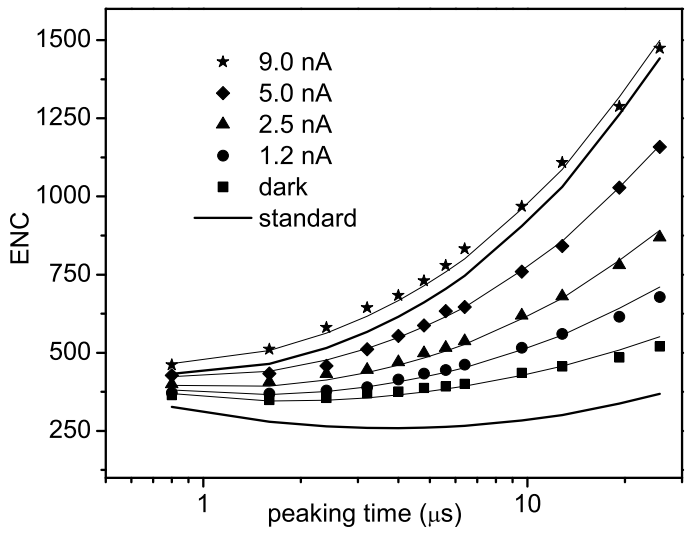

Figure 4.16: Detector AI, n-side at low bias voltage (25 V). Punch-through biased, with photogenerated currents of 300 pA (dark), 1.2 nA, 2.5 nA, 5 nA and 9 nA. The thin continuous lines are calculated from the model including the extra term $\mathrm{ENC}^2 \propto \sqrt{\tau}$. The thick line shows the prediction of the basic model for the dark case. Other parameters are $\sum C = 25$ pF, $R_S = 80\,\Omega$

sensor, followed by the 768 strips of the n-side of the same sensor and so on for all ten modules making up a half-ladder, giving a total of 15360 strips[6]. Figure 4.17 refers to 10 modules all with AE-type sensors while Figure 4.18 shows 9 modules with AI-type sensors and one – easily recognizable by the greater noise of its n-side – with AE-type sensor. During acceptance tests at the INFN Trieste laboratory, these AE-type sensors, of which we can track the serial number, have been found to deplete between 12 and 20 V. For the AI-type sensors the depletion voltage is between 26 and 30 V.

Looking at Figure 4.17, it appears evident that the n-side is noisier than p-side and that the variation of the noise level between 30 and 90 V of bias is larger on p-side than on n-side. This agrees with the above reported measurements: the noise on the n-side of AE sensors slightly decreases with bias voltage but remains quite high; on p-side, instead, the excess noise contribution $ENC^2 \propto \sqrt{\tau}$ is present at 30 V, while at 90 V it should be absent. For most modules, this decrease is significant, on the average about 25%. Considering that a m.i.p. (releasing a charge of $\sim$24 ke) gives a signal of 120 mV, the observed noise decrease of 0.5 mV, translated into electrons, gives ~ 100 e.

For the AI-type sensors in Figure 4.18, the noise on p-side does not change with bias voltage between 39 and 90 V. This seems to imply that in these sensors the electron accumulation layer at the interface is rapidly depleted in the region of the narrow punch-through gap between the end of a strip and the bias ring. Then

[6]Courtesy of ALICE Trieste group.

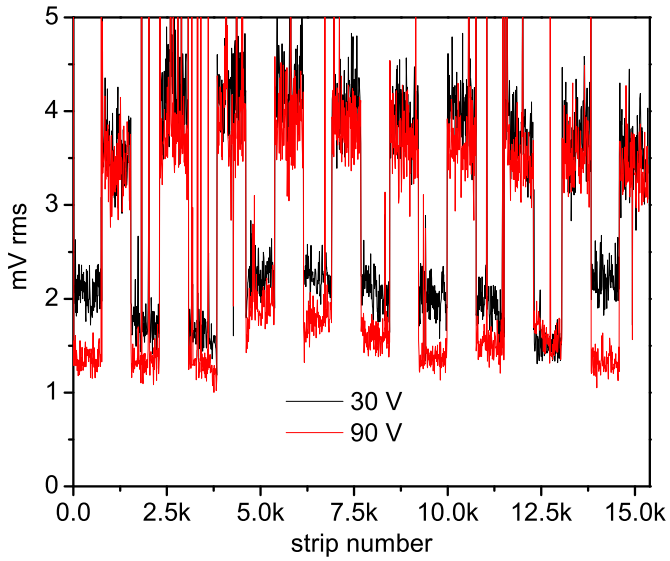

Figure 4.17: Noise scan, in mV, of the strips of p and n-side of 10 consecutive modules mounted on a half-ladder of the Silicon Strip Detector of the ALICE experiment. The sensors are of the AE type, and the noise is measured at two bias voltages: 30 V and 90 V.

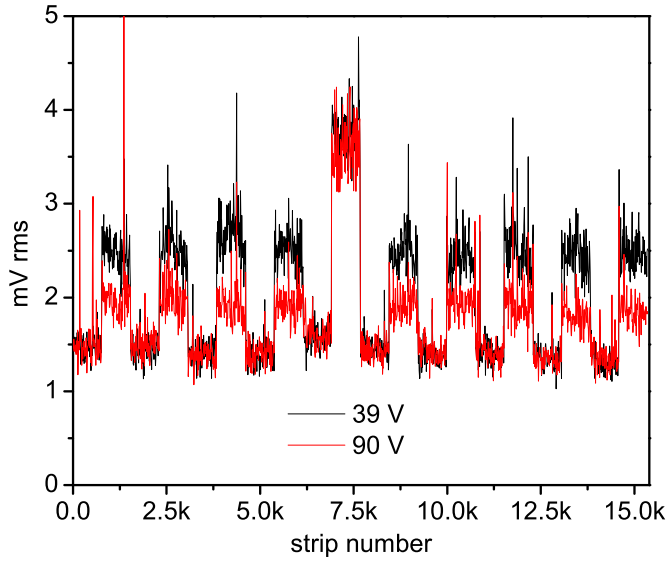

Figure 4.18: Noise scan, in mV, as in Figure 4.17. The sensors, this time, are of the AI type, except the fifth which is AE-type. The noise is measured at 39 V and 90 V.

the accumulation channels in between the p-type strips would be insulated from each other and no long-range resistive-capacitive coupling between strips would be present. On AE-type sensors, instead, this depletion would only occur at relatively high bias voltages, so that the noise decreases going from 30 to 90 V.
On the n-side of AI-type sensors, the noise difference between low and high voltage is on the order of 50 e. This can be related to the presence of a continuous resistive layer, made of accumulated electrons under the $Si - SiO_2$, interface, running all around the p-stop implants and in ohmic contact with the n-type bias ring. As discussed in Section1.1.4, at high enough voltage the accumulation layer between the p-stops begins to deplete near the ends of the strips, interrupting the continuous path.
Even at high voltage the n-side is noisier (by $\sim 50\,e$) than the p-side. This does not agree with the measurements made with the single-channel readout, which show about the same noise level on the two sides of the AI sensor at high bias voltage. It is possible that the (modest) additional noise observed on the n-side with the ALICE setup is due to different readout conditions.

On the n-side of AE-type sensors, the high noise at all bias voltages appear to be related to the presence of the resistive p-spray layer surrounding the strips. This layer undergoes a slight lateral depletion at the edges of the strips and bias ring (explaining the slow decrease of noise and of capacitance), but is never completely depleted or interrupted in some regions by the applied bias voltage.

4.4.2 Excess Punch-Through Noise

A different unexpected noise component appears on the p-side of the AS sensors. Figure 4.19 shows the noise versus peaking time measured on the AS1 sensor with punch-through biasing and several values of the photogenerated leakage current. The continuous lines are calculated from a modified model, as explained below. Note that in this plot (and only in this one) the ENC is plotted on a logarithmic scale. The ENC at high currents and/or long peaking times is significantly higher than was measured on the other sensors, and appears to be linearly dependent on τ (unit slope on the log-log plot). This excess noise was not present in the plot of Figure 4.5, relative to the same detector, in which the strip was polarized by an external resistor in order to turn off the punch-through current. In fact, the noise in Figure 4.5 was in good agreement with the basic model with no punch-through contribution but including the thermal noise of the bias resistor. This clearly shows that the large excess noise in Figure 4.19 must have its origin in the punch-through mechanism.

On n-side, this excess noise is absent and the basic model applies.

In the photodiode and the other strip detectors, the punch-through current has been found to contribute an additional shot noise term, added in quadrature to the shot noise of the leakage current. Here the situation is different: the contribution of the punch-through current to ENC^2, instead of being linearly proportional to τI_{PT} appears to be proportional to the square of both the peaking time and the punch-through current.

Since the excess noise is originated by the punch-through current, it is natural to describe it by a current noise at the amplifier input. The fact that ENC^2 is approximately proportional to τ^2 leads us to guess that the spectral power density of this current noise is proportional to $1/\omega$, or $1/f$, which can be described as a

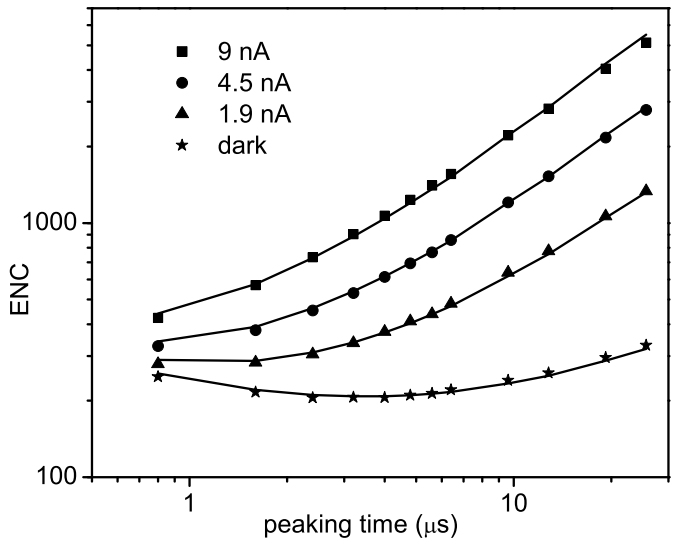

Figure 4.19: Detector AS1, p-side. Biased by punch-trough, with photogenerated currents of 170 pA (dark), 1.9 nA, 4.5 nA and 9 nA. $V_{bias} = 70$ V. $\sum C = 20$ pF, $R_S = 70\,\Omega$

"parallel 1/f noise".

A naive attempt to get from this noise current power spectral density the ENC in the time domain corresponding to a trapezoidal shaper with transfer function $T(\omega)$ – as was done in Equation 4.9 for a spectral density $\propto \sqrt{\omega}$ – fails, because the integral is divergent:

$$\mathrm{ENC}^2 = \int_0^\infty \mathrm{d}\omega \frac{|T(\omega)|^2}{\omega^2} \frac{\mathrm{d}i^2}{\mathrm{d}f} \quad \propto \int_0^\infty \mathrm{d}\omega \frac{|T(\omega)|^2}{\omega^2} \frac{1}{\omega} \quad \rightarrow \quad \infty \tag{4.11}$$

However, the $1/f$ dependence is only an approximation for the real noise process. As discussed in Section 2.1.3, the 1/f noise often results from the superposition of several Lorentzian noise processes, having a plateau at low frequency and a dependence $\propto f^{-2}$ beyond the 3dB point [33]. This superposition is obviously finite at zero frequency. The $1/f$ approximation is a convenient one in the case of a noise *voltage* with spectral power density $\propto 1/\omega$ ("*series* $1/f$ noise"), because the divergence is cancelled by the factor $|T(\omega)|^2$ in the integration. Here however we have a noise *current* with spectral density $\propto 1/\omega$ ("*parallel* $1/f$ noise"): this brings a factor ω^{-2} in the integrand, and the integral no longer converges.

If we try fitting the data in Figure 4.19 by including in the model a term simply proportional to $\tau^2 I_{PT}^2$ we do not get a good match at short peaking times. This may be due to the fact that the trapezoidal shaping is characterized by two constants (shaping time τ and flat top width FT). Although the minimum available value for FT has been selected in all cases, at short peaking times this is not negligible in comparison to τ.

Because the direct determination of the noise coefficients for trapezoidal shaping from Equation 4.11 failed, we tried using the same relative weights for τ and

FT as derived for the parallel *white* noise: $(\frac{\tau}{3} + \frac{FT}{2})$.
Consequently, in Figure 4.19, the solid lines are calculated from the model with an extra term given by:

$$\mathrm{ENC_{PT}}^2 = qK_{PT}\,(\frac{\tau}{3} + \frac{FT}{2})^2\, I_{PT}^2 \tag{4.12}$$

where the dimensionless coefficient K_{PT} has the value $7 \cdot 10^{14}$. We see that this term reproduces well the measured noise.
The modified noise model for this detector is then represented by the expression:

$$\mathrm{ENC}^2 = \sum \begin{cases} (2qI_L + 2qI_{PT})(\frac{\tau}{3} + \frac{FT}{2}) & \text{parallel white noise} \\ \frac{1}{\tau}(C_{in} + C_D + C_f)^2\, 4kT(\frac{\Gamma}{g_m} + R_S) & \text{series white noise} \\ (C_{in} + C_D + C_f)^2\, A_f & \text{series flicker noise} \\ qK_{PT}(\frac{\tau}{3} + \frac{FT}{2})^2\, I_{PT}^2 & \text{parallel flicker noise} \end{cases} \tag{4.13}$$

For operation in the ALICE experiment, where the shaping time is relatively short (on the order of 1 μs), the effect of this excess noise is hardly noticeable for "normal" values of the leakage current ($\lesssim$1 nA). However, most AS-type sensors have been pre-irradiated on p-side with low energy X-rays in order to increase the positive oxide charge and prevent the inversion of the interface [4]. As a consequence, the $\mathrm{Si-SiO_2}$ interface damage created by the irradiation increased the strip current to a value of $\sim$ 5 nA/strip. At these current levels the excess noise starts being appreciable, but the total noise is still comfortably low (the signal to noise ratio for a m.i.p. still exceeds 50:1). It is interesting to note that the irradiation affected the noise only through the increased leakage current: no effects of the surface damage on the $1/f$ noise have been observed. In particular, the parameter K_{PT} in Equation 4.12 remains practically unchanged.

It must be remarked that if in noise measurements we did not artificially increase the leakage current by photogeneration or direct injection, we would not have been able to find out this excess noise contribution.

Some authors [34] [33] reported excess noise on irradiated silicon strip detectors biased by punch-through. They found the excess noise was induced by hadron irradiation; instead, γ-irradiation was ineffective in generating this noise. They observed the excess noise was growing linearly with the shaping time [34].

This has been interpreted in terms of a $1/f$ current noise, caused by radiation generated defects [33]. The carriers (holes) making up the punch-through current – which flows in the bulk, although close to the surface – may get trapped by some kind of bulk defect and released after a time delay characteristic of the trap. Each trap generates a lorentzian noise; a large number of traps with a broad spectrum of time constants result in a frequency dependence very close to $1/f$ [33].

In the case of the AS-type sensors, however, the excess punch-through noise is present in non-irradiated sensors (and at the same level in X-ray irradiated ones), none of which is likely to have a significant level of bulk defects. If, on the other hand, interface states were responsible of the noise through modulation of the electric field in the underlying bulk region, then the X-ray irradiated sensor AS2, having a higher density of interface states, would be expected to show higher noise, which is not the case. Hence, the origin of this excess noise in the AS-type sensors remains unclear.

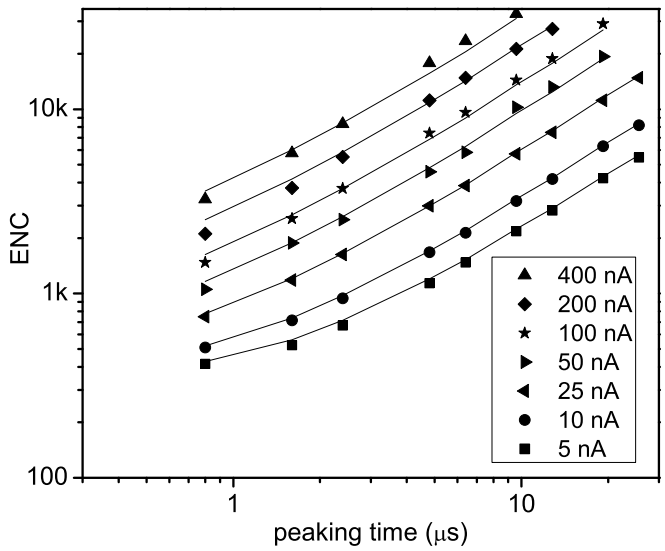

Figure 4.20: Detector AS2 (irradiated with X-rays), p-side. ENC versus peaking time, in log-log scale, for large currents injected into the DC pad of the strip. The continuous lines show the noise calculated with Equation 4.13, using the following values for the parameter K_{PT}: $6 \cdot 10^{14}$ at 5 nA and 10 nA, $5 \cdot 10^{14}$ at 25 nA, $4 \cdot 10^{14}$ at 50 nA, $2.3 \cdot 10^{14}$ at 100 nA, $1.5 \cdot 10^{14}$ at 200 nA, $0.8 \cdot 10^{14}$ at 400 nA.

The dependence on shaping time reported in [34] is the same as discussed above for the p-side of the AS sensors. However, the dependence on the leakage current is different. In [34], a square root dependence on current of the extra noise term is quoted – the same as for shot noise – but with a proportionality factor three-four times larger. They reached current levels up to 1 μA per strip: this is a quite high current to flow in the narrow punch-through region at the strip end. At these injection levels, space charge effects likely arise and the poissonian hypothesis of random emission of carriers does not hold anymore [7].

In order to see whether at high current levels the linear dependence of the excess noise found at moderate currents was modified into a square root dependence, we performed additional noise measurements by injecting large currents through the DC pad in the AS2 detector. The injected current, in addition to the leakage current, flows by punch-through from the p^+ strip to the bias ring.
At high currents, space charge effects are observed from the deviation of the punch-through I-V characteristics from an exponential law, so we may expect that the previously stated $ENC^2 \propto \tau^2 I^2$ dependence gets modified.
Figure 4.20 reports the results of these measurements, with injected currents up to 400 nA. Currents exceeding 50 nA have been injected through resistors of value lower than 1 GΩ, in order to keep the voltage drop within the voltage compliance of the current source.

For each current value, the dependence $ENC^2 \propto \tau^2$ for the excess noise is confirmed. If we fit the data with an expression like 4.12 for the excess noise, we find that the constant K_{PT} varies for currents in excess of about 10 nA, decreasing

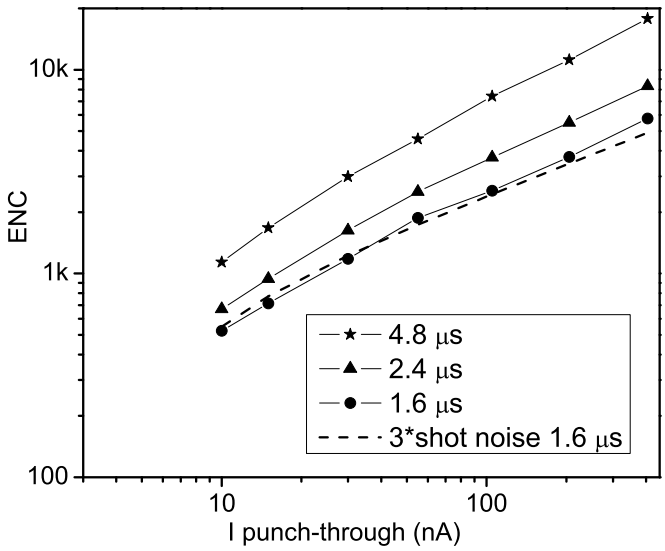

Figure 4.21: Detector AS2, p-side. ENC versus injected current for three different peaking times (1.6 μs, 2.4 μs, 4.8 μs) (the continuous lines simply join the points). The dashed line shows (for a peaking time of 1.6 μs) the ENC given simply by three times the shot noise of the current.

for higher currents. This indicated that the dependence of the excess ENC on I_{PT} is less than linear.
These measurements are plotted in a complementary way in Figure 4.21, where the noise versus punch-through current is shown for three different peaking times. Also shown (for a short peaking time of 1.6 μs) is the noise calculated as three times the shot noise of the punch-through current, corresponding to what has been observed in [34]. We see that indeed for large currents the excess noise ENC is closer to a square root dependence on I_{PT} (as is the case for the shot noise) than to a linear one.

Chapter 5

Noise Measurements on Microstrips with integrated Source-Follower structure

In this chapter we present the measurements performed on detectors with an integrated first amplification stage, consisting in a couple of JFETs in Source-Follower (SF) configuration.

One of them, J_C, acts as a current source, setting the operating point of the other FET, J_S, whose gate is connected to the detector. Because of some limitations of the set-up, the theory exposed in Chapter 2 will have to be revisited in order to derive quantitative results applicable to the real situation. Noise measurements will then be presented, first for the two kinds of SF with pixel-like sensor; secondly for the strip-like sensors, for which several read-out configurations have been explored. As in the previous chapter, the experimental data are compared with the "modified" theoretical expectations, using for the device parameters the values obtained from static measurements.

5.1 Modified theoretical analysis

The signals at the output of the SF stage have an exponential fall set by the RC time constant of the equivalent small signal circuit seen by the gate of the input JFET J_S. The time constants of the studied detectors are 18 μs and 9 μs for the pixels-like sensors having input JFET 1000/4 and 400/4, respectively, and 18.8 μs in the case of the strip detector. Such relatively short values are due to the integrated polysilicon bias resistors, whose values are 3 MΩ for the pixels and 0.8 MΩ for the strips. These decay times are shorter than the minimum value of 36 μs required at the input of the PX4 digital processor in order to get the correct trapezoidal shape at the output. However, if we set the pole-zero correction parameter PZ to zero, we still know the transfer function of the shaper, which is given by equation 3.2:

$$T(s) = \frac{(-1 + e^{-s\tau})(-1 + e^{-s(FT+\tau)})}{\sqrt{2\pi}\,\tau\, s} \tag{5.1}$$

The drawback of this approach (the only one we can adopt given the above mentioned constraints) is that the peak amplitude of the output signal will decrease

when the peaking time increases. But again, having an analytical expression for $T(s)$, the signal amplitude dependence on the peaking time can be estimated in advance, once a calibration of the gain is performed.
As explained in Chapter 2, the ENC is defined as the charge giving, for a determined detector system, a S/N=1. Then, in order to get it, we must calculate the effect of the amplification stage on both the signal and the noise. When we dealt with the CSA case, the signal (S) was independent of the shaping time, in such a way that the ENC was an expression of just the noise level (N) of the detector. In the SF case, with our set-up, the signal depends also on the shaping time and then the ENC does not measure just the noise. Using this parameter for the SF configuration may lead to some misunderstandings and erroneous evaluations of the device itself, then, without losing in accuracy and gaining in clarity, we will proceed separating the analysis of the signal and of the noise, verifying separately the theory for both. Of course, the spectrographic performance of the whole detector system, including the shaper, is still expressed by the ENC.

5.1.1 Signal

As soon as a charge Q_0 is delivered into a detector of capacitance C_D, it produces a small signal voltage at the output of the preamplifier CSA whose amplitude is, as shown in Chapter 2:

$$v(t) = \frac{Q_0}{C_{GD} + C_D} \frac{C_A}{C_f} e^{-\frac{t}{RC}} \tag{5.2}$$

where C_A is the capacitance coupling the SF to the CSA, C_f is the feedback capacitance of the CSA, C_{GD} the gate-to-drain capacitance of the input FET J_S and R the bias resistor at the gate of J_S; all these components are depicted in Figure 2.4.
Consider, now, what happens when this short exponential fall is processed by a triangular shaper (giving as a response to a step pulse at its input an isosceles triangle at the output [1]). The response $f(t)$ of the shaper to an unity amplitude step with exponential decay at its input can be more easily evaluated in the frequency domain:

$$\mathscr{L}(f(t)) = \mathscr{L}(e^{-\frac{t}{RC}})T(s) = \frac{RC}{1+sRC}T(s) \tag{5.3}$$

where $T(s)$ is the transfer function of the triangular shaper, given by Equation 5.1 with $FT = 0$. Going back to the time domain, we obtain [35]:

$$f(t) = \mathscr{L}^{-1}(\frac{RC}{1+sRC}T(s)) = \tag{5.4}$$

$$\frac{RC}{\tau}(1 - e^{-\frac{t}{RC}} + 2\theta(t-\tau)(-1 + e^{-\frac{t+\tau}{RC}}) + \theta(t-2\tau)(1 - e^{-\frac{t+2\tau}{RC}}))$$

where $\theta(t)$ is the Heavyside function.
The function $f(t)$ reaches a maximum value $f(\tau) = \frac{RC}{\tau}(1 - e^{-\frac{\tau}{RC}})$ at $t = \tau$.
Note how for $RC \to \infty$ the maximum is independent of the peaking time and it approches 1 (because we have not specified any amplification from the shaper).
On the other hand, if $RC \neq \infty$ a bipolar shape like that in Figure 5.1 appears

[1] The PX4 is a good approximation of a triangular shaper when the peaking time τ is much longer than the flat top width FT.

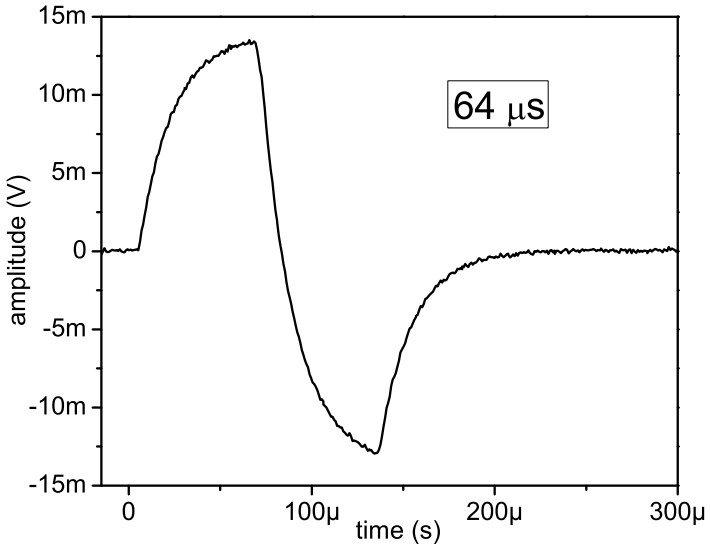

Figure 5.1: Signal processed by the PX4 shaper with peaking time set to 64 μs. The input signal is an exponential fall with decay time 18μs, i.e. the output of the PIN 1 detector. The signal is acquired by a digital scope and the noise is averaged out over many identical waveforms.

on the scope. In this figure a real signal obtained with $\tau > RC$ ($\tau = 64$ μs and $RC = 18$ μs) is shown, confirming the correctness of the expression 5.4.

Note how in Figure 5.1 the leading and falling edges follow exponential laws, as expected from formula 5.4, with time constants equal to the decay time of the input signal.

In the case of trapezoidal shaping, expression 5.4 becomes more complicated and more terms appear in the equation; but for what concerns us nothing changes: the maximum is again at $t = \tau$ and has the same value. This maximum value of the output signal is detected by the PX4 and acquired as the final result of the signal processing.
Injecting a constant charge into the detector, a different amplitude is acquired, depending on the peaking time, proportional to:

$$\frac{RC}{\tau}(1 - e^{-\frac{\tau}{RC}}) \tag{5.5}$$

To verify this point, an ^{241}Am spectrum has been acquired for several values of the peaking time: the 60 keV peak position agrees with 5.5, as shown in Figure 5.2. Fitting the curve, it is possible to have a further determination of the parameter RC, that could be estimated or by static measurements or, more accurately, by fitting the output signal as seen on a scope, like the one of Figure 5.1. Moreover, it is a way to calibrate the gain of the whole acquisition chain, necessary to scale the noise data. The expected amplitude of the signal is (in channels):

$$\frac{RC}{\tau}(1 - e^{-\frac{\tau}{RC}})\frac{Q_0}{C_D + C_{GD}}\frac{C_A}{C_f}A \tag{5.6}$$

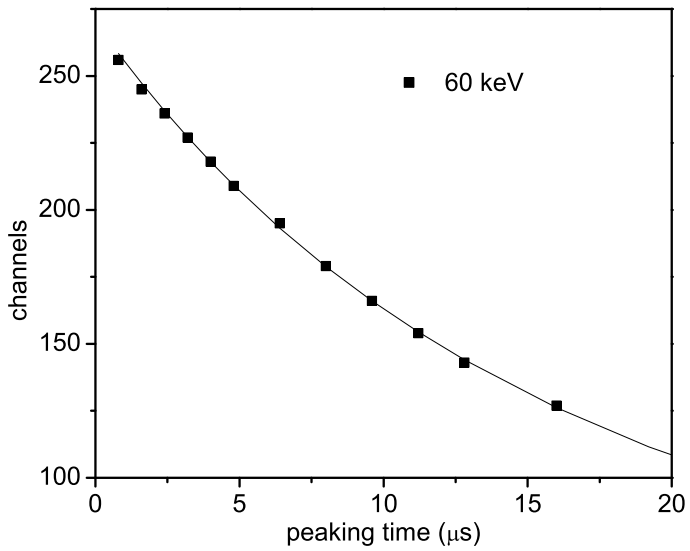

Figure 5.2: Position of the 60 keV X-ray peak acquired with the PIN 2 detector. The solid line is calculated with expression 5.5, scaled by the gain.

product of the first in expression 5.4 with the amplification introduced by detector and CSA and with the gain A of the shaper (in channels/V), the aim of our calibration.
For every device, the 60 keV peak position has been measured versus peaking time, in order to determine the gain $\frac{C_A}{C_f}A$.

5.1.2 Noise

In chapter 2, the contribution of every noise source was calculated and expressed in terms of the ENC. There, it was understood that the signal amplitude is independent of the peaking time. As explained in the previous section, this is not the case with our set-up.
Since both signal and noise change with peaking time, this parameter is misleading and we must calculate the theoretical σ^2 of the noise in some arbitrary units (for example, in channels of PX4) and compare it with the measured one, as we did for the signal. The contributions of every type of noise (flicker, series or parallel) are calculated solving the integral and scaling it for the gain of the amplification chain:

$$\sigma^2 = A^2 \int_0^\infty \mathrm{d}\omega \frac{\mathrm{d}v_{out}^2}{\mathrm{d}f} |T(i\omega)|^2 \tag{5.7}$$

where $\frac{\mathrm{d}v_{out}^2}{\mathrm{d}f}$ is the noise voltage power spectral density at the output of the CSA. The single contributions are then, making explicit the gain parameter $A\frac{C_A}{C_f}$:

- series:

$$\sigma_s^2 = (\frac{C_A}{C_f}A)^2 \frac{1}{\tau}(\frac{\mathrm{d}v_s^2}{\mathrm{d}f} + \frac{\mathrm{d}v_1^2}{\mathrm{d}f}(\frac{C_A + C_{in}}{C_A})^2) \tag{5.8}$$

- flicker:
$$\sigma_f^2 = (\frac{C_A}{C_f}A)^2(A_{f,S} + A_{f,1}(\frac{C_A + C_{in}}{C_A})^2) \tag{5.9}$$

- parallel: as seen in chapter 2, the discharging of the signal through the detector RC leads to a non trivial calculation of the noise. There, this integral has been calculated for a triangular shaper; in the case of a trapezoidal one, the integral I becomes:
$$I = \int_0^\infty \mathrm{d}x \frac{(1-\cos(x))(1-\cos(x(1+\frac{FT}{\tau})))}{x^2(1+(xa)^2)} \tag{5.10}$$
$$I = \frac{\pi}{2} + \frac{a\pi}{4}(-2 + 2e^{-\frac{1}{a}} + 2e^{-\frac{1}{a}(1+\frac{FT}{\tau})} - e^{-\frac{1}{a}(2+\frac{FT}{\tau})} - e^{-\frac{FT}{a\tau}}) \tag{5.11}$$
with $a = \frac{RC}{\tau}$, and it is easily verified that for $FT = 0$ we are back to the expression 2.59 of the triangular shaper. The parallel noise contribution can be written as:
$$\sigma_{parallel}^2 = (\frac{C_A}{C_f}A)^2 \frac{\mathrm{d}i_p^2}{\mathrm{d}f}\frac{2R^2}{\pi\tau}I \tag{5.12}$$
The parameters of the detector, $C_D + C_{GD}$ and R, enter only via the constant a.

Summing in quadrature these three independent terms, we get the total value of σ^2. Having established the required noise expressions, we began the study from the simplest devices, i.e. the pixels, in order to check our theoretical model.

5.2 Noise on integrated JFETs

The noise properties of the JFETs having, as bottom gate, one of the two p-wells of Figure 1.15 have been explored by measuring the gate referred noise voltage by means of a spectrum analyzer [36], then in the frequency domain. As can be seen in Figure 5.3, the improvement achieved with the "new" p-well is significant: both the high frequency plateau, coming from white noise contributions, and the $1/f$ noise are much better in devices built with the new technology. The $1/f$ noise corner is as low as 100 Hz and the related noise coefficient A_f, entering into noise expressions for the ENC, is less than $10^{-13}V^2$, which can be neglected. For comparison, the A_f parameter for the 2SK152 JFET used at the input of the A250 preamplifier is ten times greater. The white noise contribution is seen to scale correctly with the transconductance (not shown in the figure); however, it is quite high, due to the series resistance of those portions of the p-type implants of both the top gate and the bottom gate that are not covered by the metallization. The value of this gate resistance is of the order of 400 Ω. For the old p-well, which is less doped than the new one, this gate resistance is even larger, as can be easily appreciated from the high frequency part of the spectrum in Figure 5.3.
All devices considered in the following have the "new" p-well.
In the polarization range adopted, the gate leakage current is negligible, so the noise coming from the JFETs is uniquely due to the gate resistance and to the channel conductance. It can be expressed as a gate referred noise voltage power spectral density:
$$\frac{\mathrm{d}v^2}{\mathrm{d}f} = 4kT(\frac{\Gamma}{g_m} + R_{Gate}) \tag{5.13}$$

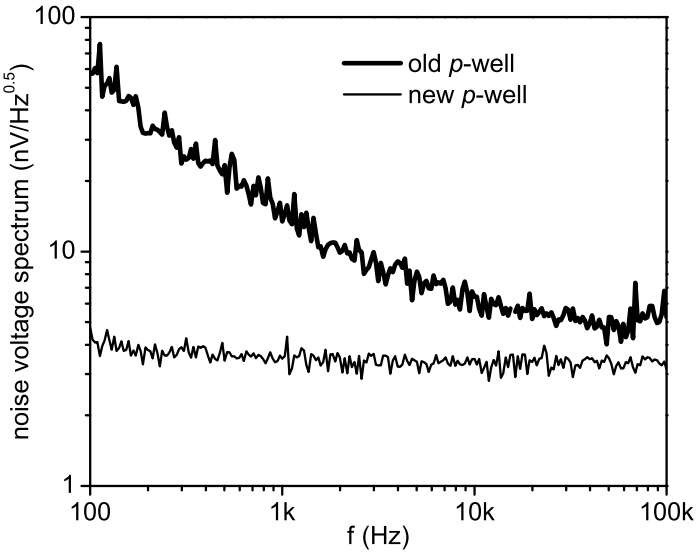

Figure 5.3: Gate referred square root of noise voltage power spectral densities of two JFETs fabricated with the two different p-wells. JFET under measure is the triode 1000/4, $V_S = 0$ V, $V_D =$ 3 V and $I_D = 250$ μA [36].

5.3 Measurements on Pixels

As anticipated in chapter 1, we have two kinds of pixels, named PIN 1 and PIN 2. The two pixel types have the same sensor size, then they have the same value for $C_D = 1.0$ pF. They also have the same value of $R_{bias} \sim 3$ MΩ, but they differ in their JFETs:

- PIN 1 has J_S of type 1000/4, i.e. having a channel length of 4 μm and channel width of 1000 μm with $C_{GD} = 4.6$ pF; J_C, the current source FET, has a 400/4 geometry;

- PIN 2 has a 400/4 J_S with $C_{GD} = 1.8$ pF and a 200/4 J_C.

The chosen values of power supply voltages must ensure the JFETs are working in the saturation region, in order to get a good Source-Follower action. The chosen voltages are $V_{DD} = 3$ V, $V_{SS} = -3$ V, $V_{GG} \rightarrow$ ground and $V_{bias} = 50$ V (see Figure 2.4), sufficient to deplete the 300 μm substrate. Both V_{DD} and V_{SS} are provided by batteries, since the S and D currents in the mA range are not easily filtered by simple RC low-pass filters. In this condition the transconductance of the JFETs and the gate-drain capacitance C_{GD} of J_S are readily obtained from their static characterization, described in Chapter 1:

- PIN 1: $g_{m,J_S} = 10.7$ mS, $g_{m,J_C} = 5.8$ mS, $C_{GD,J_S} = 4.6$ pF

- PIN 2: $g_{m,J_S} = 4.6$ mS (g_{m,J_C} is not measurable, since the gate is short-circuited to the source, and no test-structure of this size is present on the wafer), $C_{GD,J_S} = 1.8$ pF.

parameters for PIN 1			
C_A (pF)	R_{bias} (MΩ)	C parasitic (pF)	fitted τ (μs)
none	2.65	1.2	17.9
8	2.70	0.6	17.1
67	2.75	0.8	17.5
1 nF	2.75	1	18

Table 5.1: Summary of some of the parameters fitting the data acquired with the pixel PIN 1. First line (output of the SF directly connected to PX4, without capacitor C_A) refers to Figure 5.4, second line to Figure 5.5. The fitted τ values are derived from curves analogous to the one shown in Figure 5.2.

The transconductance and capacitance values above reported are measured on test structure devices, since in pixel detectors with source-follower not all terminals are accessible. For example, the gate of J_S is not accessible and the source and gate of J_C cannot be independently contacted. The quoted values must be taken as approximate, since a spreading of the parameters has been observed in test structures.
Since the leakage current is very low, few tens of pA, the voltage drop on the 3 MΩ bias resistor is negligible and the gate stays practically at the same voltage of V_{GG}, i.e. ground.
At the drain of J_C (connected to the source of J_S), a pad allows the connection of an external capacitor C_A of selectable value. Direct connection to PX4 input is also possible; in this case the input signals are very small, fractions of a millivolt. This option, however, has been explored and found to give acceptable results.
As explained in previous sections, we expect the product of R_{bias} with $C_D + C_{GD}$, symbolized by RC, to be equal to the time constant of the exponential decay of the output signal, recorded by a digital scope.
What we observe in every detector is that the DC value of polysilicon resistor multiplied by the measured capacitance is slightly greater then the decay time of the output pulses.
For PIN 1 this product is 18.5 μs and the decay time fitted on the signal shape is ~ 18 μs; for PIN 2 the RC product is 9.9 μs against a fitted decay time of ~ 9.0 μs. We expect the other way around, since parasitic capacitances are likely present. This 5-10 % discrepancy could be attributed to the fact that the bias resistor sees under the oxide a further resistance on the undepleted substrate: the oxide capacitance, in the frequency range of interest, shorts the two resistances. In this way, the effective resistance is the parallel of the two. Even though we could expect some kind of frequency dependence, throughout the noise calculations a constant resistance for every peaking time is used. Measurements made on both pixels justify this first order approximation. Capacitances of some fractions of picofarad, accounting for parasitics, are added to fit the experimental data. The product of the "effective" resistance and the "corrected" capacitance is, with good approximation, equal to the time constant derived by fitting the 60 keV data similar to those in figure 5.2. In the two tables 5.1 and 5.2, a summary of the parameter values used for the two pixel types is presented. The noise data in Figure 5.4, plotted together with the theoretical curves expected from the parameters listed in tables 5.1 and 5.2, refer to the SF directly connected to the PX4 shaper, without

parameters for PIN 2			
C_A (pF)	R_{bias} (MΩ)	C parasitic (pF)	fitted τ (μs)
none	2.65	0.5	9.1
67	2.65	0.4	9.0

Table 5.2: Summary of some of the parameters fitting the data acquired with the pixel PIN 2. First line refers to Fig. 5.4 and line 2 to Figure 5.5.

interposing the CSA. In this case, the noise contribution of the A250 is replaced by the input noise of the PX4. In the plots, it is parameterized with a series resistance of 1 kΩ, which is exactly its input impedance [37]; expected noise, as can be seen, is smaller than the measured one at the lowest peaking times, while at higher peaking times, when the thermal noise of the 3 MΩ bias resistor on the pixel dominates, the agreement is good. Flicker noise from PX4 may be responsible for this discrepancy.
Of course, the Johnson noise of the 3 MΩ resistor is dominant over other noise sources. It behaves as parallel noise until peaking times of the order 2 RC; beyond that point, it shows a series noise behavior. This is more evident on PIN 2 pixel, exhibiting a shorter RC time constant.
One could think about increasing R_{bias} by connecting an external resistor in series with the 3 MΩ integrated resistor, in order to reduce the parallel noise; however this would be ineffective because the output pad of the 3 MΩ resistor has a large capacitance to the undepleted substrate, effectively shorting it to ground in the frequency range of interest.
At low peaking times, the series noise contribution from the gate resistance becomes important. For both devices, a value of 400 Ω can be deduced from the measured noise versus peaking time dependence. Another group measured [19] [36], by means of a spectrum analyzer, the noise power spectral density (shown in Figure 1.15) of the JFETs making up the SF, finding good agreement with our measurements in the time domain. Such a high value for the series resistance is due to the resistance of the long and narrow gate implants.
Figure 5.5 shows the plots acquired from the two PIN devices, AC-coupled to the CSA through C_A. In this case, we can neglect the noise coming from the last amplification stage (the PX4) and, again, the noise is well reproduced by calculations.
With the source-follower, the test capacitance present on the preamplifier board cannot be used to inject charge into the detector. Moreover, the pixels do not have a DC pad for connecting an external C_{test} to the detector. The only way to generate events is irradiating the detector with some kind of particle. Acquisition of ^{241}Am spectra is not practical because it requires a long time (due to the small area of the pixels) and the 60 keV peak is not well separated from the background especially at high peaking times, where the system is noisier. The most convenient way is illuminating the sensor with short pulses from a LED, whose statistics of photon emission should not contribute appreciably to the noise. Data for the pixel devices are generated with this method.

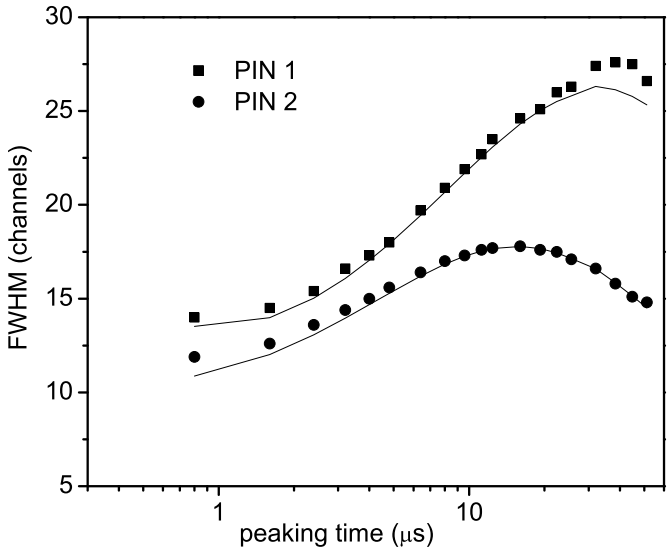

Figure 5.4: Scan of the FWHM noise (expressed in ADC channels) versus peaking time on devices PIN 1 and PIN 2, with output directly connected to PX4. Continuous lines are calculated with the measured parameter values. The gains of the amplification stage are different, so a comparative discussion of the noise in the two pixels is not possible at this level.

5.4 Measurements on Strip Detectors

The detector includes a Source-Follower at the end of each strip. The strip is DC coupled to the gate of the input JFET J_S of the SF. Since the strips are also provided with bonding pads, we have two different options for signal readout:

- CSA configuration, in which the strip is AC-coupled to the A250 preamplifier through an external capacitor;
- SF configuration, in which the output of the SF is AC-coupled to the A250 through a capacitor integrated on the detector wafer (this how the detector was intended to be operated).

In the following we discuss separately the two cases.

5.4.1 CSA Readout

An external 2 nF capacitor AC couples the strip to the input of the CSA. With reference to Figure 1.17(b), V_{DD} is set (by batteries) to 2.5 V, while V_{SS} and V_{GG} are at ground. In this way the strip is biased through the $4R$ voltage divider at $V_{DD}/2$, with an effective bias resistance of value R, which has been measured to be 0.8 MΩ. In these conditions, J_S is biased just barely into saturation; for good SF operation, a higher value of V_{DD} would be preferred, but here the SF is not used. For what concerns the noise, the effect of the SF is just to add the gate-drain capacitance of J_S to the input node of the CSA. The well calibrated 2.28 pF C_{test} mounted on

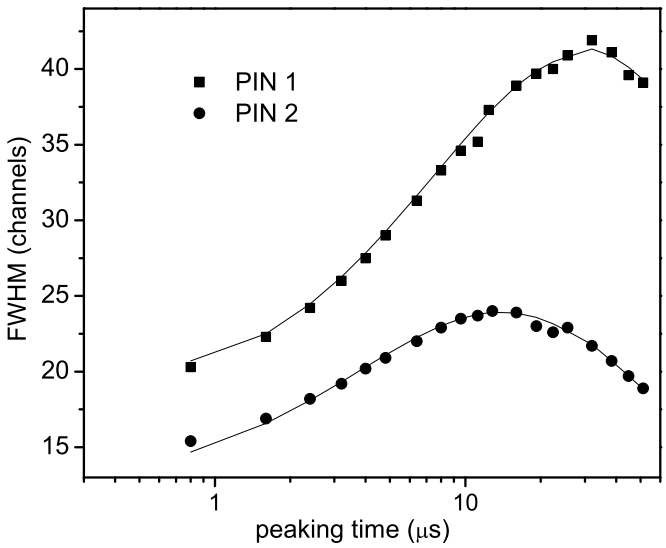

Figure 5.5: Scan of the FWHM noise versus peaking time on devices PIN 1 and PIN 2, connected to the A250 with capacitances of 8 and 67 pF respectively. As in Figure 5.4, the gains are different for the two curves, so the vertical scale does not have an absolute meaning.

the CSA board can be conveniently used to inject a charge signal into the detector.

We have two choices for the dealing with the neighboring strips:

- short the neighboring strips to ground for the signal, by connecting a large value capacitor between their DC pad and ground; in DC, all the strip remain biased at the same voltage, set by the resistive voltage divider;

- leave the neighboring strips "floating" in AC, i.e. biased only through the voltage divider, with an effective resistance to ground of $\sim$0.8 MΩ.

Noise measurements versus peaking time taken in both configurations are shown in Figure 5.7.

Neighbors grounded

Keeping the DC pads of the neighboring strips at ground (for the signal), we have again the standard configuration of a capacitive detector read out by the CSA, described in Chapter 4. Here the noise from nearby strips (due to their bias resistors and leakage currents) is not coupled, via the interstrip capacitance, to the strip under measure, but is shorted to ground. The capacitance seen by the input of CSA is the sum of the capacitances to the backside, to the bias ring, and to the adjacent strips (which we lump together under the symbol C_D), plus the gate-drain capacitance of J_S. The measured noise, because of the large parallel noise

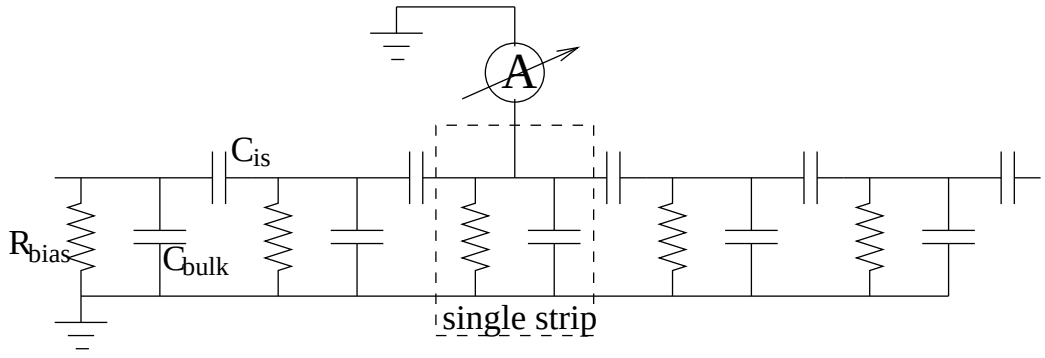

Figure 5.6: Schematic of the strip detector as used in the SPICE simulations. Every strip is represented by a capacitance towards the backside, in parallel with a bias resistance, plus a capacitance towards the neighboring strips. Values of the parameters are: R_{bias} =0.75 MΩ, C_{is} =7 pF, C_{bulk} =9 pF. In the case shown, an ammeter measures the noise current. If we are interested in measuring a noise voltage, a voltmeter replaces the ammeter.

contribution from R_{bias}, is not much sensitive to series noise and then to total capacitance. From the data of Figure 5.7 a total input capacitance of roughly 36 pF can be estimated; by subtracting the well known C_{in} of the CSA (13 pF), we get $C_D + C_{GD} \sim 23$ pF. From the same noise data we can instead obtain a good measure of the effective bias resistance, which is found to be 0.75 MΩ, slightly less than the DC measured value.

Neighbors floating

The strips are polarized by the $4R$ voltage divider; in AC, they see an effective bias resistance to ground given by $2R||2R = 0.75$ MΩ. In this condition the noise of the other strips (dominated by the contribution of their bias resistance) is coupled via interstrip capacitances to the strip under measure.
In order to estimate this noise we must solve a network of resistors and capacitors, representing the strips of the detector. Since the analytical solution is not simple, we analyzed the circuit shown in Figure 5.6 with the help of a SPICE circuit simulator [38]. A strip is represented by the parallel of a capacitance and a resistance towards ground with two interstrip capacitances towards the neighboring strips. The resistance has the value determined from the noise measurement with neighboring strips at ground in AC. For the interstrip capacitance we use the value (7 pF) obtained from direct measurements; in order to sum up to 23 pF as previously estimated for the $C_D + C_{GD}$ capacitance, the capacitance to ground in the network of Figure 5.6 must be $\sim (23 - 2 \times 7)$pF $= \sim$9 pF.
The simulator adds in series to each resistor its noise voltage source $\frac{\mathrm{d}v^2}{\mathrm{d}f} = 4kTR_{bias}$ or, in parallel, its Thevenin equivalent $\frac{\mathrm{d}i^2}{\mathrm{d}f} = \frac{4kT}{R_{bias}}$. Since we are interested in a current noise, an ammeter is used to read it.
The resulting noise current spectral density at the CSA input, in the frequency range of interest (5 to 500 kHz), can be fitted as:

$$\sqrt{\frac{\mathrm{d}i_n^2}{\mathrm{d}f}} = 1.72 - \frac{0.236}{1 + (\frac{f}{14.14\,\mathrm{kHz}})^{1.77}}(10^{-13}\frac{A}{\sqrt{Hz}}) \qquad (5.14)$$

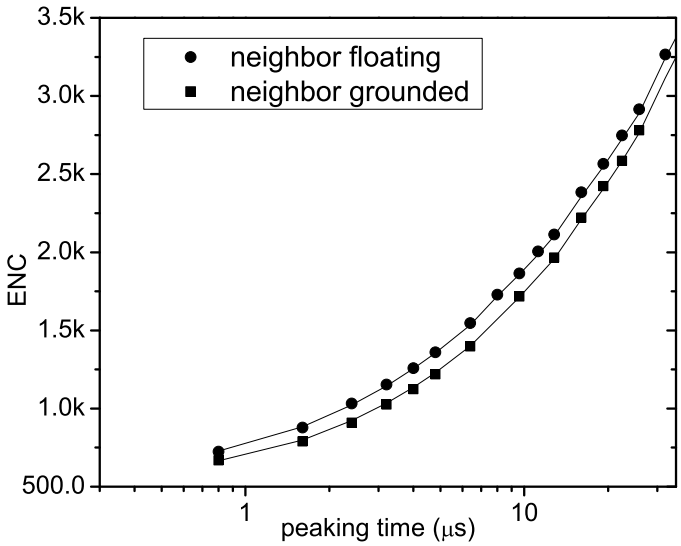

Figure 5.7: Noise measurements on strip detector with the strip AC-coupled to the CSA, bypassing the integrated SF stage. The JFETs are polarized with V_{DD} = 2.5 V and V_{SS} = 0 V. With neighboring strips grounded, the model used in Chapter 4 can be directly applied; with the strips floating (actually, connected to ground by a 0.75 MΩ effective resistance), a numerical calculation must be performed in order to estimate the expected ENC.

The contribution of this noise at the output of the shaper has been determined by numerically calculating the integral:

$$ENC^2_{parallel} = \int_0^\infty \mathrm{d}\omega \, \frac{\mathrm{d}i_n^2}{\mathrm{d}f} \frac{|T(\omega)|^2}{\omega^2} \tag{5.15}$$

where $|T(\omega)|^2$ depends on the trapezoidal shaping parameters τ and FT (equation 3.3).
This term is just the contribution of the parallel noise of the detector. We must add in quadrature other noise terms like the series noise of the CSA input FET and the $1/f$ noise. The result is shown as a continuous line in Figure 5.7, together with the measured experimental points.
It can be seen from the plot that, by increasing the peaking time (i.e. going to low frequencies), the relative difference between the two curves decreases; this happens because the impedance of C_{is} increases at low frequency, cutting off the noise current originating from the other strips. This can also be seen from equation 5.14: in the low frequency limit the noise reduces to just $\sqrt{\frac{\mathrm{d}i^2}{\mathrm{d}f}} = \sqrt{\frac{4kT}{R_{bias}}}$, with R_{bias} =0.75 MΩ, i.e. the contribution of the resistance biasing the strip under test.

5.4.2 Readout with Source-Follower

This is the way these strips were intended to be used: taking the signal from the output of the SF through the integrated coupling capacitor C_A (Figure 1.17(b)).

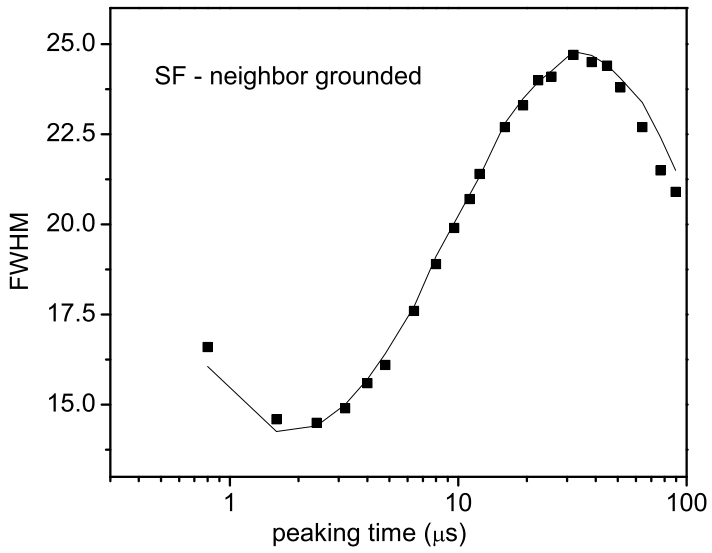

Figure 5.8: Noise measurement on strip detector taking the signal from the integrated C_A, after the SF stage. C = 26 pF, R_S = 500 Ω, R_{bias} = 0.75 MΩ. Neighbor strip are grounded, so we fall in the case of the previously seen pixels.

Due to space limitations on the wafer, the value of C_A is only 22 pF, slightly less than the capacitance $C_D + C_{GD}$ seen by the gate of J_S. V_{DD} is set by batteries to 3 V, while $V_{SS} = V_{GG} = 0$. The strips are biased at $V_{DD}/2$ =1.5 V. Static characterization of the SF has shown that this is a convenient working point. The parameters of J_S entering into noise expressions cannot be directly measured on the devices connected to the strips, because its source terminal is not externally accessible; however, devices with the same layout are included in test structures and have been characterized (Chapter 1). We obtained: $g_{m,J_S} = 1.0$ mS, $C_{GD} = 3.0$ pF.
The JFET J_C has gate and source connected together, making it impossible to measure the transconductance; since no test structure with the same geometry exists on the wafer, we can only rely on scaling considerations.
The bonding pad present on every strip can be exploited to inject a signal charge through an external 1 pF capacitor C_{test} (properly terminated with 50 Ω to ground).
Again, we can choose to leave the adjacent strips floating, or clamp them to GND with a large capacitor.

Neighbors grounded

In this configuration, we are back to the case of the pixels, since the nearby strips do not contribute to the noise. By acquiring the signal waveform at the output of the CSA with a digital oscilloscope, we could determine its decay time, which reproduces the decay time of the voltage signal on the strip. From this we can get a good estimate of $C_D + C_{GD} + C_{test}$, since R is well determined by previous measurements with CSA read-out. The decay time is 18.8 μs. Then, given the

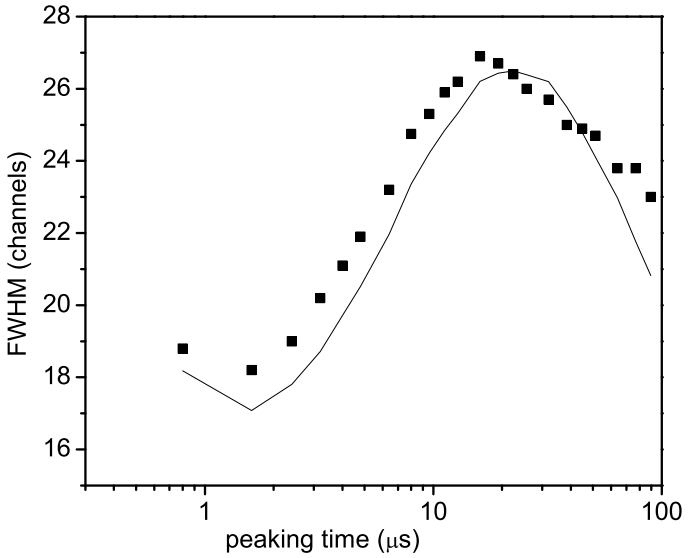

Figure 5.9: Noise measurement on strip detector taking the signal from the integrated C_A, after SF stage. Neighbors strips are floating, as in the expected SF configuration. Numerically calculated curve comes from integration 5.19, with noise voltage expression given by a SPICE simulation of the model of Figure 5.6, with the same parameters used in Figure 5.7.

value $R_{bias} = 0.75$ MΩ, a total capacitance of 25 pF (1 pF out of these 25 pF is due to C_{test}) can be deduced.
The calibration of the charge injection at the input is not straightforward: the noise of these structures is indeed high, given the low value of the bias resistor. As a result, the 60 keV X-ray peak is not well separated from the noise and is clearly visible only at the lowest peaking times.
Moreover, the injected charge depends on the ratio of C_{test} to the total capacitance of the detector node (input of the SF). Indeed, because of the high input impedance of the SF, the strip is not kept at virtual ground as it was with CSA readout, so the real injected charge is not simply $Q_0 = C_{test} v_{in}$, but less, depending on the voltage divider built-up by the capacitances C_{test}= 1 pF and $C_D + C_{GD}$= 24 pF:

$$Q_0 = C_{test}(v_{in} - v_{strip}) = C_{test} v_{in}(1 - \frac{\frac{1}{24pF}}{\frac{1}{24pF} + \frac{1}{1pF}}) \tag{5.16}$$

where v_{in} is the square wave amplitude applied to C_{test}.
Comparing the signal pulse height generated by Q_0 with the one due to the 16.6 ke released by the 60 keV photons we can, as in the case of the pixel, determine the gain of the whole system.
The measured noise data are shown in Figure 5.8 together with the expected ones, where a further 1 pF is added to the total capacitance in order to better fit the data.

Neighbors floating

In this configuration, predicting the noise level is rather difficult and we cannot give an accurate analytical expression for it. It is similar to the case shown in Figure 5.7, in which the signal is taken from the DC pad while the neighboring strips remain floating. As in that case, we must rely on SPICE simulations. Referring back to the sketch shown in Figure 5.6, the ammeter must be replaced by a voltmeter, since we are sensing a noise voltage [2]. With the same parameter values of the previous simulation, the output expression for the noise voltage spectral density is:

$$\sqrt{\frac{\mathrm{d}v^2}{\mathrm{d}f}} = \frac{1.1510^{-7}}{1+(\frac{f}{19.25\,kHz})^{1.24}}\frac{V}{\sqrt{Hz}} \tag{5.17}$$

for frequencies ranging from DC to 70 kHz and:

$$\sqrt{\frac{\mathrm{d}v^2}{\mathrm{d}f}} = 1.1810^{-3} f^{-0.983}\frac{V}{\sqrt{Hz}} \tag{5.18}$$

for frequencies from 70 kHz to 10 MHz.
At low frequency, where C_{is}, coupling the strip under test to its neighbors, has a high impedance, the noise is dominated by the bias resistor of the strip itself ($\sqrt{\frac{\mathrm{d}v^2}{\mathrm{d}f}} = \sqrt{4kTR_{bias}}$). At high frequency, the interstrip capacitances are shorted and the noise voltage at the SF input is generated by the parallel combination of many bias resistors, giving a lower level of voltage noise.
The r.m.s. noise at the output of the shaper can be obtained from the noise voltage spectral density given above at the SF input, by numerically evaluating the integral:

$$\sigma^2 = (A\frac{C_A}{C_f})^2 \int_0^\infty \mathrm{d}\omega\, \frac{\mathrm{d}v^2}{\mathrm{d}f}|T(\omega)|^2 \tag{5.19}$$

The gain term, expressed by the product $A\frac{C_A}{C_f}$, has been determined from the previous measurement with neighbors grounded. The set up, indeed, has been kept identical in the two configurations, apart from the removal of the 2 nF capacitances between the DC pads of the adjacent strips and ground.
The agreement, as can be seen in Figure 5.9, is not at the level of the previous case (Figure 5.8). Anyway, the general behavior is reproduced.

The waveform in this latter case is worth a separate discussion. It is not a simple exponential decay: the injection of a charge into a strip initially rises it to a potential: $v_{hit,0} = \frac{Q_0}{C'}$, where C' is the capacitance between the strip, connected to the gate of J_S, and all other electrodes kept at constant voltage (at ground in AC). Contrary to the previous case, the other strips are not grounded and they charge up through the voltage divider given by the interstrip capacitance C_{is} and their own C'. Referring to Figure 5.10, and calling v_{near} the voltage of the adjacent strip, we expect at time zero:

$$v_{hit,0} = \frac{Q_0}{C'} \tag{5.20}$$

$$v_{near,0} = \frac{Q_0}{C'}\frac{C_{is}}{C_{is}+C'} \tag{5.21}$$

[2] This is due to the high input impedance of the SF. By contrast, the low input impedance CSA was sensitive to the noise current.

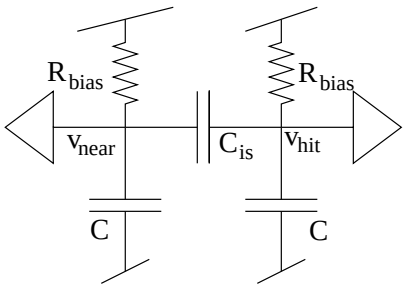

Figure 5.10: Sketch of two nearby strips for the calculation of waveforms generated by a charge released in one of the strips.

In this way, the signal spreads from one strip to the nearby ones, a so called cross-talk effect. An analogous argument holds for the other nearby strips, but, since the voltage divider is made up by more capacitances as we move away from the hit strip, the signal on those strips is expected to be smaller. Moreover, since just one strip is actually collecting the charge, the pulses from the other strips must have a bipolar shape with zero area. An example of acquired pulses is shown in Figure 5.11. To calculate the time dependence of the signal for the very schematic layout of Figure 5.10, we must solve the two differential equations expressing the Kirchhoff current law for the two strip nodes:

$$\begin{cases} \frac{v_{near}}{R} + C\frac{\mathrm{d}v_{near}}{\mathrm{d}t} + C_{is}\frac{\mathrm{d}(v_{near}-v_{hit})}{\mathrm{d}t} = 0 \\ \frac{v_{hit}}{R} + C\frac{\mathrm{d}v_{hit}}{\mathrm{d}t} + C_{is}\frac{\mathrm{d}(v_{hit}-v_{near})}{\mathrm{d}t} = 0 \end{cases} \tag{5.22}$$

The simplest way to solve the system is through a Laplace transform, but the calculation quickly diverges in complexity. A first order approximation that can be done is to set $C = C_{is}$, translating in a simple relation between the zero-time potentials of the two strips: $v_{hit,0} = 2v_{near,0}$. The signal from the hit strip is then found to be:

$$\begin{cases} v_{hit}(s) = \frac{3}{2}v_{hit,0}RC\frac{1+s2RC}{1+4sRC+3s^2(RC)^2} \\ v_{hit}(t) = \frac{1}{4}v_{hit,0}(3e^{-\frac{t}{RC}} + e^{-\frac{t}{3RC}}) \end{cases} \tag{5.23}$$

whose time integral is $\int v_{hit}(t)dt = \frac{3}{2}RCv_{hit,0}$. The solution is the sum of two exponential decays, with time constants RC and $3RC$; in the more general case of $C_{is} \neq C$, the two time constant are RC and $RC + 2RC_{is}$. The signal from the neighboring strip is:

$$\begin{cases} v_{near}(s) = \frac{3}{2}v_{hit,0}RC\frac{sRC}{1+4sRC+3s^2(RC)^2} \\ v_{near}(t) = \frac{1}{4}v_{hit,0}(3e^{-\frac{t}{RC}} - e^{-\frac{t}{3RC}}) \end{cases} \tag{5.24}$$

very similar to the previous one, but with a "-" sign, leading to a null integral. The time constants are the same.
If we inject a charge in the detector with a light pulse from an LED instead of using the C_{test}, nearly the same charge is injected on every strip, so they all charge up at the same voltage. As a result, the interstrip capacitances C_{is} do not charge up. The resulting waveform is the same on every strip: it is a single exponential decay, with a time constant much shorter with respect to the case of injection through C_{test}. This is due to the fact that the effective strip capacitance is much

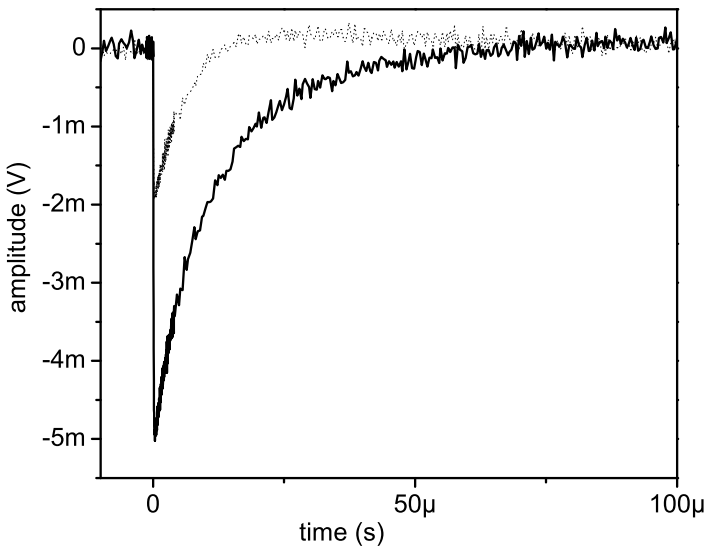

Figure 5.11: Acquired pulses on two nearby strips: the larger one, called v_{hit} in the text, is unipolar and comes from the hit strip; the smaller (v_{near}) is bipolar, with zero area, and comes from a first neighbor. As in Fig. 5.1, in order to show clean waveforms, the noise has been averaged out over many pulses.

smaller if the interstrip capacitances do not contribute. The noise, however, has been verified to be independent of the charge injection method, since it is not related to signal charge generation, but depends only on the characteristics of the detector under test.

Chapter 6

Comparative Discussion of the Experimental results on CSA and SF

An experimental comparison of SF vs CSA read-out methods has been already carried on in [39]. In that work, a low capacitance detector, used for X-ray spectroscopy, had the first JFET of the front-end electronics integrated on the same silicon substrate of the detector, and served as input device for both the SF and CSA readout configurations. All the other components of the amplifier have been placed outside the chip. The reset of the signal and leakage current charge was achieved by means of both pulsed and continuous methods, avoiding the R_{bias} and its thermal noise. It was pointed out that, considering null noise contribution of the external amplifier, the S/N performances should be equal for the two read-out methods, since the noise sources, as long as the FET is made working at the same biasing point, are the same and the amplification affects in the same manner both signal and noise. We add that, since the C_{GS} capacitance of the input FET does not contribute in the SF, SF could be even better. However, the paper shows that with the SF a much poorer linearity is achieved than with the CSA: with the latter, the output voltage of the preamplifier is directly linked to the signal charge via the feedback capacitance, a very stable parameter, whereas the SF links just the output voltage with the gate voltage of the first JFET, without making a precise conversion in advance between the input voltage and the signal charge. This relationship depends on the capacitance at the input node (sum of C_D, C_{GD} and strays) and for spectroscopic detectors (having small capacitance), significant variations with detector and FET bias are expected (and observed). Variations with temperature are observed too to be much more severe in SF than in CSA read-out. It may be stated that in an environment with controlled bias and temperature their performances are at the same level. However, it is not the case: the signal and leakage currents are integrated at the input node, shifting the polarization point of the FET and then its capacitances. In the SF, this causes a variation of the gain with a broadening effect of X-ray lines, similar to the effect of the noise.

Particular care should be taken in the choice of the reset method. A pulsed reset method, removing the charge only at fixed time intervals, should be avoided because then pulses arriving at different times are amplified at different levels. A

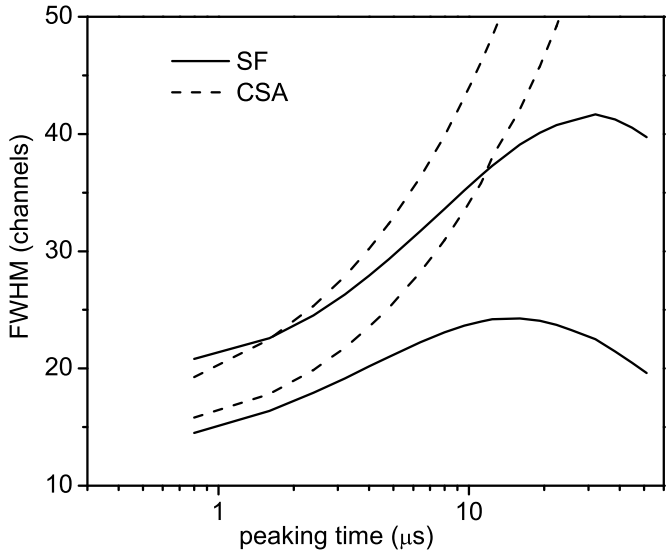

Figure 6.1: Plots of the measured FWHM noise for the PIN 1 (upper curve) and PIN 2 devices; also shown the expected noise with CSA read-out (with the same pixel parameters).

continuous reset, as a diode in parallel to the detector, is to be preferred, allowing currents from the detector to flow through its forward biased junction, whose potential drop is set by the amount of current.
In our devices, even if a parasitic diode could be a viable alternative, a polysilicon R_{bias} was chosen as a path to the currents, because of its simplicity. The noise performances, of $J_C$course, worsen. Static characterizations on FETs showed a spreading in the values of capacitances, so the gain is expected to vary from strip to strip. This issue is absent in the CSA read-out method, since the gain depends only on the well determined parameter C_f, in every case external to the detector chip. In a severe environment like a collider, a continuous calibration of the capacitance (measuring the gain) should be performed, but this is impractical.
Already these considerations on the signal make the classic CSA a better choice: but let's consider other features of the two readout configurations.

In the following analysis, we concentrate on noise issues.
In Chapter 2, when comparing the SF with the CSA, we made some crude approximations:

1 - C_{GD}, the capacitance of gate-drain junction of the input JFET of the SF, is negligible with respect to the detector capacitance C_D;

2 - R_S and A_f (the flicker noise coefficient) are negligible for the input transistor of the SF;

3 - $A_{f,1}$ of the input FET of the CSA is zero;

4 - the JFET current source J_C is noiseless.

Contrary to what done in [39], the noise coming from the external amplifier has been taken into account.
Approximation # 3 has been introduced to simplify the calculations, leading to a simple relation between the transconductances of J_S and J_1, derived in equation 2.70; obviously it does not hold in real situation, and in our case the coefficient entering noise expressions is a well determined parameter with value $1.6\,10^{-12}$ V^2.
Approximation #2 refers to an ideal low-noise JFET, fabricated for spectroscopic applications. The flicker noise coefficient on our integrated J_S and J_C JFETs are, as measured, really negligible, less than 10% of the noise of 2SK152; R_S, on the other hand, is very large, $\sim 400\ \Omega$, due to some design limitations.
Approximation # 4 is a good one, since the noise term coming from J_C can be made smaller than the noise term of J_S:

$$4kT\Gamma\frac{g_{m,C}}{g_{m,S}^2} < 4kT\Gamma\frac{1}{g_{m,S}} \tag{6.1}$$

To discuss properly item # 1, it is better to go in deeper detail, splitting the devices studied in high and low value capacitance: namely strips and pixels.
As usual, we start from the pixels.

6.1 Pixels

The PX4 digital filter is not able to shape correctly input exponential falls with time constant less than 36 μs, as is the case of our pixels. A signal pulse height deficit, function of the peaking time, will occur. This is not the case with the CSA, whose long decay time comes from the product R_fC_f of the feedback path. The signal, then, is processed correctly, giving, independently of the peaking time, an unvarying signal amplitude at the output. In this condition, the CSA is better than the SF, from the point of view of the ENC, especially at long peaking times.
In the following, we suppose to have the same signal for every peaking time, given, at the input of PX4, by Q_0/C_f in the case of CSA and $\frac{Q_0}{C_D+C_{GD}}\frac{C_A}{C_f}$ in the SF case. Figure 6.1 shows a summary of the experimental data taken from both pixels, PIN 1 and PIN 2, already shown together in Figure 5.5. Also shown is the expected value for a CSA configuration, that would be measured with the same gain of the whole acquisition set-up.
Relation 2.70 gives, for the transconductance $g_{m,S}$ of J_S of PIN 1, a minimum value of 3 mS, with the C_D and C_A values used in this particular noise measurement. In the same way, for PIN 2, relation 2.70 gives a minimum value for $g_{m,S}$ of 0.4 mS. Both conditions are largely satisfied, so the fact that the noise in CSA is less than the noise in SF for PIN 1 for short peaking times - when series noise dominates -, must be due to some not well verified approximation, listed in item #1 through #4.
Anyway, at longer peaking time, the CSA becomes much noisier than the SF, due to the Johnson noise of the 3 MΩ resistance which starts contributing as series noise in SF read-out, then giving a noise contribution decreasing with peaking time. At high frequency (low peaking times), the 3 MΩ acts as a parallel noise source, for both set-up. Its contribution to the total noise is the same for both SF and CSA read-out methods.
Since parallel noise cannot explain the different behaviour of the two read-out

at low peaking times, this difference must then arise from series contributions, expressed below. Series contributions in the CSA case are proportional to :

$$(C_D + C_{in})\sqrt{\frac{1}{\tau}4kT(\frac{\Gamma}{g_{m,1}} + R_{S,1}) + A_{f,1}} \tag{6.2}$$

The numerical value of the square root, using the parameters of the used set-up, is 2.1 10^7 V^2. For the SF:

$$(C_D + C_{GD})\frac{C_A + C_{in}}{C_A}\sqrt{\frac{1}{\tau}4kT(\frac{\Gamma}{g_{m,1}} + R_{S,1}) + A_{f,1}} + \tag{6.3}$$

$$(C_D + C_{GD})\sqrt{\frac{1}{\tau}4kT(\frac{\Gamma}{g_{m,S}} + R_{S,S})}$$

if the flicker noise of J_S and the noise from J_C are neglected.
The numerical value inside the second square root is 4.7 10^7 V^2, with the parameters of the system.
It is bigger because of the 400Ω of $R_{S,S}$. Having fixed all parameters but the capacitances, the condition for which the CSA is worse than the SF translate in a relation among them:

$$(C_D + C_{in}) > (C_D + C_{GD})\frac{C_A + C_{in}}{C_A} + 1.5(C_D + C_{GD}) \tag{6.4}$$

where $1.5 = \sqrt{2.1\,10^7}/\sqrt{4.7\,10^7}$.
Supposing that the above relation holds for both pixel types, and substituting the parameters $C_A = 8$ pF or 67 pF, $C_D = 1$ pF and $C_{in} = 14$ pF we get a condition for C_{GD}.
For $C_A = 8$ pF, equal to the capacitance used in the PIN 1 measurement, $C_{GD} <$ 2.5 pF for SF to be better than CSA: this condition is satisfied by PIN 2, having a $C_{GD} = 1.8$ pF but not by PIN 1 having $C_{GD} = 4.6$ pF; this explains why in the Figure 6.1 PIN 1 has worse noise performances than CSA.
$C_A = 67$ pF, as used for PIN 2, sets the upper limit of C_{GD} at 4.5 pF, then again SF is a better choice for PIN 2 (as seen in Figure 6.1) but for PIN 1 we need an even bigger C_A.

In Figure 6.2, it is shown the maximum C_{GD}, in function of C_A, for which the SF gives better noise performances than CSA.

6.2 Strip

The strips with integrated SF show several limitations, related to their particular design and also to some unavoidable intrinsic characteristics, making them unfit to be used for tracking purposes in high energy physics experiments.

Design Limitations

Some limitations belong to the specific detector under study and could be corrected with a suitably modified design:

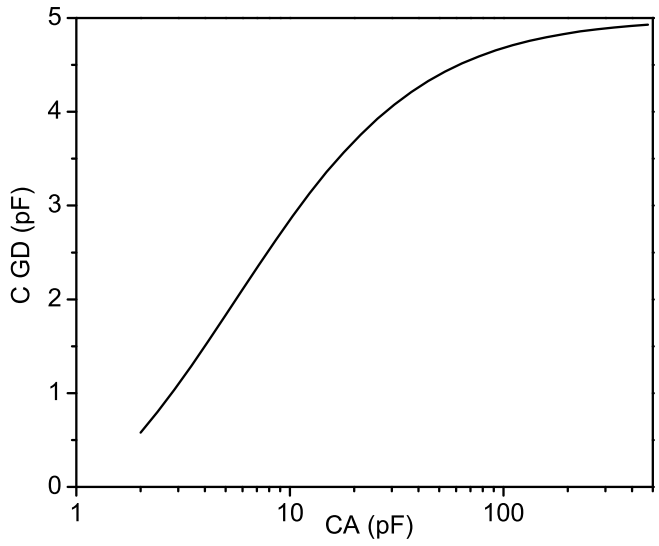

Figure 6.2: Plot of the maximum C_{GD} of J_S in function of the coupling capacitance C_A, for which - theoretically, according to 6.4 - SF is better than CSA. The parameters used are: $C_D = 1$ pF, $C_{in} = 14$ pF, $g_{m,1} = 13$ mS, $g_{m,S} = 10$ mS, $A_{f,1} = 1.6\,10^{-12}$ V^2, $R_S = 400\ \Omega$

- the integrated coupling capacitance C_A is only of 22 pF, less than C_D; in this way, strips read by SF cannot hold a comparison with CSA read out, since the first condition for obtaining a better noise performance from the SF compared to the CSA the opposite condition: $C_A > C_D$.

- the small current, generated by J_C, sets the V_{GS} of J_S to a value of -0.77 V and to a small value for the transconductance $g_{m,S}$. This makes series noise significant, as can be seen in Figure 5.9 or 5.8 where the minimum noise is achieved for 1.6 μs of peaking time, greater than the minimum allowed by the shaper.

- the big value of series resistance, due to the incomplete metallization of the gate implant, increases the series noise too.

Intrinsic Limitations

Even though the JFETs of the SF draw a relatively low current, the power dissipation is ~ 1 mW/channel ($I_{\text{drain}} = 0.3$ mA $\cdot V_{DD} = 3$ V). This thermal budget is enterely produced inside the detector substrate, which would require to be cooled. Of course, the cooling of the CSA stage is also needed.
Moreover, charge collected in one strip induces signals on the neighboring strips, giving a sizable cross-talk. This would help the signal interpolation of course; however, it leads to high occupancy, increased dead times and, possibly, event losses.

Conclusions

In this work, among all types of silicon detectors, we concentrate upon the microstrip ones. The goal was, on one side, to investigate the noise sources in microstrip detectors – with particular attention to the contribution of the punch-through biasing mechanism – and on the other side to compare two different approaches for the readout of signals: the classic charge sensitive amplifier (CSA) and a less common Source Follower (SF) integrated with the sensor as first amplification stage.

The strip sensors read out by the CSA are of the type used in the Inner Tracking System of the ALICE experiment; they come in three different versions, supplied by three manufacturers. The detectors with integrated SF are test devices designed for evaluation purposes, in view of a possible utilization of this readout scheme in High Energy Physics experiments.

The study of both detector types started with a static characterization of the devices, in order to verify their functionality and to measure the values of the parameters entering into noise expressions.

On the ALICE-type detectors, in addition to the standard tests performed to verify the quality of the sensors, some more detailed measurements have been made. In particular, the interstrip capacitance and related dissipation factor (to complete the information about the interstrip admittance) have been measured as a function of both frequency and bias voltage.
We found that at bias voltages above substrate depletion both capacitance and dissipation factor still show a substantial dependence on frequency. Only at bias voltages much above depletion this dependence flattens out.

This observed behaviour has been attributed to the presence of resistive layers, such as electron accumulation at the interface – or the p-spray implant in one sensor type – which at low frequency strongly couple one strip to the other strips of the detector. At a sufficiently high bias voltage, the electron accumulation channels (but not the p-spray implant) in between the strips become insulated from each other, because of the depletion of the narrow region between the strip end and the bias ring. Then the long-range coupling between the strips is no longer present and the capacitance and dissipation factor become independent of frequency. This point has been verified by 3D numerical simulations.

Detailed measurements of noise have been performed, exploring its dependence upon a wide set of parameters: the diode polarization method (resistor or punch-through), the shaping time, the leakage and the punch-through currents, the detector bias voltage. Photogeneration and direct injection – through the DC pad of the strip – has been used to vary over a wide interval the leakage and the punch-through currents, independently of each other.

It has been found that the current flowing by punch-through contributes an additional shot noise term, added in quadrature to the contribution of the leakage current. This suggests that fluctuations in the two currents are uncorrelated, i.e. the arrival of carriers on the strip from the bulk is uncorrelated to their emission towards the guard ring. Since the punch-through mechanism involves the "thermionic-like " emission of carriers above a potential barrier, it is expected to be subject to shot noise fluctuations, at least until space charge effects become important, smoothing out the fluctuations ([8], p. 221). However, if the fluctuations in punch-through current were (to consider the extreme case) completely

correlated to the fluctuations in leakage current, they would bring no additional contribution to the detector noise.

An unexpected noise contribution related to punch-through has been found on the p-side of one type of sensors. Unlike shot noise, which is proportional to the square root of current and shaping time, this new contribution is directly proportional to both the punch-through current and the shaping time. Its power spectral density can be described as a *parallel* flicker $(1/f)$ noise: $\frac{di^2}{df} \propto \frac{I_{PT}^2}{f}$.
A similar dependence of excess noise on the shaping time has been reported in the literature [34],[33]. However, it has been observed only in irradiated detectors, and the reported dependence on leakage current was the same as for normal shot noise, i.e. square root of I, while we observe a linear dependence, at least at moderate current values.

The bias voltage, once the sensor is totally depleted, is not expected to have a significant influence on noise, the only effect being due to a slow decrease in capacitance. Instead, an extra noise contribution has been observed, which can be parameterized as a noise current power spectral density: $\frac{di^2}{df} \propto \sqrt{f}$.
This excess noise is present precisely for those detectors and for those bias voltages for which the capacitance and dissipation factor were not flat versus frequency. It is then natural to relate the origin of this noise to the presence of resistive layers surrounding the strips. The physical mechanism responsible for this noise is not clear. In the literature, an observed excess noise has been attributed to resistive lines (p-stops), and described in terms of thermal noise associated with the resistance, capacitively coupled to the adjacent strips [40]. However, this noise mechanism would be characterized by a frequency dependence completely different from the one we observed.

Our versatile measurement set-up began to show its limitations in the study of detectors with integrated source follower.
In this case, the output signals from the preamplifier have an exponential decay with a time constant which is set by the RC constant of the detector. For the relatively low value of the bias resistors present in our devices, this time ($\sim$20 μs) is too short to be correctly processed by the PX4 shaper.
However, by using the known transfer function of the shaper we are still able to derive analytical expressions for both the noise and the signal as a function of the peaking time selected. It is important to remark that in these conditions the signal amplitude is no longer independent of the peaking time, but decreases when peaking time increases. This is due to a limitation in the pole-zero cancellation circuit of the PX4, which cannot properly handle signals with a decay time shorter than 36 μs. By using a different shaper or, better, by increasing the value of the bias resistor integrated on the detector (a resistance 10 times larger could be easily obtained, giving a decay time of $\sim$200 μs), this limitation could be overcome. Because of this, in estimating the signal to noise ratio we assume that the filtering-shaping stage is able to give an output signal whose amplitude is independent of the peaking time.

The noise model developed in Chapter 2 was first checked with single pixels; their design allows to connect, between the SF and the following stage, an external capacitor C_A, whose value can be conveniently chosen. This capacitance enters into noise and signal expressions: the signal amplitude and the noise due to the input node (detector and SF) are both proportional to C_A so that its value does

not affect the signal to noise ratio as long as the noise of the following CSA stage is negligible. The measured signal and noise dependence on the peaking time has been found to agree with the model.

Comparing the results with those expected from a pixel sensor having the same parameters (capacitance, leakage current, bias resistance) but read out by a CSA, it is found that the SF approach is actually better for low enough values of the capacitance C_{GD} of the input FET of the SF. Indeed, for the device called PIN2, having $C_{GD,J_S} = 1.8$ pF, the SF gives better noise performance for every value of the peaking time (we recall that we are assuming the signal amplitude to be independent of the peaking time); on the other hand, pixel PIN1, having $C_{GD,J_S} = 4.6$ pF, is found to be worse than the CSA at short peaking times, where series noise dominates. For very long times, the SF is much better than CSA.

With strip detectors the situation is more complicated. Because of the high impedance of the SF, the strips are floating in AC, rather than kept at virtual ground as in the CSA case. Then signal and noise in one strip are induced on neighboring strips via the interstrip capacitance, and we must rely on circuit simulation to predict the signal and noise behavior. By simulating the detector with a network including the interstrip and backside capacitances and the bias resistors, we were able to reproduce, although not as well as for the pixel case, the experimental data.

A comparison with the CSA readout is hopeless for this strip detector. The coupling capacitance C_A integrated on the sensor is slightly smaller than the total capacitance of the input node. This fact alone implies that the signal to noise ratio with the SF readout must be worse than for the CSA readout.
It must be considered that in microstrip detectors, having a large density of readout channels, the space available for the coupling capacitance is very limited, so that it is difficult to significantly increase its value.

A further drawback of the SF readout in multielectrode detectors with strong capacitive coupling between the elements (such as strip detectors) is the important cross-talk, due to the high input impedance of the SF.

Appendix A

Instruments for static characterization of devices

Capacitance measurements

For capacitance-voltage ($C-V$) or capacitance-frequency ($C-f$) measurements, an HP 4284A "Precision LCR Meter" is employed. The instrument measures, within a wide frequency range, the (complex) admittance of the circuit network connected between its "LOW" and "HIGH" terminals. The measurements is carried on with the four terminal Kelvin method: two terminals force the current, the other two sense the potential [12]. The HIGH current terminal outputs a sinusoidal signal, with frequency f in the interval from 20 Hz to 1 MHz and rms amplitude v_{AC} ranging from 5 mV to 1 V, superimposed to a DC bias voltage (Figure A.1). The LOW current terminal closes the current path to common through a vector amperometer, measuring the in-phase and the $\frac{\pi}{2}$ out-of-phase components of the small signal current flowing in response to the sinusoidal voltage. A high-impedance vector voltmeter measures the amplitude and phase of the voltage drop across the device under test. Since in our case the impedance of the connections is negligible with respect to the impedance to be measured, we can use a simpler two-terminal setup, by shorting together directly at the output of the instrument the HIGH potential to the HIGH current terminal, and similarly the LOW potential terminal

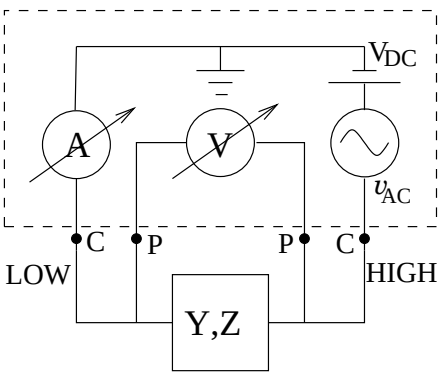

Figure A.1: Schematic of the instrument HP 4284A for impedance measurements in the frequency domain. A "four-terminal" connection to the device under test is also shown.

to the LOW current one.

Using complex notation for the amplitudes, we can relate the AC current to the voltage through a complex admittance $Y = G + iB = 1/Z$:

$$i_{AC} = Y v_{AC} = (G + iB) v_{AC}$$

The instrument can display the result of the measurement (the complex admittance or impedance) in several equivalent ways: for example, the module of the admittance or the impedance vector and the angle θ it makes with the real axis in the complex plane, or the real and imaginary parts of either vector, or it can give the values of a resistive and a reactive component, making up - either in parallel or in series combination - the measured admittance.
Since for our devices the reactive component of the admittance is essentially capacitive (rather than inductive), the two common ways of representing the network are through a resistance and a capacitance in series or in parallel ([12], pag 116).

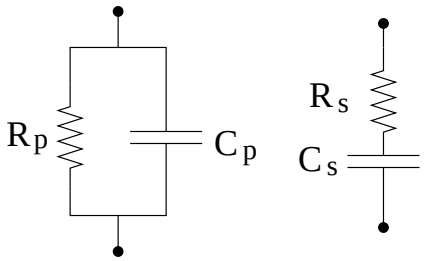

Figure A.2: Parallel and series RC models of the device under measurement.

Consider first the model in which the two lumped elements are in parallel: calling them R_p and C_p, the admittance is the sum of the admittances of the two branches in the left-side diagram of Figure A.2:

$$Y = G + iB = \frac{1}{R_p} + i\omega C_p$$

The "dissipation factor" D is defined as the ratio between the real and the imaginary parts of the admittance:

$$D = \frac{Re(Y)}{Im(Y)} = \frac{1}{\omega C_p R_p}$$

In the series model, with components R_s and C_s, the impedance of the network is given by the sum of the two impedances:

$$1/Y = Z = R_s - i\frac{1}{\omega C_s}$$

Because of the relation between a complex vector and its inverse, it is immediate to verify that the dissipation factor can be expressed in terms of the impedance as:

$$D = \frac{Re(Y)}{Im(Y)} = -\frac{Re(Z)}{Im(Z)} = \omega R_s C_s$$

From the equality $Y = 1/Z$, by writing Y in terms of R_p and C_p and Z in terms of R_s and C_s, we can derive the relation between the parameters of the series and the parallel models:

$$R_s = R_p \frac{D^2}{1 + D^2}$$

$$C_s = C_p(1 + D^2)$$

When measuring the admittance between two particular electrodes of the device under test we must connect all other electrodes of the device (plus any other close-by external electrode) to the instrument "common" (or "ground") terminal. In this way, the current flowing through these electrodes will return directly to common without being measured by the current meter and thus will not contribute to the measured admittance. In addition, because the other electrodes will be kept at constant (common) voltage, no current will flow between them and the LOW terminal. The situation can be illustrated by the simple example of the measurement of the bulk capacitance of a diode with guard ring (Figure A.3). For this measurement the backside of the wafer is connected to the HIGH terminal, the diode (D) to the LOW terminal and the guard ring (GR) to common. Only the displacement current through C_D is measured; the current through C_{GR} flows to common, while no current flows through the capacitance C_{IS} between the diode and the guard ring, since no voltage is applied across it.

It is often necessary to apply to the device a bias voltage exceeding the maximum value (40 V) of the instrument's internal DC power supply. To this purpose, the bulk terminal is connected to an external power supply through a resistance R_0 and to the HIGH terminal (carrying the v_{AC} signal) through a capacitance C_0. In order to ensure that the full v_{AC} voltage is applied to the backside contact, the capacitance and the resistance must be high enough for the conditions $C_0 >> (C_D + C_{GR})$ and $R_0 C_0 >> 1/\omega$ to hold.

The best choice between the parallel or the serial model depends not only on the device under study, but also on the measurement frequency and the bias voltage applied. In the above example of the diode, when the bias voltage is high enough to completely deplete the high resistivity substrate, only the small resistance of the thin and highly doped contacts will be present in series with the capacitance to be measured. In these conditions, the parallel model can accurately describe the real device. The series model can also be adequate, provided the leakage current is low or varies very little with bias voltage.

When the bias voltage is such that the substrate is only partially depleted, a significant series resistance may be present. If this series resistance gives the dominant contribution to dissipative effects, then the series model is appropriate. In this case the capacitance extracted with the parallel model will underestimate the real capacitance by the factor $(1 + D^2)^{-1}$. However, it is important to keep in mind that in the general case there will be both a parallel and a series resistance, so that neither model gives a faithful representation of the network; one must then try to choose the frequency in such a way that one of the two resistances gives a negligible contribution to the dissipation factor.

Current and voltage measurements

For current and voltage measurements (I-V, V-I or V-V), an HP 4156C "Precision Semiconductor Parameter Analyzer" is employed. The instrument has four inde-

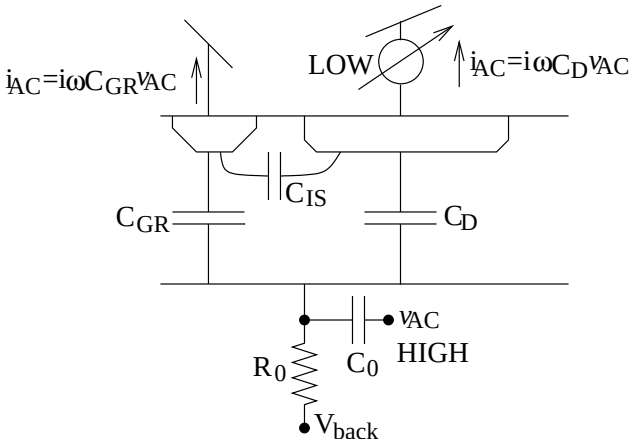

Figure A.3: Example of capacitance measurement with HP 4284A, showing that only the displacement current through C_D is measured by the LOW terminal.

pendent SMU (Source-Measure Unit) channels. Each channel can be configured to source voltage and measure current ("V-Mode") or alternatively to source current and measure voltage ("I-Mode"). The voltage range is $0 \div \pm 100$ V, the current range $0 \div \pm 100$ mA. The maximum measurement resolution (in the lowest ranges) is 1 fA for the current and 1 μV for the voltage. The SMUs are provided with separate "Force" and "Sense" terminals for remote voltage sensing in Kelvin-type measurements. Since in our measurements the voltage drop in the connections is almost always negligible in comparison with the drop across the device under test, we do not make use of the remote sensing option, thus keeping the connections much simpler. In some situations, notably when supplying a bias voltage through an RC filter, the drop across the connecting circuit may be significant; in this case we correct for the voltage drop by simply measuring the current and subtracting the IR product.

Appendix B

^{241}Am spectra

A spectrum of the radioactive source ^{241}Am has been acquired with every detector studied, in order to check its spectrographic properties.
Its most important lines are listed in table 3.1; in particular the 59.5 keV photon is well separated from the other less energetic lines and, interacting with silicon via photoelectric effect, it releases a charge of $1.65\,10^4\,e^-$, about 2/3 of the charge released by a m.i.p. traversing 300 μm of Si.
All CSA read-out spectra in this appendix are taken using the same set-up, with the same gain value of the amplification chain. The zero of energy is at channel zero (this is a nice feature of PX4 digital shaper).

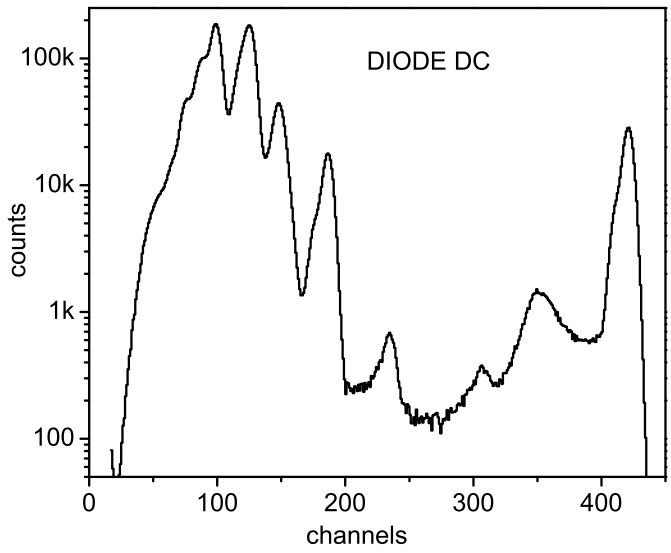

Figure B.1: ^{241}Am spectrum acquired with diode detector, CSA amplifier configuration, DC-coupled, peaking time 4.0 μs, V_{bias} = 50 V. The 60 keV peak has a standard deviation of 150 e^-. The vertical scale in set to log-scale, to enhance both the low activity peak of 33.2 keV and the events coming from Compton effect, between the two most energetic peaks of 33.2 keV and 59.5 keV.

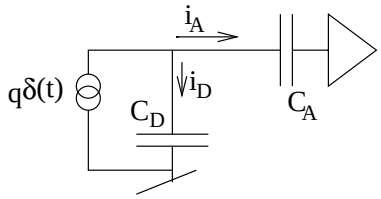

Figure B.2: Current divider made-up of C_{A} and C_{D} when we consider a finite value for C_{A}; the preamplifier is again considered as a zero resistance path. $i_A + i_D$ sum to $q\delta(t)$.

Strips are not used as spectroscopic detectors for X-rays [1], since very large area but ultra low-noise devices are already of common use.

One of this is, of course, the silicon drift chamber, invented in 1984 [43], exploiting a new concept: the electric field produced by the collecting anode is not the one responsible for the movement of charge inside the detector. Among the several advantage, it keeps the capacitance of the detector as small as the one of a pixel, while the sensing area may be designed macroscopic, whose noise contribution comes only from the leakage current. The two internal barrels of ALICE experiment, number 3 and 4, have this kind of detectors [2], making ALICE the first high energy physics experiment betting on this new technology. Some groups tried to use the ALICE Silicon Drift Detectors as spectrographic detectors with impressive results [44].

Moreover, in silicon strip detectors, usually the pitch is intentionally made small to share the charge released by an ionization event among as more strips as possible [45], in order to fit the impact position of the incoming particle.

The low capacitance 4 mm^2 diode, cut from an ALICE ITC wafer, is well suited for spectroscopy. The diode was the detector with which we calibrate the C_{test} on A250 board, since it is, among all, the less noisy device and does not suffer of effects such as charge sharing with neighboring electrodes (only the guard ring). As a result, the 60 keV peak is very clean and easy to fit, even if its FWHM is slightly greater than the one of the gaussian obtained injecting a charge pulsing the C_{test} with an external square wave.

Coupling the diode in DC to the gate of the 2SK152 JFET, the peak is found at channel # 419. Notice the shoulder at the left of the peak due to less energetic photoelectrons, produced by photons having knocked-on an electron in a preceding Compton scattering.

All strip modules show their peak below the 419$^{\mathrm{th}}$ channel. This is not due to charge sharing between nearby strips, indeed the shape of the peak is quite clean [2]; neither it is due to charge losses by recombination in the bulk. This is due to the fact that the strips are AC-coupled to the A250. The charge entering into the C_{f} is a fraction $\frac{C_{\mathrm{A}}}{C_{\mathrm{D}}+C_{\mathrm{A}}}$ of the DC coupled diode case, where C_{A} is the coupling capacitance and C_{D} the detector capacitance. The C_{A} values for the modules used are listed in table B.1 and vary depending on the supplier; they are $\sim$ 20 times

[1] Some important exceptions exist, however, in cases such as medical imaging with synchrotron radiation, in which strips are oriented to the beam in edge-on configuration, obtaining full absorption or X-rays in a direction parallel to the strips [41] [42].

[2] One could deduce that the path of the 60 keV photoelectron is less than 95 μm, pitch of ALICE strips.

C_A	p-side	n-side
CANBERRA	300	290
ITC	320	240
SINTEF	200	180

Table B.1: Measured coupling capacitance C_A of the different strip modules. Values in pF. Scan of the AC was one of the measurements aimed to decide the quality of a detector.

greater than the detector capacitance C_D, making the ratio $\frac{C_A}{C_A+C_D}$ in the range 95% - 97 % and justifying the peak displacement.
In chapter 3 we stated that signals and noise generated inside the detector see a "zero" resistance path to the amplifier, so both integrate on C_f.
C_A, however, is not infinite and must be compared with detector capacitance. Figure B.2 shows how the signal $q\delta(t)$ divides itself into two currents by a "current divider": i_A, through C_A, is equal to $q\delta(t)\frac{C_A}{C_A+C_D}$ and $i_D = q\delta(t)\frac{C_D}{C_A+C_D}$ through the detector capacitance and it does not contribute to the signal. The same holds for a fraction $\frac{C_D}{C_A+C_D}$ of the parallel noise, shorted to ground as well as the signal [3].
The assumption that the preamplifier itself is a $0\,\Omega$ path is taken as true.
The low energy shoulder at the left of 60 keV peak can be explained by a minor fraction of events, whose charge is shared between two strips.
All these spectra are acquired at the best peaking time for each detector, estimated by means of noise measurements of the kind of those described in chapter 4. In the better detectors, the S/N ratio for a m.i.p should be, with this set-up, greater than 100. In our situation, however, we do not have to cope with noise coupled from the other channel electronics or with a high rate of signal setting an upper limit to the peaking time, we can choose the optimum bias voltage and we can use a low-noise single channel amplifier, no matter its power dissipation.
Every of these things are not possible in ALICE, which performs however S/N as high as 75 [46].

About detector with SF read-out, spectra on PINs are influenced by the low value (3 MΩ) of the bias resistor integrated in the device; being the parallel noise so significant, the minimum available peaking time of $0.8\,\mu$s has been used. The gain is different from the CSA cases and different between them too, so the horizontal scale can be thought of as expressed in arbitrary units. Spectra B.9 is acquired connecting the output of the source follower directly to the PX4 shaper, avoiding the noise contribution from the CSA stage, but being more sensitive to the noise of PX4 itself.

[3] since the correction is small, throughout the chapters this consideration has not been taken into account

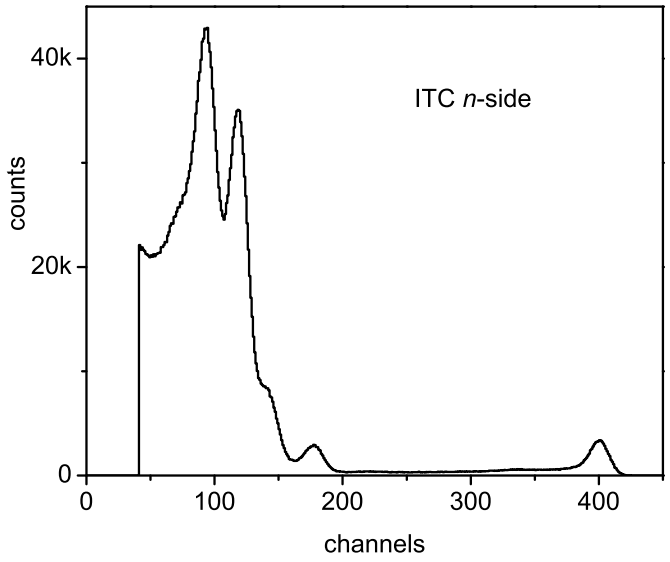

Figure B.3: Am spectrum acquired with detector AI, n-side, CSA amplifier configuration, peaking time 2.4 μs, $V_{bias} = 70$ V, ENC = 290 e^-, calculated from the standard deviation of 60 keV peak.

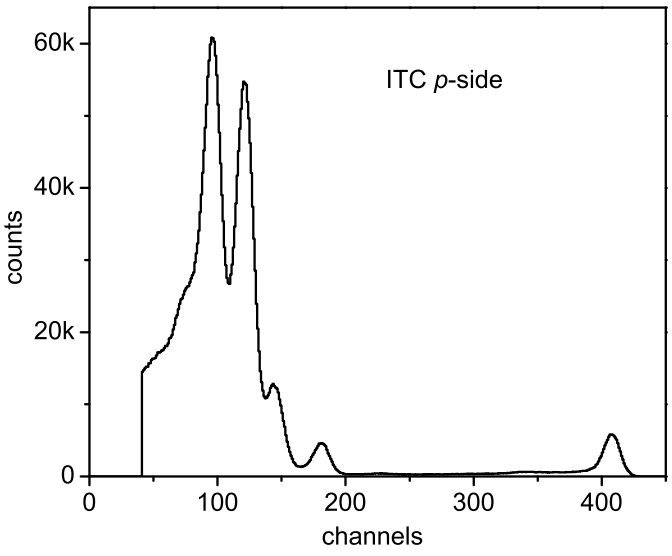

Figure B.4: Am spectrum acquired with detector AI, p-side, CSA amplifier configuration, peaking time 4.0 μs, $V_{bias} = 60$ V, ENC = 260 e^-.

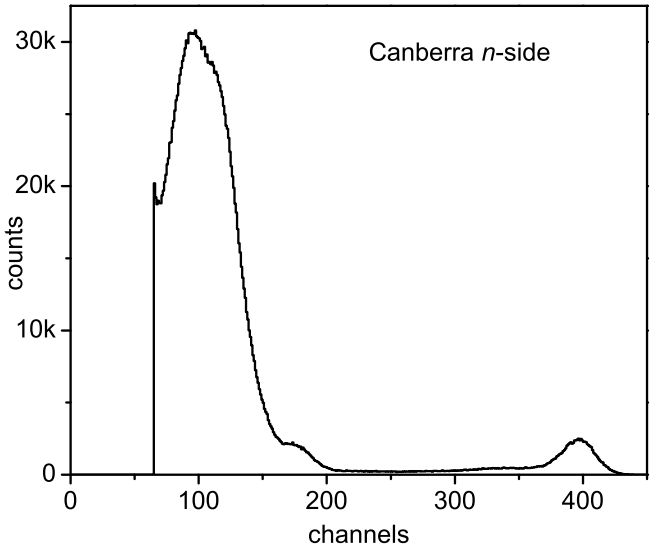

Figure B.5: Am spectrum acquired with detector AE, n-side, CSA amplifier configuration, peaking time 0.8 μs, $V_{bias} = 80$ V, ENC = 540 e^-.

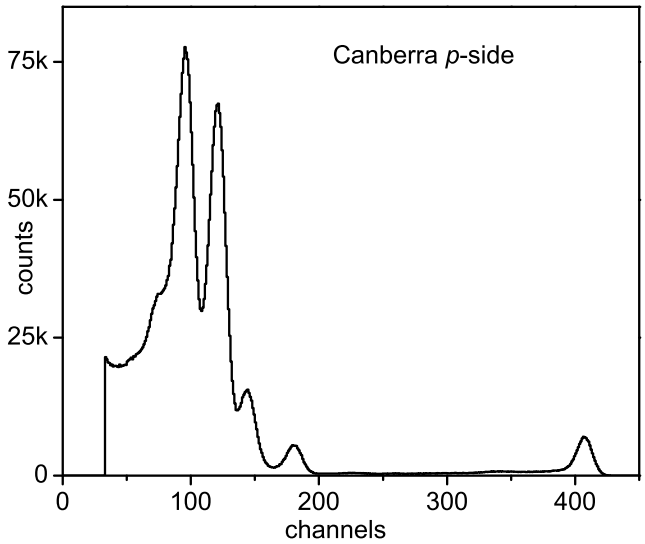

Figure B.6: Am spectrum acquired with detector AE, p-side, CSA amplifier configuration, peaking time 2.4 μs, $V_{bias} = 70$ V, ENC = 240 e^-.

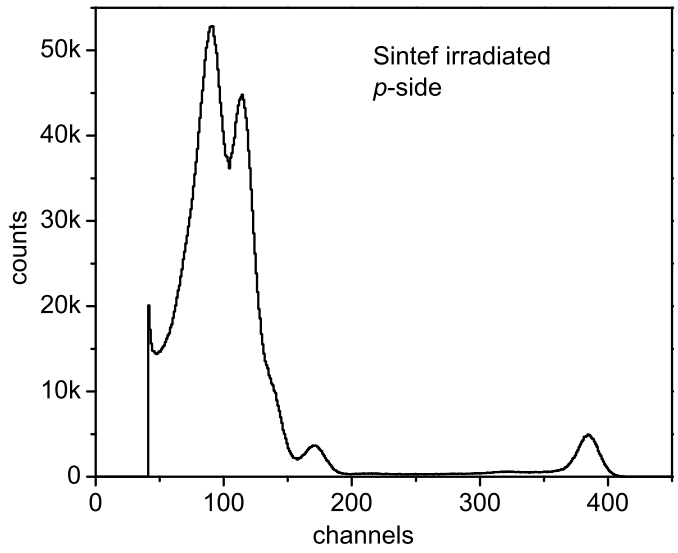

Figure B.7: Am spectrum acquired with detector AS2 (irradiated), p-side, CSA amplifier configuration, peaking time 0.8 μs, $V_{\mathrm{bias}} = 65$ V, $V_{BR_p} = -5$ V, ENC = 360 e^-.

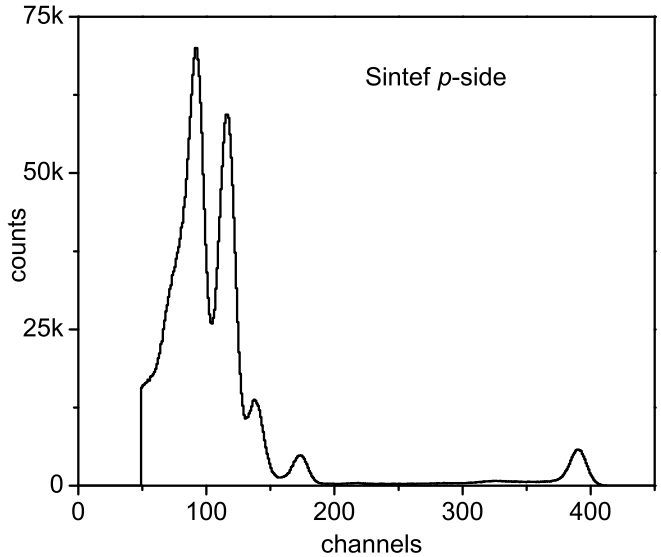

Figure B.8: Am spectrum acquired with detector AS1, p-side, CSA amplifier configuration, peaking time 2.4 μs, $V_{\mathrm{bias}} = 55$ V, $V_{BR_p} = -5$ V, ENC = 270 e^-.

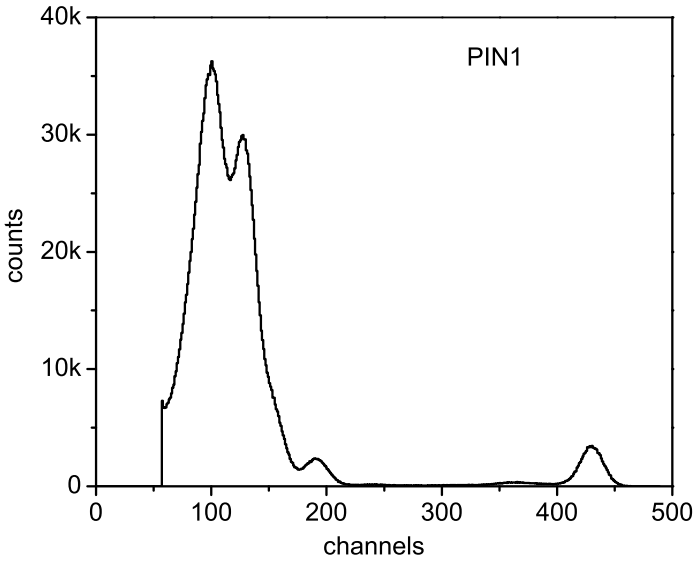

Figure B.9: Am spectrum acquired with detector PIN1 whose output was directly connected to PX4, without a coupling capacitance, SF configuration, peaking time = 0.8 μs, V_{bias} = 50 V, ENC = 380 e^-.

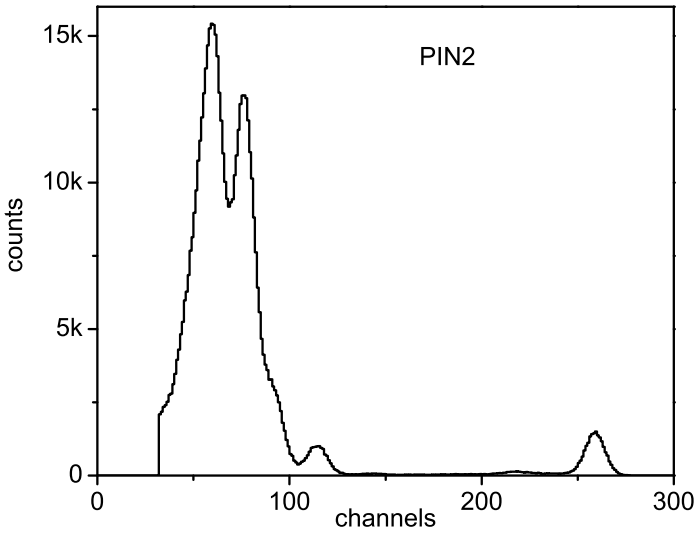

Figure B.10: Am spectrum acquired with detector PIN2, C_A= 67 pF, SF configuration, peaking time = 0.8 μs, V_{bias} = 50 V, ENC = 330 e^-.

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