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## Design of an LNA based on SiGe HBT Technology for the Beam Position Monitor of Particle Accelerators

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# Abstract

In the field of high-energy physics, the precise monitoring of particle beam position is crucial for the efficient operation and control of particle accelerators. This thesis focuses on the design and optimization of a Low-Noise Amplifier (LNA) in Silicon-Germanium Heterojunction Bipolar Transistor (SiGe HBT) technology for the Beam Position Monitor (BPM) system employed in the Proton Synchrotron (PS) particle accelerator at CERN. The objective of this research is to develop a high-performance LNA possibly exceeding the specifications of the operational one, designed more than 25 years ago. The initial stages of the thesis involve a comprehensive review of relevant literature, focusing on the principles of accelerator technology, beam position monitor, and the fundamentals of Low-Noise Amplifier design. Building upon this foundation, the SiGe HBT technology is explored for its suitability in the demanding environment of a particle accelerator, considering factors such as noise performance, linearity and operating frequency range. The design methodology encompasses various stages, including device modeling, circuit simulation, layout implementation, PCB production and laboratory tests. Utilizing industry-standard simulation tools, such as LTspice and AWR Microwave Office, the LNA circuit is optimized for minimum noise figure, maximum gain, and optimal impedance matching. Additionally, filtering and feedback techniques are employed to improve the overall performance of the amplifier. The outcomes of this research could contribute to the advancement of accelerator technology, specifically in the domain of beam position monitoring. The aim for the developed LNA design is to improve sensitivity and dynamic range of the CERN PS BPM system and, possibly, improve the control and exploitation of the particle accelerator.





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# Introduction

Chapter 1 provides a comprehensive and detailed overview of the particle accelerator complex at CERN, with a particular focus on the PS ring, which is of utmost importance in the present thesis project. The main objective of this chapter is to explore the operational aspects of the Beam Position Monitors (BPM) installed in each accelerator and their role in accurately monitoring the particle beams. Finally, attention is drawn to the Low-Noise Amplifier (LNA) and the fundamental role it plays in the analog front-end of the BPM.

## 1.1 CERN Accelerator Complex

The CERN, European Organization for Nuclear Research, was founded in 1954 and is universally recognized as one of the most prestigious and influential scientific institutions in the world. As an international organization, CERN is dedicated to scientific research in the field of high-energy physics (HEP), and its primary mission is focused on studying the fundamental structure of the universe. Through the exploration of elementary particles and the forces that govern them, main objective of CERN is to deepen our understanding of the nature and origin of the cosmos. At the heart of CERN groundbreaking research activities lies a complex of particle accelerators and detectors. CERN particle accelerators can be distinguished into several categories, each characterized by its own design and specific purpose. Firstly, we have linear accelerators (LINAC), which enable rapid acceleration of particles along a straight path using Radio-Frequency (RF) fields. LINACs find wide applications in medical facilities for cancer treatment, as well as in the industrial sector. Another type of accelerator is the synchrotrons that use powerful magnetic fields to guide particles along a circular path, gradually increasing their speed. These accelerators have diverse purposes, such as conducting high-energy physics experiments, materials research, and supporting medical applications. Finally, colliders represent

another category of particle accelerators. These devices bring together two beams of particles, causing them to collide at specific interaction points. Analyzing the sub-atomic interactions that occur during these high-energy collisions allows scientists to investigate the fundamental nature of matter. A notable example of a collider is the famous Large Hadron Collider (LHC).

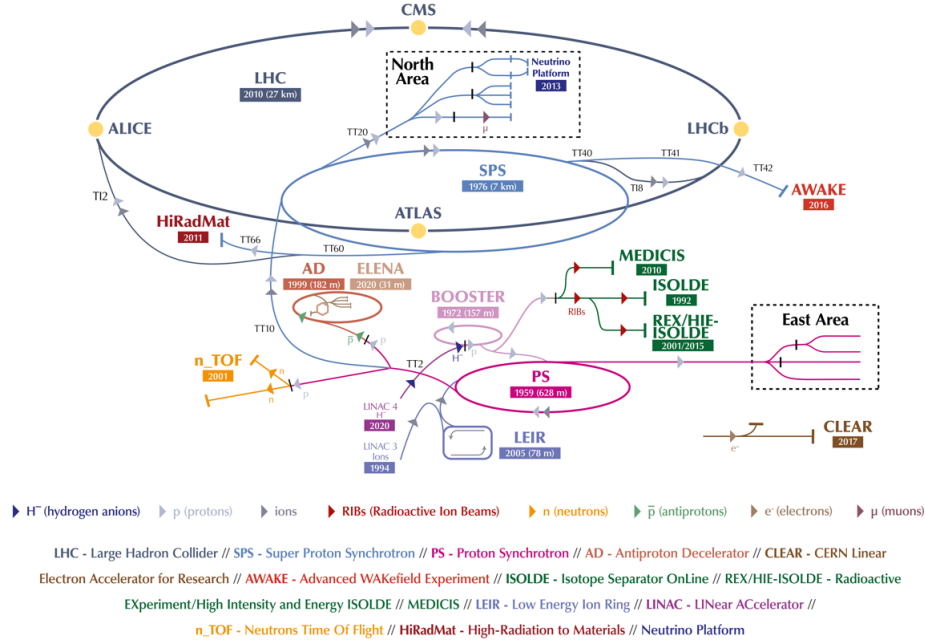


Figure 1: CERN Accelerator Complex

The Figure 1 illustrates the succession of particle accelerators at CERN [1]. As reported in [2], the process of accelerating protons begins with the Linear Accelerator 4 (LINAC4), which plays a fundamental role in generating and accelerating proton beams. Initially, negative hydrogen ions ( $H^-$ ) are accelerated to 160 MeV. Subsequently, after stripping two electrons from the  $H^-$  ions, the beam of ions is sent to the Proton Synchrotron Booster (PSB), where their energy is further amplified to 2 GeV. After this stage, the protons are sent to the Proton Synchrotron (PS) and then to the Super Proton Synchrotron (SPS), where their energy is further increased to 26 GeV and 450 GeV, respectively. Once the path through the SPS is completed, the proton beam is introduced into the massive Large Hadron Collider (LHC). The

LHC consists of two circular rings where the protons travel in opposite directions. Through this ring, the protons reach their maximum energy of 6.5 TeV before being made to collide at the center of the four main detectors: ALICE, ATLAS, CMS, and LHCb. The collisions of proton beams in these detectors, which generate a combined energy of 13 TeV, allow scientists to study the produced particles and deepen our understanding of particle physics and fundamental interactions. Parallel to this proton pathway, heavy ions can also be accelerated and brought to collision.

## 1.2 The Proton Synchrotron

This thesis will focus on the Proton Synchrotron (PS) particle accelerator, a remarkable research tool in the field of high-energy physics. The PS achieved a ground-breaking moment on 24 November 1959, when it accelerated protons for the first time, temporarily becoming the particle accelerator with the highest energy in the world [3]. Originally conceived as CERN first synchrotron, the PS represents a fundamental milestone in the development of particle physics. Despite CERN investments in new accelerators during the '70s, the PS continued to adapt to research needs, significantly increasing the intensity of the proton beam, now a thousand times higher than in its early days. Impressive from an engineering perspective, the PS has a circumference of 628 meters and is equipped with a complex system of 277 conventional electromagnets at room temperature. Among them are 100 dipole magnets, which bend the proton beams around the ring to maintain a circular trajectory. In addition to accelerating protons, the PS has demonstrated its versatility by accelerating a wide range of particles, including helium nuclei, oxygen, sulfur, argon, and lead nuclei, electrons, positrons and antiprotons. This flexibility has allowed it to contribute to numerous studies and discoveries in the field of particle physics and the structure of matter.

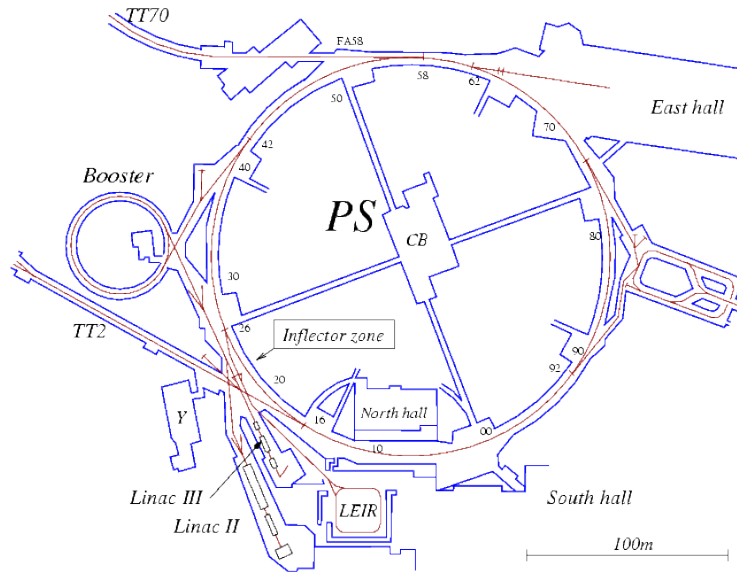


Figure 2: Proton Synchrotron Straight Section - CERN <sup>1</sup>

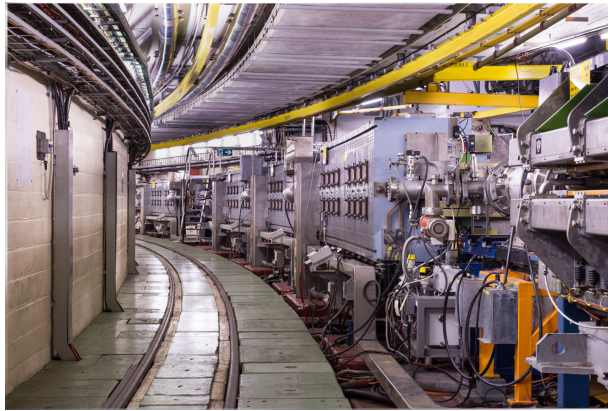


Figure 3: The Proton Synchrotron - CERN [3]

<sup>1</sup><http://psring.web.cern.ch/psring/pscomplex.html>

### 1.3 Beam Position Monitoring

Beam position monitoring plays a fundamental role in the proper functioning of particle accelerators. In fact, precise measurement and careful control of the beam position inside the accelerator are essential aspects to achieve the desired experimental results and ensure a safe and efficient operation of the entire system. Particle accelerators are designed with the primary goal of accelerating charged particles to high energy and causing them to collide with target materials or other particles. Accuracy and control of these collisions are critical, and for this reason it is important to maintain the stability of the particle beam. To this end, real-time monitoring of beam position offers valuable information that allows operators to identify and correct any deviations from the desired trajectory. Accurate beam position monitoring is equally important for beam losses detection. These leaks occur when particles deviate from their intended path and collide with accelerator components. The effects of beam losses can be diverse, including localized heating, radiation damage, and potentially hazardous situations. In this context, it is vital that operators can swiftly identify any abnormal beam behavior and take appropriate measures to mitigate or prevent such losses. Additionally, the accurate monitoring of the beam position is essential in particle physics research. In fact, precise knowledge of the beam position allows researchers to correlate recorded signals with specific beam conditions. This aspect becomes particularly important in the context of elementary particle research, where even small variations in position can have a significant impact on analyses and scientific discoveries.

For linear accelerators and transfer lines, BPMs (Beam Position Monitors) are essential for measuring and correcting beam trajectories. In circular accelerators, BPMs are not only used for measuring and correcting trajectories but also for calculating the closed orbit, which is the averaged trajectory over multiple revolutions, making them even more crucial. In the early stages of BPM development, monitoring systems were relatively simple, mainly consisting of an oscilloscope directly connected to the detection signals. Over time, significant advancements in acquisition and processing electronics have greatly improved modern BPMs. Today, they can accurately digitize signals with high precision and resolution, enabling the detection of signal groups separated by just a few nanoseconds. These technological improvements have resulted in significant practical benefits, allowing for rapid visualization and analysis of beam trajectories in a fraction of a second.

A general block diagram of a typical beam position monitor is illustrated in Figure 4. Here, four detector electrodes are symmetrically arranged along the horizontal and vertical axes of the beam pipe. The electrodes interact electromagnetically with the charged particles in the beam pipe, and each of them returns a pulsed signal proportional to the intensity of the beam packets and the distance between the beam and the electrode, i.e., the beam position. All four electrode signals are routed to the analog front-end electronics, which comprise a variety of signal processing elements, such as analog filters, low-noise amplifiers, mixers, and subsequently digitized through an analog-to-digital converter (ADC). Finally, the digitized position data is collected by a data acquisition (DAQ) system [4].

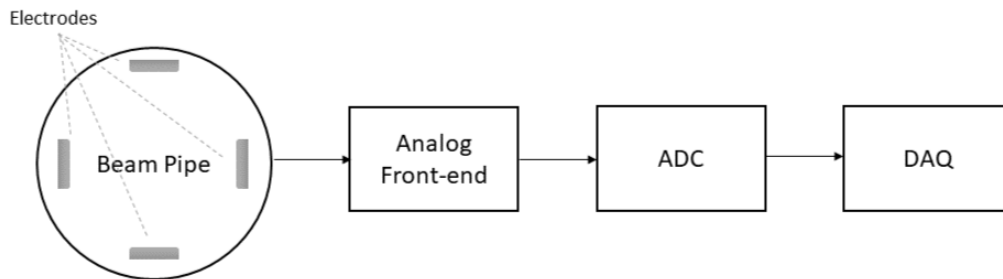


Figure 4: General Block Diagram of a BPM System

### 1.3.1 Technique for Beam Position Detection

The accurate determination of the beam position hinges upon the analysis of data collected from pick-up electrodes situated within the beam pipe. Through the digitization of electrode signals, the BPM system performs calculations to derive both horizontal and vertical beam coordinates. The sensing elements commonly used within circular accelerators are electrostatic or capacitive pick-ups that consist of metallic plates or grids arranged in a specific configuration [5]. When the beam passes through the pick-up, it induces an electric charge on the electrodes, resulting in the generation of an image current  $I_{im}(t)$  that directly relates to the intensity of the beam current  $I_{beam}(t)$ , but with reversed polarity, as shown in Figure 5 and in equations (1) and (2).



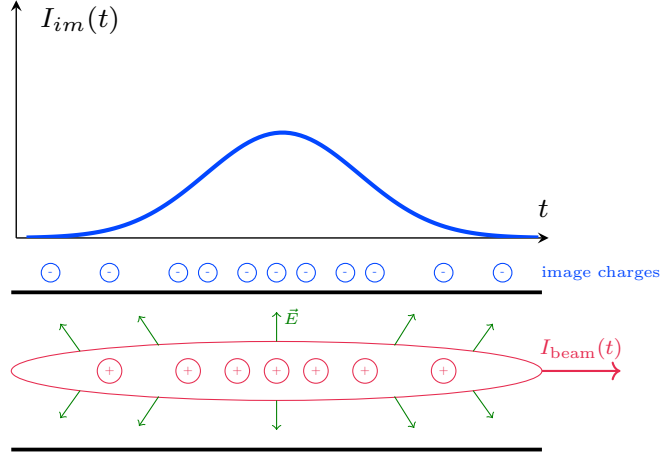


Figure 5: Electromagnetic Interaction between the beam and an electrode [4]

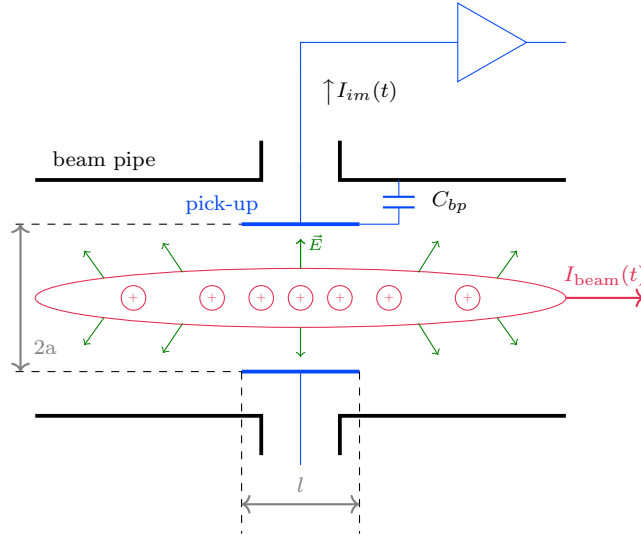


Figure 6: BPM Schematic for the vertical position

Furthermore, the image current  $I_{im}(t)$  exhibits an inverse relationship with the distance  $a$  between the beam and the plate, characterized by its length  $l$  and area  $A$ . Consequently, by accurately measuring the difference in induced charge on the four electrodes, it becomes possible to calculate the precise position of the beam.

As reported in [4], the image current  $I_{im}(t)$  driven by the image charge  $Q_{im}(t)$  is:

$$I_{im}(t) = \frac{dQ_{im}(t)}{dt} = -\frac{A}{2\pi al} \frac{dQ_{beam}(t)}{dt} \quad (1)$$

The electrical current  $I_{beam}(t)$  is formed by  $N$  particles of charge state  $q$  per unit of time  $t$ :

$$I_{beam}(t) = \frac{qeN}{t} = \frac{qeNv}{l} \quad (2)$$

where  $e$  is the elementary charge and  $v$  is beam velocity.

To simplify, let us focus only on the plates that detect the transverse displacement of the beam. It is evident that when the beam is not centered, there will be a greater charge accumulation on the plate closest to it. This phenomenon is commonly known as the “proximity effect”, and it is depicted in Figure 7. Consequently, the amplitudes of the voltage pulses captured by the two opposing electrodes will exhibit a discrepancy, allowing for the measurement of the vertical displacement ( $y$ ) of the beam.

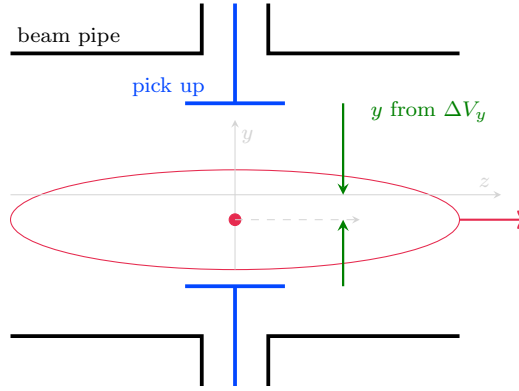


Figure 7: Proximity Effect for the BPM vertical plates

$$y = \frac{1}{S_y} \cdot \frac{V_{up} - V_{down}}{V_{up} + V_{down}} = \frac{1}{S_y} \cdot \frac{\Delta V_y}{\Sigma V_y} \quad (3)$$

where  $V_{up}$  and  $V_{down}$  are the voltage pulses measured on the upper and lower plate respectively, while  $S_y$  is the position sensitivity (for a more in-depth understanding of this sensitivity, reference can be made to Ref. [6]).

Similarly, for the longitudinal displacement ( $x$ ), we have:

$$x = \frac{1}{S_x} \cdot \frac{V_{right} - V_{left}}{V_{right} + V_{left}} = \frac{1}{S_x} \cdot \frac{\Delta V_x}{\Sigma V_x} \quad (4)$$

The capacitive pick-up is defined by its capacitance, denoted as  $C$ , which comprises three components: the capacitance  $C_{bp}$ , which represents the capacitance between the plate and the beam pipe, the capacitance between the plates, and the capacitance contributed by the cable connecting the plate to the amplifier with input resistance  $R$  [6]. From this consideration, the pick-up electrode can be schematized through the equivalent circuit shown in Figure 8.

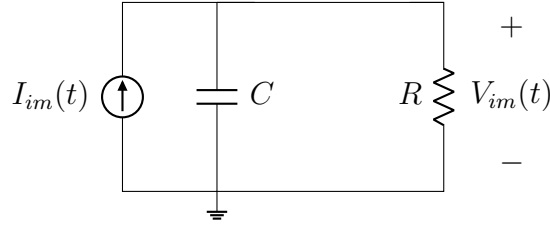


Figure 8: Equivalent Circuit of a Pick-up Electrode

Considering the parallel connection it is possible to write the impedance  $Z$  as:

$$Z = \frac{R}{1 + j\omega CR} \quad (5)$$

The voltage drop across  $Z$  in the frequency domain is:

$$V_{im}(j\omega) = Z \cdot I_{im}(j\omega) = \frac{R}{1 + j\omega CR} \cdot I_{im}(j\omega) \quad (6)$$

Considering that the Fourier Transform of  $\frac{d}{dt}$  is  $-j\omega$ :

$$V_{im}(j\omega) = \frac{R}{1 + j\omega CR} \cdot \frac{j\omega A}{2\pi al} \cdot I_{beam}(j\omega) = Z_t(j\omega) \cdot I_{beam}(j\omega) \quad (7)$$

Therefore the Transfer Function of the pick-up is:

$$Z_t(j\omega) = \frac{V_{im}(j\omega)}{I_{beam}(j\omega)} = \frac{R}{1 + j\omega RC} \cdot \frac{j\omega A}{2\pi al} \quad (8)$$

This function is characterized by a zero in the origin and a pole at a frequency  $f_p = (2\pi RC)^{-1}$ , which depends on the input resistance of the amplifier. Indeed, as this input resistance increases, the pole frequency decreases, allowing for precise control over the frequency range in which the system must operate. The Figure 9 shows the Bode Diagram of this transfer function in three particular cases of amplifier input impedance: high impedance, low impedance, transformed impedance.

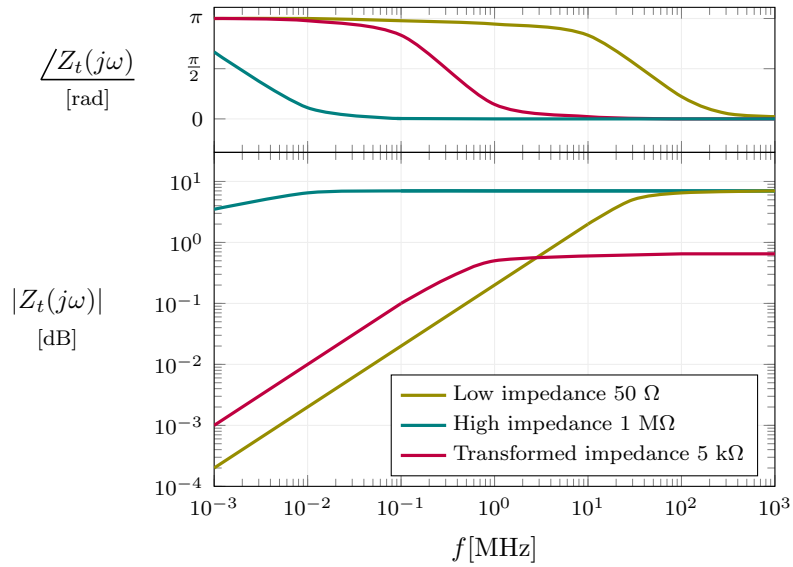


Figure 9: Bode Diagram of Transfer Function  $Z_t(j\omega)$  [6]

## 1.4 The role of Low-Noise Amplifier

The Low-Noise Amplifier (LNA) is a fundamental component in numerous electronic systems, particularly those involved in communication and signal processing, such as receivers and wireless communication systems. Even in the context of BPM (Beam Position Monitor), the LNA plays a significant role as the initial stage in the analog front-end of the BPM. Its function is to amplify weak electrical signals generated by the BPM pick-up while minimizing the addition of noise.

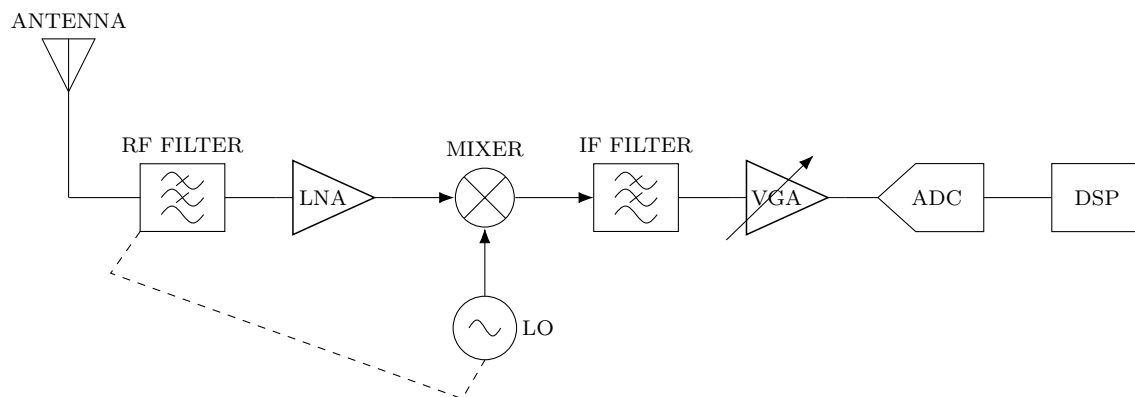


Figure 10: Block Diagram of a Typical Receiver System

The Low-Noise Amplifier currently employed in the BPM analog front-end of the PS particle accelerator at CERN was designed and implemented about 25 years ago. Despite its remarkable performance demonstrated over the years, the associated electronics are approaching the end of their lifecycle, with some components becoming obsolete. Therefore, the main objective of this research thesis is to design a new LNA using newer technology without compromising the excellent performance of the current system. This new amplifier is proposed as a viable alternative to the model currently in use.

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# Fundamentals of LNA

Chapter 2 provides a comprehensive introduction to the fundamental aspects of Low-Noise Amplifiers, providing readers with a strong foundation for understanding the principles and considerations involved in SiGe HBT LNA design. This chapter covers essential topics, including the principles of LNA operation, key parameters, and noise analysis.

## 2.1 The Principles of LNA Operation

Low-Noise Amplifiers play a fundamental role in contexts where both signal amplification and low noise are of crucial importance. Within electronic systems, noise is an intrinsic phenomenon that can compromise signal quality and hinder the accurate detection or processing of weak signals. For this reason, the primary purpose of Low-Noise Amplifiers (LNAs) is to amplify weak input signals without introducing significant levels of additional noise. This results in a substantial improvement in the overall signal-to-noise ratio (SNR), system sensitivity, and maximizes overall performance. To achieve optimal performance, a solid understanding of their fundamental principles of operation, along with the use of highly efficient technologies and components, is crucial. These principles encompass various key aspects, including gain, noise figure, input and output matching, stability and linearity. In the following paragraphs, we will delve into each of these aspects in detail, exploring their significance and impact on LNA performance. One way to simplify the analysis and study of LNAs is by representing them as quadripoles. In general a linear time invariant N-port network can be represented by a scattering parameter matrix or S-parameter matrix [7]. This matrix describes the relationship between the incident and reflected or transmitted waves at the input and output ports of the quadripole, providing valuable insights into the behavior of the network and allows for a comprehensive understanding of its performance characteristics.

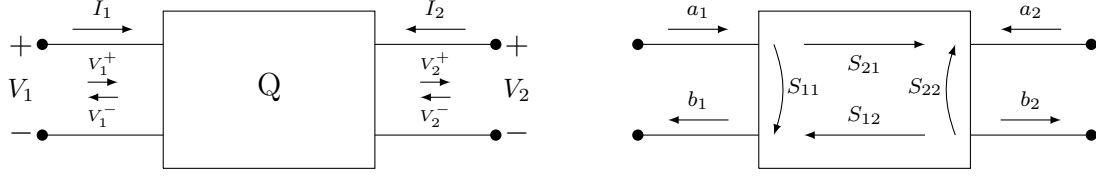


Figure 11: LNA as Two-Port Network

Taking into account the Telegrapher's equations, which describe the propagation of voltage and current phasors along a transmission line:

$$\begin{cases} V(l) = V^+ e^{j\beta l} + V^- e^{-j\beta l} \\ I(l) = \frac{V^+}{Z_0} e^{j\beta l} - \frac{V^-}{Z_0} e^{-j\beta l} \end{cases} \quad (9)$$

Where:

- $V^+$  is the phasor of the incident wave;
- $V^-$  is the phasor of the reflected wave;
- $Z_0$  is characteristic impedance of the transmission line;
- $l$  is the length of the transmission line;
- $\beta = \frac{2\pi}{\lambda}$  is the phase constant;
- $\lambda = \frac{v_f}{f_0}$  is signal wavelength;
- $v_f = \frac{c}{\sqrt{\epsilon_r}}$  is propagation speed along the transmission line.

It is possible to write:

$$\begin{cases} V_1 = V_1^+ + V_1^- \\ I_1 = \frac{V_1^+}{Z_0} - \frac{V_1^-}{Z_0} \end{cases} \quad (10)$$

$$\begin{cases} V_2 = V_2^+ + V_2^- \\ I_2 = \frac{V_2^+}{Z_0} - \frac{V_2^-}{Z_0} \end{cases} \quad (11)$$

The S-parameter matrix for a two-port network can be expressed as follows:

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \quad (12)$$

$a_1$  and  $a_2$  represent the incident waves at the input port,  $b_1$  and  $b_2$  represent the reflected and transmitted waves at the output port, respectively [8].

$$\begin{aligned} a_1 &= \frac{V_1 + Z_0 I_1}{2\sqrt{Z_0}} = \frac{V_1^+}{\sqrt{Z_0}} & a_2 &= \frac{V_2 + Z_0 I_2}{2\sqrt{Z_0}} = \frac{V_2^+}{\sqrt{Z_0}} \\ b_1 &= \frac{V_1 - Z_0 I_1}{2\sqrt{Z_0}} = \frac{V_1^-}{\sqrt{Z_0}} & b_2 &= \frac{V_2 - Z_0 I_2}{2\sqrt{Z_0}} = \frac{V_2^-}{\sqrt{Z_0}} \end{aligned}$$

$S_{11}$ ,  $S_{12}$ ,  $S_{21}$  and  $S_{22}$  are complex numbers that characterize the network behavior:

- $S_{11}$  is known as the input reflection coefficient or input return loss;
- $S_{12}$  is known as the reverse gain or the isolation of the two-port;
- $S_{21}$  is known as the transducer power gain of the two-port;
- $S_{22}$  is known as the output reflection coefficient or output return loss.



$$S_{11} = \left. \frac{b_1}{a_1} \right|_{a_2=0} \quad S_{12} = \left. \frac{b_1}{a_2} \right|_{a_1=0} \quad S_{21} = \left. \frac{b_2}{a_1} \right|_{a_2=0} \quad S_{22} = \left. \frac{b_2}{a_2} \right|_{a_1=0}$$

When designing a Low-Noise Amplifier as a two-port network, the S-parameters are typically optimized to achieve specific characteristics. To ensure efficient power transfer, the LNA is designed to have low values of  $S_{11}$  and  $S_{22}$ , indicating good matching between the input and output ports. This matching minimizes the reflection of input power, allowing most of it to be absorbed by the LNA rather than being reflected back. In addition to good input/output matching, the LNA is engineered to have a high value of  $S_{21}$ , representing a substantial power gain or amplification of the input signal. This high gain enables to boost weak signals to a level suitable for further processing or transmission. Overall, the goal of designing an LNA as a two-port network is to achieve good input/output matching, high gain, and low noise figure.

### 2.1.1 Gain

In the context of Radio-Frequency (RF), various types of power gains are defined, providing a comprehensive view of the amplification characteristics of a system and enabling accurate performance evaluation and optimal design. These types of gains include Operational Power Gain ( $G_P$ ), Available Power Gain ( $G_A$ ), and Transducer Gain ( $G_T$ ) [9].

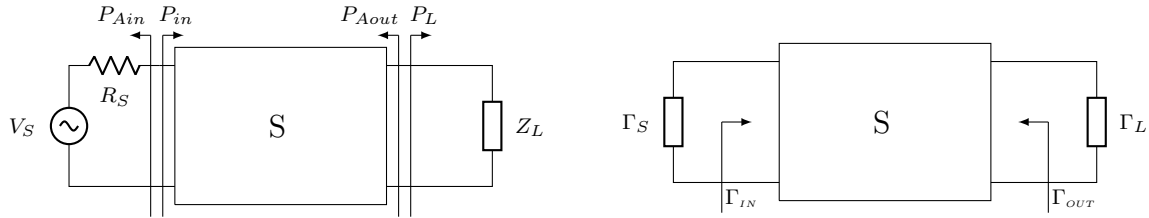


Figure 12: Two-Port Network with Power and Reflection Coefficients

*Operational Power Gain* represents the ratio between the average power delivered to the load ( $P_L$ ) and the input power to the two-port network ( $P_{in}$ ):

$$G_P = \frac{P_L}{P_{in}} \quad (13)$$

This gain directly measures signal amplification, that is, by how much a device increases the input signal power. It is essential for evaluating the effectiveness of amplification and comparing its performance.

*Available Power Gain*, on the other hand, is defined as the ratio between the available power at the output of the two-port network ( $P_{Aout}$ ) and the available power from the signal generator ( $P_{Ain}$ ). The available power is the power that a generator can supply to a matched load: the condition for conjugate matching is  $Z_L = Z_S^*$ .

$$G_A = \frac{P_{Aout}}{P_{Ain}} \quad (14)$$

This type of gain represents the increase obtainable under perfectly matched conditions at both input and output, considering lossless matching networks.

Lastly, *Transducer Gain* is defined as the ratio between the average power delivered to the load ( $P_L$ ) and the available power from the signal generator ( $P_{Ain}$ ):

$$G_T = \frac{P_L}{P_{Ain}} \quad (15)$$

This parameter represents the gain obtainable if conjugate matching occurred at the input. In general, the  $G_T$  gain is less than both  $G_A$  and  $G_P$ . However, in the presence of a conjugate matching at the input,  $G_T$  equals  $G_P$ , while with a conjugate matching at the output,  $G_T$  equals  $G_A$ . Consequently, in situations where there is a conjugate matching at both the input and output,  $G_T = G_P = G_A$  occurs.

Considering the circuit in Figure 12, it is possible to obtain the reflection coefficients at the input and output of the quadripole:

$$\Gamma_{IN} = \frac{Z_{IN} - Z_0}{Z_{IN} + Z_0} \quad (16)$$

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} \quad (17)$$

In particular, considering the system (12), it is possible to know the input and output reflection coefficient in terms of S-parameters:

$$\Gamma_{IN} = \frac{b_1}{a_1} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \quad (18)$$

$$\Gamma_{OUT} = \frac{b_2}{a_2} = S_{22} + \frac{S_{21}S_{12}\Gamma_S}{1 - S_{11}\Gamma_S} \quad (19)$$

In this way, for each gain, it is possible to provide a definition as a function of S-parameters and reflection coefficients:

$$G_P = \frac{|S_{21}|^2 (1 - |\Gamma_L|^2)}{(1 - |\Gamma_{IN}|^2)|1 - S_{22}\Gamma_L|^2} \quad (20)$$

$$G_A = \frac{|S_{21}|^2 (1 - |\Gamma_S|^2)}{|1 - S_{11}\Gamma_S|^2 (1 - |\Gamma_{OUT}|^2)} \quad (21)$$

$$G_T = \frac{|S_{21}|^2 (1 - |\Gamma_L|^2) (1 - |\Gamma_S|^2)}{|1 - S_{22}\Gamma_L|^2 |1 - \Gamma_{IN}\Gamma_S|^2} = \frac{|S_{21}|^2 (1 - |\Gamma_L|^2) (1 - |\Gamma_S|^2)}{|1 - S_{11}\Gamma_S|^2 |1 - \Gamma_{OUT}\Gamma_L|^2} \quad (22)$$

### 2.1.2 Noise Figure

The generation of electrical noise within a circuit plays a pivotal role in shaping its performance as it sets a minimum threshold for the signal level that the system can detect. When assessing the noise characteristics of a Low-Noise Amplifier, a widely employed metric is the noise factor represented by  $F$ . This metric provides information about the degradation of the signal-to-noise ratio between the input and output of the two-port network:

$$F = \frac{SNR_{IN}}{SNR_{OUT}} = \frac{\frac{S_{IN}}{N_{IN}}}{\frac{S_{OUT}}{N_{OUT}}} \quad (23)$$

In many cases, it is convenient to utilize the logarithmic scale in decibels (dB). The noise figure parameter, denoted by  $NF$ , is defined as:

$$NF = 10 \log(F) \quad (24)$$

To fully characterize a noisy amplifier, an effective approach is to use a noiseless network with the addition of two separate equivalent input noise generators: an equivalent voltage noise generator ( $e_n$ ) and an equivalent current noise generator ( $i_n$ ).

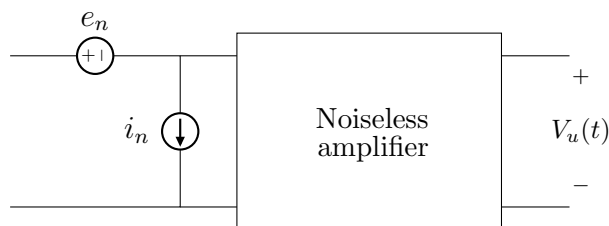


Figure 13: Noise Characterization of an Amplifier

Ideally,  $e_n$  is obtained by a procedure of shorting the input terminals of the amplifier and measuring the RMS value of the output noise voltage  $V_{nOUT}$ , considering the voltage gain  $A_v$  to be known. In parallel,  $i_n$  is obtained by keeping the input terminals of the amplifier open and measuring the RMS value of the output noise voltage, considering the voltage gain  $A_v$  and the input resistance  $R_{in}$  of the amplifier to be known:

$$e_n = \frac{V_{nOUT}}{A_v} \quad i_n = \frac{V_{nOUT}}{A_v R_{in}}$$

They are stochastic processes and can be described by the associated Power Spectral Density (PSD):

$$S_{e_n} \left[ \frac{\text{V}^2}{\text{Hz}} \right] \quad S_{i_n} \left[ \frac{\text{A}^2}{\text{Hz}} \right]$$

Considering the configuration shown in Figure 14, the total output noise is influenced by both the internal noise sources ( $e_n$  and  $i_n$ ) and the effect of thermal noise  $e_t$  of the signal generator impedance.

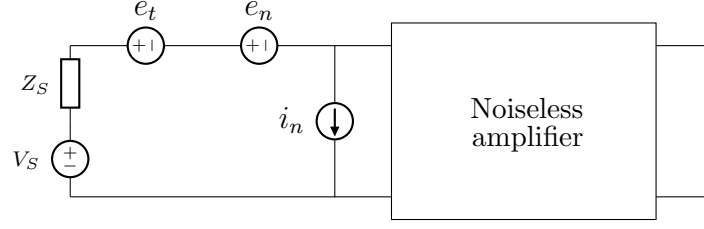


Figure 14: Internal Noise Sources and Thermal Noise

The stochastic processes  $e_n$  and  $i_n$  are correlated with each other and, in general, this correlation tends to increase with increasing frequency. However, for most cases of practical interest, it is possible to approximate the two generators as uncorrelated processes. Consequently, the power spectral density of the resulting process can be obtained simply by summing the power spectral densities of the individual contributions. This consideration leads us to derive the expression (27) for the noise figure.

The noise power output due to thermal noise of the source termination is:

$$N_{OUT_{e_t}} = KT\Delta f G_T \quad (25)$$

The total noise power output is:

$$N_{OUT_Q} = \frac{S_{e_n} + S_{i_n}|Z_S|^2}{4R_S} \Delta f G_T \quad (26)$$

Hence, considering that the noise figure can also be defined as the ratio between the total output noise power and the output noise power due to the thermal noise of the source termination, we obtain:

$$NF = \frac{N_{OUT_{e_t}} + N_{OUT_{e_n, i_n}}}{N_{OUT_{e_t}}} = 1 + \frac{N_{OUT_Q}}{N_{OUT_{e_t}}} = 1 + \frac{S_{e_n} + S_{i_n}|Z_S|^2}{4KTR_S} \quad (27)$$

From this equation we can observe that the noise figure is affected by various factors, including the power spectral densities  $S_{e_n}$  and  $S_{i_n}$  and the impedance  $Z_S$  of the signal generator. When aiming to design an amplifier with low noise, the initial crucial step involves carefully selecting the suitable active device. Once the active device

is chosen, the primary focus is on determining the optimal termination  $Z_{S_{opt}}$ , which helps minimize the noise figure. In simpler terms, achieving a Low-Noise Amplifier involves finding the best possible match between the impedance of the signal source and the input impedance of the amplifier. It is important to note that the minimum value of NF will undoubtedly be achieved when  $X_S = 0$ , so under the assumption that  $Z_S$  is real.

$$\frac{d(NF)}{dR_S} = \frac{2R_S S_{i_n} 4KT R_S - (S_{e_n} + R_S^2 S_{i_n}) 4KT}{(4KT R_S)^2} = 0 \quad (28)$$

For a given amplifier, the source resistance value at which the noise figure reaches its minimum is:

$$R_{S_{opt}} = \sqrt{\frac{S_{e_n}}{S_{i_n}}} \quad (29)$$

Because  $Z_S$  is typically determined by project specifications, it becomes crucial to integrate impedance transformation networks between the source and the amplifier input. This ensures that the amplifier perceives an impedance that is optimal in terms of noise considerations. By employing the Friis Formula, the impact of all noise characteristics can be assessed, allowing for the calculation of the overall noise figure for a network consisting of the cascade of two or more quadripoles.

$$NF_{tot} = NF_1 + \frac{NF_2 - 1}{G_{A_1}} + \dots + \frac{NF_n - 1}{G_{A_1} G_{A_2} \dots G_{A_{n-1}}} = NF_1 + \sum_{k=2}^n \frac{NF_k - 1}{\prod_{i=1}^{k-1} G_{A_i}} \quad (30)$$

The total noise figure ( $NF_{tot}$ ) is computed as the weighted sum of the noise figures of the individual quadripoles, with the weights determined by the gains of the preceding quadripoles. Consequently, the value of the overall noise figure is predominantly influenced by the characteristics of the first stage. Thus, in order to minimize the total noise figure of the system, it is crucial to ensure that the first stage possesses the lowest noise figure and the highest achievable gain. The LNA typically positioned as the initial stage in a signal receiver, holds significant importance in this context.

Its design, characterized by high gain and a low noise figure, is crucial for optimal system performance.

### 2.1.3 Bandwidth

The bandwidth of a Low-Noise Amplifier refers to the range of frequencies over which it effectively amplifies the input signal while maintaining desirable performance characteristics. To calculate the bandwidth of an LNA, we can use the following formula:

$$BW = f_{\text{high}} - f_{\text{low}} \quad (31)$$

where  $f_{\text{high}}$  represents the upper frequency limit, and  $f_{\text{low}}$  represents the lower frequency limit. Typically, the upper frequency limit is determined by the gain roll-off characteristics of the amplifier. As the frequency increases beyond this limit, the gain of the amplifier starts to decrease. This roll-off is often specified as the frequency where the gain drops by 3 dB, known as the -3 dB cutoff frequency. On the other hand, the lower frequency limit is influenced mainly by the input and output coupling capacitors. These capacitors form a high-pass filter that attenuates low-frequency signals. The -3 dB point of this high-pass filter corresponds to the lower frequency limit of the LNA bandwidth. When designing an LNA, it is crucial to consider several factors to achieve the desired bandwidth. Proper impedance matching at the input and output of the LNA, the choice of active devices, and the internal capacitances of transistors and interconnects all contribute to the overall high-pass filter response and affect the lower frequency limit. By optimizing these factors, the LNA bandwidth can be maximized, enabling effective amplification of signals across a wide frequency range.

### 2.1.4 Stability

The stability of a Low-Noise Amplifier is a crucial aspect of its design, as it pertains to the amplifier ability to maintain its intended characteristics without experiencing oscillations or instabilities. An unstable LNA can lead to signal distortion, oscillations, decreased gain, and even damage to the amplifier itself. Thus, ensuring stability is an essential step in the design and development process. Among the dif-

ferent forms of stability, unconditional stability emerges as a fundamental concept. Unconditional stability refers to the LNA capability to remain stable regardless of load conditions or the characteristics of external signal sources. This implies that the LNA will consistently maintain stability, unaffected by changes in load or the connection of external sources. This property guarantees reliable operation across various usage scenarios. Evaluating the stability of an LNA commonly involves Rollet's Stability Factor, denoted as  $K$ , which serves as a numerical parameter, which is calculated on the basis of the LNA  $S$  parameters. If the value of  $K$  exceeds 1, the circuit is considered unconditionally stable. Conversely, if it falls below 1, it indicates the presence of regions of instability or potential oscillations. Hence, a value greater than 1 is desired to ensure the unconditional stability of the LNA.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{22}S_{11} - S_{21}S_{12}|^2}{2|S_{12}||S_{21}|} > 1 \quad (32)$$

Mathematically, unconditional stability can be defined by establishing requirements for the magnitude of input and output reflection coefficients of a two-port, stating that they remain less than 1 for any passive load and source impedance. In this context, "passive" implies that the real part of the load and source impedance is positive, i.e.,  $|\Gamma_S| < 1$ ,  $|\Gamma_L| < 1$  [10].

The condition for input reflection coefficient ( $\Gamma_{IN}$ ) is expressed as:

$$|\Gamma_{IN}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1 \quad (33)$$

Similarly, the condition for output reflection coefficient ( $\Gamma_{OUT}$ ) is given by:

$$|\Gamma_{OUT}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{22}\Gamma_S} \right| < 1 \quad (34)$$

If either of the conditions (33) or (34) is violated, the two-port is considered conditionally stable. Conditional stability implies that the dual port will exhibit stability within a limited range of passive loads and source impedances while potentially displaying fluctuations for other passive terminations.



### 2.1.5 Linearity

Linearity is the ability of a Low-Noise Amplifier to faithfully amplify the input signal while minimizing the effects of distortion and intermodulation. Two fundamental parameters used to evaluate the linearity of an LNA are the Input Third-Order Intercept Point (IIP3) and the 1dB Compression Point (1dB CP). When the input signals have high power levels, devices become nonlinear, and the output signal reaches a saturation point. This phenomenon is known as gain compression. Background noise and gain compression define a dynamic range, which is the range of minimum and maximum power over which the two-port device will operate linearly. Operating below the 1 dB compression point ensures minimal distortion and maintains linearity, as an increase in input power results in a proportional increase in output power. When two or more signals are introduced into a nonlinear device, they interact with each other, generating additional frequencies called intermodulation products or distortion products, which were not present in the original signals. Among these, third-order products are particularly significant because they have higher amplitudes and are closer to the desired signals. Their proximity makes them more susceptible to interference and distortion, leading to signal quality degradation. For example, considering two input signals,  $f_1$  and  $f_2$ , the third-order intermodulation products include  $2f_1 - f_2$  and  $2f_2 - f_1$ . If these third-order products overlap with the frequency of other desired signals, they can cause interference, distortion, and the generation of unwanted signals. The IIP3 represents the input power level at which the third-order intermodulation products reach the same magnitude as the desired signal, causing distortion. A higher IIP3 value indicates greater linearity, as it means the amplifier can handle stronger input signals, in terms of power, without significant distortions. A commonly used graphical technique to characterize the linearity of a device or circuit operating in a limited frequency band is illustrated in Figure 15.

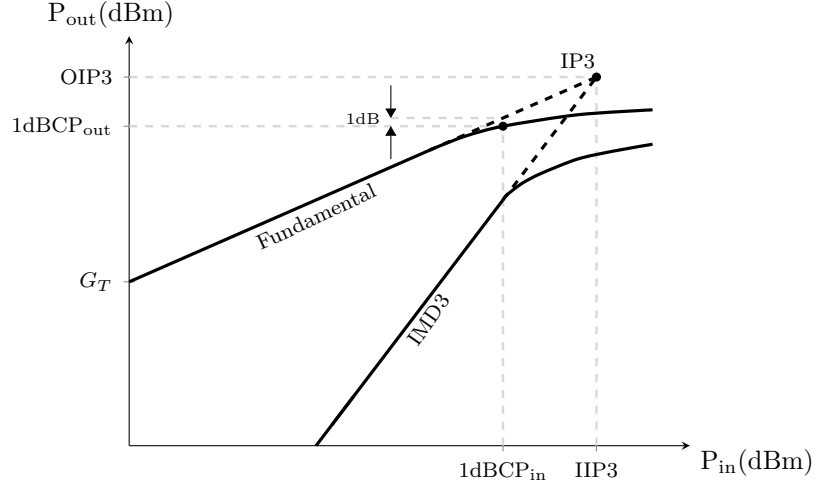


Figure 15: Graphical Representation of 1dB CP and IP3

In this diagram:

- IMD3 represents the measure of the third-order distortion products produced by a nonlinear device when two tones closely spaced in frequency are fed into its input:

$$IMD3 = k P_{in}^3 \quad (35)$$

From the definition of IIP3, we have:

$$G_T IIP3 = k IIP3^3 \implies k = \frac{G_T}{IIP3^2} \quad (36)$$

Then in logarithmic scale, we obtain:

$$\begin{aligned} 10 \log(IMD3) &= 10 \log(P_{in}^3) + 10 \log(k) \implies \\ 10 \log(IMD3) &= 30 \log(P_{in}) + 10 \log(G_T) - 20 \log(IIP3) \end{aligned} \quad (37)$$

- The input 1 dB Compression Point (1dB CP<sub>in</sub>) is defined as the input power at which the power gain ( $G_T$ ) decreases by 1 dB compared to its value for small-amplitude signals;
- The output 1 dB Compression Point (1dB CP<sub>out</sub>) is defined as the corresponding output power for the 1 dB Compression Point at the input;

- The Input Third-Order Intercept Point (IIP3) is defined as the input power level at which the output power of the fundamental signal and the output power of the IMD3 become equal;
- The Output Third-Order Intercept Point (OIP3) represents the corresponding output power level for IIP3;

## 2.2 Noise Analysis

Electronic noise is characterized by undesired, unpredictable fluctuations or disturbances within an electronic system. These fluctuations manifest as random variations in physical quantities, making them challenging to precisely predict using deterministic models. Nevertheless, statistical descriptions can be employed in certain cases to analyze these random fluctuations. To assess the magnitude of this randomness, one can study a stochastic process denoted as  $X(t)$ , which combines the deterministically known value of the observed quantity with a superimposed random phenomenon. The amplitude of this random variation can be quantified using the root mean square (RMS) value, providing a measure of its overall intensity:

$$X_{RMS}(t) = \sqrt{\int_{-\infty}^{\infty} x^2 f_x(x; t) dx} \quad (38)$$

Another key measure for analyzing electronic noise is the noise power spectral density (PSD), which provides information about the distribution of noise power across different frequencies, aiding in the identification of dominant noise sources within a specific frequency range:

$$S_x(f) = \lim_{T \rightarrow \infty} \frac{1}{T} |X_T(f)|^2 \quad (39)$$

where  $X_T(f)$  is the Fourier coefficient of the periodic extension of  $X(t)$  with period  $T$ , called  $X_T(t)$ .

The main sources of electronic noise that may introduce undesired changes in the voltage or current levels of electronic signals and cause distortion of the original transmitted information are [11]:

- Thermal noise
- Shot noise
- Flicker noise

### 2.2.1 Thermal Noise

Thermal noise, also known as *Johnson noise*, is a fundamental type of noise that occurs due to the random movement of charge carriers, within electronic components and conductors at non-zero temperatures. According to the principles of statistical mechanics, temperature is directly related to the average kinetic energy of particles. In electronic circuits, materials that conduct electricity, such as resistors and transistors, contain a multitude of electrons that are constantly in motion. These electrons interact with lattice vibrations, resulting in unpredictable fluctuations in their motion. Since electronic signals are usually very small, these random fluctuations can interfere with the desired signals, leading to a degradation in signal quality. The magnitude of thermal noise is determined by the well-known Johnson-Nyquist formula:

$$V_n = \sqrt{4kTR\Delta f} \quad (40)$$

Where:

- $V_n$  represents the noise voltage [V]
- $k$  denotes Boltzmann's constant ( $1.38 \times 10^{-23}$  J/K);
- $T$  corresponds the absolute temperature [K];
- $R$  is the resistance [ $\Omega$ ];
- $\Delta f$  indicates the considered bandwidth [Hz].

Therefore, the available thermal noise power  $P_n$ , i.e. the thermal noise power that a resistor can supply to a matched load and the thermal noise power spectral density  $S_{V_n}$  generated by a resistor, can be expressed, respectively, from the equations (41) and (42):

$$P_n = kT\Delta f \quad (41)$$

$$S_{V_n}(f) = 4kTR \quad (42)$$

From the formulas, it is evident that increasing temperature or resistance or widening the bandwidth results in higher levels of thermal noise. It is important to consider these factors in electronic circuit design and signal processing to minimize the impact of thermal noise on signal quality. Moreover, utilizing equation (41), it is possible to determine the minimum equivalent input noise, or noise floor, for a receiver at room temperature ( $T_0 = 17^\circ\text{C}$  or  $T_0 = 290\text{ K}$ ) with a 1 Hz bandwidth:

$$10\log(kT_0) = 10\log(1.38 \times 10^{-23} \times 290) \approx -174\text{ dBm/Hz} \quad (43)$$

This value represents the theoretical lower limit of detectable signals in a system due to the presence of thermal noise. Signal levels below this noise floor are often considered too weak to be reliably distinguished from the noise.

### 2.2.2 Shot Noise

Shot noise, also known as Poisson noise, is a fundamental type of electrical noise that arises from the discrete nature of electric charge and the statistical behavior of electrons. The random fluctuations in current or voltage levels caused by shot noise are a result of the discrete arrival of charge carriers at a given time interval. This noise can be described by a Poisson distribution, and its magnitude increases with the average current. The shot noise current mean-squared value can be expressed as:

$$I_n^2 = 2qI_0\Delta f \quad (44)$$

Here,  $q$  represents the elementary charge ( $1.602 \times 10^{-19}$  C),  $I_0$  is the average current flowing through the device, and  $\Delta f$  is the bandwidth over which the noise is measured.

The power spectral density of shot noise is:

$$S_{I_n}(f) = 2qI_0 \quad (45)$$

This equation indicates that shot noise is frequency-independent, often referred to as white noise. Shot noise is an important consideration in various fields, including communication systems, semiconductor devices, and photonics. In these fields, precise signal detection and accurate measurements are crucial, and understanding and managing shot noise are essential for achieving reliable performance.

### 2.2.3 Flicker Noise

Flicker noise, also known as  $1/f$  noise, is a type of electronic noise that exhibits a spectral density decreasing as frequency increases. It is particularly important in low-frequency applications. The power spectral density of flicker noise can be described mathematically using Hooge's constant ( $\alpha_H$ ), and specific constants ( $\beta$  and  $\gamma$ ) that vary for each device:

$$S_{I_n}(f) = \alpha_H \frac{I^\beta}{f^\gamma} \quad (46)$$

The primary cause of  $1/f$  noise in semiconductor devices can be attributed to the technological process by which the device is manufactured, specifically the density of states. The occurrence of flicker noise is a result of the random nature of carrier generation and recombination processes. These processes introduce fluctuations in the carrier density, consequently leading to variations in the current flowing through the device and giving rise to flicker noise. The density of states represents the number of available energy states within a specific energy range in the material. A higher density of states implies a greater number of states accessible for carriers to occupy or vacate, so it intensifies the trapping and detrapping processes, thereby amplifying the level of flicker noise. Comprehending and regulating the generation

and recombination of carriers in energy states, as well as managing the density of states, is critical for minimizing flicker noise in electronic devices and systems.

In summary, conducting a thorough noise analysis and identifying the sources of noise enable the implementation of a wide range of highly effective strategies to mitigate or minimize noise. These strategies may include techniques like shielding, filtering, incorporating low noise components, and amplifiers. By employing such measures, optimal performance levels can be achieved for electronic systems, guaranteeing their smooth operation.

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# Analysis of the Current BPM System in the PS Ring

Chapter 3 focuses on the analysis of the BPM system currently used in the PS particle accelerator. Particular attention is given to the detailed description of the Low-Noise Amplifier employed, and the results of simulations and measurements conducted on the system are presented. Additionally, the chapter examines in detail the measurement methods that have been tested, with a particular emphasis on evaluating the noise figure of the LNA. Another important aspect is the positioning strategy of the LNA within the PS to ensure effective shielding from the radiation generated by the particle accelerator. This aspect is of fundamental importance to ensure the proper functioning and longevity of the device.

## 3.1 Overview of the Current BPM System

The initial phase of the project focused on an in-depth analysis of the currently used system in the PS particle accelerator. This preliminary stage involved a comprehensive theoretical study and simulations of the existing system, examining its specifications and performance characteristics. Concurrently, rigorous laboratory tests were conducted to acquire empirical data regarding the system behavior. From the outset, the primary objective of this phase was to obtain a profound understanding of the functioning of the current system under various operating conditions and identify potential areas for improvement or alteration in the context of the new project. The adopted approach in this study has established a solid foundation for designing the new LNA, with the aim of updating the electronics, but without compromising the current performance.

The block diagram in Figure 16 illustrates the comprehensive configuration of the current BPM system that consists of a pick-up module, responsible for capturing



the signals from the particle beam, and an external chassis housing the Low-Noise Amplifier and other necessary electronics for signal processing.

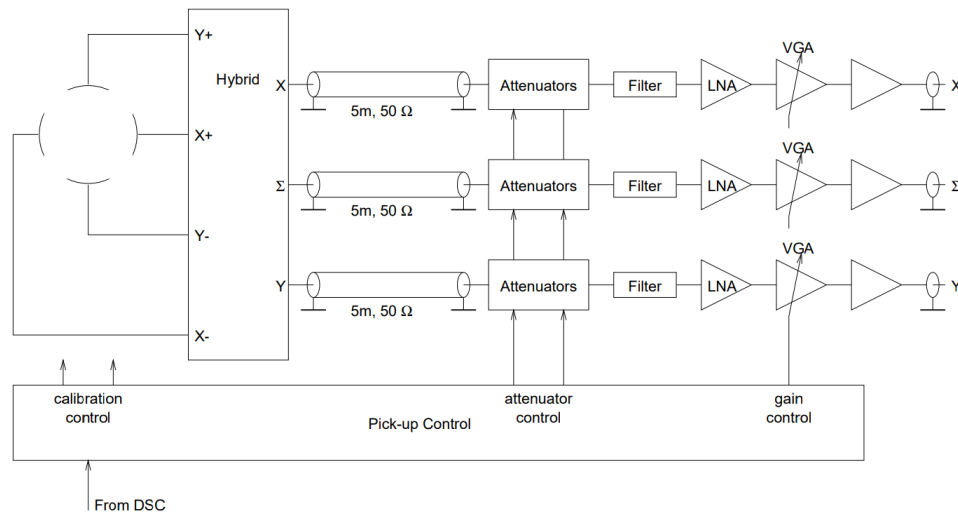


Figure 16: Block Diagram of the Current BPM System [12]

The pick-up module is strategically positioned in close proximity to the particle beam to ensure efficient and accurate signal capture. A 5-meter long cable connects the pick-up module to the external chassis, allowing the acquired signals to be transmitted for further processing. The selection of this cable is crucial to preserve signal integrity, requiring careful consideration of shielding and impedance matching to minimize any potential signal loss or interference. Recognizing the sensitive nature of the electronics within the system and the radiation environment prevalent near the particle accelerator, the external chassis has been installed in a gap between two concrete blocks, as shown in Figure 17. This strategic placement provides effective shielding, safeguarding the components from potential damage or interference caused by high-energy radiation. It is worth noting that semiconductor electronics can generally withstand an integrated dose of roughly 0.5 Gy to 1 kGy, provided that appropriate devices and design methods are carefully selected. Importantly, the area where the pick-up module is installed is subjected to a yearly radiation level of approximately 40 kGy, whereas the yearly radiation in the concrete gap measures around 40 Gy [12]. This significant difference in radiation between the two areas

demonstrates that concrete acts as a formidable barrier against high-energy radiation, substantially reducing the exposure of the electronic elements to radiation levels that are more acceptable for their proper operation.

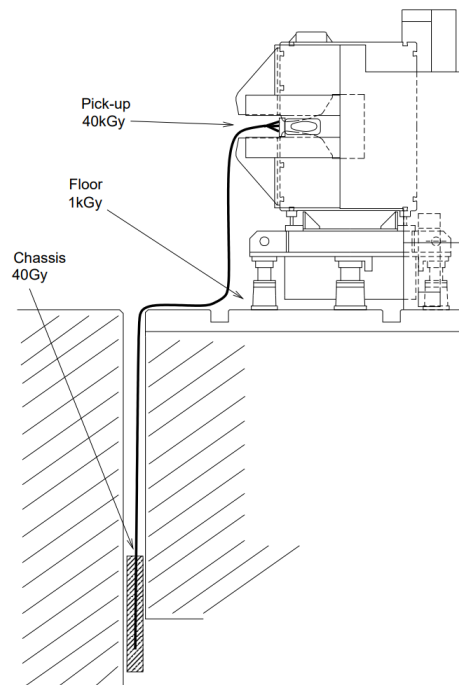


Figure 17: Electronics Chassis in gap between two Concrete Blocks

### 3.2 Examination of the Current LNA

The Low-Noise Amplifier adopted for the present system is a folded cascode with lossless feedback configuration, featuring two key stages. As can be observed from the Figure 18, the first stage consists of three BF862 JFET (Junction Field-Effect Transistor) devices connected in parallel, while the second stage employs a cascode arrangement incorporating the BFT92 and BFR92A transistors. Additionally, two feedback mechanisms are present: the first feedback is constituted by a transformer formed by L1, L2, L3, and L4, which is useful for precisely adjusting the gain of the LNA, while the second feedback, consisting of the resistance  $R_{20}$ , sets the impedance seen at the JFET gates to  $200\ \Omega$ . This impedance value is optimal for noise per-

formance, effectively minimizing the noise figure of the amplifier. Furthermore, a transformer is used to convert the input impedance to  $50\ \Omega$  and thus obtain the input matching.

The configuration adopted in the first stage serves to enhance the noise performance of the LNA by limiting the collective noise voltage supplied by each JFET. The voltage noise of a single JFET is approximately  $0.8\ \text{nV}/\sqrt{\text{Hz}}$ . Through the parallel combination of the three JFETs, the total voltage noise is reduced by a factor equal to  $\sqrt{3}$  corresponding to approximately  $460\ \text{pV}/\sqrt{\text{Hz}}$  and an equivalent noise figure of approximately 1 dB:

$$NF = 10 \log \left[ \left( \frac{V_n}{\sqrt{4kTR_S}} \right)^2 + 1 \right] = 10 \log \left[ \left( \frac{460\ \text{pV}/\sqrt{\text{Hz}}}{0.9099\ \text{nV}/\sqrt{\text{Hz}}} \right)^2 + 1 \right] = 0.988\ \text{dB} \quad (47)$$

This significant reduction in voltage noise allows for a LNA with extremely high sensitivity, crucial for detecting weak signals. However, it is worth noting that the number of JFETs represents a trade-off. Increasing the number of JFETs in parallel reduces the voltage noise, thereby improving the LNA noise performance. On the other hand, an increase in the number of JFETs in parallel results in a rise in the overall gate capacitance, which can worsen the amplifier frequency response. Consequently, optimizing the number of devices in parallel is an important aspect in balancing the noise performance and frequency response characteristics of the LNA.

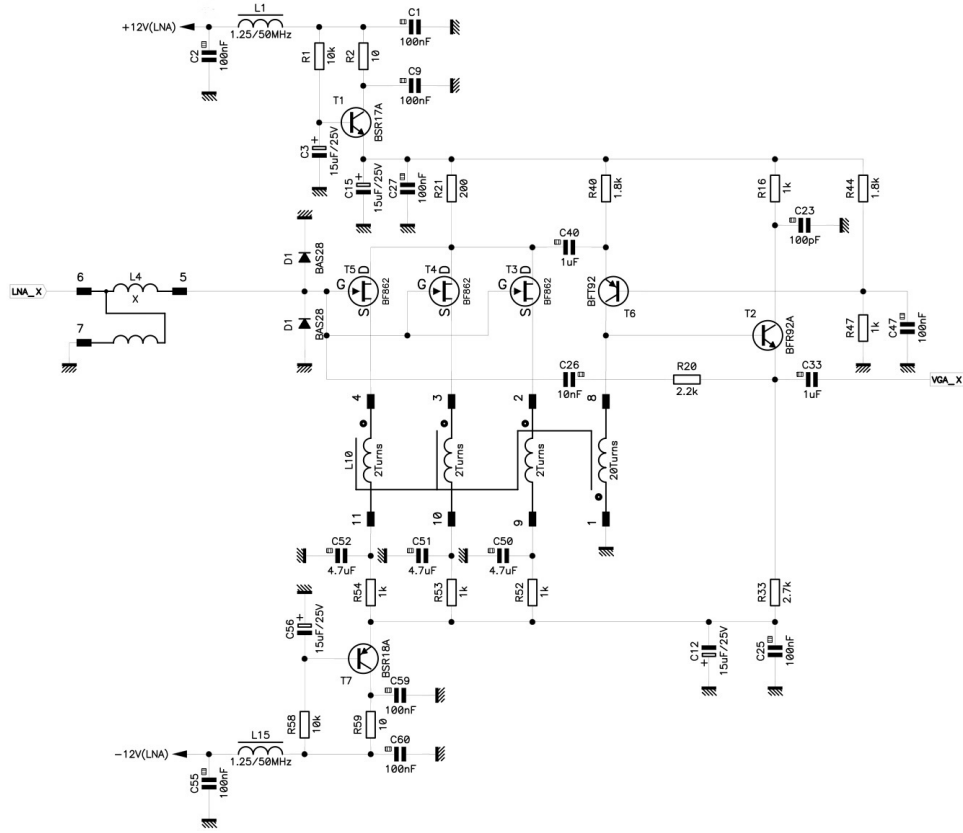


Figure 18: LNA Schematic of the Current System

To thoroughly evaluate the performance of the current Low-Noise Amplifier (LNA) and closely examine its behavior and characteristics under controlled conditions, the first step was to conduct simulations using LTspice XVII. The simulation process involved creating a circuit using ideal components. By running the simulations, we obtained detailed results for power gain ( $S_{21}$ ), input reflection coefficient ( $S_{11}$ ), and noise figure (NF). As shown in following figures, simulations revealed that the LNA exhibits a power gain of around 24 dB, an input reflection coefficient of around -27 dB and a noise figure of around 1.5 dB. These simulated values were used as a reference point to understand the expected performance of the LNA in an ideal context.

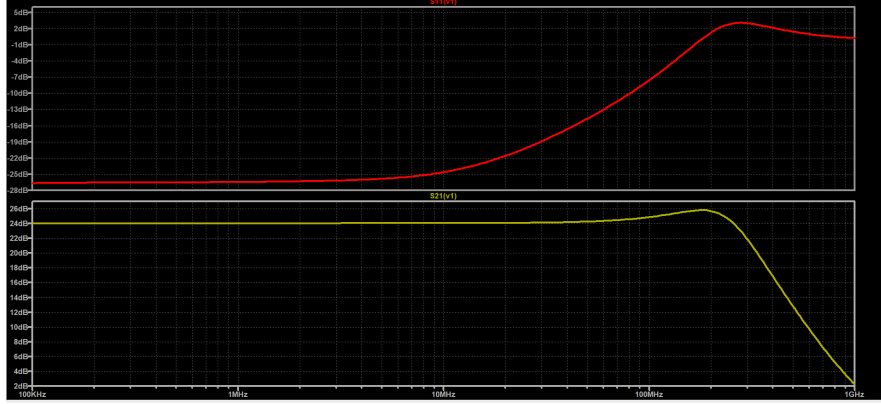


Figure 19: Plots of  $S_{21}$  and  $S_{11}$  for the Current LNA

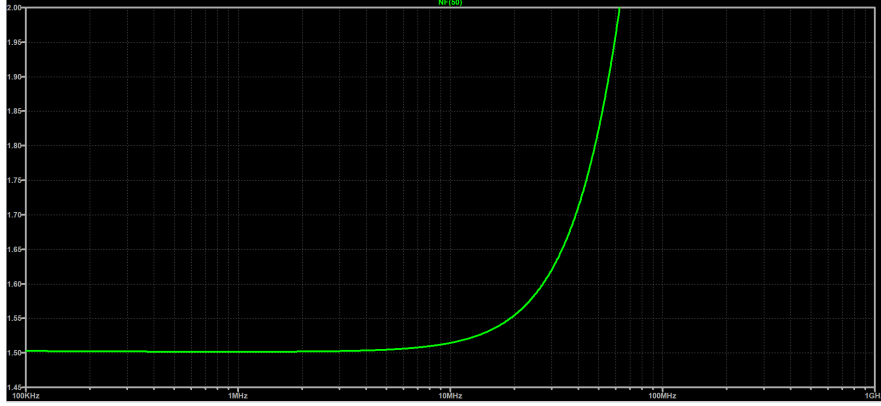


Figure 20: Plot of NF for the Current LNA

However, the practical performance of the LNA is inevitably influenced by various non-idealities, such as parasitic effects and component variations. For this reason, extensive laboratory measurements were conducted on the physical prototype of the LNA. By juxtaposing simulation and experimental data, we gained a comprehensive understanding of the current LNA actual performance under real-world conditions. This process allowed us to not only quantify the LNA gain, input matching, and noise figure accurately but also to pinpoint any deviations or limitations in the design. The power gain and input reflection coefficient were measured using the Rohde & Schwarz ZNB4 VNA (Vector Network Analyzer), and the results of these measurements showed no significant deviation from the simulated values obtained in LTspice

XVII. This consistency between simulation and measurement validated the accuracy of the simulation model, providing confidence in its predictive capability regarding S-parameters. However, measuring the very low noise figure proved to be more complex, as it necessitated finding a reliable and suitable method to obtain accurate measurements. The pursuit of an appropriate NF measurement technique required time and effort. Various methods were explored and evaluated to determine the most reliable approach. Among these, the method that allowed us to obtain reliable results is the one known as the Y-factor method. This technique involves employing a noise source that has a pre-calibrated Excess Noise Ratio (ENR), which is a crucial parameter in the process. The ENR is defined as the ratio between the difference in noise temperatures of the noise source in its *on* (*hot*) and *off* (*cold*) states and the reference temperature (usually taken as 296K) [13]:

$$ENR_{dB} = 10 \log \left( \frac{T_{sh} - T_{sc}}{T_0} \right) \quad (48)$$

The ENR calibration of the noise source is essential to accurately quantify the noise power added by the DUT. By knowing the ENR value, one can establish a direct relationship between the measured noise power and the actual noise temperature of the DUT.

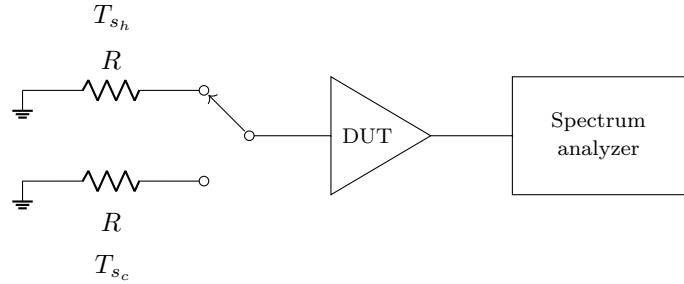


Figure 21: Block Diagram of the Y-factor Method

The Y-factor itself is a key metric in this method, representing the ratio of two noise levels: one measured with the noise source hot and the other with the noise source cold:

$$Y = \frac{N_h}{N_c} \quad (49)$$

The key advantage of using the Y-factor method lies in its ability to model the DUT noise performance through its equivalent noise temperature, denoted as  $T_e$ . This equivalent noise temperature represents the effective noise temperature that would produce the same amount of output noise power as the DUT. It can be calculated as:

$$T_e = \frac{N_{o(\text{added})}}{kBG_A} \quad (50)$$

Where  $N_{o(\text{added})}$  is the additional output noise power contributed by the DUT,  $k$  is Boltzmann's constant,  $B$  is the DUT available bandwidth, and  $G_A$  is the DUT available power gain.

By modeling the component noise through its noise temperature, we can easily find the output noise for the two input noise levels. According to [14], the output noise for the hot source ( $N_h$ ) at temperature  $T_h$  is given by equation (51), and the output noise for the cold source ( $N_c$ ) at temperature  $T_c$  is determined using equation (52):

$$N_h = kT_hBG_A + kT_eBG_A \quad (51)$$

$$N_c = kT_cBG_A + kT_eBG_A \quad (52)$$

Substituting (51, 52) in (49), we get the following equation for the Y-factor:

$$Y = \frac{T_{sh} + T_e}{T_{sc} + T_e} \quad (53)$$

From which is derived:

$$T_e = \frac{T_{sh} - Y T_{sc}}{Y - 1} \quad (54)$$

Once  $T_e$  is determined, we can then calculate the noise figure ( $NF$ ) using the following equation:

$$NF = 10 \log \left( 1 + \frac{T_e}{T_0} \right) \quad (55)$$

In our context, we have adopted a measurement approach based on the use of the Noisecom NC346Y noise source, as depicted in Figure 22. This noise source is characterized by a signal-to-noise ratio (ENR) of 15.14 dB at a frequency of 10 MHz. Additionally, for conducting this analysis, we employed the Anritsu MS2692A spectrum analyzer, equipped with the "noise figure measurement" function. This function, leveraging knowledge of the noise source used, allows for the direct calculation of the noise figure without the need for additional calculations or external processing.



Figure 22: Noisecom NC346Y Noise Source

The noise source is set to generate a broadband noise signal covering the desired frequency range and generates noise known as Additive White Gaussian Noise (AWGN) using a Zener Diode. This diode simulates various random processes observed in nature. In Figure 23, it can be observed that when a 28 V power supply is applied to the noise source, the diode is reverse-biased into the avalanche region. In this state, the diode produces a significant amount of noise due to the avalanche effect, which



involves electronic generation and multiplication of electrons across the p-n junction, resulting in the generation of high-power noise. This noise is essential for generating a random signal of uniform amplitude at various frequencies. On the other hand, when the power supply is disconnected, the noise source shows only a small amount of noise at the output since the diode is no longer biased and is not involved in the noise generation process. To ensure a constant and well-defined output, an RF choke (RFC) is used, which is a large enough inductor to act as an open circuit at all the frequencies of interest and ensures the decoupling of the DC power supply. Finally, an attenuator is used, which must be designed to produce the necessary attenuation and at the same time match the impedances. This attenuator ensures also that whether the diode is on or off, the noise source maintains a relatively constant match at the output.

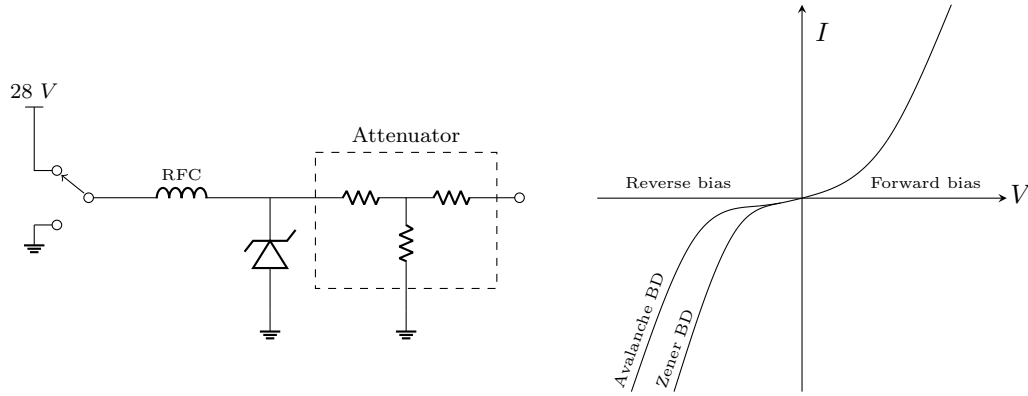


Figure 23: Schematic of a Diode-based Noise Source and Zener Diode I-V Curve

The measurement process begins with a calibration operation, which plays a vital role in ensuring precise noise figure measurements. During calibration, the measurement system is configured to compensate for losses and distortions introduced by cables, adapters, and other components between the noise source and the amplifier input, as well as between the amplifier output and the spectrum analyzer. This step ensures that the system is calibrated to measure only the characteristics of the device under test (DUT) and not any external influences. Once calibration is completed, the noise source is connected to the LNA input, while the LNA output is connected to the input of the spectrum analyzer. After setting up the equipment, the measurement parameters, such as the frequency range and resolution bandwidth, are adjusted to

display the measure of the noise figure.

For the specific Low-Noise Amplifier being used, the results over a frequency range of 1 MHz to 30 MHz are tabulated in the Table 1 ( $NF$  (dB) -  $LNA$ ). Considering the reference frequency of 10 MHz, the measured noise figure of LNA is found to be equal to 1.237 dB.

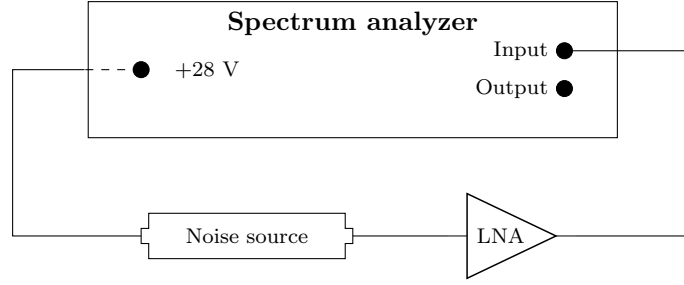


Figure 24: LNA Noise Figure Measurement

In the same way, the measurement of the entire chassis was also carried out, and the results are reported in the Table 1 ( $NF$  (dB) -  $Chassis$ ).

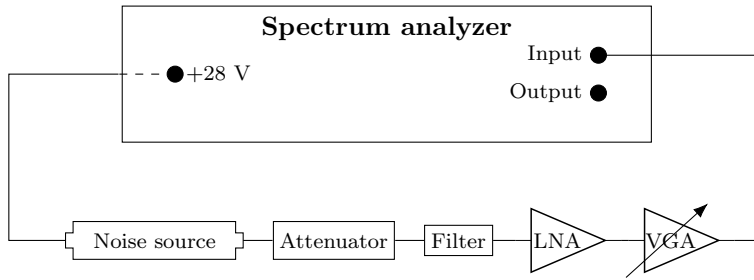


Figure 25: Chassis Noise Figure Measurement

| Frequency (MHz) | NF (dB) - LNA | NF (dB) - Chassis |
|-----------------|---------------|-------------------|
| 1               | 2.367         | 2.449             |
| 3               | 1.389         | 2.288             |
| 5               | 1.215         | 2.332             |
| 7               | 1.295         | 2.328             |
| 10              | 1.237         | 2.473             |
| 13              | 1.345         | 2.644             |
| 15              | 1.206         | 2.806             |
| 17              | 1.211         | 3.027             |
| 20              | 1.303         | 3.368             |
| 23              | 1.216         | 3.787             |
| 25              | 1.431         | 4.041             |
| 27              | 1.619         | 4.354             |
| 30              | 1.544         | 4.671             |

Table 1: Summary of LNA and Chassis Noise Figure Measurement Results

To evaluate the noise figure of the entire chassis, another noise source, designed by the current system designer, was employed (Figure 26). This source consists of two resistors controlled at specific physical temperatures to generate the required noise levels for the experiment. To create the cold noise source, one resistor is immersed in liquid nitrogen ( $LN_2$ ), maintaining a constant temperature of 77 K. This low-temperature environment ensures a stable and well-defined generation of the noise signal, significantly contributing to measurement precision. For the hot noise source, the ambient temperature of approximately 296 K is utilized. To preserve the integrity of the noise signals and minimize unwanted interference, a high-quality coaxial relay is used to connect the resistors to the chassis input. Subsequently, the noise figure

measurement was conducted in two ways. In the first method, the same spectrum analyzer previously used was employed, automatically providing the noise figure (NF) measurement. The results are presented in Table 2 under the column (NF (dB) -  $M_B$ ). In the second method, the measurement was more manual: the spectrum analyzer was used to measure the output noise under hot/cold conditions, and manual calculations were performed to determine the Y-factors and, consequently, the NF. The results are shown in the column (NF (dB) -  $M_A$ ) of Table 2. In the second case, to obtain accurate measurements of the Y-parameter using the spectrum analyzer, it was essential to properly set up the instrument. First, adjust the internal attenuator to 5 dB and set the resolution bandwidth (RBW) to 300 kHz, along with the video bandwidth (VBW) to 30 Hz, ensuring that the internal amplifier is turned off. Next, set the desired center frequency. Then, define a delta marker and proceed with the measurement of the output noise using both the hot and cold sources. The measured values correspond to the Y-factors of the entire chassis, including the attenuator, low-pass filter, LNA, and VGA. It is worth noting that among the obtained noise figure results listed in the table, no significant differences are evident.

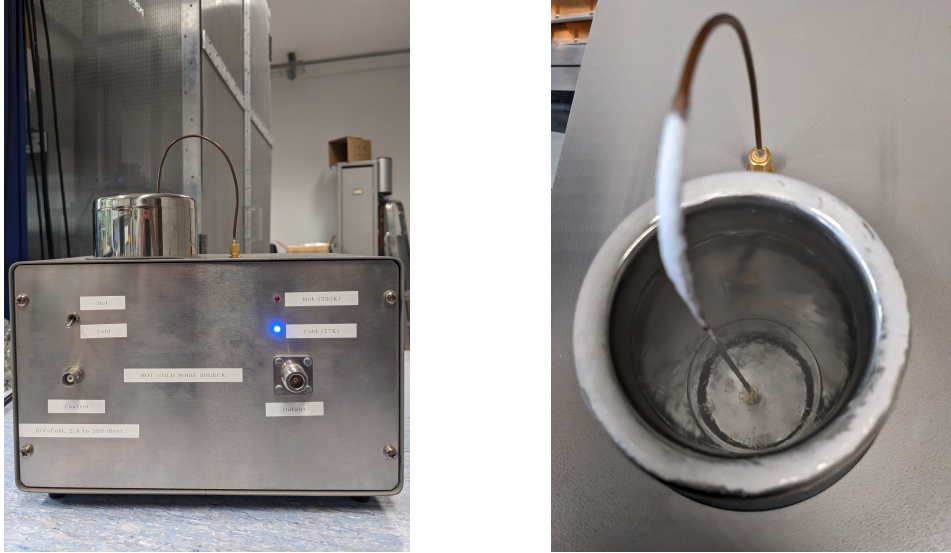


Figure 26: Cold Noise Source - Resistor in  $LN_2$

| Frequency (MHz) | Y (dB) | NF (dB) - M <sub>A</sub> | NF (dB) - M <sub>B</sub> |
|-----------------|--------|--------------------------|--------------------------|
| 0.5             | 2.5    | 2.31                     | -                        |
| 5               | 2.5    | 2.31                     | 2.33                     |
| 10              | 2.7    | 2.32                     | 2.47                     |
| 20              | 1.9    | 3.24                     | 3.37                     |
| 30              | 1.3    | 4.62                     | 4.67                     |

Table 2: Chassis Noise Figure Measurement Results

In conclusion, the measurement of LNA compression was performed using the VNA. The LNA exhibits a compression of 0.1 dB when the input power is -24 dBm and a 1 dB compression point at an input power of -22 dBm.

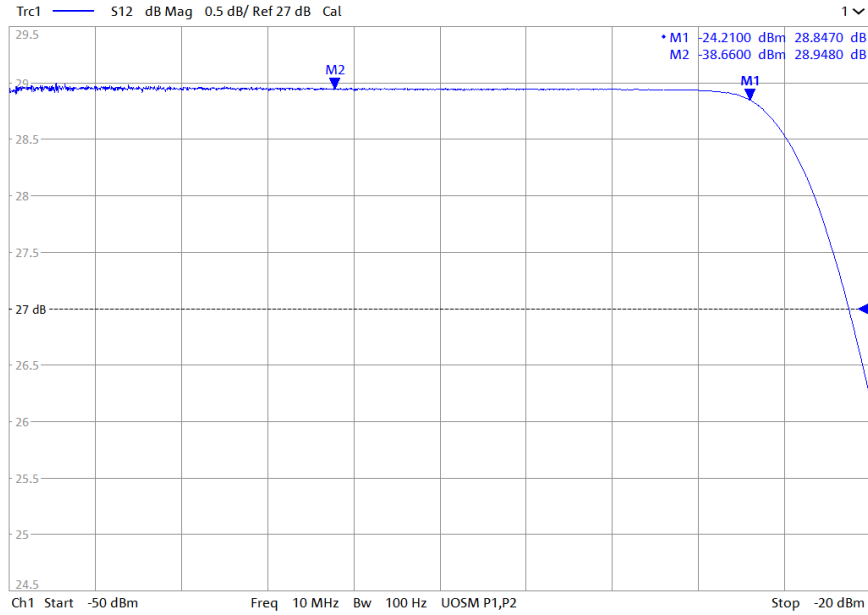


Figure 27: 1dB and 0.1dB Compression Points at 10 MHz - Laboratory Measurement of the Current LNA

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# SiGe HBT LNA Design Methodology

Chapter 4 focuses on the methodology used to design the LNA, discussing the selected components in detail and illustrating the principles applied to design the LNA schematic. Initially, the project specifications are examined, including the noise figure, the input matching, and the bandwidth. Next, a detailed explanation for the choice of SiGe HBT technology and the active component to be used in the first stage of the LNA is provided. Furthermore, the design flow adopted to obtain the first stage prototype is described in depth, showing the results of the simulations and laboratory tests. In the final part, the principles adopted for the design of the second stage and the feedback present in the system are discussed in detail, also explaining the components used.

## 4.1 Key Requirements for the New Low-Noise Amplifier

The primary goal of this project is to upgrade the LNA currently used in the analog front-end of the beam position monitor for the proton synchrotron. Despite proven reliability and functionality over time, the LNA electronics is gradually approaching the end of its life cycle. This puts the system in a phase that requires a proactive approach to ensure that optimal performance is maintained. The electronics renewal process represents a crucial step to enhance the LNA performance and allow it to be adapted to future challenges. In addition, the upgrade of the electronics results in greater robustness of the system in the long term, minimizing the dependence on obsolete and hard to find components.

Based on the in-depth analysis of the current LNA, discussed in the previous chapter, we were able to define the following key specifications for the new project:

- Noise Figure: the LNA is expected to have a noise figure (NF) of less than 2 dB. Attaining a low noise figure ensures that the LNA contributes minimal additional noise to the original signal, thereby preserving its quality and maximizing the overall signal-to-noise ratio.
- Bandwidth: the LNA must operate within a bandwidth ranging from 100 kHz to 50 MHz. The aim is to extend the bandwidth compared to the current LNA, which is limited to 30 MHz by an input filter, while also considering the integration requirements with the other system components.
- 50  $\Omega$  Input Matching: the LNA should exhibit excellent input matching with a reflection coefficient  $S_{11}$  below -20 dB. This characteristic facilitates efficient power transfer between the coaxial cable and the LNA, minimizing signal reflections and maximizing signal integrity.

In order to achieve the objectives of the project, extensive research was carried out to identify an appropriate new technology. Among the various options, the silicon-germanium heterojunction bipolar transistor (SiGe HBT) emerged as a particularly promising choice for the implementation of the new Low-Noise Amplifier. The following sections provide an exhaustive description of this technology, underlining the figures of merit (FOM) that demonstrate its adaptability to our specific use case.

## 4.2 The SiGe HBT Technology

In the field of Radio-Frequency (RF) electronics, various semiconductor materials are widely used, among which silicon-germanium (SiGe) and gallium arsenide (GaAs) stand out. These materials are employed in various types of transistors, such as the bipolar junction transistor (BJT), the heterojunction bipolar transistor (HBT), the metal-semiconductor field-effect transistor (MESFET), the high electron mobility transistor (HEMT), and the metal-oxide-semiconductor field-effect transistor (MOSFET). It is of fundamental importance to assess the advantages and limitations of these devices through the analysis of common figures of merit (FOM), which include current-voltage characteristics, stability, power gain analysis, cutoff frequency, maximum oscillation frequency, and noise factor. This analysis allows for a significant comparison between devices, facilitating technological choices, especially

in application areas such as Low-Noise Amplifiers, power amplifiers, and transmission/reception systems.

Early bipolar junction transistors (BJT) were considered unsuitable for RF and microwave circuit applications, due to the limited mobility of both electrons and holes in silicon. Indeed, electrons in silicon reach a maximum speed of approximately  $1 \times 10^7$  cm/s, making silicon a relatively “slow” semiconductor [15]. Therefore, while silicon integrated circuits are cost-effective, they cannot provide optimal performance for designing high-frequency systems. For this reason, III-V materials, such as GaAs, despite being more expensive, have dominated the RF and microwave market. However, through the implementation of silicon-germanium (SiGe) alloys to manipulate the silicon band gap (known as “Band gap engineering”), it was possible to improve the performance of silicon transistors in the RF field. Based on that, silicon has emerged as a contender against III-V devices, mainly because it guarantees a less expensive production process. Although the idea of using SiGe alloys to control the band gap in silicon devices dates back to the 1960s, the synthesis of defect-free SiGe films proved to be a challenge until the 1980s. Indeed, it was only through the development of a suitable technique for growing a homogeneous SiGe alloy on silicon that it became possible to implement the concept of combining silicon and germanium into an alloy for use in transistors [16]. The introduction of Germanium (Ge) into Silicon (Si) has significant implications. First of all, thanks to the higher lattice constant of Ge compared to Si, the energy band gap of Ge is smaller (0.66 eV) than that of Si (1.12 eV). This means that thanks to the difference in band gap between silicon and germanium, it is possible to perform band gap engineering by acting on the relative concentrations of the two materials, making SiGe a good candidate for band gap engineering. Moreover, to maintain stability and defect-free characteristics, SiGe must be thin [17]. Consequently, the SiGe proves fitting for the base region, where a small thickness is intrinsically required to obtain proper performance. This leads to the formation of a device that contains an n-Si/p-SiGe emitter-base (EB) heterojunction and a p-SiGe/n-Si base-collector (BC) heterojunction. This device is commonly known as a “SiGe Heterojunction Bipolar Transistor” (SiGe HBT), although it is more accurately called a “Double Heterojunction SiGe Bipolar”. The Figure 28 illustrates the energy band diagrams of SiGe HBT and Si BJT transistors. The two devices have an identical geometry (emitter, base, collector), and it is assumed that the doping profiles of the emitter and the collector are the same. However, the main difference lies in the structure of the base. In the case of the SiGe transistor, the base is gradually



diffused, presenting a doping profile that progressively varies from the emitter-base junction to the collector-base junction. This approach was originally proposed by Herbert Kroemer in 1953 [18]. Kroemer’s idea consisted of using a “drift transistor” to generate an electric field in the base region and to reduce the barrier to electron injection at the EB junction. This strategy accelerates the movement of minority carriers from the emitter to the collector, leading to a significantly improved frequency response. The realization of such a device involves gradually increasing the Germanium (Ge) content linearly from 0% near the EB junction until reaching the maximum value near the CB junction, followed by a decrease to return to 0%. This unique feature of SiGe HBT devices provides an additional degree of flexibility in design. The main reason underlying the use of a heterojunction in HBT lies in the use of SiGe as the material in the base region. This choice results in a different alignment between the valence band ( $B_V$ ) and the conduction band ( $B_C$ ). As a result, there is a significant reduction in the injection of holes from the base to the emitter. This mechanism circumvents the need to have a strongly doped emitter relative to the base, as is common in conventional BJTs. The elimination of this requirement allows the doping concentration in the base region to be increased, thereby reducing the resistance in this area and consequently improving high-frequency performance.

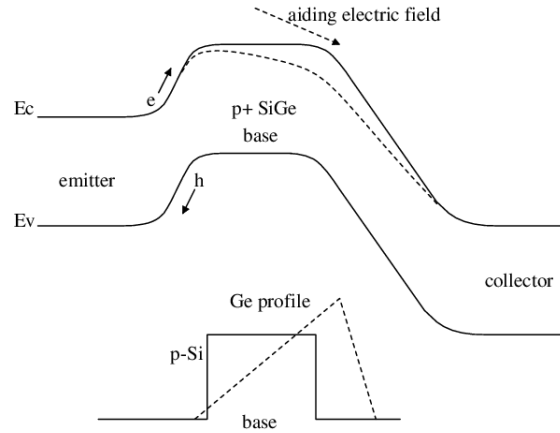


Figure 28: Energy Band Diagram comparison between Si BJT and SiGe HBT

### 4.2.1 Suitability to Our Case

In the design of the Low-Noise Amplifier which is the subject of this thesis, the choice was made to use an RF transistor fabricated with SiGe HBT technology. This selection was motivated by the exceptional performance offered by these devices, both in terms of flicker noise ( $1/f$ ) and cutoff frequency ( $f_T$ ). The cutoff frequency of a transistor plays an extremely important role since it determines the frequency response of the transistor itself and, consequently, limits the performance of the entire system. To calculate the cutoff frequency of a bipolar transistor, the following equation is used [16]:

$$f_T = \frac{1}{2\pi} \left( \frac{kT}{qI_c} (C_{eb} + C_{cb}) + \tau_e + \tau_{eb} + \tau_b + \tau_c + \tau_{bc} \right)^{-1} \quad (56)$$

where  $C_{eb}$  and  $C_{cb}$  represent the emitter-base and collector-base capacitances, while  $\tau_b$ ,  $\tau_e$ , and  $\tau_c$  denote the base, emitter, and collector transit times, respectively. Additionally,  $\tau_{eb}$  and  $\tau_{bc}$  correspond to the emitter-base and collector-base space charge region delay times, respectively.

It is evident that the decrease in  $\tau_b$ , caused by the presence of SiGe, directly leads to an increase in the cutoff frequency  $f_T$ , compared to conventional Si BJT. According to the results presented in [15], SiGe HBT demonstrates a substantial improvement in cutoff frequency  $f_T$  compared to similarly designed Si BJT. This improvement is experimentally illustrated in Figure 29, with a remarkable enhancement of approximately 1.7 times. This performance makes SiGe HBT particularly suitable for high-frequency operation and perfectly matches the required range between 100 kHz and 50 MHz for our LNA.

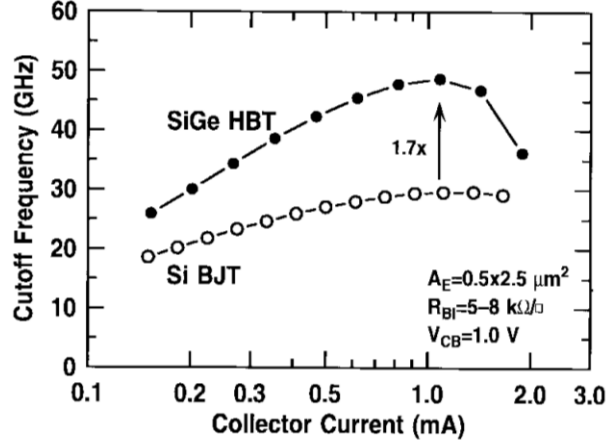


Figure 29: Cutoff Frequency comparison between Si BJT and SiGe HBT [15]

Another important distinctive feature of SiGe HBT transistor is its excellent performance in terms of  $1/f$  noise. This device produces less noise at low frequencies compared to other technologies such as silicon CMOS devices, GaAs MESFETs, GaAs HEMTs, and GaAs HBTs. In practice, SiGe HBTs exhibit an  $1/f$  noise performance comparable to that achieved with Si BJTs, achieving a  $1/f$  noise corner frequency below 500 Hz [16]. This result is highlighted in Figure 30.

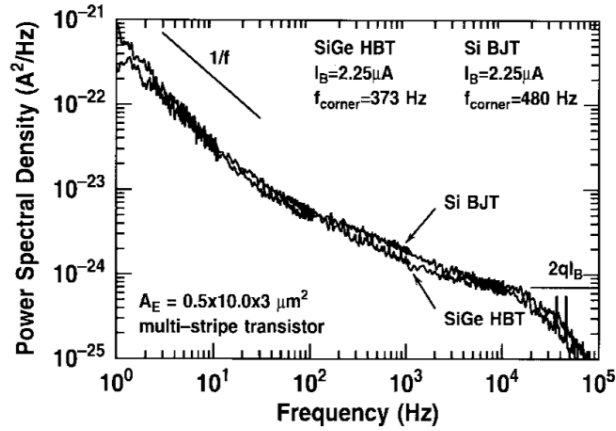


Figure 30: Comparison of the low-frequency noise characteristics between Si BJTs and SiGe HBTs [15]

The difference from the point of view of  $1/f$  noise between SiGe transistors and silicon transistors with identical area is of great relevance. As highlighted in [15], to improve wideband noise performance, it is essential to reduce the base resistance  $R_{bb}$ , increase the transition frequency  $f_T$ , and enhance the current gain ( $\beta$ ). Bandgap engineering has proven to be an ideal tool to achieve these results, and therefore SiGe BJT transistors excel in wideband noise performance.

Furthermore, another strong point of SiGe HBT transistors lies in their lower intrinsic noise compared to other alternative technologies, in fact, it ensures a minimum noise figure below 0.7 dB at 2.0 GHz, as illustrated in Figure 31. These exceptional performance characteristics allow low-noise amplifiers based on SiGe HBT to achieve a noise figure below 2 dB showing optimal signal quality.

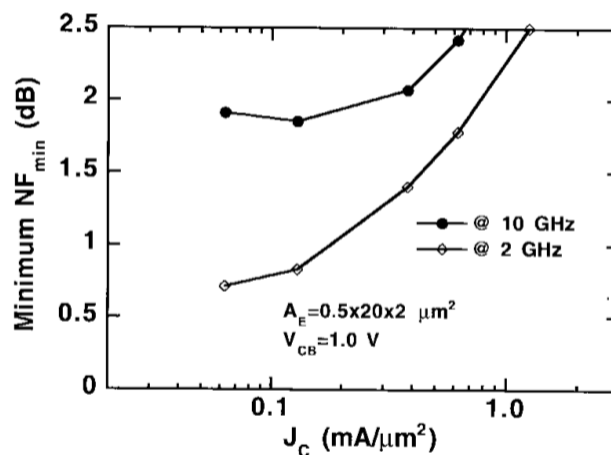


Figure 31: Minimum Noise Figure of a SiGe HBT [15]

Finally, SiGe HBT components enjoy proven reliability and long-term availability, providing assurance for project continuity and minimizing the dependence on obsolete and hard-to-find parts. This aspect is crucial to ensure reliable operation and sustainable production of the Low-Noise Amplifier.

### 4.3 LNA Design Process

The design process of the SiGe HBT-based Low-Noise Amplifier has been thoroughly and systematically conducted, in two distinct phases. Initially, special attention was dedicated to the design and analysis of the first stage. This stage, playing a crucial role in the initial signal amplification and noise reduction, required meticulous selection of the active component and careful exploration of the most suitable topology. Subsequently, following the design flow until the Printed Circuit Board (PCB) fabrication, the primary objective was to produce a prototype of the first stage. This prototype underwent a series of tests aimed at evaluating the suitability of the chosen active component for the intended purposes. Once this verification point was successfully passed, the design process entered the second phase, which focused on designing the second stage of the LNA and configuring the LNA feedback. Through the creation of detailed schematics, accurate simulations using the AWR Microwave Office software, and the creation of a layout and PCB using the Altium Designer software, the final printed circuit was obtained. Detailed tests were performed on this circuit to ensure its effectiveness and desired performance.

### 4.4 First Stage Design

#### 4.4.1 Selection of the Active Component BFP740F

In the context of designing the first stage of our circuit, the initial focus was on identifying the optimal active component. With the aim of satisfying the specific requirements of the project, a thorough analysis was carried out to select the RF transistor. After careful evaluation of the available alternatives, the choice fell on low-noise RF transistors produced by Infineon. This selection was motivated by their design aimed at meeting the needs of applications that require low noise levels and high linearity. After examining the datasheets of various transistors and comparing their characteristics, two candidates emerged as the most promising: the BFP720 and the BFP740F, both SiGe wideband RF NPN heterojunction bipolar transistors. This selection was further supported by empirical laboratory tests and the noise power spectral density measurement graphs ( $A^2/Hz$ ) provided by Infineon (Figure 32 and Figure 33).

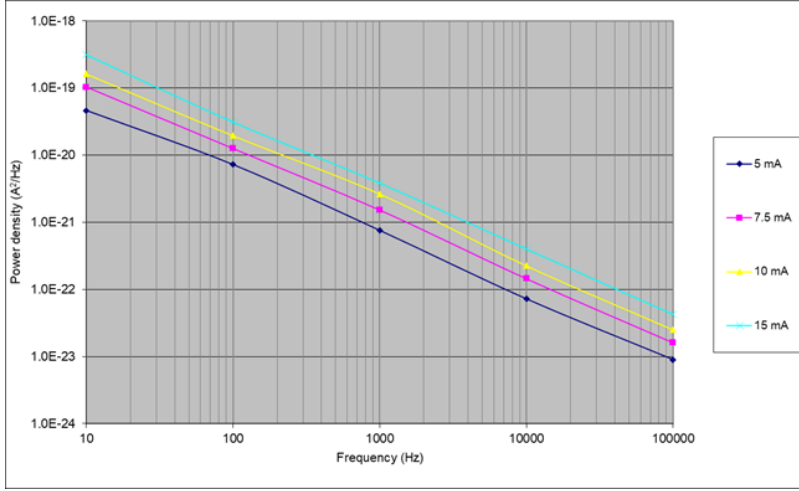


Figure 32: BFP720 Transistor Noise Power Spectral Density Measurements

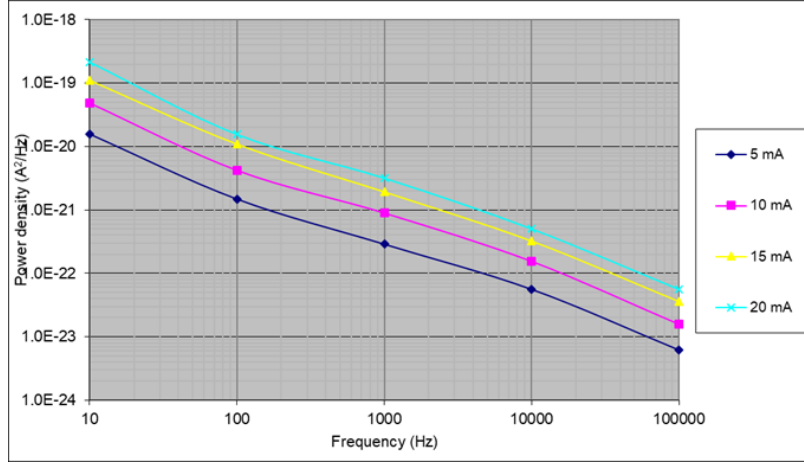


Figure 33: BFP740F Transistor Noise Power Spectral Density Measurements

Of the two selected devices, the BFP740F was preferred. A key factor driving this decision was the corner frequency ( $f_c$ ) of the flicker noise. This parameter represents the critical point at which flicker noise equals white noise. It was observed that the BFP740F has a lower corner frequency compared to the BFP720. A concrete example of this difference has been identified considering a current  $I_c$  of 5 mA. As can be seen from the Table 3, provided by Infineon, in the case of the BFP720, the

corner frequency is 64.9 kHz, whereas for the BFP740F, such frequency is 14.1 kHz.

| $I_c$ (mA) | $f_c$ (kHz) - BFP720 | $f_c$ (kHz) - BFP740F |
|------------|----------------------|-----------------------|
| 5          | 64.9                 | 14.1                  |
| 7.5        | 128.6                | 57.7                  |
| 10         | 210.7                | 138.8                 |
| 15         | 435.2                | 260.4                 |

Table 3: Extracted corner frequency values of BFP720 and BFP740F

This significant difference becomes even clearer by proceeding with the simulation of the noise figure of the first stage of the LNA, while keeping the current value constant. The comparative analysis of results obtained through simulation, shown in Figure 34, confirms that the BFP740F exhibits a remarkable ability to withstand the effects of flicker noise at low frequencies. Therefore, the substantial difference regarding corner frequencies and the demonstrated capability to preserve signal quality at low frequencies bestow a significant advantage on the BFP740F, thereby confirming the decision to use it in our project.

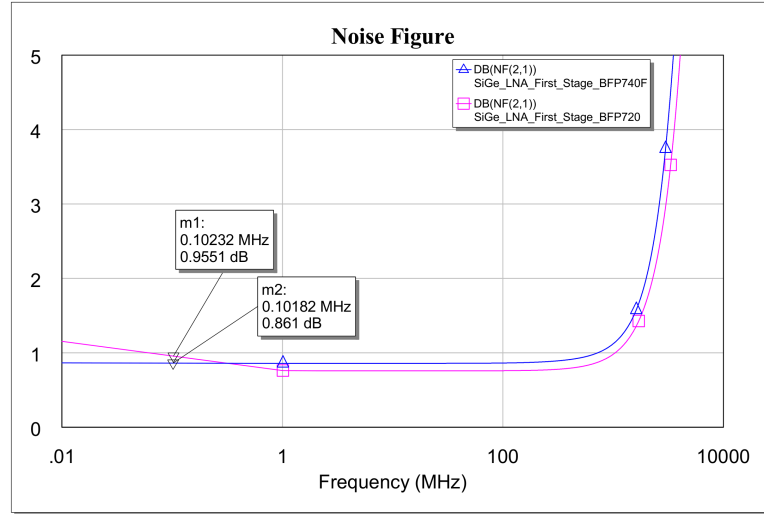


Figure 34: Noise Figure Comparison Plot - BFP720 vs. BFP740F

#### 4.4.2 Schematic and Simulations

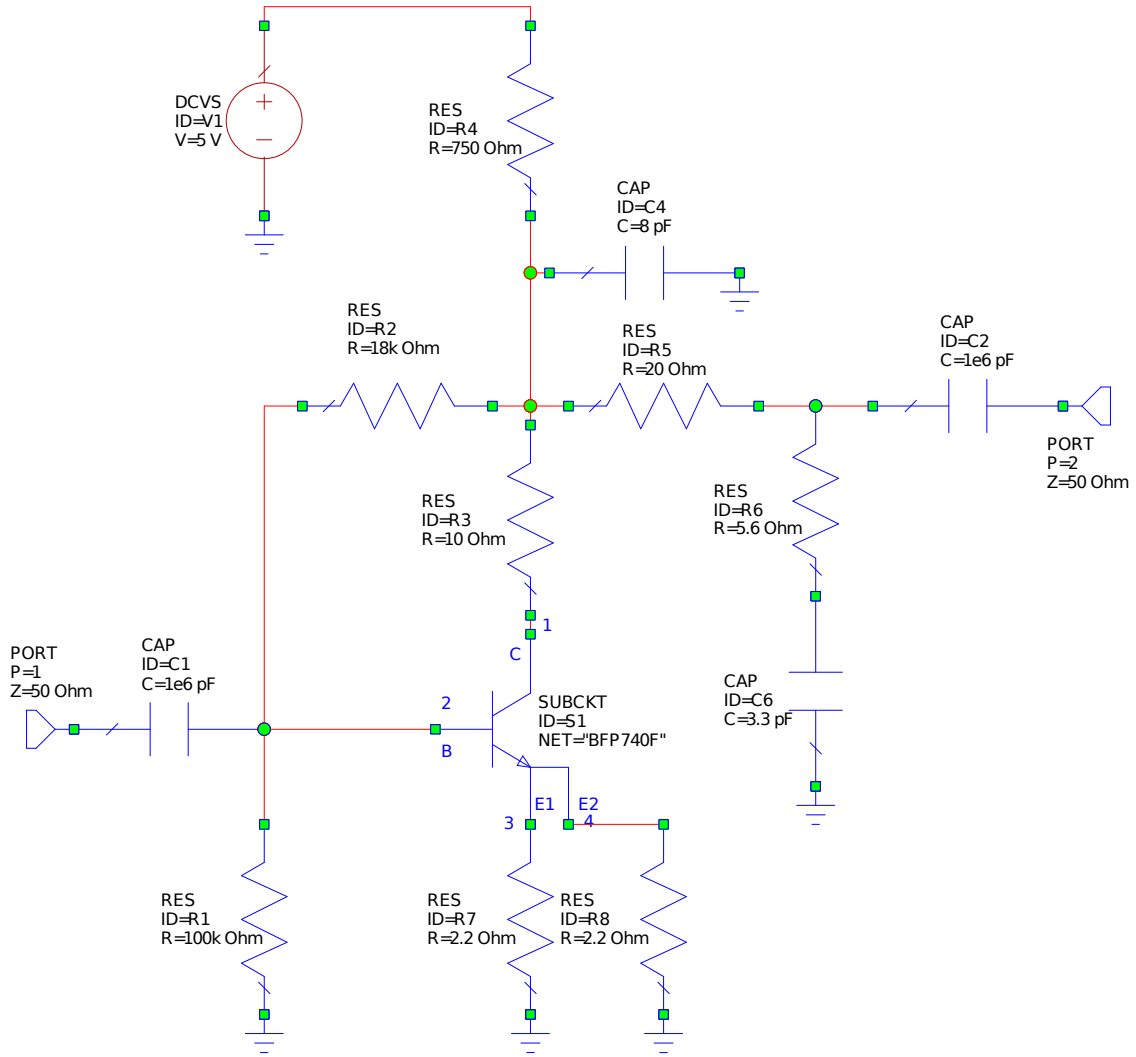


Figure 35: LNA First Stage Schematic

| Symbol | C1        | C2        | C4   | C6     | R1             | R2            | R3          | R4           | R5          | R6           | R7           | R8           |
|--------|-----------|-----------|------|--------|----------------|---------------|-------------|--------------|-------------|--------------|--------------|--------------|
| Value  | 1 $\mu$ F | 1 $\mu$ F | 8 pF | 3.3 pF | 100 k $\Omega$ | 18 k $\Omega$ | 10 $\Omega$ | 750 $\Omega$ | 20 $\Omega$ | 5.6 $\Omega$ | 2.2 $\Omega$ | 2.2 $\Omega$ |

Table 4: Component values



Figure 35 shows the initial configuration of the first stage of the LNA, highlighting its key components. In particular, this stage operates as a common-emitter amplifier. In order to ensure reliable transistor biasing, a strategic configuration of  $R_1$ ,  $R_2$  and  $R_4$  was adopted, which acts as a negative DC feedback mechanism. Specifically,  $R_1$  and  $R_2$  were designed as a voltage divider that controls the base voltage ( $V_B$ ) of the transistor. This voltage is regulated downstream of the collector resistor  $R_4$ . Consequently, if the collector current ( $I_C$ ) were to increase, this would result in a decrease in the voltage  $V_B$ , thus generating a stabilization of the working point of the transistor. Capacitor  $C_4$  and resistors  $R_3$  and  $R_5$  play a significant role in circuit stability, ensuring a K-factor greater than 1 for all frequencies. In particular, from the simulation point of view, it was observed that the inclusion of  $C_4$  and  $R_5$  results in a K-factor greater than 1 in the frequency range of 60 MHz to 4 GHz. This effect is clearly illustrated in Figure 36, where it is evident that the omission of these two components results in instability ( $K < 1$ ). Moreover, it was found that resistor  $R_3$  plays a similar role at a frequency of 8 GHz, as illustrated in Figure 37. Finally, the network  $R_6$  and  $C_6$  was added to the circuit. This element, introducing a pole, will prove advantageous to cut the amplifier band.

In general, the voltage gain of a common-emitter amplifier is given by:

$$A_v \triangleq \frac{v_{out}}{v_{in}} = -\frac{g_m R_c}{g_m R_E + 1} \quad (57)$$

But when  $g_m R_E \gg 1$ , the voltage gain can be approximated as:

$$A_v \simeq -\frac{R_C}{R_E} \quad (58)$$

It is evident that decreasing the emitter resistor  $R_E$  results in an increase in gain. In fact, in general, the resistor present in the emitter is typically used to ensure the stability of the circuit operating point, but it is then bypassed through the use of a capacitor. In our context, contrary to this common practice, maintenance of the stable operating point is achieved through a feedback system between the base and the collector. However, the emitter resistor ( $R_E = R_7 \parallel R_8$ ) is still included, since later it will be involved in a feedback loop aimed to stabilize the gain of the LNA.

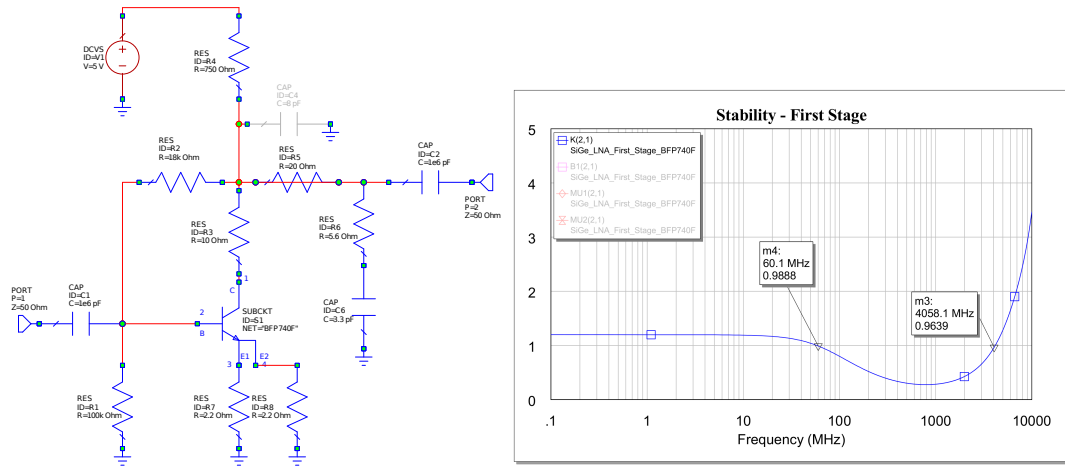


Figure 36: First Stage Instability from 60 MHz to 4 GHz with  $C_4$  removed and  $R_5$  short circuited

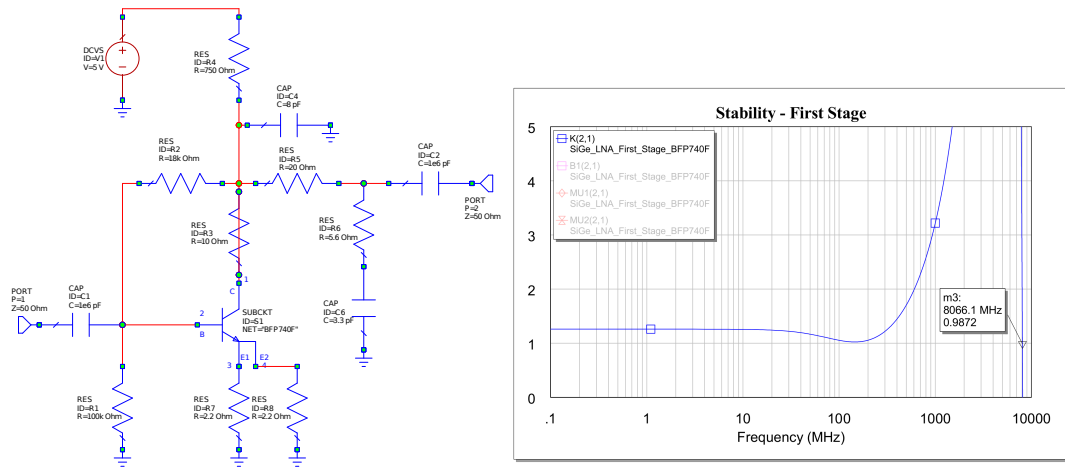


Figure 37: First Stage Instability at 8 GHz with  $R_3$  short circuited

Once the first stage topology was selected, we focused on choosing component values. This phase was strongly supported by an iterative simulation process using the AWR Microwave Office. Through this software, we tuned the values of the components in a systematic way, allowing us to progressively improve the performance of the circuit. In the context of the first stage, we have focused our attention on several aspects. First of all, we made sure that the transistor draws a current of about 6 mA, in line with the indications of the datasheet. We also aimed for a power gain ( $S_{21}$ ) of around 20 dB, a noise figure (NF) below 1 dB and a K-factor greater than 1. The iterative approach in the simulation has allowed us to obtain a configuration that adequately satisfies the various specifications. In fact, the results obtained from the simulations are the following:

|                         |           |
|-------------------------|-----------|
| Collector Current $I_C$ | 6 mA      |
| Power Gain $S_{21}$     | 21.67 dB  |
| Noise Figure $NF$       | 0.9414 dB |

Table 5: Simulation results summary

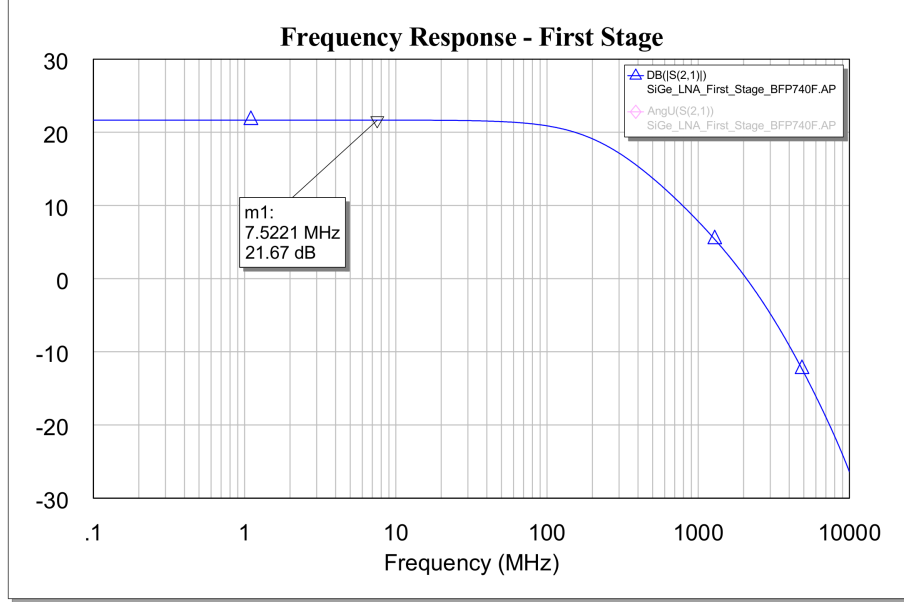


Figure 38: First Stage Gain Plot

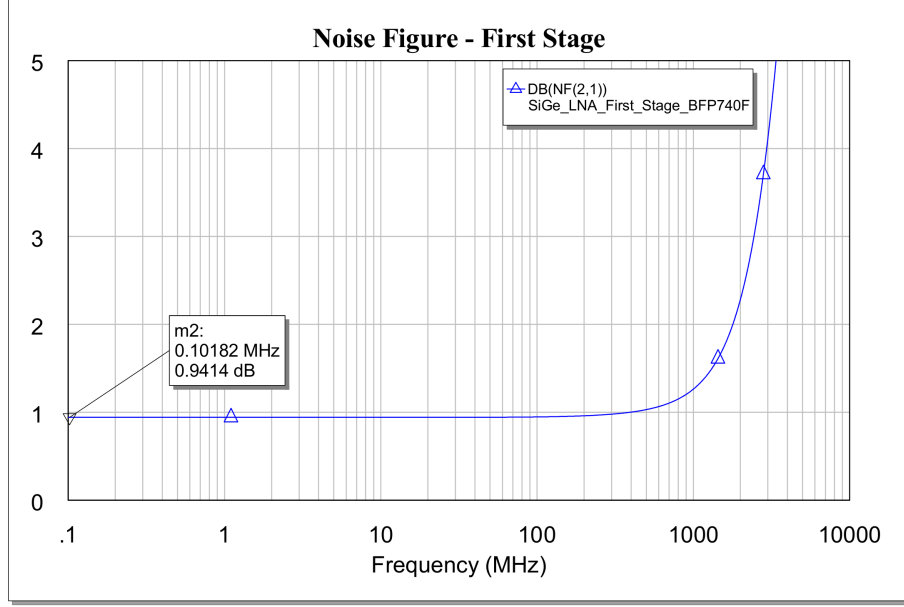


Figure 39: First Stage Noise Figure Plot

The determining criterion for stability is the K-factor, which was found to be greater than 1 over the entire frequency range, confirming the unconditional stability of the circuit. However, there are also other criteria for assessing the unconditional stability of a circuit [19]:  $\mu_1$  (geometric stability factor - load), which quantifies the distance from the center of Smith Chart to the nearest unstable point on the output stability circle (center  $C_L$ , radius  $\Gamma_L$ ) and  $\mu_2$  (geometric stability factor - source), which does the same for the input stability circle (center  $C_S$ , radius  $\Gamma_S$ ). In order to shift out of the Smith Chart the point of instability, it is desirable that both of these parameters are greater than 1. Another index that evaluates stability is B1 (auxiliary stability factor), which must necessarily be greater than 0. The results of our simulations, illustrated in Figure 40, show that all of these parameters satisfy the necessary conditions to confirm the unconditional stability of the system.

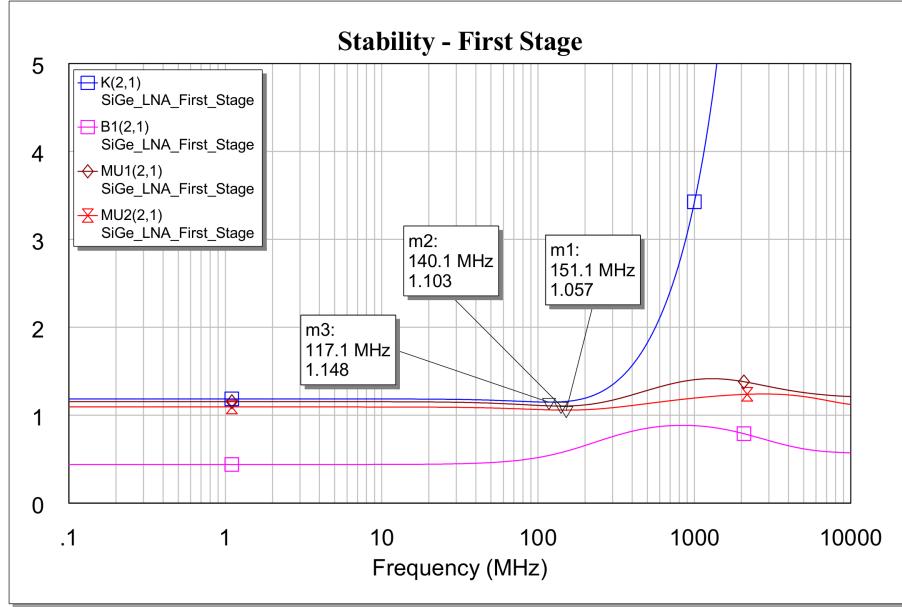


Figure 40: First Stage Unconditional Stability Plot

Before starting the printed circuit board (PCB) design phase, it was deemed essential to perform detailed simulations in order to obtain a more realistic analysis of the circuit. In particular, it was decided to incorporate models based on real components, including capacitors from the Murata library. This methodology allowed us to acquire a more complete understanding of the effect of these components on the overall performance of the system. In our study, we performed an analysis of the behavior of the impedance of a 1  $\mu\text{F}$  multilayer ceramic capacitor available in the Murata library. The modulus of the impedance, represented in Figures 41 and 42, reveals a series resonance phenomenon at 8 MHz. This particular behavior implies that beyond this frequency, the capacitor takes on an impedance of an inductive nature. Consequently, its effectiveness as a bypass element is compromised. To overcome this limitation, a capacitor of lesser value, equal to 100 pF, is adopted. This capacitor retains its capacitive nature even at much higher frequencies; in fact, it exhibits a series resonance at 646 MHz, thus preserving the bypass functionality.

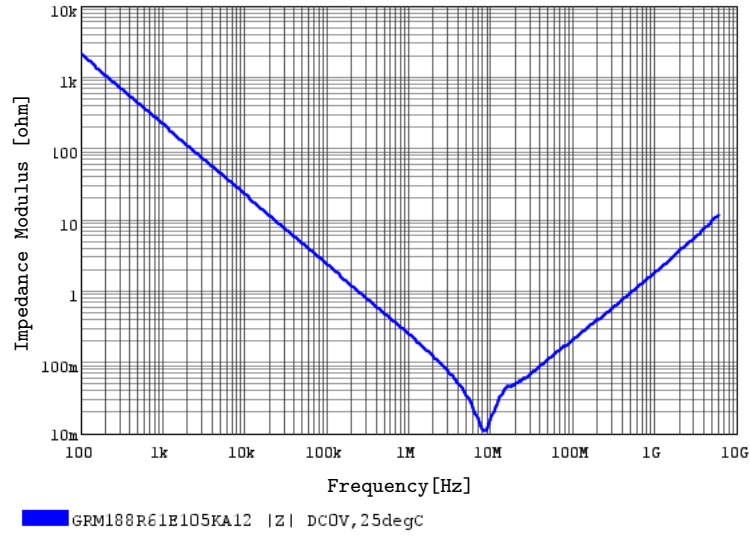


Figure 41: Modulus of the impedance vs. frequency for 1  $\mu$ F Murata Capacitor

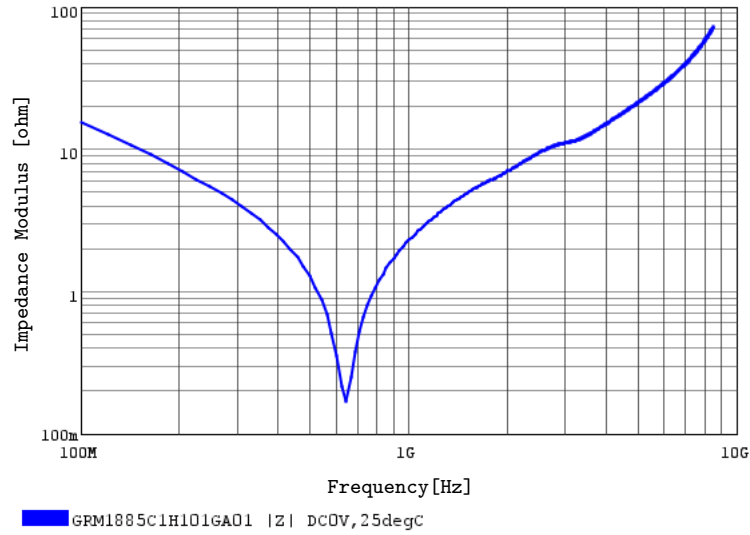


Figure 42: Modulus of the impedance vs. frequency for 100 pF Murata Capacitor

Consequently, simulations were run to compare the performance of a circuit including exclusively ideal components and one featuring real Murata capacitors and via

models, as shown in Figure 43. This was done in order to detect and analyze any significant discrepancies in circuit performance. In particular, the type of via used is a cylindrical one port via with microstrip pad. The parameters related to this via, such as hole diameter  $D$  equal to 0.5 mm and pad width  $W$  equal to 0.5 mm have been sized according to the values outlined in the PCB layout.

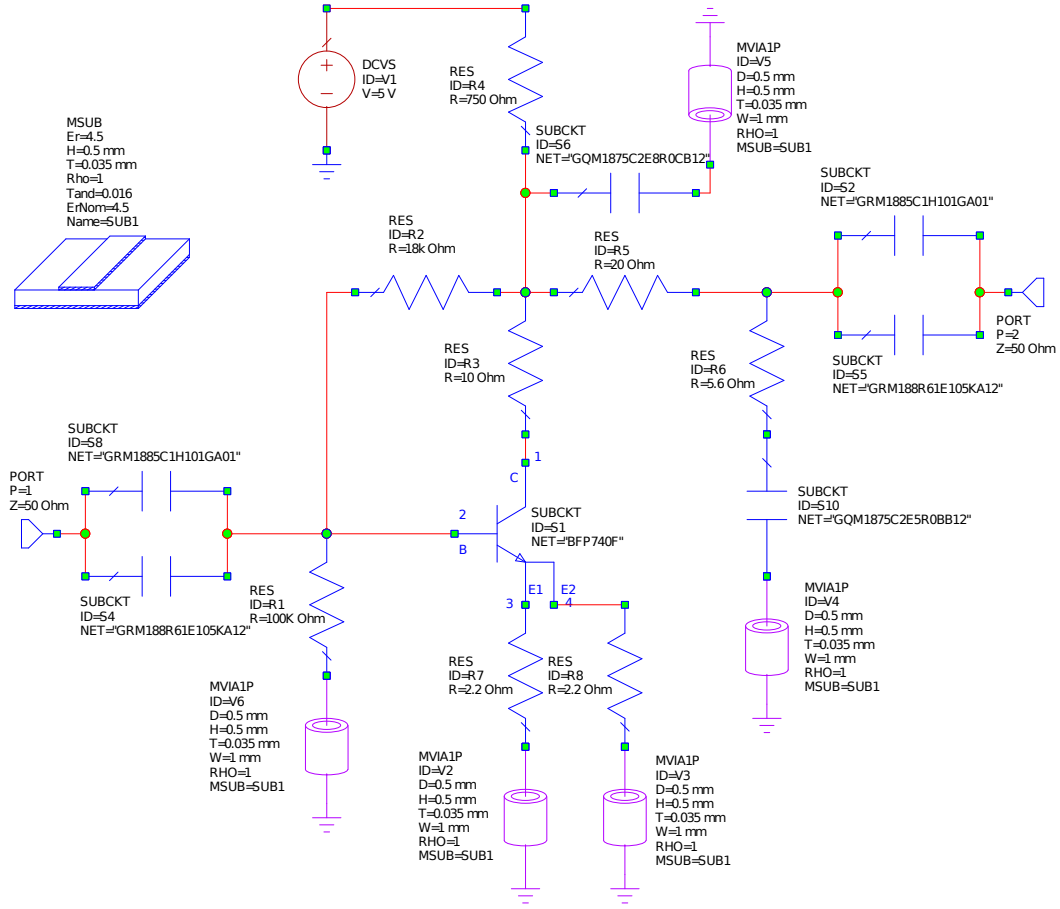


Figure 43: LNA First Stage Schematic - Murata Capacitors

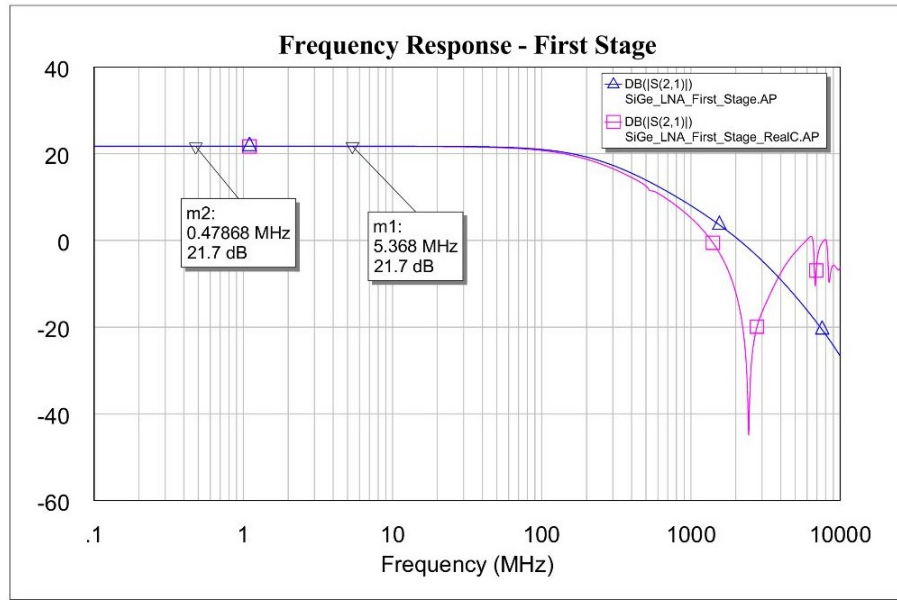


Figure 44: Gain comparison - Ideal Capacitors vs. Murata Capacitors

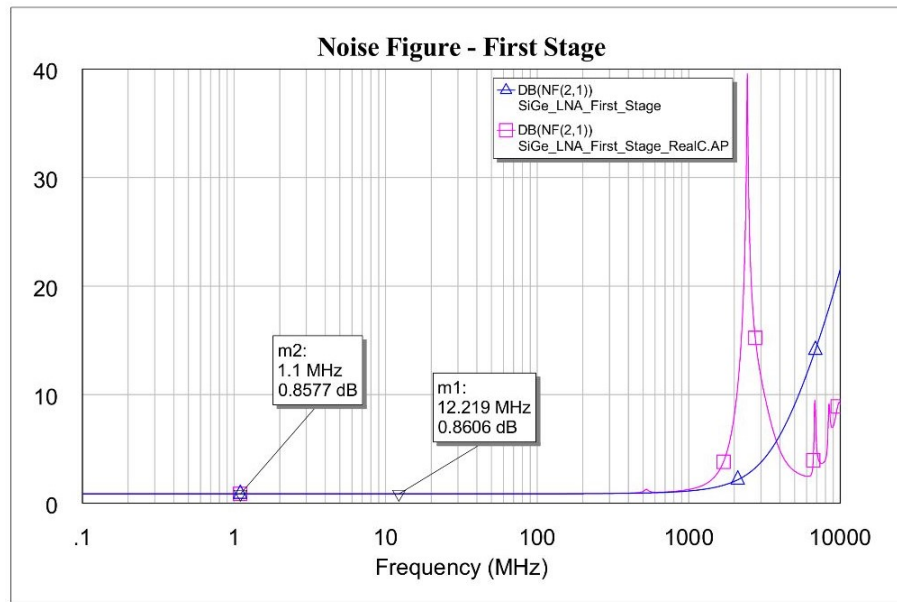


Figure 45: Noise Figure comparison - Ideal Capacitors vs. Murata Capacitors



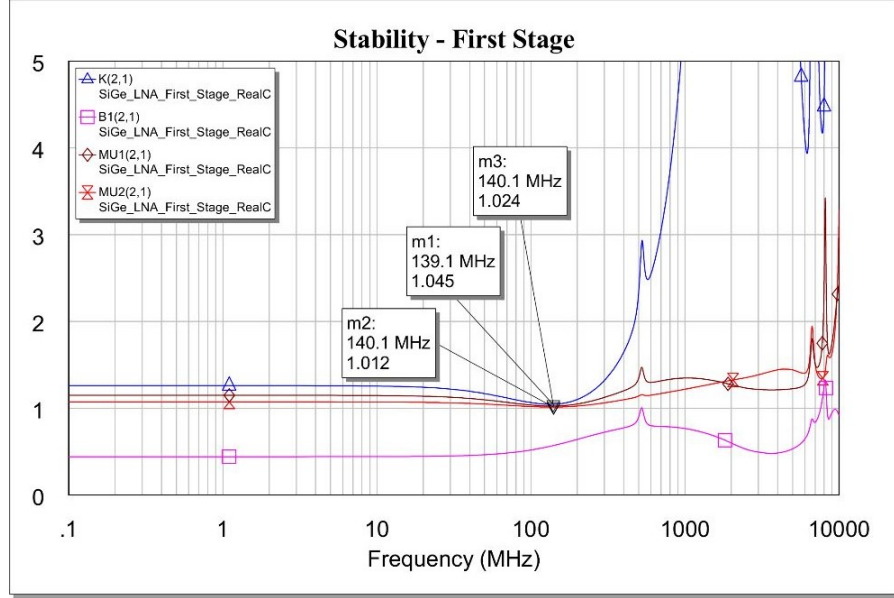


Figure 46: First Stage Unconditional Stability Plot - Murata Capacitors

From the plots shown in the figures above, it is clear that the differences in the gain, noise figure and stability parameters are negligible within the useful bandwidth, without exerting a significant impact on the overall operation of the circuit. Therefore, the strategy adopted to deal with the undesirable effect introduced by the non-ideality of the 1  $\mu$ F ceramic capacitor appears to be effective. Overall, despite the introduction of non-ideal components, the results of the simulations remain in line with our expectations.

#### 4.4.3 Printed Circuit Board

We used the Altium Designer software to develop the first stage board. Our approach resulted in the creation of a 4-layer PCB with dimensions 4 cm  $\times$  4 cm, carefully designed to maximize the performance of the LNA. This optimization was achieved through a scrupulous layout selection among the standard options offered by Eurocircuits and a meticulous arrangement of the components in the layout. The 4-layer PCB architecture features a central layer surrounded by two thinner prepreg layers. This design was chosen because it optimizes power distribution and signal

integrity. The outer layers serve a dual purpose: to accommodate signal routing and to connect the components, such as surface-mount devices (SMD), connectors, and other circuit elements. This arrangement minimizes the length of the signal path, thus reducing the risk of interference and attenuation. On the other hand, the inner layers are dedicated to a solid ground plane and to power distribution. This approach provides a low-impedance path for stable power distribution, reducing noise and helping to maintain excellent signal integrity. Thoughtful planning of a solid ground plane is critical to prevent impedance mismatch, crosstalk problems, electromagnetic interference (EMI), and to ensure good ground connectivity.

| # | Name           | Material      | Type        | Weight | Thickness | Dk  | Df    |
|---|----------------|---------------|-------------|--------|-----------|-----|-------|
|   | Top Overlay    |               | Overlay     |        |           |     |       |
|   | Top Solder     | Solder Resist | Solder Mask |        | 0.01mm    | 3.5 |       |
| 1 | Top Layer      |               | Signal      | 1oz    | 0.035mm   |     |       |
|   | Dielectric 2   | PP-006        | Prepreg     |        | 0.18mm    | 4.1 | 0.016 |
|   | Dielectric 4   | PP-006        | Prepreg     |        | 0.18mm    | 4.1 | 0.016 |
| 2 | Layer 1        | CF-004        | Plane       | 1oz    | 0.035mm   |     |       |
|   | Dielectric 1   | FR-4          | Core        |        | 0.71mm    | 4.5 |       |
| 3 | Layer 2        | CF-004        | Plane       | 1oz    | 0.035mm   |     |       |
|   | Dielectric 5   | PP-006        | Prepreg     |        | 0.18mm    | 4.1 | 0.016 |
|   | Dielectric 3   | PP-006        | Prepreg     |        | 0.18mm    | 4.1 | 0.016 |
| 4 | Bottom Layer   |               | Signal      | 1oz    | 0.035mm   |     |       |
|   | Bottom Solder  | Solder Resist | Solder Mask |        | 0.01mm    | 3.5 |       |
|   | Bottom Overlay |               | Overlay     |        |           |     |       |

Figure 47: PCB Layer Stack-Up

The representation of this structural arrangement is shown in Figure 47, which illustrates the layer stack-up of the PCB comprehensively. Both between the top layer and layer 1, and between layer 2 and the bottom layer, the PP-006 prepreg is used as a dielectric, with the relative dielectric constant  $D_k$  equal to 4.1 and the loss tangent of dielectric  $D_f$  equal to 0.016. This material is advantageous because of its dielectric properties that favor signal propagation and insulation between layers. In the central area of the PCB, between layer 1 and layer 2, FR-4, with relative dielectric constant  $D_k$  of 4.5 and the loss tangent of dielectric  $D_f$  equal to 0.02, was used. This design approach reflects careful planning in the printed circuit board design, with the goal of maximizing the overall amplifier performance and minimizing any potential negative impacts. Figures 48 and 49 provides a comprehensive representation of the schematic and PCB, offering a clear understanding of the component layout and the

connecting traces within the board. It is important to note that the illustration also includes the detailed diagram of the voltage stabilizer based on a transistor. The choice of this stabilizer compared to integrated solutions was made because it proved more suitable for the high-radiation environment in which the device will be placed.

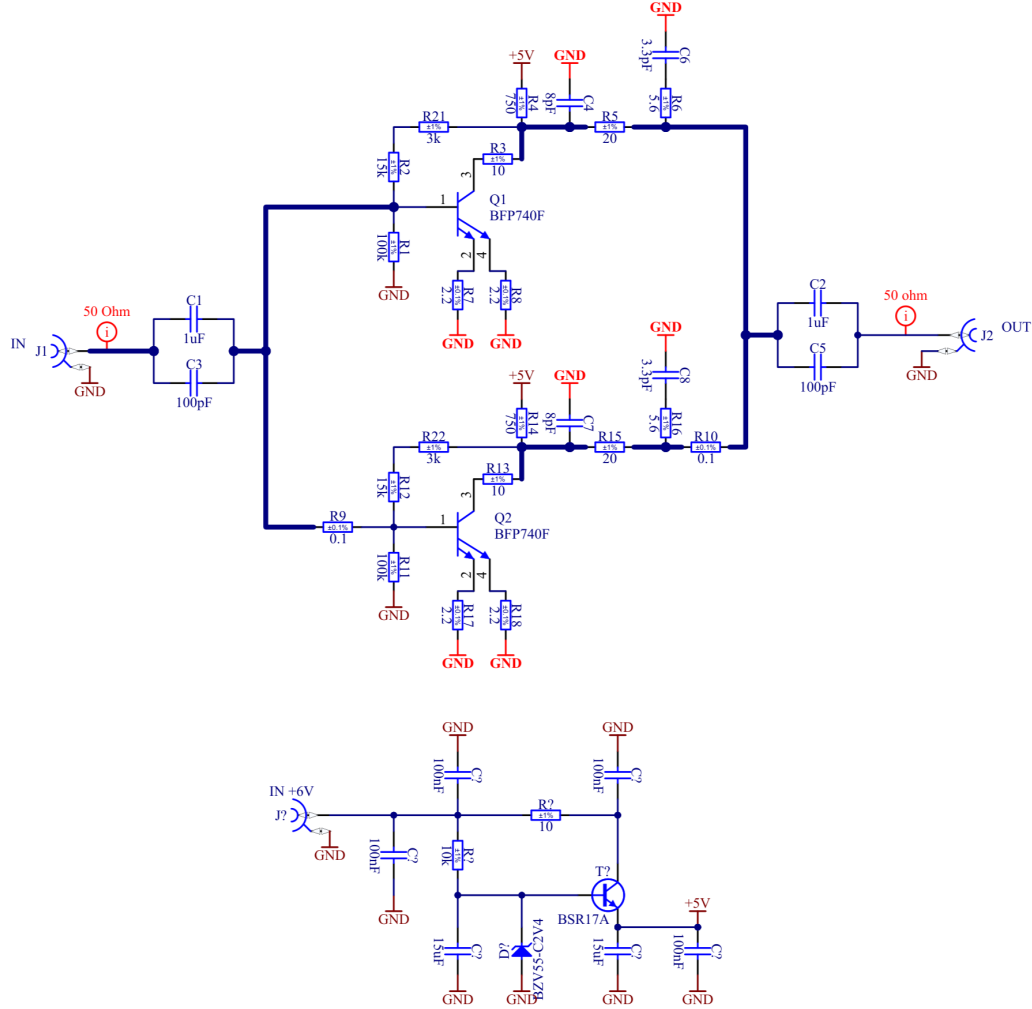


Figure 48: LNA First Stage PCB Schematic

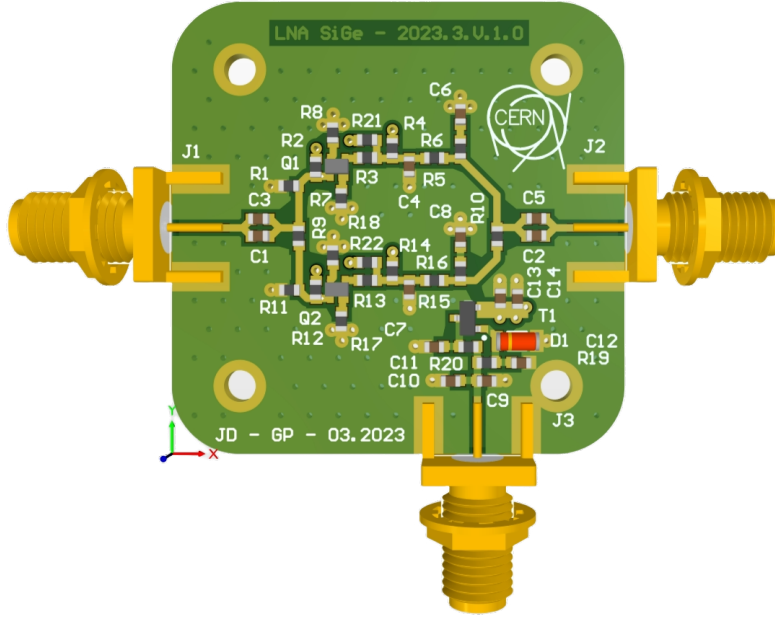


Figure 49: LNA First Stage PCB

#### 4.4.4 Outcomes of the First Stage Prototype Testing

In the ending phase of the first stage development process, we conducted rigorous testing of the prototype, revealing significant challenges related mainly to circuit stability. In particular, we encountered circuit instability problems due to parasitic effects which, in the simulation phase, could not be taken into account. However, thanks to a well-planned empirical approach, it was possible to address these issues efficiently. In parallel with the execution of laboratory tests, detailed simulations were performed to analyze the system behavior under various conditions. This synergistic approach between simulations and tests enabled the identification of weaknesses in the prototype and the iterative development of improvement solutions, ultimately leading to the optimized configuration for the first stage as shown in Figure 50.

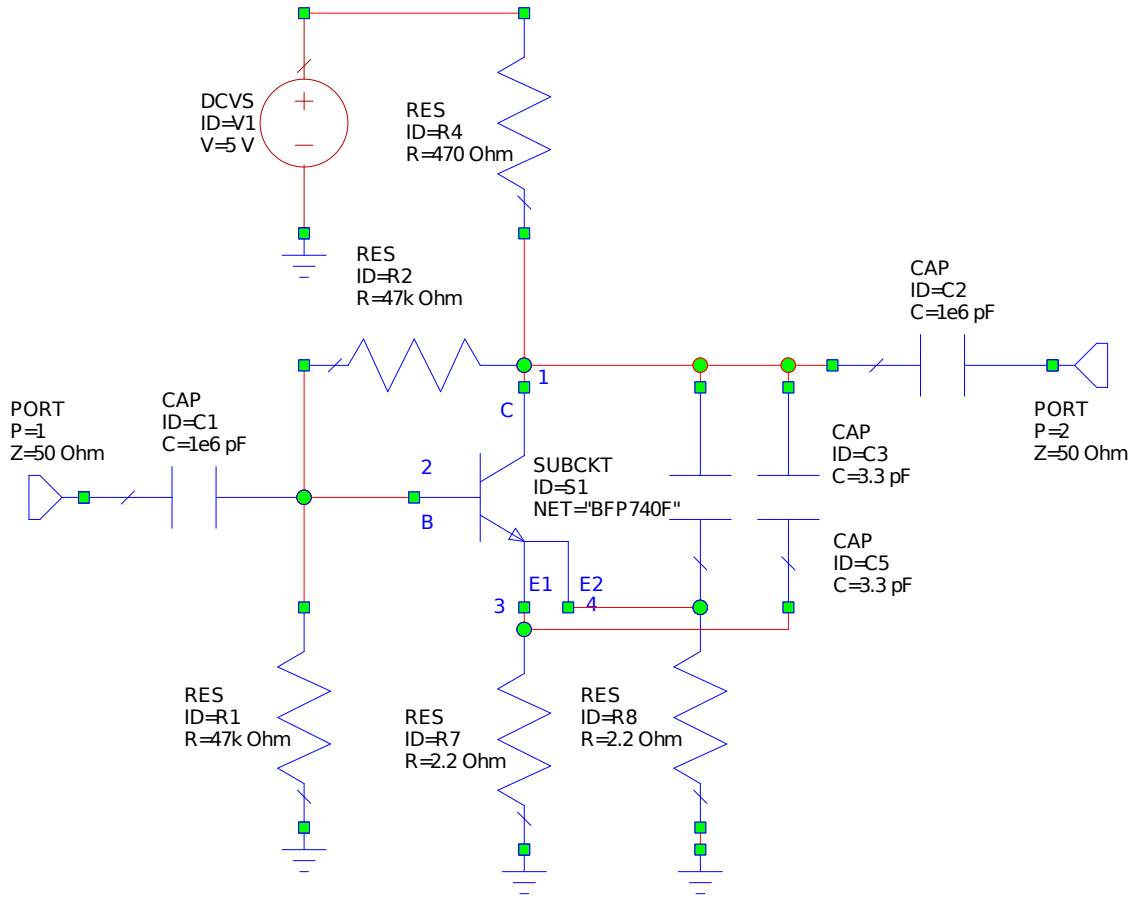


Figure 50: First Stage Optimized Schematic

| Symbol | C1        | C2        | C3     | C5     | R1            | R2            | R4           | R7           | R8           |
|--------|-----------|-----------|--------|--------|---------------|---------------|--------------|--------------|--------------|
| Value  | 1 $\mu$ F | 1 $\mu$ F | 3.3 pF | 3.3 pF | 47 k $\Omega$ | 47 k $\Omega$ | 470 $\Omega$ | 2.2 $\Omega$ | 2.2 $\Omega$ |

Table 6: Optimized Component Values

To specifically address the issues related to bandwidth and oscillations, a solution based on implementing a compensation with the addition of capacitors to the circuit was implemented. Specifically, two 3.3 pF capacitors were added, connected from the collector to the emitter. These capacitors were strategically placed to limit the

system bandwidth and prevent undesirable oscillations. The tests and simulation results are presented in the following figures.

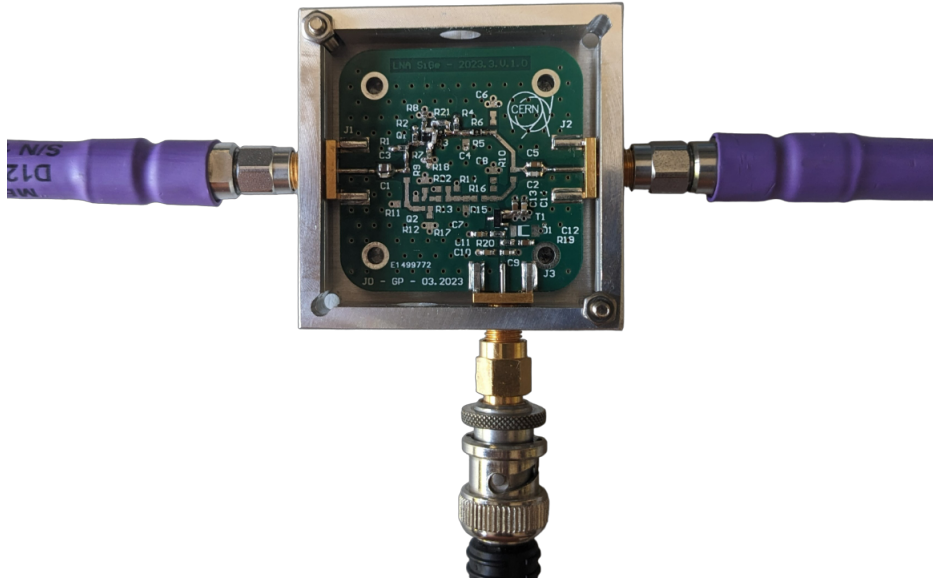


Figure 51: First Stage Board

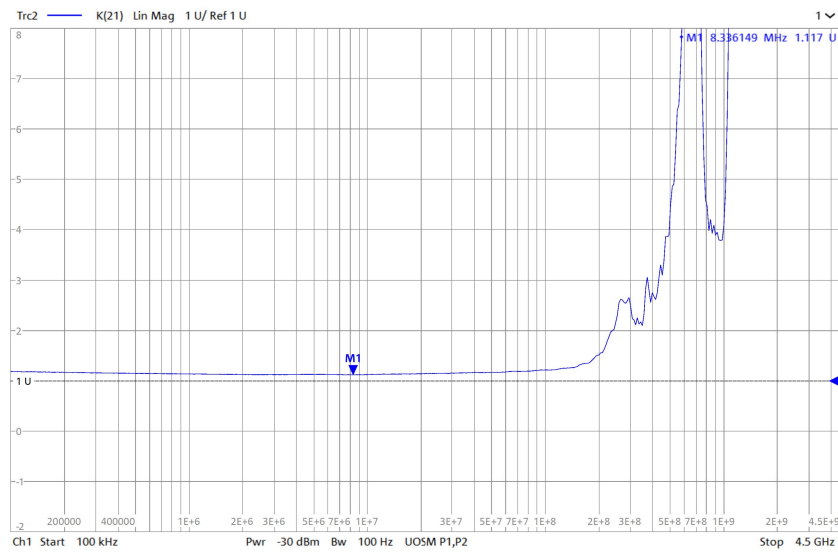


Figure 52: First Stage K-factor Measurement

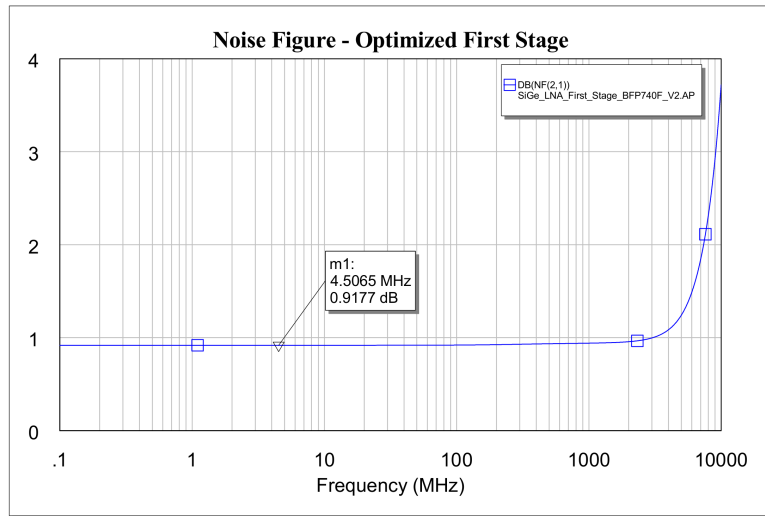


Figure 53: First Stage Noise Figure Simulation Result

| Frequency (MHz) | NF (dB) |
|-----------------|---------|
| 1               | 1.141   |
| 3               | 1.116   |
| 5               | 1.109   |
| 7               | 1.017   |
| 10              | 0.965   |
| 13              | 0.985   |
| 15              | 0.964   |
| 17              | 0.902   |
| 20              | 0.927   |
| 25              | 0.911   |
| 30              | 0.903   |

Table 7: First Stage Noise Figure Measurement

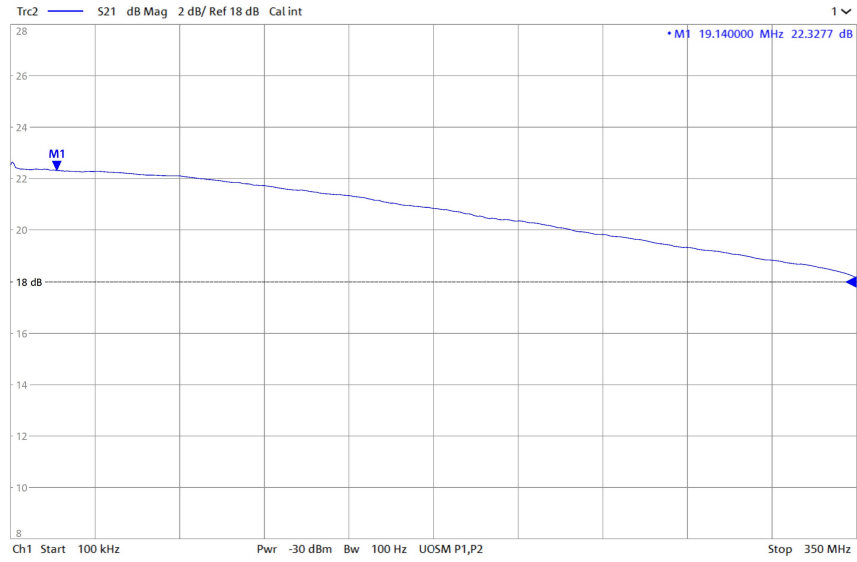


Figure 54: First Stage Gain Measurement

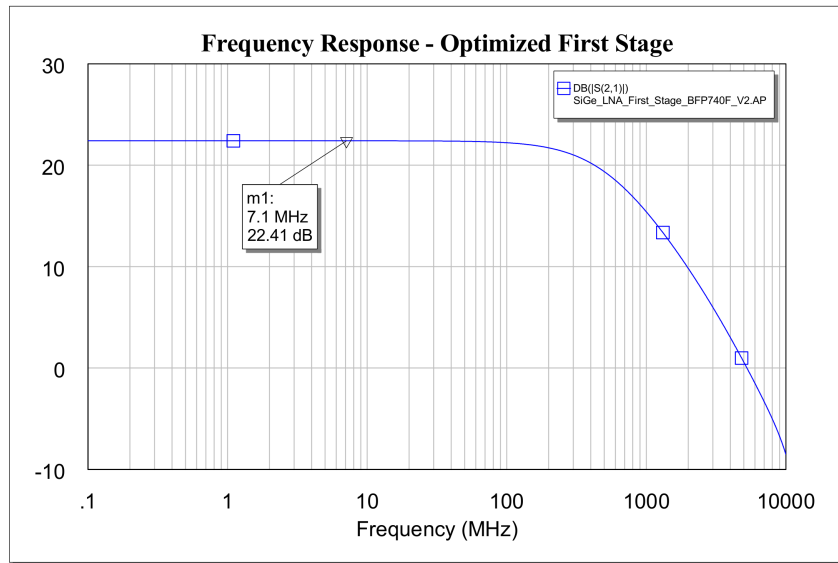


Figure 55: First Stage Gain Simulation Result

As we can see, the system is unconditionally stable (52), provides a noise figure of approximately 0.9 dB (7) and a gain of 22.4 dB (54). These results are very close to those obtained in simulation.



## 4.5 Second Stage and Feedback Design

For the implementation of the second stage of the Low-Noise Amplifier, we used the LMH6629 operational amplifier in a 3 mm x 3 mm WSON-8 package. This amplifier, fabricated using Silicon Germanium (SiGe) technology, stands out for its high-speed performance, low noise, and wide bandwidth. Thanks to the combination of these features, the LMH6629 proved to be an ideal choice for ensuring high amplification in the second stage of the LNA, without compromising the system noise level.

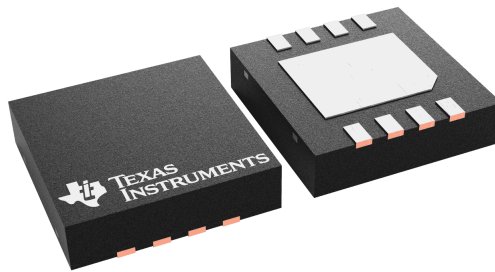


Figure 56: LMH6629 - WSON (8) Package

The operational amplifier (Op Amp) configuration illustrated in Figure 57 operates in the non-inverting amplifier mode. In this mode, the voltage gain is defined by the following relationship, as outlined in [20]:

$$A_v = 1 + \frac{R_{15}}{R_{12} \parallel R_{13}} \quad (59)$$

In order to achieve a voltage gain of approximately 26 dB, a value of 150  $\Omega$  was chosen for the resistors  $R_{12}$  and  $R_{13}$ , while the value of 1500  $\Omega$  was chosen for the resistor  $R_{15}$ .

$$A_v|_{dB} = 20 \log \left( 1 + \frac{1500}{75} \right) = 20 \log(21) = 26.4 \text{ dB} \quad (60)$$

Moreover, considering that the LMH6629 operational amplifier has a cutoff frequency at 900 MHz, we have strategically incorporated a 1 pF capacitor in parallel with the

feedback resistor to create a pole at 106.1 MHz, as indicated by equation (61). This pole significantly influences the overall circuit response, allowing us to limit the bandwidth to the value of interest:

$$f_p = \frac{1}{2\pi R_{15}C_{15}} \simeq 106.1 \text{ MHz} \quad (61)$$

Since the operational amplifier needs a dual power supply and we preferred not to introduce a negative voltage power supply just for the Op Amp, we have created a virtual ground reference with the power supply partition between  $R_{12}$  and  $R_{13}$ , as well as between  $R_9$  and  $R_{10}$ .

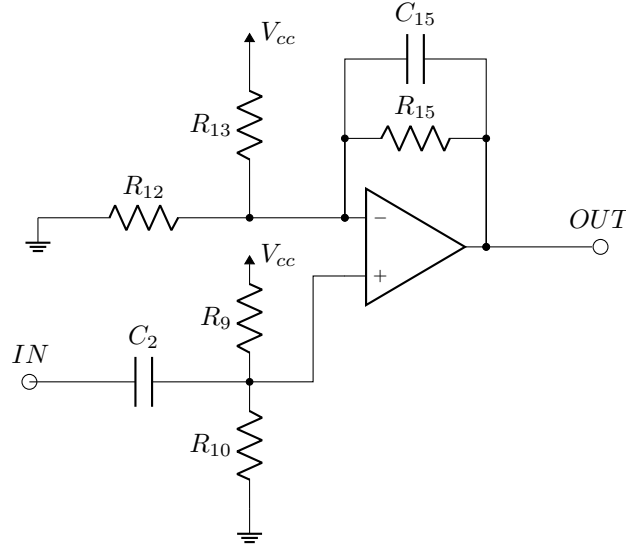


Figure 57: Non-Inverting Op Amp Configuration

### 4.5.1 Series-Shunt Feedback

A critical aspect of the design phase of a Low-Noise Amplifier is the stability of its gain. This aspect plays a fundamental role for various reasons, each of which has a significant impact on the overall system performance. Fluctuations in the amplifier gain can have direct consequences on the sensitivity of the entire system, influencing its ability to detect weak signals. Furthermore, it is important to emphasize that a change in gain could alter the amplifier noise figure, disrupting the quality of the amplified signal. Another reason to pay particular attention to gain stability is the influence that environmental factors, such as temperature, can have on the overall amplifier performance. Thermal variations can cause fluctuations in the LNA parameters, compromising its performance in unpredictable ways. Therefore, ensuring gain stability is a critical factor in ensuring the system robustness against changing environmental conditions. Based on these considerations, the approach adopted in our project has been carefully directed towards implementing a targeted control strategy aimed at gain stabilization. In particular, a series-shunt feedback approach has been adopted, which has proven highly effective in balancing and controlling gain fluctuations. This methodology acts as a control mechanism that constantly monitors the amplifier gain and makes real-time corrections to maintain the gain at the desired value. This choice has demonstrated to be particularly suitable for preserving the system integrity even in dynamic and changing contexts, ensuring a wide tolerance to parameter variations and guaranteeing reliable performance over time.

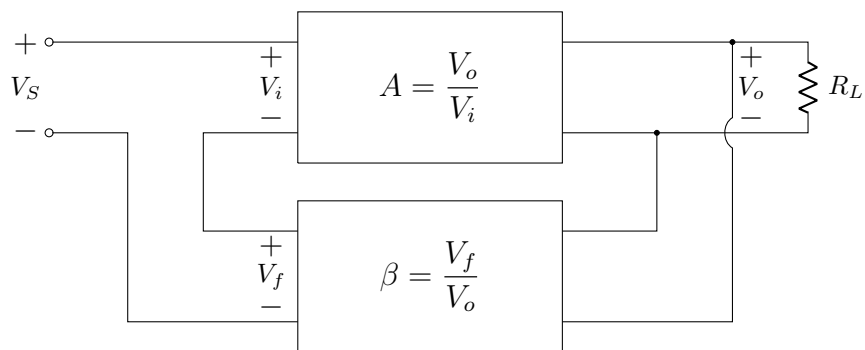


Figure 58: Series-Shunt Feedback

The block diagram depicted in Figure 58 illustrates the configuration of a series-shunt feedback. In this circuit a fraction of the output voltage is applied in series with the input voltage through the feedback loop. Hence, we can express the source voltage  $V_s$  as the combination of the input voltage  $V_i$  and the feedback voltage  $V_f$ :

$$V_s = V_i + V_f \quad (62)$$

Considering that the feedback voltage  $V_f$  is given by the product of the output voltage  $V_o$  and the feedback factor  $\beta$ , and that  $V_o$  is determined by the product of the gain  $A$  (gain of a voltage amplifier) and the input voltage  $V_i$ , we can write:

$$V_s = V_i + \beta V_o = V_i + \beta A V_i = \frac{V_o}{A} (1 + \beta A) \quad (63)$$

Hence, we obtain that closed-loop gain  $A_f$  is:

$$A_f = \frac{V_o}{V_s} = \frac{A}{1 + \beta A} \quad (64)$$

In our specific case, as can be seen in Figure 59, the network with voltage gain  $A$  consists of the cascade of the common emitter amplifier, with voltage gain  $A_1$ , and the Op Amp, with voltage gain  $A_2$ . The feedback network  $\beta$ , instead, consists of an RF transformer with turns ratio equal to 1 (1:1), a resistance  $R_{F1}$ , and decoupling capacitors. It should be noted that the presence of the transformer, which introduces a phase inversion in the gain, together with feeding the feedback signal into the emitter of the first stage, and the Op Amp configured in non-inverting mode, converge to create a negative feedback effect. The RF transformer used is the ADT1-1 of Mini Circuits which operates on a frequency range from 0.15 MHz to 400 MHz..

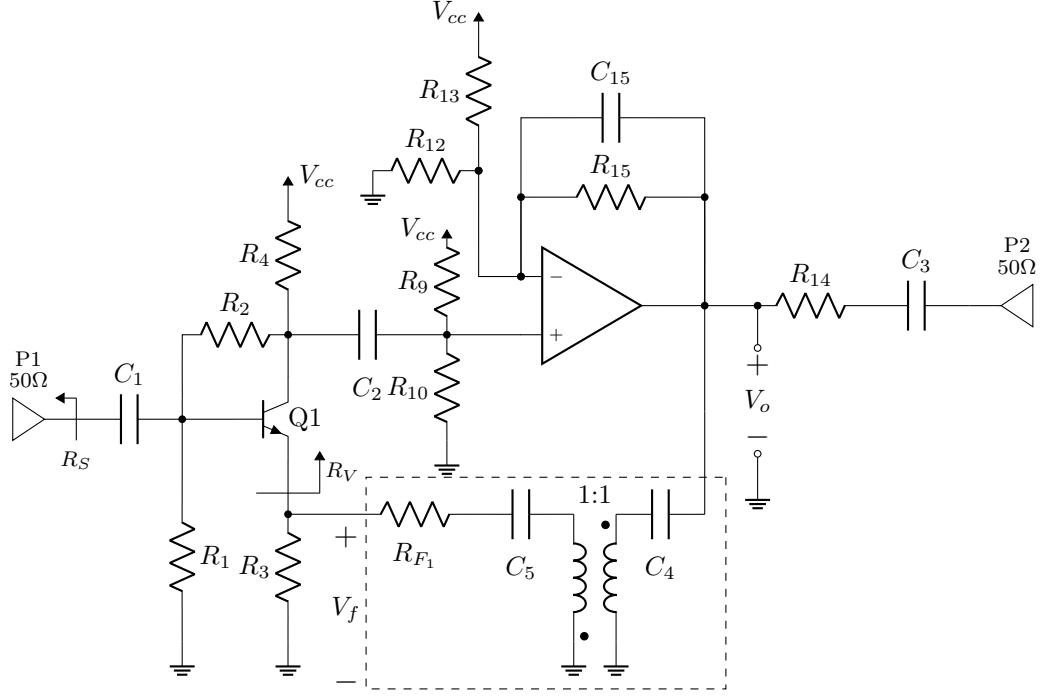


Figure 59: Series-Shunt Feedback in LNA Design

- Feedback Factor:

$$\beta = \frac{V_f}{V_o} = -\frac{R_3 \parallel R_V}{(R_3 \parallel R_V) + R_{F1}} = -0.01689 \quad (65)$$

Where:

$$R_V = \frac{h_{fe} R_B R_C + R_2 R_B + R_C R_B + h_{ie} (R_2 + R_C + R_B)}{(R_2 + R_C + R_B)(1 + h_{fe})} \quad (66)$$

$$R_B = R_1 \parallel R_S = 49.95 \Omega \quad (67)$$

$$R_C = R_4 \parallel R_9 \parallel R_{10} = 45.19 \Omega \quad (68)$$

Considering the following limiting case:

$$\lim_{R_2 \rightarrow \infty} R_V \simeq \frac{R_B + h_{ie}}{(1 + h_{fe})} \simeq 4.515 \Omega \quad (69)$$

- Loop Gain:

$$\beta A \simeq -\frac{R_3 // R_V}{(R_3 // R_V) + R_{F1}} (A_1 A_2) = 27.783 \quad (70)$$

Where:

$$A_1 \simeq -3.92 \quad A_2 = 21 \quad (71)$$

- Closed-loop Gain:

$$A_f = \frac{A}{1 + \beta A} \simeq \frac{(A_1 A_2)}{1 + \left( -\frac{R_3 // R_V}{(R_3 // R_V) + R_{F1}} \right) (A_1 A_2)} = -34.44 \quad (72)$$

$$|A_f|_{\text{dB}} = 20 \log (|-34.44|) \simeq 31 \text{ dB} \quad (73)$$

Considering both the Op Amp ability to drive an approximate  $100 \Omega$  load and the maximum achievable gain of approximately 44 dB across the two-stage cascade, and taking into account the impact of this gain on the input resistance of the LNA, the resistances  $R_{F1}$  and  $R_3$  have been carefully selected. They have been valued at  $150 \Omega$  and  $6 \Omega$  respectively. Specifically, the feedback resistance  $R_{F1}$  cannot be further reduced as it would lead to an excessive load reduction on the Op Amp. Therefore, while the optimal choice would be to keep the emitter resistance ( $R_3$ ) as low as possible to minimize noise and maximize gain, a more balanced decision must be made. This decision considers the need to maintain adequate gain by factoring in the effect of this gain on the input impedance. Therefore, an emitter resistor with a value slightly higher than the ideal value was chosen. This choice led to simulation results showing a stable gain at a value of 32 dB, which is close to the result expected from theoretical calculations of 31 dB.

### 4.5.2 Shunt-Shunt Feedback

In the design of the Low-Noise Amplifier, two highly relevant aspects to consider are input and output matching and minimum noise figure. In particular, input and output matching play a crucial role in optimizing power transfer from the source to the amplifier input and from the amplifier output to the load, in order to prevent phenomena such as reflections and signal losses. Referring to equations (16) and (17), it becomes evident that the reflection coefficient at the input becomes zero when the input impedance of the amplifier matches that of the source. Similarly, the reflection coefficient at the output becomes zero when the output impedance of the LNA is equal to that of the load. In our context, as illustrated in Figure 60, the LNA input is connected to the pick-up via a 5-meter coaxial cable with a characteristic impedance of  $50\ \Omega$ . The presence of the coaxial cable is determined by the need to position the entire electronics of the BPM system in an area characterized by a lower radiation level than that in which the pick-up is located. Consequently, despite the source is reactive, we have to considered a  $50\ \Omega$  matching between the cable and the LNA input.

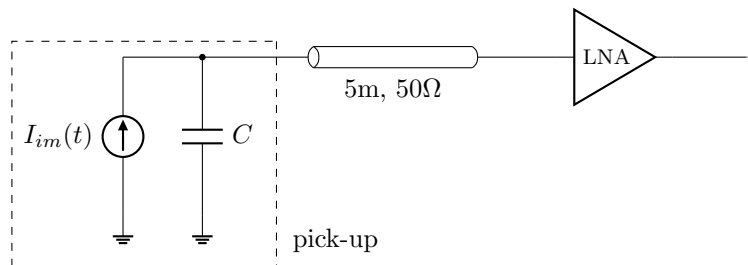


Figure 60: LNA Source

Regarding the minimum noise figure, as previously explained and demonstrated in Chapter 2, we can say that it reaches its minimum value following the formula (29). In other words, the noise figure takes its minimum value when the source impedance  $Z_S$  matches the optimal noise impedance  $Z_{S_{opt}}$ . In the specific case of the BFP740F transistor, as stated in the datasheet, the source impedance required to achieve the minimum noise figure is approximately  $100\ \Omega$ .

To achieve both of these goals, we have adopted a combined approach that includes the simultaneous use of a transformer at the input of the amplifier and a shunt-shunt

feedback circuit. Specifically, starting from the configuration illustrated in Figure 59, we introduced a transformer with a turns ratio of  $\frac{N_s}{N_p} = 2$ . This modification resulted in an increase in gain, raising it to 37 dB, while simultaneously reducing the input impedance by a factor of 4. Subsequently, we implemented a negative shunt-shunt feedback circuit, which is depicted in a block diagram in Figure 61. This form of feedback takes a portion of the output voltage and introduces it in parallel to the input current via a feedback network, thus helping to lower the input impedance.

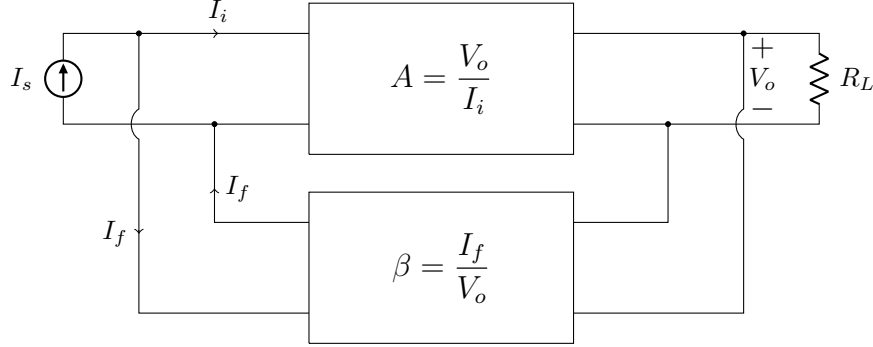


Figure 61: Shunt-Shunt Feedback

In our specific case, as depicted in Figure 63, the shunt-shunt feedback consists of a resistor  $R_{F_2} = 2.2 \text{ k}\Omega$  and a decoupling capacitor  $C_6 = 1 \mu\text{F}$ . The action of this feedback can be simply explained with Miller's theorem, as it aims to place in parallel with the still relatively high input impedance  $Z'_{IN}$  of the amplifier a much smaller resistor that dominates the parallel combination, thereby determining the input impedance as indicated in the following equation:

$$Z_{IN} \simeq \frac{R_{F_2}}{1 - A_v} = \frac{2.2 \text{ k}\Omega}{1 - (-39.81)} \simeq 54 \Omega \quad (74)$$

Where, considering the voltages  $V_A$  and  $V_B$  shown in the circuit in Figure 63, we have:

$$A_v|_{dB} = \left. \frac{V_B}{V_A} \right|_{dB} = 32 \text{ dB} \implies A_v = -39.81 \quad (75)$$



Indeed, from a theoretical standpoint, to achieve an input impedance  $Z_{IN}$  perfectly matching  $50\ \Omega$ , it would have been necessary to use a feedback resistor with a value of  $2.041\ \text{k}\Omega$ . However, the choice of the  $2.2\ \text{k}\Omega$  value was dictated by component availability in the market. Based on the discussion so far, the input impedance  $Z'_{IN}$ , which was initially relatively high, strongly capacitive, and frequency dependent, while it a value of approximately  $50\ \Omega$  is now achieved. Nevertheless, as can be observed from Figure 62, for frequencies in the tens of MHz range, a significant capacitive component is still present. Consequently, we introduced an inductance  $L_1$  of  $39\ \text{nH}$  to cancel the capacitive component. For frequencies around the hundreds of kHz, on the other hand, there is an inductive component that, being extremely low, can be considered negligible. Finally, concerning the output impedance, it is set at  $50\ \Omega$  through the use of the resistor  $R_{14}$ , of the value of  $50\ \Omega$ , placed at the output (in series with a very low impedance).

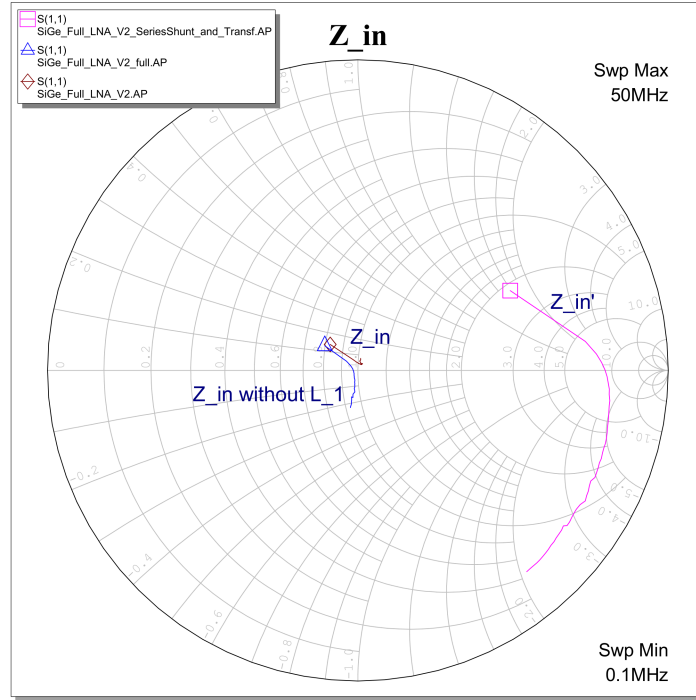


Figure 62: Input Impedance Matching

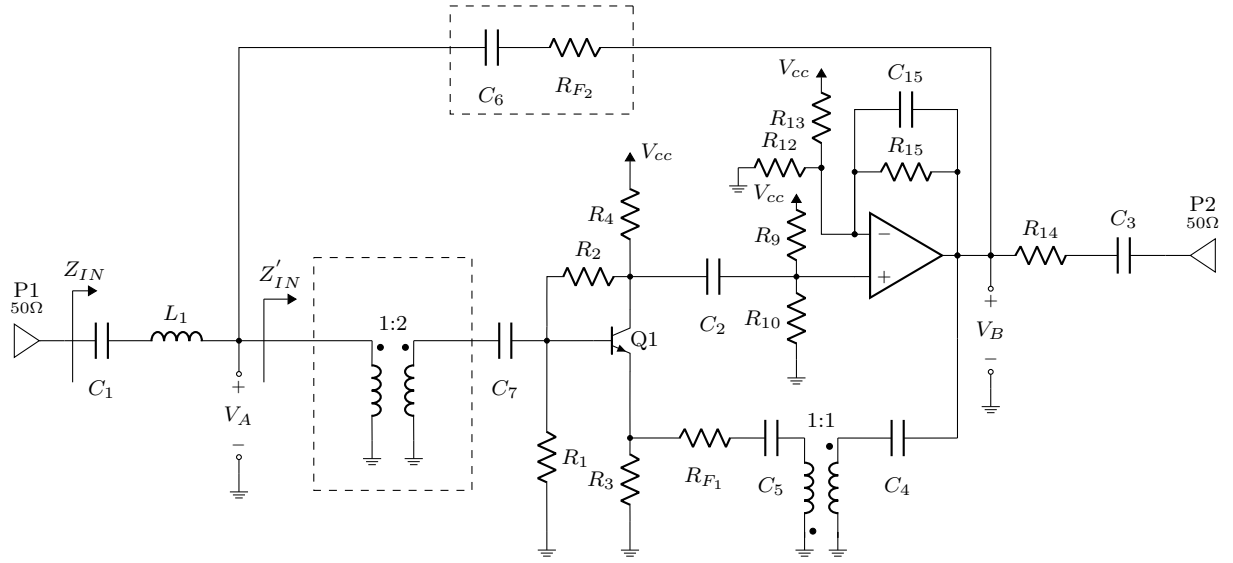


Figure 63: Input Transformer 1:2 and Shunt-Shunt feedback in LNA Design

In conclusion, taking into account all the strategies adopted and discussed so far, the schematic of the Low-Noise Amplifier was finalized, and is presented in Figure 64. Also included in the figure are some components added later during the tests, which will be discussed in the next chapter.

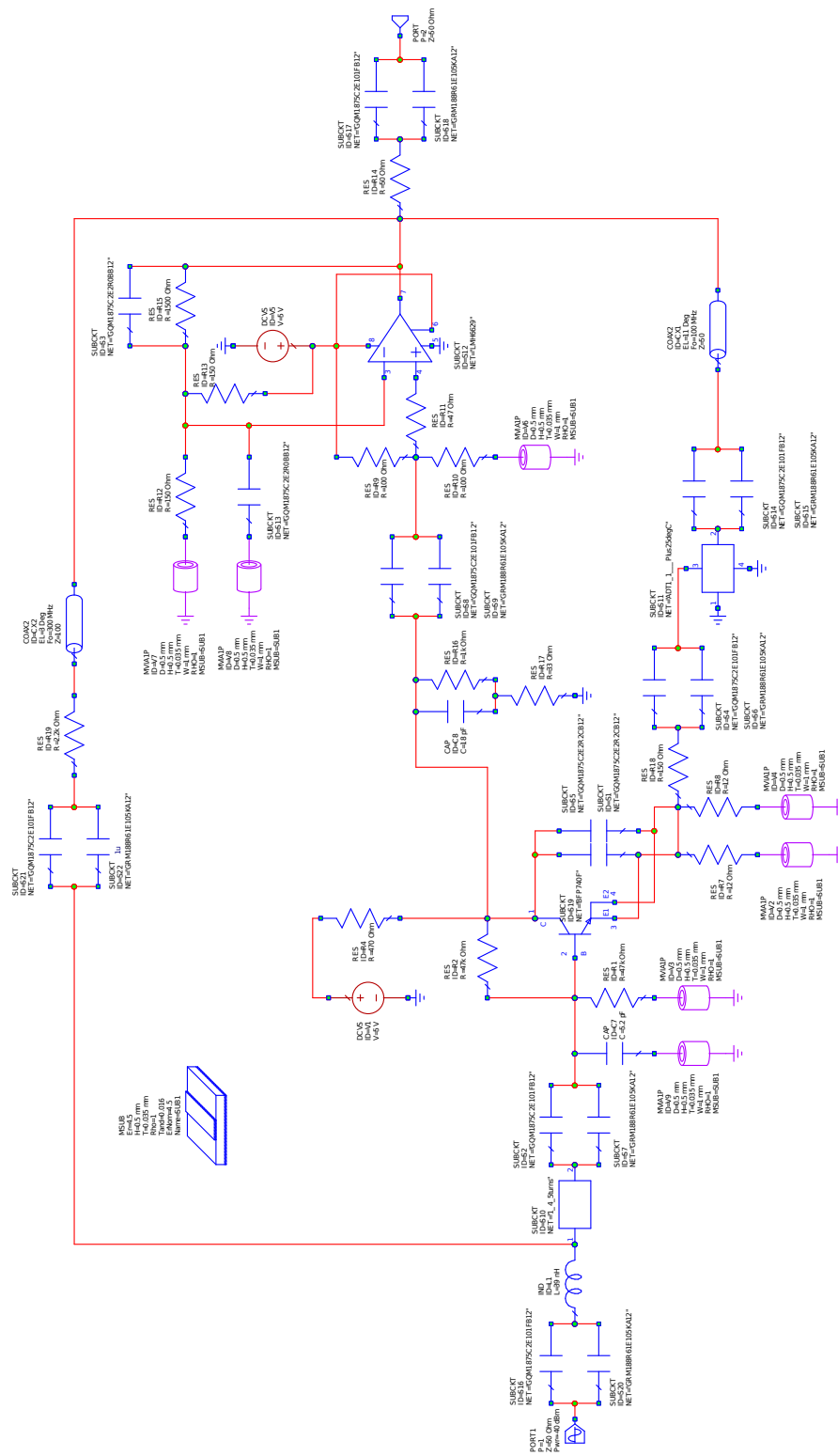


Figure 64: Schematic of the Low-Noise Amplifier based on SiGe HBT

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# Simulation Results and Measurement

Chapter 5 provides a comprehensive analysis of the results obtained through simulations conducted using AWR Microwave Office. Furthermore, this chapter focuses on the methods employed in laboratory testing and their respective outcomes. Finally, a comparative analysis is conducted between the new LNA and the one currently used in the system.

## 5.1 Simulation Results

In this section, we will present the results obtained from the simulations performed with the AWR software. First, a system stability check was conducted. As can be clearly seen from Figure 65, all the parameters, including the K-factor,  $B_1$ ,  $\mu_1$  and  $\mu_2$ , are such as to make the system unconditionally stable (for a more detailed understanding of the requirements that these parameters must meet for the system to be unconditionally stable, please refer to Section 4.4.2). Next, we proceeded to plot the power gain  $S_{21}$ . The value obtained in the band of our interest, which ranges from 0.1 MHz to 50 MHz, is 25.44 dB. It should be noted that a slight resonance is visible around 150 MHz. However, since this resonance lies outside our band of interest, it was not addressed with special attention, as we planned to use an amplifier input filter to cut the band at 50 MHz. The measured noise figure is 1.372 dB, which is less than the 2 dB required by the project specifications. Furthermore, both the input and output matching proved to be satisfactory, as evidenced by the plots on the Smith chart normalized to 50  $\Omega$  shown in figure 69. In particular, we obtained a value of  $S_{11}$  lower than -20 dB. Finally, from the point of view of linearity, it is evident from Figure 70 that the system exhibits linear behavior up to input power levels of -15 dBm. Therefore, from a simulation point of view, we can state with

certainty that all project specifications have been satisfactorily met.

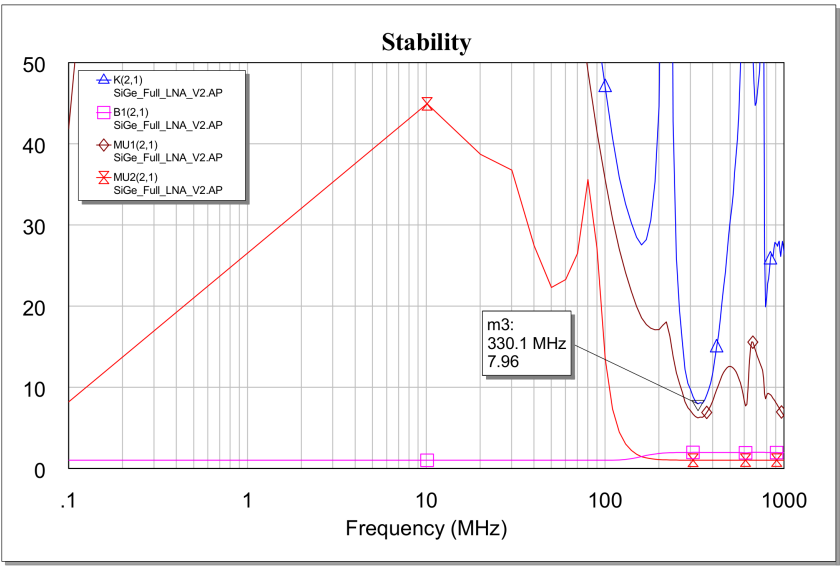


Figure 65: Unconditional Stability - Simulation Result

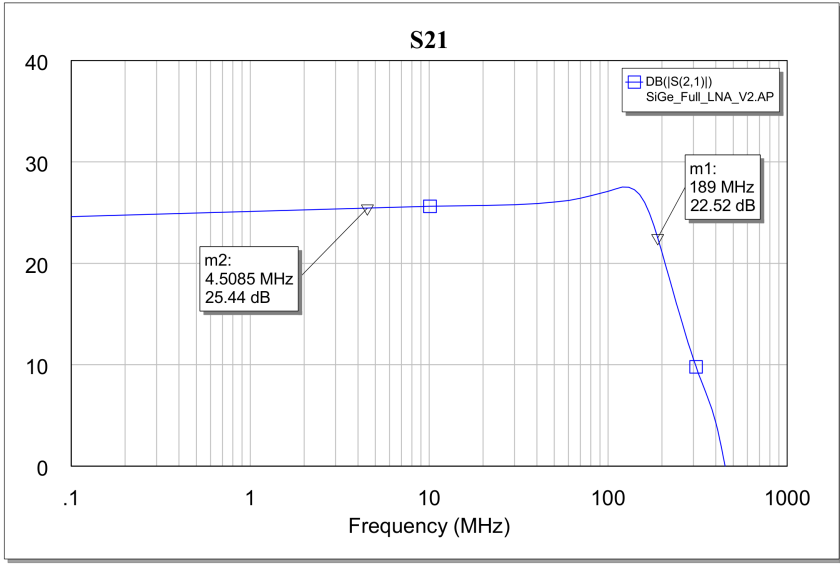


Figure 66: Power Gain - Simulation Result

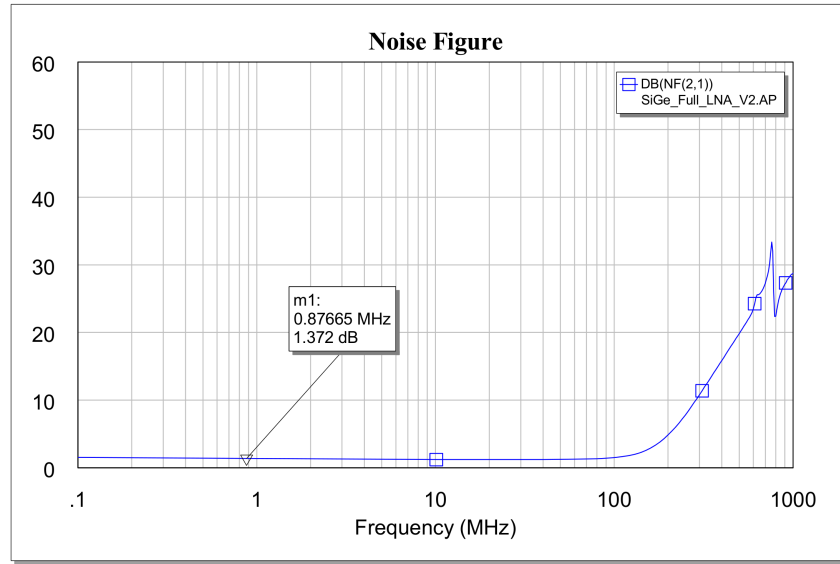


Figure 67: Noise Figure - Simulation Result

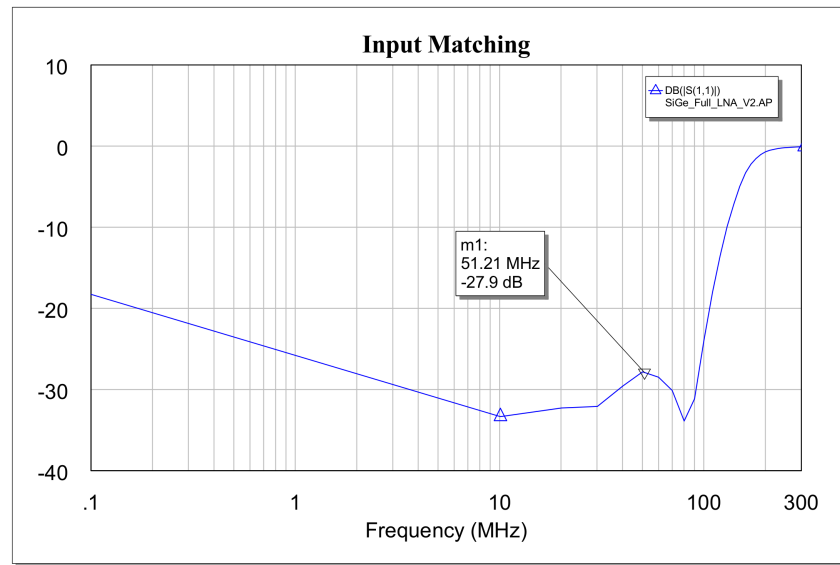


Figure 68: Input Reflection Coefficient  $S_{11}$  - Simulation Result

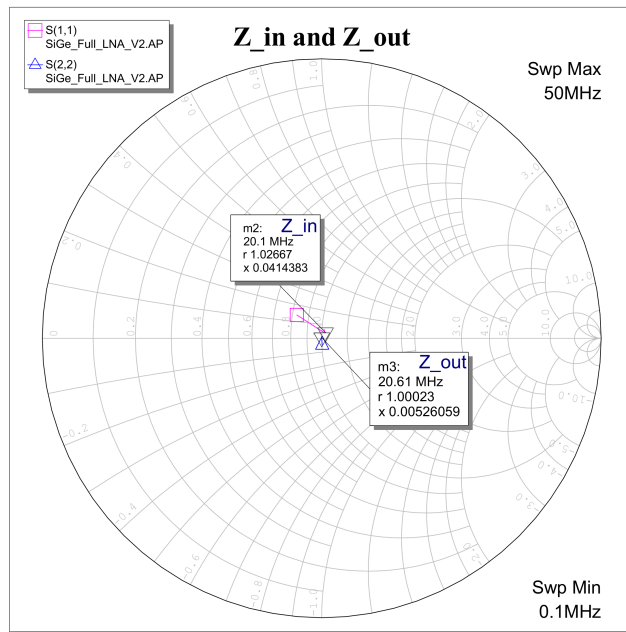


Figure 69: Input and Output Impedance - Simulation Results

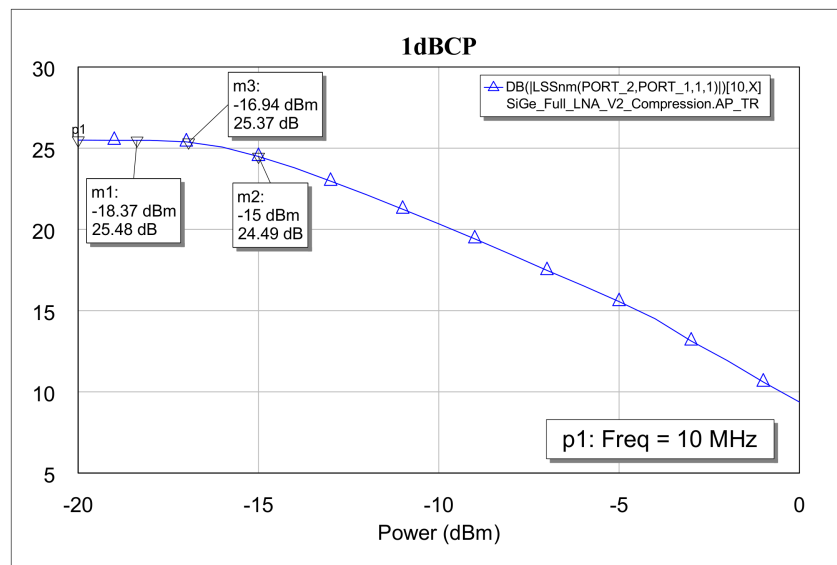


Figure 70: 1dB Compression Point at 10 MHz - Simulation Result

## 5.2 Lab Tests

Once satisfactory results were achieved from the simulation point of view, it was decided to proceed with the design of the PCB depicted in Figures 71 and 72. This PCB accommodates four distinct channels, each dedicated to one of the pick-up electrodes. In addition to the Low-Noise Amplifier, the PCB also includes the passive input filter, stabilizers and filtering for the power supply, and mechanical relays designed to bypass the LNA when the particle beam amplitude does not require amplification. To ensure optimal performance, the PCB was designed following the same layer stack-up shown in Figure 47, previously discussed for the first stage of the LNA. This approach was taken to maintain design consistency and maximize overall efficiency. Furthermore, components were strategically placed on both the top and bottom of the PCB, a strategic choice aimed at minimizing signal paths and, consequently, reducing losses.

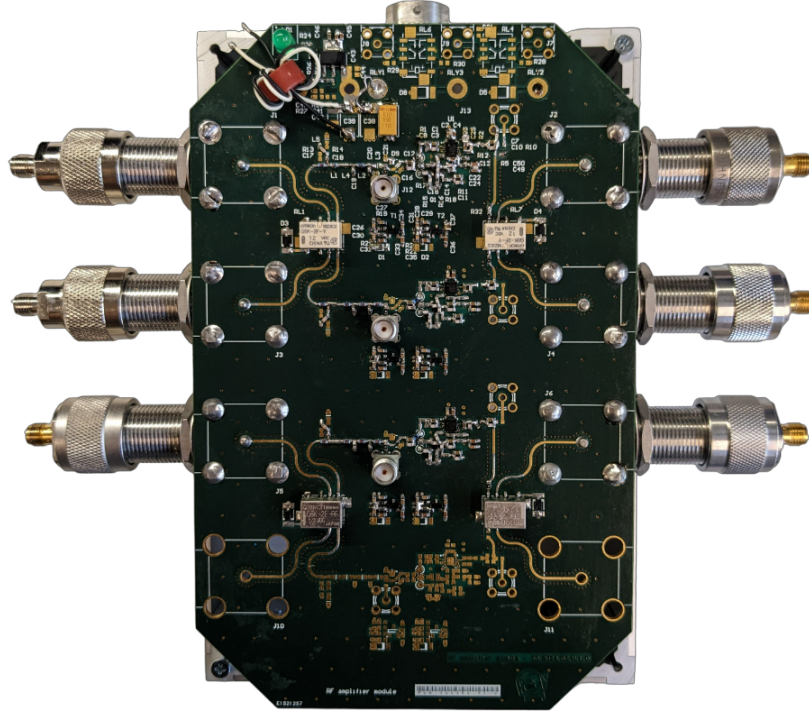


Figure 71: LNA Printed Circuit Board - Top Layer



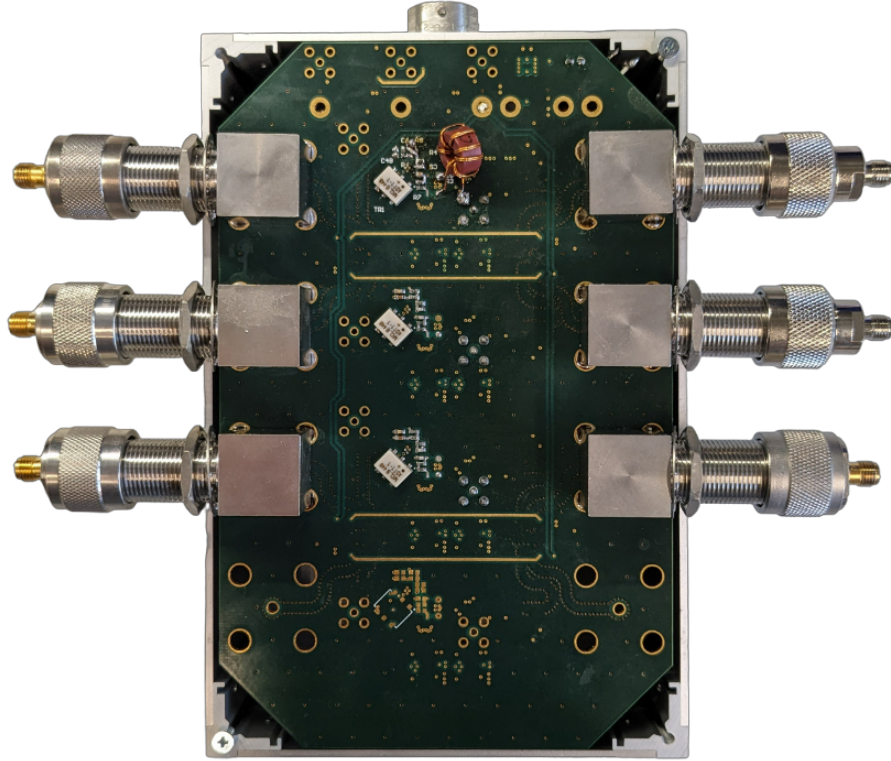


Figure 72: LNA Printed Circuit Board - Bottom Layer

The tests conducted on the board were carried out with a meticulous approach aimed at ensuring the stability and good performance of the amplifier. This strategy allowed for the effective and organized identification and resolution of potential issues. Initially, a set of tests was conducted to evaluate each stage of the amplifier separately. This phase ensured that each individual stage operated stably and consistently with the simulations. Subsequently, a combined test of the two stages was performed, assessing their interaction and the performance of the two cascaded stages. Finally, tests were conducted by introducing one feedback loop at a time. The stepwise approach used, allowed us to identify and solve instability problems, often due to parasitic effects. For example, to stabilize the Op Amp, a 1 pF capacitor, labeled as  $C_{19}$ , was added in parallel with resistor  $R_{12}$ . While, to address oscillations that occurred outside the area of interest, particularly around a few gigahertz (GHz), following the connection of the series-shunt feedback, the RC group consisting of  $C_8$

and  $R_{16}$  in series with resistor  $R_{17}$  was implemented. This network introduced a pole and a zero at the relevant frequencies, effectively resolving the oscillation issue while preserving the frequency response integrity. Finally, the oscillation that emerged after the connection of the second feedback loop was resolved by adding a 5.2 pF capacitor in parallel with  $R_1$ . Once operational stability of the amplifier was achieved, tests were performed to measure the power gain  $S_{21}$ , input and output impedances, and linearity using the Rohde & Schwarz ZNB4 Vector Network Analyzer (VNA). It is important to note that we followed a different approach to evaluate the noise figure compared to what was described earlier in Section 3.2. Specifically, we adopted the “direct method”. The amplifier under test was terminated at the input with a 50  $\Omega$  resistor, a standard condition for measurements of this kind. At the output, we connected it to the Rohde & Schwarz MXO44 oscilloscope, a high-precision instrument with a 12-bit resolution, configured with a Resolution Bandwidth (RBW) of 200 kHz, which provides the sequence of samples at the sampling rate of 1 Gsps. This allows us to measure the output noise power of the amplifier. However, since our goal is to measure the noise present at the input of the amplifier, it is necessary to subtract the gain contribution provided by the amplifier itself. This gain was measured separately using a Vector Network Analyzer (VNA). To perform this subtraction operation, a script was developed that, by receiving the data acquired from the oscilloscope and the data measured by the VNA, allows us to determine the amplifier noise figure. Plots of the results obtained from the tests are shown in the figures below.

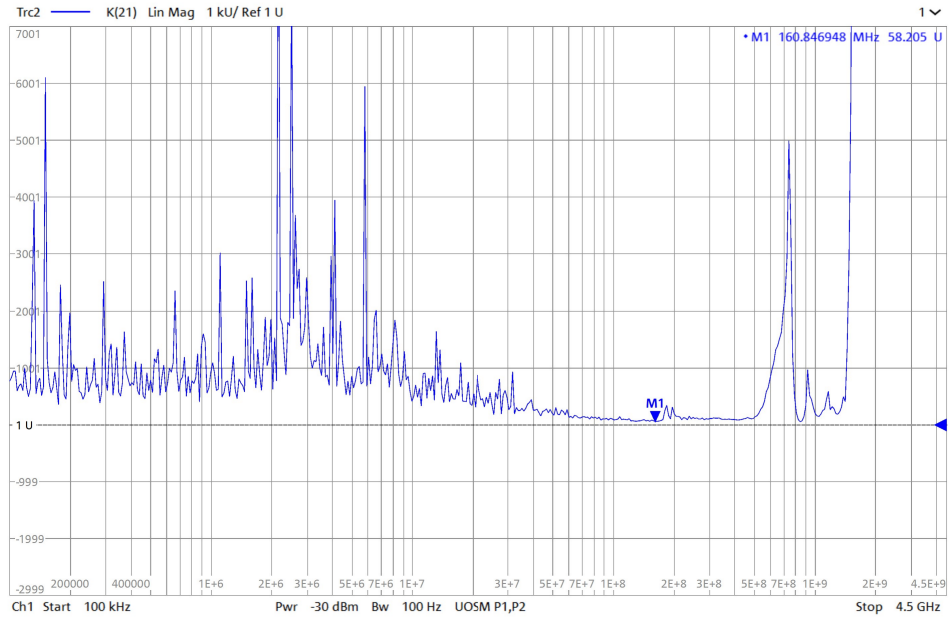


Figure 73: Unconditional Stability - Laboratory Measurement

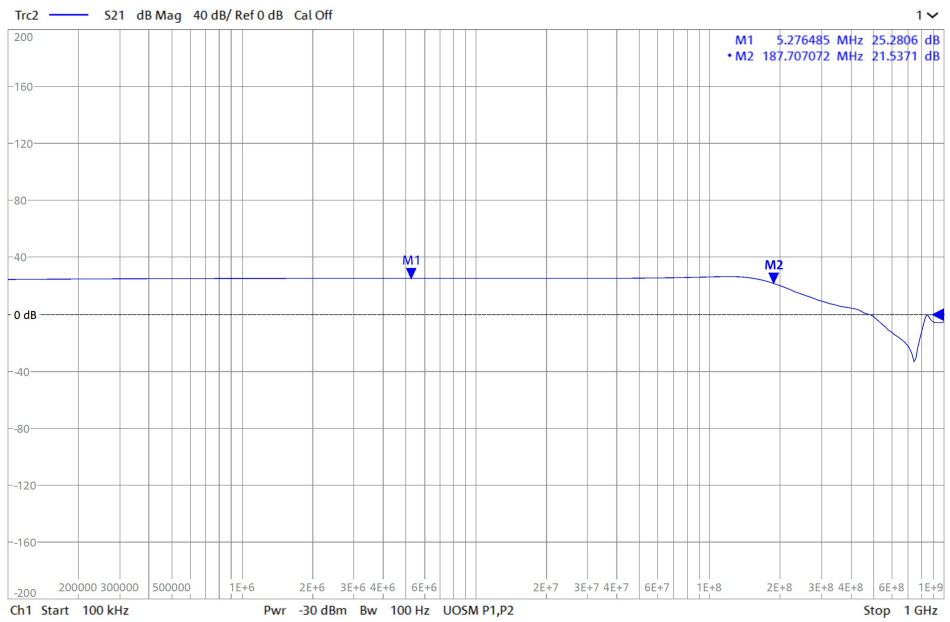


Figure 74: Power Gain - Laboratory Measurement

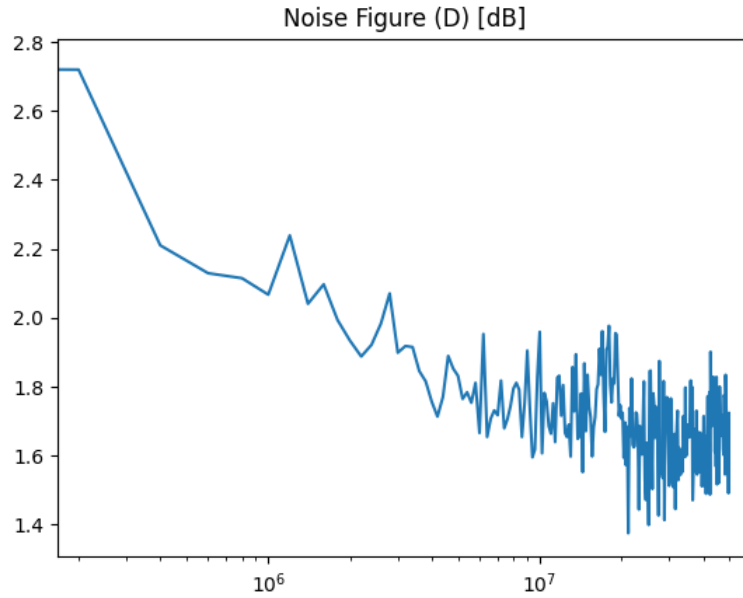


Figure 75: Noise Figure - Laboratory Measurement

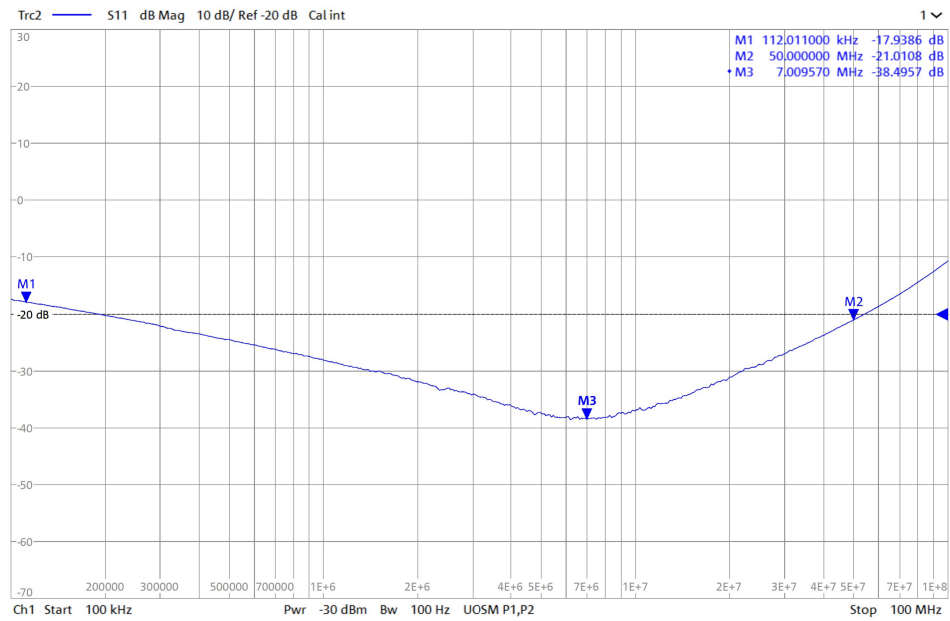


Figure 76: Input Reflection Coefficient  $S_{11}$  - Laboratory Measurement

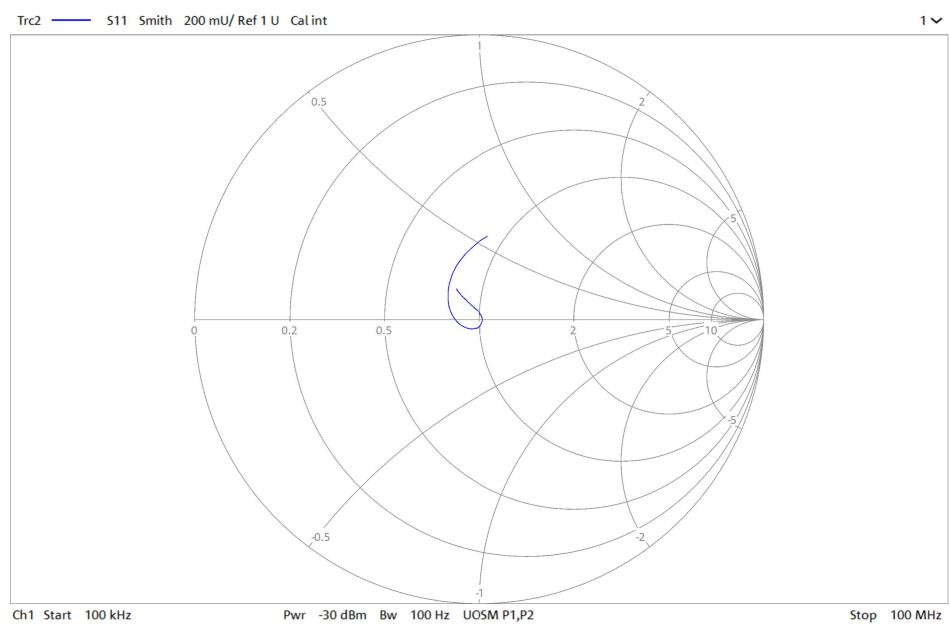


Figure 77: Input Matching - Laboratory Measurement

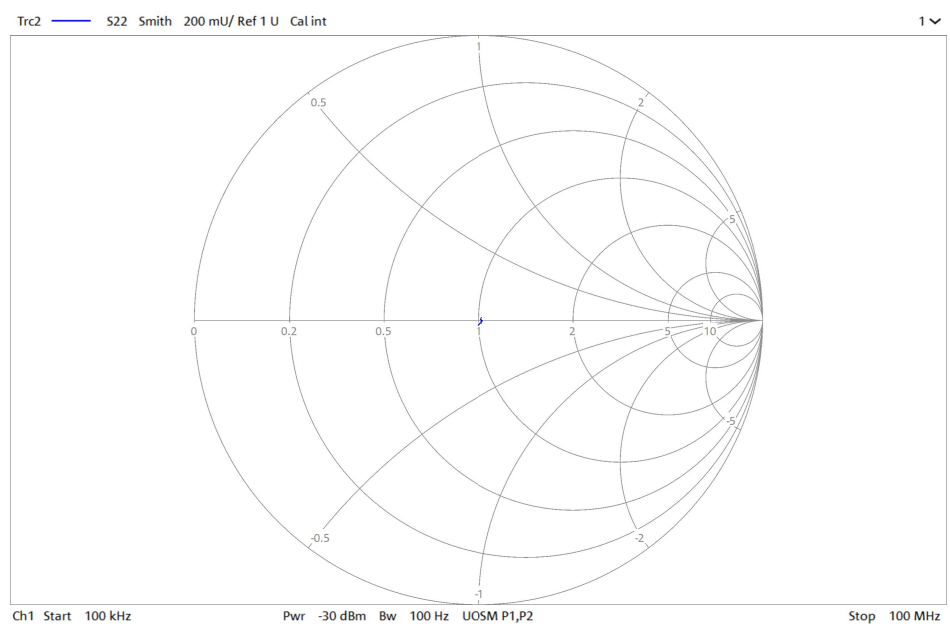


Figure 78: Output Matching - Laboratory Measurement

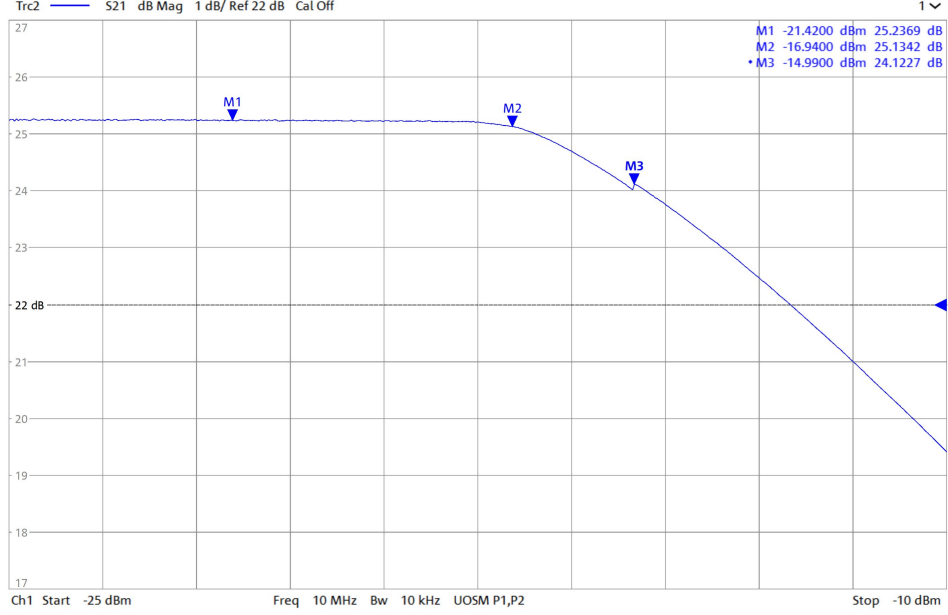


Figure 79: 1dB and 0.1dB Compression Points at 10 MHz - Laboratory Measurement

The results of our experimental tests consistently align with the predictions obtained through simulations, providing robust validation of the performance of our amplifier. Specifically, we measured a power gain ( $S_{21}$ ) of 25.3 dB, a noise figure of approximately 1.5 dB, a reflection coefficient ( $S_{11}$ ) lower than -20 dB, and a linear response (1 dBCP) up to input power levels of -15 dBm. Furthermore, the input and output impedances have a value of 50  $\Omega$ , as required. Of particular significance is the comparison with the current system. From the results presented in Table 8, it is evident that our device not only maintains the performance of the current system but even surpasses it in terms of linearity. In fact, at a frequency of 10 MHz, in the currently used system, the 1 dB compression point occurs at an input power of -22 dBm, while the 0.1 dB compression point occurs at -24 dBm, as observed in Figure 27. In the new designed LNA, these compression points occur at -15 dBm and -17 dBm, respectively.

|                   | Current LNA | New LNA  |
|-------------------|-------------|----------|
| Gain ( $S_{21}$ ) | 24 dB       | 25.3 dB  |
| NF                | 1.237 dB    | 1.5 dB   |
| $S_{11}$          | < -20 dB    | < -20 dB |
| 1dBCP             | -22 dBm     | -15 dBm  |
| 0.1dBCP           | -24 dBm     | -17 dBm  |

Table 8: Comparison between Current LNA and New LNA

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## Conclusions and Future Work

### 6.1 Conclusions

In the course of this thesis, we undertook research to upgrade the Beam Position Monitor (BPM) system of the CERN PS particle accelerator by developing a new Low-Noise Amplifier (LNA) based on Silicon-Germanium Heterojunction Bipolar Transistor (SiGe HBT) technology. Our mission was to breathe new life into a system that, having been in operation for approximately 20 years, its electronic components are now nearing the end of their life cycle, with some critical components having become obsolete. Our efforts aimed not only to update the technological perspective but also to preserve and enhance some of the system performance. The design flow began with a comprehensive analysis of the existing system, with the goal of thoroughly understanding its strengths and weaknesses. This analysis led us to define performance specifications for the new LNA: a bandwidth (BW) between 100 kHz and 50 MHz, a noise figure (NF) of less than 2 dB, and a favorable  $50\ \Omega$  input match characterized by a reflection coefficient  $S_{11}$  below -20 dB. Once the objective was clear, we engaged in the task of identifying modern technology that could effectively replace obsolete RF JFET low noise component without compromising the performance of the current system. After a rigorous evaluation of available options, SiGe HBT technology emerged as the ideal candidate, with Infineon's BFP740F transistor chosen as the key component. This decision was supported by several critical factors, especially its lower flicker noise corner frequency ( $f_c$ ), which positions it as one of the leading contenders among SiGe broadband NPN RF heterojunction bipolar transistors on the market. The next phase involved a series of detailed simulations using software such as LTSpice and AWR, extremely precise PCB design through Altium, prototype creation, and comprehensive laboratory testing. In order to ensure the utmost robustness and reliability of our solution, we built two distinct prototypes: one for the initial phase, confirming the choice of the BFP740F transistor, and a second



one for the final complete board. Laboratory tests produced results that reflected our simulations and validated our design approach. The LNA demonstrated a gain ( $S_{21}$ ) of 25.3 dB, a good  $50\ \Omega$  input matching with an  $S_{11}$  that far exceeded the -20 dB requirement, a low noise figure (NF) of about 1.4 dB, and a 1dBCP at an input power of -15 dBm which highlighted better linearity compared to the current LNA. In conclusion, the attention given to each phase of the project workflow allowed us to fully achieve the project initial goal. In fact, despite all the technical constraints we had to consider, we successfully developed an LNA using a more recent technology that exhibited satisfactory performance results.

## 6.2 Future Work

The results obtained from this thesis work pave the way for interesting future prospects. Firstly, it is evident that there is a need to focus on the optimization phase, with particular attention to reduce the noise figure. The results of this thesis can demonstrate that by lowering the emitter resistance by a few ohms, a significant reduction in the noise figure can be achieved. Therefore, the goal could be to find a solution that allows for achieving a lower noise figure while still maintaining the required load for the Op Amp and considering the impact of the fixed gain of the series-shunt feedback on input impedance. Another interesting perspective for the future is the integration of our LNA into the Beam Position Monitor of the particle accelerator, thereby allowing for a practical evaluation of its performance in a real operational environment and verifying its reliability. Additionally, it is desirable to proceed with the design and development of the other stages that make up the analog front-end, such as the Variable Gain Amplifier (VGA). One possible idea could be to position this stage in the rack cabinet to facilitate accessibility, leaving only the LNA in the gap between the two concrete blocks. Lastly, we can continue to explore and experiment with new technologies that can meet the requirements of low noise figure and increased radiation tolerance. A technology that meets these requirements could have a significant impact on future applications in the field of particle acceleration and in other areas of advanced scientific research, thus contributing to the advancement of science and technology.

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