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Etude de la technologie CMOS pour des détecteurs de particules
pixelisés sous haute intensité et haute dose radiative

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Résumé

Le trajectographe interne (ITk) de l'expérience ATLAS sera amélioré pour la nouvelle phase de prise de données du grand collisionneur de hadrons du CERN à haute luminosité (HL-LHC) en 2026. Le HL-LHC fonctionnera avec une énergie nominale de collision de 14 TeV et une luminosité instantanée maximale de $7,5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$, cinq fois plus élevée qu'à présent. La luminosité accrue se traduira par des niveaux de rayonnement et des débits de données environ dix fois plus élevés. Afin de faire face aux exigences d'ATLAS en termes d'intensité du rayonnement, de vitesse de lecture et de granularité au HL-LHC, le remplacement de l'actuel ATLAS Inner Tracker est nécessaire. Le détecteur de pixels ATLAS ITk consistera en un cylindre à 5 couches à base de silicium.

La technologie du détecteur de pixels hybrides est choisie comme base pour cette mise à niveau du détecteur de pixels ITk. Tandis qu'une option alternative existe pour la mise à niveau du détecteur de pixels: une technologie de détecteur de pixels CMOS totalement monolithiques. Dans ce cas, le capteur et les circuits électroniques de lecture sont intégrés dans le même volume de silicium au sein d'une seule puce. Outre le potentiel de réduction matérielle, cette approche présente un avantage important: elle utilise un processus commercial standard permettant un achat à faible coût et potentiellement facile. De plus, l'utilisation d'un concept monolithique se traduit par des étapes de production plus simples (pas de collage "bump bonding"), des économies de coûts et un risque moindre.

Trois prototypes de détecteurs au silicium ont été développés à l'aide de la technologie commercial CMOS LFoundry 150 nm: CCPD_LF, LF_CPIX et LF-MONPIX1. CCPD_LF est le premier prototype de puce d'une taille de 5 mm × 5 mm produite dans cette technologie. Sur la base des résultats prometteurs de CCPD_LF, une puce de démonstration de plus grande taille (LF_CPIX) a été développée avec divers types de pixels améliorés, conçus pour offrir une efficacité de détection élevée pour des traces de particules ionisantes minimales, une bonne uniformité de pixels, avant et après irradiation. Etant donné que CCPD_LF et LF_CPIX ont été développés pour améliorer les composants des capteurs et des circuits frontaux analogiques, il y avait très peu de logique de lecture à l'intérieur de la puce. La puce LF-MONPIX1 est le premier prototype totalement monolithique mis en œuvre dans la technologie LFoundry par notre collaboration. Il hérite des composants analogiques et capteurs de la puce LF_CPIX et les intègre à une logique de lecture rapide.

Le travail présenté ici montre la simulation TCAD pour l'optimisation de l'anneau de garde et la caractérisation de ces trois prototypes, avec des contributions concernant le développement de la configuration, le calibrage avec des sources ^{55}Fe et ^{90}Sr , modifications du firmware FPGA. Plusieurs programmes de test ont

été développés pour le balayage d'injection, le balayage de seuil et le réglage de seuil. L'étude de la résistance aux radiations pour l'électronique et les composants du capteur a été une préoccupation majeure. Afin de rendre la configuration compatible avec l'installation utiliser pour l'irradiation, une nouvelle configuration a été développée pour le contrôle et la surveillance à distance. Des campagnes de radiation ont été réalisées pour les prototypes LF_CPIX et LF-MONOPPIX1 en 2017 et 2018 respectivement. Nous montrerons les résultats concernant les performances de ces prototypes obtenues à partir de la caractérisation menée en laboratoire (CPPM), ainsi que les résultats des multiples campagnes d'irradiation conduites à l'installation de protons IRRAD de 24 GeV du CERN, afin d'étudier les effets de la perte d'énergie non ionisante (NIEL) et du Dose ionisante (TID) sur les prototypes.

Mots clés : LHC Haute Luminosité, ATLAS, Détecteur pixel silicium, Technologie HV/HR CMOS, Détecteur tolérant aux radiations, depleted CMOS détecteur de traces

Abstract

The Inner Tracker (ITk) system of the ATLAS experiment will be upgraded for the 2026 High Luminosity Large Hadron Collider (HL-LHC) run. The HL-LHC will operate with a center of mass energy of 14 TeV and a peak instantaneous luminosity of $7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$, five times higher than at present. The increased luminosity will result in roughly ten times higher radiation levels and data rates. To cope with the ATLAS requirements in terms of radiation hardness, readout speed and granularity at the HL-LHC, the replacement of the present ATLAS Inner Tracker (ITk) is needed. The ATLAS ITk Pixel Detector will consist in a 5-layer cylinder and endcaps equipped with silicon detector.

The hybrid-pixel detector technology is chosen as baseline for this ITk Pixel Detector upgrade. While an alternative option exists for the pixel detector upgrade: a fully monolithic depleted-CMOS Pixel Detector technology. In this case, the sensor and the full readout electronic circuitry are integrated into the same silicon volume in a single chip. In addition to a potential for material reduction, one important advantage of this approach relates to the use of a standard commercial process, which enables low cost and potentially easy procurement. Furthermore, the use of a monolithic concept translates in simpler production steps (no bump-bonding), savings in cost and with lower risk.

Three prototypes of silicon detectors have been developed using LFoundry 150 nm CMOS technology process: CCPD_LF, LF_CPIX and LF-MONOPIX1. CCPD_LF is the first prototype chip with a size of $5 \text{ mm} \times 5 \text{ mm}$ produced in this technology. Based on the promising results of CCPD_LF, a larger size demonstrator sensor chip (LF_CPIX) was developed with various improved pixel types designed to have high in-time detection efficiency for minimum ionizing particle tracks, good pixel uniformity, before and after irradiation. Since CCPD_LF and LF_CPIX were developed to improve the sensor and analog front end circuitry parts, there was very little read-out logic inside the chip. The LF-MONOPIX1 chip is the first fully monolithic prototype implemented in LFoundry technology by our collaboration. It inherits the analog and sensor parts of LF_CPIX chip, and integrates them with a fast readout logic.

The work presented here shows the TCAD simulation for the sensor guard ring optimization and characterization for these three prototypes, with contributions concerning the setup development, ^{55}Fe and ^{90}Sr sources calibration, modifications of the FPGA firmware. Several test programs were developed for injection and threshold scans and threshold tuning. A main concern was the investigation on the radiation hardness for both the electronics and the sensor parts. In order to make the setup compatible to the radiation facility, a new setup was developed for remote control and monitoring. One radiation campaign in 2017 and

two more in 2018 were performed for LF_CPIX prototypes and LF-MONOPPIX1 prototypes, respectively. We will show results concerning characterizations for these prototypes in the laboratory at CPPM, as well as results in multiple radiation campaigns performed at the 24 GeV IRRAD proton facility at CERN, to study the effects of Non-Ionizing Energy Loss (NIEL) and Total Ionizing Dose (TID) on the prototypes.

Keywords : HL-LHC, ATLAS, Silicon pixel detector, HV/HR monolithic CMOS sensor, Depleted CMOS radiation-hard detector

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Introduction

The Large Hadron Collider (LHC) located at CERN is the world's largest and most powerful particle accelerator. It first started on 10 September 2008, and remains the latest addition to CERN's accelerator complex. These complex scientific instruments allow us to study the basic constituents of matter-fundamental particles. The beams inside the LHC are made to collide at four locations around the accelerator ring, corresponding to the positions of four particle detectors. The collision process gives us clues about how the particles interact, and provides insights into the fundamental laws of nature. ATLAS is one of four main detectors, with the purpose of finding new particles, such as the discovery of Higgs boson within the Standard Model, physics beyond the Standard Model and the development of new theories to better describe our universe.

In order to increase the LHC potential for discoveries, the High-Luminosity Large Hadron Collider (HL-LHC) project is scheduled after 2025. The HL-LHC will operate with a center of mass energy of 14 TeV and a peak instantaneous luminosity of $7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$, five times higher than the present one. The increased luminosity will result in roughly ten times higher radiation levels and data rates. To cope with this harsh environment, ATLAS detector is preparing a complex series of upgrades including the installation of new detectors using state-of-the-art technology, the replacement of ageing electronics, and the upgrade of its trigger and data acquisition system. To meet all of the requirements of a charged particle tracking detector close to the beamline at the HL-LHC, the Inner Tracker (ITk) system of the ATLAS experiment has to be replaced. The design of the ITk Pixel Detector proposed is based on the highly successful concept of "Hybrid Pixel Detector" developed for and implemented in the present ATLAS Pixel Detector and in the IBL. Since the fabrication of hybrid pixel modules relies on very specific technologies and construction techniques that do not have a large commercial market outside of particle physics, the total cost need particular concern. An alternative option exists for the pixel detector upgrade or in other contexts: a fully monolithic depleted-CMOS Pixel Detector concept. In this case, the sensor and the full readout logic circuitry are integrated into a single chip and commercial CMOS processes used for the production, which enables low cost and easy procurement.

Within the ATLAS CMOS demonstration collaboration, two approaches are pursued. The first one is based on small collection electrode and the second one on large collection electrode concept. In the small collection electrode concept, the charge-collecting node is placed outside the CMOS circuitry, which reduces the input capacitance to the circuitry, and offers lower power consumption for the analog front-end circuit. However, as charges need to travel longer distances to the collection node, the radiation-hardness of such a concept needs to be care-

fully assessed. In contrast, the large collection electrode design provides a Deep-Nwell (DNW), which embeds the electronics, and acts as a charge-collecting node. This results in a more uniform electric field in the bulk and shorter drift distance and leads to better radiation hardness. The price to pay is a larger input capacitance to the electronics and also need to study the sensor to electronics coupling.

In this work, three large collection electrode concept prototypes, named CCPD_LF, LF_CPIX and LF-MONOPIX1 which were developed in LFoundry 150 nm CMOS technology on a high resistivity wafer are mainly presented. The LHC, the ATLAS experiment and upgrades will be described in Chapter 1. In Chapter 2, the silicon physics and the pixel sensor operation concepts will be discussed. Pixel detector for the ITk outermost Pixel Layer upgrade will be introduced in Chapter 3. LF_CPIX demonstrator development and characterization before and after radiation will be discussed in Chapter 4. Finally, LF_MONOPIX1: first monolithic CMOS sensor developments and characterization will be addressed in Chapter 5.

1. The LHC and ATLAS experiment

CERN (European Organization for Nuclear Research) is a European research organization located in Geneva Switzerland, which operates the largest particle physics laboratory in the world. The laboratory was established to study of interactions between subatomic particles, furthermore understand the fundamental structure and laws of the universe and origin.

1.1. The Large Hadron Collider

CERN operates a complex of eight accelerators and two decelerators, as shown in Figure 1.1 [1]. The Large Hadron Collider (LHC) is the largest and most powerful particle accelerator at CERN even in the world. It was first launched on September 10, 2008. The LHC consists of a 27 km long accelerator with superconducting magnets and many accelerating structures to increase the energy of particles along the way. Protons are obtained by removing electrons from hydrogen atoms. LINAC2 is the first accelerator in the chain, accelerates the protons to the energy of 50 MeV. The beam is then injected into the Proton Synchrotron Booster (PSB), which accelerates the protons to 1.4 GeV, followed by the Proton Synchrotron (PS), which pushes the beam to 25 GeV. Protons are then sent to the Super Proton Synchrotron (SPS) where they are accelerated to 450 GeV. The protons are finally transferred to the two beam pipes of the LHC, protons will circulate in the LHC for 20 minutes before reaching the maximum speed and energy. Heavy ions are also produced for the LHC from a source of vaporised lead and enter LINAC3 before being collected and accelerated in the Low Energy Ion Ring (LEIR). Then they follow the same route to maximum acceleration as the protons. Inside the LHC accelerator, two high-energy particle beams travel in opposite directions in separate beam pipes, which are kept at ultra-high vacuum. They are guided around the accelerator ring by strong superconducting magnetic division [2] [3].

Once the protons have reached the required energy, the two beams are made to collide in the center of the four detectors experiment: ATLAS (A Toroidal LHC ApparatuS) [4], CMS (Compact Muon Solenoid) [5], ALICE (A Large Ion Collider Experiment) [6] and LHCb (The Large Hadron Collider beauty) [7]. The two larger experiments, ATLAS and CMS, are based on general-purpose detectors to study a wide range of physics, including the search for the Higgs boson, extra dimensions, super-symmetry and particles that could make up dark matter. Setting two independent and different technology based detectors is vital for cross-confirmation of any new discoveries made. Two medium-sized experiments, ALICE is designed to study the physics of strongly interacting matter at extreme energy densities, where a phase of matter called quark-gluon

plasma forms, LHCb is a specialized b-physics experiment, designed primarily to measure the parameters of CP (Charge-Parity) violation in the interactions of b-hadrons (heavy particles containing a bottom quark) [8].

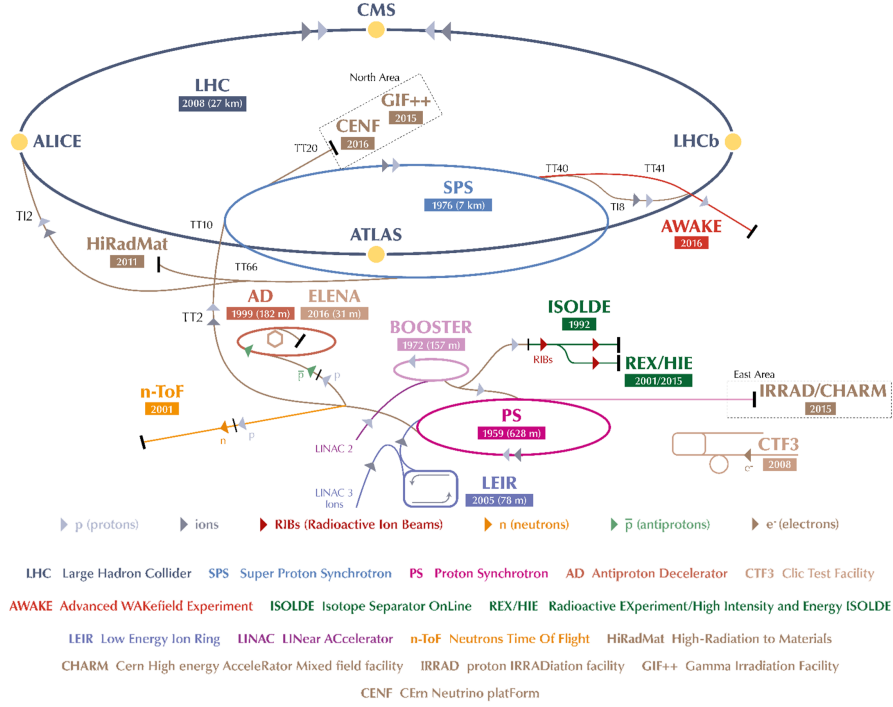


Figure 1.1. – CERN accelerator complex

1.1.1. LHC status and upgrade

The CERN LHC was designed to collide 7 TeV protons beam and heavy ions of equivalent energy. Since an incident happened in one of the main dipole circuits during the first commissioning in 2008 [9] [10], the LHC restarted at lower beam energy (3.5-4 TeV) to avoid the potential risk. Through the Run 1, around 25 fb^{-1} of proton data was obtained with a peak luminosity of $7.5 \times 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$. Luminosity is proportional to the number of collisions per square centimeter and per second ($\text{cm}^{-2} \text{ s}^{-1}$). In order to make sure that the LHC can operate at higher energy stably, a Long Shutdown 1 (LS1) from 2013 to 2014 was followed, a number of consolidation and upgrade was done during this time. Run 2 started in 2015 with the centre of mass energy of 13 TeV, and stopped running at the end of 2018, nearly 150 fb^{-1} data was delivered with a peak luminosity around $2.0 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$, as shown in Figure 1.2 [11]. The comparisons of LHC run parameters for Run 1 and Run 2 are shown in Table 1.1 [12]. There will be no physics data taking for the next 2 years due to Long Shutdown 2 (LS2).

CERN accelerator complex will be upgraded during the Long Shutdown 2 between now and spring 2021. The LHC upgrade timeline is shown in Figure 1.3. During LS2, the LHC will be tested for operation at its design energy of 14 TeV and the luminosity will be 2 times higher than Run 2. Almost the entire LHCb experiment will be replaced with faster detector components. ALICE will mainly upgrade the technology of its tracking detectors. ATLAS and CMS will undergo large improvements and start to prepare for an ambitious upgrade for HL-LHC (High-Luminosity LHC) [13].

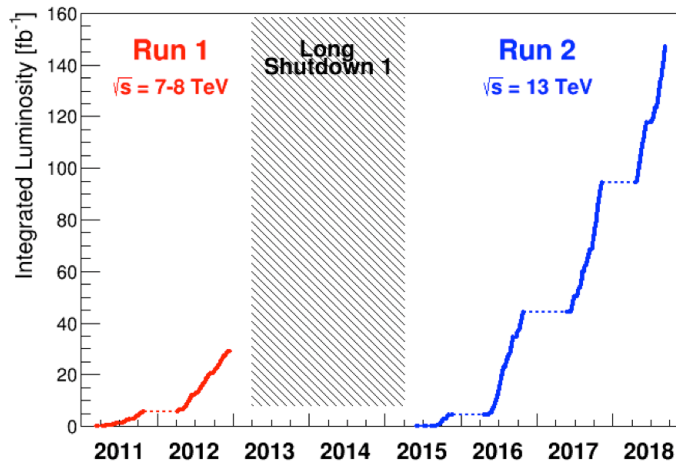


Figure 1.2. – Integrated luminosities of Run 1 and Run 2

LHC parameter	Run 1	Run 2
Center-of-mass energy	7-8 TeV	13 TeV
Peak luminosity	$7.7 \times 10^{33} \text{ cm}^{-2} \text{ s}^{-1}$	$2.1 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$
Bunch crossing spacing	50 ns	25 ns
Interactions per crossing (mean)	21 interactions	36 interactions
Number of bunches	1368 bunches/beam	2544 bunches/beam

Table 1.1. – Comparisons of LHC run parameters for Run 1 and Run 2

In order to produce more data and increase its discovery potential, the High Luminosity Large Hadron Collider (HL-LHC) is foreseen to switch on after LS3 by 2026 with a center of mass energy of 14 TeV and a levelled luminosity of $7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ and to deliver integrated luminosities of 250 fb^{-1} per year with the goal of 3000 fb^{-1} , five times higher than at present. The increased luminosity will result in ten times higher radiation levels and ten times higher data rates.

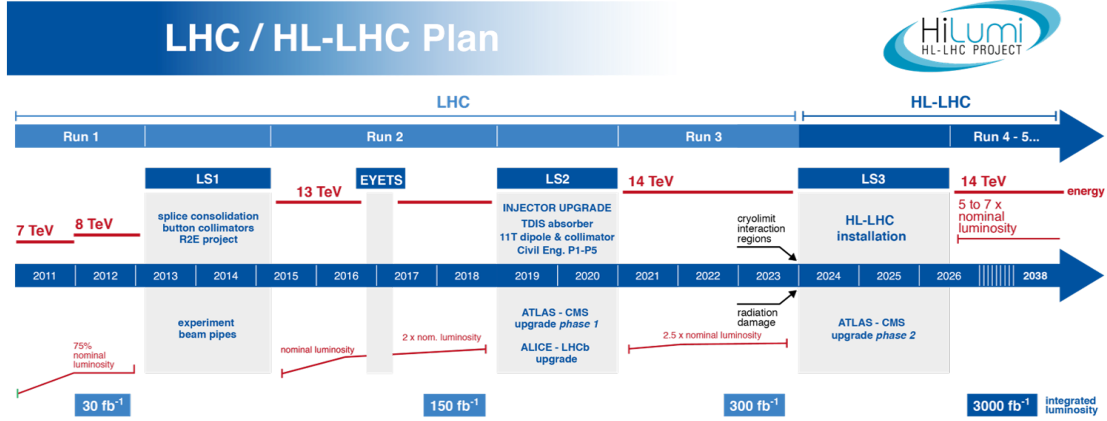


Figure 1.3. – The LHC/HL-LHC upgrade timeline

1.1.2. LHC physics goals

The Standard Model (SM) is the theory, which was developed in stages throughout the latter half of the 20th century, describing the elementary particles and their interactions, as shown in Figure 1.4 [14]. All matter around us is made of elementary particles, which are the building blocks of matter. These particles occur in two basic types called quarks and leptons. Each group consists of six particles, which are related in pairs, or "generations". The lightest and most stable particles make up the first generation, whereas the heavier and less-stable particles belong to the second and third generations. There are also four fundamental forces at work in the universe: the strong force, the weak force, the electromagnetic force, and the gravitational force. They work over different ranges and have different strengths. Although the Standard Model is believed to be theoretically self-consistent [15] and has demonstrated huge successes in providing experimental predictions, some phenomena still can not be explained by SM, such as gravitation, neutrino masses and oscillations, the presence of dark matter and dark energy, and the asymmetry between matter and antimatter [16]. The LHC provides the opportunities to study the particle physics processes within the SM and also beyond SM (BSM).

During the LHC Run 1, a big success has been achieved by discovering the Higgs boson by the ATLAS and CMS independently, which is considered as the final piece of the standard model of particle physics. The existence of Higgs boson was already predicted in 1964 based on SM theory [17] [18].

However, the discovery of Higgs boson is a huge success of LHC, the behavior of Higgs boson is still blurred. The precision measurement of the Higgs boson properties is one of the future physics goals of HL-LHC, the properties include spin and parity, the coupling strength to the SM particles, the branching ratios and the form of the Higgs potential [19] [20].

Many other investigations of the SM will continue in parallel with Higgs bo-

Quarks	mass: $\approx 2.3 \text{ MeV}/c^2$ charge: $2/3 e$ spin: $1/2$  up	mass: $\approx 1.275 \text{ GeV}/c^2$ charge: $2/3 e$ spin: $1/2$  charm	mass: $\approx 173 \text{ GeV}/c^2$ charge: $2/3 e$ spin: $1/2$  top	 gluon	 Higgs boson
	mass: $\approx 4.8 \text{ MeV}/c^2$ charge: $-1/3 e$ spin: $1/2$  down	mass: $\approx 95 \text{ MeV}/c^2$ charge: $-1/3 e$ spin: $1/2$  strange	mass: $\approx 4.18 \text{ MeV}/c^2$ charge: $-1/3 e$ spin: $1/2$  bottom	 photon	
	mass: $0.511 \text{ MeV}/c^2$ charge: $-1 e$ spin: $1/2$  electron	mass: $105 \text{ MeV}/c^2$ charge: $-1 e$ spin: $1/2$  muon	mass: $1.777 \text{ GeV}/c^2$ charge: $-1 e$ spin: $1/2$  tau	 Z boson	
Leptons	mass: $< 2.2 \text{ eV}/c^2$ charge: 0 spin: $1/2$  electron neutrino	mass: $< 0.17 \text{ MeV}/c^2$ charge: 0 spin: $1/2$  muon neutrino	mass: $< 15.5 \text{ MeV}/c^2$ charge: 0 spin: $1/2$  tau neutrino	 W boson	
				 W boson	

Figure 1.4. – Summary of the particle states in the Standard Model

son measurements. Precision measurements of top quark properties, such as the measurement of its cross sections, rare production and decay processes, mass and spin determination, and couplings.

Beyond the Standard Model, Supersymmetry (SUSY) is one of the best motivated extensions of the SM, controlling the Higgs boson mass by cancelling contributions from SM particles and their heavier SUSY partners, a natural description of the unification of forces, and a plausible dark matter candidate. The huge HL-LHC dataset will allow the investigation of electroweak production of SUSY particles [20].

1.2. The ATLAS experiment before phase 2 upgrade

ATLAS is one of the four major experiments at the LHC. It is a general-purpose particle physics experiment designed to exploit the full discovery potential and the huge range of physics opportunities that the LHC provides.

A schematic representation of the ATLAS detector is shown in Figure 1.5 [21]. ATLAS has the dimensions of a cylinder of 46 m long, 25 m in diameter, and sits in a cavern 100 m under the ground. The ATLAS detector weighs 7,000 tonnes [4].

The four main components of ATLAS detector are the Inner detectors, Calorimeters, Muon spectrometer and Magnet system. Integrating with detectors are the trigger and data acquisition systems, a specialized multi-level computing system, which can select physical events with significant characteristics; and the computing systems for storing, processing and analysing large amounts of data at 130 computing centres around the world.

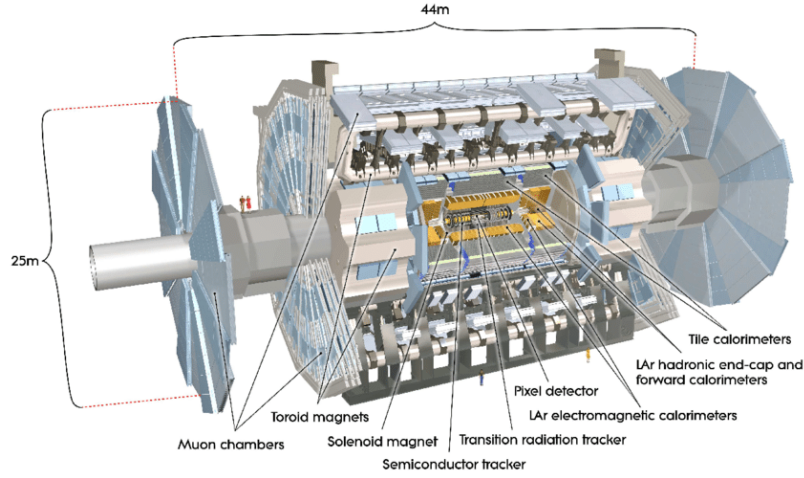


Figure 1.5. – 3D general view of the ATLAS detector

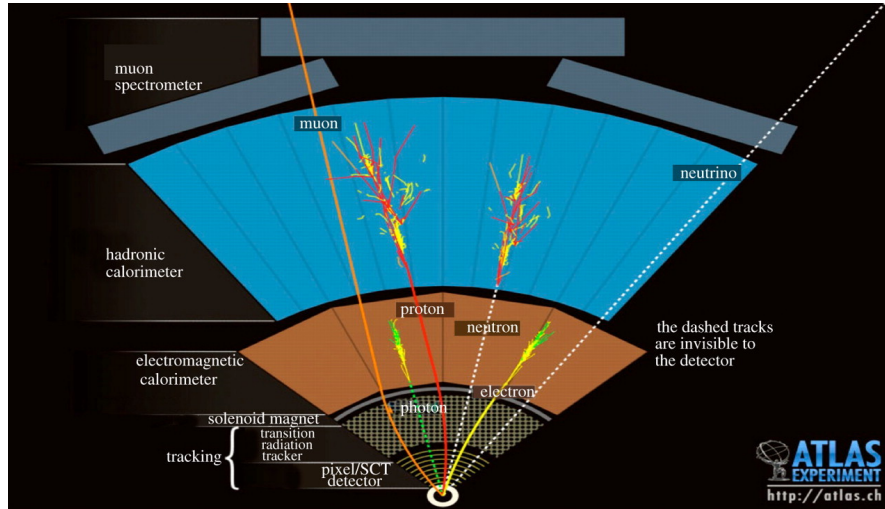


Figure 1.6. – Schematic of the particles passing through the layers in the Atlas detector

Figure 1.6 shows diagram of the interactions in the sub-detectors of the different particles entering the ATLAS detector [22]. The sub-detector system concentrically wrap around the collision point to record particle trajectories, momentum and energy, so that they can be identified and measured separately. Giant magnet systems bend the charged particles so that their momentum can be measured as accurately as possible. The photons and the electrons, having passed through the different layers of the internal detector, lose all their energy in the electromagnetic calorimeter in the form of a sheaf. Hadrons (π , K, p, n etc) deposit some of their energy in the electromagnetic calorimeter, but end up in the hadronic calorimeter in the form of a sheaf. They also go through the different layers of the

internal detector. The muons pass through the entire detector leaving a signal in each part of the detector up to the muon spectrometer. Finally, the neutrinos pass through the entire detector without being detected.

1.2.1. Inner detector

The internal detector is the first part of ATLAS, which is used to observe the charged particles from pp collisions, so it is very compact and must be highly sensitive. Figure 1.7 shows the main components of the Inner Detector: Pixel detector, SemiConductor Tracker (SCT), and Transition Radiation Tracker (TRT) [23]. All of them are surrounded by a solenoid providing a magnetic field parallel to the beam axis. The internal detector measures the direction, momentum and charge of charged particles generated in proton-proton collision.

Pixel detector

Pixel detectors originally consisted of three barrel layers. The radius of each layer is 55.5 mm, 88.5 mm and 122.5 mm, respectively and the length is around 80 cm. In 2015, a new Insertable B-Layer (IBL) was inserted and installed with an inner layer 33 mm away from the beam axis [24]. The pixel sensor contains 80 million pixels with a area 1.7 m^2 [25]. The original three outer layers of the Pixel Detector and endcaps are standard n-in-n planar sensors with pixel size of $50 \times 400 \text{ } \mu\text{m}^2$. Each pixel module is made of 2×8 FE-I3 front-end readout chips and bump bonded to a sensor tile of area $63.4 \times 24.4 \text{ mm}^2$ and $250 \text{ } \mu\text{m}$ thickness [26]. A flexible Printed Circuit Board (PCB) is glued on top of the sensor tile to connect the hybrid module. Figure 1.8 shows a schematic view of a barrel pixel module [27].

The IBL is an additional point for tracking particles, more points mean better precision. In IBL, two novel pixel sensor technologies were implemented. The central part is made of n-in-n planar sensors and 3D n-in-p sensors placed at the ends of the barrel. Both sensor types have a pixel size of $50 \times 250 \text{ } \mu\text{m}^2$ and are bump bonded to the more recent FE-I4 front-end readout chip [28].

SCT

The SCT is a key precision tracking part in the ATLAS inner detector and composed of 4088 planar p-in-n silicon micro-strip detectors two-sided modules and over 6 million implanted readout strips. 60 m^2 of silicon distributed over 4 cylindrical barrel layers and 18 planar endcap disks. Readout strips are placed every $80 \text{ } \mu\text{m}$ on the silicon, allowing the positions of charged particles to be recorded to an accuracy of $17 \text{ } \mu\text{m}$ per layer in the direction transverse to the strips.

TRT

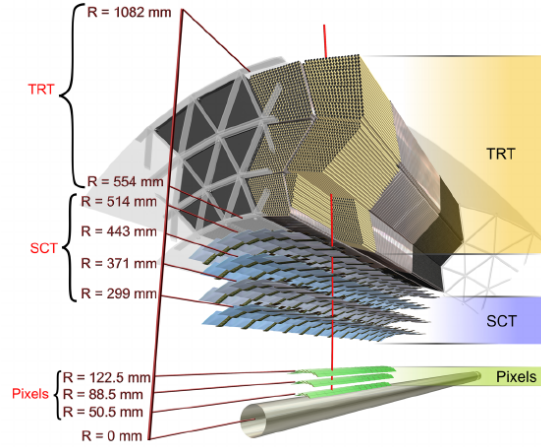


Figure 1.7. – The Inner detectors of ATLAS with the pixel detector, the SemiConductor Tracker (SCT), and the Transition Radiation Tracker (TRT)

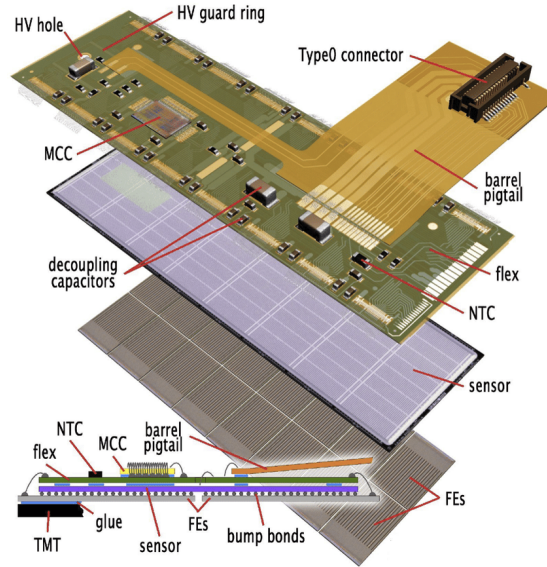


Figure 1.8. – Schematic view of a barrel pixel module

The ATLAS Transition Radiation Tracker is the outermost of the three tracking subsystems of the ATLAS Inner Detector. As mentioned before, the pixel and SCT detector are based on silicon technology while TRT is gaseous detector. The basic detector element is thinwalled straw tubes with 4 mm diameter with a 0.03 mm diameter gold-plated tungsten wire. The spacing between the straws is filled with highly structured plastic materials, in which transition radiation is generated by charged particles as they pass through this combination of layers. TRT provides electron identification capability through the detection of transition radiation X-ray photons[29]. The TRT contains 300000 thin-walled proportional-mode drift tubes providing on average 30 two-dimensional space points with $130 \mu\text{m}$ reso-

lution for charged particle tracks [30].

1.2.2. Calorimeters

Calorimeters active elements measure the energy a particle loses as it passes through the detector. Calorimeter is usually designed to stop entire or absorb most of the particles coming from a collision, forcing them to deposit all of their energy within the detector. Calorimeters typically consists of dense absorber material to fully absorb incident particles and active material to produce an output signal proportional to the input energy. So the information from the calorimeters is important for identifying the particles produced by the collision.

There are two types of subsystems in ATLAS calorimeter: the Liquid Argon (LAr) Calorimeter and the Tile Hadronic Calorimeter.

1.2.2.1. Liquid Argon Calorimeter

The Liquid Argon (LAr) Calorimeter is shown in Figure 1.9 [31]. The ATLAS LAr calorimeter consists of four subdetectors: the electromagnetic Barrel (EMB), the electromagnetic Endcap (EMEC), the hadronic Endcap (HEC) and the forward calorimeter (FCal).

EMB and EMEC

The EMB and the EMEC detect and identify electrons and photons covering respectively a pseudorapidity-range of $|\eta| < 1.4755$ and $1.375 < |\eta| < 3.2$ [32], and measures their energy. The absorbers are made of lead and the detection medium is liquid argon. The space filled with liquid argon is under an intense electric field. Particles in the shower produce ionization electrons which drift through the liquid argon driven by the electric field. The signal derived from this electron current is amplified, shaped, digitized and recorded.

Both EMB and the EMEC have an accordion geometry. The accordion geometry of EMB (see Figure 1.10) meets the requirements on energy and angular resolution, high segmentation, read-out speed with low pileup, and hermeticity [33] [34].

The EMEC is similar to the barrel in conception. However the realization of the accordion structure in the endcap region is not mechanically easy. In order to maintain a spatially constant sampling fraction, ATLAS has chosen the "wheel" like structure, this is in essence a variable fold angle with radius. This geometry is shown in Figure 1.11a. The arrangement of modules into the endcap wheel is shown in Figure 1.11b [35]. There is one wheel at each end of the detector, with 8 modules per wheel. There are 96 gaps in the outer wheel which vary in width from 2.8 mm to 0.9 mm in order to realize the constant sampling fraction; the inner wheel has 32 gaps varying in width from 3.1 mm to 1.8 mm. Each wheel assembly of 8 modules has a diameter of 4000 mm [33].

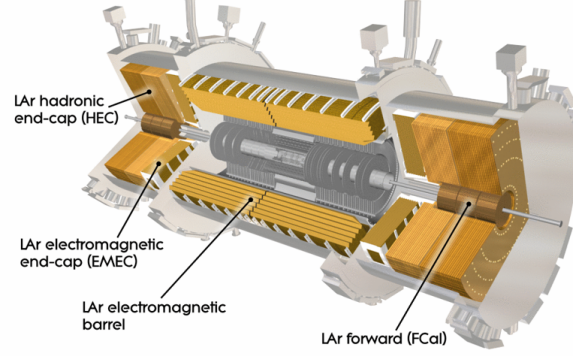


Figure 1.9. – The Liquid Argon (LAr) Calorimeter in ATLAS

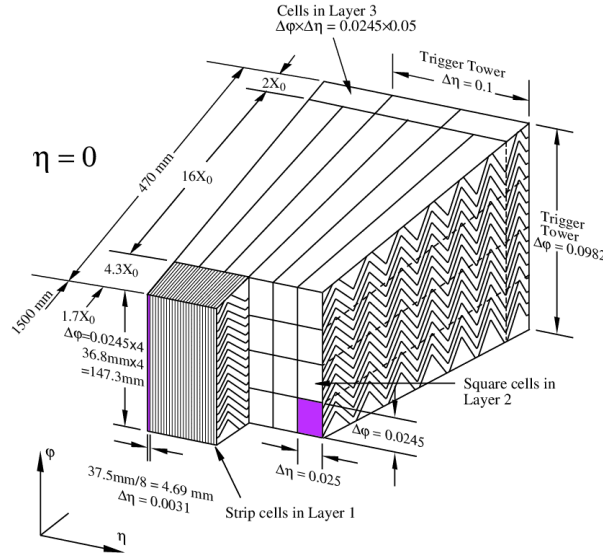
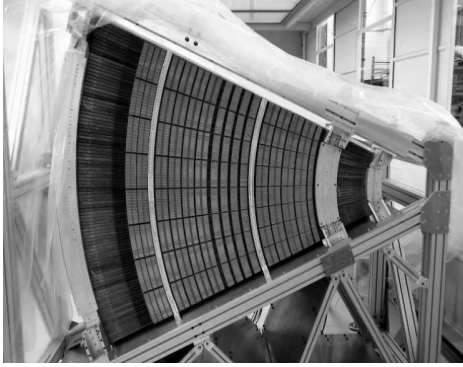


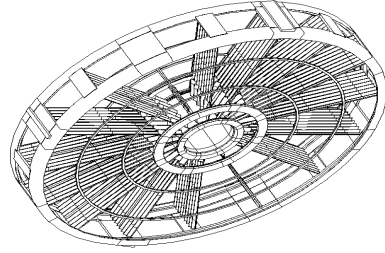
Figure 1.10. – The accordion structure of the barrel calorimeter

HEC

The HEC is a copper/liquid argon sampling calorimeter covering the $1.5 < |\eta| < 3.2$ region. Energy resolution is at a premium in the electromagnetic calorimeters. However, in the hadronic calorimeters the optimization goals are somewhat different. The hadronic calorimeters are primarily concerned with jet mass reconstruction, and the calorimeter energy resolution is not the dominant contribution. Instead the hadronic endcap calorimeter design aim is for a compact, reliable, radiation tolerant design of minimum cost [33]. It consists of two independent wheels located behind the end-cap electromagnetic calorimeter, each wheel is divided into two longitudinal segments [32].



(a) Front view of the first EMEC module



(b) The endcap wheel

Figure 1.11. – Details of the construction of the endcap electromagnetic calorimeter

FCal

The ATLAS forward calorimeter (FCal) covers the high pseudorapidity regime $3 < |\eta| < 5$. Since forward calorimeters are located near the incident beams, the most challenging issues are radiation damage resistance, reliability. For this reason, a metal matrix of radiation-hard hollow copper/tungsten tubes is used rather than metal plates as in the HEC.

FCal is made of three distinct modules, it is made of several copper tubes acting as electrodes. Each tube is hollow, with an electrode made of copper in its center, and filled with LAr. The first module (FCAL1) is an electromagnetic calorimeter, made of copper to act as absorber, while the other two are hadronic calorimeters, made of tungsten slugs "sandwiched" between two copper plates. Tungsten is used instead of copper because of its higher density, despite the fact that it is more difficult to machine. When hadrons traverse the copper tubing, they produce a hadronic shower that produces lower energy hadrons and knocks off protons and neutrons from the nuclei of some of the copper atoms, which leave a trail of electron-ion pairs along their path in the argon. The electric potential between the rod and the tube causes the ions produced to drift to the positive electrode, creating a detectable current [36].

1.2.2.2. Tile Hadronic Calorimeter

The Tile Hadronic Calorimeter covers the most central region of the ATLAS experiment, and is designed to measure the hadrons, jets and taus and to measure the missing transverse energy. It is divided in 3 parts along the beam direction, as shown in Figure 1.12 [37]. The Tile Barrel is located in the middle with 5.56 m

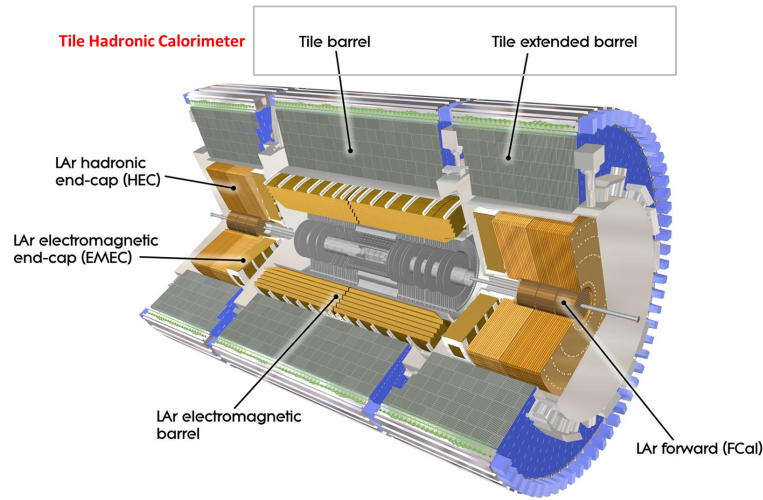


Figure 1.12. – A cut-away view of the ATLAS calorimeters

in length. Two Tile Extended barrel are placed at the edge with 2.91 m in length. The 3 parts are segmented into 64 modules each. Each module is constructed of iron plates and plastic scintillating tiles. The iron plates are used as absorber and plastic scintillating tiles are used as the active material. The scintillating tiles are placed in the plane perpendicular to the colliding beams and are radially staggered in depth, as illustrated in Figure 1.13 [38]. The scintillating tiles are read-out by wave-length shifting (WLS) fibers on both sides of each module. These fibers deliver the light which generated by the charged particles of the hadronic showers crossing the scintillator tiles, to photomultipliers (PMTs) located in the outer radius iron structure that also houses the front-end electronics [39].

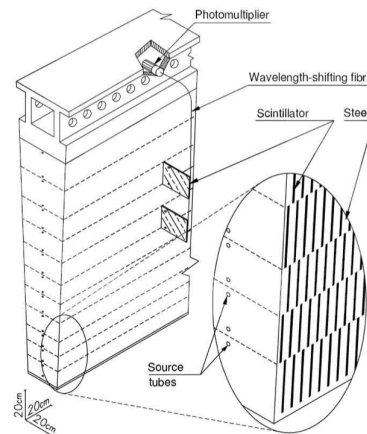


Figure 1.13. – The ATLAS Tile Calorimeter module

1.2.3. Muon Spectrometer

Muons can penetrate through the calorimeters and reach the outermost part of ATLAS, known as the muon spectrometer. Figure 1.14a shows the schematic view of the muon spectrometer in the x-y (top) and z-y (bottom) projections. This spectrometer surrounds the calorimeters and measures the trajectories of muons to determine their direction, their electric charge and their momentum.

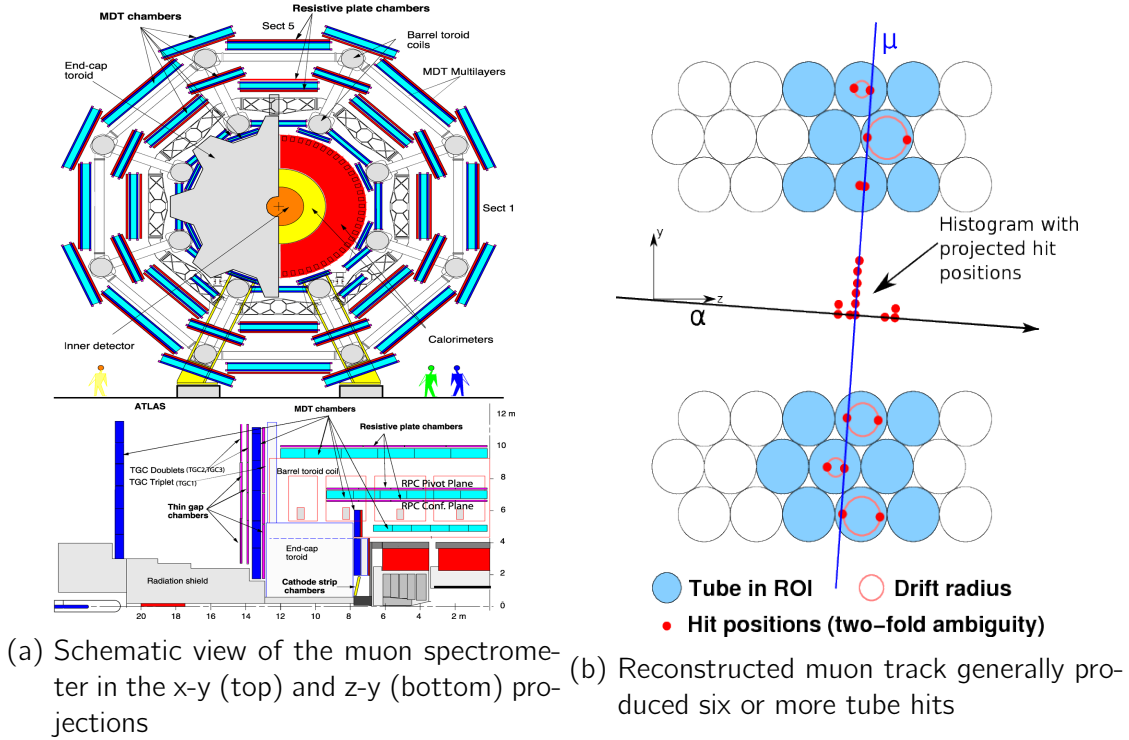


Figure 1.14. – ATLAS Muon Spectrometer precision chambers

One segment of the muon chamber contains many small tubes filled with gas, as a muon passes through these tubes it leaves a trail of electrically charged ions and electrons, which drift to the sides and center of the tube. The circles on the Figure 1.14b show the potential position of the starting point in each tube [40]. Measuring the time it takes for these charges to drift from the starting point, makes possible to determine the position of the muon as it passed through (see in Figure 1.14b).

1.2.4. Trigger system

A trigger system in particle physics is using simple criteria to rapidly decide whether or not to keep an event from a given bunch-crossing for later study. Only a small fraction of events can be recorded due to the limitations in data storage capacity and rates. Since the high instantaneous luminosity up to $2 \times 10^{34} \text{ cm}^{-2}$

s^{-1} during Run-2, the trigger system need to work at very high trigger rates. An efficient and reliable trigger and data acquisition system is required to cope with such beam conditions which result in large and complex data flows [41]. In terms of the ATLAS TDAQ system, a complex selection strategy was developed and successfully implemented. Successful and reliable early data reduction is critical for the high background process rates in hadron collisions.

The ATLAS trigger system consists of two independent levels during the Run-2 data-taking period: a hardware-based first level (L1) and a software-based high level trigger (HLT) [41]. The L1 trigger uses custom electronics to determine Regions-of-Interest (RoIs) in the detector, taking as input coarse granularity calorimeter and muon detector information. L1 can reduce the event rate from 40 MHz to 100 kHz, since a decision must be taken every 25 ns. The decision time for a Level-1 accept is $2.5 \mu s$ [42]. The L1 system in Run-2 consists of the L1 calorimeter trigger system (L1Calo), the L1 muon trigger system (L1Muon), new L1 topological trigger modules (L1Topo) and the Central Trigger Processors (CTP) [43]. The signatures which can be selected in the L1 trigger are missing transverse energy, candidate electrons, photons, jets and muons [44], but there are no information coming from the tracking devices in L1.

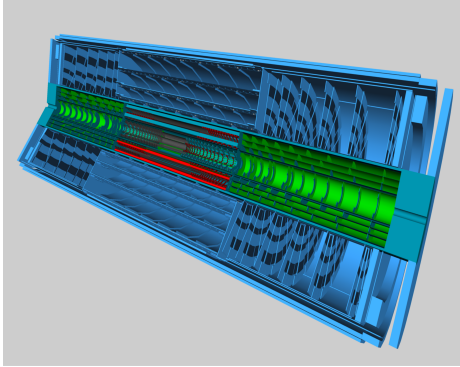
The ATLAS trigger system had separate Level-2 and Event Filter computer clusters in Run-1 period. The system was merged into a single event processing HLT farm in Run-2, which reduces the complexity and allows for dynamic resource sharing between algorithms. This new arrangement reduces algorithm duplication and results in a more flexible HLT, reducing duplicated data-fetching. The HLT reduces the rate from the Level-1 output rate of 100 kHz to approximately to a level of 0.5 kHz to 1 kHz within a processing time of about 200 ms [42].

1.2.5. ATLAS upgrades

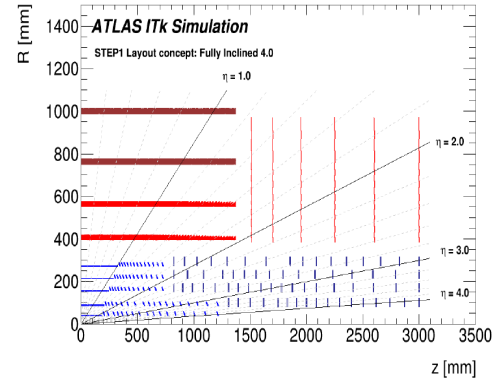
In the last few years the whole ATLAS experiment has been upgraded several times and can be divided into three phases along with the LHC/HL-LHC timeline (see in Figure 1.3). The first phase (Phase-0) was performed during the LS1, where a new layer called Insertable B-Layer (IBL) was added inside the pixel detector as an additional layer, closer to the beam line than the innermost layer at that time (B-Layer). The upgraded pixel modules in the IBL, are designed to be more radiation hard and with higher granularity for sensor and readout chip to cope with the more number of pile-up events as the LHC was proceeding to Run 2. The second phase (Phase-I) upgrade is scheduled for 2019-2020 during the LS2 and will mainly focus on the upgrade of the outer parts of the ATLAS detector.

The largest changes to the ATLAS detector come with the third phase (Phase-II) for 2024-2026 during the LS3, in order to cope with the challenging environment described in section 1.1.1, major parts of the ATLAS detector will be replaced for the HL-LHC. For the muon system, a complete replacement of the

readout electronics is foreseen, together with additional upgrades of the trigger systems, with the aim to increase the readout capabilities and the trigger rate.



(a) Display of the ATLAS ITk



(b) Schematic layout of the ITk

Figure 1.15. – ATLAS ITk for Phase-II upgrade

Regarding the Inner detector upgrade, the Pixel Detector, the Semiconductor Tracker, as well as the Transition Radiation Tracker will be indeed replaced by an all-silicon detector called the ITk (Inner Tracker), as shown in Figure 1.15a. The ITk will consist of a 5-layer Pixel detector as the inner part extending the coverage to $|\eta| < 4$ and a 4-layer Strip detector supplemented with 2×6 end-cap disks covering $|\eta| < 2.7$ as the outer part (see in Figure 1.15b) [45]. In addition, due to the harsh radiation environment expected, the inner two layers of the Pixel Detector, which will be exposed to the largest radiation fluences, will be replaceable. The upgraded pixel detector will be instrumental since it will consist of new readout electronics and sensor technologies which are able to withstand high radiation and occupancy environment of the HL-LHC, more details will be discussed in Chapter 3.

2. Silicon properties and sensor principles

2.1. Silicon properties as semiconductor

A semiconductor is a material which has an intermediate conductivity, between the typical conductivity of a metal and the one of an insulator. Silicon is an extremely common element and very likely the most important semiconductor material. Silicon-based detectors have benefited from the strength and rapid development of the semi-conductor industry, since the 1950s when McKay first reported semiconductor junction as ionizing detector [46]. As discussed above in section 1.2.5, the new upgrade of ATLAS tracker [45] [47] will only consist of silicon technology. The physics of silicon, and in particular when it is used as a material for particle detection, are introduced in this chapter.

In a silicon crystal, the periodic lattice establishes allowable bands for electrons and holes present. The low energy band is called the valence band and corresponds to the part of the electrons that are bonded to the atoms in the crystal. The next higher band is named the conduction band, which contains electrons, which can move freely through the crystal. The electrons in the conduction band and the holes in the valence band contribute to the electrical conductivity of the material. The two bands are separated by a band gap, and the energy of the band gap determines whether the material belongs to the semiconductor category or the insulator category. For insulators, the band gap is typically over 5 eV. In the case of intrinsic silicon, the valence band is full and the conduction band is empty. While for semiconductors, the band gap is much smaller than 5 eV. The band gap of silicon is 1.12 eV at 300 K.

If the valence electrons get enough energy, they can go through the bandgap into the conduction band. This process means that an excited electron can then move freely in the crystal. Furthermore, it will also leave behind a hole that can flow as current exactly like a physical charged particle. The processes produce two mobile carriers which is called an electron-hole pair and is the basic charge carrier in a solid state device.

2.1.1. n-type and p-type silicon

For intrinsic silicon (silicon with no impurities), when electron-hole pairs are created by excitation, each electron leaves a hole behind at the same time, so the concentration of electrons n in the conduction band and holes p in the valence band is equal

$$n = p = p_i = n_i = 1.45 \times 10^{10} \text{ cm}^{-3} \quad (2.1)$$

where n_i and p_i are the intrinsic electron concentration and hole concentration in silicon at $T = 300\text{ K}$, respectively. In most cases, silicon used in semiconductor devices is not intrinsic, but is doped with a small concentration of impurities to change the concentration of electron and hole carriers, thereby changing its conductivity. In this case, the semiconductor is called extrinsic. Adding impurities to the silicon crystal produces a doped material which can be of two types depending on the types of the impurities.

As an example shown in Figure 2.1b, with the addition of phosphorus, an element which has one more valence electron than the silicon atom, the additional electrons remaining after forming all covalent bonds will have an energy near the top of the gap. The energy gap between this energy level and the bottom of the conduction band is quite small, so the thermal excitation is high enough to ensure that most of the additional electrons are excited, resulting in more electron charge carriers than hole charge carriers.

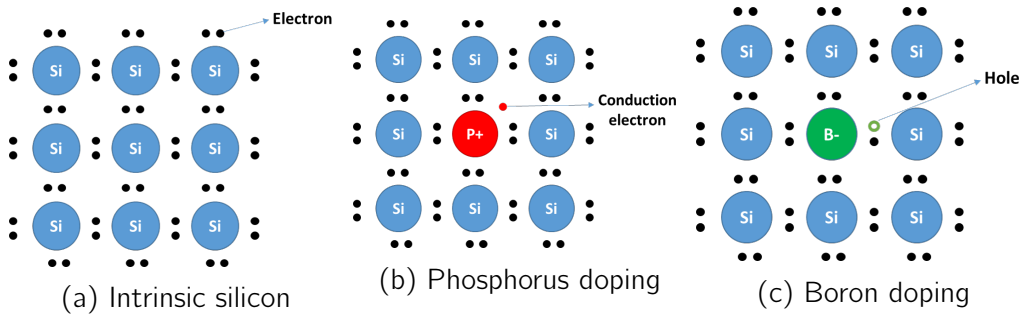


Figure 2.1. – The silicon doping diagram

As a result, an "n-type" silicon is formed in which electrons are the majority of charge carriers and holes are the minority of charge carriers. Elements like phosphorus are called donors since they are capable to provide conduction electrons in silicon, these are typical elements of the 5th column of the Mendeleev periodic table.

In opposite, boron can also dope the silicon, as shown in Figure 2.1c, The boron element has one less valence electron than the silicon atom. As a result, boron can easily accept one of the electron from a covalent bond of neighbouring silicon atoms. This missing bond can travel around the crystal due to valence electron rearrangement. Effectively, the missing electron (the hole) is a free carrier travelling in the crystal.

Elements like boron are called acceptors, as they are capable of attracting one extra electron from the silicon atoms. This type of doped silicon is called p-type silicon. These are typical elements of the 3rd column of the Mendeleev periodic table.

2.1.2. Principle of a p-n junction

When n-type silicon and p-type silicon material are joined together, there is a gradient of charges on both sides of the p-n junction, so the transportation of charges can occur, the transfer of electrons and holes on the p-n junction is called diffusion, as shown in Figure 2.2. As a result of this transfer, some free electrons from the n-type material and some holes from the p-type material recombine. The charge carrier recombination leaves a net charge behind, related to the remaining ions, positive ions on the n-type material side, and negative ions on the p-type side. The width of these p- and n+ regions depend on the acceptor density N_A and donor density N_D .

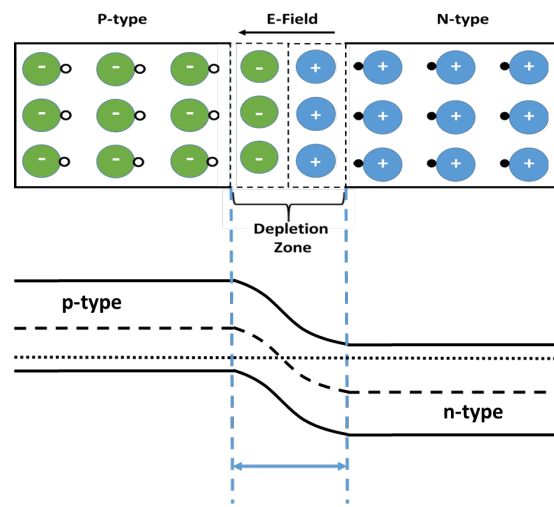


Figure 2.2. – A conceptual view of p-n junction at thermal equilibrium

The electron and hole diffusion processes will continue until building up an electric field due to the remaining ions would balance the free carrier diffusion process. When reaching an equilibrium state, it creates a potential barrier around the junction. The areas on either side of the junction are now completely depleted and this area around the p-n junction is named depletion zone. The total charge on both sides of the p-n junction must be equal and opposite to maintain a neutral state of charge around the junction. If the depleted zone width is d , the depleted zone width on the p-doped side is D_p , and the depleted zone width on the n-doped side is D_n . The following relation between the acceptor and donor density must hold to maintain charge neutrality:

$$D_p \times N_A = D_n \times N_D \quad (2.2)$$

The behavior of the P-N junction with respect to the potential barrier's width produces an asymmetrical conducting two terminal device, called P-N junction diode; the main feature of which is a non-linear current-voltage relationship.

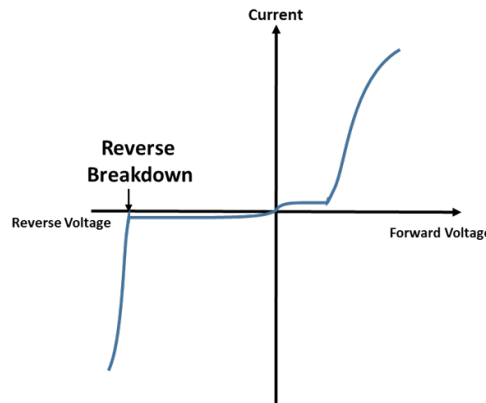


Figure 2.3. – Static I-V Characteristics of P-N junction

When the diode is connected under forward bias conditions, a negative voltage is applied to the n-type material and a positive voltage is applied to the p-type material. If this external voltage is greater than the value of the barrier (silicon is about 0.7 V), the potential barriers will be overcome and large current will start to flow, as shown in Figure 2.3.

When the diode is connected under reverse bias conditions, a positive voltage is applied to the n-type material and a negative voltage is applied to the p-type material. A positive voltage applied to the n-type material attracts electrons to the positive electrode and away from the junction, while the holes on the p-type end also attract the negative electrode from the junction. The result is that the depletion layer becomes wider due to the lack of electrons and holes and the silicon can almost act like an insulator. This effect is required to increase the detection volume and reduce the capacitance. If the reverse bias voltage V applied to the diode is increased to a sufficiently high value, it will cause the diode's p-n junction to overheat and fail due to an avalanche effect around the junction. This can cause the diode to be shorted and cause a maximum circuit current flow, which is shown as a downward slope in the reverse static characteristic in Figure 2.3.

2.2. The silicon sensor principle

Detection of ionizing particles by a reversely biased semiconductor junction was first reported over 60 years [46]. In a reversed bias silicon p-n junction, charge carriers generated by ionizing radiation or particles are separated by the existing electric field and collected on an electrode. Since there are no free carriers in the depleted silicon, the recombination process between opposite sign carriers can be mitigated drastically (collection time > recombination time). The moving charges produce a current pulse on the electrode. Figure 2.4 shows a simple pixel sensor architecture in an n-type substrate. The p+ implantation on

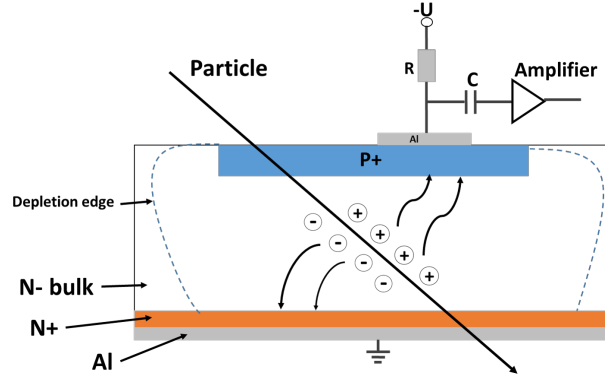


Figure 2.4. – The sketch of a particle traversing a silicon sensor

the top side forms one electrode and is biased at a negative voltage; the n+ implantation on the backside forms an ohmic contact to the ground. The ionized electrons from the striking particles drift downward and the holes drift toward the topside. The induced signal at the top electrode is then transmitted to a readout chip.

The time required to detect the entire signal depends on the drift path length and the electric field strength. In fact, by solving the one-dimensional Poisson equation, the depletion width and electric field of the depletion region can be calculated. Assuming a p-n junction with constant doping concentrations on both sides, the total depletion width can be obtained by [48]:

$$d = x_n + x_p = \sqrt{\frac{2\varepsilon_0\varepsilon_r}{e} \left(\frac{1}{N_A} + \frac{1}{N_D} \right) (V + V_{bi})} \quad (2.3)$$

where V is the applied reverse voltage, V_{bi} is built-in voltage, x_n and x_p are the parts of d on the n and p side with concentrations N_D and N_A respectively.

In most practical cases to make a detector out of doped silicon, the sensor is abrupt p-n junction. If we take as a practical example a p+ n junction, with $N_D > 10^{18} \text{ cm}^{-3}$ and $N_A = 10^{13} \text{ cm}^{-3}$, the term $1/N_D$ in equation (2.3) can be neglected. So the space charge region extends deeper towards the lower doped side of the junction. In addition, the built-in voltage V_{bi} is small compared to the typical operating external voltage and can be neglected as well. Therefore, the total width d of the depletion region can be simplified:

$$d \approx x_n \approx \sqrt{\frac{2\varepsilon_0\varepsilon_r}{eN} V} \quad (2.4)$$

The concentration N is in inverse proportion to the resistivity of the silicon. So the width of the depletion region can be also described as:

$$d \propto \sqrt{\rho V} \quad (2.5)$$

where the ρ is the silicon resistivity. Equation (2.5) indicates that the depletion width is proportional to the silicon resistivity and the reverse bias of the junction and the increasing the value of one of these parameter will expand the depletion region.

Many semiconductor detectors operate with sufficient reverse bias so that the depletion region extends across the entire wafer thickness to form a fully depleted detector. Fully depletion is required because the charge generated in the depleted zone can drift to the electrode and be collected, while the charge generated in the non-depleted region immediately recombines with the free majority carrier and is lost.

The full depletion voltage $V_{fulldep}$ can be re-expressed from equation (2.4) as a function of the wafer thickness T:

$$V_{fulldep} = \frac{eNT^2}{2\varepsilon} \quad (2.6)$$

where N is the dopant concentration on the weakly doped side of the junction, ε is the dielectric constant for silicon. The full depletion voltage is an important parameter of the sensor. If the applied bias voltage is over the full depletion voltage, the device is said to be over-depleted.

2.3. Particles interaction with matter

The electromagnetic interaction plays a main role when charged light particles cross matter. Charged particles travelling through matter can initiate the following processes: ionization of atoms, excitation of atoms, bremsstrahlung, cherenkov radiation, transition radiation e.g. These processes can lead to energy loss of charged particles. The relative contribution of these various processes to the total energy loss depends on the kinetic energy of the particle, the detector material, etc. The mean rate of energy loss (stopping power) of a heavy charged particle is given by the Bethe-Bloch formula [49]

$$-\left\langle \frac{dE}{dx} \right\rangle = \frac{4\pi r_e^2 m_e c^2 N_A z^2 Z}{A\beta^2} \times \left[\frac{1}{2} \ln \frac{2m_e c^2 \beta^2 \gamma^2 T_{max}}{I^2} - \beta^2 - \frac{\delta(\beta\gamma)}{2} \right] \quad (2.7)$$

where Z and A are the atomic and mass number of the material, N_A is the Avogadro constant, r_e is the classical electron radius, z is the charge of the traversing particle in units of electron charge, $m_e c^2$ is the rest energy (0.511 MeV) of the electron, β is the velocity of the traversing particle in units of the speed of light, γ is the Lorentz factor ($1/\sqrt{1-\beta^2}$), I is the mean excitation energy of the material (173 eV for silicon), and T_{max} is the maximum kinetic energy transfer to an electron, $\delta(\beta\gamma)$ is density effect correction to ionisation loss.

According to the equation, the stopping power (dE/dx) follows three general

properties. The first one, stopping power is independent of the mass of the incident particle, because there is not showing the mass of the incident particle in this formula. The second one, stopping power depends on the charge of the incident particle z . The last general property, if we treat the slowly varying logarithmic term as a constant, the stopping power can be considered proportional to the $1/\beta^2$.

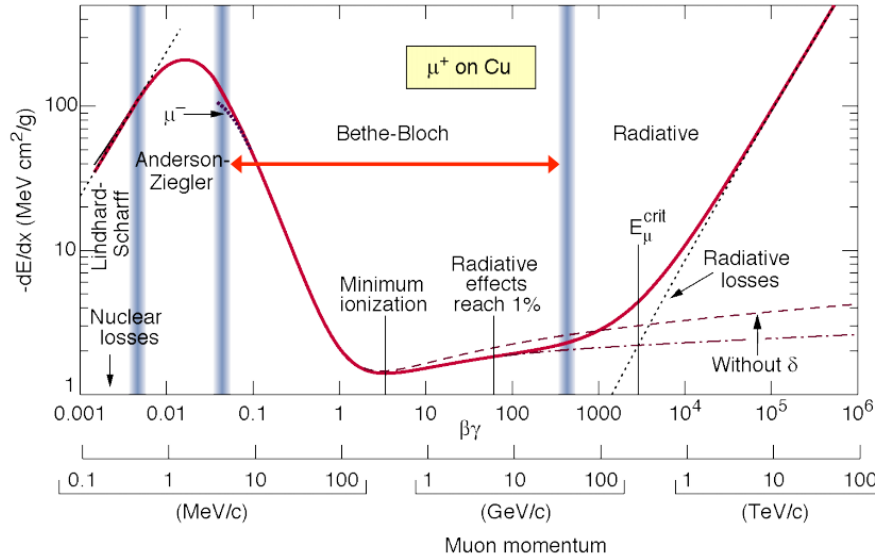


Figure 2.5. – Total energy loss $-dE/dx$ for muons in copper

Figure 2.5 shows an example of the stopping power of positive muon in copper as a function of $\beta\gamma$ over nine orders of magnitude in momentum [50] [51]. For the low energy region ($\beta\gamma \leq 3$), it is apparent from the figure that the stopping power decreases with increasing energy. A minimum stopping power is reached when $\beta\gamma=3$, this point is usually named Minimum Ionizing Particles (MIP). For momentum of muon higher than the MIP's momentum, the stopping power increases weakly for increasing momentum, so most of the charged particles to be detected in high energy experiments can be approximated as MIPs.

The energy loss is a statistical process due to the number of collisions and energy loss varying from particle to particle. In a thin layer of matter, the fluctuations of energy loss by ionization of a charged particle was theoretically described by Landau in 1944 [52], resulting a long tail distribution which is called Landau distribution. This behavior is more common in thin layer of matter because of the large fluctuations in the various processes of energy transfer due to the few collisions expected [53]. Examples of the Landau distribution based on calculations by Bichsel [54] [55] [56] are shown in Figure 2.6. The peak of Landau distribution is called the Most Probable Value (MPV) of the distribution, and is smaller than mean energy loss due to the presence of the high energy tail accounting for the ionizing released by δ -electron [53], which is typical number

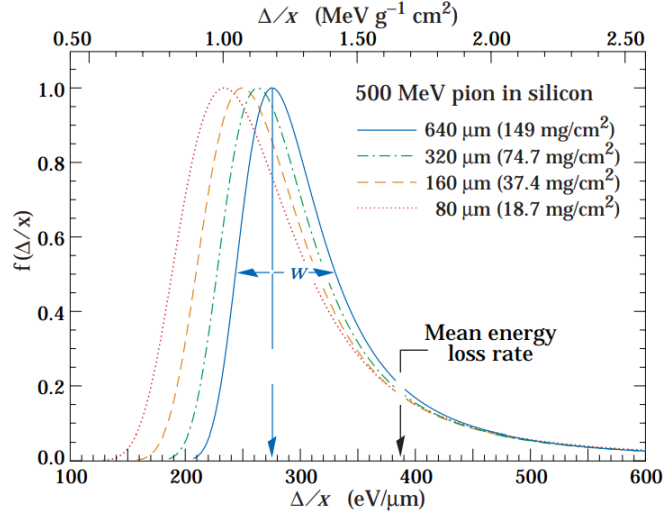


Figure 2.6. – Landau distribution in silicon for 500 MeV pions (the width w is the full width at half maximum)

of electron and hole pairs per μm generated by a MIP in a detector made of silicon.

2.4. Radiation effects and damage

The effects of radiation in silicon can be classified into two groups, cumulative effects and single event effects. Cumulative effects take place through the whole lifetime of the device, which is exposed in a radiation zone; cumulative effects include ionizing effects and non-ionizing effects. Single event effects are caused by one single particle in the readout electronic; they can be happened at any time, and their probability is expressed by cross-section. The single event effects contain non-destructive effects and destructive effects. Figure 2.7 shows the radiation effect classes.

2.4.1. Cumulative effects

Cumulative effects gradually change the behavior of the device when it is exposed to radiation. In other words, cumulative effects increasingly affect the behavior of the devices throughout the exposure time and degrade the devices' characteristics.

2.4.1.1. Ionizing effects

In silicon device, the high energy particles passing through the silicon dioxide produce defects in the oxide layer. As the crystal structure of silicon oxide is

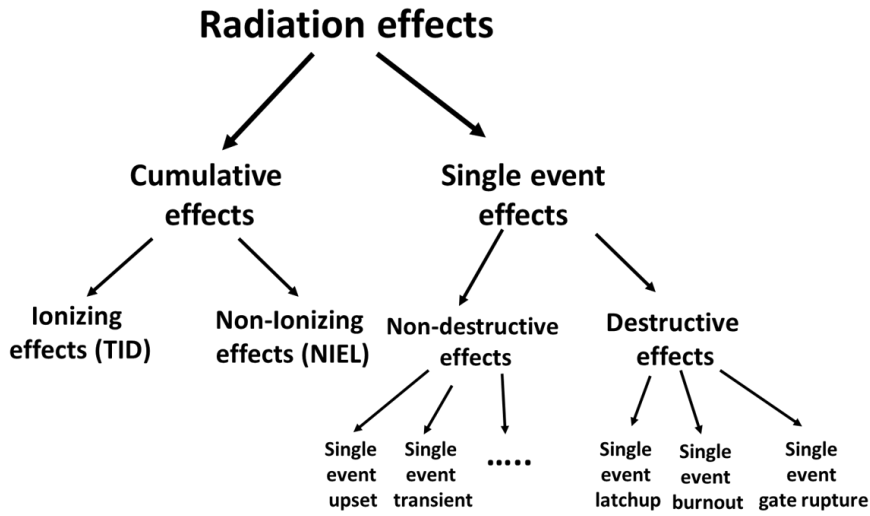


Figure 2.7. – The radiation effects classes

highly irregular, displacements of silicon atoms due to irradiation do not play the major role here; the cumulative damage, which is caused by ionizing radiation over the exposition time, plays the main role. The creation of electron-holes pair in the surface region causes long-term effects in the oxide, we usually use the Total Ionizing Dose (TID) which defines this effect. The total ionizing dose (TID) can be measured in terms of the absorbed dose, which is a measure of the energy absorbed by matter. Absorbed dose is quantified using either a unit called the Rad (radiation absorbed dose) or the SI unit which is the Gray (Gy) (1 Gy = 100 Rads).

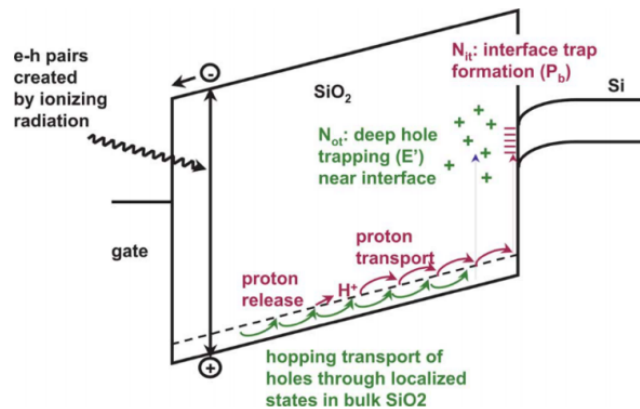


Figure 2.8. – Schematic energy band diagram for NMOS structure, indicating major physical processes underlying TID effects

In CMOS sensor, the MOSFETs is the basic building block of the circuits and the most sensitive part in MOSFETs is the oxide insulators. Figure 2.8 shows a

schematic energy band diagram of a NMOS structure [57]; this is a vertical cut through a transistor structure. The radiation creates electron hole pairs in the SiO_2 bulk, and the positive bias is applied to the gate of NMOS transistor, so that electrons flow toward the gate and holes move to the Si substrate. During this charge carrier displacement, most electron-hole pairs recombine immediately, after that, as electrons have high mobility in the oxide, in other words, the electrons can be removed quickly, they will be collected by the positively biased electrode. By contrast, the holes have a much lower mobility in the oxide, so they move very slowly to the interface in the direction of the electric field in the oxide, hopping from one shallow trap into the next as shown by these arrows on the bottom of Figure 2.8. As we know that there are large amounts of deep level traps, which is called oxide traps near the SiO_2 and silicon interface; ionizing radiation causes the density of these traps to increase and modify their energy distribution, giving rise to radiation induced oxide traps, hence new energy levels are introduced in the band gap near the Si- SiO_2 interface. Once the holes get close to the interface, they can be captured by these oxide traps, which are located somewhere in the middle of the bandgap, so we call them deep level traps. The holes get quasi-permanently trapped in these locations and cannot be moved easily any more. At the same time of oxide traps build up, hydrogen ions (protons) can be released in the oxide bulk as holes transport toward the interface through the oxide. Those protons can drift to the Si/ SiO_2 interface under positive gate bias where they may react with Si-H to form H_2 , leaving silicon dangling bonds at the interface. These dangling bonds can act as interface traps, as shown in red at the Figure 2.8 bottom. The trapped positive charges affect the localized fields and further affect the device characteristics.

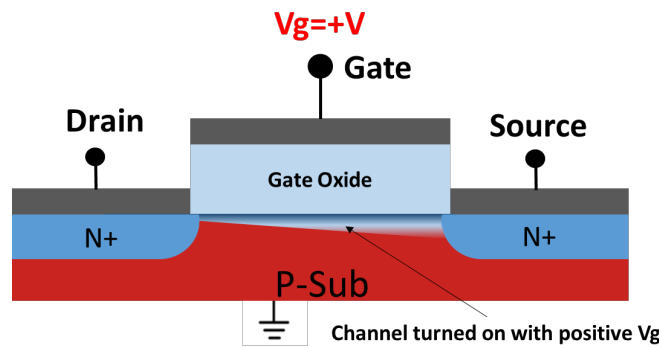


Figure 2.9. – Schematic of n-channel MOSFET: normal operation

The diagram of an NMOS device is shown in Figure 2.9; it is a four terminal device: gate, drain, source, body. The drain and source are heavily doped n type region, between them is p-type materials or hole-rich materials. Once the positive gate voltage is applied and then the surface layer is inverted from p-type to n-type, we get the high concentration of electrons because of the field

effect under the gate and then the high conductivity channel is built between the source and drain. Electric current can flow freely between the source and drain, the transistor is on, the gate voltage controls the electrons concentration in the channel.

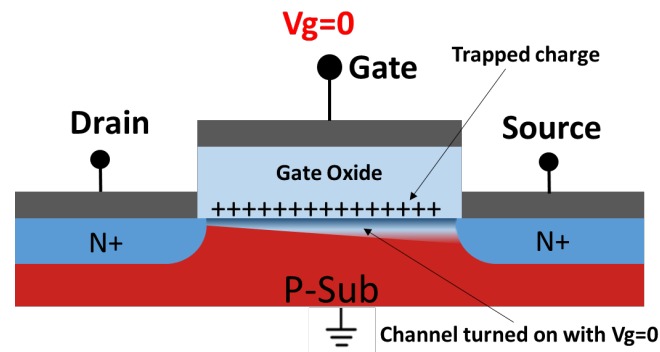


Figure 2.10. – Schematic of n-channel MOSFET: post-irradiation operation

As shown before, when the transistor is exposed in a radiation environment, the holes which are created by the particles would be trapped in deep level traps near the interface of the silicon dioxide, as shown in Figure 2.10. These positive charges attract electrons in the silicon near the interface, which can cause a shift in the threshold voltage, and then the transistor can be turned on even at zero volts applied. TID effects hence make the NMOS transistor harder to turn off at first with exposure to radiation, with the exposure going on, the transistor could be not work any more at some point. It is well known that the TID effects in MOS transistor not only cause the holes in the oxide but also the interface traps. For NMOS transistor, the oxide and interface-trapped charges are opposite in sign, as shown in Figure 2.8, so the charges built by interface traps can compensate the charges from oxide holes. In NMOS, the oxide-trapped holes induce a negative V_{th} shift while the interface traps cause a positive V_{th} shift, as shown in Figure 2.11.

As shown in Figure 2.12, PMOS devices have sources and drains made of p+ implants, in this case, the drain and source are holes enriched, which are heavily doped p-type region, and the body or substrate is n-type material. When we apply a the negative gate voltage, the electrons, which are under the oxide layer, would be pushed downward into the substrate, then leave the bound positive charges which are associated with the donor atoms in the silicon thin layer near the interface. The channel is created and the transistor is on with a negative gate voltage.

TID effect creates positive charges, which are trapped in the silicon dioxide near the interface and attract the electrons in the silicon channel layer, as shown in Figure 2.13. These trapped charge tend to push the V_{th} more negative. With radiation dose increasing, the transistor becomes harder and harder to turn on.

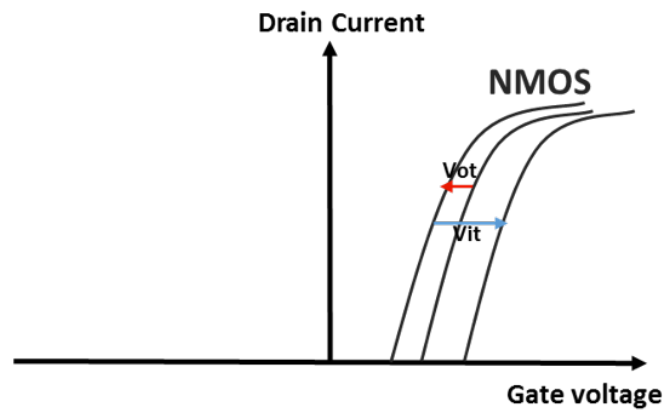


Figure 2.11. – Threshold-voltage shifts in NMOS transistors

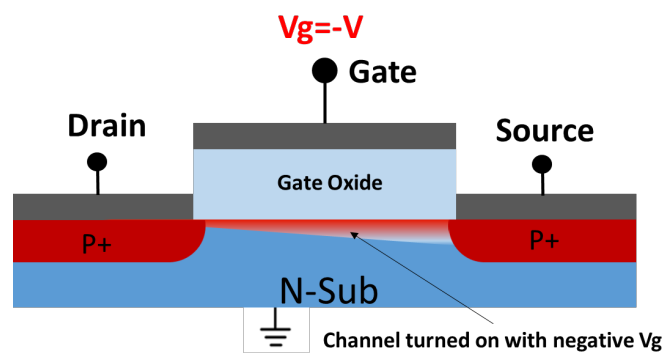


Figure 2.12. – Schematic of p-channel MOSFET: normal operation

At the same time, the interface traps also catch the charges which can affect the V_{th} as well. For PMOS transistor, the oxide and interface trapped charges are same in sign, so the interface trapped charges also push the V_{th} more negative, as shown in Figure 2.14.

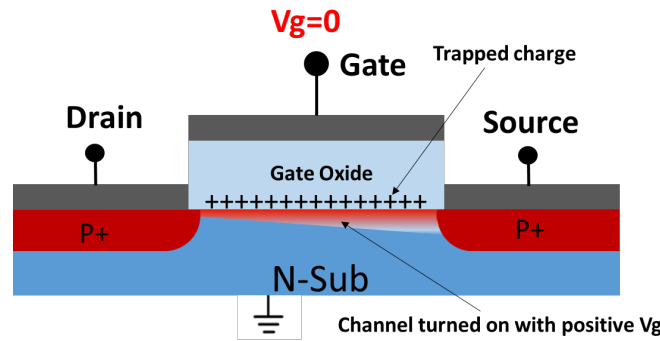


Figure 2.13. – Schematic of p-channel MOSFET: post-irradiation operation

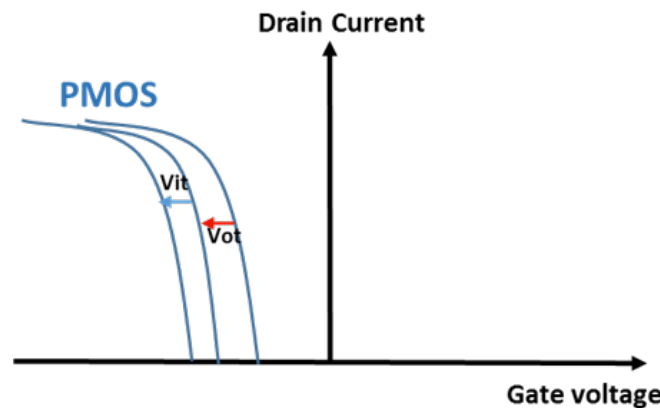


Figure 2.14. – Threshold-voltage shifts in PMOS transistors

TID effects do not only affect the gate oxide, but also all type of oxides in the device. In particular, the Shallow Trench Isolation (STI) is the typical isolation technology used between transistors for the sub $0.5 \mu m$ technology. In this technique, a shallow trench is etched into the silicon substrate, and then a thermal oxide in the trench is grown. In Figure 2.15 [58], we can see that there are two pathways to leak the charge, which are defined by the red and blue arrows. The red leakage current pathway is near the transistor sidewall isolation, Figure 2.16 illustrates the radiation effect on STI isolation. Before radiation, the current goes simply from drain to source when a positive gate voltage is applied. After radiation, oxide and interface charges appear near the side wall of the transistor and attract electrons in the p-type substrate and then create a conductive path between drain and source, as shown red arrow in Figure 2.15. Since this red

area is relatively large region, and a lot of charges accumulate at the interface of STI and p-type substrate, then the second pathway can be created under the STI isolation between the transistors which is shown in black arrow in Figure 2.15.

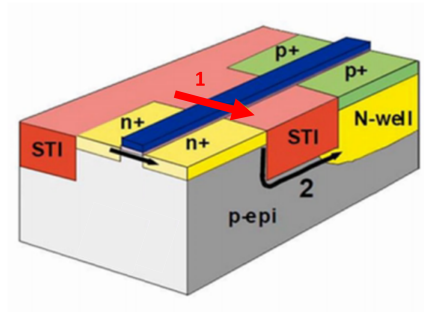


Figure 2.15. – TID induced leakage current of the CMOS circuits

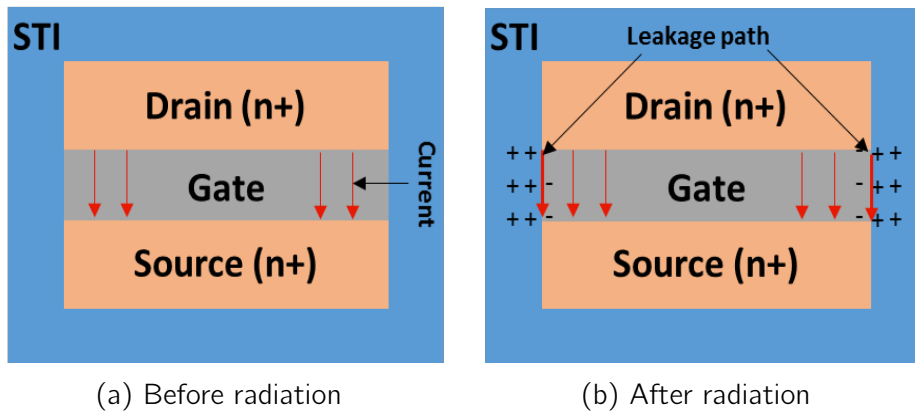


Figure 2.16. – Induced leakage current related to STI isolation

A common way to prevent the leakage current in the device, which is induced by the TID effect, is to implement a so-called the Enclosed Layout Transistor (ELT) in replacement of the standard transistor layout [59] [60], as shown in Figure 2.17. In the enclosed transistor design, the STI isolation does not face the gate channel directly, so the leakage current can be mitigated [61]. However, the enclosed transistor design has several disadvantages compared to standard transistor design: complex model of transistor behavior, larger area consumption, and bigger parasitic capacitances.

Indeed, in modern CMOS technology, the oxide layer is mostly less than 20 nm, so not so much charge can be accumulated in such thin oxide layer, so essentially, the leakage current dominates in the TID effects.

As well known, the different particles will produce different extent of TID effects. Since the electrons drift away from the oxide very rapidly in a time on the order of a picosecond, some fraction of them recombine with the holes within

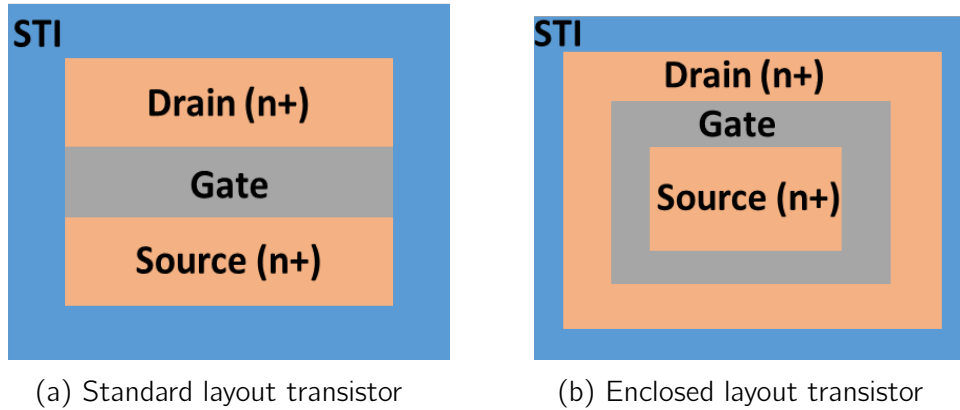


Figure 2.17. – The comparison between standard and enclosed layout transistor

this short time, and the left holes in the oxide play the main role of TID effects. In order to know the TID efficiency of different radiations, Figure 2.18 [57] gives the fractional hole yield as a function of applied field for a variety of incident particles, the horizontal axis is the electric field and the fraction yield is shown on vertical axis. From this figure, the 12-MeV electrons and Cobalt 60, which is gamma ray, are very efficient and close to 100 percent fractional yield can be reached independent of electric field. In other words, the charge generated during the irradiation, most of it stays in the oxide. In terms of some heavy particle source, the fractional yield drops rapidly, the charge yield is only 35 percent left at 2 MV/cm for the 700-keV protons, and the alpha particles is only 12 percent trapped in the silicon dioxide at 2 MV/cm. Clearly, recombination is an important effect, which must be accounted for, when comparing the effect of different radiation source.

2.4.1.2. Non-Ionizing effects

As we discussed above, the TID effects play a main role in surface transistors of the device. But Non-Ionizing effects dominate in the bulk of the device. Non-Ionizing effects disrupt the crystalline arrangement of the atoms in the lattice of the irradiated material. The amount of the energy lost related to the atom displacement by the passing through particles in the material, is described by the Non Ionizing Energy Loss (NIEL) model. In other words, NIEL is the energy that the particles deposit inside the material, which triggers displacement process. NIEL is commonly expressed in units of $\text{MeV cm}^2/\text{g}$ or NIEL cross section in units of MeV mb . It can be also described by a reference value to the damage given by 1 MeV neutron equivalent (n_{eq}) at 1 cm^2 of detector surface; for example, 1 MeV neutron NIEL is equivalent to 95 MeV mb.

Non-ionizing effects triggered in silicon detector by hadrons (e.g. neutrons, protons, pions...) is mainly caused by the displacement of a Primary Knocked

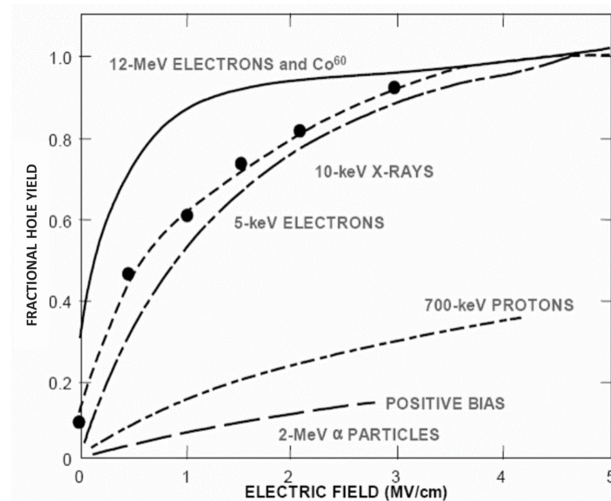


Figure 2.18. – Charge yield for various radiation sources, for a number of incident particles

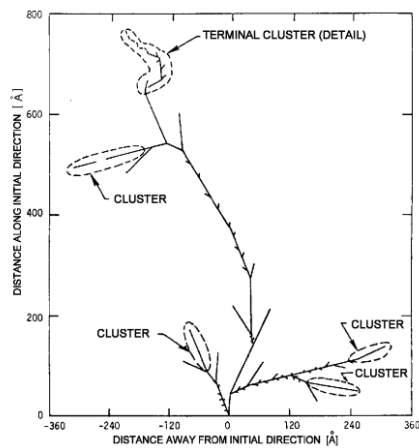


Figure 2.19. – Monte Carlo simulation of a recoil-atom track with a primary energy of 50 keV

on Atom (PKA) out of its silicon lattice position which then results in a silicon interstitial and a left over vacancy. Figure 2.19 shows Monte Carlo simulation of a recoil-atom track with a primary energy of 50 keV [62]. In this simulation, there are two competing contributions to the energy loss following the pathway of these recoils, one is the contribution of the ionization, which is around 37% of the total recoils energy loss and the other contribution is related to NIEL effects, which plays a main role in this process. At the end of the process, many disordered area or cluster (defects) are formed in the lattice, the induced defects in the silicon lattice form energy levels in the silicon bandgap, these additional energy levels have consequences on the device performance in various ways. Generally, there are three main effects on the device performance: leakage current, a modification of the effective space charge and charge trapping [63].

The first main effects on the device performance level is the leakage current. The leakage current is affected very much by the defects energy level near the middle of the bandgap. The leakage current is also an important characteristics of the silicon detector and has consequences on the readout IC, the increasing leakage current leads to a rising of the noise in the amplifiers and the power consumption as well. The defects levels can produce leakage current by electron and hole emission. Concerning all types of defects and taking into account the depletion region of the sensor, the total leakage current is given as

$$I = q_0 \omega A \sum_{defects} G_i \quad (2.8)$$

where the G_i is the generation rate of a single defect, the q_0 is the elementary charge and the ω and A is depletion width and area respectively. It is well known that the leakage current is depending on the temperature and is given as

$$I_{leakage} \propto T^2 e^{-E_g(T)/2kT} \quad (2.9)$$

From this equation, we see that the leakage current exponentially changes with the temperature. So cooling the device is an effective way to keep the leakage current low.

The second main effects on the device performance is the effective space charge. The defects created by particles can contribute to the space charge in the silicon bulk, the positive charge acts as donor and negative charge acts as acceptor. Positive or negative charge affect the electric field distribution in the device and an increase in depletion voltage due to increasing effective doping concentration. In order to maintain the depletion region as unirradiated after radiation, guard-ring structure are often used at the edge of the sensor, it could reduce the electric field value and increase the breakdown voltage and then more reverse biasing voltage could apply on the sensor. As an example in Figure 2.20 [64], we can see how the space-charge sign changes from negative to positive with increasing radiation fluence for an n-type silicon sensor.

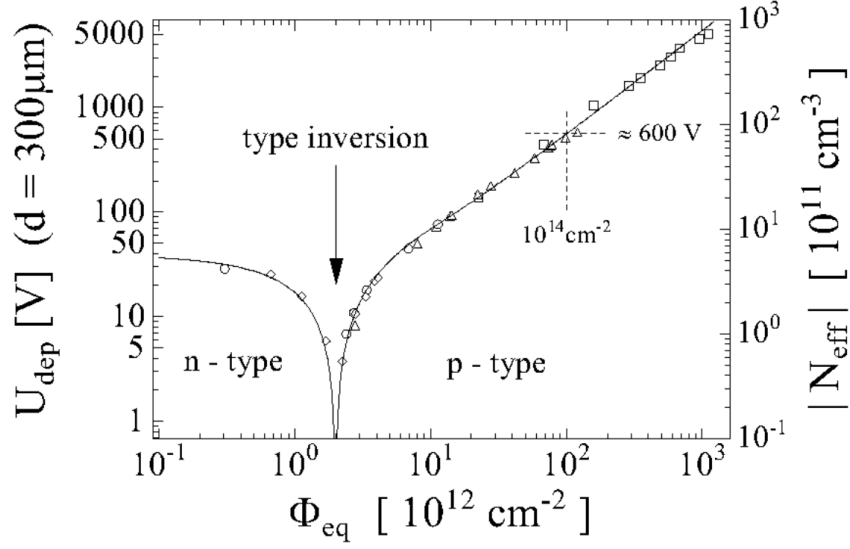


Figure 2.20. – Effective doping concentration as a function of 1 MeV neutron equivalent fluence for n-type silicon

The last main effect on the device performance is charge trapping. The defects that have been created by radiation can capture the charge carriers and release them only after a certain time. If the releasing time is longer than the standard charge collection time, it reduces the overall number of charges that can be collected on the electrode.

Non-ionizing damage induced by different particles and different energies can be related by the NIEL scaling hypothesis [65]. The NIEL scaling hypothesis states that the radiation effects scale linearly with the NIEL value regardless of distribution of the primary displacements over energy and space. In other words, according to the hypothesis that the concentration of the defects, which are created by the displacement radiation effects, is independent of the properties of the particles, essentially the amount of the defects is proportional to the NIEL. The displacement damage cross section is described by [66]:

$$D(E_p) = \sum_i \sigma_i(E_p) \int_0^{E_{Rmax}} f_i(E_p, E_R) P(E_R) dE_R \quad (2.10)$$

Here the index i indicates all interactions possibility between the striking particle with energy E_p and the silicon atoms in the crystal, which is leading to displacements in the silicon lattice. σ_i is the cross section regarding the reaction with index i . $f_i(E_p, E_R)$ shows the probability for the generation of a PKA with recoil energy E_R by a particle with energy E_p undergoing the indicated reaction i . The equation is integrating all possible recoil energies E_R (from 0 to E_{Rmax}).

As shown in Figure 2.21 [67] [68] [69], the displacement damage function D

is described to calculate the 1 MeV neutron equivalent fluence radiation in the experiments of the LHC and HL-LHC. According to this plot, the NIEL value is around 100 MeV mb for 1 MeV neutrons and 60 MeV mb for 24 GeV protons, therefore the NIEL value which related to 1 MeV neutrons is nearly 1.7 times higher than for 24 GeV proton. In other words, we have to implement 1.7 times as many 24 GeV protons to reach the same damage as with 1 MeV neutrons. The NIEL method provides an easy way to compare the radiation damage with different particles and energy.

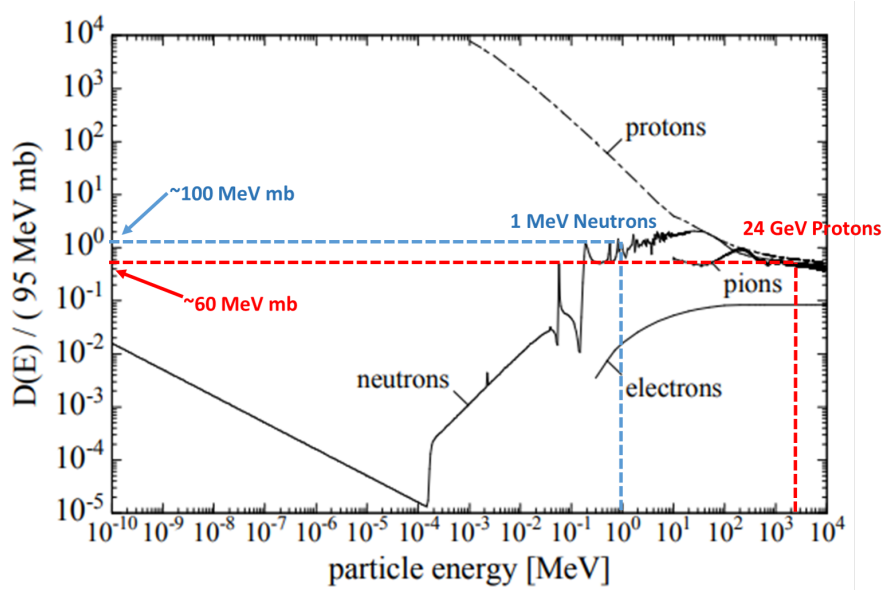


Figure 2.21. – The NIEL value of neutrons, protons, pions and electrons in silicon at different energies related to 1 MeV neutron equivalent fluence radiation

2.4.2. Single Event Effects

Single Event Effects (SEE) are caused by one single ionizing particle (ions, electrons, photons...) striking a sensitive node in a digital structure of a microelectronic circuit. We can separate these effects into two groups, non-destructive effects and destructive effects. Some Single Event Effect categories are listed in table 2.1.

2.4.2.1. Non-destructive effects

Non-destructive effects normally create “soft” error due a transient charge collection on a sensitive node. This type of error has for consequence a state change, without hardware damage and the original state may be hopefully recovered (of

Non-destructive effects	Destructive effects
SEU, Single Event Upset	SEL, Single-Event Latchup
MBU, MCU Multiple Bit (or Cell) Upset	SEHE, Single Event Hard Errors
ASET, Analog Single Event Transient	SEDR, Single-Event Dielectric Rupture
DSET, Digital Single Event Transient	SEB, Single-Event Burnout
SEFI, Single Event Functional Interrupt	SEGR, Single-Event Gate Rupture
...	...

Table 2.1. – Some categories of SEE

course this depends on implementation) by a reset, a power cycle or simply by rewriting the information. Single Event Upsets (SEUs) are one of the most common non-destructive effects. Every device having SRAM cells is a candidate to show SEUs, for example, Microprocessors, FPGAs, or custom made ASICs, etc. A SEU is a bit flip in a SRAM in the device. These upsets occur randomly but should not damage the device.

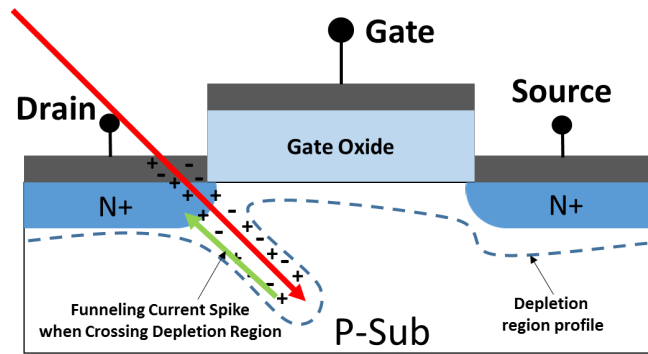


Figure 2.22. – Charged particle strikes NMOS transistor

As the charged particle strikes through the various material layers in a semiconductor device, it creates an ionization path with free electrons and holes. Generally, these electron hole pairs would recombine immediately. However, when the pathway goes through the depletion region under the drain-gate-source region, the electrons it creates can be attracted quickly to a higher voltage NMOS drain diffusion, which sometimes results in the change of state of a storage element, as shown in Figure 2.22 [70].

A simple SEU example is in the SRAM cell shown in the Figure 2.23. Imaging a SRAM holds the state high at node 1 in picture 2.23. A striking particle in region of the drain of the OFF NMOS might generate enough charges to change this state temporarily to 0. Before the charge transmits to the power supply through the transistor of this inverter, the second inverter might switch with the input

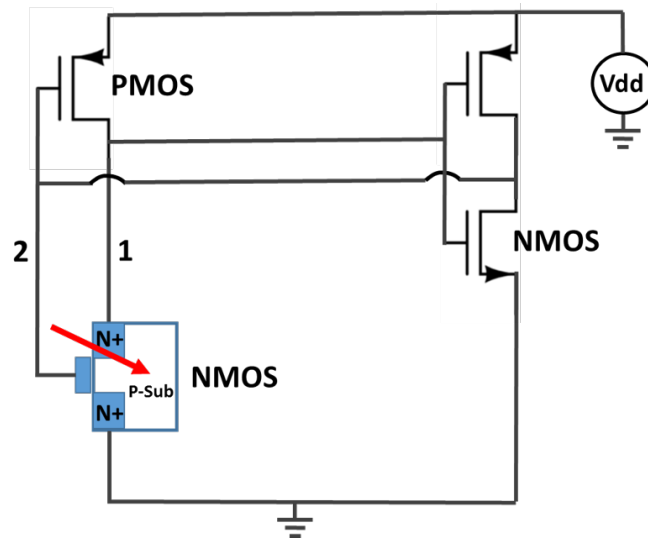


Figure 2.23. – A SEU example in the SRAM cell

from node 1. This changes the node 2 state, which in turn forces the wrong state at node 1 and then the error is saved in the memory cell in this way. There are many techniques that can be used to mitigate the SEU effects at the design level. These techniques consist Error Correction Codes (ECC), Cyclic Redundancy Check (CRC), and Triple Modular Redundancy (TMR).

2.4.2.2. Destructive effects

Destructive effects can occur through various mechanisms including Single Event Latch-up (SEL), Single Event Burnout (SEB) and Single Event Gate Rupture (SEGR). SEL is one important and common Single Event Effect, which can cause permanent damage to the device.

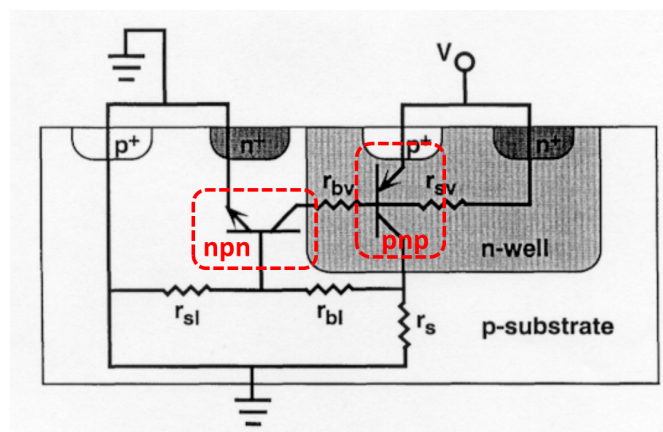


Figure 2.24. – The simple two transistor model in CMOS technology

In a CMOS technology, due to the physical implementation of the devices, there exists 2 parasitic transistors as shown in Figure 2.24 [71]. The two parasitic bipolar transistors are interconnected, so the collector current of each BJT (Bipolar Junction Transistor) feeds the base current of the other. In this model, an increasing current in pnp collector can offer an increase in the npn base current. This in turn increases the collector current of the npn, which gives an increase in the pnp base current. This positive feedback is such that, if the overall gain of the thyristor pnpn is high enough, any particles striking turning on one of the parasitic BJT structures can lead the latchup. If it is not immediately interrupted, this latchup can lead to a permanent damage of the device.

The most effective way to mitigate the SEL effect is decreasing the gain of the parasitic BJT. This can be done at the level of the physical layers implementation (technological solution) or at the level of the custom ASIC layout. In terms of a technological solution, epitaxial substrates and retrograde wells can be used to reduce or suppress SEL probability. Epitaxial substrates can limit the depth of the charge collection area when a particle strike and hence limit the current flow. The use of retrograde wells makes a lower resistance path from every point in the circuit to Vdd possible. Trench isolation can drastically shrink the gain of the lateral parasitic BJT. In terms of layout, the use of guard rings and increasing the distance between complementary devices can be implemented. We can also increase the distance between complementary devices to decrease the gain of the lateral parasitic transistor.

3. Pixel detector for the ATLAS ITk Outermost Pixel Layer upgrade

The HL-LHC will operate with a center of mass energy of 14 TeV and a peak instantaneous luminosity of $7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$, five times higher than at present. The increased luminosity will result in roughly ten times higher radiation levels and data rates. The current Inner Tracker (ITk) of the ATLAS detector will be entirely replaced by an full-silicon tracking system and the new ATLAS ITk Pixel Detector will consist in a silicon-based 5-layer cylinder with endcaps, as shown in Figure 3.1 [45]. The technology baseline for the inner 5 layers (L0 to L4) consists of hybrid pixel detectors. In the L4 layer, the Non-Ionizing Energy Loss (NIEL) and Total Ionizing Dose (TID) through the 10 year lifetime of the HL-LHC environment will be $10^{15} \text{ n}_{eq}/\text{cm}^2$ and 80 MRad respectively. Thus the sensors and the electronics in this layer do not require the high level of radiation hardness needed in the innermost layers of the HL-LHC environment. For the outer layer an alternative technological option exists or in other applications: a fully monolithic depleted-CMOS concept. In this concept, the sensor and the readout logic circuitry are integrated into a single chip. Sharing the same silicon substrate, on top of an important potential for material budget reduction, one important advantage of this approach relates to the use of a commercial process, which enables low cost and easy procurement. Furthermore, the use of a monolithic concept translates in simpler production steps (e.g. no bump-bonding) and smaller pixels, savings in production time. In this chapter, both hybrid pixel detector and monolithic depleted-CMOS pixel detector will be discussed.

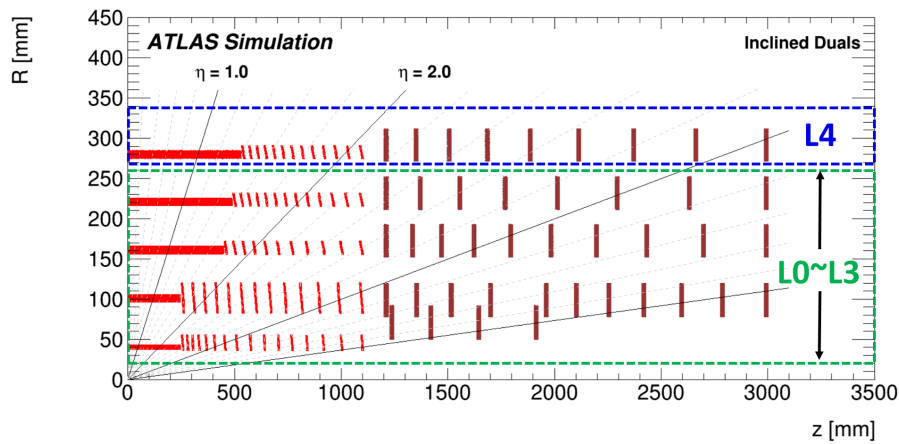


Figure 3.1. – A schematic layout of the ITk Pixel Detector

3.1. Requirements for the ITk pixel sensors upgrade

Due to the increased luminosity and the associated increase in the rate of proton-proton collisions, the expected radiation levels in the ATLAS ITk will increase by roughly an order of magnitude compared to the present Inner Detector.

3.1.1. Radiation level

The predictions of particle fluences and ionising doses for the ITk layout assume an integrated luminosity of 4000 fb^{-1} at a centre-of-mass energy 14 TeV. In Figure 3.2 the simulation fluence and dose distributions for the Pixel Detector are shown. These two plots of 1 MeV neutron equivalent fluences and dose are normalised to 4000 fb^{-1} .

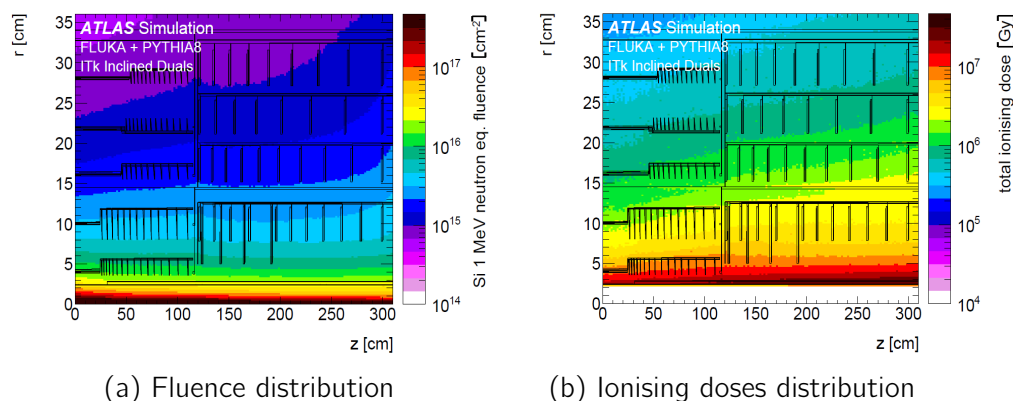


Figure 3.2. – The fluence and dose distributions for the ITk Pixel Detector.

In the baseline scenario, the outer pixel barrel and end-cap detector will be operated to collect a total integrated luminosity of up to 4000 fb^{-1} , while the inner barrel and endcaps will be replaced after 2000 fb^{-1} . This means that the devices installed in Layer 0 must be radiation hard up to a dose of 1 GRad. To deliver high track reconstruction and a low rate of fake tracks, the ITk is designed with efficient pattern recognition and track reconstruction. A summary of the maximum neutron fluences and the ionising dose levels are given in Table 3.1 for these conditions [45]. A minimum detection efficiency of 97% is required within all of the technologies under consideration [72].

3.1.2. Trigger scheme

At the start of HL-LHC operation, the ATLAS Detector will be read out with a single Level-0 trigger (L0) running at an average rate of 1 MHz with a maximum

Luminosity	Layer	Location	R (cm)	z (cm)	Fluence ($10^{14}n_{eq}/cm^2$)	Dose (MGy)
2000 fb^{-1}	0	flat barrels	3.9	0.0	131	-
			4.0	24.3	-	7.2
		inclined barrel	3.7	25.9	123	-
			3.7	110.0	-	9.9
		end-cap	5.1	123.8	68	6.3
2000 fb^{-1}	1	flat barrels	9.9	24.3	27	1.5
		inclined barrel	8.1	110.0	35	2.9
		end-cap	7.9	299.2	38	3.2
4000 fb^{-1}	2-4	flat barrels	16.0	44.6	28	1.6
		inclined barrel	15.6	110.0	30	2.0
		end-cap	15.3	299.2	38	3.5

Table 3.1. – The maximal neutron fluences and total ionising dose levels for different parts of the Inner Track (ITk) Pixel Detector

latency of $10\text{ }\mu\text{s}$. The ITk Detector will be able to deliver data to a fast track reconstruction processor that will deliver track parameters as the input to High Level Trigger processing (HLT) [73]. This trigger architecture is called "L0-only" and is considered to be the baseline for ATLAS. An alternative architecture is considered, that makes it possible to use ITk data in the first part of the trigger decision. This hierarchical scheme uses an additional level of trigger, called Level-1 (L1), and it is called "L0-L1". In the L0-L1 scheme, the L0 trigger generated, as in the L0-only scheme, using also calorimeter and muon spectrometer data, is dispatched to all the detector elements that will provide data for the track trigger or in the refinement of the L0 muon or calorimetric decision. It is possible to send the L0 trigger only to a specific "Region of Interest" (RoI) identified as a part of the L0 decision. L0 will have a maximum rate of 4 MHz and a maximum latency of $10\text{ }\mu\text{s}$. The Level-1 trigger, formed with calorimeters, muon spectrometer and tracker data, will have a maximum frequency of 800 kHz and a maximum latency of $35\text{ }\mu\text{s}$ [45].

The full ITk will be read out at L0 in the "L0-only" scheme. In the "L0-L1" scheme, different strategies will be employed in the different ITk sub-detectors. In particular, the three outer pixel layers, barrel and end-caps, will support full read-out at 4 MHz. For the two inner pixel layers full read-out at 4 MHz would require a prohibitive number of data cables; this part of the detector will only support full read-out at 1 MHz, and will be read out at L1. As a consequence, the data from the two inner layers will not be available at the track trigger processor to build the L1 decision, that will be based on Strips (inside the RoI) and outer pixel layers [45].

3.1.3. Material budget

The largest source of multiple scattering in the current ITk layouts comes from cooling pipes and electrical services connecting the end-cap layers to the outer boundaries of the ITk volume. The huge number of modules in the pixel detector would require a big amount of cables with an increased cross section with respect to the current system due to the higher power consumption of the new readout chips [74]. Therefore a new powering approach called Serial Powering has been investigated as the baseline solution for the ITk pixel system which solves the material increase problem. Comparing the ITk to the present ATLAS Tracker, the material is significantly decreased using Serial Powering scheme.

3.1.4. Power consumption

Another key performance parameter to consider in the sensor technology is the power consumption. Although the total power consumption of the module is dominated by front-end chips, sensor technology typically requires high operating voltages and moderate leakage currents to achieve high reconstruction efficiency after irradiation [45]. The increase of the bias also increase the current and this is critical for the performance of the analogue front-end that can compensate up to 10 nA/pixel [45].

3.2. The hybrid pixel detector

The baseline technology is chosen hybrid pixel detector concept for all the 5 layers of the ATLAS ITk Pixel detector upgrade due to the fact that the technology is mature, as it is already used in the current ATLAS Pixel detector (though with another planar sensor technology on the one hand, and another technology for the electronics on the other hand). Within the hybrid concept, 2 types of sensor (3D and Planar) are proposed for the upgrade. In this section, the hybrid pixel concept will be discussed in details, and these 2 types of sensor are also introduced. Hybrid pixel detector includes a sensor part which is a passive high resistivity silicon sensor and a readout chip fabricated in CMOS technology. The silicon sensor and read-out chip are joined together using a high density connection technique called "flip-chip bump-bonding" [45]. Figure 3.3a shows the layout of an individual pixel cell with a sensor and the corresponding readout electronics. The sensor and electronics matrix are bonded to each other by means of bump contacts, as shown in Figure 3.3b [75]. However, this process is a standard commercial process but requires very specialized vendors as the bump-bonding pitch is particularly small (50 μm). Hence, the cost and pixel pitch are the challenges in hybrid pixel concept.

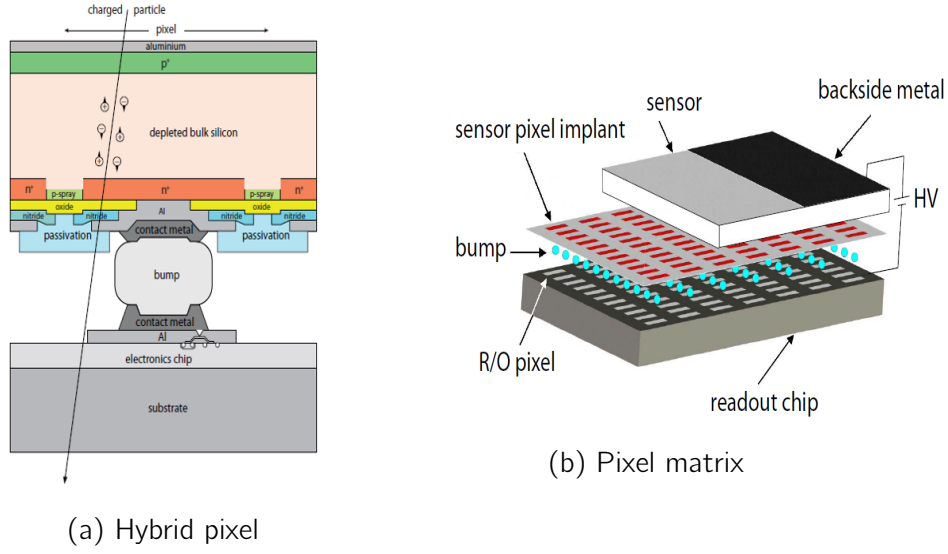


Figure 3.3. – Hybrid pixel detector: (a) Layout of an individual pixel cell having a sensor and an electronics cell ; (b) a hybrid pixel matrix; sensor and electronics chip have pixels of the same size, bonded to each other by means of bump contacts

3.2.1. Planar pixel sensors

Planar pixel sensor is the baseline for Layer 1 (L1) to Layer 4 (L4) for the Inner Track (ITk) Pixel Detector. The n⁺ implants on n-type substrate planar pixel design is used in current LHC experiment, as shown in Figure 3.4a. The fabrication of this chip requires double-sided processing. The pixel sensor consists of an n-bulk 200 μm thick, which contains n⁺ implants on the read-out side and the p-n junction on the back side. When the sensor is unirradiated, the depletion region starts at the p⁺-n junction on the backside, and the pixels are not isolated from each other until full depletion of the bulk [25]. After radiation, the bulk n-type doping changes into effectively p-type. Resulting from this so-called type inversion, the p-n junction shifts to the front side, isolating the pixels and the sensor can work correctly even if the bulk is not fully depleted. For typical substrate resistivity of 2-5 $\text{k}\Omega \cdot \text{cm}$, the type inversion happens after the fluences of $10^{12} \text{ } n_{eq}/\text{cm}^2$. With the radiation fluence increasing, in order to keep a sufficient depletion region, the HV voltage could reach 500 V at fluences around $10^{15} \text{ } n_{eq}/\text{cm}^2$. With the increased luminosity of HL-LHC, the lifetime of n⁺ in n design would get shorter.

In order to achieve sufficiently large depletion region after fluences of up to and above $10^{16} \text{ } n_{eq}/\text{cm}^2$, n⁺ in p sensor with thin wafer was designed, as shown in Figure 3.4b [76]. This has been achieved by using n⁺ pixel implants in p-substrate material and thin (100-150 μm) sensors operated at bias voltages of 500-700V [77]. The n⁺-in-p technology is a single sided process with the guard

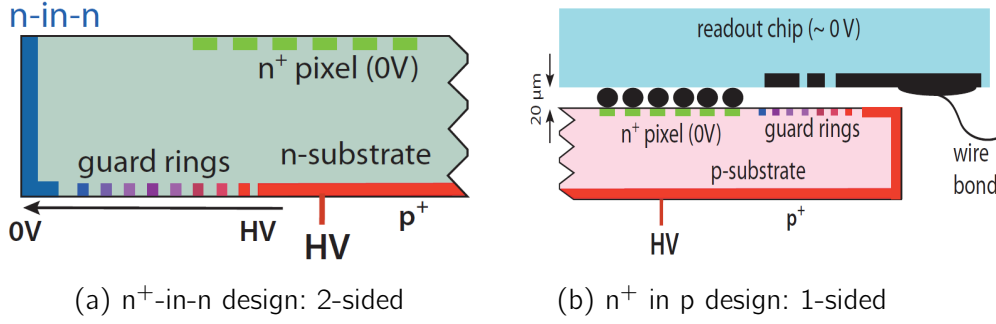


Figure 3.4. – Planar sensors: (a) LHC traditional n⁺-in-n design requiring 2-sided wafer processing ; (b) n⁺-in-p design with single-sided processing for HL-LHC upgrade

rings implanted on same side of the electrode, simplifying the fabrication process flow with respect to the n⁺-in-n technology. The guard ring design plays an important role in optimizing the breakdown voltage of sensors after irradiation. The number and distance of rings as well as metal over for vertical field suppression are the parameters to optimize.

3.2.2. 3D sensors

3D sensors are becoming the standard technology for the extremely harsh radiation environment. This technology with pixel cells $50 \times 250 \mu\text{m}^2$ has already been used in the Insertable B-Layer (IBL) [24] in ATLAS experiment. For the HL-LHC, pixel detectors with $50 \times 50 \mu\text{m}^2$ or $25 \times 100 \mu\text{m}^2$ pixel size are planned, primarily motivated by particle occupancy. Consequently, a new generation of small-pitch 3D detectors is being developed (see in Figure 3.5 [76]). 3D sensors have been chosen as baseline technology for the innermost layer (L0), due to their radiation hardness and low power dissipation [45], whereas for the other layers planar sensors are the baseline option, given their high fabrication yield and lower costs.

A similar cloud of electrons and holes generated along the track of a traversing ionizing particle is shown in Figure 3.6. Compared to the planar sensor, the charge can be collected in the 3D sensors case by the n⁺ electrode columns and p⁺ electrode columns over a much shorter distance. This results in faster signals and a much lower depletion voltage. The shorter drift distance for the charge carriers is also very beneficial in terms of radiation hardness performance.

A schematic of 3D sensor optimized for the ITk pixel detector in the HL-LHC environment is shown in Figure 3.7a [76], where a high resistance p-type wafer is supported by a low ohmic p⁺ handle wafer which can be thinned on the backside after fabrication [78]. The p⁺ columns are deeply etched through to the handle wafer where they are biased to have electric potential, the n⁺ co-

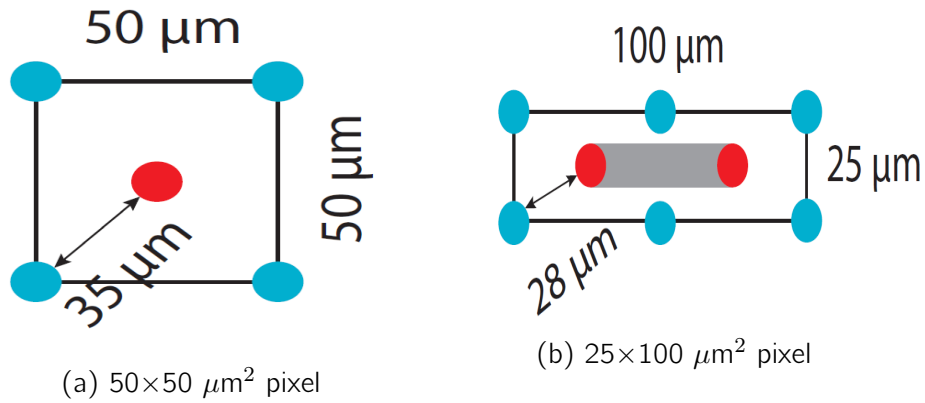


Figure 3.5. – Two top view sketches for $50 \times 50 \mu\text{m}^2$ and $25 \times 100 \mu\text{m}^2$ pixel sizes (Red: n+ column. Blue: p+ column)

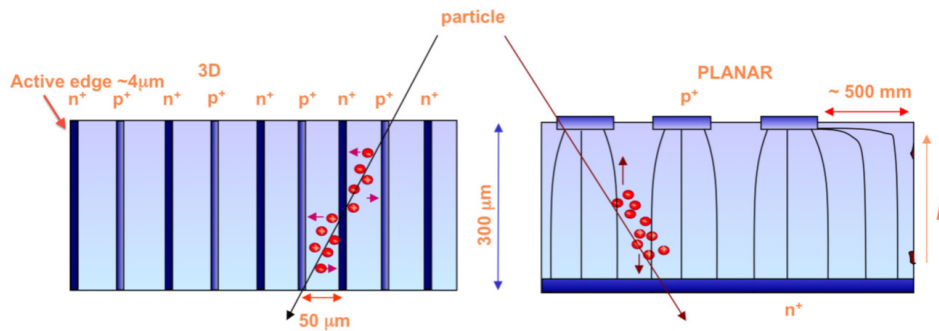
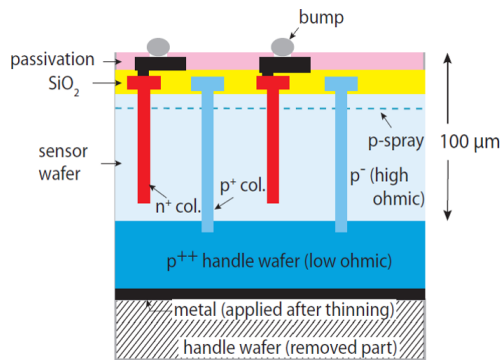
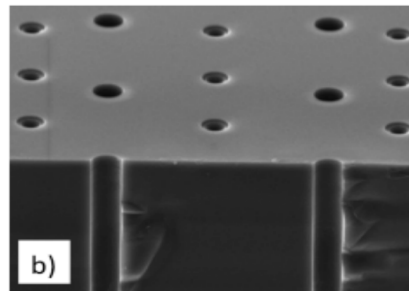


Figure 3.6. – Schematic view of charge collection in 3D and planar pixel sensors



(a) Hybrid pixel



(b) Pixel matrix

Figure 3.7. – Hybrid pixel detector: (a) A schematic layout of 3D sensor optimized for HL-LHC in the ITk Pixel Detector (b) SEM micrograph of two sets of columns etched

lumns also deeply etched but stop about $15 \mu\text{m}$ above the handle wafer, SEM

micrograph of two types of column is shown in Figure 3.7b [79]. At the top surface isolation of the n-columns is achieved by a p-spray layer avoiding the electron accumulation layer below the oxide layer from creating shorts.

3.3. The monolithic CMOS Pixel Detector

As we discussed above, hybrid pixel detectors show some advantages with respect to other technologies, in particular in terms of fast readout and radiation tolerance. However, the hybrid pixel concept has also some disadvantages due to complexity of the bump bonding process, with consequences in terms of production time, procurement and yield. Thus, an alternative option is investigated for the pixel detector: a fully monolithic depleted CMOS Pixel Detector concept. In this case, the sensor and the full readout logic circuitry are integrated into a single chip. Since recent years, it has been realized that this concept can be implemented in a commercial High Voltage (HV) CMOS technology, which enables low cost, easy procurement and low material budget et al.

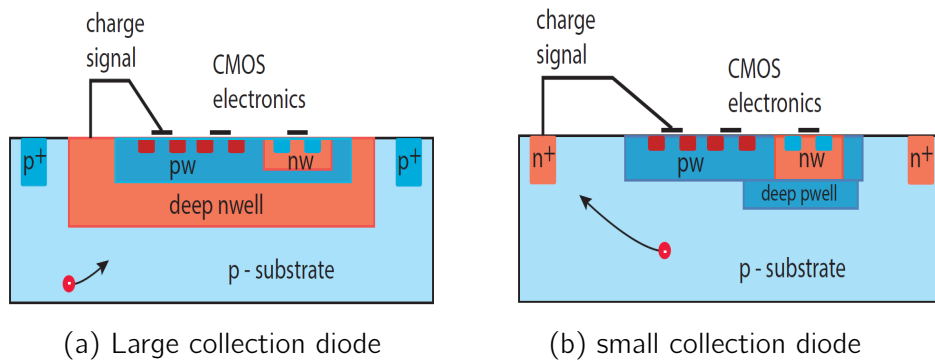


Figure 3.8. – Two approaches: (a) Large collection diode: the charge collecting deep nwell encloses the complete CMOS electronics. (b) Small collection diode: the charge collection node is placed outside the CMOS electronics area

Two approaches in this design are pursued within the ATLAS depleted CMOS sensor community. The first one is based on large collection electrode as shown in Figure 3.8a and the second one on small collection electrode concept, as shown in Figure 3.8b. In the small collection electrode concept, the charge-collecting node is placed outside the CMOS circuitry, which has for consequence that the input capacitance to the electronics is small. According to the formula (3.1) and (3.2), small amplifier input capacitance C_d directly leads to small thermal noise (electronic noise generated by the thermal agitation of the charge carriers inside an electrical conductor at equilibrium) of a pixel detector with pre-amplifier readout and shaping time as well as the detector response time τ_{CSA} [76],

$$Noise_{thermal}^2 \propto \frac{4}{3} \times \frac{kT}{g_m} \frac{C_d^2}{\tau} \quad (3.1)$$

$$\tau_{CSA} \propto \frac{1}{g_m} \times \frac{C_d}{C_f} \quad (3.2)$$

where C_f is the feedback capacitance, C_d is the pre-amplifier input capacitance, g_m is the transconductance, τ is the shaping time, and kT is the Boltzmann constant times temperature.

However, as charges need to travel longer distances to the collection node, the radiation-hardness of such a concept needs to be carefully assessed. In opposite, the large collection electrode design provides a Deep-Nwell (DNW), which embeds the electronics, and acts as a charge-collecting node. This results in a more uniform electric field in the bulk and shorter drift distance and leads to better radiation hardness. The price to pay is a larger input capacitance to the electronics and the need for careful study of sensor to electronics coupling.

3.3.1. Large collection diode CMOS sensors

On top of using the advantage of small feature size CMOS technology, high resistivity wafers are used in the fabrication process and a high biasing voltage up to 100-300 V can be applied to the substrate through top or edge to generate a sufficient depletion region. This is very beneficial in terms of the radiation hardness. The large collection diode CMOS sensors were mainly pursued in two technologies: LFoundry 150 nm technology and AMS technology. Two different digital read-out architectures are being implemented in LFoundry 150 nm technology and AMS technology. The column-drain architecture, which is similar to the present ATLAS FE-I3 front-end chip is used in LFoundry technology to evaluate their performance [80]. A Parallel Pixel To Buffer (PPTB) readout is implemented in AMS aH18 (180 nm) and aH35 (350 nm) [81].

LFoundry technology

LFoundry is a technology with a minimum gate length of 150 nm. This technology offers a Deep Nwell (DNW) on a P substrate. The NMOS transistors are implemented inside P wells which can be isolated from P substrate via the use of an Nwell ring and a NISO plus Deep Nwell area. The PMOS transistors are implemented inside N wells which can be isolated from Deep Nwell via the use of a Pwell ring and a PSUB area. These devices are fabricated using a dedicated high resistance p-type substrate. Wafer thinning and p-type back implants are available after production [82]. The overview of technology options in LFoundry process is shown in Table 3.2.

In the past five years, three prototypes have been designed and fabricated in the LFoundry technology: CCPD_LF, LF_CPIX and LF-MONOPIX. The sensor part

Feature	Comments
MOS channel length	150 nm
Metals	4-6 aluminium layers
Supply rail	1.8 V
MOS transistor types	low power/regular
Wafer type	CZ, p-type bulk, over $2 \text{ k}\Omega \cdot \text{cm}$
Deep Implants	NISO, DNWELL, PSUB
Backside processing	Thinning $300\mu\text{m}$, p-type implant, annealing, metallization

Table 3.2. – Overview of technology options in LFoundry process

and first stage of front-end was studied from prototype CCPD_LF and LF_CPIX, the first fully monolithic prototype was achieved with the LF-MONOPIX demonstrator.

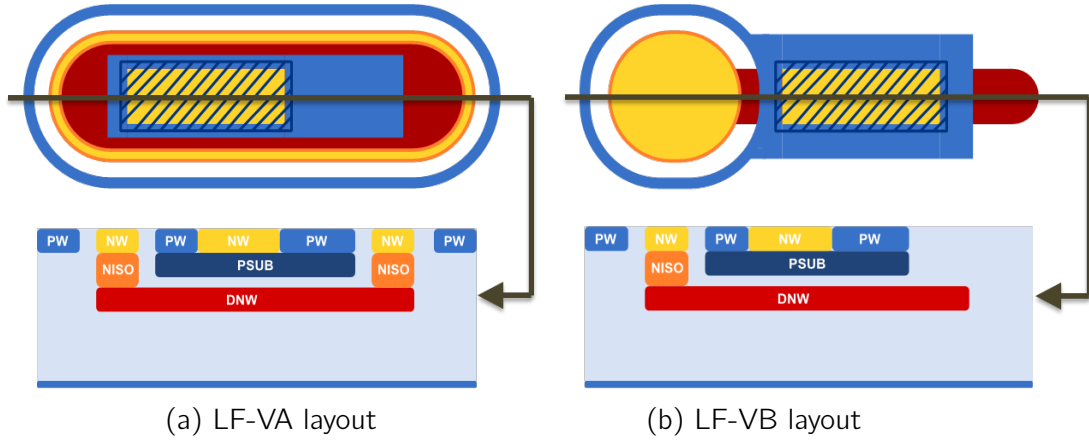


Figure 3.9. – Two kinds of design in CCPD_LF

The CCPD_LF chip size is 5 mm by 5 mm with the pixel size $33 \times 125 \mu\text{m}^2$. The pixel matrix consists of 24 rows and 144 columns resulting in 3456 pixels. A "BiasBlock" cell with eleven 6-bit DACs to generate all the polarizations of the pixel and one additional test DAC are located at the bottom of the chip. A "DigitalMatrix" cell to activate and select pixels is also in the chip periphery. An end of row cell designed for buffered signals transmission and row selection is located at the side of the chip. Two kinds of prototypes are designed with different charge collection diodes in CCPD_LF, which are named LF-VA and LF-VB. Their layout is shown in Figures 3.9a and 3.9b respectively. The electronic logic is isolated from the HV ring by Deep NWell in the VA layout. The internal Pwell and Nwell are also isolated from the substrate by using a specific isolation layer. Therefore, a negative HV can be applied by the HV ring surrounding the DNW [83]. LF-VB electronic logic is not isolated from the DNW layer, and diodes

can be biased through the DNW electrode.

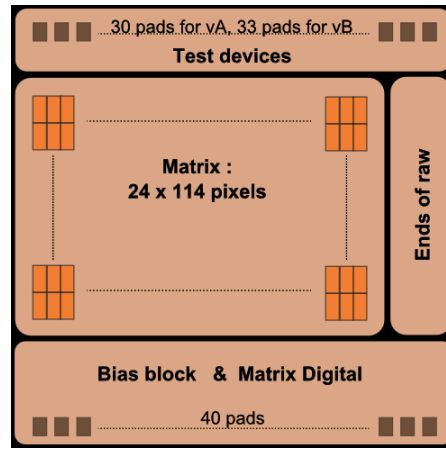


Figure 3.10. – CCPD_LF floorplan

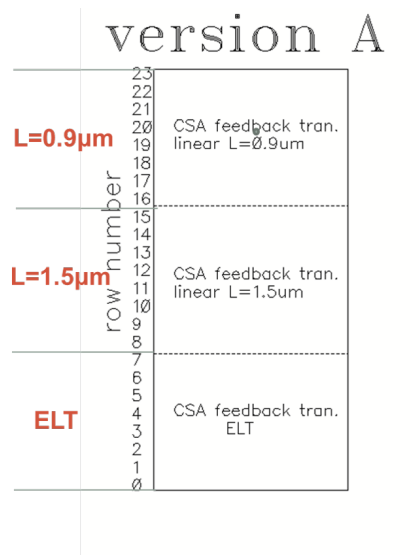
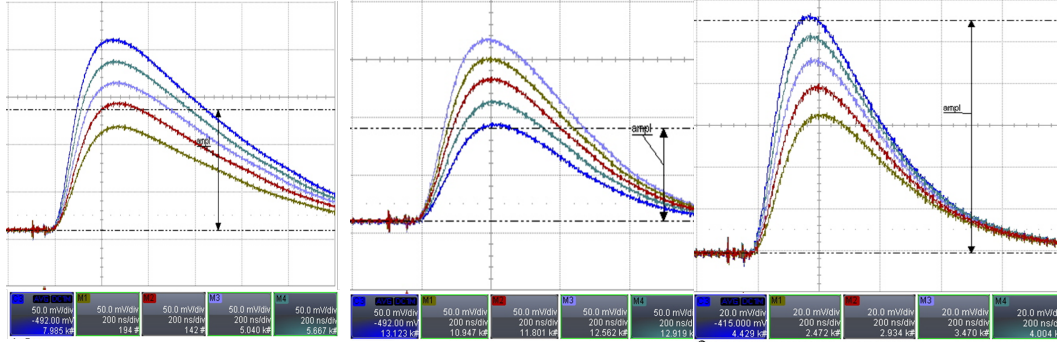


Figure 3.11. – Placement of pixel flavors in the matrix LF-VA

Since the LF-VB had very low breakdown voltage (< 20 V) and much higher leakage current than LF-VA, as a consequence only the CCPD LF-VA was carefully characterised. 3 flavors of pixels have been implemented differing by the pre-amplifier feedback transistor type: linear NMOS transistor with Length = $0.9 \mu\text{m}$, linear NMOS transistor with Length = $1.5 \mu\text{m}$ and Enclosed layout transistors (ELT). Figure 3.11 shows the placement of pixel flavors in the matrix LF-VA. The test injection signal was applied to the input of pre-amplifier by using a test capacitor which can convert the voltage signal to current pulse. The pre-amplifier outputs when varying the injection of 3 flavors are shown in Figure 3.12. Since



(a) Linear NMOS transistor: $L = 0.9\mu\text{m}$ (b) Linear NMOS transistor: $L = 1.5\mu\text{m}$ (c) Enclosed layout NMOS transistor

Figure 3.12. – The pre-amplifier outputs for the 3 flavors of pixels with different injection pulses

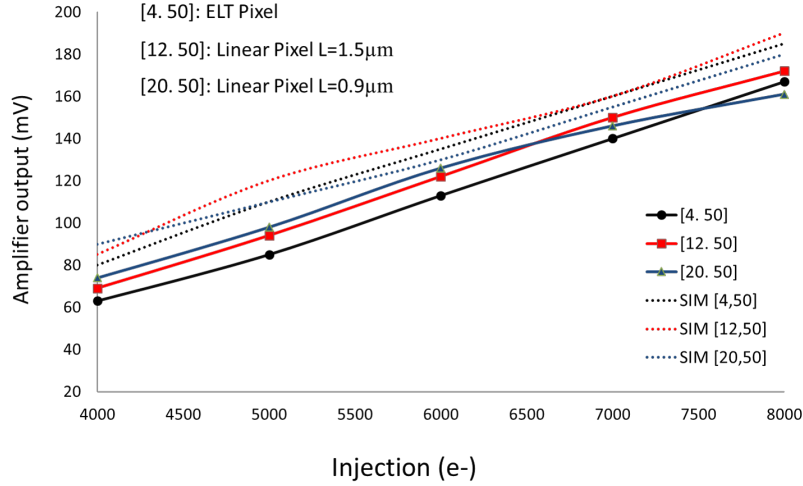


Figure 3.13. – The comparison of pre-amplifier output between simulated (dash line) and measured (solid line).

linearity is an important parameter for each analog electronics implementation, the characteristics of each pixel was tested. The comparison of pre-amplifier output between simulated (dash line) and measured (solid line) is shown in Figure 3.13, and it can be noted that the simulated and measured characteristics are nearly identical in all 3 pixel flavor cases.

In order to evaluate the performance in terms of TID tolerance in LFoundry technology, the prototypes were exposed to ionizing radiation using X-ray irradiations up to doses over 100 MRad. Gain and noise of the front-ends were measured during irradiation in order to characterize the performance during the lifetime of a CMOS detector. All measurements show very good TID tolerance,

a degradation of less than 30% in gain up to 100 MRad, and about 10-20% increase in noise [45]. In order to investigate the evolution of the depletion region with fluence, edge-TCT measurements were performed on dedicated test structures placed on the prototypes. Figure 3.14 shows that large depletion depths of more than 50 μm can be reached till up to the neutron fluences of $1 \times 10^{15} n_{eq}/\text{cm}^2$ [84].

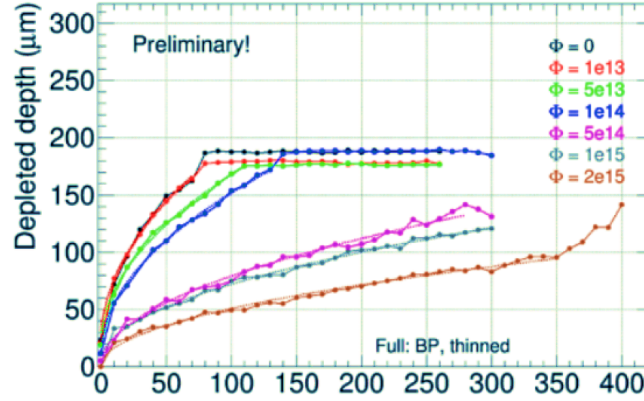


Figure 3.14. – Edge TCT measurements of depletion depth as a function of bias voltage for different radiation neutron fluences

The LF_CPIX and LF-MONOPPIX prototypes are the successor to CCPD_LF using the same technology, but a more complete description of these prototypes will be found in Chapter 4 and Chapter 5 respectively.

AMS technology

CCPDv1 which is the first sensor chip realised in AMS aH18 process, has been submitted in November 2011 [85]. Seven CCPD versions have been developed afterwards. Table 3.3 summarizes a few properties of each version. The CCPD chips are implemented in the standard AMS aH18 HVCMOS process on the standard substrate of 10 - 20 $\Omega \cdot \text{cm}$ resistivity. It is a triple well process that includes p-well, n-well, and a deep n-well [86]. The pixel contains a charge sensitive amplifier, a comparator with threshold tuning circuits and an output stage. The signals of three pixels are multiplexed to one signal pad and the signal can be transmitted capacitively to a readout FEI4 chip.

CCPD prototypes have been extensively tested. The samples irradiated to $1.3 \times 10^{14} n_{eq} \cdot \text{cm}^{-2}$, $5 \times 10^{14} n_{eq} \cdot \text{cm}^{-2}$ and $5 \times 10^{15} n_{eq} \cdot \text{cm}^{-2}$ have shown detection efficiencies of 98.1%, 99.7% and 97.6%, respectively. The bias voltage of the sensor used in these measurements was up to 85 V. Average hit efficiency as a function of threshold voltage is shown in Figure 3.15 [87].

In parallel to the AMS aH18 developments, the community has used the AMS H35 technology as well. H35DEMO is a full-size demonstrator that is implemented on three types of high-resistivity substrates (80 $\Omega \cdot \text{cm}$, 200 $\Omega \cdot \text{cm}$ and

CCPD version	Description
CCPDv1	Basic design - pixel size $33\mu\text{m} \times 125\mu\text{m}$, readout with FEI4 pixel readout ASIC
CCPDv2	Improved radiation tolerance, linear transistors replaced with enclosed ones
CCPDv3	Large matrix with $25\mu\text{m} \times 25\mu\text{m}$ pixels implemented, readout with CLICPIX pixel readout ASIC
CCPDv4	Pixel position encoded as pulse length
CCPDv5	Comparator with time walk compensation
CCPDv6	a new version of aH18 process that offers more flexibility such as the use of high resistivity substrates
CCPDv7	Chip version with a new guard ring geometry that allows higher bias voltage of up to 150 V

Table 3.3. – CCPD prototypes in AMS aH18 process

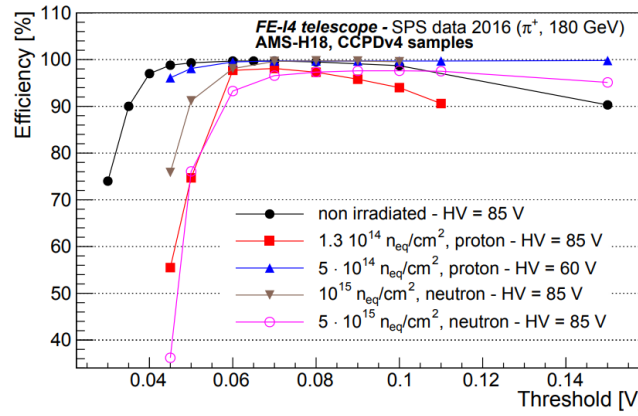


Figure 3.15. – CCPD average hit efficiency as a function of threshold voltage

$1000 \Omega \cdot \text{cm}$) in this larger feature size process. The sensor design is based on developments made for MuPix [88] [89] and CCPD detectors. H35DEMO design consists four independent sub-matrices: NMOS monolithic matrices, CMOS monolithic matrices and two analog matrices. The NMOS and CMOS monolithic matrices integrate sensor and the complete associated readout electronics into the same die, the two analog matrices are designed for capacitive-coupling to the FE-I4 readout ASIC to test the sensor diode properties.

The H35DEMO samples with different substrates were characterised before irradiation, and the $80 \Omega \cdot \text{cm}$ and $200 \Omega \cdot \text{cm}$ show low leakage current well below $1 \mu\text{A cm}^{-2}$ up to the breakdown voltage, determined to be 178 V and 180 V, respectively (see Figure 3.16 [90]). For the $1000 \Omega \cdot \text{cm}$ sample, an early offset of current is observed at a bias voltage of 30 V due to Rise-And-Flatten

(RAF) effect [91]. However, further measurements have shown that a plateau of current is reached in the device before a second upset in current at 180 V is observed, as shown in Figure 3.17 [90].

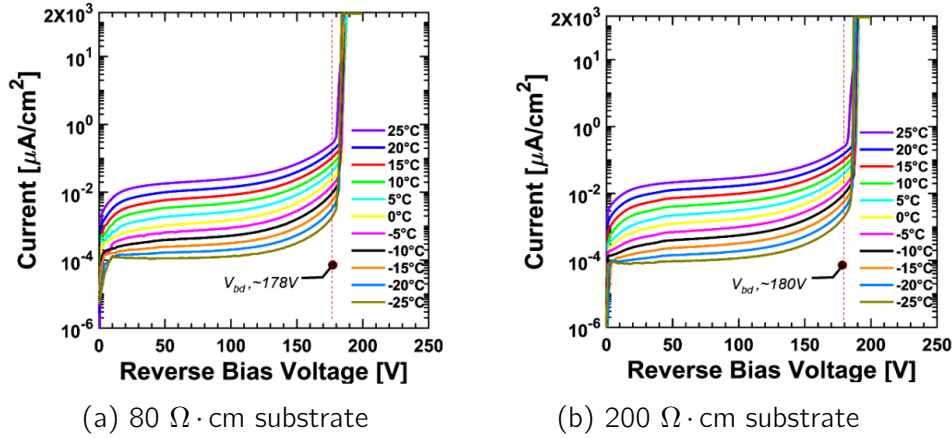


Figure 3.16. – Characteristic I-V curves for 80 $\Omega \cdot \text{cm}$ and 200 $\Omega \cdot \text{cm}$ substrate resistivity samples at different temperatures

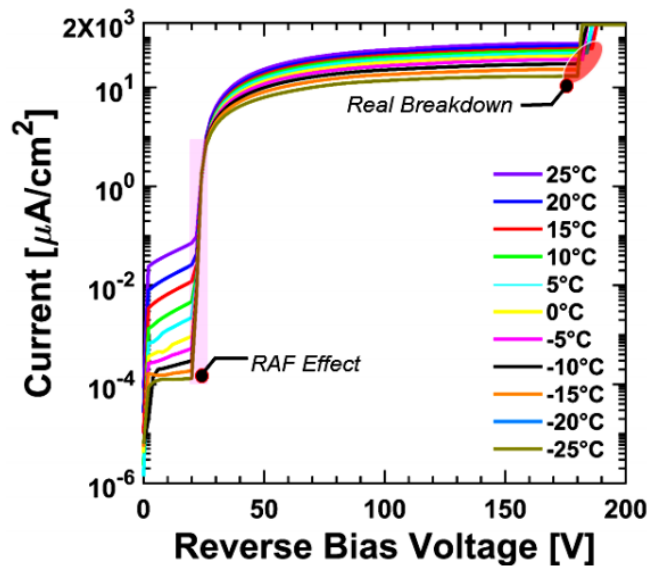


Figure 3.17. – Characteristic I-V curves for 1000 $\Omega \cdot \text{cm}$ substrate resistivity sample at different temperatures

Figure 3.18 [90] shows the average hit efficiency as a function of bias voltage for different substrate resistivities and FEI4 detection threshold. A clear dependence of the efficiency on the substrate resistivity for comparable thresholds can be observed. The higher the resistivity, the smaller the bias voltage needed to obtain a high detection efficiency. High enough detection efficiency over 99% can be achieved for all H35DEMO substrate resistivities.

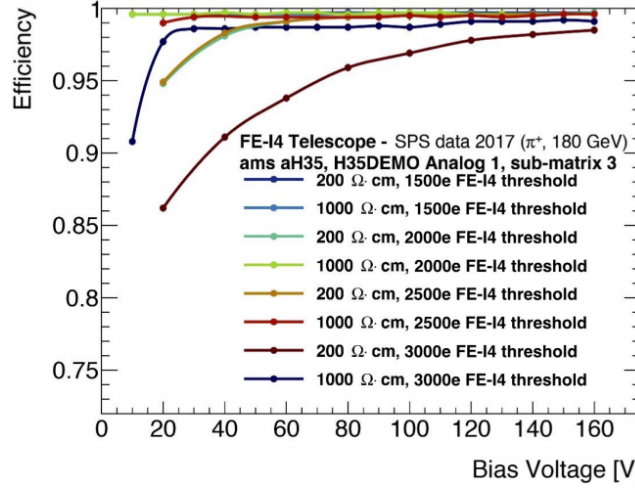


Figure 3.18. – H35DEMO sensor average hit efficiency as a function of bias voltage for different substrate resistivities and FE-I4 detection threshold

3.3.2. Small collection diode CMOS sensors

As shown in Figure 3.8b, small collection diode design approach leads to a small input capacitance, which in turn translates into low noise and fast timing. The development of small collection diode CMOS sensor was pursued in Tower-Jazz (TJ) 180 nm technology. The prototypes developed in our collaboration inherit from the design of the ALICE ITS pixel chip (ALPIDE) [92] [93]. The ALICE ITS cell cross section with n-well charge collection node is shown in Figure 3.19a, in which it can be seen that the small collection diode is located outside of the deep p-well which hosts the CMOS electronics. The depletion region is limited for a given bias voltage due to the small size of the collection electrode. As a consequence, significant charge loss can be expected at the pixel edge un-depleted regions after irradiation. In order to improve the radiation hardness performance of the prototype, the fabrication process was modified, as shown in Figure 3.19b [94] [95]. In the modified process, the epitaxial p-layer is replaced by a planar deep n^+ -p junction. The cell size and the collection node geometry are also optimized.

The modified process was implemented in two monolithic designs with different read-out design, MALTA and TJ-MONOPIX, as shown in Figure 3.20 [96]. A new asynchronous read-out architecture is used in MALTA, which avoids excessive clock activity and hence further reduces transient coupling into the active matrix region. It should also be noted that this kind of design is very efficient in terms of reduced power consumption. TJ-MONOPIX uses a similar read-out logic to the present ATLAS Pixel Detector (FE-I3 readout circuit) which is based on a column drain architecture.

MALTA and TJ-MONOPIX share the same analog front-end design with low

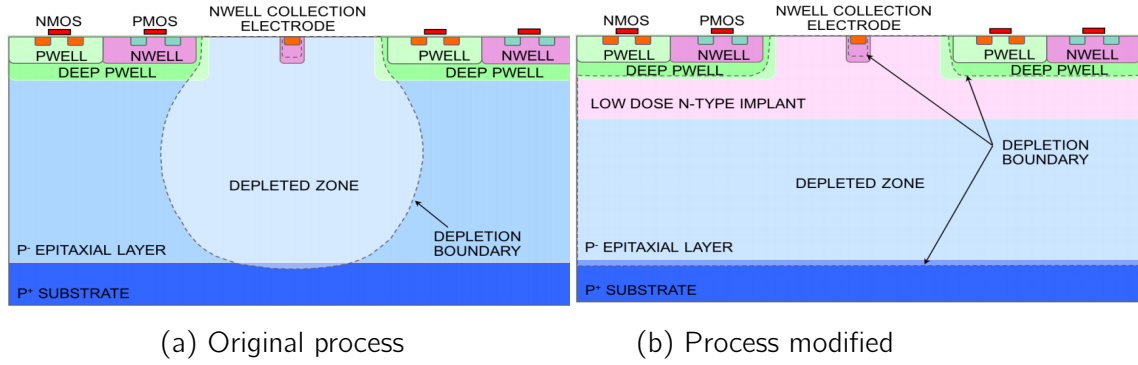


Figure 3.19. – Small collection diode in TowerJazz 180 nm technology (a) ALICE ITS cell cross section with n-well charge collection node; (b) new TowerJazz 180 nm cell with process modification to provide better depletion and improve charge collection from all regions.

noise and low power consumption. The analog front-end includes a charge-sensitive amplifier followed by a discriminator and a hit buffer. The n-well charge collection electrode maintains a geometry with a small capacitance between 3 fF and 10 fF. The matrix analog power consumption of the two designs is less than $60 \text{ mW} \cdot \text{cm}^{-2}$ ($\sim 0.9 \mu\text{W}/\text{pixel}$) [97]. The noise is about 8 e- at 500 nA leakage current, the timewalk (the different pulse height assigned to two different clock cycles effect) is less than 20 ns, and the threshold dispersion is ≤ 40 e-. These performances are quite interesting as a base for a depleted CMOS detector. The amplitude measurement is provided by a 6-bit ToT in TJ-MONOPIX or "Chain Intersection Time to Hit Signal Guide" code in MALTA [96].

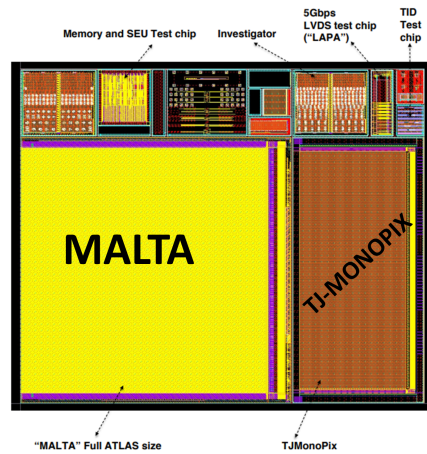


Figure 3.20. – Small collection diode prototypes in TowerJazz technology: MALTA chip with asynchronous read-out, TJ-MONOPIX chip with column-drain read-out

Both prototypes were fully operational before and after $1 \times 10^{15} \text{ n}_{eq} \cdot \text{cm}^{-2}$

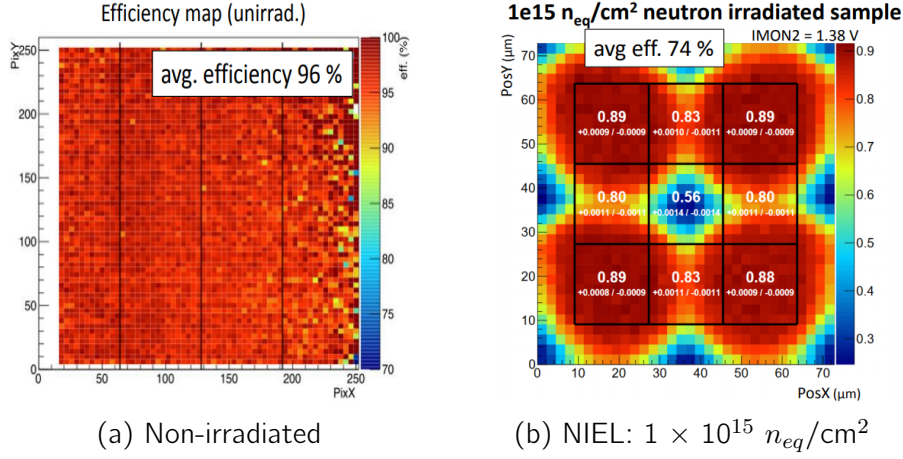
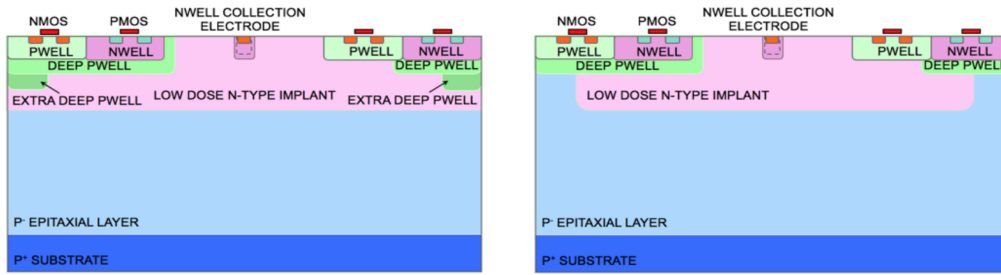


Figure 3.21. – Mean detection efficiencies before and after neutron irradiation in TJ-MALTA

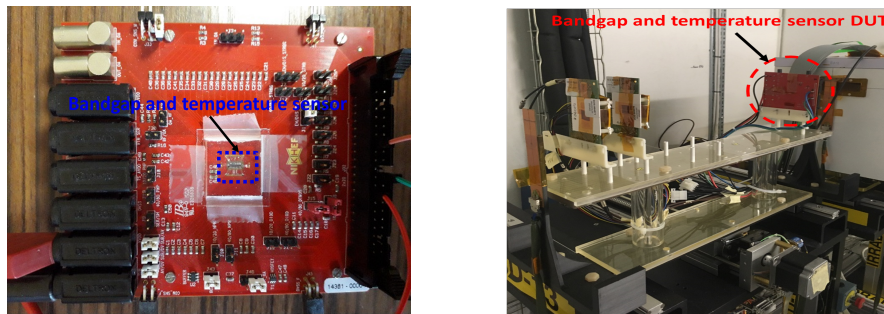
NIEL damage, but the degradation in noise and detection efficiency after irradiation can be seen and need further optimization. For TJ-MALTA, the mean detection efficiency was tested under the CERN SPS, with 120 GeV pions. Efficiencies before and after NIEL irradiation up to $1 \times 10^{15} \text{ n}_{eq} \cdot \text{cm}^{-2}$ are shown in Figure 3.21 [97]. For the non-irradiated chip, the mean detection efficiency was 96% . After irradiation, the mean efficiency dropped to 74%, due to an increased noise level, forcing an even higher threshold of 350 e-, and severe charge loss at the pixel edges [97]. Figure 3.21a and 3.21b illustrate the correlation of the efficiency with the DNW layout. Similar results were also observed with the TJ-Monopix [98]. Detailed 3D simulations established that the charge loss near the pixel edges is related to an area of a very low electric field, increasing the probability to capture the signal charge by radiation-induced traps [99]. In order to improve the charge collection ability at the edge of the pixel, two pixel improvements were proposed as illustrated in Figure 3.22 [97], significantly enhancing the lateral electric field near the pixel edges in simulation: a gap in the low dose n- layer and an additional deep p-type implant [97]. Prototype with modified process was submitted in August 2018 and received at the begin of the 2019. The characterization is still ongoing.

Finally, the bandgap and temperature sensor blocks located in the chip periphery were also irradiated in May 2018 at the 24 GeV IRRAD proton facility in CERN. Bandgap and temperature sensor blocks were wired bonded on the same test boards, as shown in Figure 3.23a. The test board mounted on the beam table is shown in Figure 3.23b. The total dose reached 72 MRad after one week irradiation, the outputs of bandgap and temperature sensor were monitored in the control room throughout the time of irradiation. Band gap output voltage increased from 0.989 V (0 MRad) to 1.066 V (72 MRad), an increase corresponding to about 1 mV/MRad, only 7.7% variation after 72 MRad irradiation (see



- (a) An extra deep p-well is added at the edge of the pixel
- (b) The n- implant is removed at the edge of the pixel

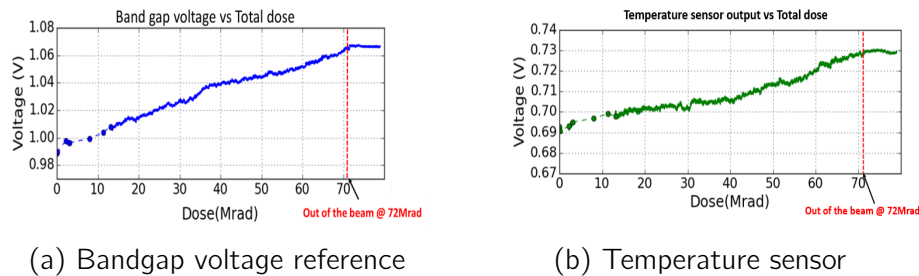
Figure 3.22. – Cross-section of the technology improvements



- (a) Bandgap and temperature sensor chip on Board
- (b) Board installed on the proton beam table

Figure 3.23. – The radiation set-up for bandgap and temperature sensor chip.

in Figure 3.24a. The temperature sensor output voltage as a function of dose is shown in Figure 3.24b, the value increased from 0.693 V (0 MRad) to 0.729 V (72 MRad), an increase corresponding to about 0.5 mV/MRad. It can also be seen that the output of both blocks became stable after moving the device under test out of the beam. Both bandgap voltage reference and temperature sensor can work properly and generate stable output voltage under proton irradiation up to 72 MRad.



(a) Bandgap voltage reference

(b) Temperature sensor

Figure 3.24. – Bandgap voltage reference and temperature sensor outputs as a function of dose

4. LF_CPIX demonstrator development and characterization

In order to investigate the sensor part and analog front-end block for the ATLAS ITk upgrade, a first prototype CCPD_LF which is using the large collection diode concept, was designed and showed promising results [100] [101]. Based on this design, a larger size demonstrator sensor chip (LF_CPIX) was developed in 2016 with various improved pixel types designed to have high in-time efficiency for minimum ionizing particle tracks and good uniformity, before and after irradiation. The readout of LF_CPIX is possible by both capacitive coupling to FE-I4, as it was the case for CCPD_LF, and with a standalone readout. This demonstrator has been fabricated on high resistivity wafers (approximately $2 \text{ k}\Omega \cdot \text{cm}$ resistivity) in LFoundry 150 nm technology. Figure 4.1 shows the layout view of CCPD_LF and LF_CPIX. In order to increase the reverse breakdown voltage of the chip as well as to reduce the inactive region, the guard-ring strategy of LF_CPIX was optimized, following detailed TCAD simulation [102]. The LF_CPIX chip implemented these new ideas, as well as new design of the analog front-ends. The chip and pixel sizes are $10 \times 10 \text{ mm}^2$ and $250 \times 50 \text{ }\mu\text{m}^2$, respectively.

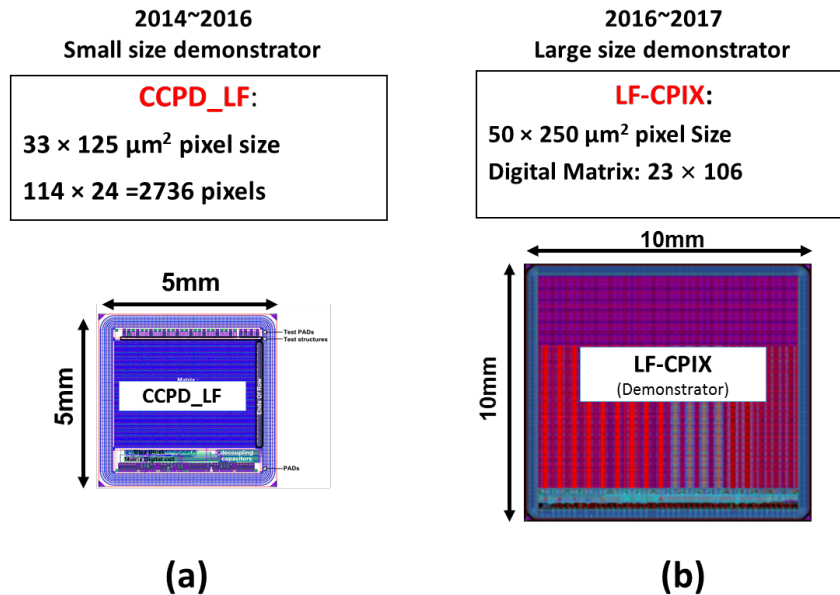


Figure 4.1. – Layout of chips (a) CCPD_LF (b) LF_CPIX

4.1. LF_CPIX prototype introduction

4.1.1. Chip and pixel rings

Based on the chip CCPD_LF, the LF_CPIX demonstrator was designed in two different versions: LF_CPIX v1 and LF_CPIX v2. The main difference between these two versions is in the chip guard ring design while they have the same electronics inside the pixels.

The V1 of LF_CPIX chip has exactly the same chip and pixel guard-ring as CCPD_LF, as shown in Figure 4.2(a). Following TCAD simulation studies, some improvements have been done for the V2, by increasing the distance between the Nwell ring and its neighbouring Pwell rings in order to improve the breakdown voltage, and by reducing the number from 10 to 7 of the Pwell chip ring in order to shrink the dead area. Rings allocation for LF_CPIX V2 is shown in Figure 4.2(b). Figure 4.3 shows the chip and pixel guard-ring comparison between these two versions.

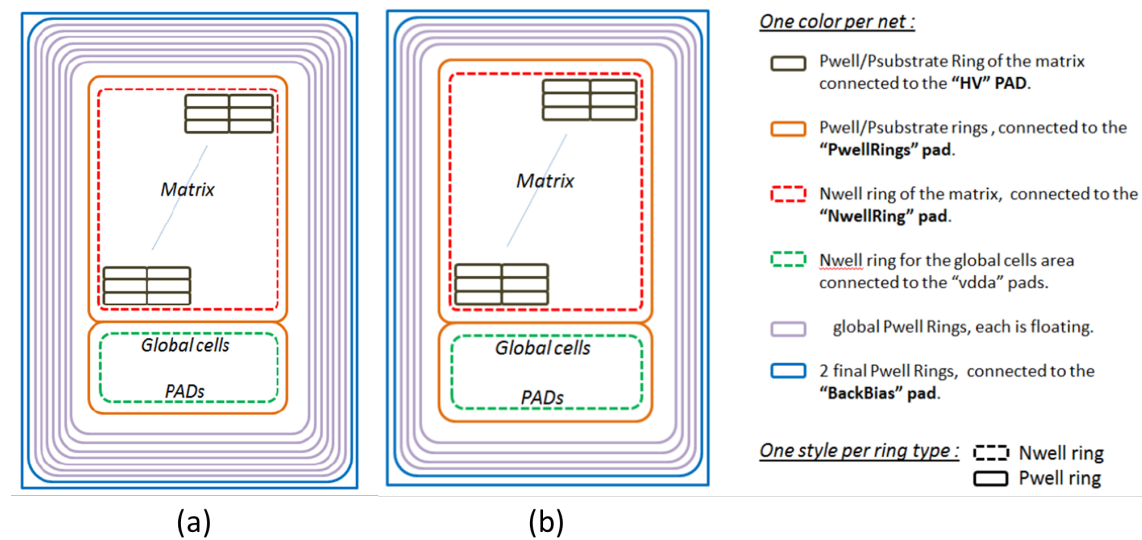


Figure 4.2. – Ring allocation for 2 versions (a) LF_CPIX V1 (a) LF_CPIX V2

4.1.2. The pixel design

Since the sensor part is biased by a high voltage, the logic and the sensor part must be isolated. If it is not the case, the high-voltage potential on the sensor part could damage the transistors in the logic part. The diagram of LF_CPIX pixel cross section is shown in Figure 4.4. The sensing diode is formed by the deep N-well and the p-type substrate diode, and the deep N-well acts as the

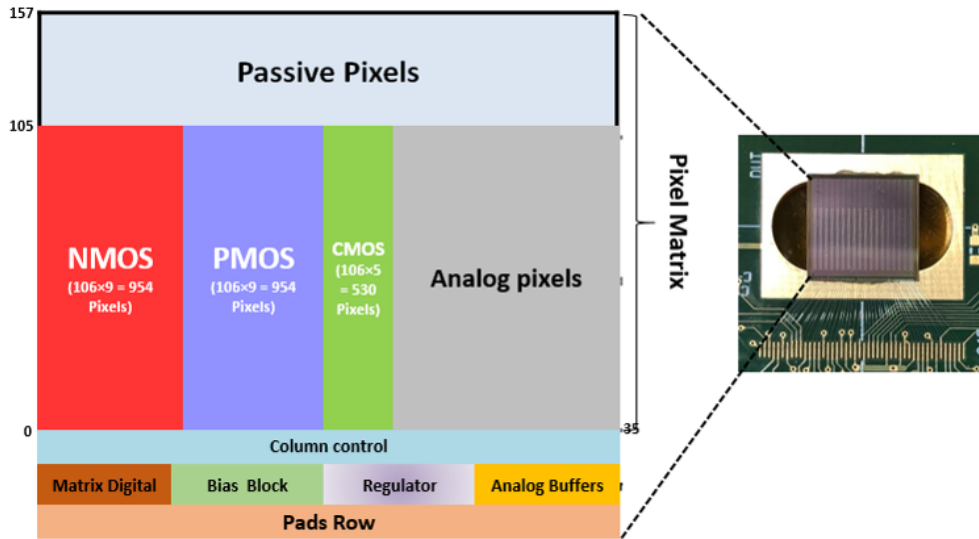


Figure 4.5. – The floorplan of LF_CPIX

tection against noise injection via the supply line. The supply of the PMOS pixel type and CMOS pixel type is "VddaPRE" (1.5 V) which is generated by an on-chip regulator, while "gndaPRE" (0.3 V) is used for NMOS type pre-amplifier.

The PMOS pre-amplifier is the baseline in LF_CPIX. The core schematic view is shown in Figure 4.6 with a similar design as CCPD_LF. A new pre-amplifier with NMOS input transistor is shown on the Figure 4.7.

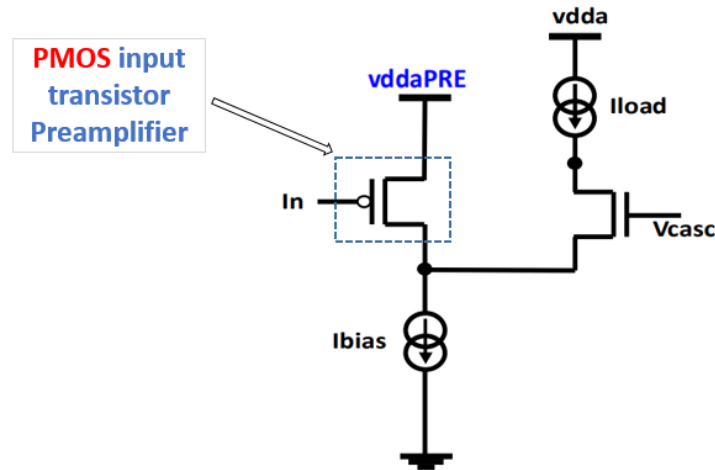


Figure 4.6. – PMOS pre-amplifier core schematic view

As we know from the formula 4.1, higher transconductance (g_m) can help in reducing the thermal noise.

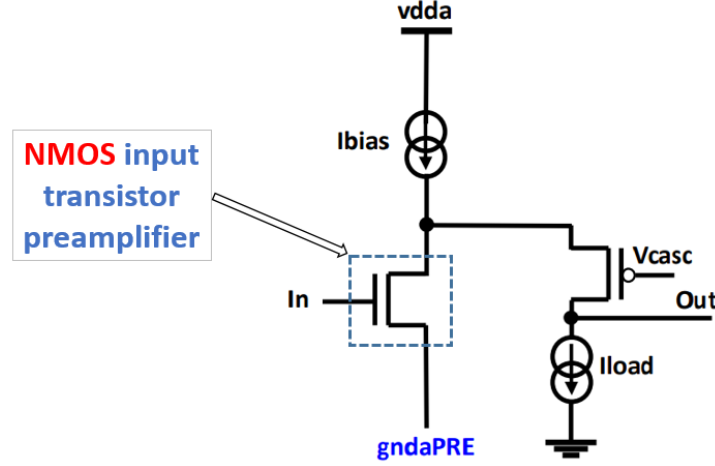


Figure 4.7. – NMOS pre-amplifier core schematic view

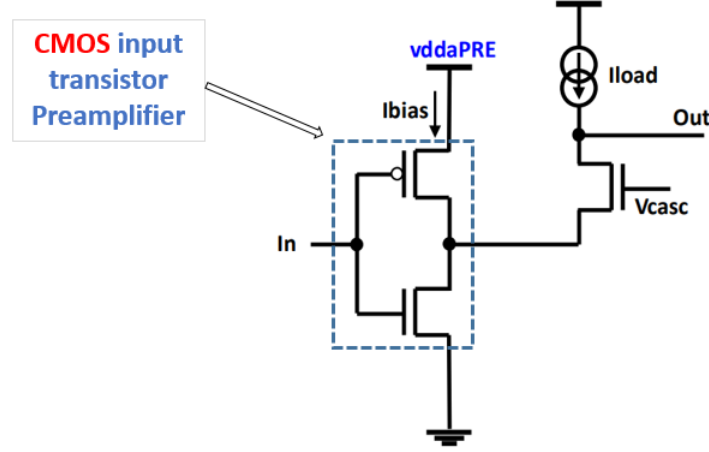


Figure 4.8. – CMOS pre-amplifier core schematic view

$$ENC_{thermal}^2 \propto \frac{4}{3} \times \frac{kT}{g_m} \frac{C_d^2}{\tau} \quad (4.1)$$

where C_d is the pre-amplifier input capacitance, τ is the shaping time, and kT is the Boltzmann constant times temperature. But in PMOS type and NMOS type pre-amplifiers, the bias transistor does not contribute to the transconductance and adds noise which is around 10-30% of the total noise in a typical configuration [103]. It is possible to replace this single PMOS or NMOS input transistor by a complementary transistor pair which contributes to the total transconductance of the input stage. In this case, the total transconductance is described as:

$$g_m(Total) = g_m(PMOS) + g_m(NMOS) \quad (4.2)$$

where $g_m(PMOS)$ and $g_m(NMOS)$ are the transconductance contribution from PMOS transistor and NMOS transistor, respectively [103]. This is the main motivation to implement a pre-amplifier with complementary NMOS and PMOS input transistors in this chip, which is shown in Figure 4.8.

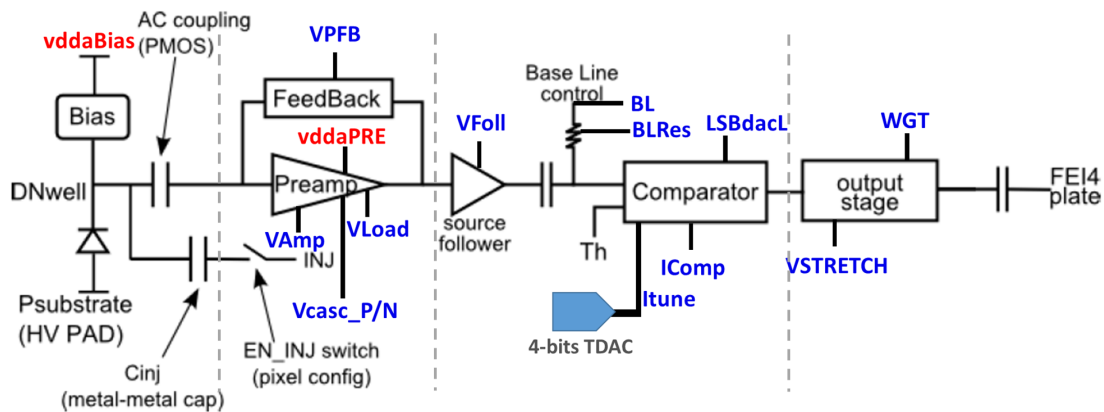


Figure 4.9. – LF CPIX Pixel architecture diagram

Figure 4.9 shows one digital pixel architecture diagram. It is composed of a pre-amplifier (CSA) which is AC coupled with the DNwell diode, a source follower and a comparator. The sensor signal is amplified by a charge-sensitive amplifier that converts the current pulse into a voltage signal through an integral feedback circuit. The output of the amplifier is sent to the comparator via the source follower and compared to an externally controlled threshold (TH). A four-bit threshold-tuned DAC (TDAC) was designed to fine-tune the threshold of each pixel. The output of the discriminator is connected to the output stage.

All the analog cells are powered by Vdda (1.8 V) and Gnda, except cells for which a special supply is mentioned in red in Figure 4.9. The Bias Block provides all the bias for the pixel circuit. It contains thirteen 6-bit DACs which are summarized in Table 4.1 and can be tuned to adjust the chip configuration, some of them are highlighted in Figure 4.9.

In the "pre-amplifier" cell, "Vamp" polarization which is defined from 6-bits global DAC, fixes the current of the pre-amplifier, "VLoad" (from 6-bits global DAC) is the polarization of the pre-amplifier load. "Vcasc_P/N" (from PAD) is the polarization of the pre-amplifier cascode. The cascode is a two-stage amplifier that consists of a common-emitter stage feeding into a common-base stage. In the "Feedback" cell, "VFPB" polarization, which is from 6-bits global DAC, tunes the feedback resistance value and adjusts the signal occupation time. In the "Source Follower" cell, "VFoll" (from 6-bits global DAC) fixes the current of the source follower. The "Base line Adjustment" cell is employed to adjust the base line value at the output of the amplifier in order to permit an adequate value for the comparator and to form a CR filter. "BL" polarization (from PAD) assures a well-defined base line value. "BLRes" polarization (from 8-bits DAC) tunes the R

DAC No	Bias name	Comment	Typical value
1	BLRes	R value of the filter	28
2	VAmp	Current of the pre-amplifier	26
3	VPFB	Feedback resistance value	47
4	VFoll	Current of the source follower	12
5	VLoad	Bias of the pre-amplifier load	11
6	IComp	Current of the comparator	24
7	VSTRETCH	Current polarization for the stretching of the width of the comparator output signal	5
8	IBOTA	Current for the OTA of the Regulator	20
9	IBCS	Current of the pre-amplifier (Analog matrix)	23
10	WGT	Current polarization for the amplitude of the pixel output	32
11	LSBdacL	Current value of the LSB of the local DAC (for AnaDig pixels)	32
12	LSBdacL2	Current value of the LSB of the local DAC (for Analogue pixels)	32
13	IBCS2	Current of the pre-amplifier (AnaSaturated Pixels with ITUNE)	23

Table 4.1. – List of global DACS in bias block

value of the filter by increasing the "BLRes" bias voltage, the time constant of the filter can be shortened.

The "comparator" cell consists of three main blocks: a discriminator, signal stretching circuit and output stage. In the discriminator block, a differential transistors pair is implemented to compare the pre-amplifier signal with the threshold. The signal stretching circuit block allows to amplify the output signal. The amplitude of the output signal can be tuned in the output stage block. In these three blocks, several parameters are used to adjust the configuration and performance. The "Th" voltage (from PAD) imposes a global value for the threshold. The "Itune" current from 4-bit local DAC (TDAC) allows a local adjustment of the threshold in each pixel. The "LSBdacL" polarization (from 6-bit global DAC) allows to tune the LSB value of the local DAC of the pixel. The "VSTRETCH" polarization (from 6-bit global DAC) allows to tune the width of the comparator output signal. The "WGT" polarization (from 6-bit global DAC) imposes the pixel output amplitude.

4.1.3. The "Matrix Digital" block

The "Matrix Digital" block contains all digital pixel matrix logics to configure and read the chip. A shift register transmits all the configuration bits to the 13 global DACs in the Bias Block cell, and to the matrix of pixels. The shift order of the entire circuit is shown in Figure 4.10. All pixels are standalone readable.

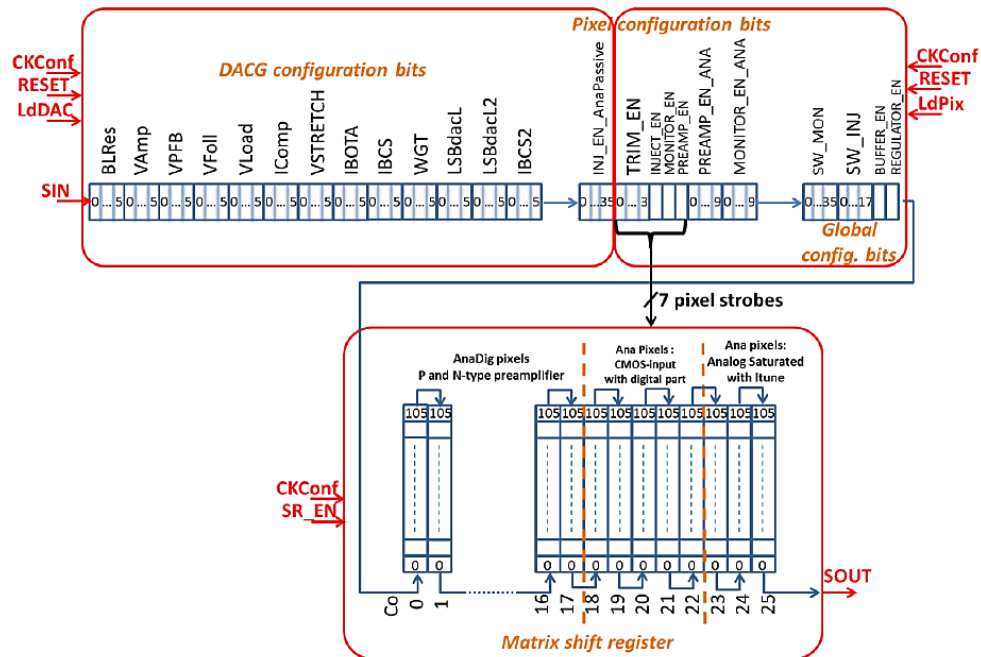


Figure 4.10. – Global Shift Register order

All the digital parts of the LF_CPIX demonstrator are controlled by 5 signals, which are described in Table 4.2.

Signal name	Description
CKConf	Shift register clock
LdDAC	Load the global DACs latches from the Shift Register
SR_EN	1 : the pixel's DFF receives the HIT (comparator output) 0 : the pixel's DFF is chained in a shift mode
RESET	Reset of the Global Shift register
LdPix	Load the pixel configuration from the Shift Register

Table 4.2. – Control signals in shift register

The data is given by series on the "SIN" pad. The data follows the entire shift register, which contains global shift register and pixels shift at the frequency of the "CKConf" clock and can be read on the "SOUT" output PAD at the end.

The data frame (Global DACs and Matrix shift register) contains 2953 bits. The shift register consists in DFF gates in series. The "SR_EN" input signal should be maintained to "0" to allow shifting through the SR. The "CKConf" clock is activated only for the loading to the SR / reading of the data. After loading into the SR the 2953 bits, a "loading" signal can be used to store the shift values inside corresponding latches:

For the "MatrixDigital" block:

- 1) For the bits localized between the "BLRes" and the "INJ_EN_AnaPassive" (see Figure 4.10), the loading signal used is "LdDAC".
- 2) For the bits localized between the "TRIM_EN" and the "REGULATOR_EN" (see Figure 4.10), the loading signal used is "LdPix"

For the pixel matrix:

- 1) Each pixel contains 1-bit shift (1 DFF) for 7 latches (7 configuration bits to store). The 7 configuration stored inside each pixel are:
Trim_EN: 4 bits local DAC.
INJECT_EN: enable the pixel to receive the injection signal (1 bit).
PREAMP_EN: enable the functioning of the pre-amplifier and the comparator of the pixel (1 bit).
MONITOR_EN: enable the output of the pixel to be read on the AMPOUT or MONITOR output PADS (1 bit).
- 2) The 1-bit shift storage inside one of these latches is activated by the signals: TRIM_EN, INJECT_EN, PREAMP_EN or MONITOR_EN.

4.2. Characterization before irradiation

4.2.1. Leakage current and breakdown voltage measurements

The measurement of the leakage current as a function of the high voltage applied is done before radiation at room temperature (25 °C). The two outmost pwell rings are connected to the external power supply and biased by reverse voltage. The diagram is shown in Figure 4.11. The breakdown voltage of LF_CPIX V1 is higher than 130 V, V2 shows better performance, the breakdown voltage is around 230 V, as shown in Figure 4.12. The leakage current of the chip is around 10 nA before the breakdown voltage in both versions. The new guard-ring strategy, which is implemented in LF_CPIX V2, can provide a smooth electric field distribution for the DNW-pixel and then improve the performance of the breakdown voltage, and match the simulation results (240 V) [102] [104]. As we know from the formula 2.5, the depletion depth is proportional to the silicon resistivity and the reverse bias on the junction. Since the resistivity (2 kΩ · cm) is the same between the 2 versions, we can expect a larger depletion region for the V2.

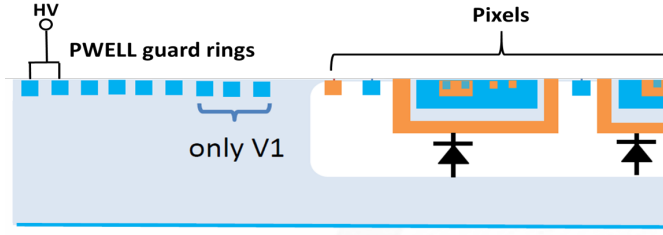


Figure 4.11. – Current voltage measurements setup on front-side of the chip

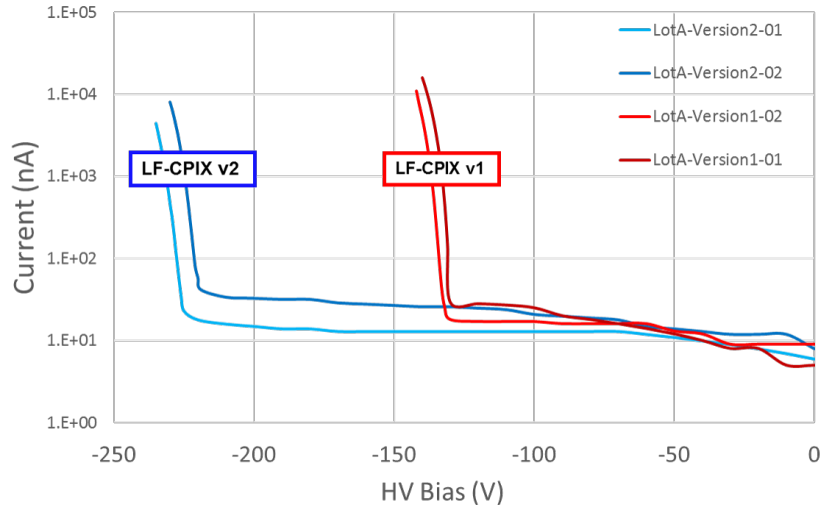


Figure 4.12. – Current voltage measurements of LF_CPIX V1 and V2

In the LF_CPIX chip it is allowed to bias the sensor either from the front side on Pwell pixel rings, or from the back side using substrate metallization, as shown in Figure 4.13. The current-voltage curve in the LF_CPIX V2 chip was measured using these two options (Figure 4.14). The breakdown voltage in both cases is around 230 V and there is no big difference between HV on Substrate or front-side. However, sensors biased on Substrate have a more uniform electric field, giving faster charge collection times and therefore higher radiation tolerances than top biased case.

In order to investigate the leakage current of the prototype with different chip thickness (250 μm and 750 μm), a comparison between the leakage current of the 250 μm thinned LF_CPIX and the 750 μm un-thinned LF_CPIX is shown in Figure 4.15. The breakdown voltage of both chips is higher than 220 V. But a little leakage current increases for the 250 μm chip is observed around -70 V, since the chip is fully depleted at this voltage.

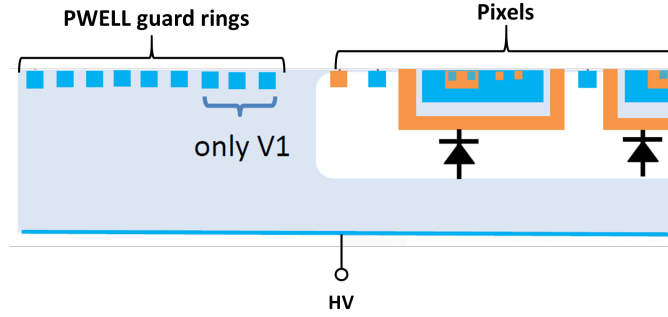


Figure 4.13. – Current voltage measurements setup on the substrate

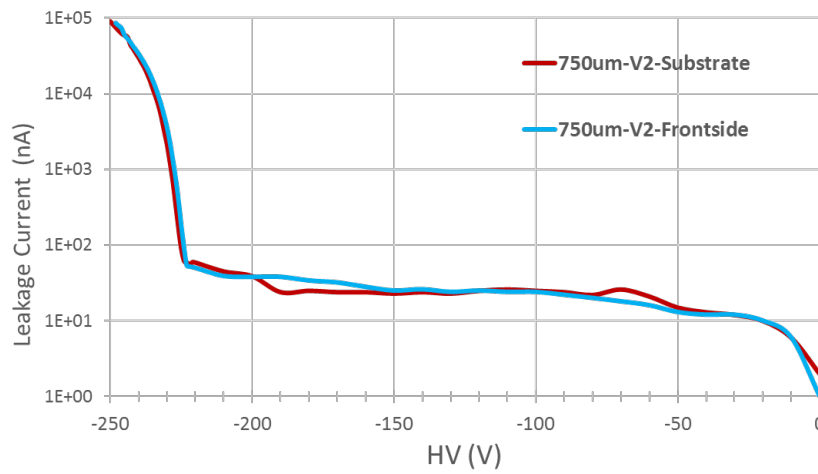


Figure 4.14. – Measurement of the leakage current as a function of the applied High Voltage on front-side and substrate (LF_CPIX V2)

4.2.2. Characterization of the pixel matrix

4.2.2.1. LF_CPIX test setup

In order to perform characterisation measurements with LF_CPIX prototype modules, a test setup was developed, as shown in Figure 4.16. It involved the GPAC (Generic Purpose Analog Card) and the Multi-IO boards, which are based on compact USBpix system [105]. The LF_CPIX chip is wire bonded on the DUT (Device Under Testing) board.

The diagram of the test setup system is shown in Figure 4.17. The Multi-IO board includes a programmable Kintex7 FPGA, SRAM Memory, USB2.0 Interface and a 8051 micro-controller with I2C and SPI functionalities [105]. It allows to communicate via Ethernet with a PC. The GPAC board is designed to extend the digital input and output capabilities of the Multi-IO board. It has analog blocks including four power supply channels, four voltage and twelve current source channels and also an injection pulse generator. Moreover, level shifters for CMOS

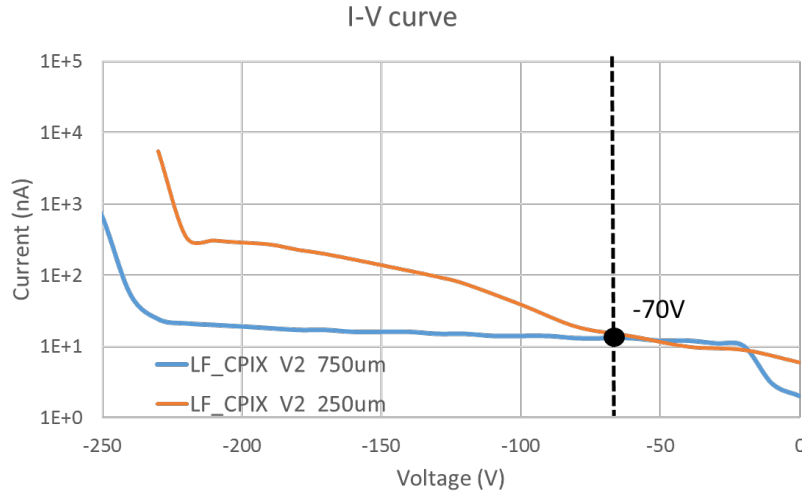


Figure 4.15. – A comparison between the leakage current of the 250 μm thinned LF_CPIX and the 750 μm un-thinned LF_CPIX

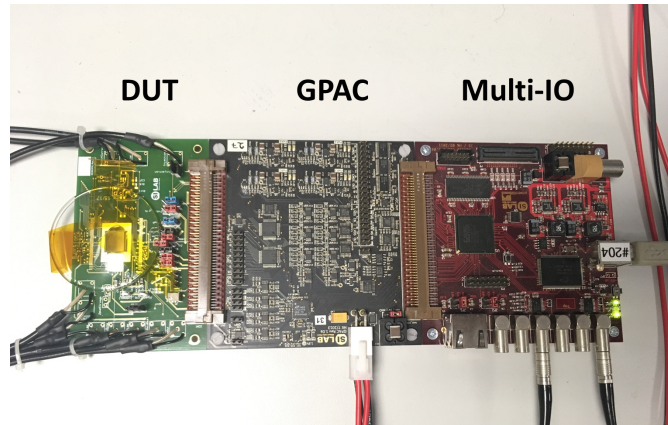


Figure 4.16. – Test setup based on GPAC and Multi-IO board

signals and low voltage differential signalling transmitters are available. This test setup can power and configure the LF_CPIX prototype without external power supplies.

4.2.2.2. Chip configuration and analog outputs characterization

The threshold voltage (T_h) and the baseline voltage ($BL=0.75\text{ V}$) are two important parameters which are biased by the GPAC board. The power voltages for digital cells ($V_{dd}=1.8\text{ V}$) and analog cells ($V_{dda}=1.8\text{ V}$) are also supplied by the GPAC board. The configuration of the DACs with default values is summarized in Table 4.1.

In the digital pixels block, three different pre-amplifier input transistors are im-

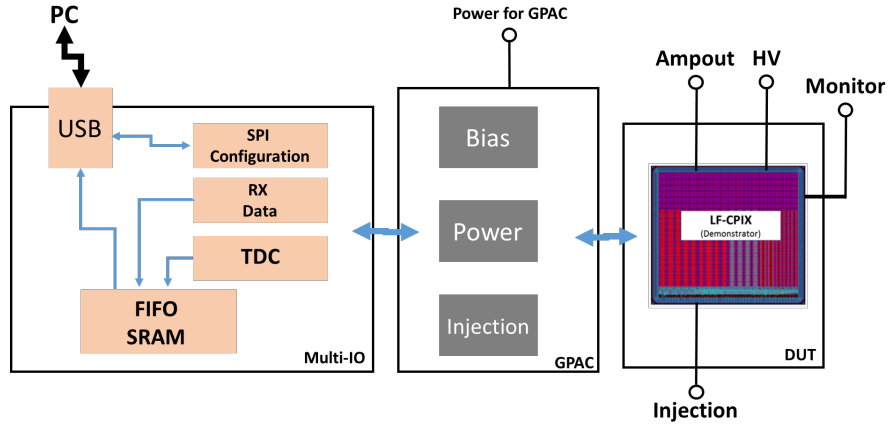


Figure 4.17. – The diagram of the test setup system

plemented. For the three flavors, both the pre-amplifier and discriminator could be shown to have response with external test injection. There are three important parameters (VPFB, Vamp and VLoad) related to the pre-amplifier performance. As said in section 4.1.2, the VPFB value (6 bits) can tune the feedback resistance value of the pre-amplifier. In order to see how the VPFB affects the behavior of pre-amplifier, the DAC of VPFB was varied from 1 to 60. Figure 4.18 gives the analog outputs of NMOS flavor by varying VPFB parameter. The leading edge as a function of VPFB DAC value for all three flavors is shown in Figure 4.19a, PMOS and CMOS flavors exhibit similar performance, the leading edge of NMOS is slightly faster than PMOS and CMOS. With the DAC value of VPFB increasing, the width of pre-amplifier output decreases, an effect particularly seen for VPFB DAC values below than 20, as shown in Figure 4.19b. In order to have fast leading edge and reasonable width output signal, the VPFB DAC should lie within 40 to 60, which is also match the typical value (47) setting in simulation.

The Vamp value (6 bits) tunes the biasing of the pre-amplifier. Figure 4.20 gives an example of the results we get for the NMOS flavor by varying Vamp from 1 to 60. The value of the leading edge as a function of Vamp for all three flavors is shown in Figure 4.21a. It decreases a lot at the beginning ($V_{amp} < 10$), and becomes stable afterwards. The amplitude of the signal at the output of the pre-amplifier can also be represented as a function of different Vamp, as shown in Figure 4.21b. It increases rapidly when Vamp is less than 20 and becomes stable after when Vamp is higher than 20. In order to have fast and high amplitude output signal, the ideal Vamp value should lie within 20 to 60, this range includes the typical value (26) during the simulation period.

The VLoad value (6 bits) tunes the bias of the pre-amplifier load. Figure 4.22 gives an example of the outputs of NMOS flavor pre-amplifier by varying VLoad from 1 to 60. The leading edge as a function of VLoad for all three flavors is shown in Figure 4.23a, the performance of the three flavors is similar, the leading

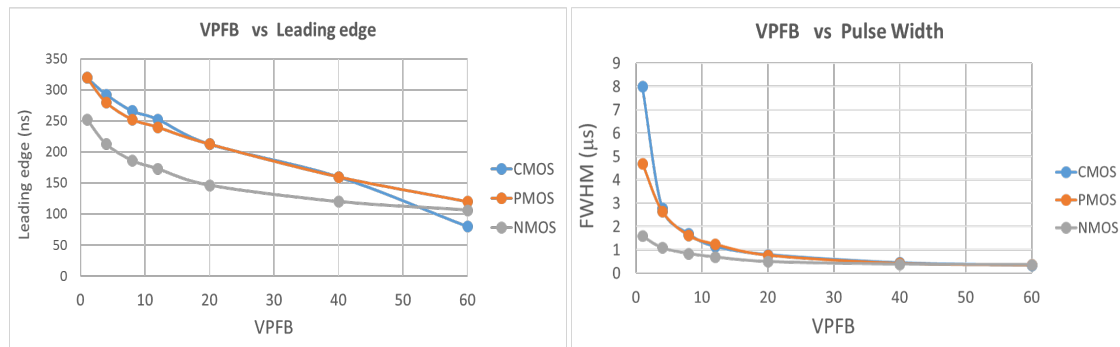
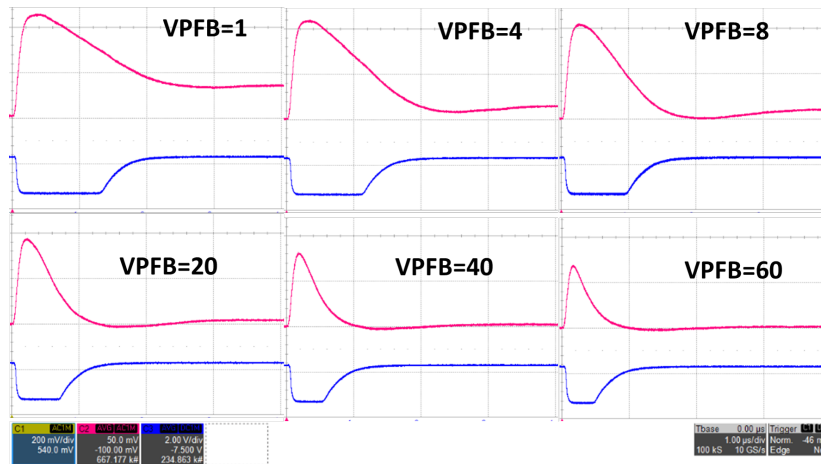


Figure 4.19. – Leading edge and Pulse width as a function of VPFB.

edge decreases a lot for small VLoad values ($VLoad < 10$) and stabilizes when increasing $VLoad > 10$. The amplitude only increases a little bit for small VLoad DAC values ($VLoad < 4$), and becomes stable afterwards, as shown in Figure 4.23b. Therefore setting the VLoad to a value between 10 to 60 would allow the pre-amplifier output to be fast.

4.2.2.3. Injection capacitance calibration with a ^{55}Fe source

In order to know the charge injected by external injection, the injection capacitance (C_{inj} shown in Figure 4.9) was calibrated with a ^{55}Fe radioactive source. The set-up is shown in Figure 4.24. The waveforms recorded when illuminating the LF_CPIX V2 prototype with a ^{55}Fe source and when using external injection were acquired with an oscilloscope. The sensor was biased at -100 V on front side at the same time. The spectra was obtained with the sensor biasing at -200 V and

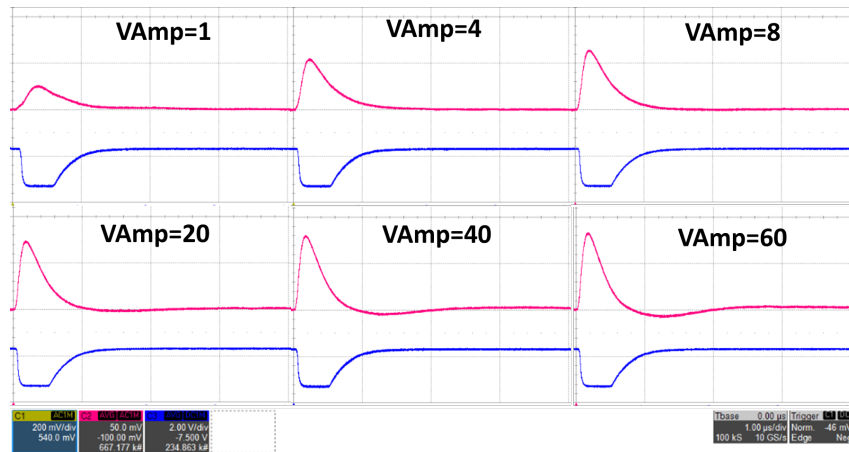
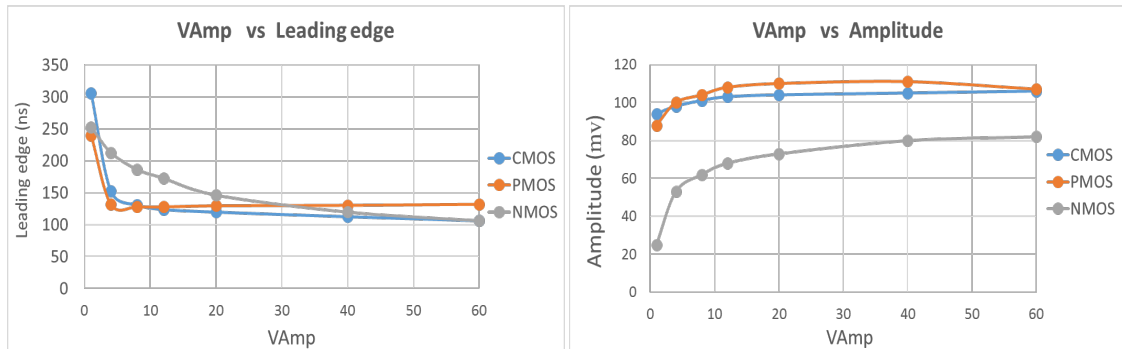


Figure 4.20. – The analog outputs of NMOS flavor by varying Vamp parameter (Pink: Pre-amplifier output, Blue: Discriminator output).



(a) Leading edge vs VAMP

(b) Amplitude vs VAMP

Figure 4.21. – Leading edge and amplitude as a function of Vamp.

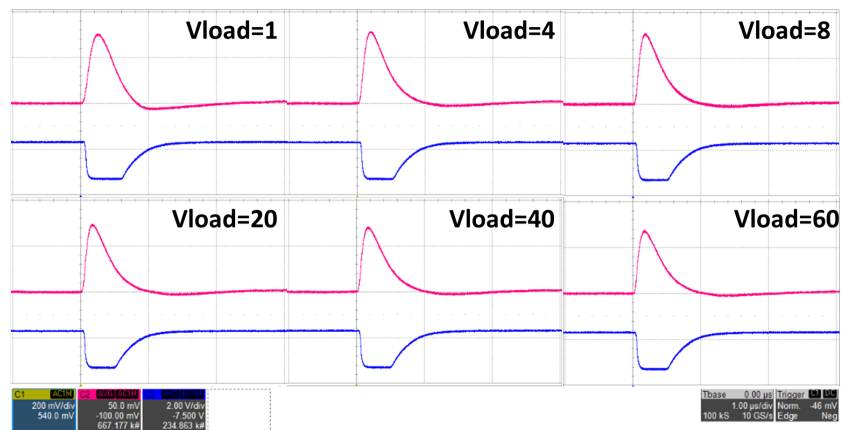
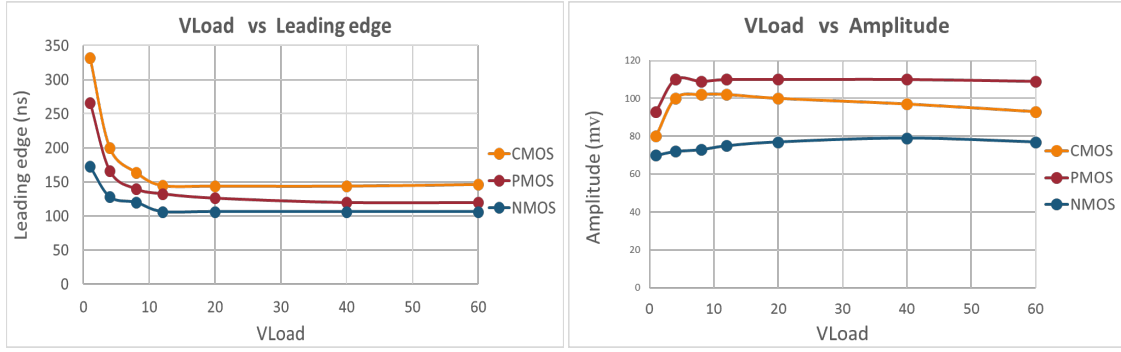


Figure 4.22. – The analog output of NMOS flavor by varying VLoad parameter (Pink: Pre-amplifier output, Blue: Discriminator output).

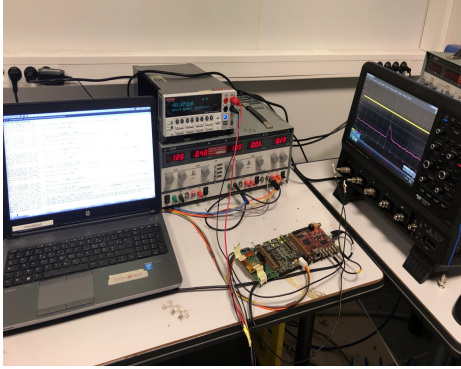


(a) Leading edge vs VLoad

(b) Amplitude vs VLoad

Figure 4.23. – Leading edge and amplitude as a function of VLoad.

an external injection of 1 V, as shown in Figure 4.25. The characteristic peak of the X-ray source spectrum (blue histogram) and external injection spectrum (red histogram) can be clearly seen.



(a) Set-up for calibration



(b) ^{55}Fe on sensor

Figure 4.24. – The set-up for injection capacitance calibration with ^{55}Fe source

As it is well known, the ^{55}Fe source emits X-rays with a characteristic peak of 5.9 keV energy, corresponding to around 1640 e- of deposited charge in the detector, so the spectrum peak of 1 V external injection can be calibrated at 12474 e-, the injection capacitance can be calculated using the equation,

$$C_{inj} = \frac{N \times e}{V_{inj}} \quad (4.3)$$

where C_{inj} is the injection capacitance, N is the electron number injected by 1 V external injection (12305 e-), e is elementary charge ($1.6 \times 10^{-19} \text{C}$) and V_{inj} is the external injection voltage. The result from this measurement is 1.97 fF. This value is almost the same as the design value 2.0 fF.

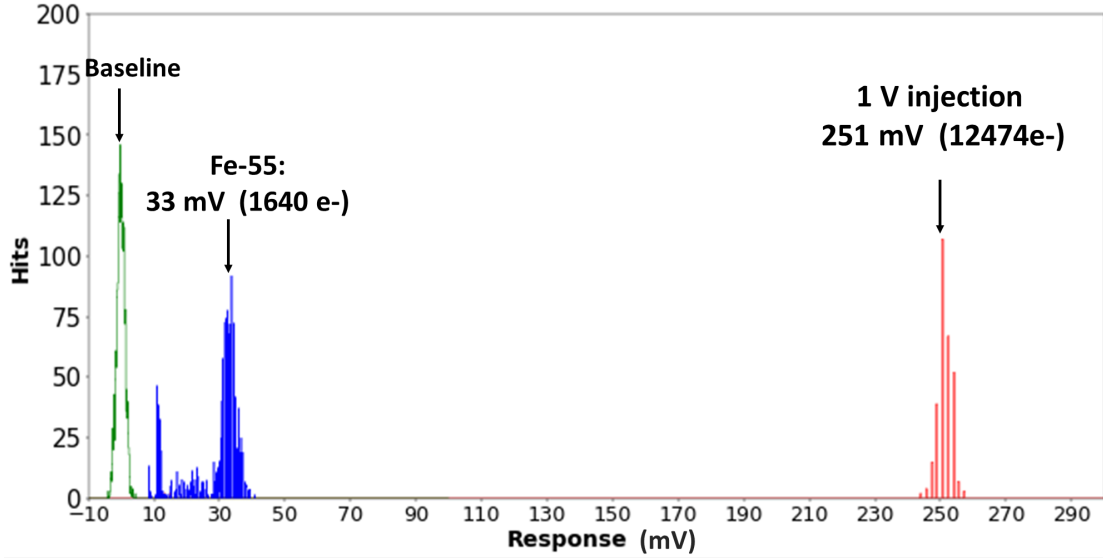


Figure 4.25. – ^{55}Fe source and external injection spectra obtained

4.2.2.4. Threshold scan and injection scan measurements

The three discriminator flavor outputs are connected to the HIT register, which stores hit/no-hit binary information coming from the in-pixel discriminator, as shown in Figure 4.26. So the scan test can be easily done by using the HIT register. Basically, two types of scan can be done:

- The threshold scan: the injection voltage is fixed, and the threshold varies from a low to a high value (Typical range: 0 V to 0.6 V).
- The injection scan: the threshold voltage is fixed, and the injection voltage varies from a low to a high value (Typical range: 0 V to 1.0 V).

One hundred test charges were sent to the pixel at each scan step via the injection capacitor (C_{inj} in Figure 4.9). Ideally, this process would produce a step function, with zero injections resulting in a hit for any charge below threshold and all injections resulting in hits for any charge above threshold. However, due to the electronic noise of each front-end channel, this step function turns into an S-curve shape [106]. For both types of scan, the S-curve can be fitted with the error function,

$$erf(x) = \frac{2}{\sqrt{\pi}} \int_0^{\frac{x-n}{\sigma}} e^{-t^2} dt \quad (4.4)$$

where x is the threshold (or injection) value at each scan step, n is the threshold (or injection) at 50% efficiency and σ is the noise.

In the case of the threshold scan, the amplitude of the test pulse corresponding to 50% efficiency (threshold) and noise of the single pixel can be extracted from the fitting curve, as shown in Figure 4.27a. The amplitude is the threshold where

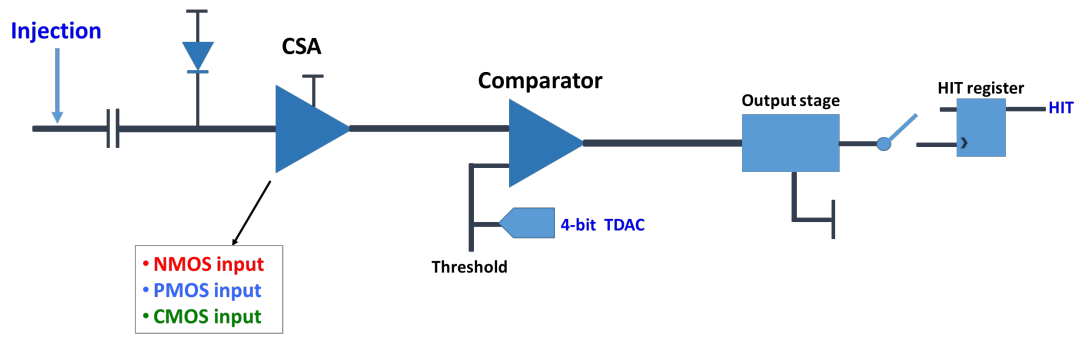


Figure 4.26. – The Readout circuitry LF_CPIX

the efficiency is 50%. The noise is measured from the slope of the turn-on region. The error function fit parameters are the amplitude and noise. Then the gain of the pixel can be calculated by using the pixel amplitude with fixed injection. Similarly for the injection scan, the threshold and noise of the signal can be extracted from the fitting curve, as shown in Figure 4.27b. The threshold is the injection charge where the efficiency is 50%. The noise is measured from the slope of the turn-on region as well. The error function fit parameters are the threshold and noise.

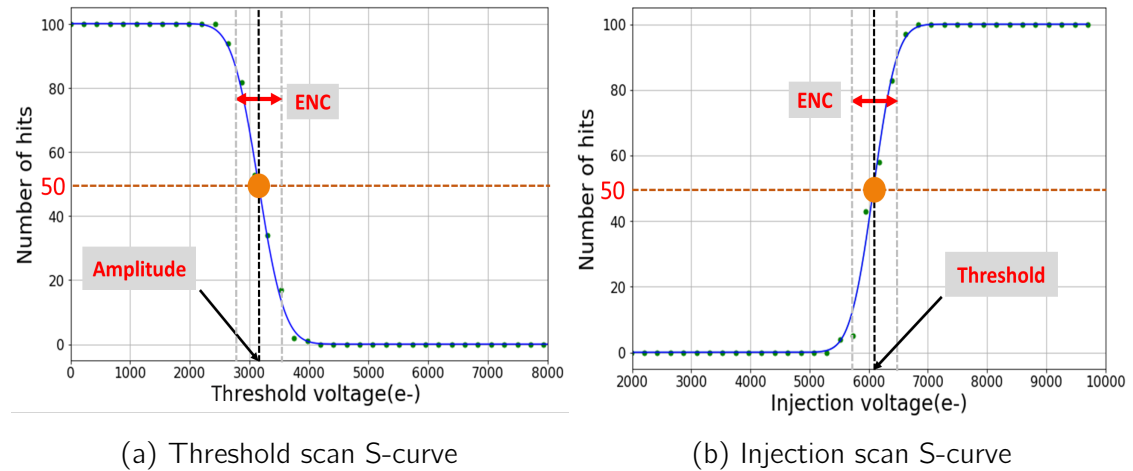


Figure 4.27. – The 2 types of scan: (a) Threshold scan S-curve (b) Injection scan S-curve

Threshold scan was performed to investigate the gain of the three different flavors. Injection signal from the GPAC board was fixed at 400 mV, the value of the injection capacitance is 1.97 fF, which was calibrated by ^{55}Fe radioactive source, so the equivalent injection value is 4000 e-. The baseline (BL) of the output was set at 0.75 V and the threshold scan was performed from 1.00 V to 0.75 V in 26 steps of 10 mV. For each step, the hit occupancy per pixel was determined, and the resulting curve was fitted with an S-curve fit. This scan was

performed at TDAC = 7, which is the middle value of the dynamic range, and Table 4.1 gives the other DAC settings used (default values). The gain of each pixel can be obtained from equation (4.5),

$$Gain(\mu V/e) = Amplitude(\mu V)/Injection(e) \quad (4.5)$$

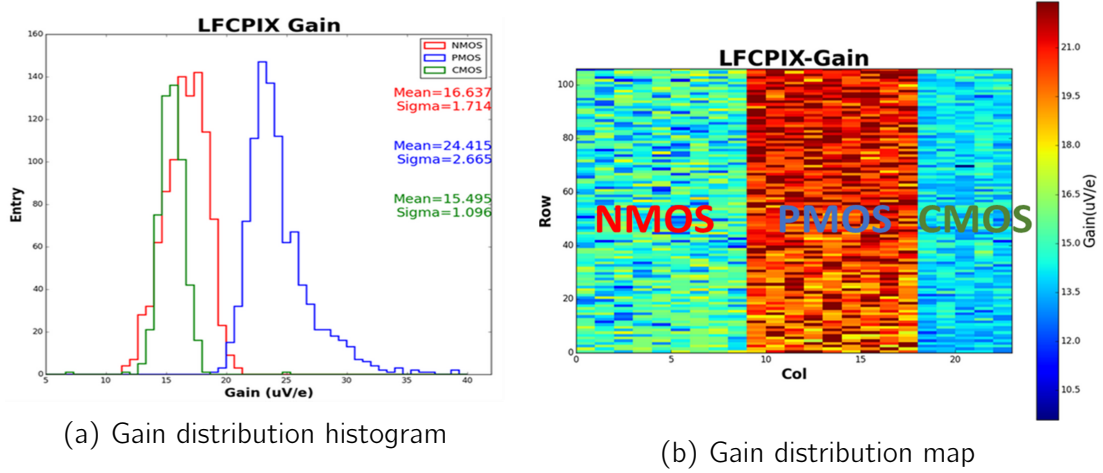


Figure 4.28. – The gain distributions for all three flavors

The gain distributions as well as maps of all three flavors are shown in Figure 4.28. The mean gain value for the NMOS flavor is $16.6 \mu V/e$ -, which agrees very well with the simulation results ($16.5 \mu V/e$ -), as shown in Figure 4.29a.

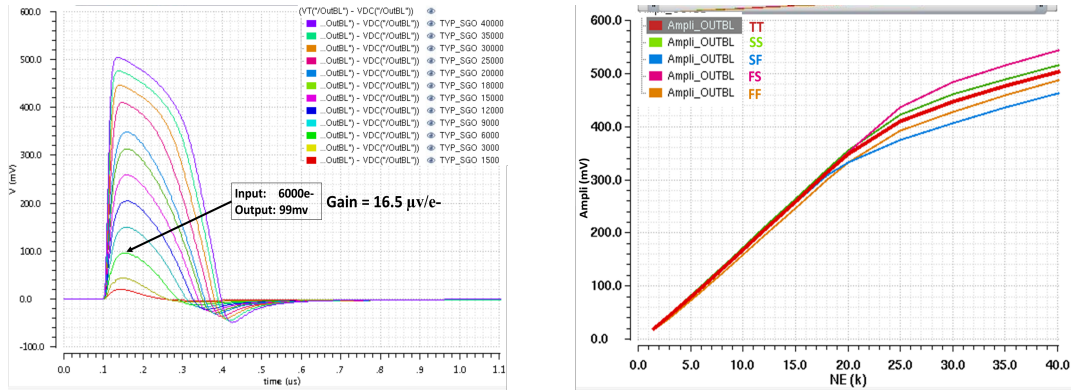
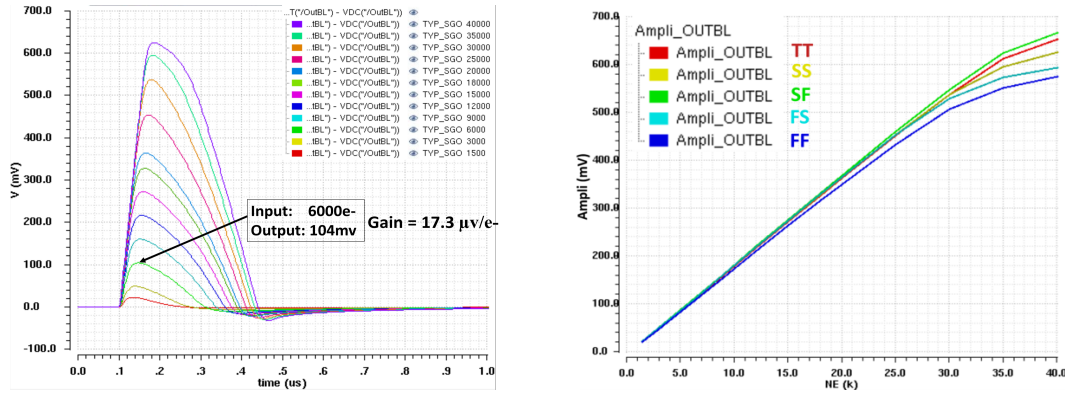


Figure 4.29. – NMOS pixel pre-amplifier output signal simulation results

The PMOS flavor shows higher gain than NMOS flavor. The mean gain value for the PMOS flavor is $24.4 \mu V/e$ - and this value is higher than what was expected from simulation ($17.3 \mu V/e$ -) in Figure 4.30a. The difference is probably due

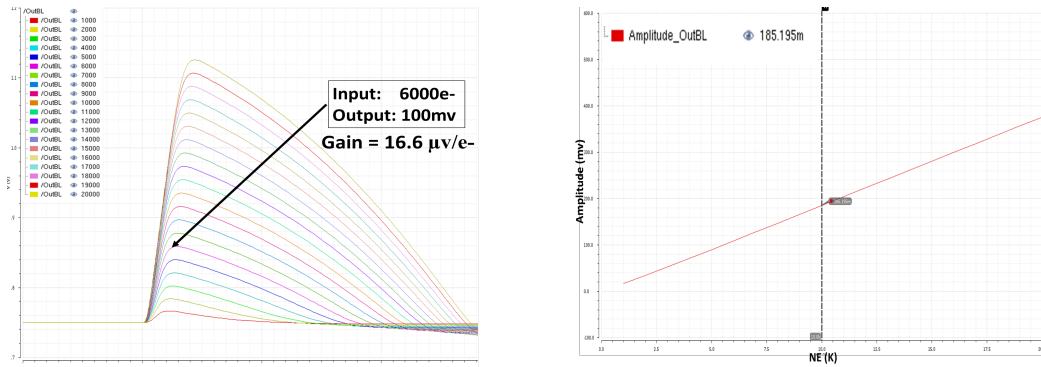


(a) Output signal versus number of electrons (b) Amplitude versus number of electrons

Figure 4.30. – PMOS pixel pre-amplifier output signal simulation results

to the nonlinear simulation result (blue line in Figure 4.30b) in worse FF case (Fast N-type and Fast P-type transistor).

The mean gain for the CMOS pixel flavor is $15.4 \mu\text{V}/e^-$, this value is nearly the same as simulation value ($16.6 \mu\text{V}/e^-$), as shown in Figure 4.31.



(a) Output signal versus number of electrons (b) Amplitude versus number of electrons

Figure 4.31. – CMOS pixel pre-amplifier output signal simulation results

The gain at three different injection amplitudes (0.7 V, 1 V and 1.3 V) is shown in Figure 4.32. From this graph, we can see that the NMOS and CMOS flavors are not affected by this change. This matches the amplitude linearity simulation results in Figure 4.29b and Fig 4.31b. The gain of PMOS flavor is stable at the injection amplitude 0.7 V and 1.0 V, but it increases at high injection amplitude (1.3 V), the gain dispersion increases as well. This difference could be explained by the degradation of the linearity observed for some corners, as illustrated by the Figure 4.30b in which the linearity for FF (Fast N-type and Fast P-type transistor) corner is getting worse after 15 ke- input.

The injection scans were also performed for all three flavors to investigate the threshold uniformity and noise of the three different flavors. The global three-

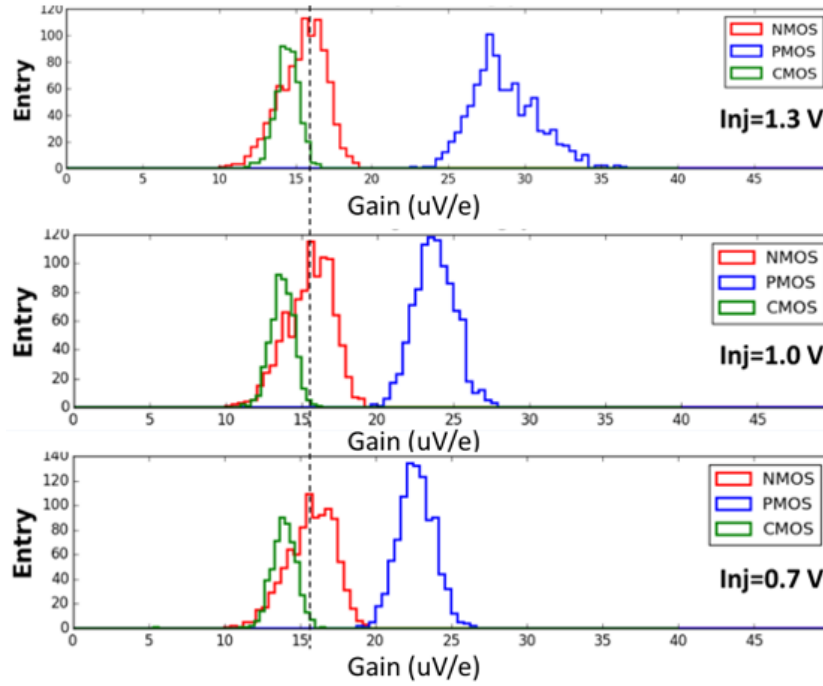


Figure 4.32. – The gain distributions at three different injection values

shold (Th) and the baseline (BL) biased by GPAC board were fixed at 0.78 V and 0.75 V, respectively and the injection signal scan was performed from 0 V to 0.60 V in 61 steps of 10 mV. The hit occupancy per pixel was determined, and the resulting points were fitted.

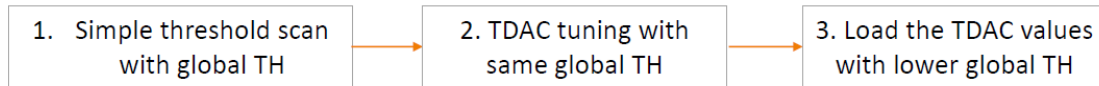


Figure 4.33. – The injection scan measurements procedure

In the pixel detector, each pixel in the matrix has an adjustable threshold, measured in electrons. Proper setting of the threshold for each pixel is necessary to achieve both high efficiency and good position resolution. This threshold should be high enough to avoid registering fake hits caused by noise in the readout electronics. On the other hand, the threshold should be low enough to register the charge from a minimum ionizing particle with high efficiency. A minimum ionizing particle typically generates approximately 20 ke- while perpendicularly traversing the the 300 μm thick silicon sensor, but this charge is usually distributed among several neighbour pixels, producing a cluster of hits. If the threshold is too high, some of these hits will be lost and the clusters can be split or mis-measured, introduce errors in position resolution [25].

In order to uniformize the threshold of the matrix and find a proper threshold for all the pixels, injection scan measurement was done in three steps, as shown in Figure 4.33. For the first step, the injection scans were performed with fixed global TH and local TDAC (value 7) for all the pixels. The global TH value should be a little bit high since the threshold dispersion is big before tuning, otherwise some pixels with high noise can not be recorded. The mean threshold, dispersion and noise of the matrix can be calculated in this step. For the second step, the mean threshold obtained in first step was set as the target value, then TDAC tuning was performed to tune the threshold of each pixel to the target value, so the reduced threshold dispersion at the same global TH as the first step can be achieved, and the proper TDAC value for each pixel can also be obtained. For the third step, the proper TDAC value for each pixel was loaded to each pixel during the injection scans, but with a lower global TH.

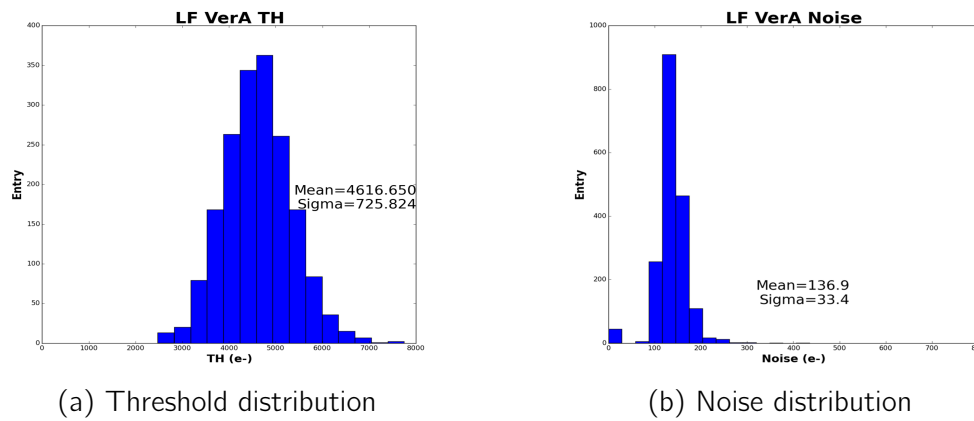


Figure 4.34. – Threshold and noise distributions of CCPD_LF before TDAC tuning

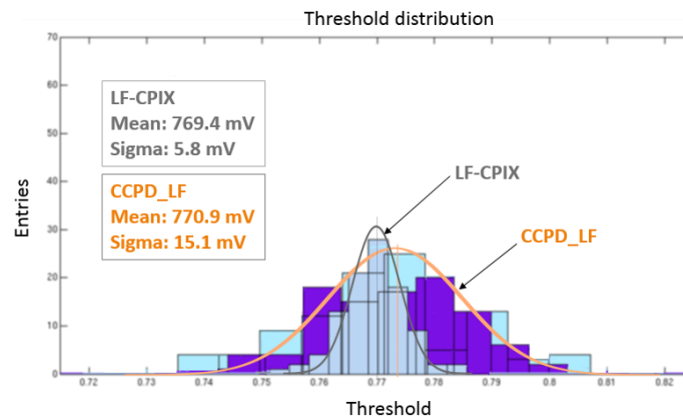


Figure 4.35. – The simulation of threshold dispersion for the CCPD_LF chip and the LF_CPIX chip

During the previous threshold scan tests, the CCPD_LF chip has shown a large

threshold dispersion (over 700 e⁻), as shown in Figure 4.34a [83]. This dispersion has been identified to be mainly due to the discriminator cell. Therefore the discriminator of LF_CPIX chip has been improved to limit its mismatch. The simulation in Figure 4.35 shows the improvement of the LF_CPIX threshold dispersion which should be decreased by a factor ~ 2.6 .

The three steps measurements were implemented for NMOS flavor of 250 μm LF_CPIX V2 prototype with global TH = 7.8 V, HV = -100 V and default DAC settings. A threshold scan was firstly done for all the pixels of the NMOS flavor, the superposition of these S-curves (954 pixels) is shown in Figure 4.36. The threshold and noise were extracted from the individual pixel S-curves. Figure 4.37 shows the threshold dispersion and noise distributions for the NMOS pixel flavor before TDAC tuning. Compared to CCPD_LF, the dispersion of LF_CPIX shrinks to 395 e⁻, and the noise is also decreased, reaching 100 e⁻.

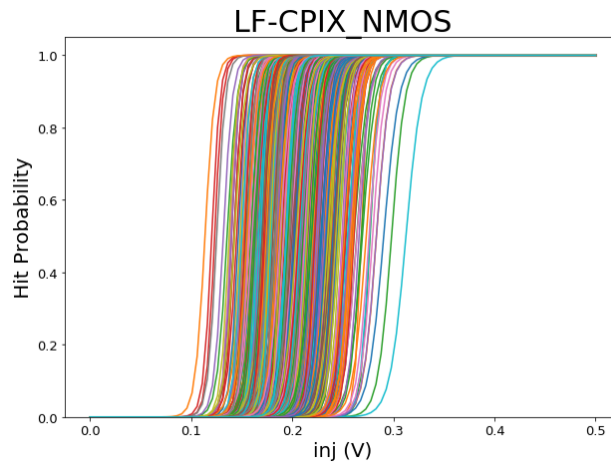
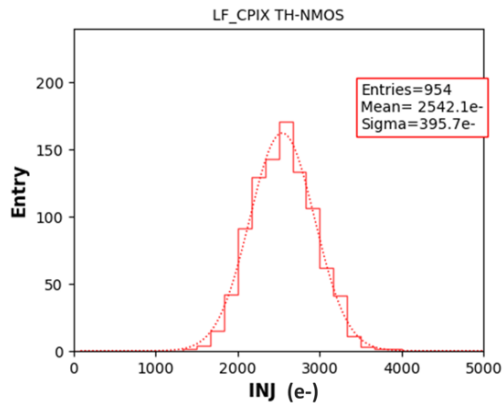


Figure 4.36. – The injection scan S-curves for NMOS flavor before tuning

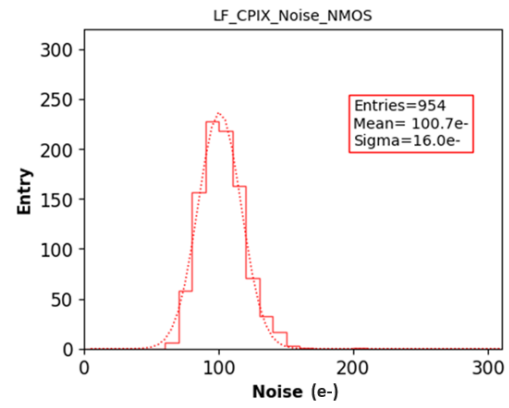
In the second step, TDAC tuning was done, the proper TDAC value of each pixel shown in Figure 4.38a was found to reduce the threshold dispersion. Since the mean threshold measured in the first step was set as the target threshold value, a Gaussian like TDAC distribution can be seen in Figure 4.38b. The threshold dispersion distribution maps of NMOS pixels before and after tuning are shown in Figures 4.39a and 4.39b respectively. Reduced dispersion from 395 e⁻ to 63 e⁻ (84 % reduction) was observed with the threshold of approx. 2500 e⁻. All the NMOS pixels can be tuned close to the target value.

In the last step, injection scans were done with the tuned TDAC values at a lower global TH, and a mean threshold of approx. 1400 e⁻ could be reached with a dispersion of 123 e⁻, as shown on Figure 4.40. As a final result of this three step procedure, all the NMOS pixels can work at relatively low threshold (~ 1400 e⁻) and good threshold uniformity.

The three steps measurements were also carried out for PMOS and CMOS flavors and similar results as NMOS flavor were obtained. For the PMOS flavor, the

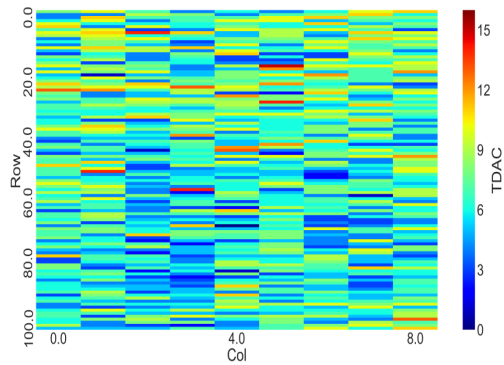


(a) Threshold distribution

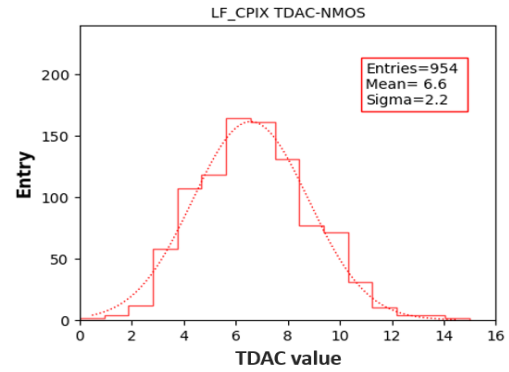


(b) Noise distribution

Figure 4.37. – Threshold and noise distributions for NMOS flavor before TDAC tuning

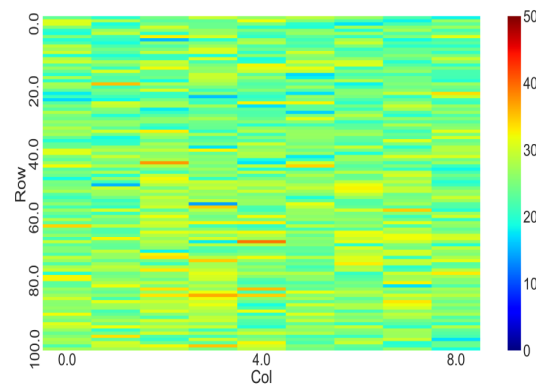


(a) TDAC map

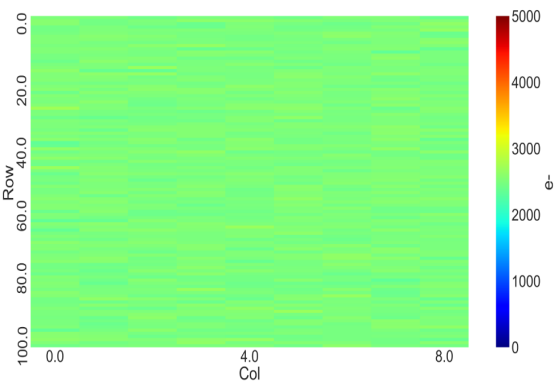


(b) TDAC distribution

Figure 4.38. – TDAC value map and histogram after tuning for NMOS flavor



(a) Un-tuned



(b) Tuned

Figure 4.39. – Threshold map for NMOS flavor before and after TDAC tuning

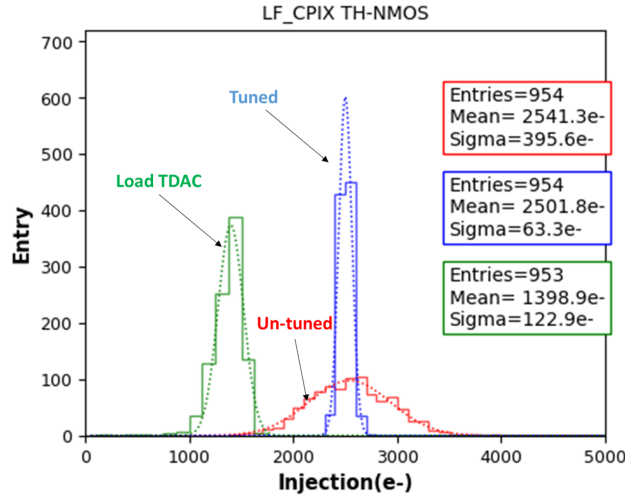


Figure 4.40. – Threshold distributions for NMOS flavor pixels in three cases: untuned (red), after tuning at high TH (blue), after using recorded value at relatively low TH (green).

dispersion of the threshold could be tuned from 270 e- down to 54 e- (80 % reduction), with a mean threshold of 2630 e-. With further lowering the threshold down to approx. 1500 e-, we reached a dispersion of 75 e-, as shown on the corresponding figures from Figure 4.41 to Figure 4.45.

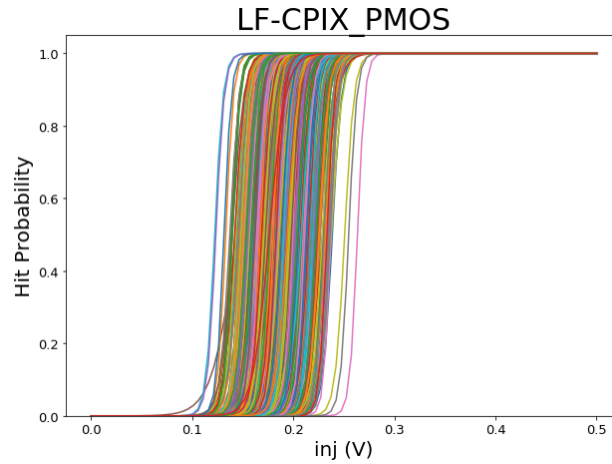


Figure 4.41. – The injection scan S-curves for PMOS flavor before tuning

Concerning the CMOS flavor, the dispersion of the threshold could be tuned down from 461 e- to 78 e- (83% reduction), at the threshold of approx. 2500 e-. The mean threshold for the CMOS flavor could then be lowered down to 1600 e- with a dispersion of 109 e-, as shown on the corresponding figures from Figure 4.46 to Figure 4.50.

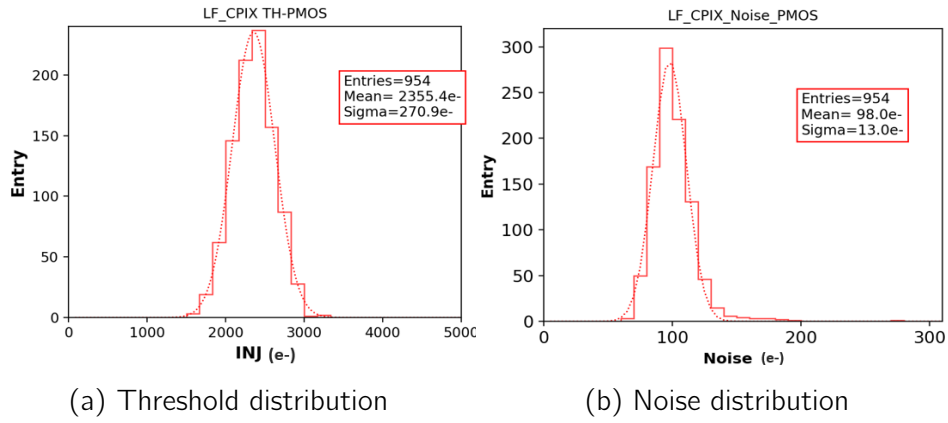


Figure 4.42. – Threshold and noise distributions for PMOS flavor before TDAC tuning

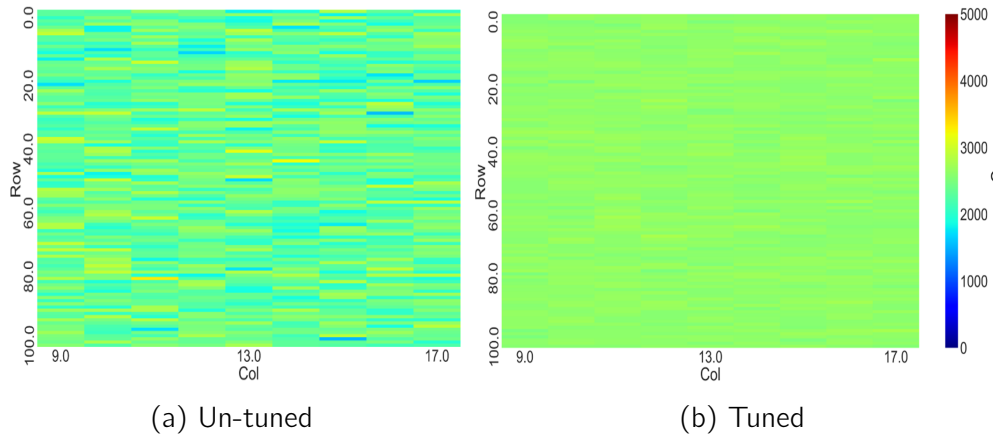


Figure 4.43. – Threshold map for PMOS flavor before and after TDAC tuning

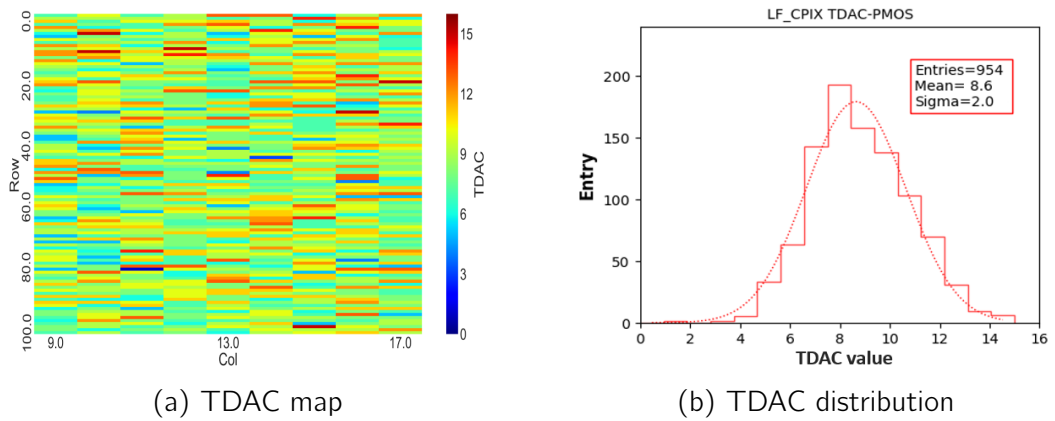


Figure 4.44. – TDAC value map and histogram after tuning for PMOS flavor

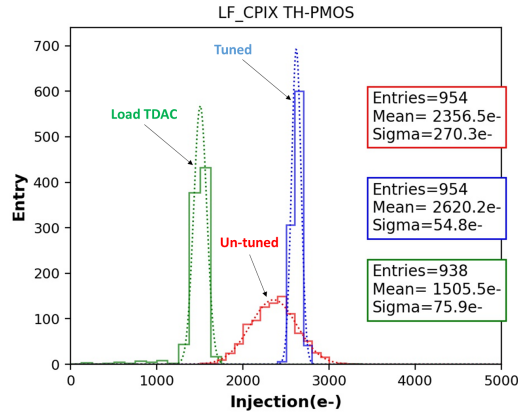


Figure 4.45. – Threshold distributions for PMOS flavor pixels in three cases: untuned (red), after tuning at high TH (blue), after using recorded value at relatively low TH (green).

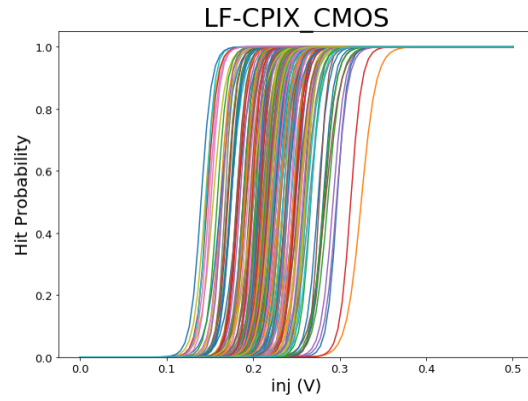


Figure 4.46. – The injection scan S-curves for CMOS flavor before tuning

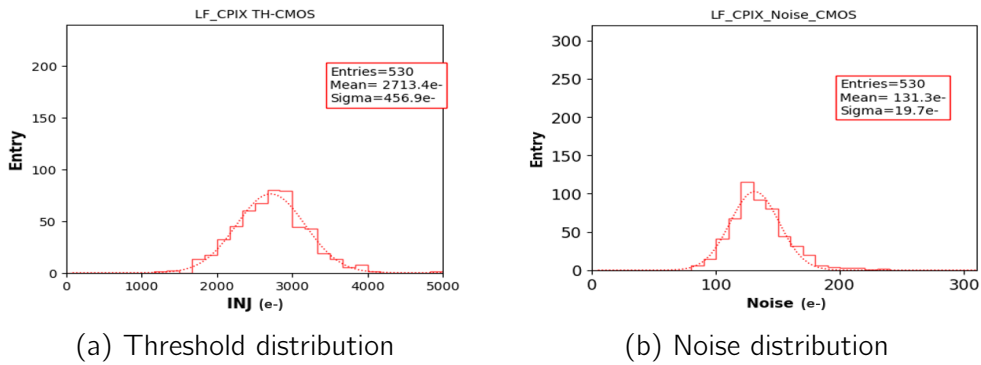


Figure 4.47. – Threshold and noise distributions for CMOS flavor before TDAC tuning

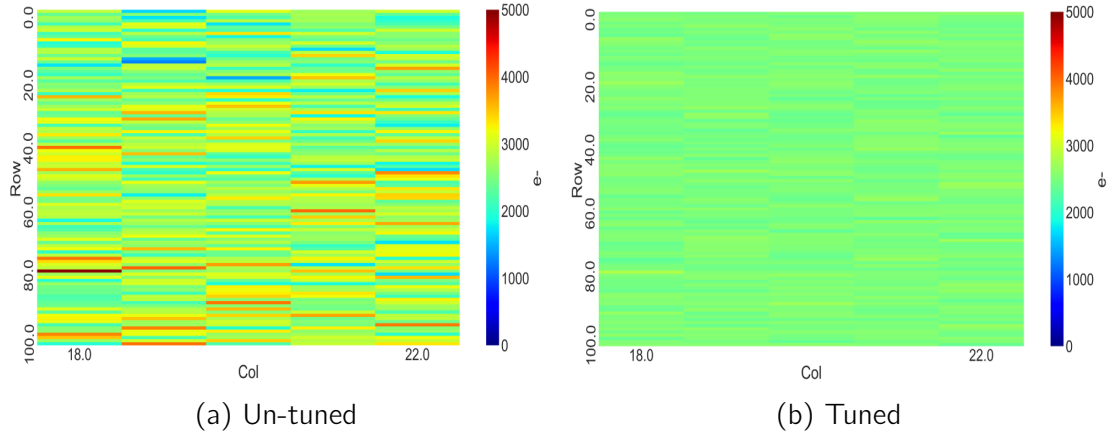


Figure 4.48. – Threshold map for CMOS flavor before and after TDAC tuning

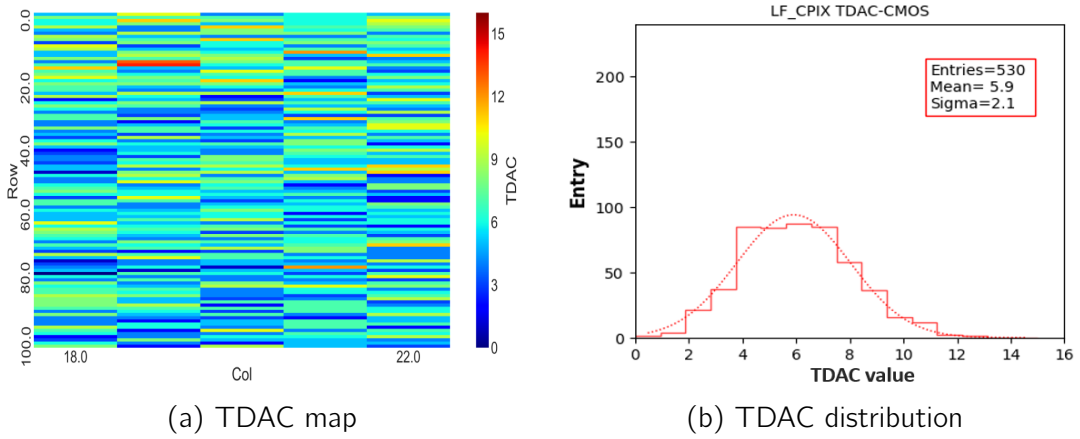


Figure 4.49. – TDAC value map and histogram after tuning for CMOS flavor

As a result of the threshold scan for all three flavors, it could be shown that the threshold dispersion of LF_CPIX is significantly improved by implementing the optimized discriminator design. In particular for PMOS flavor, the threshold dispersion is only 270 e- before tuning. Compared to CCPD_LF, the noise of LF_CPIX is also slightly lower (approx. 40 e- reduction). It has to be noted however that contrary to the simulations, the use of the CMOS input pre-amplifier does not result in a lower noise value than the use of NMOS or PMOS pre-amplifiers. A summary of LF_CPIX with NMOS, PMOS and CMOS results is shown in Table 4.3. The mean threshold values for all flavors can be tuned down around 1500 e-, and threshold dispersion less than 80 e-. The mean noise of CMOS flavor is 131 e-, which is nearly the same as expected from simulation 127 e-. The mean noise of NMOS and CMOS are slightly lower than CMOS flavor, which needs more investigation and simulation.

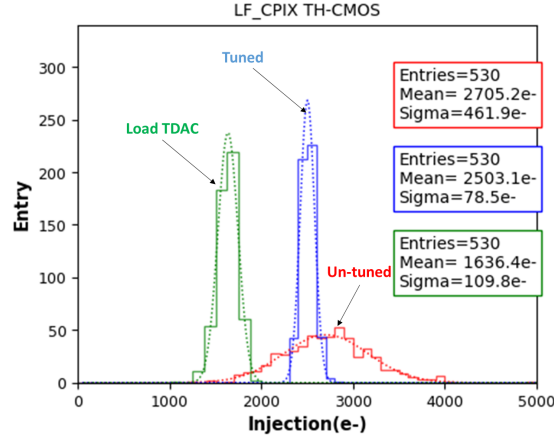


Figure 4.50. – Threshold distributions for CMOS flavor pixels in three cases: untuned (red), after tuning at high TH (blue), after using recorded value at relatively low TH (green).

LF_CPIX	NMOS	PMOS	CMOS
mean_th	2542 e-	2356 e-	2705 e-
low_mean_th	1398 e-	1505 e-	1636 e-
th_dispersion_un-tuned	395 e-	270 e-	461 e-
th_dispersion_tuned	63 e-	54 e-	78 e-
noise	100 e-	98 e-	131 e-

Table 4.3. – The recapitulative table of LF_CPIX with NMOS, PMOS and CMOS results

4.3. Characterization under proton beam

The use of a proton beam facility is interesting in that it can cause ionizing and non-ionizing effects in silicon devices at the same time. In order to investigate the radiation hardness of the prototype, LF_CPIX chips were irradiated in August 2017 at the 24 GeV IRRAD proton facility in CERN at room temperature up to a Total Ionizing Dose (TID) of 150 Mrad and Non-Ionizing Energy Loss (NIEL) of $3.42 \times 10^{15} \text{ neq} \cdot \text{cm}^{-2}$. This value is a good reference in that it is roughly 2 times the dose expected for the fifth pixel layer (L4) lifetime in the new ATLAS tracker ITk upgrade. The three prototypes that were mounted on the beam table are listed in Table 4.4. LF_CPIX1 and LF_CPIX2 are the 750 μm thick chips with V1 and V2 guard-rings strategies respectively. The LF_CPIX3 one is a 250 μm thickness chip with V2 guard-rings strategy. LF_CPIX1 was installed with in a passive setup, for which the chip is powered, but only the power consumption and leakage current could be monitored from the control room during the radiation. LF_CPIX2 and LF_CPIX3 were controlled with an active setup on the table.

It means that these two boards could be completely monitored from the control room allowing analog output and scan measurements.

Prototype ID	Chip thickness	Guard-ring strategy	Setup
LF_CPIX1	750 μm	V1	Passive
LF_CPIX2	750 μm	V2	Active
LF_CPIX3	250 μm	V2	Active

Table 4.4. – Prototypes irradiated in the August 2017 irradiation campaign

4.3.1. Radiation test facility and setup development

4.3.1.1. Radiation facility introduction

The Proton Synchrotron (PS) is a key component in the CERN accelerator complex that accelerates the protons provided by the proton synchrotron booster or heavy ions from the Low Energy Ion Ring (LEIR). The IRRAD proton facility as shown in Figure 4.51, is located on the T8 beamline of the CERN PS East Hall, where a primary proton beam with a momentum of 24 GeV/c is extracted from the PS ring [107]. Figure 4.52 gives a more detailed layout of the IRRAD proton facility [108]. The three LF_CPIX prototypes were installed on the beam table in Zone 2 and characterized from the control room during the radiation. This table can be controlled remotely, providing the possibility to move the DUT with ± 0.1 mm precision in the transversal plane (X-Y) with respect to the beam axis. The table also rotates over the azimuthal angle (θ) in order to achieve a precise alignment with the beam within $\pm 0.025^\circ$. The prototypes on the irradiation table are shown in Figure 4.53.

Since there is around a 20 m distance between the irradiation zone and the control room, the facility is equipped with a patch-panel in the control room and in the IRRAD zone respectively, providing the users the possibility to perform on-line measurements during the irradiation experiments [109], as shown in Figure 4.54. The connector list for the patch-panel is shown in Table 4.5. BNC, DB37 and RJ-45 connectors can be used for analog and digital signal transmission, while BURNDY connectors are for chip powering and polarization.

4.3.1.2. Beam parameters and monitoring

The IRRAD beam is delivered by the PS in "spills" with particles of momentum 24 GeV/c and a maximum intensity of $\sim 5 \times 10^{11}$ protons per spill of about 400 ms duration. Several spills per PS super cycle can be delivered to IRRAD resulting in a variable beam intensity depending on the number of users simultaneously served by the whole CERN accelerator complex [110]. The typical cycle period

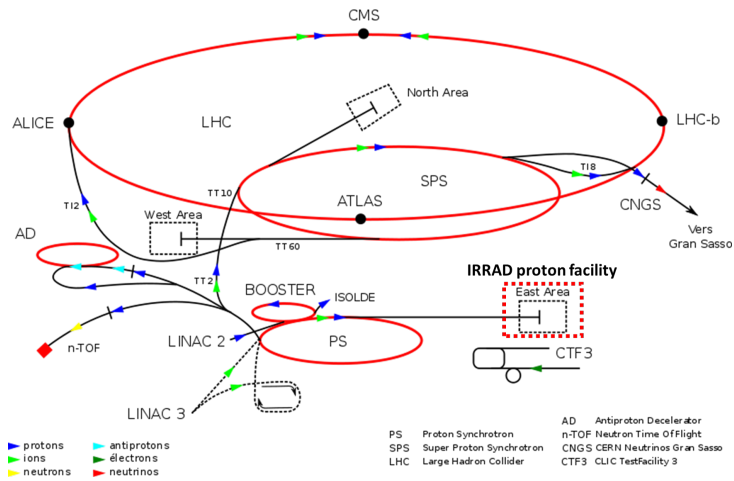


Figure 4.51. – The IRRAD proton facility location at CERN accelerator complex

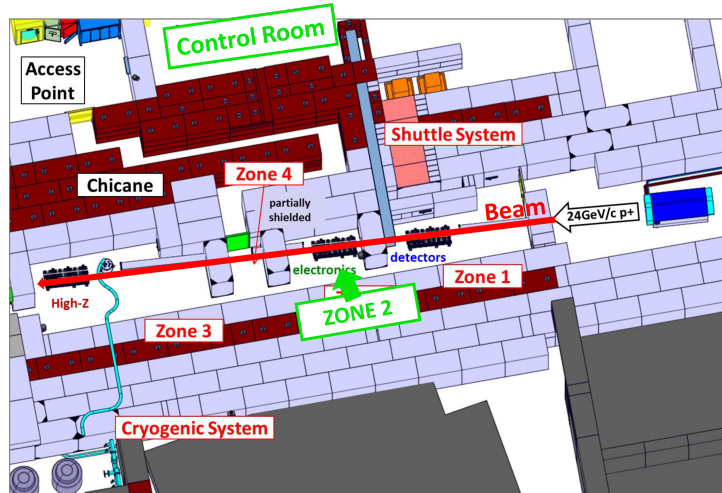


Figure 4.52. – Detailed layout of the IRRAD proton facility

Connector type	Comments
BNC	Analog signals and HV connection
BURNDY 12-contacts Female	Digital signal and chip polarization
BURNDY 19-contacts Female	Digital signal and chip polarization
220 V Swiss Plug	powering

Table 4.5. – The summary of patch panel connectors

is 30-37 s with 3 spills in each cycle. The standard beam spot size (FWHM) is $12 \times 12 \text{ mm}^2$, however the beam spot size (FWHM) can be from $6 \times 6 \text{ mm}^2$ to $20 \times 20 \text{ mm}^2$.

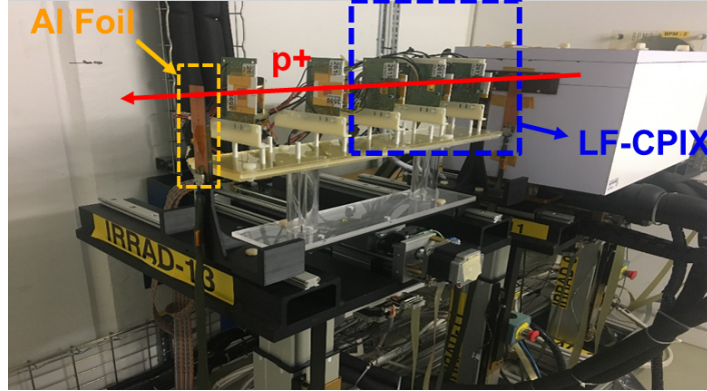
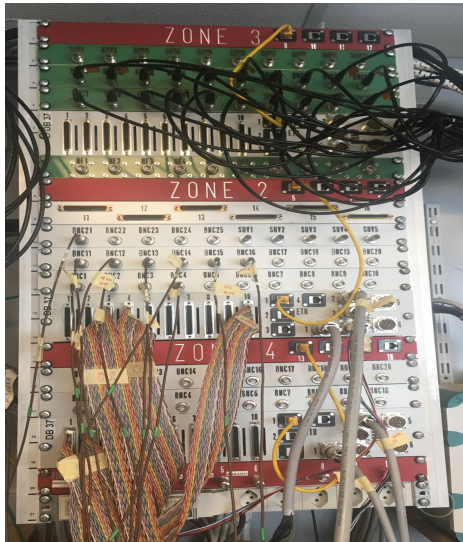
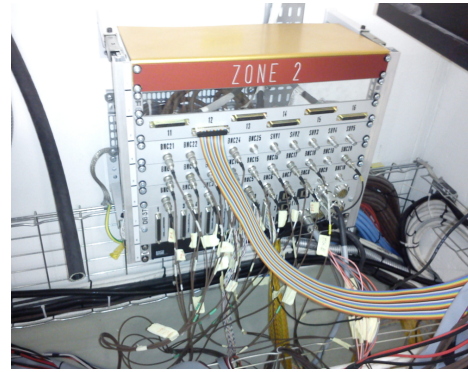


Figure 4.53. – LF_CPIX prototypes mounted on the experimental table in zone 2



(a) Control room Patch-panel



(b) Irradiation Zone 2 Patch-panel

Figure 4.54. – Patch-panels used for communication between Zone 2 inside the IRRAD area and the control room

The intensity of the extracted proton spills is monitored using a Secondary Emission Chamber (SEC) device. The profile of the proton beam with a spill-by-spill resolution can also be obtained by custom-made Beam Profile Monitor (BPM) devices (see in Figure 4.55b). The absolute measurement of the proton beam intensity (fluence) is obtained off-line via the activation-foils technique, that provides fluence measurements with an accuracy of $\pm 7\%$ [111]. This is achieved by evaluating the ^{24}Na and ^{22}Na activity of Aluminium (Al) foils produced via the nuclear reactions $^{27}\text{Al}(p,3p\text{n})^{24}\text{Na}$ and $^{27}\text{Al}(p,3p\text{n})^{22}\text{Na}$ respectively [112]. According to the time elapsed after irradiation and the irradiation time itself one of the two isotopes is chosen to be measured for the fluence calculation. The surface of the aluminium foils to be used, with a thickness of some hundred

micrometres, varies from 0.5 cm^2 to 2 cm^2 according to the size of the irradiated prototypes [111]. The Al foil mounted together with LF_CPIX prototypes is visible on Figure 4.53 [113].

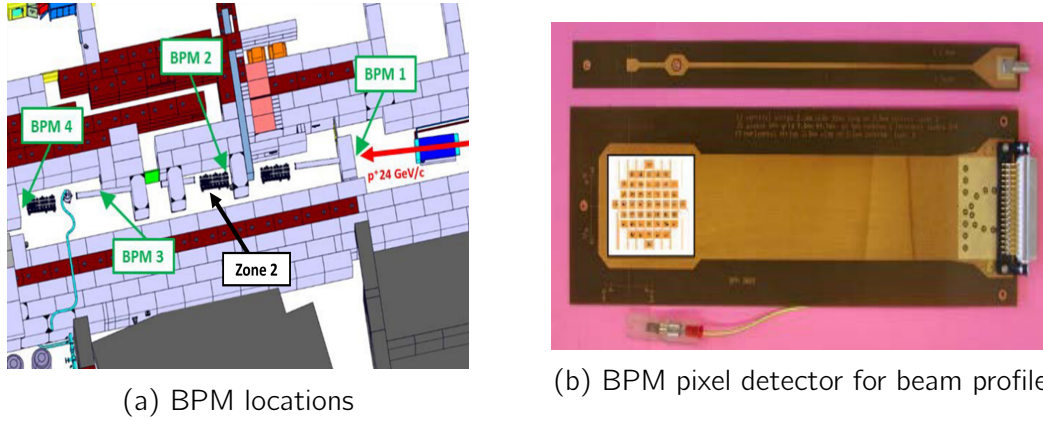


Figure 4.55. – Beam Profile Monitor system for the CERN PS facility

4.3.1.3. Setup development for characterization under radiation

Since the IRRAD zone is not accessible during the radiation period, the DUT board and data acquisition system must be separated by IRRAD zone and control room. In order to construct the full communication between the control room and IRRAD zone for LF_CPIX active setup, a new setup was developed. Instead of connecting the LF_CPIX DUT board to the GPAC board directly as done usually for in-lab tests, three types of 20 m long cables are routed between the two boards for signal transmission. The cables with BURNDY connectors were used for powering and polarization while the coaxial cables with BNC/LEMO connectors were used for analog signal input and output. In terms of digital signal, the Low-Voltage Differential Signals (LVDS) were used. LVDS is a technical standard that specifies electrical characteristics of a differential, serial communications protocol. Lower signal amplitudes reduce the power used by the circuits, and balanced signaling reduces noise coupling to allow higher speed signal transmission [114]. LVDS operates at low power and can run at very high speeds by using twisted-pair copper cables. Since the digital signals are single ended in the test setup that was initially developed, a LVDS to single ended translator board (in the control room) and a single ended to LVDS translator board (in the IRRAD zone) were produced to allow signal transmission. The transmitted signals and powers are listed in Table 4.6.

Figure 4.56 shows the connection of the set-up in the control room with the GPAC board connected to the multi IO board. The powering, polarization and analog signals are directly connected to the patch-panel. In order to make the digital signal connection between the GPAC board and the single ended to LVDS

Parameter	LF_CPIX Signals	GPAC PIN	Cable type
Power	Vdda VddaPRE Vddd	PWR0 PWR1 PWR2	Cable with BURNDAY connector
Polarization	Injection BL, GndPre TH VcascP VcascN Vcasc2	INJ PWR3 VSRC1 VSRC0 VSRC3 VSRC2	Coaxial cables with LEMO connector
Input	LdDAC CLConf SR_EN Sin LdPIX Reset	Dout0 Dout1 Dout2 Dout3 Dout4 Dout5	Twisted-pair Copper
Output	Sout Monitor Amplifier	DIN0 DIN1	Twisted-pair Copper Coaxial cables with LEMO connector
GND	gnda	GND	Cable with BURNDAY connector

Table 4.6. – LF_CPIX signal/power list for radiation test.

translator board, a small interface board was also designed. The single ended to LVDS translator board was connected to the control room patch panel using the twisted-pair cable. Figure 4.57 shows the connection sequence in the IRRAD zone 2. The powering, polarization and analog signals were sent to the LF_CPIX DUT board from the patch panel in IRRAD zone. Regarding the digital signals, the translator board was used to transfer the LVDS signals to single ended signals and then connected to the DUT board.

For the passive setup, only the HV and power signals were connected by cables with BURNDY connectors between the IRRAD zone and control room.

In order to monitor the behavior of these three prototypes during irradiation, the prototypes were tested at regular intervals, corresponding to increasing TID (called dose points below). Figure 4.58 lists all the recorded dose points.

4.3.2. Leakage current and breakdown voltage measurements

The leakage current measured on the guard-ring was probed during the irradiation at room temperature ($\sim 20^\circ\text{C}$). The current of LF_CPIX1 (750 μm -V1)

Setup in Control Room

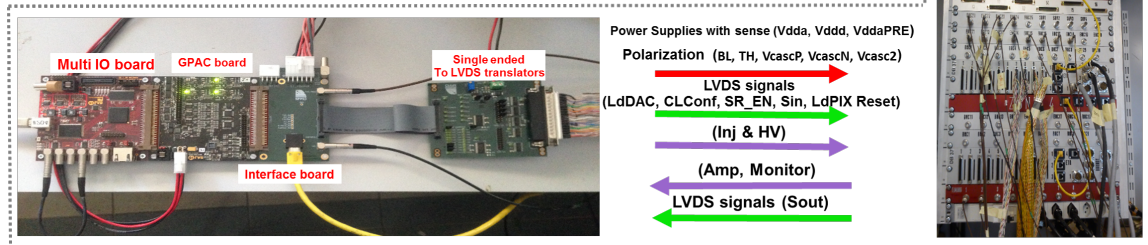


Figure 4.56. – LF_CPIX set-up in control room

Setup in Irrad Zone2

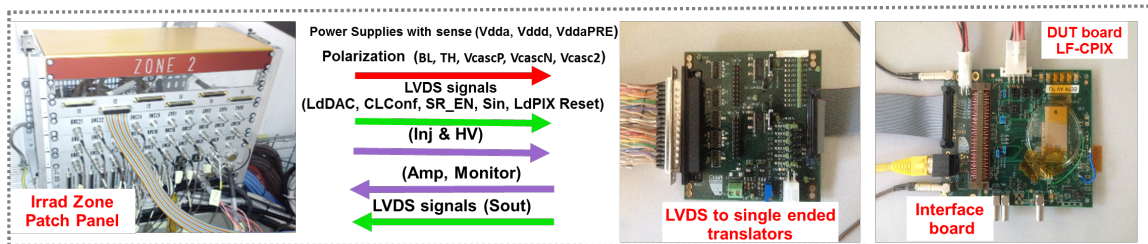


Figure 4.57. – LF_CPIX set-up in IRRAD zone 2



Figure 4.58. – LF_CPIX time line of radiation dose

before and after irradiation is shown in Figure 4.59, the blue line is the I-V curve before radiation at $\sim 20^\circ\text{C}$, the current value is around $0.015\ \mu\text{A}$ at $-100\ \text{V}$, and then increases to $450\ \mu\text{A}$ at $\sim 20^\circ\text{C}$ after 150 MRad TID (red line) and NIEL of $3.42 \times 10^{15}\ n_{eq} \cdot \text{cm}^{-2}$. The current at low temperature (-17°C , green line) after 150 MRad TID and NIEL of $3.42 \times 10^{15}\ n_{eq} \cdot \text{cm}^{-2}$ was only $13.4\ \mu\text{A}$ with total number of pixels 5866. Therefore per pixel leakage current is less than $2.4\ \text{nA}$, well below the HL-LHC design requirement ($10\ \text{nA/pixel}$) [45].

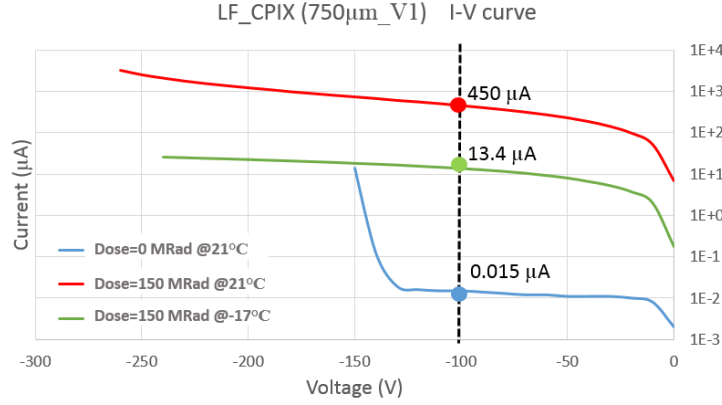


Figure 4.59. – LF_CPIX1 (750 μm -V1) I-V before and after irradiation at different temperatures.

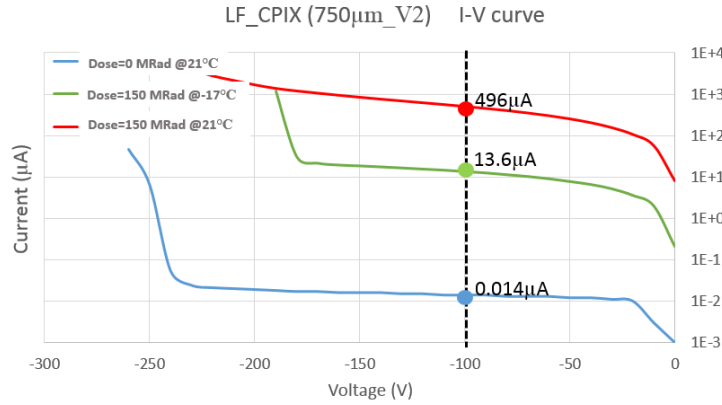


Figure 4.60. – LF_CPIX2 (750 μm -V2) I-V before and after irradiation at different temperatures.

The I-V curves of LF_CPIX2 (750 μm -V2) and LF_CPIX3 (250 μm -V2) are shown in Figures 4.60 and 4.61, and similar leakage current degradation profile can be seen after irradiation. The leakage current is less than $500\ \mu\text{A}$ at room temperature at $-100\ \text{V}$, and around $13\ \mu\text{A}$ at $T=-17^\circ\text{C}$ for both chips. The per-pixel leakage current is less than $2.5\ \text{nA}$ at $T=-17^\circ\text{C}$, well below the HL-LHC design requirement ($10\ \text{nA/pixel}$) for both prototypes.

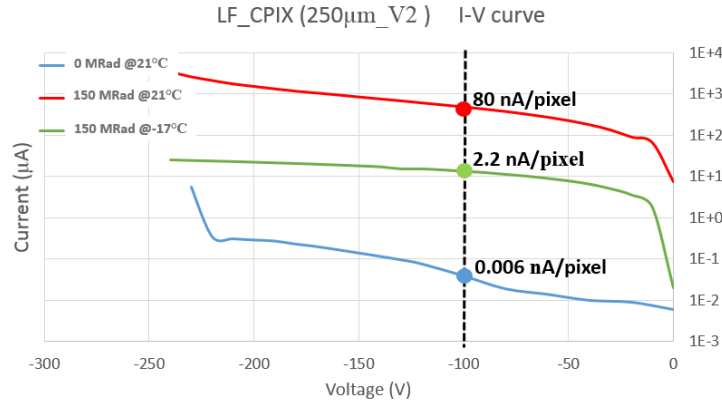


Figure 4.61. – LF_CPIX3 (250 $\mu\text{m-V2}$) I-V before and after irradiation at different temperatures.

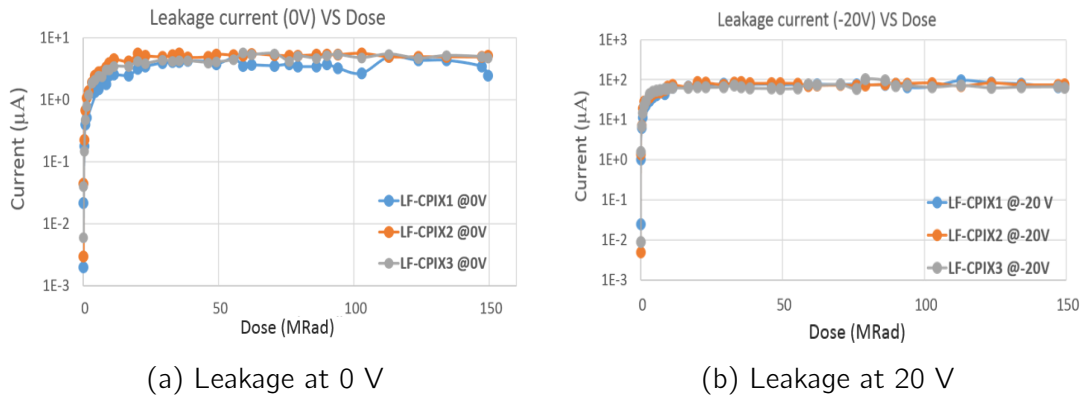


Figure 4.62. – Leakage current as a function of dose at $\sim 20^\circ\text{C}$ for three prototypes

All three chips showed similar leakage current degradation profile as a function of the integrated dose. The I-V is plotted at 0 V (see Figure 4.62a) and -20 V (see Figure 4.62b). In both cases, the current value increased rapidly at the very beginning (less 2 MRad) and stayed at about the same magnitude afterwards till the end for all three chips.

4.3.3. Pixel matrix measurements

4.3.3.1. On-line measurements during the radiation

During the irradiation, the injection scan for the two active setups (LF_CPIX2 and LF_CPIX3), a time consuming procedure, was performed at different dose points (see in Figure 4.58).

For LF_CPIX2 (750 $\mu\text{m-V2}$), the injection scans for NMOS and PMOS were done, the CMOS flavor was lost communication during the radiation period due to the bad cable connection. Figures 4.63 and 4.64 show the mean threshold

and noise evolution with dose. The threshold of the PMOS pixels decreases with increasing dose level, while the mean threshold of NMOS pixels is almost stable. The threshold dispersion (see Figure 4.65) of PMOS flavor increased a lot at the beginning of the radiation, We have therefore decided to perform a new TDAC tuning at 38 MRad. The dispersion of PMOS flavor was recovered to the initial values after TDAC tuning. Concerning the NMOS flavor, the threshold dispersion is not affected much by the dose increasing, as shown in Figure 4.65. The noise of PMOS flavor also increased (see Figure 4.64) a lot at the beginning of the radiation, and became stable (~ 400 - 500 e-) afterwards. The noise of NMOS flavor increased linearly from 110 e- at 0 MRad to 300 e- at 150 MRad, as shown in Figure 4.64.

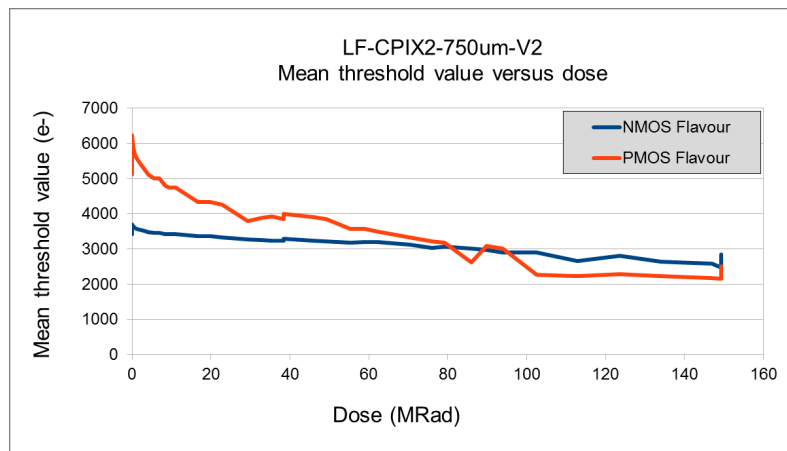


Figure 4.63. – LF_CPIX2 (750 μ m-V2) mean threshold as a function of dose at $\sim 20^\circ\text{C}$

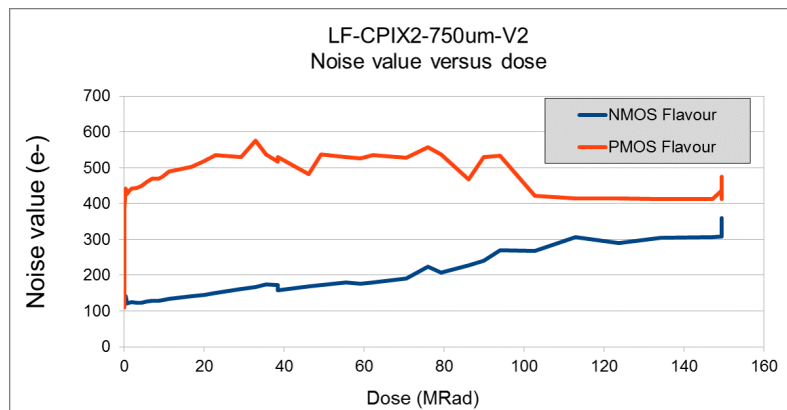


Figure 4.64. – LF_CPIX2 (750 μ m-V2) noise as a function of dose at $\sim 20^\circ\text{C}$

The same testing protocol was also implemented for LF_CPIX3 (250 μ m-V2) prototype. This chip started to misbehave at 60 MRad. This issue was probably

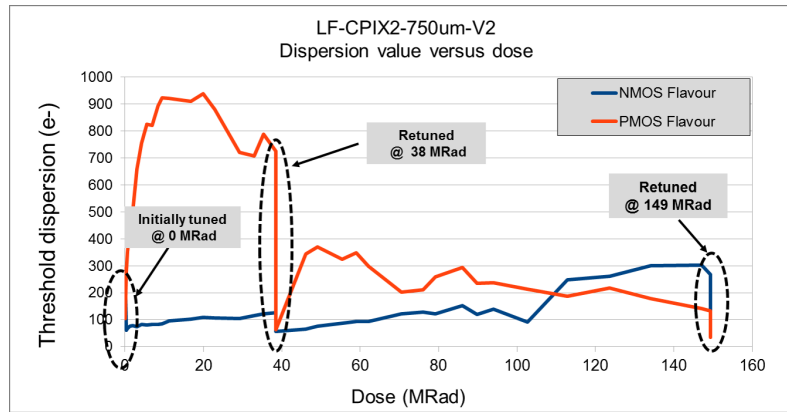


Figure 4.65. – LF_CPIX2 (750 μm -V2) threshold dispersion as a function of dose at $\sim 20^\circ\text{C}$

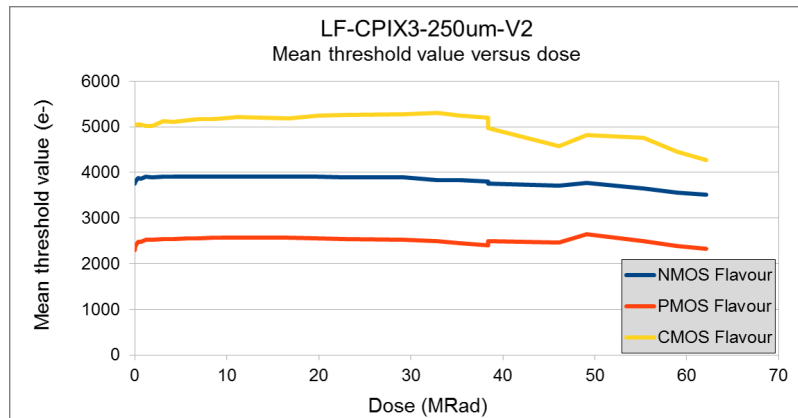


Figure 4.66. – LF_CPIX3 (250 μm -V2) mean threshold as a function of dose at $\sim 20^\circ\text{C}$

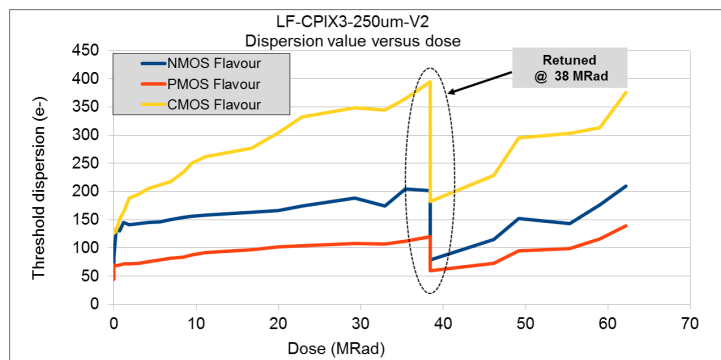


Figure 4.67. – LF_CPIX3 (250 μm -V2) threshold dispersion as a function of dose at $\sim 20^\circ\text{C}$

due to some components on the DUT or interface board, which were too sensitive

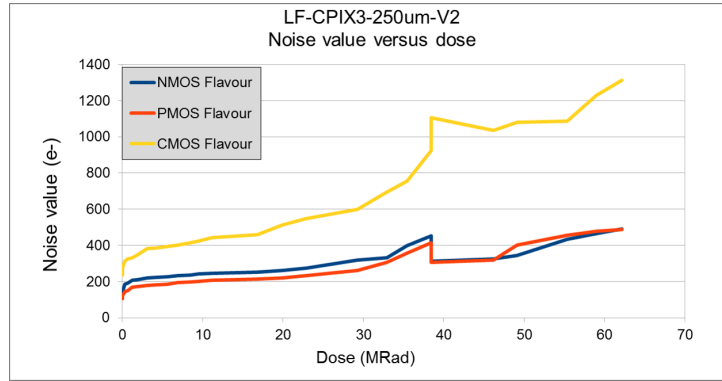


Figure 4.68. – LF_CPIX3 (250 μm -V2) noise as a function of dose at $\sim 20^\circ\text{C}$

to cope with the high dose recorded in the irradiation zone. Figures 4.66 and 4.67 show the mean threshold and dispersion behavior as a function of dose until a dose a bit in excess of 60 MRads was recorded. The threshold dispersion and noise of CMOS is more sensitive to the total recorded dose compared to PMOS and NMOS flavors (see Figure 4.67 and Figure 4.68).

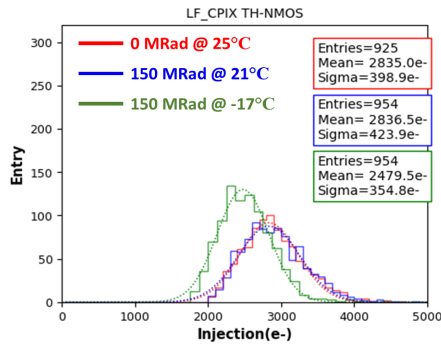
The LF_CPIX2 prototype was functional during the whole radiation campaign, and LF_CPIX3 prototype worked again after uninstallation. These prototypes were tested extensively after uninstallation, and more test results are in next section.

4.3.3.2. Off-line measurements after radiation

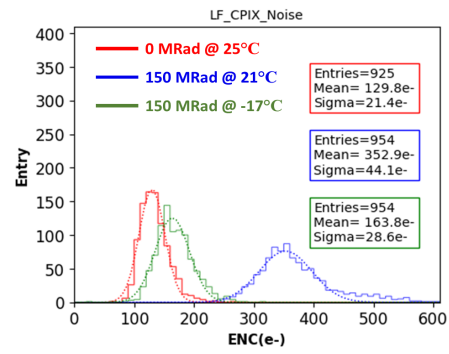
After reaching 150 MRad TID, the LF_CPIX prototypes were dismantled one week later from the table in the radiation zone, and then connected to the GPAC board directly as the setup shown in Figure 4.16.

Injection scans were performed for LF_CPIX2, and all three flavors were still fully functional. Figure 4.69 shows the threshold and noise distributions before irradiation and at different temperatures after irradiation. At room temperature, the difference between pre-irradiation and 150 MRad TID measurements is found to be rather negligible. In terms of noise, the value increased by approximately a factor of 3, from 129 e- before irradiation to 352 e- after 150 MRad. The noise degradation can be kept under control by applying low temperature, since the thermal noise of pixel is proportional to the temperature (see formula 4.1). As expected, the noise can be decreased to 163 e- at -17°C (see Figure 4.69b).

The PMOS and CMOS flavors give similar results as the NMOS flavor as can be seen in Figures 4.70 and 4.71, respectively. The mean threshold value, dispersion and noise for all three flavors are summarized in Table 4.7. Figure 4.72 shows the noise performance before and after radiation at different temperatures. In this plot, the noise degradation of the NMOS flavor after 150 MRad

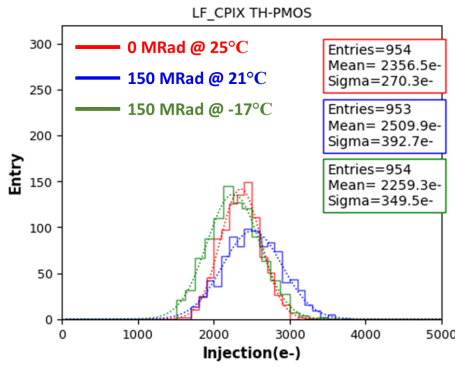


(a) Threshold distribution

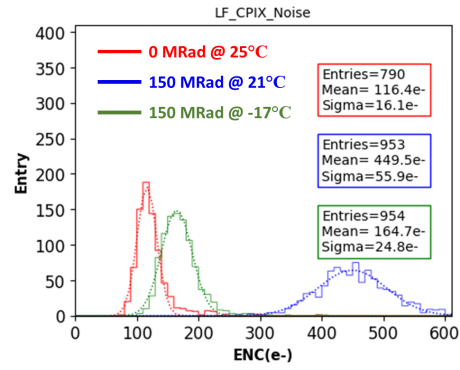


(b) Noise distribution

Figure 4.69. – Threshold and noise distribution of LF_CPIX2 NMOS flavor after radiation

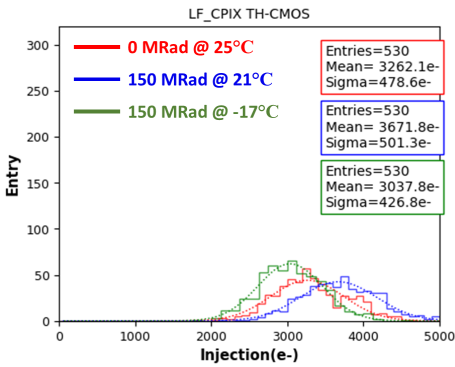


(a) Threshold distribution

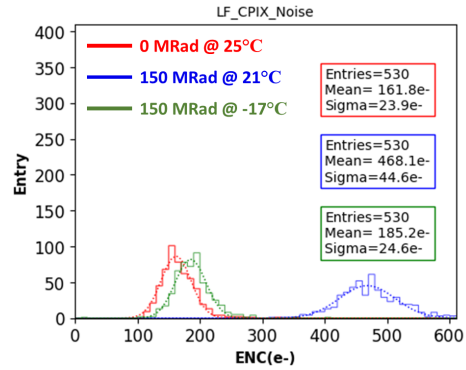


(b) Noise distribution

Figure 4.70. – Threshold and noise distribution of LF_CPIX2 PMOS flavor after radiation



(a) Threshold distribution



(b) Noise distribution

Figure 4.71. – Threshold and noise distribution of LF_CPIX2 CMOS flavor after radiation

LF_CPIX2	0 MRad (~20 °C)	150 MRads (~20 °C)	150 MRads (-17 °C)
NMOS_mean_th	2835 e-	2836 e-	2479 e-
NMOS_th_dispersion	398 e-	423 e-	354 e-
NMOS_noise	129 e-	352 e-	163 e-
PMOS_mean_th	2356 e-	2509 e-	2259 e-
PMOS_th_dispersion	270 e-	392 e-	349 e-
PMOS_noise	116 e-	449 e-	164 e-
CMOS_mean_th	3262 e-	3671 e-	3037 e-
CMOS_th_dispersion	478 e-	501 e-	426 e-
CMOS_noise	161 e-	468 e-	185 e-

Table 4.7. – The summary of LF_CPIX2 testing results

is not as large as for the PMOS and the CMOS at room temperature (around a 100 e- reduction). However, the noise recorded for all flavors is about 185 e- if low temperature is applied after proton beam irradiation up to 150 MRad. The noise is at a comparable level as the pre-radiation noise level room temperature measurement, which is very encouraging.

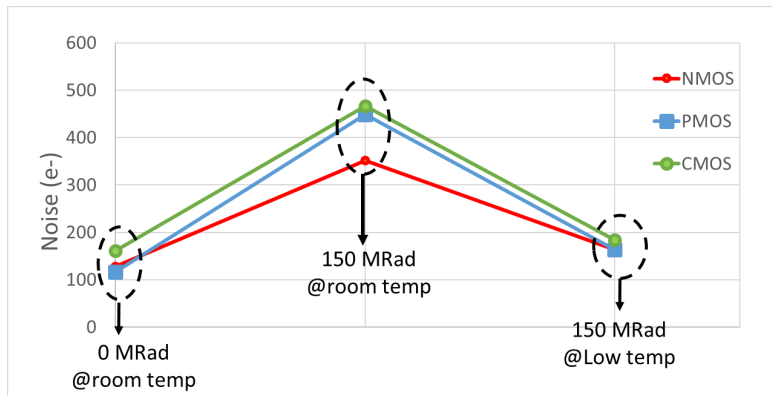


Figure 4.72. – Noise before and after radiation of LF_CPIX2

In order to investigate the tuning ability after 150 MRad proton beam irradiation, threshold tuning measurements were done as well for all three flavors. After 150 MRad, the threshold mean value for all the flavors is between 2 ke- to 3 ke- with a dispersion of around 50 e-, as shown in Figures 4.73a, 4.73b and 4.73c, as good as before irradiation. The LF_CPIX2 prototype shows encouraging irradiation results, all the blocks are still fully functional after 150 MRad radiation.

The LF_CPIX1 chip was also tested directly connected to lab measurement setup. The threshold and noise distributions for the NMOS flavor are plotted in

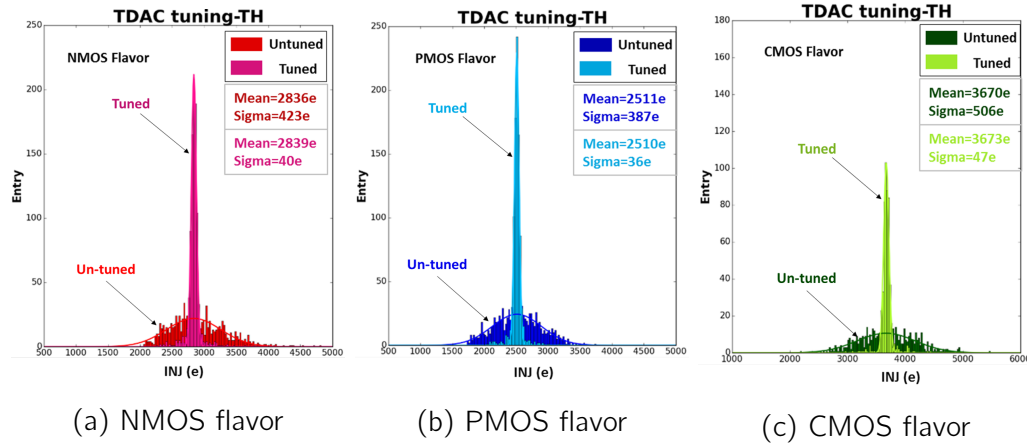


Figure 4.73. – The comparison between un-tuned and tuned pixels of LF_CPIX2 after radiation

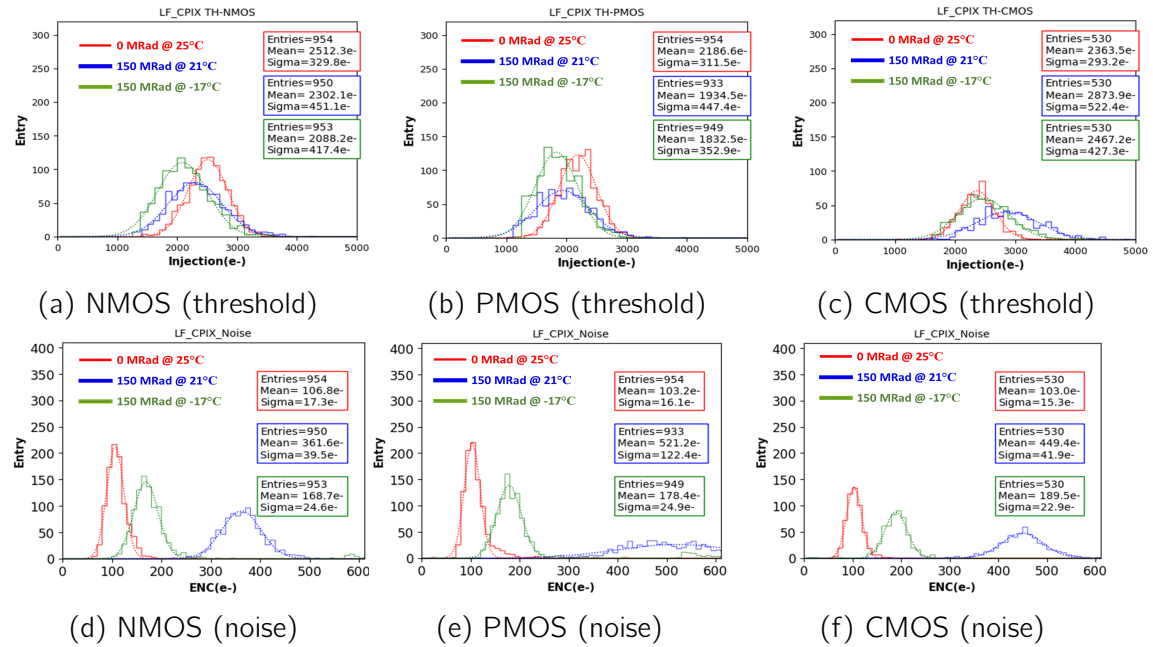


Figure 4.74. – Threshold and noise distribution of LF_CPIX1 after radiation

Figures 4.74a and 4.74d, showing that the proton radiation dose not affect too much the mean threshold (approximately 8% difference). The threshold dispersion increased a little bit (around 100 e-) after irradiation, and the noise value increase (3 times higher) at room temperature after irradiation can be in large part recovered by lowering the temperature. The Figure 4.74b, Figure 4.74e and Figure 4.74c, Figure 4.74f give the scan results of PMOS and CMOS flavors, with very similar trends as for the NMOS case.

The threshold mean value, dispersion and noise for all three flavors are sum-

marized in Table 4.8. An average noise lower than 190 e- could be achieved at low temperature (-17 °C) after 150 MRad total dose for all flavors.

LF_CPIX1	0 MRad (~20 °C)	150 MRads (~20 °C)	150 MRads (-17 °C)
NMOS_mean_th	2512 e-	2302 e-	2088 e-
NMOS_th_dispersion	329 e-	451 e-	417 e-
NMOS_noise	106 e-	361 e-	168 e-
PMOS_mean_th	2186 e-	1934 e-	1832 e-
PMOS_th_dispersion	311 e-	447 e-	352 e-
PMOS_noise	103 e-	521 e-	178 e-
CMOS_mean_th	2363 e-	2873 e-	2467 e-
CMOS_th_dispersion	293 e-	522 e-	427 e-
CMOS_noise	103 e-	449 e-	189 e-

Table 4.8. – The summary of LF_CPIX1 testing results

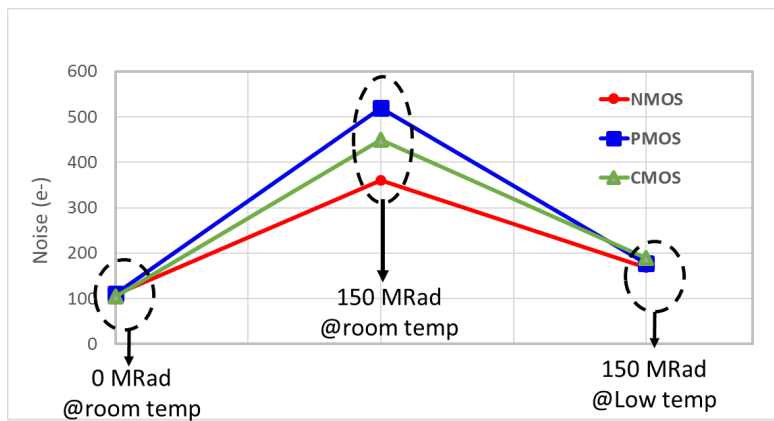


Figure 4.75. – Noise before and after radiation of LF_CPIX1

The results obtained for LF_CPIX1 are in agreement with the ones of LF_CPIX2. Same observation can be made for LF_CPIX3, which results summary is given in Table 4.9.

Conclusion

A large scale prototype LF_CPIX based on a previous design called CCPD_LF using LFoundry 150 nm technology was developed to test the sensor and analog pixel front-end part for the harsh radiation environment of the ATLAS ITk or other high radiation dose environments. Two versions of the LF_CPIX have been characterized before and after irradiation.

LF_CPIX3	0 MRad (~20 °C)	150 MRads (-17 °C)
NMOS_mean_th	3432 e-	2374 e-
NMOS_th_dispersion	471 e-	457 e-
NMOS_noise	144 e-	218 e-
PMOS_mean_th	2638 e-	2006 e-
PMOS_th_dispersion	233 e-	408 e-
PMOS_noise	134 e-	198 e-
CMOS_mean_th	3576 e-	2771 e-
CMOS_th_dispersion	449 e-	524 e-
CMOS_noise	149 e-	231 e-

Table 4.9. – The summary of LF_CPIX3 testing results (not tested at 20 °C after radiation due to the time limitation)

The laboratory measurements before irradiation are in agreement with the simulation in terms of analog outputs of the pre-amplifier. As expected from the design changes that were implemented, reduced threshold dispersion (un-tuned) and noise are observed with respect to CCPD_LF. A threshold dispersion below 80 e- after tuning can be recorded. Improved breakdown voltage of the V2 prototype is achieved compared to V1 which has the same guard-ring strategy as CCPD_LF.

For all flavors implemented, both the pre-amplifier and the discriminator are responsive up to TID of 150 MRad and NIEL of $3.42 \times 10^{15} \text{ } n_{eq} \cdot \text{cm}^{-2}$ under 24 GeV proton irradiation. A limited leakage current increase meet the HL-LHC design requirement at T=-17 °C. Small degradation of the threshold dispersion (un-tuned) and little shifting of the average threshold were observed, and there is no degradation in terms of threshold dispersion after tuning. However, the noise performance degrades a lot after irradiation at room temperature, but this degradation can be mitigated by cooling. The NMOS pixel flavor shows the best noise performance and around 100 e- less degradation than the PMOS and CMOS flavors after radiation at room temperature. The CMOS-input pre-amplifier didn't show low noise as expected compared to the other two flavors, more investigation and simulation need to be done. The comparative characterizations of the pre-amplifiers implemented in this chip allow the choice of the best pre-amplifier architecture for future developments.

A monolithic demonstrator using the same sensor and analog part design as LF_CPIX but with full readout circuits was designed and fabricated in parallel to the LF_CPIX, and will be presented in Chapter 5.

5. LF—MONOPIX1: First monolithic CMOS sensor development and characterization

CCPD_LF and LF_CPIX were used to assess sensor and analog front end performance, for which promising results before and after radiation have been presented in Chapter 4. The LF-MONOPIX1 chip is the first fully monolithic prototype implemented in LFoundry 150 nm CMOS technology for ATLAS ITK upgrade. It inherits the analog and sensor parts of LF_CPIX V2 prototype, and integrates them with a fast readout logic. These three demonstrators development time line is shown in Figure 5.1.

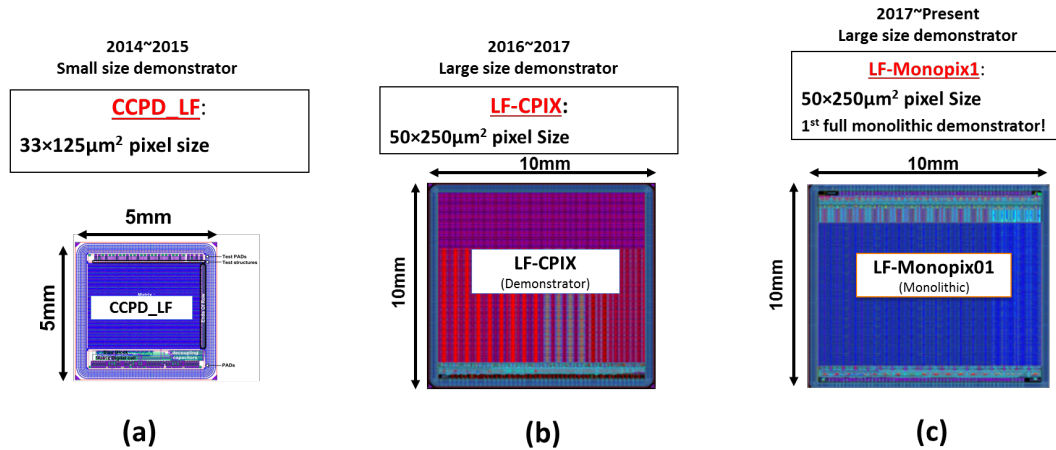


Figure 5.1. – LF technology development line (a) LF_CCPD (b) LF_CPIX (c) LF-MONOPIX1

5.1. LF_MONOPIX1 prototype introduction

The cross-section diagram of the LF-MONOPIX1 pixel cell developed in the LFoundry 150 nm CMOS technology is shown in Figure 5.2 [80]. The sensor uses a high resistivity P-type substrate (approximately $2 \text{ k}\Omega \cdot \text{cm}$), which enables the sensor to have a large depletion area. The charge collection node is formed by a very deep N-well and the P-type substrate. The in-pixel electronics are embedded in the deep N-well, and deep P-type layer allows isolating the transistor N-wells from the very deep N-well, so that full CMOS capability is achieved within the pixel cell. Wafer thinning and backside implantation are also possible after the

CMOS processing, and these process steps allow the obtention of a strong electric field and uniform charge collection inside the sensor.

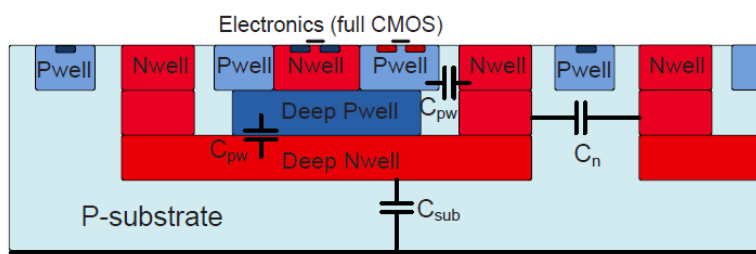


Figure 5.2. – The cross-section diagram of the LF-MONOPIX1 pixel cell

The chip contains a matrix of 129×36 pixels (129 rows, 36 columns) with size of $10 \text{ mm} \times 10 \text{ mm}$ and the pixel size is $250 \text{ } \mu\text{m} \times 50 \text{ } \mu\text{m}$. The pixel type arrangement of LF-MONOPIX1 is given in Figure 5.3. In order to compare the performance of different designs, the pixel matrix consists of nine different pixel flavors (with 4 columns per flavor). These different pixel types differ by the designs of their CSA (2 types: NMOS transistor input and CMOS complementary input), the discriminator architecture (2 types: V1 and V2) the placement of the pixel readout circuitry (2 types: in-pixel and in periphery) and also by the usage of current steering logic techniques used for noise mitigation as well as the usage of a source follower SRAM readout.

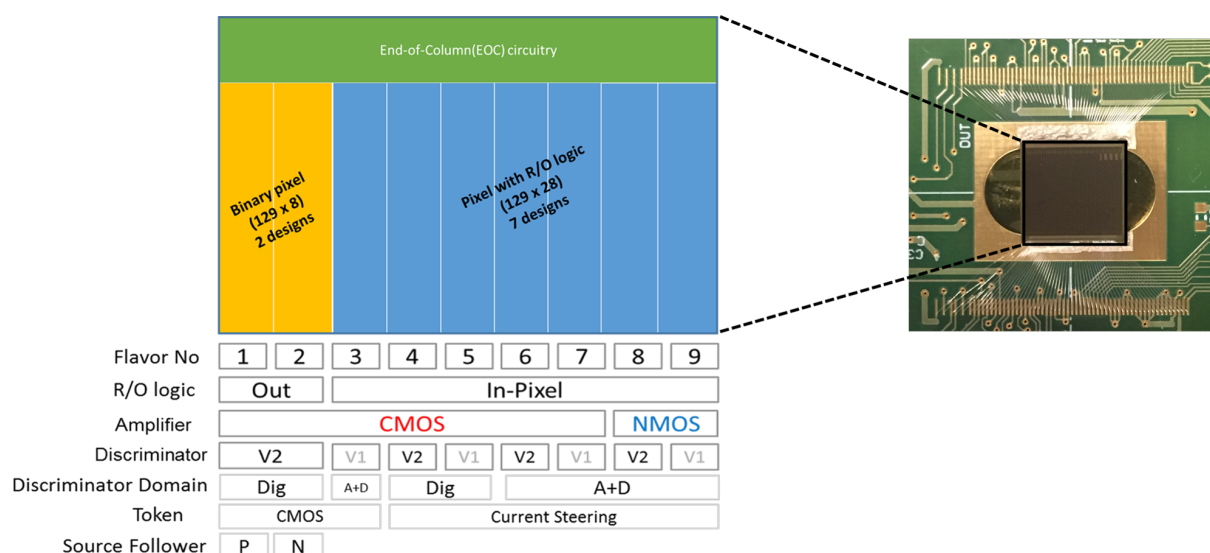


Figure 5.3. – The various pixel types in LF-MONOPIX1

5.1.1. Sensor and analog part

The block diagram of the in-pixel logic is shown in Figure 5.4 [115]. On the left side of the figure, we can find a similar diode and first stage analog front end circuitry design as LF_CPIX and CCPD_LF in the blue circle. The input signal is first amplified by a Charge Sensitive Amplifier (CSA), which converts the current pulse to a voltage signal via an integral feedback circuit. The output of the amplifier is brought to a discriminator via a source follower and compared with an externally controlled threshold. A four bit Threshold tuning Digital-to-Analog Converter (TDAC) is designed in order to provide fine adjustment of the threshold in each pixel. The discriminator output triggers the readout logic, whose working principle will be discussed in session 5.1.2.

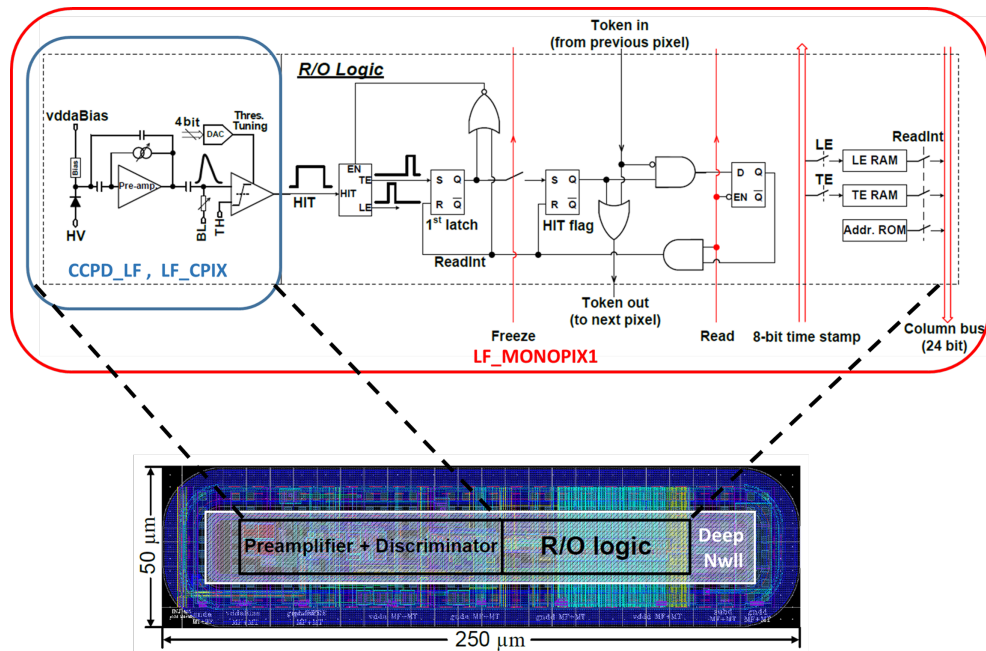
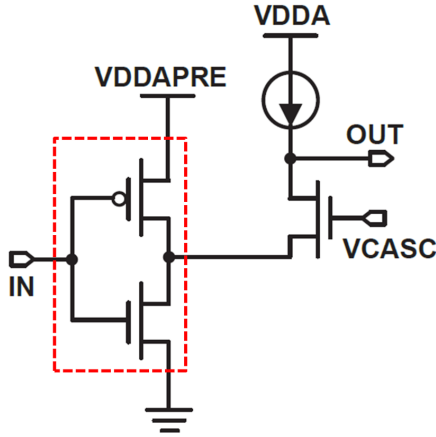
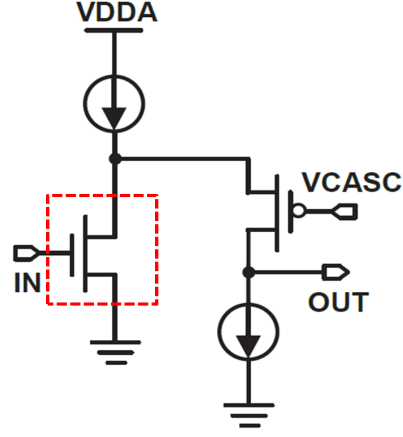


Figure 5.4. – The schematic of LF-MONOPIX1 in-pixel electronics

In terms of the pre-amplifier design, two types of designs are implemented in LF-MONOPIX1 and their schematics are shown in Figure 5.5. Both of them are using the single-ended folded cascode topology, and their transistor parameters were optimized to cope with the large detector capacitance (400 fF) anticipated in LF-MONOPIX1. The difference is that one uses NMOS input transistor, the other one uses two complementary (CMOS) input transistors to increase the transconductance for a given bias current, and thus is expected to have better speed and noise performance, the bias of the CMOS input pre-amplifier relies on a separate analog power (VddaPre in Figure 5.5a) provided by a regulator in the periphery. The simulation of these 2 types of pre-amplifier is shown in Figure 5.6, both of them have good linearity of output from 500 e⁻ to 16 ke⁻. However,

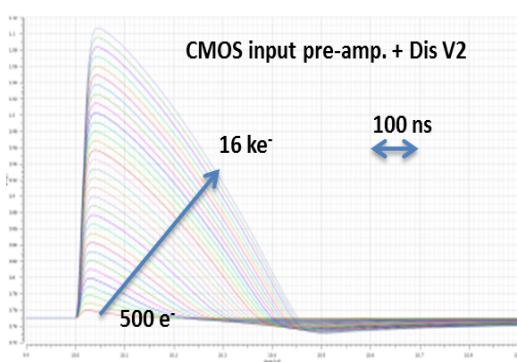


(a) CMOS input pre-amp.

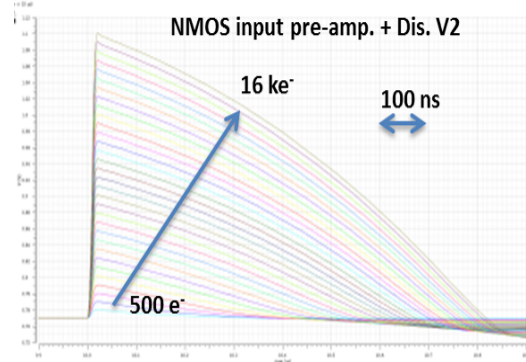


(b) NMOS input pre-amp.

Figure 5.5. – LF-MONOPIX1 pre-amplifier design (a)CMOS input transistor (b)NMOS input transistor



(a) CMOS input pre-amp.



(b) NMOS input pre-amp.

Figure 5.6. – LF-MONOPIX1 pre-amplifier simulation results

the NMOS input pre-amplifier shows better leading edge performance, which is only 20 ns at 4000 e- injection, while the CMOS input transistor CSA gives 25 ns in the same condition.

Two types of discriminator designs are also implemented in LF-MONOPIX1, and their schematics are shown in Figure 5.7. The discriminator V1 has a typical two-stage open loop structure, which is the same design as was used in LF_CPIX. The discriminator V2 is a self-biased differential amplifier, followed by a CMOS inverter as the output stage. The latter exploits the complementary character of CMOS input devices for high gain and fast operation. Therefore, the pixel with discriminator V2 is expected to have less time-walk effect [116], time-walk is one of the limiting factors for the time resolution of the pixel chip, If two simultaneous hits have a large difference in the pulse height they will be assigned to two different clock cycles and not to the same trigger signal, as shown in Fi-

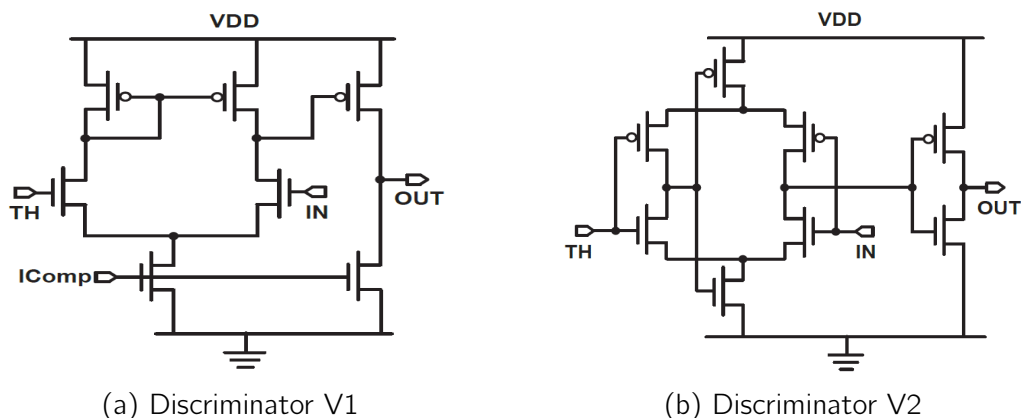


Figure 5.7. – LF-MONPIX1 discriminators design: (a) Discriminator V1 (b) Discriminator V2

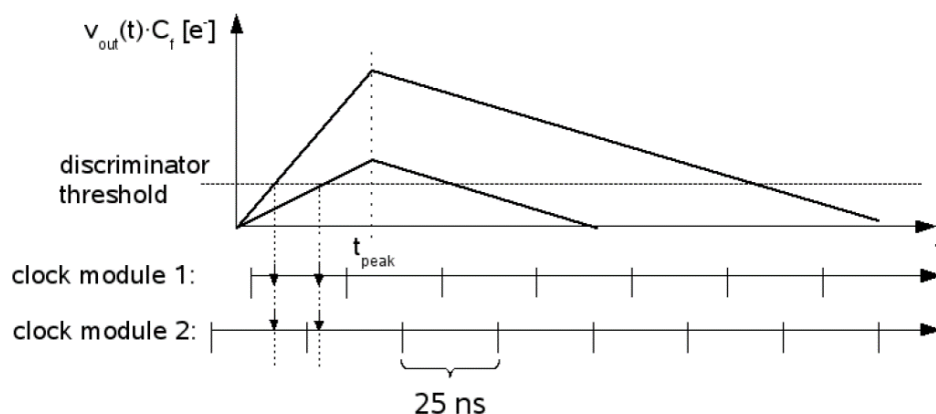


Figure 5.8. – Principle of the time-walk effect, the assignment of hits to readout windows of two modules with different clock phases is shown at the bottom.

Figure 5.8. Figure 5.9 shows the simulated waveforms of the discriminator output ("HIT") and the Leading Edge (LE) pulse, with the input charge ranging from 1500 e⁻ to 80 ke⁻. The simulated pixel uses the NMOS pre-amplifier with the detector capacitance of 400 fF, and followed by the discriminator V1 (Figure 5.9a) and V2 (Figure 5.9b). The threshold of the discriminator is adjusted to be 1500 e⁻ in both cases, it means that only signal charge above this value can generate the discriminator output and LE pulse. The LE pulse indicates the arrival time of the "HIT". The time walk of V1 which we define as the time difference between the two LE pulses that are generated from the small signal (1500 e⁻) and a very large signal (80 ke⁻) respectively, is 34 ns in the worst case. Simulation was also performed with pixel using discriminator V2, and with the same definition the time walk is only 23 ns.

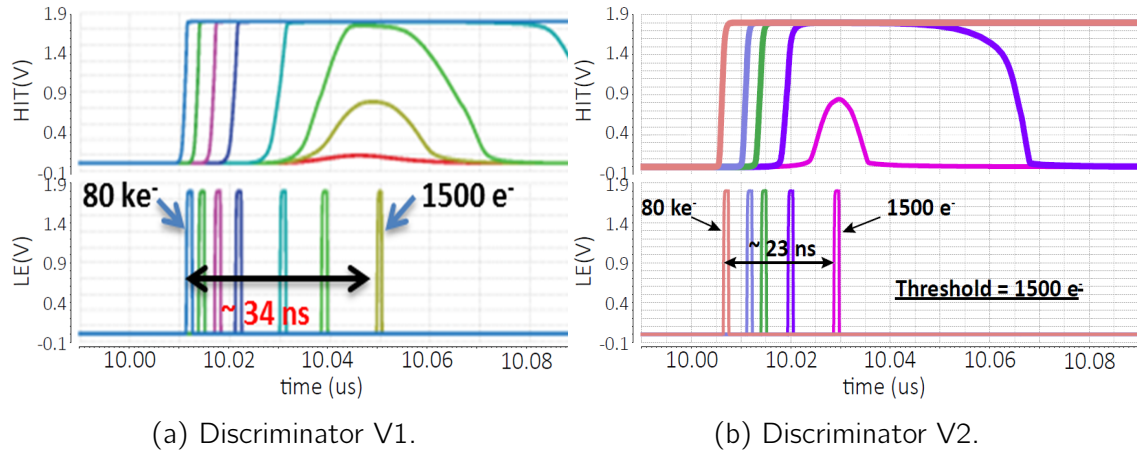


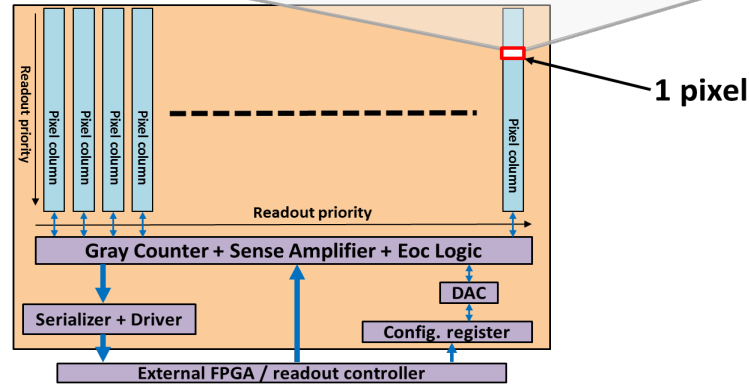
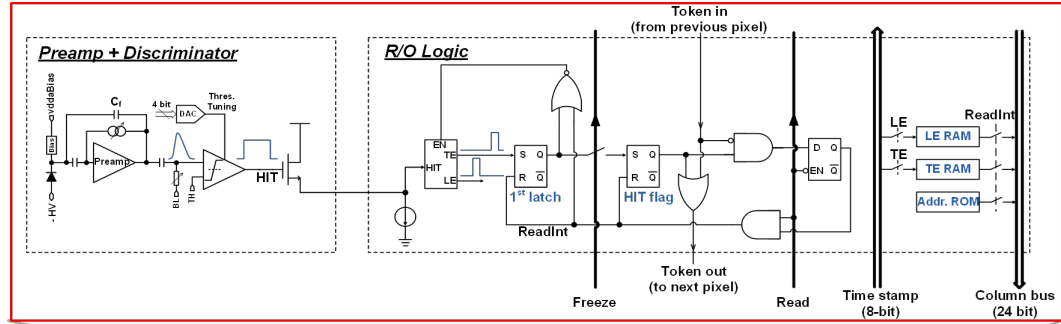
Figure 5.9. – Time walk simulation with discriminator V1 and V2

Bias name	Comment	Typical value
BLRes	R value of the filter	32
VAmp	Current of the pre-amplifier (for NMOS input CSA)	32
VPFB	Feed-back resistance value	32
VFoll	Current of the source follower (in-pixel one)	12
VLoad	Bias of the pre-amplifier load	11
IComp	Current of the comparator	32
Vbias_CS	Current bias of current steering gate for in-pixel readout	32
IBOTA	Current for the OTA of the Regulator (for CMOS CSA only)	32
ILVDS	Bias current for LVDS driver	32
Vsf	Bias current for source followers used to readout RAM and ROM	32
LSBdacL	Current polarization for the amplitude of the pixel output	32
Vsf_dis1	Bias current for source followers used for HIT propagation from pixel to readout electronics, ("SF readout"), for pixels 0-43	10
Vsf_dis2	Bias current for source followers used for HIT propagation from pixel to readout electronics, ("SF readout"), for pixels 44-86	20
Vsf_dis3	Bias current for source followers used for HIT propagation from pixel to readout electronics, ("SF readout"), for pixels 87-128	30

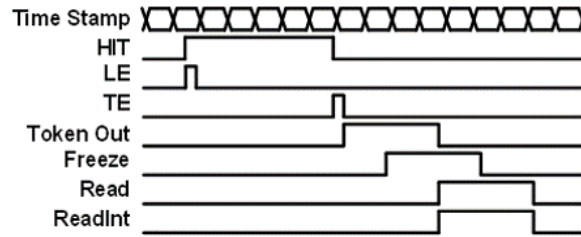
Table 5.1. – List of global DACS in bias block.

In the LF-MONOPPIX1 pixel, there are several global DACs, which are summarized in Table 5.1 and can be tuned to adjust the chip configuration. In this table, suggested values for a typical operation of this IC is also given in the last column.

5.1.2. Read out logic



(a) In-pixel design.



(b) The timing diagram for the readout logic.

Figure 5.10. – A functional view of the pixel readout logic.

The LF-MONOPIX1 is a fast readout monolithic CMOS sensor, and it uses the column drain readout logic as in FEI3 [26], whose working principle can be described with the help of the timing diagram shown in Figure 5.10b. The discriminator output is triggered when the Leading Edge (LE) of voltage signal pulse is over the threshold, and the output of discriminator would stay high until the Trailing Edge (TE) is generated when the voltage pulse falls later below the threshold. At the Leading Edge (LE) and Trailing Edge (TE) of the discriminator

output, two short signals are generated and can be recorded by the two in-pixel RAM cells, therefore the HIT arriving time and the Time Over Threshold (TOT) can be obtained. The TE pulse also sets the HIT flag register, which inserts a Token that can propagate to the column end through a chain of OR logic. The output Token is received by a readout controller, which sends back the Freeze signal to the column. The Freeze signal makes sure that new hits will not disturb the readout process, while these later hits can still be recorded by a latch. The readout controller then generates the Read signal, which is selected by a priority network, so that the topmost pixel has the highest readout priority and has its internal ReadInt signal enabled. The ReadInt signal allows the hit information (8-bit LE time stamp, 8-bit TE time stamp and 8-bit pixel address) from the in-pixel memories to be driven to the column data bus for readout. The pixel column interfaces with the End-of-Column (EoC) circuitry, which includes the gray counter running at 40 MHz to generate the Bunch Crossing Identifier (BCID) time stamp, the sense amplifiers to receive the column data, and the EoC logic to perform the column-level readout priority scan and transmits data to the serial link. The readout controller, which controls the readout sequence, is implemented in an FPGA off the chip [80] [117]. Since the ReadInt signal also clears the hit flag register, the priority network ripples down to find the next hit pixel, if any, once the Read signal goes back to zero. This readout cycle continues by sending repetitively the Read pulse until this frozen column is "drained out".

5.2. Characterization before irradiation

5.2.1. Leakage current and breakdown voltage measurements

Figure 5.11 shows the I-V curve of LF-MONOPIX1 at room temperature. The breakdown voltage is around -280 V, which is even lower than LF_CPIX, so a larger depletion area could be expected. The leakage current of the whole chip before breakdown voltage is several nA.

5.2.2. The pixel analog part characterization

The pre-amplifier and discriminator outputs were first tested. Both of them have response with external test injection for all the flavors. As an example, the analog outputs of the CMOS amplifier pixel flavors with external readout logic pixel are shown in Figure 5.12. The pink pulse is the pre-amplifier output to a 700 mV external injection and the blue signal is the output of the discriminator. Figures 5.13 and 5.14 give example snapshots of other flavors with readout logic inside the pixel.

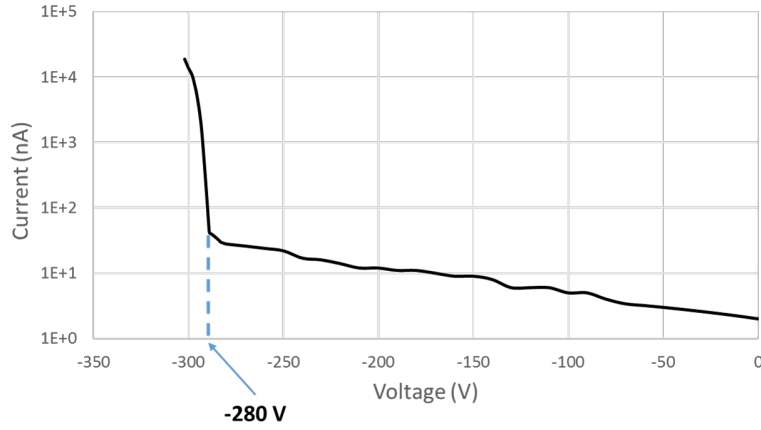
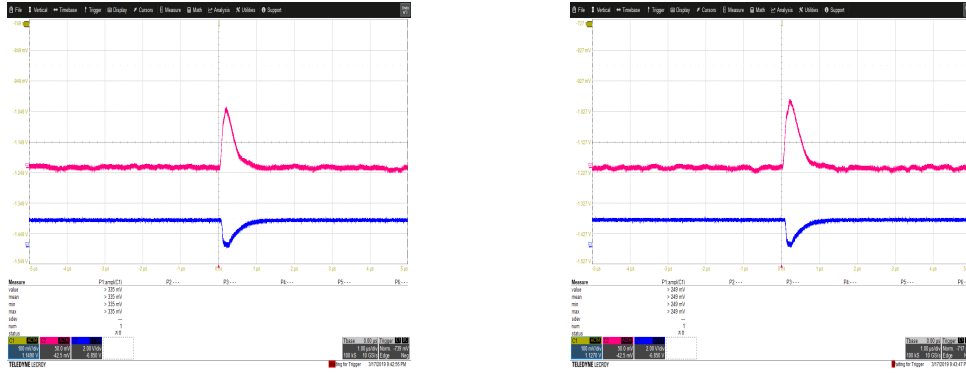


Figure 5.11. – I-V curve of LF-MONOPIX1 measured at room temperature.



(a) Flavor1: CMOS Amp + V2 Disc + P type source follower (b) Flavor2: CMOS Amp + V2 Disc + N type source follower

Figure 5.12. – The analog outputs of the CMOS flavors with readout logic outside pixel (Pink: Pre-amplifier output, Blue: Discriminator output).

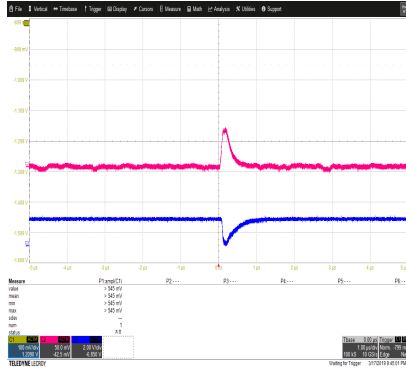
In order to investigate the power consumption of LF-MONOPIX1, a measurement of the pixel power consumption is performed for each flavor. Since the total current of the analog part (I_{Vdda}) contains consumption from pixel as well as the consumption in the global DAC block, the equation below gives the total current of one pixel with addition of the global DAC current.

$$I_{VddaP} = I_{globalDAC} + 1 \times I_{pixel} \quad (5.1)$$

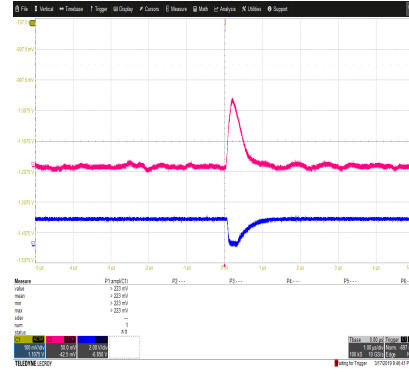
where $I_{globalDAC}$ is the current offered by global DAC block, I_{pixel} is the real pixel consumption.

The total current for one flavor (516 pixels) could be described by

$$I_{VddaF} = I_{globalDAC} + 516 \times I_{pixel} \quad (5.2)$$

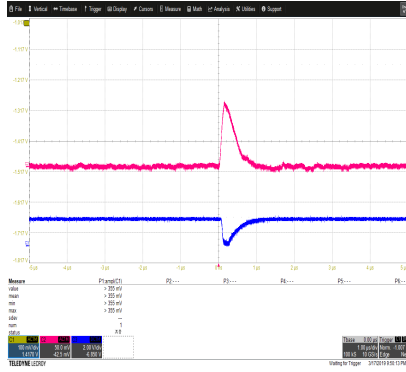


(a) Flavor3:CMOS Amp + V1 Disc + A&D

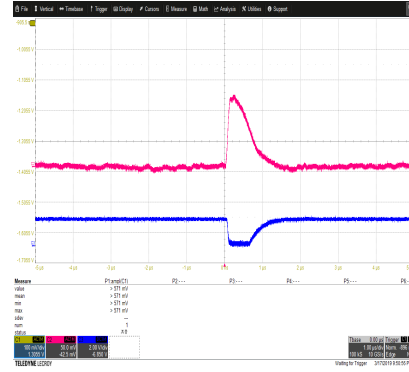


(b) Flavor4:CMOS Amp + V2 Disc + Digital discriminator domain

Figure 5.13. – The analog outputs of the CMOS flavors with readout logic inside pixel (Pink: Pre-amplifier output, Blue: Discriminator output).



(a) Flavor8:NMOS Amp + V2 Disc



(b) Flavor9:NMOS Amp + V1 Disc

Figure 5.14. – The analog outputs of the NMOS flavors with readout logic inside pixel (Pink: Pre-amplifier output, Blue: Discriminator output).

so the real pixel consumption can be given as,

$$I_{pixel} = \frac{I_{Vdda}f - I_{Vddap}}{515} \quad (5.3)$$

In red in Figure 5.15, we can find the real power consumption per pixel for each flavor. For most of these pixel implementations, the current of the pixel is around $16 \mu A$, so the power consumption per pixel is $\sim 28.8 \mu W$. This current value for single pixel matches with the design value ($17 \mu A$). But for flavor 3, 7 and 9, the current is higher than for other pixel implementations due to the analog contribution in the discriminator domain. The power consumption of these 3 flavors is around $37.8 \mu W$ per pixel. From the data shown in this table, it can also be found that the power consumption of pixels containing a V2 discriminator is lower than the pixel flavors with V1 discriminator.

Consumption @ Vdda=1.8V	lvdda	lvdda	lvdda	lvdda	lvdda	lvdda	lvdda	lvdda	lvdda
Enable only one pixel (Pp)	21.3mA	21.3mA	21.4mA	21.4mA	21.4mA	21.4mA	21.4mA	21.7mA	21.6mA
Enable one column (Pc)	23.4mA	23.4mA	24.1mA	23.5mA	23.5mA	23.6mA	24.2mA	23.6mA	24.2mA
Enable one flavor (Pf)	29.7mA	29.8mA	32.3mA	30.0mA	30.1mA	30.2mA	32.7mA	29.4mA	31.8mA
Consumption per pixel	16.3uA	16.3uA	21.1uA	16.7uA	16.9uA	17.0uA	21.9uA	14.9uA	19.8uA

Flavor No

R/O logic

Amplifier

Discriminator

Discriminator Domain

Token

Source Follower

1	2	3	4	5	6	7	8	9
Out		In-Pixel						
CMOS							NMOS	
V2		V1	V2	V1	V2	V1	V2	V1
Dig		A+D	Dig		A+D			
CMOS			Current Steering					
P	N							

Figure 5.15. – The LF-MONOPIX pixel power consumption for each flavor

5.2.3. ⁵⁵Fe and ⁹⁰Sr source test

In order to investigate the threshold distribution and noise for each flavor, the injection capacitance should be determined at the beginning of the measurement. Therefore, the LF-MONOPIX1 is exposed to a ⁵⁵Fe source, as shown in Figure 5.16. The pre-amplifier signal amplitude is shown in Figure 5.17b. The ⁵⁵Fe source is then removed and a test charge is injected to the same pixel by using external injection. The procedure consists then in finding the match between the mean amplitude of the peak of the ⁵⁵Fe source, and a specific injection test charge. According to the equation, as given in section 4.2.2.3.

$$C_{inj} = \frac{N \times e}{V_{inj}} \quad (5.4)$$

where C_{inj} is the injection capacitance, N is the number of electrons (⁵⁵Fe source: 1640 e-), e is elementary charge (1.6×10^{-19} C) and V_{inj} is the external injection voltage. With this procedure, the injection capacitance can be calculated.

Three boards were calibrated and show the similar results, as shown in Figure 5.18. The injection capacitance of CMOS input pre-amplifiers is around 2.4 fF, and 10% higher for the NMOS input pre-amplifiers flavors with respect to the CMOS input pre-amplifiers, around 2.6 fF.

The ⁵⁵Fe radioactive source emits X-rays with a characteristic peak of 5.9 keV energy, corresponding to around 1640 e- of deposited charge in the detector. An ⁵⁵Fe radioactive source spectra was obtained with the sensor biasing at -200V, as shown in Figure 5.19. The characteristic peak of the X-ray source spectra can be

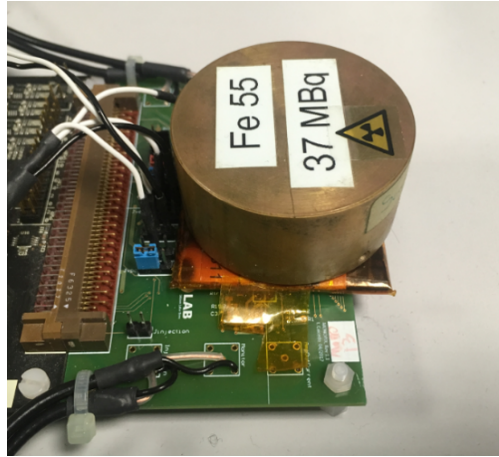


Figure 5.16. – The setup for injection capacitance calibration by ^{55}Fe

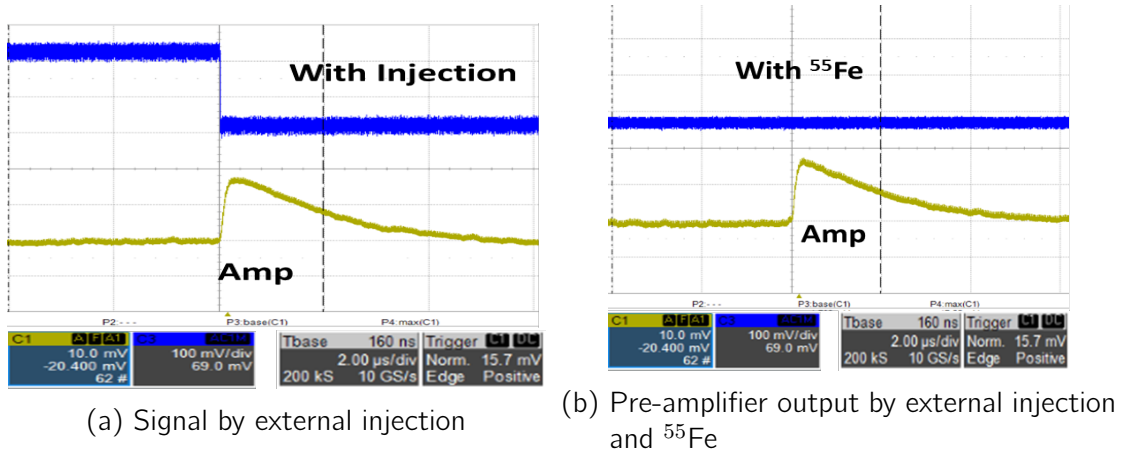


Figure 5.17. – ^{55}Fe source test

clearly identified around 1600 e-, the histograms also contain spectra of noise which was sampled at a fixed position before the rise of main pulse in each waveform.

To evaluate the overall detection performance, the LF-MONOPIX1 is exposed to ^{90}Sr β source as well. The setup for ^{90}Sr β source testing is shown in Figure 5.20a, a pre-amplifier response snapshot is also shown in Figure 5.20b. The source scan was performed with the same global TH for the whole matrix and the response of the matrix is shown in Figure 5.21. The profile of ^{90}Sr source can be identified clearly. The flavor border can be seen as well due to the differences in terms of gain of the pre-amplifiers between various pre-amplifier implementations.

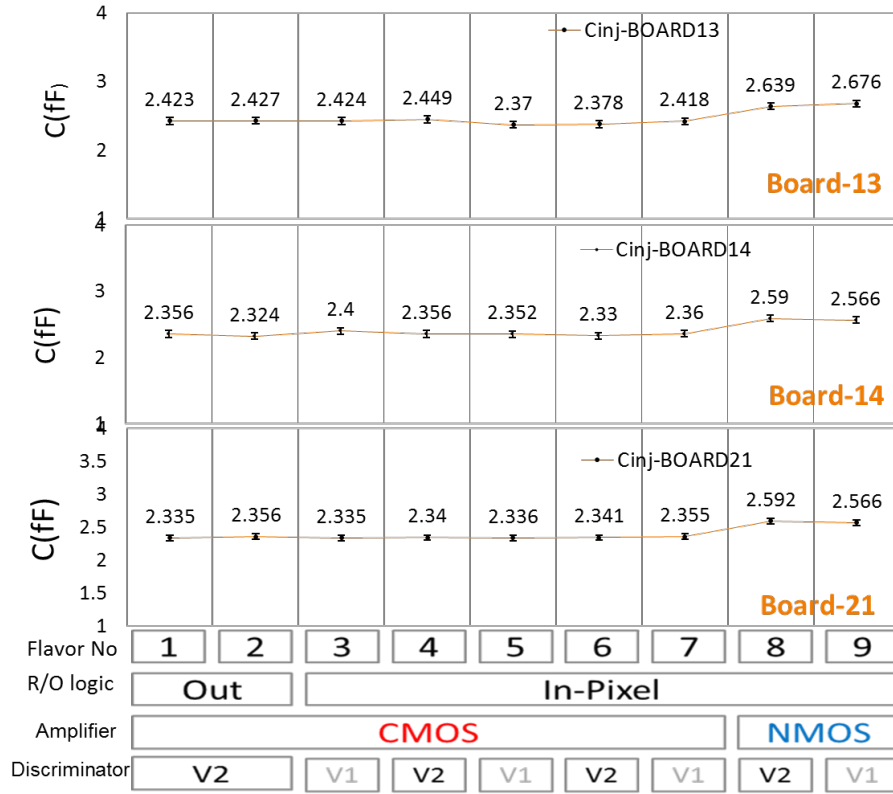


Figure 5.18. – The injection capacitance calibration for LF-MONOPIX by ^{55}Fe

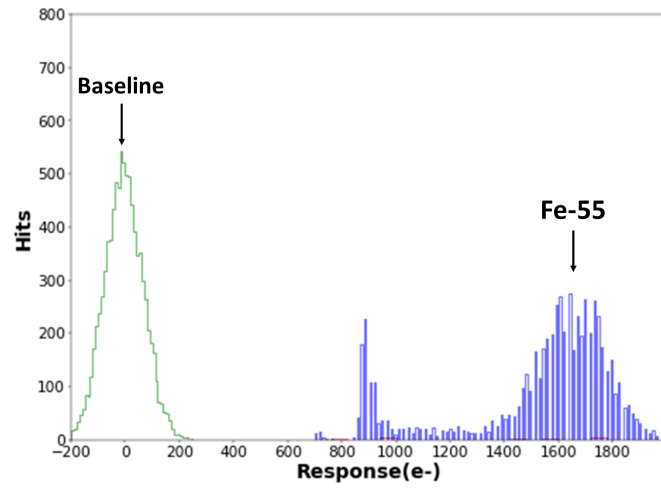


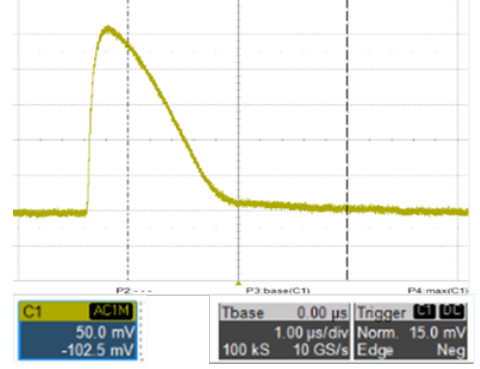
Figure 5.19. – ^{55}Fe radioactive source spectrum

5.2.4. ToT calibration

The ToT information allows to measure the radiation-induced charge collected in the pixel via measurement of the width of the pre-amplifier signal, which is



(a) The setup for ^{90}Sr source



(b) Signal output of ^{90}Sr

Figure 5.20. – ^{90}Sr source test

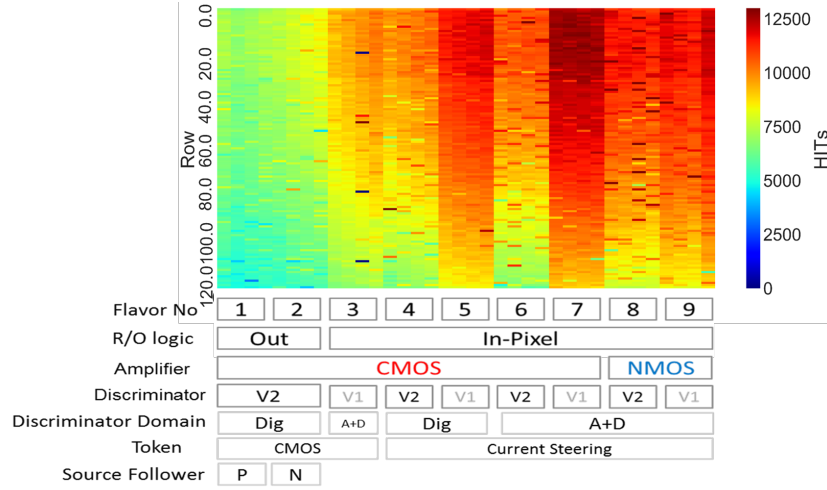


Figure 5.21. – Hitmap of LF-MONOPIX1 with a ^{90}Sr source

proportional to the deposited energy [118]. Figure 5.22 shows the schematic of the ToT working principle: the big signal has the larger ToT (on the left), the small signal has small ToT value (on the right).

In order to calibrate the ToT of LF-MONOPIX1, ToT measurements were done at external injection of 0.6 V and 1.0 V, as shown in Figure 5.23. At each test voltage, 1000 injections were performed, and for the default settings, the mean ToT value at 0.6 V and 1.0 V injection is 28 and 53 clock units respectively. To get ToT value as a function of the collected charge, the injection scan was performed for different pixels, which can be found in Figure 5.24. A saturation of the recorded ToT values was observed in each plot, the saturation value corresponds to approximately 1.2 V (20000 e-) converted by the ToT vs. Injection plots.

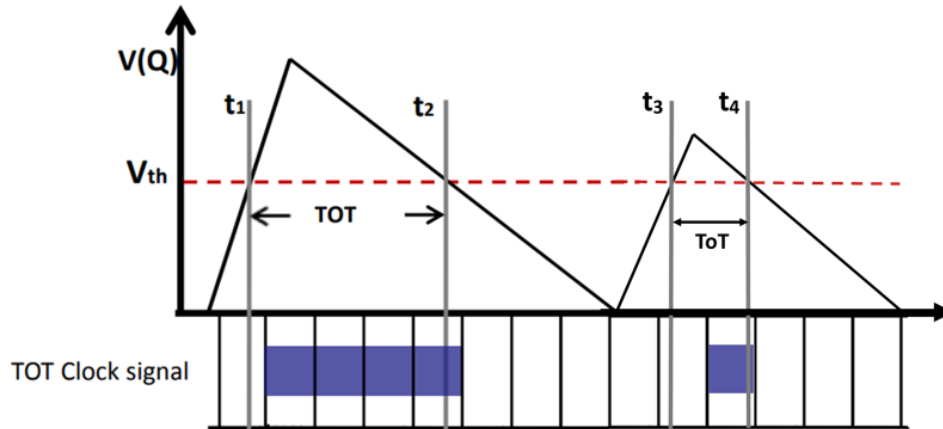


Figure 5.22. – Schematic of the ToT working principle.

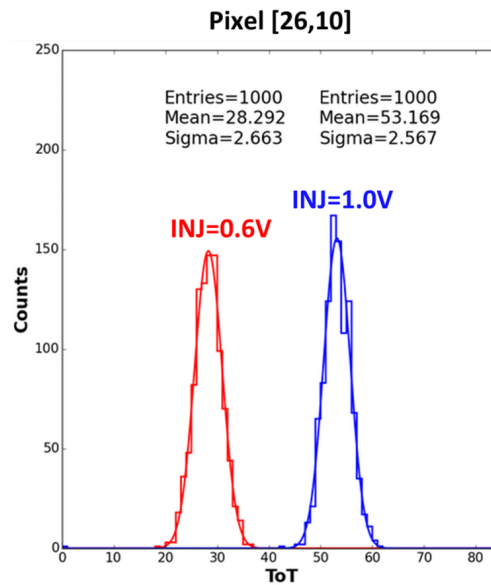
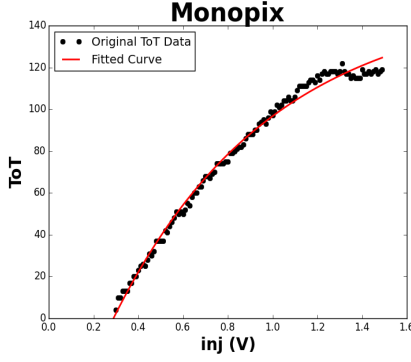


Figure 5.23. – TOT calibration at injection 0.6 V and 1.0 V (Flavor 7)

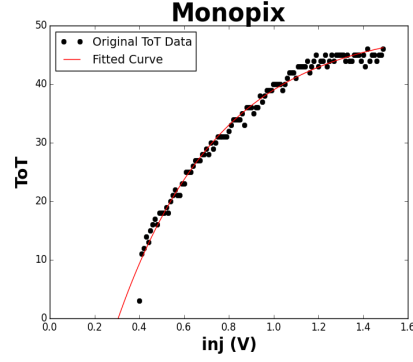
5.2.5. Injection scan and tuning test

After knowing the injection capacitance from the measurements in chapter 4.2.2.4, the injection scan and tuning was done for the whole matrix. A new tuning algorithm was developed to increase the tuning efficiency. The threshold tuning procedure is the following: threshold is tuned by setting the target threshold close to the mean threshold value, and then carrying out a 4-step binary search to optimize the local 4-bit "TRIM" threshold values by starting at the middle TRIM value "8".

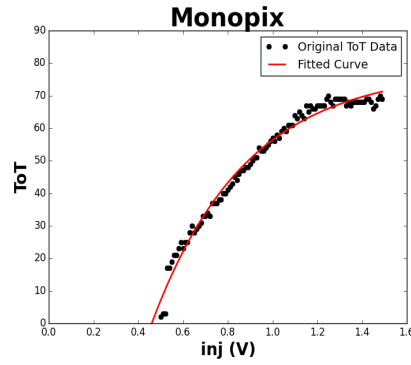
If the target value is greater than the threshold value at TRIM value "8", the search continues in the upper half of the TRIM range. By doing this, the algo-



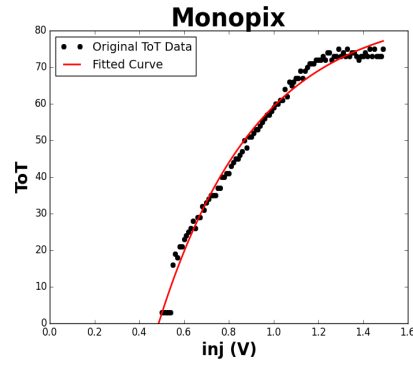
(a) Pixel: column1, row20 (Flavor 1)



(b) Pixel: column5, row20 (Flavor 2)



(c) Pixel: column9, row20 (Flavor 3)



(d) Pixel: column26, row20 (Flavor 7)

Figure 5.24. – The TOT calibration by external injection.

rithm eliminates the half in which the target value cannot lie in each iteration. Figure 5.25 gives an example of 4-step binary algorithm for threshold tuning, the TRIM value distribution is shown on the left after each step of the procedure. On the right, the threshold distributions can be found after each step. The distribution of TRIM values is a Gaussian like distribution after the last step. As the result of the procedure, the S-curve distribution of all the pixels gains in uniformity as shown bottom-right in Figure 5.25.

The injection scan and tuning was done for the Flavor 8 pixel implementation (NMOS Amp + V2 Disc) by using the binary algorithm, the results of the other 8 flavors are shown in ANNEXES 5.3.2.3. The threshold dispersion is 842 e- before tuning, the dispersion decreases to 94 e- after tuning. The comparison of the threshold distribution before tuning and after tuning is shown in Figure 5.26.

As a general remark, it should be noted that on one hand, the threshold should be low enough to register the charge from a minimum ionizing particle with high efficiency, otherwise some of these hits will be lost, but on the other hand, it should be high enough so that the number of recorded noise hit stays low. In order to investigate the low threshold ability, the same strategy as LF_CPIX was

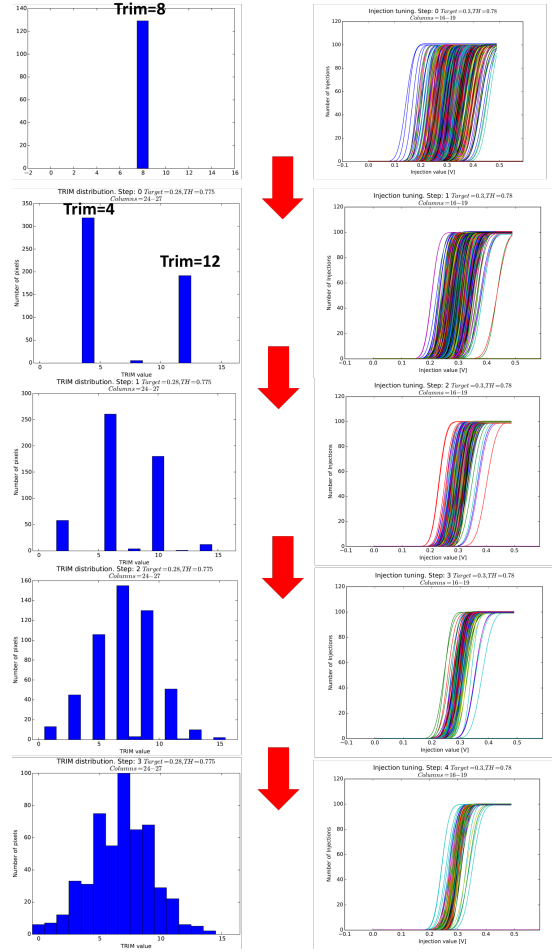


Figure 5.25. – 4 steps tuning procedure based on binary algorithm

implemented in LF-MONPIX1, and this strategy is sketched as in Figure 5.27.

By adopting the injection scan strategy for low threshold searching, sketched here, a mean threshold at 1755 e- could be achieved (see Figure 5.28). For this mean threshold value, the threshold dispersion is only 151 e-. The mean noise of pixels of the 8th flavor is shown in Figure 5.29, and is measured to be 187 e-, which is a good match to the simulation results (~ 160 e-).

The threshold map comparison before and after tuning is shown in Figure 5.30. The threshold map before tuning on the left side of Figure 5.30 exhibits rather important pixel to pixel non uniformity, while the threshold map after tuning on the right side is much more uniform inside each specific pixel implementation flavor individually (some noisy pixels in Flavor 8 were masked for Board-26).

In order to compare the performance of different designs, the same measurement strategy was implemented for the other 8 flavors as well. The threshold dispersion and noise of different flavors are shown in Figure 5.31. The threshold

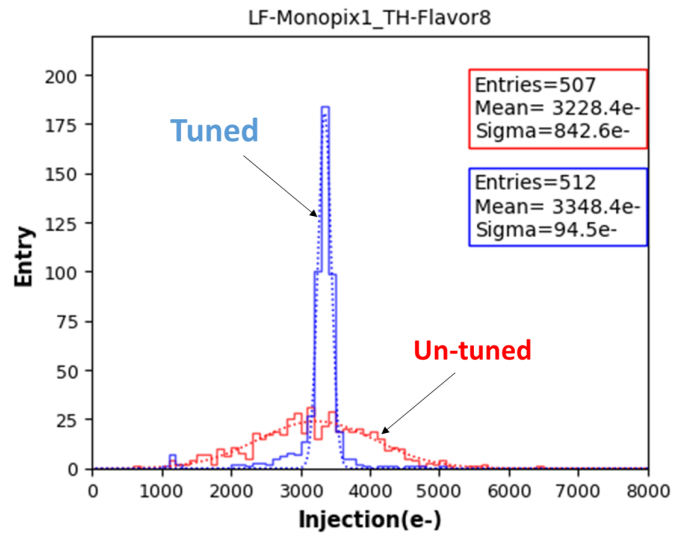


Figure 5.26. – Threshold distribution before tuning and after tuning for Flavor8 (NMOS Amp + V2 Disc).

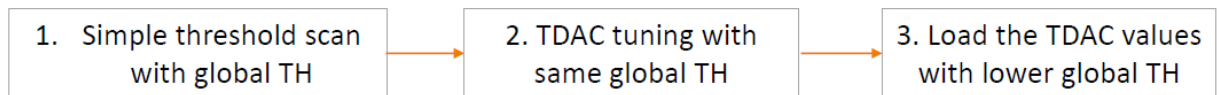


Figure 5.27. – The injection scan strategy for low threshold searching

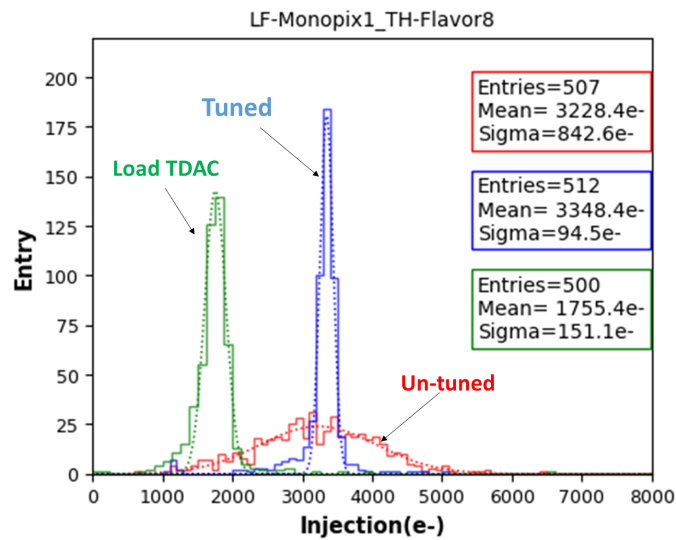


Figure 5.28. – Threshold distributions of load the TDAC scan for Flavor8 (NMOS Amp + V2 Disc).

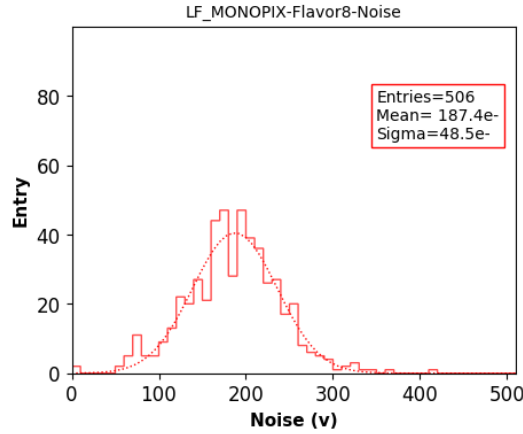


Figure 5.29. – The noise distribution of Flavor8 (NMOS Amp + V2 Disc).

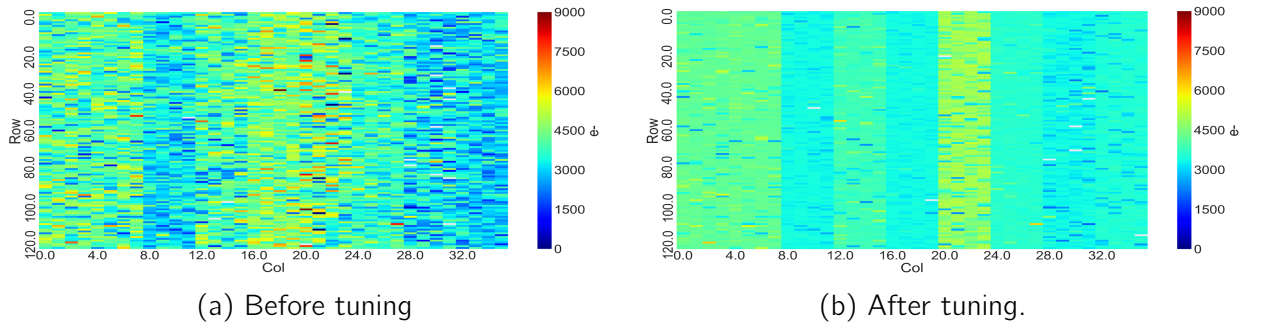


Figure 5.30. – The threshold map of LF-MONOPIX1(Board-26).

dispersion of all the nine flavors can be tuned down to less than 100 e-. In this plot, it can be seen that the pixel implementation using V1 discriminator have lower threshold dispersion than the one using the V2 discriminator implementation. In terms of noise performance for the different flavors, the pixel flavor8 and the pixel flavor9 implementations using with NMOS input pre-amplifier give lower noise than the designs with CMOS input pre-amplifier.

More boards were tested with the same protocol. Figure 5.32 shows the map of the thresholds for Board-22 before and after tuning, where it can be seen that all the pixel implementations can be tuned as well. This board has similar performance with respect to the threshold dispersion and noise (see Figure 5.33).

It can be concluded that the NMOS input pre-amplifier has better performance on noise and V1 discriminator shows less threshold dispersion and these building blocks could be very good choices for future IC implementations in this technology.

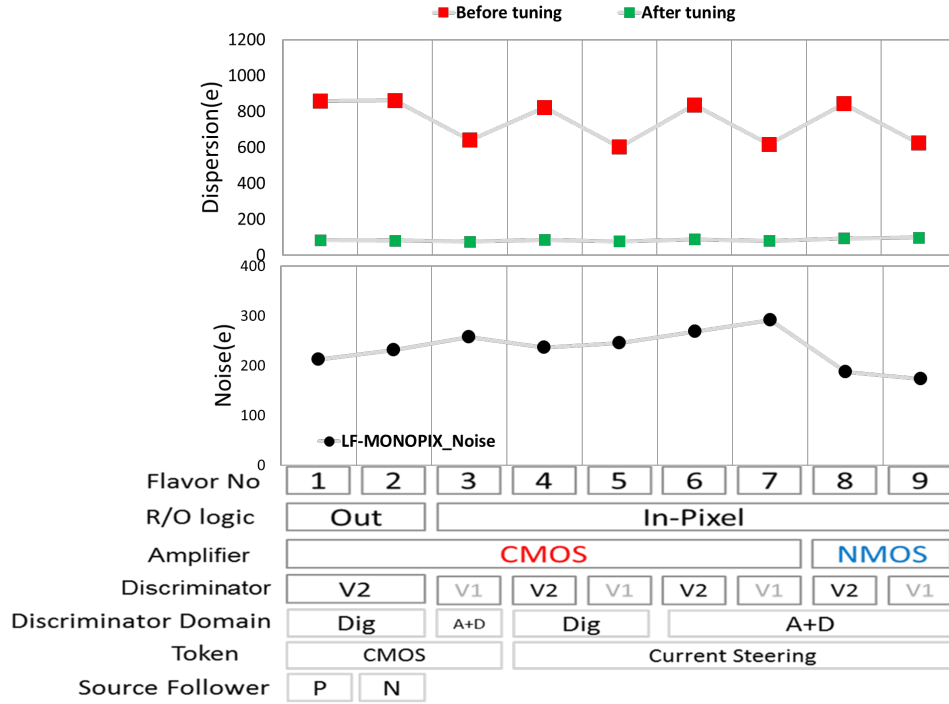


Figure 5.31. – LF-MONOPIX1 threshold dispersion and noise (Board-26).

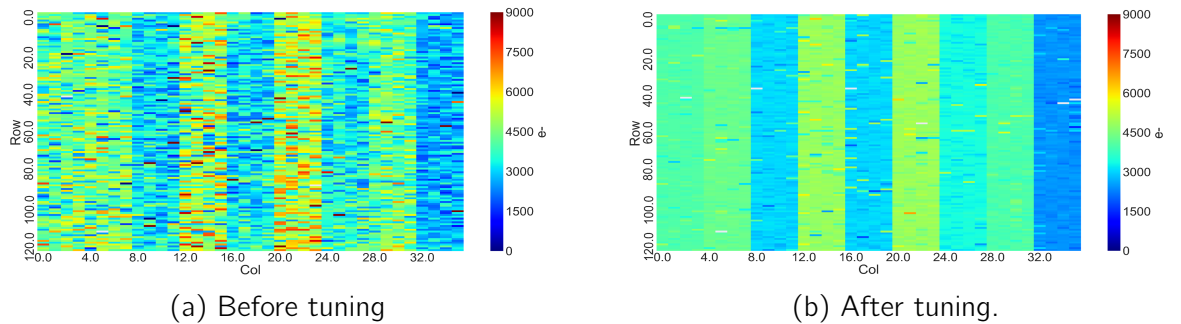


Figure 5.32. – The threshold map of LF-MONOPIX1(Board-22).

5.3. Irradiated devices characterization

As shown in section 4.3, radiation hardness of the technologies that could be used is one of the top priorities for our applications. In order to investigate the radiation hardness of the LF-MONOPIX1 demonstrator, prototypes were irradiated under the 24 GeV IRRAD proton facility in CERN at room temperature. This irradiation facility is very interesting for our studies as protons of this energy trigger both NIEL damage and TID effects, and both topics is of importance to the developments in our context. Two irradiation campaigns were deployed in May 2018 and October 2018 respectively. A passive setup was installed during

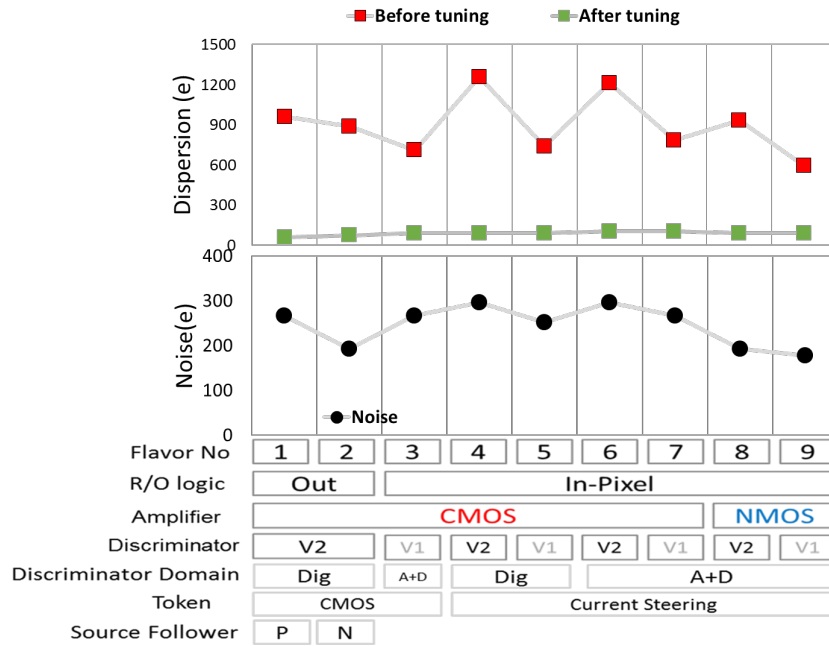


Figure 5.33. – LF-MONOPPIX1 threshold dispersion and noise (Board-22).

the first irradiation campaign in May 2018, which would not allow complete monitoring of all chips' characteristics, as a more elaborated solution (called "active setup") was under development at that time. Both active setup and passive setup were implemented during the second irradiation campaign in October 2018.

5.3.1. Irradiation campaign with passive setup in May 2018

5.3.1.1. Passive setup development

The passive setup was the first developed test setup solution, which allows only an easy on-line monitoring of the power consumption and of leakage current. Still, more measurements can obviously be done after dismounting the prototypes from the table. In this setup, five pads were polarized: Vdda, Vddd, Vdd_EOC and HV. HV is the high voltage applied on the sensor part of LF-MONOPPIX1 to polarize the sensor and test the leakage current and the breakdown voltage. All the polarization are handled by the mean of a patch panel between the control room and the irradiation zone. The setup in the control room is shown in Figure 5.34, the "TTi" DC power supplies are used for low voltage polarization, the Keithley 2400 source meter is used for high voltage supply. The setup in the irradiation zone is shown in Figure 5.35. For this first irradiation of the LF-MONOPPIX1 in May 2018, two prototypes (LF-MONOPPIX1_14 and LF-MONOPPIX1_21) were installed on the table in the irradiation zone.

The time line of LF-MONOPPIX1 irradiation campaign is described in Figure

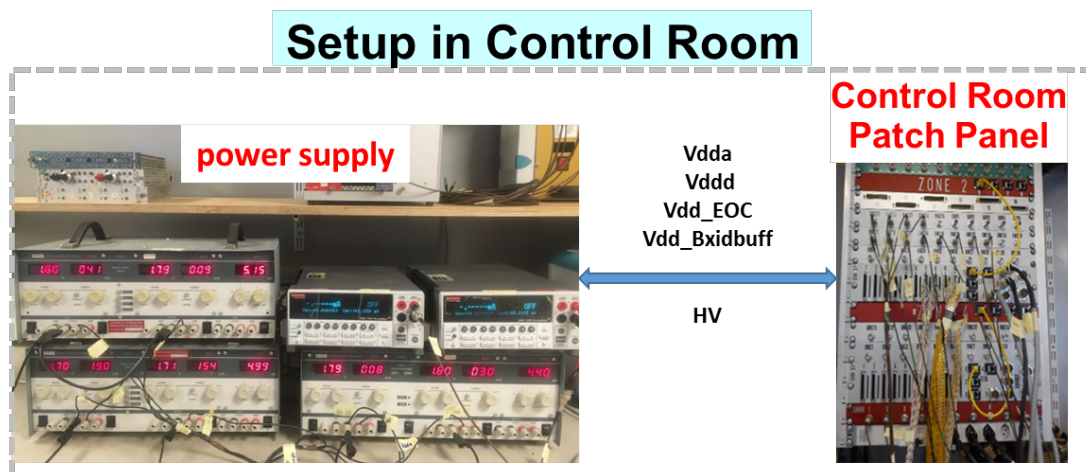


Figure 5.34. – LF-MONAPIX1 setup in the control room

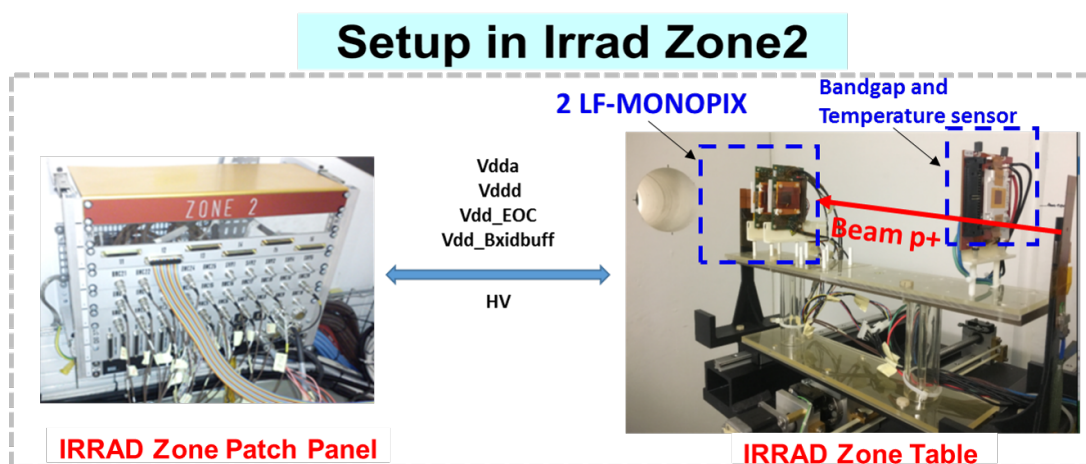


Figure 5.35. – LF-MONAPIX1 setup in the Irrad zone 2

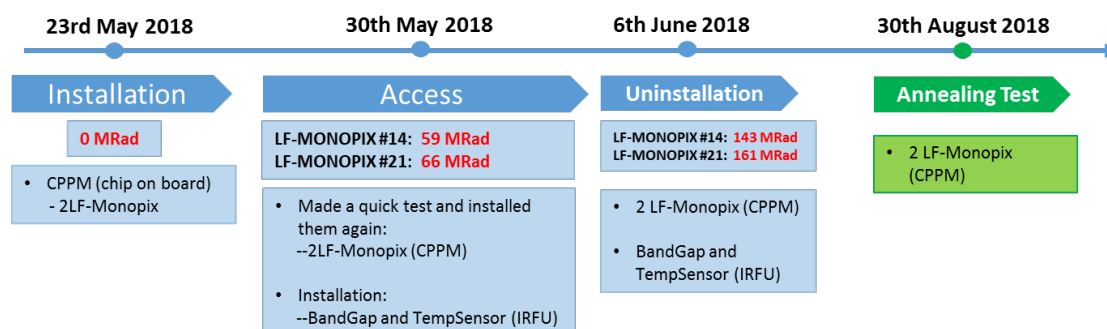


Figure 5.36. – The time line of LF-MONAPIX1 May 2018 irradiation campaign.

5.36. The 2 prototypes were installed on May 23rd 2018. Since the analog outputs and digital readout can not be tested on-line with the rather simple test setup that was used at this time, the 2 prototypes were dismantled after 7 days of irradiation (and recorded TIDs of about 50 MRad each for the two boards) and a few measurements were then performed on the analog outputs as well as an injection scan. The prototypes were then reinstalled on the irradiation table and the irradiation went on. One bandgap and temperature sensor prototype in TowerJazz 180nm CMOS technology was also mounted on the same table at this point. When the 2 prototypes were irradiated up to 143 MRad and 161 MRad respectively, we dismantled all the prototypes from the table.

5.3.1.2. Leakage current measurement

The leakage current of the two LF-MONOPIX1 prototypes was measured at different dose points during the irradiation, at room temperature (21 °C). The leakage currents for different values of the reverse voltage as a function of dose for both prototypes are shown in Figure 5.37. Both chips show similar leakage current degradation curve profile with the leakage current increasing a lot at the very beginning of the irradiation campaign and becoming relatively stable with the increasing dose afterwards.

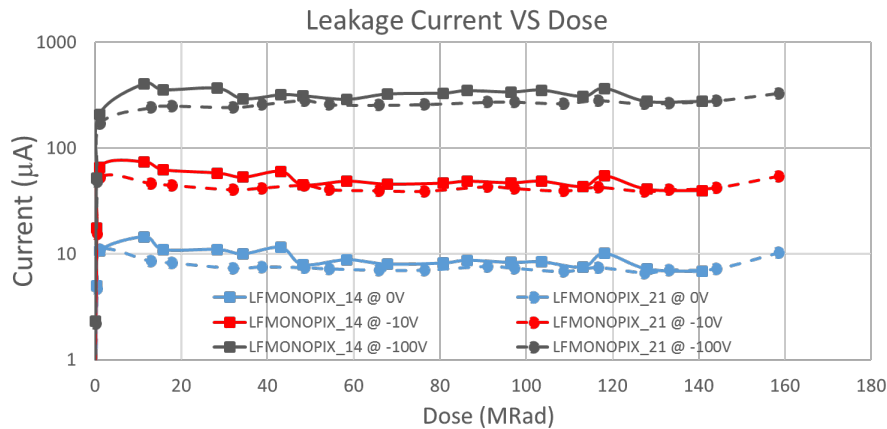


Figure 5.37. – The leakage current of LF-MONOPIX1_14 and LF-MONOPIX1_21 as a function of dose at different voltages.

The I-V curve of LF-MONOPIX1_14 is shown in Figure 5.38, the leakage at -100V increases from $0.18 \mu\text{A}/\text{cm}^2$ to $680 \mu\text{A}/\text{cm}^2$ at room temperature after an irradiation to 143 MRad and $3.26 \times 10^{15} n_{eq} \cdot \text{cm}^{-2}$. After dismantling the two prototypes from the table, it was possible to test the I-V curve of prototype in a cooling box. The current decreased from $680 \mu\text{A}/\text{cm}^2$ to $30.5 \mu\text{A}/\text{cm}^2$ at -100V

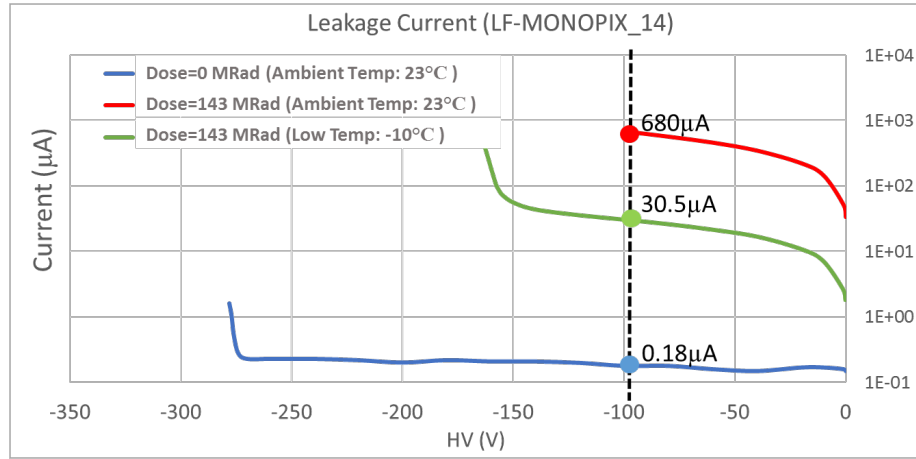


Figure 5.38. – The leakage current of LF-MONOPIX1_14 after 143 MRad and $3.26 \times 10^{15} n_{eq} \cdot cm^{-2}$ radiation.

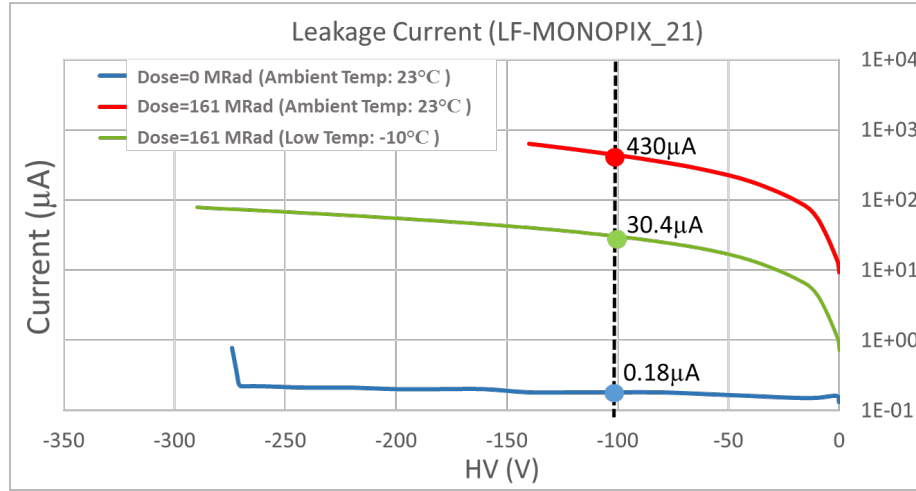


Figure 5.39. – The leakage current of LF-MONOPIX1_21 after 161 MRad and $3.67 \times 10^{15} n_{eq} \cdot cm^{-2}$ radiation.

when the sensor was cooled down to $-10^{\circ}C$ and the per-pixel leakage current appears to be less than 6.6 nA, well below the HL-LHC design requirement value (10 nA/pixel). A similar results for LF-MONOPIX1_21 is shown in Figure 5.39. The leakage current of LF-MONOPIX1 prototypes shows the same order of magnitude as LF-CPIX prototypes after radiation.

5.3.1.3. Pixel matrix measurements

After dismounting the prototypes from the table, it is possible to test them locally. The LF-MONOPIX1_21 pre-amplifier analog output of some pixels in column 30 were tested as shown in Figure 5.40. It was noticed that the trailing edge

of the pre-amplifier output was getting longer with increasing the row number. In order to investigate this behavior, a ToT measurements was performed as shown in Figure 5.41 and big differences between outputs of pixel [30,0] and [30,120] can be seen. This behavior is probably due to the poor uniformity of the beam spot.

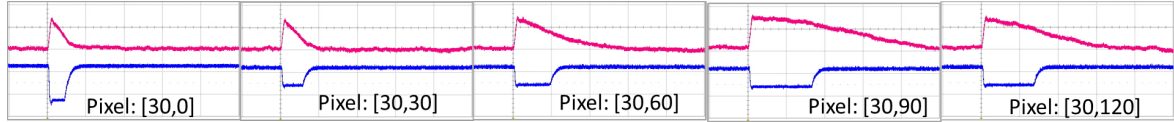


Figure 5.40. – Some examples of LF-MONPIX1 pre-amplifier outputs after radiation.

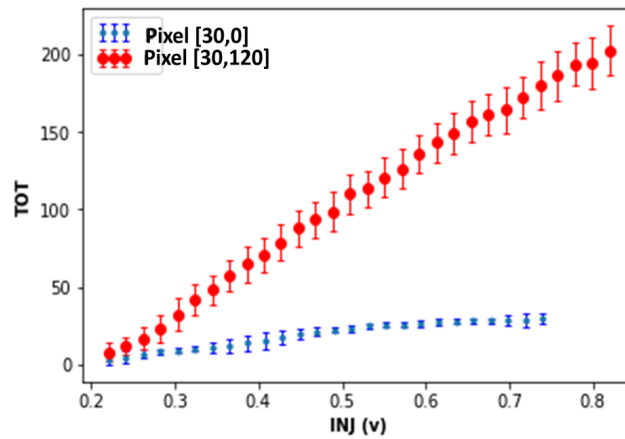
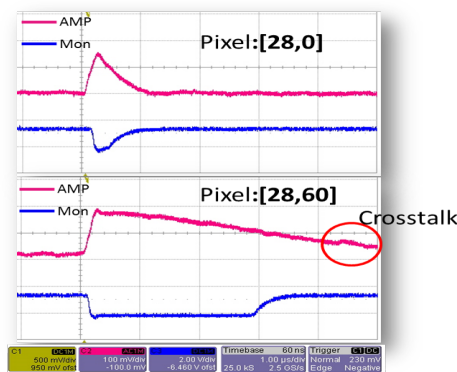
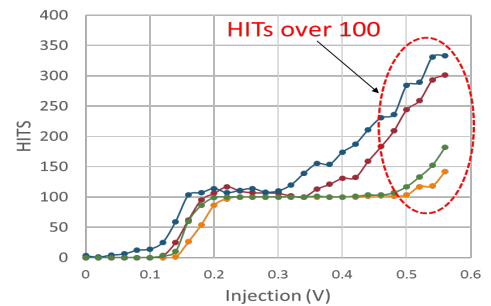


Figure 5.41. – ToT outputs after radiation.



(a) Crosstalk with long trailing edge



(b) Hits over 100 at high injection value

Figure 5.42. – The over-hits problem caused by crosstalk.

But in all cases, after irradiation the trailing edge of the amplifier output becomes longer. This issue is probably caused by the radiation effect on the pre-amplifier feedback resistance. In particular for the pixels with high row number, the trailing edge of the amplifier is so long that crosstalk from the digital signal can be seen, as shown in Figure 5.42a. The crosstalk can make the S-curve profile get worse as over hits can be seen at high injection pulse, as shown in Figure 5.42b. In order to mitigate this crosstalk effect, the digital readout signals were improved by delaying the digital signals in the firmware. Figure 5.43a shows the digital readout signals and discriminator output by using the original firmware version, for which one analog output (yellow line) can have multiple token out signal (pink line) which arbitrate the pixel readout propagation, hence showing the origin of the problem of the S-Curve with over-hits. Figure 5.43b shows the digital readout signals and discriminator output from the same pixel when using the improved of the firmware. There is no multiple digital outputs any more.

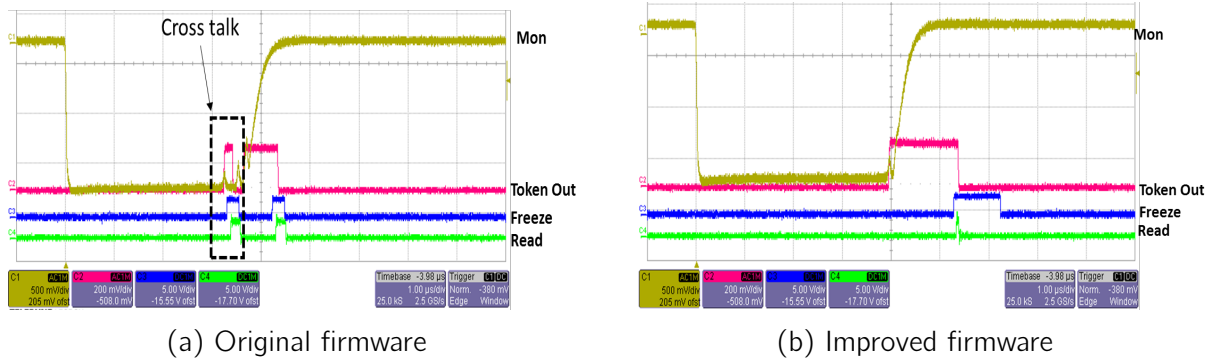


Figure 5.43. – The outputs of LF-MONOPPIX1_21 with different firmware version.

The injection scan was done with the improved firmware for the whole matrix after radiation. The threshold and noise maps are shown in Figures 5.44a and 5.44b respectively. The darker color on the top side can be seen in Figure 5.44a, it indicates that the pixel's threshold on the top side is higher than on the bottom side. Three pixel implementation flavors (shown in gray in the Figure) cannot be scanned with a fixed global TH.

To verify the threshold tuning ability after radiation, the threshold tuning was performed for all pixels of flavor 8 at -12°C . Figure 5.45a gives a comparison before tuning and after tuning of the pixel thresholds, and the dispersion after tuning at -12°C is only 156 e-. The mean noise in both cases is around 260 e- as can be seen in Figure 5.45b.

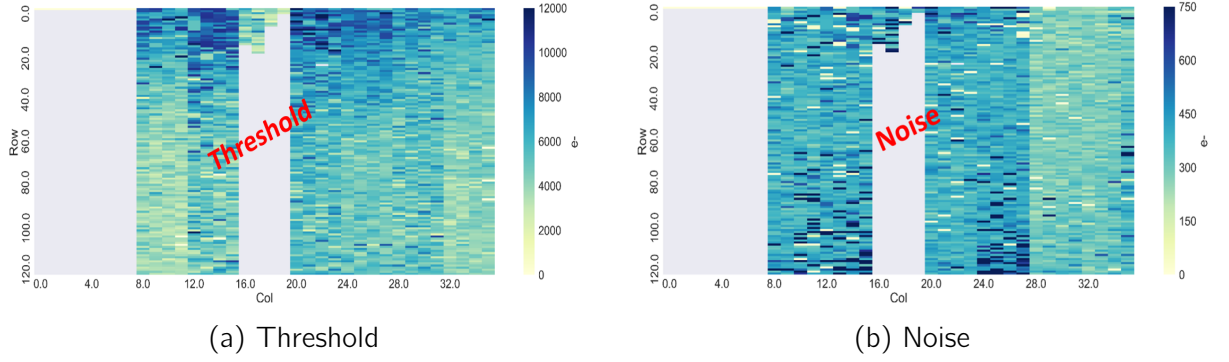


Figure 5.44. – The threshold and noise map of LF-MONOPIX1_21 after radiation.

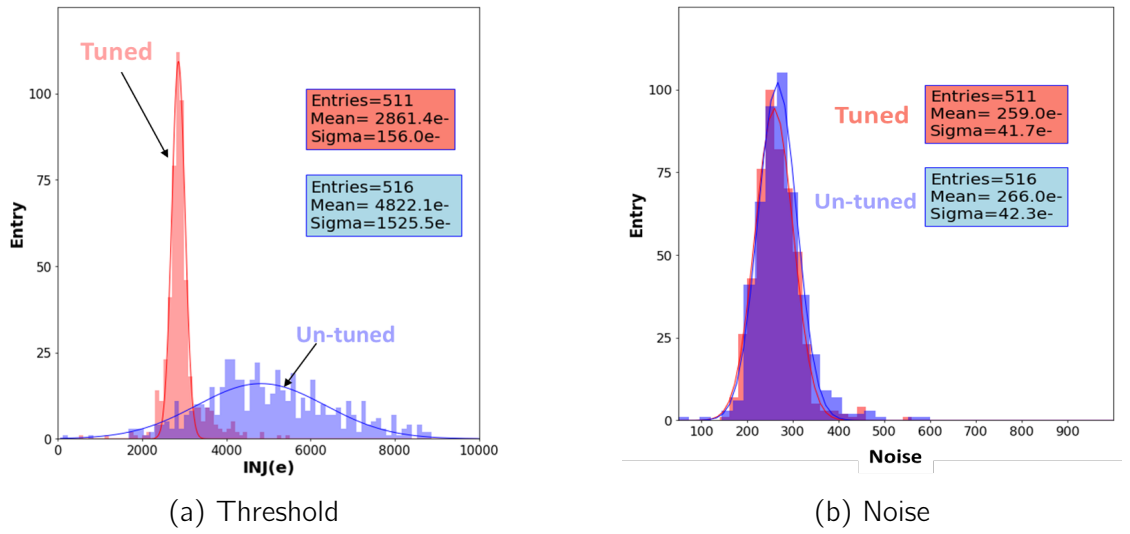


Figure 5.45. – The threshold and noise histogram of LF-MONOPIX1_21 after radiation for pixels of Flavor 8.

5.3.2. Irradiation campaign with active setup in October 2018

In order to monitor the sensor part and readout logic during the radiation and verify the radiation hardness of LF-MONOPIX1 for both NIEL and TID effects, a second irradiation campaign was deployed in October 2018. For this irradiation campaign, the initial setup was improved and evolved in a setup version for which, despite the distance between data acquisition system and DUT, continuous monitoring could be assured. For practical reasons, both active setup and passive setup were used during this campaign. Four LF-MONOPIX1 prototypes differing in terms of chip thickness, backside processes and sensor biasing strategy, were installed in the 24 GeV IRRAD proton facility at CERN. The list of the measured prototypes can be found in table 5.2.

Sample ID	Chip thickness	Setup	Comment
LF-MONOPPIX1_100	750 μm	Active	Backside metallization, HV polarization on backside
LF-MONOPPIX1_101	750 μm	Active	Backside metallization, HV polarization on backside
LF-MONOPPIX1_102	200 μm	Passive	Backside metallization, HV polarization on backside
LF-MONOPPIX1_103	100 μm	Passive	No backside metallization, HV polarization on front side

Table 5.2. – LF-MONOPPIX1 prototypes on the beam table

5.3.2.1. Active setup development

In order to construct the active setup, all the polarization, analog and digital readout signals should be connected between radiation zone and control room. All the signals used to control the prototypes are listed in Table 5.3. The diagram of the active setup is shown in Figure 5.46. Figure 5.47 gives more details on the part of the setup sitting in the control room, while the prototypes were installed on the beam table in the irradiation zone as shown in Fig 5.48. Since the LVDS signals can be transmitted with low power and high speed, single ended digital signals are converted to LVDS signals between the irradiation zone and the control room before being transmitted over the approx. 20 meter long cables. The powering and polarization signals are connected by long burndy cables; all the analog input and output signals are communicated through 20 meter Lemo cables. The LVDS to single ended translator board and the interface board are coupled to the GPAC board and the Multi-IO board in the control room, as can be glanced on the table 5.47. The GPAC board provides an injection pulse generator, plus 12-bit DACs, ADCs, power sources and the possibility to probe digital and analog signals. The Multi-IO board holds a programmable Kintex7 FPGA and it allows to communicate via Ethernet with a PC [98].

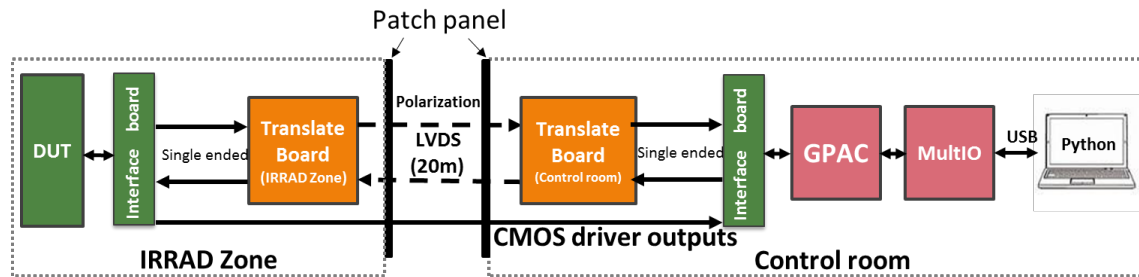


Figure 5.46. – The diagram of LF-MONOPPIX1 active setup

5.3.2.2. Leakage current measurement

The leakage current was tested at different dose point during the irradiation at room temperature (21 °C), The TID points at which measurements were performed are shown in Figure 5.49. The leakage currents of the four prototypes at

Parameter	LF-MONOPIX1 Signals	Description	Typical Value
Analog Input	Vdda, VddaSense	in-pixel analog supply	1.8 V
	Vddd, VdddSese	in-pixel digital supply	1.8 V
	Vdd_Bxidbuff	buffers distributing BXid supply	1.2 V
	Vdd_EOC	End of Column (EOC) logic	1.8 V
	Vpc	pre-charge voltage of sense ampl (AC coupled to CSA's output)	1.5 V
	VcascN	bias voltage for NMOS CSA's cascode	0.4 V
	VcascC	bias voltage for CMOS CSA's cascode	0.8 V
	BL	baseline potential of input to comparator	0.75 V
Digital Input	TH	global threshold voltage of discriminator	BL+30mV
	CLK_BX	Bunch crossing (BX) clock input	40 MHz
	READ	READ signal	
	FREEZE	FREEZE signal	
	Nrst	active low reset of in-pixel logic	1.8 V
	EN_Test_Pattern	enable for serializer test pattern output (for synch.)	1.8 V
	RST_Grey	reset for grey counters (BX encoding)	
	EN_Drive	enable of LVDS driver	0 V
Digital Output	EN_Data_CMOS	enable for CMOS output of serializer (backup for LVDS)	1.8 V
	CLK_OUT	serializer clock	160 MHz
	Token_Out	hit token output	
Analog Output	Data_Out	serialized hit data output	
	Injection	injection pulse input	
	Monitor	output of comparator's monitor	
Ground	Ampout	voltage output of CSA	
	gnda	GND	0 V
HV	HV	bias of pwell ring around pixels	0-300 V

Table 5.3. – LF-MONOPIX1 signal list for irradiation in an active test setup configuration.

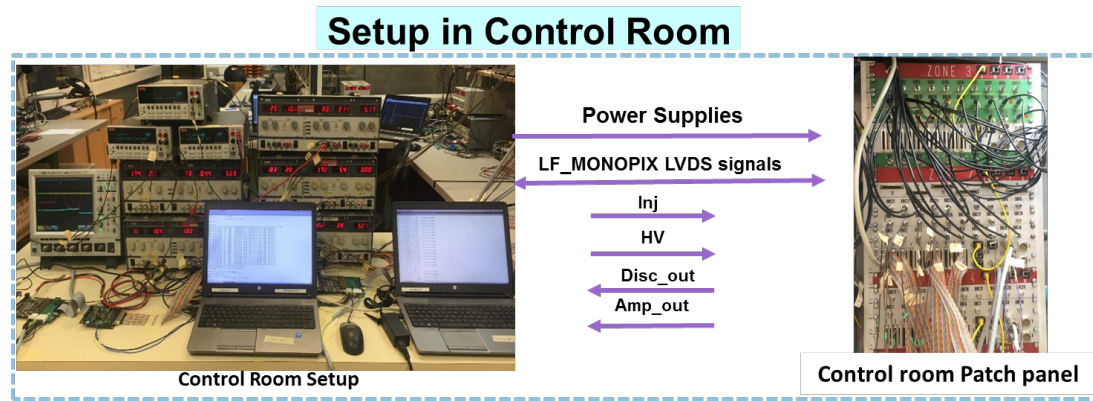


Figure 5.47. – LF-MONOPIX1 active setup in control room

-10 V, -100 V and -200 V as a function of dose are shown in Figure 5.50. Both 750 μm chips with backside processing (chip 100 and 101) show similar leakage

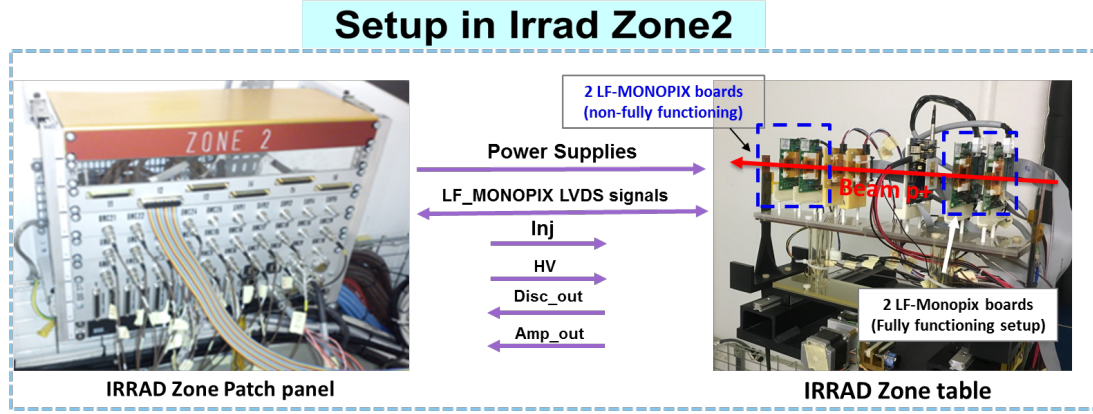


Figure 5.48. – LF-MONOPIX1 active setup in Irrad zone 2

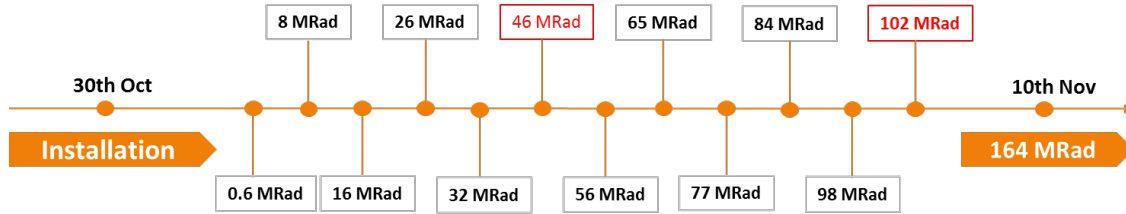
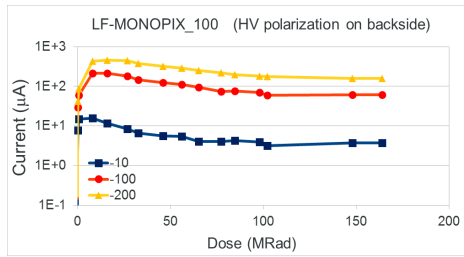


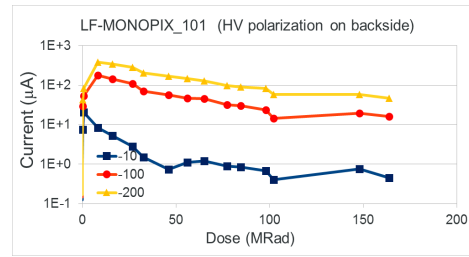
Figure 5.49. – The testing dose point during the irradiation campaign

current degradation curve profile. The leakage current increased a lot at the very beginning of the irradiation campaign and became relatively stable with the increasing dose afterwards. The other two prototypes which were thinned down to $200\ \mu\text{m}$ (chip 102) and $100\ \mu\text{m}$ (chip 103) seem more sensitive to the radiation. The leakage current is higher than for the thicker chips, so to avoid damaging the sensor, the leakage current was not measured at high voltage and high dose.

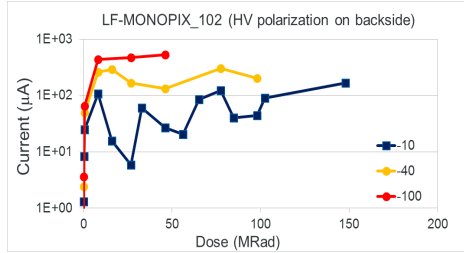
The I-V curve of LF-MONOPIX1_100 is shown in Figure 5.51a. The leakage current at $-100\ \text{V}$ biasing increases from $0.15\ \mu\text{A}/\text{cm}^2$ to $58\ \mu\text{A}/\text{cm}^2$ at room temperature after $\text{TID} = 164\ \text{MRad}$ and $\text{NIEL} = 3.74 \times 10^{15}\ n_{eq} \cdot \text{cm}^{-2}$, and the current decreased to $2.8\ \mu\text{A}/\text{cm}^2$ at $-100\ \text{V}$ in a cooling box at -22°C . It is to be noted that this value meets the requirement for the ATLAS ITK upgrade. The LF-MONOPIX1_101 shows similar results as LF-MONOPIX1_100. For LF-MONOPIX1_102 (the prototype with $200\ \mu\text{m}$ thickness), the breakdown voltage is only -130V before radiation, and the current is $17.3\ \mu\text{A}/\text{cm}^2$ at -100V in a cooling box at -22°C after a recorded $164\ \text{MRad}$ TID and $3.74 \times 10^{15}\ n_{eq} \cdot \text{cm}^{-2}$ NIEL. LF-MONOPIX1_103 (the prototype with only $100\ \mu\text{m}$ thickness) needs to be biased from the front side as neither backside processing nor metallization were implemented for this thin sensor. After an irradiation to a TID of $164\ \text{MRad}$ and NIEL of $3.74 \times 10^{15}\ n_{eq} \cdot \text{cm}^{-2}$, the leakage current is $7.9\ \mu\text{A}/\text{cm}^2$ in a cooling box at -22°C .



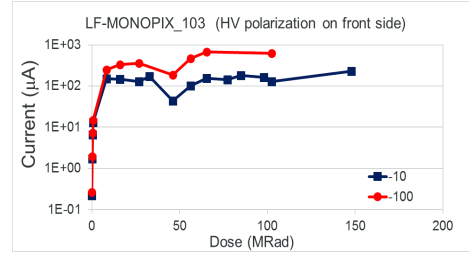
(a) LF-MONAPIX1_100



(b) LF-MONAPIX1_101

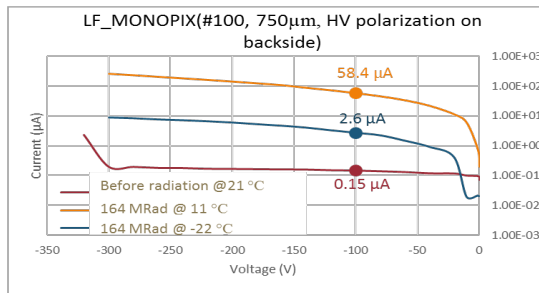


(c) LF-MONAPIX1_102

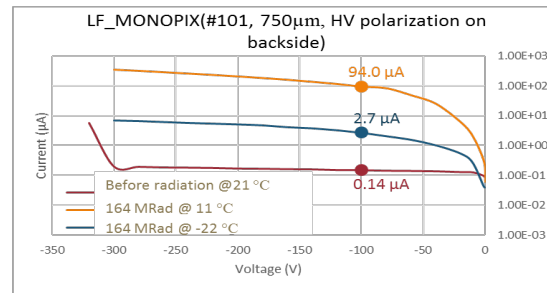


(d) LF-MONAPIX1_103

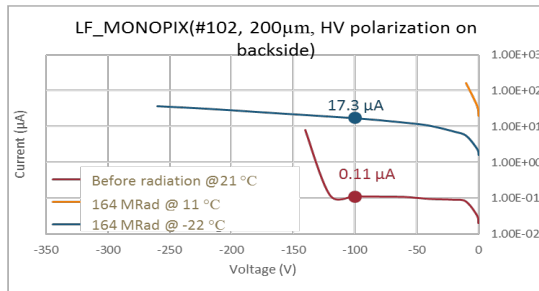
Figure 5.50. – The leakage current of LF-MONAPIX1 chips as a function of dose at 21 °C.



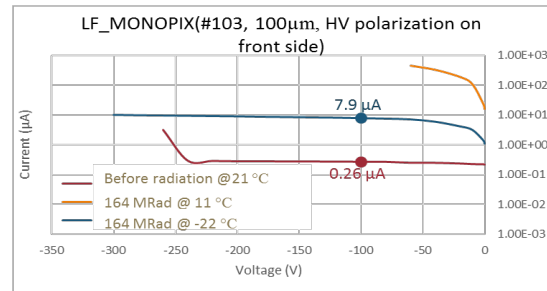
(a) LF-MONAPIX1_100



(b) LF-MONAPIX1_101



(c) LF-MONAPIX1_102



(d) LF-MONAPIX1_103

Figure 5.51. – The leakage current after radiation at room temperature and low temperature.

5.3.2.3. Pixel matrix measurements

Since the LF-MONOPIX1_100 and LF-MONOPIX1_101 prototypes were installed with the active setup, the injection scan was done during the irradiation at different dose point. Because of the time needed for the tests and risk of annealing, only one column (129 pixels) for each flavor was tested.

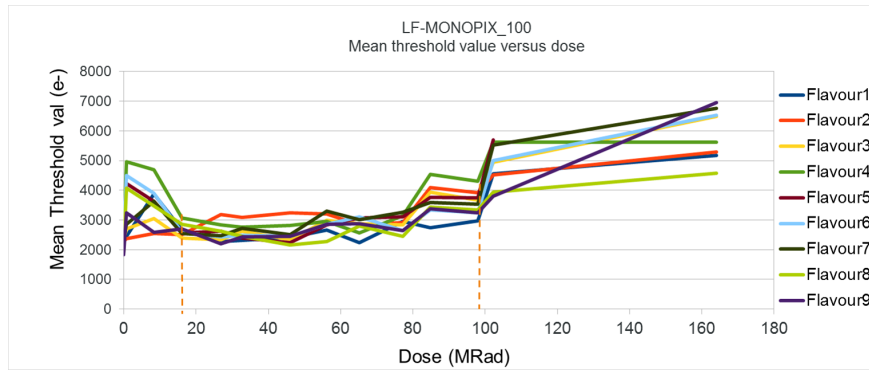


Figure 5.52. – Mean threshold value of LF-MONOPIX1_100 as a function of TID

The mean threshold value of LF-MONOPIX1_100 stayed stable until 80 MRad for all flavors, and started to increase afterwards due to the global threshold shifting by radiation effect, as shown in Figure 5.52. The threshold dispersion was also stable except flavor2 until 80 MRad, as shown in Figure 5.53. The noise jumped at the very beginning of the irradiation campaign in the few first MRads and became relatively stable with the increasing dose afterwards. The flavor8 and flavor9 pixel implementation which are NMOS input transistor pre-amplifier, show much better noise performance than other flavors, as shown in Figure 5.54. The prototype LF-MONOPIX1_101 has a similar behavior as LF-MONOPIX1_100, the threshold and dispersion stayed relatively constant under 80 MRad, the noise increased a little at the very beginning of the irradiation campaign and became stable afterwards and the noise of flavor8 and flavor9 is lower than other flavors. The corresponding distributions are shown in Figure 5.55, 5.56 and Figure 5.57. It should be underlined that all this characterization was done in-situ, hence the temperature of the prototype was around 21 °C.

An injection scan was performed at the end of irradiation campaign and the threshold map of LF-MONOPIX1_100 is shown in Figure 5.58a. All the flavors are working but the threshold distribution of flavor7 shows a large variation between top and bottom pixels. A similar behavior is obtained in prototype LF-MONOPIX1_101, as shown in Figure 5.59a. The noise map of LF-MONOPIX1_100 is shown in Figure 5.58b; in this noise map, a small area with higher noise can be identified, this is probably due to a relatively poor uniformity of the beam spot. A similar phenomenon can be found in Figure 5.60b.

In order to verify the tuning ability after radiation, the flavor8 pixel implementation of LF-MONOPIX1_101 was measured after 24 days room temperature

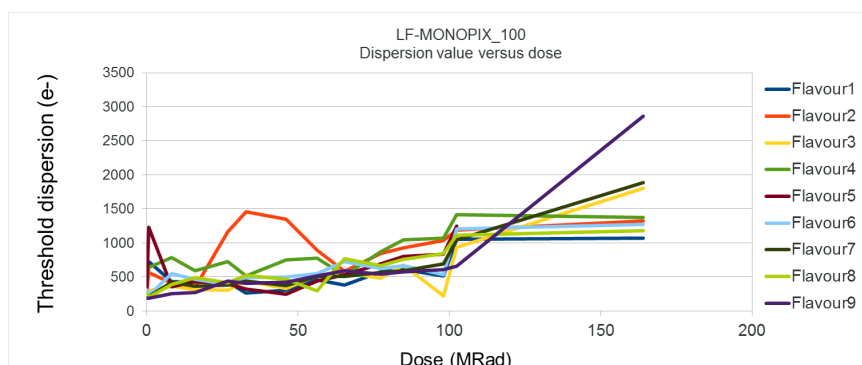


Figure 5.53. – The threshold dispersion of LF-MONOPIX1_100 as a function of dose

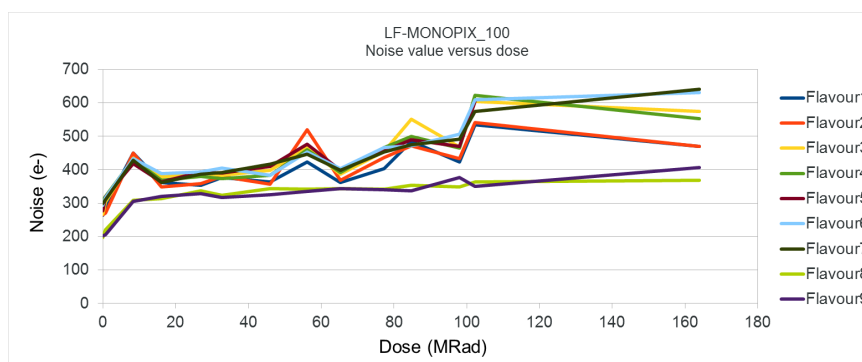


Figure 5.54. – The noise of LF-MONOPIX1_100 as a function of dose

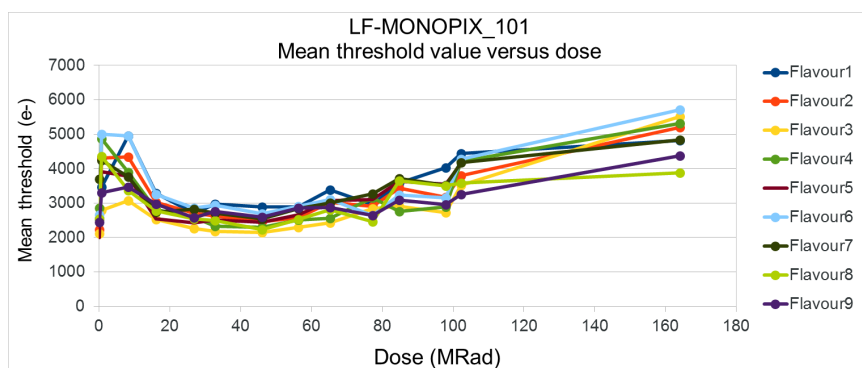


Figure 5.55. – The threshold mean value of LF-MONOPIX1_101 as a function of dose

annealing. A simple injection scan was performed with a constant global TH (0.845 V) at 10 °C. The resulting histogram is shown in Figure 5.60a. Tuning was then attempted for this pixel flavor. The blue histogram in Figure 5.60a shows the threshold dispersion after tuning, but only 39% pixels can be tuned to the target threshold value (4200 e-). The tuning procedure was also tried at low

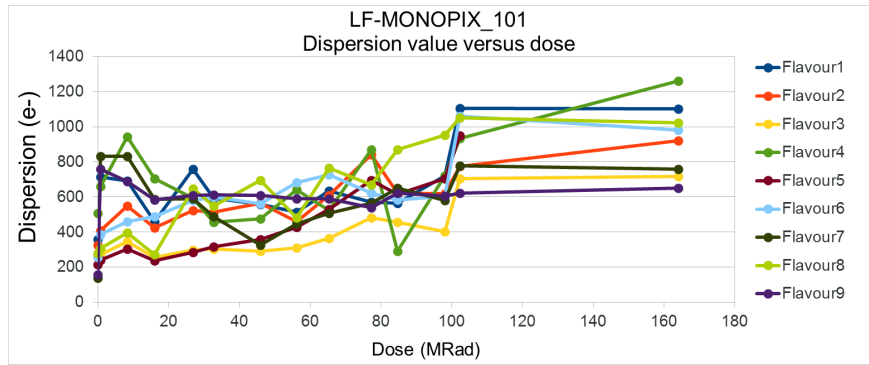


Figure 5.56. – The threshold dispersion of LF-MONOPIX1_101 as a function of dose

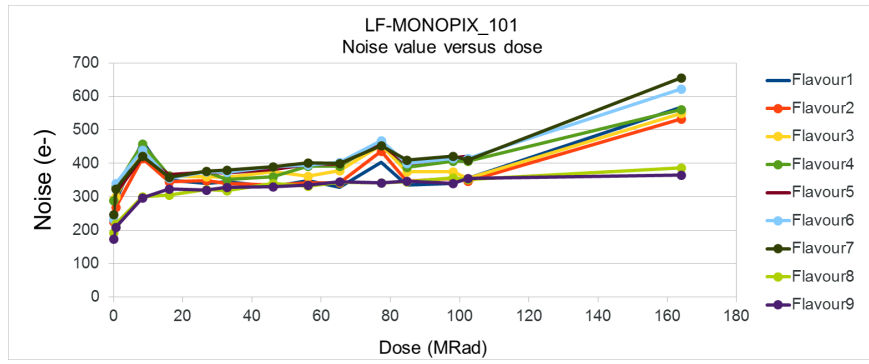


Figure 5.57. – The noise of LF-MONOPIX1_101 as a function of dose

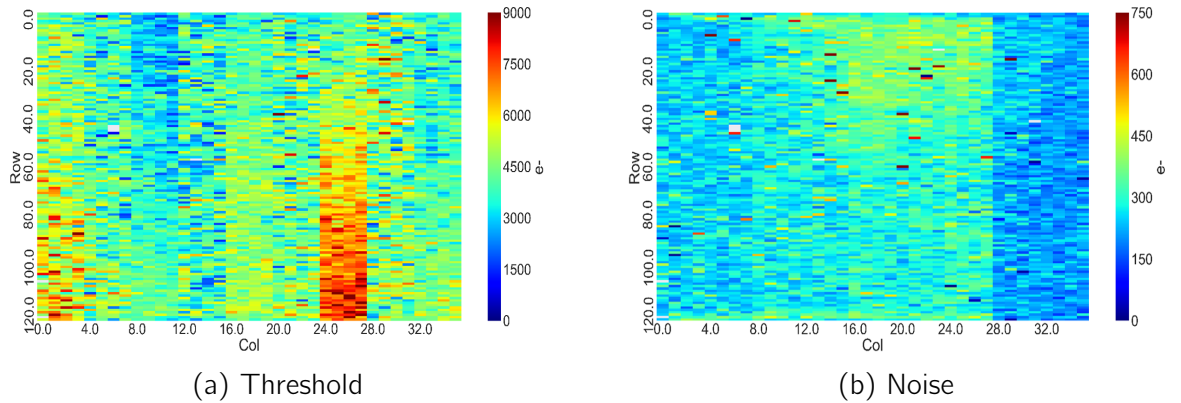


Figure 5.58. – The threshold and noise map of LF-MONOPIX1_100 after radiation at -22 °C.

temperature (-22 °C), but no improvement can be seen in Figure 5.61, still only 32% pixels can be tuned.

In order to investigate the problem, threshold values of one column in Flavor8 before and after tuning are shown in Figure 5.62. The threshold after tuning

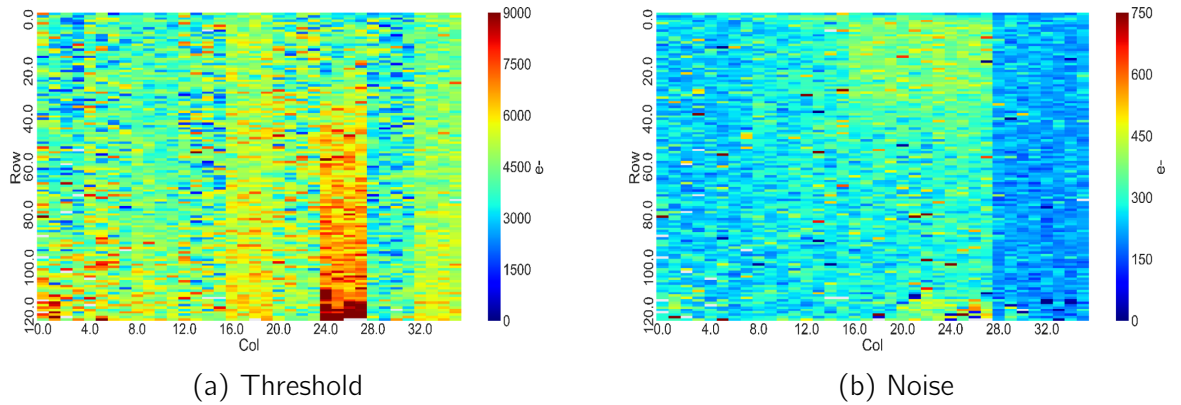


Figure 5.59. – The threshold and noise map of LF-MONOPIX1_101 after radiation at -22 °C.

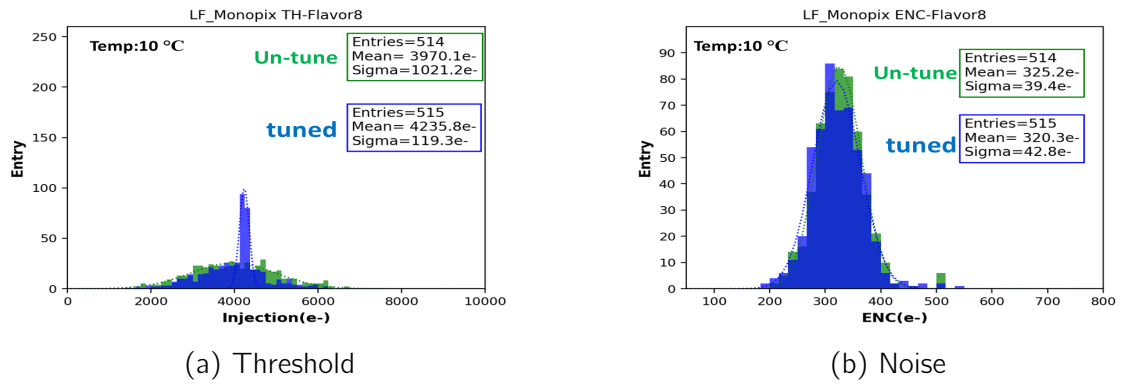


Figure 5.60. – The threshold and noise histogram of Flavor8 in LF-MONOPIX1_101 after radiation at 10 °C.

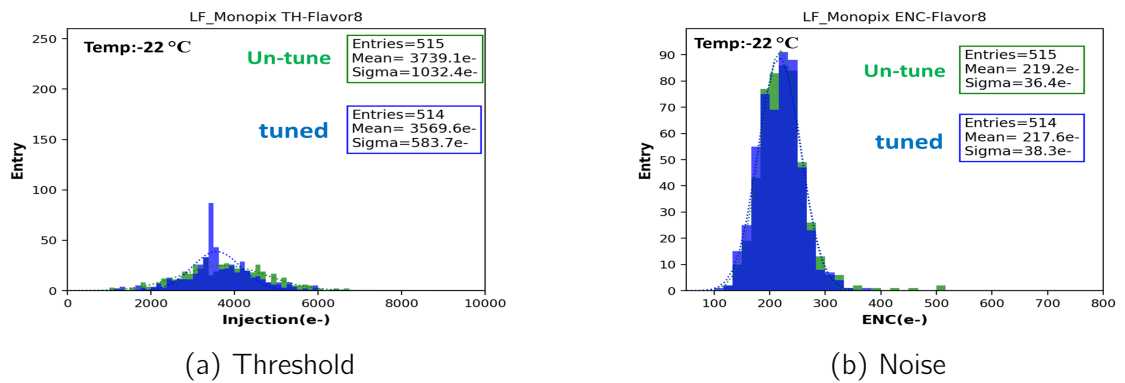


Figure 5.61. – The threshold and noise histogram of Flavor8 in LF-MONOPIX1_101 after radiation at -22 °C.

can be tuned a little bit but still far from the target value, only the threshold before tuning near the target value can be tuned correctly. It seems that the LF-MONOPIX1 shows some degradation on the range of the tunable function of pixels dispersion after 164 MRad radiation.

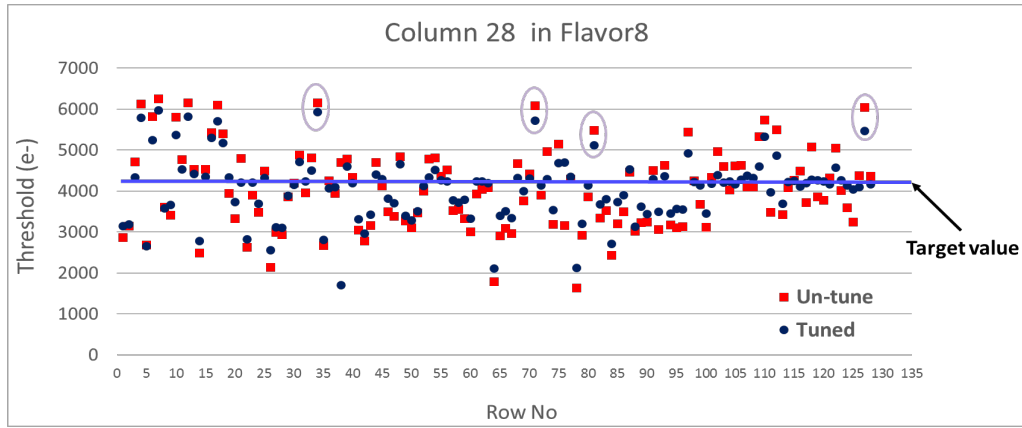
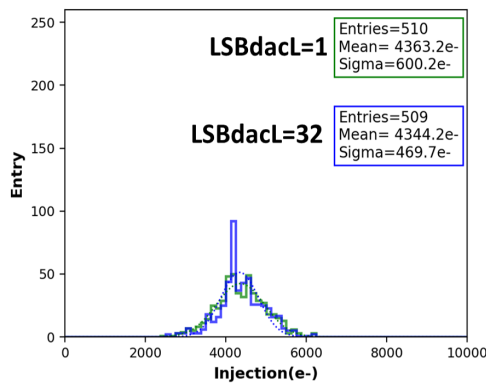
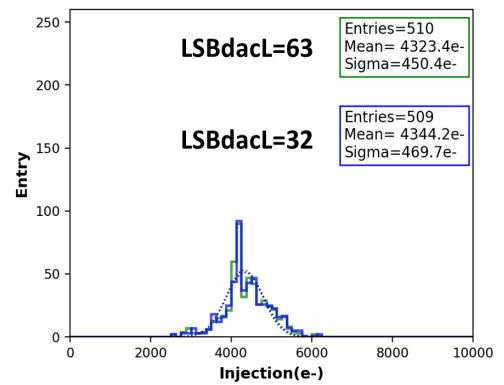


Figure 5.62. – Variation of threshold values before and after tuning

In order to mitigate the degradation of tuning ability, the tuning scan was also implemented at different LSBdacL values which is the equivalent value of the polarization parameter for the LSB (Least Significant Bit) value for the TDAC (Local Pixel Threshold DAC). There was no improvement by decreasing the LSB-dacL value from 32 (default value) to 1, as shown in Figure 5.63a. This problem was also not mitigated by increasing LSBdacL value to 63 (maximum value), as shown in Figure 5.63b.



(a) LSBdacL=1 and LSBdacL=32



(b) LSBdacL=32 and LSBdacL=63

Figure 5.63. – The threshold histogram of Flavor8 at different LSBdacL values after radiation (12 °C).

To understand the source of this problem, the voltage and current reference (PBIAS) versus the temperature before and after radiation were studied. The

pixels are polarized and tuned by a Global Bias Generator which has fourteen 6-bit DAC blocks (see in Table 5.1) and each block has a common current reference. This current reference is simply made by a diode and a 127 k Ω resistor, as shown in Figure 5.64. The current that flows through the diode is the current reference, and the PBIAS value is the voltage equivalent value. The simulation of PBIAS voltage reference as a function of temperature is shown in Figure 5.65. With the temperature increasing, PBIAS voltage reference shows positive linear relationship. The measurement results (green dots) show difference from simulation (blue line) in typical case with the design resistance (127 k Ω) before radiation, but match very well with the resistance at 100 k Ω (green line). It's probably because the R value shifted due to resistance fluctuation from the chip fabrication procedure. The values of PBIAS voltage reference (red dots) dropped after 164 MRad radiation, and close to the simulation result (red line) in worse case with the resistance at 100 k Ω .

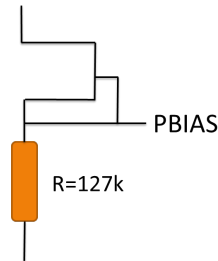


Figure 5.64. – The diagram of current reference circuit

The simulation of current reference (PBIAS) as a function of temperature is shown in Figure 5.66. The simulation in the worse case with 100 k Ω resistor can be considered as the behavior after radiation, since the simulation of PBIAS voltage reference is close to the measurement results in this case. From simulation, the current reference after radiation (red line) is around -20% (from 8.47 μ A to 6.49 μ A) difference from the design value at 10 $^{\circ}$ C, and comes to 30% (from 7.69 μ A to 5.84 μ A) difference. This significant difference of PBIAS current reference may be the reason for the degradation of the tuning function block, but need more investigation and simulation.

Conclusion

LF-MONOPIX1 have been produced in the LFoundry 150 nm process. Before irradiation, the chip was a fully operational sensor with a column-drain readout architecture. The chip shows a breakdown voltage below -280 V and an injection capacitance around 2.5 fF. The Time-Over-Threshold response can be calibrated to get spectroscopic information for characterization. The pixel implementations flavors with V1 discriminator show smaller threshold dispersion, however the tuned threshold distribution for all 9 flavors have a dispersion less than 100 e-.

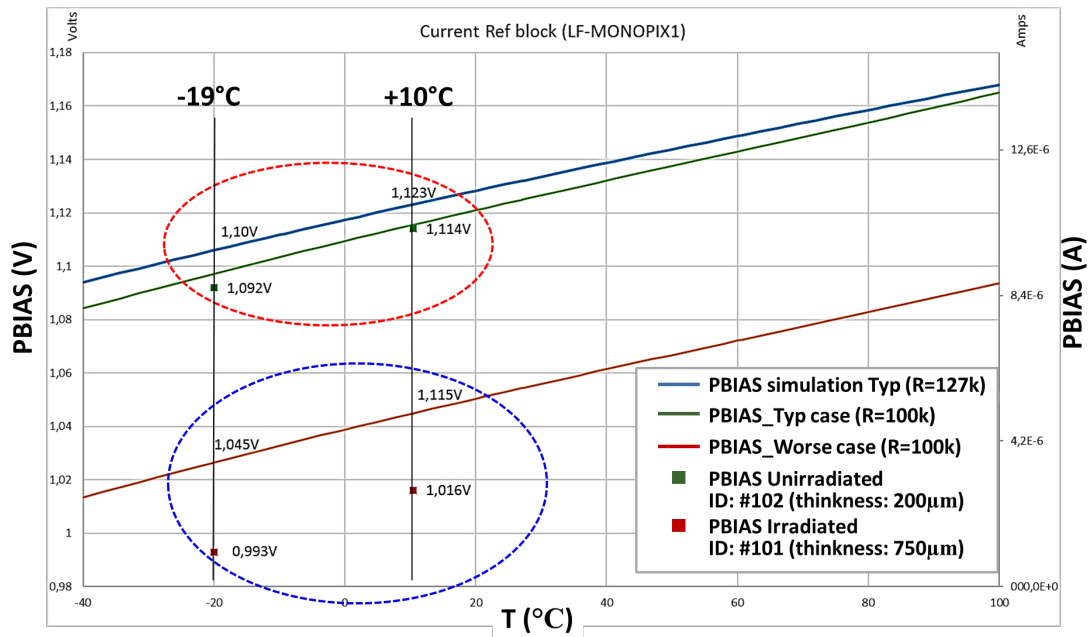


Figure 5.65. – The simulation of PBIAS voltage reference as a function of temperature compared to measurement results

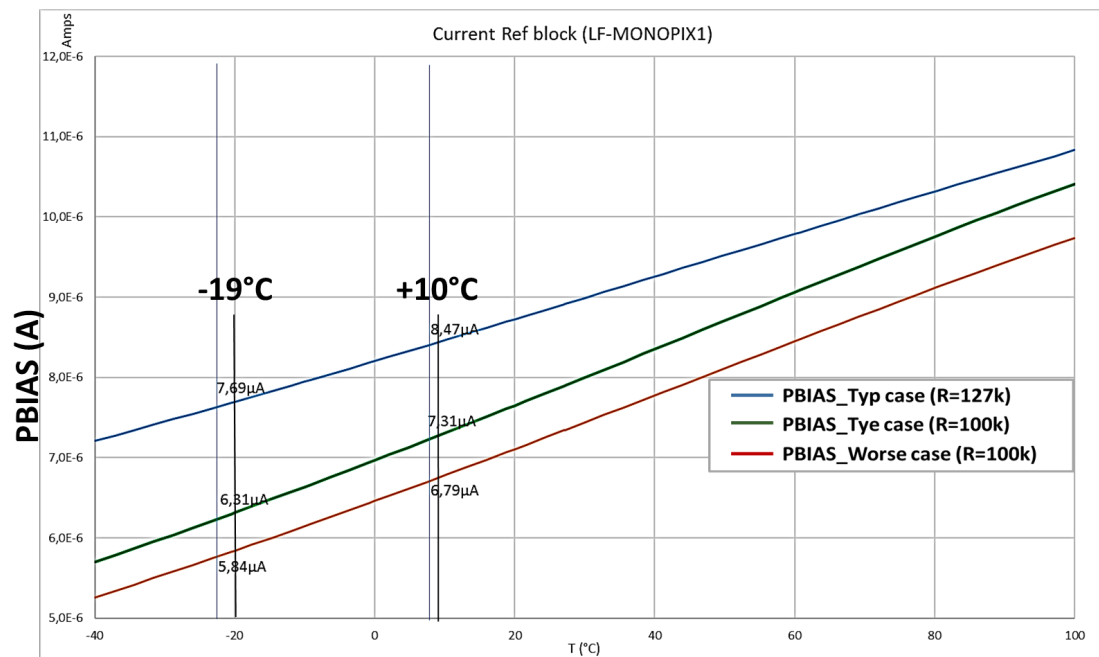


Figure 5.66. – The simulation of PBIAS current reference as a function of temperature

The noise of the flavors with NMOS input transistor are smaller than the noise of the CMOS ones, and the noise for different flavors lies within 180-280 e-.

The prototypes have been irradiated TID over 150 MRad and $\text{NIEL} > 3.6 \times 10^{15} \text{ } n_{eq} \cdot \text{cm}^{-2}$ at the 24 GeV Proton Synchrotron beam in CERN. After the highest irradiation dose, the leakage current at -100 V was well below the HL-LHC design requirement (10 nA/pixel). The chips were still functional till the end of the irradiation campaign. There is nevertheless an evidence of coupling between analog output and the "READ" signal, which can be solved by delaying the digital signals in the firmware. The degradation on the tuning function block can be seen in some prototype after 164 MRad radiation. This problem comes very likely from the significant difference of PBIAS current reference between simulation and measurement, and this part of the design will be optimized in next submission.

Based on these positive results, a next demonstrator submission is being planned which will study the possibility to reduce the pixel size, improve the analog pixel front-end, assess various readout architecture possibilities, and develop several peripheral blocks needed towards a final IC for use in the ATLAS Pixel detector upgrade or in other applications.

Conclusion and outlook

A new approach towards a pixel module called monolithic CMOS pixel module, which integrate the pixel sensor and readout chip in one entity. In contrast to the traditional hybrid pixel module, the monolithic CMOS technology offers a number of advantages and attracts the attention of the ATLAS ITk pixel community, but it still needs to address a few technical features to demonstrate its integrability in the ITk. In this thesis research work, several prototypes for ITk pixel upgrade have been developed in LFoundry 150 nm CMOS process and detailed characterized in the laboratory (CPPM), as well as in several radiation campaigns under the 24 GeV IRRAD proton facility at CERN.

A first prototype in LFoundry 150 nm CMOS technology called CCPD_LF was designed and showed promising results, such as good pre-amplifier linearity, radiation hardness, etc. Based on the results of CCPD_LF, a larger size demonstrator sensor chip LF_CPIX was developed in 2016. Since CCPD_LF and LF_CPIX prototypes are used to test sensor and analog front-end performance, there is no readout logic implemented in the pixel. The LF_CPIX chip implemented new design of the analog front-ends. The chip and pixel sizes are $10 \times 10 \text{ mm}^2$ and $250 \times 50 \text{ } \mu\text{m}^2$, respectively. Two versions of the LF_CPIX were designed, V1 has the same guard-ring strategy as CCPD_LF. In order to increase the reverse breakdown voltage of the chip as well as to reduce the inactive region, the V2 guard-ring strategy of LF_CPIX was optimized, following detailed TCAD simulation. The breakdown voltage of V2 is around -230 V at room temperature, 77% improved breakdown voltage is achieved compared to V1. The measurements in the laboratory at CPPM before irradiation are in agreement with the simulation in terms of analog outputs of the pre-amplifier. As expected from the design changes that were implemented, reduced threshold dispersion (un-tuned) and noise are observed with respect to CCPD_LF. A threshold dispersion less than 80 e- after tuning can be recorded. For all flavors implemented, both the pre-amplifier and the discriminator are working up to a TID of 150 MRad and NIEL of $3.42 \times 10^{15} \text{ n}_{eq} \cdot \text{cm}^{-2}$. A limited leakage current increase meet the HL-LHC design requirement (10 nA/pixel) at $T = -17 \text{ }^\circ\text{C}$ in terms of the NIEL effect. Small degradation of the threshold dispersion (un-tuned) and little shifting of the average threshold were observed, and there is no degradation in terms of threshold dispersion after tuning. However, the noise performance degrades a lot after irradiation at room temperature, but this degradation can be mitigated by cooling. The NMOS pixel implementation shows the best noise performance and around 100 e- less degradation than the PMOS and CMOS pixel implementation flavors after radiation at room temperature.

The design of the first fully monolithic prototype in LFoundry technology, LF-

MONOPIX1, follows the development of its two predecessors: CCPD_LF and LF_CPIX. The LF-MONOPIX1 has logic for fast readout, in addition to variants circuitry of the LF_CPIX pixel. Before irradiation, the chip was fully functional with promising results, we read-out and monitor analog and digital signals from a fully operational sensor with a column-drain readout architecture. The chip shows a breakdown voltage excess -280 V, and the injection capacitance around 2.5 fF. The Time-Over-Threshold response can be calibrated to get spectroscopic information for characterization. The pixel implementation with V1 discriminator show smaller threshold dispersion, however the tuned threshold distribution for all 9 flavors have a dispersion around 100 e-. The noise of the flavors with NMOS input transistor are smaller than CMOS ones, and the noise for different flavors lies within 180-280 e-. Some prototypes have been irradiated during two times radiation campaigns up to TID over 150 MRad and NIEL $> 3.0 \times 10^{15} \text{ } n_{eq} \cdot \text{cm}^{-2}$ at the 24 GeV Proton Synchrotron beam in CERN. The leakage current at -100 V was well below the HL-LHC design requirement (10 nA/pixel). The chips were still functional till the end of the radiation campaign. Nevertheless, there is evidence of coupling between analog output and the "READ" signal, which can be solved by delaying the digital signals in the firmware. Some degradation on the tuning function block can be seen in some prototypes after 164 MRad radiation, this problem comes very likely from the significant difference of PBIAS current reference between simulation and measurement, and should be optimized in next submission.

Beyond participating in the study of the depleted monolithic CMOS sensors in LFoundry 150 nm technology, I have also contributed to investigate the radiation hardness of the bandgap voltage reference and temperature sensor blocks located in the chip periphery in TowerJazz 180 nm technology. Bandgap output voltage increased from 0.989 V (0 MRad) to 1.066 V (72 MRad) under the proton beam, only 7.7% variation after 72 MRad irradiation. Regarding the temperature sensor, the output increased from 0.693 V (0 MRad) to 0.729 V (72 MRad), an increase corresponding to about 0.5 mV/MRad. Both bandgap voltage reference and temperature sensor can work properly and generate stable output voltage under radiation up to 72 MRad. Based on TowerJazz bandgap and temperature sensor architecture, a similar design of these two blocks in LFoundry 150 nm technology is going on.

According to these promising results of the prototypes above, a next demonstrator LF-MONOPIX2 submission is being planned at the beginning of 2020, which will continue to optimize the sensor guard ring design and analog pixel front-end, assess various readout architecture possibilities, and also include several peripheral blocks needed towards a final depleted CMOS monolithic chip. In order to increase the granularity to have better track parameter resolution and decrease the sensor capacitance to result in low noise, LF-MONOPIX2 prototype will study the possibility to reduce the pixel size to $50 \times 150 \text{ } \mu\text{m}^2$. More aggressively, $50 \times 50 \text{ } \mu\text{m}^2$ pixel size prototypes will be also designed as the testing

structure. However, the decision was taken at the beginning of this year that the depleted monolithic CMOS sensor will not be used in outermost layer of ITk, this technology could be used in other High Energy Physics (HEP) applications.

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ANNEXES

A. LF-MONOPPIX1 threshold and noise distribution

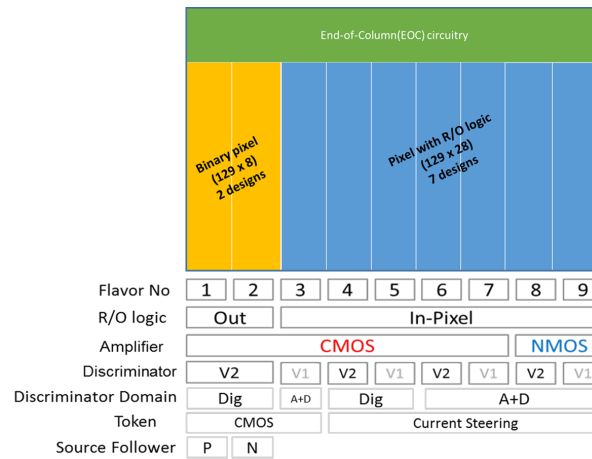
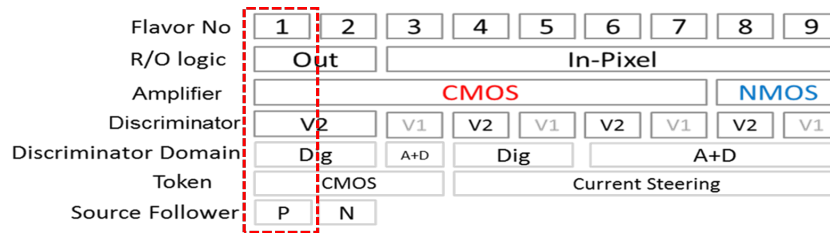
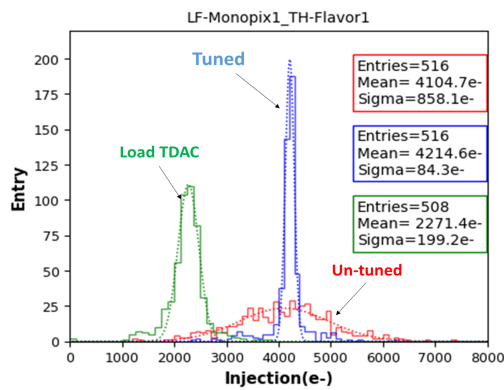


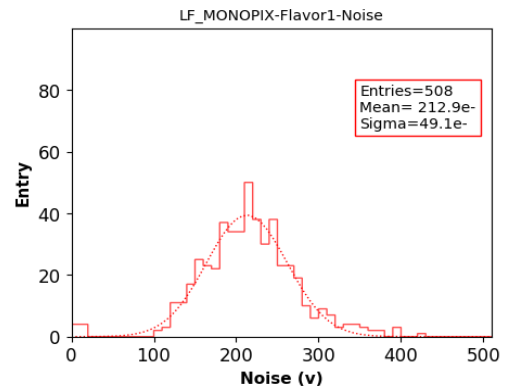
Figure A.1. – The flavor layout of LF-MONOPPIX1.



(a) Flavor1 design information



(b) The threshold distribution

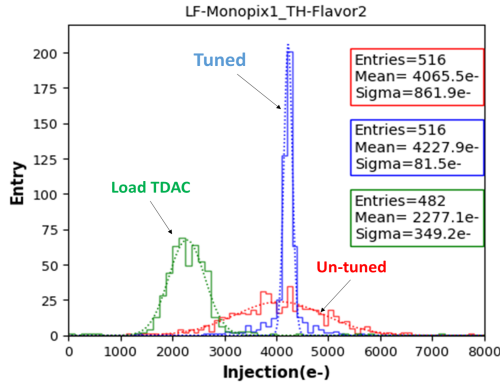


(c) The noise distribution

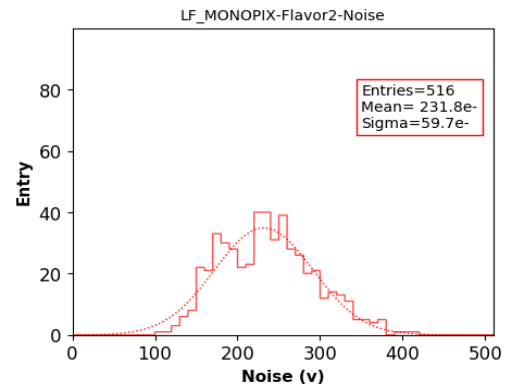
Figure A.2. – Threshold and noise distribution of Flavor1.

Flavor No	1	2	3	4	5	6	7	8	9
R/O logic	Out	In-Pixel							
Amplifier		CMOS						NMOS	
Discriminator	V2	V1	V2	V1	V2	V1	V2	V1	
Discriminator Domain	Dig	A+D	Dig	A+D					
Token		CMOS	Current Steering						
Source Follower	P	N							

(a) Flavor2 design information



(b) The threshold distribution

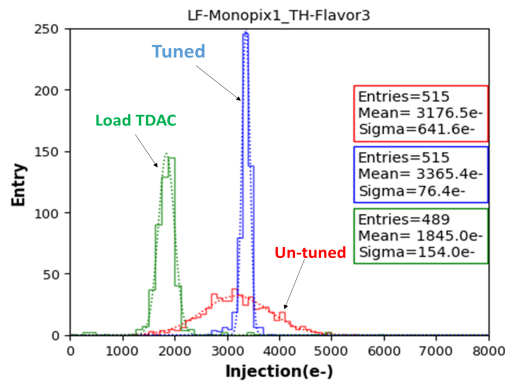


(c) The noise distribution

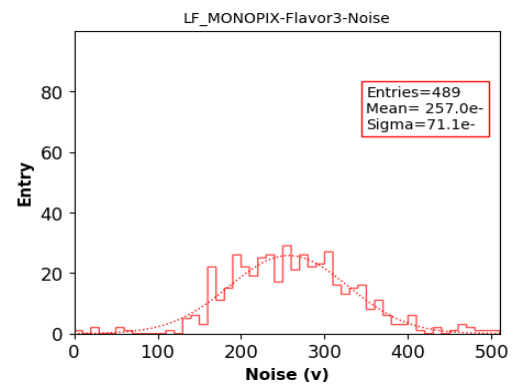
Figure A.3. – Threshold and noise distribution of Flavor2.

Flavor No	1	2	3	4	5	6	7	8	9
R/O logic	Out			In-Pixel					
Amplifier				CMOS					NMOS
Discriminator	V2	V1	V2	V1	V2	V1	V2	V1	
Discriminator Domain	Dig	A+D		Dig		A+D			
Token	CMOS			Current Steering					
Source Follower	P	N							

(a) Flavor3 design information



(b) The threshold distribution

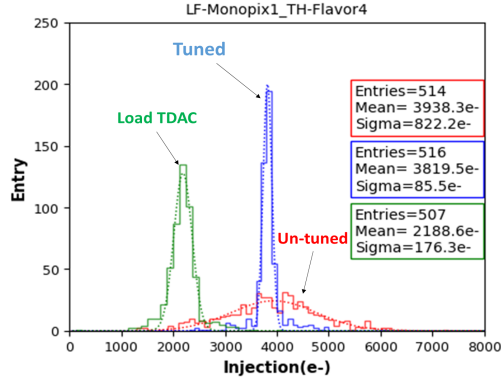


(c) The noise distribution

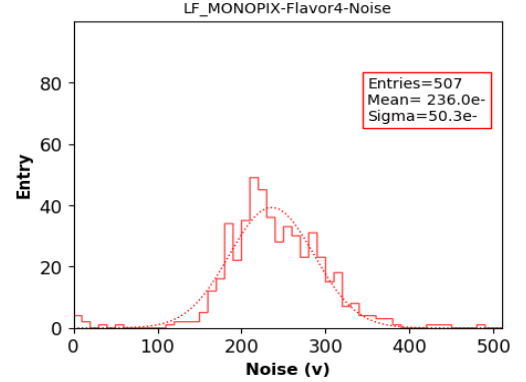
Figure A.4. – Threshold and noise distribution of Flavor3.

Flavor No	1	2	3	4	5	6	7	8	9
R/O logic	Out				In-Pixel				
Amplifier				CMOS				NMOS	
Discriminator	V2	V1	V2	V1	V2	V1	V2	V1	
Discriminator Domain	Dig	A+D	Dig				A+D		
Token	CMOS								Current Steering
Source Follower	P	N							

(a) Flavor4 design information



(b) The threshold distribution

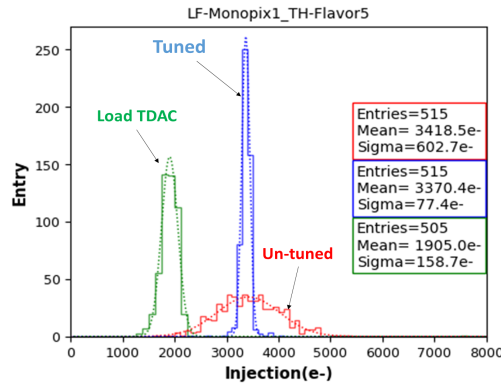


(c) The noise distribution

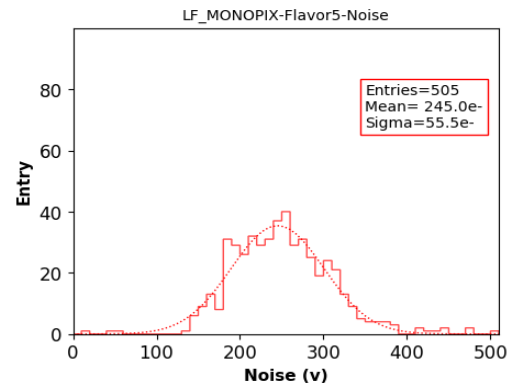
Figure A.5. – Threshold and noise distribution of Flavor4.

Flavor No	1	2	3	4	5	6	7	8	9
R/O logic	Out				In-Pixel				
Amplifier				CMOS				NMOS	
Discriminator	V2	V1	V2	V1	V2	V1	V2	V1	
Discriminator Domain	Dig	A+D	Dig				A+D		
Token	CMOS								Current Steering
Source Follower	P	N							

(a) Flavor5 design information



(b) The threshold distribution

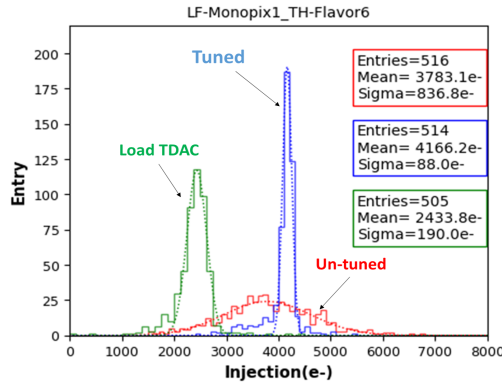


(c) The noise distribution

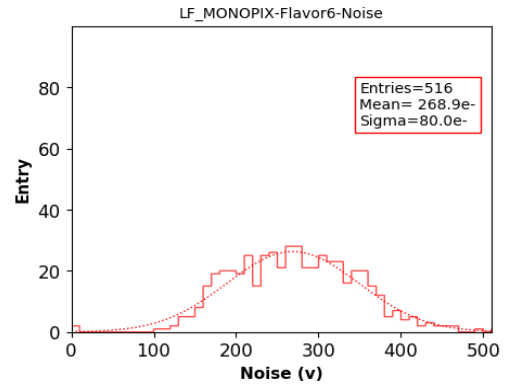
Figure A.6. – Threshold and noise distribution of Flavor5.

Flavor No	1	2	3	4	5	6	7	8	9
R/O logic	Out	In-Pixel							
Amplifier	CMOS						NMOS		
Discriminator	V2	V1	V2	V1	V2	V1	V2	V1	
Discriminator Domain	Dig	A+D	Dig				A+D		
Token	CMOS		Current Steering						
Source Follower	P	N							

(a) Flavor6 design information



(b) The threshold distribution

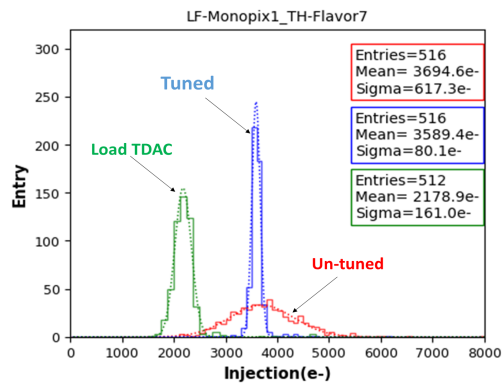


(c) The noise distribution

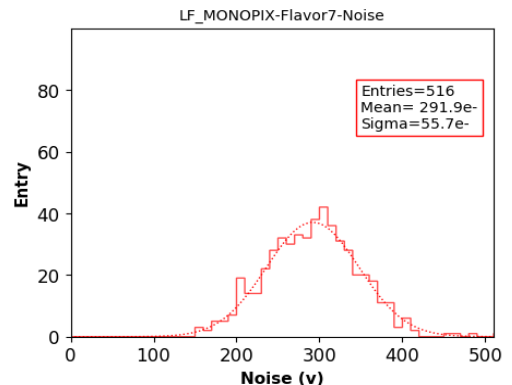
Figure A.7. – Threshold and noise distribution of Flavor6.

Flavor No	1	2	3	4	5	6	7	8	9
R/O logic	Out	In-Pixel							
Amplifier	CMOS						NMOS		
Discriminator	V2	V1	V2	V1	V2	V1	V2	V1	
Discriminator Domain	Dig	A+D	Dig				A+D		
Token	CMOS		Current Steering						
Source Follower	P	N							

(a) Flavor7 design information



(b) The threshold distribution

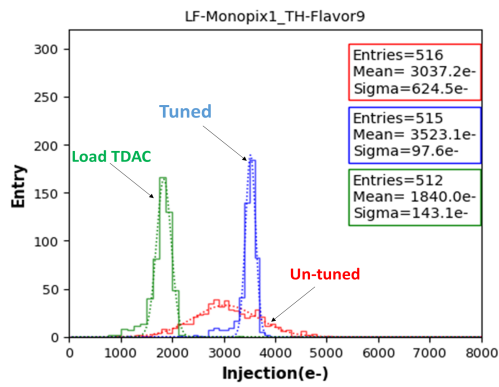


(c) The noise distribution

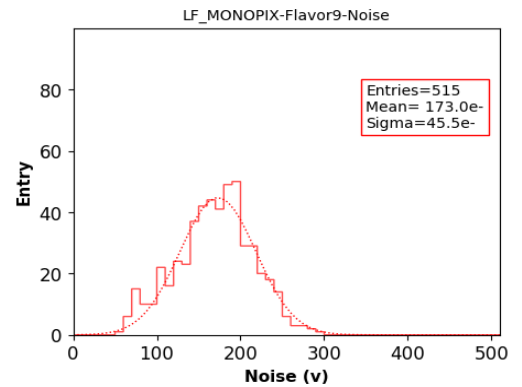
Figure A.8. – Threshold and noise distribution of Flavor7.

Flavor No	1	2	3	4	5	6	7	8	9
R/O logic	Out		In-Pixel						
Amplifier	CMOS							NMOS	
Discriminator	V2	V1	V2	V1	V2	V1	V2	V1	
Discriminator Domain	Dig	A+D	Dig	A+D					
Token	CMOS			Current Steering					
Source Follower	P	N							

(a) Flavor9 design information in the matrix



(b) The threshold distribution



(c) The noise distribution

Figure A.9. – Threshold and noise distribution of Flavor9.