Characterising Silicon Pixel Modules for the Upgrade of the ATLAS Inner Tracker (ITk)

Abbey Barnard* (Lancaster University)
Supervisor: Dr Susanne Kuehn (CERN)

January 2, 2023

Abstract

From 2029, the High-Luminosity Large Hadron Collider (HL-LHC), which is currently under development, will begin running. An increase in the rate of collisions is expected to increase the sensitivity to new and exciting physics. In preparation, some of the LHC detectors are being upgraded to be better suited to taking measurements under the conditions the HL-LHC will create. The ATLAS Inner Detector is being upgraded to an all-silicon Inner Tracker (ITk). Silicon pixel modules (silicon sensors connected to data readout electronics) which form part of the ITk, are being electrically tested at CERN. Electrical testing allows one to measure the production quality of a module, in turn determining its suitability for use in the detector. This short report details the testing procedure for such modules and highlights the importance of running such tests.

1 Introduction

The **ATLAS Inner Detector (ID)** is the first part of the ATLAS detector [1] to detect charged particles that are produced by proton-proton collisions in the Large Hadron Collider (LHC). At present, the ID is composed of three sections: the Pixel Detector, Semiconductor Tracker (SCT) and Transition Radiation Tracker (TRT) [1]. In preparation for the upgrade to High-Luminosity LHC (HL-LHC) and due to radiation damage, the ID is being replaced by an all-silicon **Inner Tracker (ITk)** [2] composed of silicon strip and pixel detectors [3].

Figure 1 shows the different parts of the ITk. The ATLAS ITk Pixel group at CERN works on the Pixel Outer Barrel (OB). This will comprise 4472 modules, with the whole ITk containing around 10,000. The entire detector is designed to withstand the harsher conditions that the HL-LHC brings and improve precision measurements [4].

Silicon sensors and readout electronics, and other components form silicon pixel modules. They will be mounted onto carbon fibre structures on which they are supported in the ITk. During the current prototyping phase, different institutes worldwide are manufacturing pixel modules sent to CERN for electrical testing in different stages.

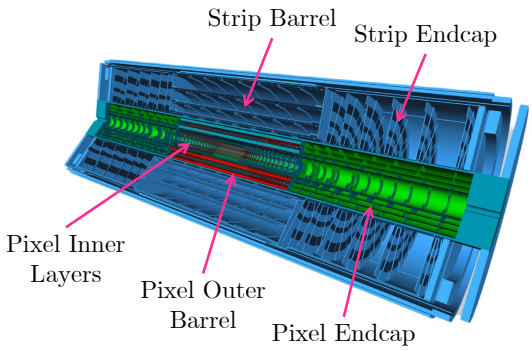

Figure 1: Schematic of the ATLAS ITk showing its different components [3].

These tests provide measurements of the modules' performance over time. During this project, six modules were tested to assess their suitability for use in the OB prototype of the

*a.barnard@lancaster.ac.uk

ATLAS ITk.

2 The ATLAS ITk Silicon Pixel Modules

2.1 Silicon Sensors

Silicon is a semiconducting material used widely in the production of particle detectors. When p-type and n-type doped silicon semiconductors are joined together, they form a p-n junction diode. A reverse bias can create a large depletion zone where charged particles (ionising radiation) can be detected. When travelling through the sensor material, they produce electron-hole pairs that travel to their respective electrodes in the electric field. The signal is detected by the charge-sensitive FE electronics [5].

2.2 RD53A Front-End Chips

The modules tested incorporated RD53A FEs, developed by the RD53 Collaboration and used by both the ATLAS and CMS experiments. They digitise the signal coming from the silicon sensors. The Yet Another Rapid Readout (YARR) software and hardware were used for testing [6]. Each FE is made up of three different analogue FE designs: synchronous (syn), linear (lin), and differential (diff) [7]. This is only the case so that they can be tested to see which design is the most suitable for each experiment, with ATLAS opting to use the diff analogue design. When testing modules, each FE could be controlled and tested separately, and each analogue FE was tested separately[1].

2.3 Module Design

As briefly described in Section 1, a silicon pixel module is a combination of a silicon sensor in the form of pixels and readout electronics (commonly known as Front-End Readout Chips (FEs)). Each module has thousands of pixels, individually bump-bonded to one of the four FEs (a quad module). This allows for charge conduction between the two components, and pixels offer a higher spatial resolution.

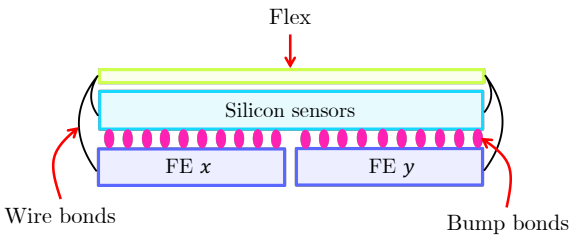

Figure 2: Schematic showing the cross-section of a four quad RD53A pixel module.

Figure 2 shows a module schematic. The flex is glued on top of the silicon sensor and is wire bonded to those and the FEs. It houses some electronics of the module (including the power and readout cables[2]) and protects the sensors.

3 The Electrical Testing Procedure

It is essential that the modules used in the ATLAS ITk work reliably, precisely and accurately to detect charged particles. Electrical testing allows modules to undergo 'quality control' at different stages, from when they're received at CERN (Reception Testing) to when they are in their final configuration in the detector (After Installation).

Using climate chambers, one can simulate temperature conditions similar to those the modules will experience in the LHC. They're used to cool the FE and sensor in operation below -10°C. Electrical testing was carried out in two different experimental setups, the climate chamber and x-ray setups.

3.1 Climate Chamber Setup

Using the climate chamber, one could change and monitor the conditions of modules placed inside. Figure 3 shows the climate chamber workstation. The temperature of the climate chamber was changed on the climate chamber itself and monitored using Grafana and the command line. The module's high and low-voltage power supply was controlled and monitored using the command line. The power supply at the

[1] Some tests allowed for the lin and diff components to be tested together.
[2] These are referred to as pigtails and will be discussed further in later sections.

workstation also displayed the leakage current and low voltage values.

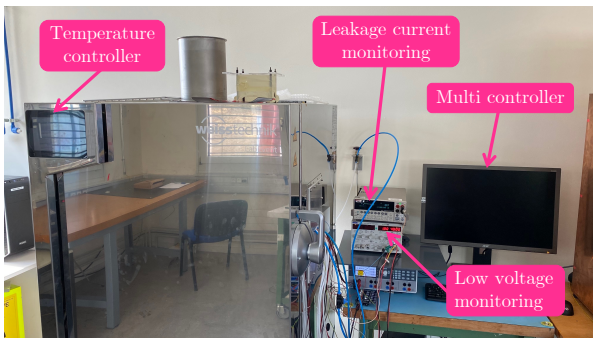

Figure 3: Climate chamber workstation showing the climate chamber on the left with monitoring and control equipment on the right.

Figure 4 shows the inside of the climate chamber, with one of the thick[3] modules connected. The two pigtails (mentioned previously in Section 2.3 connect the modules to the power supply and readout board.

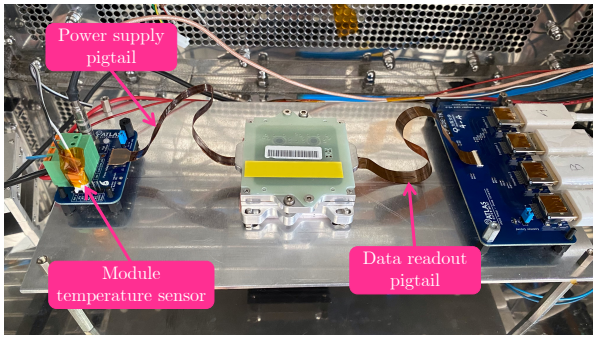

Figure 4: Inside the climate chamber. The module is connected to its power supply on the left and readout board on the right by two pigtails.

3.2 X-ray Setup

Figure 5 shows the x-ray setup. The module's temperature was controlled by a chiller and monitored using Grafana and the command line. Similarly to the climate chamber setup, the high and low voltage power supply was controlled and monitored using the command line, with monitoring for the leakage current and low voltage also visible on the power supply itself.

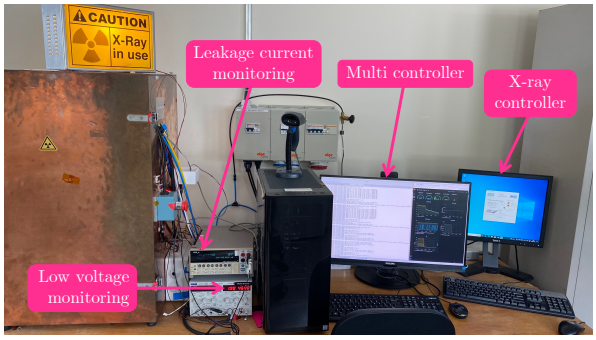

Figure 5: X-ray workstation. The chiller, which controls the temperature of the setup, is off-camera to the bottom right.

Figure 6 shows a thick module connected inside the x-ray setup. The module is simultaneously connected to the power supply and data readout board in both forms. Inside the x-ray setup, an x-ray source controlled by a separate PC (seen in Figure 5) is positioned above where the module is fixed.

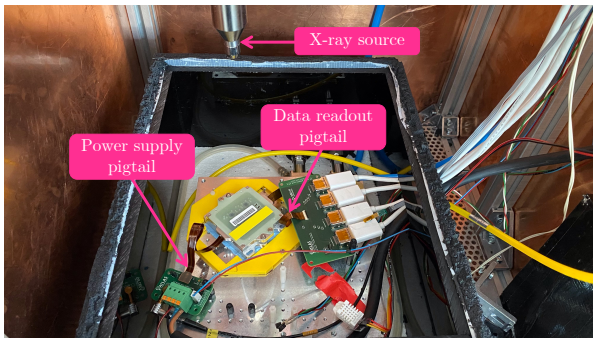

Figure 6: Inside the x-ray setup. The module is connected in the same way shown in Figure 4. The x-ray source is positioned above the module, and foam covers are placed over the black box shown when operating.

3.3 Running Scans

During testing, the module's temperature needed to be kept below 40°C so as not to damage any components. The temperature at which the scans were conducted (excluding IV scans) was approximately 28°C. The IV scans were performed at a lower temperature of roughly 15°C. The IV scan was used to find the high operating voltage if no value was provided on the reception.

The procedure for running scans was almost identical for both setups. The chronology of

[3]Thick modules, compared to standard modules, are characterised by their thicker FEs.

tests was as follows:

1. Digital scan
2. AnaloTherefore, the scan
3. Threshold scan
4. Time-over-threshold scan
5. Crosstalk scan
6. Disconnected bump scan
7. Noise scan
8. Source scan (in x-ray setup only)
9. Forward bias
10. IV curve

The scans were all conducted using command line prompts, with the general case shown below.

```
source <path>/<scan executable>
<path>/<controller type> <module
config directory>/<connectivity file>
```

It includes elements such as the scan executable (different for each scan being run), the controller type (either 4x3 or 16x1, depending on the module) and the connectivity file (allowing us to connect to and control the four FEs). In some cases, no connectivity files for some modules were sent, meaning they had to be made up using pre-existing files.

Once the scans had run, the output was checked to ensure that plots were produced (an indication of whether they ran correctly) and then transferred all the data to EOS (a data storage space used by CERN). Once on EOS, the data could be plotted using bespoke Python scripts, which allowed us to compare data from the different testing stages of each module.

4 Results

4.1 Disconnected Bump-Bond Scan

A good way of analysing how well the pixels and FE pads are connected is by running a **disconnected bump-bond scan** (disc-bump scan). As mentioned in Section 2, each silicon pixel is individually bump-bonded to the FE. The solder alloy (PbSn) thermally expands and contracts when exposed to varying temperatures (a definite scenario in the LHC) and can break as a result. Also, the bump bonds cannot be correctly made in production, and it is essential to assess the impact of this. Disconnected bump bonds lead to the charge being unable to pass through from the sensor to the FE; hence no particle is detected in this region.

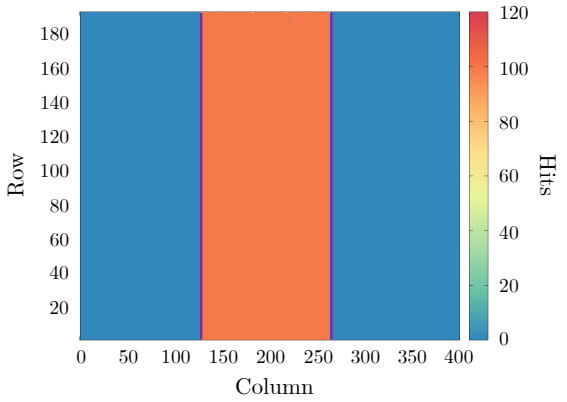

Figure 7: Occupancy map for a lin disc-bump scan on FE1 for Module X, showing mostly connected bump bonds. The lin region is within the purple lines.

Figures 7 and 8 show occupancy maps for two modules, Module X and Module Y, when running a disc bump scan. Both tests were conducted in the x-ray setup and showed results for the lin analogue on the first FE. Figure 7 demonstrates results from a good lin analogue, with very few disconnected bump-bonds (blue pixels within the region between the purple lines). It's important to note that the blue areas on either side of the central part are masked pixels which weren't being tested during this scan.

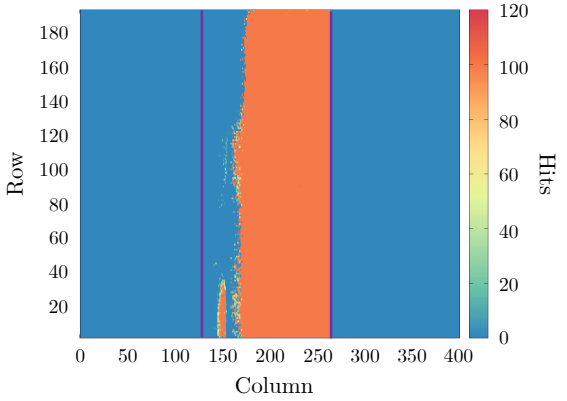

Figure 8: Occupancy map for a lin disc bump scan on FE1 for Module Y, showing a large region of disconnected bump bonds. The lin region is within the purple lines.

The occupancy map for Module Y shows many disconnected bump bonds on the left-hand side within the two purple lines. This can be seen as the blue pixels, which weren't registering hits. This result may be caused by the module being damaged in transit or damage from the thermal expansion/contraction of the bump bonds.

5 Conclusion

This project focused on testing six ATLAS pixel modules to assess their suitability in the ITk. Results presented show an example of both a suitable and an unsuitable module, which can be seen in Figures 7 and 8 respectively. Future work to improve these results includes repeating measurements and testing the modules in their later stages.

Acknowledgements

My most enormous thank you goes to Susanne for taking me on as a summer student two weeks into my stay at CERN and for her thorough supervision of my project. Thank you to the whole Summer Student Team (especially Adriana, Hannah and James) for supporting me during my stay and making the entire experience possible. A huge thank you to Andy Blake, for whom I couldn't have done it without.

References

[1] *ATLAS inner detector: Technical Design Report, 1*, Technical design report. ATLAS (CERN, Geneva, 1997).

[2] *Technical Design Report for the ATLAS Inner Tracker Pixel Detector*, tech. rep. (CERN, Geneva, Sept. 2017).

[3] S. Kuehn (ATLAS Collaboration), "The Upgrade of the Inner Tracker of the ATLAS experiment for the High-Luminosity LHC", (2019).

[4] S.-C. Hsu (ATLAS Collaboration), "ATLAS ITK Upgrade Project", (2018).

[5] G. F. Knoll, *Radiation detection and measurement* (John Wiley & Sons, 2010).

[6] T. Heim, "Yarr-a pcie based readout concept for current and future atlas pixel modules", in Journal of physics: conference series, Vol. 898, 3 (IOP Publishing, 2017), p. 032053.

[7] A. Dimitrievska and A. Stiller (RD53), "RD53A: A large-scale prototype chip for the phase II upgrade in the serially powered HL-LHC pixel detectors", Nucl. Instrum. Methods Phys. Res., A **958**, 162091. 4 p (2020).