

Roberto Russo

Towards a new generation of Monolithic Active Pixel Sensors for LHC experiments

Performance and
precision time measurements

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UNIVERSITEIT
VAN AMSTERDAM



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Towards a new generation of Monolithic Active Pixel Sensors for LHC experiments

Performance and precision time measurements

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Faculteit der Natuurwetenschappen, Wiskunde en Informatica

*“What’s there to be happy about? Job’s not finished.
Is job finished? I don’t think so.”*

Kobe Bryant, post game interview - NBA Finals Game 2, June 7 2009

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Introduction

ACCCELERATORS are machines that accelerate charged particles like protons, heavy ions or electrons to high energy. The development of nuclear and particle physics largely depends on such machines, as they allow to accelerate and collide particles under controlled conditions. Particle interactions are studied with the aid of radiation detectors - large constructions combining several layers of measuring devices, each designed to look for particular properties, such as the direction of emitted particles, their momenta or energy and in some cases their velocity, or specific types of particles.

At CERN, the Large Hadron Collider [1] accelerates and collides protons and heavy nuclei to test the Standard Model of particle physics. Among the four detectors built around the collision points, the ALICE experiment [2] is dedicated to the study of heavy ion physics. To do so, collision products have to be detected and the events that took place have to be precisely reconstructed.

The Large Hadron Collider will undergo an upgrade with the goal of increasing the collision rate. The future High-Luminosity Large Hadron Collider [3] will open the way to the study of new processes for the ALICE experiment, however, the increased number of collisions will pose, at the same time, new challenges to the detector. In particular, the spatial resolution achieved by the current detector will not be sufficient to distinguish collisions from one another. Therefore, a new generation of sensors capable of achieving an improved position resolution and coping with the radiation damage related to the increased collision rate will be needed. Moreover, the addition of time resolving power to the spatial measurement of the collision products will be required to extend the particle identification capabilities and, possibly, to facilitate the reconstruction of the particle trajectories. The study of monolithic active pixel sensors able to accomplish the challenging task of combining high-precision measurement of time and position for experiments taking place at the Large Hadron Collider, and even beyond, is the subject of this work.

The motivations behind the research presented in this dissertation and the context within it has been carried out are discussed in Chapter 1. After having introduced the fundamental concepts of track and vertex reconstruction, and the reasons to add time resolving power to tracker and vertex detectors, the ALICE tracking detector upgrades planned for the High-Luminosity Large Hadron Collider runs are outlined. The main physics goals of the experiment and the requirements for the silicon pixel sensors to be able to achieve them are specified.

Chapter 2 provides a synthetic treatment of silicon physics and properties, and outlines the basis of silicon detectors. The concepts exposed in this chapter will be then used in the rest of the dissertation.

The operation principles of monolithic active pixel sensors (MAPS) are described in Chapter 3. Being based on commercial CMOS technologies [4], the MAPS devices employed today as High-Energy Physics detectors directly descend from imaging sensors. Their properties of low noise and low material, besides the possibility they offer of building large area detectors with relatively reduced costs, make them the instrument of choice for the ALICE experiment. In particular, the test structures belonging to the first chip submission implementing the 65 nm CMOS technology for particle physics applications, developed within the ALICE ITS3 project and under the umbrella of CERN's Experimental Physics Research and Development (EP R&D) department [5], are introduced.

Chapter 4 introduces the Analog Pixel Test Structure Operational Amplifier (APTS-OA). It is a prototype designed with the specific goal of studying the charge collection and time resolution properties of pixel sensors based on the 65 nm CMOS process. The experimental setups developed to carry out the characterization campaign of such prototypes, as well as the measurements with test pulses and X-rays emitted by a ^{55}Fe radioactive source, are discussed.

Chapter 5 contains a published paper [6] on the characterization of the APTS-OA sensors with a minimum ionizing charged particle beam. In this study, a prominent role is taken by the evaluation of the time resolution of the measured samples. This measurement outlines the potential of the 65 nm CMOS technology for fast timing applications and allows a direct comparison with other monolithic pixel sensors based on the 180 nm CMOS technology. The performance of the measured devices in terms of detection efficiency and spatial resolution is also studied.

Chapter 6 illustrates the development of a simulation study to model the behavior of silicon pixel sensors based on the 65 nm CMOS process. The approach consists in the combination of three-dimensional Technology Computer Aided Design (TCAD) simulations [7], describing the semiconductor device, with Monte Carlo simulations,

reproducing the interaction of radiation with the detector, the charge propagation within the detector volume, the signal induction at the pixel's electrode, and, additionally, the effects of the pixel front-end on the voltage signal. The Monte Carlo simulation is based on the Allpix² framework [8]. The goal is to develop a tool that, whilst retaining a certain degree of independence from the technological details of the CMOS process, can describe with satisfying precision the behavior of the devices. Being the CMOS process featured by the simulated prototypes a commercial one, it is property of the foundry, and therefore its details are not accessible. The simulations are validated via comparison with the experimental results discussed in Chapter 4 and Chapter 5.

Chapter 7 comprises a published paper [9] introducing a second pixel matrix prototype based on the 65 nm CMOS technology, the Digital Pixel Test Structure (DPTS). Differently than the APTS-OA, the DPTS chip includes a novel in-pixel front-end architecture and a digital readout scheme, and is developed with the aim of studying larger pixel matrices. Its goal is then the study of the performance of the full readout chain, in addition to the evaluation of the 65 nm CMOS process. The paper presents the laboratory characterization of the device together with the measurements performed with minimum ionizing particle beam. The radiation hardness of the test structures is validated against the ALICE requirements, and the effect of a relatively low power consumption operation regime of the in-pixel front-end on the sensor's time resolution is studied.

The results presented in this thesis demonstrate the feasibility and the adequacy of monolithic active pixel sensors based on the 65 nm CMOS process for the construction of a vertex detector operating in future collider experiments. The studied test structures proof high detection efficiency and spatial resolution, also after having sustained a significant radiation damage, and appear as promising candidates for the integration of high-precision timing capabilities in particle tracking.

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Publications

Chapter 5: G. Aglieri Rinella, R. Russo et al., *Time performance of Analog Pixel Test Structures with in-chip operational amplifier implemented in 65 nm CMOS imaging process*, Nuclear Instruments and Methods in Physics Research Section A, 1070 (2025), 170034.

R. Russo participated in the beam test campaign discussed in the publication, contributed to the development of the data acquisition software, and was responsible for the time resolution analysis leading to the results presented in the paragraph *Time resolution* of Section 5.3.3. He wrote the text contained in paragraph *Time resolution analysis* of Section 5.3.2, paragraph *Time resolution* of Section 5.3.3 and Section 5.4 of the original draft, and contributed to the review and editing of the manuscript. He produced Figure 5.5, Figure 5.10, Figure 5.11, Figure 5.12, Figure 5.13, Figure 5.14, Figure 5.15, Figure E.1, and Figure H.1.

Chapter 7: G. Aglieri Rinella, R. Russo et al., *Digital pixel test structures implemented in a 65 nm CMOS process*, Nuclear Instruments and Methods in Physics Research Section A, 1056 (2023), 168589.

R. Russo participated in the beam test campaign discussed in the publication and contributed to the development of the software for the decoding of the acquired beam test data. He was one of the people responsible for the analysis of data taken to evaluate the radiation hardness of the studies sensors, discussed in Section 7.4.3 and Section 7.4.4, and was responsible for the time resolution studies presented in Section 7.4.5. He wrote the text contained in Section 7.4.2, Section 7.4.4 and Section 7.4.5 of the original draft, and contributed to the review and editing of the manuscript. He produced Figure 7.16a, Figure 7.18a, Figure 7.19, and Figure 7.20.

PART I

Motivation and Context

*“Many years later, as he faced the firing squad,
Colonel Aureliano Buendía was to remember that distant
afternoon when his father took him to discover ice.”*

Gabriel García Márquez, *One Hundred Years of Solitude*

CHAPTER 1

Tracking particles

THE word *pixel*, appearing for the first time in Reference [1], is often used to indicate the smallest distinguishable element in an image. Pixel detectors are devices able to record images, and the size of the pixel typically corresponds to the granularity of the image.

The images considered in this dissertation are generated by relativistic charged particles or photons emerging from particle collisions. Silicon pixel detectors are crucial elements in experimental particle physics, thanks to their capability of coping with increasing interaction rates and energies of modern particle accelerators while guaranteeing excellent detection efficiency and resolution for the tracking of charged particles. Silicon devices, such as *strip detectors* [2, 3] and *drift chambers* [4], have been used for particle tracking and identification since the late 1970s. Silicon pixel detectors have started to supersede these devices since the late 1990s and today are the instrument of choice for particle tracking and vertexing in high rate and high radiation environments.

The research discussed in this thesis focuses on the characterization and development of novel silicon pixel sensors, belonging to the family of monolithic active pixel sensors (MAPS), for High-Energy Physics experiments at the *Large Hadron Collider* (LHC) accelerator [5]. This chapter gives a brief overview of the current LHC complex, and introduces the machine's planned upgrades, by highlighting the challenges that future particle accelerators will pose to silicon pixel detectors.

Among the four experiments running at the LHC ring, the ALICE experiment [6] is brought forward as an example to describe the requirements for the development of new silicon pixel detectors, as the sensor R&D work presented in the following chapters is carried out within the broader context of the ALICE Inner Tracking System upgrade.

1.1 The Large Hadron Collider

The Large Hadron Collider [5], situated at the European Organization for Nuclear Research – *Conseil Européen pour la Recherche Nucléaire* – or CERN, is currently the largest existing particle accelerator. It is a circular collider with a circumference of 27 km and constitutes the last element in the chain of the CERN accelerator complex, as shown in Figure 1.1. The LHC is also the world's highest energy collider, with a beam energy of 6.8 TeV. Protons or heavy ions, such as lead nuclei (Pb^{82+}), are injected into the two counter circulating beams of the LHC, after having been accelerated by the

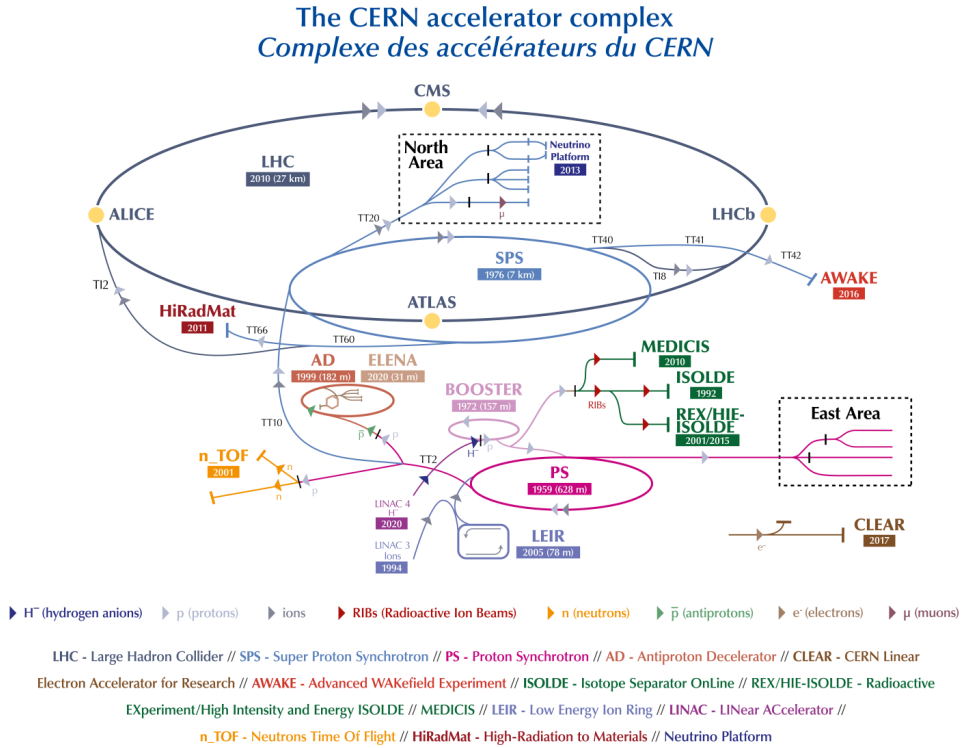


Figure 1.1 Layout of the CERN accelerator complex [7]. It consists of a sequence of machines boosting the energy of a particle beam, before injecting it into the next machine of the sequence. The Large Hadron Collider (LHC) is the last stage of the accelerator complex. In the two beam pipes of the LHC, one beam circulates clockwise and the other counterclockwise, with the particles reaching energies up to 6.8 TeV. The two beams are brought into collision inside four detectors – ALICE, ATLAS, CMS and LHCb – where the total energy at the collision point is up to 13.6 TeV.

previous stages of the accelerator complex. The two parallel beams collide head-on at four interaction points around the ring, with a resulting center-of-mass system energy of 13.6 TeV. Four detectors have been built around the interaction points: ALICE, ATLAS, CMS and LHCb.

Besides the large center-of-mass energy, required to probe new processes, a large number of interactions (events) is needed to collect sufficiently significant data sets for the study of rare events with a small production cross section. The *luminosity* describes the capability of producing a given interaction rate dN/dt for a selected process of cross section σ_p :

$$\frac{dN}{dt} = \mathcal{L} \cdot \sigma_p . \quad (1.1)$$

The factor $\mathcal{L}$ is also referred to as *instantaneous luminosity*, and is expressed in the units of $\text{cm}^{-2}\text{s}^{-1}$. The instantaneous luminosity depends on the number of particles N_1 and N_2 contained in the two colliding bunches¹, on the characteristic transversal surface of the counter circulating beams² A and on the bunch crossing frequency f :

$$\mathcal{L} = \frac{N_1 N_2}{A} \cdot f . \quad (1.2)$$

The number of events of interest N is given by the integral of Equation 1.1:

$$N = \int \mathcal{L}(t) dt \cdot \sigma_p = \mathcal{L}_{\text{int}} \cdot \sigma_p , \quad (1.3)$$

where $\mathcal{L}_{\text{int}}$ represents the integrated luminosity. It constitutes an essential quantity for the design of particle detectors since it is proportional to the amount of collected data. At current LHC's operation conditions, bunches are spaced by 25 ns, i.e. the bunch collision frequency is 40 MHz, and peak luminosities of up to $2.584 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ for proton-proton collisions have been achieved [9]. For design reasons of the experiment, the luminosity registered at the ALICE interaction point is lower than what can be delivered by the machine. Peak values of $8.05 \times 10^{31} \text{ cm}^{-2} \text{ s}^{-1}$ for proton-proton and of $6.421 \times 10^{27} \text{ cm}^{-2} \text{ s}^{-1}$ for ion collisions have been reached at the ALICE interaction point.

¹ The nominal value of protons per bunch at the LHC is 1.2×10^{11} .

² The characteristic collision surface can be expressed in terms of RMS transversal beam sizes σ_x^* and σ_y^* in the horizontal and vertical directions at the interaction point [8]:

$$A = 4\pi \sigma_x^* \sigma_y^* .$$

Since its first test operation in 2008 [10], the LHC has completed two operational run periods, namely Run 1 (2009-2013) and Run 2 (2015-2018), followed by two Long Shutdown periods, from 2013 to 2015 and from 2018 and 2022, respectively, for maintenance and upgrade of the accelerator and the detectors. Since April 2022, the LHC has entered its third operational run period, also known as Run 3.

A third Long Shutdown period is planned from July 2026 to July 2030 (indicatively), when the LHC will be upgraded to the *High-Luminosity Large Hadron Collider* (HL-LHC) [11], with the goals of increasing the peak luminosity to $5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ and the integrated luminosity of a factor ranging from 5 to 7.5 with respect to what has been achieved so far. A fourth Long Shutdown, with a further luminosity increase, is scheduled for December 2033–January 2036, at the end of the Run 4 operational period (2030-2033). The luminosity increase will be achieved by boosting the beam intensity and focusing thanks to more powerful magnets and new beam optics, while the bunch collision frequency will remain unchanged.

The augmented interaction rate targeted by the HL-LHC will pose new challenges for the experiments, especially for the vertex and tracker detectors. They will be required to improve their capability of identifying and distinguishing between primary and decay vertices while enhancing their radiation hardness, namely the property of keeping their performance undiminished despite the damage to the sensor's crystal lattice and to the electronics induced by the enhanced particle fluence to which they will be exposed. An overview of the radiation damage mechanism and its effect on detectors will be given in Section 2.7.

1.2 Fundamental concepts in track and vertex reconstruction

The point where particles are produced in a collision or a decay is called a *vertex*. The collision point of two particles is called *primary vertex*. At the LHC, many collisions can occur in a single bunch crossing; there can be, consequently, many primary vertices. Many rare but interesting particles produced at a primary vertex are unstable and have a short lifetime (of the order of 1 ps), after which they decay into a few daughter particles. The decay point is also known as *secondary vertex*³. In the

³ The decay length L separating the primary from the secondary vertex is:

$$L = \beta c \gamma \tau = \frac{p}{m_0} \tau ,$$

with βc representing the particle speed and γ the Lorentz factor.

As an example, for a particle with rest mass $m_0 = 100 \text{ MeV}/c^2$, momentum $p = 1 \text{ GeV}/c$ and lifetime $\tau = 1 \text{ ps}$, the decay length is equal to 3 mm.

case of a short-lived particle, primary and secondary vertices are typically displaced by few millimeters. For long-lived particles, the secondary vertex can be far from the primary one, and even outside the detector.

The goal of vertex reconstruction is therefore the identification of primary from secondary vertices, the separation of different primary vertices and the estimate of their position. To do so, the tracks emerging from a bunch collision or a decay must be measured as precisely as possible.

Silicon pixel detectors are fundamental tools to precisely reconstruct particle tracks and vertices because of their property of high spatial resolution and granularity. This section aims to provide the basic concepts regarding the relevant detector parameters to achieve the goals described above. A more detailed discussion can be found in specialized literature, such as Reference [12].

The pointing resolution σ_p , namely the spatial uncertainty around the reconstructed vertex position, mainly depends on three aspects:

- the intrinsic spatial resolution of the sensor;
- the extrapolation distance between the measured points and the collision point;
- the multiple scattering between the collision and the measured points due to the beam pipe and the detector material.

The first two factors contribute to the error σ_p^{geo} of the geometrical extrapolation from the measured points along the reconstructed track to the interaction point. For the simple case of the tracking system shown in Figure 1.2, made of two concentric layers of radii r_1 and r_2 , and spatial resolution σ_1 and σ_2 , respectively, the pointing resolution is [13]:

$$(\sigma_p^{geo})^2 \simeq \left(\frac{\sigma_1 r_2}{r_2 - r_1} \right)^2 + \left(\frac{\sigma_2 r_1}{r_2 - r_1} \right)^2 = \frac{1}{(r_2 - r_1)^2} [(\sigma_1 r_2)^2 + (\sigma_2 r_1)^2] . \quad (1.4)$$

Equation 1.4 highlights the importance of high precision at the inner layer, being its resolution weighted by the outer radius. If, for simplicity, the two layers have the same spatial resolution σ , Equation 1.4 can be rewritten as follows:

$$(\sigma_p^{geo})^2 \simeq \sigma^2 \frac{r_2^2 + r_1^2}{(r_2 - r_1)^2} . \quad (1.5)$$

From Equation 1.5 one can see that the impact parameter resolution improves (i.e. decreases) with the decreasing radius of the inner layer, eventually approaching the intrinsic spatial resolution of the sensor for a layer very close to the interaction point.

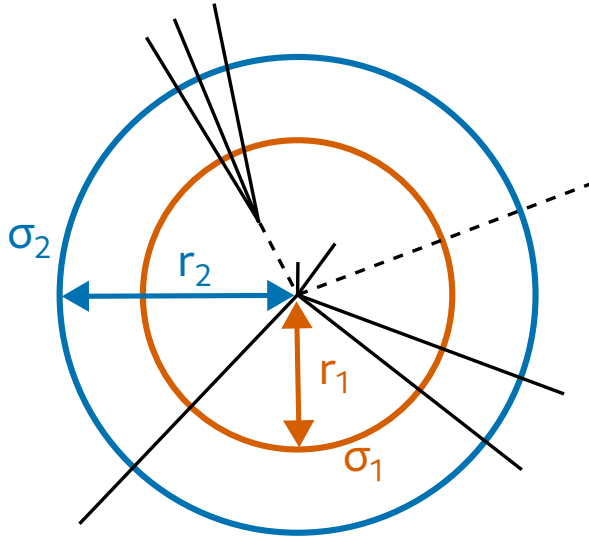


Figure 1.2 Axial view of a vertex detector made of two concentric layers of position-sensitive sensors, with radii r_1 and r_2 , and spatial resolution σ_1 and σ_2 , respectively. For simplicity, the primary vertex coincides with the interaction point. The decay products originate from secondary vertices, which are displaced from the primary one. The detected charged particles are represented with solid lines, while dashed lines represent neutral particles, as they are not detected. The charged particles travel straight paths, as no magnetic field is present in the simple case shown. In a typical vertex detector, a magnet is used to bend the tracks of charged particles. The beam pipe separating the first layer from the interaction point is not depicted.

In general, it is desirable to measure the first point at as small a radius as possible. The third factor affecting the pointing resolution is the angular deflection due to multiple scattering suffered by charged particles traveling through the detector material. The deflection can be attributed to the inelastic collisions with the atomic electrons of the material, but also, although with smaller probability, to the elastic Coulomb scattering from nuclei. The distribution of the angular deflection can roughly be described by a Gaussian distribution with an RMS width θ_0 [14]:

$$\theta_0 = \frac{13.6 \text{ [MeV]}}{\beta c p} z \sqrt{\frac{x}{X_0}} \left[1 + 0.038 \ln \left(\frac{x z^2}{X_0 \beta^2} \right) \right], \quad (1.6)$$

where p , βc and z are the momentum, velocity and charge of the incident particle, and x/X_0 is the thickness of the material expressed as a fraction of the *radiation length* X_0 . The latter is defined as the mean distance that a high energy electron needs to

travel through a material to have its energy reduced by a factor $1/e$ due to radiation loss only. In silicon, it corresponds to a thickness of 9.36 cm. Equation 1.6 describes the scattering due to a single material. In case of multiple layers of different materials, Equation 1.6 should be applied after having found the value of x/X_0 for the combined scatterer [8]. The effect of multiple scattering on the pointing resolution σ_p^{ms} due to the beam pipe and the detector material over the lever arm r_1 , by taking as an example the simple case depicted in Figure 1.2, can be computed from the RMS width of the angular distribution described by Equation 1.6:

$$\left(\sigma_p^{ms}\right)^2 \simeq (r_1\theta_0)^2 = \left(r_1 \frac{13.6 [MeV]}{\beta c p} z \sqrt{\frac{x}{X_0}} \left[1 + 0.038 \ln\left(\frac{xz^2}{X_0\beta^2}\right)\right]\right)^2. \quad (1.7)$$

It is straightforward to deduce from Equation 1.7 that the pointing resolution improves with reduced material and, as for the geometrical term, with reduced lever arm.

The final pointing resolution σ_p can be found by summing in quadrature the two contributions σ_p^{geo} and σ_p^{ms} .

From the simplified treatment presented in this section, it is possible to derive three key design objectives for a vertex detector:

- reducing the pixel size of the position-sensitive sensors for a better intrinsic spatial resolution;
- reducing the distance between the first layer and the interaction point;
- reducing the material of the detector, in particular of the innermost layers.

To the aspects listed above, it should be added that the increase of the number of tracking layers, i.e. the number of measured points of a track, improves the tracking efficiency [15]. However, the reduction of the radii of the first layers exposes them to higher radiation load. Therefore, a trade-off between all of the described design parameters must be found.

To better understand the complexity of track and vertex reconstruction in current LHC experiments, one can consider the example provided by Figure 1.3. It shows an event reconstructed by the ALICE collaboration after a Pb-Pb collision during the LHC Run 3. The levels of particle density and track multiplicity produced after a collision require already extreme tracking and vertexing precision, with the problem becoming increasingly more complex with the luminosity enhancement foreseen after the High-Luminosity LHC upgrade (cf. Section 1.1).

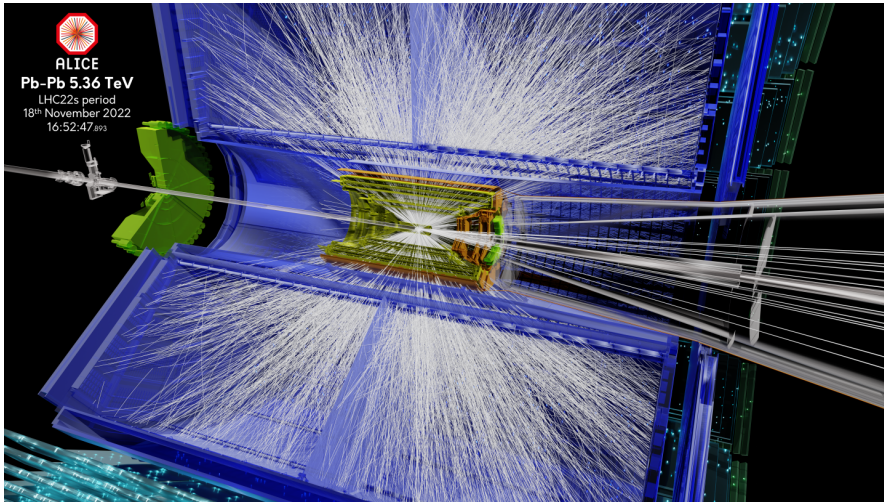


Figure 1.3 Reconstructed event in the ALICE detector after a Pb-Pb collision during the LHC Run 3 [16].

1.3 The need for high-precision time measurements

In many High-Energy Physics experiments, the temporal information is used to perform particle identification via Time-of-Flight (ToF) systems. While the momentum of a charged particle is typically deduced from the bent trajectory it travels in a magnetic field, its velocity can be determined by measuring the time it takes to traverse the distance L separating two detectors. A ToF system therefore consists of two detector layers providing the ‘start’ and ‘stop’ signals for the time measurement.

For two particles of mass m_1 and m_2 , speed v_1 and v_2 , and same momentum p , the time-of-flight difference is:

$$\Delta t = L \left| \frac{1}{v_1} - \frac{1}{v_2} \right| = \frac{L}{c} \left| \frac{1}{\beta_1} - \frac{1}{\beta_2} \right|. \quad (1.8)$$

By using $pc = \beta E$ in Equation 1.8, the mass of the particles can be explicitly written:

$$\Delta t = \frac{L}{pc^2} |E_1 - E_2| = \frac{L}{c} \left| \sqrt{1 + \left(\frac{m_1 c^2}{pc} \right)^2} - \sqrt{1 + \left(\frac{m_2 c^2}{pc} \right)^2} \right|. \quad (1.9)$$

Under the assumption $pc \gg m_{1,2}c^2$, Equation 1.9 can be expanded in:

$$\Delta t = \frac{Lc}{2p^2} |m_1^2 - m_2^2|. \quad (1.10)$$

The separation power of a ToF system is usually expressed in number of standard deviations n_σ of the detector time resolution σ_t . It means that two particles can be separated only if their time-of-flight difference is larger than $n_\sigma\sigma_t$, with n_σ expressing the statistical significance of the separation. It is thus apparent how an enhanced time resolution is desirable to extend the upper momentum limit for particle identification⁴.

The luminosity enhancement targeted by the HL-LHC paves the way to new applications of fast timing sensors in High-Energy Physics experiments, besides their operation in particle identification systems. The increase in collision rate will entail an increase in *pile-up* for the detectors, i.e. an increase in the number of (quasi-) simultaneous collisions (vertices) per bunch crossing taking place at the interaction points⁵.

The methods of track and vertex reconstruction discussed in the previous section are entirely based on the measurement of the spatial coordinates of the collision products. The increase of particle and track density per bunch crossing will add a substantial layer of complexity to the vertex separation operation, as the spatial resolution of the sensors alone will not be sufficient to distinguish among particles in the pile-up conditions mentioned above. New methods will be then required. The addition of the temporal coordinate can help in separating collision events, and at the same time it can facilitate the track reconstruction procedure by reducing the overall number of possible hit combinations among the different tracking layers. Tracking layers combining spatial and temporal particle hit measurement are referred to as *4D layers*. No current experiment operating at the LHC implements a full 4D tracking system, also because the commissioning of such a detector would require a massive redesign of the system [17]. Nonetheless, the combination of high-precision spatial and time measurements with silicon pixel sensors has become one of the main goals of detector R&D programs of the last few years.

All the four LHC experiments aim at equipping their detectors with fast timing layers in view of the HL-LHC runs, although for different reasons. The driver for the

⁴ A ToF system with flying distance $L = 1$ m and time resolution $\sigma_t = 1$ ns can separate pions ($m_{\pi^+} = 139.6$ MeV/ c^2) from kaons ($m_{K^+} = 493.7$ MeV/ c^2) with a significance of 5σ up to momenta of 240 MeV/ c . With a time resolution of 20 ps, the separation is possible up to 3.8 GeV/ c .

⁵ The expected number of concurring p-p collisions for the ATLAS and CMS detectors will be of the order of 140 to 200, against the about 50 registered during the current LHC run. The pile-up will be milder for the ALICE and LHCb detectors.

ATLAS, CMS and LHCb collaborations is the pile-up rejection. In particular, the ATLAS and CMS detector will need high time resolution to separate primary vertices, while the LHCb detector will need 4D tracking capabilities to be able to efficiently separate primary from secondary vertices. The purpose of the ALICE collaboration to provide its detector with high resolution timing layers is, instead, the need to improve the separation power of the ToF system for particle identification. In all the cases, the common objective is to identify a sensor technology able to achieve high spatial resolution combined with a time resolution of the order of 10 ps.

The factors contributing to the time resolution of a silicon pixel sensor will be discussed in the next chapter (cf. Section 2.8).

1.4 The ALICE experiment

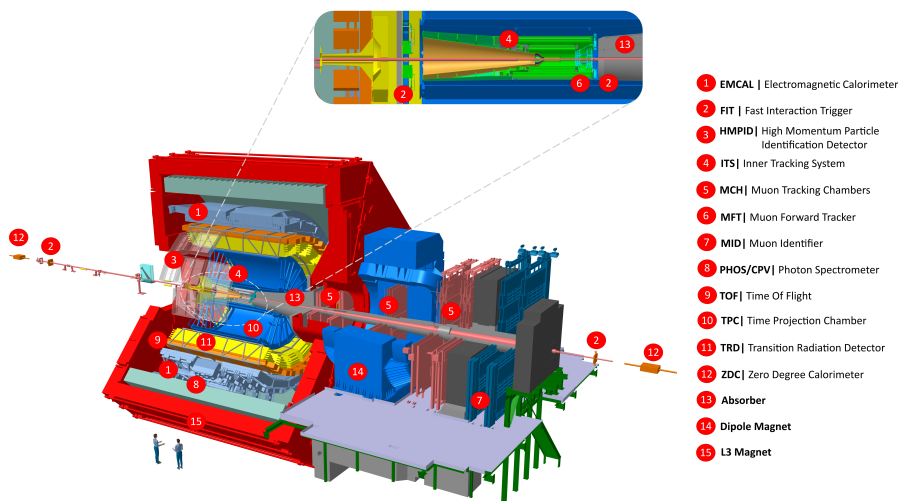


Figure 1.4 The ALICE apparatus with its subdetectors. Figure taken from Reference [18].

ALICE (A Large Ion Collider Experiment) is one of the four experiments at the LHC ring. It is specifically conceived to study heavy ion physics. The main goal of its physics program is the investigation of the properties of the *quark-gluon plasma* (QGP), a deconfined state of quarks and gluons [19]. In ultra-relativistic heavy-ion collisions, the necessary conditions of extreme temperature and density to generate QGP are

reached. To have a complete picture of strongly-interacting matter at extreme energy densities and temperatures, the ability of tracking particles down to low momenta (about 100 MeV/c for pions) as well as particle identification capabilities are required. The ALICE detector is shown in Figure 1.4. The whole detector can be divided into two groups of subsystems: the *central barrel* and the *muon spectrometer*.

The central barrel detectors cover the pseudorapidity⁶ range $|\eta| < 0.9$ and most of them cover the full azimuth. In the central barrel, a solenoid magnet provides a maximum field of 0.5 T parallel to the beam axis. The detectors constituting the muon spectrometer have a forward pseudorapidity acceptance of $-4.0 < \eta < -2.5$.

A detailed overview of the experiment is given in Reference [6].

For the physics reach of ALICE, the capability of coping with the high particle density produced by central Pb-Pb collisions is crucial. This requirement, together with the needed capability of tracking low momentum particles, has led to the design of a high granularity and low material detector in the central region.

1.5 The ALICE Inner Tracking System

To extend its physics reach further and boost the performance of heavy-flavor and dilepton measurements, the ALICE experiment underwent a major upgrade during the LHC Long Shutdown period lasted from 2019 to 2022 [18]. The upgrade included the replacement of the previous Inner Tracking System (ITS), based on two layers of hybrid pixel, two layers of silicon drift and two layers of silicon strip sensors, with a completely new detector, fully based on monolithic active pixel sensor (MAPS) technology. The new detector is known as Inner Tracking System 2 (ITS2), and its layout is shown in Figure 1.5. It consists of seven layers, one more than the ITS, with the innermost three grouped in the Inner Barrel (IB), and the two middle ones and the two outer ones forming the Outer Barrel (OB). The radii of the seven concentric layers range from 23 mm to 400 mm. A detailed discussion on the upgrade of the ALICE ITS detector is provided in Reference [22].

The ITS2 is based on the ALPIDE sensor, a MAPS chip implementing a 180 nm CMOS technology. The ALPIDE chip will be presented in greater detail in Section 3.4.2. The

⁶ The *pseudorapidity* η describes the angle of a particle relative to the beam axis. It is defined as:

$$\eta = -\ln \left[\tan \left(\frac{\theta}{2} \right) \right],$$

where θ is the angle between the particle momentum and the positive direction of the beam axis [20]. It is a commonly used quantity in hadron collider physics because the rates for many of hard-scattering processes of interest are constant as function of η [21].

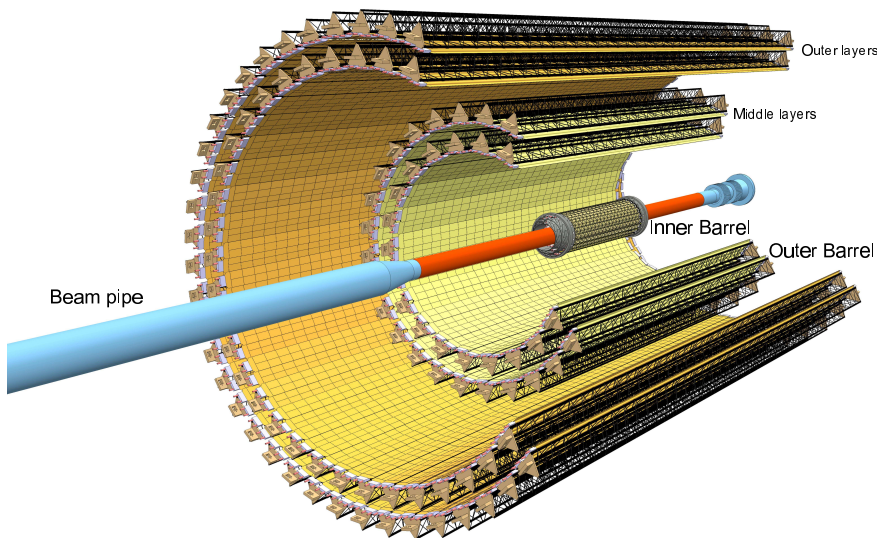


Figure 1.5 Layout of the ITS2. It consists of 3 inner layers, 2 middle layers and 2 outer layers, all covered by monolithic active pixel sensors. Figure taken from Reference [18].

seven layers of the ITS2 are covered by more than 24 000 sensors, for an equivalent of about 12.5 billion pixels and a total active area of about 10 m^2 , resulting in the largest pixel detector ever built.

With respect to its predecessor, the ITS2 can achieve an improved reconstruction of primary and secondary vertices, as well as an improved tracking of low transverse momentum particles ($p_T < 1 \text{ GeV}/c$), besides having an increased readout rate from 1 kHz up to 100 kHz in Pb-Pb and 200 kHz in p-p collisions. The keys for the enriched vertexing performance, translated into an improvement of the impact parameter resolution by a factor 3 in the $r\phi$ coordinate and 5 in the z coordinate, as shown in Figure 1.6, are:

- reducing the material of the inner layers from $1.14\% X_0$ to $0.36\% X_0$;
- reducing the pixel size from $50 \mu\text{m} \times 425 \mu\text{m}$ to $29.24 \mu\text{m} \times 26.88 \mu\text{m}$;
- moving the innermost layer from 39 mm to 23 mm from the interaction point;

while the addition of the seventh highly pixelated tracking layer allows to improve the tracking efficiency and resolution at low p_T . The reduction of the detector material budget as well as the higher sensor segmentation directly descend from the choice of adopting monolithic active pixel sensors as base technology, since MAPS are a natural

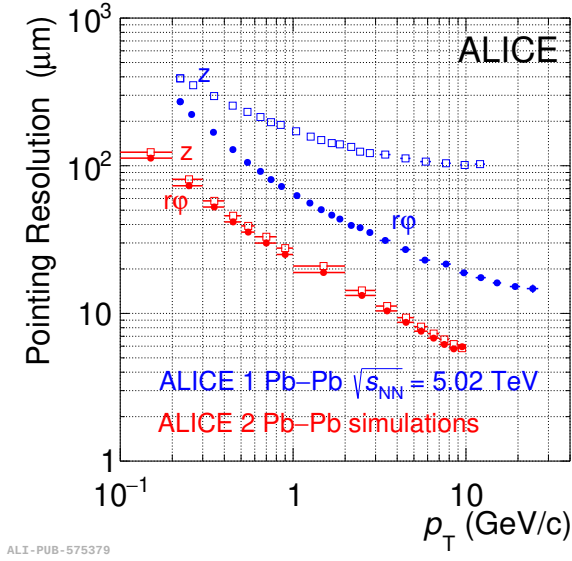


Figure 1.6 Comparison of transverse (solid circle markers) and longitudinal (open square markers) impact parameter resolution in Pb-Pb collision between ITS (blue) and ITS2 (red). Figure taken from Reference [18].

choice for light and high granularity detectors, as will be discussed in the Chapter 3. The ITS2 has been successfully commissioned in November 2021 and has started its operation since July 2022 (i.e. beginning of the LHC Run 3), providing performance within expectations both in p-p (interaction rate 500 kHz) and Pb-Pb (interaction rate up to 47 kHz) collisions.

1.6 Upgrades for High-Luminosity LHC

The current LHC run is expected to last until June 2026. At the end of it, the accelerator will go through a Long Shutdown period, during which the LHC will be upgraded to HL-LHC, with subsequent increase of both peak and integrated luminosity for the next runs (cf. Section 1.1).

To obtain a deeper comprehension of the Quark-Gluon Plasma state, the ALICE experiment is planning to exploit the improved luminosity that will be made available by the HL-LHC to perform a number of measurements not foreseen in the current LHC run. To be able to pursue this ambitious objective, the detector will be subjected to some major upgrades that will impact the Inner Tracking System in the following key aspects:

- improving the pointing resolution and the tracking efficiency at low p_T ;
- improving the radiation hardness;
- integrating fast timing layers to enhance the particle identification capability and, possibly, the vertices separation power.

The points listed above will be addressed in two distinct upgrade phases, that will coincide with the next two LHC Long Shutdown periods, planned from July 2026 to July 2030 and from December 2033 to January 2036, respectively.

The goals of developing sensors able to achieve an improved pointing resolution and to cope with an increased radiation load have already been targeted by the detector R&D effort on monolithic active pixel sensors of the last decade. An R&D program on fast-timing MAPS devices was instead kicked-off more recently. The goal is to develop sensors suitable to build large area detectors, as per ALICE requirements, with the specific aim of equipping the tracker detector with timing layers during the upgrade phase programmed for the shutdown period December 2033–January 2036.

1.6.1 Inner Tracking System upgrade

One of the main goals of the ALICE experiment for the HL-LHC runs is to extend the physics studies regarding the heavy-flavor production and the hadronization process in Quark-Gluon Plasma medium. For example, the comparison of the production yields of strange and non-strange hadrons in the heavy-flavor sector is a necessary measurement to understand heavy-flavor hadronization. To achieve this, the collaboration aims for precision studies of the B_s^0 meson nuclear modification factor via the direct reconstruction of the $B_s^0 \rightarrow D_s^- \pi^+$ decay. The latter measurements require very precise tracking and impact parameter resolution and are therefore a powerful benchmark to assess the improvement provided by the proposed Inner Tracking System 3 (ITS3) upgrade [23].

The upgrade consists in replacing the Inner Barrel of the ITS2 with three new layers:

- closer to the interaction point, with the innermost layer having a radius of 19.0 mm;
- characterized by higher intrinsic spatial resolution, thanks to a sensor with pixel size of $20 \mu\text{m} \times 22.5 \mu\text{m}$;
- featuring a thickness of $0.07\% X_0$ per layer, i.e. only one fifth of the ITS2.

As shown in Figure 1.7, the combination of these three aspects will lead to an increase of the tracking efficiency (left panel) compared to the current ITS2, especially at low

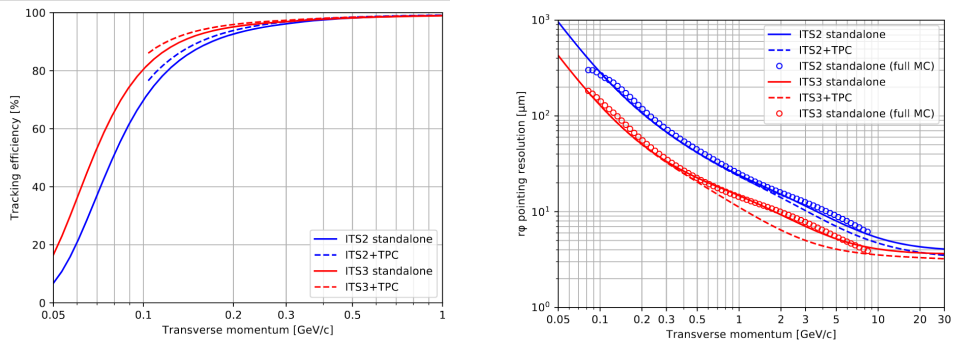


Figure 1.7 Comparison of the track-reconstruction efficiency (left panel) and the pointing resolution in the transverse plane (right panel) with the current ITS2 and the planned upgrade ITS3 detector using a fast simulation Monte Carlo Tool as well as a full Monte Carlo simulation (circles, right panel only). Figures taken from Reference [23].

transverse momentum, and to the reduction of the impact parameter resolution by a factor of two up to about $p_T = 5 \text{ GeV}/c$ (right panel). The improved tracking efficiency and impact parameter resolution reflect in an expected improvement, with respect to the ITS2, of the significance in the reconstruction of B_s^0 meson decay and in an extension of the same measurement to transverse momenta lower than $p_T = 5 \text{ GeV}/c$, as shown in Figure 1.8.

A more detailed discussion on the set of measurements that will benefit from the ITS3 Upgrade is provided in Reference [24].

The ITS3 detector layout is depicted in Figure 1.9. It is made of three concentric cylindrical layers that are split into an upper and a lower half. Each such half-layer is made of few MAPS devices about 27 cm long. The radii of the three layers are 19.0 mm, 25.2 mm and 31.5 mm, respectively⁷ [25].

The new key idea to achieve the goals of improved tracking and vertexing performance listed above is to replace the modules of tiled ALPIDE sensors constituting the current ITS2 layers with a single bent large sensor, where the digital interface circuitry and output data links, which are also the most power consuming components⁸, are confined at the sensor edge. This would allow to remove the heat produced by the ITS3 inner layers using a low-speed air flow in place of the current ITS2 water

⁷ Three wafer-scale devices are foreseen for the first layer, four for the second and five for the third.

⁸ Of the approximately 40 mW cm^{-2} consumed by the ALPIDE (cf. Section 3.4.2), the power dissipated by the pixel matrix only corresponds to a power density of about 7 mW cm^{-2} .

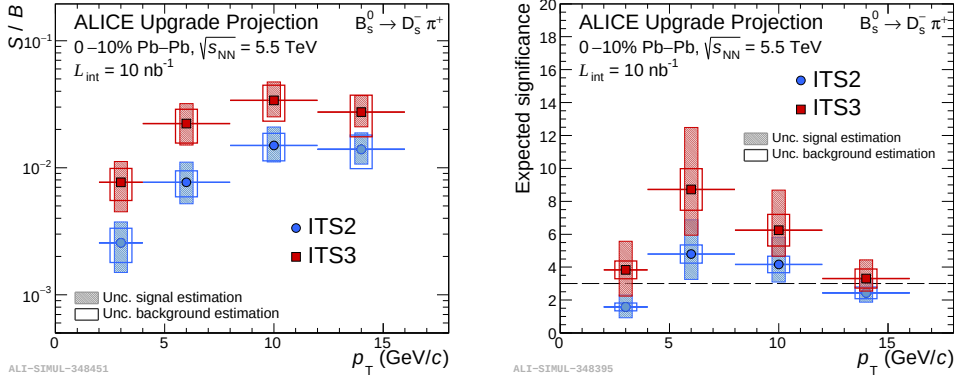


Figure 1.8 Comparison of the expected signal-over-background (left panel) and of the expected significance (right panel) for the measurement of fully reconstructed B_s^0 mesons with the current ITS2 and the planned upgraded ITS3 detector. At transverse momenta of around 3 GeV/c and 14 GeV/c, the measurement is only possible with the ITS3.

cooling system, with consistent reduction of the layers' material. The design of half-layer large sensors is possible by exploiting the stitching technology. It permits the fabrication of an image sensor that is larger than the standard CMOS circuit manufacturing (normally few centimeters in both directions). Stitching is already a mature technology in X-Ray imaging applications [26], but its adoption for the ITS3 represents a pioneering initiative in the field of High-Energy Physics detectors. The large sensors will be thinned to about 50 μm , which corresponds to a radiation length of 0.05% X_0 . Moreover, the possibility of bending and operating ultra-thin silicon sensors to curvature radii of the order of 20 mm [27] opens the way to the construction of a silicon-only cylindrical layer, with lightweight mechanical support structures, and further reduction of the detector material. Finally, the technology chosen for the development of such a sensor is the 65 nm CMOS process of the Tower Partners Semiconductor (TPSCo) foundry [28]. With respect to the 180 nm CMOS process used to manufacture the ALPIDE chip, it offers the advantages of employing silicon wafers of 300 mm diameter that can host a sensor of such a size and of using smaller feature size transistor, which would allow to reduce the pixel pitch to the target value. More details on the different CMOS technologies constituting the base of the ALICE pixel sensors will be given in the next chapters.

The key R&D milestones for the development of such a silicon sensor are therefore:

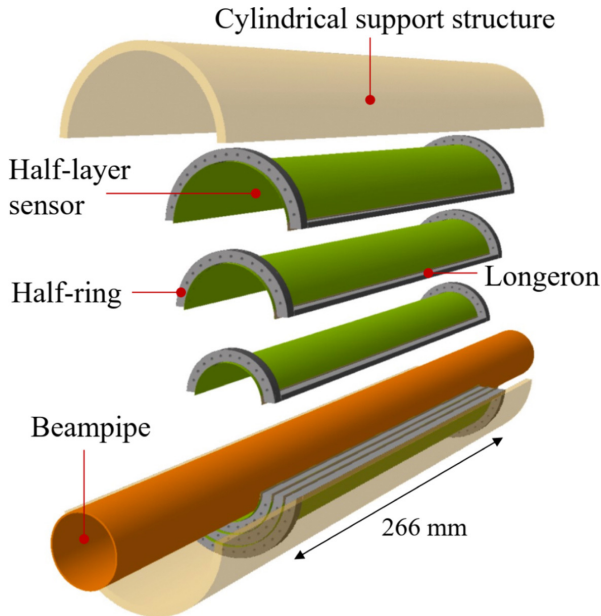


Figure 1.9 Simplified layout of the ITS3. Figure taken from Reference [25].

- the validation of 65 nm CMOS technology for MAPS in High-Energy Physics applications;
- the demonstration of bending silicon sensor to achieve fully operational cylindrical detectors;
- the design and operation of a stitched sensor of $266 \text{ mm} \times 98 \text{ mm}$ with full readout capability.

The research presented in this thesis aims at the validation of the 65 nm CMOS technology for MAPS against the ITS3 requirements and beyond, in view of applications for future vertex and tracker detectors.

A wider discussion on the remaining ITS3 R&D goals, as well as on the production and commissioning plans of the ITS3 detector, can be found in Reference [25].

1.6.2 A new ALICE detector

In spite of the expected results brought by the ITS2 and ITS3 upgrades in the improvement on the precision of heavy flavor production measurements, the precision of the expected results in other sectors, such as hadronization properties of beauty quarks [30] or thermal dilepton emission [31], will still be limited at the end of Run 4.

In particular, the study of the spectrum of low mass dilepton emission opens a window to the understanding of the phenomenon of chiral symmetry restoration. However, even the vertexing capability offered by the ITS3 would not yet allow to distinguish the signal of interest from the background constituted by leptons coming from heavy-flavor decay with sufficient precision. For this reason, a further improvement in the pointing resolution is required. For similar background rejection reasons, the tracking detector needs to be complemented by systems with enhanced particle identification to pinpoint particles with transverse momentum below $300 \text{ MeV}/c$. Moreover, the addition of layers with excellent timing capabilities to the tracker could open the possibility of reconstructing the trajectories of *loopers*, i.e. particles which travel closed spiral paths without reaching the outermost layers of the detector because of their extremely low momentum. The trajectories of such particles can be distinguished from more canonical ones, i.e. those simply bent by the magnetic field, with the combination of excellent pointing resolution and time resolution, which allows to time tag the tracks, opening the way to searches for physics beyond the standard model, like models with Axion-like particles [32].

A complete discussion on the ALICE physics cases beyond LHC Run 4 can be found in Reference [29].

To address the physics goals outlined above, the ALICE experiment has proposed

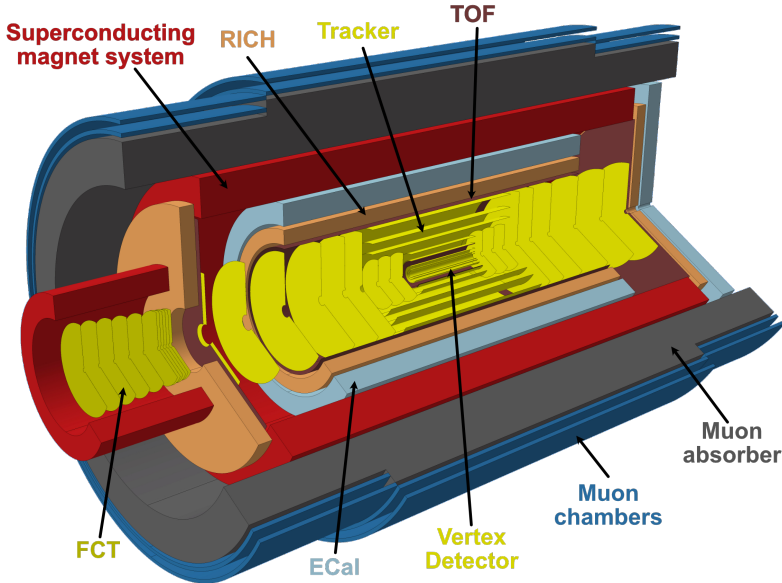


Figure 1.10 Layout of the ALICE3 detector. Figure taken from Reference [29].

an upgrade targeting the installation of a completely new detector, heavily relying on silicon sensors, during the Long Shutdown period planned for December 2033–January 2036. The layout of the *ALICE3* detector is shown in Figure 1.10. At the heart of the apparatus there is a vertex detector, consisting of three cylindrical layers and three disks on either sides, with the innermost layer having a radius of 5 mm, thickness of $0.1\% X_0$ and position resolution of the order of $2.5 \mu\text{m}$. To allow the innermost layer to be so close to the interaction point, the vertex detector is foreseen to be installed within a secondary vacuum of the beam pipe. Such a configuration is expected to grant an unprecedented pointing resolution in the $r\varphi$ plane of about $4 \mu\text{m}$ at a transverse momentum of $p_T = 1 \text{ GeV}/c$.

The tracker comprises eight cylindrical layers, divided in four middle layers and four outer layers, with the outermost layer having a radius of 80 cm, and nine forward disks on either side. Each layer contributes to about $1\% X_0$ in material.

The expected benefits brought by the *ALICE3* vertex and tracker detectors with respect to the ITS3 in the precision of thermal dielectron emission measurements is

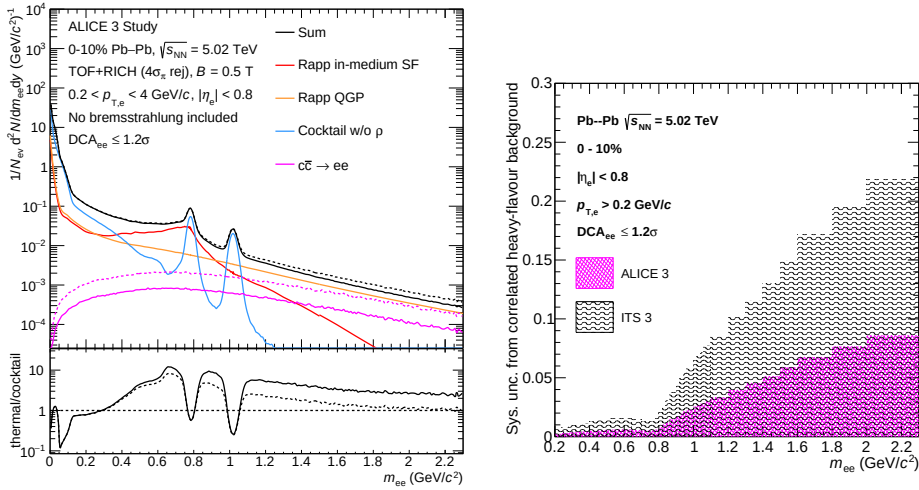


Figure 1.11 Left: Simulated raw dielectron yield as a function of the invariant dielectron mass m_{ee} using the impact parameter resolution of ITS3 or ALICE3 to reject the correlated open charm background (purple line). The ratio of expected thermal dielectrons over those from hadronic decays is shown in the lower part of the figure. The dashed lines correspond to the expectations for ITS3, the solid lines for ALICE3. Right: Corresponding systematic uncertainty on the measured thermal spectrum from hadron gas and QGP arising from the subtraction of the heavy-flavour background. Figures taken from Reference [29].

demonstrated in Figure 1.11. The upper side of the left panel shows the simulated raw signal dielectron yield in central Pb-Pb collisions with its different contributions reconstructed using the impact parameter resolution of ALICE3, depicted with solid lines, and of ITS3, depicted with dashed lines. The biggest improvement provided by ALICE3 consists in the rejection of the e^+e^- background coming from heavy-flavor hadron decays, shown with purple lines. The ALICE3 tracker provides the possibility to suppress this contribution of about a factor 2 over the whole spectrum with respect to the ITS3. The lower part of the left panel describes the same effect expressed as ratio of expected thermal dielectrons over those from hadronic decays. The right panel of Figure 1.11 shows the reduction in systematic uncertainty in the measurement of the thermal dielectron spectrum arising from the subtraction of the correlated heavy-flavor background performed by the ALICE3 tracker with respect to the ITS3.

The particle identification system is composed of the combination of a Time-of-

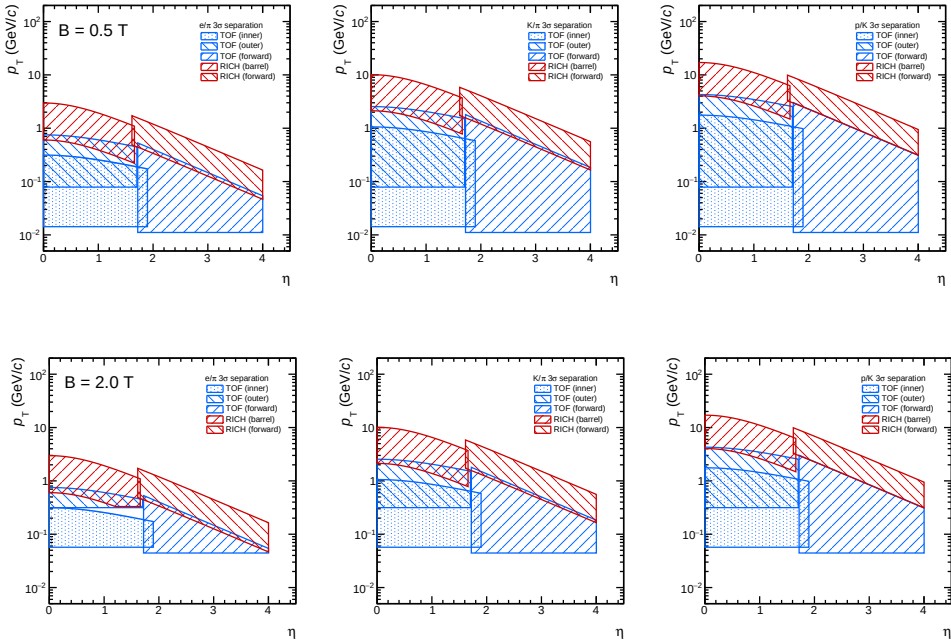


Figure 1.12 Expected regions of the pseudorapidity - transverse momentum phase space in which particles can be separated by at least 3σ with a time resolution of 20 ps. The top row refers to the case in which the particle identification subsystems are embedded in a 0.5 T magnetic field, the bottom row to the case of a 2.0 T field. Electron/pion, pion/kaon and kaon/proton separation plots are shown from left to right. Figures taken from Reference [29].

Flight (TOF) and a Ring Imaging Cherenkov (RICH) detector. In particular, the TOF consists of an inner layer at 19 cm radius, an outer layer at 85 cm radius and a forward disk following the last tracking disk on either sides. With such a configuration and a time resolution of 20 ps, the inner layer could identify particles with $p_T = 300 \text{ MeV}/c$ while the outer layer could identify electrons and hadrons up to $p_T = 500 \text{ MeV}/c$ and $p_T = 2 \text{ GeV}/c$, respectively, as shown in Figure 1.12.

More details on the ALICE3 detector concepts can be found in Reference [29].

MAPS devices are natural candidates for the ALICE3 vertex and tracker detectors, thanks to the successful integration in the ITS2 detector and the promising results already shown by the ITS3 activities. However, their potential for fast timing able to reach $O(10 \text{ ps})$ resolution has to be proven yet, as well as their capability to withstand the substantial increase of radiation load due to the extremely reduced distance between the ALICE3 vertex detector and the interaction point.

1.7 Discussion and conclusion

The experimental investigation of the Quark-Gluon Plasma state of matter requires the capability of precisely identifying primary and secondary vertices in the high particle density environment resulting from heavy-ion collisions and requires tracking of low momentum particles. These goals demand a light, highly granular and precise detector. Driven by the physics demands mentioned above, the ALICE detector is the first LHC experiment to employ monolithic active pixel sensors for its vertex and tracker subdetector, the Inner Tracking System. It has successfully operated since July 2022 and it will run until the end of the LHC Run 3, in 2026.

The HL-LHC upgrade will open the way to study new physics but will pose, at the same time, new challenges to the detectors operating in the accelerator ring. A rich detector R&D program in silicon pixel sensors is therefore at the heart of the ALICE collaboration activities for the design of new sensors. They will have to provide better pointing resolution and track reconstruction, and will have to cope with an increased radiation load related to the high accelerator luminosity. Furthermore, they will be required to integrate fast time resolving power for better particle identification and, possibly, vertex separation.

This chapter describes the current status of the ALICE silicon pixel detector (ITS2) and outlines the concepts behind the detector upgrades, ITS3 and ALICE3, respectively, planned for the next two Long Shutdown periods of the LHC accelerator. The performance achieved by the ALPIDE sensors (cf. Section 3.4.2), currently installed in the ITS2, as well as the requirements for the sensors under development in view of

the detector upgrades are summarized in Table 1.1.

The scope of the research presented in the rest of this dissertation is the characterization of the 65 nm CMOS technology applied to MAPS for High-Energy Physics applications. The test structures presented in the next chapters are studied with the goal of validating the new technology against the ITS3 requirements, with a particular focus on detection efficiency, position resolution and radiation tolerance. Moreover, high emphasis is put in the study of the time resolution achievable by the studied pixel matrix prototypes in view of a possible application of the 65 nm CMOS MAPS technology for future fast timing detectors, such as the ALICE3 Time-of-Flight system and detectors operating in future colliders beyond LHC.

Table 1.1 Pixel sensor requirements for present and future ALICE detector systems.

			ALICE3		
	ITS2	ITS3	Vertex Detector	Tracker	TOF
Detection efficiency (%)	99	99	99	99	99 *
Pixel size (μm^2)	$O(30 \times 30)$	$O(20 \times 20)$	$O(10 \times 10)$	$O(50 \times 50)$	$O(50 \times 50)$ *
Position resolution (μm)	5	5	2.5	10	10 *
Time resolution (ns)	$O(1000)$	100	100	100	0.020
Power consumption (mW/cm^{-2})	47	20	70	20	< 70
Material per layer (% X_0)	0.36	0.07	0.1	1	< 4
Non-Ionizing Energy Loss ($1 \text{ MeV } n_{\text{eq}} \text{ cm}^{-2}$)	3×10^{12}	1×10^{13}	1×10^{16}	2×10^{14} **	2×10^{14} **
Total Ionizing Dose (kGy)	3	10	3000	50 ***	50 ***

* The reported values consider an implementation of the timing layers performed with MAPS.

** The reported value refers to the middle layers of the Tracker and the inner layer of the TOF. For the outer layers, the radiation load in terms of Non-Ionizing Energy Loss is lower and it is estimated to be $6 \times 10^{12} \text{ 1 MeV } n_{\text{eq}} \text{ cm}^{-2}$.

*** The reported value refers to the middle layers of the Tracker and the inner layer of the TOF. For the outer layers, the radiation load in terms of Total Ionizing Dose is lower and it is estimated to be 2 kGy.

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CHAPTER 2

Fundamentals of silicon detectors

SEMICONDUCTOR detectors are particularly suited for the detection of light, ranging from optical photons to X and γ rays, and charged particles. The signal produced by a semiconductor detector is generated by the motion of electron-hole pairs created after the interaction of ionizing radiation with the sensing material. With respect to gaseous detectors, which are based on a similar principle of collecting electrons and ions generated by passing radiation, semiconductors require an amount of energy about a factor ten lower to produce a pair of free charge carriers. Moreover, semiconductors are about a factor one thousand denser than gases, resulting in an enhanced probability of interaction with radiation and subsequent signal generation. These two aspects, together with a relatively easy integration with the readout electronics, explain the success of semiconductor materials, and silicon in particular, as ionizing radiation detectors.

Although the concepts discussed in this section hold for any semiconductor material, silicon is the one described, as it is the most widely used in experimental particle physics. In the following, the basics of silicon physics and of detection process are outlined. An in-depth discussion on semiconductor physics can be found in specialized textbooks, such as References [1, 2], while for detailed considerations on semiconductor devices one can consult References [3, 4]. Finally, the chapter closes by summarizing the effects of radiation damage on silicon and the different factors contributing to the time resolution of a detector system, both relevant topics for the research presented in this dissertation.

2.1 Silicon physics and properties

A silicon atom has fourteen electrons, with ten of them filling the innermost energy levels close to the nucleus, and the remaining four occupying the outermost energy

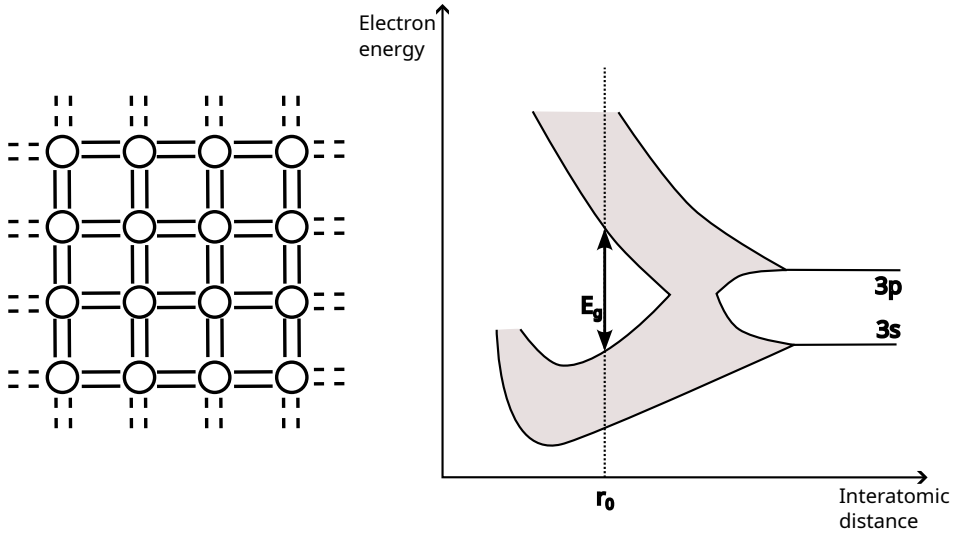


Figure 2.1 Left: two-dimensional representation of the covalent bonding among atoms in a pure silicon crystal. Right: formation of the electronic band structure and band gap in a silicon crystal represented by means of the dependence of the electron energy levels at varying spacing between atoms. At the equilibrium distance r_0 , the valence orbitals merge into two bands, called valence and conduction bands, separated by the band gap of width $E_g = 1.12$ eV.

shells, i.e. $3s$ and $3p$. These four electrons are involved in chemical reactions and are shared with four neighboring atoms, giving rise to bonding forces called *covalent bonding*. The electron sharing and the related bonding process form the silicon crystal, as sketched in the left panel of Figure 2.1. The right panel of Figure 2.1 shows the splitting process of the energy levels into discrete energy bands. At the equilibrium interatomic distance, the electron energy levels overlap into nearly continuous bands. The bands that the valence electrons can occupy are separated by gaps of forbidden energies. At temperature of 0 K, electrons are in the lowest energy state, hence all the states in the lowest band, called *valence band*, are full while all the states in the upper band, called *conduction band*, are empty. The bandgap energy E_g represents the width of the forbidden band. It slightly depends on temperature [5] and it is equal to 1.12 eV at room temperature (i.e. $T = 300$ K).

As the temperature increases above 0 K, electrons in the valence band are thermally excited and transit to the conduction band. Since the semiconductor is electrically neutral, the negative excess of charge in the conduction band caused by the electron transition is compensated by the positive ‘empty state’ left in the valence band. This latter is commonly referred to as *hole*. An electron must have an energy higher than the

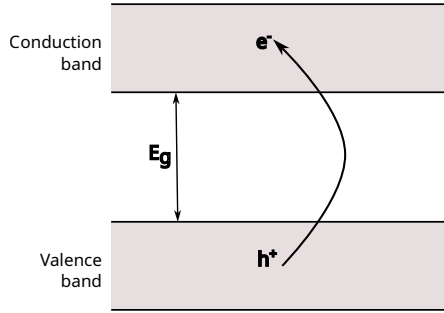


Figure 2.2 Simplified representation of the silicon energy bands and the generation of an electron-hole pair.

bandgap width E_g to hop in the conduction band and leave a hole in the valence band. The generation of an electron-hole pair is sketched in Figure 2.2. As the temperature further increases, more electron-hole pairs are generated. At the same time, some of them recombine (cf. Section 2.3) and, under stable conditions, an equilibrium between generation and recombination processes is established. For a pure silicon crystal, also called *intrinsic silicon*, the concentration n_i of electrons in the conduction band is equal to the concentration p_i of holes in the valence band. Since $n_i = p_i$, the parameter n_i can be used as the intrinsic carrier concentration. It depends on the absolute temperature T according to [4]:

$$n_i p_i = n_i^2 \propto T^{3/2} \exp\left(\frac{-E_g}{2k_B T}\right), \quad (2.1)$$

where k_B is the Boltzmann constant. For silicon at $T = 300$ K, n_i is approximately equal to $1.5 \times 10^{10} \text{ cm}^{-3}$.

Real semiconductor devices are realized by adding controlled amounts of specific dopant atoms to alter the electrical characteristics of the material. The doping process consists in adding pentavalent atoms or trivalent atoms to the silicon crystal. Dopant atoms enter the crystal lattice as substitutional impurities. Pentavalent atoms, such as phosphorus, are called *donors* because they introduce an additional electron to the lattice. Of their five valence electrons, four are involved in the covalent bonding with neighbors silicon atoms, while the fifth can easily be elevated into the conduction band, leaving behind a positively charged ion. The electron in the conduction band can move through the crystal generating a current. Conversely, trivalent atoms, such as boron, are called *acceptors* because they introduce a vacated electron position in the lattice, that can be seen as a hole. Having only three valence electrons, they accept

the fourth electron needed for the covalent bondings from the crystal, becoming a negatively charged ion and leaving a hole in the valence band. A doped silicon crystal is also referred to as *extrinsic silicon*. Silicon where donor impurity atoms have been added, namely where the density of electrons is greater than the density of holes, is called *n-type silicon*. Silicon where the density of holes is greater than the density of electrons is called *p-type silicon*, acceptor impurity atoms have been added. In an n-type semiconductor, electrons are referred to as the majority carrier and holes as the minority carrier. Similarly, in a p-type semiconductor, holes are the majority carrier and electrons the minority carrier.

2.2 The pn junction

When a p-type and an n-type semiconductor are brought into contact with one another they form a *pn junction*. Most semiconductor devices contain at least one junction between p-type and n-type regions. A device consisting of a pn junction only is a rectifying diode. Although used in a different way, also most silicon particle detectors are based on pn junctions. The simplest detector is, for example, a planar diode.

With reference to Figure 2.3a, the interface separating the n and p regions is referred to as the *metallurgical junction*. The large carrier concentration gradient present at the interface induces majority carrier electrons in the n region to diffuse to the p region and majority carrier holes in the p region to diffuse in the n region. The diffusion process leaves positively charged donor atoms in the n region and negatively charged acceptor atoms in the p region. The combination of the two negatively and positively charged regions is referred to as the *space charge region*. The charge distribution in the space charge region creates a potential difference, known as *built-in voltage*, resulting in the presence of an electric field across the metallurgical junction directed from the n to the p region. In thermal equilibrium and steady state conditions, the diffusion process is halted and the electric field sweeps out all the electrons and holes of the space charge region. Since the latter is left with no mobile charge carriers, it is also called *depleted region*. Figure 2.3b shows the charge distribution in the space charge region under the simplifying assumptions of planar abrupt junction, i.e. step variation of majority carrier concentrations between p and n regions, and that the space charge region abruptly ends at $x = +x_n$ and $x = -x_p$, with x_p being a positive quantity. The space charge $\rho(x)$ is therefore:

$$\rho(x) = \begin{cases} -eN_a & -x_p < x < 0 \\ eN_d & 0 < x < x_n \end{cases}, \quad (2.2)$$

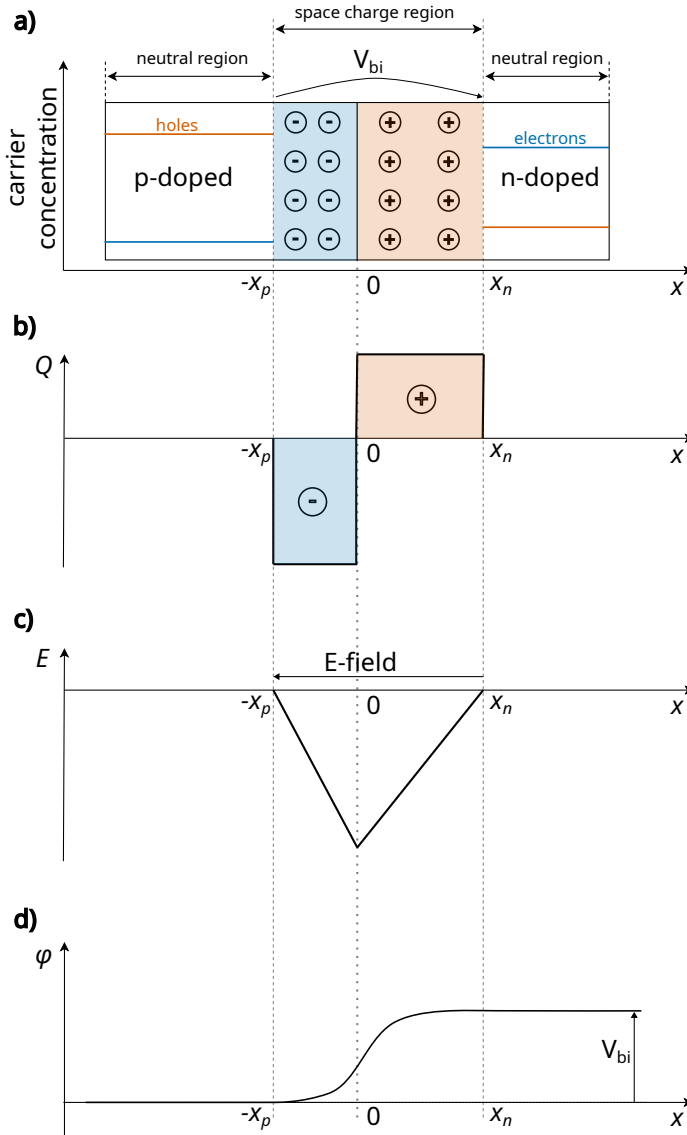


Figure 2.3 Simplified one dimensional representation of a pn junction at thermal equilibrium with no bias voltage applied. From top to bottom: a) A pn junction diode; b) Charge distribution in the space charge region; c) Electric field in the depleted region; d) Variation of potential in the depleted region.

where N_a and N_d are the acceptor and donor atom concentrations, respectively, expressed in cm^{-3} . The charge neutrality of the material implies that:

$$eN_aV_p = eN_dV_n \rightarrow eN_ax_pS = eN_dx_nS \rightarrow N_ax_p = N_dx_n, \quad (2.3)$$

where V_p and V_n are the depleted volumes in the p and n regions, respectively, and S is the surface of the junction.

The electrical properties of the pn junction diode can be deduced from the space charge by solving the Poisson equation:

$$\Delta\phi(\vec{r}) = -\frac{\rho(\vec{r})}{\epsilon_{Si}} , \quad (2.4)$$

where ϕ is the electric potential and ϵ_{Si} is the electric permittivity of silicon¹. Equation 2.4 holds for a general geometry and doping profile, however, for the simplified one dimensional case sketched in Figure 2.3b, the Poisson equation can be simplified to the following:

$$\frac{d^2\phi(x)}{dx^2} = -\frac{\rho(x)}{\epsilon_{Si}} . \quad (2.5)$$

The electric field is by definition:

$$\vec{E}(\vec{r}) = -\nabla\phi(\vec{r}) . \quad (2.6)$$

For the one-dimensional analysis:

$$E(x) = -\frac{d\phi(x)}{dx} . \quad (2.7)$$

In other words, the electric field can be computed by integrating Equation 2.5 once:

$$\frac{d^2\phi(x)}{dx^2} = -\frac{\rho(x)}{\epsilon_{Si}} = -\frac{dE(x)}{dx} \rightarrow E(x) = \int \frac{\rho(x)}{\epsilon_{Si}} dx . \quad (2.8)$$

By putting Equation 2.2 into Equation 2.8 with boundary conditions $E(-x_p) = E(x_n) = 0$:

$$E(x) = \begin{cases} -\frac{eN_a}{\epsilon_{Si}} (x + x_p) & -x_p \leq x \leq 0 \\ -\frac{eN_d}{\epsilon_{Si}} (x_n - x) & 0 \leq x \leq x_n \end{cases} . \quad (2.9)$$

¹ The electric permittivity of a material is equal to the product of the permittivity of vacuum and the relative permittivity of the material itself. For silicon:

$$\epsilon_{Si} = \epsilon_0 \times \epsilon_{r, Si} = 8.85 \cdot 10^{-3} \frac{fF}{\mu m} \times 11.68 = 0.1034 \frac{fF}{\mu m} .$$

The electric field within the space charge region is represented in Figure 2.3c. In general, the maximum electric field occurs at the metallurgical junction. For the simple case considered in this section, the maximum electric field is:

$$E_{max} = E(x = 0) = -\frac{eN_a}{\epsilon_{Si}} x_p = -\frac{eN_d}{\epsilon_{Si}} x_n. \quad (2.10)$$

The potential in the junction is found by integrating the electric field expressed by Equation 2.9 with the boundary conditions $\phi(-x_p) = 0$ and $\phi(x_n) = V_{bi}$:

$$\phi(x) = -\int E(x)dx = \begin{cases} \frac{eN_a}{2\epsilon_{Si}} (x + x_p)^2 & -x_p \leq x \leq 0 \\ -\frac{eN_d}{2\epsilon_{Si}} (x_n - x)^2 + V_{bi} & 0 \leq x \leq x_n \end{cases}. \quad (2.11)$$

The shape of the potential is sketched in Figure 2.3d. The built-in potential V_{bi} can be explicitly calculated from Equation 2.11 by considering that the potential across the junction is continuous in $x = 0$:

$$V_{bi} = \frac{e}{2\epsilon_{Si}} (N_d x_n^2 + N_a x_p^2). \quad (2.12)$$

From this last result, it is possible to calculate the width d of the depleted region, by taking into account the charge neutrality of the junction expressed by Equation 2.3:

$$d = x_p + x_n = \sqrt{\frac{2\epsilon_{Si} V_{bi}}{e} \left(\frac{N_a + N_d}{N_a N_d} \right)}. \quad (2.13)$$

For the operation of a device based on a pn junction as a particle detector, a negative voltage to the p-type region with respect to the n-type region (or, in an equivalent fashion, a positive voltage to the n-type region with respect to the p-type region) is typically applied. With such a bias voltage, the device is said to be operated in *reverse bias* condition. Figure 2.4 shows a pn junction with a reverse bias voltage V_R applied. The net effect of such an operation regime manifests in the enlargement of the depleted zone, with subsequent increase of the detection efficiency because of the larger sensitive volume of the detector. For the pn junction shown in Figure 2.3a and operated with a reverse bias voltage V_R applied, the width d of the depleted region is:

$$d = x_p + x_n = \sqrt{\frac{2\epsilon_{Si} (V_{bi} + V_R)}{e} \left(\frac{N_a + N_d}{N_a N_d} \right)}. \quad (2.14)$$

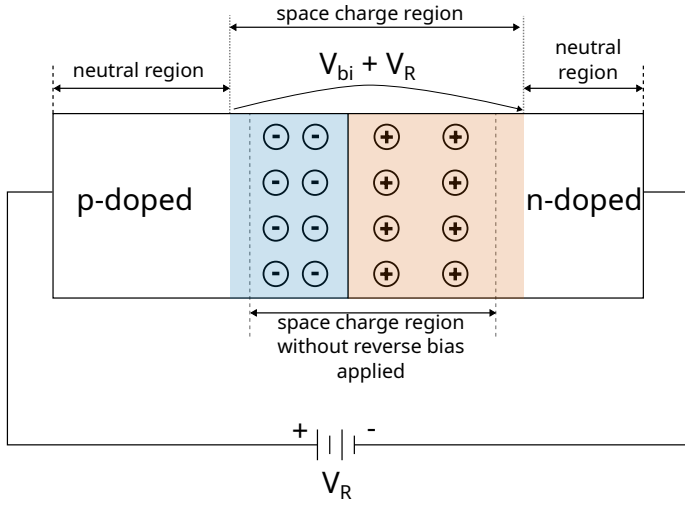


Figure 2.4 A pn junction operated with a reverse bias voltage V_R . The application of reverse bias enlarges the depleted region with respect to the junction at thermal equilibrium.

The external voltage raises the potential difference between the n-type and the p-type regions above the built-in value V_{bi} , intensifying the electric field across the junction. This favors a faster and more efficient charge collection process, because based on the drift of charge carriers (cf. Section 2.4). When the applied reverse bias voltage is higher than what is needed to fully deplete the silicon volume, the detector is said to be *over-depleted*. Such an operation condition further facilitates the charge collection, as it uniformes the intensity of the electric field throughout the junction. The maximum applicable voltage is limited by the resistance of the semiconductor. At some point, the junction will break down and will begin conducting. *Avalanche multiplication* is the main breakdown mechanism. For sufficiently high fields, free or released charge carriers gain enough kinetic energy to produce secondary charge carriers via impact ionization.

The presence of positive and negative charges on both sides of the junction is the cause of the junction, or depletion, capacitance. It depends on the variation of the charge density in the depleted region at varying reverse bias voltage and is defined as:

$$C_d = \frac{dQ}{dV_R} . \quad (2.15)$$

A planar diode with surface S and depleted volume of width d , such as the one sketched

in Figure 2.3a, behaves as a parallel plate capacitor. Its capacitance is therefore:

$$C_d = \frac{\epsilon_{Si}}{d} S. \quad (2.16)$$

Equation 2.16 shows that a more extended depleted region, obtainable with enhanced reverse bias voltage, results in a lower junction capacitance. The latter affects the noise characteristics and the amplitude of the voltage signals of the detector, and it is typically desirable to be as low as possible. In real pixel detectors, other factors contribute to the overall pixel capacitance besides the junction capacitance, such as the coupling capacitance to neighboring pixels and the capacitance of the readout electronics.

The expressions derived in this section hold for the simple case of a planar abrupt junction with uniform doping profiles. The linear dependence of the electric field and the quadratic dependence of the potential on distance through the space charge region descend from the simple uniform doping profiles presented as an example in this section. For realistic doping profiles, more complex expressions of the electric field and of the potential are found. Real MAPS devices feature complicated geometries, with several pn junctions in a single pixel. They are characterized by a highly non-linear electric field within the pixel volume. Moreover, the abrupt junction approximation hardly holds for real devices, as the high temperatures characterizing many technological processes can enhance the diffusion of majority carriers and, therefore, affect the doping profiles.

From these arguments, it follows that the Poisson equation (cf. Equation 2.4) cannot be solved analytically, hence the electrostatic properties must be derived numerically by means of a simulation software.

2.3 Carrier generation, recombination and trapping

In semiconductors, the creation of electron-hole pairs can be due to different mechanisms supplying the necessary energy, such as thermal agitation, optical excitation and ionization by incoming radiation. The interaction between radiation and detector is described in Section 2.5.

For silicon at room temperature ($T = 300$ K), the average energy W needed by an incident charged particle to produce an electron-hole pair is 3.6 eV, i.e. more than three times the bandgap energy. This is due to the stochastic nature of the energy loss of charged particles in matter. Since only part of the deposited energy ionizes the atoms, the rest is transferred to crystal lattice via phonon interaction processes, resulting

in an average required energy larger than the bandgap to produce an electron-hole pair. The value of W is nearly independent on the type of charged particle interacting with the material. In case of interaction with photons, photoelectric absorption is the main mechanism responsible for the generation of charge carriers in silicon. At low energies, a linear relation $W = h\nu$ (one electron-hole pair per incident photon) holds for photon energies between the bandgap and 4 eV, with a maximum value of $W = 4.4$ eV found at photon energy around 6 eV. For incident energies above 50 eV, the average electron-hole creation energy W is constant and equal to 3.6 eV [6], such as in the case of interaction with charged particles. It can be explained by considering that the ejected photoelectron has sufficient energy to ionize nearby atoms in the crystal, effectively behaving as a charged particle.

Once an excess of minority charge carriers, i.e. electrons in p-type silicon or holes in n-type silicon, is created, the system will take some time to come back to thermal equilibrium. The transition back to equilibrium is due to recombination of the excess minority carriers with the majority carriers. In silicon, the main recombination process occurs through *recombination centers*, namely impurities in the crystal perturbing the energy structure by adding additional levels in the forbidden gap. An electron in conduction band can be captured by a defect level with subsequent energy radiation. Afterward, it can turn from the intermediate level to the valence band. This process is also known as *Shockley-Read-Hall recombination*, or *trap-assisted recombination* [7, 8]. Another important recombination mechanism, known as *Auger recombination* and relevant for highly doped silicon (i.e. doping concentration above $1 \times 10^{18} \text{ cm}^{-3}$), involves three carriers. In this process, an electron and a hole recombine by transferring the recombination energy to a third free electron in the conduction band [9, 10].

For radiation detectors, the presence of impurities acting as recombination centers is detrimental since it reduces the charge carrier's mean lifetime, namely the time the charge carrier remains free to move and contribute to the detector's signal.

Some impurities are capable of capturing only one type of charge carrier. Trapping centers hold charge carriers for a characteristic time before releasing them. A trapping time comparable to the charge collection time corresponds to a loss of signal for a particle detector.

Besides impurity atoms, structural defects in the crystal lattice can also act as recombination and trapping centers by adding new energy levels in the bandgap. These defects can arise during the growth of the crystal, or may be related to thermal or mechanical shocks, or to the damage induced to the lattice by incident radiation. The latter phenomenon is discussed in Section 2.7.

2.4 Carrier transport phenomena

The net flow of electrons and holes in a semiconductor generates a current. There are two types of transport mechanisms: *diffusion*, due to carrier concentration gradients, and *drift*, due to the presence of an electric field.

Since charge carriers diffuse from regions of high concentration to regions of low concentration, the diffusion current density, for both electrons and holes, is proportional to the opposite of the carrier concentration gradient. Defining n and p the concentrations of electrons and holes, respectively, the electron and hole diffusion current densities can be written as:

$$\begin{cases} \vec{J}_{n,diff} = eD_n \nabla n \\ \vec{J}_{p,diff} = -eD_p \nabla p \end{cases}, \quad (2.17)$$

where D_n and D_p are the *electron diffusion coefficient* and *hole diffusion coefficient*, respectively. They are expressed in units of cm^2/s .

If an electric field $\vec{E}$ is present, such as in the case of the depleted region of a pn junction (cf. Section 2.2), the carriers move parallel to the electric field. The drift current densities can be expressed as:

$$\begin{cases} \vec{J}_{n,drift} = en\vec{v}_n = -en\mu_n\vec{E} \\ \vec{J}_{p,drift} = ep\vec{v}_p = ep\mu_p\vec{E} \end{cases}. \quad (2.18)$$

μ_n and μ_p are the *electron mobility* and the *hole mobility*, respectively, and represent the proportionality factor between the charge carrier drift velocity and the electric field strength. They are expressed in units of $\text{cm}^2/(\text{V} \cdot \text{s})$. At low electric fields, the drift velocity varies only linearly with the applied field because the charge carriers are involved in collisions with the crystal lattice and impurity atoms during their motion. Conversely, if the field is strong enough to have drift velocities comparable to thermal velocity, a strong deviation from linearity and a saturation behavior is observed. The drift velocity of electrons in silicon saturates approximately at $1 \times 10^7 \text{ cm/s}$ with applied electric field of about 30 kV/cm . For silicon at 300 K and in low electric field regime, the electron and hole mobilities at low doping concentrations, i.e. below concentrations of $1 \times 10^{16} \text{ cm}^{-3}$, are about $1450 \text{ cm}^2/(\text{V} \cdot \text{s})$ and $450 \text{ cm}^2/(\text{V} \cdot \text{s})$, respectively [11]. The mobility of both charge carriers decreases with enhanced doping concentration because of the increasing relevance of the scattering phenomena with impurity atoms. For doping concentrations of $1 \times 10^{19} \text{ cm}^{-3}$, the mobility of electrons and holes decreases to about $120 \text{ cm}^2/(\text{V} \cdot \text{s})$ and $60 \text{ cm}^2/(\text{V} \cdot \text{s})$, respectively [11]. The total current density is given by the sum of the diffusion and drift components

presented in Equation 2.17 and Equation 2.18.

For both carrier species, the mobility is linked to the diffusion constant through the Einstein relation:

$$\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = \frac{k_B T}{e} . \quad (2.19)$$

Outside the linear response regime, i.e. when the drift velocity is not a linear function of $\vec{E}$, the Einstein relation is no longer valid.

Outside the thermal equilibrium condition, the interplay between generation and recombination processes and transport phenomena of the charge carriers is described by the *continuity equation*. It can be written as:

$$\begin{cases} \frac{\partial n}{\partial t} = -\frac{1}{e} \nabla \cdot \vec{J}_n + G_n - R_n = n\mu_n \nabla \cdot \vec{E} - D_n \Delta n + G_n - R_n \\ \frac{\partial p}{\partial t} = \frac{1}{e} \nabla \cdot \vec{J}_p + G_p - R_p = -p\mu_p \nabla \cdot \vec{E} + D_p \Delta p + G_p - R_p \end{cases} , \quad (2.20)$$

where G_n and G_p are the electron and hole generation rate, expressed in units of $\text{cm}^{-3} \text{s}^{-1}$, respectively. R_n and R_p are the electron and hole recombination rate, expressed in units of $\text{cm}^{-3} \text{s}^{-1}$, respectively, and are inversely proportional to the charge carrier lifetime (cf. Section 2.3). Equation 2.20 states that the net change in the concentration of a certain carrier type in an arbitrary part of the semiconductor is given by the difference of generation and recombination in the volume and the inward current density flux through the volume's surface. The electric field $\vec{E}$ is determined by the charge distribution through Poisson equation (cf. Equation 2.4).

Another important semiconductor property can be derived from the expression of the drift current density. It may be written as:

$$\vec{J}_{drift} = e(n\mu_n + p\mu_p)\vec{E} = \sigma \vec{E} , \quad (2.21)$$

where σ is the *conductivity* of the semiconductor material. It describes the capability of the material to conduct current and is given in units of $(\Omega \cdot \text{cm})^{-1}$. The *resistivity* ρ is the inverse of the conductivity and is expressed as:

$$\rho = \frac{1}{e(n\mu_n + p\mu_p)} . \quad (2.22)$$

The doping concentration of silicon is typically expressed in terms of resistivity because it is an easily measurable quantity. For intrinsic silicon, the resistivity is of the order of $350 \text{ k}\Omega \cdot \text{cm}$. A high purity silicon is a high resistivity material, while

highly doped silicon is a low resistivity material.

2.5 Radiation-detector interaction

Particles are detected only by the energy they lose when they interact with the detector material. Different particles at different energies interact in different ways with matter. This section provides an overview of the interaction of charged particles and electromagnetic radiation with matter, with focus on the relevant processes for the research presented in the thesis. A more comprehensive treatment of these and other important phenomena can be found elsewhere [12–14].

2.5.1 Energy loss of charged particles

Charged particles traversing a material lose part of their energy through elastic collisions with shell electrons. These collisions may either transfer enough energy to the electrons to ionize the atom, or they may excite the whole atomic structure, with no ionization. In semiconductors, the former type of interaction causes the transition of an electron to the conduction band from the valence band, if the transferred energy is higher than the bandgap energy. The transferred energy can be such that the electron causes secondary ionization. If this is the case, the secondary electron is called a δ *electron*. Elastic scattering from nuclei also occurs, but the energy transferred to nuclei is usually negligible, as the masses of nuclei are large if compared to the incident particles.

The amount of energy lost by a charged particle traveling in a medium is a stochastic quantity. An expression for the average energy loss per unit path length, also referred to as *stopping power*, has been developed by Bohr [15] first, using a semi-classical approach, and later by Bethe [16] and Bloch [17]. The relation, sometimes called *Bethe-Bloch equation*, holds for particles heavier than electrons and positrons, and can be found as [12]:

$$\left\langle -\frac{dE}{dx} \right\rangle = K \rho z^2 \frac{Z}{A} \frac{1}{\beta^2} \left(\frac{1}{2} \log \frac{2m_e c^2 \beta^2 \gamma^2 T_{max}}{I^2} - \beta^2 - \frac{\delta}{2} \right), \quad (2.23)$$

where $\langle -dE/dx \rangle$ is the mean energy loss per unit length of the absorber, z is the charge number of the incident particle, Z is the atomic number of the absorber, A the atomic weight of the absorber, m_e the electron mass, and

$$K = 4\pi N_A r_e^2 m_e c^2 = 0.3071 \text{ MeVcm}^2 \text{mol}^{-1}, \quad (2.24)$$

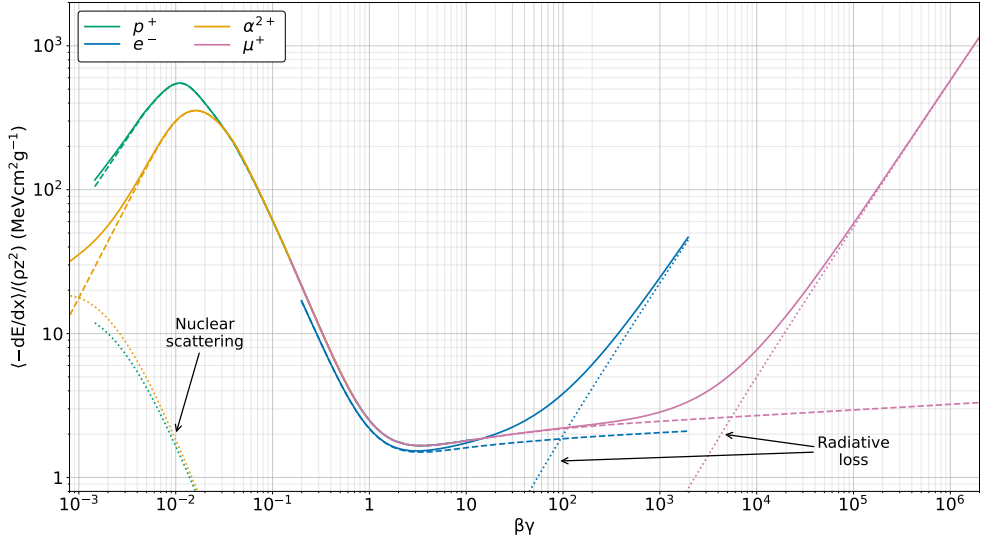


Figure 2.5 Mass stopping power in silicon as a function of the $\beta\gamma$ factor for protons [19] (green), electrons [20] (blue), alpha particles [21] (orange, normalized to the charge number squared), and muons [22] (magenta). For protons and alpha particles, the contribution of nuclear scattering to the mass stopping power (represented with dotted lines) is relevant at very low energy. For electrons and muons, the contribution of radiative loss to the mass stopping power (represented with dotted lines) becomes dominant at high energy, beyond the point of minimum ionization.

in which N_A is the Avogadro constant and r_e is the classical electron radius². The Bethe-Bloch equation depends on the maximum kinetic energy that can be transferred to a free electron at rest in a single collision by an incident particle of mass m :

$$T_{max} = \frac{2m_e c^2 \beta^2 \gamma^2}{1 + 2\gamma m_e/m + (m_e/m)^2} . \quad (2.25)$$

Moreover, Equation 2.23 depends on the mean excitation potential I , which is a property of the absorber material and depends on its atomic number Z . The quantity δ , called *density effect* [18] correction factor, takes into account the polarization of the medium, which becomes important at high energies.

² The classical electron radius is defined as:

$$r_e = \frac{1}{4\pi\epsilon_0} \frac{e^2}{m_e c^2} = 2.8179 \text{ fm} .$$

The stopping power is usually given in units of $\text{MeV cm}^2 \text{g}^{-1}$, obtained dividing Equation 2.23 by the density of the absorber. This latter quantity, representing the energy loss per area density, is also referred to as *mass stopping power*. It is a useful quantity because it is about the same for most materials, being only slightly dependent on the atomic number of the material. Figure 2.5 shows the mass stopping power of different charged particles in silicon as a function of the $\beta\gamma$ factor. At non-relativistic energies, $\langle -dE/dx \rangle$ decreases with increasing velocity until about $\beta\gamma = 1$, where a broad region of minimum ionization is reached. Particles at this point are known as *minimum ionizing*. The point of minimum ionization is about the same ($\beta\gamma \simeq 3$) for all the particles with the same charge. Beyond the point of minimum ionization, the stopping power is almost constant, with slight increasing trend due to the logarithmic dependence of Equation 2.23. For very high particle energy, energy losses due to radiation phenomena become relevant and the Bethe-Bloch equation fails, as it models only energy losses due to ionization and excitation in the absorbing material. Equation 2.23 cannot be used for slow particles ($\beta\gamma < 0.05$) as well, since a number of other effects other than ionization and excitation of the material comes into play, such as the tendency of the incident particle to pick up electrons.

Electrons and positrons also suffer from collision energy loss with the electrons of the absorbing material. However, Equation 2.23 must be modified because the ionization loss suffered by these particles differs from loss by heavy particles. The most important difference with the Bethe-Bloch equation described above is in the small mass. The modified equation must indeed take into account the frequent change of directions of the incident particle when interacting with the electrons that it ionizes. Furthermore, other considerations related to the kinematics, spin, charge and identity of the ionizing particle should be included [12]. Moreover, the probability of energy loss via radiative emission is enhanced with respect to heavier particles and plays an important role already for energies of few tens of MeV. Nonetheless, as shown in Figure 2.5, a region of minimum ionization in the mass stopping power curve can be identified also for electrons, corresponding to kinetic energies of few MeV in silicon³.

Due to the stochastic nature of the interaction process, the number of collisions and the sum of energy losses along a particle track are subject to fluctuations. Equation 2.23 only quantifies the mean energy loss of a traveling charged particle into a material and, especially for minimum ionizing particles (MIPs), it does not reliably describe the interaction of a single particle. The fluctuations in the energy loss are described by a probability density function, also known as *straggling function*, which depends on the

³ For positrons, although not represented in Figure 2.5, a stopping power curve with minimum ionization region similar to electrons can be drawn.

absorber thickness. In a relatively thick absorber⁴, the number of collisions is large and the energy loss distribution tends to a Gaussian function. For thinner materials, the number of collisions is lower and the probability density function becomes very asymmetric. The asymmetry is due to the possible large energy transfers happening in a single collision. Although rare, they can contribute to the high energy side of the distribution, giving it a skewed shape. Calculations to retrieve the expression of such a distribution have been carried out by Landau [23] and Vavilov [24]. The two solutions have different regions of applicability and the discriminating factor is the maximum transferable energy in a single collision. In particular, the probability density function f_L calculated by Landau, hence commonly called *Landau distribution*, represents the energy loss Δ of a charged particle traveling in a thin layer of thickness x under the assumption that the ratio between the mean energy loss and the maximum energy transfer in a single collision is less than or equal to 0.01. For the calculation, the free electron (Rutherford) cross section is used to compute the probability per unit path length for a collision to transfer energy to an electron in the material. The function has a complex analytical expression that can be reasonably approximated by [25]:

$$f_L(\lambda) \simeq \frac{1}{\sqrt{2\pi}} \cdot \exp \left[-\frac{1}{2} \left(\lambda + e^{-\lambda} \right) \right], \quad (2.26)$$

where λ expresses a measure of the deviation from the most probable energy loss Δ_p :

$$\lambda = \frac{\Delta - \Delta_p}{\xi}. \quad (2.27)$$

ξ is known as *Landau parameter*:

$$\xi = \frac{K}{2} \rho x z^2 \frac{Z}{A} \frac{1}{\beta^2} = 1.78 \cdot 10^{-2} \frac{\text{keV}}{\mu\text{m}} \frac{x}{\beta^2} \text{ in silicon}, \quad (2.28)$$

with all the parameters already defined for Equation 2.23. The full width at half maximum (FWHM) w is related to the Landau parameter ξ according to:

$$w = 4.018 \xi. \quad (2.29)$$

The expression for the most probable energy loss is [12]:

$$\Delta_p = \xi \left[\ln \left(\frac{2m_e c^2 \gamma^2 \beta^2}{I} \right) + \ln \left(\frac{\xi}{I} \right) + 0.2 - \beta^2 - \delta \right]. \quad (2.30)$$

⁴ The assumption of thick absorber is valid when $dE/dx \cdot x \gg 2m_e c^2 \beta^2 \gamma^2$.

If compared to experimental observations, the Landau model systematically underestimates the FWHM of the straggling function. The effect is particularly evident for thin absorbers below few hundred micrometers [26]. A better match is found if the convolution of a Landau function with parameters Δ_p and ξ with a Gaussian function is considered [27]. The standard deviation σ of the Gaussian takes into account also the detector and the electronics noise [28]. The convolution function is also referred to as *Langaus* function. The left panel of Figure 2.6 represents the comparison of the energy loss spectra normalized on the length of the absorber for 120 GeV/ c protons traveling in silicon layers of different thickness computed with the Landau (dashed lines) and the Langaus (solid lines) functions.

The right panel of Figure 2.6 illustrates the most probable energy loss per unit length

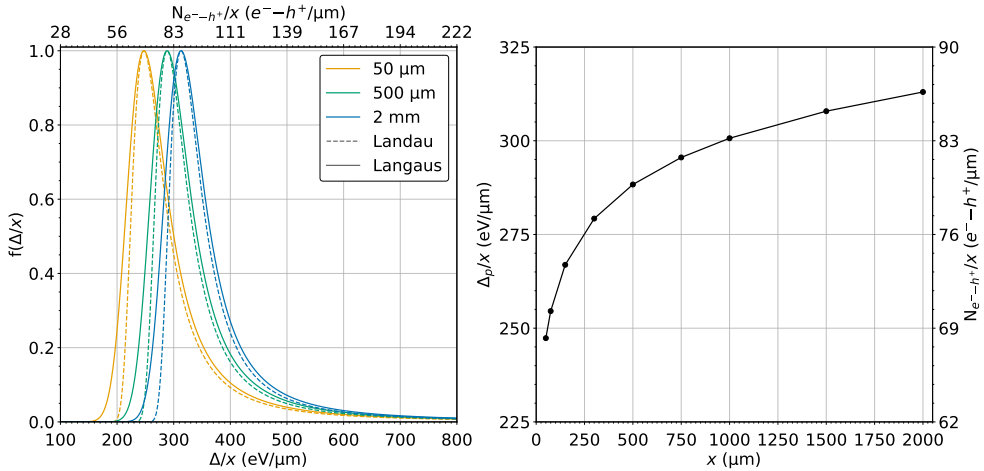


Figure 2.6 Left: Energy loss spectra per unit length calculated for 120 GeV/ c protons traveling in silicon layers of different thickness. The y-axis is an arbitrary scale, and all spectra are normalized to the same peak height. The dashed lines represent the spectra evaluated with the Landau model, the solid lines the spectra calculated with the Langaus model. For both models, the parameters Δ_p and ξ are computed with Equation 2.30 and Equation 2.28, respectively. For the Langaus function, the parameter σ is set equal to ξ . The top horizontal axis represents the corresponding number of electron-hole pairs produced per unit length. The Landau function is approximated according to the implementation of Reference [29]. Right: Most probable value of the energy loss per unit length computed with Equation 2.30 for 120 GeV/ c protons as a function of the thickness of the traversed silicon layer. The right y-axis shows the corresponding number of electron-hole pairs generated per unit length. The line connecting the points is drawn to guide the eye.

as a function of the silicon absorber thickness computed for 120 GeV/c protons. As shown, the most probable energy loss per unit length increases with the absorber thickness. Equation 2.30 is quite reliable to describe the most probable value (MPV) of the straggling function for silicon layers down to about 100 μm [30]. For thinner materials, the Landau fails in predicting what is observed experimentally. A number of corrections has been proposed to improve the calculation of the straggling function by considering that electrons in a material are not free, hence the Rutherford cross section can not be used to model the collisions between the incident particle and the electrons of the absorber, and the bonding effects of the atomic electrons must be included [30–32].

Experimental energy loss distributions are typically fitted with a Langaus function where the MPV Δ_p , the parameter ξ and the Gaussian standard deviation σ are left as fitting parameters. In particular, from the knowledge of the MPV it is possible to estimate the active thickness of the detector. An approximation of Δ_p to within 1.2% for particles with $\beta\gamma > 100$ traversing a silicon layer of thickness $13 \mu\text{m} < d < 110 \mu\text{m}$ is given by the following empirical expression [30]:

$$\Delta_p(\text{eV}) = d(\mu\text{m}) \times [100.6 + 35.35 \ln d(\mu\text{m})] . \quad (2.31)$$

For 10 μm thick silicon interacting with particles having $\beta\gamma > 100$, the most probable energy loss is 1.857 keV [30].

Minimum ionizing particles (MIPs) traverse the material producing a nearly uniform electron-hole density along their path, with fluctuations in the amount of generated carriers as described above. These fluctuations are one of the fundamental limiting factors of the time resolution of a sensor (cf. Section 2.8). Electrons emitted by β radioactive sources interacting with very thin detectors, especially in the case of particles at the high end of the β spectrum (i.e. energies of the order of 1 MeV), can also be considered as MIPs.

The energy straggling in ultra-thin silicon layers is particularly relevant for the study of MAPS, where the active thickness is of the order of few tens of μm . It is worth to underline that, as shown in the right panel of Figure 2.6, the most probable energy loss per unit length traveled by a MIP in a silicon layer varies with the thickness of the absorber. As reported above, for a thickness of the order of 10 μm , the energy loss is about 200 eV/ μm , corresponding to $55 e^-h^+/\mu\text{m}$, which is considerably lower than the usually quoted value of about 300 eV/ μm , namely $80 e^-h^+/\mu\text{m}$.

2.5.2 Energy loss of electromagnetic radiation

Photons interact differently with matter with respect to charged particles because they are either absorbed or they scatter through a given angle. A photon beam is attenuated in matter according to:

$$I = I_0 e^{-\mu x}, \quad (2.32)$$

where I_0 is the initial beam intensity, I is the attenuated beam intensity after a distance x , and μ is the *mass attenuation coefficient*. It is related to the cross sections of the different possible interaction processes:

$$\mu = \frac{N_A}{A} \sum_i \sigma_i, \quad (2.33)$$

where σ_i is the cross section of the process i , A is the atomic weight of the absorbing material and N_A is the Avogadro number. The mass attenuation coefficient is given in units of g cm^{-2} .

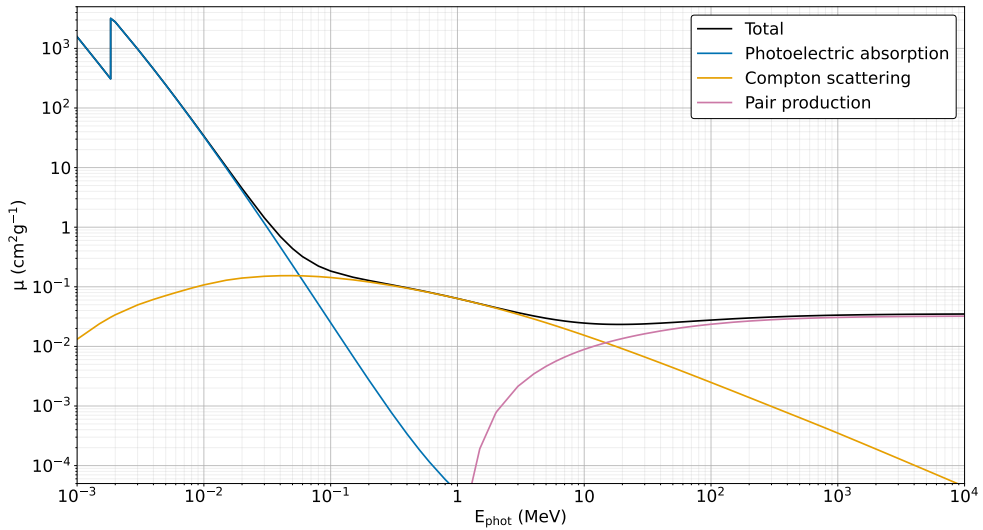


Figure 2.7 Photon attenuation coefficient of silicon as a function of the incident photon energy [33]. The attenuation coefficients for photoelectric absorption, Compton scattering and pair production are represented.

Among all, the most important interaction processes are:

- *Photoelectric interaction*, where an atomic electron absorbs an incident photon with the subsequent release of the electron from the atom. The energy of the

outgoing photoelectron is equal to the energy of the absorbed photon minus the binding energy of the electron. The photoelectric effect cross section dominates at low photon energy (i.e. $E_{phot} \ll 1 \text{ MeV}$);

- *Compton scattering*, consisting in the inelastic scattering of photons on free electrons. In matter, however, electrons are bound, and very forward scattering is suppressed as the energy transfer would not be enough to exceed the electron binding energy. To properly take this aspect into account, Compton scattering form factors [34] are used for calculations in simulation packages. The Compton scattering dominates at intermediate photon energy (i.e. $E_{phot} \approx 1 \text{ MeV}$);
- *Pair production*, involving the transformation of a photon in an electron-positron pair in the Coulomb field of a nucleus. For the process to be energetically possible, the incident photon must have an energy $E_{phot} > 2m_e c^2 = 1.022 \text{ MeV}$. The pair production cross section dominates at high photon energy (i.e. $E_{phot} \gg 1 \text{ MeV}$).

The dependence of the mass attenuation coefficients in silicon on the incident photon energy is represented in Figure 2.7, where the contributions of photoelectric absorption, Compton scattering and pair production are shown. A more comprehensive review of these and other processes involving electromagnetic radiation can be found in Reference [14].

For the calibration of MAPS devices, X-rays, with energies of few keV, are commonly used since their photoelectric interaction with silicon corresponds to an amount of absorbed energy comparable to the energy loss of a minimum ionizing particle in their thin sensitive volume. Differently than a MIP, though, the photoelectric absorption of an X-ray is a point-like phenomenon, with the formation of the charge cloud in a small spatial region.

2.6 Signal formation

The signal processed by the front-end electronics of a semiconductor detector originates from the motion of charge carriers inside the semiconductor depleted volume. Electron-hole pairs induce a given amount of charge on the electrodes, and their drift in presence of an electric field changes the amount of induced charge, producing a current signal. The induced current can be calculated analytically by means of the *Shockley-Ramo theorem* [35, 36]. For a detector system composed of n electrodes, the theorem states that the induced current on a generic electrode k is:

$$i_k(t) = -e\vec{v}(t) \cdot \vec{E}_w, \quad (2.34)$$

where $\vec{v}$ is the velocity of the considered charge carrier and e is the elementary charge. $\vec{E}_w$ is known as *weighting field* and describes how a moving charge couples to the examined electrode. It has dimensions of an inverse length. The weighting field corresponds to the electrostatic field in case all charges in the detector are removed, the electrode of interest (usually, the one connected to the front-end electronics) is put at unit potential and all the others are grounded [37].

The weighting field is substantially different from the electric field, as the former depends only on the detector geometry and determines how charge motion couples to a specific electrode, while the latter determines the charge trajectory and velocity. Although not explicitly written, the electric field also enters Equation 2.34. It influences the current signal shape via the charge carrier drift velocity, according to Equation 2.18. Both electron and holes contribute to the induced signal at a given electrode. Since they move in opposite directions and have opposite charge, they induce current of the same polarity. However, since in silicon the mobility of electrons is about three times higher than holes (cf. Section 2.4), the two charge carriers contribute to the total signal with different time scales. The electron's contribution to the induced current is peaked in time after the interaction of the detector with ionizing radiation, while hole's contribution is stretched over a longer time scale.

Similarly to the electrostatic quantities, the weighting field is related to the *weighting potential* ϕ_w according to:

$$\vec{E}_w = -\vec{\nabla}\phi_w . \quad (2.35)$$

The weighting potential describes how a charge at any position couples to a generic electrode k . It corresponds to the electrostatic potential when the electrode k is set to unit potential and the others are grounded. The charge Q_k induced at the electrode k by the charge q moving from position $\vec{x}_1$ to position $\vec{x}_2$ is:

$$Q_k = q (\phi_k(x_2) - \phi_k(x_1)) . \quad (2.36)$$

Examples of weighting potential maps for the MAPS studies in this thesis are provided in Chapter 6. In this section, only the basic concepts of signal induction by moving charges are presented. A wider and more detailed discussion can be found in Reference [38].

2.7 Radiation damage

The damage produced in silicon by ionizing and non-ionizing radiation constitutes a limitation for the operation of silicon detectors in harsh radiation environments, such

as the CERN LHC. The effects of radiation damage will be even more evident after the High-Luminosity upgrade. As discussed in Section 1.1, radiation hardness is a feature of paramount importance in the choice and design of detectors operating at the HL-LHC and at future accelerator facilities.

Two basic radiation damage mechanisms affect silicon detectors: displacement damage and ionization damage.

Displacement damage In case of displacement damage, the silicon atom is dislodged from its lattice site. It mainly depends on *non-ionizing energy loss (NIEL)*, which varies with the mass and the energy of the incident particle. Being an energy loss, the NIEL is expressed in units of $\text{MeV cm}^2 \text{g}^{-1}$. However, only a fraction of the energy loss goes into displacement, with the rest of the energy being dissipated in phonon interactions. The fraction of energy loss contributing to displacement damage describes an experimental function known as *displacement damage function*, and can be seen as a NIEL cross section [39]. It is given in units of $\text{MeV} \cdot \text{mb}$. Since the displacement damage depends on the specific particle type and energy, a scaling model to compare the effect of different radiation is needed. The latter is based on the assumption that the effects of radiation damage scale linearly with the amount of NIEL, irrespective of the primary displacement over energy and space. The scaling procedure is also known as *NIEL hypothesis*⁵. Under this hypothesis, a reference value of 1 MeV neutron equivalent (n_{eq}) has been fixed to $95 \text{ MeV} \cdot \text{mb}$. In the context of LHC and HL-LHC experiments, such as for the ALICE vertex and tracker detector requirements of Table 1.1, the displacement damage caused by a generic radiation field is quantified in units of 1 MeV neutron equivalent fluence, or $1 \text{ MeV } n_{\text{eq}} \text{ cm}^{-2}$. The effects of displacement damage mainly occur in the bulk of the sensor, i.e. in the volume where electron-hole pairs are created. Additional levels, which facilitate the emission or capture of charge carriers and act as trapping centers, form in the forbidden gap. In addition, the effective doping characteristics of the sensor is modified. In particular, irradiated sensors show the formation of negative space charge compensating the initial positive one. Such a change in the space charge, corresponding to a variation in the effective doping concentration, is observed in n-type base silicon. This phenomenon is known as *type inversion* and is more pronounced with higher particle fluence.

The consequences of displacement damage on the behavior of a silicon detector are a

⁵ Although the NIEL scaling represents a powerful method to deal with damage produced by complex radiation fields, for some particles such as protons or electrons an *effective NIEL* model has to be employed to better describe the induced displacement damage [40, 41].

partial or total loss of signal, and an effective change of the depletion voltage of the detector. If the latter is above the break down voltage of the sensor, the detector will have to be operated undepleted.

Ionization damage The ionization damage leads to the concentration of charge carriers generated by ionizing radiation in a specific point of the detector. As seen in Section 2.5, the amount of charge carriers generated by ionizing radiation does not depend on the type of radiation, but changes with the specific absorber. The *Total Ionizing Dose (TID)* is expressed in rad or Gy, with $1 \text{ Gy} = 100 \text{ rad}$.

The effects of ionization damage are more evident at the sensor's surface, where the interface with an oxide (typically SiO_2) is present. Holes reaching the silicon-oxide interface via drift or diffusion can be captured by interface's traps. The positive charge build-up can generate undesired conducting channels in peripheral detector structures or substantially modify the operation of the MOS transistors of the detector's readout electronics.

For MAPS, both damage mechanisms are equally relevant, with displacement damage mainly affecting the sensing element volume and ionization damage influencing the behavior of the integrated circuitry, and in particular MOS transistors. More comprehensive reviews of radiation damage processes in silicon detectors can be found in Reference [39] and Reference [42].

2.8 Time resolution of a silicon detector

As discussed in Section 1.3, silicon pixel detectors operating in future particle physics colliders will have to guarantee a time resolution down to a few tens of picoseconds to match the requirements of the experiments. In other words, the time of a particle hit must be determined with a few tens of picoseconds accuracy.

The time resolution σ_t of a single silicon pixel of a larger matrix depends on several aspects, involving both the actual sensing part and its readout electronics, and can be expressed as [43]:

$$\sigma_t^2 = \sigma_{jitter}^2 + (\sigma_{total \text{ ionization}} + \sigma_{Landau \text{ noise}})^2 + \sigma_{distortion}^2 + \sigma_{TDC}^2 \cdot (2.37)$$

The different terms of Equation 2.37 can be analyzed by referring to Figure 2.8, which represents the schematic block diagram of a generic time-tagging detector. The sensor is modeled as a current generator I_d with a capacitance C_d in parallel. The signal current induced at the collection electrode after the interaction with the incoming

radiation (cf. Section 2.6) is read out by an amplifier stage. The comparator fires if the signal at the amplifier output exceeds the voltage threshold V_{thr} . The comparator output is digitized by a Time-to-Digital Converter (TDC), and the particle hit time is associated to the signal leading edge crossing time. In principle, any effect altering the shape of the signal at the measured threshold voltage V_{thr} deteriorates the time resolution.

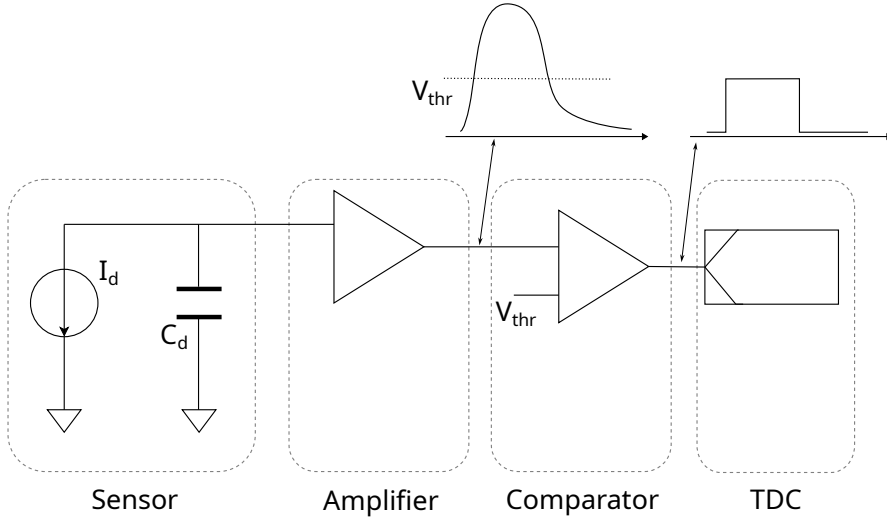


Figure 2.8 Simplified diagram of a time-tagging detector, comprising a sensor block, an amplifier block, a comparator block and a Time-to-Digital Converter (TDC) block. The particle hit time is measured when the signal leading edge crosses the threshold V_{thr} set by the comparator.

The term σ_{jitter} reflects the contribution of the voltage noise σ_n superimposed on the signal. The noise is weighted by the slope of the signal at the comparator threshold according to:

$$\sigma_{jitter} = \frac{\sigma_n}{\frac{dV}{dt}} \cdot \quad (2.38)$$

The signal slope is limited by the slew rate of the amplifier, namely the voltage variation per unit time that the amplifier can handle without distorting the signal. A high slew rate requires a high bandwidth, which in turn increases the noise. The jitter term therefore represents the contribution of the amplifier stage to the overall resolution, and its minimization requires careful electronics design optimization. Although not explicitly present in Equation 2.38, the amplifier power consumption is important for jitter considerations. Typically, high power consumption allows to achieve low voltage

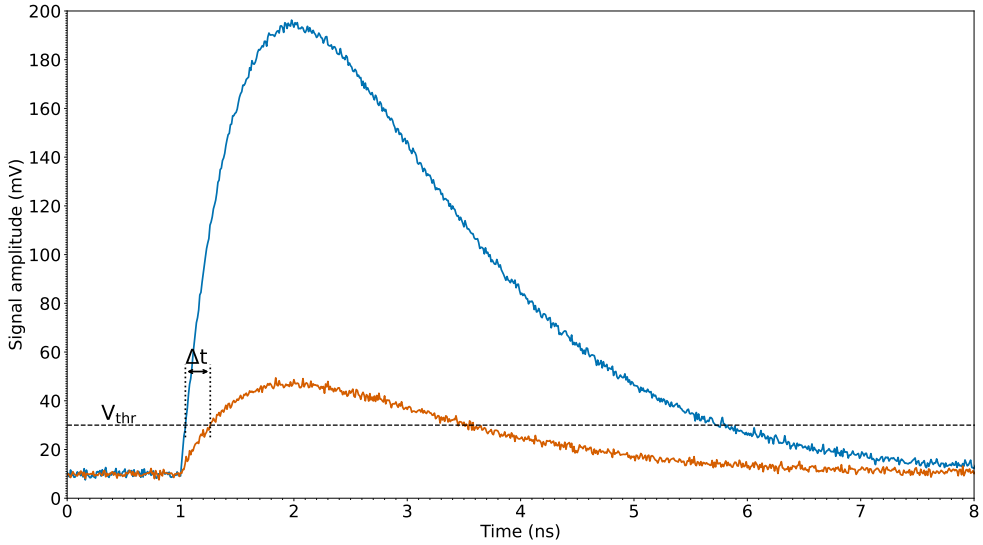


Figure 2.9 Example of signals produced by two particles hitting a detector at the same moment. The fluctuations in the amount of generated electron-hole pairs lead to different signal amplitudes. The signal times are measured when the leading edges cross the threshold V_{thr} . The time walk Δt is the difference between the two measured signal times.

noise without limiting the amplifier bandwidth [44].

The terms $\sigma_{total\ ionization}$, $\sigma_{Landau\ noise}$ and $\sigma_{distortion}$ embody the sensor's contribution to the global resolution.

$\sigma_{total\ ionization}$ and $\sigma_{Landau\ noise}$ are related to the fluctuations in the generation of electron-hole pairs along the particle path within the sensor volume (cf. Section 2.5). The first term represents the fluctuation in the amount of charge pairs generated per event, resulting in variation of the signal amplitude and leading, eventually, to the *time walk* effect. As represented in Figure 2.9, time walk is the deterministic error related to the measurement of the crossing time of signals of different amplitude performed at a fixed threshold. Time walk effects can be mitigated with proper front-end electronics design [37] or can be compensated with offline corrections. The second term represents the fluctuations in ionization density along the track, giving rise to irregularities of the current signal shape (Landau noise). These two effects are related to each other, since, especially for large signals (i.e. the right tail of the energy straggling distribution), non-uniform spatial ionization is observed.

The term $\sigma_{distortion}$ describes the signal shape variation resulting from the particle hit position in the sensor. Equation 2.34 indicates two factors to explain such an effect.

The first is the non-uniformity of the electric field, resulting in non-uniform carrier drift velocity for fields outside the drift velocity saturation regime (cf. Section 2.4). The second is the variation of the weighting field within the sensor volume. Drift velocity and weighting field are therefore critical elements in the design of fast timing sensors.

Finally, σ_{TDC} represents the finite precision with which the TDC can record the comparator firing time in a time bin of width ΔT and the uncertainty $\sigma_{\Delta T}$ of the TDC bin width:

$$\sigma_{TDC} = \sqrt{\left(\frac{\Delta T}{\sqrt{12}}\right)^2 + (\sigma_{\Delta T})^2}. \quad (2.39)$$

All the contributions discussed above limit the resolution of a single pixel only. At chip level, extra terms accounting for pixel-to-pixel fluctuations and TDC's clock distribution and synchronization should be considered. For large detector systems, other scaling effects, such as chip-to-chip fluctuations, come into play.

2.9 Discussion and conclusion

This chapter reviews the working principles of silicon particle detectors. The concepts introduced have a general validity for any silicon sensor technology.

As already discussed in the previous chapter, there are four crucial performance figures for silicon tracking detectors: detection efficiency, position resolution, time resolution and radiation hardness. These are ideally achieved with the lowest possible detector material and power consumption. A wide number of parameters has an influence on the properties of a silicon pixel sensor. A high fill factor is required for a good detection efficiency, and a small pixel pitch plays in favor of the position resolution. Drift based charge collection enhances the radiation tolerance to non-ionizing energy loss, while different components, as seen in Section 2.8, are relevant for the time resolution. In general, thin sensors featuring a high and uniform electric field and a uniform weighting field within the sensitive volume achieve better timing performance. As expected, there is no sensor design yet matching all the aspects listed at the same time.

The ALICE experiment has identified monolithic active pixel sensors (MAPS) as the technology of choice for its tracker and vertex detector because of the excellent detection efficiency and position resolution they can achieve with an extremely low amount of detector material and power consumption. Historically, monolithic pixel sensors have shown limited performance in terms of radiation hardness and time resolution, as they were based on a charge collection process heavily dependent on

diffusion phenomena. Recent developments target the design of monolithic devices able to operate with fully depleted active volume, with a charge collection process based on drift phenomena. In the next chapter, MAPS prototypes developed within the ALICE R&D program are presented, where design modifications enhance depletion, time resolution and radiation tolerance.

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CHAPTER 3

Monolithic active pixel sensors

SILICON pixel detectors are at the heart of the vast majority of particle physics experiments for their high granularity and their capability to cope with high particle rates. All the four experiments operating at the LHC accelerator have adopted such devices for their tracking and vertexing subdetectors. However, while the ATLAS, CMS and LHCb collaborations have installed detectors based on *hybrid silicon pixel sensors*, the ALICE collaboration has selected *monolithic active pixel sensors (MAPS)* to cover the seven layers of its Inner Tracking System 2 (cf. Section 1.5). Figure 3.1 shows a comparison of the schematic cross sections of the two pixel technologies. A hybrid pixel sensor consists of two separate semiconductor layers, one constituting the sensing part and the other hosting the readout electronics. The two layers are connected via bump bonds, i.e. small ($\sim 10\text{ }\mu\text{m}$) solder balls. This layout offers the possibility to design very versatile sensors, since the two layers can be separately optimized according to the application that they target. Even materials different from silicon (like diamond or silicon carbide) can be used as sensing layer. Nevertheless, hybrid sensors suffer from technical limitations related to the thickness of the final device, which become relevant if the track and vertex reconstruction of low momentum particles is targeted, as in the case of ALICE. Moreover, the hybrid technology requires an expensive fine-pitch bump bonding process, which also limits the granularity of the device. Although the hybrid technology can be optimized by thinning down both the sensor and the readout chips, the presence of two separated layers increases the amount of material encountered by a particle traversing the detector, with subsequent higher probability to initiate an electromagnetic or hadronic shower, or to suffer from multiple scattering. In fact, as discussed in Section 1.2, the amount of detector material constitutes a limitation to the achievable impact parameter resolution (cf. Equation 1.7). A different approach is therefore needed to reduce the detector material, especially when it represents one of the main limitations to the physics

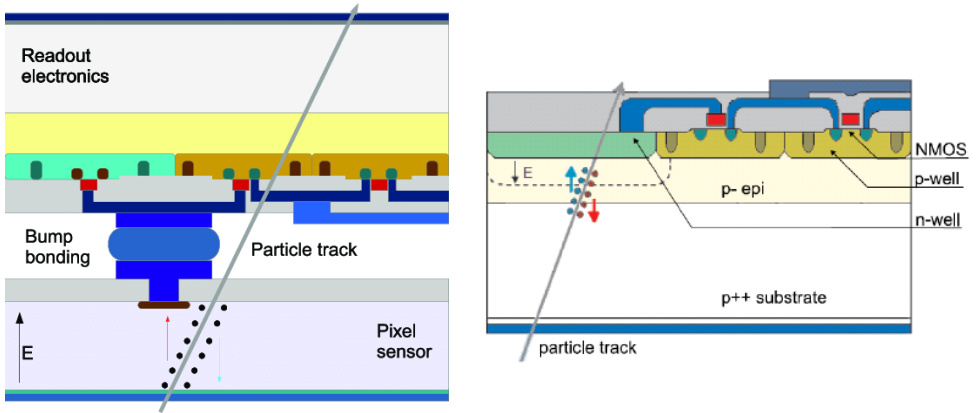


Figure 3.1 Comparison of the cross sections of a hybrid pixel (left panel) and of a monolithic pixel (right panel). The hybrid technology consists in a sensing layer bump-bonded to a layer of readout electronics. The monolithic technology combines the sensor and the readout electronics in a single silicon layer. Not to scale. Figures taken from Reference [1] and Reference [2], respectively.

measurements targeted by the experiment. One way to decrease the detector material is to integrate both sensor and readout electronics on the same silicon die. This is the idea behind monolithic active pixel sensors. MAPS are able to achieve excellent tracking efficiency and impact parameter resolution even with low momentum particles. This last argument explains the choice of the ALICE experiment to opt for such a solution for its tracking detector, together with the relatively limited cost of the monolithic technology.

This chapter describes the operation principles of MAPS and their application to charged particle detection for High-Energy Physics experiments, starting from their original development as image sensors. In particular, the concepts behind the devices designed for the ALICE detector are explained. Finally, the sensor currently installed in the Inner Tracking System 2 (ITS2) and the pixel matrix prototypes produced for the Inner Tracking System upgrade (ITS3) are presented.

3.1 Introduction and background

CMOS monolithic active pixel sensors today represent the third generation of semiconductor devices, on the path of silicon strip and hybrid pixel detectors, applied to the tracking of charged particles for High-Energy Physics experiments. Such

devices, though, have been originally developed as image sensors, and they are still in widespread use in the field of optical imaging for their property of integrating photodiodes and data processing electronics into a single chip. In the early 1990s, monolithic pixel sensors were indeed proposed as a cost-effective alternative to charge coupled devices (CCDs) [3], which were at the time the technology of choice for most imaging applications¹. The main advantage that these devices introduced was the possibility to integrate a significant amount of electronics components on the same chip with reduced costs. In particular, the appealing properties of high integration and low power consumption at reduced manufacturing costs are granted by the adoption of the CMOS process for the sensor production. A brief, non-exhaustive, introduction to CMOS technologies is given in the following section.

A typical CMOS active pixel sensor can be seen as composed of four fundamental building blocks, all embedded in the same silicon chip:

- a pn junction constituting the proper sensing element;
- an in-pixel buffer or preamplifier to process the signal induced at the collection electrode;
- an analog circuitry to reject noise (i.e. a comparator) and to digitize the signal;
- a digital circuitry to pick up and compress the digital signal, which is then sent to the outside world by means of a digital network protocol.

A more in-depth review of different CMOS active pixel architectures can be found in Reference [4].

The direct application of the first samples of CMOS sensors to the detection of charged particles was hindered by the modest detection efficiency that a non-optimized CMOS process would provide. The first generations of CMOS sensors, designed for photon detection, were not suitable for the detection of charged particles. The main limit was the reduced depletion depth (order of 1 μm) of the sensor, which is not suitable for efficient charged particle detection because of a poor signal to noise ratio. Since then, the field has made steady progress through numerous prototyping steps. Finally, charged particle tracking CMOS sensors were derived since the late 1990s by basing the pixel sensing element on a reverse biased pn diode in a relatively thick high-resistivity silicon layer, achievable with more modern CMOS technologies, which yields a higher signal charge. The current signal induced at the collection diode is then processed by the readout electronics integrated into the pixel itself. Such a layout allows to attain a very lightweight, finely segmented (order of 10 μm pixel pitch) sensor with low input

¹ CCDs are still widely used in fields where optical imaging is needed, such as astronomy.

capacitance (order of 10 fF). The impact of the input capacitance on the design and performance of a monolithic sensor is discussed in Section 3.4.1.

3.2 CMOS technology

Complementary Metal-Oxide-Semiconductor (CMOS) is a semiconductor manufacturing technology used in the vast majority of today's integrated circuits, both in the analog and digital domain [5]. As the name suggests, the technology employs MOS transistors to implement any circuit configuration. They are indeed powerful and versatile devices that can be used as signal buffers, amplifiers, current sources and sinks, active loads, switches and capacitors.

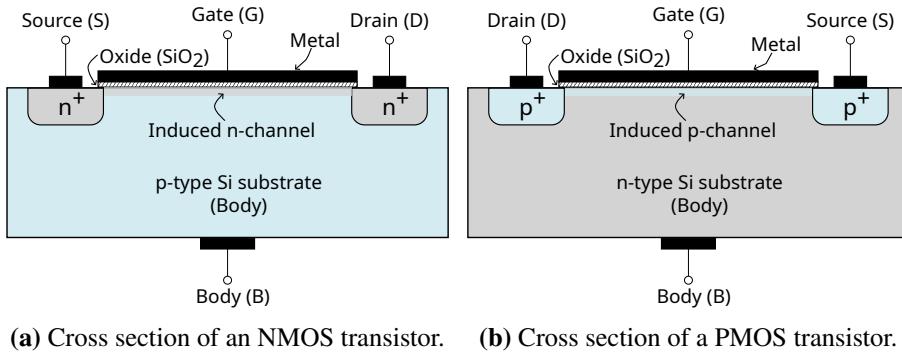


Figure 3.2 Example cross section of an NMOS and a PMOS transistor. Not to scale. Figure adapted from Reference [6].

Figure 3.2 shows the cross section of the two different MOS transistor structures, NMOS and PMOS, respectively. The former is used as a reference to explain the general properties of a MOS device. The nomenclature *Metal-Oxide-Semiconductor (MOS) transistors*, used for this family of devices, refers to their physical structure. An NMOS transistor is fabricated on a p-type silicon substrate, into which two heavily doped n-type regions, depicted in Figure 3.2a with the n^+ label and called *source* and *drain*, respectively, are implanted². A thin layer of the order of few nm of oxide, typically silicon oxide (SiO_2), is grown on top of the substrate, covering the area between the source and drain regions. Finally, a metal layer is deposited on the oxide, forming the *gate* of the device³. Metal contacts are also made for the source, drain

² The notation n^+ indicates heavily doped n-type silicon, while n^- stands for lightly doped material. The same notation is used for p-type silicon, and will be used in the rest of this dissertation.

³ Since the 1970s, the metal has been replaced with heavily doped polycrystalline silicon for its property to withstand higher temperature without reacting with SiO_2 .

and substrate regions, with the latter also called *body*. The application of a positive voltage to the gate terminal with respect to the source generates an effective n-region near the surface of the substrate under the gate. If a voltage between drain and source is applied, electrons flow from drain to source in the induced n-region, also known as *channel*.

Similar considerations hold for a PMOS transistor (cf. Figure 3.2b), since the structure is comparable to the NMOS counterpart, except for the reversed polarity of the semiconductor regions. In particular, the application of a negative voltage to the gate terminal with respect to the source induces a channel where holes can flow if a voltage between source and drain is applied. More detailed considerations on the properties of MOS transistors and on the operations of NMOS and PMOS devices can be found in specialized literature, such as Reference [6].

In the case of a CMOS chip, both transistor polarities are hosted on the same silicon die, opening the way to the design of compact and powerful circuits. Figure 3.3 illustrates how CMOS circuits are fabricated. Devices are built into a common p-type substrate, with thick regions of oxide providing electrical insulation between different transistors. While such a substrate constitutes the body for NMOS devices, dedicated n-type silicon regions, called *n-wells*, host PMOS transistors. The CMOS technology allows to integrate resistors, capacitors and inductors as well.

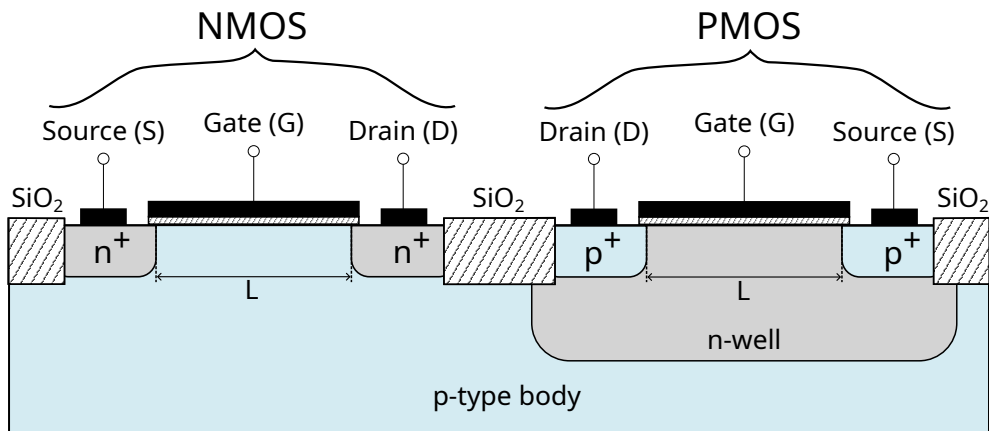


Figure 3.3 Schematic cross section of a CMOS integrated circuit. The PMOS transistor is fabricated into a dedicated n-well. For both transistor polarities, the gate length L is highlighted. The metal contacts of the body of the two devices are not shown. Not to scale. Figure adapted from Reference [6].

The CMOS manufacturing process and design rules, also called *technology node*, are identified with the transistor size. The minimum gate length achievable by a given

process, indicated in Figure 3.3, is also referred to as *feature size*. In general, shorter gates consent the operation of faster transistors, i.e. transistors with larger bandwidth, and allow the design of denser circuits. Newer generations of chips are characterized by smaller technology nodes, and therefore by smaller transistors⁴.

The simplified cross section of a pixel of a standard CMOS image sensor is depicted in the left panel of Figure 3.4. A CMOS manufacturing process typically starts from a very highly doped (i.e. dopant concentration of the order of $1 \times 10^{18} \text{ cm}^{-3}$ or $1 \times 10^{19} \text{ cm}^{-3}$) p-type silicon wafer, also known as *substrate*. A lowly doped p-type *epitaxial layer* is grown on top of the substrate. This layer is a few tens of μm thick and features high resistivity (cf. Section 2.4) because of the relatively high purity of the produced silicon material. The property of high resistivity allows to limit the leakage current between the different structures embedded in the chip. As it will become apparent later, the epitaxial layer constitutes also the sensitive volume of the sensor.

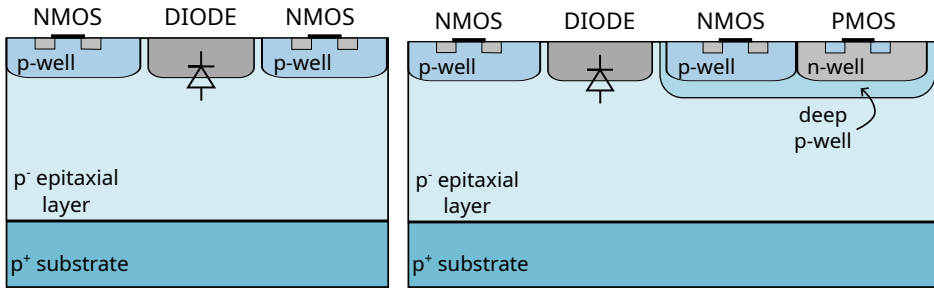


Figure 3.4 Comparison of simplified cross sections of pixels based on standard CMOS process (left) and InMAPS CMOS process (right). In standard CMOS technology, only NMOS transistors are allowed, while the so-called InMAPS technology provides deep p-wells to host PMOS transistors, enabling the realization of in-pixel full CMOS circuitry. Not to scale.

Litographic techniques are employed to introduce differently doped silicon structures in the top few micrometers of the epitaxial layer. These can be added via dopant implantation or diffusion, and their depth and doping concentration vary with the specific CMOS process. NMOS transistors, constituting the in-pixel circuitry, are hosted in p-doped wells, with a dopant concentration typically ranging from $1 \times 10^{16} \text{ cm}^{-3}$ to $1 \times 10^{18} \text{ cm}^{-3}$. A high doping concentration⁵ prevents, on the one hand,

⁴ For recent technology nodes, such as 22 nm, 16 nm, 14 nm, 10 nm, the number is only used to identify a specific generation of chips and does not correspond to the minimum achievable gate length.

⁵ The doping concentration profiles are often unknown, as they vary among manufacturers and are subject to non-disclosure agreements.

the depletion of the well itself and, on the other hand, hinders the charge generated in the epitaxial layer, i.e. the actual signal charge, to diffuse in the p-well, as explained in Section 3.4.2 (cf. Equation 3.2). The sensing element is formed by an n-doped well in the epitaxial layer, behaving as a pn-junction (cf. Section 2.2).

A fully efficient sensor is achievable if the collecting diode is the only pn junction within the pixel. This argument would automatically limit the in-pixel electronics to NMOS transistors only, as the n-well hosting a PMOS would compete with the sensing diode in the charge collection. One way to overcome such a limitation is to apply an additional p-type implantation layer, known as *deep p-well*, which extends the implantation depth of a common p-well. As sketched in the right panel of Figure 3.4, a deep p-well contains both NMOS and PMOS transistors, preventing the latter to collect charge and permitting the implementation of a full CMOS circuitry. For more modern CMOS processes, either deep p-wells or deep n-wells can be generated. Such technologies are also referred to as *InMAPS* or *quadruple well* processes [7].

To complete the manufacturing process, metal layers are deposited on top of the semiconductor structures to provide electrical contacts. These layers constitute the main limitation to the fill factor achievable by imaging sensors employed to detect optical photons, while they barely affect the performance of sensors applied to the detection of minimum ionizing particles, as MIPs can traverse the few micrometers of metal on top of the epitaxial layer.

For detailed discussions on CMOS integrated circuits and CMOS image sensors, one can consult Reference [8] and Reference [9], respectively.

3.3 Monolithic CMOS sensors for High-Energy Physics

Although modern monolithic active pixel sensors for High-Energy Physics have some common characteristics with commercial CMOS imaging devices, they need a specific optimization to be able to satisfy the requirements posed by particle physics experiments. Depending on the application they target, they must meet the following conditions⁶:

- Reliable detection of single particle hits.
- Near 100% detection efficiency over the whole pixel area.
- Position resolution of the order of few micrometers.
- Time resolution down to few tens of picoseconds, if the sensor targets 4D tracking or time of flight applications.

⁶ Specific requirements for the ALICE pixel sensors are reported in Table 1.1 of Section 1.7.

- Low power consumption to reduce the amount of material needed inside the detector to supply power to and to cool down the sensors, for an overall lighter detector with improved impact parameter resolution.
- High radiation tolerance to withstand ionizing dose up to 10 MGy and non-ionizing radiation damage up to an equivalent of 1×10^{17} 1 MeV $n_{eq} \text{ cm}^{-2}$, depending on the experiment and the length of the operation period.

Because of these points, the pixels of a monolithic CMOS sensor for High-Energy Physics can contain several hundreds of transistors for a pixel pitch of at least $10 \mu\text{m}$ while modern imaging sensors typically have matrices with order of $1 \mu\text{m}$ pixel pitches and very few transistors per pixel.

The MIMOSA sensor, based on a standard $0.6 \mu\text{m}$ CMOS process, constitutes the first proposal to apply monolithic active pixel sensors for charged particle tracking in High-Energy Physics [10]. The pixel matrix features square pixels of $20 \mu\text{m}$ pitch, containing only few NMOS transistors for a simple readout scheme. The ULTIMATE chip [11], belonging to the same family of the MIMOSA sensors and produced in $0.35 \mu\text{m}$ CMOS process on a high resistivity, i.e. above $400 \Omega \cdot \text{cm}$, $15 \mu\text{m}$ thick p-type epitaxial layer on highly p-doped substrate, represents the first MAPS installed in a large scale detector, namely the STAR PXL vertex detector at RHIC [12]. For such a sensor, the collection diode is formed by the pn junction created between the epitaxial layer and an n-well region implanted at each pixel. Although operated in reverse bias regime, the epitaxial layer is not fully depleted since the maximum applicable bias voltage is limited to few volts to avoid damaging the thin transistor gates. Electron-hole pairs generated by a charged particle are therefore mostly collected via thermal diffusion, leading to large pixel clusters, collection time of the order of 150 ns and limited radiation hardness to a NIEL damage of the order of 1×10^{12} 1 MeV $n_{eq} \text{ cm}^{-2}$. Despite the satisfactory performances reached by the MIMOSA chip series, these sensors suffer from two main weak points: an in-pixel circuitry limited to NMOS only and a not fully depleted active volume. The first one can be tackled by leveraging InMAPS processes (cf. Section 3.2), such that full CMOS circuits can be integrated within a pixel. The second point requires a thoughtful optimization of the sensor layout in order to concentrate more charge in the seed pixel, namely the pixel with the largest collected charge, and improve the radiation tolerance. Two main design approaches, which distinguish two corresponding families of MAPS devices, can be followed to increase the depletion of the pixels.

High-voltage MAPS (HV-MAPS) adopt CMOS technologies originally used in the power electronics industry, where transistors with thicker gates are able to withstand

higher voltages (above 50 V) than the standard CMOS devices introduced in Section 3.2. Such a design approach targets at the full depletion of the sensitive volume via the sensor operation with high reverse bias voltage (up to hundreds of volts) [13]. To further facilitate a fast charge collection and a high non-ionizing radiation tolerance, a large collection electrode can be employed to obtain more uniform electric and weighting fields, with the penalty of larger junction capacitance. The RD50-MPW series, for which radiation tolerance above $1 \times 10^{15} \text{ 1 MeV n}_{\text{eq}} \text{ cm}^{-2}$ is demonstrated [14, 15], and the CACTUS prototypes, showing a time resolution of 65 ps with on-chip front-end and discriminator [16], are examples of developments implementing the HV-MAPS concepts.

High-resistivity MAPS (HR-MAPS) preserve most of the design features already illustrated for the standard sensor discussed in Section 3.2. However, the usage of ultra-pure epitaxial layers, with doping concentrations reduced by two or three orders of magnitude with respect to a standard CMOS process, allows to extend the depleted volume by keeping low reverse bias voltage. Even if not fully depleted, the sensor benefits of a larger seed signal charge and of an improved radiation tolerance to non ionizing damage of about one order of magnitude with respect to what is achieved by the MIMOSA sensors. Pixels designed with small collection electrodes offer the appealing property of very small junction capacitance (order of 1 fF), at a price of non-uniform electric and weighting fields in the active volume.

HR-MAPS is the approach selected by the CERN EP R&D on monolithic pixel sensors [17] and the ALICE collaboration for the design of the pixel sensors to be installed in the ALICE tracker and vertex detector.

The focus of the remaining sections of this chapter is put on the development lines leading to the design of the MAPS based on a 180 nm CMOS process installed in the current ALICE tracking detector, the ITS2 (cf. Section 1.5), and to the test structures implementing a new 65 nm CMOS process, which are studied in this thesis in view of the application of such a technology for the upgrade of the ALICE tracker, the ITS3 (cf. Section 1.6).

A more complete historical overview of the development of monolithic CMOS sensors for High-Energy Physics can be found in Reference [18].

3.4 TowerJazz 180 nm CMOS imaging technology line

The development of MAPS for the ALICE Inner Tracking System 2 started in 2012, with the study of the charge collection properties and the optimization of the collection diode using small-scale prototypes with analog readout, and the development of the

architecture of the final sensor, namely the *ALPIDE* [19, 20]. To achieve the desired physics performance, the final detector was required to have a reduced material with high granularity, combined with limited production costs to cover an area of about 10 m^2 . Additionally, the design was driven by a maximum tolerable power density of about 50 mW cm^{-2} and tolerance to moderate radiation levels (the requirements for the ITS2 are summarized in Table 1.1). The TowerJazz 180 nm CMOS imaging process⁷ [22] was identified by the ALICE collaboration as the technology to manufacture the pixel sensors for the ITS2, as it provides high-resistivity epitaxial layers (order of $\text{k}\Omega \cdot \text{cm}$) combined with quadruple well technology. It enables full in-pixel CMOS circuitry of 180 nm feature size with up to six metal layers which allow for a high-density, low-power circuitry. Furthermore, the gate oxide thickness of about 3 nm provides a sufficient ionizing radiation tolerance of 100 kGy [23].

This section outlines the working principles of the ALICE CMOS monolithic pixel sensors and introduces the features of the *ALPIDE* chip. Finally, the R&D effort devoted to the development of a HR-MAPS able to be operated as a fully depleted sensor is presented. Many of these concepts are valid also for the pixel sensor prototypes based on 65 nm CMOS technology discussed in the next section.

3.4.1 Sensor design concepts

Monolithic sensors are appealing for the construction of low power, ultra-light tracking and vertex detectors in virtue of the advantages they offer in terms of easier detector assembly, lower material and lower production cost. Radiation tolerance and power consumption are the key features in the design of an inner detector to determine the quality of track and vertex reconstruction based on the measurement of the spatial coordinates of collision products. The main parameters influencing these elements are the charge collection mechanism and the collected charge over input capacitance ratio, respectively.

Charge collection Traditional MAPS collect charge primarily via diffusion. In this case, the collection time can take up to several hundreds of nanoseconds as there is no net force acting on the charge carriers, which "randomly" walk towards the collection electrode. Long collection times increase the probability of charges to be captured by defects or traps. Charge collection based on drift mechanism, on the other hand, pushes the charges towards collection electrodes in times of the order of 1 ns, depending on the thickness of the sensor, and on the shape and intensity of the electric field.

⁷As of March 2020, TowerJazz announced *Tower Semiconductor* as a new brand identity [21].

Since one of the main effects of NIEL damage in silicon is the creation of defects and traps (cf. Section 2.7), it is straightforward to deduce the relation between drift-based collection mechanism and radiation tolerance. Higher non-ionizing radiation tolerance is therefore achieved by sensors based on drift collection mechanism, which is favored in high-purity, depleted silicon volumes. These properties can be achieved by adopting CMOS processes providing higher resistivity epitaxial layers, for which a larger depleted volume is obtained at same reverse bias voltage applied⁸ and a higher charge carrier mobility can be reached. A larger depleted volume brings also benefits in terms of higher signal charge, relevant for the maximization of the charge over capacitance ratio, as described in the following paragraph.

Power consumption The analog power consumption P of a pixel sensor can be related to the signal charge Q over input capacitance C ratio, for a fixed signal to noise ratio⁹ and bandwidth, according to [24]:

$$P \propto \left(\frac{Q}{C} \right)^{-m} \quad \text{with } 2 < m < 4. \quad (3.1)$$

The parameter m included in the expression above depends on the operation regime of the input transistor. The meaning of equation 3.1 can be understood with the following qualitative argument: for a fixed signal charge Q , the factor Q/C can be seen as the voltage signal amplitude at the collection electrode terminal. If the pixel input capacitance, which is the sum of the junction capacitance of the pixel diode, the capacitive loads introduced by the front-end circuitry at the input node and the stray capacitance of the interconnecting lines, is sufficiently small, even for limited collected charge, a satisfying signal to noise ratio can be achieved without signal amplification, with subsequent elimination of the power consumed by an amplifier stage. A low power consumption implies a reduced detector material, as fewer cables are required to bring in the power and the cooling to dissipate it, and therefore a better impact

⁸ For simplicity, this can be explained by considering the expression of the depleted region in a reverse biased planar pn junction (cf. Equation 2.14). In a standard CMOS process, the doping concentration N_d of the n-well collection electrode is much higher than the doping concentration N_a of the epitaxial layer, hence $N_d \gg N_a$ can be safely assumed:

$$d = x_p + x_n = \sqrt{\frac{2 \epsilon_{Si} (V_{bi} + V_R)}{e} \left(\frac{N_a + N_d}{N_a N_d} \right)} \approx \sqrt{\frac{2 \epsilon_{Si} (V_{bi} + V_R)}{e N_a}} \rightarrow d \propto \sqrt{\frac{1}{N_a}}.$$

The expression above shows that the higher the resistivity of epitaxial layer, i.e. the lower the doping concentration, the wider the depleted volume.

⁹ Under the assumption that the noise is dominated by the thermal noise of the input transistor.

parameter resolution.

The maximization of the Q/C ratio requires the design of sensors with extremely small collection electrodes to minimize the pixel diode junction capacitance, as the latter mostly depends on the size of the sensing electrode.

The silicon pixel sensors designed for the ALICE tracking detector are therefore MAPS with remarkably small collection diodes (order of $1\ \mu\text{m}$ or $2\ \mu\text{m}$) manufactured with a CMOS process based on highly resistive epitaxial layer. The most prominent example of such a family of devices is constituted by the ALPIDE chip, presented below.

3.4.2 The ALPIDE sensor

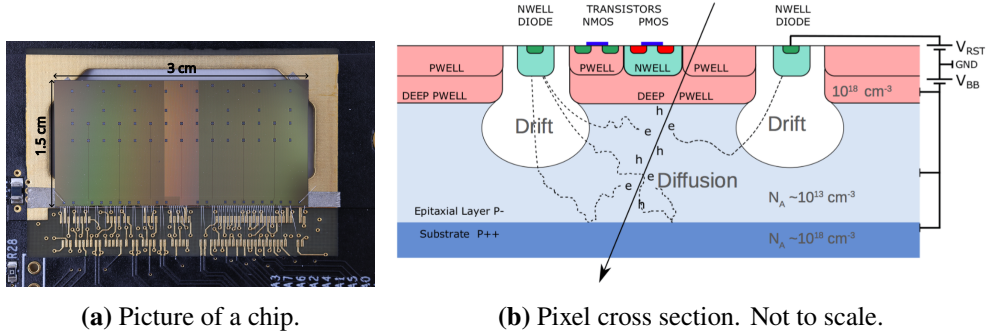


Figure 3.5 Left: Photo of an ALPIDE chip wire-bonded and glued to a carrier card for laboratory testing. Right: Schematic cross section of two ALPIDE pixels traversed by a particle, represented with an arrow. The depleted region is represented with the characteristic bubble shape around the collection electrodes. Not to scale. Figure taken from Reference [25].

The ALPIDE – *ALICE Pixel DEtector* – is the MAPS based on the TowerJazz 180 nm CMOS imaging process developed for the ALICE Inner Tracking System 2. It is a $3\text{ cm} \times 1.5\text{ cm}$ chip containing about half a million pixels, each one measuring $29.24\ \mu\text{m} \times 26.88\ \mu\text{m}$, arranged in a matrix of 1024 columns by 512 rows. Analog biasing, control, readout and interfacing functionalities are implemented in a peripheral region of $1.2\text{ mm} \times 30\text{ mm}$. Figure 3.5a shows a picture of an ALPIDE. The R&D phase was completed at the end of 2016, then the mass production was launched. The chip is manufactured on wafers with high-resistivity ($> 1\text{ k}\Omega \cdot \text{cm}$) p-type epitaxial layer of $25\ \mu\text{m}$ thickness grown on top of a p-type substrate. The substrate can be thinned down, for an overall sensor thickness of $50\ \mu\text{m}$. The sensing element is an

n-well of 2 μm diameter, 3 μm spaced from the p-well hosting the in-pixel circuitry. The pn junction is at the interface between the n-well electrode and the epitaxial layer. Therefore, a small region devoid of charge carriers develops around the n-well diode with a characteristic bubble shape, where the charge produced by incoming radiation is collected via drift. In the remaining part of the epitaxial layer, charge randomly diffuses. At the interfaces between the moderately doped epitaxial layer ($N_a \approx 10^{13} \text{cm}^{-3}$) and the highly doped deep p-well and substrate ($N_a \approx 10^{18} \text{cm}^{-3}$), repulsive potential barriers, created because of the difference in doping concentrations, keep the charge in the epitaxial layer. The magnitude of the potential difference V_b present at such borders can be calculated as [26]:

$$V_b = \frac{k_B T}{e} \ln \left(\frac{N_{a,p^+}}{N_{a,p^-}} \right), \quad (3.2)$$

where k_B is the Boltzmann constant, T the absolute temperature, e the fundamental charge, and N_{a,p^+} and N_{a,p^-} the doping concentrations of the highly doped region and epitaxial layer, respectively. At room temperature, i.e. $T = 300 \text{ K}$, the height of the potential barrier is about 300 mV. Therefore, for a non-irradiated sensor, almost all the signal charge is eventually collected by the pixel where it was generated or by a neighboring one before the end of its lifetime.

The TowerJazz 180 nm CMOS process allows to apply a negative bias voltage V_{sub} to the sensor substrate to extend the depleted volume around the n-well collection diode into the epitaxial layer. It decreases the pixel diode capacitance and, therefore, increases the Q/C ratio. The applicable voltage is experimentally studied to be limited to about -8 V , as breakdown phenomena of pn junctions inside the well structures are observed for higher reverse voltages [19]. To ensure a safe margin, the chip is never operated with a substrate voltage below -6 V . Even with the application of reverse bias, the epitaxial layer is not fully depleted, and diffusion-based charge collection remains a relevant process. However, the operation of a reverse biased ALPIDE sensor is still beneficial, as the application of substrate voltage reduces the input capacitance to a value of about 5 fF. The cross section of an ALPIDE pixel is shown in Figure 3.5b.

The high-density circuitry made possible by the 180 nm CMOS process allows to host into a single pixel a full analog front-end, comprising amplifier, shaper and discriminator stages [27], and digital logic, including three hit storage registers (Multi-Event Buffer) and a pixel mask register. A common threshold level is applied to all the pixels. The front-end and the discriminator are continuously active, with a total power consumption of 40 nW per pixel. The design of the data readout logic is also oriented towards extremely low power consumption. The readout from the matrix is

zero-suppressed and is executed by 512 priority encoding circuits, one per column pair [28]. Such circuits read the pixel buffers and provide the address of the first pixel with a hit (i.e. with higher priority) to the periphery. Thereafter, the storage element of the readout pixel is reset. The hit pixel address is therefore propagated without any clock signal distributed over the matrix, with an overall power consumption density below 47 mW cm^{-2} . A detailed discussion on the ALPIDE chip architecture can be found in Reference [29].

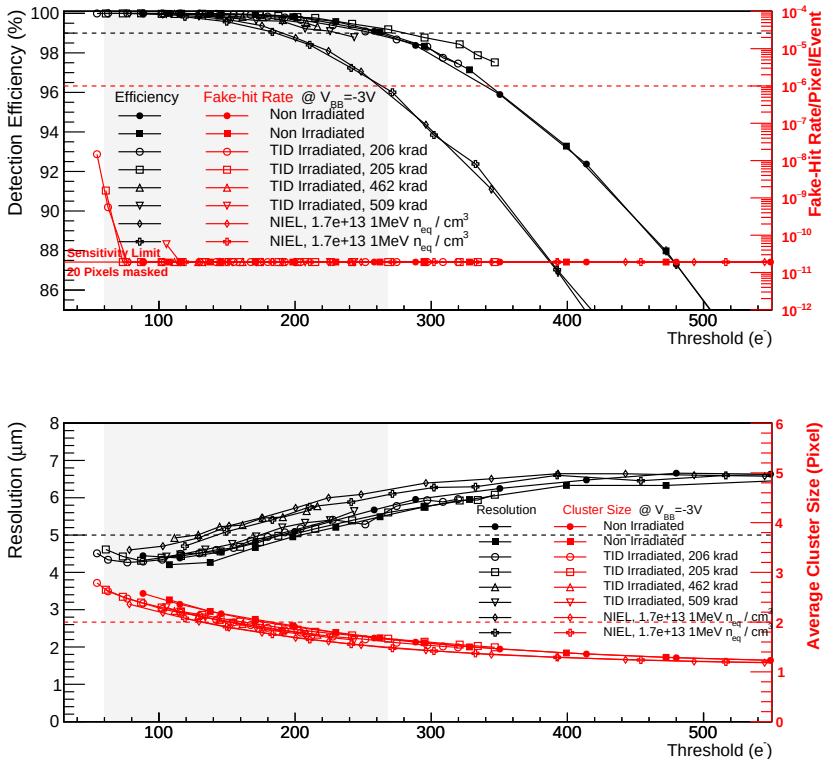


Figure 3.6 Performance of several ALPIDE chips, irradiated and non-irradiated, operated with a substrate voltage $V_{\text{sub}} = -3 \text{ V}$ and measured with a $6 \text{ GeV}/c$ negative pion beam. Top: Detection efficiency (left axis, black curve) and fake-hit rate (right axis, red curve) as a function of the operation threshold expressed in signal charge. Bottom: Spatial resolution (left axis, black curve) and average pixel cluster size (right axis, red curve) as a function of the operation threshold expressed in signal charge.

The performance of the ALPIDE chip in terms of detection efficiency, fake-hit rate, spatial resolution, cluster size and radiation hardness has been validated with

an extensive beam test campaign. In particular, this section presents some of the most relevant results obtained by measuring several ALPIDE samples, irradiated and non-irradiated, with a 6 GeV/ c negative pion beam at the CERN PS facility. The upper panel of Figure 3.6 shows the detection efficiency (left axis) and the fake-hit rate (right axis) as a function of the pixel operation threshold, expressed in signal charge, measured for sensors irradiated for total ionizing dose (TID) and equivalent neutron fluence energy loss (NIEL) up to 500 krad and 1.7×10^{13} 1 MeV n_{eq} cm^{-2} , respectively, and operated with a reverse bias voltage of -3 V. For the same samples, the spatial resolution (left axis) and the average cluster size (right axis) are shown in the lower panel of Figure 3.6. For a large operational range, the measured devices demonstrate a detection efficiency above 99% with less than 1×10^{-10} fake hits per event and a spatial resolution below 5 μm .

The excellent performance demonstrated by the ALPIDE sensor during the R&D phase and summarized in this section is currently proved on a larger scale by the ITS2 detector, where the about 24 000 chips covering the seven layers allow a stable operation of the tracking system with less than 1% loss of acceptance due to errors.

3.4.3 CMOS process optimization

Despite the full detection efficiency and spatial resolution below 5 μm achieved with a power consumption density below 47 mW cm^{-2} , even after irradiation up to 500 krad and 1.7×10^{13} 1 MeV n_{eq} cm^{-2} , the sensor layout adopted for the ALPIDE is not suitable for applications where high radiation load is foreseen or where fast timing capabilities are needed. The main limitation of the TowerJazz 180 nm CMOS imaging process is, in fact, the unfeasibility to operate a fully depleted sensor, even with the application of reverse bias voltage. In the standard TowerJazz 180 nm CMOS process (cf. Figure 3.7), the junction is located at the interface between the collection electrode and the epitaxial layer. The depletion therefore expands from the electrode into the epitaxial layer with increasing reverse bias, but the depletion region is confined by the low resistivity substrate and deep p-well. A larger collection electrode would facilitate the depletion over the full pixel volume, however it would penalize the Q/C factor, as it would increase the pixel input capacitance. Given this constraint on the collection electrode size, other solutions were found to achieve full depletion.

The optimization of the sensor design based on the TowerJazz 180 nm CMOS technology started as a side development of the ALICE collaboration for the ALPIDE sensor [31]. The strategy to obtain a full depletion of the sensitive layer without penalizing the pixel input capacitance foresees to move the junction away from the

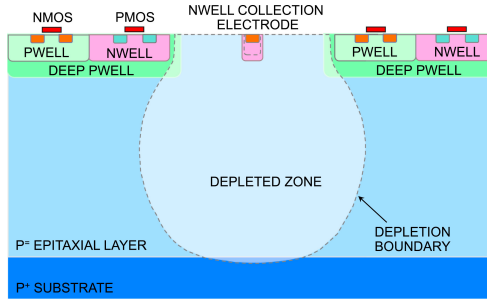


Figure 3.7 Cross section of a pixel implemented with the standard TowerJazz 180 nm CMOS process. Not to scale. Figure taken from Reference [30].

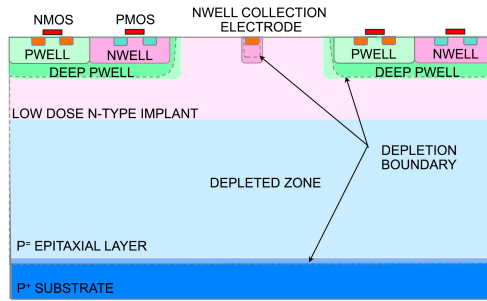


Figure 3.8 Cross section of a pixel implemented with the modified TowerJazz 180 nm CMOS process: a low dose n-type implant underneath the collection electrode is added with respect to the standard process (cf. Figure 3.7). Not to scale. Figure taken from Reference [30].

collection electrode. As shown in Figure 3.8, the implementation consists in the addition of a low dose n-type implant underneath the collection electrode, in order to realize a planar pn junction deep down the epitaxial layer as wide as the whole pixel surface. Moreover, a pn junction is present as the interface between the deep p-well and the n-type implant. The extra n-type implant combined with a reverse bias voltage of few volts makes possible to obtain full depletion of the sensitive volume and to attain a pixel capacitance of the order of few fF at the same time. The boundaries of the depleted region are set by the substrate and the deep p-well. This design has the additional advantage of not requiring any layout modification of the in-pixel circuitry, as the size of the deep p-well is not impacted.

The effort towards an optimization of the design of HR-MAPS with small collection electrodes triggered other parallel developments in the same technology, besides the one led by the ALICE collaboration. The ATLAS collaboration studied the

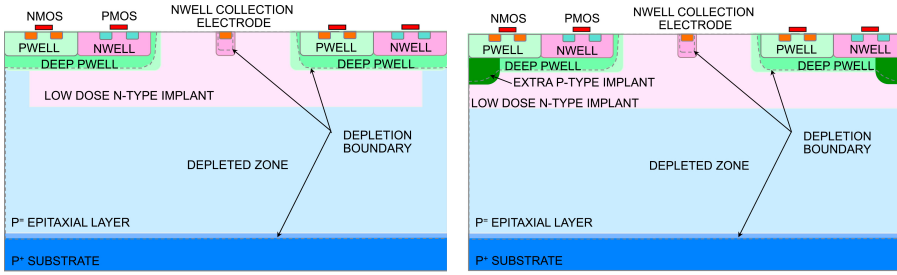


Figure 3.9 Proposed concepts to increase the lateral component of the electric field at the pixel border. Left: Cross section of a pixel with a gap in the low dose n-type implant. Right: Cross section of a pixel with an additional p-type implant below the deep p-well. Not to scale. Figures taken from Reference [30].

radiation tolerance of monolithic pixel sensors based on the modified TowerJazz 180 nm CMOS process with a family of test structures called MALTA (*Monolithic from ALice To Atlas*) [32]. The performance of the MALTA prototypes was studied after irradiation up to a NIEL level of $1 \times 10^{15} \text{ 1 MeV n}_{\text{eq}} \text{ cm}^{-2}$. With such a radiation load, detection efficiency loss at the pixel corners was observed [33]. The reason for such an inefficiency was investigated with three-dimensional simulations of the sensor layouts. They revealed that, at the boundary between neighboring pixels, the lateral component of the field is too low (or even absent) to ensure that the charge drifts fast enough before being trapped, in case of consistent radiation damage.

Reference [34] proposes two different approaches to increase the lateral electric field at the pixel border. The two process modifications are depicted in Figure 3.9 and consist in implanting the low dose n-type layer with gaps at the pixel border (left) or adding an extra p-type implant below the deep p-well. Both concepts aim at increasing the lateral component of the electric field at the pixel edge by moving the point with minimum value of the electric field inside the sensor volume. As a consequence, the field starts to bend towards the collection electrodes deeper in the silicon, reducing the drift path and hence the charge collection time. Sensor prototypes implementing both processes showed a recovered efficiency over the full pixel surface after a NIEL damage of $1 \times 10^{15} \text{ 1 MeV n}_{\text{eq}} \text{ cm}^{-2}$ [35].

The CMOS process modifications outlined in this section for the 180 nm CMOS technology are applied also for the 65 nm CMOS technology, discussed in the next section, with some further improvements. Three different pixel design are implemented for the first chip submission in 65 nm CMOS technology: the pixel design without deep n-well implant (cf. Figure 3.7), also referred to as *standard process*, the one with

a blanket deep n-well implant (cf. Figure 3.8), also referred to as *modified process*, and the one with a gap in the deep n-well implant near the pixel border (cf. left panel of Figure 3.9), also referred to as *modified with gap process*.

3.5 TPSCo 65 nm CMOS imaging technology line

After the success of the ALPIDE and the ALICE Inner Tracking System 2 (ITS2), further developments on MAPS are needed to meet the more stringent requirements posed on silicon pixel sensors for the next upgrade of the ALICE tracking detector, the ITS3, planned during the next Long Shutdown period of the LHC (July 2026-July 2030, cf. Section 1.1). The CERN Experimental Physics R&D department on monolithic pixel detectors [17], in collaboration with the ALICE ITS3 upgrade project, has identified the TPSCo¹⁰ 65 nm CMOS imaging process as the reference technology for the manufacturing of the next generation of monolithic sensors. In this section, the advantages brought by the adoption of a 65 nm CMOS process with respect to a 180 nm CMOS process are listed, and the first *Multi Layer per Reticle run* (MLR1) submission based on the TPSCo 65 nm imaging CMOS technology is introduced. The pixel matrix prototypes belonging to such a chip submission are the subject of the research presented in this dissertation.

3.5.1 Reasons for technology node scaling

Similar to advances in the field of digital electronics or imaging sensors, the adoption of smaller technology nodes (cf. Section 3.2) is beneficial also for the manufacturing of monolithic CMOS sensors for High-Energy Physics experiments. Newer technologies employ smaller transistors for denser and less power consuming sensors for the same performance. In other words, smaller nodes allow the design of sensors characterized by higher granularity, as the same circuitry can fit in smaller pixels, and less material, since the lower power consumption reduces the need of cooling¹¹.

Besides the aspects mentioned above, which have general validity for any application, the technology node scaling brings further specific advantages to High-Energy Physics sensors. Since, to first order, defect buildup in gate oxides scales with the oxide

¹⁰ TowerJazz Panasonic Semiconductor Co., Ltd. (TPSCo) was established as a joint venture of the Tower Semiconductor and Panasonic in 2014. In 2020, the company changed its name to Tower Partners Semiconductor Co., Ltd [36].

¹¹ Smaller CMOS nodes require in principle lower supply voltage. For example, circuits implemented in TowerJazz 180 nm CMOS process operate with a supply voltage of 1.8 V, while those implemented in TPSCo 65 nm need 1.2 V.

thickness, smaller transistor feature sizes are inherently more radiation resistant to ionizing radiation (TID) as they are characterized by thinner gate oxide layers [37]. However, the main reason why the ALICE collaboration has chosen the TPSCo 65 nm CMOS process for the development of the next generation of MAPS is the possibility to access larger silicon wafers of 300 mm, in place of the 200 mm wafers made available by the TowerJazz 180 nm CMOS process. This last point paves the way to the manufacturing of wafer-scale stitched monolithic pixel detectors, which represents one of the design goals of the ALICE ITS3 upgrade (cf. Section 1.6.1).

3.5.2 The MLR1 submission

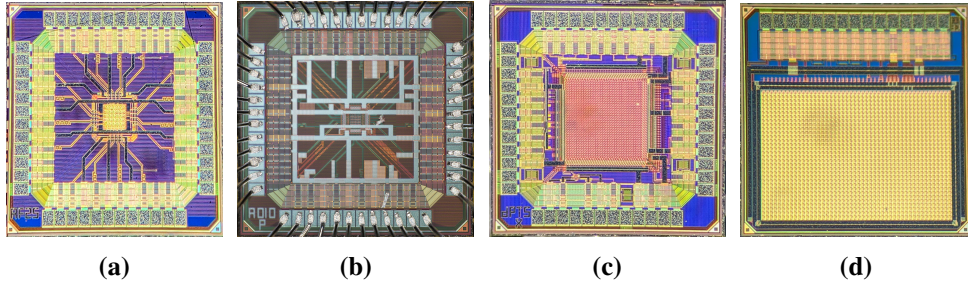


Figure 3.10 Pixel matrix prototypes implemented on the first MLR1 run: a) Analog Pixel Test Structure with source follower output buffer (APTS-SF); b) Analog Pixel Test Structure with operational amplifier output buffer (APTS-OA); c) Digital Pixel Test Structure (DPTS); d) Circuit Exploratoire 65 nm (CE65).

The MLR1 is the first submission in TPSCo 65 nm CMOS technology. It was produced in summer 2021 and includes circuit prototypes, transistor test structures for radiation hardness evaluation [38] and small pixel matrix test chips. In particular, this thesis focuses on the study of the pixel matrix structures for the validation of the technology in view of its application in future tracking detectors, such as the ALICE ITS3 and beyond.

The four pixel matrix prototypes belonging to the MLR1 submission are shown in Figure 3.10 and are (from left to right): the Analog Pixel Test Structure with source follower-based front-end output buffer (APTS-SF), the Analog Pixel Test Structure with operational amplifier-based front-end output buffer (APTS-OA), the Digital Pixel Test Structure (DPTS), and the Circuit Exploratoire 65 nm (CE65). They all measure $1.5 \text{ mm} \times 1.5 \text{ mm}$.

The first two are analog structures designed with the goal of studying the properties of the pixel sensor design, and therefore implement all the three sensor layouts, i.e.

standard, modified and modified with gap (cf. Section 3.4.3). The difference between the two chips consists in the architecture of the analog front-end output buffer: the APTS-OA is developed to study the timing properties of sensors based on the 65 nm CMOS technology and must therefore allow to access the pixel analog signals without altering them. Both chips feature a matrix of 6×6 pixels, with only the central 4×4 being read out. While the APTS-OA samples are produced with pixels of $10 \mu\text{m}$ pitch only, APTS-SF chips with different pixel pitch (from $10 \mu\text{m}$ to $25 \mu\text{m}$) are available to study the effect of the pixel size on the analog performance of the sensor.

The DPTS features a matrix of 32×32 modified with gap pixels of $15 \mu\text{m}$ pitch. Every pixel is provided with a complete front-end, comprising an amplifier and a discriminator, and a global digital readout logic reads out the entire matrix. This test structure is designed to validate the performance of both the sensor and of a novel asynchronous readout architecture (cf. Chapter 7).

Finally, the CE65 is an analog structure with a rolling shutter-based readout.

The MLR1 submission brings forward the effort to optimize the technology for ionizing particle detection initiated with the TowerJazz 180 nm process. The submission was produced in four so-called process splits, namely four wafers where gradual modifications of the doping levels of various implants were implemented, from the standard process to the most optimized [39]. While an experimental validation of the properties of the four process splits was conducted within the APTS-SF characterization campaign, the work presented in the research part of this thesis focuses on the study of sensors based on the process split expected to yield the best results.

The APTS-OA and DPTS chips are discussed in the next chapters. Further discussions and results on the APTS-SF and CE65 prototypes can be found in Reference [40] and Reference [41], respectively.

3.6 Discussion and conclusion

After having established themselves as reference technology in the optical imaging sector, monolithic active pixel sensors are becoming increasingly popular as an alternative to hybrid pixel sensors also in High-Energy Physics. The availability of modern CMOS manufacturing processes allows to implement high-density in-pixel circuitry in fully efficient sensors with low material and low power consumption.

In the development of new CMOS monolithic sensors for future particle physics detectors, and in particular in view of the ALICE ITS3 upgrade, the TPSCo 65 nm CMOS imaging technology was selected as a technology candidate. The first run based

on such a technology, MLR1, contains several pixel matrix test structures implementing various pixel sensor designs. The APTS-OA and DPTS prototypes are investigated in detail to validate the properties of monolithic sensors in 65 nm CMOS technology in terms of detection efficiency, spatial resolution, time resolution and radiation hardness against the ALICE ITS3 requirements, and in view of an application of the technology for other future detectors, such as ALICE3.

The next chapters present the studies of the test structures mentioned above, divided between the experimental characterization in laboratory and in minimum ionizing particle beam facilities, and the modeling of the device physics with Monte Carlo simulations, with a focus on the optimized sensor layout giving the best results in terms of full depletion and time resolution.

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PART II

Research

“In whatsoever mode, or by whatsoever means, our knowledge may relate to objects, it is at least quite clear that the only manner in which it immediately relates to them is by means of an intuition. To this as the indispensable groundwork, all thought points. But an intuition can take place only in so far as the object is given to us. This, again, is only possible, to man at least, on condition that the object affect the mind in a certain manner. The capacity for receiving representations (receptivity) through the mode in which we are affected by objects, objects, is called sensibility. By means of sensibility, therefore, objects are given to us, and it alone furnishes us with intuitions; by the understanding they are thought, and from it arise conceptions. But a thought must directly, or indirectly, by means of certain signs, relate ultimately to intuitions; consequently, with us, to sensibility, because in no other way can an object be given to us.”

Immanuel Kant, *Critique of Pure Reason*

CHAPTER 4

Analog Pixel Test Structures in 65 nm CMOS process

THE Analog Pixel Test Structure Operational Amplifier (APTS-OA) is one of the pixel matrix prototypes produced in the MLR1 submission (cf. Section 3.5.2). It was designed to study the properties of monolithic active pixel sensors based on the 65 nm CMOS imaging technology by directly accessing their signals. This chapter gives an overview of the prototype first, together with the readout system and the experimental setups developed to carry out the measurement campaign. Then, the sensor characterization in terms of charge collection, input capacitance, noise figures and energy straggling is discussed.

4.1 Sensor technology

The effort to optimize the CMOS process to improve the radiation hardness and time resolution of monolithic pixel sensors, started with the 180 nm CMOS technology (cf. Section 3.4.3), has been carried out also with the 65 nm CMOS imaging process, with different sensor layout variants produced. As such, the APTS-OA prototypes feature three diverse pixel designs: one based on a typical CMOS process for imaging sensors, also known as *standard* process, and two based on an optimized CMOS process aimed at enhancing the charge collection properties of the sensor, namely the *modified* and *modified with gap* processes. The cross sections of the three pixel variants are shown in Figure 4.1.

In the TPSCo 65 nm CMOS process, the high-resistivity p-type epitaxial layer is nominally 10 μm thick. It is grown on a low-resistivity p-type substrate. The sensing electrode is a low-resistivity n-well of 1.14 μm diameter placed in the center of the pixel at 1.93 μm distance from the p-wells, hosting the transistors constituting the

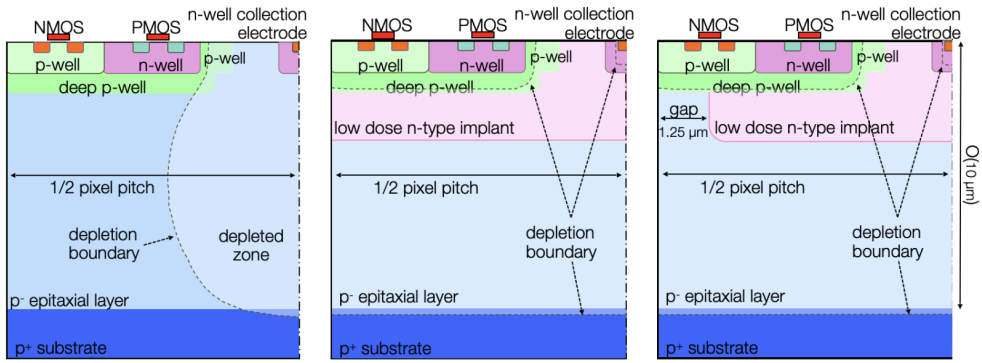


Figure 4.1 Schematic cross section of the three pixel design variants of the APTS-OA. From left to right: standard, modified (low dose deep n-type implant), and modified with gap (low dose deep n-type implant with a gap at the pixel's edges). Only half of the pixel cross section is shown for each variant. Not to scale. Figure taken from Reference [1].

front-end circuit.

In the standard design (left side of Figure 4.1), the junction is at the collection electrode and the depletion region extends into the epitaxial layer with a characteristic bubble shape. Despite the application of reverse bias to the sensor, no full depletion of the epitaxial layer is achievable. Outside the depleted region, the charge collection happens mostly by diffusion, with subsequent enhancement of the charge sharing with neighboring pixels and degradation of the charge collection speed and uniformity.

For the APTS-OA sensors, the pixel pitch is $10\text{ }\mu\text{m}$. The high ratio between pixel pitch and epitaxial layer thickness makes the adoption of the process modification, aiming at fully depleting the epitaxial layer, even more crucial.

The modified design (center of Figure 4.1) extends the depletion region by adding a low-dose n-type blanket below the collection electrode. In this way, a junction as wide as the pixel pitch is present deep in the sensor. Furthermore, another junction is present at the boundaries of the deep p-well, opening the way to a full depletion of the epitaxial layer with the application of reverse bias voltage.

The modified with gap design (right side of Figure 4.1) differs from the modified one because of a cut of $1.25\text{ }\mu\text{m}$ applied at the edges of the low-dose n-type blanket. According to simulations performed for sensors based on the 180 nm CMOS technology [2], this design feature increases the lateral component of the electric field, allowing charges generated at the pixel edges to swiftly drift towards the electrode, resulting in decreased charge sharing and improved charge collection speed and uniformity.

The investigation of the properties of the three pixel variants is conducted together with the characterization of the APTS-OA prototypes. The results and related discussions are presented in this and in the next chapter.

4.2 The Analog Pixel Test Structure

The goal of the APTS prototype is to study in detail how signals develop in sensors implemented in TPSCo 65 nm CMOS imaging process. It is a $1.5\text{ mm} \times 1.5\text{ mm}$ chip featuring a matrix of 6×6 squared pixels with $10\text{ }\mu\text{m}$ pitch (cf. Figure 4.2). Only the central 4×4 pixels are connected to readout circuitry, as the surrounding ones are left as dummy pixels to reduce the electric field distortion effects that may occur at the edges of the matrix.

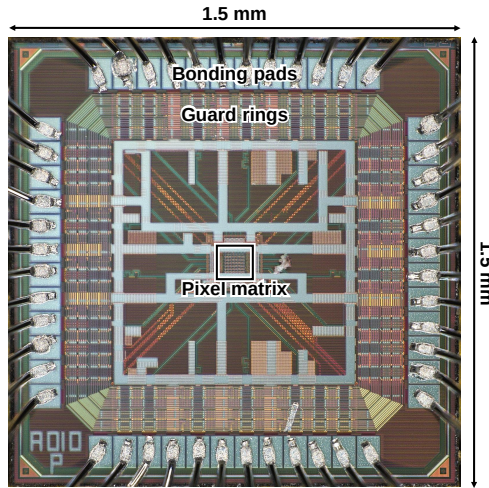


Figure 4.2 Picture of an APTS-OA chip taken under the microscope. Figure taken from Reference [1].

The signals induced at the collection electrode of each one of the central 4×4 pixels are directly buffered to analog output pads. This allows the simultaneous off-chip visualization and acquisition of analog signals from all the pixels. The remaining available chip interface pads are used to provide bias currents and voltages to the pixel matrix.

The pixel front-end schematic is shown in Figure 4.3. The fundamental idea of such a circuit is to exploit the pixel capacitance as an amplifier for the signal induced at the sensing electrode. With an n-well collection electrode, the collected charge Q_{coll}

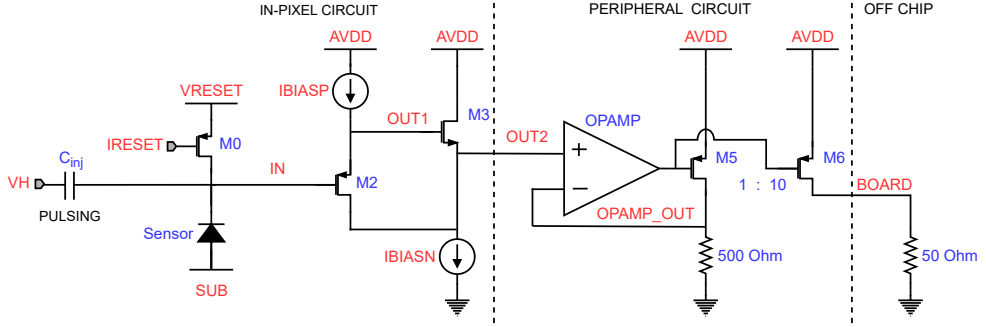


Figure 4.3 APTS-OA front-end circuit schematic. The in-pixel circuitry includes a pulsing injection capacitance C_{inj} , the reset system and the first stage of the output signal buffer. The second stage of the buffer circuit, implemented with an operational amplifier (OPAMP), is placed in the periphery of the pixel matrix. Figure taken from Reference [1].

induces a negative voltage drop V_{in} at the input node (with label IN in Figure 4.3):

$$V_{in} = \frac{Q_{coll}}{C_{in,tot}}, \quad (4.1)$$

where $C_{in,tot}$ is the total input node capacitance responsible for the signal charge to voltage conversion. Its value is given by the sum of several terms, including the pixel diode capacitance. The different terms contributing to this capacitance and their evaluation are discussed in Section 4.8. Thanks to the tiny pixel capacitance of the order of few fF, the expected voltage signal produced by a minimum ionizing particle hit is of the order of 10 mV¹. A signal of similar amplitude is reasonably accessible for further processing without the need of being amplified. Thus, the small input capacitance, characteristic of the above mentioned CMOS processes, eliminates the requirement of an active amplifier in the circuit front-end, with a subsequent reduction in the design complexity and in the power consumption of the device.

The voltage level at the input node must be restored to the nominal operation value

¹ For instance, by considering the average $50 e^- - h^+$ pair generated per μm trajectory in silicon of thickness $d = 10 \mu\text{m}$ by a minimum ionizing particle of charge $Z = 1$, the voltage drop V_{in} at the sensing node for a pixel with total input capacitance $C_{in,tot} = 5 \text{ fF}$ is:

$$V_{in} = \frac{50 e^- / \mu\text{m}}{C_{in,tot} \cdot 6.24 \frac{e^-}{\text{mV} \cdot \text{fF}}} \cdot d = 1.60 \frac{\text{mV}}{\mu\text{m}} \cdot d.$$

This translates in an average signal of about 16 mV for a 10 μm thick sensitive silicon volume.

once the signal has been read out. This task is accomplished by the PMOS transistor M0, which, in case of a particle hit and subsequent voltage drop, is biased to provide the current I_{reset} , larger than the sensor leakage current. In absence of a particle hit, the transistor M0 only has to compensate for the sensor's leakage current, and it switches its operation regime to the so-called linear-region. As a consequence, the nominal voltage level at the input node is close to the transistor M0 source voltage V_{reset} ².

To reverse bias the sensor, the pixel substrate or the p-well must be brought at lower potential with respect to the n-well electrode or, vice versa, the electrode must be brought at higher potential than the pixel substrate and the p-well. This is achieved by applying negative V_{sub} and V_{pwell} voltages with respect to the chip voltage reference. In practice, for all the measurements presented in the following sections, V_{sub} and V_{pwell} are always kept at the same potential as they are shorted off-chip. Hereafter, V_{sub} will be mentioned to indicate the sensor reverse bias. Since the V_{pwell} can be brought down to a maximum of -6 V before incurring in breakdown phenomena, the APTS-OA prototypes were always operated with V_{sub} and V_{pwell} voltages within -4.8 V , to preserve a safe operation margin. It is also worth to highlight that the V_{reset} has an influence on the reverse bias condition. A higher V_{reset} has the effect of pulling up the n-well electrode with respect to the substrate, resulting in an enhanced reverse bias of the pixel diode.

A pulsing circuitry, implemented to test the response of the front-end circuit when charge is injected at the input node, is also integrated in the pixel matrix. It consists of a square waveform generator of amplitude V_h connected to each pixel input node via an injection capacitance C_{inj} , having a nominal value of 242 aF [4]. The voltage V_h is provided by an external reference to the interface pad and can be up to 1.2 V . The charge Q_{inj} injected in the pixel front-end circuit is³:

$$Q_{\text{inj}} \simeq V_h \cdot C_{\text{inj}} . \quad (4.2)$$

To properly access the details of charge collection properties of the sensors, the pixel front-end electronics must have a bandwidth large enough to alter the signals induced on the collection electrode as little as possible. To achieve this, a buffering chain connecting the pixel to the readout system is needed. The role of the buffer is to decouple the extremely low capacitance at the pixel sensing node from the

² The actual reset current provided by M0 is of the order of 100 pA thanks to a current mirror [3] (not represented in Figure 4.3) with a current ratio of $1/10^4$.

³ As discussed more in detail in Section 4.8.1, Equation 4.2 represents a good approximation of the injected charge under the assumption that the injection capacitance C_{inj} is small with respect to the total input node capacitance $C_{\text{in,tot}}$.

capacitance of the readout system that would attenuate the signal amplitude by several orders of magnitude. In particular, for the APTS-OA structures, the buffer circuit is partially implemented inside the pixel matrix and partially in the pixel matrix periphery (cf. Figure 4.3). The pixel collection electrode is directly connected to the gate of the PMOS transistor M2, operated in source-follower configuration [3]. The buffered signal is then fed into the gate of the NMOS transistor M3, again operated as a source-follower. The currents I_{biasp} and I_{biasn} are the biasing currents of the PMOS and NMOS source-follower transistors, respectively. The peripheral buffer circuit connecting the pixel to the output pad is implemented with an Operational Amplifier (OPAMP) in voltage buffer configuration. The off-pixel OPAMP allows to read out the pixel signal on a $50\ \Omega$ impedance with no degradation of the signal bandwidth. This opens the possibility to read out the pixel signals with a large bandwidth oscilloscope, allowing the study of the sensor charge collection process via direct acquisition of the analog signals. Further details on the front-end implementations are discussed in References [5, 6].

The actual pixel signal measured by the readout system does not correspond to the signal induced at the input node because of the non-unitary gain g of the buffer chain. Therefore, with reference to Equation 4.1, the signal V_{board} measured on the output $50\ \Omega$ impedance is:

$$V_{board} = g \cdot V_{in} = \frac{g}{C_{in,tot}} \cdot Q_{coll} . \quad (4.3)$$

According to the circuit simulations, the buffer chain contributes with a gain of the order of 0.7 to the measured amplitude signal with negligible signal speed degradation [5].

The parameters of the sensor and of the front-end circuit implemented in the TPSCo 65 nm CMOS imaging process introduced in this section have been experimentally studied and optimized by probing the circuit response to charge injection and are shown and discussed in the next sections.

4.3 Readout system

The readout system designed for the operation of all the different pixel matrix prototypes produced within the MLR1 submission (cf. Section 3.5.2) consists of an FPGA-based data acquisition (DAQ) board, common for all the chips, and a so-called proximity board, specific to the operated chip.

The DAQ board, powered at 5 V, provides a USB interface for direct connection with a DAQ computer. It has I/O trigger and busy channels, for synchronized operations with other devices, and connection to sensor's p-well and substrate for reverse biasing. The

APTS-OA-compatible proximity board is equipped with Analog-to-Digital Converters (ADCs) for pixel signal readout and Digital-to-Analog Converters (DACs) to provide bias voltages and currents to the chip. More details on the boards' functionalities are available in Reference [7].

Finally, the carrier card, onto which the APTS-OA chip is glued and bonded, hosts 4 high bandwidth *SubMiniature version A* (SMA) connectors, soldered on the output lines of the central 4 pixels of the matrix, to allow the readout of their signals with a high bandwidth, high sampling frequency oscilloscope. The remaining external 12 pixels of the matrix are connected to the 4 MSa/s sampling rate ADCs of the proximity board. All the 16 pixels of the matrix are always simultaneously read out.

The system described above is shown in Figure 4.4.

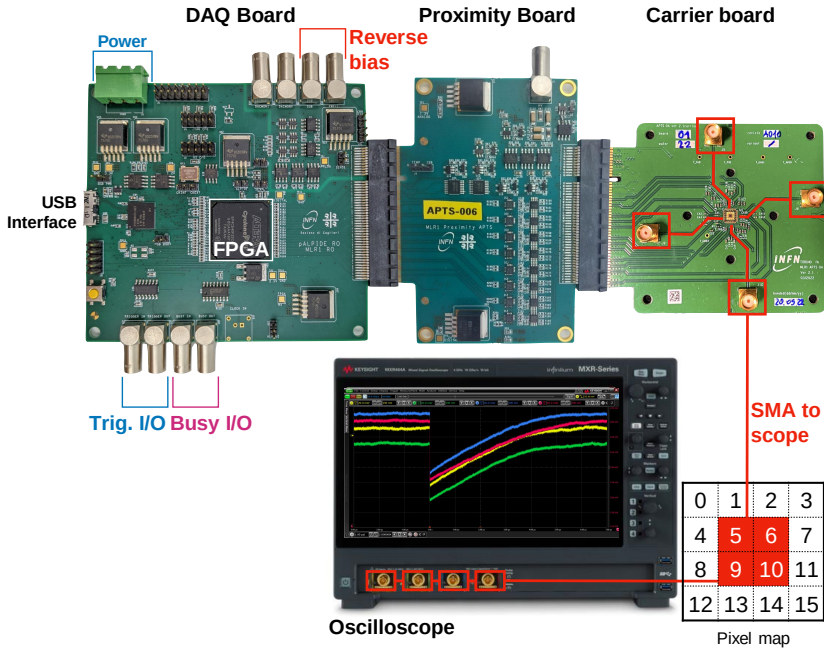


Figure 4.4 Photograph of APTS-OA readout system. From left to right: the DAQ board, the proximity board and the carrier board to which the chip is glued and bonded. The central 4 pixels of the matrix are provided with an SMA analog output, allowing direct connection to a high bandwidth, high sampling rate oscilloscope. Figure adapted from Reference [1].

4.4 Experimental setup

All the test of the APTS-OA prototypes discussed in the following sections are carried out with the readout system described in Section 4.3. For all the measurements performed at Nikhef laboratories, a 4 input channel Keysight MXR404A Infiniium oscilloscope [8], 4 GHz bandwidth and 16 GSa/s sampling rate, is used to read out the central 4 pixels of the matrix, while, for tests with a charged particle beam, a 4 input channels Teledyne Lecroy WaveMaster 813Zi-B [9], 13 GHz bandwidth and 40 GSa/s sampling rate, is employed. The oscilloscope is always operated with $50\ \Omega$ channel's input impedance to preserve the speed of the recorded signals.

The oscilloscope is connected to a DAQ computer controlling the setup via an ethernet connection, digitizes the signals with 8 bit precision and sends data packets through TCP/IP protocol. Signals sampled with the proximity board's ADCs are digitised with 14 bit precision and are sent to the DAQ computer via the DAQ board's USB interface. Given the limited sampling frequency of the ADCs, only the signals acquired with the oscilloscope can be used to precisely study the timing performance of the measured sensor.

Custom-made software allows for setup control and data acquisition during the pixel baseline measurements and the pulsing tests, while for the measurements with radioactive sources and minimum ionizing particle beam, an EUDAQ2-based [10, 11] data acquisition software is used.

4.4.1 Setup for baseline measurement and test pulses

Measuring the baseline voltage of the pixels in the matrix allows, as shown later in Section 4.6.1, to estimate the gain of the buffer stage (cf. Section 4.3). It is also a required step to perform any measurement with test pulses or radioactive source, where the acquisition is triggered when the signal leading edge falls below a selected threshold voltage level. Since no actual signal is induced at the pixel front-end input node, the data acquisition is performed by running both proximity board's ADCs and oscilloscope in self-triggering mode and by stopping them every $\sim 1\text{ ms}$, for data recording. For this measurement only, the oscilloscope's sampling frequency is limited to 4 MSa/s, i.e. the same of the ADCs, and the acquisition window is set to $50\ \mu\text{s}$.

The charge injection via test pulses (cf. Section 4.2) allows to experimentally probe the response of the front-end circuit in different configurations and to calibrate its response. The ADCs acquisition is directly triggered by sending a test pulse, and 100 samples before and 100 samples after every trigger are recorded, for a corresponding acquisition window of $50\ \mu\text{s}$. Regarding the oscilloscope, the trigger threshold level is

set 7.5 mV below the average measured baseline of each one of the connected pixels, in order to catch the leading edge of the signal produced by the injected charge without recording false triggers due to baseline fluctuations. An acquisition window of 50 ns is centered around the oscilloscope's trigger time, as the timing information is provided by the signal leading edge. Examples of an ADC acquired signal and of an oscilloscope acquired one are provided in Figure 4.7 and Figure 4.6, respectively.

4.4.2 Setup for X-ray source tests

Three devices featuring the three different sensor designs were exposed to soft X-rays from a 19 MBq ^{55}Fe radioactive source to calibrate their response and to study the charge collection properties of the different pixel variants.

Since the fine details of the pixel signals are resolved only by the fast oscilloscope, the interesting events⁴ are those inducing a signal in one of the central four pixels. The requirement of having at least one signal from one of the central four pixels in every acquired event is accomplished by setting the oscilloscope threshold level from 10 mV to 15 mV, depending on the operation reverse bias voltage, below the average measured baseline of each one of the connected pixels. The acquisition is triggered when at least one of the channels goes below the threshold. To synchronize the acquisition with the rest of the pixel matrix, the oscilloscope trigger digital output is sent to the DAQ board trigger input, starting the readout of the proximity board ADC sampled frames. The oscilloscope acquisition window is 50 ns wide and is centered around the trigger time, while the ADCs acquisition frame is 200 samples wide, for a corresponding window of 50 μs , and is centered around the time of arrival of the oscilloscope trigger signal in the DAQ board's trigger input channel. This triggering scheme allows to record the full matrix response to ^{55}Fe X-rays. For each measured configuration, about 50 000 triggers are acquired.

4.4.3 Setup for minimum ionizing particle beam tests

The response of the APTS-OA sensors to minimum ionizing charged particles was studied by using 120 GeV/ c positive hadron beam, at the CERN Super Proton Synchrotron (SPS) H6 facility [12].

Particle tracks are reconstructed by fitting the cluster positions on the ALPIDE (cf.

⁴ An event is intended as an interaction between an ^{55}Fe X-ray and the detector under test producing a signal that triggers a data acquisition.

Section 3.4.2) reference planes and on the APTS-SF (cf. Section 3.5.2) plane⁵. The latter has the function of triggering the simultaneous acquisition of all the detectors when a particle traverses its volume, defining, at the same time, a region of interest for the telescope readout, with reduction of the track multiplicity. The telescope is complemented with a low gain avalanche detector (LGAD) [13] of $1\text{ mm} \times 1\text{ mm}$ nominal area, placed downstream of the beam as a timing plane, to provide a reference for assessing the temporal resolution of the APTS-OA detector under test (DUT). The positions of the DUT and of the trigger device are adjustable with movable x and y micro-positioning stages, to guarantee a precise alignment with the tracking planes and the LGAD. A conceptual diagram of the beam telescope is shown in Figure 4.5.

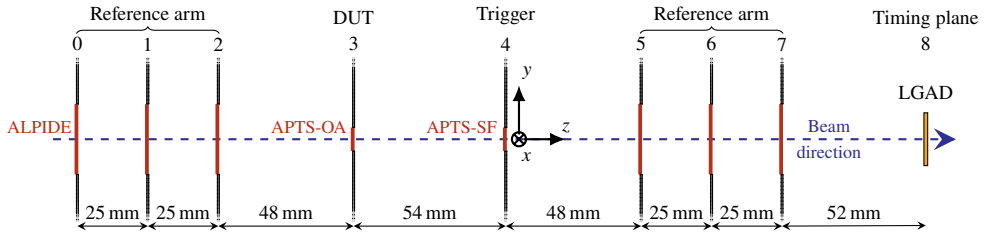


Figure 4.5 Sketch of the beam telescope (not to scale). An APTS-OA detector under test (DUT) is sandwiched between 6 ALPIDE tracking planes. The trigger signal is provided by an APTS-SF device. A low gain avalanche detector (LGAD) placed downstream with respect to the beam provides the time reference to measure the DUT time resolution. Figure taken from Reference [1].

For this specific set of measurements, only three out of the four inner pixels of the DUT's matrix are read out with the fast oscilloscope, as the fourth channel is used to acquire the LGAD's signals. The oscilloscope's acquisition window is $1\text{ }\mu\text{s}$ long. The remaining thirteen pixels of the APTS-OA are read out with the proximity board's ADCs. For every incoming trigger signal, an ADC frame constituted of 200 samples is saved.

A custom-designed trigger logic unit ensures the synchronized acquisition of the DAQ boards of all the telescope planes and of the oscilloscope when a hit is detected by the trigger detector. To avoid limiting the overall telescope readout rate, the oscilloscope is operated in segmented memory acquisition mode, i.e. the captured signals are

⁵ The trigger plane installed in the beam telescope is a modified with gap type APTS-SF of $15\text{ }\mu\text{m}$ pixel pitch, always operated at $V_{\text{sub}} = -1.2\text{ V}$ during the beam test. The device had been already measured with minimum ionizing particle beam, proving a detection efficiency above 99% and a spatial resolution of $3.3\text{ }\mu\text{m}$ at the selected operation condition.

Only tracks hitting the central four pixels of the matrix produce a trigger, as the outer twelve pixels are masked to further reduce the trigger region of interest around the APTS-OA detector under test.

temporarily saved on the instrument disk and then transferred to the DAQ computer in a second moment.

4.5 Signal extraction and data processing

The analog signals acquired from all of the sixteen pixels of the matrix are processed with an offline analysis software. Two different analysis methods are employed for the signals acquired with the fast oscilloscope and for those acquired with the proximity board's ADCs (cf. Section 4.3). This approach properly takes into account the different precision, bandwidth and sampling frequency of the instruments.

Figure 4.6 (top) shows a typical pixel signal read out with a fast oscilloscope in a $10\ \mu\text{s}$ time window. With the pixel collection electrode in a high dose n-well on a p-type epitaxial layer, the drifting charge induces a signal of negative polarity. The electrode voltage level is then restored to its baseline within few μs by the constant current I_{reset} , as explained in Section 4.2. The zoomed panel on the signal leading edge (Figure 4.6, bottom) highlights the characteristic sub-nanosecond time of the voltage drop.

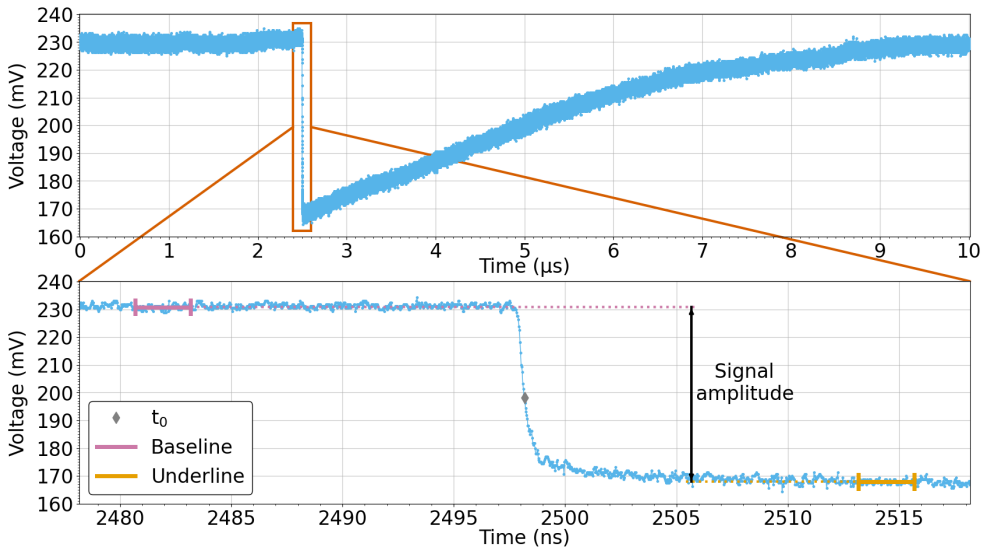


Figure 4.6 Typical signal acquired by a fast oscilloscope displayed in a $10\ \mu\text{s}$ time window (top) and the same signal zoomed in on the signal's leading edge (bottom). On the bottom figure, the sampled points used to measure the baseline (green solid line) and the underline (orange solid line) are highlighted, together with the point t_0 , corresponding to the time when the signal derivative is minimum.

For the analysis of the oscilloscope captured traces, an edge detection algorithm

adapted from Reference [14] is employed to distinguish the signal from the noise and to extract the following figures:

- the time t_0 (highlighted with a gray marker in Figure 4.6), estimated as the sampled point when the signal's derivative reaches its minimum and used as a time reference for the evaluation of the remaining parameters;
- the baseline, estimated as the average of the points sampled in the interval $[t_0 - 17.5 \text{ ns}, t_0 - 15 \text{ ns}]$ (magenta solid line in Figure 4.6);
- the underline, estimated as the average of the points sampled in the interval $[t_0 + 15 \text{ ns}, t_0 + 17.5 \text{ ns}]$ (orange solid line in Figure 4.6);
- the signal amplitude, computed as the difference between the previously defined baseline and underline;
- the signal leading edge time, defined as the difference between the time when the signal reaches 10% of its full amplitude and the time when it reaches 50% of its amplitude⁶;
- the voltage noise, calculated as the root mean square (RMS) of the distribution of the samples found 15 ns before every signal's t_0 , being these the closest sampled points to the signal used to evaluate the baseline.

The parameters chosen to calculate the baseline and the underline are defined with the aim of precisely extracting the signal amplitude while being robust to noise and low frequency fluctuations of the baseline.

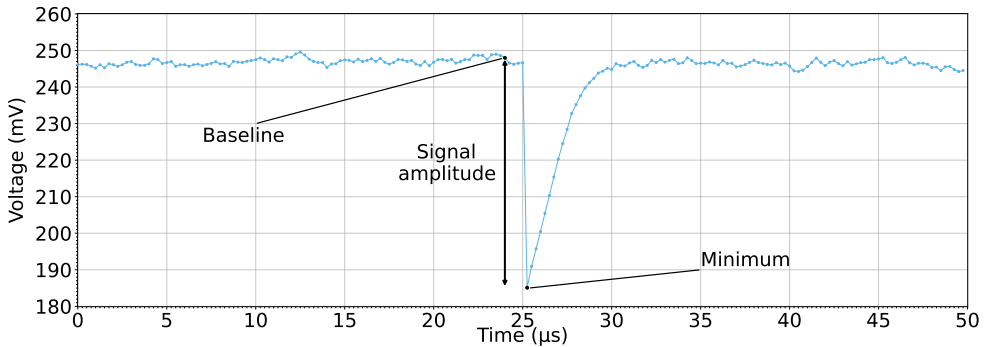


Figure 4.7 Typical signal acquired by a proximity board's ADC displayed in a $50 \mu\text{s}$ time window. The sampled points used to evaluate the baseline and signal amplitude are highlighted.

⁶ The 10% to 50% definition of the leading edge time is adopted in this context in place of the usual 10% to 90% definition. This choice avoids the error committed when evaluating the signal time at 90% of its full amplitude due to the observed signal ringing, which distorts the last part of the leading edge.

Figure 4.7 shows a typical pixel signal readout with the proximity board's ADCs in a 50 μs time window. For these signals, the amplitude is calculated as the difference between the baseline and the minimum of the signal. The baseline is evaluated as the value of the fourth sample before the minimum, and noise is evaluated as the RMS of the distribution obtained by subtracting the fourth sample found before the baseline from the baseline one, for each recorded signal. The choice of the parameters is done in accordance to the optimization reported in Reference [15].

Given the superior precision of the fast oscilloscope in resolving the details of the acquired signals, all the studies presented in the following sections of this chapter and in the next one are based on the analysis of pixels read out with the oscilloscope, with the signals digitized by the ADCs used to complete the information on the matrix collected charge.

4.6 Evaluation and optimization of the front-end operation settings

The set of bias currents and voltages sent to the chip for the pixel front-end circuit operation, i.e. the working point, was experimentally optimized by studying the sensor's response to charge injection. The initial front-end settings in this study were those used to simulate the chip performance in the design phase [5].

An optimization of the working point is a necessary step since the increase of the reverse bias down to -4.8 V exposes the transistors to voltages beyond the standard supply of -1.2 V , i.e. the limit of the transistor model used for the simulation. In particular, a large reverse substrate bias affects the operation of NMOS transistors hosted in the p-wells through body effect [6], which lowers the gain of the analog chain buffering the signal to the output.

A front-end parameter scan was conducted with the goal of optimizing the circuit performance, with particular focus on timing performance. Hence priority was given to signal amplitude maximization and signal leading edge time minimization.

The optimal settings, used for all the measurements presented in the following sections at any reverse substrate voltage V_{sub} applied, are summarized in Table 4.17.

⁷ The currents I_{bias3} , I_{bias4} and the voltages V_{casn} , V_{casp} are the bias settings of the off-pixel operational amplifier. The corresponding nodes are not depicted in Figure 4.3.

	Nominal	Optimized
I_{reset} (pA)	100	100
I_{biasn} (μA)	75	125
I_{biasp} (μA)	10	11.25
I_{bias3} (μA)	200	212.5
I_{bias4} (mA)	2.5	2.6
V_{casn} (mV)	750	900
V_{casp} (mV)	300	270

Table 4.1 Simulated nominal operation settings and experimentally optimized ones.

Finally, the V_{reset} setting is chosen depending on the applied V_{sub} to favor a linear front-end response at different reverse bias conditions. The studies for choosing the optimal V_{reset} are discussed in the next subsections.

4.6.1 Buffer circuit gain evaluation

The front-end circuit DC voltage transfer function is evaluated by varying the V_{reset} parameter and measuring the corresponding voltage level V_{board} on the output pad [16, 17]. The procedure can be better understood by considering that, in absence of a particle hit, the voltage level on the input node of the analog buffer chain is nearly equal to V_{reset} (cf. Section 4.2), hence a V_{reset} variation approximates a variation of the input node voltage V_{in} . From this follows the buffer differential gain g :

$$g = \frac{dV_{\text{board}}}{dV_{\text{in}}} \approx \frac{dV_{\text{board}}}{dV_{\text{reset}}} . \quad (4.4)$$

The transfer function is measured for all the pixels of different APTS-OA matrices operated within an interval of V_{sub} voltages between 0 V and -4.8 V, varied in steps of 0.6 V. For each V_{sub} , the V_{reset} parameter is varied from 20 mV to 900 mV in steps of 10 mV.

Figure 4.8 shows the transfer function (left) and the corresponding gain function (right) measured for pixel 5, i.e. one of the central pixels of the matrix, of a standard type (top), a modified type (middle) and a modified with gap type (bottom) sensor at varying V_{sub} . The effect of different substrate voltages manifest in an offset between the curves, with the baseline pulled towards lower values for enhanced reverse bias voltage. This behavior can be attributed to the fact that the bulk terminal of the NMOS transistors is connected to the p-well potential, which is identical to V_{sub} . Therefore, a V_{sub} variation changes the characteristics of the NMOS transistors through the body

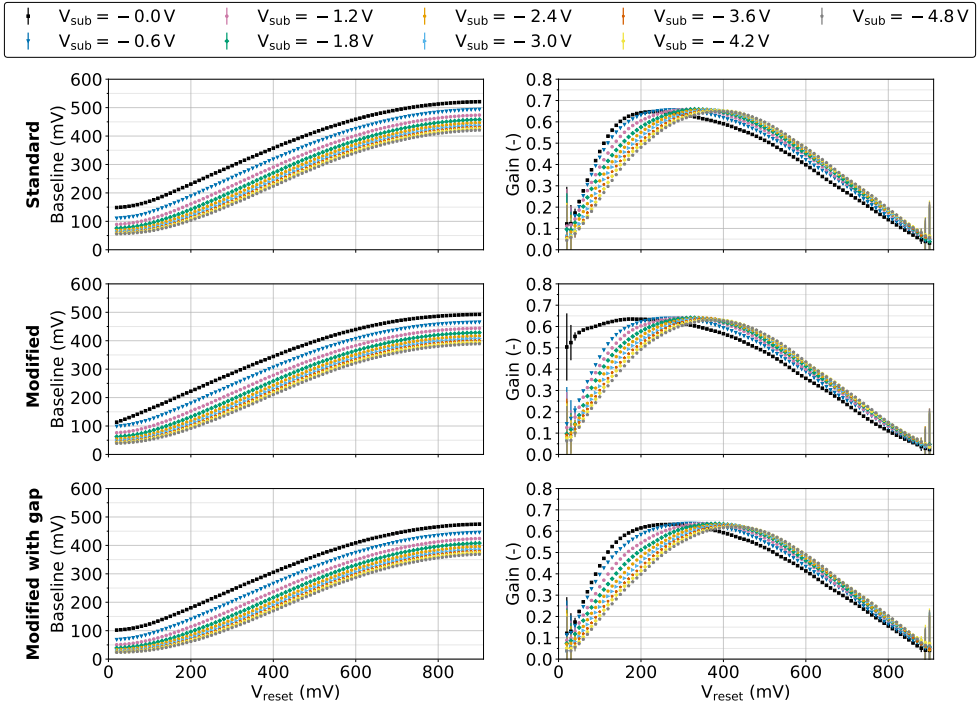


Figure 4.8 Transfer function (left) and gain function (right) measured for one of the pixels of a standard type (top), modified type (middle) and modified with gap type (bottom) sensor operated at varying V_{sub} .

effect, resulting in different voltage offsets after the NMOS source-follower stage (M3 in Figure 4.3) [16].

All the transfer functions show saturation effects both at regions of low and high values of V_{reset} . The saturation at high V_{reset} can be attributed to the PMOS source-follower stage at the sensing node (M2 in Figure 4.3), whereas the saturation at low V_{reset} can be attributed to the NMOS source-follower stage (M3 in Figure 4.3).

Furthermore, a spread of the order of 50 mV is measured between the output voltage level (i.e. the baseline) of the pixels of the same matrix at a given V_{sub} , reflecting in a subsequent pixel-to-pixel variation of the gain. Figure 4.9 shows, as an example, the transfer and the gain functions measured for all the pixels of the matrix of a standard type, a modified and a modified with gap sensor operated at fixed reverse substrate voltage of -2.4 V. Similar pixel-to-pixel spread is observed for the transfer and the gain functions measured at other V_{sub} voltages.

From the gain curves of Figure 4.8 and Figure 4.9, it is possible to identify an

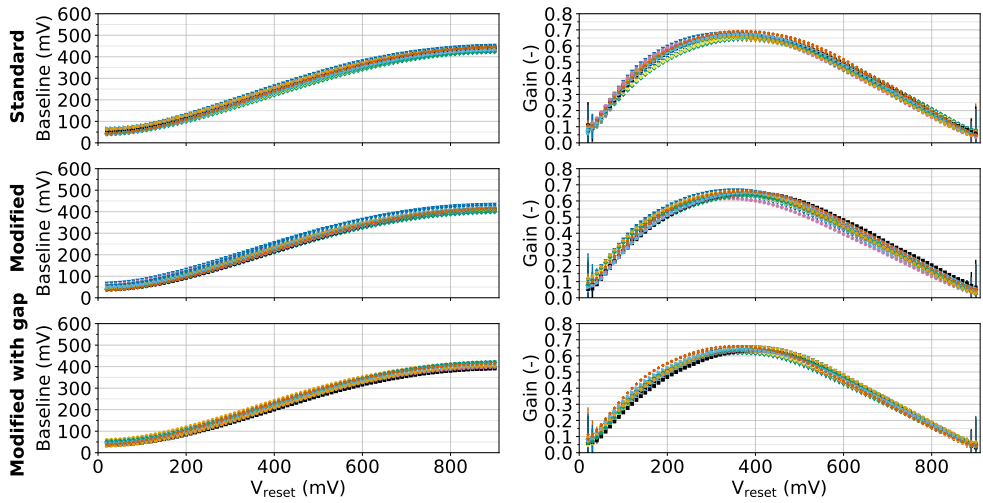


Figure 4.9 Transfer function (left) and gain function (right) measured for all the pixels of the matrix of a standard type (top), modified type (middle) and modified with gap type (bottom) sensor operated at fixed $V_{\text{sub}} = -2.4 \text{ V}$.

approximately flat region, where the circuit behavior can be considered linear and the buffer gain is around 0.65, with a systematic pixel-to-pixel spread. The plateau region shifts towards higher V_{reset} values for enhanced reverse bias voltage, in agreement with the dependence of the output voltage on the characteristics of the NMOS transistors that was already observed for the 180 nm CMOS technology [16].

No significant difference in transfer functions is found between sensors featuring different designs, as the DC characteristics of the buffer circuit are not affected by the sensor, and are therefore not depending on the specific pixel design variant.

All of these observations have to be considered when choosing the best circuit working point, namely the V_{reset} voltage to operate the chip in a region of almost constant differential gain.

4.6.2 Optimal working point assessment

The APTS-OA test structures were developed with the goal of studying the charge collection details and the time resolution of monolithic devices implemented in 65 nm CMOS technology. For this reason, the operating point must be chosen to minimize the contribution of the pixel front-end to the overall time resolution.

The V_{reset} parameter that minimizes the time jitter introduced by the buffer circuit is found by studying the chip response to a pulsing voltage $V_h = 1.2 \text{ V}$, corresponding to

an injected charge of the order of $1400 e^-$. The test is repeated for each one of the V_{sub} values measured to evaluate the transfer functions of the device under test. For a fixed V_{sub} , V_{reset} is varied in steps of 10 mV in the range of values where all the gain curves of the matrix are within 80% of their maximum, in order to include the plateau region of the gain functions. For each combination of V_{sub} and V_{reset} , 250 pulsing signals are acquired.

The determining parameter for timing measurements is the slope-to-noise ratio. As discussed in Section 2.8, the time jitter introduced by the front-end circuit can be quantified as:

$$\sigma_t = \frac{\sigma_n}{\frac{dV}{dt}} \approx \frac{t_r}{S/N}. \quad (4.5)$$

From Equation 4.5 it is possible to deduce the optimal V_{reset} as the one minimizing noise and maximizing the signal slope, also commonly referred to as *slew rate*⁸.

Figure 4.10 shows the voltage noise RMS (left) and the slew rate (right), computed as the ratio of the voltage variation between 10% and 50% of the signal's full amplitude and the corresponding leading edge time, measured for pixel 5, i.e. one of the central pixels of the matrix, of a standard type (top), a modified type (middle) and a modified with gap type (bottom) sensor at varying V_{sub} . While no clear correlation between noise RMS and V_{reset} is visible, a dependence of the signal slope on V_{reset} is found, with a maximum at high V_{reset} values. The signal slope varies with the applied V_{sub} since the bias voltage affects the operation of the NMOS transistors hosted in the p-well (cf. Section 4.6.1) but also the value of input capacitance at the sensing node (cf. Section 4.8.2). The signal slope curves also vary for the different pixel variants as the input capacitance, which affects the output signal amplitude, depends on the pixel geometry (cf. Section 4.8.2).

Therefore, the optimal V_{reset} depends on the applied V_{sub} and is tuned to allow the circuit operation in the plateau region of the gain curve as close as possible to the maximum of the signal slope curve. The V_{reset} values which guarantee the best performance in terms of front-end linearity and slope-to-noise ratio, found by averaging the optimal values measured for the individual pixels of the different analyzed devices, are listed in Table 4.2. Pixel-to-pixel and chip-to-chip fluctuations of the optimal V_{reset} are, if combined, of the order of 10% around the values reported in Table 4.2. The standard front-end operation settings used in the measurements discussed in this and in the next chapter are therefore those reported in Tables 4.1 and 4.2, unless

⁸ Since the evaluation of the slew rate is possible only for the signals acquired with the oscilloscope, the choice of the optimal V_{reset} is based on the data taken for the central four pixels of the device under test.

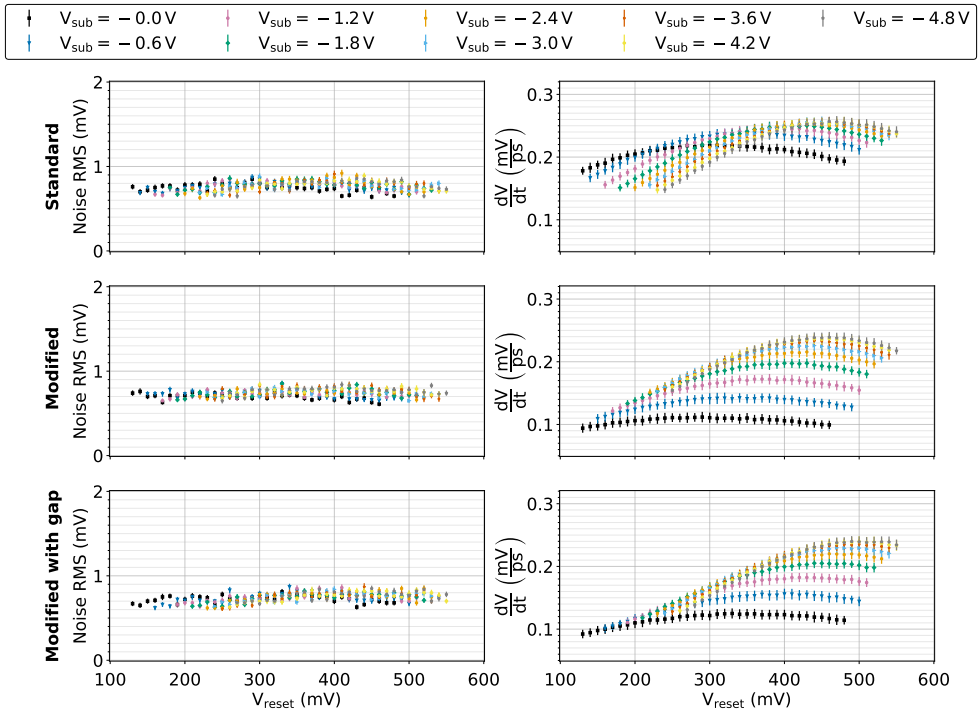


Figure 4.10 Voltage noise RMS (left) and signal slew rate (right) measured for one of the central pixels of the matrix of a standard type (top), modified type (middle) and modified with gap type (bottom) sensor operated at varying V_{sub} .

differently stated.

V_{sub} (V)	0.0	-0.6	-1.2	-1.8	-2.4	-3.0	-3.6	-4.2	-4.8
V_{reset} (mV)	270	330	360	380	400	410	420	430	440

Table 4.2 Optimal V_{reset} at varying reverse substrate bias voltage V_{sub} .

4.7 Measurements with ^{55}Fe X-ray source

Three APTS-OA prototypes, each of them featuring one of the three different pixel design variants, were characterized by studying their response to soft X-rays produced by an ^{55}Fe radioactive source. The iron source is a widespread tool for the calibration of charge coupled devices (CCDs), and in general imaging sensors, especially in X-ray astronomy. It was already used for the characterization and calibration of monolithic

devices implemented in 180 nm CMOS technology [16, 18, 19]. Using the same tool for the calibration of 65 nm CMOS-based structures allows a direct comparison with the previous generation of monolithic sensors.

An ^{55}Fe isotope decays via electron capture to ^{55}Mn . It emits photons from two modes, i.e. $\text{Mn-}k_\alpha$ and $\text{Mn-}k_\beta$ photons, with energy at 5.9 keV and 6.5 keV, respectively [20]. These photons have absorption lengths in silicon of 29 μm and 37 μm , respectively [21]. The large absorption lengths allow the emitted photons to penetrate the whole epitaxial layer of the APTS-OA devices, being its thickness of the order of 10 μm .

The X-rays interact with the detector predominantly via photoelectric effect, generating an amount of electron-hole pairs equal to $N_{e-h} = E_{ph}/W$, where $W = 3.6 \text{ eV}$ is the average energy required to generate an electron-hole pair in silicon (c.f. Section 2.3). Thus, the photoelectric conversion of the two ^{55}Fe X-rays generates in silicon 1640 $e^- - h^+$ and 1800 $e^- - h^+$, respectively. A third characteristic line, known as *Si escape peak*, can emerge from the spectrum, depending on the energy resolution of the device and on the statistical significance of the analyzed data sample. This is due to the fluorescence photons emitted by de-exciting silicon atoms. In fact, if a deep shell (K) electron is ejected after photoelectric interaction, an outer shell electron will fill the vacancy left by the photoelectron with the subsequent emission of a characteristic X-ray photon. The energy of the latter is equal to the difference between the absorbed ^{55}Fe photon, i.e. $\text{Mn-}k_\alpha$ or $\text{Mn-}k_\beta$, and the binding energy of the ejected electron in the K shell of the silicon atom, equal to 1.74 keV [22]. The fluorescence X-rays leaving the pixels where the photoelectric interaction has happened without being reabsorbed lead to the measured Si escape ($\text{Mn-}k_{\alpha,\beta} - \text{Si-}k_{\text{edge}}$) peak in the spectrum, corresponding to 1160 $e^- - h^+$ in silicon. A fourth characteristic line, known as *silicon fluorescence peak*, can eventually appear in the spectrum. It represents the photoelectric absorption of the fluorescence X-rays emitted by neighbor pixels in the de-exciting process described above. This last peak, corresponding to 480 $e^- - h^+$, is however not used for the calibration process presented in the following section as the statistical significance of the collected data sets does not allow to resolve it.

The known amount of charge produced after photoelectric interaction allows to calibrate the acquired signals in terms of collected charge and to equalize the response of different pixels, enabling the comparison of the performance of different structures operated at different bias conditions.

In the following, the signal calibration procedure based on fitting the ^{55}Fe spectrum peaks is shown, then the comparison of the response of different devices to ^{55}Fe X-rays is discussed.

4.7.1 Signal charge calibration

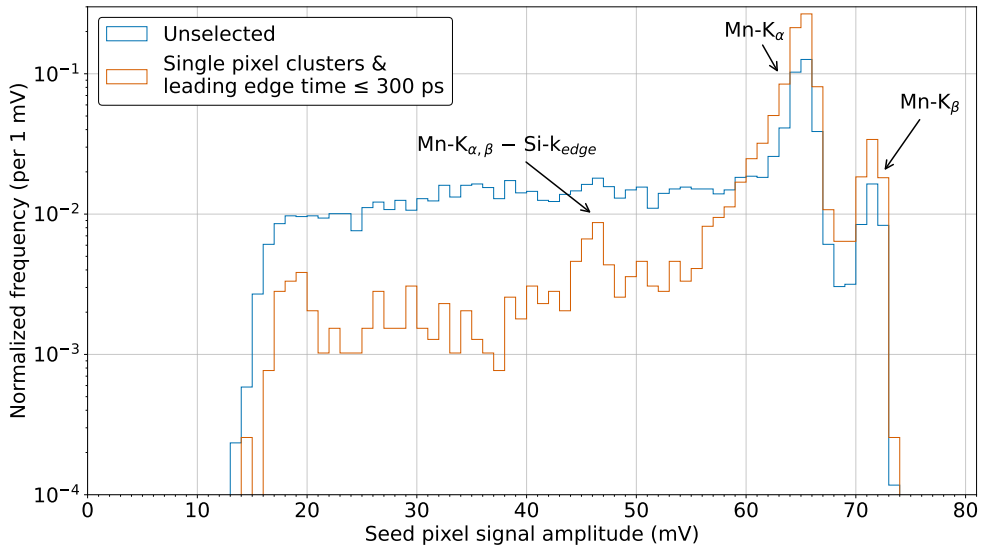


Figure 4.11 Seed pixel ^{55}Fe spectrum (blue) and spectrum of single pixel cluster events with leading edge signal time lower than or equal to 300 ps (orange). In the latter, the $\text{Mn-}k_{\alpha}$ and $\text{Mn-}k_{\beta}$ peaks are better resolved with respect to the former spectrum and the Si escape ($\text{Mn-}k_{\alpha,\beta} - \text{Si-}k_{\text{edge}}$) peak is revealed. The spectra refer to one of the central pixels of a modified with gap type sensor operated at $V_{\text{sub}} = -2.4 \text{ V}$.

The signal charge calibration of every pixel is performed individually, as this approach allows to compensate for pixel-to-pixel fluctuations in terms of gain (cf. Section 4.6.1) and input capacitance (cf. Section 4.8.2), but at the cost of reduced statistics. The calibration consists of identifying the position of the peaks in the signal amplitude spectrum of each pixel. The peaks correspond to the full collection of the charge generated after the photoelectric conversion.

An example of an ^{55}Fe signal amplitude spectrum of the events⁹ having the seed in one of the four central pixels of the matrix is shown in Figure 4.11 (blue distribution). The seed is the pixel of the matrix producing the largest amplitude signal. The cluster is instead defined as a group of neighboring pixels inside a 3×3 matrix centered around the seed, which have a signal above a certain threshold. In order to avoid edge effects and to be able to reconstruct the full cluster charge, only clusters having

⁹ In this context, an event is defined as an interaction between an ^{55}Fe X-ray and an APTS-OA pixel triggering a data acquisition (cf. Section 4.4.2).

a seed in one of the four central pixels are considered. Furthermore, to improve the calibration procedure by making the ^{55}Fe spectral lines more distinguishable, the spectra are further filtered by selecting single pixel cluster events, where the full charge collection is assumed to happen in a single pixel, with a leading edge signal time lower than or equal to 300 ps, to prioritize photoelectric interactions taking place in regions of the pixel with high electric field, where the charge collection process is fast and efficient. The effects of such a selection are reflected in the orange distribution of Figure 4.11, where the $\text{Mn-}k_\alpha$ and $\text{Mn-}k_\beta$ peaks are enhanced and the Si escape ($\text{Mn-}k_{\alpha,\beta} - \text{Si-}k_{\text{edge}}$) peak is revealed. This data selection strategy is adopted for the charge calibration procedure discussed hereafter.

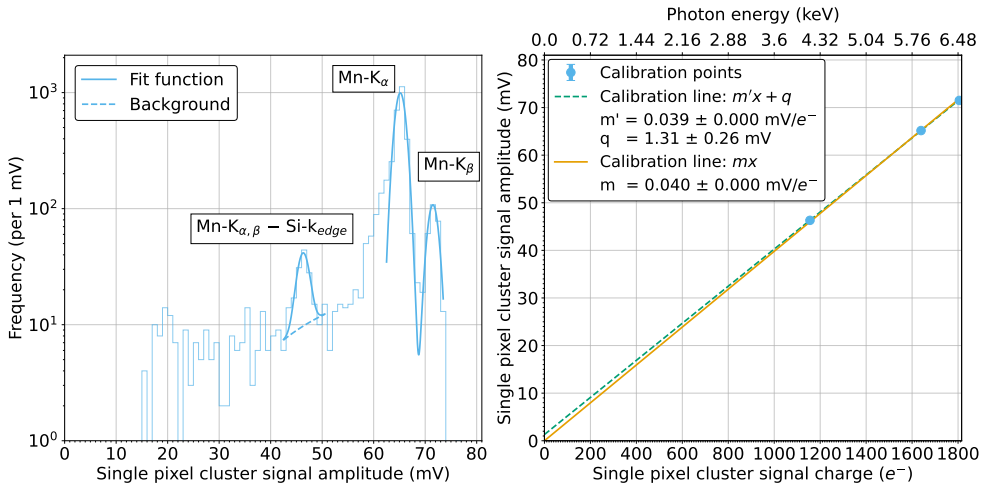


Figure 4.12 Single pixel cluster ^{55}Fe spectrum with signals' leading edge time lower than or equal to 300 ps (left) and corresponding charge calibration points (right, in blue) resulting from the Gaussian fit of the spectrum peaks. The latter are fitted with two linear models: one with intercept as free parameter (green dashed line) and one with intercept set to zero (orange solid line). The spectrum and the calibration line are for one of the central pixels of a modified with gap type sensor operated at $V_{\text{sub}} = -2.4$ V.

The left panel of Figure 4.12 shows the selected single pixel cluster spectrum of the photons emitted by a ^{55}Fe source measured by a selected pixel of a modified with gap type sensor operated at $V_{\text{sub}} = -2.4$ V. The peaks are fitted with Gaussian functions, and the value of the mean of every peak is used for the pixel charge calibration. The right panel of Figure 4.12 shows the calibration points obtained from the peak positions and the corresponding photon energies, converted to charge. Two linear functions are

fitted to the calibration points: one with slope m' and intercept q left as free parameter (green dashed line) and one with slope m and intercept set to zero (orange solid line). A high linearity is apparent for all the pixels of all the measured samples, with an intercept q close to zero. This last observation, together with a verified linearity of the pixel response, justifies the choice of the simpler model with intercept set to zero to describe the charge to voltage conversion property of the pixels. The fit parameter m defines the calibration factor allowing to convert the signal amplitude in signal charge. The difference between the slopes of the two linear models $\Delta m = m - m'$ accounts for the systematic uncertainty in the described calibration procedure and is used, in particular, for the evaluation of the systematic uncertainty of the capacitance measurements shown in Section 4.8.

Despite the data selection aimed at improving the peak fitting quality for a more precise charge calibration, the pixels of the standard type sensor are calibrated by using the $\text{Mn-}k_\alpha$ and $\text{Mn-}k_\beta$ peaks only, as the Si escape peak is not well resolved with the collected data samples.

For all the datasets related to the three measured devices at any reverse bias voltage, the spread of the calibration line slope m among the central four pixels is of the order of few percents, with the maximum variation between the calibration factor of one pixel and the mean of the four of the order of 3%. This last argument supports the choice of computing the charge calibration factor of the outer twelve pixels of the matrix as the average of the factors measured for the four central ones.

4.7.2 Charge collection studies

A way to characterize the charge collection properties of the three different pixel variants is to study their signal and cluster size distributions. The cluster size is determined by applying a clustering threshold of $100 e^-$, i.e. by counting the number of pixels with signal charge above such threshold¹⁰.

Figure 4.13 shows the comparison of ^{55}Fe seed pixel spectra acquired by three devices featuring the three different pixel designs operated at varying substrate voltage between -1.2 V and -4.8 V , before (top row) and after (bottom row) charge calibration. For the spectra represented as a function of the signal amplitude expressed in voltage, the peaks are smeared because of pixel-to-pixel variations and shift towards higher voltage values with increasing reverse bias, as a result of the decreasing pixel input capacitance (cf. Section 4.8.2). The same spectra displayed as a function of the seed signal charge

¹⁰ The chosen clustering threshold is at least four times higher than the Equivalent Noise Charge, for every measured V_{sub} setting (cf. Section 4.9.1).

show better resolved peaks, as single pixel calibrations compensate for pixel-to-pixel variations. This allows the comparison of data taken at different operation conditions. In both cases, the distributions are normalized by the total number of events after a cut applied at $400 e^-$ for the signal charge spectra and at varying thresholds between 12 mV and 20 mV for the signal amplitude spectra, depending on the sensor and the applied reverse substrate voltage. The cuts applied to the voltage spectra roughly correspond to a threshold of $400 e^-$ and depend on the input capacitance of the sensor (cf. Section 4.8.2).

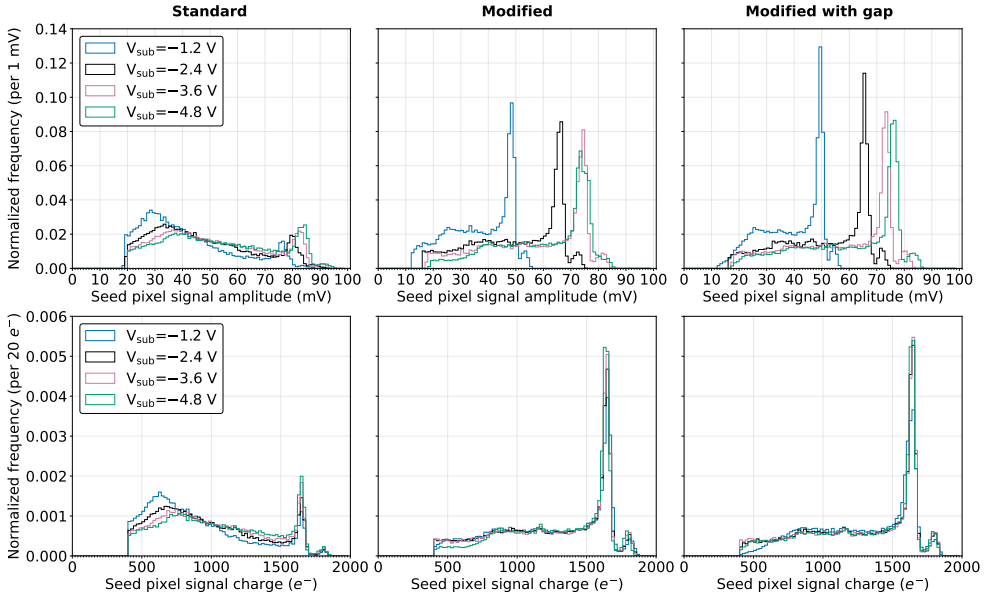


Figure 4.13 Comparison of the ^{55}Fe seed signal amplitude spectra (top) and seed signal charge spectra (bottom) measured for three devices featuring the three different pixel designs operated at varying reverse substrate voltage.

The main difference between the seed pixel spectra of the standard layout with respect to the other two variants lays in the pronounced bump appearing between $500 e^-$ and $900 e^-$ (leftmost panels of Figure 4.13), depending on the applied V_{sub} . This feature is also known as *charge sharing peak* and is due to the photoelectric conversion happening in a non-depleted region of the epitaxial layer, where the generated charge thermally diffuses and can be easily shared among neighboring pixels [18]. No notable charge sharing peak is observed in modified and modified with gap seed pixel spectra, while the Mn-k_α and Mn-k_β peaks, also known as *charge collection peaks*, are more than two times more pronounced than the corresponding peaks in the standard seed

pixel spectra, for each measured reverse bias voltage. The higher frequency of events in the charge collection peaks confirms the increased depletion of the epitaxial layer's volume introduced by the process modification, as the probability of full collection of the charge generated after photoelectric conversion by the seed pixel is enhanced. Events where the photoelectric interaction happens in the pixel substrate or in the p-wells, where no electric field is present, can also contribute to the continuum of the spectra. In this case, the charge can be collected only if it thermally diffuses in the depleted region, where the electric field will make it drift towards the collection electrode. Being diffusion a random phenomenon and considering the non-negligible probability of charge trapping in low resistivity silicon (such as substrate and p-wells), only part of the charge generated after photoelectric interaction can be collected.

The measured modified with gap sample is less affected by pixel-to-pixel fluctuations than the modified one, since the $Mn-k_\alpha$ and $Mn-k_\beta$ peaks in the signal amplitude spectra of the former are narrower and better resolved. No major differences are observed between modified and modified with gap charge spectra, as the charge calibration procedure cancels pixel-to-pixel fluctuations. A slightly enhanced frequency for the full charge collection peaks of the modified with gap sensor seed pixel spectra is observed.

To confirm what said above, the same data presented in Figure 4.13 can be studied in terms of cluster size distributions. Figure 4.14 shows the comparison between the cluster size distributions (top) and the dependence of the mean cluster size on the applied reverse substrate voltage (bottom), for all the three measured devices. The charge sharing properties of the standard pixel layout are confirmed by the cluster multiplicity distributions showing non-negligible probability of large clusters of three or four pixels, with the average cluster multiplicity considerably above 2. On the other hand, modified processes are characterized by a high frequency of single pixel clusters, with an average cluster multiplicity below 2. The difference between the distributions of modified and modified with gap structures is small, as well as the average cluster size curves at varying reverse substrate voltage are very close to each other. The reduced difference is, however, in accordance to the expectations, since the slightly lower pixel cluster multiplicity observed for the modified with gap structure can be explained with the enhanced charge sharing suppression introduced by the gap in the low dose n-type implant applied at the pixel edge.

The limited difference in cluster size distribution observed between modified and modified with gap variants can be attributed to the $10\mu m$ pitch of the measured samples. In fact, as shown in Reference [15], the distinction between the two design variants becomes more evident for larger pixel pitches.

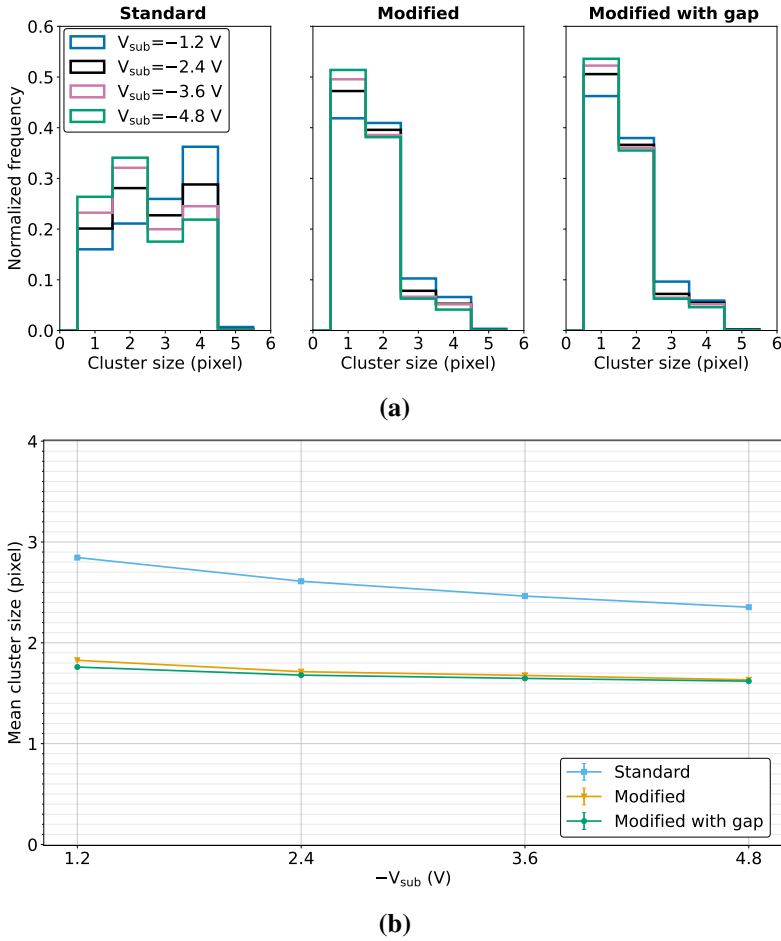


Figure 4.14 Comparison of the cluster size distributions of the three pixel layout variants operated at different reverse substrate voltage (a) and mean cluster size as a function of the applied reverse substrate voltage (b).

An instructive way to merge the information given by Figure 4.13 and Figure 4.14 is shown in Figure 4.15, where the separated contributions to the seed signal charge spectra given by clusters of different size are highlighted. It represents, as an example, the data taken with the devices operated at $V_{\text{sub}} = -2.4$ V. For the sensor featuring standard pixel design, the main contributors to the charge sharing peak are clusters with multiplicity 3 and 4, while such cluster sizes are almost absent in the modified and modified with gap pixel spectra.

Further information on the charge collection performance of the different pixel

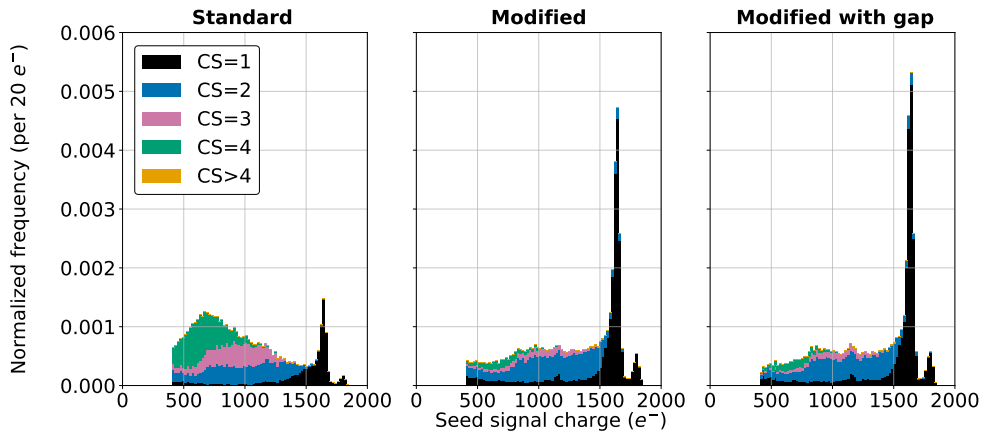


Figure 4.15 Comparison of seed signal ^{55}Fe charge spectra as a function of cluster size (CS, indicated with different colours) for the three different APTS-OA pixel layout variants measured at constant reverse substrate voltage $V_{\text{sub}} = -2.4 \text{ V}$.

layouts can be obtained by studying the correlation of signal charge with signal leading edge time. Faster signals, characterized by shorter leading edge times, are the product of photoelectric interactions in the depleted region of the sensor's epitaxial layer, where the charge efficiently and swiftly drifts towards the collection electrode as a result of the high electric field. Figure 4.16 displays the correlation between the seed signal charge and the signal leading edge time divided by single pixel clusters (top row) and clusters with pixel multiplicity larger than one (bottom row) for the three devices implemented with different pixel layouts operated at $V_{\text{sub}} = -2.4 \text{ V}$, for consistency with Figure 4.15. All the distributions are normalized by the total number of events collected by the sensor at the measured configuration.

For the single pixel cluster distributions (top row of panels in Figure 4.16), the largest fraction of events is concentrated in amplitude around the $\text{Mn-}k_{\alpha}$ ($1640 e^{-}$) and $\text{Mn-}k_{\beta}$ ($1800 e^{-}$) peaks, with a signal leading edge time well below 0.3 ns . The frequency of the events contributing to the charge collection peaks is, as already observed in the 1D spectra, enhanced for the modified pixel variants with respect to the standard sensor type. The remaining events belonging to the single pixel cluster population are divided, for all the three pixel variants, in two distinct families: one characterized by fast signals, with leading edge time lower than 0.3 ns , and one characterized by slower signals, with leading edge time higher than 0.3 ns . The first group also contains events contributing to the silicon escape peak ($1160 e^{-}$), which is well resolved in the single pixel cluster spectra of the modified and modified with gap type sensors (cf. Section 4.7.1) and

represents a case of full charge collection. The other entries pertaining to the first family are cases of partial charge collection where the photoelectric interaction has, however, likely happened in the depleted region of the epitaxial layer. The events constituting the second group, characterized by slow signals, are cases of partial charge collection where the photoelectric interaction has likely happened in a non depleted region of the pixel (i.e. p-well or substrate) or in its proximity. Slower signals can reflect indeed the contribution of the diffusion process in the charge collection.

Regarding the distributions of events with clusters of pixel multiplicity larger than one (bottom row of panels in Figure 4.16), for the standard type sensor, events with cluster size larger than one are broadly distributed in signal leading edge time while for the modified variants most of the signals have a leading edge time below 0.4 ns, illustrating the impact of the process modification on speeding up the charge collection also in case of charge sharing. In particular, it can be seen that, for the non irradiated $10\ \mu\text{m}$ pixel pitch samples measured, the distribution of the modified variant is even more concentrated towards shorter signal leading edge times than the distribution of the modified with gap variant.

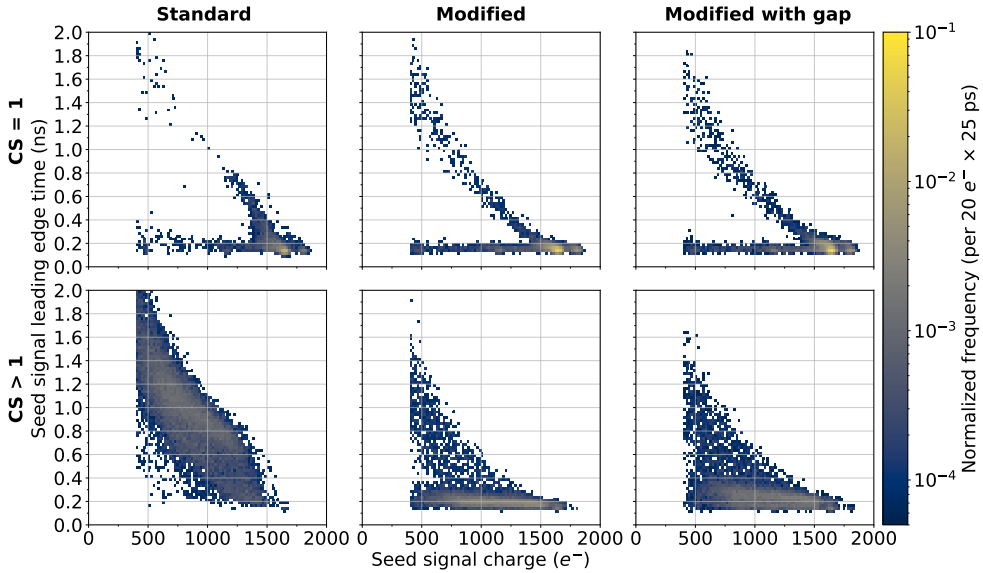


Figure 4.16 Correlation of seed signal charge with seed signal leading edge time for single pixel clusters ($\text{CS} = 1$, top row) and clusters with pixel multiplicity larger than one ($\text{CS} > 1$, bottom row) measured with ^{55}Fe X-rays for the three different APTS-OA pixel layout variants operated at constant reverse substrate voltage $V_{\text{sub}} = -2.4\ \text{V}$.

The results discussed in this section highlight the effect of process and pixel design

modifications on the charge collection properties of monolithic sensors implemented in 65 nm CMOS imaging technology. The comparison between standard and modified processes confirms that the addition of a low dose n-type implant below the collection electrode allows to extend the sensor's depleted region, reduces the probability of charge sharing between neighboring pixels and promotes a faster and more uniform charge collection, favoring phenomena of charge drifting towards the collection electrode and suppressing thermal diffusion.

For the pixels of 10 μm pitch that can be studied with the APTS-OA structures, no major differences between the modified and the modified with gap variants emerge from ^{55}Fe X-ray measurements.

Additional figures of spectra measured at different reverse substrate voltage are available in Appendix A.

4.8 Pixel capacitance

The charge Q_{coll} collected by the sensing electrode after a particle hit produces a voltage variation at the pixel diode node that is inversely proportional to the total capacitance seen at the same node (cf. Section 4.2, Equation 4.3). The resulting voltage signal is then buffered to the output pad. The output voltage measured by the readout system depends also on the non-unity gain of the buffer circuit. To fully characterize a monolithic pixel sensor, both contributions have to be quantified. The evaluation of the pixel front-end gain is already discussed in Section 4.6.1, while the assessment of the total capacitance at the pixel input node is presented in this section. As widely discussed in Reference [23], the total capacitance seen at the pixel sensing node contains a reverse bias-dependent term and a constant one. The former is formed by the junction capacitance of the pixel diode and by the source to bulk junction of the reset transistor (M0 in Figure 4.3) while the latter is the sum of the stray capacitance of the interconnecting lines, the source to gate capacitance of the reset transistor, the gate capacitance of the first source-follower stage (M2 in Figure 4.3) and the capacitance C_{inj} of the charge injection circuit. Whilst it is possible to evaluate this very last term by combining charge injection and ^{55}Fe source measurements, all the other terms contributing to the total pixel capacitance, either reverse-bias dependent or not, cannot be disentangled and will be indicated in the rest of the chapter as input capacitance C_{input} .

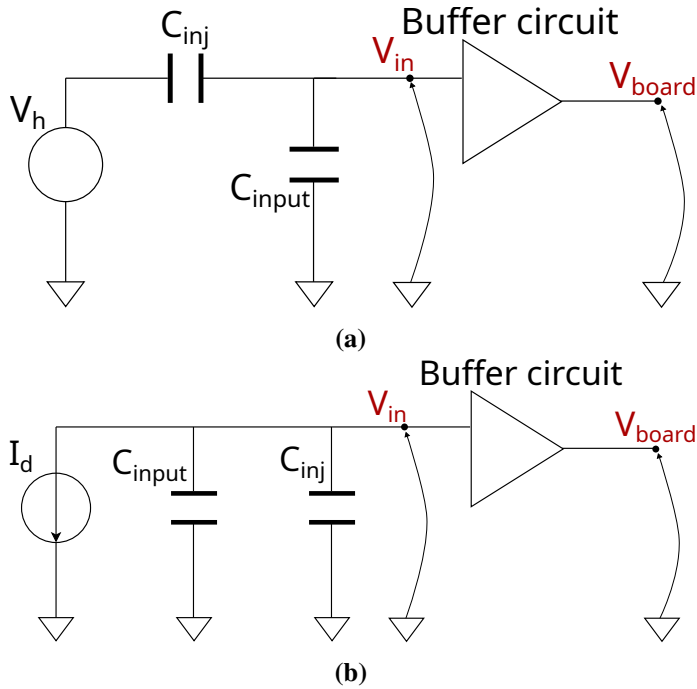


Figure 4.17 Small signal simplified equivalent circuit for the signals produced by a pulsing measurement (a) and by a radioactive source measurement (b).

4.8.1 Injection capacitance measurement

An experimental evaluation of the coupling capacitance used to inject charge in the pixel front-end via the voltage reference V_h can be performed by combining the results of test pulses measurements and ^{55}Fe source measurements.

Figure 4.17 shows the equivalent small signal circuits that are useful to determine the dependence of the measured output signal amplitude on the injected charge via test pulses (top) and on the charge generated after a photoelectric interaction (bottom). The amplitude of the voltage drop seen at the input node is denoted with V_{in} and the signal amplitude measured by the readout system is V_{board} .

The output signal measured for an input test pulse of amplitude V_h is:

$$V_{board} = g \cdot V_{in} = g \cdot \frac{C_{inj}}{C_{inj} + C_{input}} \cdot V_h. \quad (4.6)$$

The difference between the signal amplitude at the input node and the measured signal at the output pad is given by the factor g representing the non-unity gain of the buffer

circuit.

By measuring the signal amplitude variation at different injected charge, i.e. at varying V_h amplitude, it is possible to quantify the proportionality factor between V_{board} and V_h . Figure 4.18 shows, as an example, the results of the measurement of the output signal amplitude at varying injected charge for one of the central pixels of a modified with gap type sensor operated at different reverse substrate voltages. For each configuration, 1000 input pulses are sent. Similarly to what is done for the charge calibration procedure discussed in Section 4.7.1, the data points, representing the average measured output signal amplitude at varying injected charge, are fitted with two linear models: one having the intercept as a free parameter and one having a fixed intercept equal to zero. The latter is used to retrieve the fit parameter γ that, according to Equation 4.6, is equal to:

$$\gamma = g \cdot \frac{C_{inj}}{C_{inj} + C_{input}} , \quad (4.7)$$

with γ being function of the applied reverse bias voltage since C_{input} varies with this last. The difference $\Delta\gamma^{syst}$ between the slope of the line with unconstrained intercept and the slope of the line with intercept equal to zero is used to account for systematic uncertainty in the capacitance evaluation described later.

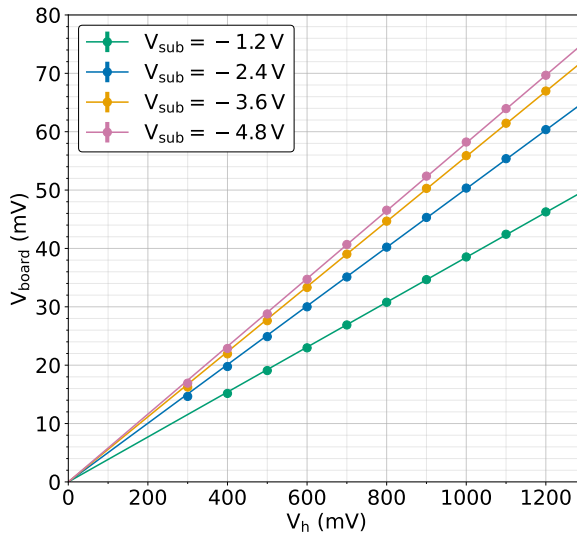


Figure 4.18 Signal amplitude measured at different injected charge in the pixel front-end via test pulses for one of the central pixels of a modified with gap sensor variant.

The signal produced by the interaction of an ^{55}Fe X-ray with the detector is:

$$V_{board} = g \cdot V_{in} = g \cdot \frac{Q_{coll}}{C_{inj} + C_{input}}, \quad (4.8)$$

where Q_{coll} is the charge collected by the sensing electrode inducing the detector current signal I_d . As shown in Section 4.7.1, V_{board} and Q_{coll} are the measured output signal amplitude and the charge generated in silicon for the corresponding ^{55}Fe peak, respectively. From Equation 4.8, the charge calibration line of an individual pixel has slope δ :

$$\delta = g \cdot \frac{1}{C_{inj} + C_{input}}. \quad (4.9)$$

As explained in Section 4.7.1, and similarly to the test pulses case, the factor $\Delta_{\delta}^{\text{syst}}$, equal to the difference between the slopes of the two linear models used to fit the data, accounts for systematic uncertainty.

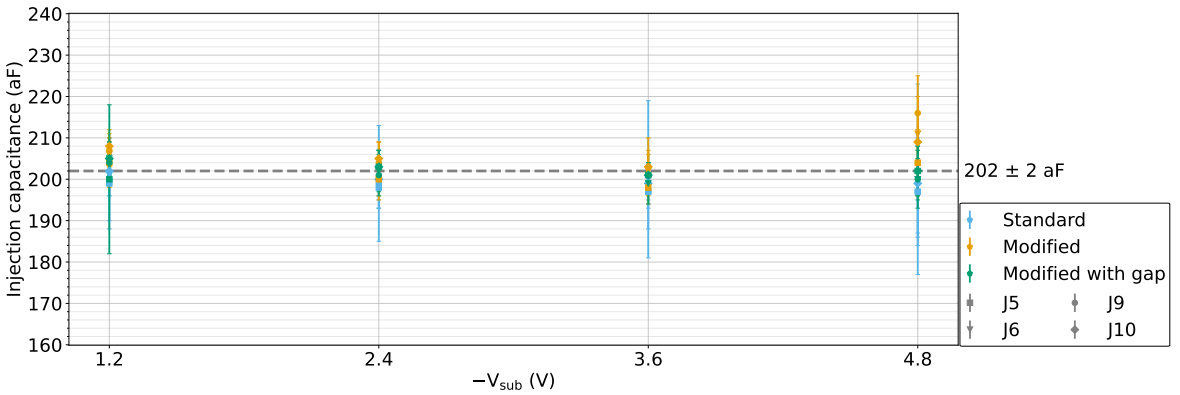


Figure 4.19 Charge injection capacitance measured for the four central pixels of three sensors implementing different pixel layouts. Mean injection capacitance value and related uncertainty are reported.

Finally, the injection capacitance can be then retrieved by combining Equations 4.7 and 4.9:

$$C_{inj} = \frac{\gamma}{\delta}. \quad (4.10)$$

Figure 4.19 shows the values of the injection capacitance of each single central pixel of the matrix retrieved by applying Equation 4.10 to the measurements performed on the three sensors featuring the three different pixel layouts with the related uncertainty computed by summing in quadrature the systematic uncertainties, $\Delta_{\gamma}^{\text{syst}}$ and $\Delta_{\delta}^{\text{syst}}$, and

the statistical ones. As expected, no clear dependence of the injection capacitance on the pixel geometry and on the applied reverse bias voltage is revealed. The experimental value of the injection capacitance is evaluated by averaging the single measurements reported in Figure 4.19. The mean injection capacitance found is 202 aF, with a standard mean error of 2 aF.

The value found experimentally differs from the nominal one of 242 aF by about 20%. This difference is understandable if the difficulty to precisely quantify sub fF capacitance is considered, and it justifies the need of the procedure described above to evaluate the charge injection capacitance.

4.8.2 Input capacitance measurement

Once the injection capacitance is known, the value of the input capacitance¹¹ can be obtained via simple algebraic manipulation of one of Equations 4.6 or 4.8. To correctly evaluate the capacitance and not overestimate it, the non-unity gain of the buffer circuit must be taken into account. To do so, a gain correction procedure to correctly estimate the potential difference at the input node V_{in} related to the measured output potential V_{board} is employed [16]. This is based on the inverse of the experimental transfer functions f_t shown in Section 4.6.1. In fact, with:

$$V_{board} = f_t(V_{in}) , \quad (4.11)$$

the inverse function f_t^{-1} , which provides the potential V_{in} for any measured V_{board} passed as input, is found by interpolating the V_{reset} (which approximates the potential at the sensing node) at varying V_{board} with a cubic spline. Said spline is then applied to the acquired output signals to retrieve the corresponding ones at the input node.

By considering the pulsing case (cf. Equation 4.6), the voltage difference at the input node is:

$$V_{in} = \frac{C_{inj}}{C_{inj} + C_{input}} \cdot V_h \rightarrow \gamma_{GC} = \frac{C_{inj}}{C_{inj} + C_{input}} , \quad (4.12)$$

where γ_{GC} differs from the factor γ defined in Equation 4.7 because it does not depend on the gain g of the buffer circuit, as this dependence is canceled by the gain correction procedure described above. The factor γ_{GC} can be obtained by applying the same fitting procedure presented in Section 4.8.1 to the gain corrected signal amplitudes measured at varying injected charge, i.e. to the signals interpolated with the function f_t^{-1} .

¹¹ In this context, the input capacitance is intended as the sum of all the capacitive contributions at the pixel input node, excluded the injection capacitance evaluated in Section 4.8.1.

The input capacitance can be finally computed as:

$$C_{input} = \left(\frac{1}{\gamma_{GC}} - 1 \right) \cdot C_{inj} . \quad (4.13)$$

The uncertainty related to the input capacitance is computed by adding in quadrature the uncertainties affecting γ_{GC} and C_{inj} .

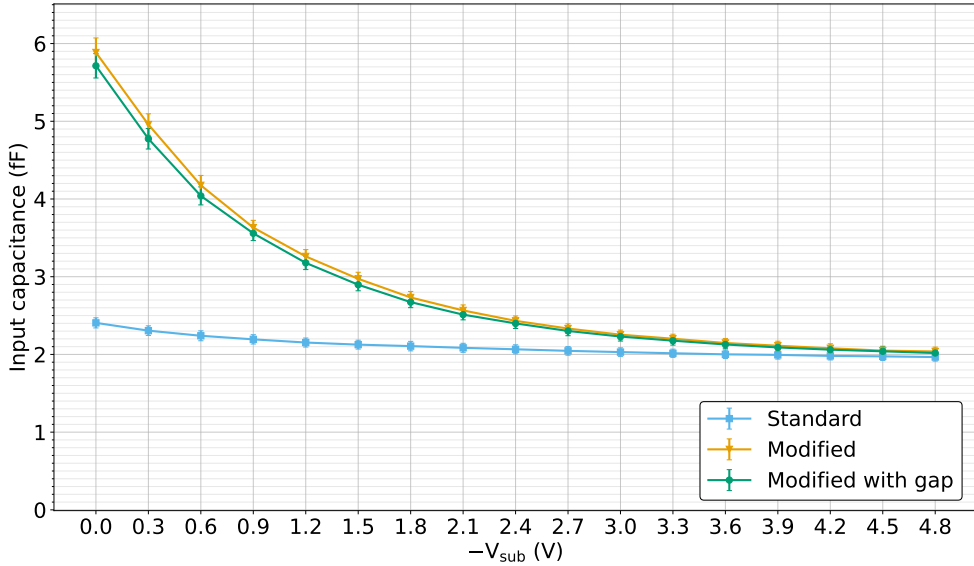


Figure 4.20 Comparison of the input capacitance measured for the three different pixel layouts operated at varying V_{sub} and fixed $V_{reset} = 400$ mV.

Figure 4.20 shows the average input capacitance of the same three devices measured with charge injection and ^{55}Fe X-rays to evaluate the injection capacitance. To properly compare the three different pixel geometries and make the pixel diode reverse bias variation only depend on the varying substrate voltage, an ad hoc measurement was carried out by sending 1000 input pulses of varying amplitude V_h to the charge injection circuit for each V_{sub} with V_{reset} kept constant at 400 mV.

The different behavior of the curves can be explained by looking at the pixel cross sections drawn in Figure 4.1. In the standard design, the junction extends from the collection electrode outward. The depletion layer assumes the characteristic 'bubble' shape and reaches the boundaries of the deep p-well already at low reverse bias voltages. Due to the high doping level of the deep p-well, the depletion region can not expand laterally any further. The depletion layer can still expand vertically into

the epitaxial layer towards the substrate, but the dependence of the extension of the depletion volume on the reverse bias voltage is weaker for a (quasi-) spherical junction than for a planar one. This explains the small decrease of the input capacitance with increasing reverse bias voltage. Although the epitaxial layer is not fully depleted, the pixel diode capacitance value is minimal because of the tiny collection electrode size. For the modified and modified with gap designs, the junction is moved deep in the epitaxial layer, at the boundary of the low dose n-type blanket with the deep p-well and the epitaxial layer. With increasing reverse bias, the depleted volume extends both towards the collection electrode and the substrate, until reaching full depletion of the sensor. This is reflected in the decrease of the capacitance down to 2 fF, converging to the value of the standard design.

It is worth to repeat once more that the curves of Figure 4.20 do not describe the behavior of the pixel diode only, as other terms contribute to the input capacitance.

4.9 Noise figures

For an analog sensor like the APTS-OA, the magnitude of the noise can be directly evaluated from the sampled signals. In the following subsections, the measurements aimed at quantifying the Equivalent Noise Charge (ENC) and the time jitter introduced by the pixel front-end circuit are discussed.

4.9.1 Equivalent noise charge

As explained in Section 4.5, the magnitude of the noise for the APTS-OA pixels is measured as a voltage RMS. In order to allow a fair comparison with the signal charge, it can be expressed in units of electrons, also referred to as *Equivalent Noise Charge* (ENC). The ENC denotes the amount of charge collected by the sensor that would generate a signal of the same amplitude of the measured noise RMS.

To experimentally evaluate the ENC, the voltage noise is converted by using the pixel charge calibration factor δ (cf. Equation 4.9):

$$ENC = \frac{\sigma_n}{\delta}, \quad (4.14)$$

with σ_n indicating the voltage noise RMS.

Figure 4.21 shows the ENC evaluated for the three prototypes whose measurements are presented in the previous sections. The ENC is evaluated from the set of output signals produced after charge injection. The measured values are compatible with the noise evaluated from the signals generated by the interaction of ^{55}Fe X-rays with

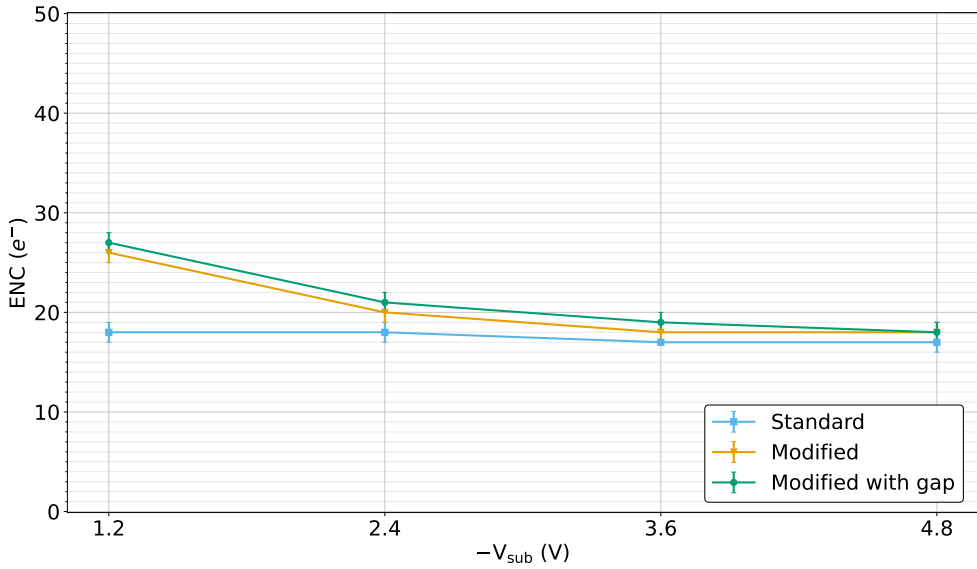


Figure 4.21 Equivalent Noise Charge evaluated for the three different pixel designs.

the APTS-OA prototypes. The dependence of the ENC with the applied reverse bias voltage as well as the difference observed among the three pixel variants can be explained by considering the input capacitance characteristics shown in Figure 4.20. In fact, since the voltage noise RMS is weakly dependent on the applied reverse bias voltage and on the pixel design, the ENC shows a dependence to V_{sub} similar to the one shown by the pixel input capacitance, which enters the term δ .

The result presented above justifies the choice of using a threshold of $100 e^-$ to determine the pixel cluster size, as this is at least about four times larger than the ENC for any measured configuration, with subsequent negligible probability of including a noise hit in the cluster.

4.9.2 Front-end time jitter

The term *time jitter* denotes the fluctuations in the measured threshold crossing time around an average value for a set of identical test pulses sent as an input to a circuit. The voltage noise introduced by the system is the source of the fluctuations in the signal time at the output. As already introduced in Equation 4.5, the slope-to-noise ratio is proportional to the circuit time jitter.

From an experimental point of view, the time jitter is the width of the distribution of the output signal times generated by a set of identical input pulses. Since the pulsing

circuit of the APTS-OA readout system (cf. Section 4.3) is not provided with a precise time reference that allows to measure the moment when charge is injected in the pixel front-end circuit, the time jitter is evaluated from the distribution of the threshold time difference between the output signals of two of the pixels connected to the oscilloscope. Under the assumption that the two considered pixels equally contribute to the measured distribution, the jitter of one pixel is quantified as the RMS of the distribution divided by $\sqrt{2}$. The measurement is repeated by sending test pulses of different amplitude V_h ranging between 300 mV and 1200 mV with the devices under test operated at varying reverse bias voltage, considering as signal time the time when the output pulse reaches 50% of its full amplitude. For each configuration, 1000 pulses are sent. The charge injected in the front-end circuit by sending a pulse of amplitude V_h can be calculated by looking at the small signal equivalent circuit of Figure 4.17a. If one defines $C_h = (C_{inj} \cdot C_{input}) / (C_{inj} + C_{input})$, i.e. the total capacitance seen by the voltage source V_h , the injected charge is then $Q_{inj} = C_h \cdot V_h$. By combining Equation 4.12 and Equation 4.13, it is possible to write:

$$Q_{inj} = C_h \cdot V_h = \frac{C_{inj}}{C_{inj} + C_{input}} \cdot C_{input} \cdot V_h = (1 - \gamma_{GC}) \cdot C_{inj} \cdot V_h. \quad (4.15)$$

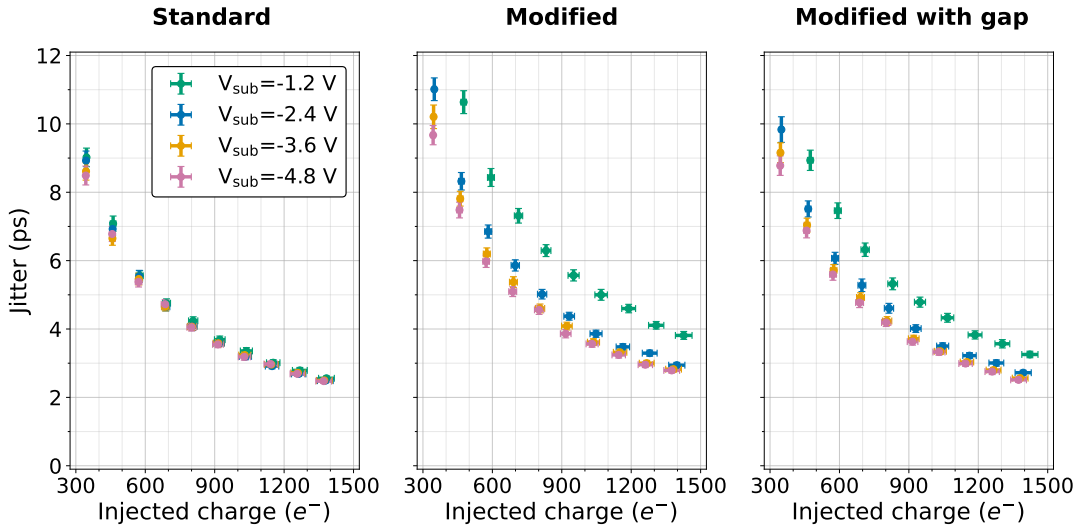


Figure 4.22 Time jitter measured for three structures based on the three different pixel designs at different amount of charge injected in the front-end circuit.

Figure 4.22 shows the results of the measurement described above. Each data point

is expressed as the average of the jitter measured from the signal time difference distributions for all the possible combinations of the central four pixels of the matrix. The uncertainty on the measured time jitter is expressed with the vertical error bars accompanying each data point, while the horizontal error bars represent the uncertainty on the injected charge.

As for the Equivalent Noise Charge, the differences observed among the jitter curves are due to the characteristic input capacitance of each pixel layout variant. The gradual decrease in input capacitance with enhanced reverse bias voltage results into an improved signal-to-noise ratio, hence a reduced time jitter (cf. Equation 4.5). For the standard type sensor, the reduced effect of the reverse bias voltage on the input capacitance translates into a negligible difference in time jitter curves measured at different V_{sub} . For the modified pixel designs, the stronger effect of the reverse bias voltage on the input capacitance, and therefore on the noise, makes the beneficial effect of a V_{sub} increase to reduce the jitter more evident.

For a structure operated at $V_{\text{sub}} = -4.8 \text{ V}$, i.e. the operation condition where the input capacitance converges to about 2 fF for all the three pixel variants, the front-end jitter is of the order of 10 ps for an amount of injected charge of $350 e^-$ while it approaches 2 ps for an amount of charge of $1400 e^-$.

4.10 Energy straggling and epitaxial layer thickness estimate

As pointed out in Section 2.5, the number of electron-hole pairs N_{e-h} generated by a minimum ionizing particle travelling through a thin silicon layer is a stochastic quantity, of which the probability density function is described by the convolution of a Landau function with a Gaussian function, also known as Langaus function. The full width at half maximum (FWHM) and the most probable value (MPV) of the function depend on the sensor thickness. Under the assumption that full charge is collected within a cluster, the cluster signal is then proportional to the energy deposited by the incoming particle (cf. Section 2.5).

Figure 4.23 shows the cluster charge distributions, also referred to as straggling functions, of the signals produced by a $120 \text{ GeV}/c$ positive hadron beam traversing a modified with gap type sensor operated at $V_{\text{sub}} = -1.2 \text{ V}$, -2.4 V and -4.8 V . A clustering threshold of $100 e^-$ is applied to identify pixels around the seed belonging to the cluster. The cluster charge spectra are fitted with a Langaus function, with the fitting parameters Δ_p , ξ and σ representing the most probable energy loss (MPV), the Landau parameter and the standard deviation of the Gaussian, respectively. The three distributions are almost overlapped, suggesting that the epitaxial layer is already

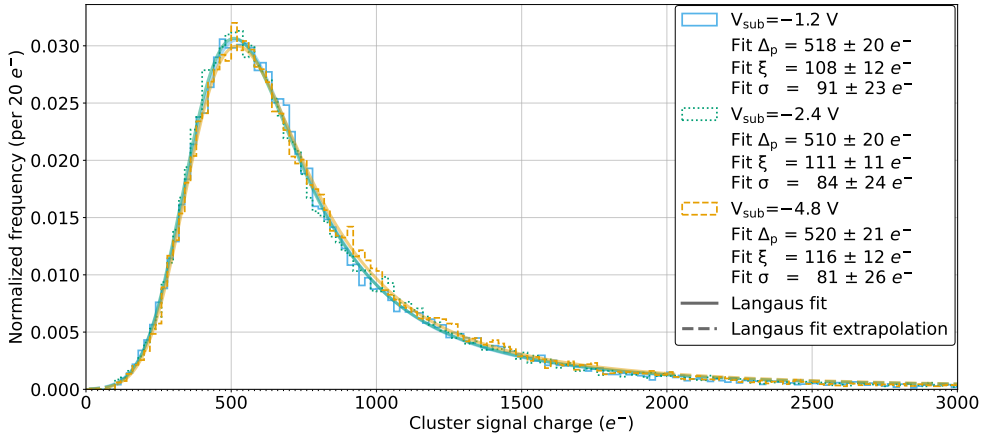


Figure 4.23 Comparison of cluster signal charge distributions of a modified with gap type sensor operated at different reverse substrate voltages and measured with 120 GeV/c positive hadrons. The distributions are fitted with a Langaus function.

approximately fully depleted at reverse substrate voltages of -1.2 V and -2.4 V. Under the assumption that all the collected charge is generated in the epitaxial layer, it is possible to infer its thickness x from the fitting parameters with a simple approximation of the energy E deposited in the detector sensitive volume:

$$E = \left(\frac{dE}{dx} \right) x \rightarrow x \approx \frac{\Delta_p W}{\left(\frac{dE}{dx} \right)}, \quad (4.16)$$

where the deposited energy is approximated by the product of the distribution MPV with the factor $W = 3.6 \text{ eV}/e^-$ (i.e. the average energy to generate an electron-hole pair in silicon) and the most probable energy loss per unit length is retrieved from the empirical expression reported in Equation 2.31. For a sensor of thickness $10 \mu\text{m}$, i.e. the nominal epitaxial layer thickness, the corresponding dE/dx is $182 \text{ eV}/\mu\text{m}$. By putting this value into Equation 4.16 in combination with the Δ_p parameter obtained from the fit of the three distributions, one achieves an epitaxial layer thickness of $10.2 \pm 0.4 \mu\text{m}$, $10.1 \pm 0.4 \mu\text{m}$ and $10.3 \pm 0.4 \mu\text{m}$, respectively. The reported uncertainties are statistical only. The three values are in good agreement with each other and with the nominal one. As it will be discussed in Chapter 6, the contribution of the charge generated in the substrate which eventually reaches the epitaxial layer via diffusion is not negligible. This reflects into an effective thickness of the epitaxial layer lower than $10 \mu\text{m}$.

4.11 Discussion and conclusion

The APTS-OA prototypes are developed with the aim of studying the analog properties of 10 μm pitch pixel sensors implemented in TPSCo 65 nm CMOS imaging process. In this chapter, the comparison of the performance of sensors based on different variants of the CMOS process is studied with charge injected in the pixel front-end circuit by test pulses or X-rays from an ^{55}Fe radioactive source. Moreover, the straggling functions of a modified with gap sensor measured with a minimum ionizing charged particle beam are shown.

The influence of the V_{reset} parameter on the sensor's performance is investigated and the optimal working point in terms of linearity and signal-to-slope ratio is chosen. The measurements with ^{55}Fe X-rays highlight the charge collection properties of the three different pixel designs. While the standard pixel layout, which does not reach full depletion of the epitaxial layer even for the highest applied reverse substrate voltage of -4.8 V , is characterized by charge collection via thermal diffusion and charge sharing among neighboring pixels, the introduction of a low dose n-type blanket below the collection electrode in the modified pixel designs makes the charge collection by drift a dominant phenomenon, with suppression of the charge sharing and reduction of the charge collection time. The beneficial effect of the reverse substrate voltage on the sensor's performance, already observed with the ^{55}Fe measurements, is quantified with the pixel capacitance studies. The influence of the reverse substrate voltage is, however, limited on the standard pixel variant while it is crucial for the modified and modified with gap type pixels, where the input capacitance can be reduced down to 2 fF for a voltage of -4.8 V . The enhancement of the reverse bias voltage can be also seen as a noise reduction strategy since it diminishes the Equivalent Noise Charge (ENC), and therefore the time jitter introduced by the front-end circuit. Finally, the energy straggling functions of a modified with gap type device measured with a minimum ionizing particle beam show a most probable value which is compatible with the nominal epitaxial layer thickness of 10 μm . Moreover, for this pixel variant, full depletion is reached already with a reverse substrate voltage of -1.2 V .

The change in the sensor's characteristics introduced by the process modification with respect to the standard design is experimentally proven and discussed in this chapter. No major differences are observed, however, between the modified and modified with gap pixel designs for the 10 μm pixel pitch, non-irradiated APTS-OA samples.

The timing performance of monolithic sensors implemented in 65 nm CMOS technology, with particular attention to the modified pixel designs, is discussed in the next chapter.

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CHAPTER 5

In-beam measurements of 65 nm CMOS analog structures

THE APTS-OA prototypes are excellent vehicles to study the charge collection and the timing properties of sensors implemented in TPSCo 65 nm CMOS imaging process since they provide direct access to the analog signal induced at the pixel electrode by an incoming particle.

The previous chapter provides insights on the increased charge collection performance introduced by the CMOS process modification by comparing the behavior of the three different APTS-OA pixel variants illuminated with ^{55}Fe X-rays. This picture is completed by the present chapter, which contains a paper describing the beam test campaign carried out at the CERN Super Proton Synchrotron (SPS) [1] facility. It targeted the characterization of APTS-OA sensors based on the modified CMOS processes. Because of the limited beam time available, the latter were prioritized over the standard CMOS process, as they are expected to have a superior time resolution. Besides the study of the detection efficiency and the spatial resolution achieved by the test structures, emphasis is put in the evaluation of the time resolution obtained by the measured APTS-OA prototypes.

The paper is titled *Time performance of Analog Pixel Test Structures with in-chip operational amplifier implemented in 65 nm CMOS imaging process* and has been published in Nuclear Instruments and Methods A [2].

The chapter closes with a section showing the comparison of the time resolution of three APTS-OA chips implementing the different TPSCo 65 nm CMOS processes measured with electrons from a ^{90}Sr radioactive source.

Time performance of Analog Pixel Test Structures with in-chip operational amplifier implemented in 65 nm CMOS imaging process

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Abstract In the context of the CERN EP R&D on monolithic sensors and the ALICE ITS3 upgrade, the Tower Partners Semiconductor Co (TPSCo) 65 nm process has been qualified for use in high energy physics, and adopted for the ALICE ITS3 upgrade. An Analog Pixel Test Structure (APTS) featuring fast per pixel operational-amplifier-based buffering for a small matrix of four by four pixels, with a sensor with a small collection electrode and a very non-uniform electric field, was designed to allow detailed characterization of the pixel performance in this technology. Several variants of this chip with different pixel designs have been characterized with a 120 GeV/ c positive hadron beam. This result indicates that the APTS-OA prototype variants with the best performance achieve a time resolution of 63 ps with a detection efficiency exceeding 99% and a spatial resolution of 2 μm , highlighting the potential of TPSCo 65 nm CMOS imaging technology for high-energy physics and other fields requiring precise time measurement, high detection efficiency, and excellent spatial resolution.

5.1 Introduction

In the field of high-energy physics, Monolithic Active Pixel Sensors (MAPS) have emerged as a promising technology for vertex detectors, demonstrating potential to revolutionize tracking capabilities in future experiments [3, 4]. Their innovative design, integrating readout circuitry with the detection volume in single, commercially fabricated chips, facilitates ultra-thin, large-scale tracking detectors – a breakthrough for precision and scalability in research.

As high-energy physics experiments evolve, they are expected to cope with higher interaction rates and to resolve several primary interaction vertices as well as vertices from secondary decays [5]. This trend demands pixel detectors with enhanced spatial resolution and superior timing capabilities, essential for precise tracking in dense particle environments [6]. Recent developments in the 180 nm TowerJazz CMOS technology have led to significant improvements. Sensor modifications have enabled improved depletion [7] and significantly accelerated charge collection especially for hits near the pixel edge [8], allowing for time resolutions between 100 and 120 ps [9, 10].

A new generation of MAPS detectors is being developed for the third generation ALICE Inner Tracking System (ITS3) [11–13], using the Tower Partners Semiconductor Co. (TPSCo) 65 nm CMOS Image Sensor Process [14] introducing similar sensor modifications as in the 180 nm technology [8, 10]. This 65 nm technology enables higher circuit densities and hence more advanced readout circuitry can be fitted in the same pixel pitch, allowing for more precise timing measurements. An Analog Pixel Test Structure (APTS), equipped with fast individual Operational Amplifier

(OA)-based buffering was produced to evaluate the intrinsic timing performance of the sensors in this new technology. Several variants of the chip with different pixel designs were implemented and characterized in Ref. [15, 16] and are summarized in the next section. The results of a study carried out during a test beam campaign with positive hadrons are presented in this paper, with a focus on the sensor timing performance.

5.2 The APTS-OA

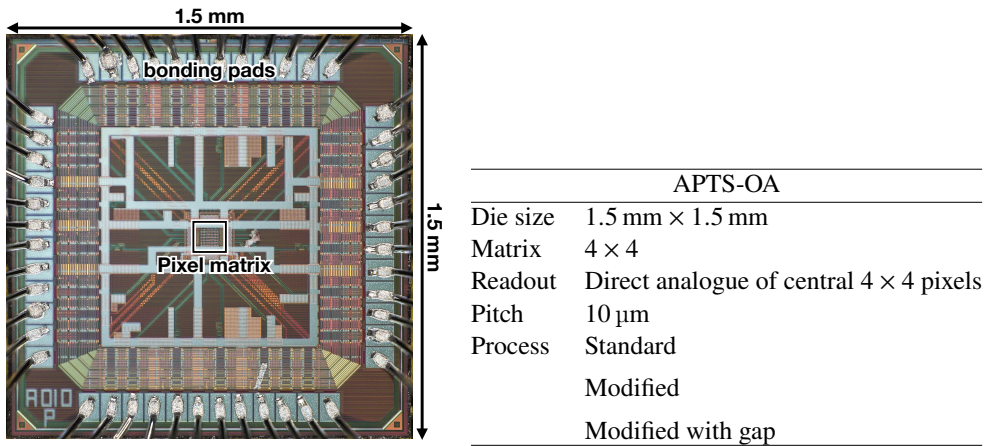


Figure 5.1 Photograph of the APTS-OA taken with a microscope. **Table 5.1** Main characteristics of the APTS-OA.

The APTS-OA measures $1.5 \times 1.5 \text{ mm}^2$ and features a 4×4 squared $10 \mu\text{m}$ pitch pixel matrix directly buffered to output pads for readout and controlled by a set of external reference currents and voltages. This matrix is surrounded by dummy pixels that help to reduce the electric field distortion effects at the edges of the matrix. In Figure 5.1, the APTS-OA chip is shown where, going from the center to the periphery, the pixel matrix, and the bonding pads can be observed. Table 5.1 presents the primary characteristics of the chip detailed below.

The sensor can be reverse biased by applying a negative voltage referred to as V_{sub} to the substrate and p-wells down to a minimum of -4.8 V .

5.2.1 Sensor variants

The APTS was produced with three process variants of its sensor, starting from a standard imaging CMOS design and introducing modifications resulting in faster charge collection and reduced charge sharing [7, 15, 17].

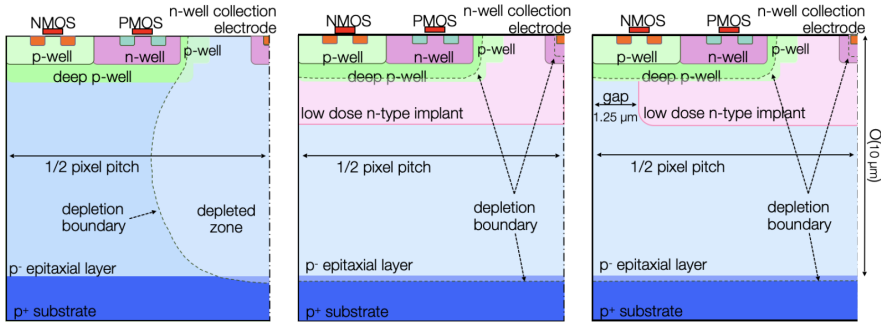


Figure 5.2 Schematic cross section of the three pixel process variants of the APTS. From left to right: standard, modified featuring a low dose deep n-type implant, and modified with gap employing a low dose deep n-type implant with a gap at the pixel's edges. Not to scale [15].

- **The standard process** (cf. Fig. 5.2 left) is formed by an n-well collection electrode of about $1\ \mu\text{m}$ diameter on a high-resistivity p-type epitaxial layer, grown on top of a low-resistivity p-type substrate. In this structure, the depletion extends from the small n-well electrode resulting in a balloon-shaped depleted zone covering only part of the epitaxial layer. Charge collection outside this region happens mostly by diffusion, leading to long and non-uniform collection times but also to significant charge sharing [18]. A deep p-well, located at about $2\ \mu\text{m}$ from the collection electrode, separates circuitry n-wells from the epitaxial layer, allowing to use PMOSs as well as NMOSs in the pixel matrix without competing with the electrode for charge collection.
- **The modified with blanket implant process**, for brevity called 'modified' in the following, (cf. Fig. 5.2 center) differs from the standard structure for the addition of a low-dose n-type implant in the epitaxial layer, resulting in a planar junction over the full pixel that helps in achieving full depletion of the epitaxial layer.
- **The modified with an implant with gap process**, called 'modified with gap' in the following, (cf. Fig. 5.2 right) is similar to the modified process but the deep n-type implant no longer covers the full pixel: a gap is introduced near the pixel edge to create a lateral field pushing the signal charge towards the collection electrode, thus decreasing collection time (as demonstrated in the simulation [8] for the 180 nm CMOS TowerJazz technology) and charge sharing.

Characterization of a version of the APTS with source follower output buffers (APTS-SF) has demonstrated the improvements described above for the 65 nm technology [15, 19].

5.2.2 Analog circuit

The analog circuit of APTS-OA is depicted in Fig. 5.3. An analog front-end powered at 1.2 V (AVDD) is connected to the collection electrode of each pixel (IN) and buffers its signal to an output pad (BOARD). To do so, the circuit is composed of several buffering stages: a low input capacitance stage with two source followers buffering the IN signal to OUT1 and OUT2, respectively, and a fast operational amplifier driving the output stage BOARD. The circuit also provides reset current to the sensor and allows to inject charge at the input of the front-end via a pulsing circuitry. Most of the analog circuit is implemented in the pixel matrix, but due to lack of area the operational amplifiers and output stages are located at the periphery immediately surrounding the pixel matrix.

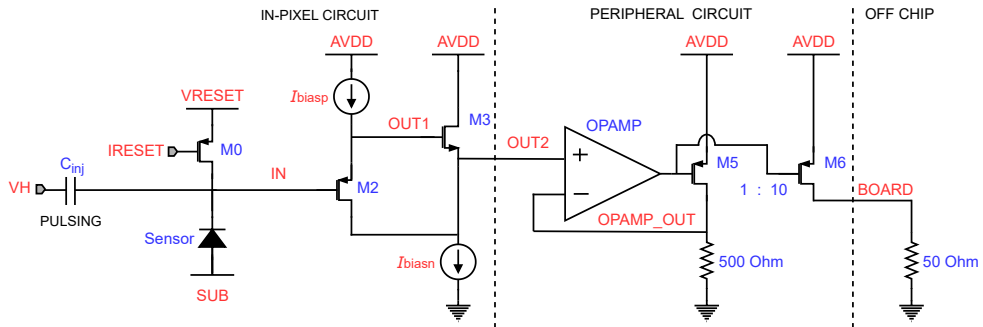


Figure 5.3 Left: APTS-OA front-end circuit with the circuitry inside the pixel. Right: circuitry located in the periphery of the matrix. The off chip line to the measurement system is also represented.

In case there is no hit, the transistor M0 only compensates for the leakage current of the sensor and maintains its collection electrode at a voltage close to V_{reset} . The current generated after a particle hit entails a voltage drop on the input node (IN), turning on the transistor M0 to deliver constant current I_{reset} . I_{reset} is chosen larger than the sensor leakage current to ensure that IN returns to its baseline within a few microseconds.

The collection electrode (IN) is directly connected to the input of a PMOS source follower stage M2 that makes its output OUT1 follow the input voltage. To take full advantage of the low sensor capacitance in this process, the input capacitance of

the front-end is further reduced by making the drain of M2 also follow the same voltage. This is achieved by the NMOS source follower M3 driving OUT2. These source followers are biased by two current sources: I_{biasp} and I_{biasn} .

An in-pixel pulsing circuit can inject charge in the collection electrode through a capacitance of $C_{\text{inj}} = 242 \text{ aF}$ (nominal value). The amount of injected charge is controlled by an external voltage reference (V_h) and the injection is triggered via an external signal.

The NMOS source follower output (OUT2) is connected to a high-speed (1.9 GHz unity-gain bandwidth in post layout simulation) operational amplifier (OPAMP) at the periphery of the matrix that, combined with an output stage capable of driving a 50Ω load, allows for signal termination on the board or on an oscilloscope to preserve the signal timing information. A well-controlled internal feedback loop is used for the operational amplifier to achieve better stability over a wide range of external capacitive loads [19] and the well-controlled output is copied by M6 and sent off-chip (BOARD) where the external load is.

All voltages and current biases for the front-end and the operational amplifier are externally generated and supplied via pads to the chip, where an ad hoc mirroring ratio is applied to, for example, provide a front-end reset current as low as a few tens of pA. The in-pixel and out-of-pixel power consumptions per pixel, estimated from the front-end biases, are $150 \mu\text{W}$ and 3.1 mW respectively.

The operating point was optimized using charge injection for the fastest front-end response to establish the best working condition for measuring timing. This set of parameters is referred to as the operating point, it is given to the chip which distributes it to the pixels. The operation point values are listed in App. B. Experimental optimization was necessary because the NMOS transistors are in a p-well at voltage V_{sub} , reaching values beyond the range where the transistor model was available. Consequently, an extrapolation of the model was used in simulation to establish the nominal operating point, and proved afterward to deviate significantly from measurements [20].

5.2.3 Chip readout system

Figure 5.4 shows the test setup used to operate the APTS-OA. It consists of an FPGA-based data acquisition (DAQ) board, powered at 5 V and controlled by PC via USB interface, a proximity board that hosts the analog to digital converters (ADCs) for the readout of peripheral pixels and sends power and biases to the chip, and a carrier board to which the chip is glued and bonded. More details on this system can be found in Ref. [21].

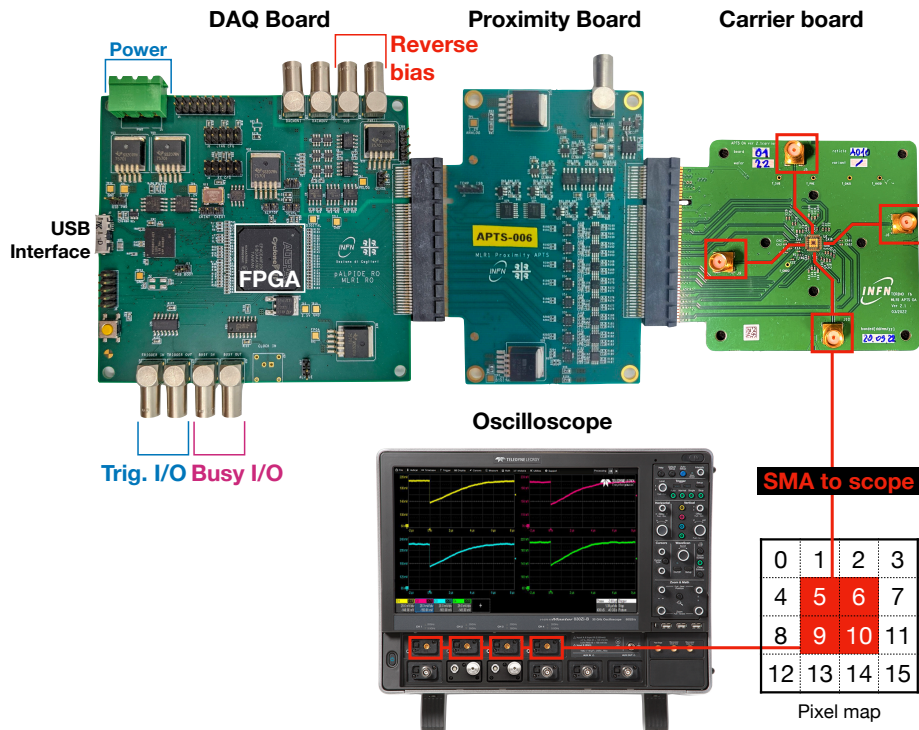


Figure 5.4 Scheme of the APTS-OA readout system. From left to right: picture of the DAQ board, hosting the firmware control FPGA as well as trigger, busy, and reverse bias connection, the proximity board, hosting ADCs for external pixel readout, and the carrier board to which the chip is glued and wire bonded. In the bottom part, a sketch of the 4×4 pixel matrix with the four inner pixels (highlighted in red) connected to an oscilloscope.

The carrier board has four high bandwidth SMA connectors soldered to the output lines of the four innermost pixels (highlighted in red in Fig. 5.4) that can be read out with an oscilloscope (Teledyne Lecroy, WaveMaster 813Zi-B, having a sampling rate of 40 GS/s and a bandwidth of 13 GHz). In the present work, only 3 out of 4 pixels will be read out with the oscilloscope. The remaining pixels (12 external plus one of the inner) are read out by analog-to-digital converters on the proximity board with a fixed sampling rate of 4 MHz.

5.3 Test Beam Measurements

To characterize the performance of the APTS-OA with respect to its time resolution, detection efficiency and spatial resolution, a beam test was conducted at the CERN-SPS H6 facility using positive 120 GeV/ c hadrons [1].

5.3.1 Test beam telescope

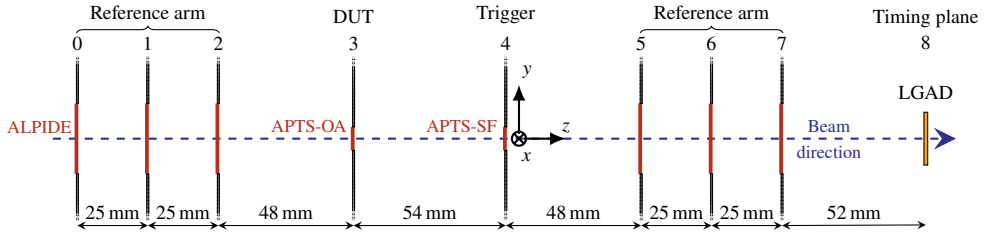


Figure 5.5 Schematic of the test beam setup showing each detector plane.

The setup, which is sketched in Fig. 5.5, consisted of nine planes, in particular:

- Planes 0, 1, 2, 5, 6, and 7, each containing an ALPIDE [22], tuned to a $100 e^-$ threshold at -3 V reverse substrate bias, for track reconstruction.
- Plane 3: an APTS-OA, as a device under test (DUT), placed on xy moving stages.
- Plane 4: an APTS-SF [15], in the modified process with $15 \mu\text{m}$ pitch is used as trigger plane. Only the central four pixels were activated for the trigger signal generation in order to achieve a coverage slightly larger than the DUT. The modified process was chosen to enhance single pixel clusters and therefore the probability to trigger on a seed signal. The APTS-SF plane is mounted on xy moving stages and is operated with a -1.2 V reverse substrate bias and all other biases at the optimal operating point, based on Ref. [15].
- Plane 8: a Low Gain Avalanche Detector (LGAD) produced by Fondazione Bruno Kessler [23] as a time reference, operated at 110 V bias voltage. The signal is amplified with a commercial external circuit (MiniCircuits TB-409-52+) and readout with one channel of the oscilloscope.

The reference system is defined with the positive z -axis along the beam direction and with x - and y -axis defining the sensor planes.

Two chips having different sensor processes were considered in this study: the modified and the modified with gap variants, as these processes demonstrated the best performance in terms of charge collection [19]. The substrate bias (V_{sub}) was varied from -1.2 V to -4.8 V with steps of 1.2 V, consequently varying the depletion and electric field in the sensor. Table 5.2 shows the acquired number of triggers recorded for the different configurations. A larger sample of events was accumulated for the modified with gap structure to study the in-pixel contribution of the lateral electric field.

V_{sub}	Modified with gap	Modified
-1.2 V	290,000	15,000
-2.4 V	334,050	15,000
-3.6 V	15,000	20,000
-4.8 V	258,600	58,100

Table 5.2 Total number of events recorded during test beam measurements in each configuration.

5.3.2 Data reconstruction and analysis

DUT signal extraction The data recorded in the telescope, which includes the analog waveform from each pixel, was analyzed offline. Figure 5.6 shows an example of a typical signal acquired with the oscilloscope. In the inset at the left bottom, the full waveform is shown, while the main plot highlights the main parameters used to extract the amplitude of the waveform:

- the time zero (t_0 showed as a pink marker in Fig. 5.6), estimated as the minimum of the signal's derivative [24];
- the baseline, calculated as the average of 100 points (corresponding to a time interval of 2.5 ns), 15 ns before t_0 (orange segment in Fig. 5.6);
- the underline, computed as the average of 100 points (2.5 ns), 15 ns after t_0 , corresponding to the waveform minimum (green segment in Fig. 5.6);
- the signal amplitude, determined as the difference between the underline and the baseline;

These values are chosen to accurately extract the amplitude of the signal while being robust to noise and the low frequency variation of the baseline. For the external

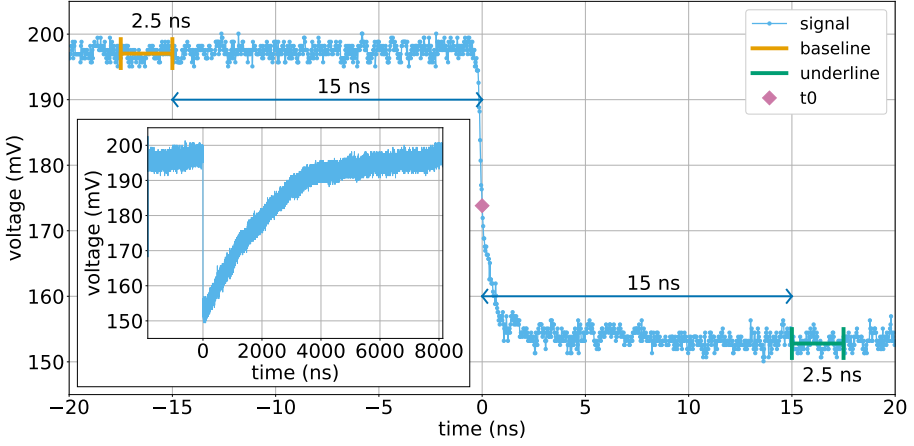


Figure 5.6 Typical signal acquired by the oscilloscope with baseline, underline, and t_0 definitions. The x -axis is shifted to put t_0 at the origin to highlight the time intervals for the baseline and underline definitions.

pixels and one of the 2×2 central ones the signal amplitude is calculated as the difference between the baseline, defined as the 4th sample before the minimum of the signal, corresponding to its underline, and the minimum itself, following the definition adopted in Ref. [15]. This definition avoids short-range auto-correlation among points and is not influenced by the signal edge.

DUT signal calibration To merge the information from different pixels and compare results taken under different working conditions, the measured signal amplitude is converted into the charge collected by the sensor (expressed in e^-). The calibration is performed analysing the X-ray spectrum from a ^{55}Fe source: the $^{55}\text{Mn} - K_\alpha$ and $^{55}\text{Mn} - K_\beta$ peaks are fitted simultaneously with 2 Gaussian functions to account for the partial overlap of the peaks at low reverse bias voltages. Then the mean of the $^{55}\text{Mn} - K_\alpha$ peak is used to perform the conversion to electrons with the following formula:

$$Q = V_{\text{out}} \frac{E(K_\alpha)}{V_{\text{mean}}(K_\alpha) \epsilon}, \quad (5.1)$$

where $E(K_\alpha)$ is the energy of the $^{55}\text{Mn} - K_\alpha$ photon, $V_{\text{mean}}(K_\alpha)$ is the mean of the $^{55}\text{Mn} - K_\alpha$ peak estimated from the fit, and ϵ is the average energy required to produce an electron hole pair in silicon. For this method the linearity of the energy response of the APTS is assumed, since it has been demonstrated in Ref. [15].

The signal amplitude spectrum from a single pixel of the modified with gap sensor operated at $V_{\text{sub}} = -4.8 \text{ V}$ is shown in Fig. 5.7.

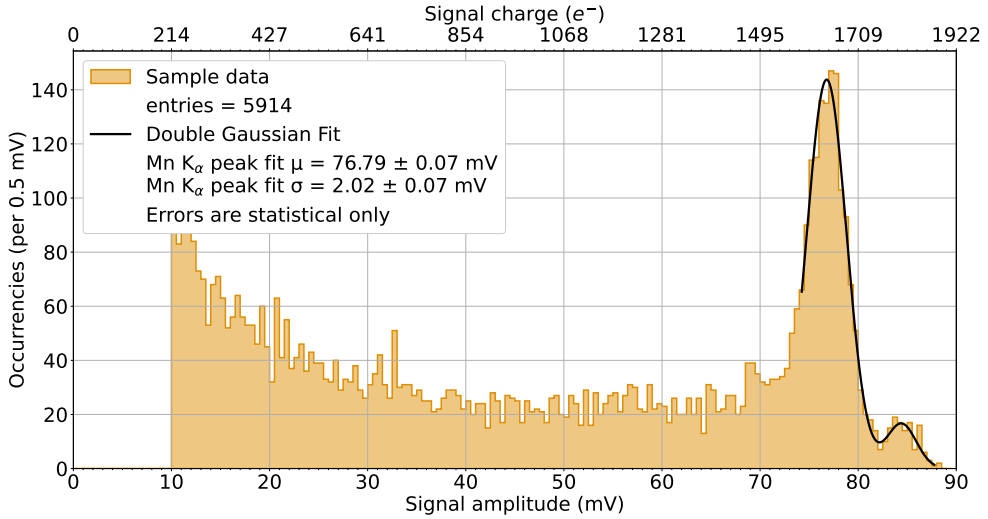


Figure 5.7 Amplitude distribution of signals acquired with the ^{55}Fe source for a single pixel read out with the oscilloscope. The $^{55}\text{Mn}\text{-}K_{\alpha}$ and K_{β} peaks are fitted together with the sum of 2 Gaussian functions.

Clustering Data from DUT, trigger, and tracking planes have been analyzed with the Corryvreckan software framework [25]. Adjacent pixels recording a charge above a certain threshold form a cluster. The clustering threshold, introduced in the DUT data analysis to emulate the effect of a discriminator, is only applied offline and not during data taking. Each signal amplitude is converted into units of electrons following the calibration procedure described above. The seed pixel is defined as the one collecting the highest amount of charge within the cluster and the charge-weighted center-of-gravity defines the cluster position.

Track reconstruction The Corryvreckan framework uses the General Broken Line (GBL) algorithm [26] to reconstruct the particle tracks by fitting the cluster position on the reference planes and taking into account the multiple scattering effect through the detector material budget. Software alignment of the telescope planes has been performed in subsequent steps in which the different planes are shifted and rotated iteratively with respect to a chosen reference plane to increase the tracking quality. These tracks are then interpolated at the plane of the DUT. The six ALPIDE planes

and the trigger plane (APTS-SF) are included in the tracking, excluding the DUT in order to obtain unbiased results. The following quality selection criteria are applied to filter the data for the analysis:

- a cluster is required in each tracking plane;
- tracks are selected based on the quality of the fit, such that $\chi^2/\text{dof} < 5$, where dof stands for the number of degrees of freedom;
- only events with a single reconstructed track are selected, where an event has to be triggered by the APTS-SF (cf. Sec. 5.3.1, Plane 4);
- DUT clusters are associated to tracks passing within a radial distance of $15\text{ }\mu\text{m}$. A study was performed to select the proper association window radius, choosing it in order to guarantee the independence of the efficiency from this parameter (cf. App. C).
- a Region Of Interest (ROI) is set to include only the associated tracks crossing one of the three central pixels read out via the oscilloscope, in order to avoid border effects.

The applied selection cuts reduce the statistics to roughly 20% of the recorded samples quoted in Tab. 5.2.

Detection efficiency analysis In order to estimate the detection efficiency, a cluster is searched on the DUT plane, within the ROI, for each track. The detection efficiency is computed as the ratio between the number of tracks providing an associated cluster in the DUT and the total number of tracks crossing the ROI. It is worth noting that the choice of the above mentioned association window radius allows one to estimate the efficiency without any bias, taking into account that the tracking resolution is much smaller, being equal to $\sigma_{\text{track}} = 1.8\text{ }\mu\text{m} \pm 0.1\text{ }\mu\text{m}$, as obtained by the telescope optimiser tool [27]. Moreover, to assess the chip noise, an analysis of the baseline fluctuations was conducted (cf. App. D). The results in the following figures are shown for thresholds above $75\text{ }e^-$, 3 times the maximum noise RMS.

Spatial resolution analysis For this analysis, the so-called η -algorithm [28, 29] has been applied to correct for the non-linear charge-sharing mechanism among the pixels. Residual distributions are obtained by evaluating the distance between the intercept of each track on the DUT plane (reconstructed position) and the associated

cluster position (corrected with the η -algorithm), in both the x and y directions. The spatial resolutions σ_x and σ_y in, respectively, the x and y directions are computed by quadratically subtracting the estimated telescope tracking resolution σ_{track} from the standard deviation of the residual distributions in the x and y direction, respectively. The final position resolution is then defined as the arithmetic average between σ_x and σ_y and it will simply be referred to as spatial resolution in the rest of the paper.

Time resolution analysis The sensor time residuals are computed as the difference between the time when the APTS-OA DUT seed pixel signal reaches 10% of its full amplitude and the time reference provided by the LGAD in the beam telescope (cf. Fig. 5.5). Selecting a constant fraction of the signal amplitude aims at mitigating time walk effects in the time resolution; 10% proved to provide the lowest RMS of time residual distribution (cf. App. E). A similar method is applied to the LGAD signals, for which the signal leading edge time at 40% of its amplitude is chosen as it provides the best time resolution. Consequently, the distribution of the time residuals, namely the time difference between the signals of the DUT and the time reference, is defined as follows:

$$\Delta t = t_{10\%}^{\text{DUT}} - t_{40\%}^{\text{LGAD}} . \quad (5.2)$$

Only the seed signals of the three pixels read out by the oscilloscope can be used in the analysis, being the only ones providing precise time information. This further reduces the events previously selected by cluster association via tracking by another 15%, resulting in a number of available signals for the time resolution analysis equal to 17% of the number of recorded triggers reported in Tab. 5.2.

Finally, the LGAD time resolution $\sigma_{\text{LGAD}} = 30 \text{ ps} \pm 3 \text{ ps}$ ¹ is quadratically subtracted from the standard deviation of the time residuals to calculate the time resolution of the DUT σ_t :

$$\sigma_t = \sqrt{\sigma_{\Delta t}^2 - \sigma_{\text{LGAD}}^2} , \quad (5.3)$$

as the two quantities are assumed to be independent.

5.3.3 Results and discussion

In the following section, the results of the analysis are presented. They are grouped in three main paragraphs and results are presented in the following order: detection efficiency, spatial resolution and cluster size, and, finally, the time resolution.

¹ The LGAD time resolution was characterized with a positive hadron beam (cf. Ref. [30]).

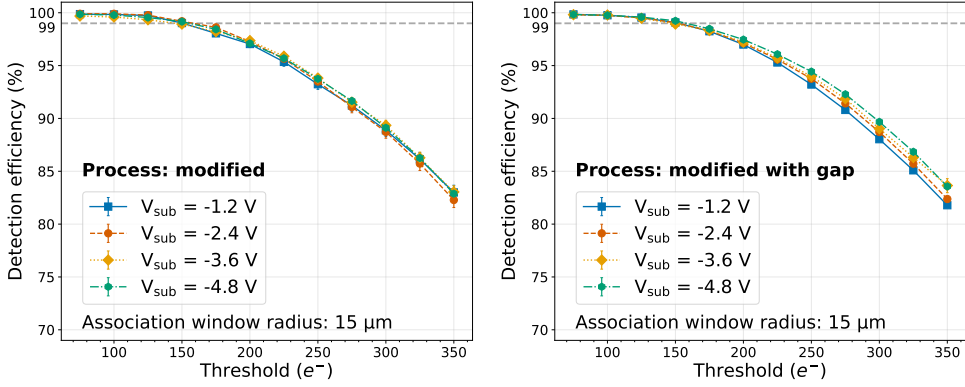


Figure 5.8 Detection efficiency for the modified (left) and modified with gap (right) pixel processes as a function of the applied threshold and for different V_{sub} . The dashed line in both plots indicates the 99% detection efficiency.

Detection efficiency Figure 5.8 shows the detection efficiency for the modified (left) and modified with gap (right) process as a function of the threshold at different reverse bias voltages. The results are plotted for thresholds exceeding 3 times the RMS of the noise distribution to ensure unbiased efficiency values. As expected, a clear decreasing trend of the detection efficiency with the increasing threshold can be observed for both the modified and modified with gap process.

Both pixel variants achieve a detection efficiency higher than 99% up to a threshold of $150 e^-$, in agreement with the results obtained in Ref. [15], offering a comfortable operational range for the sensor. Furthermore, achieving a high detection efficiency is essential to prevent any bias in time resolution. No significant differences are observed between the two variants for this 10μ m pixel pitch at the threshold of $100 e^-$ (cf. App. F).

Spatial resolution and cluster size Figure 5.9 shows the spatial resolution, computed as described in Sec. 5.3.2, and the average cluster size as a function of the applied threshold. The cluster size decreases with increasing threshold, degrading the spatial resolution, which, nevertheless, for both processes at all biases, is always better than the pixel pitch divided by $\sqrt{12}$. For both processes, the cluster size also reduces with increasing the reverse bias, because of the enhanced lateral electric field, resulting in a reduced charge sharing. This V_{sub} dependence, clearly visible at lower thresholds, gradually becomes undetectable with increasing threshold as the information from low amplitude signals is removed. To better visualize the cluster size, the distributions at

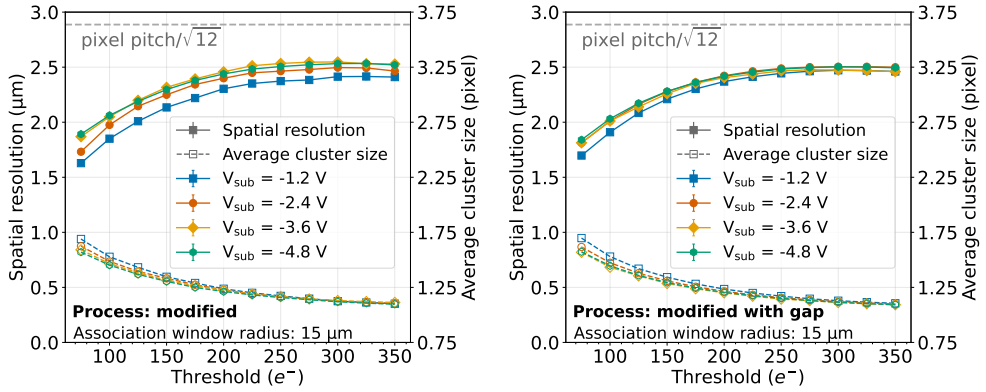


Figure 5.9 Spatial resolution and cluster size as a function of the applied threshold for the modified (left) and modified with gap (right) structures, comparing different reverse substrate voltages in different colors. The grey dashed line represents the pixel pitch divided by $\sqrt{12}$.

different reverse bias are shown in App. G. All the observations are in agreement with the results from APTS-SF (cf. Ref. [15]).

Time resolution Figure 5.10 shows, as an example, the time residual distribution for the DUT based on the modified with gap process operated at $V_{\text{sub}} = -4.8$ V (blue histogram). The measured time reference signals are delayed with respect to the DUT ones, resulting in negative time residuals (cf. Eq. 5.2).

Despite the efforts in the analysis to reduce the dependence of the measured signal time on the signal amplitude, the longer tail towards higher time residual values suggests a remaining presence of time walk, confirmed by Fig. 5.11 (top) which shows the correlation of time residuals and DUT seed signal charge. This can be explained by considering that a time measurement based on constant amplitude fraction only suppresses time walk in case of a constant signal shape [31]. Since the acquired analog waveforms differ in shape depending on the amount of collected charge and on the position of the ionization within the pixel (cf. App. H), a correction is needed to compensate for these effects.

Figure 5.12 shows the dependence of the deviation from the mean value of the non-corrected time residual distribution reported in Fig. 5.10 and of the cluster size on the in-pixel reconstructed track incidence position. It can be seen that, on average, lower time residual values, i.e. negative deviations from the mean, are associated to smaller clusters while higher time residuals, i.e. positive deviations from the mean,

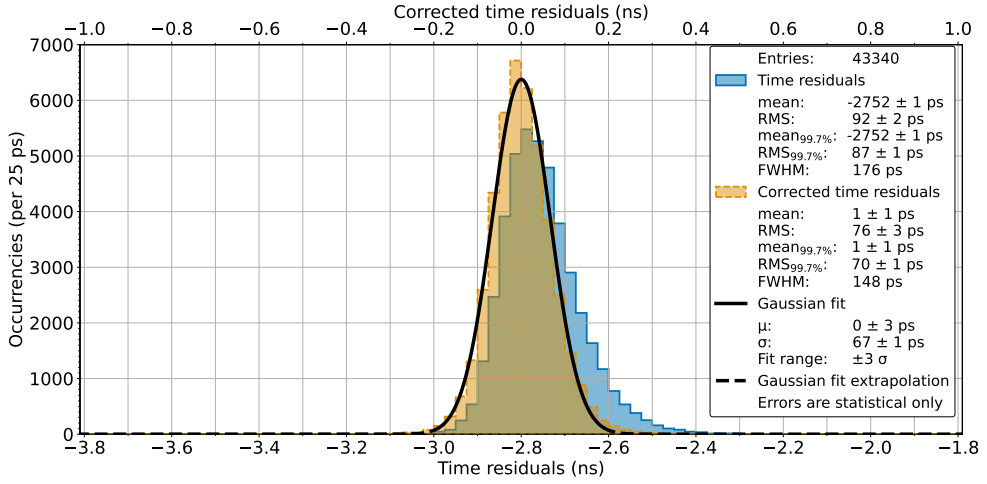


Figure 5.10 Time residuals measured for the modified with gap process DUT operated at $V_{\text{sub}} = -4.8$ V, before (blue distribution, bottom horizontal axis) and after (orange distribution, top horizontal axis) time walk-like correction. The latter distribution is fitted with a Gaussian function on a range of $\pm 3\sigma$ (black solid line, dashed line for points outside the fit range).

are associated to larger ones. In other words, a slower DUT response is observed when a track hits the pixel edges or corners, where the probability of charge sharing with neighboring pixels, hence cluster size, is enhanced. The pixel cluster multiplicity can be therefore used as a proxy to account for the reconstructed track incidence position within the pixel. Single pixel clusters are likely to be related to particles colliding with the center of the pixel, larger clusters with particles hitting the border. The correlation between time residual values and associated cluster size is further highlighted by Fig. 5.13. It shows the different contributions coming from signals associated with single pixel clusters (green histogram) and from signals associated with multiple pixel clusters (red histogram). As already pointed out for Fig. 5.12, the signals associated to single pixel clusters are on average faster and contribute to a narrower distribution than signals from clusters of larger size. Moreover, the distribution associated to the latter explains the asymmetric feature of the time residuals.

The arguments presented above suggest a correction to compensate for the dependence of the time residuals on the seed signal charge and on the associated cluster size², as

² The performance of the correction based on the dependence of the time residuals on the seed signal charge and on the associated cluster size has been verified with a similar approach based on the dependence on the seed signal charge and on the reconstructed track hit coordinates, with the former producing better results.

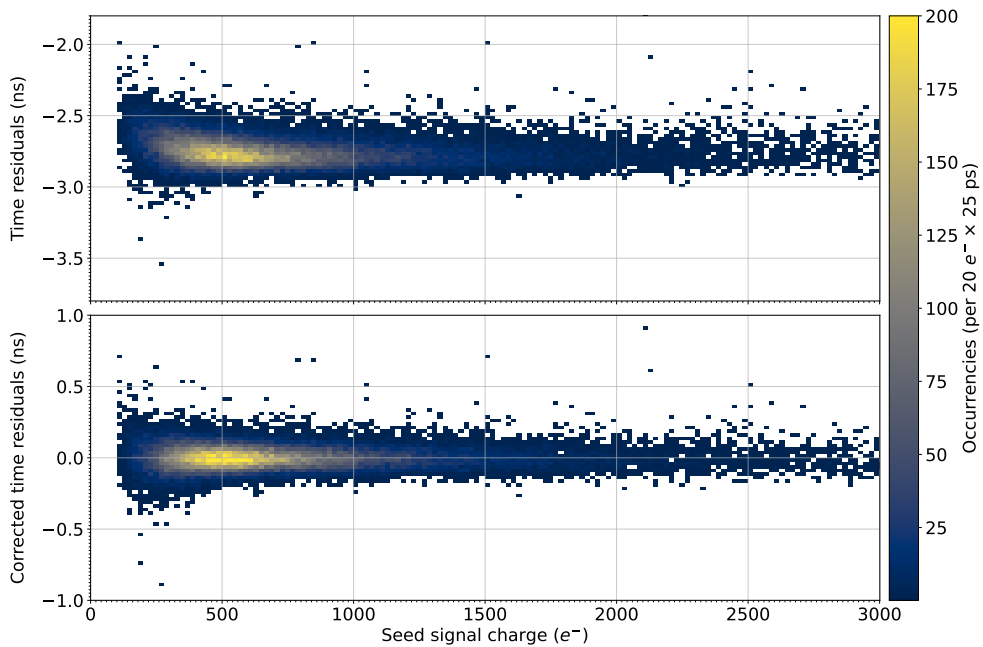


Figure 5.11 Time residuals versus seed signal charge with no correction applied (top) and after the correction (bottom) for the DUT featuring modified with gap process operated at $V_{\text{sub}} = -4.8$ V.

proposed in Ref. [10].

For this correction, a clustering threshold of $100 e^-$ (cf. Sec. 5.3.2) is adopted and the data are divided in two subsets: the first one with single pixel clusters and the second with clusters of multiplicity larger than one. For both subsets, to avoid introducing any bias in calculating the correction, the mean time residuals for each signal charge bin of one half of the dataset are interpolated with a quadratic function. The latter is then subtracted from the time residuals of the other half of the data set, and vice versa.

Figure 5.11 (bottom) shows the time residuals as a function of seed pixel signal charge after the correction discussed above. As intended, it reduces the dependence on the seed signal charge and removes its asymmetric feature, as also highlighted by the corrected time residual distribution shown in Fig. 5.10 (orange histogram).

Three estimators for the time residual distribution width are finally derived: the RMS of the entire data set, the RMS evaluated on the central 99.7 percentiles of the distribution and, for the corrected data, the standard deviation σ of a Gaussian fit within a 3σ interval. The fit is performed on the corrected data only, as, without the correction,

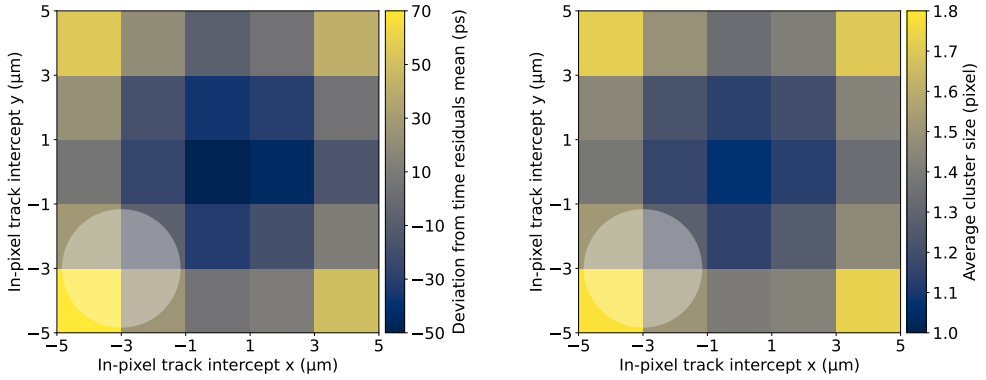


Figure 5.12 Map of the deviation from the time residuals mean value (left) and cluster size map (right) for in-pixel track incidence positions for the DUT based on modified with gap process operated at $V_{\text{sub}} = -4.8$ V. The tracking resolution is represented by the white circle ($r = \sigma_{\text{track}} = 1.8 \mu\text{m}$) in the bottom left corner of both maps.

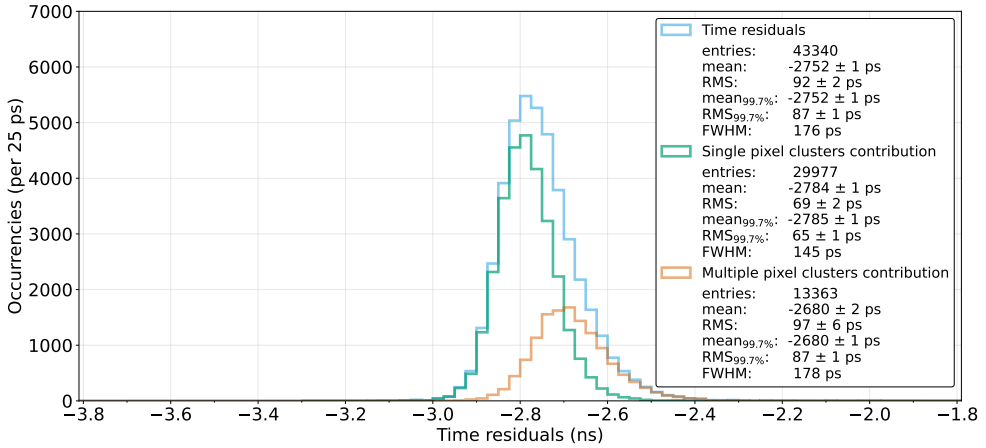


Figure 5.13 Distributions contributing to non corrected time residuals (blue histogram) divided according to the associated cluster size for the DUT implementing modified with gap process operated at $V_{\text{sub}} = -4.8$ V. The green distribution represents the time residual values related to single pixel clusters, while the red one describes the contribution of clusters with pixel multiplicity larger than one.

the residual distribution is not symmetric around the maximum. The RMS of the corrected distribution gives $76 \text{ ps} \pm 3 \text{ ps}$ and is higher than the width $\sigma = 67 \text{ ps} \pm 1 \text{ ps}$ of the Gaussian fit. The fit is comparable with the $\text{RMS}_{99.7\%} = 70 \text{ ps} \pm 1 \text{ ps}$. All the

reported uncertainties are statistical only. The time resolution of the APTS-OA is calculated according to Eq. 5.3 by considering $\text{RMS}_{99.7\%}$ as the width of the time residual distribution.

Since the correction requires a large data sample to be effective, only the data taken with the modified with gap structure operated at $V_{\text{sub}} = -1.2, -2.4$ and -4.8 V can be corrected.

The dependence of the time resolution on the reverse substrate bias voltage V_{sub} , for both modified and modified with gap sensors, is shown in Fig. 5.14.

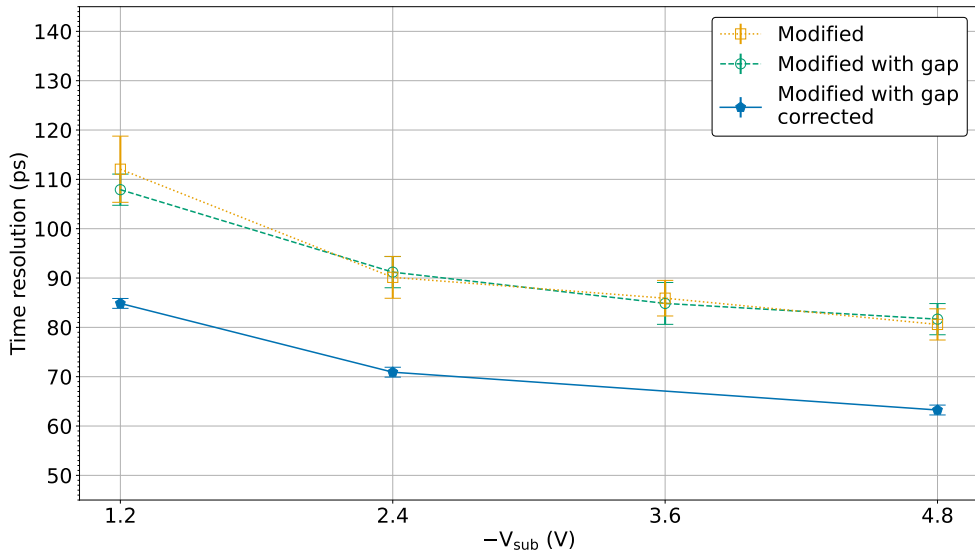


Figure 5.14 Non-corrected (open symbols, orange dotted line and green dashed line) and corrected (full symbols, blue solid line) time resolution measured for modified and modified with gap DUT process variants. A time walk-like correction, described in Sec. 5.3.2, is applied only to high statistical significance data sets, namely those measured with the modified with gap structure.

The time resolution is found to be independent of the process variant, for this $10\text{ }\mu\text{m}$ pitch. An improvement in timing performance with increasing reverse bias is observed, resulting in a resolution $\sigma_t = 63\text{ ps} \pm 3\text{ ps (stat.)}$ and $\sigma_t = 82\text{ ps} \pm 3\text{ ps (stat.)}$ at $V_{\text{sub}} = -4.8\text{ V}$ for corrected and not corrected data, respectively.

The uniformity of timing performance along the pixel surface can be studied by looking at the correlation of the time resolution with the in-pixel track position. Figure 5.15 shows the map of corrected time resolution of the modified with gap DUT operated at $V_{\text{sub}} = -4.8\text{ V}$, with hits from all the pixels grouped per associated

track hit position and projected onto one pixel area. As expected, the lowest time resolution $\sigma_t = 52 \text{ ps} \pm 4 \text{ ps}$ is measured for tracks hitting the pixel center, where the distance to the collection electrode is minimal and the electric field is maximum, and it deteriorates for incident tracks on the pixel edge ($\sigma_t = 58 \text{ ps} \pm 4 \text{ ps}$) and corner ($\sigma_t = 72 \text{ ps} \pm 4 \text{ ps}$), marked by the points A, B, and C of Fig. 5.15, respectively. The reported uncertainties are statistical only.

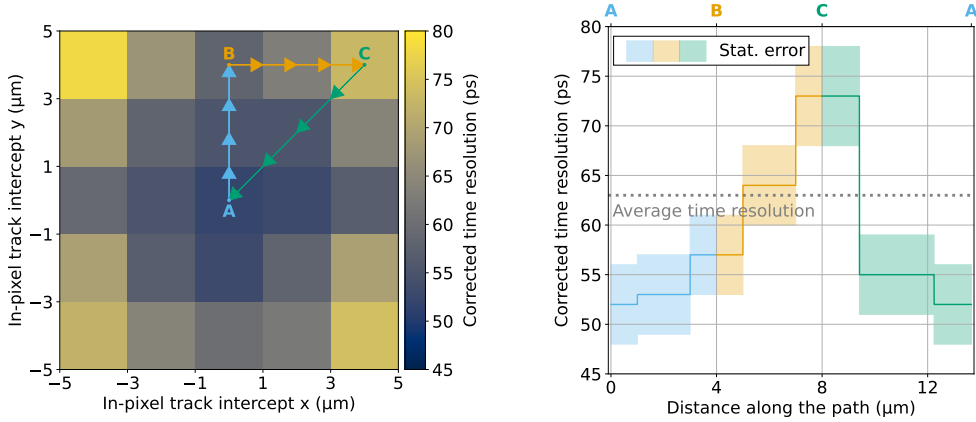


Figure 5.15 Left: corrected in-pixel time resolution of the modified with gap structure operated at $V_{\text{sub}} = -4.8 \text{ V}$. Right: time resolution variation along the path from the pixel center to the edge, and to the corner.

The obtained results demonstrate the improvement in particle detection timing performance brought by the TPSCo 65 nm CMOS technology with respect to the 180 nm CMOS technology. In fact, the best time resolution, after the correction, measured for monolithic pixel sensors implemented in 180 nm CMOS imaging technology is 106 ps [10], while a time resolution of 63 ps is achieved, after time walk correction, for the structures implemented in 65 nm CMOS technology discussed here when operated at reverse substrate voltage $V_{\text{sub}} = -4.8 \text{ V}$.

However, it is worth noticing that the study presented in this publication concentrates on the time resolution of the sensor only, while the time resolution of a full detector system will also be affected by other components, such as the readout circuitry.

5.4 Conclusions

The performance of the analog pixel test structures realized in the 65 nm TPSCo CMOS imaging technology is presented in this publication. The APTS-OA was successfully integrated in a beam telescope for the evaluation of its time resolution,

spatial resolution, and detection efficiency with minimum ionizing particles. The modified pixel processes achieved a remarkable time resolution of 63 ps with over 99% detection efficiency and a spatial resolution of 2 μm when tested at a substrate voltage V_{sub} of -4.8 V and 100 e^- threshold, without any observed process dependence.

The results demonstrate the potential of the 65 nm CMOS process over its 180 nm CMOS process predecessor, especially in terms of sensor development for high-precision time measurements. Monolithic active pixel sensors based on the 65 nm CMOS imaging technology are promising candidates not only for future high-energy physics vertex detectors but also for other applications demanding precise timing information in combination with full detection efficiency and high spatial resolution.

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5.5 Time resolution measurements with a ^{90}Sr electron source

To further investigate the timing properties of the APTS-OA prototypes, a setup aiming at the measurement of the time resolution of monolithic sensors with β electrons emitted by a ^{90}Sr radioactive source was built at Nikhef. A system made of a quartz crystal of 6 mm height and 3 mm diameter glued on top of a silicon photomultiplier (SiPM) acts as a time reference for the APTS-OA device under test (DUT). The Cherenkov photons generated by the interaction of the β electrons with the crystal are converted into an electrical signal by the SiPM, which is directly read out by one of the four channels of an oscilloscope. The remaining channels of the oscilloscope are connected to three of the four central pixels of the tested APTS-OA matrix. The signals of the other thirteen pixels of the matrix are acquired with the ADCs provided by the chip proximity board, similarly to the readout system of the test beam measurements (cf. Section 5.2.3). The radioactive source, the DUT and the time reference system are stacked and placed in a dark Faraday cage to minimize the effects of external electromagnetic interference and ambient light on the measurement. A detailed description of the test setup is provided by Reference [32].

The setup is developed to measure the time resolution of MAPS in conditions as close as possible to those achieved during beam tests with minimum ionizing particles. To do so, the feasibility of such a measurement is proven first. Afterward, the setup is used to accomplish the goal of collecting data sets with high statistical significance for the standard and modified CMOS process sensor variants, and expand the study presented in the publication included in this chapter.

To validate the setup, the results of the measurement of a modified with gap APTS-OA sample operated at $V_{\text{sub}} = -4.8 \text{ V}$ are compared with the beam test data taken by the same sensor type at the same operation conditions. The most straightforward observables to study the ionization produced by different particle species are the cluster signal charge and the pixel cluster multiplicity distributions. To find the condition for which the electrons from the radioactive source deposit an amount of energy in the APTS-OA pixels comparable to the one transferred by MIPs, the correlation between the signal amplitude of the SiPM and the most probable value of the cluster charge distribution is studied. In particular, it is found that by selecting events where the SiPM signals have amplitude larger than 40 mV, i.e. signals produced by electrons generating more than eight Cherenkov photons when interacting with the quartz crystal, it is possible to obtain a cluster charge distribution that almost matches the one produced by MIPs, as shown in the top panel of Figure 5.16. The bottom panel of Figure 5.16 shows the comparison of the cluster size distributions. The small difference observed between

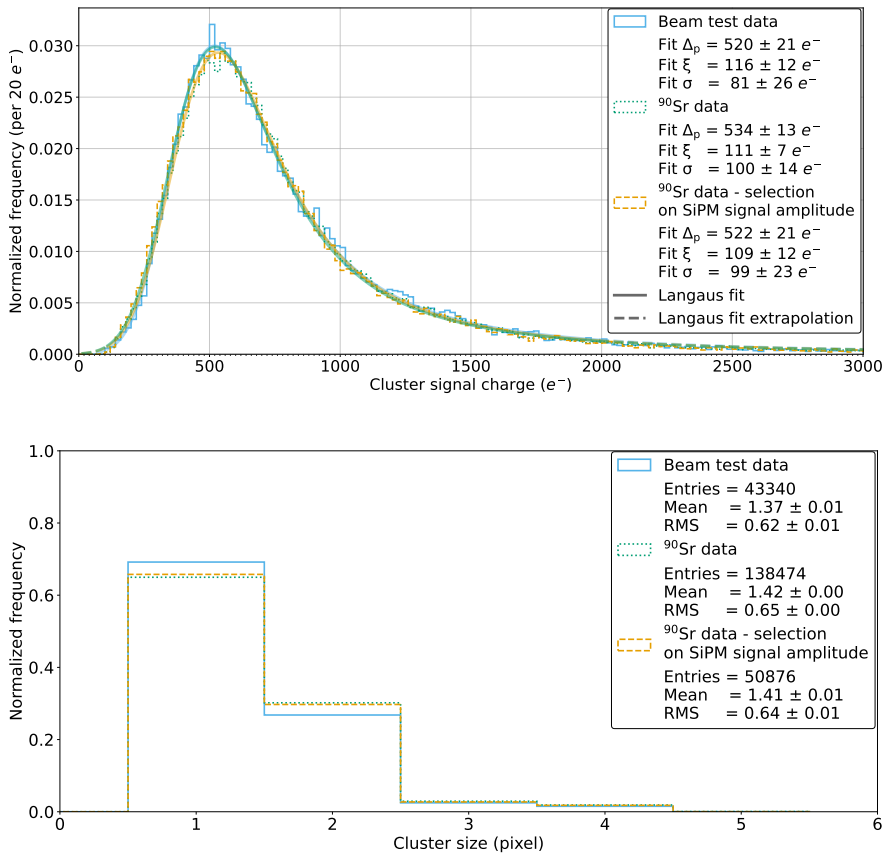


Figure 5.16 Comparison of measurements performed with a 120 GeV/c positive hadron beam and with β electrons from a ^{90}Sr source by a modified with gap APTS-OA prototype operated at $V_{\text{sub}} = -4.8$ V. The blue solid histograms represent the beam test data, the green dotted histograms the data taken with the β setup and the orange dashed histograms the latter data with a selection on the events for which the SiPM signals have a voltage amplitude above 40 mV. Top: Cluster signal charge distributions. The distributions are fitted with a Languas function (cf. Section 2.5.1). Bottom: Cluster size distributions.

beam test and ^{90}Sr cluster size distributions, even after the data selection procedure explained above, is likely due to the different particles interacting with the sensor, with the electrons more subject to scattering in silicon. An exhaustive discussion on the comparison of the two measurements and on the data selection condition applied to data taken with the setup built at Nikhef can be found in Reference [32]. In the following, the timing studies of three APTS-OA matrices implementing the different

pixel sensor variants carried out with the setup introduced above are presented. The results obtained refer only to events causing ionization in the APTS-OA matrix with a simultaneous SiPM signal above 40 mV.

Figure 5.17 shows the time residual distributions measured for the three process variants operated at $V_{\text{sub}} = -4.8 \text{ V}$. The time residuals are defined, similarly to the beam test data analysis, as the difference between the time when the APTS-OA DUT seed pixel signal reaches 10% of its full amplitude and the time provided by the time reference system. The latter is measured at 30% of the SiPM signal amplitude. With such a measurement method, the time reference system has a resolution of the order of 40 ps [32]. The same analysis method adopted for the beam test data, which aims at the compensation of the dependence of the time residuals on the seed signal charge and the in-pixel ionization position, accessed via the cluster size information, is used. As already observed with a minimum ionizing particle beam, no difference in timing performance is found between the modified and the modified with gap sensors, with a time resolution in line with what is measured at the beam test. The sensor implementing a standard process shows instead, as expected, a worse time performance due to the charge collection dominated by diffusion in the non-depleted regions of the epitaxial layer. This is demonstrated by the long tail towards high time residuals characterizing the non-corrected distribution. Even after applying the same correction of the other two sensor variants, the width of the time residuals of the standard sample is noticeably larger than the modified counterparts.

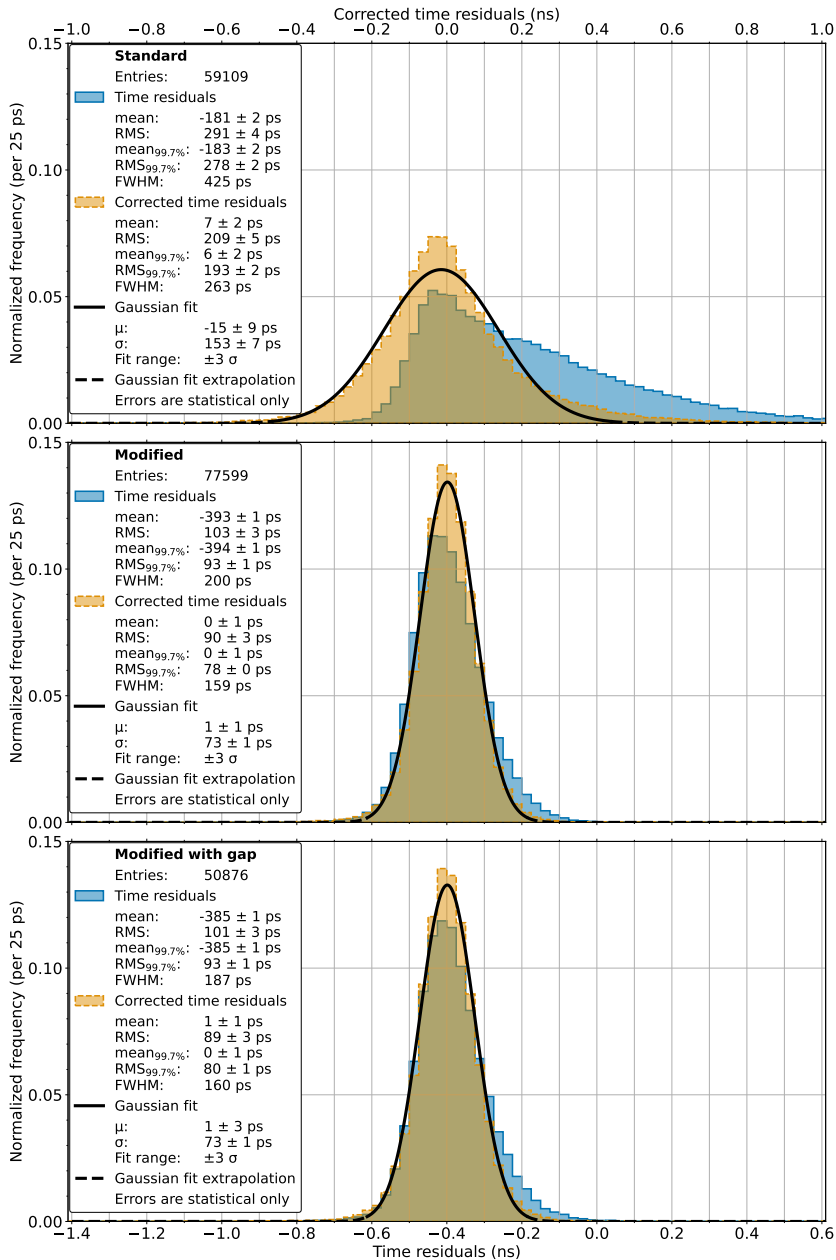


Figure 5.17 Time residuals measured with the electrons emitted by a ^{90}Sr source for the three APTS-OA process variants operated at $V_{\text{sub}} = -4.8$ V, before (blue distribution, bottom horizontal axis) and after (orange distribution, top horizontal axis) time walk-like correction. The latter distribution is fitted with a Gaussian function on a range of $\pm 3\sigma$ (black solid line, dashed line for points outside the fit range).

5.6 Summary and discussion

The paper included in the present chapter provides a deeper knowledge on the properties of the APTS-OA prototype variants based on a modified and a modified with gap CMOS processes. The response of two samples to a minimum ionizing particle beam has been measured with an ALPIDE-based beam telescope including an LGAD plane acting as a timing reference.

Both sensors, operated at varying reverse substrate voltage of -1.2 , -2.4 , -3.6 and -4.8 V, show a detection efficiency above 99% and a spatial resolution of the order of $2\text{ }\mu\text{m}$, or slightly better depending on the applied bias voltage³, when a threshold corresponding to $100\text{ }e^-$ is applied during the analysis.

Regarding the timing properties of the sensors, an increasing reverse bias voltage positively impacts the time resolution, while there is no notable difference between the two different sensor designs for the $10\text{ }\mu\text{m}$ pixel pitch available⁴. The best result is provided by the modified with gap sensor operated with $V_{\text{sub}} = -4.8\text{ V}$, for which a time resolution of $82\text{ ps} \pm 3\text{ ps}$ is achieved when the time of the acquired signals is measured at 10% of the full amplitude, and a software threshold of $100\text{ }e^-$ is applied. Such a result can be further improved to $63\text{ ps} \pm 3\text{ ps}$ if the dependence of the time residuals on the signal charge and in-pixel track hit position is compensated for with the analysis method shown in the paper⁵.

The measurements performed at Nikhef with the setup based on a ^{90}Sr radioactive source presented in the last section of the chapter are in line with what is discussed in the paper, and confirm the improved performance brought by the CMOS process modification with respect to the standard process in terms of time resolution.

The obtained results can be further commented by recalling the factors contributing to the time resolution σ_t of a silicon pixel sensor (cf. Section 2.8), reported here below for clarity:

$$\sigma_t^2 = \sigma_{\text{jitter}}^2 + (\sigma_{\text{total ionization}} + \sigma_{\text{Landau noise}})^2 + \sigma_{\text{distortion}}^2 + \sigma_{\text{TDC}}^2 . \quad (5.4)$$

In the case of the APTS-OA, the term σ_{TDC} is absent as the test structure has an analog

³ The measured spatial resolution, significantly better than what a purely binary sensor with same pixel pitch would achieve, benefits from the analog readout of the test structure. The latter allows a precise signal charge evaluation, which translates in a precise assessment of the cluster center of gravity via charge weighting.

⁴ A more evident difference between the two processes is expected for larger pixel pitches.

⁵ The figures resulting from the analysis of the data pertaining to the modified with gap device operated at -1.2 and -2.4 V reverse bias voltage, for which high statistical significance data sets are available, are reported in Appendix I.

readout, while σ_{jitter} is of the order of 10 ps or lower⁶, depending on the signal charge (cf. Section 4.9.2), hence negligible with respect to the measured σ_t . Furthermore, no contribution to the time resolution due to pixel-to-pixel fluctuations is expected, as the measured pixels are individually calibrated. Thus, only the components strictly related to the sensor contribution to the time resolution remain. The factor $\sigma_{\text{total ionization}}$ is compensated by adopting the analysis method based on the software measurement of the time at fixed amplitude fraction to mitigate time walk effects. The element $\sigma_{\text{distortion}}$ is instead corrected by taking into account the dependence of the measured time residuals on the signal charge and the in-pixel position of the ionization. Such a procedure improves the time resolution from 82 ps to 63 ps. However, as shown in Figure 5.15, the latter correction only partially balances the effect of non-uniform electric and weighting fields, as the time resolution still varies within the pixel. Therefore, the final result of $63 \text{ ps} \pm 3 \text{ ps}$ includes the contribution of $\sigma_{\text{Landau noise}}$, namely the ultimate limit to the resolution of the sensor, and the residual effects of $\sigma_{\text{distortion}}$ and of the correlation of $\sigma_{\text{total ionization}}$ with $\sigma_{\text{Landau noise}}$.

As intended, the APTS-OA proves to be an excellent tool to evaluate the actual properties and limits of monolithic active pixel sensors implementing the TPSCo 65 nm CMOS technology. The adoption of a smaller technology node with respect to the previous generation of devices based on the 180 nm line, combined with a CMOS process modification aiming at fully depleting the sensitive volume, makes such sensors promising candidates for applications where high-precision time measurements, besides precise tracking, are required. Nonetheless, it is worth to repeat that the reported timing results describe the performance of the sensor only. For a fully integrated device (i.e. including front-end circuitry with discriminator and TDC) with a large pixel matrix, other factors, such as a non-negligible front-end jitter, limitation on the evaluation of the signal charge, contribution of the TDC, and pixel-to-pixel fluctuations, would contribute to the time resolution of the system.

The studies exposed in this and in the previous chapter provide a complete overview on the properties of non-irradiated APTS-OA sensors. The effect of non-ionizing damage is currently under investigation with a new measurement campaign of devices irradiated up to $1 \times 10^{16} \text{ 1 MeV } n_{\text{eq}} \text{ cm}^{-2}$.

⁶ This number includes the contributions of the finite time binning and noise introduced by the readout system, i.e. the oscilloscope, to the measurement.

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CHAPTER 6

Simulations of 65 nm CMOS sensors

THE APTS-OA prototype studies presented in the previous chapters provide a comprehensive overview on the properties of monolithic sensors implemented in TPSCo 65 nm CMOS imaging process. At the same time, some physical properties of the sensors, such as the electric or weighting field distributions, or details of their response, such as the contribution of the substrate to the amount of collected charge, are not immediately accessible through experimental investigation. To obtain a more complete understanding of the device physics, the behavior of MAPS based on the TPSCo 65 nm CMOS imaging process was simulated. The simulation is based on the combination of three-dimensional Synopsys Technology Aided Design (TCAD) models [1] and Monte Carlo simulations performed with the Allpix² framework [2]. The former describe and evaluate the electrical properties of the sensor while the latter reconstruct the process behind the formation of the voltage signal read out at the output channel of a pixel, from the interaction of radiation with the detector to the current induction at the pixel's electrode.

The idea of the research presented in this chapter is to study the 65 nm CMOS technology through the modeling of the APTS-OA sensor, with direct comparison with the experimental data acquired for such a device to validate the simulation pipeline. A precise model of the APTS-OA sensor would require, however, the knowledge of the details of the TPSCo 65 nm CMOS process. Since this specific process is commercial and covered by non-disclosure agreements with the foundry, some details, such as the doping profiles, are not accessible. The simulation is therefore developed on the basis of the known features of the sensor layouts, combined with approximated doping profiles. The doping profiles implemented in the simulation are iteratively adjusted after the comparison with the experimental results in view of a more realistic description of the sensor behavior. The goal of the study discussed in this chapter is not to reverse engineer the TPSCo 65 nm CMOS process, but to qualitatively describe

its main characteristics in order to obtain a more comprehensive understanding of the physics of monolithic devices based on the 65 nm CMOS technology.

6.1 Simulation concepts

The investigation on the physics of monolithic sensors based on the TPSCo 65 nm CMOS imaging process is conducted via the simulation of the APTS-OA prototypes. In particular, the modified with gap process is chosen as simulation target. It is, in fact, the most promising one among the various sensor layouts in terms of performance and future developments, and experimental data sets of high statistical significance pertaining to such a structure measured with a minimum ionizing particle beam are available. As the comparison with experimental data is a crucial step in the validation of the simulation chain, the simulated sensor has to generate analog voltage signals to be processed with the same analysis developed for the experimental signals presented in Chapter 4 and Chapter 5.

The simulation workflow is based on the combination of three-dimensional Synopsys TCAD models with Monte Carlo simulations performed with Allpix². TCAD allows the modeling of semiconductor devices by means of finite element analysis. They represent a powerful tool for the calculation of the sensor's electrostatic (cf. Section 2.2) and weighting (cf. Section 2.6) fields, which are highly non-linear for the high-resistivity monolithic devices with small collection electrode under investigation. The three-dimensional field maps produced in such a way are then taken as an input by the Allpix² framework, which simulates the energy deposition resulting from the interaction of the sensor with incoming radiation, accounting for the stochastic nature of the phenomenon, the subsequent charge formation and transport within the semiconductor volume and the signal induction at the collection electrode due to the moving charges. Although many of the aspects related to the physics of charge transport and signal induction can be investigated with TCAD transient simulations as well, the high computation time needed already by a single event only would make such an approach unpractical. Allpix² runs instead with simulation rates of tens of Hertz, allowing the generation of data sets with high statistical significance, which are essential for a detailed study of the behavior of a sensor interacting with minimum ionizing particles, for which Landau fluctuations play a predominant role (cf. Section 2.5.1).

Examples of studies utilizing the combination of the TCAD and Allpix² tools for the modeling of MAPS are provided by Reference [3] and Reference [4].

6.2 TCAD model

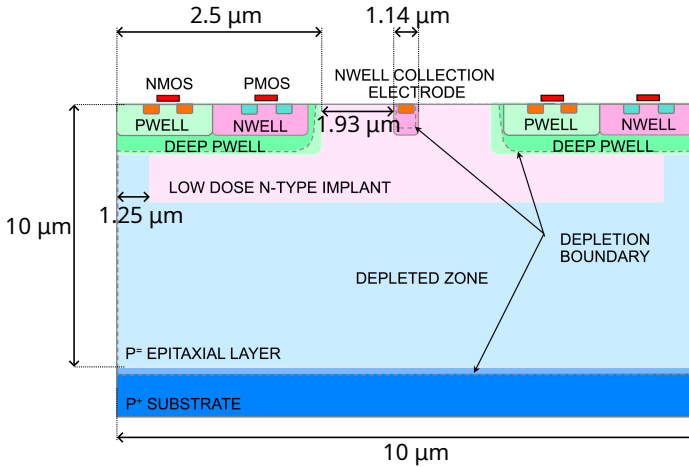


Figure 6.1 Schematic cross section of a pixel cell implementing the TPSCo 65 nm CMOS modified with gap imaging process. The characteristic dimensions of the pixel of an APTS-OA prototype are indicated. Not to scale. Figure adapted from Reference [5].

Three-dimensional TCAD simulations using the Synopsys Sentaurus framework are used to compute the electrostatic properties of an APTS-OA sensor implementing a TPSCo 65 nm CMOS imaging modified with gap process. To reduce the calculation complexity, the simulation of a single pixel cell is sufficient, as the Allpix² framework allows to apply periodic boundary conditions to generate a pixel matrix. Figure 6.1 shows the cross section of the 10 μm pitch pixel cell simulated with TCAD. It is based on a 10 μm thick high-purity p-type (p^-) epitaxial layer grown on top of a p^+ substrate. The collection electrode is an octagonal shaped n-well of 1.14 μm . For simplicity, in the simulation the electrode is approximated with a square of 1.14 μm edge. The deep p-well hosting the in-pixel circuitry is 5 μm wide and centered along the pixel edges. In the simulation, the latter is simplistically treated as a highly doped p-type well, with no circuitry included in the model. It is distanced 1.93 μm from the collection electrode. The low dose n-type implant underneath the collection electrode has a cut of 2.5 μm centered along the pixel edges. The doping concentrations of the epitaxial layer, the wells and the implant are not known as they are covered by a non-disclosure agreement. They are approximated as uniformly doped structures with a Gaussian profile at the interface with other structures to avoid abrupt nonphysical changes in doping concentration. The substrate is treated as a highly doped p-type silicon of

15 μm thickness¹. The p-type regions are assumed to be doped with boron atoms, the n-type ones with phosphorus.

The model is provided with biasing contacts to the collection electrode, the p-well, and the substrate. To emulate the working conditions of the APTS-OA sensor providing the best results in terms of timing performance (cf. Section 4.6.2), the collection electrode has a positive bias voltage of 0.4 V (reproducing the effect of the V_{reset} voltage in the real device), while the p-well and substrate are biased with -4.8 V.

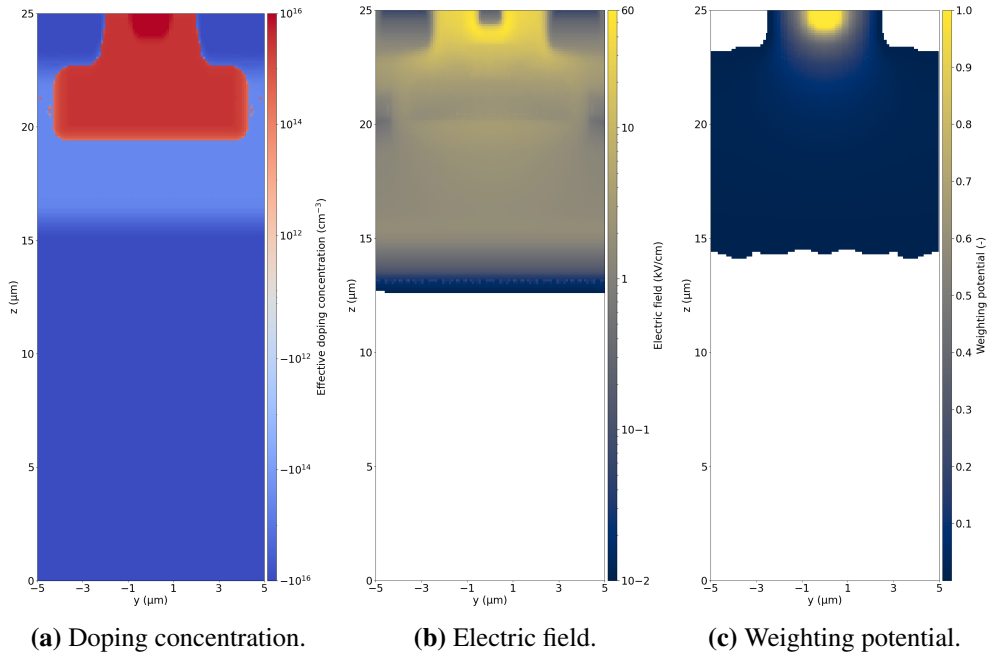


Figure 6.2 Example of cross sections (cut performed at the pixel center, i.e. $x = 0.0 \mu\text{m}$) of the electrostatic properties of an APTS-OA pixel in TCAD: a) Effective doping concentration. A divergent color map is used to distinguish structures with opposite doping polarities. Shades of blue indicate p-doped silicon (here illustrated with a negative doping concentration), shades of red n-doped silicon (here illustrated with positive doping concentration). b) Electric field. The white color is used to identify regions with electric field intensity lower than $1 \times 10^{-2} \text{ kV/cm}$. c) Weighting potential. The white color is used to identify regions with zero weighting potential.

The TCAD model consists of a mesh reproducing the geometrical features

¹ It is reasonable to assume a substrate thickness between 10 μm and a few tens of μm . As is shown later in the chapter, only the region at the interface with the epitaxial layer has an effect on the charge collection process.

described above, where each node carries the information related to the dopant type and concentration. TCAD calculates the electrostatic field in each point by solving the Poisson equation (cf. Section 2.2). The solution depends on the doping concentrations applied in the mesh, as well as on the biasing condition, since both influence the charge distribution in the sensor's volume. Finally, TCAD allows the computation of the weighting potential according to the definition given in Section 2.6. By producing two electrostatic potential maps at slightly different bias voltage applied to the electrode of interest, the weighting potential map can be calculated from the difference of these two in each node normalized to the difference in bias voltage. Examples of a generic doping profile mesh produced to simulate the APTS-OA sensor, and the corresponding electric field and weighting potential maps are provided in Figure 6.2.

It is worth to repeat that the electric field depends on the implemented doping profile, while the weighting potential depends only on the geometrical properties of the pixel. As explained in Section 2.6, the weighting field allows the evaluation of the current signal induced by moving charges. Pixel designs based on small collection electrodes are characterized by a non-uniform weighting potential within their sensitive volume, with high potential found in the proximity of the collection electrode only. In other words, only the charge carriers drifting nearby the electrode contribute to the output signal.

6.3 Allpix² pipeline

Allpix² is a modular framework that allows to run a full simulation pipeline, from the interaction of the detector with incoming radiation to the signal formation. As such, a 4×4 pixel matrix illuminated with a $120 \text{ GeV}/c \pi^+$ beam is simulated to reproduce the beam test conditions discussed in Chapter 5. The simulation presented hereafter focuses on the study of the behavior of a modified with gap APTS-OA prototype traversed by minimum ionizing particles, and does not include the telescope tracking planes and the timing plane.

In the following subsections, the physics models implemented in the modules relevant for the simulation discussed in this chapter are outlined. A more detailed description of the modules is provided by Reference [6].

6.3.1 Particle-detector interaction

The module *DepositionGeant4* provides an interface to Geant4 [7–9] for advanced Monte Carlo simulations of the passage of particles through matter.

The simulation consists in a 120 GeV/ c positive pion beam pointing towards the positive z direction, perpendicular to the xy detector surface, evenly illuminating the pixel matrix. The deposited energy is converted in electron-hole pairs according to the silicon conversion factor of 3.6 eV per e^-h^+ pair. For an accurate description of the energy deposition process in very thin silicon layers, the Photo Absorption Ionization model [10] is adopted.

The framework also stores Monte Carlo (MC) truth quantities, such as the impact time or energy deposited by each single track or information on secondary particles (i.e. delta rays), which are relevant for the analysis discussed in Section 6.4.

6.3.2 Sensor electrostatic properties

The TCAD doping profile, electric field and weighting potential maps presented in the previous section can be used as an input for the Monte Carlo simulation to properly account for the electrical properties of the simulated sensor. The Allpix² framework provides a tool to convert the TCAD meshes into regularly spaced grids compatible with the Monte Carlo simulations. Such grids are loaded through the modules *DopingProfileReader*, *ElectricFieldReader*, and *WeightingPotentialReader* and are required for a precise simulation of the charge transport and signal formation steps.

The doping profile is used to properly compute the lifetime of the charge carriers (cf. Section 2.3), the electric field is needed for the calculation of the transport properties (for example the drift velocity, cf. Section 2.4) and the weighting potential is needed for the evaluation of the induced signal current (cf. Section 2.6).

6.3.3 Charge carrier transport

The *TransientPropagation* module propagates the charge carriers after the energy deposition and charge generation steps. The propagation consists of a combination of drift and diffusion simulations (cf. Section 2.4). In the nodes of the grid where the electric field is non-zero, charge carriers are propagated along the lines of the electric field provided by the *ElectricFieldReader* module. Such a movement is evaluated by solving the drift transport equation (cf. Equation 2.18) with a fourth-order Runge-Kutta method, by using a time step of 5 ps. This number is selected as a trade-off between satisfying simulation precision and reasonable computation time. The carrier mobility model chosen in the simulation extends the commonly used Jacoboni-Canali model [11], with a further improvement of the mobility description in regions with low field or high doping concentration [12]. After every ‘drift step’,

diffusion is accounted for by applying an offset to the charge carrier position sampled from a Gaussian distribution with standard deviation described by the Einstein relation (cf. Equation 2.19), where a temperature of 300 K is assumed for the calculation. In zero field regions, only the diffusion component plays a role in the transport of the carriers.

The simulated carrier lifetime τ depends on the doping concentration profile of the sensor provided by the *DopingProfileReader* module. It is computed by considering the combination of the lifetime τ_{SRH} given by the Shockley-Read-Hall (SRH) recombination model and τ_{Auger} given by the Auger model (cf. Section 2.3), according to:

$$\tau = \frac{1}{\frac{1}{\tau_{SRH}} + \frac{1}{\tau_{Auger}}}. \quad (6.1)$$

The SRH lifetime depends on the reference lifetime τ^{ref} [13] and reference effective doping concentration $N_{\text{eff}}^{\text{ref}}$ [14] coefficients, equal to 1×10^{-5} s and 1×10^{16} cm⁻³ for electrons and 4×10^{-4} s and 7.1×10^{15} cm⁻³ for holes, respectively, and on a temperature scaling factor $[300/T(\text{K})]^{1.5}$ [15], which is equal to 1 for the simulations illustrated in this chapter:

$$\tau_{SRH} = \frac{\tau^{\text{ref}}}{1 + \frac{N_{\text{eff}}}{N_{\text{eff}}^{\text{ref}}}}, \quad (6.2)$$

where N_{eff} is the effective doping concentration of the silicon structure where the considered charge carrier propagates. The Auger lifetime is instead:

$$\tau_{Auger} = \frac{1}{k_{Auger} \times N_{\text{eff}}^2}, \quad (6.3)$$

where $k_{Auger} = 3.8 \times 10^{-31}$ cm⁶ s⁻¹ [16]. The Auger recombination mechanism is particularly relevant in heavily doped silicon, as demonstrated by the quadratic dependence of the lifetime on the effective doping concentration. The trapping process is instead neglected as a non-irradiated sensor is simulated.

The charge carriers propagate for a number of steps summing up to a maximum of 50 ns. A propagation is halted if the carrier reaches the borders of the 4×4 pixel matrix or the collection electrode of one of the pixels, or if it recombines. For each time step, the charge induced on the collection electrodes by the moving carriers is calculated via the Shockley-Ramo theorem (cf. Section 2.6) by using the weighting potential provided by the *WeightingPotentialReader* module.

6.3.4 Signal formation

The *PulseTransfer* module computes the pixels' current pulses $i(t)$ by summing the charge induced at each collection electrode.

Then, the *CSADigitizerModule* module calculates the output voltage signals $v(t)$ as the convolution of the current pulses with the impulse response function, or transfer function, $T(t)$ of the pixel front-end circuit, under the assumption that it implements a Charge Sensitive Amplifier (CSA) configuration [17]. The voltage signal is therefore:

$$v(t) = (i \otimes T)(t) = \int i(t')T(t - t')dt' . \quad (6.4)$$

The transfer function of a simple CSA stage can be written as:

$$T(t) = \frac{\tau_f}{C_f} \left(\frac{e^{-t/\tau_f} - e^{-t/\tau_r}}{\tau_f - \tau_r} \right), \quad (6.5)$$

where C_f is the feedback capacitance, τ_r the rise time constant, and τ_f the feedback time constant of a Charge Sensitive Amplifier circuit. More details on the calculation of $T(t)$ can be found in Reference [18].

As seen in Section 4.2, the APTS-OA circuitry does not implement a charge amplifier stage. However, the parameters of Equation 6.5 can be tuned to reasonably mimic the behavior of the APTS-OA front-end operated with a $V_{\text{sub}} = -4.8$ V. The feedback capacitance can be thought as a charge to voltage conversion capacitance, which for the APTS-OA pixels corresponds to the sum of the input and injection capacitance divided by the non-unitary gain of the front-end (cf. Equation 4.8 of Section 4.8). Given this consideration, a value of $C_f = 3$ fF is used for the simulation². The factor τ_r , describing the signal leading edge time constant, is set to 180 ps, while τ_f , describing the signal trailing edge time constant, is set to 2.5 μ s. Both values are extracted from test pulses measurements of the APTS-OA prototypes. Finally, a Gaussian-distributed noise with standard deviation of 0.8 mV, corresponding to the voltage noise RMS measured for the APTS-OA (cf. Figure 4.10), is added to the simulated voltage signal. The latter constitutes the final outcome of the simulation workflow.

²This number results from the combination of the measured input capacitance of a sensor based on a modified with gap process operated with $V_{\text{sub}} = -4.8$ V equal to about 2 fF (cf. Figure 4.20), the measured injection capacitance of 0.2 fF (cf. Figure 4.19), and the measured front-end gain of about 0.65 (cf. Figure 4.8).

6.4 Analysis methods

With respect to the experimental scenario, where the signals of the outermost 12 pixels of the matrix are acquired with ADCs of 4 MSa/s sampling rate and the central four pixels are read out by an oscilloscope with higher sampling rate (cf. Section 4.3), all the pixels of simulated matrix produce voltage signals having a period of 25 ps between the sampled points. All the simulated signals are therefore processed with the same analysis methods developed for the signals read out with the oscilloscope, as discussed in Section 4.5 and Section 5.3.2.

The results presented in the following sections refer to MC events having the seed in one of the central four pixels of the simulated matrix, while the signals from the outer ones are used to reconstruct the information on pixel cluster multiplicity and cluster signal charge. As done for the experimental data, a threshold corresponding to $100 e^-$ is applied to identify pixels belonging to a cluster.

Regarding the time resolution studies, the time residual distribution is computed as the difference between the simulated signal time measured at 10% of its full amplitude and the time reference, given by the MC truth interaction time of the simulated particle with the detector.

6.5 Simulation validation

The workflow presented in Section 6.3 makes possible to study the response to minimum ionizing particles of the CMOS sensor modeled in TCAD with high statistical significance, in order to properly account for the fluctuations in energy deposition due to the stochastic nature of particle-detector interaction.

The simulation validation is performed by comparing the outcome of the simulated data analysis with the beam test campaign results presented in the previous two chapters. In particular, the pixel cluster charge and the pixel cluster size distributions are the observables chosen for the comparison, as they describe the charge collection properties of the studied sensor technology. Such an investigation allows to explore the impact of some physical parameters, such as the thickness and doping concentration of the substrate, on the sensor performance.

6.5.1 Substrate contribution to the charge collection

The top panel of Figure 6.3 shows the comparison of the cluster charge distribution of a modified with gap device biased with a substrate voltage of -4.8 V (cf. Section 4.10), depicted with black points, with the simulated counterpart. The solid histograms

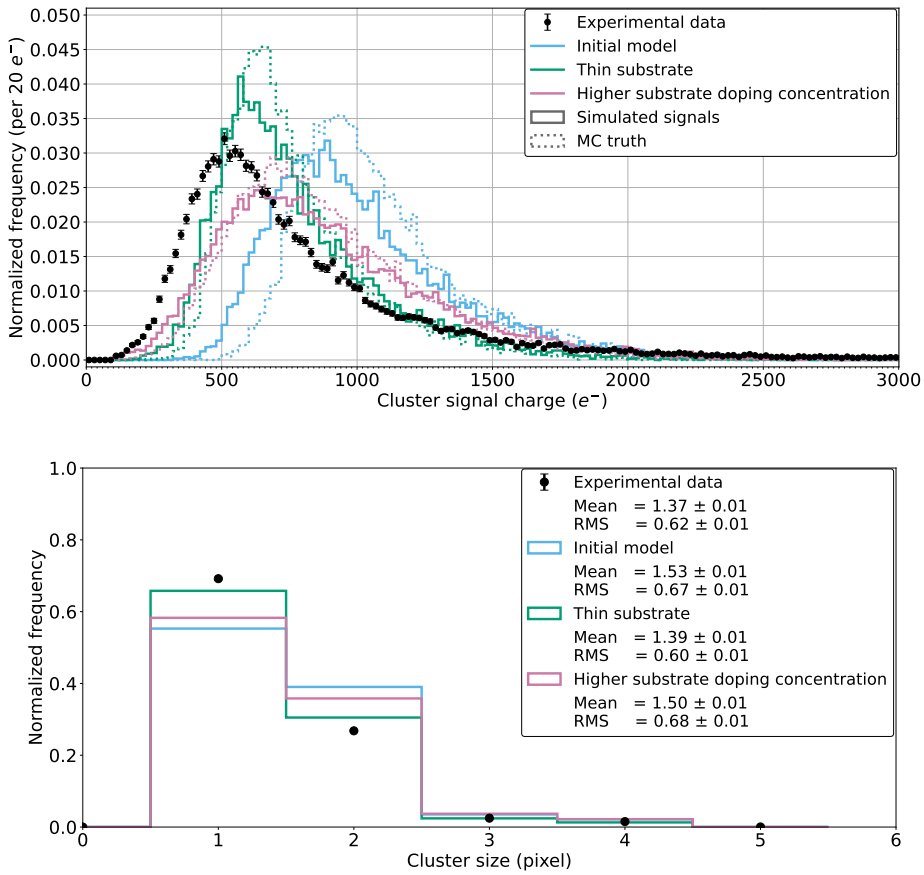


Figure 6.3 Comparison of the experimental (in black) and simulated cluster charge (top panel) and cluster size (bottom panel) distributions for an APTS-OA matrix operated at $V_{\text{sub}} = -4.8 \text{ V}$ and traversed by a minimum ionizing particle beam. Different pixel sensor models are tested against the experimental results: $15 \mu\text{m}$ thick substrate of $N_a = 1 \times 10^{18} \text{ cm}^{-3}$ doping concentration (in blue), $1 \mu\text{m}$ thick substrate of $N_a = 1 \times 10^{18} \text{ cm}^{-3}$ doping concentration (in green), and $15 \mu\text{m}$ thick substrate of $N_a = 1 \times 10^{19} \text{ cm}^{-3}$ doping concentration (in magenta). For the cluster signal, both the distributions resulting from the selection of the simulated signals (solid lines) and from the MC truth information (dashed lines) are depicted.

represent the charge extracted from the simulated signals with the same analysis procedure applied to the experimental signals. For completeness, the MC truth value of the collected charge is illustrated with dashed histograms. The difference among the two quantities is due to the clusterization threshold of $100 e^-$ applied to the simulated

signals, which excludes pixels collecting less charge than the threshold value from the cluster. The bottom panel shows the comparison of the distributions of the pixel cluster size. In particular, the blue histograms are the results obtained by running the whole simulation pipeline with the TCAD model discussed in Section 6.2 as input. The latter implements the pixel cell as a $10\text{ }\mu\text{m}$ thick epitaxial layer on top of a $15\text{ }\mu\text{m}$ thick substrate doped with an acceptor atom concentration of $1 \times 10^{18}\text{ cm}^{-3}$. For such a model, both the simulated cluster charge and cluster size distributions show evident disagreement with the experimental ones, with a clear excess of collected charge and frequency of two-pixel clusters. These observations are evidence of a disproportion in charge sharing between the simulated sensor and the actual one. Further investigations were therefore conducted to identify the causes of the observed mismatch in the charge collection behavior.

The impact of the substrate on the charge collection process is studied by varying its physical parameters in the TCAD model. The green distributions of Figure 6.3 display the charge collection properties of the same sensor discussed above, but with a $1\text{ }\mu\text{m}$ thick substrate. A thinner substrate corresponds to a lower amount of charge generated in the same region, with subsequent reduced number of carriers able to diffuse until the proximity of the epitaxial layer, where they can contribute to the collected charge since they can drift to the pixel's collection electrode because of the non-zero electric field. Nonetheless, an excess of collected charge is still observed. Moreover, such a thin substrate is unfeasible, since a layer of the order of at least $10\text{ }\mu\text{m}$ is needed to provide a contact for the reverse bias operation of the sensor. Such a model is anyway useful to visualize the impact of the substrate thickness.

Finally, a third model implementing a $15\text{ }\mu\text{m}$ thick substrate doped with an acceptor atom concentrations of $1 \times 10^{19}\text{ cm}^{-3}$ is tested. This modification implies, according to Equation 6.1, a reduction of the electrons' lifetime in the substrate from about 100 ns to about 7 ns , with a subsequent diminished substrate contribution to the overall charge collection. A lower lifetime implies a lower probability for an electron generated in the substrate to diffuse up to the epitaxial layer and eventually be collected. The diffusion suppression is reflected in the related cluster charge distribution, which shows a peak closer to the experimental one if compared with the less doped substrate model. A similar effect is present in the pixel multiplicity distribution, where an increase in single pixel clusters frequency is seen. However, this last adjustment is not sufficient yet to satisfactorily describe the real device, since an excess of collected charge and a mismatch in the cluster size distribution is still observed.

6.5.2 Towards a more realistic sensor model

Despite the improvement brought by the increase in the substrate doping concentration, further refinements of the sensor model are required to correct for the excess of collected charge. As discussed in Reference [19], a sensor is subjected to high temperatures during the CMOS manufacturing process. In particular, the procedures of chemical vapor deposition and annealing expose the sensor to temperatures above 1000 °C. High temperature is expected to favor dopant diffusion from the substrate to the epitaxial layer. The effect of such a phenomenon is reproduced in the TCAD model shown in Figure 6.4. In particular, the doping concentration mesh depicted in

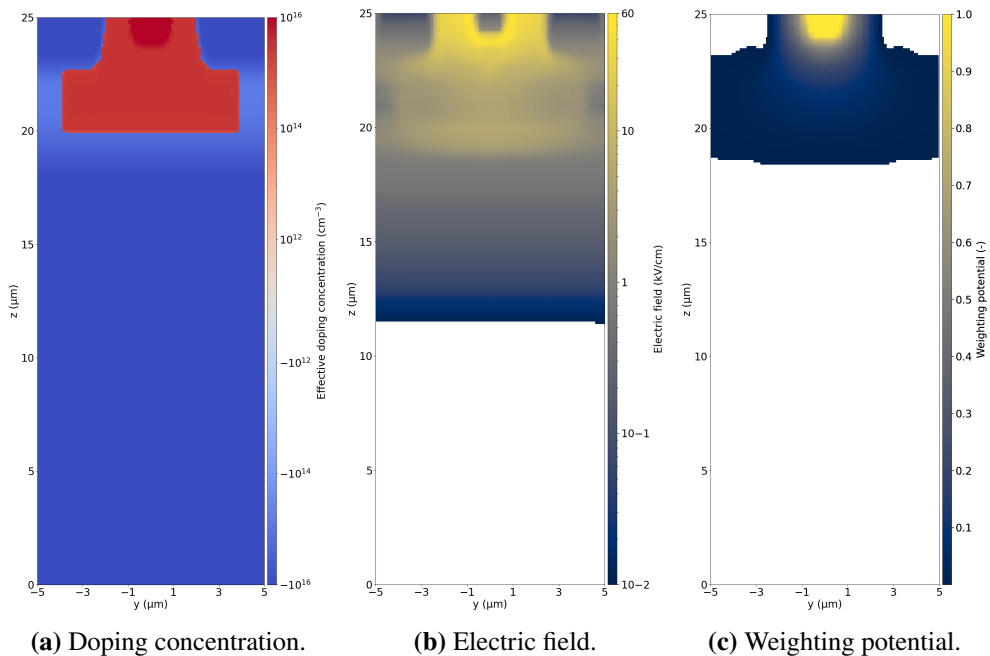


Figure 6.4 Cross sections (cut performed at the pixel center, i.e. $x = 0.0 \mu\text{m}$) of the electrostatic properties of the TCAD APTS-OA pixel model emulating the effect of dopant diffusion from the substrate to the epitaxial layer: a) Effective doping concentration. A divergent color map is used to distinguish structures with opposite doping polarities. Shades of blue indicate p-doped silicon (here illustrated with a negative doping concentration), shades of red n-doped silicon (here illustrated with positive doping concentration). b) Electric field. The white color is used to identify regions with electric field intensity lower than $1 \times 10^{-2} \text{ kV/cm}$. c) Weighting potential. The white color is used to identify regions with zero weighting potential. The net effect of the dopant diffusion is an epitaxial layer thinner than $10 \mu\text{m}$.

the left panel implements a more consistent diffusion layer at the interface between the substrate and epitaxial layer (represented in Figure 6.4 as the region where the dark shade of blue turns into light blue) than what is displayed in the corresponding map of Figure 6.2. In other words, the net effect of the dopant diffusion corresponds to the reduction of the epitaxial layer thickness, namely the active sensing volume. Such an effect can also be visualized from the comparison of the electric field of the ‘highly diffused interface’ model of Figure 6.4 with the initial model of Figure 6.2, both simulating a reverse bias of -4.8 V .

The electrostatic properties of the new sensor model are passed as an input for a Monte Carlo simulation. The comparison of the experimental and simulated charge collection observables is represented in Figure 6.5. Very good agreement between data sets is shown both by cluster charge and cluster size distributions. An effectively thinner epitaxial layer yields a reduced amount of collected charge, with the most probable value of the cluster charge aligning with the experimental one. The MC truth distribution is instead shifted towards higher cluster charge values since it also accounts for the contribution of pixels collecting less than 100 e^- . A good agreement is observed also for the cluster size distribution.

For further validation, the correlation between the in-pixel track hit position and the pixel multiplicity of the associated cluster can be studied. Figure 6.6 provides a picture of both the in-pixel cluster size map and the cluster size variation along the path from the pixel center to the edge, and to the corner. The top row shows the experimental data, for which a tracking resolution of $1.8\text{ }\mu\text{m}$, namely an uncertainty on the reconstructed track intercept, is estimated. The central row illustrates the simulated data, where each cluster is associated to the track hit position given by the corresponding MC truth variable. The last row shows the same dataset, now taking into account the same experimental limited tracking resolution. Such an effect is emulated by shifting the simulated track hit coordinate by an offset sampled from a Gaussian distribution with $1.8\text{ }\mu\text{m}$ standard deviation in both x and y directions. A good agreement between experimental and simulated data is found if the limitation of the experimental setup are accounted for in the comparison. This kind of study allows to disentangle the performance of the studied device from the effects arising from the limited tracking resolution introduced by the experimental setup. The correlation between the simulated MC truth track intercepts and the size of the associated clusters depicted in the center of Figure 6.6 confirms the enhancement in charge collection introduced by the process modification. According to the chosen in-pixel binning of $2\text{ }\mu\text{m} \times 2\text{ }\mu\text{m}$, the charge generated by tracks hitting the central $6\text{ }\mu\text{m} \times 6\text{ }\mu\text{m}$ surface of a pixel is expected to be fully collected by the pixel itself.

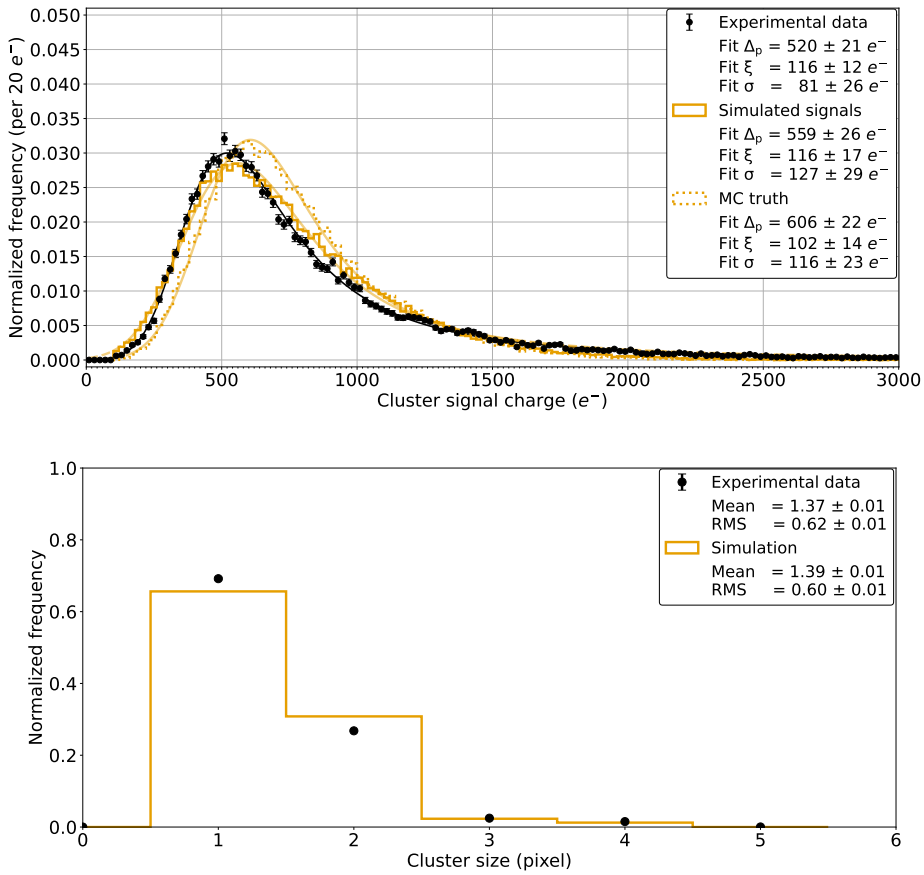


Figure 6.5 Comparison of the experimental (in black) and simulated (in orange) cluster charge (top panel) and cluster size (bottom panel) distributions of an APTS-OA matrix operated at $V_{\text{sub}} = -4.8$ V and traversed by a minimum ionizing particle beam. The simulated sensor model implements a $15\text{ }\mu\text{m}$ thick substrate of $N_a = 1 \times 10^{19}\text{ cm}^{-3}$ doping concentration with a relevant diffusion region at the interface with the epitaxial layer emulating the diffusion of acceptor atoms during the high temperature procedures typical of the CMOS manufacturing process. For the cluster signal, both the distributions resulting from the analysis of the simulated signals (solid line) and from the MC truth information (dashed line) are depicted. All the three distributions are fitted with a Langaus function. The refinement in the substrate description reasonably approximates the experimental charge collection observables, improving the models presented in Figure 6.3.

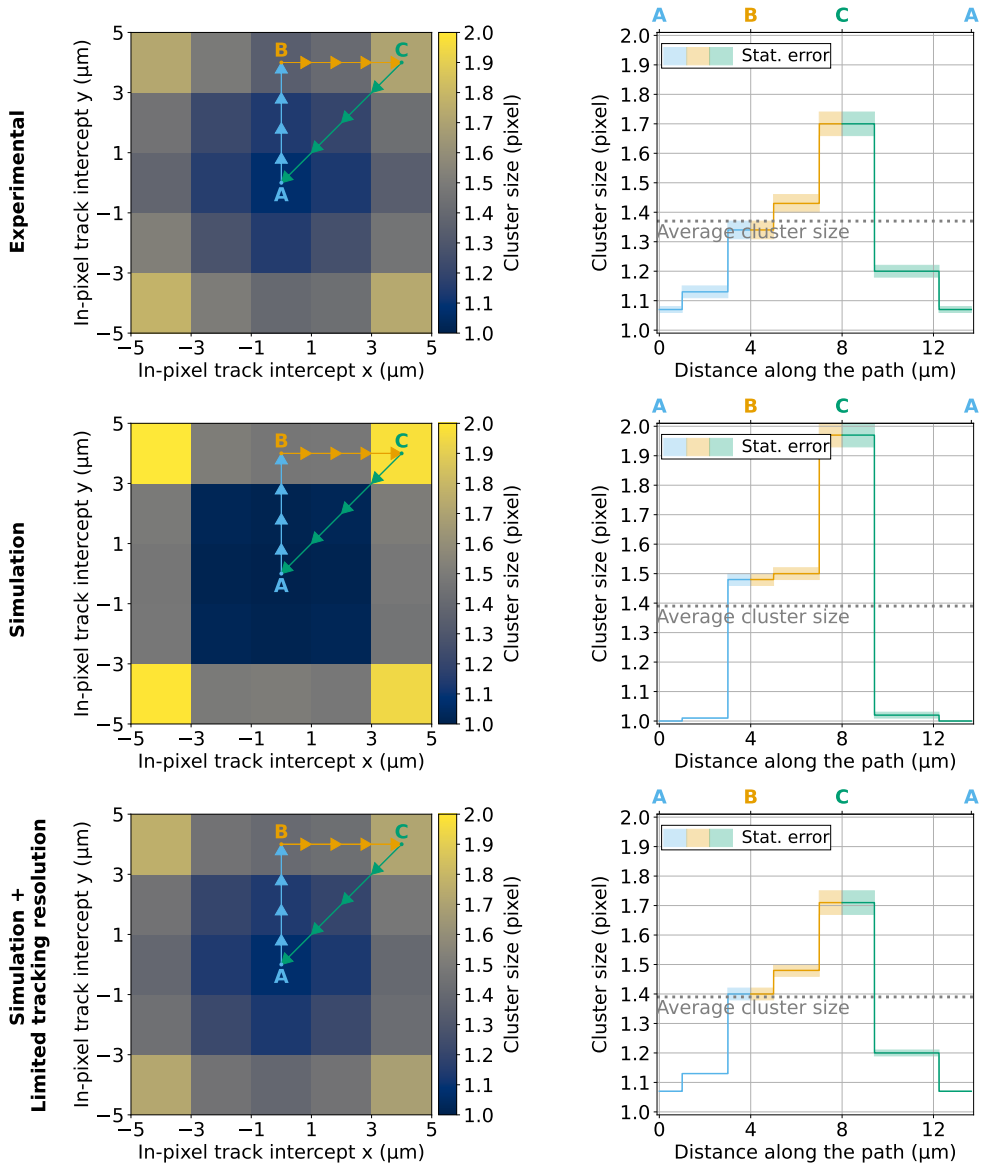


Figure 6.6 Cluster size map (left) and cluster size variation along the path from the pixel center to the edge, and to the corner (right) for experimental and simulated in-pixel track incidence positions of an APTS-OA sensor based on the modified with gap process operated at $V_{\text{sub}} = -4.8 \text{ V}$. For the experimental data (top row), the reconstructed track hit position is used. For the simulated data, the information provided by MC truth on the hit position (central row) and the same information affected by a limited tracking resolution of $1.8 \text{ } \mu\text{m}$ (bottom row) are illustrated.

6.6 Time resolution studies

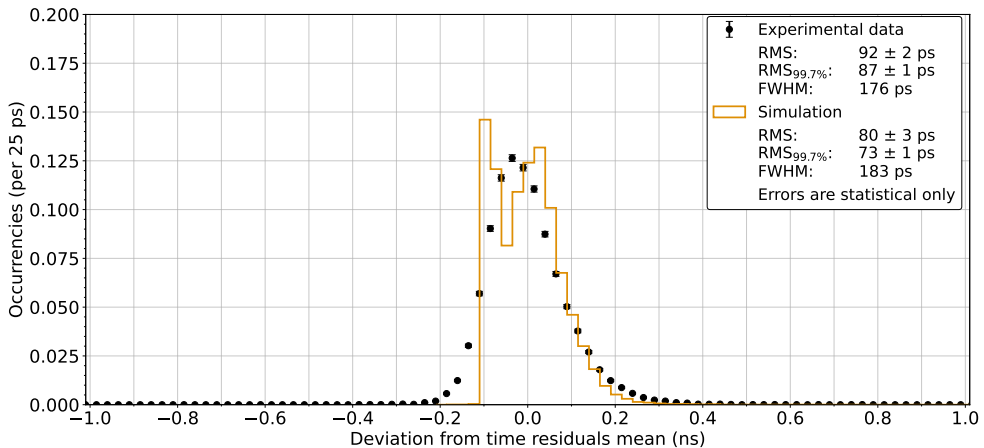


Figure 6.7 Comparison of the distributions of the deviation from time residuals mean obtained from the beam test measurements of an APTS-OA device implementing the modified with gap process (black points) and from a selection of simulated signals of the sensor model presented in Figure 6.4 (orange solid line), both operated at $V_{\text{sub}} = -4.8$ V.

The refined sensor model described in the second half of the previous section, which proved to reasonably approximate the experimental observations in terms of charge collection, is further studied in terms of timing performance. The time residual distribution obtained from the simulation data, computed as the time difference between the simulated signal time and the MC truth time given by the interaction of the simulated track with the detector, is compared with the experimental distribution measured with a modified with gap APTS-OA sample, which was discussed in Chapter 5. Figure 6.7 shows the deviation from the mean for both the experimental distribution, depicted with black points, and the simulated one, represented with orange solid line³. The latter is characterized by a double-peak structure, with an unexpected narrow peak at low time residuals, corresponding to the contribution of a set of faster signals. To investigate the nature of such events, the correlation between the deviation from the mean value of the time residual distribution and the associated cluster size mapped according to the MC truth in-pixel track incidence position is studied. As shown in Figure 6.8, the signals contributing to the fast time residual peak

³ In the comparison, one has to take into account that the experimental distribution's width is affected by the limited resolution of the time reference.

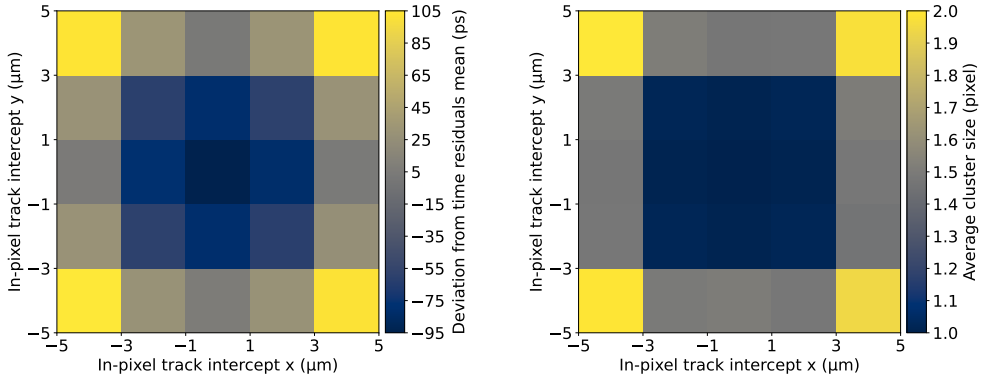


Figure 6.8 Map of the deviation from the time residuals mean value (left) and cluster size map (right) as a function of the MC truth in-pixel track incidence positions for the simulated sensor model represented in Figure 6.4 operated at $V_{\text{sub}} = -4.8$ V.

are associated to tracks hitting the center of the pixel, in the proximity of the collection electrode, where the generated charge is very likely collected by a single pixel only. This is confirmed also by Figure 6.9, where different distributions contributing to the time residuals are divided according to the size of the cluster they are associated with. The ‘fast peak’ clearly belongs to the single pixel cluster distribution only.

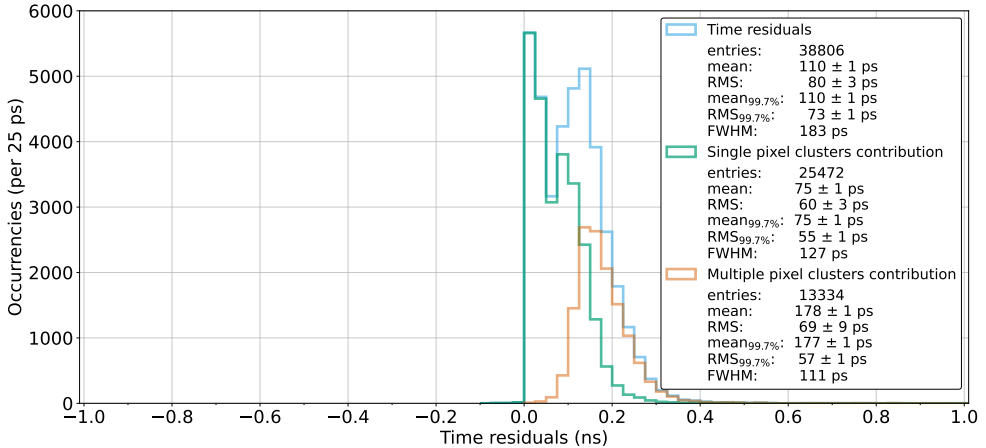


Figure 6.9 Distributions contributing to simulated time residuals (blue histogram) divided according to the associated cluster size for the simulated sensor model represented in Figure 6.4 operated at $V_{\text{sub}} = -4.8$ V. The green distribution represents the time residual values related to single pixel clusters, while the red one describes the contribution of clusters with pixel multiplicity larger than one.

The study of the simulated temporal resolution reveals that finer adjustments to the sensor model are needed to better approximate the experimental observation. In particular, from the analysis presented in this section, it is legitimate to think that the simulation underestimates the charge collection time in the center of the pixel with respect to the border, resulting in non-physically fast signals due to tracks hitting the pixel at the proximity of the collection electrode. It is reasonable to expect that an optimization of the thickness and doping concentration parameters pertaining to the n-type implant underneath the collection electrode, not performed for the studies presented in this dissertation, could provide a better description of the electric field in the pixel center and help to recover a single-peak time residual distribution. Moreover, the use of a transfer function properly describing the APTS-OA analog front-end, instead of the approximation discussed in Section 6.3.4, is expected to be beneficial for the calculation of the simulated voltage signals from the induced currents.

6.7 Discussion and conclusion

The simulation workflow discussed in this chapter is developed with the goal of obtaining a deeper understanding on the properties of monolithic sensors based on the TPSCo 65 nm CMOS imaging process. The combination of the Synopsys TCAD and Allpix² tools allows to study the behavior of the sensor, from the interaction with particles to the signal formation, including its electrostatic properties. The adopted simulation approach is based on a simplified description of the sensor, as approximated doping profiles are used to study the physics of the sensor. In particular, the TPSCo 65 nm CMOS modified with gap imaging process is the subject of this study, as the APTS-OA sensor variant based on the latter process is the one providing the best results in terms of time resolution. The simulated sensor model is then validated against experimental results.

The relevance of the charge generated in the substrate and collected after having diffused in the epitaxial layer for such thin monolithic sensors is highlighted in this chapter. In addition, the effect of the doping concentration on the lifetime of the charge carriers and of the interface between substrate and epitaxial layer are studied, and a reasonable agreement with the experimental distributions in terms of charge collection observables is found if these two factors are properly accounted for. Nonetheless, the latter model is not able to approximate the experimental results in terms of time resolution, for which deeper studies on the effect of the low dose n-type implant on the strength of the electric field in the central region of the pixel are required, together

with a better modeling of the pixel analog front-end.

From the experimental point of view, further verification and indications for refinement of the TCAD model can be provided by a measurement of an APTS-OA device with a Two Photon Absorption laser setup. It allows indeed to perform a high resolution 3D characterization of a silicon sensor and to eventually reconstruct a volumetric map of the drift field inside a pixel [20]. Such a setup has been built at Nikhef [21], and is currently being upgraded.

Upon full validation of the simulation against the experimental data, the pipeline presented here can be used as a design tool to test the performance of new designs for pixel based on the 65 nm CMOS technology.

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CHAPTER 7

Digital Pixel Test Structures in 65 nm CMOS process

THE Digital Pixel Test Structure (DPTS) is the most complex pixel sensor prototype implementing the TPSCo 65 nm CMOS imaging technology produced in the MLR1 submission. It features a complete readout chain, consisting of a per pixel analog front-end with discriminator and a global, fully asynchronous, digital readout.

Unlike the APTS-OA structures presented in the previous chapters, which aim at the investigation of the properties of sensors based on 65 nm CMOS imaging technology by directly accessing the analog signal of a few pixels, the DPTS is designed with the goal of studying larger area sensors, with multiple pixels to be read out at the same time. To make this possible, the pixel matrix has a digital readout logic to combine the outputs of multiple pixels.

This chapter contains a paper describing the properties of the DPTS and its characterization with laboratory tests, performed with charge injection via test pulsing and via an ^{55}Fe X-ray source, and with minimum ionizing charged particle beam measurements. In particular, the latter focus on the study of the detection efficiency and of the spatial resolution of samples irradiated at various ionizing doses and non-ionizing fluences, and on the temporal resolution of non-irradiated devices. The paper is titled *Digital Pixel Test Structures implemented in a 65 nm CMOS process* and is published in Nuclear Instruments and Methods A [1].

Digital Pixel Test Structures implemented in a 65 nm CMOS process

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Abstract The ALICE ITS3 (Inner Tracking System 3) upgrade project and the CERN EP R&D on monolithic pixel sensors are investigating the feasibility of the Tower Partners Semiconductor Co. 65 nm process for use in the next generation of vertex detectors. The ITS3 aims to employ wafer-scale Monolithic Active Pixel Sensors thinned down to 20 μm to 40 μm and bent to form truly cylindrical half barrels. Among the first critical steps towards the realisation of this detector is to validate the sensor technology through extensive characterisation both in the laboratory and with in-beam measurements. The Digital Pixel Test Structure (DPTS) is one of the prototypes produced in the first sensor submission in this technology and has undergone a systematic measurement campaign whose details are presented in this article.

The results confirm the goals of detection efficiency and non-ionising and ionising radiation hardness up to the expected levels for ALICE ITS3 and also demonstrate operation at $+20^\circ\text{C}$ and a detection efficiency of 99% for a DPTS irradiated with a dose of $10^{15} \text{ 1 MeV } n_{\text{eq}} \text{ cm}^{-2}$. Furthermore, spatial, timing and energy resolutions were measured at various settings and irradiation levels.

7.1 Introduction

Over the past decade, Monolithic Active Pixel Sensors (MAPS) have well established their position in high energy physics experiment vertex detectors [2–4]. By combining the readout circuitry and the sensitive volume in the same sensor produced in commercial processes, they pave the way for ultra-thin and large-scale tracking detectors. The state-of-art ALPIDE chip, in use in the ALICE Inner Tracking System 2 (ITS2), was produced in the TowerJazz 180 nm technology and demonstrated an excellent detection efficiency ($\gg 99\%$) and spatial resolution (5 μm) performance at very low power dissipation ($< 40 \text{ mW/cm}^2$) and material budget of $0.05 \%X/X_0$ up to irradiation levels of about 3 kGy and $10^{13} \text{ 1 MeV } n_{\text{eq}} \text{ cm}^{-2}$ [5–7]. Other developments produced in the same technology demonstrated comparable detection efficiency at -20°C even after a non-ionising radiation dose of $10^{15} \text{ 1 MeV } n_{\text{eq}} \text{ cm}^{-2}$ [8]. The next upgrade of ALICE tracker, the ALICE ITS3, planned for the Long Shutdowns 3 (2026-2028), is extending the requirements on the sensor characteristics. The ITS3 detector integration imposes a wafer-scale sensor size $O(10 \times 27 \text{ cm}^2)$ and operation at temperatures achievable by air cooling $O(20^\circ\text{C})$ [9].

In order to address the arising challenges in the design of the next generation MAPS detector, the Tower Partners Semiconductor Co. (TPSCo) 65 nm CMOS imaging process [10] was chosen as the starting point in the framework of the ALICE ITS3 upgrade [9, 11] and the CERN EP R&D on monolithic pixel sensors [12]. The critical

aspect of the new technology node for the ALICE ITS3 is the larger wafer size (30 cm as opposed to 20 cm in TowerJazz 180 nm process). The goal of the first submission designated MLR1 and produced in summer 2021, was to verify the radiation hardness (the expected levels for the ITS3 are below 10^{13} 1 MeV n_{eq} cm^{-2} and 10 kGy [9]) and the detection efficiency (>99%) of the MAPS produced in this technology. Therefore, a sensor prototype featuring in-pixel amplification and discrimination was characterised using soft X-rays and ionising particle beams and the results are described in this paper. In particular, the sensors were irradiated¹ up to 100 kGy and 10^{15} 1 MeV n_{eq} cm^{-2} and their detection efficiency and spatial, timing and energy resolutions were measured. In total, 48 sensors have been tested, with at least two for each radiation level (three in case of 10^{15} 1 MeV n_{eq} cm^{-2}). For visualisation purposes and to eliminate any selection bias, each measurement point is represented by a single device, chosen as the first one that was tested.

7.2 The DPTS chip

The Digital Pixel Test Structure (DPTS) is the most complex prototype MAPS produced in the first submission in TPSCo 65 nm technology process [10]. In order to optimise the technology for ionising particle detection, the submission was produced in four process splits, gradually modifying the doping levels of various implants (cf. Fig. 7.1a). The present work focuses only on the split expected to yield the best performance [13].

To better collect the signal charge and accelerate it to the collection diode, similar measures to those in the 180 nm technology have been applied [8, 14]. As illustrated in Fig. 7.1a, a deep, low-dose, *n*-type implant has been introduced to displace the junction from the collection diode into the epitaxial layer and thus deplete the epitaxial layer over the full pixel width [14]. This additional implant does not extend to the pixel border, but there is a gap in the implant near the pixel edges with the aim to increase the lateral field, pushing the signal charge to the collection diode [15]. This is expected not only to accelerate the charge collection but also to reduce charge sharing to give more operating margin due to the larger seed pixel signal.

The DPTS chip (cf. Fig. 7.1b) measures 1.5 mm $\times$ 1.5 mm and features a 32 $\times$ 32 pixel matrix of 15 μ m $\times$ 15 μ m pitch, controlled by a set of external reference currents and voltages, and read out via a current mode logic (CML) output. The in-pixel front end amplifies, shapes, and discriminates the signal from the collection diode. The

¹Sensors irradiated with non-ionising, ionising, and combined doses were exposed to neutrons at JSI Ljubljana, 10 keV X-rays from a tungsten target at CERN, and 30 MeV protons at NPI Prague, respectively.

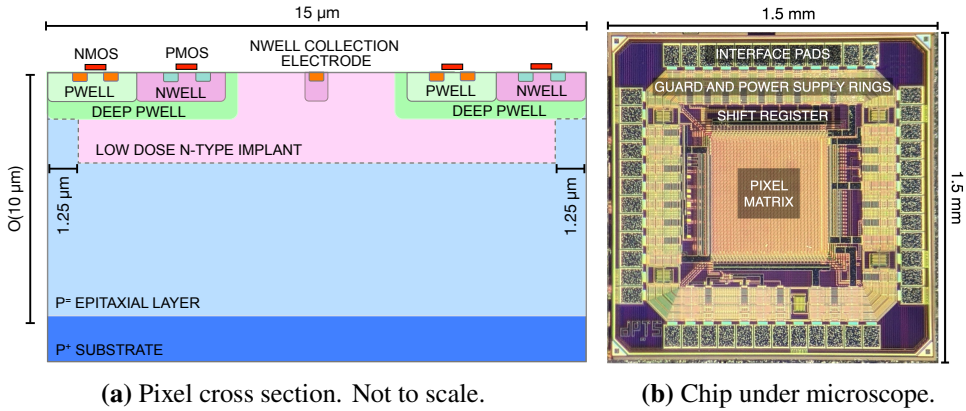


Figure 7.1 A cross section of a DPTS pixel and a photo of the chip under a microscope.

positions of the hit pixels are time-encoded (cf. Sec. 7.2.2) and all 1024 pixels are read out simultaneously via a differential digital output line (cf. Fig. 7.2). The pixels can be masked from readout and selected for pulsing via a 480 bit triplicated shift register. Given its space-constrained size, the possible masking and pulsing combinations are limited. Those used in this paper are the following: pulsing a single pixel, masking a single pixel, and masking the whole matrix with the exception of one row (unmasking a single pixel is not possible).

Figure 7.1b shows a photograph of the DPTS taken under a microscope. Starting from the centre and going outwards, the pixel matrix, shift register block, guard rings, and bonding pads can be distinguished. Most of the pads are dedicated to supplying power and reverse bias to the chip. The power supply is split into three domains (all operated at 1.2 V): analogue in-pixel front end, CML output driver, and all other digital circuitry. The reverse bias can be supplied separately to the substrate (V_{sub}) and the deep p-wells (V_{pwell}) hosting the circuitry (cf. Fig. 7.1a), however, in this work they were kept at the same potential.

There are three variants of the chip, implementing different time-encoding (cf. Sec. 7.2.2) and ground connection schemes². As the laboratory testing revealed no difference in their performance, no distinction will be made in the results discussed here.

²In one of the DPTS variants, the ground of the digital and analogue power domains is connected on the chip. In all the measurements presented in this paper, the ground was connected for all three power domains off-chip.

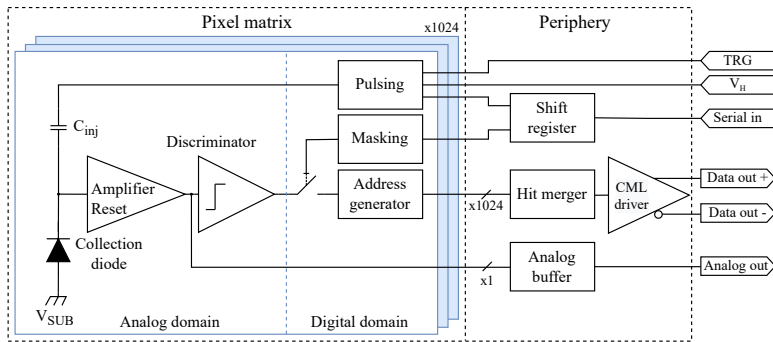


Figure 7.2 DPTS functional diagram. 1024 pixels can be masked from readout and selected for pulsing via a shift register. The addresses of hit pixels are read out via a differential digital output line. The in-pixel amplifier output of a single pixel is connected to an interface pad.

7.2.1 In-pixel front end

The analogue in-pixel front-end circuit (cf. Fig. 7.3) is controlled via four currents (I_{bias} , I_{biasn} , I_{reset} and I_{db}) and two voltages (V_{casb} and V_{casn}), all externally generated and supplied to the chip via the interface pads. The front end [16] is based on a high gain cascoded inverting amplifier, requiring direct feedback to the input to correctly define its operating point. This is achieved by the V_{casb} transistor (M6) in combination with the I_{reset} current source (M5): the feedback will make the current through the V_{casb} transistor equal to I_{reset} minus the leakage current on the collection electrode and correctly set the voltage of the collection electrode. When charge is collected on the collection diode, the output of the inverting amplifier at the source of the V_{casb} transistor will make a positive voltage excursion and switch off the V_{casb} transistor, causing the collection diode to be reset by a constant current and, therefore, resulting in a close to linear time-over-threshold behaviour. The high gain amplifier output is the input to a subsequent common-source stage (M9-M10). As soon as the amplifier output is sufficiently high for the input transistor of this second stage to overcome I_{db} , the output node of the second branch will fall and convert the signal into a digital rail-to-rail signal.

The front end has been designed to operate at current levels in the main branch (I_{bias} , M0-M3) between 10 nA and 5 μA , in a power-to-speed trade-off. The I_{biasn} current source (M8) balances the amplifier output current and is to be operated at one-tenth of the I_{bias} current. V_{casn} (M7) is used to further control the operating margin of the

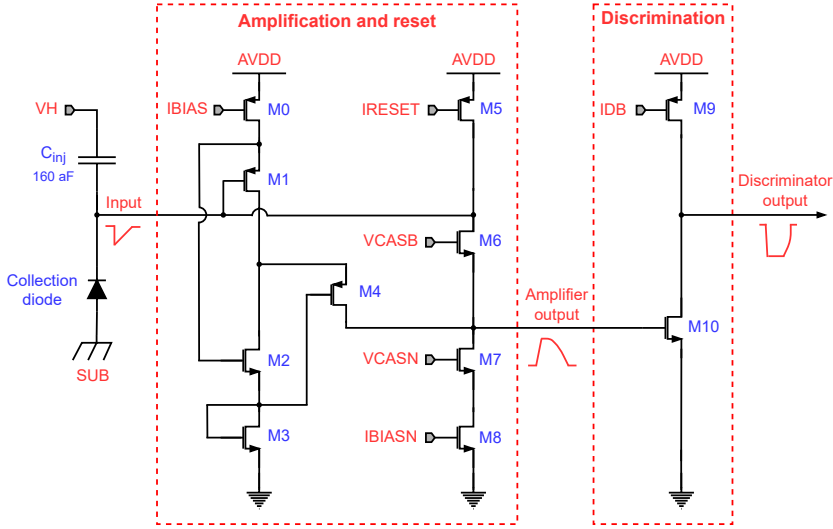


Figure 7.3 In-pixel amplifying, discriminating and reset circuit. All front-end biases are provided externally, in common to all pixels.

amplifier. In the lower current ranges, all transistors are in weak inversion. In addition, the NMOS transistors are subject to the reverse bias applied to the sensor (V_{pwell}), requiring biases like V_{casb} and V_{casn} to be adjusted to V_{pwell} voltage and current levels in the circuit. The power consumption in the steady state is given by the current in the main branch (I_{bias}) as the reset current is orders of magnitude lower and the I_{db} current in the discriminator branch is flowing only while M10 is active. With the typical settings used in this paper (cf. Sec. 7.3.1), it amounts to about 120 nW.

A test circuitry, which can inject charge in the collection electrode through a capacitance of $C_{inj} = 160$ aF, is also integrated in the pixel (cf. Fig. 7.2 and Fig. 7.3). The amount of injected charge can be regulated by an external voltage reference, V_h , and the injection is triggered by asserting the TRG signal via an interface pad.

Besides the 1024 digital output pixels, the DPTS features a monitoring pixel with an analogue output connected to an interface pad. The analogue pixel front end is identical to the one described above with the exception of the last common-source stage being replaced by a source follower, which buffers its analogue output signal to the interface pad.

7.2.2 Hit position encoding and time-over-threshold

The transition of the discriminator output triggers the address generator (cf. Fig. 7.2) to send two consecutive pulses on the CML output with a duration based on the pixel position [17]. As indicated in Fig. 7.4, the first pulse is of a fixed duration, the time distance between the two pulses encodes the pixel position in a group of columns (PID) and the duration of the second pulse the column group position in the matrix (GID).

The assertion and the deassertion of the discriminator result in two sets of pulses, delimiting the time interval in which the front-end pulse was over the threshold (ToT). Because the front end is designed such that the pulse length is monotonically increasing with the input signal, the ToT provides information on the collected or injected charge.



Figure 7.4 DPTS hit position encoding scheme. The two pulses encoding the pixel position with the matrix are sent to CML output, both at the assertion and at the deassertion of the discriminated pixel output signal.

As the time-encoded output of the 1024 pixels is merged to a single output line, two or more pixels firing simultaneously result in a signal collision, i.e. non-decodable output (the firing pixels' coordinates cannot be determined). In order to minimise the probability of signal collisions in case of charge sharing among neighbouring pixels, two optimisations were implemented in the encoding scheme: (1) the output signals of pixels in every other column are delayed by a fixed offset, and (2) in every other row of a column pair, the GID is swapped between the two pixels.

7.3 Laboratory measurements

7.3.1 Data acquisition setup

The laboratory and testbeam measurements used a custom-designed setup for the DPTS sensor that supplies biases and control signals to the chip. The CML and analogue outputs of the chip were recorded on an oscilloscope, with a sampling rate of 5 GS/s and a bandwidth of 500 MHz. For all the temperature sensitive measurements, in particular those involving irradiated chips, the chip temperature was controlled using a water-cooled (+20 °C) aluminium jig in thermal contact with the chip carrier card and thus the chip.

The bias settings of the chip are set to “nominal” values (defined by the design operating point) for all measurements unless otherwise stated or varied in the measurement. These settings are $V_{\text{casb}} = 300 \text{ mV}$, $V_{\text{casn}} = 300 \text{ mV}$, $I_{\text{reset}} = 10 \text{ pA}$, $I_{\text{db}} = 100 \text{ nA}$, $I_{\text{bias}} = 100 \text{ nA}$, $I_{\text{biasn}} = 10 \text{ nA}$, $V_h = 600 \text{ mV}$ (the pixel pulsing amplitude) and $V_{\text{sub}} = V_{\text{pwell}} = -1.2 \text{ V}$. For irradiated sensors, the I_{reset} is increased to 35 pA to overcome the sensor leakage current. Furthermore, when adjusting V_{pwell} , the values of V_{casb} and V_{casn} are adjusted as well (cf. Sec. 7.2.1). The maximum V_{pwell} foreseen by the design is -6 V , however, in this work, the V_{pwell} is capped at -3 V as further increasing it did not improve performance, at least not in the measurements presented here.

7.3.2 Analogue response

The inclusion of an additional monitor pixel to the chip allows the analogue pulse of the front end to be directly measured (cf. Sec. 7.2.1). The monitor pixel was pulsed, and the output responses at different chip bias settings are shown in Fig. 7.5, demonstrating the influence of varying V_h , V_{casb} , V_{casn} , I_{reset} , I_{bias} and I_{biasn} . For the case of I_{bias} , I_{biasn} was also varied, keeping $I_{\text{biasn}} = I_{\text{bias}}/10$, which is the recommended regime.

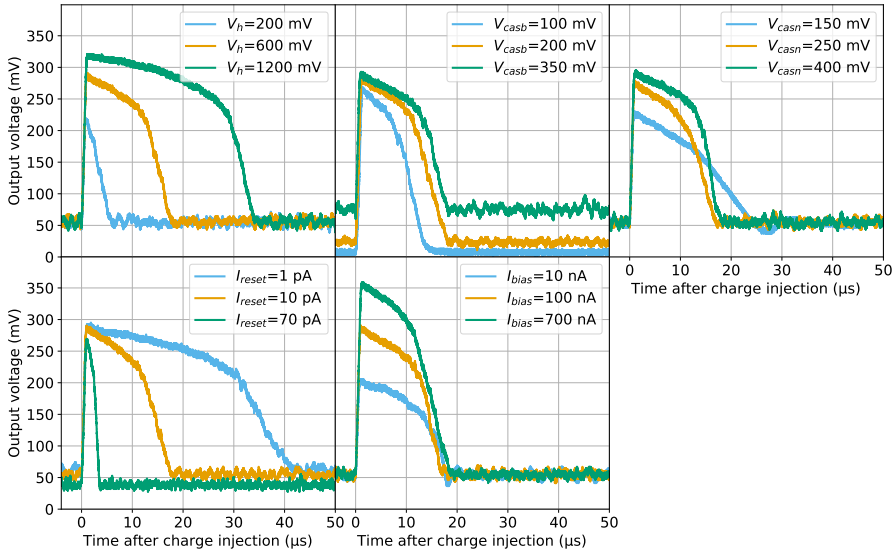


Figure 7.5 The analogue responses produced when the monitor pixel is pulsed and V_h , V_{casb} , V_{casn} , I_{reset} and I_{bias} are varied. For I_{bias} , $I_{\text{biasn}} = I_{\text{bias}}/10$. Other chip bias settings not mentioned in the legend are at nominal values (cf. Sec. 7.3.1).

Increasing V_h , which controls the injected charge, increases the amplitude and length of the pulse. It can easily be observed that, in accordance with the amplifier design (cf. Sec. 7.2.1) the pulse length, rather than amplitude, is proportional to the amount of injected charge. V_{casb} has a direct influence on the baseline, at low V_{casn} the pulse changes shape, I_{reset} changes the duration of the pulse and increasing I_{bias} increases the amplitude. The impact of changing I_{db} on the analogue pulse is not presented as this last stage of the front end is not included in the monitor pixel.

7.3.3 Threshold and noise

Investigation into the front-end response of the chip used the in-pixel pulsing circuitry to conduct threshold measurements. This involved counting the number of hits while varying V_h , that is, the amount of injected charge. For every V_h value, each pixel was pulsed 25 times. As the injected charge approaches the threshold, the number of hits increases until a plateau is reached, producing a so-called “s-curve”. Figure 7.6 shows examples of the measured s-curves. The threshold and the noise are given by the mean and standard deviation of the derivative of the s-curve, respectively. A hit was determined to occur if at least two sets of pulses were captured by the oscilloscope, ensuring both the assertion and deassertion of the discriminator were recorded (cf. Sec. 7.2.2). The final threshold value is calibrated to electrons via a measurement of the $Mn-K_\alpha$ peak position, details of which are given in Sec. 7.3.7, and this method is used throughout the paper. This calibration is done separately for each sensor, as deviations of up to 20% of the measured injection capacitance with respect to its design value have been observed.

Examples of the pixel threshold and noise distributions at $V_{sub} = 0\text{ V}$, -1.2 V and -3 V are shown in Fig. 7.7, with the V_{casb} value chosen such that the mean threshold of all pixels is 180 e^- . The threshold distributions show comparable performance for $V_{sub} = -1.2\text{ V}$ and -3 V , with both having a similar width and centred around 180 e^- . However, at $V_{sub} = 0\text{ V}$, the distribution is wider and asymmetric – indicating a substantial pixel-to-pixel threshold spread resulting in a non-uniform response across the matrix. For the noise distributions, $V_{sub} = 0\text{ V}$ continues to show the widest distribution, while $V_{sub} = -1.2\text{ V}$ has a better performance in terms of a smaller mean and spread than $V_{sub} = -3\text{ V}$, suggesting non-optimal chip biasing settings for $V_{sub} = -3\text{ V}$. In general, even with chip biasing settings optimised for threshold and noise, a worse performance in terms of threshold spread and noise was observed when decreasing V_{sub} towards 0 V or increasing it towards -3 V and above.

Figure 7.8 demonstrates the effect of the chip bias settings on the threshold at

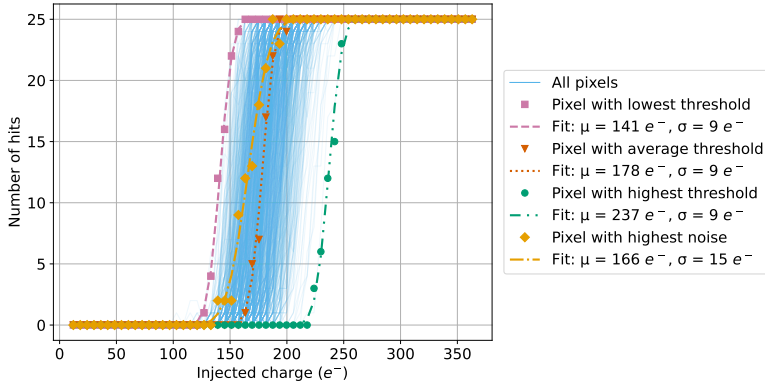


Figure 7.6 S-curves of a chip tuned to a threshold of $180 e^-$ with $V_{\text{casb}} = 180 \text{ mV}$ at $V_{\text{sub}} = -1.2 \text{ V}$. Four pixels have been highlighted along with their s-curve fits (non-solid lines). These four pixels represent the response of pixels with the lowest, average and highest threshold and the pixel with the highest noise. Other chip bias settings are at nominal values (cf. Sec. 7.3.1).

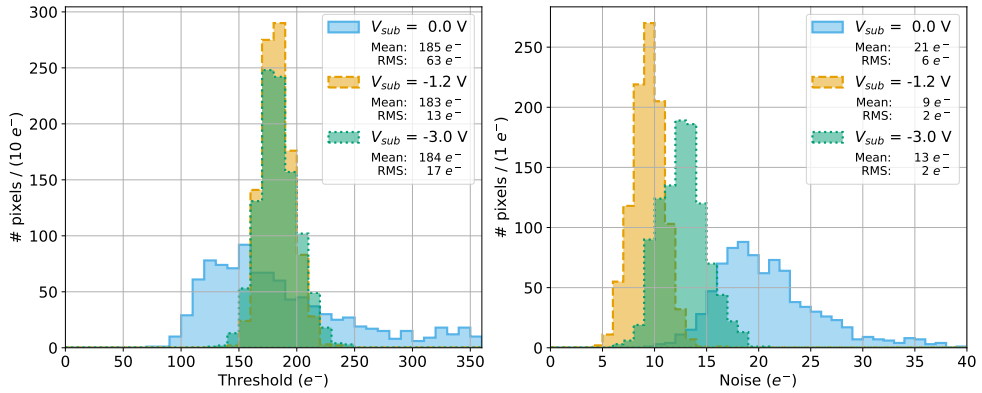


Figure 7.7 Pixel threshold (left) and noise (right) distributions of a chip tuned to a threshold of $180 e^-$ with $V_{\text{casb}} = 110, 180$ and 500 mV at $V_{\text{sub}} = 0.0, -1.2$ and -3 V , respectively. Other chip bias settings are at nominal values (cf. Sec. 7.3.1).

$V_{\text{sub}} = 0 \text{ V}, -1.2 \text{ V}$ and -3 V by plotting the mean and the RMS (given by the error bars) of all pixels. For V_{casb} , it can be observed that this chip bias has the largest impact on the threshold. Also, there is a linear relationship between the mean threshold and V_{casb} in a certain range, which is larger for larger V_{sub} . This linear relationship is the motivation for using V_{casb} as the main handle to control the threshold of the chip during operation and for all subsequent results. Figure 7.8 also illustrates that

at different V_{sub} values, the same value of V_{casb} does not produce the same mean threshold.

While the other chip biases affect the threshold as well, for V_{casn} , I_{bias} and I_{biasn} , the influence is expected to be minimal once in a stable operating regime. The changes due to chip biases other than V_{casb} are largest at $V_{\text{sub}} = 0$ V. Whereas, at lower reverse bias values, the changes to the mean threshold (for the plotted range) are within $100 e^-$ except for I_{reset} , where the increase is around $150 e^-$. However, this large dependence of the threshold on I_{reset} does not mean that this parameter is a good handle to set the threshold because changing I_{reset} alters the diode biasing (cf. Sec. 7.2.1) and influences the charge collection properties. Consequently, I_{reset} is only used to compensate for the increased leakage current caused by non-ionising radiation damage and not to tune the threshold.

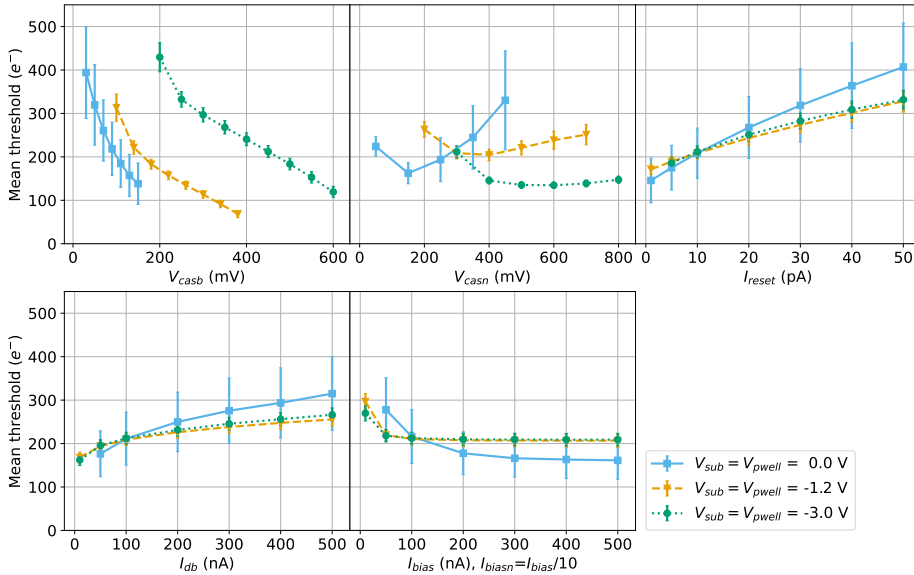


Figure 7.8 The mean threshold as a function of different chip bias settings at V_{sub} of 0.0, -1.2 and -3 V with V_{casb} set to 95, 150 and 450 mV, respectively. V_{casb} was tuned so that the mean threshold was $210 e^-$ for nominal settings. The error bars represent the threshold RMS. The parameters not varied in the measurement are at nominal values (cf. Sec. 7.3.1).

Another operating condition that impacts the threshold is the temperature. Measurements of a non-irradiated chip have shown the mean threshold decreases by $0.5 e^-$ per degree Celsius in the measured range of 15°C to 40°C . However, for an irradiated chip, the dependence is not linear. This is compatible with the non-linear dependence

of the leakage current on the temperature for higher non-ionising radiation fluence levels.

7.3.4 Time-over-threshold

Further investigation into the front-end response was performed by observing the impact of the chip biasing settings on the time-over-threshold (ToT, cf. Sec. 7.2.2). By varying the injected charge, Q_{inj} , and measuring the ToT for all pixels, it can be seen from Fig. 7.9 that at lower injected charge values, around the pixel threshold, the response is non-linear. Whereas, for larger injected charge values, the ToT response becomes linear and the spread in the ToT increases. There is also a sizeable pixel-to-pixel variation that is demonstrated by highlighting the response of two pixels. To account for this spread, a ToT calibration was performed for all pixels individually, by fitting with the empirical function

$$ToT = aQ_{inj} + b - \frac{c}{Q_{inj} - d}, \quad (7.1)$$

where a , b , c and d are the fit parameters. Example fits of two pixels are shown by the solid lines in Figure 7.9. The effect of the ToT calibration to normalise the pixel response over the matrix is shown and discussed in Sec. 7.3.7.

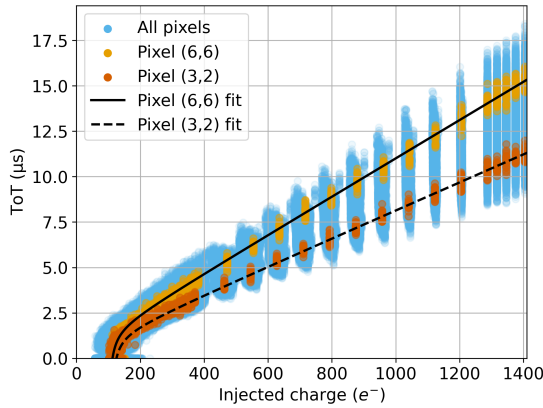


Figure 7.9 Time-over-threshold (ToT) as a function of injected charge for all pixels with two pixels highlighted to demonstrate the pixel-to-pixel variation. The two pixels have been fitted with Eq. 7.1 shown by the solid and dashed lines.

The impact of the other chip biases on ToT was also investigated at a fixed charged injection of $725 e^-$. The results in Fig. 7.10 demonstrate that I_{reset} produces the most significant change in ToT (within $40 \mu s$), which is compatible with I_{reset} resetting the

diode (cf. Sec. 7.2.1). For the other biases, the change is within $10\ \mu\text{s}$. Furthermore, the non-linear behaviour of the ToT as a function of V_{casb} for values above $70\ \text{mV}$ illustrates the limited operation margin at $V_{\text{sub}} = 0\ \text{V}$.

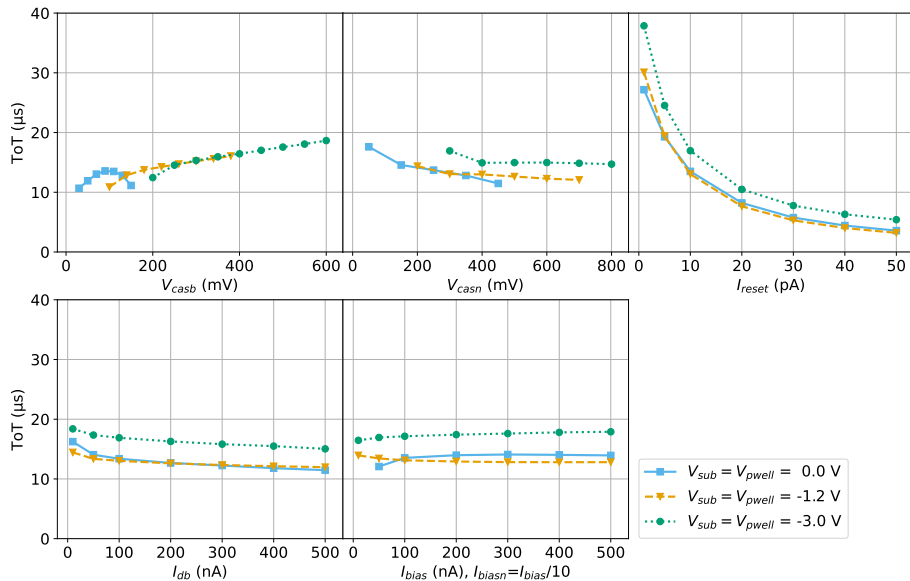


Figure 7.10 Time-over-threshold (ToT) as a function of different chip biases at a fixed charged injection of $725\ e^-$. Non-varied parameters are at nominal values (cf. Sec. 7.3.1).

7.3.5 Fake-hit rate

The impact of the chip bias settings on the fake-hit rate (FHR) was evaluated and is shown in Fig. 7.11. The FHR is defined as the number of hits per pixel and second in the absence of external stimuli as the chip operates in a continuous readout. Given that the oscilloscope captures a fixed-size time window, the FHR is estimated as the aggregate of hits in a number of randomly triggered oscilloscope acquisitions divided by the sum of their duration and the total number of pixels (1024). In general, the measurements show that the lower the threshold, the higher the FHR. As with the threshold results shown in Sec. 7.3.3, operating at $V_{\text{sub}} = -1.2\ \text{V}$ gives the best performance, with many of the results below the sensitivity limit³ of the measurements, even at the low threshold used for the measurements. At $V_{\text{sub}} = 0\ \text{V}$, the sharp increase

³The sensitivity limit is defined as the lowest measurable FHR for the number of oscilloscope captures in the measurement.

in the FHR from the lowest operable V_{casb} further illustrates the limited operation margin without supplying reverse bias.

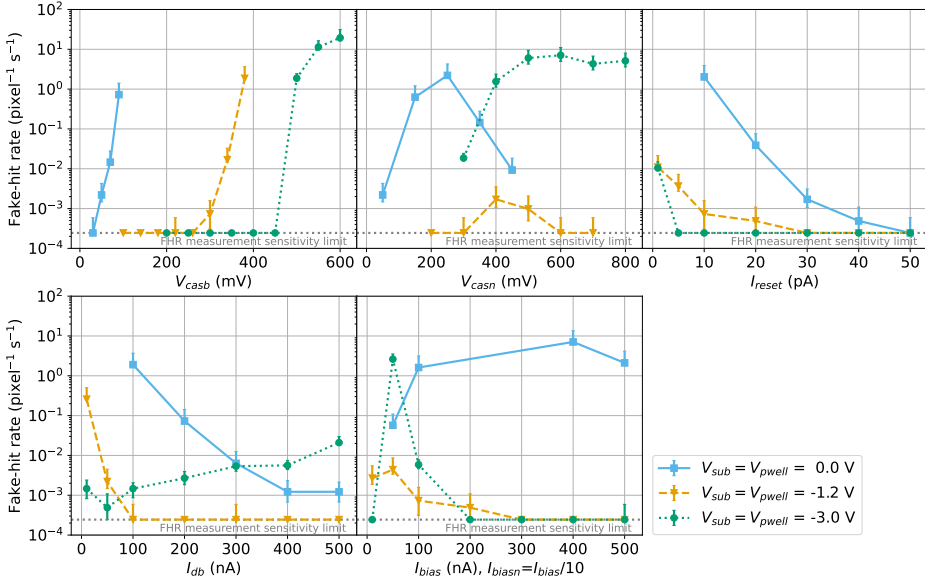


Figure 7.11 Fake-hit rate as a function of different chip biases. At $V_{sub} = -1.2$ V, the threshold was set at $120 e^-$, while for the other V_{sub} values it was $210 e^-$ (for the nominal parameters). Other chip bias settings not varied in the measurement are at nominal values (cf. Sec. 7.3.1).

7.3.6 Pixel position decoding

As described in Sec. 7.2.2, the positions of the hit pixels are time-encoded in the CML output pulses in terms of PIDs and GIDs. An example of the measured PIDs and GIDs for all pixels, each pulsed 100 times, at $V_{sub} = V_{pwell} = -1.2$ V and -3 V is given in Fig. 7.12. It can be observed that the data points form clusters, corresponding to 1024 pixels. Some of the clusters for the different pixels are very close (and look to be overlapping due to an artefact of the axis scales), demonstrating where the decoding errors can arise.

Given that the time constants in the encoding are dependent on the production process and measurement conditions [17], a decoding calibration is needed to convert the measured PIDs and GIDs of the waveforms to pixel rows and columns. The calibration is performed by pulsing each pixel 100 times and measuring the PIDs and GIDs of the recorded waveforms. The centre of gravity of the PID and GID cluster

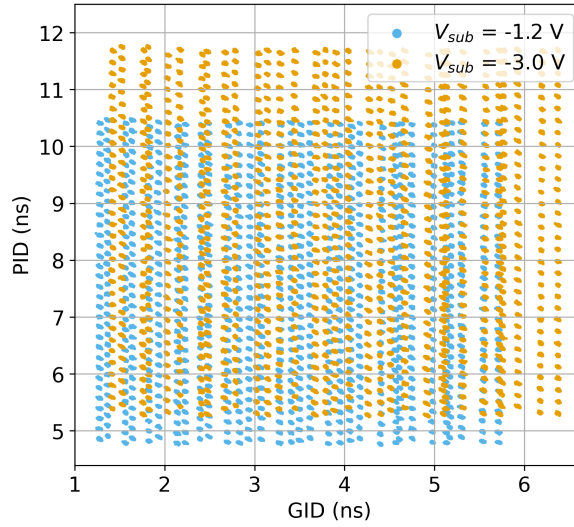


Figure 7.12 The PID and GID data points corresponding to all pixels pulsed 100 times at $V_{sub} = V_{pwell} = -1.2 \text{ V}$ and -3 V demonstrating the reverse bias dependence. Each cluster consists of 100 points and represents the measured PID and GID value for one pixel.

for each pixel gives the decoding calibration. By associating a (GID, PID) pair to the nearest centre of gravity, the conversion to columns and rows is obtained.

Except for the reverse bias dependence, PIDs and GIDs were found to also depend on supply voltage and temperature. In particular, it was found that the mean PID and GID increase by 8 ps and 4 ps per degree Celsius, respectively, in the range 15°C to 40°C .

7.3.7 Measurements with X-rays emitted by an ^{55}Fe source

X-ray emissions from an ^{55}Fe source illuminating the top side of the chip at a distance of approximately 12 mm have been measured. Two cuts have been applied to the data: the removal of all pixels on the matrix edge and the removal of pixels with hit rates of five standard deviations above the mean. The measured signal spectrum of clusters involving only one pixel for a sensor with a threshold tuned to $120 e^-$ is shown in Fig. 7.13 (in blue).

A ToT calibration for each pixel is applied to account for the variation in the pixel-to-pixel response, as described in Sec. 7.3.4. After the ToT calibration, the Mn-K_α and Mn-K_β emission peaks are resolved, as shown in Fig. 7.13 (in orange), as

well as the $\text{Mn-K}_{\alpha,\beta}$ escape ($\text{Mn-K}_{\alpha,\beta} - \text{Si-K}_{edge}$) and silicon fluorescence ($\text{Si-K}_{\alpha,\beta}$) peaks. The Mn-K_{α} and Mn-K_{β} peaks are fitted with a sum of two Gaussians. The resolution of the Mn-K_{α} peak is defined as the FWHM divided by the measured peak value and was calculated to be $7.42\% \pm 0.01\%$. For the fluorescence and escape peaks, the signal is fitted with a Gaussian and a background fit of either exponential or linear form for the fluorescence and escape peaks, respectively. Since the response of ToT as a function of injected charge was found to be linear for ToT values above $3 \mu\text{s}$ (cf. Sec. 7.3.4), the comparison between the measured and literature peak values is fitted with a linear function, giving the conversion from ToT to energy in e^- .

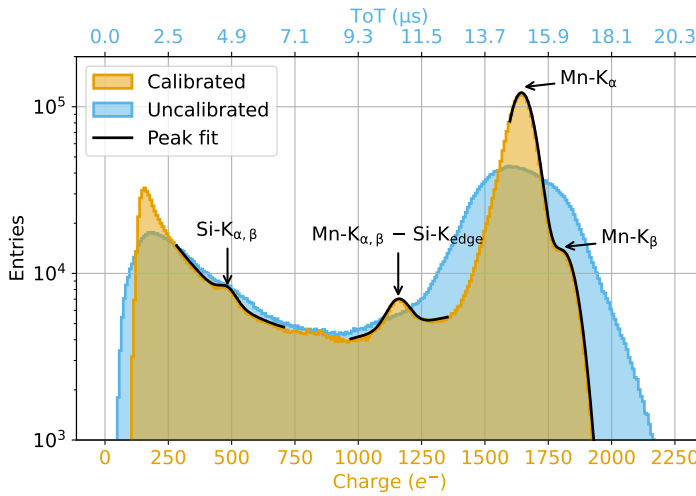


Figure 7.13 Measured ^{55}Fe spectrum of single pixel clusters with a threshold set to $120 e^-$. The initial spectrum (blue) is ToT calibrated (orange) which resolves the two x-ray peaks (Mn-K_{α} and Mn-K_{β}) plus the $\text{Mn-K}_{\alpha,\beta}$ escape ($\text{Mn-K}_{\alpha,\beta} - \text{Si-K}_{edge}$) and silicon fluorescence ($\text{Si-K}_{\alpha,\beta}$) peaks.

Figure 7.14 shows the measured ^{55}Fe spectra for sensors irradiated with different non-ionising doses (non-irradiated, 1×10^{13} , 1×10^{14} and $1 \times 10^{15} \text{ 1 MeV n}_{eq} \text{ cm}^{-2}$). For these measurements, the seed pixel ToT is plotted, where the seed pixel is defined as the pixel with the largest ToT in the set of adjacent pixels firing within the same oscilloscope capture. As the level of irradiation increases, the Mn-K_{α} peak becomes broader, with a notable broadening between $1 \times 10^{14} \text{ 1 MeV n}_{eq} \text{ cm}^{-2}$ and $1 \times 10^{15} \text{ 1 MeV n}_{eq} \text{ cm}^{-2}$. These differences are shown in the resolution of the Mn-K_{α} peak between the irradiated sensors whose values are given in Table 7.1. The table shows that the largest increase in the resolution is from $1 \times 10^{14} \text{ 1 MeV n}_{eq} \text{ cm}^{-2}$ to $1 \times 10^{15} \text{ 1 MeV n}_{eq} \text{ cm}^{-2}$. In addition, at the largest irradiation dose, the four peaks

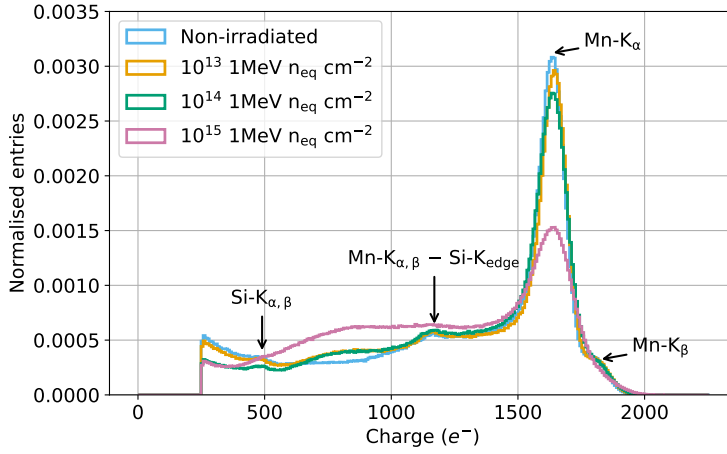


Figure 7.14 Measured ^{55}Fe spectra of seed pixels for different levels of non-ionising irradiation: non-irradiated, 1×10^{13} , 1×10^{14} and 1×10^{15} $1 \text{ MeV } n_{\text{eq}} \text{ cm}^{-2}$.

are no longer resolved and the contribution from seed pixels with energy in the range of $400 e^-$ to $1400 e^-$ becomes more prominent. These changes to the spectrum at 1×10^{15} $1 \text{ MeV } n_{\text{eq}} \text{ cm}^{-2}$ indicate an alteration to the charge collection mechanisms in the sensor due to radiation damage, such as the increased recombination rate and the changes in the electric fields.

Table 7.1 Measured resolution of the Mn-K_α peak for different levels of non-ionising irradiation in seed pixel signal spectra in Fig. 7.14.

Irradiation	Resolution (%)
Non-irradiated	7.40 ± 0.02
1×10^{13} $1 \text{ MeV } n_{\text{eq}} \text{ cm}^{-2}$	7.42 ± 0.03
1×10^{14} $1 \text{ MeV } n_{\text{eq}} \text{ cm}^{-2}$	8.73 ± 0.02
1×10^{15} $1 \text{ MeV } n_{\text{eq}} \text{ cm}^{-2}$	12.05 ± 0.07

7.4 Measurements with ionising particle beams

The DPTS sensors were also characterised at facilities providing charged particle beams. The results presented in this section are based on data taken from September 2021 to July 2022 at DESY II [18] and CERN PS testbeam facilities. As such, the

sensors were subject to normally incident 5.4 GeV/ c electrons and 10 GeV/ c positive hadrons, respectively.

7.4.1 Setup

A beam telescope comprising of reference planes equipped with ALPIDE chips [5–7] has been used to reconstruct particle tracks. Two DPTS sensors were installed in-between the reference planes. A sketch of the beam telescope is shown in Fig. 7.15. The data acquisition was based on the EUDAQ2 framework [19]. The trigger signal was provided either by one of the DPTS chips or by a discriminated output of photomultiplier tubes (operated in the plateau regime) connected to a set of three 2 cm×2 cm scintillators placed in front and behind the telescope. One of the scintillators (S1) features a 1 mm hole in its centre and is operated in anti-coincidence with the other two ($\neg S1 \wedge S2 \wedge S3$, cf. Fig. 7.15). The x and y position of a DPTS and the anti-coincidence scintillator were adjustable via micro-positioning stages to achieve the overlap with the other DPTS. The DPTS chip(s) not used for triggering are the device(s) under test or DUT(s). An aluminum cooling jig (cf. Sec. 7.3.1) with a 1 mm opening corresponding to the chip position was used to keep the DUT at a controlled temperature of 20 °C during the detection efficiency and position resolution measurements.

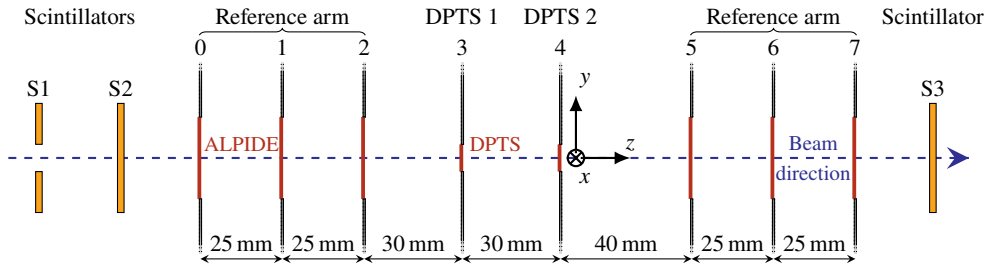


Figure 7.15 Sketch of the beam telescope (not to scale). Two DPTS are sandwiched between reference planes comprised of ALPIDE chips. Two scintillators (S2 and S3), operated in coincidence, and one featuring a 1 mm hole (S1), operated in anti-coincidence, are used for triggering. The trigger can also be provided by one of the two DPTS.

7.4.2 Analysis tools and methods

Data were processed in the Corryvreckan test beam reconstruction software framework [20] by fitting General Broken Lines [21] to clusters found in the reference planes

and interpolating the tracks to the DUT(s). Event and track quality selection criteria were applied to ensure a clean data sample: precisely one track per event, reduced track $\chi^2 < 3$, and track points on each reference plane. Pixels on the reference planes with too large hit-rate (more than 1000 times the average; < 1 pixel per plane were affected) were masked. Furthermore, the tracks intersecting the DUT within two pixel pitches from the sensor edge were rejected.

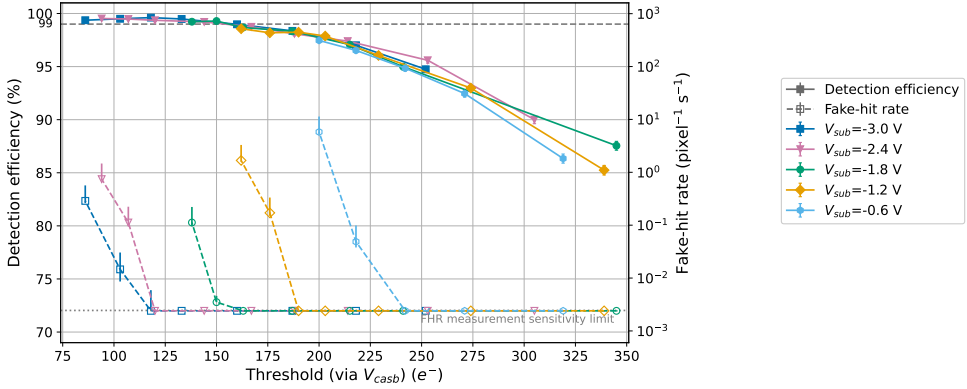
The DPTS hit pixel position was derived from the CML output corresponding to the assertion of the in-pixel discriminator (cf. Sec. 7.2.2). The non-decodable events, resulting from the collisions on the CML lines when multiple pixels fire simultaneously, were associated to pixel (15, 15), i.e. to the centre of the matrix. Given the negligible likelihood that two fake hits coincide in time and result in a non-decodable event, these events are considered as real hits with an undetermined position. The fraction of such events was below 3%, for all chips and settings.

In the detection efficiency calculation, the DUT clusters were associated to tracks passing within a circular window with a radius of $480\text{ }\mu\text{m}$. The loose spatial cut prevents the underestimation of the efficiency that would result from the exclusion of non-decodable events associated to pixel (15, 15). In order to minimise the probability of associating a fake (noise) hit to a track, the DUT response was required to be within $1.5\text{ }\mu\text{s}$ of the trigger signal. The efficiency of the DUT is then estimated by the fraction of tracks with associated clusters. The relative uncertainties are obtained by calculating the 68.3% Clopper-Pearson confidence interval and summing in quadrature the probability of associating a fake hit (given by the in-situ measured fake-hit rate, cf. Sec. 7.3.5 and Sec. 7.4.3).

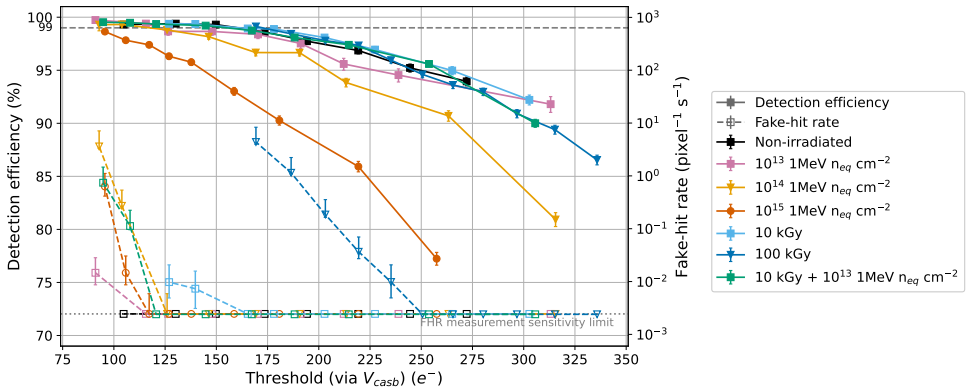
For the position resolution evaluation, a spatial acceptance window with a radius of $45\text{ }\mu\text{m}$ around the track and a time acceptance window of $1.5\text{ }\mu\text{s}$ were applied. The distance between the intercept on the DUT plane and the associated cluster position (given by the centre of mass of pixels in the cluster) in column and row direction is determined for each track, yielding two spatial residual distributions. By fitting the latter with two Gaussian functions, the standard deviation parameters σ_{col} and σ_{row} are obtained. The position resolution is then retrieved by quadratically subtracting the estimated telescope tracking resolution of $\sigma_{\text{track}} = 2.4\text{ }\mu\text{m}$ [22]. Given that the obtained position resolution in the two directions is equal within the measurement precision and compatible with square pixel geometry, their average will be referred to as the position resolution in the rest of the paper.

The timing resolution analysis involved no time acceptance window, while the spatial acceptance window was the same one used in the position resolution analysis.

7.4.3 Detection efficiency and fake-hit rate



(a) Sensor irradiated to a dose of 10 kGy and 10^{13} 1 MeV n_{eq} cm^{-2} at different $V_{sub} = V_{pwell}$.



(b) Sensors irradiated to different levels.

Figure 7.16 Detection efficiency (filled symbols, solid lines) and fake-hit rate (open symbols, dashed lines) as a function of average threshold, measured with 10 GeV/c positive hadrons.

Figure 7.16a shows the detection efficiency and the fake-hit rate (measured in situ) as a function of the average chip threshold set by changing V_{casb} at different reverse biases for a sensor irradiated with protons, i.e. that has received a combination of an ionising dose of 10 kGy and a non-ionising dose of 10^{13} 1 MeV n_{eq} cm^{-2} (levels compatible with the ITS3 requirements). Instead of showing the data for a non-irradiated sensor, which exhibits fake-hit rates below the measurement sensitivity limit, this particular sensor was chosen to better illustrate the effect of the reverse bias on the performance. In particular, it can be observed that by increasing $V_{sub} = V_{pwell}$,

the onset of the measured fake-hit rate is offset to lower thresholds, thus increasing the operational margin at above 99% detection efficiency.

The effect of different irradiation levels on the detection efficiency and the fake-hit rate is shown in Fig. 7.16b, where the reverse bias is kept at -2.4 V. It can be observed that non-ionising irradiation leads to a decrease in the detection efficiency, while ionising irradiation leads to an increase in the fake-hit rate. These trends are consistent with the expectation that the largest effect of the non-ionising and ionising radiation damage is on the charge collection and the noise (front-end) performance, respectively. For the 100 kGy irradiated sensor, a significant increase in the fake-hit rate can be noticed, with onset at a much higher threshold than in the other cases. Finally, although the 10^{15} 1 MeV n_{eq} cm^{-2} irradiated sensor shows notable performance deterioration, it can still be operated at 99% efficiency at the temperature of 20°C .

The origin of the detection efficiency loss was investigated by studying its dependency on the particle hit position within a pixel. Figure 7.17 shows the detection efficiency of a 10^{15} 1 MeV n_{eq} cm^{-2} irradiated sensor as a function of reconstructed track position relative to the nearest pixel centre. As expected, the detection efficiency decreases when the particle track is further away from the collection diode. A similar result was obtained for a non-irradiated sensor, with the same magnitude of efficiency loss observed at higher thresholds.

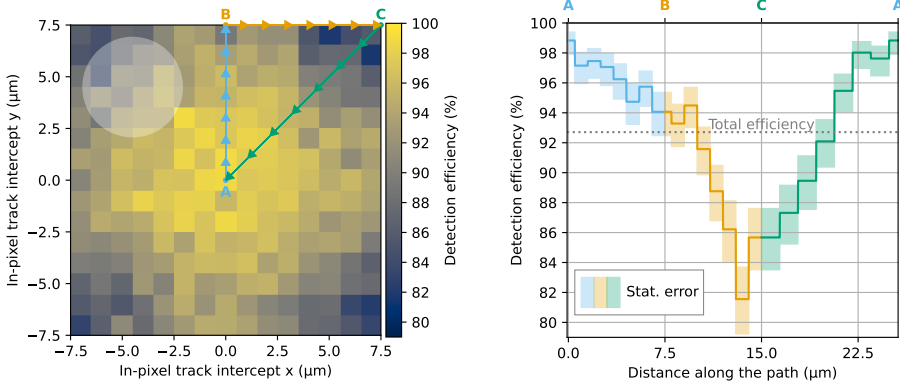
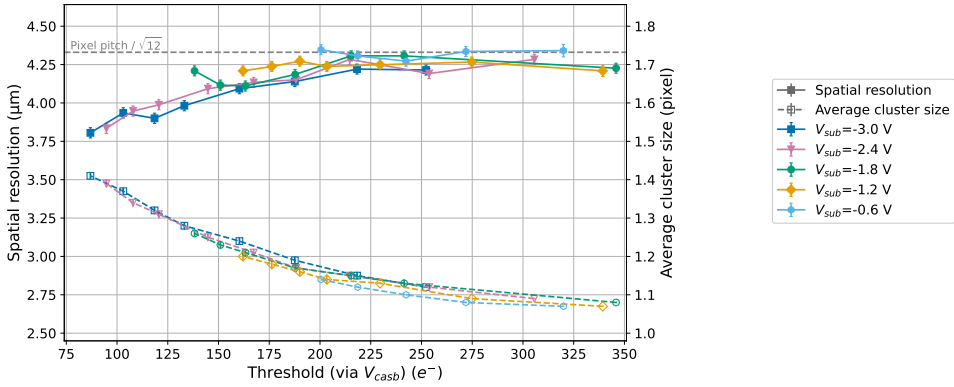


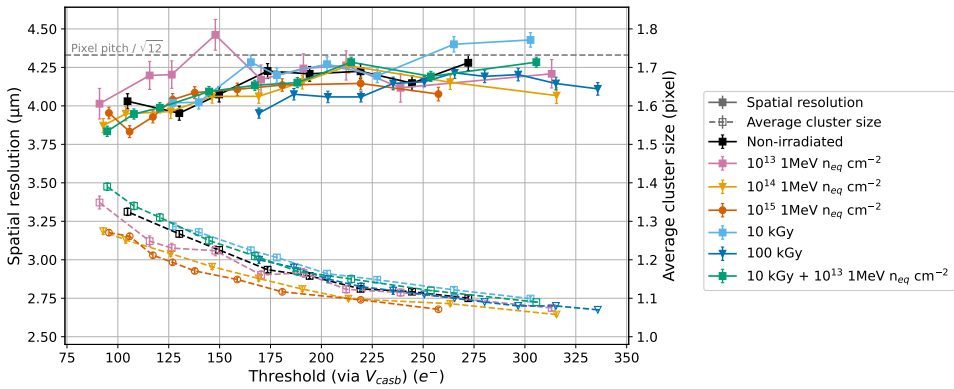
Figure 7.17 In-pixel detection efficiency of a 10^{15} 1 MeV n_{eq} cm^{-2} irradiated sensor with threshold set to $160 e^-$, measured with $10 \text{ GeV}/c$ positive hadrons. The tracking resolution is represented by the white circle ($r = \sigma_{\text{track}} = 2.4 \mu\text{m}$) in the top left corner.

7.4.4 Spatial resolution and cluster size

Figure 7.18a shows the sensor spatial resolution and average cluster size as a function of the average threshold for different V_{sub} applied, measured with 10 GeV/c hadrons for the device irradiated with both an ionising radiation dose of 10 kGy and a non-ionising radiation dose of 10^{13} 1 MeV n_{eq} cm^{-2} (levels compatible with the ITS3 requirements). The benefit of applying higher V_{sub} is not evident without combining the information from Fig. 7.16a, which shows that higher V_{sub} is necessary to operate at lower thresholds. In this regime, the additional positional information, given by a larger average cluster size, results in a spatial resolution better than that of a purely binary sensor (pixel pitch divided by $\sqrt{12}$).



(a) Sensor irradiated to a dose of 10 kGy and 10^{13} 1 MeV n_{eq} cm^{-2} at different $V_{\text{sub}} = V_{\text{pwell}}$.



(b) Sensors irradiated to different levels.

Figure 7.18 Spatial resolution (solid lines) and average cluster size (dashed lines) as a function of the average threshold, measured with 10 GeV/c positive hadrons.

The effect of different irradiation levels on the spatial resolution and the average cluster size is demonstrated in Fig. 7.18b, where the reverse bias is kept constant at -2.4 V. Regardless of the irradiation level, the measured spatial resolution is equal or even slightly better than pixel pitch divided by $\sqrt{12}$, with no degradation of the spatial resolution performance related to the received dose. The average cluster size exhibits a slight, but systematic, decrease with the increasing non-ionising radiation dose. This trend is compatible with the previous observations of a deteriorated charge collection process.

7.4.5 Timing resolution

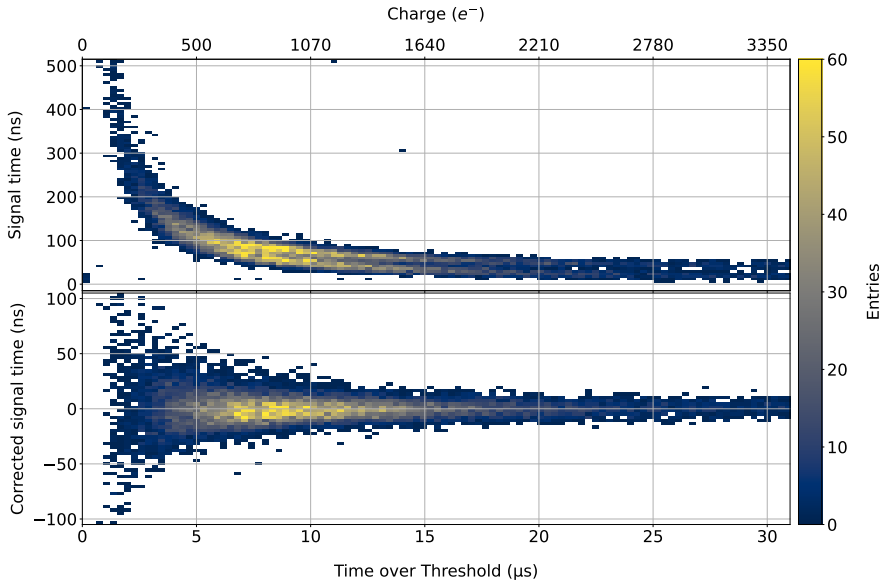


Figure 7.19 Signal time vs ToT for the upstream DPTS measured with $5.4 \text{ GeV}/c$ electrons, with no corrections applied (top) and after readout scheme and time walk corrections (bottom). The conversion to charge is obtained by applying the procedure discussed in Sec. 7.3.7.

The timing resolution was estimated by measuring the output signal coincidence of two DPTS using a $5.4 \text{ GeV}/c$ electron beam. The trigger signal and thus the time reference is given by the scintillators signal (cf. Fig. 7.15).

Figure 7.19 (top), shows the correlation of the signal arrival time and ToT, i.e. signal amplitude, for one of the two DPTS chips. The influence of the chip readout scheme on the signal time response is notable at high ToT, where the distribution

splits into two tails which correspond to odd and even columns (cf. Sec. 7.2.2). The correction for this effect is applied by subtracting the asymptotic value of the two tails from even and odd columns, respectively. The time walk observed for the lower input amplitude is corrected by fitting the data with the empirical function

$$\text{Signal time} = A + \frac{B}{ToT - C}, \quad (7.2)$$

where A , B and C are fit parameters, and then subtracting its value from the measured data points. The signal (arrival) time vs ToT correlation corrected for the chip readout scheme and the time walk is shown in Fig. 7.19 (bottom). As intended, it can be observed that the amplitude of the time walk is reduced by a factor of about 3 and its asymmetric feature is removed. The correlation between the amplitude of the time walk and the time-over-threshold remains but was not further investigated in this study.

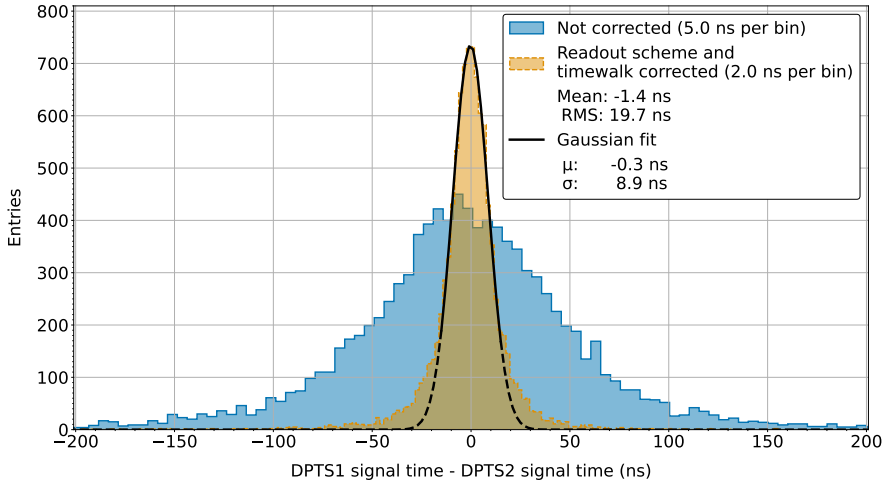


Figure 7.20 Time residuals distributions of two DPTSs measured with 5.4 GeV/ c electrons with no corrections (blue) and with readout scheme and time walk corrections applied (orange). The corrected distribution is fitted with a Gaussian function in the time residuals range from -15 ns to 15 ns (black solid line, dashed line for points outside the fit range).

The distribution of time residuals, i.e. the time differences of the output of the two DPTSs is shown in Fig. 7.20 for non-corrected data (in blue) and with corrections discussed above applied independently for the two DPTSs (in orange). The timing resolution of a single DPTS is obtained by fitting the distribution with a Gaussian, and the fit parameter σ is divided by $\sqrt{2}$, resulting in $\sigma_t = 6.3 \text{ ns} \pm 0.1 \text{ ns (stat)}$. It is worth highlighting that this result is obtained by operating the chips at the low end of the

in-pixel front-end power consumption range (i.e. nominal conditions in Sec. 7.3.1). An improvement in timing performances is expected by increasing the front-end current, namely I_{bias} and I_{biasn} .

7.5 Conclusions

Laboratory and in-beam measurements have been used to systematically validate the charge detection and radiation hardness of the Digital Pixel Test Structure MAPS prototype submitted in the TPSCo 65 nm process. The front end has shown a robust performance that can maintain a suitable operation regime in terms of threshold spread, noise and fake-hit rate. In addition to measuring the ToT response from X-ray emissions of an ^{55}Fe source, the DPTS achieved a resolution of $7.40\% \pm 0.02\%$ for the Mn-K_α peak. The impact of irradiation on the performance becomes evident at $1 \times 10^{15} \text{ 1 MeV } n_{\text{eq}} \text{ cm}^{-2}$; however, the sensor is still able to effectively detect the X-ray emissions. This demonstration of the radiation hardness is reinforced further by the excellent detection efficiency of 99% and spatial resolution below the binary resolution for chip irradiation doses compatible with the ITS3 requirements ($10^{13} \text{ 1 MeV } n_{\text{eq}} \text{ cm}^{-2}$ and 10 kGy) as well as to doses above these levels at $1 \times 10^{15} \text{ 1 MeV } n_{\text{eq}} \text{ cm}^{-2}$ and 100 kGy at $+20^\circ\text{C}$ while preserving a fake-hit rate below $10 \text{ pixel}^{-1} \text{ s}^{-1}$. The DPTS also demonstrates a timing resolution of about 6 ns for the nominal chip bias settings, with improvements expected if operated at conditions optimised for timing performance.

The first step to validate this sensor technology has been presented and makes up an important aspect of the R&D for the ALICE ITS3 as well as a significant contribution to the CERN EP R&D on monolithic sensors. The excellent performance of the DPTS opens the way for further developments in this technology and with this sensor design. The next step towards a wafer-scale bent sensor and a fully cylindrical detector is the validation of stitching and yield via the full-scale sensor prototypes produced in the second submission in the 65 nm process, designated ER1.

Further work to investigate the limit of the radiation hardness of this technology and probe the performance of the DPTS with ionising particles at non-zero incident angles is foreseen. Moreover, the front-end operating point is being tuned to optimise the power consumption for low power applications, such as ALICE ITS3, where high radiation hardness and fast timing response are not crucial requirements.

Acknowledgements

The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF). We would like to thank the coordinators at DESY for their valuable support of this testbeam measurement and for the excellent testbeam environment.

P. Becht acknowledges the support by the HighRR research training group [GRK 2058] and funding by the German Federal Ministry of Education and Research/BMBF (project number 05H21VHRD1) within the High-D consortium.

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This work has been sponsored by the Wolfgang Gentner Programme of the German Federal Ministry of Education and Research (grant no. 13E18CHA).

7.6 Summary and discussion

The Digital Pixel Test Structure is a versatile prototype allowing the evaluation of the TPSCo 65 nm modified with gap CMOS process for High-Energy Physics applications. Furthermore, the studies carried out with the DPTS validate the performance of a novel in-pixel front-end circuit architecture and the reliability of a distributed, asynchronous, time-based encoding readout scheme. Both the designs of the analog front-end and the readout logic are proofs of concept in view of an application to wafer-scale pixel sensors targeted by the ITS3 upgrade (cf. Section 1.6.1). The in-pixel front-end can be operated with a power density down to 12 mW cm^{-2} , well below the limit of 20 mW cm^{-2} envisaged by the ITS3, while the readout scheme allows to group the output of a large number of pixels (the whole matrix in the case of the DPTS) into a single digital line. Although the signal decoding is performed off-chip for the structure presented in this chapter, with all the limitations related to the dependence of the time encoding on temperature, supply and reverse bias, a fully integrated device including on-chip TDCs and buffer memories can be developed. In particular, such a device would require a limited number of TDCs, with noticeable reduction in power consumption, as many pixels can be readout with a single digital line. Further details on the design of the analog front-end and the digital readout can be found in Reference [16] and Reference [17], respectively.

The paper included in this chapter focuses on the characterization of the DPTS prototype to validate the properties of the TPSCo 65 nm modified with gap CMOS process for High-Energy Physics applications. The measurements performed with a minimum ionizing particle beam demonstrate full detection efficiency at the temperature of $+20^\circ\text{C}$, even after irradiation up to $1 \times 10^{15} \text{ 1 MeV n}_{\text{eq}} \text{ cm}^{-2}$, where, despite the degraded performance, 99% efficiency is achieved. The DPTS shows also a better spatial resolution than what a purely binary sensor with the same pixel pitch would achieve, with no notable effect of radiation damage on this figure. Finally, a time resolution of $6.3 \pm 0.1 \text{ ns}$ is measured for a non-irradiated sensor⁴ operated with an in-pixel front-end power consumption regime of about 50 mW cm^{-2} , i.e. 120 nW/pixel . This last result, especially if compared with what is measured for the APTS-OA (cf. Chapter 5), highlights the effect of the in-pixel front-end on the timing performance of a pixel sensor. Given that the modified with gap version of the APTS-OA and the DPTS pixel structures are identical, except for the pixel pitch ($10 \mu\text{m}$ versus $15 \mu\text{m}$, respectively), it is legitimate to expect a contribution of the order of 100 ps, or below, to

⁴ The quoted number refers to the standard deviation retrieved from the Gaussian fit of the corrected time residual distribution (cf. Figure 7.20).

the time resolution of the DPTS coming from the terms strictly related to the sensor (cf. Section 2.8), negligible with respect to what is measured. The discrepancy in temporal resolution between the APTS-OA and the DPTS sensors is therefore attributable to pixel-to-pixel fluctuations, as for the timing studies discussed in the paper the pixels of the measured DPTS devices are not individually calibrated, and to the jitter introduced by the in-pixel analog front-end. In particular, as shown in Reference [16], the latter heavily depends on the circuit operation regime. Measurements with charge injection via test pulses show evidence of a time jitter of the order of 30 ns for a power consumption of 12 nW/pixel, which reduces to about 3 ns at 120 nW/pixel (i.e. the operation regime adopted for the measurements presented in the paper), and about 1 ns at 600 nW/pixel, when the injected charge is of the order of $500 e^-$, i.e. the most probable cluster charge value measured for a modified with gap TPSCo 65 nm CMOS process (cf. Section 4.10). An optimization is therefore crucial not only on the sensor layout aspects, but also on the design of the in-pixel front-end if fast timing applications are targeted.

Nonetheless, the results achieved with the DPTS fully validate the 65 nm CMOS technology satisfying the ITS3 requirements, and make such a technology a promising option for particle physics experiments where higher radiation loads are expected.

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PART III

Closure

*“If we want things to stay as they are,
things will have to change.”*

Giuseppe Tomasi di Lampedusa, *The Leopard*

CHAPTER 8

Perspectives and future work

THE results achieved with the small scale MAPS prototypes belonging to the MLR1 submission qualify the TPSCo 65 nm CMOS imaging process as a promising technology for future applications in High-Energy Physics experiments. This dissertation focuses on the investigation of the potential of the new sensor technology, with particular interest towards its application for the ALICE experiment. However, other R&D challenges are present in the field of monolithic sensors.

The ALICE ITS3 upgrade targets the production of a large scale sensor (of the order of $30\text{ cm} \times 10\text{ cm}$) to be thinned and bent for a lightweight and self-supported barrel layer. Therefore, the collaboration conducts dedicated R&D and design efforts, in parallel with the evaluation of the 65 nm CMOS technology.

The feasibility of operating bent MAPS while preserving their electrical properties has been studied with the ALPIDE chip and a beam test campaign with bent sensors has demonstrated no loss of detection performance [1].

Besides the benefits of a smaller feature size and improved detection performance resulting from the process modifications, the adoption of the TPSCo 65 nm CMOS process offers the possibility of accessing wafers of 300 mm to produce large scale sensors. The stitching technology provides a method to manufacture ultra-large pixel matrix image sensor by repeating many stitching blocks and overcome the limit set by the size of the typical exposure of the photolithographic equipment, or reticle, used in a standard CMOS process, which is of the order of $2\text{ cm} \times 3\text{ cm}$ [2]. Two stitched sensor prototypes were designed and fabricated in a first engineering run ER1, submitted at the end of 2022. They are called *MOSS* and *MOST*, and are available for testing and characterization since summer 2023. They both comprise 10 repeated stitched units, and measure $14\text{ mm} \times 259\text{ mm}$ and $2.5\text{ mm} \times 259\text{ mm}$, respectively. These two sensors represent the first demonstration of wafer-scale CMOS MAPS developed for

High-Energy Physics applications. The first tests focused on the assessment of the production yield and the validation of the stitching technology. A full characterization aiming at the evaluation of the electrical and detection performance with minimum ionizing particle beam [3] of the prototypes is currently ongoing.

The production of the first ITS3 sensor prototype is planned with the second engineering run ER2, which will be submitted to the foundry in the first half of 2025.

The advancements in the production of wafer-size sensors, combined with the full qualification of the TPSCo 65 nm CMOS imaging process, pose a very promising basis towards a successful installation and operation of the ALICE ITS3 detector during the LHC Run 4.

The small scale prototypes discussed in this thesis show encouraging results also in view of performing precise time measurements with monolithic sensors based on a 65 nm CMOS process. In particular, the results obtained with the APTS-OA chip demonstrate that sensors implementing such a technology can achieve a time resolution down 63 ps. Nonetheless, different approaches to achieve fast timing with monolithic sensors are possible. Some examples are represented by the small-scale chip prototypes produced within the *ARCADIA* and *MONOLITH* projects. The first one aims at developing fully depleted MAPS based on the Lfoundry 110 nm CMOS technology to reach 20 ps resolution for the ALICE3 Time-of-Flight detector. To achieve such a challenging timing performance, the sensor includes an internal gain layer to perform charge multiplication, similar to charge multiplication layers used in LGADs. Preliminary results show a time resolution of 70 ps with a gain of about 13 [4, 5]. The *MONOLITH* approach relies instead on a 130 nm process featuring Silicon-Germanium (SiGe) Heterojunction Bipolar Transistors operating at cut-off frequencies which are not reached by CMOS processes adopted in High-Energy Physics. Such an implementation demonstrated to achieve 20 ps resolution at full efficiency [6–8], which can be further improved to 11.5 ps if a gain layer is embedded in the sensor, in a similar fashion to the *ARCADIA* approach [9, 10].

High-resistivity MAPS with small collection electrode have proved to be superlative tracking sensors thanks to their low material, combined with full detection efficiency and excellent spatial resolution at reduced power consumption. The synergy between the High-Energy Physics community and semiconductor foundries, driven by the market of consumer imaging application for visible light, gives access to advanced CMOS processes and has allowed the development of devices which have already demonstrated high radiation tolerance and fast timing capabilities, which are no longer limiting factors for monolithic devices. This context offers a very optimistic perspective for the development of and application of MAPS to future collider experiments.

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Summary

THE infinite quest towards a more complete understanding of nature and its fundamental building blocks relies on the development of increasingly advanced instrumentation capable of testing theoretical models. In Particle Physics, a crucial role is played by particle accelerators and detectors, which allow to accelerate and collide particles under controlled conditions, and to study their properties, respectively. The Large Hadron Collider (LHC) [1], the largest existing particle accelerator complex of the world located at CERN, accelerates protons and heavy ions to collide them in four interaction points, around which four detectors are built. These are operated by the ATLAS, CMS, ALICE and LHCb experiments with the goal of investigating the Standard Model of Particle Physics [2] and looking for hints of additional symmetries or new forces or constituents beyond the Standard Model itself.

The four detectors, although specifically conceived to study distinct aspects or phenomena of Particle Physics, share common design concepts. The innermost subsystems, called tracking detectors and responsible for the reconstruction of the trajectories of the particles emerging from a collision or a decay, are made of several layers of silicon detectors. Because of their high spatial resolution and granularity, these devices have become the instrument of choice for the measurement and reconstruction of tracks emerging from a collision. The pointing resolution of a tracking detector, namely the uncertainty with which a collision or decay point is reconstructed, depends on three main parameters: the intrinsic spatial resolution of the sensor, the distance between the measurement point and the interaction point, and the amount of material in the detector. In particular, the ALICE experiment has the goal to investigate the properties of the quark-gluon plasma, a deconfined state of quarks and gluons [3]. An effective study of such a state of matter requires the capability to precisely reconstruct the track of low momentum particles (down to 100 MeV/ c for pions) emerging from a collision. For such a reason, the collaboration has decided to cover the seven layers

of its tracking detector, called Inner Tracking System 2, with monolithic active pixel sensors (MAPS). This technology integrates both sensor and readout electronics on the same silicon die, allowing the manufacturing of devices featuring small pixels and reduced amount of material, capable to achieve excellent tracking efficiency and impact parameter resolution even with low momentum particles.

To access and study new physics phenomena, the LHC complex will be upgraded [4] in the period July 2026-July 2030 with the final goal of increasing the collision rate at the interaction points. This will allow the experiments to more easily collect highly significant data sets to study rare process but will pose, at the same time, new challenges to the detectors. The increase in track multiplicity and radiation load will require tracking detectors to improve their pointing resolution and resistance to radiation damage. Moreover, the capability to measure the particle interaction time with ps resolution can boost the particle identification via Time-of-Flight measurements and can be combined with the measurement of spatial coordinates to resolve the increased number of (quasi-) simultaneous collisions with a method called 4D tracking [5].

In view of the LHC upgrade, the ALICE collaboration is conducting an intense R&D program aiming at the development of the next generation of monolithic sensors for Particle Physics experiments. For the upgrade of the ALICE Inner Tracking System 3 (ITS3), the collaboration is evaluating the TPSCo 65 nm CMOS Image Sensor technology for the manufacturing of the new ALICE sensors. MLR1 is the first chip submission adopting a 65 nm CMOS process for MAPS in High-Energy Physics applications. It was produced in summer 2021 and includes circuit prototypes, transistor test structures and small pixel matrix test chips to test the potential of the new technology.

The APTS-OA is an analog test structure designed to study the properties of the pixel sensor design. It features a matrix of 6×6 squared pixels with $10\text{ }\mu\text{m}$ pitch implementing an operational amplifier-based analog front-end output buffer to directly access their signals and study the timing properties of the technology. The APTS-OA prototypes present three diverse pixel designs: one based on a typical CMOS process for imaging sensors, also known as standard process, and two based on process optimizations aimed at enhancing the detection properties with charged particles, namely the modified and modified with gap processes. The cross section of the three pixel variants are shown in Figure S1. All the three pixel designs are based on a high-purity p-type silicon epitaxial layer of $10\text{ }\mu\text{m}$ nominal thickness grown on top of a p-type substrate. The sensing electrode is an n-type silicon well placed in the center of the pixel. The modified processes add an n-type silicon blanket below the collection electrode to allow full depletion of the epitaxial layer when reverse bias

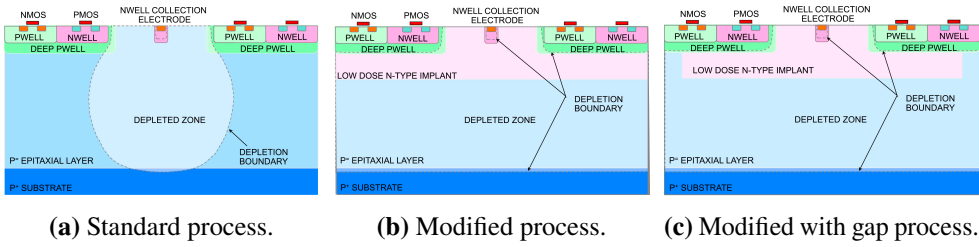


Figure S1 Pixel sensor variants implemented in the MLR1 submission: a) Standard; b) Modified; c) Modified with gap. Not to scale. Figures taken from Reference [7].

voltage is applied. In particular, the modified with gap process introduces a cut at the edges of the blanket to increase the lateral component of the electric field, with subsequent improvement of the charge collection speed and uniformity [6].

The investigation of the properties of the three pixel variants is conducted with measurements of charge injection via test pulses or X-rays emitted by a ^{55}Fe radioactive source. The latter emits photons from two modes, with energy of 5.9 keV and 6.5 keV, respectively, which can be used to calibrate the sensor's response. Figure S2 shows the ^{55}Fe seed pixel spectra of three APTS-OA devices based on the different processes operated at -2.4 V reverse bias voltage. The seed pixel is the pixel of the matrix producing the largest amplitude signal. The signal spectra are expressed in equivalent charge, with the voltage to charge conversion performed by identifying the position of

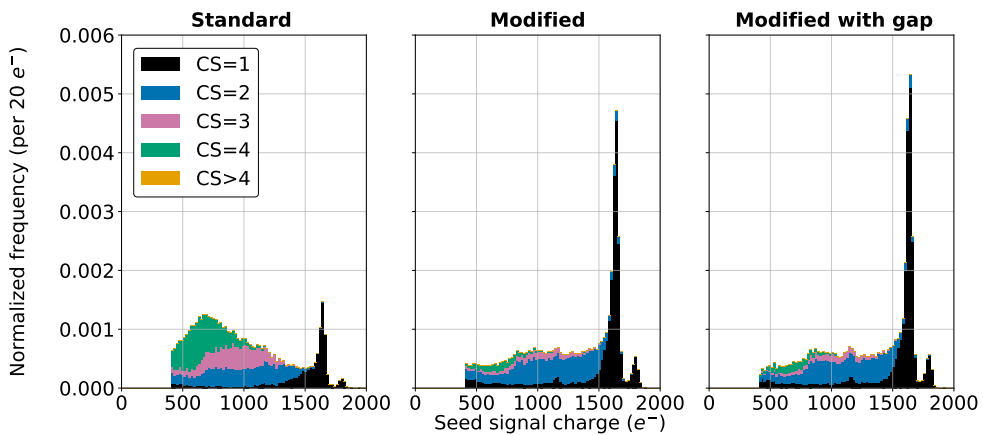


Figure S2 Comparison of seed signal ^{55}Fe charge spectra as a function of cluster size (CS, indicated with different colors) for the three different APTS-OA pixel layout variants measured at constant reverse substrate voltage $V_{\text{sub}} = -2.4$ V.

the peaks in the spectrum, knowing that they correspond to the full collection of the charge generated after the absorption of the photon. In Figure S2, the contribution to the seed signal charge given by clusters of different size is highlighted. A cluster is defined as a group of neighboring pixels inside a 3×3 matrix centered around the seed, which have a signal above a certain threshold. In the case of the APTS-OA, the threshold is set to an equivalent of $100 e^-$. The main difference between the standard process and the modified ones lays in the pronounced bump appearing between $500 e^-$ and $900 e^-$, known as charge sharing peak. It is due to the photoelectric conversion happening in a non-depleted region of the epitaxial layer. In this case, the generated charge can easily be shared among neighboring pixels via thermal diffusion. The modified processes are instead characterized by prominent charge collection peaks corresponding to full absorption of the charge generated by the ^{55}Fe photons, hint of larger depleted volume and suppressed charge sharing. No major difference is observed between the modified and modified with gap processes for the $10 \mu\text{m}$ pixels studied.

The experimental characterization of the APTS-OA prototypes is completed with a beam test campaign, aiming at studying the response of the sensors to minimum ionizing particles. The experimental setup includes a Low Gain Avalanche Detector (LGAD) used as a time reference for the reconstructed tracks to measure the time resolution of the APTS-OA [8]. Such a measurement is performed by computing the difference between the time when the APTS-OA seed pixel reaches 10% of its full amplitude and the time reference provided by the LGAD, defined as the time when the signal leading edge reaches 40% of its amplitude. The distribution of the time residuals, namely the difference between the APTS-OA signal times and the time reference, is defined as:

$$\Delta t = t_{10\%}^{\text{APTS-OA}} - t_{40\%}^{\text{LGAD}}.$$

The signal times are measured at a given amplitude fraction to reduce the dependence of the time residuals on the signal charge. Figure S3 shows the time residual distribution measured for an APTS-OA sample implementing the modified with gap process operated with -4.8 V reverse bias voltage. The blue distribution is obtained by applying the definition given above, the orange results after having corrected for the dependence of the time residuals on the signal charge and on the in-pixel track hit position. The correction requires a high statistical significance data set to be effective. The time resolution can be finally calculated by quadratically subtracting the 30 ps time resolution of the LGAD from the time residuals width, expressed as the Root Mean Square (RMS) of the distribution or the standard deviation σ of a Gaussian fit.

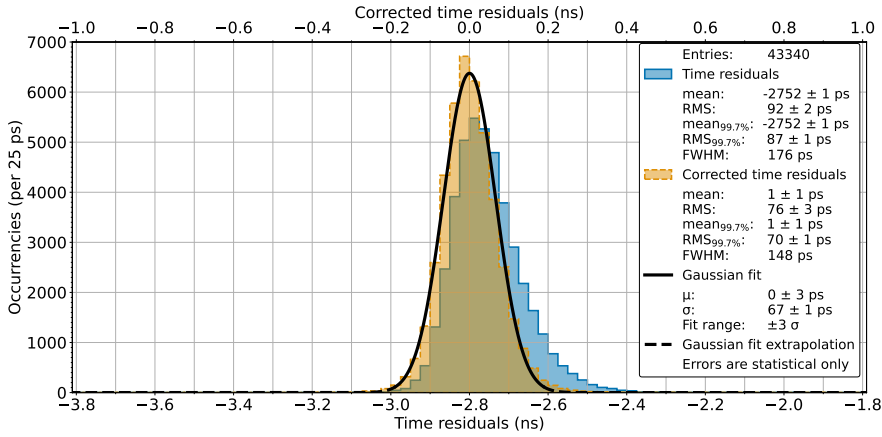


Figure S3 Time residuals measured for an APTS-OA sensor implementing the modified with gap process operated at -4.8 V reverse bias voltage, before (blue distribution, bottom horizontal axis) and after (orange distribution, top horizontal axis) correction of the dependence of the signal time on the signal charge and in-pixel track hit position. The corrected distribution is fitted with a Gaussian function on a range of $\pm 3\sigma$ (black solid line, dashed line for points outside the fit range). Figure taken from Reference [8] .

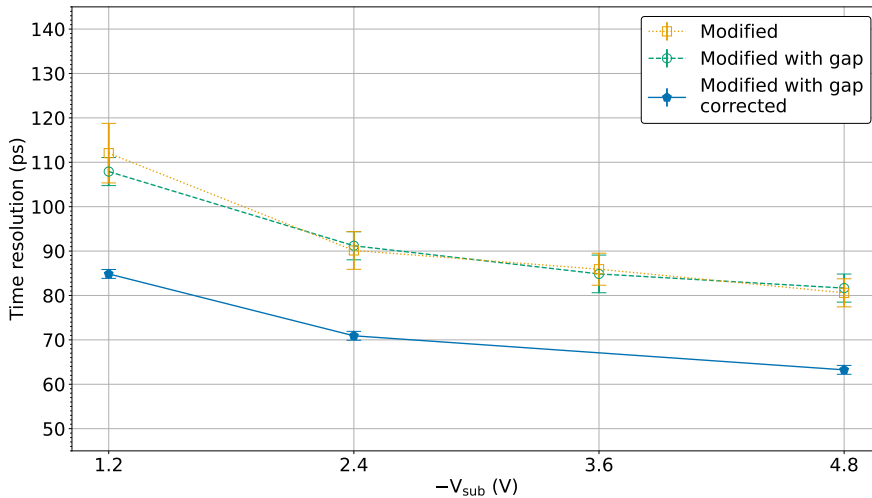


Figure S4 Non-corrected (open symbols, orange dotted line and green dashed line) and corrected (full symbols, blue solid line) time resolution measured for modified and modified with gap APTS-OA sensor variants operated at varying reverse bias voltage. The correction is applied only to high statistical significance data sets, namely those measured with the modified with gap structure. Figure taken from Reference [8].

Figure S4 shows the dependence of the time resolution on the applied reverse bias voltage for both a modified and a modified with gap sample. As already observed with ^{55}Fe measurements, no meaningful difference emerges between the two process variants for the studied $10\text{ }\mu\text{m}$ pixel pitch sensors. For a modified with gap pixel variant operated with -4.8 V reverse bias voltage, a time resolution of 82 ps before correction and 63 ps after correction is measured.

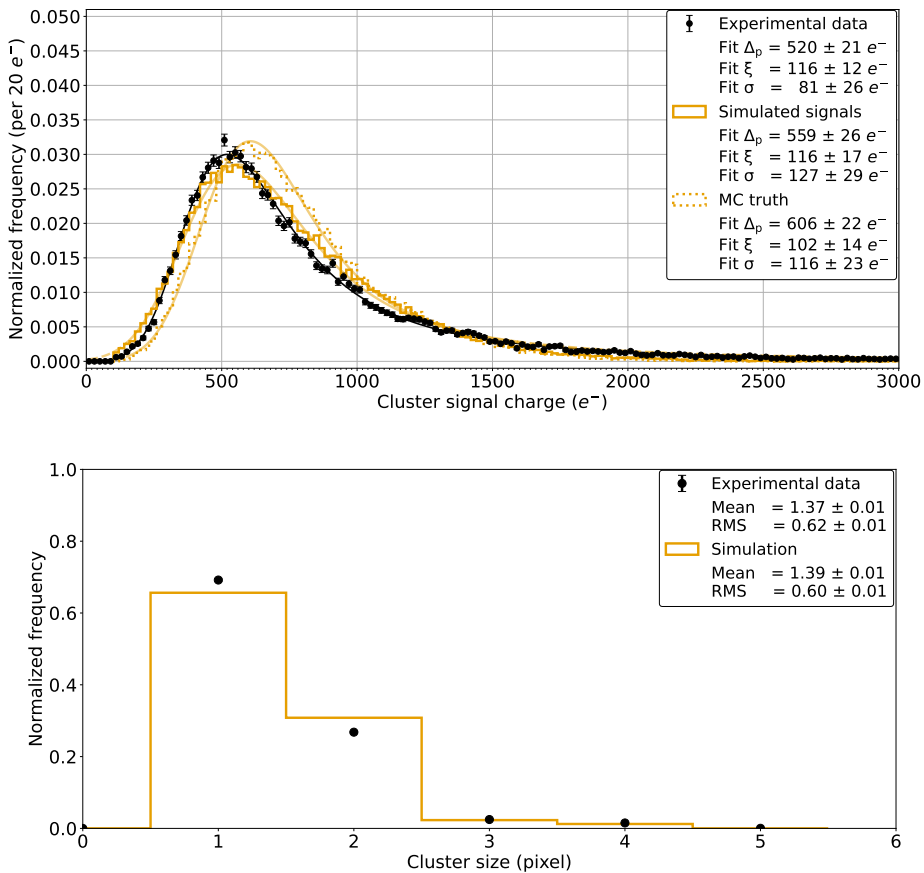
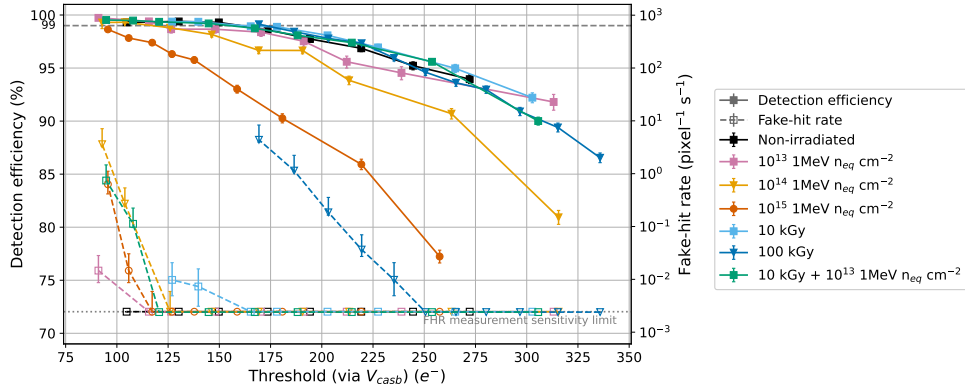


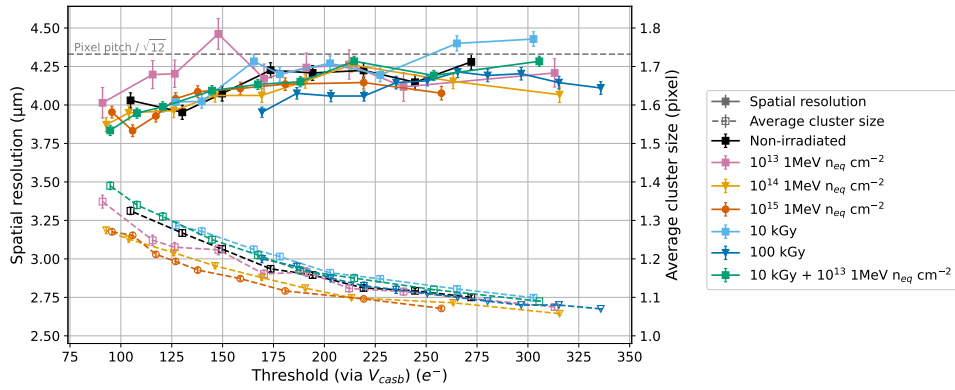
Figure S5 Comparison of the experimental (in black) and simulated (in orange) cluster charge (top panel) and cluster size (bottom panel) distributions APTS-OA matrix operated at -4.8 V reverse bias voltage and traversed by a minimum ionizing particle beam. For the cluster signal, both the distributions resulting from the analysis of the simulated signals (solid line) and from the MC truth information (dashed line) are depicted. All the three distributions are fitted with a Langaus function.

The experimental study of the APTS-OA prototypes allows to assess the potential of monolithic pixel sensors based on a 65 nm CMOS technology and to evaluate the benefits of the process modification. At the same time, some physical properties, such as the electric field distribution or the contribution of the substrate to the amount of collected charge, are not immediately accessible through experimental investigation. To obtain a more complete understanding of the device physics, the behavior of MAPS implementing a 65 nm CMOS imaging process was simulated. The simulation is based on the combination of three-dimensional Synopsys Technology Aided Design (TCAD) models [9] and Monte Carlo simulations performed with the Allpix² framework [10]. The former describe and evaluate the electrical properties of the sensor, while the latter simulate the signal formation at the output channel of a pixel. These two tools are combined to model the behavior of an APTS-OA sensor traversed by minimum ionizing particles, and the simulation is validated by directly comparing its output with experimental data. A precise model of the APTS-OA would require, however, the knowledge of the details of the TPSCo 65 nm CMOS process. These are not available, since the process is covered by non-disclosure agreement with the foundry. The simulation is therefore developed on the basis of the known features of the sensor layouts, combined with approximated doping profiles. The doping profiles implemented in the simulation are therefore iteratively adjusted on the basis of the comparison with experimental results in view of a more realistic description of the sensor behavior. Figure S5 shows the comparison of simulated and experimental cluster signal charge and cluster size for a modified with gap APTS-OA sensor operated with -4.8 V reverse bias. A good agreement in charge collection observables is found if the simulation considers a highly doped substrate and a thick interface between substrate and epitaxial layer due to the high temperatures to which the sensor is subjected during the CMOS manufacturing process [11], which results in an epitaxial layer effectively thinner than $10\text{ }\mu\text{m}$. While the simulation is able to satisfactorily describe the charge collection observables, some optimization is needed to match the experimental timing observables. Upon full validation, this simulation workflow can be used as a design tool to predict the performance of new sensor designs based on the TPSCo 65 nm CMOS process.

The DPTS is the most complex test structure belonging to the MLR1 submission. It consists of a matrix of 32×32 squared pixels with $15\text{ }\mu\text{m}$ pitch, all implementing the modified with gap process. The chip features a complete readout chain, consisting of a per pixel analog front-end with discriminator and a global, fully asynchronous, digital readout designed to read out multiple pixels at the same time. The prototype is characterized with laboratory tests and with minimum ionizing charged particle



(a) Detection efficiency and fake-hit rate.



(b) Spatial resolution and average cluster size.

Figure S6 Performance of several DPTS chips, irradiated and non-irradiated, operated with -2.4 V reverse bias voltage and measured with 10 GeV/ c positive hadrons as a function of average threshold: a) Detection efficiency (filled symbols, solid lines) and fake-hit rate (open symbols, dashed lines); b) Spatial resolution (filled symbols, solid lines) and average cluster size (open symbols, dashed lines). Figures taken from Reference [12].

beam measurements. Figure S6a and Figure S6b show the detection efficiency and fake-hit rate, and spatial resolution and average cluster size, respectively, as a function of the average threshold for several DPTS chips irradiated at various ionizing doses and non-ionizing fluences traversed by 10 GeV/ c positive hadrons, all operated with -2.4 V reverse bias voltage at the temperature of 20°C . The 100 kGy irradiated sensor suffers from significant increase in the fake-hit rate, while the 1×10^{15} 1 MeV n_{eq} cm $^{-2}$

irradiated sensor, despite showing notable performance deterioration, can still be operated at 99% efficiency. Regardless of the irradiation level, the measured spatial resolution is equal or better than the binary one, with no degradation due to the radiation damage.

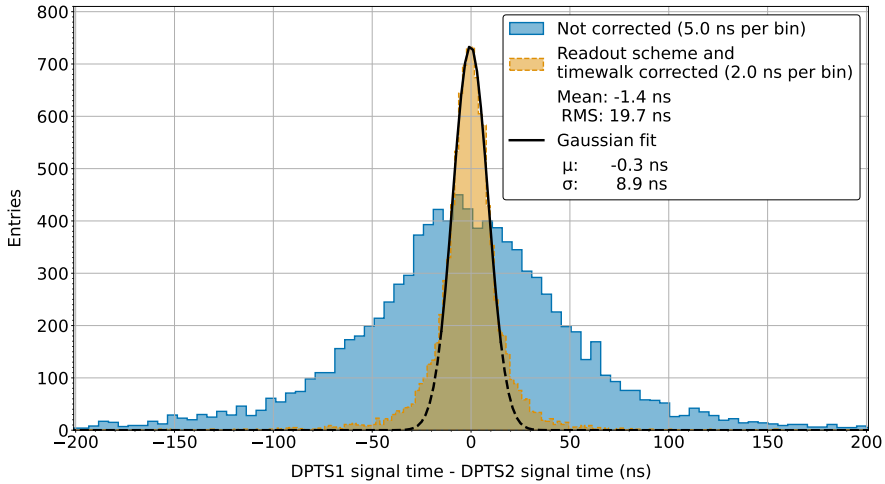


Figure S7 Time residuals distributions of two DPTS chips measured with 5.4 GeV/ c electrons with no corrections (blue) and with readout scheme and time walk corrections applied (orange). The corrected distribution is fitted with a Gaussian function in the time residuals range from -15 ns to 15 ns (black solid line, dashed line for points outside the fit range). Figure taken from Reference [12].

The time resolution is evaluated by measuring the difference between the signal times of two DPTS chips crossed by a 5.4 GeV/ c electron beam. The distribution of the time residuals is shown in Figure S7 for non-corrected data (in blue) and with corrections to compensate the influence of the chip readout and of the signal charge on the signal time response. The corrected distribution is fitted with a Gaussian function, with the parameter σ divided by $\sqrt{2}$ giving the time resolution of a single device equal to 6.3 ns. With respect to the APTS-OA, such a result includes, besides the resolution of the sensing part, the contribution of the in-pixel analog front-end and digital readout operated at low power consumption regime.

The results obtained with the test structures belonging to the MLR1 submission enforce MAPS based on a 65 nm CMOS technology as strong candidates for particle tracking in future High-Energy Physics applications. Full detection efficiency and excellent spatial resolution are proven even after significant radiation damage when operated at 20 °C. The process modification allows to reach a time resolution down

to 63 ps for the sensing part, which combined with an optimized design in terms of readout electronics, paves the way for future developments to establish MAPS as a fast timing technology.

The evolution of Particle Physics and the advancement of technology and instrumentation are mutually dependent. In this context, the synergy between the High-Energy Physics community and semiconductor foundries, proven by the development of a new generation of sensors for Particle Physics experiments based on a commercial technology, offers optimistic perspectives towards the achievement of more and more challenging goals.

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Samenvatting[†]

DE oneindige zoektocht naar een volledig begrip van de natuur en haar fundamentele bouwstenen is afhankelijk van de ontwikkeling van steeds geavanceerdere instrumentatie die in staat is theoretische modellen te testen. In de deeltjesfysica spelen deeltjesversnellers en detectoren een cruciale rol, omdat zij het mogelijk maken om deeltjes onder gecontroleerde omstandigheden te versnellen en te laten botsen, en respectievelijk hun eigenschappen te bestuderen. De Large Hadron Collider (LHC) [1], het grootste bestaande deeltjesversnellingscomplex ter wereld, gelegen bij CERN, versnelt protonen en zware ionen om ze te laten botsen in vier interactiepunten, waar omheen vier detectoren zijn gebouwd. Deze worden geëxploiteerd door de ATLAS-, CMS-, ALICE- en LHCb-experimenten met als doel het Standaardmodel van de deeltjesfysica [2] te onderzoeken en op zoek te gaan naar aanwijzingen voor aanvullende symmetrieën, nieuwe krachten of deeltjes voorbij het Standaardmodel.

De vier detectoren, hoewel specifiek ontworpen om verschillende aspecten of verschijnselen van de deeltjesfysica te bestuderen, delen gemeenschappelijke ontwerpconcepten. De binnenste subsystemen, genaamd trackingdetectoren en verantwoordelijk voor het reconstrueren van de trajecten van de deeltjes die uit een botsing of verval voortkomen, bestaan uit verschillende lagen silicium detectoren. Vanwege hun hoge ruimtelijke resolutie en granulariteit zijn deze apparaten uitgegroeid tot het instrument bij uitstek voor de meting en reconstructie van de sporen die uit een botsing voortkomen. De zogenoemde pointing resolution van een trackingdetector, oftewel de onzekerheid waarmee een bots- of vervalpunt wordt gereconstrueerd, is afhankelijk van drie hoofdparameters: de intrinsieke ruimtelijke resolutie van de sensor, de afstand tussen het meetpunt en het interactiepunt, en de hoeveelheid materiaal in de detector. In het bijzonder heeft het ALICE-experiment als doel de eigenschappen van het quark-gluon-plasma te onderzoeken, een gedeconfinerde toestand van quarks en gluonen [3].

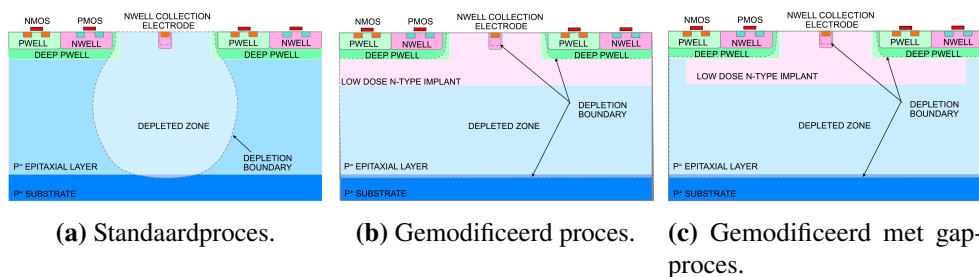
[†]Text generated by translating the Summary with ChatGPT and later revised.

Een effectieve studie van een dergelijke materietoestand vereist de mogelijkheid om het spoor van deeltjes met een lage impuls (tot 100 MeV/c voor pionen) die uit een botsing voortkomen nauwkeurig te reconstrueren. Om die reden heeft de collaboratie besloten om de zeven lagen van haar trackingdetector, genaamd Inner Tracking System 2, te bekleden met monolithische actieve pixel sensoren (MAPS). Deze technologie integreert zowel de sensor als de uitleeselektronica op dezelfde siliciumchip, waardoor apparaten met kleine pixels en een verminderde hoeveelheid materiaal geproduceerd kunnen worden, die in staat zijn een uitstekende trackingefficiëntie en impactparameter-resolutie te bereiken, zelfs met deeltjes met een lage impuls.

Om nieuwe fysische verschijnselen te onderzoeken, zal het LHC-complex worden gemoderniseerd [4] in de periode Juli 2026–Juli 2030 met als einddoel het aantalbotsingen per seconde op de interactiepunten te verhogen. Dit zal de experimenten in staat stellen om gemakkelijker zeer significante datasets te verzamelen om zeldzame processen te bestuderen, maar zal tegelijkertijd nieuwe uitdagingen voor de detectoren met zich meebrengen. De toename in het aantal sporen en de stralingsbelasting zal vereisen dat trackingdetectoren hun pointing resolution verbeteren en dat ze beter bestand zijn tegen stralingsschade. Bovendien kan de mogelijkheid om de interactietijd van de deeltjes met een resolutie in de orde van ps te meten de deeltjesidentificatie via Time-of-Flight-metingen verbeteren, en kan dit worden gecombineerd met de meting van ruimtelijke coördinaten om het toegenomen aantal (bijna) gelijktijdige botsingen uit elkaar te houden met een methode die 4D-tracking wordt genoemd [5].

Gezien de LHC-upgrade voert de ALICE-collaboratie een intensief R&D-programma uit gericht op de ontwikkeling van de volgende generatie monolithische sensoren voor de deeltjesfysica-experimenten. Voor de upgrade van het ALICE Inner Tracking System 3 (ITS3) evalueert de collaboratie de TPSCo 65 nm CMOS Image Sensor-technologie voor de productie van de nieuwe ALICE-sensoren. MLR1 is de eerste chipinzending die een 65 nm CMOS-proces gebruikt voor MAPS toepassingen in de hoge-energetische deeltjesfysica. Deze werd in de zomer van 2021 geproduceerd en omvat circuitprototypes, transistor-teststructuren en kleine pixelmatrix-testchips om het potentieel van de nieuwe technologie te testen.

De APTS-OA is een analoge teststructuur ontworpen om de eigenschappen van het pixel sensordesign te bestuderen. Het bevat een matrix van 6×6 vierkante pixels met een pitch van 10 μm en elk een op een operationele versterker gebaseerde analoge front-end outputbuffer om direct toegang te krijgen tot hun signalen en om de timing-eigenschappen van de technologie te bestuderen. De APTS-OA-prototypes presenteren drie diverse pixelontwerpen: één gebaseerd op een typisch CMOS-proces voor beeldsensoren, ook wel het standaardproces genoemd, en twee gebaseerd op



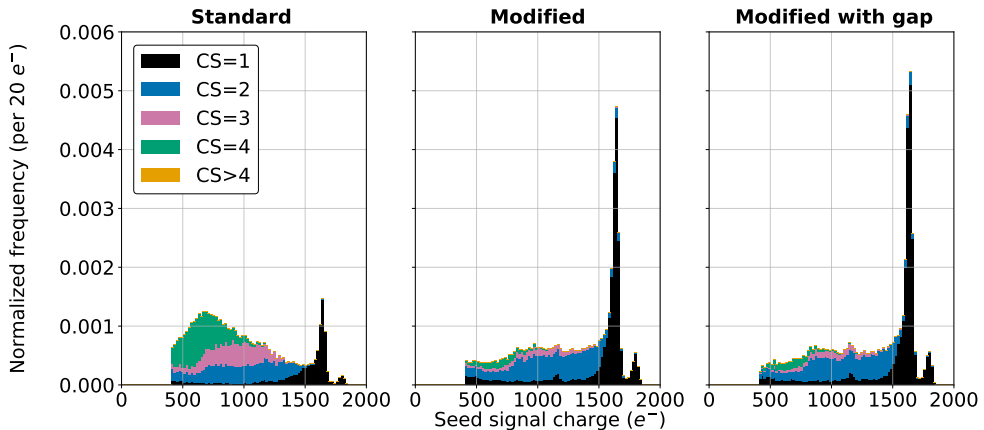
Figuur S1 Pixel sensormodellen geïmplementeerd in de MLR1 inzending: a) Standaard (Standard); b) Gemodificeerd (Modified); c) Gemodificeerd met gap (Modified with gap). Niet op schaal. Figuren overgenomen uit Referentie [7].

procesoptimalisaties die gericht zijn op het verbeteren van de detectie-eigenschappen met geladen deeltjes, namelijk de 'modified' en 'modified with gap'-processen. De dwarsdoorsnede van de drie pixelvarianten wordt getoond in Figuur S1. Alle drie de pixelontwerpen zijn gebaseerd op een hoogzuivere p-type silicium epitaxiale laag met een nominale dikte van $10\text{ }\mu\text{m}$ die bovenop een p-type substraat is gegroeid. De sensor-elektrode is een zogenaamde n-type silicium well in het midden van de pixel. De gemodificeerde processen voegen een n-type siliciumdeken toe onder de verzamel-elektrode om een volledige verarming van de epitaxiale laag te verkrijgen wanneer een omgekeerde spanning wordt aangelegd. In het bijzonder introduceert het 'modified with gap'-proces een uitsparing aan de randen van de deken om de laterale component van het elektrische veld te verhogen, met als gevolg een verbetering van de snelheid en uniformiteit van de ladingverzameling [6].

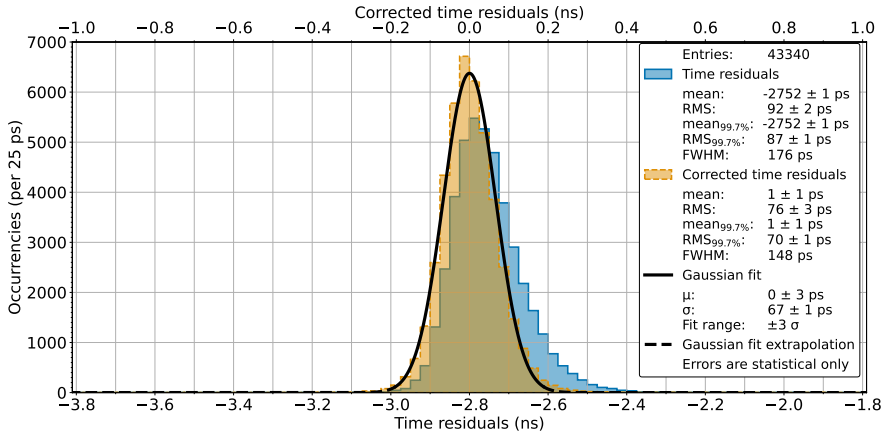
De studie van de eigenschappen van de drie pixelvarianten wordt uitgevoerd door metingen van ladingsinjectie via testpulsen of röntgenstraling uitgezonden door een ^{55}Fe radioactieve bron. De laatste zendt fotonen uit in twee modi, met een energie van 5.9 keV en 6.5 keV respectievelijk, welke kunnen worden gebruikt om de respons van de sensor te kalibreren. Figuur S2 toont de ^{55}Fe seedpixel-spectra van drie APTS-OA apparaten gebaseerd op de verschillende processen, in gebruik bij een omgekeerde bias-spanning van -2.4 V . De seedpixel is de pixel in de matrix die het grootste signaal qua amplitude produceert. De signaalspectra worden uitgedrukt in equivalente lading, waarbij de omzetting van spanning naar lading wordt uitgevoerd door de positie van de pieken in het spectrum te identificeren, in de wetenschap dat deze overeenkomen met de volledige verzameling van de lading die wordt gegenereerd na absorptie van het foton. Figuur S2 laat de bijdrage aan de seedsignaallading, gegeven door clusters van verschillende grootte zien. Een cluster wordt gedefinieerd als een groep aangrenzende

pixels binnen een 3×3 matrix gecentreerd rond de seedpixel, die een signaal boven een bepaalde drempelwaarde hebben. In het geval van de APTS-OA is de drempel ingesteld op een equivalent van $100 e^-$. Het voornaamste verschil tussen het standaardproces en de gemodificeerde processen ligt in de uitgesproken piek die verschijnt tussen $500 e^-$ en $900 e^-$, bekend als de ladingsdelingspiek. Deze piek ontstaat door de foto-elektrische conversie die plaatsvindt in een niet-verarmd gebied van de epitaxiale laag. In dit geval kan de gegenereerde lading gemakkelijk worden gedeeld tussen aangrenzende pixels via thermische diffusie. De gemodificeerde processen daarentegen worden gekenmerkt door prominente ladingsverzamelingspieken die overeenkomen met de volledige absorptie van de door de ^{55}Fe fotonen gegenereerde lading, wat wijst op een groter verarmd volume en verminderde ladingsdeling. Er wordt geen significant verschil waargenomen tussen het gemodificeerde en het gemodificeerde met gap-proces voor de bestudeerde $10 \mu\text{m}$ pixels.

De experimentele karakterisatie van de APTS-OA prototypes wordt afgerond met een test bundel campagne, gericht op het bestuderen van de respons van de sensoren op minimum ioniserende deeltjes. De experimentele opstelling omvat een Low Gain Avalanche Detector (LGAD) die wordt gebruikt als tijdsreferentie voor de gereconstrueerde sporen, om zo de tijdsresolutie van de APTS-OA te meten [8]. Een dergelijke meting wordt uitgevoerd door het verschil te berekenen tussen de tijd waarop de APTS-OA-seedpixel 10% van zijn volledige amplitude bereikt en de tijdsreferentie



Figuur S2 Vergelijking van de seedsignaal ^{55}Fe ladingsspectra als functie van de clustergrootte (CS, aangegeven met verschillende kleuren) voor de drie verschillende APTS-OA pixel layoutvarianten, gemeten bij een constante omgekeerde substraatspanning $V_{\text{sub}} = -2.4 \text{ V}$.

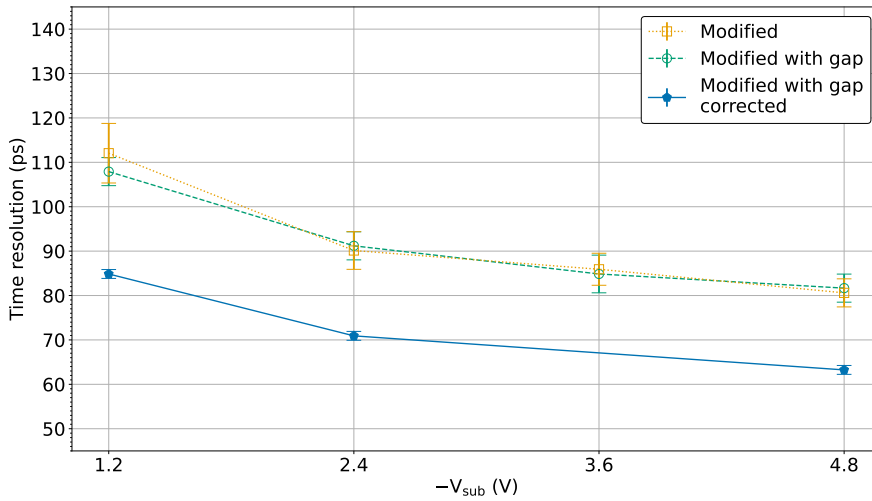


Figuur S3 Tijdresiduen gemeten voor een APTS-OA sensor die het 'modified with gap'-proces implementeert en bediend wordt met een omgekeerde bias-spanning van -4.8 V, vóór (blauwe distributie, onderste horizontale as) en na (oranje distributie, bovenste horizontale as) correctie van de afhankelijkheid van de signaaltijd van de signaallading en de in-pixel spoortrefferpositie. De gecorrigeerde distributie is gefit met een Gaussiaanse functie over een bereik van $\pm 3\sigma$ (zwarte doorgetrokken lijn, stippellijn voor punten buiten het fitbereik). Figuur overgenomen uit Referentie [8].

geleverd door de LGAD, gedefinieerd als de tijd waarop de stijgende flank van het signaal 40% van zijn amplitude bereikt. De distributie van de tijdresiduen, oftewel het verschil tussen de signaaltijd van de APTS-OA en de tijdsreferentie, wordt gedefinieerd als:

$$\Delta t = t_{10\%}^{\text{APTS-OA}} - t_{40\%}^{\text{LGAD}}.$$

De signaaltijden worden gemeten bij een gegeven amplitudefractie om de afhankelijkheid van de tijdresiduen van de signaallading te verminderen. Figuur S3 toont de tijdresiduen-distributie gemeten voor een APTS-OA-prototype dat het 'modified with gap'-proces implementeert en in gebruik is met een omgekeerde bias-spanning van -4.8 V. De blauwe distributie wordt verkregen door de hierboven gegeven definitie toe te passen, de oranje distributie na correctie voor de afhankelijkheid van de tijdresiduen van de signaallading en de in-pixel hit or track hit positie. De correctie vereist een dataset met hoge statistische significantie om effectief te zijn. De tijdresolutie kan uiteindelijk worden berekend door de 30 ps tijdresolutie van de LGAD in kwadratuur af te trekken van de breedte van de distributie van tijdresiduen, uitgedrukt als de Root Mean Square (RMS) van de distributie of de standaarddeviatie σ van een Gaussiaanse fit.

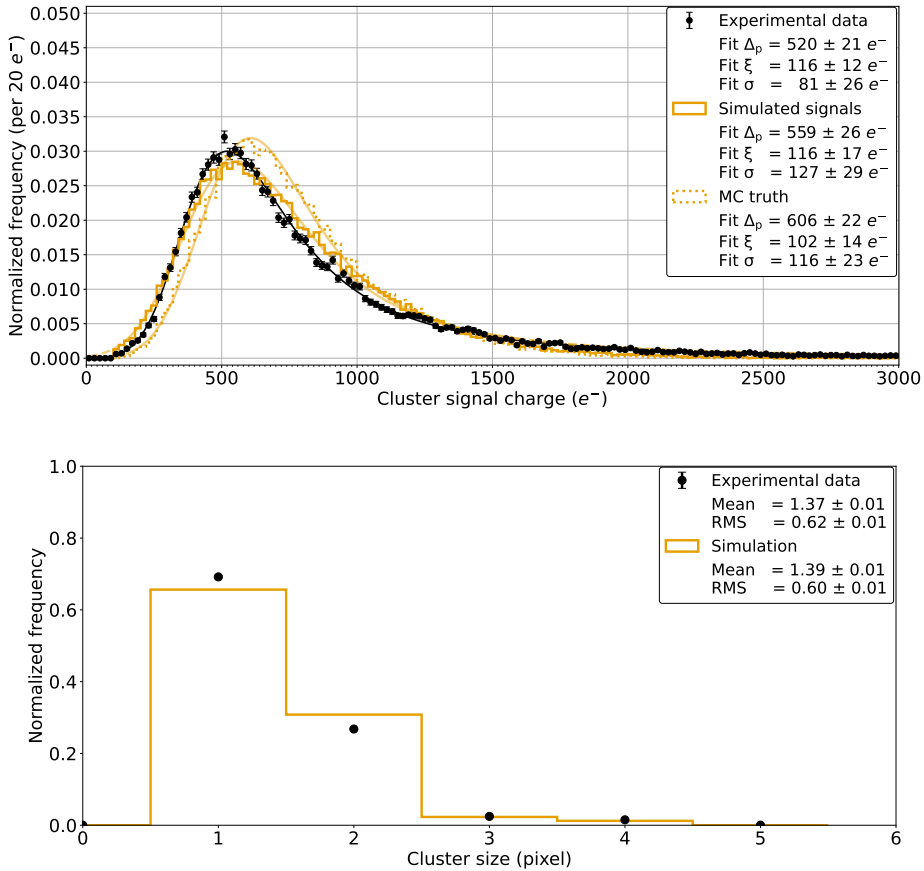


Figuur S4 Niet-gecorrigeerde (open symbolen, oranje stippellijn en groene gestippelde lijn) en gecorrigeerde (gevulde symbolen, blauwe doorgetrokken lijn) tijdresolutie gemeten voor de APTS-OA sensorvarianten 'modified' en 'modified with gap', in gebruik bij variërende omgekeerde spanningen. De correctie wordt alleen toegepast op datasets met hoge statistische significantie, namelijk die gemeten met de 'modified with gap'-structuur. Figuur overgenomen uit Referentie [8].

Figuur S4 toont de afhankelijkheid van de tijdresolutie van de aangelegde omgekeerde biasspanning voor zowel een 'modified'- als een 'modified with gap'-prototype. Zoals al eerder waargenomen bij ^{55}Fe -metingen, komt er geen betekenisvol verschil naar voren tussen de twee procesvarianten voor de bestudeerde $10\ \mu\text{m}$ pixelpitch-sensoren. Voor een 'modified with gap'-pixelvariant in gebruik bij een omgekeerde spanning van $-4.8\ \text{V}$, wordt een tijdresolutie van $82\ \text{ps}$ vóór correctie en $63\ \text{ps}$ na correctie gemeten.

De experimentele studie van de APTS-OA prototypes maakt het mogelijk om het potentieel van monolithische pixelsensoren op basis van een $65\ \text{nm}$ CMOS-technologie te beoordelen en de voordelen van de procesmodificatie te evalueren. Tegelijkertijd zijn sommige fysische eigenschappen, zoals de verdeling van het elektrische veld of de bijdrage van het substraat aan de verzamelde lading, niet direct toegankelijk via experimentele methoden. Om een volledig begrip van de fysica van de sensor te verkrijgen, is het gedrag van MAPS die een $65\ \text{nm}$ CMOS beeldproces implementeren gesimuleerd. De simulatie is gebaseerd op de combinatie van driedimensionale Synopsys Technology Computer Aided Design (TCAD) modellen [9] en Monte Carlo-simulaties uitgevoerd met het Allpix² framework [10]. De eerste beschrijft en evalueert de elektrische eigenschappen van de sensor, terwijl de tweede de signalvorming op

het uitgangskanaal van een pixel simuleert. Deze twee tools worden gecombineerd om het gedrag van een APTS-OA sensor, doorkruist door minimum ioniserende deeltjes, te modelleren, en de simulatie wordt gevalideerd door de uitkomsten direct te vergelijken met experimentele data. Een nauwkeurig model van de APTS-OA zou echter kennis vereisen van de details van het TPSCo 65 nm CMOS-proces. Deze details zijn niet

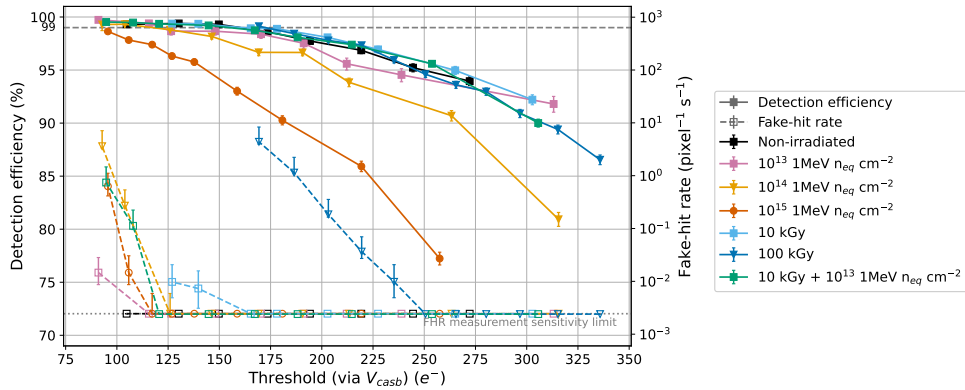


Figuur S5 Vergelijking van de experimentele (in zwart) en gesimuleerde (in oranje) distributies van clustersignaal (bovenste paneel) en clustergrootte (onderste paneel) voor een APTS-OA matrix, in gebruik bij een omgekeerde spanning van -4.8 V en doorkruist van een minimum ioniserende deeltjesbundel. Voor het clustersignaal worden zowel de distributies uit de analyse van de gesimuleerde signalen (doorgetrokken lijn) als de MC-truth informatie (gestippelde lijn) weergegeven. Alle drie de distributies worden gefit met een Langauss-functie.

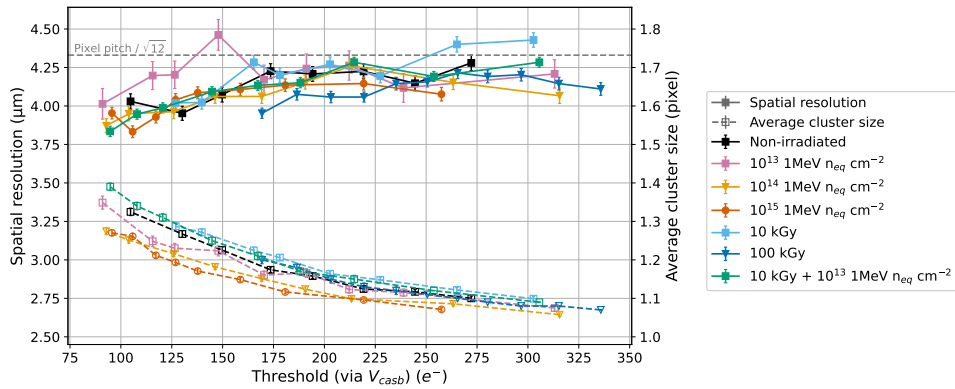
beschikbaar omdat het proces wordt beschermd door een geheimhoudingsverklaring met de foundry. De simulatie is daarom ontwikkeld op basis van de bekende kenmerken van de sensorlayouts, gecombineerd met een benadering van dopingsprofielen. De in de simulatie geïmplementeerde dopingsprofielen worden dan iteratief aangepast op basis van de vergelijking met experimentele resultaten, met als doel een realistischere beschrijving van het sensorgedrag. Figuur S5 toont de vergelijking van de gesimuleerde en experimentele distributies van clustersignaallading en clustergrootte voor een 'modified with gap' APTS-OA sensor, in gebruik bij -4.8 V omgekeerde spanning. Er is een goede overeenkomst in de ladingsverzamelingsobservabelen te vinden als de simulatie rekening houdt met een sterk gedopeerd substraat en een dikke interface tussen substraat en epitaxiale laag, als gevolg van de hoge temperaturen waaraan de sensor wordt blootgesteld tijdens het CMOS-productieproces [11], wat resulteert in een effectieve epitaxiale laag dunner dan $10\text{ }\mu\text{m}$. Hoewel de simulatie in staat is om de ladingsverzamelingsobservabelen naar behoren te beschrijven, is enige optimalisatie nodig om de experimentele timingobservabelen te matchen. Na volledige validatie kan deze simulatieworkflow worden gebruikt als ontwerptool om de prestaties van nieuwe sensorontwerpen op basis van het TPSCo 65 nm CMOS-proces te voorspellen.

De DPTS is de meest complexe teststructuur behorende bij de MLR1 inzending. Deze bestaat uit een matrix van 32×32 vierkante pixels met een pitch van $15\text{ }\mu\text{m}$, allemaal geïmplementeerd met het 'modified with gap'-proces. De chip bevat een volledige uitleesketen, bestaande uit een per-pixel analoog front-end met discriminator en een globale, volledig asynchrone digitale uitlezing, ontworpen om meerdere pixels tegelijk uit te lezen. Het prototype wordt gekarakteriseerd met laboratoriumtests en met metingen in een bundel van minimum ioniserende geladen deeltjes. Figuur S6a en Figuur S6b tonen respectievelijk de detectie-efficiëntie en het vals-positief-hitpercentage, de ruimtelijke resolutie en gemiddelde clustergrootte, als functie van de gemiddelde drempel voor diverse DPTS-chips die zijn bestraald met verschillende ioniserende doses en niet-ioniserende fluïenties, doorkruist door $10\text{ GeV}/c$ positieve hadronen, allen in gebruik bij -2.4 V omgekeerde spanning op een temperatuur van $20\text{ }^\circ\text{C}$. De sensor bestraald met 100 kGy ondervindt een significante toename in het vals-positief-hitpercentage, terwijl de sensor bestraald met $1 \times 10^{15}\text{ } 1\text{ MeV } n_{\text{eq}}\text{ cm}^{-2}$ ondanks een duidelijke prestatieverslechtering nog steeds met 99% efficiëntie kan worden bediend. Ongeacht het bestralingsniveau is de gemeten ruimtelijke resolutie gelijk aan of beter dan de binaire resolutie, zonder degradatie door stralingsschade.

De tijdresolutie wordt bepaald door het verschil te meten tussen de signaaltijden van twee DPTS-chips die door een $5.4\text{ GeV}/c$ elektronenbundel worden doorkruist. De



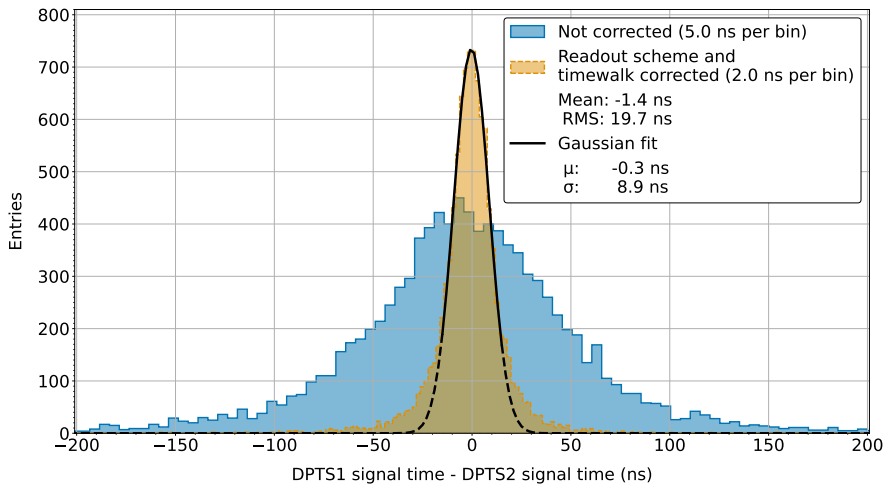
(a) Detectie-efficiëntie en vals-positief-trefferpercentage.



(b) Ruimtelijke resolutie en gemiddelde clustersize.

Figuur S6 Prestaties van diverse DPTS-chips, zowel bestraald als niet-bestraald, in gebruik met -2.4 V omgekeerde spanning en gemeten met $10 \text{ GeV}/c$ positieve hadronen als functie van de gemiddelde drempelwaarde: a) Detectie-efficiëntie (gevulde symbolen, doorgetrokken lijnen) en vals-positief-hitpercentage (open symbolen, stippellijnen); b) Ruimtelijke resolutie (gevulde symbolen, doorgetrokken lijnen) en gemiddelde clustergrootte (open symbolen, stippellijnen). Figuren overgenomen uit Referentie [12].

de distributie van de tijdsresiduen wordt getoond in Figuur S7 voor niet-gecorrigeerde data (in blauw) en na correcties om de invloed van het uitleesschema van de chip en van de signaallading op de tijdsrespons te compenseren. De gecorrigeerde distributie wordt gefit met een Gaussiaanse functie, waarbij de parameter σ gedeeld door $\sqrt{2}$ de tijdsresolutie van een enkel apparaat geeft, gelijk aan 6.3 ns . In vergelijking met de APTS-OA omvat een dergelijk resultaat, naast de resolutie van het sensoronderdeel,



Figuur S7 Distributies van tijdresiduen van twee DPTS-chips, gemeten met 5.4 GeV/c elektronen, zonder correcties (blauw) en met toegepaste correcties voor het uitleesschema en de timewalk (oranje). De gecorrigeerde distributie is gefit met een Gaussiaanse functie in het tijdresiduumbereik van -15 ns tot 15 ns (zwarte doorgetrokken lijn, stippellijn voor punten buiten het fitbereik). Figuur overgenomen uit Referentie [12].

ook de bijdrage van het in-pixel analoge front-end en digitale uitlezing, die in een modus met laag vermogen werken.

De resultaten verkregen met de teststructuren behorende bij de MLR1 inzending bevestigen dat MAPS op basis van een 65 nm CMOS-technologie sterke kandidaten zijn voor de deeltjestracking in toekomstige toepassingen in de hoge-energetische deeltjesfysica. Volledige detectie-efficiëntie en uitstekende ruimtelijke resolutie worden aangetoond, zelfs na aanzienlijke stralingsschade bij een temperatuur van 20°C . De procesmodificatie maakt het mogelijk om een tijdresolutie tot wel 63 ps voor het sensoronderdeel te bereiken, wat in combinatie met een geoptimaliseerd ontwerp van de uitleeselectronica de weg vrijmaakt voor toekomstige ontwikkelingen om MAPS te vestigen als een technologie voor snelle timing.

De evolutie van de deeltjesfysica en de vooruitgang in technologie en instrumentatie zijn wederzijds afhankelijk. In dit verband bieden de synergie tussen de deeltjesfysicagemeenschap en de halfgeleiderfoundries, aangetoond door de ontwikkeling van een nieuwe generatie sensoren voor deeltjesfysica-experimenten gebaseerd op een commerciële technologie, hoopvolle perspectieven richting het bereiken van steeds uitdagendere doelen.

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Appendix: additional figures

A Response of APTS-OA to ^{55}Fe X-rays

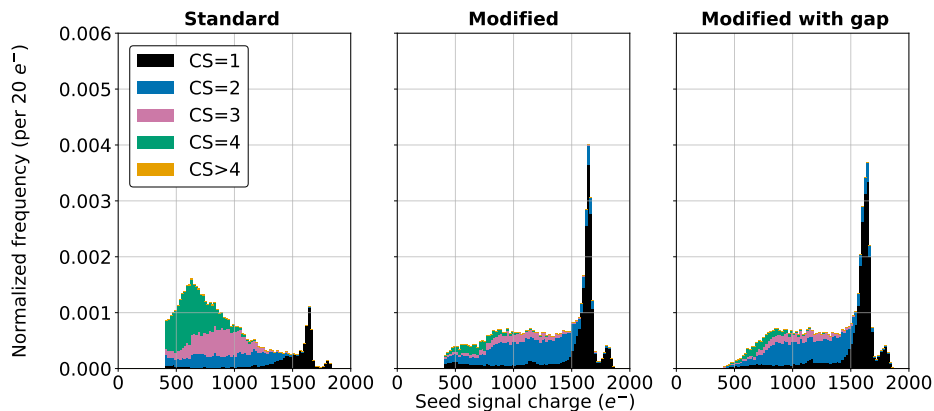


Figure A.1 Comparison of seed signal ^{55}Fe charge spectra as a function of cluster size (indicated with different colors) for the three different APTS-OA pixel layout variants measured at constant reverse substrate voltage $V_{\text{sub}} = -1.2$ V.

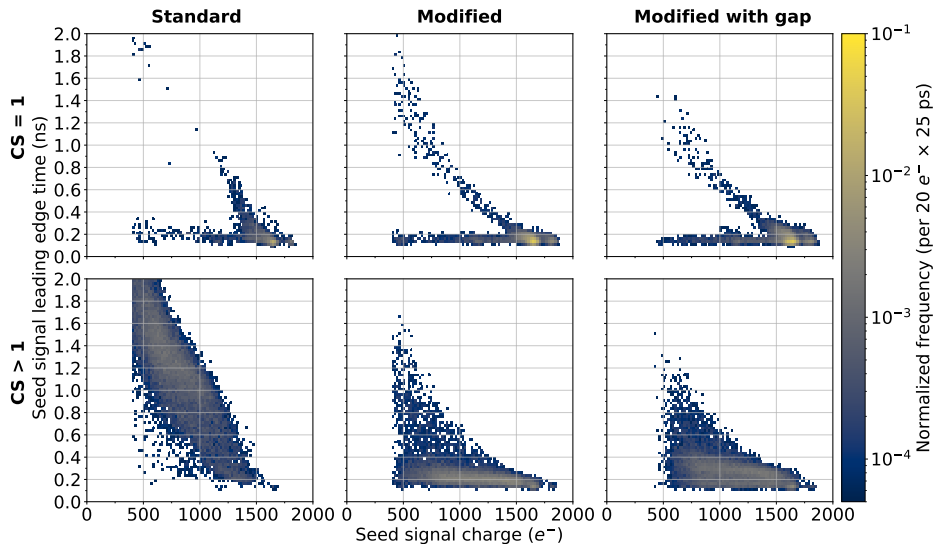


Figure A.2 Correlation of seed signal charge with seed signal leading edge time for single pixel clusters (CS = 1, top row) and clusters with pixel multiplicity larger than one (CS > 1, bottom row) measured with ^{55}Fe X-rays for the three different APTS-OA pixel layout variants operated at constant reverse substrate voltage $V_{\text{sub}} = -1.2$ V.

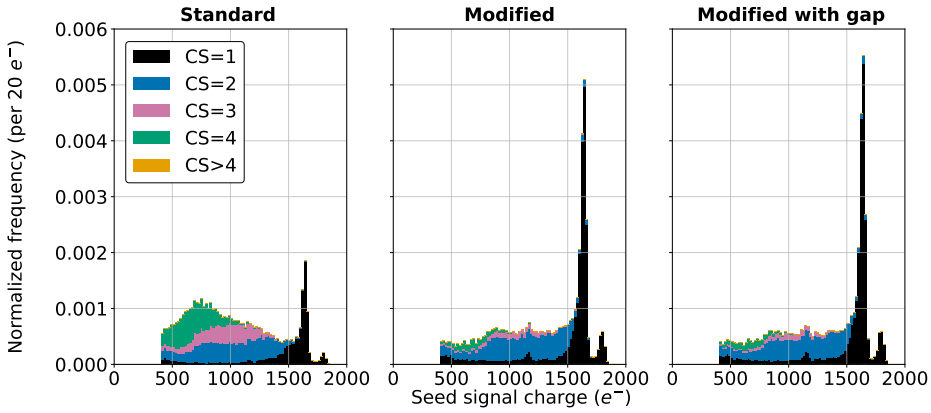


Figure A.3 Comparison of seed signal ^{55}Fe charge spectra as a function of cluster size (indicated with different colors) for the three different APTS-OA pixel layout variants measured at constant reverse substrate voltage $V_{\text{sub}} = -3.6 \text{ V}$.

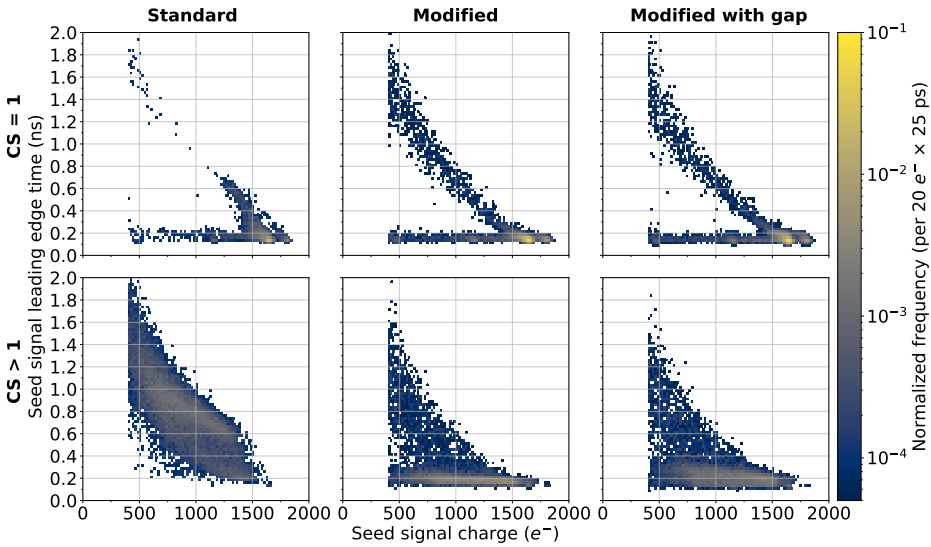


Figure A.4 Correlation of seed signal charge with seed signal leading edge time for single pixel clusters (CS = 1, top row) and clusters with pixel multiplicity larger than one (CS > 1, bottom row) measured with ^{55}Fe X-rays for the three different APTS-OA pixel layout variants operated at constant reverse substrate voltage $V_{\text{sub}} = -3.6 \text{ V}$.

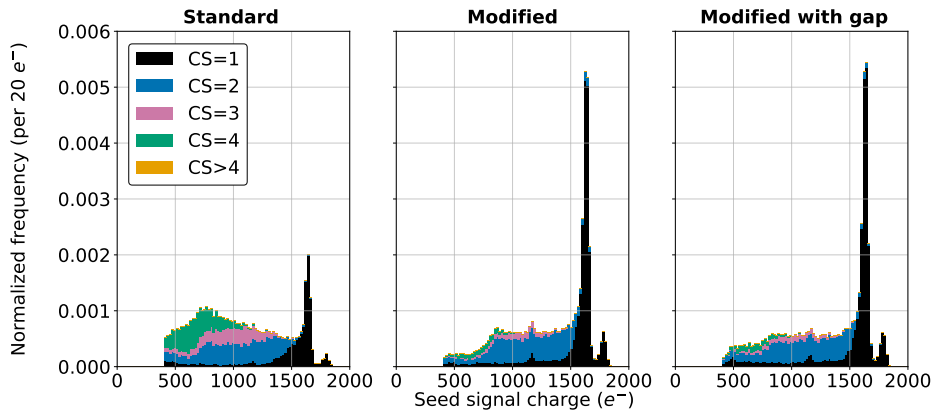


Figure A.5 Comparison of seed signal ^{55}Fe charge spectra as a function of cluster size (indicated with different colors) for the three different APTS-OA pixel layout variants measured at constant reverse substrate voltage $V_{\text{sub}} = -4.8$ V.

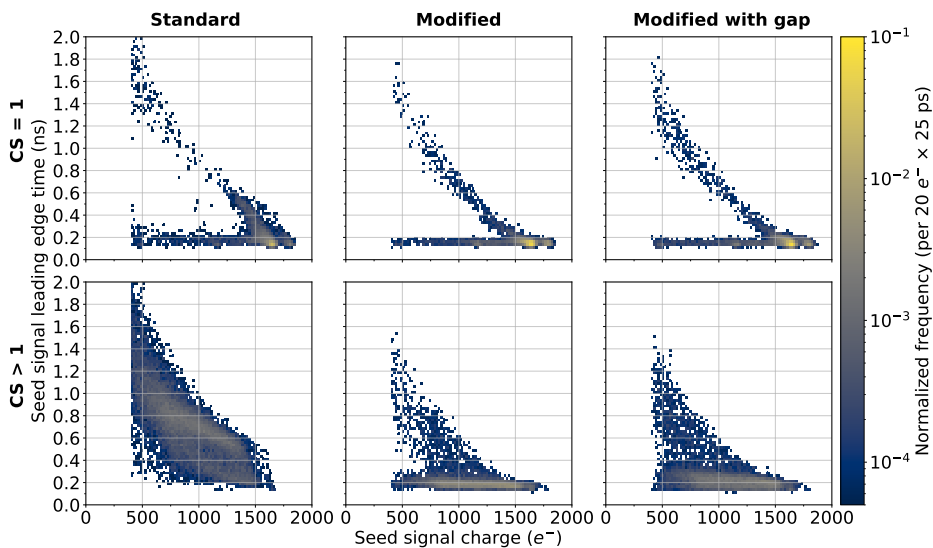


Figure A.6 Correlation of seed signal charge with seed signal leading edge time for single pixel clusters ($\text{CS} = 1$, top row) and clusters with pixel multiplicity larger than one ($\text{CS} > 1$, bottom row) measured with ^{55}Fe X-rays for the three different APTS-OA pixel layout variants operated at constant reverse substrate voltage $V_{\text{sub}} = -4.8$ V.

B APTS-OA analog front-end settings

The operating point used for measurements reported in this paper is summarized in the Table. B.1. The currents I_{reset} , I_{biasn} , I_{biasp} are shown in Fig. 5.3 while the biasing currents for the operational amplifier I_{bias3} , I_{bias4} , V_{casn} , and V_{casp} are not depicted in Figure. Finally, the value of V_{reset} chosen depending on V_{sub} in order to operate in the most linear region of the front-end is reported in Table B.2.

In-pixel	
I_{reset}	100 pA
I_{biasn}	-125 μA
I_{biasp}	11.25 μA
Out of pixel	
I_{bias3}	212.5 μA
I_{bias4}	2.6 mA
V_{casn}	900 mV
V_{casp}	270 mV

Table B.1 The operating point used for the measurement. See the details in Fig. 5.3.

V_{sub} (V)	-1.2	-2.4	-3.6	-4.8
V_{reset} (mV)	380	420	440	440

Table B.2 V_{reset} settings at different V_{sub}

C APTS-OA detection efficiency as a function of the threshold with different association window radius

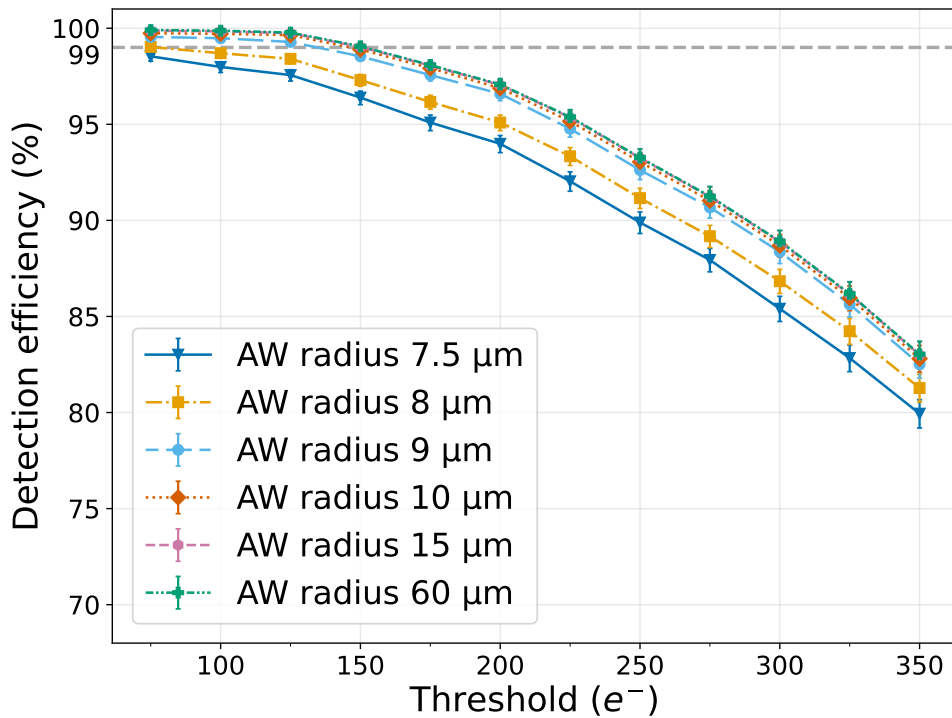


Figure C.1 Detection efficiency of the APTS-OA modified DUT as a function of the threshold at $V_{\text{sub}} = V_{\text{pwell}} = -1.2 \text{ V}$, varying the association window (AW) radius.

A study on the association window radius was conducted, starting with a value smaller than the pixel pitch and gradually increasing it to 60 μm . The detection efficiency improved with larger association windows across all thresholds. However, the difference in efficiency between the 15 μm and 60 μm radii was less than 0.05%. Consequently, an association window of 15 μm was selected for the analysis.

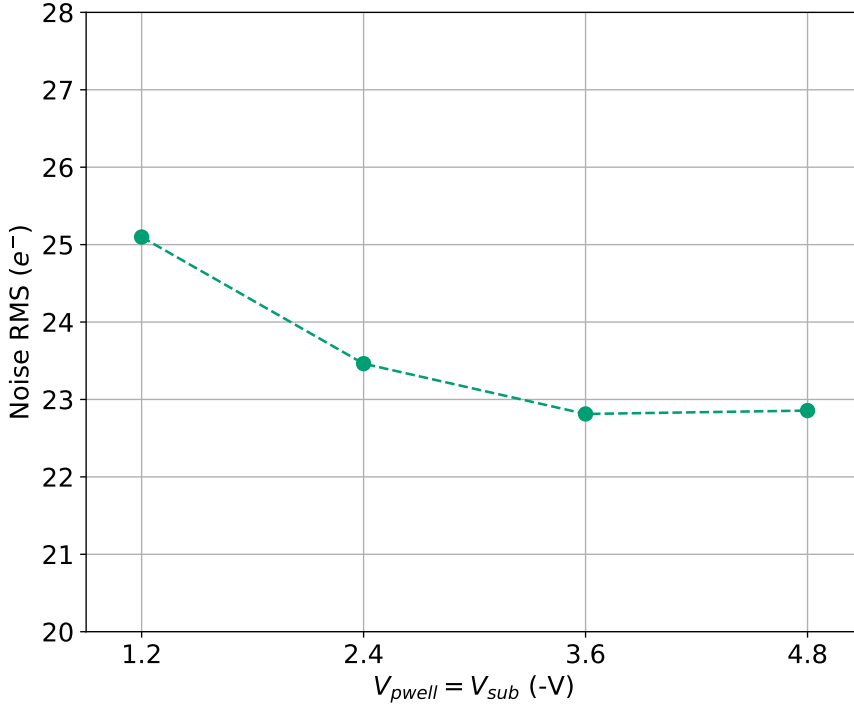
D APTS-OA noise

Figure D.1 Noise RMS of the APTS-OA modified with gap at different $V_{sub} = V_{pwell}$ configurations.

In order to show only results not biased by noise, an analysis of the baseline fluctuations was conducted and efficiency and spatial resolution were plotted for thresholds above 3 times the RMS of the noise distribution, shown in Fig. D.1.

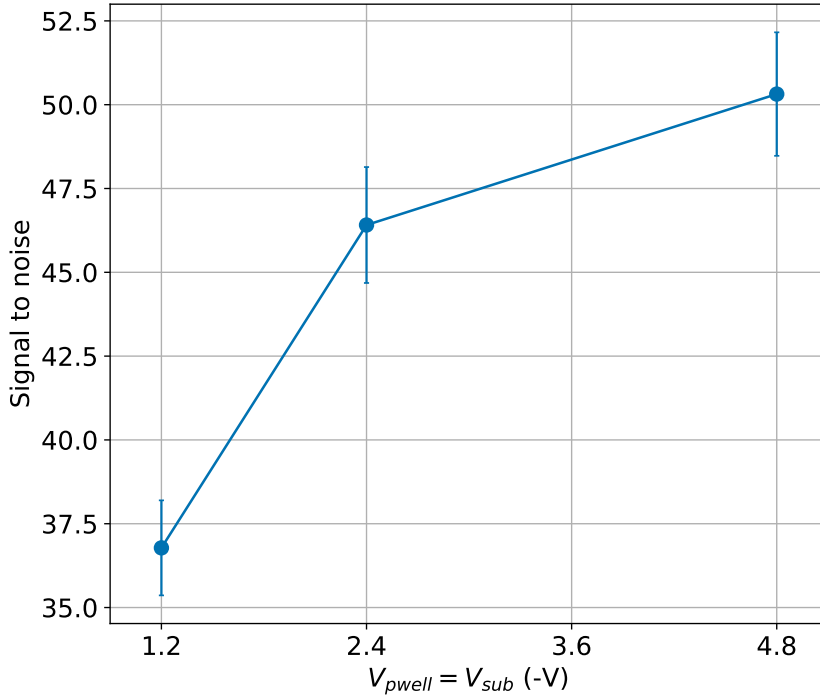


Figure D.2 Signal to noise of the APTS-OA modified with gap at different $V_{sub} = V_{pwell}$ configurations.

To complete the previous information, the signal to noise ratio (SNR) was calculated for the data samples with the highest statistics ($V_{sub} = V_{pwell} = -1.2, -2.4$ and -4.8 V) by fitting the cluster charge distribution with a Landau-Gauss function. The most probable value was used to calculate the SNR, shown in Fig. D.2.

E APTS-OA time residuals width at varying signal amplitude fraction

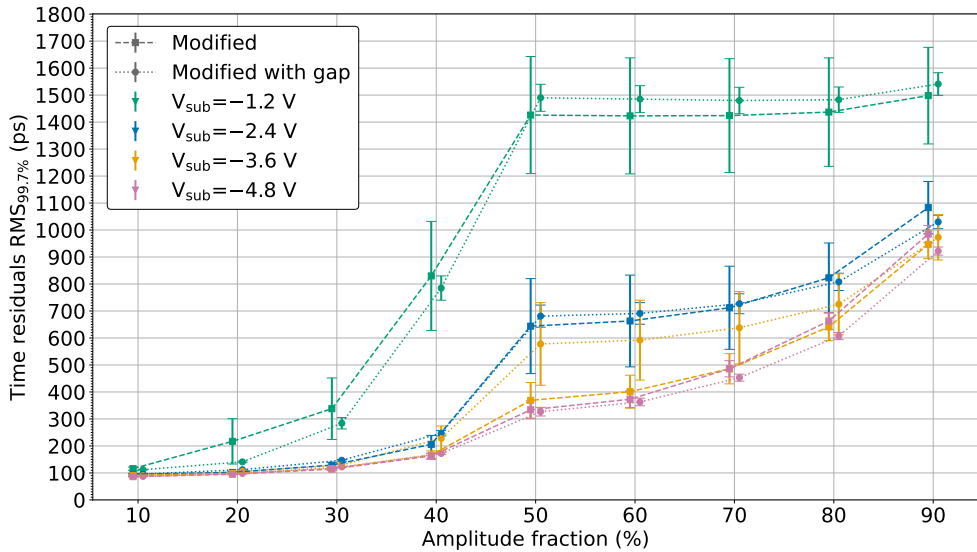


Figure E.1 Time residuals distribution width for APTS-OA DUTs' signal times measured at different fractions of the signal amplitude for each operation V_{sub} . The values pertaining to the modified process DUT are indicated with square markers and dashed lines, while those referring to the modified with gap process DUT with circle markers and dotted lines. A slight displacement in the x axis is added between the two curves to allow better visibility.

The time residuals width, expressed as the RMS of the 99.7 central percentiles of the distribution, has been evaluated for both measured DUTs at varying seed signal amplitude fraction. Signal times measured at 10% of the signal amplitude provide the lowest time residuals RMS, and are therefore used for the analysis presented in this paper.

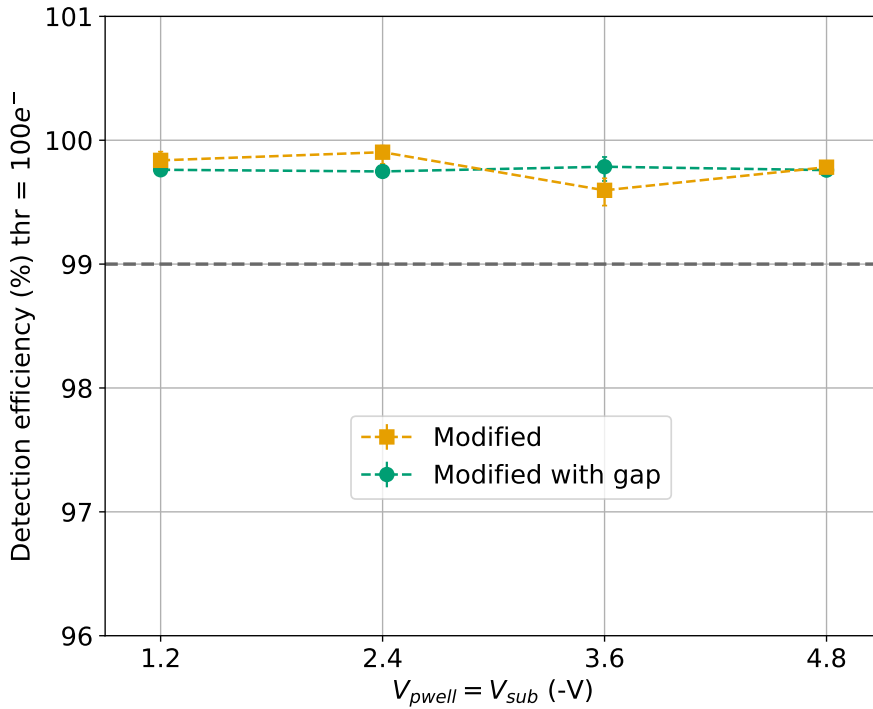
F APTS-OA detection efficiency at 100 e^- threshold

Figure F.1 Detection efficiency of the APTS-OA modified and modified with gap DUT at 100 e^- threshold at different $V_{sub} = V_{pwell}$ configurations.

Fig. F.1 compares the efficiency measured at 100 e^- threshold at different V_{sub} . No significant difference can be observed between the modified and modified with gap process variants and the efficiency is well above 99% for all the V_{sub} configurations.

G APTS-OA cluster size distributions

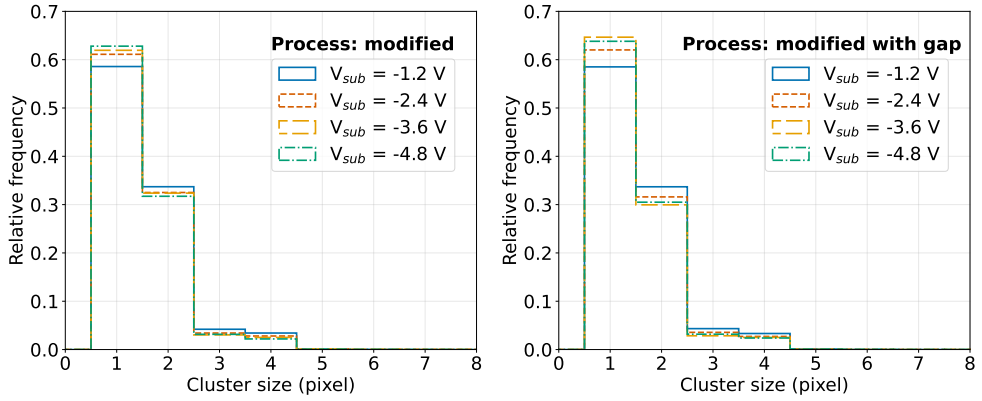


Figure G.1 Cluster size distribution of the APTS-OA modified and modified with gap DUT at 100 e^- threshold at different $V_{\text{sub}} = V_{\text{pwell}}$ configurations.

Fig. G.1 shows the cluster size distribution at 100 e^- threshold at different V_{sub} for the APTS-OA modified and modified with gap processes. All the tracks are perpendicular to the DUT plane and the incident angles on x and y are lower than 0.001 degree.

H APTS-OA correlation between seed signal charge and seed signal leading edge time

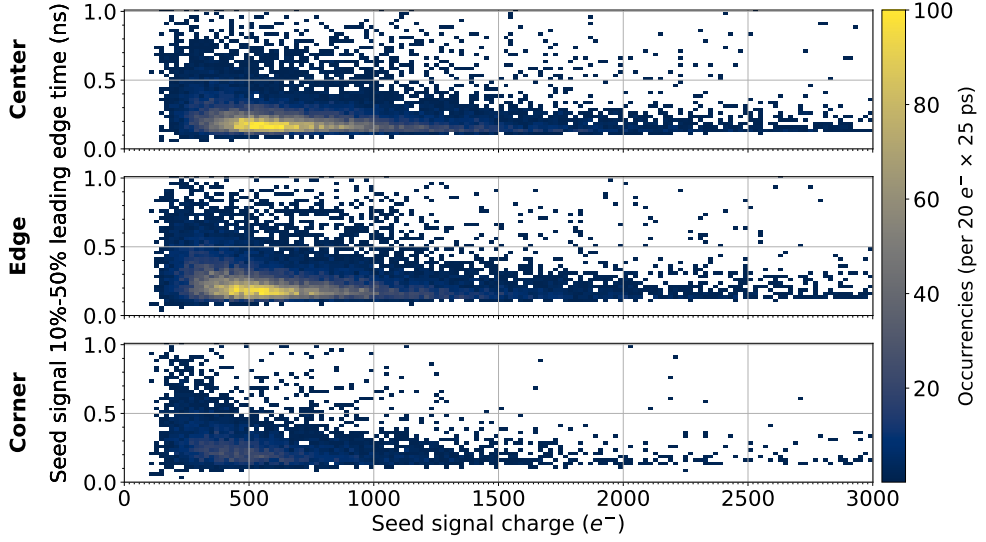


Figure H.1 Correlation between seed signal charge and signal leading edge time for the APTS-OA modified with gap DUT operated at $V_{\text{sub}} = -4.8$ V. Data is grouped in three different datasets depending on the reconstructed in-pixel track hit position.

The non-uniformity of the analog signal shape is investigated by studying the correlation between the seed signal charge and the signal leading edge time, expressed as the difference between the signal time at 50% of full amplitude and the time at 10% of full amplitude. The leading edge time is used as a proxy to evaluate the signal slope. Slower signals, i.e. longer leading edge times, are observed for smaller collected charge. Data are selected depending on the reconstructed in-pixel associated track hit position. With reference to the $2\text{ }\mu\text{m} \times 2\text{ }\mu\text{m}$ in-pixel binning used in Fig. 5.12, events associated to the pixel center have reconstructed intercept $-3\text{ }\mu\text{m} < x < 3\text{ }\mu\text{m}$ and $-3\text{ }\mu\text{m} < y < 3\text{ }\mu\text{m}$. Events associated to the corner dataset belong to the four corner in-pixel bins, edge is the remaining data.

I Response of APTS-OA to minimum ionizing particle beam

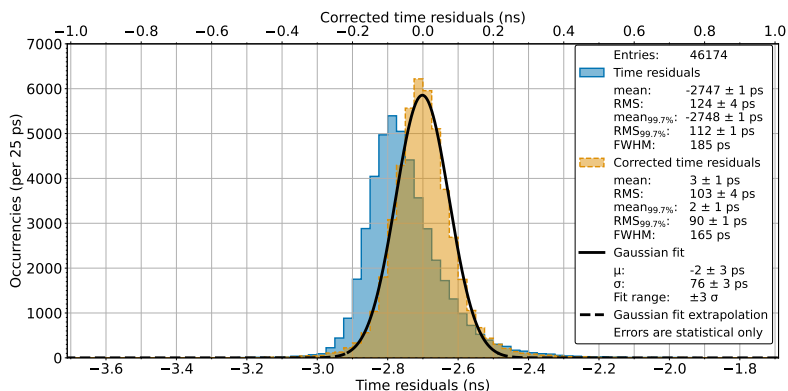


Figure I.1 Time residuals measured for the modified with gap process DUT operated at $V_{\text{sub}} = -1.2$ V, before (blue distribution, bottom horizontal axis) and after (orange distribution, top horizontal axis) time walk-like correction. The latter distribution is fitted with a Gaussian function on a range of $\pm 3\sigma$ (black solid line, dashed line for points outside the fit range)

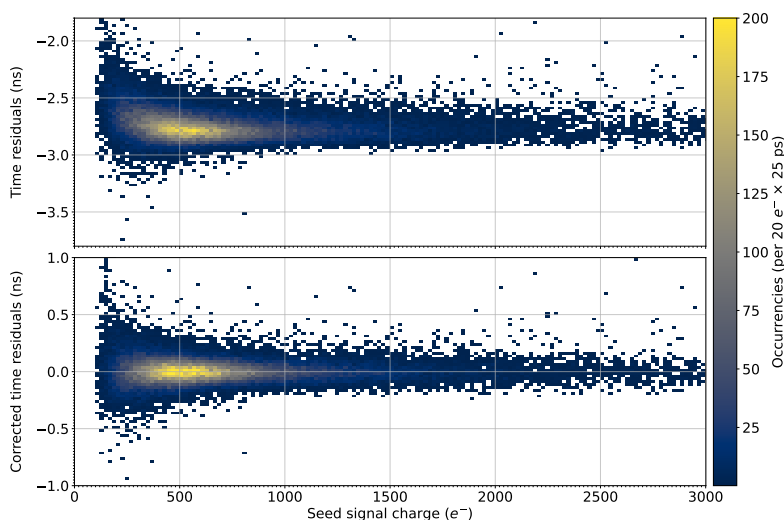


Figure I.2 Time residuals versus seed signal charge with no correction applied (top) and after the correction (bottom) for the DUT featuring modified with gap process operated at $V_{\text{sub}} = -1.2$ V.

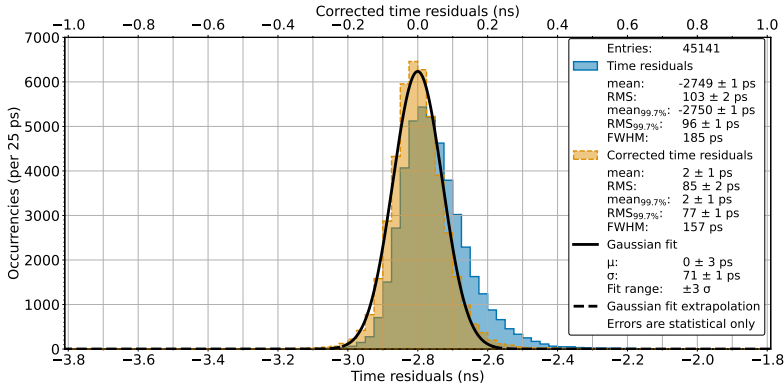


Figure I.3 Time residuals measured for the modified with gap process DUT operated at $V_{\text{sub}} = -2.4$ V, before (blue distribution, bottom horizontal axis) and after (orange distribution, top horizontal axis) time walk-like correction. The latter distribution is fitted with a Gaussian function on a range of $\pm 3\sigma$ (black solid line, dashed line for points outside the fit range)

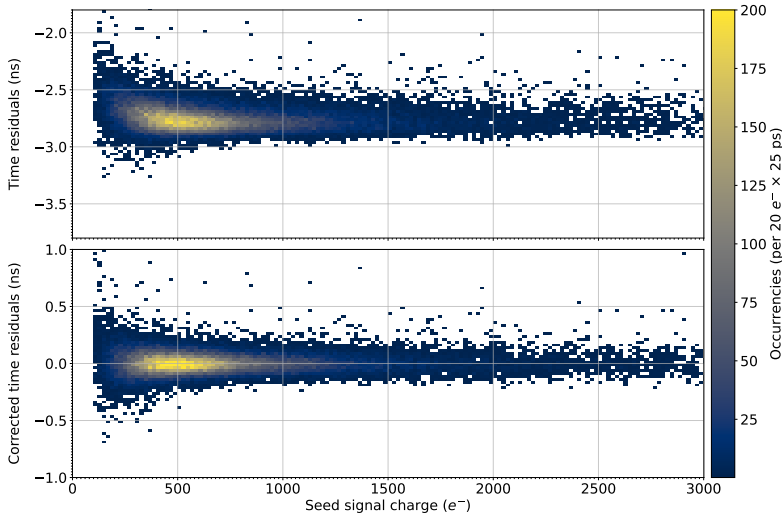


Figure I.4 Time residuals versus seed signal charge with no correction applied (top) and after the correction (bottom) for the DUT featuring modified with gap process operated at $V_{\text{sub}} = -2.4$ V.

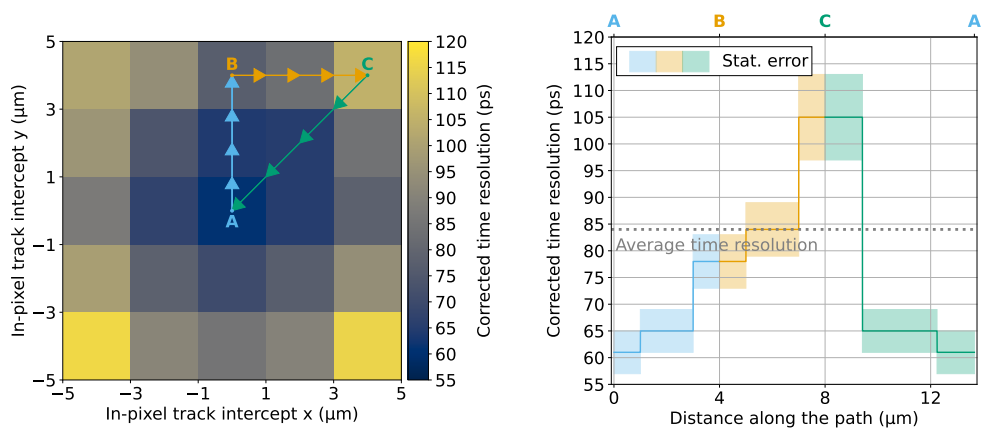


Figure I.5 Left: corrected in-pixel time resolution of the modified with gap structure operated at $V_{\text{sub}} = -1.2$ V. Right: time resolution variation along the path from the pixel center (A) to the edge (B), and to the corner (C).

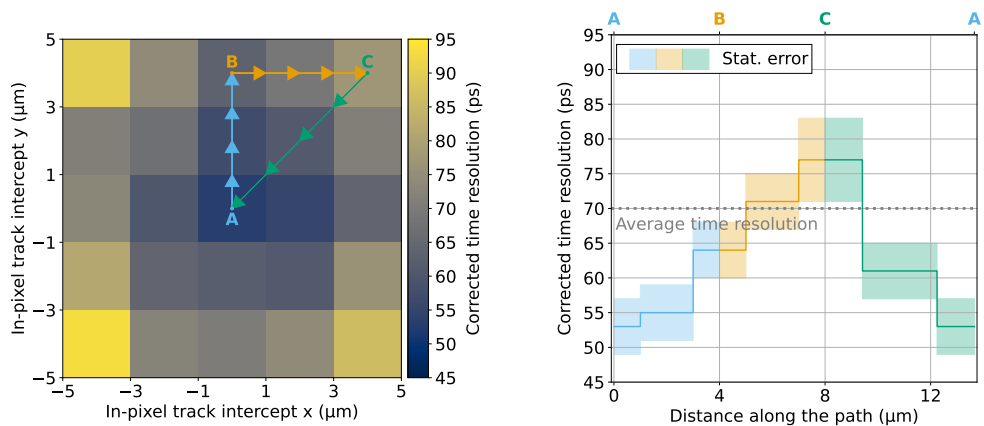


Figure I.6 Left: corrected in-pixel time resolution of the modified with gap structure operated at $V_{\text{sub}} = -2.4$ V. Right: time resolution variation along the path from the pixel center (A) to the edge (B), and to the corner (C).

Acknowledgements

ALTHOUGH they typically close a PhD thesis, the acknowledgements pages are usually the first ones to be read and often receive the most attention. Aware of the importance of the following words, I will try my best to not disappoint you with my dry writing style, dear Reader. And if I do it, I hope the rest of the manuscript won't let you down.

My four years in the Netherlands have been a long journey. I came to Amsterdam during the pandemic - not the brightest moment to land into a new place - and left a city I gradually learnt to appreciate.

And now that my PhD at Nikhef, through thick and thin, is over, it's time to take stock. I've reflected many times on how to evaluate this experience, and changed my mind just as many. I can finally say that my Dutch adventure has been highly instructive and, yes, successful. Among the many amazing people I met along the way, there are a few with whom I want to share the credit for this success.

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