Towards a 40 ps silicon (Si) tracker

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Abstract

Towards the High Luminosity - Large Hadron Collider (HL-LHC) era, the LHCb collaboration is envisaging a new silicon tracker introducing timing. The timing performance of multiple 3D and planar silicon sensor pixel structures, irradiated up to 10^{17} $n_{eq}cm^{-2}$ is evaluated in SPS pion (π^+) test-beams using a EUDET type telescope for precision tracking. A novel 16 channel, high bandwidth, fast timing board in conjunction with a SAMPIC Time to Digital Converter (TDC) is being developed and evaluated as a base platform for future R&D. Both the test-beam setup and the timing board are discussed and results are presented from the prototype production.

Introduction

VELO upgrade II and silicon(Si) detectors

The ten-fold increase on instantaneous luminosity to 1.5×10^{34} $cm^{-2}s^{-1}$ [1] expected during HL-LHC operation imposes strict constraints on detector operation and design. Extensive radiation damage as well as a higher data rates and event multiplicity are only some of the challenges faced by the experiments. The pile up at the LHCb experiment (number of interactions per bunch crossing) is expected to increase from 5.5 to 42 [2], leading to primary vertex separation issues, reconstruction inefficiency and ghost vertices. A visual representation of the described issues can be shown in Fig.1.

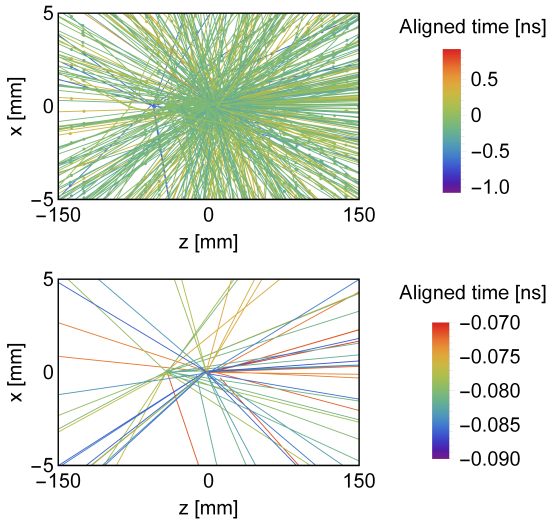

Figure 1: Extrapolated upgrade II bunch crossing with 2000 ps and 20 ps track time resolution[3]

Both planar and 3D technologies are evaluated in terms of their performance and radiation hardness. The main difference between planar and 3D sensors lies in the electrode geometry, used to collect the deposited charge. Whilst for planar pixels the bias and readout electrodes are typically located at the top and bottom of the active silicon layer, for 3Ds, they are perpendicular to the silicon substrate. In such a geometry, the drift distance is decoupled from the charge generating volume. A graphical representation of both technologies is shown in Fig.2.

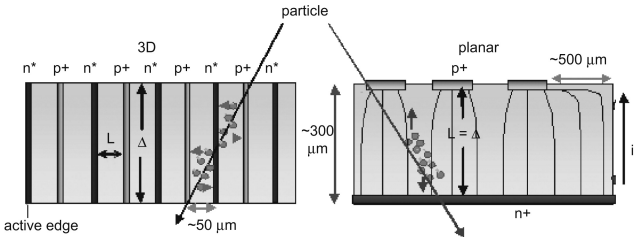

Figure 2: Cross section image of a 3D (left) and a planar (right) sensor with active thickness Δ [4]

Planar sensors are an older, proven technology with a lower manufacturing cost. They possess important physical advantages such as uniform electric field (therefore constant drift velocity) compared to non-uniform one in the case of 3D sensors(cylindrical topology around the doped column). Their reduced cell capacitance leads to a reduced jitter and a better Signal to Noise Ratio (SNR). Their drawbacks include a high power dissipation after irradiation, as well as thickness dependence of the charge yield in the order of 72 e^-/h^+ pairs um^{-1} [4]. 3D sensors are more resistant to radiation damage with proven operation at $\sim 2 \times 10^{16}$ $n_{eq}cm^{-2}$ [5] compared to the $\sim 7 \times 10^{15}$ $n_{eq}cm^{-2}$ [6] of the planars. This result is a direct consequence of the shorter drift distances (distance between cathode and anode elec-

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trodes) leading to less trapping and therefore a higher radiation tolerance.

16 channel board and SAMPIC TDC

In order to meet the requirements of current and future R&D, a 16 channel timing board with rapid DUT (Device Under Test) replacement capabilities was developed. The board utilities discrete analog components to amplify and shape the sensor induced signal. The circuit is based on a two stage amplification circuit designed around a high bandwidth SiGe transistor. The first stage is configured as a transimpedence amplifier followed by a voltage amplifier, with a total estimated gain of 72. The sensor matrix is mounted on an interchangeable daughter board, facilitating the quick replacement of DUTs. Each channel's amplifier is encapsulated in an individual Faraday cage to mitigate pickup and minimize electromagnetic noise.

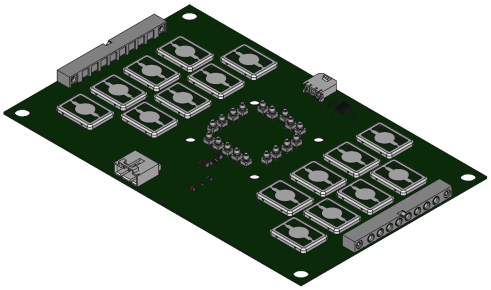


Figure 3: 16 channel board

The amplified signal is directed to a SAMPIC TDC, which performs the digitization using a continuous read-out via a rolling shutter Analog to Digital Converter (ADC). The device can provide a sampling frequency of 8 GS/s on 16 channels simultaneously. The ADC related jitter is estimated in the order of 4 ps per channel [7].

Setup

Testbeam

To evaluate the timing performance of silicon sensors, a test-beam setup was installed at the CERN SPS H6 beam-line. Using a 160 GeV pion (π^+) beam, the induced MIP-like (Minimum Ionizing Particle) signal was recorded and digitized. This setup consists of a EUDET pixel telescope [8] with 6 MIMOSA26 planes of matrix 576×1152 pixels with a 18.4 µm pitch [9]. Behind the 5th telescope plane, an FEi4 single chip module [10] was attached to construct Region Of Interest (ROI) trigger and enable precise DUT alignment. A diagram of telescope is shown in Fig.4.

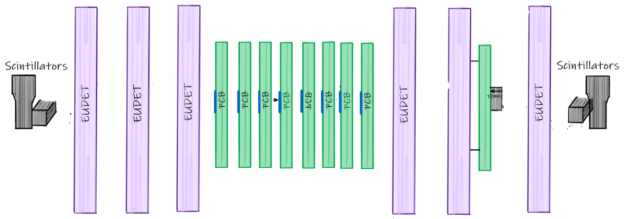


Figure 4: EUDET telescope diagram

Between the upstream and downstream arms of the telescope, each consisting of three planes, an XPS box is placed housing the DUTs assemblies. The latter, consisting of a readout PCB containing the sensor, is mounted on a two-axis micro-metric alignment stage featuring piezo-electric motorization Fig.5. All DUT assemblies are fixed on a removable metal drawer. A heat exchanger, mounted at the top part of the DUT box, allows for low temperature operation (-20 °C), essential to avoid annealing and mitigate the high leakage current of irradiated structures.

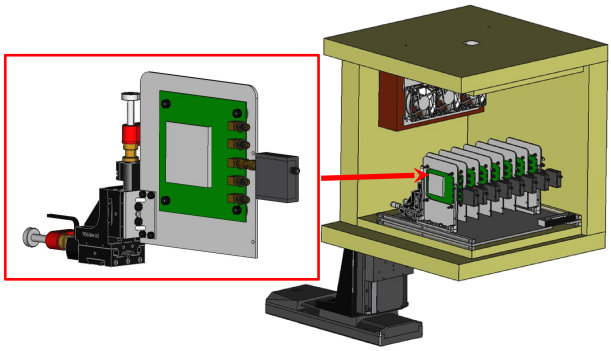


Figure 5: Motorised stage with mounted amplification board (left) and cooling DUT assembly (right)

The Low Voltage (LV) components of each PCB board consist of a first stage tranceimpedance SiGe amplification circuit and an output for an external high bandwidth (6GHz) second stage voltage amplifier. Each board also has a High Voltage (HV) input used to bias the mounted sensor. Independent LV and HV Power Supply Units (PSU) were set up and controlled remotely (custom LabView software) to ensure reliability and to allow for remote operation.

Triggering was handled by a Trigger Logic Unit (TLU), that was used to collect the trigger signals from a scintillator (mounted in front of the telescope), and the FEi4 module which are subsequently processed and a general trigger signal

is produced in each coincidence event. A custom analogue trigger board was developed to minimise data loss by receiving the SPS synchronization signal as well as the TLU triggers and creating a VETO trigger zone. The DUT signal was collected using two 10 GHz bandwidth oscilloscopes registering the raw waveform for each trigger event.

The planar DUTs were 1mm diameter circular diodes of active thicknesses 50 µm and 100 µm. The single sided 3D sensors had a pixel-size of 50 µm x 50 µm and 25 µm x 100 µm, with active thicknesses of 190 µm and 150 µm respectively. The double sided 3D sensors had a pixel-size of 55 µm x 55 µm and an active thickness of 230 µm. Testing was performed using unirradiated and neutron and proton irradiated DUTs in fluences of 10^{15} $n_{eq}cm^{-2}$, 8×10^{15} $n_{eq}cm^{-2}$, 6×10^{16} $n_{eq}cm^{-2}$, 10^{17} $n_{eq}cm^{-2}$. The DUTs occupy the six central positions in the metal drawer. The outer slots consist of stationary LGAD [11] type sensors, acting as timing references.

16 channel board testing setup

For pickup and noise measurements of the 16 channel board, an oscilloscope was used to perform simultaneous measurements of 4 channels (Fig.6). Capton tape secured the readout cables to an electrostaticaly safe mat to isolate the system and minimise noise. A LV PSU was used to supply the amplification electronics with 5 V while the sensor was biased by a HV PSU at a negative voltage of 50 V. These measurements were performed with and without the presence of a sensor matrix. The channels from the board were connected to TDC with the same numbering scheme as in Fig.7.

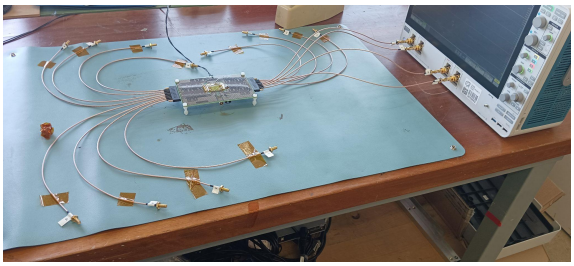


Figure 6: Testing setup for 16 channel board pickup measurements

For sensor performance measurements, a source of ^{90}Sr was used. Two different configurations (orders) were considered for measured output connections. Order 1 measurements had four consecutive channels (ex. 1-2-3-4) connected simultaneously, while order 2 had four alternate channels (ex. 1-3-5-7) connected. The numbering configuration can be found in Fig.7. Each order had a waveform collected per channel with the trigger set to the minimum possible voltage.

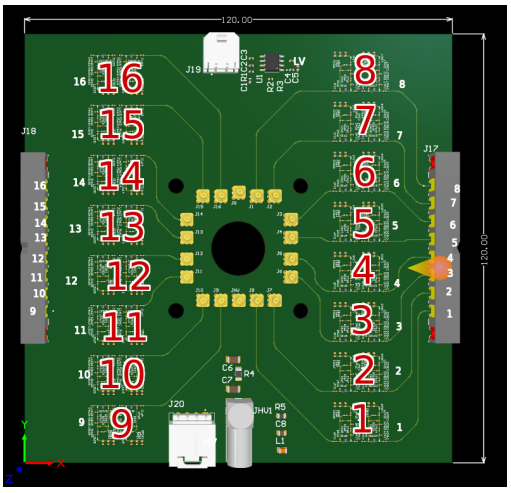
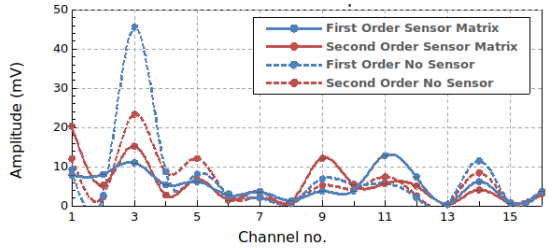


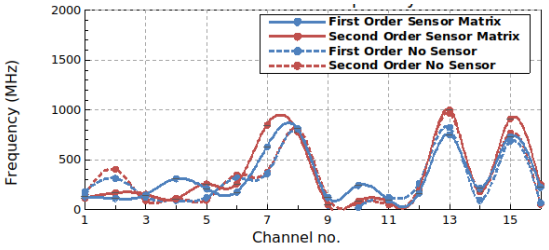
Figure 7: Numbering channel schematic for 16 channel board measurements

Results

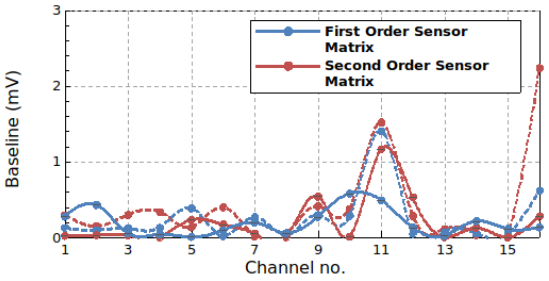
The pickup measurements produced voltage over time waveforms. Data analysis was performed using Python, due to its library access. The detecta library's `detect_peaks` function was used for the identification of the waveform peaks. This function compares the neighbouring values of array to distinguish the peaks from a dataset. Jitter induced false peaks can occur by using this method. In order to prevent this effect, the function's mpd (minimum peak distance) parameter was set altered. The mpd parameter was found to work most optimally for this dataset at a value of 80. The mean amplitude, mean frequency and mean baseline (y-axis shift) values were calculated and plotted as a function of channel number (Fig.8).



(a)



(b)



(c)

Figure 8: Pickup measurements for the 16 channel board with (a) Mean amplitude value per channel (b) Mean frequency per channel (c) Mean baseline per channel

Low amplitude values are measured for all setup configurations for channels 8, 13 and 15 (Fig.8a). The low amplitude in combination with the higher frequency values on the same channels (Fig.8b) is an indication of malfunctioning amplification electronics. After further investigation, these channels were found to contain out of spec resistors, thereby not allowing for proper operation.

In Fig.8c it can be observed that channels 11 and 16 have higher baseline values $\sim 1.5 - 2.5$ mV compared to the average value ~ 0.3 mV. This can be explained by a floating ground (lack of connection with ground plane). All channels behave similarly with and without the presence of a biased matrix sensor. This behaviour indicates that the sensor capacitance is low on input as well as low pickup from the HV circuit to the LV one.

Conclusion

The 16-channel board results are promising for further R&D and implementation within the testbeam setup. Such an implementation will provide the ability for quick installation of the DUTs within the setup, as well as improvements in the efficiency of measurements, as multiple silicon sensors can be wire-bonded into daughter boards and very quickly swapped with already tested samples.

Furthermore this platform can provide a decrease in the alignment time for DUTs, as the process can be performed once and then small corrections can be made when introducing new daughter boards. The SAMPIC TDC also allows for the simultaneous recording of 16 channels, thereby increasing the overall timing precision of the setup. These potential improvements in the setup process indicate that a correction of the out of spec hardware as well as further pickup testing be performed so as to allow for seamless integration of this upgrade.

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