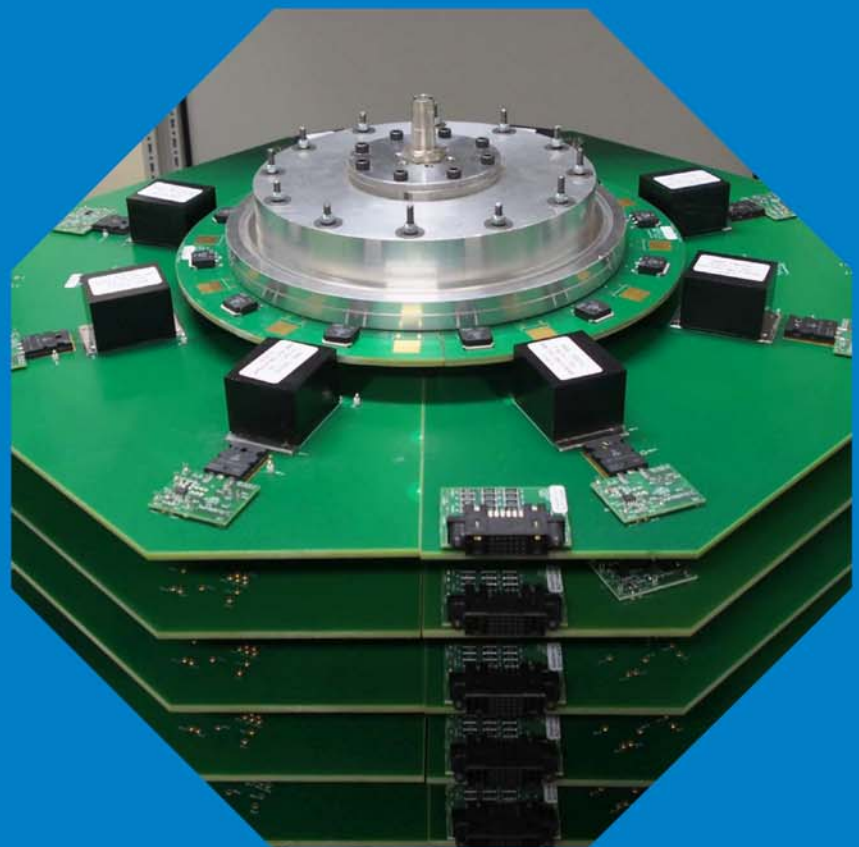


A Pulse Power Modulator with Extremely Flat-top Output Pulses for the Compact Linear Collider at CERN

Janne Holma



A Pulse Power Modulator with Extremely Flat-top Output Pulses for the Compact Linear Collider at CERN

Janne Holma

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Abstract

This dissertation presents the design procedure and results of measurements on two prototypes for a high-stability pulse power modulator. Design and prototyping of the pulse modulator is a part of the feasibility study of Compact Linear Collider (CLIC) study. The CLIC design relies on Pre-Damping Rings (PDR) and Damping Rings (DR) to achieve the very low emittance through synchrotron radiation. The pulse power modulators for the DR kickers must provide extremely flat, high-voltage pulses. The final specifications of the 2 GHz baseline called for a 160 ns duration flat-top of 12.5 kV, 250 A, with a combined ripple and droop of not more than ± 0.02 % of the output voltage, corresponding to ± 2.5 V of absolute accuracy.

The dissertation begins with a literature review to choose the topology for a high-precision pulse power modulator. A modulator based on solid-state switches, the inductive adder, has been selected as the most promising approach to meeting the specifications. This topology allows the use of both digital and analogue modulation techniques. Then, the electrical and mechanical design of the inductive adder are presented, especially for matching the output impedance of the modulator to a load. The reasoning for selecting the main components for an inductive adder is also covered. Simulation studies of applying different compensation methods for achieving the required pulse waveform for the CLIC DR extraction kicker system are also presented. Two prototype inductive adders were built to verify these methods experimentally. Finally, a design proposal is presented for a 12.5 kV inductive adder covering main components and preliminary simulation results.

As the main results, the dissertation presents experimental verification of applying modulation methods to improve the pulse flat-top stability of a high-voltage pulse power modulator. These measurement were done with two built prototype inductive adders. The best measured relative accuracy for the pulse flat-top stability was ± 0.05 % at 1.8 kV for 160 ns pulse flat-top duration, which corresponds to ± 1 V of absolute accuracy. The dissertation shows that the required high stability for the CLIC DR extraction kicker inductive adder is very probably feasible with the developed design.

Keywords inductive adder, analogue modulation, droop compensation, ripple compensation

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Tiivistelmä

Väitöskirjassa esitetään suunnitteluaskeleet ja kaksi prototyyppilaitetta erittäin suuren tarkkuuden pulssiteholähteen toteuttamiseen. Tutkimus on osa Compact Linear Collider (CLIC) -kiihdyttimen toteutettavuustutkimusta. CLIC-hiukkaskiihdyttimessä käytetään esivaimennuspiirejä (Pre-Damping Ring) ja vaimennuspiirejä (Damping Ring), joilla saavutetaan synkrotronisäteilyä hyödyntäen erittäin alhainen hiukkassuihkun emittanssi. Vaimennuspiirien ohjausmagneetteja syöttävien pulssiteholähteiden täytyy tuottaa äärimmäisen tasalattvaisia korkeaajännitteisiä pulsseja. Teholähteen vaatimukset vaimennuspiiriin 2 GHz:n perustaajuudella toimivalle versiolle ovat seuraavat: 160 ns:n pituinen tasalattvainen pulssi 12.5 kV:n jännitteellä ja 250 A:n virralla, jonka yhdistetty amplitudin vaihtelu ja virran tai jännitteen alenema pulssin aikana saa olla korkeintaan ± 0.02 % asetetusta arvosta. Tämä vastaa ± 2.5 V:n absoluuttista tarkkuutta.

Aluksi työssä esitetään kirjallisuuskatsaus topologian valitsemiseksi annettujen vaatimusten mukaan. Tämän perusteella pulssiteholähteen perusratkaisuksi on valittu puolijohdekytkimiin perustuva induktiivinen summain, koska summaimen ulostulojännitettä voidaan moduloida sekä digitaalisilla että analogisilla modulaatiomenetelmillä. Tämän jälkeen esitellään induktiivisen summaimen sähköinen ja mekaaninen suunnittelu sekä menetelmä summaimen lähtöimpedanssin asettamiseksi haluttuun arvoon. Työssä käsitellään myös yksityiskohtaisesti induktiivisen summaimen pääkomponenttien valinta sekä kompensointimenetelmiä, joilla induktiivisen summaimen ulostulojännitteen tarkkuutta voidaan parantaa. Työssä esitetyt suunnittelumenetelmiä käyttäen on rakennettu kaksi 3.5 kV:n prototyyppilaitetta, joilla on kokeellisesti todistettu ulostulopulssin jännitteen aleneman ja korkeataajuisen vaihtelun aktiivinen suodatus. Lopuksi esitetään toteutussuunnitelma 12.5 kV:n induktiiviselle summaimelle sisältäen komponenttien valinnan ja alustavat simulointitulokset.

Työn tärkein tulos on kokeellinen osoitus siitä, että induktiivisen summaimen ulostulojännitteen tarkkuutta pystytään parantamaan modulaatiomenetelmiä käyttäen. Paras työssä saavutettu jännitepulssin tarkkuus oli ± 0.05 % 1.8 kV:n jänniteellä, joka vastaa ± 1 V:n absoluuttista tarkkuutta. Työssä on osoitettu, että CLIC-kiihdyttimen vaimennuspiirien ohjausmagneettien pulssiteholähteen vaatimusmäärittelyt voidaan hyvin todennäköisesti saavuttaa induktiivisella summaimella, joka rakennetaan väitöskirjassa esitetyt suunnitteluperiaatteita noudattaen.

Avainsanat induktiivinen summain, analoginen modulaatio, jännitteen aleneman kompensointi, jännitteen vaihtelun kompensointi

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Preface

The aim of the CLIC project is to broaden our knowledge of the structure of the fundamental particles and, therefore, the entire universe. It has been really fascinating to work for such a universal scientific study. Constructing prototype devices was as exciting as building a toy car of Lego bricks as a child, just with a difference that I also needed to design the bricks this time.

I want to thank all people who have helped and supported me during this project. First of all, I want to express my best gratitude to Dr. Mike Barnes for excellent supervising, all valuable pieces of advice and encouragement which I have received during the last five years at CERN. Secondly, I wish to thank professor Ovaska for great support and highly appreciated guiding of this work from the academic point of view. Thirdly, I want to give my thanks to all my colleagues at CERN. I would like to name a few people, to whom I would like to give special thanks: Michael Betz, for helping with measurements, Petri Leinonen, for providing knowledge about RF electronics and soldering work, and Tuukka Berg for an intensive course on 3D modelling tools. Great thanks also to Iikka Mätäsaho and Jose Varela Campelo for fruitful discussions at lunch times at CERN, about life, the universe and everything, including particle accelerators, floorball and skiing. I also want to thank Ed Cook from the Lawrence Livermore National Laboratory for providing his expertise and knowledge in use for this project, and Wade Bittle from the Rochester University for some very valuable piece of advice considering the design of the prototype devices.

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ternet. I want to thank my parents and friends for all kind of support which I have received during my studies at the university. I would like to give special thanks to the Finnish Society of Electronics Engineers, Ulla Tuominen Foundation and Jenny and Antti Wihuri Foundation for promoting my research study by giving grants for conference trips and for writing work. Finally, I wish to thank all the members of ski touring section of Cern Ski Club for providing many refreshing outings to the white shimmering mountains in the French, Swiss and Italian Alps at the winter weekends. These breaks were essential to have fresh ideas in mind in the working weeks. Special thanks also to a passionate singer, a single blackbird, which used to practice beautiful chords in a tree at the Prévessin site of CERN in spring 2015, when I was busy in writing the last paragraphs of this dissertation. That lovely music, as well as the violin concerto from Jean Sibelius, were important incentives for me in that finishing phase.

Prévessin, November 4, 2015,

Janne Holma

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Symbols and Abbreviations

Symbols

(Note: For symbols, for which form e.g. I_{load} is shown in a figure and I_{load} written in a caption, only I_{load} is shown below.)

A_c	physical cross-sectional area of a magnetic core
$A_{c,eff}$	effective cross-sectional area of a magnetic core
A_s	cross-sectional area of a conductor
B	flux density
$\vec{B}$	magnetic field
B_{S-}	negative saturation flux density of a magnetic core
B_{S+}	positive saturation flux density of a magnetic core
B_{R-}	negative remnant flux density of a magnetic core
B_{R+}	positive remnant flux density of a magnetic core
BV_{DSS}	breakdown voltage between a drain pin and a source pin of a MOSFET
BW_{-3dB}	–3 dB bandwidth of a measurement system
c	velocity of light
C	capacitance
C_c	coupling capacitance per layer of an inductive adder
C_{PF}	packing factor of a magnetic core
C_s	capacitance per layer of an inductive adder
$C_{s,1br}$	capacitance of a single branch of a layer of an inductive adder
$C_{s,2br}$	effective capacitance of two parallel branches of a layer of an inductive adder
C_{st}	capacitance between stripline electrodes
C_{stg}	capacitance between a stripline electrode and ground
d	outside diameter of the secondary winding (stalk)

dB	differential change of magnetic field
d_{mp}	diameter of a magnetic path
dt	differential step of time
D	decimation ratio of the averaging filter
D_1	inside diameter of the inner wall of a primary circuit
D_1/d	ratio of the inside diameter of the inner wall of a primary circuit to the outside diameter of the secondary winding
D_2	inside diameter of a magnetic core
D_3	outside diameter of a magnetic core
D_4	outside diameter of the outer wall of a primary circuit
D_i	diode
D_{ins}	insulation thickness between the primary and secondary windings
$\vec{E}$	electric field
E_{max}	maximum electric field between the primary and secondary windings
$\vec{F}_{(E+B)}$	Lorentz force to a charged particle in an electric and a magnetic field
F_r	pulse repetition rate
F_s	sampling rate
$F_{s,eff}$	effective sampling rate
$f_{Res,FFT}$	frequency resolution of the fast Fourier transform algorithm
h_r	thickness of the ribbon of a magnetic core
h_s	height of a conductor
I	current
I_b	biasing current of a magnetic core
I_{beam}	current of particle beam in an accelerator
$I_{b,img}$	image current of particle beam in a stripline of a kicker
I_{Cs}	current of a pulse capacitor
I_D	current to a drain pin of a MOSFET
I_{Di}	diode current
I_{eddy}	eddy current in a strip of magnetic material
I_{Lm}	magnetising current of a magnetic core
$I_{Lm,max}$	maximum magnetising current of a magnetic core
I_{load}	load current
I_m	modulation current source in an analogue modulation layer
I_{out}	output current of a inductive adder
I_p	primary current

I_r	ripple current source
I_{Rc}	current of a core loss resistance
I_{st}	stripline current
I_{Sw}	current of a switch
l_c	height of a magnetic core
l_{av}	arithmetic average value of the inside and outside circumferences of a magnetic core
l_{mean}	mean length of a single turn of the ribbon of a tape-wound magnetic core
l_p	length of a layer of an inductive adder
l_s	length of a conductor
L	inductance
L_m	magnetising inductance
L_{ma}	magnetising inductance of an analogue modulation layer
L_{pl}	primary loop inductance per layer of an inductive adder
$L_{pl,1br}$	primary loop inductance of a single branch of a layer of an inductive adder
$L_{pl,2br}$	effective primary loop inductance of two parallel branches of a layer of an inductive adder
L_s	inductance of a section of a conductor
L_{ss}	secondary inductance per layer of an inductive adder
n	number of measurements to average
N	number of constant voltage layers
N_{ADC}	bit length of an analogue to digital converter
$N_{ADC,eff}$	effective bit length of an analogue to digital converter
N_{boxcar}	length of the averaging filter
N_{ri}	noise amplitude of a signal
N_s	number of samples in a data set
N_t	number of turns of the ribbon of a tape-wound magnetic core
N_w	number of turns of the primary winding
P_c	eddy current power loss in a magnetic core
$P_{c,pv}$	eddy current power loss density (W/m^3) in a magnetic core
q	charge of a particle
R	resistance
R_a	primary resistor value of an analogue modulation layer
$R_{a,eff}$	effective primary resistance of an analogue modulation layer
R_c	core loss resistance
$R_{c,comp}$	computed core loss resistance

$R_{c,meas}$	measured core loss resistance
Res_{Abs}	absolute resolution of an analogue to digital converter
Res_{ADC}	resolution of an analogue to digital converter
Res_{Eff}	effective resolution of an analogue to digital converter
$Res_{Enh,ea}$	resolution enhancement of an analogue to digital converter given by ensemble averaging
$Res_{Enh,os}$	resolution enhancement of an analogue to digital converter given by oversampling
Res_{Rel}	relative resolution of an analogue to digital converter
R_{load}	load resistance
$R_{load,eff}$	effective load resistance
R_{load}/N	load resistance per layer
R_p	primary resistance per layer
$R_{p,1br}$	primary resistance of a single branch of a layer
$R_{p,2br}$	effective primary resistance of two branches of a layer
R_s	secondary resistance per layer
R_{sw}	effective on-state resistance of the switches of a layer
$R_{sw,1br}$	on-state resistance of a single switch of a layer
$R_{sw,2br}$	effective on-state resistance of the switches of two parallel branches of a layer
S	amplitude of a signal
Sw	switch
t	time
t_d	single-way time delay of a coaxial cable
t_p	pulse flat-top duration
$t_{p,50}$	pulse duration at half maximum
T_{adder}	transmission line model for an inductive adder
T_{cable}	transmission line model for a coaxial cable
T_r	rise time of the pulse
$T_{r,0.02\%-99.98\%}$	rise time from 0.02 % to 99.98 % of the pulse voltage
$T_{r,10\%-90\%}$	rise time from 10 % to 90 % of the pulse voltage
$T_{rd,1w}$	single-way electrical propagation delay through the secondary of an inductive adder
$T_{rd,2w}$	two-way electrical propagation delay through the secondary of an inductive adder
t_s	sampling interval
$T_{s,\pm 0.02\%}$	settling time of the pulse to ± 0.02 % of the flat-top voltage
$T_{stripline}$	transmission line model for a stripline kicker

T_x	transformer
$\vec{v}$	velocity of a particle
V_b	beam-induced voltage in a stripline
V_{Bias}	biasing DC voltage for an RF power transistor
V_c	voltage across a capacitor
V_{ci}	initial charging voltage of the pulse capacitors
V_{cl}	voltage stress across an insulation layer in a tape-wound magnetic core
V_{DS}	voltage between a drain pin and a source pin of a MOSFET
V_e	volume of a magnetic core
$V_{\text{e,eff}}$	effective volume of a magnetic core
V_{GS}	voltage between a gate pin and a source pin of a MOSFET
V_{layer}	voltage across the secondary of a layer of an inductive adder
V_{load}	load voltage
$(V_{\text{load}} + I_{\text{load}})/2$	normalised sum of the load voltage and the load current
V_{out}	output voltage of an inductive adder
$V_{\text{r,ADC}}$	voltage range of an analogue to digital converter
$V_{\text{Ra,max}}$	maximum voltage across an analogue modulation layer during a pulse
V_s	voltage source
V_{st}	stripline voltage
V_{sum}	sum of the output voltages of the constant voltage and digital modulation layers of an inductive adder
V_{Tr}	trigger voltage
w_s	width of a conductor
Z	impedance
Z_{load}	load impedance
Z_{out}	output impedance
$Z_{\text{stripline}}$	impedance of a stripline electrode
ΔB	flux-density swing
ΔI	change of current
ΔI_{Lma}	change of the current of the magnetising inductance in an analogue modulation layer
Δt	time period for a change of variable

$\Delta\phi$	deflection angle of a kicker
ΔV_{d+r}	combined droop and ripple of the output voltage
ΔV_{pl}	voltage droop of the pulse capacitors of a layer
ΔV_{load}	droop of the load voltage
ΔV_{Ra}	decrease of the voltage across an analogue modulation layer during a pulse
ϵ	permittivity
ϵ_i	product of the relative permittivity and the permittivity of free space
ϵ_r	relative permittivity
μ	permeability
μ_0	permeability of free space
μ_c	product of the relative permeability of a magnetic core and the permeability of free space
μ_r	relative permeability
ρ	resistivity
σ	standard deviation
σ_C	standard deviation of capacitance
σ_L	standard deviation of inductance
σ_R	standard deviation of resistance

Abbreviations

3D	three dimensional
ADC	analogue to digital converter
AM	active analogue modulation
ARM	Advanced Radiography Machine
av.	average
B	branch of an inductive adder
C	collector pin of an insulated-gate bipolar transistor
CERN	European Organization for Nuclear Research
CHF	Swiss Franc
CLIC	Compact Linear Collider
comp.	compensation
CR	combiner ring
d	droop
D	drain pin of a metal-oxide-semiconductor field-effect transistor
DARHT	Dual-Axis Radiographic Hydrodynamic Test Facility
DC	direct current
d&r	droop and ripple
deg.	degree
DR	damping ring
E	emitter pin of an insulated-gate bipolar transistor
ECSA	effective cross-sectional area of a magnetic core
ENOB	effective number of bits of an analogue to digital converter
Ext.	extraction
FFT	fast Fourier transform
FET	field-effect transistor
G	gate pin of a transistor
IA	inductive adder
Inj.	injection
IGBT	insulated-gate bipolar transistor
IP	interaction point
L	layer of an inductive adder
LCR	inductor-capacitor-resistor
LHC	Large Hadron Collider
linac	linear accelerator
LLNL	Lawrence Livermore National Laboratory
LTD	linear transformer driver

magn.	magnitude
mod.	modulation
MOSFET	metal-oxide-semiconductor field-effect transistor
n/a	not available
PCB	printed circuit board
PFL	pulse forming line
PFN	pulse forming network
PDR	pre-damping ring
PM	passive analogue modulation
r	ripple
Ref.	reference
RF	radio frequency
RL	resistor-inductor
S	source pin of a metal-oxide-semiconductor field-effect transistor
SLAC	Stanford Linear Accelerator Center
TEM	transverse electromagnetic
TO-264	a standard semiconductor package of transistor series

1. Introduction

The European Organization for Nuclear Research, CERN, is one of the world's largest centres for scientific research. The abbreviation CERN is derived from the French expression of its predecessor, "Conseil Européen pour la Recherche Nucléaire" and CERN is usually referred to as the European Laboratory for Particle Physics. CERN was founded in 1954 and it has now 21 member states [1]. The aim of CERN is to study fundamental physics, which basically means researching laws of nature and discovering what the universe consists of and how it works. The other missions for CERN are technology development, especially regarding particle accelerators and detectors as well as collaboration between nations through science, and education.

The Large Hadron Collider (LHC) is the flagship of the CERN's accelerators (Fig. 1.1). It was started for the first time in 2008. The LHC is 27 km long and it is the largest and the most powerful particle accelerator in the world [2]. The biggest scientific achievement made by the LHC so far is the discovery of the Higgs boson by its Atlas and CMS experiments [3], [4]. The discovery of a new subatomic particle, the first since 2000, was a remarkable event and was noticed in media worldwide [5].

The LHC will be running at least until 2023, and with upgrades until 2035 or even further [6] but new generations of particle accelerators are already under design. One of the project plans for the large future accelerators is the Compact Linear Collider (CLIC). It is a study of a large electron-positron collider, which would have up to 3 TeV energy at the collision point [7]. In comparison with LHC's proton-proton and proton-ion collisions, which generate a number of sub-atomic interactions after a single collision, CLIC would be a precision instrument to study further the interactions found with the LHC [8]. The large accelerators are often built with new technology, which has not been used in such a large scale pre-

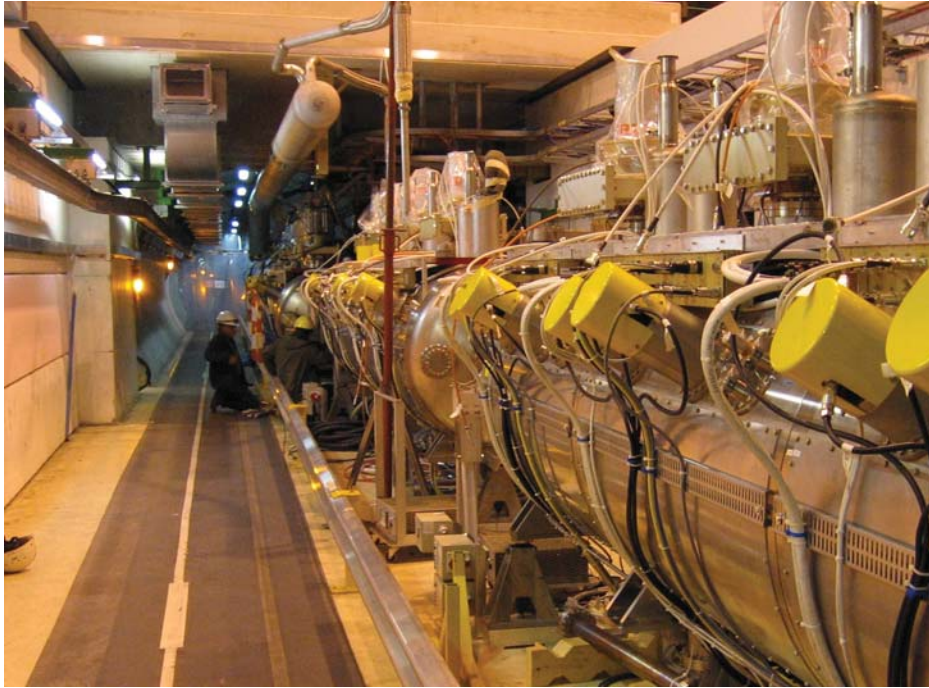


Figure 1.1. A view from the LHC tunnel at CERN.

viously. Therefore the accelerator projects are a driving force to advance limits of existing technologies. For the CLIC project, there are several feasibility studies going-on in the various fields, the goals of which are to verify that the machine is feasible with existing technology, or with the technology which can be developed to meet the given specifications. The subject of this doctoral dissertation is one of the feasibility studies of the CLIC project.

The goals of this feasibility study were the following:

1. Find a suitable pulse power modulator topology for the CLIC damping ring (DR) kickers, which meets the often conflicting requirements.
2. Make a proposal for possible means for achieving the required performance by carrying out in-depth analyses for the pulse modulator and by optimising the design to meeting the specifications for the pulse flat-top.
3. Design, manufacture and test a prototype pulse modulator to demonstrate that it is technically feasible to meet the demanding specifications for the pulse flat-top.

All these subjects have been covered in this doctoral dissertation.

Chapter "2 Requirement and Topology Selection for the CLIC DR Kicker

Systems" starts by highlighting some basic parameters of the CLIC accelerator and kicker systems, which are necessary for understanding the background of this study. It also includes a literature review to identify the most suitable topology for the extremely high-precision pulse power modulator. The dissertation introduces several topologies and gives reasoning for selecting the inductive adder topology as the starting point for the pulse power modulator with high stability and repeatability.

Chapter "3 Design of the Inductive Adder" gives a step-by-step description of designing for a pulse power modulator based on the inductive adder topology. It describes the main components of the modulator and gives detailed reasoning for selecting the components for the pulse power modulator with this topology, covering semiconductor switches, storage capacitors and magnetic cores. Chapter "3 Design of the Inductive Adder" also describes a design procedure for the inductive adder stack with a given output impedance and voltage. Most of the content of Chapter 3 is based on existing literature references. A preliminary design study is given for the CLIC DR extraction kicker inductive adder and for the two prototype inductive adders which are presented in Chapter 5. The main purpose of the preliminary design studies presented in Chapter 3 has been to define parameters for the simulation and modelling studies, which are presented in Chapter 4.

Chapter "4 Modelling and Simulation Studies" presents the developed simulation models of the inductive adder. The chapter includes the simulation studies of applying different compensation methods for achieving the required output waveform for the CLIC DR extraction kicker system and to study the effects of the parasitic circuit elements. PSpice simulation models have been developed for verifying different compensation methods and three dimensional (3D) models have been developed for finding the values of the parasitic circuit elements. The main results of these studies are presented in Chapter 4.

Chapter "5 Prototyping, Experimental Results and Design Proposal" presents the main results of the measurements on two prototype inductive adders. The most significant results are experimental verifications of both passive and active analogue modulation methods. The passive analogue modulation method has been applied to compensate the droop of the output waveform and the active analogue modulation method has been applied to compensate both droop and ripple. The accuracy of the measurements of the flat-top stability is also discussed in detail.

The prototype adders were built according to the design steps shown in Chapter "3 Design of the Inductive Adder". The electrical and mechanical design and assembly of the prototype inductive adders are presented in detail in Appendix A "Assembly of the Prototype Inductive Adders". Selection and testing of the main components have also been briefly covered, including verification of pulse capacitors, on/off-type semiconductor switches and RF power transistors. The guidelines for designing an inductive adder have been verified by comparing the output waveforms of the developed simulation models and the prototype inductive adder. The parameters of the simulation model of the prototype inductive adder, presented in Chapter "4 Modelling and Simulation Studies", are updated according to the evaluation of the components and the updated simulation models are used to estimate the output waveform of the 12.5 kV inductive adder for the CLIC DR extraction kicker system. Finally, the design proposal for the 12.5 kV inductive adder is presented in the last section of Chapter 5.

Chapter "6 Conclusions" clarifies the main results of this dissertation and scientific importance of the author's work. The most significant result is the successful demonstration of applying the active droop and ripple compensation to the output waveform of an inductive adder, which resulted in a measured flat-top stability of $\pm 0.05\ldots\pm 0.07\%$ ($\pm 0.96\ldots\pm 1.23\%$) for a 1.8 kV pulse for 160 ns flat-top duration. This dissertation is a part of the feasibility studies of the CLIC accelerator project and the flat-top stability obtained is a significant step towards meeting the final specifications of the flat-top stability of the output waveform of the CLIC DR kicker modulator ($\pm 0.02\%$). Also in this chapter, several promising proposals are presented for further developments, in order to improve the pulse flat-top stability, and hence to meet the final specifications of the CLIC DR extraction kicker system.

The presented studies have been covered partly or completely in other publications. Short literature reviews of existing pulse modulators were shown in [9] and [10]. The reasoning for choosing the main components of the inductive adder has been given in [10]-[12]. In addition to these, the stripline kicker system was presented in status reports [10] and [12]. Simulation studies of compensation of droop and ripple of the output pulse were presented in detail in [10] and [13], and briefly in [12]. Testing of components and sensitivity analyses of the effects of various parameters upon the pulse quality of the inductive adder were presented in [13] and

[14]. Modelling studies of the inductive adder structure and some results of the initial measurements of the prototype inductive adder were published in [15] and [16].

The journal article [17] presents simulation models of the inductive adder and the initial measurements on the first prototype inductive adder. It explains contributors to the droop of the output waveform and presents simulation studies of cancellation of both droop and ripple of the output pulse. As the most important topic, it presents measured results of applying passive analogue modulation to reduce droop of the output waveform. The publication [18] presents the successful demonstration of applying active analogue modulation together with passive analogue modulation to compensate both the droop and ripple of the output pulse of an inductive adder. Both modulation methods are presented and, especially, applying the active analogue modulation method to compensate ripple components of the output waveform is explained in detail. The paper highlights the measured waveform of a prototype inductive adder for the case when active analogue modulation was applied. The flat-top stability for a 1.8 kV output pulse, the total duration of which is 400 ns including rise and fall times, is $\pm 0.05\%$ for 160 ns flat-top duration. This measurement is explained in detail in Chapter 5.

The first three chapters of this dissertation conclude the previously presented work to a seamless entity by presenting an extensive literature survey of existing pulse power modulators and a comprehensive design guide for the high-precision inductive adder. The fourth chapter, which is about the simulation studies, also mainly refers to previously presented work but the studies are presented in more detail. The fifth chapter presents the experimental results of the measurements on the two prototype inductive adders and most of the measured waveforms are published for the first time. This dissertation provides an experimental proof of applying the active analogue modulation method to compensate both droop and ripple of fast, high-voltage, pulses of an inductive adder.

Author's Contribution

The author is the main contributor to the research study presented in this dissertation and he is the sole contributor to most subjects. The author has studied independently the contributors to the droop and ripple of an inductive adder and has demonstrated both theoretically and empirically compensation of the droop and attenuation of a ripple frequency of the

output waveform of an inductive adder.

The role of Dr. Michael Barnes, who has been supervising the research work at CERN, has been mainly to share existing knowledge about pulse power technology with the author and, therefore, to help the author to focus on the subjects which have been the most important for the progress of this research study. He has also suggested several ideas which have been used in this dissertation. Dr. Barnes greatly helped to link this research tightly to the optimisation studies of the CLIC DR striplines, which are cited in Chapter 2. He also suggested the idea of measuring the very low inductance of the pulse capacitors and the primary circuit of an inductive adder indirectly by measuring the transient response of a resonant circuit. The method is explained briefly in Chapter 4. Dr. Barnes proposed to use FastHenry 3D simulation code to estimate the primary loop inductance of an inductive adder. This study is presented in Chapter 4. Dr. Barnes also made a proposal for measuring the output pulses of two prototype inductive adders, which were operating with opposite polarity, with a single current transformer in order to reduce the dynamic range of the measurement of active droop compensation. The results of these measurements are presented in Chapter 5.

Prof. Seppo J. Ovaska has guided this research from the academic point of view and provided constructive feedback in the writing and finishing phases of this dissertation.

2. Requirements and Topology

Selection for the CLIC DR Kicker Systems

2.1 The Compact Linear Collider (CLIC) Project

CLIC is a study for an electron-positron collider with nominal centre-of-mass energy up to 3 TeV [7]. The goal of this 48 km long linear accelerator (linac) facility would be to explore the new energy region in the multi TeV range beyond the capabilities of existing particle accelerators. The main accelerator of the CLIC facility is considered to be compact despite its physical length, because the accelerating gradient of CLIC is required to be 100 MV/m. This is far beyond the accelerating gradients of existing accelerators and would allow a relatively short length for the linac. CLIC would provide a unique combination of high energy and precision and it could, for example, complete unknown features of the recently discovered Higgs boson or possibly unveil more Higgs bosons [19]. Fig. 2.1 shows the schematic of the proposed CLIC facility.

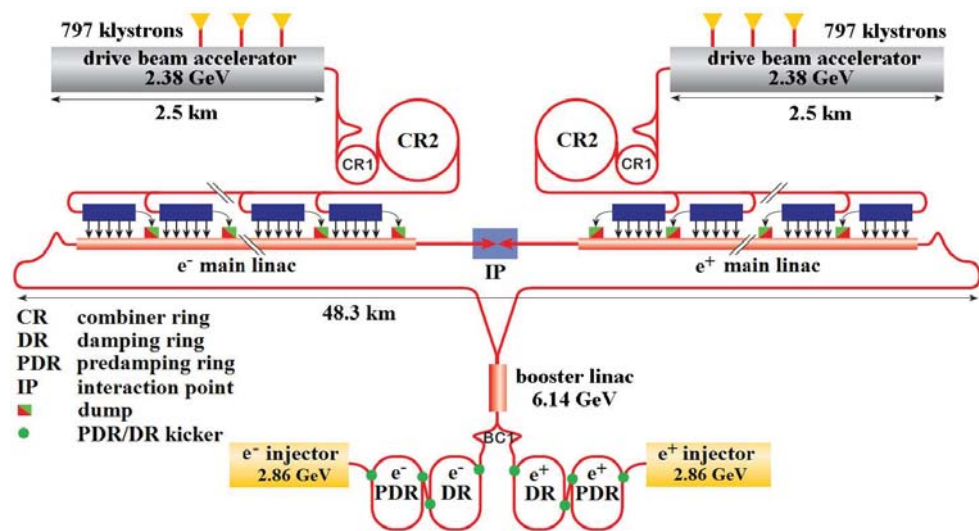


Figure 2.1. Schematic of the CLIC facility. Revised after [8].

The large accelerators consist of several stages, each of which can operate with a certain range of the beam energy. CLIC has two accelerator chains, one for electrons and another one for positrons. Each chain consists of an injector, a Pre-Damping Ring (PDR), a Damping Ring (DR), a booster linac and the main linac. Damping ring kicker systems, shown as green dots in Fig. 2.1, are used to inject and extract the beam from one stage to another, and they will employ striplines fed by pulse power modulators. The damping rings are necessary to achieve the very low emittance for the particle beam. Emittance is the measure of the size of the particle beam in an accelerator and it defines the spread of the particles in phase-space. In phase-space coordinates, each spatial direction, namely vertical, horizontal and longitudinal dimensions, has two variables which correspond to the position and the momentum of the particle. The injection and extraction systems should ideally minimise beam loss and they should place the particles onto the correct trajectory with the correct phase-space parameters [20].

In damping rings, the particle bunches pass through wiggler magnets, which force the beam to undulate. This causes the particles to emit synchrotron radiation and lose their energy. The trajectory of the beam is reduced in all dimensions, but the loss of longitudinal trajectory is compensated by accelerating the beam in radio frequency (RF) cavities. Therefore, the damping rings make the horizontal and vertical dimensions of the beam smaller and preserve the longitudinal trajectory. Effectively, it makes the cross-sectional size of the beam size smaller without reducing the energy of the particles and hence the emittance of the beam is decreased [21]. The physical explanation for the small emittance is that the particles of the beam are close to each other and they have very similar momentum spread.

In the CLIC machine, the pulse power modulators for the DR kickers must provide extremely flat, high-voltage, pulses. The pulse current and voltage amplitudes must not deviate from the set flat-top value during the pulse more than specified, because any excess variation in the magnetic and electric field could cause beam emittance blow-up. Also any deviation in the magnetic and electric field from zero between the pulses could cause small offsets with respect to the closed orbit of the beam [20]. The emittance of the beam is reduced in the damping rings, and the extraction kickers must keep the emittance within the specifications. Any emittance blow-up caused by the DR kickers cannot be corrected in the linacs of

CLIC. Therefore, the specifications for the DR extraction kicker system are the most demanding.

2.2 Specifications for the CLIC DR Kicker Systems

2.2.1 The Stripline Kicker System

The damping ring kicker systems require low beam coupling impedance, high-voltage and high-current pulses and must be of high stability [22]. In order to achieve the required low beam coupling impedance the damping ring kickers will be stripline devices, as reported in [7], [23] and [24]. Very high-precision pulses are required for the extraction kickers from the CLIC damping ring and hence the impedance of the system must be well matched, or any impedance mismatches must be of a short electrical delay relative to the required rise and fall times. The pulse generator is an extremely important element in achieving the required high-voltage, high-current and extremely high-precision pulses.

The Parts of the Stripline Kicker System

Figure 2.2 shows a simplified schematic of a stripline kicker system with a pulse power modulator. A stripline kicker consists of two parallel metallic electrodes which are connected at each end to the external circuit by feedthroughs. The two electrodes are driven to an equal magnitude of voltage but of opposite polarity. The pulse power modulators feed pulses towards the striplines. For simplicity, Fig. 2.2 only shows one pulse source which feeds the upper electrode. For feeding both electrodes, either one bipolar or two unipolar pulse power modulators are required. The pulse propagates through the striplines and is then absorbed by a terminating resistor. Ideally, the stripline kicker is seen by the pulse power modulator as a transmission line and if the impedance of the stripline kicker is perfectly matched to the terminating resistor and the cables between them, the pulse from the modulator propagates to the terminating resistors without reflections.

Contributors to the Flat-top Instability of the Kicker System

There are many possible sources for causing ripple, or droop and ripple, and therefore corrupting the stability and repeatability of the pulse and eight possible sources are listed below [7], [25]. The first contributor is

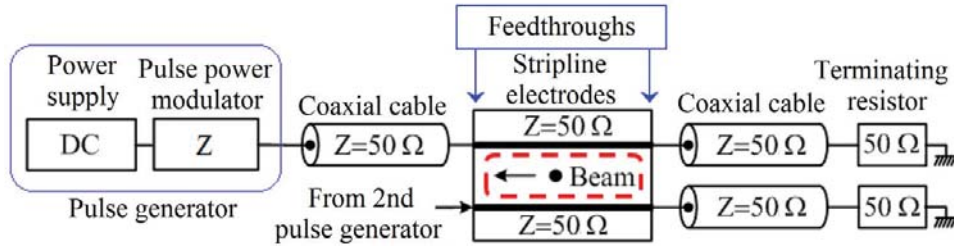


Figure 2.2. Stripline kicker system.

the pulse modulator itself, depending on its topology, compensation methods (if applied) and their precision range. The second is precision and repeatability of the output voltages of the high-voltage power supplies which are needed to charge the energy storages, for example capacitors or pulse forming lines, in the pulse power modulator. The third contributor is attenuation and dispersion of the pulse in the transmission lines and in the pulse power modulator depending on the topology. The fourth source is dynamic characteristic of a switch or switches. The fifth contributor is temperature effects upon a switch or switches of the pulse power modulator. The sixth source is high-voltage, vacuum feedthroughs of the stripline kicker and high-voltage connectors of the pulse power modulator and the terminating resistors. The seventh contributor is frequency dependence of the impedance of the terminating resistors and their long-term stability and temperature effects. The last one is the overall impedance matching of the system, including the transmission lines. The characteristic impedance of the pulse power modulator, transmission lines, striplines and terminating resistors must be matched to minimise reflections, which could cause ripple on the flat-top of the kicker pulse.

The Operation Principle of a Stripline Kicker

The two electrodes of the stripline kicker are fed by two pulse power modulators, one of which feeds positive and the other negative pulses. The electrodes are terminated by two separate load resistors. Fig. 2.3 shows a cross-sectional view of striplines. When the two electrodes of the stripline are fed from the same end by voltage pulses with opposite polarities, an electromagnetic wave with transversal electric and magnetic fields (TEM) starts propagating through the electrodes towards the other ends, which are terminated by the load resistors. In Fig. 2.3, the stripline kicker is operating in a TEM mode, and the particle beam travels in the opposite direction with respect to the TEM wave. In this case, the contributions

of the electric and magnetic fields of the stripline kicker to the beam add to each other [26]. The reasoning for this conclusion is shown with the equations below.

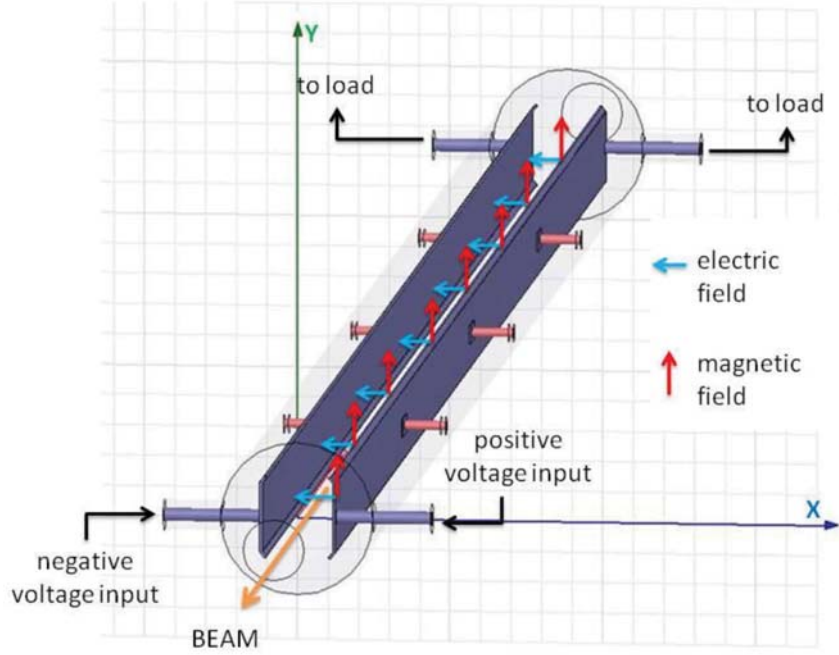


Figure 2.3. Schematic of a stripline kicker in operation. Revised after [27].

The beam which passes between the electrodes is deflected by the Lorentz force $\vec{F}_{(E+B)}$, which is given by the following equation:

$$\vec{F}_{(E+B)} = q(\vec{E} + \vec{v} \times \vec{B}) \quad (2.1)$$

In this equation, q is the charge of a particle, which in the case of CLIC DR striplines is either an electron or a positron. $\vec{E}$ is electric field between the electrodes, $\vec{B}$ is the magnetic field which results from the currents flowing in the electrodes, and $\vec{v}$ is the velocity of the particles. In Fig. 2.3, the electric field would deflect the electron beam in the plane which is parallel to the electric field and with force $q\vec{E}$, the direction of which is towards the positive X axis. The magnetic field would deflect the electron beam with force $q\vec{v} \times \vec{B}$, the direction of which is perpendicular to the magnetic field and to the beam. In Fig. 2.3, the deflecting force of the magnetic field upon the electron beam points towards the positive X axis.

If the passing beam has the velocity of light c , the contributions of the electric and magnetic field of a stripline kicker have exactly the same amplitude [26]. For this statement, it is assumed that the ratio of the electric and magnetic fields is linked together according to the following equation:

$$|\vec{B}| = \frac{|\vec{E}|}{c} \quad (2.2)$$

In this case, the passing beam is deflected by the force, the magnitude of which is given by the following equation:

$$|\vec{F}_{(E+B)}| = q(|\vec{E}| + c \times \frac{|\vec{E}|}{c}) = 2q|\vec{E}| \quad (2.3)$$

This result means that in the stripline kicker, the contributions of the deflecting forces of the electric and magnetic fields to the beam add to each other and they effectively have exactly the same amplitude, as concluded briefly in [26]. Recently, detailed simulations have shown that the electric and magnetic deflections only have the same magnitude when the odd mode impedance of the striplines is terminated in its characteristic impedance [28].

The Even and Odd Mode Impedances of a Stripline Kicker

The cross-section of the striplines will be optimised to achieve the desired even-mode characteristic impedance and the required field homogeneity [24]. The even-mode characteristic impedance of the stripline kicker defines the interaction of the beam with the striplines when the striplines are not driven by the pulse generator. In the even-mode, the characteristic impedance of the kicker depends on the proximity of each stripline to the beam pipe. The impedance which is seen by the beam when it passes through the kicker is called the beam coupling impedance and it should be low in order to avoid beam instabilities [7]. High beam coupling impedance could result beam energy loss and beam shape perturbation. The even-mode characteristic impedance is chosen to be nominally 50 Ω for the CLIC DR kicker striplines so that standard transmission lines and feedthroughs can be used. Ideally, for the beam, the terminating resistors should be matched to the even-mode impedance of the striplines.

When the striplines are pulsed to equal magnitude but opposite polarity voltages, the characteristic impedance of the kicker is odd-mode [7]. In the odd-mode, there is a virtual ground mid-way between the striplines (Fig. 2.4). The characteristic impedance of each stripline is dependent upon the proximity of each stripline to both the beam pipe and the virtual ground. The odd-mode characteristic impedance will be smaller than the even-mode characteristic impedance. Since the transmission lines will be

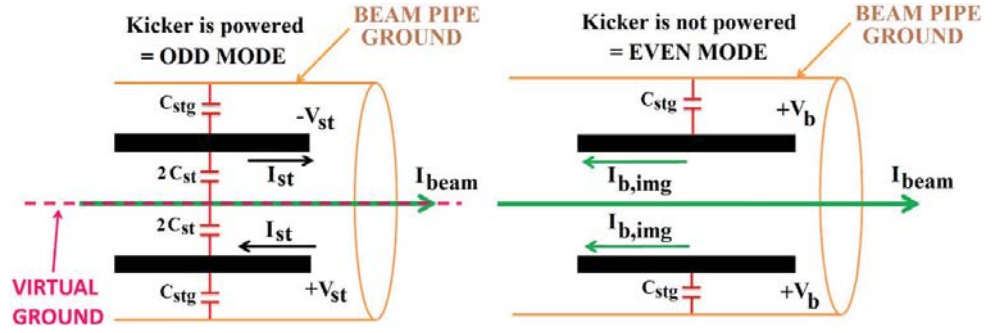


Figure 2.4. Stripline kicker in odd (left) and even (right) modes. Revised after [29].

commercially available coaxial cables, it may not be feasible to match the odd-mode characteristic impedance of the striplines to the characteristic impedance of the other elements of the kicker system [7]. This means that the odd-mode characteristic impedance of the striplines, which is seen by the pulse generator, may not be matched to the terminating resistor and the modulator. The optimised design of the CLIC DR extraction kicker striplines, which theoretically meets the required field homogeneity for the striplines, has the even-mode characteristic impedance of $50 \, \Omega$ and the odd-mode impedance of $41 \, \Omega$ [30].

Mismatched impedance causes reflections, which makes the settling time of the kicker waveform longer. The settling time is the time period after the rise time of the pulse which is needed to damp the oscillations of the pulse flat-top to within the specifications. The specifications and pulse definition for the CLIC DR kicker modulator are presented in detail in the next Section 2.2.2. The settling time depends on several parameters of the kicker system, for example rise time of the pulse and the lengths of the cables between the parts of the system. As a first estimate, the settling time is expected to be as long as the desired rise time, 100 ns. Fig. 2.5 shows the images of the prototype stripline kicker for the CLIC DR extraction system. Design and manufacturing of the prototype striplines is a part of the feasibility studies of CLIC [7].

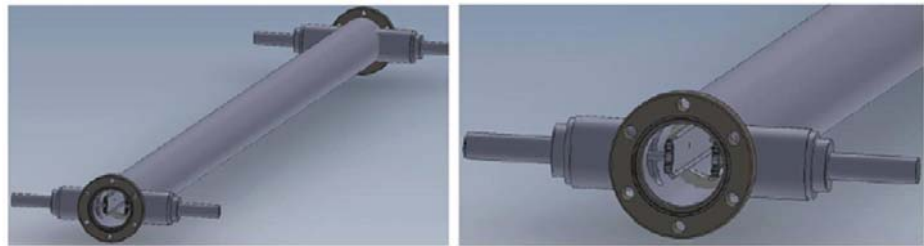


Figure 2.5. 3D Drawings of the prototype of the CLIC DR extraction kicker striplines [31].

2.2.2 Electrical Specifications and Pulse Definition

The proposed CLIC design presents two different baselines for the damping rings. The RF frequency of the baseline, 1 GHz or 2 GHz, corresponds to the bunch spacing of the particle beam in the damping rings, which is 1 ns or 0.5 ns, respectively. Table 2.1 shows the 2 GHz specifications for the CLIC DRs and PDRs [7].

Table 2.1. 2 GHz specifications for CLIC PDR and DR kicker systems.

	PDR	DR
Beam Energy (GeV)	2.86	2.86
Deflection angle (mrad)	2	1.5
Field rise time [incl. settling time] (ns)	700	1000
Field fall time [incl. settling time] (ns)	700	1000
Pulse flat-top duration (ns)	160	160
Pulse flat-top repeatability (%)	± 0.01	± 0.01
Pulse flat-top stability, Inj. [incl. d&r] (%)	± 2	± 0.2
Pulse flat-top stability, Ext. [incl. d&r] (%)	± 0.2	± 0.02
Field inhomogeneity, 3.5 mm radius (%)	± 0.1 (Inj.)	± 0.1 (Inj.)
Field inhomogeneity, 1 mm radius (%)	± 0.1 (Ext.)	± 0.01 (Ext.)
Repetition rate (Hz)	50	50
Pulse voltage per stripline (kV)	± 17	± 12.5
Stripline pulse current [50 Ω load] (A)	± 340	± 250

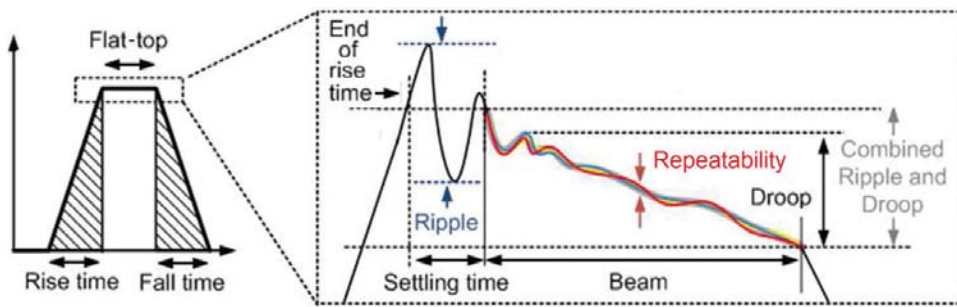


Figure 2.6. Pulse definition for the CLIC DR kicker systems.

In Table 2.1, the specifications for the DR extraction kicker system, of the 2 GHz baseline, call for a 160 ns duration flat-top pulse of 12.5 kV, 250 A, with a combined droop (d) and ripple (r) of not more than ± 0.02 ($\pm 2 \times 10^{-4}$). Fig. 2.6 shows the detailed pulse definition for the DR kicker requirements. The stripline is a passive device, therefore the pulse gener-

ator is the most important element in achieving the required high-voltage, high-current and extremely high-precision pulses.

In Fig. 2.6, pulse rise time is the time which is needed to reach the required flat-top voltage. According to specifications, the field rise and fall times including settling time may be up to 1000 ns for the DR kicker. However, for several reasons the target rise and fall times are considerably shorter, as is explained in the following sections. Settling time is the time which is needed to damp the oscillations to within the flat-top specifications and beam time is the time window during which droop and oscillations must be within specifications. To minimise settling time, the impedance of the system has to be well matched. According to specifications the beam time is 160 ns, for the 2 GHz option, however because of the impedance mismatch between the kicker system elements, the flat-top duration of the pulse may be required to be longer, up to 260 ns, including 100 ns of settling time. Fall-time is the time which is needed for voltage to return to zero. Off-time is the time between two consecutive pulses and this is not shown in Fig. 2.6.

The DR extraction kicker has the most demanding specifications for the flat-top stability and it was chosen for the subject of this dissertation. In this dissertation, "CLIC DR kicker" refers to the CLIC DR extraction kicker, if it is not otherwise mentioned. Flat-top stability of the output waveform is required to be within $\pm 0.02\%$ ($\pm 2 \times 10^{-4}$). In fact, this number defines the allowed instability of the flat-top of the output waveform, including the droop and ripple. In literature this is often referred to as pulse stability and, for clarity, this term is used in this dissertation. Droop is a sag of the pulse voltage during the flat-top and ripple is any other variation of the pulse flat-top voltage. The stability requirement of $\pm 0.02\%$ for the flat-top of a 12.5 kV pulse corresponds to ± 2.5 V range absolute accuracy and it is extremely tight. A literature survey of existing pulse modulators was carried out and the flat-top stability requirement for the CLIC DR extraction kicker was found to be tighter than for any high-voltage pulse modulator operating with similar pulse lengths, described in the literature [10]. In the literature, the pulse flat-top stability is sometimes referred to as pulse flatness.

In this dissertation, pulse flat-top repeatability is defined as the maximum difference which is allowed between any two pulses when the set value of the output voltage of the pulse modulator is kept unchanged. The repeatability is required to be within $\pm 0.01\%$ ($\pm 1 \times 10^{-4}$) for the CLIC DR

extraction kicker. In the literature, this is also referred to as pulse to pulse stability. Sometimes in the literature the term reproducibility has the same meaning as repeatability. However, reproducibility can also be defined as the allowed difference of the pulses in the case when the operation point of the modulator is changed and then returned to the previous setting.

In order to meet these demanding specifications for the CLIC DR extraction kicker pulse power modulator, especially the flat-top stability requirements, a combination of broadband impedance matching, optimised electrical design and advanced control techniques is required.

2.2.3 Other Requirements for the Pulse Power Modulator for the CLIC DR Extraction Kicker System

In addition to electrical specifications shown above, there are several other requirements for the CLIC DR kicker pulse modulator. These relate to machine safety, the reliability of the modulator and modularity of the design, especially concerning the use of the same design in other applications in the CLIC project. The desired rise and fall times and the off-time voltage between two consecutive pulses are also defined in this section.

Machine Safety, Reliability and Redundancy

The high energy beam in CLIC may cause catastrophic failure for the machine in the case of malfunction as the beam has considerable destructive capacity already in the damping rings [32]. Therefore the kicker systems, which steer the beam during injection and extraction processes, should be very reliable [7]. The pulse modulators which feed the kicker striplines should be fault-tolerant: a failure in a single switch or a single trigger line should not prevent the pulse modulator from supplying the full pulse voltage or a large fraction (e.g. more than 90 %) of the flat-top voltage to the striplines. The kicker system will be placed close to the beam line to minimise cable lengths and it cannot be accessed frequently. This also requires a fault-tolerant pulse modulator, which can tolerate a failure of a single switch or another component and can still continue operating reliably for some time before maintenance or repair work. In addition the modulator must have adequate radiation shielding around it.

Modularity

There are other kicker systems with tight specifications in the damping rings of CLIC, namely DR injection kicker and PDR injection and ex-

traction kickers. All these systems require pulse power modulators and, preferably, the same design could be applied for all the required pulse modulators. The specifications for the DR injection and PDR injection and extraction kicker systems are relaxed in comparison with the DR extraction kicker, but still demanding [7]. For the DR injection kicker, the pulse voltage and currents are the same as for the DR extraction kicker, but the repeatability and stability requirements are an order of magnitude less strict. For the PDR kickers, the pulse voltage is ± 17 kV for a $50\ \Omega$ load. The repeatability and stability requirements for the PDR extraction kicker are similar to the DR injection kicker, and for the PDR injection kicker the requirements are an order of magnitude less strict than for the PDR extraction kicker.

An abort kicker is also needed for CLIC DR systems and the space available in the lattice of the accelerator may be very limited [33]. The abort kicker study [34] is a proposal for a kicker system, in which the same pulse modulator could be used to generate pulses with two different voltages for the DR extraction kicker magnet. The stripline kicker would operate with two different deflection angles, depending on the operation mode: to extract the beam, or to abort it to the dump system.

Rise and Fall Times and Pulse Duration

According to [7], the maximum allowed rise and fall times are 1000 ns, for 0.02-99.98 % of the pulse field. However, the measurable ranges for rise and fall times were estimated to be 0.1-99.9 % and this definition was used in this dissertation. Long rise and fall times increase stress for switches of the pulse modulators and termination resistors of the kicker system. Also, depending on the topology of the modulators, shorter rise and fall times would require smaller energy storage components, e.g. capacitors, because the total discharge time would be shorter. If the modulators include magnetic cores, shorter rise time would result in smaller magnetising current flowing in the magnetic cores at the end of the rise time, which could cause smaller droop for the output pulse, and also would decrease the cross-sectional area required for the cores. In addition, excessive power loss may cause temperature-dependent effects on the striplines, the terminating resistors and other components. Therefore, the field rise and fall times (0.1-99.9 % of the pulse amplitude) are desired to be significantly shorter than allowed in the specifications, less than 250 ns. The output impedance of the pulse power modulator must be well matched

to the cables, in order to minimise the settling time and the total pulse duration.

The maximum pulse length, which is the sum of the rise time, the flat-top of the pulse and the fall time, is allowed to be $2.2 \mu\text{s}$ [7]. Ideally, after this the voltage must return to zero and during the off-time of the kicker the field must be close to zero. The allowed deviation from zero is as small as for the flat-top variation, corresponding to $\pm 2.5 \text{ V}$ or $\pm 0.02 \%$ of the flat-top magnitude. However, according to [35], the minimum time required to reach the design extraction emittance for the beam in the CLIC DR is approximately 15 ms. With a 50 Hz repetition rate, this could allow up to 5 ms long fall time for the field of the CLIC DR extraction kicker. This means that the off-time voltage requirement for the pulse modulator may be significantly relaxed. Therefore, this dissertation emphasises the flat-top specifications of the pulse and the off-time requirements have not been considered in detail.

2.2.4 Double Kicker System

It is possible that the final flat-top stability requirements of the output waveform for the CLIC DR extraction kicker modulator cannot be reached with a single kicker system. In that case, a double kicker system (Fig. 2.7) presented for the first time in [36] and developed further in [37] could be a means of reducing ripple and relaxing the pulse flat-top stability requirements of the pulse modulator. The double kicker consists of two identical kicker magnets which are fed with a single pulse power modulator, or two identical pairs of striplines, which are fed with one pair of pulse power modulators. The operation principle of the double kicker system is presented in Fig. 2.7. Ideally, both kickers steer the beam with the same angle. The variations of the kick angle of a kicker are caused by the magnitude variations of the field and the phenomenon is called kick angle jitter. As it has been explained in earlier sections of this dissertation, the variations of the field can be caused e.g. by impedance mismatch between the kicker and the modulator. A delay is applied for the pulse which is fed into the second kicker, e.g. in order to kick the beam for the second time at the time point, in which the phase of its natural transverse oscillation is advanced by a half-wave length, by π . In that manner, the second kicker ideally completely compensates for the kick angle jitter of the first kicker.

The prototype double kicker system, tested at the KEK-Accelerator Test Facility in Japan, achieved a factor of 3.3 reduction in kicker angle varia-

tion, from $4.7 \pm 0.8 \mu\text{rad}$ to $1.4 \pm 0.8 \mu\text{rad}$, and the reached fractional stability of the deflection angle of the double kicker system was $0.028 \pm 0.016 \%$, of the 5 mrad deflection, in single bunch operation [38]. The flat-top length of the kicker pulse was 60 ns and the beam energy 1.28 GeV. For the CLIC DR extraction kicker, the deflection angle is 1.5 mrad and the flat-top stability requirement of $\pm 0.02 \%$ for the kicker pulse corresponds to $\pm 0.3 \mu\text{rad}$ for the deflection angle variation. In addition, the pulse flat-top length for the CLIC DR extraction kickers is at least 160 ns (2 GHz baseline) and the beam energy 2.86 GeV [7].

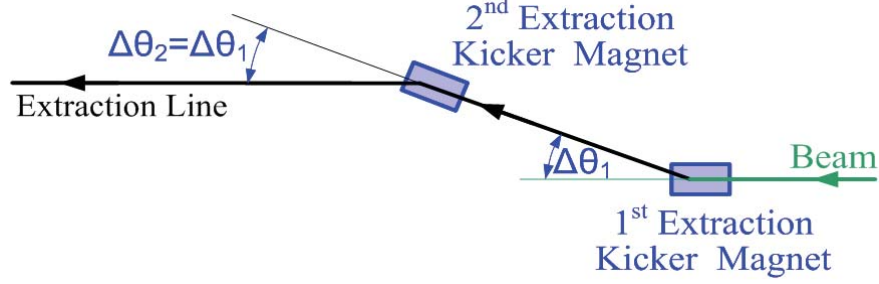


Figure 2.7. Operation principle of a double kicker system.

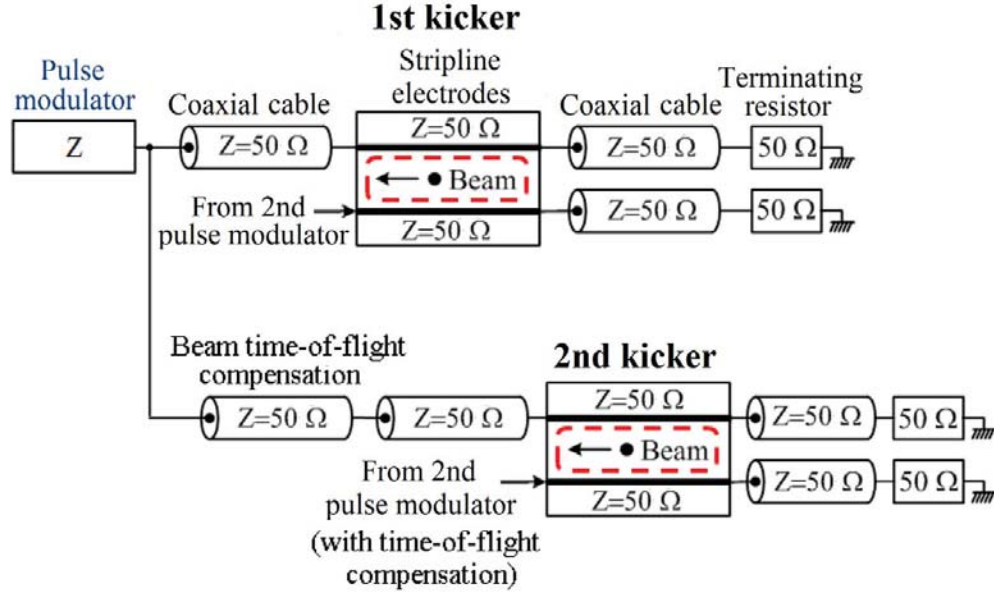


Figure 2.8. Schematic of a double kicker system with stripline kickers.

There are several reasons why the kick angle jitter of the first kicker is not necessarily completely cancelled by the second kicker. Fig. 2.8 shows a schematic of a double kicker system with stripline kickers. In order to obtain complete cancellation of magnitude jitter, the interconnecting cables, high-voltage feedthroughs, stripline kickers and terminating resis-

tors must be identical but this is not the case in reality. Also, ideal beam optics is required. Moreover, although both striplines are fed by the same power modulators, the relative timing of the arrival of the pulses at the striplines must be synchronised with the time of flight of the beam. This requires a longer length of coaxial cables to the second kicker (Fig. 2.8), which results in higher attenuation of the pulses and the ripple. In addition, the requirement to have either two kicker magnets or two stripline kickers increases costs and complexity. Thus it is preferable to use a single kicker system if possible.

2.3 Topology Search

A review of literature has been carried out to determine the most suitable topology for the pulse power modulator for the CLIC DR extraction kicker system. The search has covered especially the existing pulse power modulators used for particle accelerators and kicker systems. Comparisons have been made between the topologies considering their suitability for generating fast pulses with the required flat-top stability and conclusions have been drawn to define the best means of achieving the demanding specifications. It has been found that the flat-top stability specifications for the CLIC DR extraction kicker system are an order of magnitude stricter than for any existing single kicker system presented in the literature. Therefore, new developments are needed in order to meet the requirements regarding the pulse flat-top stability.

2.3.1 Line-Type Modulators

Considering only pulse voltage and current, pulse length and repetition rate, there are a couple of topologies which could be applied for the CLIC DR extraction kicker pulse modulator. In line-type modulators all the stored energy is fed to the load during the pulse. Commonly used line-type modulators are pulse forming line (PFL), pulse forming network (PFN) and Blumlein line. A detailed presentation of these types of pulse modulators is given in [39] and the schematics of the PFL and PFN, according to European definitions for these topologies, are shown in Fig. 2.9 and 2.10, respectively. Line-type topologies include a closing high-voltage switch and the commonly used switches in them are spark gaps, thyratrons and thyristors [40].

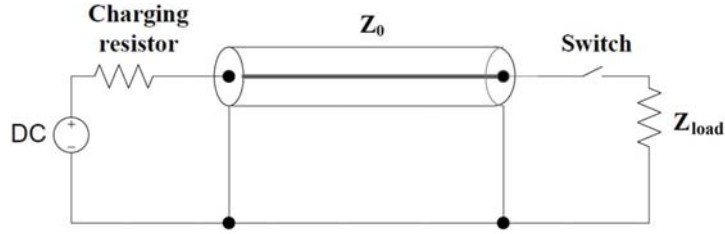


Figure 2.9. Schematic of a pulse forming line.

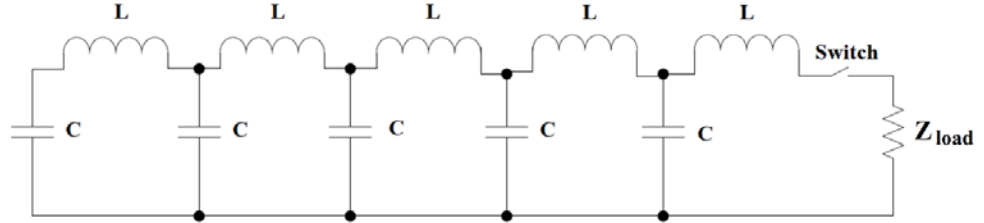


Figure 2.10. Schematic of a pulse forming network.

The advantages of the line-type modulators are that they are in general simple circuits to design and build, have limited stored energy and have good efficiency [40]. The PFLs can produce relatively rectangular pulses with short rise and fall times and they are generally used to generate short pulses, typically 2-3 μs [20], because longer pulses can suffer from considerable droop due to losses in the line. The PFLs may also be cost-effective in comparison with solid-state modulator topologies [41].

A disadvantage of line-type modulators is that they must be completely recharged between the pulses. Also, the impedance matched PFL or PFN needs to be charged to twice the load voltage and thus the high-voltage switches in the PFLs and PFNs must also operate at twice load voltage. The impedance of the modulator needs to be matched to the load in order to minimise reflections. The PFL has limitations considering the characteristic impedance, because the transmission line or lines used in the topology should be matched to the load and the coaxial transmission lines are commercially available only with certain impedances. Therefore, a pulse transformer may be required to match the impedance to the load. The PFN tends to have slow rise and fall times unless it has many sections. For example, with a PFN consisting of five sections, each of them including an inductor and a capacitor, the minimum rise time from 10 % to 90 % of the pulse amplitude is 8 % of the pulse length [40].

Taking into consideration the stability and repeatability requirements of the CLIC DR kicker system, the line-type modulators have severe limitations. The output pulse shape of the PFN is prone to having over-

shoot and ringing [40], and it is likely to have more ripple than with the PFL [7], therefore the PFN has not been considered further. A PFL-based pulse power modulator would have a significant attenuation and dispersion in the pulse voltage. Theoretically, this could be compensated with frequency dependent attenuation using a suitable length of transmission line and the resulting droop would be within the specifications up to a 240 ns long pulse [23]. However, this method makes the falling edge of the pulse longer, which can be a potential problem, and there is no easy means of controlling ripple [23], therefore the PFL has not been studied further.

Historically a Marx generator (Fig. 2.11) was also considered to be a line-type modulator from the point of view that it was usually operated in a way that it discharged all the stored energy into the load. It consists of a stack of capacitors, which are charged in parallel and discharged in series. The Marx generator is presented in detail in [39]. The rise time of the Marx generator can be very short, a few nanoseconds. However, the load impedance determines the output waveform and the fall time can be much longer than the rise time [40]. To give an example, a Marx generator presented in [42] can feed up to 221 kV, 20 ns duration pulses with a 71Ω source impedance. The minimum reported rise time was 2.4 ns and according to the output waveforms shown in [42], the minimum fall time was approximately 12 ns with a 50Ω load and 20 ns with a 100Ω load. The switches used in the Marx generators are historically spark gaps but they can also be built using solid-state switches. The pulse shape of the solid-state Marx modulator can be modulated during the pulse and this variation of the Marx generator is presented in the next section.

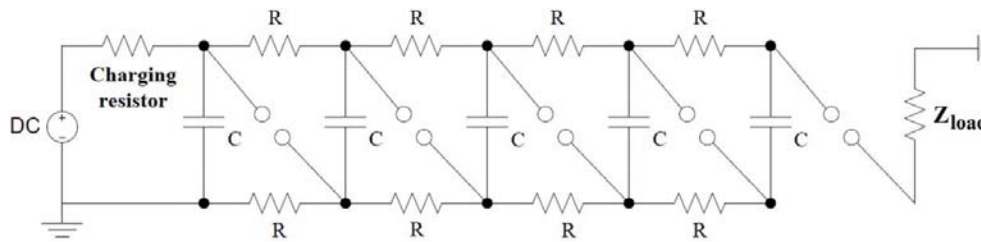


Figure 2.11. Schematic of a Marx generator.

2.3.2 Solid-State Modulators

Solid-state modulators differ from the line-type modulators in the sense that they have a switch which can be opened when it is conducting full

load current and therefore only a portion of the stored energy is delivered to the load during the pulse. Solid-state modulator topologies provide a possibility to modify the pulse length and thus to reach very good efficiency, because the pulse form can be close to an ideal rectangular pulse with very short rise and fall times. A short introduction to solid-state modulator topologies is given in [40], covering a series switch topology and an inductive adder. A detailed description of a solid-state Marx modulator is presented in [43].

Solid-state modulators provide many advantages over line-type modulators, and especially over single-switch based modulators. Modulators using for example thyratrons, ignitrons or spark gaps have limitations with regard to combinations of desired repetition rate, efficiency, pulse width agility, average power and cost, and in some cases even switch availability [44]. In general, the solid-state modulators may also provide better overall reliability and efficiency, and longer expected life-time over modulators which use a single thyatron switch [45]. Thyatron switches also require very stable operating conditions to be reliable [46]. The source impedances of the solid-state modulators are low and therefore, unlike for example a PFL, the source voltage does not need to be significantly higher than the output voltage. The most common switches used in solid-state modulators are metal-oxide-semiconductor field-effect transistors (MOSFETs) and insulated-gate bipolar transistors (IGBTs).

The following sections present a selection of the most advanced examples of series switch topologies, solid-state Marx modulators and inductive adders found in the literature. Transmission line adders and matrix transformer topologies are also briefly discussed.

Series Switch Topology

The simplest solid-state modulator topology consists of a capacitor bank and a stack of solid-state switches in serial connection. The modulator can be connected to the load also with a step-up transformer. Fig. 2.12 shows a simplified schematic of a series switch modulator topology.

The advantages of the series switch topology are that it is relatively simple and it can be used to generate both short and long pulses. If there is not an output transformer, the maximum pulse length is a function of the value of the capacitor bank and the load impedance. The absence of a transformer also means that the fault currents are not dependent on the saturation of a transformer.

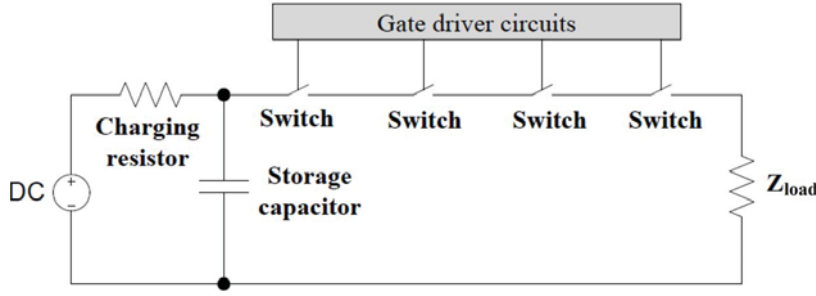


Figure 2.12. Schematic of a series switch topology.

The disadvantages of the series switch topology include the fact that the control electronics of the switches are floating and not referenced to the ground, therefore the power for the gate drive circuits and trigger signals need to be isolated from the switches. This requires use of transformers or fibre optics. The timing of the trigger pulses has to be well synchronised to keep the voltage stress over the switches below the safe operation margins. Especially, great care must be taken in designing the fibre optic link for the trigger signals, in order to avoid non-controllable time jitter between the stacked switches [47]. In addition, if a single switch in the stack fails, the voltage stress over other switches is increased and this may cause the other switches to fail, unless redundancy is included.

Examples of Kicker Modulators Based on Series Switch Topology

Pulse modulators based on the series switch topology have previously been used in various kicker systems. They have usually been built with field-effect transistors (FETs) or MOSFETs. The topology has been used in various voltage ranges, repetition rates and pulse lengths. An extensive development of pulse modulators based on this topology has been done at TRIUMF accelerator laboratory in Canada. The built modulators have reached very high repetition rates and extremely low ripple as is shown below.

A pulse power modulator developed at Saskatchewan Accelerator Laboratory generated up to 20 kV pulses with 10 A of load current [48]. The flat-top length could be adjusted from 0.5 μs to 6 μs . The repetition rate was up to 360 Hz and the rise and fall times were 100 ns and 1 μs , respectively. The voltage droop of the flat-top was reported to be 0.5 % and the ripple 0.3 %.

The first series switch topology based modulator developed at TRIUMF was presented in [49] and [50]. This modulator was based on the design shown in [48] but it was modified considerably. A push-pull configuration

was used, which reduced the fall time of the pulse, especially with capacitive loads. The output voltage was 6 kV, pulse width variable from 250 ns to 1 s and repetition rate adjustable from less than 1 Hz to 20 kHz. Rise and fall times from 10 % to 90 % of the pulse voltage were about 30 ns. The load was the deflector plates of a beam chopper. The reached stability for the pulse flat-top has not been reported.

A bipolar pulse modulator was developed for KAON factory at TRIUMF [51]. This modulator generated ± 15 kV pulses with adjustable pulse length from 25 ns to 120 ns. The rise and fall times were less than 32 ns from 10 % to 90 % of the pulse voltage and the repetition rate was 930 kHz. The flat-top ripple was ± 8 % for 48 ns long pulses.

Another version of the FET stack based modulator was a unipolar 10 kV modulator which operated up to 925 kHz repetition rate [52]. The modulator generated adjustable 50-500 ns long pulses with measured rise and fall times of 38 ns, from 10 % to 90 % of output voltage. The achieved flat-top stability was not reported.

A pulse power modulator designed for a kicker of a charge booster at ISAC facility at TRIUMF generated unipolar -3.5 kV pulses with a repetition rate up to 52 kHz [53]. The pulse width was adjustable from 350 ns to longer than 10 s and the rise and fall times were 63 ns from 10 % to 90 %. The ripple and droop of the output pulse have not been reported.

A MOSFET stack based pulse modulator for Muon Lifetime measurements at Paul Scherrer Institute in Switzerland generated adjustable pulses up to ± 12.5 kV for deflector plates of a kicker system [54]. The load consisted of deflector plates, the capacitance of which was in total 108 pF. The length of the pulse flat-top was adjustable from 200 ns as minimum and the rise and fall times less than 40 ns from 10 % to 90 % of the pulse voltage. The repetition rate was up to 77 kHz. The modulator was developed further in order to improve the pulse flat-top stability. Finally, the pulse voltage overshoot, for the capacitive load, was reduced from 10 % to 2 % and the flat-top droop from 0.18 % to less than 0.001 % for a 22 μ s long output pulse [55]. The settling time of the output pulse was not reported.

A pulse power modulator operating at over 2 MHz repetition rate and based on stacked switch technology was developed in Extreme Energy Density Institute at Nagaoka University of Technology in Japan [56]. This modulator generates 5 kV pulses to a 70 Ω load. The peak current was 75 A, operation frequency up to 2.1 MHz, rise and fall times 33 and 43 ns,

respectively, and the pulse width of the load voltage was 240 ns.



Figure 2.13. Photo of a series switch stack comprising 15 FETs [57].

A series switch modulator based on MOSFET switches has also been built to generate very short pulses (Fig. 2.13). An example is a prototype pulse modulator for the damping ring kicker of the ILC [57]. This pulse modulator produced 4.8 kV pulses with pulse width of 14 ns and with rise and fall times close to 5 ns. The pulse repetition rate was up to 60 kHz and the post-pulse ripple, i.e. the ripple of the off-time voltage, below 5 %.

Table 2.2 shows a summary of the pulse modulator applications presented above. The specified voltage ranges and pulse lengths of the existing applications are comparable with the CLIC DR kicker systems but in many cases the series switch modulators have been used to drive capacitive loads, which means that there is no current flowing through the load during the pulse flat-top. Very high flat-top stability has been reached for the pulse modulator presented in [55]. However, in comparison with the CLIC DR kicker specifications, there are a few points to note: the load was capacitive hence droop was not an issue, the length of the pulse flat-top was 137 times longer than the length of the CLIC DR kicker pulse, and the settling time of the output pulse was not reported.

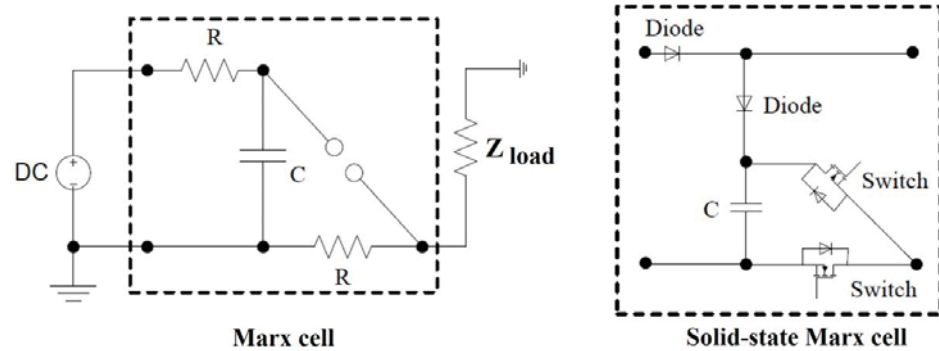
Solid-State Marx Modulator

Figure 2.14 presents schematics of single cells of a conventional Marx generator (left) and of a solid-state Marx modulator (right) [58]. The operation principle of the solid-state Marx modulator is similar to the conventional Marx generator: the pulse capacitors are charged in parallel and

Table 2.2. Summary of pulse modulators based on series switch topology.

Ref.	Output voltage (kV)	Flat-top current (A)	Pulse duration (ns)	Load	Reported flat-top stability (%)
[48]	20	10	500-6000	8 k Ω + 80 pF	0.5 (droop) 0.3 (ripple)
[49], [50]	6	0	250-10 ⁹	capacitive	n/a
[51]	± 15	0	25-120	capacitive	± 8 (ripple)
[52]	10	0	50-500	capacitive	n/a
[53]	-3.5	0	350-10 ¹⁰	capacitive	n/a
[54], [55]	± 12.5	0	200-DC	108 pF	0.001 (droop)
[56]	5	75 (peak)	240	70 Ω	n/a
[57]	4.8	n/a	14	100 Ω	n/a

discharged in series to achieve a high-voltage output pulse. The parallel charging of the capacitors can be implemented using resistors, inductors or semiconductor switches. In Fig. 2.14, the charging component is a switch. An advantage of the solid-state Marx modulator is that it does not have an output transformer. The maximum pulse length is restricted only by the size of the capacitors in each Marx cell and the output resistance.

**Figure 2.14.** A Marx cell with a spark gap (left) and a solid-state Marx cell (right). Revised after [58].

The disadvantages are similar to a series switch topology, namely the switches and control electronics of the stages are not referenced to ground. Therefore, the control signals need to be fed to each stage by a transformer or by fibre optics. Also, the current for the gate drivers needs to be sup-

plied by galvanically isolated transformers or by high-voltage capacitors in each stage. A failure in a single switch in the Marx modulator can cause, depending on the place of failure, either increased voltage stress over components in other layers, or the inability to charge the Marx cell capacitors. Thus appropriate redundancy must be included if the output voltage is to be maintained in the case of failure.

Examples of Solid-State Marx Modulators

Most of the solid-state Marx modulators presented in the literature have been designed for much longer pulse lengths and often for higher voltages than those required for the CLIC DR kicker pulse modulator. The applications in the particle accelerators are typically klystron modulators, which require tens to hundreds of kilovolts of output voltage and pulse lengths from microseconds to milliseconds. However, the solid-state Marx topology can also be designed to generate pulses with a flat-top of a few hundred nanoseconds and rise times of close to 100 ns have been reached, as reported in references to be presented below. A few examples have also been found in which the output pulse of the solid-state Marx have been modulated during the pulse either by switching on the Marx cells at different times or by regulating the output of the individual layers during the pulse [59].

A document from commercial supplier Applied Energetics presents solid-state Marx modulators for the voltage ranges up to 20 kV with output current from 10 A to 4 kA [60]. The output waveform is "square wave" but the flat-top precision or minimum rise and fall times have not been specified.

The prototype solid-state Marx modulator presented by Stangenæs Industries in 2004 produces 28 kV pulses across a 1 k Ω load [61]. The minimum rise time was less than 150 ns and the pulse width was adjustable from 500 ns to 5 μ s. The repetition rate and the droop were limited by the charging power supply and pulse capacitors and were not reported.

The solid-state Marx modulator, developed for Fermilab's Tevatron electron lens tune compensation system, produced 14 kV pulses into a 800 Ω load at 25 kHz repetition rate [62]. The first prototype was equipped with IGBT switches. The pulse width was 600 ns and the rise time 200 ns. The fall time was in the same range but it has not been specified. Each stage of this Marx modulator could be switched on and off during the pulse. Therefore, the output voltage could be dynamically changed in discrete

steps, providing the possibility to digitally modulate the output waveform. It was mentioned that by using MOSFETs instead of IGBTs, the rise and fall times could be shortened with low output voltages. The ripple and droop of the output pulse were not reported.

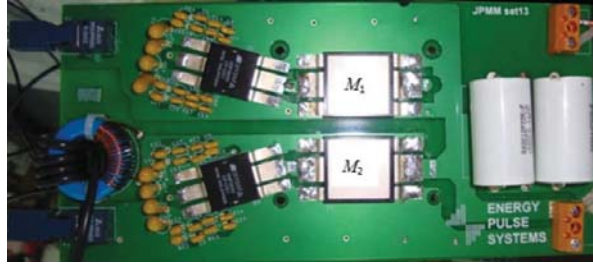


Figure 2.15. A single cell of a solid-state Marx modulator, developed by Energy Pulse Systems [63].

A solid-state Marx modulator developed at Tsinghua University in China generated 10 kV pulses across a 1 k Ω resistive load [64]. The pulse rise time was 30 ns, pulse length 250 ns and repetition rate 400 Hz. The pulse flat-top precision was not reported but according to figures of the output pulse waveforms presented in [64], the flat-top ripple was a few percent of the output pulse amplitude.

The P2 Marx Modulator developed at SLAC for ILC klystrons produces 120 kV output voltage and 140 A output current [58]. The pulse length was 1.6 ms, repetition rate 5 Hz and pulse flatness within $\pm 0.5\%$. This high-voltage modulator included novel approaches regarding the redundancy and output waveform. Each of its 32 cells regulates the output waveform individually and up to two layers can fail and the modulator still gives the rated output voltage.

A bipolar solid-state Marx modulator developed in the Lisbon Technical University in Portugal generates ± 5 kV pulses to a capacitive load of 340 pF with 1 kHz repetition rate [59]. The modulator consists of five stages, each of which can be switched on and off individually to generate 11 different voltage levels (five positive, five negative and zero volts) and to create arbitrary waveforms by using digital modulation. The semiconductor switches of the modulator are MOSFETs. Rectangular, triangular and other type of waveforms have been demonstrated and in the measurements the capacitive load was connected in parallel with a 2 M Ω resistor. The flat-top stability of the output pulse and the maximum pulse duration have not been reported.

Another bipolar solid-state Marx modulator has been developed in Fudan

University in China [65]. The prototype modulator, built using MOSFET switches, generates ± 2 kV pulses with 200 ns pulse duration to a 50Ω load. Rise time of the output pulse is 37 ns and fall time 50 ns. The flat-top stability of the of the output waveform has not been reported.

A new injection kicker system is under development for J-PARC accelerator facility in Japan. In this system, a solid-state Marx modulator will feed a fast kicker magnet [66]. The modulator, based on MOSFET switches and consisting of at least 40 layers, will feed 10 kV pulses to a kicker magnet which has a 10Ω characteristic impedance. The output waveform would be modulated with a predefined function with bandwidth up to 100 MHz to compensate the irregular kicker tail.

Table 2.3. Summary of solid-state Marx modulators.

Ref.	Output voltage (kV)	Flat-top current (A)	Pulse duration (ns)	Load	Reported flat-top stability (%)
[60]	20	0.01-4	n/a	n/a	n/a
[61]	28	28	500-5000	1 k Ω	n/a
[62]	14	17.5	600	800 Ω	n/a
[64]	10	10	250	1 k Ω	n/a
[58]	120	140	1.6×10^6	n/a	± 0.5
[59]	± 5	0	n/a	340 pF	n/a
[65]	± 2	40	200	50 Ω	n/a
[66]	10	500	1000	10 Ω	n/a

Table 2.3 shows a summary of the solid-state Marx modulators presented above. To sum up, the solid-state Marx modulators found in the literature have mainly been designed for higher voltages and the rise and fall time are longer than 100 ns, which is desired for the CLIC DR kicker system. Also, the load impedance has often been much higher than the 50Ω specified for the DR kicker striplines. In general, flat-top stability of the output pulses has not been reported for the Marx modulators in the literature. Modulation methods can be applied for shaping the output pulse of the Marx modulator. To give examples, digital modulation has been used in [62] and a modulated output waveform will be needed in the application described in [66]. Therefore, the solid-state Marx could be a candidate topology for the CLIC DR kicker pulse modulator.

Inductive Adder

The inductive adder, shown in Fig. 2.16, consists of multiple single-turn primary circuits, a single-turn secondary winding, and a fast coaxial pulse transformer with adequate voltage isolation. Each primary circuit has a fast switch or an array of switches and a capacitor bank. The primary circuits are independent and each of them is referenced to ground. The output voltage of the inductive adder is the sum of the voltages, which are induced to the secondary winding by the individual primary circuits.

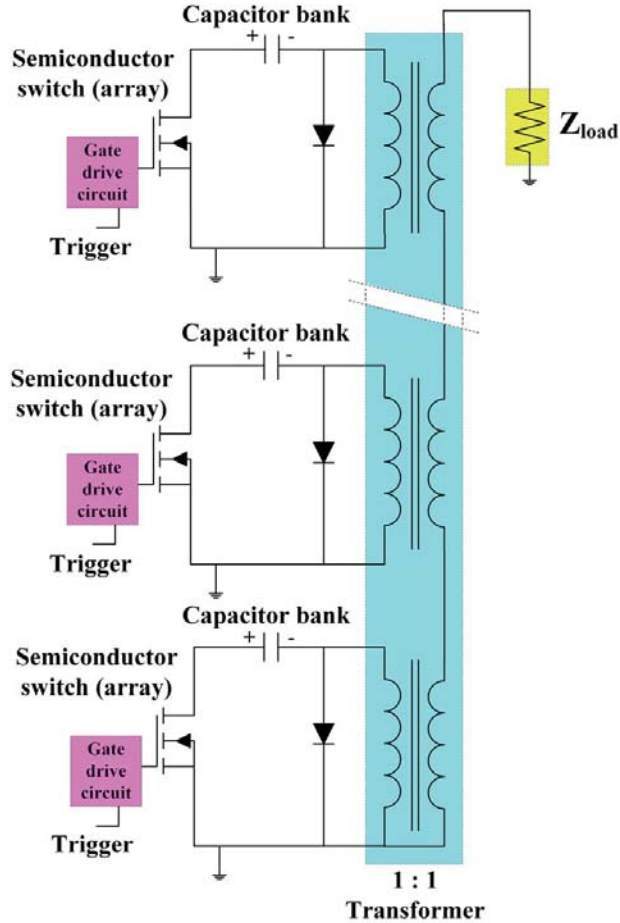


Figure 2.16. Schematic of an inductive adder.

The inductive adder has some benefits in comparison with the series switch topology and the Marx modulator topology. All the control electronics can be referenced to ground and there are no electronics which would be referenced directly to the high-voltage output pulse. It has a good built-in fault-tolerance and redundancy, because if one or more solid-state switches of a layer of the inductive adder stack fails to switch, the pulse magnitude of the adder is reduced only by the voltage of a single layer. For example, in the case of an adder with 10 layers, one of which

fails to switch, the output voltage still reaches approximately 90 % of the maximum output voltage of the adder. Also, the full output voltage could still be reached for subsequent pulses by changing the pre-charge voltage of the capacitor banks in the operating layers, although with the disadvantage of higher voltage stress on the operational layers. However, this can be allowed for by having redundant layers in the stack, in which case the normal operating voltage per layer can be smaller and it can be increased appropriately if a failure occurs in a layer. The inductive adder can be used to generate positive and negative pulses depending on the grounding of the adder secondary winding. Also bipolar output can be achieved, either by having separate negative and positive primary windings in each layer [67] or by using two secondary windings with opposite groundings [68].

A drawback of the inductive adder is that it is a rather complex device requiring many components. Also, each layer must switch full load current and the fault currents may be very large [40]. In general, the pulse width of the inductive adder is limited by the saturation of the magnetic core. The minimum pulse rise time of the inductive adder is limited by the loop inductance of each primary layer and the number of the primaries (layers) in the adder [69].

State-of-Art Inductive Adders

The Advanced Radiograph Machine (ARM) at Lawrence Livermore National Laboratory (LLNL) was one of the first high power pulse modulators built with solid-state switches [70]. ARM was designed to generate 45 kV and 5 kA pulses with voltage rise and fall times of 100 ns. The flat-top pulse width was adjustable from 200 ns to 1.5 μ s and the repetition rate up to 2 MHz. The ripple and droop of the output pulses were not reported.

Another of the earliest inductive adder applications found in the literature was a solid-state kicker modulator for the Dual-Axis Radiographic Hydrodynamic Test Facility (DARHT-2), which was also designed and built at LLNL. The output voltage of the modulator was ± 20 kV across the 50 Ω load and voltage rise and fall times were less than 10 ns from 10 % to 90 % of the pulse. The pulse flat-top duration was continuously adjustable from 16 ns to 200 ns. The maximum repetition rate was 1.67 MHz for a burst of four pulses which have 600 ns between leading edges [71]. The flat-top stability of the modulator was not reported.

A DARHT II fast dipole kicker modulator at LLNL was developed to provide 18-20 kV across a $50\ \Omega$ load with voltage rise and fall times of 10 ns from 10 % to 90 %. The flat-top pulse width was adjustable from 20 to 200 ns [72]. An interesting feature of this device was the possibility to use analogue modulation to modulate the output pulse over 10 % of the output voltage range and with modulating frequencies up to the MHz range. Applying analogue modulation to the output waveform of an inductive adder has been presented in detail in [73]. The flat-top ripple of this modulator was $\pm 1\%$ [72]. A photo of the prototype inductive adder for the DARHT II fast dipole kicker modulator is shown in Fig. 2.17.

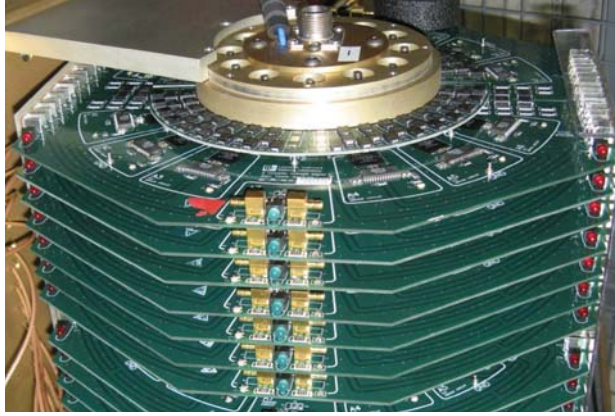


Figure 2.17. Photo of a prototype inductive adder developed at LLNL. Courtesy of M. Barnes, 2010.

Another pulse modulator was developed at LLNL for the DARHT II Fast extraction kicker. It was designed for 50 kV output voltage [72]. The flat-top pulse width was 73 ns and pulse flatness specification is better than one percent. The rise and fall times were 64 ns from 0 to 100 %. The intra-pulse voltage ripple was required to be less than 300 V, which is 0.6 % of the maximum output voltage. To achieve this, digital amplitude modulation was used to cancel the droop of the capacitor voltages: some layers of the adder stack were charged to a fraction of the maximum voltage of other layers and switched on later than most of the layers to compensate droop.

Another example of applying digital modulation to manipulate the output of the inductive adder pulser is the conceptual design of a ± 4 kV, 40 A adder for the Muon Electron Conversion Experiment at Brookhaven National Laboratory [67]. The pulse rise and fall times are 20 ns, pulse flat-top 100 ns, pulse repetition rate 300 kHz and the output is a sinusoidal wave, modulated at 60 kHz. Therefore, the pulse modulator gives

five pulses per modulation frequency period. By charging each layer of the adder stack to different fractional voltages of the full voltage, as a maximum to a half, a quarter or an eighth of the full voltage etc., it is possible to achieve the desired output resolution, which is defined by the lowest charging voltage of a layer. In the proposed design, the total number of layers is twelve, seven of which are charged to the nominal maximum voltage, 500 V, and five of which are charged to fractional voltages, the lowest of which is 15.6 V. The polarity of each layer can be changed. With this design, the output voltage can be theoretically adjusted with the resolution of better than 0.5 % of the maximum output voltage of ± 4 kV [67]. The achieved precision was not reported.

The power modulator for LINAC klystrons at Fermi National Laboratory is based on the inductive adder but it has an auxiliary pulse transformer in the output. The output voltage is 320 kV and peak current 350 A. The output pulse width of the modulator is $4.5 \mu\text{s}$ and voltage rise and fall times less than 500 ns. The pulse to pulse repeatability is better than 0.2 % of the peak voltage and the flat-top ripple is specified to be less than 1 % of the peak voltage. In order to achieve this, droop of the output pulse caused by a finite value of primary storage capacitance is compensated by a separate passive resistor-inductor (RL) circuit [74].

One of the more recently published papers concerning applications of the inductive adder is for the solid-state driver for the National Ignition Facility at LLNL to feed plasma electrode Pockels cells [75]. This modulator consists of 27 layers, designed to operate at 750 V per layer, maximum, and the output voltage is 17 kV. The rise time is 20 ns and the fall time is in the same range but purposely held longer to avoid voltage transients in the overall system. The modulator provides the ability to generate flat-top pulses, burst mode capability, continuously variable pulse spacing and pulse burst frequency agility. A flat-top precision of ± 2 % is given for the overall system including the pulse modulator, transmission lines and a Pockels cell but the flat-top precision for the inductive adder itself has not been specified.

A prototype solid-state modulator was developed at National Synchrotron Radiation Laboratory for a fast kicker in Hefei Light Source, in China [76]. The modulator consisted of four stages and generated 2.4 kV pulses across a 20Ω load. The rise time was 30 ns and pulse flat-top width 40 ns. The repetition rate was adjustable up to 500 kHz. The droop or ripple has not been specified.

Tsinghua University in China and Nagaoka University in Japan have developed a very compact inductive adder type modulator for industrial applications. Instead of an inductive adder, the first prototype was named a linear transformer driver (LTD) and it was presented in 2010 [77]. The first prototype was a single layer device and it generated 700 V pulses across a 3.2Ω resistive load. The repetition frequency was up to 500 Hz, and the rise and fall times of the voltage pulses were 20 and 40 ns, respectively.

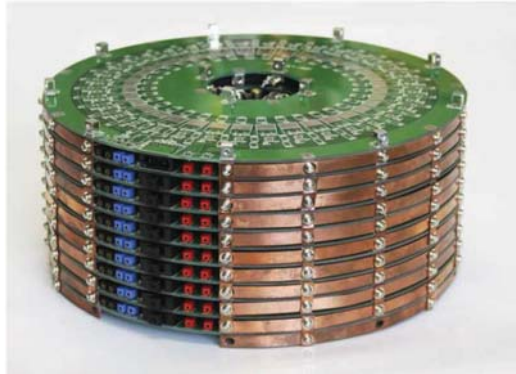


Figure 2.18. Photo of a compact LTD with 10 layers [78] .

An updated design of the LTD (Fig. 2.18), developed at Tsingua and Nagaoka Universities, was presented in 2012. This modulator generated up to 9 kV pulses with 175 A of peak current [78]. The prototype modulator is very compact: the height of the stack is 12 cm and the outside diameter 28 cm. In the latest version, digital modulation has been applied to shape the output pulse. Each layer of the adder can be switched on and off individually and thus different patterns of pulses can be generated, with variable durations and flat-top voltages (maximum is limited by the magnetic cores), or digitally modulated arbitrary waveforms [79]. This approach has been named "smart pulsed power". The flat-top precision of the output waveform has not been reported.

Department of Electronic and Electrical Engineering of the University of Strathclyde and Pulsed Power group of Atomic Weapons Establishment, both located in the United Kingdom, have developed a 600 V, 1 kA pulse power modulator module [80]. The initial specifications for the modulator, which they call an LTD, are 20 kV, 1 kA output pulses. The specifications for the LTD module are up to 1 kV, 1 kA pulses with 60-100 ns total duration, with repetition rate up to 1 MHz and with rise and fall times less than 10 ns. The ripple and droop have not been reported. A single module has been tested without a magnetic core to feed 100 ns,

600 V pulses to a resistive load of 0.9Ω at up to 400 kHz. The measured rise time was 4.8 ns and fall time 9.6 ns.

Recently, a pulse power modulator has been developed at Energetic Laser Laboratory at Rochester University for driving Pockels cells and a detailed design report is presented in [81]. The design of the modulator is based on the inductive adders developed at LLNL. The requirements for the modulator are the following: up to 10 kV of peak voltage with a 50Ω output impedance and with better than $\pm 3 \%$ of peak voltage stability and less than $\pm 4 \%$ of flat-top variation. Pulse rise and fall times are required to be less than 10 ns from 10 % to 90 % of pulse voltage and pulse length adjustable from 9 to 100 ns. The repetition rate is 10 Hz. The developed pulse modulator has met the specifications.

In 2013, Siemens AG presented a prototype of an industrial pulse modulator which is based on inductive adder topology and equipped with IGBT switches. The prototype modulator consists of three layers and generates a peak voltage of 12 kV and a peak current of 6 kA [82]. Only initial results have been published so far without details on pulse rise and fall times or flat-top stability.

Table 2.4. Summary of state-of-art inductive adders.

Ref.	Output voltage (kV)	Flat-top current (A)	Pulse duration (ns)	Load	Reported flat-top stability (%)
[70]	45	5000	200-1500	n/a	n/a
[71]	± 20	n/a	16-200	50Ω	n/a
[72]	18-20	400	20-200	50Ω	± 1
[72]	50	1000	73	50Ω	1
[67]	± 4	40	100	100Ω	n/a
[74]	320	350 (peak)	4500	n/a	1
[75]	17	n/a	n/a	n/a	$< \pm 2$
[76]	2.4	120	40	20Ω	n/a
[77]	0.7	219	n/a	3.2Ω	n/a
[78]	9	175	n/a	n/a	n/a
[80]	0.5-1	500-1000	60-100	0.9Ω	n/a
[81]	10	175	9-100	50Ω	± 4
[82]	12	6000	n/a	n/a	n/a

Table 2.4 shows a summary of the inductive adders presented above. To conclude, the inductive adder type solid-state modulator has been used in various pulse power applications and also in many kicker systems. The required voltage ranges, pulse lengths and rise and fall times of the CLIC DR kicker systems are moderate in comparison with existing applications. The ripple and droop requirements for CLIC are much tighter than for any of the existing applications, however an analogue modulation technique presented in [73], is a promising solution to keep ripple and droop within the demanding specifications for the CLIC DR kickers.

Other Solid-State Modulator Topologies

A transmission line adder is similar to an inductive adder except that the pulse transformer units are replaced with transmission lines. There are quite a few examples of the transmission line adders in the literature. The existing applications have been designed for short pulse lengths, up to 10 ns, and with very fast rise times, up to five nanoseconds [83], [84]. According to [83], the advantage of transmission line adder topology over a inductive adder topology is the suitability to generate high-voltage pulses with extremely fast rise times, down to a nanosecond. For an inductive adder, the minimum achievable rise time may be limited by the geometry of the adder stack and, consequently, its electrical length [83]. Also, if the pulse flat-top duration is very short, e.g. 10 ns, the transmission line adder may be technically simpler and cheaper than an inductive adder [84]. Based on these references, the transmission line adder is more suitable for shorter pulses and faster rise times than what are required for the CLIC DR kicker system. Therefore, the transmission line adder topology has not been studied further in this dissertation.

A solid-state modulator topology with a matrix transformer, which is also called a split core transformer, is presented, for example, in [85]. Scandinova AS in Sweden has built a modulator based on the split core transformer topology, the measured flat-top stability of which is $\pm 0.05\%$ [86]. This was measured for 3 μs duration of the 4.5 μs long flat-top of a 200 kV pulse, the total pulse duration of which was approximately 10 μs , and the load was a TH2100C klystron [89]. The flat-top stability is one of the best numbers reported in the literature for high-voltage pulse modulators. However, the klystron is a non-linear load and therefore, for example, the overshoot of the pulse fed by the modulator can be significantly smaller than for a resistive load the impedance of which is the same as

the impedance of the klystron at the full flat-top voltage [87]. Both active and passive compensation methods have been applied to improve the pulse flat-top stability of the matrix transformers. In [89] an RL filter was used to reduce the droop of the output waveform. In [88], an active bouncer circuit was applied to decrease the amount of capacitance which was needed to keep the droop within allowed limits. However, the modulators based on matrix transformer topology have usually been designed to drive klystrons and, therefore, they have much higher voltage, longer pulse duration and longer rise and fall times than specified for the CLIC DR kicker modulator. Also, according to [85], the inductive adder topology could be considered as a special case of the matrix transformer topology. Therefore, the matrix transformer topology has not been discussed separately in detail in this dissertation.

2.3.3 Reasoning for Selecting the Inductive Adder Topology

Based on the literature survey of pulse power modulator topologies presented above, the inductive adder topology has been chosen as the most promising means to achieve the specifications for the pulse power modulator of the CLIC DR kicker system. The detailed reasoning for this choice is given below.

Considering only the output voltage range, the pulse duration and rise and fall times of the CLIC DR kicker modulator, each of the solid-state topologies presented above could be a suitable candidate. Each of the designs is also scalable and could be re-used for designing a modulator with higher current or voltage ranges. However, the inductive adder topology has two obvious advantages in comparison with the solid-state Marx topology and the series switch topology. All control electronics of the inductive adder can be referenced to ground and there is no active component referenced directly to the high-voltage output. In Marx modulators and in the series switch topologies, there are stages which are referenced to high-voltage and to these the control signals need to be fed by fibre optics or by galvanically isolated transformers. Also, the current for gate driver of the semiconductor switches needs to be supplied by high-voltage capacitors of each stage or by galvanically isolated transformers. This increases the number of components which are required for the modulator and adds to the complexity of the system. Use of fibre optics may also require testing and matching of the transmitters and receivers in order to have low time jitter between trigger lines, as was reported in [54].

Another benefit of the inductive adder topology is that the polarity of the output pulse can be changed very easily, simply by changing the grounded end of the secondary winding. This is a major advantage because in the CLIC DR kicker system one of the stripline electrodes must be driven with a positive pulse and the other with a negative pulse. By using inductive adder topology, two identical modulators can generate pulses with both polarities.

The third aspect which supports choosing the inductive adder topology is the built-in fault tolerance. Considering machine safety with the high energy beam, a topology which is intrinsically fault-tolerant is highly desirable for the CLIC DR kickers. Typically, each layer of the inductive adder has several identical current branches in parallel, which consists of a pulse capacitor and a switch. If one switch fails, it does not necessarily affect the operation of the other current paths in the layer. If a single switch fails to switch on, then the other switches need to carry higher current but the layer in which the failure occurs still continues operation. If a single switch fails to short-circuit, the complete layer may be shorted, but the other layers continue operation. If a complete layer of the inductive adder fails either to short-circuit or fails to switch on, the modulator still gives a significant proportion of the full output voltage for the kicker magnet, because the output voltage of the adder is reduced by the voltage of a single layer. Therefore, the inductive adder topology resists both open circuit or short-circuit fault of a single switch, without requiring any modification to the basic circuit topology. The only design constraint, considering the fault-tolerance described above, is that the charging current to the capacitors of each primary layer need to be limited, for example by charging each capacitor through a resistor, in order to limit the current flow to a capacitor in the case when a capacitor is in short-circuit through a switch. Also, redundant layers can be added in the adder stack, to compensate the loss of one or several layers. The design of the inductive adder stack can also be such that changing a single layer is relatively simple work which can be carried out quickly [45].

In a series switch topology, a failure in a single switch increases the voltage stress on the other switches connected in series and failures in several switches may destroy the modulator [40]. However, redundancy can be applied also in the case of series switch topology in a similar manner to the inductive adder. For Marx modulators, designs have been proposed which tolerate a fault of a single stage and have spare stages which can

be powered to replace another stage in the case of fault, as reported for example in [58].

The required flat-top stability for the CLIC DR extraction kicker modulator is an order of magnitude more demanding than for any similar resistively terminated pulse modulator reported in the literature. Therefore it was expected that the output waveform needs to be modulated in order to meet the specifications. Examples of applying modulation techniques to shape the output waveform were found in the literature for the inductive adder and for the solid-state Marx topology. Both digital modulation, with discrete steps, and analogue modulation, controlled by a continuous predefined waveform have been reported. The best measured flat-top stability was reached with the series switch topology with a capacitive load [55], but the techniques utilised are not applicable for a resistive load. The best reported flat-top stability for a Marx modulator was $\pm 0.05\%$ [58], however this was specified for a klystron load the impedance of which was approximately $860\ \Omega$. For Marx modulators, the active compensation of the droop and ripple were applied either by regulating the output of each cell individually or by using a separate bouncer circuit. However, in most cases the flat-top stability of the output pulses has not been reported for the Marx modulators in the literature and the load impedance has been much higher than the $50\ \Omega$, specified for the CLIC DR extraction kicker striplines. The reported precision for the flat-top stability for short pulses from a few hundred nanoseconds to one microsecond were in general more accurate for the inductive adders than for other presented topologies, as can be seen in Tables 2.2, 2.3 and 2.4. For the inductive adders, the compensating circuits were implemented using a single layer in the stack, which is dedicated for the pulse shaping, as presented in [73]. In this approach, the compensation circuit is as robust, i.e. fault-tolerant, as the modulator itself. The expected necessity of applying analogue modulation techniques in order to meet the specification also validates the inductive adder to be the most suitable candidate topology for the CLIC DR kicker system.

Regarding the requirements of the CLIC DR kicker modulator, the inductive adder topology has been found to be the most promising candidate for meeting the given specifications. The inductive adder is a solid-state modulator capable of providing relatively short and precise pulses and with a proper design of the modulator it may be possible to meet the ripple and droop requirements of the CLIC DR kicker system. In the

measurements presented in Chapter 5, both passive and active analogue modulation methods have been applied to compensate droop and ripple of the output waveform of the pulse modulator.

2.4 Methods for Measurement of the Output Waveform

It is not obvious that the flat-top of the output pulse of the pulse power modulator could be measured with $\pm 0.02\%$ of relative accuracy using a direct electrical method. The required relative accuracy of the measurement is far greater than the gain accuracy of high-end oscilloscopes, which is typically $\pm 1\%$. To give an example, for Tektronix DPO 5034 oscilloscope the gain accuracy is $\pm 1.5\%$ [90]. Another problem arises from the short flat-top duration of the pulse, 160 ns, because this is in the same order as the settling time of the measuring preamplifiers of the oscilloscopes [91]. Current transformers are commercially available with droop and rise time specifications, which are good enough for measuring the output pulse of the CLIC DR kicker modulator. For example, the manufacturer Bergoz gave the following specifications for a CT-E0.1 current transformer [92]: maximum peak current 10 kA, droop $0.002\%/ \mu\text{s}$, rise time 7 ns and 3 dB cut-off frequency at 50 MHz.

In order to avoid the preamplifier of the oscilloscope being driven into saturation, the dynamic range of the measured output waveform can be appropriately chosen. Theoretically the droop and ripple of the output pulse of the power modulator can be measured by summing the output pulse with an ideal flat-top pulse, of the same magnitude, which is the output of a high-precision source but with an opposite polarity. The pulses could be summed in a high-precision current transformer and ideally they cancel. Any difference of the zero net field is caused by the ripple and droop of the pulse modulator. A difficulty in applying this method is that an ideal pulse does not exist in reality. However, the relative stability and repeatability of two pulse power modulators can be measured by comparing the output waveforms of two nominally identical devices by feeding their output pulses through a single current transformer with opposite senses. Ideally, the measured currents cancel each other if the pulses are identical. This approach could also be used to measure the precision of the modulation methods, for example by modulating the output of only one of the two inductive adders. This measurement method is demonstrated in Chapter 5.

Another factor which may limit the accuracy of the measurements is the bit length of the analogue to digital converters (ADC) of the oscilloscope. The resolution of the ADC, Res_{ADC} , is calculated with the following equation:

$$Res_{ADC} = \frac{V_{r,ADC}}{2^{N_{ADC}} - 1} \quad (2.4)$$

In this equation, $V_{r,ADC}$ is the maximum absolute voltage range of the single channel of an oscilloscope and N_{ADC} is the bit length of the ADC. Eq. (2.4) gives the absolute resolution and the relative resolution is computed by replacing $V_{r,ADC}$ by 1. In this dissertation, all the measurements were done using a Tektronix DPO 5034 oscilloscope [90], the length of the ADC is 8 bits. For an 8-bit ADC, the basic relative resolution is 0.39 % of the maximum absolute voltage range of the input channel. However, the effective number of bits (ENOB) of the ADC is less, because the resolution is degraded due to quantization noise, non-linearity of preamplifiers, missed digitising levels and a change of a signal during the sampling process [93]. The ENOB of an 8-bit ADC with high dynamic range is typically between 6 and 7 bits [93], [94]. The effective bit length of the ADC can be increased by applying oversampling [95]. In this method, the input signal is oversampled at a frequency above the Nyquist criteria and the samples are averaged to create a single data point of several samples. One criterion for oversampling to be effective is that the signal component of interest does not vary significantly during the processing time of the ADC. This should be true for the flat-top of the pulse from an inductive adder. Assuming that the signal contains some noise whose amplitude is at least one least significant bit of the ADC, then for each additional bit, the input signal must be oversampled four times [95]. For Tektronix oscilloscopes this is known as "high resolution mode" and it may increase the effective bit length of the 8-bit ADC of a DPO 5034 oscilloscope up to 11 bits [96]. The resolution enhancement of the ADC is given by the following equation [96]:

$$Res_{Enh,os} = 0.5 \times \log_2 D \quad (2.5)$$

In this equation, $Res_{Enh,os}$ is the number of bits by which the resolution of the ADC is improved by applying oversampling. D is the oversampling factor. This technique is also called boxcar-averaging and D corresponds

to the number of taps of the averaging filter, N_{boxcar} . The effective sampling rate $F_{s,\text{Eff}}$ is given by the following equation:

$$F_{s,\text{Eff}} = \frac{F_s}{N_{\text{boxcar}}} \quad (2.6)$$

in which F_s is the sampling rate of the signal.

One drawback of applying this technique is that the -3 dB bandwidth of the measurement system, $BW_{-3\text{dB}}$, is reduced according to the following equation [97]:

$$BW_{-3\text{dB}} = 0.44 \times F_{s,\text{Eff}} \quad (2.7)$$

In most of the measurements presented in this dissertation, oversampling by a factor of four was applied, which is expected to give one additional bit for the ADC of the oscilloscope. Therefore, the effective bit length of the ADC was the ENOB summed with one bit, which gives 7-8 bits.

Arbitrary, asynchronous ripple and noise can be reduced in magnitude in the output waveform by taking the average of otherwise identical consecutive pulses. The method of averaging the corresponding samples of different pulse recordings is called ensemble averaging or normal averaging. According to theory, the signal-to-noise ratio, S/N_{ri} , increases with the square root of the number of averaged measurements, as follows [98]:

$$\frac{S}{N_{\text{ri}}} = \sqrt{n} \frac{S}{\sigma} \quad (2.8)$$

In this equation, S is signal amplitude, N_{ri} is noise amplitude, n is the number of measurements and σ is the standard deviation of the noise. It is assumed that the signal and noise are not correlated, signal amplitude remains constant in the measurements, the noise is random with a mean value of zero and the noise has constant variance. In reality, these assumptions are not completely true and this leads to a lower signal-to-noise ratio improvement. Eq. (2.8) can be rewritten as follows:

$$N_{\text{ri}} = \frac{\sigma}{\sqrt{n}} \quad (2.9)$$

If the standard deviation σ presents the noise in a single measurement,

the total noise N_{ri} is reduced by the square root of the number of the measurements which are averaged.

In all measurements shown in this dissertation, the ensemble averaging method has been applied in order to filter the asynchronous ripple of the output voltage and hence to improve the relative accuracy of the measurement of the output waveform. Applying the ensemble averaging method also improves the vertical resolution of the ADC according to the following equation [96]:

$$Res_{Enh,ea} = 0.5 \times \log_2 n \quad (2.10)$$

In this equation, n is the number of averaged measurements and $Res_{Enh,ea}$ is the resolution enhancement of the ADC. To give an example of Eq. (2.10), an average of 8 samples would give 1.5 bits enhancement and average of 1024 samples gives 5 bits enhancement for the resolution of the ADC. By taking into account the worst case estimate of the ENOB of an 8-bit ADC, 6 bits [93], the resolution of the ADC would be effectively 7.5 and 11 bits, for an average of 8 and 1024 samples, respectively. According to Eq. (2.4), this would give the relative resolution of 0.56 % and 0.05 %, respectively. If oversampling by a factor of four is applied, this would give one additional bit according to Eq. (2.5) and improve the relative resolution to 0.28 % and 0.025 %, respectively. The effective resolution of the measurements shown in Chapter 5 and the effectiveness of ensemble averaging method to suppress noise is discussed in Section 5.6.

Finally, if the direct electrical measurement of the ripple of the pulse modulator is not possible, to the required accuracy, another method could be to measure the pulse flat-top stability with a stripline kicker. The kicker would be installed in a beam line and it could be followed by a static dipole magnet, which could be fed with a high stability DC power supply [38]. The dipole magnet would deflect the beam equally but in the opposite direction to the kicker. The fluctuations seen in the beam after the second kick, from the dipole magnet, are caused by ripple of the pulse modulator which feeds the kicker magnet. However, applying this method requires machine time in an accelerator facility and a specific set-up for the beam line.

3. Design of the Inductive Adder

This chapter presents the general design of the inductive adder type pulse modulator. Most of the content is based on the previously published literature about the design of inductive adders which gives good preliminary design parameters for an inductive adder with a typical required flat-top stability of $\pm 1\%$. The main purpose of this chapter is to provide reasoning for selection of the parameters for the simulation and modelling studies, which are presented in Chapter 4. This chapter also explains the main design procedures which have been applied in designing the prototype adders presented in Chapter 5.

Initially, the design parameters for the CLIC DR kicker inductive adder and for the two built prototype inductive adders are discussed. Then, the main components of the inductive adder and the requirements for them are presented, covering semiconductor switches, pulse capacitors and magnetic cores. This chapter also covers dimensioning of the inductive adder cells and a stack. The mechanical design of the adder structure is discussed and a step-by-step design guide is given for defining the dimensions of the adder stack, in order to reach the desired output impedance for the pulse modulator.

3.1 Design Parameters for the CLIC DR Extraction Kicker Inductive Adder and for the Two Experimental Prototypes

In order to verify the design and modelling studies presented in this dissertation, two small-scale prototype inductive adders were built. The design parameters for the CLIC DR extraction kicker inductive adder and for the prototypes are shown in Table 3.1. The main reason to build two prototypes, instead of one, was that with two prototypes it was possible to demonstrate a measurement method in which a net current of two pulses

with opposite polarities is measured, in order to decrease the dynamic range of the measured signal, as discussed in Section 2.4.

The maximum output voltage of the prototype modulators was defined to be 3.5 kV in order to demonstrate the high-voltage operation of the inductive adder with extremely flat-top pulses. The prototype inductive adders have $50\ \Omega$ nominal output impedance, which gives 70 A for the maximum current at 3.5 kV to a $50\ \Omega$ load. However, the goal was to design the primary circuits of the prototype adders to feed the full load current needed for the CLIC DR extraction kicker system, which is 250 A, as shown in Table 2.1. The maximum pulse length of the CLIC DR extraction kicker system is 160 ns for the 2 GHz baseline and 900 ns for the 1 GHz baseline [7]. The maximum pulse length of the prototype inductive adder was defined to be the largest of these, 900 ns. The pulse rise and fall times were defined to be 100 ns as maximum, from 0.1 % to 99.9 % of the pulse voltage, because these are desired parameters for the CLIC DR kicker pulse modulator.

Regarding the flat-top stability, the final specification for the CLIC DR extraction kicker system is $\pm 0.02\%$. However, it was found in the literature review, presented in Chapter 2, that this requirement is very tight and novel methods are needed in order to meet this specification. Therefore, the first goal for the prototype modulator was to reach the flat-top stability for the CLIC PDR extraction kicker system, $\pm 0.2\%$ [7], and then improve it towards the final goal, $\pm 0.02\%$. This was seen as a proper approach for the feasibility study, because achieving the final precision may require several time-consuming and costly prototypes. Also, the direct electrical measurement of the output pulse with better than $\pm 0.02\%$ precision may not be possible, as discussed in Section 2.4.

3.2 Operation Principle of the Inductive Adder

Figure 3.1 shows a schematic of an inductive adder. The inductive adder consists of coaxial pulse transformers, the secondary windings of which are connected in series. Both the primary and secondary windings will have a single turn for the CLIC design to minimise parasitic inductances [72] and, therefore, to allow fast rise and fall times for the output pulse. The inductive adder primary consists of stacked layers of printed circuit boards (PCB). The primary circuits are independent and each of them is referenced to ground. The inductive adder shown in Fig. 3.1 consists

Table 3.1. Design parameters for the CLIC DR extraction kicker inductive adder and for two prototype inductive adders.

	CLIC DR extraction kicker inductive adder	Two prototype inductive adders
Output voltage (kV)	12.5	3.5
Output current [50 Ω load] (A)	250	70
Pulse flat-top duration (ns)	160 900	≤ 900
Pulse rise time [0.1-99.9 %] (ns)	100	100
Pulse fall time [0.1-99.9 %] (ns)	100	100
Flat-top stability [for 160 ns] (%)	$\leq \pm 0.02$	$< \pm 0.2$

of three different types of layers, namely constant voltage layers, digital modulation layers and an analogue modulation layer. Ideally, all constant voltage layers of the adder generate identical voltage pulses and digital and analogue modulation layers may be used to shape the output waveform. The main differences of the designs of these layers are explained in the next paragraphs.

3.2.1 Constant Voltage Layers

The primary circuits of the constant voltage layers are constructed of PCBs, each of which includes capacitors, fast solid-state switches with their driver circuits and transient protection components. Constant voltage layers are switched on to generate the load pulse and every layer nominally generates the same output voltage. The pulse capacitors of each constant voltage layer are charged to the same voltage using a single power supply and the trigger signals may be fed from the same trigger source. Examples of an inductive adder stack and a primary circuit are shown in Fig. 3.2.

If an inductive adder only consists of constant voltage layers, which are identical and the storage capacitors of which are initially charged to the same voltage before switching on, the output voltage of the adder, V_{load} , is approximately given by the following equation:

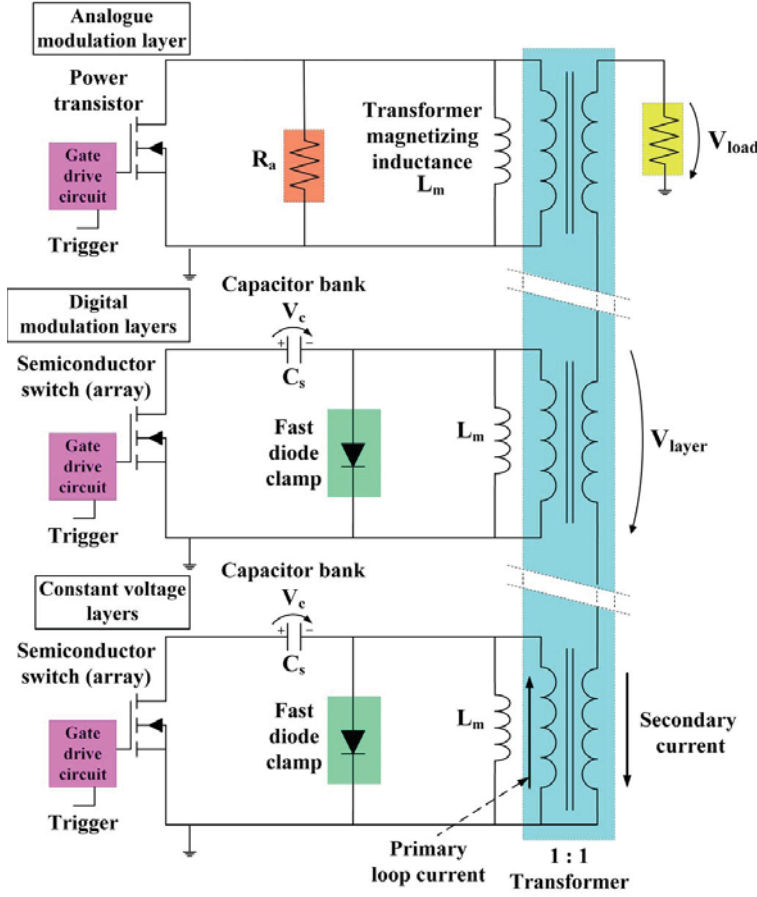


Figure 3.1. Schematic of an inductive adder with constant voltage layers, digital modulation layers and an analogue modulation layer.

$$V_{load} \approx NV_{layer} \quad (3.1)$$

In this equation, N is the number of primary constant voltage layers and V_{layer} is the voltage which is induced on the secondary of each constant voltage layer. In Eq. (3.1) it is assumed that the semiconductor switches of each constant voltage layers are switched on. In Fig. 3.1, the voltage arrow for capacitor voltage V_c points from the positive voltage to the negative voltage and it has positive polarity. In this case, load voltage V_{load} and the secondary voltage of a single layer V_{layer} have negative polarity. The output current of the inductive adder is assumed to be defined by the load impedance and the load current flows through each layer of the inductive adder stack.

In the schematic shown in Fig. 3.1, each layer includes an inductance L_m . This parasitic circuit element describes a finite magnetising inductance of each layer. During the pulse, the capacitor bank of each constant

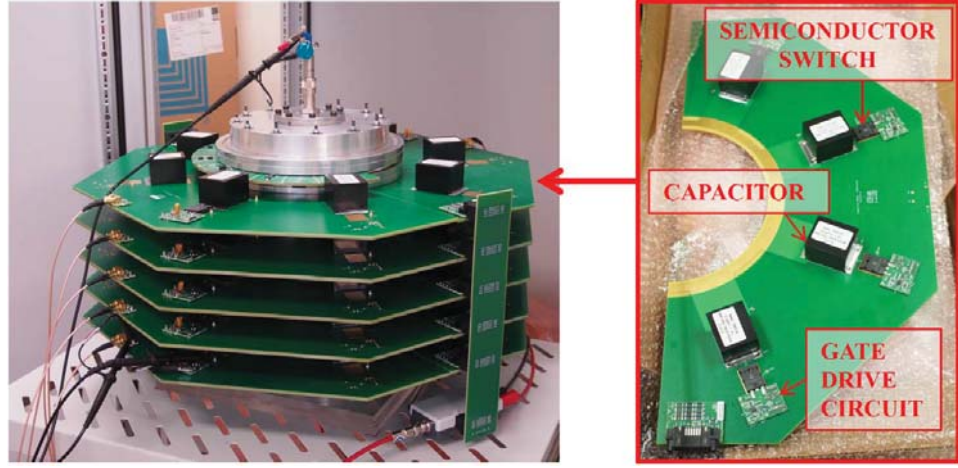


Figure 3.2. Photographs of a 5-layer prototype inductive adder (left) and a half-layer PCB of the primary circuit (right) at CERN.

voltage layer needs to supply the load current, the magnetising current and the core loss current. The magnetising current depends on the pulse duration and its maximum value during the pulse, I_{Lm} , is given approximately by the following equation:

$$I_{Lm} \approx \frac{V_{layer} \times t_{p,50}}{L_m} \quad (3.2)$$

In Eq. (3.2), L_m is the magnetising inductance and $t_{p,50}$ is the pulse duration at half maximum. By using the pulse duration at half maximum instead of pulse flat-top duration, the rise and fall times are taken into account. In Eq. (3.2), it is assumed that the magnetising inductance remains constant during the pulse and it does not depend on the bandwidth of the pulse nor the magnetising current. If the core starts to saturate, this assumption is not true.

In the schematic shown in Fig. 3.1, there is also a fast diode clamp in each constant voltage layer. This clamp, which consists usually of an array of parallel diodes, has two purposes. At first, the diode is needed to provide a free-wheeling path for the transformer magnetisation current, following turn-off of the switches. In some references, for example [40] and [99], the diode clamp circuit comprises a Zener diode in series with the rectifying diode. The threshold voltage of the diode clamping circuit defines the maximum resetting voltage across the magnetic cores, and therefore the resetting time during normal operation [68]. Hence, the Zener diodes may be needed to increase the minimum threshold voltage across the clamping circuit, in order to reset the magnetic core in a short

time after the pulse. Secondly, the fast diode clamp is also needed for the case when a layer does not switch on in the adder stack, either as a result of a switching failure, or on purpose, e.g. if digital modulation is applied. In this case, the secondary current induces current in the primary winding of the layer which is not switched on and a low impedance current path is provided by the diodes to avoid failures of components in this layer. The forward voltage of the fast diode clamp determines the voltage over the layer in which the switching has not occurred.

In addition to a fast diode clamp, in some references a snubber circuit is drawn in the schematic of the inductive adder to protect the semiconductor switches against voltage transients. This is shown, for example, in [40] and [99]. However, it has not been included in Fig. 3.1, because according to [100], the fast diode clamping circuit is often adequate to protect the switches and the separate snubber circuit is not needed. However, this depends on the circuit design and the need of snubber circuits for the CLIC DR kicker inductive adder, especially in the case of a fault, will be reviewed when more experience is gained. The two built prototype inductive adders presented in Chapter 5 were not equipped with snubber circuits. No damage was detected in the semiconductor switches during the measurements which were done for this dissertation.

3.2.2 Modulation Layers

Digital Modulation Layers

The digital modulation layers are similar to constant voltage layers except that the charging voltage of the pulse capacitors may be different for each digital modulation layer and the layers are not necessarily switched on during each pulse. Each digital modulation layer can be switched on and off during the pulse to provide pulse shaping, or it can be used to compensate the voltage droop of the capacitors of the constant voltage layers during a burst of pulses [72]. The charge voltages of the pulse capacitors in the digital modulation layers can be controlled independently and the layers also have independent trigger signals. Otherwise the electrical design of the digital modulation layer is identical to the constant voltage layers, as can be seen in Fig. 3.1. In the case in which the inductive adder consists of constant voltage layers and digital modulation layers, the output voltage of the adder is the sum of the induced voltages of the individual layers which are switched on. A digital modulation scheme is

not applicable to reduce the ripple and droop of the CLIC DR extraction kicker modulator, because the specified voltage range of the amplitude variations is only a few volts in total (± 2.5 V).

Analogue Modulation Layers

The output pulse of an inductive adder can be modulated using analogue modulation techniques, which are applied using an analogue modulation layer. The analogue modulation layer, shown in Fig. 3.1, differs in a number of ways from the constant voltage layers. In the analogue modulation layer, there is not a semiconductor switch, a capacitor bank neither a diode clamp, but instead there is a low valued resistance R_a connected in parallel with the transformer primary. In an active analogue modulation layer, there is also a power transistor in parallel with resistor R_a . This transistor is operated in the linear operation mode, in which a small change in the gate-source voltage causes a linear change in the drain current. In Fig. 3.1, there is only a single analogue modulation layer shown, however, there could be more than one analogue modulation layer in the adder stack.

The operation principle of the analogue modulation layer is the following: during the output pulse, resistor R_a is effectively in series with the load resistor and the secondary winding of the adder [73]. If only the resistor R_a is conducting in the analogue modulation layer, i.e. the power transistor is not conducting, the load voltage, V_{load} , is approximately given by the following equation:

$$V_{\text{load}} = \frac{R_{\text{load}}}{R_a + R_{\text{load}}} \times V_{\text{sum}} \quad (3.3)$$

where V_{sum} is the sum of the output voltages of the constant voltage layers and R_{load} is the resistance of the load resistor. V_{sum} can be computed with Eq. (3.1), by substituting the number of operating constant voltage layers and the voltage which is induced on the secondary winding of a single layer, V_{layer} . It can be seen in Eq. (3.3) that the load voltage V_{load} is smaller with the analogue modulation layer than without it.

As the author has demonstrated with simulation results in [9] and [10], the analogue modulation layer can work either passively or actively. For passive analogue modulation, the power transistor, which is typically an RF power MOSFET, is not conducting and at the beginning of the pulse the full load current flows through resistor R_a and the voltage drop across

resistor R_a reaches its maximum. However, during the pulse a proportion of the load current of the analogue modulation layer transfers to the magnetising inductance L_m thus reducing the voltage drop across R_a . This change in the voltage drop across R_a is opposite to the voltage droop of the capacitors of the constant voltage layers. Therefore, the analogue modulation layer can be used to compensate for the droop of the output pulse. This has been verified in this dissertation with both simulations and measurements.

For active analogue modulation, the power transistor in the analogue modulation layer is used in its linear operation mode. The transistor provides a shunt path for the current which flows through resistor R_a . By controlling the current sharing between the resistor and the power transistor, it is possible to modulate the voltage over resistor R_a and hence the load voltage. If the power transistor is operating at its minimum on-state resistance, a significant portion of the current flows through the transistor and hence the voltage drop across R_a is minimised. The power transistor needs a linear gate drive circuit and the control signal for this could be generated using a function generator. An example of such a gate drive circuit is shown in [73]. The author reported in [9] and [10] that the active analogue modulation could potentially be used to cancel, for example, the voltage droop and ripple components of the output pulse. This is discussed in Chapter 4 and experimentally verified in Chapter 5.

3.3 Design Steps of the Inductive Adder Stack

The mechanical structure of the core housing of a single layer of the inductive adder stack is similar to that of an induction accelerator cell [40]. The coaxial transformer structure of a single layer is called an inductive adder cell in this dissertation. The dimensions of these coaxial transformer units and the PCB design are critical to achieve the desired low ripple and relatively short rise and fall times for the output pulse. Matching of the output impedance of the adder to the load needs to be very good in order to minimise reflections.

The design of the dimensions of the inductive adder is an iterative process. The process can be carried out as follows:

1. Choose the type of semiconductor switches, their voltage rating and operation voltage.

2. Calculate the number of primary layers, including redundancy, taking into consideration a suitable derating for the semiconductors.
3. Estimate the need of capacitance per layer.
4. Determine the minimum effective cross-sectional area (ECSA) of the magnetic core and define the minimum cross-sectional area of the core taking into consideration a suitable safety margin and a packaging factor. In addition define the minimum inside diameter of the core to avoid saturation and operation in non-linear sections of the B-H curve.
5. Determine the dimensions of the coaxial transformer structure of the inductive adder stack.

The first four steps are described in Section 3.4. A point to note is that the resistive losses of semiconductor switches and other components of the primary circuit can initially be neglected. Dimensioning the coaxial transformer structure of the inductive adder is an iterative design process in itself and all the other design steps affect it. The detailed step-by-step example for determining the dimensions of the coaxial transformer for an inductive adder was presented by the author in [10] and the revised version of the design process is repeated in Section 3.5.

The primary loop inductance affects the output impedance of the adder stack, which is desired to be matched to the load impedance. The exact value of primary loop inductance is difficult to compute analytically and in the past an iterative process has been used to tune the output impedance [68]. In Chapter 4, a simulation method is presented to predict the primary loop inductance.

3.4 Selection of Components for the Inductive Adder

3.4.1 Semiconductor Switches and Power Transistors

Selection of the switching components for the inductive adder has been discussed in [40] and by the author in [10]. To sum up, each constant voltage layer of the adder stack must switch and conduct full load current, which may require several switches to be connected in parallel in each

layer and the parallel switches must have low time jitter. It is not important that each switch has the same on-state resistance, because each switch has its own capacitor, the switches are not directly in parallel, and hence current sharing is not a critical issue. The loop inductance of the primary circuits of the inductive adder must be very low to avoid high-voltage transients during turn-off. Thus, the package of the switch and layout of the PCB needs to be of low inductance. The maximum operation voltage of the semiconductor switches of the constant voltage layers defines the maximum operation voltage of the capacitor banks, and therefore the number of layers which are needed to generate a specified output voltage.

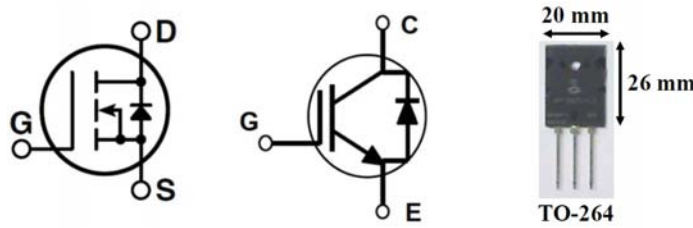


Figure 3.3. Drawing symbols of an N-channel MOSFET (left) [101] and an IGBT (center) [102] and a photo of a TO-264 package (right).

MOSFETs and IGBTs (Fig. 3.3), as well as other switch technologies can be used. The advantages of MOSFETs in the inductive adder applications are that the switching transitions are very short in duration, thus the switching losses are relatively low, the repetition rate of the pulses may be high and it is possible to generate short duration pulses. MOSFETs are also easy to control and they have low time jitter. The disadvantages of MOSFETs are that they presently have a relatively low voltage rating, up to 1.2 kV, and low current ratings, up to 150 A pulse current at 1 kV rating. Therefore parallel devices are needed for high currents and a low voltage rating may require more layers in the adder than with other switches with higher voltage ratings. Fast switch-off transitions of MOSFETs may also generate large voltage transients due to the energy stored in the parasitic loop inductances. Furthermore, MOSFETs do not have a reverse blocking capability. In order to avoid voltage induced failures, either clamping or snubber circuits, or both, are needed.

IGBTs are available with considerably higher maximum current and voltage ratings than MOSFETs, up to 600 A and 6.5 kV. They have relatively fast switching transitions and they can be used up to tens of kHz of switching frequency. IGBTs are also relatively easy to control and have

a low time jitter. The disadvantages of the IGBTs are that, during the turn-off, there is a tail current which may take hundreds of nanoseconds to extinguish and the turn-off delay time is often relatively long in comparison with rise and fall times. This excludes the use of the IGBTs for generating short duration pulses and in applications of very high repetition rate. In addition, in order to limit fault current, it is desirable to be able to turn off the switches with a small delay. As in the case of MOSFETs, a voltage induced failure is usually catastrophic for an IGBT and hence snubber circuits are frequently needed to protect the switch.

Semiconductor switches can have a long lifetime in pulse power systems if properly used. A certain voltage margin needs to be reserved to protect the switching components against cosmic ray failures and transients. In the case of MOSFETs, the operation voltage is often selected to be 70 % of the rated voltage as chosen in an example of the inductive adder design in [40]. However, a larger safety margin may be advisable for long-term reliability [103]. The core loss current and magnetising current need to be taken into consideration in defining the current rating for the switch. The magnetising current depends on the permeability of the core material of the transformers. In order to reach high electrical efficiency, the magnetising current should be a small fraction of the load current [104] and in designing the inductive adder it can be expected to be 15 %, as an average, of the load current during the pulse, for a suitable core [40].

The current ratings for the MOSFETs are usually shown in data sheets for a constant drain current, at certain junction temperatures, and for a pulsed drain current. The maximum pulse current is given for repetitive pulses the durations of which are limited by the maximum junction temperature. When a MOSFET is operating as an on-state switch, it is operating in its Ohmic region, in which the drain current depends on the drain-source voltage according to Ohm's law, similarly to a resistor. The Ohmic region is also called a linear region [105] and the operation mode is called a triode mode. This region is shown in Fig. 3.4 on the left side of the dashed curve. The pulse current rating gives the maximum current, with which the MOSFET still operates in the Ohmic region and with which the current density in the die or in the bond wires will not cause burn-outs [106]. If the operating point moves from the Ohmic region to the saturation region, any increase of drain current results in a significant increase in drain-source voltage and, therefore, a consequent rise in conduction loss [106]. In inductive adder designs, the maximum current through the

MOSFETs should typically have at least 100 % of margin, in comparison with the pulsed current rating, so that the temperature rise of the components is not notable [68].

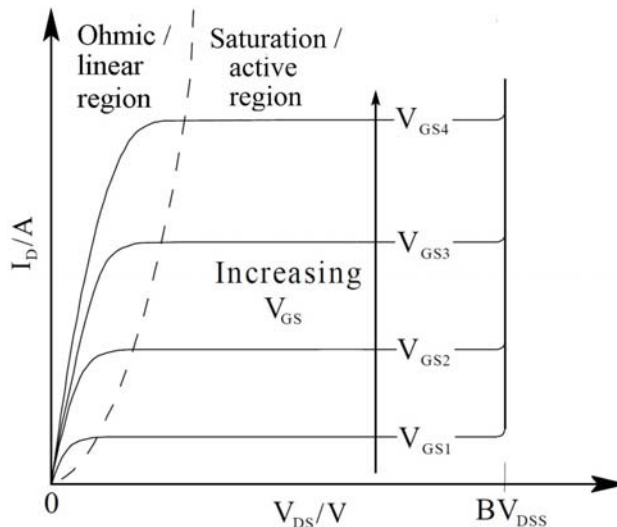


Figure 3.4. Drain current I_D of a MOSFET as function of drain-source voltage V_{DS} with different values of gate-source voltage V_{GS} . Revised after [106].

Analogue modulation techniques can be used to modulate the output voltage of the inductive adder and this may be necessary to keep output droop and ripple within the specifications. Applying this method requires power transistors which operate in the saturation region, in which a small variation of the gate-source voltage results in linear changes of the drain current, almost independently of the drain-source voltage. This operation mode corresponds to a voltage controlled current source. This region is shown on the right side of the dashed curve in Fig. 3.4 and the transistors are used in the saturation region.

Fast power transistors are commercially available, for example from Microsemi and IXYS, which have been designed to be operated in the saturation region and which are equipped with low inductance packages. These devices are based on MOSFET technology and they are called RF power MOSFETs by the manufacturers, in which the abbreviation RF means radio frequency. These components are available with voltage ratings up to 1200 V, pulse current ratings to tens of amperes and operating frequencies up to tens of MHz. On the contrary, IGBT manufacturers do not give specifications for the bandwidth in the linear mode of operation. The current sharing inside a multi-die IGBT may be bad, if used as a linear amplifier, and as a consequence the die may overheat even with low currents [107]. However, an active bouncer circuit has been presented in [108] in which

IGBTs are used as voltage controlled current sources. The modulation bandwidth of that circuit presented in [108] was 1 kHz [109] and it was limited by the driver circuit.

For the CLIC DR kicker inductive adder, use of RF power MOSFETs is the most desirable solution because of the availability of the purpose-built linear RF power MOSFETs which have proven bandwidth up to tens of MHz in a similar application [73]. Also, the expected current requirement of the modulation circuit for the CLIC DR kicker inductive adder is moderate. For example, in [73], the current through the linear MOSFET was a few percent of the total load current. To give an example for the CLIC DR kicker inductive adder, assuming 5 % of the nominal load current, 250 A, would mean 12.5 A of current through the RF power MOSFETs. This could be fed with a single RF power MOSFET.

3.4.2 Gate Drivers

In order to achieve fast rise and fall times of the output pulse and relatively low switching losses, switching-on and switching-off transition times of the drain-source current of semiconductor switches must be short. Gate drivers need to be able to provide sufficiently large current for rapidly charging and discharging the Miller capacitance of the gates of the switches. The gate drivers of the switches are referenced to ground in each layer of the inductive adder. In an analogue modulation layer, the gate driver needs to be a linear amplifier circuit which has a large bandwidth with considerable high current feeding capability, up to a few amperes. Fig. 3.5 shows an example of a linear gate drive circuit for RF power MOSFETs. In this circuit, input V_{Bias} sets the DC voltage of the gate pin of the RF power transistor to bias the transistor to the desired operating conditions. The high-frequency modulation signal is fed through two amplifier stages, the first of which provides voltage amplification and the second of which operates as a current buffer.

3.4.3 Capacitor Banks

The capacitor banks, shown as C_s in Fig. 3.1, feed current to the primary windings of the constant voltage layers when the switches are on. Historically, the capacitance of the capacitor banks has been considered to mainly define the voltage droop of the output waveform and the capacitance has been chosen according to the allowed droop of the output pulse

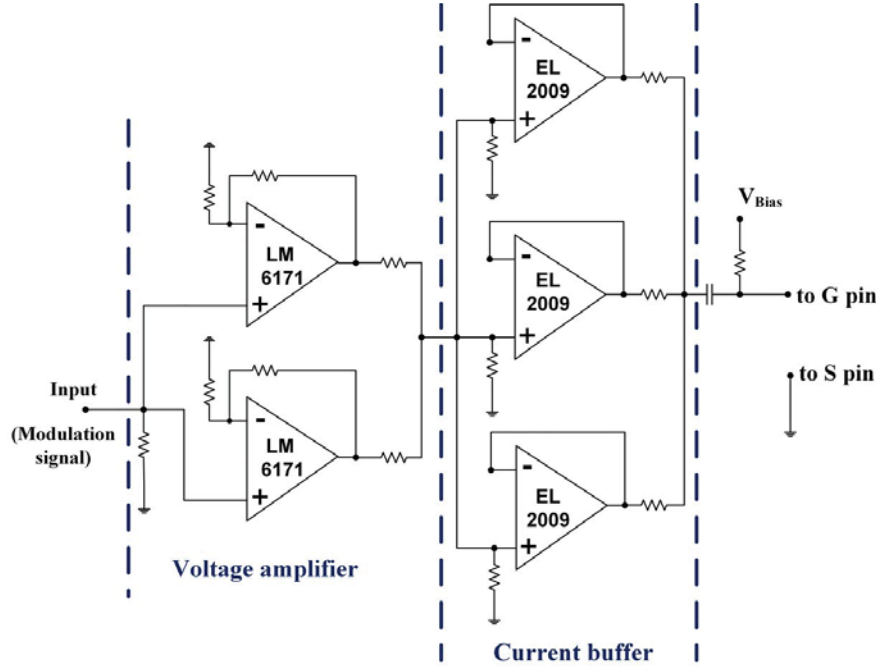


Figure 3.5. Example of a linear gate drive circuit. Revised after [73].

[40]. However this is not true for an inductive adder with very low droop (i.e. much less than 1 %), as the author has shown in [17] and briefly concluded in Chapter 4. Rather the resistive losses of the primary circuit together with increasing magnetising current of the magnetic cores may cause much larger droop for the output waveform than that caused by the voltage droop of the capacitor banks, and this droop cannot be compensated by adding more capacitance per layer. However, the approach presented in [40] and below gives a reasonable first estimate for choosing the capacitance for the capacitor banks in order to keep the portion of the total droop, which is caused by the capacitor bank, within the desired value.

The total droop of the output of the inductive adder is summed over all the layers. Therefore, the absolute voltage droop of an individual layer in the adder stack, with N layers, is allowed to be $(1/N)^{\text{th}}$ of the permitted absolute voltage droop of the inductive adder. According to [40], the estimate for the required capacitance, C_s , per layer for a given droop per layer, ΔV_{pl} , flat-top pulse duration t_p and required primary current I_p can be calculated, from the following equation:

$$C_s = \frac{I_p t_p}{\Delta V_{pl}} \quad (3.4)$$

In Eq. (3.4), the primary current I_p is the sum of the load current, the

magnetising current and the core-loss current of the magnetic core of the layer.

It is important to note that the total droop of the output waveform may be much larger than the droop which is caused by limited capacitance per layer, as was shown in [17] by the author. In addition, it may even be impractical to fit the required capacitance, given by Eq. (3.4), on the PCB. Analogue modulation methods may be used to compensate the voltage droop of the output waveform, regardless of the source of the droop, as is shown in Chapters 4 and 5.

The capacitors need to have extremely low inductance [71], [72] especially to avoid large voltage transients during turn-off, caused by the energy stored in the parasitic loop inductance. This may require custom-made capacitors which have wide low-inductance leads. The capacitors need to be located close to the transformer primary, with a wide return path on the other side of the PCB, to keep the total loop inductance of the primary circuits low.

3.4.4 Magnetic Cores

Core Material

The transformers of the inductive adder must provide adequate insulation between the primary and secondary windings. The secondary windings of the transformers are connected in series whereas the primary windings are each referenced to ground. Both primary and secondary windings consist of a single turn to keep the bandwidth of the transformer high. With a coaxial design of the transformer and the inductive adder stack, the high voltage is present only inside the adder structure and at the high-voltage connectors of the adder. The secondary conductor is usually a straight conducting rod which goes axially through all the primary layers and it is also referenced as a "stalk". Each primary must provide both the full load current, the core loss current and the magnetising current of the transformer. Ideally, the magnetising inductance should be as high as possible to minimise the magnetising current.

Figure 3.6 shows an example of the B-H curve of a magnetic core. The maximum output pulse duration of the inductive adder is limited by saturation of the magnetic core. The maximum available flux density swing of the magnetic core is from the negative remanence to the positive saturation. If both the positive and negative range of the flux-density swing

are to be used, the core needs to be biased to a negative remanent field after each pulse. A reset and biasing circuit may be either passive or active and it forces the magnetic flux of the magnetic cores to a negative value after the pulse. For ferrite cores, the maximum flux-density swing is only approximately 0.5 T. Cores made of nanocrystalline material could allow maximum flux-density swings up to 2 T [110] and cores made of amorphous alloys up to 3.4 T [111]. The nanocrystalline cores and cores made of amorphous materials are manufactured from thin wound tape with insulation between each turn.

For achieving good flat-top stability, it is recommended to remain within the linear region of the B-H curve of the magnetic core, shown in Fig. 3.6, to avoid non-linearities which will be more difficult to compensate for. Also, in the non-linear region, the magnetising current would start to increase rapidly, which would increase the stress on components such as the semiconductor switches. Inductive adders are typically designed to have a significant margin between the available and usable flux density swing [112]. A reasonable first estimate for the usable flux density swing is e.g. a half of the flux-swing range from the positive saturation to the negative remanence [112], however this depends on the core material. In addition the material should be chosen such that temperature variations of the core do not result in non-linear B-H characteristics, over the working range of the B-H curve. The effective permeability of the core material depends on the frequency content of the pulse. A core with square-loop magnetising characteristics could potentially have the highest permeability and the lowest magnetising current. A drawback of a core material with a square-shaped B-H curve is the necessity to use a reset and biasing circuit, because the remanent magnetic field is close to saturation. If a core material is used which has a large linear region of the B-H curve and which has very low remanence value, close to 0 T, approximately a half of the maximum flux-swing may be theoretically usable during the pulse without biasing.

Insulation Requirements

The magnetic cores used in an inductive adder need to have adequate insulation for fast pulse application, in order to avoid break down and hence large interlaminar eddy currents between adjacent turns. In [113], the following equation is presented for estimating the voltage stress across an insulation layer, V_{cl} , between two adjacent ribbon turns in a tape-wound

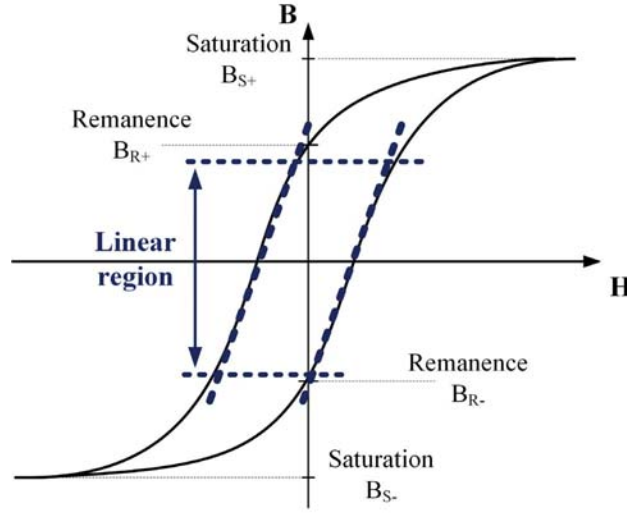


Figure 3.6. Example of a hysteresis loop of a magnetic material.

core:

$$V_{cl} = l_c t_r \frac{\Delta B}{\Delta t}. \quad (3.5)$$

In Eq. (3.5), l_c is the height of the ribbon, t_r is the thickness of the ribbon, ΔB is the change of the flux density and Δt is the time period for the change of the flux density. The interlaminar voltage stress may be much higher during fault conditions than during normal operating conditions, because of potentially faster current rise time and therefore higher magnetisation rate.

Core Dimensions

The required ECSA of the magnetic core, $A_{c,eff}$, is computed from the effective pulse duration $t_{p,50}$ and pulse voltage V_c divided by the maximum flux-density swing ΔB which is to be used. The effective pulse duration $t_{p,50}$ is the duration of the pulse at half maximum, which is the sum of the pulse flat-top duration and a half of the rise and fall times, assuming a linear rise and fall of the voltage.

Thus, the minimum ECSA of the core can be estimated from the following equation:

$$A_{c,eff} \approx \frac{V_c \times t_{p,50}}{\Delta B} \quad (3.6)$$

The larger the flux-density swing of the core material, the smaller is the required cross-sectional area of the magnetic core. The magnetic core of

the inductive adder should never saturate, because the saturated core is seen as very low inductance by the circuit of the primary layers, which may cause very large fault currents and thus destroy the semiconductor switches. To avoid saturation, the ECSA of the core has to be large enough for all operating conditions. A fairly large margin, for example 100 % [40], is recommended to avoid the magnetic core becoming saturated during normal operating or fault conditions. The ECSA increases linearly as a function of the effective pulse duration $t_{p,50}$.

In addition to the ECSA, the inside radius of the core must be large enough that the magnetic field does not saturate the inside turns of the core. The saturation of the inside turns may happen before the complete core becomes saturated, because the magnetic path length of the inside turns is shorter than the average magnetic path length of the core. For a single-turn, the magnetic field H in the core as a function of the diameter of a magnetic path, d_{mp} , is given by the following equation:

$$H = \frac{I_{Lm}}{\pi d_{mp}} \quad (3.7)$$

In Eq. (3.7), H is magnetic field, I_{Lm} is magnetising current and d_{mp} is the diameter of a magnetic path length of the core. By applying this equation and using the inside diameter of the core, the maximum magnetic field applied to the core turns can be estimated. However, a problem in applying Eq. (3.7) is that the magnetising current I_{Lm} needs to be estimated. The magnetising current depends on the magnetising inductance, as it is shown in Eq. (3.2). The magnetising inductance depends on the permeability of the core and the effective permeability of the core depends on the magnetisation of the core and the frequency content of the pulse. In the early design phase, all these parameters may not be known exactly. However, if the maximum outside diameter of the core is allowed to be, for example, only two times larger than the inside diameter of the core, the magnetic field H at the inside diameter is, as a maximum, two times larger than in the outside diameter of the core. If only the linear part of the B-H curve is taken into consideration in defining the maximum usable flux-swing and a 100 % margin is applied for the ECSA of the core, approximately 50 % of the linear B-H curve is not used during normal operating conditions. Thus, during normal operating conditions, the average magnetic field could be increased by 50 % before the B-H curve becomes non-linear. This means that the inside diameter of the core stays in the

linear part of the B-H curve with the applied magnetisation and would not be saturated. By applying the design rules shown above, namely using only the linear part of the B-H curve with a 100 % margin and limiting the outside diameter of the core to be less than two times the inside diameter of the core, the inside diameter of the core is not driven into saturation during the normal operating conditions.

Core Losses

In the inductive adder design presented in this dissertation, the core housing encloses the magnetic cores completely. Therefore, it is necessary to estimate the core losses in order to evaluate if cooling by natural convection is adequate, or if e.g. cooling by forced air or liquid is needed. The temperature of the magnetic material should be kept below Curie temperature in all operating conditions. Also, the maximum continuous operation temperature for tape-wound cores may be much lower than the Curie temperature, and it depends on the insulation material between the ribbon turns and the material of the case of a core, if the core is encapsulated. To give two examples, the Curie temperature for Vitroperm 500 F nanocrystalline material is above 600 °C and the maximum continuous operation temperature for an epoxy-coated core is 120 °C [114], and for Metglas 2605CO material the Curie temperature is 567 ± 10 °C [115] and the maximum continuous operation temperature of this core is 125 °C [111].

In the literature, the losses in a magnetic core are divided in three parts, namely hysteresis losses, classical eddy current losses and excess or anomalous losses [116]. The hysteresis losses of magnetic materials can be estimated with the Steinmetz equation [117] and further developed versions of this method for non-sinusoidal waveforms, namely modified Steinmetz equation [118], [119], generalised Steinmetz equation [120], improved Steinmetz equation [121], and improved-improved Steinmetz equation [122].

Each of these methods has some imperfections in describing the core losses and they require parameters, so called Steinmetz coefficients, which are usually not available for custom-made tape-wound magnetic cores. Also, the loss models, which are developed for sinusoidal waveforms, are not directly applicable for rectangular or trapezoidal voltage pulses. Accurate estimate for the core losses, under pulsed conditions, requires measurement of the current of a magnetic core with a representative voltage

waveform and an open-circuit secondary.

The dominant loss mechanism in tape-wound cores with high magnetisation rates is eddy current losses [40]. As a first estimate of the core losses, it is convenient to apply a method which is based only on the available material parameters and the geometry of a magnetic core.

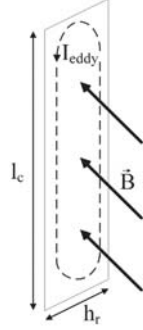


Figure 3.7. A cross-section of a strip of a magnetic material with an induced magnetic field $\vec{B}$.

In [123], the eddy current power loss per unit volume (W/m^3) for a strip of a thin magnetic material with a rectangular cross-section, shown in Fig. 3.7, is given as follows:

$$P_{c,pv} = \frac{h_r^2}{12\rho} \left(\frac{dB}{dt} \right)^2 \quad (3.8)$$

In this equation, h_r is the thickness of the strip of a magnetic material, ρ is the resistivity of the ribbon and dB is the change of the magnetic field inside the ribbon during a time dt . The second term of the equation, the rate of change of magnetic field, can be expressed as follows:

$$\frac{dB}{dt} = \frac{V_c}{A_{c,eff}} \quad (3.9)$$

In Eq. (3.9), V_c is the voltage which is applied across the magnetic core and $A_{c,eff}$ is the effective cross-sectional area of the magnetic core. In applying Eq. (3.9) it is assumed that the rate of change of magnetic field is homogeneous throughout the cross-section of the magnetic core and the voltage V_c is a constant during a pulse.

By substituting Eq. (3.9) into Eq. (3.8) and taking the effective volume of the magnetic core, i.e. the volume of the magnetic material of the core, into account, the power loss P_c (W) of a tape-wound core can be written as follows [124]:

$$P_c = \frac{h_r^2 V_c^2 V_{e,\text{eff}}}{12 \rho A_{c,\text{eff}}^2} \quad (3.10)$$

The effective cross-sectional size of a magnetic core, $A_{c,\text{eff}}$, can be estimated as follows:

$$A_{c,\text{eff}} = h_r l_c N_t \quad (3.11)$$

In Eq. (3.11), N_t is the number of turns of the ribbon of a tape-wound magnetic core and l_c is the height of the ribbon of a the magnetic core. The effective volume of the core, $V_{e,\text{eff}}$, can be estimated with the following equation:

$$V_{e,\text{eff}} = h_r l_c N_t l_{\text{mean}} \quad (3.12)$$

In Eq. (3.12), l_{mean} is the mean length of a single turn of the ribbon of a tape-wound magnetic core.

By substituting Eq. (3.11) and Eq. (3.12) into Eq. (3.10), P_c , can be expressed as follows:

$$P_c = \frac{V_c^2 h_r l_{\text{mean}}}{12 \rho l_c N_t} \quad (3.13)$$

The eddy current losses, P_c , can be expressed as a loss resistance, R_c , with the following equation:

$$R_c = \frac{V_c^2}{P_c} \quad (3.14)$$

By substituting Eq. (3.13) into 3.14, the estimate for the loss resistance of a core, R_c , can be written as:

$$R_c = \frac{12 \rho l_c N_t}{h_r l_{\text{mean}}} \quad (3.15)$$

The core loss resistance R_c , given by Eq. (3.15), can be used as the first

estimate for calculating the core losses of an inductive adder. The equivalent core loss resistance for an inductive adder can be estimated experimentally by measuring the current of a single layer with an open-circuit secondary. This method is presented in Appendix B of this dissertation.

Reset and Biasing

The magnetic cores of the inductive adders need to be demagnetised after the pulses. In Fig. 3.1, in the schematic of a constant voltage layer, a diode is shown in parallel with the primary of the transformer. When the switches of a constant voltage layer are turned off at the end of the pulse, the primary current starts flowing through the diode, which induces a voltage over the magnetising inductance with the opposite polarity in comparison with the pulse voltage. This voltage causes the flux-density of the cores to decay. The decay time depends on the pulse voltage, pulse duration and the forward voltage of the diode. An estimate of the decay time, which can also be considered as the reset time, can be computed by dividing the maximum nominal voltage per layer by the forward voltage of the diode and multiplying this by the pulse duration. When the current stops flowing in the diode, the flux-density of the core is expected to be the positive remanence value of the flux-density swing. As mentioned in Section 3.2.1, the decay time can be reduced by connecting a Zener diode in series with each diode.

The reset and biasing of the cores, which could be applied for example by feeding a constant DC current through the cores through a large inductor [71], would ensure that most of the usable flux-density swing is available during the pulse and the starting point of the flux-density swing of the cores would ideally be exactly the same for each pulse. However, in reality a pulse voltage across the reset and biasing circuit would result in a change of the reset and biasing current. In order to ensure that the starting point on the B-H curve is the same, the biasing and reset current must return to exactly the same point before the next pulse. In addition, the starting point on the B-H curve depends on the recent history of the magnetic material, i.e. operating voltage and pulse duration. If the repetition rate is too high, the starting point of the flux-density swing may begin to drift, if the current of the diode does not decay completely before the next pulse begins. This could lead the flux-density to reach saturation at the end of a pulse, even in the case in which the total flux-density swing caused by the pulse is smaller than the difference between the remanent

flux-density and the saturation flux-density. A simple DC reset circuit, consisting of a large inductor and a DC supply, as presented for example in [125], could cause flat-top ripple for the output pulse. Also, in [126] it is mentioned that a DC reset circuit could cause undesired intra-pulse ripple which also would not be acceptable for the CLIC DR extraction kicker system.

3.5 Dimensioning of the Inductive Adder Stack

3.5.1 Mechanical Design of the Inductive Adder Cell

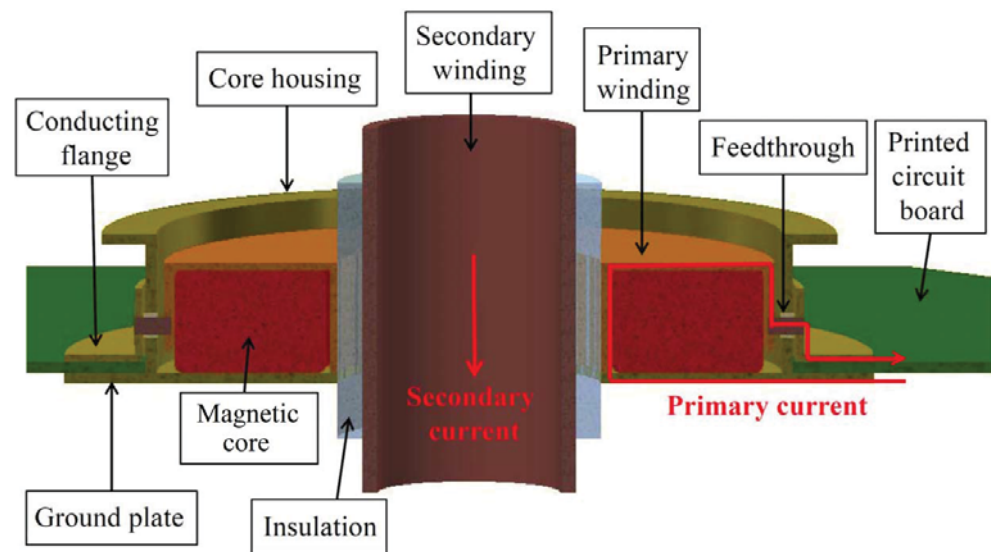


Figure 3.8. Cross-section of a single layer of an inductive adder stack.

Figure 3.8 shows the cross-section of a three-dimensional model of a single layer of the inductive adder stack. The figure visualises approximately relative dimensions, parts and assembly of the stack. The circuit elements located on the PCB, e.g. pulse capacitors, are not shown. The PCB of the primary circuit, which includes the pulse capacitors, switches and transient voltage protection circuits, is connected to the primary winding via a conducting flange. In this design, there are feedthroughs between the conducting flange and the primary winding, and two of these are shown in Fig. 3.8. The primary winding is made of conducting, non-magnetic metal or alloy which surrounds the magnetic core with a single turn. The secondary winding is a non-magnetic metal rod, which passes through the central hole of all the magnetic cores of the adder stack. Insulation is also shown and it may be an air gap or dielectric material. The ground plate,

which is on the lower side of the magnetic core, provides the return path for the primary current to the bottom side of the PCB. It is connected to ground potential. The core housing is made of conducting non-magnetic metal, for example aluminium, and it is also the support structure of the adder stack. In the design shown in Fig. 3.8, the core housing is also at ground potential and its upper side can be fastened to the ground plate of the adjacent layer by screws. A photo of a typical inductive adder cell with the similar design is shown in Fig. 3.9.

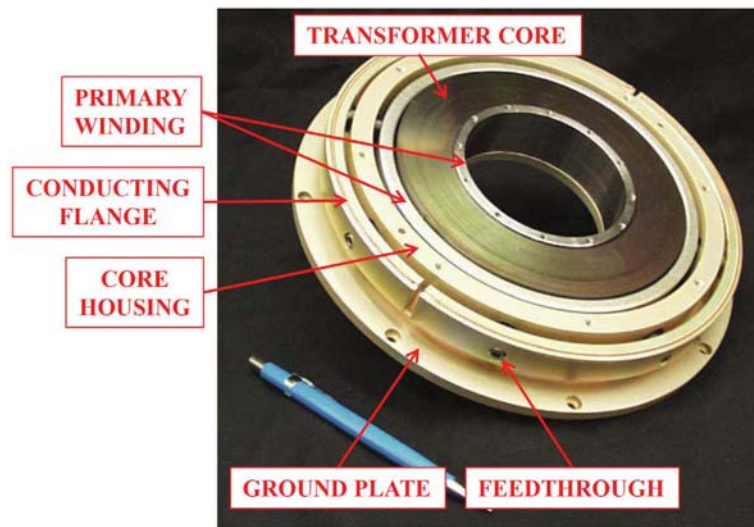


Figure 3.9. An example of an inductive adder cell developed at LLNL. Revised after [110].

In more recent designs, for example in [81], the magnetic core is housed between two metal flanges. An example of such design is presented in Fig. 3.10. This design, which was originally developed at LLNL, has been used in the prototype inductive adders presented in this dissertation. The structure is mechanically much simpler than the design shown in Fig. 3.8. The left photo of Fig. 3.10 shows a single bottom flange with a magnetic core. The bottom flange is at ground potential. In the right photo of Fig. 3.10 a top flange is assembled on the bottom flange. This structure comprises a single inductive adder cell. The PCBs are inserted between the flanges and good electrical connection between the PCBs and the flanges can be ensured via spring-loaded sliding contacts. The high-voltage pulse from the PCBs is fed into the top flange. The bottom flange is electrically connected to the adjacent bottom flanges by metal spacers. There are holes for these spacers in each top flange as shown in the right photo of Fig. 3.10. Assembled spacers are visible in Fig. 3.11.

Figure 3.11 shows an assembly of the stack of a prototype inductive

adder at CERN. The secondary winding (stalk) is a metallic, non-magnetic straight rod which passes through the centre hole of each flange. The inductive adder cells are attached together with threaded bars. The flanges are made of aluminium and they are finished with iridite coating [127], to prevent oxidation and to maintain good electrical conductivity of the contact surfaces of the flanges.

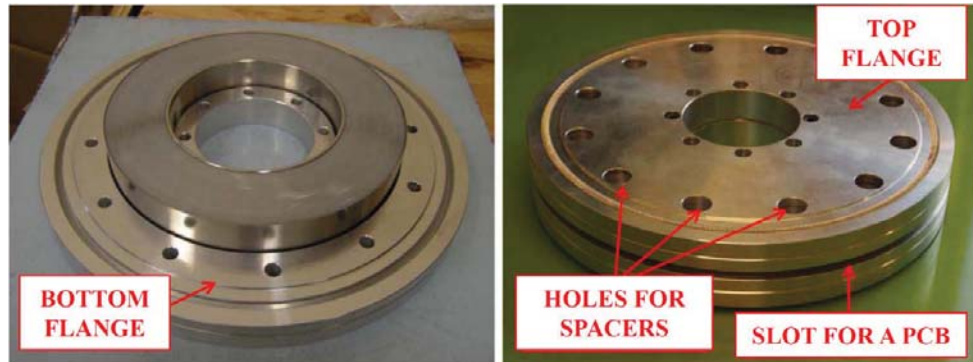


Figure 3.10. A single bottom flange of an inductive adder with a magnetic core (left) and a single cell (right).

The space between the primary and secondary windings can be filled with dielectric material to provide sufficient insulation between the high-voltage secondary and the low-voltage primary circuits. Below 20 kV, air insulation may be sufficient [68]. The mechanical and electrical design of the prototype inductive adders built at CERN are explained more in detail in Chapter 5 and in Appendix A of this dissertation.

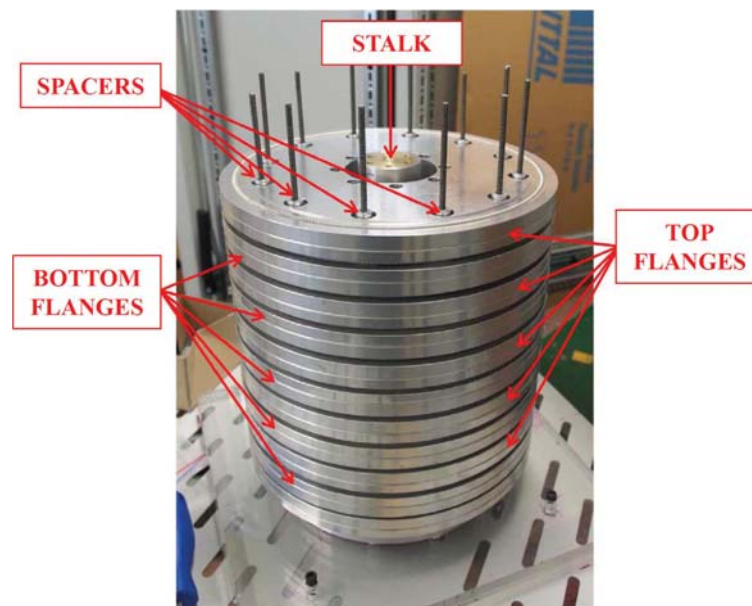


Figure 3.11. An assembly of a prototype inductive adder at CERN (without PCBs).

3.5.2 Equations for Defining Electrical Parameters of the Inductive Adder Cell

Figure 3.12 shows a generalised equivalent circuit for a single layer for the inductive adder. Fig. 3.13 presents an illustration of the coaxial transformer structure of a single inductive adder cell and Fig. 3.14 shows a cross-section of an inductive adder cell. The total primary loop inductance L_{pl} can be very small, a few nanohenries [15], because the single turn primary has a relatively short electrical length and the primary conducting path has a large cross-sectional area. The primary resistance R_p is also small, much less than an Ohm [44], because the primary winding encloses the core and it is a relatively short length. In order to avoid excess voltage droop during the pulse, the total loop resistance of the primary circuit should be less than $1\ \Omega$ [72]. The parasitic elements in the secondary circuit, which are secondary inductance L_{ss} , secondary resistance R_s and coupling capacitance C_c between primary and secondary, are dominated by the stalk and its proximity to the core housing. The primary leakage inductance is assumed to be negligible for a single-turn primary, which encloses the magnetic core completely [40] and therefore it is not included into the model in Fig. 3.12. However, this assumption requires that the space between the primary winding and the core is negligible.

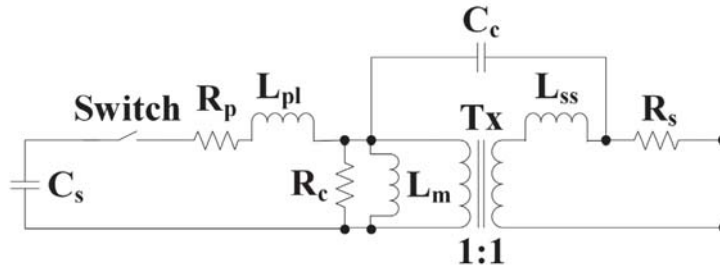


Figure 3.12. Simplified equivalent circuit of a single layer of an inductive adder.

References [104] and [128] give analytical equations for secondary inductance L_{ss} and for coupling capacitance C_c between each primary and the secondary winding. In [128], L_{ss} corresponds to the distributed inductance of the stalk per cell length and, because of the coaxial nature of the structure, the equation is the same as given in [39] to calculate the inductance of a coaxial cable. The equation for L_{ss} given in [128], using notations shown in Fig. 3.13, can be written as follows:

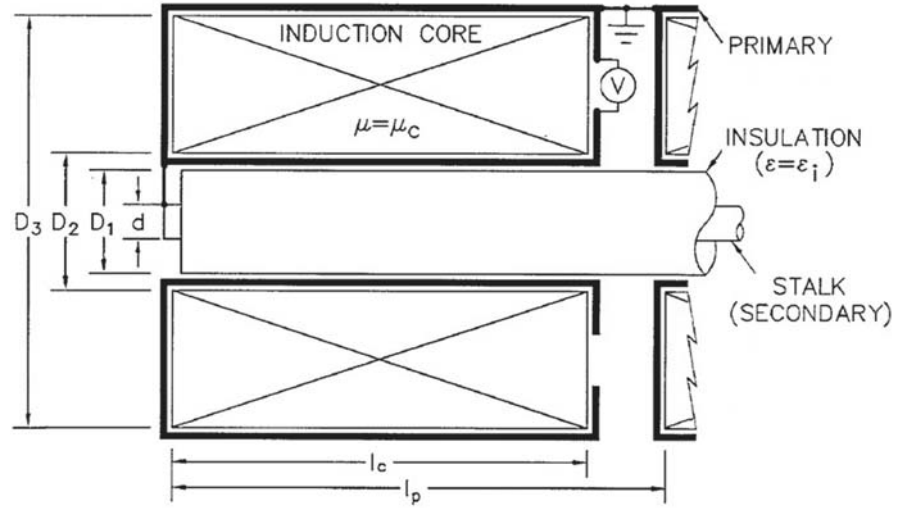


Figure 3.13. Illustration of an inductive adder cell. Revised after [104].

$$L_{ss} = \frac{\mu_0 l_p}{2\pi} \ln \frac{D_1}{d} \quad (3.16)$$

In Eq. (3.16), l_p is the length of the adder layer, D_1 is the inside diameter of the cylindrical core housing, d is the outside diameter of the stalk and μ_0 is the permeability of free space. Any insulation between the core housing and the stalk is assumed to be non-magnetic. Theoretically, Eq. (3.16) is valid for an infinite length of a coaxial cable. In reality, the length of an inductive adder cell is typically a few centimetres and the outer conductor of the coaxial structure is not continuous. The gap between the adjacent core housings is typically less than 10 % of the length of a cell, l_p . Also, the coaxial structure is not uniform close to the top and bottom ends where the stalk is connected to feedthroughs. However, Eq. (3.16) gives a reasonable, but slightly low, analytical estimate for L_{ss} . In Fig. 3.13, the secondary resistance R_s is the stalk resistance per cell length l_p .

The coupling capacitance, C_c , is given by the following equation [104], [128]:

$$C_c = \frac{2\pi\epsilon_i l_p}{\ln \frac{D_1}{d}} \quad (3.17)$$

In this equation ϵ_i is the product of the permittivity of free space and the relative permittivity of the insulation between the primary winding and the secondary stalk. C_c corresponds to distributed capacitance of the stalk per cell length [128], [129]. Similarly to Eq. (3.16), Eq. (3.17) is

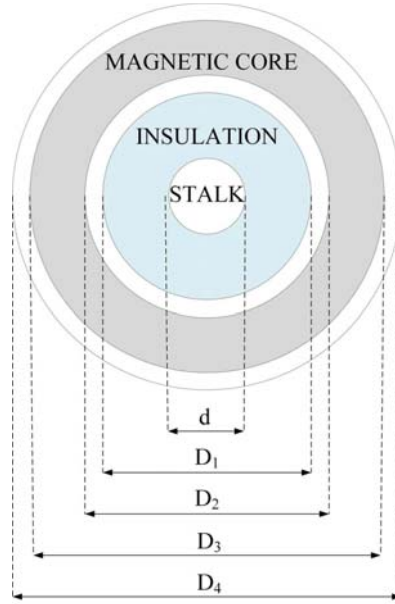


Figure 3.14. Cross-section of an inductive adder cell.

also defined for an ideal coaxial cable which has an infinite length. Therefore, Eq. (3.17) gives an approximation for the coupling capacitance of an inductive adder cell.

A general equation for magnetising inductance, or self-inductance, of a magnetic core is given as follows:

$$L_m = \frac{\mu_c N_w^2 A_{c,eff}}{l_{mean}} \quad (3.18)$$

In Eq. (3.18), N_w is the number of turns of the primary winding, $A_{c,eff}$ is the effective cross-sectional size of a magnetic core and l_{mean} is the mean magnetic path length of a core. μ_c is the permeability of the magnetic core, which is the product of the permeability of free space, μ_0 , and the relative permeability of the magnetic core, μ_r . A first approximation for the mean magnetic path length, l_{mean} is the arithmetic average value of the inside and outside circumferences of the core, l_{av} . This is given by the following equation:

$$l_{av} = \frac{\pi(D_3 + D_2)}{2} \quad (3.19)$$

In Eq. (3.19), D_2 is the inside diameter and D_3 the outside diameter of the core. A more accurate estimate for the mean magnetic path length of a toroidal core with a rectangular cross-section is given by the following equation:

$$l_{\text{mean}} = \frac{\pi(D_3 - D_2)}{\ln \frac{D_3}{D_2}} \quad (3.20)$$

Derivation of Eq. (3.20) is shown in detail for example in [130].

By substituting Eq. (3.20) to Eq. (3.18) the following equation can be written for a magnetising inductance of a toroidal core:

$$L_m \approx \frac{\mu_c N_w^2 A_{c,\text{eff}}}{\pi(D_3 - D_2)} \ln \frac{D_3}{D_2} \quad (3.21)$$

If the number of turns, N_w is 1, Eq. (3.21) can be simplified as follows:

$$L_m \approx \frac{\mu_0 \mu_r A_{c,\text{eff}}}{\pi(D_3 - D_2)} \ln \frac{D_3}{D_2} \quad (3.22)$$

Eq. (3.22) is valid for operation in the linear region of the B-H curve (Fig. 3.6), in which case the permeability μ_r is constant and hence does not depend on applied magnetic field H . For a tape-wound core, which consists of a wound ribbon with an insulation between adjacent layers, the packing factor needs to be taken into account. With these parameters, the equation for magnetising inductance can be written as follows:

$$L_m \approx \frac{C_{\text{PF}} \mu_0 \mu_r A_c}{\pi(D_3 - D_2)} \ln \frac{D_3}{D_2} \quad (3.23)$$

In Eq. (3.23), C_{PF} is the packing factor of the magnetic core, which is the ratio of the cross-sectional area of the magnetic material to the total cross-sectional area of the core. The effective cross-sectional area of the core depends on the selected core material and insulation.

$$A_{c,\text{eff}} = C_{\text{PF}} A_c \quad (3.24)$$

The core must provide the required volt-seconds for the pulse duration so that it is never driven into saturation, as discussed in Section 3.4.4.

According to Fig. 3.13, the outside diameter D_3 , the inside diameter D_2 and the length of the core l_c need to be adjusted to satisfy the following equation:

$$A_c = l_c \frac{(D_3 - D_2)}{2} \quad (3.25)$$

In 3.25 A_c is the actual cross-sectional area of the magnetic core of one layer.

The minimum core inside diameter D_2 is defined by two requirements: it needs to be large enough that the magnetic field, induced by the magnetising current, does not drive the inside turns of the core into saturation, and there needs to be space for sufficient insulation between the secondary winding and the core housing, which encloses the magnetic core. The required space for insulation depends on the output voltage of the inductive adder and chosen insulation material. To avoid saturation, a fairly large margin, e.g. 100 %, is recommended for the effective cross-sectional area of the core [40]. The secondary inductance per layer increases with increasing cell length according to Eq. (3.16). The magnetising inductance increases with increasing core length, as shown in Eq. (3.23) and Eq. (3.25). The parasitic coupling capacitance C_c can be reduced by decreasing the diameter of the stalk, d , according to Eq. (3.17), but this increases the secondary inductance L_{ss} , as is seen from Eq. (3.16).

3.5.3 Electrical Characteristics of the Inductive Adder Stack

The adder stack can be used as a bipolar or single-ended voltage source. The pulses produced by each layer will propagate bi-directionally and add up at the load. If the inductive adder is used as a bipolar source and is terminated at both ends with matched impedance loads, the pulse rise time of the outputs are influenced by the one-way propagation time of a TEM pulse through a layer multiplied by the number of the layers [129]. The single way electrical propagation delay through the secondary of the inductive adder can be estimated from the following equation [129]:

$$T_{rd,1w} = N \sqrt{(L_{pl} + L_{ss})C_c} \quad (3.26)$$

in which L_{pl} is the primary loop inductance, L_{ss} is the secondary inductance per cell, and C_c is the distributed capacitance per cell length, which corresponds to coupling capacitance.

The electrical propagation delay time of a single-ended adder stack, with a matched impedance load and a direct connection to ground on the other end, is the two-way propagation time of the TEM pulse from the top of the stack to the bottom and back [112]. This can be written as [129]:

$$T_{rd,2w} = 2N\sqrt{(L_{pl} + L_{ss})C_c} \quad (3.27)$$

The output impedance of the stack has to be matched to the load to avoid reflections and to keep the rise and settling time of the output pulse short. Neglecting the primary loop resistance and secondary resistance, the output impedance of an inductive adder depends on the coupling capacitance C_c , secondary inductance L_{ss} and primary loop inductance L_{pl} , according to the following equation [129]:

$$Z_{out} = \sqrt{\frac{L_{pl} + L_{ss}}{C_c}} \quad (3.28)$$

The above parameters, except the primary loop inductance L_{pl} , can be computed from the stalk dimensions and layer dimensions and material parameters, as shown below. The primary loop inductance must be estimated from the dimensions of the primary circuit and core housing, or determined numerically.

3.5.4 Design Steps for an Inductive Adder Cell

The design of the cell requires definitions for the following parameters: the stalk diameter d , the diameter of the inside wall of the primary winding, D_1 , the cell height l_p and the dielectric constant, ϵ_i , of the insulation material between the stalk and the inside wall of the primary winding. The inside diameter of the core, D_2 , the height of the core, l_c , and the outside diameter of the core, D_3 , can be defined after defining the parameters D_1 and l_p . The minimum value of the inside diameter of the core, D_2 , is larger than the diameter of the inside wall of the primary winding, D_1 . The maximum value of the height of the core, l_c , is smaller than the cell height l_p . The outside diameter of the core, D_3 , can be defined after defining the inside diameter of the core D_2 and the inside diameter of the inner wall of the primary winding, D_1 .

The following design constraints effect the dimensions of the cell: the required output impedance Z_{out} , the permittivity ϵ_i of the insulation material between the stalk and the inside wall of the primary winding, and the minimum height of a single layer including the thickness of the PCB, the maximum height of the components and the thickness of the PCB. The output impedance depends on the secondary parasitic inductance L_{ss} ,

coupling capacitance C_c and the primary loop inductance L_{pl} . L_{ss} and C_c depend on the dimensions d and D_1 and on permeability and permittivity of the insulation material. The primary loop inductance L_{pl} depends on the primary circuit design, e.g. the number of parallel current branches and the inductance of a single branch. It cannot be computed analytically easily and, therefore, it needs to be estimated for the preliminary design. The insulation material defines the maximum applicable electric field between the stalk and the inside wall of the primary winding. For a coaxial structure, the maximum electric field between the primary and secondary windings can be computed with the following equation:

$$E_{\max} = \frac{V_{\text{out}}}{\frac{d}{2} \ln \frac{D_1}{d}} \quad (3.29)$$

In Eq. (3.29), V_{out} is the output voltage of the inductive adder, d is the outside diameter of the stalk and D_1 is the inside diameter of the inner wall of the primary winding. In this equation, it is assumed that the coaxial structure is infinitely long and that the inside wall of the primary winding is continuous. In reality this is not true and the electric field will be higher than that given by Eq. (3.29) at the pulse output end of the structure. Thus it may be desirable to radius the corners of the inside inside diameter of the core housing.

One goal of the design of a cell for the CLIC DR kicker inductive adder is to achieve good impedance matching between the inductive adder and the cables, striplines and a terminating resistor. Good impedance matching minimises reflections between the parts of the kicker system and, therefore, reduces the ripple of the pulse flat-top. This keeps settling time short and reduces the minimum duration of the pulse flat-top, as is shown in Fig. 4.25. The goal of the presented design procedure is to meet both the required output impedance and the insulation requirements. This design approach is not optimised regarding the other possible design parameters, e.g. size and cost. Dimensioning of an inductive adder cell may require several iterative steps. Also, a few assumptions needs to be made in the beginning of the design process. The following steps describe a design flow for the inductive adder cell.

1. Choose the initial insulation material for the gap between the stalk and the primary winding. This choice defines the permittivity ϵ_i and the maximum applicable electric field of the insulation material. Accord-

ing to [68], air insulation is generally suitable for inductive adders up to 20 kV output voltage but this will depend upon the design and the maximum electric field inside the stack.

2. Estimate the primary loop inductance L_{pl} . The output impedance of the inductive adder can be computed with Eq. (3.28) but parameter L_{pl} cannot be computed easily analytically. The primary loop inductance consists of a parallel connection of several current branches, therefore it is expected to be low, in the region of a few nanohenries. In previous designs of the inductive adders, an approach has been to use an estimate for L_{pl} which is larger than the expected real value. This leads to slightly too large stalk diameter d , which can be then machined smaller to adjust the impedance to the required value [68].
3. Define the initial minimum length of a single cell. The length of a single cell of an inductive adder is defined by either the height of the components of the primary layers, e.g. pulse capacitors, or the height of the magnetic cores. In an iterative design process of an inductive adder, the length of the cell is one of the parameters which can be changed in order to meet the requirements.
4. Define the minimum diameter of the stalk, d , and the minimum inside diameter of the inner wall of the primary winding, D_1 . Substituting Eq. (3.16) and Eq. (3.17) to Eq. (3.28) gives the following equation:

$$Z_{out} = \sqrt{\frac{L_{pl} + \frac{\mu_0 l_p}{2\pi} \ln \frac{D_1}{d}}{\frac{2\pi \epsilon_i l_p}{\ln \frac{D_1}{d}}}} \quad (3.30)$$

For Eq. (3.30), all other parameters except d and D_1 have been defined above and the ratio of D_1 to d is constant for a required output impedance Z_{out} . The minimum value for d can be determined by writing Eq. (3.29) as follows:

$$d = \frac{V_{out}}{\frac{E_{max}}{2} \ln \frac{D_1}{d}} \quad (3.31)$$

By substituting the ratio D_1 to d and the acceptable maximum electric field E_{max} in Eq. (3.31), the minimum value for d can be solved.

5. Define the dimensions of the magnetic cores. These are the height l_c ,

the minimum inside diameter D_2 and the minimum outside diameter D_3 of the magnetic core. Repeat steps 3. and 4. if the core length is longer than the defined initial cell length. The primary winding encloses the magnetic core completely. The inner wall of the primary winding serves as the mechanical structure of the inductive adder stack and therefore the thickness of the primary winding should be relatively large, for example 10-15 mm. In addition to this, tape-wound cores are wrapped around a mandrel, the thickness of which is typically 2-5 mm. Therefore, the inside diameter of the core, D_2 should be at least 24 mm larger than the inside diameter of the inner wall of the primary winding, D_1 .

6. Check that the design requirements are met. One of these can be, for example, the minimum single-way propagation delay of the pulse through the stack. The delay for a single cell is given by Eq. (3.26). Repeat steps 1.-6. iteratively if necessary.

7. Define other dimensions for flanges. These are the inside and outside diameters of the outer wall of the core housing, the minimum insulation gap between the top and bottom flanges of a single cell, the minimum insulation gap between a top flange and the preceding bottom flange of the layer above, the required gap for the PCBs and needed minimum space for grooves for sliding contacts. The insulation gap between adjacent flanges of two layers can be e.g. 2.5-3 mm for up to 1 kV of primary voltage.

3.6 Preliminary Design of the CLIC DR Extraction Kicker Inductive Adder and the Two Experimental Prototypes

In this section, design examples for inductive adders are given following the design guidelines presented in the previous sections. At first the components for the inductive adders are selected and finally the dimensions for the inductive adder cells are defined. Most of the content of this section is based on the previous research and design work for the inductive adders. The purpose of the preliminary designs for the CLIC DR kicker inductive adder and for the two experimental prototypes have been to provide initial electrical parameters for the simulations and modelling studies, which are presented in Chapter 4.

3.6.1 Preliminary Selection of Components for the CLIC DR Inductive Adder and for the Two Prototypes

Semiconductor Switches

The operating voltage of the semiconductor switches defines the maximum operation voltage of the constant voltage layers of an inductive adder. In the preliminary design study, the operation voltage of 700 V per layer was chosen for the CLIC DR kicker inductive adder and for the 3.5 kV prototype inductive adders, because of availability of fast 1 kV and 1.2 kV semiconductor switches. The voltage rating for semiconductor switches for 700 V operation voltage was required to be at least 1 kV, according to the design principle explained in Section 3.4.1. The minimum number of the layers of the adder stack is defined by the required load voltage and the operating voltage of the semiconductor switches. For the given maximum output of 12.5 kV of the CLIC DR kicker inductive adder, the minimum number of 700 V layers is 18. For the 3.5 kV prototype inductive adders, the number of the layers in the prototype adder stack is five. The prototype adders do not include any spare layer for redundancy. MOSFETs were chosen as the most suitable switch technology, because of the required 100 ns rise and fall times for the output pulses.

Capacitor Banks

For the CLIC DR kicker, with 12.5 kV of output voltage and 250 A of output current, 18 layers is assumed with an operating voltage of approximately 700 V per layer. The total current discharged from the capacitor bank in each layer is assumed to be the sum of the load current, the magnetising current and the core loss current of the layer. The magnetising inductance of the magnetic cores cannot be accurately estimated before the dimensions of the inductive adders cells and the core material are known. However, a good practice is to ensure that the magnetising current is significantly less than the load pulse current, e.g. an average of 15 % of the load current. Using this value, 15 %, gives the average of the total primary current to be 287.5 A. The pulse flat-top duration is assumed to be 160 ns. The allowable droop is assumed to be 0.02 %, which is a half of the allowed maximum variation ± 0.02 % of the output pulse. This corresponds to a total droop of 2.5 V in the output waveform, which corresponds to a droop of 0.14 V per each of 18 layers. In this case, the droop is not assumed to be corrected by modulation.

According to Eq. (3.4), the required capacitance to ensure a flat-top droop of no more than 0.14 V per layer, during the 160 ns flat-top, is given as follows:

$$C_s = \frac{I_p t_p}{\Delta V_{pl}} = \frac{287.5 \text{ A} \times 160 \text{ ns}}{0.14 \text{ V}} = 329 \text{ } \mu\text{F} \quad (3.32)$$

The required capacitance per layer is 329 μF . A candidate capacitor could be, for example, a 12 μF pulse capacitor T00216 from NWL [131], which has been developed for pulse power applications. The required capacitance per layer, 329 μF , could be achieved by using 28 capacitors of 12 μF each in parallel per layer, which gives a total capacitance of 336 μF per layer. The 160 ns flat-top duration is required in the 2 GHz option of the CLIC DR extraction kicker system [7] and if the flat-top duration is 900 ns, corresponding to the 1 GHz requirement [7], the amount of capacitance needed per layer would be 1.8 mF.

For the two prototype inductive adders, the nominal load current is 70 A, as is shown in Table 3.1. Estimating 15 % of this for the average magnetising current, the primary current is in total 80.5 A. According to Eq. (3.4), 92 μF of capacitance per layer would be enough to limit the droop to 0.02 % during a 160 ns pulse flat-top. This amount of capacitance would require eight 12 μF capacitors per layer, which gives to a total capacitance per layer of 96 μF . With 900 ns flat-top duration, the required capacitance would be 518 μF per layer. In the computations presented above, the resistive losses of both the semiconductor switches and the current loop of the primary circuit have not been taken into account.

Magnetic Cores

The required cross-sectional size for the magnetic cores of the CLIC DR kicker inductive adder and for the two prototypes can be computed as follows. In Section 3.4.4, Eq. (3.6) is given for computing the ECSA of the magnetic core. The operation voltage of the switches in the primary circuits is assumed to be 700 V. For the effective pulse duration at half-maximum $t_{p,50}$, equal linear rise and fall times of 100 ns are assumed and the worst-case pulse flat-top of 900 ns for CLIC DRs with 1 GHz specifications is applied [7]. The settling time of the output pulse is expected to be 100 ns. The duration of the pulse, $t_{p,50}$, is the sum of pulse flat-top duration, 900 ns, an estimated settling time of 100 ns, and a half of the rise and fall times, 50 ns each, which gives in total 1100 ns. Therefore, a

requirement for each magnetic core is to have enough volt-second integral to supply a $1.1 \mu\text{s}$ long voltage pulse with 700 V.

The preliminary magnetic core material was chosen to be 2605CO from Metglas [111]. With longitudinal field annealing, this material has square-shaped B-H curve [110] and it could provide a maximum flux-density swing of 3.25 T from the negative remanent field to the positive saturation [111]. Therefore, the magnetising inductance could be very high and the cross-sectional size of the core could be relatively small. The cores made of this material have also been designed for use with high magnetisation rates in pulse power applications and therefore they have adequate insulation between the adjacent turns of the metal ribbon [132]. These cores are supplied with custom-made dimensions, therefore the core dimensions can be chosen according to design requirements [111]. In [133], the B-H loop of the material 2605CO is shown. In frequency range from DC up to 1 kHz, the flux density increases linearly as a function of magnetising field across, approximately, 90 % of the flux-density swing. However, it was expected that the usable, linear, flux-density swing of material 2605CO at the pulse bandwidth could be up to two thirds of the maximum flux-density swing, 3.3 T, which gives 2.2 T.

The effective cross-sectional size of the core is computed according to Eq. (3.6) presented in Section 3.4.4. According to Eq. (3.6), the effective cross-sectional area of the solid core, i.e. magnetic area of the core with the given parameters, would be the following:

$$A_{c,\text{eff}} \approx \frac{V_c \times t_{p,50}}{\Delta B} = \frac{700 \text{ V} \times 1.1 \mu\text{s}}{2.2 \text{ T}} = 3.5 \text{ cm}^2. \quad (3.33)$$

Hence, the ECSA of a core should be at least 3.5 cm^2 per layer and including the 100 % margin, the ECSA should be 7 cm^2 per layer. Assuming a packing factor of 65 % for the magnetic core, the actual cross-sectional area of the tape wound core should be at least 10.8 cm^2 .

A drawback of a core material with square-loop B-H curve, e.g. 2605CO from Metglas, is that it cannot be used without a reset and biasing circuit. The remanent magnetic field is close to saturation which means that the permeability of the core is very low after a single pulse, if it is not biased with negative magnetisation. Examples of B-H curves of core materials with a square-loop B-H curve with high remanent field and with a linear B-H curve with low remanent field are shown in Fig. 3.15.

Another core material has been considered for the prototype inductive

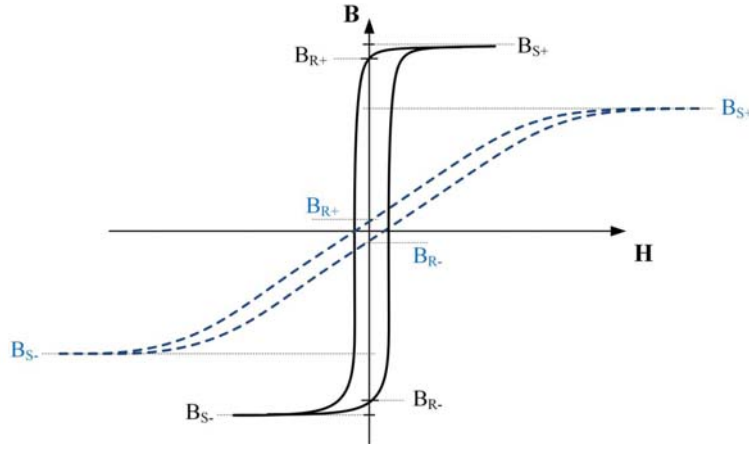


Figure 3.15. Examples of a square-shaped B-H curve (black) and a linear B-H curve (dashed blue).

adders, in order to be able to test the prototype adders without a reset and biasing circuit. As mentioned in Section 3.4, a biasing circuit was not desirable because of the added complexity and possible effects on the flat-top stability and intra-pulse voltage. A core material Vitroperm 500 F from Vacuumschmelze [134] was considered. This material has very linear B-H characteristics. The maximum flux-density swing of this core material is 2 T [114] and it has a very low remanent field, 0.05 T, measured for a 10 Hz sine wave [135]. These cores are available only as off-the-shelf products, and therefore the cross-sectional dimensions could not be freely chosen. However, an advantage of these cores for experimental prototypes was the very short delivery time, a few days, in comparison with custom-made cores, which may take months to receive. A model W567 [136] was chosen as a candidate core for the two prototype inductive adders. The effective cross-sectional area of these cores is 2.85 cm^2 and the usable, linear, flux-density swing of these cores was estimated to be 0.9 T without biasing. With these values, the maximum pulse flat-top duration would be theoretically restricted to 266 ns with 700 V per layer, allowing in total 100 ns of rise and fall times. This pulse duration would be the maximum and it would not include any margin. However, with a lower voltage, e.g. 500 V per layer, the maximum pulse flat-top duration would be 413 ns. Another drawback of using Vacuumschmelze cores is that the insulation between ribbon turns cannot be customised, and that the typical inter-laminar voltage withstand is 0.3 V per insulation layer [137]. The ribbon thickness of Vacuumschmelze cores is $20 \text{ }\mu\text{m}$ and the packing factor is typically 75 % [137]. The average voltage stress during a pulse for a single insulation layer can be estimated with Eq. (3.5) [113] as follows:

$$V_{cl} = l_c h_r \frac{\Delta B}{\Delta t} = \frac{2.85 \times 10^{-2} \text{ m} \times 20 \times 10^{-6} \text{ m} \times 0.9 \text{ T}}{366 \times 10^{-9} \text{ s}} = 1.4 \text{ V}. \quad (3.34)$$

According to Eq. (3.34), the voltage stress per insulation layer is 1.4 V, which is 4.7 times larger than the typical withstand of the insulation layer, 0.3 V. In fault conditions, the voltage stress could be even higher. Therefore, there may be insulation breakdowns in the core insulation in the long run, which increases eddy currents and degrades the magnetic characteristics of the core.

The magnetising inductances of the candidate cores have been estimated for modelling and simulation studies. The 100 ns rise time corresponds to approximately 3.5 MHz bandwidth for the output pulse. For Vacuum-schmelze W567 core, the inductance for a single turn is specified to be 50 μH at 10 kHz and 19.4 μH at 100 kHz, with tolerances of +45 % and –25 %, respectively, for the inductance values [138]. The average relative permeability of the magnetic material of the W567 core is 50,000 at 10 kHz [136]. By substituting this relative permeability and the dimensions of the W567 core into Eq. (3.22) gives 50 μH at 10 kHz. Taking into consideration the pulse frequency content, the effective magnetising inductance was expected to be significantly lower than 19.4 μH during the rise time. Fig. 3.16 shows the relative permeability of samples of Vitroperm 500 F material as a function of frequency [137]. The samples have relative permeability at low frequency from 4,000 to 100,000 and the permeability is shown in the frequency range from 1 Hz to 6 MHz.

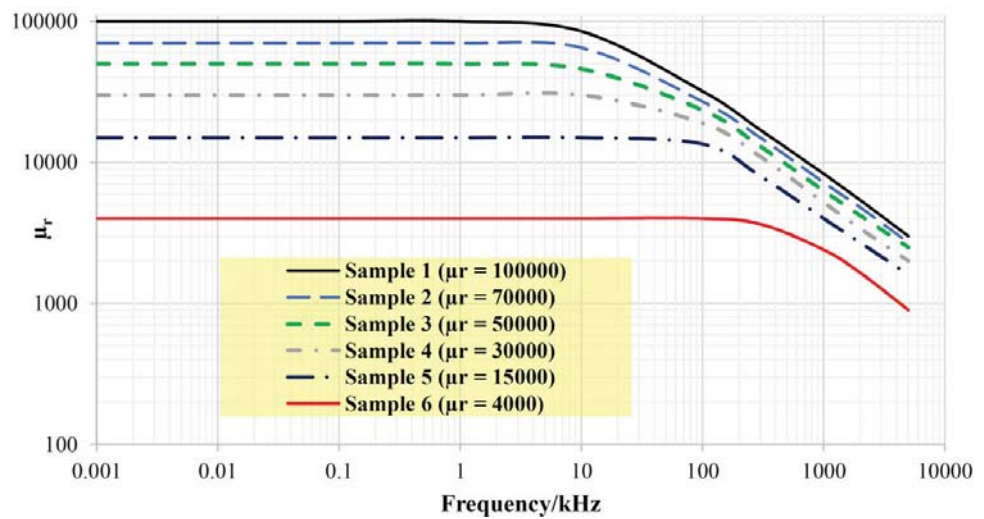


Figure 3.16. Relative permeability of Vitroperm 500 F as function of frequency. Revised after [137].

As the first estimate for the magnetising inductance of a core during a pulse, the effective permeability of the core material was estimated to be the permeability at 500 kHz, which corresponds to a $2 \mu\text{s}$ fundamental period of the pulse waveform. In Fig. 3.16, the relative permeability at 500 kHz for a material which has low frequency permeability of 50,000 is approximately 10,000. Applying Eq. (3.22) and dimensions of Vacuumschmelze W567 core, the first estimate for a magnetising inductance for the prototype inductive adders during the pulse is $10 \mu\text{H}$ per layer. The core losses can be estimated by applying Eq. (3.15). For Vacuumschmelze W567 core, which is made of Vitroperm 500 F material, the ribbon thickness is typically $20 \mu\text{m}$ and the resistivity of the ribbon $115 \mu\Omega \text{ cm}$ [114]. The estimated loss resistance R_c is 27.5Ω . These two parameters have been used as starting points for the simulations of the operation of an inductive adder in the following sections. The magnetising inductance of magnetic cores for the CLIC DR kicker inductive adders required a few assumptions concerning the Metglas 2605CO cores because these cores are supplied with custom-made dimensions. The height of the core is 30 mm, the outside diameter is defined to be 160 mm and the inside diameter 90 mm. The packing factor was expected to be 70 % and the relative permeability 10,000. With these parameters, Eq. (3.23) gives $24.2 \mu\text{H}$ for the magnetising inductance. For Metglas 2605CO, the resistivity of the material is $123 \mu\Omega \text{ cm}$ [111], the thickness of the ribbon has been estimated to be $25 \mu\text{m}$, and the estimated loss resistance is 37.1Ω .

3.6.2 Preliminary Design of the Adder Cells for the CLIC DR Inductive Adder and for the Two Prototypes

The goals of the preliminary design of an inductive adder cell for the CLIC DR kicker inductive adder and for the prototype adders is to fulfil the requirements for the output impedance and for the insulation between the stalk and the primary winding. Good impedance matching keeps settling time short and reduces the minimum overall duration of the pulse flat-top. Dimensioning of an inductive adder cell is an iterative process which requires a few assumptions. The impedance and insulation requirements are relatively easy to meet, but repetitions of the preliminary design steps may be needed if other parameters, e.g. minimising delay, size and cost, need to be taken into consideration. The design steps for the inductive adder cells, as described in 3.5.4 are explained in detail for the CLIC DR kicker inductive adder and for the two prototype inductive adders in the

following paragraphs.

1. The first step is to choose the initial insulation material for the gap between the stalk and the primary winding. This choice defines the permittivity ϵ_i and the maximum applicable electric field of the insulation material. According to [68], air insulation is generally suitable for inductive adders up to 20 kV output voltage. The advantages of air insulation are easy assembly and modifications, and no risk of ageing of the insulation material. Any solid insulation, for example epoxy or polyethylene, could be difficult to modify later, if necessary. Also, solid insulators should be attached very carefully to the metal parts, preferably in vacuum, in order to avoid air bubbles to be captured between the insulator and the conducting metal parts, because air bubbles could cause the insulator to deteriorate as result of partial discharge in the long run. Use of liquid insulation, e.g. silicone fluid, would require a more complex design, it would be prone to leakage and maintenance is more difficult. An insulation with a gas or a vacuum also has the same drawbacks, risk of leakage and more complex design than air insulation. However, a drawback of the air insulation is a relatively low dielectric strength, which means that the gap between the stalk and the primary winding needs to be relatively large in comparison with other insulation materials and the outside diameter of the stalk is increased to reduce electric field here, according to Eq. (3.29). With air insulation, the relative permittivity ϵ_r and the relative permeability μ_r of the insulation material are 1, and a conservative value for the maximum design electric field between the stalk and the inner wall of the primary winding is 0.7 kV/mm.

2. The second step is to estimate the primary loop inductance L_{pl} . It is the only parameter in the equation for the output impedance of the inductive adder, Eq. (3.28), which cannot be computed easily analytically. The primary loop inductance consists of a parallel connection of several current branches, therefore it is expected to be low, a few nanohenries. In the preliminary design presented here, the loop inductance L_{pl} is estimated with simple inductance calculations of individual circuit parts. An approach to predict the primary loop inductance using a 3D simulation code is shown in Chapter 4.

The primary circuit is expected to consist of four different sections and

Table 3.2 shows the dimensions and estimated inductances for each of the four sections. The inductance L_s of each section is estimated with the following equation:

$$L_s = \frac{\mu_0 \mu_r l_s h_s}{w_s} \quad (3.35)$$

In applying Eq. (3.35), each section is assumed to consist of two vertically parallel conductor, the lengths of which are l_s , the widths w_s and the distance between the conductors is h_s . The μ_r is relative permeability of the material between the conductors, which is assumed to be 1 for all sections. μ_0 is the permeability of free space. The thickness of the conductors have not been taken into consideration as for the relatively high frequency content of the pulse, due to proximity effect, the current will flow on the inner surfaces of the conductors.

The first section is a pulse capacitor, which is assumed to be NWL T00216 [131]. The width and the length of the capacitor are the outside dimensions of the capacitor and the inductance of the capacitor is expected to be the inductance of a current loop whose distance between conductors is a half of the height of the capacitor. The second section includes a semiconductor switch with a TO-264 package and a PCB trace from the switch to the vias, which connect the track of the top surface of a PCB to the bottom side. The width of this section is estimated to be approximately the width of the TO-264 package, 20 mm. The distance between conductors of this section is estimated to be 1 mm more than the thickness of a PCB, which gives 5 mm, and the estimated length of the section is 45 mm. The third section is a wide PCB trace from the pulse capacitor to a top flange. This sections is chosen to be 50 mm wide, 50 mm long and with 4 mm between conductors. The fourth section is the current loop along the flanges. The loop is estimated to be 80 mm wide, 35 mm high and 35 mm long. The cross-sectional area of a magnetic core, which is between a top flange and a bottom flange, is estimated to be, as maximum, 35 mm times 35 mm. The last row in Table 3.2 is the sum of the inductances of the four sections, 66 nH, which is the estimated primary loop inductance of a single current branch. A good margin, e.g. 50 %, is advisable, in order to have a reasonable error margin. Therefore, the estimate for the maximum loop inductance is chosen to be 96 nH. Hence, the total inductance of a primary circuit consisting of e.g. eight parallel branches is 12 nH. This is considered

to be the maximum primary loop inductance. Mutual inductance between parallel branches is neglected as the separation of conductors in a section is generally relatively small compared to the distance between parallel branches. The estimate for L_{pl} is supposed to be higher than the total primary loop inductance of a real prototype, which will lead to larger stalk diameter d than is necessary to get 50Ω output impedance.

Table 3.2. Dimensions of the sections of the primary loop of an inductive adder cell.

Section	h_s (mm)	l_s (mm)	w_s (mm)	L_s (nH)
1. Pulse capacitor	20	45	40	28.3
2. Switch - vias	5	45	20	14.1
3. Capacitor - top flange	4	50	50	5
4. Loop around flanges	35	35	80	19.2
Total	n/a	n/a	n/a	66.6

3. The initial minimum length of a single cell of the inductive adder is defined. The minimum length of a cell is defined by either the height of the components of the primary layers, e.g. pulse capacitors, or the height of the magnetic cores. In this initial design, the limiting (minimum) height is expected to be the pulse capacitor. The height of a candidate pulse capacitor is 32 mm [131]. In addition, the thickness of the PCB is estimated to be four millimetres and nine millimetres are reserved for an air gap between the components on a PCB and the neighbouring layer of the stack. The nine millimetre gap between the components on a PCB and the preceding PCB also includes components which may be mounted on the bottom side of the PCB above. Thus, the minimum length of a cell, l_p , is estimated to be 45 mm. This limits the maximum height of the magnetic core to be approximately 35 mm, to reserve a few millimetres for the primary winding above and below the core, and a few millimetres for an air gap between the winding and the preceding magnetic core in the stack.

4. The minimum diameter of the stalk, d , and the minimum diameter of the inside diameter of the inner wall of the primary winding, D_1 are defined. By substituting Eq. (3.16) and Eq. (3.17) to Eq. (3.28) gives the following equation:

$$Z_{\text{out}} = \sqrt{\frac{L_{\text{pl}} + \frac{\mu_0 l_p}{2\pi} \ln \frac{D_1}{d}}{\frac{2\pi \epsilon_i l_p}{\ln \frac{D_1}{d}}}} \quad (3.36)$$

For Eq. (3.36), all other parameters except D_1 and d have been defined above and the ratio of D_1 to d is fixed for the required output impedance Z_{out} . For the defined set of parameters, Z_{out} is equal to 50Ω , ϵ_i equals to permittivity of free space, l_p equal to 45 mm and L_{pl} equal to 12 nH, the ratio of D_1 to d is 1.49. The absolute minimum values of D_1 and d depends on the maximum applicable electric field between the stalk and the inside wall of the primary winding.

Figure 3.17 shows the maximum electric field between the stalk and the core housing for an air-insulated inductive adder for 3.5 kV (black, dashed) and 12.5 kV output voltage (solid blue). The curves are plotted according to Eq. (3.29). According to the black, dashed, curve in Fig. 3.17, the minimum stalk diameter d for a 3.5 kV inductive adder, with air insulation and with 45 mm of the length of a cell, is approximately 18 mm, to have a maximum electric field of 0.7 kV/mm between the stalk and the core housing. For a 12.5 kV inductive adder the minimum stalk diameter is 90 mm. However, if the insulation material, the length of the stalk or the other parameters are changed, the minimum outside diameter of the stalk and its ratio to the inside diameter of the inner wall of the primary winding are changed.

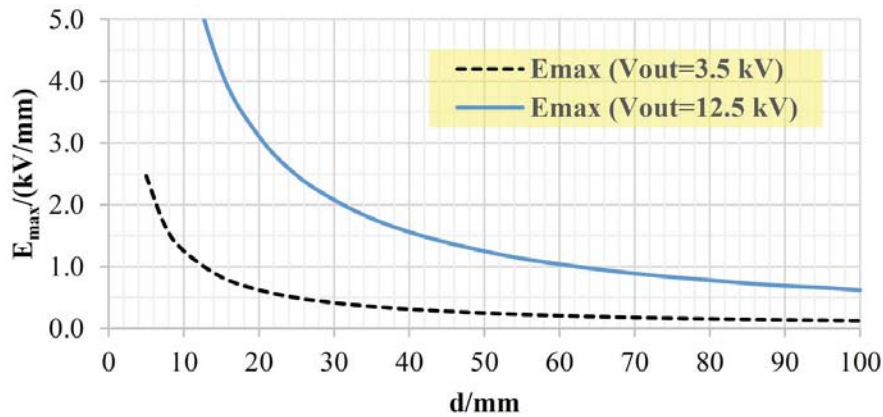


Figure 3.17. Maximum electric field E_{max} as a function of stalk diameter d for 3.5 kV (dash black) and 12.5 kV (blue) output voltage. Ratio D_1/d is equal to 1.49 and corresponds to a 50Ω output impedance.

For the two prototype inductive adders, the dimension of the stalk was chosen to be such that the same dimensions of the flanges could be used for the 3.5 kV prototypes and for the 12.5 kV CLIC DR kicker inductive

adder. An initial idea was to choose dimension D_1 such that the same cells could be used for the 3.5 kV prototypes with air insulation and for the 12.5 kV CLIC DR kicker inductive adder with a solid insulation, which has a higher relative permeability than air. This choice requires that the parameters d and D_1 are chosen to be larger than the minimum required dimensions for the 3.5 kV output voltage with air insulation. For this reason, the stalk diameter d has been chosen to be 44 mm. With air insulation, this gives 66 mm for the inside diameter of the inner wall of the primary winding, D_1 . For the 12.5 kV adder with a given D_1 equal to 66 mm, stalk diameter d will be chosen to give the appropriate output impedance, e.g. for epoxy.

Figure 3.18 shows the diameter of the inside wall of the primary winding as function of the outside diameter of the stalk, d , with three different output impedances, Z_{out} equals to 35, 50 and 65 Ω , with air insulation. These curves have been plotted by solving D_1 from Eq. (3.36) as a function of d . For simplicity, this has been done in two steps, the first of which is shown below:

$$\ln \frac{D_1}{d} = \frac{-L_{\text{pl}} \pm \sqrt{L_{\text{pl}}^2 + 4\mu_0\epsilon_i l_p^2 Z_{\text{out}}^2}}{\frac{2\mu_0 l_p}{\pi}} \quad (3.37)$$

By substituting the parameters, L_{pl} is equal to 12 nH, l_p equal to 45 mm, permittivity of insulation and permeability of free space, and the output impedance Z_{out} into Eq. (3.37), the logarithm in the left side of can be solved by choosing the positive value given by the right side of the equation and applying the natural exponential function for the both sides. In Fig. 3.18, the straight lines are shown for output impedances of 35 Ω , 50 Ω and 65 Ω , which correspond to ratios of D_1/d of 1.25, 1.49 and 1.83, respectively. In Fig. 3.18, there are also three contour plots which show the maximum electric field between the stalk and the core housing, E_{max} , with 0.4, 0.7 and 1.0 kV/mm. These have been plotted by solving D_1 from Eq. (3.29) as follows:

$$D_1 = e^{\left(\frac{2V_{\text{out}}}{E_{\text{max}}d}\right)} \quad (3.38)$$

Fig. 3.18 is plotted by assuming the output voltage of 3.5 kV. The chosen design parameters for the prototype inductive adders are 44 mm for d and 66 mm for D_1 . The corresponding output impedance, 50 Ω , and

maximum electric field, 0.4 kV, are shown in Fig. 3.18 with red arrows.

Figure 3.19 shows the diameter of the inside wall of the primary winding as a function of the outside diameter of the stalk, d , with three different output impedances, Z_{out} equals to 35, 50 and 65 Ω , for an epoxy-insulated inductive adder. The relative permittivity of the epoxy insulation is assumed to be 4.8. The straight lines in Fig. 3.19 correspond to ratios of D_1/d of 2.17, 3.58 and 6.06, respectively. In Fig. 3.19, three contour plots show the maximum electric field between the stalk and the core housing, E_{max} , with values of 0.7, 1.1 and 2.5 kV/mm. The preliminary design parameters for the CLIC DR kicker inductive adder are 18 mm for d and 66 mm for D_1 and the corresponding output impedance, 50 Ω , and maximum electric field, 1.1 kV, are shown in Fig. 3.19 with red arrows.

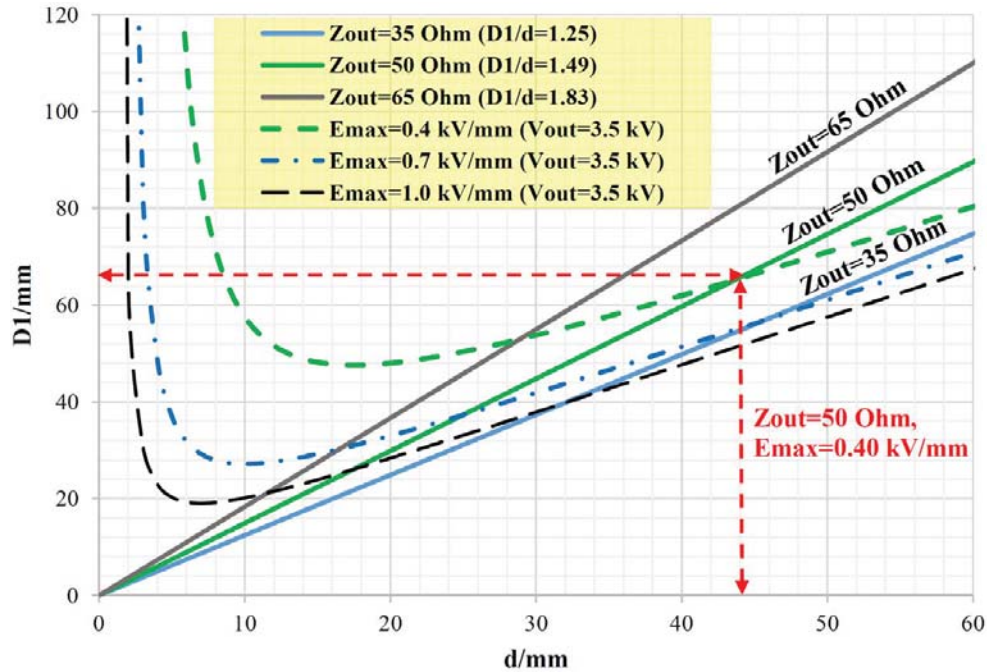


Figure 3.18. The inside diameter of the core housing, D_1 , of an air-insulated inductive adder ($\epsilon_r=1.0$) as a function of the outside diameter of the stalk, d , with the output impedance Z_{out} of 35, 50 and 65 Ω , with V_{out} of 3.5 kV and with E_{max} of 0.4, 0.7 and 1.0 kV/mm.

5. Define the initial height and the minimum inside and outside diameters of the magnetic core. The primary winding encloses the magnetic core completely and the inner wall of the winding, which consists of the top and bottom flanges, is located between the magnetic core and the insulation of the secondary winding. The primary winding serves as the mechanical structure of the inductive adder and therefore the inner

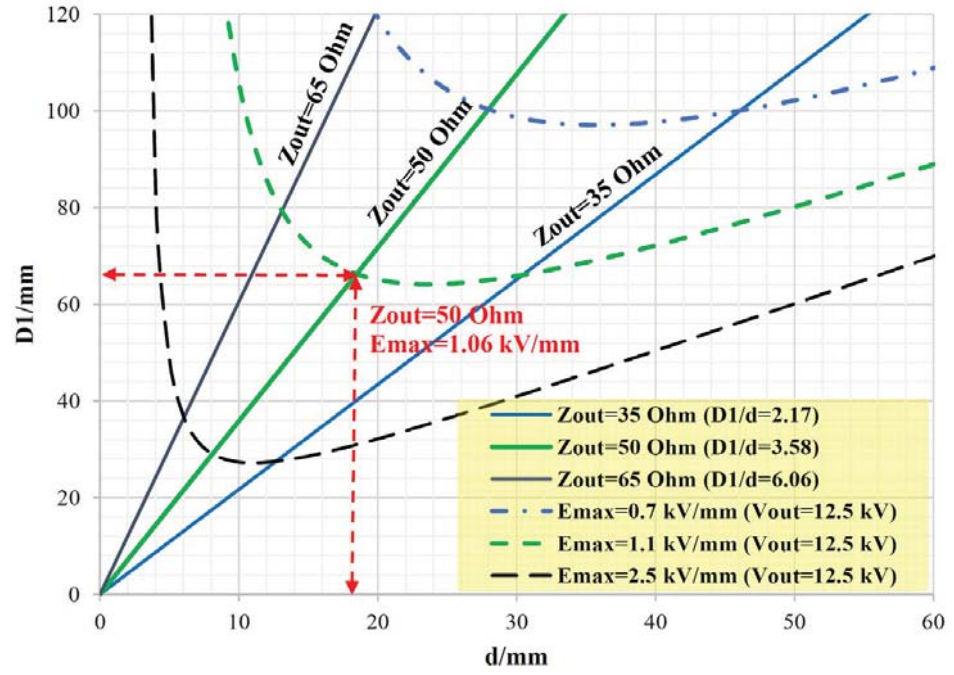


Figure 3.19. The inside diameter of the core housing, D_1 , of an epoxy-insulated inductive adder ($\epsilon_r=4.8$) as a function of the outside diameter of the stalk, d , with the output impedance Z_{out} of 35, 50 and 65 Ω , with V_{out} of 12.5 kV and with E_{max} of 0.7, 1.1 and 2.5 kV/mm.

wall of the primary winding should be relatively thick, for example 10-15 mm. In addition to this, many tape-wound cores are wrapped around a non-magnetic mandrel, the thickness of which is typically 2-5 mm. Therefore, the inside diameter of the core, D_2 should be at least 24 mm larger than the inside diameter of the inner wall of the primary winding, D_1 . According to the previous design step, D_1 is 66 mm, which requires D_2 to be at least 90 mm.

The outside diameter of the core can be computed with the following equation:

$$D_3 = D_2 + 2 \frac{A_c}{l_c} \quad (3.39)$$

In Eq. (3.39), A_c is the cross-sectional size of the core and l_c is the height of the core. In order to avoid saturation of the inside diameter of the core in normal operating conditions, the outside diameter of the core, D_3 , should be as maximum two times larger than the inside diameter of the core, D_2 . The reasoning for this requirement is explained in detail in Section 3.4.4. In the same Section, 3.4.4, the cross-sectional areas of the magnetic core are given for the CLIC DR kicker inductive adder and

for the prototype inductive adders. The cross-sectional area of the core, made of material 2605CO, should be at least 10.8 cm^2 . A candidate core for the prototype adders, Vacuumschmelze W567, has a cross-sectional area of 5.63 cm^2 . For a Metglas 2605CO core, D_2 is expected to be 90 mm and l_c 35 mm, and according to Eq. (3.39) D_3 should be at least 152 mm. A few more millimetres for D_3 could be reserved for insulation of the core, because custom-made tape-wound cores are often supplied without casing and they need to be insulated, for example with an insulating tape, before placing them inside the conductive flanges. Therefore, the inside diameter of the outer wall of the flange is set to 160 mm. The candidate core for the prototype inductive adders, Vacuumschmelze W567 has inside diameter is 95 mm, the outside diameter 134.5 mm and the height 28.5 mm, and it fits to the defined flange dimensions.

6. Check that the design requirements are met. Repeat steps 1.-6. iteratively if necessary. Table 3.3 shows the preliminary design parameters for the cell of the CLIC DR kicker inductive adder and for the two prototype inductive adders. The dimensions of the cell are the same for both designs, except that the stalk diameter d is 44.2 mm for an air-insulated cell and 18.4 mm for an epoxy-insulated cell, to achieve 50Ω output impedance. The insulation thickness between the primary winding and the secondary winding, D_{ins} , is computed with the following equation:

$$D_{\text{ins}} = \frac{(D_1 - d)}{2} \quad (3.40)$$

For the air-insulated cell of the prototype inductive adders, the insulation thickness D_{ins} is 10.9 mm and the maximum electric field E_{max} is 0.4 kV/mm. With 12.5 kV output voltage, the maximum electric field of this cell design would be 1.4 kV/mm, which is less conservative for air insulation and could lead to sparking between the stalk and the primary winding. For the epoxy-insulated cell for the CLIC DR kicker inductive adder, the thickness of the epoxy insulation is 23.8 mm and the maximum electric field is 1.06 kV/mm. This is acceptable for epoxy and the design could be used with considerably higher output voltages, above 20 kV. A disadvantage of the solid insulation is that it is not easy to trim the output impedance by changing the diameter of the secondary winding.

According to Table 3.3, the preliminary designs of the cells meet the

Table 3.3. Preliminary design parameters for cells for the prototype inductive adders and for the CLIC DR extraction kicker inductive adder.

Parameter	Prototype inductive adders	CLIC DR extraction kicker inductive adder
insulation material	air	epoxy
V_{out} (kV)	3.5	12.5
Z_{out} (Ω)	50.0	50.0
ϵ_r	1.0	4.8
A_c (cm^2)	5.63	10.8
$A_{c,\text{eff}}$ (cm^2)	2.85	7.0
C_c (pF)	6.2	9.4
l_c (mm)	28.5	35
l_p (mm)	45	45
d (mm)	44.2	18.4
D_1 (mm)	66	66
D_2 (mm)	90	90
D_3 (mm)	160	160
D_{ins} (mm)	10.9	23.8
E_{max} (kV/mm)	0.40	1.06
L_m (μH)	10	24.2
L_{pl} (nH)	12	12
L_{ss} (nH)	3.6	11.5
R_c (Ω)	27.5	37.1
$T_{\text{rd},1w}$ (ns)	0.31	0.47

requirements. However, if the cell designs are to be optimised, e.g. concerning the volume of the core or other parameter, the steps 1.-6. should be repeated. The coupling capacitance C_c and the secondary inductance L_{ss} are usually desired to be as low as possible, because both of these parameters affect the bandwidth and delay through the inductive adder and therefore the pulse rise and field settling times. The insulation material, the length of each cell and the diameter of the secondary stalk, could be changed to modify the electrical characteristics of the cell. In Table 3.3, the minimum single-way propagation delay of the pulse through a single cell, $T_{\text{rd},1w}$, is shown. The delay for a single cell is given by Eq. (3.26). For an air-insulated cell of the prototype inductive

adders, the delay is 0.31 ns, and for an epoxy-insulated cell of the CLIC DR kicker inductive adder, the delay is 0.47 ns.

7. Define other dimensions for flanges. In cell designs presented in Table 3.3, the outside diameter of the magnetic cores, D_3 , is defined to be 160 mm. This is the minimum inside diameter of the outer wall of the primary circuit. Approximately 20 mm is needed for holes for spacers, which connects the bottom flanges together through top flanges. Another 20 mm is needed for sliding contacts, which connect the PCB of the primary circuit to the bottom and top flanges. Therefore, the outside diameter of the flanges would be at least 240 mm. If the primary circuit is a PCB the contact surfaces of which are circularly shaped, the minimum inside diameter of the inside edge of the PCB is 200 mm.

The voltage of a single layer in both design examples is 700 V. The electric field between the flanges should be in normal operating conditions less than 0.4 kV/mm. This requirement is met if the minimum air gap between the top and bottom flanges on the primary circuit side is at least 2 mm and the edges of the flanges are rounded appropriately to avoid sharp edges. The thickness of the PCBs of the primary circuits was estimated to be 4 mm. With a 0.2 mm clearances per side, the distance between the top and bottom flanges on a PCB slot should be at least 4.4 mm.

In this preliminary design iteration, parameter L_{pl} is estimated with a significant margin, 50 %, which leads to larger stalk diameter d than needed. If the primary loop inductance can be estimated with a good precision, the stalk diameter d and the inside diameter of the inner wall of the primary winding, D_1 , are known well. In this case, an iterative trimming of the stalk diameter is not needed and the dimensions of the cell can be chosen to give the required output impedance. Therefore, an accurate estimate for L_{pl} is useful and a method to predict it by using a 3D code is shown in Section 4.4.

4. Modelling and Simulation Studies

This chapter includes simulation and modelling studies which were completed in order to design the inductive adder, the output waveform of which meets the requirements of the CLIC DR kicker inductive adder. The main goals of the simulation studies presented in this chapter were the following:

1. To verify the main parameters, i.e. the values of the main components, and to learn how different design parameters affect the output waveform of an inductive adder. Simulation studies were completed of the normal operation and typical fault conditions of an inductive adder, and these studies are presented in Sections 4.1 and 4.2 of this chapter. These studies were completed with PSpice simulation software [139].
2. To study the contributors to the ripple and droop of an inductive adder, in order to improve the flat-top stability of the output waveform of an inductive adder beyond the level which had been reached with previous designs, e.g. with the inductive adders listed in Table 2.4. Simulations were carried out to understand the most important contributors to the stability of the pulse flat-top, which are set by the inductive adder and by the other parts of a stripline kicker system.
3. To design an inductive adder with a desired output impedance. The aim of this study was to develop a new design method for the adder stack, with which the laborious and time-consuming iteration steps for tuning the output impedance of the stack could be avoided. The primary loop inductance is the only design parameter of an inductive adder stack which cannot be easily estimated with analytical equations, as has been explained in Section 3.5.2. Especially, the primary loop induc-

tance of a single layer of an inductive adder has been predicted with a three-dimensional model of the primary circuit using a FastHenry simulation code [140]. The prediction, given by the simulation, were compared to the measured primary loop inductance of a prototype inductive adder, in order to evaluate the precision of the simulations. The effect of the primary loop inductance on the output waveform was studied with PSpice [139].

4. To study whether the passive and active analogue modulation methods can be used to adequately compensate the droop and ripple of the output pulses of the inductive adder. The passive and active analogue modulation were found to be feasible methods to compensate the droop and ripple of the output waveform with the required precision. These studies were carried out with the PSpice simulation package [139]. The results of these simulations studies have also been experimentally verified with the prototype inductive adders and the result of the measurements are presented in Chapter 5.
5. To build accurate simulation models, which could be used to model the operation of the prototype inductive adders and the full-size 12.5 kV inductive adders for the CLIC DR kicker systems. This goal was defined so as to be able to study in detail use of modulation methods to improve the flat-top stability of an inductive adder. It was also assumed, that this technique could be demonstrated with a small scale prototype, which could have been less expensive and less time-consuming to build and test than a full-scale prototype. A point to note is that the prototype inductive adders, presented in detail in Chapter 5, were the first inductive adders built at CERN. Therefore, one purpose of building these prototypes inductive adders was to verify the simulation studies presented in this chapter.

All five goals of these studies were set by the main objective of this dissertation, which was to find a suitable topology for a high-precision pulse modulator, and to improve its performance in order to achieve the flat-top stability required for the CLIC DR kicker system. The simulation models were verified by comparing the measured output waveforms to the predicted waveforms of the prototype inductive adders. Then, the verified simulation models were applied to complete a design proposal for a

12.5 kV inductive adder, with the nominal output voltage, current capability and flat-top stability which are required for the CLIC DR kicker inductive adder. This design proposal and the comparisons of simulated and measured waveforms of the prototype inductive adders, are presented in Chapter 5.

4.1 Simulations of an Inductive Adder in Normal Operation

In this section, the simulation studies are presented of an inductive adder, which is operating normally, i.e. without faults or considerable differences in turn-on or turn-off times of parallel semiconductor switches or individual layers of the adder stack. In Section 4.1.1, the simulation models are presented along with the parameters for the models. In Section 4.1.2, the voltage and current waveforms are shown for an inductive adder, which is operating normally, and the operation is explained in detail.

4.1.1 Simulation Models and Parameters for Normal Operation

Figure 4.1 shows the PSpice schematic of a single layer of an inductive adder. The model is based on the equivalent circuit of a single layer, shown in Fig. 3.12. The parameters for the simulation model are shown in Table 4.1 and they are based on the preliminary design of the 5-layer prototype adders, presented in Table 3.3. Fig. 4.2 shows a simulation model of a single layer in which each primary circuit consists of eight parallel current branches. Each current branch includes a semiconductor switch, a pulse capacitor, parasitic primary loop resistance and parasitic primary loop inductance. In the first section of Table 4.1, the parameters are given for the secondary circuit and for the magnetic cores. In the second section of the table, the parameters are given for a model, in which the primary of each layer of an inductive adder is modelled as a single current branch. In the last section of the table, the parameters are given for the model, in which the primary circuit of a layer is modelled with eight identical branches in parallel.

The resistive losses in the primary circuit, R_p , and in the secondary circuit, R_s , can be estimated with the following equation:

$$R = \frac{\rho_s l_s}{A_s} \quad (4.1)$$

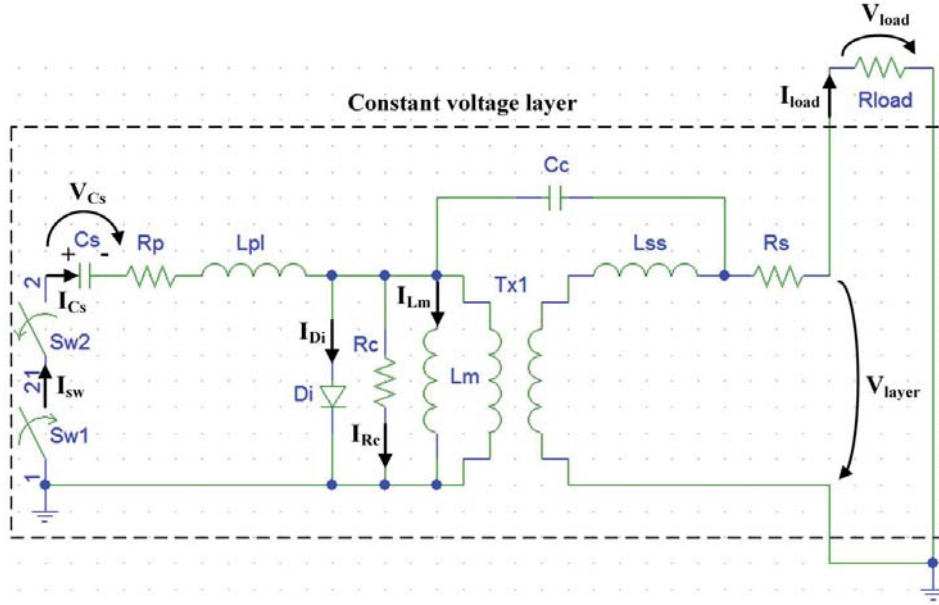


Figure 4.1. The PSpice schematic of an equivalent circuit of a constant voltage layer of an inductive adder with a load. The arrows for currents show the direction of positive current flow. The arrows for voltages show the positive polarity in the case when the arrows point from the positive voltage to the negative voltage.

In Eq. (4.1), R is the resistance of a conductor, the length of which is l_s , cross-sectional area A_s and resistivity ρ . In computing R_s , the conductor is a section of the stalk, the length of which corresponds to the length of a single layer, 45 mm, as given for l_c in Table 3.3. The stalk is expected to be solid aluminium, the resistivity of which is $26.7 \mu\Omega \cdot \text{m}$ [141]. For the primary resistance R_p , the dimensions of the sections of the primary loop is assumed to be the same which has been used in estimating the loop inductance of the primary circuit, given in Table 3.2 in Section 3.6.2. The thickness of the PCB traces has been estimated to be $35 \mu\text{m}$ and the material of the traces is assumed to be copper, the conductivity of which is $16.9 \mu\Omega \cdot \text{m}$ [141]. The material of the flanges of the core housing is expected to be aluminium. The estimated resistance of a single current branch of an inductive adder with the dimensions given in Table 3.3 is $3.4 \text{ m}\Omega$. However, the resistance of a pulse capacitor has not taken into account in this number. The first estimates for conductive losses $R_{p,1br}$ and R_s , given by Eq. (4.1), have been rounded upwards to the values shown in Table 4.1, $50 \text{ m}\Omega$ and $0.1 \text{ m}\Omega$, respectively. Skin effect has not been taken into consideration in computing these values. The on-state resistance of the semiconductor switches is not included in primary loop resistance R_p . The on-state resistance of a single switch, $R_{sw,1br}$, has been

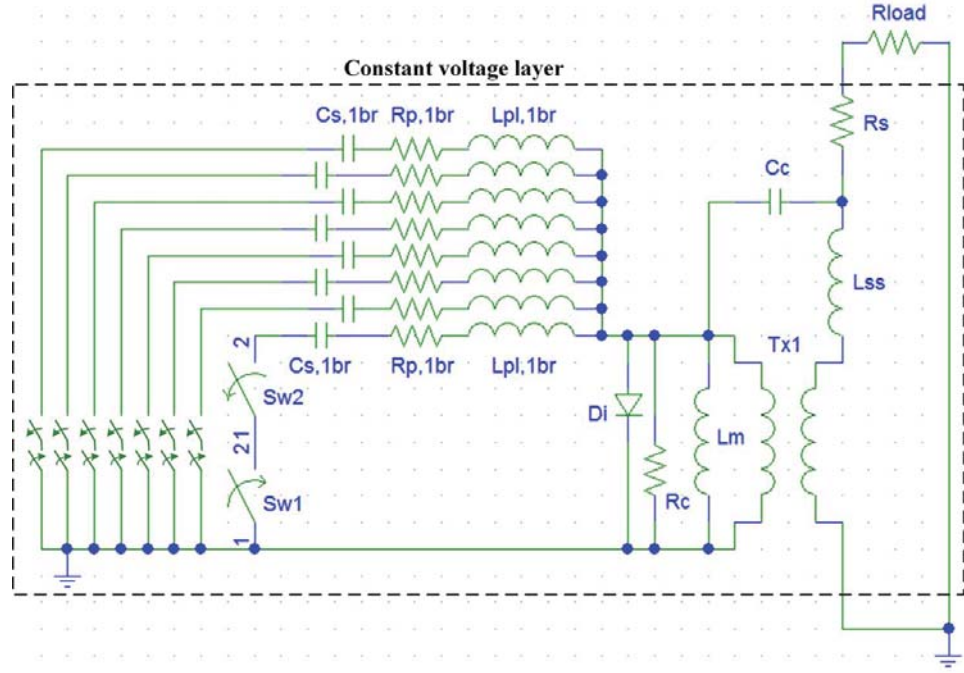


Figure 4.2. The PSPice schematic of a constant voltage layer with eight parallel branches with a load.

chosen to be 0.67Ω , which is a typical value for a fast 1.2 kV MOSFET switch, type APT12067LFLL [101]. R_{sw} is the effective on-state resistance of the parallel switches of a single layer.

4.1.2 Voltage and Current Waveforms of an Inductive Adder in Normal Operation

Figure 4.3 shows simulated output voltage V_{load} of a 5-layer inductive adder. It also shows voltage V_{layer} , L1-L5, which corresponds to the voltage, which a single primary layer induces to the secondary. Voltage V_{layer} , L1-L5 can be considered as the net output voltage of each primary circuit of the inductive adder, i.e. the voltage which is induced on the secondary winding of a single layer. In this simulation study, the model consisted of five identical layers, each of which was similar to the PSPice model shown in Fig. 4.1. Therefore, in this simulation, the net voltage of each primary circuit was the same, V_{layer} , L1-L5, shown in Fig. 4.3. Each layer of the simulation model consisted of a single branch, and the parameters for a single layer from Table 4.1 were applied. The on-state resistance of semiconductor switches, R_{sw} , is not shown in Fig. 4.1. Parameter R_{sw} is the effective on-state resistance of the parallel switches of a layer and it is modelled as the on-state resistance of switch S1 of the primary loop in each layer of the model. The pulse capacitors of each constant voltage

Table 4.1. Parameters for a single layer and for a single branch for simulation models based on the preliminary design of a 5-layer prototype inductive adders.

Parameters for the secondary and for the magnetic core	Value
C_c (pF)	6.2
L_m (μ H)	10
L_{ss} (nH)	3.6
N_{layers}	5
R_c (Ω)	27.5
R_s (m Ω)	0.1
R_{load} (Ω)	50.0
Parameters for a single layer (8 branches per layer)	
C_s (μ F)	96
L_{pl} (nH)	12
R_p (m Ω)	6.3
R_{sw} (m Ω)	84
Parameters for a single branch	
$C_{s,1br}$ (μ F)	12
$L_{pl,1br}$ (nH)	96
$R_{p,1br}$ (m Ω)	50
$R_{sw,1br}$ (Ω)	0.67

layer were initially charged to 700 V. The maximum net flat-top voltage of each primary layer is 690.4 V and the maximum flat-top load voltage V_{load} is 3.452 kV and these voltages have negative polarity. Therefore, the flat-top output voltage of an inductive adder is the net flat-top voltage of the primaries times the number of the primaries, as shown in Eq. (3.1) in Section 3.2.1. In Fig. 4.3, the droop of the load voltage, V_{load} , is approximately 35.6 V for 950 ns flat-top duration and 6.0 V (0.17 %) for 160 ns flat-top duration. After the end of the pulse, at time point 1.55 μ s, the free-wheeling diodes, shown as D_i in Fig. 4.1, start conducting and the load voltage V_{load} is reverse-biased to 10 V. Neglecting the very small resistive losses in the secondary, this voltage corresponds to 2 V of forward voltage across the diode D_i in each layer.

Figure 4.4 shows the currents of a few main components of a single layer of an inductive adder for the same simulation as the voltages are shown in Fig. 4.3. The currents are shown for the load, I_{load} , the loss resistance

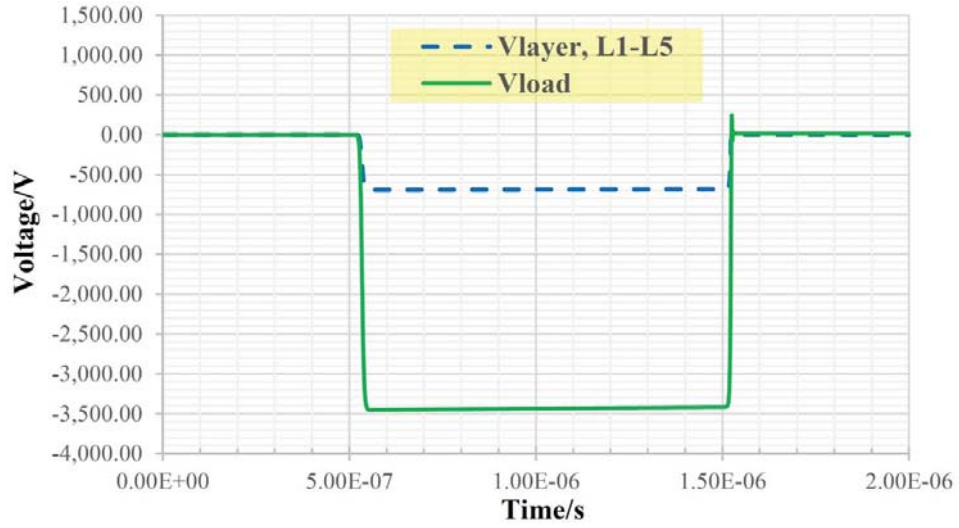


Figure 4.3. Simulated V_{load} and $V_{layer, L1-L5}$ of an inductive adder with five constant voltage layers, with $V_{ci} = 700$ V.

of a magnetic core, $I_{Rc}, L1$, the magnetising inductance, $I_{Lm}, L1$, the pulse capacitor, $I_{Cs}, L1$ and for the free-wheeling diode, $I_{Di}, L1$. After the turn-on of the switch, at time point 500 ns, the load current I_{load} starts flowing. The rise time of the load current from 0.01 % to 99.9 % of the maximum amplitude of the pulse flat-top is approximately 50 ns. During the rise time, the current starts flowing through the loss resistance of a magnetic core. The current of the core loss resistance is shown as $I_{Rc}, L1$ in Fig. 4.4. When the current starts flowing in the primary circuit, a voltage is applied across the magnetising inductance, and the magnetising current, shown as $I_{Lm}, L1$ in Fig. 4.4 starts flowing through it. The magnetising current increases almost linearly and its maximum value can be estimated with Eq. (3.2) given in Chapter 3. To estimate the change of the magnetising current during a given time t , Eq. (3.2) can be written as follows:

$$\Delta I_{Lm} \approx \frac{V_{layer} \times t}{L_m} \quad (4.2)$$

In Eq. (4.2), V_{layer} is the voltage which is induced to the secondary winding by a single layer, L_m is the linear magnetising inductance and ΔI_{Lm} is the change of the magnetising current. In Eq. (4.2), it is assumed that voltage V_{layer} is constant during the time t and therefore it is an approximation and will result in the magnetising current being slightly overestimated. In Fig. 4.4, the magnetising current $I_{Lm}, L1$ increases linearly and its maximum value is 67.8 A at 1.5 μs . According to Eq. (4.2), the maximum magnetising current with 1 μs pulse duration, a half of rise

and fall times taken into consideration, 690.4 V of voltage and 10 μH magnetising inductance gives 69.0 A, which is a reasonably good estimate.

The current flowing in each primary circuit, shown as I_{Cs} , $L1$ in Fig. 4.4 is fed from the pulse capacitors during a pulse. The capacitor current I_{Cs} , $L1$ is the sum of the load current and the currents which flow through the magnetising inductance and the core loss resistor. In this simulation, the peak value of the capacitor current is 161 A at time point 1.51 μs in Fig. 4.4. This is considerably larger than the peak value of the load current, I_{load} , which is 69 A in Fig. 4.4. However, theoretically the magnetising current and the core loss current are only weakly dependent on the load current, and if the load current is increased e.g. by increasing the output voltage of an inductive adder by increasing the number of the layers of the adder stack, and the charging voltage of the pulse capacitors remains the same, the magnetising current and the core loss current are a smaller proportion of the load current.

In this simulation, the maximum voltage which is induced to the secondary stalk by each primary layer is 690.4 V, which is 9.6 V less than the initial voltage of the pulse capacitors, 700 V. The majority of this voltage loss is caused by the on-state resistance of the switches, R_{sw} , which is modelled in switch S_1 in Fig. 4.2. In the very beginning of the pulse, at the time point 550 ns in Fig. 4.4, the current flowing through the switch in each layer is the sum of the load current and the current flowing through the loss resistance of a magnetic core. The maximum load current is 69.0 A and the current of the core loss resistor is 25.1 A. These cause in total 7.9 V of voltage across the on-state resistance R_{sw} , the value of which is 84 m Ω , as given in Table 4.1. The second contributor for the voltage drop in the primary circuit is the primary loop resistance R_p , which is 6.3 m Ω . At the beginning of the pulse, the voltage drop across the primary loop resistance is 0.6 V. The third contributor is primary loop inductance L_{pl} , which is 12 nH. The voltage across the inductance is given by the following equation:

$$V \approx L \frac{\Delta I}{\Delta t} \quad (4.3)$$

In Eq. (4.3), V is voltage, L is inductance, ΔI is the change of current in the time period of Δt . During the flat-top of the output pulse of an inductive adder, the current through the magnetising inductance, shown as I_{Lm} in Fig. 4.4, increases and the rate of change of I_{Lm} is 69 A/ μs .

By substituting this to Eq. (4.3), together with primary loop inductance L_{pl} , the value of which is 12 nH in Table 4.1, gives 0.83 V for the voltage across L_{pl} . In total, these three main contributors to the voltage drop in the primary circuit, namely R_p , R_{sw} and L_{pl} , sum up to 9.3 V, which is 97 % of the total voltage loss. The majority of the missing 0.3 V is contributed by the additional resistive losses in R_p and R_{sw} which are caused by magnetising current I_{Lm} , which is not exactly zero at the end of the rise time of the pulse. A more detailed study of contributors to the droop of the output voltage of an inductive adder is given in Section 4.3.1.

A point to note is that in this simulation, the 50 Ω load was connected to the inductive adder, which is designed to have a 50 Ω output impedance. Therefore, the load was matched to the output impedance of the inductive adder. There is not overshoot neither ringing on the pulse flat-top of the load voltage, which is shown as V_{load} in Fig. 4.3. In reality, a high-voltage feedthrough and a coaxial cable would be needed to connect the output of the inductive adder to the load and the impedances of all parts of the kicker system will not be perfectly matched to each other. Impedance mismatches in the kicker system cause partial reflections of the pulses, which may cause ripple on the load voltage. Contributors to the flat-top stability of the output voltage of an inductive adder and the load voltage of a stripline kicker system are shown in Section 4.3.

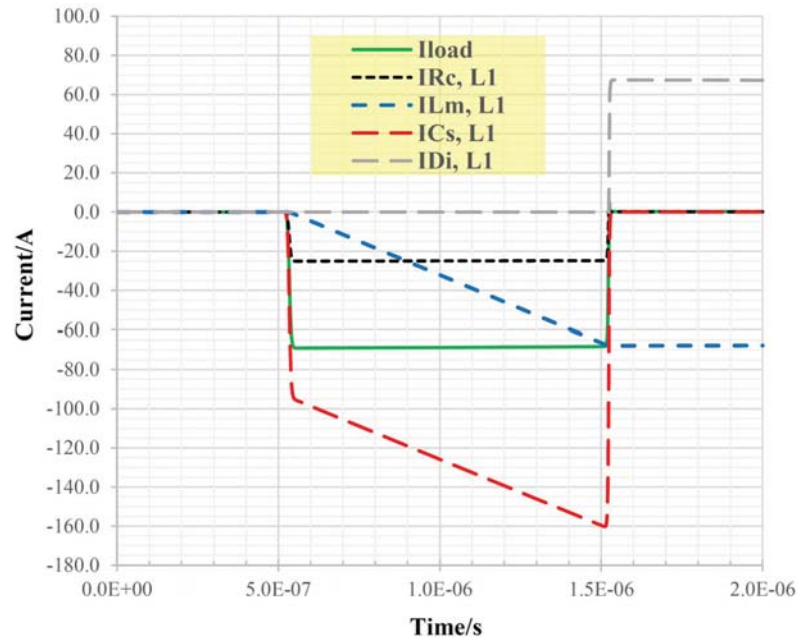


Figure 4.4. Simulated I_{load} , $I_{Rc}, L1$, $I_{Lm}, L1$, $I_{Cs}, L1$, and $I_{Di}, L1$, of an inductive adder with five constant voltage layers, with $V_{ci} = 700$ V.

4.2 Simulations of Typical Fault Conditions

As it was emphasised in Section 2.3.3, an inductive adder is in principle moderately fault-tolerant and a failure of a single switch or layer does not stop the operation of the modulator but may increase stress on other components. This section presents simulations of typical fault conditions of an inductive adder and the consequences of the faults for the operation of the adder.

4.2.1 Delayed or Advanced Triggering of a Single Layer

Figure 4.5 shows the output waveform of an inductive adder in the case when a single constant voltage layer switches on later than the other constant voltage layers of the inductive adder. The trigger delay of the switches in the single layer, which are turned on last, is 250 ns in comparison with the switches in the other layers. This relatively large delay is chosen to emphasise the effect. In this simulation, the pulse capacitors of the constant voltage layers were initially charged to 700 V and the simulation model consisted of five identical constant voltage layers, which were similar to the one shown in Fig. 4.1. The switches of four layers of the inductive adder are turned on at 500 ns and the load voltage, shown as V_{load} in Fig. 4.5, reaches approximately 2760 V at 550 ns. The switches of layer $L1$ of the stack are turned on at 750 ns and the output waveform reaches 3452 V. The switches of four layers are turned off at 1.5 μs . The output voltage of the inductive adder drops to the voltage, which corresponds to the net voltage of a single layer, approximately 685 V, and the output pulse terminates at 1.75 μs when the switches of the last conducting layer are turned off.

The amplitude of the load voltage, shown as V_{load} in Fig. 4.5, is significantly lower for the first 250 ns in comparison with the load voltage in normal operation, in which all the layers are switched on at the same time. The difference of the load voltages corresponds approximately to the net voltage of a single layer, 690 V. However, when all the primary layers are conducting at 800 ns, the flat-top of the output waveform for the output of the adder, V_{load} , is clean and similar to the normal operation shown in Fig. 4.3 until 1.5 μs . The only difference is that because the first layer is switched on later than the four other layers of the inductive adder, the droop of this layer is smaller at time 800 ns, after the rise time of the voltage of this layer. This means that the absolute amplitude of

the output waveform is approximately 1.5 V larger than during normal operation, from 800 ns to 1.5 μ s. At the time point when the four other layers are turned off, the layer in which the turn-on of the switches were delayed, remains conducting and the load voltage of the adder, shown as V_{load} in Fig. 4.5, is the net voltage of a single layer, approximately 680 V, until 1.75 μ s, when the switches of that layer are turned off.

Figure 4.6 shows the simulated output voltage of the inductive adder in the situation in which a single layer is switched on 250 ns in advance with respect to other four layers, and it is turned off 250 ns earlier than the other layers of the stack. The load voltage, shown as V_{load} in Fig. 4.6, is comparable to the normal operation from time point 550 ns to 1.25 μ s. In this case, the absolute amplitude of the output waveform during the flat-top is approximately 1.5 V smaller than in the normal operation, because at 500 ns, when four layers are switched on, the first layer has been conducting for 250 ns, which causes a droop of that amplitude for the net voltage of that layer.

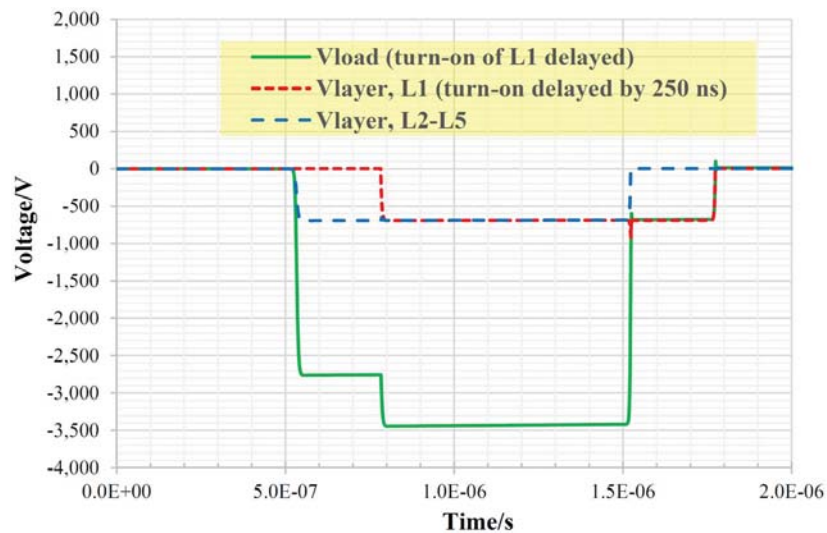


Figure 4.5. Simulated V_{load} and V_{layer} , L2-L5 of layers which are operating normally, and V_{layer} , L1 of a layer, which is turned on 250 ns late with respect to other layers. The inductive adder is equipped with five constant voltage layers, with $V_{ci} = 700$ V.

4.2.2 Fault in a Switch

A Switch Does Not Turn on

A fault in a switch of an inductive adder may occur e.g. as a consequence of a fault in a gate drive circuit or a fault in a single semiconductor switch of the primary circuit. In the inductive adder designs shown in this dis-

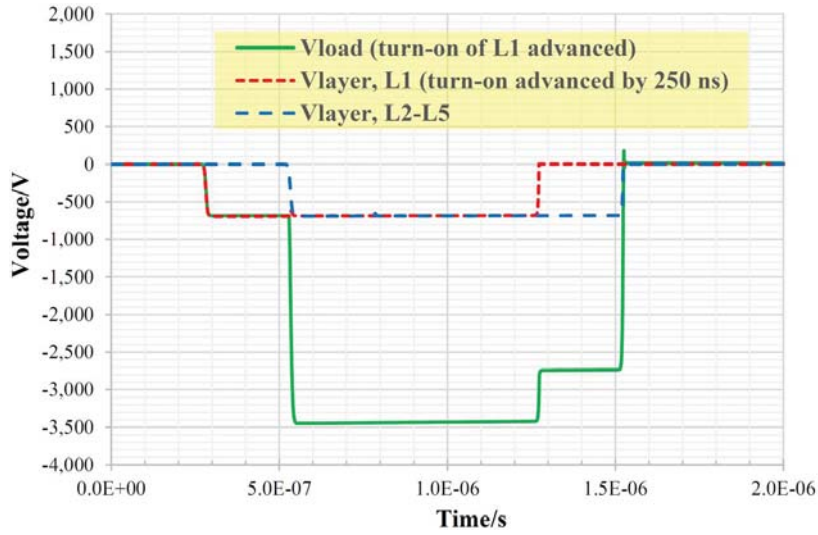


Figure 4.6. Simulated V_{load} and $V_{layer, L2-L5}$ of layers which are operating normally, and $V_{layer, L1}$ of a layer, which is turned on 250 ns in advance with respect to other layers. The inductive adder is equipped with five constant voltage layers, with $V_{ci} = 700$ V.

sertation, there are eight branches in parallel in a single layer of an inductive adder and therefore the layer, in which the switch fault happens, remains operational until the end of the pulse. However, the current per switch in the layer is increased and also the droop of the output pulse, as a consequence of larger losses in the switches in the layer, in which the fault has happened. In this simulation, the PSpice model of an inductive adder consisting of five layers was used. Four layers of the inductive adder were similar to the model shown in Fig. 4.1 and a single layer was modelled with eight parallel current branches in the primary side, shown in Fig. 4.2. A single switch of that layer, namely L1, was not turned on during the pulse. For reference, Fig. 4.7 shows the simulated voltages of the layers L1-L5 of an inductive adder, $V_{layer, L1-L5}$, in the case when all layers are operating normally and in this case, each of five layers generates the same voltage. The sum of the voltages of the layers, which is the load voltage, is shown in Fig. 4.8 as V_{load} .

If a single switch does not turn on, each operating switch of that layer must carry more current, which increases the losses per switch and also the losses of each operating primary loop. This causes the net voltage of that layer, in this case L1, to be lower than the net voltage of the layers which are operating normally. In Fig. 4.7, $V_{layer, L1}$, is the net voltage of a layer in which a single switch fails to switch on. Voltage $V_{layer, L1}$ is lower than the net voltage of layers, which are operating normally, shown as $V_{layer, L1-L5}$ in the same figure. The difference of the voltages is approxi-

mately 1.6 V at 550 ns. The effective switch resistance increases by 14 %, if a single switch of eight switches fails to turn on. In Section 4.1.2, the voltage across the on-state resistance of the switches was estimated to be 7.9 V and the losses across the primary loop resistance 0.6 V if a layer was operating normally. A 14 % increase of these losses gives an increase of 1.2 V for the total voltage drop in the primary loop, which corresponds to the predicted decrease in the load voltage. In Fig. 4.8, the load voltages are shown for the case in which the adder is operating normally, V_{load} , and in the case in which a single switch fails to turn on, $V_{\text{load,fault}}$. The amplitude of the pulse at 550 ns is effectively 1.2 V smaller in the case of a switch fault.

In Fig. 4.7, the droop of the net pulse of the layer, in which a single switch does not turn on, is larger than the droop of the net voltage of the layers, which are operating normally. However, the net voltage of the other layers of the stack, shown as $V_{\text{layer}, L2-L5}$, is practically the same as in the case of normal operation, and the droop is also of the same magnitude. The larger droop of the net voltage of layer L1, in which a single switch fails to turn on, is also caused by the increase of dynamic losses in the primary loop during the pulse. The contributors to the droop is discussed more in detail in Section 4.3.1. However, a point to note here is that the magnitude of the droop of an inductive adder can be dominated by the resistive losses and the magnetising current of each layer, as is the case here. In Fig. 4.7, the droop of the net pulses of the layers, which are operating normally, $V_{\text{layer}, L1-L5}$, is approximately 7 V. A 14 % increase of the primary loop resistance increases the droop approximately by 14 %, to 8 V, as is seen in Fig. 4.7 for $V_{\text{layer}, L1}$. The same differences of the pulse amplitude and magnitude of the droop are also visible in Fig. 4.8, for $V_{\text{load,fault}}$ in comparison with V_{load} .

A Switch Does Not Turn off

In this simulation, the same simulation models were used as in the previous section. Four layers of the inductive adder were similar to the model shown in Fig. 4.1 and a single layer, layer L1, was modelled with eight parallel current branches in the primary side, shown in Fig. 4.2. A single switch of layer L1 did not turn off after the pulse. For a reference, Fig. 4.9 shows the simulated net voltages of the layers L2-L5 of an inductive adder, $V_{\text{layer}, L2-L5}$, which are operating normally. In the same figure, V_{load} is the load voltage and $V_{\text{layer}, L1}$ is the net voltage of layer L1,

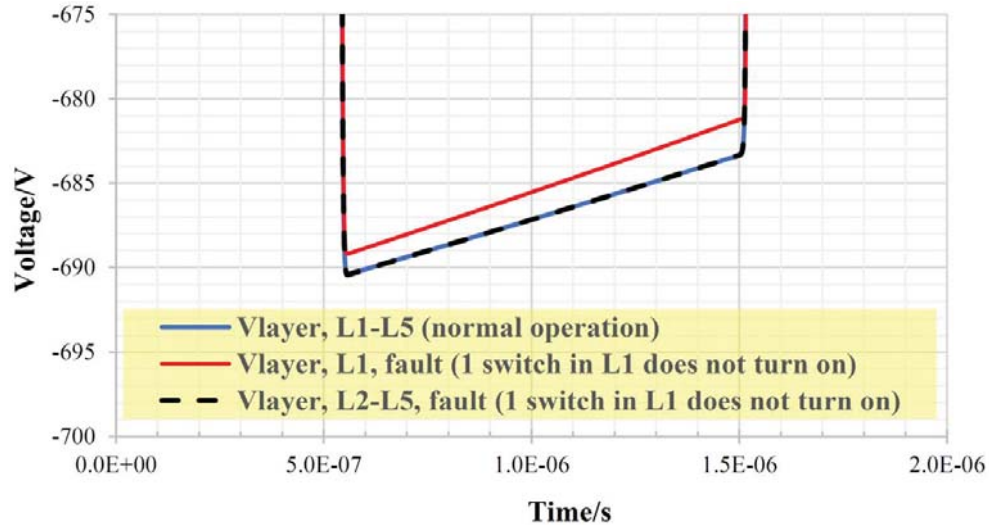


Figure 4.7. Simulated $V_{\text{layer}, L1-L5}$ of a single layer, in which all eight switches are switched on, and $V_{\text{layer}, L1, \text{fault}}$ for the case in which one of eight switches of in layer L1 does not turn on, and $V_{\text{layer}, L2-L5, \text{fault}}$ of layers which are operating normally when a switch in layer L1 does not turn on. The inductive adder is equipped with five constant voltage layers, with $V_{\text{ci}} = 700$ V.

in which a single switch does not turn off. The operation of the inductive adder is normal until the turn-off of the switches and therefore, the load voltage and the net voltages of the layers, shown in Fig. 4.9, corresponds to the load voltage and the net voltages of the layers during the normal operation, shown in Fig. 4.3, until $1.5 \mu\text{s}$.

The fault in the inductive adder happens at $1.5 \mu\text{s}$, when a switch in layer $L1$ does not turn off at the time when the other switches in that layer and in other layers turn off. The load voltage in Fig. 4.9 falls to zero and after a short transient, it rises to approximately at 650 V. This voltage corresponds to approximately the net voltage of layer $L1$, which is shown as $V_{\text{layer}, L1}$ in Fig. 4.9. The net voltage of the other layers, in which all the switches turn off normally is shown as $V_{\text{layer}, L2-L5}$ and after $1.55 \mu\text{s}$ the net voltage of the other layers is the forward voltage of the diodes in these layer, approximately 2 V.

Figure 4.10 shows the simulated currents in the case in which a single switch of a layer fails to turn off. Similarly to the load voltage shown in Fig. 4.9, the load current, shown as I_{load} in Fig. 4.10 continues flowing at a reduced magnitude after time point $1.55 \mu\text{s}$, when the switches of layers $L2-L5$ and the switches of layer $L1$ except the switch in branch $B1$ are turned off. In Fig. 4.10, $I_{\text{Sw}, L1, B2-B8}$ is the current of the switches of seven current branches, $B2-B8$, of layer $L1$, which are turned off at $1.5 \mu\text{s}$. $I_{\text{Lm}, L1, B1}$ is the current of the switch of branch $B1$, which does

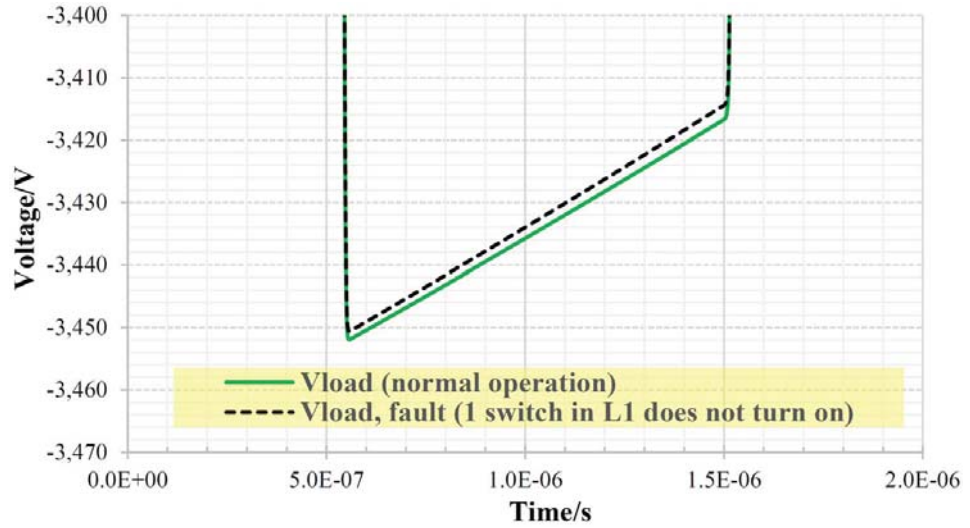


Figure 4.8. Simulated V_{load} in the case in which all layers are operating normally and $V_{load, fault}$ in the case in which a single switch in one layer does not turn on. The inductive adder is equipped with five constant voltage layers, with $V_{ci} = 700$ V.

not turn off. After the currents of the other branches in $L1$ fall to zero, the switch in branch $B1$ needs to carry the load current, shown as I_{load} in Fig. 4.10 as well as magnetising current, I_{Lm} , $B1$, and the current flowing through the core loss resistor, I_{Rc} , $B1$. Immediately after turn-off of all the other switches in branches $B2$ - $B8$ of layer $L1$ and in other layers at time point $1.5 \mu s$, the current flowing through the switch in branch $B1$ in layer $L1$ increases to 105 A, and then it continues increasing with the same gradient as the magnetising current of that layer, shown as I_{Lm} , $S1$ in Fig. 4.10.

If the switch, which remains conducting after turn-off of the other switches in the same layer, continues conducting long enough, the magnetic core of that layer is driven into saturation. The inductance of the saturated core is very low, and the primary loop current which flows through the switch would start increasing very rapidly. Simulation of this fault condition is shown in Section 4.2.4. However, the current flowing through the switch increases to very high value and the power loss in the switch may cause it to be damaged irreversibly. As the worst case, the switch may remain in short-circuit. That fault condition is presented in Section 4.2.2. Depending on the internal structure of the switch, another possible result of a high current flowing through the switch is that the switch finally remains as an open circuit, and it will not turn on. This fault condition has been presented in Section 4.2.2. Usually the magnetic core is not damaged if it is driven into saturation. When the current in the primary circuit finally

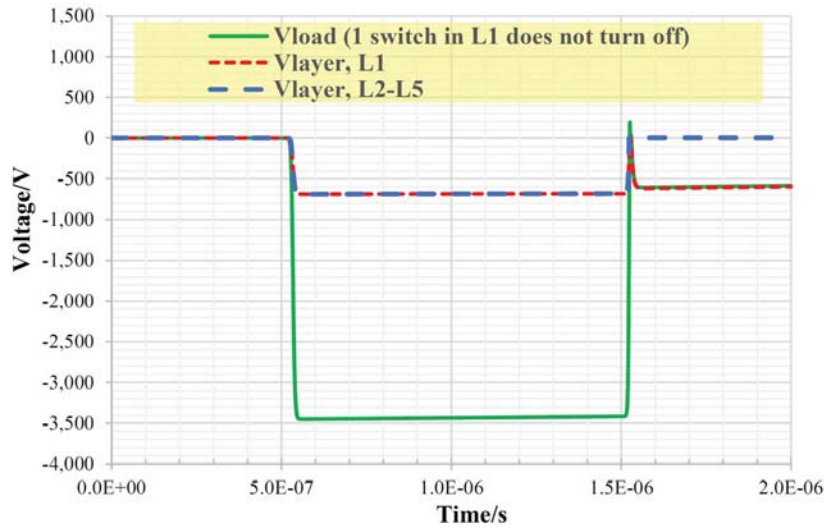


Figure 4.9. Simulated V_{load} and V_{layer} , $L2-L5$ of layers which are operating normally, and V_{layer} , $L1$ of a layer, in which a switch does not turn off at the end of a pulse. The inductive adder is equipped with five constant voltage layers, with $V_{ci} = 700$ V.

vanishes, e.g. as result of complete discharge of the pulse capacitor of the current branch in which the switch failure occurred, the magnetic field in the core returns to the remanent value and the core will have its normal, high, inductance.

A Switch in Short-circuit

A turn-off failure of a single switch in the primary circuit of an inductive adder may destroy the switch, in which the fault happens, especially if the core is driven into saturation as a result of that turn-off fault. Other faults which may cause a short-circuit in a switch are a failure in the gate driver or high, rapidly changing, voltage or current in the primary circuit. High transient voltages and currents may occur as a result of a fault in another current branch in the same layer or in another layer of the inductive adder, or a fault in the kicker system to which the inductive adder is connected. If a short-circuit happens in a single switch, the pulse capacitor of that branch is discharged completely through the switch. In this simulation, it is assumed that the other capacitors remain charged, i.e. the capacitors are charged through diodes or relatively high impedances and a short-circuit in one current branch does not cause the other capacitors to be discharged through the branch in which the short-circuit occurred.

Figure 4.11 shows the load voltage, V_{load} , in the case in which a switch in a single branch is in short-circuit (black). The pulse capacitors of this branch is assumed to be completely discharged in the beginning of the

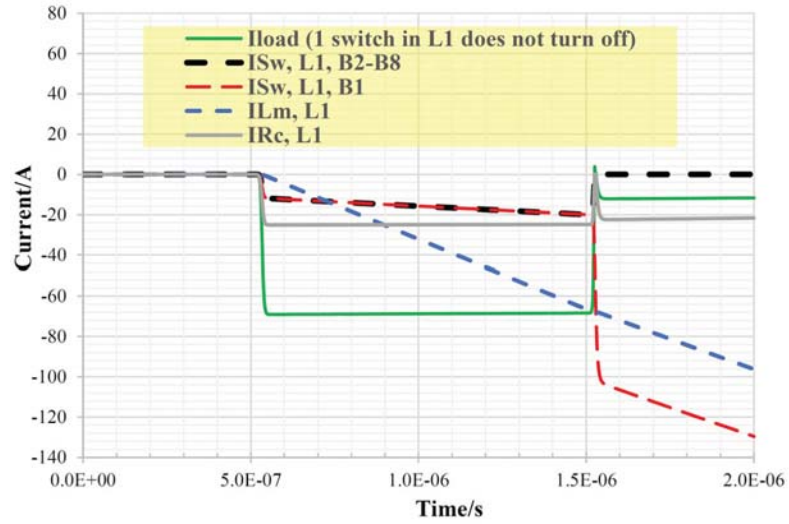


Figure 4.10. Simulated I_{load} and $I_{Sw, L1, B2-B8}$ of switches of layer L1 which turns off normally, and $I_{Sw, L1, B1}$ of a switch in L1, which does not turn off at the end of a pulse, and $I_{Lm, L1}$ and $I_{Rc, L1}$ in layer L1. The inductive adder is equipped with five constant voltage layers, with $V_{ci} = 700$ V.

simulation, at 0 ns. For reference, in Fig. 4.11, the load voltage is also shown for the case in which all five layers are operating normally (green). The amplitude of the load voltage is lowered by approximately 100 V. In Fig. 4.11, the net voltages are also shown for layer L1, as $V_{layer, L1}$, in which a switch is in short-circuit, and for the layers which are operating normally, as $V_{layer, L2-L5}$. The amplitude of the net voltage of L1 is approximately 100 V less than the net voltage of the other layers. The droop of the net voltage of layer L1 is not considerably larger than the droop of the net voltages of the other layers.

Figure 4.12 shows the simulated currents of the fault condition, in which a single switch in layer L1 is in short-circuit. When the switches of the branches B2-B8, which are operating normally, are switched on in layer L1, currents start flowing through these switches. The current of the switches in these branches is shown as $I_{Sw, L1, B2-B8}$ in Fig. 4.12 and the current increases up to 130 A in 500 ns. The current of a switch of a single branch in normal operation is approximately 16 A, as is shown in Fig. 4.10 for $I_{Sw, L1, B2-B8}$. The reason for the high current flow in the switches in branches B2-B8 in Fig. 4.12 is that the pulse capacitors of these branches charge the capacitor in the branch which is in short-circuit.

The current flowing through the switch in branch B1 in layer L1 is shown as $I_{Sw, L1, B1}$ in Fig. 4.10 and the predicted peak current through the switch is 791 A at 1.1 μ s. The direction of the current in branch B1 is opposite in comparison with the other branches in layer L1. The net

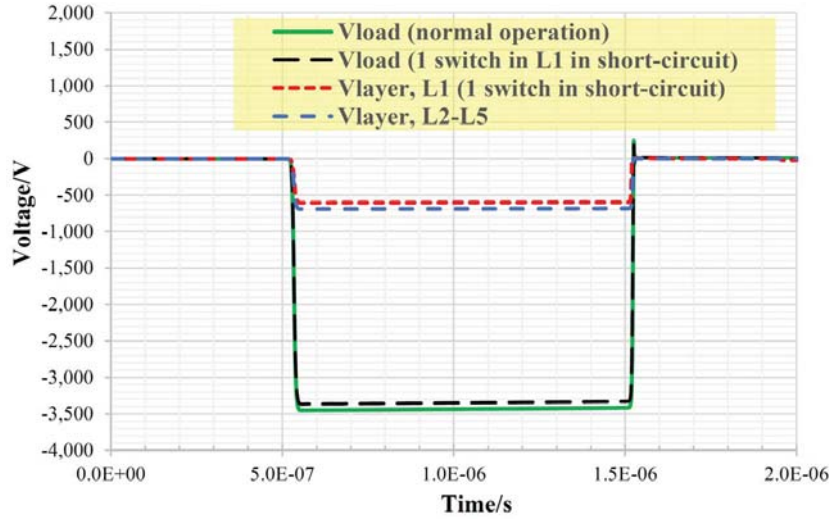


Figure 4.11. Simulated V_{load} in the case when a single switch of a single layer is in short-circuit (black) and in the normal operation (green), $V_{layer, L1}$ of the layer in which a switch is in short-circuit and $V_{layer, L2-L5}$ of layers, which are operating normally. The inductive adder is equipped with five constant voltage layers, with $V_{ci} = 700$ V.

voltage of that layer is lower than the net voltage of the other layers, because there is high discharge current from the capacitors, which cause relatively high voltage drop across the switches, primary loop resistances and primary loop inductances. This effectively decreases the net voltage of that layer by 100 V. The net voltage of layer $L1$ is shown as $V_{layer, L1}$ in Fig. 4.11. However, the magnetising current of that layer, shown as $I_{Lm, L1}$ in Fig. 4.12, is effectively lower than in the other layers, because the voltage across the magnetising inductance is lower, and at the end of pulse, at $1.55 \mu s$, it starts decreasing normally. The diode current of the layer, in which a switch is in short-circuit, is very high after the pulse, as is shown as $I_{Di, L1}$ in Fig. 4.12. The reason for high diode current is that the current in branch $B1$ is very high and it stores energy in the parasitic loop inductance of that branch. When the switches in branches $B2-B8$ turn off, the current of branch $B1$ starts flowing through the diode of that layer, and then decays as the capacitor discharges.

4.2.3 Fault in a Load

A Short-Circuit in the Stripline

In this simulation, an inductive adder is connected to a stripline electrode with a cable and a short-circuit occurs at the input to a stripline electrode. The cable and the stripline were modelled as lossless transmission lines.

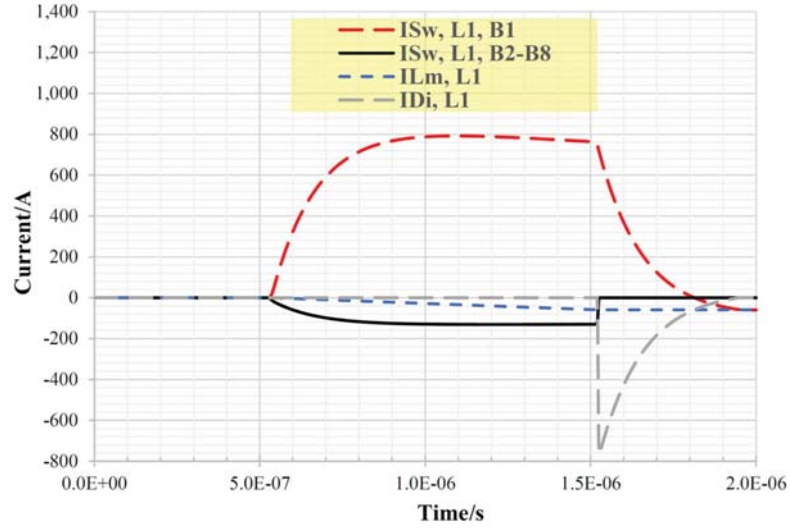


Figure 4.12. Simulated $I_{Sw, L1, B1}$ of a switch of layer L1 which does not turn off at the end of a pulse, and $I_{Sw, L1, B2-B8}$ of switches of layer L1 which turn off normally, and $I_{Lm, L1}$ and $I_{Di, L1}$ in layer L1. The inductive adder is equipped with five constant voltage layers, with $V_{ci} = 700$ V.

Fig. 4.13 shows the schematic of the circuit used in this simulation. In Fig. 4.13, T_{cable} is the cable between the adder and a stripline, $T_{stripline}$ is the stripline electrode and R_{load} is the terminating resistor. The simulation model of the inductive adder consisted of five identical layers, which were similar to the model of a single layer shown in Fig. 4.1. The parameters of the simulation model are shown in Table 4.1. In this simulation, the impedances of the cable, stripline and load were 50Ω and the propagation delays of the cable and the stripline were 11.5 ns and 7 ns, respectively. The stripline electrode was short-circuited via switch S_{w1} , which is shown in Fig. 4.13.

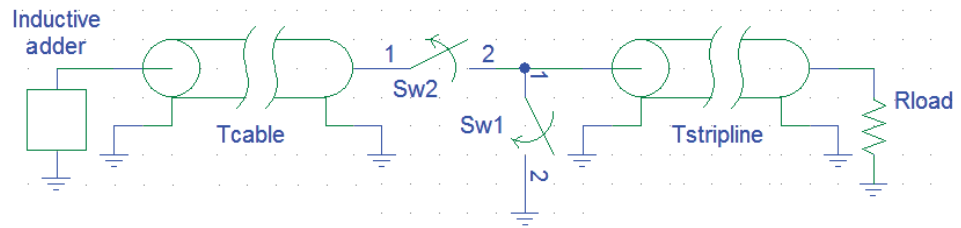


Figure 4.13. Schematic of the load fault simulations.

Figure 4.14 shows the load voltage V_{load} , output voltage of an inductive adder, V_{out} and net voltage of each layer, $V_{layer, L1-L5}$ in the case when the input end of the stripline electrode is connected into a short-circuit at 750 ns. The transient time of the short-circuiting switch S_{w1} is 1 ns. The load voltage, shown as V_{load} , in Fig. 4.14, drops to zero after the propa-

gation delay of the stripline and there is a considerable backswing of the pulse amplitude, caused by the inductance of the circuit. In Fig. 4.15, it can be seen that the short-circuit causes the output current I_{out} and the current flowing from pulse capacitors of each layer, $I_{\text{Cs}}, L1-L5$, to start increasing very rapidly. The gradient of the current rise is defined by the voltage on the capacitors, the total inductance of the primary circuit, the secondary circuit and the cable, and it reaches $5 \text{ kA}/\mu\text{s}$ during the first 200 ns after the short-circuit occurs and the peak load current is 3.17 kA. The output voltage of the inductive adder, shown as V_{out} in Fig. 4.14, decreases because of high resistive losses in the primary circuit and because of drop of the capacitor voltage. In this simulation, the fault in stripline occurs quickly, in 1 ns, and this fast change triggers oscillations in the cable, which connects the inductive adder to the stripline. The oscillations in the output voltage V_{out} are coupled to the primary side of the inductive adder and they are visible also in the net voltage of the layers, shown as $V_{\text{layer}}, L1-L5$ in Fig. 4.14.

In the simulation, the pulse is terminated at time $1.5 \mu\text{s}$ when the primary switches are turned off and the output current I_{out} starts decreasing. The current does not return to zero immediately and in the primary side, the current starts flowing through the free-wheeling diodes. The diode current is shown in Fig. 4.15 as $I_{\text{Di}}, L1-L5$. The maximum diode current is 3.23 kA and it is the sum of the peak load current and the peak magnetising current, at time $1.52 \mu\text{s}$. The magnetising current of the magnetic cores, shown as $I_{\text{Lm}}, L1-L5$ in Fig. 4.15, is slightly lower than in normal operation. The net voltages of the layers of the inductive adder are lower than in normal operation, as consequence of higher currents, and therefore higher resistive losses, in the primary circuits.

In a real set-up, it is important that the fault condition is detected and the current reduced towards 0 A, in order to protect both the inductive adder and the load. Thus, in the final implementation of the inductive adder for the CLIC DR kicker system, a fault current detection circuit will be needed in order to switch off the MOSFETs with a relatively short delay.

An Open-Circuit in the Stripline

An open circuit in the load was simulated with the same model as the short-circuit, except that in this case a stripline electrode was disconnected from the cable by switch S_{w2} , shown in Fig. 4.13. The stripline

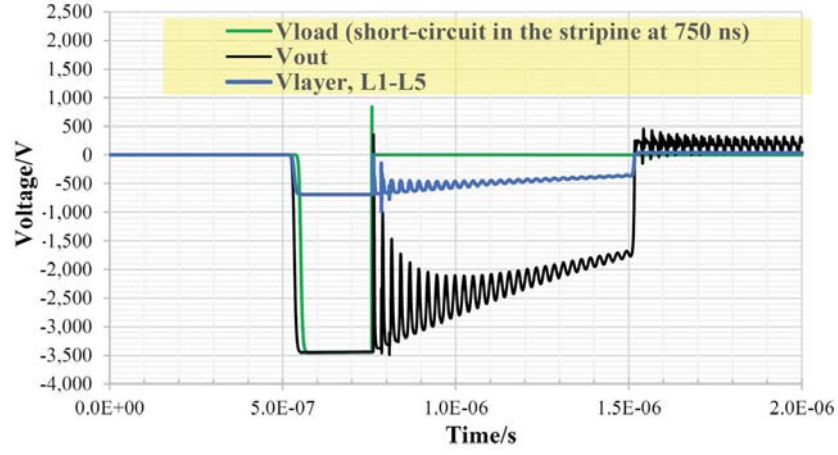


Figure 4.14. Simulated V_{load} , V_{out} and $V_{layer, L1-L5}$ in the case, when a short-circuit fault occurs in a kicker stripline at 750 ns. The inductive adder is equipped with five constant voltage layers, with $V_{ci} = 700$ V.

electrode was disconnected at time point 750 ns. Fig. 4.16 shows the load voltage V_{load} , output voltage of an inductive adder, V_{out} and the net voltage of each layer, $V_{layer, L1-L5}$ in the case when the stripline electrode is disconnected from the cable at 750 ns. The transient time of the opening of switch S_{w2} is 1 ns.

The load voltage drops to zero after the propagation delay of the stripline and there is a relatively high backswing in the load voltage, approximately 800 V, which is caused by the circuit inductance. The output voltage of the inductive adder, V_{out} remains at the same average value, but the fast open-circuit causes reflections on T_{cable} and these reflections are coupled to the primary side of the inductive adder, to $V_{layer, L1-L5}$. The peak amplitude of the oscillations in the output is predicted to be 7.5 kV and the oscillations are damped by the resistive losses in the primary and in the secondary circuits. Fig. 4.17 shows the load current I_{load} , output current of an inductive adder I_{out} , current of the pulse capacitors, $I_{Cs, L1-L5}$ and the magnetising current of each layer, $I_{Lm, L1-L5}$. It can be seen that turn-off of the primary switches, at 1.5 μs also triggers oscillations on the secondary circuits. The current of the pulse capacitors, $I_{Cs, L1-L5}$, is forced to zero. After turn-off, the oscillations of I_{out} die out slowly, because of low resistive losses in the secondary circuit. A point to note is that the magnetising current in the primary circuits of an inductive adder, shown as $I_{Cs, L1-L5}$ in Fig. 4.17, increases until the switches turn off, similarly as in the normal operation. The final magnitude of the magnetising current is slightly higher than in the normal operation, because the resistive losses of output current are smaller than in normal operation.

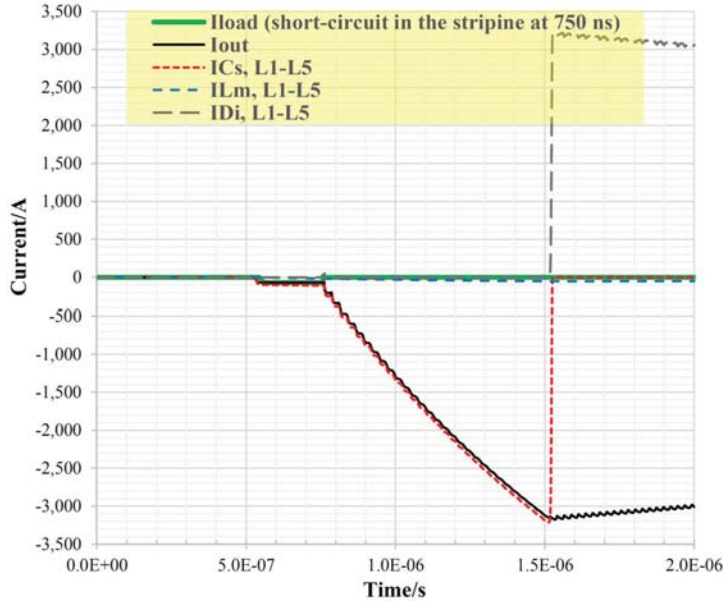


Figure 4.15. Simulated I_{load} , I_{out} , I_{Cs} , $L1-L5$; I_{Lm} , $L1-L5$ and I_{Di} , $L1-L5$ in the case, when a short-circuit fault occurs in a kicker stripline at 750 ns. The inductive adder is equipped with five constant voltage layers, with $V_{ci} = 700$ V.

4.2.4 A Magnetic Core is Driven into Saturation

In this simulation study, a magnetic core of a single layer was driven into saturation. This may happen if an inductive adder is operated with a pulse voltage and pulse duration which together exceeds the volt-second product of the magnetic core, or if a switch fails to turn off, as discussed in Section 4.2.2. In Eq. (3.6) presented in Section 3.4.4, it can be seen that the cross-sectional area and the maximum usable flux swing of the magnetic core equals to the product of the pulse voltage and the pulse duration. This is the maximum volt-second product, which can be applied across the core, and if it is exceeded, the core saturates. In this simulation, the pulse capacitors of the constant voltage layers were initially charged to 700 V and the simulation model consisted of five identical constant voltage layers, each of which was similar to the model shown in Fig. 4.1. In a layer, in which the core saturated, the magnetising inductance L_m was changed during the pulse from 10 μ H to 100 nH at time point 750 ns. In the model, this was done by having two magnetising inductances in parallel, and switching the 100 nH inductance on at 750 ns.

Figure 4.18 shows the load voltage of an inductive adder, V_{load} , voltages of layers which are operating normally, V_{layer} , $L2-L5$, and voltage of a layer, in which a magnetic core is saturated at 750 ns, V_{layer} , $L1$. Fig. 4.19 shows the load current, I_{load} , and the magnetising current of the mag-

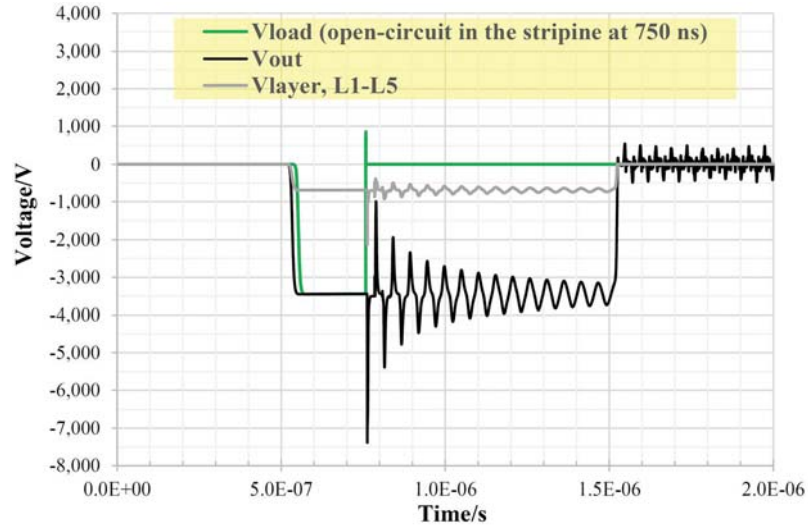


Figure 4.16. Simulated V_{load} , V_{out} and $V_{layer, L1-L5}$, in the case when an open-circuit fault occurs in a kicker stripline at 750 ns. The inductive adder is equipped with five constant voltage layers, with $V_{ci} = 700$ V.

netic cores of the layers, which are operating normally, $I_{Lm, L2-L5}$, and the magnetising current of a layer, in which a magnetic core saturates at 750 ns, $I_{Lm, L1}$. It can be seen in Fig. 4.19 that when the magnetic core saturates, the voltage of that layer, shown as $V_{layer, L1}$ in Fig. 4.18 starts to decrease. The other layers continue operating normally, and the net voltage of these layers is shown as $V_{layer, L2-L5}$ in Fig. 4.18. The load voltage, V_{load} in the same figure, starts decreasing and its droop from 750 ns to the end of the pulse, $1.5 \mu s$, is dominated by the voltage of the layer in which the core is saturated.

In Fig. 4.19, it can be seen that the magnetising current of the layer, in which the core saturates, $I_{Lm, L1}$, and the magnetising currents of other layers, $I_{Lm, L2-L5}$, are the same until time point 750 ns. Then, the magnetising current of layer $L1$ starts increasing very rapidly. The load current, I_{load} , shown in the same figure, starts decreasing more rapidly at 750 ns than in the first 250 ns of the pulse, as a consequence of the drop of the voltage $V_{layer, L1}$, shown in Fig. 4.18. The magnetising current of the other layers, $I_{Lm, L2-L5}$ in Fig. 4.19, has the amplitude which is very similar to the normal operation. At 750 ns, the magnetising current of the saturated core starts increasing by approximately $6.1 \text{ kA}/\mu s$. The maximum gradient of the current rise is defined by the voltage of the pulse capacitor, approximately 688 V at 750 ns, and the total loop inductance of the primary circuit, 112 nH, which is the sum of the loop inductance of the primary circuit, 12 nH, and the magnetising inductance of the sat-

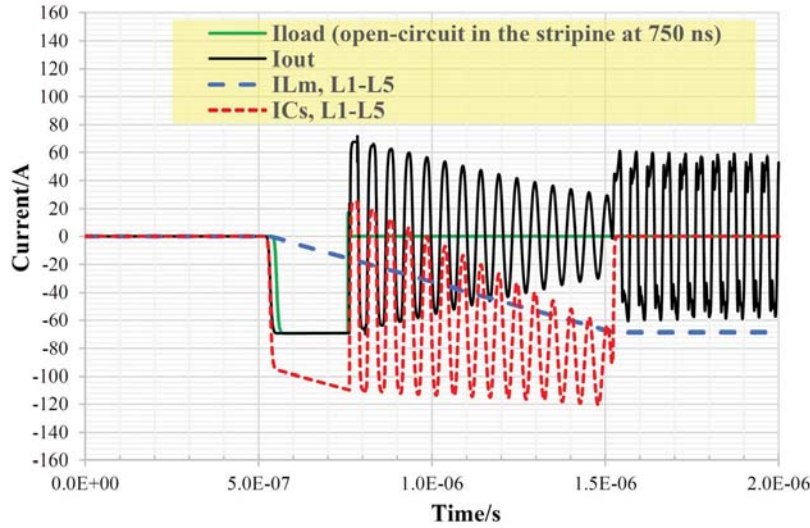


Figure 4.17. Simulated I_{load} , I_{out} , $I_{Cs, L1-L5}$, and $I_{Lm, L1-L5}$ in the case, when an open-circuit fault occurs in a kicker stripline at 750 ns. The inductive adder is equipped with five constant voltage layers, with $V_{ci} = 700$ V.

urated core, 100 nH. Fig. 4.20 shows the magnetising current $I_{Lm, L1}$ and it reaches 3.4 kA, before the semiconductor switches in that layer turns off at $1.5 \mu s$. After turn-off of the switches, the magnetising current starts flowing through the free-wheeling diode and this current is shown as $I_{Di, L1}$ in Fig. 4.20.

If the core is driven into saturation, the current in the primary circuit of the layer in which the core saturates is comparable to the case in which the load is connected in short-circuit, shown in Section 4.2.3. The difference is that in the case of saturation of a magnetic core, only one layer of primary circuit is carrying high current, whereas in the case of a short-circuit in the load, all the primary circuits are feeding the same current at the time of turn-off of the switches. As discussed in Section 4.2.3, in reality the switches could not necessarily reliably turn off if the primary current is too high, and even if the switches turn off, the transient voltages in the primary circuit may be very high, which may destroy the switches. Hence snubber circuits may be used to limit the voltage. Also, the resistive losses in the semiconductor switches and diodes of the layer, in which the core saturates, could cause these components to be irreversibly damaged. Therefore, the magnetic cores of an inductive adder should never be driven into saturation in any operating conditions.

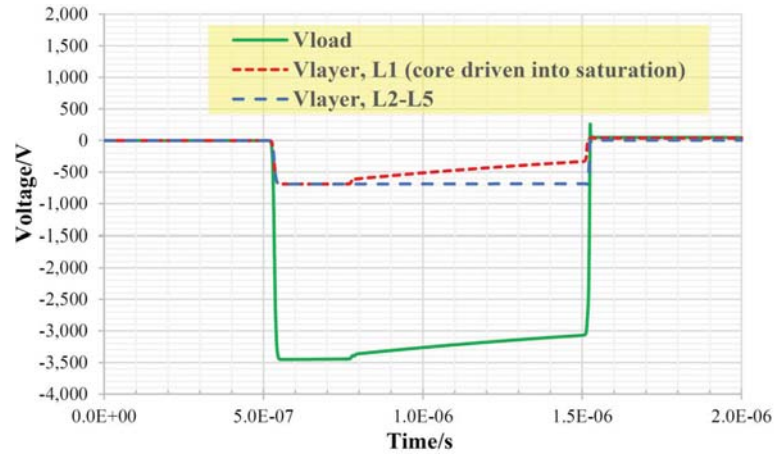


Figure 4.18. Simulated V_{load} and $V_{layer, L2-L5}$ of layers which are operating normally and $V_{layer, L1}$ of a layer, in which a magnetic core is saturated at 750 ns. The inductive adder is equipped with five constant voltage layers, with $V_{ci} = 700$ V.

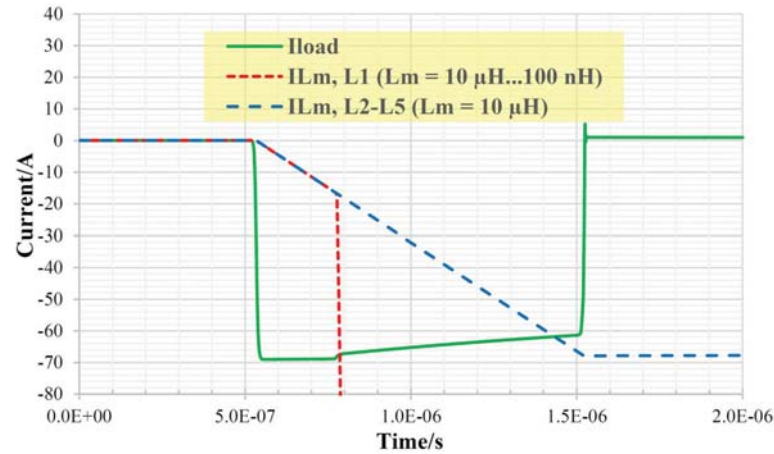


Figure 4.19. Simulated I_{load} and $I_{Lm, L2-L5}$ of layers, which are operating normally, and $I_{Lm, L1}$ of a layer, in which a magnetic core is saturated at 750 ns. The inductive adder is equipped with five constant voltage layers, with $V_{ci} = 700$ V.

4.2.5 Summary of Simulated Fault Conditions

Table 4.2 shows a summary of the results of the simulations of typical fault conditions and the consequences of these faults, which have been presented in Section 4.2. The worst cases are a short-circuit in the load, a single switch which does not turn-off at the end of the pulse, a single switch in short-circuit, and saturation of a magnetic core. Saturation of the magnetic core may be a result of other faults, e.g. a switch failing to turn off. In each of these fault conditions, the currents flowing in the primary circuits of an inductive adder increase rapidly and may reach very high amplitudes, potentially thousands of amperes.

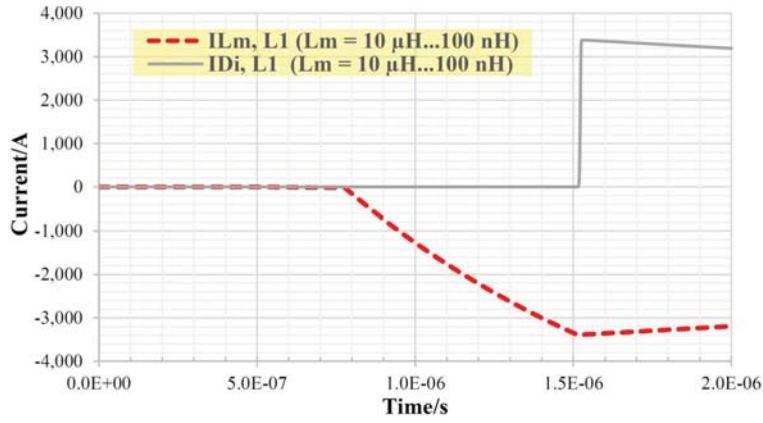


Figure 4.20. Simulated $I_{Lm}, L1$ and $I_{Di}, L1$ of a layer, in which a magnetic core is saturated at 750 ns. The inductive adder is equipped with five constant voltage layers, with $V_{ci} = 700$ V.

In order to avoid the magnetic cores to be driven into saturation, the cross-sectional area of the cores should be large enough to have sufficient margin, i.e. volt-second product which is e.g. 100 % larger than needed for a pulse in the nominal operation, as discussed in Section 3.4.4. However, this does not protect the primary circuits against e.g. a pulse with too long duration, which may be caused by a fault in the trigger system. A method to protect the semiconductor switches in this case would be to have integrator circuits in the primary, which switch off the semiconductor switches after a defined volt-second integral [68]. Another method to limit the current in the primary circuit in fault conditions, in which a core saturates or the load current starts to increase to too high amplitude, would be to add a current feedback in the primary loop. This could be implemented e.g. by a current sensing resistor. If the primary current exceeds the nominal primary current by e.g. two times, the semiconductor switches would be turned off. The turn-off of the switches could be done for example by grounding the input or output of a gate driver of the semiconductor switch via a fast MOSFET, the gate voltage of which would be defined by the voltage across the current sensing resistor. However, a feedback from a current sensing resistor to the gate driver or the switch is not effective if the fault occurs in the switch itself. If a switch is in short-circuit, the current continues increasing, until the capacitor voltage has decreased to the level, in which it starts limiting the current rise. For that reason, each layer of the inductive adder should also be protected by a fuse or other means, which switches off the charging current to the pulse capacitors of a single layer, if the voltages of the pulse capacitors of that layer drops suddenly, as a consequence of a short-circuit in a switch.

The drop of the output voltage of the inductive adder, which is caused by the loss of a single layer, can be compensated either by increasing the charging voltage of the other constant voltage layers, or by switching on a possible redundant layer in the adder stack.

Table 4.2. Summary of simulations of typical fault conditions of an inductive adder operating in a stripline kicker system and the consequences of the fault for the operation.

Description of fault	Consequences
Delay/advance of trigger of a layer	Pulse rise and fall times are increased Pulse flat-top duration is shortened Pulse flat-top amplitude is reduced
A switch fails to turn on	Pulse flat-top amplitude is reduced Pulse flat-top droop increases Power losses in switches increase
A switch fails to turn off	High power losses in the switch, which does not turn off Risk of saturation of a magnetic core Considerable voltage across the load during off-time
A switch in short-circuit	Very high current can flow through the short-circuited switch during a pulse High power losses in parallel switches during a pulse High current in the free-wheeling diode after the pulse
A magnetic core saturates	High power loss and high peak current in switches in the layer, in which the core saturates High peak current in diodes the layer, in which the core saturates
Short-circuit in a load	High power losses and high peak current in switches High peak current in diodes Risk of high transient voltage during turn-off
Open circuit in a load	Risk of high transient peak voltage in the secondary

4.3 Contributors to the Flat-top Stability of the Pulse Waveform of an Inductive Adder Driven Stripline Kicker System

4.3.1 Contributors to the Droop of the Pulse Flat-top of an Inductive Adder

In [40] an equation is given for calculating the required capacitance per layer for an inductive adder to keep the voltage droop per layer, during the pulse flat-top, within a defined limit. This is shown as Eq. (3.4) in Chapter 3 and is repeated here:

$$C_s = \frac{It_p}{\Delta V_{pl}} \quad (4.4)$$

In Eq. (4.4), C_s is the estimate for the required capacitance per layer to limit the droop per layer to ΔV_{pl} , t_p is the duration of the pulse flat-top and I is the sum of the load and magnetising currents. However, the author showed in [17] that the droop per layer is significantly dependent on the resistance of the semiconductor switches together with the increase in current flowing through the magnetising inductance during the pulse flat-top. These results are briefly reported here.

In Eq. (4.4), it is assumed that the current through the magnetising inductance is constant during the pulse. It is also assumed that the load voltage droop (ΔV_{load}) is equal to the sum of the voltage droops, which are caused in the constant voltage layers by the decreased voltage of the storage capacitors, i.e.

$$\Delta V_{load} = N(\Delta V_{pl}) \quad (4.5)$$

where N is the number of constant voltage layers in the inductive adder.

To give an example, Eq. (4.5) is applied to calculate the droop of an inductive adder, which includes five constant voltage layers. In these simulations, the capacitance per layer, in the constant voltage layer, is $24 \mu\text{F}$ and the pulse capacitors are initially charged to 300 V. The load resistance is 50Ω , the magnetising inductance of the magnetic cores is assumed to be constant and $10 \mu\text{H}$. The pulse flat-top duration is 350 ns and the rise time of the pulse is expected to be 100 ns. In order to estimate the droop of the capacitor it is necessary to first estimate the average magnetising current during the pulse flat-top. The magnetising current at the end of

the rise time is estimated from half of its duration and Eq. (4.2) is applied:

$$\Delta I_{Lm} = \frac{V_{layer} \times t}{L_m} = \frac{300 \text{ V} \times 50 \text{ ns}}{10 \mu\text{H}} = 1.5 \text{ A} \quad (4.6)$$

During the 350 ns pulse flat-top, the magnetising current increases by 10.5 A, according to Eq. (4.2):

$$\Delta I_{Lm} = \frac{V_{layer} \times t}{L_m} = \frac{300 \text{ V} \times 350 \text{ ns}}{10 \mu\text{H}} = 10.5 \text{ A} \quad (4.7)$$

Hence, the current in 10 μH magnetising inductance at the end of the 350 ns flat-top is 12.0 A and the average magnetising current during the pulse flat-top is 6.75 A. According to Eq. (4.4), the droop per layer for 30.0 A of load current and 6.75 A of magnetising current is 0.54 V. According to Eq. (4.5), the total droop in the output pulse is 2.7 V, which corresponds to 0.18 % of ideally 1.5 kV maximum voltage.

For comparison, Fig. 4.21 shows the simulated output waveform of the 5-layer inductive adder with the same parameters but with switch on-state resistance (0.34 Ω) modelled. The simulation model comprised five identical layers, each of which were similar to Fig. 4.31. The absolute maximum voltage of the output pulse, which has negative polarity, is 1.434 kV and the droop of the pulse flat-top is 21.1 V, which corresponds to 4.2 V per layer. The total droop corresponds to 1.5 % of the pulse voltage.

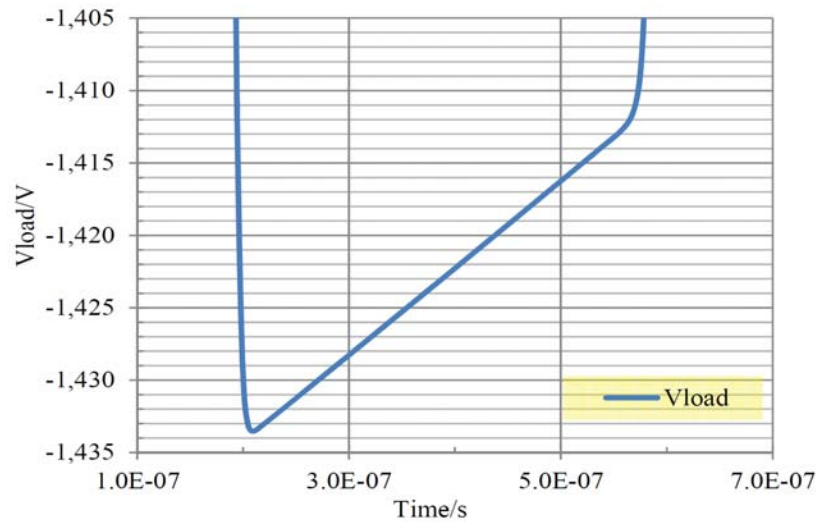


Figure 4.21. Simulated V_{load} of an inductive adder with five constant voltage layers, with $V_{ci} = 300 \text{ V}$.

The magnitude of the droop of the simulated waveform is 7.8 times larger than the estimate for the droop, given by Eq. (4.4) and (4.5). This

difference is mainly caused by Eq. (4.4) neglecting both the switch on-state resistance and the increase in magnetising current during the pulse flat-top. The constant voltage layer of an inductive adder behaves as an inductor-capacitor-resistor (LCR) circuit during the pulse, shown in Fig. 4.22. This circuit consists of storage capacitor C_s , which corresponds to the storage capacitance per layer. The storage capacitor is in series with switch resistance R_{sw} , which is the effective on-state switch resistance per layer. This series circuit is in parallel with both the magnetising inductance L_m and the load resistance per layer, R_{load}/N , which is the load resistance divided by the number of constant voltage layers of the inductive adder.

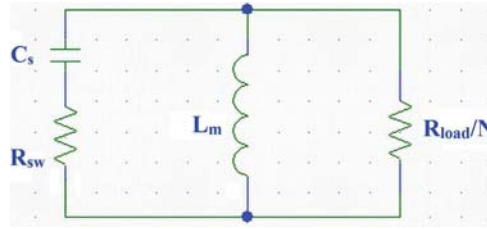


Figure 4.22. Simplified model of a constant voltage layer of an inductive adder during the pulse.

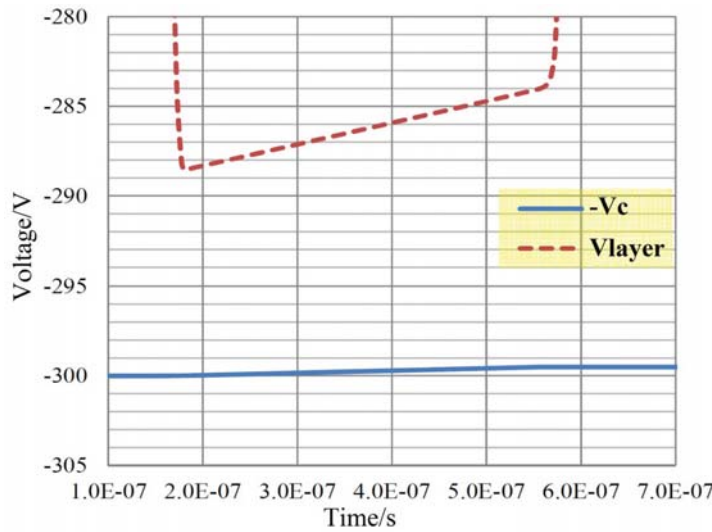


Figure 4.23. Simulated V_{layer} and voltage across a capacitor V_c of a simplified layer of an inductive adder.

Figure 4.23 shows a simulated output waveform for the circuit shown in Fig. 4.22. The capacitor was initially charged to 300 V. In this simulation, capacitance per layer C_s was $24 \mu\text{F}$, the magnetising inductance L_m was $10 \mu\text{H}$, load resistance per layer R_{load}/N was 10Ω , and switch on-state resistance included in R_{sw} , was 0.34Ω . These parameters correspond to

the simulations which were carried out for Fig. 4.21. A switch with negligible on-state resistance, in series with C_s , is not shown in Fig. 4.22. This switch was turned on to excite the resonance and it was turned off to limit the pulse flat-top duration to 350 ns. The primary resistance R_p , shown in Fig. 4.31, also affects the droop and its value was modelled as 50 m Ω and was included in R_{sw} to give a total resistance of 0.39 Ω for R_{sw} in this simulation. In Fig. 4.23, the capacitor voltage drops during the pulse flat-top by only 0.45 V, which is even less than would be expected from Eq. (4.4). One reason for this is that the load current is slightly smaller than the initial capacitor voltage divided by the effective load resistance per layer and the rise time is less than 100 ns.

The load current is defined by the sum of voltages, which are induced by the primary circuits to the secondary of an inductive adder. The magnetising current through L_m increases to 9.8 A during the pulse flat-top, which causes the voltage across R_{sw} to increase by 3.77 V during the flat-top. Thus the total voltage droop across the output of the layer is 4.22 V during the 350 ns flat-top. Scaling this up to five layers (21.1 V), this is in agreement with the predictions shown in Fig. 4.21.

The above clearly demonstrates that the resistance of the semiconductor switches and the resistance of the primary loop, together with the change in magnetising inductance current during the pulse flat-top, must be taken into consideration when estimating the droop of the output pulse of an inductive adder. In addition, increasing the capacitance per layer reduces only the droop which is caused by the storage capacitors, and does not compensate the change in voltage drop across the switch on-state resistance. This change in voltage drop can be limited, for example, by decreasing the on-state resistance of the switches e.g. by using silicone carbide MOSFETs or by connecting several switches in parallel, or by increasing the value of the magnetising inductance to reduce the increase in magnetising current. Analogue modulation of the output waveform is another effective method, which compensates the droop of the output waveform regardless of whether it is caused by the voltage droop of the capacitors or the change in voltage drop across the resistance of the layer.

4.3.2 Settling Time of the Output Pulse as a Function of the Stripline Impedance

In Section 2.2.1, a list of possible contributors to the flat-top stability of a kicker system is given. One of these is the impedance matching of the

system, including the pulse modulator, cables and the striplines. Ideally, the complete system would be perfectly matched but this is very difficult in reality.

When the striplines are pulsed to equal magnitude but opposite polarity voltages, the characteristic impedance of the kicker is odd-mode [7]. The odd-mode characteristic impedance of the prototype kicker striplines, which are optimised to have the required field homogeneity for the CLIC DR extraction system, is $41\ \Omega$ [30]. When the stripline electrodes are not powered, the beam which passes between the electrodes sees the even-mode characteristic impedance, which is nominally $50\ \Omega$ for the CLIC DR extraction kicker striplines. The transmission lines and the terminating load will be matched to $50\ \Omega$ impedance and therefore, the odd-mode characteristic impedance of the striplines, which is seen by the pulse modulator, may not be matched to the terminating resistor and the modulator.

Mismatched impedance causes reflections, which make the settling time of the kicker current longer. The settling time is the time period after the rise time of the pulse which is needed to damp the oscillations of the pulse flat-top to within the specifications. The specifications and pulse definition for the CLIC DR kicker modulator are presented in detail in Section 2.2.2. Fig. 4.24 shows the PSpice simulation model which was used to study the effect of the stripline impedance upon the settling time of the output pulse. In this model, the inductive adder, the cable between the inductive adder and the stripline kicker, and the striplines have been modelled as lossless transmission lines. The adder, shown in Fig. 4.24 as T_{adder} and the cable, shown as T_{cable} , are ideally matched to the load, which has $50\ \Omega$ output impedance. For these simulations the output pulse of the inductive adder is modelled as being trapezoidal and was driven into the transmission line T_{adder} by a pulse source shown as V_s in Fig. 4.24. The stripline is shown in Fig. 4.24 as $T_{stripline}$. The inductive adder and coaxial cable to the striplines have a total modelled single way delay of 13 ns, and the striplines have a single way delay of 7 ns [29].

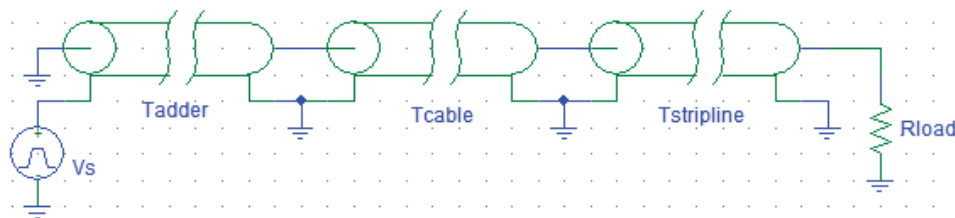


Figure 4.24. PSpice model for simulating effects of stripline odd-mode mismatch.

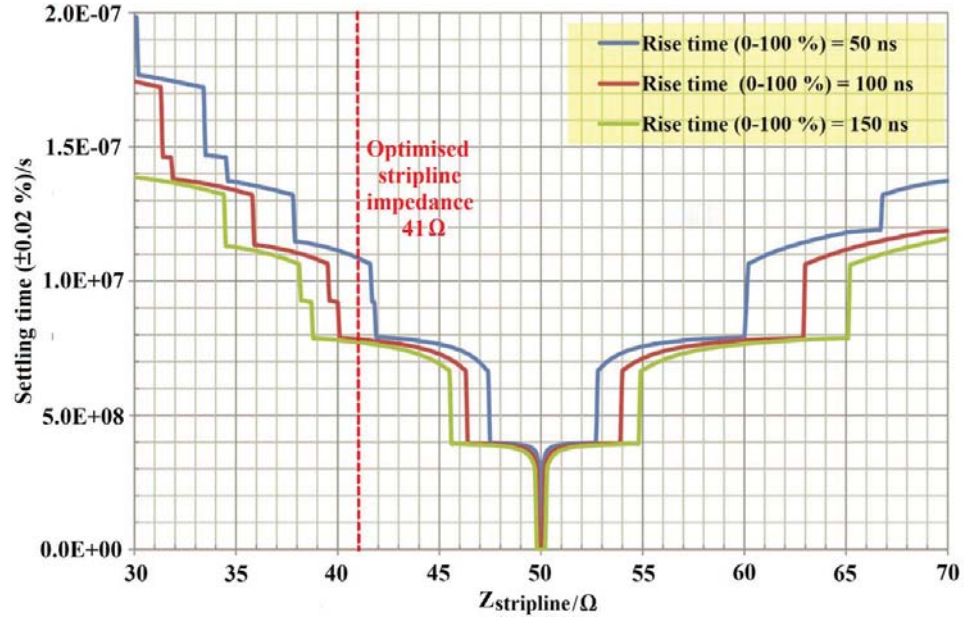


Figure 4.25. Settling time (to $\pm 0.02\%$) of the stripline voltage pulse as a function of stripline impedance with different pulse rise times T_r for an inductive adder. The impedance of the inductive adder, transmission line and terminating resistor was $50\ \Omega$.

Figure 4.25 shows the simulated settling times of the stripline kicker voltage as a function of stripline kicker impedance with different pulse rise times. The optimised odd-mode characteristic impedance of the prototype CLIC DR extraction kicker striplines is $41\ \Omega$ [30]. According to Fig. 4.25, with a characteristics odd-mode impedance of $41\ \Omega$, the settling time is approximately 77-110 ns longer than with matched $50\ \Omega$ stripline kicker impedance. The actual settling time depends on the rise time of the pulse and shorter rise times have longer settling times. These simulations have been done using models of lossless transmission lines. In reality, the losses of the transmission lines, striplines and the inductive adder may damp the reflections and hence shorten the predicted settling time.

4.3.3 Effect of the Output Impedance of the Inductive Adder upon the Settling Time of the Field of the CLIC DR Extraction Kicker

In Section 2.2, the goal rise time of the field of the striplines of the CLIC DR extraction kicker system was defined to be less than 250 ns. As discussed in the same section, the odd-mode impedance of the CLIC DR extraction kicker striplines is $41\ \Omega$ [30]. The load and the cables of the stripline kicker system have an impedance of $50\ \Omega$. The mismatched

impedance of the striplines causes reflections, which makes the settling time of the kicker current longer. The effect of the output impedance of an inductive adder upon the settling time of the stripline kicker voltage was studied with PSpice simulation code [139]. The simulation model was similar to the model which was used in Section 4.3.2 for simulations of settling time of the output pulse as function of stripline impedance, shown in Fig. 4.24.

Figure 4.26 shows the simulated settling times of the stripline kicker voltage as a function of the output impedance of an inductive adder with different pulse rise times. The settling time was calculated in the range of $35\ \Omega$ to $65\ \Omega$ from the time when the kicker voltage has reached 99.98 % of the flat-top voltage, to the time when the variations of the flat-top settled below $\pm 0.02\%$. In these simulations, the output pulse of the inductive adder has been modelled as being trapezoidal. The inductive adder, shown as T_{adder} in Fig. 4.24, has a total single way delay of 9.6 ns and the coaxial cable from the inductive adder to the stripline, shown as T_{cable} , has a total single way delay of 3.4 ns. The stripline, shown as $T_{stripline}$ in Fig. 4.24, has a single way delay of 7 ns [29]. The simulations were done using models of lossless transmission lines. In reality, the losses of the transmission lines, striplines and the inductive adder may damp the reflections, which may shorten the settling time. Furthermore, the transit time of the pulse through the striplines will tend to filter out the effect of small magnitudes of high-frequency ripple upon the field. Thus, the following gives only an approximation of the rise time of the stripline fields, but it is useful to demonstrate the importance of the output impedance.

Figure 4.26 shows the settling time of the stripline kicker voltage as a function of the output impedance for an inductive adder, with 25 ns steps of the rise time from 50 ns to 150 ns. The simulation results show that when the striplines are mismatched to the load, transmission lines and the output impedance of the inductive adder, the output impedance has a certain range, around $50\ \Omega$, within which it has almost no effect on the settling time. If the output impedance is in this range and the rise times of the output pulse of an inductive adder are from 75 ns to 150 ns, the settling time of the kicker voltage also remains very close to the minimum settling time.

It can be seen in Fig. 4.26 that with a rise time of 150 ns, the output impedance of $48.7 \pm 7.0\ \Omega$ gives a settling time of 77 ± 1 ns. Within this range of the output impedance, the sum of the rise and settling times is

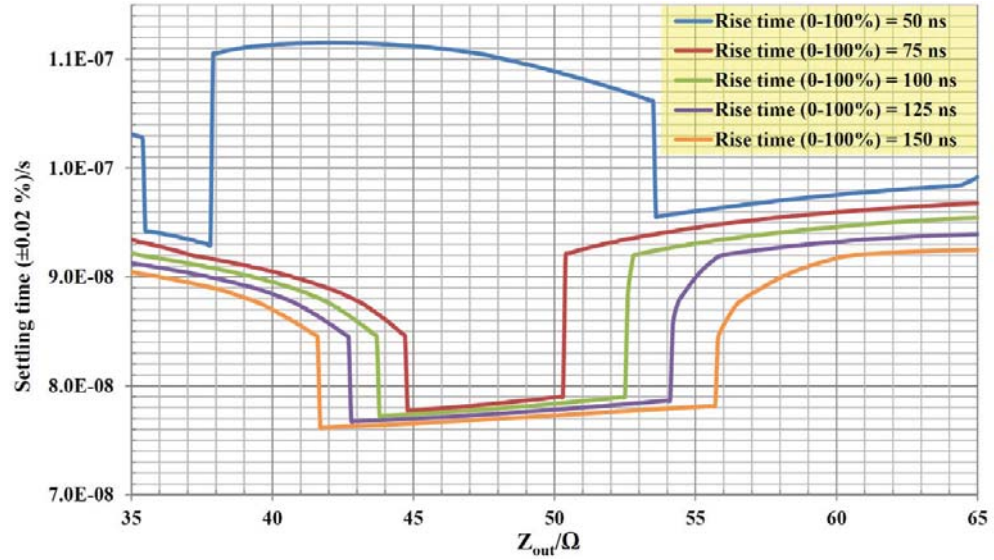


Figure 4.26. Settling time (to $\pm 0.02\%$) of the stripline voltage as a function of the output impedance of an inductive adder with different pulse rise times T_r with stripline impedance of $41\ \Omega$. The impedance of the transmission line and the terminating resistor is $50\ \Omega$.

227 ± 1 ns. The maximum settling time for 150 ns rise time is 92.5 ns, which is given by the $65\ \Omega$ output impedance. The sum of the rise time and the maximum settling time is 242.5 ns, which is close to the maximum goal value for the field rise time of the kicker, 250 ns.

According to Fig. 4.26, with the rise times of 125 ns and 100 ns, the sum of rise and settling times is considerably less than 250 ns for the full range of simulated output impedance values. The maximum settling times for 125 ns and 100 ns rise times are 94 ns and 95.5 ns, respectively, and they are predicted for the $65\ \Omega$ output impedance. The corresponding sums of the rise and settling times are 229 and 195.5 ns. Also for 125 ns and 100 ns rise times, there is a range of the output impedance within which the settling time changes slowly as a function of the output impedance. With a rise time of 125 ns, the output impedance of $48.4 \pm 5.6\ \Omega$ gives a settling time of 77.5 ± 1 ns, and with rise time of 100 ns, the output impedance of $48.1 \pm 4.3\ \Omega$ gives a settling time of 78 ± 1 ns.

For a 75 ns rise time, the output impedance of $47.6 \pm 2.7\ \Omega$ gives the settling time of 78.5 ± 0.5 ns, and the sum of the rise and settling times is 153.5 ± 0.5 ns. If the output impedance is less than $44.8\ \Omega$ or more than $50.3\ \Omega$, the settling time increases stepwise to 85 ns or 92 ns, respectively. At the limits of the simulation range of the output impedance, $35\ \Omega$ and $65\ \Omega$, the settling times are 93 ns and 97 ns, respectively. The longest combined rise and settling time, with a 75 ns rise time, is 172 ns with a

65 Ω output impedance.

With a 50 ns rise time, the output impedance from 35.5 Ω to 37.8 Ω gives the settling time from 93.5 ± 0.5 ns. This is the shortest value predicted with a 50 ns rise time and it results in the sum of the rise and settling time of 143.5 ± 0.5 ns. With the output impedance of an inductive adder between 53.6 Ω and 65 Ω , the settling time is between 95.5 ns and 99 ns, and between 38 Ω and 53.5 Ω , the settling time is between 106 ns and 111.5 ns. The settling time is 108.8 ± 2.7 ns with the output impedance of 45.7 ± 7.8 Ω . The longest combined rise and settling time for a 50 ns rise time is 161.5 ns with 42 Ω of output impedance.

The simulations results presented in Fig. 4.26 show that in the case in which the impedance of the striplines is not matched to the transmission lines and the terminating loads of the kicker system, the optimal output impedance of the inductive adder, which gives the shortest settling time for the stripline fields, depends on the rise time of its output pulse. In each settling time curve shown in in Fig. 4.26, corresponding to rise times from 50 to 150 ns, there is a relatively flat section, in which the settling time changes by 1-2 ns, whereas the output impedance changes by 5.5-15 Ω , depending on the rise time. To give an example, with the output rise time of 75 ns, a nominal output impedance of 47.6 Ω of the inductive adder gives at least ± 2.6 Ω (± 5.2 %) margin for the deviation of the actual output impedance, which does not affect the settling time by more than ± 0.5 ns. According to simulation results shown in in Fig. 4.26, if the rise time of the output pulse of the inductive adder is 150 ns or less, the output impedance of the inductive adder of 50 ± 15 Ω results in actual rise and settling time of the stripline voltage which is less than 250 ns. On the other hand, for all rise times simulated, the settling time is not very sensitive to the deviation of the output impedance of the inductive adder in the range of 45 Ω to 50 Ω .

This study shows that precise matching of the output impedance of the inductive adder to the transmission lines and the load is not crucial for the CLIC DR kicker system. The differences between the shortest settling times, given by the optimal output impedance for each rise time, and the longest settling times, given by the output impedance which deviates from the optimal output impedance in the simulated range, are relatively short in comparison with the sum of the rise and settling times. However in different system designs, in which transmission lines, loads and other parts of the system are well matched, the output impedance of the inductive

adder needs to be well matched in order to minimise the settling time.

4.3.4 Simulation Study on a Time Variant Load

The voltage pulse which is generated by the inductive adder is fed into a stripline kicker and finally absorbed by a terminating resistor. With the 900 ns of flat-top pulse, 100 ns rise and fall times, 50 Hz repetition rate and 12.5 kV voltage across a 50 Ω load, the average power for the terminating resistor will be 156 W. The beam passes the kicker in each turn in the damping ring, and this causes an image current to flow in the striplines. Therefore, the impedance of the load is seen by the beam which will further increase the dissipation in the load. In order to avoid perturbations to the beam, the kicker and the load need to be high bandwidth. The resistance of the terminating load may change during the pulse because of both heating of the load and due to voltage dependence of the load. The manufacturing specification for the impedance of a high-voltage, high-bandwidth 50 Ω terminating load is rarely better than $\pm 1\%$ [142].

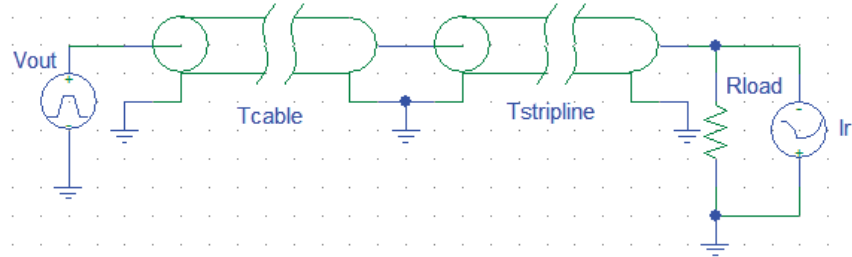


Figure 4.27. PSpice model for simulating effects of time variant load.

The effect of a time-varying load was studied by simulating either a linear or an exponential change for the load resistance. The initial results were published by the author in [14]. The output pulse of the inductive adder was simulated as a controlled voltage source V_{out} . The single-way delay of the inductive adder, the coaxial cables to the striplines and the odd mode impedance of a stripline electrode are modelled as ideal transmission lines T_{cable} and $T_{stripline}$, as shown in Fig. 4.27. The time variant load was implemented by terminating resistor R_{load} and a parallel controlled current source I_r .

Figures 4.28 and 4.29 show the simulated responses of the load voltages for linear and exponential changes of the load resistance, respectively. In both simulations, the nominal 50 Ω load resistance was varied by $\pm 1\%$, from 49.5 Ω to 50.5 Ω during the flat-top pulse. Figures show source voltage V_s , load resistance R_{load} , load voltage V_{load} and load current I_{load} . All

these quantities are normalised. The normalised sum of the load voltage and the load current, $(V_{\text{load}} + I_{\text{load}})/2$, the physical meaning of which is explained in the following paragraphs, is also shown in Fig. 4.28 and 4.29.

Figure 4.28 shows that the effect of the linear change of the load resistance causes a response for the load voltage which is of transient nature. After the 2-way delays of the transmission line and the stripline electrode, in total 40 ns, the pulse voltage remains constant for the duration of linear change of resistance. In Fig. 4.28, the amplitude of the flat-top voltage during the linear change of the load resistance is higher than during the time when the load resistance is not changing. The magnitude of the flat-top voltage during the linear change could be set by changing the charging voltage of the storage capacitors.

However, in Fig.4.28, the load current I_{load} decreases during the time when the load resistance changes. As discussed in Section 2.2.1, the electric and magnetic field of the stripline kicker deflect the beam ideally with the same amplitude. The magnetic field is linked to the current of the stripline and the electric field is linked to the voltages of the electrodes. Therefore, the normalised sum of the load voltage and the load current, $(V_{\text{load}} + I_{\text{load}})/2$, shown in Fig. 4.28 and Fig. 4.29, is proportional to the total deflection which is caused to the beam when it travels through the striplines. In Fig. 4.28, $(V_{\text{load}} + I_{\text{load}})/2$ decreases linearly, when the resistance of the terminating loads increases linearly. This indicates that the total deflection of the beam, caused by the stripline, also reduces linearly in the case of linear increase of the load resistance during the pulse. The reduction of the kick amplitude could be compensated by applying a linear change to the voltage of the electrodes. This would reduce the rate of change of the I_{load} during the pulse and would cause V_{load} to increase linearly during the pulse. Ideally, this would lead to a constant $(V_{\text{load}} + I_{\text{load}})/2$ during the pulse flat-top. The stripline voltage can be changed during the pulse by applying active analogue modulation for the output voltage of the inductive adders.

Figure 4.29 shows that the exponential change of the load resistance causes distortion of both the voltage and current of the striplines. The deflection of the beam is proportional to both the electric and magnetic field and for a $50\ \Omega$ system the contributions from these two components are equal. When the rate of change of the load resistance approaches a constant asymptotic value, the response of the load voltage approaches

the linear case, in which the load voltage remains constant while the load current decreases. The load current I_{load} decreases exponentially during the pulse as well as $(V_{\text{load}} + I_{\text{load}})/2$. The plots show that the kick of the stripline for the beam would also reduce exponentially during the pulse. Also in this case, the reduction of the total kick strength during the pulse could be compensated by applying active analogue modulation to the output pulses of the inductive adders. By increasing the stripline voltage during the pulse, the total deflecting effect, which is proportional to $(V_{\text{load}} + I_{\text{load}})/2$, could be kept constant during the pulse flat-top. In Chapter 5 it is experimentally shown how the active analogue modulation can be used to compensate both slow and fast changes of the output waveform of an inductive adder.

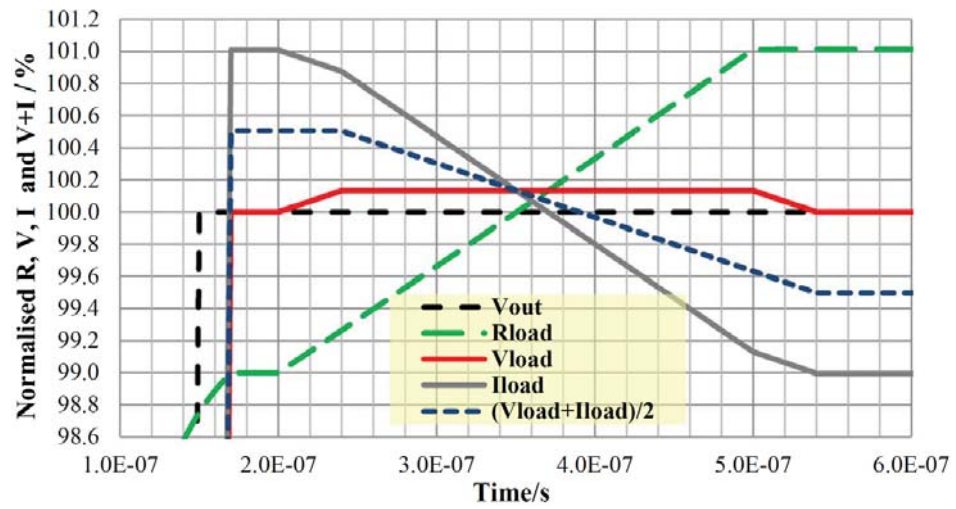


Figure 4.28. Kicker system response for a linearly time variant load resistance.

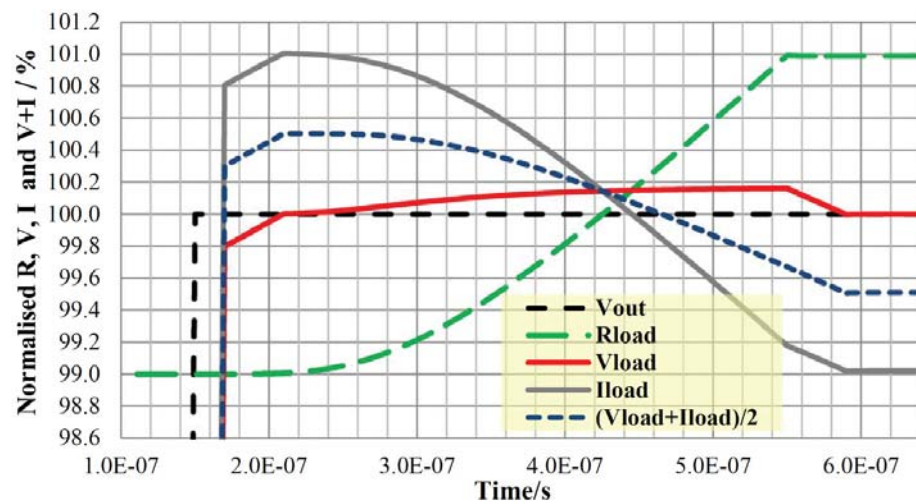


Figure 4.29. Kicker system response for an exponentially time variant load resistance.

4.4 Designing of the Inductive Adder with an Ideal Output Impedance

The output impedance of the inductive adder should ideally be matched to the load, in order to avoid reflections and therefore to achieve relatively short rise and settling times for the field of the stripline kicker. In Chapter 3, the following analytical equation is shown for the output impedance of the inductive adder [129]:

$$Z_{\text{out}} = \sqrt{\frac{L_{\text{pl}} + L_{\text{ss}}}{C_c}} \quad (4.8)$$

Figure 3.12 in Chapter 3 presents a simplified schematic of a single layer of the inductive adder together with the main parasitic circuit elements. Fig. 4.30 shows a cross-section of a single branch of a layer of an inductive adder with the main parasitic elements, namely secondary inductance L_{ss} , coupling capacitance C_c , and primary loop inductance L_{pl} , all referred to a single cell. The estimates for parameters L_{ss} and C_c can be computed analytically based on the dimensions of an inductive adder cell, as shown in Section 3.5. However, the parameter L_{pl} cannot be computed easily analytically. This parameter has a significant effect on the output impedance, as it was emphasised in Section 3.5.3. Therefore, an accurate estimate of this parameter is essential for designing an inductive adder with the desired output impedance.

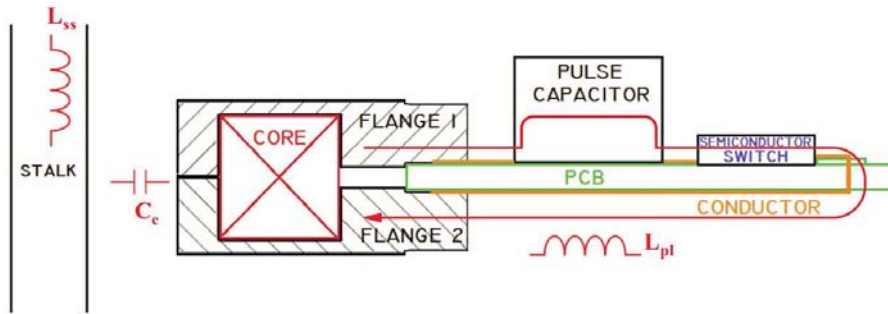


Figure 4.30. Simplified cross-section of a single cell of an inductive adder with the main parasitic elements, L_{ss} , C_c and L_{ks} , which refers to the parameters of a single cell.

4.4.1 Effect of the Primary Loop Inductance for the Transient Response of an Inductive Adder

The output impedance of the inductive adder depends upon the primary loop inductance L_{pl} , the secondary inductance L_{ss} and the coupling capacitance C_c . The values of the secondary parameters depend on inner diameter of the housing of the magnetic core, the outside diameter of the secondary stalk, and the insulation material between the primary and the stalk. For a given primary loop inductance L_{pl} , which depends on the design and components of the primary circuit, the output impedance of the inductive adder can be adjusted by changing the outside diameter of the secondary stalk. However, the transient behaviour of the inductive adder also depends on the propagation delay through the adder stack, which influences the settling time of the output pulse.

An equivalent circuit of the inductive adder was developed and simulated using PSpice software [139]. The simplified equivalent circuit of a single layer of the inductive adder, which is derived from the model shown in [129], is presented in Fig. 4.31. The complete model consists of 18 identical layers, each of which includes storage capacitor C_s , primary loop inductance L_{pl} , magnetising inductance L_m , secondary inductance L_{ss} , coupling capacitance C_c , primary resistance R_p and switches. The parasitic electrical parameters of the simulation model are based on the physical dimensions of the adder stack, as presented in [104], and the preliminary design parameters for the CLIC damping ring inductive adder have been shown in [9]. The semiconductor switches were modelled as almost ideal switches, i.e. fast switch-on and low loss. The transit times of the switches were set to 10 ns in PSpice. According to simulations, this transit time for a closing switch from high impedance, open mode, of a switch to low impedance, closed mode, effectively corresponds to 6.1 ns switching time from 99.9 % to 0.1 % of the voltage across the switch and 1.3 ns switching time from 90 % to 10 % of the voltage across the switch. Extremely fast switching times were simulated in order that the modelled inductances and capacitances mainly influenced the rise time. Snubber and diode clamping circuits were not included in the model.

In the beginning of the analysis, a nominal value of 20 nH was assumed for L_{pl} and the values of L_{ss} and C_c were calculated from the equations shown in [128], to obtain an output impedance of 50 Ω . The value of L_{pl} was then changed by ± 6 nH (± 30 %) and the values of L_{ss} and C_c were

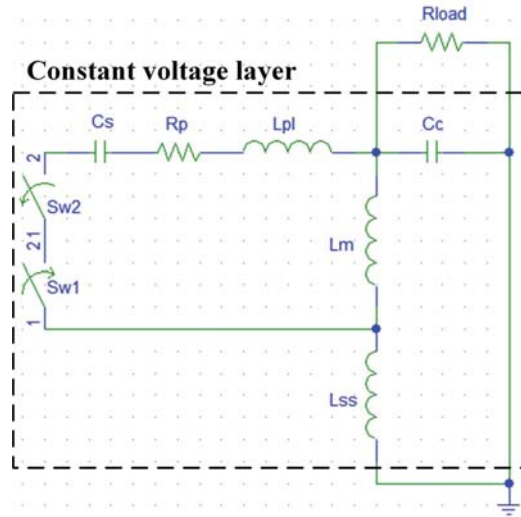


Figure 4.31. Equivalent circuit of a layer of an inductive adder without a transformer and with a load.

recalculated, by effectively changing the diameter of the stalk, so that the output impedance remained at $50\ \Omega$. The insulation material between the primary and secondary windings was assumed to be polyethylene with a relative permittivity of 2.3. Table 4.3 shows the parameters for the sensitivity analysis and two way propagation delay $T_{rd,2w}$, given by Eq. (3.27), for each set of parameters.

Table 4.3. Parameters for sensitivity analysis ($Z_{out} = 50\ \Omega$).

L_{pl} (nH)	14	20	26
C_c (pF)	8.71	10.8	12.9
L_{ss} (nH)	7.85	6.94	6.32
C_s (μ F)	320	320	320
L_m (μ H)	20	20	20
R_p (m Ω)	6	6	6
$T_{rd,2w}$ (ns)	15.7	19.4	23.2

Figure 4.32 shows the predicted output voltage of an 18-layer inductive adder for the three sets of parameter values shown in Table 4.3. The output of the adder is in all cases matched to the load, which is an ideal $50\ \Omega$ resistor. The different values of the secondary inductance, coupling capacitance and primary loop inductance affect the rise time and settling time of the pulse. Table 4.4 shows the rise time of the load voltage from 10 % to 90 %, indicated as $T_{r,10-90}$, the rise time from 0.02 % to 99.98 %, indicated

as $T_{r,0.02-99.98}$, the settling time of the flat-top voltage to $\pm 0.02\%$, $T_{s,\pm 0.02}$, and the sum of $T_{r,0.02-99.98}$ and $T_{s,\pm 0.02}$.

The two way propagation delay $T_{rd,2w}$ can be considered as the minimum estimate for the rise time of the output pulse [69]. The computed values of $T_{rd,2w}$ for the output pulse of an 18-layer inductive adder stack are 15.7 ns for L_{pl} of 14 nH, 19.4 ns for L_{pl} of 20 nH and 23.2 ns for L_{pl} of 26 nH, as shown in Table 4.3. In the simulations, the rise times of the output voltage from 10 % to 90 %, $T_{r,10-90}$, for L_{pl} of 14 nH, 20 nH and 26 nH were 20.8 ns, 22.8 ns and 24.9 ns, respectively, as is shown in Table 4.4. These values are 5.1, 3.4 and 1.7 ns longer than the estimates given by Eq. (3.27) for $T_{rd,2w}$.

When L_{pl} is its nominal value, 20 nH, the rise time from 0.02 % to 99.98 % of the load voltage, $T_{r,0.02-99.98}$, is 59.3 ns. The settling time of the load voltage to $\pm 0.02\%$, $T_{s,\pm 0.02}$, is 14.1 ns and the sum of $T_{r,0.02-99.98}$ and $T_{s,\pm 0.02}$ 73.4 ns. When the parameter L_{pl} is reduced by 30 % to 14 nH, $T_{r,0.02-99.98}$ is decreased by 0.2 ns and $T_{s,\pm 0.02}$ by 5.2 ns. On the other hand, a 30 % increase of parameter L_{pl} lengthens the rise time from 0.02 % to 99.98 % of the load voltage by 2.3 ns and settling time by 5.4 ns. The difference between the minimum and the maximum of the sum of the rise and settling times, $T_{r,0.02-99.98}$ and $T_{s,\pm 0.02}$, of these simulations is 13.1 ns.

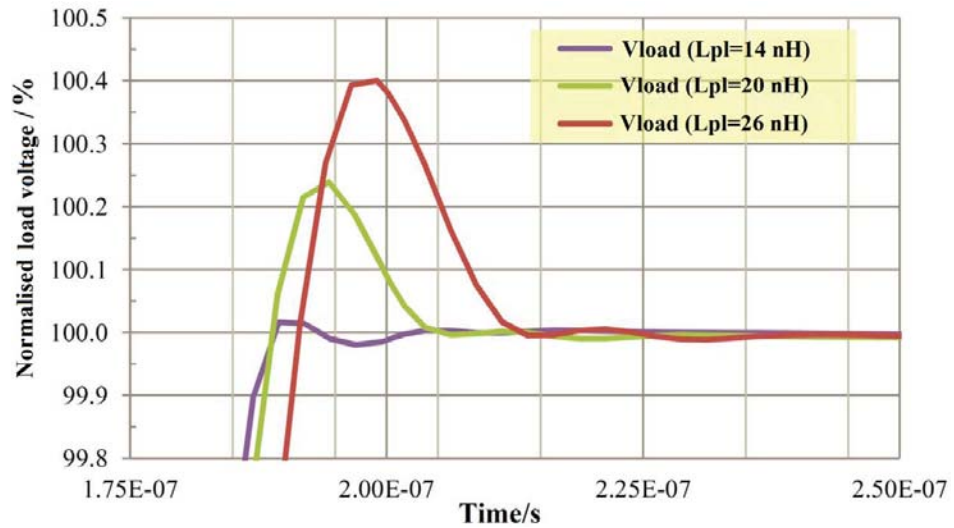


Figure 4.32. Output voltage of an 18-layer inductive adder with three different sets of parameters.

These simulation results show that accurate modelling of the primary loop inductance is important for designing an inductive adder with the desired transient behaviour. The output impedance can be matched to the load by modifying the diameter of the secondary stalk but the settling

Table 4.4. Predictions from sensitivity analysis ($Z_{\text{out}} = 50 \Omega$).

L_{pl} (nH)	14	20	26
$T_{\text{r},10-90}$ (ns)	20.8	22.8	24.9
$T_{\text{r},0.02-99.98}$ (ns)	59.1	59.3	61.6
$T_{\text{s},\pm 0.02}$ (ns)	8.9	14.1	19.5
$T_{\text{r},0.02-99.98} + T_{\text{s},\pm 0.02}$ (ns)	68.0	73.4	81.1

time is minimised by minimising the primary loop inductance. Hence, an accurate prediction of the primary loop inductance is necessary to minimise the true primary loop inductance and hence the rise and settling times.

4.4.2 Modelling of the Primary Loop Inductance of an Inductive Adder

The author presented in [15] and [16] an approach to estimate the primary loop inductance using FastHenry simulation code [140]. This modelling study has been continued and the updated results are presented here. FastHenry software applies a partial element equivalent circuit approach to solve numerically the inductances and resistances of a modelled structure. The solution is derived from magneto-quasistatic Maxwell equations, which neglects capacitive effects and delays. FastHenry generates an equivalent circuit of the modelled structure as a mesh of filaments and uses an iterative multipole-accelerated algorithm to find the solution for the problem [143].

In the electrical design of an inductive adder, presented in Chapter 3, the current loops of the primary circuit consist of two different sections. The first section is the current path on a PCB, which includes the storage capacitor, semiconductor switch and tracks on the PCB up until the flanges, as shown in Fig. 4.30. Usually, a single layer of an inductive adder has several current branches in parallel. If the mutual inductances between the current branches are neglected, the primary loop inductance for the first section for a single branch is approximately the inductance of a single branch on a PCB divided by the number of parallel loops. This section of the primary loop inductance has been modelled using FastHenry simulation code [140]. The same software has also been used to determine whether the mutual coupling between parallel branches is significant.

The second section of the primary loop inductance is the current path from the contact point between the top surface of the PCB and a top flange, shown as flange 1 in Fig. 4.30, along the flanges to the contact point between a bottom flange, shown as flange 2 in Fig. 4.30, and the bottom surface of the PCB. The inductance of this current path was also estimated with the FastHenry simulation code.

A 3D Model of the Inductance of the PCBs

Figure 4.33 shows the FastHenry model of a single current branch of the primary circuit of a single layer of an inductive adder. The current loop includes a simple model of a pulse capacitor NWL T00216 [131], a semiconductor switch with a TO-264 package [101] and the tracks and vias of the PCB. The physical dimensions of the model are based on the data sheets of the components and dimensions of the first prototype inductive adder built at CERN, which is presented in Chapter 5.

The large NWL pulse capacitor of the primary circuit was modelled as a current loop, the height of which was approximately a half of the physical height of the capacitor, and the width two millimetres less than the physical width of the capacitor. The dimensions of the model were trimmed to match the estimated inductance of the pulse capacitor to the measured inductance of the pulse capacitor, which was presented by the author in [13].

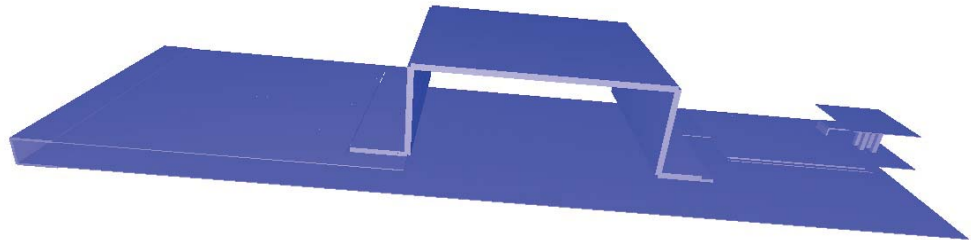


Figure 4.33. A FastHenry model of a single current branch of a layer of the inductive adder of the PCBs and components up until the flanges.

The predicted self-inductance of a single primary loop ($L_{pl,1br}$) is 37.2 nH. As a first approximation it was assumed that the total primary loop inductance of a single layer can be calculated by dividing the single loop inductance by the number of the parallel current branches, i.e. mutual inductance between parallel primary loops of a layer is assumed to be negligible, because the cross-sectional area of the loops is small, the width of the conductors is generally quite large, and the spacing of adjacent loops is relatively large. This assumption was verified to be correct with

a simulation using the FastHenry code. In the CERN prototype inductive adders, presented in Chapter 5, the nominal number of the loops per layer is eight. The mutual inductance between two adjacent current loops, in the case when there were eight current branches per layer with a 45 degree angle between the adjacent current loops, was less than 0.1 nH. The mutual inductance between vertically adjacent current branches of two stacked PCBs was also studied and it was also less than 0.1 nH. Neglecting the mutual inductances, the predicted primary loop inductance for the PCB section of a single layer is 4.65 nH.

A 3D Model of the Inductance of the Flanges

The second section of the primary loop inductance consists of the current path from the contact point between the top surface of the PCB and a top flange, shown as flange 1 in Fig. 4.30, to the contact point between a bottom flange, shown as flange 2 in Fig. 4.30, and the bottom surface of the PCB. The inductance of this current path was also estimated with the FastHenry simulation code [140]. Fig. 4.34 shows a figure of the simulation model of the flanges. Although the flange is round, this geometry was not feasible to model with FastHenry and instead the flange is modelled as an octagon where each section of the octagon is a single current path. The physical dimensions of the model are based on dimensions of the first prototype inductive adder built at CERN, which is presented in Chapter 5. The sliding contacts between the PCB and the flanges were not included in the simulation model.

The total primary loop inductance of a single current path was thus predicted with a FastHenry model, which included a single current loop of the half-layer PCB and the simulation model of the flanges. The prediction for the total primary loop inductance of a single current path is 42.4 nH, which gives the total primary loop inductance of 5.3 nH for eight parallel current paths.

Measurements on the Primary Loop Inductance

The prediction for the primary loop inductance of an inductive adder was verified by measuring the inductance of a single current branch of a prototype inductive adder built at CERN. The experimental method to measure the inductance of the primary circuit of an inductive adder was presented by the author in [15] and the method is similar to that presented by the author in [13] for defining the inductance of the pulse capacitors. The method is based on measuring the frequency of the voltage of the reso-

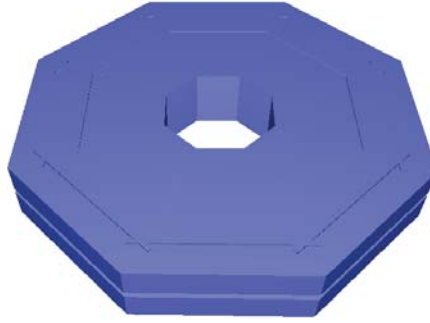


Figure 4.34. A FastHenry model of the bottom and top flanges of a layer of the inductive adder.

nant circuit, which is formed by the primary branch. Fig. 4.35 shows a simplified model of the resonant circuit.

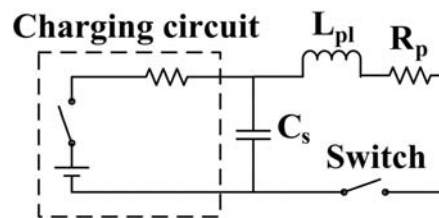


Figure 4.35. A simplified lumped element model of the resonant circuit formed by a primary branch of an inductive adder.

Figure 4.36 shows photographs of a PCB, which is a half of a single layer of the inductive adder. The copper sheet, which is attached close to a large black pulse capacitor, replaces the semiconductor switch to permit the measurement of the primary loop inductance of a single branch. Another thin piece of copper was soldered on the driver board, which is labelled as "switch" in the upper figure. This was used as a switch to trigger the resonant circuit. At first, the primary loop inductance was measured for the primary branch without flanges. The top contact surface, which is visible in Fig. 4.36 as a golden coloured arc at the edge of the PCB, was connected to the bottom contact surface, which is located in the same position but on the other side of the PCB, by soldering a sheet of copper between them. This copper conductor is labelled as "short-circuit" in both photos in Fig. 4.36. The width of this copper conductor was the same as the width of the PCB tracks on the top and bottom surfaces of the PCB.

The measured value for the primary loop inductance of a primary branch without flanges was 39.3 nH. This value is an average of 10 measurements, the standard deviation of which was 0.3 nH. The average of the measurements is 2.1 nH (+5.6 %) higher than the prediction given by the

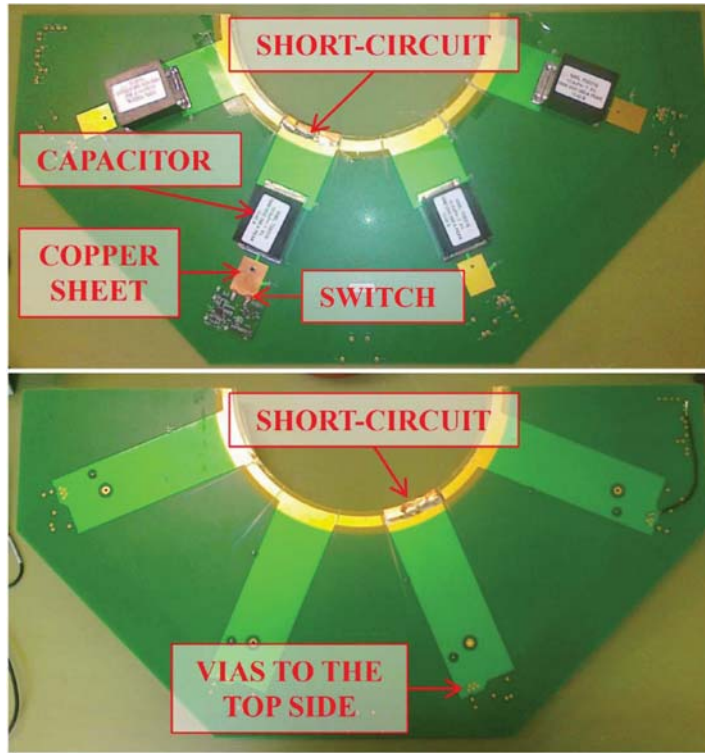


Figure 4.36. A half-layer PCB of the prototype inductive adder at CERN from the top side (upper) and the bottom side (lower).

simulation studies, presented in the previous section of this dissertation.

The total primary loop inductance, including both the PCB section and the flange section, was also measured using the same approach as for the PCB part of the primary. In this measurement, the PCB was inserted into a slot between a top flange and a bottom flange, which were attached together. The magnetic core was not assembled into the core hollow between the flanges, in order to measure the inductance of the primary branch without magnetising inductance. This measurement gave the total primary loop inductance including both the PCB section and the current path along the flanges.

The measured value for the total primary loop inductance was 47.6 nH, which is an average for 10 measurements, the standard deviation of which was 0.8 nH. The predicted value of the total primary loop inductance for a single branch is 5.2 nH (−10.9 %) less than the average of the measured values. The prediction of the primary loop inductance of a primary branch in a PCB differs from the measured value by 2.1 nH, therefore it is assumed that the flange model increases the error by 3.1 nH. One reason for this difference may be the sliding contacts between the flanges and the contact surfaces of the PCBs, which were not implemented in the simulation model.

However, as shown in Fig. 4.36, the half-layer PCB of the prototype inductive adder built at CERN includes four current branches and the single layer consists of eight parallel branches. By neglecting the mutual inductances between adjacent current branches, the total primary loop inductance per layer would be 47.6 nH divided by eight, which gives 5.95 nH. The prediction given by simulation studies would result in 5.3 nH of total primary loop inductance per layer. The difference between these values is only 0.65 nH and the effect of this error is evaluated in the next section of this dissertation.

4.4.3 Effect of the Discrepancies of the Stack Parameters Upon the Output Impedance

The measured value of the primary loop inductance for a single layer is higher than the predicted value by 0.65 nH. The effect of this difference can be estimated by using the design method shown in Section 3.5.4 and the preliminary design dimensions of the CLIC DR kicker inductive adder, shown in Table 3.3. At first, the total primary loop inductance is expected to be the prediction given by the simulation, 5.3 nH per layer. The dimensions of an inductive adder cell are defined using this value for the total primary inductance, to give an output impedance of 50 Ω . The inside diameter of the core housing, D_1 , and the height of the cell, l_p , are kept constant, 66 mm and 45 mm, respectively, as given in Table 3.3. The diameter of the stalk, d , is changed to give the desired output impedance and the corresponding values for coupling capacitance C_c and secondary inductance L_{ss} have been computed. Then, the predicted value for the total primary loop inductance per layer is replaced by the measured value, 5.95 nH, which causes the output impedance to increase. The difference of the output impedance values, computed with a predicted or measured values for the primary loop inductance, shows how much the difference between the predicted and measured values effects the output impedance.

Using the dimensions of an adder cell of the CLIC DR kicker prototype inductive adders in Table 3.3, the predicted primary loop inductance of 5.30 nH requires a secondary with outside diameter of 36.6 mm in order to obtain a 50 Ω output impedance. When the primary loop value is changed to the measured value of 5.95 nH, the same dimensions for the cell and stalk would result in the output impedance of 51.5 Ω (+3.0 %). In the case of an epoxy-insulated adder stack, presented in Table 3.3 for the CLIC DR kicker inductive adder, the diameter of the stalk which is required

in order to get a $50\ \Omega$ output impedance in the case of predicted 5.3 nH primary loop inductance, is 13.9 mm. The measured value of the primary loop inductance, 5.95 nH, results in $50.9\ \Omega$ (+1.8 %) output impedance.

The other parameters which effect the output impedance are the secondary inductance L_{ss} and the coupling capacitance C_c . The author published in [15] and [16] the analytical values and measured values for these parameters for a 5-layer prototype inductive adder stack built at CERN. For the coupling capacitance C_c , the difference between the calculated (6.2 pF per layer) and measured (7.0 pF per layer) value was +12.9 %, and for the secondary inductance, the difference between the calculated (6.3 nH per layer) and measured (6.6 nH per layer) value was +4.5 %. The analytical equations for estimating the coupling capacitance and the secondary inductance, Eq. (3.17) and Eq. (3.16), respectively, are valid for a coaxial structure with an infinite length, whereas the measured values include end-effects of the structure which increase the total capacitance and inductance. The same approach as in evaluation of the effect of the error of the estimate primary loop inductance has been applied for evaluating the effect of the difference of the analytical and measured values of parameters C_c and L_{ss} . In the case of an air-insulated inductive adder with the dimensions shown in Example 1 in Table 3.3, the 12.9 % error in the coupling capacitance decreases the impedance from $50\ \Omega$ to $47.0\ \Omega$ (−6.0 %), and the 4.5 % error in the loop inductance increases the output impedance from $50\ \Omega$ to $50.6\ \Omega$ (+1.2 %). The same error margins of parameters C_c and L_{ss} have also been applied to an epoxy filled inductive adder. The 12.9 % error in the coupling capacitance decreases the output impedance to $47.1\ \Omega$ (−5.8 %), and the 4.5 % error in the secondary inductance increases the output impedance to $50.9\ \Omega$ (+1.8 %).

Table 4.5 summaries all different combinations of an estimated and a measured primary loop inductance, the coupling capacitance and the secondary inductance with applied error margins, to compute the output impedance for an air-insulated inductive adder. According to Table 4.5, the nominally $50\ \Omega$ output impedance may be between $47.0\ \Omega$ (−6.0 %) and $52.1\ \Omega$ (+4.2 %). This gives an estimate for the range, within which the nominally $50\ \Omega$ output impedance of an air-insulated inductive adder will be, if it is designed according to design steps presented in Chapter 3. For comparison, the specification for the impedance of the commercial 18 kV high-voltage coaxial cable type HTC-50-7-2, which is used in pulse power systems at CERN, is $50\pm2\ \Omega$ [144].

The computations of the effects of the discrepancies of the stack parameters were also carried out for an epoxy filled inductive adder with the dimensions shown in Table 3.3. In this case, the different combinations of parameters give a range for the output impedance from 47.1Ω [-5.8 %] to 51.8Ω (+3.6 %). However as mentioned above, the error margins for the secondary inductance and coupling capacitances have been measured for an air-insulated prototype adder and they are not directly applicable for an epoxy-insulated adder.

Table 4.5. Evaluation of the effects of discrepancies of the design parameters for the output impedance of an air-insulated inductive adder. The precited value and the discrepancy is $5.30+0.65 \text{ nH}$ (+12.2 %) for L_{pl} , $4.25+0.55 \text{ pF}$ (+12.9 %) for C_c , and $5.31+0.26 \text{ nH}$ (+4.8 %) for L_{ss} .

L_{pl} (nH)	L_{ss} (nH)	C_c (pF)	Z_{out} (Ω)
5.30	5.31	4.25	50.0
5.95	5.31	4.25	51.5
5.30	5.57	4.25	50.6
5.95	5.57	4.25	52.1
5.30	5.31	4.80	47.0
5.95	5.31	4.80	48.5
5.30	5.57	4.80	47.6
5.95	5.57	4.80	49.0

Considering the design of an inductive adder for the CLIC DR kicker system the effect of the uncertainty of the output impedance has been evaluated for the settling time of the output waveform. Fig. 4.26 presents the settling time of the stripline voltage of the CLIC DR kicker system as a function of the output impedance of an inductive adder. The estimated output impedance range, from 47.0Ω to 52.1Ω as shown in Table 4.5, of a nominally 50Ω inductive adder, is compared to the settling time. If the nominal output impedance of the inductive adder is designed for 50Ω , the error margins of the output impedance may cause $\pm 0.5 \text{ ns}$ discrepancy for the settling time with pulse rise times from 100 to 150 ns, and $\pm 1.5 \text{ ns}$ with a 50 ns rise time. With a 75 ns rise time, the settling time may be either 78-79 ns or 92-93 ns, depending on the actual value of the output impedance, and in this case the discrepancy of the settling time is 15 ns. On the other hand, if the nominal output impedance is designed to be 47.5Ω and the error margins are assumed to be the same

percentages of the output impedance as in the case of $50\ \Omega$ nominal output impedance, the discrepancy of the settling times is $\pm 0.5\text{ ns}$ for the rise times from 75 to 150 ns, and $\pm 1.5\text{ ns}$ for a 50 ns rise time. Taking into account the sum of the rise and settling times and the total pulse length of the CLIC DR kicker inductive adder, the discrepancy of a few nanosecond for the settling time is negligible. However, it is advantageous to aim for a nominal output impedance of $47.5\ \Omega$, for striplines of $41\ \Omega$ characteristic impedance.

4.5 Compensation of the Droop and Ripple of the Output Waveform of an Inductive Adder

This section presents simulation studies on compensating the droop and ripple of the output waveform of an inductive adder. At first, the main contributors to the droop of the output pulse are discussed. Then, the simulation models which were used in this study are presented. Finally, the simulation results of applying both passive and active analogue modulation methods to compensate the droop are presented, as well as a step-by-step approach for active compensation of ripple. The simulation models presented in this section were analysed using PSpice simulation software [139].

4.5.1 Simulation Models for Studying Modulation Methods

The analogue modulation method, presented in Chapter 3.2.2, was studied with the simulation model of an inductive adder. The PSpice models of a constant voltage layer and an analogue modulation layer are shown in Fig. 4.37.

Both passive and active analogue modulation were studied. Simulations were carried out with a 5-layer inductive adder model, using the analogue modulation layer as a passive and an active compensator. The results of these simulations have been published previously by the author in [9], [10] and [17]. The main results are briefly repeated below.

4.5.2 Passive Analogue Modulation for Compensating the Droop

The circuit analysis showed that passive analogue modulation layer behaves as a resistor-inductor (RL) circuit. During the pulse, the current through resistor R_a , shown in Fig. 4.37, decreases as the current trans-

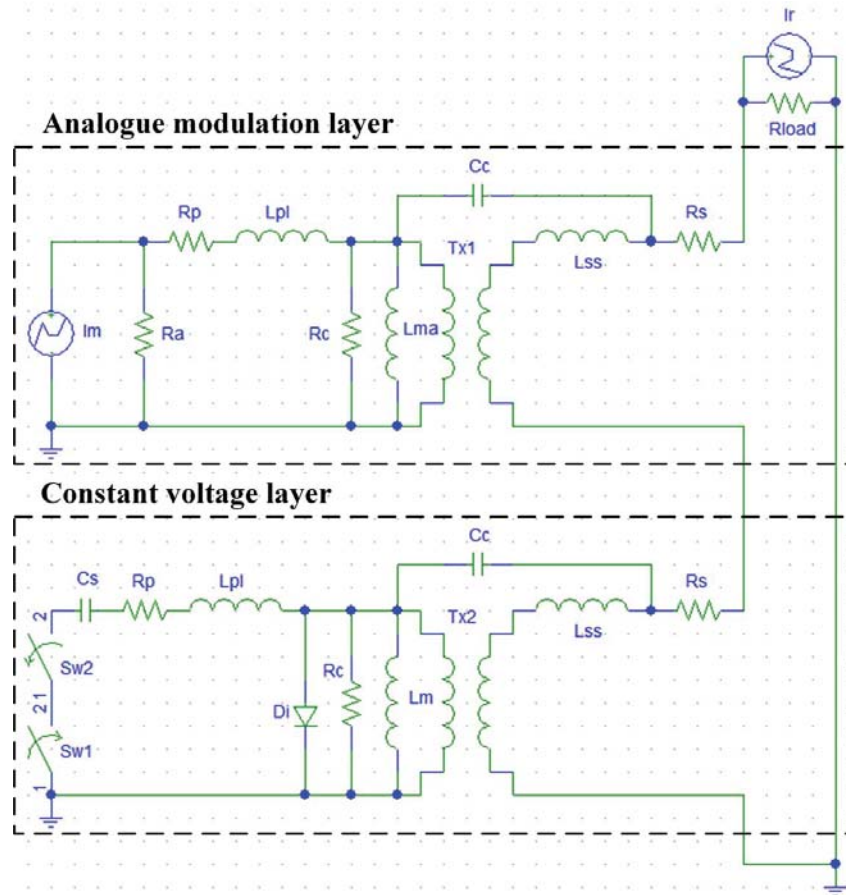


Figure 4.37. Equivalent circuit of an analogue modulation layer and a constant voltage layer of an inductive adder with a load. Current source I_r produces programmed ripple of load voltage and current.

fers into the magnetising inductance, which causes the voltage over the resistor R_a to decrease. The time constant of the RL circuit is defined by the ratio of the magnetising inductance of the transformer primary to the resistance R_a , and it can be selected to compensate both the voltage droop across the capacitors in the other layers and the change in voltage drop across the on-state resistance of the constant voltage layers. In reality, the magnetising inductance should be large enough to keep the magnetising current below 15 % of the load current [40] and R_a cannot be very large to avoid excessive power loss. Most of the load current flows through R_a and its resistance defines the voltage across the analogue modulation layer, and thus the cross-sectional area required for the magnetic core of this layer. According to simulations made for this dissertation, the resistance of R_a is typically less than 10 Ω .

Figure 4.38 shows the simulated output waveform for the inductive adder with four constant voltage layers and the primary of the fifth layer is short-circuited (labelled w/o AM). In the same figure, the output wave-

form is also shown for the adder stack with four constant voltage layers and with a passive analogue modulation layer with two different values of resistor R_a (labelled AM). The blue, dashed curve in Fig. 4.38 shows the simulated output waveform for an inductive adder without an analogue modulation layer. The pulse capacitors were initially charged to 270 V per layer. The other parameters of the model were the following: capacitance per layer C_s was 24 μF , the magnetising inductances L_m and L_{ma} were 10 μH , load resistance 50 Ω , and switch resistance R_{sw} was 0.34 Ω and primary resistance R_p was 50 m Ω . The core loss resistance R_c was neglected in these simulations.

For the model with one primary layer in short-circuit, the maximum output voltage is 1.020 kV and the duration of the pulse flat-top is 350 ns. The droop of the pulse flat-top is 14.8 V which corresponds to 1.5 % of the pulse voltage. The red, dashed curve in Fig. 4.38 shows the output waveform of an inductive adder with a passive analogue modulation layer with resistor R_a of 3.9 Ω . In this case, the voltage of the pulse capacitors was initially 280 V and the maximum output voltage is 1.003 kV. The droop of the pulse flat-top is 5.6 V, which corresponds to 0.6 % of the pulse voltage. This is less than a half of the droop which is seen in the output pulse if passive analogue modulation is not applied. The green, solid curve in Fig. 4.38 shows the output waveform of an inductive adder with a passive analogue modulation layer with resistor R_a of 5.0 Ω . The voltage of the pulse capacitors was initially 280 V and the maximum output voltage is 984 V. The pulse flat-top is slightly rounded and therefore does not show a clear droop. The difference of the minimum and the maximum values of the 350 ns duration pulse flat-top is 0.6 V, which corresponds to 0.06 % (i.e. ± 0.03 %) of the pulse voltage.

The simulation results show that the passive analogue modulation layer can be used to decrease the total droop, which is caused by the voltage droop of the storage capacitors, and by the resistive losses in the printed circuit board tracks and semiconductor switches in combination with increasing magnetising current in the constant voltage layers. In order to reach very low droop, it is necessary to apply analogue modulation, because increasing the capacitance per layer does not decrease the droop which is caused by the resistive losses. Potentially, by applying passive analogue modulation, the capacitance per layer can be reduced significantly without causing excessive droop in the load voltage, as was shown by the author in [9] and [10]. The drawback of passive analogue modu-

lation is that the load current flows through resistor R_a of the analogue modulation layer, which causes additional resistive losses. The compensating droop of the passive analogue method cannot be adjusted quickly, because it requires that the value of resistor R_a is changed. Also, the compensation effect of the analogue modulation layer depends on the sum of the voltages of the constant voltage layers, and therefore the modulation effect changes if the charging voltage of the constant voltage layers, or the load resistance, is changed.

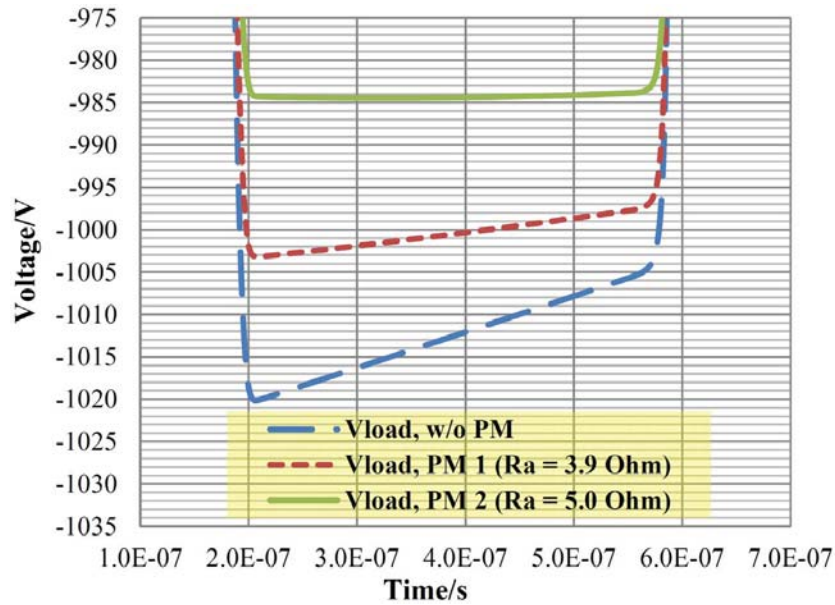


Figure 4.38. Simulated V_{load} with four constant voltage layers (blue, dashed), and with four constant voltage layers and a passive analogue modulation layer with $R_a = 3.9 \Omega$ (red, dashed) and $R_a = 5.0 \Omega$ (green, solid line).

The measurements of applying passive droop compensation for the output pulse of a prototype inductive adder are presented in Section 5.4.

4.5.3 Active Analogue Modulation for Compensating the Droop

In [73] measurements were reported in which active analogue modulation was applied to an inductive adder with a modulating frequency up to tens of MHz and the amplitude of the output waveform was modulated up to 10 % of the maximum pulse voltage. The accuracy of the amplitude modulation was not reported in reference [73] and the goal of that publication was obviously to demonstrate the bandwidth and amplitude range of the active analogue modulation method. Active droop and ripple compensations was not mentioned neither demonstrated in publication [73]. The modulation bandwidth is limited by the cut-off frequency of the inductor-

resistor (LR) type low-pass filter, which is formed by the inductance of the stack and the load resistor [73].

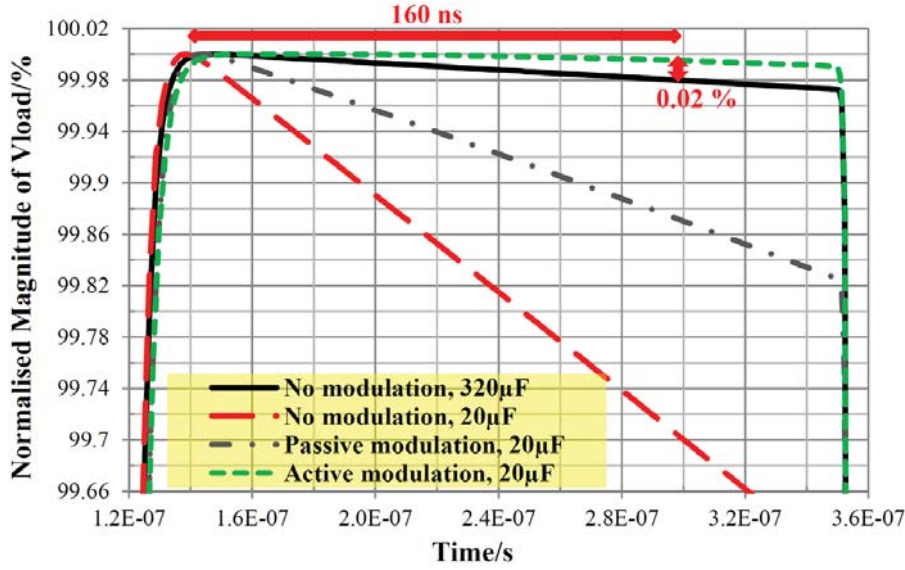


Figure 4.39. The simulated normalised load voltage of an inductive adder with different capacitor bank values with passive modulation, with active modulation and without modulation. $R_a = 1.2 \Omega$.

Simulations were carried out with a 5-layer inductive adder model, using various storage capacitance values and using the analogue modulation layer as a passive or an active compensator. The main results of these simulations have been published previously by the author in [10] and [9]. There were four constant voltage layers pre-charged to 700 V each, one analogue modulating layer and an 11.2Ω load. With this load resistance and four constant voltage feeding 700 V of each, the maximum load current during the pulse was ideally 250 A, which corresponds to the nominal current of the CLIC DR extraction kicker striplines. In the simulations, resistance R_a in the analogue modulation layer was 1.2Ω . The magnetising inductance of the constant voltage layers and the analogue modulation layer was $13.1 \mu\text{H}$, which was expected to be a realistic value for the magnetising inductance of the magnetic cores of the prototype inductive adder for the CLIC DR kicker system, at the time when these simulation studies were completed. The core loss resistance R_c was neglected. In these simulations, the transit time of the switches, of the constant voltage layers, was set to 10 ns. The on-state resistance of the semiconductor switches were assumed to be negligibly small. This means that the magnitude of the droop of the output waveform was similar to the droop of the pulse capacitors, if the analogue modulation was not applied. The pulse width was 250 ns and the rise time from 10 % to 90 % of the

output pulse was 8.5 ns.

The dashed green curve in Fig. 4.39 shows the load voltage of the inductive adder with 20 μF of capacitance and with the modulating layer actively compensating the voltage droop. In this simulation, there was a voltage controlled current source in parallel with resistor R_a for modelling a linear power transistor in the analogue modulating layer, as shown in Fig. 4.37. The current through the current source I_m was controlled with a ramp function. The resulting droop in the load voltage is about 0.005 %, despite that the capacitance per layer being only 20 μF . This is one sixteenth of 320 μF , the amount of capacitance which is required to meet the 0.02 % droop specifications without the analogue modulating layer, if the resistive losses of the primary circuits are neglected. The maximum current through the power transistor was less than 2 % of the load current. Without an analogue modulation layer, the droop of the load voltage with 20 μF of capacitance per layer was 0.3 %, during 160 ns, and with a passive analogue modulation layer with R_a equals to 1.2 Ω it was 0.13 %.

Figure 4.40 shows the load current in the case of passive modulation, I_{load}, PM , and in the case of active modulation I_{load}, AM for the cases in which the capacitance per layer was 20 μF . In the same figure, the current through resistor R_a is also shown for active modulation, $I_{R_a, \text{eff}}, AM$, and for passive modulation, $I_{R_a, \text{eff}}, PM$.

Figure 4.41 shows magnetising current and the current through the controlled current source, I_m , which is the waveform for the active modulation. In Fig. 4.41, I_{Lm}, AM , is the magnetising current in the active modulation layer, I_{Lm}, PM , is the magnetising current in passive modulation layer, I_m, AM , is the modulation current generated by the current source for active modulation and I_m, PM , the modulation current through I_m for passive modulation. Fig. 4.42, shows the effective impedance of the analogue modulation layer, which is computed by dividing the voltage over resistor R_a by the sum of currents flowing through R_a and modulation current source I_m . In Fig. 4.42, $R_{a, \text{eff}}, AM$, is the effective impedance of analogue modulation layer in the case of active modulation and $R_{a, \text{eff}}, PM$ the effective impedance in the case of passive modulation. In Fig. 4.41, current I_m, AM starts decreasing at time point 350 ns and this decrease of the current flow down to zero at the end of the pulse was programmed in the controlled current source I_m , in order to terminate the current flow at the end of the pulse. In the real circuit, this corresponds to the decrease of the voltage across the analogue modulation layer during the fall time

of a pulse, until the RF power transistor of the analogue modulation layer stops conducting. However, in the simulation, the fast change of the current flow through I_m at 350 ns causes the fast changes for the effective impedance $R_{a,eff}$, which are visible in curve $R_{a,eff}, AM$ in Fig. 4.42 in time period 350-360 ns.

The time constant of the passive analogue modulation layer, defined as L_m/R_a , was 10.9 μs . This corresponds to 1.46 % of current reduction through the resistor R_a during the 160 ns flat-top. Therefore, the maximum current through the magnetising inductance L_m of the analogue modulation layer at the end of the pulse was 3.3 A. With the active analogue modulation and 20 μF capacitors, the peak power dissipation of the power transistor was 1.15 kW and the average power dissipation for 50 Hz repetition frequency was 7 mW. For resistor R_a , the peak power dissipation was 60.2 kW and the average power dissipation with 50 Hz repetition rate was 700 mW. Resistor R_a and the linear power transistor can be implemented using several parallel components to reduce the power dissipation per device, in comparison with a single device. However, the current sharing between the parallel connected components must be taken into consideration. The measurements of applying active droop compensation for the output pulse of a prototype inductive adder are presented in Section 5.5.2.

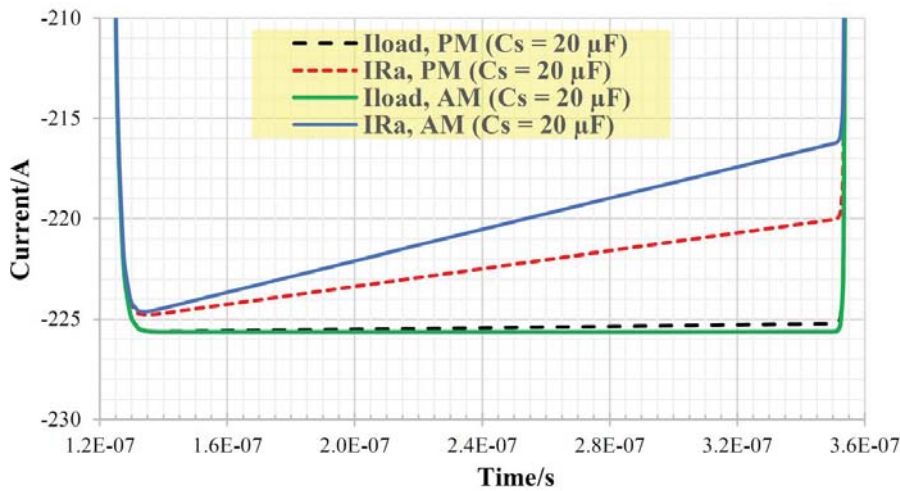


Figure 4.40. Simulated $I_{load, PM}$ and $I_{Ra, PM}$ with passive analogue modulation, and $I_{load, AM}$ and $I_{Ra, AM}$ with active modulation. $R_a = 1.2 \Omega$.

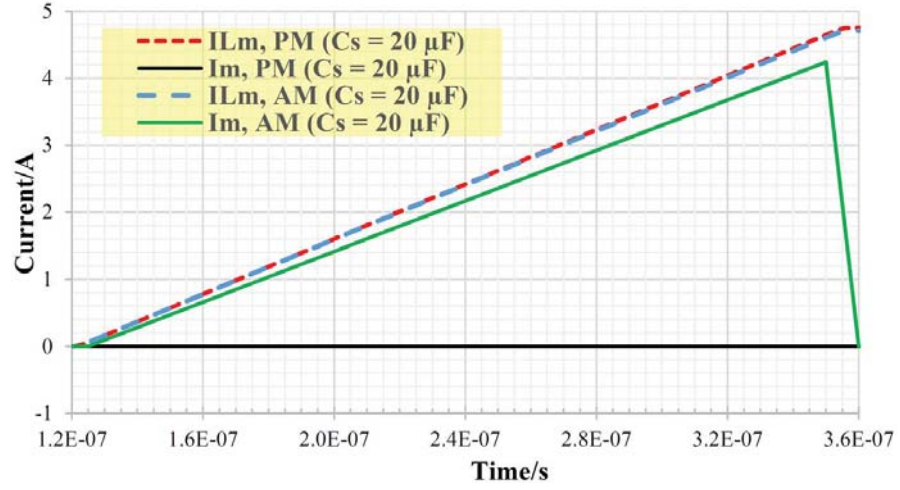


Figure 4.41. Simulated $I_{Lm, PM}$ and $I_{m, PM}$ with passive modulation, and $I_{Lm, AM}$ and $I_{m, AM}$ with active modulation. $R_a = 1.2 \Omega$.

4.5.4 Active Analogue Modulation for Compensating Ripple

Simulation Study of Active Ripple Compensation

Passive analogue modulation can be used to compensate only the droop of the load voltage, whereas active analogue modulation can be used to compensate either droop or ripple or both. This was reported briefly by the author in [17] and is repeated in detail here. For a reference, the waveforms are shown for the case in which the output of the inductive adder is compensated by the passive modulation but the droop of the output pulse is not completely compensated. This corresponds to the case shown in Section 4.5.2. The simulated waveforms are also shown for the case in which the droop is practically completely compensated by the active analogue modulation, with the same approach as presented in Section, 4.5.3.

The simulations presented in this section were completed with a model of an inductive adder, which included five layers. The four constant voltage layers and the analogue modulation layer were similar to those shown in Fig. 4.37. The parameters of the simulation model were the following: R_{load} was 11.2Ω , C_s equal to $24 \mu F$, L_{pl} equal to $24 nH$, L_{ss} equal to $3.6 nH$, C_c equal to $6.2 pF$, R_p equal to $25 m\Omega$, L_m equal to $13.1 \mu H$ and L_{ma} equal to $20 \mu H$. Parameters R_{sw} , R_s and R_c were neglected in these simulations. The pulse capacitors of the constant voltage layers were initially charged to 700 V. In this simulation, an ideal controlled current source, shown as I_r in Fig. 4.37, was connected in parallel with the load resistor to feed repetitive ripple into the load. The ripple was a sine wave at 30 MHz

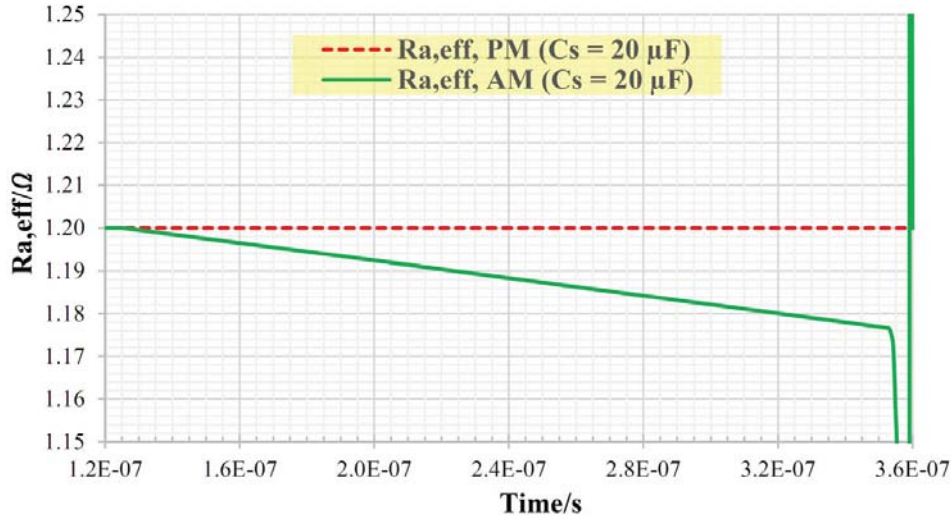


Figure 4.42. The effective impedance of the analogue modulation layer in the case of passive modulation, $R_{a,eff, PM}$, and active modulation, $R_{a,eff, AM}$. $R_a = 1.2 \Omega$.

with a fixed amplitude of ± 0.11 A, corresponding to ± 0.05 % ripple for the load current. Fig. 4.43 shows the simulated load voltage of the inductive adder in each case. The amplitudes of the curves in Fig. 4.43 are shown in relative scale and $V_{load, PM}$ is the load voltage in the case of passive modulation, $V_{load, AM, d}$ is the output voltage in the case of active droop compensation and $V_{load, AM, d \& r}$ is the output voltage in the case of active droop and ripple compensation.

In Fig. 4.43, the droop of the load voltage, in the case of passive droop compensation, shown as $V_{load, PM}$, is approximately 0.15 % for 160 ns flat-top duration, from 140 ns to 300 ns, and the ripple of the load voltage is ± 0.05 %. When the active compensation of the droop is applied for the load voltage, shown in this case as $V_{load, AM, d}$, the droop is practically completely compensated over the 160 ns flat-top duration. However, there is ripple in load voltage and it has the same amplitude as in the case of passive droop compensation, ± 0.05 %. $V_{load, AM, d \& r}$ in Fig. 4.43 is the simulated load voltage, in the case in which the droop and ripple of the load voltage are actively compensated. There is no droop, as in the case of active droop compensation, which is shown as $V_{load, AM, d}$ in the same figure. Also, the amplitude of the ripple has been considerably decreased by the active ripple compensation, and it is approximately ± 0.018 % of the load voltage.

Figure 4.44 shows the load currents and Fig. 4.45 the currents flowing through resistor R_a for the same three simulations for which the load

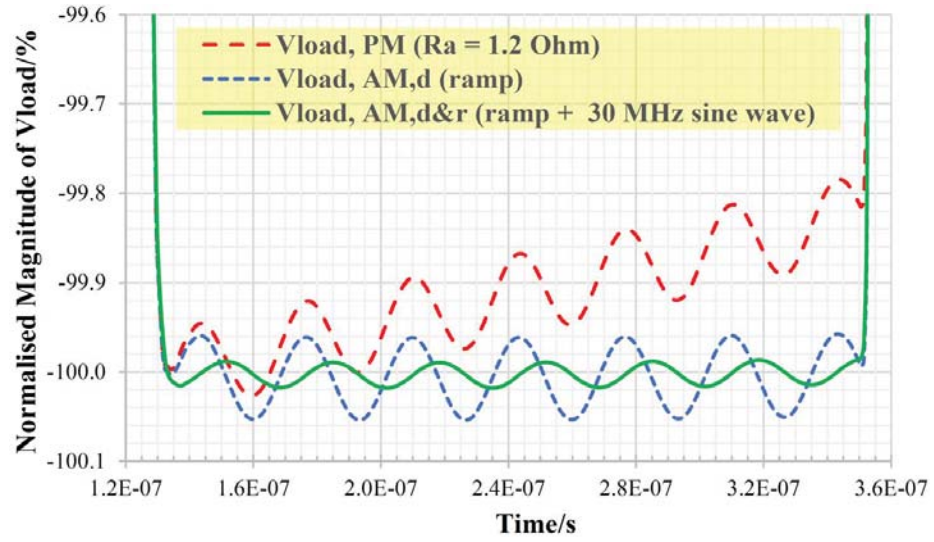


Figure 4.43. Simulated V_{load} with passive modulation, $V_{load, PM}$, with partial droop compensation, $V_{load, AM, d}$, and with partial droop and ripple compensation, $V_{load, AM, d\&r}$.

voltages are shown in 4.43. In Fig. 4.44, $I_{load, PM}$, is the load current in the case of passive modulation, $I_{load, AM, d}$ is the load current in the case of active droop compensation and $I_{load, AM, d\&r}$ is the load current in the case of active droop and ripple compensation. In Fig. 4.45, $-IR_a, PM$, is the current of resistor R_a in the case of passive modulation, $-IR_a, AM, d$ in the case of active droop compensation and $-IR_a, AM, d\&r$ in the case of active droop and ripple compensation. The voltage polarity of the components of the primary circuit of the analogue modulation layer, e.g. L_m and R_c , is the opposite in comparison to the other layers of an inductive adder. Therefore the currents flowing through R_a are shown with the negative sign, as $-IR_a$. The amplitudes of the load current and the current flowing through R_a are comparable, and the difference of these currents is caused by the current flowing through the magnetising inductance L_m of an analogue modulation layer, the current flowing through controlled current source I_m and the current flowing through the resistor R_c of an active analogue modulation layer.

Figure 4.46 shows the current of the controlled current source I_m of an analogue modulation layer in each simulation and Fig. 4.47 the effective impedance of the analogue modulation layer, $R_{a, eff}$. In Fig. 4.46, I_m, PM is the modulation current in the case of passive modulation, I_m, AM, d in the case of active droop compensation and $I_m, AM, d\&r$ in the case of active droop and ripple compensation. In Fig. 4.47, $R_{a, eff, PM}$ is the effective impedance of the analogue modulation layer in the case of pas-

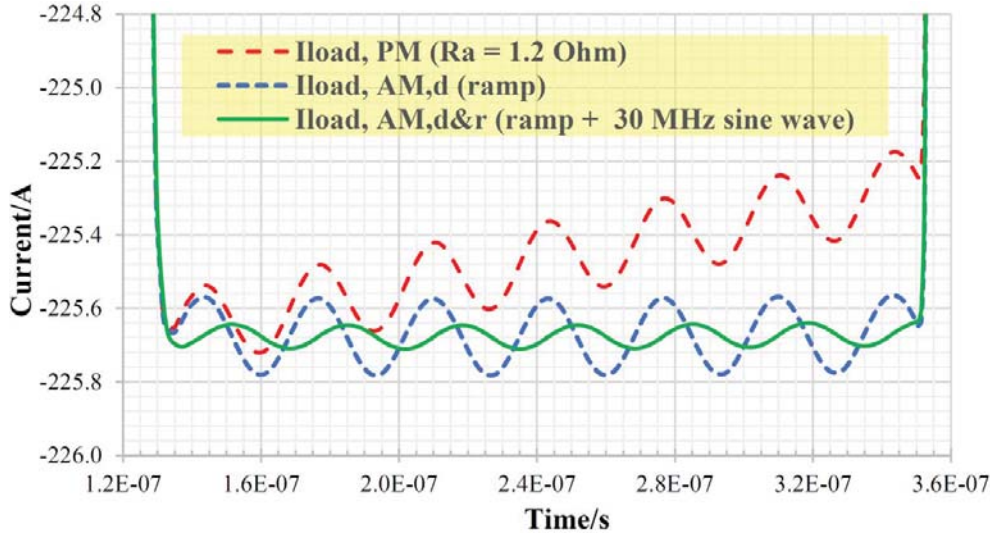


Figure 4.44. Simulated I_{load} with passive modulation, $I_{load, PM}$, with partial droop compensation, $I_{load, AM, d}$, and with partial droop and ripple compensation, $I_{load, AM, d \& r}$.

sive modulation, $R_{a, eff}$, AM, d in the case of active droop compensation and $R_{a, eff}$, $AM, d \& r$ in the case of active droop and ripple compensation. In the case of passive modulation, the current of the modulation current source, I_m, PM in Fig. 4.46, is zero. In the case of active droop compensation, I_m, AM, d is a ramp signal.

The droop of the load current without active droop compensation, shown as $I_{load, PM}$ in Fig. 4.44, is 0.30 A for the 160 ns pulse flat-top duration from 140 ns to 300 ns. The amplitude change of the modulation current source for compensating the ramp, shown as I_m, AM, d in Fig. 4.46 is approximately 3.0 A for 160 ns flat-top duration from 140 ns to 300 ns. This means that effectively, the compensation waveform of the current source is attenuated by factor of ten. However, this attenuation depends on the resistance R_a of the analogue modulation layer, because the required compensation amplitude for the load voltage is generated by feeding current through the resistor R_a , to cause the required amplitude effect in voltage across the analogue modulation layer. In absolute numbers, the 0.15 % droop of the load voltage $V_{load, PM}$ for 160 ns flat-top duration in Fig. 4.43 corresponds to approximately 3.6 V and this is compensated by increasing the current flowing through R_a , in such way that the voltage across that resistor is changed by 3.6 V with the appropriate phase. In order to determine the phase of the modulation waveform, studies are required to determine the transfer function between modulation source and load, as a function of frequency.

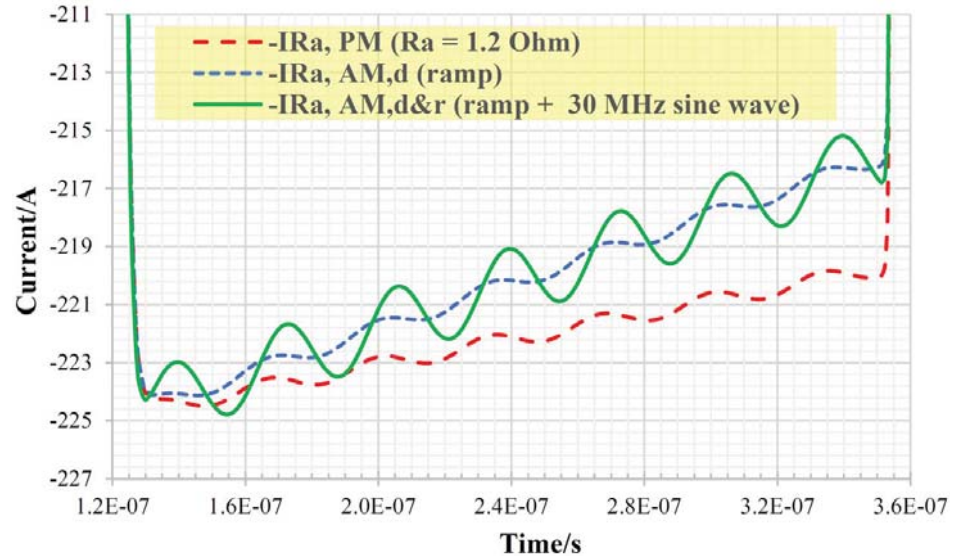


Figure 4.45. Simulated I_{Ra} with passive modulation, I_{Ra}, PM , with partial droop compensation, I_{Ra}, AM, d , and with partial droop and ripple compensation, $I_{Ra}, AM, d\&r$.

The 30 MHz ripple, which is visible in $-I_{Ra}, PM$ and $-I_{Ra}, AM, d$ in Fig. 4.45, is coupled to the analogue modulation layer from the secondary of the inductive adder, and it is generated by the ripple source. The current of the modulation current source I_m is shown in Fig. 4.46 in each simulation. In the case of passive modulation, shown as I_m, PM , the current of I_m is zero. In the case of active droop compensation, I_m, AM, d , the current flowing through I_m is a ramp with a constant gradient. In the case of active droop and ripple compensation, shown as $I_m, AM, d\&r$, the current flowing through I_m is a combination of a ramp, which has the same magnitude as I_m, AM, d , and a 30 MHz sine wave with an amplitude of ± 1.2 A. In the case of active ripple compensation, the sine wave current generates a sine wave voltage over the analogue modulation layer, and in this case the amplitude of the sine wave of the modulation current, shown as $I_m, A, d\&r$ in Fig. 4.46, is ± 1.2 A. This current is fed through R_a , which is 1.2Ω , and this causes voltage amplitude of ± 1.4 V across the resistor R_a and, effectively, across the analogue modulation layer. In Fig. 4.43, the amplitude of the ripple of the load voltage in the case of passive modulation, and in the case of active modulation for droop compensation, is approximately $\pm 0.05\%$ of the load voltage, which corresponds to ± 1.3 V. Ideally, the modulation current from I_m should compensate the ripple completely and the amplitude of the compensation current was slightly larger than required for full compensation, and therefore, if it was appropriately aligned to the phase of the original ripple, it could have gener-

ated a small ripple, approximately 0.1 V, with an opposite phase. However, in Fig. 4.44, in the case of active droop and ripple compensation, shown as $I_{\text{load}}, AM, d\&r$, it can be seen that there is ripple in the load current and the phase is not perfectly opposite, delayed by -180 degrees, in comparison with the load current in the case of droop compensation, shown as I_{load}, AM, d in the same figure. This means that the phase of the compensation waveform was not perfectly aligned to compensate the ripple completely. However, in Fig. 4.43, it is clearly visible, that the total droop and ripple in the case of active droop and ripple compensation, shown as $V_{\text{load}}, AM, d\&r$, is reduced to the magnitude of $\pm 0.018\%$ between 140 ns and 300 ns. In the case of passive droop compensation, shown as V_{load}, PM, d in the same figure, the combined droop and ripple was $\pm 0.1\%$ and in the case of active droop compensation, shown as V_{load}, AM, d , it was $\pm 0.05\%$.

Figure 4.47 shows the effective impedance $R_{a,\text{eff}}$ in each simulation and it is computed by dividing the voltage applied across the analogue modulation layer by the sum of the currents flowing through the resistor R_a and through the modulation current source I_m . In the case of passive droop compensation, shown as $R_{a,\text{eff}}, PM$ in Fig. 4.47, the effective impedance $R_{a,\text{eff}}$ is constant, $1.2\ \Omega$. In the case of active droop compensation, shown as $R_{a,\text{eff}}, AM, d$ in the same figure, the effective impedance $R_{a,\text{eff}}$ reduces during the pulse, which effectively decreases the voltage across the analogue modulation layer and generates the compensating ramp for the output voltage. In the case of active droop and ripple compensation, shown as $R_{a,\text{eff}}, AM, d\&r$, the effective impedance of R_a is reduced during the pulse to compensate the droop, and in addition to that the effective impedance is modulated with a frequency of 30 MHz, to create a sine wave to compensate the ripple of the load voltage.

For simplicity, in this simulation study, the droop and ripple of the load voltage was assumed to consist of a sine wave at a single frequency. In reality, the flat-top ripple could consist of a mixture of ripple waveforms, with a variety of amplitudes and frequencies. It was also assumed that the droop and ripple of the load voltage can be predicted from the previous pulses, in order to compensate it by the means of mixed feedback-feed-forward control. For a real set-up with an inductive adder, cables, a stripline kicker and the load, this might be achieved by recording the load voltage and taking an average of consecutive pulses, in order to filter out the non-repetitive ripple components of the output waveform. The

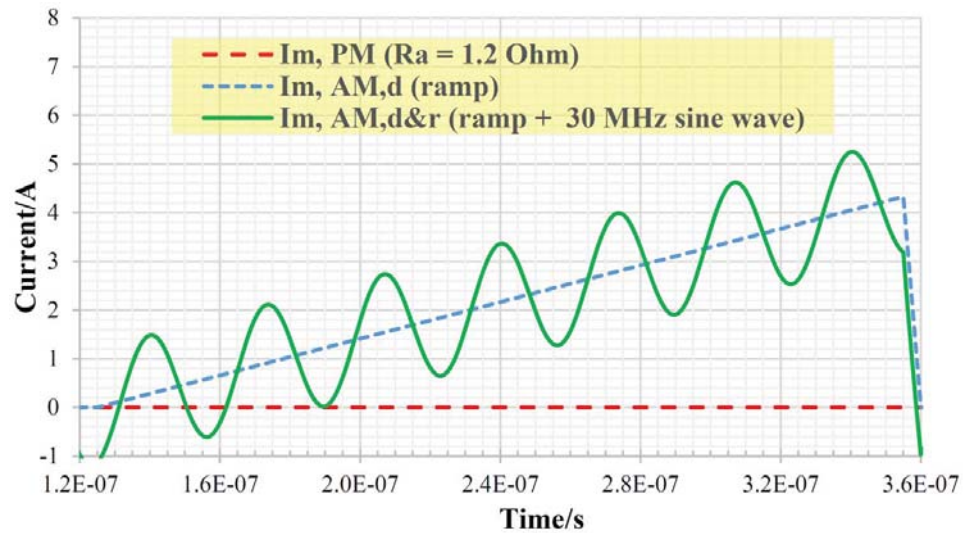


Figure 4.46. Simulated I_m with passive modulation, I_m, PM , with partial droop compensation, I_m, AM, d , and with partial droop and ripple compensation, $I_m, AM, d\&r$.

non-repetitive droop and ripple of the pulse waveform are assumed to be smaller than the required stability requirement, $\pm 0.02\%$. This assumption is based on the identified possible sources of droop and ripple, shown in Section 2.2.1, and on the simulation studies presented in this chapter, especially in Section 4.3. Considering the list of contributors to the stability of the kicker system, given in Section 2.2.1, various sources of droop and ripple have been studied with simulations in this chapter. At first, based on the simulation studies, the proposed preliminary design for the prototype inductive adder, presented in Table 3.1, is not prone to generate ringing or overshoot for the output pulse, as is shown in Section 4.1.2. Secondly, if MOSFET switches are used in an inductive adder, the time jitter of the switching times of the switches is supposed to be very short. Finally, as was shown with simulation studies in Sections 4.3.2 and 4.3.3, the reflections, caused by mismatches of characteristics impedances of the parts of the kicker system, e.g. the inductive adder and the striplines, die out relatively quickly in the stripline kicker system which is driven by an inductive adder. This means that after a certain settling time, e.g. 110 ns as found in Section 4.3.2 for a stripline kicker system with the $41\ \Omega$ stripline and the $50\ \Omega$ inductive adder with 50 ns rise time of the output pulse, shown in Fig. 4.25, the reflected waveforms are damped below $\pm 0.02\%$ of the pulse amplitude. The result of this simulation study gives an idea of the settling time required to damp reflections which may be caused by other possible mismatches in the system, e.g. terminating loads and

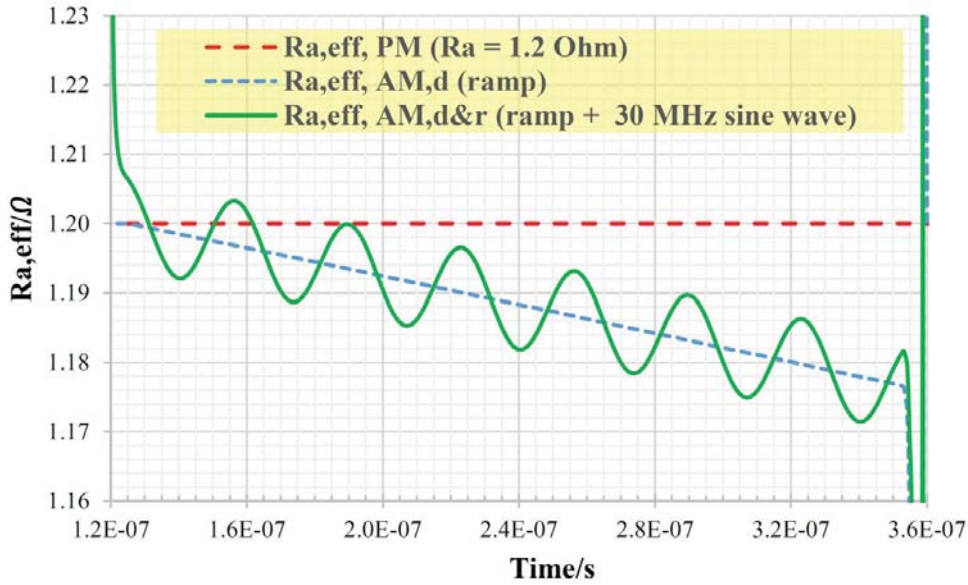


Figure 4.47. Simulated $R_{a,eff}$ with passive modulation, $R_{a,eff}, PM$, with partial droop compensation, $R_{a,eff}, AM, d$, and with partial droop and ripple compensation, $R_{a,eff}, AM, d \& r$.

the feedthroughs. Based on the reasoning given above, the assumption that the non-repetitive ripple and droop during the required flat-top duration of the pulse, 160-900 ns, are below $\pm 0.02\%$, can be considered realistic. However, referring back to Section 2.2.1, a few points cannot be confirmed without measurements with the real prototypes. These are stability and repeatability of the output voltage of the high-voltage power supplies, which are needed to charge the capacitors of an inductive adder. Also, the temperature effects of the switches and other components cannot be easily simulated. As the last point, the frequency dependence and stability of the terminating resistors cannot be confirmed without careful measurements. In addition, all simulation models are based on simplifications and assumptions, which are not necessarily true in reality. However, Chapter 5 presents measurements, which were made with inductive adder prototypes, and which showed that the reasoning given above is also true for real inductive adders.

One limitation of the operation of the analogue modulation layer in a real inductive adder is that the operating voltage and current range of the RF power transistor is limited and the current flowing through the RF power transistor in the analogue modulation layer has to be of a single polarity. The voltage across the analogue modulation layer in the case of the active analogue modulation is defined by the effective impedance of the layer, i.e. the parallel connection of the resistor R_a , the core loss re-

distance R_c and the operating impedance of an RF power transistor in the layer. The voltage across the RF power transistor and the average current flowing through it during the pulse can be set by choosing resistance R_a appropriately. It is also possible to apply more than a single modulation layer in an inductive adder if a larger modulation range is needed.

The main goal of this dissertation was to demonstrate that it is technically feasible to generate high-voltage pulses with the flat-top stability of $\pm 0.02\%$, which is required for the modulator of the CLIC DR kicker system. In simulation studies shown above, in Sections 4.5.2, 4.5.3 and in this section, it is shown that the droop and ripple of the output waveform of an inductive adder can be compensated. According to this simulation study, the droop and ripple could be compensated with a bandwidth and current-driving capability of components, which are commercially available. Therefore, the study shown in these three sections, together with the simulation studies for the various contributors to the flat-top stability of an inductive adder, shown in Section 4.3, and the study of designing of an inductive adder with a desired output impedance, shown in Section 4.4, clearly demonstrates that, in theory, achieving these specifications is possible and technically feasible. This is one of the main results of this dissertation. Also, the proposed approach to compensate the droop and ripple with the means of active analogue modulation, in order to reach a high stability for an inductive adder is unique and according to the Author's best knowledge, it has been proposed for the first time in this study.

4.5.5 Steps and Considerations for Applying Active Droop and Ripple Compensation for an Inductive Adder

There are a few technical aspects which need to be taken into consideration in applying the proposed method of active analogue modulation for compensating the droop and ripple for a real inductive adder. First of all, in the simulation studies shown in the previous sections, the most important known contributors have been taken into account, including both the main components and parasitic circuit elements. However, it is practically impossible to include all the possible contributors to the droop and ripple into a simulation model. In the real set-up of two inductive adders, cables, a stripline kicker and the terminating resistors, the current flowing in a stripline could include an arbitrary number of ripple components. It has been assumed in the simulation studies presented in the previous section, that there is no asynchronous ripple in the load current, which

had an amplitude comparable to the allowed flat-top variation during the pulse flat-top. This means that the components of the inductive adder and the complete set-up performs well and in reality, it is necessary to evaluate all the main components.

As mentioned in Section 2.4, the measurement of the output waveform with required accuracy and required rise time may be very difficult and even impossible with the direct electrical measurements and different averaging techniques needs to be applied to improve the resolution of the measurements, as is discussed in Section 2.4. Also, in an output pulse of a real inductive adder, there may be a mixture of repetitive ripple components, each of which has a certain amplitude, frequency and phase in respect to the main pulse amplitude. These needs to be carefully analysed in defining the compensation waveform for the active analogue modulation layer. In defining the final compensation waveform for the RF power transistor of an active analogue modulation layer, the amplitude and phase responses of the transistor, as well as the analogue modulation layer, the inductive adder stack, the cables, the stripline and the terminating resistor needs to be taken into consideration.

First estimates for the component values for the passive analogue modulation layer can be defined with the following equations:

$$R_a = \frac{V_{Ra,max}}{I_{load}} \quad (4.9)$$

$$\Delta V_{Ra} \approx R_a \times \Delta I_{Lma} = R_a \times \frac{V_{Ra,max} t}{L_{ma}} \quad (4.10)$$

$$L_{ma} = \frac{R_a^2 I_{load} t}{\Delta V_{Ra}} \quad (4.11)$$

In Eq. (4.9), $V_{Ra,max}$ is the maximum voltage across the passive analogue modulation layer, when the load current I_{load} flows completely through resistor R_a . In Eq. (4.10), ΔV_{Ra} is the decrease of the voltage across the passive analogue modulation layer during the pulse, and it is caused by the transfer of a portion of the load current, ΔI_{Lma} , from resistor R_a to the magnetising inductance L_{ma} of the analogue modulation layer in duration t . Eq. (4.11) gives an estimate for the required magnetising inductance L_{ma} for a given resistance R_a , load current, pulse flat-top duration and required voltage decrease ΔV_{Ra} , which is the magnitude of the droop to

be compensated. Equations shown above are approximations and e.g. the change of the voltage across the analogue modulation layer is neglected in defining the magnetising inductance L_{ma} . To take that into account, e.g. a half of the voltage decrease during the pulse flat-top, ΔV_{Ra} , could be subtracted from $V_{Ra,max}$ to estimate the effective voltage across L_{ma} during the pulse flat-top, and corresponding current change ΔI_{Lma} . Also, the core loss resistance, R_c , which is in parallel with R_a and L_{ma} , could be taken into account by replacing R_a in equations by the resistance of the parallel connection of R_a and R_c .

Compensation of ripple components of the output waveform of an inductive adder can be carried out with the following steps.

1. The output waveform of the inductive adder is measured and recorded.
2. The frequency content of the output waveform is computed by applying a fast Fourier transform (FFT) for the measured pulse. The FFT gives the magnitude and the phase information of the frequency components of the pulse flat-top. The most significant ripple components, which are in the modulation bandwidth of the analogue modulation layer, are considered.
3. A compensation waveform is built by summing the most significant ripple components. The phase of the ripple components in the compensation waveform is opposite in comparison with the original measured output waveform. The gain and the phase shift of the analogue modulation layer are also taken into consideration and the compensation waveform is calculated.
4. If a compensation waveform already exists, e.g. to compensate the droop, the new compensation waveform, computed in step 3., is summed with the previous compensation waveform. The new compensation waveform will significantly suppress the remaining ripple. This waveform is fed to the gate of the RF power transistor during the pulse and the output pulse is measured. If necessary, the steps 1.-4. are repeated, in order to improve the compensation effect.

In applying this method, it is assumed that the flat-top of the output waveform is repetitive. Windowing functions and zero padding can be ap-

plied in order to improve the result of the FFT analysis for the measured pulse [145]. The control method explained above is a mixed feedback-feedforward control scheme, because the compensation signal is computed based on measured pulses and the compensation is applied for the coming pulses. A point to note is that it is practically impossible to use a simple feedback control loop for the CLIC DR kicker inductive adder. Firstly, the total pulse duration is short, the duration of the flat-top is less than $1\text{ }\mu\text{s}$ and the pulse is of high-voltage, 12.5 kV, and therefore it is very difficult to measure the ripple and droop of the flat-top with adequate accuracy without taking an average of several pulses. Secondly, the compensation signal cannot be computed directly in time-domain, because the analogue modulation layer of an inductive adder has characteristic frequency-dependent phase shift and gain, which needs to be taken into account in computing the compensation waveform, in order to reach good accuracy. The third point is that the FFT needs to be computed for the total duration of the pulse flat-top, which is to be compensated. If the FFT would be taken e.g. for the first 100-200 ns of the pulse flat-top, which has a total duration of $1\text{ }\mu\text{s}$, and the compensation waveform would be computed based on the frequency and phase information computed from the first 100-200 ns, most probably it would not give correct compensation waveform for the rest of the 800-900 ns of the pulse flat-top, because the information of the ripple and droop during that time period have not been included in the FFT.

The measurements of applying the described method to reduce ripple of the output pulse of a prototype inductive adder are presented in Section 5.5.4.

5. Prototyping, Experimental Results and a Design Proposal

This chapter presents the two prototype inductive adders built and highlights the most important measurements on the prototype devices. In Section 5.1, the main components for the prototype inductive adders are selected and evaluated. The design of the prototype inductive adders, which is based on the design steps presented in Chapter 3, is also presented in this section. Section 5.2 describes the measurement set-up in detail. In Sections 5.3, 5.4 and 5.5, the experimental results are shown for applying passive analogue modulation method to compensate droop of the output waveform of the inductive adder, and for applying active analogue modulation method to compensate both the droop and ripple components of the output waveform. The most important result is the measurement of a 1.8 kV pulse with flat-top stability of $\pm 0.05\%$ for 160 ns. In this measurement, the droop and the most significant frequency component of ripple of the output waveform was compensated with active analogue modulation. The accuracy of the presented measurements is evaluated in Section 5.6. This section also presents comparison of the measured and simulated waveforms of the inductive adder. The parameters of the simulation model of the prototype inductive adder, presented in Chapter 4, are updated according to the evaluation of the components. The updated model parameters are used to estimate the output waveform of the 12.5 kV inductive adder for the CLIC DR kicker system. Finally, the design proposal and a cost estimate are presented for the 12.5 kV CLIC DR kicker inductive adder in Section 5.7.

5.1 The Two Prototype Inductive Adders

Two prototype inductive adders were built according to design steps presented in Chapter 3. These prototype adders were used to verify the pre-

sented design steps and to demonstrate experimentally both passive and active modulation methods. The main reason to build two prototypes was to demonstrate the measurement method presented in Section 2.4, according to which the dynamic range of the pulse measurement can be decreased by measuring the net pulse of two summed pulses with opposite polarities, and therefore the dynamic range of the measured signal can be decreased and the measurement can be made using higher sensitivity of an oscilloscope. This is demonstrated in Section 5.5.5. This section presents the specifications for the prototype inductive adders and gives the reasoning for selection of components for the prototype inductive adders. Finally, the mechanical and electrical design of the two prototype inductive adders built at CERN are briefly presented.

5.1.1 Design Parameters

The design parameters for the prototype inductive adders are shown in Table 3.1 in Chapter 3. The maximum output voltage was 3.5 kV with five layers, each of which gives nominally 700 V. The PCB layouts of the primary circuits of the prototype adders were designed to feed the full load current needed for the CLIC DR kicker system, nominally 250 A. The nominal maximum pulse length of the prototype inductive adder was defined to be 900 ns, which is required for the pulse duration for the CLIC DR kicker system for the 1 GHz baseline [7]. The goal values for the pulse rise and fall times were defined to be 100 ns as maximum, from 0.1 % to 99.9 % of the pulse voltage, because these are desired parameters for the CLIC DR kicker pulse modulator. Regarding the flat-top stability, the first goal for the prototype modulator was to reach the flat-top stability for the CLIC PDR kicker system, ± 0.2 % [7], and then improve it towards the final goal, ± 0.02 %. The nominal output impedance of the prototype inductive adders was defined to be 50Ω , which gives 70 A for the maximum current at 3.5 kV with a 50Ω load.

5.1.2 Selection and Evaluation of the Components for the Prototype Inductive Adders

Semiconductor Switches and Gate Drive Circuits

The operating voltage of the semiconductor switches defines the maximum operation voltage of the constant voltage layers of an inductive adder. In order to reach the operation voltage of 700 V per layer, the volt-

age rating for semiconductor switches for the prototype inductive adder was desired to be at least 1 kV, according to the design principles explained in Chapter 3. The number of the layers of the adder stack is defined by the required load voltage and the operation voltage of the semiconductor switches. For the given maximum output of 3.5 kV, the number of the layers in the prototype adder stack is five. The prototype adders do not include any spare layer for redundancy.

The specified rise and fall times of the switches were desired to be less than 100 ns and pulsed current capability at least 35 A. Several MOSFETs and IGBTs were tested and the results of these tests were reported by the author in [13]. The purpose of evaluating the switches was to measure the obtainable rise and fall times of the switches as well as measure their transient response with a specific gate drive circuit. Several promising candidate switches, all based on MOSFET technology, were identified. A rise time of less than 100 ns was not measured on any IGBT tested and therefore IGBTs were not considered further.

The decision for selecting the switches and the gate driver was made based on measurements on the candidate components and discussions with experienced designers from SLAC [100] and Rochester University [146]. In general, the measured pulse waveforms of the Microsemi's MOSFETs evaluated in [13] were very clean with the tested gate drive circuit, which was manufactured by IXYS. Microsemi's devices, especially the models designed by APT, have also been very reliable in pulse power applications [100]. However, some of the suitable candidate components would have had very long delivery time in larger quantities, which was not acceptable for the schedule of the prototype device. Based on the reasoning described above, the MOSEFT APT12067LFLL [101] was selected as the switch for the prototype inductive adders. This switch has a voltage rating of 1.2 kV, maximum constant drain current rating of 18 A (up to 64 A pulsed), and typical rise and fall times of 19 ns. The gate drive circuits used previously during evaluation of components by the author [13], [14] were not anymore available at the time of placing orders for the parts of the prototype inductive adders, therefore the gate drive circuit was chosen to be IXYS IXDD614SI [147]. This model had worked well in another inductive adder application with fast switching times [81], [146]. Fig. 5.1 shows a single branch of a half-layer PCB of the first prototype inductive adder.

Linear RF power transistors, needed for the active analogue modula-

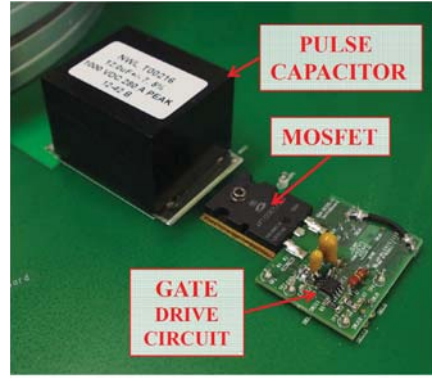


Figure 5.1. A MOSFET switch, a gate drive circuit and a pulse capacitor of the prototype inductive adder.

tion layer, were also tested for the prototype inductive adder. The results of the measurements were published in [13]. Based on that study, an ARF463AP1G type RF power transistor from Microsemi [148] was chosen for the active analogue modulation layer of the first prototype inductive adder.

Pulse Capacitors

The pulse capacitors need to have extremely low inductance to avoid large voltage transients during turn-off of the switches, as mentioned in Chapter 3, and to minimise the primary loop inductance and thus the two-way propagation delay of the inductive adder, as discussed in Chapter 4. The pulse capacitors, chosen for the prototype inductive adders, are manufactured by NWL Capacitors [131]. Each capacitor, shown in Fig. 5.1, is nominally 12 μF , rated for 280 A of peak pulse current, and for 1 kV DC voltage. The inductance of the pulse capacitor was determined by measurements. Ten pulse capacitors were tested by short-circuiting a charged capacitor and measuring the resonant frequency of the voltage waveform. The measurement set-up and a detailed description of the results were reported in [13]. The results of these measurements are summarised in Table 5.1. The average inductance of the ten pulse capacitors was approximately 14 nH.

Table 5.1. Average values and standard deviation of capacitance, parasitic inductance and parasitic resistance of 10 NWL pulse capacitors.

C (μF)	σ_c (μF)	L (nH)	σ_L (nH)	R ($\text{m}\Omega$)	σ_R ($\text{m}\Omega$)
12.12	0.15	14.35	0.40	16.66	2.73

Ideally with 70 A of load current and 15 % of magnetising current, in total 80.5 A of primary current, 92 μF of capacitance per layer would be enough to limit the droop of the capacitor voltage to 0.02 % during a 160 ns pulse flat-top. This is computed using Eq. (3.4) presented in Chapter 3. Therefore, the number of 12 μF capacitors per layer is chosen to be eight, which gives a total capacitance per layer of 96 μF . However, as discussed in Section 4.5, in this estimate the resistive losses of both the semiconductor switches and the current loop of the primary circuit are not taken into account. The resistive losses of the primary circuit can be the main contributor to the droop of the output waveform, as the author presented in [17].

Magnetic Cores

A requirement for each magnetic core in an inductive adder is to have enough volt-second integral to supply a 1.1 μs long voltage pulse of 700 V. In this calculation, the flat-top pulse duration is 900 ns, settling time is expected to be 100 ns and a half of the rise and fall times are taken into account, corresponding to 100 ns in total for the edges. The effective cross-sectional size of the magnetic cores for the prototype inductive adders was computed in Section 3.6.1 by Eq. (3.33). According to the equation, the ECSA of a core would be at least 3.5 cm^2 per layer and including the 100 % margin, the ECSA should be 7 cm^2 per layer. Assuming a packing factor of 65 % for the magnetic core, the actual cross-sectional area of the tape wound magnetic core should be at least 10.8 cm^2 .

Originally, the magnetic core material was chosen to be 2605CO and the cores were ordered from Metglas [111]. This material could potentially provide very high magnetising inductance, square-shaped B-H curve and maximum flux-density swing of 3.4 T [111]. The cores have also been designed for use with high magnetisation rates in pulse power applications and they have adequate insulation between the adjacent turns of the metal ribbon [132]. However, the initial measurements on the prototype adder, with the delivered cores, showed that the magnetising current of these cores was much higher than expected. After careful studies it was also found that the loss resistance of these cores was very low, which caused the loss current to increase rapidly to a high value, over 100 A, by the end of the rise time of a 700 V pulse voltage. It was also found that the B-H curve of these cores was very square-shaped and, therefore, the remanent magnetic field of these cores was very high after a single

pulse. This caused the magnetising inductance of these cores to be very low, an order of magnitude lower than expected without biasing. It was found that biasing of the cores between the pulses was necessary. However, this was not desirable for the prototype inductive adders, because of the added complexity and possible effects on the flat-top stability and intra-pulse voltage.

The replacement cores, with linear B-H characteristics and very low remanent field, were ordered from another supplier for the prototype adders. Core material Vitroperm 500 F was chosen to be tested, and core type W567, manufactured by Vacuumschmelze, was chosen. The maximum flux-density swing of the core material, Vitroperm 500 F, is 2 T [114]. The outside diameter of the core is 130 mm, the inside diameter 100 mm and the height 25 mm [136]. The effective cross-sectional area of these cores is 2.85 cm^2 and the usable, linear, flux-density swing of these cores was estimated to be 1.4 T without biasing, which is the same as expected for the original Metglas cores. With these values, and allowing a 100 % safety margin, the maximum pulse flat-top duration was theoretically restricted to 180 ns with 700 V per layer, allowing for 100 ns of rise and fall times. This pulse length would still include 100 % margin in order to avoid saturation of the magnetic core. The magnetising inductance of the cores for a single turn is specified to be $50 \mu\text{H}$ at 10 kHz and $19.4 \mu\text{H}$ at 100 kHz, with tolerances of +45 % and -25 %, respectively, for the inductance values [138]. The 100 ns rise time corresponds to approximately 3.5 MHz bandwidth for the output pulse, therefore the effective magnetising inductance was expected to be significantly lower than $19.4 \mu\text{H}$ during the rise time. Fig. 5.2 shows a bottom flange of the prototype inductive adder with a Vacuumschmelze W567 magnetic core.



Figure 5.2. An aluminium bottom flange of the prototype adder with a Vacuumschmelze W567 magnetic core.

Connectors

High-voltage connectors are needed to connect the secondary winding of the inductive adder to a high-voltage cable. These connectors were selected according to high-voltage insulation requirement and for impedance requirements in order to minimise the impedance mismatch with the $50\ \Omega$ system. The output connector of the inductive adder should preferably be similar to the connectors of the terminating resistors, stripline kicker and the load. Kyocera 15 kV-F-UHV Vacuum feedthroughs were chosen for the prototype stripline kicker [149]. This is compatible with Teledyne Reynolds 167-4534 plug, which is compatible with Teledyne Reynolds 167-3517 connector [150]. In contrast to Kyocera's connector [151], Teledyne Reynolds 167-3517 is not specified for use as vacuum feedthrough. Its outside surface has threads and its assembly for the prototype device was expected to be simpler and therefore it was selected. In addition the Teledyne Reynolds 167-3517 connector is rated for 20 kV, as opposed to 15 kV for the Kyocera connector, so it has a higher safety margin. Fig. 5.3 shows two output connectors as utilised for the prototype adders.



Figure 5.3. Two Teledyne Reynolds 167-3517 high-voltage connectors.

Terminating Resistors

The load resistor needed for each CLIC DR kicker system should have a high bandwidth, ideally from DC up to more than 100 MHz and they should absorb an average power of at least 156 W coming from the inductive adders. In addition to this, the loads should also absorb the power which is induced to the stripline kicker from the passing beam. In order to match each load to an inductive adder and the stripline kicker, they need to be ideally $50\ \Omega$ and the connectors of the loads should also have the same impedance.

Ideally, the resistance of the loads should remain stable during the pulse when the striplines are powered by the inductive adders. However, as it was shown with simulations in Section 4.3.4, the absolute value of a lin-

ear deviation of the load resistance during the pulse is not critical, as the deviation should be able to be compensated with analogue modulation. In addition, the passing beam, which induces a short pulse to the striplines, should ideally see $50\ \Omega$ impedance when the striplines are not powered by the adders. Therefore, the long-term stability of the loads should preferably be very good and the impedance should remain within $\pm 0.01\%$ of $50\ \Omega$ for years.

Two pieces of custom-made $18\ \text{kV}$, $50\ \Omega$, $160\ \text{W}$ (Fig. 5.4) loads were ordered from Diconex [152] to test the prototype inductive adders. They are equipped with Teledyne Reynolds 167-3517 connectors.



Figure 5.4. Diconex $18\ \text{kV}$, $50\ \Omega$, $160\ \text{W}$ terminating load.

5.1.3 Mechanical and Electrical Design of the Prototype Inductive Adders

The mechanical and electrical designs of two prototype inductive adders were carried out according to the design principles presented in Chapter 3. The design of the prototype adders is discussed briefly in this section. In addition Appendix A "Assembly of the Prototype Inductive Adders" presents the mechanical and electrical assembly of the first prototype inductive adder in detail. The physical dimensions of the cells of the two prototype inductive adders were the same as shown in Table 3.3 and the secondary stalks were insulated by air. Fig. 5.5 shows the stack of five cells of the first prototype inductive adder without half-layer PCBs and diode boards inserted.

Figure 5.6 shows a single half-layer PCB of the first prototype inductive adder. The half-layer PCBs were equipped with four current branches per half-layer PCB and hence in a single layer there were eight current branches. A single current branch consists of a $12\ \mu\text{F}$ pulse capacitor and a MOSFET switch. In the measurements presented in this dissertation,



Figure 5.5. The complete stack of the first prototype inductive adder without PCBs.

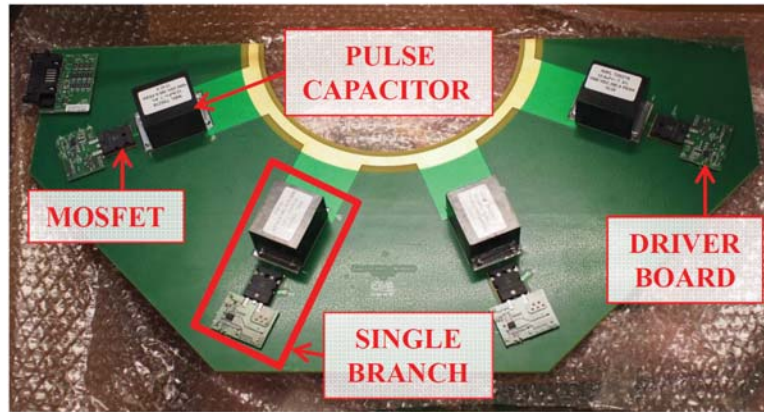


Figure 5.6. A half-layer PCB of the first prototype inductive adder.

a single current branch per half-layer PCB was powered in the first prototype device. The reason for this was that the first manufactured batch of the driver boards shown in Fig. 5.6 required manual assembly work and trimming to work stably. Powering of only the single branch per half-layer PCB caused the droop of the output waveform, without modulation, to be approximately four times larger than what it would have been with all eight branches powered. However, it was found in the measurements that the droop of the output pulse could be compensated completely with the passive and active analogue modulation, as is shown in this chapter. Therefore, all the measurements for this dissertation were completed with a single branch powered per half-layer PCB. Powering of two branches per layer instead of eight also caused the output impedance of the prototype inductive adders to increase, because the total primary loop inductance was increased. According to analytical equations presented in Chapter

3, the output impedance of the first prototype inductive adder with two branches per layer powered was 64.6Ω and the output impedance of the second prototype adder with two branches per layer powered was 68.8Ω . The diameters of the secondary stalks were 45 mm and 43 mm, respectively. In this chapter, the first prototype adder is also referenced as inductive adder 1 and the second prototype adder is referenced as inductive adder 2.

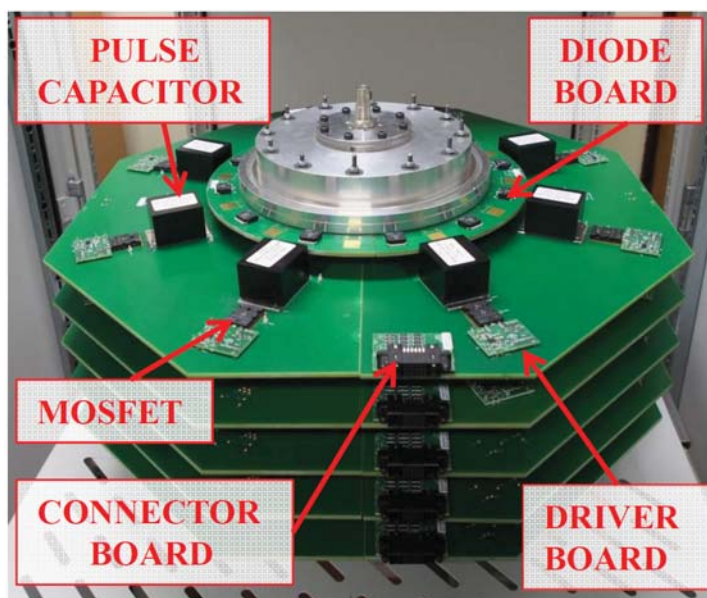


Figure 5.7. The first 5-layer prototype inductive adder at CERN.

Figure 5.7 shows the first prototype inductive adder with diode boards and half-layer PCBs inserted. The maximum pulse duration of the prototype inductive adders was restricted in the measurements to approximately 350 ns with nominal voltage 700 V per layer, because of the relatively small cross-sectional area of the chosen magnetic cores, and this pulse duration required the use of flux-density swing from close to zero to close to saturation, i.e. operation without considerable safety margin. The magnetic cores of the prototype inductive adders are demagnetised after the pulses by the diode boards. When the switches are turned off at the end of the pulse, the primary current starts flowing through the diode boards, which induces a voltage over the magnetising inductance with the opposite polarity in comparison with the pulse voltage. This voltage causes the flux-density in the cores to decay. The decay time depends on the voltage and duration of the pulse and the forward voltage of the diode. An approximate estimate of the decay time can be computed by dividing the maximum nominal voltage per layer, 700 V, by the typical

forward voltage, 1.7 V, of APT60D100SG diode [153] used in the prototype adder. In this case, the decay time would be 412 times the effective pulse duration $t_{p,50}$ and with $t_{p,50}$ of 500 ns, the decay time would be 206 μ s. Thus, theoretically, the inductive adder could be operated at a frequency of almost 5 kHz without requiring additional reset circuitry.

When the current stops flowing in the diode, the flux-density of the core is expected to be the positive remanence value of the flux-density swing. According to [135], the remanence value of Vitroperm 500 F material is 0.05 T, which is measured for a 10 Hz sine wave. Biasing of the cores, which could be applied for example by feeding a constant DC current through the cores through a large inductor [71], would ensure that most of the usable flux-density swing is available during the pulse. If the biasing is not used, and the repetition rate is too high, the starting point of the flux-density swing may begin to drift, because the current of the diode does not decay completely before the next pulse begins. This could lead to saturation of the cores, even in the case in which the total flux-density swing caused by the pulse is smaller than the initial difference between the remanence flux-density and the saturation flux-density.

In the measurements presented in this dissertation, the cores of the prototype inductive adders were not biased between the pulses. This limited the maximum pulse duration to approximately 350 ns with Vacuumschmelze W567 cores with nominal operation voltage, 700 V per layer, without applying any safety margin for the usable flux-density swing from close to zero to close to saturation. However, the choice that biasing was not applied may also have been beneficial in order to reach extremely good flat-top stability for the output pulse, because a simple DC reset circuit, consisting of a large inductor and a DC supply, as presented for example in [125], could cause flat-top ripple for the output pulse. Also, in [126] it was mentioned that a DC reset circuit could cause undesired intra-pulse ripple which also would not be acceptable for the CLIC DR kicker system. The repetition rate of the output pulses of the prototype inductive adders was kept at 1 Hz in order to ensure that the starting point of flux-density swing of each pulse in each measurement was the same. The only measurements in which the magnetic cores were biased, are presented in Appendix B.

5.1.4 Design of the Analogue Modulation Layer

The passive and active analogue modulation layers were built using a similar PCB layout as was used for the constant voltage layers. The differences were that in the passive analogue modulation layer, the pulse capacitors were removed and replaced with a nominally non-inductive resistor R_a , manufactured by HVR [154]. In the active analogue modulation layer, an RF power transistor type ARF463AP1G from Microsemi [148] was connected in parallel with the resistor R_a . In all the measurements of the active analogue modulation presented in this dissertation, the measured value of resistance R_a was $7.96\ \Omega$, at an ambient temperature of $21.7\ ^\circ\text{C}$.

Figure 5.8 presents the schematic and Fig. 5.9 shows a photo of the active modulation layer which was used in the measurements presented in this dissertation. In the measurements in which only the passive analogue modulation was applied, only the resistance R_a shown in Fig. 5.9 was connected on the analogue modulation layer. In the cases when the active analogue modulation was applied together with the passive analogue modulation, the RF power transistor, control signal input with a DC blocking capacitor ($2.2\ \mu\text{F}$) and DC biasing input were also connected on the analogue modulation layer, as shown in Fig. 5.9. The control signal for the RF power transistor was fed from a signal generator through two relatively short $50\ \Omega$ coaxial cables, the time delay t_d of each was $5\ \text{ns}$. The high-frequency control signal was coupled to the gate pin of the RF power transistor through a $2.2\ \mu\text{F}$ tantalum capacitor, which blocked the DC biasing voltage of the gate pin from being fed to the signal generator. The signal path, adjacent to the DC blocking capacitor, was terminated with a $50\ \Omega$ resistor in order to avoid reflections. The DC biasing voltage for the RF power transistor was fed from a DC laboratory power supply and fed through a $2\ \text{k}\Omega$ resistor to the gate pin. The oscilloscope shown in Fig. 5.8 had an input impedance of $1\ \text{M}\Omega$.

All the measurements shown in this dissertation were done using the schematic shown in Fig. 5.8. However, in the left side of the schematic, there is a $50\ \Omega$ resistor in parallel with the output of the signal generator. This resistor is not necessary for the operation of the analogue modulation layer and therefore, it is marked as a dashed, red, line in the figure. The reason why the resistor is in the schematic is that the purpose was to connect an attenuator between the output of the signal generator and

the cable. This attenuator could have helped to suppress possible voltage transients coming from the inductive adder towards the signal generator. By a mistake, instead of an attenuator, a $50\ \Omega$ resistor with an identical coaxial housing was connected to the output of the signal generator. As a consequence, the signal generator was effectively connected to a $25\ \Omega$ transmission line, instead of a $50\ \Omega$ as expected. However, when that mistake was found and the resistor was removed, the operation of the analogue modulation layer did not change.

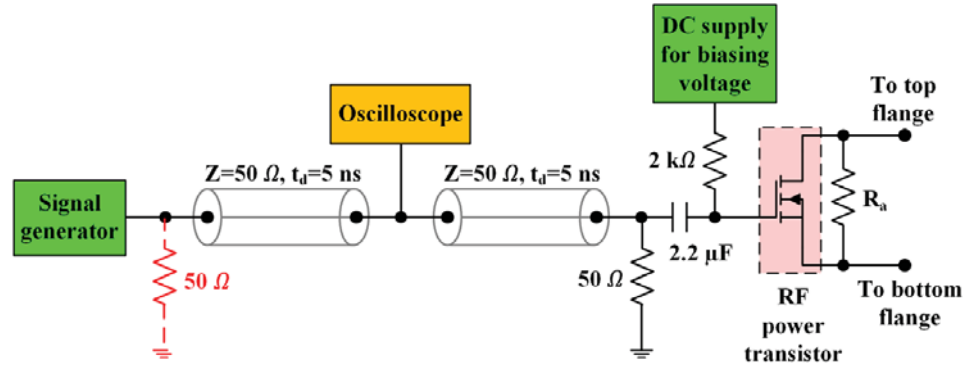


Figure 5.8. Schematic of the active analogue modulation layer of the first prototype inductive adder.

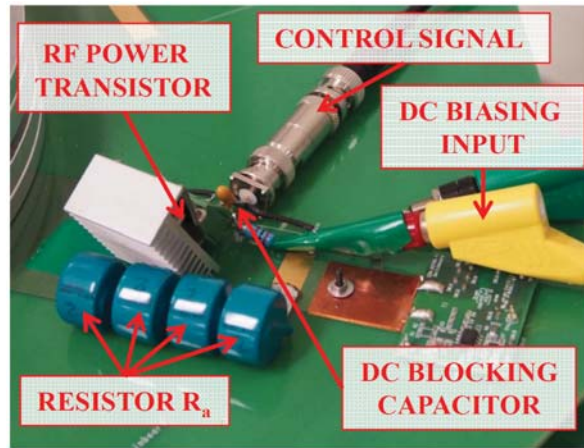


Figure 5.9. Photograph of the active analogue modulation layer of the first prototype inductive adder.

It is a point to note that in the measurements shown in this dissertation, there was not an RF amplifier circuit connected. The absence of the amplifier caused some drawbacks, the biggest of which was that the output impedance of the signal generator ($50\ \Omega$) and the cables with which it was connected to the DC blocking capacitor were visible to the RF power transistor. This made the RF power transistor sensitive to relatively small changes of the operation point of the signal generator and also to any

changes in the cabling. Despite these drawbacks, applying the active analogue modulation to compensate the droop and a single ripple component of the output waveform was successfully demonstrated with the measurements, as is shown in this chapter.

5.2 Description of the Measurement Set-up

Figure 5.10 shows the measurements set-up which was used to complete the measurements presented in this dissertation. Fig. 5.11 shows a schematic of the measurements set-up with characteristic impedances and delays of the cables. The measurements were carried out in a high-voltage test cage, the temperature of which was controlled to 21.7 ± 0.5 °C. In Fig. 5.10, the inductive adder is connected to the load with a coaxial cable, which is equipped with a current transformer. The $50\ \Omega$ load resistor, made by Diconex [152], was connected to the adder with a 2.5 m long, $50\ \Omega$, coaxial cable of type HTC-50-7-2 [144]. In this dissertation, the measurements are referred to as load voltage. Due to the inherent difficulty in measuring fast high-voltage pulses and trimming the probe compensation properly, a high quality current transformer was used instead of a high-voltage probe. Therefore, in the measurements shown in this dissertation, the load voltage was derived by multiplying the measured current by the nominal impedance of the load, $50\ \Omega$. The load current was measured with the Bergoz CT-E0.1-B current transformer, which was installed around the inner conductor of the coaxial cable. The specifications of the current transformer were the following: maximum peak current 10 kA, droop $0.002\ \%/ \mu\text{s}$, rise time 7 ns and 3 dB cut-off frequency of 50 MHz [92]. In the vicinity of the current transformer, the outer conductor of the coaxial cable was replaced with a 10 mm wide and 1 mm thick piece of copper sheet, which was bent tightly to minimise the area between the inner and outer conductors and thus to minimise the impedance mismatch which was introduced by removing the outer conductor. The axial direction of the current transformer was kept parallel to the coaxial cable, as is shown in Fig. 5.10. The current transformer was connected to the oscilloscope with a coaxial cable, which had a characteristic impedance of $50\ \Omega$. The impedance of the input channel of the oscilloscope was set to $1\ \text{M}\Omega$ and the coaxial cable was terminated at the oscilloscope input with a $50\ \Omega$ coaxial resistor.

The impedance of the Diconex load was measured with a network anal-

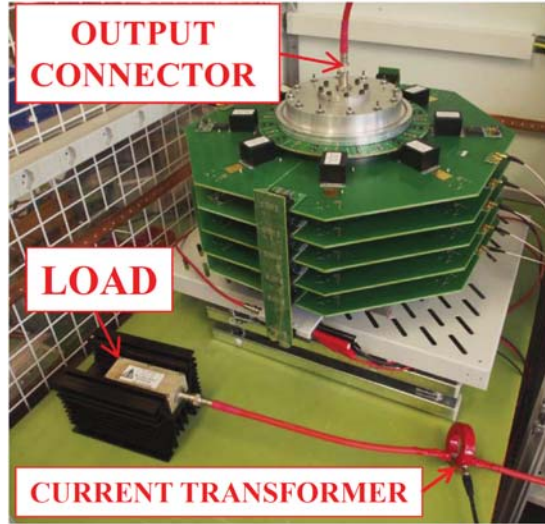


Figure 5.10. The five layer prototype inductive adder with a load and a current transformer.

yser [155]. The measured load impedance is shown in Fig. 5.12 and it is $49.7\text{--}50.2\ \Omega$ in the bandwidth of 2 to 30 MHz. The real part of the load impedance was $49.97\text{--}50.02\ \Omega$ in the same bandwidth, and the imaginary part of the load impedance decreased from $0.06\ \Omega$ at 2 MHz to $-0.66\ \Omega$ at 30 MHz. In the measurements shown in this dissertation, the measured load current was converted to the load voltage directly by multiplying the current by $50\ \Omega$. According to [92], the conversion factor of the Bergoz CT-E0.1-B current transformer is $0.05\ \text{V/A}$ when terminated in $50\ \Omega$, and therefore the signal from the current transformer was converted to the load voltage in the oscilloscope by multiplying it by 1000. The sensitivity of the input channel of the oscilloscope was set to the maximum applicable value in each measurement, to maximise the resolution of the ADC of the oscilloscope.

The pulse capacitors of the inductive adders were charged with a Heinzinger PNChp 1 kV, 2 A, high-precision, high-voltage power supply [156]. The specified stability of this power supply is better than 0.001 % of the nominal voltage over eight hours. The DC voltage for gate drive circuits and an external trigger amplifier were generated with PL303QMTP and PL303QMD laboratory power supplies from Aim & Thurlby Thandar Instruments [157], respectively. The trigger pulses for the constant voltage layers of the inductive adders were generated with a TG5011 function generator manufactured by Aim & Thurlby Thandar Instruments [158]. In the measurements in which the active analogue modulation was applied, another similar function generator was used to generate the con-

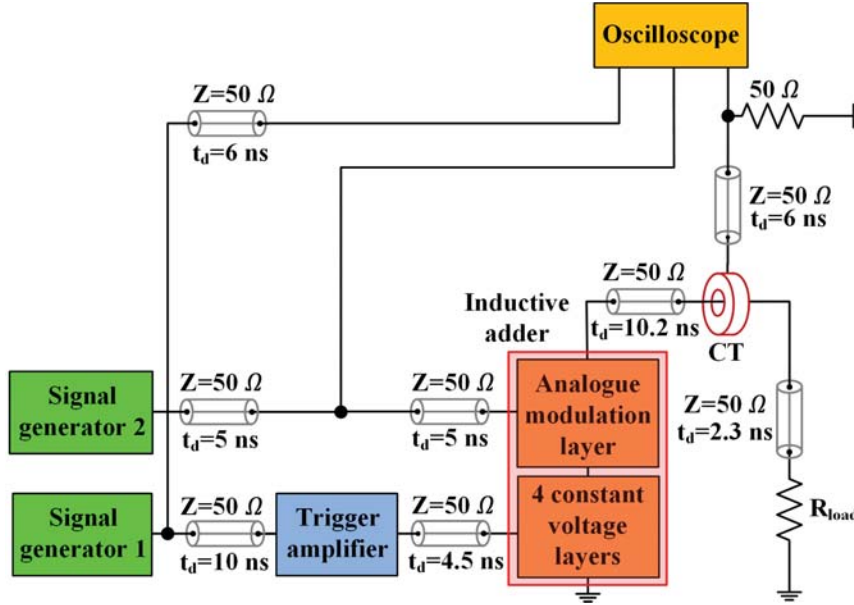


Figure 5.11. Schematic of the measurement set-up with the five layer prototype inductive adder with the active analogue modulation layer, a current transformer (CT), an oscilloscope and the cables with characteristic impedances and delays.

trol signal for the RF power transistor of the analogue modulation layer. Unless mentioned otherwise, the trigger pulses for the MOSFETs of the constant voltage layers were amplified by a trigger amplifier, designed at CERN, which could feed up to nine $50\ \Omega$ trigger lines with up to 10 V trigger pulses [159]. Each half-layer PCB of the constant voltage layers comprises a single trigger line.

In the measurements shown in Appendix B, the second prototype inductive adder was equipped with a DC reset and biasing circuit, which allowed to bias the magnetic cores of the adder between the pulses. The DC reset and biasing circuit was built using a DC power supply and a

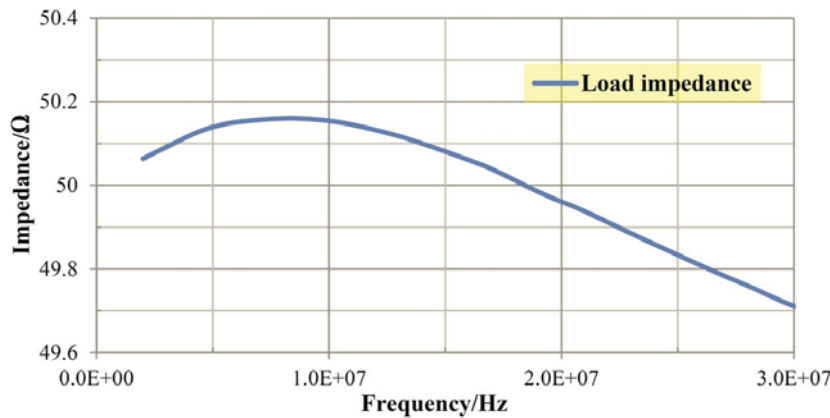


Figure 5.12. The measured impedance of the Diconex load. Revised after [155].

large insulating inductor, similarly to [71]. The difference in the reset and biasing circuit in comparison with the reset circuit described in [71] was that instead of connecting the inductor to the ungrounded end of the adder stack, the inductor was connected to an insulated copper wire, which was fed through the magnetic cores of the adder stack. The wire was physically fed through the screw holes, which are in the inside walls of the core housings, and normally used to tighten the bottom and top flanges together. Removal of one of the eight screws did not affect notably the electrical contact between the top and bottom flanges. The DC power supply used in the reset and biasing circuit was one channel of TTI PL303QMTP, manufactured by Aim & Thurlby Thandar Instruments [158], and the maximum biasing current was 8.0 A. The inductor was type X24246, the inductance of which was 6 mH and it was manufactured by Elektro-Apparatebau A.G. Courtelary (stopped business in 2005). The copper wire has diameter of 4 mm.

5.3 Measurements without Analogue Modulation

5.3.1 Initial Measurements on the Two Prototype Inductive Adders

Figure 5.13 shows the measured output pulse of the first prototype inductive adder in the case in which the adder stack was equipped with five constant voltage layers. These results have been published previously by the author in [17]. The pulse capacitors were initially charged to 302 V. At the time of completing this measurement, the maximum voltage of the pulse capacitors of the constant voltage layers was limited by the power supply, which was available for the tests. There was no other technical reason to restrict the charge voltage of the capacitors below the nominal design value of the prototype adder, of 700 V per layer. In this measurement, only one branch was powered in each half-layer PCB and hence the effective capacitance per layer was 24 μF .

In Fig. 5.13, V_{load} is the load voltage, I_{load} is the load current, V_{DS} is the drain-source voltage of a MOSFET switch and V_{Tr} is the trigger input voltage for a half-layer PCB. The maximum load voltage is 1.408 kV, which indicates that the voltage drop of each primary circuit was 20.4 V as an average. The maximum load current was 28.2 A and the on-state resistance of each semiconductor switch, type APT12067LFLL, is typically

0.67Ω [101]. With two parallel branches, the effective resistance is a half of that and the voltage across each switch, caused by the load current, is approximately 9.4 V. The rest of the resistive voltage drop is caused by the loop resistance of the primary circuit and the additional current through the core loss resistance. Also, the increasing magnetising current causes a voltage drop across parasitic inductances of the primary loop, as explained in Section 4.1.2. These losses cause in total 20.4 V voltage drop per layer at the beginning of the pulse, and the total voltage drop caused by these contributors increases during the pulse as the magnetising current increases. The pulse flat-top length is 300 ns. The rise and fall times of the pulse voltage, from 0.1 % to 99.9 %, are less than 100 ns. The droop of the pulse flat-top is 21.2 V, corresponding to 1.5 % of the maximum voltage. The output waveform in Fig. 5.13 is relatively clean. The ripple in the output voltage is approximately ± 5 V, which corresponds to ± 0.36 %. The ripple of the output waveform mainly consisted of random noise, i.e. the noise is not synchronised with the pulse. Based on simulations studies presented in Chapter 4, the inductive adder should not generate asynchronous ripple and therefore, the ripple was most probably coupled to the measurement set-up from outside rather than generated by the inductive adder.

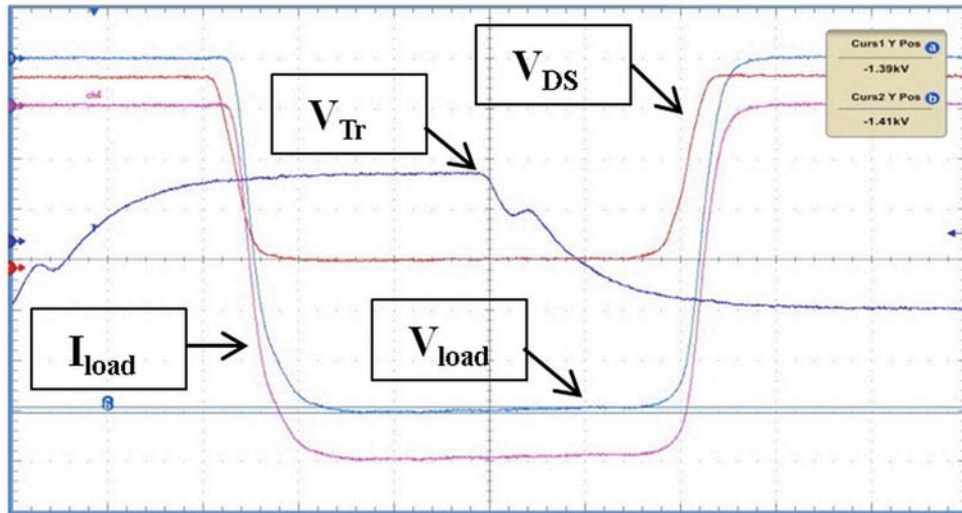


Figure 5.13. V_{load} (light blue), I_{load} (purple), V_{DS} (red) and V_{Tr} (dark blue) of the prototype inductive adder with five layers ($24 \mu\text{F}/\text{layer}$), with $V_{Ci} = 302$ V. No modulation applied. Time scale is 100 ns/div and vertical scale 200 V/div for V_{load} , 4 A/div for I_{load} , 80 V/div for V_{DS} and 3.0 V/div for V_{Tr} .

For comparison, Fig. 5.14 presents the measured output waveform of Fig. 5.13 with a simulated output pulse presented in Fig. 4.21 in Section 4.5. The simulated waveform is for a 5-layer inductive adder, the param-

eters of which were similar to the prototype inductive adder. The capacitance per layer was $24 \mu\text{F}$ and the initial voltage of the capacitors was 302 V. The linearised magnetising inductance was expected to be $10 \mu\text{H}$ and core loss resistance 27.5Ω , based on assumptions presented for magnetic cores of the prototype inductive adders in Section 5.1.2. The measured output voltage of Fig. 5.13 is also shown on Fig. 5.14.

The maximum load voltage of the simulated output pulse (Fig. 5.14) is 1.434 kV and the droop of the pulse flat-top is 21.1 V for 160 ns duration. This corresponds to 1.5 % of the pulse voltage. By comparing the load voltages shown in Fig. 5.14, a conclusion can be drawn that the measured waveform, especially the droop of the pulse, is in reasonable agreement with the prediction, given by the simulation. The parameters used in the simulation were based partly on data sheets and partly on measured parameters of the components. The difference can be caused, for example, by a combination of small discrepancies of the inductance of the magnetic cores, the switch resistance during turn-on and the load resistances in the model. All these parameters were not measured.

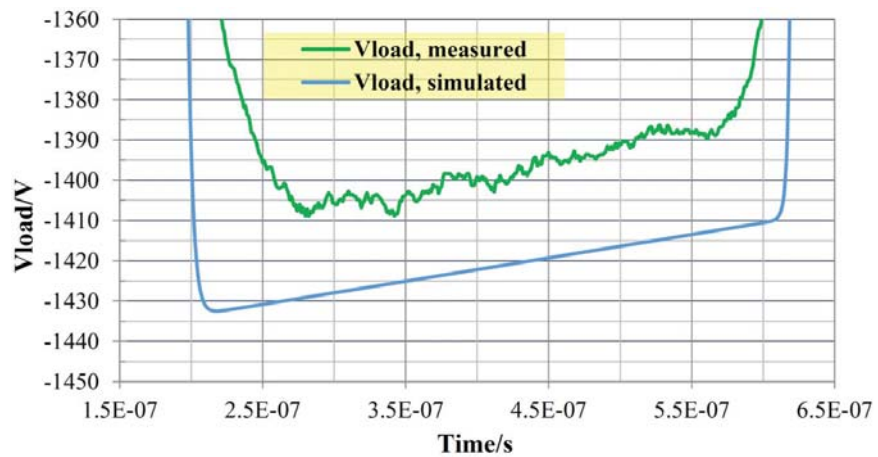


Figure 5.14. Simulated (green) and measured (blue) V_{load} with five layers ($24 \mu\text{F}/\text{layer}$) and with $V_{\text{ci}} = 302 \text{ V}$.

In the above measurements, the supply voltage for the gate drivers was 10 V and therefore the rise time of the output pulse was longer than it would have been with a higher gate driver voltage. A few measurements were also done using higher gate supply voltages and the rise time was reduced from approximately 100 ns to 30-40 ns with 14.5 V. The specified rise and fall times given for the APT12067LFL MOSFET switch are 19 ns [101], however these have been measured with a gate resistance of 0.6Ω . In the prototype adder, the gate resistance was 5Ω , in order to avoid possible oscillations. This choice probably increased the minimum

rise and fall times. However, the rise and fall times are not emphasised in the measurements shown in this dissertation because, as explained in Chapter 2, the main goal was to find a suitable pulse power modulator topology to reach the flat-top stability specifications. Therefore, the detailed measurements of the shortest reachable rise and fall times of the prototype inductive adders, by applying higher gate supply voltage than what was used in the measurements shown in this chapter, are not included in this dissertation.

5.3.2 Measured Output Waveform with Nominal Output Voltage

Subsequently, a 1 kV power supply was used and the output voltage range of the first 5-layer prototype inductive adder was tested by increasing the initial voltage of the pulse capacitors gradually up to 762 V per layer. With this initial voltage, an output voltage of 3.518 kV was reached. The measured load voltage is shown in Fig. 5.15. However, the flat-top of the load voltage is clearly degraded due to rapidly increasing magnetising current. The droop of the pulse flat-top in Fig. 5.15 is 120 V for 166 ns duration. Also in this measurement, only two branches were powered per layer, which made the current through a single MOSFET relatively high. The estimated current flow through a single MOSFET is 57 A at the end of the pulse flat-top. This is computed by taking half of the sum of the load current, 70 A, the estimated current through the core loss resistance, approximately 26 A, and the magnetising current at the end of the pulse flat-top, approximately 17 A. In this calculation, the core loss resistance is assumed to be 27.5Ω and the magnetising inductance $10 \mu\text{H}$, as given in Table 4.1 in Chapter 4. The rise time of the load voltage in Fig. 5.15 is 158 ns from 0.1 % to 99.9 %. In Fig. 5.15, the pulse flat-top is taken from the maximum value of the load voltage and the flat-top duration is 166 ns. The fall time, 149 ns, is measured from near to the end of the pulse flat-top, shown by a cursor in Fig. 5.15, to 0.1 % of the maximum pulse voltage.

5.3.3 Evaluation of the Magnetic Cores for the CLIC DR Extraction Kicker Inductive Adder

All the measurements presented in this chapter were carried out using the Vacuumschmelze magnetic cores type W567 in the prototype inductive adders. The reason for this was long delivery times of custom-sized tape-

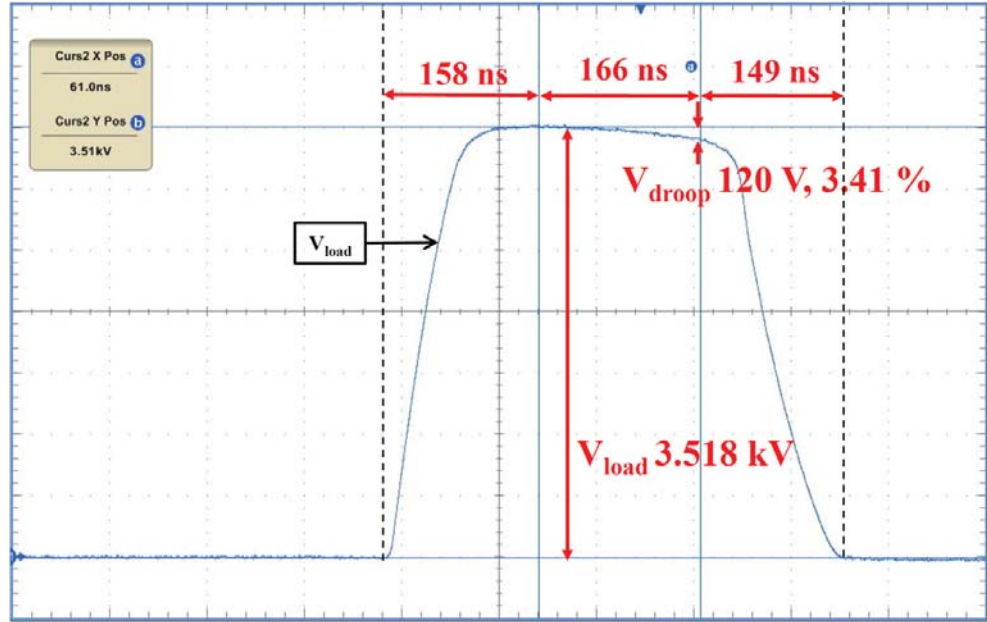


Figure 5.15. Measured V_{load} with five layers ($24 \mu\text{F}/\text{layer}$), with $V_{ci} = 762 \text{ V}$.

wound cores, typically several months, as well as difficulties in finding cores, which have large usable flux-swing, adequate insulation between the ribbon turns, high inductance at high frequencies and relatively low losses. However, six different core materials were studied with the prototype inductive adders, in order to find the most suitable magnetic core material for the CLIC DR kicker inductive adder, regarding the requirements for the flat-top stability of the output pulses. This evaluation study is presented in detail in Appendix B of this dissertation.

The evaluated core materials were the following: Finemet FT-3L [160] nanocrystalline material by Hitachi-Metals [161], annealed amorphous alloys Metglas 2605CO [111], 2605HB1M [162] and 2605SA1 [163] manufactured by Metglas (Now part of Hitachi-Metals) [164] and an amorphous core made by Permagan [165]. The reference cores were Vacuumschmelze W567 [136], which were used in most of the measurements presented in this dissertation.

Measured Magnetising Inductances and Loss Resistances of the Cores

Table 5.2 gives a summary of the measurements on the loss resistance and magnetising inductance of the candidate cores. In the table, V_{ci} is the initial capacitor voltage of the single layer of the inductive adder and I_b is the applied biasing current. $I_{Lm,max}$ is the magnetising current at the time when the pulse was terminated, and t_p is the pulse duration until $I_{Lm,max}$ was reached. R_c is the estimated core loss resistance, L_m

is the magnetising inductance and μ_r is the relative permeability of the core material. Two values, estimated minimum and maximum, are given for parameters L_m and μ_r . The maximum values are estimates for the beginning of the pulse, immediately after the stepwise rise of the current into the core loss resistance, and the minimum values are estimates at the time when the magnetising current reaches $I_{Lm,max}$.

Table 5.2. Measured core loss resistance and magnetising inductance of candidate magnetic cores for the prototype inductive adders.

Core	V_{ci} (V)	I_b (A)	$I_{Lm,max}$ (A)	t_p (μs)	R_c (Ω)	L_m (μH) max min	μ_r $\times 10^3$ max min
Finemet	700	0	100	0.9	25.0	110 0.9	57.6 0.5
FT-3L	700	8	100	1.7	25.1	40.1 1.9	21.1 1.0
Metglas	700	1	100	3.3	6.2	n/a* 39.5	n/a* 16.6
2605CO	700	8	100	3.5	6.3	n/a* 39.4	n/a* 16.5
Metglas	700	1	100	1.1	8.4	12.7 7.4	6.3 3.7
2605HB1M	700	8	100	2.4	8.6	29.2 10.1	14.6 5.0
Metglas	700	1	100	2.1	8.4	n/a* 5.2	n/a* 2.6
2605SA1	700	8	100	2.6	8.3	36.2 3.3	18.0 1.6
Permagan	700	1	100	0.5	10.5	7.4 3.8	2.6 1.4
Sample 1	700	8	100	3.8	10.6	n/a* 10.9	n/a* 3.9
Vacuum-	500	0	100	0.6	25.3	4.9 0.8	4.8 0.8
schmelze	700	8	100	1.1	24.8	16.0 1.4	16.0 1.4
W567							

* Maximum L_m cannot be defined because I_{Lm} did not increase monotonically during the pulse

Estimate of Core Losses for the CLIC DR Extraction Kicker Inductive Adder

The core losses in the nominal operating conditions for the CLIC DR inductive adder kicker were evaluated based on the measurements of the core loss resistance, shown in the previous section. Table 5.3 summarises the results for each type of the evaluated cores. In the table, V_c is the core volume, $R_{c,meas}$ is the measured core loss resistance, P_c/cm^3 is the core losses per volume unit and P_c is the estimated core losses per core. For comparison, the estimated core loss resistance, $R_{c,comp}$, which is com-

puted by Eq. (3.15) shown in Chapter 3, is also given for each core. The core losses have been estimated for the nominal operating conditions of the CLIC DR inductive adder, namely assuming the initial voltage of the pulse capacitors in each layer to be 700 V and pulse duration to be $1.1 \mu\text{s}$, which includes 900 ns pulse flat-top, 100 ns settling time and a total of 100 ns of rise and fall times, and assuming pulse repetition rate of 50 Hz. The voltage drop, caused by the resistive losses in the primary circuit, and inductive voltage drop, caused by the increasing magnetising current flowing through the parasitic loop inductance in the primary circuit, as well as the drop of the capacitor voltages, are neglected. Therefore, the loss estimates given in Table 5.3 can be considered as the worst case, the maximum, core loss estimates.

In Table 5.3, Finemet FT-3L has the smallest loss, 1.1 W per core, and Metglas 2605CO the highest loss, 4.3 W per core. The detailed estimate of the thermal resistance of the core housing of an inductive adder cell has not been included in this dissertation, however, it is assumed that the core losses of up to a few Watts would not require forced cooling of the adder stack. The core housings of the prototype inductive adders were made of aluminium, which has good thermal conductivity, approximately $240 \text{ W}/(\text{m}\cdot\text{K})$ for temperature range $0\text{-}100^\circ\text{C}$ [166]. Also, the magnetic materials of the cores are expected to have relatively high thermal conductivities. However, the cores need to be insulated with a insulating coating or by insulating tape, which will considerably increase the thermal resistance between the magnetic core and the aluminium housing. To give an example, the thermal conductivity of a polyester tape with 5.5 kV breakdown voltage, with which the evaluated custom-made cores were coated before placing them in an inductive adder cell, is $0.15\text{-}0.40 \text{ W}/(\text{m}\cdot\text{K})$ at 23°C , depending on the voltage [167]. However, measurements of the temperature increase of the cell and the core are left as a subject for further studies.

Selection of the Core Material for the CLIC DR Extraction Kicker Inductive Adder

Based on the evaluation of the cores, the most suitable core materials for the CLIC DR kicker inductive adder would be Finemet FT-3L and Vacuumschmelze Vitroperm 500 F (shown as W567 in Table 5.2). Based on the measurements shown in Appendix B (especially in Fig. B1 and Fig. B2), the cores made of these materials have very linear B-H curves. Also, according to Table 5.2, if biasing is not applied, the pulse duration is

Table 5.3. Estimated core losses per core and per unit volume for the cell of the CLIC DR kicker inductive adder cell for nominal operating conditions.

Core	V_e (cm ³)	$R_{c,meas}$ (Ω)	$R_{c,comp}$ (Ω)	P_c/cm^3 *	P_c *
Finemet FT-3L	340	25.1	67.4	3.16	1.08
Metglas 2605CO	421	6.3	39.6	10.1	4.27
Metglas 2605HB1M	346	8.6	33.2	9.08	3.14
Metglas 2605SA1	346	8.3	34.5	9.37	3.24
Permagan Sample 1	404	10.6	n/a	6.30	2.54
Vacuumschmelze W567	203	24.8	27.5	5.36	1.09

* Operating conditions: $V_{ci} = 700$ V, $t_p = 1.1$ μ s and $F_r = 50$ Hz

approximately half of the maximum pulse duration with biasing, which means that approximately a half of the usable range of the B-H curve remains available without biasing. This means that the remanent magnetic field is low for these cores. Also, according to Table 5.3, these cores have the highest equivalent, parallel, loss resistances and, therefore, lowest losses per core and per volume unit. Finemet FT-3L has an advantage of considerably higher magnetising inductance in comparison with Vacuumschmelze W567, as can be seen in Table 5.2. Also, Vacuumschmelze cores are not available in custom-made sizes, except in very large quantities [137]. Therefore, Finemet FT-3L is the recommended core material for the CLIC DR kicker inductive adder.

A point to note is that each of the evaluated core materials is suitable to be used in an inductive adder. However, except for the Finemet FT-3L and Vacuumschmelze W567 cores, reset and biasing need to be applied for the cores. Considerably higher losses for material 2605CO in comparison with other core materials may require that a forced air cooling or liquid cooling is applied with these cores for high repetition rates. Also, the large loss current, which is caused by the high losses of this core material, needs to be taken into consideration in defining the current rating for the

semiconductor switches. The higher current would also increase the droop that needs to be compensated.

5.4 Measurements with Passive Analogue Modulation

According to simulation studies presented in Chapter 4, analogue modulation is a promising means to reach the desired flat-top stability required for the CLIC DR kicker system. The author presented simulation results of applying the analogue modulation method for compensating the droop of the output waveform of the CLIC DR kicker inductive adder in [9] and [10]. In addition, the author presented in [17] initial measurements on applying the passive analogue modulation to compensate the droop of the output pulse of the first prototype inductive adder at CERN. The results are briefly summarised in the next section and completed with the measurements, in which the droop of the output waveform is practically fully compensated.

5.4.1 Initial Measurements with Passive Droop Compensation

Figure 5.16 shows the load voltage waveforms of the first prototype inductive adder with (red) and without (blue) passive analogue modulation. In these measurements, the passive analogue modulation layer was implemented by modifying a constant voltage layer of the prototype inductive adder. For the initial measurements presented in this section, the pulse capacitors of a half-layer PCB were short-circuited by a wire and resistor R_a was connected on a PCB by using simple alligator connectors. Later, for the measurements which are presented in the following sections of this dissertation, the short-circuited capacitors of a modified constant voltage layer were removed and the resistor R_a was soldered on a PCB, to ensure good electrical contact.

In the measurement without the analogue modulation layer, shown as the blue curve in Fig. 5.16, the prototype inductive adder was equipped with four constant voltage layers in which the pulse capacitors were initially charged to 270 V, which would ideally give a load voltage of 1080 V. The primary of the fifth layer was short-circuited. In Fig. 5.16, the maximum measured load voltage without the analogue modulation is 1.025 kV. The resistive losses and the voltage drop across the primary loop inductance per layer can be estimated by subtracting the measured maximum

load voltage, 1.023 kV, from the ideal load voltage, 1.080 kV, and dividing the difference, 55 V, by four layers. This gives 13.8 V per layer at the beginning of the pulse, at time point 280 ns in Fig. 5.16. The pulse flat-top duration is 350 ns. In Fig. 5.16, the droop of the load voltage, in the case when the passive analogue modulation was not applied, is 12.9 V over the 160 ns flat-top between 300 ns and 460 ns, which corresponds to 1.3 %.

The red curve in 5.16 shows the measured load voltage waveform for the prototype inductive adder in the case when the adder stack was equipped with four constant voltage layers, each charged to 285 V, and a passive analogue modulation layer. The resistor R_a of the analogue modulation layer was 4.4Ω . The maximum voltage of the output pulse is 1.002 kV and the length of the pulse flat-top is 350 ns. In Fig. 5.16, the droop in the case when the passive analogue modulation was applied is 6.9 V over 160 ns flat-top duration between 300 ns and 460 ns, which corresponds to 0.7 % of the pulse voltage. This is just over half of the droop of the pulse flat-top when it was not compensated with the passive analogue modulation, as is visible in Fig. 5.16. Although the resistor value of the passive modulation layer was not optimised here, it is demonstrated that the passive analogue modulation is an effective and straightforward means to compensate droop of the load voltage.

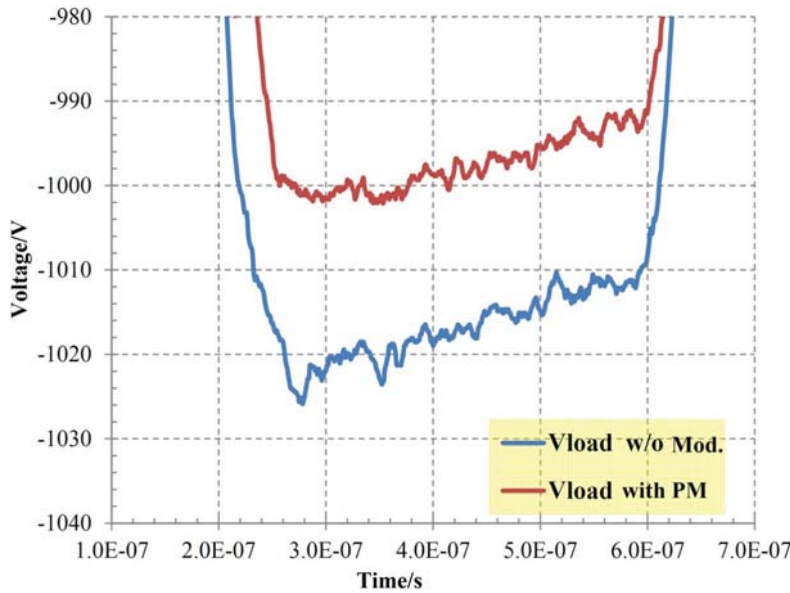


Figure 5.16. Measured V_{load} waveforms with four constant voltage layers with $V_{ci} = 270$ V (fifth layer short-circuited) (blue), and with four constant voltage layers with $V_{ci} = 285$ V and with a passive analogue modulation layer ($R_a = 4.4 \Omega$) (red).

5.4.2 Measurements with Optimised Passive Droop Compensation

Figure 5.17 shows the measured load voltage waveform for the prototype inductive adder in the case when the resistor value of the analogue modulation layer was optimised to compensate the droop of the pulse flat-top completely. In this measurement the adder stack was equipped with four constant voltage layers, each charged initially to 350 V, and a passive analogue modulation layer. The resistor R_a of the analogue modulation layer was $7.96\ \Omega$. The maximum voltage of the output pulse is 1.18 kV and the total duration of the pulse flat-top is 800 ns. The droop of the pulse flat-top in Fig. 5.17, for 160 ns, is practically zero but its value cannot be defined because of the shape of the flat-top. The ripple of the pulse waveform is $\pm 1.9\text{ V}$, which corresponds to $\pm 0.16\%$ of the pulse voltage. The waveform in Fig. 5.17 is an average of 100 measured waveforms, which means that each data point of the waveform is computed as an average of 100 consecutive pulses. This method, called ensemble averaging, effectively reduces random noise and ripple of the measured waveform and increases the effective resolution of the ADC of the oscilloscope. The method has been discussed in detail in Section 2.4.

The measurement of output voltage with the passive droop compensation was repeated with different initial charge voltages for the pulse capacitors of the constant voltage layers. With 300 V of initial charge the output voltage was 1.009 kV and the flat-top stability for 160 ns pulse flat-top was $\pm 1.68\text{ V}$ ($\pm 0.17\%$). With 400 V of initial charge the output voltage was 1.344 kV and the flat-top stability was $\pm 2.68\text{ V}$ ($\pm 0.20\%$). These values were also measured for averages of 100 pulses. The section of the flat-top, for which the droop was visually the smallest, moved along the pulse, when the initial charge of the pulse capacitors of the constant voltage layers was increased.

The limitation of the passive analogue modulation is that the value of the resistor R_a needs to be adjusted according to the output voltage, in order to maximise the compensation effect and therefore to generate a pulse without droop. If the initial voltage across the storage capacitors is changed, the output voltage changes, which changes the compensation effect of the analogue modulation layer. This may cause either positive or negative slope of the top of the output pulse. Also, the ripple of the flat-top pulse cannot be easily reduced with a passive analogue modulation

layer. On the contrary, the active analogue modulation method provides a flexible means for adjustable droop and ripple compensation, as is shown in the following sections.

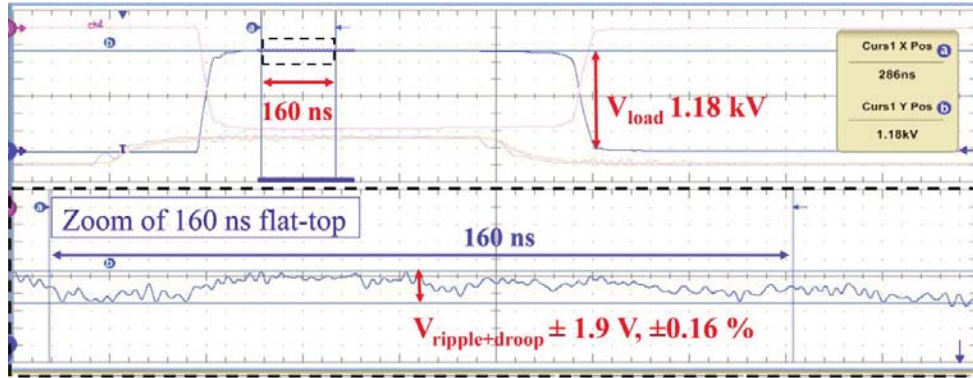


Figure 5.17. Measured V_{load} waveform with four constant voltage layers with $V_{ci} = 350$ V and with a passive analogue modulation layer ($R_a = 7.96 \Omega$). The upper figure is the complete pulse voltage and the lower figure is a zoom of 160 ns duration of the pulse flat-top.

5.5 Measurements with Active Analogue Modulation

The active analogue modulation method allows to modulate the output waveform of the inductive adder with a defined control signal. This method can be used to compensate both the droop and ripple of the output waveform. The following sections present the step-by-step approach for applying the active analogue modulation to compensate the droop and ripple of the output waveform, starting with defining the modulation range, then continuing with active compensation of the droop, and then describing the active generation of high-frequency components for the output waveform, and finally compensation of both the droop and a high-frequency ripple component. The author presented briefly the results of measurements of applying active analogue modulation to compensate the droop and ripple of the output waveform of the prototype inductive adder in [18]. These results are also repeated in the following sections in detail.

5.5.1 Modulation Range of the Active Analogue Modulation Layer

The operation range of the active analogue modulation layer is defined by the resistance range of the parallel connection of the resistor R_a and the output (drain-source or collector-emitter) of the RF power transistor.

Fig. 5.18 shows a measured output waveform of the prototype inductive adder with the active analogue modulation applied. The pulse capacitors in the constant voltage layers were initially charged to 550 V and the pulse flat-top duration was close to 300 ns. In this measurement the resistor R_a was 7.96 Ω . The red curve is measured in the case in which the RF power transistor is not biased and it is not conducting. In this case the maximum voltage of the output waveform is defined by the parallel circuit of resistors R_a and R_c of the analogue modulation layer according to Eq. (3.3). The blue curve in Fig. 5.18 is measured for the case in which the RF power transistor was DC biased with 16 V. Beyond 16 V the on-state resistance of the RF power transistor did not change. In this case the resistance of the parallel circuit of the resistor R_a , the resistor R_c and the RF power transistor is lower than in the case in which the RF power transistor was not conducting, and according to Eq. (3.3), the maximum output voltage is higher. Both curves in Fig. 5.18 were computed as an average of 10 measured pulses, in order to partially attenuate random, asynchronous, ripple of the pulse.

In Fig. 5.18, the difference between the blue and red curves gives the modulation range for the active analogue modulation. In Fig. 5.18, the maximum value of the 280 ns pulse flat-top which is modulated with active analogue modulation, shown in blue colour, is 1.975 kV. The maximum value of the pulse flat-top which is modulated with passive analogue modulation, shown in red colour, is 1.815 kV. Thus the modulation range for the active analogue modulation, is in total 160 V. The output voltage is between these limits depending on the biasing voltage and the control voltage which are applied for the RF power transistor. In this measurement, the total modulation range was 8.1 % of the maximum voltage of the pulse with analogue modulation.

Sections 5.5.2 and 5.5.4 present results of measurements in which the active analogue modulation was applied to compensate the droop and ripple of the output waveform of the prototype inductive adder. In the measurement set-up which was built for this dissertation, there was not an amplifier between the signal generator and the DC blocking capacitor connected to the gate pin of the RF power transistor of the analogue modulation layer, as shown in the schematic in Fig. 5.8. The DC biasing voltage for the RF power transistor was fed from a static DC power supply and the signal generator supplied only the high-frequency modulation signal for the power transistor. For this reason, the maximum modulation range

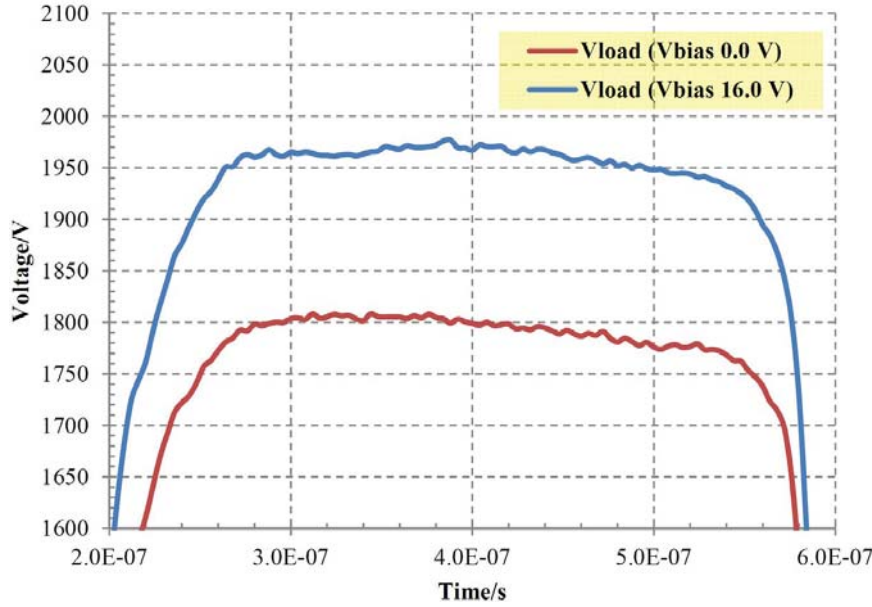


Figure 5.18. Measured V_{load} with four constant voltage layers with $V_{ci} = 550$ V and with an analogue modulation layer ($R_a = 7.96 \Omega$). $V_{Bias} = 0.0$ V (red) and $V_{Bias} = 16.0$ V (blue).

was defined by the current and voltage range of the signal generator and according to measurements, it was approximately one third of the total modulation range shown in Fig. 5.18.

5.5.2 Active Droop Compensation

The red curve in Fig. 5.18 is effectively the output waveform of the prototype inductive adder for the case in which the analogue modulation layer is operating in the passive mode. The biasing voltage for the RF power transistor is zero and it is not conducting. The droop of this curve is the starting point for adjusting the active analogue modulation to cancel the remaining droop. The droop of the red curve in Fig. 5.18, for 160 ns flat-top duration from 340 ns to 500 ns, is 24 V (1.3 %). The goal of applying the active droop compensation was to reduce this droop practically to zero.

Figure 5.19 shows the output waveform of the prototype inductive adder for the cases when only a biasing DC voltage of 6.0 V is applied to the RF power transistor (red), and when both the biasing DC voltage and a compensating ramp function is fed to the RF power transistor (blue). In this measurement, the initial voltage across the capacitors of the constant voltage layers was 551 V. The red curve in Fig. 5.19 is clearly rounded and, effectively, during the first half of the pulse the asymptotic voltage change is positive and then during the second half it is negative. The combined

droop and ripple of the pulse, when the RF power transistor is only DC biased, is over 30 V (1.7 %) between 300 ns and 500 ns. The blue curve in Fig. 5.19 is the measured output voltage in the case in which the active droop compensation was applied. The control signal was a piecewise linear exponential curve, which was defined experimentally. This curve is shown in Fig. 5.27. To define the compensation ramp, at first a ramp function with a constant gradient was applied as a compensation signal, and the amplitude of the ramp was trimmed until the voltage of the end point of the pulse flat-top was the same as the voltage of the starting point of the pulse flat-top. This approach lead to a rounded flat-top, which was then improved further by applying more complicated, piece-wise linear, functions. The blue curve in Fig. 5.19 has a clear flat-top which is over 210 ns long. The maximum voltage is 1.817 kV and the flat-top stability for 210 ns duration is 4.36 V, corresponding to ± 0.12 % of the maximum flat-top voltage. The blue curve is an average of 200 measured pulses.

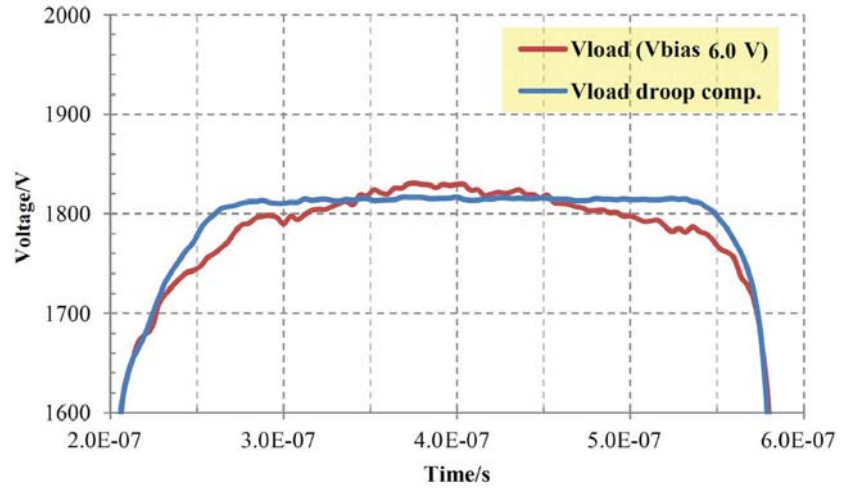


Figure 5.19. Measured V_{load} with four constant voltage layers with $V_{ci} = 551$ V and with an active analogue modulation layer ($R_a = 7.96 \Omega$), with 6.0 V DC biasing only (red) and compensating control signal (blue).

Figure 5.20 shows the measured load voltage waveform for the prototype inductive adder with four constant voltage layers and an analogue modulation layer with optimised droop compensation. The pulse capacitors in the constant voltage layers were initially charged to 553 V and the pulse flat-top duration was set close to 300 ns. The analogue modulation layer was operating in active mode, the control signal was a piecewise linear exponential curve (Fig. 5.27) and the DC biasing voltage for the RF power transistor was 6.0 V. The upper curve in Fig. 5.20 shows the load voltage of the inductive adder. The maximum voltage of the pulse is 1.823 kV.

The lower curve is a zoom-in of the pulse flat-top for 160 ns duration. The droop of the pulse flat-top is negligible and, therefore, the droop can be considered as fully compensated with the active analogue modulation. The flat-top stability of the pulse waveform is ± 1.23 V, which corresponds to ± 0.07 % (more precisely 0.067 %) of the pulse voltage. The waveforms in Fig. 5.20 are averages of 1000 measured pulses. Fig. 5.21 shows the measured load voltage for the same set-up for an average of 4000 pulses. The flat-top stability is ± 1.17 V, which corresponds to ± 0.06 %. The repeatability of the measurements of active droop compensation was good and other measurements, with the same set-up and the same maximum output voltage, gave flat-top stabilities of ± 1.32 V (± 0.072 %) for an average of 1000 pulses and ± 1.26 V (± 0.069 %) for an average of 4000 pulses.

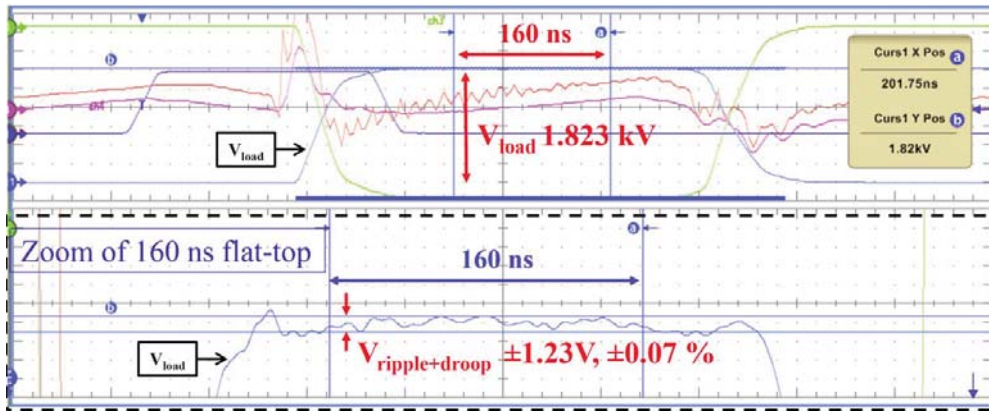


Figure 5.20. Measured V_{load} with four constant voltage layers with $V_{ci} = 553$ V and with an active analogue modulation layer ($R_a = 7.96$ Ω). $V_{Bias} = 6.0$ V and the modulating control signal is a piece-wise linear ramp. The curves are averages of 1000 pulses.

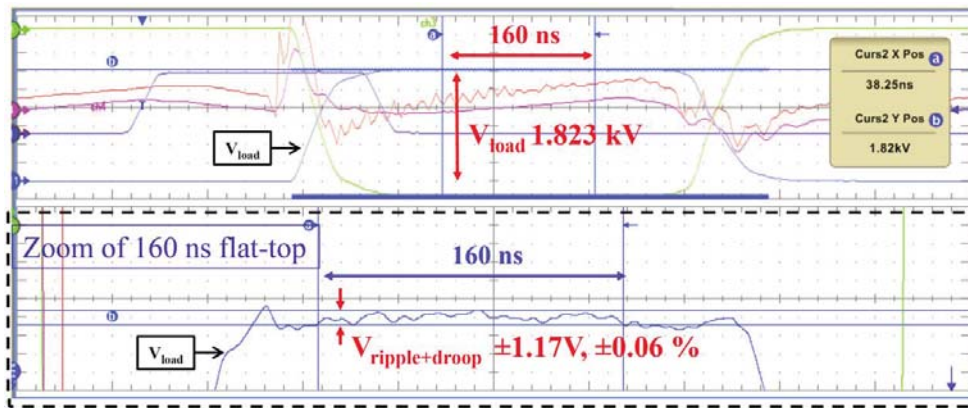


Figure 5.21. Measured V_{load} with four constant voltage layers with $V_{ci} = 553$ V and with an active analogue modulation layer ($R_a = 7.96$ Ω). $V_{Bias} = 6.0$ V and the modulating control signal is a piece-wise linear ramp. The curves are averages of 4000 pulses.

5.5.3 Active Ripple Generation

The active analogue modulation layer can be used to modulate the pulse waveform arbitrarily within the usable modulation range and bandwidth of the active analogue modulation layer. Fig. 5.22 demonstrates generation of a positive ramp and sine waves at frequencies of 2, 10 and 30 MHz on the load voltage. In these measurements, the first prototype inductive adder was equipped with four constant voltage layers. The analogue modulation layer was operating in active mode and the resistor R_a was $7.96\ \Omega$. The initial voltage of the pulse capacitors in the constant voltage layers was set to only 200 V to allow a relatively long pulse duration, 500 ns. The average voltage of the output pulses in Fig. 5.22 is approximately 700 V. The clearly visible variations on the pulse waveform were deliberately generated by the active analogue modulation layer. In the blue curve shown in Fig. 5.22, the amplitude of the positive ramp is 35 V. In the red curve there is a 75 V (peak-to-peak) sine wave at frequency of 2 MHz. The purple waveform is modulated with 10 MHz sine wave and the peak-to-peak value of the actively generated ripple component is 30 V. The green curve is modulated with a 30 MHz sine wave and the peak-to-peak value of the controlled variation of the pulse flat-top is 10 V.

The measured waveforms shown in Fig. 5.22 demonstrate that the output waveform of the inductive adder can be modulated according to a desired function by applying the active analogue modulation. Fig. 5.22 also verifies that the bandwidth of the active analogue modulation layer, of the first prototype inductive adder, is high enough for applying active ripple compensation for the output waveform. The waveforms shown in Fig. 5.22 are averages of 10 recorded output pulses and the small number of samples result in relatively high noise.

5.5.4 Active Ripple Compensation

Methodology for the Active Ripple Compensation

In order to apply the active analogue modulation method to compensate a ripple component of the output waveform, the magnitude and phase responses of the analogue modulation layer, together with cables, were measured. In these measurements, the prototype inductive adder was equipped with four constant voltage layers, the pulse capacitors of which were initially charged to 553 V. The RF power transistor of the active ana-

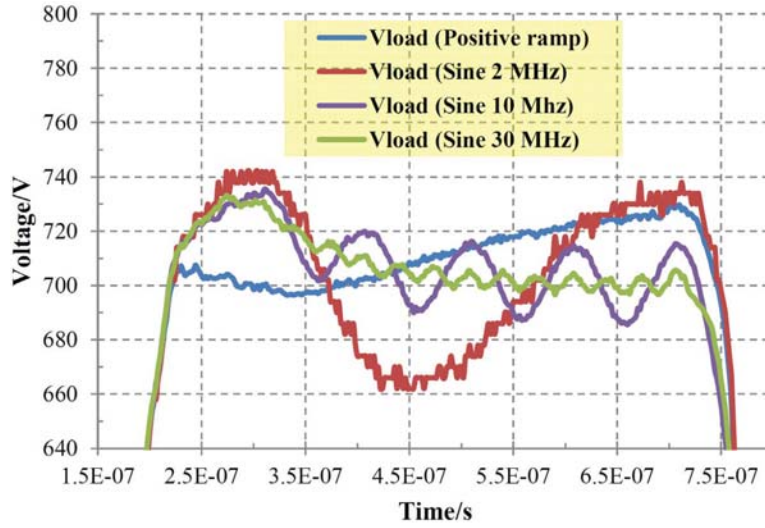


Figure 5.22. Measured V_{load} with four constant voltage layers with $V_{ci} = 200$ V and with an active analogue modulation layer ($R_a = 7.96 \Omega$). $V_{Bias} = 7.0$ V and modulating control signal is a positive ramp (blue), 2 MHz sine wave (red), 10 MHz sine wave (purple) and 30 MHz sine wave (green).

logue modulation layer was DC biased to 6.75 V. The modulating control signal was the sum of the droop compensating ramp, which was used in the measurements of active droop compensation in this chapter (Fig. 5.27), and a sine wave with a peak-to-peak voltage of 2.2 V. The frequency of the sine wave was changed from 5 MHz up to 25 MHz with 2.5 MHz increments.

The measured magnitude response, for the active analogue modulation layer of the first prototype inductive adder, is shown in Fig. 5.23 and the phase response is shown in Fig. 5.24. These plots show the gain and phase responses, respectively, of the actively generated ripple on the flat-top of the load voltage as a function of the frequency from the signal generator. These curves were used to define the correction factors for the modulation signal, which included a pre-defined sine wave to cancel a measured ripple component of the output waveform, as is shown below in this chapter. In the measurements of the magnitude and phase responses, the set-up for the active analogue modulation layer was similar to the schematic which is shown in Fig. 5.8. If the single-way delay of the cables is changed, the phase response will need to be re-measured.

The blue curve in Fig. 5.30 shows the output waveform of the inductive adder without active ripple compensation. In this measurement, the initial voltage over the pulse capacitors in the constant voltage layers was 553 V. The droop of the output waveform was compensated with active analogue modulation by applying a droop compensating ramp, similarly

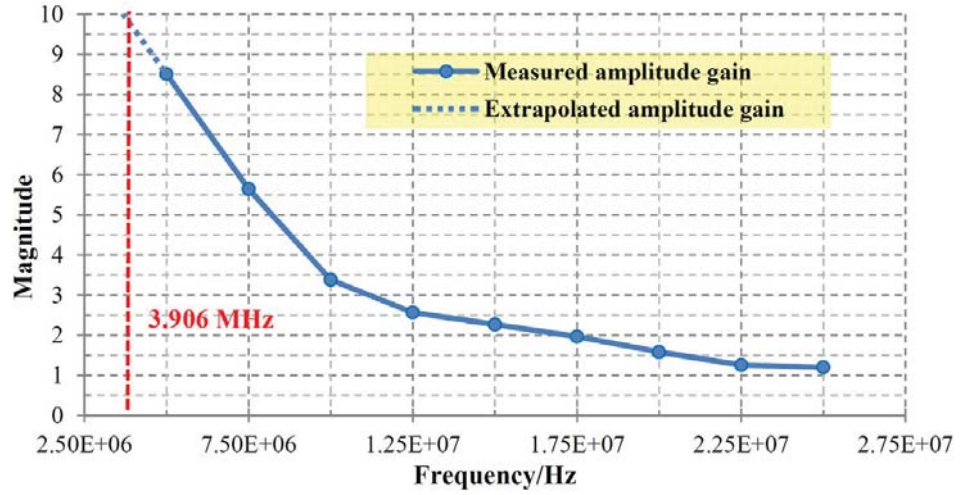


Figure 5.23. Measured magnitude response of the analogue modulation layer operating in active mode. The inductive adder was equipped with four constant voltage layers, with $V_{ci} = 553$ V, and with an analogue modulation layer ($R_a = 7.96 \Omega$). $V_{Bias} = 6.75$ V, modulating control signal was a droop compensating ramp and 2.2 V (peak-to-peak) sine wave at a frequency 5-25 MHz.

to shown in Section 5.5.4. A fast Fourier transform (FFT) was computed for the pulse flat-top shown in Fig. 5.30, in order to define the magnitudes and phases of the ripple frequencies visible in the pulse flat-top. Before computing the FFT for the output waveform, the DC offset of the pulse flat-top was removed and a windowing function was applied to the flat-top of the measured waveform.

The frequency content of the pulse flat-top was considered by taking the pulse flat-top from 99.8 % of the maximum voltage of the rising edge to 99.8 % of the maximum value of the falling edge. Three different windowing functions were evaluated, namely the Rectangular (also called a Boxcar windowing function), Hann and Blackman windows. The Rectangular window could ideally give the best frequency resolution of these three windowing functions but it is poor regarding amplitude accuracy and spectral leakage [168]. The Blackman window would result in the smallest spectral leakage but it is poor considering the frequency resolution, and the Hann window would give good frequency resolution and rather low spectral leakage but only fairly good amplitude accuracy [168]. However, the differences of the FFT magnitude and phase calculated from the three different windowing functions were very small, as is shown in Fig. 5.25 and Fig. 5.26. Finally the Rectangular windowing function was chosen.

The length of the data set for the FFT was 256 data points and the time step was 4 ns. In the measurement of the original waveform, the sam-

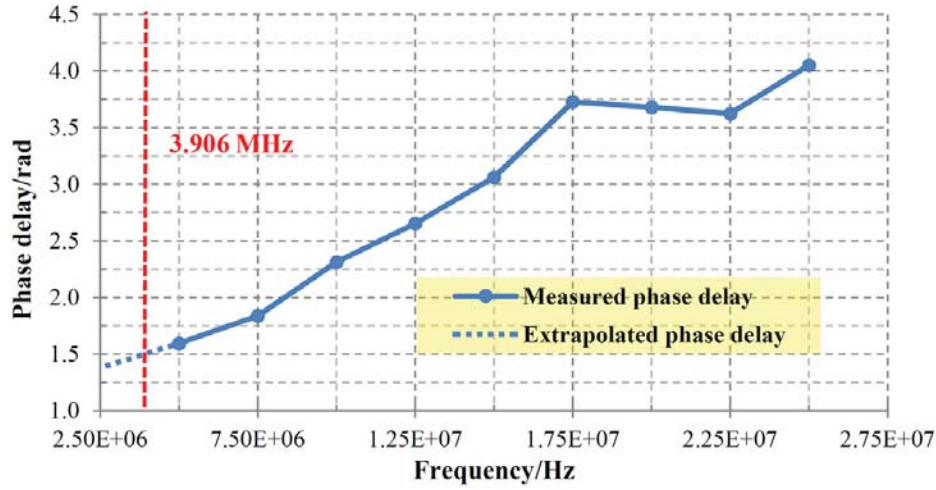


Figure 5.24. Measured phase response of the analogue modulation layer operating in active mode. The inductive adder was equipped with four constant voltage layers, with $V_{ci} = 553$ V, and with an analogue modulation layer ($R_a = 7.96 \Omega$). $V_{Bias} = 6.75$ V and the modulating control signal was a droop compensating ramp and 2.2 V (peak-to-peak) sine wave at a frequency 5-25 MHz.

pling rate of the oscilloscope was set to 1 GS/s and each data point was an average of four consecutive data samples. The frequency resolution of the FFT algorithm, $f_{Res,FFT}$, is defined by the length of the data set according to the following equation:

$$f_{Res,FFT} = \frac{1}{N_s t_s} \quad (5.1)$$

In Eq. (5.1), N_s is the number of data points in the data set and t_s is the time interval between two consecutive samples. In the measurements with the prototype inductive adders, the maximum pulse duration was limited by the cross-sectional area of the magnetic cores. The maximum pulse length was approximately 400 ns including the rise and fall times, and the duration of the flat-top was 67 samples, corresponding to 268 ns. The DC offset was removed from the pulse flat-top. The mean of the samples was computed and the resulting number was subtracted from each sample. Zero padding was applied to increase the length of the data set to 256. The frequency resolution of the FFT in Fig. 5.25 and Fig. 5.26 is 0.977 MHz.

For demonstration of the active ripple compensation, a ripple component at frequency 3.906 MHz was chosen. The computed magnitude and phase for this ripple component were 0.55 V and -1.0 radians, respectively. The compensation signal was computed, taking into consideration the magnitude and phase responses shown in Fig. 5.23 and Fig. 5.24. The frequency

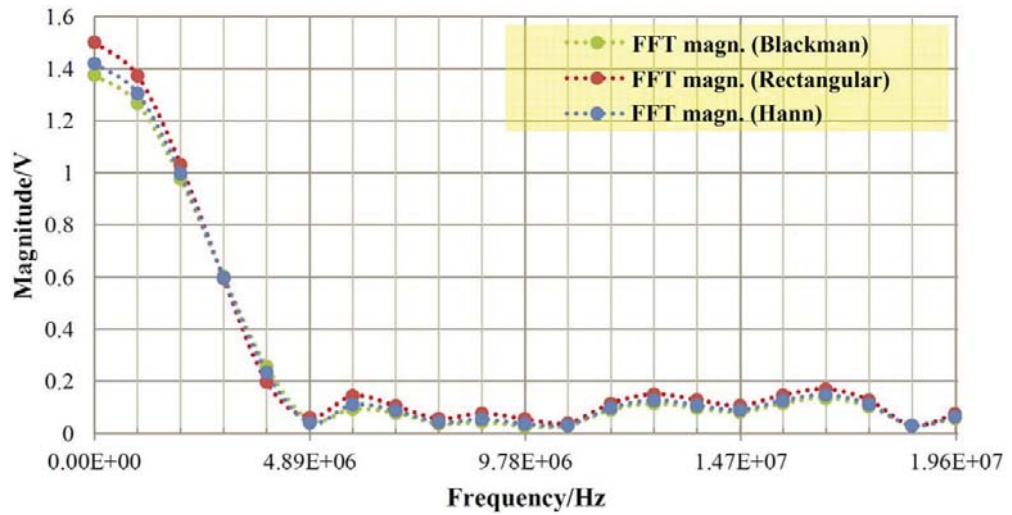


Figure 5.25. Magnitude of the fast Fourier transform for a measured load voltage of the prototype inductive adder. The FFT has been computed after applying rectangular (red), Hann (blue) and Blackman (green) windowing functions to the measured flat-top of the load voltage.

3.906 MHz is outside of the measured curves of the magnitude and phase responses, therefore the corresponding values were linearly extrapolated from the curves as is shown in Fig. 5.23 and Fig. 5.24. According to Fig. 5.23, the correction factor for magnitude was 9.8, and according to Fig. 5.24, the phase delay was 1.5 radians. Both the gain and the phase responses are quite smooth, close-to linear functions of frequency in the measured range from 5 MHz up to 10 MHz, therefore the error margin for the estimates given by the linear extrapolation is expected to be only a few percent.

The correction waveform was computed and summed to the droop compensation waveform. For a reference and to verify the measurement, another compensation waveform was created with the same frequency component but with the opposite phase. Fig. 5.27 shows the original droop compensation signal (red), the droop compensation signal with a ripple compensation waveform (blue) and the droop compensation signal with a ripple component with an opposite phase (green). These waveforms are reference signals for the signal generator and the total voltage range was set by the signal generator. In the measurements shown in Section 5.5.4, the DC biasing voltage was 6.0 V and the total voltage range of the compensation control signals shown in Fig. 5.27 was 5.895 V.

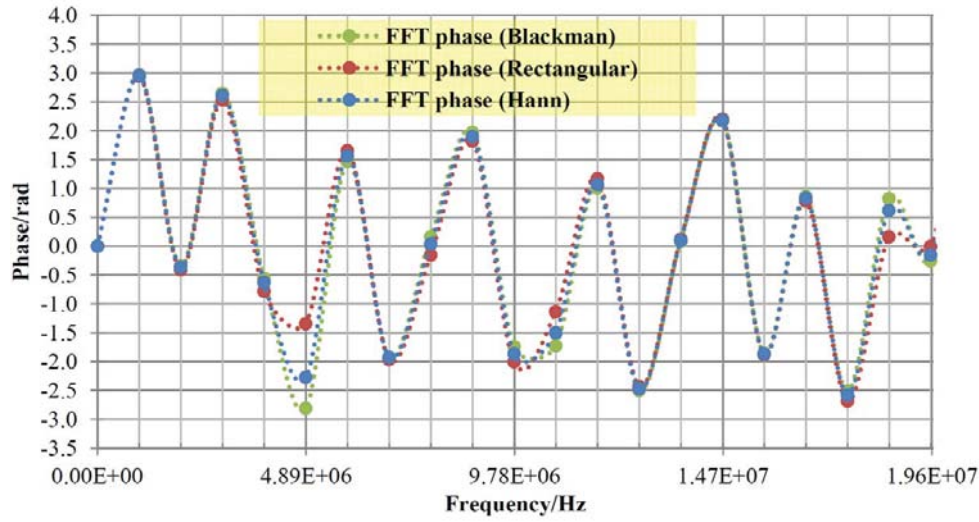


Figure 5.26. Phase of the fast Fourier transform for a measured load voltage of the prototype inductive adder. The FFT has been computed after applying rectangular (red), Hann (blue) and Blackman (green) windowing functions to the measured flat-top of the load voltage.

Application of the Active Ripple Compensation

Figure 5.28 shows the measured output waveform of the first prototype inductive adder in the case when the active ripple compensation was applied for the 3.906 MHz frequency component. The upper curve shows the load voltage and the lower curve is a zoom-in of the pulse flat-top. The measured flat-top stability is ± 0.96 V for the 160 ns duration of the zoomed period and actually it remains the same over 185 ns. The flat-top stability for a 210 ns pulse flat-top, starting from the left cursor, in Fig. 5.28 is ± 1.41 V, corresponding to ± 0.08 %. The curves in Fig. 5.28 are averages of 1000 measured pulses. The maximum value of the pulse flat-top is 1.823 kV and the absolute value of ± 0.96 V for the flat-top stability for 160 ns duration corresponds to ± 0.05 % of 1.823 kV. The measured flat-top stability is the best which was reached with the first prototype inductive adder in the measurements which were carried out for this dissertation. Another measurement with the same set-up and applying the active ripple compensation for the 3.906 MHz frequency component gave ± 1.02 V (± 0.06 %), for the averages of both 1000 and 4000 measured pulses. Therefore, increasing the number of averaged pulses from 1000 to 4000 did not improve the measured stability any further. Also in these cases, the measurements were done for 160 ns flat-top duration but the flat-top remained within ± 1.02 V up to 185-190 ns. Thus the repeatability for these three measurements of active ripple compensation was reasonably good.

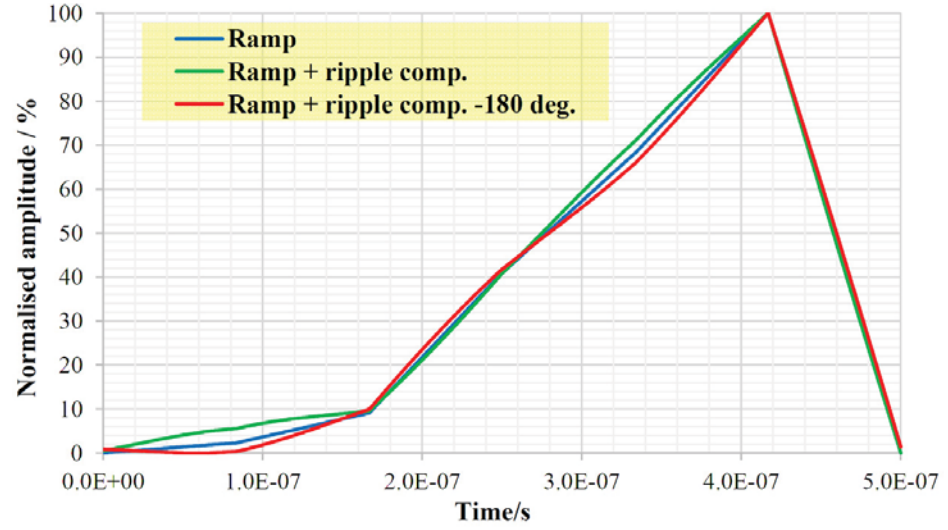


Figure 5.27. Control signals for the RF power transistor of the analogue modulation layer. Compensation ramp for cancelling the droop (blue), ramp with ripple cancelling 3.906 MHz frequency component (green) and ramp with 3.906 MHz frequency component with opposite phase (red).

For comparison, the droop of the output voltage without any compensation at 1.41 kV output pulse, shown in Fig. 5.14, is 21.2 V (1.5 %) for 300 ns flat-top duration. With passive analogue modulation, the smallest measured flat-top stability was ± 1.9 V ($\pm 0.16\%$) for 160 ns flat-top duration at 1.18 kV output voltage with R_a equals to 7.96Ω , as shown in Fig. 5.17. With active droop compensation, shown in Fig. 5.20, the best measured flat-top stability was ± 1.17 V ($\pm 0.06\%$) for 160 ns flat-top duration at 1.823 kV output voltage. However, the averaging of each measurement must be taken into consideration in comparing these values with each other. The accuracy of the measurements presented in this chapter is discussed in Section 5.6 and Table 5.4 summarises the most important measurements of this dissertation with estimated resolutions.

For comparison and to verify the experimental result of applying the active ripple compensation, another measurement was carried out with the ripple compensation component of the modulation signal delayed by 180 degrees. Effectively, if the ripple at 3.906 MHz was suppressed with the original phasing of the ripple compensation waveform, shown in green colour in Fig. 5.27, the phase delay of 180 degrees of the 3.906 MHz frequency component, which is shown in red colour in Fig. 5.27, should amplify the ripple at this frequency. Fig. 5.30 presents the waveforms of the output pulse with the original compensating ripple component (green), without active ripple compensation (blue) and with the ripple component with an opposite phase (red). Clearly, in the latter case the ripple of the

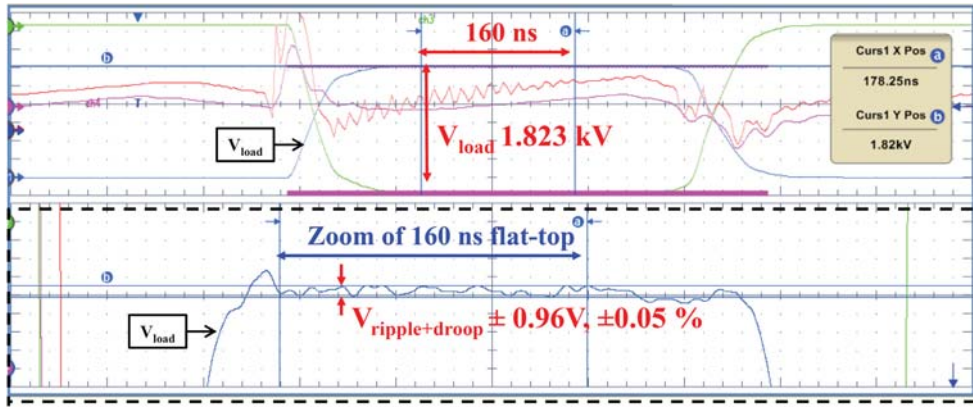


Figure 5.28. Measured V_{load} with four constant voltage layers with $V_{ci} = 553 V$ and with an active analogue modulation layer ($R_a = 7.96 \Omega$). $V_{Bias} = 6.0 V$ and the amplitude of the ramp and ripple compensating control signal was 5.895 V. The curves are averages of 1000 pulses.

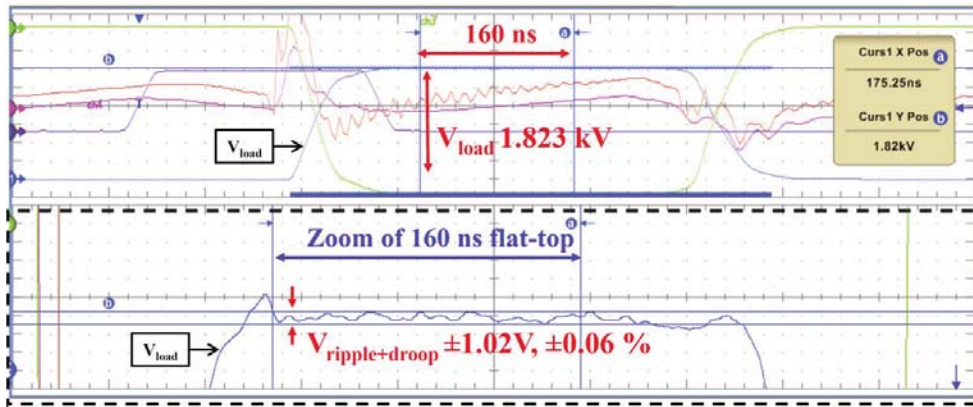


Figure 5.29. Measured V_{load} with four constant voltage layers with $V_{ci} = 553 V$ and with an active analogue modulation layer ($R_a = 7.96 \Omega$). $V_{Bias} = 6.0 V$ and the amplitude of the ramp and ripple compensating control signal was 5.895 V. The curves are averages of 4000 pulses.

output voltage is actually amplified (red) and the combined ripple and droop is considerably larger than for the measurements with the original phasing of the ripple compensation waveform. The curves in Fig. 5.30 are averages of 200 measured pulses. The flat-top stability for the waveform with active ripple compensated, shown in green colour in Fig. 5.30, was 2.52 V for 160 ns duration and 3.6 V for 210 ns duration. When the phase of the ripple component was shifted by 180 degrees, shown in red colour in Fig. 5.30, the flat-top stability of the pulse waveform was 3.60 V for 160 ns pulse flat-top duration and 7.26 V for 210 ns duration. Without active ripple compensation, the corresponding values for the flat-top stability were 3.8 V and 4.5 V, as can be seen in the blue curve in Fig. 5.30.

From the results shown above, the following points were noted. Because

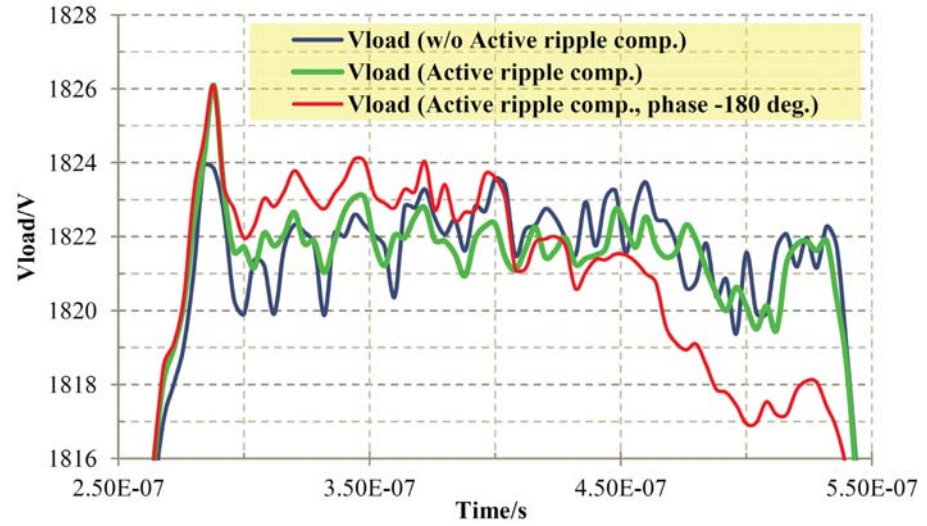


Figure 5.30. Measured V_{load} with four constant voltage layers with $V_{ci} = 553$ V and with an active analogue modulation layer ($R_a = 7.96 \Omega$). $V_{Bias} = 6.0$ V, the compensation signal consisted of a ramp and a 3.906 MHz ripple component with correct phase (green) and 180 degrees shifted (red) phase. The blue curve is the output waveform without ripple compensation applied.

the green curve in Fig. 5.30, in which case the active filtering of a ripple component is applied, has better flat-top stability than the blue curve, which was generated using only the ramp compensation, the flat-top stability of the output pulse was improved by applying the active ripple compensation. Therefore, a ripple component of the output waveform was successfully attenuated actively and the result is visible in the time domain signals shown in Fig. 5.30. Furthermore, the red curve in Fig. 5.30, which is the output waveform modulated by a ripple component with an opposite phase in comparison with the green curve, has worse flat-top stability than the blue curve. This indicates that in the case of the red curve, the ripple of the output waveform was amplified, as was expected.

For comparison, Fig. 5.31 shows the magnitude of FFT for the output waveform in the cases, when the active ripple compensation was not applied (blue) and when it was applied successfully to reduce the ripple (green), and when it was amplifying the ripple (red). The frequency resolution of the FFT in Fig. 5.31 is 0.977 MHz. The measured waveform in the case when the active modulation was applied successfully was the same as is shown in Fig. 5.28. The modulating control signal included a 3.906 MHz frequency component to compensate this frequency component of ripple. In Fig. 5.31, the magnitude of 3.906 MHz frequency component was reduced from 0.26 V (blue) to 0.13 V (green). When the phase of the 3.906 MHz component of the compensation waveform was shifted by 180

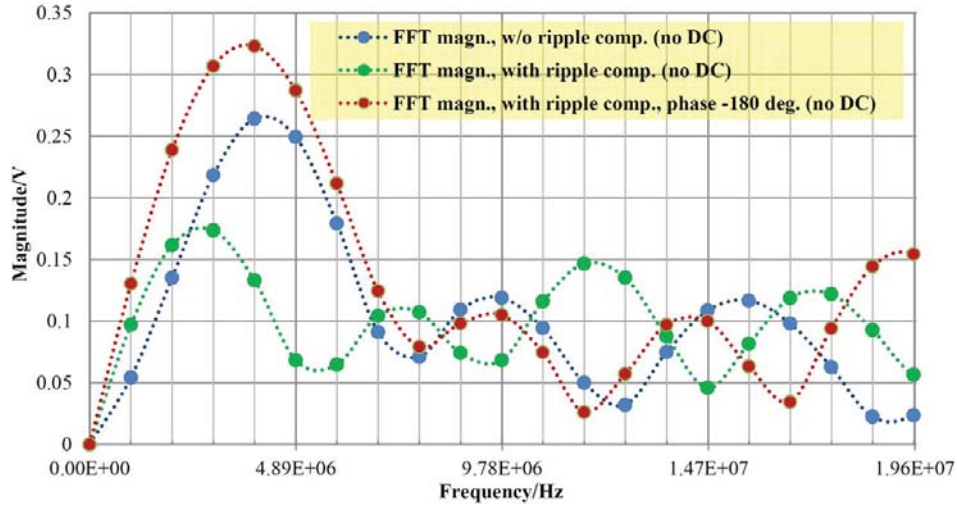


Figure 5.31. Magnitude of the fast Fourier transform for the flat-top of the output waveform of the prototype inductive adder, in the cases when the active ripple compensation is applied with compensating phase (green), with 180 degrees shifted (red) and when it is not applied (blue).

degrees, the magnitude of this component in the output waveform was increased from 0.13 V (green) to 0.32 V (red). This indicates that the amplitude of this frequency component was clearly attenuated or amplified by the active modulation layer and that the amplitude of this frequency component of the ripple was reduced approximately to a half by applying the active ripple compensation. The peak amplitude of the ripple of the green curve in Fig. 5.30 is at 2.9 MHz. The magnitude of this frequency component, 0.17 V, is attenuated in comparison with the magnitude of this frequency component of the blue curve, 0.22 V. On the other hand, the third highest magnitude of ripple of the green curve, 0.15 V, is at 11.7 MHz and this is larger than the magnitude of this frequency component of the blue curve, 0.05 V. This means that the magnitude of the 11.7 MHz ripple component was actually amplified by the active ripple compensation. The effect of active ripple compensation is clearly visible in the output waveforms in the frequency domain, as shown in Fig. 5.31, as well as in the time domain, shown in Fig. 5.30. The conclusion is drawn that a frequency component of the ripple of the output waveform of the inductive adder, shown in Fig. 5.28, was successfully compensated by applying the active analogue modulation.

Demonstration of active ripple compensation for a fast, high-voltage pulse is one of the most significant results of this dissertation. The best flat-top stability presented in this section, $\pm 0.05\%$ for a 1.823 kV pulse for 160 ns flat-top duration, was obtained by applying active compensa-

tion of the droop and the ripple for the output waveform. According to the literature survey presented in Chapter 2, the best measured flat-top stability was reported for a series switch topology feeding ± 12.5 kV pulses to a 108 pF capacitive load with flat-top stability of 0.001 % for 22 μ s [55]. However, the settling time of the pulse was not reported and the load was capacitive, hence there was no current flow during the flat-top. The second best flat-top stability was reported for a modulator based on a matrix transformer, which fed a non-linear klystron load. For this modulator, the flat-top stability was ± 0.05 % for a 200 kV pulse during 3 μ s of a 4.5 μ s pulse flat-top and the total duration of the pulse was approximately 10 μ s [89]. In this case, the pulse amplitude was more than 100 times larger and the pulse flat-top duration was approximately 19 times longer than what was measured for the inductive adder in this dissertation. However, according to the literature review, the flat-top stability reported in this dissertation is better than reported for any pulse power modulator feeding short, less than 1 μ s, long pulses to a resistive load with a comparable high voltage. The measured flat-top stability is also better than reported for any inductive adder or any Marx modulator in the literature.

5.5.5 Measurements on the Two Inductive Adders with Opposite Polarities with a Single Current Transformer

This section presents the measurements on the output waveforms of two prototype inductive adders with a single current transformer. This measurement technique was applied to demonstrate the accuracy of the analogue modulation method in manipulating the output waveform. The output currents, of opposite polarities, from two inductive adders were fed through a single current transformer to two separate loads. The inductive adders were assembled from components which had the same nominal parameters. The dimensions of the adder stacks were also the same except for the diameters of the secondary stalks which were 45 mm and 43 mm, as mentioned in Section 5.1.3. Fig. 5.32 shows the current transformer with two loads and two high-voltage, HTC-50-7-2, coaxial cables. As mentioned in Section 5.2, the outer conductor of the coaxial cables were stripped for a short distance, where the coaxial cable passed through the current transformer. The outer conductor of each coaxial cable was replaced with a 10 mm wide and 1 mm thick piece of copper sheet for a length of approximately 20 mm. The copper sheet was bent tightly on the current transformer to minimise the area between the inner and outer

conductors and thus to minimise the impedance mismatch which was introduced by removing the outer conductors of the cables. Fig. 5.33 shows the complete measurement set-up with two inductive adders.

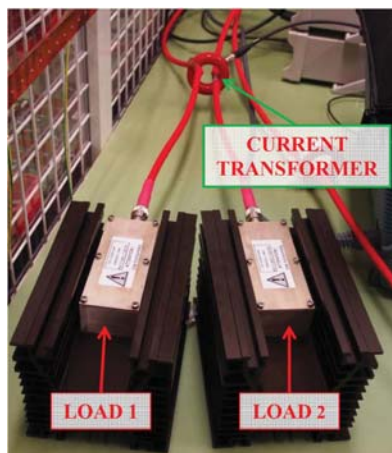


Figure 5.32. Two loads with the cables connected through a single current transformer.

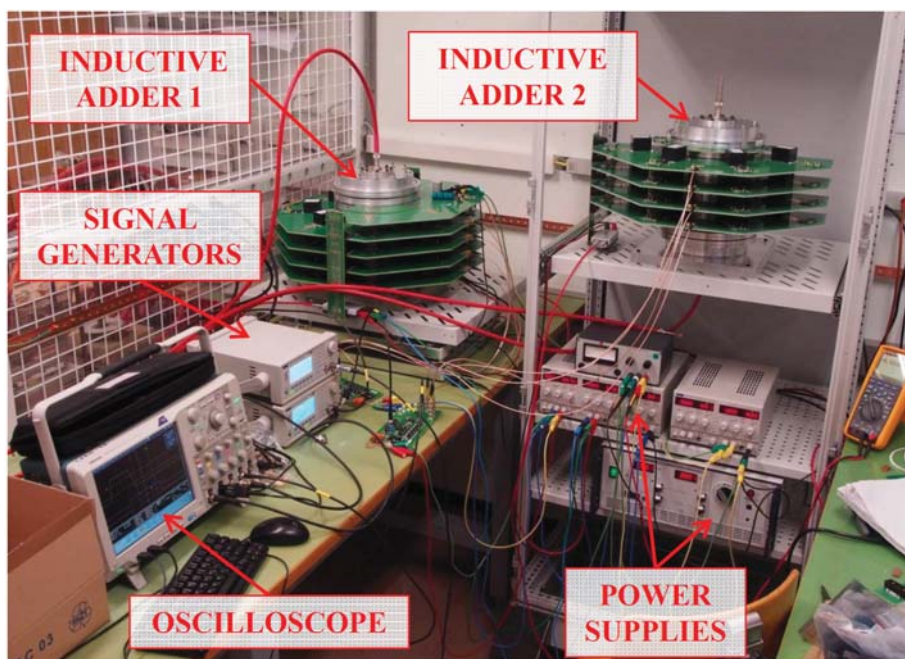


Figure 5.33. Two prototype inductive adders in the measurement set-up.

The purpose of measuring the two pulses with a single current transformer was to improve the relative resolution of the measurements, by decreasing the total dynamic range of the measured current. Ideally, if the pulses are of opposite polarity but otherwise identical, they would cancel each other, therefore summing to a zero net current in the current transformer. Analogue modulation methods, both passive and active, were applied to the output waveform of one inductive adder. In the ideal

case, the measured net current in the current transformer is small in comparison with the full load current and is only due to the modulation. Therefore, the maximum value and the range of the amplitude of the measured signal from the current transformer would be much smaller than in the measurements of the high-current pulse shown in the previous sections. The summed measurement was carried out using a higher sensitivity for an oscilloscope than for individual pulse measurements shown in this dissertation, because the dynamic range of the measured waveform was reduced by a factor of 3, as is shown below.

Figure 5.34 shows the output pulses of both inductive adders. Inductive adder 1 was equipped with an analogue modulation layer, in which the resistor R_a was 7.96Ω . The pulse capacitors of the four constant voltage layers were initially charged to 326 V. In inductive adder 2 the pulse capacitors of the four constant voltage layers were initially charged to 300 V and it was not equipped with an analogue modulation layer. The primary of the fifth cell of inductive adder 2 was short-circuited. The red curve in Fig. 5.34 is the output waveform of inductive adder 1 and it is a single measured waveform. The maximum output voltage of inductive adder 1 is 1095 V and the flat-top stability for the 210 ns pulse flat-top duration is 12 V, which consists mainly of ripple. The blue curve in Fig. 5.34 is the output waveform of inductive adder 2 and it is an average of 10 measured pulses. For inductive adder 2, the maximum output voltage is 1120 V and the flat-top stability is 15.0 V for 210 ns duration and this consists mainly of the droop.

Figure 5.35 shows the net waveform $V_{\text{load1+load2}}$ of the output pulses of two prototype inductive adders with opposite polarities. The output waveforms were measured with a single current transformer. The pulse capacitors of inductive adder 1 were initially charged to 313 V and the analogue modulation layer was operating in passive mode with resistance R_a of 7.96Ω . The pulse capacitors of the four constant voltage layers of inductive adder 2 were initially charged to 290 V and the primary of the fifth layer was short-circuited. The analogue modulation layer of inductive adder 1 was operating in passive mode and resistance R_a was 7.96Ω . The combined droop and ripple of the net waveform was 13.7 V ($\pm 1.25 \%$) for 210 ns duration. Any ripple or droop, which is not present in both output waveforms, increases the net current through the current transformer.

Fig. 5.36 shows the net waveform $V_{\text{load1+load2}}$ of the output pulses of two prototype inductive adders with opposite polarities in the case when the

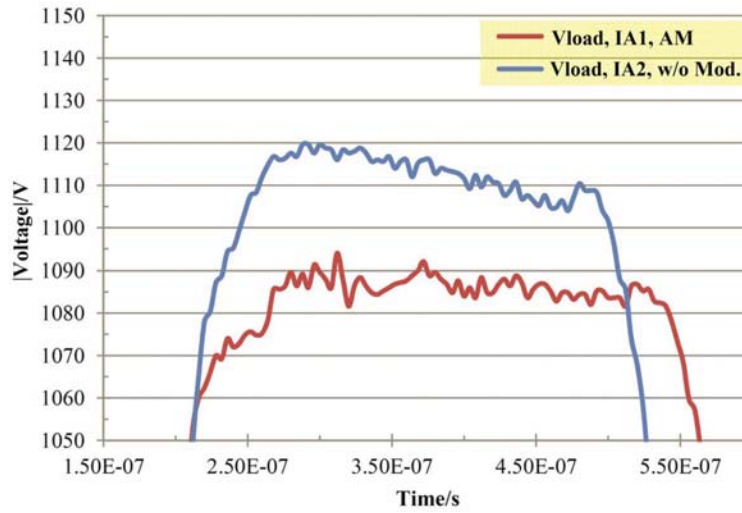


Figure 5.34. The output waveforms of two prototype inductive adders. In inductive adder 1, $V_{ci} = 326$ V and it was equipped with a passive analogue modulation layer ($R_a = 7.96 \Omega$) (red). In inductive adder 2, $V_{ci} = 300$ V and the primary of the fifth layer was in short-circuit (blue).

active analogue modulation method was applied to the output waveform of inductive adder 1 to compensate the droop of the sum waveform. The pulse capacitors of inductive adder 1 were initially charged to 313 V and the analogue modulation layer was operating in active mode. The pulse capacitors of the four constant voltage layers of inductive adder 2 were initially charged to 290 V and the primary of the fifth layer was short-circuited. The flat-top stability of the sum waveform $V_{load1+load2}$ shown in Fig. 5.36 is ± 1.16 V (± 0.1 %) for 210 ns duration for individual amplitudes of approximately 1100 V. The droop of the sum waveform is practically zero, which means that the droop of the summed waveform is completely compensated by the active analogue modulation. The flat-top stability of the summed waveform was reduced from 13.7 V to ± 1.16 V with the active droop compensation. The sum waveform $V_{load1+load2}$ shown in Fig. 5.36 is an average of 50 measured pulses.

In Fig. 5.36, the total dynamic range of the measured net sum of the two pulses is 370 V and the peak values of the sum waveform occurred during the rise and fall times of the pulses. The pulse shapes of the two inductive adders are slightly different, because inductive adder 1 includes the analogue modulation layer, which affects also the pulse rise and fall times. Also, the secondary stalks of the inductive adders had slightly different diameters which increased the output impedance from 64.6Ω for inductive adder 1 to 68.8Ω for inductive adder 2, as explained in Section 5.1.3 of this chapter. However, the dynamic range of the output waveform

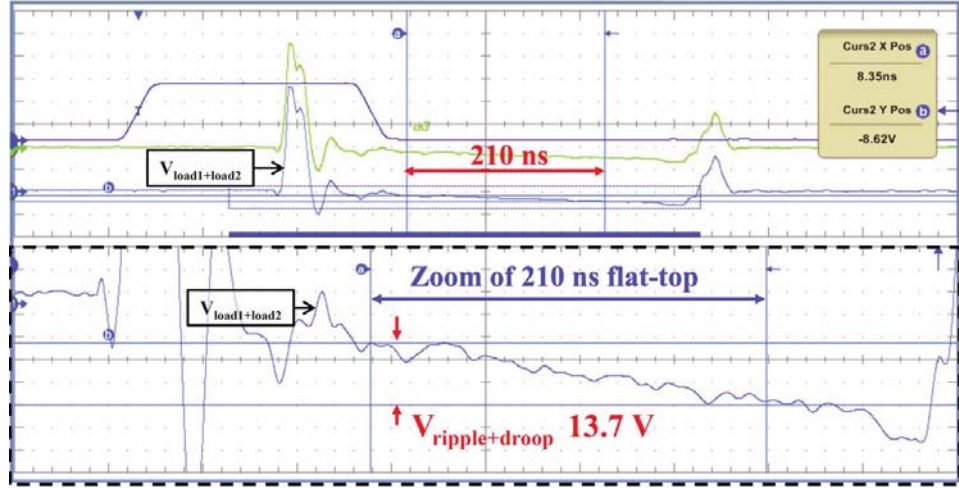


Figure 5.35. Measured net waveform $V_{load1+load2}$ of the output pulses with opposite polarities, generated by two prototype inductive adders. In inductive adder 1, $V_{ci} = 313$ V and it was equipped with a passive analogue modulation layer ($R_a = 7.96 \Omega$). In inductive adder 2, $V_{ci} = 290$ V and the primary of the fifth layer was short-circuited.

was significantly smaller than in the measurements of a single pulse, where the dynamic range of the output waveform was 1.1 kV. The very low droop of the measured sum waveform $V_{load1+load2}$ verifies that compensation of the droop, applied by the analogue modulation layer, is very effective. This result is in agreement with previous measurements shown for a single pulse in previous sections of this chapter. In the output waveform shown in Fig. 5.20 the droop is completely compensated and the compensation of the droop was repeatable with a smaller dynamic range of the oscilloscope signal, as is shown in Fig. 5.36. This measurement also demonstrates that in the kicker system with two modulators and a stripline kicker, with appropriate measurements and feedback, the active analogue modulation should be able to compensate the small variations or non-linearities introduced by the terminating resistors and cables.

5.6 Evaluation of the Resolution of the Measurements

The stability of the measured pulses, shown in the preceding sections, in many cases exceeds the specified basic accuracy of the measurement equipment. The ripple of the output waveform of an inductive adder consists of synchronous and asynchronous ripple. The frequency components of the synchronous ripple remain in the same phase in comparison with the pulse in the measurements of consecutive pulses. This means that

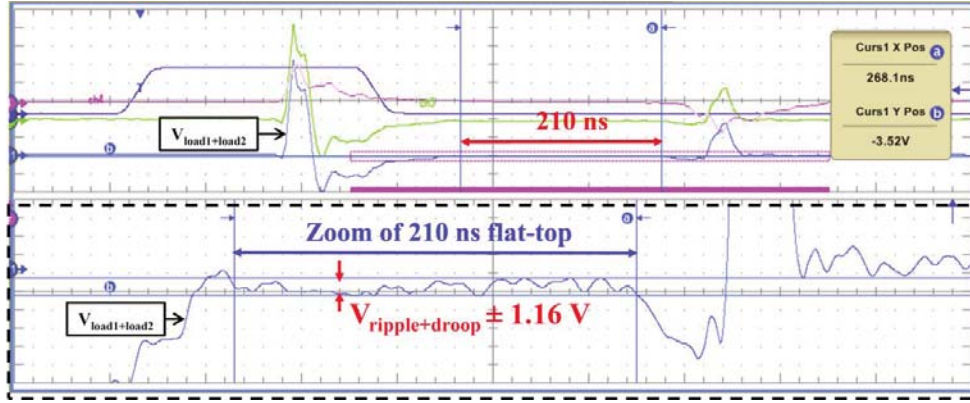


Figure 5.36. Measured net waveform $V_{\text{load1}+\text{load2}}$ of the output pulses with opposite polarities, generated by two prototype inductive adders. In inductive adder 1, $V_{\text{ci}} = 313 \text{ V}$, $R_a = 7.96 \Omega$ and the droop of the summed waveform was compensated by applying active analogue modulation. In inductive adder 2, $V_{\text{ci}} = 290 \text{ V}$ and the primary of the fifth layer was short-circuited.

when an average of several measured pulses is computed, these frequency components are not cancelled but they are visible in the computed average waveform. These ripple components are also expected to be repeated with similar amplitudes in every output pulse. The main source for the synchronous ripple components is the impedance mismatch in the inductive adder itself and the impedance mismatch between the inductive adder, the high-voltage coaxial cable and the load. For example, a small piece of outer conductor of the coaxial cable between the inductive adder and the load was replaced by a copper sheet for mounting a current transformer, as is shown in Section 5.2. However, care was taken to minimise the length and the corresponding delay of the mismatch.

On the contrary, asynchronous ripple consists of arbitrary frequency components, the phases of which are not dependent on the output pulse. The amplitude of asynchronous frequency components can also vary in the measurements of consecutive pulses. It is expected that the asynchronous ripple is coupled or conducted to the measurement system from outside of the inductive adder. The asynchronous ripple may also be caused by coupling from an external source to the current transformer, the oscilloscope or any electrical device in the set-up. The measurements for this dissertation were completed in a high-voltage test cage at CERN. The test cage was electrically not a Faraday cage and therefore the asynchronous ripple could have been coupled to the measurement set-up from outside.

The measurements shown in this chapter were done with a Tektronix DPO 5034 Oscilloscope, which has an 8-bit ADC [90]. The effective number of bits (ENOB) of this ADC is 6-7 bits, as mentioned in Section 2.4.

However, in most of the measurements presented in this dissertation, and in all measurements of applying active analogue modulation, over-sampling by a factor of four was applied, which gives one additional bit for the ADC of the oscilloscope. The sampling rate of the oscilloscope was set to 1 GS/s and each data point was an average of four samples, which gives 250 MHz effective sampling rate. Therefore, the effective bit length of the ADC was expected to be at least 7 bits. According to Eq. (2.7), the -3 dB bandwidth of the measurement system was 110 MHz, which is well above the maximum frequency of interest. The 3 dB cut-off frequency of the Bergoz CT-E0.1-B current transformer which was used in the measurements is 50 MHz [92].

The ensemble averaging method, discussed in Section 2.4, was also applied in the measurements shown in this dissertation. The ensemble averaging filters the asynchronous noise of the output voltage and hence improves the resolution of the measurement of the output waveform. According to Eq. (2.10), the vertical resolution of the ADC is improved as follows:

$$Res_{\text{Enh,ea}} = 0.5 \times \log_2 n \quad (5.2)$$

In this equation, n is the number of measurements to average and $Res_{\text{Enh,ea}}$ is the enhanced resolution of the ADC. As explained in Section 2.4, this averaging method would also ideally reduce the uncorrelated measurement noise by the square root of the number of the measurements which are averaged.

Figure 5.37 shows zooms of flat-top of the measured output waveforms for the inductive adder with active droop compensation. In these measurements, the pulse capacitors were initially charged to 551 V. Ensemble averaging of 10, 50, 200 and 1000 pulses were applied for the measured pulses. The repetition rate of the pulses was 1 Hz and the test was carried out for an inductive adder which had been running for more than half an hour to reach thermal equilibrium. The peak-to-peak ripple for the 160 ns flat-top duration from 350 ns to 510 ns is ± 4.06 V (± 0.22 %) for 10 pulses, ± 2.65 V (± 0.15 %) for 50 pulses, ± 2.32 V (± 0.13 %) for 200 pulses and ± 1.67 V (± 0.09 %) for 1000 pulses. According to Eq. (2.9), the amplitude of the asynchronous ripple would reduce ideally by factors of 2.24, 2 and 2.24, when the number of averaged pulses was increased from 10 to 50, from 50 to 200 and from 200 to 1000. For the measured waveforms

in Fig. 5.37 the reduction in the amplitude of the ripple was by factors 1.53, 1.14 and 1.39, respectively. This means that, effectively, a proportion of the ripple of the output waveforms shown in Fig. 5.37 was actually not asynchronous arbitrary background noise but the ripple was synchronised with the output pulse. On the other hand, if the synchronous ripple can be accurately measured, it also means that a significant portion of it could be potentially filtered with the active ripple compensation.

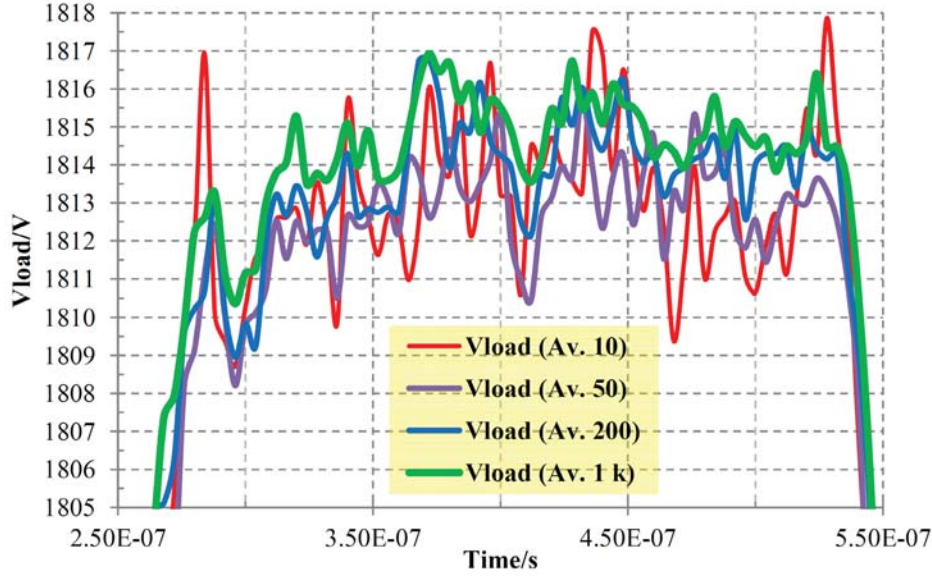


Figure 5.37. Measured V_{load} of the first prototype inductive adder, with four constant voltage layers, with $V_{ci} = 551$ V, and with an active droop compensation applied. Ensemble averaging of 10 (red), 50 (purple), 200 (blue) and 1000 (green) pulses.

In order to evaluate the measurements which are presented in Chapter 5, Table 5.4 summarises the measurements presented together with the oversampling and the averaging used and the expected enhancement to the vertical resolution, computed according to Eq. (2.5) and (5.2). The first row in the table shows the applied modulation method, PM corresponding to passive analogue modulation and AM active analogue modulation. The letters d and r correspond to droop and ripple compensation, respectively. Notation 2 IAs in the heading of the last column refers to measurements of the output pulses of two inductive adders with a single current transformer. The second row shows the references to the figure of each measurement in this dissertation. ΔV_{d+r} is the combined droop and ripple of the output voltage. The fifth row shows the enhancement of the vertical resolution of the ADC by applying oversampling, $Res_{Enh,os}$ according to Eq. (2.5). Oversampling by factor of four was applied for

the measurements of active droop and ripple compensation, which gives $Res_{Enh,os}$ of 1 bit. n is the number of averages for computing the enhancement of the vertical resolution of the ADC by applying ensemble averaging, according to Eq. (5.2). $N_{ADC,Eff}$ is the effective bit length of the ADC of the oscilloscope and it is calculated as the sum of the worst case estimate for the ENOB, 6 bits, and $Res_{Enh,os}$ and $Res_{Enh,ea}$. The third last row $V_{r,ADC}$ gives the total voltage range of the input channel of the oscilloscope. As mentioned in Section 5.2, the output pulses of the inductive adders were measured with a current transformer and the output signal of the current transformer was converted to the pulse voltage. In each measurement, the maximum applicable sensitivity of the oscilloscope was used by setting $V_{r,ADC}$ as low as possible but still keeping the full pulse displayed to avoid saturation of the channel. The last two rows are the relative resolution of the ADC, Res_{Rel} , and the absolute resolution of the ADC, Res_{Abs} , which are computed according to Eq. (2.4).

Table 5.4. Summary of measurements presented in Chapter 5.

Mod. method	w/o mod.	PM (d)	AM (d)	AM (d)	AM (d&r)	AM (d&r)	AM (d) 2 IAs
Fig.	5.14	5.17	5.20	5.21	5.28	5.29	5.36
ΔV_{d+r} (%)	1.5	± 0.16	± 0.07	± 0.06	± 0.05	± 0.06	± 0.1
ΔV_{d+r} (V)	21.2	± 1.9	± 1.23	± 1.17	± 0.96	± 1.02	± 1.15
$Res_{Enh,os}$ (bits)	0	0	1	1	1	1	1
n	1	100	1000	4000	1000	4000	50
$Res_{Enh,ea}$ (bits)	0	3.3	5.0	6.0	5.0	6.0	2.8
$N_{ADC,Eff}$ (bits)	6.0	9.3	12.0	13.0	12.0	13.0	9.8
$V_{r,ADC}$ (V)	2000	2000	3000	3000	3000	3000	500
Res_{Rel} (%)	1.6	0.16	0.024	0.012	0.024	0.012	0.11
Res_{Abs} (V)	32	3.2	0.73	0.37	0.73	0.37	0.55

According to Table 5.4, the absolute resolution Res_{Abs} of each measurement is smaller than the range of the combined droop and ripple of the output voltage ΔV_{d+r} , except in the first column in which ensemble averaging has not been applied. An approximate estimate for the confidence level of the measurements presented in Table 5.4 could be $\pm Res_{Abs}$ for each measurement. A point to note is that in computing the values of $N_{ADC, Eff}$, Res_{Rel} and Res_{Abs} in Table 5.4, the ENOB of the ADC of the oscilloscope was estimated to be 6. If the ENOB is 7 bits, then the relative resolution Res_{Rel} and the absolute resolution Res_{Abs} would be further improved by a factor of 2.

The difference of the measured flat-top stability between the best measured output pulses, in the case in which the active droop compensation was applied, Fig. 5.20, and in the case in which the active droop and ripple compensation was applied, Fig. 5.28, is relatively small. The flat-top stability of the output pulse which was modulated with the active droop compensation was ± 1.23 V (± 0.07 %) for an average of 1000 pulses and with the active droop and ripple compensation it was ± 0.96 V (± 0.05 %). For ensemble averages of 4000 pulses, Fig. 5.21 and Fig. 5.29, the flat-top stability for the output pulse which was modulated with the active droop compensation is ± 1.17 V (± 0.06 %) and with the active droop and ripple compensation it was ± 1.02 (± 0.06 %). The absolute resolutions Res_{Abs} of the measurements of 1000 and 4000 averages were 0.73 V and 0.37 V respectively, as is shown in Table 5.4. Therefore, the improvement of the flat-top stability of the output pulse by applying the active ripple compensation instead of active droop compensation could not be proved by only comparing the values of ΔV_{d+r} of these measurements. However, the effect of the active ripple compensation was verified in the measurement, in which the output voltage was modulated by a ripple cancelling control signal, and then applying the modulating signal with the same frequency component but with an opposite phase, as was shown in Section 5.5.4.

Because of the relatively high ripple of the measurements of a single pulse, the actual flat-top stability for a single pulse cannot be defined exactly from the electrical measurements. However, it might be possible to measure later at an accelerator facility with a stripline kicker and the beam, as discussed in Chapter 2. Also, the measurement resolution was adequate to experimentally verify in the laboratory that the presented modulation methods work and they can be applied to modulate the output waveform of the inductive adder with adequate stability. The mea-

surement results of this dissertation also showed that the active analogue modulation can be applied to compensate the droop of the output waveform practically down to zero. The active compensation of ripple was successfully demonstrated by carrying out a Fourier analysis for the output voltage and then applying an appropriate compensation signal in the frequency domain to filter the defined ripple component. The ripple of the output voltage was successfully suppressed to ± 1 V level for a 1.8 kV pulse for 160 ns flat-top duration.

5.6.1 Verifications of the Simulation Models for the CLIC DR Extraction Kicker Inductive Adder

The PSpice simulation models for the inductive adder, presented in Chapter 4, were evaluated by comparing the measured output waveforms with the simulated waveforms. It was found that by modifying two model parameters, namely magnetising inductance L_m and the on-state resistance of the semiconductor switches, R_{sw} , the measured waveforms could be reproduced with the simulation model with a reasonable accuracy. These parameters were assumed to have the largest discrepancy, because the effective magnetising inductance of a magnetic core at a certain time point depends on the applied voltage and the pulse duration until that point, as well as the pulse history of the magnetic core. Also, the parameter R_{sw} was given in the data sheet of the manufacturer as a typical value, without estimated discrepancy, and it was seen in the measurements of the magnetising current that with high current values, e.g. more than half of the data sheet rating for pulse current of the switch, the on-state resistance was not constant during the pulse but it was dependent on the current flow through the switch. Also in this comparison of the measured and simulated waveforms, the main goal was to repeat the pulse flat-top and not the rise and fall times, which were not the main interest of this dissertation. The rise time can be reduced by increasing the gate-source voltage of the MOSFETs, as shown in Section 5.3.1.

The measured waveforms were compared with simulated waveforms and parametric simulations were carried out, in which the values of L_m and R_{sw} were modified in order to reach a good match between the measured and simulated waveforms. The starting point values for all parameters for the simulation models were the same as given in Table 4.1 in Chapter 4. However, in all cases of the simulations shown in this section, two branches of the inductive adder were powered. Therefore, the simu-

lation parameters were computed to correspond to two parallel branches. Also, the measured value for the primary loop inductance, given in Section 4.4.2, was included into the simulation model and the measured value for the core loss resistance R_c was applied. A reasonable range for the effective magnetising inductance L_m was estimated to be 2.5-10.0 μH for the Vacuumschmelze W567 cores used for all these measurements. The same inductance value was applied for L_m and L_{ma} . The range for the on-state resistance of the semiconductor switches, R_{sw} , was estimated to be 0.66-1.0 Ω for a single switch, which for a parallel connection of two branches effectively corresponds to 0.33-0.50 Ω , as given in Table 5.5.

Table 5.5. Parameters for a single layer of inductive adder 1 based on the modelling studies of the 5-layer prototype inductive adders.

Parameters for the secondary and for the magnetic core	Value
C_c (pF)	6.5
L_m, L_{ma} (μH)	2.5-10.0
L_{ss} (nH)	3.4
N_{layers}	5
R_a (Ω)	4.4 7.96
R_c (Ω)	25.3
R_s (m Ω)	0.1
R_{load} (Ω)	50.0
Parameters for a single layer with two branches powered	
$C_{s,2br}$ (μF)	24
$L_{pl,2br}$ (nH)	23.8
$R_{p,2br}$ (m Ω)	25
$R_{sw,2br}$ (Ω)	0.33-0.50

Measured and Simulated Output Waveform without Analogue Modulation

Figure 5.38 shows simulated waveforms for a 5-layer inductive adder which consists of five constant voltage layers. The measured waveform, shown in Fig. 5.38, is the same which is shown in Fig. 5.13. The prototype inductive adder was equipped with five layers, in each of which two primary current branches were powered. The pulse capacitors were initially charged to 302 V. In the same figure, there are six simulated output waveforms with different parameters. The first three curves from the bottom

show the effect of the magnetising inductance upon the output waveform. The actual magnetising inductance depends on the linearity of the B-H curve of the magnetic cores and on the voltage-time product of the pulse, and therefore the duration of the pulse. In simulated waveforms shown in Fig 5.38, $7.5 \mu\text{H}$ of magnetising inductance gives the gradient for the droop, which is the most similar in comparison with the measured waveform. The magnetising inductance is the main contributor to the droop of the pulse flat-top in the prototype inductive adder during the normal operation. Therefore, the value of the magnetising inductance was changed in order to find the value, which gives the same gradient as what the measured output waveform has.

The second, third and fourth curves from the top in Fig. 5.38 show the simulated output waveforms of the inductive adder with three different values of the on-state resistance of the semiconductor switches. In this case, when $R_{\text{sw},2\text{br}}$ equals to 0.42Ω , the simulated waveform has the same amplitude as the measured waveform. The on-state resistance presents the second most important contributor to the losses in the inductive adder, after the core losses. Therefore, the value of the on-state resistance was changed in order to get the amplitude, which corresponds to the measured output waveform. The best simulated waveform, which was achieved with values $R_{\text{sw},2\text{br}}$ equals to 0.42Ω and L_m equals to $7.5 \mu\text{H}$, differs from the measured output waveform by approximately $\pm 7 \text{ V}$ in the flat-top duration of the pulse from 275 ns to 580 ns. This corresponds to an error of $\pm 0.49 \%$ of the pulse amplitude and in Fig. 5.38, it is clearly visible that this is mainly due to ripple, which is not present in the simulated waveforms. The assumed magnetising inductance, $7.5 \mu\text{H}$ is greater than shown for W567 core in Table 5.2 without biasing, however the measurements on magnetising inductance were carried out with higher voltage than the measurements and simulations shown in Fig. 5.38. Also, the non-linear on-state resistance of switches has not been taken account in the simulations.

Figure 5.39 shows the measured waveform with nominal 3.5 kV output voltage of the prototype inductive adders. The same measured output voltage is shown in Fig. 5.15 and, for this measurement, the pulse capacitors were initially charged to 762 V. In Fig. 5.39, there are two simulated output waveforms with different parameters. In the first simulated output waveform, shown as red dashed curve, the magnetising inductance was assumed to be $4.8 \mu\text{H}$ and the effective on-state resistance

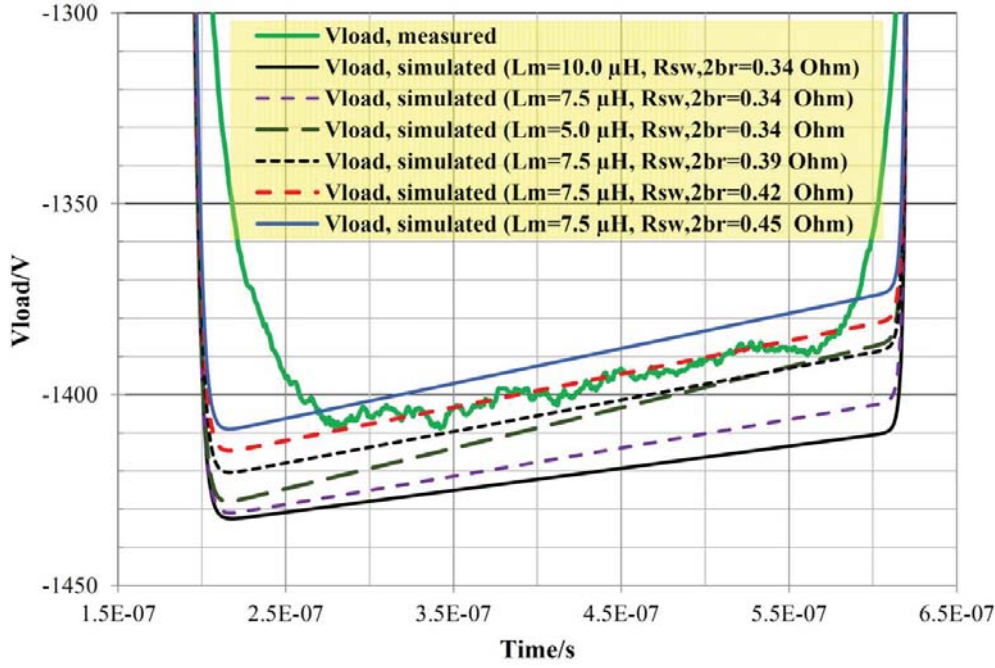


Figure 5.38. Measured and simulated output waveforms of the 5-layer inductive adder without analogue modulation. $V_{ci} = 302$ V.

of the switches in two powered branches 0.47Ω . The second simulated output waveform, shown as solid blue curve, the magnetising inductance was $2.5 \mu\text{H}$ and the effective on-state resistance 0.37Ω . For comparison, the measured magnetising inductance for W567 cores in Table 5.2 is from $4.9 \mu\text{H}$ to $0.8 \mu\text{H}$ without biasing. In Fig. 5.39, the first simulated waveform (red, dashed) fits reasonably well to the measured pulse waveform from 180 to 280 ns, during which the difference of the simulated and measured waveform is approximately ± 20 V ($\pm 0.57\%$) and explained mainly by noise and ripple, which does not exist in the simulated waveforms. In Fig. 5.39, the second simulated waveform (blue) fits better to the measured waveform from 230 ns to 320 ns and the error is also approximately ± 20 V ($\pm 0.57\%$). The decrease of the magnetising inductance during the pulse corresponds to the decrease of the permeability of the core, and therefore decrease of the incremental gradient of the B-H curve when magnetic field H increases. However, if the temperature of the MOSFET switch increases, the on-state resistance tends to increase, because it has a positive temperature coefficient [169]. In Fig. 5.39, setting the on-state resistance lower in the second simulation was necessary to adjust the amplitude of the simulated waveform to the measured waveform between 230 ns and 320 ns.

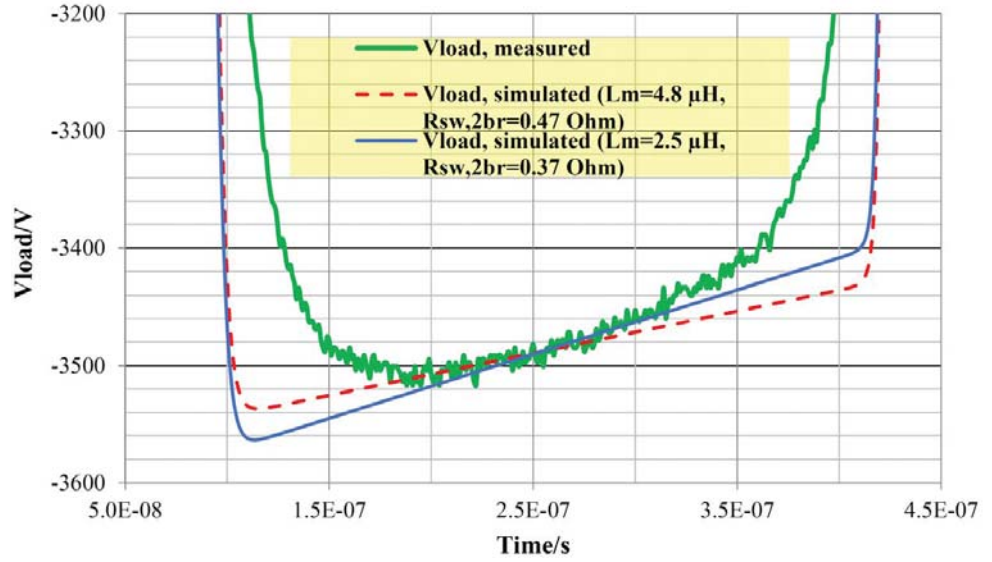


Figure 5.39. Measured and simulated output waveforms of the 5-layer inductive adder without analogue modulation, $V_{ci} = 762$ V.

Measured and Simulated Output Waveform with Passive Analogue Modulation

The same approach as presented in the previous section, for the simulations of the output waveforms without modulation, has been applied in this section to the cases in which the output of an inductive adder is modulated with passive analogue modulation. For a reference, Fig. 5.40 shows the measured output waveform of the prototype inductive adder for the case in which there are four constant voltage layers operating normally and the primary of one layer is in the short-circuit. The measured load voltage, shown as a green curve in Fig. 5.40, is also shown in Fig. 5.16. The parameters for the simulation model were the same as shown in Table 5.5, except that the primary of one layer of the model was short-circuited. In these operating conditions, the on-state resistance of 0.36Ω and the magnetising inductance of $10 \mu\text{H}$ gave the best match between the simulated and measured waveform. The error is approximately ± 8 V, $\pm 0.78 \%$ for the flat-top duration from 260 ns to 580 ns and also in this case, the difference is mainly caused by the noise and ripple of the measured output waveform.

In Fig. 5.41, the measured output waveform is shown for the case in which there have been four constant voltage layers and one analogue modulation layer operating in the passive mode. The capacitors of the constant voltage layers were initially charged to 285 V and the resistance R_a was 4.4Ω . The measured load voltage, shown as a green curve in

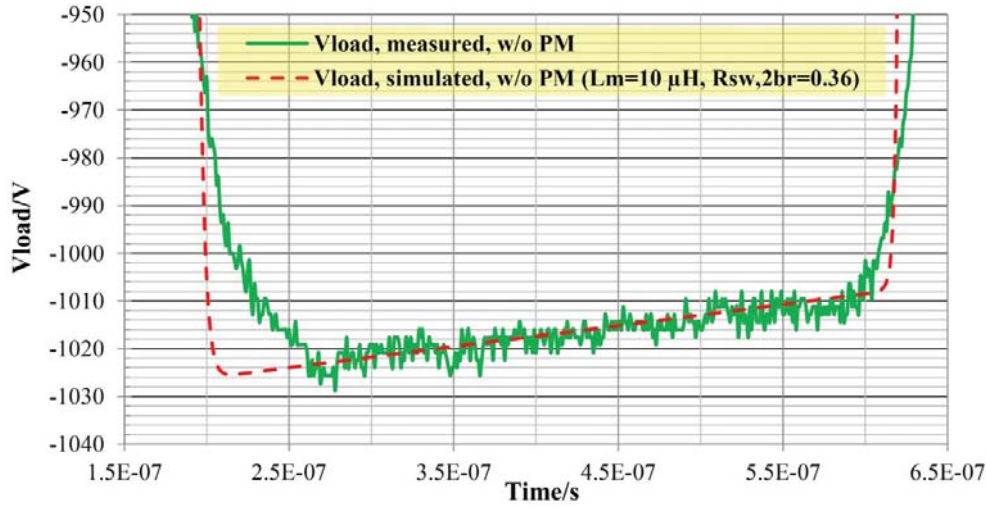


Figure 5.40. Measured and simulated output waveforms of the 5-layer inductive adder, with $V_{ci} = 270$ V, and without analogue modulation for the case in which the primary of one layer is short-circuited.

Fig. 5.41, is also shown in Fig. 5.16. In these operating conditions, the on-state resistance of 0.45Ω and the magnetising inductance of $10 \mu\text{H}$ gave the best match between the simulated and measured waveform for the flat-top duration from 250 ns to 590 ns. The error is approximately ± 5 V, $\pm 0.5\%$ and also in this case, the difference is mainly caused by the noise and ripple of the measured output waveform.

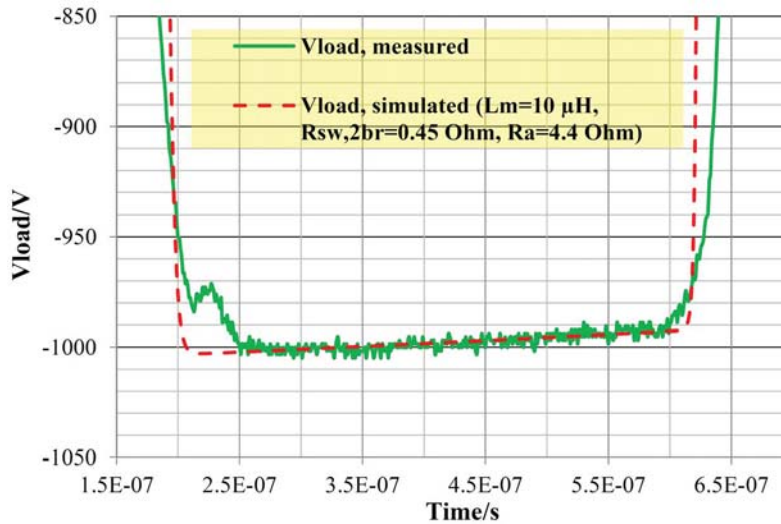


Figure 5.41. Measured and simulated output waveforms of the 5-layer inductive adder with a passive analogue modulation layer ($R_a = 4.4 \Omega$), $V_{ci} = 285$ V.

In Fig. 5.42, the measured output waveform is shown for the case in which the passive analogue modulation was applied. The measured waveform in this figure is the same as shown in Fig. 5.17. The capacitors of the constant voltage layers were initially charged to 350 V and the resistance

R_a was 7.96Ω . In these operating conditions, the on-state resistance of 0.50Ω and the magnetising inductance of $4 \mu\text{H}$ was the combination with which the simulated waveform was very close to the measured waveform, as is shown in Fig. 5.42. The difference of the simulated and measured waveform for the flat-top duration from 320 ns to 820 ns is approximately $\pm 2 \text{ V}$, $\pm 0.2 \%$. Also in this simulation, the difference is mainly caused by the noise and ripple of the measured output waveform. There is practically no ripple in the simulated waveform.

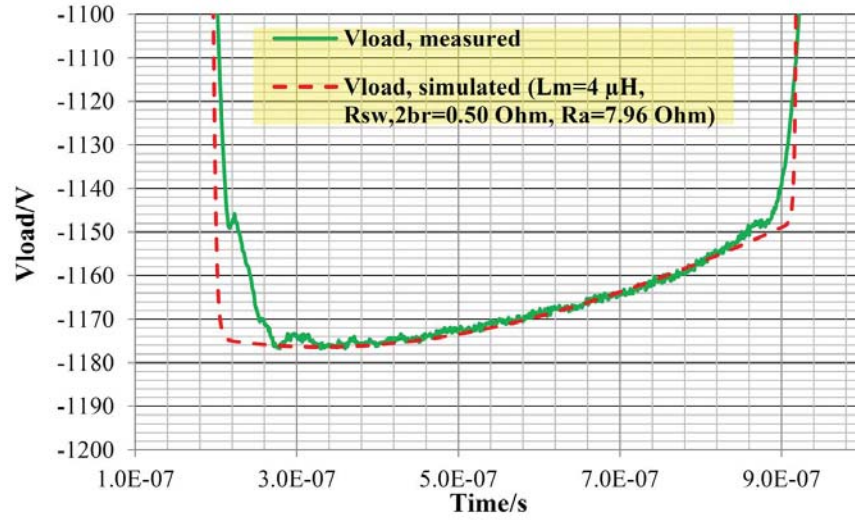


Figure 5.42. Measured and simulated output waveforms of the 5-layer inductive adder, $V_{ci} = 350 \text{ V}$, with a passive analogue modulation layer ($R_a = 7.96 \Omega$).

5.7 Design Proposal for the CLIC DR Extraction Kicker Inductive Adder

In this section, a design proposal is given for the full-power, 12.5 kV, 250 A inductive adder for the CLIC DR extraction kicker system. The design proposal is based on experience with the chosen components for the prototype inductive adder, the analysis of the measurements on the prototype inductive adders and the simulation studies. The design proposal includes the preliminary design dimensions for the geometry of the stack and the main components. Simulated output waveforms, based on the comparisons of the measured and simulated waveforms of the prototype inductive adders, are also given. Finally, a cost estimate is given for the full-power, 20-layer, 12.5 kV prototype inductive adder.

Revised Preliminary Design of the CLIC DR Extraction Kicker Inductive Adder

Table 5.6 shows the revised preliminary design parameters for the CLIC DR kicker inductive adder. The electrical parameters and the geometry of the cell are the same as shown in Table 3.1. However, the measured value of the primary loop inductance of the prototype inductive adder has been used in computing new values for coupling capacitance C_c and secondary stray inductance L_{ss} , and therefore, the stalk diameter has been changed from 18.4 mm to 15.1 mm. Based on the measurements of the magnetic cores, Finemet FT-3L is the most suitable material for the CLIC DR kicker inductive adder. The usable B-H flux swing of this core material is 0.84 T. For 700 V voltage per layer and 1.1 μ s pulse duration, the required effective cross-sectional area for the cores is 9.2 cm², computed according to Eq. (3.33). With a 100 % margin and applying the packing factor of Finemet cores, 68 %, the total cross-sectional area of the cores should be 27.0 cm².

By applying 35 mm for the height and 90 mm for the inside diameter of the core, the outside diameter of the core needs to be at least 244 mm. The estimated magnetising inductance for the core is 135 μ H and the estimated core loss resistance 61.5 Ω . These numbers are based on the measurements of the magnetising cores, shown in Section 5.3.3. The permeability is estimated to be a half of the maximum value shown in Table B2 for Finemet FT-3L core. The core loss resistance has been scaled by assuming the same packing factor but increased number of turns and larger ribbon height, both of which, theoretically, increase the core loss resistance according to Eq. (3.15).

The primary loop inductance L_{pl} will be increased, because the cross-sectional area of the flanges is increased. The dimensions of the primary current loops in the half-layer PCBs are assumed to remain the same, but the total loop from the top flange to the bottom flange is increased. In Section 4.4.2, the total loop inductance was measured to be 47.6 nH and the loop inductance without flanges was 39.3 nH. The loop inductance of the flanges is expected to be the difference of these values, 8.3 nH. The inductance of the current loop along the flanges is estimated to increase from 8.3 nH to 18.6 nH. Therefore, the inductance of a single loop is estimated to be 57.9 nH, instead of the 47.6 nH, which was measured for the prototype inductive adders. The total primary loop inductance of eight parallel current branches is estimated to be 7.2 nH. The output impedance

is matched to $50\ \Omega$ by changing the diameter d of the stalk, which will change the values of the secondary stray inductance L_{ss} and coupling capacitance C_c correspondingly, as is shown in Table 5.6.

Table 5.6. Preliminary design parameters and revised parameters for the CLIC DR extraction kicker inductive adder.

Parameter	Preliminary design	Revised design
insulation material	epoxy	epoxy
V_{out} (kV)	12.5	12.5
Z_{out} (Ω)	50.0	50.0
ϵ_r	4.8	4.8
A_c (cm^2)	10.8	18.3
$A_{c,\text{eff}}$ (cm^2)	7.0	27.0
C_c (pF)	9.4	8.2
l_c (mm)	35	35
l_p (mm)	45	45
d (mm)	18.4	15.1
D_1 (mm)	66	66
D_2 (mm)	90	90
D_3 (mm)	160	244
D_{ins} (mm)	23.8	25.5
E_{max} (kV/mm)	1.06	1.12
L_m (μH)	24.2	135
L_{pl} (nH)	12	7.2
L_{ss} (nH)	11.5	13.3
R_c (Ω)	37.1	61.5
$T_{\text{rd},1w}$ (ns)	0.47	0.41

In addition to the electrical and geometrical parameters, given in Table 5.6, the list of evaluated main components is given in Table 5.7. The table shows the components, which have been found to work well in the prototype inductive adders, and which are therefore recommended to be used in the full-power 12.5 kV prototype inductive adder for the CLIC DR kicker inductive adder.

Table 5.7. Proposed main components for the CLIC DR extraction kicker inductive adder.

Component	Manufacturer	Type	Parameters
Gate driver	IXYS	IXDD614SI [147]	14 A
HV connector	Teledyne Reynolds	167-3517 [150]	20 kV,DC
Modulation resistor (R_a)	HVR	radial [154]	1.2 Ω
MOSFET	Microsemi	APT12067LFLL [101]	1.2 kV, 18 A,DC, 72 A,pulsed
Pulse capacitor	NWL	T00216 [131]	1.0 kV, 12 μ F, 280 A,pulsed
RF power transistor	Microsemi	ARF463AP1G [148]	500 V, 9 A,DC, 100 MHZ
Transformer core	Hitachi-Metals	Finemet FT-3L [160]	n/a

Simulation of the Output Waveform of the CLIC DR Extraction Kicker Inductive Adder

Simulations were carried out with the simulation model consisting of 20-layers, 19 of which were constant voltage layers and one of which was an analogue modulation layer. Table 5.8 shows the parameters for the simulation model for the 20-layer inductive adder for the CLIC DR kicker inductive adder. The parameters are revised from parameters shown in Table 4.1 in Chapter 4, which were based on the preliminary design, and they were updated according to Table 5.6. Eight parallel branches per layer were assumed, following the design of the prototype inductive adders. The simulated waveforms are shown in Fig. 5.43, 5.44 and 5.45.

In Fig. 5.43, the load voltage $V_{\text{load}, w/o PM}$ is shown for the case in which modulation has not been applied. In this simulation, there were 19 operating constant voltage layers in the stack and the pulse capacitors were initially charged to 684 V. The primary side of the analogue modulation layer was short-circuited. The maximum predicted amplitude of the load voltage during the flat-top is approximately 12.537 kV. The droop of the load voltage is 9.0 V (0.072 %) for 160 ns and 53.0 V (0.42 %) for 900 ns. By applying the passive analogue modulation, the specifications

Table 5.8. Parameters for the simulation model of the CLIC DR extraction kicker inductive adder.

Parameters for the secondary and for the magnetic core	Value
C_c (pF)	8.2
L_m (μ H)	135
L_{ss} (nH)	13.3
N_{layers}	20
R_c (Ω)	61.5
R_s (m Ω)	0.1
R_{load} (Ω)	50.0
Parameters for a single layer	
C_s (μ F)	96
L_{pl} (nH)	7.2
R_p (m Ω)	6.3
R_{sw} (m Ω)	84

for the 160 ns flat-top duration, as given in Table 3.1, has been reached when R_a of the analogue modulation layer equals to 6.0 Ω . A zoom of the pulse flat-top for this case is shown as $V_{load}, PM1$ in Fig. 5.44. In this simulation, the pulse capacitors of the constant voltage layers were initially charged to 754.2 V and the magnetising inductance of the core in the analogue modulation layer, L_{ma} , was 135 μ H. The droop of the pulse flat-top duration is 1.0 V (0.008 %). However, for 900 ns, the droop is 5.0 V (0.04 %). As has been explained in the previous chapters of this dissertation, the idea is to budget a half of the stability specification for the amplitude variations of the pulse flat-top for droop and the other half for ripple. Therefore, this result is not yet considered acceptable, despite the fact that the droop is within ± 0.02 %.

The next simulation was run with R_a equal to 6.3 Ω and a zoom of the flat-top of the load voltage is shown as $V_{load}, PM2$ in Fig. 5.44. The initial voltage of the pulse capacitors in the constant voltage layers was 757.3 V, L_{ma} was 135 μ H and R_a 6.3 Ω . This gives exactly 12.500 kV for the average value of the load voltage during the pulse flat-top. The droop of the load voltage during the flat-top is 0.2 V (0.002 %) for 160 ns and 2.0 V (0.016 %) for 900 ns. However, a point to note in this simulation study is the voltage across the resistor R_a in the analogue modulation layer during the pulse. In Fig. 5.45, $-V_{layer}, PM2$ shows the net voltage of a single

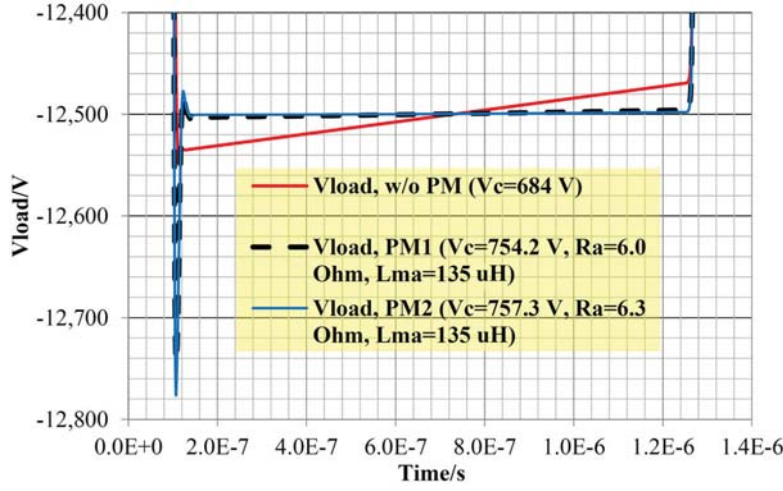


Figure 5.43. Simulated $V_{load, w/o PM}$ of the 20-layer inductive adder without passive analogue modulation, $V_{ci} = 684$ V and the primary of one layer was in short-circuit. $V_{load, PM1}$ is the simulated output waveform with passive analogue modulation layer with $V_{ci} = 754.2$ V, $R_a = 6.0 \Omega$ and $L_{ma} = 135 \mu\text{H}$. $V_{load, PM2}$ is the simulated output waveform with passive analogue modulation layer, $V_{ci} = 757.3$ V, $R_a = 6.3 \Omega$ and $L_{ma} = 135 \mu\text{H}$.

constant voltage layer, and $V_{Ra, PM2}$ shows the voltage across the resistor R_a in the analogue modulation layer for the same simulation. The voltage across the resistor R_a has a maximum amplitude of approximately 1520 V, whereas the net voltage across a constant voltage layer is approximately 730 V. These voltages are applied across the magnetic cores and the voltage across the analogue modulation layer is so high that the magnetic core could be driven into saturation. Another point to note is that the voltage across the resistor R_a is too high to connect an RF power transistor directly in parallel with a single resistor. The maximum drain-source voltage of the RF power transistor type ARF463AP1G, proposed in Table 5.7, is 500 V. Therefore, the resistance required for R_a should be made using a series network of resistors, in which the RF power transistor could be connected in parallel with a sub-resistor, which provides suitable voltage range for the operation of the RF power transistor.

In order to decrease the voltage across the analogue modulation layer, there are different options. Another analogue modulation layer could be added to the stack, in order to share the voltage stress of the analogue modulation layer into two layers, and effectively, across two magnetic cores. This could be achieved either by increasing the total number of the layers to 21, or by keeping the total number of layers 20, but reducing the number of constant voltage layers to 18 by increasing the initial voltage of the constant voltage layers by 5.6 %, from 757.3 V to 799.4 V.

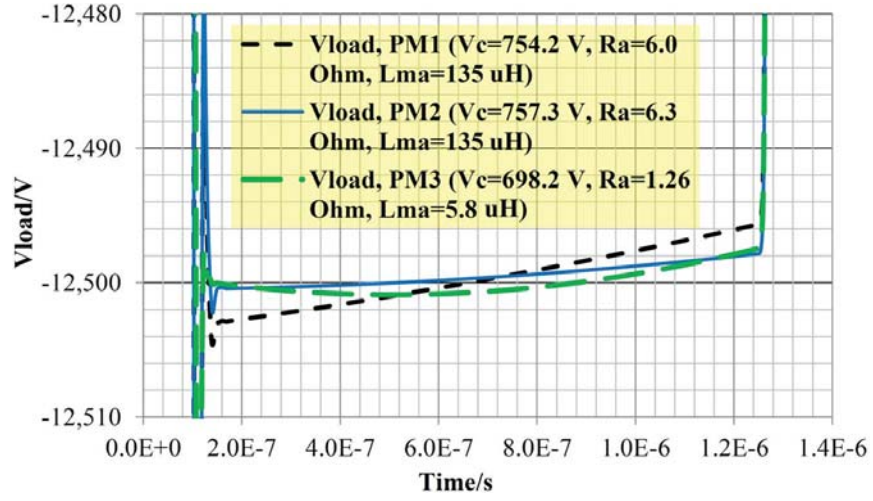


Figure 5.44. $V_{load, PM1}$ is the simulated output waveforms with passive analogue modulation layer with $R_a = 6.0 \Omega$, $L_{ma} = 135 \mu\text{H}$ and $V_{ci} = 754.2 \text{ V}$. $V_{load, PM2}$ is the simulated output waveform with $V_{ci} = 757.3 \text{ V}$, $R_a = 6.3 \Omega$ and $L_{ma} = 135 \mu\text{H}$. $V_{load, PM3}$ is the simulated output waveform with passive analogue modulation layer with $R_a = 1.26 \Omega$, $L_{ma} = 5.8 \mu\text{H}$ and $V_{ci} = 698.2 \text{ V}$.

Another solution would be to use a different type of the magnetic core in the analogue modulation layer, with a lower permeability, which would cause a larger compensating droop along the pulse. The value for resistor R_a can be defined according to the maximum allowed voltage across the analogue modulation layer during the pulse flat-top and the load current by applying Eq. (4.9). According to Eq. (4.10), a magnetic core with a lower magnetising inductance, i.e. lower permeability, would require less voltage to generate the compensating droop of the same magnitude, and the required magnetising inductance can be estimated with Eq. (4.11).

The final simulation was carried out with a lower magnetising inductance, L_{ma} equal to $5.8 \mu\text{H}$, and a smaller resistance value, R_a equal to 1.26Ω . In Fig. 5.44, $V_{load, PM3}$ also fulfils the requirements for the flat-top stability and the variation of the load voltage during the flat-top is 0.1 V (0.001%) for 160 ns and 2.1 V (0.017%) for 900 ns . The flat-top of the load voltage is slightly rounded and in fact, the load voltage increases from 150 ns to 550 ns . The voltage across resistor R_a for this simulation is shown as $V_{Ra, PM3}$ in Fig. 5.45 and its maximum value is 337 V . This is considerably less than in the previous simulation, shown as $V_{Ra, PM2}$ in the same figure.

Two simulated output waveforms, $V_{load, PM2}$ and $V_{load, PM3}$ in Fig. 5.44, fulfil the pulse flat-top stability requirements for both the 1 GHz and the 2 GHz versions of the CLIC DR kicker inductive adder, the specifications for which are shown in Table 3.1. However, in these simulations, the

non-linearity of the magnetising inductance of the magnetic cores has not been taken into account. This is a characteristic of the cores, which is not easy to include accurately in a simulation model without evaluating the cores. However, it is planned to use the cores in a linear range of the B-H curve if possible. Also, in these simulation, active analogue modulation has not been applied. The reason for this is that, once the behaviour of the non-ideal components for the full-power prototype are measured, it is straight-forward to generate the compensation signal to improve the pulse flat-top stability. If the B-H curve is non-linear, the gradient of the droop will increase during the pulse, because of the drop of the value of the magnetising inductance. However, based on the experimental results presented in Section 4.5.3, this can be compensated with the active analogue modulation.

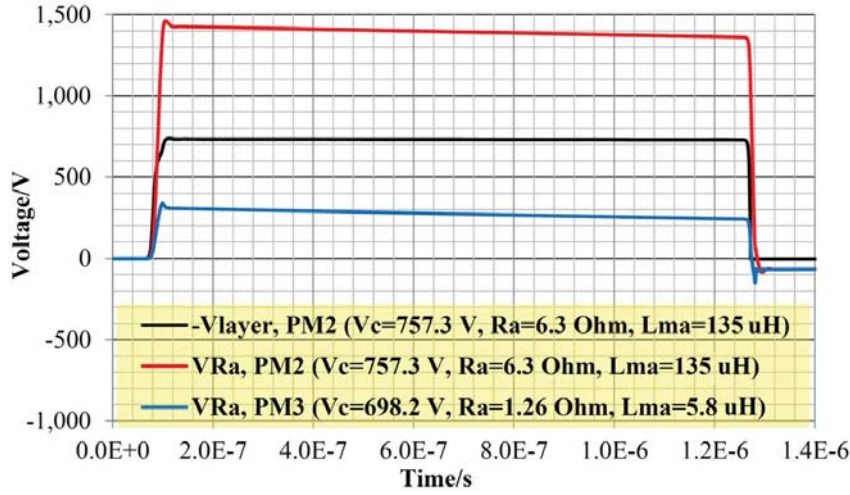


Figure 5.45. Simulated $V_{Ra, PM2}$ and $-V_{layer, PM2}$ of the 20-layer inductive adder with passive analogue modulation with $V_{ci} = 757.3$ V, $R_a = 6.3$ Ω and $L_{ma} = 135$ μ H. Simulated $V_{Ra, PM3}$ with passive analogue modulation, with $V_{ci} = 698.2$ V, $R_a = 1.26$ Ω and $L_{ma} = 5.8$ μ H.

5.7.1 Costs and Size

The cost of the inductive adder for a 50 Ω load scales approximately with voltage squared [68]. If the voltage is doubled, the number of layers is doubled. However, each layer needs to provide double the current which requires twice the number of semiconductor switches, and assuming one capacitor per switch, this would require twice the capacitance per layer. This may require that the size of PCBs is increased, in comparison with an inductive adder with a lower output voltage, to have enough space for increased number of capacitors and semiconductor switches. In addition

insulation requirements of the stack are increased, which may require that the inside diameter of the core housing and the inside diameter of the magnetic cores need to be increased. This may also require a larger outside diameter for the core housing, and therefore increase the minimum size of the half-layer PCBs.

Table 5.9. Cost estimate with the main contributors for a 12.5 kV, 250 A, 1 μ s, 20-layer, inductive adder for the CLIC DR kicker inductive adder consisting of 19 constant voltage layers and one analogue modulation layer.

Contributor	Cost/piece (euros)	Number needed	Costs (euros)	Costs (%)
Diodes	3	456	1,400	1
Flanges	250	40	10,000	9
HV feedthroughs	500	2	1,000	1
Magnetic cores	2,800	20	56,000	49
Other electrical components	4000	1	4,000	3
Other mechanical components	4000	1	4,000	3
PCBs	750	20	15,000	13
Power supplies	12,500	1	12,500	11
Pulse capacitors	20	152	3,000	3
Switches and gate drivers	30	152	4,600	4
Trigger system and cables	3,500	1	3,500	3
Total	n/a	n/a	115,000	100

The estimate for a 12.5 kV inductive adder for feeding a 50 Ω load with 1 μ s flat-top duration is 115,000 euros. This estimate is based on the costs of the two prototype inductive adders built at CERN and it includes the trigger system and DC power supplies. It does not include interlocking systems neither a cabinet. The contributors for the costs are shown in detail in Table 5.9. In this estimate, the costs of an analogue modulation layer are estimated to be equal to the costs of a constant voltage layer. The analogue modulation layer does not include pulse capacitors, switches, gate drivers and diodes but the same costs are expected for high-voltage resistors, RF power transistors and their gate drive circuits. The costs of these components are included in the sum of other electrical components in Table 5.9. The magnetic cores contribute approximately 50 % of the total costs of the CLIC DR kicker inductive adder. The PCBs for the

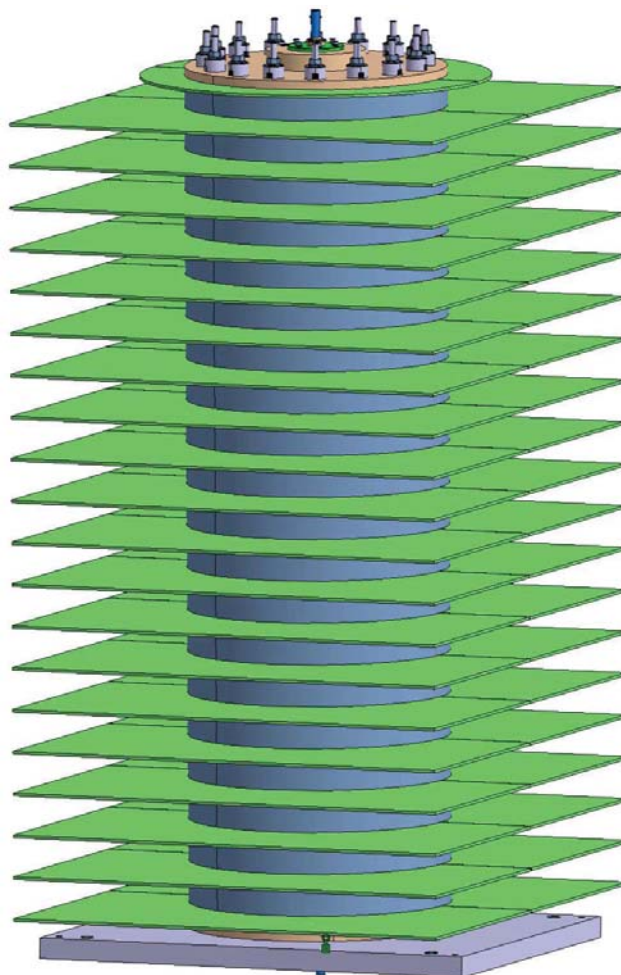


Figure 5.46. A 3D drawing of a 20-layer, 12.5 kV, prototype inductive adder for the CLIC DR extraction kicker system. Courtesy of P. Faure, 2015.

primaries, excluding semiconductor switches and pulse capacitors, contribute 13 % of the total costs and the mechanical flanges for the cells 9 % of the total costs. The semiconductor switches, gate drivers and diodes contribute 5 % and pulse capacitors 3 % of the total costs. The costs of DC power supplies are in total approximately 11 % of the costs of the 12.5 kV inductive adder. For a 50 Hz repetition rate, the adder stack can be air-cooled.

Figure 5.46 shows a 3D drawing for the 20-layer 12.5 kV prototype inductive adder for the CLIC DR kicker system. The mechanical and electrical design of this prototype adder is based on the design steps presented in this dissertation. The inductive adder in Fig. 5.46 is 70 cm wide, 70 cm deep and 120 cm high.

6. Conclusions

6.1 Main Results

This dissertation presents in detail a technological solution to meet the specifications of the pulse power modulator for the CLIC DR extraction kicker system starting from topology selection and ending with experimental verification of modulation techniques for compensating droop and ripple of the pulse waveform. According to a literature review presented in Chapter 2, the inductive adder was selected as the most promising topology for meeting the ripple and droop requirement for the pulse power modulator of the DR extraction kicker system. In Chapter 3, a complete preliminary design procedure is presented for a high-precision inductive adder, including component selection and mechanical design. According to simulations studies presented in Chapter 4, passive modulation was found to be effective in compensating the droop, and active analogue modulation to compensate both droop and ripple of the output waveform of an inductive adder. The experimental verification of these methods is presented in Chapter 5.

In the best measurement presented in this dissertation, in which the droop and the most significant ripple component of the pulse were actively compensated, the resulting flat-top stability of a 1.823 kV pulse was within ± 0.96 V, corresponding to ± 0.05 %, for 160 ns duration. This relative stability is better than the CLIC PDR extraction and DR injection kicker requirements, of ± 0.2 %, shown in Table 2.1. The total duration of the pulse was 400 ns including rise and fall times and the flat-top stability was measured for an average of 1000 pulses. Other measurement with the same set-up gave stability of ± 1.02 V (± 0.06 %) for averages of both 1000 and 4000 pulses. In the best measurements, in which only the droop

was actively compensated, the resulting flat-top stability of a 1.823 kV pulse was within ± 1.17 V (± 0.06 %) for an average of 1000 pulses and ± 1.23 V (± 0.07 %) for an average of 4000 pulses. According to the literature review presented in Chapter 2, and to the author's best knowledge, these are the best reported flat-top stabilities for such fast, high-voltage pulses with a resistive load.

In addition to droop and ripple compensation, this dissertation also includes other important results concerning the design of a high-performance inductive adder. A design method of estimating the primary loop inductance of an inductive adder, using FastHenry, has been presented and shown to be in good agreement with measurements. The simulation studies showed that in an application requiring very short rise time, less than 100 ns, the primary loop inductance of an inductive adder needs to be carefully considered. It was also shown that the impedance of the nominally 50 Ω air-insulated inductive adder, which is designed according to steps given in Chapter 3, was estimated to be 47.0-52.1 Ω in Chapter 4. This discrepancy of the output impedance could cause up to 15 ns difference for the settling time of stripline voltage of the CLIC DR extraction kicker system, however the effect depends on the rise time of the output pulse and the output impedance and typically, according to simulations, it is 1-3 ns. An important conclusion is that for striplines with an odd mode impedance of 41 Ω , terminated in 50 Ω , the optimum output impedance of the inductive adder, for rise times of 75 ns or more, is in the range of 45-50 Ω .

For the CLIC DR extraction kicker modulator, the absolute accuracy of ± 2.5 V would be enough to achieve the required ± 0.02 % flat-top stability for a 12.5 kV output pulse. Taking into consideration the literature review, simulation studies and presented experimental results, this dissertation presents technical solutions as to how the final flat-top stability requirement of ± 0.02 % of the CLIC DR extraction kicker modulators can be reached. Based on the measurements of the best measured flat-top stabilities, the precision of the voltage control capability of the active analogue modulation layer for the output waveform is at worst-case of the order of ± 1.0 V. The voltage accuracy of the output waveform was defined by the active analogue modulation layer itself and there is not an obvious reason foreseen why a higher output voltage would effect significantly the operation and precision of the analogue modulation layer. Also, the measurements on the prototype inductive adders did not raise any reason

that the mechanical design of the prototype inductive adders would not be scalable to higher voltages as is done in other laboratories. The absolute voltage accuracy of the analogue modulation layer could be degraded approximately by factor of 2.5 before the flat-top stability would be out of the specifications. If the relative flat-top stability could not be improved further from the demonstrated $\pm 0.05 \dots \pm 0.07 \%$, for 12.5 kV output pulses, the double kicker system presented in Chapter 2 could be a solution to meet the specifications. The double kicker system could provide a relative reduction of the ripple by factor up to 3.3 [37], which would relax the requirements for the pulse flat-top stability from $\pm 0.02 \%$ to $\pm 0.066 \%$. However the double kicker system is not a preferable solution because of its complexity and relative cost.

To conclude, this dissertation provides a feasible solution to meet the specifications of the CLIC DR extraction kicker modulator. All the steps to design, build and test a pulse power modulator with extremely high flat-top stability are covered in this dissertation. The most important methods to improve the flat-top stability of the output pulses of inductive adders, the passive and the active analogue modulation, were analysed by simulations and experimentally verified with the measurements. Therefore, the main goals of this research study were fulfilled.

6.2 Scientific Importance of Author's Work

The main scientific importance of this dissertation is that the author researched and proposed a method to generate fast, rectangular, high-voltage pulses with an extremely high flat-top stability. Typically, the flat-top stability of existing pulse power modulators is in the order of 1 %. The best measured flat-top stabilities reported in this dissertation are for 1.823 kV pulses, for which the flat-top stability was $\pm 0.05 \dots \pm 0.07 \%$ ($\pm 0.96 \dots \pm 1.23$ V) for 160 ns flat-top duration. The total duration of the pulses was 400 ns including rise and fall times and the pulses were fed to a 50Ω load. The flat-top stabilities were measured for averages of 1000 or 4000 pulses. Either the droop, or the droop and the most significant ripple component of the output waveform were actively compensated. According to the extensive literature review presented in Chapter 2, and to the author's best knowledge, these are the most precise reported flat-top stability results for such fast, high-voltage pulses with a resistive load. The author has been the main contributor to this work and he has done

the study independently of other researchers.

The second most important subject with scientific importance is that the author demonstrated, with prototype inductive adders, generation of actively modulated, high-voltage, pulse waveforms with very good accuracy. The active filtering of a ripple component was successfully demonstrated and the droop, which consists of considerably lower frequencies than the ripple, was compensated practically to zero. Based on these measurements, the precision of the voltage control capability of the active analogue modulation layer for the output waveform is at worst-case of the order of ± 1.0 V. It was also demonstrated with the measurements that waveforms, other than flat-top pulses, can be generated by applying the active analogue modulation, within the modulation range of the pulse modulator. The active, precise pulse shaping can be used, for example, to compensate non-linearities of a load in pulse power systems. According to the literature review of this dissertation and to the author's best knowledge, the accuracy of the droop compensation and demonstration of active ripple compensation reported in the dissertation are unique for a pulse power modulator generating such fast, high-voltage pulses with a resistive load. The author has been the main contributor to this work and he has done the study independently.

The third result of this dissertation which has scientific importance is that the author showed with simulations that applying either a passive or an active analogue modulation method is necessary in order to achieve very low droop, much less than 1 %, for the output pulse of an inductive adder. Adding more capacitance per layer does not decrease the droop of the output pulse which is caused by contributors other than the capacitors themselves. The resistive losses of the semiconductor switches and increasing magnetising current need to be taken into consideration in estimating the droop of the output waveform. This is a crucial aspect for designing the inductive adder with extremely high flat-top stability, for example for the CLIC DR extraction kicker system. According to the author's best knowledge, this design issue of the inductive adders has not been reported earlier in the literature. The author has been the sole contributor to this work.

The fourth point regarding the scientific importance is that this study is a significant part of the feasibility study of the CLIC accelerator project at CERN. The specifications for the stability of the output waveforms of the DR extraction kicker modulators are set by the beam parameters of

the collider. In the best measured results presented in this dissertation the relative accuracy of the flat-top stability ($\pm 0.05 \dots \pm 0.07 \%$) was 2.5-3.5 times larger than allowed for the CLIC DR extraction kicker modulator ($\pm 0.02 \%$). However, use of a double kicker system could relax the requirements for the pulse flat-top stability up to $\pm 0.066 \%$. Also, in the same measurements, the absolute voltage range of the flat-top stability ($\pm 0.96 \dots \pm 1.23 \text{ V}$) was 40-50 % of the allowed absolute flat-top stability of the CLIC DR extraction kicker modulator ($\pm 2.5 \text{ V}$), although this has not been demonstrated at full output voltage of the CLIC DR extraction kicker modulator. To conclude, the author has presented a solution to meet the specifications of the CLIC DR extraction kicker modulator and demonstrated the feasibility of the technology with the prototype inductive adders. The author has been the main contributor to this work.

Fast, high-precision, high-voltage pulse power systems are needed in various fields of technology. The literature survey in Chapter 2 showed that the pulse flat-top stability of existing power modulators is typically 1 % or worse. According to the literature review, inductive adders have been used, for example, to power kicker magnets and striplines, to drive klystrons in particle accelerators, and to drive Pockels cells in a research facility for fusion energy. High-voltage pulse power modulators are also used in medical radiotherapy devices, in military applications e.g. to power RF amplifiers for radars, and in industrial applications e.g. in X-ray scanners. The improvement of the pulse flat-top stability could potentially provide benefits for many of these applications. In kicker systems, the droop and the ripple of the pulse flat-top increases the beam emittance. In klystron modulators, the flat-top ripple of the output pulse of the modulator causes phase shifts in the output RF voltage of the klystron, which also may lead to emittance blow-up of the beam. Improved flat-top stability in these applications would allow to decrease the beam emittance, which is desirable especially for synchrotron light sources and free electron lasers. In medical radiotherapy accelerators, the improved precision of the pulse flat-top of the modulators, which are used to drive klystrons and to power kicker systems, could improve the precision of the delivery of the doses [89]. In a radar system, the stability of the pulses of the modulator, which feeds an RF amplifier, defines the accuracy and consistency of the data which the radar produces [170]. In industrial applications of X-ray sources, the improvement of the pulse flat-top stability of the modulator could increase the efficiency of radiation and therefore reduce the

need for cooling and radiation shielding [89]. To conclude, the technology to improve the flat-top stability of the high-voltage pulse power modulator presented in this dissertation may potentially be beneficial for many types of applications in the future. The complete design procedure for the inductive adder, including component selection, mechanical design and design of the analogue modulation layer, has not been presented in the literature previously.

6.3 Proposals for Future Work

The research work on the CLIC DR extraction kicker system will be continued at CERN. The prototype adders will be tested together with the prototype stripline kicker with bipolar pulses. The prototype adders will also be operated with all four branches powered in each half-layer PCB, to test the full current and the full voltage capability. The prototype inductive adders and the measurement set-up will be further improved in order to attempt to achieve the final specifications for the relative flat-top stability of the CLIC DR extraction kicker system. The inductive adders will be equipped with larger magnetic cores in order to permit a longer duration for the output pulses. This would allow longer settling time, which could further reduce the ripple of the flat-top. Also, the longer output pulses would improve the frequency resolution of the FFT algorithm, computed for the output waveform. The improved resolution of the computed ripple content of the output waveform would allow to generate a more accurate compensation waveform, which could allow to improve the flat-top stability even further. The PCB design of the prototype inductive adder could be improved to minimise the primary loop inductance, e.g. by complete metallisation of the underside of the half-layer PCBs. A reliable over-current detection and protection circuit will also be needed for the full-power, 12.5 kV, inductive adder, in order to limit fault currents e.g. in the case of a short-circuit in the load.

The operation of the analogue modulation layer could be improved further. In the measurements presented in this dissertation, the precision for the output waveform was limited by the control precision of the analogue modulation layer and by the limited frequency and amplitude accuracy of the FFT, computed for the output waveform. Also, only one frequency component was compensated. Despite these limitations, the droop, which consists of lower frequencies, was compensated completely. However, there

was no amplifier between the signal generator, which fed the modulation signal, and the RF power transistor in the analogue modulation layer. The phase and amplitude precision of the analogue modulation layer was defined by the current feeding capability of the signal generator. Another drawback, caused by the missing amplifier, was that the impedance of the signal generator and the cable was seen by the RF power transistor of the analogue modulation layer. In the measurements which were done for this dissertation, any change of settings of the signal generator, the interconnecting cables, or the DC supply for biasing voltage, affected the operation of the analogue modulation layer. An RF amplifier between the signal generator and the RF power transistor would allow more precise control of the current through the RF power transistor.

The ability of the active analogue modulation to filter ripple components of the output waveform could be further improved by repeating the correction, in an iterative manner, in several steps. As discussed in Chapter 4, the FFT could be taken again for an average of the multiple recorded pulses of the corrected output waveform. The second compensation signal would be computed, summed with the first signal, and applied. This iterative procedure could be done automatically with a laboratory computer and repeated until the ripple cannot be reduced any more. The control system could automatically compensate fast and slow variations of the kicker system with a mix of feedback and feed-forward control schemes. The number of recorded pulses chosen is a compromise between minimising asynchronous ripple and the effects of thermal and short-term drifts.

In this dissertation, the main goal has been to improve the flat-top stability of the inductive adder. However, the off-time voltage, i.e. the load voltage between the output pulses, is also required to be very low, ± 2.5 V, for the CLIC DR extraction kicker inductive adder. Even if the magnetic cores would be reset by diodes which are connected in series with Zener diodes to shorten the decay time, a low decaying voltage would be applied across the load for a relatively long time. The decaying voltage could be possibly compensated by adding a special constant voltage layer and an active modulation layer to the inductive adder stack and generate an equal but opposite polarity voltage in comparison with the reset circuit during the decay time. Another solution could be to connect an array of parallel diodes to the output of the inductive adder, which would provide a low impedance current path for the off-time current, which has an opposite polarity in comparison with the normal output pulse.

Repeatability, in other words long-term stability, of the output pulses of the prototype inductive adders was not considered in this dissertation. It could be measured with a set-up in which two inductive adders feed a single current transformer. The nominally zero output of the current transformer could be measured in different cases, at first when both adders are either recently turned on or have operated for an extended period, and then one having operated for an extended period and the other recently turned on. These experiments would give data of possible short-term or long-term drift of the pulse flat-tops and changes of droop and ripple, and therefore the repeatability of the output waveforms of the prototype inductive adders.

Finally, two full-size 12.5 kV prototype inductive adders will be built with nominal specifications for the CLIC DR extraction kicker systems. These modulators will be tested together with a prototype stripline kicker in an accelerator test facility. If the required relative accuracy of measurement, better than $\pm 0.02\%$ at 12.5 kV, is impossible to achieve in direct electrical measurements in the laboratory, the measurement in a suitable test facility, with adequate beam instrumentation, could provide the desired accuracy. The deflection angle and the induced jitter to the beam will be recorded with high-precision beam position monitors. With these measurements, it should be possible to verify the performance of the inductive adders and the complete kicker system with the required stability. New oscilloscopes with high sampling rates and high-quality ADCs with increased bit lengths are also available, which would allow to improve the resolution of the direct electrical measurements [171]. An optical current measurement system, presented in [172], could also theoretically allow very high precision and high dynamic range for the measurement of the output pulses.

The inductive adder technology is seen as a promising technology for many future research projects at CERN as well as for replacing obsolete technology in old existing systems. The feasibility study for the CLIC DR extraction kicker system has required and will require new technological developments. The dissertation verified that the required absolute flat-top stability is feasible with high-voltage pulses and that the required relative precision could also very probably be achieved. As mentioned above, these new advances for the flat-top stability of the high-voltage pulse power modulators can potentially have new applications in various fields of particle accelerator technology.

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Appendix A: Assembly of the Prototype Inductive Adders

Mechanical Assembly of the Prototype Inductive Adder Stack

The dimensions of the adder stack have been defined according to the design principles presented in Chapter 3. The prototype inductive adder consists of five layers. Each magnetic core is enclosed between a top flange and a bottom flange, the latter of which is connected to ground potential. The pair of flanges is attached together, on its inside diameter, with screws to create a mechanical support for the printed circuit boards (PCB), as shown in Fig. A1.

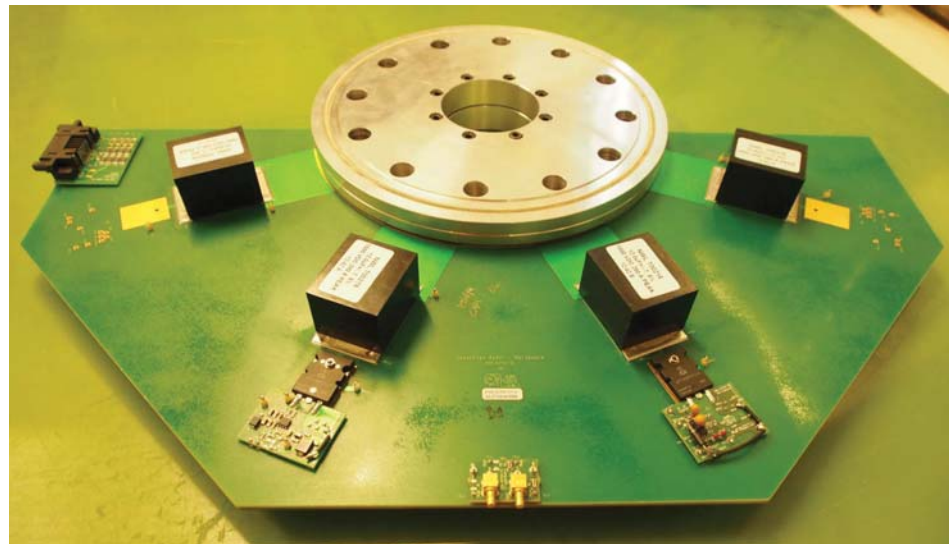


Figure A1. A single cell of an inductive adder with a half-layer PCB.

Each layer is assembled into an inductive adder stack: the core assemblies are attached to each other with threaded bars. Fig. A2 shows a photo of the assembly of the prototype inductive adder with a single core assembly installed (left). The prototype adder was assembled on a support,

which was made of pieces of transparent acrylic sheets. Each flange of the adder stack has a machined groove on its top and bottom surfaces. These grooves have been designed for canted coil springs. The PCBs of the primary circuits are inserted between the flanges and the canted coil springs provide good, high-frequency, electrical contact and mechanical force between the flanges and PCBs of the primary circuits. Fig. A3 shows details of the structure of the adder stack, including canted coil springs installed in the grooves, and spacers between bottom flanges.

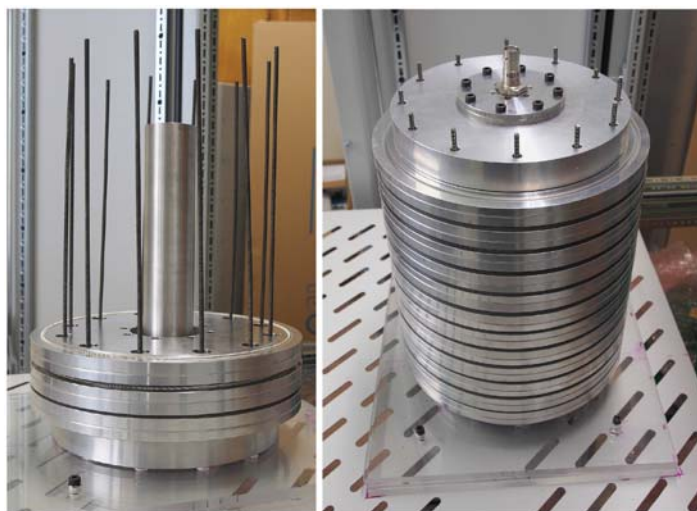


Figure A2. Assembly of the prototype adder stack with a core assembly (left) and a complete inductive adder stack without PCBs (right).

Figure A4 shows a photo of the adder stack assembly from the top. A top flange is shown on the top of the stack and the metal spacers, which are fed through but insulated from the top flange, are clearly visible. The voltage between a top flange and a conducting metal spacer, which is at

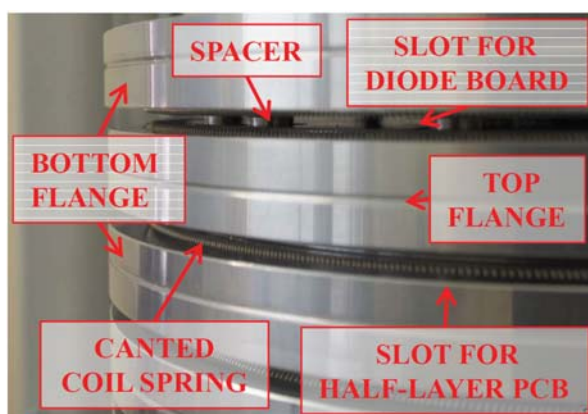


Figure A3. Canted coil springs are assembled in the upper and lower grooves of the flanges. The bottom flanges of adjacent layers are electrically connected together with metal spacers.

ground potential, is nominally 700 V. The metal spacers have an outside diameter of 8 mm and they are centered in holes which have diameters of 12 mm. Therefore, there is a 2 mm air gap between the top flange and the spacers (Fig. A4). The secondary winding, the stalk, is also assembled into the stack.

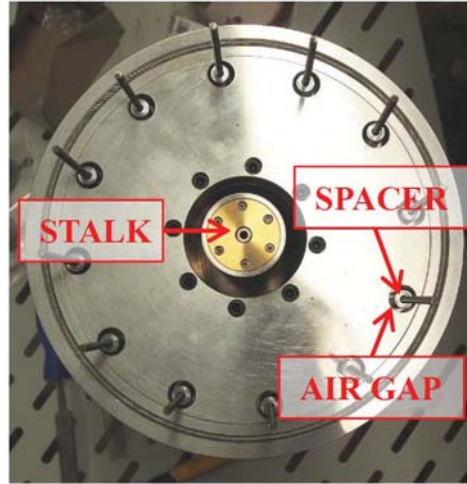


Figure A4. A top flange with metal spacers, which are fed through it.

Figure A2 (right) shows the complete adder stack without PCBs and with a high-voltage output connector on the top. The prototype adder has output connectors on both ends, therefore it can be used to generate positive or negative pulses, depending on which end of the adder stack is grounded. The grounding can be made by connecting a short-circuited connector plug into one of the output connectors.

Design of the Printed Circuit Boards

A single layer of the prototype inductive adder consists of two half-layer PCBs, each of which includes four parallel current branches. The number of the semiconductor switches per layer is defined either by the current rating of the switch or the number of capacitors required per layer. The storage capacitors chosen for the prototype adder are large in comparison with the switches, therefore the number of the switches was chosen to be equal to the number of the capacitors, in order to keep the loop resistance of the primary circuits and the primary loop inductance low. Each current branch comprises a storage capacitor, a MOSFET switch and a driver board. Fig. A5 presents a photo of a half-layer PCB of the prototype inductive adder. Half-layer PCBs are connected between a high-voltage

flange and a ground flange. The half-layer PCB has several daughter boards, namely a trigger board, a connector board and four driver boards (Fig. A5).

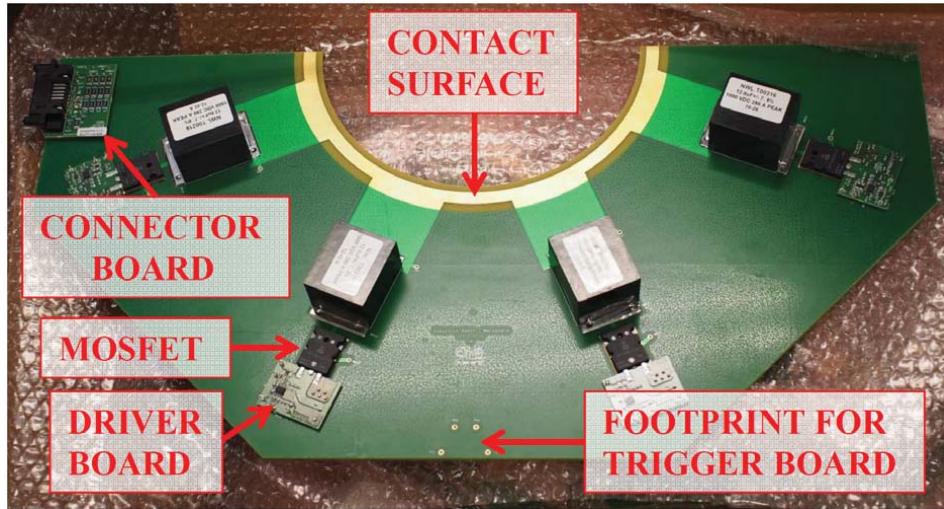


Figure A5. A single half-layer PCB of the prototype inductive adder.

In order to make testing and replacing of parts, in the case of failure or upgrade, easy, the daughter boards are connected into each half-layer prototype PCB with plug-in connectors, as is shown in Fig. A6. The gold plated receptacles and pins are manufactured by Mill-Max [173]. The chosen connectors, types 0328 and 3102, had been reliable in similar applications at LLNL [68]. Each half-layer PCB includes four $12\ \mu\text{F}$ pulse capacitors and the total capacitance per layer is $96\ \mu\text{F}$. According to Eq. (3.4) presented in Chapter 3, this would ideally allow to achieve 0.02 % of droop for a 160 ns long pulse flat-top with 70 A of load current.

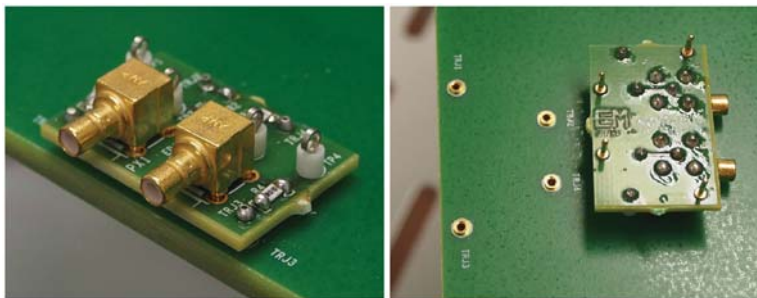


Figure A6. A trigger board of the prototype inductive adder, plugged into a half-layer PCB (left), and plug-in connectors for connecting daughter boards, in this case a trigger board, to a half-layer PCB (right).

The trigger board, shown in Fig. A6 (left), feeds trigger signals for the half-layer PCB to control the semiconductor switches. The connector board, shown in Fig. A7 (left), feeds high-voltage (700 V) DC to the half-

layer PCB for charging the storage capacitors. It also feeds low-voltage DC to the half-layer PCB, for the gate drive circuits. The connector board also houses resistors for limiting charging current from the 700 V DC power supply. The charging resistors are effectively 200 Ω resistors consisting of two 100 Ω resistors in series.

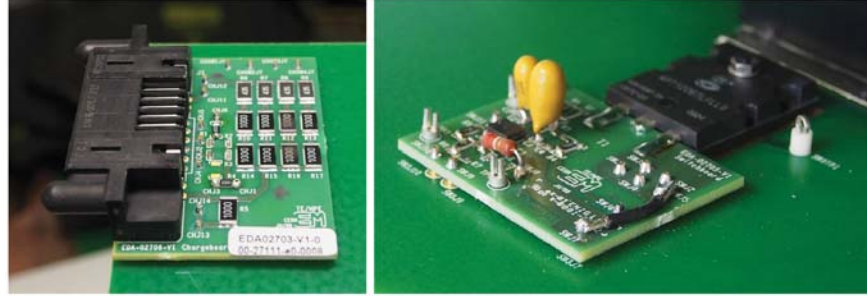


Figure A7. A connector board with a charging resistor network, plugged into a half-layer PCB (left) and a driver board of the prototype inductive adder (right).

The driver board, shown in Fig. A7 (right), includes a gate drive circuit. It receives both the DC voltage for the gate driver and the trigger signal via the half-layer PCB. The output of the driver board is connected to the gate and source pins of the semiconductor switch. The drain pin of the chosen MOSFET switch is internally connected to the metal bottom side of its package, and this wide flat contact is connected to the half-layer PCB by conducting copper tape. The good electrical contact is ensured by a screw, which fastens the MOSFET tightly on the half-layer PCB (Fig. A7, on the right).

The diode board, shown in Fig. A8, includes fast clamping diodes to provide a low inductance path for the inductive load current when the semiconductor switches are turning off. On the other side, which is not visible in Fig. A8, it also includes soldering pads for transient voltage suppressors or Zener diodes on series with the diodes, which may be installed later to increase the conducting threshold voltage of the clamping diodes, in order to shorten the resetting time of the magnetic cores. Each layer includes two semi-circular diode boards and these have similar contact surfaces as the half-layer PCBs. Diode boards are connected between a high-voltage flange and a ground flange. The ground flanges of the adder stack are electrically connected together with metal spacers, which are fed through high-voltage flanges. This approach provides a short, low inductance, path for the diode current.

Figure A9 shows the complete prototype inductive adder. The narrow connector board in front of the adder feeds the high voltage for pulse ca-



Figure A8. A diode board of the prototype inductive adder.

capacitors and low operating voltage for the gate drive circuits in the half-layer PCBs of the adder stack. The high-voltage output of the top end of the adder is connected to the load with a high-voltage cable. The bottom end connector, which is not visible in A9, is connected to ground with a short-circuited high-voltage plug.

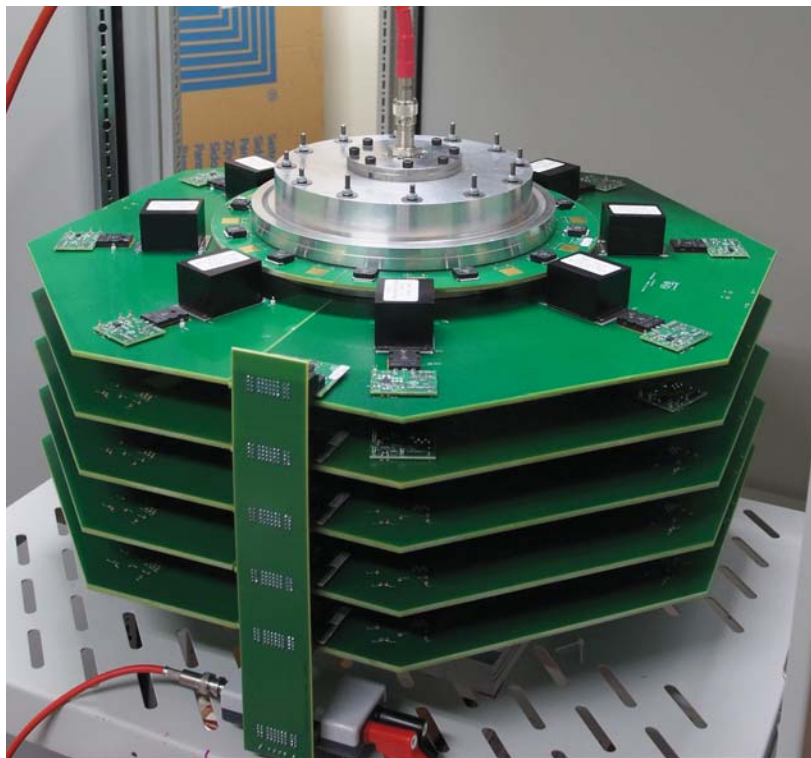


Figure A9. The complete prototype inductive adder.

Appendix B: Evaluation of Magnetic Cores for an Inductive Adder

Table B1 shows the evaluated core materials and the dimensions of the cores. Finemet FT-3L [160], is made of nanocrystalline material and manufactured by Hitachi-Metals [161]. Metglas 2605CO [111], 2605HB1M [162] and 2605SA1 [163] are made of annealed amorphous alloys and manufactured by Metglas (Now part of Hitachi-Metals) [164]. A Permagan Sample 1 core, manufactured by Permagan Ltd. [165], is also made of amorphous material. The last row, core W567, is made of nanocrystalline material Vitroperm 500 F and manufactured by Vacuumschmelze [134]. In Table B1, l_c is the height, D_2 is the inside diameter, D_3 is the outside diameter, A_c is the total cross-sectional area, $A_{c,eff}$ is the effective cross-sectional area, C_{PF} is the packing factor and V_e is the volume of the core.

Pulse Responses of a Single Layer without Biasing of the Cores

Figure B1 shows the measured voltage pulse responses of the six evaluated cores. In this measurement, a single layer of an inductive adder with two current branches was powered and the load voltage of a $50\ \Omega$ load was measured. The initial charging voltage of the pulse capacitors, V_{ci} , was chosen to be relatively low, 250 V, in order to obtain a pulse response of a single layer for each type of the cores. The cores were not biased before the pulse and the pulses were measured with 1 Hz repetition rate. The pulse flat-top duration was set to $1.0\ \mu s$. In Fig. B1, the estimated flux density swing is shown for each core and it has been computed by applying Eq. (3.6).

In Fig. B1, Finemet FT-3L (blue) and Vacuumschmelze W567 (green), have the lowest losses during the pulse and the load voltage at the beginning of the pulse, at 150 ns, is approximately 240 V for both cores. For

Table B1. Dimensions of the evaluated magnetic cores.

Core	l_c (mm)	D_2 (mm)	D_3 (mm)	A_c (cm ²)	$A_{c,eff}$ (cm ²)	C_{PF}	V_e (cm ³)
Finemet FT-3L	25.0	91	160	8.63	5.82	0.68	340
Metglas 2605CO	32.0	94	160	10.6	7.39	0.70*	421
Metglas 2605HB1M	25.4	91	160	8.63	6.13	0.70*	346
Metglas 2605SA1	25.4	91	160	8.63	6.13	0.70*	346
Permag Sample 1	30.0	92	160.0	10.2	8.67	0.85	404
Vacuum- schmelze W567	28.5	95	135	6.3	2.85	0.51	203

* estimate

Metglas 2605HB1M, 2605SA1 and for the Permag core, the losses are considerably higher and the load voltages at time point 150 ns are 230-235 V. Metglas 2605CO has the highest losses and the load voltage reaches only 200 V. In Fig. B1, it can be seen that Finemet FT-3L has the highest magnetising inductance, because the load voltage decreases only a few volts during the pulse flat-top, which means that it causes the lowest droop of the capacitors because the current is the lowest. With W567 core, the load voltage drops from 245 V to 220 V during the pulse flat-top. For Metglas 2605HB1M, the droop of the pulse flat-top is 30 V, for Permag Sample 1 the droop is 50 V and for Metglas 2605SA1, the droop is 70 V. For Metglas 2605CO, the pulse is terminated at 490 ns, because the rapid decrease of the load voltage indicates that the magnetising inductance is very low and that the current through the magnetising inductance is reaching a very high value.

The measurements shown in Fig. B1 are measurements for single cores. The measurements were repeated for five sample cores of Finemet FT-3L and ten W567 cores, and the differences between the evaluated cores of the same types were not significant. The pulse measurements were also

repeated for three samples of Metglas 2605CO cores and five pieces of Permagan cores with similar results. For Metglas 2605HB1M and 2605SA1, only single sample cores were available to be evaluated.

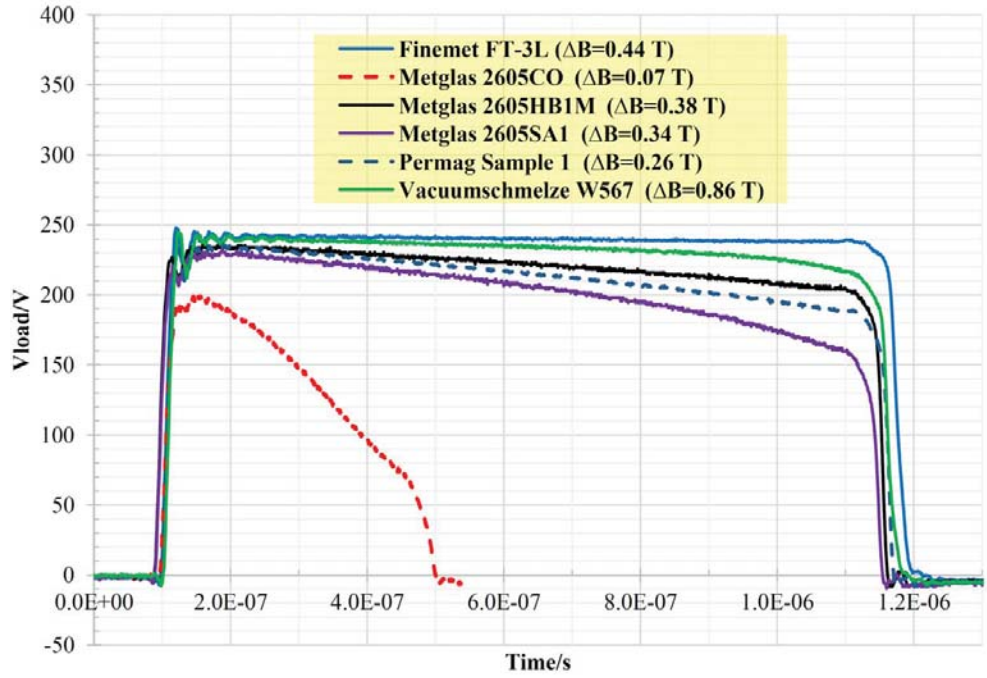


Figure B1. Load voltage of an inductive adder with a single layer operating with different cores. Two branches powered, $V_{ci} = 250$ V and the cores were not biased before the pulse.

Pulse Response of a Single Layer with Biasing of the Cores

Figure B2 shows the pulse responses of the six evaluated core in the case, when 8 A of DC current was fed through the cores by a biasing circuit. In the measurement, a single layer with a single current branch was powered and the pulse capacitors of the layer were initially charged to 700 V, which corresponds to the nominal operation voltage of a single layer. The pulses were measured with a 1 Hz repetition rate. The pulse flat-top duration for each measurements was defined to be the time by which the voltage of the pulse flat-top had decreased by approximately 10 % of the maximum flat-top voltage.

In Fig. B2, Finemet FT-3L (blue) and Vacuumschmelze W567 (green) have the lowest losses during the pulse and the load voltage at the beginning of the pulse, at 150 ns, is approximately 680 V for both cores. The droop of the pulse flat-top is slightly larger for Vacuumschmelze W567, but the characteristics of these two cores are close to each other. The pulse

duration is approximately $1.0 \mu\text{s}$ for Vacuumschmelze W567 and $1.5 \mu\text{s}$ for Finemet FT-3L. According to Table B1, the effective cross-sectional size of the Finemet core is two times larger, which would ideally give two times longer pulse with the same material. Hence the maximum usable flux-swing, with the applied biasing current, 8 A, is higher for Vacuumschmelze W567 than for Finemet FT-3L.

In Fig. B2, Metglas 2605HB1M (black) and 2605SA1 (purple) have very similar characteristics. The maximum load voltage is 660 V for both cores and the pulse duration is $2.4 \mu\text{s}$ for 2605HB1M and $2.5 \mu\text{s}$ for 2605SA1. The losses of these cores are higher than the losses of Finemet FT-3L and Vacuumschmelze W567 cores. However, the droop of the pulse flat-top is very low for the first $1.5 \mu\text{s}$, which indicates that the magnetising inductance is almost constant for that time period and, therefore, the B-H curves of these cores are close to linear in these operating conditions.

The curves of measured load voltages with Metglas 2605CO core and the Permagan core in Fig. B2 are approximately 590 V at the beginning of the pulse, at 700 ns. However, with Permagan Sample 1 core, the load voltage drops to 560 V after a fast transient and the load voltage with Metglas 2605CO increase until $1.7 \mu\text{s}$ and reaches 620 V at its culmination point. Both of these curves increase during, approximately, half of their durations. This phenomenon is most probably caused by a thermal effect in the switch. These cores give the two lowest load voltages, which indicates that the losses are highest, and the primary currents, which flow through the semiconductor switch, are the two highest for these cores.

Measurements on the Magnetising Inductances and Core Loss Resistances

The goal of these measurements was to characterise different core materials and not to qualify the products or the manufacturers, and therefore, the results of the measurements are shown for single samples. A half-layer PCB of an inductive adder was modified to allow to measure the current of a single current branch. A short surface track of a PCB was carefully cut and a bent piece of 4 mm wide, 0.5 mm thick sheet of copper was soldered to replace the removed PCB track. Fig. B3 shows a photo of the measurement set-up. In these measurements, only a single branch of the layer of an inductive adder was powered, and therefore, the measured current was the total current flowing in the primary circuit.

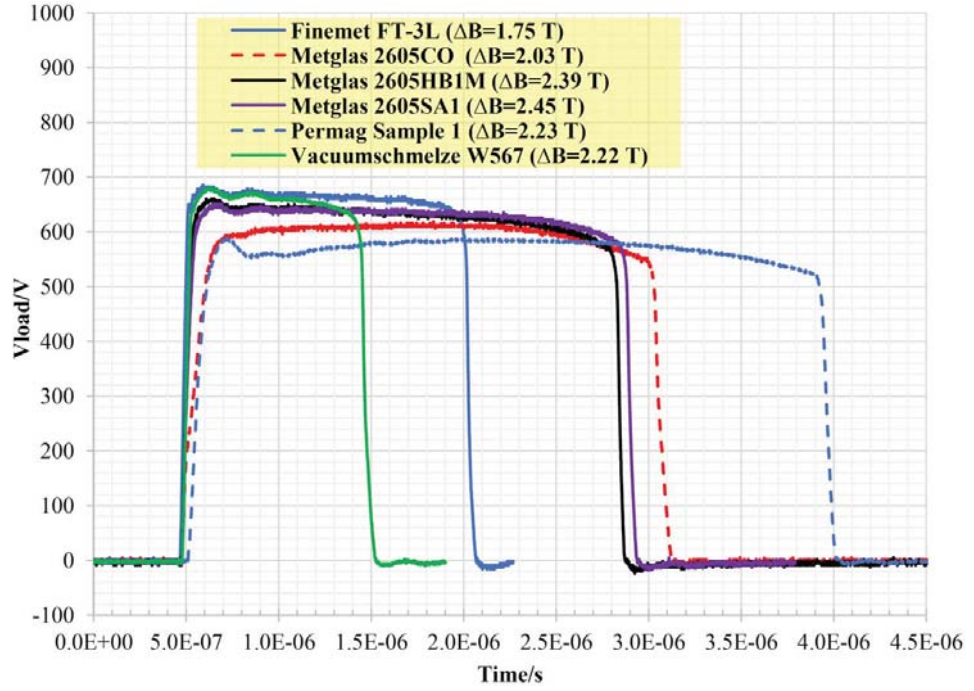


Figure B2. Load voltage of an inductive adder with a single layer operating with different cores. A single branch per layer powered, $V_{ci} = 700$ V and the cores were biased with 8 A of DC current.

The current was measured with a current waveform transducer, which is based on the Rogowski coil principle. The current transducer was type 30, made by Power Electronic Measurements [174]. The measurements were completed for all the cores shown in Table B1. The core loss resistance R_c was evaluated from the magnitude of the stepwise increase of the current within 100 ns from the beginning of the pulse. The magnetising inductance L_m was evaluated from the gradient of the measured current. The current was evaluated up to 100 A, after which the pulse was terminated by turning the MOSFET off. In these measurements, the inductive

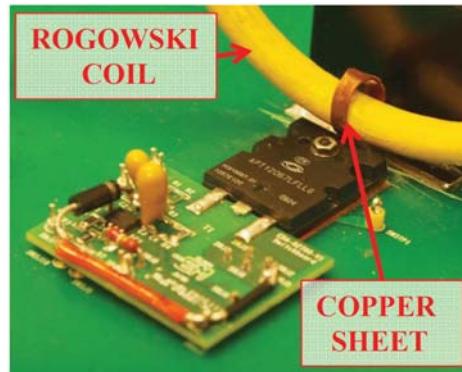


Figure B3. Measurement set-up for measuring magnetising current. The yellow cable is a Rogowski coil current transducer.

adder was not connected to the load and the secondary stalk was effectively an open circuit. Therefore, there was not a load current flowing in the primary circuit. The on-state resistance of the MOSFET switch was estimated to be $0.67 \, \Omega$ [101] and it was taken into consideration in estimating the core loss resistance.

Table B2 gives a summary of the measurements. In the table, V_{ci} is the initial capacitor voltage of the single layer of the inductive adder and I_b is the applied biasing current. $I_{Lm,max}$ is the magnetising current at the time when the pulse was terminated, and t_p is the pulse duration until $I_{Lm,max}$ was reached. R_c is the estimated core loss resistance, L_m is the magnetising inductance and μ_r is the relative permeability of the core material. Two values, estimated minimum and maximum, are given for parameters L_m and μ_r . The maximum values are estimates for the beginning of the pulse, immediately after the stepwise rise of the current into the core loss resistance, and the minimum values are estimates at the time when the magnetising current reaches $I_{Lm,max}$.

Table B2. Measured core loss resistance and magnetising inductance of candidate magnetic cores for the inductive adders.

Core	V_{ci} (V)	I_b (A)	$I_{Lm,max}$ (A)	t_p (μs)	R_c (Ω)	L_m (μH) max min	μ_r $\times 10^3$ max min
Finemet FT-3L	700	0	100	0.9	25.0	110 0.9	57.6 0.5
	700	8	100	1.7	25.1	40.1 1.9	21.1 1.0
Metglas 2605CO	700	1	100	3.3	6.2	n/a* 39.5	n/a* 16.6
	700	8	100	3.5	6.3	n/a* 39.4	n/a* 16.5
Metglas 2605HB1M	700	1	100	1.1	8.4	12.7 7.4	6.3 3.7
	700	8	100	2.4	8.6	29.2 10.1	14.6 5.0
Metglas 2605SA1	700	1	100	2.1	8.4	n/a* 5.2	n/a* 2.6
	700	8	100	2.6	8.3	36.2 3.3	18.0 1.6
Permag Sample 1	700	1	100	0.5	10.5	7.4 3.8	2.6 1.4
	700	8	100	3.8	10.6	n/a* 10.9	n/a* 3.9
Vacuum- schmelze W567	500	0	100	0.6	25.3	4.9 0.8	4.8 0.8
	700	8	100	1.1	24.8	16.0 1.4	16.0 1.4

* Maximum L_m cannot be defined because I_{Lm} did not increase monotonically during the pulse

In various pulse power systems in scientific research, medical and military applications, improvement of flat-top stability of the output waveform of the pulse modulator could provide higher performance for the complete system. This dissertation presents an extensive design guide for an inductive adder with extremely high flat-top stability. It covers detailed electrical and mechanical design, and both theoretical confirmation and experimental proof of applying passive and active modulation methods to improve the flat-top stability. The target application is a kicker system of the Compact Linear Collider (CLIC) at CERN. Methods to measure fast, short duration, high-voltage pulses are also presented, which makes this dissertation invaluable reading for researchers and engineers designing advanced pulse power systems with demanding flat-top stability requirements.



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