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Micro-fabricated Silicon Devices for Advanced Thermal Management and Integration of Particle Tracking Detectors

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Abstract

Since their first studies targeting the cooling of high-power computing chips, micro-channel devices are proven to provide a very efficient cooling system. In the last years micro-channel cooling has been successfully applied to the cooling of particle detectors at CERN. Thanks to their high thermal efficiency, they can guarantee a good heat sink for the cooling of silicon trackers, fundamental for the reduction of the radiation damage caused by the beam interactions. The radiation damage on the silicon detector is increasing with temperature and furthermore the detectors are producing heat that should be dissipated in the supporting structure. Micro-channels guarantee a distributed and uniform thermal exchange, thanks to the high flexibility of the micro-fabrication process that allows a large variety of channel designs. The thin nature of the micro-channels etched inside silicon wafers, is fulfilling the physics requirement of minimization of the material crossed by the particle beam. Furthermore micro-channels are well suited to be fabricated in silicon, as the same material of the detector they need to cool, and in this way mechanical stresses due to thermal gradients and different Coefficients of Thermal Expansion are minimized in the structure.

The silicon micro-channel device fabrication starts with the etching of the channels in a silicon wafer, followed by the bonding of a cover wafer in silicon (or in Pyrex for testing purposes) to close the channels, and ends with the etching of the fluidic apertures for the fluid circulation. The fluid circulating inside can be in single phase or two phase flow and the flow parameters like pressure, temperature or mass flow, can vary following each detector requirements. After the micro-fabrication of the cooling devices, thermal and fluidic tests are done to validate the channels performances before integrating them in the detector structure. The mechanical integration inside the detector starts with the equipment of the device with fluidic connectors for the fluid circulation, is followed by the gluing of the detector on the micro-channels surface, and ends with the mechanical jigs and supports needed to integrate the cooling in the detector structure.

The first High Energy Physics experiment pioneering micro-channel cooling was the NA62 detector who chose to cool its three GTK stations with a micro-channel plate circulating C_6F_{14} in liquid flow. The LHCb VELO detector has chosen a CO_2 evaporative flow in micro-channels for its upgrade in 2018. The ATLAS and ALICE detectors are evaluating the possibility of adopting a cooling system based on two-phase cooling in micro-channels using CO_2 and C_4F_{10} fluids respectively.

Starting with the first application of micro-channel cooling, this novel cooling system applied to particle detector at CERN is fully analysed in this thesis. The four micro-channels cooling applications currently developed at CERN, are analysed in different fields: the micro-fabrication of the cooling plates, the structural properties of silicon to understand the maximum pressure a device can hold, the thermal exchange and fluid circulation to evaluate the cooling performances and, in the last part, the mechanical integration of the silicon cooling plate inside the detector infrastructure.

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1 INTRODUCTION

1.1 CERN

CERN, the European Organization for Nuclear Research [1], is the world largest research centres in particle physics. It was founded in 1954 by 12 member states, in Geneva across the border between France and Switzerland. Nowadays it has 21 member states and scientists and physicists from more than 100 countries work there.
At CERN the fundamentals particles and the composition of the universe, are studied. The physics particles are studied with accelerators and detectors. The accelerators bring the particles to high energies and speeds and make them colliding between each other or with a fix target. The detectors analyse the results of these collisions.

In order to increase the speed and the energy of the particles, the accelerator is a circular tunnel in which the particles are bended and focused together in a small beam using magnets while they are accelerated with radiofrequency cavities. The accelerated particles are mainly protons, extracted from a simple bottle of hydrogen gas. Quadrupole magnets are used to focalize the particle beam, while dipole magnets are used to bend the protons and make them following a circular trajectory. The protons are accelerated by the radiofrequency cavities that are hollow bodies in which the beam is passing. Inside the cavity an electric field that changes polarity with a very high frequency, is created. When the positive sign is oriented towards the incoming protons, they are attracted inside the cavity while, when the electric field changes, the protons are pushed away from the cavity with higher speed. In order to reach speeds close to the speed of light and very high energies, CERN hosts an accelerator complex with a succession of one accelerator following the other. The last accelerator of the chain is the biggest and more powerful CERN accelerator, the Large Hadron Collider (LHC). In *Figure 1.1* is shown the CERN accelerator complex scheme.

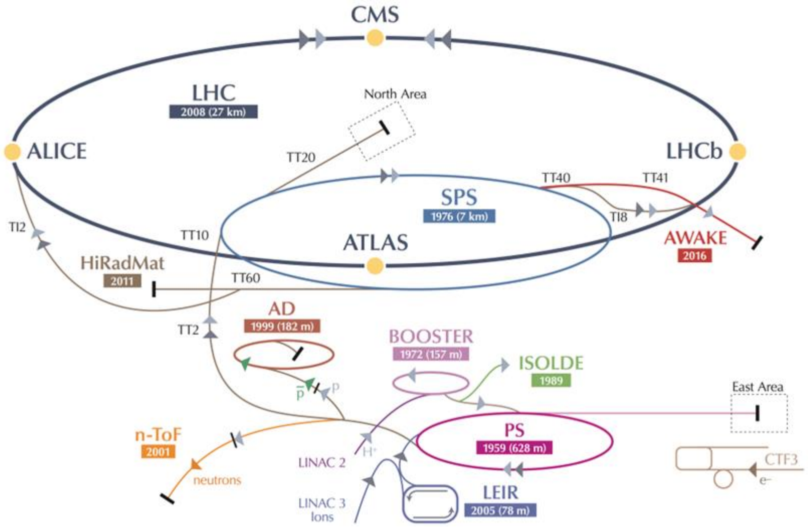


Figure 1.1: The CERN accelerator complex scheme.

The detectors instead are experiments placed at specific spots along the accelerators length that detect and analyse the results of the particle collisions. A detector usually tries to understand the nature of a particle by studying its momentum, energy, mass and charge. The structure of a detector is organized in layers of subdetectors each of them looking at a particular property of the particle or to a specific particle type.

A detector can be a ‘fix target experiment’ if it is analysing the result of a beam collision on a fix target. In this case the detector is built in a line-structure with the subdetectors placed one after the other along the particles trajectories. Contrary, the detector analysing the collision of two particle beams, is a ‘colliding beam experiment’ where the subdetectors are organized in a cylindrical structure around the collision point.

The four biggest colliding beam experiments at CERN are placed on the LHC ring and they analyse the results of the LHC colliding beams turning with a speed very close to the speed of light and with an energy of around 7 TeV. Between the four, ATLAS (A Toroidal LHC ApparatuS) and CMS (Compact Muon Solenoid) are general purpose detectors in charge of analysing all collisions of the two beams. The other two detectors, ALICE (A Large Ion Collider Experiment) and LHCb (LHC-beauty) are more specific detectors studying respectively heavy-ion collisions and CP violation in the interactions of b-hadrons.

The particle beam of the SPS (Super Proton Synchrotron) accelerator has an energy of 450 GeV. The SPS is suppling several experiments, among them fix target experiments are present like the NA62 (North Area 62) or the COMPASS (Common Muon and Proton Apparatus for Structure and Spectroscopy) experiments. In *Figure 1.2* two pictures of the CMS and ATLAS colliding beam particle detectors can be seen.

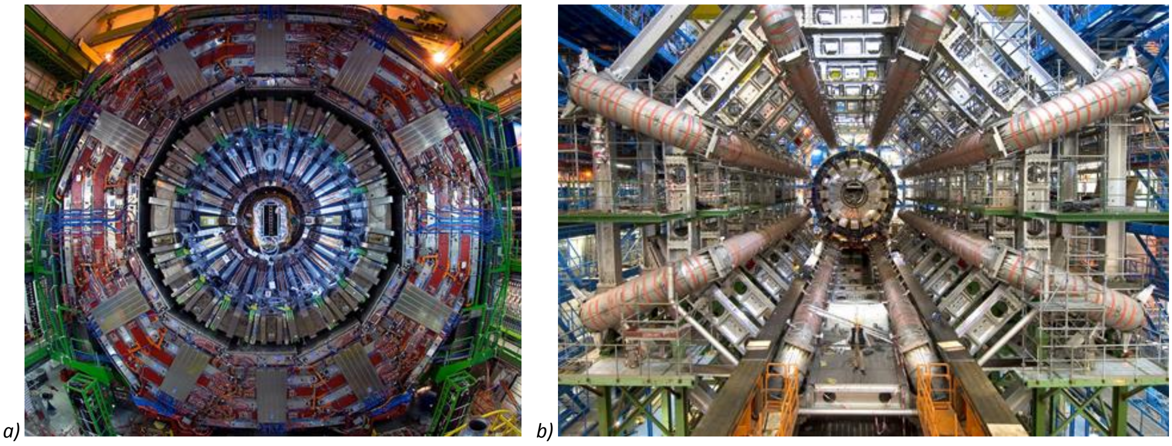


Figure 1.2: Front pictures of CMS (a) and ATLAS (b) experiments at CERN.

Normally particles, after collision, travel in straight lines, but the presence of a magnetic field inside the detector make them bending according to their charge. From the curvature of the particle path, the particle momentum can be calculated that is a clue on the particle identity.

Among all detectors, tracking detectors can identify the path of a particle, while calorimeters can stop, absorb and measure a particle energy. A big range of techniques is then used by the identification detectors to understand a particle identity.

1.2 SILICON TRACKING DETECTORS

A fundamental component of a particle detector is the tracking detector used to identify the path of a particle after the collisions with another particle or with the fix target. The particle path is a fundamental information to understand the particle identity by discovering the particle momentum. During the tracking process the particle trajectory should be disturbed as less as possible. This leads to a minimization of the physical material of the detector structure. In order to identify the particle position on one layer and then, layer after layer, the particle trajectory, a suitable substance has to be crossed by the particle and an electrical signal is left on each layer. The particle has enough energy to ionize the substance that is crossing and so the detector has to find the ionization trail left behind. A particle creates ionization by detaching electrons and ions in an atom or in a molecule of the crossed substance. The detached ions and electrons cause a current flow that can be measured.

According to the different substance that the particles have to traverse the most used tracking detectors are: gaseous detectors, scintillator detectors and solid state detectors.

In gaseous detectors, the used substance is a gas, in which the atoms or molecules are ionized by the passing particles. In scintillator detectors the material used is a scintillator that absorbs the particle energy and scintillates by re-emitting the absorbed energy in the form of light. The detector is then coupled to a scintillator counter like a photomultiplier tube, a photodiode or a silicon multiplier to identify the particle position. The solid state detectors [2], also called semiconductor detectors, use a solid crystal material as detecting medium. When a particle passes, a current pulse is created by the ionization thanks to the internal structure of the semiconductor. The current is measured and the particle position is known.

The detecting medium usually used in solid state detectors is a semiconductor material like silicon or germanium. The internal structure of a semiconductor is connected to two electrodes, so when an ionizing particles traverse the semiconductor, the amount of free electrons and holes (the electron-deficient sites) creates a current that starts flowing in the material. The current amount is directly proportional to the particle energy.

Silicon, as a detector material, can be fabricated in two forms: n-type, with a surplus of electrons in the structure, and p-type, with a deficit of electrons. The silicon *strip* detectors, in use at the LHC experiments, consist of n-type body material on which the back side has an aluminium layer while on the front side there are deposited strips of p-type material, in the middle of which a small strip of aluminium is deposited (*Figure 1.3 a*). The aluminium strips are separated from the p-type strips from a thin layer of insulator. By applying in the detector material an electric field between the p-type material and the back aluminium face, when a particle passes through it, it creates ionisation in the body material. The free electrons move to the positive back aluminium side, while the vacancies left by the electrons move towards the negative p-type strips. When the vacancies reach the p-type, they induce a measurable charge on the aluminium strips that are connected to the read-out channels. The electronics read-out components are placed at the end of the sensor on one side of the strips (*Figure 1.3 b*). By reading which aluminium strip collected the charge is possible to know where the particle passed. If a similar detection system is applied in the other direction is possible to see the x-y coordinates of where the particle passed.

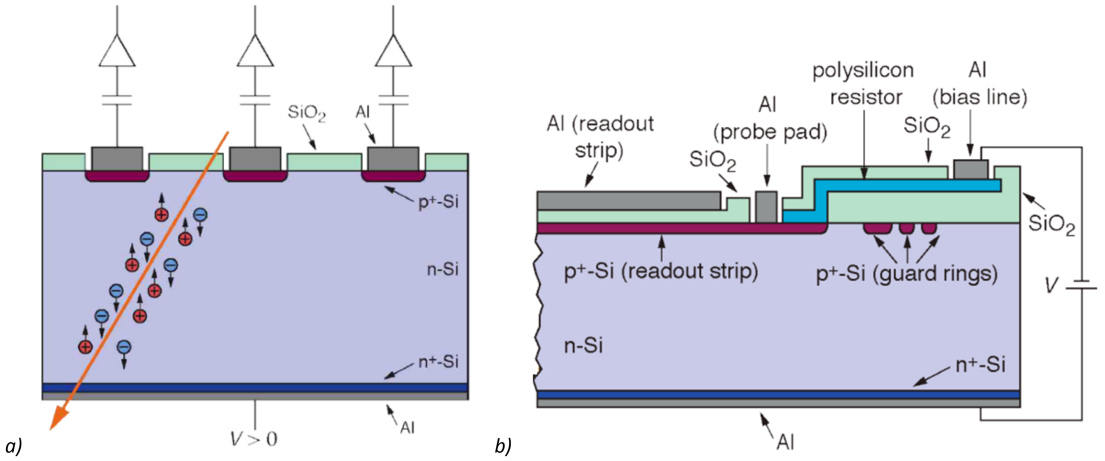


Figure 1.3: Internal structure of a strip detector: transversal section (a) and longitudinal section (b).

Another type of silicon detectors is the *pixel* detector. This time the p-type material is not present as a strip but as a small square, a pixel. The working principle is the same, but this time the electronics to collect the charge information is not placed at the end of the sensor but below. Each pixel is connected to the electronics through a metal ball, thanks to a process called bump-bonding, to the corresponding electronic path. In *Figure 1.4* is possible to see a cross section of a single pixel with the corresponding electronics. Thanks to its structure, the pixel detector is, in terms of precision and efficiency, better than strip detector. In the strip detectors the electrical signal is slower since it has to cross the complete detector before delivering the signal and furthermore the pixel structure allows a more precise resolution detecting more particles.

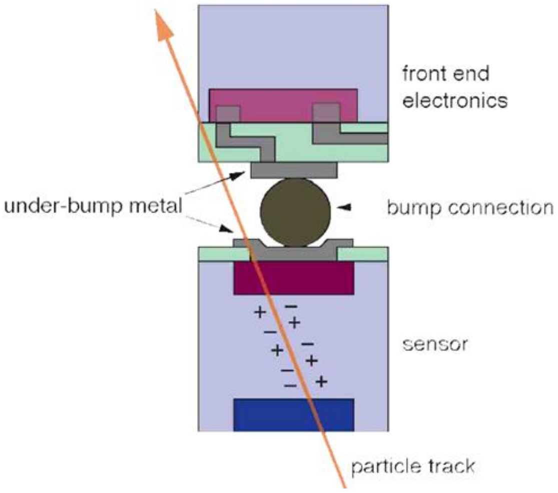


Figure 1.4: Internal cross section of a pixel detector (Ref. [4]).

The sensitivity of these detectors is increased at low temperature. With the increase of temperature the conductivity of the semiconductor material increases meaning that the number of electrons and holes increases for the temperature effect and not due to particle crossing. Also the leakage current (uncontrolled parasitic current flowing in the semiconductor not due to crossing particles) starts to increase with temperature and so the detector sensitivity decreases.

Particle detectors, and in particular silicon trackers, are exposed to high intensity particle beams and this can cause severe radiation damage that degrades the sensor performances. The intense particle beam can cause severe damages in the semiconductor detector structure and consequently in the detectors performances [3]. These damages are temperature dependent and with the increase of temperature the radiation damage is more and more important in the detector, and the detector work life is significantly reduced. For all these reasons it is necessary to keep the detector at low temperature integrating in the detector structure also a cooling system.

1.2.1 Cooling of Tracking Detectors

In addition to the reasons just explained for the silicon detectors, the tracker detectors need an efficient cooling system to remove the heat produced by the electronics from the small and compact mechanical volume typical of these structures [4]. From the physics point of view a good pixel detector has to be hermetic within the cover range, as transparent as possible to particle (the material of the detector must be minimized to not disturb the particle tracks) and stable to a few microns to obtain better results. Furthermore, as explained before, the detector must be operated at low temperatures (below 0 °C), therefore it has to be kept in dry atmosphere to avoid condensation. All these requirements are translated in a set of specifications for the mechanical structure of a detector. The detector structure has to be lightweight to minimize the material crossed by the particles, stiff to guarantee the stability of the detector, stable by using materials with the same coefficient of thermal expansion (CTE) to avoid thermal deformations and stresses, radiation hard and with an efficient cooling system. The cooling system should use a coolant fluid stable, non-flammable, non-toxic, electrical insulator.

A pixel detector is usually composed by the silicon sensor, sensitive to the particle passing, by the electronic chips, to collect and read the information of the sensor, and by the hybrid circuit, usually build on a printed circuit board (PCB), connected to the read-out chips housing the chip control module and providing the optical, data and power cables. All these components should be integrated together in the detector structure and they should be coupled to the cooling system.

The heat is produced mainly in the electronic read-out chips and it has to be transferred to the coolant fluid. One of the detector requirements in term of cooling system is a good temperature uniformity over the detection area to minimize any possible mechanical stress and to let all the detector pixels react at the same way. A low temperature difference between the cooling fluid and the silicon detector is also needed to avoid really low cooling temperatures that would require higher technical problems and costs.

The three main components that have to be assembled together by fulfilling all the detector requirements are the detector module, the mechanical support and the cooling channels.

When the new generation of pixel detectors was described in 2001 in the review of M. Olcese [5], the best mechanical structure of a detector and the most efficient cooling system, were presented for the CERN experiments ALICE, ATLAS and CMS and for the Fermilab BTeV pixel detector. The detector scheme is presented in *Figure 1.5* where three interfaces are visible. The three interfaces should minimize the CTE mismatches between the different materials and they should introduce a flexible joint between them. The first interface (A in the picture) is the interface between the detector module and the support structure; this is a critical point not only for the stability of the detector but also for the thermal coupling of the detector. Interface A should guarantee a good thermal contact while minimizing mechanical actions on the module due to CTE mismatches. Interface B is the coupling of the cooling tube to the support structure and it should also guarantee an efficient heat transfer. Interface C instead is just a structural interface between the local and the global detector support.

The first generation of cooling systems for the pixel detectors was using carbon fibre support structures glued to the modules, cooled with stainless steel or aluminium tubes connected to the module through thermal paste. The coolant fluids used were fluorocarbon fluids either in mono or two-phase flows.

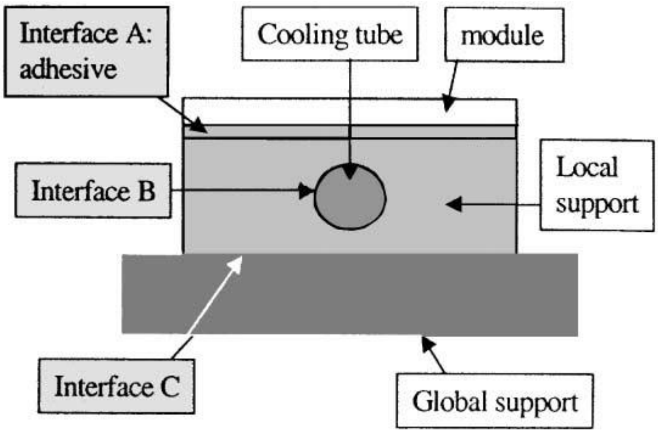


Figure 1.5: Thermal stability: relevant interfaces (Ref. [5]).

1.3 SILICON MICRO-CHANNEL COOLING OF TRACKING DETECTORS

In the last years, the PH-DT (Physics Department, Detector Technologies) group at CERN [6] proposed a new system for the thermal management of particle tracking detectors using a micro-channel fluidic circuit [7],[8]. The micro-channel circuit is embedded in a silicon wafer that is then glued through a thermal interface to the detector module. In the micro-channels a coolant fluid is circulate to dissipate the heat produced by the electronics.

The first idea of liquid cooling using micro-channel instead of air cooling was presented by Tuckerman and Pease in 1981 [9]. The advent of more and more high-speed, high-density and very large scale integrated circuits was demanding an effective and compact system for heat removal. The authors investigated a new cooling system for planar integrated circuit based on liquid cooling. The theory of a system based on convective heat transfer with a laminar flow in micro-channels was discussed in the paper. They then designed and tested a first prototype by etching micro-channels inside a silicon wafer and closing the channels by anodic bonding with a Pyrex wafer. They deposited on the silicon surface a thin layer of metal to simulate the heat produced by the integrated circuit and they circulated deionized water at 23 °C inside. The maximum allowed temperature increase for the integrated circuits was between 50 and 100 °C above the fluid inlet temperature. Power densities up to the values of 790 W/cm^2 were proven to be cooled by the 1 cm^2 area of the prototype.

Since this work, the micro-channel cooling of electronic chip both in single-phase and two-phase flow, has been extensively studied and several exhausting reviews have been recently published [10], [11], [12], [13], [14].

The first micro fabricated fluidic devices applied to particle physics were scintillation particle detectors based on microfluidics [15]. The scintillation detector consists in a single microfluidic channel filled with liquid scintillator. The channel is designed to reproduce an array of scintillating waveguides each coupled to a photodetector. When the particle is passing in a specific part of the channel, that waveguide scintillates and the photodetector is able to know the exact particle position. A particle detector prototype was built using an SU-8 resin and tested with electrons from a radioactive source.

After this first application of microfluidics in particle detectors, the micro-channels were evaluated as an alternative technique for cooling the electronics modules of tracking detectors.

The micro-channel cooling system presents a very efficient solution for the cooling of particle detectors. In

Figure 1.6 it is possible to see a comparison between the standard cooling systems adopted for the pixel detectors and the novel micro-channel based system.

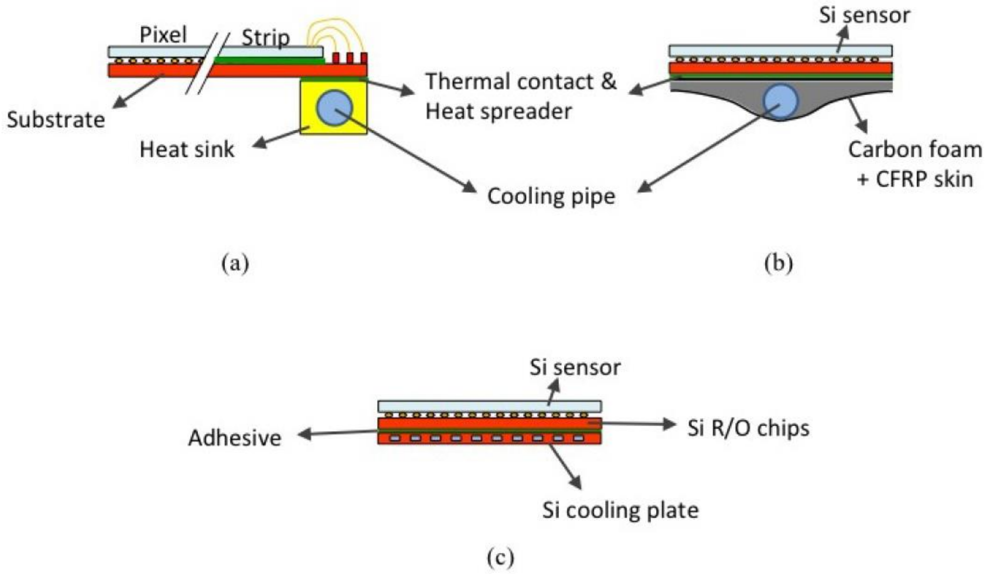


Figure 1.6: Cooling configurations for tracking detectors (Ref. [7]).

The standard thermal management techniques (*Figure 1.6 a,b*), as previously discussed, present a cooling system based on a high thermal conductivity structure with a cooling pipe embedded inside that removes the heat produced by the detector module.

The first solution (*Figure 1.6 a*) is referring to a standard cooling scheme adopted in the first generation of silicon trackers at LHC, both for strip and pixel detectors [16]. The sensor modules are connected with a thermal interface to a heat sink in a lateral position. For the CMS tracker, for instance, the cooling tube is a metal tube circulating a fluorocarbon fluid, C_6F_{14}. The tube is bonded to two CFRP (Carbon Fibre Reinforced Polymers) blades that are holding the silicon modules. The internal space between the two blades is filled with a foamed material to guaranty rigidity and the thermal conductivity. In this solution the lateral cooling pipe brings important mechanical stresses due to the non-uniform thermal gradient across the module. Furthermore the small thermal contact area between the module and the heat sink and the long chain of thermal resistances, increase the thermal gradient across the module, inducing mechanical stresses in the structure and increasing the TFoM. The Thermal Figure of Merit (TFoM) is defined as the ratio between the temperature difference between the sensor and the fluid, over the power density. The TFoM is an indicator of the efficiency of a thermal management system because it defines, for a given power density, how cold the cooling fluid has to be, in order to keep the sensor to the target temperature.

In order to improve the thermal uniformity over the module area, in the second solution is possible to see how the cooling pipes is placed at the centre of the structure to allow a more uniform thermal flux. The solution presented in *Figure 1.6 b* was used for the ATLAS IBL (Insertable B-Layer) pixel detector in the phase I upgrade [17]. The IBL is the innermost part of the ATLAS detector, and it is composed by fourteen local supports for the silicon modules arranged cylindrically around the beam line called staves. The staves are tilted in order to have an overlap between them and cover the all area. The stave structure is built in carbon foam material that provides a thermal path for the heat generated in the sensor and in the electronics. The titanium cooling pipe is strongly bonded to the structure with a thermally conductive epoxy resin. The coolant fluid used is CO_2. The rigidity of the stave is provided by a CFRP skin, the Omega, that surrounds the carbon foam. The CTE difference between all materials involved in the stave structure is considerable and it induces a non-negligible mechanical deformation in the stave. The largest deformation occurs when the stave is cooled while the detector modules are not powered, and the corresponding bow in the stave reaches a maximum of 0.15 mm. These problems were taken into account during the detector design and construction and the minimum gap between one stave and the other was 1 mm in order to leave enough space to avoid interferences and clashes.

An innovative solution, shown in *Figure 1.6 c,* takes advantage of the high cooling power of micro-channels to improve all aspects of the thermal management of the pixel detectors. The micro-channel circuit is embedded in a silicon wafer and it is then glued to the detector module. All the material involved in the structure is silicon; the CTE of the cooling part is exactly the same as the one of the detector modules and so mechanical stresses due to CTE mismatches are avoided. The thermal gradient across the detector is uniform since the channels are designed to be equally distributed along the module area. The thermal flux is flowing in the vertical direction from the electronics and sensor, to the channels. The interface between the cooling pipe and the support structure is eliminated since the silicon device acts as support structure and as cooling pipe at the same time. The use of micro-fabrication techniques allows the production of very thin cooling devices, thus minimizing the amount of material to be crossed by the particles.

One crucial point in the three configuration shown in *Figure 1.6,* is the thermal interface between the silicon modules and the detector structure. This thin layer should provide a perfect and uniform thermal contact without air bubbles or defects, while being also radiation resistant. It should be as light as possible to minimize the material crossed by the particles and, for the solutions of *Figure 1.6 a,b,* it should also be enough flexible to absorb the CTE mismatches in the whole structure. Several studies will be presented in *Chapter 5* to select the best suitable adhesive.

The critical point of the correct thermal interface between the cooling structure and the detector modules can be avoided in the future thanks to the silicon micro-channels. The micro-channels are etched in a silicon wafer as well as the detector modules, in a future it can be imagined to etch the channels on the backside of the same wafer of the detector. In this way a monolithic structure could be obtained, avoiding the thermal interface between the two parts.

A silicon micro-channel cooling device is fabricated using standard micro-fabrication techniques inside cleanrooms. The device fabrication starts with the photolithography mask fabrication to be able to transfer, on the silicon wafer surface, the design of the cooling circuit. The micro-channels are plasma etched on the silicon surface using a resin mask. The micro-channels are then sealed by a cover wafer that can be of Pyrex material with an anodic bonding technique, or again in silicon using a direct bonding process. Usually silicon-Pyrex devices are used in a preliminary phase due to the simpler anodic bonding technique compared to the direct bonding process. Pyrex, thanks to its transparency, is also used for visualizing the flow in the channels. In a second time, for final prototyping and for the insertion of the cooling system in the detector assembly, only silico-silicon devices are used. The final step of the fabrication is the etching of the openings for the inlet and the outlet of the fluid. Depending on the detector structure a very final step of localized thinning can be applied to minimize the material in the detecting area. In *Figure 1.7* is possible to see a simple design example for a silicon-Pyrex wafer fabrication. More details on the micro-fabrication will follow in *Chapter 2*.

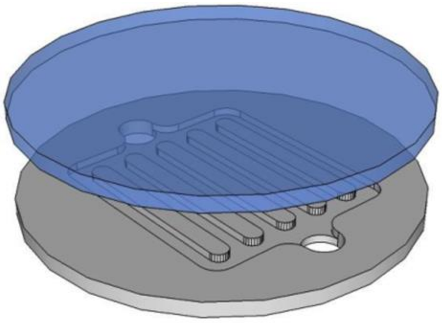


Figure 1.7: Micro-channel simple design for a silicon-Pyrex device.

1.4 SILICON MICRO-CHANNEL COOLING AT CERN

The application of micro-channel cooling systems to particle physics is gaining more and more success. The first micro-channels cooling system was installed in 2014 for the thermal management of the NA62 GTK (GigaTracKer) stations at CERN [18]. The three GTK stations are cooled by a micro-channel silicon device circulating C_6F_{14}, in liquid flow. The LHCb VELO (Vertex Locator) detector has adopted a micro-channels based cooling system for its upgrade in 2018 [19]. The cooling fluid in the VELO detector will be CO_2 circulating in two-phase flow. A micro-channel cooling system is the backup solution for the ALICE ITS (Inner Tracking System) upgrade [20]. The silicon micro-channels circulate in this case C_4F_{10}, in evaporative flow. Very preliminary studies are also going on for the cooling of an ATLAS FEI4 chip, cooled with CO_2 evaporative flow, for a future integration in the upgrade of the ATLAS pixel detector.

1.4.1 NA62 GTK

The NA62 GTK detector was the pioneer in evaluating micro-channel cooling for the thermal management of its three stations. The NA62 detector [21] is a fix target detector of the SPS accelerator, focused on the rare decay of charged kaons. It started physics data taking in 2015. The three GTK stations provide precise measurement of momentum, time and angle of the incoming particle beam. The detector layout consists in a silicon sensor 63x29 mm bump-bonded to ten 12x20 mm read-out chips. The power dissipation foreseen is 2.5 W/cm^2 for the analog part of the chip and 0.4 W/cm^2 for the central digital part, for a total maximum power of 48 W per station. The detector requirements are to keep the sensor surface at a temperature below -10°C and a maximum temperature gradient of 5°C along the sensor area.

The micro-channel device foreseen for this application is a 480 µm thick silicon wafer with a localised thinning in the central part, in order to minimize the material crossed by the particles in the sensor area. In the central part the micro-channels device is 150 µm thick. The detector assembly of the silicon sensor bump-bonded to the ten read-out chips is glued onto the thinned part of the micro-channel plate with a thermal interface. The external parts of the chips are then wire-bonded to the PCB for data transfer. A cross section scheme is shown in *Figure 1.8.*

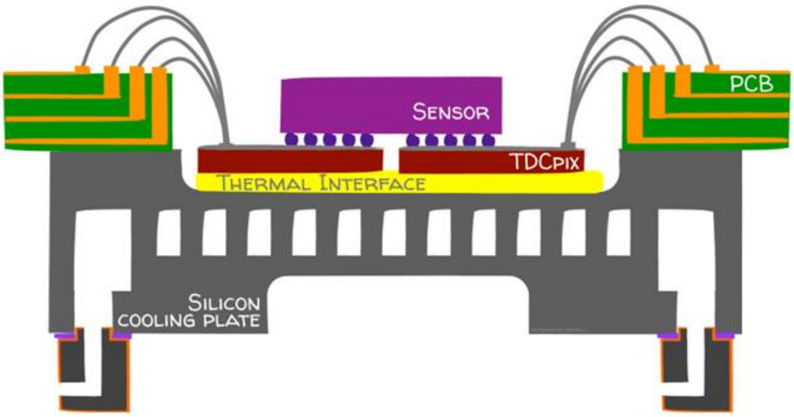


Figure 1.8: Cross section concept of the micro-channel cooling for the NA62 experiment.

The micro-channel design consist in two parallel circuits for the C_6F_{14} liquid flow. The 154 micro-channels of the device are 200 µm wide and 70 µm deep, separated by 200 µm walls. The two fluidic circuits start with an inlet hole and a distribution manifold from where the fluid is distributed in the channels; the circuits end with a recollection manifold where the fluid from the channels is collected before leaving the device from the outlet hole. In *Figure 1.9* it is possible to see a picture of a micro-channel device designed for NA62 with the transparent front Pyrex wafer.

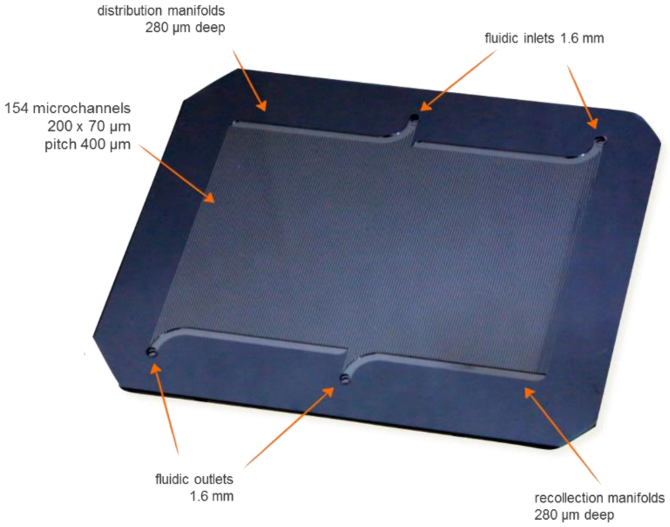


Figure 1.9: Micro-channel design for the NA62 experiment.

Test devices have been fabricated in the CMi (Center of Micronanotechnology) EPFL (École Polytechnique Fédérale de Lausanne) class 100 cleanroom [22]. After thermal, mechanical and structural tests conducted at CERN on test devices fabricated in silicon and Pyrex, the design is validated. The micro-cooling devices installed in the experiment since 2014 are full silicon devices fabricated by the Leti 3S [23] at CEA-Leti in Grenoble [24].

1.4.2 Proposal for ALICE ITS Upgrade

During the long LHC shutdown scheduled in 2018, also the ITS detector of the ALICE experiment is planned to be upgraded [25]. The existing detector will be replaced by seven new layers of pixel

detectors. The ITS detector is responsible of the high precision tracking and momentum identification of the incoming particles. For this reason the material minimization is quite crucial in this case. The new pixel detectors are expected to dissipate between 0.1 and 0.3 W/cm^2. The maximum allowed temperature on the detector surface is 30°C and the minimum is 15°C, to avoid condensation on the electronics surface. The allowed maximum temperature difference over the chip area is 5°C.
Micro-channels cooling is studied as backup cooling option for the ITS upgrade. In order to minimize the material of the cooling system a frame design is investigated: the micro-channels are present only at the edges of the chip to avoid additional material in the central part. In *Figure 1.10* it is possible to see a picture of a first prototype of a silicon frame with the Pyrex cover wafer.

Figure 1.10: Micro-channel frame design for the ALICE ITS upgrade (Ref. [20]).

While for NA62 a liquid flow is used, since the heat transfer coefficient of C_6F_{14} in single phase is fulfilling the detector requirements, for the ALICE ITS studies currently on-going at CERN, an evaporative flow has been chosen. The fluid is entering the micro-channel device in sub-cooled liquid state. At the inlet of the circuit the channels present a much narrower cross section than in the entire circuit. The length of these narrow capillary parts is dimensioned to induce the desired pressure drop and to bring the fluid in the saturation conditions at the end of the capillaries. The sudden increase of the channels width favours the onset of boiling by flash evaporation. In the specific case of ALICE ITS, due to the reduced pressure budget provided by the C_4F_{10} saturation properties at room temperature, a large distribution manifolds acts as a plenum and, in order to stabilize the flow when it enters in the micro-channels and to avoid back flow, short inlet restrictions are foreseen. In *Figure 11* the inlet restrictions for the ALICE ITS micro-channel device are shown.

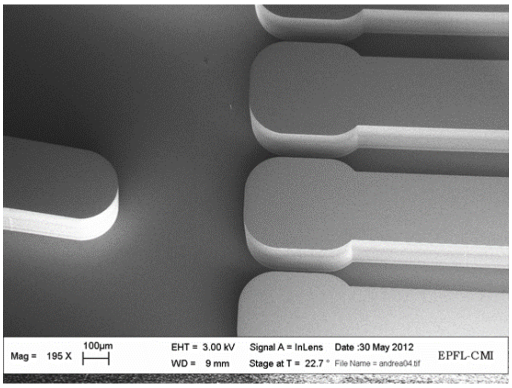


Figure 1.11: SEM image of the ALICE inlet restrictions.

The ITS detector staves are 270 mm long, making it impossible to have a single micro-channel cooling device that covers the entire area. Standard wafer sizes are too small to cover in a single piece this length. For this reason it is foreseen to use several micro-channels devices in chain one after the other.

It is so necessary to study a fluidic interconnection between one wafer and the other. The ITS geometry requires minimal mechanical structure and out-of-plane solutions should be avoided. The first tested prototype was a “bridge” connection where a small piece of silicon with a small microchannel is connecting one frame to the following one [26]. Further studies are on-going to find the best solution.

1.4.3 LHCb VELO Upgrade

The VELO tracker is the closest LHCb detector to the interaction point, it was a pioneer in the use of the evaporative CO_2 cooling since its first installation in 2007 [27]. The VELO experiment will be upgraded in 2018 to run at higher luminosities and with higher speeds. The upgraded detector will work also in higher radiation environment and it will see the silicon strip technology substituted by silicon pixels. This, bringing much higher power distributed on the whole sensor surface, requires innovative thermal management techniques to keep the silicon sensor temperature below -20°C. In 2013 silicon micro-channels cooling was selected as the basic solution for the upgrade. The new VELO detector will be composed of 26 stations of two silicon micro-channel modules facing each other around the beam. The layout of one station is available in *Figure 1.12*. On each micro-channel module two sensor and chip assemblies, will be glued, one on the front side and one on the back side. A silicon pixel sensor (orange in *Figure 1.12*) will be bump-bonded to three ASICs (Application Specific Integrated Circuit) chips (yellow in *Figure 1.12*). The expected power densities are around 1.5 W/cm^2 that means about 36 W per module.

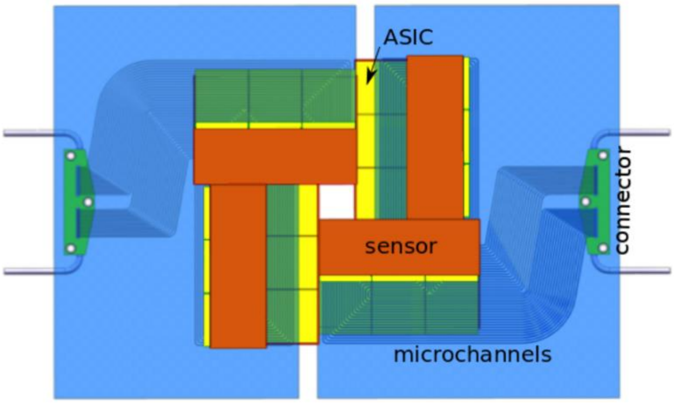


Figure 1.12: Micro-channel cooling station or the LHCb VELO upgrade (Ref. [28]).

The micro-channel design will consist of a 400 µm thick silicon device with 19 parallel micro-channels, 200 µm wide and 120 µm deep, separated by walls of 500 µm. Each channel has a fluidic inlet and a fluidic outlet and the fluid distribution occurs inside a specific connector soldered on the silicon surface. Taking advantage from the high pressure of CO_2 flow, subcooled liquid is distributed in each micro-channel from the fluidic connector. The liquid enters a long capillary (60 µm wide and 60 µm deep), where it is brought in saturation conditions at the entrance of the micro-channels. A SEM image of the change of size between capillaries and micro-channels is shown in *Figure 1.13 a*. The final dimension of a micro-channel module will be 80x104 mm, fabricated starting from a 6 inches wafer. In order to validate the design with thermal and mechanical tests, a smaller prototype was built inside the CMi EPFL cleanroom with a silicon 4 inches wafer bonded to a Pyrex 2 mm thick wafer. A picture of the fabricated test device can be seen in *Figure 1.13 b*.

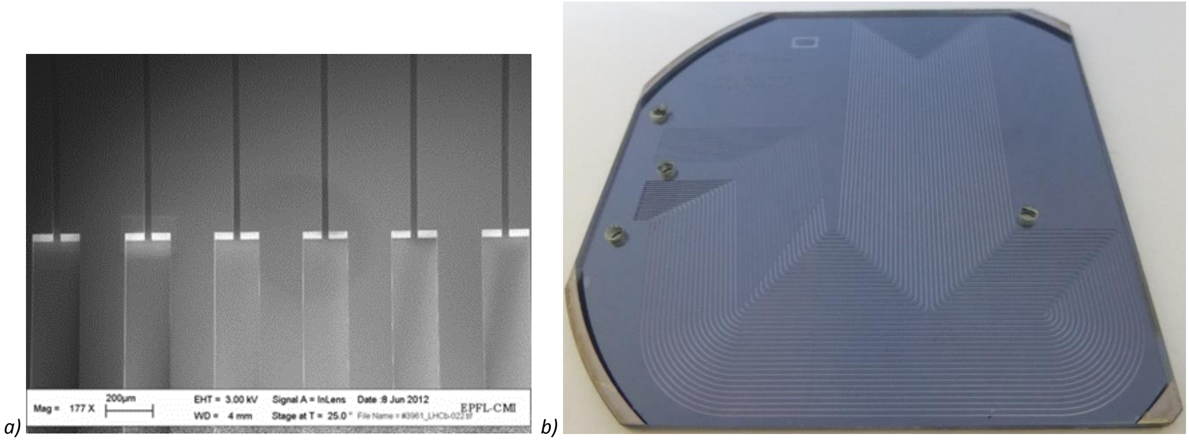


Figure 1.13: SEM picture of restrictions (a) and micro-channel test prototype for the VELO cooling (b).

1.4.4 Studies on ATLAS FEI4 cooling

Preliminary studies are also done with micro-channel cooling for the cooling of an FEI4 chip of the ATLAS IBL experiment. The chip is 20x20 mm and it is supposed to dissipate a power density of 0.376 W/cm^2, so a total power in the chip of 1.5 W. The requirement is to keep the detector surface at -15°C to minimize radiation damages on the chip structure. The proposed micro-channel solution is to use a silicon micro-channel device circulating CO_2 in evaporative flow. The first prototype of micro-channels device is 760 µm thick with a total area of 20x40 mm. The design is based on the LHCb solution, with 35 parallel micro-channels 50 µm wide and 190 µm deep. From the inlet hole, the fluid is distributed into the 10 µm wide capillaries, and then is evaporating in the channels under the chip area. The outlet manifold is collecting the fluid from the channels and it is filled with structural pillars to avoid a mechanical failure of the region due to high internal pressure. In *Figure 1.14* is possible to see a design of the micro-channels with the FEI4 footprint.

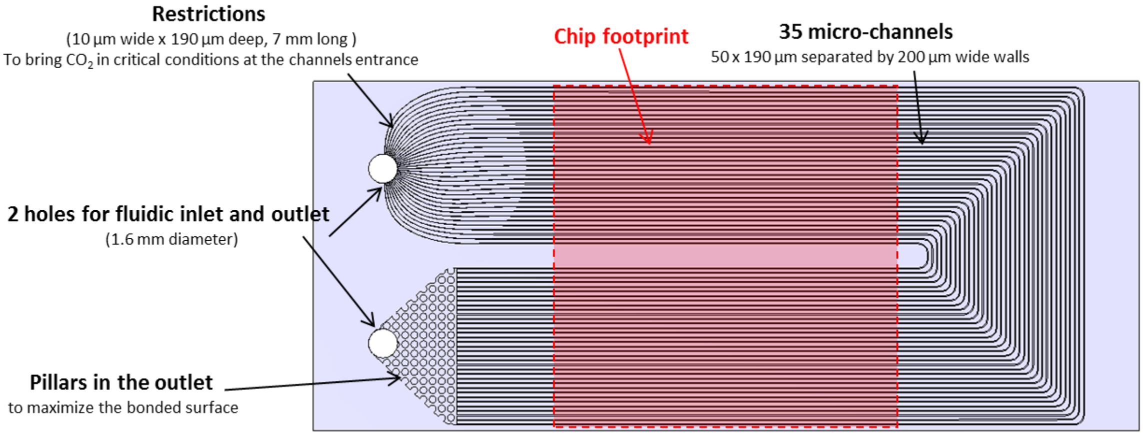


Figure 1.14: Micro-channel design for the ATLAS FEI4 chip cooling.

2 MICRO-FABRICATION OF SILICON MICRO-CHANNEL COOLING SYSTEMS

2.1 WHY SILICON?

As discussed in the first chapter micro-channel cooling is gaining lot of attention for the detector cooling of silicon trackers. The high thermal efficiency of micro-channels is strongly pushing in this direction. Furthermore, compared to the standard cooling approaches, the micro-channels give the possibility to spread the local heat sink in a planar array of channels uniformly distributed under the sensor area, in direct contact with the heat source. Different micro-channel cooling techniques are being studied in the last years for the cooling of particle detectors.

One of the alternatives that are being explored for the cooling of the ALICE ITS upgrade is a polyimide micro-channels cooling system [29]. The polyimide micro-channel structure is a system of parallel micro-channels with rectangular cross-section manufactured by deposition of epoxy walls on a polyimide substrate, then glued to the silicon detector (*Figure 2.1*). The heat flux generated by the electronics is transferred firstly to the polyimide substrate and then is dissipated by the cooling fluid flowing inside. Two studies were conducted using single-phase demineralized water and single phase C_6F_{14} fluid. Indeed the thin polyimide covers have a very poor structural properties and they cannot stand internal pressure in the channels: the system is only suited for liquid circulation in sub-atmospheric pressure. The foreseen channels were 16 per stave with a cross section of 200x800 µm. Successful thermal tests were conducted using a kapton heater with a heat power production between 0.1 and 0.5 W/cm^2 as foreseen for the ALICE ITS detector [30].

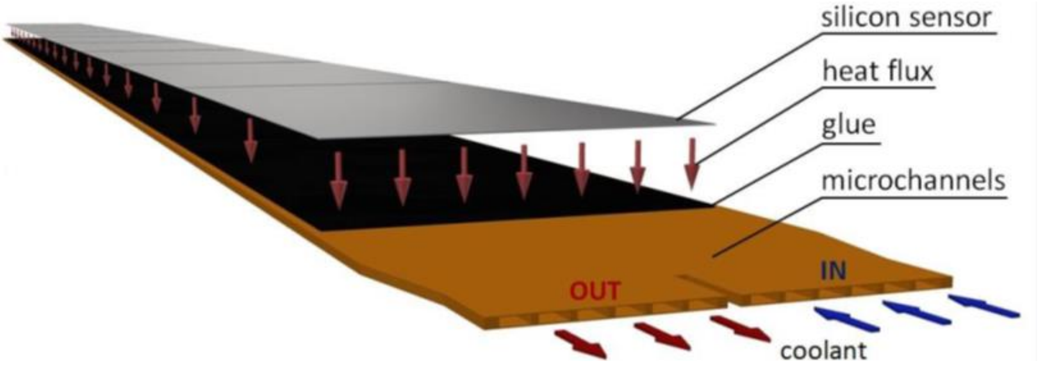


Figure 2.1: Sketch of the polyimide cooling system (Ref. [29]).

Another relevant work about micro-channel technology is the study by F. Bosi and others [31], for the cooling of the SuperB Layer0 Vertex Detector. The proposed solution is an array of PEEK capillaries with 50 µm thick walls, encapsulated in a protruded carbon fiber. A single unit is a 700x700 µm square cross-section micro-tube with at the centre the PEEK pipe and the carbon fiber all around (*Figure 2.2 a*). The single units are glued together with epoxy glue Araldite 2011 (*Figure 2.2 b*). The micro-channels are 130mm long as the total length of the detector. The prototype was tested using as coolant a mixture of water and ethylene glycol.

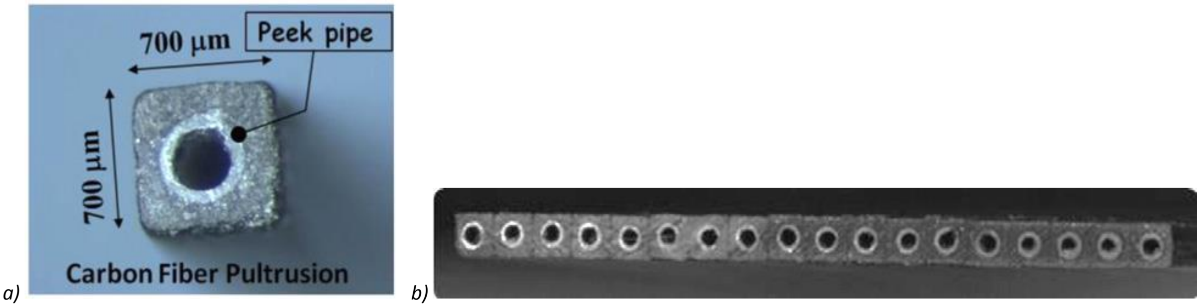


Figure 2.2: Single unit cross section (a) and full module support cross section (b) (Ref. [31]).

All these methods of micro-channel cooling benefits from the heat spread aspect and from the short thermal path between the heat sink and the heat source. Unfortunately for both polyimide and carbon fiber, the CTE values are not matching with the one of silicon, and possible stresses due to thermal gradient can occur on the detector modules.

W. E. Cooper in his work [32], lists the most used materials in tracker detectors structures. He is dividing the materials into three groups according to their CTE values or their FOM (Figure Of Merit). One of the most fundamental parameters in thermal exchange, is the thermal impedance, defined as the ratio of the temperature gradient to the heat transferred. The FOM is the inverse of the thermal impedance. According to Cooper's classification, inside the group of the standard material for silicon structures (together with carbon-carbon composites, glass epoxy composites, aluminium nitride, …), also silicon is present. The thermal conductivity of silicon is good compared to the other materials, and moreover the CTE is the same of the one of the sensor module. The possible use of silicon as a structural element should be taken in account.

Following this idea, the BELLE II detector upgrade is designed using the silicon material of the sensor as structural material [33]. The BELLE II detector is built using DEPFET (Depleted-Field Effect Transistor) modules. The DEPFET technology allows to realize very thin sensors, even to thicknesses down to 50 µm. In this concept the read-out electronics is located outside the sensitive area, which contributes to the minimization of the material to be crossed by the particles. The sensor itself produce very little power in such a way that gas injection cooling is sufficient to dissipate the heat there generated. The detector module is so fabricated starting from the same substrate with a localised thinning in the central part with the sensor and with an outer thick frame for the electronics. The thicker part is in contact with a cooling block in non-magnetic metal material cooled down with evaporative CO_2 flow at around -30 °C.

The method proposed in the PH-DT group of using silicon micro-channels for the cooling of particle detector, seems to gather all the advantages of the previous technologies reported. The micro-channels guarantee the spread cooling system below the sensor area and the small thermal path between the heat sink and the heat source. Furthermore the silicon itself is used as a structural material and so the CTE mismatch is not affecting the structure.

Another fundamental reason to choose silicon as the material of the micro-channels, is related to the fabrication method. In the last years MEMS (MicroElectroMechanical Systems) fabrication techniques for silicon electronic devices were largely developed: standard and well controlled processes can be used to fabricate micro-channels devices in silicon.

Based on the projects currently under study at CERN for the cooling of tracker detectors, also the DEPFET collaboration is investigating the possibility to use silicon micro-channel cooling for the new ILC (International Linear Collider) detectors [34]. Contrary to the Belle II detector, where the support and cooling structure can be placed outside the sensitive area, for the future ILC detector the detector material has to be kept at minimum in the whole volume. Very preliminary studies are carried out on the possibility of inserting the micro-channels in the thick frame of the DEPFET detector and to circulate a forced gas flow. In *Figure 2.3* is possible to see a tentative layout of the micro-channel cooling part in the thick frame of the detector.

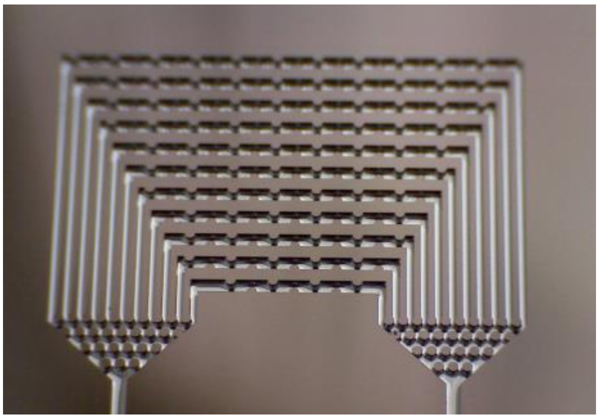


Figure 2.3: Tentative micro-channel circuit design for the gas cooling of the DEPFET new ILC detectors (Ref. [34]).

2.2 MICRO-CHANNELS FABRICATION

As previously anticipated, among the benefits of choosing a silicon micro-channel cooling system, there is the controlled and highly reproducible fabrication done using the standard and well known MEMS processes inside cleanrooms.

For the studied micro-cooling projects at CERN, after the channels dimensioning, the micro-channel designs for the different experiments have been prototyped and tested before the design validation. The test devices production takes place in the class 100 cleanroom of the CMi (Center of Micronanotechnology) at EPFL (École Polytechnique Fédérale de Lausanne) [22], while the thermodynamic tests are done at CERN inside the PH-DT laboratory. In a second time, the micro-channel devices for the final application in the experiments, are purchased from high qualified micro-technology companies that develop a series production of the devices.

Thanks to a collaboration between the PH-DT group at CERN and the CMi centre in Lausanne, it is possible for the PH-DT personnel, after a training period, to have access to the CMi cleanroom and to perform the micro-fabrication of the test devices. The CMi is a university cleanroom where typical micro-fabrication processes are taking place in a temperature and humidity controlled environment, principally on silicon wafers but also on other substrates. In order to avoid the contamination of the high sensitive processes done in the cleanroom, there is a driven laminar air flow inside the room, flowing from the ceiling to the floor, to evacuate possible pollution particles through the holes present in the floor. Furthermore the cleanroom users have to wear a cleanroom suit to minimize the pollution of the working environment.

The micro-fabrication of the test devices starts with the process flow definition in order to decide all the working steps with the correct parameters necessary to reach the targeted device. Often the micro-fabrication processes done in the CMi cleanroom for the test prototypes, and the processes done in the external companies for the final realisation of the micro-channel devices, present some differences due to the complexity of the processes.

In *Figure 2.4* is possible to see, in a simplified form, a complete standard process flow for a micro-cooling device fabrication. The process starts from a silicon wafer. The channel design is transferred on a chromium/glass photolithography mask (*Figure 2.4 1*). After a photolithography process (*Figure 2.4 2*), the micro-channel circuit is etched on the wafer surface with a DRIE (Deep Reactive Ion Etching) etching process (*Figure 2.4 3*). The wafer is well cleaned from all the impurities and the cover wafer is bonded on top of the etched one. The cover wafer can be a Pyrex wafer or another silicon wafer. The bonding process is an anodic bonding, if the cover wafer is Pyrex, otherwise it is a silicon-silicon direct bonding process (*Figure 2.4 4*). A wafer thinning, localized or applied to the whole wafer surface, is then performed on the wafer to minimize the amount of material to be crossed by the particles (*Figure 2.4 5*). The fluidic inlets and outlets are then etched in the cover wafer or in the bottom wafer (*Figure 2.4 6*). If required from the device application, a metal deposition is done at this point on the wafer surface for the soldering of the fluidic connectors or for temperature measurements (*Figure 2.4 7*). The last step of the process flow is to dice the wafer to have the single devices ready for testing (*Figure 2.4 8*).

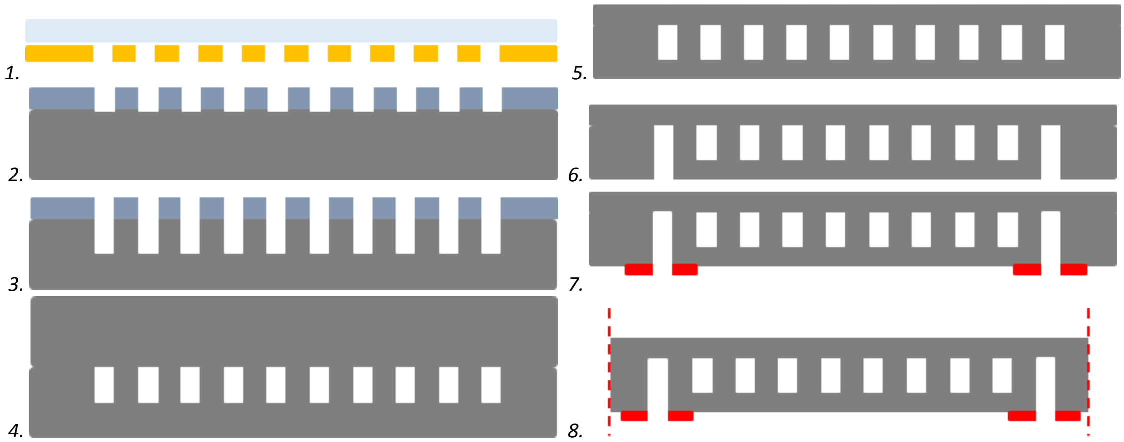


Figure 2.4: Simplified process flow for the micro-channels fabrication in cleanrooms.

In the next section each single step of the process flow is analysed and explained form the point of view of the micro-channel device fabrication. The description is done showing the problems found during the fabrication and underlining the differences between the production in the CMi cleanroom and in the external companies.

2.2.1 Silicon

The first time that silicon was considered suitable for a microfabrication process was with the first silicon transistor in 1952 [35]. But it became even more interesting with the discovery of the good insulation properties of silicon dioxide. Silicon is processed in the micro-fabrication machines starting from circular thin substrates of monocrystalline silicon called *wafers*. The silicon-wafer manufacturing is a multistep process, usually based on the so called Czochralski process that starts with the sand purification and ends with the wafer inspection. The silica sand, with the correct amount of dopants, is heated up in a quartz crucible under vacuum, to 1420 °C to melt the silicon. A single-crystalline seed of known orientation is dipped in the bath. The seed is gently pulled outside the bath and the silicon solidify around the seed following its orientation. A small neck is created at the beginning of the ingot for the high temperature difference and then the resulting ingot increases diameter with the decreasing of the pulling rate. During the process the crucible and the ingot are rotated in different directions (*Figure 2.5*). Since the silicon ingot is not mechanically strong enough at 1400°C, a graphite susceptor is providing the mechanical strength to the silicon.

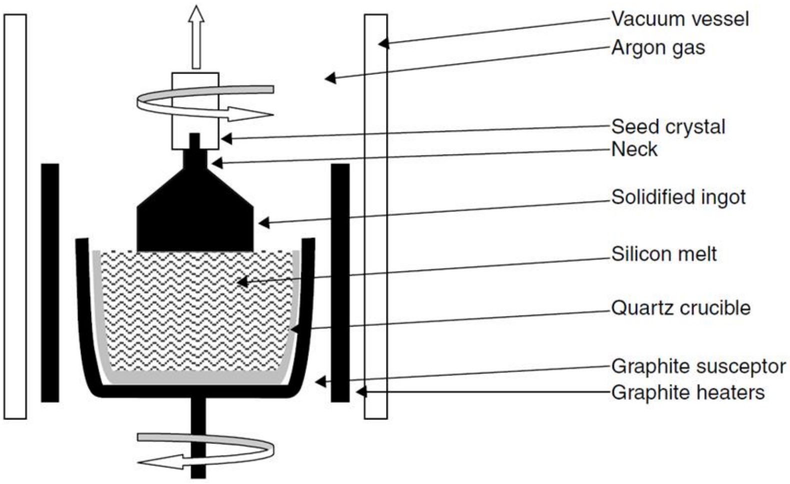


Figure 2.5: Czochralski process to create wafers from a silica crucible (Ref [35]).

Silicon has a cubic diamond lattice structure (*Figure 2.6 a*). Miller indices define the planes of the crystal (*Figure 2.6 b)*. The indices are the reciprocals of the intersections of the plane with the three axis, for example the front plane in *Figure 2.6 b* is the (1 0 0).

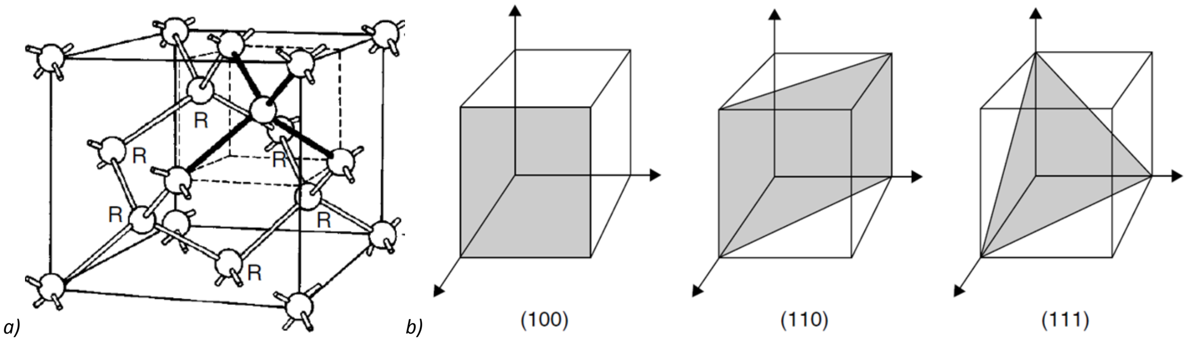


Figure 2.6: Silicon lattice structure (a) and important silicon planes with Miller indices (Ref [35]).

The silicon ingots are then transformed into silicon wafers trough a long thermal, mechanical and chemical process. A flat part is cut from the cylindrical shape of the ingot to indicate the crystal plane orientation of the resulting wafers. At the end the wafer is sawed in slices. Each slice is thinned and polished with mechanical and chemical processes to the desired thickness and roughness. The silicon wafers can be of different sizes, from less than 100 mm of diameter to more than 300 mm.
For the micro-fabrication inside the CMi the standard wafer size is 4 inches wafers while in the external companies that collaborated with PH-DT the fabrication is done typically on 6 or 8 inches wafers.

2.2.2 Patterning – Photolithography

Lithography is the technique to transfer copies of a master pattern on a solid surface like a silicon wafers. Photolithography is the lithography done using the UV light to transfer the pattern from a masks onto the wafer surface.

The first step is to realize the photolithography mask used as the master to reproduce the design on all the wafers. The most commonly used photolithography masks are made of chromium coated glass. The masks are prepared and the chromium is etched in order to obtain the desired pattern design. The scheme of the photolithography mask production done inside the CMi cleanroom is shown in *Figure 2.7*. The glass mask (light blue in *Figure 2.7 1*) is chromium coated on one side (orange in *Figure 2.7 1*) and a resist layer is deposited on top of the chromium (dark blue in *Figure 2.7 1*). The resist is exposed to a laser beam that scans the whole mask surface and illuminates the parts that have to be etched (*Figure 2.7 2*). The third step is to start developing the resist where it has been illuminated by the laser (*Figure 2.7 3*), and after the complete development the result is like in *Figure 2.7 4*. The wafer is now dipped in an etching bath to remove the chromium parts to be etched (*Figure 2.7 5*). Finally the resist on the mask is removed and the photolithography mask is ready to be used (*Figure 2.7 6*).

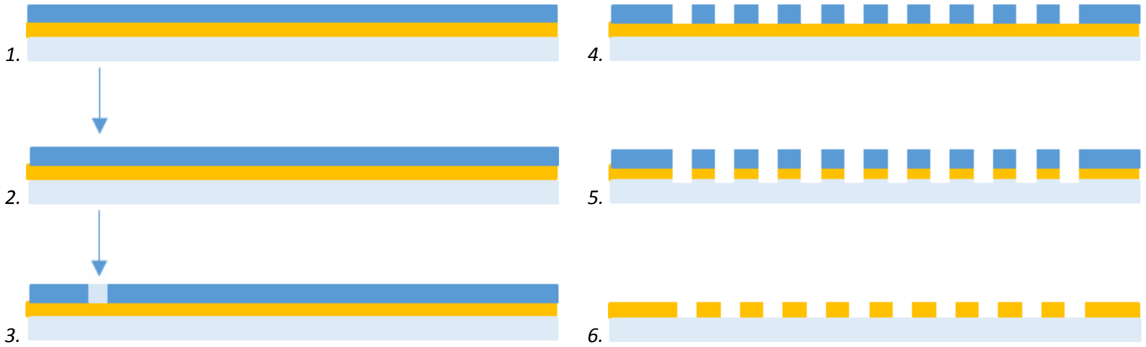


Figure 2.7: Mask fabrication process flow.

The photolithography process to transfer the channels design on the wafer surface is very similar to the one used to fabricate the mask. The wafer is coated with a photoresist and then the resist is exposed to UV light using the photomask just fabricated. In *Figure 2.8* all the steps of the process are shown. The standard resists used in micro-fabrication are organic polymers sensitive to UV light. One of the most common processes to deposit the resist on the wafer surface, is by spin-coating. The liquid resist is deposited in the centre of the wafer and after a while the wafer is accelerated to high rotational speed to let the resist spread on the wafer surface (*Figure 2.8 1*). The amount of resist to deposit is a critical parameter for the good outcome of the process. Too less resist may leave uncovered areas, while too much resist results in ridges, wrinkles and defects on the wafer surface. The resist is sensitive to UV light and so the next step is to illuminate the wafer surface through the photolithography mask to let the light passing where the chromium has been etched (*Figure 2.8 2*). The exposure time, the light energy and the others parameters are calculated on the base of the resist type and thickness. An important parameter to consider during the photolithography process is the thickness of the resist mask. The thickness is usually determined by the etching step following the photolithography. After the patterning of the resist deposited on the wafer, the portion of silicon non-protected by the mask is attacked by the etching agent selected. Nevertheless also the mask is etched during the process through with a slower etching rate. The ratio between the etching rates of the two materials, silicon and the resist, is called selectivity of the resist. The resist thickness is so calculated depending on the silicon depth to be etched and the selectivity of the resist.

The wafer is then dipped in a solvent bath where the resist is developed and the areas exposed to UV light are dissolved (*Figure 2.8 3*). Now the resist mask is ready to be used for the next step that can be for example the etching of the wafer surface (*Figure 2.8 4*). As last step of the photolithography process the resist mask is removed with a dry of wet process (*Figure 2.8 5*). The dry stripping of the resist is done with an oxygen plasma beam while the wet process is done by dipping the wafer in a solvent bath that dissolves the unexposed resist.

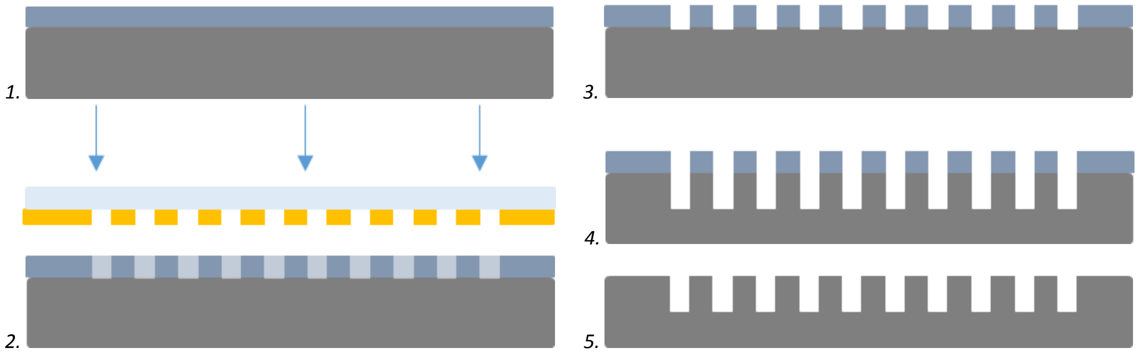


Figure 2.8: Photolithography process.

A picture of a wafer with the resist mask ready to be etched is shown in *Figure 2.9 a*. The channel design on the wafer is the one chosen for the NA62 project with two distribution manifolds at the inlet and two collection manifolds at the outlet. The mask in the picture is the one used to etch just the manifolds that have a different depth of the channels according to the circuit design.

Sometimes during the resist deposition and developing, a local defect can appear due to problems during the process. In *Figure 2.9 b* is possible to see a zoom of the green circle in *Figure 2.9 a*, where a defect is present on the resist mask. The defects can be due to a different air condition during deposition (temperature and humidity out of range in the cleanroom environment), or to internal defect of the resist. Another cause of defects in the resist mask can be the direct contact with the photomask during the UV exposition. In order to obtain the highest precision, the distance between the mask and the wafer is to be minimized up to the “direct contact” exposition. The contact can cause defects on the resist mask because, if the photomask is not perfectly cleaned, parts of resist can stick to the mask. In *Figure 2.9 b* is possible to see a small bubble in the resist, probably due to the presence of a contaminant particle, and also a missing part of resist on the wafer surface maybe due to the wafer and mask hard contact. In the resist hole is possible to see the wafer surface with the blue colour characteristic of the silicon oxide, below the resist.

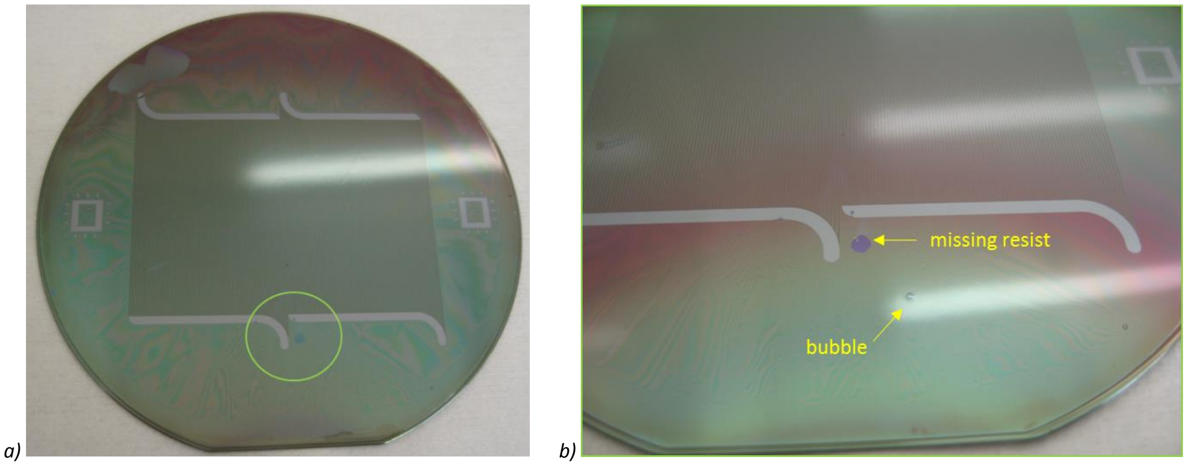


Figure 2.9: Photoresist mask deposited on a NA62 wafer before the etching of the manifolds.

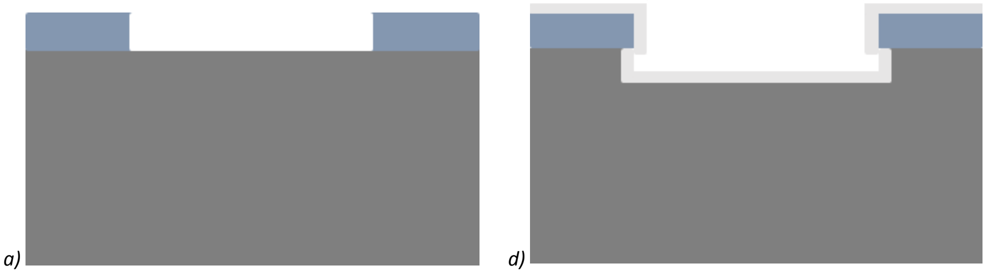
2.2.3 Etching the Channels

A lithography usually precedes an additive or a subtractive process. Materials are either added or removed from the wafer surface in a selective way following the pattern created with the lithography. In the silicon micro-channel fabrication, the next step in the process flow is to etch the channels on the wafer surface, which is a subtractive process. Usually the etching is done using the DRIE (Deep Reactive Ion Etching) process. DRIE etching is a dry etching technique, contrary to the wet etching where the wafer is dipped in an acid bath.

The dry etching is done in a vacuum chamber by a plasma hitting the wafer surface. The plasma etching is the result of an excited and ionized reactive gas that is mechanically and chemically attacking the wafer surface. The resulting profile of this etching process is an anisotropic etching with almost vertical sidewalls. Normally the etching process, as soon as the channels depth is growing, is affecting also the sidewalls by bouncing of the ions in the bottom of the channel.

The DRIE etching process, named also Bosch process, guarantees vertical sidewalls thanks to two alternating phases, an etching phase and a passivation phase (*Figure 2.10*). Two gases are alternatively pulsed in the vacuum chamber (*Figure 2.10 a*). An etching gas is bombarding the wafer surface and it starts to increase the channel depth (*Figure 2.10 b*). After a while, the ion particles start attaching also the sidewalls inducing an under-etching effect (*Figure 2.10 c*). To stop this behaviour the second gas is pulsed in the chamber and a thin polymer layer is deposited on the wafer surface and inside the channel (*Figure 2.10 d*). During the following phase the polymer in the bottom of the channel is etched immediately from the plasma and the channel depth is increased, while the polymer on the sides is protecting the walls from the bounce of the ions and the lateral etching is minimized (*Figure 2.10 e*). As soon as also the lateral polymer starts to be etched, a second passivation phase takes place and the polymer layer is redeposited on the wafer surface. At the end of the etching process the wall surface finishing is the resulting of the succession of the two phases, and it presents an indented profile with a chain of small circular arcs (*Figure 2.10 f*). This profile is called “scalloping” and it is shown in detail in the SEM image in *Figure 2.11* where is possible to see a tilted top view of a channel design for the LHCb micro-channel device. Varying the parameters of the two phases and varying the mask design can lead to different etched profiles (*Figure 2.12*). Normally with the same etching time, the wider profiles are deeper while the thinner profiles are less deep, due to side effects.

Using this Bosch process not only pure silicon can be etched, but it is also possible to etch silicon oxide of silicon nitride layers used during the micro-fabrication flow as insulating layers or hard masks to etch silicon.



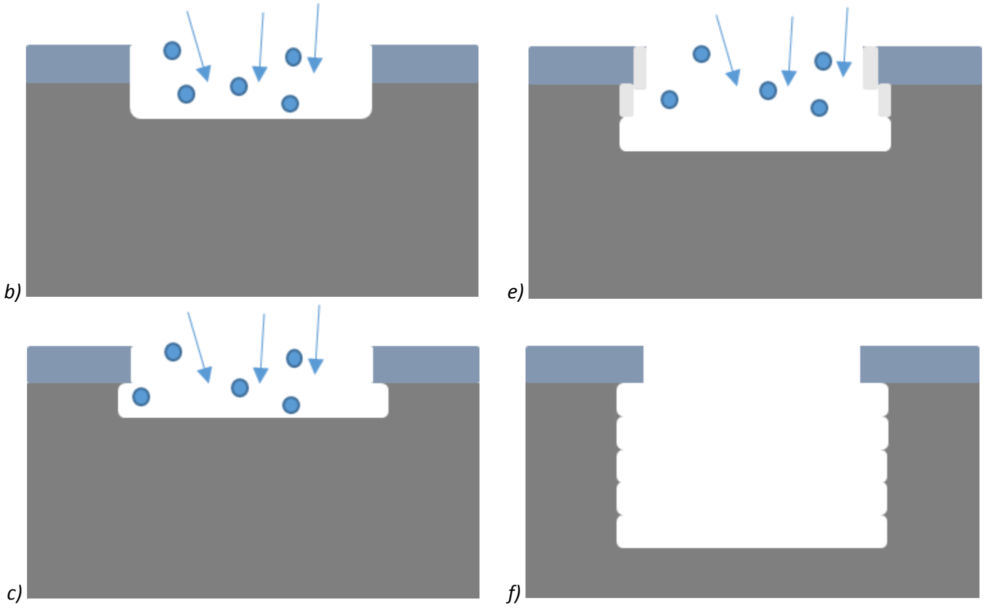


Figure 2.10: DRIE etching process steps.

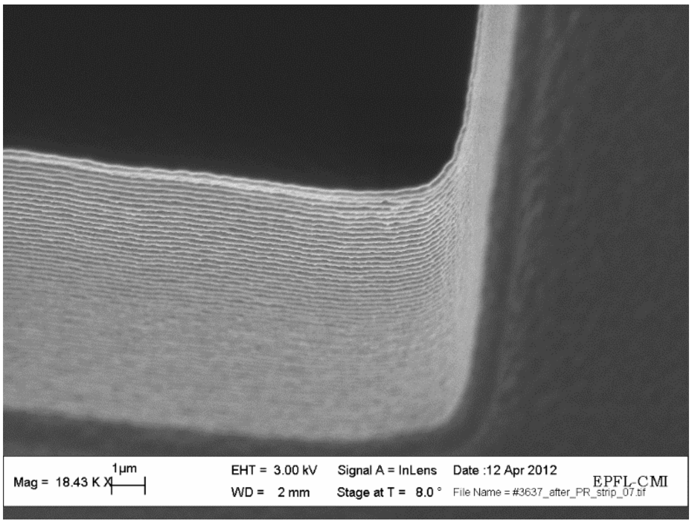


Figure 2.11: DRIE etching process scalloping effect on the sidewalls of a channel.

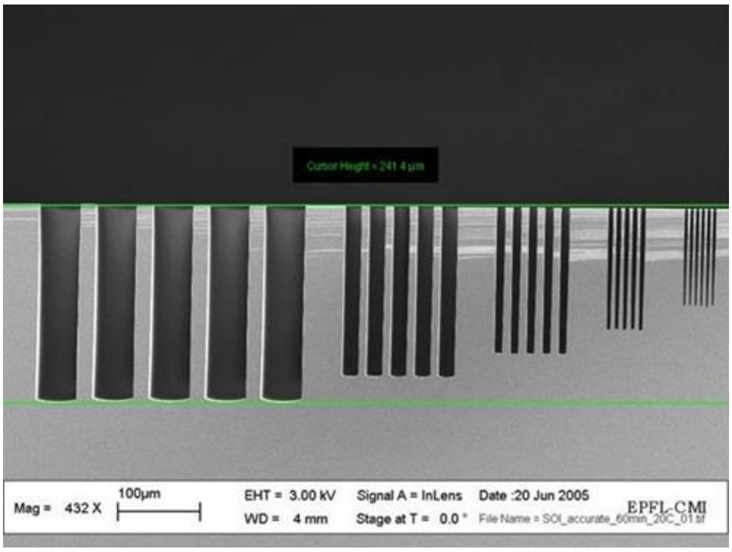
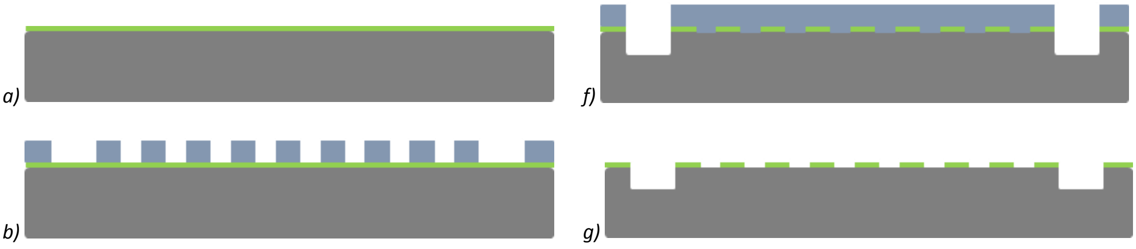


Figure 2.12: DRIE etching profiles obtained in the CMi EPFL cleanroom (Ref [22]).

In order to obtain different etching depths on the same wafer, for example for the channels and for the distribution manifolds, two photolithography steps are necessary. Since the sputtering of the resist on a wafer with already etched structures is almost impossible due to the non-uniform surface, two masks have to be present on the wafer surface at the same time. The first mask will be a hard mask done with an oxide layer while the second one will be a standard resist mask. The mask are then used in reverse order of how they are deposited on the wafer surface.

In *Figure 2.13* it is possible to see a small process flow of how to realize different depths on the same wafer surface. A standard resist photolithography mask is created on the wafer surface, using as support an oxide layer previously grown on the silicon surface (*Figure 2.13 a*). In this first resist mask both depths (the channels and the manifolds designs) are present (*Figure 2.13 b*). The first etching step is to etch the oxide layer on the silicon wafer (*Figure 2.13 c*). The resist mask is removed and the hard oxide mask is patterned on the silicon surface and it is ready to be used (*Figure 2.13 d*). A second resist mask is then created this time only with the deeper structure that is going to be realized, like the distribution manifolds (*Figure 2.13 e*). The etching of the silicon wafer starts with the depth corresponding to the difference between the two depths to be realized (*Figure 2.13 f*). Once this depth is reached, the resist mask is removed from the wafer surface (*Figure 2.13 g*). The oxide mask is ready to be used to perform the second etching step with the total depth of the less deep between the two structures (*Figure 2.13 h*). Since the two structures are present on this mask the less deep one, will be etched of the targeted amount, while the deeper one will be etched as the sum of the two etching steps. At the end of the process is possible to remove the oxide mask with a selective plasma etching or with a wet etching inside an acid chemical bath (*Figure 2.13 i*).



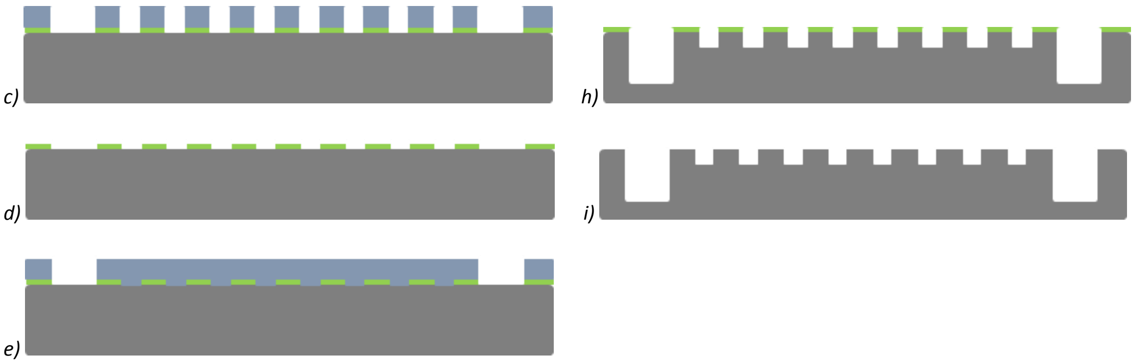


Figure 2.13: Process flow to realize two different etching depths on the same wafer.

A two-depths etching process is used for the final micro-channel device installed in the NA62 experiment. The 280 µm deep distribution and collection manifolds are etched in the bottom wafer (380 µm thick wafer), while the cooling channels are only 70 µm deep in the central area of the device. In *Figure 2.14 it* is possible to see a picture of a NA62 test device processed in the EPFL cleanroom after the etching on the channels and the manifold before the bonding with the cover wafer.

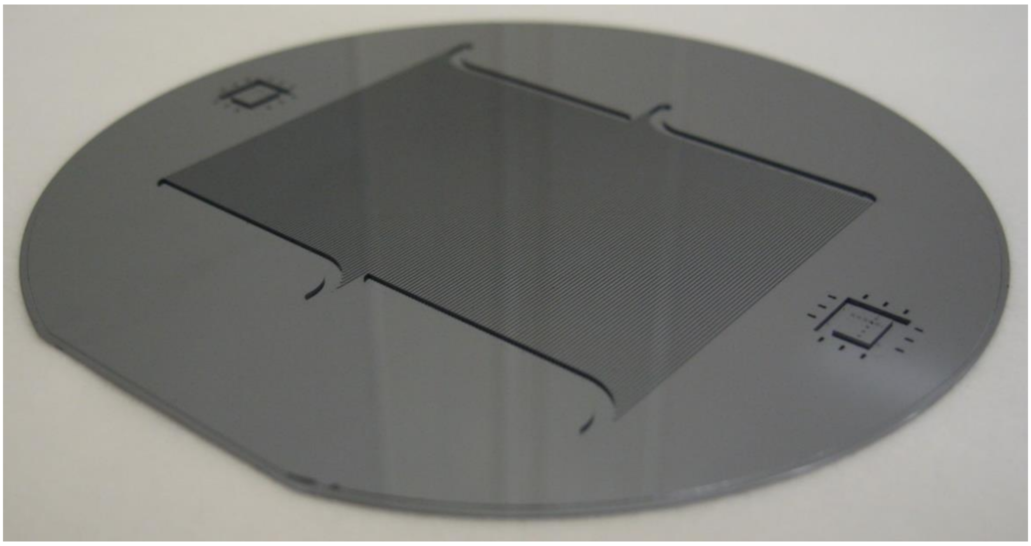


Figure 2.14: NA62 test device realized in the EPFL cleanroom with two etching depths.

2.2.4 Bonding of Cover Wafer

The next step in the micro-channel process flow is the bonding of the cover wafer. The cover wafer can be a Pyrex wafer or a silicon wafer. For the final installation in the detectors, a full silicon device (silicon cover wafer) is required for the CTE properties, for the transparency to particles and for the mechanical properties. Structural tests have been conducted evaluating the maximum pressure that can be sustained by a given amount of material on top of a micro-channel (see *Chapter 3*). Results show how a silicon membrane is holding much more pressure than a Pyrex one. For this reason, with the same fluid pressure, a full silicon device can be thinner than a silicon-Pyrex one, helping to minimize the material in the beam area. For testing purposes a Pyrex-silicon device is usually chosen because of the easier bonding technique and for the possibility offered of flow observation in the channels through the transparent wafer.

Both bonding processes (silicon on silicon and silicon on glass) belong to the “direct bonding” category [36]. A direct bonding is when two substrates are bonded together without using an intermediate adhesive layer. Contrary to the direct bonding, the indirect bonding involves the use of an intermediate layer that acts as adhesive agent. It can be made of different materials like metals, polymers or glass.

In theory two wafers of every materials can be bonded together at room temperature using the Van der Waals intermolecular forces. This type of bonding requires the wafer surfaces to be perfectly clean, flat and smooth but the bonding strength of the resulting bond is not very high. In order to obtain a stronger bond, the two wafer surfaces are placed in contact and then a driving force is acting to perform the bonding between the two. The driving force in bonding can be temperature, an electric field or a combination of the two. The silicon-Pyrex bonding process takes the name of *anodic bonding* while the silicon-silicon bonding is called *fusion or silicon direct bonding*.

The standard phases to obtain a direct bonding process start with the surface cleaning and wafer preparation, followed by the joining of the two surfaces at room temperature. At this point the bonding driving force is applied.

2.2.5 Anodic Bonding

The anodic bonding technique as sealing method between glass and silicon, was firstly presented by G. Wallis and D. I. Pomerantz in 1969 [37]. In the paper they present a new method to bond glass to metals and semiconductors. The setup used is based on a hot plate or a furnace in which the wafers are heated to the sealing temperature and then an electric field is applied to the wafer assembly. Starting from a test on the sealing of Pyrex (Corning 7740) to silicon, they selected the best temperature (300 – 600 °C) and voltage (200 – 2000 V) ranges. Temperature plays an important role in the anodic bonding since it increases the mobility of the ions in the glass. Based on this work and the works of others [38], [39], the selected temperature and voltage for the bonding of micro-channel wafers at CMi, were respectively 350 °C and 1000 V.

The anodic bonding process for the realization of the micro-channels test devices at EPFL, is done using a small controlled oven and two brass electrodes. The oven is set to 350 °C and, after the temperature is reached, a waiting time of at least 30 minutes is applied to let all the assembly be at a constant temperature. Once the temperature is set, the bonding voltage is applied. The glass wafer is connected to the anode while the silicon wafer is connected to the cathode. In *Figure 2.15 a* it is possible to see a scheme of the ion mobility during the bonding process. At high temperature the sodium oxide (NaO_2) molecules present in the Pyrex, decompose into sodium and oxygen ions. As soon as the voltage is applied the positive sodium ions (Na^+) start to migrate towards the anode glass surface while the negative oxygen ions (O^{2-}) are attracted by the negative silicon and migrate towards the two wafers interface (*Figure 2.15 b*). When the ions start to move, the current is flowing in the wafer, and during the process, when the ions start reaching the top surface or the interface between the two wafers, the current is decreasing. When the current reaches the 10% of its starting value, the anodic bonding is considered finished. The movement of the ions creates a depletion layer without the presence of free charge carriers. The electrostatic force in the assembly pulls the silicon and glass together. The negative oxygen ions at the interface react with the silicon and create a silicon oxide layer that, being insulator avoid further flow of the current.

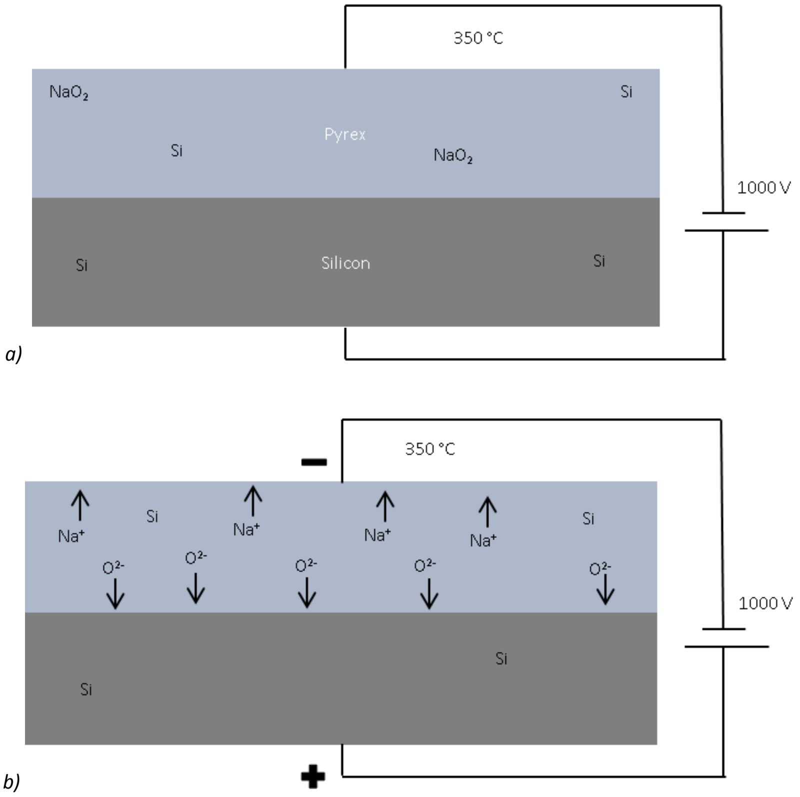


Figure 2.15: Anodic bonding scheme procedure.

In order to understand better the voltage and current behaviour during the bonding process, the values have been recorded during a bonding between a 2 mm thick Pyrex wafer and a 380 µm thick silicon wafer. The bonding was done at 350 °C with an applied voltage of 1000 V. In the graphs of *Figure 2.16* it is possible to see the voltage and current behaviours during the process. After setting the full voltage, the current reaches its maximum value of 12.5 mA and then start to decrease. At 0.8 mA (less than 10 % of the peak value) the voltage was removed and the bonding process was completed after around 13 minutes. By calculating the amount of current flowed in time is possible to see the total displaced charge inside the wafers during the entire process. The displaced charge can be used as an indicator for the bonding quality and the bond strength [40].

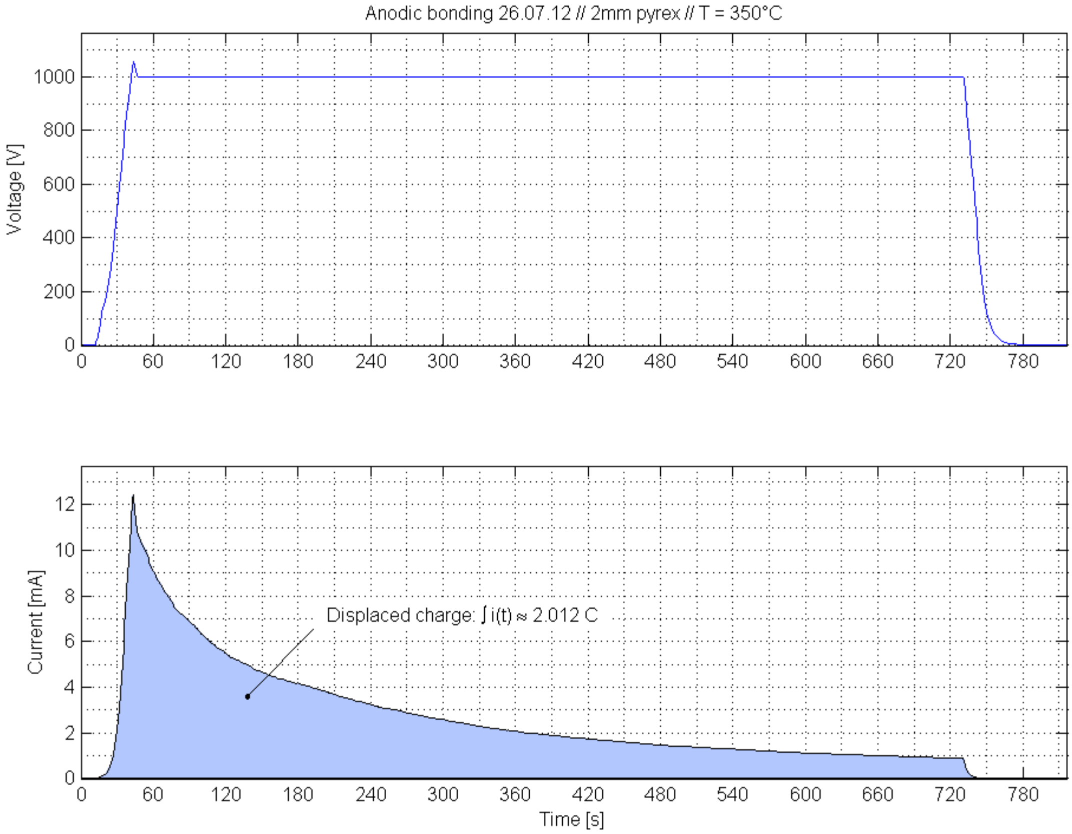


Figure 2.16: Anodic bonding current and voltage monitoring in EPFL.

In the anodic bonding process the quality inspection of a good bonding process is easy, since the defects are visible at the interface between the two wafers from the Pyrex side. The well bonded areas are dark while the defects appear in a lighter colour. In *Figure 2.17* it is possible to see bonded wafers with many defects at the interface. Both wafers were done as a test for the NA62 experiment. Bonding defects can be due to the presence of dust particles in the interface, to defects in the wafer surface, to roughness and others. In *Figure 2.17 b* the Pyrex wafer has been previously machined and four holes have been drilled inside it. This leads to the presence of bonding defects next to the drilled areas caused by the particles and the damages surface next to the hole.

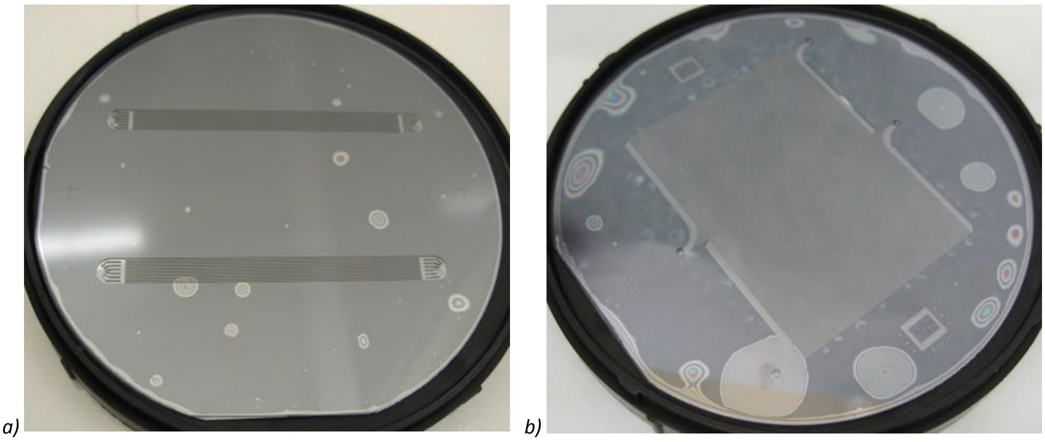


Figure 2.17: Anodic bonding tests done at EPFL for the NA62 experiment.

Cleaning is one of the key parameters for a good quality of anodic bonding. As suggested in different works [41], several cleaning ways and surface preparation have been tested. A cleaning method used was an oxygen plasma process with high power before the anodic bonding. Another test was done using the cleaning bath with the so-called “piranha solution”: H_2SO_4 acid boiling at 100 °C with H_2O_2 added at high temperature. For higher cleaning purposes also the combination of the two methods, “piranha” and oxygen plasma, was tested. Another tested bath was the RCA cleaning procedure with a mixture of different acids bath NH_4OH, HF, HCl at high temperatures. For the surface treatment a CMP (Chemical Mechanical Polishing) procedure was done on the silicon bonding surface followed by a RCA treatment. At the end of the test campaign the “piranha solution” was chosen as best cleaning method for the anodic bonding procedure in the EPFL CMi cleanroom.

2.2.6 Direct Bonding

In the direct bonding procedure, also called fusion bonding, two silicon wafers, with mirrored surfaces, are placed in direct contact without an intermediate layer. The bonding is the result of chemical reactions among the OH groups present on the wafer surface. Direct bonding can be performed at room temperature or low temperature [42], but usually a high annealing temperature (more than 800 °C) is applied to increase the interface energy and so the bonding strength. More than for the anodic bonding, the wafer cleaning is a very critical step in fusion bonding. During the cleaning of the wafer also a surface activation takes place. Two different bonding types are possible: the hydrophilic bonding [43] and the hydrophobic bonding [44]. In the hydrophilic process, at the bonding interface a thin layer of silicon dioxide is present while, in the hydrophobic bonding, no intermediate layer is used and just Si-Si bonds are present. For the hydrophilic type, the RCA cleaning leaves on the wafer surface a large number of silanol groups (Si-OH) responsible of the wafer bonding. For the hydrophobic instead the wafers are cleaned in HF solution to leave on the surface Si-H groups. In *Figure 2.18* and *Figure 2.19* it is possible to see in detail the chemical bonds present at the interface of the hydrophilic and hydrophobic bonding before and after the annealing step.

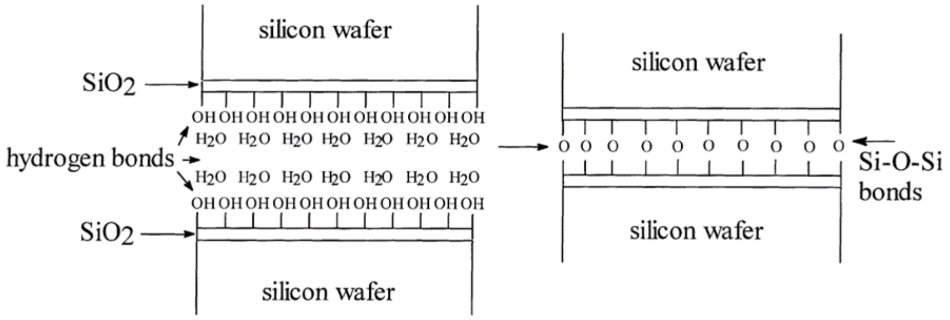


Figure 2.18: Direct bonding chemical bonds for the hydrophilic process before and after annealing (Ref [42]).

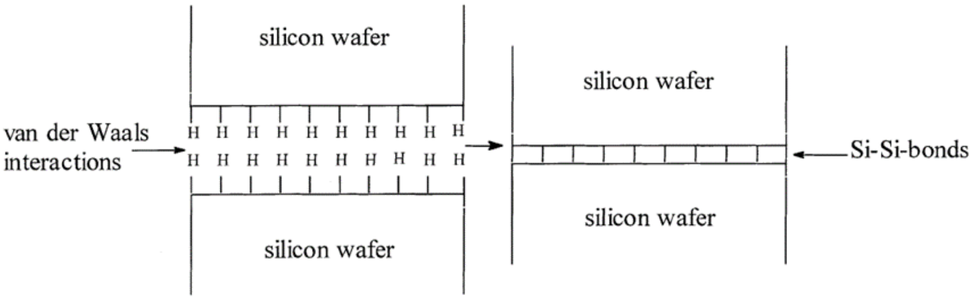
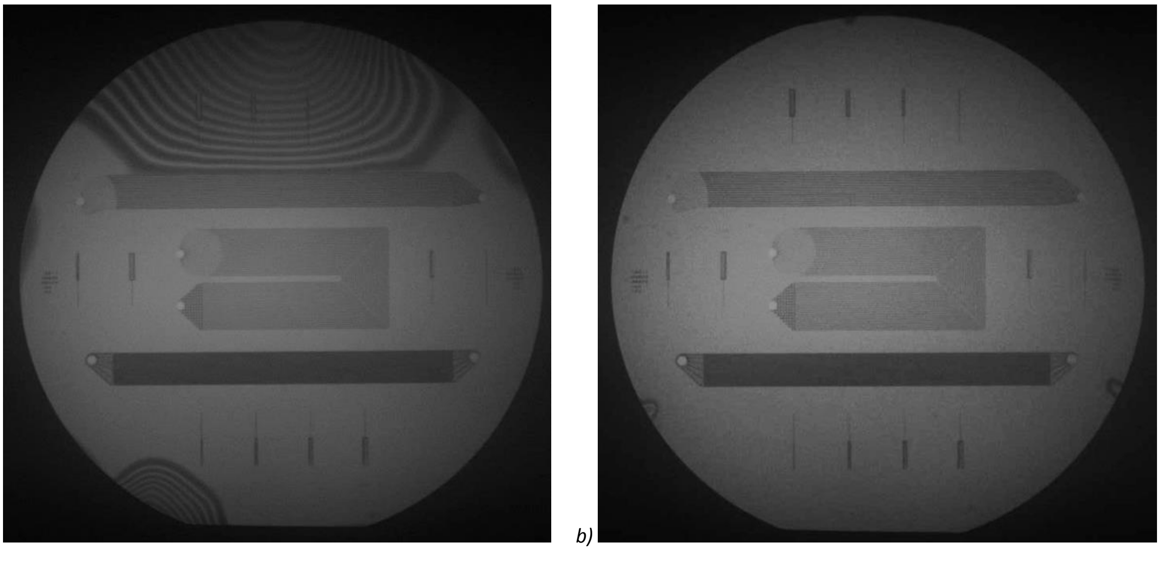


Figure 2.19: Direct bonding chemical bonds for the hydrophobic process before and after annealing (Ref [42]).

Due to the high cleaning requirements, inside the EPFL cleanroom the direct bonding process was never successful. Thanks to a collaboration between CERN and CSEM (Centre Suisse d'Electronique et de Microtechnique) [45] in Neuchatel, it was possible to process, inside the CMi cleanroom, 4'' silicon wafers until the bonding step and then send them to bond to CSEM. The final quality inspection is more complicated for the direct bonding than for the anodic bonding, since the interface in not visible. To test the bond quality, at CSEM infra-red images were done. In *Figure 2.20* is possible to see two examples of infra-red images done on the 4'' wafer to see the bonding interface. In the first wafer (*Figure 2.20 a*) it is possible to see how the top part of the wafer is un-bonded, while for the second test (*Figure 2.20 b*) only small defects are visible far from the micro-channels area.



a) *b)*

Figure 2.20: Direct bonding infra-red images of wafer processed inside the EPFL cleanroom and bonded by CSEM.

In order to assess the wafer bonding quality a specific method has been adopted by the PH-DT group. A specific test structure was inserted in the channel design to be etched on the wafer. The test structure is a single micro-channel, few mm long, with a single inlet for the fluid inlet and a small injection capillary. In the infra-red picture of *Figure 2.20 b,* it is possible to see 12 single channels test structures distributed on the wafer surface. The test structure aims to test the bonding quality by a destructive test. The fluid is injected in the channel and the pressure is slowly increased until the rupture of the sample. From the rupture pressure and observing the fracture mode, it is possible to check the bonding quality. If a test chip is well bonded, the silicon will break according to internal crystalline planes with an irregular surface, and the bonding surface will not be visible anymore. Instead if the bonding is not good, the fracture will occur along the two wafers interface and the flat and polished surface of the wafer before bonding, will be visible. In *Figure 2.21 a* it is possible to see the results of the pressure tests done for the wafer in *Figure 2.20 a*. The rupture pressures for each chip is reported in black on top of the picture of the broken chip. The red numbers below the chips are instead the widths, in microns, for each single channels in the wafer. All the test structures belonging to the top portion of the wafer in *Figure 2.21 a* show lower rupture pressures than the ones with the same channel widths coming from the other parts of the wafer. Form the infra-red picture (*Figure 2.20 a*) it is possible to see how only the top line of the test structures is affected by a bad bonding contact and this is confirmed from the results of the pressure tests. In the top left 1000 µm wide chip (*Figure 2.21 b)* is possible to see how the fracture interface corresponds to the bonding interface between the wafers. The bonding interface with the polished surface on one side and the etched channel on the other side is showed in the chip picture.

Usually the infra-red analysis in not considered the best method to analyse the bonding quality since it gives often fake positive results. This is due to the minor forces acting at the beginning of the bonding (hydrogen bonds or van der Waals forces) that can create an interface between the two wafers impossible to detect with infra-red images. For this reason the infra-red images are used for checking the wafer bonding quality but a proper method should be used in addition to these. A very efficient method to check the wafer bonding quality is acoustic imaging based on ultrasonic emission. This technique is very precise but also very difficult and expensive to perform.

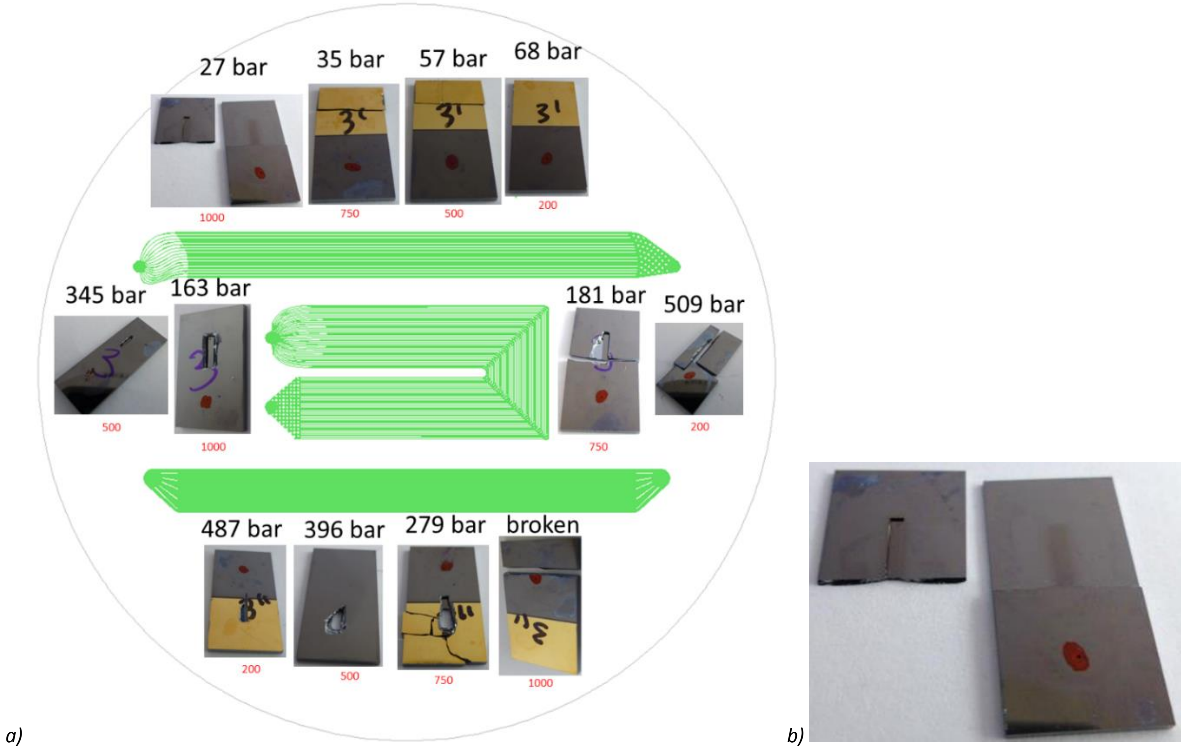


Figure 2.21: Pressure test results (a) to test the bonding quality of the wafer processed inside the EPFL cleanroom and bonded by CSEM and zoom of an un-bonded sample (b). (Black numbers: rupture pressure of the samples; red numbers: width of the sample channel in µm.)

2.2.7 Wafer Thinning

The following step in the micro-channel fabrication process flow is the thinning of the wafer in order to minimize the material crossed by the particle beam. The thinning of the wafer can be applied to the whole surface or can be done as a localized thinning applied just to the beam area. For the LHCb and ATLAS micro-channel test devices the entire wafer is thinned and the global thickness of the micro-channel device is decreased. Instead, for the NA62 and for the ALICE experiments the thinning is selective and just the internal part is thinned to minimized the material in the beam area while keeping a thicker external rigid frame.

For the selective thinning a silicon etching has to be done with a mask that avoids the etching of the external frame. The used etching method can be dry etching or wet etching.

For the thinning of the complete wafer a mechanical grinding of the silicon wafer is done, in some cases followed also by a chemical mechanical polishing.

The dry etching process is already been discussed in the previous paragraphs. The plasma etching to thin the central part of a wafer is used after a photolithography step, where the resist mask is deposited on the wafer surface to avoid the etching of the external frame. This technique is not uniform over the wafer surface and some areas are etched more than others depending from the machine configuration. The non-uniformity of the process can cause a problem for the targeted etching depth. If the silicon thickness reached in the central part is not uniform, the micro-channel device can be faulty and present problems during the operation, like fractures in the silicon structure due to the differences in thickness. For this reason, the dry etching process for thinning the central part of the micro-channel device, is only used with silicon-Pyrex devices to thin the silicon side up to the Pyrex and removing completely the silicon part. This technique can be clearly applied just to the design that do not have micro-channels in the central area or a specific stop-layer has to be foreseen. A stop-layer is usually made of an internal oxide layer in the wafer structure. As the area to be thinned in the two designs, for ALICE and for NA62, is in the order of few cm^2, the resist mask has to be as thick as possible to preview possible low selectivity of the mask. In *Figure 2.22* it is possible to see a silicon-Pyrex NA62 device with the central area etched by dry etching process.

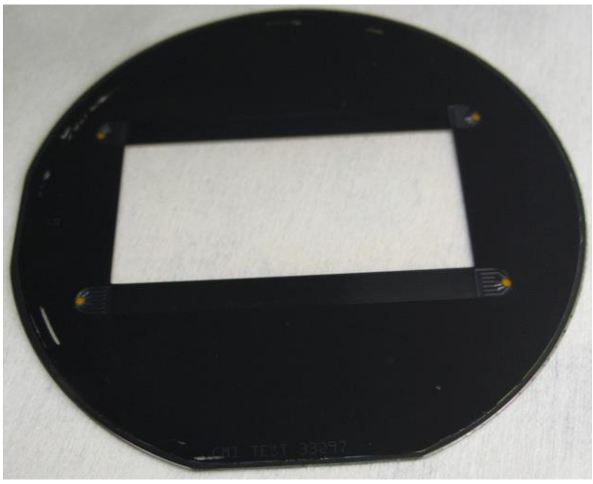


Figure 2.22: Dry etching process used to do the selective thinning of the central part in a NA62 device.

For the silicon-silicon devices or for the silicon-Pyrex devices that have channels in the central part, the wet etching process is used. The wet etching involves the dipping of the wafer into an acid bath where the silicon is attached by the acid solution and is uniformly etched [46]. Compared to the dry etching technique, wet etching guarantee a higher etching rate and high selectivity respect to the mask used. The wet etchants can perform an isotropic or anisotropic etching depending respectively, if the etching rate is equal in all directions or if the etching is faster in one direction compared to the others. The anisotropic etching can result in well-defined geometrical shapes that follow the silicon crystalline planes.

For the micro-channels application the desired wet etching is the anisotropic one, since the etching in the vertical direction has to be faster than the etching on the sides. The most common wet etchant for silicon anisotropic etching is the KOH solution. KOH etching rate depends from the bath temperature and the KOH concentration.

In the micro-channels process flow a 40% KOH concentration at 90 °C bath is used to perform the selective etching of the central area. The bath is also continuously mixed by a fluidic pump in order to obtain even more etching uniformity on the wafer surface. The used mask is a hard mask done in silicon oxide or in silicon nitride.

In most of the cases the wet etching step is performed in the process flow after the plasma etching of the inlets holes for the micro-fluidic circuit. After thinning of the central part of the wafer it is indeed very difficult to perform a photolithography for the etching of the holes, due to the wafer surface topography. For this reason a process flow similar to the two etching depths is used. A first hard mask in silicon oxide is created on the wafer surface for the etching of the central area and on top of it a resit mask is done for the etching of the inlets. The plasma etching is performed and the inlets are opened, the resist is removed and the wafer is ready with the hard mask for the KOH etching. In order to avoid the KOH to enter in the holes and destroy the internal structure of the micro-fluidic circuit, a special tool is used. The tool is machined in Teflon, a material that is not etched by the KOH, and Viton joints are used to seal the inlets of the micro-channel circuit. The leak tightness is guaranteed by the compression of the joints on the silicon surface done by holding bars fixed with stainless steel metallic parts and screws. In *Figure 2.23* it is possible to see the Teflon tool used for the NA62 experiment during the KOH etching of the central part.

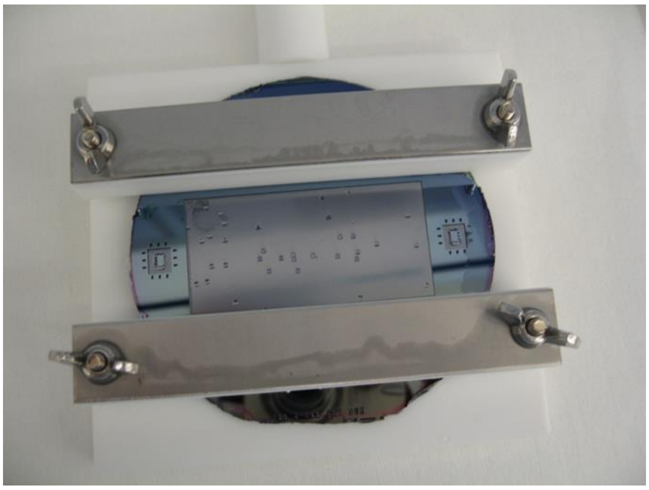


Figure 2.23: Teflon tool used for the wet etching in KOH of the NA62 micro-channels devices.

The mechanical thinning of the wafer surface to decrease the total device thickness, is done with a grinding process: abrasive particles of different sizes are mounted on a resin wheel and the wheel is turned on the wafer surface. The silicon wafer is thinned by the mechanical action of the abrasive particles. Grinding is very fast but it leaves a very coarse roughness on the silicon surface. The total depth of the marks on silicon may even reach 10 µm. Grinding is usually used when hundreds of micrometres of silicon have to be removed from the wafer surface. In *Figure 2.24* is possible to see the grinding marks left on a silicon chip surface after the grinding process.

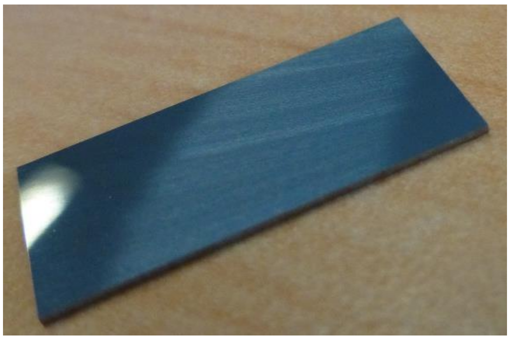


Figure 2.24: Grinding marks left on the silicon surface after grinding process.

The final step after the grinding process, to obtain a polished wafer surface, is the CMP (Chemical Mechanical Polishing) where abrasive particles, smaller than the ones used in the grinding process, are dispersed in a slurry. The wafer is hold upside down by a rotating chuck which pushes it on a polishing pad while rotating. The slurry is poured on the polishing pad and the wafer is polished by the chemical mechanical action at the atomic regime.

2.2.8 Metal Deposition

One of the last steps of the micro-channels process flow is the metal deposition for the soldering of the fluidic connectors on the device surface. In order to circulate the coolant fluid in the micro-channels, fluidic connectors are needed for the interface between the silicon surface and the external cooling tubes. A solution recently adopted by the PH-DT group, based on the original work of Murphy and others [47], involves the soldering of a metal connector to a metal layer deposited on the silicon surface. For further details on the connectors used see *Chapter 5*.

Several methods exist in micro-fabrication to deposit thin metal layers on a wafer surface. The method usually used in the EPFL cleanroom for the deposition of the metal around the inlets holes of the micro-channel devices is the sputtering. Sputtering is an example of a PVD (Physical Vapour Deposition) technique. The basic idea of the PVD technique is the material ejection from a solid target and its transport through vacuum towards the wafer surface. One PVD technique diverges from the other for the target excitation method. In sputtering the atoms of the material to deposit are ejected from the solid target with an argon ions bombardment. During the process the substrate is cooled down and the deposition can be done at room temperature. In *Figure 2.25* is possible to see a schematic principle of a general PVD technique.

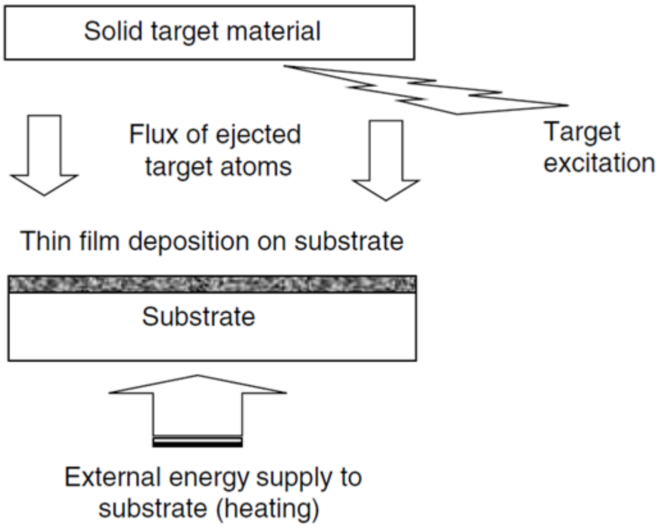
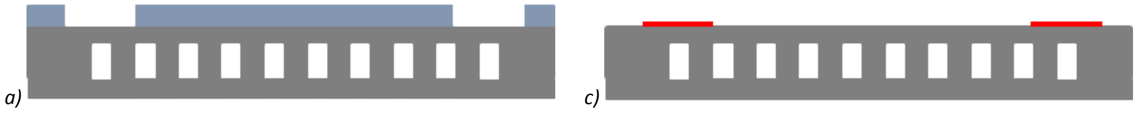


Figure 2.25: Schematic working principle of a PVD technique.

In order to deposit the metal only in the desired region of the wafer a mask is necessary. The mask can be a resist mask or a physical hard mask in metal, plastic or silicon.

If a resist mask is used a *lift-off* process is applied, in which the resist mask during the deposition, is protecting the areas where the metal has to be avoided and later is removed (*Figure 2.26*). The standard photolithography process is applied on the wafer surface to create a resist mask (*Figure 2.26 a*). The sputtering process takes place and the thin metal layer is deposited on the wafer surface (*Figure 2.26 b*). The wafer is then dipped in a solvent bath that dissolves the resist and leaves the metal where needed (*Figure 2.26 c*). In order to manage to deposit the resist mask on the wafer surface, this process can be done only on devices that have still the inlets holes closed. The etching of the holes will be done afterwards (*Figure 2.26 d*).



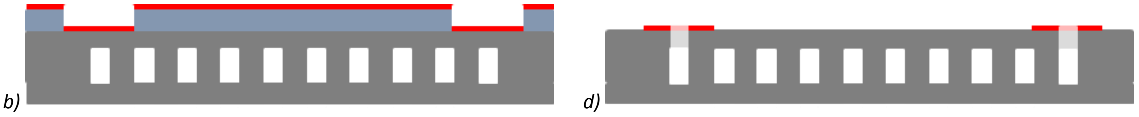


Figure 2.26: Schematic representation of the lift-off process for metal deposition.

When the inlets holes for the fluid are already opened on the wafer surface, for wafer topography reasons is impossible to use a resist mask, it is therefore necessary to use a hard mask. The hard mask is usually made by a thin disk machined to have the metal deposit where is needed. The mask can be done in different materials like plastic, silicon or metal.

For the ATLAS micro-channel devices a hard mask in stainless steel was machined at CERN and the sputtering deposition was done in the EPFL cleanroom. The mask was 0.5 mm thick and the mask design presented holes of 8 mm and even smaller holes up to 1.2 mm diameter. The mask was used to metalize six ATLAS micro-channel chips fixed on the back of the mask. In *Figure 2.27* it is possible to see a 3D model of the machined mask (*Figure 2.27 a*) and a picture of one of the resulting metallized chips (*Figure 2.27 b*).

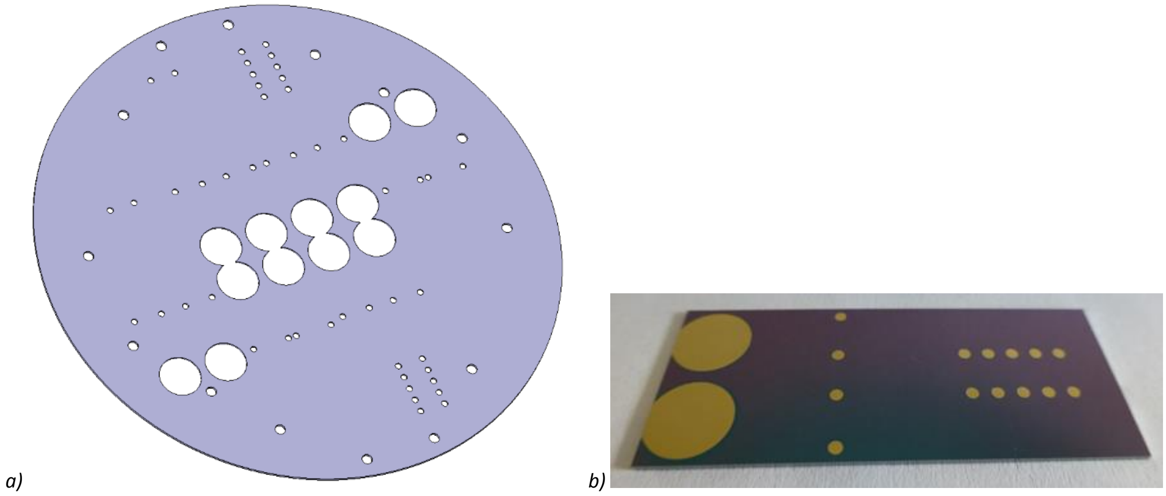


Figure 2.27: 3D model (a) of the stainless steel mask used for the metal deposition of the ATLAS micro-channel chips (b).

For the NA62 micro-channel device a hard mask in silicon was used. A silicon wafer with an oxide mask is completely etched in KOH across the total thickness in the areas where the oxide is not present. The round structures, like circles, in KOH are not reproducible, due to the KOH preference of etching along the crystalline planes (anisotropic etching). In *Figure 2.28 a* it is possible to see the silicon mask with four holes to perform the metallization on the NA62 micro-channels chip around the inlets holes (*Figure 2.28 b*).

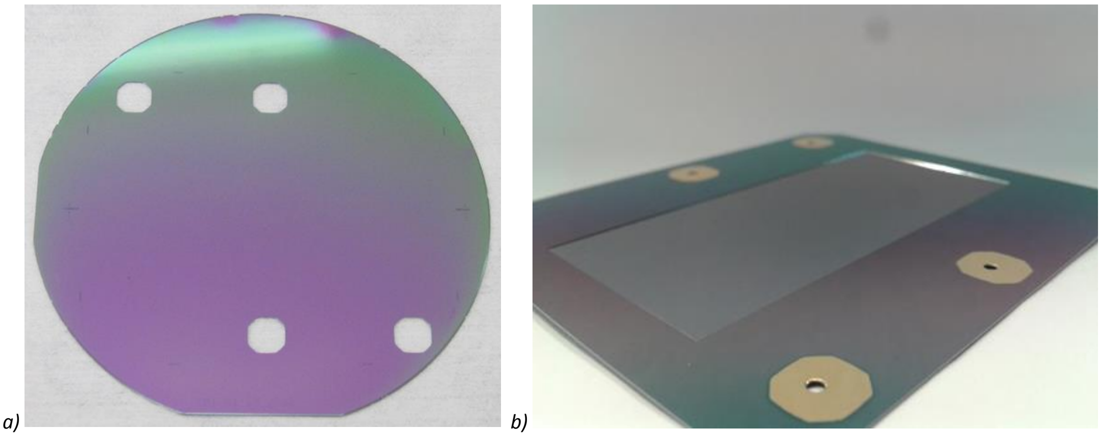

a) b)

Figure 2.28: Silicon mask (a) used for the metal deposition of the NA62 micro-channel chip (b).

2.2.9 Dicing of the Device

The final step in micro-fabrication is wafer dicing to separate the structures fabricated on the wafer. Wafer dicing inside the EPFL cleanroom is usually done using a spinning dicing blade. The saw usually is made of a hard thick central hub that has a thin rib impregnated with diamond sand. The hard hub can be made of different materials, the hardness of the material is chosen based on the substrate to dice. For the full silicon devices a saw with the hub in nickel in used. For the Pyrex-silicon devices a resinoid saw is used. The blade thickness and speed is defined by the device to be cut. The resinoid saw is rotating at 25000 rpm and has a cut speed of 1mm/s. The nickel saw instead has a 30000 rpm rotational speed with a cutting speed of 5 mm/s. The cut width on the wafer surface is 250 µm for the resinoid saw and around 100 µm for the nickel saw. The wafer is glued on an adhesive tape inside a metal ring that is mounted in the machine below the saw. During the cut the wafer is cooled down by a cooling water jet of around one litre per minute. The cut is usually performed by using alignment marks present on the wafer surface. The maximum wafer thickness that can be cut by the machine is given by the thickness of the thin rib with the diamond sand.

Sometimes it is necessary to partially cut the wafer in order to obtain a micro-channel device with a non-rectangular shape. For the LHCb experiment upgrade, for example, the micro-channel device proposed is a rectangular device with an L-shape edge. For cutting the L-shape edge, the above described process is not suitable, and a diamond wire saw was tested at CERN. The diamond wire is mounted in vertical between two pulleys that are rotating with alternating directions. The wafer is brought in contact with the cutting wire and is water cooled during the cut. At the corner position, the wafer is turned by 90° and the L-shape is done. Compared to the spinning saw, the wire saw is slower and the cut surface is more rough and inaccurate. In *Figure 2.29* it is possible to see the difference in the cuts performed with the spinning saw (*Figure 2.29 a*) and the wire saw (*Figure 2.29 b*).

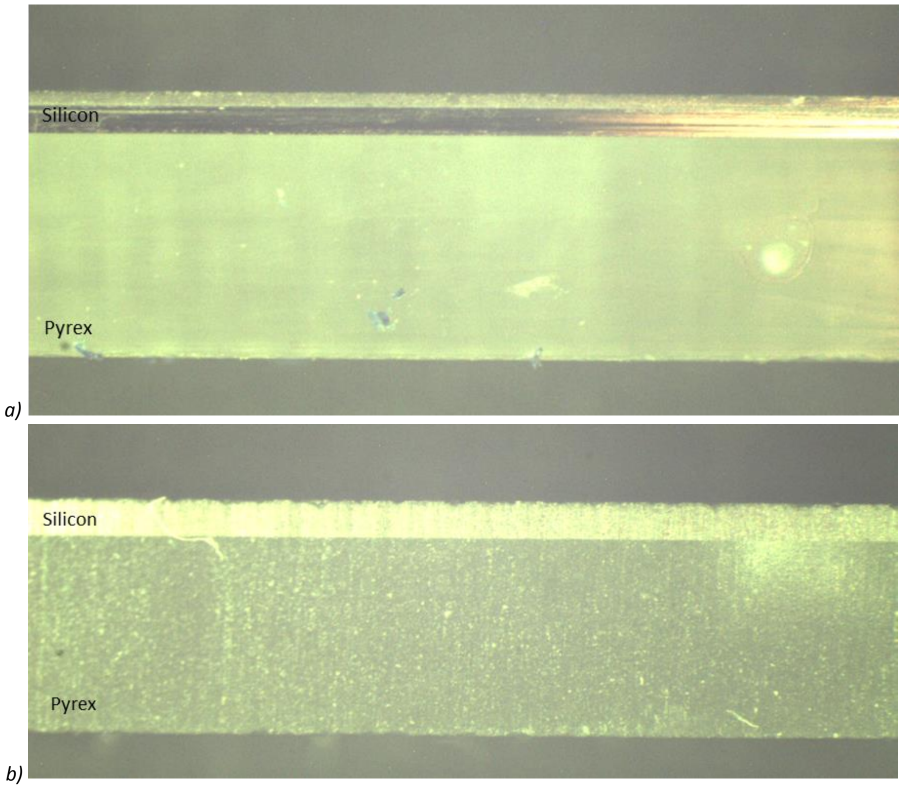


Figure 2.29: Cut surface on a silicon-Pyrex device done with the spinning saw (a) and the wire saw (b).

3 SILICON PRESSURE TESTS

In micro-channel fluidic devices, silicon is not used for its semiconductor properties but it is instead used as a structural material holding the internal fluid pressure and acting as the support for the silicon detectors. Thanks to the high precision micro-fabrication techniques, silicon can be used as a high-strength, high-precision and high-reliability mechanical material. Miniaturized mechanical devices and components can be realized for application fields where mechanical and electronics parts are integrated. Application fields are for examples pressure transducers, silicon printing heads and cantilever beams [48].

In micro-channel devices, silicon has to be minimized in thickness to decrease the particle interaction. This requirement is clearly in disagreement with the pressures of the cooling fluids inside the micro-channels, particularly high, for instance, when CO2 is used. In fact, in order to sustain the fluid pressures, the silicon thickness on top of the channels has to be increased, contrary to the physics requirement.

In order to forecast the silicon thickness that can be left on top of a channel with a safety margin to avoid silicon ruptures, experimental and simulation methods have been applied.

Silicon is well known in literature for its semiconductor properties but in the mechanical field many characteristics are unknown. From a simulation point of view, simulating with FEM (Finite Element Analysis) the rupture of a silicon micro-channel filled with pressure can be quite difficult and not much work is available in literature.

From the experimental point of view, in order to have at least a reference value for pressure and thickness to design the micro-channels for the experiments, a testing method has been developed. A study is conducted on single-channel test chips, with an inlet for the channel and no outlet, in which the internal pressure is increased up to the rupture of the samples. The channel width and silicon thickness for each test chip, are modified in such a way to develop a correlation between the rupture pressure, the channels width and the silicon thickness. The experimental results are then used to foresee the rupture pressure of new devices and also to provide a basis for the simulations. The goal is to develop a forecast method for the maximum pressure that can be applied in a micro-channel device.

Interpreting the results of such test campaigns must however take into account that several different factors are influencing the fracture strength of a silicon membrane [49]. Possible factors are the membrane shape at the intersection with the channel vertical walls, the membrane thickness, the bonding between the two wafers, the membrane stress, the membrane surface roughness and many others. Only some of these factors are evaluated in this chapter and further research will be conducted on this subject.

In order to understand the maximum fluid pressure that a micro-channel device can hold, test structures are fabricated and tested in pressure. The test structures used are silicon-silicon devices or silicon-Pyrex chips with the micro-channels etched inside. The channels are filled with water increasing the internal pressure up to the channels rupture. The test structures can be single or multi-channel structures designed on purpose for this test with just an inlet hole and no outlet hole, or can be circulating devices where one of the two inlets is sealed.

For every device the breaking behaviour is analysed and studied to understand better the silicon properties as a mechanical material. Furthermore the pressure tests give also an idea about the bonding quality. If the bonding is bad the device under test is failing at the interface between the two wafers and the silicon membrane on top of the channels is not tested.

3.1 TEST SETUP

All the pressure tests described below are tested in the CERN PH-DT laboratory, using a pressure test stand built for this purpose. The fluid used for the pressure tests is demineralized water and the pressure is applied using a manual water pump. The pressure injected in the samples under test is measured trough a pressure sensor fixed on the tube between the pump and the samples. The pressure sensor values are recorded and saved using a Labview program.
A typical pressure behaviour during a test is shown in *Figure 3.1*. In this case the pressure in increased by the operator up to the sample rupture. When the samples is broken the pressure decreases suddenly and the test is over. The samples is always kept under a transparent protection structure to avoid small silicon particles to be shot everywhere.

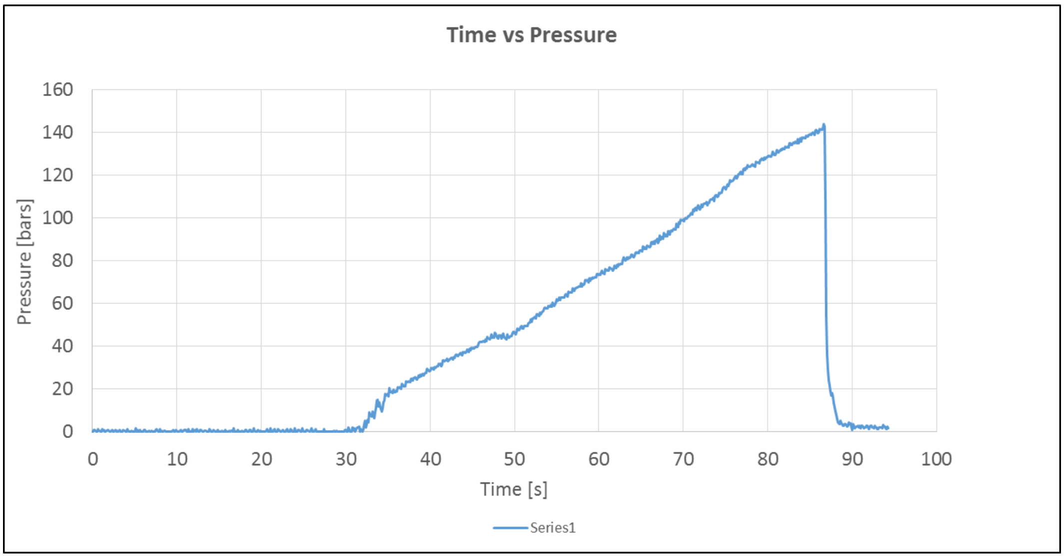


Figure 3.1: Graph of a pressure test with the pressure behaviour in time.

The drawback of this system applied to several samples, is the low repeatability of the tests. From one test to the other, a large uncertainty is introduced by the operator using the manual pump. It is almost impossible to reproduce the same pressure ramp used from one test, to in the following one. A big improvement for the system repeatability is the use of an automatic pump. For this purpose the test stand was modified and an automatic pressure multiplier was added. The upgraded system block diagram can be seen in *Figure 3.2*. The system is composed by a piezoelectric valve that pilots a pressure multiplier. The valve produces a controlled air pressure and the pressure multiplier transmits the corresponding amplified water pressure for the test. The pressure multiplier selected has a factor 1:46, where for 1 bar of air, 46 bar of water are sent in the experiment. The pressure at the output of the pressure multiplier is monitored using a pressure sensor. In order to improve the system reliability a security valve is installed at the inlet to stop the air flow if necessary. Also an exhaust valve is installed on the water side to empty the tubes from water if necessary. The automatic setup is controlled by a Labview program that sends commands to the piezoelectric valve and to the safety valve, while reading the pressure sensors output values.

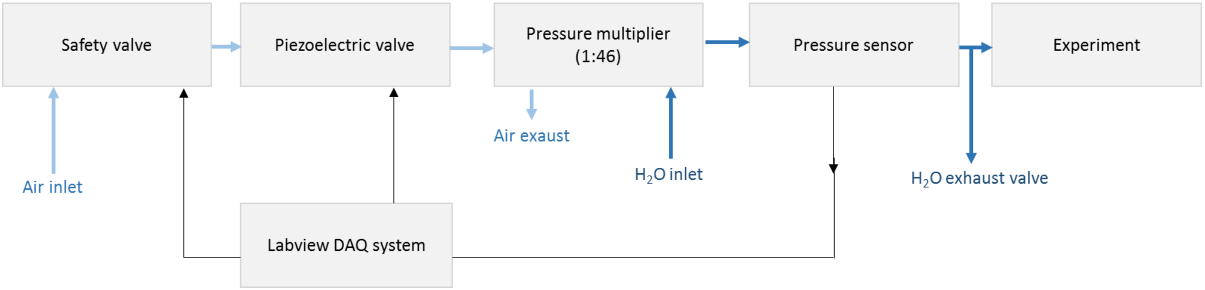


Figure 3.2: Block diagram of the automatic setup for pressure tests.

Using this automatic setup, it is possible to realize a controlled and repeatable pressure ramp-up. The pressure multiplier is able to increase the pressure in controlled steps, but there is no way to decrease the water pressure in the tubes during operation, and so cycling tests are not possible.

Another drawback of the system is the low accuracy that prevents the program to understand when the sample is broken. In the manual test stand, the operator, when the sample is broken and the water pressure read by the pressure sensor decreases, stops the pump and ends the tests. In the automatic system, it is the piezoelectric valve that should be controlled and that should discharge the pressure and stop the cycle. In order to do this procedure in an automatic way, a tentative modification to the program is done. The pressure ramp profile, input for the piezoelectric valve, is divided in several time steps. At the end of each time step, the pressure sensor is checked, if the pressure measured at the output of the system is lower than the one set to the pump the test is stopped. If instead the pressure is the same, the ramp is continued up to the rupture. Unfortunately, the flow exiting from the test sample at the rupture is so small that is very difficult to see the pressure decrease with the pressure sensor in short time stamps. This means that, reached the following step without any visible pressure change, the piezoelectric valve keeps sending the same amount of pressure. The result of the tests is not indicating the exact moment and the corresponding pressure at which the sample broke, since the system is not aware of the sample break. Other modifications, maybe increasing the time stamps and adding another pressure sensor before the pressure multiplier can be done to improve the system.

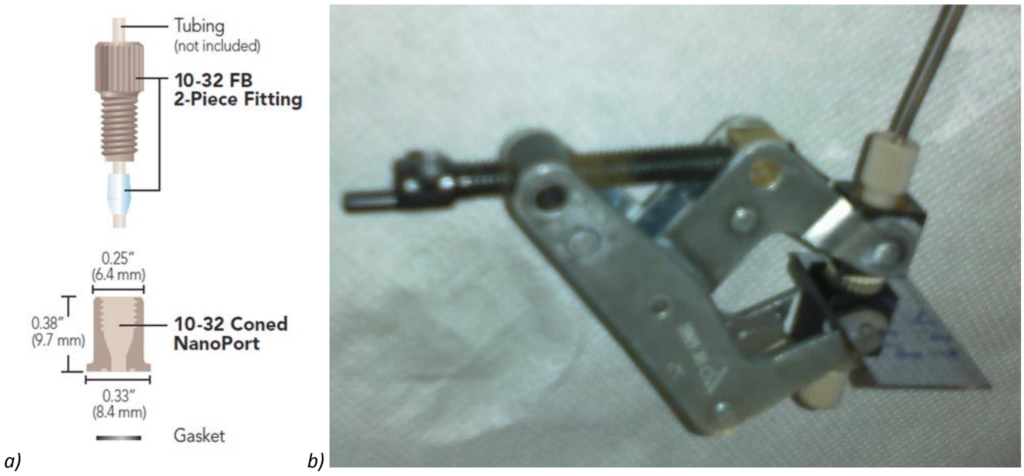
Further research is going on for this setup to provide a better program to control the automatic pressure test setup. All the test results shown in this chapter are done with the manual water pump.

3.2 PRESSURE TESTS CONNECTORS

The fluidic connector to join the test stand tube and the pressure structure under test, is a very critical point for the testing procedure. The connector should be re-usable for multiple tests in order to simplify the testing procedure and it should be also reliable and capable of guaranteeing repeatable tests. Furthermore it should not over constrain the test structure but let it free to deform and break for the internal pressure.

Following these requirements, glued or soldered connectors were discarded and the proposed connector for the pressure tests was based on a clamping system with an o-ring for guaranteeing the leak-tightness. One critical aspect of this type of connector is to understand the required clamping pressure to guarantee the leak tightness without damaging the chip under test. Another crucial point is to guarantee the perfect perpendicularity between the two connector parts and guarantee the uniformity of the applied clamping pressure on the chip surface.

The first connector was made using a standard fluidic connector in PEEK from Idex [50]. The clamping system is shown in *Figure 3.3 b*. The two arms of the clamp, end with two turning joints that become parallel to the chip surface once the chip is inserted and clamped between the two. Inside the joints two Idex connectors are glued. The Idex connector is composed of two parts: a female part in contact with the chip surface and a male one with the tube inside (*Figure 3.3 a*). The female part provides the leak-tightness of the system with the compression of the gasket against the chip surface. The male part is screwed inside the female one and holds the fluidic tube. On the other arm of the clamp, is glued another female Idex connector to provide mirror balance to the compression force of the o-ring. The chip alignment is done by eye using the visual access from the top female connector before screwing the male part inside.



a) b)

Figure 3.3 Idex connector scheme (a) (Ref.[50]) and first clamping connector for pressure tests (b).

This connector has been used for several tests but, at high pressure (more than 30 bar) the compression force from the clamp acting on the two o-rings damages the chip structure. In order to hold high water pressures the compression force of the gasket is increased to avoid leaks, but in this way the chip structure is stressed by the gasket footprint on the two sides of the chip. With the test chip under stress, when the water is entering the micro-channel with high pressure, the chip can break. In *Figure 3.4* can be seen how one chip under test broke due to the gasket compression force.

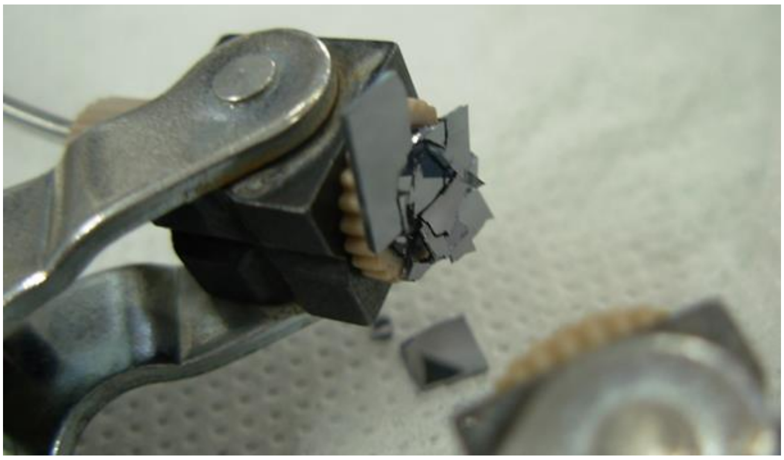


Figure 3.4: Broken chip for the two gaskets compression force on the two sides of the chip.

In order to avoid the rupture of the chips tested at high clamping pressure, a tentative improvement is done to the connector. On the bottom side of the clamp, the female Idex connector is removed and a flat precise machined brass part is glued. In this way the chip is not stressed between two gasket footprints but there is just the front gasket pushing against a flat surface. Pictures of the modified connectors are shown in *Figure 3.5*. In the top arm of the clamp is kept the Idex connector with the black gasket to perform the leak tightness, while in the bottom arm the brass piece is glued (*Figure 3.5 a*). The chip is inserted between the two arms and, when the connector is closed, the turning joints with the Idex connector and the brass part, are aligned perpendicular to the chip surface (*Figure 3.5 b*).

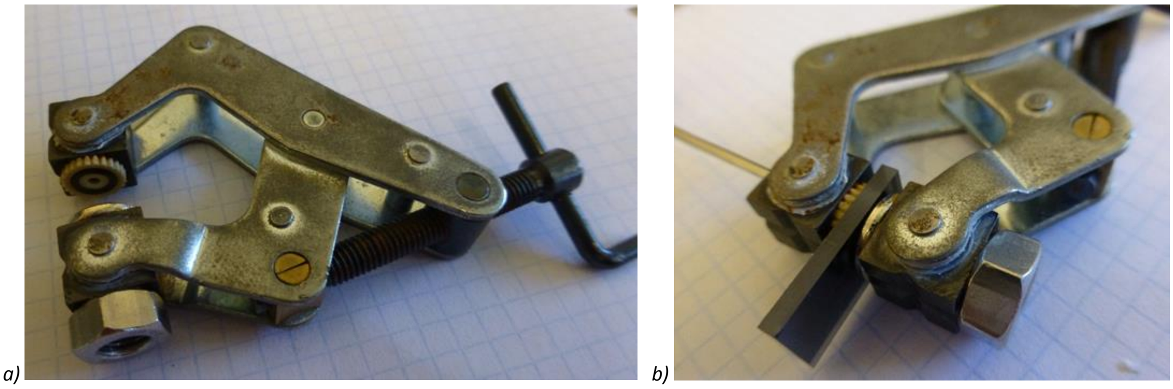


Figure 3.5: Modified connector with one Idex component on the top part, without (a) and with a chip under test (b).

This version of connector is used with pressures up to 150 bar. For higher pressures the connector starts to have leaking problems due to the mechanical structure of the clamp. An improved connector, designed on purpose for high pressures, is made by two parallel metallic bars screwed together with two screws (*Figure 3.6 a*). On the top bar a fluidic connector with a rubber gasket is inserted while the bottom one is completely flat. The improvement of this connector compared to the previous one is to have a much smaller gasket in diameter and a stiffer structure. A smaller gasket allows to have a smaller area under pressure and the rigidity of the structure guarantees a more uniform distributed pressure on the chip surface. The chip is inserted between the two metal bars and the alignment is done from the visual access inside the fluidic connector before connecting it to the tube (*Figure 3.6 b*). When the chip is inserted in between the bars, the two screws are closed simultaneously in order to guarantee the parallelism between the two bars. The o-ring, visible in *Figure 3.7*, is compressed between the chip surface and the top metal bar. The compression value is selected on the basis of the water pressure of the test, but in general the top metal bar should never be in contact with the silicon surface to avoid rupture of the sample.

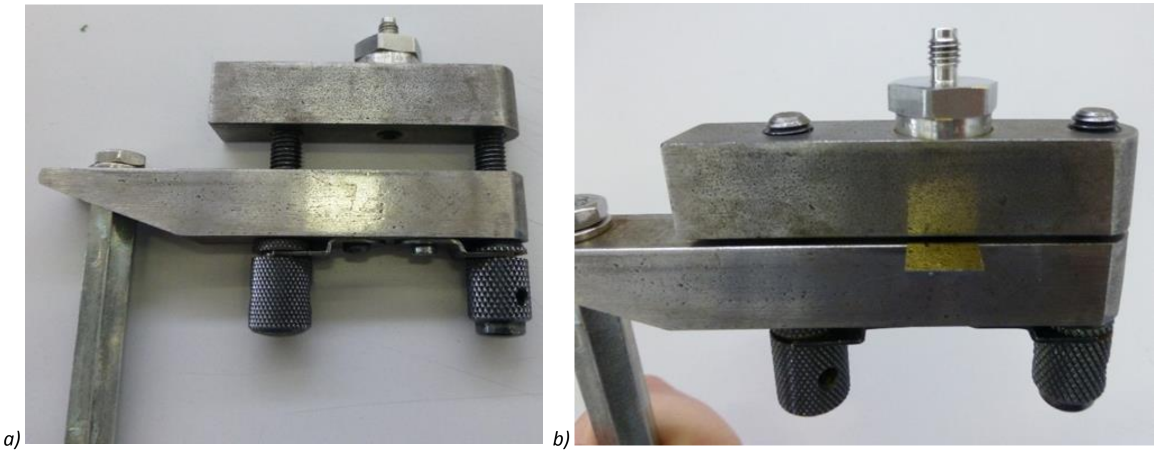


Figure 3.6: Improved connector design for high pressure test, without (a) and with the chip under test (b).

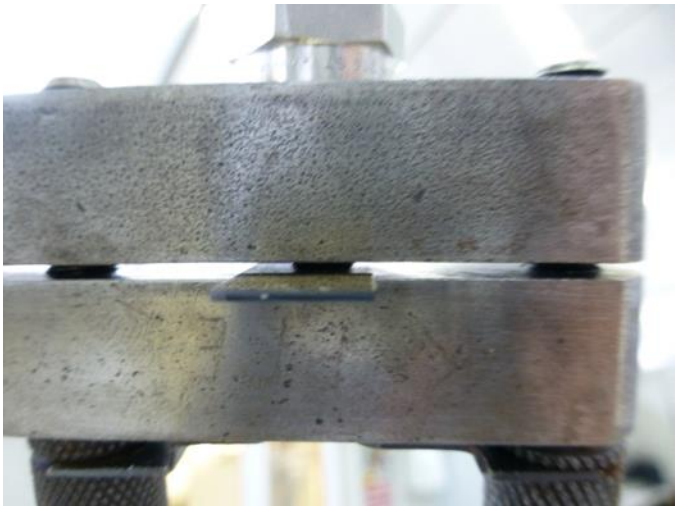


Figure 3.7: Closed connector for high pressure with the chip under test inside.

A last version of connector has been proposed in the frame of a general PH-DT study for testing in series several test structures with the same dimensions. The connectors presented so far, are indeed based on the visual alignment that should be done for each chip under test. If a family of test structures has the inlet hole in the same position respect to the outer edges, a mechanical alignment system can be proposed. Based on the high pressure connector shown in *Figure 3.7*, a standardized connector has been designed with two metal parts and two closing screws (*Figure 3.8 a*). On the top part on the fluidic connector, the tube for the fluid is connected. In this case there is no need of disconnecting the tube every time for visual alignment, since the alignment is performed mechanically. In the bottom part of the connector (*Figure 3.8 b*) a groove with the lateral width of the standardized pressure test chip is machined and, at the end of the groove, a small alignment pin is inserted to stop the chip in the vertical direction. As a result, the chip is mechanically aligned with the top hole for the fluid injection.

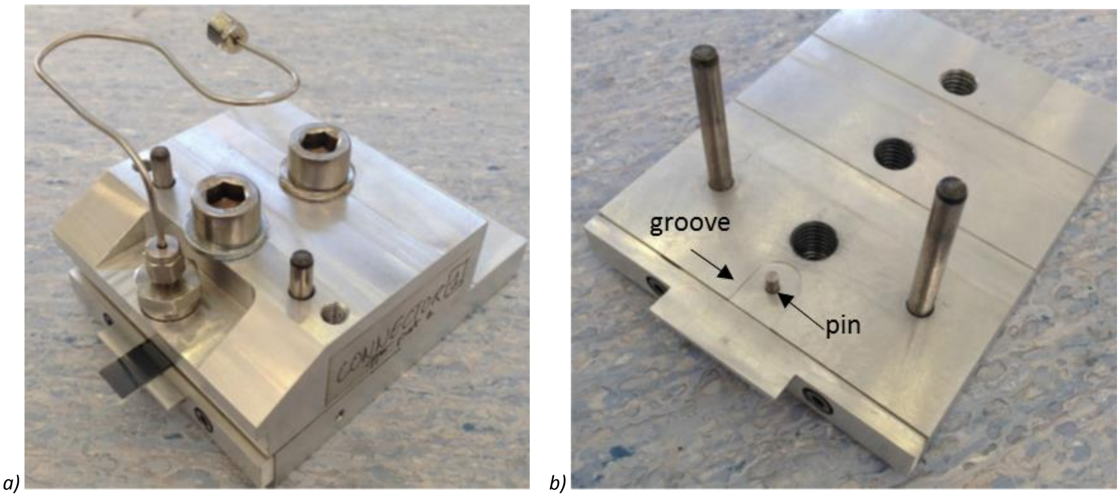


Figure 3.8: Standardized connector for chip testing in series: closed (a) and open connector (b).

3.3 SINGLE-CHANNEL TEST STRUCTURES

After analysing in detail the test stand and the fluidic connectors used during the tests, in the next sections the design of the pressure test chips is described. The tested chips are of two different designs: single channel structures and full fluidic structures with multiple parallel channels.

The single channel test structures are designed on purpose to measure the maximum pressure that a channel of a certain width and silicon thickness can hold during operation. The channel to be tested has a thin distribution channel with a small hole, through which the liquid is injected. In *Figure 3.9* it is possible to see a sketch (*Figure 3.9 a*) and a picture (*Figure 3.9 b*) of the single-channel silicon-Pyrex test structure. Usually for each structure an identification number that refers to the channels width in microns is etched on the silicon surface.

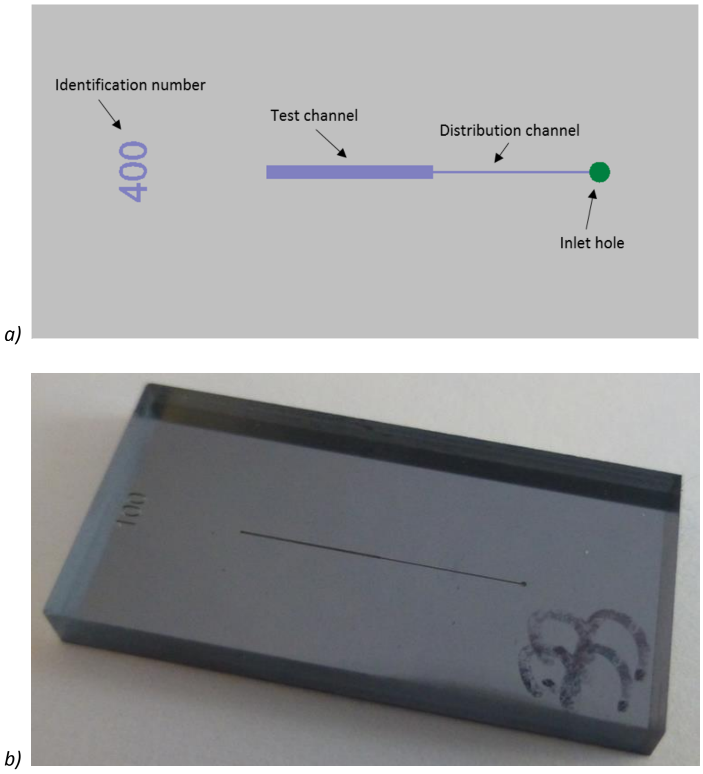


Figure 3.9: Sketch (a) and picture (b) of a single-channel pressure test structure.

3.3.1 Single-channels Silicon/Pyrex

Some of the tested test structures are produced inside the EPFL cleanroom. The fabricated devices are in silicon-Pyrex, with a Pyrex wafer 2 mm thick on the top side of the structure to hold the high pressure applied during test. The silicon-Pyrex chips are fabricated with different silicon thicknesses and channels widths. The simplified process flow of these devices is visible in *Figure 3.10*. A silicon wafer 525 µm thick, is prepared for the etching with a photolithography process (*Figure 3.10 a*), the etching of the channels is done with dry etching up to a depth of 80 µm (*Figure 3.10 b*), the silicon wafer is then bonded to the Pyrex wafer (*Figure 3.10 c*), and finally the inlet holes are opened with dry etching from the silicon backside (*Figure 3.10 d*). At this level just the thinning on the silicon side and the dicing of the wafers is performed. The thinning is done at different target thicknesses to test the silicon strength.

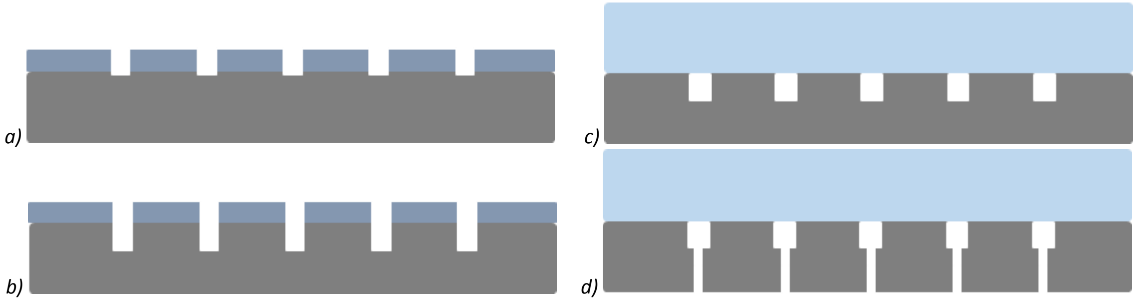


Figure 3.10: Pressure test structure process flow.

Similar tests were conducted by Blom *et al.* [51], they performed pressure tests on micro-channels to test the anodic bonding energy. They observed two failure mechanisms of the micro-channel chips. Since micro-channels are often fabricated by bonding of two wafers, the maximum pressure is directly related to the failure either of the bond, or of one of the two wafers. The micro-channels tested by Blom are silicon-Pyrex structures with a thinner Pyrex wafer designed to to determine the bonding energy of the anodic bonding depending on the bonding temperature. The two failure mechanisms observed are shown in *Figure 3.11*, in the first case (*Figure 3.11 a*) the Pyrex is cracking right at the edge of the channel for the bending and shear stress in the structure exceeding the maximum stress that Pyrex can withstand. In the second case (*Figure 3.11 b*), the bonding interface between silicon and Pyrex is opening for the high pressure.

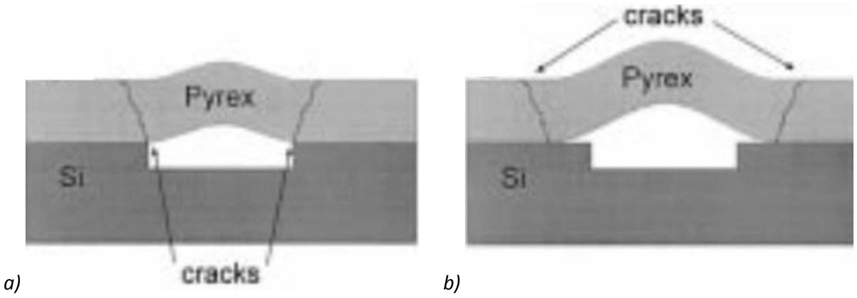


Figure 3.11: Channel failure mechanisms (Ref [51])[50].

A very similar behaviour is observed also in the test done on the single-channels structure by PH-DT. The two different failure mechanisms described in [51] are found, but the behaviour of Pyrex and silicon is opposite. These samples are specifically designed to test the silicon resistance to pressure, and the Pyrex side is much thicker than the silicon side, so that the failure always occurs in the silicon side. The two failure mechanisms are shown in *Figure 3.12* where the channels profile is represented by a dashed square. In one case (*Figure 3.12 a*) the silicon membrane is stressed and the fracture occurs in the silicon wafer starting from the channel edges. In the other case (*Figure 3.12 c*) the bonding interface between Pyrex and silicon is stressed and the fracture mechanism starts opening the bonding to reach the top of the silicon wafer only after a significant widening of the surface subject to pressure. The pictures of the tested samples corresponding to the two rupture modes are also shown in *Figure 3.12 b* and *Figure 3.12 d*. It is worth noticing that only the first case of rupture provides a quantitative indication of the resistance to pressure of the silicon membrane. In the second case the wafer bonding collapses before (possibly due to local imperfections), and it is only possible to infer that the silicon membrane withstands higher pressures that the one measured.

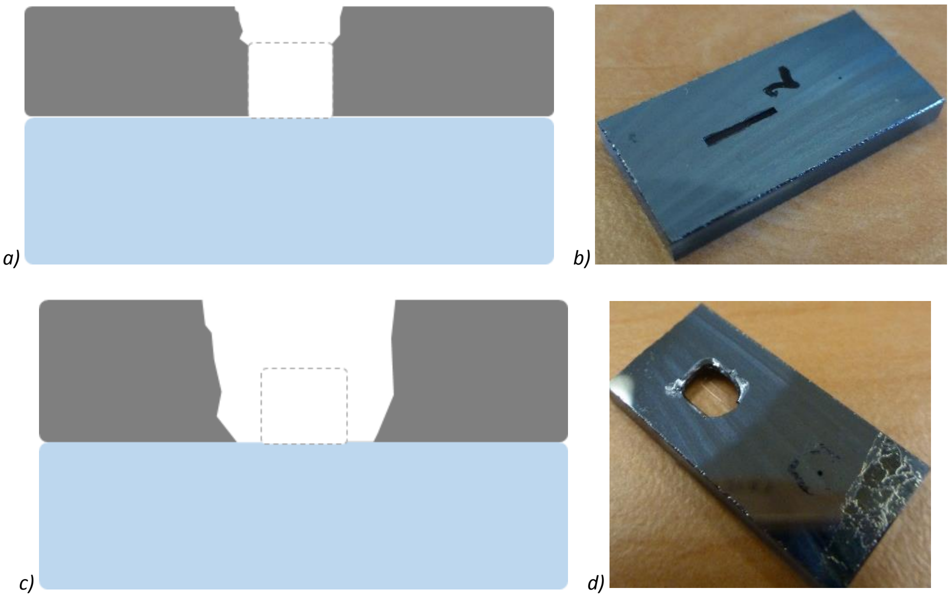


Figure 3.12: Sketch of the fracture modes on the single-channel test structures in Pyrex-silicon.

During the micro-fabrication etching step, a channel depth of 80 µm is targeted but the etching uniformity of the dry etching process over the wafer surface is not always very accurate. Furthermore the plasma etching process is geometry dependent, meaning that the channel width is influencing the channels depth. After the etching step a measurement of the channels depths, over the wafer area, may show a sensitive non-uniformity of the etching process. In *Figure 3.13* it is possible to see, as an example, the photolithography mask used for this process with the corresponding measurements of some channels depths obtained during one realization. The measurements are performed using a mechanical profilometer for surface measurements. From the measures it is possible to see how in this case the non-uniformity over the wafer surface is very high, reaching also 12 µm of depth difference between two channels. On the other hand, the thinning process by grinding and CMP is extremely uniform over the whole wafer surface. For this reason, the effective thickness of the silicon membrane over the channel can vary of several microns from sample to sample even in the same wafer.

Due to this problem, in order to get the measure of the membrane thickness as precise as possible, a direct post-test thickness measurement is done on each chip. After the pressure test, each sample is cut in half and the broken channel section is observed under the microscope, measuring also the silicon thickness on top of the channel. In *Figure 3.14* is possible to see a measure of the channel thickness done with the optical microscope (*Figure 3.14 a*) and with the SEM (*Figure 3.14 b*).

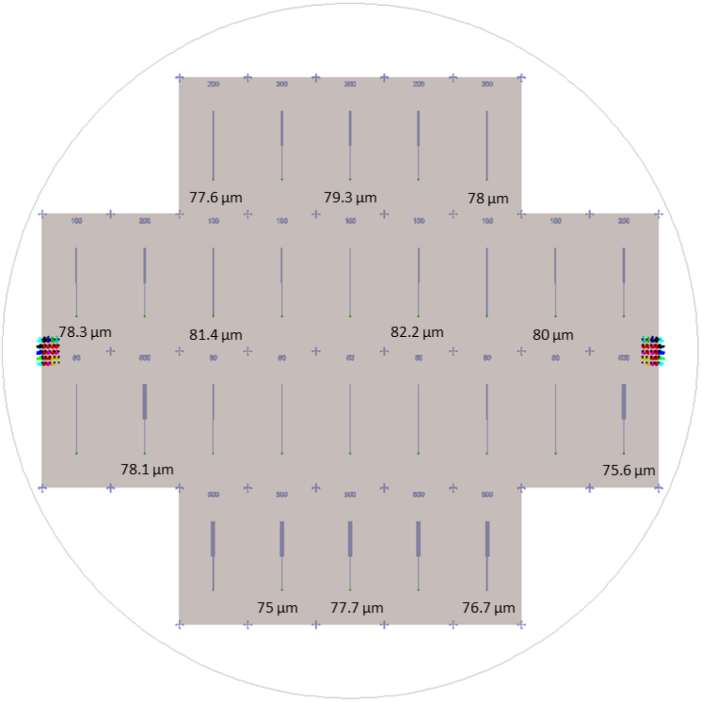


Figure 3.13: Photolithography mask used for the fabrication for the Pyrex-silicon pressure test with the some channels depths after etching.

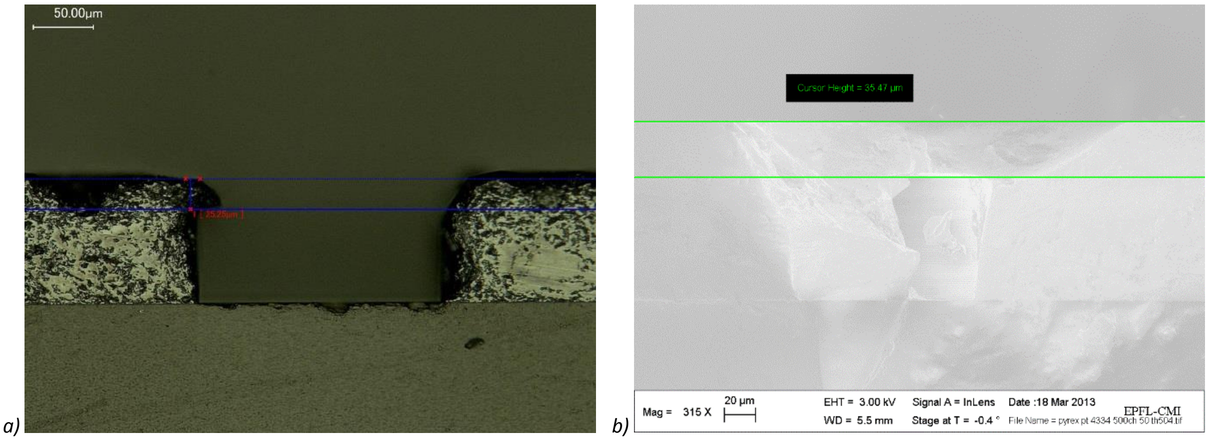


Figure 3.14: Section of the broken channel after testing and silicon thickness measure using the optical microscope (a) and the SEM (b).

The pressure tests executed show how with wider channels and thinner silicon layers the fracture pressure decreases significantly. In *Figure 3.15* it is possible to see for each channel width (100 µm, 200 µm, 500 µm), the fracture pressure plotted versus the silicon membrane thickness on top of the channel measured with the microscope. A tentative fitting line is plotted for each channel width but the scattering among the results is high, probably due to internal defects of the silicon samples.

The results have been taken into account as reference for the design of micro-channel devices for the experiments. Further research is nevertheless necessary to understand better the bond at the interface between Pyrex and silicon and the silicon strength.

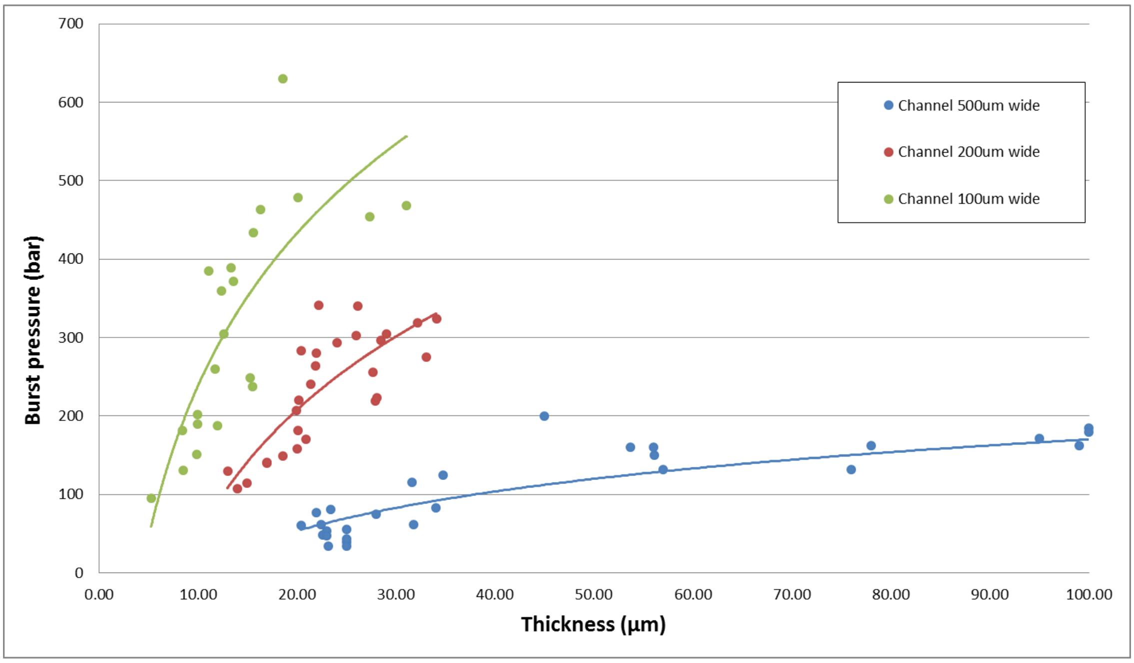


Figure 3.15: Test results for the silicon-Pyrex pressure tests with different channels widths.

3.3.2 Single-channels Silicon/Silicon

Silicon-silicon single-channel test structures have been also tested to understand the maximum pressure that a full silicon channel can sustain. Due to the difficulty of the direct bonding process, the silicon-silicon test devices were produced by external companies and not inside the EPFL cleanroom. Pressure tests structures have been added on the wafer surface of several micro-channel devices ordered to external companies.

Similarly to what shown for the Pyrex-silicon samples, the maximum pressure depends by the strength of the bonding at the interface between the two wafers. For the same channels width, with the same silicon thickness on top, a good bonding is holding more pressure than a bad bonding. The pressure test devices were also used to check the bonding quality of the wafer produced by the companies (see *2*).

Another important aspect of the pressure test structures, is the internal channel structure that is influencing the rupture mode. Following a process flow similar to the Pyrex-silicon devices, the single-channel structures are etched in a wafer until the desired depth and then a second wafer is bonded on top to close the channels. The internal corners of the channel are different at the top and at the bottom, because of the etching process on one side and the bonding with the cover wafer on the other side. The bottom corners of the channel, etched with the plasma, present a small curvature, depending on the parameters of the etching process. The top corners instead, bonded with the cover wafer, present 90° straight corners. In *Figure 3.16* it is possible to see a SEM image, done in the EPFL cleanroom, of the channel cross section of a silicon-silicon pressure test structure after test, fabricated by the IceMos company in Ireland [52]. The difference between the corners on the bottom and on the top is well visible in the enlarged images reported in *Figure 3.17 a,b.* From the basic theory of fracture mechanics, it is evident that the corners with a bigger curvature are more resistant while the sharp ones can be crack initiators and lead to the samples rupture. In fact, in *Figure 3.17 b* it is possible to notice how the fracture crack is starting from the top right corner. Next to the channel top edge, it is still possible to see the bonding line between the two wafers, symptom of an unprecise direct bonding.

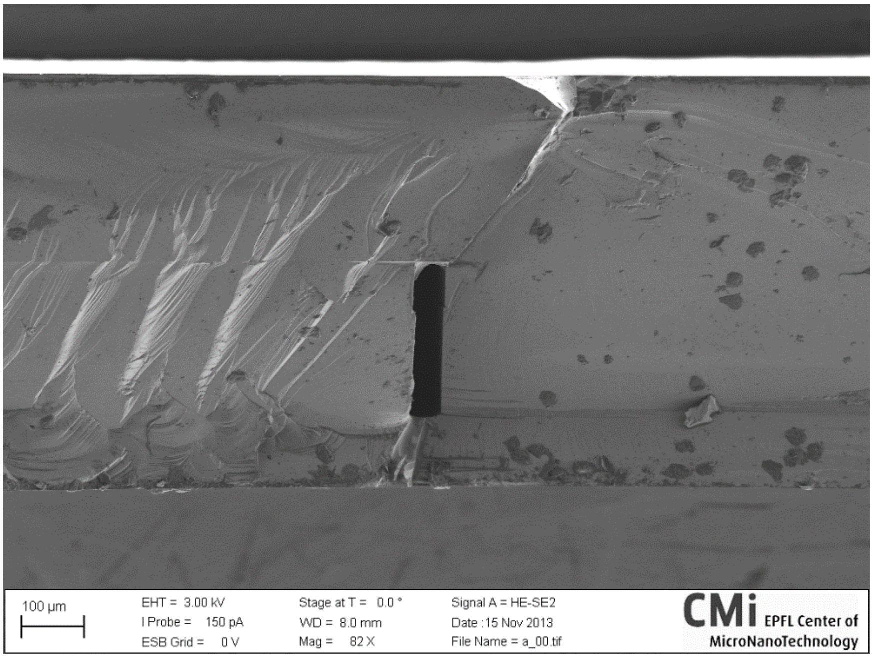


Figure 3.16: SEM image of the channels cross section of a pressure test structure after testing done by IceMos company.

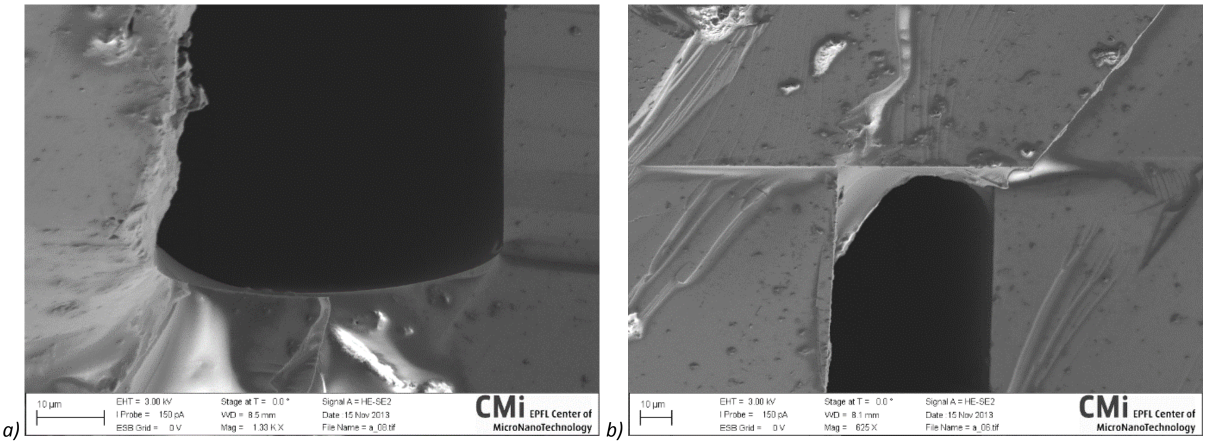


Figure 3.17: SEM images of the channel bottom (a) and top (b) corners.

Due to the crystalline nature of silicon, the crack starts from the edges of the channel and breaks the silicon following the crystalline planes. The same behaviour was observed in other tests that presented tilted fracture planes starting from the channel edges. In *Figure 3.18* it is possible to see a picture from top of a broken channel (*Figure 3.18 a*) and a SEM magnification of the broken area (yellow circle in *Figure 3.18 a*), where the fracture planes are tilted respect to the channel walls (*Figure 3.18 b*).

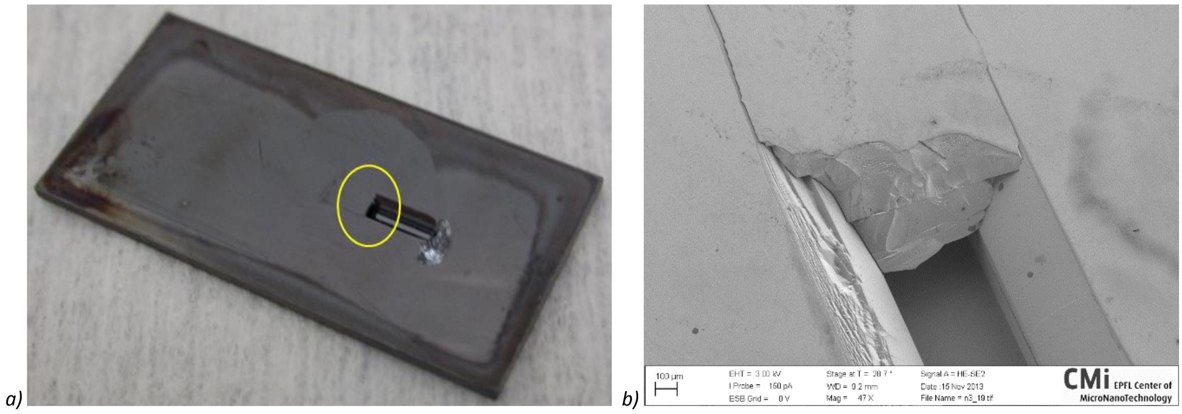


Figure 3.18: Camera picture of a tested sample (a) and SEM image of the tilted fracture planes (b).

For the IceMos chips, a tentative plot of the silicon thickness versus the maximum pressure for each channel width, similar to the one presented for the Pyrex-silicon results, is shown in *Figure 3.19*. In the silicon-silicon case the scattering between the results is much higher than in the Pyrex-silicon test due to the influence of the more erratic quality of the direct bonding on the results.

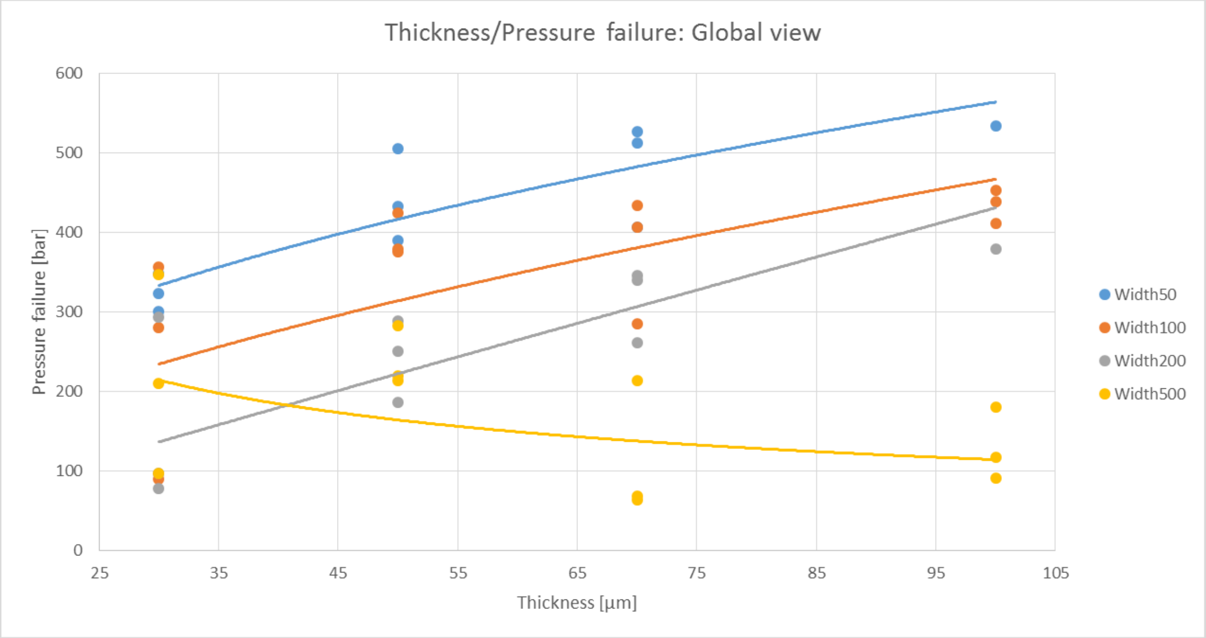


Figure 3.19: Test results for the silicon-silicon pressure tests from IceMos with different channels widths.

3.4 MULTI-CHANNELS TEST STRUCTURES

In the single-channel test structure the goal was to identify the maximum pressure that a channel of fixed width can sustain with a certain silicon thickness on top. On the other hand, the multi-channel test structures are used to test specific design features of a complete micro-channel device. In this section two examples of design features for the NA62 and the LHCb experiments are described.

In order to investigate the mechanical resistance of the micro-cooling device for the NA62 experiment, test structures with the design of the starting part of the distribution manifolds have been produced. Different samples have been fabricated inside the EPFL cleanroom in silicon-Pyrex. On the samples, the first part of the distribution manifold and the attached channels have been reproduced (*Figure*

3.20 a). In order to discover the maximum pressure that this structure can hold, different samples have been produced varying the manifold width: the original NA62 manifold is 1.6 mm wide, while on the fabricated samples other two widths of 1 mm and 1.3 mm, have been designed. The fabricated samples have the same channel dimensions and depths as the NA62 micro-channel plate. The process flow for fabricating this devices starts with a 380 µm thick silicon wafer where the manifold are etched until 280 µm while the channels are only 70 µm deep. The silicon wafer is than bonded at 350 °C to a 525 µm thick Pyrex wafer to close the channels. The weaker area of the sample is the area below the manifold with 100 µm thickness of silicon left. The purpose of the test is to understand if this area can hold the operation pressure for the NA62 experiment.

From the tests results it turned out that 525 µm of Pyrex are less resistant than 100 µm of silicon over the manifold area. In the majority of the tested samples, the failure occurs in the Pyrex wafer. For the 1.3 mm and 1 mm wide manifolds, the fracture is always on the Pyrex side (*Figure 3.20 a*). For the 1.6 mm wide manifold, few samples show a silicon fracture (*Figure 3.20 b*) at an average pressure of more than 30 bar. This maximum pressure largely fulfils the experiment requirements (maximum operation pressure of 10 bar).

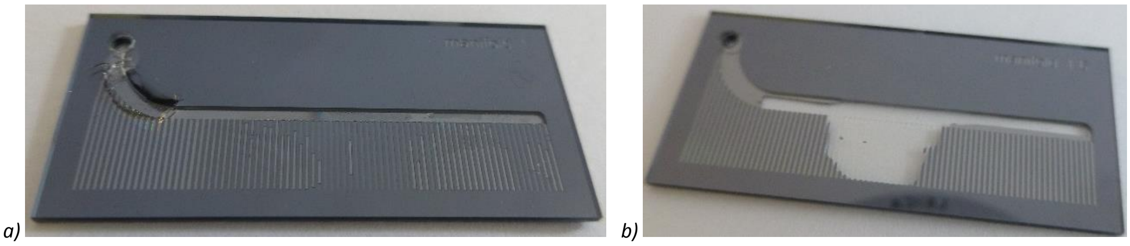


Figure 3.20: Two tested NA62 manifold chips with fracture on the Pyrex side (a) and on the silicon side (b).

Also for the LHCb experiment multi-channel test structures have been fabricated by the LETI company in Grenoble [53]. The test samples are fabricated in order to understand the best design suitable for the first micro-channel cooling prototype for the VELO upgrade. In *Figure 3.21* it is possible to see the four sample designs used for the tests. The parameters that change from one design to the other are the channels width, the walls width between one channel and the other and the distribution manifold. The samples have an inlet hole followed by small restriction channels becoming larger at halfway and ending in a recollection manifold. In one of the four designs the channels are ending without the manifold (*Figure 3.21 d*).

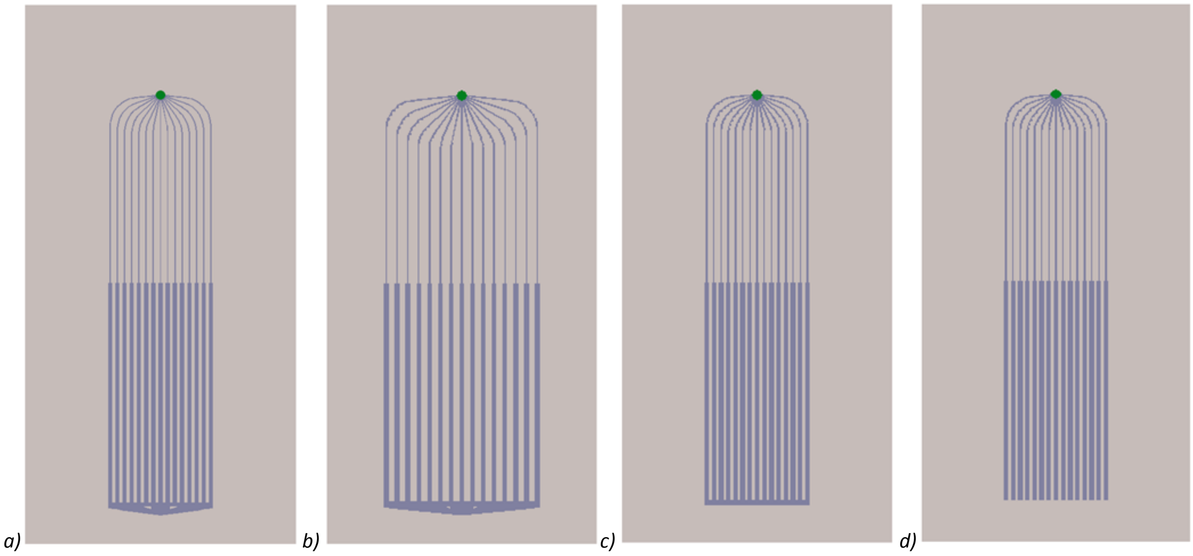


Figure 3.21: Four designs of the multi-channel test devices for LHCb micro-channel cooling.

The fabricated samples are made in silicon-silicon using the hydrophilic or hydrophobic bonding. As already discussed in *Chapter 2*, the hydrophilic bonding is easier to obtain in terms of fabrication process. However the mechanical strength of the two bonding processes is also different and the hydrophobic bond is stronger than the hydrophilic one. From the tests results it is evident this difference in the bond strength. From the pressure point of view, the maximum pressure that a hydrophobic samples is holding, is more than three times the one a hydrophilic sample holds with the same channel design. For the channels designs in *Figure 3.21 a* and in *Figure 3.21 b*, with the two big manifolds, the mean rupture pressures for the hydrophobic and hydrophilic samples are respectively 250 bar and 75 bar. For the other channels design with the small manifold (*Figure 3.21 c*) the average maximum pressure for the hydrophilic sample was 220 bar while the hydrophobic samples were tested until the pump limit to 700 bar without any rupture. The same behaviour occurred for the hydrophobic test device without manifold (*Figure 3.21 d*) while for the hydrophilic one the maximum mean rupture pressure was of 400 bar.

Also from the fractures modes a difference could be observed between the hydrophilic and the hydrophobic samples. The hydrophilic ones often presented un-bonded areas at the interface between the two wafers and this can explain the lower rupture pressure. *Figure 3.22* reports two microscope pictures of the manifold of the channel design in *Figure 3.21 a*. The microscope pictures show the broken area after the pressure tests. In the hydrophobic sample (*Figure 3.22 a)* it is possible to notice how all the fracture planes are inside the silicon structure, while in the hydrophilic sample (*Figure 3.22 b*) shiny and clear areas are visible at the interface between the two wafers. The un-bonded areas lead to a bigger surface stressed by the pressure that results in a lower rupture pressure for the samples.

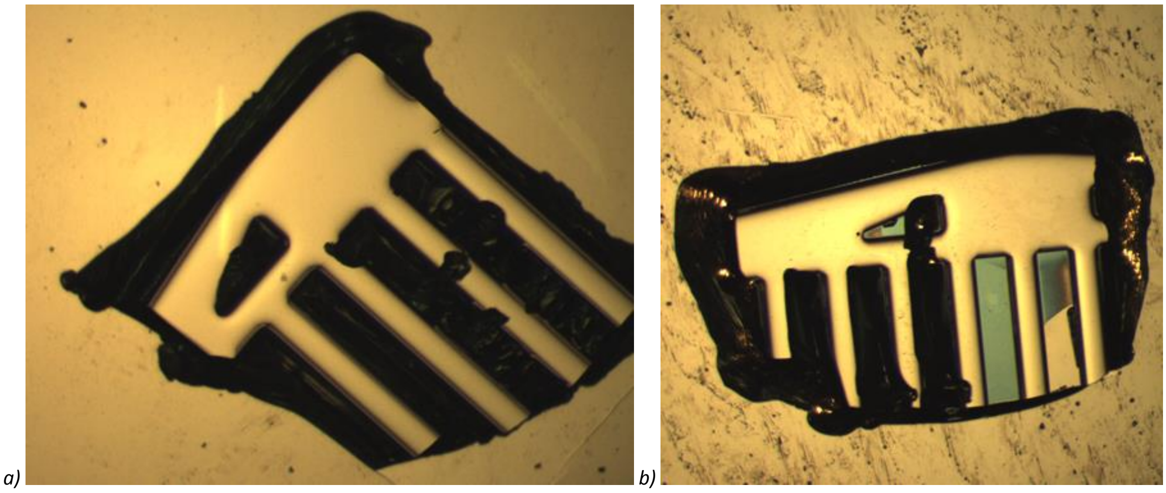


Figure 3.22: Tested hydrophobic (a) and hydrophilic (b) samples done by the LETI company.

3.5 CIRCULATING TEST DEVICES

Sometimes it is easier and cheaper to perform a pressure test on an existing device fabricated for fluidic tests, sealing one of the two holes and injecting the pressure through the other one until the sample rupture. In this way the information about the maximum pressure resistance will be very precise since the pressure test channels design is the same as the circulating device.

In the examples here described of circulating samples used for pressure testing purposes, the micro-channels devices are fabricated for CO_2 two-phase flow. The maximum pressure of CO_2 at ambient temperature is around 65 bar, considering a small safety factor a pressure of at least 80 bar has to be hold by the samples.

An example of circulating devices used for pressure test are the ATLAS micro-channel devices fabricated by the CSEM company in Neuchatel [45]. The samples are used both for pressure tests and for fluidic tests. For the pressure tests, a silicon piece is glued on one of the two holes and pressure is applied using demineralized water as testing fluid trough the other hole. The channel design is shown in *Figure 3.23 a*: the inlet hole is connected to several small capillaries that lead to bigger straight channels, which end in the recollection manifold with the outlet hole. In the recollection manifold several silicon pillars are foreseen to strengthen the large area; the pillars are in fact increasing the bonding surface between the two wafers, increasing also the mechanical strength of the device. Since gluing the silicon piece to seal one of the two inlets is adding mechanical support to the structure, the silicon piece is glued on the inlet hole being the stronger part between the two. In this way the outlet region, that is the weakest area of the device, is not influenced by any external help and the measure in pressure is not faked. In *Figure 3.23 b* is shown the sample after the pressure test with the glued silicon piece on the inlet part and the broken area in the outlet region.

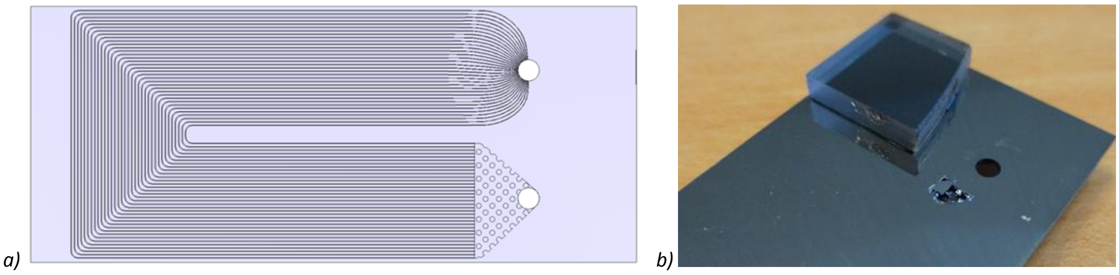


Figure 3.23: Channel design (a) and tested sample picture (b) of the CSEM samples done for the ATLAS experiment.

Also for the NA62 frame micro-channel solution, silicon-silicon circulating devices fabricated by CSEM were tested in pressure. The channels design is really similar to the ATLAS one with restrictions at the inlet, bigger straight channels and manifold with pillars and an outlet hole at the end (*Figure 3.24 a*). Also for the NA62 devices the silicon sealing piece is glued on the inlet hole and the samples are tested with demineralized water. In *Figure 3.24 b* the outlet manifold with the broken area above the pillars is shown, it the channels design of *Figure 3.24 a* is possible to see with the red circle the area in which the silicon broke.

Figure 3.24: Channel design with broken area in red (a) and tested sample picture (b) of the CSEM samples done for the NA62 experiment.

In the ATLAS and in the NA62 designs, the outlet manifold has a very similar geometry with the same pillars diameter and pitch. The maximum pressure in both cases, with a silicon thickness of around 100 µm, was more than 80 bar, value sufficient to hold the CO_2 pressure at ambient temperature.
SEM images were taken of the broken areas and it is possible to observe how the fracture planes are not at the interface between the two wafers but, they are occurring inside the silicon material on top of the pillars (*Figure 3.25*) showing a very good bonding quality.

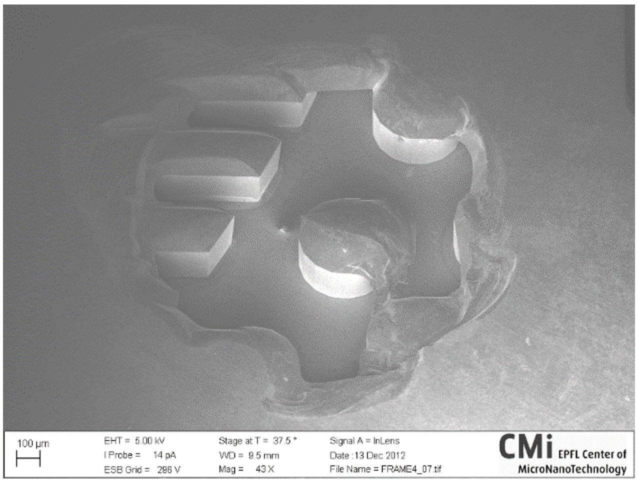


Figure 3.25: SEM image of the broken area with pillar of the CSEM sample done for the ATLAS experiment.

4 FLUIDIC AND THERMAL TESTS

In this chapter the micro-channels are presented from the thermal and fluidic point of view. Thermal and fluid-circulation tests are performed for the physics experiments to validate the micro-channel designs. The performances of each design are evaluated and studied.

As previously discussed (*Chapter 1*), a silicon tracker detector needs an efficient thermal management system to remove the heat generated by the electronics. This task becomes even more demanding during the detector lifetime, when the heat production can be increased by the leakage current becoming higher with the irradiation of the detectors. For the micro-channel cooling system the heat transfer is based on the heat conduction inside the silicon of the micro-channel plate and on the forced convection of the fluid circulating inside the channels. As discussed in *Chapter 2*, silicon is a material with high thermal conductivity and it guarantees indeed a fast and efficient heat transfer between the heat source and the heat sink. The forced convection of the cooling fluid operates to guarantee a target fluid temperature on the detector surface, being controlled by an external cooling plant. The flow inside the channels can be single-phase, or a more efficient evaporative cooling depending on the experiment requirements.

After the micro-fabrication of the test devices, the micro-channels are brought at CERN for testing. The prototypes require a testing phase to validate the channel design and to evaluate the cooling performances. For testing purposes, in order to simulate the heating power of the electronics, a mock-up heater is glued on the micro-channel surface. The mock-up heaters are powered to different power levels to check the full cooling performances of the micro-channels. Before doing the thermal tests, the devices are always tested from the fluidic point of view. The selected fluid is circulated in the channels at different pressures and temperatures to validate mechanically the device. Most of the tests performed at CERN inside the PH-DT laboratory, use C_6F_{14} liquid flow and CO_2 evaporating flow. Other micro-channel devices, like the ones made for the ALICE experiment, are circulating C_4F_{10} in two-phase flow.

Studying the cooling system from a fluid-dynamics and thermal exchange point of view, brings naturally to investigate more in the flow and heat transfer topics available in literature in the micro-channels field. Since the CO_2 evaporative flow is not well studied in literature, while it presents several advantages to be used in a micro-channel cooling system, a test camping is being conducted to study in detail the behaviour of CO_2 in micro-channels and mainly in two-phase flow. A CO_2 circulating station in Manchester University is used to test micro-channel devices and to conduct evaporative studies in mini-pipes.

4.1 NA62 GTK LIQUID C_6F_{14} FLOW

NA62 was the first experiment investigating the possibility to use a micro-channel cooling system for the thermal management of its three GTK stations [21]. The NA62 structure is the one of a fix target experiment, where the detectors are placed in line one after the other following the particle track. The NA62 objective is to measure a rare decay of kaon particles. The particle are colliding on a fix target and they are decaying in the following 270 m while crossing the detectors in the line (*Figure 4.1*). The GTK stations are placed at the beginning of the decay region and they measure the momentum, the velocity and the angle of the incoming particles.

The three GTK detectors are placed in three different vacuum vessels along the beam line. The GTK detectors work in a high radiation environment and, since they are at the very beginning of the experiment detectors chain, they need to influence as less as possible the particle tracks. The electronics of the detector is characterized by very fast read-out chips that require a good and reliable thermal management. Each detector, with the cooling system and the electronics is foreseen to work 6 months inside the experiment and then to be replaced by a new module due to the high radiation damage on the detector internal structure.

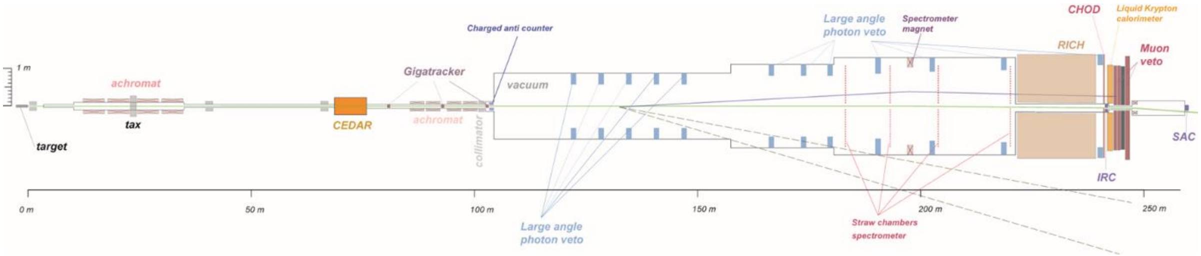


Figure 4.1: NA62 detectors structure along the beam line.

Each one of the three GTK detector stations consist of a 63x29 mm^2 200 µm thick silicon sensor bump-bonded to 10 read-out chips, 100 µm thick and 12x20 mm^2 in size. The sensor is placed in the centre of the vacuum vessel, perpendicular to the particle beam. The chips are bonded to it and they precede the sensor in the beamline. The sensor and electronics are mounted on a PCB placed at the centre of the vacuum vessel. In *Figure 4.2 a* it is possible to see a scheme of the sensor and the read-out chips in the GTK structure. The sensor is the sensitive area of the detector and therefore the material crossed by the particles has to be minimized below it. The read-out chip structure is divided into two areas: an analog area where the pixel matrix is, located below the sensor, and a digital area with the end of column (EoC), standing outside the sensor area on the sides (*Figure 4.2 b*). The two different areas are producing different power densities: in a nominal condition the analog part has a power density of 0.4 W/cm^2, while the digital area produces 2.46 W/cm^2. In addition to the nominal values, a maximum power condition is provided by the experiment, in which the analog and digital parts are producing 0.55 W/cm^2 and 3.17 W/cm^2 respectively.

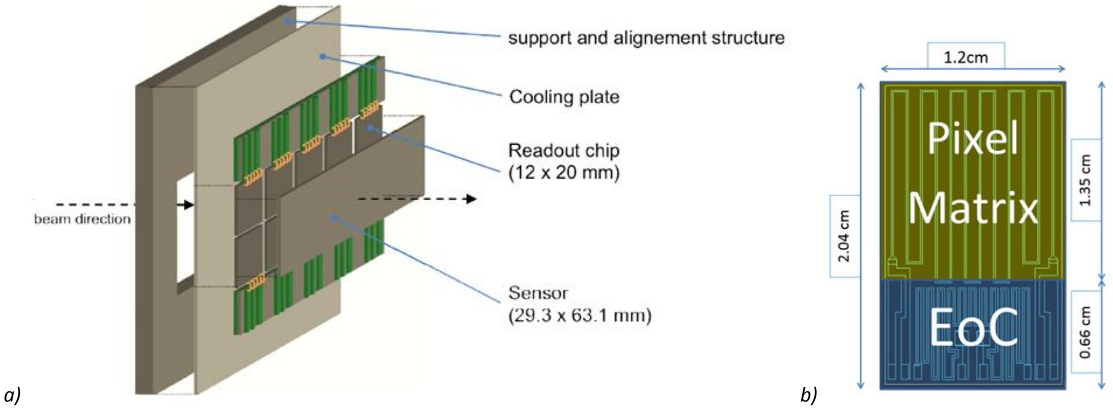


Figure 4.2: GTK detector structure (a) and read-out chip areas (b).

Starting from 2011 [7], several simulations and analytical calculations were performed to finalize the micro-channel design. Since the first ANSYS parametric model, several versions were designed, fabricated and tested. In some cases the fabricated devices were made on purpose only to perform structural tests increasing the internal pressure up to the sample rupture to evaluate the mechanical strength of the channels design. Following this iterative process, the channels have been designed, fabricated and tested in order to obtain a nearly optimal mechanical design.

In parallel, thermo-hydraulic simulations were executed to define a starting range of parameters for the geometry of the micro-channels. The computational fluid dynamics (CFD) calculations were performed using the C_6F_{14} fluid in single phase liquid flow. This flourocarbon fluid is well known at CERN and it is used since many years as cooling fluid in several other physic experiments [54], [55]. It presents a good radiation resistance as well as thermal and chemical stability. It is also non-flammable, non-toxic, electrically insulator and it guarantees low temperature in liquid flow at ambient pressure. The NA62 requirements impose to keep the GTK detectors at temperature below -20°C with a maximum thermal gradient over the sensor area of 5°C.

Based on the results of the CFD and FEM simulations, the final micro-channel design, the "baseline" design, is composed by two parallel fluidic circuits with 77 channels each. The channels have a cross section of 200x70 μm^2 separated by walls of 200 µm, and they are 45 mm long. At the entrance of each fluidic circuit, a distribution manifold, 1.6 mm wide and 280 µm deep, guarantees a uniform fluid distribution in the channels. At the end of the circuit another recollection manifold is present before the exit of the fluid trough the outlet aperture. The micro-channel plate is a 480 µm thick silicon wafer with a localized thinning in the central part, corresponding to the sensor sensitive area, where the thickness is reduced to 130 µm. The thinning is performed on the two sides of the silicon plate, leaving 30 µm of silicon above and below the channels. The thinning is made by wet etching with KOH acid (see *Chapter 2*) leaving two "pools" on the two sides of the device. The detector is glued in the centre of the front pool with a thin polymeric interface. The distribute micro-channels geometry under the detector allows to have a large thermal exchange area. This aspect provides a freedom in choosing the polymeric interface for connecting the detector to the cooling plate. The thin nature of the interface and the excellent thermal exchange between the two surfaces, are largely enough to fulfil the thermal requirements. In *Figure 4.3* it is shown a scheme of the micro-channel plate with the channels design, on which are represented the areas of the front pool (in green), the 10 read-out chips with the digital part sticking out from the sensor area (in yellow) and the silicon sensor (in orange).

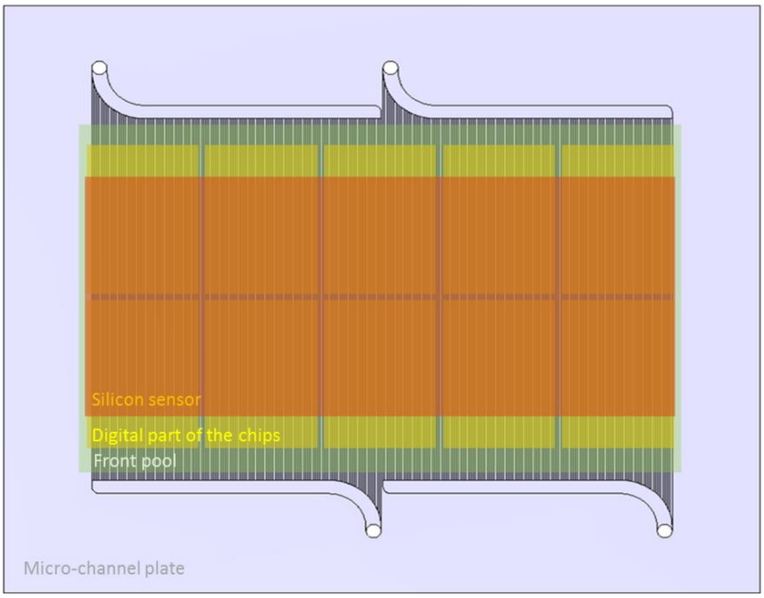


Figure 4.3: Scheme of NA62 micro-channel plate with silicon sensor and read-out chips.

Fluidic tests have been performed on a micro-channel plate with this design. In *Figure 4.4* the pressure drop between the inlet and the outlet of the device is reported for different values of the mass flow rate. In the cooling plant two pressure sensors are mounted on the tubes next to the inlet of the micro-channels and next to the outlet, but there is still a small part of capillary going from the pressure sensor up to the fluidic connector glued on the silicon surface. For this reason a preliminary calibration is operated connecting the two capillaries of the inlet and of the outlet without any micro-channel device. The pressure drop calculated without micro-channels is then subtracted to the measured one on the circuit with the micro-channels, producing a “corrected” value of the pressure drop. In *Figure 4.4* the measured pressure drop is plotted together with the corrected pressure drop after the subtraction of the calculated one from the calibration.

The pressure drop inside the micro-channel is not high and it confirms the simulations previously done.

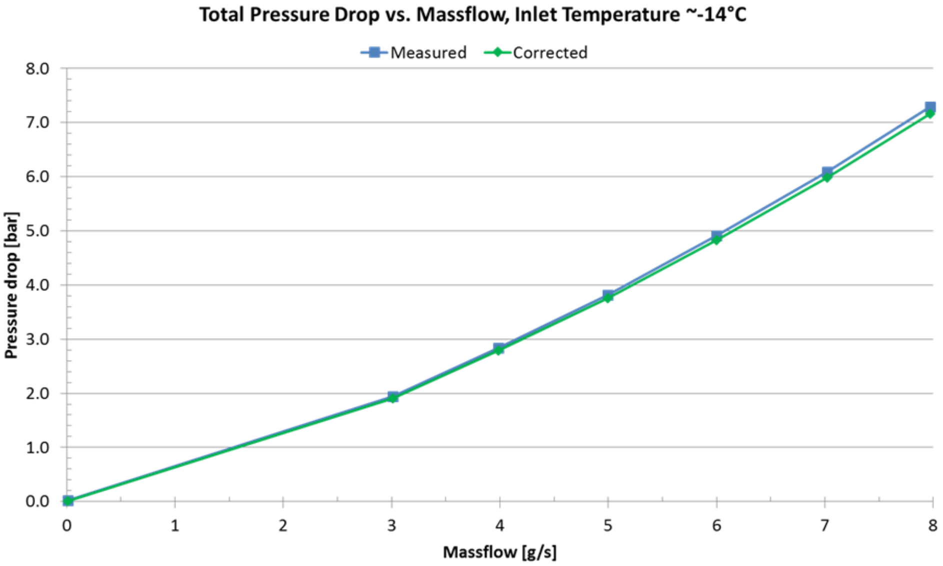
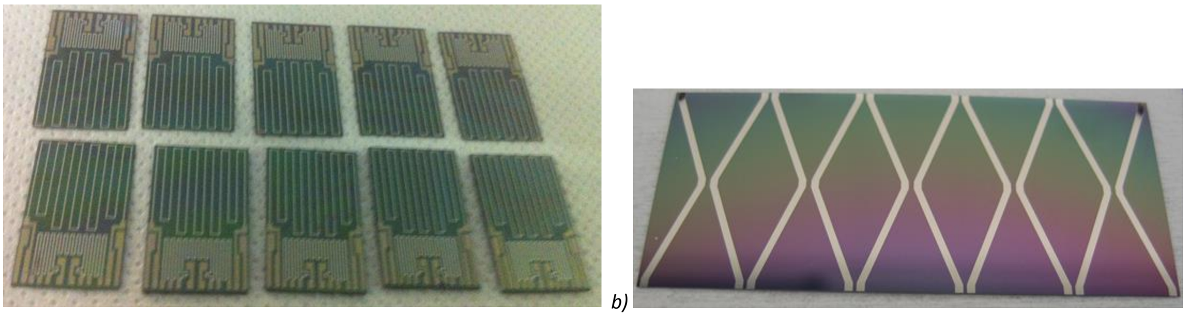


Figure 4.4: Mass flow versus pressure drop in the NA62 micro-channel device.

For validating the channel design from the thermal point of view, without gluing the real detector on the micro-channel plate, a silicon heater is used to simulate the power. The silicon heater consists of 10 silicon chips with metal lines deposited on top to represent the read-out chips and a larger silicon element that simulates the sensor with no heat production. The metal lines deposited on top of the chips are connected to a power supply and they can reproduce the exact power density as the real read-out chips. The micro-fabrication of the silicon heaters has been the result of a collaboration between CERN, EPFL and CSEM. The chip metal lines are deposited in such a way that it is possible to power the two different areas with different power densities. On the sensor surface metal lines are deposited to connect temperature sensors glued on top of the surface, so that it is possible to measure directly the sensor surface temperature to evaluate the cooling efficiency. In *Figure 4.5* the 10 heaters chips (*Figure 4.5 a*) and the silicon sensor (*Figure 4.5 b*) are shown. Also on the digital area of the chip two lines are foreseen to power a temperature sensor glued on the chip surface. In this way on the full assembly 15 temperature sensors are available.



a) b)

Figure 4.5: Heater chips (a) and heater sensor (b) to simulate the power of the real detector.

The 10 chips are glued to the silicon sensor with an adhesive tape using a special mechanical jig that guarantees the good alignment between them respecting the real detector dimensions and constraints (see *Chapter 5*). Also the thicknesses of the heaters are the same as the real detectors, meaning a thickness of 200 µm for the sensor and 100 µm for the chips. In this way the thermal path in the testing device is kept as similar as possible to the real case. The full heater assembly looks like in *Figure 4.6*, where the sensor is glued on top of the analog part of the chips and where it is possible to see the 15 temperature sensors, in blue, glued on the silicon surface.

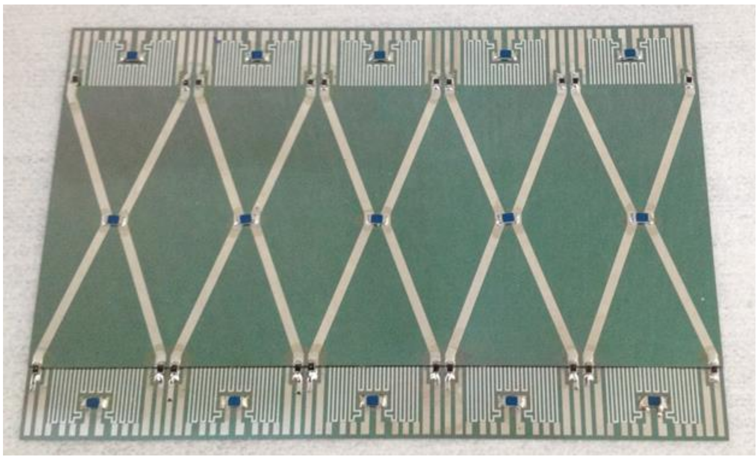


Figure 4.6: Full heater assembly to simulate the heat produced by the GTK detector.

The heater assembly is glued inside the front pool of the micro-channels plate and the metallic lines of the heaters are powered trough kapton extender cables bonded on the two sides. The kapton extenders are then connected, with an electric connector and a cable, to the power supply and to the read-out system for the temperature sensors located outside the vacuum vessel.

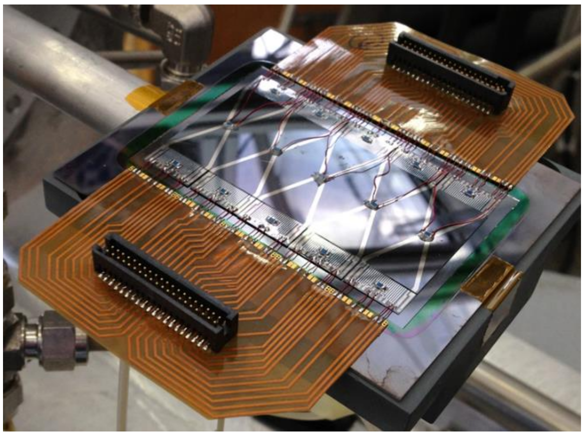


Figure 4.7: NA62 micro-channels device with heater glued on top and kapton extenders.

On the heater surface there are 15 temperature sensors that can be divided in three areas: those from number 1 to number 5 are located in the top digital area of the chips, numbers from 6 to 10 are in the central area over the sensor and the analog part of the chips, while numbers from 11 to 15 are in the bottom digital part of the chips. The two fluidic circuits with the 77 channels per circuit, can be circulated in counter flow or in parallel flow. The two inlets and two outlets of the circuit are disposed like in the scheme of *Figure 4.3*, and four fluidic connectors are glued on the silicon surface on top of the 1.6 mm diameter holes. According to how the fluidic tubes, coming from the cooling plant, are connected a parallel flow can be obtained in the channels by entering in both the top holes and exiting in both the bottom holes. Instead if a circuit is entered in the top hole and the other one in the bottom one, a counter flow is achieved below the sensor surface. In *Figure 4.8* is possible to see a representation of the three heater zones with the temperature sensors numbers and with an indication of the counter flow circulation.

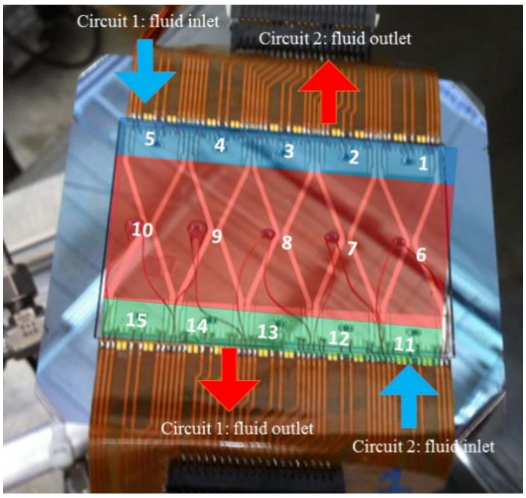


Figure 4.8: Temperature sensor names and positions, and fluid circulation in counter flow.

Thermal tests are run with this counter flow in the channels. The graph in *Figure 4.9* shows the temperature profiles along the three heater zones. The results shown are related to tests performed with a liquid C_6F_{14} flow with a mass flow rate of 8 g/s and an inlet fluid temperature of -23°C. The measures start with no power applied on the heater and continue with an increasing power. The first data are taken with half the nominal power of the detector (red line in *Figure 4.9 a, b, c*) so with 10 W, on the two digital parts (5W in top part and 5W in the bottom one), and 1.5 W on the analog part.

The green line is related to the nominal power condition for the NA62 experiment, where 20 W are dissipated by the digital parts and 3 W by the analog ones. Two additional power configurations have been evaluated to take into account the worse conditions for the NA62 detector. The two graphs for the digital zones (top and bottom, *Figure 4.9 a, c*) indicate an increase of temperature corresponding to the outside manifold where the fluid is recollected. The central analog zone presents instead a uniform temperature distribution showing less than 1°C of thermal gradient on the sensor surface.

Regarding the detector requirements: the thermal gradient on the detector surface is largely fulfilled, the sensor temperature instead is guaranteed by increasing the mass flow to 10 g/s during the operation in the experiment or decreasing the fluid inlet temperature. Unfortunately the cooling plant used for the tests is not powerful enough to provide more than 8 g/s and a fluid inlet temperature colder than -23°C. Further tests have been done to verify the thermal gradient on the detector surface also in parallel flow, and no significant difference is observed. The final solution installed in the experiment presents the parallel flow for an easier access with the tubes suppling the cooling fluid.

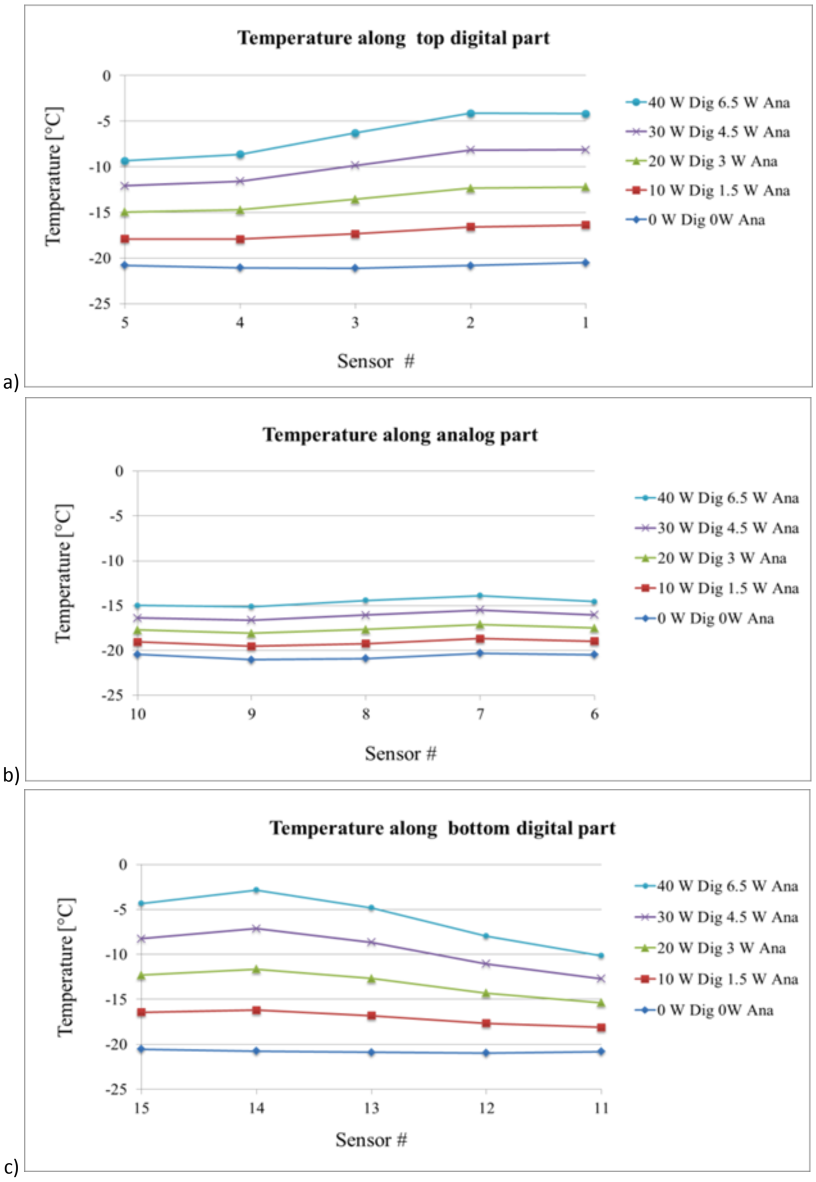


Figure 4.9: Thermal profile on the detector mock-up surface versus temperature sensor numbers: top digital part (a), central analog area (b) and bottom digital part (c).

Since the zones dissipating more power are the two digital zones of the chips, and since the material has to be minimized below the detector area, a second micro-channel design has been proposed. The so called “frame” solution is a rectangular silicon frame with an empty area in the centre. In the two longest sides, it has two arrays of parallel channels flowing below the digital part of the chips, while in the two short sides the frame is just bulk silicon. The proposed solution foresees to glue the lateral part of the detector assembly on the two microchannel arrays and remove directly the heat just from the digital area, counting on the conduction inside the electronics chip to remove the one produced by the analog part in the centre. A simple scheme of the micro-channel design is available in *Figure 4.10 b*, with the sensor and the read-out chips areas on top. The channels are 100 µm wide, 300 µm deep and 62 mm long, separated by walls of 50 µm. The fluidic circuit design is really simple with two distribution manifolds at the inlet and at the outlet of the channels (magnification available in *Figure 4.10 b)*. Inside the distribution manifolds short walls are designed in order to increase the mechanical resistance of the device to internal pressure (see *3*).

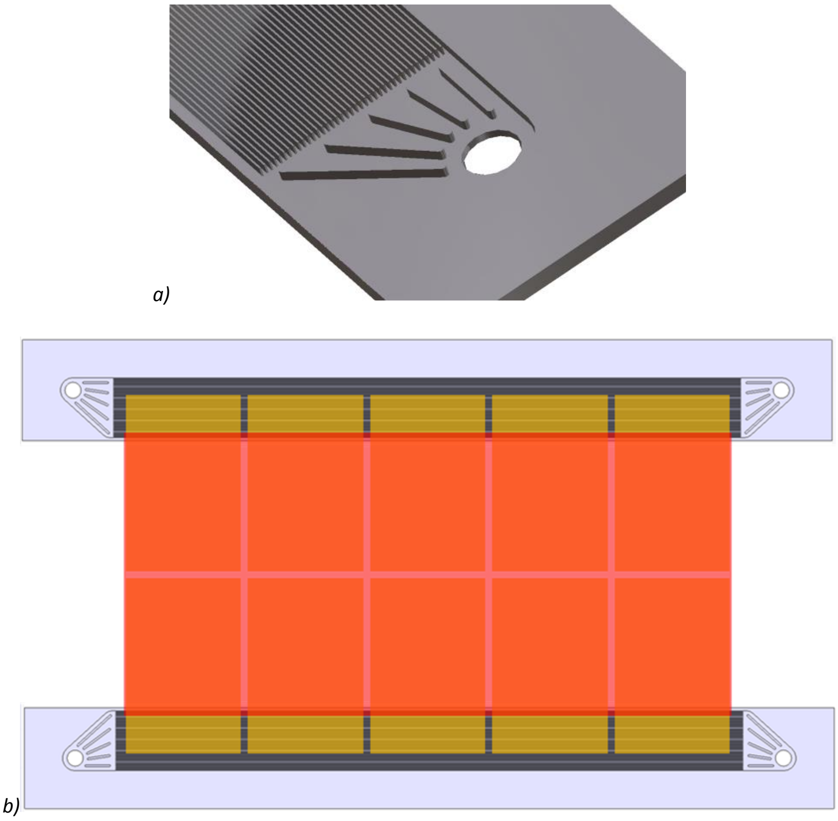


Figure 4.10: Frame design proposed for the GTK cooling.

In order to simplify the fabrication process, the two bars with the channels arrays are fabricated detached and then two small silicon bars are glued between them on the two sides. A picture of the so assembled frame design can be seen in *Figure 4.11 a*. Thermal tests have been conducted also with this design and the same thermal mock-ups have been used also in this case, in *Figure 4.11 b* is shown a picture of the frame with fluidic connectors glued on top, the thermal heater and one side of the kapton extender.

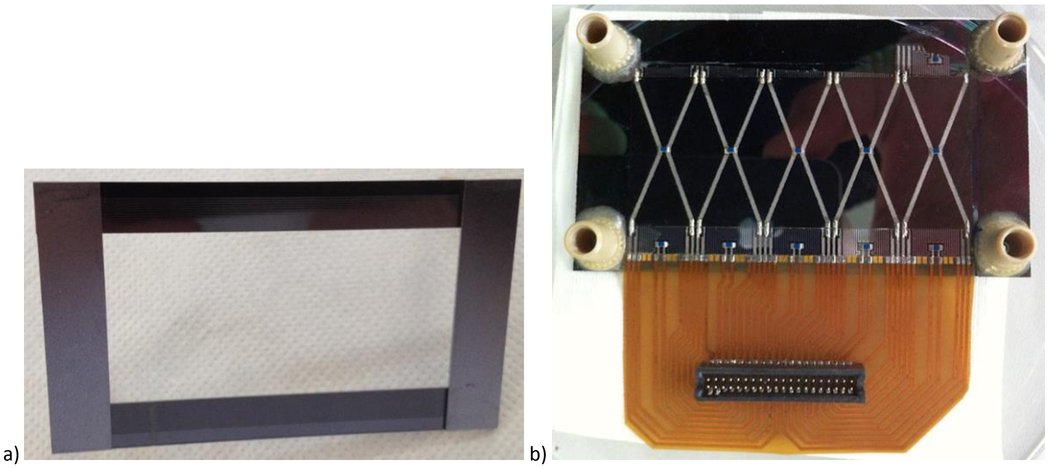


Figure 4.11: Frame micro-channel design (a) with heater glued on top with a Kapton extender already connected (b).

A comparison between the two designs proposed can be drawn by taking thermal pictures of the two micro-channel plates with the heaters on top with an Infra-Red (IR) camera. The baseline design tested for this study, presents a parallel flow from the bottom to the top in the thermal pictures. The frame design instead has a flow from right to left in the top channels array and a flow from left to right in the bottom array to uniform the temperature over the sensor area. The thermal pictures are taken outside the vacuum vessel and therefore the test have been executed at ambient temperature to avoid ice and condensation on the two prototypes. The fluid inlet temperature is around 15°C. Unfortunately 3 heaters on the frame design were not working during the test for electrical problems. In *Figure 4.12* it is possible to see the thermal pictures of the baseline design (*Figure 4.12 a*) and of the frame design (*Figure 4.12 c*) taken with nominal power conditions. The blue arrows in the pictures indicate the flow direction in the two cases, while the three red rectangles in *Figure 4.12 c* indicate the three faulty heaters of the mock-up mounted on the frame design. As it can be seen by the temperature legend, in nominal power conditions, the sensors area of the frame design has a warmer temperature with respect to the baseline solution. Since the channels are covering the whole detector area in the baseline solution the hottest points are the digital areas of the chips that produce more heat. The difference in temperature between the colder bottom digital areas and the warmer top ones is due to the flow direction; the flow arrives to the top digital areas after having crossed the whole plate and therefore warmer than in the bottom line. In the frame design, since the channels are present just below the digital areas of the chip, the warmer zone is the central sensor area not directly cooled by the channels but cooled trough conduction in the silicon sensors and chips.

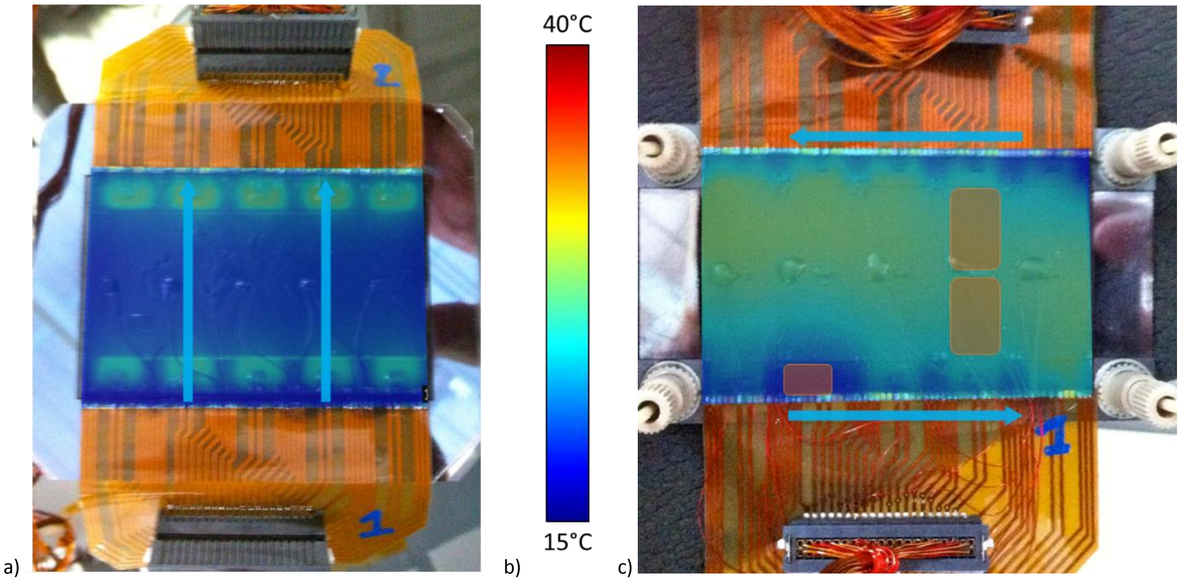
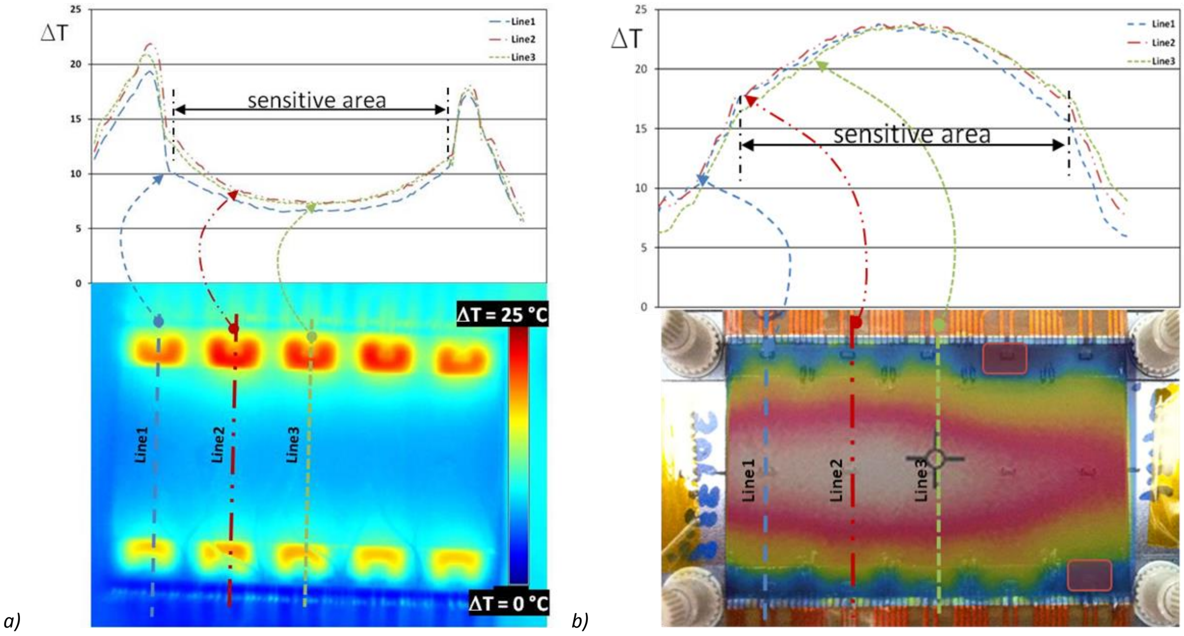


Figure 4.12: Thermal picture comparison in nominal power conditions: baseline design (a), temperature legend (b) and frame design (c).

If the power is increased up to the maximum values, the temperature difference between the areas is even more emphasized. The thermal pictures are in this case taken on a frame device on which a different thermal mock-up was mounted, where 2 digital parts of two chips were not working. In the graphs above the thermal pictures in *Figure 4.13*, the temperature profiles in the cross sections (lines 1, 2 and 3 in the pictures) are plotted for the two cases, the baseline (*Figure 4.13 a*) and the frame (*Figure 4.13 b*) design. The temperature profiles show the temperature difference between the detector surface and the cooling fluid. In this extreme scenario of maximum power conditions, in the baseline solution a maximum temperature difference of 6 °C over the sensor area is reported. In the frame solution instead, inside the sensitive area, the temperature difference is more than 8°C.

After a complete series of tests, it was evident how the frame solution respects the experiment requirements only when the read-out chips are thick enough to have a high heat transfer, as soon as the chips are 100 µm thick or less the frame solution is not working anymore. Since the selected electronics chips are 100 µm thick, the frame solution has not been selected as solution for cooling the experiment but it is kept as back up plane in case the chips thickness or the detectors requirements will change.



a) b)

Figure 4.13: Temperature difference between the detector surface and the fluid in maximum power conditions for the baseline (a) and for the frame (b) design.

4.2 ALICE C_4F_{10} EVAPORATIVE FLOW

A very similar configuration to the one of the frame design for the NA62 experiment, is adopted for the ALICE micro-channel frame design for the upgrade of the ALICE ITS detector. The ALICE frame design presents two arrays of micro-channels on the long sides of the rectangular frame and two distribution manifolds in the short sides of the frame. Contrary to the frame proposed for NA62, the frame is not assembled by gluing separate pieces, but it is fabricated in one piece with the central window empty. The stronger constrain of the ALICE detector is in fact the reduction of the material crossed by the particles in the sensitive area. Other requirements, for this detector operated at room temperature, are a maximum working temperature of 30°C and a maximum thermal gradient over the detector area of 5°C. The nominal power the detector is foreseen to produce is 0.3 W/cm^2.

A research group at CERN [20] performed thermal test to verify the thermal performances of the proposed micro-channel frame. The device used during the tests, has been fabricated inside the EPFL CMi cleanroom from a 380 µm thick silicon wafer bonded to a 525 µm thick Pyrex wafer (*Figure 4.14*). The channels are etched in the silicon by 200 µm (*Figure 4.15 a*) and they are four on each side, 60 mm long and 200 µm wide separated by 300 µm walls. At both ends two distribution/recollection manifolds are present with internal walls to rigidify the silicon structure in this region (*Figure 4.15 b*).

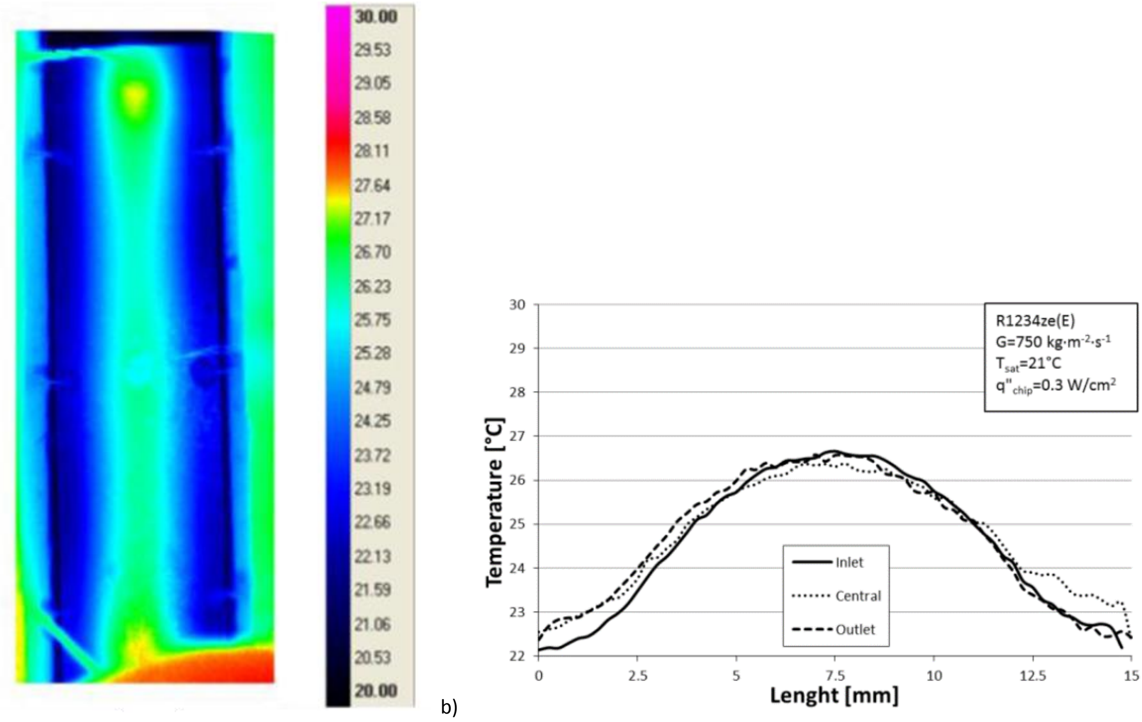
Figure 4.14: ALICE frame design with central window to reduce the material crossed by particles (Ref. [20]).

a) b)

Figure 4.15: ALICE micro-channel frame design (a) with the magnification of the distribution manifold (b).

To perform thermal tests a silicon heater has been glued on the micro-channel plate to simulate the heat dissipated by the detector. The heater is a 100 µm thick silicon chip with 20 nm of titanium and 200 nm of platinum deposited on top. On the platinum surface two wires are soldered and connected to a power supply. The tests are performed using C_4F_{10}, fluid already used for the cooling of the ALICE detector [25], in evaporative flow. Reversed flow phenomena and other pressure instabilities have been sometimes reported in literature for evaporative flows in multiple parallel channels at the micro-scale [56], [57]. For this reason, channels restrictions have been introduce at the inlet of the channels by decreasing the width of the channels in half.

A thermal picture is done (*Figure 4.16 a*) on the device circulating a mass flux of 750 kg/m^{2}s, and with an inlet fluid temperature of 21 °C. The temperature variation along the channels is less than 1°C. Three temperature profiles are taken in cross direction to the channels, at the inlet, at the centre and at the outlet of the device to verify the temperature gradient in this direction. The three lines (*Figure 4.16 b*) are showing a maximum temperature difference of 4 °C and a maximum temperature of 26.5 °C on the sensor area. These results largely fulfil the experiment requirements.



a) b)

Figure 4.16: Thermal picture for the micro-channel frame in nominal power conditions (a) and temperature profiles over the detector area (b) (Ref. [20]).

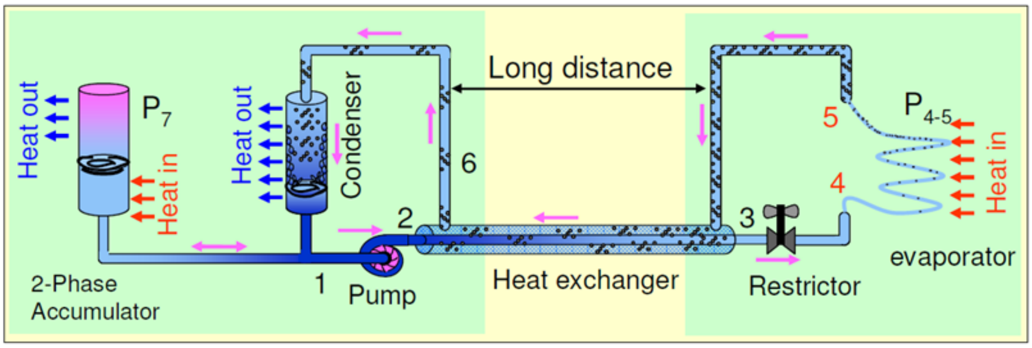
4.3 CO_2 EVAPORATIVE FLOW

CO_2 is gaining more and more interest in cooling of particle detectors [58], [59]. In the last years, CO_2 evaporative cooling systems are replacing the previous cooling systems of tracking detectors in several experiment at CERN [60]. It is well known that evaporative cooling is more efficient in terms of heat transfer than single phase, and this can be an advantage in decreasing the mass of the cooling systems following the physics requirements of minimize the material in the particle tracks. The flow needed to cool the same amount of power in two-phase flow is smaller than the one needed for single-phase flows, and the diameter of the tube bringing the flow can be indeed reduced. Furthermore, during evaporation the temperature of the refrigerant remains constant and this greatly reduces the temperature gradients along the detector.

The choice of CO_2 as cooling fluid is mainly advantageous for its excellent heat transfer capability and its low density, which allows for even smaller pipes. CO_2 is also radiation hard like the other fluorocarbon fluids already presented but it is cheaper than flourocarbon fluids and it is more environment friendly. In addition CO_2 is a high pressure fluid that allows for working with large pressure drops in the cooling system. This means that CO_2 can be used in really small tubes without problems of pressure losses and, on the other hand, with high thermal properties. Due to these favourable characteristics, CO_2 has been therefore studied for applications in micro-channels cooling systems [61].

The micro-channel cooling systems circulating CO_2 in two-phase flow, currently developed at CERN, use a cooling principle based on the two phase accumulator controlled loop (2PACL) successfully applied for the first time for the cooling of the LHCb VELO detector and for the Alpha Magnetic Spectrometer (AMS) silicon tracker detector [62]. The 2PACL is a mechanically pumped two phase closed loop where vapour CO_2 is condensed in a cold radiator (*Figure 4.17 a*). The evaporative pressure, and therefore the evaporative temperature in the micro-channel system (P_{4-5} in *Figure 4.17 a, b*), is controlled by a two-phase accumulator. The accumulator, mounted in parallel to the circuit, contains by design liquid and vapour CO_2. The pump is working with sub-cooled liquid and it brings the CO_2 from state 1 to state 2 in the pressure/enthalpy graph of *Figure 4.17 b.* Between 2 and 3 heat is exchanged in the heat exchanger with the outlet of the system between state 5 and 6. Thanks to the presence of a restriction (capillary or calibrated orifice), a liquid expansion takes place between 3 and 4 ending with saturated liquid at the entrance of the micro-channel evaporator. The heat exchange inside the detector, removing the heat produced by the electronics, takes place between states 4 and 5. In state 5 the vapour quality is still low and usually there is still liquid in the system. Heat is exchanged with the inlet fluid between 5 and 6, and the condenser finally brings back the fluid to the initial conditions.

This system is very advantageous since it allows for a complete passive evaporation, and no active elements (heaters or actuators) are needed inside the detector volume, which is usually characterized by a very difficult or impossible accessibility.

a)


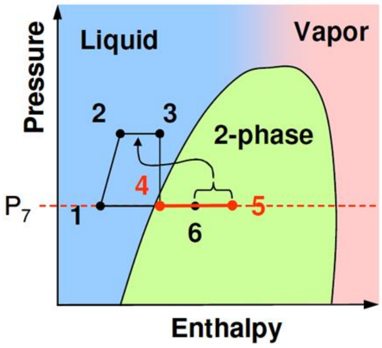
b)


Figure 4.17: Two-phase cooling system principle used at CERN: scheme (a) and pressure/enthalpy graph (b) (Ref. [62]).

4.3.1 ATLAS FEI4 Cooling with CO_2 Evaporative Flow

A similar 2PACL has been used to provide the CO_2 flow to the micro-channel cooling system developed in the frame of a study for the ATLAS FEI4 chip. The FEI4 chip is used in the IBL tracking detector of the ATLAS experiment: it is 2x2 cm^2 and it is foreseen to dissipate a power of 0.376 W/cm^2. The detector requirements are to keep the sensor surface at a temperature below -15°C.

A first micro-channel prototype has been produced inside the EPFL CMi cleanroom with a 525 µm thick silicon wafer bonded to a 2 mm thick Pyrex wafer. The prototype has 35 micro-channels, 50 µm deep, 50 µm wide separated by walls of 200 µm, that do a U-turn in the device bringing side by side the inlet and outlet apertures. As usual in the outlet manifolds several pillars are designed to strengthen the silicon structure in that large area. At the beginning of the fluidic circuit, inlet capillaries, 20 µm wide, are acting as restrictions to bring CO_2 in critical conditions at the entrance of the larger channels. A scheme and a picture of the prototype are available in *Figure 4.18 a* and *Figure 4.18 b* respectively.

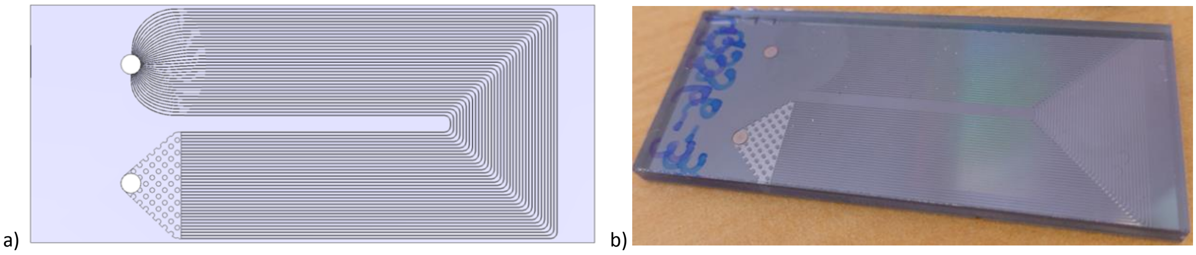

a) b)

Figure 4.18: Scheme (a) and picture (b) of the first ATLAS micro-channel design.

In order to simulate the heat produced by the FEI4 chip, a silicon heater is glued on the silicon side (*Figure 4.19 a*). The heater is a 100 µm thick silicon chip with 20 nm of titanium and 200 nm of gold deposited on top. Two wires, connected to a power supply, are soldered on the heater surface to provide the power needed. In order to check the temperature on the surface of the sensor mock-up and on critical points of the device, PT100 temperature sensors are glued on the prototype. In *Figure 4.19 b* a scheme of the PT100s position is shown. Tests have been conducted with a two-phase CO_2 flow of 0.25 g/s. The inlet temperature measured on the inlet tube was -2°C for all power levels; a lower inlet temperature was avoided to prevent ice formation on the wafer surface since the measurements were done outside vacuum. The graph shown in *Figure 4.20*, shows the temperature measurements of the PT100s on the device surface. At the nominal power level (1.5 W on the chip surface), the temperature on the sensor surface is always lower than the fluid inlet temperature showing an evaporation in the channels below the sensor. The very large temperature drop measured along the microchannel is an indication of an excessive mass flow rate causing an excessive pressure drop. Unfortunately, for this very preliminary test it was impossible to further decrease the mass flow rate below the value of 0.25 g/s. However, the temperatures have a stable behaviour even with double power in the heater. This means that by doing the test under vacuum, lowering the inlet temperature, the detector requirements would be easily satisfied.

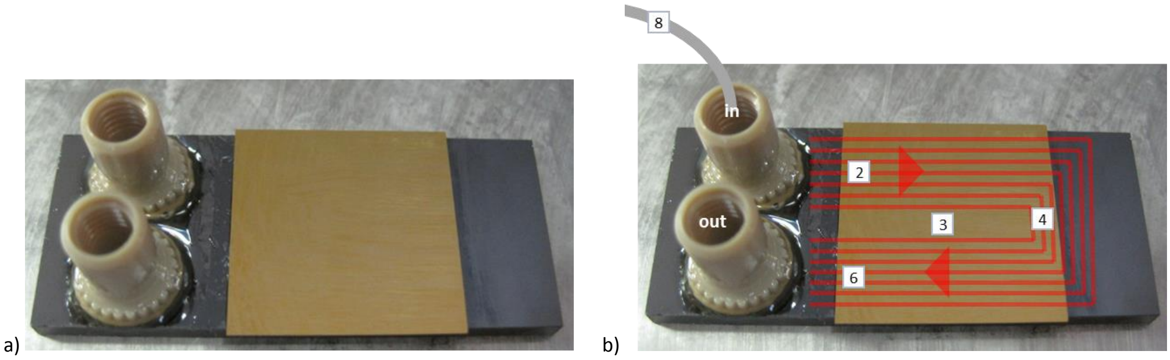


Figure 4.19: Heater glued on the first micro-channel device (a) and PT100s positions (b).

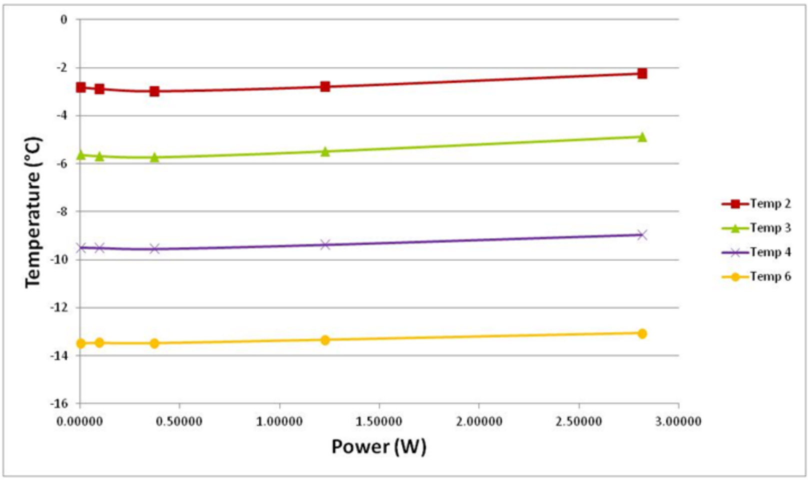


Figure 4.20: Temperature measurement of the PT100 glued on the prototype surface.

A second preliminary test that confirms the data presented in *Figure 4.20* was done by taking thermal pictures on a similar micro-channel device with a heater glued on top. In order to perform thermal pictures on silicon the device surface has to be painted in black to avoid reflections induced by the silicon reflective surface. The thermal pictures were taken in atmosphere without a proper insulation so the silicon surface was covered with ice as can be seen in the standard pictures shown below the thermal pictures in *Figure 4.21*. The temperature legend is available in *Figure 4.21 a*, and the fluid inlet temperature is 7 °C. With 0 power the detector surface is uniformly cooled around -10°C (*Figure 4.21 b*), increasing the power to the nominal power of the FEI4 chip (1.5 W) is not visibly influencing the temperature of the sensor (*Figure 4.21 c*). The power level that increases the temperature of the sensor surface in a significant way is at 36 W, about 24 times the nominal value of the chip poor consumption (*Figure 4.21 d*): the heater surface starts indeed to be hot around the two wires soldered on it. The detector temperature increase can also be noticed by the ice on the sensor surface that is slowly starting to melt.

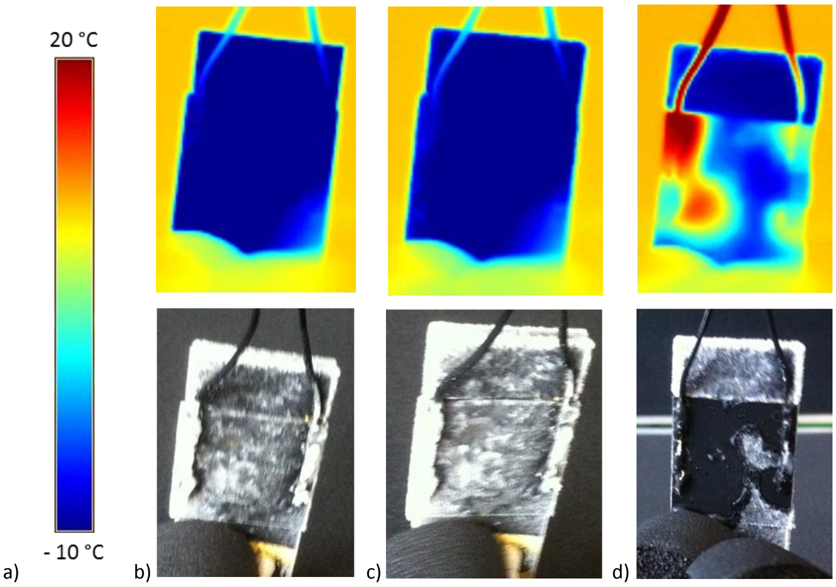


Figure 4.21: Temperature legend (a), and thermal pictures with 0 power (b), nominal power (c) and 36 W (d) applied on the heater.

After these preliminary tests, a first full silicon device was fabricated inside the CMi cleanroom and a real FEI4 chip was glued on top. The full silicon micro-channel plate has 35 channels, 50 µm wide and 190 µm deep, etched in the 380 µm thick bottom wafer. The top wafer, bonded to the first one by the CSEM company, is also 380 µm thick. No thinning has been performed on this device, because the minimization of the material was not the goal of this specific investigation. The micro-channel plate has been glued on a PCB card and the FEI4 chip has been glued on top of it. The chip is connected to the card trough wire-bonding performed by the PH-DT bonding lab. In the picture in *Figure 4.22 a* it is possible to see the micro-channel plate, in dark grey, glued on the PCB, with the FEI4 chip, in white, glued on top. The wire-bonding is performed on the front side of the chip to the gold pads on the PCB. In the picture it is also possible to notice the PT100 temperature sensors glued on top of the micro-channels device to measure its temperature in different points. The scheme of *Figure 4.22 b* shows the identification numbers of the PT100 and theirs position with respect to the chip (in red in the picture). The sensors number 5 and 6 are glued on the Kovar fluidic connectors, while number 7, 8, 3, 4 are glued directly on the silicon surface. Number 1 and 2 are glued on the back on the device, below the chip area, on the silicon surface. Two independent temperature sensors measure the inlet tube temperature inside the vacuum vessel before the inlet of the channels (In2 and In1 in *Figure 4.22 b*). In addition to these ones there are two pressure sensors outside the vacuum vessel to measure the pressure on the fluid in the inlet and the outlet tubes.

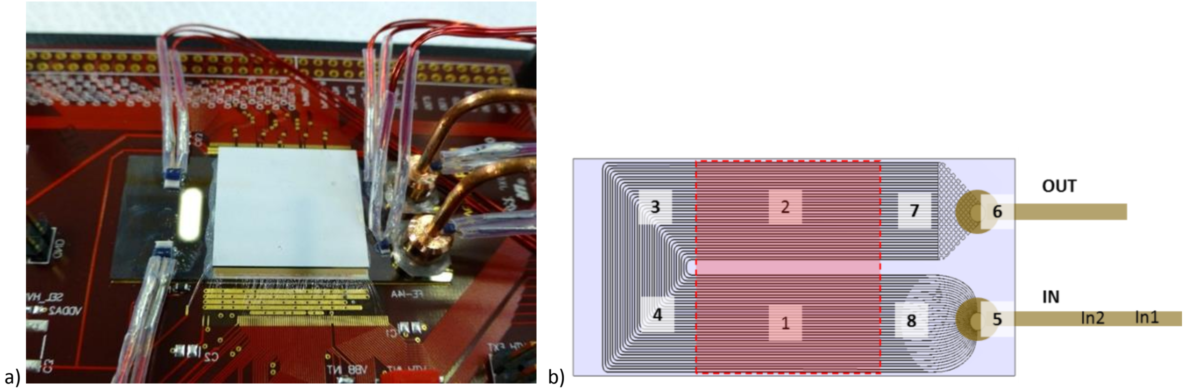


Figure 4.22: Micro-channel plate glued on the PCB with the FEI4 on top wire-bonded to the card (a) and PT100s position on the device (b).

A very first test was done at ambient temperature of 24 °C, without refrigerant in the tubes, switching on the chip at its nominal power. In the graph of *Figure 4.23*, the profiles of the temperature sensors of the system are plotted in time. The sensors In1 and In2 are not influenced by the chip power since they are measuring the tubes temperature and the cooling is off. All the other temperature sensors are influenced by the chip power and they measure a progressive increase of temperature even if they are not directly on top of the sensor, as an effect of the good thermal conductivity of silicon. The small decrease of temperature right after the switching on of the chip is due to electrical currents influencing the PT100s readings, and to instabilities at the starting of the chip. When the chip reaches a stable condition, producing the nominal power of 1.5 W, the micro-channel plate temperature starts to increase quickly reaching temperatures above 30 °C in few minutes.

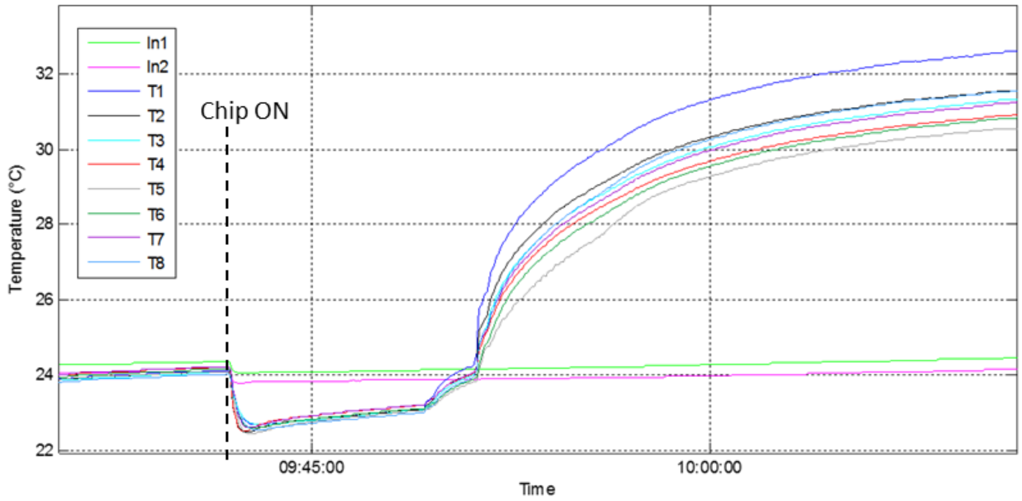


Figure 4.23: Switching on the FEI4 without cooling, ambient temperature 24 °C.

The same test was repeated with the refrigerant circulating in the device at low temperature: the temperature set on the CO_2 cooling unit was at -25°C, resulting in an average temperature on the chip surface of -23°C. When the temperature sensors were stable, the chip was switched on and the temperatures profiles observed (*Figure 4.24*). The chip was switched on at 11.57 and no temperature changes are evident in the graph. This behaviour underlines the very efficient power of this micro-channel design.

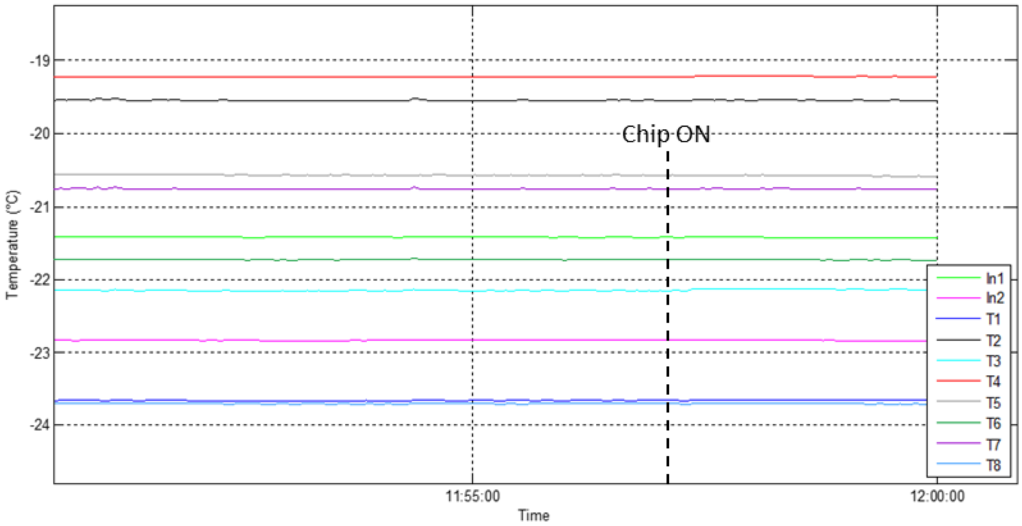


Figure 4.24: Switching on the FEI4 with cooling at -25°C.

All these measurements are taking into account the PT100s values measured next to the chip on the micro-channel surface. In order to know the exact sensor temperature it would be necessary a temperature measurement directly on the sensor surface. Due to future tests with particle beams, requiring a fully functional detector, planned to be done with the same prototype, gluing another temperature sensor on the detector surface is totally forbidden. For the same reason, painting in black the detector surface to take thermal images of the assembly is also not feasible. An alternative proposed way of appreciating the sensor surface temperature without measuring it directly, is to calculate is from the bias current of the sensor.

The bias voltage of the silicon sensor of the FEI4 chip is the voltage necessary to the sensor to work properly. The corresponding current is varying with the sensor temperature and a specific relationship is connecting the two values. By calibrating the silicon sensor knowing the specific temperature of the vessel and of the micro-channels, and reading the corresponding bias current, a calibration table can be associated to the sensor in order to infer the sensor temperature from the value the current in each moment.

To start the sensor calibration, standard IV curves are programmed on the sensor control program to repeat them at each temperature. The programmed IV curve starts from 0 V and arrives up to -50 V decreasing of 2 V every 5 seconds. The corresponding current is measured in the meanwhile. An example of the resulting curve is shown in *Figure 4.25 a*. During the IV curve the electronic chip is off to avoid thermal production that could disturb the calibration. During the IV curve the temperature sensors inside the vacuum vessel are monitored and their signals are plotted to evaluate the temperature stability during the curve (*Figure 4.25 b*).

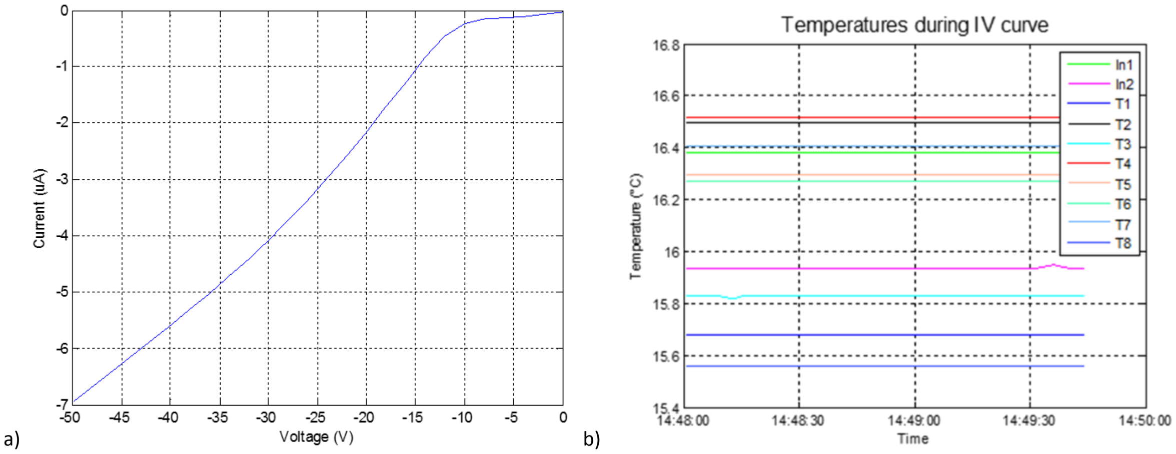


Figure 4.25: Example of IV curve of the sensor (a) and temperature measurements during the curve (b).

The temperatures measured during the IV curve are taken as reference temperatures to calculate the sensor temperature. Since the tests are done under vacuum and the electronic chip is off, it is possible to assume without a large error that the average of the temperatures measured by the PT100's corresponds to sensor temperature during the curve. Further research is still needed to understand better the best correspondence between the temperature and the current.

The calibration tests are done spanning the temperatures from ambient value to -25 °C. In *Figure 4.26* it is possible to see a series of calibration curves done starting from ambient temperature and going down until -25 °C. Between one temperature step and the following one a sufficient time (45 min at least) is left in order to do the measurements during a stable state. As it is possible to observe in the graph of *Figure 4.26*, for a fixed bias voltage, the bias current is increasing with the decreasing of temperature. Following this method, by selecting a bias voltage and reading the corresponding current, after the complete sensor calibration the sensor temperature is known.

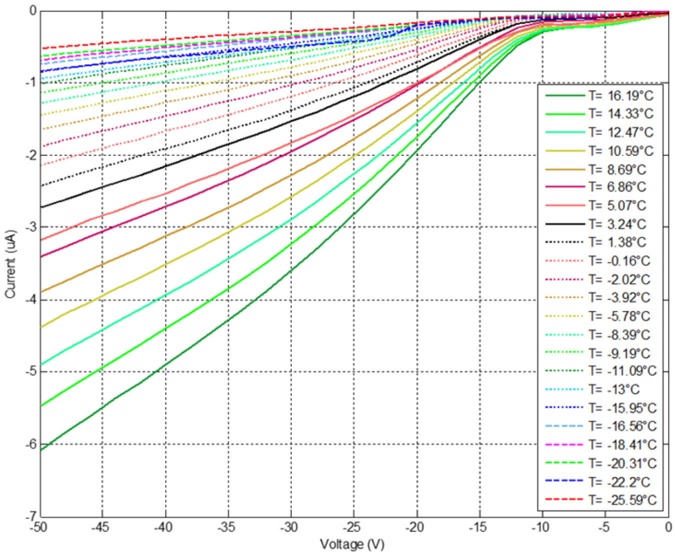


Figure 4.26: IV curves at different temperatures.

4.3.2 LHCb Velo Cooling with Evaporative CO_2 Flow

Another micro-channel project using CO_2 in two-phase flow is the LHCb Velo upgrade. For the installation of the new tracker detector, LHCb decided to base the thermal management of the silicon detectors on a full silicon micro-channel plate glued to the detectors circulating evaporative CO_2 flow [19].

For testing purposes and for validating the cooling proposal, a 40x60 mm^2 micro-channel prototype was fabricated inside the EPFL cleanroom with a silicon wafer bonded to a 2 mm thick Pyrex wafer. The micro-channels design is very similar to the one proposed for the ATLAS experiment. The inlet hole is distributing the flow in 15 restriction channels 30 µm wide and 70 µm deep. The restrictions are then leading in the bigger channels, 200 µm wide and 70 µm deep, separated by 200 µm walls. The outlet recollection manifolds is characterized by regularly arranged mechanical pillars to increase the rigidity of the structure. The scheme of the micro-channel circuit and the picture of the tested prototype are shown in *Figure 4.27 a* and in *Figure 4.27 b* respectively.

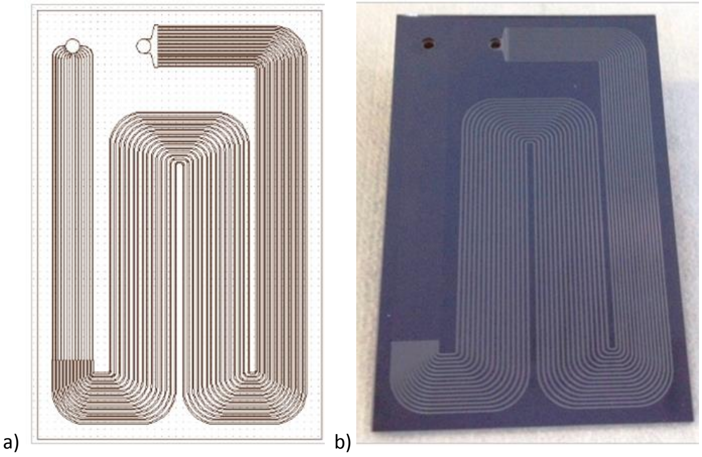


Figure 4.27: Cooling circuit (a) and micro-channel prototype in silicon-Pyrex (b).

In order to simulate during the thermal tests the power generated by the detector, silicon heaters are glued on top of the silicon micro-channel surface. The basic element of the Velo detector will be composed by 3 electronics chips and a silicon sensor bump bonded on top. The silicon dummy heaters are silicon chips with deposited on top metal lines with a specific design to reproduce the exact power distribution. A "detector module" is composed by 6 electronics chips and two silicon sensors on top of them. In *Figure 4.28 a* it is possible to see a picture of the three dummy chip heaters and of the resulting complete detector thermal mock-up. The heaters are glued on the micro-channels surface and three temperature sensors are glued on them (*Figure 4.28 b*). The heaters are glued on the silicon side of the micro-channels with a small portion (about 6 mm) cantilevered outside the micro-channels area. This is representative of the real detector design, where the silicon detector will be pushed as close as possible to the beam line and no material will be allowed below it for a width of about 6 mm, in order to avoid unwanted particle interaction. The temperature is measured in three points: the sensors labelled *uch1* and *uch2* are positioned on top of the micro-channels while the one labelled *uch3* is positioned on the hottest point of the sensor, in the cantilevered area that is not directly cooled by the channels.

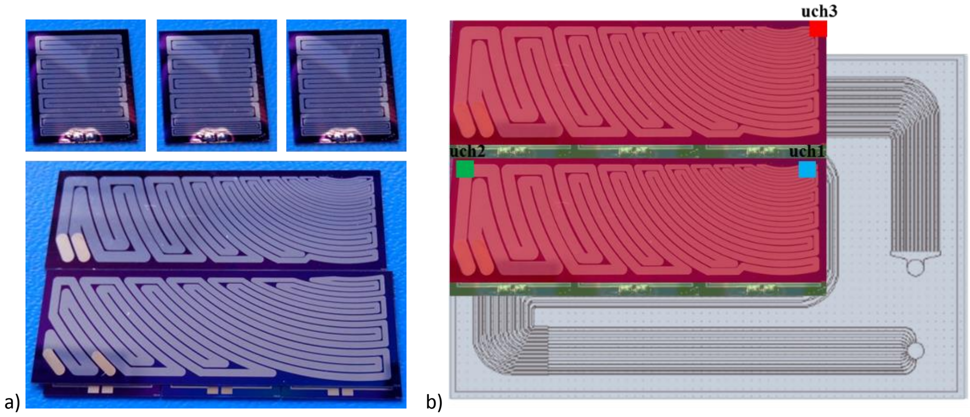


Figure 4.28: Heaters to simulate the detector power (a) and gluing position of the temperature sensors (b).

The thermal tests presented were run with an inlet CO_2 temperature of -30 °C. In *Figure 4.29* is plotted the difference between the reading of the three temperature sensors and the inlet fluid temperature, vs. the power provided to the heaters. The power of the heaters is increased slowly up to the maximum power foreseen for the VELO detector. The temperature sensors *uch1* and *uch2* are showing an almost constant behaviour, revealing the high cooling power of the micro-channel. The *uch3* sensor, glued on the tip of the heaters without direct cooling from channels below, is increasing temperature with the power until a maximum temperature difference of 7 °C. This means that an inlet fluid temperature of -30 °C is largely sufficient to keep the whole sensor surface, including the cantilevered portion, at a temperature below -20 °C as requested by the experiment.

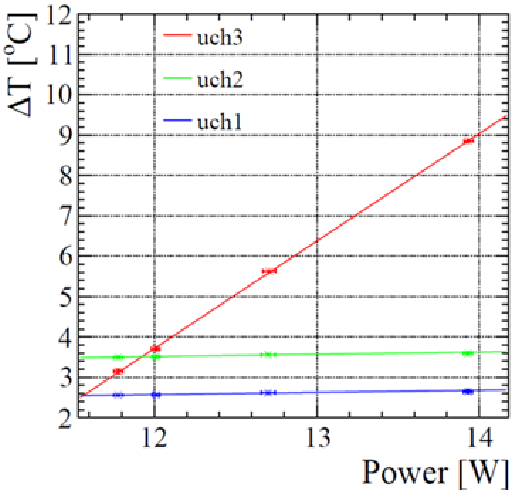


Figure 4.29: Temperature measurements for the LCHb Velo prototype.

4.4 CO_2 TWO-PHASE FLOW STUDIES

In order to fill the lack of studies on CO_2 two-phase flows in micro-channels in literature, fluidic tests in small tubes have been recently started in collaboration with the University of Manchester. The idea is to observe, with high speed cameras, and measure, with temperature and pressure sensors, the CO_2 flow in micro-tubes of simple geometry in different conditions.

To perform these tests, a CO_2 blow station is in use at the University of Manchester. The CO_2 blow station is an open loop, where the CO_2, coming from a pressurized bottle, runs in the system in two-phase or single-phase flow and then is heated up from an external heater before being discharged outside the window. A scheme of the full system is available in *Figure 4.31*.

The CO_2 bottle lies on a scale in order to monitor the amount of fluid left inside the bottle. The CO_2 inlet inside the system is controlled by an on/off valve, and is filtered right after the entrance to clean the fluid before circulating in the system. The CO_2 pressure at the entrance is monitored through a manometer and a pressure sensor. As in the 2PACL system, the fluid goes through an internal heat exchanger to reach the critical conditions at the entrance in the experiment. A needle valve regulates the flow going through the circuit before entering the experiment. The CO_2 goes through the experiment setup where usually the evaporation is targeted. After the experiment and the internal heat exchanger, the fluid is heated up by an external boiler to 40 °C in order to have warm vapour at the discharge. A pressure valve at this point in the system, controls the back pressure of the whole circuit. A mass flow meter measures the flow circulating inside the circuit; it measures the flow at the outlet, in single vapour phase, to avoid the large measurement uncertainty of taking a two-phase flow measure. The tube going to the experiment and the outlet one, are connected to a security valve to exhaust the pressure in case the maximum pressure value set for the circuit is overcome. The fluid temperature in the system is checked by temperature sensors glued on the tubes in critical positions (blue circles in the scheme of *Figure 4.31*) read by an acquisition program.

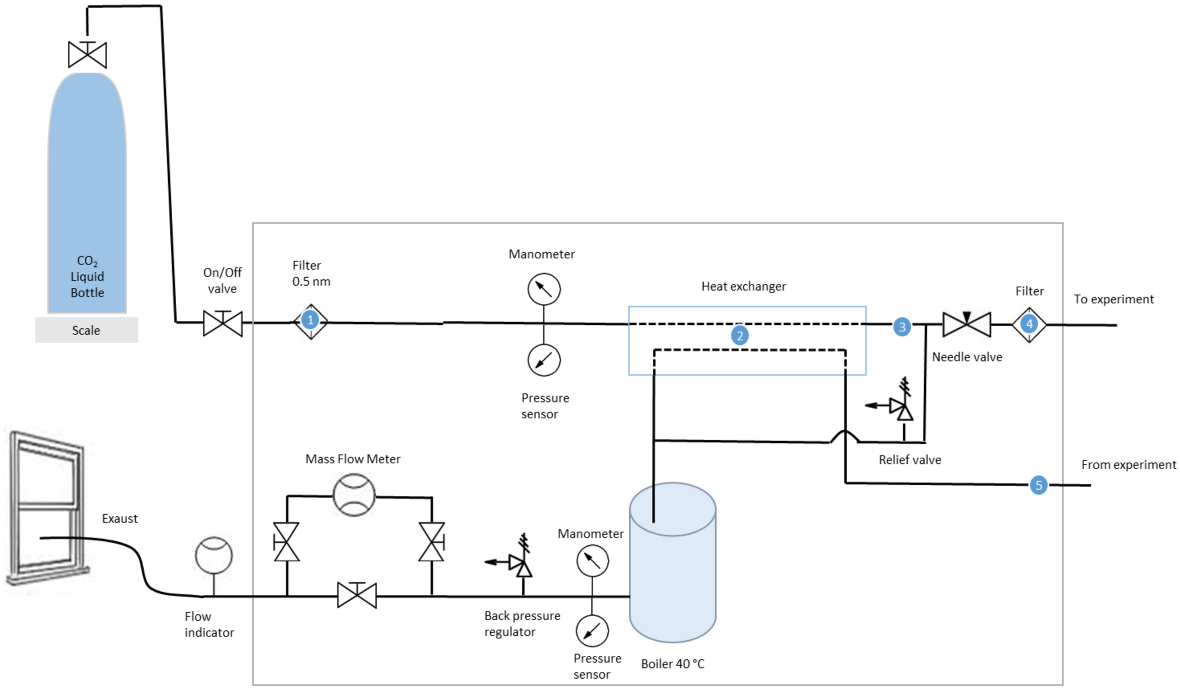


Figure 4.30: Scheme of blow station in Manchester.

The CO_2 station is essentially contained inside a closed metal box filled up with an insulation foam. The tubes going outside the insulated box, are also covered by a thermal foam to prevent temperature losses. A picture of the real system is shown in *Figure 4.31*, where it is possible to see the internal structure of the tubing inside the metal box, after the removal of the insulation foam. The whole system is built mainly with ¼'' stainless steel tubes. The internal heat exchanger of the blow station is built following the one used in the 2PACL systems where the heat is exchanged by inserting the tube going to the experiment inside the outlet one. The two tubes are then rolled together to obtain the circular spiral in central position of *Figure 4.31*.

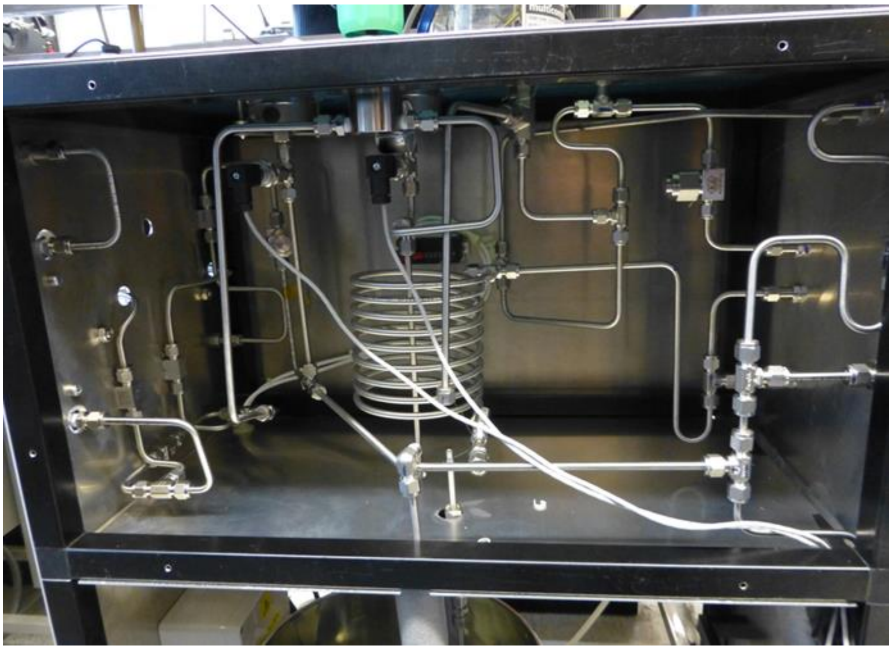


Figure 4.31: Picture of the blow station inside.

The first experimental setup is composed by a 20 cm long tube with an external diameter of 1/16'' and an internal diameter of 1 mm (*Figure 4.32*). The tube is fixed between two Swagelok cross connectors [63]. On the crosses two pressure sensors and two temperature sensors are mounted to check the fluid state at the inlet and at the outlet of the tube. Along the tube are then glued 6 thermocouples to measure the tube temperature. In order to trigger the evaporation in the system, the tube is directly heated by thermos-electric effect via two wires soldered on the edges of the tube. The picture of the real setup used during the test is shown in *Figure 4.33*, with a zoom of the tube area in *Figure 4.34*. During this first test the 6 thermocouples are glued on the tube using different thermal pastes to check the best one that could survive to the thermal gradients occurring on the tube surface.

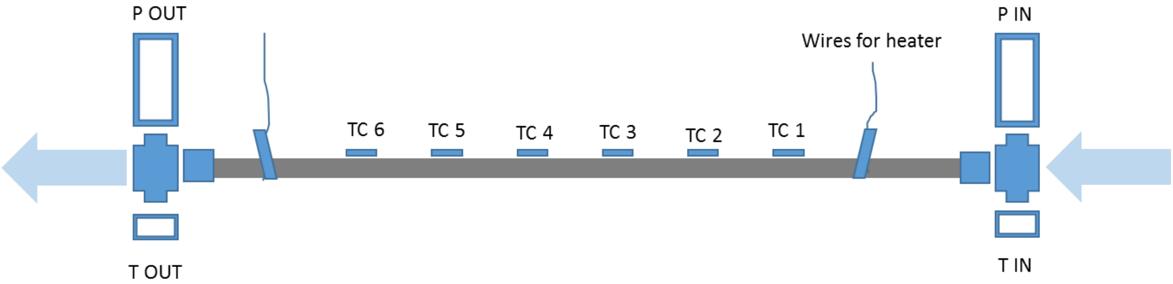


Figure 4.32: Scheme of the test stand.

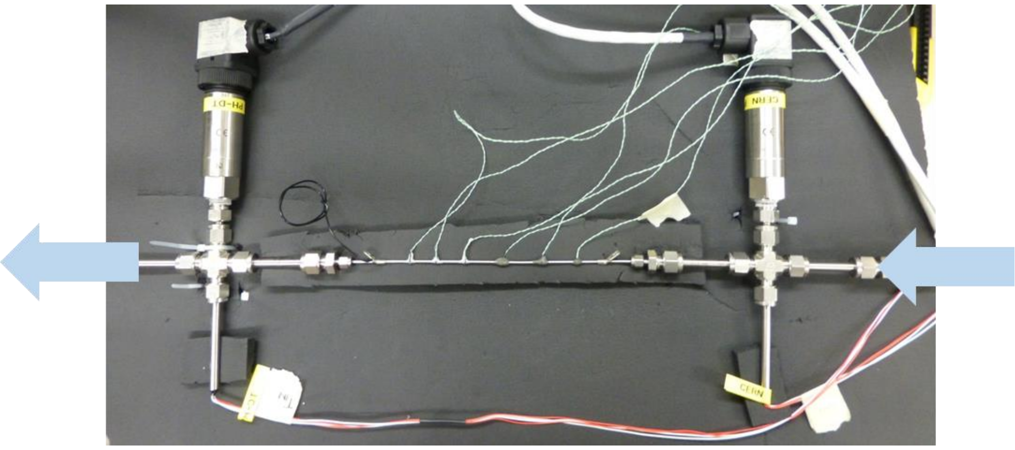


Figure 4.33: Picture of the test stand.

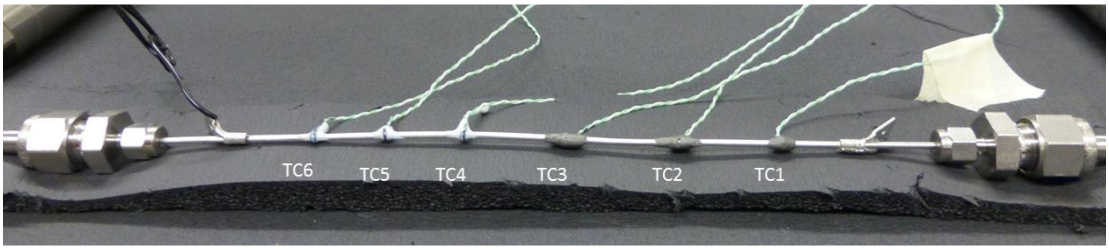


Figure 4.34: Zoom of the tube under test with thermocouples numbers.

A first test was done to test the system with high and low temperatures and pressures, and to calibrate the thermocouples. As an adequate vacuum vessel was not available for this test, the test section was fully insulated with Armaflex insulating foam during the tests to minimize the influence of the external environment. The graph showing the test done to calibrate the thermocouples is available in *Figure 4.35*. The machine is started with a back pressure set point of 12 bar. The ambient temperature, *cold junction temperature* in the graphs, is around 21°C, as well as the CO_2 inlet temperature. The CO_2 inlet pressure instead is around 59 bar, and it can be seen how, being an open circuit, the CO_2 inlet pressure is decreasing during the test done. The calibration of the thermocouples is done taking 2 minutes of data at 4 different temperature set points. The first one is at -30 °C and then the back pressure control valve is progressively closed a bit to increase the pressure and decrease the temperature. The flow is stable around 0.6 g/s, but every time the back pressure valve is turned an instability is introduced in the system and the flow is oscillating until it reaches a stable value again. The second calibration point is taken with an average temperature of -25 °C and an average pressure of 15 bar. The third point is at -20 °C and 18 bar, while the last one is at -15 °c and 21 bar.

The preliminary results on the thermocouples calibrations are shown in *Figure 4.36*, where four graphs are shown for the four calibration set points, with the 8 temperature sensors. The temperature values in green are the measured ones, while the ones in black are the temperatures calculated from the physics CO_2 state. The corrected temperature after the calibration are shown in red. The thermocouples glued on the tube surface, show an error around 0.2 °C pretty good for a two phase flow measurements.

All 6 thermocouples survived to the thermal cycles done, and all the thermal pastes used for gluing them to the tube are successfully tested.

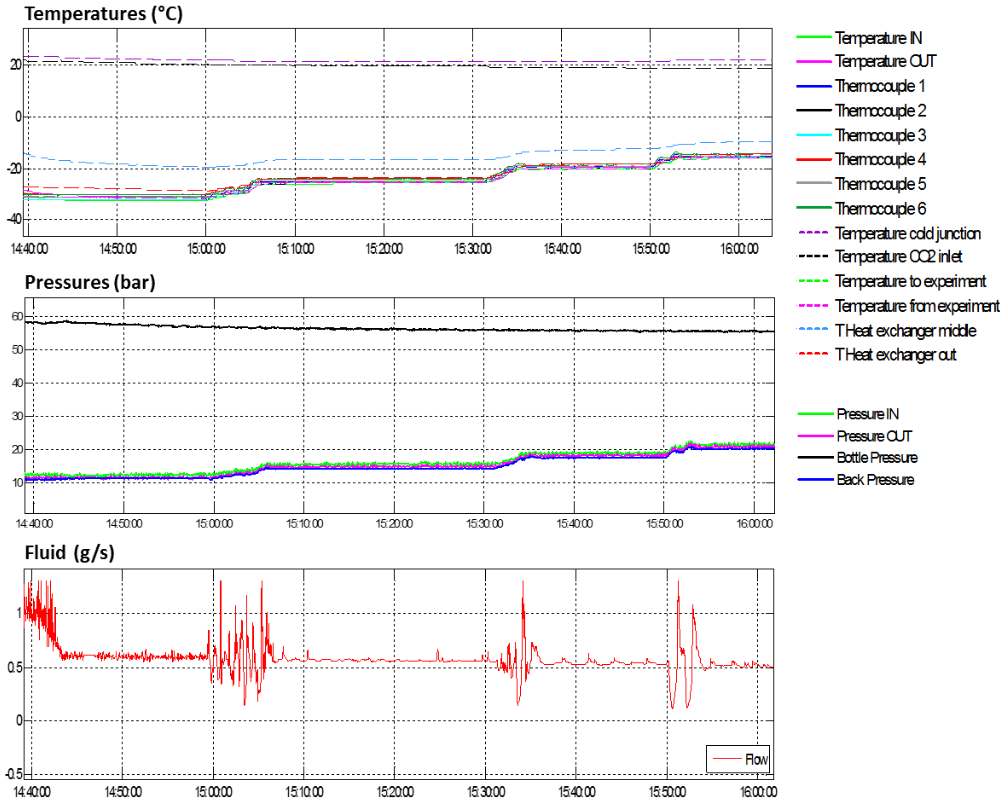


Figure 4.35: Thermal test results: calibration of the thermocouples.

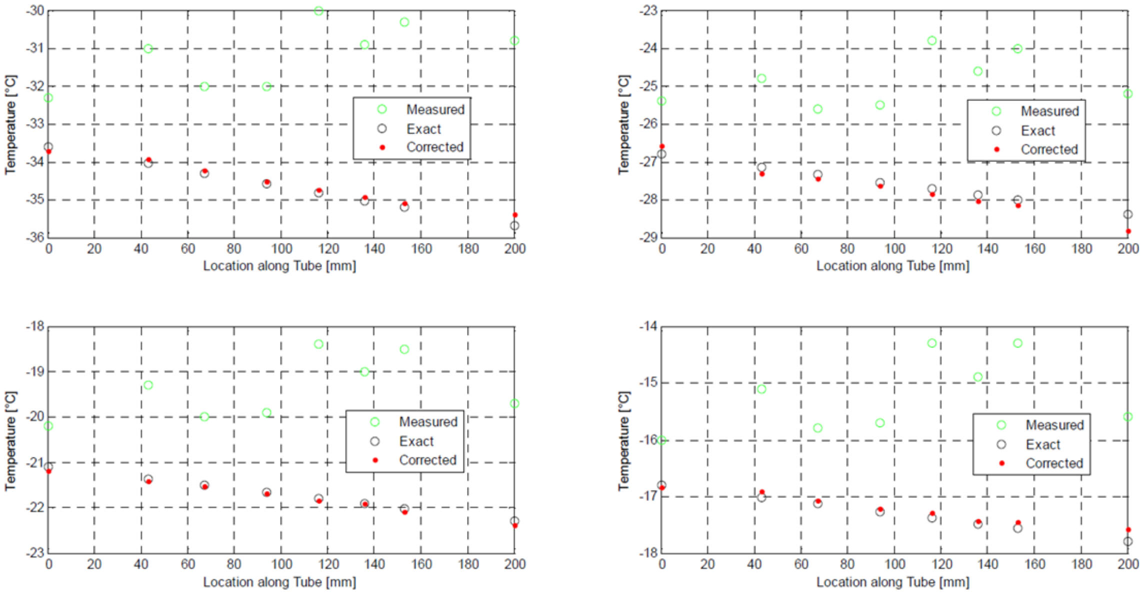


Figure 4.36: Thermocouples calibration preliminary results.

5 MICROCHANNEL DEVICE INTERFACES

After the fabrication of the micro-channels inside the cleanroom (*Chapter 2*) and the validation of the channels design from the mechanical (*Chapter 3*) and thermo-fluid dynamic point of view (*Chapter 4*), the following step is the design of the best suited hydraulic and mechanical device interfaces to ensure a reliable installation inside the detector.

A particle detector is a complex mechanical assembly where all the components need to be placed in an organized structure in order to work well and efficiently. The detectors need to cover the whole area of the incoming particle beam but also the one of the possible resulting collisions. In a colliding beams experiment the detector layers are assembled one on top of the other in a cylindrical structure surrounding the point of collision, placed at the experiment centre (Interaction Point: “IP”). The innermost layers are the tracker detectors (see Chapter 1), to whom this study is specifically addressed. In *Figure.5.1 a* is possible to see an example of a tracker for colliding beams experiment, the ALICE ITS detector, where all the sensing modules are surrounding the IP. In a fix target experiment instead the detectors are placed one after the other in a straight line beyond the particle target to detect the results of the collisions. An example for a fix target experiment is the NA62 experiment (*Figure.5.1 b*).

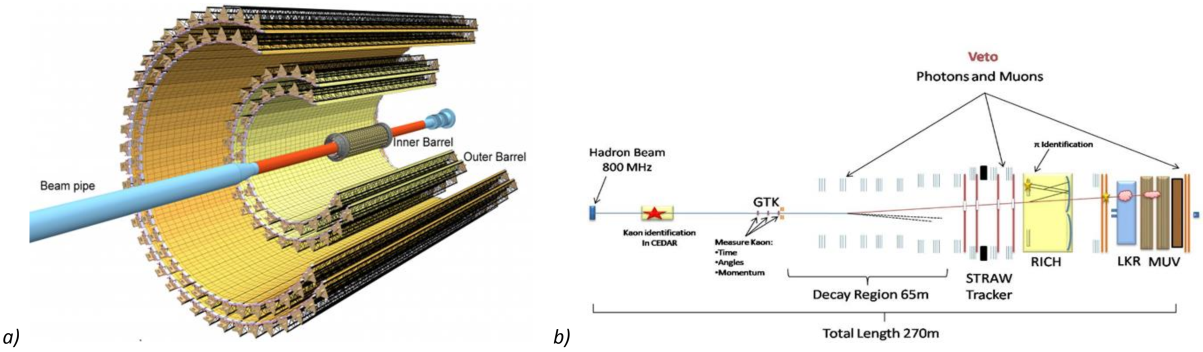


Figure.5.1: Structures of a colliding beams experiment like ALICE (a) and a fix target experiment like NA62 (b).

In addition to the detectors, there are many other components to be inserted in an experiment assembly, like the cooling pipes, the magnets, the supporting structures, the electrical and optical cables and many others. For this reason the free space inside an experiment is is reduced to a minimum.

Focusing on the mechanical structure of the tracking detectors [64], the main requirements are low mass, stability and precision. To guarantee a very precise measure, the detecting components need to be very stable, consequently the mechanical structure requires high stiffness and rigidity, contrary to the requirement of low mass. Often the mechanical structure includes also the thermal management system to dissipate the heat generated by the electronics. The low mass structures are usually associated with short thermal response time increasing the cooling efficiency, but a high thermal capacity and a low conductive resistance thermal path usually require mass addition..

Therefore the requirements of a mechanical structure for a tracking detector are in disagreement between each other, requiring a good compromise to obtain the best structure. Most of the times a significant lack of space is influencing the design of the mechanical structure and the cooling system need to be minimized or built following external constraints. However, the micro-channel silicon cooling systems, as previously discussed, guarantee a very high thermal efficiency in removing the

heat generated by the detector. In term of mechanics, its advantage relies on being a very precise full-silicon element, therefore providing a good interface for the silicon sensor, with the same CTE.
The mechanical integration of the micro-channel plate inside the detector structure starts with the choice of the best fluidic connector. The fluidic connectors are the elements providing the interface between the microscale circulation inside the device and the macroscale circulation in the pipework of the cooling system. The second step in the mechanical integration process, is gluing the detector on top of the micro-channel plate. A mechanical supporting structure is then necessary to support the micro-channels during operation in the experiment. The support needs also to provide the stiffness and stability required for the precise physics measures.

5.1 FLUIDIC CONNECTORS

The issue of reliable, reduced size, hydraulic connections between the external piping and the microfluidic devices is one of the factors still limiting today a wider use of this technology. In the last years the microelectronics field has been trying to reduce further and further the size of the components. Following this tendency, also the fluidic components have to be minimized adapting to the MEMS word. One of the challenges of this miniaturization, is to find a reliable and robust interface between the microfluidic chip and the outside world. A big variety of connections systems have been developed so far, with different methods for sealing the connector to the chip [65]. Several research groups presented in the past years numerous prototypes of fluidic connectors with different characteristics like out-of-plane or in-plane connections, or soldered, glued or mechanically clamped solutions [66][67][68][69].

The studies for the fluidic connectors for the present micro-cooling application are based on the existing connector proposals in literature, aiming to find a solution that could fulfil all the requirements of the application. A connector for a micro-channel device installed in a tracking detector has to be as small as possible to minimize the interaction with the traversing particles; has to be well connected to the micro-channels surface to guarantee the leak tightness also at high pressures; it should not damage the very fragile surface of the device; and, in several cases, it should be in-plane with the device for geometrical external constraints.
So far different types of connectors have been studied by the PH-DT cooling group with different assembling techniques. The very first fluidic connection adopted for laboratory tests was a commercial solution of plastic PEEK connectors glued on the silicon surface with a rubber joint for leak tightness. A mechanical clamping connector screwed around the silicon was then designed and tested; also in this solution the sealing was performed using an o-ring. A third method studied is soldering a metallic connector on top of the inlet hole on the silicon surface previously metallized. In the following these options will be described in detail. A couple of additional solutions will be also discussed for future developments on this subject.

5.1.1 NanoPort Peek Connectors

One of the first solution that was investigated inside the PH-DT group, is the commercial solution “lab-on-a-chip”, largely used in micro-fluidics application, of NanoPort Connectors from Idex Health and Science [50].

The solution used is the coned assembly in PEEK material, already seen in *Chapter 3*. The assembly is made of two parts screwed one inside the other (*Figure 5.2 a*): the bottom one is glued on the chip surface using a glue ring provided by the company and the leak tightness is given by a polymeric gasket compressed between the peek connector and the chip surface. A PEEK tube is inserted and is fixed using a plastic ferrule inside the top part of the connector. The assembly procedure starts with the gluing of the bottom part of the connector with the glue ring on the silicon at 160°C for one hour in the oven (*Figure 5.2 b*), then the top part is prepared with the tube and the ferrule, and it is screwed in the bottom part (*Figure 5.2 c*).

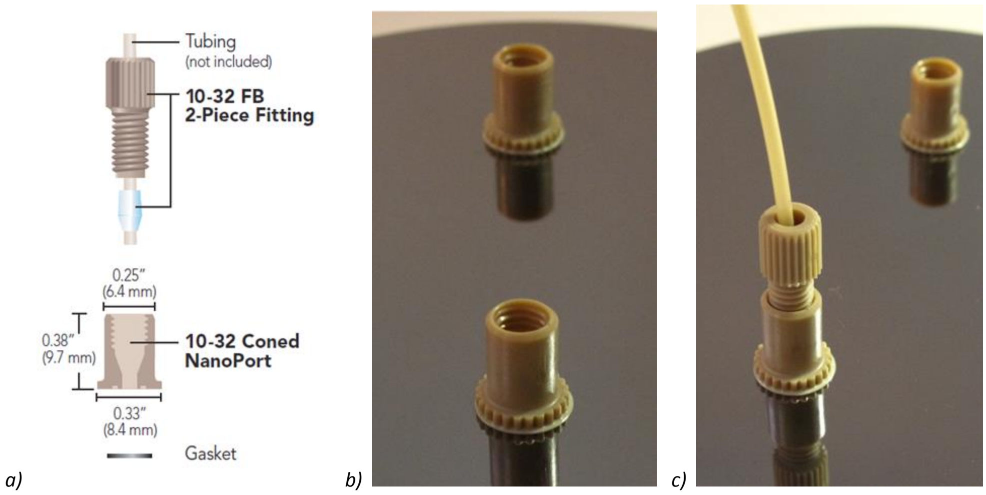


Figure 5.2: NanoPort PEEK connector scheme (a) Ref [50], picture of the bottom part of the connector glued on the silicon surface (b) and picture of the complete connector with the top part and the PEEK tube (c).

The drawbacks of this kind of connectors is the low reliability under thermal cycles or with high pressures. In fact, due to thermal cycles or to high pressures, the glue is detaching from the silicon surface. Using these connectors during temperature cycles, leads to a glue detachment due to the different CTEs of the two bonded materials. The high pressure of the CO_2 flow (more than 60 bar) stresses the glued joint, bringing also to the detachment of the connector. In the pictures of *Figure 5.3* it is possible to see two examples of the phenomena just described, during a thermal test for the NA62 experiment (*Figure 5.3 a,b*) and after a pressure test for the ATLAS experiment (*Figure 5.3 c*).

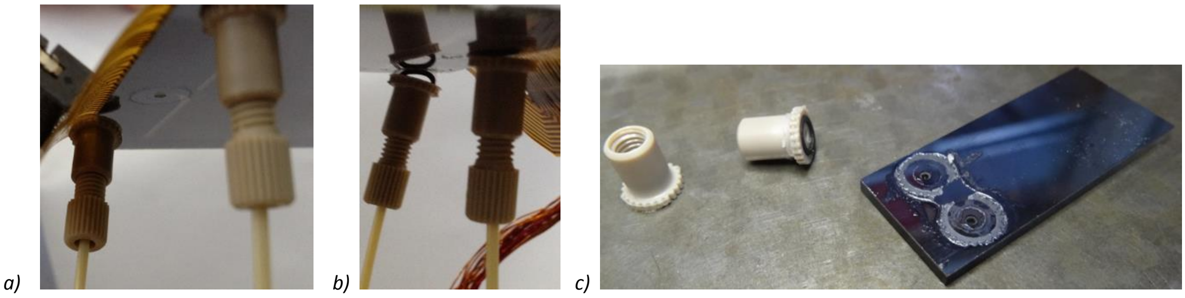


Figure 5.3: NanoPort PEEK connector detached from the silicon surface during a thermal test for the NA62 Experiment (a), detail of the black o-ring and the transparent glue ring detaching from the silicon (b) and two detached connectors from an ATLAS micro-channel device.

In order to try working with Nanoport connectors also with high pressures and during thermal cycles, several “in-house developed” methods were tested to increase the adherence of the connector on the mirrored silicon surface, like acting on the roughness of the silicon surface or adding more epoxy glue around the connectors. For the test with two-phase CO_2 flow for the LHCb experiment, a small metallic plate with two holes, was glued on the silicon surface on top of the NanoPort connectors to stiffen the glued joint (*Figure 5.4 a*). For CO_2 circulation the PEEK tubes are substituted by stainless steel tubes to be used with high pressures (*Figure 5.4 b*).

Due to the low reliability of these “in-house” methods a further study in different connection techniques was deemed necessary.

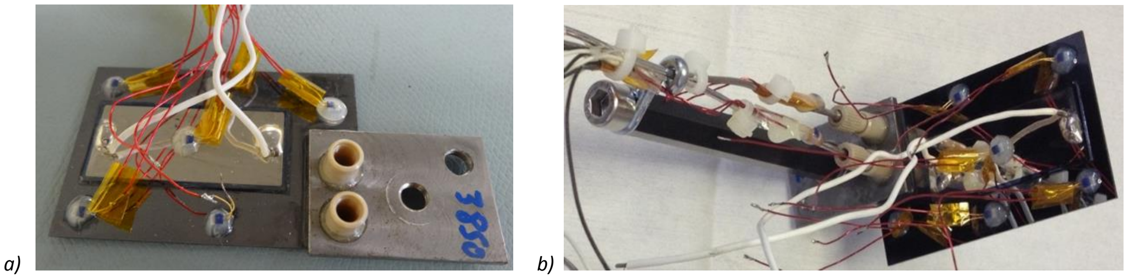


Figure 5.4: Metallic plate glued on top of the two NanoPort connectors for the LHCb experiment (a) and installation of the device using stainless steel tubes (b).

5.1.2 Mechanical Clamping Connectors

In order to solve the low reliability of the NanoPort connectors for the conditions of interest, and the related problems, a new mechanical clamped connector was developed inside the PH-DT group for the LHCb experiment.

The connector is made of two metallic parts: the bottom one presents a mechanical groove to align precisely the silicon micro-channel device and two holes, with rubber o-rings for sealing. In *Figure 5.5 a* is possible to see a 3D design and an exploded view (*Figure 5.5 b*) of the connector. The first prototype realized, with a silicon-Pyrex LHCb micro-channel device, is shown in *Figure 5.6*.

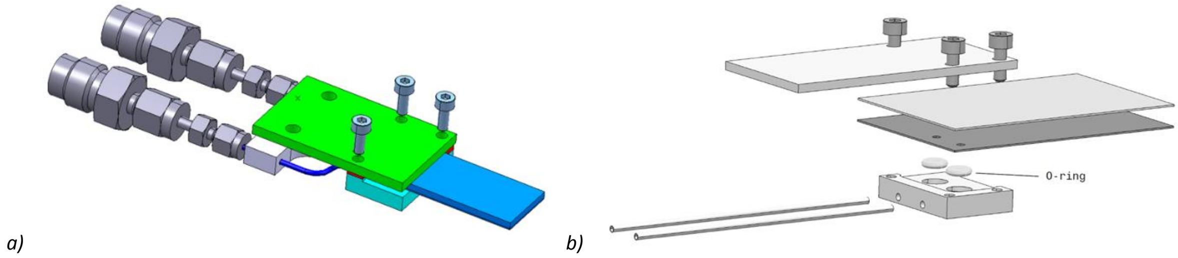


Figure 5.5: Clamping connector for LHCb experiment in 3D model (a) and exploded view (b).

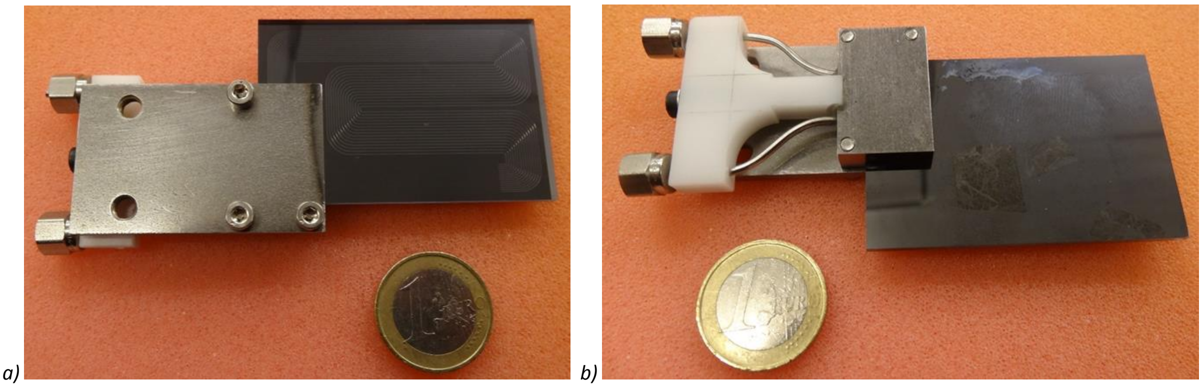


Figure 5.6: Pictures of clamping connector for LHCb experiment.

Following the design proposed for LHCb, a clamped connector was realized also for the ATLAS prototypes. This type of connector was tested and used several times with CO_2, showing great reliability and good mechanical properties. Unfortunately this connector requires fabrication and adjustments specific to each single micro-channel device. Indeed, the groove on the bottom part must be machined with the precise thickness of the prototype: every time that a new micro-channel plate has to be tested a new connector has to be machined. To avoid this aspect and to find a new high-pressure reliable method, the soldering of metallic connectors on the silicon surface was studied.

5.1.3 Soldered Brass Ferrules

An interesting paper was found in literature [47], reporting a new type of solder-based chip-to-tube connection. Metal bonding pads are deposited on the silicon or glass wafer surfaces and reliable connections are built by using standard soldering tools. Following this work, a similar connection method was tried for our micro-channel cooling systems.

In this method, 1/16'' stainless steel tubes are equipped with two Swagelok ferrules: the front ferrule in stainless steel and back ferrule in brass (*Figure 5.7 a*). The ferrules are inserted on the tube and they are then swaged on it inside a Swagelok connector according to the Swagelok ferrules working principle (*Figure 5.7 b*) [63]. The two ferrules guarantee sealing and mechanical grip on the tube; during assembly the front ferrule is driven into the fitting body and the tubing to create a primary seal, while the back ferrule is pressed inside to create a strong grip on the tube.

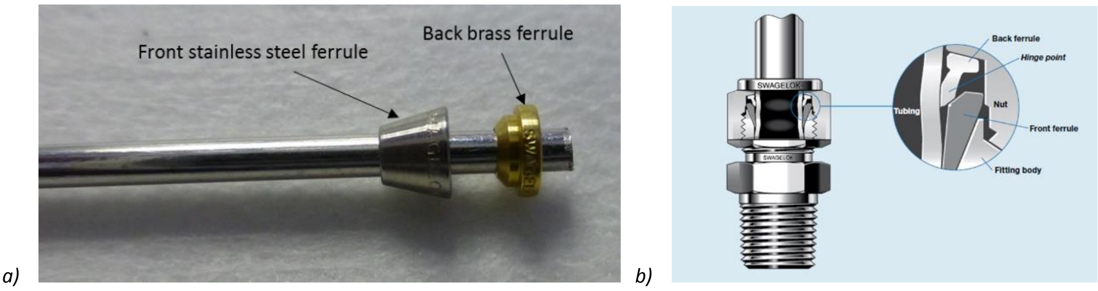


Figure 5.7: Pictures a 1/16'' stainless steel tube with two ferrules inserted (a), and scheme of Swagelok ferrules working principle (b).

When the ferrules are fixed on the tube, the tube is cut next to the brass ferrule in order to have a conical shape around the hole in silicon. The back ferrule is chosen in brass because it is directly involved in the soldering and it is in contact with the silicon surface. The silicon surface is metalized with different metal layer; the first test was done with 20 nm of titanium and 200 nm of gold. The soldering was performed by hand with a tin wire and, as soon as the brass ferrule was heated up by the soldering iron, a nice collar sets up around the connector (*Figure 5.8 a,b*). These first connectors have been tested in pressure with demineralized water and the maximum pressure of the available manual pump (700 bar) was not enough to break the joint.

A destructive analysis has been performed on one soldered connector. It was encapsulated inside an epoxy resin and then, after the resin polymerization, cut in half and polished to observe the cross section (*Figure 5.9*). From the section shown in *Figure 5.9 a* it is evident how the ferrules deformed in an irreversible way the tube diameter being tightened around the tube. No gap is visible between the back brass ferrule and the front stainless steel one. In the magnification of the right part of the soldering collar (*Figure 5.9 b*), it is possible to notice how the soldering is filling the area between the brass ferrule and the metalized silicon without blocking the tube and the silicon holes.

Connectors based on this technology are currently used in the PH-DT group for laboratory testing purposes. For final installation inside the detectors, a new more repetitive method have been developed.

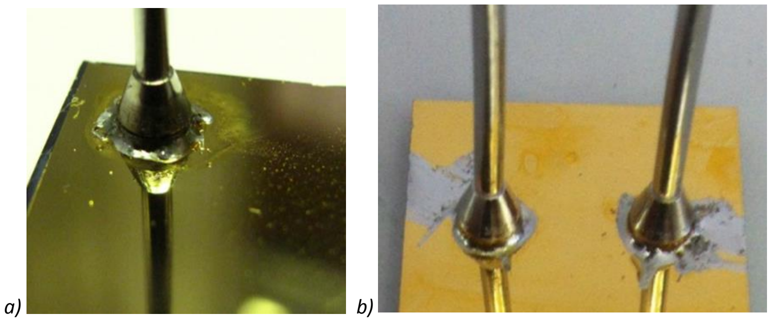


Figure 5.8: Pictures 1/16'' stainless steel tubes tin-soldered on the silicon metallized surface.

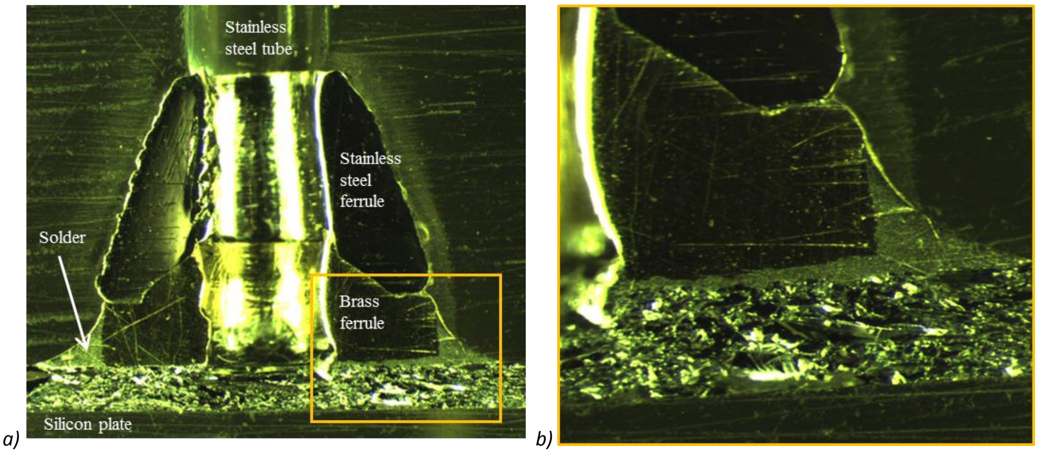


Figure 5.9: Cross section of a soldered ferrule connector on a silicon chip (a) with magnification of the soldering collar (b).

5.1.4 Kovar Connectors

Building on the experience gained with the soldered tube-ferrule connector, a new connector was designed for the specific micro-cooling application. The connector is machined in Kovar, a FeNiCo alloy with a CTE coefficient comparable with the CTE of silicon (~ 3 10^{-6}/K) in order to avoid mechanical stresses due to temperature changes.

Kovar is considered one of the best materials to be mechanically connected to glass and silicon. As reported in literature [70], Kovar has a CTE very close to the one of Pyrex and silicon at least up to 350 °C (*Figure 5.10*). . For this reason Kovar is also suitable for anodic bonding with glass in large area for micro-structures [71] or in local bonding for fluidic connectors [72].

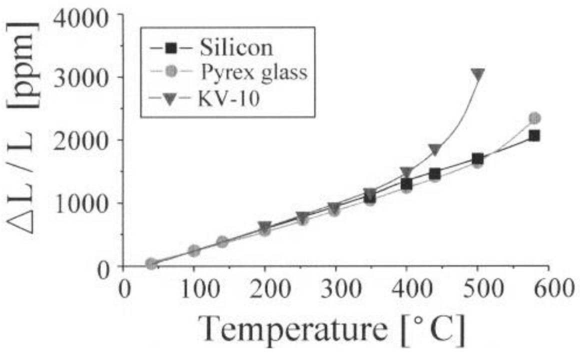


Figure 5.10: Thermal expansion characteristic of Pyrex, silicon and Kovar (Ref. [70]).

The Kovar connector designed for the micro-channels application is copper coated to perform the soldering. Also, on the silicon surface three metal layers are deposited: first a titanium layer to avoid metal diffusion inside silicon, then a nickel layer to perform the soldering and finally a gold layer to avoid nickel oxidation before soldering. To perform the soldering a SnPb foil, cut in a round shape few millimetres larger than the connector diameter, is inserted between the Kovar connector and the silicon plate. In *Figure 5.11 a,* a sketch of the assembly of the connector is shown. This first prototype of Kovar connector has an external diameter of 6 mm and a total height of 8 mm, for the moment no particular effort in made to minimize the connector size, that could be reduced further. The soldering is done in a vacuum oven (around 10^{-6}-10^{-7} mbar) at 200°C. The temperature profile adopted during the soldering is shown in the graph of *Figure 5.11 b*.

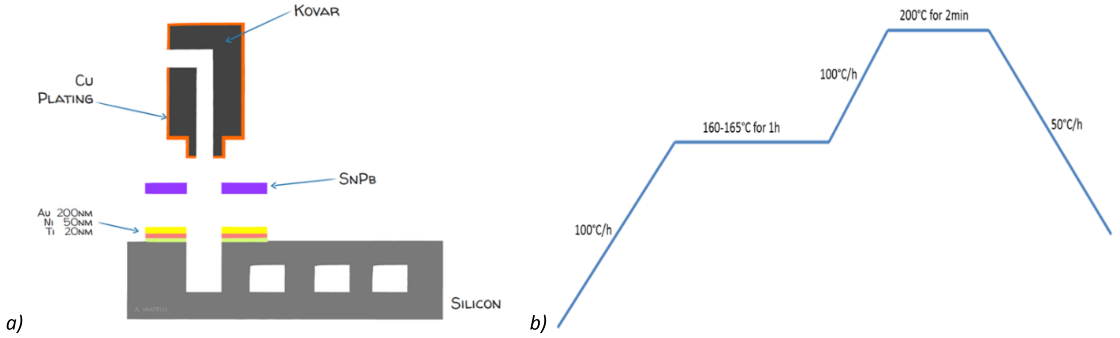


Figure 5.11: Scheme of the Kovar connector with the SnPb foil (a) and temperature profile during the vacuum soldering in the oven (b).

In *Figure 5.12* it is possible to see, before and after the soldering, the first test done in the vacuum oven. The Kovar connector, copper coated (*Figure 5.12 b*) is machined with a central pin to precisely align with the hole in silicon. The 15x15 mm silicon chip is fully metalized with Ti Ni Au respectively with 20-50-200 nm thicknesses (*Figure 5.12 a*). In the picture after the soldering (*Figure 5.12 c*) it is important to notice that the solder Sn-Pb foil, during the melting phase, covered the whole chip metallized surface.

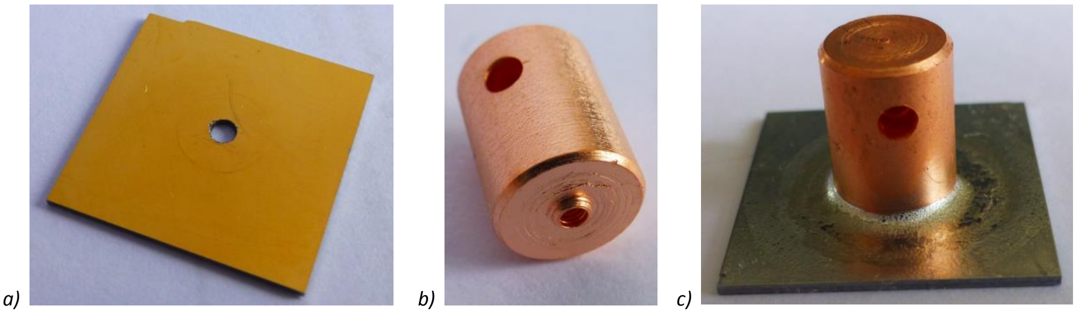


Figure 5.12: Silicon metalized chip with central hole (a), Kovar connector copper coated before (b) and after the soldering (c).

A destructive analysis has been performed on a sample to understand the nature of the interface between the connector and the silicon after the soldering. The analysis was conducted by the CERN EN-MME group. The connector has been cut in vertical until a total height of few millimetres to better perform the analysis. An x-ray picture of the soldering interface allows to individuate the presence of small voids in the solder that might potentially weaken the soldering up to the joint failure (*Figure 5.13*). After the x-ray image, the connector has been encapsulated in an epoxy resin and cut to observe its cross section (*Figure 5.14*). The sample surface has been polished and observed with a LEICA DMRME optical microscope. The picture shows a general view (*Figure 5.14 a*), the inner left (*Figure 5.14 b*) and right (*Figure 5.14 c*) detail, and the outer left (*Figure 5.14 d*) and right (*Figure 5.14 e*) edges of the connector. From the x-ray it was possible to see how the soldering quality is relatively good, with few visible voids at the interface between the Kovar and the silicon, quite small in dimensions. While from the cross section optical image it is possible to observe the soldering in between the Kovar and the silicon, the high external soldering collar around the connector and the lack of soldering in the central pin of the hole.

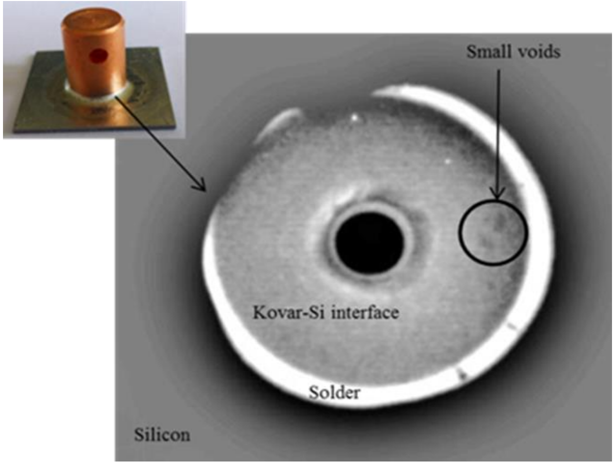


Figure 5.13: X-ray image of the interface between the Kovar connector and the silicon after soldering in the vacuum oven.

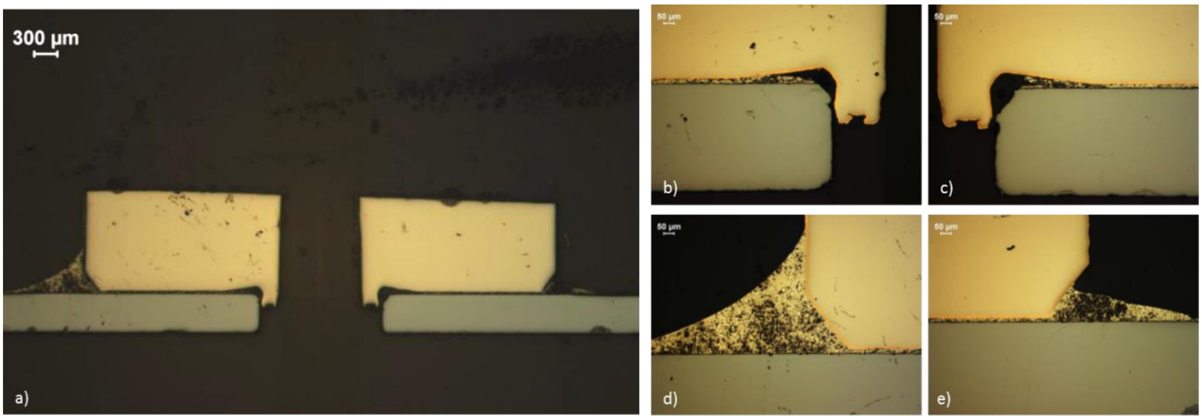


Figure 5.14: Cross section microscope pictures of the soldered assembly in vacuum oven: general view (a), inner left side (b), inner right side (c), outer left side (d) and outer right side (e).

A very similar test was repeated with another Kovar copper plated connector, on a full metallized silicon chip (Ti Ni Au, 20-50-200 nm) with a trough hole, using a SnPb foil. This time the soldering was done at 230°C using a vapour phase oven, where a perfluorocarbon fluid in vapour-phase form is used to transfer the heat to the components and the solder. The result was less satisfactory than the one in the vacuum oven, as it is possible to see in *Figure 5.15*. The first difference with respect to the sample done in the vacuum oven is the bad melting of the SnPb foil that has not covered the whole chip surface. This means a bad wettability of the surface due to bad soldering temperature parameters.

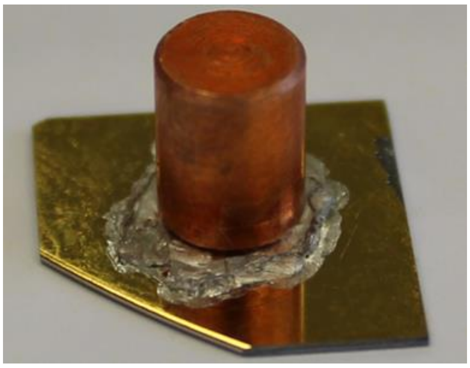


Figure 5.15: Picture of the soldering of a Kovar copper plated connector with a full metallized silicon chip in a vapour phase oven.

Another destructive analysis has been performed on this sample by the CERN EN-MME group in order to make a comparison with the soldering done in the vacuum oven. The x-ray picture of the soldering surface shows the bad quality of the soldering with the presence of numerous large voids at the interface (*Figure 5.16*) contrary to the previous sample. The presence of voids is visible also in the cross section (*Figure 5.17*) in the general picture (*Figure 5.17 a*) of the assembly, but also in the detail of the inner parts with the central pin (*Figure 5.17 b,c*) and in the outer sides (*Figure 5.17 d,e*) of the connector. A big difference from the connector soldered in the vacuum oven is the absence of the high collar around the connector, which is typically an indication of a good soldering quality. The solder at the interface between the two materials presents large voids, visible also with the microscope (*Figure 5.18 a,b*), due probably to gas trapped inside the solder during the melting of the SnPb foil. Starting from the top of the *Figure 5.18* it is possible to see the Kovar material, the copper layer, the solder layer with the voids inside and finally the silicon material.

Based on the results of the destructive analyses shown, it was finally decided to use the vacuum oven instead of the vapour-phase oven for the soldering procedure.

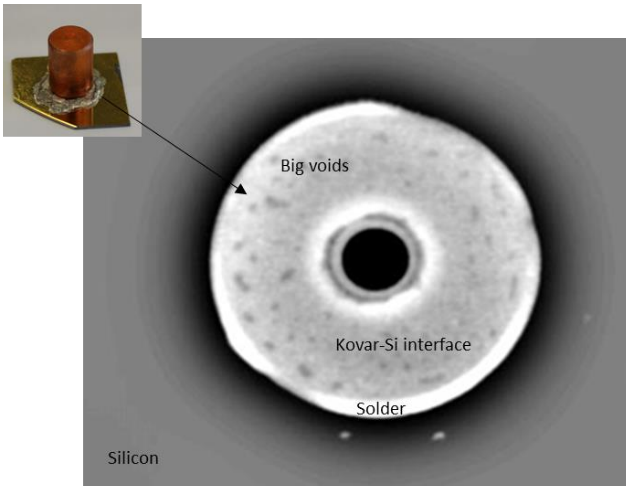


Figure 5.16: X-ray image of the interface between the Kovar connector and the silicon after soldering in the vapour-phase oven.

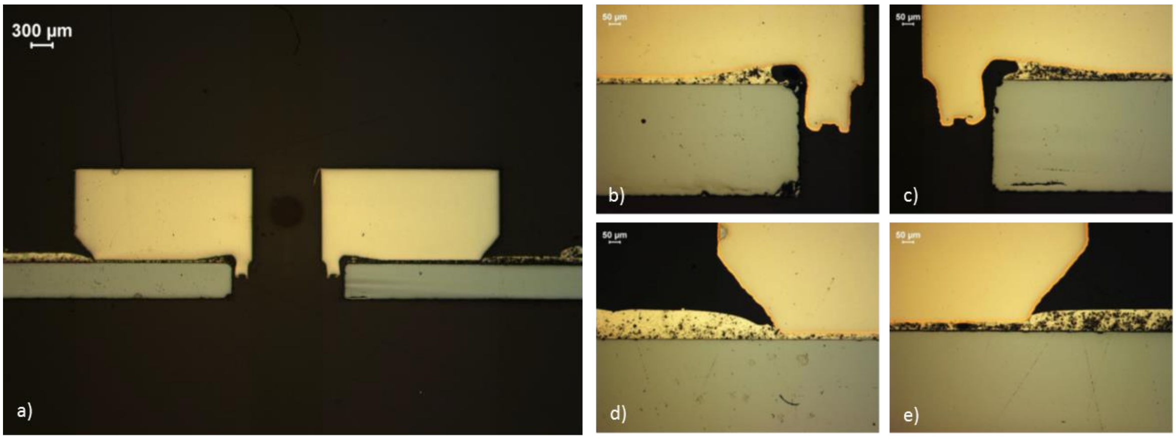


Figure 5.17: Cross section microscope pictures of the soldered assembly in vapour-phase oven: general view (a), inner left side (b), inner right side (c), outer left side (d) and outer right side (e).

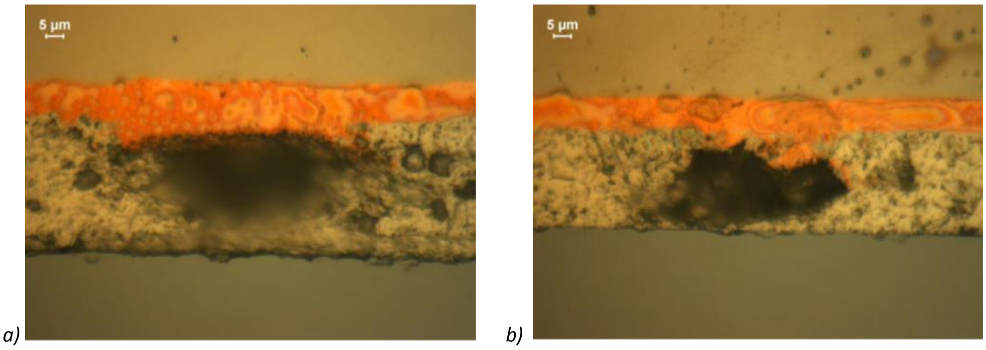


Figure 5.18: Microscope magnification of the voids in the solder at the Kovar silicon interface in the vapour-phase soldered connector.

The next step of the assembly procedure is to connect the Kovar connector to the external stainless steel tube. As shown in *Figure 5.12 b* a hole is machined on the Kovar side to host the stainless steel tube. The first method tested was to solder the stainless steel tube to the Kovar connector in the vacuum oven together with the soldering on silicon. Also the stainless steel tube has to be copper coated in order to perform the soldering. A test was done using a Sn Ag foil between the Kovar and the silicon, and a Sn Ag wire around the tube. The soldering was done in the vacuum oven at 230 °C. In *Figure 5.19* it is possible to see how the soldering around the tube, done in vertical position, brings to a lack of solder in the top part of the tube. Successive pressure tests done with water showed that the soldering was not sealed and the water leaked out around the tube.

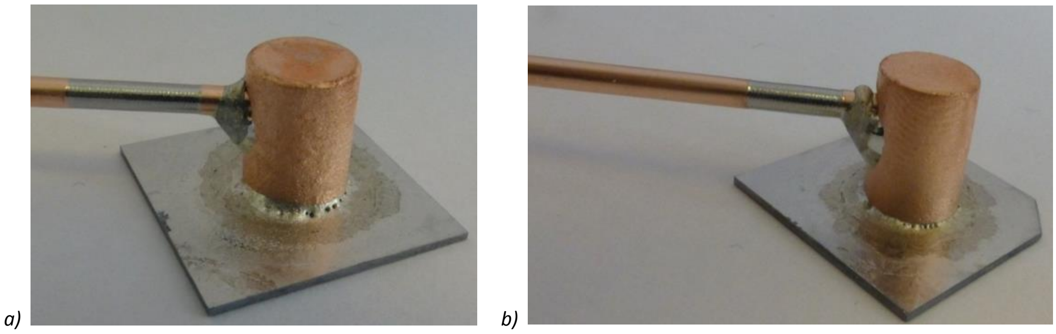


Figure 5.19: Picture of the first (a) and the second (b) test done with the Sn Ag wire to solder the stainless steel tube to the Kovar connector.

In order to avoid this problem, two improvements were introduced in the soldering procedure. First a small pocket was machined on the connector side around the hole for the tube, to host the wire for soldering, trying to avoid the gravity effect. In *Figure 5.20 a* is shown the model prototype connector machined in brass. Secondly the soldering of the tube was executed in vertical direction (like in *Figure 5.20*), in such a way that the connector is horizontal and the tube is kept vertical on it. In this way gravity is helping the soldering procedure. In order to avoid the soldering to enter inside the connector and to block the hole, the gap between the hole and the tube should be less than 0.1 mm. The soldering of the tube is done as a first step at 230 °C with a Sn Ag wire, while the soldering on the silicon is done as a second separated step, with the SnPb foil at a lower melting temperature of 200 °C. From *Figure 5.20 b* it is possible to see a first test of the stainless steel tube soldered inside the Kovar connector, and how the solder is confined inside the pocket on the Kovar side.

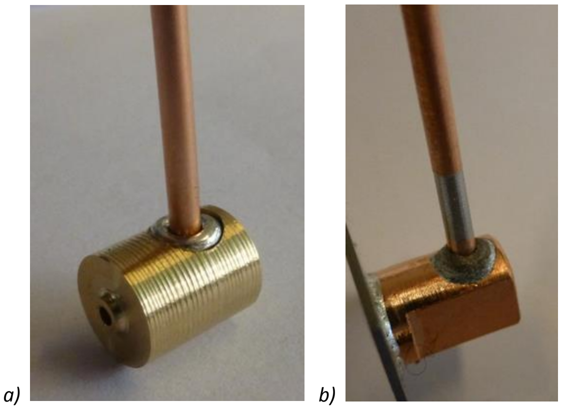


Figure 5.20: Brass prototype of the new connector with the pocket for the soldering wire (a) and test of Sn Ag soldering of the tube in the Kovar connector (b).

The SnPb foil used for the soldering of the Kovar on silicon has been later replaced by a SnPb wire to simplify the mechanical assembly of the pieces before soldering. In order to confine the solder on the chip surface a selective metallization of the chip is done, by using a hard mask during the metal deposition (*Figure 5.21 a*). A circular pad of around 8 mm of diameter has been chosen as default metallization on the chip. An alternative method tried to confine the soldering on the chip surface, is the etching of a circular trench around 30 µm deep, on the fully metallized silicon surface around the connector (*Figure 5.22 a*). In both cases the result is positive: in the selective metallization of the chip, the silicon low wettability is preventing the solder to spread (*Figure 5.21 b*), while in the trench case the edge of the trench stops the solder (*Figure 5.22 b*).

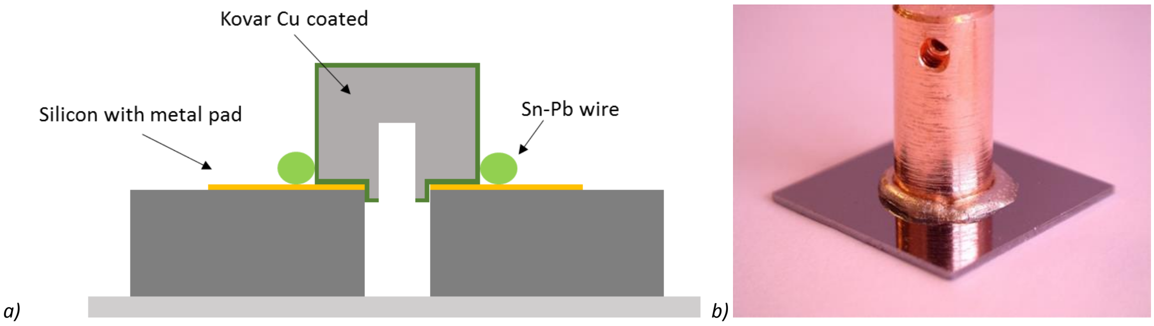


Figure 5.21: Soldering scheme of the partial metallization of the silicon surface (a) and picture of the resulting test (b).

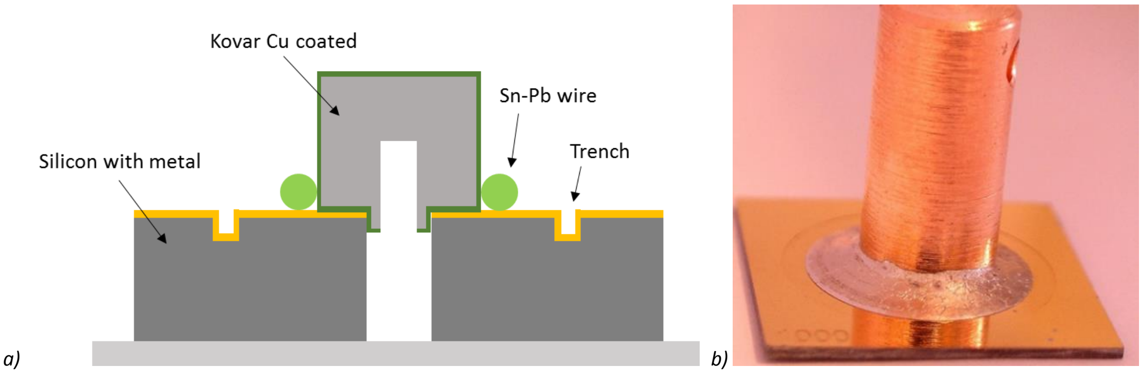


Figure 5.22: Soldering scheme of the etched trench of the silicon surface (a) and picture of the resulting test (b).

However, for the final procedure, the method of the metal pads has been selected for simplicity of the process flow where just a hard mask is necessary for the metallization of all the pieces.

A first test was done with a silicon micro-channel fluidic device with the ATLAS channels design. The chip has been processed inside the EPFL CMi cleanroom on a 4’’ wafer and the direct bonding has been done by CSEM in Neuchatel. The result of both soldering tests of the tube in the connector, and of the connector on the silicon, were successful (*Figure 5.23*).

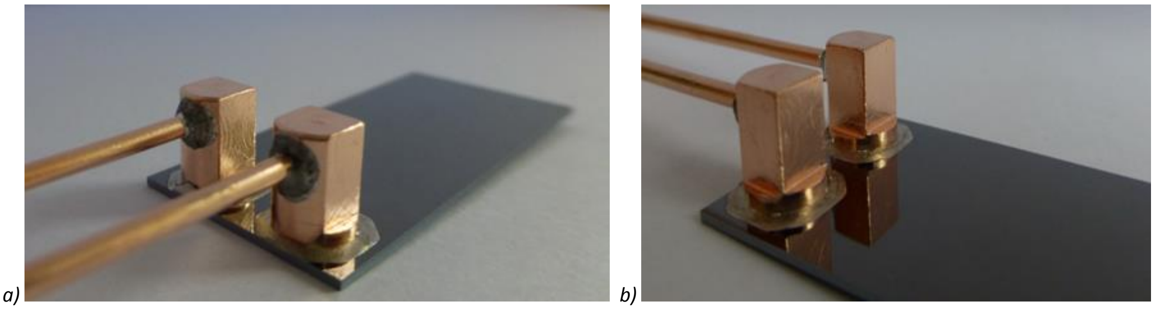


Figure 5.23: Front (a) and back (b) pictures of the first soldering test of a Kovar connector on a micro-channel cooling plate.

A circulation test was also done, but unfortunately the channels were found blocked by the soldering. Probably the soldering entered inside the silicon holes preventing the fluidic circulation. To avoid this problem, a further improvement was introduced removing the copper coating of the connector in the bottom side around the alignment pin. A first trial was done simply machining a previously Cu coated connector in the bottom part (*Figure 5.24 a*) and soldering it on a silicon chip with a through hole. The result was successful, as it is possible to see from the picture taken from the back of the silicon plate, where the hole is completely free from the soldering (*Figure 5.24 b*).

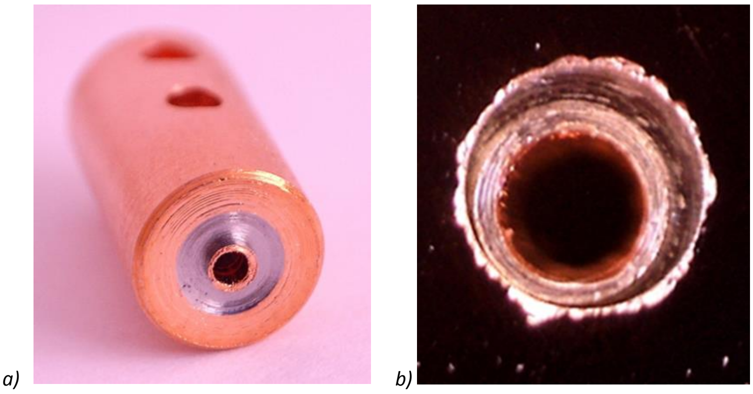


Figure 5.24: Kovar connector machined in the bottom side to remove the Cu coating (a), and back picture of the hole in silicon with the Kovar connector soldered on it (b).

Another procedure was also tested, in order to avoid the machining of the connectors after the copper deposition. Instead of coating everywhere the Kovar connector and then machine it afterwards, a selective coating of the Kovar connector was tried. A wax mask was deposited on the portion of the bottom side of the Kovar connector that should not be copper coated (*Figure 5.25 a,b*). After the copper deposition the wax is removed and the Kovar connector presents a selective copper coating (*Figure 5.25 c*).

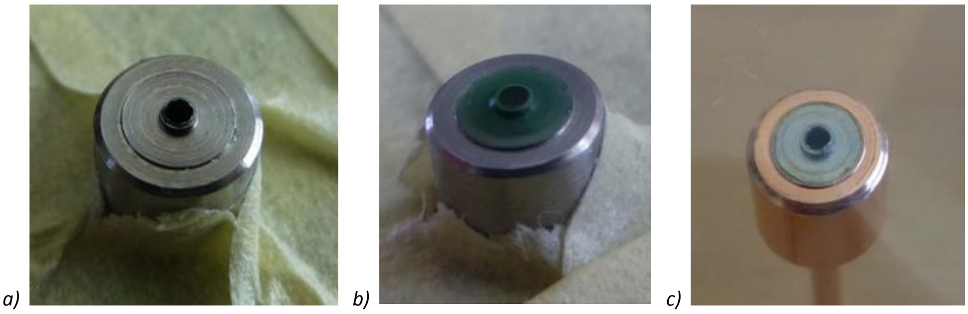


Figure 5.25: Kovar connector before (a) and after (b) the wax mask deposition to do a selective copper coating (c).

In order to simplify the connector assembly, laser welding has been tested for the connection of the stainless steel tube to the connector. A test of laser welding has been done (*Figure 5.26 a,b*) on a simplified design of the connector, where the tube is coming from the top. The laser welding showed good results: it has been also positively tested in pressure and leak and, for this reason, it has been selected for the final solution.

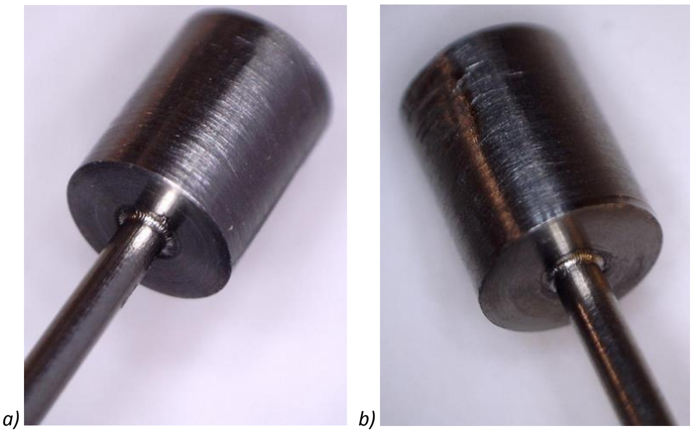


Figure 5.26: Pictures of laser welding tests of the stainless steel tube to the connector.

Finally the standard procedure for connecting the silicon micro-channel plates to the external tubing has been identified as follows: the Kovar connector is first laser welded to the stainless steel tube, and then the assembly is soldered with a SnPb wire to the silicon plate, where metal (Ti/Ni/Au) has been selectively deposited around the aperture. A picture of the final solution before (*Figure 5.27 a*) and after the soldering (*Figure 5.27 b*) is available in *Figure 5.27*. This final solution has been adopted for the NA62 micro-channels plate and also for the studies on the ATLAS prototype. For ALICE and LHCb, subject to different constraints, other types of connectors are being developed.

Several pressure tests have been performed on the soldered connectors using a manual water pump and the pressure of 700 bars (limit for the pump) was reached without any leak, showing the good reliability of this connection technique.

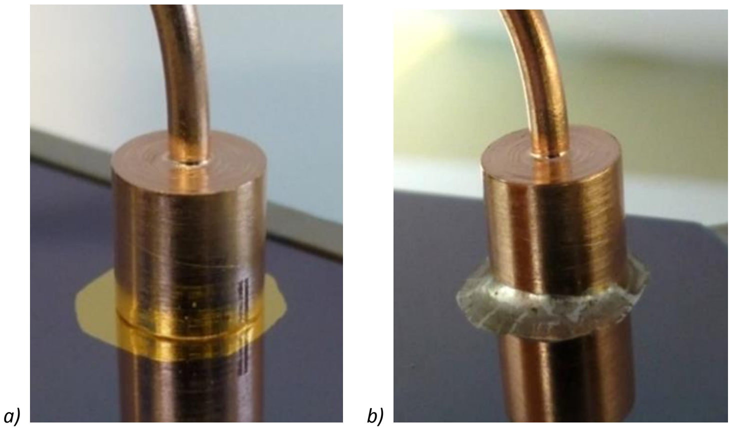


Figure 5.27: Pictures of the final solution of connector before and after the soldering on silicon.

5.1.5 LHCb Upgrade Connector

For the LHCb experiment, the proposed connector for the upgrade of the VELO detector [19] will be in between the soldering and the clamping solutions (*Figure 5.28*). The proposed solution is a Kovar piece with two stainless steel tubes brazed in it, machined in such a way to present two fluidic slots that provide the fluid to each channel in the micro-channel plate. The Kovar piece is soldered with a SnPb foil on the silicon surface. In the Kovar piece and in silicon three holes are made to insert three screws that provide an additional security by holding the connector attached to the silicon.

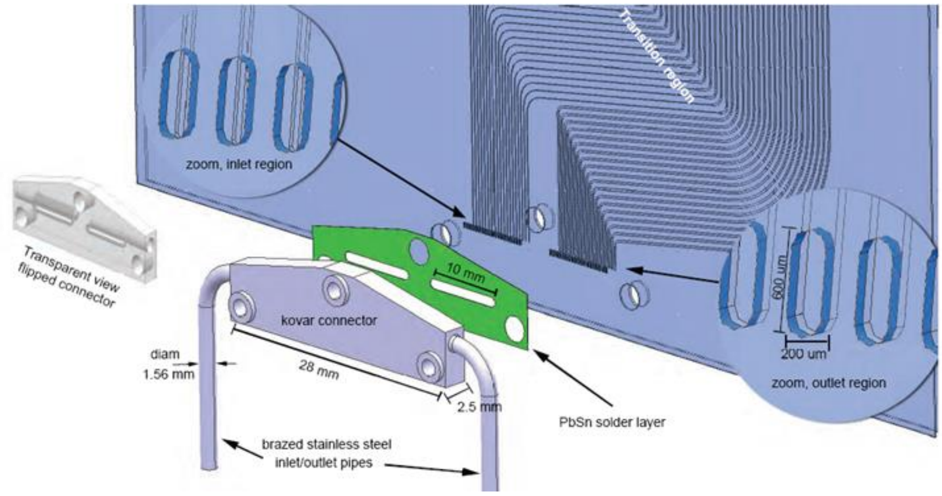


Figure 5.28: LHCb connector proposal for the VELO detector upgrade.

5.1.6 3D-Printed Connectors and Micro-channels

Recently, in collaboration with Manchester University, a study has been conducted on a new generation of connectors produced by Additive Manufacturing (“3D-printing”) in ceramic. Ceramic materials and in particular alumina, like Kovar, may have a coefficient of thermal expansion very close to the one of silicon. For this reason a new campaign of test on connectors 3D-printed in alumina has been launched. In particular the 3D printing technique allows a freedom in the connector design that is not guaranteed by the traditional machining techniques. The connector will be soldered to the silicon surface with a Sn-Pb foil and two titanium tubes will be brazed in it. The first connector tested has been realized by the French company 3DCeram [73]. The connector design is based on the ATLAS micro-channels chip. On the top part it presents a slot to align the silicon micro-channels surface to the two holes on the connector (*Figure 5.29 a*). On the bottom part instead the two tubes will be brazed (*Figure 5.29 b,c*).

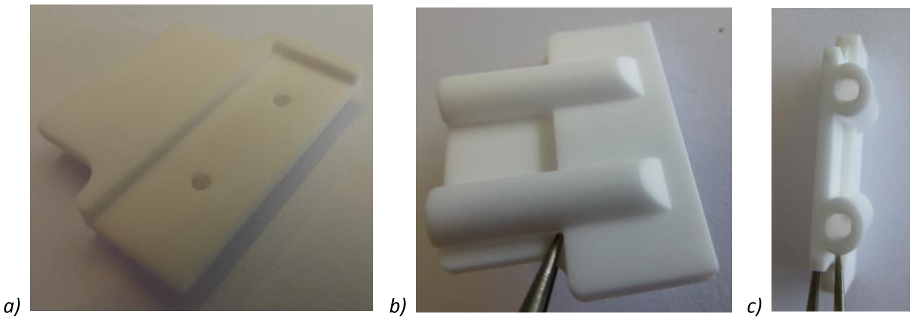


Figure 5.29: Front (a), back (b) and side (c) pictures of the first 3D printed connector in alumina.

In collaboration with the same company also a test to realize a complete micro-channel plate in ceramic material 3D printed has been developed. The technique used to print the device in ceramic material is based on the stereolithography additive process. During the first part of the process, a laser polymerizes, layer after layer, a paste made of ceramic and a photosensitive resin. After the complete polymerization, the object is exposed to a heat treatment where the resin is burned and the ceramic is densified to 100%. This techniques allows to realize different designs, but some constraints in the fabrication of micro-channels are set. The non-polymerized paste of resin and ceramic, has to be removed from all the cavities and channels, before the heat treatment in the oven. This means that the channels must be open to evacuate the non-polymerized paste and they should not be too small or too long. According to the preliminary constraints set by the experts of the company, two prototype designs for the micro-channel cooling plates have been proposed (*Figure 5.30*). A short micro-channels device is designed (*Figure 5.30 a*) with outside dimensions of 10x18 mm, with four micro-channels 0.4 mm in diameter. The total thickness of the device is 1 mm and the channels length is 8 mm for the two inner shorter channels and 10 mm for the outer longer channels. A second device is designed with longer channels (*Figure 5.30 b*), with total dimension of 10x28 mm. The four channels have a more complex design that allows for all the same length of 20.5 mm. In this case the channels have a diameter of 0.6 mm with a total height of the device of 1.4 mm.

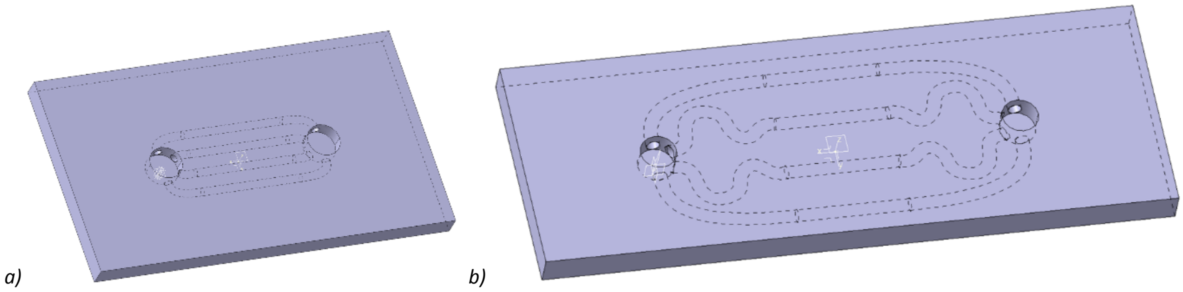

a) b)

Figure 5.30: Micro-channel short (a) and long (b) designs for 3D printing.

The two designs have been realized by the company in alumina pure to 99.8 %. The CTE of this type of alumina (~ 7.5 10^{-6}/K) is very close the CTE of silicon. A picture of the two realized prototype is available in *Figure 5.31*, in particular in the long channels device, the shape of the internal channel is visible through the device. During the testing phase some micro-channel devices have been cut to observe the internal cross section and the shape of the channels. In *Figure 5.32 a,b* are shown the cross sections of the short channel prototype while in *Figure 5.32 c,d* are shown those of the long channels device.

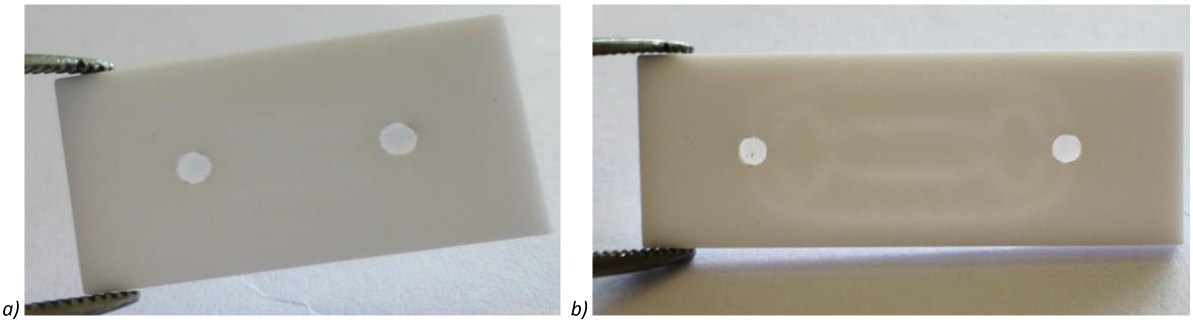
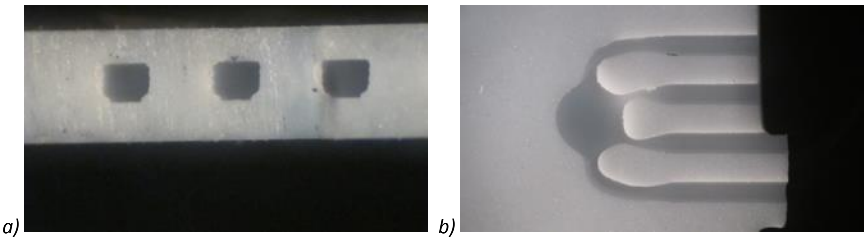

a) b)

Figure 5.31: Pictures of the short (a) and long (b) micro-channels devices 3D printed.


a) b)

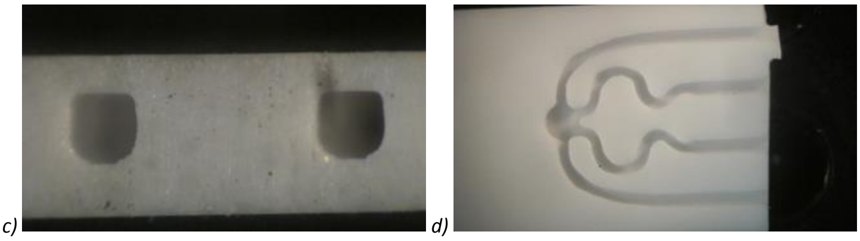


Figure 5.32: Cross sections of the short (a,b) and the long (c,d) 3D printed devices.

Pressure and fluidic circulation tests on these devices are planned for the next future.
In order to connect the 3D printed micro-channels to the external world, a connector based on the ferrules-connector used in the PH-DT group for silicon micro-channels has been developed. The connector proposed is a stainless steel tube with two Swagelok ferrules. The back ferrule in this case is in titanium in order to perform the direct soldering on ceramic without the metallization of the ceramic itself. The soldering is performed via a standard foil, ABA CuSil, made of a composition of copper, silver and titanium that allows the soldering on not-metallized ceramic. A scheme and a picture of the connector used is shown in *Figure 5.33*.

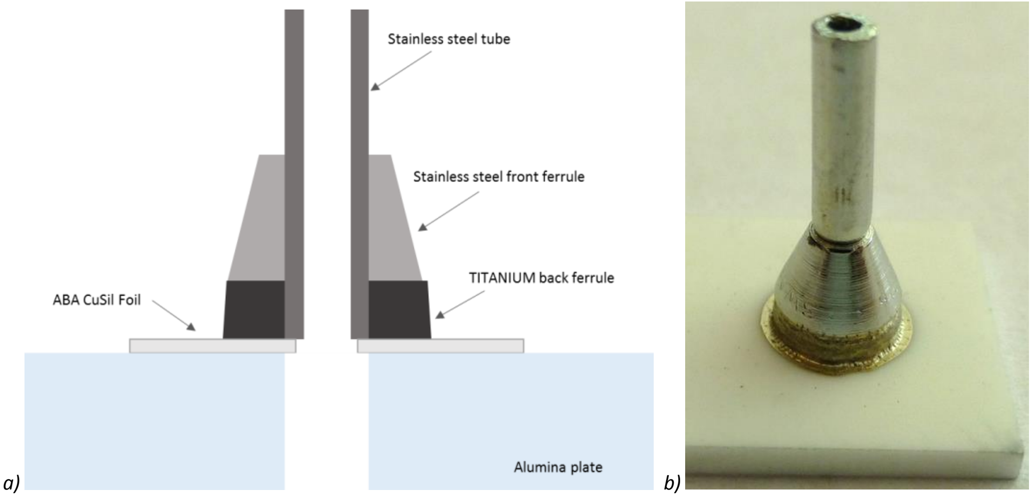


Figure 5.33: Scheme (a) and picture (b) of fluidic connector soldered on ceramic.

The first devices have been leak and pressure tested to check the connectors reliability. The leak test with helium shows zero leak with a vacuum level of $3x10^{-10}$ mbar l/s, while the pressure tests is done up to 400 bars with demineralized water with no leaks or fractures of the samples. In *Figure 5.34 a* is shown the long-channel prototype with the connectors and a details of the soldered connector in the ceramic surface (*Figure 5.34 b*).
Further tests are going on to understand the structural properties and the thermal properties of the micro-channels device 3D in ceramic compared to the ones on the silicon devices.

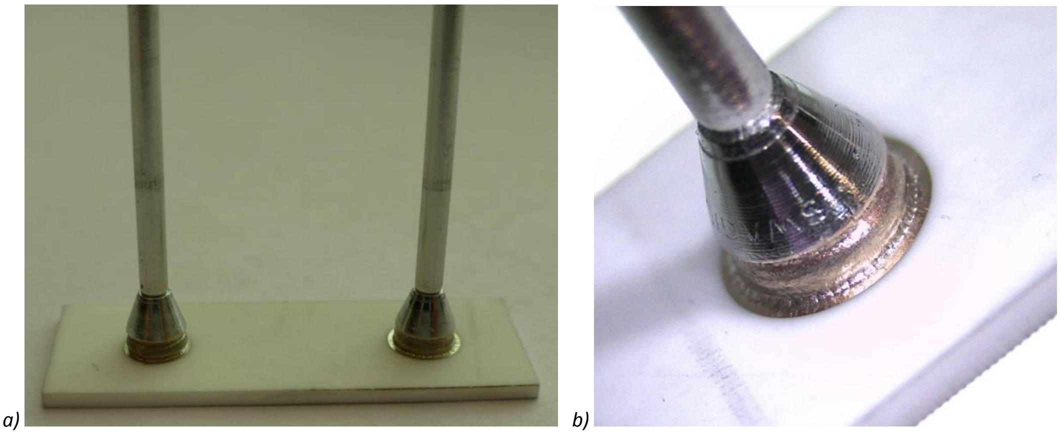


Figure 5.34: First realized long channels prototype (a) and detail of the soldered connector (b).

5.1.7 In-Plane Connectors

In micro-channels devices one of the most important requirements of the fluidic connector is to be as small as possible. In some cases, in addition, the connector should be laying in the same plane as the cooling device due to external constrains of the detector.
In the ALICE ITS detector, for example, the staves on which the silicon detectors lay, are organized in a circular shape around the beam area. For mechanical design constraints, one stave is overlapping for a small part the following one to obtain the correct angle. In this case the presence of a fluidic connector out of the stave plane is forbidden by the detector structure itself.
Other space-constrained application fields present in literature in-plane connections for fluidic devices. In [74] is presented a method based on mechanical machining of silicon to insert a tube on the side of a micro-channel chip. The technique foresees the fabrication of a silicon tube to insert inside a polymeric tube connecting to the outside world. Other applications, like implantation of microsystems inside the human body [75], propose in-plane connection for fluidic devices. In particular a capillary polyimide tube is inserted in-plane into the side of a fluidic micro-channel. The micro-channel is etched in silicon and it is closed by anodic bonding with a glass wafer. The tube is held in place with a Parylene deposition filling an empty volume around the tube (*Figure 5.35*).

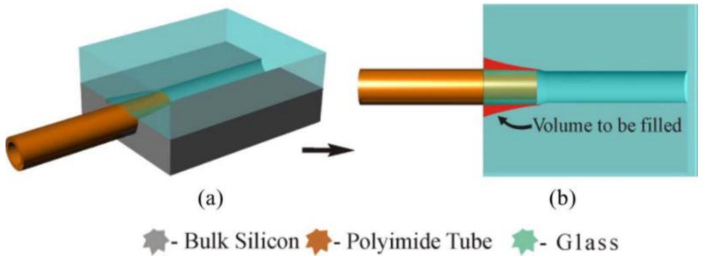


Figure 5.35: In plane connection of polyimide capillary in a micro-channel (Ref. [75]).

The solution shown in [75], is tested with an internal pressure up to 8 bar, pressure not sufficient for the micro-channel cooling devices. A tentative silicon in-plane connector has been developed inside the PH-DT group. In order to improve the mechanical resistance of the connection between the capillary and the micro-channel, a soldering technique is proposed. For the first tests, the micro-channel chip has been simplified to a simple silicon chip with a through hole, simulating the inlet of the micro-channel device. The idea is to have a silicon micro-fabricated *coupler*, as done in [76], mechanically aligned on top of the hole of the micro-channel circuit. The bonding between the coupler and the bottom plate can be done by soldering as in [77]. During the soldering of the coupler to the chip also the tube will be soldered in the channel. The mechanical alignment between the coupler top part and the bottom chip, is done by a mechanical structure obtained with a KOH wet etching. In the top and in the bottom parts a "pool" and a "counter-pool" are etched by KOH, as well as the distribution channel in which the tube will be soldered (*Figure 5.36 a,b*). When the two parts are aligned the fluid is entering trough the distribution channel, filling the pool area between the two silicon pieces and going down inside the micro-channels (*Figure 5.36 c*).

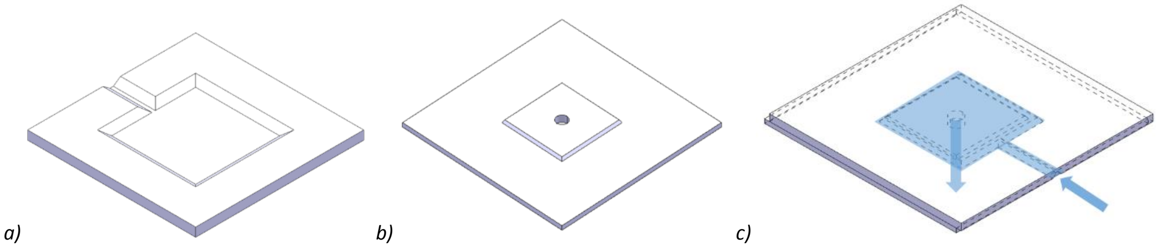


Figure 5.36: Top (a) and bottom (b) parts of the silicon in-plane connector (c).

A first fabrication test was done inside the EPFL CMi cleanroom. The resulting chips are shown in *Figure 5.37 a,b*, the hole in the bottom part is made afterwards by mechanical drilling. A first test of aligning the two parts and inserting the tube was done by gluing the components with an epoxy glue. The result was successful and the fluid flows in the chip (*Figure 5.37 c*).
Other futures tests will be done with metal deposition and soldering of the parts.

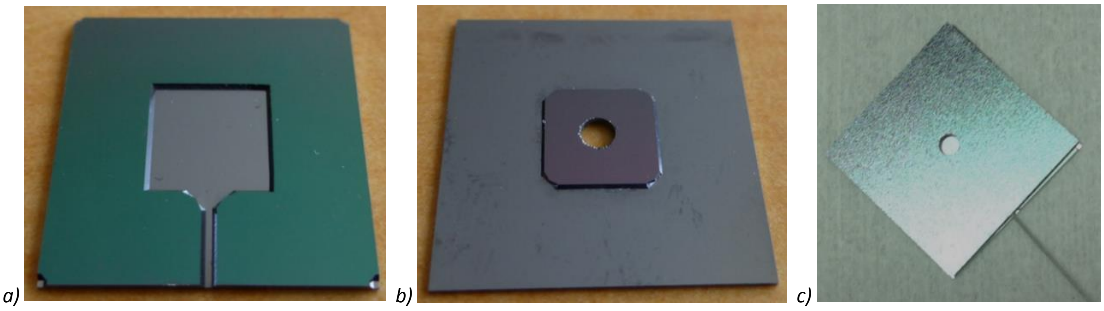


Figure 5.37: Top (a) and bottom (b) parts of the silicon connector and first test with glued metal tube (c).

5.2 DETECTOR GLUING

After a micro-channel plate is equipped with fluidic connectors, the next interface to take care of is the gluing of the detector on the micro-channels.
In order to glue the detector on the micro-channel device it is necessary to take into account different aspects like the correct positioning of the detector on the micro-channels and the glue choice.

The position of the detector on the micro-channel plate can be driven by mechanical or design aspects. For the NA62 experiment, the micro-channel plate is thinned in the central part in order to minimize the material crossed by the particles, and the detector has to be placed exactly in the centre of the thinned area. It is necessary to develop a special tool to glue the detector exactly in the centre of the

pool on the micro-channel surface. The gap between the edge of the detector and the edge of the pool is less than one millimetre.
For the case of the tests on the ATLAS prototype, instead, the position of the detector on the micro-channels is driven by the position of the wire-bonding pads on the chip that have to be perfectly aligned with the wire-bonding pads on the PCB.

The choice of the glue is complex because it has to keep into account different aspects. The glue layer should be thin to minimize the material crossed by the particle and to minimize the thermal resistance between the detector and the micro-channels. For this reason the glue should be dispensed in such a way that no air bubbles are trapped at the interface acting as thermal barriers. The presence of air bubbles trapped in the glue is dangerous also for the possibility of bursting in case of operation inside a vacuum vessels. The glue has also to sustain the large number of thermal cycles of the detector operation, while surviving to the high radiation level. It should finally cure at ambient temperature, or with only moderate heat, in order not to damage the detector with high curing temperatures. On the other hand, thanks to the large surface of exchange and to the very small distance between heat source and het sink, for a micro-channel device the conductivity of the glue only marginally affects the thermal performances.
Furthermore the glue has also often to fulfil specific mechanical constraints given by the experiment geometry. In case of NA62, for example, the 10 electronic chips are bump-bonded to the sensor with a gap of 100 µm between them, and the glue should not rise in between the gaps and touch the bump-bonds. Taking into account all these different aspects different glues were selected and tested for the gluing of the detector on the micro-channels plate.

5.2.1 NA62 Glue Choice

For the NA62 experiment the micro-channel plate is thinned in the central area where the detector should be precisely glued with a thermal interface. The detector is composed by the 63x29 mm sensor that is bump-bonded to the ten 12x20 mm TDCpix chips with a gap between them of less than 100 µm. On the top edge of the digital part of the chips the wire-bonding pads are located to perform the connection with the PCB. The total thickness of the glue should be around 30 µm that is the foreseen maximum planarity error of the chip and sensor assembly. It is possible to see a sketch of the structure and the assembly for the NA62 application in *Figure 5.38*.

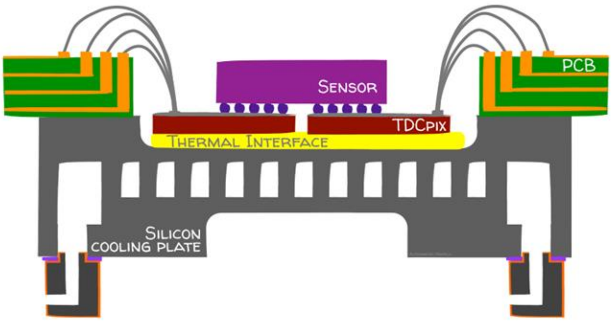


Figure 5.38: Schematic of the NA62 micro-channel cooling plate with the glue layer, the electronic chips and the detector.

Four glue types were initially selected and tested for this application: a double side tape from Nitto Denko [78], a glue thin layer from FastelFilm [79], a double side non supported adhesive from 3M [80] and a two-component liquid epoxy glue from Araldite [81].

The Nitto Denko double side tape is the number 5603, composed by a polyester film coated on the two sides with an acrylic adhesive with a total thickness of 30 µm. The 3M tape (number 9461P) instead is just a pure layer of acrylic adhesive without a support plastic film, with a total thickness of 30 µm as well. The FastelFilm 30 µm adhesive is an EVA (Ethylene-Vinyl Acetate) based solvent free adhesive that requires a thermal treatment to be softened and then polymerized. The epoxy glue is the Araldite 2020 two components liquid glue already used in several experiment and application at CERN.

The four glues were first tested in shear gluing two silicon samples. In a second moment, the silicon samples were also irradiated to observe the glue behaviour after the irradiation. The test samples were built by gluing a 10x10 mm silicon chip to another 10x10 mm silicon chip with the glue layer in between.

The samples were sent to irradiate at the high flux neutron and proton irradiation facility of Louvain-La-Neuve Cyclotron in Belgium. The selected radiation level is equivalent to the nominal radiation level for the NA62 experiment, with a value of $1x10^{14}$ MeV eq.neutron/cm^2. Other two radiation levels were also chosen to test the sample to a lower and a higher level, with values of $3x10^{13}$ MeV eq.neutron/cm^2 and $1x10^{15}$ MeV eq.neutron/cm^2. For each radiation level and for the non-irradiated level, five test samples were prepared and tested to have a probability indicator.

The shear tests were performed at the DIME (Dipartimento di Ingegneria meccanica, energetica, gestionale e dei trasporti) of the University of Genoa in Italy and the machine used was the Instron 8802 machine to perform tensile and fatigue tests. A special tool was machined to adapt the machine holding clamps to thin and fragile samples like the silicon ones. The tool is divided into two parts: the bottom one has a pocket in which the bottom silicon chip is positioned, the other part is a sliding part that pushes the top silicon chip. In this way the glue at the interface between the two silicon chips is shear tested. In *Figure 5.39* is possible to see a gluing scheme of the sample under test (*Figure 5.39 a*), a tested specimens glued with the NittoDenko tape (*Figure 5.39 b*) and the adapting tool for the shear tests machine used for the samples (*Figure 5.39 c*). In the picture of the tested sample it is possible to see how the two silicon chips slide one on the other and the adhesive in between in tested.

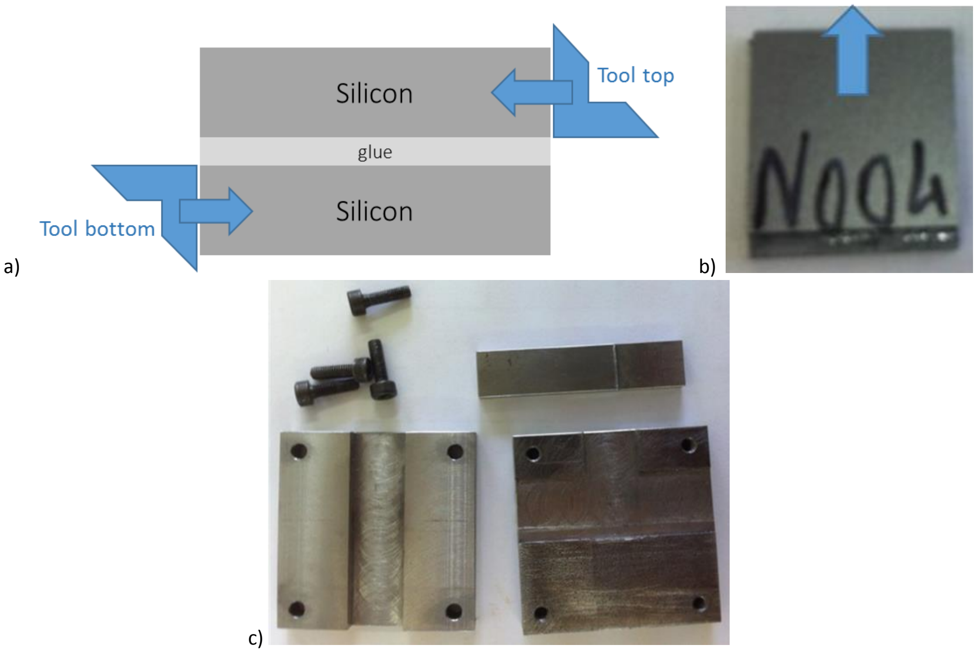


Figure 5.39: Scheme of the samples (a), tested samples glued with NittoDenko tape (b), and picture of the adapting tool for the shear test machine (c).

In the graph of *Figure 5.40* it is possible to see as an example the trend of the shear tests repeated on 5 samples for the 3M double side tape without irradiation, where in the x-axis is shown the strain of the sample during the test, while in the y-axis is shown the stress applied to the glue layer. The strain is the deformation of the sample compared with the initial length and it is reported as $\varepsilon = \Delta L / L_0$ where $\Delta L = L - L_0$ is the difference between the current length of the sample during the test while it is stressed (L) and the initial length of the sample (L_0 = 10 mm). The stress instead is defined as the load applied to the sample area (A = 10 x 10 mm) and it is indicated with $\sigma = F / A$ where A is the area of the sample and F is the applied increasing load during the test. The graph shows a good repeatability of the samples in the five tests.

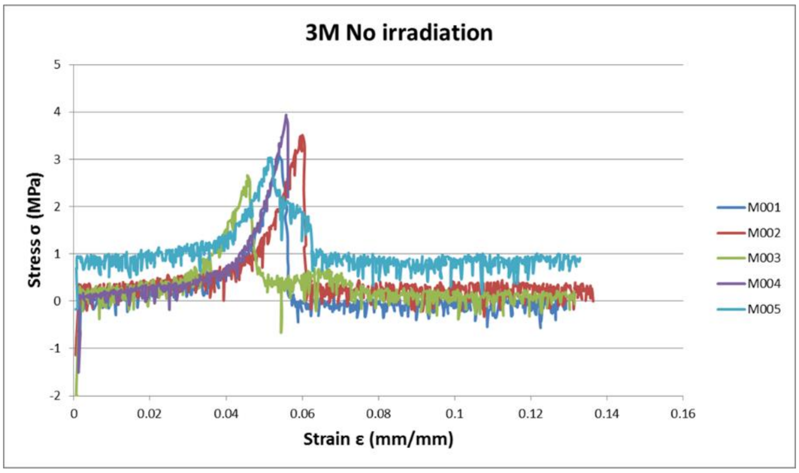
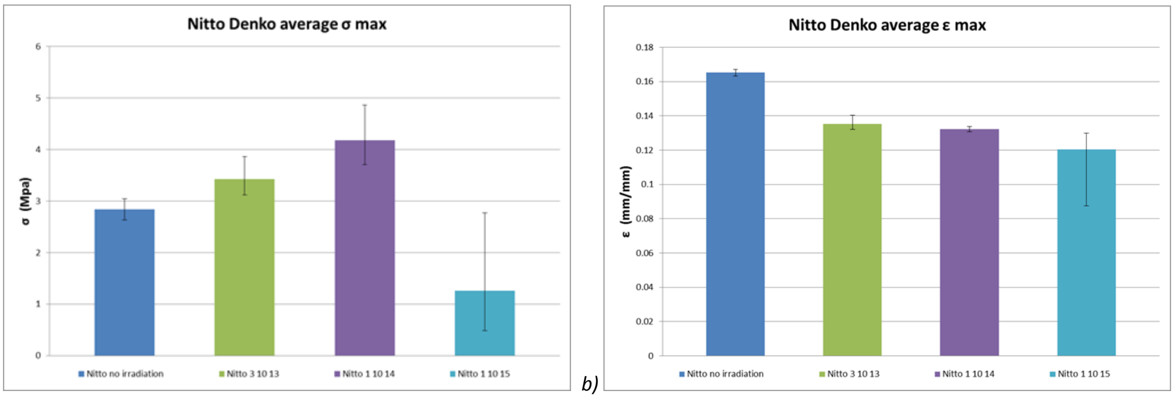


Figure 5.40: Stress-Strain curve for the 3M tape five samples without irradiation.

To better understand the glue behaviour after the three radiation levels, two bar charts have been built for each glue type with the average maximum strain over 5 realizations and the corresponding stress for the four cases of the non-irradiated samples and the three radiation levels.

The Nitto Denko double side tape behaviour, after the first two radiation levels, is to become harder and to resist more to the stress with a lower strain. With the highest radiation level the tape is completely damaged and the stress resistance is significantly lower than in the previous cases (*Figure 5.41 a*). The strain corresponding to the maximum stress is decreasing with the increasing radiation level showing a stiffening of the material (*Figure 5.41 b*).



a) *b)*

Figure 5.41: Comparison bar-charts for the Nitto Denko double side tape with average maximum stress (a) and corresponding strain (b).

For the first radiation level the behaviour for the 3M double side tape is similar to the Nitto Denko tape (*Figure 5.42*). For the second radiation level the tape is stiffer and the breaking stress and strain are lower than in the previous cases. For the highest radiation level, the tape is, also in this case, less resistant but is deforming more showing a viscous behaviour. It is important to notice that at the highest radiation level the 3M behaviour is comparable to the one of the non-irradiated case.

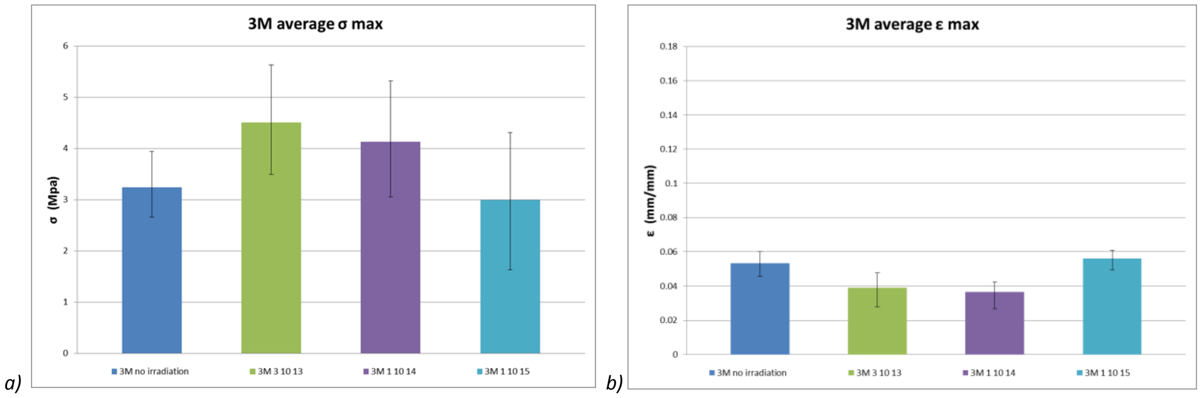


Figure 5.42: Comparison bar-charts for the 3M double side tape with average maximum stress (a) and corresponding strain (b).

For FastelFilm adhesive the tests are incoherent since it melted during the irradiations. In particular, being a thermoplastic material, it could have melted and polymerized again many times during the irradiation. The silicon chips are found misaligned and shifted compared to the non-irradiated ones. In the graph of *Figure 5.43* it is possible to see how the FastelFilm behaviour is really inconsistent.

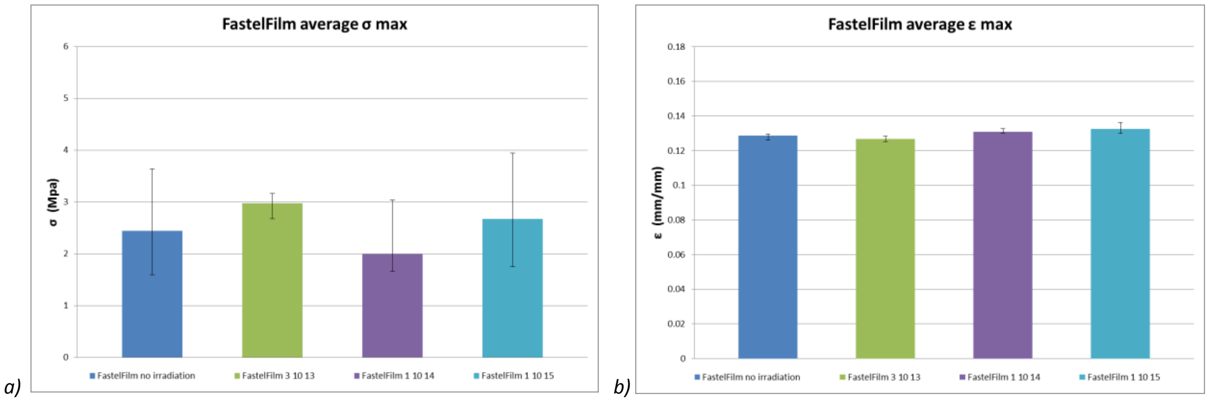


Figure 5.43: Comparison bar-charts for the FastelFilm adhesive with average maximum stress (a) and corresponding strain (b).

In the graphs of Figure 5.44, showing the results for the Araldite glue, it is important to notice that the stress values are one order of magnitude higher than the other glues. The epoxy glue is almost as hard as silicon and so it is difficult to have correct results while testing the samples. The majority of the times the silicon breaks instead of the glue. As it is possible to see in *Figure 5.45,* instead of stressing the samples in a shear mode and obtaining the deformation of glue by the sliding of the two silicon chips, the chips are completely destroyed in pieces since the silicon is a brittle material and the stress requested by the epoxy is too high for it.

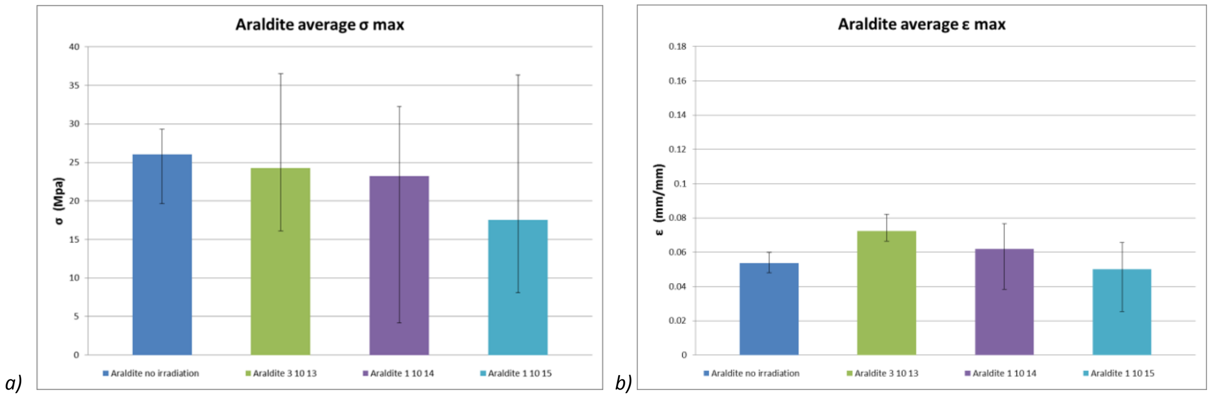


Figure 5.44: Comparison bar-charts for the Araldite glue with average maximum stress (a) and corresponding strain (b).

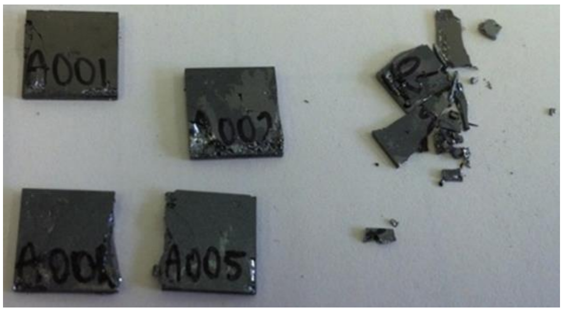


Figure 5.45: Picture of silicon sample glued with Araldite 2020 after test.

Since the Nitto Denko double side tape does not withstand the highest level of radiation and the FastelFilm melts under the radiations, these two adhesive were discarded from the glue choice for the NA62 experiment. After the irradiation and shear test campaigns, just two glues were still considered: the 3M double side tape and the Araldite 2020 epoxy glue.

In order to perform another test on the glues, a micro-channel device was glued to a heater simulating the chip heat dissipation using the Araldite 2020 liquid glue. The heater is made of 10 chips with metal lines to produce the heat glued to one central sensor. During the first test in vacuum the central thinned pool of the micro-channel device blew off in the central part, probably caused by an air bubble in the glue layer. In *Figure 5.46* it is possible to see the micro-channel plate broken in the centre with below the 10 chips covered by the glue.

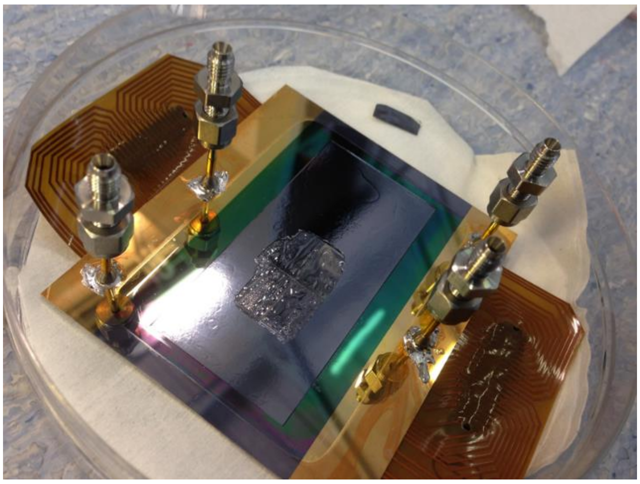


Figure 5.46: Picture of the broken micro-channel device glued with Araldite 2020 after the first test in vacuum.

The liquid glue maybe is not best solution for the NA62 application since the 10 read-out chips are bump-bonded to the sensor with a small gap in between them. The liquid glue could go in between the chips gap and reach the bumps causing electrical and mechanical problems. Furthermore the liquid glue should not spread outside the chips and sensor area in the silicon pool, and in particular it must not overcome the chips covering the wire-bonding pads that should be free for the metal wires. In order to test this glue behaviour and to understand better what happens at the interface between the two pieces several gluing tests were done.
A special jig has been developed to glue silicon chips, with the same dimensions and thickness of the read-out chips, to a glass piece with the same dimensions and thicknesses of the sensor. A schematic of the gluing test is show in *Figure 5.47*.

Figure 5.47: Schematic of gluing tests of ten silicon chips to one glass sensor

The mechanical jig to perfectly align the chips to the sensor and to leave the correct gap between them is the same used also for the assembly of the heater mock-ups. It consists of a bottom part, where ten pockets for the position of the chips are machined (*Figure 5.48 a*), and a top part with one pocket for the sensor (*Figure 5.48 b*). The bottom and top parts of the jig are aligned with precision alignment pins.

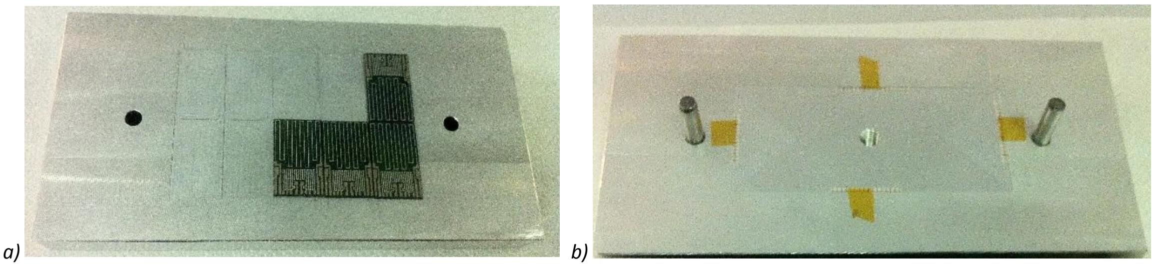


Figure 5.48: Bottom (a) and top (b) part of the jig to align the chips to the sensor.

A first test using this jig, was done using the Araldite 2020 liquid glue to glue the ten silicon chips to the glass sensor. The glue is dispensed using a syringe with a needle (internal diameter of 0.51 mm) and putting a drop of glue on each chip. A weight of 1.6 kg is positioned on top of the jig after the alignment during the polymerization of the glue. In *Figure 5.49* it is possible to see the result of the gluing; the glue is totally spread also outside the chips and the print of the original drops are visible. The assembly was completely glued to the jig and it was impossible to detach without breaking it.

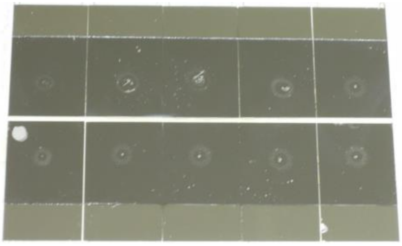


Figure 5.49: Gluing test with Araldite 2020 deposited with a syringe (needle internal diameter 0.51 mm).

A second test was done using Araldite 2020 where a small amount of glue is dispensed this time with a brush on each chip (*Figure 5.50 a,b*). The gluing was done with the same weight of 1.6 kg on top. The result (*Figure 5.50 c*) is better than the previous one, and the glue is not completely spread on the jig so the assembly is easy to detach from the jig surface. On the other hand, the glue is not covering all the chip surface and is leaving large air bubbles at the interface.

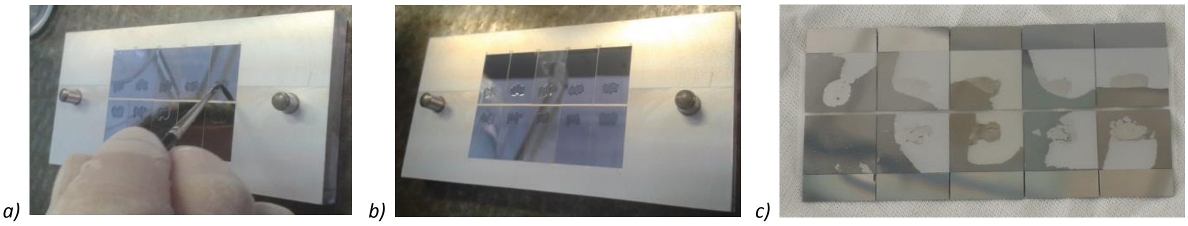


Figure 5.50: Gluing test with Araldite 2020 deposited with a pencil (a, b), and result of the gluing (c).

A third test was done using Araldite 2020. Also this time a syringe with a needle was used but the needle diameter was smaller (0.2 mm internal diameter) to reduce the quantity of glue for each chip. Also the weight was reduced to 1.3 kg. After the gluing the result (*Figure 5.51*) is similar to the result obtained with the pencil, where it is not really possible to control the glue behaviour as part is going out of the chips area and part of the chips are not covered by the glue.

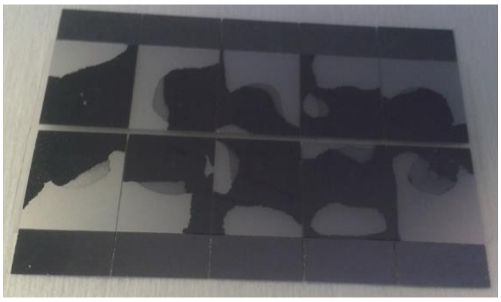


Figure 5.51: Gluing test with Araldite 2020 deposited with a syringe (needle internal diameter 0.2 mm).

The same tests were done with the 3M double side tape. The tape was cut at the same dimension of the sensor and it was glued on it before aligning and closing the jig on top of the chips (*Figure 5.52*). A weight of 2.8 kg was used to complete the gluing. The glass sensor was already stretched before the assembly in correspondence of the bottom left chip. In a first moment the gluing seems not perfect with at least two top chips not completely glued (*Figure 5.52 a*). After some time the gluing quality seems to improve, in fact the whitish parts in the sensor are gradually decreasing after a day (*Figure 5.52 b*) and after six days (*Figure 5.52 c*), until they completely disappear after a month (*Figure 5.52 d*). This phenomena can be explained by the 3M characteristic of increasing the bond strength with time and temperature [80].

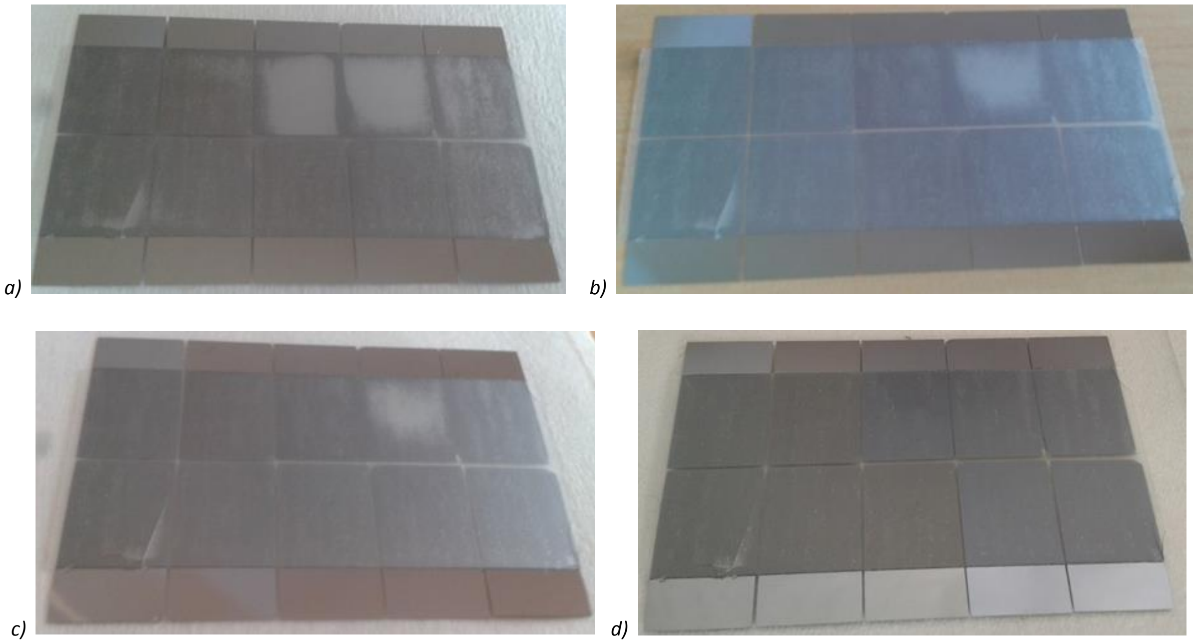


Figure 5.52: Result of gluing test with 3M double side tape, right after gluing (a), after a day (b), after six days (c) and after a month (d).

After the described tests, a final test was done by gluing the assembly of the dummy chips and sensors on top of a glass piece to understand the 3M behaviour at the interface between the micro-channels and the detector. The gluing was done with a total weight on top of the dummy detector of 1.3 kg. In *Figure 5.53* it is possible to see the good result of the gluing from the backside of the glass piece where the glue is not presenting any defect.

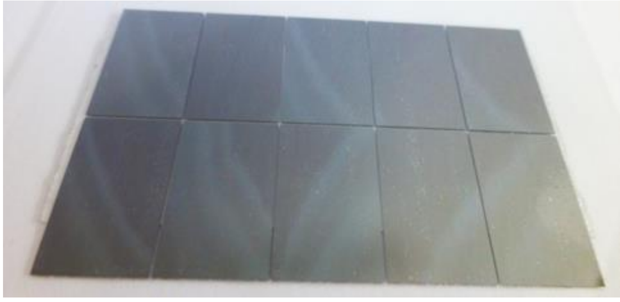


Figure 5.53: Picture from the back side of a gluing test with 3M double side tape of a dummy detector on top of a glass piece.

Thermal cycling tests were also done on a glued assembly with the 3M double side tape, cycling the temperature from +30 °C to -25 °C. No visible damages occurred on the glued assembly.
According to the datasheet, the 3M double side tape has temperature range resistance from -40 °C up to 232 °C. It has been also proven how it guarantees a good gluing without air bubbles, and without the risk of overcoming the chips and touching the bump-bonds or the wire-bonding pads.
Based on all the tests performed and the good characteristics, the 3M double side tape was selected as thermal interface between the detector and the micro-channel device for the NA62 experiment.

5.2.2 ATLAS Glue Choice

For the tests on tha ATLAS prototypes the requirements are a bit different. The goal is to test the micro-channel cooling system for the thermal management of a FEI4-A chip of 2x2 cm that dissipates, under nominal conditions, a total heat of 1.5 W. A specific micro-channel circuit is designed for the application. The chip is composed by a 3D silicon sensor bump-bonded to an electronic chip. The electronic chip needs to be wire-bonded to a PCB in order to be tested. The FEI4 chip has to be glued on the micro-channels with a precise alignment of the wire-bonding pads on the PCB and the ones on the electric chip. For this reason there is the need of a glue that allows the movement after the two pieces are in contact. For this reason it is not possible to use the 3M tape like for the NA62 experiment. Like for NA62, the thermal layer needs to be as thin as possible, with not air bubbles and with no spreading outside the contact area between the two. In this case the maximum glue thickness is not determined by the planarity of the detector since the detector is done by a single piece. There are no gaps in between chips, like for NA62, where the glue can go.

For these reasons a liquid glue is selected from Master Bond [82]. The glue used is the EP37-3FLFAO a two components epoxy liquid glue, that is thermal conductive and electrically insulative, it has a NASA approved low outgassing feature, it cures at ambient temperature and it has a high flexibility.

The glue is used to glue the micro-channel plate on top of the PCB and, after the glue polymerization, to glue the FEI4 chip on the micro-channel plate. During the second gluing after the two parts are in contact, the chips can still be moved to perfect align it with the wire-bonding pads of the PCB. In *Figure 5.54* it is possible to see the complete assembly after gluing. The micro-channels are the dark grey silicon chip with soldered on top the Kovar connectors. The 3D sensor is the white part and below it there is the electronic chip, of which it is possible to see the wire-bonding pads with the wires connected. The Master Bond glue is not perfectly aligned with the detector and a small quantity of glue is sticking out from the interface on the right and on the left side, but it has no influence on the chip working conditions.

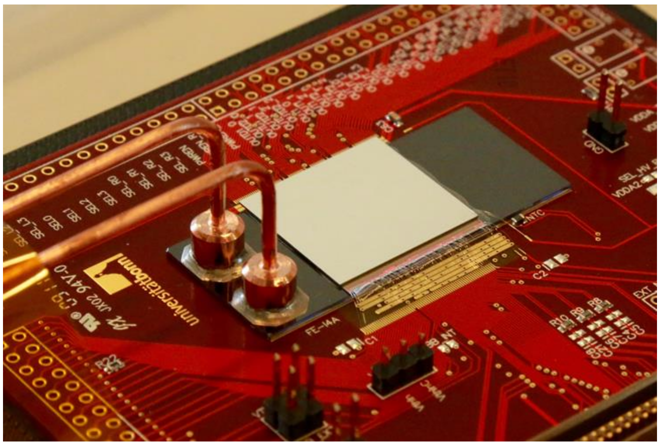


Figure 5.54: Picture of the FEI4 chip, glued on top of the micro-channel silicon plate with the wire-bonds for the ATLAS experiment.

5.3 INTEGRATION WITH OTHER COMPONENTS

Beside the fluidic connectors and the detector gluing, the silicon micro-channels require also other integration processes before being inserted in the test sections or in the real detectors.

A crucial point is the support for the micro-channels. For every test a solid mechanical support is needed to fix the fragile and light micro-channels. The support is necessary also to protect the micro-channels from any stress that can occur from the environment. For examples the metal tube of the connectors are heavier than the micro-channels plate and they need to be fixed to a solid support to avoid stress on the micro-channels. During the connection of the connector capillaries to the bigger tubes of the experiment, a stress release point is necessary to avoid fractures in the silicon.

For the ATLAS test the PCB itself is used as a support for the micro-channels and also for the NA62 application. However a mechanical support for the tubes is necessary in both cases since they are heavier and they could detach the silicon plate from the PCB.

For the ATLAS application the silicon micro-channels are glued on the PCB and a 3D printed frame, with a wall to support the tubes, is screwed to the PCB. In *Figure 5.55 a* it is possible to see the PCB with the micro-channels and the 3D printed black frame around with a details of the wall to support the tubes (*Figure 5.55 b*).

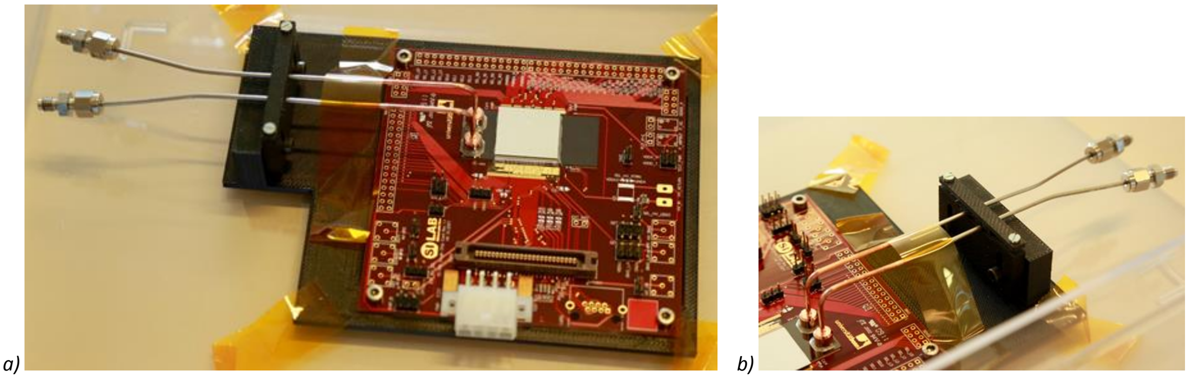


Figure 5.55: ATLAS PCB with the micro-channels and the 3D printed black frame (a) with a detail of the wall to support the tubes (b).

For the NA62 a similar solution is adapted, but the micro-channels are not glued on the surface but fixed with mechanical clips, and the frame around the PCB is done in metal as well as the wall to support the tubes. In *Figure 5.56* it is possible to see a picture of the NA62 module with the metal frame and the support for the tubes.

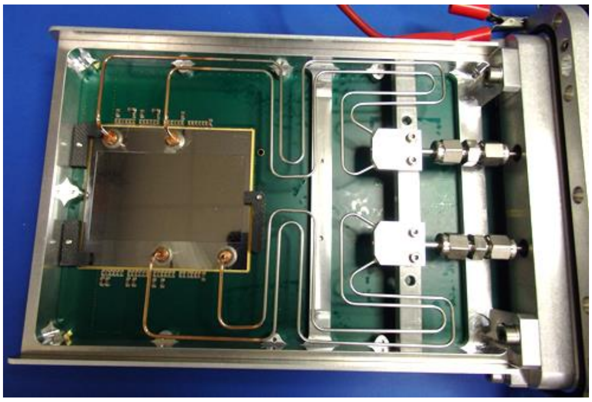


Figure 5.56: Picture of the NA62 PCB with the micro-channels and the metal frame.

Also in the ALICE micro-channel solution a support is needed. In the ALICE configuration the Inner Tracking System (ITS) is compostED by several staves 29 cm long that are displaced in circular structure around the beam. A micro-channel-based solution is being developed for this application as a back-up for the traditional cooling scheme adopted as a baseline. In order to cover the 29 cm length of a stave, the micro-channels need to be connected one to the other in line to create a long unique cooling plate.

The detector chips are glued on the micro-channels and a mechanical carbon fibre structure is fixed on the back for the cooling plate as it is possible to see in the scheme of *Figure 5.57*.

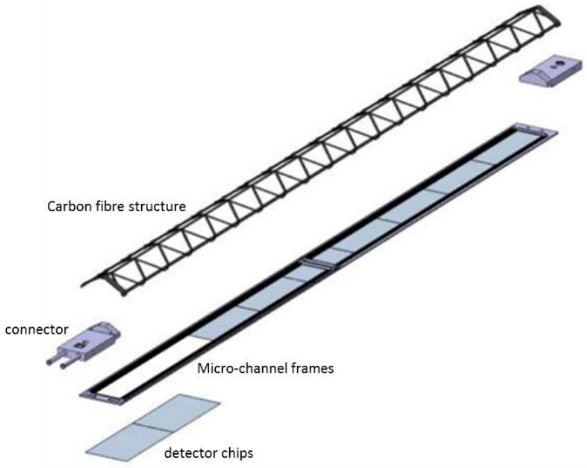


Figure 5.57: Scheme of the ALICE micro-channels cooling proposal.

In order to connect two micro-channel frames in line, an in-plane design of a connector has been proposed [26]. The connector design is called the “bridge” solution, where a very small single micro-channel piece is glued on one side, in correspondence with an outlet hole of a frame and on the other side in correspondence with the inlet hole of the next frame. In this way the fluid exits from a frame, goes up in the bridge and then goes down again in the other frame. In *Figure 5.58* it is possible to see a scheme and a picture of the “bridge” connector.

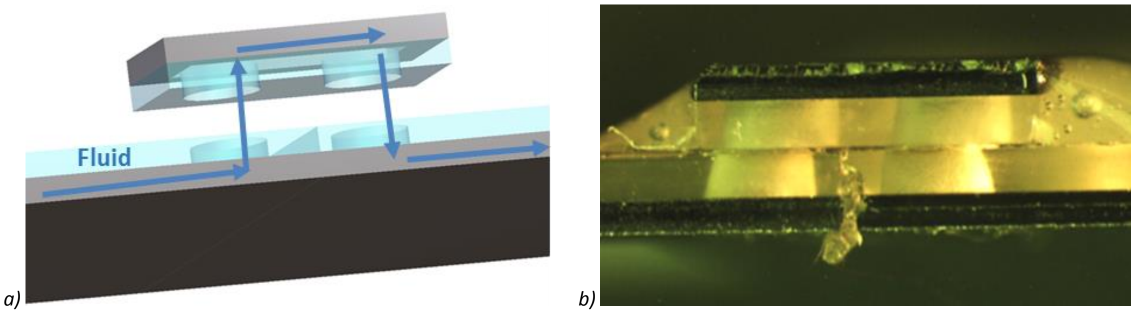


Figure 5.58: Scheme (a) and picture (b) of the “bridge” connector to transfer the fluid from one cooling plate to the other (Ref. [26]).

6 INTEGRATION OF THE COOLING DEVICE IN THE NA62 GTK MODULE

After the study of the interfaces for the mechanical integration of a micro-channel device inside a particle detector, discussed in the previous chapter (*Chapter 5*), a complete mechanical assembly procedure has been developed for the GTK detector of the NA62 experiment. The first micro-channels cooled station was installed in the NA (North Area) cavern of the SPS accelerator in December 2014. A detailed description of the assembly procedure done for the installation in the experiment is described in this chapter.

The micro-channel devices installed in the cavern are fabricated by the CEA LETI company in Grenoble [23]. The micro-channels are delivered to CERN directly from the cleanroom and the assembly procedure is divided in different steps until the final installation. First the stainless steel tubes for the cooling fluid are prepared and laser welded to the Kovar connectors, then the fluidic connectors are soldered on the silicon surface. Before proceeding further, the micro-channel device and the soldering are leak tested. Then a full fluidic qualification campaign takes place to validate the micro-channel plate before the gluing of the detector. The gluing of the detector with the 3M double side tape requires a precise mechanical tool. After gluing, the assembly needs to be fixed to a PCB with mechanical clips and perfectly aligned to the wire-bonding pads on the PCB. After the wire-bonding the module is ready to be tested electrically and again fluidically before the installation in the vacuum vessel of the cavern.
At the end of the assembly procedure the full NA62 module looks like in *Figure 6.1* where a 3D model of the module is shown.

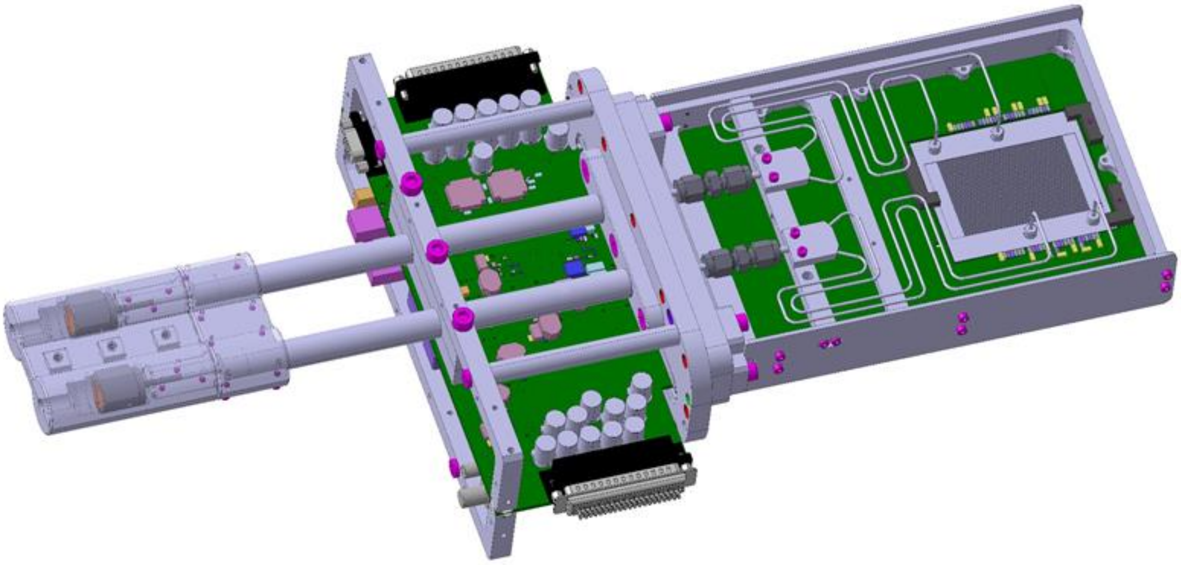


Figure 6.1: 3D model of the NA62 GTK module fully assembled.

6.1 TUBES PREPARATION

The tubes bringing the cooling fluid to the micro-channels are stainless steel capillaries of 1.6 mm external diameter that have to be laser welded in the Kovar connectors. The tubes will be parallel to the PCB and they will be fixed to the feedthrough flange of the PCB. In order to avoid mechanical stresses on the micro-channels transmitted by the deformations of the tubes during the thermal cycles in operation, it is necessary to find a way to absorb the mechanical stresses. After several tests, a solution was proposed consisting in bending the tubes several times in order to act as a spring during the thermal cycles absorbing all the stresses.

After the laser welding with the Kovar connectors, the tubes are bent using a special "bending jig" that uses brass wheels to perform each curve. The jig is composed by an aluminium plate, where the wheels for the bends are fixed. During the bending, the tube is guided on one side by the brass wheel and on the other side by a sliding brass pad. The two parts, the wheel and the sliding pad, are manually controlled and moved by a rotating arm. In *Figure 6.2 a* it is possible to see the jig used to bend the tube number 4 with the detail of a bending phase using the brass wheel and the brass pad (*Figure 6.2 b*). After one bending is done the tube is fixed to the aluminium sheet with small "bridges" 3D printed in ABS material (black blocks in the picture) that are screwed onto the Al plate, as can be seen in *Figure 6.2 a* where the complete tube is bent and fixed to the plate.

The micro-channel plate chosen for the first installation in the NA62 experiment, is the *baseline* solution (see *Chapter 4*) that presents two fluidic circuits with 77 channels each. Each circuit has one inlet and one outlet for the fluid and so on the micro-channel plate there will be soldered four connectors. The four tubes are all bent in a different way, in such a way to create a matching structure to compensate the mechanical stresses. Each tube needs a different bending jig. In *Figure 6.3* the four tubes are shown after bending.

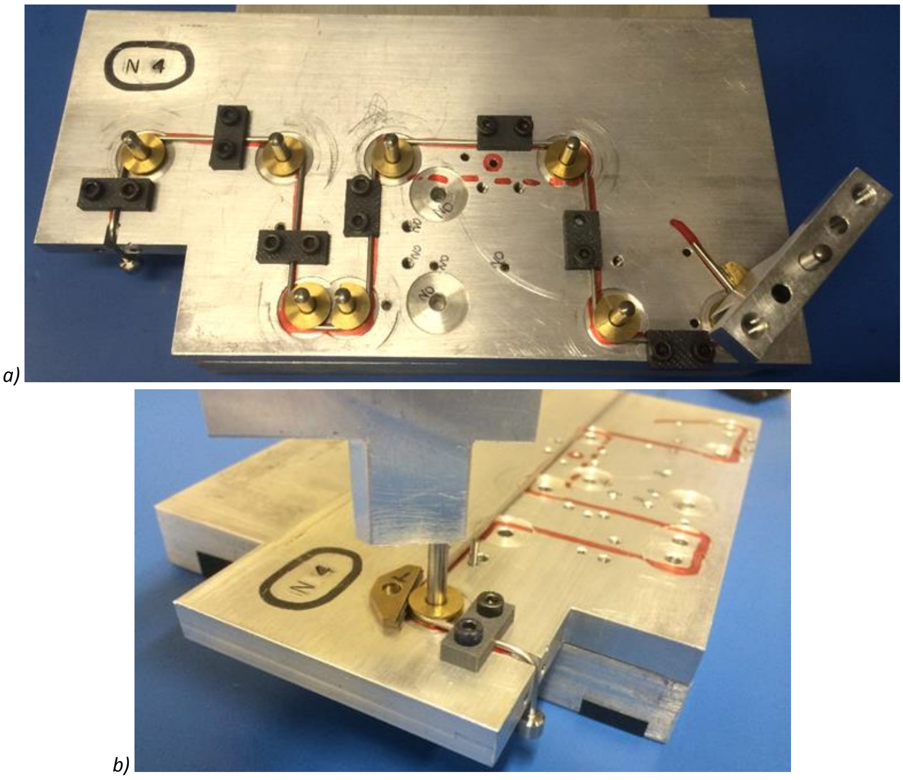


Figure 6.2: Bending jig for a stainless steel capillary (a) and detail of a bending (b).

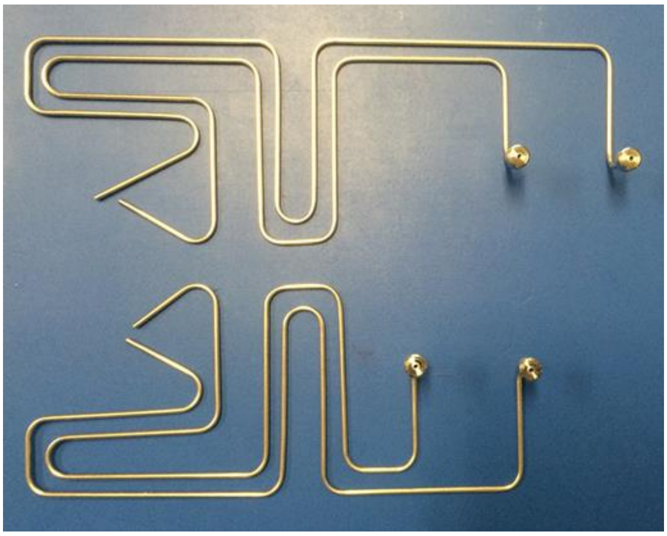


Figure 6.3: Four stainless steel capillaries after bending.

On the opposite side of the connectors the tubes have to be joined to two larger tubes, 1/8’’ of external diameter, that pass through the feedthrough flange for the outlet and the inlet of the fluid. In order to make a connection as small as possible, specific stainless steel manifolds are machined and brazed to the tubes. Each manifold is laser welded to a segment of 1/8’’ stainless steel tube connected to a standard Swagelok union (*Figure 6.4*).

To join the two capillaries on the other side of each manifold, the Nicrobraz brazing technique is used. Nicrobraz is a nickel-based brazing filler metal, patented by Wall Colmonoy [83] used for high temperature brazing alloys. The Nicrobraz is applied as a paste around the capillaries inserted in the manifold body. In order to have an aligned and precise brazing with the Kovar connectors placed in the correct position required by the micro-channel device, another mechanical jig has been developed (*Figure 6.5 a*). The jig is composed by a stainless steel plate, where the manifold and the Kovar connectors are fixed. Due to the high temperature process (brazing temperature 800 °C), stainless steel has been chosen as material for the jig to reduce the expansion compared to an aluminium plate. In order to avoid a local melting of the manifold and the tubes in contact with the steel plate, several ceramic inserts are placed on the jig. Ceramic has a higher melting temperature so the risk of bonding due to the brazing temperature is avoided. In order to guarantee that the Kovar connectors and the manifolds are fixed during the brazing process mechanical clamps are used. The clamps are made with a ceramic piece and a molybdenum spring is used to keep them in place (*Figure 6.5 b*).

a) *b)*

Figure 6.4: Exploded view (a) and picture (b) of the stainless steel manifold with Swagelok connector, 1/8'' tube, and capillaries.

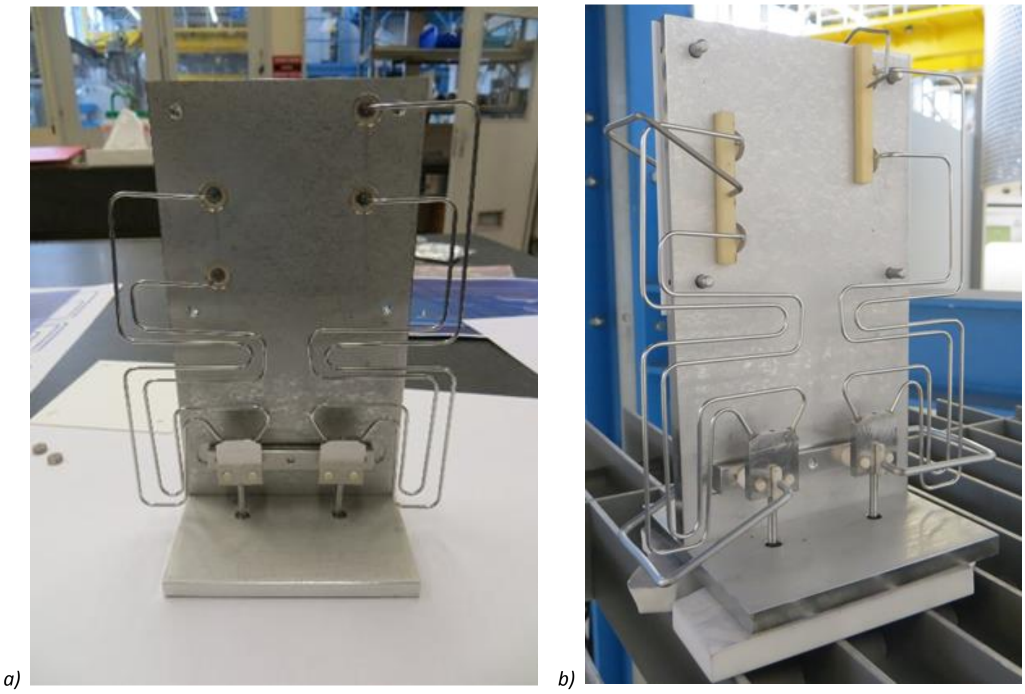

a) b)

Figure 6.5: Mechanical jig to braze the manifolds to the capillaries with ceramic inserts (a) and ceramic-molybdenum clamps (b).

The result of the Nicrobraz process is shown in *Figure 6.6*, with the four capillaries brazed to the two manifolds (*Figure 6.6 a*) and with a details of the brazed connection (*Figure 6.6 b*).

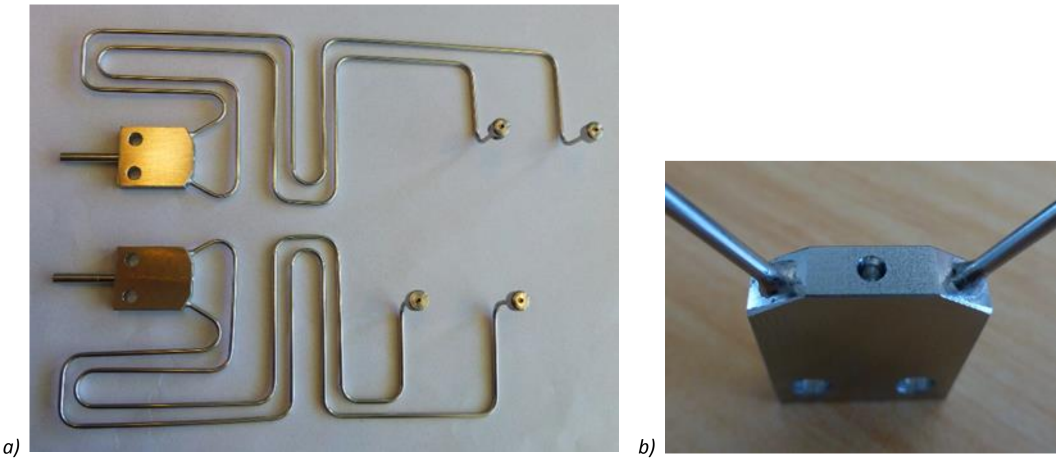

a) b)

Figure 6.6: Brazed connection between the manifolds and the capillaries: general view (a) and detail of the brazing (b).

6.2 CONNECTOR SOLDERING

After the tubes are bent and connected to the manifolds, the soldering of the Kovar connectors takes place. The micro-channel device is delivered from the cleanroom with the metal deposition around the holes for the soldering of the connectors (*Figure 6.7*). The metal layers deposited for the final production are 200 nm of titanium, 350 nm of nickel and 100 nm of gold.

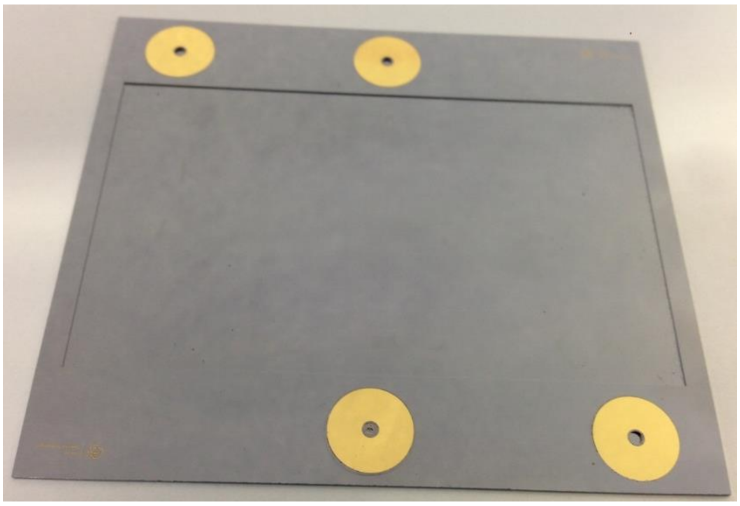


Figure 6.7: NA62 micro-channel device before the Kovar connectors soldering.

To perform the soldering of the Kovar connectors a third dedicated jig has been designed. The jig has the function to keep the connectors aligned with the metal pads on the silicon and to guarantee the planarity and the contact with the silicon. The micro-channel device is inserted in a pocket machined on the jig surface. The stainless steel manifolds are screwed on a support bar. As already seen in *Chapter 5*, the Kovar connectors present, on the bottom part, a small pin to be inserted inside the aperture in the silicon. In this way the alignment between the entrance of the fluidic circuit and the connector is guaranteed. In order to keep the connector in place a mechanical clamp is used. The clamp is made by a graphite piece that surrounds the connector and a molybdenum spring that applies the load on it. The interface between the graphite and the molybdenum spring is obtained with a stainless steel piece to avoid the molybdenum to break the graphite at high temperatures. Before placing the clamps in position, the soldering wire is inserted around the Kovar connectors. For the final soldering of the GTK connector three overlapping wires are used with a wire diameter of 0.5 mm. In *Figure 6.8* it is possible to see a complete assembly of the micro-channel plate and tubes fixed on the soldering jig (*Figure 6.8 a*) with a detail of the mechanical clamp acting on the Kovar connector (*Figure 6.8 b*). The soldering result, with the micro-channel plate soldered to the four Kovar connectors and the tubes, can be seen in *Figure 6.9*.

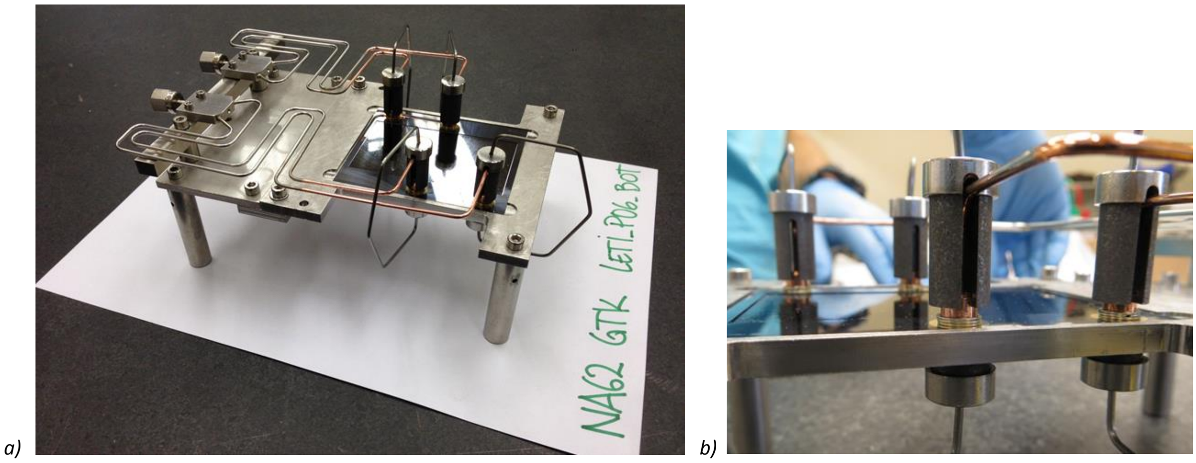


Figure 6.8: NA62 micro-channel device during soldering of the connectors (a) and detail of mechanical clamps (b).

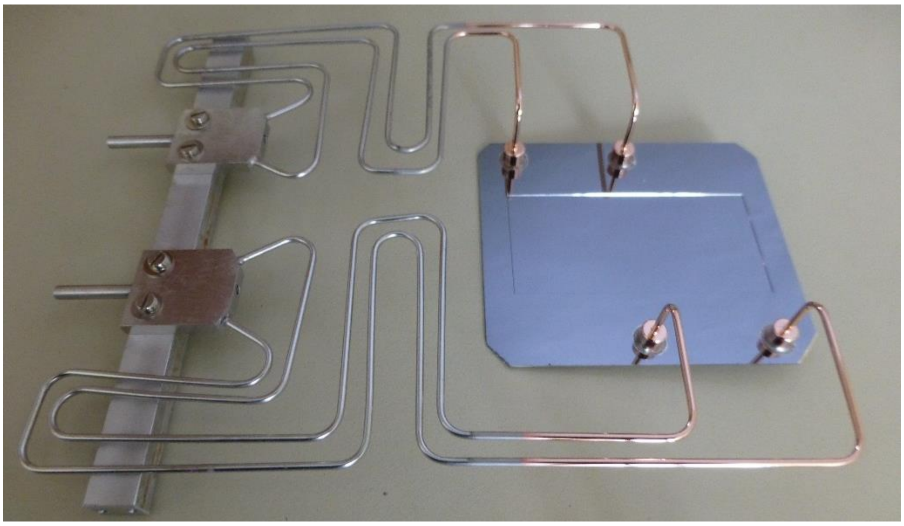


Figure 6.9: NA62 micro-channel device after the soldering of the connectors.

6.3 PCB-COOLING PLATE INTERFACE

The GTK PCB, for the electrical connections inside the vacuum vessel and for the cooling system support, has been designed by the PH-ESE group at CERN, produced by the Eltos company [84] and is then equipped with all electrical components by the EMD lab at CERN. After the soldering of the electrical components the PCB structure is reinforced with a metallic frame that is screwed to the PCB edges. A stainless steel flange is glued on the two sides of the PCB to be inserted in the vacuum vessel flange. The stainless steel manifolds are fixed to the metallic frame as well as the two tubes for the vacuum flange feedthrough. The micro-channel cooling plate is inserted in a pocket etched in the back of the PCB, in such a way that, on the front side of the PCB, the wire-bonding pads of the read-out chips are perfectly aligned with the wire-bonding pads on the PCB. The cooling plate is kept in position inside the pocket by three 3D printed mechanical clips.
To avoid a rigid contact between the PCB and the micro-channel plate, thin elements of polymeric material are glued inside the PCB pocket. The polymeric material has the double function of acting as a spring between the PCB and the silicon and absorbing the thermal stresses while also avoiding the sliding of the cooling plate inside the pocket. The cooling plate has to be as stable as possible in position to avoid the damaging of the wire-bonds and to guarantee the desired precision with respect to the particle beam. Furthermore the cooling plate should not be glued to the PCB to avoid mechanical stresses due to CTE mismatches between the two materials. For this reason a polymeric material to act as a soft glue and a stress absorber is chosen. The polymeric material has a maximum allowed thickness of 0.4 mm, given by the maximum vertical gap that the wire-bonds can cover.

In order to choose the best suitable polymeric material, four different materials have been investigated and radiation tests have been performed on them. The selected materials are an epoxy glue, a polyurethane, an EPDM and a silicone. The epoxy glue is the two components Duralco 4538 from Cotronics Corporation [85] with a very high flexibility and a severe thermal cycle resistance. The EPDM material is a foamed flat profile from Angst and Pfister [86] that has already been used in other detectors of the NA62 experiment. The polyurethane material is a two components, RE 11501A polyol and RE1020 isocyanate, resin from Axson Technology [87] already used at CERN in contact with electrical components. The silicone is the RTV8335 liquid two-component silicon rubber from Sinus

Electronic [88] that can be diluted with a silicon oil to obtain the desired softness and that was already used inside the CMS experiment at CERN.

Several specimens have been realized with the four materials following the standard UNI EN ISO 527-3. After mixing the two components, the materials are poured in a pocket machined in an aluminium plate. The pocket is 2 mm deep and the materials are cured for the required time. After the polymeric sheet is cured and detached from the aluminium base, the sample are cut out from the polymer sheet using a mould with the dimensions shown in *Figure 6.10*.

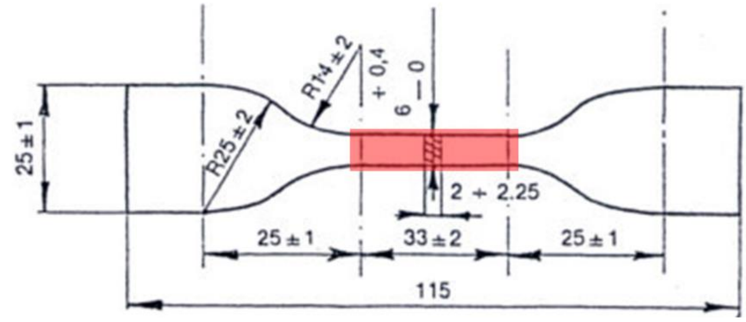
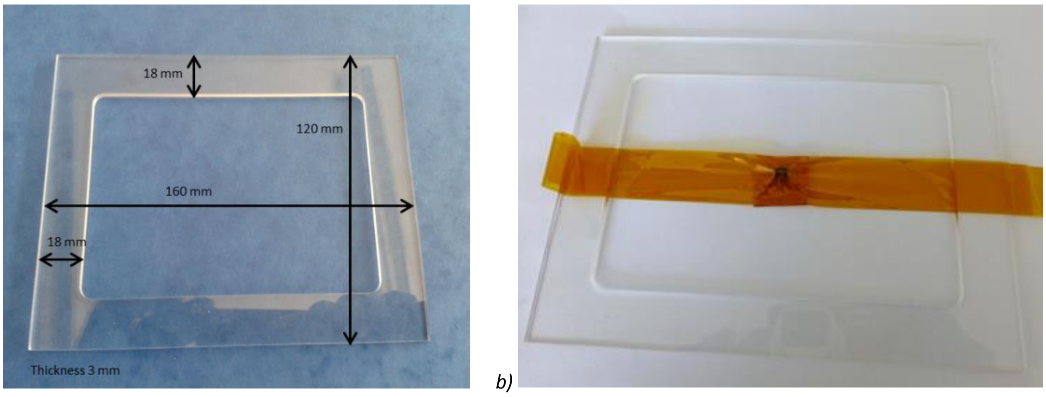


Figure 6.10: Dimensions of the specimens of polymeric materials for tensile tests.

To evaluate the polymer reaction to radiation exposure, the samples have been sent to irradiate at the high flux neutron and proton irradiation facility of Louvain-La-Neuve Cyclotron in Belgium. The selected radiation levels are the same chosen for the glue tests: the nominal radiation level for the NA62 experiment, with a value of 1 x 10^{14} MeV eq.neutron/cm^2 and a lower and a higher level with values of 3 x 10^{13} MeV eq.neutron/cm^2 and 1 x 10^{15} MeV eq.neutron/cm^2. Seven samples of each polymer have been exposed to each radiation level. The samples are exposed at the same time but, in order to obtain different intensities they are positioned at a different distance in the beam axis. The irradiation test stand looks like in *Figure 6.11* where the beam is coming from the front and all the samples to be tested are placed one after the other in a line and inserted inside the Plexiglas structure.

Figure 6.11: Louvain cyclotron irradiation test stand.

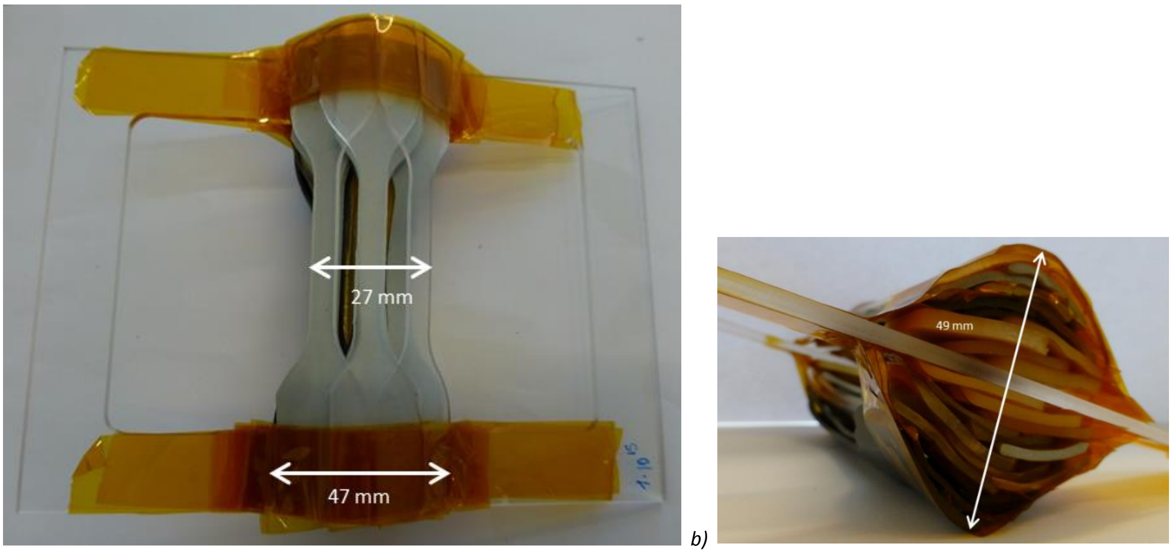
In order to fix the specimens in the irradiation test stand, Plexiglas frames have been machined following the facility requirements (*Figure 6.12 a*). The sample are fixed on the Plexiglas frame with kapton adhesive tape. At the centre of each frame a small diode is fixed to precisely measure the radiation received by the samples in the three cases. Also the diode is fixed with kapton tape (*Figure 6.12 b*).



a) *b)*

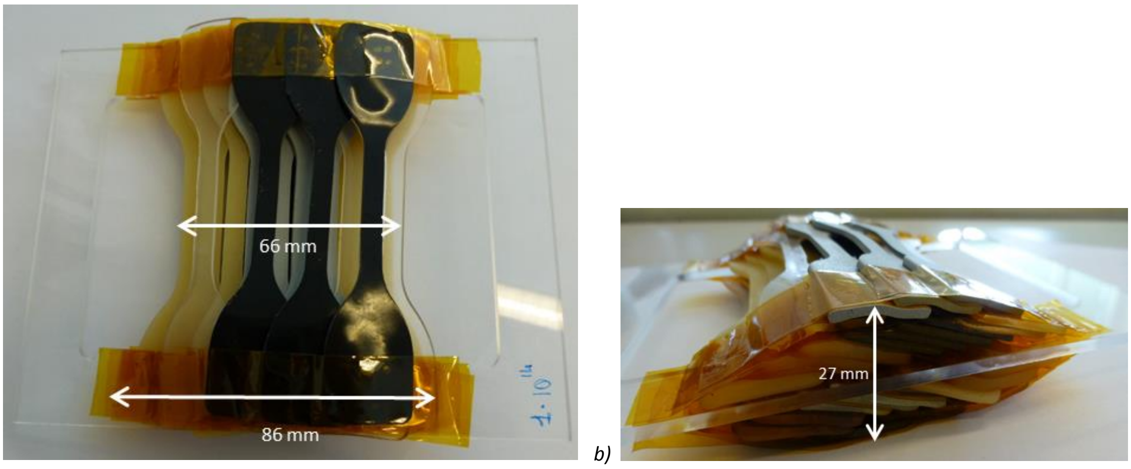
Figure 6.12: Plexiglas frame structure used to fix the samples (a) and diode at the centre of it (b).

The polymer specimens are fixed on the frame with different overlapping percentages depending on the radiation level. Each Plexiglas frame, for a specific radiation level, must be placed at a precise distance from the starting point of the beam. The beam structure is a conical shape increasing the diameter while moving away from the vertex. The frame targeting the highest radiation level among the three is placed at 10 cm from the vertex, where the beam radius is of 3 cm. The one for the nominal NA62 radiation level is placed at 32 cm from the vertex with a radius of 6 cm, and the last one, for the lowest radiation, is placed at 82 cm from the beam vertex with a corresponding radius of 10 cm. For this reason the specimens are spaced on the three frames with different overlapping in such a way to best cover the beam area. The specimens for the higher radiation level are focused in an area of 3 cm in the centre of the frame (*Figure 6.13*), the specimens for the nominal radiation level are focused in an area of 6 cm (*Figure 6.14*), while for the lower radiation level the specimens are spread in a wider area of 10 cm (*Figure 6.15*).



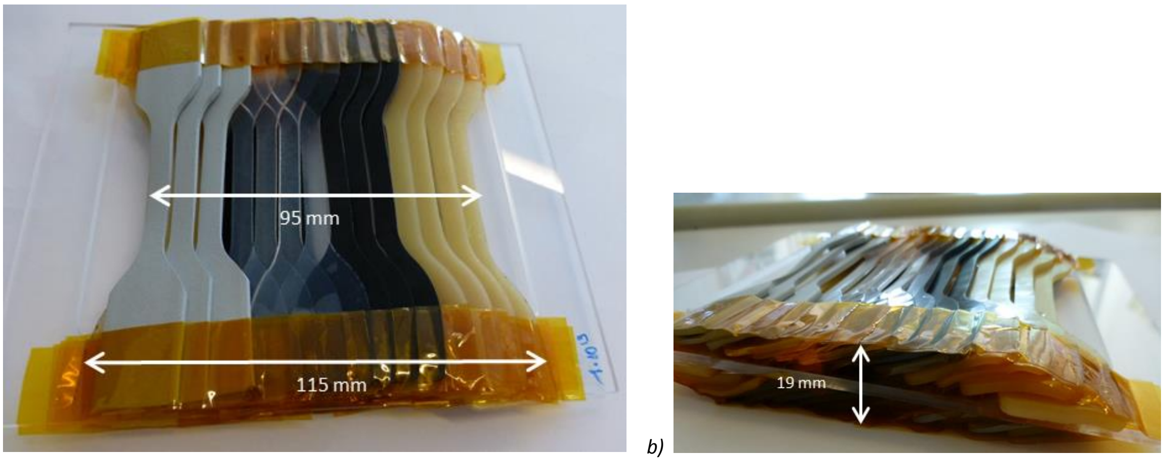
a) *b)*

Figure 6.13: Plexiglas frame structure with the highest radiation level (beam area of 3 cm) front (a) and side (b) pictures.



a) b)

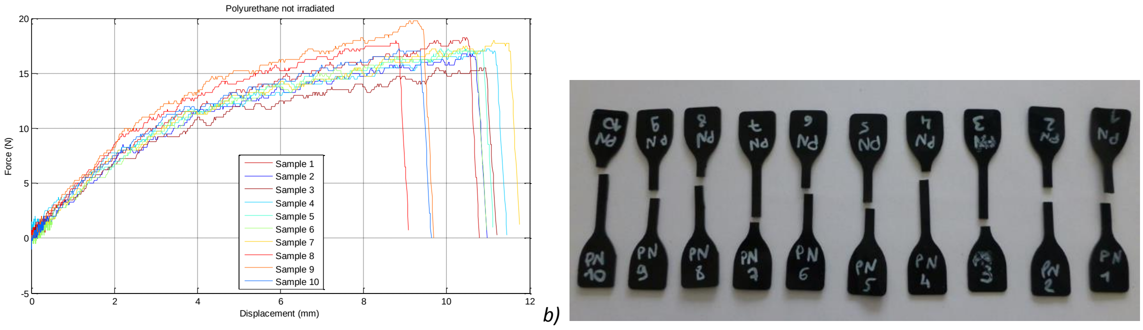
Figure 6.14: Plexiglas frame structure with the nominal radiation level (beam area of 6 cm) front (a) and side (b) pictures.



a) b)

Figure 6.15: Plexiglas frame structure with the lower radiation level (beam area of 10 cm) front (a) and side (b) pictures.

After the irradiation, the diodes have been measured and the values confirmed the target radiation levels. All specimens have been tested with a tensile test machine inside the DIME (Dipartimento di Ingegneria meccanica, energetica, gestionale e dei trasporti) of the University of Genoa. For each polymer also seven non-irradiated samples were tested in traction. For each tested sample a load-displacement curve was obtained and for each family of specimens the average curve and the average breaking point was found. In *Figure 6.16 a* it is possible to observe a family of load-displacement curves for the polyurethane not-irradiated (where more than seven specimens are tested in traction), and a picture of the samples after testing is also show in *Figure 6.16 b*.



a) b)

Figure 6.16: Load-displacement curve for the polyurethane not-irradiated samples (a) and picture of the tested specimens.

None of the tested polymers is affected significantly by the irradiation, but some are showing little variations in the behaviour under test.

After all polyurethane specimens were tested, a graph with the four average load-displacement curves and the crosses corresponding to the four average breaking points, was produced (*Figure 6.17*). In the graph it is possible to see how with the increasing of the radiation level the curve is slightly modified, going to lower loads and larger displacements.

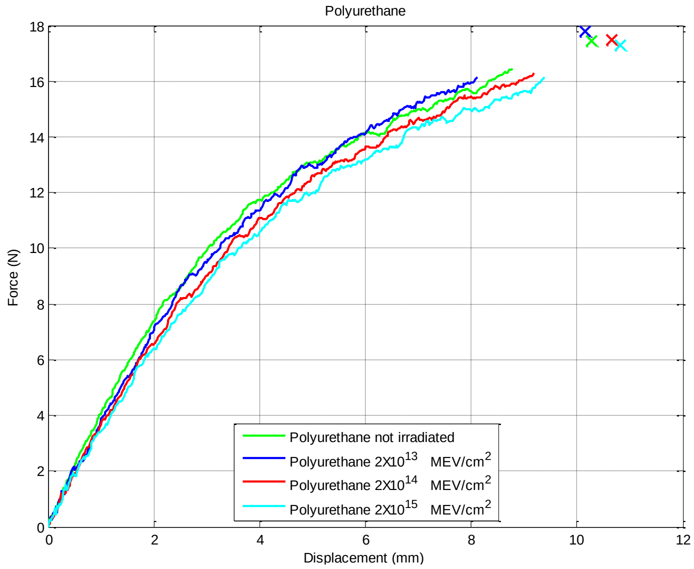


Figure 6.17: Average load-displacement curves for the polyurethane samples in the four radiation levels.

Looking at the comparison graph for the silicone specimens (*Figure 6.18*), it is possible to see how the silicone becomes more rigid with the increment of radiation. The silicone displacement values are in general around three times higher than the ones of the polyurethane. The average breaking displacement is decreasing with the increasing of radiations.

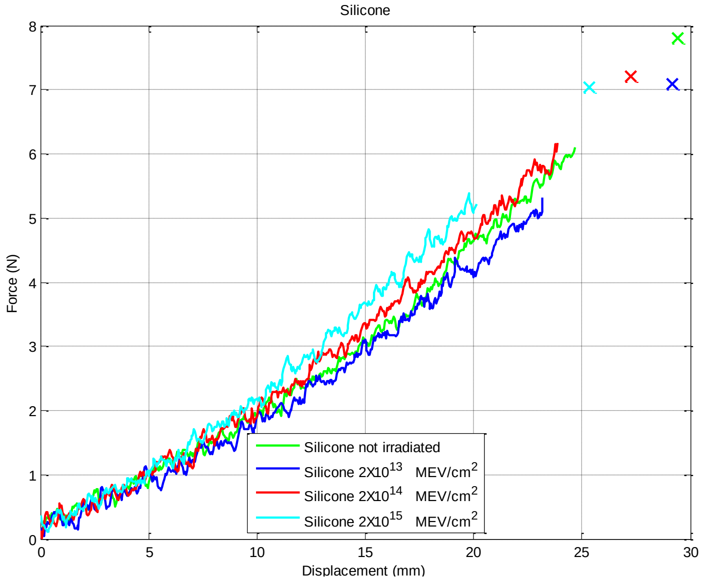


Figure 6.18: Average load-displacement curves for the silicone samples in the four radiation levels.

The specimens made with the epoxy glue were sticky and too flexible even after irradiation. The glue was not completely polymerized and it was attached to the Plexiglas frame and to the other samples even if the required curing time and temperature had been followed. In the comparison graph (*Figure 6.19*) the load-displacement curve is increasing in load with the increasing radiation level (an indication of post-curing effect).

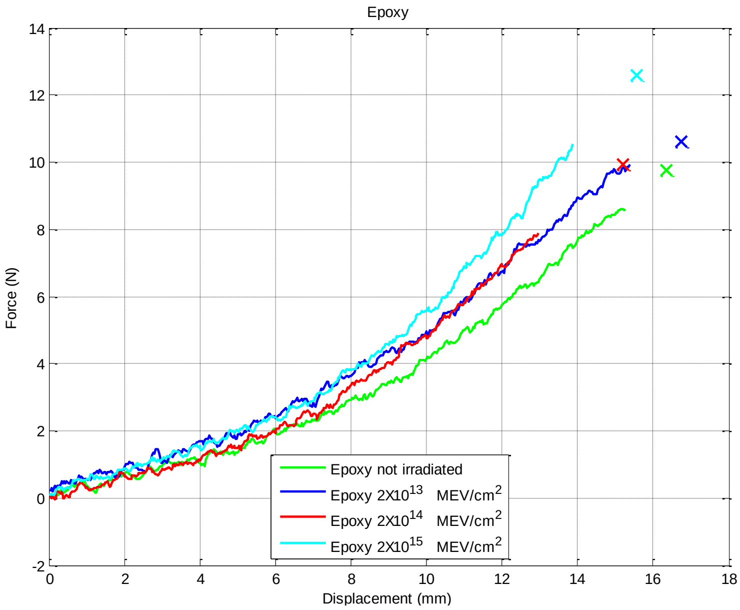


Figure 6.19: Average load-displacement curves for the epoxy samples in the four radiation levels.

Finally for the EPDM specimens it is possible to see how the radiation did not affect at all the behaviour of the material (*Figure 6.20*).

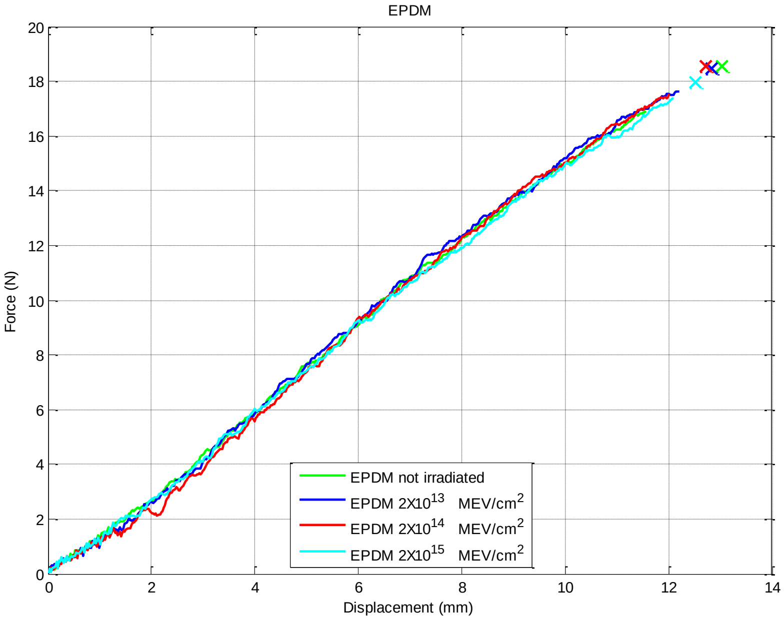


Figure 6.20: Average load-displacement curves for the EPDM samples in the four radiation levels.

In the graph of *Figure 6.21* it is possible to appreciate the totality of the tests made with the four different materials.

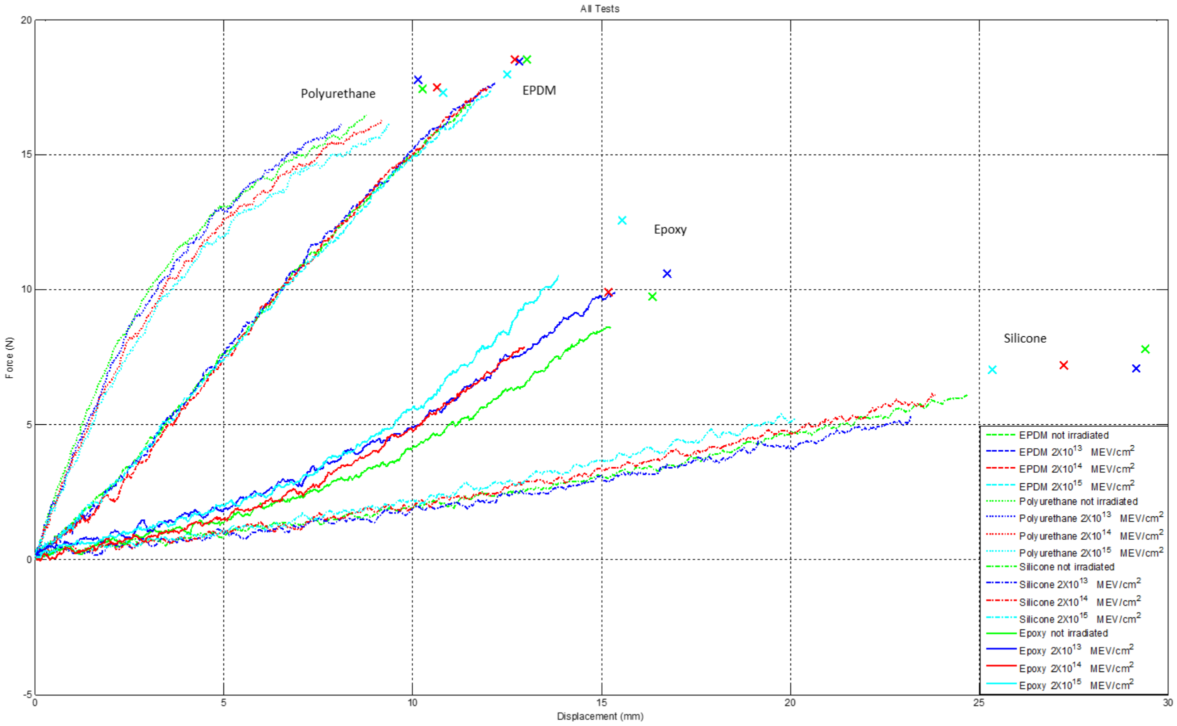


Figure 6.21: Different behaviour of load-displacement curves for the polymeric materials in the four radiation levels.

As already observed, all materials are not much affected by the irradiation. The two materials that show a bigger influence of the radiation are the silicone and the epoxy. Between the other two, the polyurethane material is selected to be used for application in the NA62 experiment. This choice is dictated by the results of the irradiation tests in addition to the low outgassing properties of the material, the easy preparation procedure and its availability in the CERN polymers laboratory.

Three round pads are cut out from a 0.4 mm thick polyurethane sheet and are glued on the back of the PCB on the pocket surface in correspondence with the mechanical clips. In this way the clips are forcing on a supported area of the cooling plate. In *Figure 6.22* it is possible to see the back of the PCB with the polyurethane pads glued inside the yellow pocket.

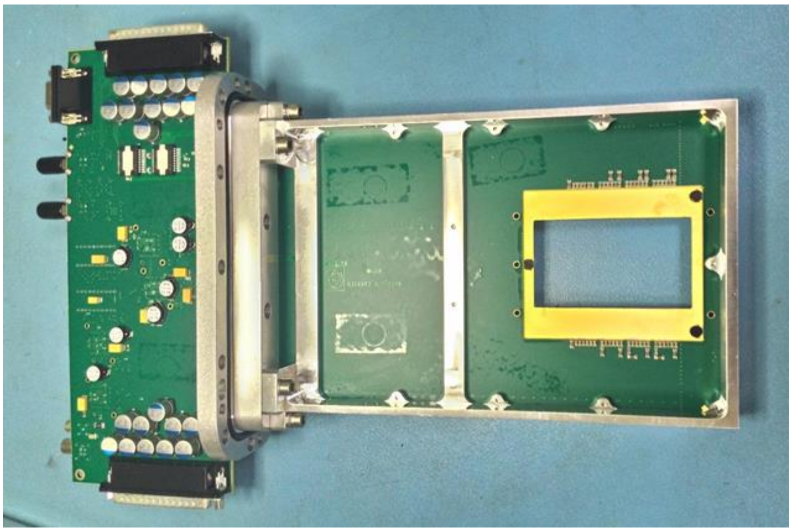
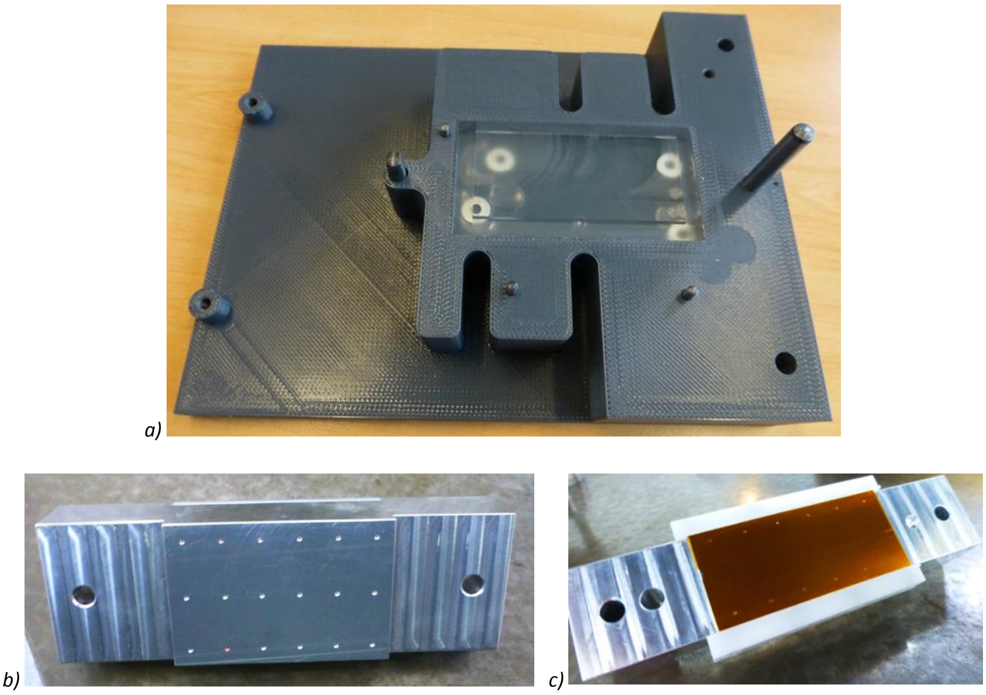


Figure 6.22: Back of the PCB with the three black polyurethane pads glued in the PCB pocket.

Before fixing the cooling plate to the PCB, fluidic tests on the micro-channels after the soldering of the connectors are executed. Each micro-channel plate is tested for at least 14 hours before being validated. The test are done in a vacuum vessel with C_6F_{14} in liquid phase. Several cycles with different fluid temperatures and mass flows are performed. During a cycle the temperature goes from ambient temperature to -25 °C while the mass flow starts from 0 g/s to 3.5 g/s.

6.4 DETECTOR GLUING

After a micro-channel plate is tested, the detector can be glued on top using the 3M double side tape. The gluing requires a mechanical jig to assure the required precision and repeatability. The bottom of the mechanical jig is 3D printed in ABS. The central part, where the micro-channel plate is in contact with the jig, is made in Plexiglas, glued inside the 3D printed structure, and machined precisely afterwards to guarantee a high planarity of the surface (*Figure 6.23 a*). Two other metallic parts are needed to perform the gluing: one to correctly position the tape (*Figure 6.23 b*) and the second one to align the detector (*Figure 6.23 c*). Both pieces are aligned with the 3D printed bottom piece through alignment pins and they are holding the tape and the detector using small vacuum suckers achieved by holes machined in the structure.


a)

b)

c)

Figure 6.23: Mechanical jig used to glue the detector on the silicon micro-channels: bottom part 3D printed in ABS (a), and two metal top parts for the double side tape (b) and for the detector (c).

The micro-channel plate with the tubes is positioned on the jig with the pool of the micro-channels in contact with the Plexiglas part. The tape is cut in the correct dimension and is taken by the specific metal part of the jig with vacuum suckers. The piece carrying the tape is inserted on the alignment pins and is glued in the pool. After gluing in the micro-channel plate pool, the metal counter-piece is removed and the exposed protection paper is removed from the 3M tape. The detector is taken with the third part of the jig and using the alignment pins is deposited on top of the tape (*Figure 6.24*). After the gluing a small pressure is applied and the top jig is removed. In *Figure 6.25* it is possible to see the result of the gluing of the first NA62 detector. The white part in the picture is the silicon sensor while the ten read-out chips are the gold chips sticking out from the sensor.

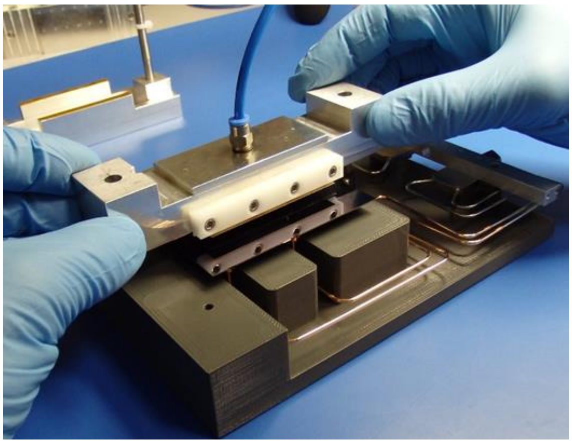


Figure 6.24: Detector gluing on the micro-channel plate using the metal part with vacuum holders.

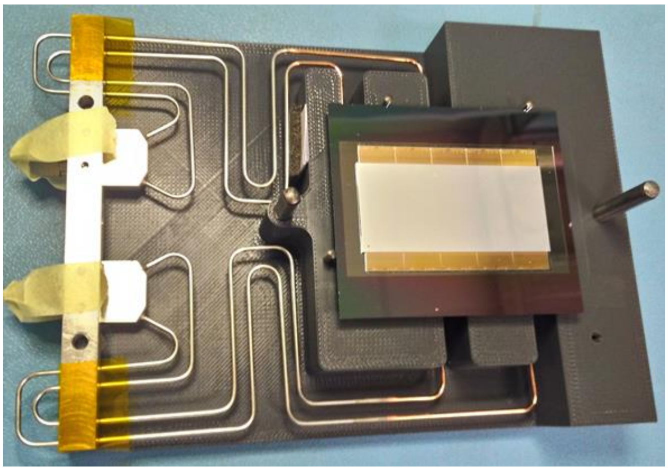


Figure 6.25: First gluing for NA62 of the detector to the micro-channel cooling plate.

6.5 PCB ALIGNING AND WIRE-BONDING

After the gluing of the detector, the cooling plate with the tubes is ready to be fixed to the PCB. The mechanical clips to fix the cooling plate are screwed on the PCB and they guarantee the good alignment of the wire-bonding pads. The stainless steel manifolds are fixed on the PCB metallic frame. In order to achieve the perfect alignment between the bonding pads a precision camera is required with micrometric screws to adapt the position of the micro-channel plate. A mechanical jig is built for this purpose. The jig has four columns to lift the PCB and guarantee an access from below, in addition it has also a lower central part, made of micrometric screws with a vacuum jig to hold the micro-channel plate and moving it according to the required position. The jig, with the PCB fixed to the four columns and the central part for the movement of the cooling plate, can be seen in *Figure 6.26*.

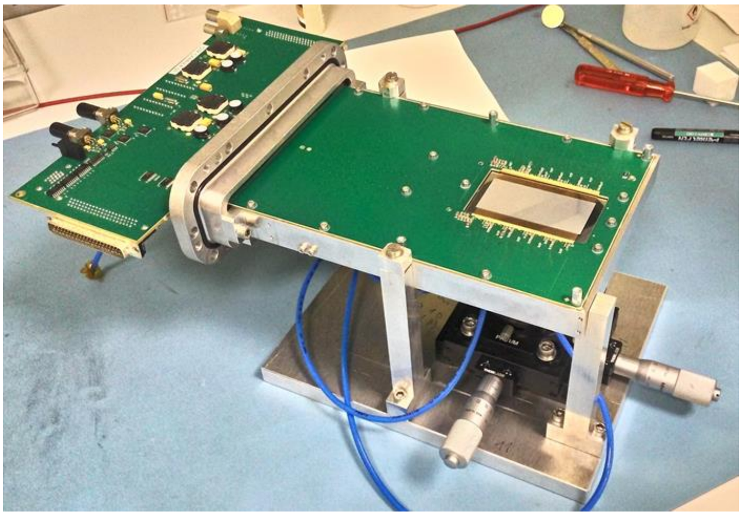


Figure 6.26: Mechanical jig for the alignment of the cooling plate to the PCB wire-bonding pads.

The alignment is performed under a precision camera SmartScope CNC 250 and, once in position, the mechanical clips are fixed. The PCB is then unscrewed from the columns and it is placed on a flat surface to go under the wire-bonding machine. In *Figure 6.27* it is possible to see when the wire-bonds are done between the pads of the detector and the pads of the PCB with the machine Devoltec 6400 by the CERN PH-DT bond lab.

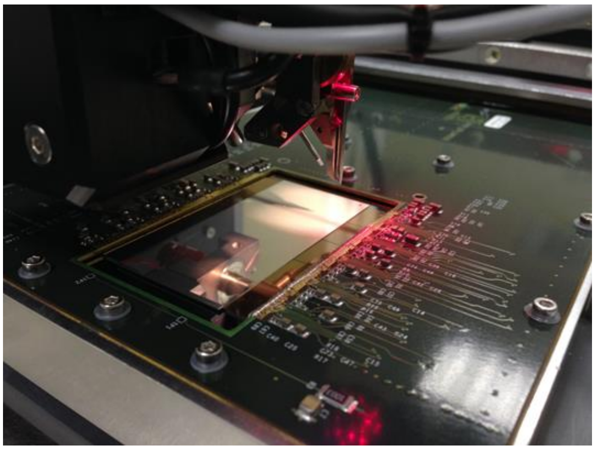


Figure 6.27: Wire bonding machine during the wire-bonding process for the NA62

After the wire bonding, electrical and thermal tests are executed to validate the electronics before the installation in the cavern. The first NA62 GTK module with micro-channel cooling was installed in the north area cavern in December 2014. In *Figure 6.28* it is possible to see the insertion of the first PCB module inside the experiment vacuum vessel.

Figure 6.28: Insertion of the first NA62 GTK module in the vacuum vessel in the cavern.

7 CONCLUSIONS

The first applications of micro-channels cooling systems used for the thermal management of tracking detectors have been presented in this work. After the first application in the cooling of electronics devices, this technology has been considered for its outstanding performances applied to the specific cooling of particle detectors.

Particle detectors have heavy requirements for their thermal management systems: a very good thermal efficiency, a low mass and a high stiffness. So far cooling systems based on metal pipes circulating a cooling fluid, interfaced to the detector with a thermal layer have been used in the detectors at CERN. The proposed silicon micro-channels solution presented in this work, largely satisfy all the particle detector requirements in terms of cooling, thermal efficiency, mechanical structure and support.

Silicon, as a structural material, has a very good thermal conductivity and for this reason is suitable for the cooling of particle detectors. Furthermore, the silicon micro-channel devices are very well suited for fabrication processes based on standard micro-fabrication techniques. The fabrication process has been presented and discussed in details in *Chapter 2.* The process starts with the photolithography of the channels design on the wafer surface, then the channels are DRIE-etched and they are closed with a wafer bonding. The holes for the fluid circulation are finally etched on the silicon surface. The process steps are presented in details and the main problems found during the fabrication are analysed. In particular, the more critical step of the fabrication process resulted to be the bonding of the cover wafer to close the channels. Several tests done show a huge difference in the device performances according to the good or the bad bonding of the device. An in-house method based on the destructive test of small single-channel devices has been developed to test the anodic and direct bonding quality.

In addition to the good thermal conductivity, silicon also presents good mechanical properties. However, since silicon is also a very fragile material, it is necessary to carefully determine the maximum internal pressure that a micro-fabricated device can sustain during operation. The cooling fluid can reach high pressures inside the micro-channels and induce the device rupture. Due to the lack of studies in literature, a tentative prediction method is proposed in *Chapter 3*. A deep study is conducted on the maximum pressure that a channel, or a structure with a fixed design, can hold, by taking into account the silicon thickness on top and below the channels. A specific pressure test stand has been built to be able to test in pressure with demineralized water the micro-channels devices. According to the parameters under tests, different specimens design have been designed. Preliminary results have been presented and discussed.

For future improvements on the subject it is necessary to study a correlation between the maximum pressure that a channel can hold and the silicon membrane internal strength. In addition to the mechanical pressure tests, a FEM analysis as well as a simulation method will be developed.

Following the high performance of the heat transfer in micro-channels, well detailed in literature, several thermal and fluidic studies of single and two-phase flow in micro-channel devices have been presented in *Chapter 4*. Different micro-channel designs have been shown for each experiment interested in the technology.

For the NA62 experiment two different channel designs have been proposed for the cooling of the GTK stations. A baseline solution, where the channels are distributed below the sensor, has been extensively tested with C_6F_{14} in single-phase flow. A “frame geometry” solution has been also proposed as an alternative solution for the experiment. Silicon dummy heaters are used to simulate the power of the real detectors and to prove the cooling performances during the test phase. Thermal pictures have been shown to compare the two cooling proposals. The baseline solution has been finally selected for operation in the NA62 experiment.

Thermal test with temperature sensors and thermal pictures have been shown also for the cooling test executed on a FEI4 chip used in the ATLAS experiment. Successful initial cooling tests, using dummy heaters, have been performed with a CO_2 two-phase flow circulating inside silicon-silicon and silicon-Pyrex micro-channel devices. A testing phase with a real FEI4 chip is started and a good cooling has been already achieved, fulfilling the detector requirements. Further tests will be done on this device in order to understand better the sensor surface temperature and the cooling performances after irradiation of the chip.

Successful thermal tests have been also presented shortly for the LHCb VELO detector using CO_2 in evaporative flow, and for the ALICE ITS detector using C_4F_{10} in two-phase flow.

For general research studies, a new setup for fluidic tests in single phase and two phase flow is used in Manchester University. The setup and the first test for the thermocouples calibration have been described. Future tests will be conducted to better understand the CO_2 behaviour in small capillary tubes.

Regarding the mechanical structure of the cooling devices, it should be as stiff as possible in order to guarantee precise measurements from the sensor while being very light to minimize the particle interaction. Furthermore the cooling structure is obliged to follow the external constraints of the experiment structure itself. The mechanical integration is the process of the installation of the cooling structure inside the detector assembly. The process is fully described inside *Chapter 5*.

The mechanical integration starts from the definition and optimization of the interface of the cooling device with the external word: the first step is the equipment of the cooling plate with the fluidic connectors. Several models of fluidic connectors, commercial or in-house solutions, have been described and tested. The best solution for the connection is the soldering of the connector on the micro-channel plate. Among the soldering connectors two solution have been the selected ones: the Kovar connector to be installed inside the experiments, and the ferrule-based connector to be used for tests done in the laboratory. A new generation of in-plane connectors and 3D printed solutions have been presented for future developments.

The second interface, the glue choice for gluing the detector on the micro-channel plate, is a very crucial point of the integration process. Several glue types have been presented and tested with shear test, irradiation test or visual test. The glue has to guarantee a good and continuous contact, no air bubbles, and it should not spread outside the gluing area. The glue choice is well dependent by the detector configuration, so different glues can be selected for different experiments. For the NA62 experiment the selected glue is a double side tape, while for the ATLAS chip a two components liquid glue is chosen.

The mechanical integration has to take into account also other elements like, the tubes for the cooling fluid, the mechanical frame around the cooling system, mechanical supports. Some examples of mechanical integration problems and the corresponding solutions adopted are also presented.

As final chapter of this work, the mechanical integration of the silicon micro-channel device for the NA62 experiment has been described in full details. The cooling system has been installed in the experiment in December 2014. The process starts with the bending of the capillary tubes to guarantee the absence of mechanical stresses, and finishes by the alignment of the wire-bonding pads on the PCB. The detector gluing on the micro-channel plate is a very challenging step: a precise alignment jig is used to align and glue the detector inside the front pool of the micro-channel plate. In order to select the interface material between the PCB and the micro-channels, irradiation and traction tests have been performed on different materials and the best polymer suitable to this application has been chosen.

In this research work, silicon micro-channel cooling are proven to be an efficient and reliable system for the thermal management of particle detectors. The micro-channel systems are gaining more and more interest in this field. Starting with NA62, a micro-channel cooling system has been chosen for the LHCb upgrade in 2018 and other experiments like ALICE and ATLAS are considering it as a cooling solution.

Silicon micro-channels have been proven to guarantee a very good thermal efficiency due to the high thermal conductivity of silicon and the good heat transfer typical of micro-channels. Furthermore they provide a stiff and stable mechanical structure to support the detectors. The fabrication process is done using standard techniques of micro-technologies and the fabrication costs are still low compared to the ones of the silicon detectors used. The first prototypes have been developed, and future improved devices are being planned. On the mechanical integration field future improvements are necessary on the fluidic connectors for the micro-channel plate or in supporting the silicon plate inside the detectors areas. On the thermal exchange, more tests on the heat transfer of CO_2 in small capillary tubes will be performed to better understand and model the properties of evaporation at the microscale. As for the fracture prediction tool a new method should be developed taking into account additional experimental results as well as numerical simulations.

The main future development of the silicon micro-channel cooling system will be to integrate the micro-channels inside the silicon detector structure. The idea is to start with the micro-channel fabrication on a silicon wafer, and when the channels are embedded inside, use the wafer for the detector fabrication as if it was a normal blank wafer. An integrated device with cooling and sensitive area, is the future target for the next years of research on the application of this novel cooling technology.

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