

# Acknowledgments

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# Abstract

Les rayonnements ionisants et non ionisants sont connus pour causer des dommages aux composants électroniques, entraînant une réduction des performances et un éventuel dysfonctionnement. Cela pose un problème majeur pour les applications où l'électronique opère dans un environnement radioactif. Un exemple extrême est le futur projet du Grand Collisionneur de Hadrons à Haute Luminosité (HL-LHC) du CERN, où des doses totales d'ionisation (TID) de 1 Grad(SiO<sub>2</sub>) et des flux de 10<sup>16</sup> particules/cm<sup>2</sup> seront atteints dans les détecteurs de particules après 10 ans d'exploitation.

Ces niveaux de radiation excèdent de plusieurs ordres de grandeur ceux rencontrés dans les applications spatiales, nécessitant une investigation approfondie des effets délétères des radiations sur les technologies CMOS utilisées dans les ASIC pour les détecteurs de particules. A cet effet, cette thèse explore plusieurs sujets qui se rapportent à la qualification des technologies utilisées dans l'électronique des détecteurs du CERN.

Nous présentons les résultats sans précédent de l'inspection systématique de dizaines de puces en technologie CMOS 130-65 nm qui sont habituellement utilisées dans les ASIC développés pour les détecteurs HL-LHC. Cette étude a révélé une variabilité extrême entre les fabricants et les lots pour ce qui est de l'impact de la Dose Totale d'Ionisation (TID). Cette recherche démontre que la variabilité induite par la TID doit être prise en compte dès les phases de conceptions et de qualifications.

Les effets des dommages générés par déplacement ont été étudiés sur deux processus CMOS de 28 nm au moyen d'irradiations par protons et neutrons, jusqu'aux niveaux de flux rencontrés en physique des hautes énergies. L'étude a révélé que la dégradation induite par les radiations étaient liées à la dose totale d'ionisation plutôt que qu'aux dommages induits par déplacement, soutenant que la technologie CMOS de 28 nm est adaptée aux détecteurs de particules.

La sensibilité de cette technologie vis à vis des effets induits par la dose de radiations est également à évaluer. Les preuves d'une Sensibilité Améliorée aux Faibles Dose (ELDRS) basées sur une augmentation du courant de fuite induite par la TID ont été observées dans des oscillateurs à anneau et des SRAMs en technologie CMOS 28 nm. L'irradiation à haute température (ETI) sur des dispositifs isolés permet d'estimer la dépendance de l'ELDRS aux conditions de polarisations et à la taille des dispositifs. Les résultats montrent que l'irradiation à haute température peut s'apparenter à la dégradation induite par une faible dose, offrant ainsi une solution pour réaliser des tests de radiation accélérés.

La réponse aux radiations des transistors MOS en Silicium sur Isolant (FD-SOI) de 22 nm exposés à une TID ultra-élevée a également fait l'objet d'une étude. Celle-ci révèle que les performances sont manifestement affectées par la TID, dominées par la charge piégée dans l'oxyde enterré. Malgré des techniques pour atténuer ces effets indésirables, le FDSOI de 22 nm s'est avéré ne pas être adapté aux applications internes des détecteurs, mais pourrait convenir pour des niveaux de TID plus faibles.

**MOTS-CLÉS:** CERN, HL-LHC, ASIC, technologie CMOS, radiation ionisante, radiation non ionisante, effets de radiation, variabilité de radiation, sensibilité améliorée aux faibles taux de dose (ELDRS), dose totale d'ionisation (TID), dommages par déplacement (DD), applications en physique des hautes énergies, Silicium entièrement épuisé sur isolant (FDSOI).

# Abstract

Ionizing and non-ionizing radiation is known to cause damages in electronic components, resulting in reduced performance and possible failure. This is a major issue for any application where electronics operate in a radioactive environment. An extreme example is the future High-Luminosity Large Hadron Collider (HL-LHC) at CERN, where Total Ionizing Dose (TID) of 1 Grad(SiO<sub>2</sub>) and fluences of 10<sup>16</sup> particles/cm<sup>2</sup> will be reached in the inner layers of particle detectors after 10 years of operation. The radiation levels in question are orders of magnitude higher than those typically encountered in space applications and require a careful and dedicated investigation of radiation effects in the Complementary Metal-Oxide-Semiconductor (CMOS) technologies used in the Application Specific Integrated Circuits (ASICs) designed for particle detectors. This thesis explores several topics related to the qualification of technologies for use in CERN particle detector electronics.

The results of an unprecedented monitoring effort on dozens of chips in the 130-65 nm CMOS technologies used for ASICs developed for the HL-LHC detectors are discussed. This study revealed extreme fab-to-fab and lot-to-lot variability in the TID response of the technologies used. This investigation demonstrated that TID-induced variability must be taken into account in the design and qualification phases of developments.

Displacement damage effects on two 28 nm CMOS technology processes were investigated through proton and neutron irradiation up to the fluences of interest for high energy physics applications. The study revealed that the observed radiation-induced degradation was caused by the amount of total ionizing dose deposited during neutron and proton exposure, rather than by displacement damage. These results support that 28 nm CMOS technology is suitable for applications in CERN particle detectors.

The potential susceptibility of this technology to dose-rate effects is another aspect to be evaluated. Evidence of Enhanced Low Dose-Rate Sensitivity (ELDRS) in TID-induced leakage current increase was observed in ring-oscillators and SRAMs in 28 nm CMOS technology exposed to ultra-high doses. Elevated Temperature Irradiation (ETI) on isolated devices is used to evaluate the dependence of ELDRS on bias conditions and devices size and threshold voltage. The results obtained show that irradiation at high temperature can represent reasonably well the enhanced degradation induced by low-dose-rate, providing a viable solution for accelerated radiation tests.

The radiation response of MOS transistors in a 22 nm Fully Depleted Silicon-



on-Insulator (FDSOI) technology exposed to ultra-high TID was investigated. The investigation revealed that the performance is significantly affected by TID, with the radiation response being dominated by the charge trapped in the buried oxide. Despite the techniques used to mitigate TID effects, the 22 nm FDSOI did not prove suitable for application in the inner parts of detectors. However, it could be suitable for applications with lower TID levels.

**KEYWORDS:** CERN, HL-LHC, ASIC, CMOS technology, Radiation Effects, Radiation Variability, Enhanced Low Dose Rate Sensitivity (ELDRS), Total Ionizing Dose (TID), High Energy Physics Applications, Fully Depleted Silicon On Insulator (FDSOI)

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# List of Acronyms

**ASICs** Application Specific Integrated Circuits

**BG** Back Gate

**BIST** Built-in Self-Test

**BJT** Bipolar Junction Transistor

**BOX** Buried OXide

**BSIM** Berkeley Short-channel IGFET Model

**CCD** Charged-Coupled Device

**CERN** European Organization for Nuclear Research

**CMOS** Complementary Metal-Oxide-Semiconductor

**CMS** Compact Muon Solenoid

**COTS** Commercial-Off-The-Shelf

**CTRW** Continuous Time Random Walk

**CVD** Chemical Vapor Deposition

**DAC** Digital to Analog Converter

**DD** Displacement Damage

**DP** Dual Port

**DPUHD** Dual Port Ultra-High Density

**DR** Dose-Rate

**DUT** Device Under Test

**e-h** electron-hole

**EKV** Enz-Krummenaker-Vittoz

**ELDRS** Enhanced Low Dose-Rate Sensitivity

|                |                                                            |
|----------------|------------------------------------------------------------|
| <b>ELT</b>     | Enclosed Layout Transistor                                 |
| <b>EP-ESE</b>  | Experimental Physics - Electronics Systems for Experiments |
| <b>ESD</b>     | Electrostatic Discharge                                    |
| <b>ESE</b>     | Electronics Systems for Experiments                        |
| <b>ETI</b>     | Elevated Temperature Irradiation                           |
| <b>FBB</b>     | Forward Body Biasing                                       |
| <b>FDSOI</b>   | Fully Depleted Silicon-on-Insulator                        |
| <b>FG</b>      | Front Gate                                                 |
| <b>FinFETs</b> | Fin Field-Effect-Transistors                               |
| <b>HDR</b>     | High Dose-Rate                                             |
| <b>HEP</b>     | High Energy Physics                                        |
| <b>HL-LHC</b>  | High-Luminosity Large Hadron Collider                      |
| <b>KIT</b>     | Karlsruhe Institute of Technology                          |
| <b>L</b>       | length                                                     |
| <b>LDD</b>     | Lightly Doped Drain                                        |
| <b>LDR</b>     | Low Dose-Rate                                              |
| <b>LET</b>     | Linear Energy Transfer                                     |
| <b>LHC</b>     | Large Hadron Collider                                      |
| <b>LS4</b>     | Long Shutdown 4                                            |
| <b>MBU</b>     | Multi Bit Upset                                            |
| <b>ME</b>      | Microelectronics                                           |
| <b>MOS</b>     | Metal-Oxide-Semiconductor                                  |
| <b>MOSFETs</b> | Metal-Oxide-Semiconductor Field-Effect-Transistors         |
| <b>NAL</b>     | narrow and long                                            |
| <b>NOM</b>     | nominal                                                    |
| <b>nPG</b>     | pass-gate nMOS                                             |
| <b>nPU</b>     | pull-up nMOS                                               |
| <b>OA</b>      | Operational Area                                           |

|              |                                         |
|--------------|-----------------------------------------|
| <b>PIN</b>   | Positive Intrinsic Negative             |
| <b>pPD</b>   | pull-down pMOS                          |
| <b>PS</b>    | Pixel Strip                             |
| <b>RBB</b>   | Reverse Body Biasing                    |
| <b>REV</b>   | reverse                                 |
| <b>RINCE</b> | Radiation Induced Narrow Channel Effect |
| <b>RISCE</b> | Radiation-Induced Short Channel Effects |
| <b>ROs</b>   | Ring Oscillators                        |
| <b>RSCE</b>  | Reverse Short Channel Effect            |
| <b>SBU</b>   | Single Bit Upset                        |
| <b>SEB</b>   | Single Event Burnout                    |
| <b>SEEs</b>  | Single Event Effects                    |
| <b>SEL</b>   | Single Event Latch-up                   |
| <b>SET</b>   | Single Event Transient                  |
| <b>SMUs</b>  | Source Metering Units                   |
| <b>SP</b>    | Single Port                             |
| <b>SPUHD</b> | Single Port Ultra-High Density          |
| <b>SRAMs</b> | Static Random-Access Memories           |
| <b>SSA</b>   | Silicon Strip ASIC                      |
| <b>STI</b>   | Shallow-Trench-Insulator                |
| <b>TDEs</b>  | Time-Dependent Effects                  |
| <b>TID</b>   | Total Ionizing Dose                     |
| <b>UDCI</b>  | Ultra-high dose Drain Current Increase  |
| <b>W</b>     | width                                   |

# Chapter 1

## Introduction

Particle detectors are at the heart of high-energy physics experiments at the European Organization for Nuclear Research (CERN), allowing scientists to probe the fundamental particles and forces that govern our universe. The detectors, employed at Large Hadron Collider (LHC), operate in some of the most extreme conditions found in any scientific environment. Furthermore, the upcoming HL-LHC will push the boundaries of particle detection, significantly increasing the luminosity [16]. This increase in collision events comes with a proportional rise in the radiation environment within the detectors as indicated in Fig.1.1.

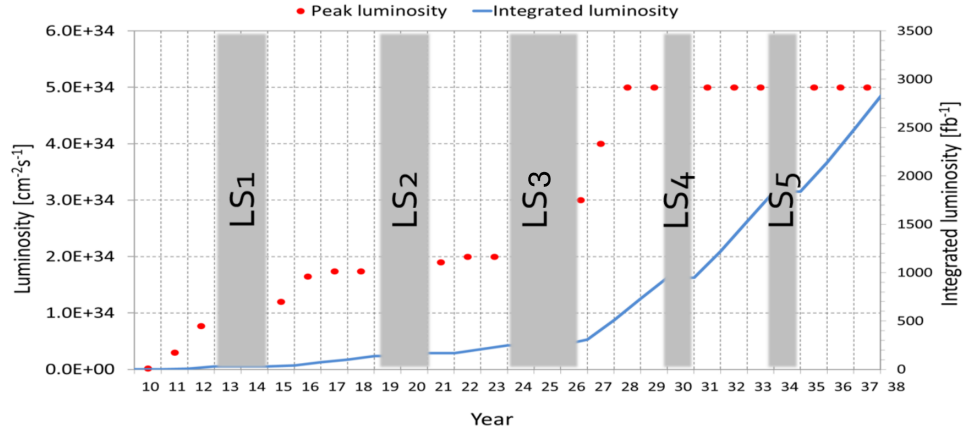


Figure 1.1: Projected LHC performance from 2010 to 2038. Highlighted also the Long Shutdowns [1].

The innermost layers of these detectors, closest to the particles collision point, are subjected to extremely high levels of radiation. The radiation environment in the LHC detectors is complex, dominated by neutrons, charged hadrons (mainly pions, protons, and kaons), and photons, with lesser contributions from electrons, positrons, and muons. Neutrons are the most abundant, with fluences reaching up to  $10^{15}$  particles/ $\text{cm}^2$  and energies from thermal levels ( $\sim 0.025$  eV) to hundreds of MeV. Charged hadrons follow, with fluences of up to  $10^{14}$  particles/ $\text{cm}^2$  and energy ranges typically from hundreds of MeV to a few GeV. Photons, spanning from keV to several GeV, reach similar fluences and contribute significantly to the

total ionizing dose. Electrons and positrons (keV to hundreds of MeV) and muons (hundreds of MeV to several GeV) are also present, though in lower fluences, with muons notable in outer detectors due to their long-range penetration [17, 18]. Over 10 years of operations of the HL-LHC, an increase of one order of magnitude for the particle fluences and TID of up to 1 Grad( $\text{SiO}_2$ ) are expected [19]. Such extreme condition will be exacerbated with the upgrades beyond HL-LHC after the Long Shutdown 4 (LS4) [20].

These levels of radiation are orders of magnitude higher than those typically found in space or medical applications, rendering the use of Commercial-Off-The-Shelf (COTS) components impractical. Therefore, ASICs represent the only viable solution in order to use complex electronics in particle detectors. ASICs are critical to the operation of particle detectors, performing vital tasks such as data acquisition, signal processing and communication. The ASICs for the detectors of the LHC are designed using a commercial 250 nm CMOS process. However, for the HL-LHC, they are expected to transition to a 130-65 nm process. In anticipation of the forthcoming upgrades, the new ASICs will utilize a 28 nm technology [21].

The harsh radiation present in the detector environment poses a serious threat to the reliable operation of these electronics. Radiation can induce various effects that degrade the performance of Metal-Oxide-Semiconductor (MOS) transistors eventually leading to failures. Therefore, the qualification of radiation-hardened ASICs is essential to ensure long-term performance and reliability of detector systems. As a result, it is essential to know the radiation response of CMOS technologies in order to be able to design electronic components capable of withstanding such extreme radiation environments.

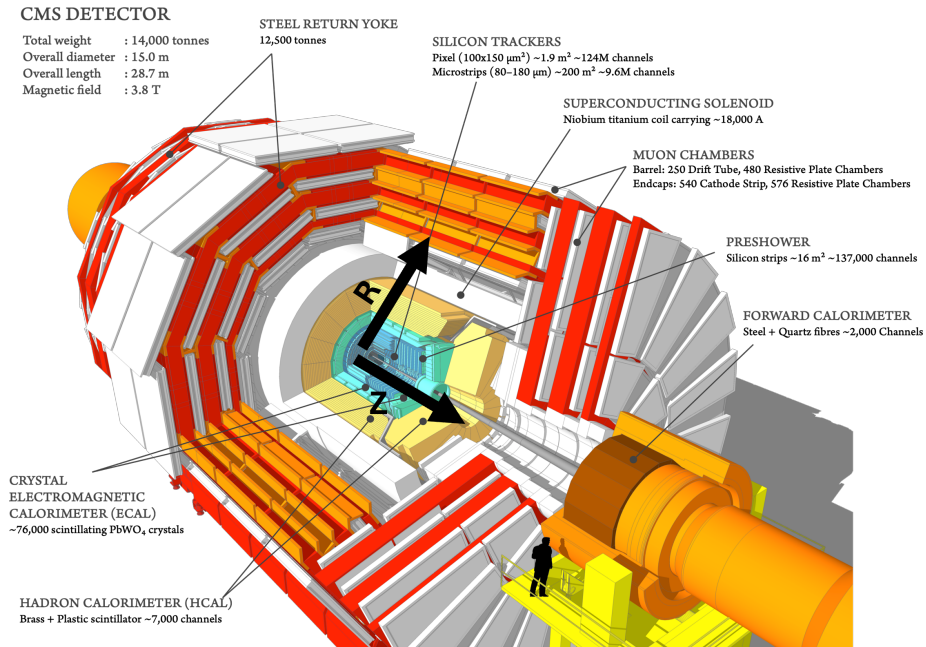
Radiation can be broadly classified into three categories: cumulative ionizing radiation (i.e., TID), cumulative non-ionizing radiation (i.e., Displacement Damage (DD)), and stochastic ionizing radiation (i.e., Single Event Effects (SEEs)). Each type of radiation introduces unique challenges to the performance of electronic components. *Total ionizing dose*, primarily impacts the dielectric layers in CMOS transistors. Charge generated by ionizing particles can accumulate in the oxide of the device, resulting in performance degradation such as threshold voltage shifts. *Non-ionizing* radiation particles, such as neutrons, displace atoms in the semiconductor lattice, leading to displacement damage causing changes in the physical properties of materials and affect performance of transistors. *Single Event Effects* SEEs occur when highly-ionizing individual particles, as heavy ions, strike sensitive regions of a device, causing transient or permanent errors.

While non-ionizing and SEEs are important to the overall performance of electronics, this thesis will primarily focus on the effects of ionizing radiation therefore TID. However, the other effects will be briefly discussed and more details will be added when needed.

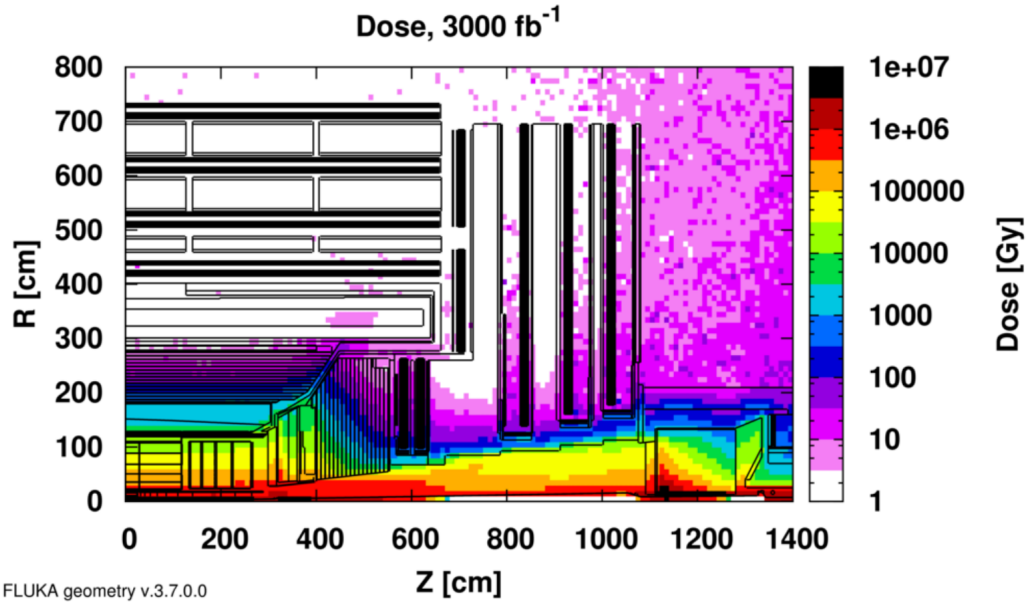
According to the International System of Units the TID is measured in *gray* (Gy) where  $1 \text{ Gy} = 1 \text{ J kg}^{-1}$ , however the *rad* is still widely used and  $1 \text{ rad} = 100 \text{ ergs/g} = 0.01 \text{ Gy}$ .

This thesis explores the radiation hardness of advanced CMOS technologies used in ASICs for CERN's particle detectors, focusing on the TID effects. The goal





(a)



(b)

Figure 1.2: a) Schematic of the Compact Muon Solenoid (CMS) experiment [2].  
b) Simulated ionizing dose levels in CMS [1].

is to evaluate the performance and reliability of various CMOS technology nodes under extreme ionizing radiation and provide insights for future improvements in radiation-hardened design.

In Chapter 2, the basic mechanisms of radiation defects formation in Metal-Oxide-Semiconductor Field-Effect-Transistors (MOSFETs) will be discussed focusing aiming to summarize the main mechanisms of generation and transport of charge in silicon dioxide.

Chapter 3 gives an overview of the experimental setup used in almost all of the experiments reported in this thesis and reports the definition of the several parameters that will be used to quantify the performance of transistors exposed to radiation.

Chapter 4 summarizes the current understanding of the main phenomena associated with TID exposure in MOS transistors. Attention will be given to the phenomena related to charge trapping in Shallow-Trench-Insulator (STI) and spacer oxides in advanced CMOS technology nodes.

In Chapter 5, the extreme TID-induced fab-to-fab variability observed in the 130-65 nm CMOS technologies for the ASICs of the HL-LHC upgrade is presented. Its impact on circuit level examples and qualification procedure is discussed.

In Chapter 6, the presence of displacement damage effects in the 28 nm CMOS technology is investigated through neutron and proton irradiation at extremely high fluences. Aiming to distinguish between DD and TID effects, X-ray irradiation were also employed.

In Chapter 7, the true dose-rate dependence observed in the TID response of isolated transistors, Static Random-Access Memories (SRAMs) and Ring Oscillators (ROs) in 28 nm is discussed. The possibility of using irradiation at high temperature to avoid time-consuming low Dose-Rate (DR) testing is also investigated.

In Chapter 8, the TID response of a commercial 22 nm FDSOI CMOS technology is evaluated for the first time at ultra-high dose.

Eventually, Chapter 9 summarized the key findings of this thesis.

## Chapter 2

# Basic Mechanisms of Radiation Defects Formation in MOSFETs

Exposure to ionizing radiation significantly impacts the behavior of MOS transistors, leading to performance degradation. The primary concern lies in the radiation-induced charges that become trapped within the oxides forming the MOSFETs structure and at their interfaces with silicon.

In this chapter, we delve into a thorough examination of the current knowledge surrounding the creation and development of radiation-induced defects and trapped charges in MOS transistors. While much of the existing literature focuses on studying radiation effects specifically in the gate oxide, it is essential to recognize that the significance of this oxide's radiation response has diminished in contemporary technologies. Nevertheless, the underlying physical mechanisms governing charge generation and transport remain consistent across other oxides within the MOS structure. Such effects have been thoroughly investigated in the literature, both in books ([22, 23]) and articles (such as [4, 5, 24, 25]). This chapter summarizes the key phenomena associated with radiation-induced alterations in MOS devices.

### 2.1 Photon-Matter interaction

The interaction between photons and matter is based on three fundamental mechanisms: photoelectric effect, Compton scattering, and pair production [26, 3, 27]. As summarized in Fig. 2.1, the occurrence of one or more of these mechanisms is dependent on both the energy of the incident photons and the atomic number of the target material. In almost all the experiments conducted in this thesis, the target material is silicon ( $Z_{Si} = 14$ ) and silicon dioxide ( $Z_O = 8$ ), with the radiation source being X-rays peaking at 10 keV. Therefore, the photoelectric effect is the primary interaction mechanism.

Such effect, consists in the complete absorption of an incident photon, resulting in the emission of an electron. If the energy of the incident photon is sufficient to excite an electron from the innermost shell (K-shell) then approximately 80% of interactions will involve electrons from the K-shell [26, 27, 28]. For silicon, the

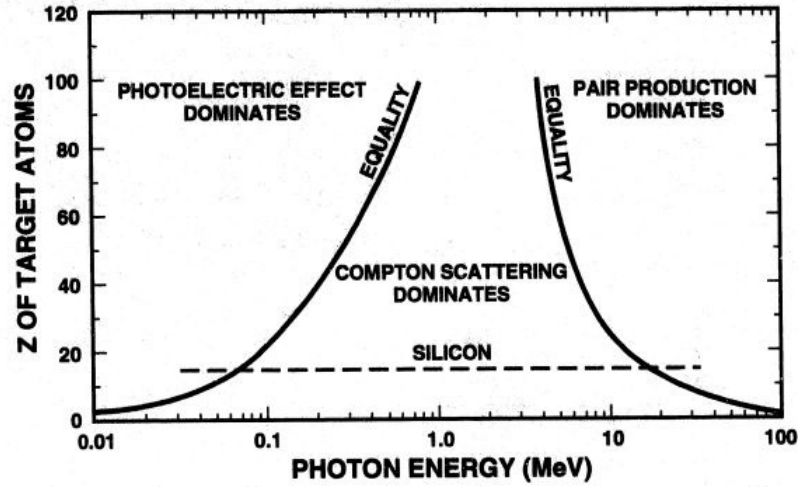


Figure 2.1: Summary of photon-matter interaction for different photon energies and target atomic number. At 10 keV X-rays, the dominant effect in silicon ( $Z_{\text{Si}} = 14$ ) is photoelectric. After ([3]).

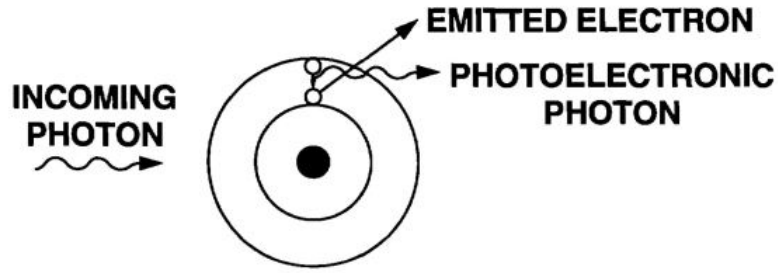


Figure 2.2: Illustration of the photoelectric effect.

energy of the K-shell is measured to be 1.8389 keV [29]. Following the release of the electron, another electron from an outer orbit (such as the L orbit if the electron comes from the K-shell) will pass to occupy the vacated state, causing the emission of a low-energy photon as schematically represented in Fig. 2.2. In turn, the generated electron can ionize other atoms in its path.

## 2.2 e-h Generation, Transport and Trapping in SiO<sub>2</sub>

This section provides an overview of the current understanding of the mechanisms that cause charge trapping in MOS oxides after exposure to an ionizing source. These mechanisms can be summarized as follows:

1. production of electron-hole (e-h) pairs;
2. initial recombination of e-h pairs;
3. h transport in the oxide;

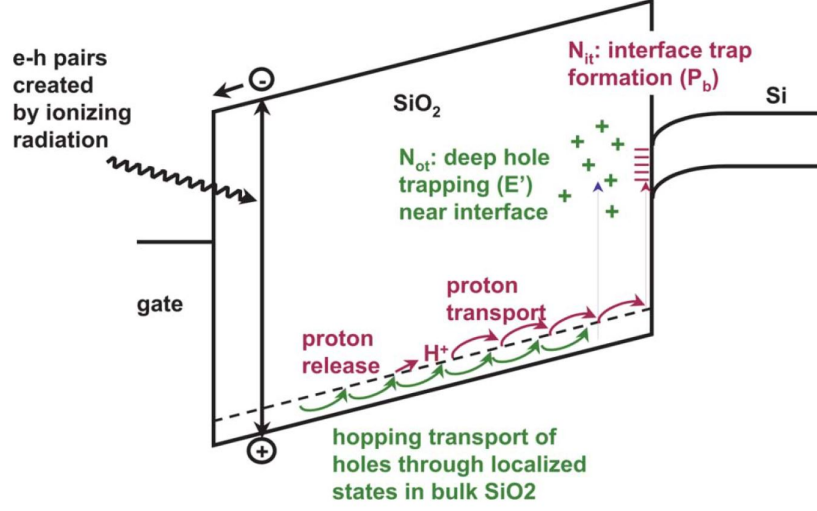


Figure 2.3: Graphic representation of TID-induced oxide traps (green) and interface traps (red) formation in the gate oxide of an nMOS with  $V_G > 0$  V bias ([4]).

4. formation of hydrogen ions ( $H^+$ );
5. holes trapping near Si/SiO<sub>2</sub> interface;
6. hydrogen ions drift and formation of interface traps;

The discussion will be conducted with reference to an nMOS device with a positive bias applied to the gate, as described in Fig. 2.3.

### 2.2.1 Electron-Holes Pairs Production

Secondary electrons (or more generally electrons in the environment) produced by the interaction of photons with silicon dioxide can ionize atoms, creating an e-h pair. This process can continue for as long as the energies of the secondary electrons exceed the threshold energy for the creation of e-h pairs. Therefore, a single high-energy photon can effectively create many e-h pairs. In SiO<sub>2</sub>, the energy required to create an e-h pair is 17 eV [30] and the pair density generated per rad is  $8.1 \times 10^{12}$  pairs/cm<sup>3</sup> [26].

### 2.2.2 e-h Pairs Recombination

Following their creation, electrons and holes begin to move in opposite directions in the oxide if an electric field is applied, as is usually the case in MOS. Electrons have a relatively high mobility in SiO<sub>2</sub>, about  $20 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$  at room temperature and increases to  $40 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$  at temperatures below  $-100^\circ \text{C}$ , reaching a saturation velocity of about  $1 \times 10^7 \text{ cm s}^{-1}$  for electric fields exceeding  $5 \times 10^5 \text{ V cm}^{-1}$  [31, 32, 33]. In contrast, the mobility of holes can vary considerably with temperature and electric field, yet remains several orders of magnitude lower than that of electrons

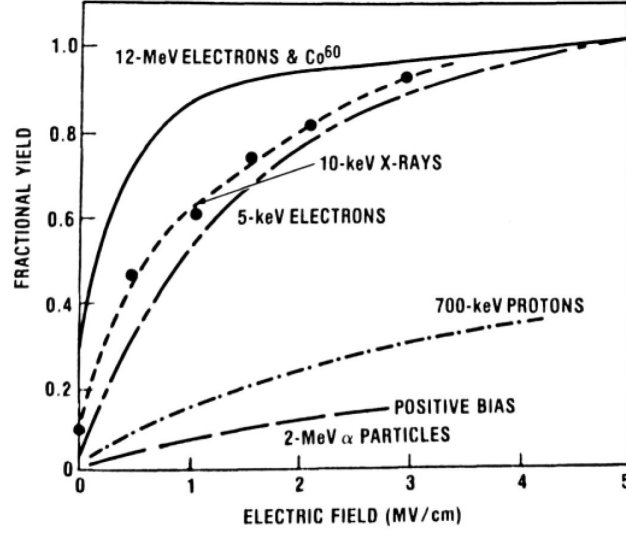


Figure 2.4: Fraction of charge yield in the oxide, after ([5]). The yield is strongly dependent on the type of incident particle as well as the electric field in the oxide.

[34, 35, 36]. This difference in mobility implies that while electrons can rapidly escape from the oxide, holes can be considered immobile.

Despite the very high mobility, a fraction of electrons can still recombine with holes in the very first moments after e-h pairs generation. This process is usually referred to as *initial recombination*. The amount of holes that escape this initial recombination represent the *charge yield*.

Both initial recombination and charge yield depend on the source type and energy of the incident particle as well as the electric field in the oxide [22]. An empirical conclusion is that strongly ionizing particles form dense columns of pairs whereas weakly ionizing sources create isolated pairs [22]. The closer together are the e-h pairs the higher is the probability they will recombine [5]

Depending on the proximity of different e-h pairs, two recombination models are adopted in literature: the *columnar model* for the case where e-h pairs are very close together [37]; the *geminate model* for the case where pairs are far from each other [5]. In the columnar model, e-h pairs are positioned closer to each other compared to the geminate model, resulting in a higher recombination rate. Note, however, that in most applications the actual recombination model is a combination of the two [5]. Fig. 2.4, illustrates the charge yield for different radiation sources in SiO<sub>2</sub>; the charge yield is inversely proportional to the ionizing power of the radiation source. Notably, <sup>60</sup>Co and 10 keV X-ray produce the same charge yield for electric fields greater than 3 MVcm<sup>-1</sup>.

At this point the total number of holes generated that escaped the initial recombination ( $N_h$ ) can be calculated as [27, 26]:

$$N_h = f(E_{ox})g_0Dt_{ox} \quad (2.1)$$

where  $f(E_{ox})$  is the holes yield as a function of the field in the oxide,  $D$  is the dose,  $t_{ox}$  is the oxide thickness and  $g_0$  is a parameter specific of the material. In

SiO<sub>2</sub>, Eq. 2.1 becomes [26]:

$$N_h = 8.1 \times 10^{12} f(E_{ox}) D t_{ox} \quad (2.2)$$

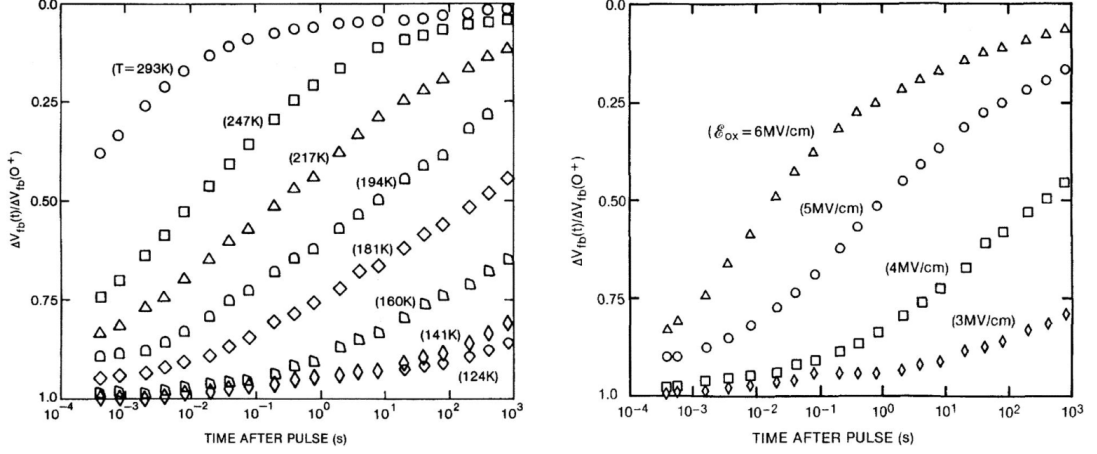
### 2.2.3 Transport of Holes in the Oxide

When an electric field is applied, the holes escaped from the initial recombination can move in the oxide depending on the direction of the electric field; in the case considered (positive gate bias), the holes move toward the Si/SiO<sub>2</sub> interface. Several studies have been conducted over the years, such as [35, 38, 39, 23], and the description that best fits the experimental data is "polaron hopping", a complex and highly time-dispersive mechanism [40, 41]. As a h traverses the oxide, it alters the spatial arrangement of neighboring atoms through electrostatic interactions, resulting in a localized distortion of the material structure. The system hole + distortion is a Polaron, a quasi-particle with mass larger than the hole and smaller mobility. Within the oxide, polarons traverse by "hopping" through shallow, dispersed states, although with an approximate separation of 1 nm [5]. Temperature, electric field and oxide thickness influence holes transport in the oxide as illustrated in Fig. 2.5. The data were obtained after pulsed 12 MeV electron irradiation of MOS capacitors and normalized to the flatband voltage shift immediately after the pulse, i.e. before any transport occurs [22].

Notice how, in Fig. 2.5a and Fig. 2.5b, the flat band voltage nearly returns entirely to its pre-irradiation level under conditions of elevated temperature and/or strong electric fields. This suggests that only a minimal quantity of holes becomes confined in trapping sites within these oxides. Furthermore, research has indicated that the transit time of holes varies proportionally to  $t_{OX}^4$ . This can be seen in Fig. 2.5c where a reduction of the oxide thickness of a factor 2.4 (from 98.7 nm to 41.3 nm) results in a reduction in the transit time by a factor of  $\sim 33$ . This implies that in contemporary technologies, characterized by gate oxide thicknesses of a few nanometers ( $t_{OX} < 10$  nm) and electric fields  $E_{OX} \geq 2$  MeV, any unhindered holes can be expelled from the gate oxide within moments after the generation of electron-hole pairs even at room temperature. Another piece of information that can be deduced from Fig. 2.5 is that changes in external parameters do not appear to have a great effect on the shape of the recovery curves when plotted against logarithmic time. In fact, changing any of these parameters only results in a rigid translation of the curves along the time axes, i.e. only the time scale of the transport is affected [5, 6].

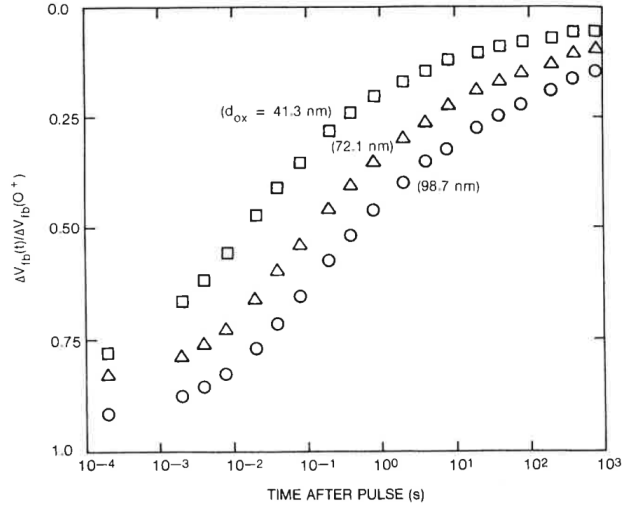
Several studies (see [22] and the references cited in Section III.C) have shown that hole transport can be effectively characterized using the Continuous Time Random Walk (CTRW) framework. This approach proves valuable for modeling hopping transport phenomena, as illustrated by the solid line in Fig. 2.6.

This model led to a description of hole transport represented by the functional form  $F(\alpha; t/t_s)$  [36], where only the time scale factor  $t_s$  varies with temperature, electric field and gate oxide properties, while  $\alpha$  remains unaffected by these parameters, consistent with the expected universality of behaviour.



(a) Recovery time at different temperatures of the flatband voltage shift. The shift was normalized to its value after the irradiation pulse ( $t_{OX} = 96.5$  nm,  $E = 1$  MVcm<sup>-1</sup>). From [42].

(b) Recovery time at different electric fields of the flatband voltage shift. The shift was normalized to its value after the irradiation pulse ( $t_{OX} = 86.5$  nm,  $T = 79$  K). From [43].



(c) Recovery time of the flatband voltage shift for different oxide thicknesses. The shift was normalized to its value after the irradiation pulse ( $T = 80$  K,  $E = 5$  MVcm<sup>-1</sup>). After [44].

Figure 2.5: Recovery time of the flatband voltage shift after the irradiation pulse for different temperatures, electric field and oxide thickness.



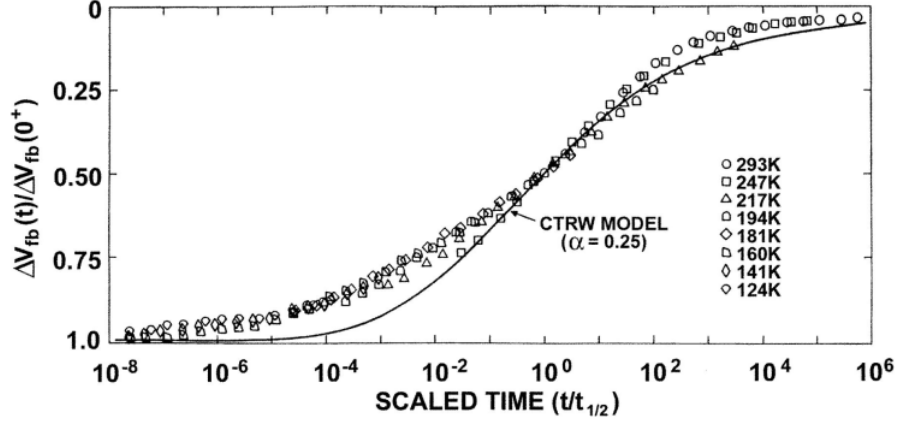


Figure 2.6: Normalized flatband voltage shift of 2.5a rescaled to time the at which half recovery occurs. The solid lines illustrated the calculation of the CTRW model recovery for  $\alpha = 0.25$  [6].

### 2.2.4 Formation of Hydrogen Ions

Hydrogen is widely employed in CMOS technology for passivating dangling bonds at the silicon/gate oxide interface [45, 46]. Holes (h) passing through the SiO<sub>2</sub> can react with hydrogen, releasing hydrogen ions (H<sup>+</sup>) in the reaction:



These ions play a crucial role in the formation of interface traps, which will be discussed later in this chapter.

### 2.2.5 Oxide Trapping

As holes travel through the oxide, they may become trapped in oxide traps, which are mainly associated with vacancies within the oxygen structure of SiO<sub>2</sub>. Amorphous silicon dioxide has a structure in which each silicon atom is bonded to four oxygen atoms, and each of these oxygen atoms is shared between two silicon atoms. The absence of an oxygen atom weakens the bond between the two Si atoms facilitating the rupture of the bond by a hole. This hole can then readily combine with one of the two electrons within the Si – Si bond, forming a structure commonly referred to as an E' center. At this point there are two different possible types of defects: E'<sub>δ</sub> center and E'<sub>γ</sub> center. In an E'<sub>δ</sub> center the remaining electron in the Si-Si bond is equally shared between the two silicon atoms [47]. In an E'<sub>γ</sub> center, instead, the remaining electron is primarily bound with one of the two silicon forming an asymmetrical structure with positive charge [48].

The E'<sub>γ</sub> center is illustrated in the top part of Fig. 2.7, where the strained Si-Si bond (a) and the trapping of a hole (b) are reported [7]. Fig. 2.7 illustrates also the annealing processes that neutralize trapped positive charge, depicted as reversible or permanent. Permanent annealing occurs when an electron tunnels from the substrate and recombine with the positively charged silicon atom (Fig. 2.7(c)→(a)).

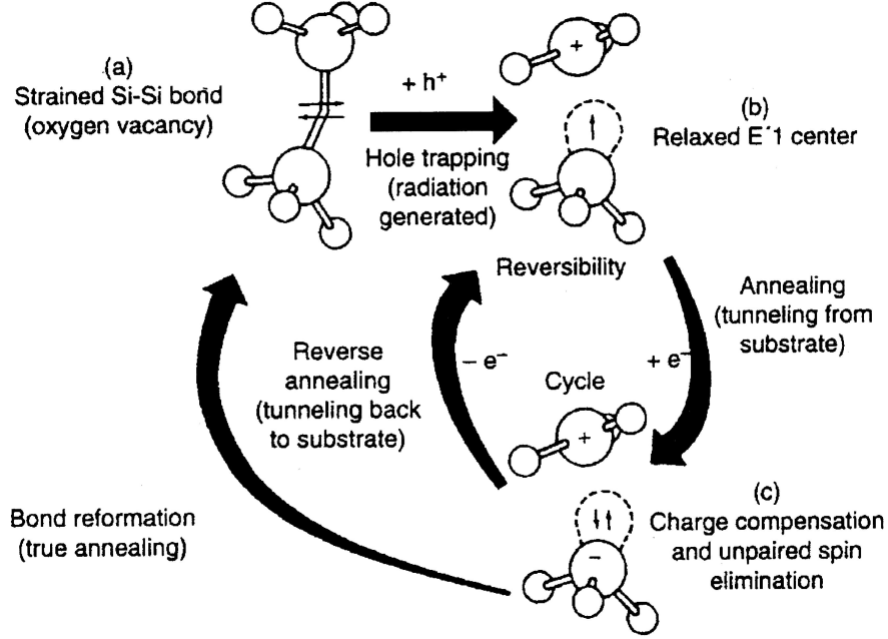


Figure 2.7: Schematic representation of the generation and annealing of oxide trapped charge [7].

Conversely, an electron can tunnel towards the neutral silicon atom, in this case the charge will be compensated but the silicon bond will not reform and the process can be reversed by applying a negative bias to the gate (Fig. 2.7(b)). The farther the charge trapped in the oxide is from the interface, the less likely it is to be neutralized by tunneling electrons. As a consequence, the probability that traps located far from the interface can be reached by electrons from the substrate is low. This results in prolonged annealing times for charges trapped in these defects. The oxide traps instead located near the interface, can easily interact with electrons coming from the silicon substrate. This allows it to quickly respond to changes in polarization and switch from a positive to a neutral configuration. These traps are commonly referred to as "border traps" [49, 50]. As a general guideline, any E' center located within 3 nm from the Si/SiO<sub>2</sub> interface are classified as border traps [51].

The charge build-up process can be described mathematically as:

$$\Delta n_{th}(x, \Delta D) = F_h(x) \sigma_{ht}(E_{ox}(x)) [N_{ht}(x) - n_{ht}(x)] - F_e(x) \sigma_r(E_{ox}(x)) n_{ht}(x) \quad (2.4)$$

Where,  $F_h(x)$  and  $F_e(x)$  are the local fluences per unit of dose for radiation-generated holes and electrons;  $n_{ht}(x)$  is the local density of trapped holes;  $N_{ht}(x)$  is the local density of hole traps;  $\sigma_{ht}$  is the local oxide field-dependent cross-section for recombination of an electron with a trapped hole and  $\sigma_r$  is the local oxide field-dependent cross-section for recombination of an electron with a trapped hole. The first part takes into account that, starting from initial fluences per unit of dose of

generated holes, some of them will be captured, hence the presence of the cross section term. The difference  $[N_{ht}(x) - n_{ht}(x)]$  represents the empty traps state, so the ones that are actually participating in the charge build-up process. The second operand of the equation refers to electrons and since they have a negative impact (due to the recombination process) in charge accumulation, this term must be subtracted from the first. At this point, the areal charge density referred to the SiO<sub>2</sub>/Si interface is given by:

$$\Delta N_{ot} = \frac{1}{t_{ox}} \int_0^{t_{ox}} n_{ht}(x) x \, dx \quad (2.5)$$

The threshold voltage shift that results from the trapped holes ( $\Delta V_{ot}$ ) is [23]:

$$\Delta V_{ot} = -\frac{q}{\epsilon_{ox}} t_{ox} \Delta N_{ot} \quad (2.6)$$

The flatband voltage shift is quadratically dependent on the oxide thickness, since the term  $\Delta N_{ot}$  is proportional to  $t_{ox}$ . The continuous thinning of the gate oxide thickness with technology scaling is therefore enhancing the radiation hardness of gate oxides. While this behavior holds for  $t_{ox} > 20$  nm, below 20 nm the dependence is even more pronounced as it can be observed in Fig. 2.8. In Fig. 2.8, the flatband voltage shift in MOS capacitors has been measured at  $T = 80$  K [52, 53] so that holes cannot promptly move from their generation point therefore preventing the formation of interface traps (as it will be shown in the next section) [54].

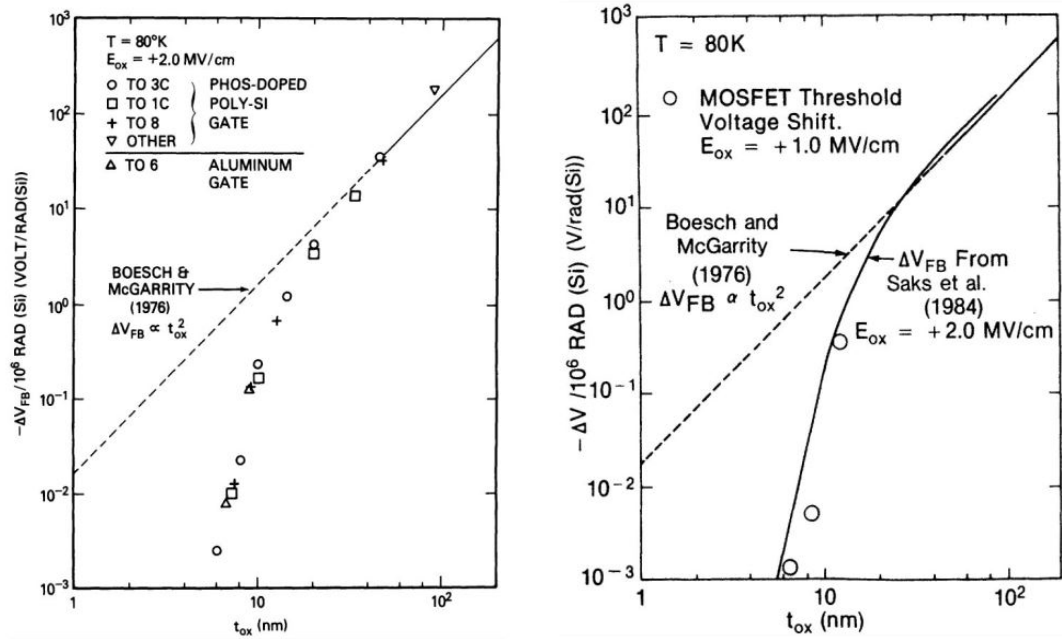
The greater reduction in  $\Delta V_{FB}$  for thinner oxides has been attributed to the enhanced possibility of charge compensation by the electrons tunneling from the silicon substrate [52, 53].

### 2.2.6 Interface Trapping

The production of hydrogen ions  $H^+$  due to the reaction of holes with hydrogen (subsection 2.2.4) in SiO<sub>2</sub> is the primary precursor to interface trap formation. In the presence of a positive bias applied to the gate,  $H^+$  is directed to the SiO<sub>2</sub>/Si interface where it can depassivate a Si – H bond. The depassivation ends with a H<sub>2</sub> and a Si dangling bond, i.e., a Si atom bonded with other three Si atoms and with an unpaired electron, a defect named  $P_b$  center [55, 56, 57]. Temperature and/or electric field can strongly affect the development of interface traps as depicted in Fig. 2.9. The creation of interface traps is a much slower process than the trapping/annealing of oxide traps. In fact, at room temperature, saturation is reached in 1000 s, whereas it is  $\sim 10$  s for oxide traps.

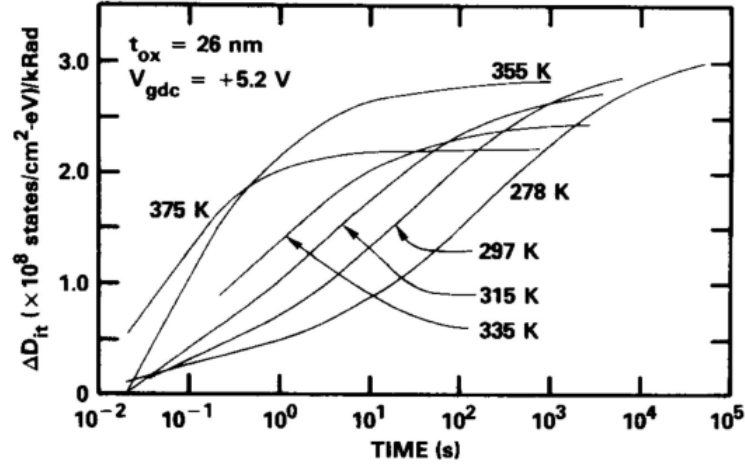
Interface traps annealing is also slower and might be evident only at high temperatures [59, 60].

As with the oxide traps, the density of the interface traps is also lower for thinner oxides, thus confirming that technology scaling improves the radiation response of MOSFETs devices. [61, 62].  $P_b$  centers are amphoteric, i.e., they can

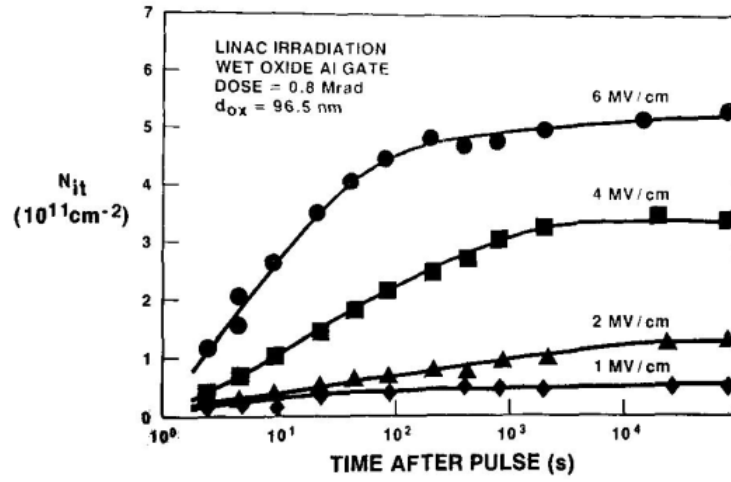


(a)  $\Delta V_{FB}$  for each 1 Mrad(SiO<sub>2</sub>) in MOS capacitors [52].  
 (b)  $\Delta V_{FB}$  for each 1 Mrad(SiO<sub>2</sub>) in MOSFETs [53].

Figure 2.8: Flatband threshold voltage shift for different oxide thicknesses ( $t_{ox}$ ) measured at  $T = 80 \text{ K}$ . For  $t_{ox} > 20 \text{ nm}$ , the shift is  $\propto t_{ox}^2$  as described in 2.6. For  $t_{ox} < 20 \text{ nm}$ , the dependence is even steeper than the expected quadratic dependence.



(a) Interface trap density at different temperature after electron pulse irradiation (six electron pulses at 40 MeV of 0.5  $\mu$ s) on MOS-FETs. The pulses provided 50 krad(SiO<sub>2</sub>) per pulse [58].



(b) Electric field dependence of interface traps in Al-gate MOS capacitors irradiated with electrons at room temperature. The capacitors were irradiated to 800 krad(SiO<sub>2</sub>) with a 4  $\mu$ s 13 MeV pulse [57].

Figure 2.9: Influence of temperature and electric field on interface traps buildup.

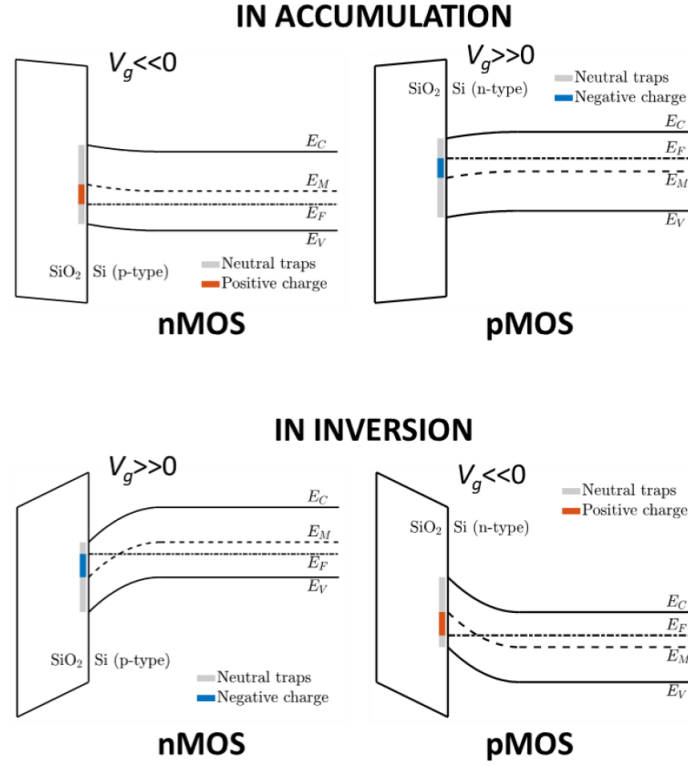


Figure 2.10: Energy band diagram of MOS devices: The net trapped charge at the interface is determined by the position of the Fermi level at the channel surface. (top) Off-state, where the channel is in accumulation, and (bottom) On-state, where the channel is in inversion. Here,  $E_C$  represents the conduction band energy level,  $E_M$  is the midgap,  $E_F$  is the Fermi level, and  $E_V$  denotes the valence band energy level.

be positively charged (donor) or negatively charged (acceptor) depending on their energy level with respect to the midgap ( $E_M$ ) and Fermi level ( $E_F$ ). Generally, traps in the lower portion of the band gap are predominantly donors, i.e., they are likely to "donate" an electron when above  $E_F$  becoming positive and are neutral when below. Contrary, defects in the upper portion of the band gap are for the majority acceptors, meaning that they tend to "accept" an electron from the silicon becoming negatively charged when below  $E_F$  and neutral above [63, 57]. Consequently, while the oxide charge is always positive, the charge of an interface trap can be readily altered by applying an external bias. In an n-type device, where a positive gate bias is typically employed, the interface traps will predominantly be negatively charged, whereas in p-type devices they are positively charged. Consequently, since the oxide charge is positive for n/p MOSFETs, the oxide charge and interface charge tend to compensate for nMOS and add up for pMOS, resulting in a significant difference in the radiation response of these two devices. Fig. 2.10 schematically summarizes the process of interface charge trapping in MOS capacitor.

# Chapter 3

## General Elements

This chapter presents an overview of the experimental setup used in all X-ray irradiation tests discussed in this thesis, along with a discussion of key parameters that will be employed to evaluate the behavior of MOS transistors.

### 3.1 Experimental Setup

#### 3.1.1 X-ray Machine Details

$^{60}\text{Co}$  is the reference radiation source for TID tests specified in many standards, such as ESA ECSS. However,  $^{60}\text{Co}$  sources are generally characterized by a relatively low DR. As the electronics of the HL-LHC upgrade will have to withstand extremely high radiation levels,  $^{60}\text{Co}$  tests would not be feasible due to the time required for each test. In recent years, X-ray machines have become a popular alternative for TID testing because they are easy to manipulate (less restrictive safety protocol), provide results comparable to  $^{60}\text{Co}$ , and offer a very high dose-rate. For this reason, the Microelectronics (ME) section of the Electronics Systems for Experiments (ESE) at CERN operates two Seifert RP149 X-ray machines with a 10 keV irradiation source. The irradiation setup is similar to the one developed by in 1982 by Palkuti and LePage [64]. These machines can deliver a very high DR with a maximum of about  $10 \text{ Mrad}(\text{SiO}_2)/\text{h}$ , which means that it takes about 5 days to perform an irradiation to  $1 \text{ Grad}(\text{SiO}_2)$ .

In the Seifert RP149, X-rays are generated from electrons at 40 keV hitting a Tungsten target. The tube is sealed using a Beryllium window of  $250 \mu\text{m}$  and an Aluminium filter of  $150 \mu\text{m}$  is used to filter low-energy photons, eventually generating an X-ray spectrum with a peak around 10 keV [64]. The X-ray spectrum is reported in Fig. 3.1. The three peaks around 8, 10, 11 keV correspond to specific L-lines of tungsten, i.e., transition that involve electron from the L-shell respectively  $L_{\alpha_1}, L_{\beta_1}, L_{\gamma_1}$ . The part of the spectrum with energies above 11 keV is instead due to Bremsstrahlung interaction with the tungsten where the electrons are slowed down by nuclear interaction with tungsten resulting in photon emission [65]. To prevent the X-rays from reaching the external environment, the machine is enclosed within a protective cabinet.

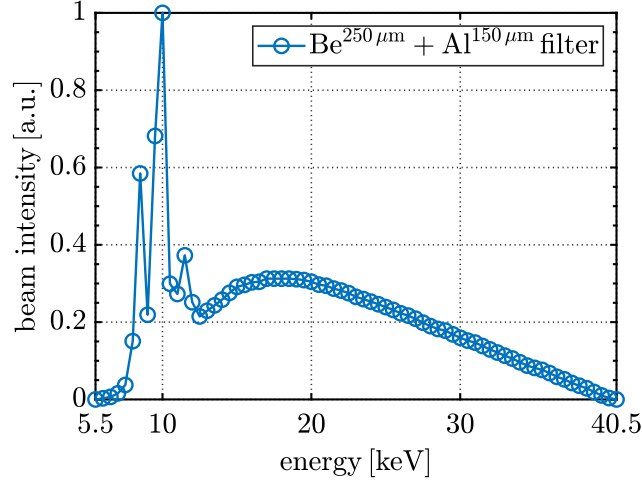


Figure 3.1: X-ray spectrum generated by the irradiation system. The beam intensity is normalized to that at 10 keV.

The dose-rate mapping of the beam of the Experimental Physics - Electronics Systems for Experiments (EP-ESE) irradiation setup is done using a pre-calibrated Positive Intrinsic Negative (PIN) diode [64, 66]. In a reverse-biased PIN diode, the depletion region invests the entire intrinsic region, and the current is proportional to the electron-hole pairs produced by the incident photons. Consequently, it is possible to measure the DR by subtracting the current before exposure ( $I_{\text{dark}}$ ) from the measured current ( $I_{\text{exposure}}$ ) in order to obtain the photo-current, and then multiplying the result by a given coefficient as:

$$DR = \beta \cdot (I_{\text{exposure}} - I_{\text{dark}}) = \beta \cdot I_{\text{photo-current}} \quad (3.1)$$

In order to obtain the spatial distribution of the dose-rate, the diode is moved to different positions relative to the tube. An example of the calibration map is reported in Fig. 3.2 for a distance between the tube and the diode of 2 cm and with input voltage 40 keV and current 50 mA.

### 3.1.2 DUT and Measurement Setup

In all the experiments reported in this thesis, the Device Under Test (DUT) is a silicon die fabricated as an ASIC containing MOS transistors divided into several arrays, each array being designed specifically to study a particular aspect of radiation response. Two pad columns constitute an array, as shown in Fig. 3.3. To maximize the number of transistors on a single ASIC, in most cases the devices in an array share gate, source and bulk terminals. The transistors are protected with customized Electrostatic Discharge (ESD) protection circuits.

A custom-designed probe card with needles of a few  $\mu\text{m}$  is then used to measure these ASICs. The probe card's needles are manually connected to the DUT assisted by a Charged-Coupled Device (CCD) camera. The mechanical friction caused by the needles removes the thin oxide layer covering the pads, exposing



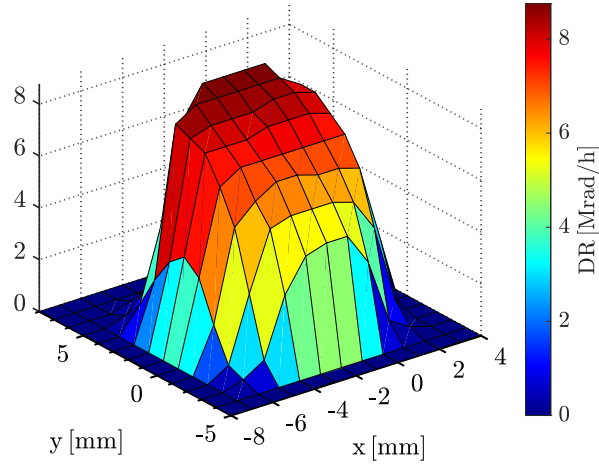


Figure 3.2: Dose-rate map measured at 2 cm from the diode with X-ray tube set at  $V = 40$  kV and  $I = 50$  mA.

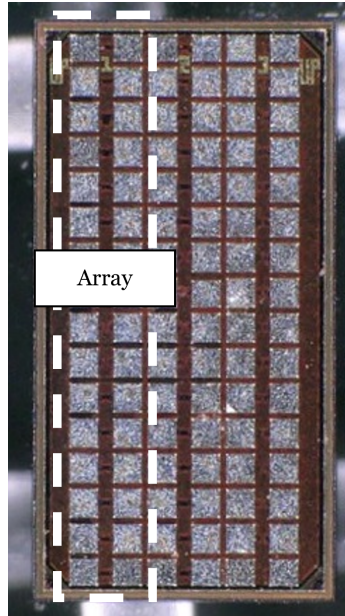


Figure 3.3: Custom designed ASIC for radiation studies.

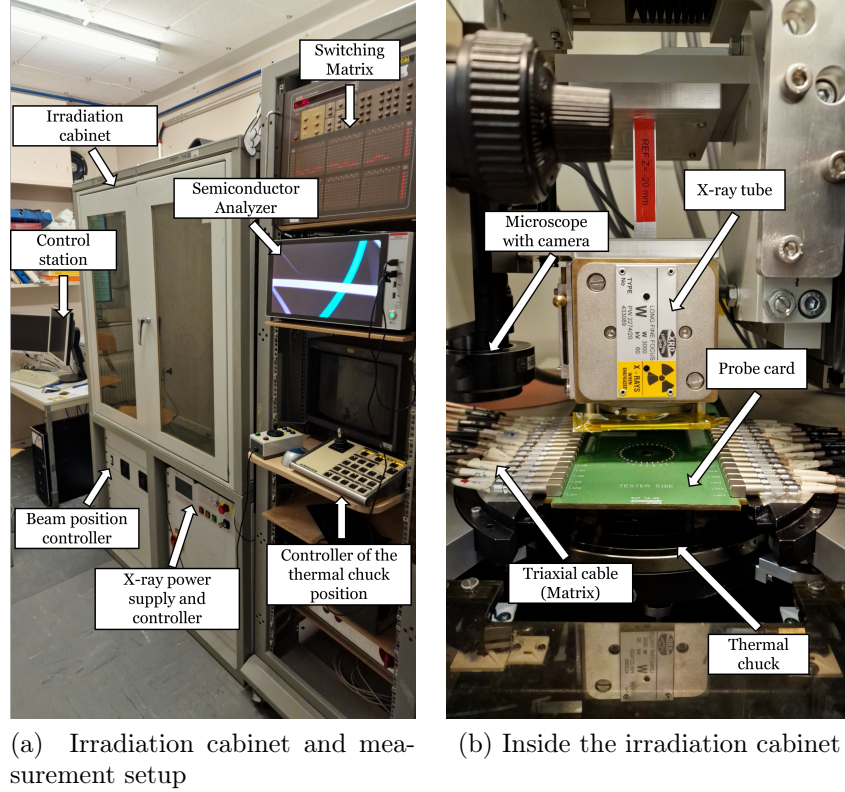


Figure 3.4: EP-ESE-ME setup.

the metal layer and thus creating the electrical connection. Before the DUT is positioned in the machine, it is attached to a copper plate and placed on a thermal chuck whose positioning is controlled by a customized external system. The electrical isolation and a good thermal exchange are ensured by using a thermal pad between the chip and the block and between the block and the thermal chuck.

The transistors can be heated or cooled via the thermal chuck which can provide temperatures in the range  $-50^{\circ}\text{C}$  to  $100^{\circ}\text{C}$ . For irradiation at  $T < 0^{\circ}\text{C}$ , the cabinet is filled with dry air to prevent ice formation. The irradiation/measurement setup is illustrated in Fig. 3.4a, where all the instruments are highlighted.

Fig. 3.4b illustrates the inside of the cabinet of the X-ray irradiation system. Each needle is connected via Lemo triaxial cables to a Keythley 707A switching matrix that houses 3 7072 matrix cards with 12 outputs each and is responsible for routing signals from the devices to a Keythley 4200A-SCS semiconductor analyzer. The Keythley 4200A analyzer is equipped with 6 Source Metering Units (SMUs) that allow simultaneous sourcing and measurement to perform DC characterization.

The switching matrix can also connect two more input signals in addition to the 6 channels connected to the semiconductor analyzer, these two channels are usually connected to a voltage generator to provide a bias to the DUT during irradiation and/or annealing. Typically, an irradiation test consists of several

irradiation steps, each followed by measurements. After a measurement step, the bias is applied again and the DUT is irradiated at a target dose before being measured again. Every aspect of the test, apart from connecting the chip, is automated using customized LabVIEW software. Post-irradiation annealing is usually performed in the same setup, but sometimes the ASIC is removed from the X-ray machine and connected to another setup with the same characteristics of the one described in this chapter apart for the semiconductor analyzer which in this case is an HP-4155B.

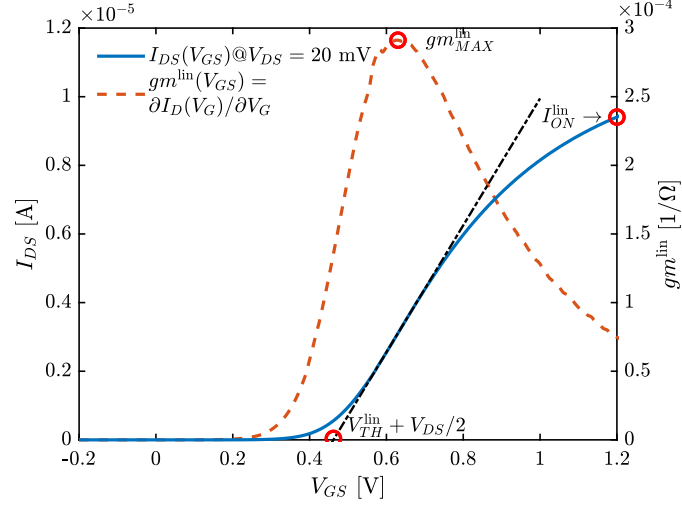
## 3.2 MOS Transistor Parameters

In the course of this thesis, we will repeatedly use different parameters extracted from the  $I_D - V_G$  curves of the measured transistors. Since each of these parameters can be extracted in different ways, it is good to define what these parameters are and how they were extracted. Fig. 3.5a, reports the  $I_D - V_G$  of an n-type transistor in 65 nm CMOS technology measured in linear region,  $V_{DS} = 20$  mV sweeping the gate voltage from  $-0.2$  V to  $1.2$  V while  $V_S = V_B = 0$  V. We define as  $I_{ON}^{\text{lin}}$  the maximum drain current reached at  $V_G = V_{DD}$ . The threshold voltage in linear region,  $V_{TH}^{\text{lin}}$ , which indicates the minimum gate voltage to pass from the OFF state to the ON state of a transistors, is extracted with the linear extrapolation method [67, 68]. This method is based on the definition of the drain current in the ON region as:

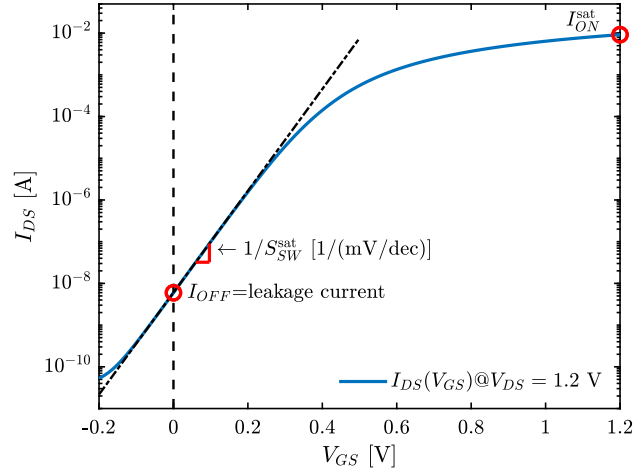
$$I_{DS}^{\text{lin}} = \frac{W}{L} \mu C_{OX} \left[ (V_{GS} - V_{TH}^{\text{lin}}) V_{DS} - \frac{V_{DS}^2}{2} \right] \quad (3.2)$$

where width (W) and length (L) are the channel width and length, respectively,  $\mu$  is the mobility measured in  $\text{m}^2/\text{V}$  and  $C_{OX}$  is the oxide capacitance, measured in  $\text{F}/\text{m}^2$ . The peak of the transconductance  $g_m^{\text{lin}} = \partial I_{DS}^{\text{lin}} / \partial V_{GS}$  (red dashed lines) is used to determine the region where the drain current is best described with 3.2. The  $V_{TH}^{\text{lin}}$  is defined as the intersection between the  $I_{DS} = 0$  A and the linear linear fit of the characteristic (black dotted line) minus  $V_{DS}/2$ . Both the  $g_m^{\text{lin}}$  and the mobility  $\mu$  are on their own two important benchmarks used to investigate the response of MOS transistors to radiation.

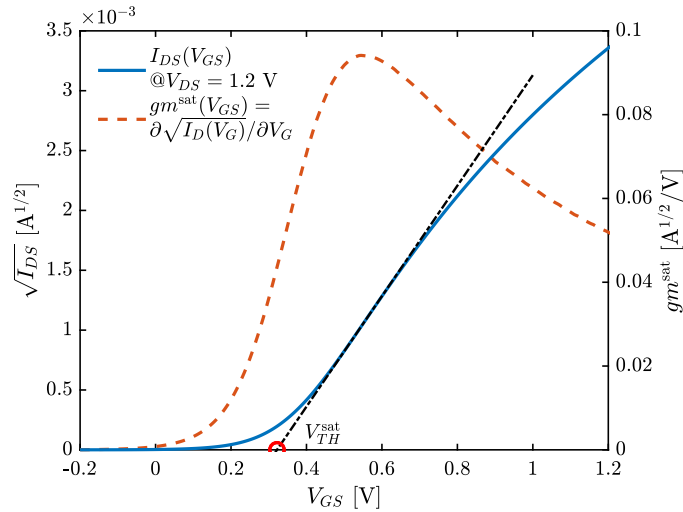
From the  $I_D - V_G$  in saturation region (Fig. 3.5b), are highlighted three other key parameters: on current ( $I_{ON}^{\text{sat}}$ ), the leakage current ( $I_{OFF}$ ) and the subthreshold swing ( $S_{SW}^{\text{sat}}$ ). As in linear region, the  $I_{ON}^{\text{sat}}$  is the drain current at the maximum gate voltage whereas the  $I_{OFF}$  is the  $I_D$  at  $V_{GS} = 0$  V, i.e. the current that flows into the channel when the transistor is supposedly off. The subthreshold swing,  $S_{SW}^{\text{sat}}$ , is the reciprocal of the slope of the  $I_D - V_G$  curve in logarithmic scale below the threshold voltage, typically measured in mV/dec. The linear extrapolation method in saturation region is employed to extract the threshold voltage in saturation region,  $V_{TH}^{\text{sat}}$  [69, 68, 70]. The method is based on the description of the drain



(a)  $I_D - V_G$ (left) and  $g_m^{\text{lin}}(V_G)$ (right). Highlighted, the parameters extracted in linear region.



(b)  $I_D - V_G$  in saturation region. The  $I_{\text{OFF}}^{\text{sat}}$ ,  $I_{\text{ON}}^{\text{sat}}$ , and slope are indicated in red.



(c)  $\sqrt{I_D(V_G)}$  in saturation region. In red: the  $V_{th}^{\text{sat}}$  extracted with the linear extrapolation method.

Figure 3.5: Main MOSFETs parameters used for studying the radiation response [8].

current in saturation region as:

$$I_{DS}^{\text{sat}} = \frac{W}{2L} \mu C_{OX} (V_{GS} - V_{TH}^{\text{sat}})^2 \quad (3.3)$$

As illustrated in Fig. 3.5c, the  $V_{TH}^{\text{sat}}$  can be extracted as the intersection between the linear fit of the square root of Eq. 3.3 and the  $\sqrt{I_{DS}} = 0$   $A^{1/2}$ .

## Chapter 4

# Radiation-Induced Effects in Advanced CMOS Nodes

In Chapter 2, the charge build-up processes that occurs in oxides following exposure to ionizing dose were discussed. It is now well established that gate oxides are almost immune to ionizing radiation [71, 24], as their thickness is less than 3 nm, increasing the possibility of tunneling and thus making charge trapping highly unlikely. Studies conducted by Faccio and co-workers in [72] on the 130 nm CMOS technology node, which gate oxide is around 3 nm, demonstrated the immunity of TID for thin gate oxides up to ultra-high doses.

However, the STI and the *spacers* oxide are two additional oxides present in a typical MOS structure. The STI is used to isolate adjacent MOSFETs [73] whereas the spacer oxides are positioned alongside the polysilicon gate to allow the implantation of *Lightly Doped Drain (LDD)* extensions [74]. Contrary to the gate oxides, STI and spacers are much thicker and richer in defects therefore more prone to trap charge.

This chapter will provide an overview of the main TID-induced effects observed in nanoscale CMOS technology nodes. An in-depth discussion of these effects was provided by Borghello in [8]. As will be discussed further in Chapter 5, radiation significantly increases device-to-device variability [75]. Therefore, rather than focusing on the absolute value of each parameter after irradiation, it is more relevant to assess the general trend of its response to radiation.

The discussion will focus mainly on the 65 nm CMOS technology node, and many of these results have also been reported in:

[9] Borghello, G., Lerario, E., Faccio, F., Koch, H. D., **Termo, G.**, Michelis, S., Marquez, F. J., Palomo, F. R., Muñoz, F. (2021). "Ionizing radiation damage in 65 nm CMOS technology: Influence of geometry, bias and temperature at ultra-high doses". *Microelectronics Reliability*, 116, 114016.

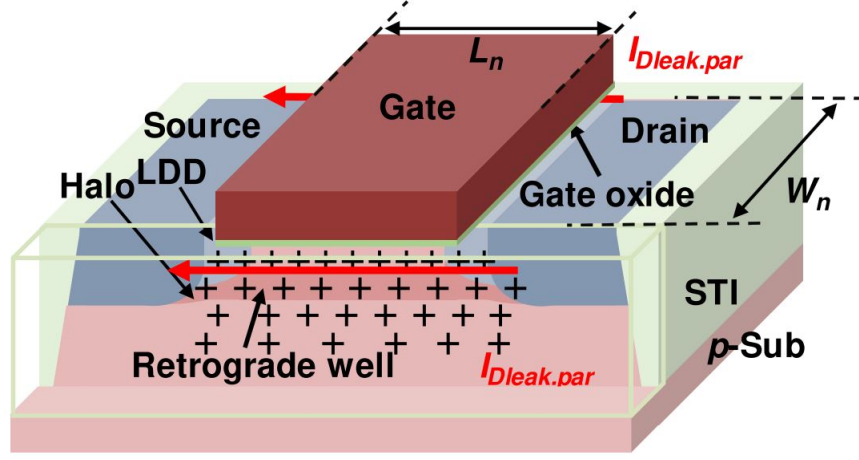


Figure 4.1: Visual representation of the parasitic channels created by the charge trapped in the STI in an nMOS transistor. After [8].

## 4.1 Effects Induced by Charge Trapping in STI

Ionizing radiation effects related to the presence of STI are a well known problem for the radiation hardness of CMOS technology. Many studies have been conducted on these oxides, especially for TID < 1 Mrad(SiO<sub>2</sub>) [76, 77, 24], level of dose compatible with space missions. Irradiation to ultra-high doses, has revealed additional details about the physical mechanisms influencing these effects [78, 79]. In the following, two main phenomena are discussed: the *radiation-induced drain-to-source leakage current* and the *Radiation Induced Narrow Channel Effect (RINCE)*.

### 4.1.1 Radiation-Induced Drain-to-Source Leakage Current

The radiation-induced increase in leakage current is one of the most relevant problems in CMOS technologies, since it has a direct impact on power consumption [80]. It is an effect common to all CMOS technology, from older nodes [81] to more advanced ones [82] or non-planar technology such as Fin Field-Effect-Transistors (FinFETs) [83, 79]. The increase in leakage current is mainly attributed to the radiation-induced charge trapping in the STI [78, 84, 72]. For an nMOS, trapped holes in the STI can invert the p-type substrate along the STI sidewalls and open two parasitic leakage paths parallel to the main channel as shown in Fig. 4.1 [8]. This allows the current to flow from drain to source even if the main transistor is turned off. In contrast, in pMOS the positive charge repels the holes near the STI/n-substrate interface, preventing the formation of such parasitic channels [22, 82].

The effects of the activation of the parasitic channels on the drain current are illustrated in Fig. 4.2. Three n-type transistors in 65 nm with same channel length  $L = 0.06 \mu\text{m}$  and different width from  $0.06$  to  $1.2 \mu\text{m}$  were irradiated to 1 Grad(SiO<sub>2</sub>) with  $V_{GS} = V_{DS} = V_{DD} = 1.2 \text{ V}$  during irradiation at room temper-

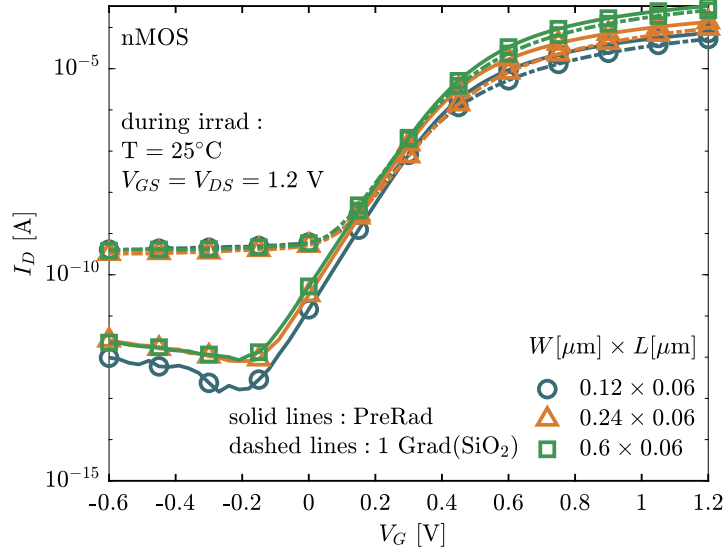


Figure 4.2:  $I_D - V_G$  curve of nMOS with  $W = 0.12, 0.24, 0.6 \mu\text{m}$  and  $L = 0.06 \mu\text{m}$  in 65 nm before irradiation (solid curves) and after 1 Grad( $\text{SiO}_2$ ). The irradiation provoked an increase of leakage current of  $\sim 2$  orders of magnitude.

ature. The opening of the parasitic channels caused an increase of the off-current of about 2 orders of magnitude.

A proof that the increase in leakage is caused by the parasitic channels and not the main channel comes from the observation that for  $V_G < 0 \text{ V}$  the drain current is independent of the gate voltage. This also indicates that the charge responsible for this effect may be located in the lower part of the STI where the influence of the gate voltage is lower [84, 85].

The length of the parasitic path is comparable to the length of the main transistor (the leakage current flows from source to drain), whereas the width is defined by the spatial distribution of trapped charge along the trench. Therefore, the  $I_{OFF}$  follows a  $1/L$  trend as it can be deduced from Fig. 4.3. The  $I_{OFF}^{\text{sat}}$  of nMOS transistors with different aspect ratio in 65 nm node is reported before and after irradiation to 500 Mrad( $\text{SiO}_2$ ). Before irradiation, the leakage current is dependent on the  $W/L$  ratio of the devices, i.e., the larger the ratio the higher the current. At ultra-high doses the current flowing in the parasitic channels overcomes the current flowing in the main channel, i.e., the pre-rad value. As a result, the current is dependent only on the length of the transistor, in fact, it is comparable in devices with the same length and different width. For devices with higher initial  $I_{OFF}^{\text{sat}}$ , the effects of the radiation-induced leakage current starts to become evident at higher levels of TID, since more charge is needed to induce enough parasitic current to overcome the leakage of the channel. As a consequence, for a given channel length, wider transistors have a smaller difference between pre- and post-irradiation  $I_{OFF}^{\text{sat}}$  (e.g., comparing  $0.12 \times 0.06$  and  $1 \times 0.06$  in Fig. 4.3) [9].

It is known that the off-current increase in older CMOS technology nodes, as 130 nm, is sensitive to the bias during irradiation, with greater degradation occurring when a gate voltage is applied [86, 87]. Given that the polysilicon/metal



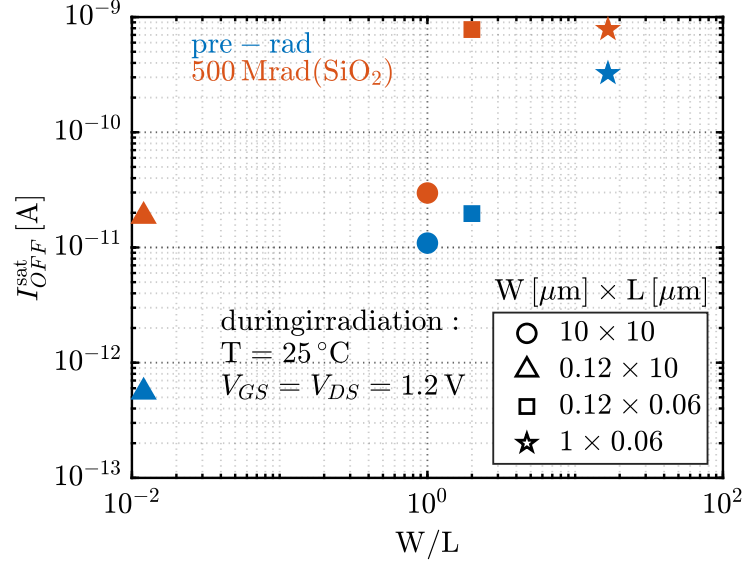


Figure 4.3: TID-induced off current increase of nMOS in 65 nm with different aspect ratio. Devices with different width and same length show the same  $I_{OFF}^{sat}$ , indicating that the parasitic current is dominating over the main channel leakage.

gate typically spans the STI, gate bias should have an impact on the electric field in the trench which in turn will affect the charge distribution [85, 88]. However in more advanced CMOS node, it was not possible to define a real worst case bias for this effect. Results in both 65 nm [9] and 28 nm CMOS nodes [89, 82], showed that the bias during irradiation has a marginal influence on the radiation-induced leakage current increase. This can be seen in Fig. 4.4 for a minimum size nMOS in 65 nm. The device was irradiated to 1 Grad(SiO<sub>2</sub>) in diode ( $V_{GS} = V_{DS} = V_{DD}$ ) and only  $V_{DS}$  ( $V_{GS} = 0V, V_{DS} = V_{DD}$ ) bias configuration.

Despite the radiation response for  $V_G > 0V$  is dependent on the applied bias, at  $V_G < 0V$  the parasitic current is the same for the two bias configuration, proving that in this technology, the radiation-induced leakage is negligibly influenced by gate bias during exposure. However, as it will be discussed in Chapter 5, the radiation response is strongly dependent on the manufacturing process, and therefore the bias independence of the off current increase should not be considered a general behaviour for all CMOS technologies.

Generally, the parasitic current anneals quickly, indicating that the opening of the parasitic path is due to positive charge captured in low-energy defects within the trench [8, 9]. A few hours at  $T = 100^\circ\text{C}$  are usually enough to restore the current to its pre-irradiation value.

One solution to suppress the radiation-induced leakage current available in CMOS technologies from 250 to 40 nm was the introduction of Enclosed Layout Transistor (ELT) (Fig. 4.5) [90, 91, 92, 21]. In an ELT transistor, the STI oxides are not in direct contact with the channel, making it impossible for the charge trapped within them to create leakage paths. However, the aspect ratio of an ELT is invariably greater than that of a standard transistor with an equivalent channel

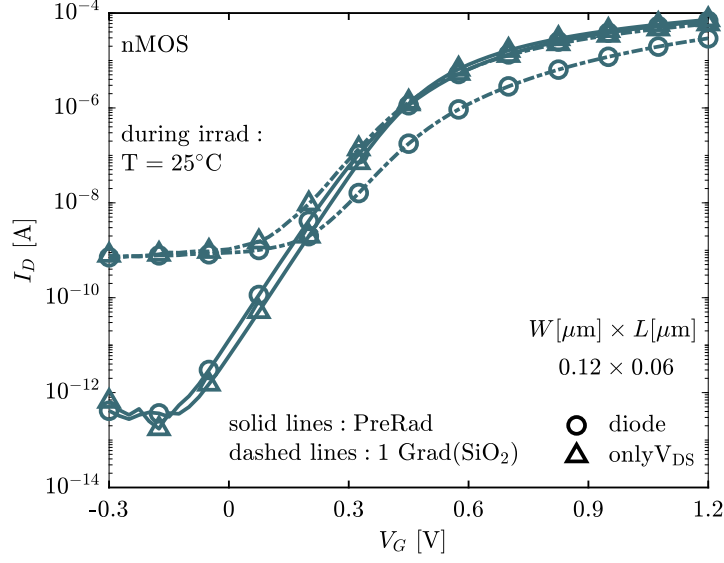


Figure 4.4: Influence of bias during irradiation of minimum size nMOS transistors. The device was irradiated in "diode" ( $V_{GS} = V_{DS} = V_{DD}$ ) and "onlyV<sub>DS</sub>" ( $V_{GS} = 0\text{ V}, V_{DS} = V_{DD}$ ) configuration. The off-current increase ( $V_G < 0\text{ V}$ ) is not dependent on the applied bias.

length, limiting its use in very high power designs. Furthermore, ELTs are no longer available in modern CMOS technology such as 28 nm.

#### 4.1.2 Radiation Induced Narrow Channel Effects

The charge trapped in the STI is also responsible for the dependence of the radiation response on the width of the transistor [87]. The electric field generated by the trapped positive charge influences the electric field in the main channel, causing variations in threshold voltage and transconductance. In narrower devices, a larger portion of the channel is affected by this lateral electric field, resulting in greater sensitivity to TID as illustrated in Fig. 4.6. This phenomenon is therefore known as Radiation Induced Narrow Channel Effects [72, 8].

The effects of RINCE on transistors in 65 nm are illustrated in Fig. 4.7. The devices were irradiated to 400 Mrad( $\text{SiO}_2$ ) with bias  $V_{GS} = V_{DS} = 1.2\text{ V}$ . The choice of long transistors is to reduce the contribution of radiation-induced short channel effects which will be discussed in the next section.

The  $I_{ON}^{\text{sat}}$  is decreasing as the TID increases and the degradation is more severe in narrower transistors for transistors of both polarity. In nMOS for TID  $< 2\text{ Mrad}(\text{SiO}_2)$ , there is an increase of the on-current caused by the positive charge trapped in STI which lowers the threshold voltage. After 2 Mrad( $\text{SiO}_2$ ), the build-up of negative interface starts to compensate for the effects of the positive charge eventually decreasing the current. In pMOS since the charge in the oxides and at the interface has the same sign (positive) the two effects combine, leading to a greater degradation. This is observed in all CMOS nodes as it was explained in Chapter 2. The TID-response of the on-current is caused by the effects of

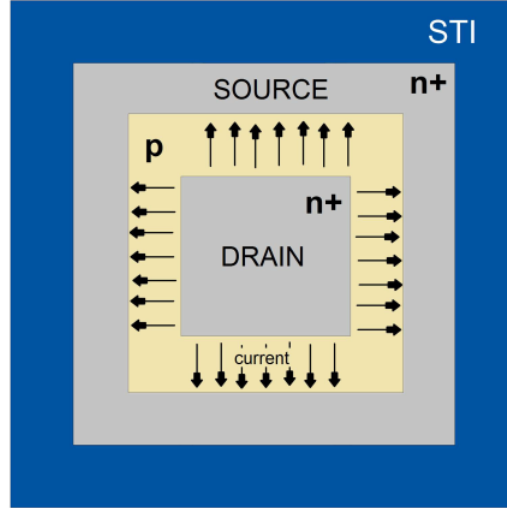


Figure 4.5: Schematic drawing of the geometry of an ELT. After [8]

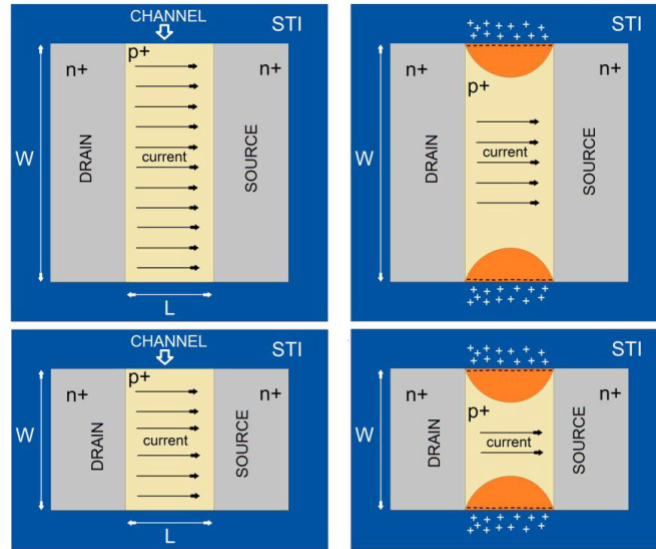


Figure 4.6: Schematic representation of charge accumulation provoking RINCE for wide (top row) and narrow (bottom row) nMOS transistors. The narrower the transistors the larger is the portion of the channel (orange area) affected by the electric field generated by the charge in the STI [8].

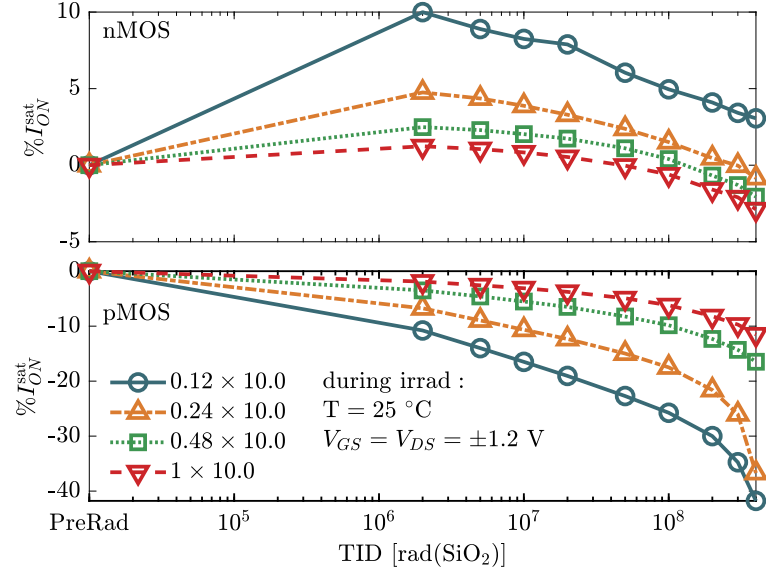


Figure 4.7: Percentage variation of the  $I_{ON}^{\text{sat}}$  of long channel MOS transistors irradiated to 400 Mrad( $\text{SiO}_2$ ) in diode configuration. The degradation is more evident on narrower devices.

the charge in the STI on both the  $V_{TH}^{\text{sat}}$  and  $g_m^{\text{sat}}$  as illustrated in Fig. 4.8 for the narrowest and widest devices of Fig. 4.7.

Although the increase in leakage and RINCE are both caused by the charge trapped in the STI, they seem to behave differently. The leakage current increases monotonically, for example in 65-28 nm [9, 82], while the RINCE exhibits a rebound. Their different behavior is also evident from the bias dependence of the RINCE shown in Fig. 4.9.

Bias during irradiation has an influence on RINCE with nMOS devices being more sensitive to the applied bias. After the peak, a  $V_{GS} > 0$  V tends to decrease the current while applying a  $V_{DS} > 0$  V provokes a second increase of the current which does not saturate even at 700 Mrad( $\text{SiO}_2$ ). Such effect is called Ultra-high dose Drain Current Increase (UDCI) and was briefly studied in [8]. P-type transistors, instead, exhibit a mild dependence on bias only at ultra-high doses where applying a negative bias to the gate provokes the largest degradation.

The reason for the difference between off-current increase and RINCE could be related to the location of the charge in the STI. As suggested by Bonaldo and co-author for the 28 nm node [93], RINCE might be caused by the charges trapped in the corner of the STI near the channel whereas the leakage increase could be caused by the charges located deeper in the trench where it is easier to open the parasitic path.

## 4.2 Radiation-Induced Short Channel Effects

Spacers are insulating layers used during the manufacturing process in advanced CMOS technologies to enable the implantation of LDD needed to reduce effects

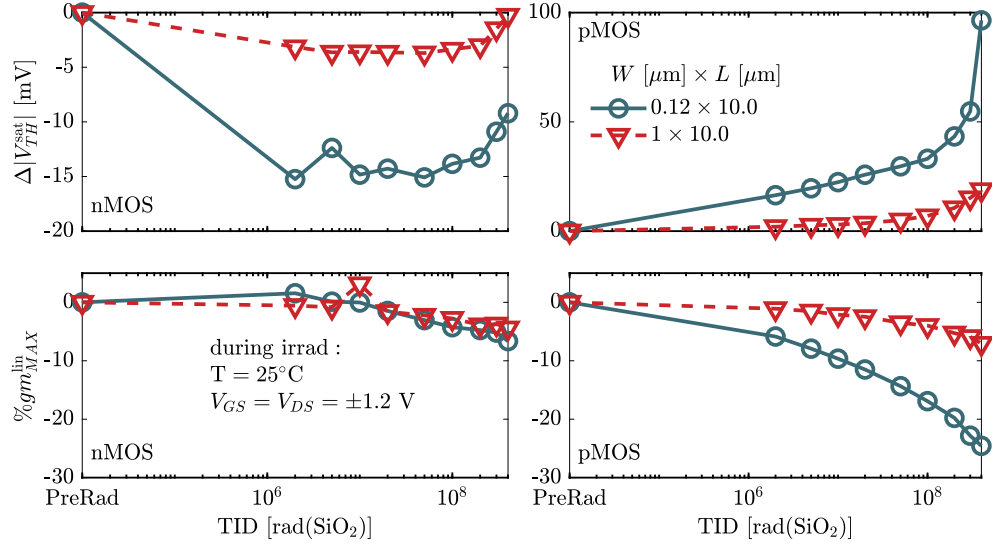


Figure 4.8: Extraction of the  $V_{TH}^{sat}$  (top row) and  $gm_{MAX}^{sat}$  (bottom row) of the minimum and maximum width transistors of Fig. 4.7.

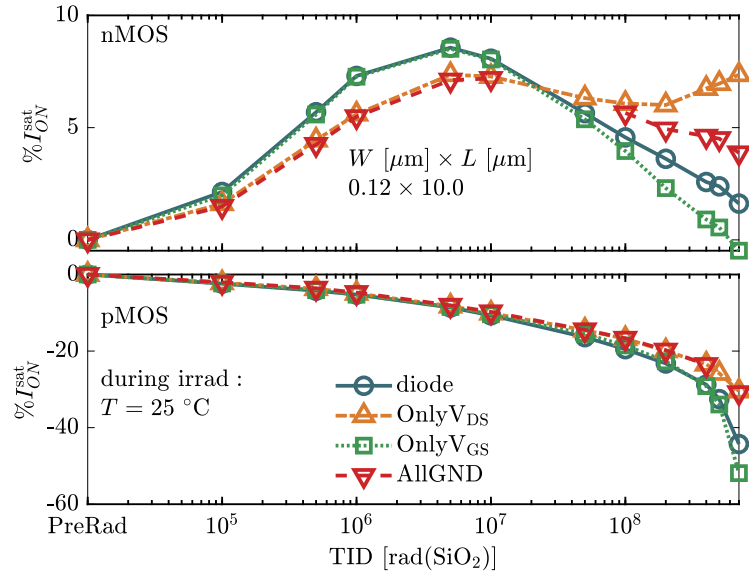


Figure 4.9: Influence of bias during irradiation on the radiation response of narrow and long transistors. For TID < 10 Mrad(SiO<sub>2</sub>) only nMOS exhibit a slight dependence on bias. For higher doses, the influence of bias becomes evident with the "only V<sub>GS</sub>" ( $V_{GS} = \pm 1.2 V, V_{DS} = 0 V$ ) configuration inducing the largest degradation of the  $I_{ON}^{sat}$ .

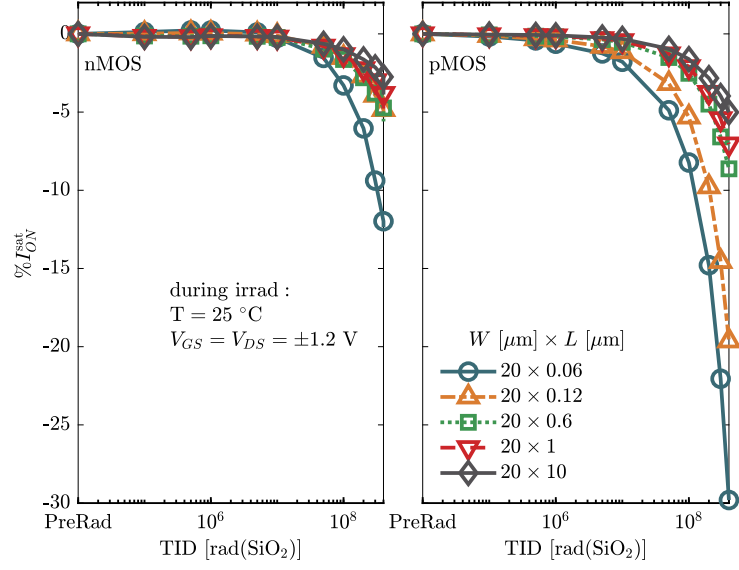


Figure 4.10: Percentage variation of the  $I_{ON}^{sat}$  of wide channel MOS transistors irradiated to 400 Mrad( $\text{SiO}_2$ ). The degradation is more evident in shorter devices.

such as hot carriers [94]. The spacers usually consist of an approximately 10-20 nm layer of  $\text{SiO}_2$  topped by a thick layer of  $\text{Si}_3\text{N}_4$  [95]. These oxides are generally made by a Chemical Vapor Deposition (CVD) technique, so they have lower quality than thermally grown gate oxides. The thickness and poor manufacturing quality make the spacers susceptible to charge trapping. Spacer-related effects are evident only for doses above 1 Mrad( $\text{SiO}_2$ ), doses much higher than those of interest for space applications. Studies on these effects have been conducted only in recent years and particularly on the 130 nm [72] and 65 nm nodes [8, 9, 96, 15].

The term Radiation-Induced Short Channel Effects (RISCE) indicates the dependence of radiation response on transistor length, with shorter devices exhibiting greater degradation, hence the name. Since these effects have been extensively treated for the 65 nm CMOS node, RISCE will be discussed with reference to transistors of this technology.

Fig. 4.10 shows the radiation response of wide nMOS and pMOS exposed to 400 Mrad( $\text{SiO}_2$ ), ELTs and wide transistors are particularly useful for studying spacer-related effects because of their lower sensitivity to accumulated charge in the STI, as previously discussed.

There is a relevant  $I_{ON}^{sat}$  decrease during irradiation for transistors of both polarities. The magnitude of the degradation is dependent on channel length, with the minimum length devices exhibiting the largest degradation.

The causes of degradation have been studied in the literature [95, 8] and two mechanisms were identified as the underlying causes:

- build-up of charge in the spacers which increases the source-drain resistance which reduces the effective  $V_{GS}, V_{DS}, V_{TH}$ ;
- temperature activated transport of  $\text{H}^+$  into the gate oxide where they form

interface traps causing significant threshold voltage shift;

In pMOS, the transport of charge appears only at high temperature making it possible to study the two effects separately therefore the discussion will focus on these devices [95].

The decrease in on current (Fig. 4.11a) during irradiation is caused by the charge trapped in the spacer, which locally reduces carrier concentration increasing the series resistance ( $R_{SD}$ ). While the  $R_{SD}$  is more or less the same regardless of transistor size, the current through it is greater in shorter transistors and thus the effects are more pronounced [72]. The variation of  $V_{TH}$  during irradiation is almost negligible (excluding the minimum length) and therefore could not explain the observed current decrease as shown in Fig. 4.11b. During high temperature annealing, the transport of  $H^+$  from the spacers to the gate oxide is activated and a significant shift of the threshold voltage occurs, which causes a further decrease of the current, as shown in the right side of Fig. 4.11. The RISCE is influenced by the bias applied during the exposure and the diode configuration ( $V_{GS} = V_{DS} = V_{DD}$ ) is the bias that causes the maximum degradation [72, 95]. The effects of RISCE are instead milder at lower temperature [95].

Theoretically in MOSFETs, source and drain should be symmetric, i.e., no difference should appear in the device characteristics when switching their role.

However, post-irradiation annealing at high temperature makes the transistor highly asymmetrical. Fig. 4.12 shows the  $V_{TH}^{sat}$  extraction of pMOS ELTs of three different lengths after irradiation and after high temperature annealing. The devices were measured in nominal nominal (NOM) and reverse (REV) configuration, i.e. with the source and drain terminals reversed with respect to their roles during irradiation and annealing. After irradiation, the threshold voltage shift is negligible and almost identical in NOM and REV. After annealing, a strong shift of the threshold voltage as a function of channel length is observed, which is more severe in NOM [9]. This asymmetry only appears when a drain bias is applied. Applying a  $V_{DS} < 0$  V bias, inhibits the transport of  $H^+$  on the drain side and facilitates it on the source side in pMOS devices, whereas the dual happens for nMOS.

RISCE is an effect observed in the 130-65 nm CMOS technology nodes. However, it should be noted that in the more advanced 28 nm node this effect was not observed. The figure shows the radiation response of transistors of different lengths in the 28 nm CMOS technology. A different dependence of the radiation response on the channel length can be observed. In this node, the use of short-channel transistors results in better radiation hardness as illustrated in Fig. 4.13.

This Reverse Radiation Induced Short Channel Effect was explained by Bonaldo and co-authors in [11]. The decreased sensitivity of short channel devices was explained as induced by the overlap of halo implants in short channel transistors as it will be discussed in the next section. Halo implants are very often employed in modern CMOS technology to reduce the impact of short channel effects [97]. Moreover, in the 28 nm we do not observe the temperature-activated transport of hydrogen and the consequent asymmetry, confirming that down-scaling improves the radiation response of CMOS technology.

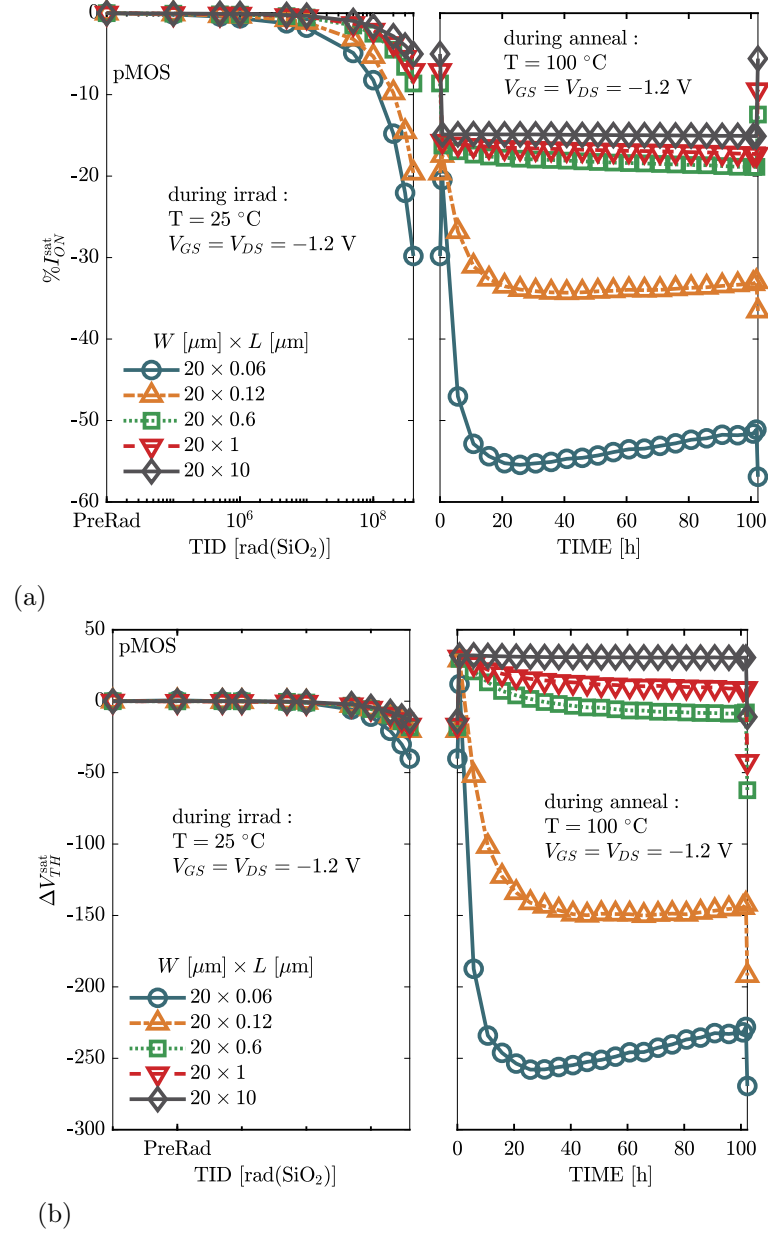


Figure 4.11:  $\%I_{ON}^{\text{sat}}$  (top) and  $\Delta V_{TH}^{\text{sat}}$  (bottom) of wide channel pMOS devices irradiated at room temperature and then annealed at  $T = 100^\circ\text{C}$ . High temperature provokes an additional decrease of the  $I_{ON}$ .



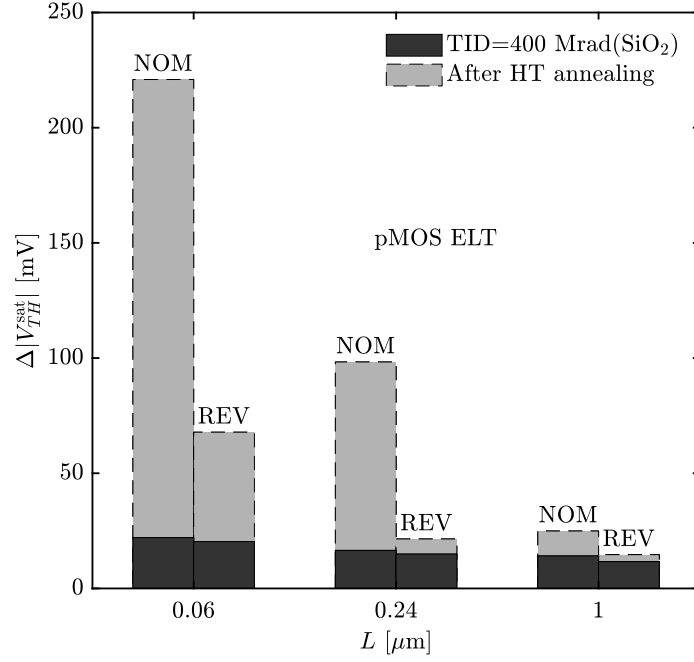


Figure 4.12:  $\Delta V_{TH}^{sat}$  of 3 ELT pMOS measured after irradiation and after high-T annealing in nominal (NOM) and reverse (REV) configuration. High-T annealing makes the irradiated devices strongly asymmetric ([9]).

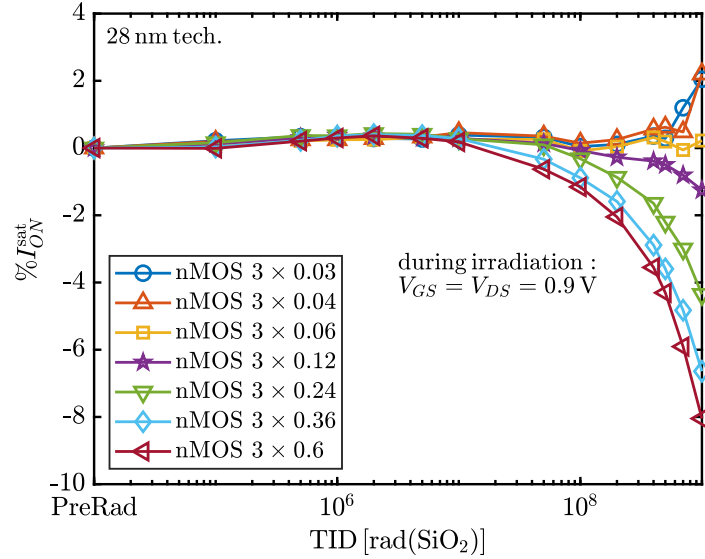


Figure 4.13: Percentage variation of the on-current of short channel n-type transistors in 28 nm CMOS technology. Shorter devices exhibit a less severe degradation as a consequence of the overlapping of halo implants.

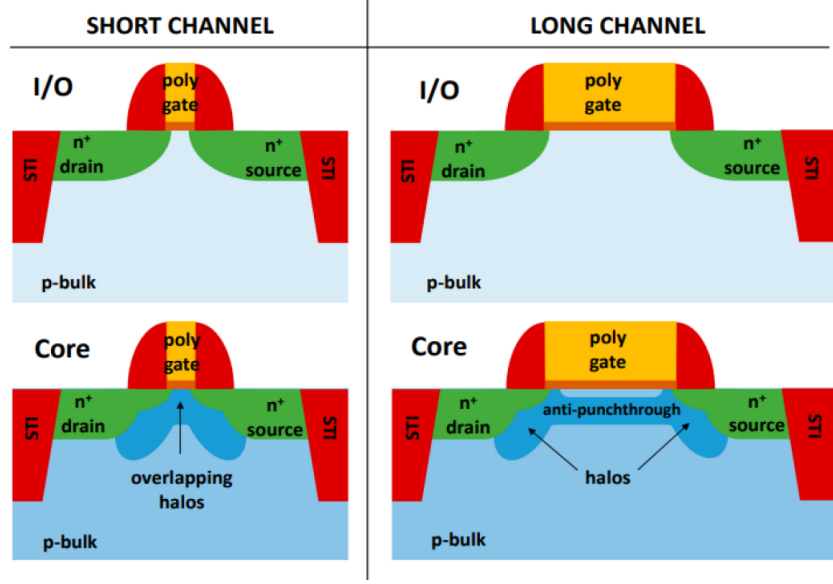


Figure 4.14: Schematic representation of I/O and core nMOS with short (left) and long channel (right) nMOS. In core transistors usually anti-punchthrough and halo implantations are employed (bottom). After [10].

### 4.3 Halo Implants Influence

The continued scaling of technology nodes has highlighted the limitations of traditional CMOS fabrication techniques, necessitating the development of new solutions. One such problem is the punch-through effect, which results from the short channel length in smaller devices [98, 99]. As the channel length ( $L$ ) approaches the depletion width of the source/drain junction, there is an increase in leakage currents, a degradation of the subthreshold oscillation, and a reduction in the threshold voltage. In addition, very short channel lengths increase the risk of transistor response collapse due to very high leakage currents and loss of gate control over the channel [100, 101]. To overcome these limitations two different solutions are employed in modern MOS transistors: anti-punchthrough implantation and halo implantation. Punchthrough implantation are a highly doped bulk-region implanted a few nanometers under the gate oxide, whereas halos are implanted close to source and drain implants deeper in the bulk, as summarized in Fig. 4.14 [10]. Halos prevent the loss of  $L_{eff}$  by limiting the expansion of the source/drain depletion region into the channel area [102, 103]. Consequently, the bulk doping is no longer uniform.

Over the years, different studies proved that increasing the doping of the bulk doping along the STI sidewalls reduces the radiation-induced leakage current [104, 84, 85]. Therefore, since the halo implants affect the doping in channel area along the STI sidewall they can influence the radiation response of MOS transistors.

The overlapping of halo implants in short channel transistors can result in an improved radiation-response with respect to longer channel transistors, an effect called Reverse Short Channel Effect (RSCE) [11, 10, 105]. This effect is visible

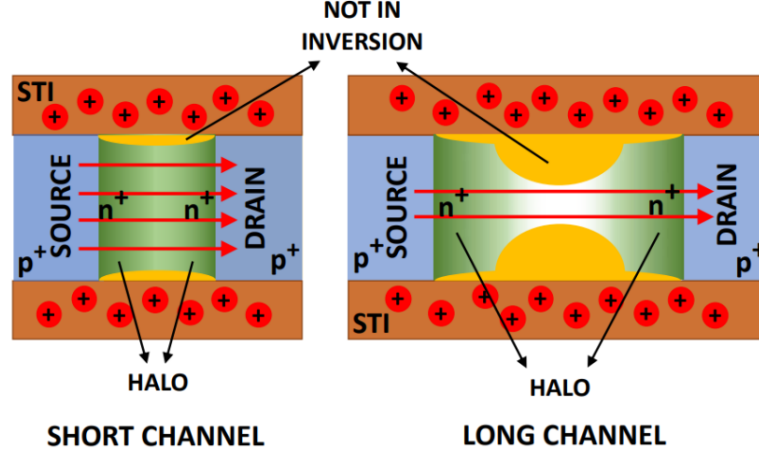


Figure 4.15: A top view of pMOS transistors is shown along a horizontal cut-plane just below the gate oxide in both long and short channel devices. This schematic illustrates the TID mechanism associated with STI (Shallow Trench Isolation) charge buildup, as well as the effect of halo implantation in narrow MOSFETs biased in strong inversion and the linear region (low  $V_{DS}$ ). Red arrows represent the current flow in the channel, while yellow areas denote the surface regions that, due to the trapped charge in the STI, are not in inversion. The shaded green areas indicate the bulk doping level, with the dark green regions highlighting the halo implantation areas. After [11].

only in narrow channel transistors where the radiation response is dominated by charge trapped in STI. Bonaldo and co-authors explained RSCE as a result of the threshold voltage increase caused by the overlapping of halos in short channel. Such increase is also responsible of the improved radiation response of short channel transistors compared to longer channel devices, contrary of what observed in previous CMOS nodes (RISCE). In particular, in short-channel devices, the overall increase of the bulk doping caused by the halo reduce the extension of the lateral not-inverted regions responsible for RINCE as depicted in Fig. 4.15. This was proved by Bonaldo and co-authors via TCAD simulations in [11].

The improved radiation response of short-channel devices is a common feature of aggressively scaled CMOS technology as observed also in the 28 nm CMOS technology treated in this thesis (Fig. 4.13) and in more advanced FinFET technology [83, 106].

## 4.4 Enhanced Low Dose-Rate Sensitivity

ELDRS describes the more severe degradation that devices exhibit when exposed with low dose-rates compared to that measured at high dose-rates. In some cases, this difference can be several orders of magnitude and is a major problem in radiation hardness assurance. The problem is caused by the fact that, generally, radiation qualification tests are performed at high rates and thus may underes-

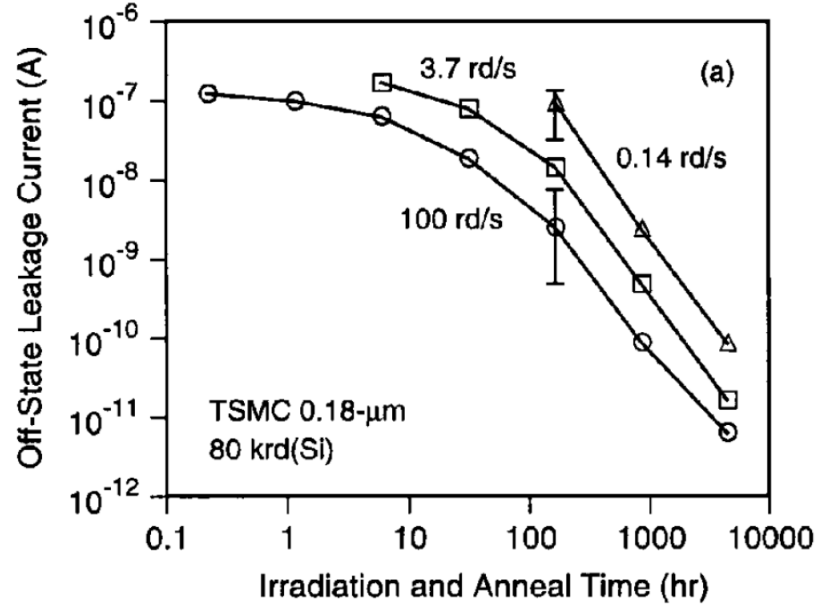


Figure 4.16: Evidence of ELDRS of the leakage current of MOS transistors in 180 nm technology. After [12]

estimate the damage in low rates radiation environments. Although ELDRS is a known problem in Bipolar Junction Transistor (BJT) devices, MOSFETs are generally considered immune to dose-rate effects. However, in the 2000s it was shown that MOS transistors in 350 nm, 250 nm and 180 nm also suffer from ELDRS. Fig. 4.16 reports a representative example of the ELDRS of the leakage current of devices in 180 nm suggesting that in these technologies STI mechanisms were influenced by DR. It is evident that for any combination of irradiation + annealing time, the leakage current is higher in devices irradiated at lower dose-rate. However, in the same study, devices from two other CMOS technology processes, 500 nm and 350 nm, did not exhibit any dependence on DR. This results highlights that ELDRS depends strongly on the manufacturing process. More recently, it has been shown that the effects related to spacer oxides in 130 nm and 65 nm are susceptible to true dose-rate sensitivity. In this section, ELDRS will be discussed focusing on this latest node. The following discussion is based on:

[15] Borghello, G., Faccio, F., **Termo, G.**, Michelis, S., Costanzo, S., Koch, H. D., Fleetwood, D. M. (2021). "Effects of bias and temperature on the dose-rate sensitivity of 65-nm CMOS transistors". IEEE Transactions on Nuclear Science, 68(5), 573-580.

#### 4.4.1 ELDRS in 65nm CMOS technology

The dose-rate dependence of the damage in pMOS transistors is shown in Fig. 4.17 for a standard  $1.32 \mu\text{m} \times 0.06 \mu\text{m}$  irradiated in diode configuration ( $V_{GS} = V_{DS} = V_{DD}$ ) up to 50 Mrad( $\text{SiO}_2$ ). The device was irradiated at different dose rates ranging from 30 krad( $\text{SiO}_2$ )/h to 10 Mrad( $\text{SiO}_2$ )/h at  $T = 25^\circ\text{C}$ . It is evident that

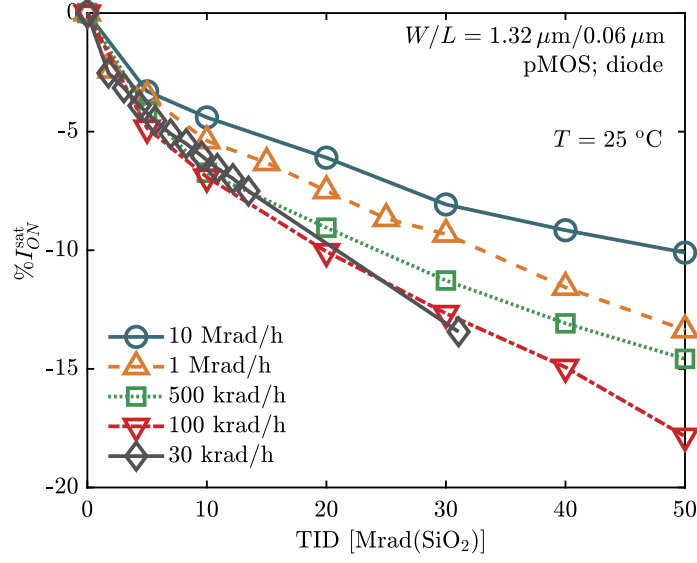


Figure 4.17:  $\%I_{ON}^{\text{sat}}$  degradation for standard  $1.32 \mu\text{m} \times 0.06 \mu\text{m}$  pMOS transistor irradiated to  $\text{TID} = 50 \text{ Mrad}(\text{SiO}_2)$  with different DRs. Lower DRs cause more degradation.

devices irradiated at a lower dose rate show greater degradation, which almost doubles in the case of the highest dose rate compared to the lowest dose rate. It is important to note that the “enhanced” degradation appears to saturate around  $100 \text{ krad}(\text{SiO}_2)/\text{h}$ , which means that, at least for this technology, it is possible to test directly under this worst-case scenario while saving a great deal of time and funds.

To understand whether dose-rate sensitivity is caused by effects occurring in the STI and/or spacer oxides, irradiation campaigns were carried out using ELTs and narrow and long (NAL) transistors. As highlighted in the previous sections, ELTs allow the study of spacer-related effects, while NAL allow the study of STI-related effects. The results of this investigation are reported in Fig. 4.18.

The time scale in the two experiments considered is significantly different, with the High Dose-Rate (HDR) test being 100 times faster than the Low Dose-Rate (LDR) one. To rule out time-dependent effects, and to make sure that what is observed is a true dose-rate dependence, the devices irradiated at HDR have been kept under bias at  $T = 25^\circ\text{C}$  for the time required by the LDR experiment to reach the same dose. This ensures that the larger degradation in the LDR test is caused by a true enhanced dose-rate sensitivity.

The narrow/long device is more damaged by TID but its degradation is almost the same for the two different DRs, indicating that the mechanisms taking place in the STI are mildly influenced by dose-rate. In the ELT device, the damage at the end of irradiation is almost double in the LDR experiment compared to the HDR one. Since ELT devices are immune from STI-related effects, it is safe to say that the different degradation must be due to radiation effects taking place in the spacers. The same conclusion is true also for nMOS as indicated by the results in Fig. 4.19.

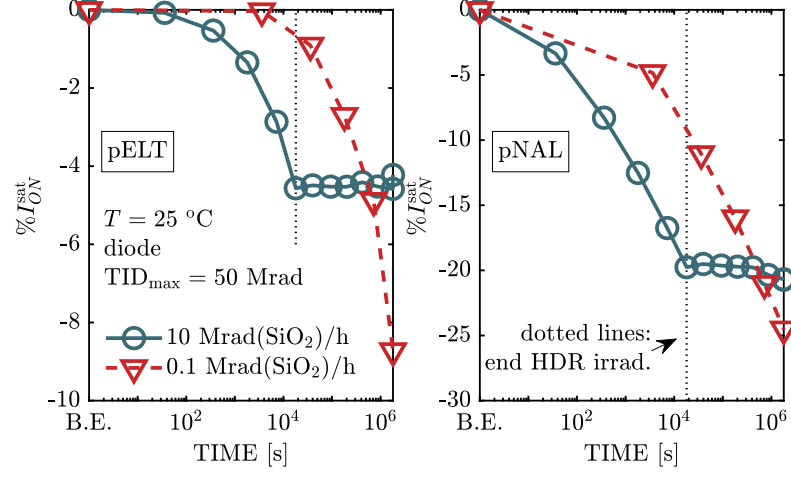


Figure 4.18: Percentage variation of the maximum drain current for ELT and NAL pMOS transistor irradiated to 50 Mrad( $\text{SiO}_2$ ) with two different dose rates, in diode configuration at room temperature. The dotted line indicates the end of the high-dose irradiation.

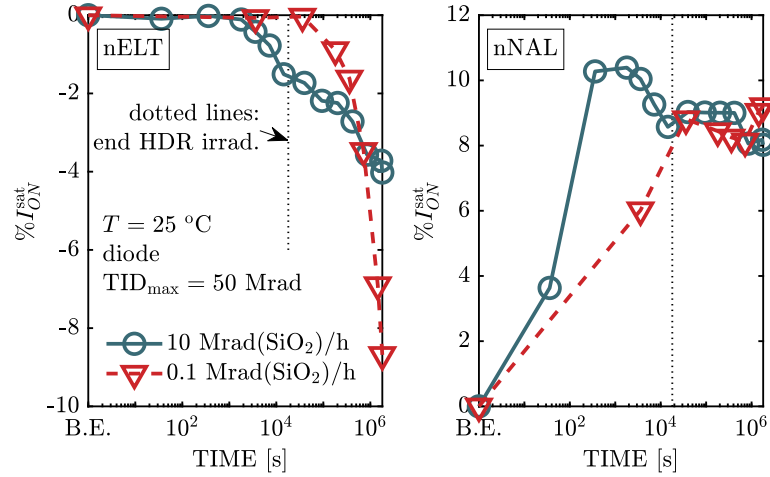
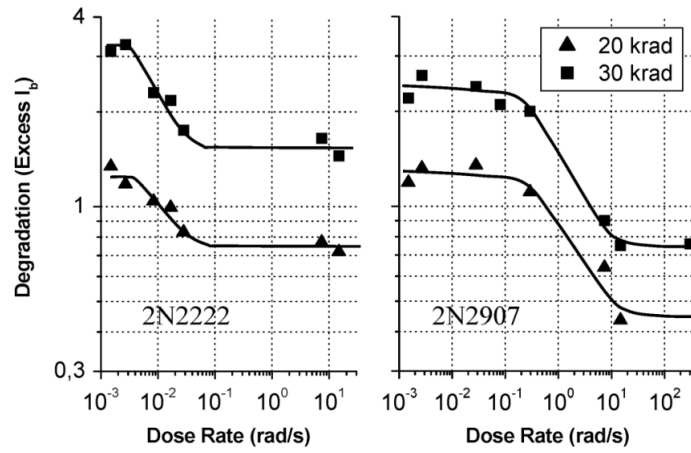
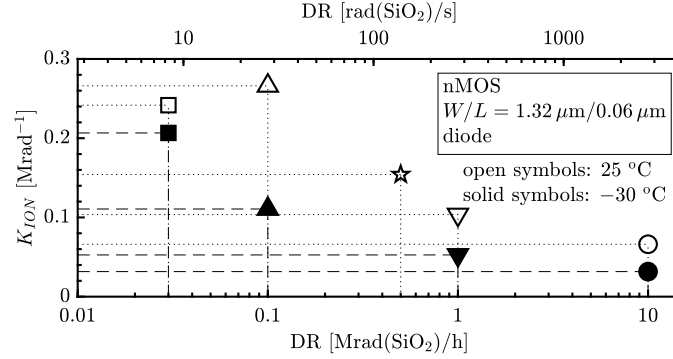


Figure 4.19: Percentage variation of the  $I_{ON}^{\text{sat}}$  for ELT and  $0.12 \mu\text{m} \times 10 \mu\text{m}$  (NAL) nMOS irradiated to  $\text{TID} = 50\text{Mrad}(\text{SiO}_2)$  with 10 and 0.1 Mrad( $\text{SiO}_2$ )/h DRs. As for pMOS, the x-axis reports time to allow a direct comparison between HDR and LDR irradiation. The dotted line indicates the end of high dose-rate irradiation.



(a)



(b)

Figure 4.20: The dose-rate dependence saturates at both high and low dose rates, resulting in a characteristic inverted S-shaped curve. Fig. 4.20a illustrates this behavior for bipolar devices ([13, 14]), while Fig. 4.20b presents the results for MOS transistors in 65 nm CMOS technology ([15]).

The physical mechanisms driving ELDRS in CMOS devices appear to be well described by the models originally developed for bipolar transistors. The increase in leakage current observed at low dose rates in [12] is attributed to the modulating effect of space charge on the trapping and annealing dynamics within the STI. Measurements at various temperatures and dose-rates were performed on the 65 nm CMOS node. The results showed that, for a given TID, current degradation saturates at both high and low DR, forming the characteristic inverted S-shaped curve measured in BJT devices sensitive to ELDRS [25, 107, 108, 109, 110, 14]. The comparison between the S-shaped plot in BJT and the results obtain in MOS transistors is reported in Fig. 4.20 which confirms the similarity between the two physical mechanisms. It is important to note that, at low temperatures, the entire S-curve shifts towards lower dose rates. A similar shift in the S-curve was predicted for bipolar devices in [110].



## Chapter 5

# Enhanced Process Variability of CMOS Technology at Ultra-High Doses

As semiconductor technologies continue to shrink, achieving higher integration density and improved chip performances, the effects of process variations have become one of the main issues in modern CMOS technology [111]. Process variations refer to all those fluctuations of the fabrication process that directly affect the electrical characteristics of interconnections and transistors, with the latest being the focus in this chapter. Such process variations can be either systematic, and therefore predictable, like variations due to lithography or doping profiles, or non-systematic variations which are less predictable and exhibit randomness. Process variations have a direct impact on the functionality of any chip since they increase mismatch and impacts the long-term reliability as it affects aging and wear-out mechanisms.

In recent years, many works focused on device-to-device variability showing how these variations in the manufacturing process could cause significant effects on the performance of virtually identical transistors [112, 113]. In the case of MOS transistors, the increase in variability in as-processed devices is primarily caused by minor variations in the production process, such as random dopant fluctuations [114], oxide thickness variations [113] and hydrogen concentration variations [115]. Several studies showed that the random statistical fluctuations in manufacturing process impact the radiation response of a given technology [116, 117, 75, 118, 119]. The production of radiation defects involves quantities such as dopants, hydrogen contents (see Chapter 2) therefore radiation can exacerbate the differences between theoretically identical devices which might not be as visible before irradiation. As a result, variability increases the costs and complexity of the radiation qualification process [120].

An extreme fab-to-fab variability was observed also in the 130 nm and 65 nm CMOS technology used for the ASICs developed for the upgraded High Luminosity LHC (HL-LHC) physics experiments. This mandated constant monitoring of the TID response of such technology to verify the consistency of the manufacturing process over time. To that end, technology monitoring chips have been added to

each production run of ASICs for particle detectors designed in the EP-ESE-ME section at CERN.

As of 2014, 22 chips from 3 different fabs in 130 nm and 10 chips from 2 different fabs in 65 nm were measured, some of them in different conditions of temperature and bias. The chips were irradiated to ultra-high doses, ranging from 100 Mrad(SiO<sub>2</sub>) to 1 Grad(SiO<sub>2</sub>). For purposes of non-disclosure, in the following, the three different factories will be referred to as Fab A, B, C.

Although the radiation-induced mechanisms in these technologies will be discussed to some extent, they are not the focus of the reported study. Extensive studies on the TID response of the 130 nm and 65 nm technologies have already been conducted in previous works and discussed in Chapter 4, and further details can be found in [87, 86, 72, 96, 121, 9, 15]. In this chapter, it will be shown the results of this unprecedented monitoring effort as well as its impact on the reliability of the radiation models of MOS developed in 65 nm to enable the simulation of ASICs including the degradation introduced by TID.

The discussion will be based on the results published in:

[122] Termo, Gennaro, et al. "Fab-to-fab and run-to-run variability in 130 nm and 65 nm CMOS technologies exposed to ultra-high TID." *Journal of Instrumentation* 18.01 (2023): C01061.

DOI 10.1088/1748-0221/18/01/C01061 available at:

<https://iopscience.iop.org/article/10.1088/1748-0221/18/01/C01061/meta>

All reported measurements and irradiations were performed with the setup described in Chapter 3 to avoid introducing systematic errors due to the measurement setup.

## 5.1 Off-Current Variability

In Chapter 4, the mechanism of radiation-induced increase in leakage current was explained. In nMOS devices, the charge accumulated in the STI causes the opening of parasitic paths between source and drain, resulting in a significant increase in leakage current and, consequently, in the power consumption of ASICs.

The most striking variability observed was the fab-to-fab difference in TID-induced leakage current in nMOS transistors in 130 nm. In Fig.5.1 are reported the off current increase measured in 22 runs (13 from Fab.A, 5 from Fab.B and 4 from Fab.C) of minimum size  $0.15\ \mu\text{m} \times 0.13\ \mu\text{m}$  nMOS standard threshold voltage flavor (svt). The irradiation were performed with X-ray to 1 Grad(SiO<sub>2</sub>) and the devices were biased in diode configuration. The devices from Fab.C exhibit a significant  $I_{OFF}^{\text{sat}}$  increase which peaks around 1 Mrad(SiO<sub>2</sub>) and then decrease eventually becoming comparable to the leakage measured in the devices from the two other fabs. This behavior can be explained by the different buildup time between the quick formation of oxide charge and the late buildup of interface traps which happen around 1 – 2 Mrad(SiO<sub>2</sub>) in this technology [87]. After their formation, the negative charge at the interface start to compensate for the threshold voltage reduction induced by the charge in the oxide and the typical "bump" behavior is observed. It should be noted that the observed differences are actually caused by

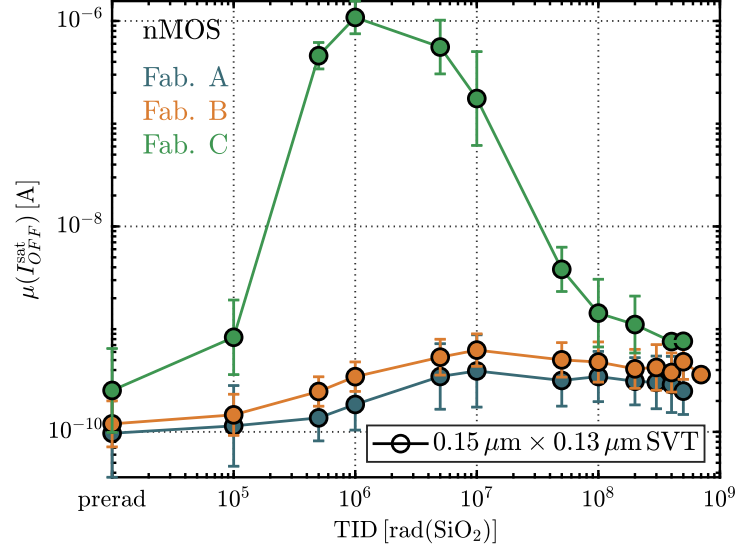


Figure 5.1: Mean  $I_{OFF}^{sat}$  of minimum size nMOS in 130 nm. The bars indicate the standard deviation. The leakage current peak at about 1 Mrad(SiO<sub>2</sub>) only, but consistently, in samples from Fab. C.

irradiation; in fact, devices from different fabs had similar leakage current before exposure.

Despite the large number of devices measured from Fab.B and C, no peak in leakage current was observed and the lot-to-lot variability (standard deviation bar in Fig.5.1) was practically negligible.

An important consequence of these observations is that the systematic use of ELT transistors can be avoided, provided that production in Fab.C is avoided, improving the performance of ASICs [91].

The same study was conducted also in the 65 nm CMOS technology node and the results are reported in Fig.5.2. In this technology only two fabs were available, therefore only the devices from Fabs B and C were investigated: 4 runs from Fab.B and 7 from Fab.C.

An important difference with the 130 nm is that in this technology none of the fabs exhibit a peak in the leakage current which indicates that leakage increase observed in Fab.C is specifically related to the manufacturing process of devices in 130 nm. An interesting observation is that although the mechanism underlying the  $I_{OFF}$  current increase is the same in both technologies, in the 65 nm node the current increases monotonically and does not saturate even at 1 Grad(SiO<sub>2</sub>). Despite these differences, the lot-to-lot and fab-to-fab differences were not as severe as in the previous node and their impact on the design approach is practically negligible.

The on-current fab-to-fab and lot-to-lot variability observed in nMOS was small and not practically significant therefore it will be discussed in the next section in the case of pMOS transistors.

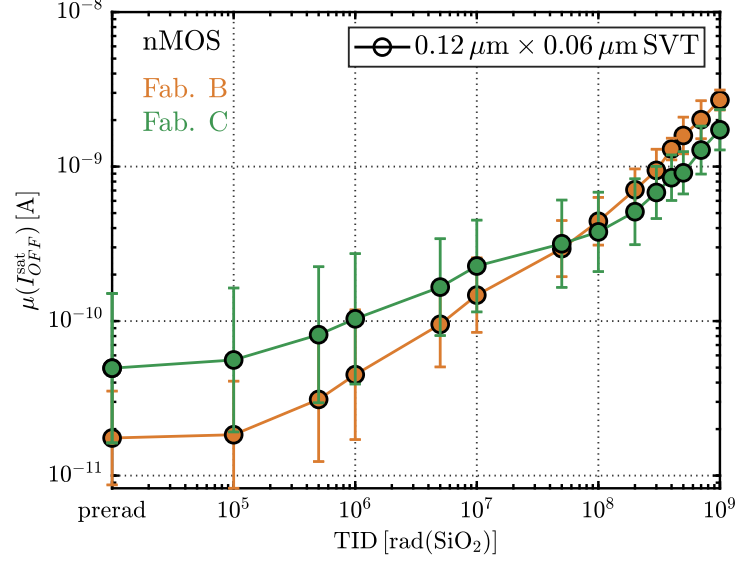


Figure 5.2: Mean  $I_{OFF}^{\text{sat}}$  of minimum size nMOS in 65 nm. The bars indicate the standard deviation. The leakage current monotonically increases and is similar in both fabs.

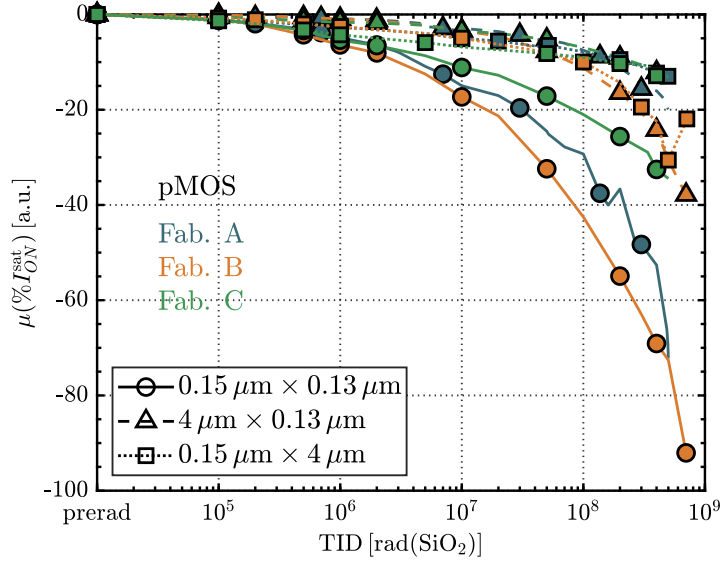
## 5.2 On-current

In pMOS devices, the charge trapped in the STI increases the threshold voltage of the lateral parasitic transistors, so the off-current is not an appropriate parameter to study radiation-induced variability. However, considerable fab-to-fab variability was observed in the on-current of pMOS transistors in both 130-65 nm CMOS nodes reported in Fig.5.3.

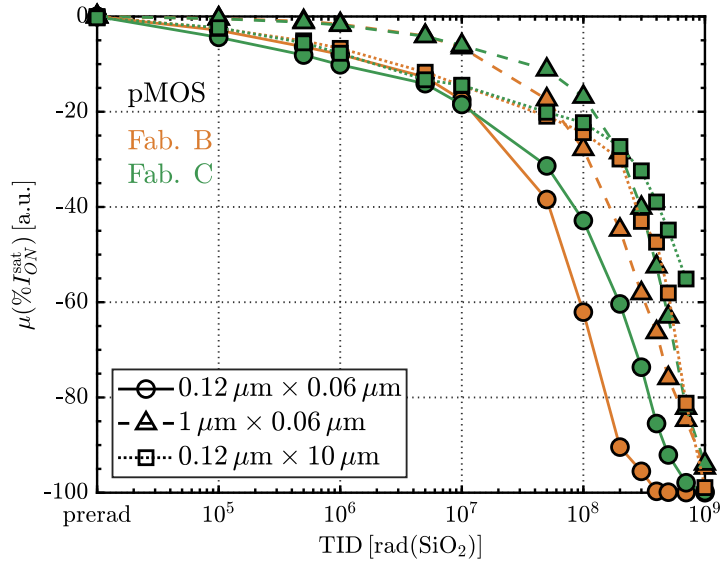
P-type transistors were irradiated up to 700 Mrad(SiO<sub>2</sub>) for the 130 nm and to 1 Grad(SiO<sub>2</sub>) for 65 nm node. Transistor sizes were chosen to be representative of the radiation response in these technologies. In minimum size transistors, the radiation response is a combination of STI and spacer oxide effects, in wide and long transistors it is mainly dominated by RISCE, and in narrow and long transistors it is instead influenced by RINCE, as discussed in Chapter 4. In both technologies, the minimum size devices exhibit the largest fab-to-fab variability. In 130 nm, at ultra high doses, the degradation in devices from Fab.B is twofold the degradation induced in devices from Fab.C, the same fab that in the case of nMOS transistors offered the poorest performance instead (Fig 5.1).

Transistor size dependence was also observed with respect to run-to-run variability. Fig.5.4 shows the average percentage degradation of the on-current of  $0.15 \mu\text{m} \times 0.13 \mu\text{m}$  and  $4 \mu\text{m} \times 0.13 \mu\text{m}$  pMOS transistors in all runs of the 130 nm node from Fab.A. Both the TID-induced degradation and its variability are considerably smaller for the wide/short transistor.

In nMOS transistors, the observed fab-to-fab or lot-to-lot variability was significantly smaller than that of pMOS and was practically not significant.



(a)



(b)

Figure 5.3: Mean  $\%I_{ON}^{sat}$  as a function of TID of minimum size (circles), wide/short (triangles), narrow/long (squares) pMOS transistors in 130 nm (a) and 65 nm (b) CMOS technology. Fab-to-fab variability is larger in minimum size devices.

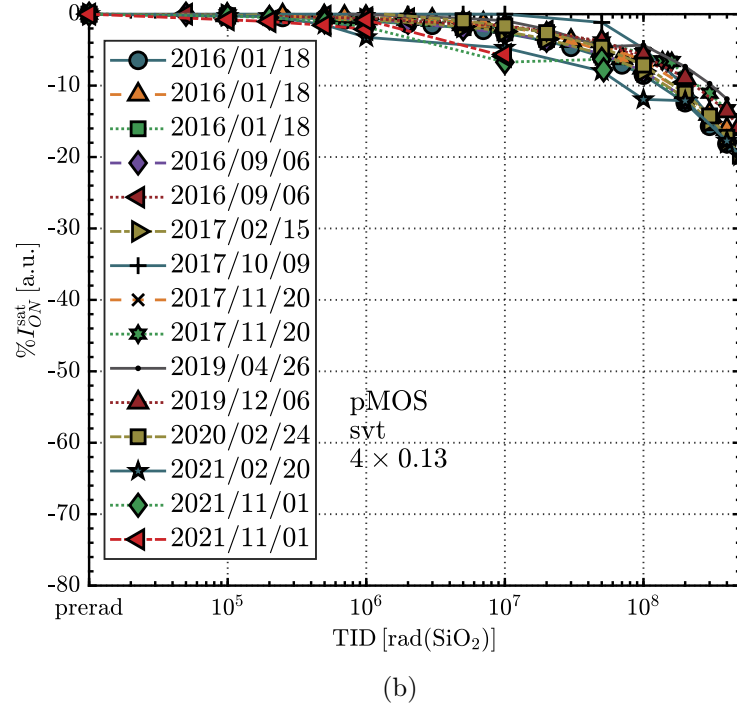
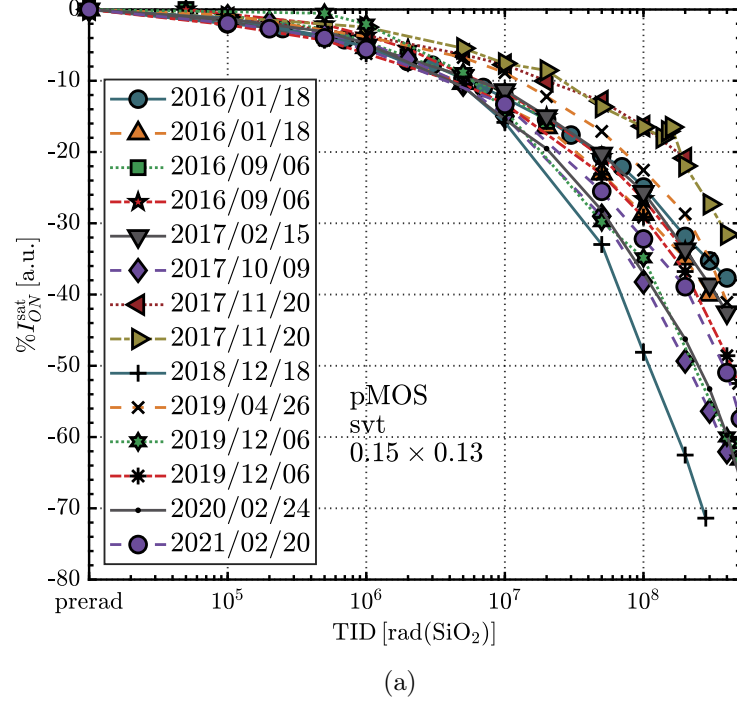


Figure 5.4: Run-to-run variability of  $\%I_{ON}^{sat}(TID)$  of minimum size (a) and wide/short (b) pMOS transistors in 130 nm CMOS technology from Fab.A.

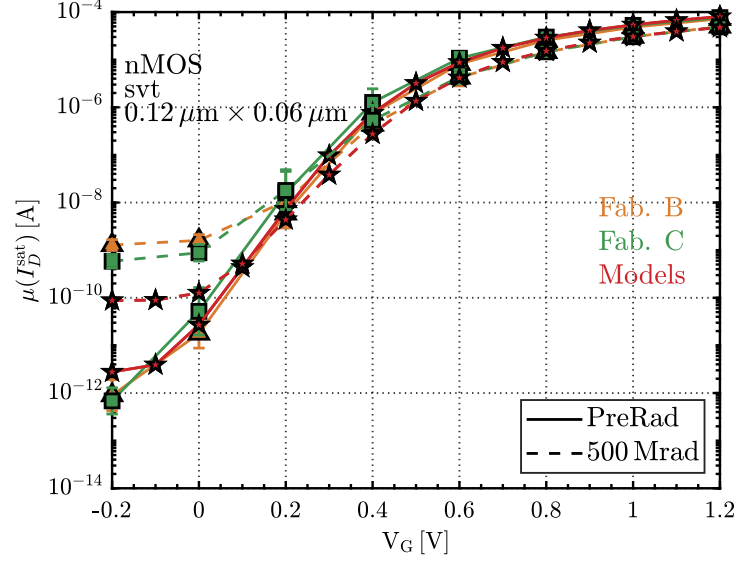


Figure 5.5: Comparison of the mean  $I_D - V_G$  characteristics over all the available runs and simulation of minimum size nMOS transistors in 65 nm CMOS technology.

### 5.3 Variability and SPICE-level Radiation Models

Compact MOSFET models, such as Berkeley Short-channel IGFET Model (BSIM) [123] or Enz-Krummenaker-Vittoz (EKV) [124], do not take TID effects into account. Therefore, when designing ASICs for the HL-LHC particle detector, CERN designers developed 65 nm CMOS transistor models based on BSIM4. The goal was to adapt the process design kit provided by the foundry to include TID effects at very high levels. The result of this effort, provided transistor models that reasonably predicted the behavior of MOSFETs in 65 nm up to 500 Mrad( $\text{SiO}_2$ ). Details on the models and their performance are available in [125, 126, 127, 128]. However, these models use data gathered on samples from one single run, since the wide dataset provided in this thesis was not available at the time.

Comparison of the prediction from the models with measured variable degradation is a thus useful exercise providing ASIC designers with a benchmark for their post-rad circuit simulations.

Fig.5.5, shows the comparison between the mean  $I_D - V_G$  measured in all the runs of  $0.12 \mu\text{m} \times 0.06 \mu\text{m}$  nMOS minimum size transistors and the simulations before and after exposure to 500 Mrad( $\text{SiO}_2$ ). The models accurately predict the behavior of pristine devices and the irradiation-induced threshold voltage shift. However, the increase in leakage current is underestimated by an order of magnitude in samples from both fabs.

P-type transistors are generally modeled reasonably well, with the exception of Fab.B minimum-size transistors, whose post-rad degradation is strongly underestimated, as shown in Fig.5.6. This again evidences the greater variability of the smaller transistors.

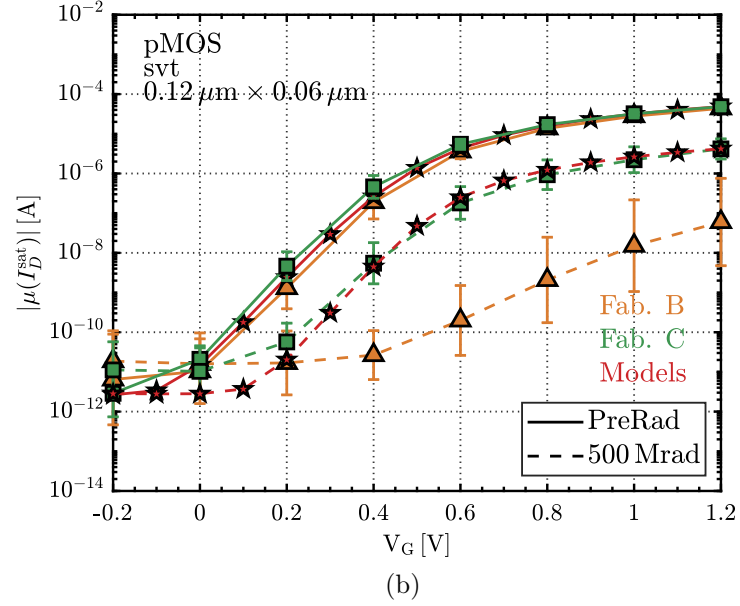
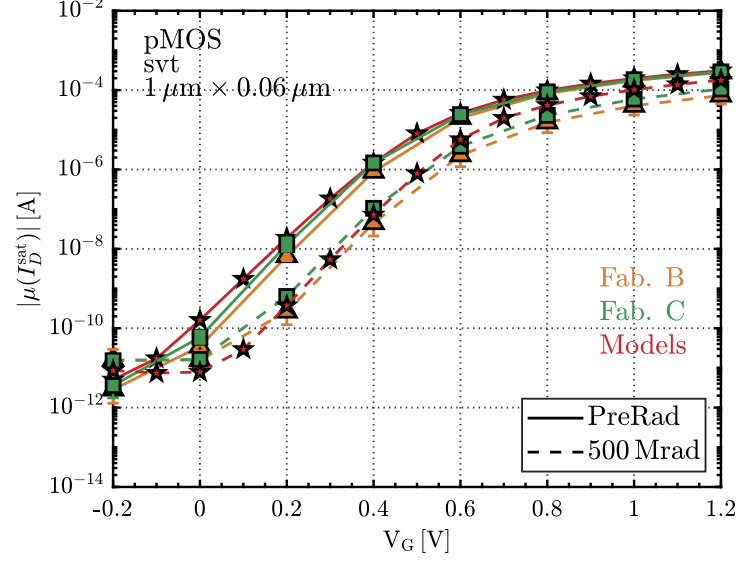


Figure 5.6: Comparison of the mean  $I_D - V_G$  over all the available runs and simulation of  $1\mu\text{m} \times 0.06\mu\text{m}$  (a) and  $0.12\mu\text{m} \times 0.06\mu\text{m}$  (b) pMOS transistors.



## 5.4 Circuit-Level examples

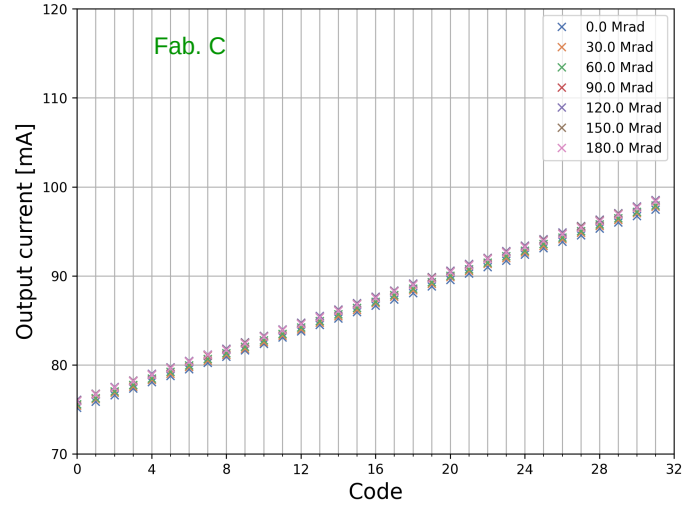
This section reports two examples of TID-induced degradation variability on small circuit blocks in 65 nm to evidence how the variability discussed thus far on transistors can impact real ASICs. Fig.5.7 concerns the behavior with TID of a 5-bits Digital to Analog Converter (DAC) embedded in the Silicon Strip ASIC (SSA) for the Pixel Strip (PS) module of the Compact Muon Solenoid (CMS) experiment Outer Tracker detector upgrade [129].

The DAC from Fab.C exhibits stable output current for each of the input codes even at 180 Mrad( $\text{SiO}_2$ ). In Fab.B, instead, there is an increase in the output current for increasing levels of TID. However the available data is insufficient to conclude whether these differences are due to a lot-to-lot or fab-to-fab variability.

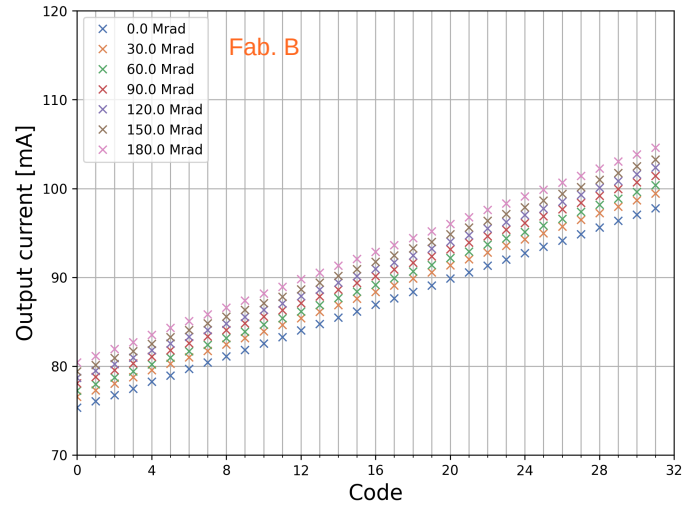
Fig.5.8, shows the TID-induced degradation in the oscillation frequency of ROs consisting of a chain of 25 inverters and representative of the change in speed of standard cells in the 65 nanom technology. The TID-induced degradation of the oscillation frequency is more severe in the ROs of Fab.C. At 180 megarad( $\text{SiO}_2$ ), the ROs of Fab.C show almost twice as much degradation as those of Fab.B. Once more, only a single run was available per fab, thus precluding any determination of whether the observed discrepancies are attributable to variations between fabs or between runs.

## 5.5 Conclusions on Variability

It was demonstrated that the TID-induced degradation in both the 130 nm and 65 nm technologies used for the HL-LHC ASICs is affected by fab-to-fab and run-to-run variability, the impact of which depends on transistors type and size. This variability must be taken into account when using the SPICE-level radiation models developed at CERN. It was presented evidence of variability in the radiation response of both individual transistors and circuit blocks, eloquently demonstrating that this variability can and most likely will affect more complex ASICs and that it should be accounted for in the design as well as qualification phases of the developments.

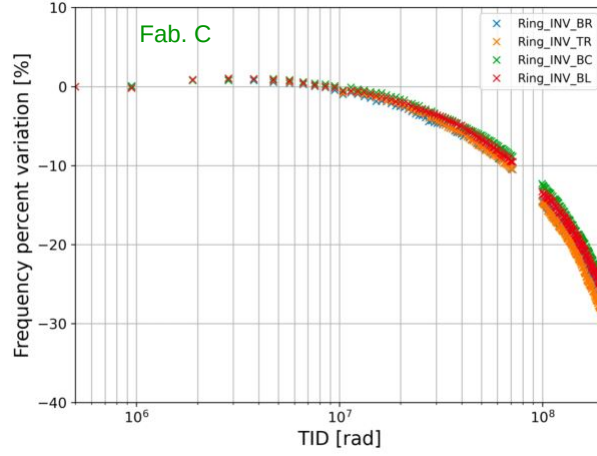


(a)

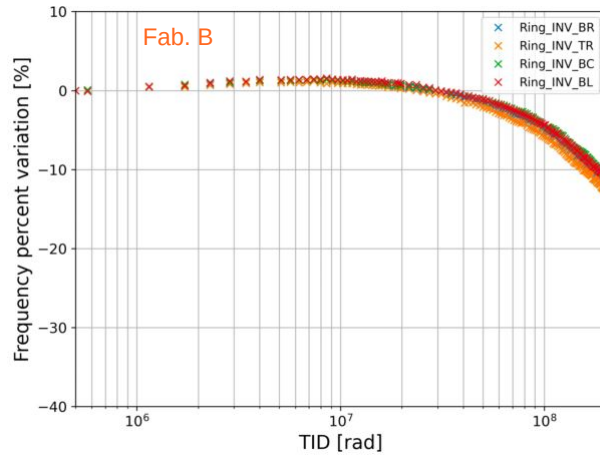


(b)

Figure 5.7: Output current of a 5-bits DAC from two prototype runs exposed to TID up to 180 Mrad( $\text{SiO}_2$ ). Only DACs from one run showed a stable output current with TID.



(a)



(b)

Figure 5.8: Difference in the degradation of the oscillation frequency as a function of TID of the inverter ring oscillators (bottom-right, top right, bottom-center, bottom-left) from two prototype runs. Ring oscillators from one run showed less TID-induced degradation.

## Chapter 6

# Neutron- and Proton- Induced Degradation in 28nm CMOS Technology

The 28 nm CMOS technology has been chosen as the next node for the upgrade of detector's electronics beyond the HL-LHC upgrade [130]. The response to ultra-high levels of TID of this technology has been thoroughly characterized in recent years [82, 131, 11, 93, 132, 89, 133]. As for other CMOS technologies, TID-induced degradation in this node is mainly caused by charge buildup in STI oxides and at their interface with the channel. The main phenomena observed were increased leakage current in n-type devices along with parametric shifts in both n- and p-type transistors with narrower devices more affected by TID (RINCE) [82, 131, 11, 93, 132, 89, 133]. One of the key advantages of 28 nm technology with respect to older nodes is the absence of RISCE [72, 95]. The reduced degradation in short-channel devices provides clear advantages for digital applications, where minimum or near-minimum channel length transistors are typically used. The mechanism of such effects were described in Chapter 4.

The response to Displacement Damage (DD) of 28 nm is instead unknown. DD effects are a well-known problem in bipolar transistors, where radiation-induced recombination centers reduce the recombination lifetime of minority carriers, consequently causing gain degradation [134, 135, 136, 137]. Because the electrical properties of MOS transistors are not significantly affected by the lifetime of minority carriers, they are generally very robust against displacement damage and thus have been less studied in the literature [22]. However, the introduction of new materials, increasing levels of silicon doping, and the use of new manufacturing techniques in more advanced CMOS technologies require evaluation of their response to high fluences. Moreover, with technology scaling, new materials and channel/diffusion engineering techniques have become necessary such as introduction of Lightly Doped Drain (LDD) and halo implants to handle short channel effects. Nowadays, transistor length is shrinking to the point where the active channel region is comparable to the size of displacement damage clusters [135, 138].

Effects attributable to displacement damage have been observed in CMOS technologies at 180 nm [139] or even in the more advanced FinFETs [140]. ASICs

for the HL-LHC upgrade are required to withstand  $10^{16}$  neq/cm<sup>2</sup> fluences in 10 years and upcoming upgrade of the HL-LHC may require even greater radiation hardness [141]. Considering that these fluences are several orders of magnitude higher than in typical tests or application [142, 143, 144, 145], it is necessary to assess whether there is evidence of displacement damage in 28 nm CMOS technology and if observed, the severity of it. Eventually, to identify whether the cause of the observed degradation is TID or DD, an X-ray campaign was performed. X-rays only cause TID, so they are a valuable tool for comparison.

In this chapter, the results of the investigation of DD effects through proton and neutron irradiation in 28 nm technology will be discussed. The discussion will be based on the results published in:

[146] Termo, G., Borghello, G., Faccio, F., Michelis, S., Koukab, A., Sallese, J. M. (2024). "Radiation response of 28 nm CMOS transistors at high proton and neutron fluences for high energy physics applications". Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment, 169497.

Available at: <https://www.sciencedirect.com/science/article/pii/S0168900224004236>

## 6.1 Irradiation Details

Radiation source, temperature and bias all play a role in the radiation response of MOS transistors. Therefore, this section will describe some details of the irradiation facilities used as well as the devices conditions during exposure. In all irradiation, the samples were unpackaged, i.e. bare silicon, custom structure (described in Chapter 3) containing several isolated n- and p-channel transistors. The test structures were designed in the EP-ESE-ME section at CERN and fabricated in commercial-grade bulk 28 nm CMOS technology from two different manufacturers that, for non-disclosure reasons, we will name hereafter M1 and M2. Fig.6.1 shows the widths (W) and lengths (L) of the implemented transistors for core and I/O devices for both manufacturers. The measurement of one chip takes about 6 hours and a total of 20 chips and almost 2000 transistors were measured before and after irradiation. All irradiation reported in this Chapter were performed with devices in floating configuration, i.e., with no bias applied to any of the terminals. This choice was forced by the difficulties in providing a continuous bias to the devices during proton and neutron irradiation in the facilities used. However, the lack of biasing during proton and neutron irradiation is not a concern since displacement damage is known to be insensitive to the bias applied during exposure [147]. Although TID damage is strongly dependent on the bias applied during irradiation and generally shows greater degradation when bias is applied [148, 82, 11], to provide a valid comparison with proton and neutron results, X-ray irradiation were performed under the same bias and temperature conditions. Since the goal is to compare the results between TID and DD tests rather than to induce the greatest degradation, the floating bias is a valid choice.

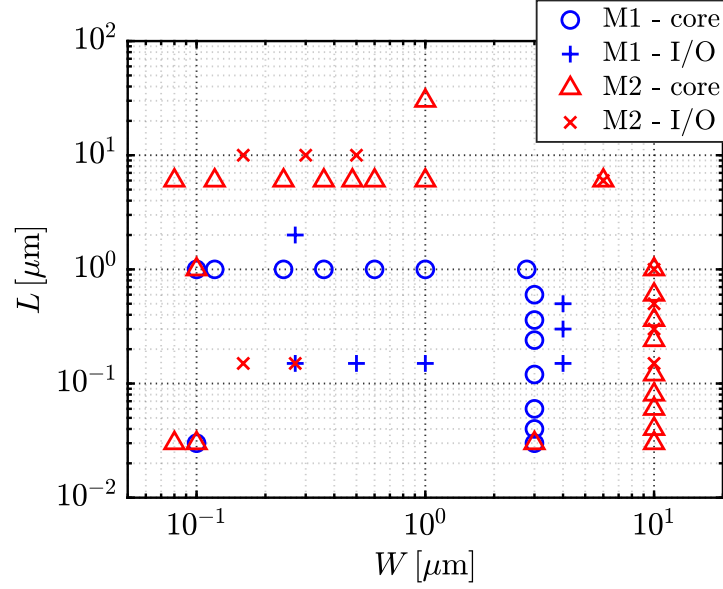


Figure 6.1: Size of the studied transistors. For each dimension, both nMOS and pMOS devices were included. Some devices (e.g. minimum size devices) were duplicated many times. For some dimensions of core devices, also high-vth and low-vth transistors were implemented.

### 6.1.1 Proton Irradiation

Proton irradiation was performed at the MC40 cyclotron facility in Birmingham, England [149]. Proton energy at MC40 is 27 MeV, with a flux of about  $6 \times 10^{11} \text{ p cm}^{-2} \text{ s}^{-1}$  [150] which are representative of the detectors environments. At this energy, protons have a penetration range of about 4.1 mm and 4 mm in Si and  $\text{SiO}_2$  respectively. 3 chips from M1 and 2 chips from M2 were exposed to a fluence of  $1 \times 10^{16} \text{ 1 MeV neq/cm}^2$ , which corresponds to a TID  $\sim 1.3 \text{ Grad}(\text{SiO}_2)$ . During irradiation, the samples were kept at  $T = -30^\circ\text{C}$  and with all terminal floating. Exposure to such large particle fluence induces relevant radioactivity, preventing measurements to be performed for a long period of time. The chips were thus measured at CERN  $\sim 2$  months after the irradiation, during which period they were constantly kept at  $T = -30^\circ\text{C}$ , including during the transport back from Birmingham. The samples were brought to room temperature only for the measurements.

### 6.1.2 Neutron Irradiation

Neutron irradiation was carried out at the TRIGA Mark II research reactor in Ljubljana, Slovenia [151]. The chips have been exposed with all terminals floating to 1, 2 and  $3 \times 10^{16} \text{ n/cm}^2$ . For each fluence, 3 chips from M1 and 2 chips from M2 were irradiated. Neutron spectrum at TRIGA presents two energy peaks at about 0.05 eV and 2 MeV [152, 153]. Neutrons deposit roughly 10 Mrad( $\text{SiO}_2$ ) every  $1 \times 10^{16} \text{ n/cm}^2$ , meaning that the samples received a TID of  $\sim 10 - 30 \text{ Mrad}(\text{SiO}_2)$  due to mostly secondary gamma in TRIGA reactor. TID calculations were pro-

vided by the facility, where they were estimated with a RADFET device [154]. Note that the temperature of the sample during the irradiation depends on the flux of neutrons. The chips exposed to  $1$  and  $2 \times 10^{16}$  n/cm<sup>2</sup> were irradiated with  $1.62 \times 10^{12}$  neq cm<sup>-2</sup>s<sup>-1</sup> flux and reached a temperature of 40 °C. A higher flux channel with  $6.25 \times 10^{12}$  neq cm<sup>-2</sup>s<sup>-1</sup> was used to reach  $3 \times 10^{16}$  n/cm<sup>2</sup>, and the samples were then heated to  $\sim 90$  °C [152, 153]. The measurement, performed at room temperature, started  $\sim 3$  months after the irradiation during which time they were stored at  $T = -30$  °C.

### 6.1.3 X-ray

X-ray irradiation were carried out at CERN at CERN using the irradiation setup described in Chapter 3. The devices were irradiated up to 1.3 Grad(SiO<sub>2</sub>) with a dose-rate of 6 Mrad(SiO<sub>2</sub>)/h, with all terminals floating, at  $T = -30$  °C, 25 °C, 90 °C. At the end of irradiation, the devices were measured at room temperature.

## 6.2 Results of Proton Investigation

The blue lines in Fig.6.2 show the mean  $I_D - V_G$  measured in saturation region for 6 minimum size  $100 \text{ nm} \times 30 \text{ nm}$  pMOS devices from M1 irradiated with protons. Protons induce a threshold voltage shift of  $\Delta|V_{TH}^{\text{sat}}| = 45.7 \text{ mV} \pm 12.7 \text{ mV}$  and a decrease in the transconductance ( $g_m$ ) of  $8.01\% \pm 2.5\%$ . To verify if the degradation is caused by DD or by TID, an irradiation with X-ray to TID = 1.3 Grad(SiO<sub>2</sub>) was performed on chips floating and kept at  $T = -30$  °C, the same dose deposited during  $1 \times 10^{16}$  1 MeV neq/cm<sup>2</sup> proton irradiation. The black lines show the results of the test. X-ray induce threshold voltage shift of  $\Delta|V_{TH}^{\text{sat}}| = 66.1 \text{ mV} \pm 13.3 \text{ mV}$  and a decrease in the transconductance ( $g_m$ ) of  $5.20\% \pm 4.67\%$ . Pre- and post-irradiation  $I_D - V_G$  curves are very similar for both TID- and proton-irradiated transistors, suggesting that the degradation is caused by ionizing effects rather than DD.

Another strong indication that the degradation observed in transistors exposed to protons is caused by TID comes from the size dependence of the radiation response. Fig.6.3 reports the percentage variation of the drain current in pMOS transistors measured at maximum  $V_{GS}$  and  $V_{DS}$  ( $I_{ON}^{\text{sat}}$ ) as a function of  $1/W$ . The degradation caused by  $1 \times 10^{16}$  neq/cm<sup>2</sup> at  $T = -30$  °C is indicated by light-blue markers. The degradation is clearly dependent on the channel width, with narrow devices being more affected by protons in both technology processes.

The same behavior is often observed in devices exposed to TID, known as radiation-induced narrow channel effects (RINCE) [72]. This is evident when comparing the results of proton and X-ray exposure at TID = 1.26 Grad(SiO<sub>2</sub>) (black markers) in Fig.,6.3. The difference in degradation between the two sources in narrower devices is likely due to the difference in temperature during exposure: X-rays at  $T = 25$  °C and protons at  $T = -30$  °C. Zhang previously observed milder degradation during cold exposure for the same technology node [155]. Despite differences in the absolute value of degradation, the dependence on  $W$  is

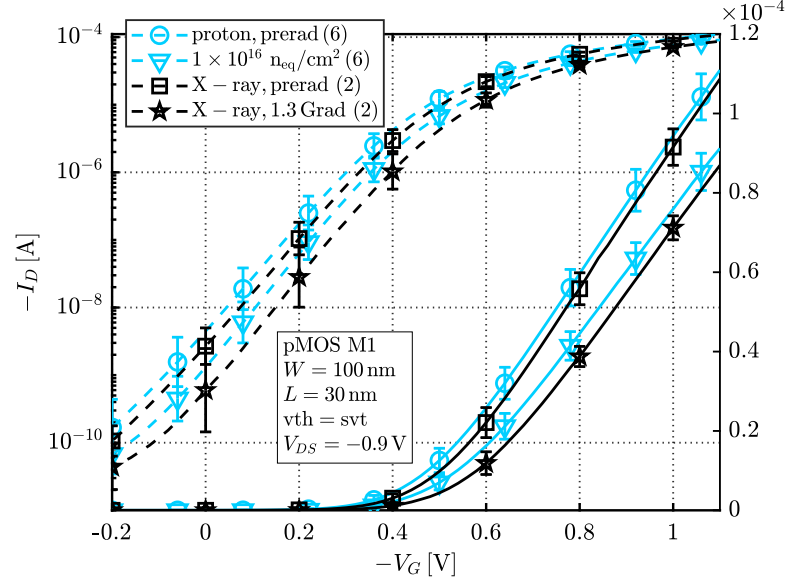


Figure 6.2: Comparison of the mean  $I_D - V_G$  curves in linear (solid lines) and logarithmic (dotted lines) scale of minimum-size pMOS transistors irradiated with protons (light blue triangles) and X-ray (black stars). Numbers in parentheses indicate the amount of devices measured. The degradation caused by the two irradiation runs is very similar.

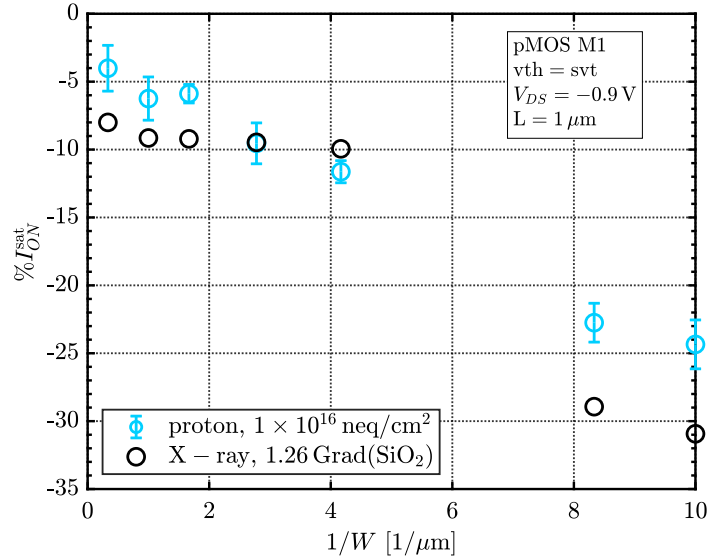


Figure 6.3: Mean  $\%I_{ON}^{sat}$  deviation induced by proton irradiation (blue) in pMOS core transistor from M1 (circles) with  $L = 1 \mu\text{m}$  and  $W = 0.1 \mu\text{m} - 3 \mu\text{m}$ . Note that the x-axis shows the reciprocal of the transistor width ( $1/W$ ). X-ray irradiation (black lines) of a chip from M1 to 1.26 Grad(SiO<sub>2</sub>) at  $T = 25^\circ\text{C}$  is added for comparison.



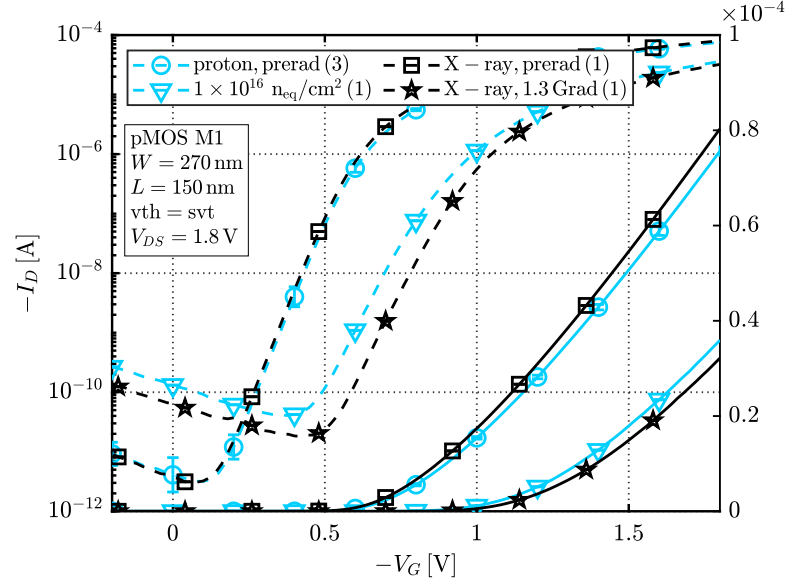


Figure 6.4: Comparison of the mean  $I_D - V_G$  curves of minimum-size pMOS I/O transistors from M1 irradiated with protons (light blue) and TID (black). There is a good agreement in the degradation caused by the two irradiation.

clearly the same. Since the degradation mechanisms due to DD have a completely different origin from those due to TID, they are unlikely to show the same dependence on transistor size. DD degradation mechanisms arise from defects in the Si substrate where the channel is formed, which should be independent of transistor size. In contrast, TID degradation results from charge accumulation in the oxides near the channel region, meaning device size influences the portion of the channel affected by this charge. Devices from M2 (not shown) exhibit a similar trend, with greater degradation observed in short channel devices.

The same correlation between proton- and X-ray-irradiation was observed also in I/O devices as reported in Fig. 6.4 for 270 nm  $\times$  150 nm pMOS I/O from M1. During X-ray irradiation to 1.3 Grad(SiO<sub>2</sub>) the devices were kept floating at  $T = -30^\circ\text{C}$ .

In both proton and X-ray irradiation, an increase in leakage current of about an order of magnitude is observed. The same increase was already observed in previous work on pMOS transistors in 28 nm technology irradiated at high doses [93]. Bonaldo and coworkers explained this increase as a result of the buildup of interface traps at the channel/oxide interface and/or at the drain/body interface [156]. The high density of interface traps generated at the intersection of the depletion region and STI sidewalls may actually increase the leakage current of the drain to substrate junction [157, 156, 158].

A clear agreement between proton-irradiated and X-ray-exposed devices has also been measured in transistors of different size and threshold voltage. Fig. 6.5 reports the results of nMOS transistors 100 nm  $\times$  30 nm from M1 exposed to  $1 \times 10^{16}$  neq/cm<sup>2</sup> and the last measurement at  $T = 25^\circ\text{C}$  of fresh chips irradiated with X-ray to 1.3 Grad(SiO<sub>2</sub>). During irradiation the devices were kept floating

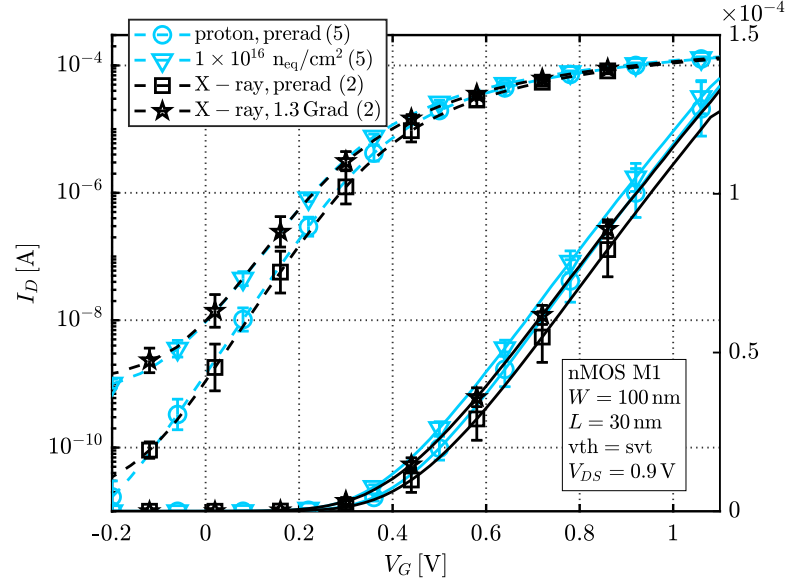


Figure 6.5: Mean  $I_D - V_G$  in saturation region measured at  $T = 25^\circ\text{C}$  of 100 nm  $\times$  30 nm nMOS exposed to protons and X-ray. During X-ray irradiation the devices were at  $T = -30^\circ\text{C}$  with all terminals floating.

at  $T = -30^\circ\text{C}$ , conditions used during proton exposure.

The near-complete overlap between the proton- and X-ray-irradiation results suggests that, even for n-type transistors, the primary cause of degradation is the TID deposited during proton or X-ray exposure. This is strongly supported by the increase in  $I_{OFF}^{\text{sat}} = I_D(V_G = 0 \text{ V}, V_D = 0.9 \text{ V})$  observed in the  $V_G < 0 \text{ V}$  region, a characteristic effect of TID in nMOS transistors caused by the formation of source-to-drain parasitic channels [76, 87].

Comparing the results of nMOS and pMOS transistors reveals that pMOS devices exhibit more severe degradation. This common phenomenon in transistors exposed to high doses of ionizing radiation is explained by the fact that in pMOS transistors, both the charge trapped in the oxides and at the interface are positive, leading to a compounding effect. In contrast, in nMOS transistors, the positive charge in the oxides and the negative charge at the interface partially compensate each other [22, 131, 93].

Figure 6.6 depicts the evolution of the on-current  $I_{ON}$ , normalized to its pre-irradiation value, for two 100 nm  $\times$  30 nm pMOS devices. These devices were irradiated with X-rays to a dose of 1.3 Grad(SiO<sub>2</sub>) at  $T = -30^\circ\text{C}$  and exposed to a fluence of  $1 \times 10^{16}$  neq/cm<sup>2</sup>, followed by annealing for approximately 2 days at  $T = 60^\circ\text{C}$  and roughly 1 day at  $T = 100^\circ\text{C}$ . During both irradiation and annealing, the devices remained floating. After irradiation, both protons and X-rays cause similar levels of degradation, which is not mitigated even after annealing at  $T = 100^\circ\text{C}$ . The comparable behavior of the two curves implies that the defect responsible for the degradation is of the same nature.

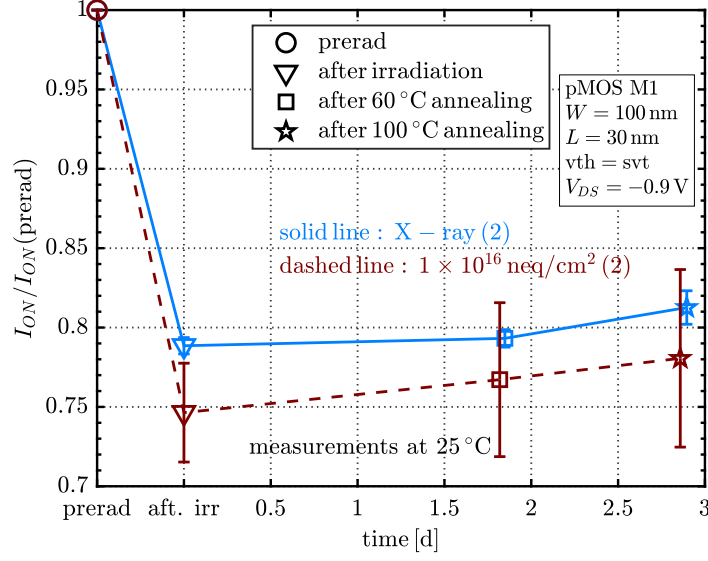


Figure 6.6: Annealing at different temperature of the on-current of two 100 nm  $\times$  30 nm pMOS core transistors after exposure to 1.3 Grad(SiO<sub>2</sub>) (blue) at  $T = -30^\circ\text{C}$  and  $1 \times 10^{16}$  neq/cm<sup>2</sup> proton (red). The  $I_{ON}$  was normalized to its value before irradiation. The data reported were measured at  $T = 25^\circ\text{C}$  after each step of annealing at a given temperature.

### 6.3 Results of Neutron Investigation

Thicker oxides, lower doping, and higher operating voltages (resulting in a higher electric field in the oxides) increase the susceptibility of I/O transistors to charge accumulation, making these devices significantly less robust against TID degradation [10]. Fig.6.7 compares the degradation of core and I/O devices from M1 exposed to a neutron fluence of  $3 \times 10^{16}$ , n/cm<sup>2</sup>. The top plot shows the increase in leakage current of nMOS transistors measured in the saturation region ( $I_{OFF}^{\text{sat}}$ ). Due to the leakage increasing by several orders of magnitude, the variation of the  $\log_{10}$  of  $I_{OFF}^{\text{sat}}$  has been reported. The bottom plot shows the degradation of  $\%I_{ON}^{\text{sat}}$  for pMOS devices. When comparing devices with similar channel widths, I/O transistors exhibit more severe degradation than core devices. This is even more pronounced in p-type transistors, where the degradation can be as much as double in I/O devices compared to their core counterparts. Since the degradation of core devices is relatively low at these fluences, this section will focus on the results for I/O transistors, though similar conclusions can be drawn for core transistors.

Fig. 6.8 displays the average  $I_D - V_G$  characteristics of 270 nm  $\times$  150 nm pMOS I/O transistors that were exposed to  $1 - 3 \times 10^{16}$ , n/cm<sup>2</sup>. This includes the final measurement taken at  $T = 25^\circ\text{C}$  following X-ray irradiation at 30 Mrad(SiO<sub>2</sub>). During the X-ray irradiation, the devices were kept floating at  $T = 90^\circ\text{C}$ , which is the highest temperature reached during neutron irradiation.

Neutron exposure within the range of  $2 - 3 \times 10^{16}$ , n/cm<sup>2</sup> leads to a degradation closely resembling that observed following 30 Mrad(SiO<sub>2</sub>) X-ray exposure.

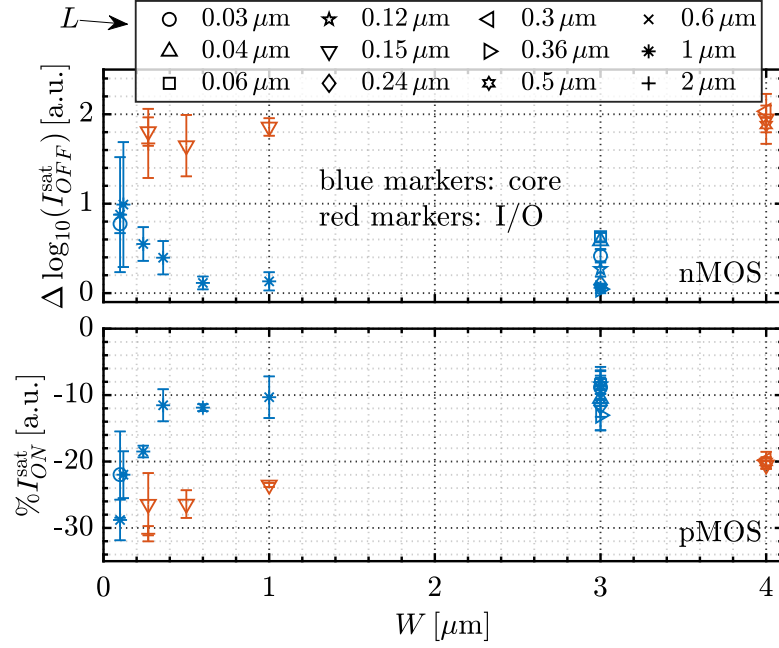


Figure 6.7: Comparison of core (blue) and I/O (red) devices from M1 as a function of the channel width. Top: increase in orders of magnitude of the leakage current of nMOS transistors measured in saturation region ( $I_{OFF}^{sat}$ ). Bottom:  $\%I_{ON}^{sat}$  degradation of pMOS devices. Different markers identify different  $L$ s, as reported in the legend. For the same channel width, I/O transistors exhibit more severe degradation.

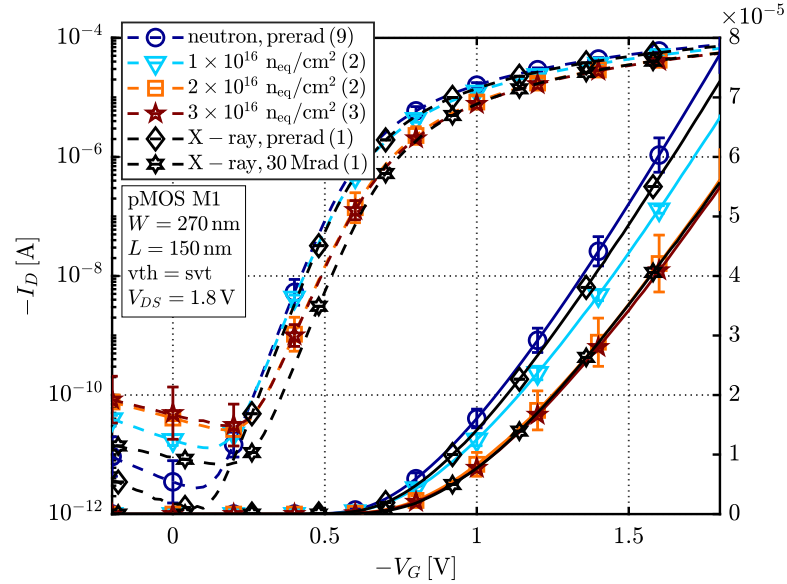


Figure 6.8: Mean  $I_D - V_G$  in linear (solid lines) and logarithmic (dashed lines) scale of 270 nm  $\times$  150 nm pMOS I/O transistors exposed to neutrons and X-ray. Numbers in parentheses indicate how many devices were measured. The degradation observed in neutron-irradiated devices is in agreement with the amount of TID deposited during exposure.

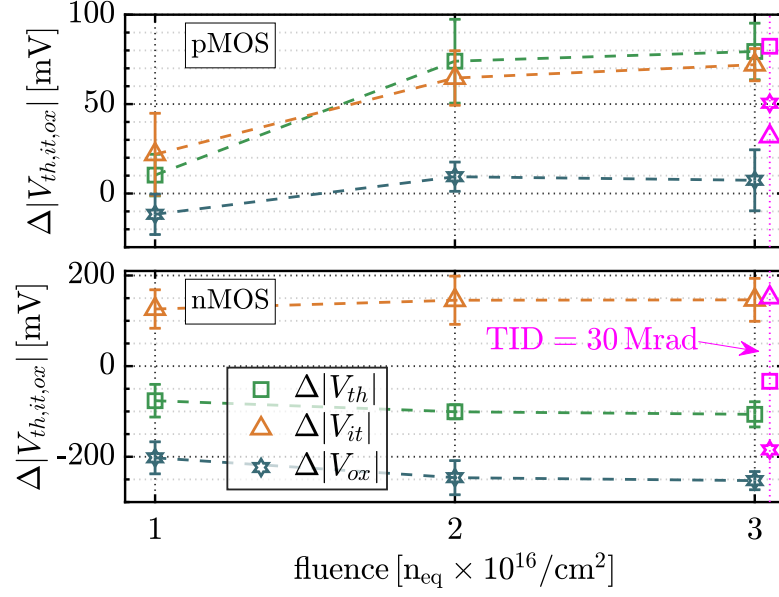


Figure 6.9: Contribution of oxide- and interface-trapped charge to the total  $\Delta V_{th}$  for 270 nm  $\times$  150 nm pMOS (top) and nMOS (bottom) I/O devices from M1. The green, orange and blue dashed lines report the results of neutron irradiation while the purple markers show the effect of X-ray exposure.

The discrepancy in post-radiation leakage current between neutron and X-ray irradiation is attributed to the formation of bulk defects within the depletion region of the drain-substrate junction subsequent to neutron irradiation [159, 160, 161, 162]. A similar mechanism may also be at play in proton-irradiated devices. Nonetheless, due to the substantial dose received, this current is primarily influenced by the leakage current resulting from total ionizing dose (TID)-induced traps at the STI/drain interface. Another distinction lies in the modest reduction observed in the curve slopes at  $2 - 3 \times 10^{16}$ ,  $n/cm^2$  compared to X-ray irradiation.

For pMOS devices, the total shift in threshold voltage ( $V_{th}$ ) at the highest fluence closely mirrors that observed after an exposure of 30 Mrad( $SiO_2$ ). However, the proportionate impact of charge trapping at the interface and within the oxide layer differs. In devices subjected to neutron exposure, the  $V_{th}$  shift is primarily influenced by charge trapping at the interface. The minor negative shift in  $V_{ox}$  at the lowest fluence appears to be an anomaly. Conversely, pMOS devices exposed to X-rays exhibit a comparable contribution from both oxide- and interface-trapped charge. This pattern was consistent across all sizes of pMOS I/O devices.

Additional inquiries are necessary to confirm whether this variation suggests a distinct neutron-induced impairment not replicable with X-rays. It's worth highlighting that this phenomenon was solely noted in the pMOS I/O transistors subjected to neutron exposure. Specifically, core pMOS transistors irradiated with neutrons, along with all nMOS irradiated with neutrons and devices exposed to protons, did not exhibit this characteristic.

Fig. 6.10 illustrates the  $I_D - V_G$  characteristics of nMOS I/O transistors irradiated with neutron and X-ray. The overall shift in  $V_{th}$  is nearly negligible for

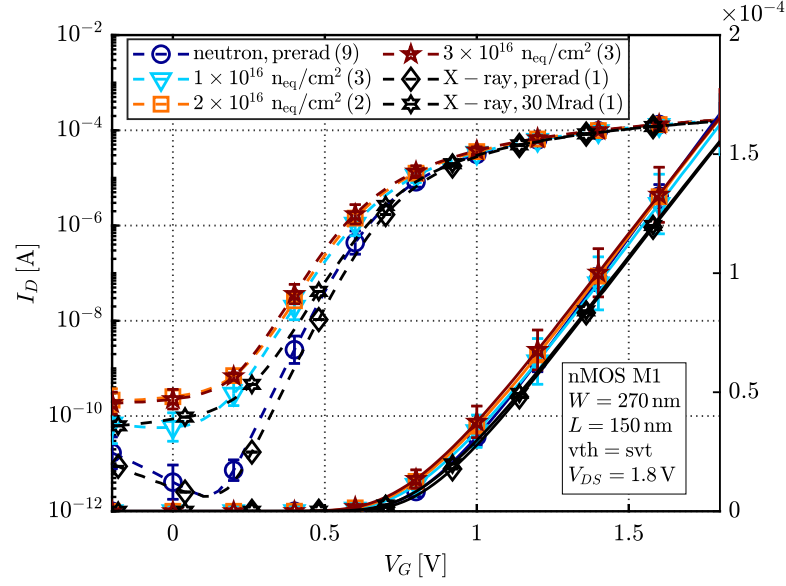


Figure 6.10: Mean  $I_D - V_G$  in linear (solid lines) and logarithmic (dashed lines) scale of 270 nm  $\times$  150 nm nMOS I/O transistors exposed to neutrons and X-ray.

the X-ray-exposed device, whereas there is a more noticeable negative shift in  $V_{th}$  for the samples irradiated with neutrons. This dissimilarity primarily stems from a lower accumulation of charge trapped in the oxide compared to the accumulation of charge trapped at the interface during neutron irradiation (see Fig. 6.9). Despite this distinction, the measurements exhibit reasonable concurrence, even considering the limited statistical data on X-ray-irradiated devices.

The most notable effect of TID on nMOS transistors is the rise in leakage current, denoted as  $I_{OFF}^{sat} = I_D(V_G = 0 \text{ V}, V_D = 1.8 \text{ V})$ . This increase becomes apparent in the region where  $V_G < 0.1 \text{ V}$ , as depicted in Fig. 6.10. Notably, the increase in  $I_{OFF}^{sat}$  in devices irradiated with neutrons and X-rays is nearly identical.

Similar to the correlation observed with proton irradiation, the consistency between devices exposed to neutrons and X-rays was also noted across various sizes, threshold voltages ( $V_{th}$ ), and manufacturers. This observation supports the notion that the degradation is predominantly induced by TID.

Further insights into the nature of defects caused by radiation can be gained by performing annealing at different temperatures. Fig. 6.11 illustrates the change in off-current  $I_{OFF}$  normalized to its post-irradiation level for a 270 nm  $\times$  150 nm nMOS I/O transistor, which was exposed to 30 Mrad( $\text{SiO}_2$ ) radiation (solid line) at  $T = 90^\circ\text{C}$  and  $3 \times 10^{16} \text{ neq/cm}^2$  (dashed line). Each data point represents a measurement taken at room temperature after several days of annealing at the temperatures specified in the legend. The transistor remained floating during both irradiation and annealing processes. For each annealing step at a fixed temperature of comparable duration, the behavior of  $I_{OFF}$  appears consistent across both transistors. Specifically, both exhibit a slight increase in  $I_{OFF}$  after approximately 4 days at  $40^\circ\text{C}$ , followed by a decrease at  $60^\circ\text{C}$  and a more rapid reduction at  $100^\circ\text{C}$ . Given the improbability of different radiation-induced defects exhibiting

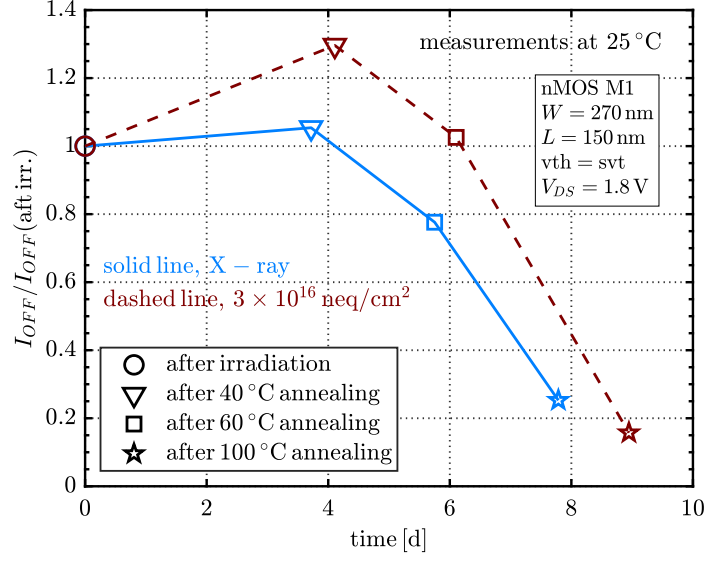


Figure 6.11: Annealing at different temperature of the off-current of one  $270 \text{ nm} \times 150 \text{ nm}$  nMOS I/O after exposure to 30 Mrad( $\text{SiO}_2$ ) (blue) and  $3 \times 10^{16} \text{ neq/cm}^2$  (red). The  $I_{OFF}$  was normalized to its value after irradiation. The data reported were measured at  $T = 25^\circ\text{C}$  after each step of annealing at a given temperature.

identical temperature-dependent trends, these findings strongly suggest a common underlying nature of the defects.

## 6.4 Conclusions on DD in 28nm CMOS Technology

A comprehensive irradiation campaign was carried out on ASICs in 28 nm CMOS technology, exposing them to extremely high levels of proton and neutron fluences. The radiation response of this technology is primarily affected by TID-induced degradation. Potential signs of displacement damage were detected in the leakage current of neutron-irradiated pMOS transistors and the subthreshold slope of neutron-irradiated pMOS I/O transistors. These findings confirm the overall resilience of CMOS technologies to displacement damage and are crucial in proving that 28 nm CMOS technology can endure the harsh environments of CERN particle detectors.

# Chapter 7

## Low Dose-Rate Sensitivity of 28nm CMOS technology

### 7.1 Introduction

This chapter investigates the Enhanced Low-Dose-Rate Sensitivity (ELDRS) of a 28 nm commercial CMOS technology exposed to ultra-high doses. The 28 nm node has been selected as the CMOS technology for the development of the next generation of Application-Specific Integrated Circuits (ASICs) for particle detectors in the High Luminosity Large Hadron Collider (HL-LHC) at CERN, where total-ionizing-dose (TID) levels of several hundred Mrad( $\text{SiO}_2$ ) are expected in the inner layers of particle detectors over a 10-year operational period [1]. This process exhibits excellent radiation hardness compared to older nodes, even at ultra-high doses [148, 82, 11, 93, 132]. However, studies investigating the TID response of this process have only been conducted at very high dose-rates (HDRs).

Although ELDRS is a significant concern for the radiation hardness assurance of linear bipolar transistors [108], MOSFETs are generally considered to be immune to true Dose-Rate (DR) effects and only be sensitive to Time-Dependent Effects (TDEs) [163]. However, Witczak and co-workers demonstrated the presence of ELDRS in MOS transistors in 350nm, 250nm, and 180nm CMOS nodes [12]. The source-to-drain leakage current caused by TID-induced charge trapped in the Shallow Trench Isolation (STI) oxides in nMOSFETs was found to increase more in devices irradiated at Low-Dose Rate (LDR) [12, 164, 165]. More recently, radiation effects related to the presence of spacer oxides have been found to be sensitive to true DR effects in 130 nm and 65 nm CMOS technologies [166, 15]. These results indicate that the ELDRS must also be evaluated in CMOS technologies.

SRAMs and ROs designed in 28 nm CMOS technology have been exposed to a TID of 200 Mrad( $\text{SiO}_2$ ) at either a High-Dose-Rate typical of qualification procedures ( $\text{HDR} \simeq 5.91 \text{ Mrad/h} = 1.64 \text{ krad/s}$ ) or at a considerably Lower-Dose-Rate ( $\text{LDR} \simeq 0.10 \text{ Mrad/h} = 27.8 \text{ rad/s}$ ) to observe possible ELDRS of this technology. Both SRAMs and ROs exhibit higher power consumption when irradiated at LDR, indicating that HDR qualification procedures may underestimate the actual degradation of ASICs in the 28 nm technology. Measurements on isolated



transistors irradiated at different temperatures and biases indicate that the parameter responsible for this ELDRS is the source-to-drain leakage current caused by charge trapped in the STI oxide. Other TID-induced effects, such as threshold voltage shift and ON-current degradation, may be sensitive to DR depending on the applied bias.

The results discussed in this Chapter have been presented in the "Basic Mechanisms of Radiation Effects" at the IEEE RADiation Effects on Components and Systems (RADECS) 2024 conference and will be published in IEEE Transaction on Nuclear Science:

Borghello G., **Termo G.**, Faccio F., Ceresa D., Pejasinovic R., Bergamin G., Piernas Diaz F., Kloukinas K. "ELDRS in a commercial 28nm CMOS technology" <https://radecs2024.org/program/technical-sessions/>

## 7.2 Experimental Details

The CMOS process studied is a commercial 28 nm technology with a nominal supply voltage of 0.9 V. Two custom test structures, hereafter identified as EXP28:TID and TESTCHIP28, were designed and manufactured for this study:

### 7.2.1 EXP28:TID

This test chip contains 4 foundry SRAMs and 368 ring-oscillators (ROs). A more detailed description of the chip can be found in [132]. The measurement of all the structures integrated in the chip takes approximately 15 minutes.

#### SRAMs

Foundry SRAMs are compact and efficient SRAMs designed by the technology manufacturer. EXP28:TID contains 4 SRAMs, called Single Port (SP), Single Port Ultra-High Density (SPUHD), Dual Port (DP), and Dual Port Ultra-High Density (DPUHD). Table 7.1 summarizes their characteristics. SP, SPUHD, and DPUHD are based on 6-transistors cells (6T), while DP is designed with 8-transistors cells (8T). The table reports the channel width  $W$  and length  $L$  of the pull-up nMOS (nPU) transistors, pull-down pMOS (pPD), and pass-gate nMOS (nPG)).

The functionality of the SRAMs is observed using voltages from 0.5 V to 1.0 V with a step of 10 mV and reading/writing frequencies from 20 MHz to 1.97 GHz with a step of 50 MHz. For each combination of frequency  $f_{\text{SRAM}}$  and voltage  $V_{\text{SRAM}}$ , the functionality of the SRAMs is tested by a Built-in Self-Test (BIST) [167, 168]. The BIST verifies the whole content of the SRAMs, counting the corrupted bits. In the event that even a single bit is identified as corrupted, the corresponding frequency/voltage combination is then excluded from the Operational Area (OA). The final output is an OA defined by voltages and frequencies at which the SRAMs work properly. This can be represented by a Shmoo plot, as reported in Fig. 7.1 for the four SRAMs before irradiation.

Table 7.1: SRAMs number of bits and transistors size.

| SRAM  |      | SIZE [bit]       | $W$ [nm] $\times$ $L$ [nm] |                |                 |
|-------|------|------------------|----------------------------|----------------|-----------------|
| name  | type |                  | nPD                        | pPU            | nPG             |
| SP    | 6T   | $4096 \times 32$ | $95 \times 35$             | $40 \times 35$ | $65 \times 35$  |
| SPUHD | 6T   | $2048 \times 32$ | $95 \times 35$             | $40 \times 35$ | $65 \times 35$  |
| DP    | 8T   | $4096 \times 32$ | $195 \times 35$            | $50 \times 35$ | $140 \times 35$ |
| DPUHD | 6T   | $4096 \times 32$ | $95 \times 35$             | $40 \times 35$ | $65 \times 35$  |

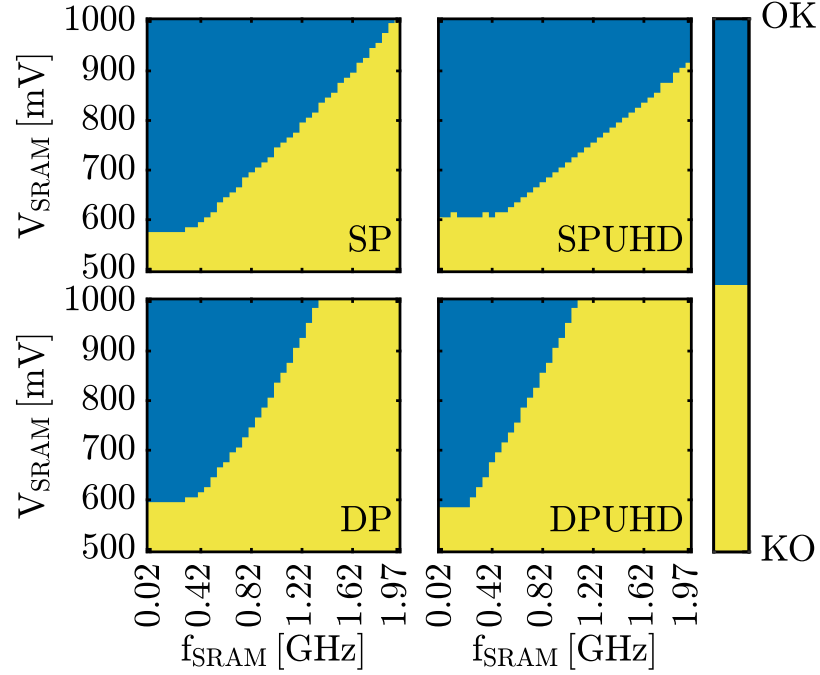


Figure 7.1: BIST output for the 4 SRAMs before irradiation. For sufficiently high frequencies and low voltages the BIST reports an error in every SRAM. At  $V_{\text{SRAM}} = V_{\text{DD}} = 0.9\text{ V}$ , the maximum frequencies inside the operating area are  $f_{\text{MAX}}^{\text{SP}} = 1.62\text{ GHz}$ ,  $f_{\text{MAX}}^{\text{SPUHD}} = 1.87\text{ GHz}$ ,  $f_{\text{MAX}}^{\text{DP}} = 1.12\text{ GHz}$ ,  $f_{\text{MAX}}^{\text{DPUHD}} = 0.87\text{ GHz}$ .

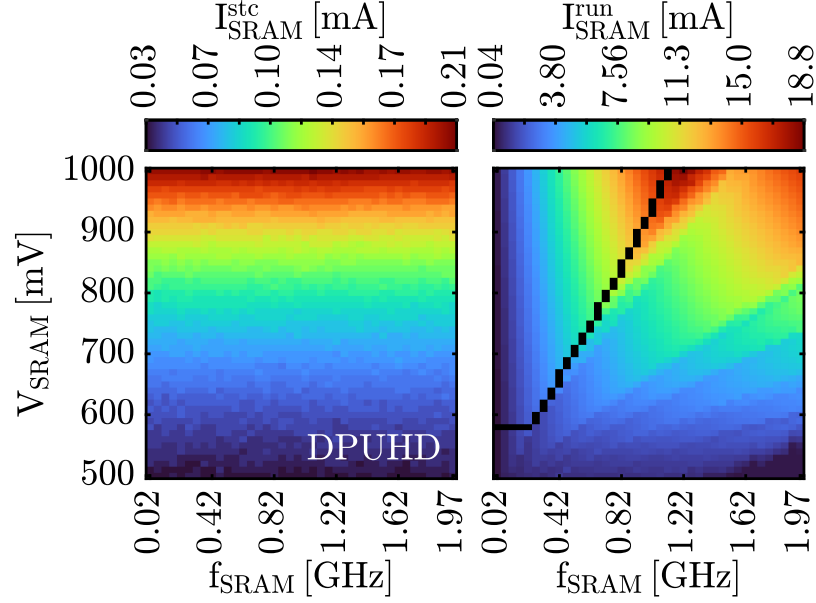


Figure 7.2: Pre-rad static (left) and run (right) current consumption. The black line in the run current plot identifies the limit of the operational area shown in Fig. 7.1.

In addition to functionality, the power consumption of the SRAMs is also measured at various voltages and frequencies, with either the BIST running (run current  $I_{\text{SRAM}}^{\text{run}}$ ) or stopped (static current  $I_{\text{SRAM}}^{\text{stc}}$ ). The SP, SPUHD, and DP SRAMs share the same power terminal, meaning that only their combined power consumption can be measured. For this reason, this work focuses mainly on the DPUHD SRAM. Fig. 7.2 shows the pre-rad measurement for both the static and run current for DPUHD. As expected,  $I_{\text{SRAM}}^{\text{stc}}$  increases with voltage and exhibits minimal dependence on frequency due to the absence of operational activity.  $I_{\text{SRAM}}^{\text{run}}$  increases with voltage and frequency within the Operational Area (OA) identified by the BIST. Outside the specified operational area, the relationship between voltage, frequency, and current becomes more complex. This is due to the fact that BIST automatically stops when a predetermined number of errors per second are detected, whereas  $I_{\text{SRAM}}^{\text{run}}$  is a value averaged over a fixed period of time. This time is equal to the time it takes BIST to complete its normal operation. Therefore, if BIST stops early, a portion of the run current is measured while BIST is not operating. Moreover, for sufficiently high frequencies and low voltages, the time needed to charge/discharge a bit line in reading/writing operations becomes larger than the reading/writing time  $t_{\text{SRAM}} = 1/f_{\text{SRAM}}$ . For this reasons, the rest of this chapter will focus only on the frequencies and voltages in the OA identified by BIST.

The run current  $I_{\text{SRAM}}^{\text{run}}$  is the sum of the static current  $I_{\text{SRAM}}^{\text{stc}}$  and the dynamic current  $I_{\text{SRAM}}^{\text{dyn}}$ . As displayed in Fig 7.3,  $I_{\text{SRAM}}^{\text{run}}$  increases linearly with frequency inside the OA and is dominated by  $I_{\text{SRAM}}^{\text{dyn}}$ . Only at very low frequencies the static power consumption, reported in the plot at  $f_{\text{SRAM}} = 0 \text{ Hz}$ , starts to be relevant and comparable to  $I_{\text{SRAM}}^{\text{dyn}}$ .

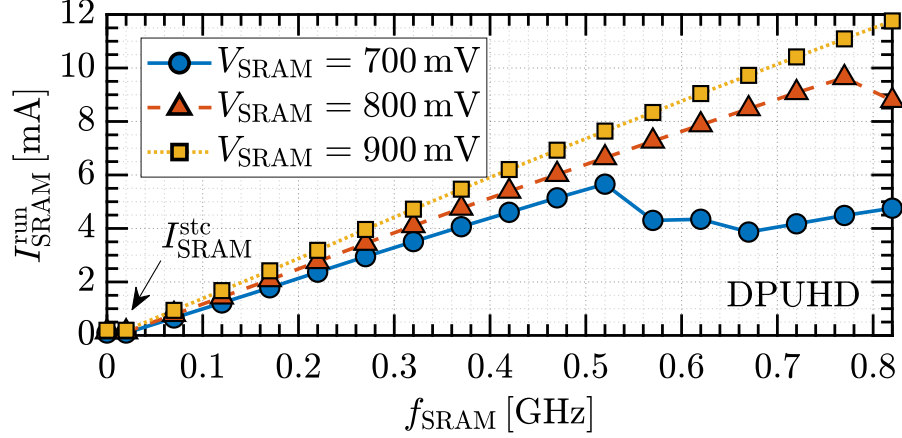


Figure 7.3: Total current in DPUHD SRAM at increasing frequency and three different voltages. The current increases linearly with frequency except at very low  $f$ , where the static current compares with the dynamic one. Outside the OA the linear relationship is lost.

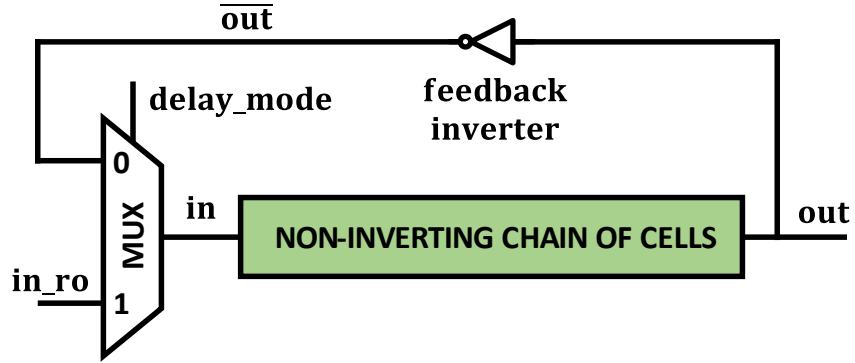


Figure 7.4: Ring oscillator (RO) simplified schematic.  $in\_ro = 0$  for all the tests reported in this chapter.

### Ring-Oscillators

Fig. 7.4 illustrates the basic circuit for the ROs included in the chip. A non-inverting chain of cells is made to oscillate by an inverter placed in the feedback ring. The `delay_mode` signal controls the behavior of the RO. With `delay_mode = 0`, the RO behaves as a regular ring-oscillator. With `delay_mode = 1` the feedback loop is cut off, and the RO stops oscillating. `in_ro` provides additional control over the behavior of the ring oscillator, but for the tests reported in this chapter it was always set to 0.

The technology offers digital libraries with various combinations of threshold voltage flavor VT (ultra-low-VT, low-VT, standard-VT, high-VT, ultra-high-VT, and extra-high-VT), channel length  $L$  (30 nm, 35 nm, and 40 nm), and number of tracks T (7T, 9T, and 12T). The number of tracks is proportional to the physical height of the digital cell. Cells with higher T tend to have transistors with larger channel width. The test chip contains structures using 23 different libraries. For each library, 16 ROs designed with different digital cells (e.g., inverters, NAND,

Table 7.2: Available and used libraries

| <b>7T</b>  | ULVT     | LVT      | SVT      | HVT | UHVT     | EHVT |
|------------|----------|----------|----------|-----|----------|------|
| 30 nm      | <b>O</b> | X        | <b>O</b> | X   | <b>O</b> |      |
| 35 nm      | <b>O</b> | X        | <b>O</b> | X   | X        |      |
| 40 nm      |          | <b>O</b> | <b>O</b> | X   | <b>O</b> | X    |
| <b>9T</b>  | ULVT     | LVT      | SVT      | HVT | UHVT     | EHVT |
| 30 nm      | <b>O</b> | X        | <b>O</b> | X   | <b>O</b> |      |
| 35 nm      | <b>O</b> | X        | <b>O</b> | X   | X        |      |
| 40 nm      |          | <b>O</b> | <b>O</b> | X   | <b>O</b> | X    |
| <b>12T</b> | ULVT     | LVT      | SVT      | HVT | UHVT     | EHVT |
| 30 nm      | <b>O</b> | X        | <b>O</b> | X   |          |      |
| 35 nm      | <b>O</b> | X        | <b>O</b> | X   | X        |      |
| 40 nm      |          | <b>O</b> | <b>O</b> | X   | <b>O</b> | X    |

Table 7.3: ROs cells

| N | name  | N | name  | N  | name   | N  | name    |
|---|-------|---|-------|----|--------|----|---------|
| 1 | INVD0 | 5 | ND2D1 | 9  | NR2D1  | 13 | CKBD0   |
| 2 | INVD1 | 6 | ND4D1 | 10 | NR4D1  | 14 | CKBD1   |
| 3 | ND2D0 | 7 | NR2D0 | 11 | XOR2D0 | 15 | DFCNQD1 |
| 4 | ND4D0 | 8 | NR4D0 | 12 | XOR2D1 | 16 | LHCNQD1 |

NOR, etc.) are included, resulting in a total of 368 ROs [132]. Table 7.2 reports the available and used libraries, where **O** indicates a used library and X indicates an available but unused library. The 16 cells used to design the ROs are indicated in Table 7.3. The digit after the D at the end of the cell name indicates the driving strength of the cell (0 or 1). Cells with higher driving strength have output transistors with a larger channel width. The digit before D indicates the number of inputs of the cell if larger than 1.

The number of stages in the ROs has been chosen to achieve an oscillation frequency  $f_{\text{RO}} \simeq 100$  MHz before irradiation. The chip enables measurement of the oscillation frequency of each RO and the power consumption of each library (i.e., 16 ROs combined). The current can be measured with either the ROs oscillating ( $I_{\text{RO}}^{\text{osc}}$ ), or stopped (static current  $I_{\text{RO}}^{\text{stc}}$ ). During exposure the ROs are oscillating and are stopped only to measure the static power consumption. When the ROs are not oscillating, the irradiation is stopped.

### 7.2.2 TESTCHIP28

TESTCHIP28 was designed to study the radiation response of isolated MOS transistors, i.e., transistors with all terminals accessible and measurable. The

chip includes a structure with 4 nMOS and 4 pMOS minimum size transistors ( $W/L = 0.1 \mu\text{m}/0.03 \mu\text{m}$ ). Devices of the same polarity (i.e., nMOS or pMOS) are separated in 4 groups, similarly to what described in [15]. Different groups can be biased with different voltages, allowing to investigate the effect of the bias on the radiation response in a single exposure. Notice that the smaller sizes used in the SRAMs are forbidden by the design rules and cannot be manufactured outside the dedicated SRAM structure.

Measurement and irradiation of TESTCHIP28 were performed with the setup described in Chapter 3.

### 7.2.3 X-ray irradiation

High-dose-rate tests were carried at  $\sim 6 \text{ Mrad}(\text{SiO}_2)/\text{h}$  while LDR irradiation were performed at  $\sim 0.1 \text{ Mrad}(\text{SiO}_2)/\text{h}$ . This DR is one order of magnitude lower than typical dose-rates used in qualification procedures for ultra-high doses, but is still at least ten times faster than what expected in the most exposed regions of HL-LHC particle detectors ( $1 \text{ Grad}/10 \text{ years} \simeq 0.01 \text{ Mrad/h}$ ). After exposure, the chip irradiated at HDR was annealed under the same temperature and bias conditions as during irradiation. For all tests, the irradiation is stopped during measures.

## 7.3 Results

### 7.3.1 Dose-rate effects

#### SRAMs

Fig. 7.5 shows the time evolution of the static current  $I_{\text{SRAM}}^{\text{stc}}$  for DPUHD SRAMs irradiated to  $200 \text{ Mrad}(\text{SiO}_2)$  at either high or lower dose-rate. The current was measured at  $f_{\text{SRAM}} = 0.82 \text{ GHz}$ ,  $V_{\text{SRAM}} = 0.9 \text{ V}$ , and has been normalized to its pre-radiation value. A  $f_{\text{SRAM}} = 0.82 \text{ GHz}$  was chosen because it is close to the maximum value inside the OA at  $V_{\text{SRAM}} = 0.9 \text{ V}$ . Following exposure, the HDR-irradiated chip was kept under identical temperature and bias conditions to those applied during irradiation for a period equivalent to that required for LDR irradiation to be completed.

Compared to the end of the HDR irradiation (without annealing), the increase in  $I_{\text{SRAM}}^{\text{stc}}$  at  $200 \text{ Mrad}(\text{SiO}_2)$  is more than 2 times larger in the LDR test. This larger increase is not explainable by the difference in time between the end of irradiation at HDR and LDR, as  $I_{\text{SRAM}}^{\text{stc}}$  steadily decreases after the end of the HDR exposure. The larger increase of leakage current at LDR is measured also at other voltage/frequencies points and other SRAMs, as indicated in Table 7.4. The parameter  $K_{\text{SRAM}}^{\text{stc}}$  is equal to the ratio of  $I_{\text{SRAM}}^{\text{stc}}$  at the end of the test, i.e., for  $200 \text{ Mrad}(\text{SiO}_2)$  and  $t = 2000 \text{ h}$ , and before irradiation:

$$K_{\text{SRAM}}^{\text{stc}} = \frac{I_{\text{SRAM}}^{\text{stc}}(\text{TID} = 200 \text{ Mrad}, t = 2000 \text{ h})}{I_{\text{SRAM}}^{\text{stc}}(\text{TID} = 0 \text{ rad})} \quad (7.1)$$

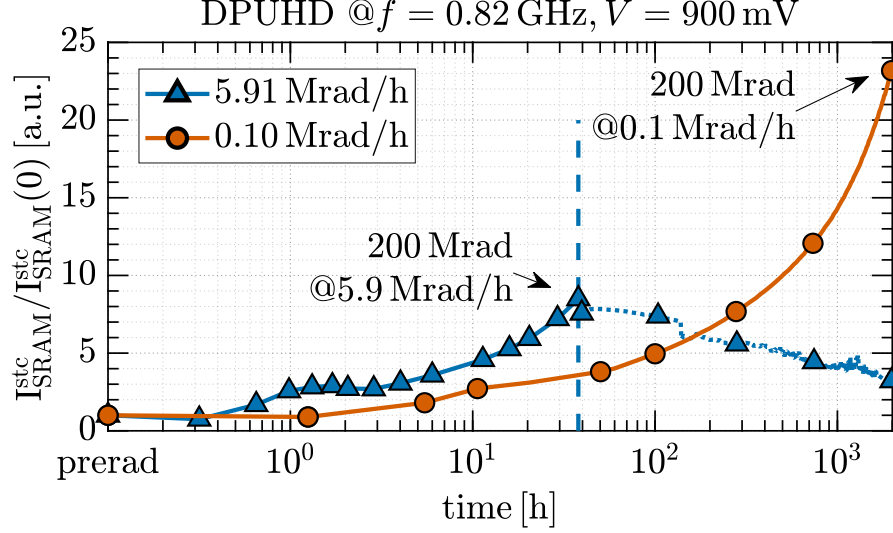


Figure 7.5: Static current in DPUHD SRAMs irradiated to 200 Mrad( $\text{SiO}_2$ ) at different DRs. The red lines with circular markers indicate the results for the HDR test while the blue line with triangular markers show the LDR test. The blue vertical dashed line indicates the end of HDR irradiation. Solid lines are used for measures taken during irradiation, while dotted lines indicate measures taken during annealing.

Table 7.4: DR effects on  $I_{\text{SRAM}}^{\text{stc}}$

| type                  | $V_{\text{SRAM}}$ | $f_{\text{SRAM}}$ | HDR<br>$K_{\text{SRAM}}^{\text{stc}}$ | LDR<br>$K_{\text{SRAM}}^{\text{stc}}$ | $R_{\text{SRAM}}^{\text{stc}}$ |
|-----------------------|-------------------|-------------------|---------------------------------------|---------------------------------------|--------------------------------|
| DPUHD                 | 900 mV            | 0.82 GHz          | 3.21                                  | 23.18                                 | 7.21                           |
|                       | 900 mV            | 0.02 GHz          | 3.23                                  | 22.87                                 | 7.09                           |
|                       | 600 mV            | 0.02 GHz          | 4.71                                  | 33.19                                 | 7.05                           |
| SP +<br>SPUHD<br>+ DP | 900 mV            | 0.82 GHz          | 3.62                                  | 27.41                                 | 7.61                           |
|                       | 900 mV            | 0.02 GHz          | 3.37                                  | 26.61                                 | 7.90                           |
|                       | 600 mV            | 0.02 GHz          | 5.38                                  | 36.98                                 | 6.87                           |

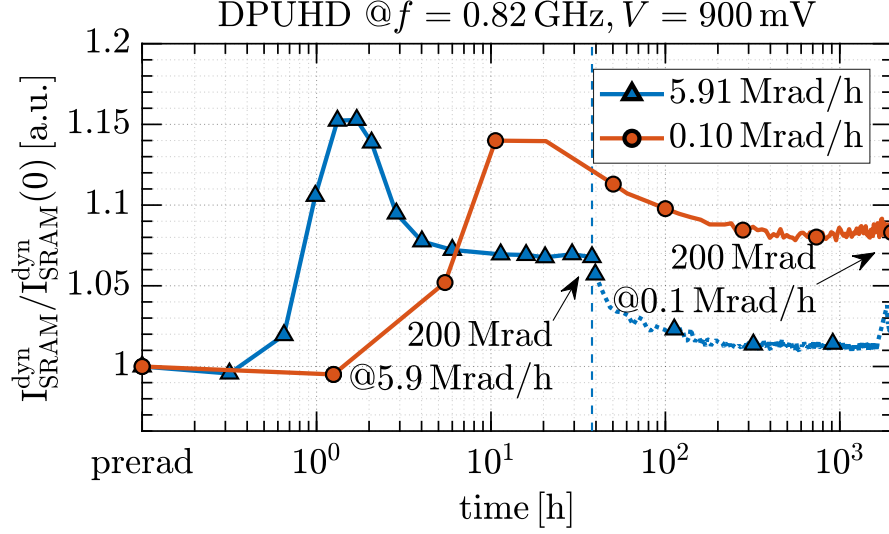


Figure 7.6: TID-induced variation of dynamic current in DPUHD SRAM irradiated at different DRs.

while the dose-rate coefficient  $R_{\text{SRAM}}^{\text{stc}}$  defined as

$$R_{\text{SRAM}}^{\text{stc}} = K_{\text{SRAM}}^{\text{stc}}(\text{LDR}) / K_{\text{SRAM}}^{\text{stc}}(\text{HDR}) \quad (7.2)$$

quantifies the relative increase of  $I_{\text{SRAM}}^{\text{stc}}$  at the lower dose-rate. While  $K_{\text{SRAM}}^{\text{stc}}$  changes depending on the voltage,  $R_{\text{SRAM}}^{\text{stc}}$  is comparable between different voltages, and always higher than 1, meaning that  $I_{\text{SRAM}}^{\text{stc}}$  increases more at LDR than at HDR. A similar result is measured in all available SRAMs (not shown).

While the static current increases significantly with TID and is dependent on the dose-rate, the dynamic current  $I_{\text{SRAM}}^{\text{dyn}} = I_{\text{SRAM}}^{\text{run}} - I_{\text{SRAM}}^{\text{stc}}$  is much less sensitive to TID and only slightly dependent to dose-rate, as shown in Fig. 7.6 for DPUHD.

### Ring-Oscillators

ROs have comparable behavior to SRAMs in terms of dose-rate dependence. Fig. 7.7 reports the static current ( $I_{\text{RO}}^{\text{stc}}$ ) for 9T,  $L = 35$  nm, standard-VTH ROs libraries.

The sudden change in current after the end of HDR irradiation is caused by a problem in the measurement setup that happens between the first and second measurement whenever the test is stopped and restarted. A similar “jump” can be observed in both LDR and HDR between the first and second measurement during irradiation. Despite the undesired behavior, the conclusion remains the same: ROs irradiated with LDR experience a larger increase in static current compared to those irradiated with high-dose-rates. This larger increase cannot be explained by TDEs, as  $I_{\text{RO}}^{\text{stc}}$  decreases when irradiation is stopped. Note that, while the difference between  $I_{\text{RO}}^{\text{stc}}$  increase at the end of the HDR exposure and at the end of the LDR test might seem marginal, the LDR irradiation is still at least ten times faster than what expected in particle detectors ( $1 \text{ Grad}/10 \text{ years} \simeq 0.01 \text{ Mrad/h}$ ).



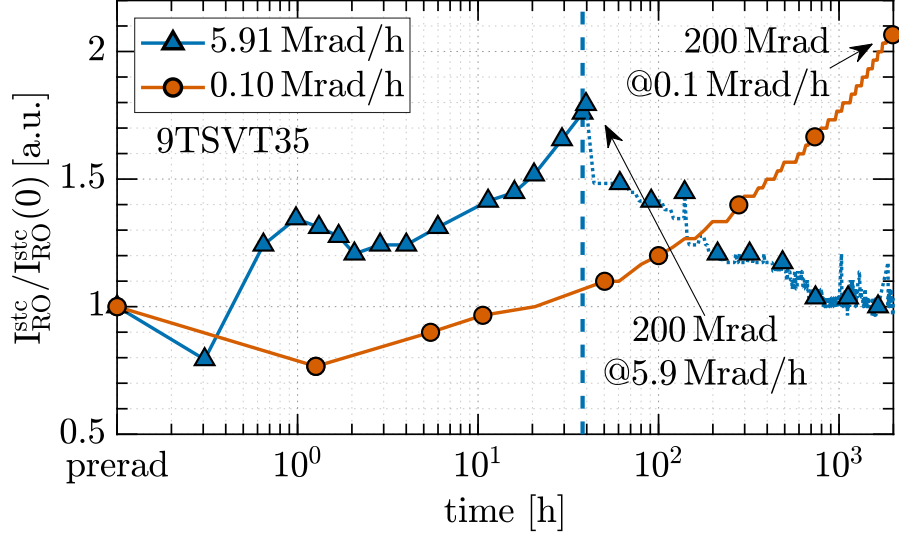


Figure 7.7: Static current in  $L = 35$  nm, standard-VTH, 9 tracks ROs libraries irradiated to 200 Mrad( $\text{SiO}_2$ ) at different DRs.

Similar to SRAMs, both the TID- and dose-rate-sensitivity of the dynamic current  $I_{RO}^{dyn} = I_{RO}^{osc} - I_{RO}^{stc}$  are reduced compared to the static current, as illustrated in Fig. 7.8.

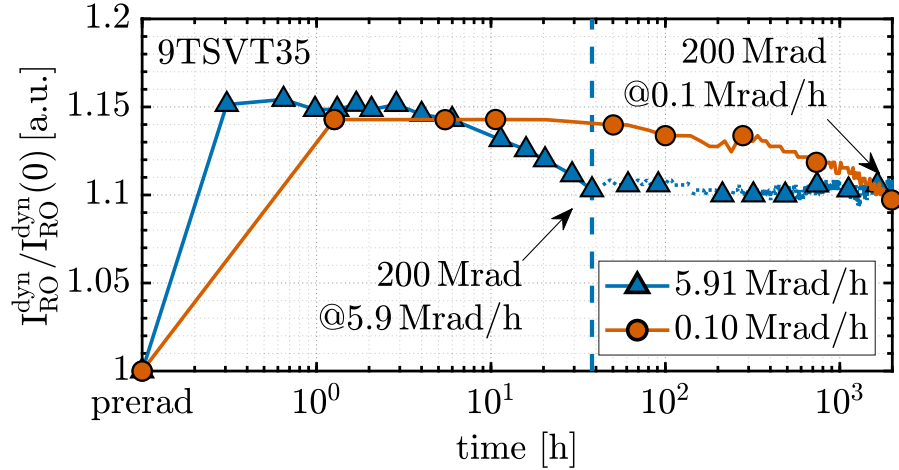


Figure 7.8: Dynamic current ( $I_{RO}^{dyn} = I_{RO}^{osc} - I_{RO}^{stc}$ ) variation in  $L = 35$  nm, standard-VTH, 9 tracks ROs libraries irradiated to 200 Mrad( $\text{SiO}_2$ ) at different DRs. The sudden increase in the second measure at both high and low dose-rate is caused by a problem in the measurement system and it is not a TID-induced effect. From the second measure, the dynamic current tends to decrease with TID.

This result is consistent among all libraries, as specified by the dose-rate coefficient  $R_{RO}$  reported in Fig. 7.9. For the static current,  $R_{RO}^{stc} > 1$  for all libraries, indicating that  $I_{RO}^{stc}$  increases more at LDR. On the other hand, a  $R_{RO}^{dyn} \simeq 1$  evidences a negligible dependence of  $I_{RO}^{dyn}$  to dose-rate.

Although the increase in static current consumption is sensitive to true dose-

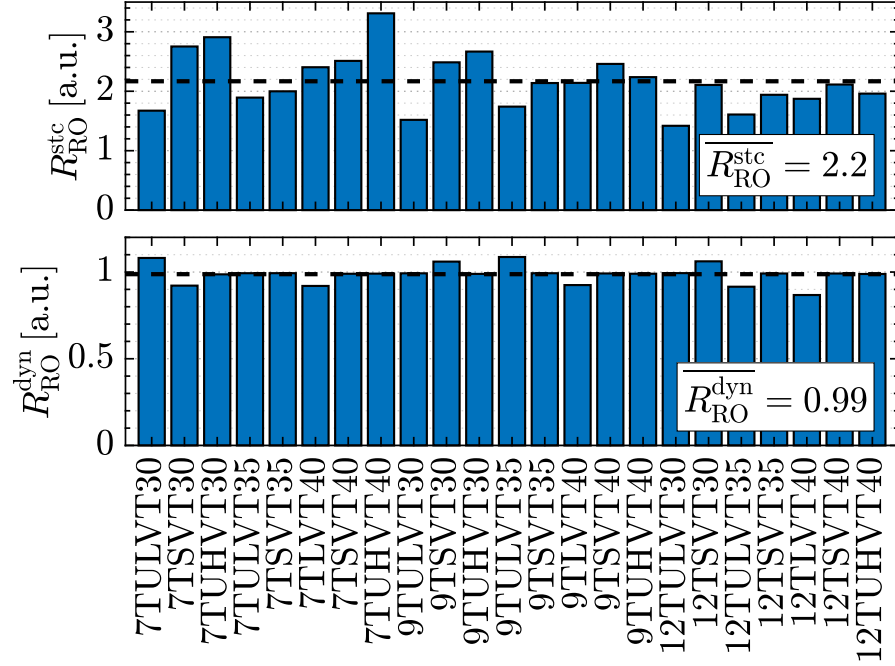


Figure 7.9: Static (top row) and dynamic (bottom row) dose-rate coefficient for all RO libraries. The average among all libraries is identified by a dashed black line and its value is reported in the bottom-right of the plot.

rate effects, the radiation-induced variation of the oscillating frequency  $f_{RO}$  appears to be independent of DR. Fig. 7.10 shows the percentage variation of  $f_{RO}$  for 4-input-NOR (NR4) ROs in 7-tracks,  $L = 40$  nm libraries, for 3 threshold voltages (LVT, SVT, UHVT).

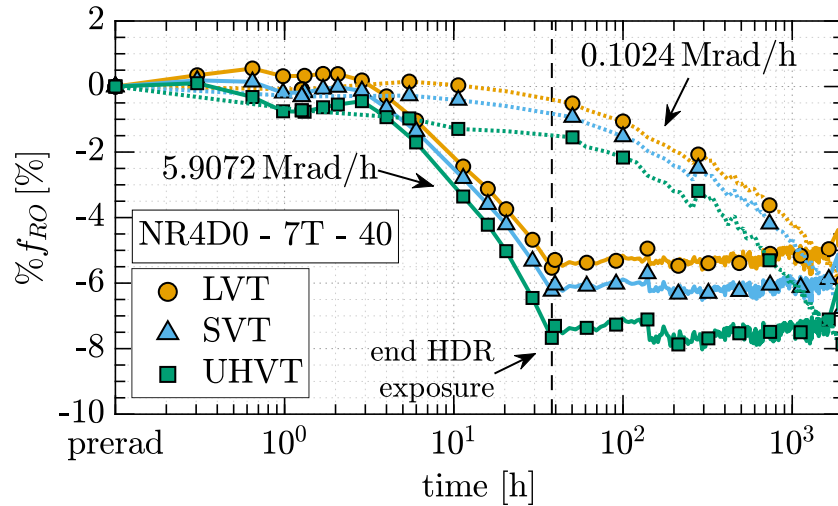


Figure 7.10: Percentage variation of oscillation frequency for NR4D0-based RO in 7-tracks,  $L = 40$  nm libraries, for 3 threshold voltages (LVT, SVT, UHVT). The results for the HDR test are reported by solid lines, while the LDR test results are shown by dotted lines.

The D0 suffix in the cell name indicates the driving strength of the cell. NR4D0 ROs are particularly sensitive to TID due to the 4 pMOS transistors connected in series in the pull-up network and the relatively small channel width  $W$  of the transistors in driving strength 0 cells [132].

The percentage degradation of  $f_{RO}$  at 200 Mrad( $\text{SiO}_2$ ) is independent of dose-rate and  $f_{RO}$  shows minimal evolution after the end of the HDR exposure, with a total variation comparable to that of LDR-irradiated devices. A similar behaviour is measured in all 368 ROs. As discussed later, the difference between the dose-rate sensitivity of static current and oscillation frequency is related to the different sensitivity of TID-induced degradation mechanisms happening at transistor level.

### 7.3.2 Temperature effects

#### Isolated MOS transistors

The probe card system used to measure TESTCHIP28 makes long-term LDR tests on isolated devices nearly impossible. The isolated transistors were instead irradiated at different temperatures and biases. Elevated Temperature Irradiation (ETI) is a technique used to evaluate the presence of ELDRS in electronic components through high dose-rate tests [109, 169]. The purpose of these tests is therefore to evaluate if and how high-temperature irradiation affects the radiation response of isolated devices and to correlate the results with the DR-sensitivity of SRAMs and ring-oscillators. The variation of static power dissipation in SRAMs and ROs

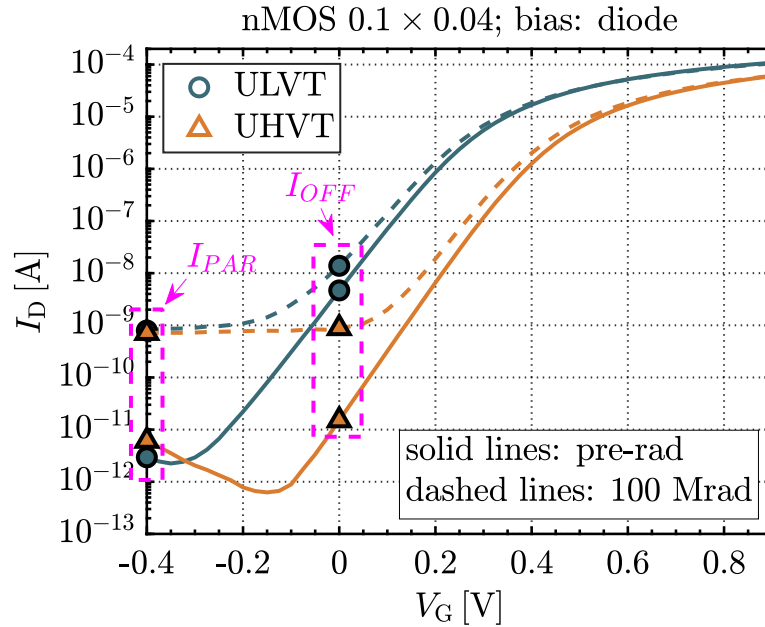


Figure 7.11:  $I_D - V_G$  characteristics of  $W/L = 0.1 \mu\text{m}/0.04 \mu\text{m}$  ULVT and UHVT nMOS transistors irradiated to 100 Mrad( $\text{SiO}_2$ ). The increase in  $I_{OFF}$  in the ULVT device is mainly caused by a negative  $V_{TH}$  shift, while variation of  $I_{OFF}$  in the UHVT transistor is primarily caused by the current flowing in the parasitic channels. Note that  $I_{PAR}$  is almost independent on the VT flavor of the transistors.

is related to the variation of the leakage current  $I_{\text{OFF}} = I_D(V_{\text{GS}} = 0 \text{ V}, V_{\text{DS}} = V_{\text{DD}})$  in nMOS transistors.  $I_{\text{OFF}}$  can increase due to a negative  $V_{\text{TH}}$  shift [87] and/or the opening of source-to-drain parasitic paths at the two edges of the channel [76, 170, 87, 82]. This difference is better explained with the support of Fig. 7.11, where the  $I_D - V_G$  characteristics of  $W/L = 0.1 \mu\text{m}/0.04 \mu\text{m}$  nMOS transistors with different VT are reported. The increase in  $I_{\text{OFF}}$  in UHVT devices is mainly due to the negative  $V_{\text{TH}}$  shift, while the  $I_{\text{OFF}}$  in ULVT nMOS is dominated by the parasitic current  $I_{\text{PAR}}$ . To decouple the two effects, the parasitic leakage current  $I_{\text{PAR}}$  was measured at  $V_{\text{GS}} = -0.4 \text{ V}$ , where the post-rad drain-to-source current  $I_D$  is dominated by the parasitic channels and the variation in  $V_{\text{TH}}$  has a negligible effect.

To understand if the LDR sensitivity of  $I_{\text{SRAM}}^{\text{stc}}$  and  $I_{\text{RO}}^{\text{stc}}$  is related to the increase in parasitic current or to a negative threshold voltage shift, Fig. 7.12 shows the variation in  $I_{\text{PAR}}$  (top row) and  $V_{\text{TH}}$  (second row) for minimum size nMOS transistors irradiated at  $-30^\circ\text{C}$ ,  $25^\circ\text{C}$ ,  $100^\circ\text{C}$ , and  $120^\circ\text{C}$ . The left column reports devices biased in onlyVDS configuration ( $V_{\text{GS}} = 0 \text{ V}$ ,  $V_{\text{DS}} = 0.9 \text{ V}$ ), while the right column displays results for nMOS biased in diode configuration ( $V_{\text{GS}} = V_{\text{DS}} = 0.9 \text{ V}$ ) during exposure.

The increase in  $I_{\text{PAR}}$  is more pronounced in devices irradiated at high temperature (HT), regardless of the applied bias. This result strongly suggests that the TID-induced parasitic current is sensitive to true DR effects. Time-dependent effects, in fact, tend to reduce  $I_{\text{PAR}}$ , as evidenced by the decrease in leakage current during post-irradiation annealing observed in 28 nm [11, 132], other nodes [171, 172], and highlighted by the results in Figs. 7.5 and 7.7. Since HT accelerates time-dependent effects (i.e., accelerates annealing), a smaller increase in  $I_{\text{PAR}}$  during HT irradiation would be expected if TDEs dominated the radiation response. As a consequence, the dose-rate sensitivity of  $I_{\text{SRAM}}^{\text{stc}}$  and  $I_{\text{RO}}^{\text{stc}}$  is likely related to a ELDRS in source-to-drain leakage current of the nMOS transistors.

To further support the relationship between  $I_{\text{PAR}}$  and  $I_{\text{RO}}^{\text{sat}}$ , it is interesting to note that the RO libraries that experience the greater increase in  $I_{\text{RO}}^{\text{sat}}$  at LDR are those that have a small pre-rad static current (e.g. UHVT and/or 7T libraries in Fig. 7.9). Since  $I_{\text{PAR}}$  is independent on the  $W$  of the channel and only moderately dependent on the threshold voltage flavor, devices with a small pre-rad  $I_{\text{OFF}}$  are the ones that experience the largest variations after TID. This also explains why the relative increase in power consumption is higher in SRAMs than in ROs ( $\sim \times 7$  in SRAM and  $\sim \times 2$  in ROs). As reported in Table 7.1, MOS devices in SRAMs have a  $W$  smaller than the minimum used in standard cells (100 nm). Moreover, many cells in the ROs have transistors with  $W$  larger than the minimum (e.g., the nMOS in a D0 inverter in the 9T library has a  $W = 140 \text{ nm}$ ).

While  $I_{\text{PAR}}$  increases more at high temperature independently on the voltage applied, the radiation response of  $\Delta V_{\text{TH}}$  at different temperatures changes with bias. The variation of  $V_{\text{TH}}$  is almost independent on temperature when  $V_{\text{GS}} = 0 \text{ V}$ , while devices biased in diode configuration show a larger positive  $\Delta V_{\text{TH}}$  when irradiated at high temperature. Note that a positive  $\Delta V_{\text{TH}}$  goes in the direction of reducing the  $I_{\text{OFF}}$  and therefore cannot explain the larger power consumption

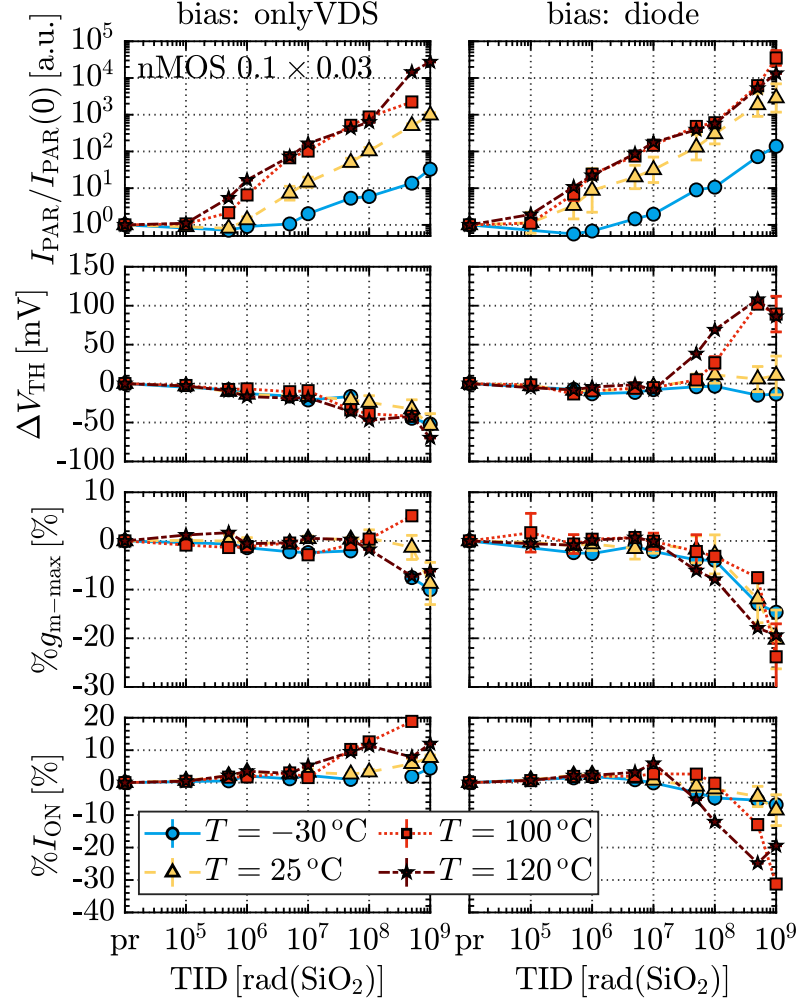


Figure 7.12:  $I_{\text{PAR}}$  increase,  $V_{\text{TH}}$  shift, and percentage variation of  $g_{\text{m-max}}$  and  $I_{\text{ON}}$  in  $W/L = 0.1 \mu\text{m}/0.03 \mu\text{m}$  nMOSFETs irradiated at different temperatures in onlyVDS (left) and diode (right) bias configuration. These results are a collection of data from many tests. For  $-30^\circ\text{C}$  and  $120^\circ\text{C}$  data, only one nMOS per TID is reported. For  $100^\circ\text{C}$ , 2 nMOS are reported for diode bias and 1 for onlyVDS bias. For  $25^\circ\text{C}$  test, a minimum of 4 devices per TID for diode configuration and 2 devices for onlyVDS bias are reported. Given the relatively low sensitivity of the TID response of 28 nm CMOS node to  $V_{\text{DS}}$  [89], these two bias configurations offer a comprehensive overview of the dependency of the radiation response on temperature and bias.

in SRAMs and ROs irradiated at LDR. Similar to  $I_{\text{PAR}}$ , post-irradiation annealing tends to reduce the  $V_{\text{TH}}$  shift [11], meaning that time-dependent effects go in the direction of limiting the variation of  $V_{\text{TH}}$ . This result suggests that  $\Delta V_{\text{TH}}$  might be sensitive to true DR effects when a  $V_{\text{GS}} > 0 \text{ V}$  is applied, but does not explain the larger increase in  $I^{\text{stc}}$  in SRAMs and ROs at LDR.

The last two rows of Fig. 7.12 show percentage variation of the maximum of the transconductance  $g_{\text{m}}$  and the maximum of the drain current  $I_{\text{ON}} = I_{\text{D}}(V_{\text{GS}} =$

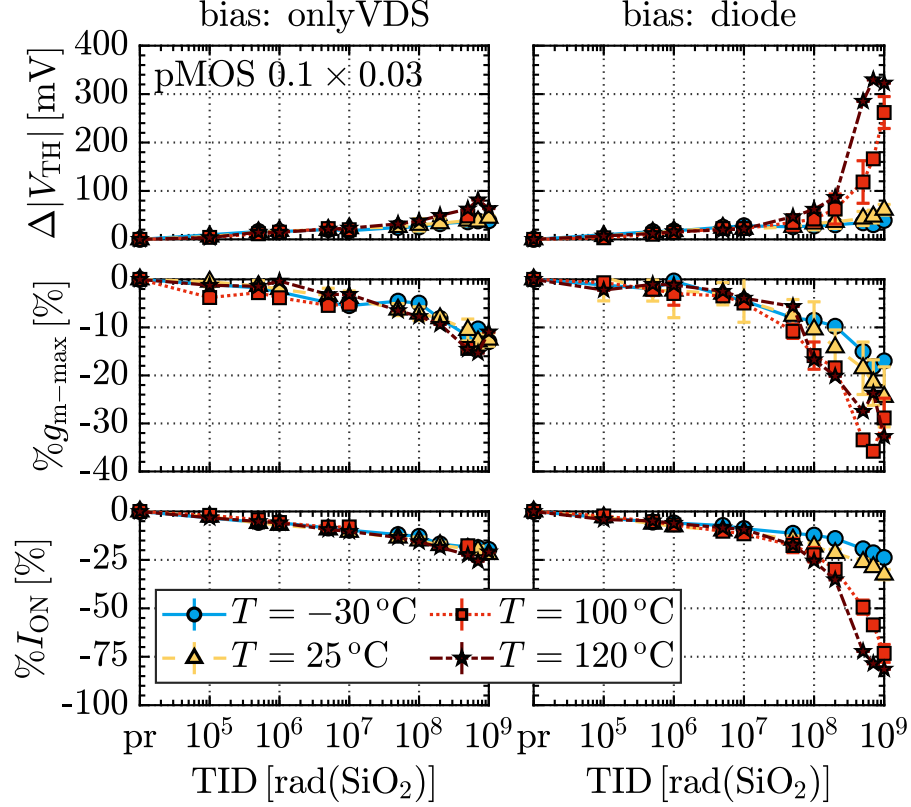


Figure 7.13:  $V_{TH}$  shift and percentage variation of  $g_{m-max}$  and  $I_{ON}$  in  $W/L = 0.1 \mu\text{m}/0.03 \mu\text{m}$  pMOSFETs irradiated at different temperatures in onlyVDS (left) and diode (right) bias configuration.

$V_{DS} = 0.9 \text{ V}$ ). The TID sensitivity of both parameters is larger in samples biased in diode conditions. However, while the TID-induced variation of  $g_m$  is only slightly dependent on temperature,  $I_{ON}$  in diode-biased devices degrades more at HT. This behaviour is caused by the  $V_{TH}$  increase reported in the second row of Fig. 7.12.

A similar relation between temperature and bias was measured in pMOSFETs, as reported in Fig. 7.13. The percentage degradation of  $I_{ON}$  depends on temperature when the devices are biased in diode configuration ( $V_{GS} = V_{DS} = -0.9 \text{ V}$ ), while it is only slightly dependent on temperature when  $V_{GS} = 0 \text{ V}$ . Similar to nMOS, the temperature-sensitivity of  $I_{ON}$  is caused by a temperature-dependent  $V_{TH}$  shift.

Since the oscillation frequency of ROs can be expressed as  $f_{RO} \sim \frac{I_D}{NC_L V_{DD}}$ , where  $N$  is the number of stages in the RO,  $C_L$  is the load capacitance, and  $I_D$  is the current flowing in transistors [173], the minor temperature dependence of  $I_{ON}$  in nMOS and pMOS transistors biased in onlyVDS configuration correlates well with the small dose-rate sensitivity of the TID response of  $f_{RO}$  reported in Fig. 7.10.

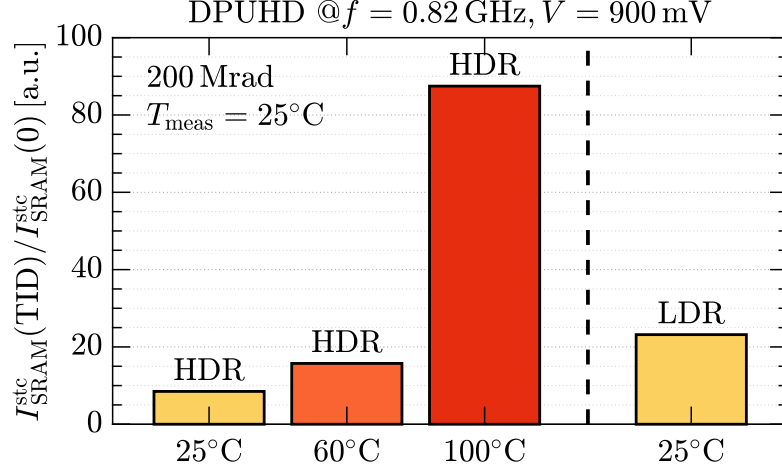


Figure 7.14: TID-induced increase of  $I_{\text{STC\_SRAM}}^{\text{stc}}$  in DPUHD SRAM exposed to 200 Mrad( $\text{SiO}_2$ ) at different temperatures and dose-rates. The measurements were taken at  $T_{\text{meas}} = 25^\circ\text{C}$ .

Table 7.5:  $I_{\text{SRAM}}^{\text{dyn}}$  ratio VS temperature

| DR                                                                         | HDR   |       |        | LDR   |
|----------------------------------------------------------------------------|-------|-------|--------|-------|
| $T$                                                                        | 25 °C | 60 °C | 100 °C | 25 °C |
| $I_{\text{SRAM}}^{\text{dyn}}(\text{TID})/I_{\text{SRAM}}^{\text{dyn}}(0)$ | 1.07  | 1.14  | 0.60   | 1.08  |

## SRAM

The enhanced high-temperature sensitivity of leakage current measured in nMOS transistor causes  $I_{\text{STC\_SRAM}}^{\text{stc}}$  to increase more when SRAMs are irradiated at high temperature. Fig. 7.14 shows the relative increase of  $I_{\text{STC\_SRAM}}^{\text{stc}}$  for devices exposed to 200 Mrad( $\text{SiO}_2$ ) at different temperatures. The measurements were taken at the  $T_{\text{meas}} = 25^\circ\text{C}$ . The last bar on the right reports the result measured at LDR. On the other hand, the increase in dynamic current is not very sensitive to temperature, as reported in Table 7.5.

## RO

A larger increase in static current is measured also in ROs when irradiated at high temperature. Fig. 7.15 shows the relative increase of  $I_{\text{RO}}^{\text{stc}}$  for 9 RO libraries exposed to 200 Mrad( $\text{SiO}_2$ ) at different temperatures and dose-rates. Also in this case,  $I_{\text{RO}}^{\text{stc}}$  increases significantly more in devices exposed at high temperatures. As expected from dose-rate tests on ROs and temperature tests on single devices, instead, the TID-induced  $f_{\text{RO}}$  degradation is only slightly dependent on temperature (Fig. 7.16).

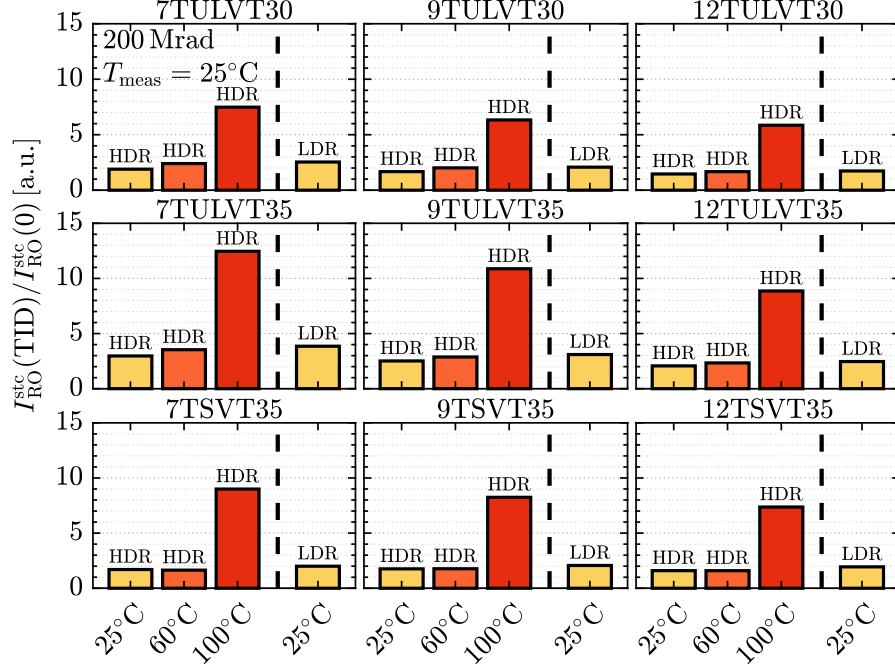


Figure 7.15: TID-induced increase of  $I_{\text{RO}}^{\text{stc}}$  in 9 RO libraries exposed to 200 Mrad( $\text{SiO}_2$ ) at different temperatures and dose-rates. The measurements were taken at  $T_{\text{meas}} = 25^\circ\text{C}$ .

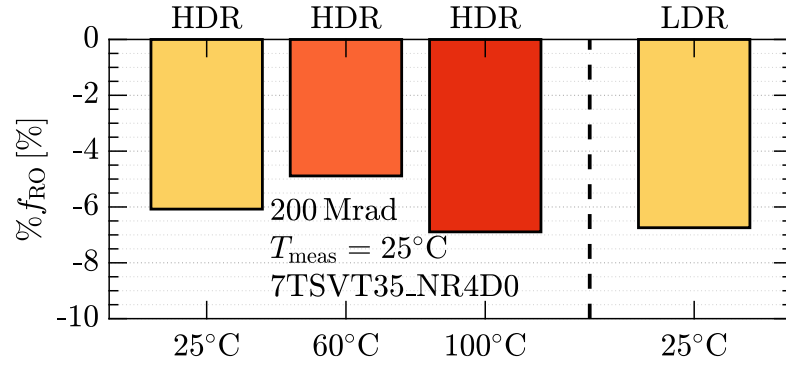


Figure 7.16: TID-induced degradation of  $f_{\text{RO}}$  in 9TSVT35\_ND4D0 RO exposed to 200 Mrad( $\text{SiO}_2$ ) at different temperatures and dose-rates. The measurements were taken at the  $T_{\text{meas}} = 25^\circ\text{C}$ .



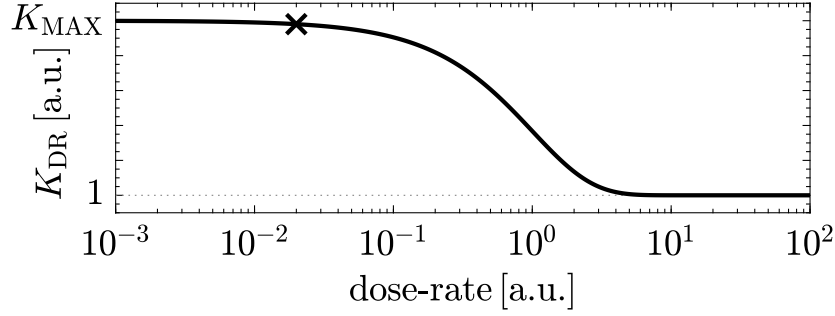


Figure 7.17: Illustration of the typical dose-rate dependence of ELDRS, where  $K_{\text{DR}}$  represents the LDR degradation factor. The enhanced degradation saturates for sufficiently low dose-rates. The cross marks the DR value at which the enhanced degradation starts to saturate.

## 7.4 Conclusions on ELDRS in 28nm CMOS Technology

The results presented in this chapter on SRAMs and ring-oscillators demonstrate for the first time the presence of ELDRS in a 28 nm CMOS technology. Tests at different temperatures on isolated MOS transistors, SRAMs, and ROs correlate well with the radiation response measured in ROs and SRAMs at low-dose-rate. The greater increase in power consumption at LDR in SRAMs and ROs appears to originate from the DR-sensitivity of parasitic leakage current caused by charge trapped in the STI.

These results also suggest that circuits where MOSFETs are permanently biased with high  $V_{\text{GS}}$  may suffer from DR effects in the  $V_{\text{TH}}$  shift and  $I_{\text{ON}}$  degradation.

These results can represent a first step in defining a qualification procedure for chips designed in 28 nm CMOS technology operating in extreme TID environments. Testing ASICs at ultra-high TID with the dose-rates expected in the particle detectors of HL-LHC is a challenging task due to the long time required to reach such doses. Results on single devices, SRAMs, and ROs show that high-temperature irradiation under bias might be a viable solution for accelerated tests. Determining a quantitative correlation between the effects of temperature and those of DR is beyond the scope of this work. Nevertheless, we can attempt a qualitative analysis of the results. It is known that, in dose-rate-sensitive devices, TID-induced degradation saturates for sufficiently low dose-rates [110, 12, 14, 108, 164, 107, 174, 25, 15], as schematically illustrated in Fig.7.17. The low-dose-rate tests reported in this chapter were performed with a DR  $\simeq 0.1 \text{ Mrad}(\text{SiO}_2)/\text{h}$ , which is at least ten times higher than the maximum DR expected in the detectors of the HL-LHC ( $1 \text{ Grad}/10 \text{ years} \simeq 0.01 \text{ Mrad}/\text{h}$ ). The vast majority of the ASICs installed in the particle detectors will be exposed to much lower DRs. The results in Figs. 7.14 and 7.15 indicate that a temperature of  $100^\circ\text{C}$  causes a significantly larger degradation compared to the LDR test of this work, suggesting that a DR =  $0.1 \text{ Mrad}(\text{SiO}_2)/\text{h}$  is still far from the

saturation point. On the other hand, the results in Fig. 7.12 suggest that the radiation-induced parasitic drain-source current  $I_{\text{PAR}}$  does not further increase with temperature beyond about 100°C. This result may indicate that this temperature is close to the one needed to reach the degradation that would be reached with DRs below the saturation point. Future studies will concentrate on assessing the impact of device size and threshold voltage flavor on dose rate sensitivity and on establishing a quantitative correlation between dose rate and temperature effects.

# Chapter 8

## 22nm Fully Depleted Silicon-On-Insulator

### 8.1 Introduction

Single Event Effects (SEEs) are a major cause of failure for Application-Specific Integrated Circuits (ASICs) operating in harsh radiation environments, such as space or particle accelerators [175]. SEE is a general term that identifies several effects caused by ionizing radiation. The common element between these effects is that they are caused by a single particle with high Linear Energy Transfer (LET), like an energetic ion, generating an ionization tail of electron-hole pairs as it passes through the substrate of a semiconductor device. In a bulk technology, this charge can be collected relatively deep in the substrate and is responsible for current pulses at active nodes of the circuit, giving origin to SEE [176, 177, 178]. SEE are usually categorized in non-destructive or destructive events. Non-destructive events, also called soft-errors, are identified as those for which it is possible to return to pre-irradiation conditions without the need to turn the chip off. Two common examples of soft-errors are Single Bit Upset (SBU) and Multi Bit Upset (MBU), a radiation-induced flip of one or more bit [179, 180, 181], and Single Event Transient (SET) [182, 183, 184, 185], a current or voltage spike traveling in the circuit [183]. Destructive events may result in the destruction of the chip or, if it is possible to return to pre-radiation conditions, require the interruption of the power supply and temporary shutdown of the chip. Single Event Latch-up (SEL) [186, 187] and Single Event Burnout (SEB) [188, 189] are two examples of destructive SEE.

In Fully Depleted Silicon-On-Insulator (FDSOI) technologies, the thin ( $< 7$  nm) silicon channel layer overlays a thick Buried OXide (BOX) ( $\sim 20$  nm) that isolates the channel from the bulk substrate [190]. The presence of the BOX limits the extension of the charge collection region, making these technologies intrinsically more tolerant to SEE than classic bulk devices [191, 192]. Furthermore, the electrical coupling between the front and back channel interfaces in an FDSOI transistor enables the tuning of its electrical characteristics via back-gate biasing [193]. In other words, it is possible to tune the threshold voltage of a device by applying a

voltage on the back gate. Despite the advantages in terms of SEE reliability and tunability, the presence of a tens of nanometers thick BOX makes these technologies intrinsically sensitive to Total Ionizing Dose (TID) effects [194]. Moreover, the high temperature annealing required in the Smart Cut Technique process, a technique typically used in the manufacturing of SOI devices, cause oxygen to out-diffuse from the BOX, leaving behind a number of defects [195, 196]. The TID susceptibility of FDSOI devices results mainly from the coupling between the back gate and the front gate, meaning that charges trapped in the BOX modify the electrical characteristics of the transistor [197, 198, 199, 200, 201]. Thus, although SOI technologies are appealing in reducing SEE, they may exhibit a greater sensitivity to TID compared to bulk technologies. In view of possible application in High Energy Physics (HEP), where doses can be orders of magnitude higher than those typically reached in space applications [202], it is interesting to study the TID response of commercial SOI technologies and if/how it can be improved by dedicated biasing techniques. In this chapter, the characteristics of n- and p-channel transistors with different sizes and threshold voltages in a 22 nm FDSOI technology were evaluated before irradiation and after exposure to X-rays up to a TID of 100 Mrad(SiO<sub>2</sub>). High-temperature annealing and compensation of TID-induced effects using back-biasing were also studied.

The results discussed in this chapter extend the study published in:

[203] Termo, G., Borghello, G., Faccio, F., Kloukinas, K., Caselle, M., Elsehans A. F., Ulusoy, A. C., Koukab, A., Sallese, J.M. "Characteristics and ultra-high total ionizing dose response of 22 nm fully depleted silicon-on-insulator." *Journal of Instrumentation* 19.03 (2024): C03039.

Available with open access at: <https://iopscience.iop.org/article/10.1088/1748-0221/19/03/C03039/meta>

## 8.2 Test structures

The irradiated samples were custom test structures containing several isolated n- and p-channel transistors as schematically depicted in Fig. 8.1. Note that both

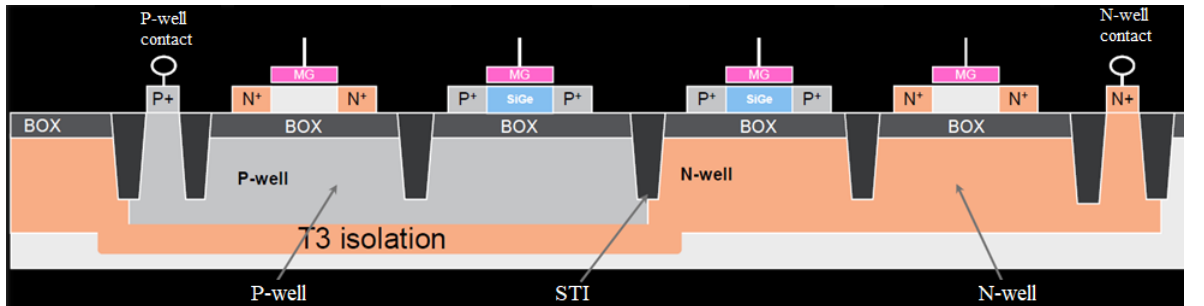


Figure 8.1: Schematic of the irradiated transistors in 22 nm FDSOI. The p-well and n-well contact are used to tune the threshold voltage of the device.

pMOS and nMOS devices can be built on top of a p- or n-well doped substrate region, and that p-wells have to be biased at voltages lower than n-wells. The

chips were designed at Karlsruhe Institute of Technology (KIT) and fabricated in a commercial-grade 22 nm FDSOI technology. In the technology studied, the thin silicon film that forms the channel is undoped and the devices are equipped with an external pad to provide back-gate biasing via p-well/n-well contacts in order to tune the threshold voltage ( $V_{TH}$ ) of the device. While the supply voltage in this technology is 0.8 V, the voltage that can be applied to the back-gate can exceed this value and is limited only by the breakdown of the p-well/n-well diode. The majority of documentation indicates that the maximum value that can be applied to the back-gate is  $\pm 2$  V. However, this is merely a limitation imposed by the models that have been simulated up to  $\pm 2$  V, rather than a physical limitation inherent to the technology itself. Applying a negative bias to the p-well reduces the  $V_{TH}$  of the pMOS (Forward Body Biasing (FBB)) and increases it for the nMOS (Reverse Body Biasing (RBB)). Similarly, applying a positive bias to the n-well increases the  $V_{TH}$  of the pMOS and reduces it for the nMOS.

## 8.3 Results

### 8.3.1 TID response

In this section, the radiation response of 22 nm FDSOI technology is discussed referring only to the devices that are in the p-well, i.e., FBB pMOS and RBB NMOS (left structure in Fig. 8.1). The same phenomena were observed in the devices in the n-well.

In a fully depleted SOI technology, the silicon film of the SOI structure is thin enough that completely depletion can occur, thereby coupling the Front Gate (FG) with the Back Gate (BG). The coupling of the gates makes the threshold voltage of each gate dependent on the conditions of the other [197], meaning that once the two gates are coupled, applying a bias to the BG influences the front channel threshold voltage  $V_{TH}$ . Low, high, and standard threshold voltage transistors were investigated, hereafter denoted as lvt, hvt and, svt, respectively.

Fig. 8.2 shows the  $\Delta V_{TH}^{sat}$  of the FG induced by changing the BG bias from  $-8$  V to  $7$  V in pMOS and nMOS transistors built on p-well, with  $W = 3$   $\mu$ m and  $L$  ranging from 20 nm to 360 nm. As the bias applied to the BG decreases,  $V_{TH}$  linearly decreases for p-type transistors whereas it linearly increases for n-type devices. For a very high FBB, the threshold voltage decreases significantly to the point that the device is on even at very low  $V_G$ , so a true threshold voltage cannot be extracted, which explains the missing data in Fig. 8.2. At very high RBB, however, the coupling between the two gates is lost, and  $V_{TH}$  no longer changes as the BG changes. This effect seems to depend on the channel length, with shorter transistors showing better coupling, as can be seen for minimum length nMOS.

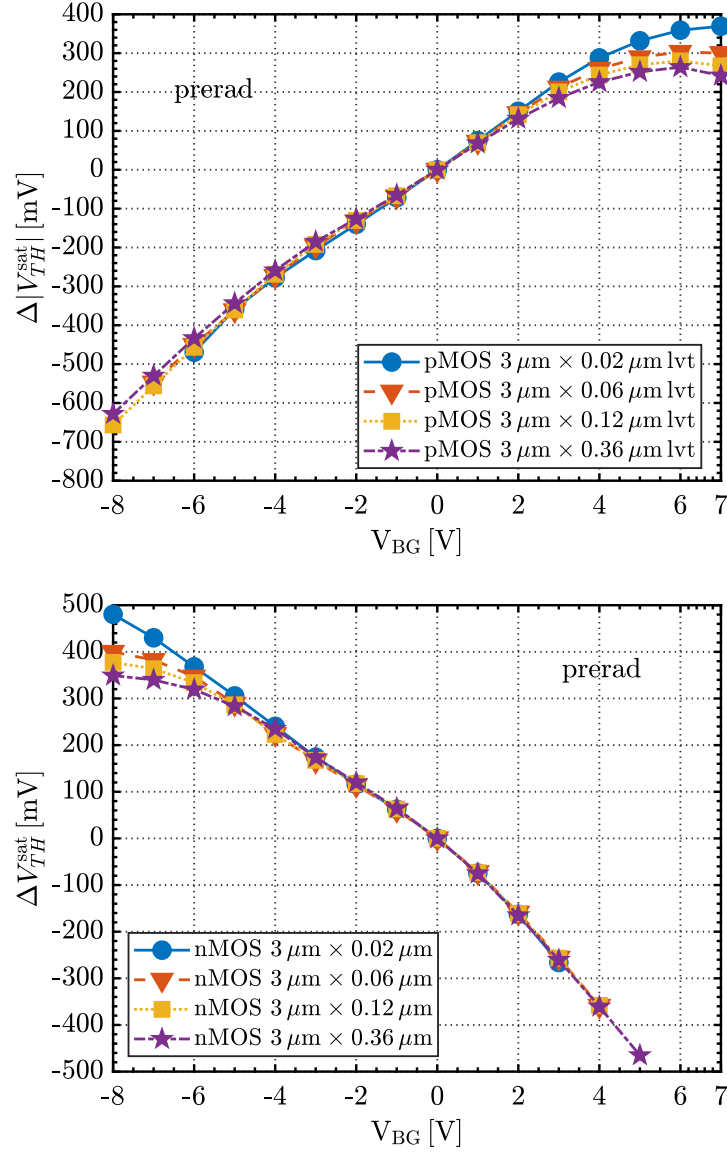


Figure 8.2: Front-gate threshold voltage as a function of back-gate bias of pristine  $W = 3 \mu\text{m}$  and  $L$  ranging from 20 nm to 360 nm pMOS (top) and nMOS (bottom) built on p-well.

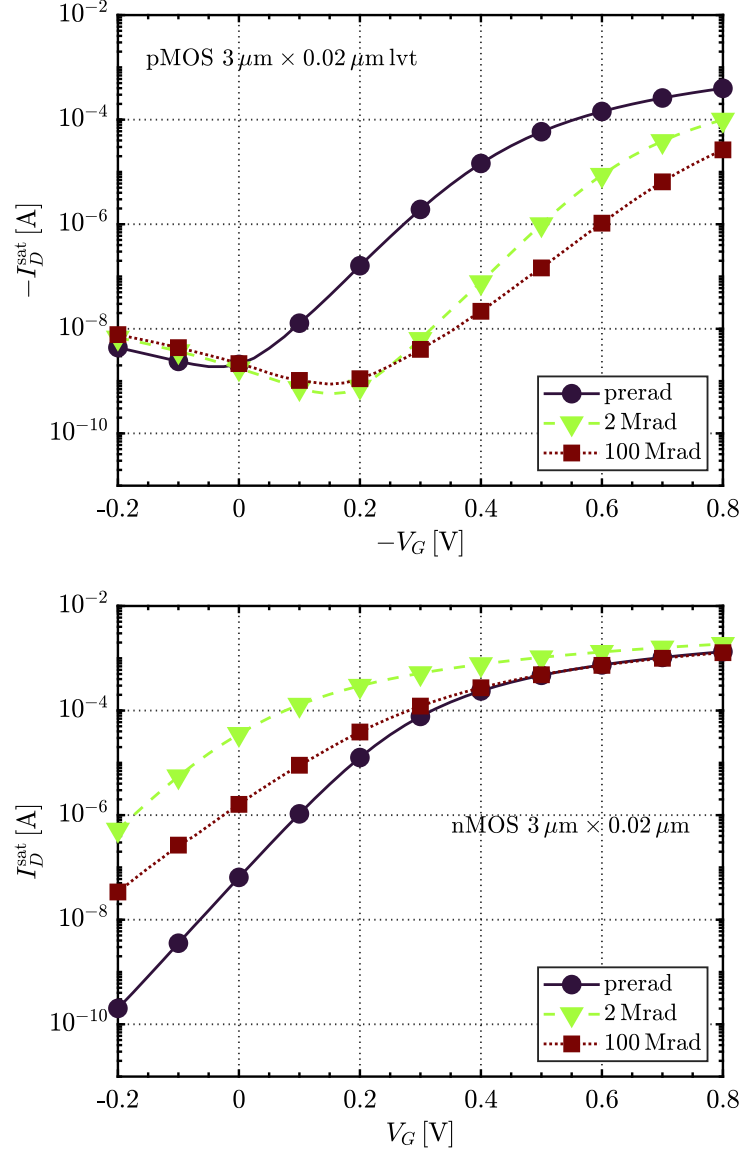


Figure 8.3:  $I_D - V_G$  at  $V_{BG} = 0\text{ V}$  of lvt p- and svt n- type transistors with  $W = 3\ \mu\text{m}$  and  $L = 20\text{ nm}$  exposed up to 100 Mrad( $\text{SiO}_2$ ).

Fig. 8.3 shows the  $I_D - V_G$  curve measured at  $V_{BG} = 0\text{ V}$  of minimum length p- and n-type transistors with  $W = 3\ \mu\text{m}$  irradiated up to 100 Mrad( $\text{SiO}_2$ ) with X-ray at  $T = 25^\circ\text{C}$ . During exposure, the devices were biased with  $V_{FG} = \pm 0.8\text{ V}$ ,  $V_S = V_D = 0\text{ V}$ ,  $V_{BG} = -2\text{ V}$ . Both types of transistors are severely affected by TID. The relatively small dose of 2 Mrad( $\text{SiO}_2$ ) is sufficient to cause a significant shift in the threshold voltage. At 2 Mrad( $\text{SiO}_2$ ), the positive charge accumulated in the BOX reduces the  $V_{TH}$  in the nMOS, thus increasing the current. For higher doses, the accumulation of negative charge at the interface compensates for the positive charge in the oxide, resulting in a reduction in the threshold voltage and a decrease in the subthreshold slope. This is a characteristic behavior of nMOS exposed to TID, observed in all CMOS technologies studied [87]. In contrast, in

pMOS, both the charge trapped in the oxide and the charge at the interface are positive, leading to more significant degradation at the same dose. The observed increase in off current in nMOS transistors is attributed to a reduction in threshold voltage, rather than the opening of parasitic channels from source to drain, as commonly observed in bulk technologies. This may be attributed to the enhanced electrostatic control exerted on the channel in the SOI structure. In previous nodes, the opening of parasitic paths occurred in the lower part of the STI/channel interface, where gate control is weaker [84, 85, 79], and could be observed in the  $V_G < 0$  V region of the  $I_D - V_G$  as a flat current independent of  $V_G$ .

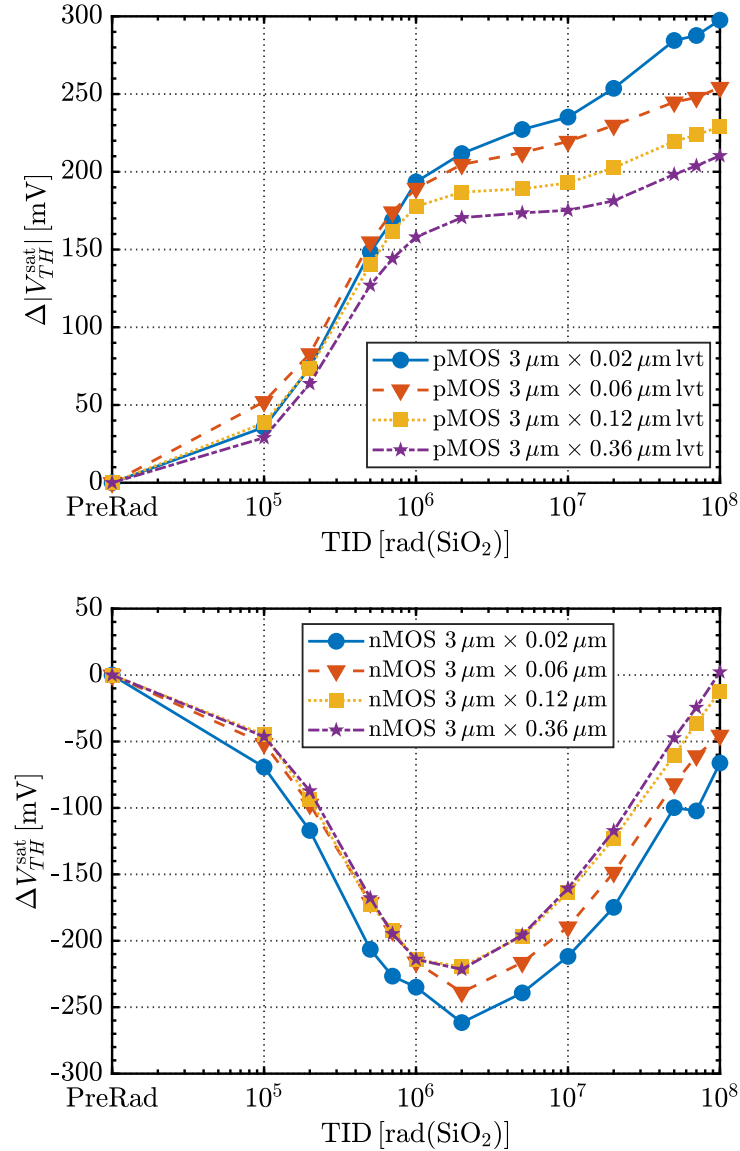


Figure 8.4:  $\Delta V_{TH}^{sat}$ (TID) of p- and n- type transistors with  $W = 3 \mu\text{m}$  and  $L$  ranging from 20 nm to 360 nm exposed to 100 Mrad(SiO<sub>2</sub>).

The dominant TID effect in the 22 nm FDSOI technology is the  $\Delta V_{TH}$  caused by the charge in the buried oxide which being coupled to the front-gate causes a



change in the threshold voltage of the front channel [197, 198, 199, 200, 201], as shown in Fig. 8.4 for devices with same width and different lengths. As previously mentioned, after 2 Mrad( $\text{SiO}_2$ ), nMOS transistors show a rebound caused by the different build-up time of positive charge in the oxides and negative charge at the interface [72, 87, 93, 9] whereas pMOS exhibit a monotonic behavior.

The observed response depends on transistor length, with shorter devices exhibiting a greater variation. This can be better observed in Fig. 8.5 where the  $\Delta V_{TH}^{\text{sat}}$  as a function of channel length is reported. The TID response of some bulk

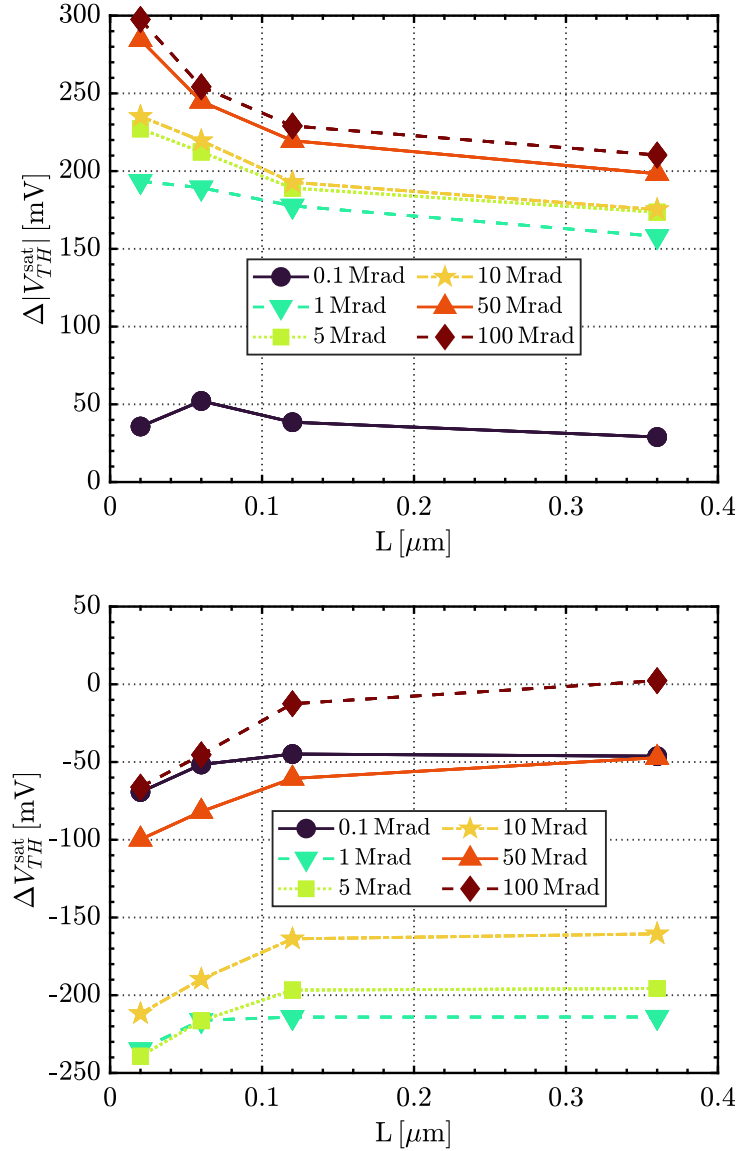


Figure 8.5:  $\Delta V_{TH}^{\text{sat}}$ (TID) of p- and n- type transistors with  $W = 3\mu\text{m}$  and  $L$  ranging from 20 nm to 360 nm exposed to 100 Mrad( $\text{SiO}_2$ ).

technologies depends on  $L$  due to the presence of the Lightly Doped Drain (LDD) [72, 95] or the presence of halo implants in the channel [11] (as described in the Chapter 4). However, in the 22nm FDSOI neither LDD nor halo implants are

used. In this technology, the length dependence also appears in the  $\Delta V_{TH}^{sat}(V_{BG})$  curve of pristine devices when a high RBB is applied (Fig. 8.2), which suggest that this effect is enhanced rather than caused by the irradiation. A possible explanation is that the buildup of interface charge during irradiation act as an additional  $V_{BG}$  which makes the saturation of the  $\Delta V_{TH}^{sat}(V_{BG})$ , i.e., the loss of coupling between FG and BG, appear at lower  $|V_{BG}|$  compared to before irradiation, as shown in Fig. 8.6. As a consequence, the shortest transistor, which loses the coupling the latest, is the one more affected by the charge in the BOX. On the contrary,

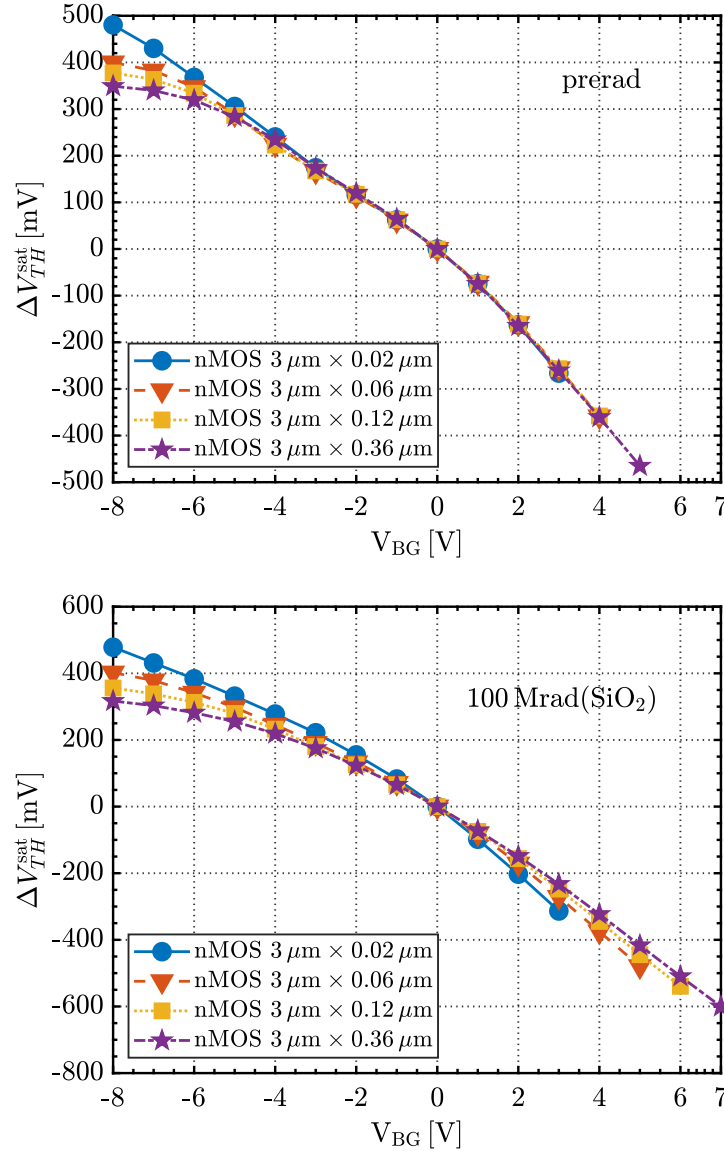


Figure 8.6: Front-gate threshold voltage as a function of back-gate bias of pristine  $W = 3 \mu\text{m}$  and  $L$  ranging from  $20 \text{ nm}$  to  $360 \text{ nm}$  nMOS before irradiation (top) and at  $100 \text{ Mrad}(\text{SiO}_2)$  (bottom).

no width dependence (RINCE described in Chapter 4) of the TID response was observed (not shown). The absence of RINCE and off-current increase, suggest

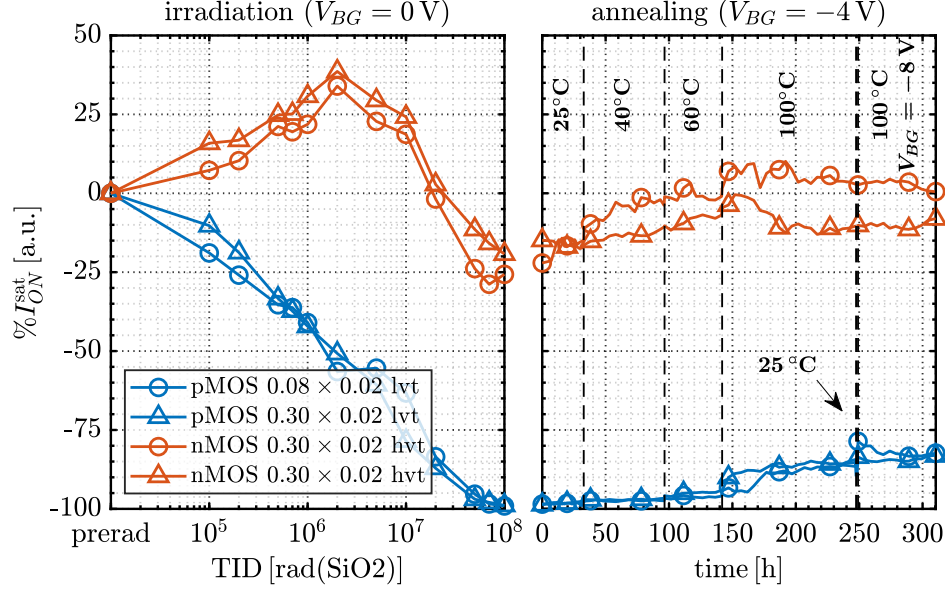


Figure 8.7:  $\%I_{ON}^{sat}$ (TID) of  $[80, 300] \times 20$  nm lvt pMOS and  $[80, 300] \times 20$  nm hvt nMOS irradiated to 100 Mrad(SiO<sub>2</sub>) and annealed at different temperatures  $T = 25 - 100^\circ\text{C}$ . The last measurement after annealing was performed at room temperature.

that the double gate control over the channel strongly limits the influence of the charge trapped in the STI.

Fig. 8.7 shows the percentage degradation of the on current of  $[80, 300] \times 20$  nm lvt pMOS and  $[80, 300] \times 20$  nm hvt nMOS transistors measured at room temperature with  $V_{BG} = 0$  V after irradiation to 100 Mrad(SiO<sub>2</sub>) and then annealed at different temperature up to  $T = 100^\circ\text{C}$ . During irradiation, the devices were biased at  $V_{GS} = \pm 0.8$  V and  $V_{DS} = V_{BG} = 0$  V. The same bias was kept during annealing with exception of the back-gate where  $V_{BG}$  was set to  $-4$  V. In the last  $\sim 50$  h of annealing,  $V_{BG}$  was set to  $-8$  V to enhance the recovery of the devices. The performance of both types of transistors is severely degraded by TID, with pMOS devices most affected (Fig. 8.7, left). In pMOS, a total dose of 1 Mrad(SiO<sub>2</sub>) results in  $\sim 50\%$  degradation of the turn-on current. Unlike what observed in bulk technology [72], the radiation response is independent of the transistor width. The performance of the devices did not recover after several hours of annealing at  $T = 25, 40, 60, 100^\circ\text{C}$ , indicating that the irradiation produced deep-level defects whose removal process requires more energy than that provided during annealing at this temperature. Switching to  $V_{BG} = -8$  V did not significantly enhance recovery.

### 8.3.2 Compensation of TID effects

The most significant effect induced by TID in 22 nm FDSOI is the threshold voltage shift (Fig. 8.4). Since the back-bias provides designer with an additional degree of freedom for tuning the threshold voltage, it might be possible to compensate

for TID induced threshold voltage shift by varying the back-gate bias accordingly. Fig. 8.8 shows the BG voltage that should be applied in order to compensate for the  $V_{TH}$  shift induced by different levels of TID as a function of the length of the transistor for both pMOS and nMOS devices. To obtain compensation voltage

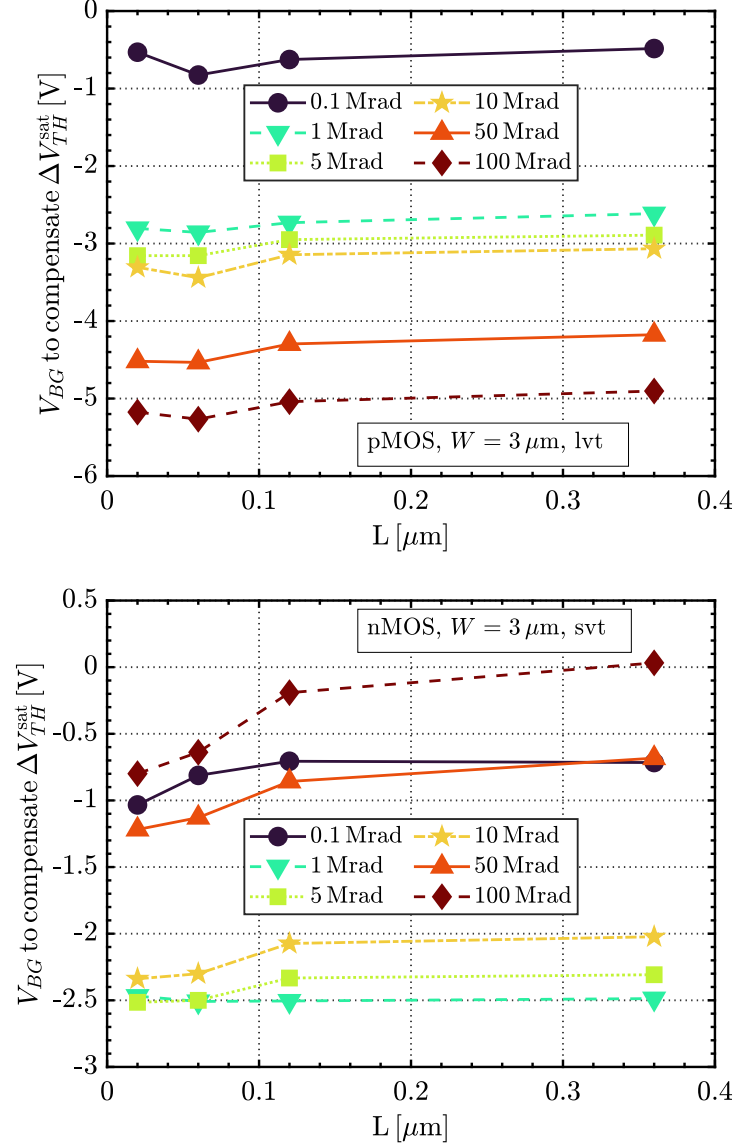


Figure 8.8: Compensation of the threshold voltage shift caused by different levels of TID by applying a different back-gate bias in pMOS (top) and nMOS (bottom) with same width and different lengths.

values, the  $I_D(V_G)$  characteristics of the devices were measured at varying back-gate voltages. The  $V_{BG}$  used ranged from  $-8$  V to  $1$  V with a step size of  $1$  V. The compensation value was then obtained by finding the intersection point between the  $\Delta V_{TH}(V_{BG})$  curve and  $0$  V. It is possible to compensate for the shift caused by a certain level of TID, up to  $100$  Mrad( $\text{SiO}_2$ ), by applying a specific BG bias. Note that the required back bias depends on the size of the transistors. This is

most evident in nMOS transistors, where there is a difference of approximately 1 V between the shortest and longest transistor at 100 Mrad(SiO<sub>2</sub>). The bias to be applied to an specific device also depends on the received dose. In order to apply the appropriate bias in a practical application, it would be necessary to actively monitor the dose during operation and to apply different voltages to devices with different sizes. It should also be noted that the  $V_{BG}$  to be applied to devices of the same size but different polarity is different for a certain level of TID. This difference could be as small as  $\sim 0.5$  V at 0.1 Mrad(SiO<sub>2</sub>) and increase to several volts for higher doses.

## 8.4 Conclusions on 22nm FDSOI

The radiation response of 22 nm FDSOI transistors was evaluated by X-ray irradiation at ultra-high levels of TID. The study revealed that the main TID-induced effect observed in this technology is the coupling between the front and back gates, that allows the charge trapped in the buried oxide to severely shift the front gate threshold voltage. The absence of TID-induced effects typical of bulk technologies such as RINCE and RISCE also confirms that the charge trapped in the BOX dominates the radiation response of this technology. The observed degradation is not recovered when the devices are annealed at high temperature. The possibility to compensate TID-induced effects by varying the back-gate bias has been explored, showing that the  $V_{BG}$  needed to compensate for the TID-induced  $V_{TH}$  shift depends on the channel length and polarity of the device. From a practical standpoint, this study underscores two noteworthy issues in implementing a compensation method in a real chip where hundreds of thousands of n- and p-type transistors with different sizes are involved. Firstly, it is necessary to actively monitor the degradation of the device to apply the appropriate bias. Secondly, the bias to be applied at each TID level is different for devices of different sizes and polarity, posing a significant challenge in the actual application of the compensation method.

# Chapter 9

## Conclusions

This thesis has explored several aspects of radiation-induced degradation mechanisms at very high doses and fluences in several CMOS technologies, providing guidelines for the radiation hardness assurance of ASICs for high-energy physics applications. Through comprehensive studies of 130 nm, 65 nm, 28 nm, and 22 nm CMOS technologies it has been demonstrated how factors such as manufacturing process variability, dose-rate, device size, transistor polarity, and operating conditions are critical to account in the design, testing and qualification of radiation-hardened ASICs.

First, it was shown that the TID-induced degradation in both 130 nm and 65 nm technologies is significantly affected by fab-to-fab and run-to-run variability. This variability is transistor polarity- and size-dependent, making it a critical factor in the design and qualification phases of complex ASICs. The variability in radiation response not only impacts individual transistors but also cascades into larger circuit blocks. These results highlighted the need for a constant monitoring of the manufacturing process of the technologies involved in radiation-hardened designs as well as the limits of simulation models and methodologies which do not take variability into account. Therefore, CERN's EP-ESE-ME group continues to include dedicated monitoring ASICs in each set of ASICs to verify manufacturing process consistency. In addition, this work has helped identify fabrication facilities that employ processes that offer superior radiation response, guiding the selection of foundries for future projects.

In the study of 28 nm CMOS technology, high-fluence irradiation campaigns were carried out, revealing that TID-induced degradation remains the primary concern for this technology, with limited evidence of displacement damage. The results underscore the resilience of 28 nm CMOS transistors, confirming their suitability for use in the high-radiation environments expected at the HL-LHC. This study was a key step in the official adoption of this technology for future upgrades of CERN's particle detector electronics, demonstrating that it can withstand the unprecedented stress of  $10^{16}$  p/cm<sup>2</sup> fluence expected in upcoming CERN experiments."

This thesis also reports the first evidence of Enhanced Low Dose Rate Sensitivity (ELDRS) in SRAMs and ring oscillators 28 nm CMOS technology. This phenomenon, which manifests through increased power consumption at low-dose-

rate due to parasitic leakage currents in shallow trench isolation (STI) regions, is critical for the qualification of circuits for particle detectors. The findings also suggest that circuits with MOSFETs permanently biased at high  $V_{GS}$  may suffer from dose-rate effects in the threshold voltage ( $V_{TH}$ ) and on-current ( $I_{ON}$ ) degradation. This introduces new challenges in testing and qualification, especially for ultra-high TID, as the typical high-dose-rate tests currently used to qualify chips may underestimate the degradation in the final application. The potential of high-temperature irradiation as an accelerated qualification method has been investigated and appears to show promise. However, further research is required to establish a quantitative correlation between temperature effects and dose degradation. The results of this work therefore show that tests conducted exclusively at high dose rate are insufficient to qualify CMOS technologies for applications where the dose rate in the real environment is much lower, such as in CERN detectors. As consequence, designers, based on these results, adopt a margin of safety by designing a TID tolerance 2-3 times higher than expected to account for dose rate effects. Although low-dose testing at the very high TID levels expected in CERN applications is not feasible because of the time required for each test, this study has shown that high-temperature irradiation could be a viable alternative for irradiation testing of 28 nm CMOS technology and possibly in future nodes. However, this method must be carefully evaluated according to the CMOS technology node considered, since high-temperature irradiation was found to be unsuitable for the 130 nm and 65 nm nodes because of the specific effects triggered at high temperatures.

Lastly, the investigation into 22 nm FDSOI transistors highlighted severe degradation mechanisms due to the coupling between the front and back gates, with the charge trapped in the buried oxide being the primary driver of TID-induced threshold voltage shifts. This front-to-back gate coupling creates challenges not encountered in bulk technologies, underscoring the growing complexity of the radiation qualification of advanced nodes. While attempts to mitigate these effects using back-gate biasing showed potential, practical implementation on a large scale remains challenging due to the variability in required compensation across different transistor sizes and polarities. Therefore, this technology is not suitable for applications in the inner parts of detectors at CERN because of its higher sensitivity to TID. However, it could find use in other applications where the expected TID levels are much less severe.

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# Gennaro Termo, PhD

## Electronics Engineer – PhD in Microelectronics

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### Professional Summary —

Experienced radiation effects engineer with 5 years of expertise in semiconductor technology and electronics, specializing in the impact of radiation on CMOS technology for advanced applications. Proven ability to manage and run complex laboratory setups, including leading tests and experiments with X-ray equipment and qualifying semiconductor devices. Strong technical background in semiconductor physics, MOS transistors, and p-n junctions, complemented by proficiency in data analysis tools like MATLAB. Skilled in problem-solving through hands-on testing, simulation (TCAD, Monte Carlo methods), and data interpretation, with a focus on improving the reliability of electronic systems in extreme environments. Adept at collaborating with cross-functional teams, delivering presentations, and communicating complex technical information to diverse audiences. Published author and experienced presenter at international conferences. Seeking to leverage advanced research skills and technical expertise in semiconductor technology to drive innovation in industries such as aerospace, automotive, or medical devices.

### Skills

**Technical Skills:** CMOS technology, Electronic Circuit Testing, Semiconductor Physics, TCAD Simulations, Monte Carlo simulations, Radiation Effects on Electronics

**Software/Tools:** C, MATLAB, LabVIEW, TCAD Tools, GEANT4, X-ray Equipment Operation

**Analytical Skills:** Data Analysis and Interpretation, Simulation and Modeling, Troubleshooting and Problem-Solving

**Soft Skills:** Technical Communication, Project Management, Collaboration with Cross-Functional Teams

### Experience

#### European Organization for Nuclear Research (CERN)

2021 – 2024

*PhD Researcher - Radiation Effects Engineer*

- Advanced the research on radiation effects in CMOS technology, focusing on Total Ionizing Dose (TID) and displacement damage effects in ASICs for LHC particle detectors
- Managed an X-ray laboratory, conducting extensive chip qualification and testing, and training external users in radiation testing procedures
- Led TCAD simulations and performed Monte Carlo simulations (GEANT4) to analyze the effects of radiation on semiconductor devices
- Published multiple scientific papers and presented research findings at international conferences, contributing to CERN's radiation-hardened design initiatives
- Collaborated with cross-functional teams to design, test, and qualify electronics for use in extreme radiation environments, ensuring the reliability of detectors in LHC experiments.

#### European Organization for Nuclear Research (CERN)

2019 – 2020

*Technical Student*

- Conducted initial research on radiation effects in CMOS technology for the development of radiation-hardened ASICs used in the particle accelerator experiments
- X-ray lab operations, performing radiation test automated using LabVIEW and analyzing experimental data using MATLAB
- Collaborated with senior engineers on TCAD simulations of MOS transistors and gained foundational knowledge in semiconductor physics
- Delivered a strong performance, resulting in an extended contract and progression into a PhD role

### Education

**PhD in Microelectronics:** École polytechnique fédérale de Lausanne (EPFL), Lausanne, Switzerland | 2021 - 2024

**MSc in Electronics Engineering:** Università degli Studi di Napoli Federico II, Naples, Italy

**BSc in Electronics Engineering:** Università degli Studi di Napoli Federico II, Naples, Italy