Master Thesis

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DESIGN OF A RAD-HARD EFUSE TRIMMING CIRCUIT FOR BANDGAP VOLTAGE REFERENCE FOR LHC EXPERIMENTS UPGRADES

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ABSTRACT

For the Large Hadron Collider (LHC) experiments upgrade, a power distribution system based on DC/DC converters was proposed to increase the efficiency and to decrease the material budget. It is a two-stage system: the first converts the 10-12V line voltage down to 2.5V to supply voltage to optoelectronics circuits. A second stage DC/DC converter further steps down 2.5V to 1.2 and 0.9V to supply voltage to front-end analog and digital circuits respectively. Since these converters will be placed close to the proton collision point inside the experiment, they will be exposed to intense radiation and magnetic field [1]. The radiation levels are in order of 100-1000 times more than space applications.

Commercial and space-rated components are not rated for these levels of radiation, therefore, Application Specific Integrated Circuits (ASIC) have to be designed and developed, addressing radiation tolerance.

In order to generate a stable output voltage for the converters, a very precise reference voltage (for example, 300mV) is required. This reference voltage value must be independent of temperature, power supply, radiation, intrinsic technology mismatch, and process variation.

This master thesis reports the development of a radiation hard bandgap voltage reference circuit with electrical fuse (eFuse) based analog calibration in a commercial 130nm technology. This circuit will be used as the reference voltage of the first (wire-bonded on top) and the second stage converter (fully integrated in the layout).

Since the circuit has to operate in a harsh radiation environment (up to 100Mrad), the radiation-induced degradation of the devices poses major design challenges. Radiation hardness is achieved with appropriate choice of the technology, layout modifications and appropriate design.

In addition to the bandgap voltage reference with eFuse based analog calibration circuit, an over-temperature protection block was developed. Main function of this block is to disable the DC/DC converter at a high temperature level, and to enable it again after cooling down.

All the building blocks and their design methodologies are introduced in this thesis. Both simulation and measurement results after tape-out are presented and compared. Measurement results show that a rad-hard bandgap reference voltage at 300mV with an error of less than ±0.6mV was achieved by the eFuse based analog calibration.

Keywords: CMOS technology, radiation hardening, bandgap voltage reference, electrical fuses (eFuses), analog calibration.

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CHAPTER 1
INTRODUCTION

This work presented in this master's thesis was carried out in collaboration between the STI IEL ELAB of EPFL (École Polytechnique Fédérale de Lausanne) and Microelectronics section of CERN (the European Organization for Nuclear Research).

CERN is a European research organization that operates the largest particle physics laboratory in the world. Its aim is to investigate fundamental constituents of matter and their reciprocal interaction, in order to expand the frontiers of our knowledge of the fundamental laws of nature.

The main instruments required for particle physics experiments are particle accelerators and detectors. Accelerators are used to accelerate beams of charged particles up to a speed very close to the speed of light. CERN hosts the world's largest and most powerful particle accelerator, the Large Hadron Collider (LHC). It consists of a 27-km long ring and four main detectors where the counter-rotating beams can collide along the ring [2]. A detector and its infrastructure are called as an experiment. These corresponding LHC experiments are ALICE, ATLAS, CMS and LHCb (Figure 1.1). The current collision energy for protons is up to 13TeV [3].

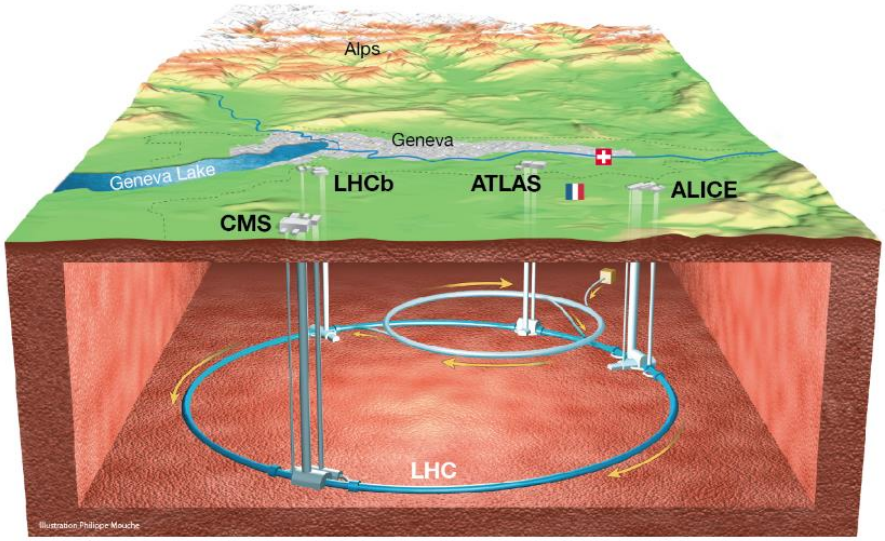

Figure 1.1: Large Hadron Collider (LHC) and the location of experiments.

The detectors in each experiment provide information about the particles produced during the collisions. The information about the position, charge, speed, mass and energy of the generated particle can be recorded via detectors. They usually consist of a large number of detecting devices that can be grouped into two main categories [4]:

1. Tracking devices detect and reconstruct the trajectories of charged particles.

2. Calorimeters measure the energy of the particles by stopping them and measuring the amount of energy released.

Trackers provide information about the identification of neutral and charged particles. With the presence of a very high magnetic field (up to 4Tesla), the trajectory of the particles is modified depending on their charges. On the other hand, calorimeters provide information about the energy of the particles. The cross-section of the biggest LHC experiment, ATLAS, is shown in Figure 1.2.

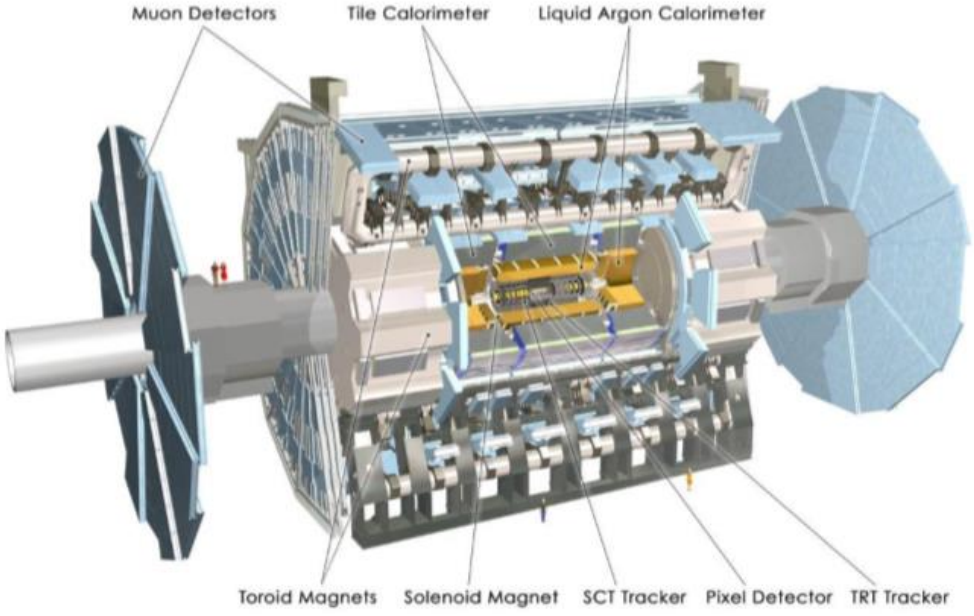

Figure 1.2: Cross-section of the ATLAS experiment.

These detectors are exposed to high level of radiation (up to some hundreds of Mrad) and high magnetic field (up to 4 T). Thus, the electronic circuits in the detectors must be radiation-tolerant, and also withstand high magnetic field.

1.1 POWER DISTRIBUTION OF THE EXPERIMENTS

The power distribution in LHC experiment has challenging requirements in terms of power needs, available cooling capability and limited material budget. Today, the front-end circuits are reached with long cables (up to 100m) that do not guarantee a stable input voltage (2-4 V) and dissipate large amount of power in heat, and increase the load on the cooling system.

The High-Luminosity LHC upgrade will increase the luminosity of the colliding beams, and this upgrade will increase the current necessary for front-end circuits, while further reducing the material budget. The cooling system and the cables comprises a large share of the material budget. Therefore, power consumption in the detectors must be reduced in order to minimize these two share of material budget. This will be achieved by using two different power domains for the front-end circuits, 1.2V for analog circuits and 0.9V for digital circuits.

To have a more efficient power distribution system for LHC Experiment upgrades, a power distribution system based on DC/DC converters was proposed [1,5]. It is a two-stage system, as shown in Figure 1.3. Firstly, the 10-12V line voltage is stepped down to 2.5V by 1st stage DC/DC converters in order to supply voltage to optoelectronic circuits. After that, two converters further step down the voltage to 1.2V and 0.9 V, the power supply voltage of front-end analog and digital circuits respectively.

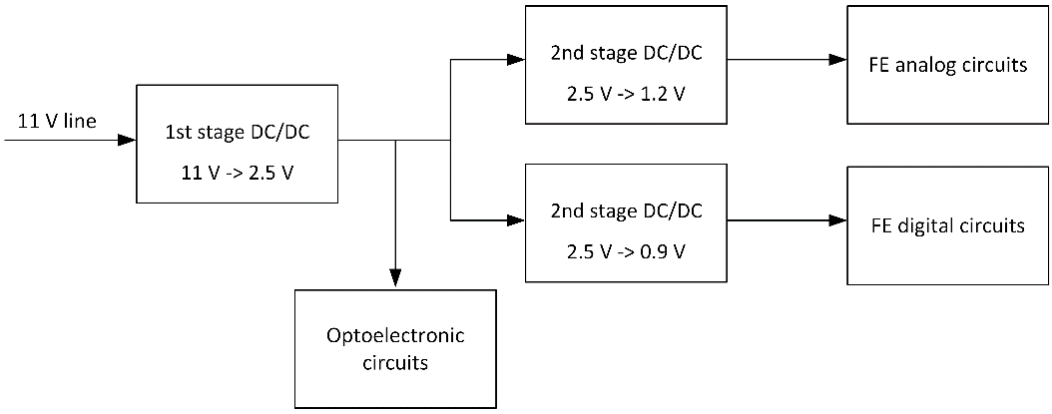

Figure 1.3: The power distribution scheme based on DC/DC converters.

The main challenge of this solution is the development of DC/DC converters that can withstand the high radiation levels up to several hundred Mrads and high magnetic field up to 4 T. Since commercial DC/DC converters do not operate in such a harsh environment, Application Specific Integrated Circuits (ASICs) have to be developed.

During my thesis work, I have took part in the design of the second stage DC/DC converter, which has been developed in a commercial 130nm technology. Radiation tolerance of the device will be explored in the following chapter.

1.2 OBJECTIVES

Considering the low material budget, (any added mass is detrimental for physics performance of the tracker) and the high efficiency requirement, the buck converter topology was used in the DC/DC converter design [5,6]. The design of buck converter is composed of two main parts, which are power stage and control section. A control loop keeps the output voltage,V_{out}, constant regardless of variation in the output load or in the input voltage as shown in Figure 1.4.

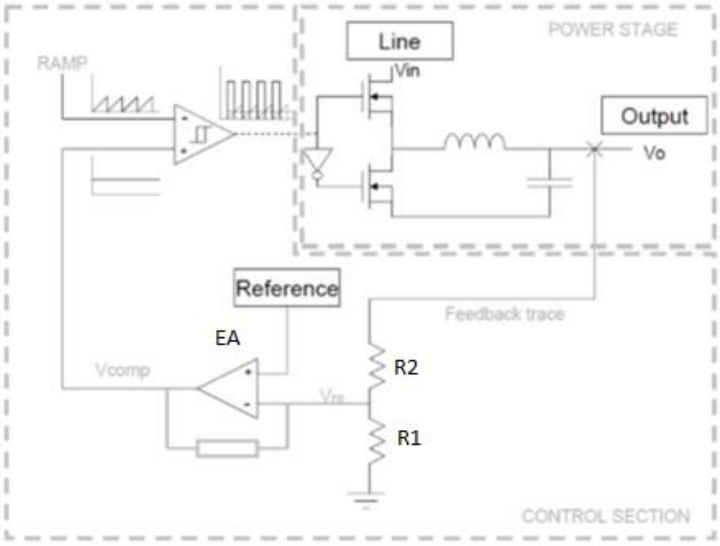

Figure 1.4: Block diagram of the DC/DC converter.

In order to have a precise output voltage, a very precise reference voltage is required. A bandgap voltage reference has been developed to provide a stable reference voltage to the Error amplifier (EA), in order to obtain an accurate output voltage. The output of the bandgap has to experience very small variations in temperature and power supply, since these changes are mirrored to the output by amplified as a factor of four (given by the voltage divider $Vout = \frac{R_1+R_2}{R_1} V_{bg} = 4V_{bg}, since\ R_1 = 333k\Omega\ and\ R_2 = 1M\Omega$).

In order to generate a precise 1.2V at the output of the 2nd stage DC/DC converter, a precise reference voltage at 300mV is necessary. The bandgap voltage reference provides a stable voltage, however due to radiation, technology mismatch and process variation, the output voltage of the bandgap has an error about ±30mV. This 30mV shift in the bandgap is mirrored to the output as 120mV, and an error of ±120mV can be observed at the output of the 2nd stage DC/DC converter.

In this work, an 8-bit radiation-hard electrical fuse (eFuse) based analog trimming circuit for the bandgap voltage reference was developed in a commercial 130nm technology to reduce the error at the output of the bandgap to less than ±0.7mV. With this analog trimming method, the maximum error at the output of the bandgap is expected as ±0.7mV and the maximum error at the output of the DC/DC converter is expected as ±2.8mV. During the manufacture, due to mismatch and process variations, all the bandgaps will be trimmed with the eFuse circuit in order to have exactly 300mV at the output of the bandgap voltage reference.

In addition to bandgap voltage reference with eFuse trimming, an over-temperature protection circuit was designed to be used in DC/DC converters. This block is to disable the DC/DC converter, if it heated up more than 100^{0}C, enable it again when the temperature decreased to 70^{0}C, with a hysteresis of about 30^{0}C. This will protect the DC/DC converter against over temperature.

CHAPTER 2
RADIATION TOLERANCE

There are different types of radiation and the effects of both charged and neutral particles on matter can be divided in two main subgroups: ionization effects and nuclear displacement. These phenomena may be caused directly by an incident particle or from a secondary event induced by it. Photons and electrons give origin to mainly ionization effects, on the other hand, neutrons that are neutral and massive particles are responsible for nuclear displacement [7].

Ionization effects essentially consist in the creation of electron-hole pairs in a semiconductor or in an insulator. The number of pairs created is proportional to the quantity of energy deposited in the material, which is expressed through the total absorbed dose. In this way, the radiation effects can be evaluated by taking into account only the energy absorbed by the material, regardless of the nature of the particle [5]. The so-called Total Ionizing Dose (TID) is the absorbed energy by radiation per unit mass of the target material and is usually expressed in rads (1 rad = 0.01J/kg).

Nuclear displacement leads to creation of Frenkel pairs that are composed of a neighboring interstitial atom and vacancy. In silicon dioxide, 90% of the Frenkel pairs recombine within a minute after the end of the irradiation at room temperature [8]. Furthermore, the used MOSFETs are characterized by a relatively high doping of the channel. Therefore, the displacement of few dopants in the channel does not considerably affect the electrical characteristics of the MOSFETs. Thus, nuclear displacement was neglected in this work.

2.1 RADIATION EFFECTS ON MOSFETS

The most sensitive part to the radiation of a MOS is the oxide layer that divides the gate from the region where channel is formed (gate oxide). When an ionizing particle goes through an MOS transistor (Figure 2.1.1), electron-hole pairs are created. These electron-hole pairs disappear quickly in the gate (metal or polysilicon) and in the substrate due to the low resistances of these materials. Conversely, in the oxide, which is an insulator, electrons and holes have different behaviors, and their mobility differs by five to twelve orders of magnitude. The mobility of electrons in SiO_2 at room temperature is typically $20 cm^2 V^{-1} s^{-1}$, while that of holes is between 10^{-4} to $10^{-11} cm^2 V^{-1} s^{-1}$ depending on temperature and electric field [9]. As a result of that, the electron-hole pairs which do not recombine are separated in the oxide by the electric field (Figure 2.1.2). Electrons can quickly escape from the gate oxide, while the holes move much more slowly towards the gate or channel, depending on the polarity of the gate voltage. For instance, in the case of a positive bias applied to the gate, the electrons drift to the gate in a very short time (order of picoseconds), while the holes move towards the $SiO_2 - Si$ interface with a very different characteristic transport phenomenon (Figure 2.1.3). Close to the interface, but still in the oxide, some of the holes may be trapped, and cause a fixed positive charge in the oxide (Figure 2.1.4). Thus, ionizing radiation also induces the creation of traps at the $SiO_2 - Si$ interface (Figure 2.1.5) [5].

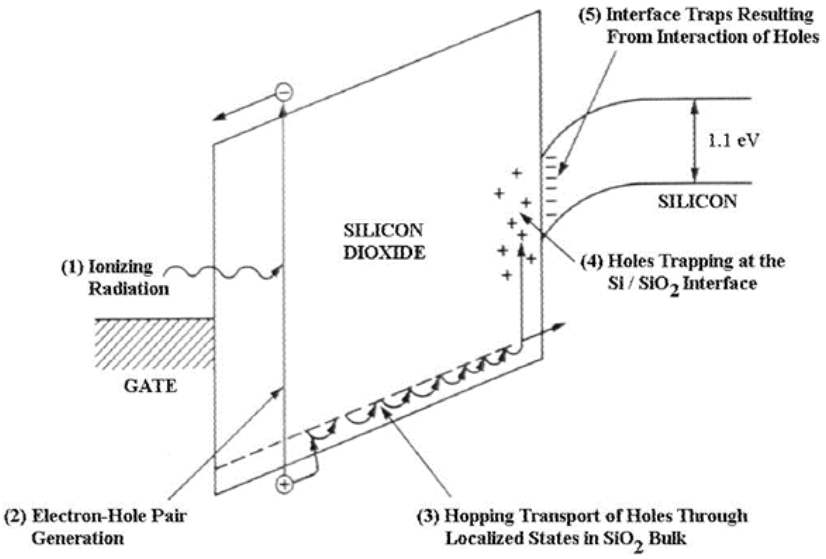

Figure 2.1: Representation of radiation effects in MOS devices. The gate is positively biased in this example.

Other critical oxides in deep submicron CMOS technologies are Shallow Trench Isolations (STIs) that isolate the single devices from each other. Similar to the gate oxide, holes can accumulate there by irradiation. It affects the conduction both in NMOS and in PMOS transistors and can also results in leakage currents between different NMOS devices [9].

2.1.2 RADIATION-INDUCED VARIATIONS OF ELECTRICAL PARAMETERS OF MOSFETS

The above-mentioned radiation effects change several electrical parameters of MOS transistors such as the threshold voltage V_{th}, the subthreshold current and the leakage current, the carrier mobility μ and the transconductance g_m. Furthermore, the positive charge accumulated in the STI can induce parasitic currents at the edges of the channel and also between adjacent devices. The shift of the electrical parameters of MOS transistors are explained in the following subsections.

2.1.2.1 THRESHOLD VOLTAGE

The threshold voltage, V_{th}, of an MOS transistor changes when the device is irradiated. The shift ΔV_{th} is given by the sum of two contributions, ΔV_{ox} and ΔV_{it}, which are related to the hole trapping in the silicon dioxide and to the charge state of the interface traps respectively.

The first contribution, ΔV_{ox}, is responsible for a shift of the flat-band voltage (voltage that must be applied to the gate to have flat energy bands inside the silicon), and therefore it gives origin to a shift in the threshold voltage. By this contribution, the absolute value of threshold voltage of NMOS transistors are decreased while the absolute value of this parameter are increased in PMOS transistors [9].

The second contribution, ΔV_{it}, introduces defect states that work as acceptor or donor-like traps finally shifting the threshold voltage. This contribution increases the absolute value of threshold voltages of both NMOS and PMOS transistors [9].

The increase of interface states slower compared to the build-up of positive charge in the oxide. Therefore, ΔV_{it} can start to play a role later than ΔV_{ox}. Therefore, the threshold voltage shift in the n-channel transistors as a function of TID is negative at the beginning, and at a later time, it can be positive due to the opposite contribution of interface traps. This phenomenon is known as rebound effect. The slower temporal evolution of the radiation-induced interface states also plays a significant role in the annealing of the irradiated transistors, because this will decrease ΔV_{ox} but will most often increase ΔV_{it} both for NMOS and PMOS transistors [5].

In addition to these effects, positive charge accumulation in the STI shifts the threshold voltage significantly in narrow channel devices. In other words, when the width of the transistor is short enough, the absolute value of threshold voltage |Vth| increases in PMOS devices and decreases in NMOS devices. This effect, which is characterized by a width-dependent threshold voltage shift, is called Radiation Induced Narrow Channel Effect (RINCE) [9,10].

2.1.2.2 SUBTHRESHOLD AND LEAKAGE CURRENTS

The leakage current (current that a transistor passes when its gate voltage is 0V) is increased in an NMOS transistor both by the decrease of the threshold voltage and subthreshold slope. In fact, it can be shown that the radiation-induced increase in the interface state density decreases the subthreshold slope [9].

The accumulated positive charge in the STI can cause lateral parasitic channels underneath the STI itself, and at the edges of an NMOS device. For this reason, two parasitic transistors are created in parallel to the original one. Since the threshold voltage, V_{th}, is proportional to the thickness of the gate oxide, t_{ox}, the V_{th} of these parasitic transistors are significantly higher than that of the device. Nevertheless, more positive charges can accumulate in the STI than in the gate oxide, due to the significantly larger thickness of the former. This results in a much larger threshold voltage shift in the parasitic transistors than in the device. At high-absorbed doses, the parasitic channels contribute more and more to the overall conduction, since their I_d-V_g curves are shifted to lower voltages more rapidly compared to the I_d-V_g curve of the device (see Figure 2.2) [9].

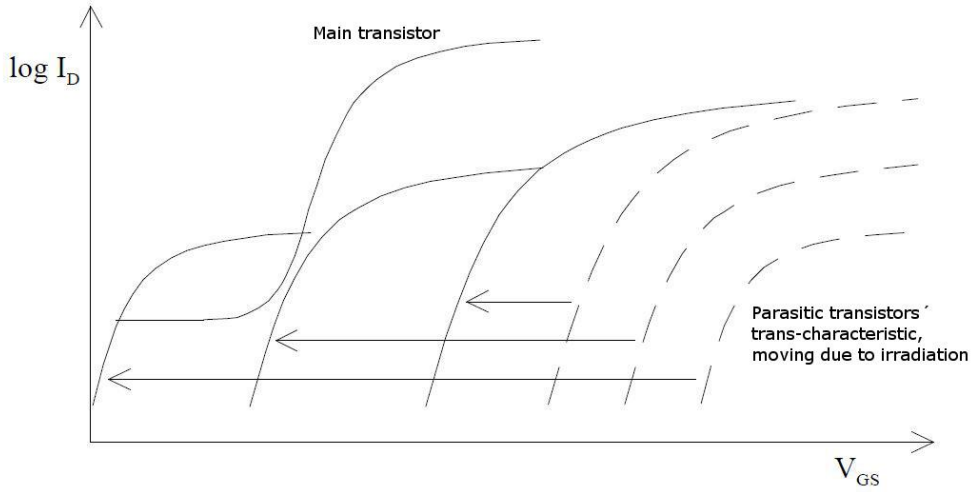

Figure 2.2: Representation of the I_d-V_g curves of the irradiated transistor and those of the parasitic transistors. At high-absorbed doses, the parasitic channels contribute more and more to the conduction, because their I_d-V_g curves shift faster to lower voltages.

Leakage currents can also be found between two n-doped diffusions of two different devices. The reason of this leakage current is again the hole trapping in the STI, which makes the conduction of negative charges underneath the oxide considerably easier. If two n-doped diffusions at different potentials are present at the edges of the STI, a parasitic transistor is created as shown in Figure 2.3. A biased line on top of the oxide further worsens the situation [7].

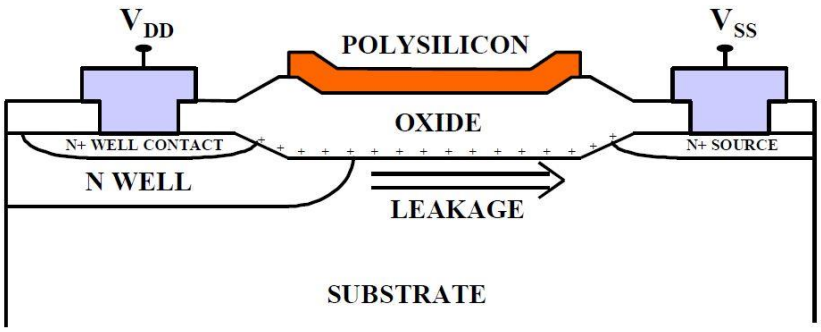

Figure 2.3: Radiation-induced leakage current between n-doped diffusions of two different devices and biased at different voltages. A biased line on top of the oxide (polysilicon) can worsen the problem.

2.1.2.3 MOBILITY AND TRANSCONDUCTANCE

A mobility degradation can be observed after irradiation, due to the increase of the interface traps, since the conduction in an MOS transistor is close to the $SiO_2 - Si$ interface. The decrease in the value of mobility causes a drop in the device's transconductance [5].

2.2 RADIATION EFFECTS ON DIODES

The forward characteristic of diodes is affected by radiation as shown in Figure 2.4. Especially, the dominant effect of radiation on diodes is the increase in the leakage current. Similar to MOS devices, parasitic channels are created at the periphery of the device. The impact of this radiation-induced leakage is effective for low values of forward voltage, while for larger voltage values it is negligible compared to the diode current. To ensure their stability under irradiation, large current densities are required for diodes. However, this is harmful for the power consumption of the circuits that use diodes, such as bandgap voltage references [9].

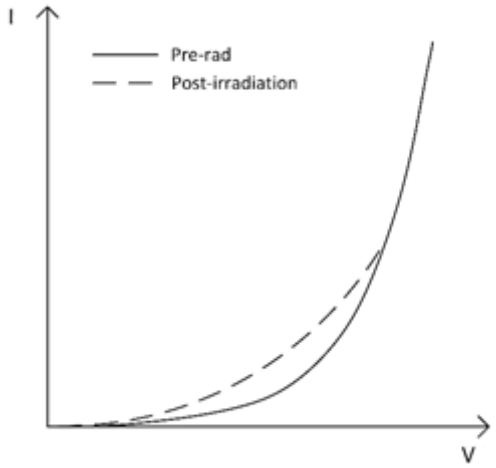

Figure 2.4: Representation of the I-V curve of diodes before and after irradiation.

2.3 SINGLE EVENT EFFECTS (SEE)

Single Event Effects (SEE) are resulted from high-energy particles passing through an integrating circuit, and this can result in a malfunction of one or more transistors. These effects are divided into two as soft errors and hard errors. If the errors are reversible, they are called as soft errors and if the errors are non-reversible, they are called as hard errors.

There are different kinds of SEE, however most of them are negligible when CMOS deep submicron technologies are used. In this work, only the so-called Single Event Upset (SEU) and Single Event Latch-Up (SEL) have been considered, because they have the most significant impact on circuits designed with the chosen technology.

2.3.1 SINGLE EVENT UPSET (SEU)

An SEU is the instantaneous reversible modification of the logic state of a logic cell, when an incoming particle generates charge in a sensitive node of the logic cell. Since it leads to reversible changes, it only causes soft errors. This kind of problem has usually more impact on digital circuits, since it can change the logic state.

Critical charge is a very convenient measure of circuit robustness to SEU and can be obtained by simulation. The amount of energy deposited by a charged particle per unit length can be expressed in

terms of linear energy transfer (LET) in units of $MeVcm^2mg^{-1}$. In order to estimate the maximum LET in the LHC experiment upgrades, we assume that the worst event generated by nuclear interaction is fission of the tungsten used in tiny amounts in the metallization stack in the ASIC. This extremely rare event might generate fragments with LET up to 40 $MeVcm^2mg^{-1}$ [5].

2.3.2 SINGLE EVENT LATCH-UP (SEL)

When a Latch-Up occurs, a parasitic PNPN structure called thyristor is switched on, and a current starts flowing between the two power lines (Figure 2.5). This leads to the permanent failure of the entire device, if the latch-up current is not promptly interrupted. Thus, it is a hard-error. The latch-up can occur only if the two parasitic bipolar transistors that form the thyristor are both forward biased and if the product of the gains of the two transistors is larger than 1 [9].

A high-energy particle can results in a latch-up by creating electron-hole pairs, whose flow can result in a current that switches on the parasitic thyristor.

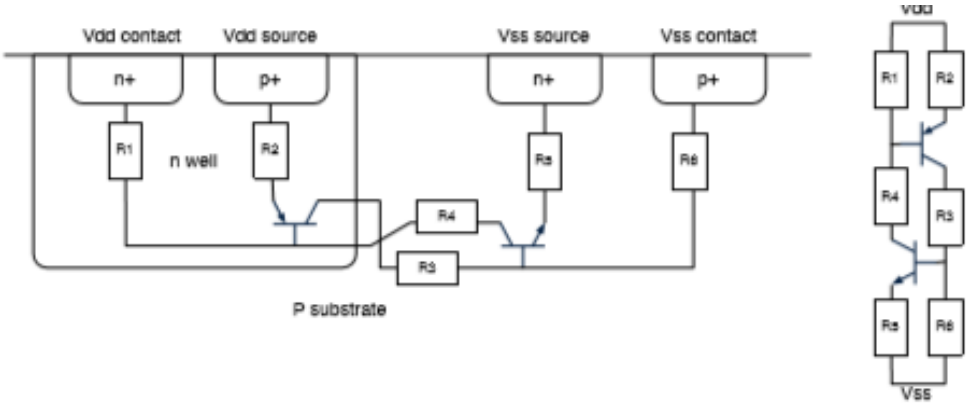

Figure 2.5: Parasitic thyristor in CMOS can be destructive due to Single Event Latch-Up.

2.4 RADIATION HARDENING TECHNIQUES

There are three possible methods that can improve radiation tolerance of a CMOS IC:

1. Hardening by process: acting on the process and modification of some technological parameters in order to achieve high radiation tolerance. This technique cannot be implemented in this work, because a commercial technology and MPW (Multi Process Wafer) run were used.
2. Hardening by design: use of special layout techniques to improve radiation tolerance of the circuit. These techniques are used in this presented work.
3. Hardening by circuit and system architecture: studying special circuit architectures, which are less sensitive to the shifts in the device characteristics due to irradiation or to the charges generated in the circuit. For instance, some of these techniques are used in this work to prevent SEE.

In this work, 2nd and 3rd methods are applied, because a commercial technology is used, and thus the process cannot be modified.

2.4.1 HARDENING BY DESIGN

In the used technology, all NMOS transistors (core, rated 1.2V and I/O, rated 2.5V) suffer from leakage current due to the presence of the STI on the transistor's edges. As a countermeasure, Enclosed Layout Transistors (ELTs) are used for all NMOS transistors because there is no more STI between source and drain, only gate oxide.

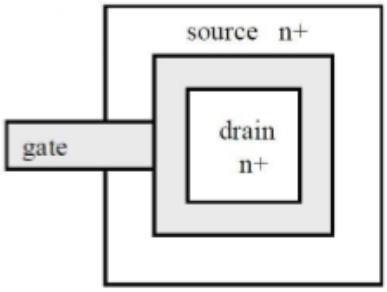

Figure 2.6: Representation of Enclosed Layout Transistor (ELT).

However, the use of ELT geometry has some drawbacks compared to traditional layout:

- It has larger area and lower density compared to traditional layout of transistors.
- It has larger gate to source or to drain capacitances, depending on whether the drain or source is internal (minimum capacitance). The device is therefore no more symmetric.
- There are restrictions on the choice of the W/L ratio. Due to the layout of the ELTs, W/L ratio cannot be smaller than about four when the minimum possible L is selected. The minimum achievable W/L ratio becomes lower when L is increased. Therefore, an arbitrary size of transistor cannot be selected compared to traditional layout of a standard self-aligned transistor.

In addition to the parasitic path between drain and source of NMOS devices, irradiation creates also a parasitic path between different n+ diffusions or nwells at different potential. To prevent parasitic currents between different n-doped diffusions, p+ guard rings have to be used to cut off the possible leakage paths below the STI. Figure 2.7 shows the guard ring to remove the parasitic paths between two ELT transistors having different source voltages. The disadvantage is the increased area.

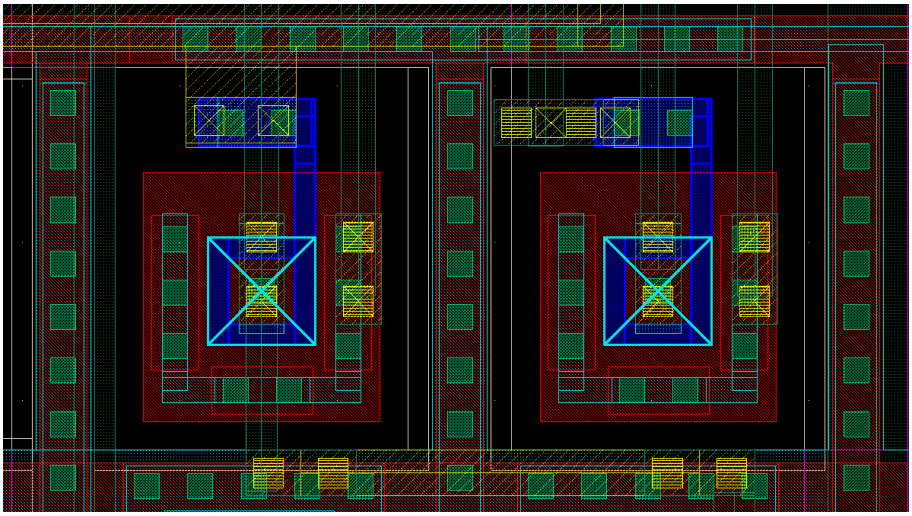

Figure 2.7: Example of guard ring to remove the parasitic paths between devices having different source voltages.

Specific layout techniques are applied to avoid SEE. With regard to SEL, several methods are adopted as follows [5,9]:

1. A deep n-well (low resistance) was added to the n-well in order to decrease the resistance R1 in the parasitic thyristor (Figure 2.5). When an incoming particle generates a radiation-induced current in the n-well, the base-emitter voltage of the parasitic PNP bipolar will be lower and it will be more difficult to switch on the parasitic thyristor.
2. A large amount of n-well and substrate contacts was used to lower the resistances R1 and R6. Switching on of the parasitic thyristor becomes much more difficult.
3. Both NMOS and PMOS devices were enclosed by guard rings. P+ guard rings reduce the gain of the parasitic NPN bipolar transistor, introducing a highly doped region in the base and keeping the base tight to ground. N+ guard rings reduce the gain of PNP transistor and keeping the base tight to Vdd voltage.

Concerning the SEU, large capacitances were added to the most sensitive nodes to minimize the effect of the current injections.

2.4.2 HARDENING BY CIRCUIT AND SYSTEM ARCHITECTURE

This work was developed by using a commercial 130nm CMOS technology. Several modifications were made to MOSFET models to simulate the TID effects on circuit. The modelling of the behaviour of the irradiated devices was carried out for:

1. High voltage (I/O, rated 2.5V) PMOS transistors at TID = 100 Mrad,
2. Low voltage (core, rated 1.2V) NMOS and PMOS transistors at TID =100Mrad and 400Mrad.

In this work, models of both I/O and core devices with a TID of 100Mrad are used. An effective modelling of the behaviour of irradiated I/O NMOS transistor could not be achieved, however it is observed that the leakage current due to irradiation is minimized by using ELTs in I/O NMOS devices.

Compared the I/O transistors, core transistors are more radiation tolerant, since high voltage devices have a thicker oxide, and the ionization can occur in larger region.

One of the effects of TID on CMOS devices is the trapping of positive charges in the STI. This effect can change the effective width of the transistors, which occurs especially in PMOS devices as a significant degradation in narrow channel devices (Radiation Induced Narrow Channel Effect - RINCE [10]). In PMOS transistors, the positive charges trapped in the STI due to irradiation attracts the electrons on the channel to the edge of the channel and prevent channel inversion in that region thereby reducing the available channel width. This effect is more evident in narrow channel devices, and it shows a larger decrease of the on current I_{on} with TID.

In the BSIM model (Berkeley short-channel IGFET model for MOS transistors), the effective width W_{eff} is expressed as [11]:

$$W_{eff} = W_{drawn} - 2dW \tag{2.2}$$

For a particular type of devices that has absorbed a specific dose, the parameter dW in PMOS transistors was shifted by a positive quantity, regardless of nominal channel width and length. The width shift of the PMOS transistors can be seen in Table 2.1. In order to minimize the radiation induced narrow channel effect on PMOS devices, the minimum width of the PMOS devices was selected as 2μm in this design.

PMOS I/O – 100Mrad	PMOS core – 100Mrad	PMOS core – 400Mrad
2dW = 95nm	2dW = 20nm	2dW = 55nm

Table 2.1: Shift in the effective width used for I/O and core PMOS transistors at given TID values.

Concerning the SEU, specific techniques are used to minimize radiation-induced effects. A common radiation hardening technique employed in digital circuits is the physical triplication. For instance, each memory element is instantiated three times and an output voting cell takes the decision by selecting the logical value stored by at least two of the three memory cells. In case a fault occurs in one of the three blocks due to SEU, it will be masked by the voting cell and not be seen at the output. Furthermore, some circuit architectures based on rewriting the information lost in case of a memory are used. For instance, if the output of one of the triplicated memory elements becomes different from other two due to SEU, then the data will be rewritten to the memory cells.

CHAPTER 3
BANDGAP VOLTAGE REFERENCE

A bandgap voltage reference is a temperature, power supply, radiation-independent voltage reference circuit. The shifts at the output of the bandgap are mirrored to the output of the DC/DC converter as a factor of four. Furthermore, due to process and mismatch variation, the bandgap voltage may exhibit less than ±10% wafer to wafer, inter-die or intra-die variation. For instance, the bandgap reference voltage in this application is 300mV, and may have a maximum error of about ±30mV due to process variation, radiation and mismatch. To correct this error, resistors and switches connected in parallel are added to the output of the bandgap to trim the reference voltage. At the end, we intend to decrease this error to less than ±0.7mV.

In the proposed bandgap voltage reference, similar principles to Brokaw cell is used to obtain an output voltage whose temperature behaviour is corrected at first order. In the Brokaw bandgap reference, the circuit maintains an internal voltage source that has a positive temperature coefficient, and another internal voltage source that has a negative temperature coefficient. It employs two bipolar transistors, so that base-emitter voltage for each transistor has a negative temperature coefficient and the difference between the two base-emitter voltages has a positive temperature coefficient. The output is the sum of the base-emitter voltage difference with one of the base-emitter voltages. With proper component choices, two opposing temperature coefficients cancels each other and the output becomes temperature independent [12].

The bipolar transistors or diodes are affected strongly by radiation, therefore it is not convenient to use BJTs or diodes in this rad-hard application. Figure 3.1 shows that the measurements of the I_d-V_d characteristics of the irradiated diodes showed a strong radiation-induced leakage current. A current of at least some tens of μA must flow through the device in order to ensure the stability in radiation environment and leads to high current consumption.

In this work, use of n-type Dynamic Threshold MOSFETs (DTMOS) was proposed. In such devices, the gate is tied to the drain and to the bulk. Thus, the threshold changes according to the value of the gate voltage due to the Body effect. Another important result of the configuration is that DTMOS devices in weak inversion (WI) have an ideal subthreshold slope of 60mV/decade [13, 14]. They show same exponential trans-characteristic behaviour with BJTs and diodes in WI [9,15]. In contrast to bipolar transistors, core n-type DTMOS shows an excellent characteristics in terms of radiation tolerance, even at low currents (Figure 3.2). Therefore, DTMOS transistors can be used instead of bipolar transistors.

In this work, core DTMOS transistors are used, since they are not supposed to withstand for high voltage and since the core transistors have improved radiation tolerance compared to I/O transistors.

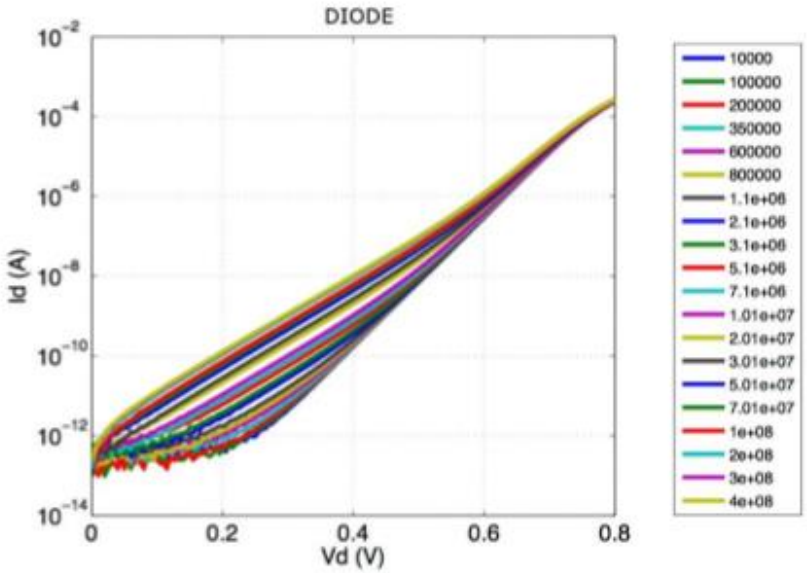

Figure 3.1: Characteristic of a diode irradiated up to different values of TID[rad]. The leakage current significantly increases with TID.

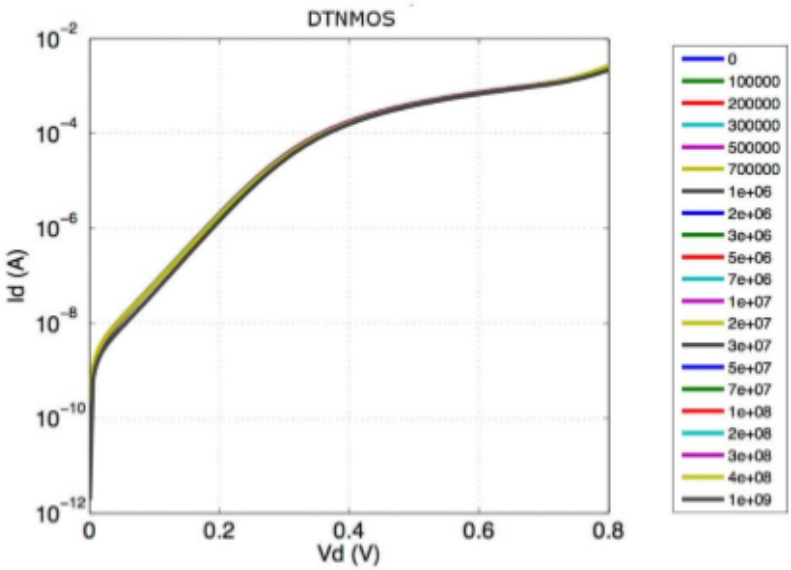

Figure 3.2: I_d –V_d curve of an n-type DTMOS irradiated up to different values of TID[rad]. No significant radiation-induced change due to TID was observed.

3.1 WORKING PRINCIPLE

The voltages of transistors are referred to their bulks, thus $V_g = 0V$ and $V_d = 0V$ for a DTMOS. For the weak inversion,

$$V_s > V_p \tag{3.1},$$

$$V_g - n.V_s < V_{t0} \tag{3.2}.$$

Since $V_g = 0$ and V_{t0} is positive for n-channel devices, this DTMOS operates in weak inversion (WI). In WI, its drain current can be written as:

$$I_d = I_s e^{\frac{-nV_s - V_t(V_{ds})}{nU_T}} = I_s e^{\frac{nV_{ds} - V_t(V_{ds})}{nU_T}} = I_S e^{-\frac{V_t(V_{ds})}{nU_T}} . e^{\frac{V_{ds}}{U_T}} \tag{3.3},$$

where $U_T = \frac{k_b T}{q}$ is the thermal voltage and $I_s = 2n\mu C_{ox}\left(\frac{W}{L}\right) {U_T}^2$ is the specific current of the transistor.

From the equation 3.3, V_{ds} can be written as:

$$V_{ds} = U_T \ln\frac{I_d}{I_s} + \frac{V_t(V_{ds})}{n} \tag{3.4}.$$

The V_{ds} of the MOS transistors typically decreases with temperature. This drop in V_{ds} with rising temperature can be easily observed in simulations. Expressing V_{ds} using a series expression:

$$V_{ds} = V_{ds0} - \lambda T + f(T) \tag{3.5},$$

in which V_{ds0} is the value of V_{ds} at T = 0 Kelvin and λ is a positive coefficient. Since the linear term is dominant compared to higher-order terms, the voltage across a DTMOS is Complementary to Absolute Temperature, CTAT. In order to obtain a constant voltage with temperature, an additional Proportional to Absolute Temperature (PTAT) voltage has to be obtained. A PTAT voltage can be obtained by subtracting the V_{ds} of two DTMOS devices:

$$\Delta V_{ds} = V_{dsM1} - V_{dsM2} = \left(U_T \ln\frac{I_{dM1}}{I_{sM1}} + \frac{V_{tM1}(V_{dsM1})}{n}\right) - \left(U_T \ln\frac{I_{dM2}}{I_{sM2}} + \frac{V_{tM2}(V_{dsM2})}{n}\right)$$

$$= U_T \ln\left(\frac{I_{dM1}\left(\frac{W_{M2}}{L_{M2}}\right)}{I_{dM2}\left(\frac{W_{M1}}{L_{M1}}\right)}\right) + \frac{V_{tM1}(V_{dsM1}) - V_{tM2}(V_{dsM2})}{n} \tag{3.6}.$$

The threshold voltages of the DTMOS transistors have almost the same behaviour with temperature; therefore we can neglect the effect of the difference between the two threshold voltages on ΔV_{ds}.

The proposed bandgap voltage reference, shown in Figure 3.3, achieves a first order correction of the behaviour of the current in temperature. This first order correction is obtained by adding a PTAT current to a CTAT current, in order to have a temperature-independent current.

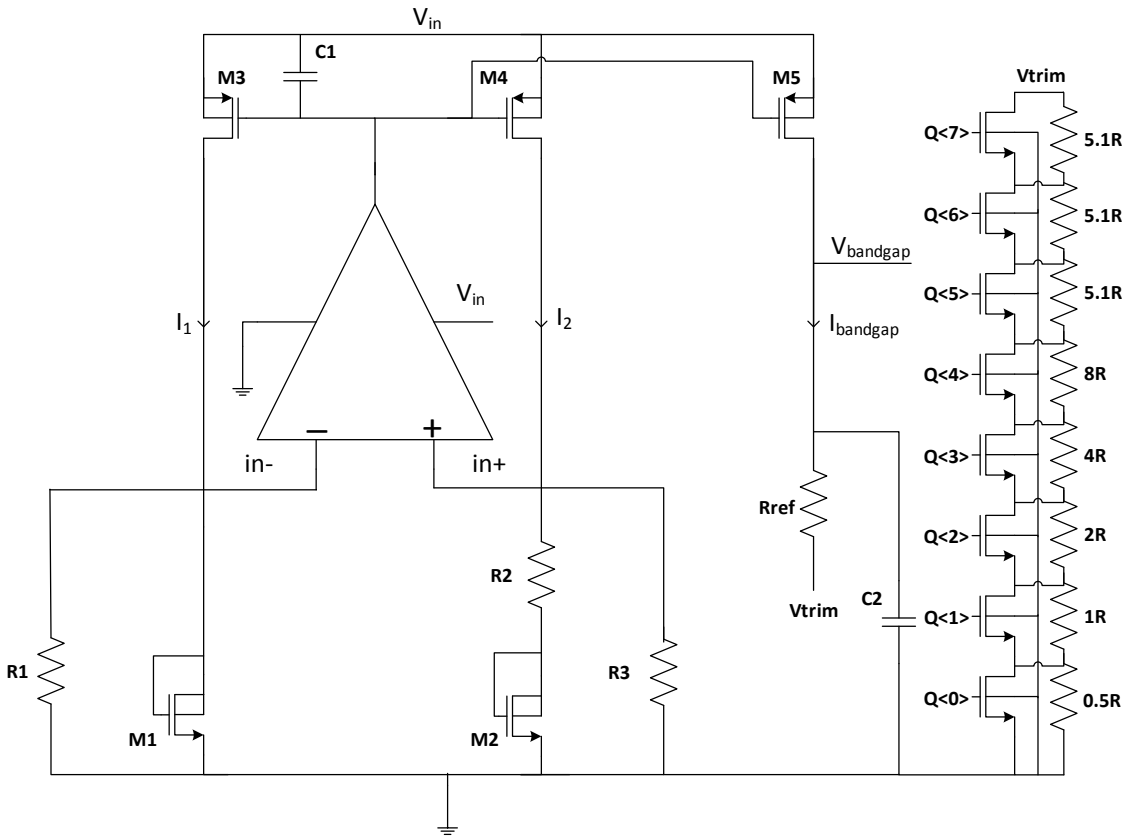

Figure 3.3: Schematic of the designed bandgap voltage reference.

The amplifier can be assumed as ideal:

$$in_{-} = in_{+} = V_{dsM1} = V_{ds0M1} - \lambda T + f(T) \tag{3.7}$$

Since V_{ds} of DTMOS is CTAT, the CTAT current can be generated by the resistance R_3:

$$I_{CTAT} = \frac{in_{+}}{R_3} \tag{3.8}$$

On the other hand, the voltage drop across R_2 is PTAT, since the difference between two V_{ds} voltages is PTAT. Therefore, the resistance R_2 generates the PTAT current:

$$V_{R2} = in_{+} - V_{dsM2} = V_{dsM1} - V_{dsM2} = U_T \ln\left(\frac{I_{dM1}\left(\frac{W_{M2}}{L_{M2}}\right)}{I_{dM2}\left(\frac{W_{M1}}{L_{M1}}\right)}\right) \tag{3.9}$$

$$I_{PTAT} = \frac{V_{R2}}{R_2} \tag{3.10}$$

Summing up the two currents in order to have temperature independent current:

$$I_2 = I_{CTAT} + I_{PTAT}$$

$$= \frac{V_{ds0M1}}{R_3} - \frac{\lambda T}{R_3} + \frac{f(T)}{R_3} + \frac{U_T}{R_2}\ln\left(\frac{I_{dM1}\left(\frac{W_{M2}}{L_{M2}}\right)}{I_{dM2}\left(\frac{W_{M1}}{L_{M1}}\right)}\right)$$

$$= I_0 + \left(\frac{k_b}{qR_2} \ln \left(\frac{I_{dM1} \left(\frac{W_{M2}}{L_{M2}} \right)}{I_{dM2} \left(\frac{W_{M1}}{L_{M1}} \right)} \right) - \frac{\lambda}{R_3} \right) T + \frac{f(T)}{R_3} \quad (3.11).$$

Higher order terms, which are shown by $f(T)$ can be neglected. In order to have temperature independent current:

$$\left(\frac{k_b}{qR_2} \ln \left(\frac{I_{dM1} \left(\frac{W_{M2}}{L_{M2}} \right)}{I_{dM2} \left(\frac{W_{M1}}{L_{M1}} \right)} \right) - \frac{\lambda}{R_3} \right) = 0 \quad (3.12).$$

The ratio $\frac{I_{dM1}}{I_{dM2}}$ is fixed by the PMOS current mirror. The current I_1 that flows in the left branch is linked to the current I_2, which flows in the right branch:

$$I_1 = \frac{\frac{W_{M3}}{L_{M3}}}{\frac{W_{M4}}{L_{M4}}} = kI_2 \quad (3.13).$$

The resistance $R_3 = kR_1$ in order to have $I_{dM1} = kI_{dM2}$. Since $R_3 = kR_1$, $I_{R1} = kI_{R3}$. Consequently:

$$I_{dM1} = I_1 - I_{R1} = k(I_2 - I_{R3}) = kI_{dM2} \quad (3.14).$$

As a result, a first order compensation is obtained if $R_2, R_3, M1, M2$ and k are sized so that:

$$\frac{k_b}{qR_2} \ln \left(k \frac{\left(\frac{W_{M2}}{L_{M2}} \right)}{\left(\frac{W_{M1}}{L_{M1}} \right)} \right) = \frac{\lambda}{R_3} \quad (3.15).$$

In this design, we decided to set $k = \frac{\frac{W_{M2}}{L_{M2}}}{\frac{W_{M1}}{L_{M1}}} = 8$. The current I_{R2} which is I_{PTAT} can be calculated by applying the equations 3.9 and 3.10. The resistance R_2 is chosen as 200kΩ and since $I_{dM1} = kI_{dM2} = kI_{R2}$. Thus, $I_{dM1} = 4.32\mu A$.

The behaviour of the DTMOS in temperature shows that $\lambda \approx 0.28\, mV/K$ [9]. Since the value of R_2 was already selected as 200kΩ, the value of R_3 is calculated from the equation 3.15, $R_3 = 156k\Omega$. Since $R_3 = kR_1$, $R_1 = 19.5k\Omega$.

Lastly, the operating point of the amplifier $in_+ = in_-$ is calculated from the equation 3.4. The $\frac{W_{M1}}{L_{M1}}$ is selected as 3.6 considering the available ELT transistors. Then, the operating point is calculated as $in_+ = in_- \approx 302mV$.

After all the resistor and $\frac{W}{L}$ ratio of the transistors have been calculated, some simulations were performed to achieve the best bandgap performance. After some iterations, the parameters were chosen as:

$$R_1 = 22.25k\Omega, R_2 = 201k\Omega, R_3 = 178k\Omega,$$

$$\frac{W_{M1}}{L_{M1}} = 3.6, \frac{W_{M2}}{L_{M2}} = 8 \times 3.6, \frac{W_{M4}}{L_{M4}} = \frac{W_{M5}}{L_{M5}} = 3.3, \frac{W_{M3}}{L_{M3}} = 8 \times 3.3.$$

The current in the left branch $I_1 = 20\mu A$ and the current in the right branch $I_2 = 2.5\mu A$. Since the current flowing through the third branch, $I_{bandgap}$, is also $2.5\mu A$, the total current consumption of the bandgap voltage reference is $25\mu A$.

In order to improve power supply rejection ratio, PSRR, the capacitance C_1 was added to the gate of the PMOS current mirror. It ensures that the gate of the current mirror follows the oscillations of the input voltage. Additionally, the capacitance C_2 was added to eliminate the single event effects (SEE) caused by sudden current injections in the output node.

3.2 TRIMMING OF THE BANDGAP REFERENCE VOLTAGE

The temperature independent current I_2 is mirrored to the third branch as $I_{bandgap}$by the transistor M5 and generates the bandgap voltage by flowing through the reference resistor R_{ref}. However, the bandgap voltage (300mV in this application) can experience an error up to ±30mV due to mismatch and process variation. Therefore, eight resistors and eight switches connected in parallel are added to the R_{ref} in order to trim output voltage after the chip has been manufactured. For the switches, wide NMOS transistors are used to have small parasitic resistors less than 20Ω. For the switching NMOS transistors, W=320µm and L=0.13µm. Since the gate of the switches experiences a high capacitance, the gate voltages of the switches are insensitive to SEEs.

The resistance values and gate voltages of the switches are arranged so that in nominal corner, Q<7>, Q<6> and Q<5> are set to logic-low and others are set to logic high. Thus, fifth, sixth and seventh switches are off, and the three resistances with the values of 5.1R are added to R_{ref}.

The first five resistors are binary coded, and the values of other three resistors are set to the sum of the binary coded resistors over three. The binary coding is applied only for first five resistors. If it would be applied to all the resistors, the most significant resistor would be much larger than others and in case of a single event, the bandgap voltage might be much lower or much higher than 300mV. In this configuration, the largest resistor is 8R, and its effect due to SEU is less than 25mV, to have an error less than 0.1V at the output of the DC/DC converter.

In order to have a precision of ±0.7mV, the voltage shift due to change in less significant bit (LSB) resistor must be 1.4mV. However, the parasitic resistances of the switches and connection lines may affect this voltage shift. Thus, the precision of the bandgap is selected as ±0.6mV and the effect of the LSB resistor is selected as 1.2mV in order to have a safety factor.

Table 3.1 lists the voltage shift of the bandgap voltage after the selected bit was inverted. As can be seen, the most significant 3 bits are to decrease and the others are to increase the bandgap reference voltage. It also shows that, the error on the bandgap voltage less than ±36mV can be trimmed with an error of less than ±0.7mV. Additionally, the effect of the largest resistance (8R) in case of an SEU is 19.2mV, which is less than 25mV.

Bit to Program	Output Voltage (Q) (before/after)	Voltage Change of BGP
7^{th}	0 → 1	-12.24mV
6^{th}	0 → 1	-12.24mV
5^{th}	0 → 1	-12.24mV
4^{th}	1 → 0	+19.2mV
3^{rd}	1 → 0	+9.6mV
2^{nd}	1 → 0	+4.8mV
1^{st}	1 → 0	+2.4mV
0^{th}	1 → 0	+1.2mV

Table 3.1: Calculated results - The shift of the bandgap reference voltage after the selected bit was inverted.

3.3 SIMULATION RESULTS

Figure 3.4 shows the simulated behaviour of the bandgap reference voltage with temperature. The voltage shift with temperature is approximately -7.2mV from -30°C to 100°C. At a voltage drop in Vin (VddCORE) from 1.2V to 0.9V, the shift in the bandgap voltage is less than 0.5mV.

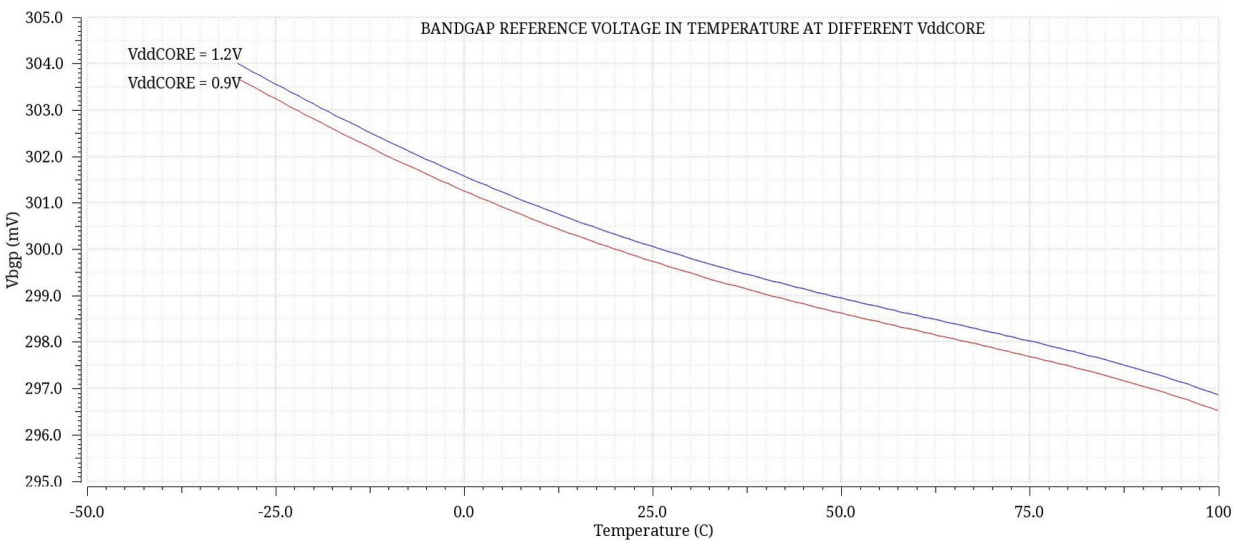

Figure 3.4: Simulated behaviour of bandgap reference voltage in temperature at two different power supply voltage.

The power supply rejection ratio (PSRR) should be higher than 40dB for this application, and the DC value of PSRR decreases significantly when the value of Vin (VddCORE) is reduced. As shown in Figure 3.5, the PSRR of the circuit is acceptable, being never lower than 40dB in absolute value, even if Vin (VddCORE) is only 0.9V.

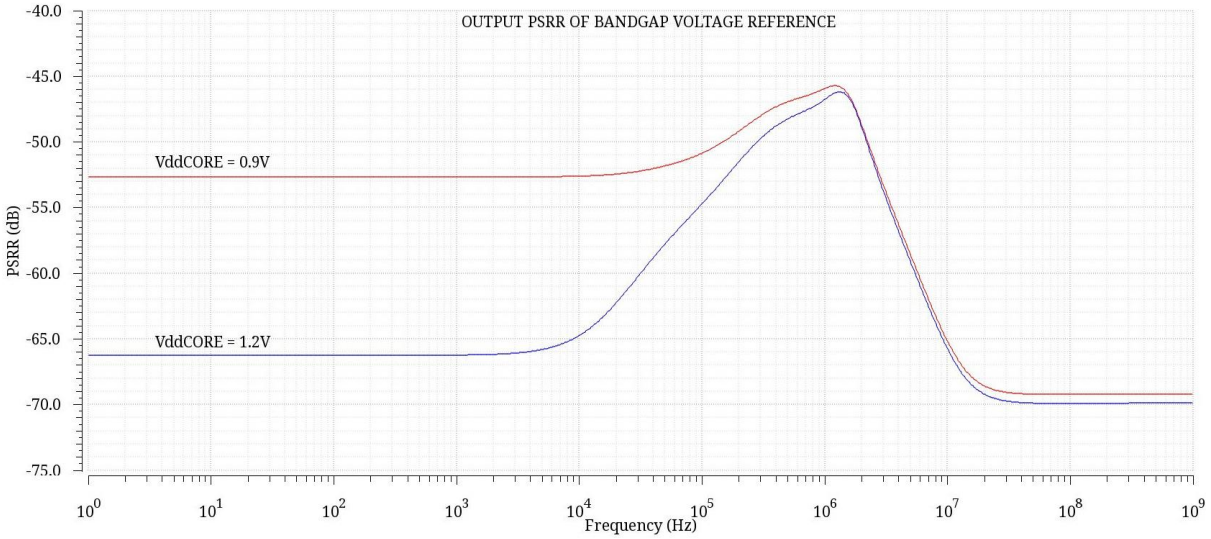

Figure 3.5: Simulated behaviour of the output PSRR at two different power supply voltage.

Process corner simulations of the bandgap voltage reference were performed. These simulations include process corners for both active and passive devices, and also radiation-induced effects for a TID of 100Mrad. Figure 3.6 shows the bandgap reference voltage with temperature at different radiation and process corners. The bandgap voltage varies with different corners by less than ±30mV. The main reason of the voltage shift in V_{bgp} is that the process variation in the threshold voltages of DTMOS transistors shifts the value of I_0 in Equation 3.11. Even resistors experiences a very strong process variation, they do not lead to a shift in I_2, because in the expression of I_2, only ratios of the resistances are present. Since the value of I_0 shifts due to radiation and process variation, the value of bandgap reference voltage changes. In order to eliminate this voltage shift, eight trimming resistors with switches were employed.

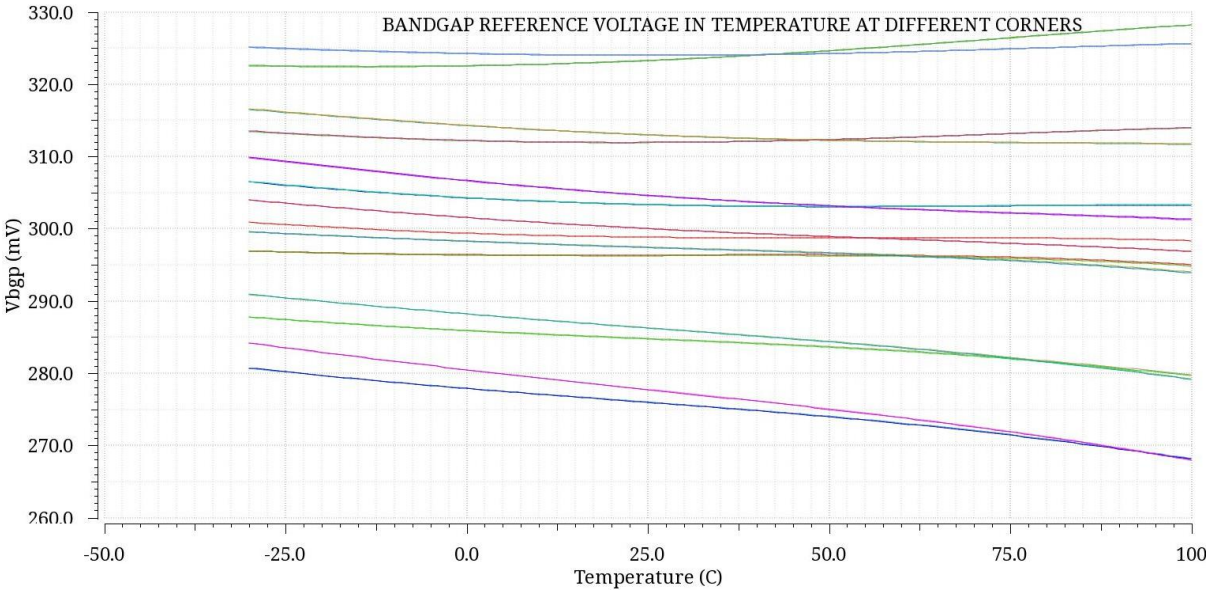

Figure 3.6: Simulated behaviour of the bandgap reference voltage with temperature at different corners. Process corners for both active and passive devices, as well as radiation-induced effects were included in the corner simulations.

In addition to process corner simulations, Monte Carlo simulations were carried out to observe the effect of mismatch. 200 runs were performed at room temperature and at Vin (VddCORE) = 1.2V. Figure 3.7 shows that maximum shift in the bandgap voltage is less than ±20mV, which is in the range of trimming resistors. Main causes of these variations are the input offset of the amplifier, the mismatch between the DTMOS devices and in the PMOS current mirror.

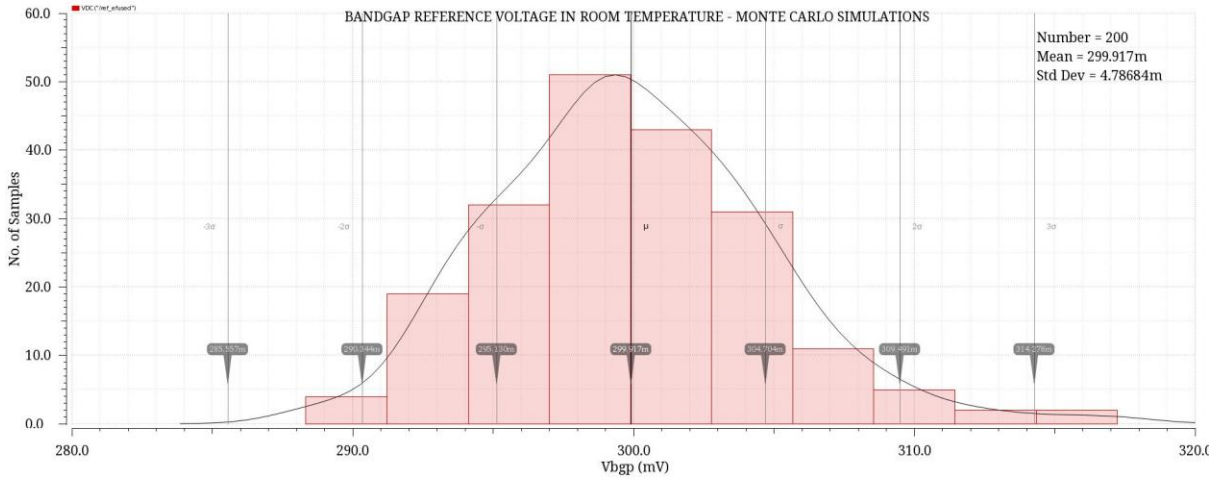

Figure 3.7: Variation of the bandgap reference voltage due to mismatch, as simulated by Monte Carlo Simulations (200 runs at room temperature and Vin(VddCORE) = 1.2V). Its mean is 299.9mV and standard deviation is 4.79mV.

Finally, the shift of the bandgap voltage after inverting of the selected bit is simulated. Table 3.1 lists the calculated results, and shows that the calibration circuit has a range of about ±36mV and a precision of ±0.6mV. Table 3.2 lists the simulation results of the calibration circuit. Simulations were performed at room temperature in order to determine the voltage change after inverting the selected bit. At higher and lower temperatures, very small variations might be observed, however the purpose of the circuit is to have 300mV at room temperature. To invert the selected bit, the eFuse cell that is connected to this switch will be programmed.

Bit to Program	Output Voltage (Q) (before/after)	Voltage Change of BGP
7^{th}	0 → 1	-12.28mV
6^{th}	0 → 1	-12.32mV
5^{th}	0 → 1	-12.34mV
4^{th}	1 → 0	+19.27mV
3^{rd}	1 → 0	+9.73mV
2^{nd}	1 → 0	+4.89mV
1^{st}	1 → 0	+2.49mV
0^{th}	1 → 0	+1.25mV

Table 3.2: Simulation results - The shift of the bandgap reference voltage after the selected bit was inverted.

According to simulation results, the range of the circuit increased to ±37mV and the precision of the calibration circuit became ±0.63mV. These results are fine for this application, since the maximum voltage shift due to mismatch, radiation and process variation is ±30mV and the objective precision is better than ±0.7mV. The main reason of the difference between calculated and simulated results is that switches and metal lines add some parasitic resistances to the bandgap branch.

3.4 LAYOUT

The layout of the bandgap voltage reference block can be seen in Figure 3.8. The area of this block is 593.285µm×205.0µm. The width and length of the bandgap block was determined depending on the free area in the top-level chip of the DC/DC converter. The main area consuming parts of this block are capacitors, which are used as compensation capacitor of the amplifier, C_{comp}, to improve the PSRR of the block, C1, and to have a SEU proven output voltage, C2. For all the capacitances in this block, MOM capacitors with 4 layers (Metal 1 to Metal 4) are used and their capacitance per unit area is about $0.88 fF/\mu m^2$.

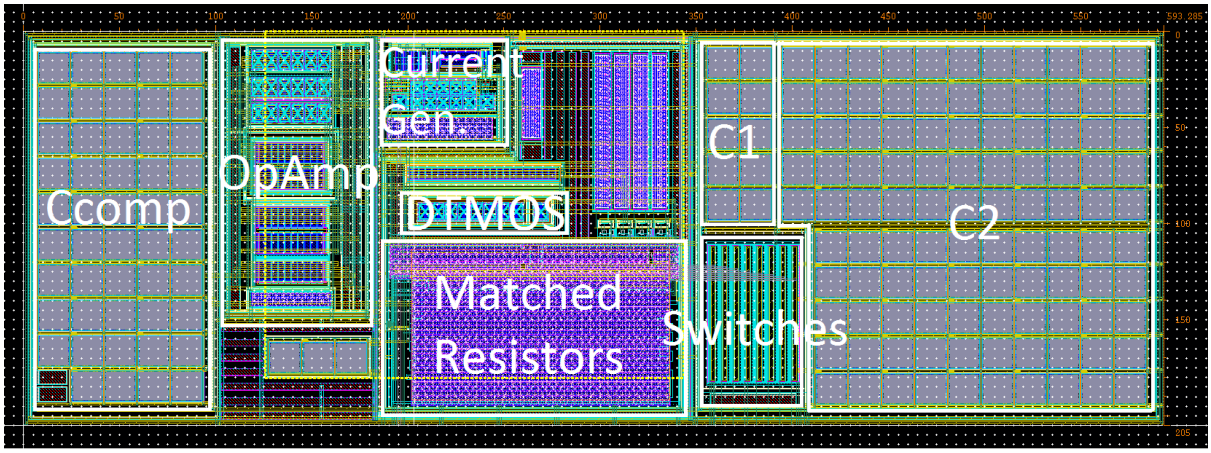

Figure 3.8: Layout of the bandgap voltage reference.

CHAPTER 4
ELECTRICALLY PROGRAMMABLE FUSE (EFUSE)

An electrical fuse (eFuse) cell is a one-time programmable macro cell that can be used as chip ID, memory redundancy implementation, security code, configuration setting, or for analog circuit trimming [16]. The eFuse component used in this work is a silicided-polysilicon fuse utilizing silicide electromigration (EM). Main advantage of a silicided-poly fuse is compatibility with standard CMOS technology; means there is no need for an extra litho- or process-steps. Therefore, its usage is very easy and practical [17]. In order to program an eFuse, high current density is applied through the eFuse and high current removes the silicidation layer and increases its resistance [17,18].

In this project, an 8-bit rad-hard eFuse cell was designed to be used for analog circuit calibration. The 8-bit eFuse cell trims the bandgap reference voltage. As explained in Chapter 3, there are eight resistors and eight NMOS switches connected in parallel at the output of bandgap voltage reference. If the gate voltage of NMOS transistor is logic-high, the resistor is short-circuited and if it is low, the resistance value is added to reference resistor at that branch. The 8-bit output of the eFuse block is connected to the gate voltages of the NMOS switches. By programming or, in other words, burning the selected eFuses, the bandgap reference voltage can be precisely adjusted.

4.1 1-BIT EFUSE CELL

The 1-bit eFuse cell is a one-time programmable block, that includes an eFuse component, was developed for analog circuit trimming to be used in harsh environments, especially in terms of radiation. The designed eFuse cell has two power domains: I/O domain at 2.5V and core domain at 1.2V. This cell has three input and one output pins:

1. READ input to read the output of the eFuse cell.
2. CLK input to store the output of the eFuse cell into the memory cells.
3. PROG input to burn the eFuse component to change its output value.
4. DATA_Q output that is the final output of 1-bit eFuse cell.

All input and output signals are in core domain, i.e. logic low is 0 and logic high is 1.2V for the input and output pins. When they are used in I/O blocks, their logic-high values are shifted-up by level-shifters and their logic-high value becomes 2.5V.

Firstly, the working principle of the I/O block, and then the working principle of the core block will be expressed.

4.1.1 I/O BLOCK

The eFuse component that determines the output value of the cell is present in I/O block. All transistors in this block are I/O transistors that can withstand up to 2.5V. Since the READ and PROG

inputs are used in I/O domain, their levels are changed by level-shifters. Figure 4.1 shows the essential part of the I/O block.

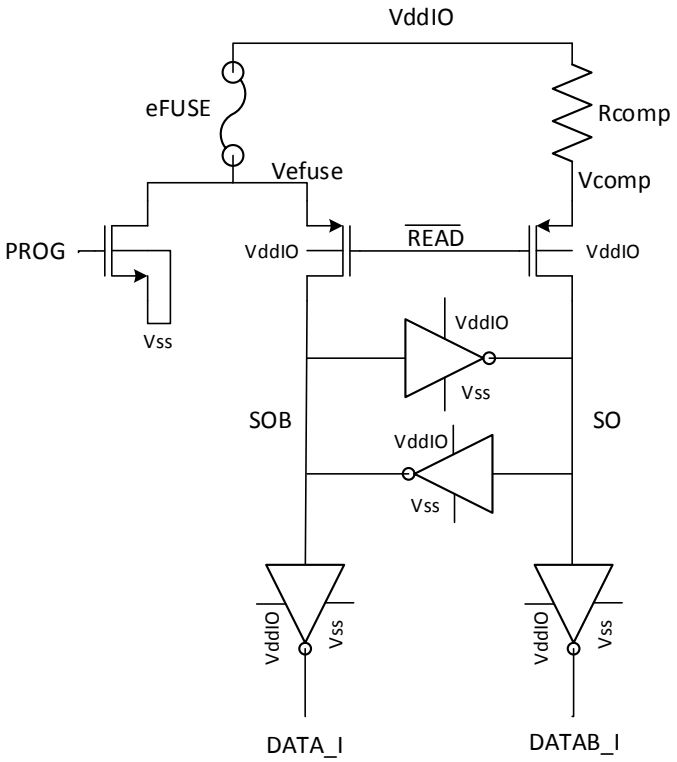

Figure 4.1: I/O domain part of 1-bit eFuse cell.

There is an eFuse component and comparison resistor R_{comp} to determine the output of the 1-bit eFuse cell. The resistance of a non-programmed or non-burned eFuse component is about 10Ω and the resistance of the comparison resistor R_{comp} is about 1.1kΩ. The burning operation removes the silicidation of the eFuse, increasing the resistance. Figure 4.2 shows the internal signals in the I/O block of a 1-bit eFuse cell during the read operation if the eFuse is non-burned. During the read process, PROG signal should always be logic-low. The signals behave as follows:

1. When READ signal is applied, its level is shifted up into the I/O domain by a Level-Shifter and the $\overline{READ}$ signal, that is inverted version of the shifted-up READ signal, is applied to the gate of the PMOS switches.
2. Since the resistance of the eFuse is smaller than R_{comp}, the value of V_{efuse} is larger than the value of V_{comp}.
3. Since the value of V_{efuse} is larger than V_{comp}, the value of SOB is greater than the value of SO.
4. After the rising edge $\overline{READ}$ signal, the current flow from the VddIO to the SOB and SO nodes stops, and since the value of SOB was larger than SO during READ, the back-to-back inverter latch sets SOB to logic-high and SO to logic-low.
5. Since SOB was set to logic-high and SO to logic-low, DATA_I is set to logic-low and DATAB_I to logic-high after the falling edge of the READ signal. During the period where READ was logic-high, both DATA_I and DATAB_I are reset to logic-low.

This is the read operation for a non-burned eFuse. If the eFuse is burned, its resistance becomes about 3kΩ, which is greater than R_{comp}. Therefore, SOB is set to logic-low and SO to logic-high after the falling edge of READ signal. In contrast to non-burned eFuse case, DATA_I becomes logic-high and DATAB_I becomes logic low.

For the programming operation, a wide NMOS driver (81.75µm/0.28µm) are used to allow a high current of about 40mA to 50mA to flow on left branch via the eFuse component. During the programming mode, READ signal must be logic-low, and a high current of about 40mA to 50mA flows from VddIO to Vss through the eFuse. Since a current greater than 20mA burns the eFuse, the eFuse will be programmed in the programming operation. When an eFuse is burned once, there is no possibility to convert it into the non-burned version again. Thus, it is a one-time programmable cell.

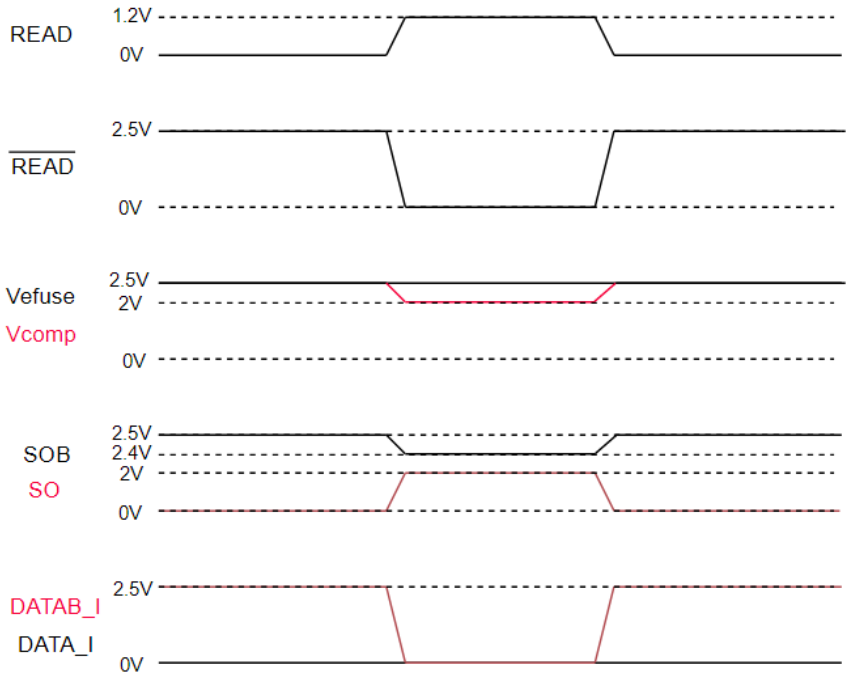

Figure 4.2: Read operation in the I/O part of the eFuse cell.

4.1.2 CORE BLOCK

In the IO block, the values of DATA_I and DATAB_I are set in the read operation. After that, these two signals are connected to NMOS I/O transistors in the core domain (Figure 4.3).

As can be seen from Figure 4.3, the DATA signal is connected to VddCORE while READ is logic-high and $\overline{READ}$ is logic-low. After the rising edge of $\overline{READ}$, this connection becomes open, and the value of DATA is set by the signals DATA_I and DATAB_I. If the eFuse is non-burned, DATA_I is logic-low and DATAB_I is logic high. Thus, DATA is connected to Vss, which is 0V. When the eFuse is burned, then DATA_I is logic high, and DATAB_I is logic low. Consequently, DATA is connected to VddCORE that is 1.2V.

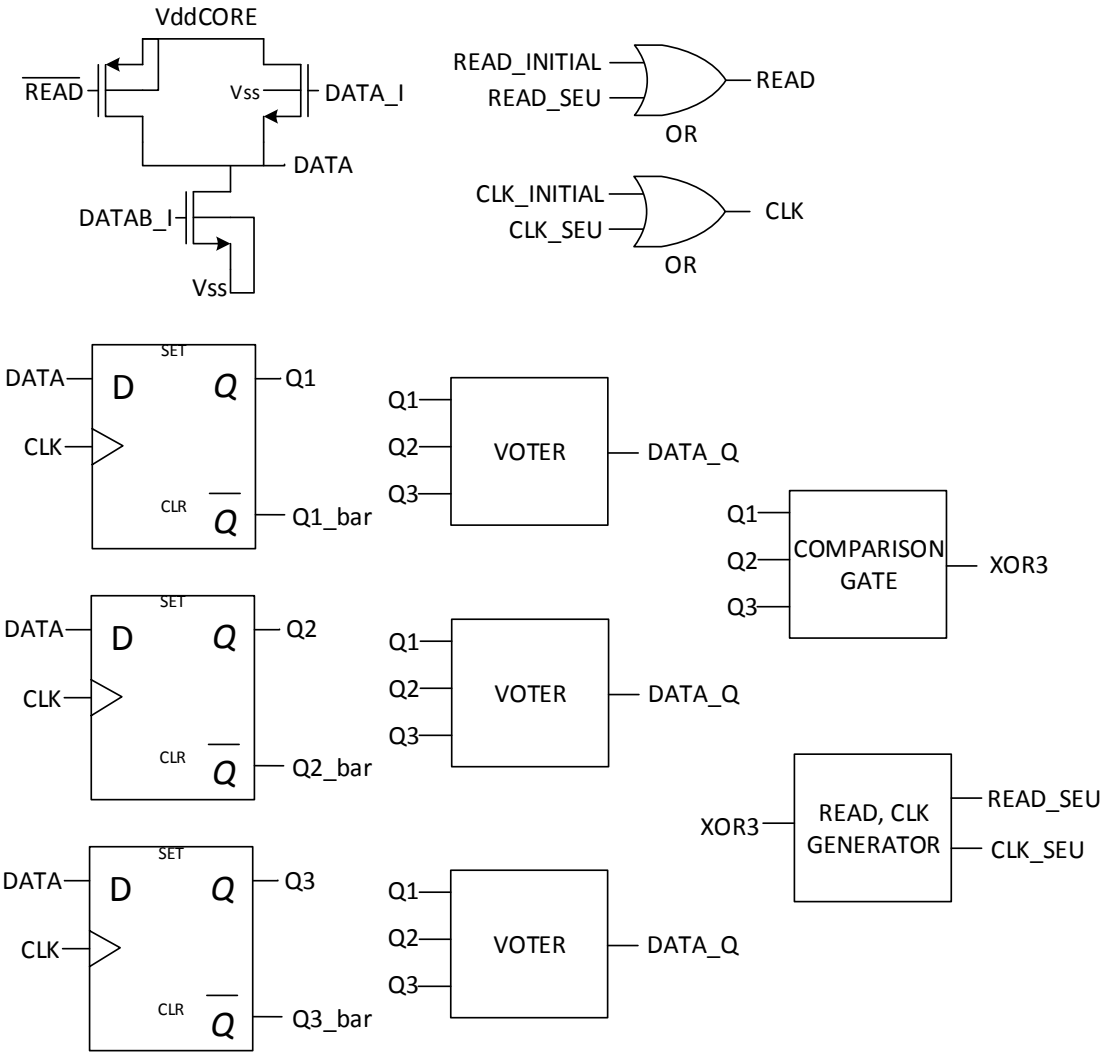

Figure 4.3: Core domain part of 1-bit eFuse cell. Triplicated parts are to prevent SEU.

Normally, the DATA signal could be the final output of the eFuse cell, however the value of DATA can change for a short time due to single event upset (SEU), and it may lead to a shift in the bandgap reference voltage. In order to have a SEE-resistant output signal, critical digital blocks were physically triplicated. Figure 4.4 shows the internal signals in the core part, and its working principle is the following:

1. The signal DATA, which has been read, is stored in 3 D-flip-flops as Q1, Q2 and Q3 in the rising edge of the CLK signal. D-flip-flops are physically triplicated against the SEU within the D-flip-flop.
2. The outputs of the 3 D-flip-flops are connected to the triplicated voters, which takes the decision by selecting the logical value stored by at least two of the three memory cells. The voters are also triplicated against the SEEs. The outputs of the voters, DATA_Q, are connected to each-other against SEUs, and DATA_Q is the final output of the eFuse cell.
3. Since a memory cell, D-flip-flop, is used in this block, SEEs can create a permanent error. Thus, the D-flip-flop has to be reset in case of a change at its output. The outputs of the D-

flip-flops, Q1, Q2 and Q3 are connected to Comparison gate, and if one of the inputs is different, XOR3 becomes logic-high, and the rising edge of XOR3 signal triggers the generation of READ_SEU and CLK_SEU signals in the READ_CLK_Generator block.

4. The initial read and clock signals, READ_INITIAL and CLK_INITIAL are applied to OR gates with the created read and clock signals due to SEU, which are READ_SEU and CLK_SEU. Finally, READ and CLK signals are applied to I/O block and D-flip-flops respectively.

The DATA_Q signal is the final output of the 1-bit eFuse cell and applied to the gates of the NMOS switches in the bandgap voltage reference.

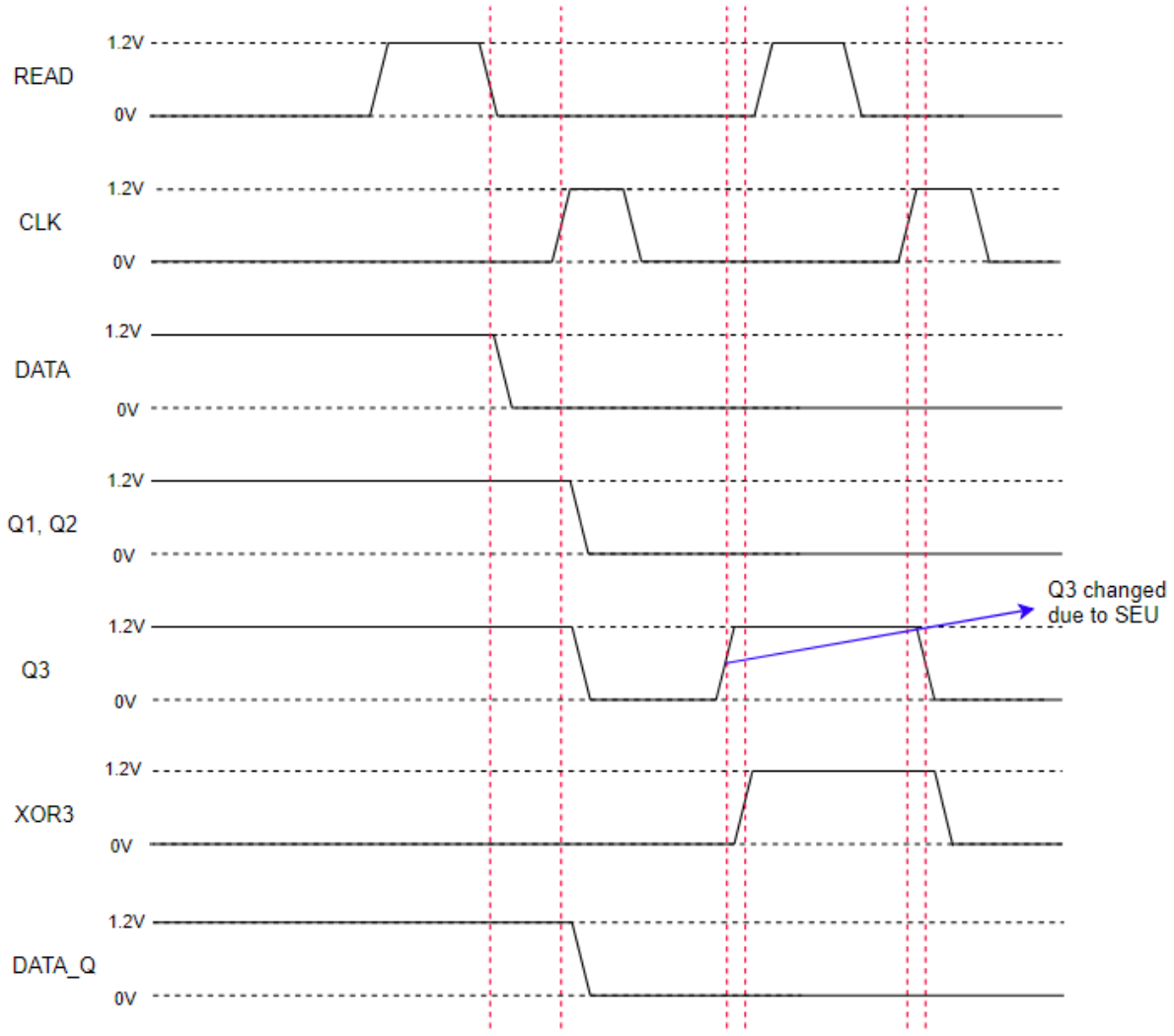

Figure 4.4: Internal signals in the core domain of the 1-bit eFuse cell. The DATA is read at the falling edge of the READ signal and stored as Q1, Q2 and Q3 at the rising edge of CLK. If there is a SEU at the output of the D-flip-flops, and for instance if it changes the value of Q3 (one of the stored outputs), XOR3 signal becomes logic high and it triggers additional READ and CLK signals. Since the final output DATA_Q is the majority of Q1, Q2 and Q3, it is not affected by SEU.

4.2 8-BIT EFUSE CELL

The 8-bit eFuse block is a rad-hard analog trimming block in order to adjust the bandgap reference voltage. This block consists of eight 1-bit eFuse cells, an 8-bit decoder and some logic gates. This block has the following input and output pins:

1. READ input signal is applied to eight 1-bit eFuse cells to read the value of the eight eFuses.
2. CLK input signal is applied to eight 1-bit eFuse cell to store the read data and acquire the final outputs of the eight 1-bit eFuse cells.
3. PROG input signal is applied to program single eFuse cell at a time.
4. 3-bit address signal Address<2:0> is applied as an input signal, to select the eFuse which will be programmed.
5. 8-bit output signal Q_buff<7:0> to be connected to the switches in the bandgap voltage reference to trim the bandgap voltage.

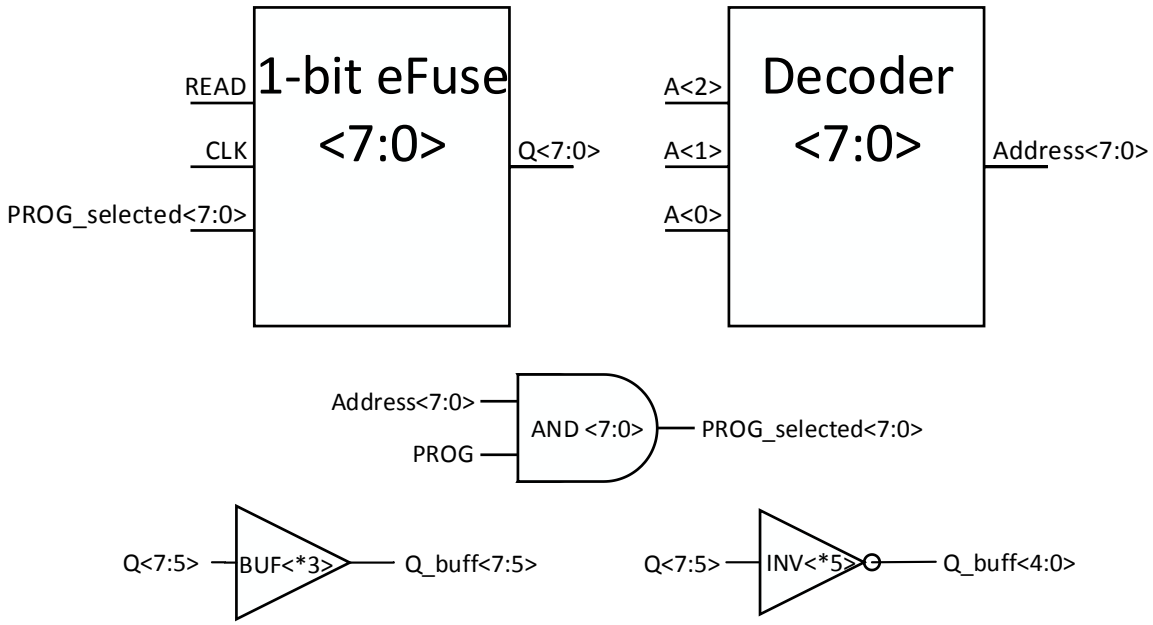

Figure 4.5: Representation of 8-bit eFuse cell.

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The common READ and CLK signals are applied to all eight 1-bit eFuse cells. On the other hand, only single 1-bit eFuse cell can be programmed at a time, thus 3-bit address signal Address<2:0> is applied to the block in order to create 8 bit address by a decoder. This 8-bit address signal is connected to the inputs of 8-bit AND gate with PROG signal. Depending on the applied address signals Address<2:0>, the selected eFuse is burned. If an eFuse was already burned, there is no chance to program this eFuse again, since it is a one-time programmable cell and a burned eFuse component cannot be fixed.

The output of the eight 1-bit eFuse cells is Q<7:0> and the output of a non-burned eFuse is 0V. Thus, Q<7:0> is <00000000> for the non-programmed 8-bit eFuse block. As explained in Chapter 3, the switches in the bandgap voltage reference are connected to <00011111> to be able to trim the reference voltage upwards and downwards. Consequently, the most significant three bits are buffered and

other five bits are inverted as Qbuff<7:0>. This output signal is the final output of the 8-bit eFuse cell and connected to the gates of the NMOS switches in the bandgap voltage reference (Figure 3.3).

4.2.1 DC ELECTRICAL CHARACTERISTICS AND TIMING WAVEFORMS

4.2.1.1 PROGRAMMING OPERATION

The electrical fuse, eFuse, is one time programmable at a time, i.e. only one of the 1-bit eFuse cells can be programmed at a time by applying the required address and programming signals. After the programming of a bit is finished, another 1-bit eFuse cell can be programmed in the 8-bit eFuse block. In the programming mode, the READ signal must be kept as logic low, and the PROG signal must be kept as logic-high for a period of t_{PG}. All of the address signals have to satisfy that they become logic-high t_{ASP} before PROG goes to logic-high, and become logic-low t_{AHP} after PROG goes to logic-low. Thus, the minimum period to program a 1-bit eFuse is $t_{ASP}+t_{PG}+t_{AHP}$ as shown in Figure 4.6.

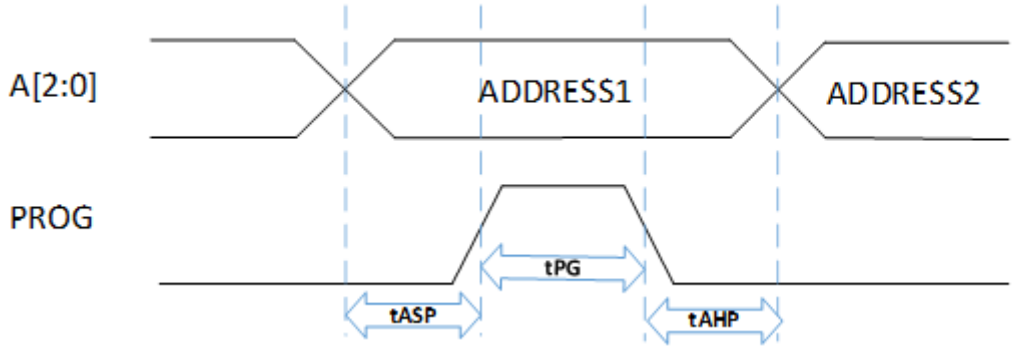

Figure 4.6: Waveforms of the PROG and Address signals during programming operation.

The timing parameters for the programming mode are listed in Table 4.1. In the table, minimum and maximum values are shown, and the simulations are run at t_{ASP}=100ns, t_{PG}=20µs and t_{AHP}=100ns.

Parameter	Meaning	Min. Value	Max. Value
t_{ASP}	Address to program rising setup time	100ns	-
t_{PG}	Programming duration	10us	30us
t_{AHP}	Address to program falling hold time	100ns	-

Table 4.1: Timing parameters for the programming mode.

The minimum current value to burn an eFuse must be more than 20mA. Table 4.2 shows the programming current that flows via eFuse in different temperatures, I/O voltages and process. The programming current is more than sufficient for any corners; even if the VddIO is decreased to 2V. In nominal conditions, VddIO is set to 2.5V. Programming operation will be performed at room temperature and when VddIO is connected to an external power supply and set to 2.5V. Therefore,

the programming current is about 42mA in the worst case, when the process is asspss, which means actives slow (NMOS) slow (PMOS), passives slow (resistors) slow (capacitors). Thus, the value of the programming current is high enough to burn the eFuse at any corner.

Programming Current (I_{pg})	Temperature	VddIO	Process
47.5mA	0C	2.5V	attptt
45.3mA	27C		
33.1mA	0C	2V	
31.6mA	27C		
50.6mA	0C	2.5V	affpff
48.5mA	27C		
35.9mA	0C	2V	
34.1mA	27C		
44.5mA	0C	2.5V	asspss
42.3mA	27C		
30.7mA	0C	2V	
29.1mA	27C		

Table 4.2: Programming current flows through the eFuse to burn it.

4.2.1.2 READ OPERATION

Read operation is applied to unload data from the electrical fuse. The default, not programmed, value of an 8-bit eFuse is <00011111>. A programmed bit will be inverted and the value of the bandgap reference voltage will change accordingly.

In the read operation, the PROG and the address signal Address<2:0> are set to ground by pull down resistors and the READ signal has to be kept logic-high for a period of t_{READ} to unload the data out. After t_{RD_CLK} seconds of the falling edge of the READ signal, the CLK signal has to be applied and be kept as logic-high for a period of t_{CLK}. The final output DQ will be latched after a time of t_{DQ} of the rising edge of the CLK signal and it will be kept constant as long as the CLK is kept as logic-low. The timing parameters are shown in Table 4.3.

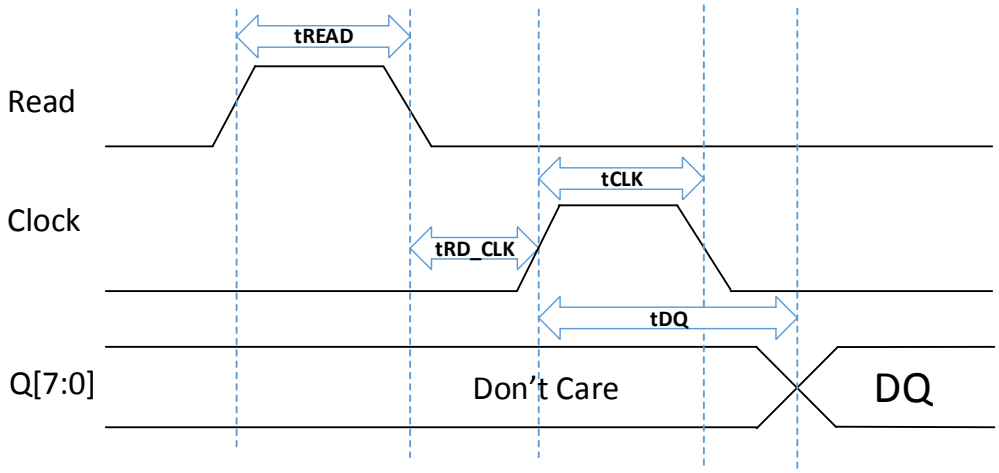

Figure 4.7: Waveforms of the READ, CLK and the output Q signals during the read operation.

Parameter	Meaning	Min. Value	Max. Value
t_{READ}	Read pulse high width	35ns	-
t_{RD_CLK}	Read falling edge to Clock rising edge	15ns	-
t_{CLK}	Clk pulse high width	7ns	-
t_{DQ}	Clk rising to data out access time	5ns	-

Table 4.3: Timing parameters for the reading mode.

4.3 LAYOUT

The layout of the 8-bit eFuse cell can be seen in Figure 4.8. The area of this block is 372.94µm×356.485µm. It consists of eight 1-bit eFuse cells, eight 1-bit buffers, an 8-bit decoder and some additional blocks. In addition to MOM capacitors, NMOS transistors are used as a capacitor due to their large capacitance per unit area ($12.25 fF/\mu m^2$).

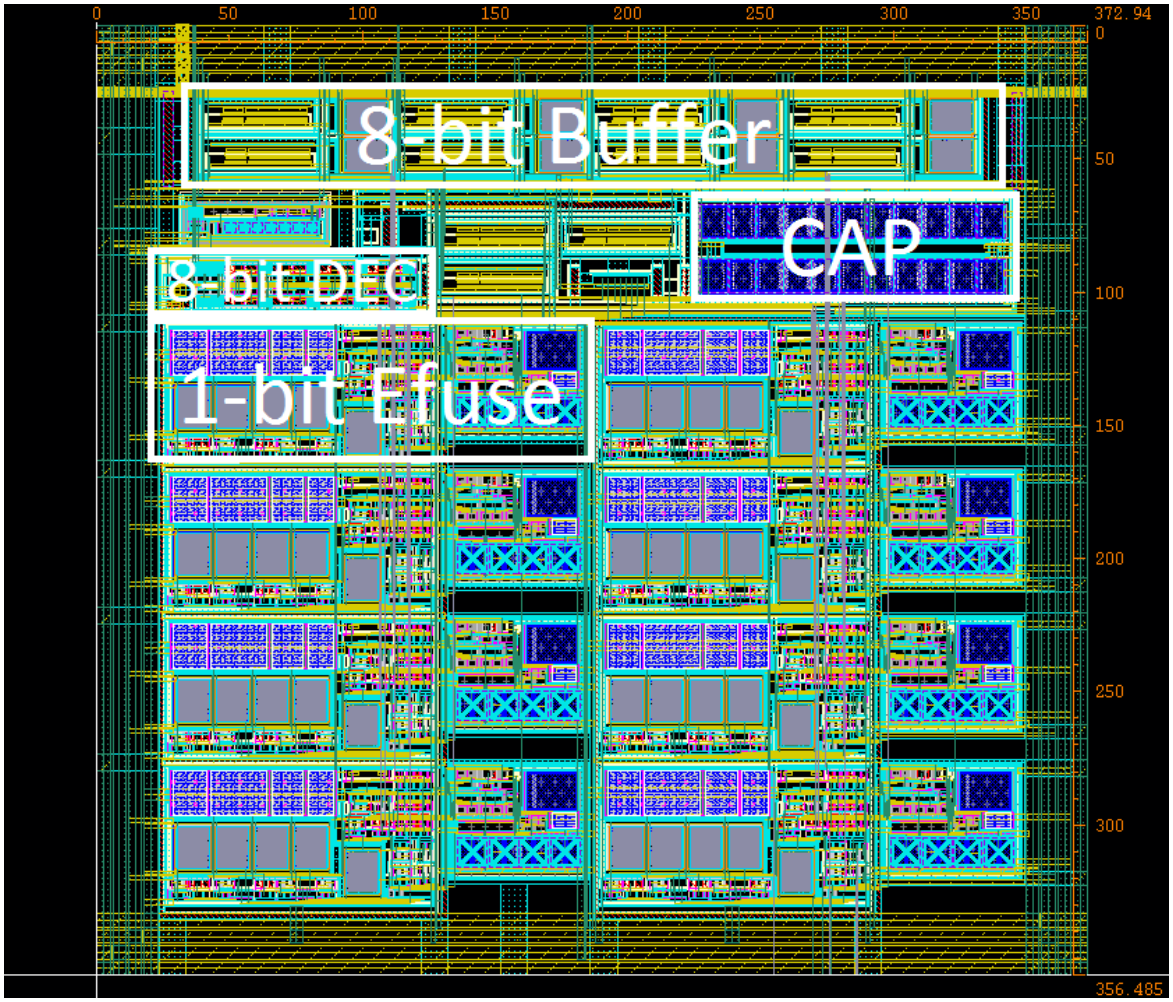

Figure 4.8: Layout of the 8-bit eFuse cell.

CHAPTER 5
OVER-TEMPERATURE PROTECTION CIRCUIT

In addition to eFuse based calibration block for the bandgap voltage references, an over-temperature protection circuit was designed to be used in DC/DC converters. This block is to disable the DC/DC converter, if it heated up more than 100^0C, enable it again when the temperature decreased to 70^0C. It has a hysteresis of about 30^0C, and after the DC/DC converter was disabled, it will start to cool down since there is no current flow inside of the chip. When the temperature decreased to 70^0C, the DC/DC converter will be enabled again.

In the DC/DC converter, there is already an enabling part and when its input is logic-low, it enables, and when its input is logic-high, it disables the DC/DC converter. Thus, a pulse signal, shown in Figure 5.1, with a hysteresis of 30^0C has to be generated.

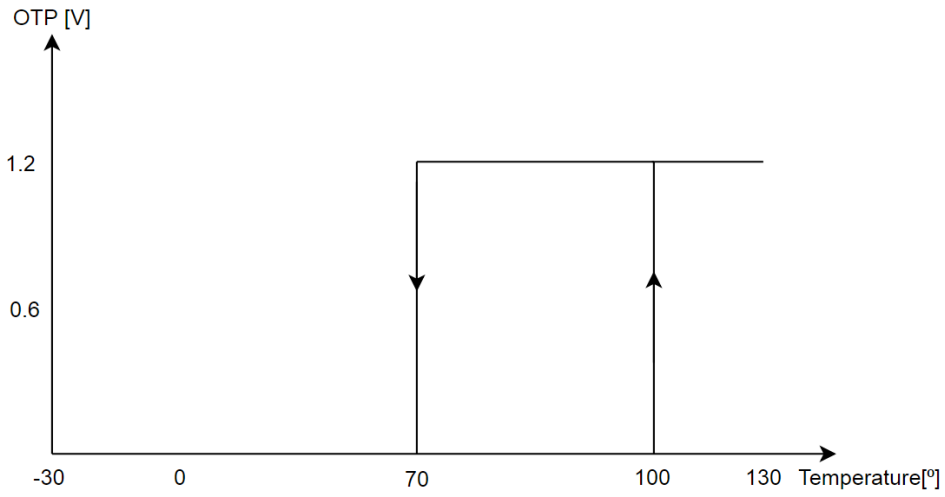

Figure 5.1: Over-Temperature Protection (OTP) signal becomes logic-high at 100°C and logic-low at 70°C with a hysteresis of 30°C.

5.1 WORKING PRINCIPLE

In order to create this OTP signal, the in+ signal and bandgap signal in the bandgap voltage reference block (Figure 3.3) are compared. In+ voltage, that has a negative temperature coefficient, must cross V_{bgp} (at 300mV, independent of temperature) at 100^0C, however its value is about 258mV at this temperature. Therefore, in+ voltage is amplified to become 300mV at 100^0C and the name of the output signal of the amplifier is called as CTAT. After that, the bandgap voltage, V_{bgp}, is compared with CTAT voltage as shown in Figure 5.2. Since CTAT voltage decreases in temperature, V_{bgp} becomes higher than CTAT after a point, and OTP becomes logic-high, $\overline{OTP}$ becomes logic-low. When $\overline{OTP}$ becomes logic-low, the NMOS switch in the non-inverting amplifier becomes off, the resistance R4 is added to the resistance branch (R1,R2,R3) and the gain of the amplifier decreased. Thus, CTAT voltage drops, right after OTP becomes logic-high. When the temperature started to decrease, the

voltage of CTAT node increases, however OTP does not become logic-low at same temperature, since the value of CTAT was decreased when OTP became logic-high. Thus, OTP becomes logic-low at a lower temperature compared to the temperature when it becomes logic-high. By changing the resistance in the non-inverting amplifier, its gain and the value of CTAT voltage were shifted and a hysteresis of 30^0C was achieved. The behaviours of the signals are shown in Figure 5.3.

In addition to the over-temperature protection part, a temperature monitor part was designed and integrated inside of this block. Temperature monitor consists of an inverting amplifier and two op-amp based unity gain buffers. The bandgap reference voltage, that is 300mV, is attenuated by the resistances R6 and R7 to about 280mV, and this attenuated voltage is connected to the positive node of the inverting amplifier as the reference voltage. By using this reference voltage, the in+ voltage is amplified by the inverting amplifier and PTAT_amp voltage is generated. As can be seen in Figure 5.3, it increases linearly from about 0V to 1V between -30^0C and 100^0C. After about 100^0C, its slope decreases a bit, and it becomes 1.2V at about 150^0C. The temperature inside of the chip can be estimated with this temperature monitor.

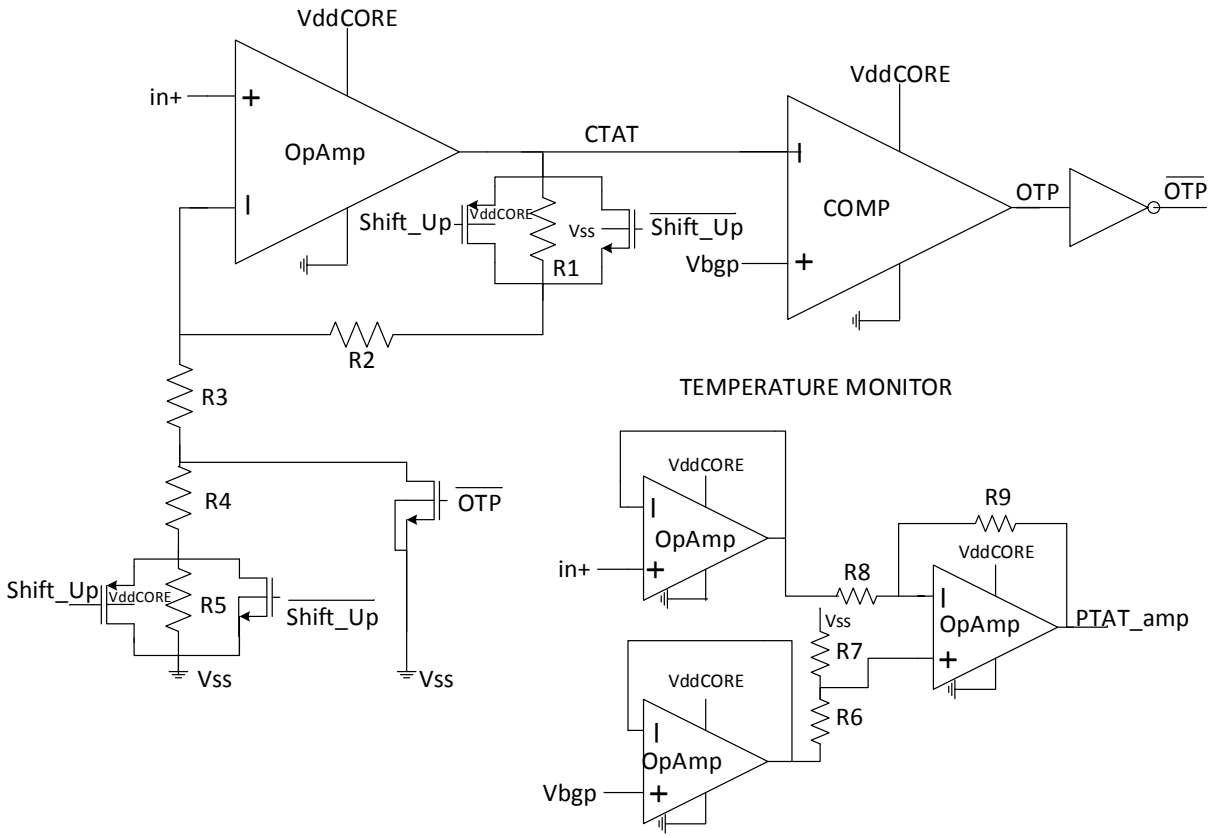

Figure 5.2: Over-temperature protection and temperature monitor circuit.

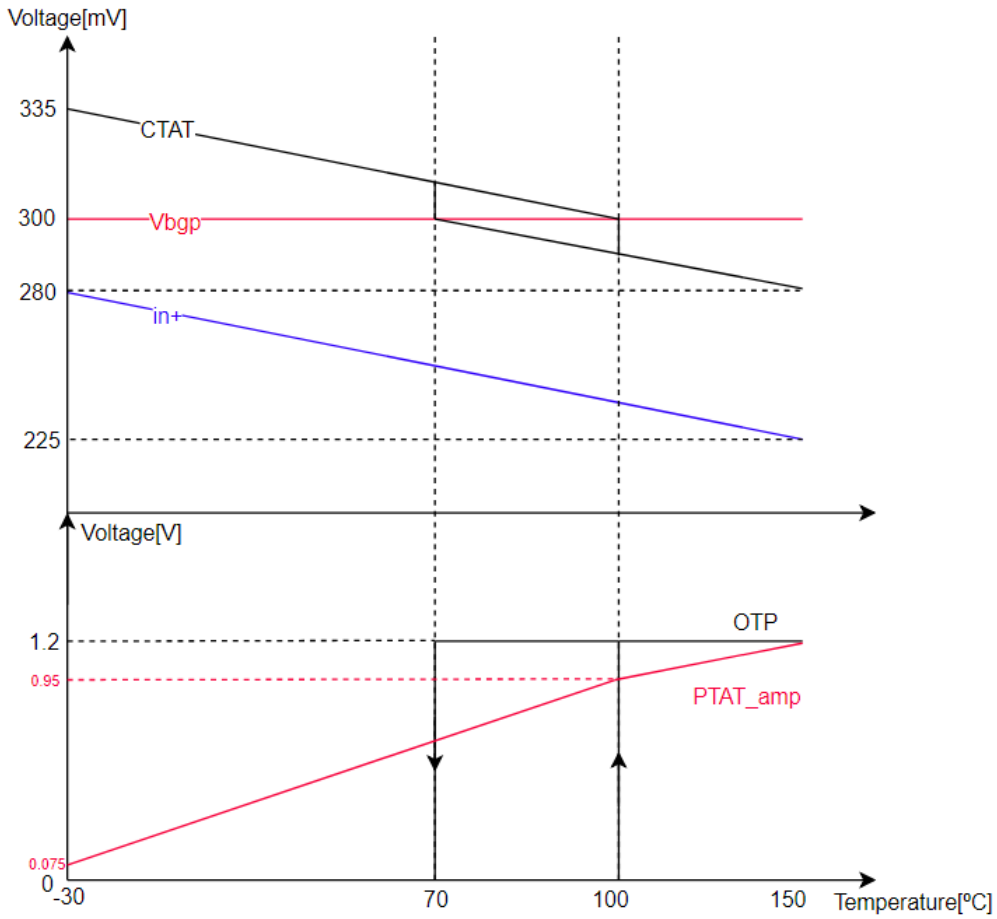

Figure 5.3: Waveforms in the over-temperature protection system. In+ signal is amplified and generates CTAT signal. CTAT is compared with the reference Vbgp and generates the OTP signal with a hysteresis of 30°C. PTAT_amp is the temperature monitor signal.

5.2 SIMULATION RESULTS

Under nominal conditions, OTP and PTAT_amp signals behave as shown in Figure 5.3. In this part, their variations due to radiation, process and mismatch are analyzed. Under nominal conditions, OTP becomes logic-high at 100°C and logic-low at 70°C. These characteristic must not change significantly with radiation, process variation and mismatch.

Figure 5.4 shows the OTP versus temperature graph in different radiation and process corners, and Figure 5.5 shows the variation of OTP in temperature due to mismatch. As can be seen, the rising and falling temperatures of OTP may shift up to about ±40°C and the hysteresis of OTP may shift up to about ±10°C.

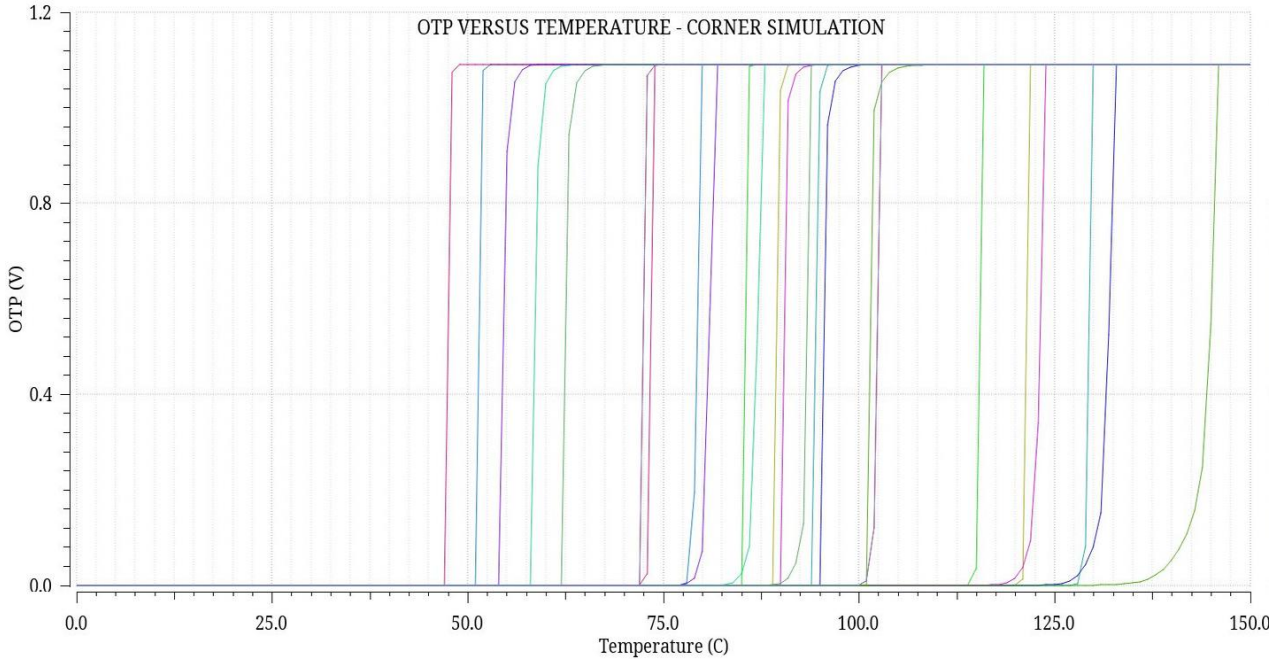

Figure 5.4: OTP versus temperature graph in different radiation and process corners. The rising and falling temperatures of OTP shifts about +40^{o}C and - 25^{o}C and the hysteresis of OTP shifts about ±10^{o}C in worst case corner.

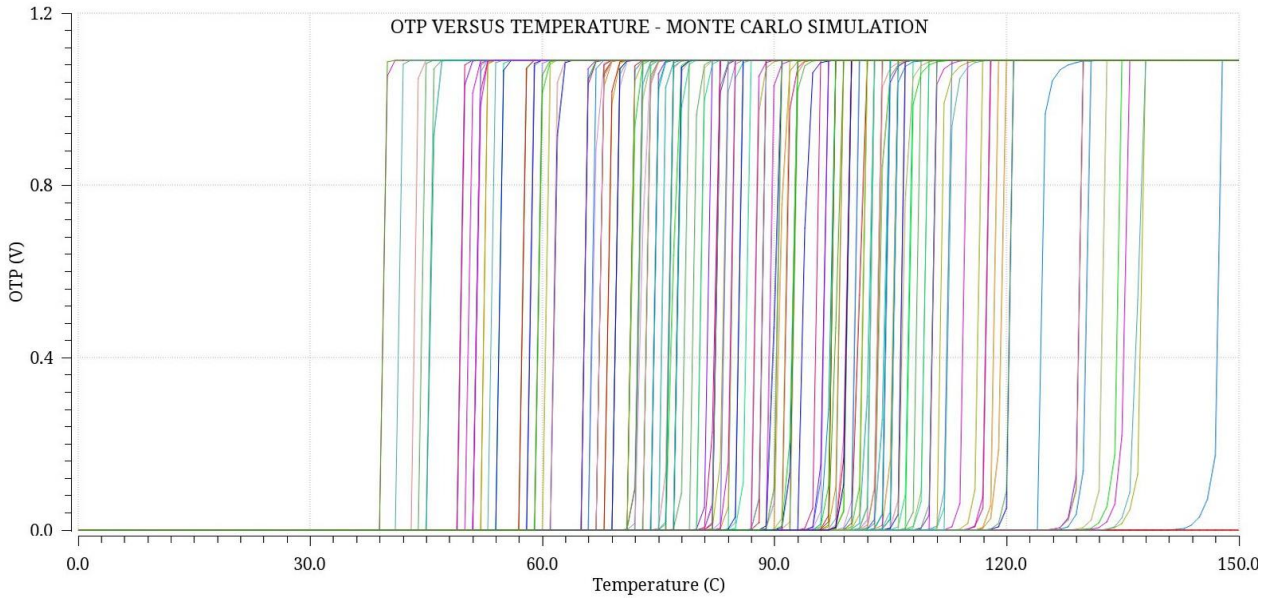

Figure 5.5: Variations of OTP signal due to mismatch, as simulated by Monte Carlo Simulations with 100 runs. The rising and falling temperatures of OTP shifts about +50^{o}C and -30^{o}C and the hysteresis of OTP shifts about ±10^{o}C in worst case.

Figure 5.6 shows the PTAT_amp signal, which is for monitoring the temperature inside the chip, versus temperature in different radiation and process corners, and Figure 5.7 shows the variation of PTAT_amp in temperature due to mismatch. The PTAT_amp voltage shifts about 0.4V in temperature due to mismatch, process variation and radiation, however its slope becomes constant up to about 70^{o}C.

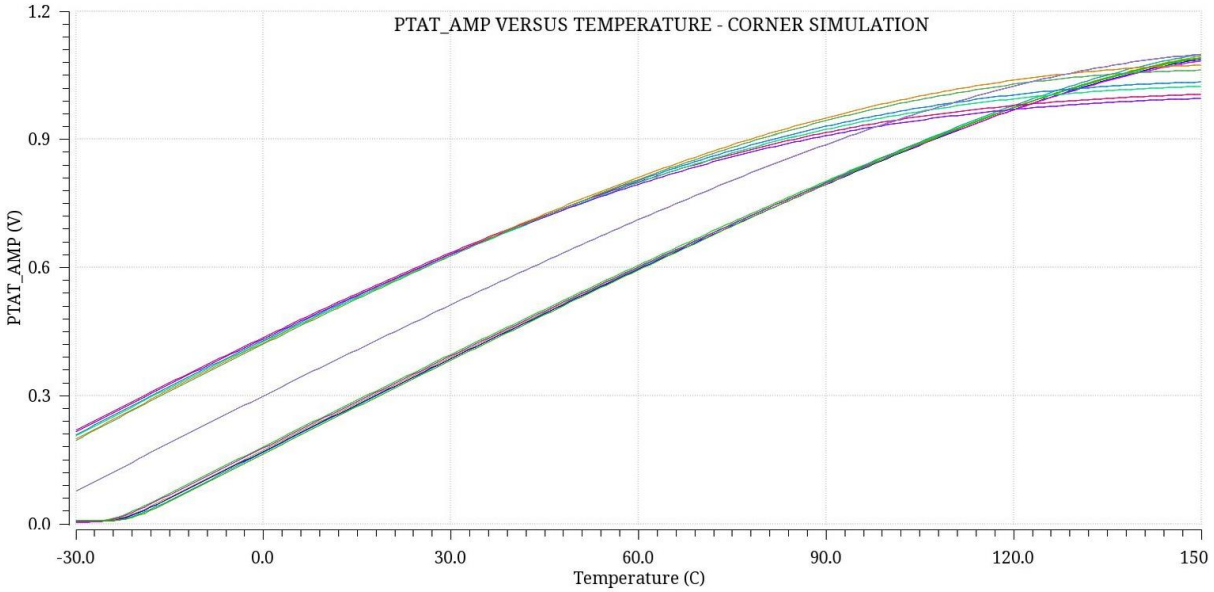

Figure 5.6: PTAT_amp versus temperature graph in different radiation and process corners. PTAT_amp voltage shifts less than 0.3mV in different process corners.

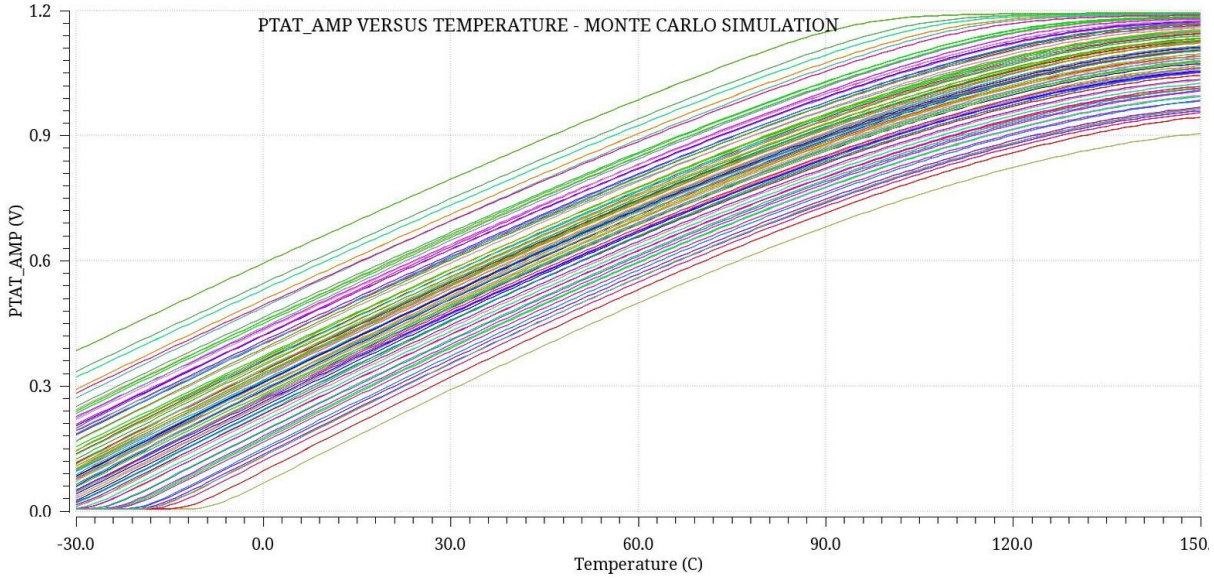

Figure 5.7: Variations of PTAT_amp signal due to mismatch, as simulated by Monte Carlo Simulations with 100 runs. PTAT_AMP voltage shifts less than 0.4V due to mismatch.

The properties of the OTP and PTAT_amp change significantly due to process and mismatch. The main reason is that, in+ and bandgap voltages in Figure 3.3 do not behave in same way with radiation, process and mismatch.

In the Over Temperature Protection part, in+ voltage is amplified and CTAT signal is generated. The variations in the in+ due to mismatch and process are also amplified, thus CTAT varies more in process and mismatch compared to in+. Since OTP is generated by comparing V_{bgp} and CTAT voltages, it shifts significantly due to mismatch and process variation.

In the Temperature Monitor part, the buffered version of in+ and V_{bgp} create the PTAT_amp signal. As can be seen in Figure 5.2, the attenuated version of V_{bgp} and the amplified version of in+ are the inputs of the third OpAmp. Thus, the variation of V_{bgp} is attenuated and the variation of in+ is amplified. As a result of that, PTAT_amp voltage varies considerably due to radiation, process variation and mismatch.

Furthermore, if the eFuse block is programmed and changes the bandgap reference voltage, both OTP and PTAT_amp shift considerably, because in+ node do not change, but V_{bgp} changes.

The crucial part of this block is to generate an OTP signal with a hysteresis about 30^0C and creating a PTAT_amp signal that increases with a constant slope in temperature. This OTP signal has 30^0C hysteresis with an error of $\pm10^0$C and PTAT_amp has a constant slope up to about 70^0C. In the second version of the chip, we will try to reduce the changes in OTP and PTAT_amp signals due to process variation and mismatch.

5.3 LAYOUT

The layout of the Over Temperature Protection circuit is shown in Figure 5.8. The area of this block is 219.53µm×395.885µm. This block consists of an operational amplifier, a comparator, matched resistors for the amplifiers, some switches, pull down resistors and capacitors against SEU.

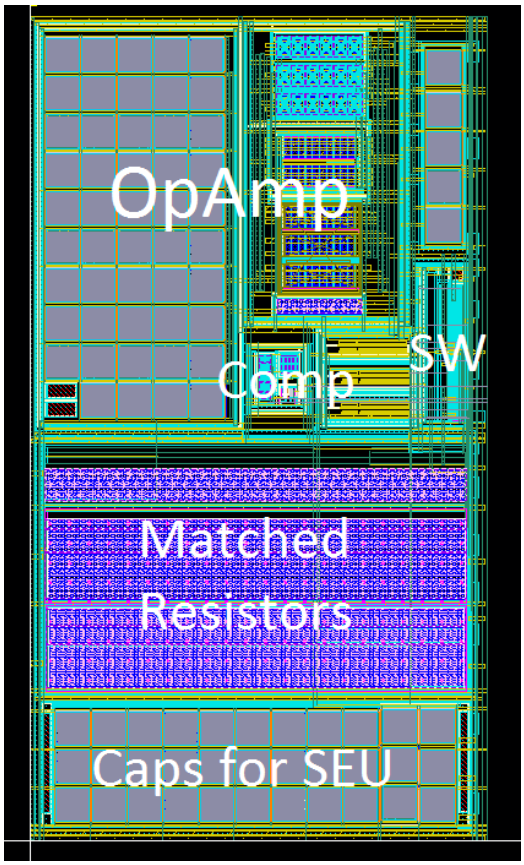

Figure 5.8: Layout of the Over Temperature Protection block.

The layout of the Temperature Monitor block can be seen in Figure 5.9. Its area is 555.03µm×213.635µm. This block is composed of three operational amplifiers and matched resistors for the amplifiers.

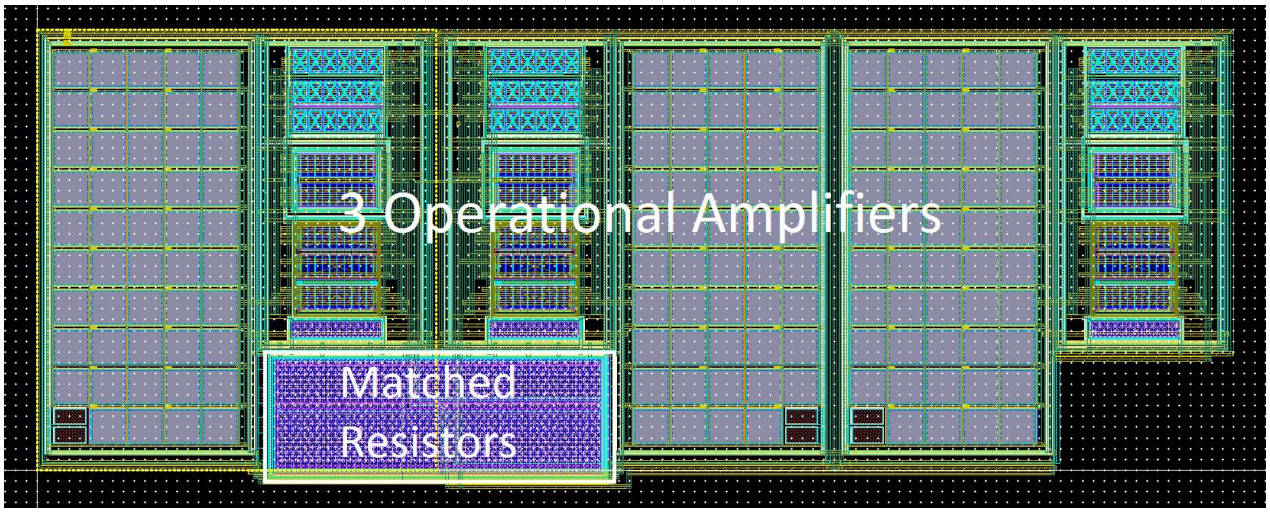

Figure 5.9: Layout of the Temperature Monitor Block.

CHAPTER 6
DESIGN OF THE TEST CHIP

This test chip was designed to characterize four identical bandgap voltage references with eFuse based analog trimming circuit on same chip. It includes four bandgaps with four 8-bit eFuse cells, and these blocks can be programmed separately, which means four bandgaps per chip can be tested.

The chip has dimensions of 1100µm × 2400µm and it contains two rows of 18 pads. The layout of the chip is shown in Figure 6.1 and the pinout is listed in Table 6.1. Dual power supply voltage is required for this chip (VddCORE = 1.2V and VddIO = 2.5V). The blue pins in Table 6.1 have IO ESD protections, and the others have CORE ESD protections.

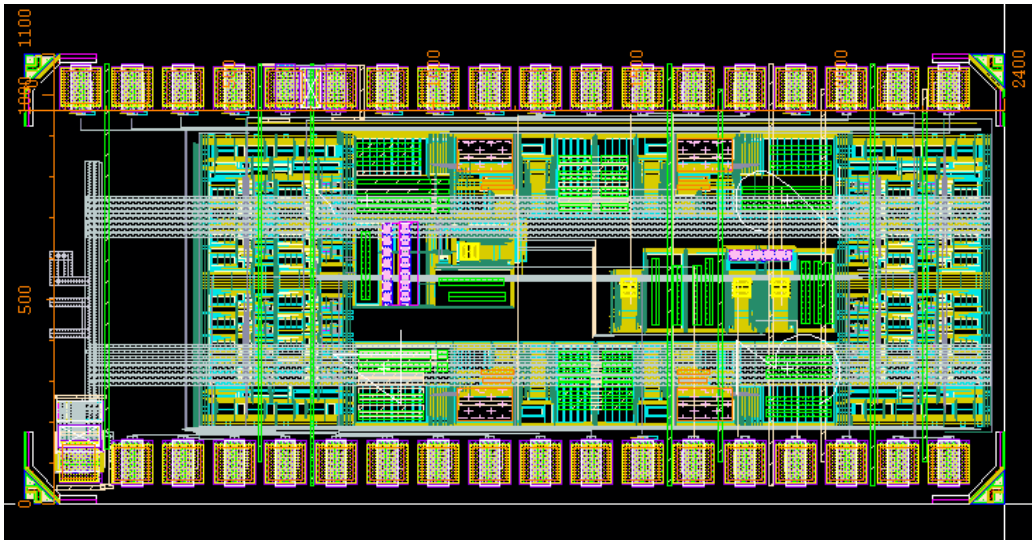

Figure 6.1: Layout of the test chip that contains four bandgaps. Only first bandgap includes over-temperature protection and temperature monitor blocks additionally.

1	VddIO	Address<0>	1
2	READ_bar	Address<1>	2
3	FuseOut<0>	Address<2>	3
4	FuseOut<1>	READ	4
5	FuseOut<2>	VddCORE	5
6	FuseOut<3>	Vss	6
7	FuseOut<4>	PROG_BGP1	7
8	FuseOut<5>	PROG_BGP2	8
9	FuseOut<6>	PROG_BGP3	9
10	FuseOut<7>	PROG_BGP4	10
11	CLK_sum	BGP1	11
12	Shift_Up_OTP	BGP2	12
13	OTP	BGP3	13
14	in+	BGP4	14
15	PTAT_AMPLIFIED	CLK	15
16	DATA_before_latch	XOR3	16
17	Q1	Q3	17
18	Q2	RX5	18

Table 6.1: The pinout of the test chip. The blue pins are in IO domain and have IO ESD protections. All the other pins are in CORE domain and have CORE ESD protection.

This test chip consists of four bandgaps and all the bandgaps include a bandgap voltage reference block and an 8-bit eFuse block. In addition, the first bandgap includes an over-temperature protection and a temperature monitor blocks. Furthermore, some internal signals of the first bandgap are connected to the pads in order to make a detailed analysis on this bandgap. The other three bandgaps are exactly same, and only their bandgap voltages are connected to the output pads.

The input signals of the chip are "READ, CLK, Address<2:0>, PROG_BGP1, PROG_BGP2, PROG_BGP3, PROG_BGP4 and Shift_Up_OTP". Same READ, CLK and Address signals are applied to all the four bandgaps. Each bandgap has its own programming signal. Thus, bandgaps can be programmed differently in order to have a precise output voltage after manufactured.

The BGP2, BGP3 and BGP4 are the outputs of the second, third and fourth bandgaps. To have a detailed observation, the first bandgap has additional outputs. BGP1, OTP and PTAT_AMPLIFIED signals are the main outputs of the first bandgap. Furthermore, it has several outputs such as FuseOut<7:0> to observe the output of the 8-bit eFuse cell in the first bandgap, Q1, Q2 and Q3 to observe the output of the D-flip-flops against SEU, READ_bar and CLK_sum to monitor the internal read and clock signals after SEU.

6.1 PROCEDURE TO PROGRAM THE EFUSES

The purpose of the eFuses in this chip is to calibrate bandgaps to have 300mV at the outputs BGP1, BGP2, BGP3 and BGP4. Due to mismatch and process variation, the value of the bandgaps can shift up to ±30mV and the maximum error in the bandgap voltage after the programming should be less than ±0.7mV. The procedure to calibrate the bandgap reference voltage follows:

1. Read the value of the BGP1.
2. According to the value of the BGP1, calculate the difference from 300mV and decide which bits to program depending on the Table 3.2.
3. Start programming from highest significant bit. After programming of every single bit, read the bandgap value to check if the voltage shifts correctly.
4. If the error is less than ±0.7mV, do not program it anymore.
5. Apply same procedure for the other three bandgaps.

The aimed precision was ±0.7mV, but the simulation results in Table 3.2 shows that a better precision at ±0.625mV was achieved. Thus, in the 4^{th} step of programming procedure, the chip can be programmed until the error is less than ±0.625mV.

CHAPTER 7
PROGRAMMING, MEASUREMENT SETUP AND MEASUREMENT RESULTS

In this chapter, the programming setup for the chip; and trimming, temperature and radiation test results of different bandgap chips will be presented. All the chips were designed in a commercial 130nm technology and manufactured in same fab. Each chip includes four identical bandgap blocks.

7.1 PROGRAMMING AND MEASUREMENT SETUP

After the chips were manufactured, they were wire-bonded to the printed circuit boards (PCBs) that were already designed by the other members of the group. This PCB model has 32 pins, and the chip has 36 pads. The pads that has to be wire-bonded to the PCB were selected and the PCB with wire-bonded chip is shown in Figure 7.1(a). The microscopic photo of the design on silicon is shown in Figure 7.1(b).

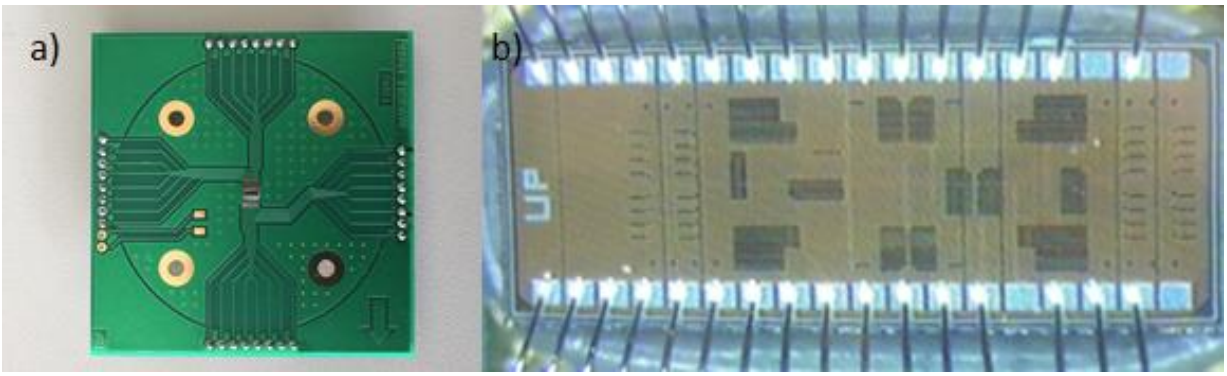

Figure 7.1: a) The PCB with the wire-bonded chip. b) The microscopic photo of the design on silicon.

This PCB has male-connectors and a programming setup with female connectors was prepared as shown in Figure 7.2(a). The programming setup has three power connections for VddIO, VddCORE, Vss; three address connections for 3-bit address signal; one read and one clock connections; four programming connections to apply four different programming signals to each bandgap; and four bandgap connections to observe the bandgap reference voltages of each bandgap block. For the READ, CLK and PROG signals, pulse signals are applied to the pins by waveform generators. Since the ports of the waveform generators are 50Ω-matched, 50Ω-resistors are connected to the READ, CLK and 4 PROG pads in the test setup.

Since the PCB of the chip has male connectors and the programming setup has female connectors, the PCBs of each chip can easily be plugged in the programming setup. Figure 7.2(b) shows that the PCB of the chip was plugged in the programming setup.

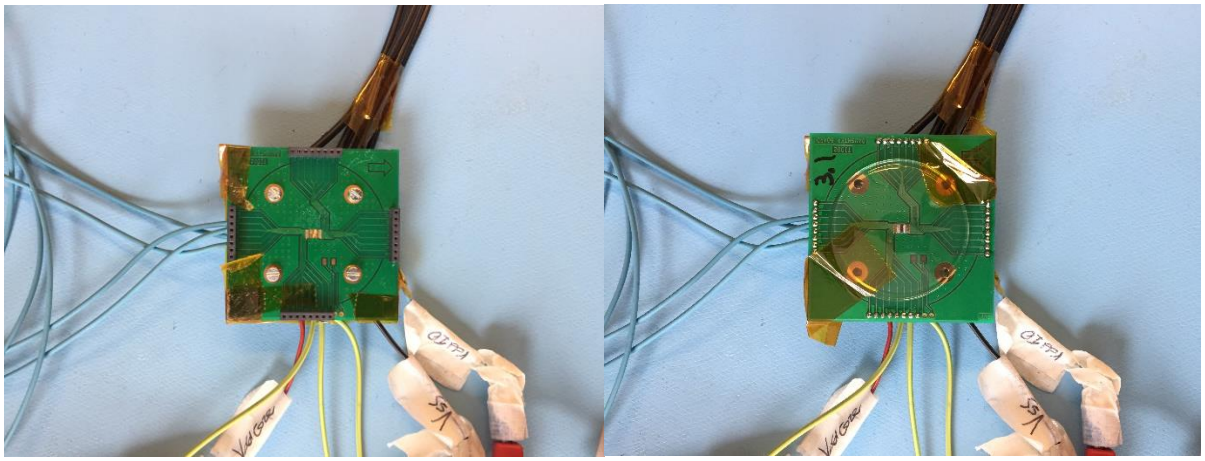

Figure 7.2: (a) The programming setup to program and test the chips (at left). (b) The PCB with the wire-bonded chip was plugged-in the programming setup.

To program and test the chips, the test setup in Figure 7.3 was used. Two DC power supplies were used to provide VddIO and VddCORE voltages, and three waveform generators were employed to provide READ, CLK and PROG signals. Four table multimeters were used to observe the bandgap reference voltages of each bandgap block simultaneously, and an oscilloscope was used to observe the FuseOut<7:0> output and some internal signals of the first bandgap block.

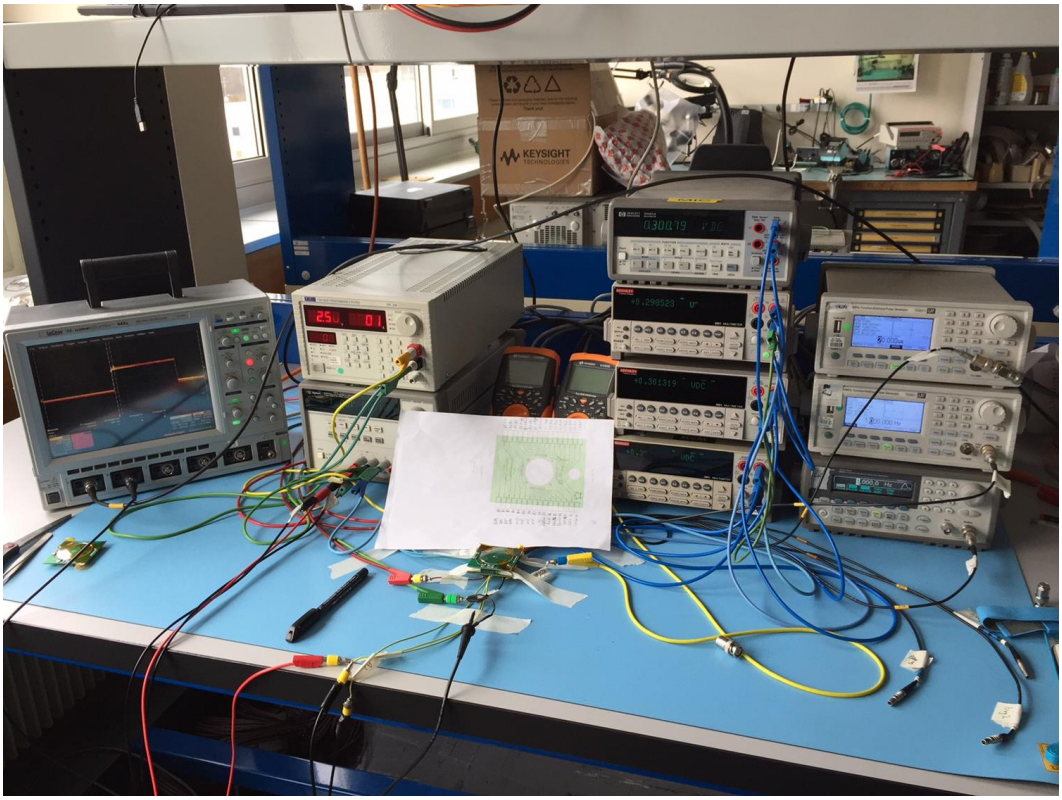

Figure 7.3: Programming and test setup for the chips.

For the TID and heavy ion tests, the setup shown in Figure 7.4 is used. Since the chip was exposed to radiation during these tests, it should be controlled outside of the X-ray machine or heavy ion chamber. Thus, the motherboard to connect the PCB of the chip was connected to the red control unit with 2-meter flat cable. The red control unit is outside of the radiation zone, and all the power lines, inputs and outputs are applied to the red test device.

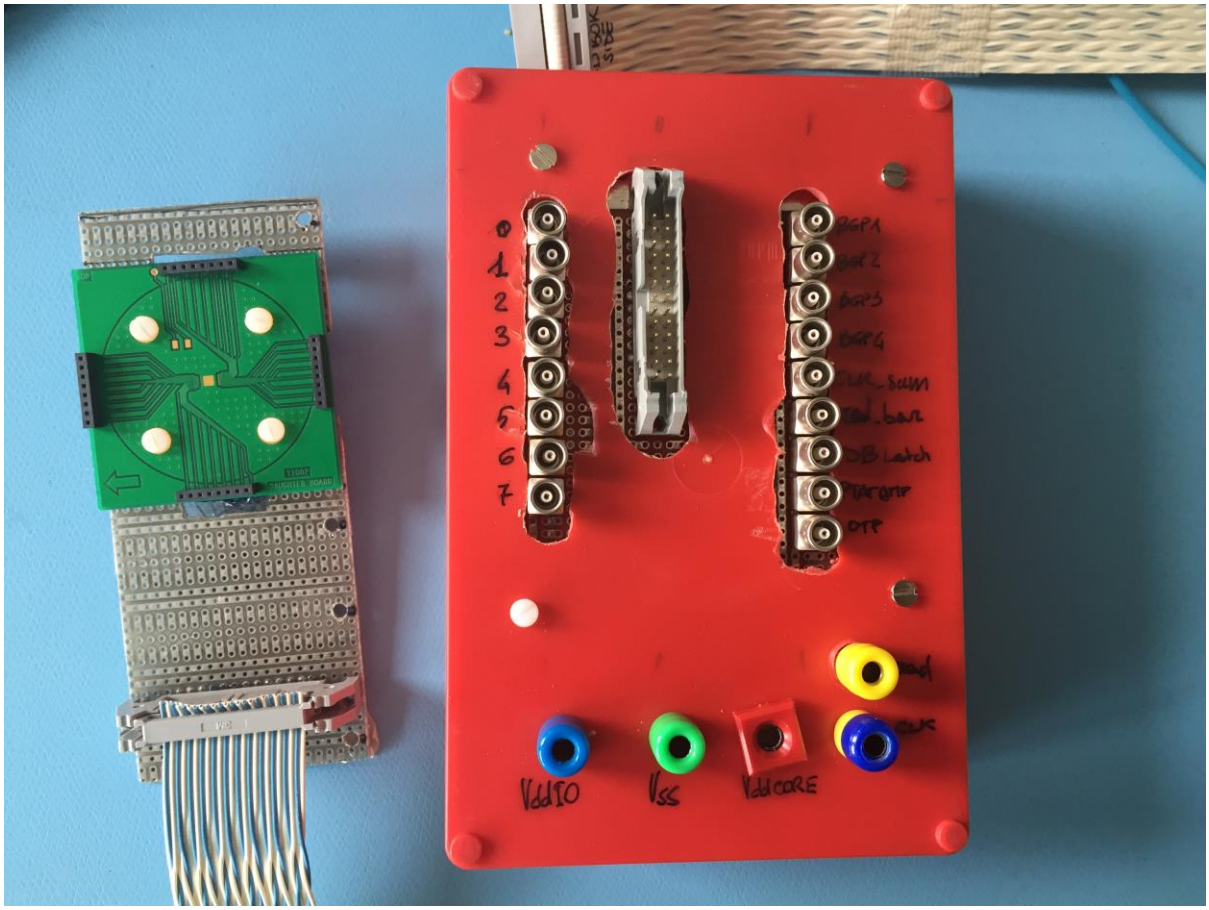

Figure 7.4: Measurement setup for the TID and heavy ion tests.

7.2 BANDGAP VOLTAGES BEFORE AND AFTER PROGRAMMING

In this part, 7 chips consist of 28 bandgaps in total are programmed and tested in room temperature. As explained in Chapter 3, the bandgap reference voltage shifts less than about ±30mV due to mismatch and process variation. The shifts of +30mV and -30mV are for the worst-case corners and it is a very low probability to have such a high variation. This can be experienced on very big productions of thousands of wafers.

Firstly, the bandgap voltages of 7 chips are observed before programming and the measurement results are shown in Figure 7.5. The tested bandgap reference voltages shift less than about ±10.5mV mainly due to mismatch because the chips come from the same wafer.

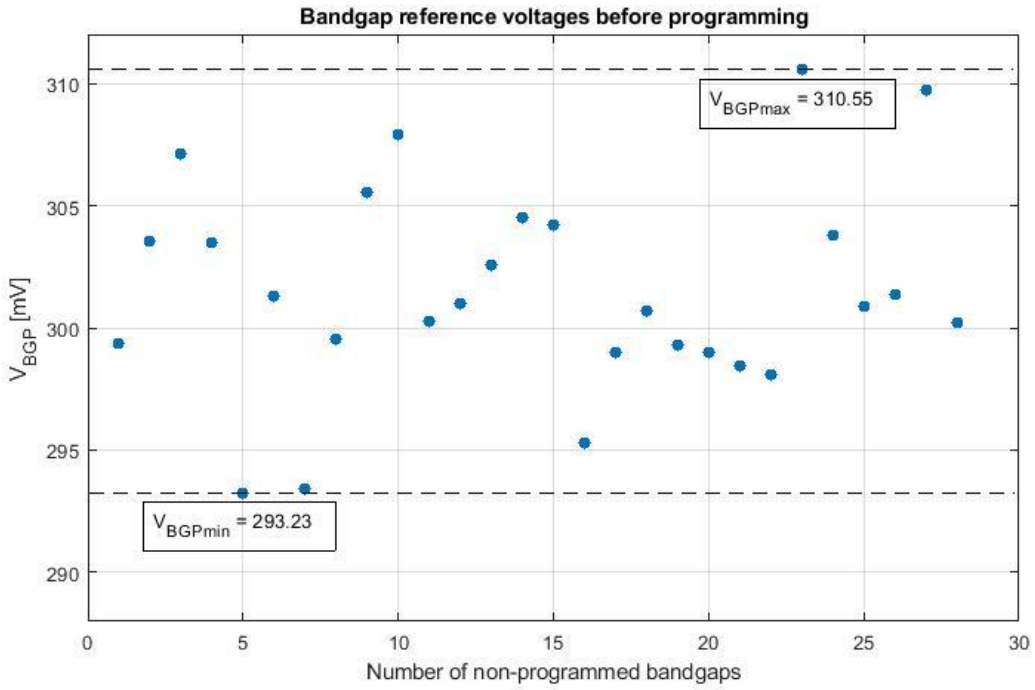

Figure 7.5: Measurement result – Bandgap reference voltages before programming in room temperature. The shifts in the bandgap reference voltages due to mismatch are observed (7 chips with 28 bandgaps from same wafer are tested).

After the bandgap voltages of the bandgap blocks were observed, these blocks were programmed by following the procedure to program the chips as explained in Chapter 6. After the programming, the maximum shift due to mismatch and process variation has to be ±0.6mV. Figure 7.6 shows the bandgap reference voltages after programming. These results show that the error due to radiation, mismatch and process variation can be decreased to ±0.6mV after programming.

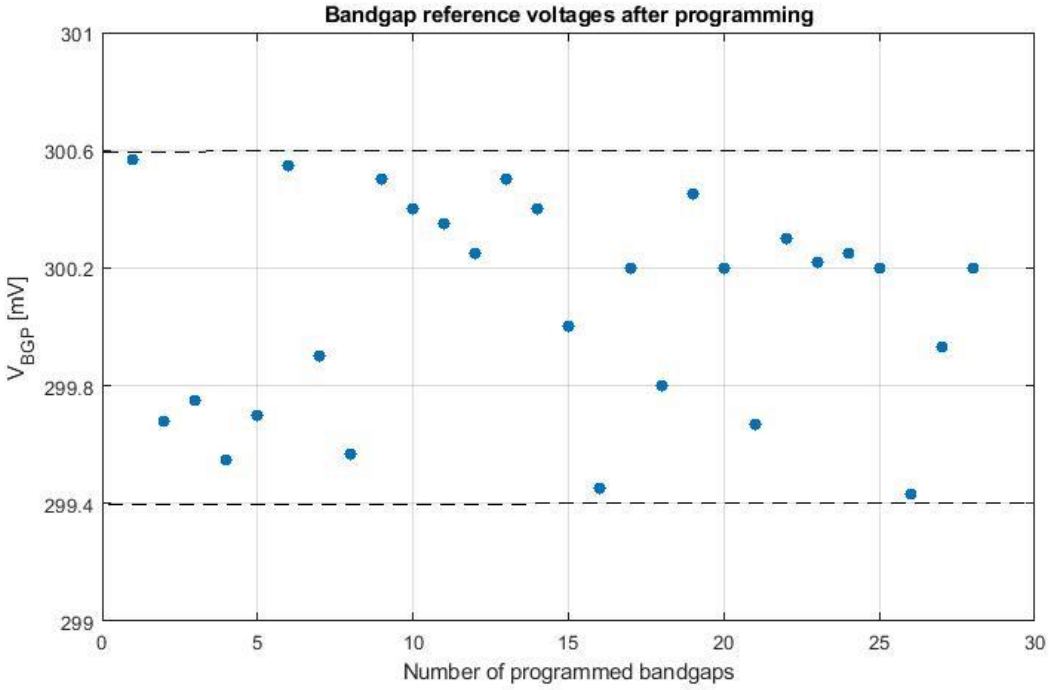

Figure 7.6: Measurement result – Bandgap reference voltages after programming in room temperature. The maximum shift due to mismatch and process variation is decreased to ±0.6mV (7 chips with 28 bandgaps are tested).

The power consumption of the tested chips are compatible with the simulation results. The static CORE current consumption of the chips with four bandgaps is between 850µA and 1050µA and static IO current consumption is about 10µA to 20µA. The IO power current consumption increases during read and programming mode.

In order to test the voltage shift after the programming of each bits, the eFuses are programmed one by one from bit-0 to bit-7, and the voltage change on V_{bgp} is observed. This test was done by using 3 chips, means 12 bandgaps in total.

Table 7.1 lists the mean value and the standard deviation of the voltage shifts after programming for 12 bandgaps, and there is 10 to 20% drop in the voltage shifts compared to simulation results. The measurement results show that the bandgap reference voltages can be programmed with a precision of ±0.6mV when the voltage shift due to radiation, process variation and mismatch is less than ±30mV. Thus, a bandgap voltage at 300mV with an error of less than ±0.6mV is achieved.

Table 7.1 shows the average values of voltage shifts of bandgap voltages after the selected bit was programmed. However, this test was done by programming the eFuses from bit-0 to bit-7. If the programming starts with another bit, and continues with another order, these results may change less than about ±10% due to parasitic resistances of the switches and connection lines. It is not crucial, since the eFuses can be programmed with a precision of ±0.6mV by following the programming procedure explained in Chapter 6.

Bit to Program	Output Voltage (Q) (before/after)	Mean of the Voltage Shifts of BGPs [mV]	Standard Deviation of the Voltage Shifts of BGPs [mV]
7^{th}	0 → 1	-9.91	0.18
6^{th}	0 → 1	-9.92	0.17
5^{th}	0 → 1	-9.91	0.19
4^{th}	1 → 0	+16.32	0.25
3^{rd}	1 → 0	+8.34	0.14
2^{nd}	1 → 0	+4.34	0.07
1^{st}	1 → 0	+2.22	0.06
0^{th}	1 → 0	+1.18	0.05

Table 7.1: Measurement Results - The shift of the bandgap reference voltage after the selected bit was programmed (3 chips with 12 bandgaps are tested).

Three chips with 12 bandgaps were tested at room temperature with different power supply voltages. According to simulation results, if the VddCORE decreases from 1.2V to 0.9V, there is about 0.5mV drop in the bandgap voltage. Figure 7.7 shows that the maximum voltage drop when VddCORE is decreased from 1.2V to 0.9V is less than 1mV and the bandgaps continue to work fine even at a power supply voltage of 0.7V, and its voltage drop is about less than 3mV from 1.2V to 0.7V. As a

result, the instantaneous voltage drops in the power supply voltage up to 0.7V will not affect the bandgap reference voltage significantly.

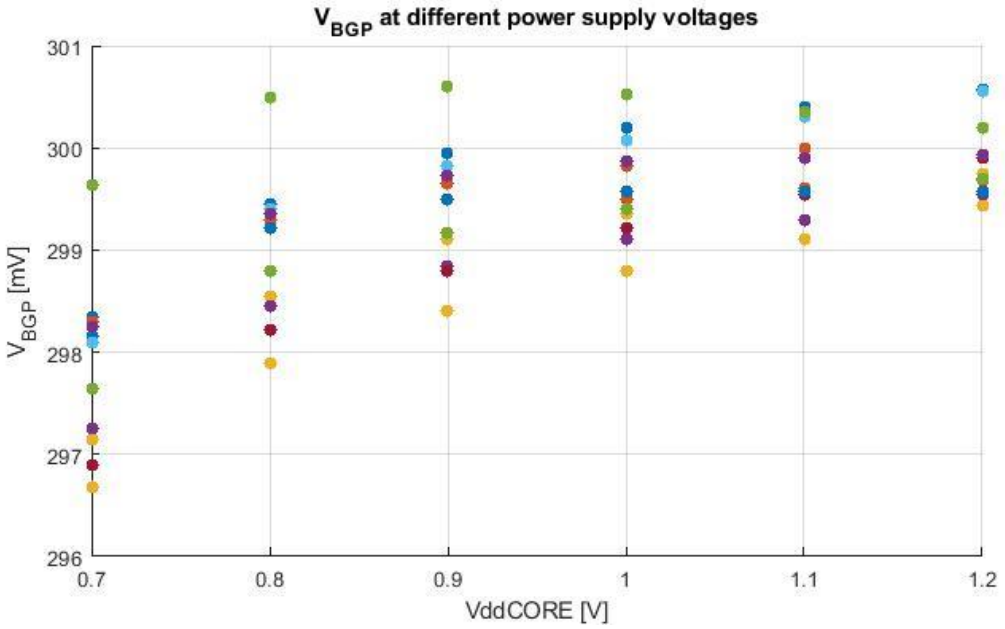

Figure 7.7: The bandgap voltages in room temperature at different power supply voltages (3 chips with 12 bandgaps are tested).

7.3 TEMPERATURE CHARACTERISTICS OF THE BANDGAP

Temperature characteristics of two chips were tested in a climatic chamber from -30^{0}C to 120^{0}C. The temperature was increased with a step of 0.5^{0}C per minute. In each chip, 3 bandgaps are observed and the measurement results are shown in Figure 7.8.

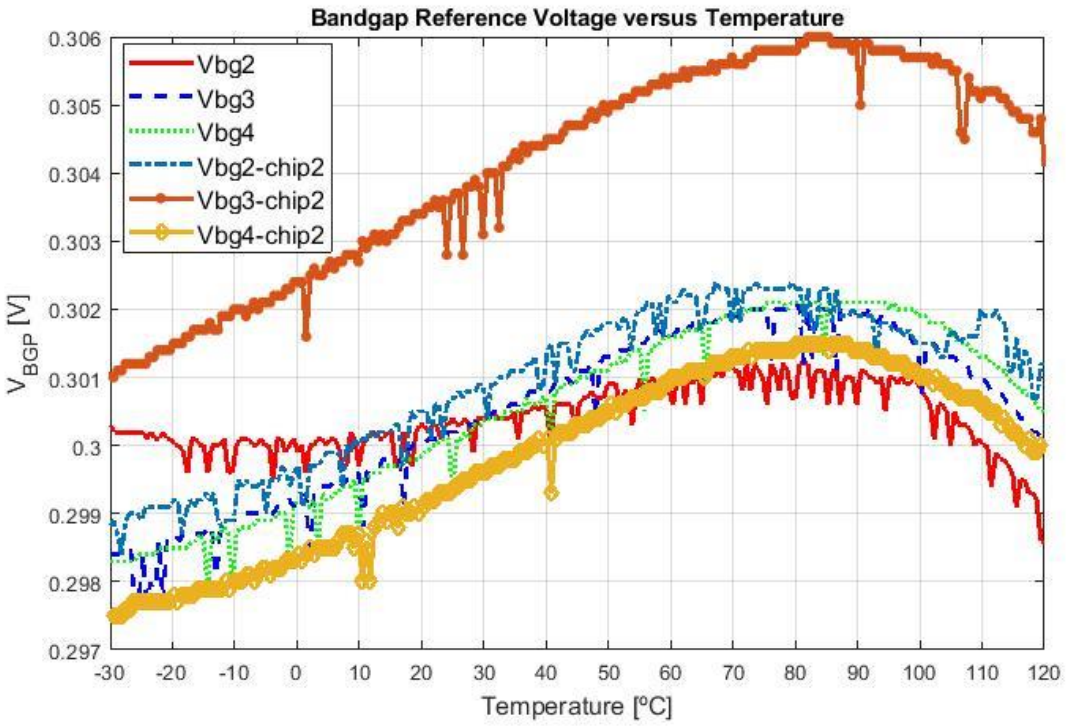

Figure 7.8: Temperature behaviour of bandgap reference voltage (Two chips with 6 bandgaps were tested).

According to simulation results, the voltage shift from -30^{0}C to 100^{0}C was 7.2mV as shown in Figure 3.4 and the bandgap voltage behaved like CTAT, which means it always decreases in temperature from -30^{0}C to 100^{0}C.

On the other hand, measurement results show that the bandgap voltage increases from -30^{0}C to 80^{0}C and it starts to decrease afterwards. The voltage shift from -30^{0}C to 120^{0}C is about 5mV which is better than simulation results.

7.4 OVER-TEMPERATURE PROTECTION SYSTEM'S RESULTS

Over-temperature protection system consists of an Over-Temperature Protection block and a Temperature Monitor block. The measurement results of these two blocks are shown in the following two parts.

7.4.1 OVER-TEMPERATURE PROTECTION BLOCK

According to the simulation results, OTP becomes logic-high at 100^{0}C and logic-low at 70^{0}C under nominal conditions. When the Shift_Up is logic-high, OTP becomes logic-high at 130^{0}C and logic-low at 100^{0}C. However, Figure 5.4 and Figure 5.5 show that the rising and falling edge temperatures of the OTP signal and its hysteresis shift significantly due to radiation, mismatch and process variation.

Measurement results confirm the variation of the OTP signal due to mismatch. Furthermore, both rising and falling edges of OTP shift to the lower temperatures. Figure 7.9 shows the measured OTP signals of two different chips. Firstly, the rising and falling edge temperatures of the OTP signals shift about 25^{0}C - 30^{0}C to the lower temperatures. Secondly, the hysteresis of the OTP signal decreased for both chips, but it is more than 17^{0}C for both chips. This is mainly due to mismatch problem that will be corrected in the following version.

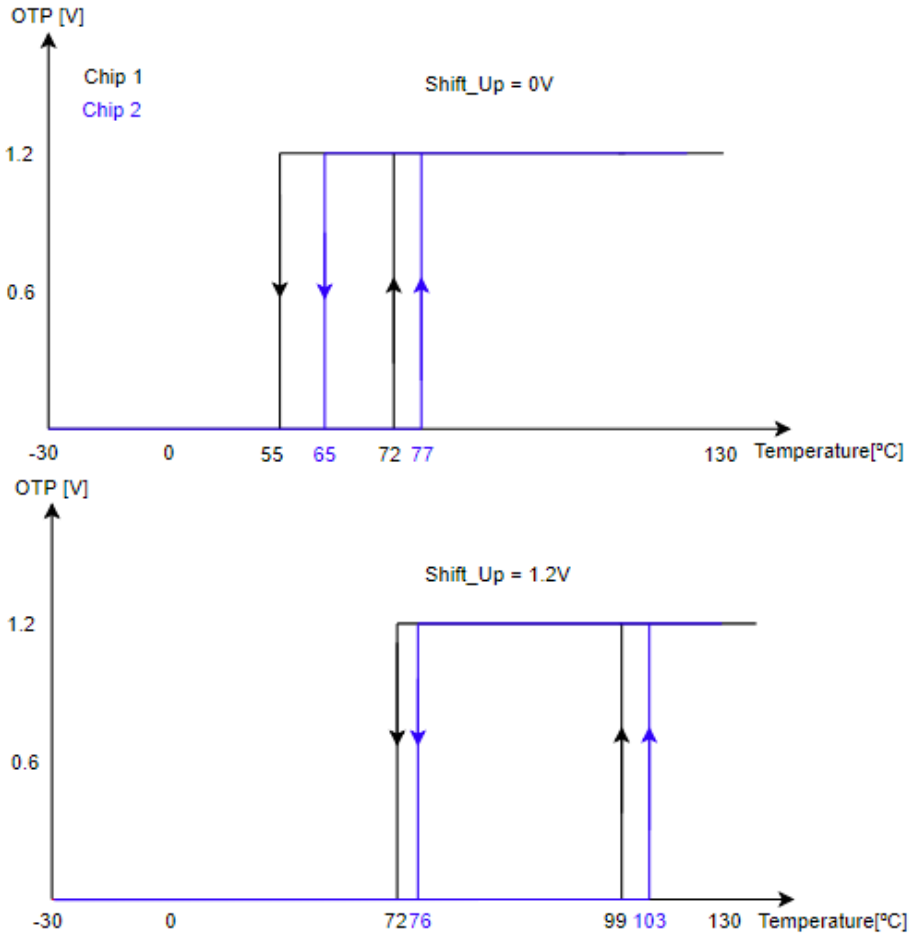

Figure 7.9: OTP signals in temperature for 2 chips. Upper graph is for the nominal and lower graph is for shifted-up version.

7.4.2 TEMPERATURE MONITOR BLOCK

To test the temperature monitor block, a full characterization was done for a single chip in the climatic chamber from -30^{0}C to 120^{0}C. The temperature was increased in 0.5^{0}C per minute. Figure 7.10 shows that the temperature is saturated before -20^{0}C and after this temperature, PTAT_amp starts to increase. It increases linearly as in simulation results; however, it shifted significantly due to mismatch. In addition to that, if the bandgap voltage is trimmed, these PTAT_amp signal shifts completely, since it was generated by comparing in+ and V_{bgp} signals.

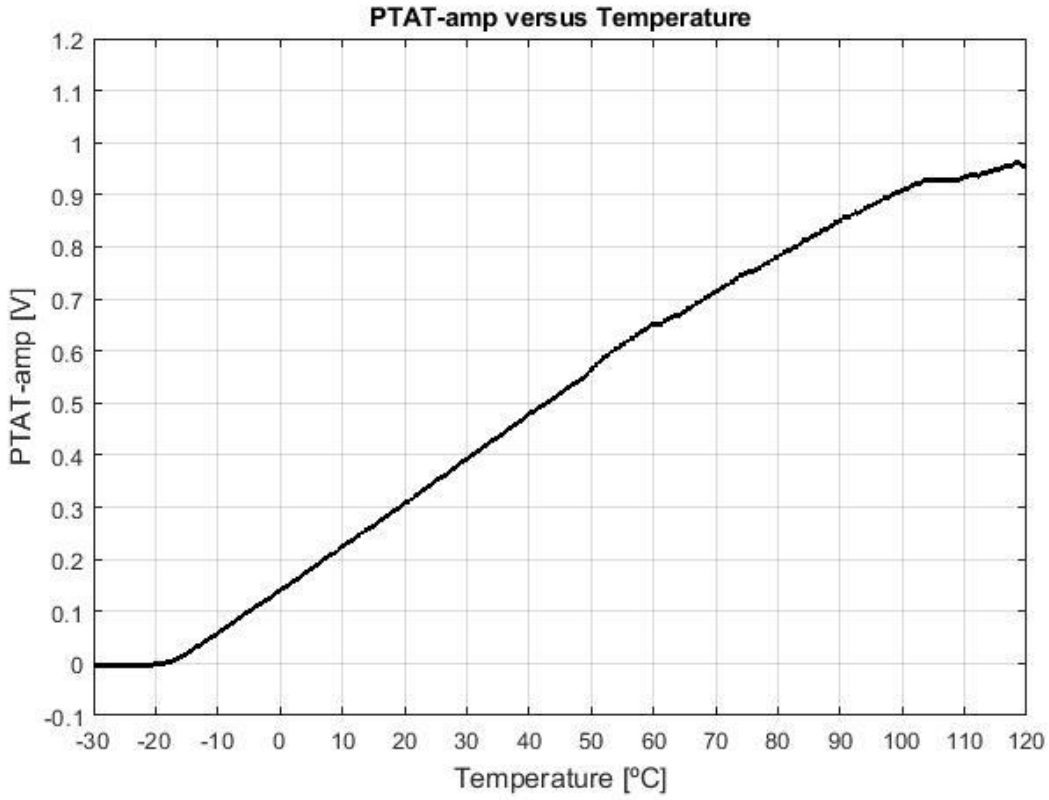

Figure 7.10: Measured PTAT_amp signal to monitor the temperature inside the chip.

To test additional chips, the oven was used only to increase the temperature. Thus, the behaviour of the chips below room temperature could not be analyzed. Figure 7.11 shows PTAT_amp signals of two different chips and this signal in the simulation results. The slopes of PTAT_amp signals are similar to the simulation result, however the values of PTAT_amp signals are shifted down by different amounts at same temperature mainly due to mismatch. These measurement results are compatible with the mismatch and corner simulations. The most significant specification of the temperature monitor is that PTAT_amp has to increase in temperature with a constant slope. Measurement results show that its slope is constant and almost identical with the simulation results. To have a full linear region from -30^{0}C to 120^{0}C in any mismatch case and process corner, the block will be modified in the second version.

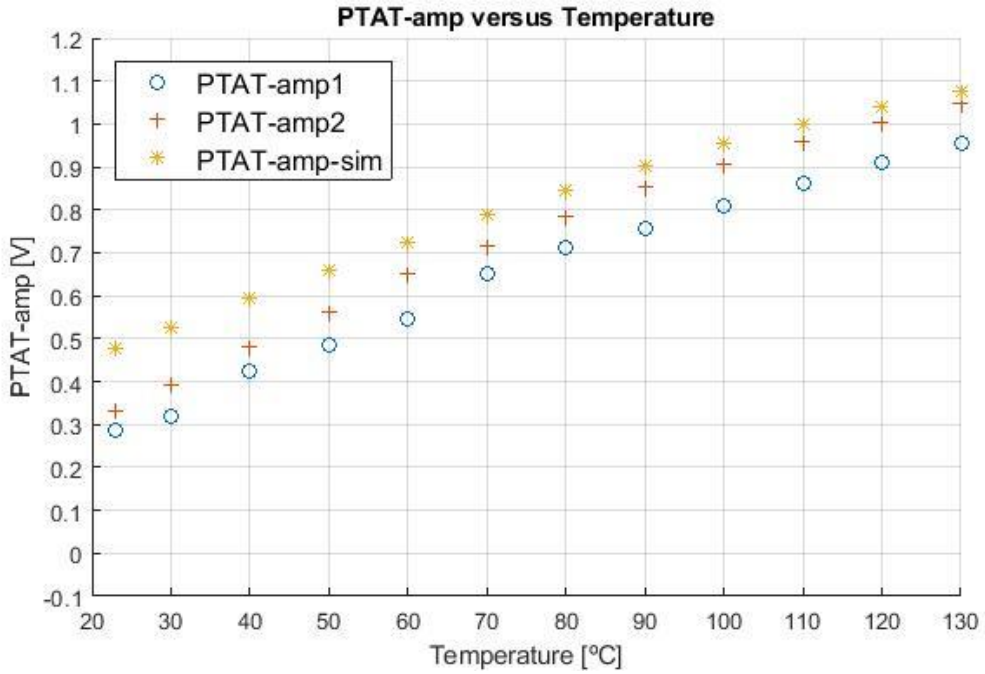

Figure 7.11: Measured PTAT_amp signals to monitor the temperature inside the 2 different chips and comparison with the simulated PTAT_amp signal.

7.5 RADIATION TESTS

As explained in the previous chapters, the ASIC has to work in the radiation environment created by particles' collisions. The radiation tolerance specification is up to 100Mrad in the TID test and also this ASIC must not be affected by SEEs due to heavy ions. In this chapter, the TID and heavy ion test results are represented.

7.5.1 TOTAL IONISING DOSE (TID) TEST

In worst-case scenario, the ASIC will be placed only at 30cm from the collision point, where the calculated TID, over ten years of experiment's life, if equal to 100Mrad. Thus, the maximum average dose rate is about 1140 rad/hour.

To have a safety factor, the ASIC was irradiated in room temperature up to 200Mrad. In order to test the ASIC up to 200Mrad in a reasonable time (20-24 hours), a much higher dose rate of 9.85Mrad/hour was used. Since there were no more available places in the X-ray machine, we could not irradiate a second chip at -30^{0}C.

The measurement results in Figure 7.12 shows that the values of four bandgap voltages decrease about 1.6mV up to 80Mrad and after that, they start to increase. The maximum variation in radiation up to 200Mrad is less than ±1.6mV and it shows that the circuit is perfectly TID radiation-hardened. This confirms that the values of the eFuses' outputs do not change with TID irradiation.

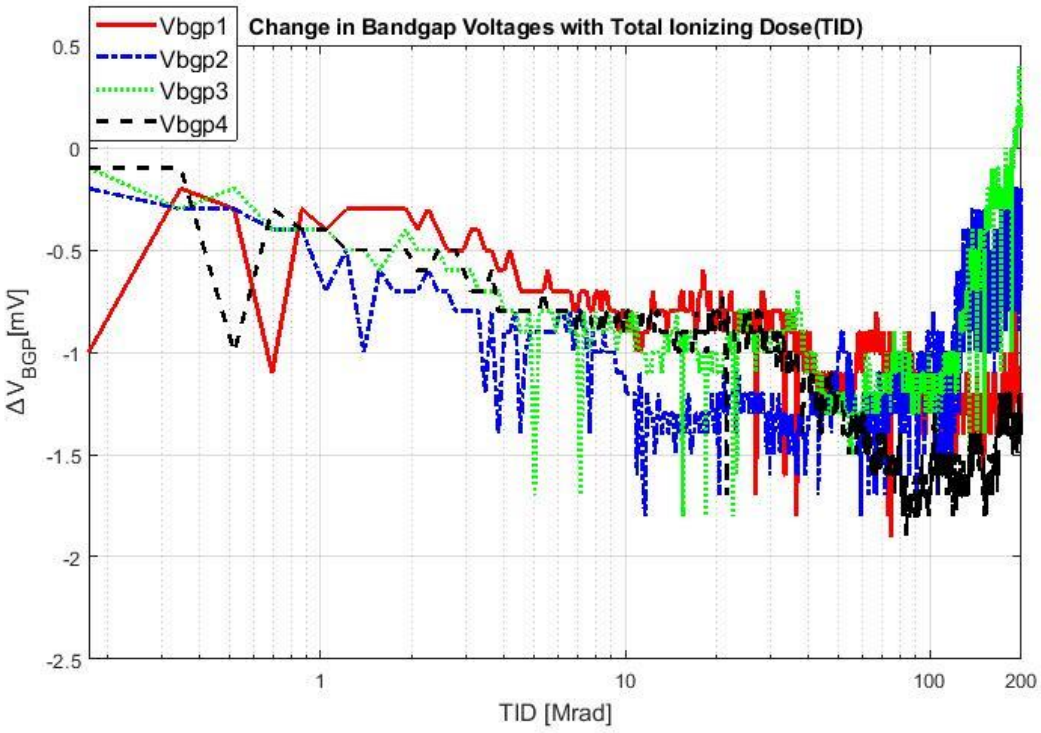

Figure 7.12: Four bandgap voltages in a single chip versus TID at room temperature, with a dose rate of 9.85Mrad/hour.

Figure 7.13 shows the PTAT_amp signal in radiation up to 200Mrad. PTAT_amp signal has to stay constant at a given temperature; however, it increases about 60mV under radiation. The increase in PTAT_amp was expected, because the bandgap voltage, Vbgp1, decreases about 1.4mV up to 200Mrad, and since this drop is amplified by a factor of 30 in the Temperature Monitor part, it increases the PTAT_amp voltage at about 42mV in nominal process corner and mismatch. In the second version of the Temperature Monitor block, it will be amplified by a factor of 5 and the increase of PTAT_amp under irradiation is expected to be less than 10mV.

The TID measurement results show that the chip works properly under radiation up to 200Mrad.

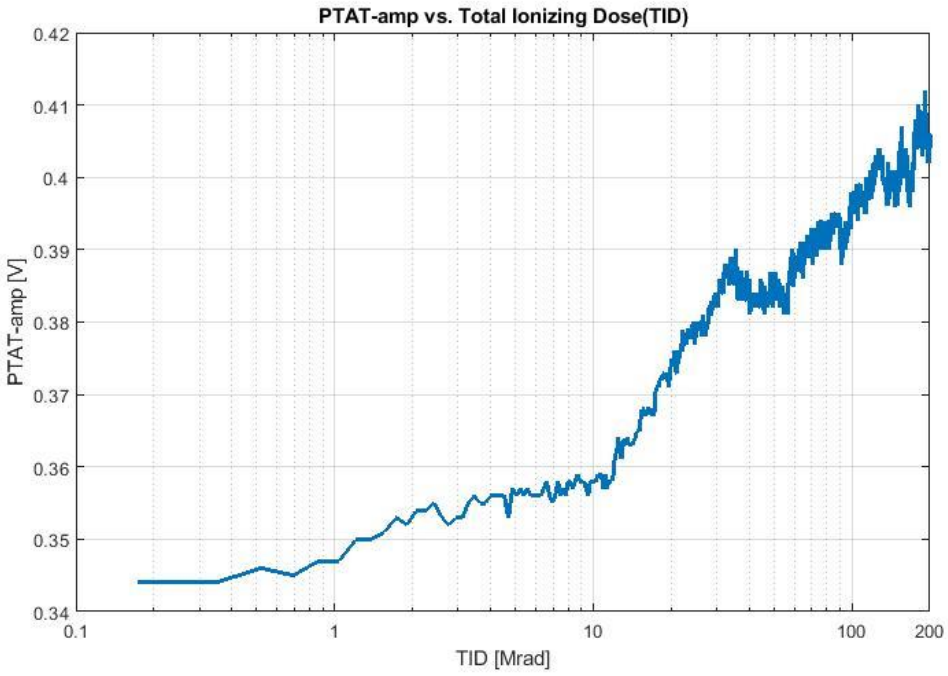

Figure 7.13: PTAT_amp signal versus TID at room temperature, with a dose rate of 9.85Mrad/hour.

7.5.2 HEAVY IONS TEST

The experiment's particle environment is dominated by the presence of high-energy hadrons, thus the sensitivity of the chip to SEEs was tested.

To estimate the maximum linear energy transfer, LET, in the LHC experiment upgrades, worst case is assumed as fission of the tungsten used in tiny amounts in the metallization stack in the chips. This worst case is an extremely rare event and can generate fragments with an LET up to 40 $MeVcm^2mg^{-1}$. Thus, the ASIC was tested in a worse case than the worst possible case in LHC Experiment Upgrades.

Heavy ions irradiation tests have been performed at CRC (Centre de Recherche du Cyclotron in Louvain-la-Neuve) in Belgium. The Rhodium ion with an LET of 50 $MeVcm^2mg^{-1}$ was used to irradiate the circuit with an effective LET of more than 40 $MeVcm^2mg^{-1}$.

Firstly, a heavy ion irradiation with Rh ions and with a fluence of 4 million ions/cm^2 has been done. During the irradiation, no shifts in the four bandgap voltages are observed. After the irradiation, FuseOut<7:0> signals are measured to see if there was a permanent error in the eFuses due to heavy ions. There was not any permanent error in the eFuses and in the bandgaps. Then, a second irradiation with a fluence of 6 million ions/cm^2 was done, and there was no change neither in the bandgap reference voltages nor in the eFuses' outputs. .

In case of a single event, XOR3 signal becomes logic-high for a few nanoseconds and READ_bar and CLK_sum signals become logic-low and logic-high respectively for a few tens of nanoseconds. The test system was noisy, and the changes in these signals could not be observed by oscilloscope, since they changes in nanosecond range. However, it can be concluded that the chip works well under heavy ions and is robust against SEEs, since 10 million ions/ cm^2 were applied, and no change on the bandgap voltages was observed.

CHAPTER 8
SECOND VERSION OF THE CHIP

After the first version of the chip was submitted for tape-out, a second version with several upgrades was designed. This designed ASIC called as BGP will be used to provide a precise bandgap reference voltage to another chip called as bPOL12V that was designed in another technology. Thus, it will be wire-bonded on top of bPOL12V chip as shown in Figure 8.1. This chip has strict area constraints to fit on the free area of bPOL12V. The number of pads was reduced as much as possible, since they consume the area significantly. Furthermore, only IO power supply voltage, VddIO, has to be applied externally, therefore core power supply voltage, VddCORE, was generated internally.

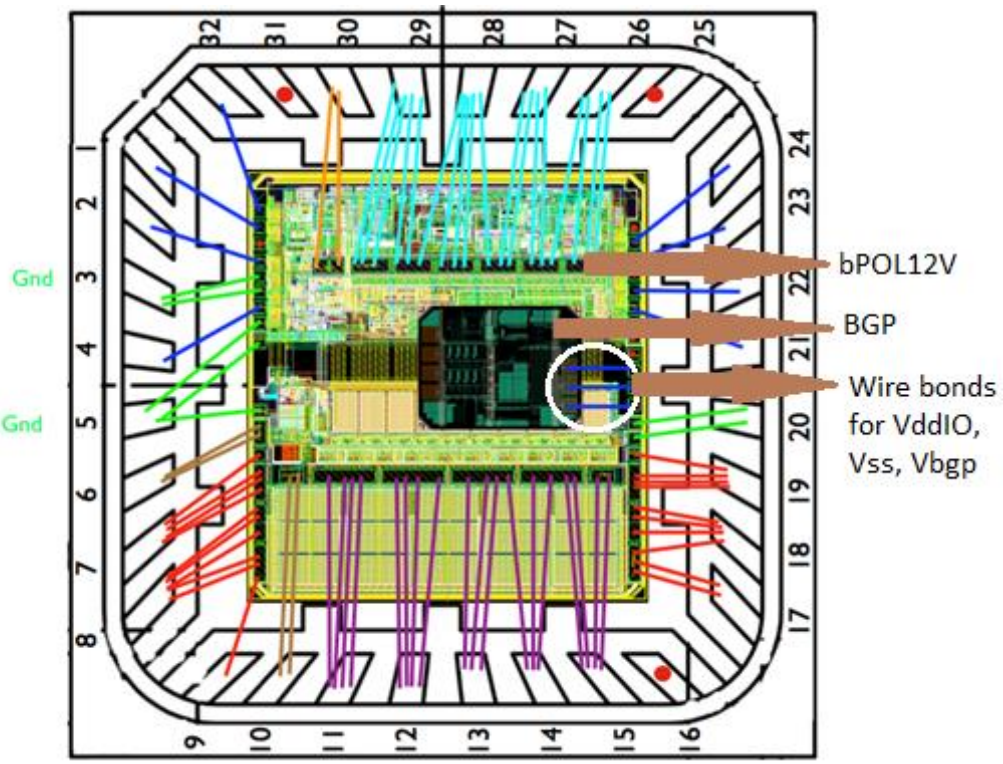

Figure 8.1: The second version of the chip called as BGP will be wire-bonded on top of the other chip, bPOL12V.

Three pads for the power voltages, VddIO, Vss, and output voltage, V_{bgp}, are present on the right side of the chip, and they will be wire-bonded on top of bPOL12V as shown in Figure 8.1. On the left side of the chip, there are four pads to program the eFuses before wire-bonding. These are PROG and 3-bit Address signals.

The schematic of the second version of the chip is shown in Figure 8.2. The main modifications can be expressed as follows:

1. A linear regulator to generate VddCORE internally was integrated into the chip.
2. To decrease the number of pads as much as possible, a read and clock generator block was designed to read and store the data in every power cycle and also after every programming signal. These signals are generated with delay cells as it will be explained later.

3. In the first version of the chip, READ signal was applied to eight 1-bit eFuses simultaneously, and it was drawing current about 7mA. Since VddIO will be connected to the output of the linear regulator of bPOL12V, and an instantaneous current consumption of 7mA may drop the VddIO about 0.8 – 0.9V. This is due to the fact that the linear regulator has output capacitor on chip only, and this capacitance is 600pF. To avoid this situation, eight READ signals are applied to the 1-bit eFuse blocks one by one, and the maximum drop of VddIO becomes less than 0.2V. CLK signal is applied to all the eFuses simultaneously, because it does not cause high current consumption from VddIO.
4. An Enable block was designed to enable the chip, and also READ and CLK generator only when the VddIO and VddCORE power supply voltages and BGP_IO voltage are sufficiently high.
5. A bandgap voltage reference in IO domain, BGP_IO, is integrated into the chip to supply several levels of reference voltages to the Enable block, linear regulator and READ and CLK generator. This voltage reference is not trimmed as we do not need very high precision. We can cope with the variation of the bandgap value.
6. A current generator block was integrated in the layout to supply the required currents for the operational amplifiers and comparators in the new blocks.

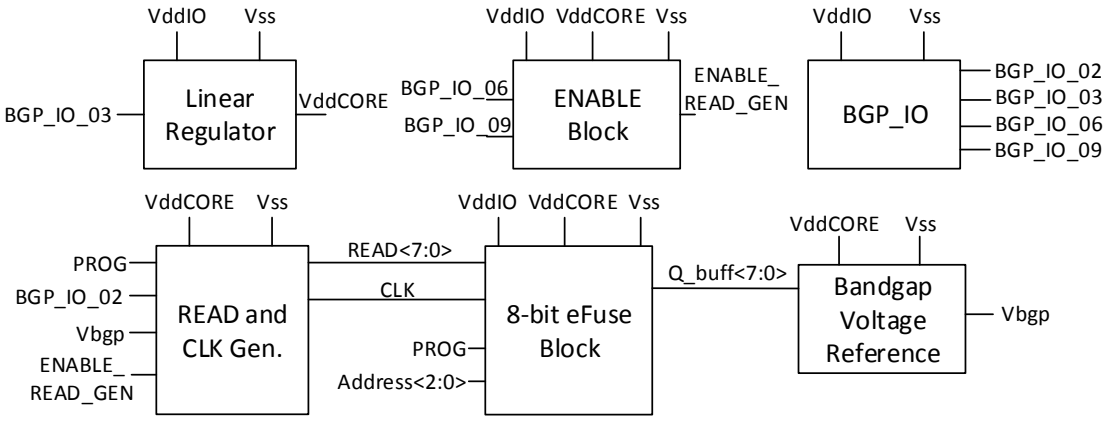

Figure 8.2: Schematic of the second version of the chip.

The designed blocks with their working principles and simulation results will be explained in the sub-sections of this chapter.

8.1 ENABLE BLOCK

An Enable block was developed to enable the chip when VddIO, VddCORE and BGP_IO voltages are high enough to ensure proper biasing of all the circuits. When Enable block provides signal logic-high, this triggers the READ and CLK generator and eFuses' outputs are read and stored.

Enable block has four comparators to monitor VddIO, VddCORE and BGP_IO. The schematic of the block can be seen in Figure 8.3 and the nominal simulation results of the internal signals can be observed in Figure 8.4.

Initially, TURNON1, TURNON2 and CLAMP signals are pulled down to ground by the resistors R5, R8 and R14 respectively.

First comparator checks if VddIO is higher than 0.9V. A diode-connected NMOS transistor, M1, and the resistance R1 generate NET1, and a basic voltage divider consists of R2, R3 and R4 generates V+ signal. M1 is off until its gate voltage higher than its threshold voltage (about 620mV), and NET1 is exactly same with VddIO until 620mV, since there is no current flow and voltage drop on R1. After its gate voltage becomes higher than its threshold voltage, 620mV, M1 transits to saturation mode, and NET1 saturates to 0.9V. Since V+ is generated by a voltage divider consists of only resistors, V+ increases linearly up to 1.3V and at some point it crosses the value of NET1 signal. When the value of V+ is larger than 0.9V, TURNON1 becomes logic-high and OUT_INV1 becomes logic-low. Since OUT_INV1 becomes logic-low, it adds the resistance R4 to the V+ node and the value of V+ suddenly increases about 80mV. This sudden increase in voltage ensures that TURNON1 does not change due to voltage spikes on V+ or NET1 nodes, because the voltage difference between them are increased right after OUT_INV1 became logic-low.

Second comparator checks if the BGP_IO_09 voltage created in BGP_IO block is higher than the value of NET2, which is 0.8V. BGP_IO_09 voltage increases slowly up to 0.9V, and when it crosses the value of NET2, 0.8V, TURNON2 signal becomes logic-high and TURNON2 signal turns the PMOS switch,M4, off. Thus, the resistance R6 is added to the branch of NET2 and the value of NET2 decreases about 20mV. This voltage drop ensures that TURNON2 will not change due to voltage spikes on BGP_IO_09 or NET2 nodes.

Third comparator checks if VddCORE is higher than 1.05V. When the voltage on NET3 becomes larger than BGP_IO_06 signal that is at 600mV, then VddCORE_OK becomes logic-high.

In order to be sure that VddIO is very close to its nominal value, 2.5V, the TURNON2 signal is delayed about 20μs and TURNON2_delayed signal is generated. TURNON2_delayed and TURNON1 signals are applied to the inputs of an AND gate and the final TURNON signal is generated.

This logic-high TURNON signal clamps the fourth comparator to VddIO and CLAMP and CLAMP_INV signals become logic-high and logic-low respectively. When the CLAMP_INV becomes logic-low, first two comparators are clamped to VddIO and TURNON1 and TURNON2 remain always logic-high. The purpose of the fourth comparator is to clamp the first two comparators to be sure that TURNON1 and TURNON2 do not change in case of a SEU. Since they are clamped to VddIO, they will be always logic-high until the next power cycle.

Lastly, TURNON and VddCORE_OK signals are connected to the inputs of an AND gate, and when both are logic-high, ENABLE_READ_GEN becomes logic-high and it allows to generate READ and CLK signals. The capacitors C1, C2, C3 and C4 are connected to the critical nodes to be safe against SEU. Furthermore, additional capacitors are connected to TURNON2_delayed, TURNON and ENABLE_READ_GEN blocks. The values of the capacitors are adjusted by simulating single event effects by injecting currents on the critical nodes.

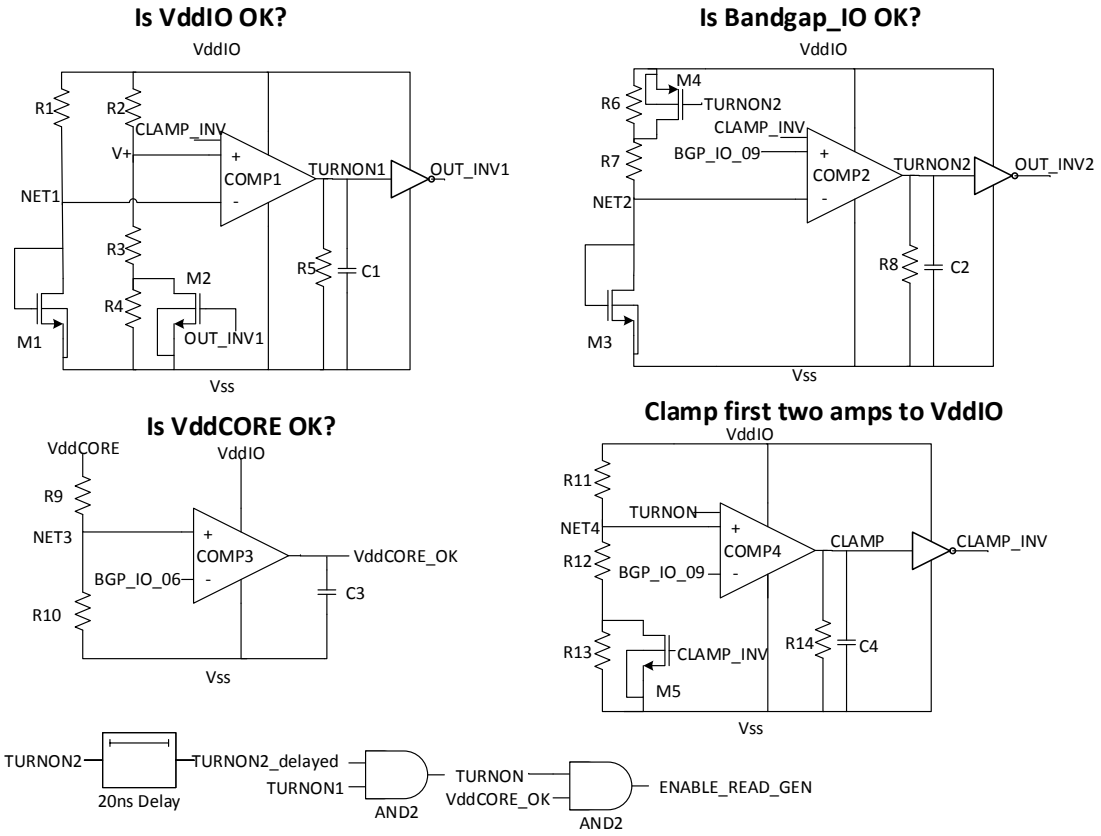

Figure 8.3: Schematic of the Enable block to enable the chip when the VddIO, VddCORE and BGP_IO are sufficiently high.

Simulation results for nominal corners are shown in Figure 8.4. Process and radiation corner simulations and Monte Carlo simulations for mismatch are performed. The chip works properly at every corner and in all mismatch scenarios. The only difference is that the enabling time of the chip shifts to a lower or higher time depending on the mismatch, process and radiation corner, however we do not care about the speed of these signals.

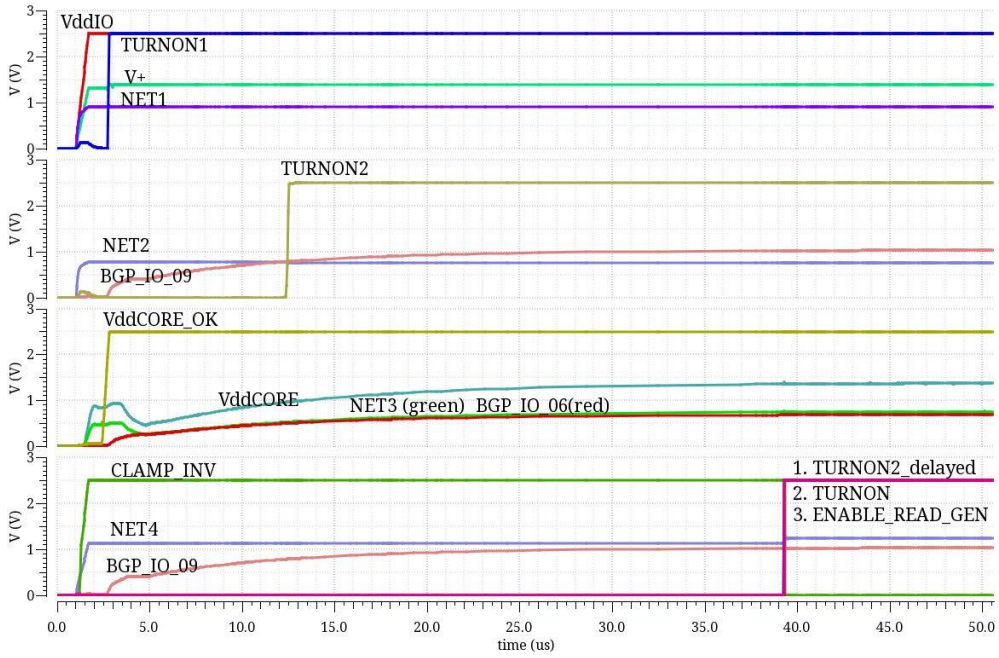

Figure 8.4: Nominal simulation results of the Enable Block and internal signals.

8.2 READ AND CLOCK GENERATOR

This block was designed to generate READ and CLK signals internally, in every power cycle and after the PROG signal was applied. It applies separate 8-bit READ signal, and common CLK signal to the eight 1-bit eFuse blocks.

The READ and CLK generator creates 8-bit READ signals and then a 1-bit CLK signal. READ signals are generated with a delay of 1.2µs between them, because VddIO voltage is generated by a linear regulator, and high current consumption during the READ phase results in an instantaneous voltage drop on VddIO. Since the linear regulator regulates the voltage with a frequency of about 1MHz, a delay more than 1µs was set between read signals. In order to reduce the current consumption in a 1µs period, the READ signals are applied to the eFuses one by one with a period of 1.2µs.

Firstly, a Pulse Generator block was designed to generate single READ and CLK pulse signals by following the minimum timing rules listed in Table 4.3. To be in safe region in every process and radiation corners, the timing parameters are chosen as t_{READ}=63ns, t_{CLK}=12ns and t_{READ_CLK}=24ns.

The Pulse Generator block is shown in Figure 8.5. The TRIGGER signal is the input of this block and when it becomes logic-high, it is delayed 63ns and NET3 signal, that is the delayed version of the TRIGGER, is created. A high resistive inverter, INV3, inverts this NET3 signal and NET4 is generated. By applying NET4 and TRIGGER signals to an AND gate, the READ_initial pulse is generated. For the delay cells, a low current at about 2µA is applied to the drain of the NMOS transistor and a highly resistive inverter was used to decrease the cross-conduction current in the NMOS transistor and in the inverter.

By applying same methods, the delay between the falling edge of the READ_initial signal and the rising edge of the CLK_initial signal is generated by R2 and C2, and the pulse width of CLK_initial signal is created by R3 and C3. After the falling edge of the CLK_initial signal, the TRIGGER signal becomes logic-low and waits for the next triggering.

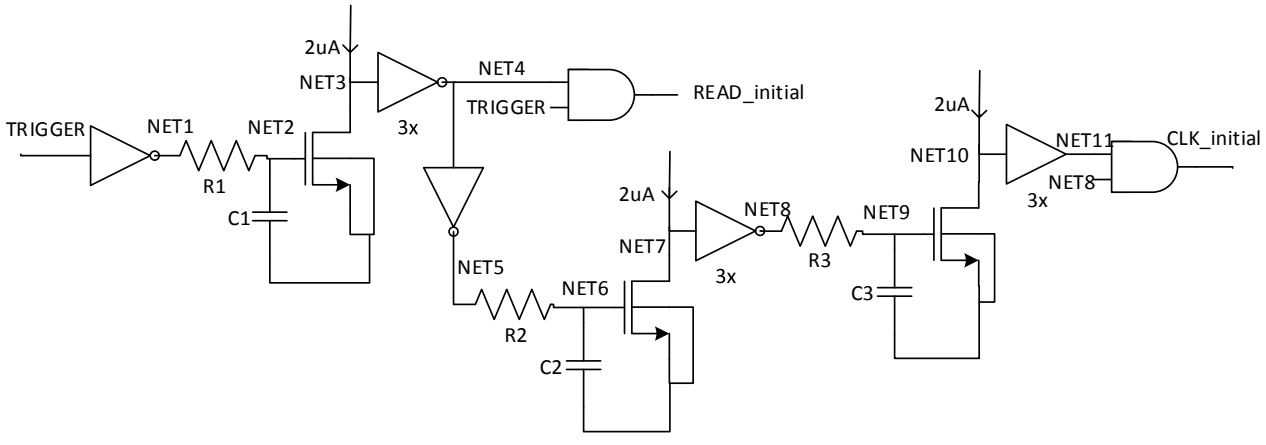

Figure 8.5: Schematic of Pulse Generator showing the delay cells to generate READ and CLK signals.

Figure 8.6 represents the simulation results in nominal corners at room temperature. The timing parameters t_{READ}, t_{CLK} and t_{READ_CLK} were chosen about 80% larger than minimum values, to be sure that it works even in worst case corner in terms of process, radiation and temperature. The Monte

Carlo simulations for mismatch and the process and radiation corner simulations are performed, and we analyzed that this block works properly in every cases.

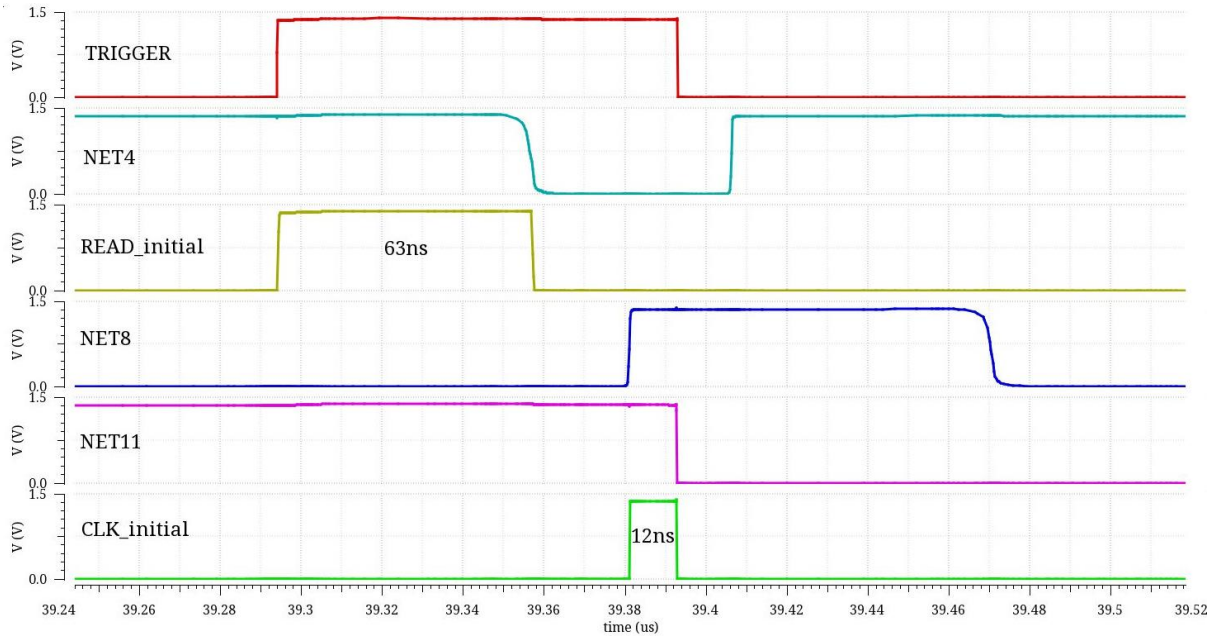

Figure 8.6: Simulation results of Pulse Generator in nominal corner.

After that, the Pulse Generator was integrated to the top-level block of the READ and CLK Generator shown in Figure 8.7. Firstly, when the ENABLE signal becomes logic-high, it enables the comparator. Since $V_{bandgap}$ and BGP_IO_02 signals were already set to their values, the COMP_OUT becomes logic-high and NET1 becomes logic-low. PROG was pulled down and it is always logic-low, unless a PROG signal is applied externally. Thus, NET2 becomes logic-low and TRIGGER becomes logic-high. The rising-edge of the TRIGGER signal triggers the Pulse Generator block and READ_initial and CLK_initial are generated.

The falling edge of the CLK_initial signal triggers the first D-flip flop, and Q1 becomes logic-high and thus TRIGGER becomes logic-low again and waits for the following triggering. Q1_bar goes to logic-low and it is applied to the gate of an NMOS transistor to create a delay about 1.2µs between two read signals. As can been from simulation results in Figure 8.8, when Q1_bar becomes 0V, a very low current of 500ns starts to charge-up the capacitor C1 and NET5 starts to increase slowly. This low current and high capacitance C1 creates about 1.2µs delay and buffered version of NET5 triggers the second D-flip-flop with a delay of 1.2 µs. When the D-flip-flow is triggered, res1_pulse becomes logic-low for only 1ns, since its 1ns delayed version, Reset2, resets the D-flip-flop. This res1_pulse signal makes Reset1 logic-low for 1ns and the Reset1 signal resets the first D-flip-flop. Therefore, Q1 becomes logic-low and triggers the Pulse Generator again to generate the second READ_initial and CLK_initial signals.

In this block, a Counter circuit counts the number of CLK_initial signals. In every CLK_initial signal, CLK_counter triggers the 4-bit Counter block and it counts the number of CLK_initial pulses. Since we need only 8 READ signals for the eFuse block, when Q<3> becomes logic-high, means that 8 READ signals were already created, it keeps the first D-flip-flop reset. Thus, Q1 stays always at 0V

and no more READ_initial and CLK_initial signals are generated. Q<3> also resets the counter and it will start from zero to count the next CLK_initial pulses.

After that, the Decoder generates READ<7:0> signal by following the sequence of the counter and 8 READ signals with a delay of 1.2μs are generated. After 8 CLK_initial signals are counted, the last CLK_initial signal is selected as the final CLK.

In case of a single event in this block, our purpose is that no READ signal will be generated due to SEU, because it increases the power consumption of the circuit. The CLK signal can change instantaneously; it does not influence the power consumption of the circuit.

This block is robust against SEU, because if we can keep the output of the counter, Q<3:0>, as <1000>, no more READ signal can be generated. Since the READ<7:0> signal is connected to the eFuse block, we do not care about READ_initial signal. Since it is not connected to the eFuse cell, it will not affect power consumption of the circuit. In case of a single event, READ_initial and CLK_initial signals may change, however they do not have a significant effect on the power consumption of the block. In order to have a Q<3:0> signal insensitive to SEU, physically triplicated counter and decoder were used. Since Q<3> is kept as logic-high, the CLK_counter signal is independent of CLK_initial, and always logic-high. In addition, some capacitors are connected to the critical nodes, such as CLK_counter, Reset_counter to make the counter insensitive to SEU.

In case of a power cycle, the ENABLE block, explained in 8.1, makes the ENABLE signal logic-high and enable the comparator in READ and CLK Generator. Shortly after a power cycle, the READ<7:0> and CLK signals are generated in this block. Similar to the power cycle case, when the PROG signal is applied, TRIGGER signal becomes logic-high after the falling edge of the PROG signal and same procedure is followed to generate READ<7:0> and CLK signals. Thus, when the chip is switched-on, or when a PROG signal is applied, the eFuse data will be read and stored automatically.

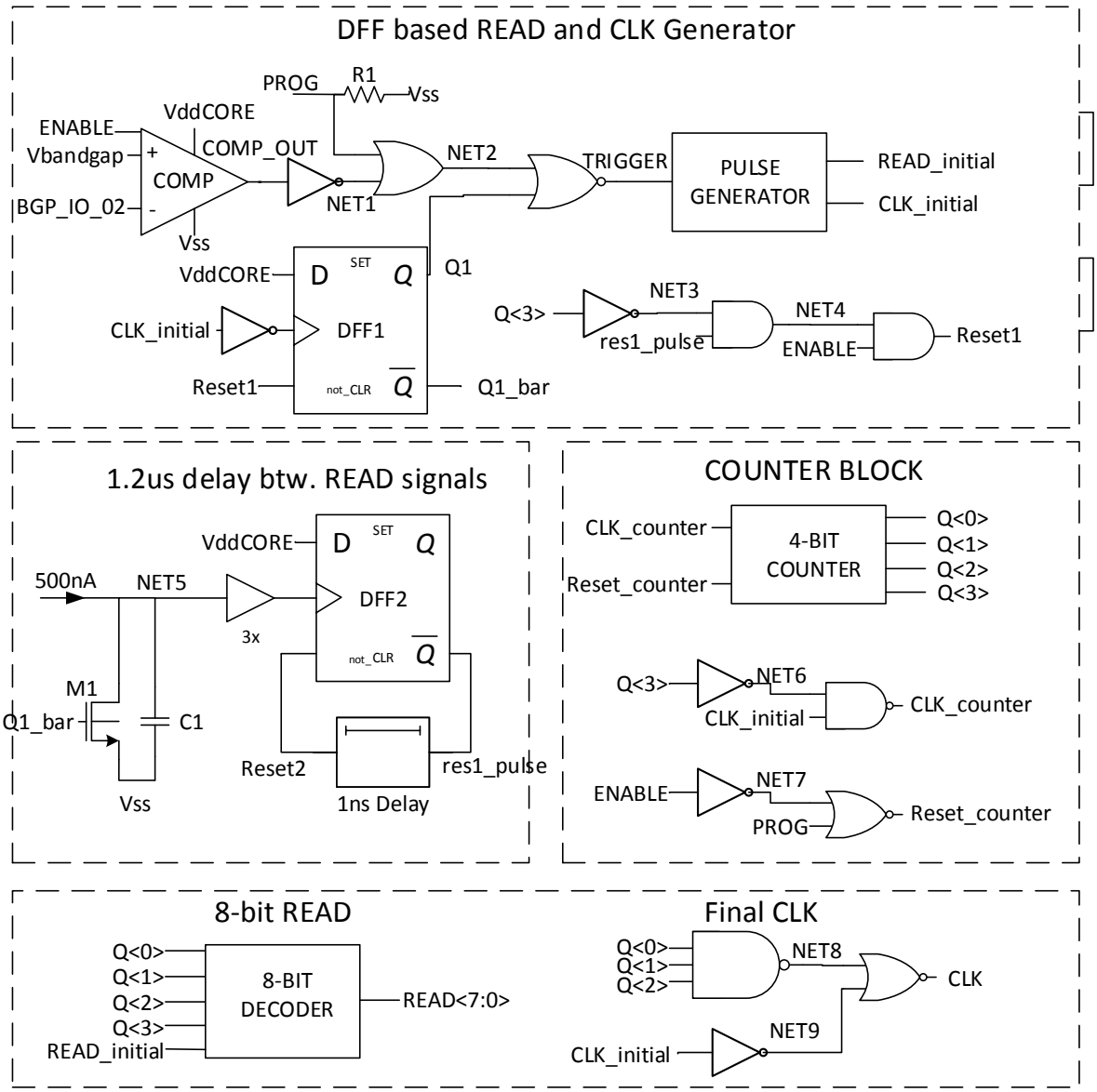

Figure 8.7: Schematic of READ and CLK Generator block. This block generates 8-bit READ signal and 1-bit CLK signal to be applied to the 8-bit eFuse block.

Figure 8.8 shows the simulation results in nominal process, radiation and temperature corners. A Monte Carlo simulation with 200 runs was performed to see the effect of the mismatch to this block. After that, the corner simulations were carried out for process, radiation and temperature. The results show that the READ and CLK signals are generated properly for every corner, and it always respects the timing constraints given in Table 4.3.

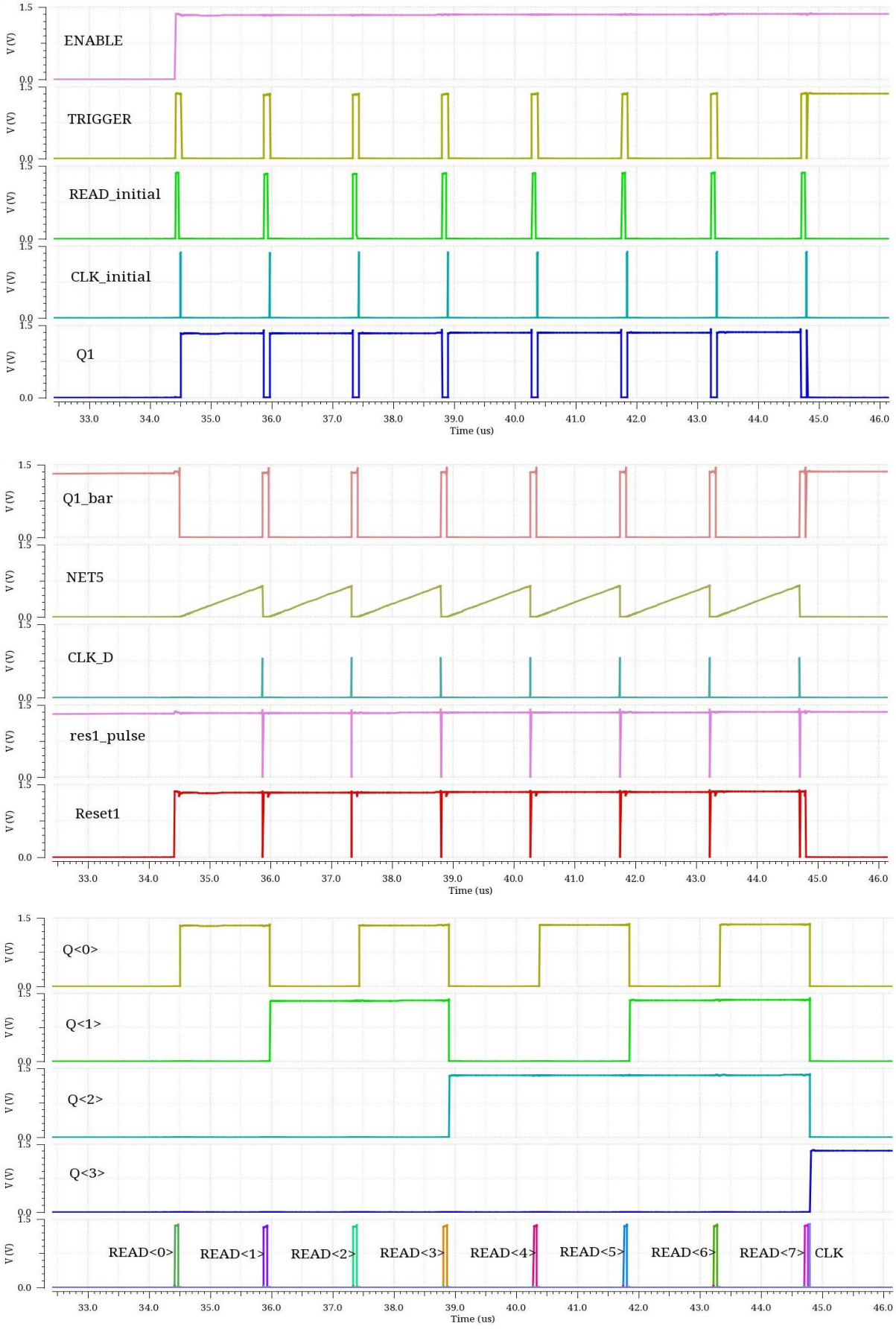

Figure 8.8: Simulation results of the READ and CLK Generator in nominal corner.

8.3 MODIFIED VERSION OF OVER-TEMPERATURE PROTECTION CIRCUIT

In the first version of the Over-Temperature Protection block, the outputs OTP and PTAT_amp changed significantly due to radiation, process variation and mismatch. These signals are generated by comparing the values of in+ and V_{bgp} (Figure 3.3) and in+ and V_{bgp} nodes do not move in same way in mismatch or process variation. Furthermore, if the bandgap is programmed, its value changes and OTP and PTAT_amp signals shift considerably. In order to improve its behaviour in mismatch and process variation, second version of the Over-Temperature Protection circuit was developed.

Firstly, instead of in+ voltage in the bandgap voltage reference, the difference between the in+ and drain voltage of M2 was selected (in+ - V_{dM2}) (Figure 3.3). Since the drain of the DTMOS transistor M2 and the in+ node behave in same way in process variation and mismatch, the difference of their values, means the voltage drop on R2 resistor, V_{R2}, stays constant.

Secondly, V_{bgp} node is selected as the other reference voltage. Since the bandgap will be programmed after manufacture process, its value will always be about 300mV. We obtained the second reference voltage that do not vary in process and mismatch.

By comparing the voltage drop on R2, V_{R2}, with the bandgap reference voltage, V_{bgp}, output signals that do not change significantly with mismatch and process are generated. Figure 8.9 shows the schematic of the modified over-temperature protection circuit and Figure 8.10 shows the simulation results in nominal conditions. Firstly, in+ voltage is subtracted from the drain voltage of M2, V_{dM2}, and this difference is amplified as a factor of two and generates SUBSTRACT voltage. Then the bandgap voltage at 300mV is attenuated to 280mV in REF_BGP node. This node is buffered and subtracted from SUBTRACT node to generate PTAT_amp signal. Since the difference of in+ and V_{dM2} and the bandgap voltage does not shift in process and mismatch significantly, PTAT_amp signal will not vary considerably due to process variation and mismatch.

For the Over Temperature Protection part, the bandgap and PTAT_amp voltages that do not vary in process and mismatch generate the OTP signal. The bandgap voltage at 300mV is amplified to generate V_{bgp_scaled} voltage at 800mV. After that, V_{bgp_scaled} is compared with PTAT_amp and when PTAT_amp is larger than V_{bgp_scaled}, OTP becomes logic-high and shorts the resistor R3. Thus, V_{bgp_scaled} decreases to 660mV as soon as OTP becomes logic-high. When the temperature decreases, PTAT_amp becomes lower than V_{bgp_scaled} at a lower temperature, and OTP becomes logic-low again. This setup creates a hysteresis of 30^0C in the OTP node.

The falling and rising edge temperatures are decreased compared to the first version and they can be shifted-up by the switch parallel to the R2. The main modification in the block is that the voltage difference between in+ and V_{dM2} nodes is selected as reference, since both voltages move in same direction with process and mismatch, and their difference is expected to stay constant.

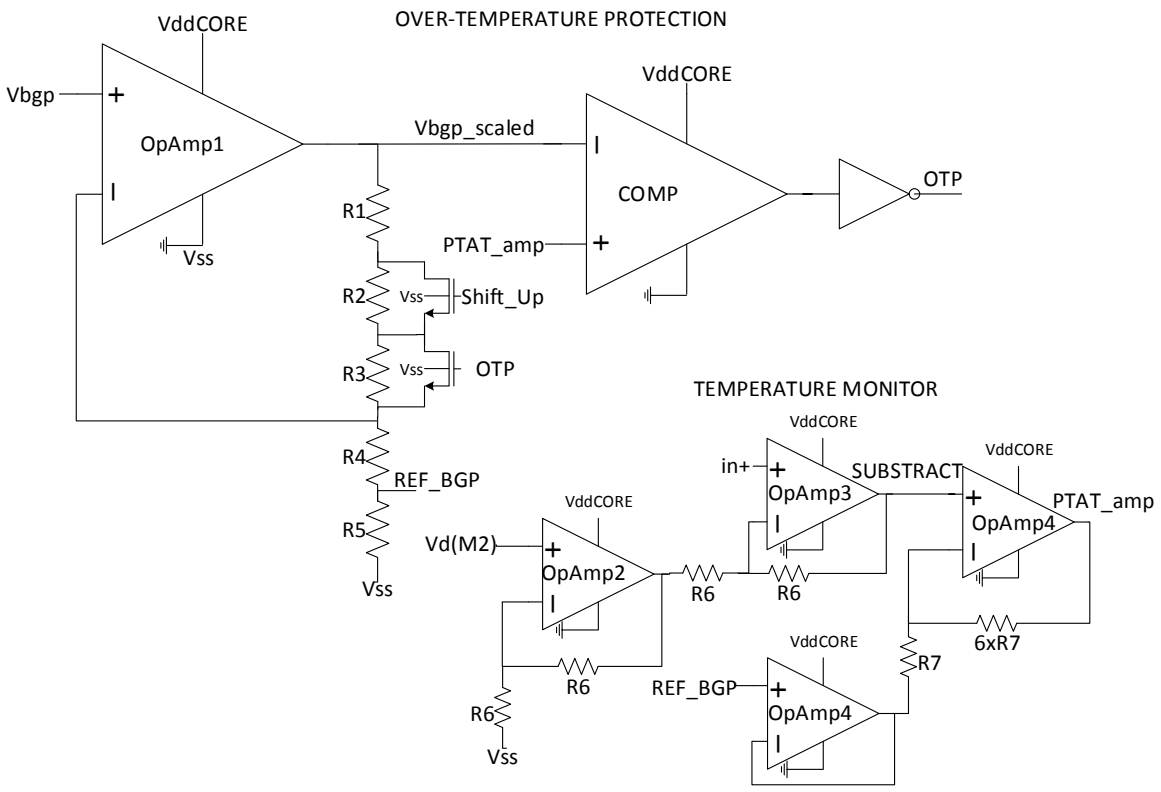

Figure 8.9: Schematic of the modified Over-Temperature Protection block with Temperature Monitor circuit.

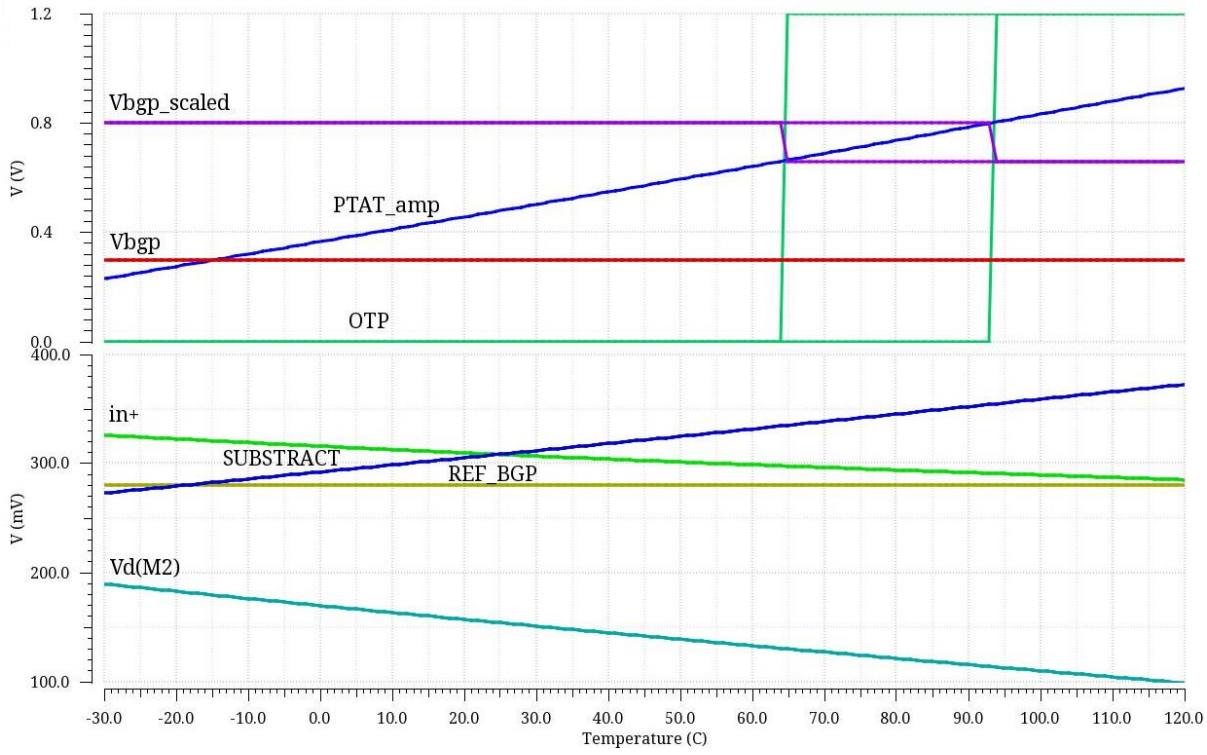

Figure 8.10: Simulation results of the Over-Temperature block in nominal conditions.

Figure 8.11 shows the OTP versus temperature graph in different radiation and process corners, and Figure 8.12 shows the variation of OTP in temperature due to mismatch. In the first version of the

chip, the rising and falling temperatures of OTP shifted about ±40^{0}C and the hysteresis of OTP changed about ±10^{0}C with radiation, process and mismatch (Figure 5.4, Figure 5.5). In the updated version, OTP shifts less than ±25^{0}C and the hysteresis changes only about ±2^{0}C due to radiation, mismatch and process variation. Since the most important specification was the hysteresis of the OTP signal, these simulation results are promising for the second version of the chip.

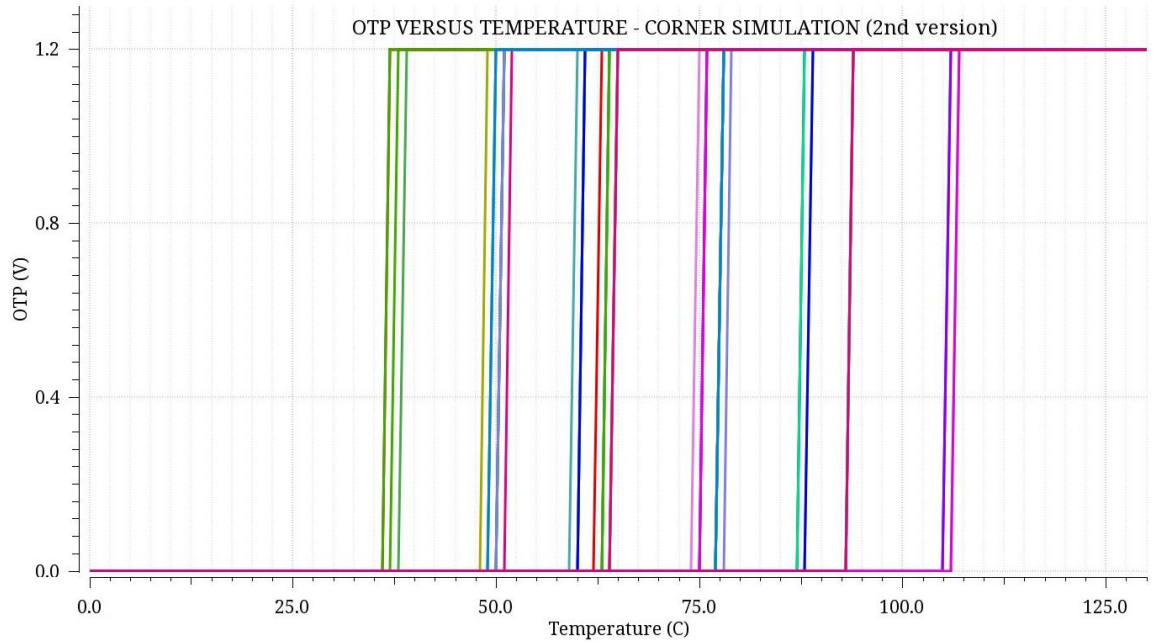

Figure 8.11: OTP versus temperature graph in different process and radiation corners for the second version of the chip. The rising and falling temperatures of OTP shifts about ±25^{o}C and the hysteresis of OTP shifts only about ±2^{o}C in worst case.

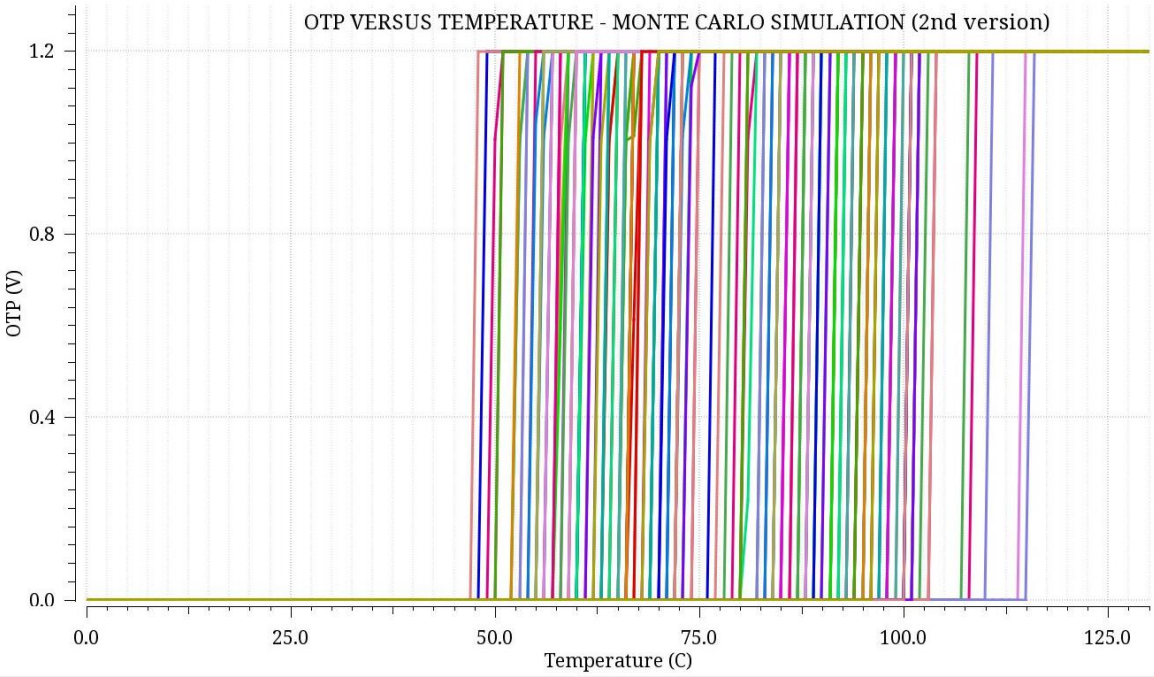

Figure 8.12: Variations of OTP signal due to mismatch, as simulated by Monte Carlo Simulations with 100 runs. The rising and falling temperatures of OTP shifts about ±20^{o}C and the hysteresis of OTP shifts about ±2^{o}C in worst case.

Figure 8.13 shows the PTAT_amp versus temperature graph in different radiation and process corners, and Figure 8.14 shows the variation of PTAT_amp in temperature due to mismatch. Compared to first version of the chip, the slope of the PTAT_signal in temperature is almost same and constant at different radiation and process corners and it does not change due to mismatch. We can conclude that PTAT_amp signal increases linearly with temperature and its slope is constant at all the radiation and process corners and also in case any of a mismatch. Since the most important specification for this block was that PTAT_amp increases linearly in temperature with a constant slope, these simulation results are promising for the second version of the chip.

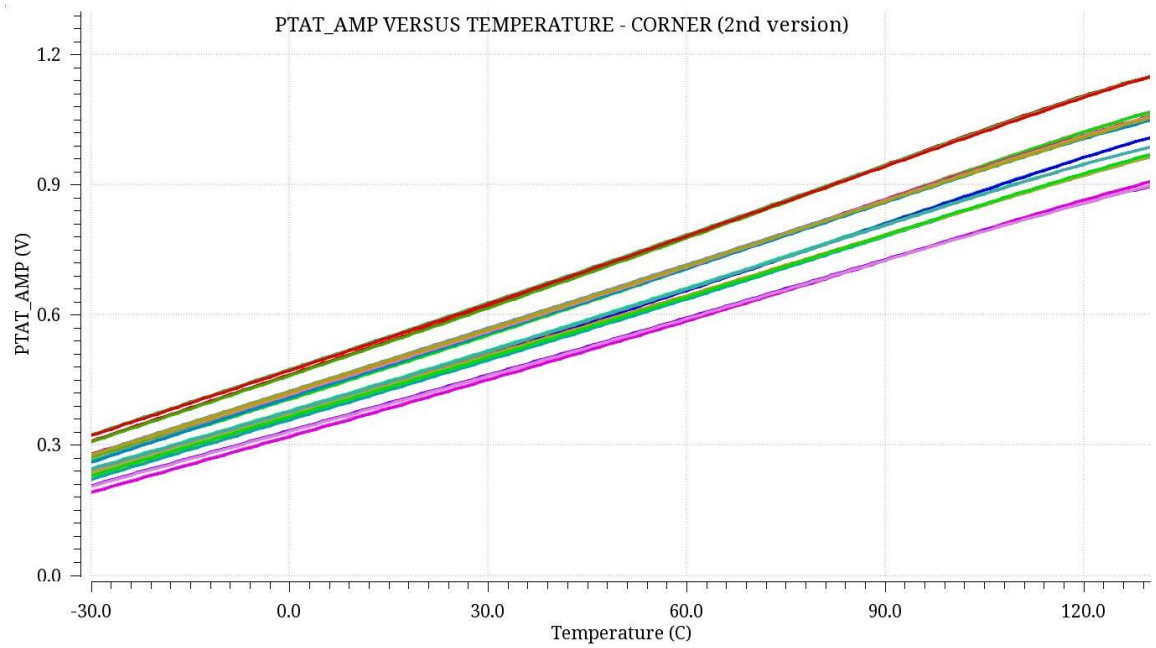

Figure 8.13: PTAT_amp versus temperature graph in different radiation and process corners. PTAT_amp voltage shifts about less than 0.12V in different process and radiation corners and its slope is constant and almost same in any cases.

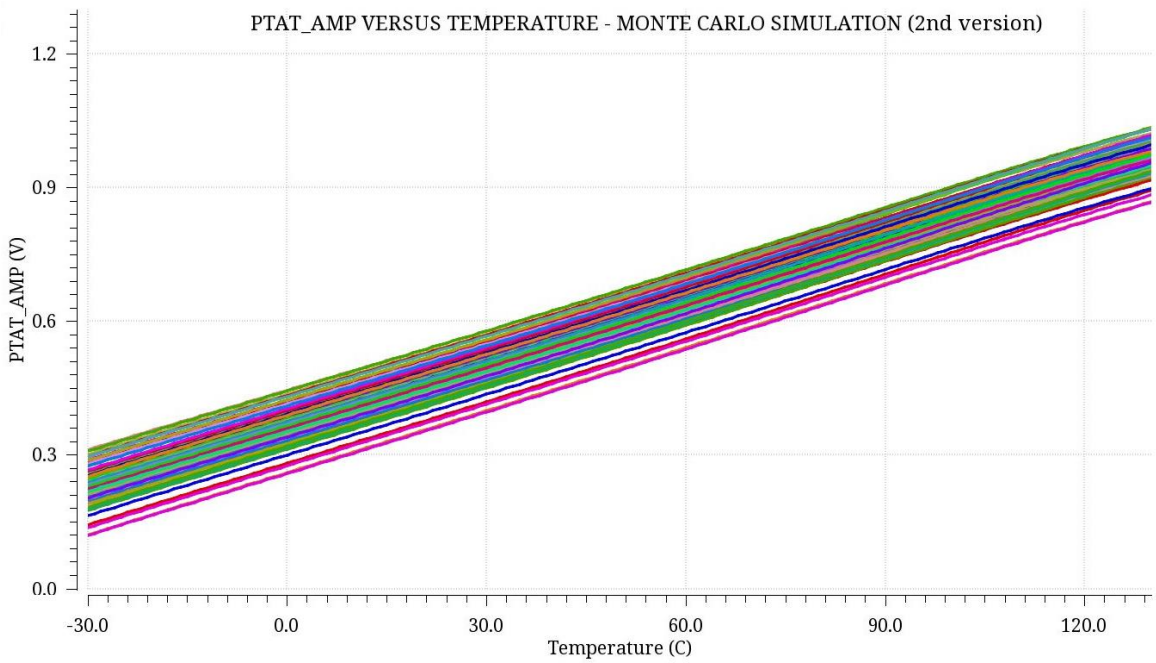

Figure 8.14: Variations of PTAT_amp signal due to mismatch, as simulated by Monte Carlo Simulations with 100 runs. PTAT_amp voltage shifts less than 0.15V and its slope does not change due to mismatch.

8.4 DESIGN OF THE FULL CHIP

The chip was developed to provide a precise bandgap reference voltage to the bPOL12V. Its layout is shown in Figure 8.15 and its area is 810µm x 1060µm. At right part of the chip, there are VddIO, Vss and BGP pads to be wire-bonded to bPOL12V chip. At left part of the chip, there are pads for PROG and 3-bit Address signals. It will be programmed after manufacturing and then will be wire-bonded on top of the bPOL12V.

As can be seen in Figure 8.15, it consists of a bandgap reference voltage (to provide a temperature, power supply, radiation-independent reference voltage), an 8-bit eFuse block (to calibrate the bandgap voltage), a linear regulator (to generate VddCORE power supply voltage internally), a current generator (to generate and distribute current to all the blocks), an Enable block (to enable the chip when VddIO, VddCORE and BGP_IO are sufficiently high), a read and clock generator (to read and store the data of the eFuses in every power cycle and after every PROG signal) and a bandgap_IO block (to provide temperature, power supply, radiation-independent reference voltages to the Enable block).

VddIO pad has IO ESD protection and all the other pads have CORE ESD protection. It can be programmed by following the procedures explained in the Chapter 6, and then will be wire-bonded on top of the bPOL12V chip.

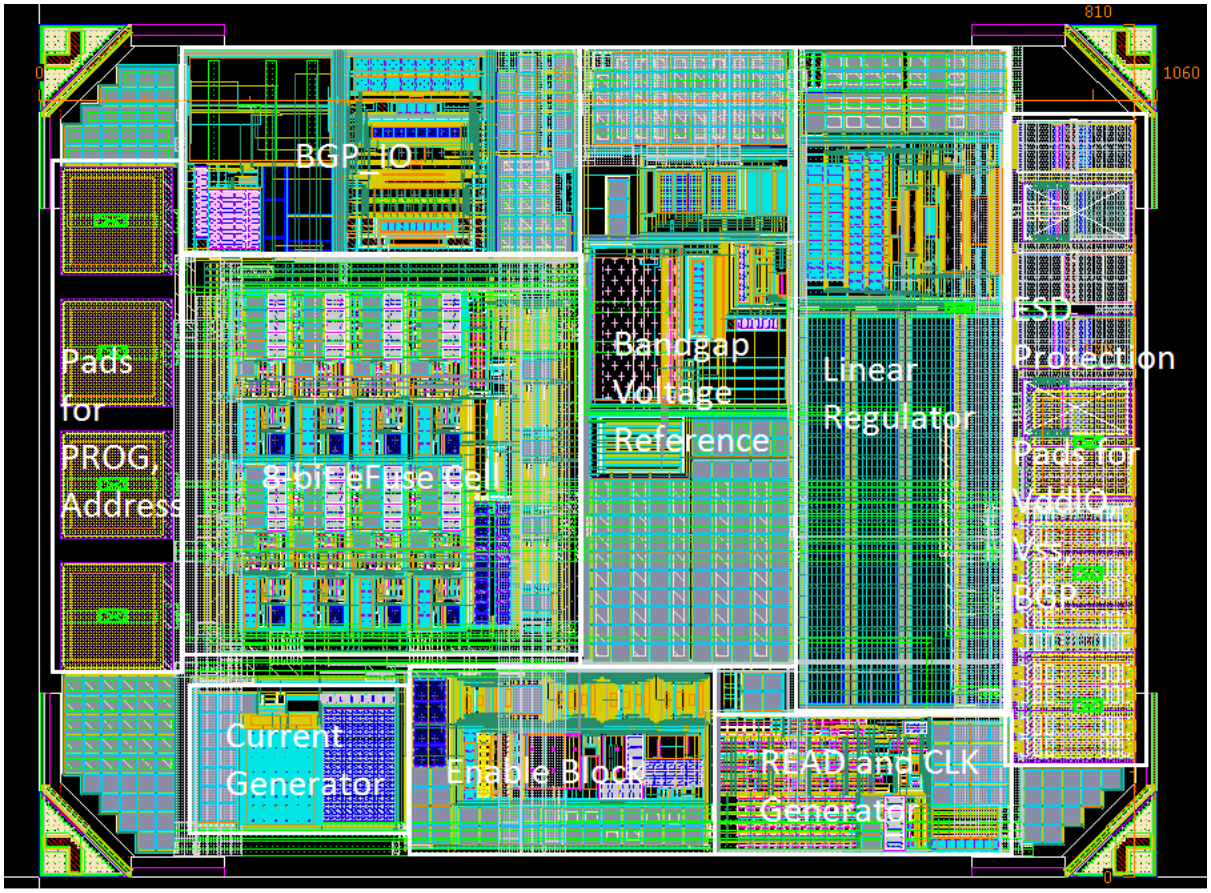

Figure 8.15: Layout of the second version of the chip with highlighted main blocks.

CHAPTER 9
CONCLUSION

In this master's project, a radiation-hardened bandgap voltage reference with electrical fuse (eFuse) based analog trimming circuit and an over-temperature protection circuit were developed in a commercial 130nm technology to be integrated into the DC/DC converters for LHC experiments upgrades. The purpose of this circuit is to provide a precise reference voltage to the first and second stage DC/DC converters and to protect them against high temperature.

These circuits will be placed close to front-end electronics (and therefore close to the proton collision point) and they will be exposed to intense radiation (up to 100Mrad). Since commercial components cannot survive in this harsh experiment environment, a custom ASIC (application specific integrated circuit) was designed. The radiation-induced degradation of the devices poses a major challenge in these applications.

Radiation hardness is achieved with appropriate choice of the technology, layout modifications and appropriate design against Single Event.

Enclosed layout transistors were used for all NMOS transistors to cut the radiation-induced leakage current between source and drain of the transistor due to presence of STI on the transistor's edges. In addition, p+ guard rings were used to prevent the radiation-induced parasitic currents between different n-doped diffusions biased with different voltages. The circuit nodes sensitive to Single Event Effects (SEE) were identified by simulations and either physically triplicated or filtered with on-chip capacitors to avoid errors.

The bandgap voltage reference provides a radiation, temperature and power supply independent reference voltage (at 300mV) to the DC/DC converters, in order to generate a stable output voltage at the output of the DC/DC converters. Due to radiation, process variation and mismatch, the bandgap reference voltage may have an error up to ±30mV and this error was decreased to ±0.6mV by the developed eFuse based trimming circuit.

The over-temperature protection circuit is to disable the DC/DC converters at high temperatures about 90^0C - 100^0C and to enable them again when the temperature was decreased to about 60^0C - 70^0C. In this way, the converters will be protected against high temperature.

The first chip was designed, manufactured and tested under harsh environment. Measurement results show that, firstly, the bandgap reference voltage at 300mV can be programmed with a precision of ±0.6mV to calibrate the bandgap against radiation, mismatch and process variation. Secondly, the voltage shift of the bandgap from -30^0C to 120^0C is only 5mV. Thirdly, its voltage shift due to TID is less than ±1.6mV and the bandgap voltage do not change under heavy ions with an LET of up to 50 $MeVcm^2mg^{-1}$. These results show that a temperature, power supply, radiation, mismatch, process and single event independent reference voltage was generated.

The measurement results of the over-temperature block shows that the DC/DC converters can be disabled at high temperature and enabled again at a lower temperature with a hysteresis of 30^0C with

an error of ±10^{0}C. Furthermore, the temperature inside of the chip can be estimated by observing the PTAT_amp signal that increases linearly with temperature.

A second version of the chip was designed and this chip will be wire-bonded on top of the first stage DC/DC converter (bPOL12V), which was designed in a different technology, to provide a precise reference voltage to it. This chip works with a single power supply voltage, VddIO, compared to the dual power supply requirement of the first version. The READ and CLK signals for the eFuse cells are generated internally in this version. Furthermore, the over-temperature block was improved to disable and enable the DC/DC converter with a hysteresis of 30^{0}C with an error of ±2^{0}C.

As a future work, the second version of the chip will be tested in temperature, under irradiation and heavy ions after manufacturing. Afterwards, it will be wire-bonded on top of bPOL12V and re-tested.

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