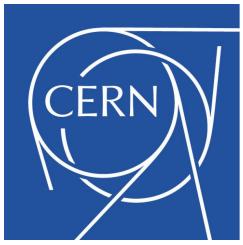

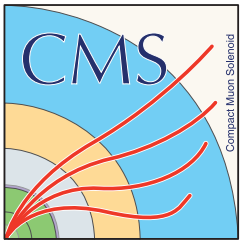

CERN SUMMER STUDENT PROGRAM 2018
FINAL REPORT

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Contents

INTRODUCTION

During the CERN Summer Student Program 2018, my project was to work on the On-detector electronics of the Drift Tube muon detector of CMS. The Muon Drift Tube(MDT) will be continuously used for the High Luminosity LHC, the high luminosity data taking period with the upgraded LHC. This period is called 'Run 3' and is expected to last from 2026 till 2038. The shutdown for the HL-LHC upgrade ending in 2026, which is called 'Phase-2' will start after the current 'Run 2' which ends in 2023. Although the MDT will be continuously used, the electronics of the MDT will be upgraded during the shutdown, due to the increase of the data rate and radiation. The board on the detector used as a TDC(Time-to-digital converter) to get the time information of the MDT will be exchanged to OBDT(On-Board electronics for DT boards) for the Phase-2. The new board will use a Flash based FPGA called Polarfire, which is more radiation hard then SRAM based.

About 1000 OBDT's will be made for the MDT in the CMS. However, the OBDT's must be tested to qualify the production of the OBDT. To make the board test efficient, a firmware will be prepared. During the Summer Student Program for 10 weeks, my task was to make the firmware for testing the input of the OBDT. One board will be used to generate two kinds of signals, and another board will be used to receive the signals. In turn, all the produced OBDT will be used as receiver for testing their inputs.

MUON DRIFT TUBE

CMS is a general purpose experiment measuring proton-proton(p-p) and heavy-ion collisions at the Large Hadron Collider (LHC). CMS is used to distinguish and measure the properties of the particles produced in the collision. As shown in figure1, CMS consists of several kinds of detectors to measure different kinds of particles produced in the collision.

The Muon Drift Tube(MDT) is used to measure the position of the muon in the barrel part of the CMS detector. Each DT chamber consists of 12 aluminium layers, which are arranged in three groups(Super layer) of four. The middle group is used to measure the direction parallel to the beam and the two outside groups measure the direction perpendicular to the beam. When the muon passes through the detector volume, it knocks electrons off the atoms of the gas and are drifted by the electric field shown in figure2.

The drifted electrons create a pulse along the wire which possess the information of time. The position of the muon can be derived by multiplying the speed of an electron in the tube by the time.

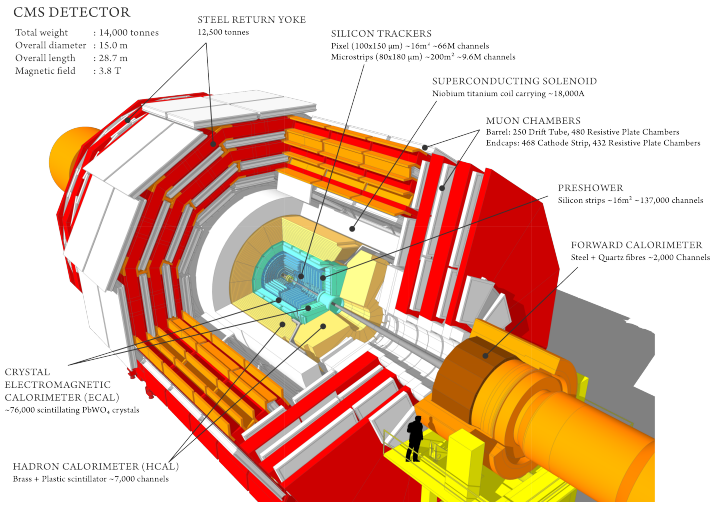

Figure 1: Schematic of the CMS detector

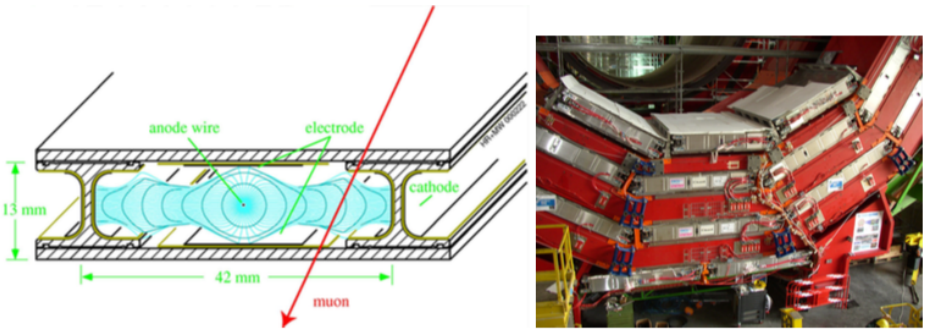

Figure 2: Muon Drift Tube

On-Board electronics for DT boards(OBDT)

The board on the detector will be exchanged to OBDT module in Phase-2. At present, there is an ASIC for doing the time to digital conversion(TDC) in the detector. A SRAM based FPGA called Virtex7 is instead used in the demonstrator of the new electronics in the spare chamber on the surface of CMS pit. OBDT has two large features compared to the present one.

1. low power (the estimated power is half of the present).
2. board based on a Flash-FPGA (Microsemi PolarFire)

Flash based FPGA‘s are more radiation tolerant compared to SRAM based FPGA‘s.

Microsemi FPGA

With the top two FPGA companies, Xilinx and Altera, taking up 89% of the FPGA market(2016), Microsemi is gradually winning market share by targeting specific applications. Microsemi specializes in low-power and mixed signal FPGAs.

BOARD TEST

The OBDT is not yet available but the OBDT prototype will be produced in September 2018. Since a demonstrator for the MDT with 3 super layers is now working in the CMS site, 3 OBDT prototypes will be made to qualify the board. Eventually, about 1000 OBDT's will be made for the MDT and each OBDT needs to be qualified by conducting a board test. To make the firmware for the board test, I used two evaluation boards of the Polarfire FPGA, one for outputting signals and the other for receiving the signals with the TDC as shown in figure3.

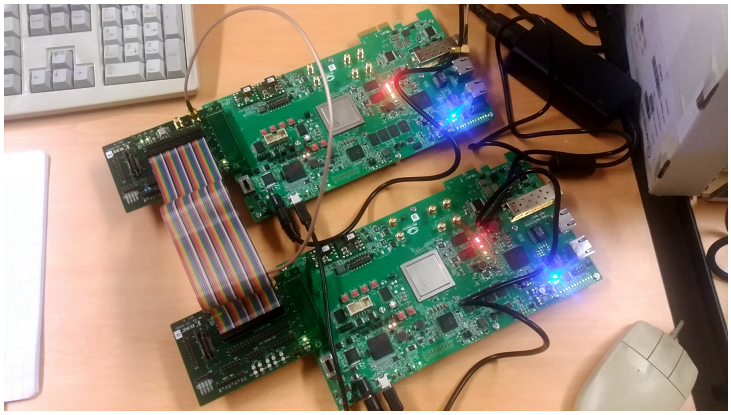

Figure 3: test using two boards

Libero

Libero is a software used to configure FPGA's of Microsemi by using Hardware description language(HDL), which is a computer language to describe the behavior of digital logic circuits. Two kinds of HDL are commonly used, Verilog HDL and VHDL, and both languages can be used in Libero, but cannot be mixed.

Evaluation board

Since the OBDT is not yet available, I used the evaluation board with the Polarfire FPGA built in to make the firmware for the board test. The schematic of the evaluation board is shown in figure4.

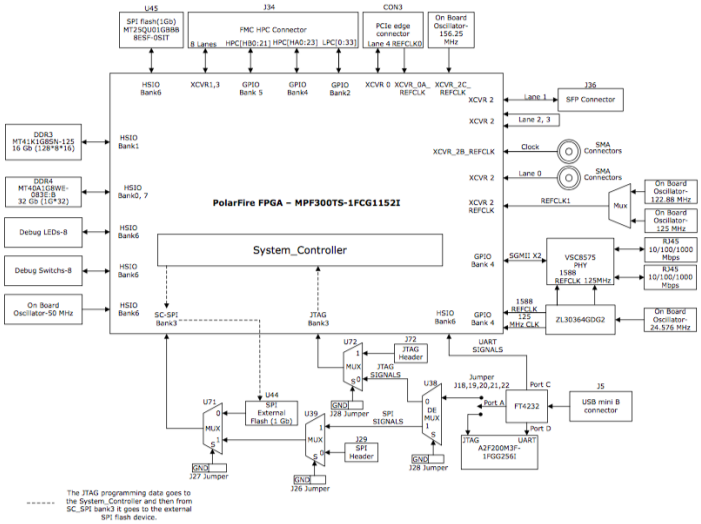

Figure 4: Schematic of evaluation board

In addition, the Xilinx mezzanine card was also used to output and input the LVDS signals. 20 LVDS inputs and outputs, 1 push button switch, 1 DIP(Dual In-line Package) switch were used in the board test.

Signal

The firmware required for the board test can switch between two kind of signals

1. PRBS(Pseudo random binary sequence)
2. Pulse signal with delay

These signals are used for different purposes.

PRBS(Pseudo random binary sequence) is a random signal which is difficult to predict and exhibits statistical behavior similar to a truly random sequence. By using this signal, the response of the board for several frequencies can be checked.

The Pulse signal with delay is to qualify the performance of the TDC. This signal is produced by inputting a 10 bit parallel signal into a IP core which converts it into a serial signal. By shifting the parallel signal, a delayed pulse signal can be produced. The operation principle of the serialization is shown in figure5.

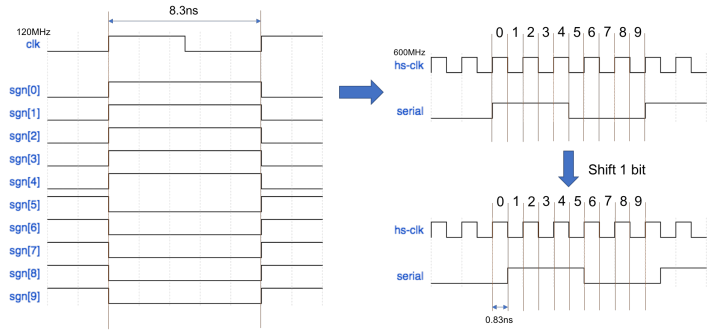

Figure 5: Serialization

Block Diagram

The block diagram of the board test firmware is shown in figure6.

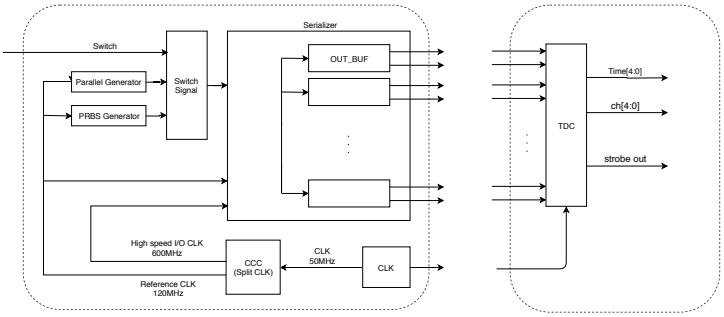

Figure 6: Block diagram of the board test firmware

50 MHz clock oscillator

A 50 MHz clock oscillator with an accuracy of +/-50 ppm is available on the board. This clock oscillator is connected to the FPGA fabric to provide a system reference clock. It is also connected to the output of the board and sent to the other board by using a cable to synchronize the two boards.

CCC(Clock Conditioning Circuitry)

CCC is used to generate synchronized clocks with new frequencies. For the board test, a 600 MHz high speed I/O clock and a 120 MHz fabric clock is generated from the CCC. The 600 MHz high speed I/O clock is connected to the serializer to serialize the parallel signals at 1.2 GHz. The 120 MHz fabric clock is connected to the other modules as a reference clock.

Parallel Generator

The parallel generator is a module which generates a 10 bit signal ,as shown in figure7,to generate a 41.67 ns serialized pulse from the serializer.

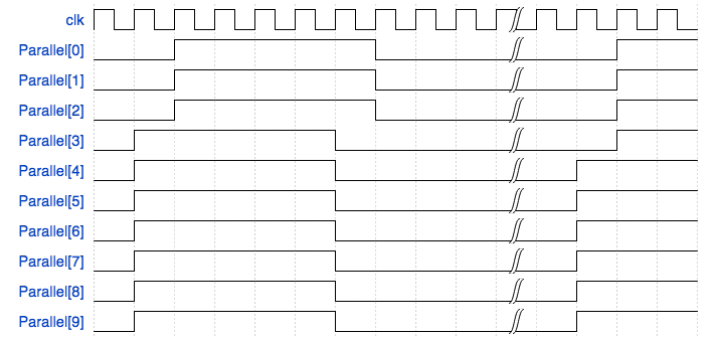

Figure 7: Parallel signals generated by the parallel generator

PRBS Generator

The PRBS Generator is a module which generates a 1 bit signal of the PRBS as shown in figure8.

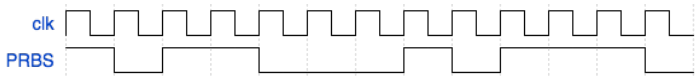

Figure 8: PRBS generated by the PRBS generator

Switch Signal

The Switch Signal module receives the Parallel signal and the PRBS, and switches between these two signals by using the DIP switch.

Serializer

The serializer is used to serialize the parallel signals it receives from the switch signal module.

TDC (Time-to-digital converter)

TDC (Time-to-digital converter) is used to output the time of arrival for each incoming pulse from the MDT and is embedded in the OBDT. The TDC for the MDT samples the input pulse at the rate of 1.2 GHz and measures the time of the rising edge of the pulse. The TDC has

an output of 25 bit signal called "data out", which contains the information of the time and channel number, and a 1 bit signal which is called the "strobe out". The first 5 bits of data out corresponds to the channel number and the last 5 bits corresponds to the time. The time starts to be measured with the rising edge of the LHC clock(40 MHz) and can be measured for 30 bins. The strobe out turns to 1 when the TDC is outputting data out. When the TDC receives several pulses at the same time, the signal will be serialized as shown in figure9. Figure10 shows an example of how the TDC works with 5 channels.

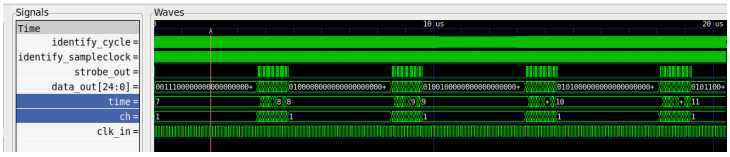

Figure 9: Serialized signal from the TDC

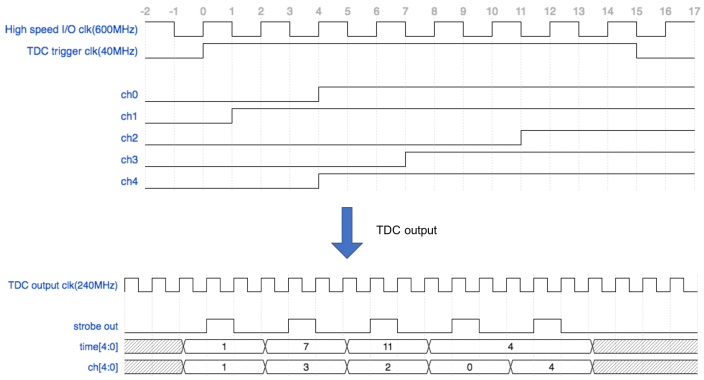

Figure 10: Example for the output of the TDC for 5 channels

To see all the 20 channels, the period of the pulse was set to 1 μs, which is long enough to contain all the serialized signals.

As the serialized signals are shifted one tick for each pulse, the time from the TDC is expected to increase one tick each time the TDC receives the pulse. Figure11 and figure12 shows the time and channel received from the TDC for an adjacent pulse.

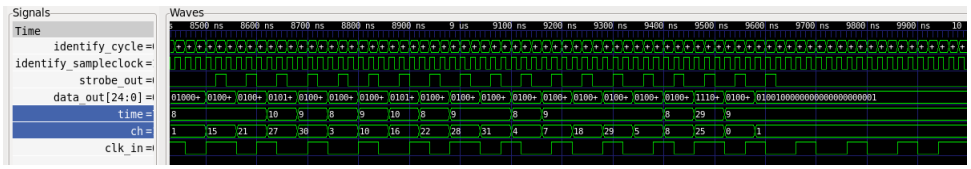

Figure 11: Time and channel information for the first pulse

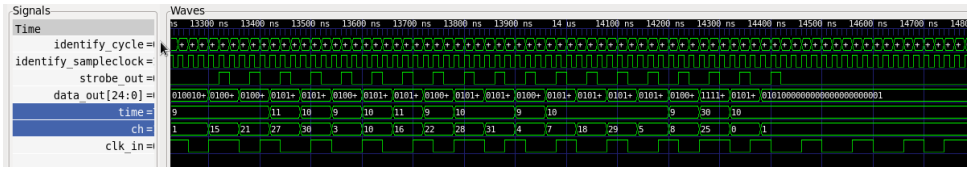

Figure 12: Time and channel information for the second pulse

Comparing the time for the two adjacent pulses, we can see that the time for each channel is increasing with 1 tick. For the board test, we need to check whether the time for each channel is shifted by 1 tick or not.

CONCLUSION

During the summer student program, I was able to learn the basics about electronics and how to write firmware for the FPGA by using Libero. Since the demand for the FPGA is increasing, not only in the high energy fields, but also in our other fields, it was a great experience to work on the FPGA. Although I do not know what I will be working on after the summer student program, I would like to continue my studies on FPGA's since it was an interesting subject for me.

ACKNOWLEDGEMENT

I would like to thank a lot of people who have supported me for the summer student program.

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