A Temperature Dependent Study of the Calibration of Timepix4 Assemblies

CERN Summer Student Report

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Abstract

Timepix4 hybrid pixel detector ASICs are used by the LHCb collaboration to construct the Timepix4 telescope. The temperature dependence of Timepix4 assemblies has been studied to outline the considerations required when cooling down the telescope "planes" to improve performance. The assemblies were studied with temperatures measured on the ASIC that varied between around 25 °C and 40 °C, in a 0% humidity environment. It was found that cooler sensors have a lower leakage current, but their breakdown and depletion voltage is a function of more than just temperature, and as such doesn't show one uniform dependency. It was shown that the digital to analogue converters of the ASIC have a measurable but negligible temperature dependence. The threshold equalisations demonstrated a negligible change between the maximum and minimum temperatures on the per pixel local threshold, however the number of pixels that could not be equalised increased as temperature decreased.

Contents

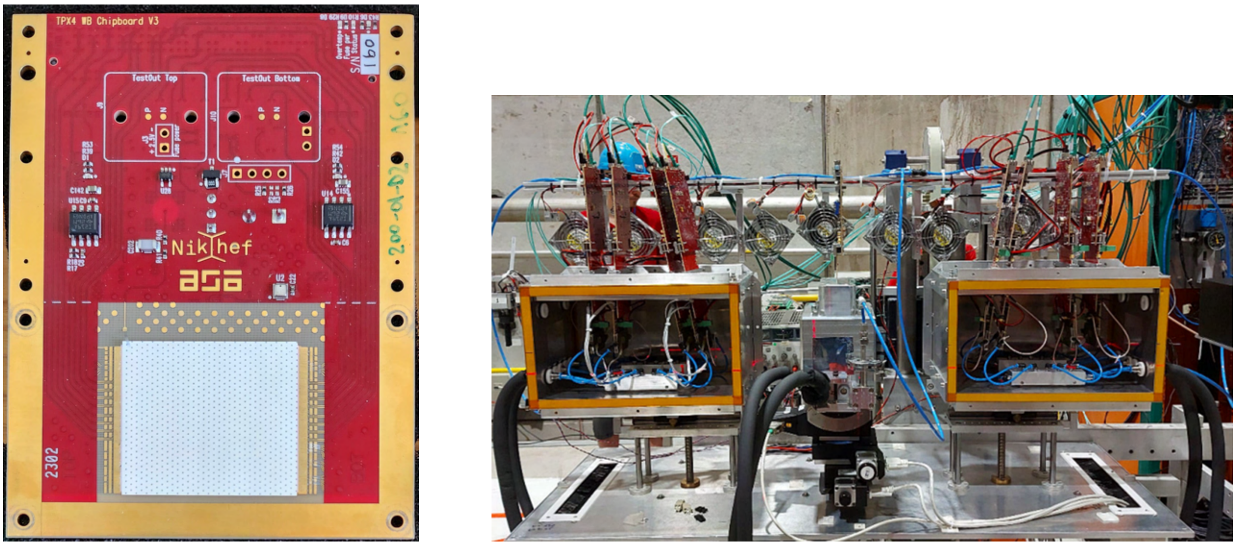
1 Acknowledgements

I would like to thank my supervisors Morag Williams and Edgar Lemos Cid, for their endless support and feedback during this amazing project. The time taken out of their busy schedules to run this is greatly appreciated. I would also like to thank Federico De Benedetti, Victor Coco, Paula Collins for their useful input and suggestions. My thanks go to Martin van Beuzekom for his help with the Timpix4 settings. And finally I would like to thank the LHCb collaboration and CERN as a whole for facilitating this once in a lifetime opportunity.

2 Introduction

The LHCb experiment at the LHC at CERN in Geneva, Switzerland searches for new physics by studying CP violation and rare decays of heavy quarks [1]. As the collaboration prepares for the high-luminosity upgrade, R&D on detector technology has increased to introduce fast-timing to the Vertex Locator (VELO). The VELO is a silicon vertex detector that encapsulates the interaction point and is the first detector particles will traverse after colliding [2] at LHCb. As a part of this R&D movement, the Medipix collaboration has developed their latest particle tracking ASIC, Timepix4.

The Timepix4 ASIC is a hybrid pixel detector readout chip designed to be bonded to silicon pixel detectors with a pitch of 55 μm [3]. Once bonded to a sensor they are referred to as a "hybrid assembly", this is shown in figure 2.1a. The LHCb collaboration utilises Timepix4 assemblies to create a "telescope", in which multiple Timepix4 planes are arranged one after each other along the beam axis to create a system capable of tracking a particle through the sensors and creating a 4D reconstruction of its track. Then, a new, uncharacterised device can be placed in the telescope, and its measurement can be compared to the telescope track reconstruction. This allows the device to be characterised with respect to an already well-understood system. Because of this, the Timepix4 planes need to be highly characterised, such that their measurements are as reliable as possible and the track reconstruction is accurate. Figure 2.1b shows an image of this.



(a) (b)

Figure 2.1: Picture of a Timepix4 Assembly (a), and side on view of the Timepix4 telescope (b) [4].

Until this point, the telescope planes have been kept at a fixed temperature during their operation using a cooling system mounted to the rear of the chip. This maintains the ASIC at a temperature of around 40°C during data taking. The idea of cooling the planes down to improve ASIC performance has been considered, as this allows the device to draw a higher current without sustaining damage. However, the effect of temperature on the calibration needs to be quanitified. The goal of this study is to characterise the temperature dependence of Timepix4 ASICs and sensors. This will allow the collaboration to understand what needs to be considered when altering the temperature of the telescope planes. For example if the telescope is used at a different time of year or if the planes are cooled for better performance.

3 Theory

3.1 Semiconductor Detectors

In semiconductors, a P-N junction is created when an N-type and P-type semiconductor are placed in contact; the excess electrons from the N-type fill the gaps where electrons are missing in the P-type in a thin region around the contact. The number of free charge carriers here is small, so the conduction band is almost empty, and an electric field is induced across the boundary. This thin section is called the depletion region [5].

This thin region can then be extended to take up the majority of the bulk by applying a "reverse-bias" electric field opposite to the one induced. As the electric field across the sensor increases in magnitude, the depletion region grows until the bulk is completely depleted. Additionally, a small amount of charge carriers will be promoted to the conduction band by thermionic emission and begin to flow across the junction, which is called the leakage current [6]. Since this is a thermal effect, it is expected that hotter sensors will have a higher leakage current. The width of the depletion region as the voltage increases up to full depletion can be approximated by 1, where W is the width of the depletion region, ϵ_0 is the permittivity of free space, ϵ_{Si} is the relative permittivity of silicon, e is the charge of the electron, N_D is the doping concentration and V is the voltage across the bulk. A $\sqrt{\text{V}}$ dependence is expected. The leakage current is proportional to the amount of depleted bulk, so it is expected that this also follows a $\sqrt{V}$ dependence.

$$W \approx \sqrt{\frac{2\epsilon_0\epsilon_{Si}}{eN_D}V} \tag{1}$$

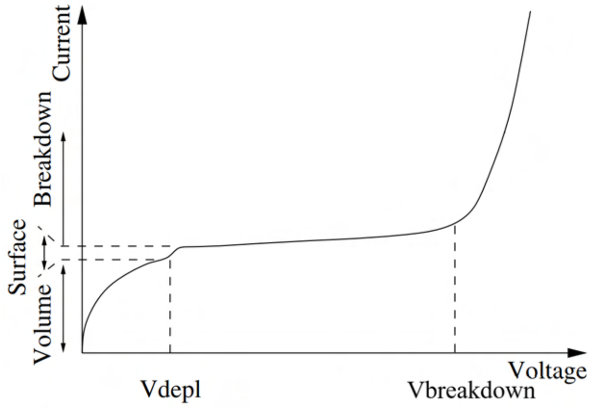
Once the bulk is fully depleted, an increase in voltage doesn't change the size of the depletion region, and the leakage current slope becomes small; however, it does increase the drift velocity of charge carriers across the bulk. The minimum voltage required to fully deplete the bulk is given by equation 2, where V_{dep} is the depletion voltage, e is the charge of the electron, N_D is the doping concentration, d is the sensor thickness, ϵ_0 is the permittivity of free space and ϵ_{Si} is the relative permittivity of silicon. It is expected that depletion voltage goes at d^2 [6].

$$V_{\text{dep}} = \frac{eN_D d^2}{2\epsilon_0\epsilon_{Si}} \tag{2}$$

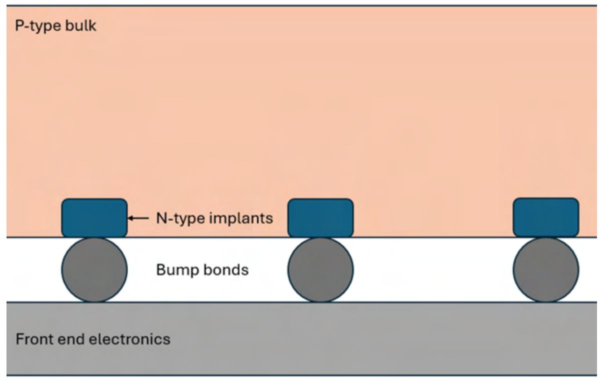
When a charged particle traverses the depletion region, it deposits energy into the lattice, promoting electrons from the valence band to the conduction band. They now act as free charges again and begin drifting towards the anode. Additionally, the "hole" left behind by the missing electron acts too as a charge carrier and drifts towards the cathode. This drift of charge carriers is a current pulse and is detected as a particle "hit".

Figure 3.1a shows the reverse bias IV characteristics of a PN junction. It shows the $\sqrt{V}$ dependence under V_{dep}, denoted the "volume" region, followed by the linear depletion region. An important feature to note is the "surface" region, a convex inflection just before the depletion voltage. This effect depends highly on the geometry of the sensor and arises when the depletion region approaches the edge of the bulk, causing current losses in various ways. Eventually, as the voltage increases past "$V_{\text{breakdown}}$", it reaches the breakdown section.

Breakdown is a region of exponential leakage current and is caused by two different effects: avalanche or Zener. The Zener effect occurs because the electric field from the applied voltage reduces the thickness of the P-N junction barrier. As the voltage increases, the slope of the



(a) Sketch of the reverse bias IV curve of a silicon P-N junction. [6]



(b) Cross section diagram of a planar pixel detector.

Figure 3.1

boundary across the junction increases, effectively making the "distance" shorter, so the probability of tunnelling increases. Avalanche breakdown occurs because the electric field accelerates the charge carriers as they drift towards the electrodes. If the field is strong enough, the charge carrier can gain enough energy in its mean free path to promote more charge carriers from the lattice. These two effects cause identical-looking IV curves but can be distinguished by their temperature dependence [7]. Breakdown should be avoided while operating the Timepix4 assemblies; while this would damage the diode and the front end electronics, the latter is much more sensitive to this.

3.2 Pixel Detectors

Each pixel of a pixel detector consists of a doped silicon implant in an oppositely doped bulk. There are many ways of doing this, and one of the most common ways is the N-on-P planar sensor; a diagram of this can be seen in figure 3.1b. Small N-type implants are placed at regular intervals in the P-type bulk, and an electric field is applied until the bulk is depleted. Each implant represents 1 pixel in the matrix and Timepix4 is designed for detectors with a pixel size, "pitch", of 55 μm.

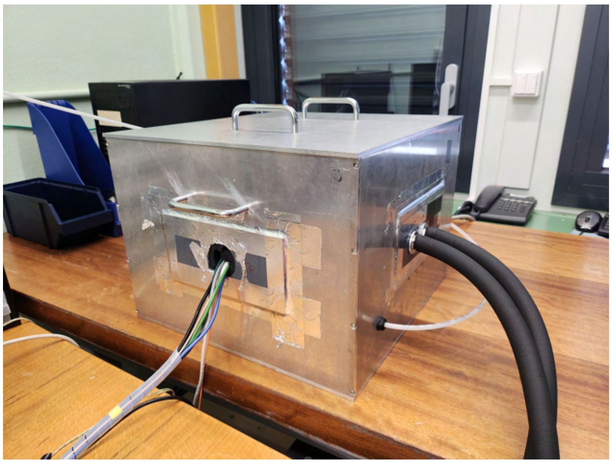
Each pixel is bonded via a small solder ball to its own set of front-end electronics on the Timepix4 ASIC. This process is called bump-bonding and is used to create "hybrids"; detectors with the sensor and readout electronics The front end electronics aim to turn the short, current pulse output from the sensor into a longer, smoother voltage signal that can then be used for digitisation. An ideal front end system would be consistent enough in this process that only the amplitude of the voltage changes as a function of the input current, and by extension as a function of energy deposited in the sensor. Information about the particle's energy is extracted from the ToA and ToT, time of arrival and time over threshold.

Slight differences in each pixel arise from the manufacturing process, meaning they all have slightly different noise thresholds. The noise threshold is the minimum voltage required to count as a real detection and must be set above the maximum amplitude of the random fluctuations in the output signal (noise). Because of the inhomogeneity of the pixel matrix, each front end needs to have its noise threshold tuned such that they all act identically. An equalisation scan does just this, altering the threshold per pixel until they all act identically.

In many semiconductors, the band gap is a temperature-dependent quantity, reaching a minimum value at 0 K and increasing as T increases [7]. As mentioned earlier, the leakage current is caused by charge carriers being promoted across the band gap via only thermal excitation. therefore it is expected that the noise on the signal will change as the temperature changes, and as such the noise threshold per pixel may change. This is why studying the temperature dependence of the equalisations is important.

4 Experimental Set-Up

To perform temperature-dependent measurements on the Timepix4 ASIC, a purpose-built set-up was created. This consists of a thermally insulated and air-tight container and an external cooling system with connections to the container, as shown in figure 4.1a. The external cooling system uses a Huber Minichiller, with a minimum coolant temperature of -20 °C when using glycol rather than water. This is shown in figure 4.1b.



(a)

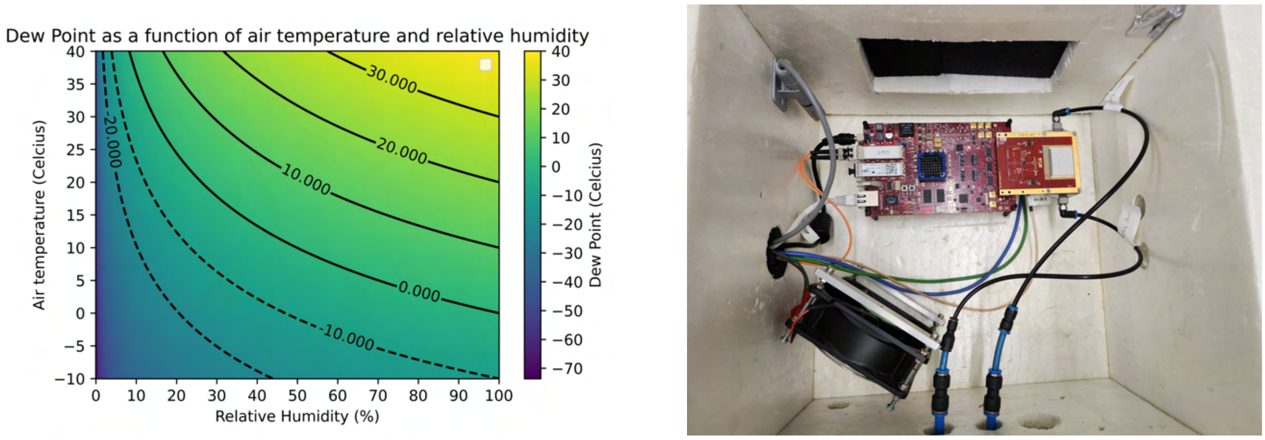
(b)

Figure 4.1: Picture of the thermally insulated, air-tight container (a) and the Huber Minichiller (b).

The low temperature is the reason the air-tight container is required. The dew point is the temperature at which the rate of condensation and the rate of evaporation of water off a surface is equal [8]. If an object has a temperature below the dew point in its environment, water will begin to condense on it. The dew point is a function of the air temperature and humidity, where hotter, more humid air has a higher dew point, as shown in figure 4.2a. Condensation during testing could be a problem, due to the high voltages used to deplete the sensors, so the box is sealed and flushed with dry air before the chiller is turned on.

The inside of the box is shown in figure 4.2b. On the top right is the Timepix4 assembly, mounted atop the SPIDR4 Board, which is used to communicate between the external computer and Timepix4. The top left shows a grey thermometer and hygrometer, for keeping track of the climate inside the box. The humidity and temperature are also both recorded locally on the Timepix4 assembly and the SPIDR4 board. There is also a fan which circulates air in the box reducing the possibility of temperature gradients.

This set-up allows for the measurements and calibrations of Timepix4 assemblies with an on-chip temperature range of around 24 °C and 43 °C. With each measurement, the temperature is recorded in Celsius to 1 decimal place, although it usually varies by up to half a degree during the measurement. The cooling block is attached to the back of Timepix4 assembly, on the opposite side of the sensor. The mounting system involves nuts on the front and back of the PCB, which can cause uneven mounting pressure. The cooling block would sometimes appear to be mounted evenly, despite not being. This was only visible after waiting for the chiller to cool down below around 0°C, at which point it would be clear that the ASIC temperature was higher than normal. This caused a lot of delays, as cooling down this far could take between 30 to 45 minutes. To mitigate this, the cooling block mounting was checked by shining a torch from one side to make any gaps visible. While this method greatly reduced the number of times the cooling block would have to be replaced, it was not a perfect solution and ideally a new cooling solution should be found. Table 1 shows the assemblies used in this study.



(a) (b)

Figure 4.2: Plot of dew point as a function of air temperature and humidity (a), and picture of the set-up inside the insulated container (b).

Assembly	Sensor Thickness (μm)
N37	50
N38	100
N155	200
N160	200
N22	300

Table 1: Table of assembly number and thickness.

5 IV measurements

An IV curve is a quick way of determining important information about a silicon sensor, for example the breakdown and depletion voltages. As such it is often the first step in assembly characterisation. IV curves are taken at multiple temperatures to understand what effect this has on the position of the depletion and breakdown voltages. This will allow the collaboration to better understand what operational voltages are available when using the telescope. For example, if the breakdown voltage changes with temperature, it is important to ensure that the operational voltage remains below breakdown regardless of external conditions to not damage the front end electronics.

Theory suggests that the two dominating forms of breakdown, Zener and Avalanche have opposite temperature coefficients; ergo, they follow opposite trends under a temperature change. For Zener, an increase in temperature causes a decrease in the magnitude of the breakdown voltage due to the band junction reducing in width. For Avalanche, an increase in temperature causes an increase in the breakdown voltage. This is because higher temperature charge carriers release their energy faster to the lattice, leaving less energy available for the impact ionisation effect [7]. Studying IV curves gives insight into the dominating form of breakdown of these assemblies, and what needs to be considered when the temperature is changed.

5.1 Procedure

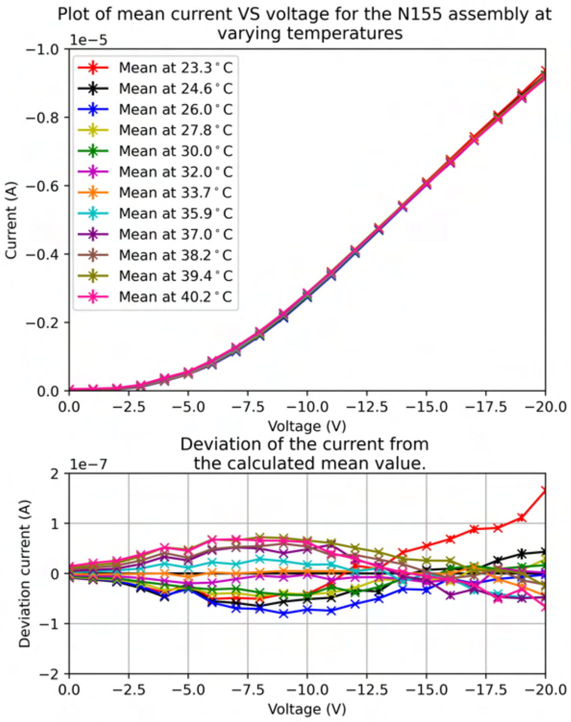
After being set up as in figure 4.2b, the room temperature chiller was set to -20°C. Once the coolant liquid reached 16°C, the assembly and LV power supply were turned on. The Timepix4 ASIC uses a 2 V LV channel, drawing around 4 A after initialisation. This was left until the glycol coolant fluid reached -20°C and the chip temperature stabilised. From here, after running the programs to read out the sensors on the chip and in the box, the high voltage measurement program is set up. The HV was applied by a Keithly 2410 SourceMeter [9], which follows a python program to apply a range of voltages and measure and record the current. To avoid damaging the front-end electronics of the ASIC, the Keithly is set to switch off if a current of more than 10 μA is recorded. This is known as the “compliance” limit. The HV program brings up the voltage slowly in predefined steps, averaging the current over 10 measurements after 5 s of stabilisation time, until the user input maximum, and then does the same in reverse. The analysis program then averages the up and down motion to take into account the hysteresis process.

5.2 Results and Analysis

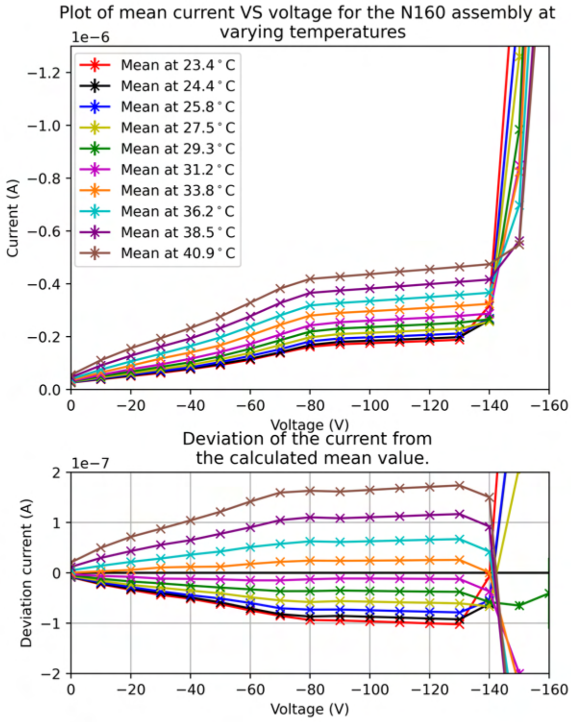
The first assembly tested was N155. N155 consists of a 200 μm thick planar silicon sensor bump bonded to the Timepix4 ASIC. Before testing, it was noted by the manufacturer that N155 had a wire bond issue, which caused an early breakdown, as written in table 1. The IV curve for N155 can be seen in figure 5.1a.

For N155, little variation between the temperatures is obvious on the scale of the leakage current. This can only be seen on the deviation plot in the bottom subfigure. The trend seen is that the higher temperatures record a higher leakage current, until a point of inflection. However, for N155 there is no clear depletion or breakdown region. The compliance limit is reached well before the sensor depletes and therefore it cannot be used within the telescope due to it not having a fully depleted bulk. This nicely demonstrates the importance of an IV curve. From this, it is decided that the N155 assembly should no longer be used for further testing.

N160 is a similar assembly to N155, also consisting of a 200 μm thick sensor and its IV curve is shown in figure 5.1b. The immediate difference is that the N160 assembly shows the expected IV curve for a reverse bias diode as shown in figure 3.1. There is a clear section of leakage current growth with voltage, ending at around -80 V, followed by a flat region and a temperature-varying breakdown between -130 and -150 V. It is also much clearer here that lower temperatures produce a lower leakage current, made more apparent by the overall lower leakage current of this assembly when compared to N155, by around 1 order of magnitude.



(a) IV plot of the N155 assembly at varying temperatures.

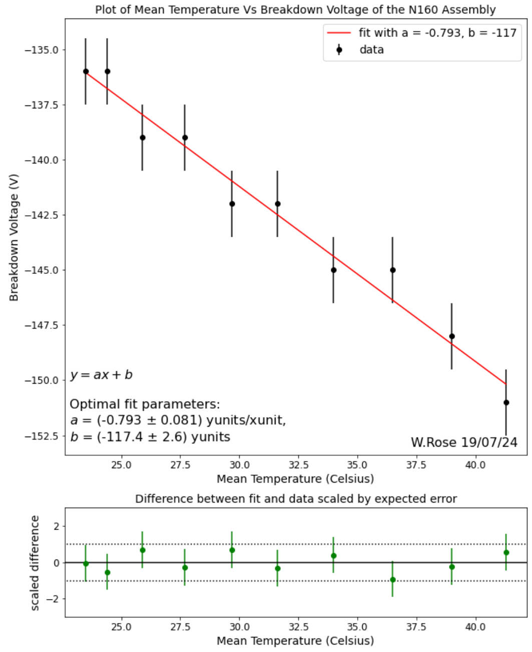


(b) IV plot of the N160 assembly at varying temperatures.

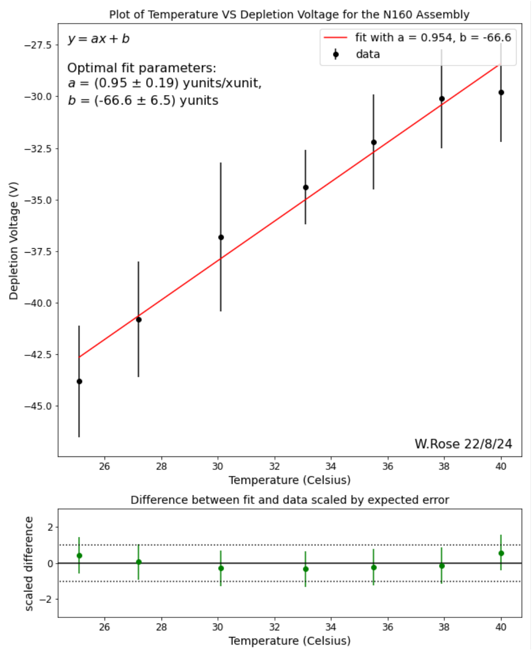
Figure 5.1: IV plots at varying temperatures for N155 (left) and N160 (right).

From here, a higher resolution data set was taken around the breakdown region. This was then analysed to find the breakdown voltage per temperature. The method used was to fit a straight line to the depletion region and then find the first point that deviates from this straight line by 10%. This point is then given voltage uncertainty of plus or minus half a voltage step. The values found for each temperature were then plotted, which can be seen in figure 5.2a. Additionally, the sensor's depletion voltage was found. This process involved plotting the IV on a semi-log-y graph and fitting a straight line to the low-valued data and to the depletion plateau. These lines were then extrapolated and their intersection (the depletion voltage) was found. This was performed this way because the surface effect, as mentioned in Section 3.1, reduces the current as the bulk approaches full depletion and, as such, skews the position of the depletion voltage. The found depletion voltage was then plotted as a function of temperature, as shown in figure 5.2b.

Both plots show a linearly dependent trend within their respective errors. Figure 5.2a shows a linear trend towards earlier breakdown as temperature drops, which confirms the avalanche effect dominates over Zener here. Figure 5.2b shows an opposite temperature dependence in the depletion voltage. The physics reason for this is still not fully explained.



(a) Plot of mean temperature vs breakdown voltage of the N160 assembly.



(b) Plot of mean temperature vs depletion voltage of the N160 assembly.

Figure 5.2: Plots demonstrating the temperature dependence of the depletion and breakdown voltages of the N160 assembly.

One thing to note is that the breakdown trends between -136 V and -152 V. For a silicon sensor of this thickness, this is unexpectedly low. Also, the depletion voltage is on the order of -30 V to -44 V, instead of around -80 V as it naively appears to be on the IV curve in figure 5.1b. The explanation for both of these effects can be attributed to the addition of a "guard ring" to these sensors. The guard ring is an implant around the edge of the sensor matrix. It comes in many forms, for example grounded or floating, continuous or staggered, but its purpose is to stop the flow of current towards the edge of the silicon [10]. This is necessary because the edge of the sensor is often not a smooth surface, which allows charge to build up when a voltage is placed across the pixels. This can then cause electrostatic discharge from the sensor to the ASIC, which can be damaging for the front end electronics. As the depleted region grows, it grows in a roughly spherical pattern around the implant. Eventually, the depleted region reaches the guard ring, and some current flows into the guard ring instead of the pixel pad. This causes the drop in current which skews the position of the depletion voltage. Additionally, the layout of the bulk consists of a higher doping concentration around the N-type implant - called the P-spray region. The guard ring and the pixel implants are both in this high doping concentration P-spray region. The voltage required to cause avalanche breakdown is inversely proportional to the doping concentration, and therefore this is the region that breaks down first, as current flows from the guard ring to the pixel implant. Without this effect, the breakdown would be at a much higher value [11]. The guard ring is generally a necessary thing which improves sensors, however in this case the highly doped p-spray region causes problems for them.

The N38 assembly has a 100 μm thick sensor and is currently used as one of the timing-focused planes in the Timepix4 telescope. Its IV curve is shown in figure 5.3. As expected, N38 follows the same trend as N160. As it cools down it has a lower leakage current and a lower breakdown voltage. Counterintuitively, it maintains a higher breakdown voltage than N160, which is the opposite of what might be expected as the sensors get thinner, as the E-field across the bulk should increase. However, this is because the breakdown here is within the P-spray region, and not the bulk itself, so the impact of the thickness cannot be seen. The breakdown voltage temperature dependence can be seen in figure 5.4a. This plot shows reasonable evidence for a non-linear trend, based on the residuals, however more data would need to be taken to verify this.

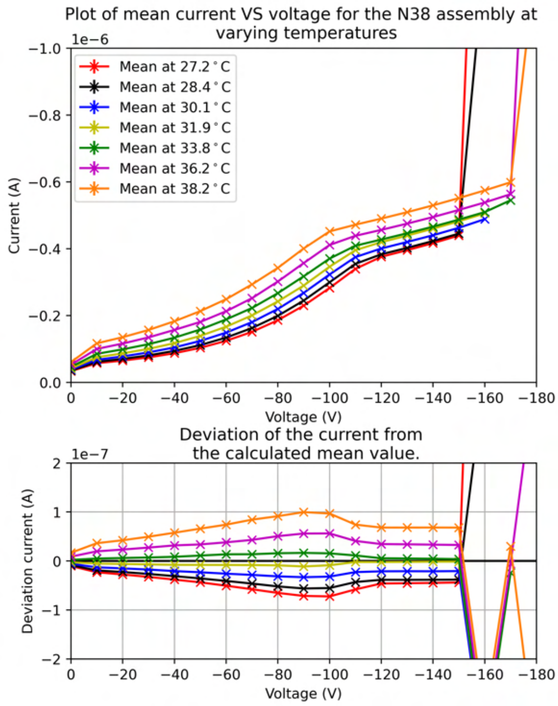
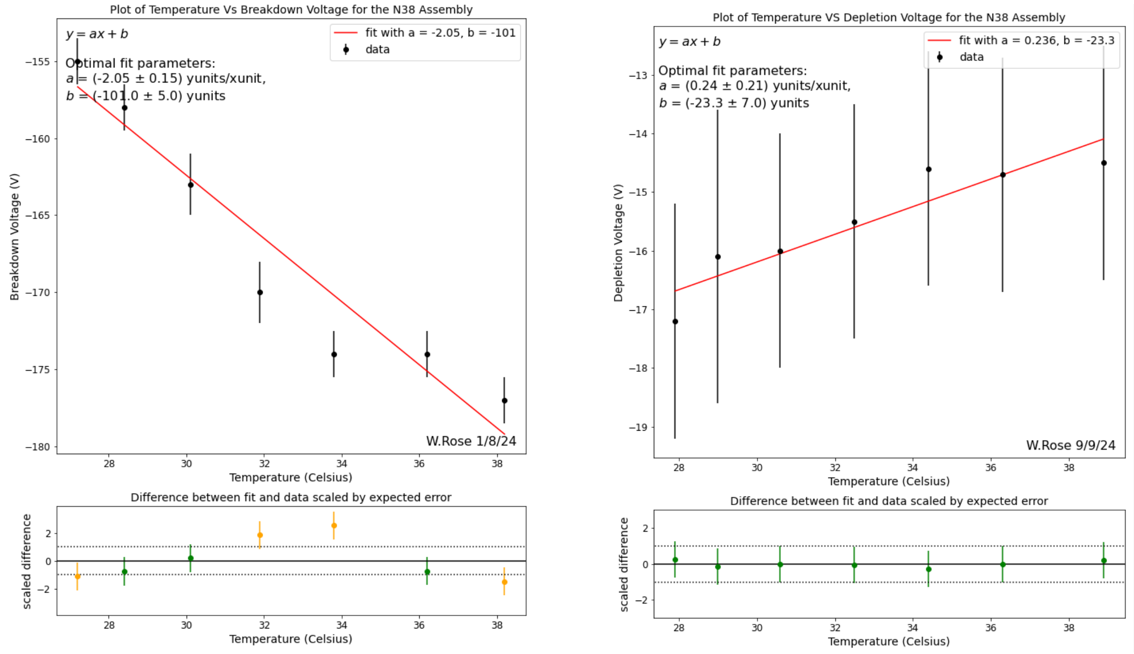


Figure 5.3: IV plot at varying temperatures for the N38 assembly.

The other noticeable difference of the IV curve is the shape of the curve below the depletion voltage. Here, the surface region has a much more significant effect and influences the majority of the curve below V_{dep}, as shown by the convex shape. This is because the thinner sensor has a lower surface area to volume ratio, and as such the complexity of extracting the depletion voltage of this sensor is increased. The plot of depletion voltage is shown in figure 5.4b. Due to only having a few points at low voltage that were unaffected by the surface region, the accuracy of the extrapolation was affected, and so the errors on these measurements are large. Still, the trend is consistent with being linear as is the same with N160.

The N37 assembly was measured next, containing a 50 μm thick sensor. Its IV curves are shown in figure 5.5. The N37 IV plot shows the same trend as the others; cooler sensors showing a lower leakage current. It also appears to show that the surface effect dominates the entire curve below V_{dep}, showing no volume region at all. Higher resolution data around 0 V showed no conclusive evidence for a measurable volume region and therefore the depletion voltage could not be measured in this case. Additionally, the breakdown for this assembly appears to be much less temperature-dependent. It is clear in figure 5.5 that the lowest two temperatures are beginning to breakdown at -55 V however the current change is still less than 10% and therefore not yet enough to define it as breakdown. Higher resolution data was taken around this point and it was found that all temperatures enter full breakdown at around -61 V to -62 V. The breakdown is highly dependent on the local doping profile and geometry of the pixels and guard ring, and so the reason why this appears less temperature-dependent is hard to diagnose.



(a) Plot of mean temperature vs breakdown voltage of the N38 assembly

(b) Plot of mean temperature vs depletion voltage of the N38 assembly

Figure 5.4: Plots demonstrating the temperature dependence of the depletion and breakdown voltages of the N38 assembly

Finally, the 300 μm thick N22 assembly was measured, and its IV curves are shown in figure 5.6a. Similarly to N37, the breakdown voltage does not seem to be as temperature dependent in this case, where all but the coolest setting show no deviation until sudden breakdown at -140 V. The depletion voltage for N22 also doesn't show any temperature dependence, within the errors of the fit. This is shown in figure 5.6b.

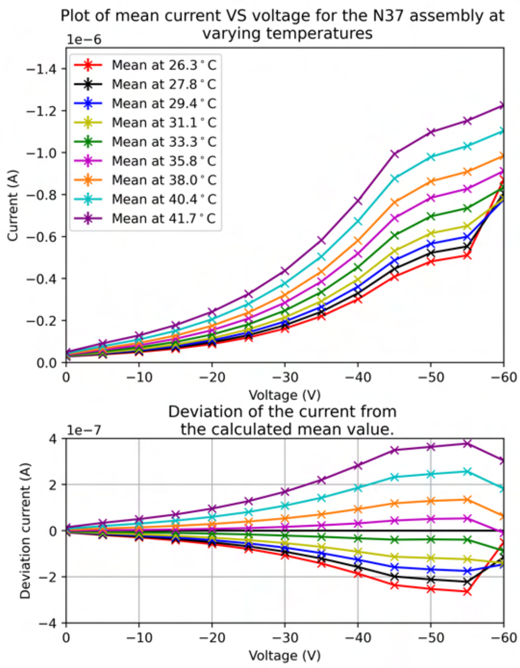
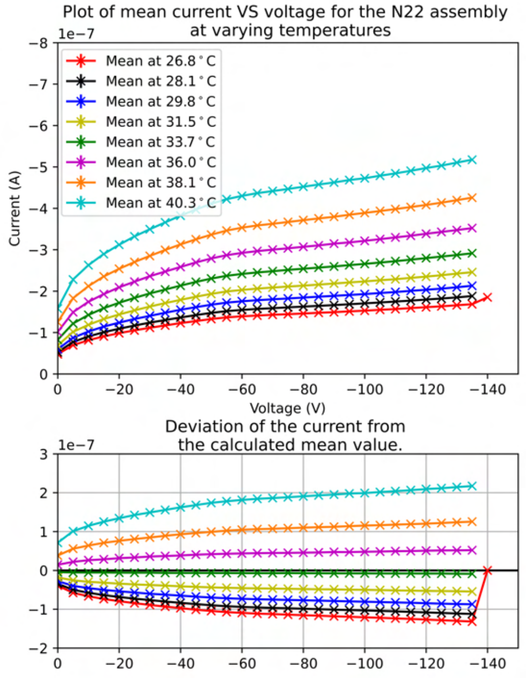
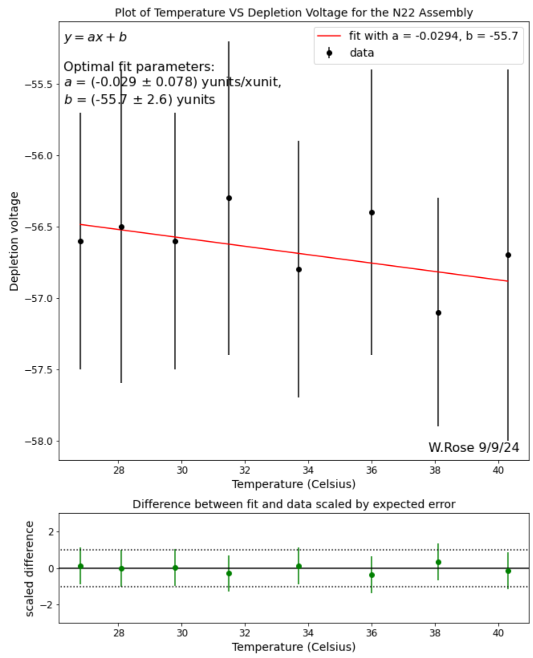


Figure 5.5: IV plot of the N37 assembly at varying temperatures.



(a) IV plot at varying temperatures for the N22 assembly.



(b) Plot of mean temperature vs depletion voltage of the N22 assembly.

Figure 5.6

The depletion voltages found for all the sensors can be compared to those found in the previous work by J.Haimberger [11], in which sensors from the same production were tested before bonding to any front end ASIC. These can be seen in table 2. These values were taken with the sensors at 24 °C, and so the value given from this paper's data takes the value of the fit at that temperature. Both sets of data show that a larger bias voltage is needed to reach depletion of the bulk as the sensor thickness increases, as expected. The theory suggested that this should increase as a function of thickness squared as in equation 2. While the data from J.Haimberger appears to follow this to within about 20%, the data taken in summer 2024 does not.

There is a noticeable difference between all the values of roughly ±10 V. There were a few ideas on what might cause this. The tests done by J.Haimberger were on "big diodes" not full sensors. There is a possibility that there is a significant difference between the depletion voltages of these two different types. Additionally, the temperature recorded in this paper comes from a thermal sensor on the back of the assembly chip board. The PCB separates this from the ASIC and then the sensor is bump bonded atop that. There is therefore likely to be a significant difference in temperature between the sensor and the thermal measurement, and therefore it may not be accurate to compare these readings. The method used to find the depletion voltage by J.Haimberger used a capacitance-voltage curve, rather than current voltage, and this may also account for the differences.

To study this a thermal camera was procured in an attempt to read the temperature of the surface of the sensor, and not beneath the ASIC. It was also considered that the thermal camera would give valuable insight into temperature gradients within the temperature-controlled environment and on the ASIC itself, which may exist but can't be seen by the static thermal sensor. This, however, came up with inconclusive results, as the front of the sensor is too polished, and as such the camera would only measure the temperature of whatever object was in the reflection of the sensor, e.g the walls of the container. An example of this can be seen in figure 5.7.

Thickness (μm)	V_{dep} (V) [From J.Haimberger]	V_{dep} (V) [Summer 2024]
50	-3.7	Not Found
100	-8.2	-17.5
200	-31.6	-43.8
300	-63.9	-56.4

Table 2: Table of sensor thickness, measured depletion voltage adapted from J.Haimberger [11] and the measured depletion voltage from this paper at 24 °C.

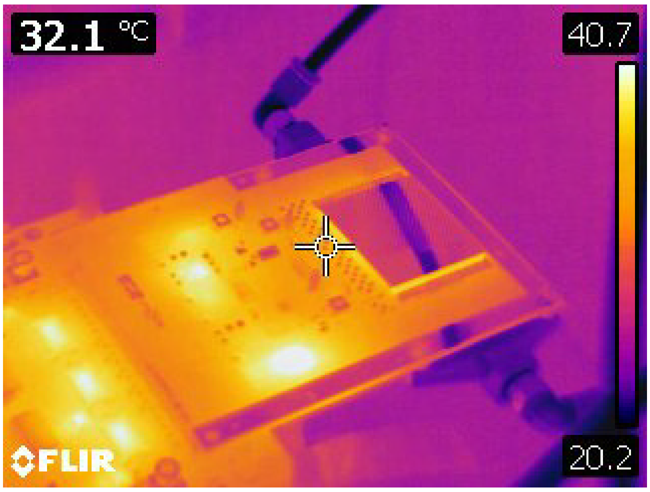


Figure 5.7: An example image of the Timepix4 ASIC taken with a thermal camera. The dark purple line across the sensor is a reflection of the cold coolant pipe just above.

6 DAC Scans

A Digital to Analogue Converter (DAC) is an electrical component that converts an arbitrary digital setting to a voltage or current output. It allows a user to set voltages and currents in different registers on the ASIC. Since it uses an arbitrary value setting, it varies depending on the ASIC layout differences at the transistor level and so a conversion must be found between these values and the real output in volts for a specific output to be chosen. A DAC scan measurement scans through the DAC settings at regular intervals and measures the output value. This then allows the user to set the real value required as a digital value in code. In this paper, only voltage DACs are considered. The temperature dependence of the DAC scans needs to be studied, as the voltage outputs control many functions on the ASIC: for example, the threshold voltage for particle detection, and the charge injected when doing a test pulse scan. If the temperature changes the conversion between the digital setting and voltage output, the detection threshold may not be as expected, and noise may end up being detected as a hit. Furthermore, the ASIC to ASIC difference is not yet understood, so this is an extra interesting result.

6.1 Procedure

The system was prepared in much the same way as for the IV scans. For the DAC scans, the HV system was not required, but everything else was identical. Then, the “tpx4dacscan”

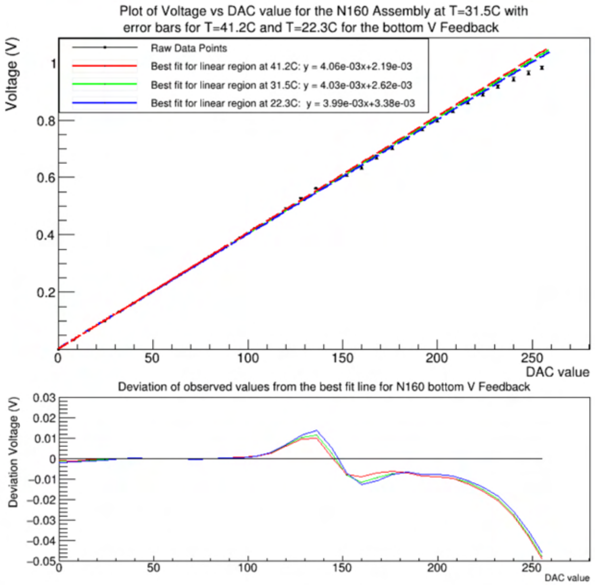
C++ program was run, which goes through each voltage DAC on the ASIC and measures the relationship between digital input and output voltage. This was performed for many temperatures between the maximum and minimum available on the chiller, which in this case gave chip temperatures in the range of 22 °C and 42 °C. Plots could then be generated of the conversion between DAC value and output voltage using error bars to show the difference between the maximum, middle, and minimum temperatures.

6.2 Results and Analysis

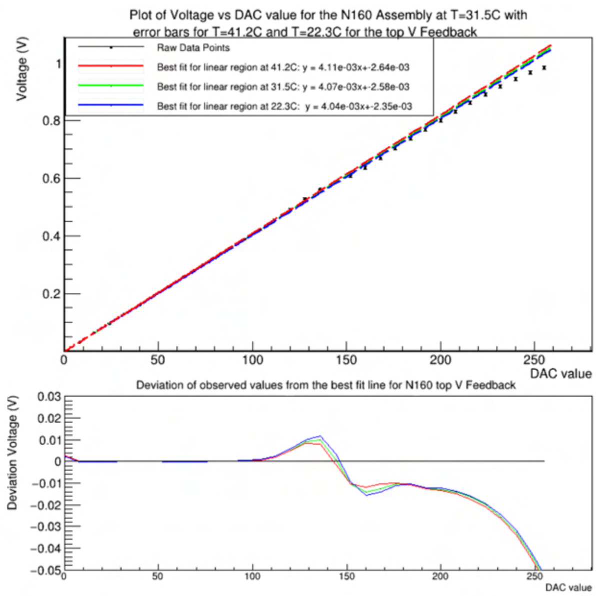
There are many voltage DACs on the Timepix4 ASIC, all of which have a top and a bottom version for the two halves of the ASIC wafer. All but the most interesting are omitted to save space. Figure 6.1 shows the top and bottom voltage feedback DACs for the N160 and N37 assemblies. This DAC is important because it plays a role in setting the front end's detection threshold. Comparing the top and bottom versions of the same assembly, there is a negligible difference, where the slopes of the fit lines only differ on the order of 1%. There is a measurable difference between the temperature slopes per DAC, however, it is also negligible, as it is only on the order of 1%. It can also be seen using the deviation plots that, while the DAC conversion is not perfectly linear, the temperature dependencies all follow the same non-linearity, and only appear to separate from each other in these non-linear areas, and still on the order of 10 mV. It can be noted here that all of the DACs measured follow a similar trend.

To consider whether this difference is significant or not, plots that show the difference between the output voltage at the max and min temperature for a given DAC value have been generated and are shown in figure 6.2. This comparison is useful because it informs the collaboration by how much the output voltage of each DAC could change when the temperature is altered. In this case, the max and min temperatures are roughly 15 °C apart. It is clear that at no point does the output voltage change more than 18 mV. From the config files, the DAC settings are generally in the 80-140 range for all the DACs with 256 settings over the 4 assemblies. In this region, the error ranges from around 5 mV to 15 mV, so on the order of 5% at most. When it comes to operating the telescope, this deviation is likely negligible, however, if the planes were to be cooled much more than what was measured in this study, it would be something that should be reconsidered.

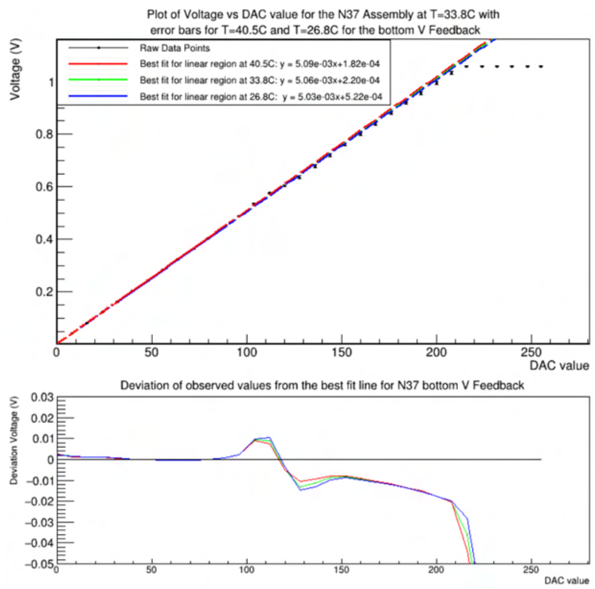
The voltage feedback DAC is used with the voltage threshold DAC to define the "applied threshold". While the difference between the maximum and minimum temperatures on each DAC is negligible, it is also pertinent to consider whether their temperature variation is collinear or not. Another plot was made where the voltage output from these two registers was subtracted and plotted against the arbitrary units of the voltage feedback DAC. This is shown in figure 6.3 for the top and bottom versions of this subtraction. Each plot shows two assemblies, N160 and N38, however, the remaining two follow a similar trend. The interesting point of these plots is not the voltage difference as shown on the y-axis, because these are adjusted separately, but the trends between the two different temperatures. It is clear here that there are no major differences between the hot and cold versions of each ASIC. This means that the temperature dependence of both DACS follows roughly the same trend and, as such, they don't significantly diverge when considered together. This is optimal for running the telescope, as it means that the predefined settings for these will work at any temperature and do not need to be constantly monitored.



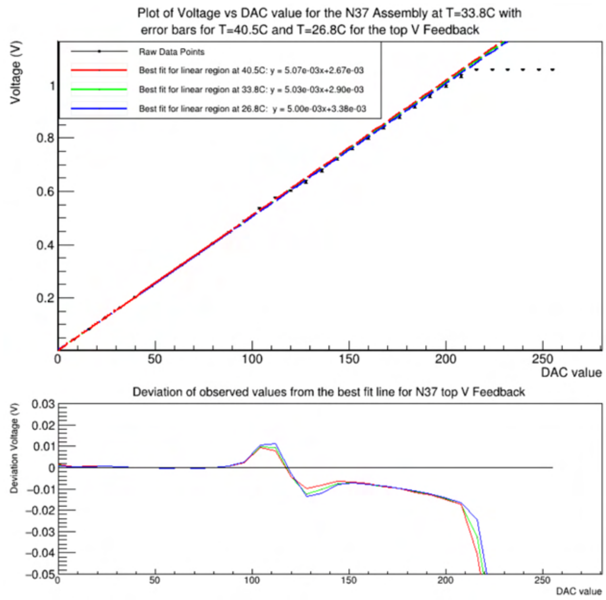
(a)



(b)

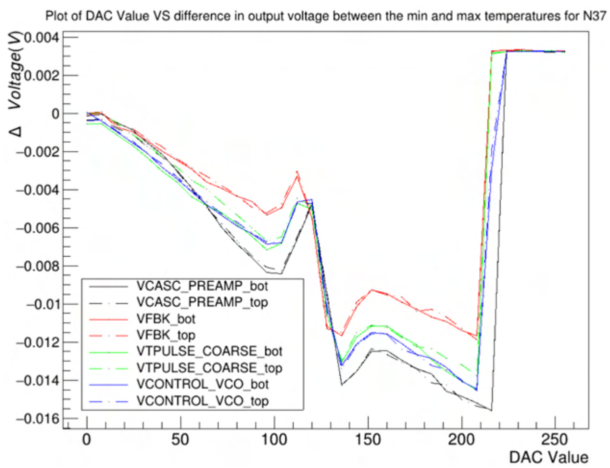


(c)

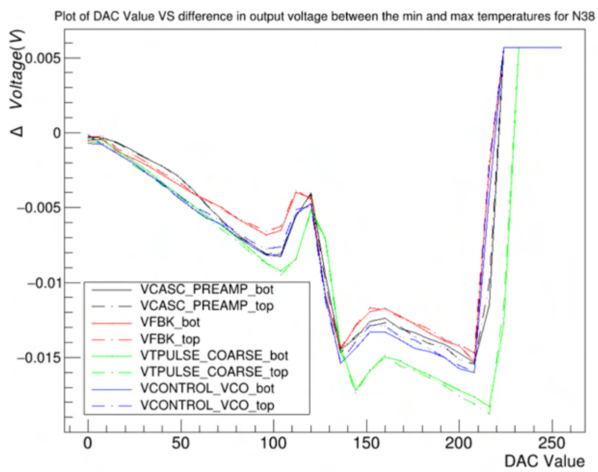


(d)

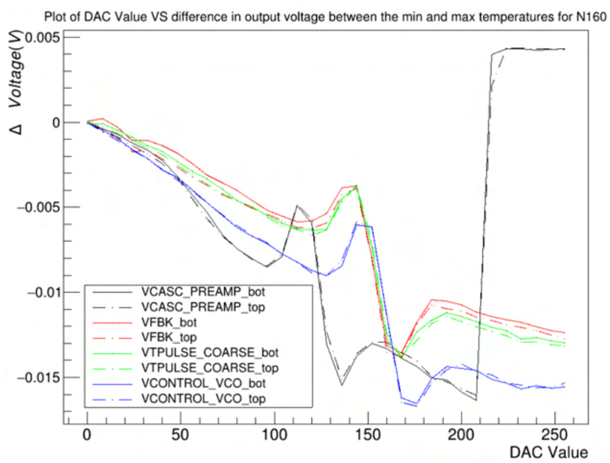
Figure 6.1: Plots of DAC value vs output voltage for 3 temperatures. For N160 Voltage Feedback DAC bottom (top left) and top (top right) and for N37 Voltage Feedback DAC bottom (bottom left) and top (bottom right).



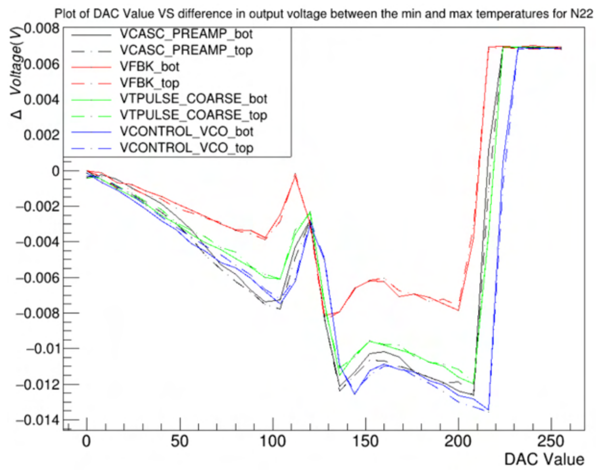
(a) $T_{min} = 26.8\,°C$, $T_{max} = 40.5\,°C$



(b) $T_{min} = 24.7\,°C$, $T_{max} = 40.8\,°C$

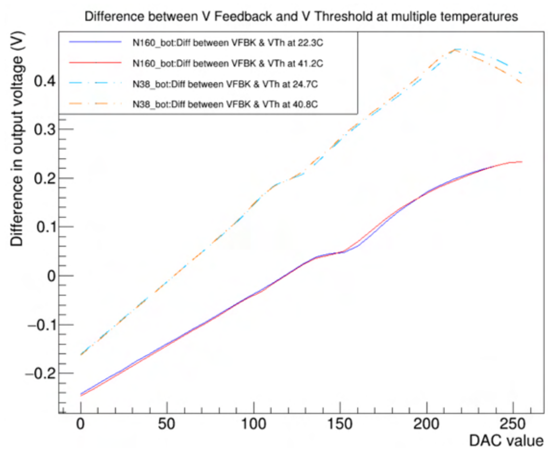


(c) $T_{min} = 22.3\,°C$, $T_{max} = 41.2\,°C$

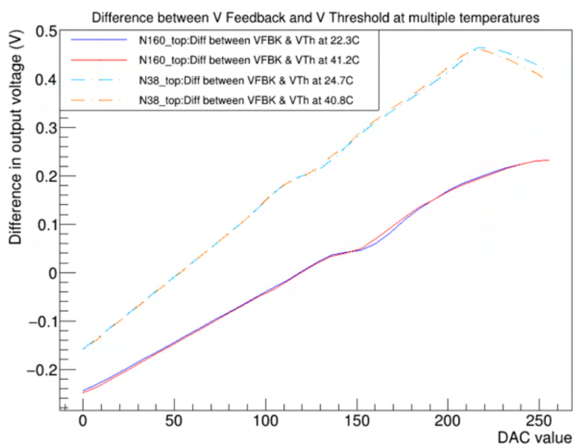


(d) $T_{min} = 26.2\,°C$, $T_{max} = 39.1\,°C$

Figure 6.2: Plots showing the difference in output voltage between the max and min temperature as a function of DAC value. N37 (top left), N38 (top right), N160 (bottom left), N22 (bottom right).



(a)



(b)

Figure 6.3: Plots of the difference between the voltage feedback and voltage threshold DACs for N160 and N38. Bottom DAC (left), top DAC (right).

7 Equalisations

Variations in the manufacturing process of the components of each pixel cause them all to have slightly different noise thresholds. This means that setting 1 threshold for noise across the whole matrix may cause some pixels to show hits from just noise, and others to show nothing when hits occur. An equalisation aims to achieve a more homogeneous response from the matrix by adjusting a local threshold register. Theoretically, lower temperatures could decrease thermal emission in the lattice, and so it is important to understand the effects of temperature on this. This is especially important as each equalisation can take multiple hours to run, and so if the same equalisation can be used for all temperatures this will save significant time in the case where the telescope is being used in a time sensitive application.

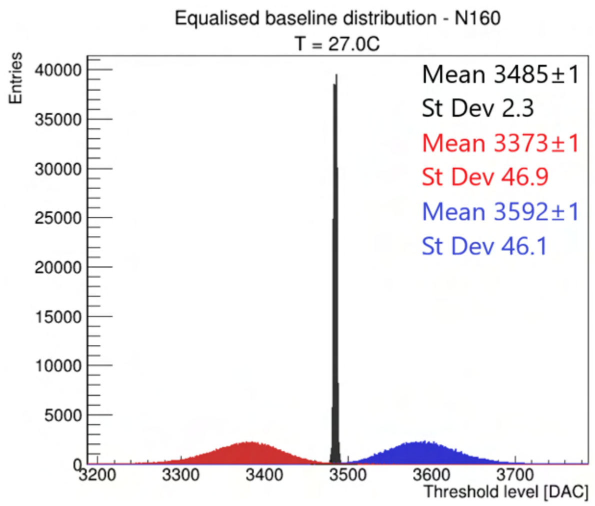
7.1 Procedure

Like the DAC scans, the set up is prepared in much the same way as the IV curves. In this case however, the chip must be biased such that it is in the state it would be in when being used as a detector. For this, the IV curves were used to find an appropriate voltage that could be used at both the maximum and minimum temperatures, for consistency. -120 V was chosen for N38, N160, and N22, whereas -50 V was used for N37. The equalisation process iterates through each pixel, iterating the local threshold between the maximum and minimum local threshold values and measuring the output of the pixel. Eventually the pixel will "turn off", meaning that the local threshold has peaked above the noise threshold and it is no longer measuring hits. This is measured for each pixel and then these adjusted local thresholds are applied across the pixel matrix. The plots show the "turn off" value for each pixel as histograms at the maximum and minimum threshold values.

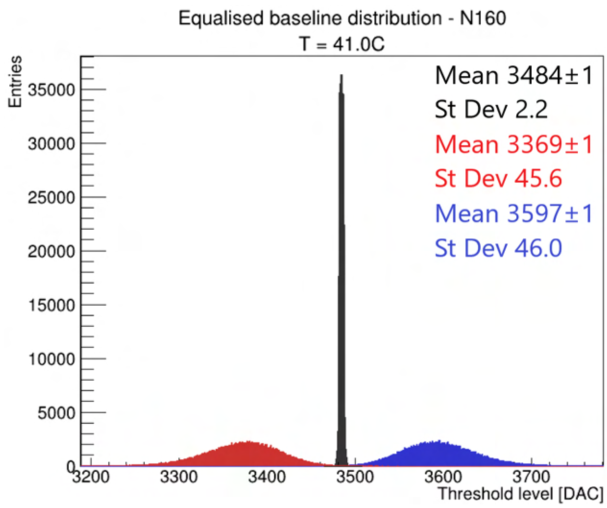
7.2 Results and Analysis

Figure 7.1 shows the plots of the equalised baseline distribution for the N160 assembly for the max and minimum temperatures. Each plot shows the red and blue histograms, which represent the minimum (0) and maximum (31) local threshold values. The black histogram then shows the threshold level after equalisation. The reduction in standard deviation by a factor of around 20 demonstrates the increase in homogeneity of the response after equalisation, a perfect equalisation would produce a delta function around the equalised mean value.

The difference between the equalised mean of the two temperatures is 1 DAC value for this ASIC. Using a conversion ratio from the ASIC designers, 1 DAC value on the N160 assembly corresponds to around 15 electrons. For a threshold of around 1000 electrons, this is a negligible change. The standard deviation is related to the electronics noise and also does not change significantly so therefore it can be concluded that for N160 the temperature does not affect the equalised baseline mean. Tabulated in table 3 are the same statistics for the remainder of the ASICs. This shows that the means change by at most 4 DAC values as the temperatures change. This is small enough to be considered negligible.



(a) Equalisation at T = 27.0 °C



(b) Equalisation at T = 41.0 °C

Figure 7.1: Plots of the N160 equalised baseline distribution.

	Min T		Max T	
Assembly	Mean	Std Dev	Mean	Std Dev
N37	2626	2.8	2622	2.4
N38	2618	2.5	2618	2.3
N160	3485	2.3	3484	2.2
N22	2650	2.5	2646	2.2

Table 3: Table of the Equalised mean values of each ASIC at the minimum and the maximum temperatures.

Even though the mean values are not changing, that doesn't necessarily mean that the individual pixels on the matrix aren't. To see this, the plots of the maximum and minimum temperature local pixel threshold adjustment matrices were subtracted from each other to show the difference between them per pixel. In the ideal case, the entire matrix would show 0 as the equalisation before and after is identical. Plots of this are shown in the left column of figure 7.2. The first thing to note is that all these plots show that the majority of pixels are on or around 0, this is close to ideal for a non-temperature dependent equalisation. The only significant pixels that have changed, are different by a factor of a few thousand.

During the equalisation, all the pixels are tested, however, some are returned as "missing baselines" or "out-of-range". This can account for as many as a few thousand pixels. This can be caused by pixel issues, however it is also possible that a pixel that is missing its baseline in one equalisation has it found in another, as a random process. It is believed these pixels that have a difference of a few thousand are just those that were missing a baseline in one of the readings, due to a failed fit function. Table 4 shows the number of out-of-range and missing baseline pixels. The trend is that at the minimum temperature, the amount of out-of-range pixels is roughly doubled, and the amount of missing baselines is either similar or slightly higher.

	Min T		Max T	
Assembly	Out-Of-Range	Missing Baselines	Out-Of-Range	Missing Baselines
N37	2998	32	1615	17
N38	1391	635	810	516
N160	1070	776	627	566
N22	1730	416	840	415

Table 4: Table number of out-of-range and missing baseline pixels of each ASIC at the minimum and maximum temperature.

The 2D histograms from the left column of figure 7.2 were turned into 1D histograms by iterating over each pixel and binning its value. Y-axis zoomed-in versions of these can be seen in the right column of figure 7.2. The truncated central peak is given by the majority of pixels that are on or around 0 after the subtraction. There are then one or two distinct peaks on either side of this, which are given by these pixels that are thought to be missing baselines in one of the equalisations. The baseline equalisations like the ones shown in figure 7.1 ignore these missing baseline pixels and as such the mean value of these histograms (which shows the difference between the equalisation mean at max and min T) are inconsistent with those shown in table 3 due to the difference in dataset. The number of pixels in the extreme peaks is roughly the same as the difference between the number of missing baselines. This backs up the hypothesis that pixels that are off by a few thousand are just those that were missing baselines in 1 measurement.

The key takeaway from these plots is that there are no peaks in between the central 0 peak and the outliers at 1000s of DAC values. The pixels either stay on or close to 0 when subtracted, or they had a missing baseline and have the maximum or minimum difference. This proves that it is not just the mean that is staying roughly similar at each temperature, it is also that the individual pixels are not changing significantly. This consolidates the claim that the difference between equalisations at the different temperatures is negligible and so new equalisations do not need to be run when the telescope is cooled, saving the collaboration valuable time.

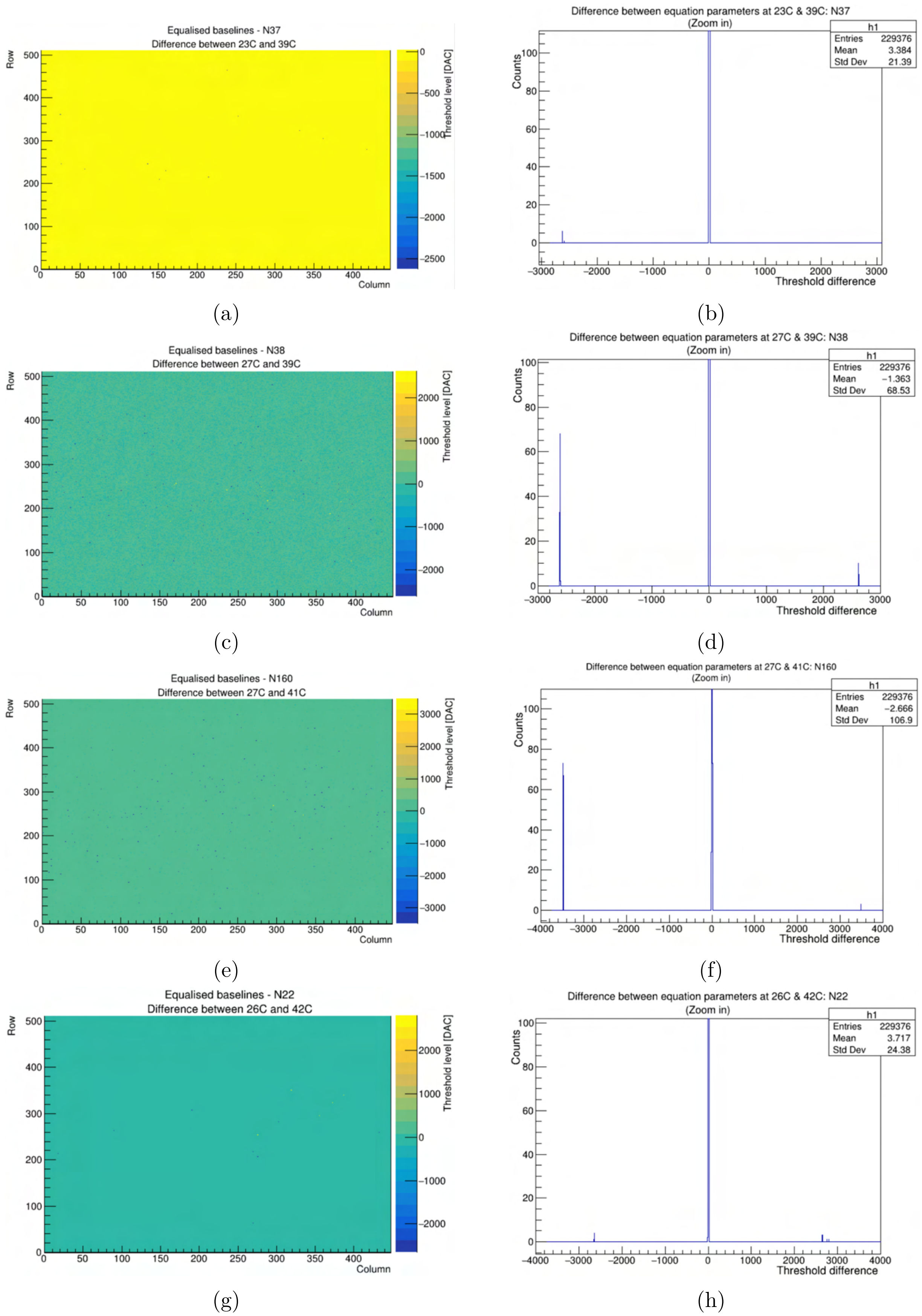


Figure 7.2: 2D histograms of the Timepix4 pixel matrix showing the subtracted thresholds at the maximum and minimum temperature (left) and 1D histograms of the difference between the threshold values at the max and min temperature, zoomed in on the y-axis (right).

7.3 Low Power Mode

So far, all the equalisations have been run using the timing-optimised settings for the ASICs that push the timing resolution as much as possible. Further investigations were completed using the low power mode settings that reduce the current draw of the ASIC and cause it to operate at a lower temperature during data taking. Due to time constraints, only N160 was measured in this way. The results of this are shown in table 5.

N160 was equalised in the "normal" timing-optimised mode first, as it had been some time since the ones displayed in table 3. This was necessary as is shown by the large difference between the number of out-of-range between this time and the previous. The equalised mean and standard deviation are different in the low power mode vs the timing mode. This is expected as the low power mode aims to reduce the current draw and thermal output of the ASIC by reaching a compromise between the power and the noise level, as shown by the higher standard deviation. The more aggressive timing mode pushes this much further, having significantly less noise which provides a better timing performance, at the cost of a larger current draw and higher thermal output. A new equalisation will have to be performed if the ASIC is to be used in low power mode. The two temperature data sets in low power mode also show no difference in the equalised mean, and the same previously noticed trend of slight increase in standard deviation at the colder temperature. The major difference is the number of out-of-range and missing baseline pixels. For low power mode, the number of out-of-range pixels is an order of magnitude larger than that of the timing mode. Also, the number of missing baselines is doubled at the same temperature and tripled when 10 °C colder. The reason for this trend is as yet unknown.

Mode	Temp (°C)	Equalised Mean	Std Dev	Out-Of-Range	Missing Baselines
Timing	38.4	3484	2.2	692	597
Low Power	38.5	3550	3.5	5140	1258
Low Power	29.8	3550	3.9	6291	1701

Table 5: Table of temperature, equalised baseline mean, standard deviation, out-of-range and missing baselines for the N160 assembly in multiple modes.

8 Conclusion

The Timepix4 assemblies have been shown to follow IV curve theory well. They showed a reduction of leakage current as temperature decreases, due to a reduction of thermonic emission in the lattice. The temperature dependence of the depletion and breakdown voltages was found to vary from sensor to sensor, as these values are highly dependent on local geometry and doping profiles per sensor. The source of the breakdown was found to be avalanche multiplication in p-spray region between the guard ring and the pixel pad implants due to its negative temperature coefficient, which backs up conclusions from previous studies. It was shown that depletion voltage increases with sensor thickness as expected, however due to extrapolation the errors on the values deduced were significant and as such a d^2 dependence was not visible. It is concluded that when operating the telescope, the temperature should be monitored, with the knowledge that cooling down the planes may cause some of them to breakdown earlier.

The DAC scans showed good evidence that the voltage output change between the maximum and minimum temperatures is measurable, but in most cases negligible. However, if the temperature of the telescope planes was changed significantly further than what was measured in this study, they would likely need to be recalibrated for the required output.

The equalisations showed a clear trend that number of out-of-range or missing baseline pixels increases when moving from around 40 °C to around 25 °C. They also showed that the equalised mean tended to either stay constant or trend a few DAC values higher when the temperature was reduced, still to a negligible degree. The standard deviation of the equalisations also showed that the electronic noise increased slightly as the temperature reduced. The same trends were seen when using the low power settings rather than the timing settings, except there were considerably more out-of-range and missing baseline pixels. It can be concluded that the equalisations do not need to be retaken when operating the telescope in the temperature range measured in this study, which is a major benefit as this saves a lot of valuable time.

This study opens the door for the collaboration to begin using cooling on the telescope planes, as it is now clear what needs to be considered when this is done. It also helps to verify that any local temperature variations (caused by a badly attached cooling block, for example) for data that has been taken in the past is still accurate. It is, however, still recommended that a new cooling block be designed, one that applies even pressure across the back of the PCB. Cooling the telescope planes may allow them to gain a better timing resolution to increase the accuracy of the track reconstructions, and reduce the effects of radiation damage.

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