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Screening and Reliability Testing of Beam Loss Monitor Electronics at CERN

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Abstract

A new processing board (VFC-HD) was developed for the Beam Loss Monitoring system at CERN with the purpose to increase the system performance. To fulfil defined reliability requirements during the operation, a screening strategy is defined.

Validation tests of pre-series boards during the design phase assured the production quality and additional functional tests during the series-production performed at the manufacturer ensure that quality. After reception of the boards, thermal cycling and a Run-In at operational conditions are executed to eliminate infant mortality failures. The main part of this thesis is the preparation and performance of the various tests, the data acquisition and analysis as well as the identification of occurring failure mechanisms.

The results show that screening and accompanying tests are necessary. The functional test filtered around 8 % faulty boards and an additional high temperature test proved the robustness and high design quality of the VFC-HD. The temperature cycling triggered failures for almost 3 % of the tested boards mostly due to cleanliness issues. No hardware failure like a broken solder joint was observed. The failure-free powering at operational conditions determined a current minimum $MTTF$ bearing in mind that conservative assumptions were used and possible acceleration factors were not considered.

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Symbols

Symbol	Meaning	Unit
AF	Acceleration Factor	-
b	Shape Parameter	-
$d\vartheta$	Thermal Rate of Change	°C·min^{-1}
E_a	Activation Energy	eV
$f(t)$	Density Function	%
$F(t)$	Failure Probability	%
g_rms	Root Mean Square Acceleration	-
k	Boltzmann Constant	eV·K^{-1}
m	Temperature Range Exponent	-
$MTTF$	Mean Time To Failure	Time Unit
n	Cycling Frequency Exponent	-
N	Number of Cycles	-
NL	Noise	dB
r	Number of Failures	-
$R(t)$	Survival Reliability	%
SS	Screening Strength	%
t	Time	Time Unit
t_0	Failure-Free Time	Time Unit
T	Temperature	K
α	Confidence Level	%
η	Characteristic Lifetime	Time Unit
ϑ	Temperature	°C
$\lambda(t)$	Failure Rate	1·(Time Unit)$^{-1}$
X^2	Chi-Square	-

Abbreviations

Abbreviation	Meaning
ADC	Analog/Digital Converter
BIT	Built-In Test
BLM	Beam Loss Monitor
BLT	Block Transfer
BPM	Beam Position Monitor
CERN	Conseil Européen pour la Recherche Nucléaire
CPU	Central Processing Unit
CRC	Cycling Redundancy Check
DAB	Data Acquisition Board
DAC	Digital/Analog Converter
DDR	Double Data Rate
DUT	Device Under Test
EAM	Enterprise Asset Management
EEPROM	Electrically-Erasable Programmable Read-Only Memory
ESS	Environmental Stress Screening
FESA	Front-End Software Architecture
FMC	FPGA Mezzanine Card
FMECA	Failure Mode and Effect Critically Analysis
FPGA	Field-Programmable Gate Array
FTA	Failure Tree Analysis
GA	Geographical Address
GOL	Gigabit Optical Links
GPIO	General Purpose Input Output
GUI	Graphic User Interface
HPC	High Pin Count
HSSL	High Speed Serial Link
I^2C	Inter-Integrated Circuit
IRQ	Interrupt Request
JTAG	Joint Test Action Group
LBIS	LHC Beam Interlock System
LED	Light-Emitting Diode
LHC	Large Hadron Collider
Linac	Linear accelerator
MTF	Manufacturing and Test Folder
MTTF	Mean Time To Failure
NXCALS	Next CERN Accelerator Logging System
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
PS	Proton Synchrotron
PSB	Proton Synchrotron Booster

Abbreviation	Meaning
PSU	Power Supply Unit
RH	Relative Humidity
SEM	Secondary Emission Monitor
SFP	Small Form-factor Pluggable
SPS	Super Positron Synchrotron
TGV	Train à Grande Vitesse
TTL	Transistor-Transistor Logic
VME	Versa Module Europa

Indices

Index	Meaning
A	Accelerated
d	Function of the Number of Failures
J	Junction
m	Mean
max	Maximum
min	Minimum
O	Operational
p	Function of the Confidence Coefficient
T	Temperature
TC	Temperature Cycling

1 Introduction

Availability of machines is getting more and more important in all kind of industry sectors. Especially for large systems, reliability engineering is an essential part of the whole design process. In 2013 the company Takata KK started a recall of around 37 million vehicles due to defective airbags [1]. The costs for the recall sum up to 10 billion $ [2]. It is the largest automotive recall in history and was caused by a design fault of the inflator module [3]. This shows the impact of mistakes during product design. In all phases of the product development faults can occur. Particularly, since the complexity increases but the development time of products decreases. For this reason, it is important to follow a precise reliability procedure, as the costs per failure increase significantly between the individual phases: development process, manufacturing and the use of the product. Thus, the costs for error prevention raise from one phase to the other but the costs for internal and external failures are lower. [4]

A good example to show the importance of high availability is the Large Hadron Collider (LHC) shown in Figure 1.1 at the European Organization for Nuclear Research (CERN, “Conseil Européen pour la Recherche Nucléaire“) which is the biggest machine in the world. High availability is essential due to the high costs to run it which can be estimated at 125 000 CHF per hour [5]. In a ring of 27 km in circumference particles are accelerated to almost the speed of light. At top energy, the circulating beams store 13 TeV which is equal to the energy of a TGV at the speed of 150 $km \cdot h^{-1}$. [6]

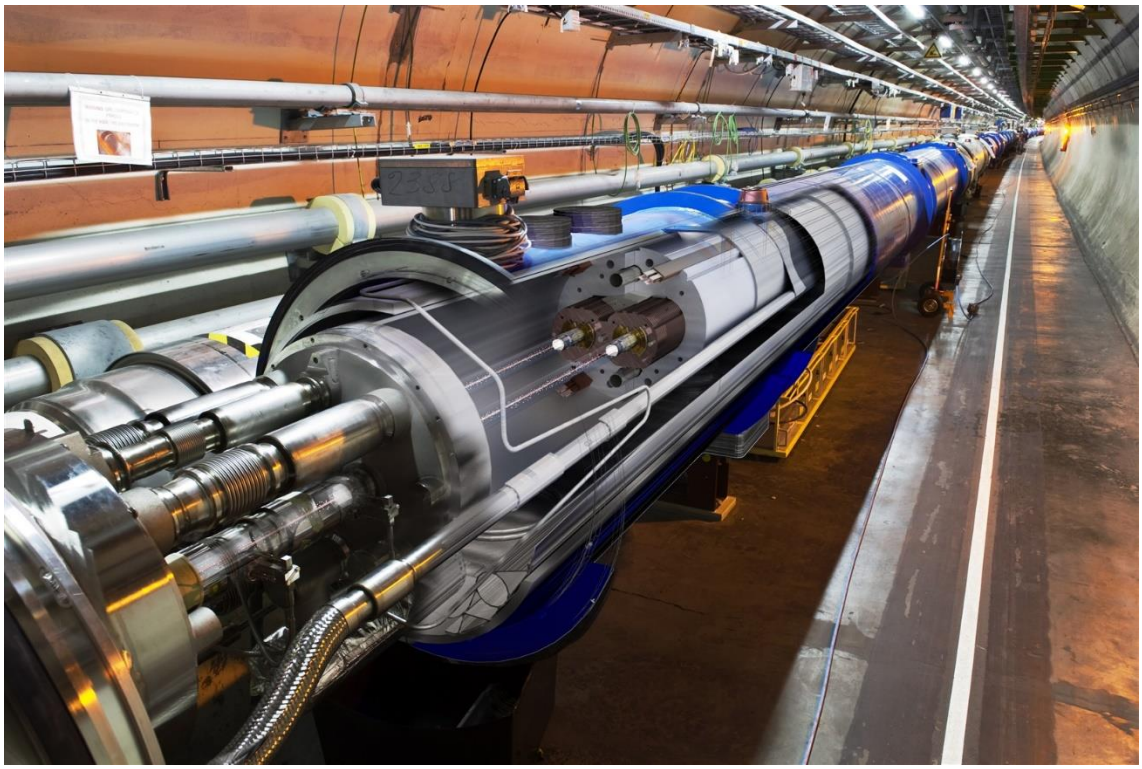


Figure 1.1: Cross section of an LHC dipole in the accelerator tunnel [7]

Due to this high energy level, it is necessary to circulate the particle beams safely. Therefore, several safety and protection systems exist at CERN which control the beam stability and react in case of wrong behaviour. A part of the machine protection system is the Beam Loss Monitoring (BLM) system. It detects beam losses through secondary particle showers and requests a beam dump if the losses are higher than predefined thresholds. For the surface installation of the BLM system, a new processing module named VME FMC Carrier HPC-DDR3 (VFC-HD) was designed. This board receives and processes data from the tunnel acquisition part. During the development, several reliability methods were executed, such as a Mean Time To Failure ($MTTF$) prediction or a Failure Mode, Effects and Criticality Analysis (FMECA). Afterwards, functional tests, validation tests and a screening process are performed. The screening comprises temperature cycling stress in a climatic chamber and in a second step powers the boards under normal operational conditions. The screening intends to filter the early in life failures to decrease the so-called infant mortality. By means of this testing, it is possible to determine the reliability of the VFC-HD.

2 Context and Background

Initially, CERN and the BLM system is presented. Then, the basics of reliability engineering for electronic systems with the focus on screening methods are introduced.

2.1 CERN

The European Organization for Nuclear Research (CERN) was founded in 1954 at the French-Swiss border region near Geneva. In this laboratory, amongst other employees, physicists and engineers research the fundamental structure of the universe. The world's largest and most complex scientific instruments are used to study fundamental particles. Used instruments are particle accelerators and detectors. Particle beams are accelerated to high energies before they are brought to collision with each other or with stationary targets. Detectors are used to observe and record the results of such collisions. This process gives insight about particle interactions and fundamental laws of nature. The accelerator complex at CERN is shown in Figure 2.1. [8]

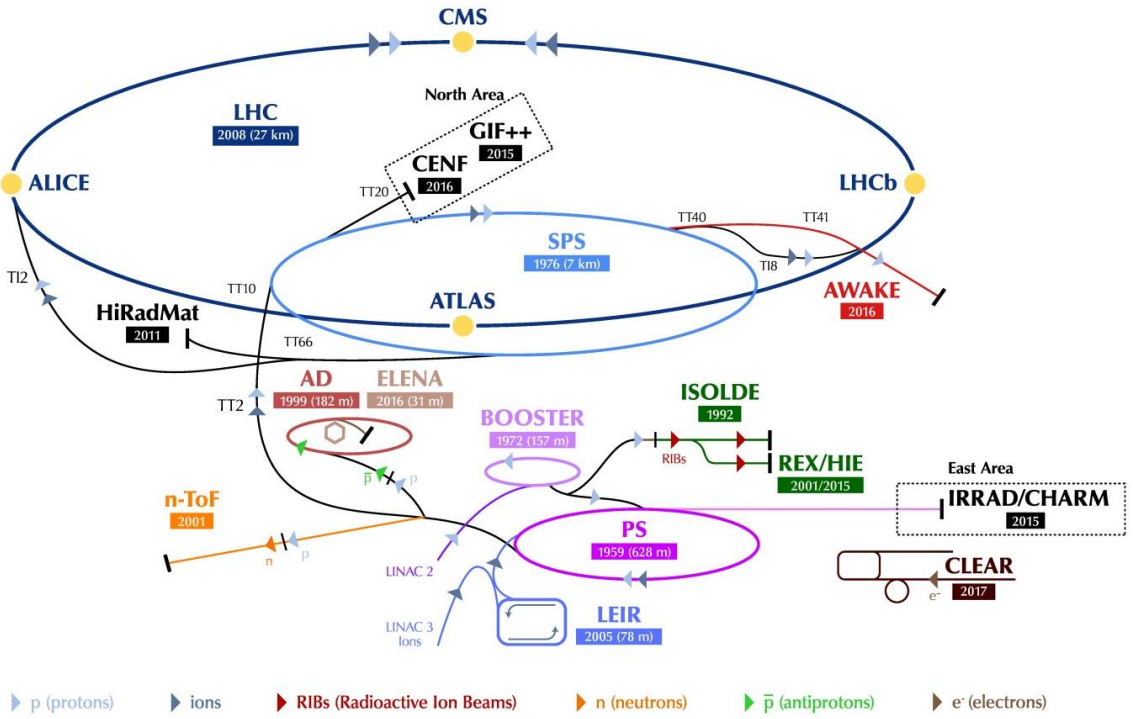


Figure 2.1: The accelerator complex of CERN [9]

At the beginning of the accelerator chain, a bottle of hydrogen gas serves as a source for protons. An electric field is used to strip hydrogen atoms off their electrons to yield protons. The first accelerator in the chain is currently the Linear accelerator (Linac) 2 which accelerates the protons to the energy of 50 MeV. Afterwards, the beam is injected to the Proton Synchrotron Booster (PSB), the Proton Synchrotron (PS) and the Super Proton Synchrotron (SPS) before

finally being transferred to the Large Hadron Collider (LHC). There are two particle beams in different pipes which circulate in opposite directions and are currently accelerated up to the energy of 6.5 TeV. The beams are brought into collision inside the four detectors ALICE, ATLAS, CMS and LHCb. Most of the other accelerators in the chain have their own experimental areas where beams are used for experiments at lower energies. Besides protons, there are also lead ions accelerated in the LHC. [10]

The LHC is the largest and most powerful particle accelerator in the world and sits in a tunnel around 100 m below the surface. It consists of a ring of different magnets which are built from coils of a special material that operates in a superconducting state. To conduct the electricity efficiently, nearly without resistance or energy loss, the magnets need to be chilled down to 1.9 K. 1232 dipole magnets bend and 392 quadrupole magnets focus the beams. Prior to the collision, another type of magnet is used to squeeze the particles closer together to increase the chances of collisions [11]. In one second a beam revolves 11 245 times which is equal to around 1 billion particle collisions. The experiments of the LHC produce around 30 petabytes of data per year and the total power consumption of the LHC is 600 GWh per year. [12]

2.2 Beam Loss Monitoring System

The strategy for machine protection of the LHC uses the BLM system of which the optical link is shown schematically in Figure 2.2. Data is constantly recorded and processed in real-time in order to decide if the beams should be permitted to continue circulating or their safe extraction is necessary [13]. In the case of beam losses above a predefined threshold, the system sends a beam inhibition request to the LHC Beam Interlock System (LBIS) which transmits it to the LHC Beam Dumping System (LBDS). As a result, the beam is extracted before it damages the equipment. It must be guaranteed that all dangerous losses are detected and that false alarms are kept to a minimum [14]. The majority of the BLM detectors are ionisation chambers and secondary emission monitors for regions with very high loss rates. The ionisation chamber consists of stacked parallel electrodes which are inserted in a stainless yellow steel tube. The chamber is filled with N_2 at 1.1 bar [15]. Both types of detectors are mounted horizontally on the outside of the cryostat of the accelerators. [16]

The electrical current generated by the beam loss inside the ionisation chamber is proportional to the secondary particle shower intensity. The signal is digitised by tunnel electronics and then transmitted to the surface by a redundant optical fibre link. One part of the tunnel electronics is an acquisition board called BLECF [17]. An Analog/Digital Converter (ADC) digitises the obtained signal and a Field-Programmable Gate Array (FPGA) processes it and performs system surveillance functions. 256 bits are transmitted every 40 µs. The tunnel FPGA sends two identical signals via Gigabit Optical Links (GOL) [14] which serialise the signal and transmit it via a laser diode. The fibres coming from the tunnel electronics are interfaced with a photodiode which converts the signal from optical to electrical. An input transceiver decodes this signal and sends it to the receiving FPGA of the current surface processing board (DAB64x). The board checks the signals and compares them with threshold values depending on the beam energy, beam position and other parameters. In case of losses exceeding these values, the DAB64x halts the beam permit-signal and sends a beam inhibition request to the

Combiner card. This card is interfaced with the redundant current loop signals of the LBIS and also responsible for the energy distribution received from the Safe LHC Parameter system [14].

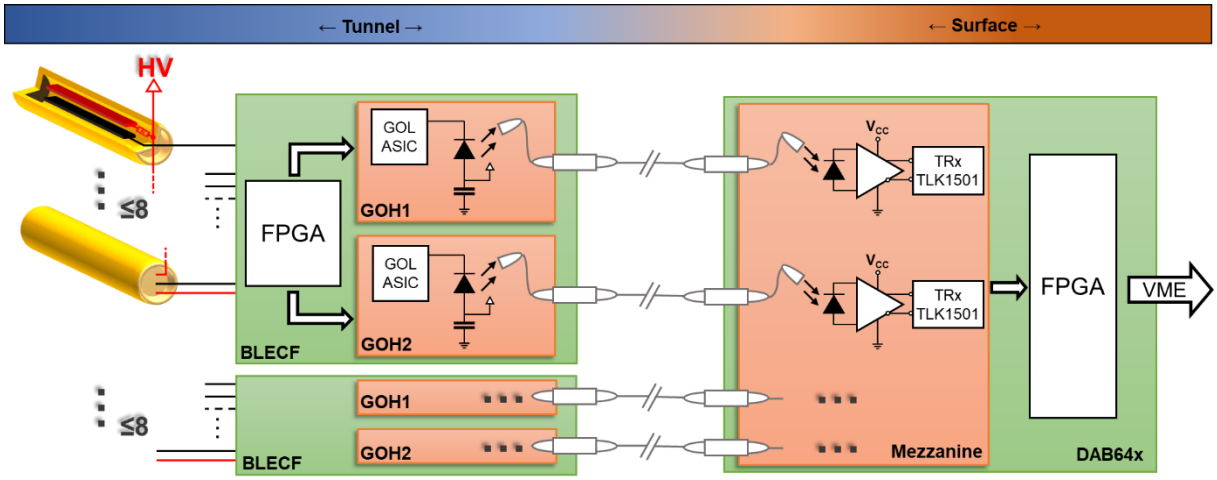


Figure 2.2: Schematic LHC Beam Loss Monitoring system optical link [18]

2.2.1 Current Surface Processing Module – BLETC

The currently installed threshold comparator module for the surface electronic is the BLETC. It uses the Versa Module Europa (VME) technology and comprises the DAB64x which provides the processing power. A mezzanine card links the tunnel with the surface installation by receiving the optical signals. The mezzanine card hosts the receiver parts for two redundant optical links which is equal to four physical fibre cables and handles the de-serialisation and decoding of the data transmission lines. [13]

The BLM system logging from 2012 to the end of 2017 shows in total 129 failures which are illustrated in Figure 2.3. As a consequence, a failure analysis of the BLETC and the connecting fibre link were executed with the conclusion to develop a new board [19].

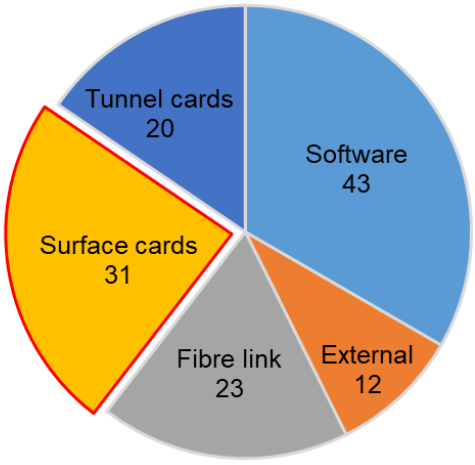


Figure 2.3: BLM failure logging between 2012 and the end of 2017 [19]

2.2.2 Future Surface Processing Module – VFC-HD

Because of the current system weaknesses mentioned in the previous chapter, the BLETC is to be replaced by the VFC-HD (Figure 2.5). The VFC-HD is a VME carrier board which was developed by the Beam Instrumentation group at CERN as a general purpose digital acquisition card for beam instrumentation back end systems. It is not only used by the BLM system but will be also installed in various other systems like for example in the Beam Position Monitoring (BPM) system. The percentage number of VFC-HD which later are used by the different systems is shown in Figure 2.4.

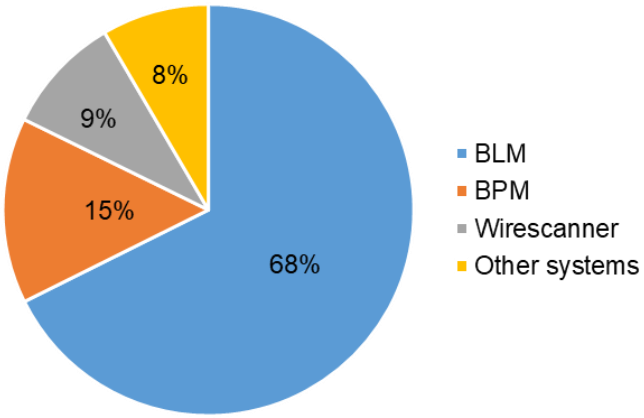


Figure 2.4: Percentage distribution of the VFC-HD to different systems

The architecture of the VFC-HD is shown in Appendix A. Around 1150 units of these 12 layer Printed Circuit Boards (PCB) are produced and have the following main characteristics [20]:

- Intel Arria® V GX FPGA
- High Pin Count (HPC) FPGA Mezzanine Card (FMC) slot
- 6 Small Form-factor Pluggable+ (SFP+) transceiver slots
- 2 DDR3 memories
- Flexible clocking resources
- VME64x standard with a custom P0 connector

To achieve better reliability for this module, the dependability design of the VFC-HD was influenced by lessons-learnt of the existing system in operation. The upgrade includes the usage of an SFP standard connector providing hot swap ability and additional diagnostic functions. This shall improve the current solution which uses a pigtail fibre cable glued onto the photodiode. Furthermore, the upgrade uses no mezzanine card but an identical reliable transmission of data via the redundant links. The VFC-HD continues to use the same tunnel electronics and fibre link. Only an E2000/LC optical fibre patch cord is added to link the different optical connector systems. [19]

After the definition of all board specifications, an $MTTF$ prediction and an FMECA were prepared during the design phase. The $MTTF$ prediction created 1200 component blocks using the bottom-up approach. This resulted in a predicted $MTTF$ of 600 000 h for the BLM system. The parts count method determined operational parameters for all mounted components and combined them with either component manufacturer data or models according to the

“Handbook of 217Plus™ Reliability Prediction Models” [21]. In a following step, the critical parts of the system were classified by the FMECA. Functional blocks were defined to which failure modes and effects were assigned. The FMECA end effects are classified by four severity levels:

1. False beam dump request
2. Immediate maintenance required
3. Scheduled maintenance
4. No effect

In this way, failure modes having no effect on the system level can be excluded. For the remaining critical system parts, an $MTTF$ of 750 000 h was determined for the BLM system. [22]

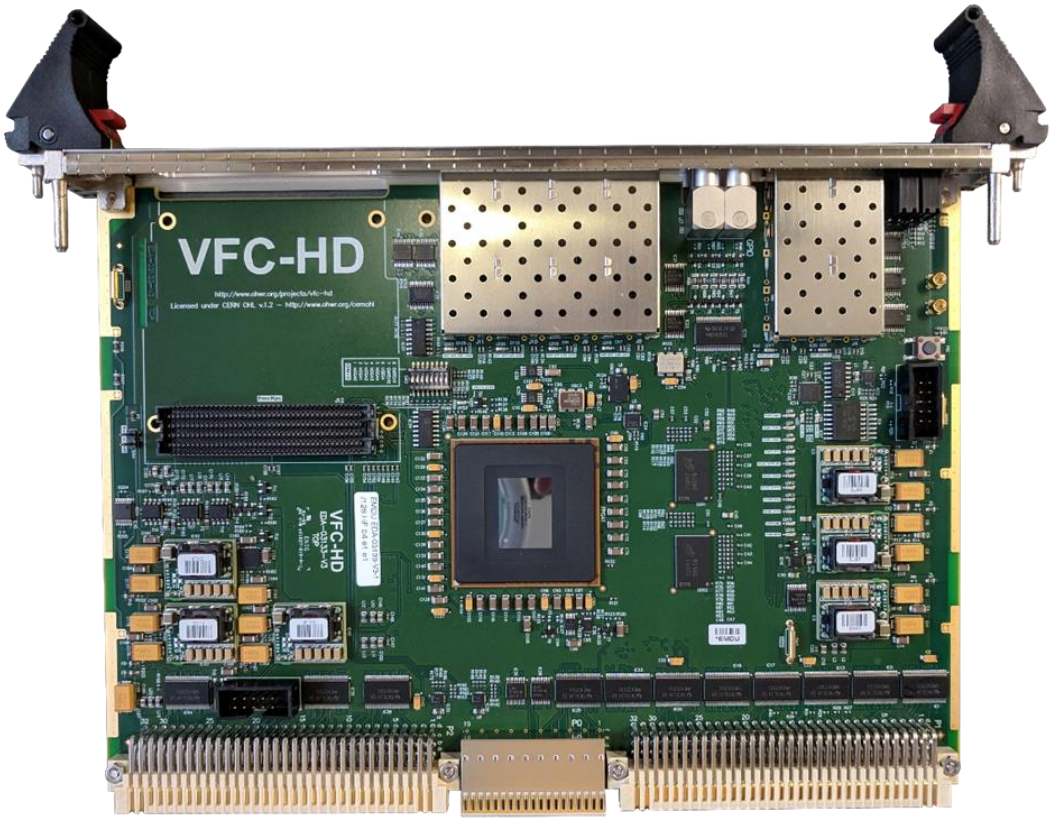


Figure 2.5: The VFC-HD from the top view

2.2.3 Validation of the VFC-HD

Previous to this work, two types of validation tests were implemented to ensure that the VFC-HD meets the design specifications. Firstly, a selection of boards underwent temperature-humidity cycling and secondly, high temperature tests were executed.

Temperature-Humidity Cycling

The first validation test performed combined humidity and temperature cycling with two boards of the pre-series production. For fibre communication, experiences with the previous system

showed errors starting at temperatures of around 25 °C and a high error rate above 30 °C. Relative Humidity (RH) measurements inside the temperature controlled (25 °C) racks of the current BLM system range from 10 % to 75 % and indicate a failure correlation. Bearing this data in mind, the validation test was designed to assess the environmental tolerances of the new system. A temperature range from 5 °C to 55 °C and RH between 10 % and 90 % were determined. Each of the two boards was equipped with six optical transceivers and different setups were prepared to loop back the optical fibre connections of the transceiver modules [23]:

1. 3.5 dB attenuation electrical loopback SFP+ adapter
2. LC-system fibre loopback
3. LC/E2000-systems loopback with adapters

After proving their functionality at nominal conditions, 11 tests at different stresses were performed. The results showed no VFC-HD failures, no errors with the 3.5 dB SFP loopback adapter but various SFP fibre loopback errors. The following summarises the validation results [23]:

- $\vartheta_{max} = 30\,℃\ for\ RH \leq 80\,\%$
- $\vartheta_{max} = 40\,℃\ for\ RH \leq 50\,\%$

High Temperature Test

This test validates the system at its design limits as well as aims to trigger failure mechanisms. The VME crate was partly placed outside the climatic chamber and was connected to one board inside via 1 m long cables for three backplane connectors. The test was executed for three boards of the pre-series and was repeated with a board of the first series batch. The temperature was raised in small steps from the maximum design temperature (Equation 2.1). This maximum test temperature ϑ_{test} for the VFC-HD is determined by subtracting the temperature increase at the semiconductor junction $\Delta\vartheta$ due to the FPGA's power dissipation from the maximum recommended junction temperature $\vartheta_{J,max}$ of the used Arria® V GX version [23]:

$$\vartheta_{test} = \vartheta_{J,\max} - \Delta\vartheta = 85\,℃ - 31\,℃ = 54\,℃ \tag{2.1}$$

Therefore, the initial temperature was set to 50 °C and the temperature was increased in steps of 5 °C.

All three boards passed the test without hardware failure. No failures occurred for the electrical SFP loopback modules. FMC issues occurred at elevated temperatures but were due to the test firmware at that time. Later upgrades solved the issue. The internal FPGA temperature reached a maximum of 127 °C which is above the given maximum junction temperature of 125 °C. [23]

2.3 Reliability

In the following subsections, the necessary fundamentals of reliability engineering are presented. In particular, screening methods for electronics are introduced and compared.

2.3.1 Fundamentals

According to the VDI 4001 standard reliability is defined as “the probability that a product does not fail under given functional and environmental conditions during a defined period of time” [24].

The failure probability also called the distribution function $F(t)$ describes the probability at which failures occur depending during a certain time t. The following equation shows that $F(t)$ represents the sum of failures as a function of time:

$$F(t) = \int f(t)dt \tag{2.2}$$

Rearranging the equation above, the density function $f(t)$ can be expressed:

$$f(t) = \frac{dF(t)}{dt} \tag{2.3}$$

For many applications it is interesting to see the sum of systems which are still intact. This can be displayed using a histogram of the survival frequency. The histogram is obtained by subtracting the number of defect units from the total number of components or machines for a certain time interval. Consequently, the survival probability $R(t)$ is the complement of the failure probability. [25]

$$R(t) = 1 - F(t) \tag{2.4}$$

For a better understanding of how the density function relates to the failure and survival probability, Figure 2.6 explains this state as a function of the time. [25]

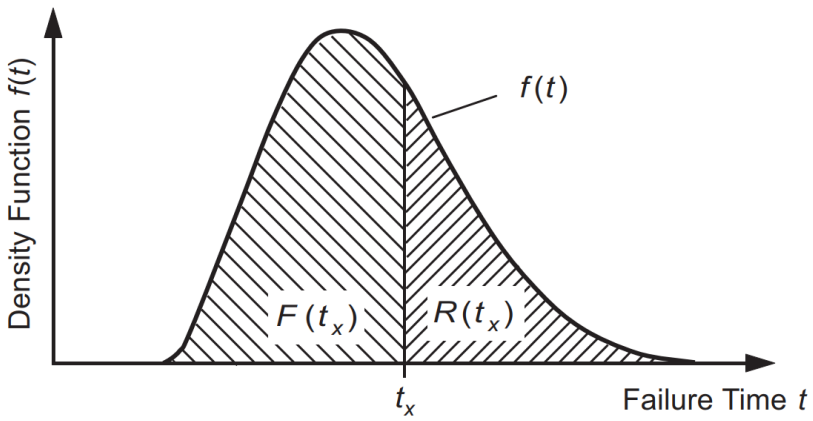


Figure 2.6: Density function as a function of the failure time [25]

Another important reliability variable is the failure rate $\lambda(t)$. It describes the failures at the point of time divided by the sum of units still intact. Furthermore, the failure rate can be calculated as the quotient of the density function $f(t)$ corresponding to the number of failures and the survival probability $R(t)$ which describes the number of units still intact. [25]

$$\lambda(t) = \frac{failures}{sum\ of\ units\ still\ intact} = \frac{f(t)}{R(t)} \tag{2.5}$$

2.3.2 Lifetime Distributions

There are different types of distributions to mathematically describe different failure characteristics in time. The most widely used statistical distribution is the normal distribution. However, it is of limited use in reliability engineering. The Weibull distribution is the most common lifetime distribution used to describe the failure behaviour of mechanical systems, while the exponential distribution is often used to describe the failure behaviour of electronic components. The log-normal distribution is sometimes used in material science. In this thesis, only the Weibull and the exponential distribution are explained in detail. [25]

Weibull Distribution

With the Weibull distribution, various failure behaviours can be described. Illustrated by the density function in Figure 2.7, only one of the distribution parameters, the shape parameter b, is varied. For values lower than 1, the failure behaviour can be described as being similarly to the exponential distribution. The exact exponential distribution results for $b = 1$. If the shape parameter is higher than 1, the density function always begins at $f(t) = 0$, reaches a maximum with increasing lifetime and decreases slowly again. The normal distribution can be approximately reproduced for $b = 3.5$. [25]

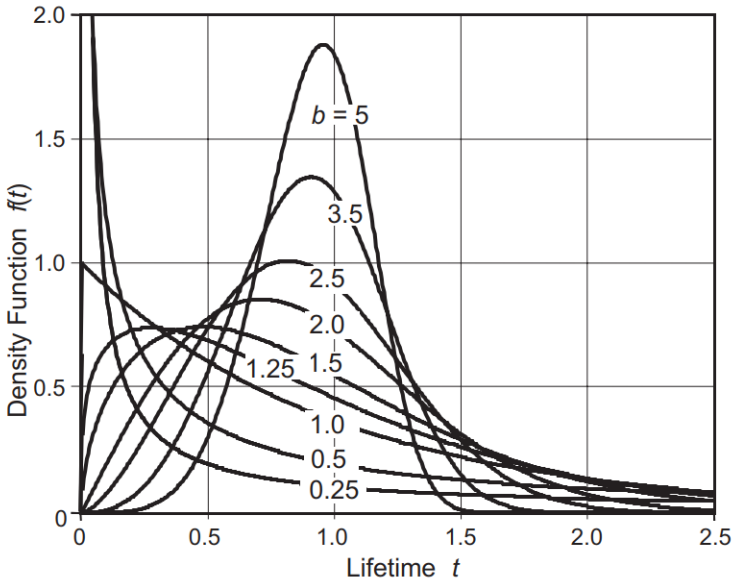


Figure 2.7: Density function for different shape parameters [25]

The Weibull distribution is divided into a two-parametric and a three-parametric distribution. The two-parametric distribution exhibits the characteristic lifetime η and the shape parameter b. The characteristic lifetime, also called scale parameter, is an estimate of the mean and shows the location of the distribution. The shape parameter is a measurement for the statistical spread

of the failure times. The two-parameter Weibull distribution always starts at the time $t = 0$. Additional to the scale and shape parameter, the three-parametric Weibull distribution exhibits a location parameter for a failure-free time t_0. Only failures that occur after a certain time t_0 are described. The three-parametric distribution can be derived from the two-parametric distribution. The equations for the two-parametric Weibull distribution are listed in Table 1 to give an overview of the difference to the exponential function. [25]

Table 1: Equations of the Weibull distribution [25]

Reliability Probability	$R(t) = e^{-\left(\frac{t}{\eta}\right)^b}$	(2.6)
Failure Probability	$F(t) = 1 - e^{-\left(\frac{t}{\eta}\right)^b}$	(2.7)
Density Function	$f(t) = \frac{dF(t)}{dt} = \frac{b}{\eta} \cdot \left(\frac{t}{\eta}\right)^{b-1} \cdot e^{-\left(\frac{t}{\eta}\right)^b}$	(2.8)
Failure Rate	$\lambda(t) = \frac{f(t)}{R(t)} = \frac{b}{\eta} \cdot \left(\frac{t}{\eta}\right)^{b-1}$	(2.9)

Exponential Distribution

The density function of the exponential distribution decreases steadily from its starting point as an inverse exponential function. The failure behaviour is described by starting with a high failure frequency and then decreases continuously. The constant failure rate is a significant characteristic of the exponential distribution and it is independent of time. The exponential distribution is used for random failures. One feature is that the same proportion of parts fail relatively to the number of parts remaining. The equations for the exponential distribution are listed in the following Table 2. [25]

Table 2: Equations of the exponential distribution [25]

Reliability Probability	$R(t) = e^{-\lambda t}$	(2.10)
Failure Probability	$F(t) = 1 - e^{-\lambda t}$	(2.11)
Density Function	$f(t) = \lambda \cdot e^{-\lambda t}$	(2.12)
Failure Rate	$\lambda(t) = \text{const.}$	(2.13)

A common parameter to characterise electronics reliability data is the Mean Time To Failure. It specifies the mean for the time without failures for an observed period of time. The $MTTF$ can be calculated as [25]:

$$MTTF = \int_0^\infty t \cdot f(t)dt = \int_0^\infty R(t)dt \tag{2.14}$$

In the case of the exponential distribution, the $MTTF$ is calculated as:

$$MTTF = \int_0^\infty e^{-\lambda t}dt = \frac{1}{\lambda} \tag{2.15}$$

2.3.3 Bathtub Curve

The failure rate is used to describe early, random or wear out failures. The objective is to gather the complete failure behaviour of a part or a machine. The result is illustrated in Figure 2.8. It shows a typical shape which is known as the "bathtub curve". There are three distinct sections which characterise the curve: early failures, random failures and wear out failures.

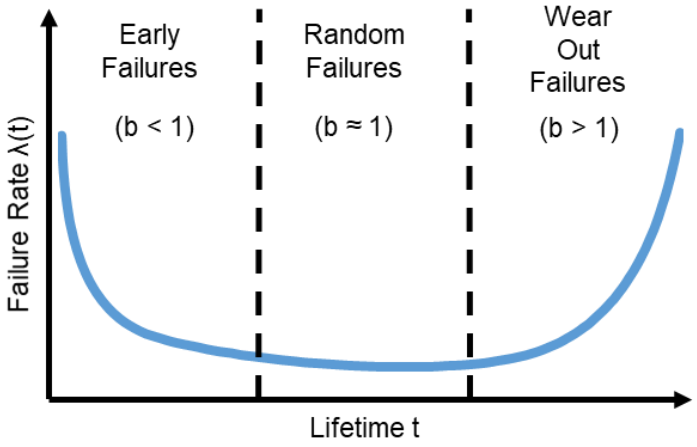


Figure 2.8: Bathtub curve divided in three sections [25]

The first section is characterised by a decreasing failure rate. With increasing time the failure rate reduces. Early failures are usually caused by failures in the production, assembly, material or by a definite design flaw. In the second section $\lambda(t)$ is almost constant because in this area some early failures still occur so that the failure rate alternates while decreasing slightly. In the following the shape parameter is assumed to be 1 for this region. The random failures are normally impossible to pre-estimate because they can be provoked by operating or maintenance failures or by dirt particles. In section 3, the failure rate increases because wear out failures occur. These failures are caused by fatigue failures, ageing or pitting. The bathtub curve not only characterises the failure behaviour for complex systems, but also differs failure distributions to visualise different behaviours in the individual sections. The three sections can also be divided by the shape parameter b as shown in the following Table 3. [25]

Table 3: Relation between the Weibull shape parameter b and the bathtub curve

Shape Parameter	Description	Section in Bathtub Curve
b < 1	With increasing lifetime the failure rate decreases	1. Early failures
b = 1	The failure rate is constant	2. Random failures
b > 1	With increasing lifetime the failure rate increases drastically	3. Wear out failures

2.3.4 Confidence Intervals

A confidence interval is characterised by the probability that a variable is located within a certain interval. A 90 % confidence interval indicates that 90 out of 100 cases observed are within this interval. For instance, the 90 % confidence interval is limited by a 5 % and a 95 % confidence limit which is also shown in Figure 2.9. [25]

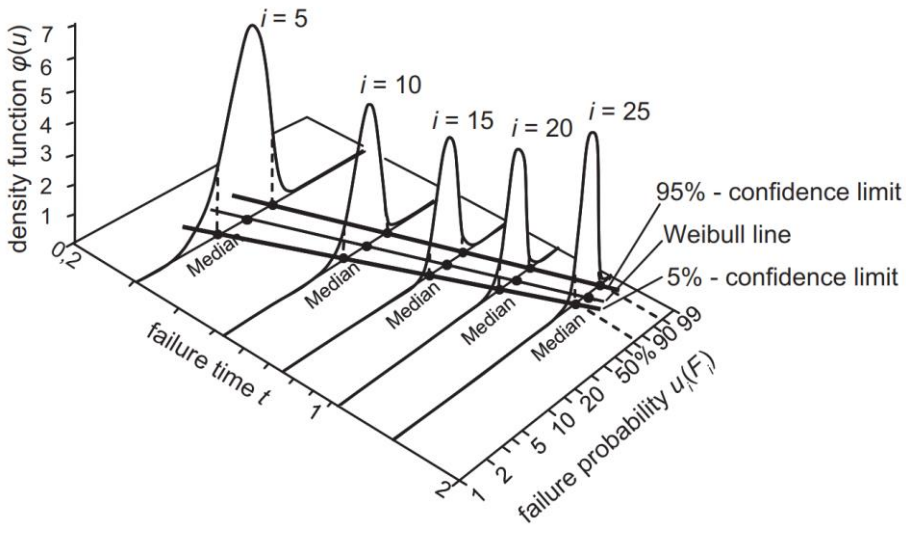


Figure 2.9: Confidence interval of a Weibull distribution [25]

There are two different situations for an exponential distribution to estimate the confidence interval for an $MTTF$ obtained by test data. In one, the test runs until a preassigned number of failures occur and in the other in which the test is stopped after a preassigned time. The equation for the confidence interval employs the X^2 (chi-square) distribution. The conventional notation used is $X^2_{p,d}$. The quantity p is a function of the confidence coefficient and d of the number of failures. The different equations are shown in the following Table 4. [26]

Table 4: Confidence intervals according to [26]

MTTF	**Fixed Number of Failures**	**Fixed Truncation Time**
One-sided (lower limit, ∞)	$\left(\frac{2 \cdot t}{\chi^2(\alpha, 2 \cdot r)}, \infty\right)$	$\left(\frac{2 \cdot t}{\chi^2(\alpha, 2 \cdot (r+1))}, \infty\right)$
Two-sided (lower limit, upper limit)	$\left(\frac{2 \cdot t}{\chi^2\left(\frac{\alpha}{2}, 2 \cdot r\right)}, \frac{2 \cdot t}{\chi^2\left(1-\frac{\alpha}{2}, 2 \cdot r\right)}\right)$	$\left(\frac{2 \cdot t}{\chi^2\left(\frac{\alpha}{2}, 2 \cdot (r+1)\right)}, \frac{2 \cdot t}{\chi^2\left(1-\frac{\alpha}{2}, 2 \cdot r\right)}\right)$

The terms used are defined as:

t = Total test time

α = Acceptable risk of error

r = Number of failures accumulated at time t

2.3.5 Screening Methods

Electronic systems experience a higher failure density at the beginning of their lifetime which decreases after a certain time to a lower constant failure rate. To enter this second region, called the “useful lifetime”, it is necessary to screen the population for early in life failures. In the following paragraphs, screening is introduced generally until several screening test strategies are presented and put in contrast to each other. [27]

Screening is a verification testing process of finding which components or assemblies of a production batch are defective without weakening or causing failure of good parts [28]. The goal is to pre-empt potential reliability problems before the parts are being installed. That is also the reason why the screening involves 100 % of the manufactured products to detect or precipitate all defects. These failures, often called infant mortality, exist due to the use of faulty materials, poor manufacturing or mishandling. By eliminating those failures they will not occur in field use. Burn-In and Environmental Stress Screening (ESS) [29] are two typical screening methods for electronics which are performed on either the part, unit, or system level. Both methods aim to reduce early field failures but there are differences in how to execute them and their purpose. For Burn-In, the tested item is powered, the stress level is low compared to ESS and the test duration reaches from several hours up to a few days. For ESS, the stress level is commonly more diverse and the test duration reaches from several minutes up to hours. Environmental Stress Screening is more effective to precipitate stress-dependent defects which result in overstress failure, but it is less effective for defects caused by time or usage-dependent failure modes. On the contrary, Burn-In is used to precipitate time- and usage-dependent defects providing useful information for predicting reliability performance of the product [29]. Temperature and vibration are widely used stresses to accelerate but voltage, humidity, electric fields or current density are also applicable [30]. The failure modes and mechanisms must be known to determine which stress condition and magnitudes precipitate failures. Screening is justified when the costs are lower than the consequential costs of not screening or when the

expected proportion defective is sufficiently high that early removal improves yield in later tests and reliability in operation.

Table 5 summarises different screening methods, which are explained more precisely in the following subchapters. Based on those methods the later chosen screening strategy for the VFC-HD is described in chapter 3.3.1.

Table 5: Overview of screening methods

Standard/ Publisher	Type	Temperature Range [°C]	Thermal Rate of Change [°C·min^{-1}]	Number of Cycles	Dwell Time	Vibration	Year of Issue
MIL-STD-883E [31]	High-Temperature	175 – 250	-	-	48 – 12 h	-	1996
MIL-STD-883E [31]	Thermal Cycling	-65 – 175	16	≥ 10	≥ 10 min	-	1996
ESS Guide [32]	Thermal Cycling	-50 – 75	5 – 20	≥ 20	Until thermal stability	-	1989
MIL-HDBK-781A [33]	Thermal and Vibration Cycling	-54 – 85	5 – 20	6 – 8	Until thermal stability	≥ 10 min	1996
Birolini [27]	Thermal and Vibration Cycling	0 – 80	1 – 5	100	≤ 10 min after thermal stability	15 min at 2 g_{rms}, 20 – 500 Hz	2017

In addition, Table 6 shows the application of the above listed screening methods. The ESS Guide and MIL-HDBK-781A mention besides the chosen parameters also adaptations for other screening levels.

Table 6: Application of the screening methods

Standard/Publisher	Application
MIL-STD-883E (High Temperature)	Microcircuits
MIL-STD-883E (Thermal Cycling)	Microcircuits
ESS Guide	• Assembly level screening • Different requirements for lower or higher level of assembly • Parameters for unit and system level screening also exist

MIL-HDBK-781A	Distinguishes in complexity of equipment: • Simple: 100 parts • Moderately complex: 500 parts • Complex: 2000 parts • Very complex: 4000 parts
Birolini	Assembly level screening

MIL-STD-883E

The Military Standard MIL-STD-883E (method 1015.9) defines Burn-In proposing different test conditions with various types of stresses:

- Test condition A: Steady-state, reverse bias
- Test condition B: Steady-state, forward bias
- Test condition C: Steady-state, power and reverse bias
- Test condition D: Parallel excitation
- Test condition E: Ring oscillator
- Test condition F: Temperature-accelerated test

In this case, the test condition F is explained more in detail. During the temperature accelerated test, microcircuits are subjected to bias at temperatures of 175 °C to 250 °C (Table 7) which exceeds the maximum junction temperature. Microcircuits are not operating normally at these elevated temperatures and it is therefore necessary that special attention is given to the choice of bias circuits and the conditions to assure that nothing is damaged by overstress. The minimum time and temperature for the accelerated test are:

Table 7: Minimum temperature and time for temperature accelerated tests [31]

Minimum Temperature ϑ_A [°C]	**Minimum Time t_A [h]**
175	48
200	28
225	16
250	12

For temperature cycling, method 1010.7 is conducted to determine the limiting resistance of a part at high and low temperatures. The test conditions are listed in Table 5. [31]

ESS Guide

The Environmental Stress Screening Guide [32] distinguishes screening on the assembly and unit level which requires the design and fabrication of specialised test equipment. The applied stress during assembly and unit level testing should not be as severe as during part level. For a higher level of assembly, the equipment is more vulnerable to damage and the stress must be adapted accordingly. The purpose of unit or system level screening is to trigger defects in

fasteners and interconnections between PCBs, subassemblies and assemblies. Screening at this level is important because it is the first opportunity to detect defects from final assembly operations which would otherwise occur in field use. The following screening methods exist which can be used at the assembly level to precipitate and detect latent defects:

- Thermal Cycling
- Random Vibration
- Immersion
- Overpressure
- Voltage Variation

Each of these screening methods primarily provokes specific types of defects, although some have overlapping capabilities. The choice of the method depends on the types of defects expected to be triggered in field-use. Thermal cycling and random vibration have been found to be the most effective screen for electronic systems and are therefore the most widely used. Both work well to uncover microscopic defects which can be present in electronics. The following Table 8 shows the types of defects which can be triggered by thermal cycling and random vibration. [32]

Table 8: Defect type detected through thermal or vibration screen [32]

Defect Type Detected	**Thermal Screen**	**Vibration Screen**
Defective part	X	X
Broken part	X	X
Improperly installed part	X	X
Solder connection	X	X
PCB etch, shorts, and opens	X	X
Loose contact	-	X
Wire insulation	X	-
Loose wire termination	X	X
Improper crimp or mating	X	-
Contamination	X	-
Debris	-	X
Loose hardware	-	X
Chafed, pinched wires	-	X
Parameter drift	X	-
Hermetic seal failure	X	-
Adjacent boards/parts shorting	-	X

The least controversial and most widely used stress method is thermal cycling. It is a powerful screen to precipitate defects at all levels of assembly from PCBs to complete end items. This

method is a relatively inexpensive screen, especially when performed at PCB assembly level where several units can be tested simultaneously in a climatic chamber. In order to induce stress on the parts, thermal cycling consists of changing the equipment's temperature at a fairly high rate of change. Three main parameters determine the strength of the screen:

- Temperature range
- Thermal rate of change
- Number of cycles

The temperature range and the rate of change must be specified as unit temperature values, not as climatic chamber air temperature values. The screened equipment has a larger thermal mass than the climatic chamber air, thus the equipment response lags behind the input stress (Figure 2.10). Due to the temperature change, the test items expand and contract. The repeated cycling causes different materials to expand and contract at different rates, resulting in stress at junction points such as connections and solder joints. Microcracks, voids or material impurities cause stress concentrations from fatigue build-up while there is no significant stress concentration on good connections. The low temperature precipitates electrical shorts due to condensation while the high temperature accelerates part failure mechanisms. The equipment should be powered up and monitored in order to identify defects that are only detectable under certain environmental conditions. [32]

The temperature cycling should be performed on all items. Therefore, it is necessary to determine the requirements according to the screen strength. Thermal cycling is a much stronger screening method than a high temperature Burn-In or ambient Burn-In. The strength of the screen is defined as the probability that the screen is precipitating a possible defect and is determined by the following equation:

$$\mathrm{SS_{TC}} = 1 - \exp(-0.0017 \cdot (\Delta\vartheta + 0.6)^{0.6} \cdot (\ln(\mathrm{e} + \mathrm{d}\vartheta))^3 \cdot \mathrm{N}) \tag{2.16}$$

- SS_{TC}: Thermal Cycling Screening Strength
- $\Delta\vartheta$: Temperature range ($\vartheta_{\max} - \vartheta_{\min}$)
- $d\vartheta$: Thermal rate of change
- N: Number of cycles

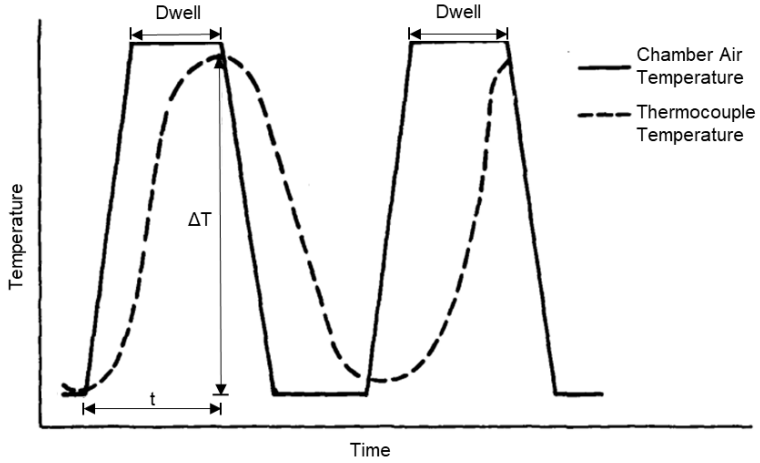


Figure 2.10: Thermal cycle profile [32]

The temperature range for PCB assemblies should be as large as component characteristics permit, but the nominal range is -50 °C to 75 °C. If the PCB contains parts which have ratings smaller than the nominal values, the temperature range should be limited but at least 110 °C temperature difference should be applied. If this is not possible, more cycles or a higher thermal rate of change can be used to increase the screening strength. [32]

The stress of interest is the thermal rate of change of the individual parts and depends on the climatic chamber performance and the size of the hardware as well as the individual thermal resistance. The rate should fall between 5 °C·min^{-1} and 20 °C·min^{-1} with higher rates providing a better screen. The thermal rate of change should be determined by a thermocouple on the electronic component and not by the temperature of the input air because of the higher thermal capacitance of the PCB. [32]

The required number of cycles is more closely related to the temperature range and the rate of change than to the equipment complexity or number of parts. There should be at least 20 cycles for PCBs with more required if the rate is less than 15 °C·min^{-1} or the range is less than 110 °C. The number of cycles should be increased by 5 for every drop in the rate of change of 5 °C·h^{-1} or for every 10 °C drop in temperature range below 110 °C. [32]

The dwell time should be only long enough to reach thermal stability which is achieved when the thermocouple of the PCB comes within 2 °C of the temperature extreme or when the rate of change falls below 2 °C·h^{-1}. [32]

MIL-HDBK-781A

According to MIL-HDBK-781A [33], ESS assures that amongst the already mentioned production impacts, also quality control procedures and the accumulation of design changes do not degrade the original reliability. The screening procedure is applied to the whole system and if possible the system is powered and operated when put under environmental stress. All items are subjected to a series of stress cycles consisting of thermal or vibration stress or a combination of both. Typically, the equipment is stressed until a minimum of one failure-free interval is attained. This standard describes thermal and vibration stress as an ESS method. [33]

Historical data indicates that thermal immerse do not contribute significantly to screening effectiveness, therefore, the dwell time at high and low temperatures need to be long enough that the internal temperature stabilises. It follows that each successive thermal ramp should be started after the internal parts have stabilised within 2 °C of the specified temperature. The best screening result is achieved by using the maximum practicable temperature rate of change of internal parts. The equipment performance should be monitored continuously, but if costs or other constraints do not permit this, periodic checks and the monitoring of the final cycle is sufficient. [33]

The vibration stress method consists of random vibration which should be applied for at least 10 minutes if the direction is along a single axis. When vibration along more than one axis is required, the stress should be applied for at least 5 minutes along each axis. The equipment must be hard-mounted to the shake table so that the direction of stress is perpendicular to the plane of the PCBs. [33]

Birolini – Reliability Engineering

Birolini implies in [27] that for a PCB with about 500 components and 3000 solder joints, 0.5 % to 2 % defective PCBs can be found with a mean value of 1.5 defects per defective PCB during a screen of electronic assemblies. Considering such information, it is important to remember that defective PCBs are often reworked, which has a negative influence on the quality and reliability of a PCB. The screen of populated PCBs with higher integration level is generally a difficult task, because of the many different technologies involved. For a large number of PCBs used in high reliability or safety applications, the following screening procedure is recommended [27]:

1. Visual inspection and reduced electrical test
2. 100 thermal cycles from 0 °C up to 80 °C with a temperature gradient between 1 °C and 5 °C per minute, a maximum dwell time of 10 min after the thermal equilibrium has been reached within ± 5 °C and power off during cooling
3. 15 min random vibration at 2 g_{rms}, 20 Hz to 500 Hz
   (only to be performed if significant vibrations occur in the field)
4. 48 h Run-In at ambient temperature, with periodic power on/off switching
5. Final electrical and functional test

This procedure can be considered as an ESS, performed on a 100 % basis in series production of PCBs. In general, a screening strategy for PCBs should be established on a case-by-case basis and be periodically reconsidered depending on the percentage of early failures. [27]

2.3.6 Accelerated Testing

This chapter aims to introduce different ways to calculate additional stress through accelerated tests and not to present different types of test methods.

The failure rate of electronic assemblies lies typically between 10^{-7} and 10^{-5} h^{-1}. This demands the use of accelerated testing for a failure rate estimation and demonstration. An accelerated test applies stress which exceeds the encountered during field operation but still ranges below design limits. Possible early failure mechanisms are assumed to be activated by increased stress. [27]

The acceleration factor AF describes the quantitative relationship between the operational lifetime t_O and the lifetime during the accelerated test t_A [34].

$$AF = \frac{t_O}{t_A} \tag{2.17}$$

Generally, the type of the failure-free time distribution function of the device under test is not affected by stress [27]. Different models to determine the acceleration factor exist for thermal stress, three of them are presented in the following.

Arrhenius Model

Failure mechanisms of many electronic components are activated through temperature increase. The Arrhenius model is used to calculate the acceleration factor for higher temperatures than operational conditions [27]:

$$AF_T = e^{\frac{E_a}{k}\cdot\left(\frac{1}{T_\mathrm{O}}-\frac{1}{T_\mathrm{A}}\right)} \tag{2.18}$$

- k: Boltzmann constant ($8.623\cdot10^{-5}$ eV·K^{-1})
- T_O: Operational temperature
- T_A: Test temperature
- E_a: Activation energy

Coffin-Manson Model

The Coffin-Manson model considers three factors: maximum temperature, temperature change and cycling frequency. The acceleration factor for temperature cycling is calculated as:

$$AF_\mathrm{TC} = \left(\frac{N_\mathrm{fail,O}}{N_\mathrm{fail,A}}\right) = \left(\frac{\Delta T_\mathrm{A}}{\Delta T_\mathrm{O}}\right)^m \cdot \left(\frac{N_\mathrm{daily,O}}{N_\mathrm{daily,A}}\right)^{-n} \cdot e^{\frac{E_A}{k}\cdot\left(\frac{1}{T_{max,O}}-\frac{1}{T_{max,A}}\right)} \tag{2.19}$$

- m: Temperature range exponent
- n: Cycling frequency exponent

Given the fact that this model considers the effect of three parameters, it is only an estimation. Dwell time and ramp rate are critical factors in thermal cycling, so the Coffin-Manson model cannot distinguish between temperature cycling and thermal shock. [35]

ESS Model

Using Equations 2.16 and 2.17, it is possible to calculate the acceleration factor without any particular model. The screening strength formula is derived for the operational and accelerated case and both are rearranged to get the temperature cycling screening number. Thereof, the following equation is obtained assuming that the same screening strength is achieved:

$$AF_\mathrm{TC} = \left(\frac{N_\mathrm{O}}{N_A}\right) = \left(\frac{\Delta T_\mathrm{A}+0.6}{\Delta T_\mathrm{O}+0.6}\right)^{0.6} \cdot \left(\frac{\ln(e+d\vartheta_\mathrm{A})}{\ln(e+d\vartheta_\mathrm{O})}\right)^3 \tag{2.20}$$

This equation shows that the screening acceleration effect is related to the conditions of the thermal fatigued effect. Raising the temperate range and temperature changing rate improves the screening acceleration effect to achieve the same screening strength in fewer cycles. [36]

3 Experimental Procedure

In this chapter, the developed test strategy, as well as the test planning and setup, is presented. Subsequently, the procedure of accompanying tests is introduced and the screening and reliability testing strategy is described.

3.1 Test Planning and Setup

3.1.1 Methodology and Test Strategy

The following strategy to test and validate the produced boards is embedded into a greater methodology from development to installation which is shown in Figure 3.1. [23]

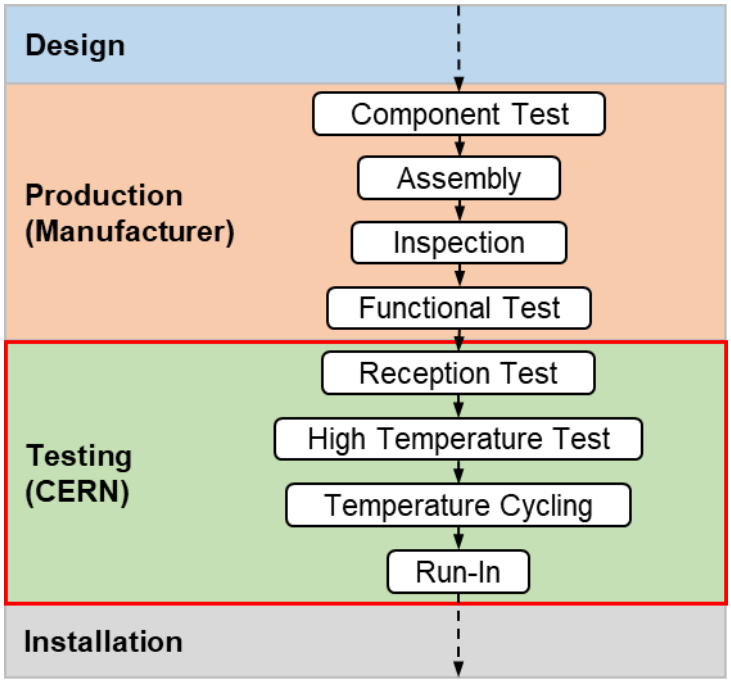


Figure 3.1: Adjusted methodology for the VFC-HD development according to [23]

After the design phase, a pre-series of ten boards was produced for testing purposes and to evaluate any production issues. Before assembly to the main board, the power supply modules are treated as separate components and are tested on a custom designed test bench. All boards must pass either a 3D x-ray or camera inspection before they undergo a functional test at the manufacturer on another test bench designed by the Beams Instrumentation group at CERN aiming to verify a total of 16 features of the board. All process steps are saved by the manufacturer to an electronic route card for each board. An overview of these prescribed process instructions can be found in Appendix B. After successful validation and production, the supplier delivers monthly batches of around 150 VFC-HD boards. A reception test and an additional high temperature test for the first batch are performed before the boards undergo a

screening process composed of temperature cycling and an additional Run-In at operational conditions to assess a minimum $MTTF$ of the system. Based on the presented results of the validation test, the screening strategy is defined to fit into the obtained design margins. Results of all the tests are fed back to the manufacturer to adapt the production process if necessary. Finally, the PCBs are directly installed in the different systems or are stored sealed under vacuum for spare usage or until installation is foreseen. [23]

3.1.2 Test Setup

To be able to perform the four different tests (highlighted in Figure 3.1), the necessary hardware, firmware and software is to be procured and developed. Figure 3.2 shows the hardware setup including the firmware implementation for one board under test. The VME crate can be equipped with up to 16 VFC-HD, a P0 pull-up, P0 jumper, and P0 loopback board and a Central Processing Unit (CPU) module to request the test results and to communicate with the external logging. The P0 connector is used for PCI Mezzanine Cards (PMC) which connect stacked PCBs [37]. For the firmware, a Built-In Test (BIT) was designed for the on-board FPGA to test several functionalities, which are illustrated in the block diagram and separately listed in Table 9.

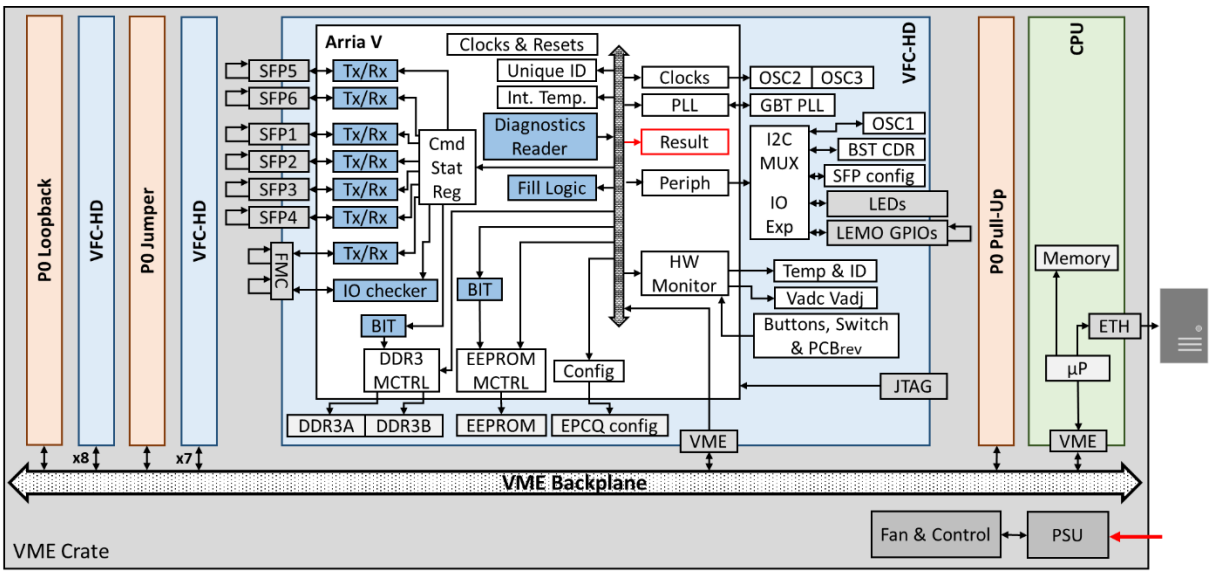


Figure 3.2: Hardware including firmware setup according to [23]

In total, 220 different parameters of the board and its interfaces are tested all in parallel by the FPGA without any need of software. The firmware sends commands and reads back the results which are saved into a register. The results register is then read by the CPU card. The test results data size is approximately 1 kB in a single block including the status, errors, counters and 32-bit Cyclic Redundancy Check (CRC).

Table 9: Summary of tested parameters by the firmware [38]

6 SFP at 2.5 GB·s^{-1} and BST CDR	Arria® V Unique ID and temperature
10 FMC HSSL at 2.5 GB·s^{-1}	Feedback clocks
FMC input clocks GPIO, JTAG and I2C	LEMO, LEDs, SFP status
3 onboard oscillators (+I2C and DAC)	Voltage ADC
Reference PLL (+I2C)	VME IRQ
DDR3, EEPROM, Config Flash	One wire sensor
Fill Logic (80 % LE, 60 % MACC, 75 % BRAM)	P0 connector (daisy chain, P0HW, TTL clocks, BLMIN)
VME BUS + GA	DIP switch, button, PCBrev, Testio

The CPU module requests the content of the register via the VME bus and communicates the data to an external database called Next CERN Accelerator Logging System (NXCALS). The design complies to a Front-End Software Architecture (FESA) framework which is an environment to design, develop, test and deploy real-time control software [39]. There is one FESA device per VFC-HD under test and Block Transfer (BLT) is used for the data transfer. Commands to start or stop the test and publication and a configuration mode are implemented for one device or the whole crate. The read-out of the temperature cycling is executed every second and every 30 seconds for the Run-In. An application was created in JavaFX providing a Graphical User Interface (GUI) with which it is possible to have an overview of the ongoing tests and occurring errors. The interface of this application is shown in Figure 3.3.

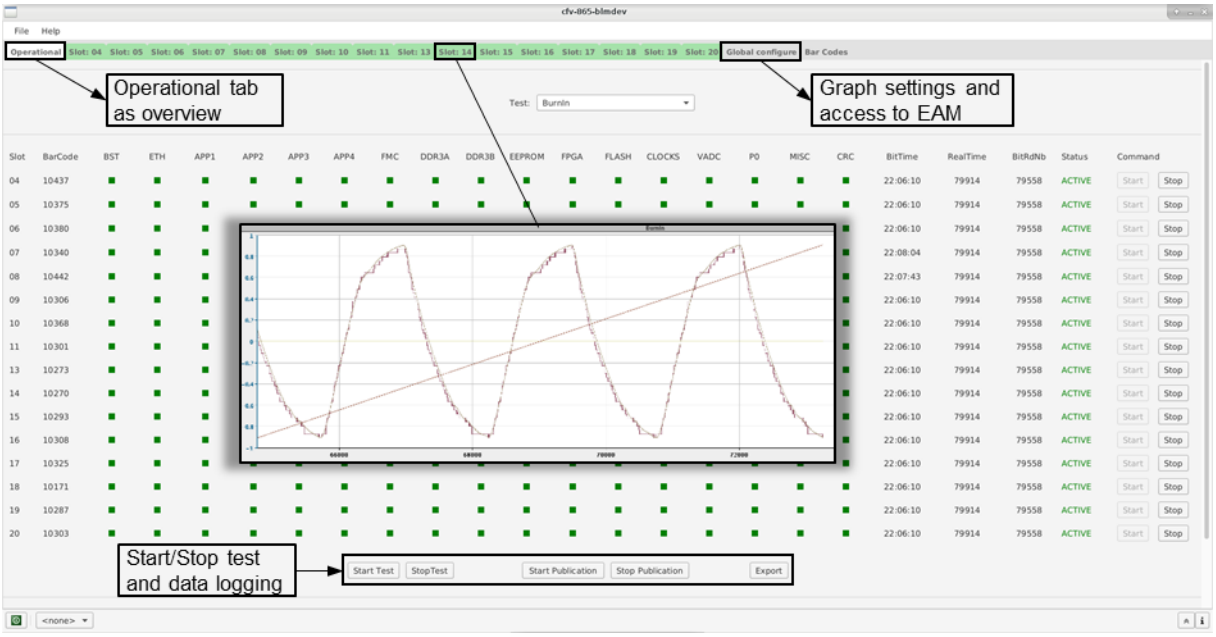


Figure 3.3: Test application GUI

NXCALS is a system created at CERN and in this case used to log the results of the screening tests. The used data rate for the temperature cycling is approximately 20 $KB \cdot s^{-1}$ and 5 $KB \cdot s^{-1}$ for the Run-In. The cluster-computing framework Spark™ is applied for queries and a corresponding Python script was written to extract the data which can be found in Appendix C.

Furthermore, the application is linked to Infor EAM (Enterprise Asset Management) which includes MTF (Manufacturing and Test Folder), an additional interface to track the tested boards during manufacturing and installation. There the results of the following four workflow steps are recorded:

- Functional Test
- Visual Inspection
- Temperature Cycling
- Run-In

By means of this tool, a status report of each board is created to later on be able to track which step was executed, which non-conformities occurred and in which current state the board is. It is a powerful tool to track and monitor the reliability in operation, to create repair statistics and furthermore to execute a lifetime data analysis.

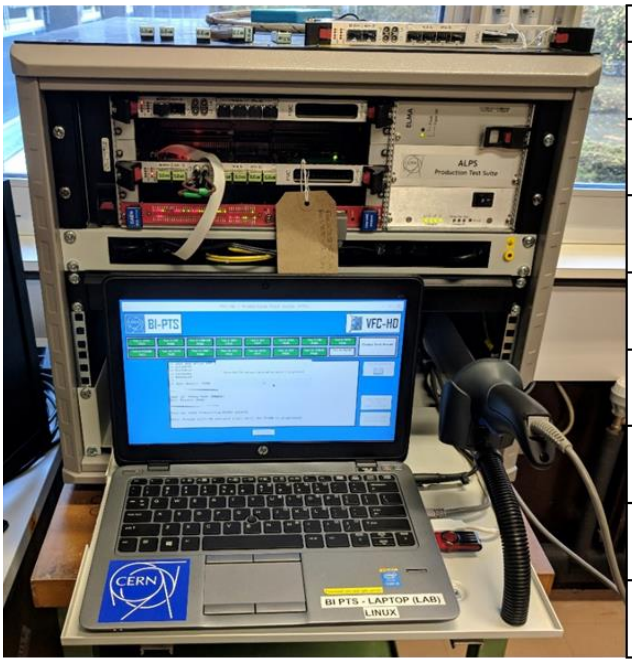
3.2 Accompanying Tests

In this chapter, the procedure and the hardware setup of the accompanying tests are described before the results are presented in chapter 4.1.

3.2.1 Functional Test

The functional test is performed on an at CERN designed test bench by the manufacturer. Therefore, equipped boards are tested for a variety of predefined parameters. The test bench and the 16 tested functionalities are shown in Figure 3.4.

If all functionalities pass the test, there is a global test column which confirms that the whole test passed. The results are provided by the manufacturer in form of a spreadsheet for every performed test. Hence, it is possible to see how often a board was tested until it passed and also which particular functionality caused a failure. An overview is created to determine how many boards in total failed the functional test, how often they are tested and what the main cause for failing the test is. These results are compared with the ones of the screening to examine if there is a correlation.



16 Functionalities	
FPGA Programming Cable	Light-Emitting Diodes
VME-WishBone Communication	Multi-Gigabit Transceivers
Beam Synchronous Timing Receiver	General Purpose Inputs/Outputs
VME Interrupts	VME P0 and P2 Connectors
Power Supplies	DDR3 RAMs
FPGA Mezzanine Card Connector	Clocks Scheme
Miscellaneous	VME System Reset
Debug Mode	FPGA Programming FLASH

Figure 3.4: Functional test bench and the 16 tested functionalities

3.2.2 Reception Test

After receiving the boards at CERN visual inspection tests are performed. For that purpose, a laboratory space was equipped with a high resolution digital microscope (TAGARNO FHD UNO, Horsens, Denmark) and a corresponding monitor. The laboratory setup is shown in Figure 3.5. At least 10 boards per batch undergo this inspection, in which the conformity to the IPC-A-610 [40] class 3 standard for high performance electronic products is verified. This step is put in place to assure that the boards are not damaged from shipping and that the manufacturer complies with the agreed quality. The results of each batch are fed back to the manufacturer to improve the production processes.

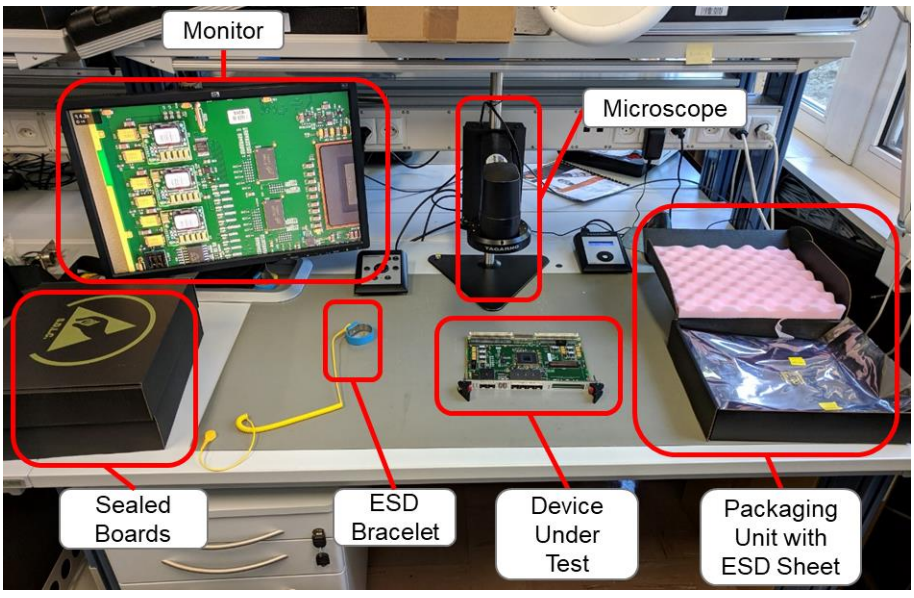


Figure 3.5: Laboratory setup for the visual inspection

3.2.3 High Temperature Test

As mentioned in chapter 2.2.3, the high temperature test is repeated with one board of the first batch to assure continuity in production quality. The test setup is the same as for the validation test (Figure 3.6) but all the slots of the VME crate are equipped. Additionally, the logging application is running to evaluate the different component failures. The temperature is increased from 50 °C to 80 °C in 10 °C steps to reach the critical range of the FPGA. Afterwards, the temperature steps are reduced to 5 °C. At this small interval, the dwell time for each temperature is 10 min. The set goal is to perform the test until the first damage occurs. The current consumption of the crate is measured. Furthermore, it is to be mentioned that for each temperature step the climatic chamber is opened to take an infrared picture of the board's surface to monitor the temperature development.

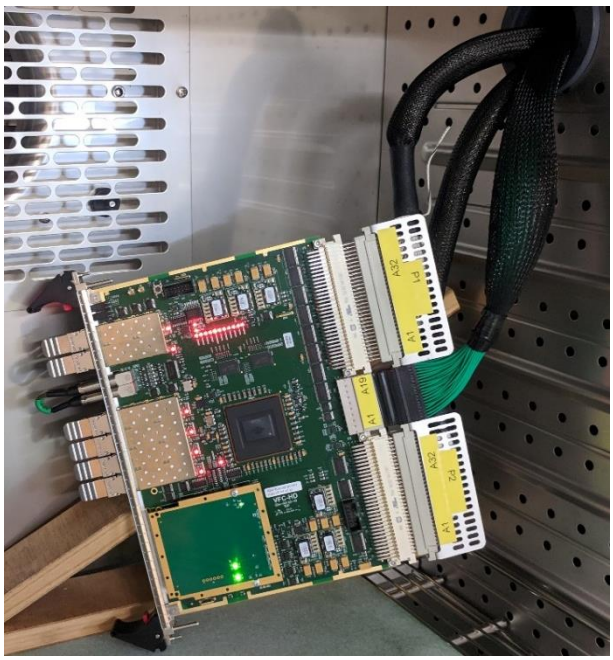


Figure 3.6: Equipped VFC-HD for high temperature test inside the climatic chamber

3.3 Screening and Reliability Testing

The test procedure for the screening and reliability testing is developed by combining the strategies presented in chapter 2.3.5 and under consideration of the validation test results.

3.3.1 Temperature Cycling

To perform the temperature cycling, a temperature and humidity controlled climatic chamber of the type MKF 240 from the company BINDER GmbH, Tuttlingen, Germany, was used. It is also able to fit a full VME crate including its power supply unit and the fan and control module (Figure 3.7). The power and communication lines exit from the sealed chamber. Additionally, a turning table is installed to prevent the introduction of damages while handling the crate and test devices. The accessories comprise two LEMO cables looped back between four connectors, six 3.5 dB electrical SFP loopbacks and one loopback FMC mezzanine.

In chapter 2.3.5, three different types of screening methods were introduced: high temperature Burn-In, thermal cycling and the combination of thermal and vibration cycling. The high temperature test is not applicable to the VFC-HD because the proposed temperatures are too high for most components. For example the maximum recommended operating temperature for the Arria® V GX FPGA is 85 °C [41]. As mentioned before, thermal or vibration cycling is assumed to be the best choice for an ESS. Failure mechanisms caused by vibration are not considered because the devices are not subjected to vibration stress during later operation. For that reason, thermal cycling is more suitable to the purpose and more expected failures can be detected due to a higher screening strength [32].

Figure 3.7: Fully equipped VME crate inside the climatic chamber

Since the type of test method is set, the parameters must be examined. The development of the test procedure for the temperature cycling is conducted by determining the three most important parameters separately: temperature range, thermal rate of change and number of cycles.

The temperature range is derived from the design limitations of the VFC-HD. Since the cycling is not performed on the component level but for the whole device, the maximal applicable temperature should be the lowest maximum recommended amongst the mounted components. For the VFC-HD, the ambient test temperature should not exceed 54 °C because of the Arria® V GX. This calculation was already proven by Equation 2.1 during the validation test. To prevent damages due to temperatures below the component specifications, the cycling will only go to a minimum environmental temperature of 5 °C. For example, the recommended minimum operational temperature for the DDR3, FPGA or OSC3 is 0 °C [41–43].

The thermal rate of change is set by the capabilities of the climatic chamber to an average of 5 °C·min^{-1} [44].

The previous parameters are below the values proposed in 2.3.5, which is why the number of cycles is adjusted to provide a sufficient high screening strength. According to the ESS Guide, 60 cycles should be applied for this procedure which equals 42 h. Due to internal constraints, the goal is to execute one temperature cycling per day. Hence, the number of cycles is set to 30 which corresponds to 21 h (Figure 3.8) of temperature cycling.

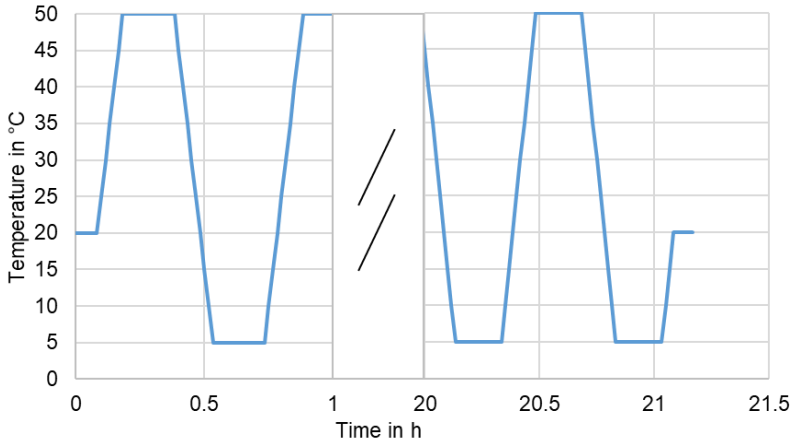


Figure 3.8: Climatic chamber program for the temperature cycling test

The dwell time is determined through tests and observations on how the temperature behaves at its maximum and minimum. This is shown in Figure 3.9 for an equipped VME crate inside the climatic chamber. Thermal stability of the board is reached if the slope is smaller than 2 °C·min^{-1} [32] which is reached after 12 min. The ambient temperature shows a stable plateau, while the board temperature just reaches this stability within the dwell time. The validation test (2.2.3) showed that humidity cycling is not possible. According to the datasheet (Appendix D) of this type of climatic chamber, humidity regulation below 10 °C is not possible. Hence, the humidity is programmed to the minimum possible. This does not avoid a relative humidity peak at low temperature (Figure 3.9) but tests showed no condensation. Moreover, the elevated humidity serves as additional stress to trigger failures due to moisture.

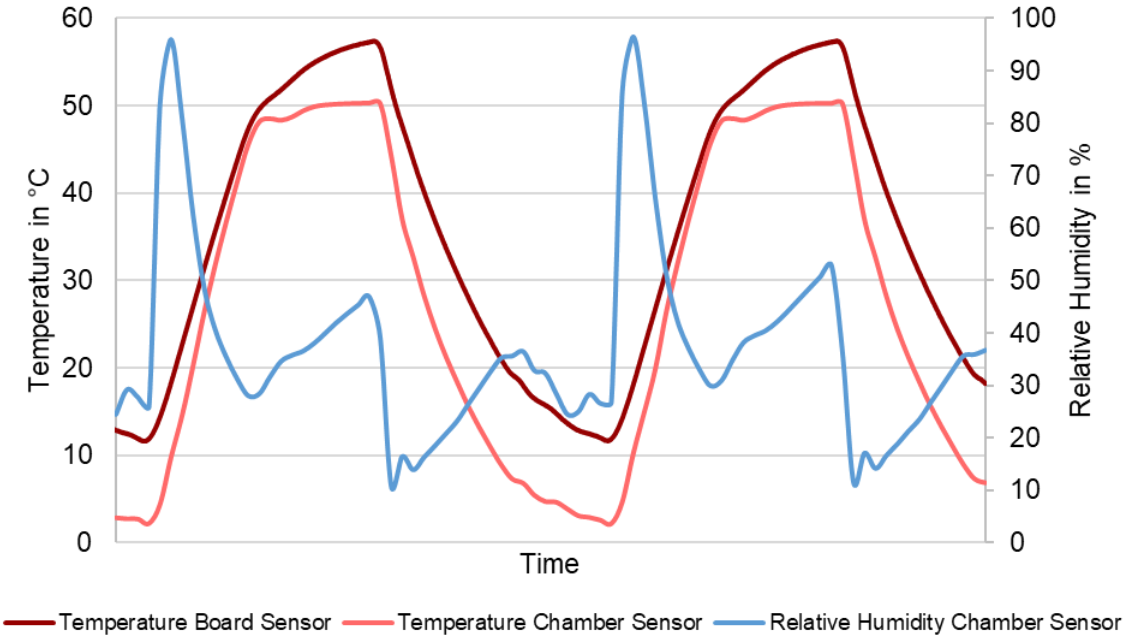


Figure 3.9: Two test cycles with temperature and humidity curves

For the in Table 10 determined test parameters and under use of Equation 2.16, a temperature cycling screening strength of 98.65 % is achieved which does not reach the proposed 100 %

but the additional Run-In ensures to achieve a sufficient high screening strength and compensates the described restrictions.

Table 10: Test parameters temperature cycling

Parameter	Value	Unit
Temperature range	5 to 50	°C
Thermal rate of change	5	$°C \cdot min^{-1}$
Number of cycles	30	-
Dwell time	12	min
Relative humidity	10	%

A full failure analysis of every occurring fault is presented in chapter 4.2.1. The testing strategy shall be reviewed and improvements shall be determined to increase the efficiency of screening. Because of the accelerated stress due to temperature cycling an acceleration factor can be used. But since the temperature controlled racks prevent temperature cycling in operation no compulsory model exists and hence, no acceleration factor is applied.

3.3.2 Run-In

For the Run-In, a small barrack was set up with the necessary arrangements to fit and power eight VME crates in two racks. Each crate is again equipped as shown in Figure 3.10. In contrast to the temperature cycling, it is not foreseen to use FMC, SFP or LEMO loopbacks and their test statuses in the software application are masked. Possible defects are to be tested before the systems get deployed.

After the temperature cycling, the boards are running at operational conditions to gain confidence for the screening success and to monitor the $MTTF$ progression for the accumulated test time. The boards run for four weeks and one crate for a longer time to monitor possible long term effects with a sample size of 16 VFC-HD.

The set $MTTF$ goal is derived from the current installed 350 BLETC. For 10 failures per year, an $MTTF$ of 306 000 h is calculated. Since the operational time of the system is not one year but approximately 5000 h, this number adjusts to 175 000 h. Furthermore, the commissioning of the boards begins before the LHC is running which should result in additional 80 000 device hours of data.

Figure 3.10: Eight equipped crates for the Run-In

4 Results and Discussion

In this chapter, the results of the previous described accompanying tests, temperature cycling and Run-In are presented successively. The ESS is analysed and the determined test procedure is reviewed critically.

4.1 Accompanying Tests

In the following, the results of the functional test, reception test and high temperature test are listed and explained.

4.1.1 Functional Test

Up to the time being, 634 boards underwent the functional test at the manufacturer. The test reports show that 445 boards passed the test without any error and 52 boards failed the test completely. This means that for 137 boards, the functional test was performed more than one time until it passed. In this context, it needs to be mentioned that the manufacturer performs this test with 5.0 dB noise SFP loopbacks and if those tests fail, boards which pass the test with 3.5 dB are also accepted. The respective numbers are illustrated in Figure 4.1. After testing the first batch, the manufacturer remarked that too many boards do fail the functional test. Thereupon, the test bench firmware was reviewed and indeed a bug was found and corrected resulting in fewer boards failing the test.

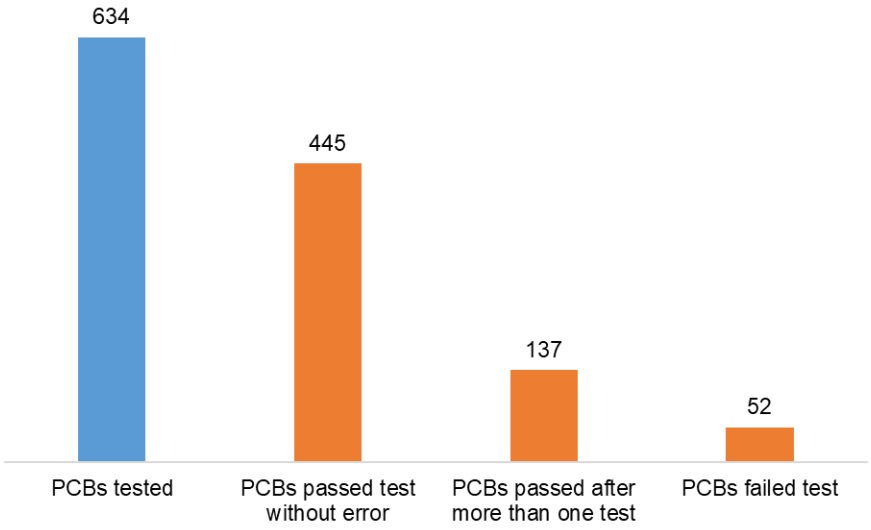


Figure 4.1: Results of the functional test performed at the manufacturer

In total, the functional test was performed 1062 times for the 634 boards. Subtracting the 445 boards passing at the first test run results in 617 test runs for 189 boards and an average of 3.26 times per board. The following Figure 4.2 shows the failed test functionalities sorted in order

of execution, bearing in mind that per test run several functionalities can fail. It shows that most failures occur for the transceivers (246) and the debug mode (429). It is important to mention that the Debug Mode test fails if the FPGA Programming FLASH test is not executed. This means that if one of the previous functionality tests fail, the manufacturer skips the last test because of time reasons, therefore the number of Debug Mode failures is high.

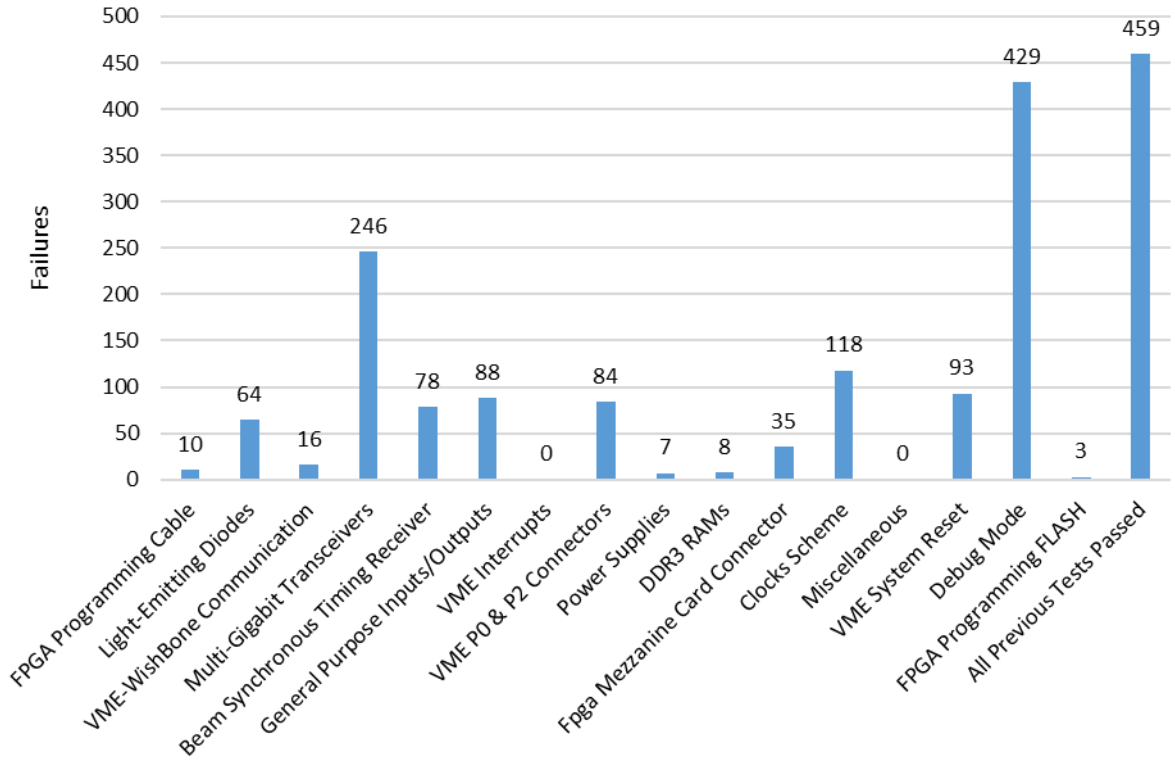


Figure 4.2: Breakdown of failed functionalities during the functional test of 634 boards

The test bench proofed that it is important and necessary to perform this kind of test. With 8.68 % failed boards, the rate is higher than expected. That is the reason why further investigations are carried out to find the failure cause. The test bench is not fully-developed and this test only functions as first filtering of faulty boards. The final approval is done by the followed tests at CERN.

4.1.2 Reception Test

The results of the reception test are shown in Table 11. The more detailed results are presented separately per batch, while the production quality change of each batch is evaluated and compared.

After inspecting 10 boards of the first batch, detecting conspicuous anomalies, it was necessary to inspect the whole batch in detail. Examples of five major anomalies found on several devices are shown in Figure 4.3:

- Material on the surface (a)
- Twisted components (b)
- Cleanliness issues (c)

- Damaged surface (d)
- Soldered pins out of tolerance (e)

Table 11: Overview results of the reception test

Batch Number	Number of Tested Boards	Number of Anomalies	Number of Failures	Main Anomalies
1	141	73	10	• Cleanliness • Solder pins out of tolerance
2	10	4	0	• Solder balls • Solder pins out of tolerance
3	10	4	0	• Repair works
4	10	3	0	• Repair works

The most frequent issue was the cleanliness which affected 54 boards. In total, 10 boards were sorted out for further investigations. For those boards, rework was done and one board has been used for the high temperature test. All detected issues were fed back to the manufacturer with the consequence that additional washing steps of the board were introduced.

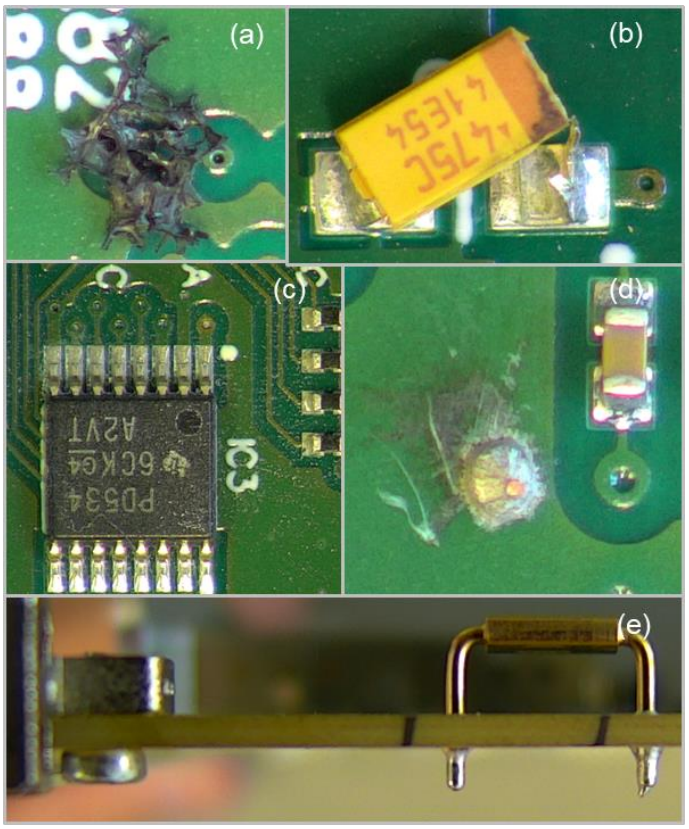


Figure 4.3: Collection of detected anomalies during the visual inspection of the first batch

In contrast to the first batch, it was only necessary to inspect 10 VFC-HD of the second batch. Especially, the cleanliness of the boards improved significantly. However, some solder pins

were still out of tolerance, several solder balls were found on the surface, and some components, as well as the solder mask, showed scratches.

The third batch showed similar results as the second batch. The main difference was, that the solder pins were cut to not exceed the front panel's height. On one board, a part of the copper layer below the solder mask was exposed.

The results of the reception test of the fourth batch are comparable to the third. There are still anomalies, but most of them are solvable through a short cleaning process. During the production of this batch, the manufacturer sent several concession requests whether CERN will accept minor defects like for example a resist delamination. Most were accepted because the functionality was not affected even though the IPC standard does not comply.

In general, it can be concluded that the reception test in the form of a visual inspection proved to be necessary and useful. The cleanliness problem was identified early and the production process was adjusted, also proving the significance of collaboration with the manufacturer.

4.1.3 High Temperature Test

The results of the high temperature test are illustrated in Figure 4.4. The FPGA temperature sensor saturated at 127 °C which corresponds to a climatic chamber temperature of 84 °C. This sensor is defined as an unsigned 8-bit integer for which 127 °C is the maximum value. The diagram shows that the FPGA and board sensor temperatures follow the programmed temperature curve of the climatic chamber but the discrepancy increases by time. The first failure occurred at an ambient temperature of 95 °C and the most failures at around 111 °C when also the PCB temperature sensor failed. This corresponds to 128 °C measured by the board sensor. Finally, the VME connection got lost (last cross) at 115 °C resulting in no communication to the on-board FPGA. The test was stopped shortly thereafter when all LEDs of the board turned out. Additionally, the VME crates power consumption was monitored, resulting in an increase of 5 A from 36 A up to 41 A. This increase in consumption at higher temperatures is probably related to the subthreshold power leakage of transistors [45].

The manually measured surface temperature of the FPGA shows that this test was performed above the maximum recommended operating temperature of 85 °C. Keeping in mind that the manufacturer specifies a maximum junction temperature of 125 °C [41]. Because of the FPGA sensor saturation, a linear extrapolation was created (Figure 4.5) between the present data of the FPGA and the temperatures of the climatic chamber. Thereby, only data points were used after 12 min of testing when the temperature curves stabilised. It has to be taken into account that this extrapolation is not accurate because the range is more than twice the time as data is given but further investigations showed that the ratio between the climatic chamber and FPGAs surface temperature is equal to the one with the FPGA sensor. It emerges that the ratio increases by time and for the highest chamber temperature of 115 °C, an FPGA junction temperature of 186.78 °C results.

After cooling down the board all functionalities of the board worked again and no hardware failure was detected. This again proves the robustness and design quality of the VFC-HD.

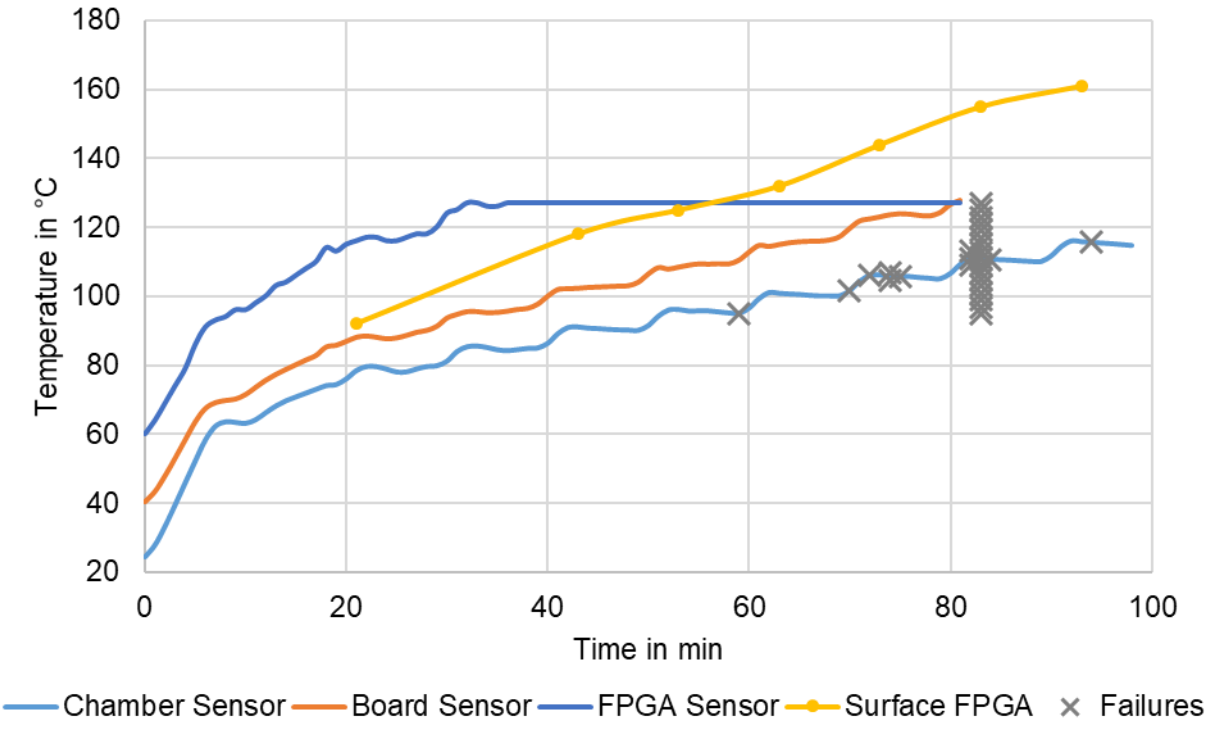


Figure 4.4: Different temperatures and error occurrence during the high temperature test

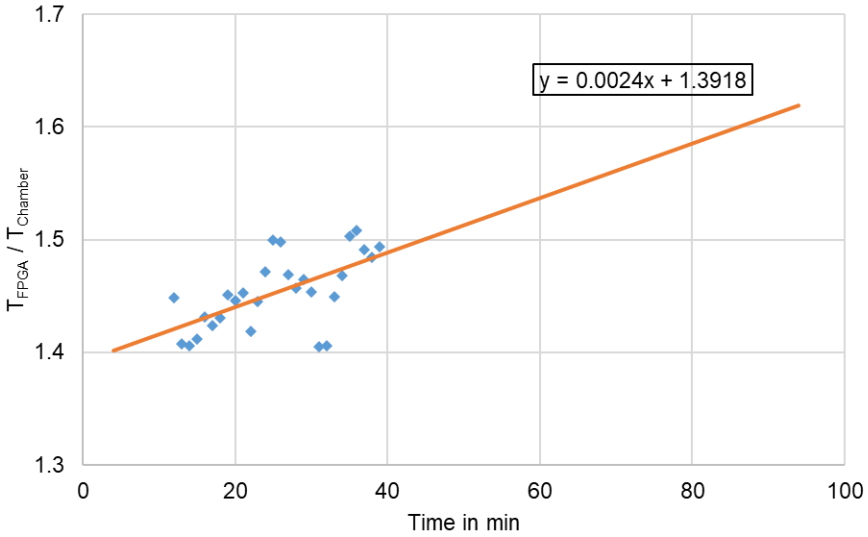


Figure 4.5: Linear extrapolation of FPGA and climatic chamber sensors temperature ratio

4.2 Screening and Reliability Testing

In this chapter, the results of the temperature cycling and the following Run-In are presented. A high confidence level of 95 % is chosen for determined reliability values which corresponds to high-reliability applications [30]. Therefore, the one sided, time-truncated equation of chapter 2.3.4 is used. Since the testing was not completed during this thesis, a current status is established. A schedule for the planned future test campaign is attached in Appendix E.

4.2.1 Temperature Cycling

At this time, 400 boards underwent the temperature cycling corresponding to one third of the whole production. The applied temperature stress triggered failures on 11 VFC-HD with three different causes of failure. A failure overview sorted by batch number is shown in Table 12. The main failure cause is the cleanliness of the board due to the production process which confirms the observations during the reception test. All failures traced back to cleanliness occurred for boards of the first batch and most affected is the pushbutton circuit with the component itself and additional passive components. The temperature cycling including the humidity peak most probably triggered short circuits in different circuits resulting in communication errors or loss of the connection to the board when for example the I^2C (Inter-Integrated Circuit) is affected. Thereupon, the manufacturer improved the production process and no cleanliness failure occurred during tests of the other batches. So far, there are 8 cleanliness, 1 manufacturing and 2 unknown failures. The manufacturing failure was detected due to a missing resistor before the actual cycling was started. The other two failures are still under investigation but the cause is unknown because the boards recovered after the ESS. Furthermore, the number of functional test runs per board are listed. All boards passed the test at the first time except two boards needed one additional run. This shows that there is no correlation between the results of the functional test and the thermal cycling.

Table 12: Failures overview during the temperature cycling

Batch	Number of Tested Boards	Temperature Board Sensor [°C]	Type of Failure	Cause of Failure	Number of Functional Test Runs
1	137	48.06	VME Bus + GA	Cleanliness	2
		19.25	Push Button	Cleanliness	1
		25.69	Push Button	Cleanliness	1
		23.81	VME Bus + GA	Cleanliness	1
		27.13	Push Button	Cleanliness	1
		55.00	Push Button	Cleanliness	1
		/	Push Button	Cleanliness	1
		/	PCBrev	Unknown	1
		/	Push Button	Cleanliness	1
2	150	24.25	PCBrev	Manufacturing	1
3	108	56.25	SFP ETH	Unknown	1
4	5	-	-	-	2

Figure 4.6 shows all occurred failures during a generic temperature cycling test. For this graph the data of the temperature board sensor is used. Most of the failures were triggered at low

temperatures and in the first third of the cycling process. This shows that the number of applied cycles are sufficient to screen for the discovered failure mechanisms. 3 failures are not listed because during one test run the data logging was not functional and therefore the time of failure is unknown.

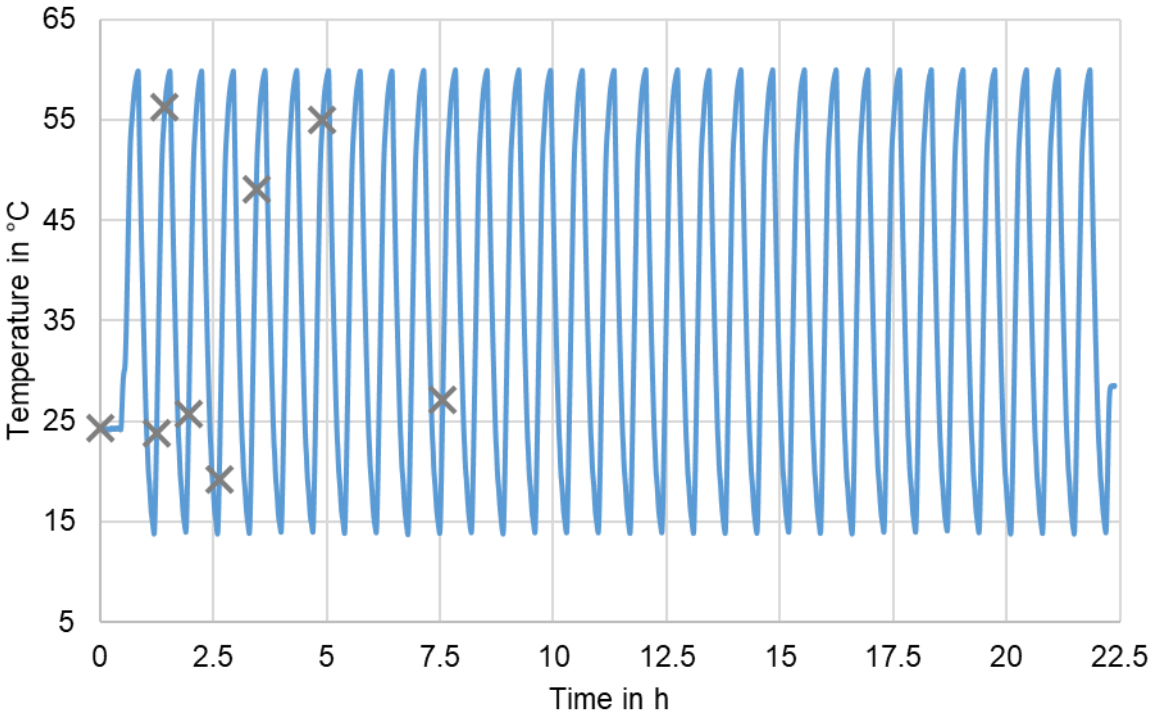


Figure 4.6: Failure occurrences during a generic temperature cycling test

For a better understanding of the failure causes, Figure 4.7 shows the occurrences merged into one cycle with relative humidity data of the climatic chamber and temperature data of the on-board sensor. The manufacturing failure is not listed because it occurred before and not during cycling. The figure shows that all failures happened on ascending temperature mostly during the relative humidity peak. The results indicate that the relative humidity peak, as well as possible delayed effects which need time to propagate, probably trigger most failures due to cleanliness. Several components like the push button are mounted manually resulting in a higher risk of introducing dirt. If this dirt contains salty or metallic elements it can get diluted by humidity during the test whereby the distilled water gets conductive resulting in a short circuit.

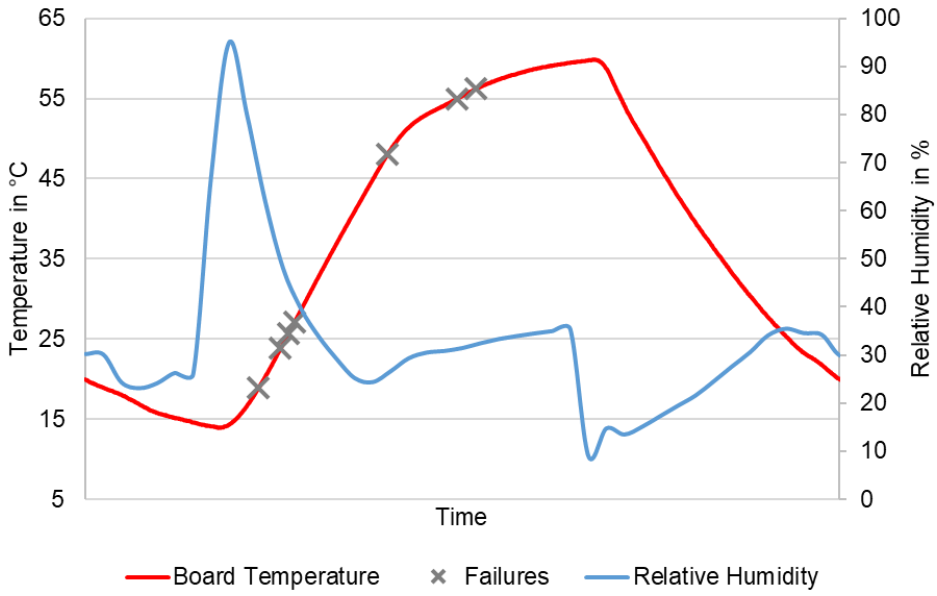


Figure 4.7: Failure occurrences listed during one standardised cycle

The accumulated test time for ESS is listed in Table 13. Furthermore, during some time slots the equipped crate was powered while no tests were performed. This additional time can be counted as testing time and is used for the Run-In determining the minimum $MTTF$ of the VFC-HD.

Table 13: Accumulated test time during temperature cycling

Parameter	**Value**	**Unit**
Test Time	8680	h
Additional Time	22 656	h
Total ESS Time	31 336	h
	3.58	a

Figure 4.8 shows the failure rate depending on failure censoring for the accumulated test time during the temperature cycling. The failures are sorted by time occurrence. The manufacturing failure and the three failures without time logging are set to $t = 0\ h$. Failure censoring is used because the cleanliness failures occurred in the first third of the cycling and this problem was solved after the first batch. The unknown failed boards recovered after the thermal cycling and the manufacturing failure was detected as soon as the board was powered. The figure shows the large gap between the two curves which results in a 6 times higher failure rate compared to the failure-censored assumption.

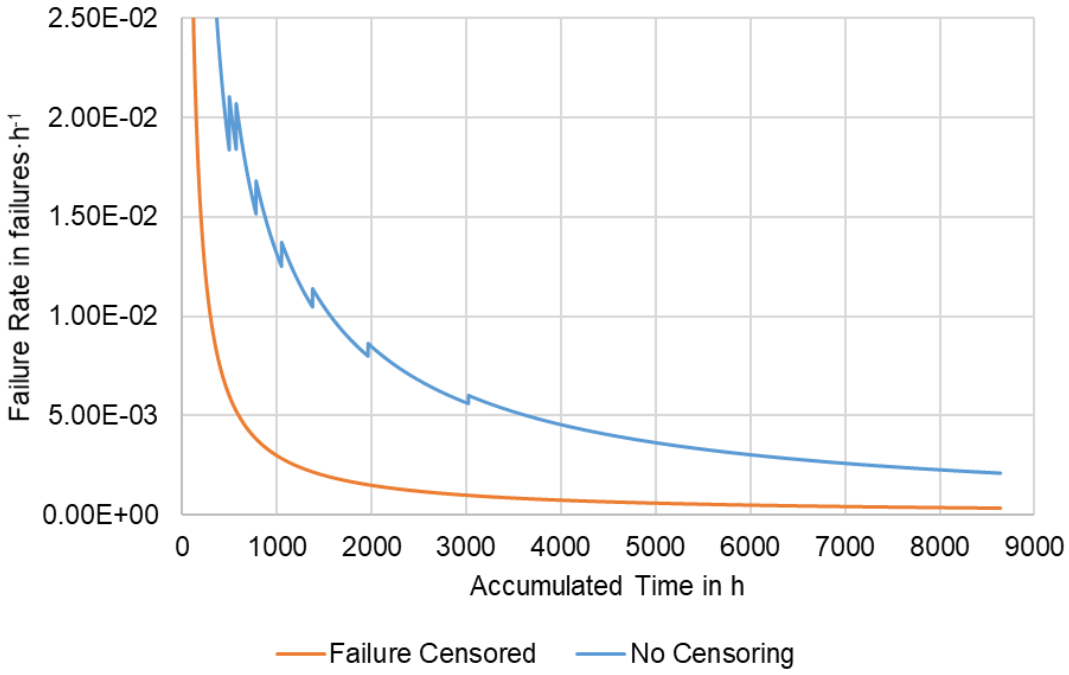


Figure 4.8: Current failure rate depending on failure censoring after temperature cycling

4.2.2 Run-In

For analysing the Run-In data, all occurred failures during the ESS are censored.

Until now, three complete Run-In phases were performed, each with approximately four weeks of testing time except the crate which is powered until the end of the test campaign. The test summary is listed in Table 14. No failure occurred until the time being. In total, 352 boards passed all performed tests. Additionally, an acceleration factor could be implemented because of higher ambient temperatures in the barrack than in field operation in temperature controlled racks (25 °C). The temperature in the barrack is estimated by the temperature sensor of the board (Appendix F) resulting in $t_{Barrack} \geq 30\,°C$. For these values and an activation energy of 0.7 [46] using Equation 2.18, an acceleration factor of 1.57 results. However, this accelerated stress is not considered resulting in a higher confidence of the current results.

Table 14: Overview of performed Run-In tests

Parameter	Run 1	Run 2	Run 3	Total
Number of Days	29	28	28	85
Number of VFC-HD	128	112	112	352
Failures	0	0	0	0
Device Hours	87 552	87 040	86 165	260 757

The current failure rate over the accumulated test time which combines censored ESS and Run-In is illustrated in Figure 4.9. The reached low failure rate $\lambda = 1.11 \cdot 10^{-5}\ \frac{failures}{hour}$ indicates already the success of the test because by testing one third of the whole production already the half of the required minimum MTTF is reached.

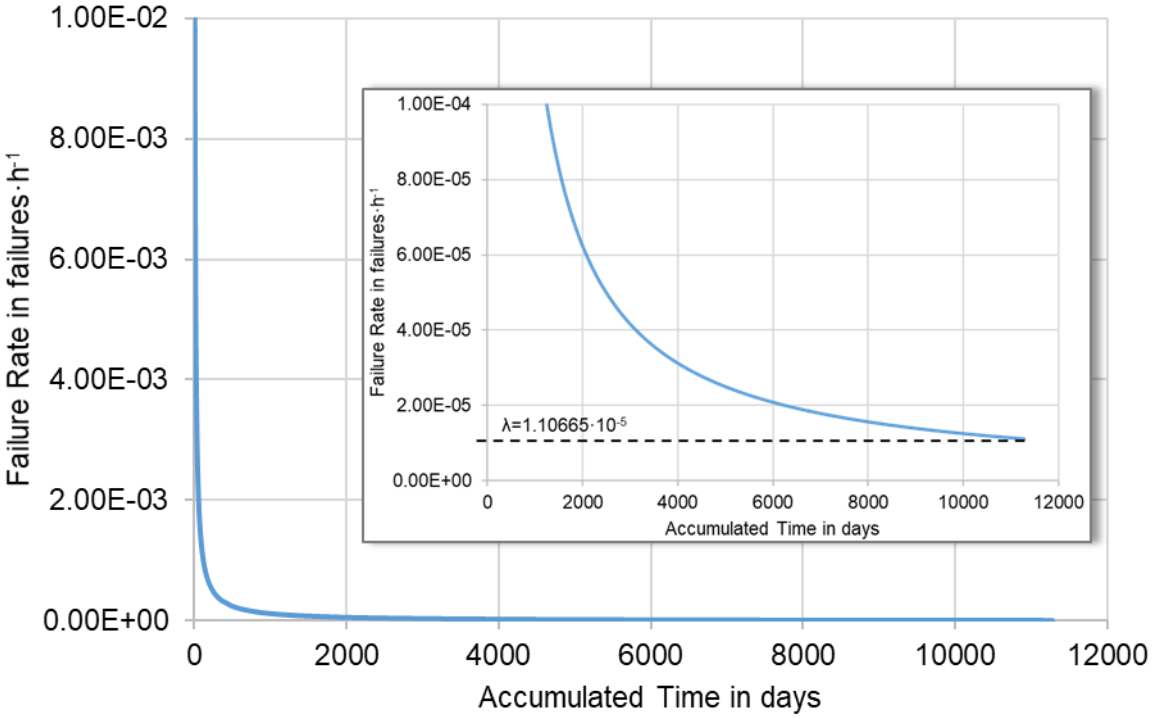


Figure 4.9: Current failure rate with failure censoring for the combined screening

The current $MTTF$ is 90 363 h (10.32 years) without acceleration factor and at a high confidence level. The test process will be carried on until the last batch is received and all boards are tested. A simulation of how the bathtub curve would look like affected by possible future failures is illustrated in Appendix G.

4.3 Review of the Test Strategy

To review the test strategy, the main parameters of the ESS are regarded. First, the temperature range was set referring to the climatic chamber's temperature contrary to the standards which recommend to refer to a thermocouple on the PCB. After taking a closer look at the climatic chambers compared to the board sensors temperatures (Figure 4.10) it is possible to reduce the minimum temperature by 5 °C to 10 °C. The maximum FPGA temperature recorded was 80 °C hence, the range could be extended from 0 °C up to 55 °C climatic chamber temperature which corresponds to a gain of 10 °C in range. The observation of the chronological failure occurrence showed that all failures were triggered in the first third of the temperature cycling indicating a sufficient number of cycles. The thermal rate of change is limited by the climatic chamber's performance and the dwell time was adequately high to reach thermal stability.

Applying the higher temperature range results in a higher screening strength of 99.22 %. It can also be used to perform fewer cycles to save time but with the lack of screening strength. The second part of the screening strategy, the Run-In, served its purpose and no improvements are considered. Furthermore, the strategy could have been adjusted during the testing period which was not implemented to maintain the same conditions for each board.

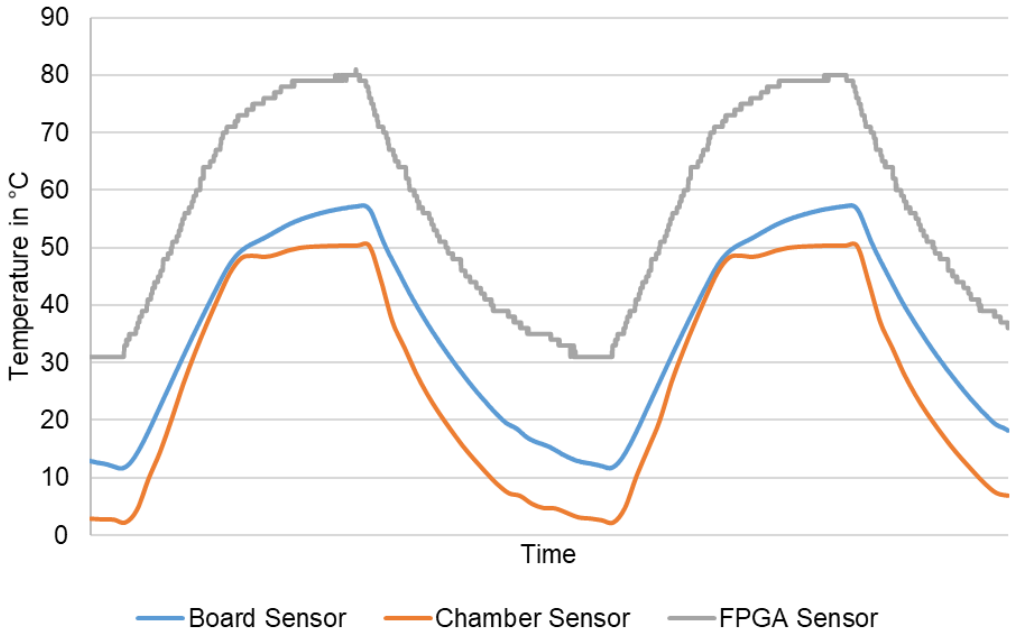


Figure 4.10: Two cycles of board, climatic chamber and FPGA sensor temperatures

5 Conclusion and Outlook

The thesis results show the importance of a screening process for electronics prior to their installation. It can be noted that the screening after production was necessary even though no hardware failure occurred.

The accompanying tests demonstrated their usefulness. The functional test bench already filtered 8 % of at production non-functional boards emphasising the difficulties and complexity of the VFC-HD. The visual inspection after reception at CERN turned out to be necessary. Especially for the first production batch, cleanliness issues and other problems were discovered. After improving the washing process of the boards, these problems were solved for upcoming batches. The high temperature test as additional validation of the first production batch quality showed that it is possible to power the board above the design specifications and proved the robustness and high design quality of the VFC-HD.

The screening strategy consisted of temperature cycling and powering the boards at operational conditions turned out to be sufficient. The temperature cycling uncovered a quality issue of mainly the first production batch. 11 failures were triggered but no hardware failure like a damaged solder joint was precipitated by the testing. The most frequent failure cause is due to cleanliness which was most likely triggered by humidity. The followed Run-In determined a minimum $MTTF$ of 90 000 h which is below the set goal of 175 000 h but not even the half of the whole production is tested and a high confidence level of 95 % is chosen.

This test campaign will be carried on until the whole VFC-HD production is fully tested. Therefore, a temperature cycling with other parameters could be executed to determine if there is a difference to current results. The outcome of the performed strategy compared to Burn-In or a method combining temperature and vibration cycling can be helpful for a better understanding of how powerful the screening methods are.

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7 Appendix

A Appendix A

Figure 7.1 shows the architecture of the VFC-HD. Only the NIOS Debug is not implemented.

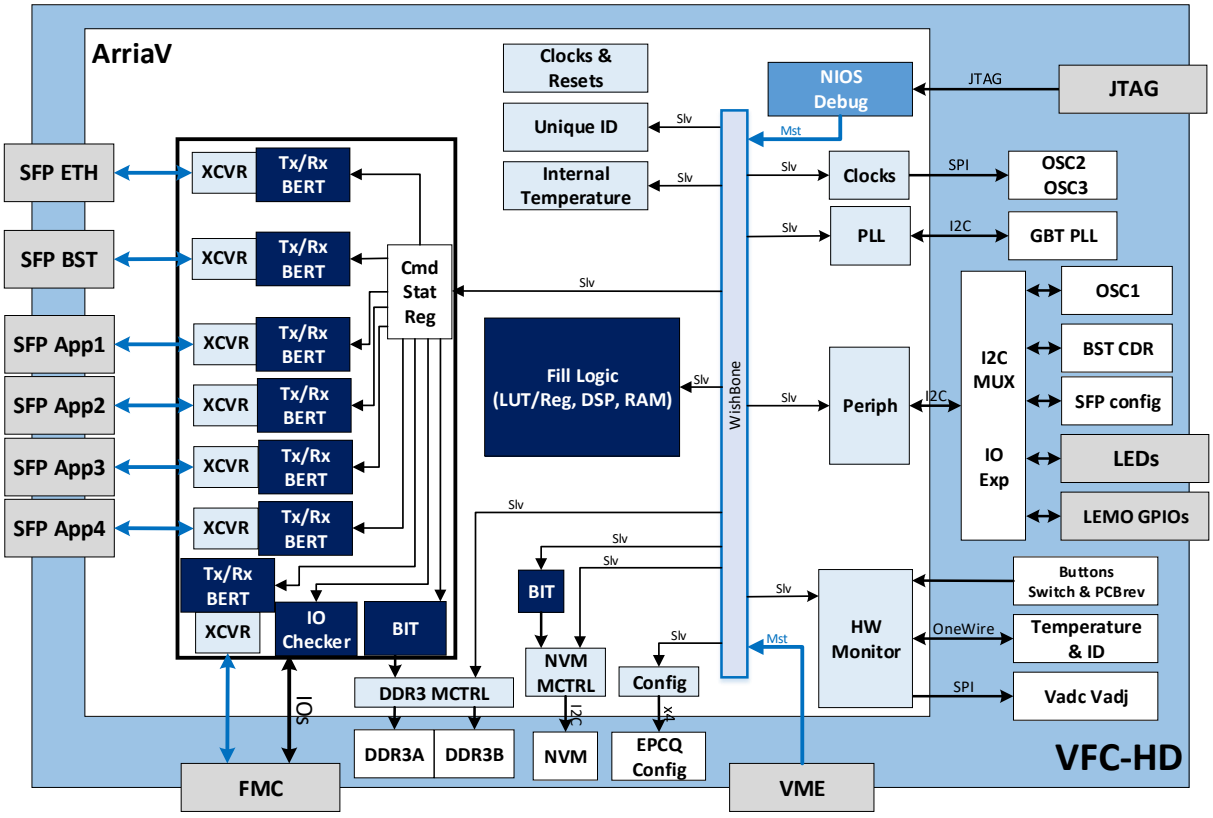


Figure 7.1: Architecture of the VFC-HD [47]

B Appendix B

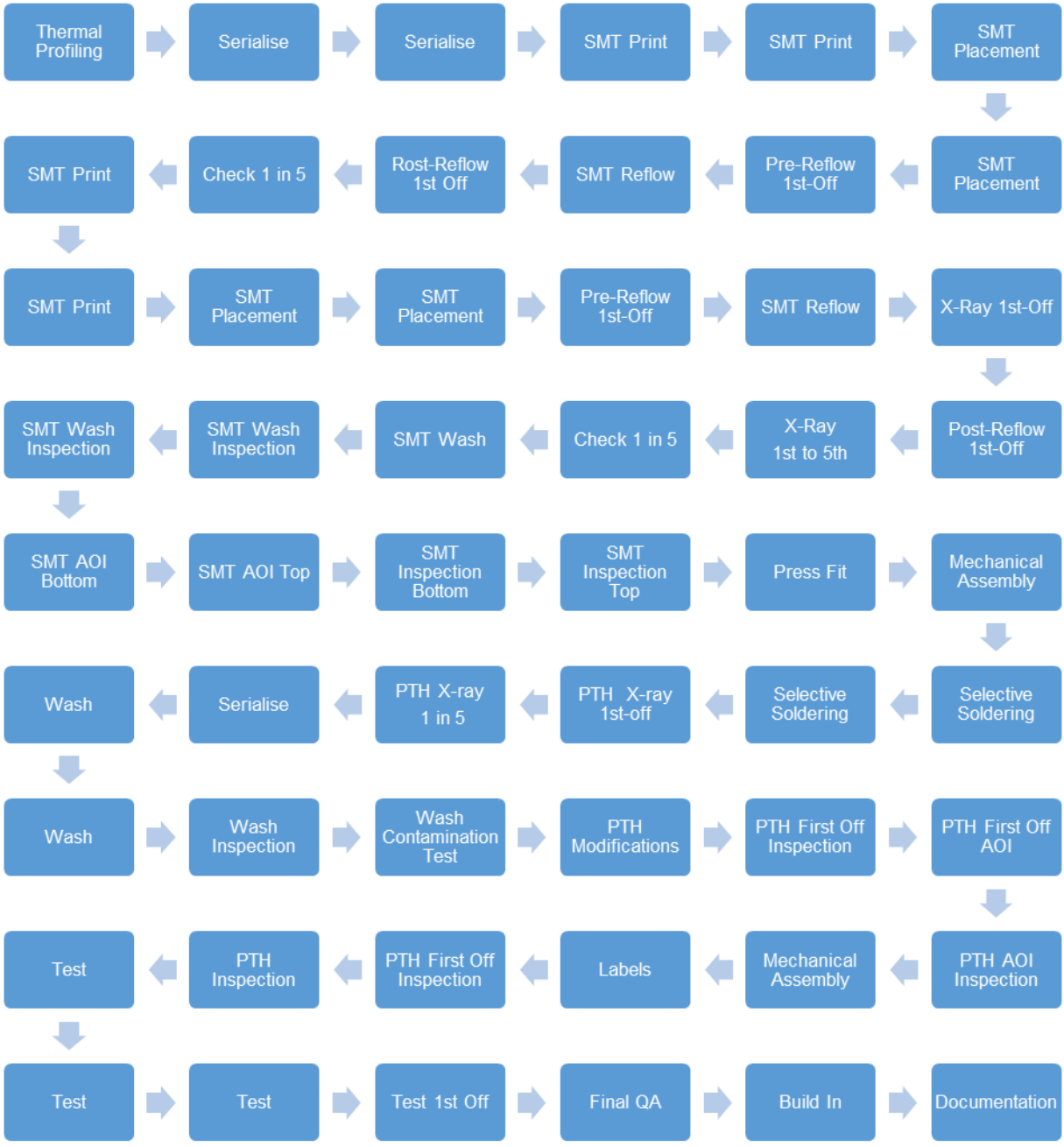


Figure 7.2: Process instructions VFC-HD

C Appendix C

Table 15: Python script to extract data from NXCALS

```
1  import pandas
2  import pandas as pd
3  from cern.nxcals.pyquery.builders import *
4  df = DevicePropertyQuery.builder(spark).system("CMW").startTime("year-
   month-day hour:min:sec.000").endTime("year-month-day
   hour:min:sec.000").entity().parameter("VFC_HD_Validation_SlotXX/Acquisi
   tionAppBitMsg").buildDataset()
5  from pyspark.sql import DataFrame
6  df3 = df2.select('acqStamp', 'parameter1', 'parameter2',
   …'parameterX').orderBy('acqStamp')
7  df2 = DataFrame(df, spark)
8  df3.toPandas().to_csv('filename.csv')
```

D Appendix D

Data Sheet Model MKF 240

Model MKF 240 | Dynamic climate chambers for rapid temperature changes with humidity control

A BINDER MKF series environmental simulation chamber is ideally suited for any cold and heat testing based on current temperature and climate testing methods according to DIN and IEC standards. The comprehensive standard equipment for this environmental simulation chamber ensures ease of operation.

BENEFITS

- Homogeneous climate conditions thanks to APT.line™ technology
- Automatic water and wastewater management
- Pressure humidification with fast response times
- Comprehensive programming and data acquisition
- Large heated viewing window

Model 240

Model 240

MAIN FEATURES

- Temperature range: -40 °C to 180 °C
- Humidity range: 10 % to 98 % RH
- Integrated water-storage tank, 20 liters
- 4 zero-voltage relay contacts
- APT.line™ preheating chamber technology
- Programmable condensation protection for test material
- Heated viewing window with LED interior lighting
- Humidity regulation with capacitative humidity sensor and vapor humidification
- BINDER Multi Management Software APT-COM™ 4 Basic Edition
- Troubleshooting system with visual and audible alarms
- Intuitive touchscreen controller with time-segment and real-time programming
- Internal data logger, measured values can be read out in open format via USB
- Access port with silicone plug: 50 mm, left
- Class 2 independent adjustable temperature safety device (DIN 12880) with visual alarm
- 4 castors, two with brakes
- Computer interface: Ethernet
- 230 V power socket on the right-side control panel
- Adjustable ramp function
- Integrated chart recorder
- Real-time clock
- Door heating
- Alarm notification in the event of insufficient water in fresh water tank
- 1 stainless steel rack
- Complete safety connection kit for water supply and drainage, up to 1 m height
- Inner chamber made of stainless steel
- CFC-free refrigerant R-404A
- Cooling with compressor cooling unit

Data Sheet Model MKF 240

BINDER

ORDERING INFORMATION

Interior volume [L]	Voltage	Option model	Version	Art.-No.
Model MKF 240				
228	400 V 3~ ph 50 Hz	Standard	MKF240-400V	9020-0208
	480 V 3~ ph 60 Hz	with voltage and frequency converter	MKF240-480V-C	9020-0358

TECHNICAL DATA

Description	MKF240-400V[1]	MKF240-480V-C[1]
Article Number	9020-0208	9020-0358
Performance Data Temperature		
Temperature range [°C]	-40…180	-40…180
Temperature variation depending on setpoint [± K]	0.1…1.5	0.1…1.5
Temperature fluctuation depending on setpoint [± K]	0.1…0.5	0.1…0.5
Average heating-up rate according to IEC 60068-3-5 [K/min]	5	5
Cooling down time from 180 °C to -40 °C [min]	110	110
Average cooling down time according to IEC 60068-3-5 [K/min]	5	5
Max. heat compensation at 25 °C [W]	2800	2800
Performance Data Climate		
Temperature range [°C]	10…95	10…95
Temperature fluctuation depending on setpoint [± K]	0.1…1.3	0.1…1.3
Humidity range [% RH]	10…98	10…98
Humidity fluctuation depending on setpoint	≤2,5 ± % RH	≤2,5 ± % RH
Dew point temperature range [°C]	5…94	5…94
Electrical data		
Rated Voltage [V]	400	480
Power frequency [Hz]	50	60
Nominal power [kW]	6.8	6.8
Unit fuse [A]	16	16
Phase (Nominal voltage)	3~	3~
Outer dimensions		
Width net [mm]	1115	1115
Height net [mm]	1715	1715
Depth net [mm]	925	925
Wall clearance back [mm]	300	300
Wall clearance sidewise [mm]	200	200
Viewing window width [mm]	508	508
Viewing window height [mm]	300	300
Doors		
Unit doors	1	1
Internal Dimensions		
Width [mm]	735	735
Height [mm]	700	700
Depth [mm]	443	443
Measures		
Interior volume [L]	228	228
Net weight of the unit (empty) [kg]	360	360
permitted load [kg]	70	70
Load per rack [kg]	30	30

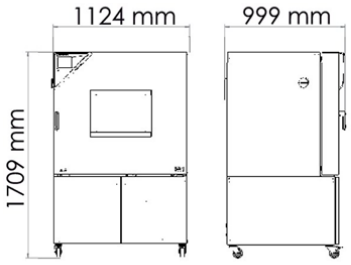
1 All technical data is specified for unloaded units with standard equipment at an ambient temperature of +22 °C ±3 °C and a power supply voltage fluctuation of ±10 %. The temperature data is determined in accordance to BINDER factory standard following DIN 12880, observing the recommended wall clearances of 10 % of the height, width, and depth of the inner chamber. Technical data refers to 100 % fan speed. All indications are average values, typical for units produced in series. We reserve the right to change technical specifications at any time.

Data Sheet Model MKF 240

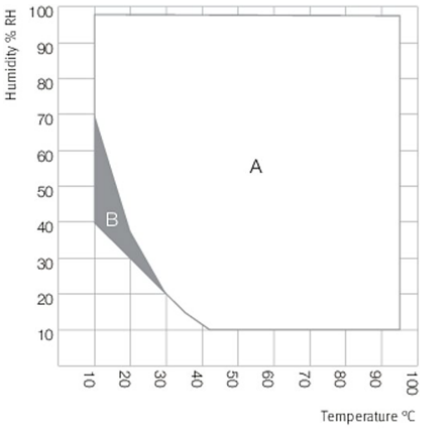
Description	MKF240-400V[1]	MKF240-480V-C[1]
Article Number	9020-0208	9020-0358
Environment-specific data		
Sound-pressure level [dB(A)]	65	67
Fixtures		
Number of shelves (std./max.)	1/6	1/6

1 All technical data is specified for unloaded units with standard equipment at an ambient temperature of +22 °C ±3 °C and a power supply voltage fluctuation of ±10 %. The temperature data is determined in accordance to BINDER factory standard following DIN 12880, observing the recommended wall clearances of 10 % of the height, width, and depth of the inner chamber. Technical data refers to 100 % fan speed. All indications are average values, typical for units produced in series. We reserve the right to change technical specifications at any time.

DIMENSIONS incl. fittings and connections [mm]

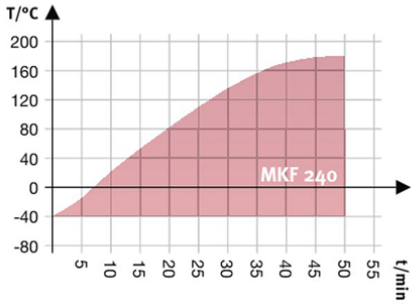


CHARTS



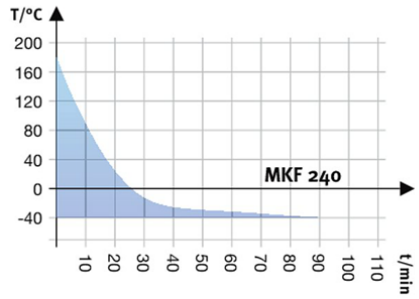
A: Standard Climate range
B: Time-limited operation (max. 24 hours)

Climate chart

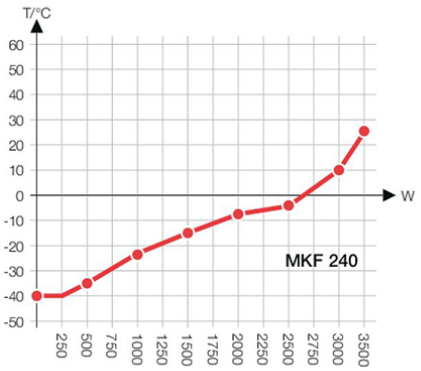


Heating up rate

Data Sheet Model MKF 240



Cooling down rate



Heat compensation chart

OPTIONS AND ACCESSORIES

Designation	Description	*	Art.-No.
Access port	notch-type access port in door, 100 x 35 mm	–	8012-1856
Access port with silicone plug	left		
	30 mm	01	8012-1323
	50 mm	01	8012-1329
	80 mm	01	8012-1335
	100 mm	01, 11	8012-1543
	125 mm	01, 11	8012-1352
	right		
	30 mm	01	8012-1320
	50 mm	01	8012-1326
	80 mm	01	8012-1332
	100 mm	01, 11	8012-1540
	125 mm	01, 11	8012-1349
	top		
	80 mm	01	8012-1537
	100 mm	01, 11	8012-1531
	125 mm	01, 11	8012-1534
Analog output 4-20 mA	for temperature and humidity values (output not adjustable)	–	8012-1085
APT-COM™ 4 GLP-Edition	for working under GLP-compliant conditions. Measured values are documented in a tamper-proof way in line with the requirements of FDA Regulation 21 CFR 11.		
	version 4, GLP edition	19	9053-0042
APT-COM™ 4 PROFESSIONAL-Edition	convenient unit and user management built on the BASIC edition. Suitable for networking up to 100 units.		
	version 4, PROFESSIONAL edition	19	9053-0040
BINDER PURE AQUA SERVICE	system for preparation or complete desalination of tap water, containing single-use cartridge, hoses and measuring device	–	8012-0759
BINDER PURE AQUA SERVICE, accessories	Single-use, replacement cartridge for BINDER PURE AQUA System	–	6011-0165
Calibration certificate, expanded	for temperature and humidity; for extending the measurement in center of chamber to include another test value	–	8012-1194
Calibration certificate, temperature	temperature measurement incl. certificate and 27 measuring points at specified temperature	–	8012-1609
	temperature measurement incl. certificate, 15- 18 measuring points at specified temperature	–	8012-1589
	temperature measurement incl. certificate, 9 measuring points at specified temperature		8012-1568
Calibration certificate, temperature and humidity	Measurement in center of chamber at 25 °C / 60% RH or at specified test values	–	8012-1188
	temperature (according to DIN12880) and humidity measurement incl. certificate, 27 temperature measuring points and 1 humidity measuring point, at 25 °C / 60 % RH or at specified values	–	8012-1615

* Notes › See last page

E Appendix E

	Week 1						
	29/10/2018	30/10/2018	31/10/2018	01/11/2018	02/11/2018	03/11/2018	04/11/2018
Deliveries	141						
ESS				Lot 1			
				DUT 1 - 16			
Run-In							
	Week 2						
	05/11/2018	06/11/2018	07/11/2018	08/11/2018	09/11/2018	10/11/2018	11/11/2018
Deliveries				131			
ESS	Lot 2			Lot 3	Lot 4		
	DUT 17 - 32			DUT 33 - 48	DUT 49 - 64		
Run-In							
	Week 3						
	12/11/2018	13/11/2018	14/11/2018	15/11/2018	16/11/2018	17/11/2018	18/11/2018
Deliveries							
ESS	Lot 5	Lot 6	Lot 7	Lot 8	Lot 9		
	DUT 65 - 80	DUT 81 - 96	DUT 97 - 112	DUT 113 - 128	DUT 129 - 144		
Run-In							

	Week 4						
	19/11/2018	20/11/2018	21/11/2018	22/11/2018	23/11/2018	24/11/2018	25/11/2018
Deliveries							
ESS	Lot 10 DUT 145 - 150	Lot 11 DUT 151 - 166	Lot 12 DUT 167 - 182	Lot 13 DUT 183 - 198	Lot 14 DUT 199 - 214		
Run-In				Lot 1			
				Lot 2			
				Lot 3			
				Lot 4			
				Lot 5			
				Lot 6			
				Lot 7			
				Lot 8			
	Week 5						
	26/11/2018	27/11/2018	28/11/2018	29/11/2018	30/11/2018	01/12/2018	02/12/2018
Deliveries							
ESS					Lot 15 DUT 215 - 230		
Run-In	Lot 1						
	Lot 2						
	Lot 3						
	Lot 4						
	Lot 5						
	Lot 6						
	Lot 7						
	Lot 8						
	Week 6						
	03/12/2018	04/12/2018	05/12/2018	06/12/2018	07/12/2018	08/12/2018	09/12/2018
Deliveries			150				
ESS							
Run-In	Lot 1						
	Lot 2						
	Lot 3						
	Lot 4						
	Lot 5						
	Lot 6						
	Lot 7						
	Lot 8						
	Week 7						
	10/12/2018	11/12/2018	12/12/2018	13/12/2018	14/12/2018	15/12/2018	16/12/2018
Deliveries							
ESS		Lot 16 DUT 231 - 246	Lot 17 DUT 247 - 262				
Run-In	Lot 1						
	Lot 2						
	Lot 3						
	Lot 4						
	Lot 5						
	Lot 6						
	Lot 7						
	Lot 8						

	Week 8						
	17/12/2018	18/12/2018	19/12/2018	20/12/2018	21/12/2018	22/12/2018	23/12/2018
Deliveries							
ESS							
Run-In	Lot 1				Lot 9		
	Lot 2				Lot 10		
	Lot 3				Lot 11		
	Lot 4				Lot 12		
	Lot 5				Lot 13		
	Lot 6				Lot 14		
	Lot 7				Lot 15		
	Lot 8						
	Week 9						
	24/12/2018	25/12/2018	26/12/2018	27/12/2018	28/12/2018	29/12/2018	30/12/2018
Deliveries							
ESS							
Run-In	Lot 9						
	Lot 10						
	Lot 11						
	Lot 12						
	Lot 13						
	Lot 14						
	Lot 15						
	Lot 8						
	Week 10						
	31/12/2018	01/01/2019	02/01/2019	03/01/2019	04/01/2019	05/01/2019	06/01/2019
Deliveries							
ESS							
Run-In	Lot 9						
	Lot 10						
	Lot 11						
	Lot 12						
	Lot 13						
	Lot 14						
	Lot 15						
	Lot 8						
	Week 11						
	07/01/2019	08/01/2019	09/01/2019	10/01/2019	11/01/2019	12/01/2019	13/01/2019
Deliveries							
ESS		Lot 18	Lot 19	Lot 20	Lot 21		
		DUT 263 - 278	DUT 279 - 294	DUT 295 - 300	DUT 301 - 316		
Run-In	Lot 9						
	Lot 10						
	Lot 11						
	Lot 12						
	Lot 13						
	Lot 14						
	Lot 15						
	Lot 8						

	Week 12						
	14/01/2019	15/01/2019	16/01/2019	17/01/2019	18/01/2019	19/01/2019	20/01/2019
Deliveries							
ESS	Lot 22	Lot 23	Lot 24		Lot 25		
	DUT 317 - 332	DUT 333 - 348	DUT 349 - 364		DUT 365 - 380		
Run-In	Lot 9				Lot 16		
	Lot 10				Lot 17		
	Lot 11				Lot 18		
	Lot 12				Lot 19		
	Lot 13				Lot 20		
	Lot 14				Lot 21		
	Lot 15				Lot 22		
	Lot 8						
	Week 13						
	21/01/2019	22/01/2019	23/01/2019	24/01/2019	25/01/2019	26/01/2019	27/01/2019
Deliveries					150		
ESS							
Run-In	Lot 16						
	Lot 17						
	Lot 18						
	Lot 19						
	Lot 20						
	Lot 21						
	Lot 22						
	Lot 8						
	Week 14						
	28/01/2019	29/01/2019	30/01/2019	31/01/2019	01/02/2019	02/02/2019	03/02/2019
Deliveries							
ESS							
Run-In	Lot 16						
	Lot 17						
	Lot 18						
	Lot 19						
	Lot 20						
	Lot 21						
	Lot 22						
	Lot 8						
	Week 15						
	04/02/2019	05/02/2019	06/02/2019	07/02/2019	08/02/2019	09/02/2019	10/02/2019
Deliveries							
ESS							
Run-In	Lot 16						
	Lot 17						
	Lot 18						
	Lot 19						
	Lot 20						
	Lot 21						
	Lot 22						
	Lot 8						

	Week 16						
	11/02/2019	12/02/2019	13/02/2019	14/02/2019	15/02/2019	16/02/2019	17/02/2019
Deliveries				150			
ESS							
Run-In	Lot 16						
	Lot 17						
	Lot 18						
	Lot 19						
	Lot 20						
	Lot 21						
	Lot 22						
	Lot 8						

F Appendix F

Figure 7.3 shows the board and FPGA sensor temperatures for a four week Run-In. Assuming a 10 °C difference between ambient and board temperature, the mean temperature in the barrack is ≥ 30 °C.

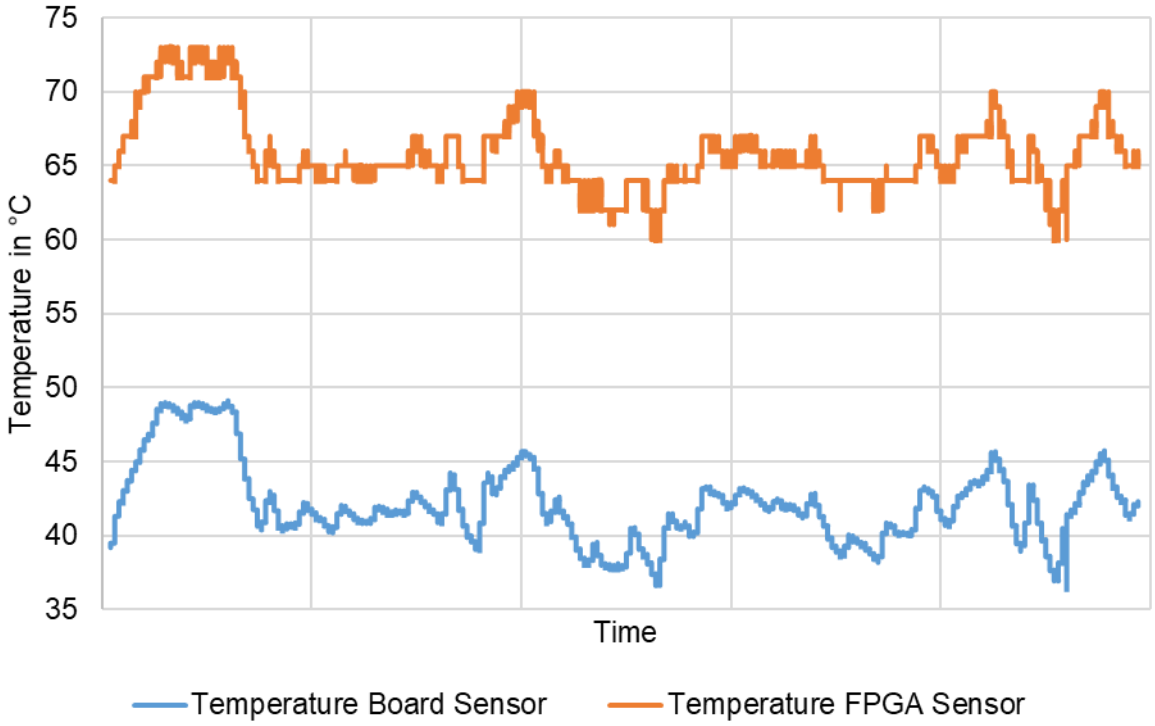


Figure 7.3: Temperature profile of one Run-In in the barrack

G Appendix G

The test process will be carried on until the last batch is received and all boards are tested. Figure 7.4 illustrates how the failure rate would develop affected by possible future failures. These failure times are evenly distributed starting at the current status until the planned end of testing. A detailed view shows the effect of failures in a shorter time period.

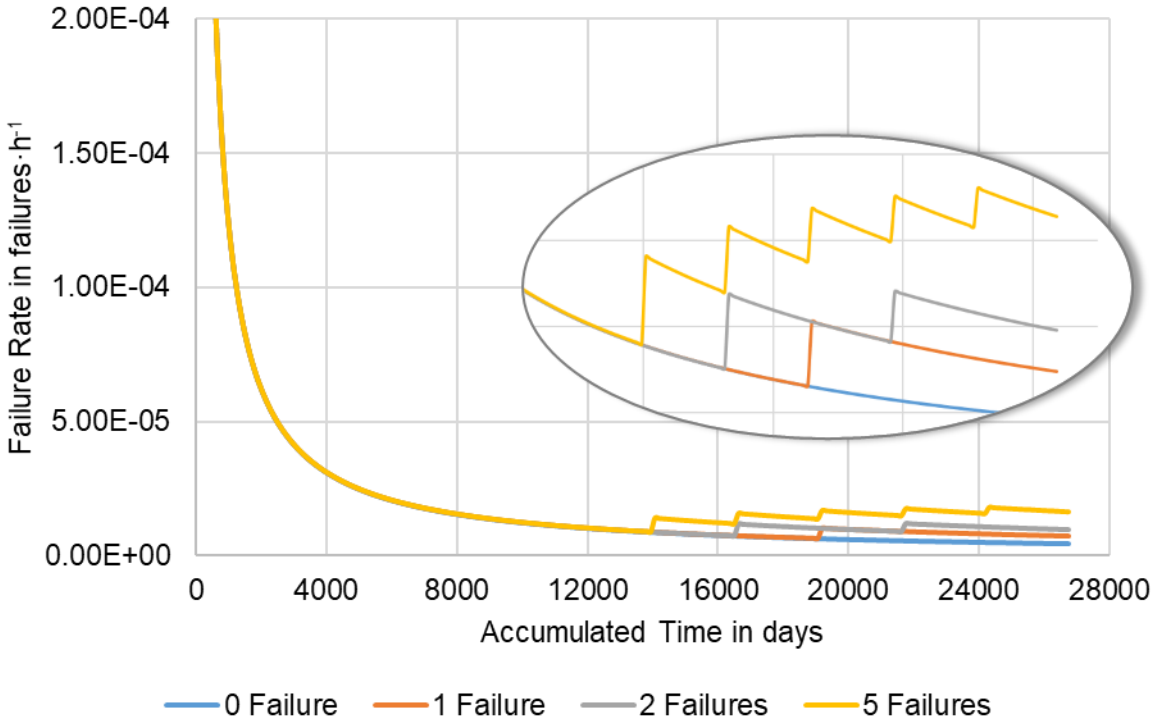


Figure 7.4: Run-In results until the planned end of testing depending on possible failures

The resulting $MTTF$ for the above assumptions are listed in Table 16. It shows that for a failure-free Run-In the $MTTF$ prediction is high enough for the BLM system.

Table 16: $MTTF$ assuming failures until end of Run-In

Failure Prediction	***MTTF* [h]**	***MTTF* [years]**
0	214 142	24.45
1	135 230	15.44
2	101 895	11.63
5	61 021	6.97