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SUPER CAVIAR: MEMORY MAPPING THE GENERAL-PURPOSE MICROCOMPUTER

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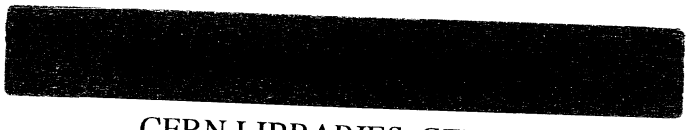

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SUPER CAVIAR: MEMORY MAPPING THE GENERAL-PURPOSE MICROCOMPUTER

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Abstract

Over the past 3 years, CAVIAR (CAMAC Video Autonomous Read-out) microcomputers have been applied in growing numbers at CERN and related institutes.

As typical user programs expanded in size, and the incorporated firmware libraries were enlarged also, the microprocessor addressing limit of 64 Kbytes became a serious constraint.

An enhanced microcomputer, SUPER CAVIAR, has now been created by the incorporation of memory mapping to expand the physical address space to 344 Kbytes. The new facility provides independent firmware and RAM maps, dynamic allocation of common RAM, automatic inter-page transfer modes, and a RAM/EPROM overlay.

A memory-based file system has been implemented, and control and data can be interchanged between separate programs in different RAM maps. 84 Kbytes of EPROM are incorporated on the mapper card itself, as well as an ADLC serial data link.

In addition to providing more space for consolidated user programs and data, SUPER CAVIAR has allowed the introduction of several improvements to the BAMBI interpreter and extensions to the CAVIAR libraries. A context editor and enhanced debug monitor have been added, as well as new data types and extended array-handling and graphics routines, including isoline plotting, line-fitting and FFT operations.

A SUPER CAVIAR converter has been developed which allows a standard CAVIAR to be upgraded to incorporate the new facilities without loss of the existing investment.

1. Standard CAVIAR memory constraints

Since CAVIAR (CAMAC Video Autonomous Read-out) microcomputers (ref. 1,2) were first introduced generally in early 1978, a total of over 85 systems has been installed, representing an investment of over 1 M Sw.Fr. During this period, users have applied the systems to a wide range of tasks (ref. 3), added more peripherals to the basic configuration, and developed BAMBI programs of increasing size and complexity. As a result, the restriction imposed by the microprocessor addressing limit of 64 Kbytes became a serious constraint in several applications.

CAVIAR is based on the 6800 microprocessor, and the address map of the standard configuration is shown in Fig. 1. 32 Kbytes of RAM, 28 Kbytes of system firmware and a 1K debug monitor are incorporated, while the remaining address space is occupied by miscellaneous functions such as the alphanumeric video RAM, floating point processor, and CAMAC, GPIB, FSK and data communications I/O.

First it became desirable to incorporate more firmware than the standard CAVIAR 28K BAMBI package. For high-speed program and data storage in stand-alone applications, many users acquired floppy disk units which could be connected directly to CAVIAR by the GPIB. While the units incorporate their own DOS, convenience of use could be improved by adding a support package to the CAVIAR firmware.

It was also desired to incorporate self-test programs, and a CAMAC system test, as part of the standard firmware. There was a demand to add a text editor, trace facility, and additional data types; and to enhance the libraries already provided by extended graphics, isoline plotting and fast Fourier transform routines.

As an interim solution, extra firmware was incorporated in some CAVIARs by adding a user EPROM card with a capacity of up to 16 Kbytes. However, owing to the restricted total address space, it was necessary to disable conflicting sections of RAM when extra firmware was included.

But at the same time, demand for additional RAM was also increasing. As the scale of experimental apparatus was enlarged, it became necessary to process larger histograms. In control and measurement applications, it was required to store tables of several thousands of parameter setting values, and limits against which measurements were to be compared. Cyclic storing of a significant amount of recent parameter history was found to be a valuable tool for the diagnosis of an apparatus failure when it occurred, but this too generates substantial data volumes.

2. Alternative solutions

Three possible solutions to the addressing constraint problem were considered. One approach to the problem is to tailor the hardware and firmware configuration of each CAVIAR to the requirements of the application. For example, where DOS support was required and also 32K RAM, a non-standard version could be made to substitute the

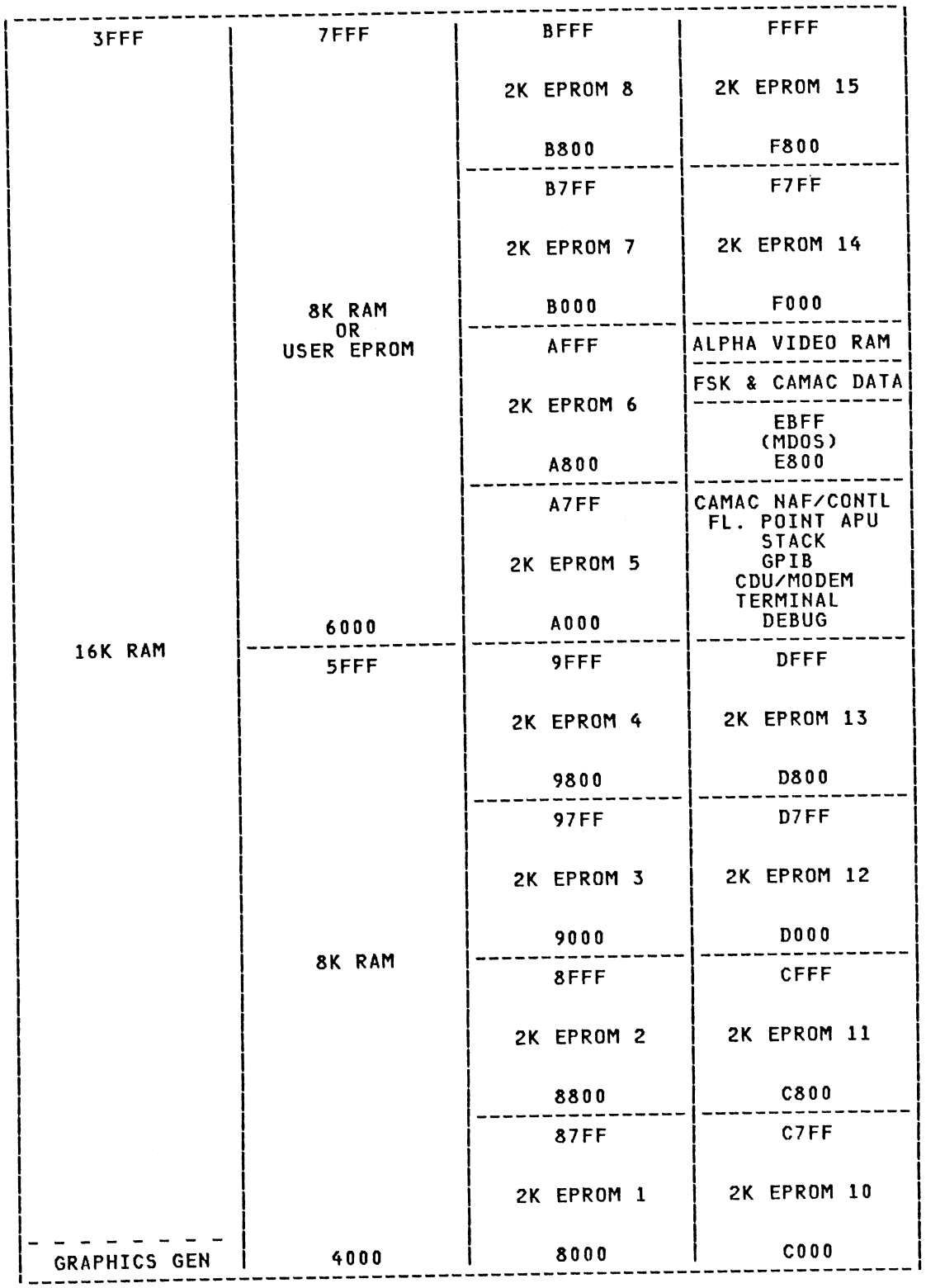

Fig. 1 Standard CAVIAR Address Map

debug monitor. Or where extended graphics were required but not ESONE CAMAC calls, a special version of the system firmware could be configured to suit.

The disadvantage of this approach is that the addressing space which can be gained varies considerably from case to case, and is least in those applications which exploit CAVIAR's facilities most fully.

In addition, the proliferation of a large variety of configurations would complicate the documentation and field support operations, which experience had shown were only just sufficient to deal with the distribution to all users of each revision of only one version of the system firmware within a reasonable time scale.

A more radical approach would have been to commence an entirely new development, using a more recently introduced microprocessor having a larger addressing capability. With the more powerful instruction set of such an MPU, some gains in execution speed could be anticipated also.

Since compatibility with existing user programs was considered essential, it would be necessary to re-write the BAMBI interpreter and libraries. In addition, this approach would not lead to a low-cost enhancement to the standard CAVIAR hardware, but would require a substantial part of the existing investment to be replaced.

The compromise solution which has been implemented involved the development of a memory mapping hardware and firmware upgrade, which can be retrofitted to a standard CAVIAR to provide enhanced facilities for minimum additional cost. This has been achieved by the introduction of a SUPER CAVIAR Converter, which extends the CAVIAR address space from 64 to 344 Kbytes, and a compatible single-card 256 Kbyte RAM.

3. Mapped memory configuration

While general-purpose memory mapper LSI circuits have been produced (ref. 4,5), a special memory configuration was found to be more suitable for SUPER CAVIAR, in which memory reference instructions access three distinct types of address space.

A simplified SUPER CAVIAR address map is shown in Fig. 2, which portrays a 512 Kbyte range. The first address space, occupying 8000-BFFF and E000-FFFF (of which E000-E7FF is internal to the MPU card), is a fixed 24 Kbyte area which is unmapped. In this area reside an enlarged kernel of the interpreter, a debug monitor and RAM stack, the floating-point arithmetic and function processor (APU), and interfaces for CAMAC, GPIB, FSK cassette, video alphanumerics and data communications I/O.

The majority of the addressable hardware in this area consists of standard CAVIAR cards, so that only 16 bits from the 19 required for full decoding are used, and the addresses image in the 14 unlabelled areas of the map.

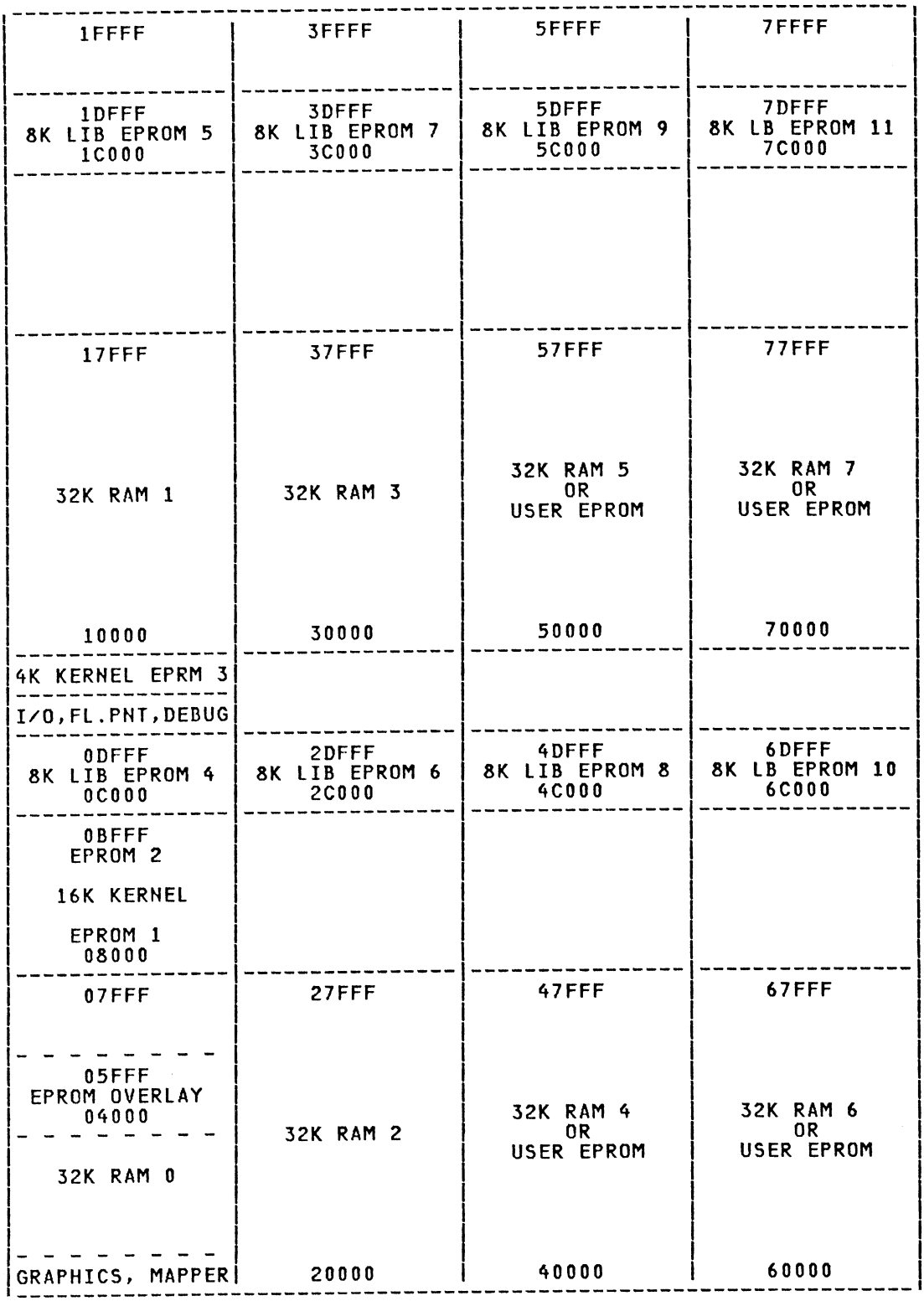

Fig. 2 SUPER CAVIAR Address Map

The second address space, composed of the eight areas XC000-XDFFF (X = 0-7) and consisting of 64 Kbytes of EPROM, comprises library firmware which is mapped into one 8 Kbyte logical area. The process of firmware mapping is transparent to the user, who simply finds that in SUPER CAVIAR there is a greater number of BAMBI calls at his disposition.

The third address space, which can accommodate 256 Kbytes of RAM or a mix of RAM and user-program EPROM, consists of the eight areas X0000-X7FFF, and is mapped into 32 Kbytes. Programs and data can be readily interchanged between different RAM maps, and programs resident in more than one map can be executed with no limit to the jumps between maps. RAM maps are also assigned logical unit numbers, and can be referenced as sequential files by I/O instructions.

All the memory mapping functions of the SUPER CAVIAR Converter are controlled by two PIAs located at addresses 4-7/8-B, immediately following the graphics generator. These locations were chosen to permit access by direct mode addressing for the highest speed of map switching, but they superpose base page RAM. The PIAs are configured as write-only, and current map numbers are read back from RAM.

Schottky TTL is used for the address translation logic, as a result of which mapped memory accesses can be achieved without extending the microprocessor cycle time. The SUPER CAVIAR Converter card is shown in Fig. 3.

4. Memory mapped development system

To permit debugging of the libraries and map control routines, the memory mapping system of SUPER CAVIAR was implemented in the Exorciser system used for software development. However, the BAMBI system which resides in firmware in SUPER CAVIAR required to be held in RAM during development.

This was achieved by making a special development version of the prototype mapper. A set of eight 8K RAM cards was converted to EPROM simulators and mounted on an auxiliary chassis to which control and timing signals were conveyed by an extension of the Exorciser bus. The remaining address, chip (card) select and data lines were connected from each RAM card to DIL plugs which directly replaced the EPROMs on a SUPER CAVIAR Converter which had been modified to permit writing at the firmware addresses. The unmapped kernel EPROMs were disabled and substituted by normal Exorciser mainframe RAM.

During initialization, the Exorciser MDOS system overwrites low-order addresses at which the map, mode control, and other registers are located. The converter card was provided with means to disable these addresses during the initialization and loading of each file, and enable them for manipulation by the debug monitor to change the maps between files.

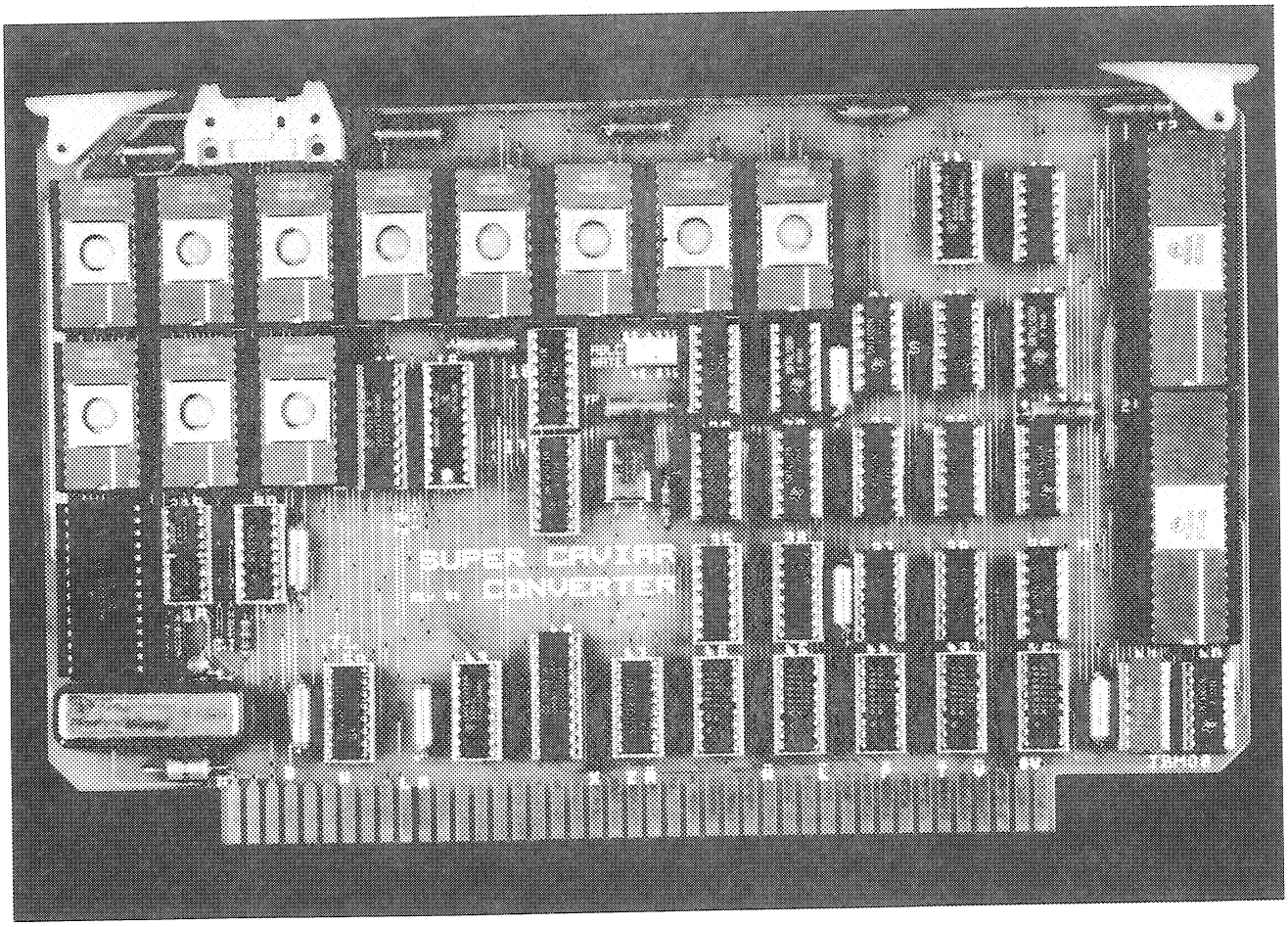

Fig. 3 SUPER CAVIAR Converter

5. EPROM memory

Since CAVIAR was originally designed, available semiconductor memory densities have increased from 8 Kbits for UV EPROM and 4 Kbits for dynamic RAM to 64 Kbits in both cases. These advances have allowed the complete 84 Kbyte system firmware package to be accommodated on the SUPER CAVIAR Converter card itself, and a new single-card 256 Kbyte RAM compatible with the mapping to be introduced.

Converter pc board area being at a premium, a novel EPROM device (ref. 6) was selected which, by using special circuitry to multiplex the enable and Vpp functions, fits a 24-pin DIP instead of the JEDEC 28-pin package. 8 mapped EPROMs accommodate the entire SUPER CAVIAR library.

The kernel of the BAMBI interpreter, formerly occupying 17K of the standard CAVIAR 28K firmware, has been expanded to 20K and can be programmed in 3 EPROMs on the Converter. One device can be the half-functional type currently marketed at reduced cost, with jumper selection of the active section.

The expansion of the kernel firmware has allowed the introduction not only of the map control procedures, but also of several improvements to the BAMBI interpreter. Byte and double-integer data types have been added, COM statements with equivalence have been introduced, and error messages considerably improved.

Where an existing standard CAVIAR is upgraded to SUPER CAVIAR, the 8K area C000-DFFF of the original 28K system firmware card can be disabled, and the cost of the new kernel EPROMs saved by programming the new firmware in the remaining 20K section of this card. In a new SUPER CAVIAR, the card can be omitted entirely.

6. Economy RAM upgrade

Existing standard CAVIARs incorporate a 32 Kbyte RAM card which can be modified for use with the SUPER CAVIAR Converter and upgraded to 64K. The total cost of such a card exceeds that of a new 256 Kbyte RAM card populated to 64K, no error detection is provided, and the card has some technical drawbacks. But the incremental cost of the upgrade is low enough that this procedure is of interest in cases where a modest retrofit of a standard CAVIAR is desired.

To minimise the modifications to the existing RAM card required for use with the memory mapping, the SUPER CAVIAR Converter generates a set of new VRA (valid RAM address) signals on 4 free microcomputer bus lines (see Table 1). In particular,

$$\overline{VRA0} = VUA.A15.\overline{A17}.\overline{A18}$$

After adding 4116 RAMs to the card and configuring it for 64K operation, it is thus only necessary to transfer the normal A15 input of the card to the new address line A16, and the VUA input to VRA0, to achieve compatibility with the RAM mapping. The detailed procedure is given in ref. 7.

BUS CONTACT	EXORCISER I	EXORCISER II	SUPER CAVIAR
23	N/C	N/C	A16
22	N/C	Gnd	A17
20	N/C	Gnd	A18
$\overline{A}$	N/C	N/C	VRA0
Z	N/C	Gnd	VRA1
Y	N/C	Gnd	VRA2
X	N/C	Gnd	VRA3
18	$\overline{TSC}$	CLOCK	PTM CLK
21	AC OFF	Gnd	$\overline{PEN}$

TABLE 1

SUPER CAVIAR micromodule bus - Additional signal assignments

7. 256 Kbyte mapped RAM

The arrival of the 64 Kbit semiconductor RAM has been the subject of unusual publicity in circles well beyond the computer electronics world. Market predictions for what could be the industry's first $1000M device have spurred the founding of new enterprises, and promised fortune to those able to overcome the formidable design and manufacturing challenges of a 135,000-element LSI chip.

At this time, about 10 manufacturers have devices in full or trial production, with a variety of refresh, speed and power characteristics, while price and availability are highly variable. In these circumstances, it is not easy to make the optimum choice for a memory product which may have a lifetime of several years (the 256 Kbit RAM chip is not expected before 1983), and which constitutes the highest semiconductor cost element in SUPER CAVIAR.

In spite of the attractive circuit simplification offered by devices promising automatic and self-refresh modes, previous experiences with proprietary products having no second-source cautioned the exercise of prudence. The 256 Kbyte dynamic RAM card design was therefore based on the use of 'dumb' 64 Kbit chips (ref. 8) with externally-generated RAS-only refresh cycles. Both 128-cycle/2ms and 256-cycle/4ms variants can be accommodated.

By generating stable timing signals from multi-tap delay lines, adequate margins are obtained with lowest-cost 250 ns access-time devices, even when undershoot damping is applied and phase 1 of the microprocessor clock cycle is used for fully-transparent hidden refresh operation. The card can be populated, or a fully-populated card can be enabled, in increments of 64 Kbytes (2 maps); and the address areas of disabled sections are freed for use by other mapped memory devices, such as a 128 Kbyte user-program EPROM card which is being developed.

Separate trees generate write parity and check that of data read. Write protect and parity disable can be selected manually on the RAM card, and parity error interrupts to the MPU (which are non-maskable) can be inhibited by a control signal from the SUPER CAVIAR Converter card. This facility allows the system firmware to read RAM locations before they have been written, as is required at power-on to distinguish from manual reset.

As with the economy memory upgrade, the 256 Kbyte RAM uses the VRA selects, in this case to permit the EPROM overlay feature described later.

To provide SUPER CAVIAR with a new facility for generating interrupts at programmable time intervals, a 6840 multi-mode triple timer (ref. 9) has also been provided on the 256K RAM card. The timer input is derived from the 6 MHz ADLC clock on the SUPER CAVIAR Converter, which is free from the phase stretching applied to the MPU clock during accesses to the floating-point APU.

8. Common RAM

As in standard CAVIAR, SUPER CAVIAR interrupts are vectored through locations in firmware immediately below FFFF, which are unmapped, and then through locations in low-order RAM. To facilitate the processing of interrupts which may occur while any RAM map is selected, it is convenient if a range of RAM at the base of each map be common to all of them. In addition to the interrupt vectors, the common RAM is used for the EPROM and RAM pointers required for inter-RAM communication, and for the storage of parameters which are common to all RAMs.

The SUPER CAVIAR Converter maps an address range starting at the lower boundary of all 32K RAM sections to the corresponding range in RAM 0. The upper limit is programmable through a common range select register in power-of-two steps from 32 to 512 bytes. The range is normally set to 32 bytes at initialization, and can be expanded dynamically if required.

9. Transfer modes

The speed and flexibility of transfer operations can be enhanced by special modes (ref. 10) in which the memory mapping is a function of the direction of the data transfer. The SUPER CAVIAR Converter provides a facility for the program selection of transfer modes which modify the RAM mapping on a cycle-by-cycle basis.

In one mode, microprocessor read operations (including executable code fetches) access the currently selected RAM map, while all write cycles reference RAM 0. In an alternate mode, data are loaded from RAM 0 and automatically stored in the selected mapped RAM. Common RAM mapping overrides transfer mapping in the affected range.

10. Overlay mode

The SUPER CAVIAR Converter provides one overlay mode, to facilitate the development in RAM of assembler-written subroutines which are subsequently to be added to the BAMBI firmware library. While RAM/EPROM overlay action requires complementing the existing A15 address line, modification of the MPU card is avoided by the use of the new VRA signals for all RAM map selection.

When overlay mode is selected, the 8 Kbyte address range C000-DFFF normally occupied by library EPROM 4 is mapped into RAM 0 at 4000-5FFF. However, the development of user subroutines is not an activity currently supported by software contacts and documentation.

11. ADLC Data communications

A new serial data link facility has been added to CAVIAR by the incorporation of a 68A54 ADLC (ref. 11) on the SUPER CAVIAR Converter. This serial interface, including a digital PLL clock circuit and interrupt-driven software package (ref. 12), is intended to meet the need for a serial diagnostic network in large DAQ systems.

Up to 256 SUPER CAVIARs can be connected in an ADLC loop, and data can be exchanged between that acting as primary station and any addressed secondary (or all secondaries simultaneously). The secondaries can execute independent BAMBI programs concurrent with ADLC data link transfers to or from any of their mapped RAMs.

Any secondary can be commanded to treat the ADLC loop as terminal I/O. Thus the primary SUPER CAVIAR can (either by program execution or from its terminal in TMODE) load and run programs in any of the secondaries.

Switch-selectable transmission rates of 23.4375-46.875 KBaud are provided (6 MHz/256-128), and RS-422 (ref. 13) drivers are incorporated for a transmission range exceeding 1 km over telephone-type line. Circuit integrity is maintained by a reed relay should any SUPER CAVIAR in the ADLC loop be powered down.

12. Program development

SUPER CAVIAR incorporates a general-purpose editor which may be used to edit text including BAMBI programs. The editor is an interactive program which accepts commands similar to those of the HP minicomputer editor.

The source and destination of the text to be edited can be specified as the current BAMBI program, a logical unit, a RAM map, or a BAMBI array.

A new trace facility is provided to aid the debugging of user BAMBI programs. When tracing is enabled the line numbers, followed by the values of a preselected set of parameters, are printed for all BAMBI program lines executed.

13. Data analysis and display

SUPER CAVIAR includes a new set of calls intended to enhance the signal analysis capability of the standard unit. Routines using the fast Fourier decimation in frequency algorithm (ref. 14) are provided to compute the discrete Fourier transform and power spectrum of a data vector. An inverse transform routine is also provided.

In addition to the standard CAVIAR facilities for data display by plotting with scaling, gridding, rotation, labelling, replot and hidden line options, SUPER CAVIAR incorporates a library routine to display a function of two parameters as an isoline plot.

Grid resolution, data limits and total number of isolines are selectable independent of data array dimensions. Isolines, which according to the application may represent isobars, isotherms, height contours or equipotentials, are flagged at a specified constant or progressive step interval.

14. Conclusion

The mapping facility described in this paper allows the expansion of a standard CAVIAR microcomputer memory to 84 Kbytes of EPROM and 256 Kbytes of RAM.

As well as providing extra memory for user programs and data, this upgrade has allowed the incorporation of valuable improvements to the BAMBI interpreter and additions to the system library. For further details, the reader should consult ref. 15. These features offer the experimenter a substantial enhancement in microcomputer capability for a modest additional cost.

15. Acknowledgments

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