Summer Studentship Report

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ACAI: Automated Clock-Oriented Acquisition Infrastructure for LHCb TFC Clock Studies

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Summary

Clock stability is a critical parameter for the Timing and Fast Control (TFC) system of the LHCb detector, ensuring reliable readout across all subdetectors. With the current clock distribution architecture reaching its limitations, particularly in terms of skew stability, scalable and reproducible testing are required for the upcoming Run 4 and Run 5 upgrades. In this project, we developed the Automated Clock-Oriented Acquisition Infrastructure (ACAI), a reusable, queue-driven data acquisition framework enabling systematic clock studies across different hardware and firmware configurations. The system was validated on known clock trees, provided insights into the behaviour of novelty firmware, and highlighted correlations between FPGA and external instrument measurements that validates the FPGA measurement module. This work represents a strategic step in ensuring the robustness of testing to plan next upgrades of the LHCb TFC hardware architecture.

Contents

1 Introduction

The Timing and Fast Control (TFC) system defines the synchronisation of detector readout in LHCb. Given this broad control, clock stability across the distribution tree is essential to the LHCb functioning - maintaining timing alignment between subdetectors and ensure high-quality data acquisition.

However, the current clock tree implemented on SOL40(see figure 1) is limited in its skew stability, a constraint that becomes more severe in the context of the LHCb Upgrade II and the requirements of Run 4 and Run 5 at the High-Luminosity LHC (HL-LHC). Therefore, the group has done extensive work on new architectures to improve it, but so far the clock studies data acquisition were performed using ad-hoc scripts and hardware-specific approaches. While useful, they lacked scalability, reproducibility, and the flexibility to explore the wide space of firmware and hardware configurations.

This project addresses these limitations by delivering a systematic and reusable infrastructure for clock testing, aiming to provide reliable input for TFC upgrade choices and to enable efficient validation workflows.

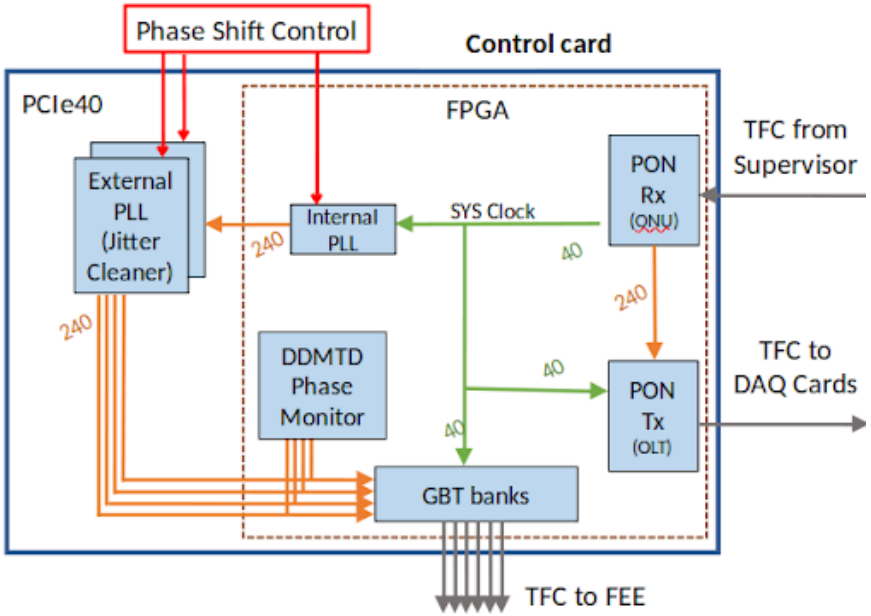

Figure 1: Current clock tree on the SOL40 board of the TFC system.

2 Goals

The objectives of this work were:

- Develop a reproducible and automated testing infrastructure for clock studies.
- Ensure reusability across testbenches, hardware, and firmware variations.
- Provide scalability in test size, duration, and number of subdetectors studied.

- Validate firmware options and edge cases relevant to clock stability.
- Explore correlations between FPGA-based measurements and external instruments as a step towards runtime monitoring.

3 The ACAI Infrastructure

The Automated Clock-Oriented Acquisition Infrastructure (ACAI) was developed to meet these goals. Its main design principles are derived both from good software engineering practices and the usability requirements of the platform. The final design decisions that support our goals can be summarized as:

- **Declarative configurations:** Tests, instruments, and parameters defined in YAML files, enabling reproducibility and fast reconfiguration.
- **Queue-driven acquisition:** An asynchronous DAQ core separates data-taking from peripheral tasks, improving scalability and efficiency.
- **Hardware abstraction:** Instrument-specific controllers are decoupled from test logic, making the system portable across different boards and firmware versions.
- **Maintainability:** A modular, object-oriented code structure ensures clarity and extensibility.
- **Validation and emulation:** Configurable emulation modes allow testing without hardware, ensuring robustness of the framework itself.

The infrastructure enables not only faster and more reproducible tests, but also ensures that insights gathered from one testbench can be consistently compared to others. In practice, this transforms the process of clock studies from ad-hoc scripting into a systematic, maintainable workflow. The final achieved architecture is represented on the diagram of figure 3 on a module level abstraction - representing the daemon and measurement processes at the nottom and showing how the modules and configuration files spread out on the measurement process.

4 Measurements and Insights

Using ACAI, some datasets were already collected across different reconfiguration conditions and firmware variations. The framework enabled systematic measurements of clock skew and timing stability, as well as comparisons between FPGA readings and oscilloscope traces.

4.1 Clock Skew Distributions

ACAI reproduced the same results for architectures and configurations with known stability, confirming the validity of the automated approach. The tests performed to validate those

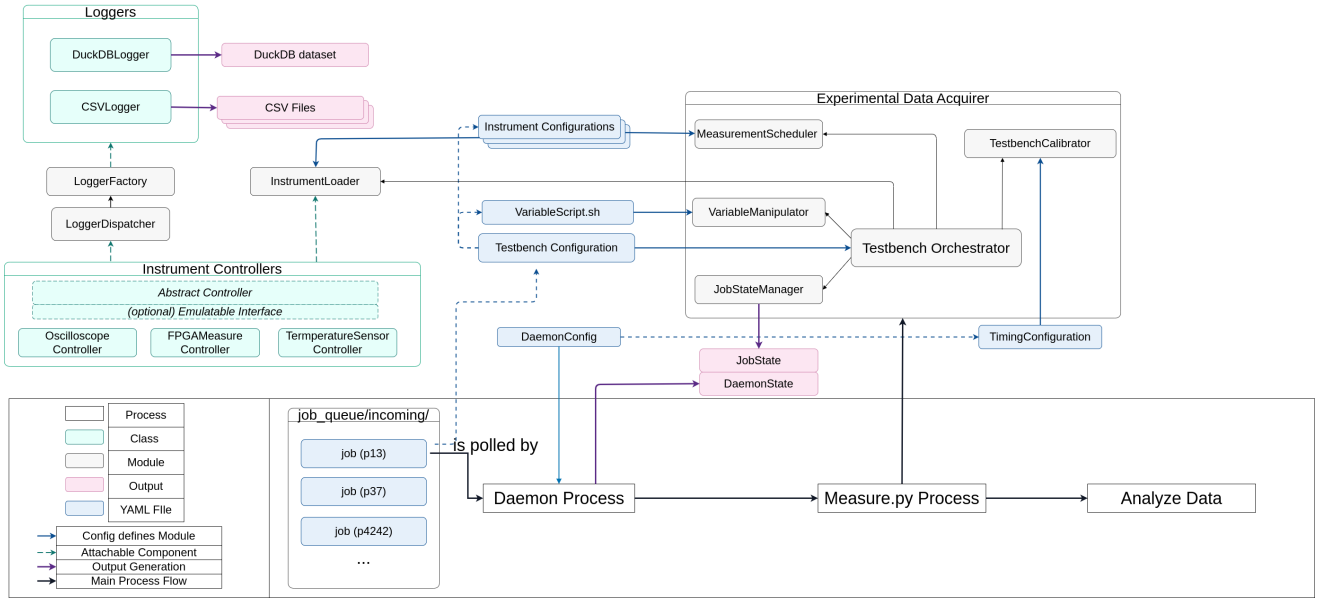

Figure 2: Software architecture of the ACAI framework, showing decoupling of hardware controllers and test logic.

measurements regarded temperature-skew dependency and skew distribution on the Marseille firmware (i.e. the one used so far in production), largely explored by the group before.

A characteristic two-peak behaviour in skew distributions, already observed in earlier studies, was also reproduced with ACAI in a systematic way. The current analyses provided indications that allowed to isolate this feature and trace (at least a major part of) its explanation to the alignment procedure of external PLLs in firmware, offering a more structured path to follow up on these observations.

4.2 Insights and Preliminary Results

Beyond validating known benchmarks of clock skew stability, ACAI enabled the collection of datasets that would have been impractical to obtain with ad-hoc methods. The framework systematically exposed behaviours such as variations across firmware configurations, subtle patterns in skew distributions, and correlations between FPGA TXCLKOUT readings and external oscilloscope measurements.

While these results are preliminary, their value lies in the structured way they were obtained. The automated approach highlights potential trade-offs in firmware design, identifies patterns that deserve deeper investigation, and suggests that FPGA-based monitoring could, in the future, contribute to runtime assessment of clock quality. These insights, though not yet statistically final, illustrate how ACAI transforms exploratory observations into reproducible, comparable datasets, providing a fertile ground for future developments.

5 Relevance to LHCb

The insights enabled by ACAI directly strengthen the LHCb upgrade programme in several key ways. Primarily, it establishes a reliable validation mechanism for the TFC clock system, which is a fundamental component for the success of Run 4 and Run 5 operations at the HL-LHC. By doing so, ACAI significantly reduces our traditional reliance on manual and ad-hoc workflows, thereby saving considerable time and expert effort. This efficiency, in turn, provides us with a systematic methodology for comparing firmware and hardware options across different subdetectors. Furthermore, the work opens up valuable exploratory insights into future runtime monitoring possibilities, which could become critical for the detector's operational resilience in the years to come.

6 Future Work

Future extensions of ACAI will focus on improving efficiency and coverage. Work is already planned to parallelize test execution in order to reduce acquisition time, while dataset versioning with embedded metadata will make analyses easier to reproduce. Finally, the development of runtime analysis strategies based on FPGA self-monitoring is expected to open the way towards online assessment of clock quality.

7 Conclusions

The ACAI framework demonstrates that automated, declarative testing can transform clock stability studies from ad-hoc and labour-intensive tasks into reproducible and extensible workflows. While the scientific results are preliminary, the infrastructure has already validated previous measurements, uncovered new behaviours in firmware-induced skew, and pointed towards runtime monitoring possibilities. These contributions are directly relevant for ensuring the robustness of the TFC system in preparation for Run 4 and Run 5 of LHCb at the HL-LHC.

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