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TITRE :

Conception et mise au point de l'électronique frontale du détecteur de pied de gerbe (Preshower) de l'expérience CMS

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To my 3 wonderful children:

Daniel, Thomas and Matthew

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Résumé en Français

Préface

Le travail présenté dans cette thèse concerne la conception et la mise au point de l'électronique de lecture du détecteur Preshower (détecteur de pied de gerbe), de l'expérience CMS, qui sera installé sur l'accélérateur LHC au CERN. Ce détecteur requiert un système d'acquisition capable de mesurer, à intervalles de 25 ns, l'énergie déposée par des particules chargées, dans quelques 140000 canaux de capteurs à pistes silicium. L'électronique de lecture doit présenter des performances élevées (précision de mesure meilleure que 5%, grande gamme dynamique, faible consommation, environnement radiatif intense). Le développement de circuits ASIC, autorise une grande densité d'intégration. Ceci permet de concentrer l'électronique de traitement près des capteurs et ainsi de réduire le flux d'informations transitant en direction des salles de comptage. Le système électronique intégré développé pour le Preshower est le système PACE ("Preshower Analog CMS Electronics"); sa conception est l'objet ce cette thèse.

Le chapitre 1 situe le détecteur Preshower dans le contexte du LHC et de l'expérience CMS. Les recherches sur la physique, qui seront permises avec le LHC, sont présentées avec un accent particulier sur la question "quelle est la nature de la masse ?" Le chapitre décrit le rôle du Preshower dans la recherche du boson de Higgs, présente les caractéristiques physiques et géométriques du détecteur ainsi que les spécifications électriques du circuit PACE .

Le chapitre 2 se rapporte aux contraintes particulières supportées par les composants électroniques confinés dans un environnement très radioactif. Il est constitué de 3 parties : La première partie présente les différents profils de radioactivité dans différents secteurs de CMS, la deuxième les mécanismes de défaillance des composants électroniques soumis à des radiations importantes, et la troisième les différentes technologies de circuits intégrés existantes capables de répondre au besoin.

Le chapitre 3 se rapporte à la conception et aux résultats obtenus avec le circuit intégré prototype initial (PACE1). Des résultats de test en faisceau, avec un module comprenant 8 détecteurs et leur ASIC de lecture y sont également présentés.

Le chapitre 4 présente une modification majeure dans l'architecture de lecture de PACE, le changement d'une architecture à intégration de courant à une architecture à tension échantillonnée. Les motivations de cette évolution sont expliquées et un nouveau préamplificateur de charges avec gain commutable (circuit Delta) est décrit.

La fonction Delta a été utilisée dans 2 circuits test dont les résultats de mesures, avant et après irradiations, sont présentés.

Le chapitre 5 présente la conception complète du circuit PACE2 dans une technologie durcie aux radiations. Ce chapitre couvre la conception : du préamplificateur (Delta), du circuit de mise en forme ("shaper") à gain commutable, et celle de la mémoire analogique à tension échantillonnée.

Chapitre 1: Introduction au Preshower de CMS

Section 1.1 Les buts physiques

La plus grande partie de notre compréhension actuelle de l'univers est décrite par une théorie sur la constitution interne de la matière dite théorie du modèle standard (SM). Cependant, le modèle standard n'est pas tout à fait complet dans la mesure où il nécessite l'emploi de paramètres empiriques comme la masse des particules élémentaires. Une particule qui pourrait expliquer la masse, cohérente avec le modèle standard, est une particule sans spin, non encore observée, appelée boson de Higgs (H^0).

La théorie de Higgs ne prédit pas la masse même de cette particule (M_H), néanmoins, pour concorder avec les éléments du modèle standard cette masse devrait se situer dans l'intervalle ($\sim$100 GeV $< M_H <$ 1 TeV). Les résultats récents en provenance des expériences LEP II permettent d'estimer une masse du boson de Higgs inférieure à 215 GeV avec un niveau de confiance (CL) proche de 95%.

L'accélérateur du LHC produira des collisions récurrentes, entre protons, jusqu'à une énergie de 14 TeV (centre de masse). Ainsi, l'étendue d'énergie prédite par la théorie de Higgs sera largement couverte. Une fois créés, les bosons de Higgs présentent plusieurs canaux possibles de désintégration. L'expérience CMS ("Compact Muon Solénoïd") sera le terrain d'un grand nombre de sujets de recherche en physique. CMS est néanmoins optimisé pour la détection du Higgs, avec une optimisation particulière pour observer sa désintégration en 2 photons ($H^0 \longrightarrow \gamma\gamma$) qui est le canal le plus facilement observable pour une masse $M_H < 140$ GeV. De ce fait, CMS est pourvu d'une excellente résolution en énergie dédiée à la reconstruction $H^0 \longrightarrow \gamma\gamma$.

Néanmoins, dans cette expérience, un certain nombre d'événements physiques (donnant naissance à des électrons et à des photons) produisent des effets ressemblants au processus recherché. La désintégration de pions neutres (π^0) en deux photons très proches dans l'espace qui apparaissent dans le calorimètre électromagnétique (ECAL), dans la partie bouchon, comme un seul photon, constitue une source de bruit de fond. Afin de détecter des photons très proches dans l'espace, et ainsi les différentier des photons résultants de la désintégration du Higgs, il est nécessaire d'interposer un détecteur de fine granularité devant le calorimètre électromagnétique. Ce détecteur est le Preshower.

Les figures, tableaux et équations importants de ce chapitre sont les suivants :

- La figure 1.1 présente schématiquement l'anneau du LHC avec la position des 4 sites d'expérience ATLAS, ALICE, CMS, et LHCb.
- Le tableau 1.1 présente l'inventaire des éléments du modèle standard répartis en 3 familles de quark, leurs leptons associés et les bosons transportant les forces.
- La figure 1.2 montre l'évolution des expériences de physique des hautes énergies et la gamme d'énergie dans le centre de masse adressée par le LHC.
- La figure 1.3 montre le diagramme de Feynman de 4 mécanismes de production possibles du Higgs dans le LHC.
- La figure 1.4 montre les différentes canaux de désintégration possibles dans le modèle standard et leur probabilité associée (rapport d'embranchement). Le tableau 1.2 dresse les désintégrations les plus facilement identifiables du Higgs en fonction de sa masse.
- La figure 1.5 est une vue en coupe de l'expérience CMS faisant apparaître les différents sous détecteurs.
- La figure 1.6 donne la largeur naturelle du Higgs en fonction de sa masse. Un Higgs léger aura une largeur étroite, ce qui demande un détecteur avec une très bonne résolution à la fois en masse et en énergie.
- La figure 1.7 illustre le principe d'un calorimètre à échantillonnage et montre la forme d'une gerbe électromagnétique.
- La figure 1.8 montre les 4 principaux événements physiques qui peuvent ressembler à la désintégration du Higgs en 2 photons. Le Preshower est capable d'identifier le quatrième type et permet donc de rejeter le bruit de fond causé par la désintégration des pions neutres.

Section 1.2 Le détecteur Preshower dans CMS

Le Preshower est un détecteur à granularité fine placé dans les bouchons, en avant du calorimètre électromagnétique (ECAL). Son rôle est de détecter les photons avec une bonne résolution spatiale et de mesurer leur énergie avec une bonne précision. Il permet de rejeter le bruit de fond causés par la désintégration des pions neutres.

Le Preshower consiste en un calorimètre électromagnétique à échantillonnage dont le principe est le suivant : Quand des photons pénètrent dans un matériaux dense il se produit une cascade électromagnétique (encore appelée gerbe électromagnétique) qui contient des électrons, des photons et des positrons. Les particules chargées peuvent être détectées et leur énergie mesurée. Les éléments de détection choisis sont des capteurs silicium à pistes. Deux plans de capteurs, orthogonaux entre eux, permettent une résolution bidimensionnelle. Les capteurs silicium ont une réponse linéaire à la charge déposée. Ainsi l'énergie déposée dans l'absorbeur en plomb peut être mesurée

de façon précise, puis combinée avec la mesure d'énergie donnée par le détecteur ECAL, pour obtenir l'énergie totale du photon incident.

Les plans de capteurs ont la forme d'un disque d'un rayon intérieur de 0.457 m et d'un rayon externe de 1.23 m, offrant ainsi une couverture $\eta = 1.653$ à $\eta = 2.6$. Il y a 4 disques au total (2 dans chaque bouchon). Au total ∼4300 capteurs silicium, composés de 32 pistes de 1.9 mm × 60 mm sont répartis sur ces disques. Les dimensions d'un capteur silicium sont de 63 mm × 63 mm.

L'assemblage du Preshower est décomposé en 3 phases distinctes, correspondant chacune à la réalisation d'un sous-ensembles pouvant être testé isolément. La structure élémentaire (micro-module) regroupe un capteur de 32 pistes et l'électronique de lecture analogique associée. Au niveau supérieur on définit des "ladder" (regroupement de micro-modules en matrice) qui regroupent de 7 à 10 micro-modules. Finalement, les ladder sont assemblés sur les disques.

- La figure 1.9 montre l'emplacement du Preshower dans les régions bouchons de CMS ainsi que sa couverture.
- La figure 1.10 présente le profil de gerbe électromagnétique provoqué, dans le Preshower, par un photon incident et par 2 photons incidents très proches dans l'espace.
- La figure 1.11 est une vue en coupe du Preshower.
- La figure 1.12 est une vue en coupe d'un capteur silicium utilisé dans le Preshower.
- Les figures 1.14 à 1.16 montrent les différentes composantes d'un disque du Preshower (micro-module, "ladder", système complet).
- La figure 1.17 montre le résultat de simulation de 2 photons proches dans l'espace traversant le détecteur ECAL.

Section 1.3 Etablissement des spécifications de l'électronique du Preshower.

La conception du système PACE ("Preshower Analog CMS Electronic") est l'élément central de cette thèse. Une caractéristique essentielle du système d'acquisition PACE est la très grande gamme dynamique de signal d'entrée (charge comprise entre 4 fC et 1600 fC) ce qui correspond à une échelle de 1 à 400 MIPs ("Minimum Ionising Particles"). Garantir une bonne précision de mesure au seuil de 1 MIP requiert une électronique bas bruit. Dans l'application, 2 gammes dynamiques différentes sont à considérer : une gamme réduite en mode calibration et une gamme plus étendue en mode acquisition. Pour optimiser la résolution de mesure dans ces 2 cas, la chaîne de lecture devra présenter un gain programmable.

- Mode acquisition : 0.4 MIP < gamme dynamique < 400 MIPs (10 bits)
- Mode calibration : 0.16 MIP < gamme dynamique < 50MIPs (9 bits)

Le Preshower est composé de 4300 capteurs de 32 pistes ; un circuit de lecture de 32 voies a donc été choisi pour s'adapter à cette segmentation. Le développement de circuit ASIC permet d'installer l'électronique de lecture à proximité immédiate des capteurs.

Au total, le Preshower représente 137600 voies d'acquisition qui sont échantillonnées toutes les 25 ns avec une précision de 10 bits. Ce volume d'information de $\sim 5.6 \times 10^{15}$ bits/s n'est pas transmis jusqu'en salle de comptage. Pour réduire ce volume de données, et ne retenir que les informations intéressantes, la machine CMS délivre un certain nombre de signaux de déclenchement ("trigger"), d'une manière hiérarchique. Le premier niveau de déclenchement (LV1) est produit avec un décalage de 3.2 μs par rapport à l'événement physique. PACE doit donc retenir l'information qu'il échantillonne pendant une durée au moins égale à 3.2 μs, et ne transférer sur sa sortie que les échantillons cohérents avec LV1. Une des architectures qui permet de réaliser cette fonction est la mémoire analogique ; elle a dans PACE les caractéristiques suivantes : 32 lignes, 160 colonnes. Le nombre de colonnes (profondeur de la mémoire) est conditionné par :

- Le décalage du signal LV1 (3.2 μs)
- Le nombre de cases mémoire nécessaires à coder un événement (3)
- Le nombre d'événements (correspondants aux déclenchements LV1) que l'on souhaite pouvoir garder en mémoire simultanément (8)

Finalement la profondeur mémoire nécessaire est calculée de la manière suivante :

- P = (3.2 μs / 25 ns) + (3×8) = 152
- Une profondeur de 160 colonnes a été retenue (marge d'une case mémoire par événement)

Cette profondeur permet d'accepter une fréquence maximale de déclenchement LV1 de 100 kHz et autorise une fréquence de relecture de 20 MHz, avec une probabilité de débordement de 1×10^{-5}.

Le chapitre se termine par un tableau qui résume les principales spécifications de PACE. De nombreux renvois à ce tableau sont faits tout au long de ce rapport.

- La figure 1.19 présente l'architecture simplifiée de la mémoire analogique de PACE.
- La figure 1.20 montre le couplage DC entre une piste de capteur silicium et l'électronique de lecture. Les entrées des préamplificateurs doivent présenter une impédance faible et doivent être capables d'absorber le courant de fuite du capteur.
- Le tableau 1.6 résume les spécifications électriques de l'électronique de lecture PACE.

Chapitre 2, Considérations sur les radiations

Les capteurs silicium, comme l'électronique de lecture, seront exposés à des taux de radiation élevé, ce qui n'est pas sans conséquence sur l'évolution de leurs performances. Ce chapitre présente l'environnement radiatif dans CMS (section 2.1), les effets des radiations sur les composants électroniques (section 2.2), et les technologies disponibles pour concevoir des ASICs devant fonctionner dans un tel environnement (section 2.3). Le chapitre conclut en proposant un choix technologique pour la réalisation de PACE.

Section 2.1 L'environnement radiatif dans CMS.

Les particules secondaires les plus massivement produites dans les collisions proton-proton dans le LHC seront des pions de grande énergie. D'autres mésons comme les kaons (k) ainsi que des baryons comme les protons et les neutrons de grande énergie peuvent également être produits. Les pions chargés constitueront l'essentiel du flux de particules chargées. L'intensité de ce flux suit une loi en $\frac{1}{(r_\perp)^2}$, dans laquelle $r_\perp$ représente la distance à l'axe du faisceau. Le nombre de pions neutre produits est environ la moitié du nombre de pions chargés. Le pion neutre a une durée de vie moyenne de 8.4×10^{-17} s, il se désintègre donc sur une distance de quelques dizains de nm à partir du point d'interaction. Bien qu'il y ait plusieurs mécanismes possibles de désintégration, 98.8% des pions neutres se désintègreront en 2 photons, $\pi^0 \rightarrow 2\gamma$. Il y aura donc un flux de photon du même ordre de grandeur que le flux de particules chargées qui aura la même distribution en ce qui concerne la pseudorapidité mais une impulsion moyenne deux fois plus faible.

La dose d'irradiation équivalente prédictible dans les régions bouchon varie avec η. Le maximum pour $\eta = 2.6$ sera de 60 kGy (6 Mrad(Si)).

Les sous produits secondaires vont perdre une partie de leur énergie en traversant successivement les matériaux des différents détecteurs (le détecteur de trace (tracker), les calorimètres électromagnétiques (ECAL) et hadronique (HCAL)). Dans chaque couche de détecteur, du fait des cascades électromagnétiques provoquées par le passage des particules incidentes, il y a création de neutrons de faible énergie et de photons. La plupart des photons sont rapidement réabsorbés dans le matériau, une minorité d'entre eux se converti en électrons et positrons. Les neutrons vont se disperser et être éventuellement captés, produisant à leur tour d'autres photons. Les constantes de temps de ces divers processus sont supérieures à la cadence de production de ces produits secondaires, ainsi il y a création d'un gaz pratiquement uniforme et isotrope constitué de particules de faible énergie.

A ce bas niveau d'énergie radioactive, le silicium subit des dégradations importantes. Dans le tracker, en particulier, si les capteurs silicium, comme l'électronique de lecture, n'étaient pas protégés, leur durée de vie dans un tel environnement serait trop courte. Etant donné que la majorité des neutrons est créée par interaction hadronique dans le calorimètre électromagnétique, un modérateur peut être introduit entre la partie "Tracker" et la partie "ECAL". Le but est de réduire l'énergie des neutrons d'albedo d'environ 1 MeV à 100 keV. Les neutrons d'énergie inférieure à 100 keV sont beaucoup moins nuisibles au silicium. La manière la plus efficace de ralentir les neutrons est de

favoriser leur diffusion élastique dans des atomes d'hydrogène. Dans les bouchons, un modérateur constitué par une structure alvéolaire en aluminium, dans laquelle est injecté un gel de paraffine, est placé de part et d'autre du Preshower. Ainsi le tracker est protégé du ECAL par 2 modérateurs, tandis que le Preshower n'est protégé que par un seul. La fluence neutronique est maximale à $\sim 7 \times 10^{14}$ n cm^{-2} dans le centre du ECAL ; elle est réduite à 1.8×10^{14} n cm^{-2} à $\eta = 2.6$ dans le Preshower et à $\sim 5 \times 10^{13}$n cm^{-2} dans le tracker.

- Les figures 2.2 à 2.7 présentent la dose cumulée et la fluence neutronique en différents points de CMS.
- Les tableaux 2.1 à 2.4 résument les doses cumulées et les fluences (neutrons et hadrons chargés) dans les 4 sous détecteurs Pixel, Tracker, Preshower et ECAL.

Section 2.2 Effets des irradiations sur les composants électroniques.

Dans le silicium, les dégradations cumulatives dues aux irradiations peuvent être classées en 2 types: les effets en surface et les effets en volume (bulk). Les effets transitoires singuliers ("single event") constituent un troisième type d'effet, bien différent, qui est causé par la déposition brutale et localisée de charges. Cette section présente les 3 différents phénomènes et illustre leurs effets sur les caractéristiques des transistors MOS et bipolaires.

Les effets en volume sont la conséquence de dislocationss de la structure cristalline du silicium, causées par des collisions entre particules de forte énergie et des atomes de silicium. Dans le LHC, les particules majoritairement responsables de ce type de dislocation seront les neutrons, les protons et les pions. Quand une telle particule percute un atome de silicium, il est éjecté de son réseau cristallin, laissant derrière lui une place vacante. Si suffisamment d'énergie cinétique est transfèrée, l'atome de recul peut à son tour bousculer des atomes et créer ainsi une réaction en cascade. Ces atomes déplacés prennent, le plus souvent, des positions quelconques dans le réseau cristallin créant ainsi des défauts qui ont pour effet l'apparition de niveaux d'énergie intermédiaires dans la bande interdite du silicium. D'autres types de défauts peuvent induire des courants de fuite entre composants, réduire la durée de vie des porteurs minoritaires ou modifier le profil de dopage des jonctions.

Le transistor bipolaire est particulièrement sensible aux effets en volume. Le gain en courant (β), d'un transistor bipolaire, est directement proportionnel à la durée de vie des porteurs minoritaires présents dans la base (τ_b). Une diminution de la durée de vie des porteurs, causée par recombinaison de charge, va donc dégrader β.

Les effets dits de surface sont attribués à la présence de défauts à l'interface entre le silicium (Si) et l'oxyde (SiO_2). Ces défauts créent des piégeages dans cette région. Les transistors MOS sont particulièrement sensibles à ces effets. D'une part, les charges piégées à l'interface Si/SiO_2 altèrent la tension de seuil du transistor (V_t), d'autre part des porteurs majoritaires, présents près de la surface du canal, sont capturés par les pièges d'interface. Ce deuxième effet altère à la fois la tension de seuil du transistor et la mobilité des porteurs minoritaires (μ).

Le piègeage de charges dans l'oxyde est par ailleurs favorisé par les radiations ionisantes qui produisent en quantité des paires électron/trou dans l'oxyde. Les électrons libres sont beaucoup plus mobiles que les trous dans l'oxyde de silicium. Ceux d'entre eux qui ne se recombinent pas instantanément sont happés par le champ électrique en direction de l'électrode positive (la grille pour un MOS N) en quelques pico secondes. Les trous, quant à eux, se déplacent vers l'électrode négative avec une constante de temps de l'ordre de la seconde. Une irradiation continue provoque donc une accumulation de charges positives dans l'oxyde. Quelques-uns de ces trous vont éventuellement recombiner et d'autres seront capturés par des piéges présents dans l'oxyde.

La quantité de charge piégées dans l'oxyde dépend fortement de l'épaisseur de l'oxyde de grille. Dans les transistors MOS, aux frontières de l'oxyde mince, l'épaisseur d'oxyde s'accroît progressivement pour rejoindre l'épaisseur de l'oxyde de champ. Ces zones, plus connues sous le nom de 'bec d'oiseau', sont une source de piégeage prépondérante dans le MOS. Il en résulte un courant de fuite entre drain et source qui peut devenir significatif. Tout se passe comme si des transistors parasites, avec une tension de seuil réduite, étaient connectés en parallèle du composant principal.

Les effets singuliers ("Single Event Effects": SEE) sont dus à l'apport soudain de charges dans le silicium, causé par l'ionisation d'une particule chargée incidente. L'amplitude de l'ionisation est déterminée par la puissance d'arrêt des particules ("Linear Energy Transfer": LET). Des particules à grands LET peuvent produire un plasma très dense de trous et d'électrons, focalisé en une région du silicium, réduisant ainsi localement la résistivité. Ce mécanisme peut, par exemple, déclencher l'amorçage de structures thyristors parasites (ou 'Silicon Controlled Rectifier' : SCR) qui drainent alors un courant incontrôlé entre les alimentations d'un circuit intégré ("latchup"). Si un tel dépôs de charge se situe en une région du circuit où sont implantées des fonctions logiques, il peut provoquer un changement d'état dans les bascules ("Single Event Upset": SEU). Alors que les effets "SEU" se traduisent par des disfonctionnements temporaires dans un circuit, le "latchup" peut entraîner sa destruction.

- La figure 2.9 montre comment se créent des défauts à l'interface Si/SiO_2 par la présence d'impuretés ou par connexions pendantes.

- La figure 2.10 représente la vue en coupe et les diagrammes des bandes d'une capacité MOS. Elle illustre le processus d'ionisation à l'interface Si/SiO_2, la production d'électrons et de trous et, comment les électrons sont capturés rapidement par l'électrode positive, tandis que les trous, très lents, restent piégés dans l'interface.

- La figure 2.11 présente la vue en coupe d'un transistor MOS de type N en particulier la formation du canal de conduction sous la grille.

- L'équation 2.3 montre la contribution des charges piégées dans l'oxyde dans la modification de la tension de seuil du transistor. Dans un MOS N, alors que la quantité de charge piégée dans l'oxyde augmente, la tension de seuil diminue (figure 2.12).

- La figure 2.13 montre que le piégeage de charges est accentué dans les régions 'becs d'oiseaux'. C'est ici le siège d'un courant de fuite drain/source.

- La figure 2.14 illustre le fonctionnement d'un transistor bipolaire. Les équations 2.4 à 2.6 établissent la relation entre le gain en courant (β) et la durée de vie des porteurs (τ_b) dans la base.

- La figure 2.15 présente la façon de dessiner un transistor bipolaire pour minimiser la dégradation du β. Il faut réaliser une structure verticale présentant une largeur de base minimale.

- Les figures 2.16 et 2.17 montrent comment des effets en surface peuvent provoquer des courants de fuite entre composants.

- La figure 2.18 donne des valeurs de "LET" types (indispensable pour estimer les probabilités de défaillance de type "SEE") pour différents ions. Ces valeurs augmentent avec le numéro atomique.

- La figure 2.19 montre comment un entonnoir d'électrons et de trous peut-être créé par une particule de grande énergie percutant une région du silicium.

- La figure 2.20 montre le mécanisme de verrouillage ("latch up") d'une structure "SCR" parasite dans une technologie CMOS.

Section 2.3 Technologies tolérantes aux radiations, options et choix.

Cette section passe en revue les principales tendances technologiques de ces 10 dernières années sur le segment des filières tolérantes ou durcies aux radiations. Trois principaux types de technologie sont présentés: Silicium couche mince sur isolant (SOI), silicium couche épaisse sur isolant et les technologies submicroniques modernes. Tandis que les deux premiers types de technologie ont été développés pour les marchés spécifiques des composants utilisés en environnement radioactif, le dernier type concerne les technologies modernes destinées aux marchés grand public, gros volumes et à très grande densité d'intégration. La qualité des matériaux et la finesse des procédés de réalisation de ces technologies submicroniques leur confèrent des propriétés remarquables quant à la tolérance aux radiations.

Les technologies SOI offrent la possibilité d'isoler complètement les transistors N des transistors P, ce qui permet d'éviter la création de structures parasites sensibles au phénomène de "latchup". Le matériaux de départ, dans ces technologies, est un wafer en SIMOX produit par implantation d'ions d'oxygène, pour former une couche d'oxyde enterrée. La couche de silicium située au dessus de cet oxyde est utilisée pour implanter les composants alors que le silicium situé au dessous joue le rôle de substrat isolant (report mécanique).

Les courants de fuite, le long des 'becs d'oiseau', peuvent être réduits par des dessins particuliers de transistor. La nature de la technologie SOI apporte aussi des complications en même temps que des avantages. L'effet 'Kink' dans le drain par exemple: augmentation soudaine du courant drain/source (I_d) en zone de saturation, à tension V_{gs} fixe, phénomène due à des piégeages de charges dans le caisson. Ce phénomène peut être corrigé par l'addition de contacts dans le caisson afin d'en abaisser

l'impédance. Mais, en résolvant le problème de cette façon on provoque une remontée dans le spectre de bruit.

Les technologies SOI couches épaisses, utilisent également des tranches en SIMOX, mais l'implantation de l'oxyde enterré y est plus profonde, dégageant ainsi une épaisseur de silicium utile supérieure. La filière DMILL est un exemple de technologie SOI couche épaisse. Les composants sont implantés sur le silicium supérieur et demeurent très éloignés de l'oxyde enterré. L'isolation latérale entre composants est réalisée au moyen de tranchées verticales, isolées des composants par un diélectrique. Combinée avec l'isolation verticale par l'oxyde enterré, cette isolation latérale supprime l'existence de structures "SCR" parasites. Il s'agit d'une technologie BICMOS 0.8 μm avec un oxyde de grille d'une épaisseur de 18 nm. La tenue aux radiations de la technologie spécifiée par le producteur est la suivante :

- Evolution de la tension de seuil des MOS : $\Delta V_{tn} < -90$ mV et $\Delta V_{tp} < -130$ mV à 10 Mrad
- Evolution de la transconductance des MOS : $\Delta g_{mn} = -25\%$ et $\Delta g_{mp} = -6\%$ à 10 Mrad
- Evolution du gain en courant des transistors NPN (PNP inexistant dans la technologie) à $I_c = 100$ μA.: $\Delta\beta = -15\%$ à 10 Mrad et $\Delta\beta = -35\%$ à 1×10^{14} ncm^{-2}.

Les deux mécanismes principaux, responsables de la dégradation des caractéristiques des MOS soumis a des radiations, sont le piégeage de charges dans les oxydes (oxyde de grille et LOCOS) et la création d'états d'interface. Il paraît assez logique de penser qu'en diminuant l'épaisseur de l'oxyde de grille, on va diminuer le volume de charges piégeables et donc obtenir une dérive moindre de la tension de seuil. Ce qui paraît moins logique, c'est de constater comme il l'a été prouvé par Saks et al., que l'amélioration résultante n'est pas linéaire. En étudiant la quantité de charges piégées en fonction de l'épaisseur d'oxyde (t_{ox}), en mesurant la tension de bande plate (V_{fb}), Saks montra que pour des épaisseurs d'oxyde $t_{ox} > 20$ nm, $\Delta V_{fb} \propto t_{ox}^2$, tandis que pour des épaisseurs d'oxyde <10 nm, le V_{fb} est de plusieurs ordres de grandeur inférieure à la variation prédictible. Des études ultérieures sur les états d'interface dans les technologies à très faible épaisseur d'oxyde ont montré des résultats similaires. L'explication admise est que, dans le cas d'oxyde très minces, les électrons et les trous, présents transitoirement dans l'oxyde, sont directement collectés par effet tunnel dans la bande de valence du polysilicium de grille ou dans celle du silicium du caisson. Il a donc prédit, à cette époque, que les technologies futures avec des oxydes de grilles <10 nm seraient naturellement résistantes aux radiations.

Aujourd'hui les technologies CMOS courantes présentent une longueur de grille de $\sim$0.25 μm, voire moins. L'épaisseur d'oxyde de grille se situe autour de $\sim$5 nm, donc dans la zone où la tension de bande plate V_{fb} est minimale.

Une étude de résistance aux radiations de ces technologies submicroniques a été initiée au CERN. Les résultats obtenus sont particulièrement intéressants :

- Evolution de la tension de seuil des MOS : ΔV_{tn} =15 mV et ΔV_{tp} =-30 mV à 10 Mrad
- Evolution de la tension de seuil des MOS : ΔV_{tn} =35 mV et ΔV_{tp} =-70 mV à 30 Mrad
- Evolution de la transconductance des MOS : $\Delta g_{mn} = -6\%$ à 30 Mrad
- Evolution du bruit : +15% (NMOS) et +7% (PMOS) à 100 Mrad(Si)
- La figure 2.21 illustre la réalisation des composants CMOS à partir d'un substrat SIMOX.
- La figure 2.22 présente les modifications à apporter au dessin des transistors pour supprimer l'effet 'Kink' et, sa contrepartie en figure 2.25 (remontée dans le spectre de bruit).
- La figure 2.24 illustre l'effet 'Kink' associé aux transistors SOI à caisson flottant.
- La figure 2.26 est une vue en coupe de la technologie DMILL.
- Les figures 2.27 et 2.28 montrent l'évolution de la tension de bande plate et l'évolution de la densité des états d'interface dans une capacité MOS en fonction de la dose d'ionisation. Ces courbes expliquent pourquoi les technologies submicroniques, avec des épaisseurs d'oxyde de grille <10 nm, présentent une dérive de tension de seuil très faible.

Dans le projet Preshower, la stratégie adoptée pour le développement de PACE a résidé en 2 étapes : Dans un premier temps, validation de l'architecture du circuit (PACE1, technologie non durcie aux radiations, Mietec 0.7 μm CMOS); puis, dans un deuxième temps, portage de cette architecture sur une technologie durcie (PACE2, technologie DMILL 0.8 μm BICMOS). La technologie DMILL a été retenue, à cette époque, parce qu'il s'agissait de la seule technologie durcie validée, disponible, présentant un niveau de résistance aux radiations compatible avec les exigences du Preshower.

Par la suite, la très bonne tenue des technologies submicroniques a été démontrée. Aujourd'hui, le portage de PACE2 sur une technologie submicronique (CMOS 0.25 μm) peut être envisagé (PACE3). Cette éventualité dépendra, en partie, des résultats de test de PACE2 après irradiations. Ces tests n'ont pas encore été effectués à ce jour.

Chapitre 3 : PACE1

PACE1 a été le premier ASIC développé pour le Preshower. Ce circuit, développé dans une technologie bulk CMOS 0.7 μm, est constitué d'une mémoire analogique à intégration de courant. Les motivations pour ce premier développement étaient de valider l'architecture du circuit et de permettre la réalisation d'un système électromécanique complet (prototype démonstrateur de Preshower) utilisable en faisceau test. Certaines spécifications du tableau 1.6 étaient relâchées comme la dynamique d'entrée (abaissée

à 250 MIPs au lieu des 400 nécessaires). PACE1 n'était pas durci contre les radiations ni pourvu d'une interface de communication conviviale, ces deux évolutions étant prévues pour PACE2 (chapitre 5).

Section 3.1 L'architecture de PACE1

PACE1 comporte 32 voies actives de lecture plus 4 voies "dummy". Chaque voie est composée d'un préamplificateur avec compensation de courant de fuite capteur, d'un amplificateur d'écriture, d'une succession de capacités commandées par des interrupteurs MOS et d'un amplificateur d'écriture. En aval, un multiplexeur analogique sérialise les différents canaux à la cadence de 20 MHz. La longueur de la matrice de capacités est conforme au tableau 1.6 (160 colonnes) mais la taille réduite de la pile FIFO autorise la consignation de 4 événements (LV1) seulement. La polarisation des fonctions analogiques est assurée par des DAC internes adressables extérieurement.

La charge en provenance du capteur est convertie par le préamplificateur en une impulsion de courant proportionnelle à la quantité de charge. Le courant de sortie du préamplificateur est alors intégré dans une capacité de la matrice mémoire connectée en contre réaction sur l'amplificateur d'écriture. En cycle de lecture, la charge de cette capacité est reconvertie en tension. L'image de la charge totale collectée par le capteur est obtenue en additionnant la charge de trois cases mémoires consécutives. Cette architecture était extrêmement intéressante pour le Preshower dans la mesure où elle autorise une reconstruction aisée de la charge. En outre la précision de reconstruction est insensible aux battements d'horloge (jitter et bruit de phase).

Le préamplificateur utilisé dans PACE1 est connu sous l'appellation FCICON, il est basé sur le principe du convoyeur de courant. Il se caractérise par une impédance d'entrée très faible, une impédance de sortie élevée, et une réponse linéaire de 1 à 300 MIPs en entrée (soit une charge de 4 fC à 1.2 pC).

- La figure 3.1 montre le schéma synoptique d'une voie analogique complète. La figure 3.2 illustre le principe de l'intégration de charge dans 3 capacités de la mémoire analogique.
- La figure 3.3 montre un schéma synoptique du circuit PACE1.
- La figure 3.4 montre le principe de construction du signal de sortie: dans ce cas, sérialisation de 3 colonnes avec un signal sur la ligne 5.
- La figure 3.5 présente le synoptique du préamplificateur FCICON. Les équations des impédances d'entrée et de sortie sont données en équation 3.1 et 3.2.
- La figure 3.6 présente le modèle de bruit du préamplificateur FCICON. Les équations 3.3 à 3.8 donnent les composantes de bruit série et parallèle, on aboutit à un bruit de 3250 e + 29 e/pF .

Section 3.2 Résultats de mesure de PACE1

PACE1 a démontré un fonctionnement correct et conforme à celui attendu dans pratiquement toutes les fonctions de contrôle (séquenceur, sérialiseur, FIFO, multiplexeur, DAC, interfaces LVDS, calibration autonome, espacement programmable des

pointeurs d'écriture et de lecture, programmation du nombre de points consignés par déclenchement). Le codeur de colonne a présenté, en revanche, un disfonctionnement à 40 MHz avec pour conséquence des marquages erratiques dans la FIFO. La fréquence d'horloge à partir de laquelle ce disfonctionnement est apparu est de 33 MHz. Le sous dimensionnement d'un transistor dans l'encodeur était à l'origine de cette anomalie. PACE1 était donc limité à une fréquence d'horloge de 33 MHz. La gamme dynamique a été explorée de 1 à 250 MIPs. Le gain de conversion présente une évolution de 6 mV/MIP à 4.5 mV/MIP sur l'étendue de mesure.

L'évolution de la ligne de base (piédestal) d'un point à l'autre de la mémoire est un paramètre très important pour le Preshower dans la mesure où le gain de la chaîne demeure faible (pour accepter une grande dynamique). Un gain faible signifie que les perturbations transitoires, que peuvent subir les échantillons stockés en mémoire, vont contribuer pour une part importante au bruit global du système. La variation de piédestal est la déviation standard mesurée sur les échantillons d'un même canal (σ_{ped}). L'observation du piédestal de PACE1, en l'absence de signal d'entrée, en appliquant uniquement des commandes d'accès récurrentes dans la mémoire, a révélé des fluctuations importantes. Ces fluctuations, synchrones des commandes d'accès délivrées par le séquenceur ont été attribuées à des perturbations induites par des couplages de charges dans le substrat entre les parties digitales et la mémoire analogique.

Pour que ces charges puissent remonter dans le canal analogique cela suppose qu'il existe quelque part dans la chaîne un noeud sensible présentant une impédance relativement élevée et une capacité par rapport au substrat importante. La sortie du préamplificateur FCICON est justement un noeud sensible de ce type. Ce préamplificateur possède une sortie en courant (donc haute impédance), et il est chargé par le bus d'écriture (capacité parasite importante avec le substrat). Pour vérifier cette hypothèse une rangée de la mémoire a été rendu accessible de l'extérieur de l'ASIC au moyen de connexions déposées par FIB (focus ion beam). Sur cette rangée particulière de la mémoire un driver d'écriture avec sortie basse impédance a été câblé et les mêmes stimulis de test ont été réinjectés. Les résultats de test n'ont plus révélé, dans ce cas, de fluctuations de piédestal synchrones des signaux logiques du séquenceur.

PACE1 a permis de construire un prototype électromécanique du Preshower utilisable en faisceau test, mais les résultats de mesures ont montré la nécessité de modifier l'architecture analogique dans un redesign ultérieur, afin de rendre la mémoire analogique beaucoup moins sensible aux perturbations du substrat.

- La figure 3.13 montre le dessin physique de PACE1.

- La figure 3.14 montre l'acquisition d'un signal de 100 Mips distribué en trois tranches de temps et la figure 3.15 montre la gamme dynamique de 250 Mips.

- Les figures 3.16 et 3.17 montrent les modifications de connexion réalisées par FIB (Focused ion beam): rajout de plots pour accéder directement à une rangée de la mémoire. La figure 3.18 montre la réduction de fluctuation de piédestal après l'intervention FIB, confirmant que la sortie de FCICON est particulièrement sensible à la collection de charges parasites.

Section 3.3 Le prototype Preshower et les résultats de test en faisceau.

En 1999 un prototype démonstrateur de Preshower a été réalisé. Le but de cette réalisation était de placer ensemble dans un faisceau test d'électrons un prototype Preshower (incluant les absorbeurs, les capteurs silicium, l'électronique et le système de refroidissement) et un prototype ECAL. Ce prototype Preshower était constitué de 2 plans d'absorbeurs (construits par un empilement acier/plomb/acier) chacun équipé d'une matrice de 2×2 micro-modules. Chaque micro-module contenant un détecteur silicium et un circuit PACE1. L'orientation des micro-modules était telle qu'ils étaient tournés de 90 degrés d'un plan à l'autre. Chaque matrice était recouverte par une carte mère contenant 4 ADC et l'électronique logique de contrôle.

Le prototype Preshower était placé devant un prototype ECAL dans une ligne de faisceau d'électrons. Le prototype Preshower était orientable grâce à un pivot situé dans un des angles pour permettre de modifier son inclinaison par rapport au faisceau et par rapport à l'orientation des cristaux. De cette manière il était possible d'explorer toutes la gamme des valeur de η.

La mesure de l'énergie déposée dans les deux plans de Preshower (E_1 et E_2) pour une énergie de faisceau donnée s'est montrée conforme à celle prédite par les simulations. L'énergie mesurée par le Preshower a donc été ajoutée à celle mesurée par le prototype ECAL dans un groupe de 9 cristaux. La distribution des énergies mesurées à 180 GeV a été comparée avec et sans la contribution du Preshower. La distribution des mesures ECAL seules donne un $\sigma = 1.15\%$ tandis qu'en ajoutant la contribution du Preshower $\sigma = 0.62\%$.

Tous les résultats concordent avec les prédictions issues de la simulation. Ceci permet donc de confirmer les choix faits jusqu'ici dans le développement hardware et de valider la modélisation du Preshower utilisée dans les simulations.

- Les figures 3.19 et 3.20 sont des photos montrant les micro-modules du prototype Preshower comportant les détecteurs silicium et les puces PACE1.

- La figure 3.21 montre une vue de dessus du prototype Preshower et la figure 3.22 une vue de face avec en arrière plan le prototype ECAL.

- La figure 3.23 montre comment le Preshower peut être orienté d'un angle variable par rapport à l'axe du faisceau et l'orientation des cristaux pour couvrir différents η.

- La figure 3.25 compare les énergies mesurées dans les deux plans de détecteurs à celles obtenues par simulation.

- L'équation 3.11 donne la résolution en énergie mesurée par les cristaux ECAL seuls, on remarque un terme stochastique (4.1%) et un terme de bruit (0.25%). Les équations 3.13 et 3.14 montrent comment l'énergie totale est calculée à partir des mesures issues du Preshower et du ECAL.

- La figure 3.27 montre les mesures d'énergie obtenues avec le détecteur ECAL seul, comparées à celles obtenues avec ECAL + Preshower. Les figures 3.28 et 3.29 retracent la résolution en énergie du Preshower à différents angles.

Chapitre 4 : Echantillonnage en tension - Développement de Delta et DeltaStream.

Ce chapitre présente une évolution majeure de PACE dans l'architecture de traitement analogique; on passe d'une architecture à intégration de courant (PACE1) à une architecture à tension échantillonnée. La motivation essentielle de cette évolution était la nécessité d'abaisser l'impédance de sortie du driver d'écriture, afin de diminuer la sensibilité de ce noeud aux charges impulsionnelles provenant du substrat. Ce chapitre est en 4 parties. La première partie concerne la reconstruction de charge à partir d'échelons de tension, la seconde explore différentes architectures de circuit, la troisième présente en détail l'architecture retenue (Delta) et la quatrième présente un circuit multivoies construit autour de Delta.

Section 4.1 Reconstruction de charge.

L'intégration de courant était initialement choisie pour sa simplicité vis à vis de la reconstruction de charge (sommation des charges de trois échantillons) et pour sa robustesse aux battements d'horloge (phase et jitter). Ce paragraphe explore les limitations de la méthode de reconstruction de charges à partir d'échantillons de tension.

Une approche largement répandue dans la physique des hautes énergies, pour réaliser la conversion charge/tension, consiste en un amplificateur de charge suivi par un filtre de mise en forme du signal ("shaper"). La charge collectée par le capteur (Q) est stockée dans la capacité de contre réation (C_f) d'un préamplificateur de charges. L'étage de mise en forme qui suit permet de reduire la bande passante de bruit et assure un retour du signal à zéro. La fonction de transfert établie dans ce paragraphe repose sur un filtre de second ordre de type $CR - RC^2$.

Le Preshower doit être capable de déterminer le positionnement temporel des signaux détectés, ainsi que leur amplitude (V_p), ($Q \propto V_p$). Une technique de déconvolution peut être utilisée, en prenant trois échantillons de tension seulement, séparés de 25 ns, pour obtenir la résolution temporelle. Elle convient également pour la reconstruction de charge mais peut être entachée d'erreurs significatives si le signal subit quelques dérives (forme et décalage temporel).

Dans le Preshower il est prévu d'utiliser cette technique pour le comptage du nombre d'événements. Pour s'approcher au mieux de la reconstruction de charge optimale, un ensemble de poids optimaux est recherché en utilisant la loi de régression du χ^2.

Dans une étude de cette technique, avec pour hypothèse un bruit majoré de 0.25 MIP, une variation de phase de +/- 2ns et un jitter de +/- 0.5ns sur un échantillon, la précision de la reconstruction de charge est meilleure que 1%. Alors qu'avec la méthode de déconvolution directe on aboutirait à une imprécision de 10%.

- La figure 4.1 montre le schéma synoptique d'un amplificateur de charge suivi d'un filtre $CR - RC^n$.
- Les équations 4.1 à 4.3 établissent la fonction de transfert du circuit dans le domaine fréquentiel puis dans le domaine temporel.

- La figure 4.2 montre le signal $V_{o(t)}$ avec la position des instants d'échantillonnage.
- Les équations 4.5 à 4.7 représentent le fonctionnement de la technique de déconvolution pour la résolution temporelle, et l'équation 4.8 pour la résolution en charges.

Section 4.2 Architecure de la Chaîne de lecture.

L'électronique de lecture (spécifications du tableau 1.6) doit présenter 2 gains distincts pour garantir une résolution optimale dans les 2 gammes dynamiques d'entrée spécifiées (1-400 MIPs en mode acquisition, et 0.1-50 MIPs en mode calibration). Il faut donc considérer un mode fort gain (HG) en mode calibration et un mode gain réduit (LG) en mode acquisition.

Trois versions différentes de système à 2 gains ont été conçues et réalisées en DMILL sur un circuit test: une chaîne de lecture double (une sortie HG, une sortie LG); un préamplificateur de charge suivi d'un shaper à gain commutable (HG/LG); et un préamplificateur à transimpédance suivi également d'un 'shaper' à gain commutable (HG/LG). Les avantages et les inconvénients de chacune de ces solutions sont discutés dans cette section. Ces trois solutions techniques permettent de satisfaire les exigences du tableau 1.6, mais la préférence a été portée sur la deuxième solution; sa constitution est détaillée dans la section 4.3.

- La figure 4.3 montre les trois architectures de système à double gain qui ont été envisagées pour PACE.

Section 4.3 Delta.

Le nom qui a été attribué au système frontal de lecture (préamplificateur de charge + shaper à gain commutable) est "Delta". Cette section décrit en détail la conception et les résultats de mesure de Delta.

Le préamplificateur Delta est composé d'un étage d'entrée BICMOS de type cascode replié. Un étage source suiveuse recopie la tension de l'étage cascode sur la sortie. La capacité de contre réaction assure le stockage de la charge. Cette charge stockée décroit lentement à travers une résistance de contre réaction, assurant ainsi un retour du circuit à son point de repos. Le point de repos est choisi de façon à maximiser la dynamique de sortie.

La compensation de courant de fuite capteur (LCC) est assurée par un OTA doté d'une très faible bande passante, connecté en contre réaction sur le préamplificateur. Ce circuit détecte les variations lentes sur la sortie du préamplificateur et corrige la dérive constatée en absorbant le courant de fuite du capteur. Il dispose, par ailleurs, d'une tension de consigne programmable qui permet d'ajuster la gamme dynamique admissible.

Le shaper $CR - RC^2$ comporte deux gains. Pour augmenter le gain une capacité additionnelle est commutée en parallèle sur la capacité série ($C_c s$). Afin de ne pas présenter un peaking time dont la valeur dépendrait de la valeur du gain, un dispositif, commandé par la commande de changement de gain, modifie la transconductance gms du shaper en conséquence. Ainsi le ratio $\frac{g_m s}{C_c s + C_f s}$ demeure constant.

Les résultats de mesures effectuées sur les deux gains, présentent un peaking time quasi invariant de ∼25 ns et un temps de montée constant sur toute la gamme dynamique . Les gammes dynamiques sont respectées, c'est à dire, 50 MIPs en mode HG et 400 MIPs en mode LG, avec des gains correspondants de 30 mV/MIP et 4 mV/MIP respectivement. Pour vérifier l'absence d'effet d'empilement un signal de 20 MIPs a été injecté à une fréquence de 5 MHz; aucun effet de saturation n'a été observé sur l'électronique dans ces conditions. A noter que les simulations Pythia montrent un effet d'empilement maximal prévisible dans le Preshower à 2 MIPs et 2 MHz. Le gain demeure constant pour un courant de fuite capteur allant jusqu'a 150 μA (pour 20 μA spécifiés).

Les expressions relatives au bruit sont établies dans ce paragraphe, elles montrent la prépondérance de la contribution du transitor d'entrée, et les implications sur son dimensionnement. Le bruit série s'avère proportionnel à la résistance de base, qui est elle même, inversement proportionnelle à la surface d'émetteur. Le bruit parallèle est inversement proportionnel au β, lequel diminue sous l'effet du rayonnement d'autant plus fortement que sa surface d'émetteur est grande. Le dimensionnement de la surface d'émetteur résulte alors d'un compromis entre bruit optimum avant et après irradiations. Différentes tailles de transistors ont été expérimentées sur différents canaux du circuit test pour trouver les choix optimaux. Des transistors isolés de différentes tailles ont également été expérimentés sur ce circuit test pour tracer la courbe de dégradation du β en fonction de la dose d'irradiation.

Le bruit mesuré avant irradiation, en mode HG, présente une ENC moyenne de 640 e + 33 e/pF, et confirme l'augmentation du bruit série des canaux possédant des transistors d'entrée de taille réduite.

A la suite de ces mesures, 2 circuits ont été exposés jusqu'a 10 Mrads(Si) et 2 autres ont été exposés à une fluence neutronique de 4×10^{13} ncm^{-2}. Seul un effet sur le gain de la chaîne a été observé: l'exposition aux radiations ionisantes provoque une augmentation de gain de l'ordre de 17% tandis que la fluence neutronique provoque une diminution de l'ordre de 14%. La diminution du gain de la chaine est due à la diminution du β et aurait donc du se manifester dans les deux types d'exposition. En réalité, des mesures effectuées sur des composants isolés ont permis d'établir qu'une variation importante (+50%) de la résistance de contre réaction (R_f) du préamplificateur était responsable de l'augmentation apparente du gain de la chaîne sous radiations ionisantes. Le type de résistance employé (DMILL RHV), s'avère être un composant à utiliser avec précaution dans la conception de circuit durcis.

Les bruits mesurés après irradiation montrent des différences sensibles d'une chaîne à l'autre et par rapport aux mesures effectuées avant irradiation. En l'occurrence, on observe des dégradations de β supérieures à 50% sur les transistors de grosse géométrie. Ces résultats ont permis d'identifier une taille d'émetteur optimale garantissant un niveau de bruit minimal du préamplificateur sur toute la durée de vie de l'expérience CMS.

- Les figures 4.4 à 4.8 présentent les schémas du préamplificateur Delta, du circuit de compensation de courant de fuite, et du shaper à gain commutable. Les équations

4.9 et 4.10 établissent les critères à respecter pour égaliser les “peaking time” dans les deux cas de gains (HG/LG).

- La figure 4.9 et les équations 4.11 et 4.18 établissent les équations qui déterminent le bruit du circuit. On peut remarquer qu'il exite une surface d'émetteur optimale conduisant à un bruit minimal après irradiation.

- La figure 4.10 montre le signal de réponse mesuré pour chacun des gains.

- Les figures 4.11 et 4.12 montrent l'invariance du temps de montée en fonction du signal d'entrée.

- Les figures 4.13 et 4.14 montrent les fonctions de transfert obtenues dans les deux modes (∼30 mV/MIP en mode HG, ∼4 mV/MIP en mode LG).

- La figure 4.15 montre le gain normalisé en fonction du courant de fuite capteur.La figure 4.16 montre le bruit (en ENC) en fonction de la capacité du capteur; il s'établit à 640 e + 33 e/pF.

- Les figures 4.17 à 4.22 montrent les performances obtenues après irradiation: signal de sortie de Delta, β en fonction du courant Ic, et bruit en fonction de la géométrie des transistors.

Section 4.4 Circuit DeltaStream.

Les capteurs silicium du Preshower seront fabriqués dans 4 centres différents. Chacun de ces centres aura en charge la production et le test d'une partie des capteurs silicium ainsi que l'assemblage d'une partie des micro-modules. Afin d'obtenir la plus grande cohérence possible dans les méthodes de test, entre ces 4 centres de production, un banc de test commun est en cours de développement. Ce système de test comporte en outre un laser qui permet d'exciter individuellement chacune des pistes d'un capteur.

L'électronique de ce banc de test doit présenter des caractéristiques analogiques similaires au circuit PACE2. PACE2 pourrait, lui même, être utilisé mais sa complexité et sa mise en oeuvre son mal adaptées à un tel système. Pour cette raison, un circuit simplifié, baptisé “Deltastream”, a été développé en technologie DMILL.

Le circuit DeltaStream comporte 36 canaux de lecture constitués chacun d'un préamplificateur + shaper (identiques à Delta) et d'un étage échantillonneur-bloqueur. Un multiplexeur de sortie, suivi d'un buffer, permet de sérialiser la lecture des 36 canaux en une seule trame de valeurs analogiques.

La conception de l'étage échantillonneur-bloqueur est décrite dans ce chapitre ainsi que le multiplexeur fonctionnant à 20MHz. Pour pouvoir passer toute la dynamique en sortie, ce multiplexeur utilise des 'switch' MOS complémentaires (N + P), qui présentent ainsi une résistance (R_{on}) à l'état passant quasi indépendante du signal.

Les résultats de mesures obtenus sur DeltaStream sont analogues à ceux obtenus sur Delta en ce qui concerne la mise en forme des signaux. D'autres performances,

particulièrement déterminantes pour le design de PACE2, ont été mesurées sur DeltaStream comme les dispersions entre canaux (tension de repos, gain, bruit) ou l'influence du multiplexeur sur la gamme dynamique admissible.

Les mesures de la valeur de repos des 36 canaux présentent une courbe de dispersion en cloche. La dispersion min/max est de 91 mV en mode LG et 69 mV en mode HG. L'explication la plus probable de ce profil en cloche est une variation progressive de la tension d'alimentation d'un canal à l'autre. Dans la mesure où le rail d'alimentation alimente verticalement les canaux, et où il est connecté à l'alimentation analogique à la fois par le haut et par le bas, la région où la chute de tension est la plus forte se trouve être le centre. La dispersion de gain d'un canal à l'autre a été estimée (déviation standard autour de la moyenne) à $\sim$ 100 μV en mode LG et $\sim$1 mV en mode HG.

Les performances en bruit ont été mesurées, sur chaque canal, en mode HG; l'interpolation linéaire des résultats sur l'ensemble du circuit donne un ENC=676 e + 28 e/pF. Les relevés de linéarité effectués avec le multiplexeur positionné soit en statique ou bien opérant à 20 MHz, ne présentent pas de différence observable.

- La figure 4.24 montre le schéma synoptique du circuit DeltaStream.
- La figure 4.25 présente les schémas de l'échantillonneur-bloqueur et du multiplexeur, et la figure 4.30 montre le dessin physique du circuit DeltaStream.
- Les figures 4.31 à 4.33 décrivent la mise en oeuvre et les différents modes de fonctionnement de DeltaStream.
- Les figures 4.34 à 4.37 donnent les résultats de mesures de DeltaStream: signaux de sortie, temps de montée, niveaux DC, linéarité et bruit, dispersions entre canaux.
- Le tableau 4.3 résume les résultats de mesure.

Chapitre 5 : PACE2

PACE2 représente le système de lecture frontal du Preshower, il couvre l'ensemble des spécifications du tableau 1.6. Il associe le circuit Delta (chapitre 4) à une mémoire analogique à tension échantillonnée. PACE2 est divisé en deux ASICs distincts afin d'isoler les préamplificateurs de charge des fonctions numériques qui contrôlent les cycles d'écriture/lecture dans la mémoire analogique. Le circuit comportant les amplificateurs de charge est appelé Delta et le circuit comportant la mémoire analogique est appelé PACE-AM.

Ce chapitre présente, dans un premier temps, comment PACE2 est intégré dans l'ensemble électronique du Preshower, puis une grande partie est dédiée à la conception de la mémoire analogique et aux fonctions de calibration internes.

Section 5.1 L'électronique du Preshower

La chaîne d'acquisition commence par les capteurs silicium. Chaque micro-module contient un capteurs silicium (32 voies) et les deux ASICs qui constituent PACE2. La sortie analogique du circuit PACE-AM est connectée à un ADC situé sur la carte mère.

La carte mère comporte donc autant de convertisseurs ADC que de micro-modules qui lui sont rattachés. Un circuit numérique de concentration de données, appelé “K chip”, reçoit les données provenant de 4 ADC. Ce circuit assure le formatage des données, et l'ajout des informations de 'timing', en une trame numérique qui est alors envoyée vers un transducteur électro-optique, également situé sur la carte mère. A partir de là, les données quittent le détecteur central CMS pour être acheminées dans la salle de comptage par l'intermédiaire de liens optiques. Leur interface d'entrée, au niveau de la salle de comptage, est une carte FED (Front End Driver).

Deux ASICs numériques, situés sur la carte mère, assurent la synchronisation et le contrôle des communications; il s'agit du circuit CCU (Communication Control Unit) et d'un circuit PLL (Phase Locked Loop). Les signaux de contrôle en provenance de la salle de comptage arrivent sur une carte FEC (Front End Controller) via des liens optiques. Ils sont transformés par la carte CCU en signaux électriques et distribués en direction de la carte mère. Les signaux rapides sensibles sont acheminés en différentiels (LVDS) tandis que les signaux lents de contrôle sont délivré au format I^2C.

- a figure 5.1 montre un schéma synoptique de PACE2 et la figure 5.2 donne une vue générale de l'électronique du Preshower, faisant apparaître les chemins “ données” et les chemins “contrôle” .

Section 5.2 Le chemin analogique.

Deux buts fondamentaux sont recherchés dans la conception du circuit PACE2:

- Minimiser les fluctuations de piédestal.
- Maintenir une large gamme dynamique.

Le circuit PACE1 a montré une sensibilité importante aux parasites transitoires induits dans le substrat. PACE2 est conçu avec une architecture nettement moins sensible à la collection de charges parasites. Premièrement, l'impédance vue par le bus d'écriture de la mémoire a été réduite par l'utilisation d'une commande en tension plutôt qu'en courant; deuxièmement, le chemin de couplage par le substrat, entre les fonctions numériques 40 MHz et les fonctions d'amplification, a été physiquement supprimé; et troisièmement, le dessin du point mémoire a été optimisé pour minimiser l'injection de charges.

En mode tension, la mémoire analogique se comporte comme un échantillonneur-bloqueur. Chacune des cellules successives de la mémoire suit un échantillon de signal délivré par Delta, pendant un intervalle de temps de 25 ns, et mémorise la valeur atteinte à la fin de cet intervalle. Des imperfections peuvent cependant altérer le signal ainsi échantillonné. Elles se traduiront par de la distorsion de signal, et part du bruit. Le choix des composants du point mémoire, son dessin physique, et la qualité de la filière technologique sont autant de facteurs qui vont influencer les performances électriques de la mémoire.

Cette section examine, en terme de sensibilité aux injections de charges, les performances d'un point mémoire utilisant des 'switchs' MOS complémentaires (pour

accepter une large dynamique de tension). Tandis que l'injection de charge augmente en valeur absolue en utilisant des 'switchs' MOS complémentaires, la dispersion de cette injection dépend de la valeur de la capacité du point mémoire. Cette dispersion contribue au bruit du système, par conséquent, la structure de point mémoire retenue minimise le nombre de 'switch' et maximise la valeur de la capacité de stockage.

La section se termine par la présentation des fonctions de calibration développées et implantées sur le circuit Delta.

- La figure 5.5 montre les deux mécanismes d'injection qui peuvent altèrer la charge stockée dans le point mémoire (effet de canal et débordement de grille).
- Les équations 5.1 à 5.3 donnent l'erreur de tension induite par les effets de la figure 5.5.
- Les figures 5.6 à 5.8 montrent les schémas du point mémoire de PACE2 utilisant des switchs MOS complémentaires pour des raisons de gamme dynamique.
- L'équation 5.4 donne la contribution en tension des perturbations dues aux switchs complémentaires. Les figures 5.9 et 5.10 tracent l'effet des charges injectées sur la tension signal.
- Les figures 5.12 à 5.14 ainsi que les équations 5.6 à 5.12 illustrent le principe de relecture de la mémoire analogique.
- Les figures 5.15 à 5.17 montrent la méthode de calibration dans l'échelle des MIP et le circuit de calibration interne conçu.

Section 5.3 Les fonctions numériques de contrôle et les différents modes de fonctionnement.

PACE2 comporte un grand nombre de fonctions numériques, certaines commandent directement le fonctionnement du coeur du circuit, d'autres assurent la communication externe avec le reste du système. Cette section décrit le rôle de chacune de ces fonctions et présente les différents modes de fonctionnement du circuit.

- La figure 5.18 montre un schéma synoptique de la logique de contrôle de la mémoire analogique de PACE-AM (génération des signaux de séquencement: horloge d'écriture et horloge de lecture)
- La figure 5.19 est un organigramme fonctionnel de PACE2.

Section 5.4 Dessin physiques de PACE2.

Ce bref chapitre présente les dessins physiques des circuits Delta et PACE-AM et leur schéma de câblage. Les dimensions de Delta sont de 3.5 mm $\times$ 6 mm (21 mm^2) et celles de PACE-AM de 9.6 mm $\times$ 6.3 mm ($\sim$60 mm^2).

- La figure 5.20 donne la liste des plots d'entrée/sortie de Delta et de PACE-AM.
- Les figures 5.21 et 5.22 montrent le dessin physique des circuits Delta et PACE-AM.

Conclusions

La conception et le développement de PACE (système électronique de lecture frontale du sous détecteur Preshower de l'expérience CMS) ont été présentés.

Le Preshower consiste en un calorimètre à échantillonnage constitué de 2 plans absorbeurs en plomb intercalés avec 2 plans de capteurs silicium (ces deux plans de capteurs sont orthogonaux entre eux). Il comporte ∼4300 capteurs silicium composés de 32 pistes indépendantes. Les électrons ou les photons traversant l'absorbeur en plomb déclenchent une cascade électromagnétique provocant une gerbe de particules chargées. L'énergie contenue dans cette gerbe est proportionnelle à l'énergie du photon ou de l'électron qui a déclenché la cascade; elle est mesurée par la quantité de charge déposée sur les capteurs silicium. La granularité des capteurs autorise la séparation de photons proches dans l'espace et permet de discriminer les photons résultant de la désintégration des pions neutres de ceux résultant d'une possible désintégration du Higgs en deux photons ($H^0 \longrightarrow \gamma\gamma$).

Le Preshower n'est pas utilisé dans le déclenchement de niveau 1 de CMS et doit donc stocker les informations lues sur les capteurs jusqu'à ce qu'il soit sollicité par un cycle de lecture. PACE a done une fonctionalité similaire à celle del'électronique des detecteurs de traces au LHC, avec en plus la difficulté de mesurer des énergies dans une large gamme.

PACE a été développé par étapes:

- PACE1, le premier circuit prototype, basé sur une architecture à intégration de courant, a permis de réaliser un prototype électromécanique complet d'un démonstrateur (absorbeur, capteur silicium, électronique frontale) qui a conduit, après les mesures sur faisceau test, à la validation des performances physiques du Preshower.

- L'architecture à intégration de courant a montré des limitations qui influent fortement sur le bruit du système. Une architecture différente, à tension échantillonnée, moins sensible au couplage de charges entre les fonctions numériques et les fonctions analogiques bas signaux s'est révélée plus adaptée aux exigences de PACE. Le circuit Delta, mettant en oeuvre une partie de cette nouvelle architecture, comportant les préamplificateurs de charges et les fonctions de filtrage de mise en forme, a été réalisé en technologie DMILL. Delta est conçu pour mesurer des charges dans les gammes: 4 fC à 1.6 pC en mode gain réduit, et 0.4 fC à 200 fC en mode gain élevé. - Un circuit 36 voies, dérivé du circuit Delta, a été développé spécialement pour le test en production des capteurs. Ce circuit baptisé DeltaStream, comporte l'électronique frontale de Delta à laquelle sont ajoutés un étage échantillonneur-bloqueur et un multiplexeur analogique à grande dynamique fonctionnant à 20 MHz.

- Pour constituer PACE2, le circuit Delta (préamplificateurs + filtres de mise en forme) est associé au circuit PACE-AM (mémoire analogique à tension échantillonnée). PACE2 est capable de mesurer des charges comprises entre 4 fC et 1.6 pC (équivalent à une charge déposée de 1 à 400 MIPs); ce qui correspond à la gamme de charge récupérable sur une seule piste de capteur silicium avec un LHC opérant à haute luminosité (L≈ $10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$). Le mode gain élevé du circuit

Delta est destiné à la calibration système au seuil du MIP. Cette calibration peut s'appuyer sur l'utilisation d'un générateur d'impulsions programmable, intégré au circuit Delta, permettant de balayer les gammes LG et HG.

PACE2 est sorti de fabrication très récemment. A la date de rédaction de ce document, un programme d'essai intensif a débuté afin de vérifier si toutes les spécifications électriques sont tenues. Il est donc trop tôt pour dire si PACE2 (en DMILL) sera le circuit final retenu pour construire le Preshower. D'autres éléments, comme la stabilité et le rendement de la technologie seront particulièrement déterminants. Une pré étude est actuellement entreprise pour envisager une transposition du développement entrepris sur PACE2 dans une filière submicronique (circuit PACE3). L'utilisation d'une telle filière permettrait de réaliser une mémoire de plus grande capacité (sans impact notable sur le rendement technologique), d'obtenir une consommation de puissance inférieure et un coût final de production inférieur.

Preface

The work presented in this thesis describes the design and development of the front-end electronics for the CMS Preshower detector intended for use in the LHC experiment at the CERN laboratory for particle physics. The detector requires dedicated analog signal processing of charge deposited in $\sim$ 137600 silicon sensor elements by traversing charged particles at regular time intervals of 25 ns. The electronics must measure the charge to within 5% accuracy over a wide dynamic range and operate within a harsh radiation environment. Microelectronic ASIC design allows dedicated electronics to be located directly next to the silicon sensors in order to reduce huge quantities of information produced to manageable levels. The front-end ASIC design for the CMS Preshower experiment is called PACE (Preshower Analog Cms Electronics) and forms the subject of this thesis.

Chapter 1 introduces the Preshower detector within the context of the LHC experiment. The physics goals of LHC are discussed with particular emphasis on the question "What is the nature of mass ?". The chapter describes the role of the Preshower in the search for the Higgs boson, defines the physical design of the detector and establishes a set of electrical specifications for the design of PACE.

Chapter 2 deals with the difficulties imposed on the electronics by a harsh radiation environment. The chapter is in three sections; the first describes the radiation environment within CMS, the second describes mechanisms of radiation damage in electronic devices and the third reviews technology choices available to the designer.

Chapter 3 describes the design and results of an initial PACE prototype ASIC (PACE1). An electro-mechanical prototype of the Preshower detector containing 8 silicon sensors and PACE1 chips was built and used in tests with an electron beam. The results of these beam tests are described.

Chapter 4 describes a fundamental change in the technique of signal processing used within PACE from current integration to voltage sampling. The motivation for this change is explained and the design of a new charge preamplifier plus switched gain shaper (DELTA) is described. DELTA was validated in two ASIC chips and the results before and after irradiation are shown.

Chapter 5 presents the complete PACE design (PACE2) in a radiation tolerant technology. It incorporates the DELTA pre-amplifier and switched gain shaper and uses a voltage sampling analog memory.

Chapter 1

Introduction to the CMS Preshower Detector

1.1 Physics Goals

Much of the present understanding of the physical mechanisms of the universe from today back through 15 billion years of history to the origin of the universe (the so called "Big Bang") is described by a theory of the sub-atomic structure of matter known as the Standard Model (SM). Experimentation in the field of particle physics (a science that aims to find out what are the elementary constituents of matter and what forces control their behaviour) has verified most of the predictions within the SM. However the SM is not yet complete in its description of the universe since it still requires empirical input parameters and leaves some fundamental questions unanswered.

Questions such as :

- **What is the nature of mass ?**
- **Why does the universe appear to be made from matter as opposed to antimatter, why did the Big Bang not result in equal amounts of each ?**
- **Is it possible to describe all particles and forces within a single unified theory ?**
- **Is there a fourth state of matter "Quark Gluon Plasma" and what are its properties ?**

To refine our understanding of nature and provide further insight into some of these questions a particle accelerator known as the Large Hadron Collider (LHC) is

under construction at the CERN [1] laboratory on the French/Swiss border near Geneva. Combined with the LHC are 4 experiments called CMS, ATLAS, Alice and LHCb.

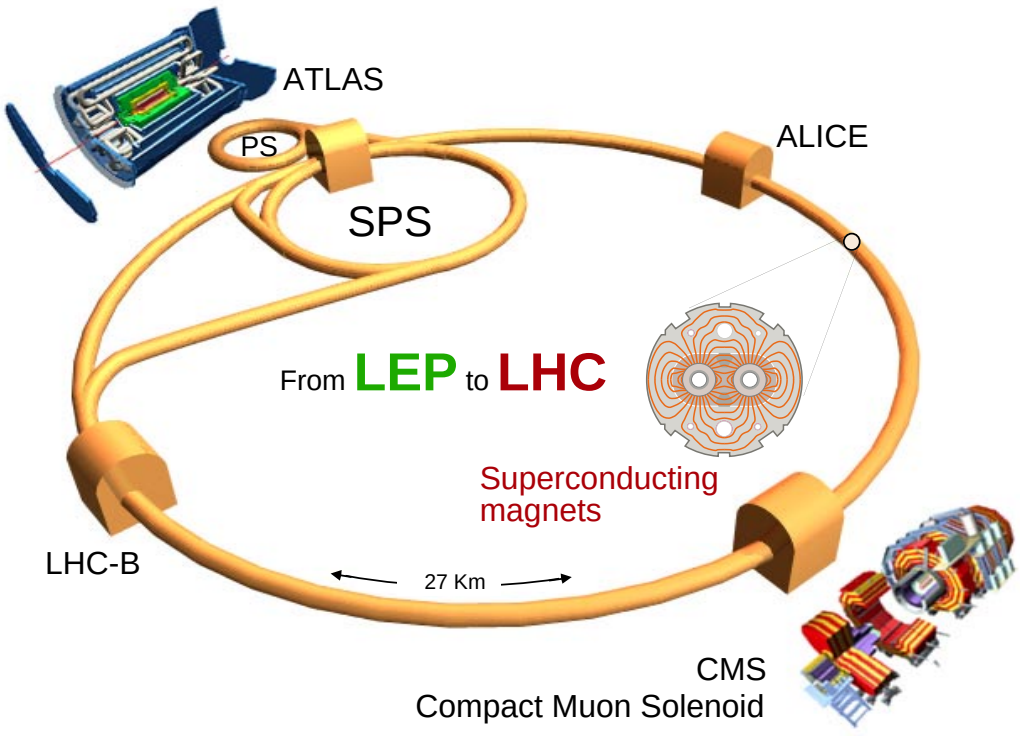

Figure 1.1: Schematic diagram of the LHC tunnel and the location of the 4 experiments

The LHC consists of a 26.7 km circular accelerator, containing two beam pipes, capable of accelerating counter rotating bunches of protons with beam energies up to 7 TeV. The bunches are focused to collide within the experiments with centre of mass "CM" energies up to 14 TeV. This will occur for the first couple of years at a luminosity (L) of L $\approx 10^{33}$ cm^{-2}s^{-1}. A higher luminosity period (L $\approx 10^{34}$ cm^{-2}s^{-1}) will then follow. Proton proton (p-p) collisions at this energy provide the interactions necessary to study the first three questions above. The LHC can also provide collisions of heavy ions at CM energies of up to 1312 TeV with L $\approx 10^{27}$ cm^{-2}s^{-1} for the study of quark gluon plasma.

CMS [1] and ATLAS [2] are general purpose detectors optimised for the study of the origin of mass but are also capable of exploring other physics avenues. Section 1.1.1 focuses on the current theory behind the origin of mass within the SM and section 1.1.2 focuses on the design goals of the CMS detector in order to test experimentally the theory.

[1]CERN : European Organisation for Nuclear Research

The LHCb detector [3] is designed to study CP violation in order to gain a better understanding of the asymmetries between matter and anti-matter. It plans to do this by studying the decays of quarks and antiquarks. A difference between the two decay processes breaks symmetry and could offer an explanation for the imbalance in our universe between matter and anti-matter. CP violation has been observed in the decay of neutral K mesons (K^0 and $\overline{K^0}$) however the effect is very weak and difficult to observe. It is expected that CP violation will be easier to observe in the decay of heavier mesons such as the B meson containing the bottom (b) quark.

Numerous B mesons will be created through the p-p interactions of LHC and most will be created close to the beam line. While both CMS and ATLAS are capable of studying B meson decays, LHCb has a structure that is purely designed to optimise their detection.

The ALICE experiment [4] is a dedicated detector designed to study heavy ion interactions at LHC energies. The aim is to study the physics of strongly interacting matter at extreme energy densities where the formation of a new phase of matter, quark-gluon plasma (QGP), is expected. Quarks are held together within protons and neutrons by the strong force and its carrier boson, the gluon. It is expected that at high enough energy the quarks and gluons will pass through a phase transition of deconfinement such that they will exist independently in a dense and energetic plasma. Physicists believe that the QGP existed in the very early state of the universe ($< 10^{-5}$ s after the Big Bang) and may exist today in the core of neutron stars.

The ion collisions of LHC at CM energies up to 1312 TeV is thought to be enough to enable detailed study of the phase transition to create QGP.

1.1.1 Mass and the SM Higgs boson

III	t (top)	b (bottom)	τ (tau)	ν_τ (tau neutrino)	γ g Z W (photon, gluon, Z & W bosons)
II	c (charm)	s (strange)	μ (muon)	ν_μ (muon neutrino)	
I	u (up)	d (down)	e (electron)	ν_e (electron neutrino)	γ: Carrier of the electromagnetic force g: Carrier of the strong force Z & W: Carriers of the weak force
Family	Quarks		Leptons		Force Carriers
SM Elementary Particles					

Table 1.1: Table of the SM elementary particles

The SM describes 3 families of quarks and their associated leptons. Each quark has 3 variations (red, green and blue) and can have right or left handed spin. The electron (e), muon (μ) and tau (τ) also have left and right handed spin. These particles plus 8 gluons (carriers of the strong force (g)), the photon (carrier of the electromagnetic force (γ)) and W^+, W^- and Z^0 bosons (carriers of the weak force) have been predicted by the SM and subsequently discovered through experimentation. Table 1.1 shows these elementary particles grouped into 3 families. Particle physics experiments have measured the mass of each particle very precisely.

One element that is missing however, is an experimentally proven mechanism that gives a particular particle its mass.

The particle that could explain the mass mystery is described within the SM as a spin-less Higgs boson (H^0). Associated with the Higgs particle is a Higgs field covering the whole of space. The strength of a given particle's interaction with the Higgs field defines the particle's mass.

The theory does not specify the mass of the Higgs (M_H) particle itself. There are limits however within which the SM Higgs must exist if the SM is to remain intact. The lower limit is set by present day experimentation and in particular LEP II. The upper limit is given by mathematical unitarity. As the theoretical mass of the Higgs increases, the probability of a Higgs decaying into known particles also increases. At approximately 1 TeV the probability becomes 1 and hence sets an upper limit.

Figure 1.2 shows the evolution of particle physics experiments and the window of operation for the LHC.

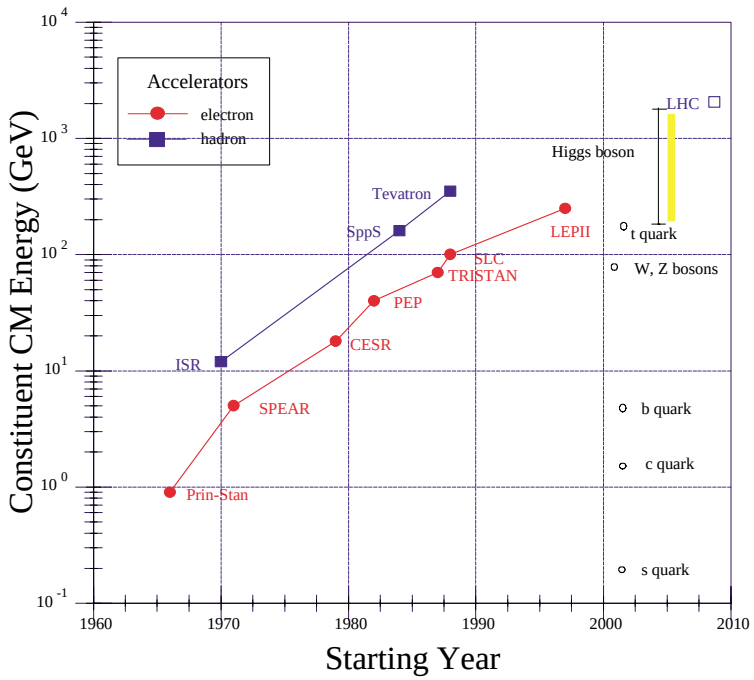

Figure 1.2: The evolution of HEP experiments with respect to CM energy [5]. The window to be covered by LHC is indicated.

Results from the LEP experiments up until 2000 [6] pointed towards a relatively light Higgs particle of < 215 GeV with a 95% confidence level (CL). More recent results during 2000 [7, 8, 9] have shown the lower limit to be 113.5 GeV (95% CL) and a possible Higgs signature at ~ 114 GeV. The 114 GeV measurement however is not conclusive since the measured result has less than 3σ excess above background. An excess of 5σ would be necessary to confirm a discovery hence more statistics are needed as will be provided by the LHC.

The SM Higgs has 4 possible production processes at LHC. These are illustrated in figure 1.3 [10]. The most probable process for Higgs production at LHC is the gluon gluon fusion mechanism.

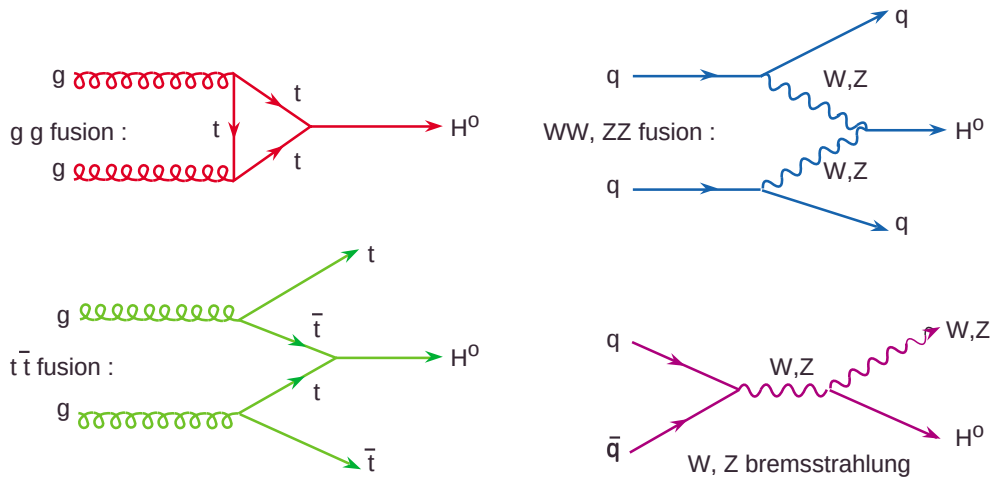

Figure 1.3: Standard model Higgs production mechanisms at LHC

Once created the Higgs has a number of possible decay modes. Figure 1.4 shows the various Higgs decay processes as a function of the Higgs mass and their branching ratios (probability of decay).

The dominant decay process is the $H^0 \longrightarrow b\overline{b}$ channel but this is very difficult to detect efficiently due to many background processes that mimic it. The most easily distinguishable Higgs channels can be summarised for 3 different Higgs mass regions as shown in table 1.2.

The ultimate quest of particle physics is to find a "theory of everything" (TOE), the unification of fermions and bosons into a single theory. At present the SM breaks down at very high energies, does not include gravity and offers no framework for unifying the 4 forces of nature (electromagnetism, weak, strong and gravity). A theory of Supersymmetry attempts to do this by introducing further families of particles (supermultiplets) in addition to the SM but at present there is no experimental evidence of any supersymmetric particles. If Supersymmetry exists then the origin of mass will be more complex, composing of elementary Higgs bosons accompanied by a number

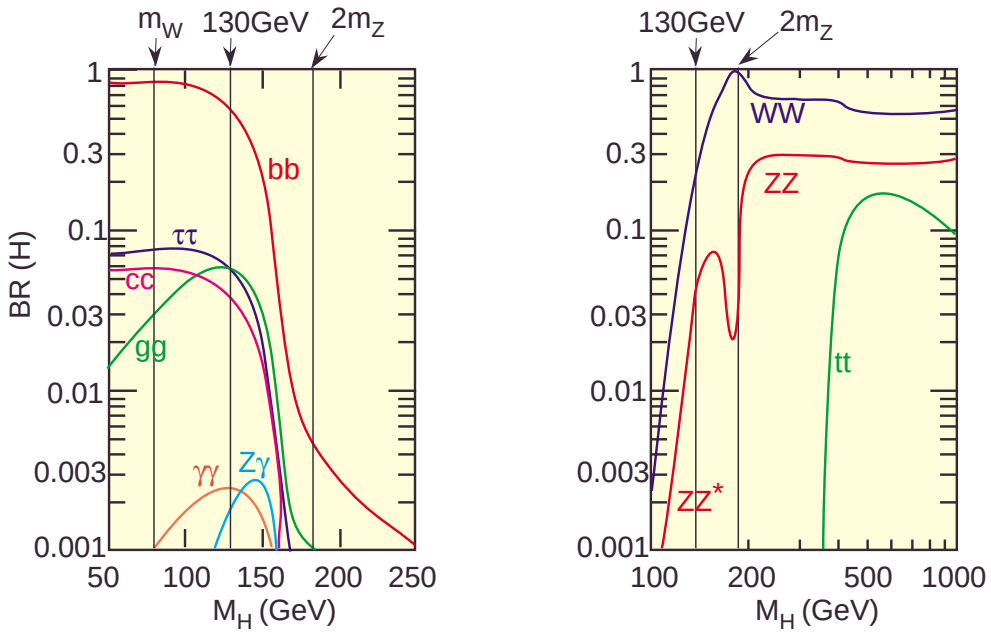

Figure 1.4: The branching ratios for the main decay channels of the SM Higgs as a function of its mass.

$\boldsymbol{M_H < 140}$ GeV	$H^0 \longrightarrow \gamma\gamma$
140GeV $< \boldsymbol{M_H} <$ 700 GeV	$H^0 \longrightarrow ZZ^* \longrightarrow 2l + 2l^-$ $H^0 \longrightarrow ZZ \longrightarrow 2l + 2l^-$
$\boldsymbol{M_H}$ >500 GeV	$H^0 \longrightarrow ZZ \longrightarrow l^+l^-\nu\nu$ $H^0 \longrightarrow ZZ \longrightarrow l^+l^-jj$ $H^0 \longrightarrow ZZ \longrightarrow l^{\pm}jj$

Table 1.2: The most distinctive H^0 decay channels according to the Higgs mass

of supersymmetric particles. At least one such boson (h^o) must have a mass smaller than ($\sim$ 130 GeV). The discovery of a supersymmetric particle is within the reach CMS and ATLAS and would be a major step towards a TOE (super unification).

1.1.2 CMS and the electromagnetic calorimeter

Particle detectors need to be able to identify particles and measure their position, momenta or energy.

Both CMS and ATLAS have the same macroscopic elements although they differ in terms of the technologies employed. Radiating out from the interaction point, these macroscopic elements are :

- **A Tracker** The tracker is designed to measure precisely the momentum of charged particles. It does this by having a highly segmented and layered charged particle detector involving millions of channels. Silicon pixel and strip sensors are used. The presence or not of a charged particle is recorded in each channel and the tracks reconstructed. The radius (R) of curvature of the tracks in the magnetic field (B) reveal the momentum (p) of the particle since $R \propto \frac{p}{0.3B}$.
- **An Electromagnetic Calorimeter (ECAL)** The electromagnetic calorimeter measures the energy of photons and electrons (γ, e). Almost no photons or electrons originating from the p-p interaction point pass beyond the ECAL.
- **A Hadron Calorimeter (HCAL)** The hadronic calorimeter measures the energy of particles such as protons, pions, neutrons and kaons (p, π, ν, κ). Almost no hadrons generated from the p-p interaction pass beyond the HCAL.
- **Muon Detector** The only particles generated from the p-p interaction to reach the muon detector are muons and neutrinos (μ, ν). The muons are detected directly but the neutrinos escape undetected. The presence of a neutrino is inferred by missing transverse energy (E_T).

An illustration of the CMS detector showing the various detecting elements listed above and the superconducting solenoid magnet is shown in figure 1.5.

where

- TK is the tracker
- EE and EB are the ECAL in the endcaps and barrel regions respectively
- HE and HB are the HCAL endcaps and HCAL barrel
- HF is the HCAL in the forward region
- ME and MB are the endcap and barrel muon chambers.

At the start of the CMS project, CMS specified 4 main design goals. These were as follows :

1. a very good and redundant muon system,
2. the best possible electromagnetic calorimeter consistent with 1.

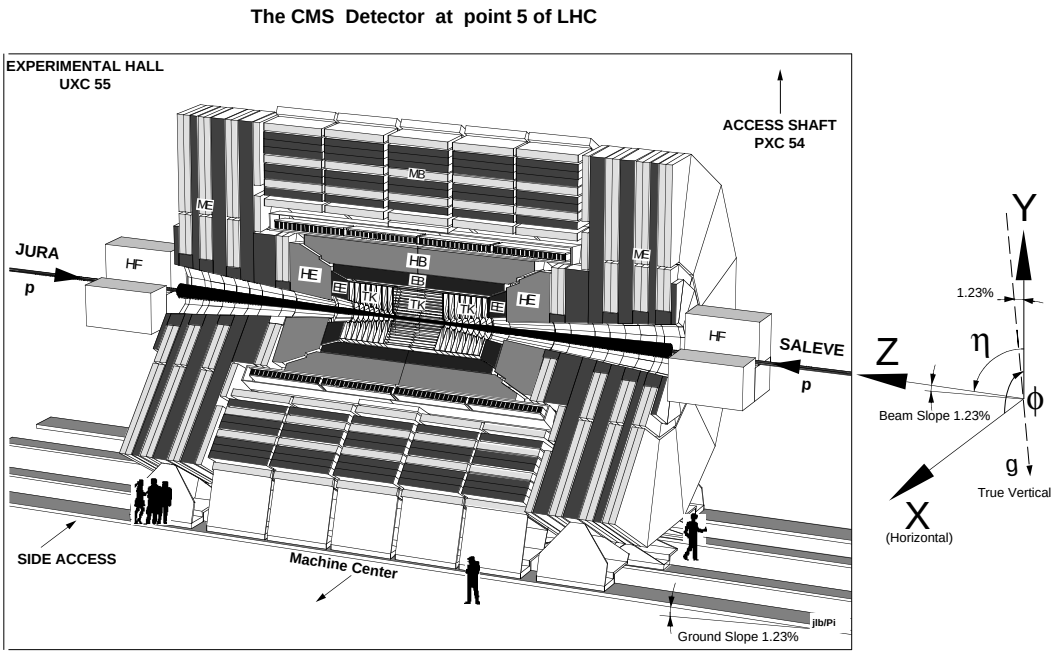

Figure 1.5: The CMS detector

3. a high quality central tracking to achieve 1. and 2.

4. a financially affordable detector.

From table 1.2 we can see that the gold plated Higgs decay channels involve photons or leptons. It is therefore evident that the ECAL will play an important role in furthering the understanding of mass and perhaps the discovery of the Higgs boson.

CMS has decided to place considerable importance on the ECAL as specified by the "best possible" statement in 2. of the design goals.

The most demanding of all Higgs decay channels on the ECAL is the $H^0 \rightarrow \gamma\gamma$ channel. This channel also lies within the most probable Higgs mass region (<130 GeV) as predicted by current theory and hinted at by LEP II. CMS has therefore used the $H^0 \rightarrow \gamma\gamma$ channel as the benchmark for the design of the ECAL.

The natural width of the Higgs particle increases for high mass Higgs particles as shown in figure 1.6. If the Higgs mass is < 150 GeV such that its width is of the order of 10 MeV then the Higgs mass resolution will be entirely dominated by the detector resolution. Under such conditions the mass resolution ($\frac{\sigma_m}{m}$) for $H^0 \rightarrow \gamma\gamma$ is given by equation 1.1.

$$\frac{\sigma_m}{m} = \frac{1}{2}\left(\frac{\sigma_{E_1}}{E_1} \oplus \frac{\sigma_{E_2}}{E_2} \oplus \frac{\sigma_\theta}{tan(\frac{\theta}{2})}\right) \tag{1.1}$$

where :

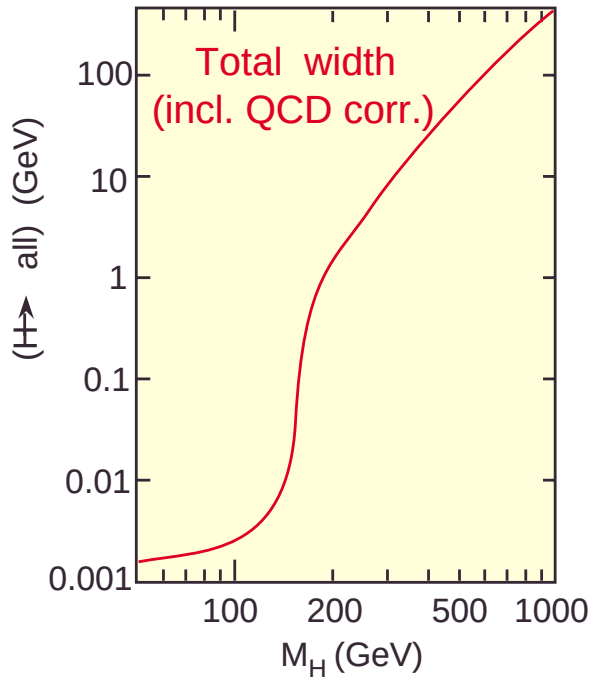

Figure 1.6: The natural width of the SM Higgs as a function of its mass.

- $\frac{\sigma_m}{m}$ is the mass resolution.
- $\frac{\sigma_{E_1}}{E_1}$ and $\frac{\sigma_{E_2}}{E_2}$ are the energy resolutions for the two photons.
- θ is the angle (in radians) between the two photons.
- σ_θ is the angular resolution.
- $\oplus$ is used to indicate the quadratic sum.

The photon energy resolution has the form of equation 1.2.

$$\frac{\sigma_E}{E} = \frac{a}{\sqrt{E}} \oplus \frac{\sigma_N}{E} \oplus c \tag{1.2}$$

where :

- $\frac{\sigma_E}{E}$ is the energy resolution (E is energy in GeV).
- a is the "stochastic" term - mainly governed by photostatics and sampling fluctuations.
- σ_N is the noise term.

- c is the "constant" term - mainly from shower containment limitations and calorimeter non-uniformities.

There are two common structures for calorimeter design namely, "sampling" calorimeters and "homogeneous" calorimeters [11].

A sampling calorimeter consists of layers of dense absorber (eg. lead) interleaved with a material sensitive to charged particles eg. silicon or scintillator. Incident photons or electrons create electromagnetic cascades of electrons, positrons and secondary photons via bremsstrahlung and pair production processes in the absorber. In silicon charged particles create electron/hole pairs and the charged is read directly by front-end electronics. In the case of scintillators, charged particles create photons and photo-sensors are used to convert the light into electrical signals. High energy electrons and photons that have not yet converted go through to the next layer. This process continues, absorbing progressively the energy of the incoming photon or electron. The sum of the electrical signals from the sensors is proportional to the energy of the incoming photon or electron. Figure 1.7 illustrates the design of a sampling calorimeter based on scintillation which is the most common type of sampling calorimeter. Also illustrated is the electromagnetic shower production process.

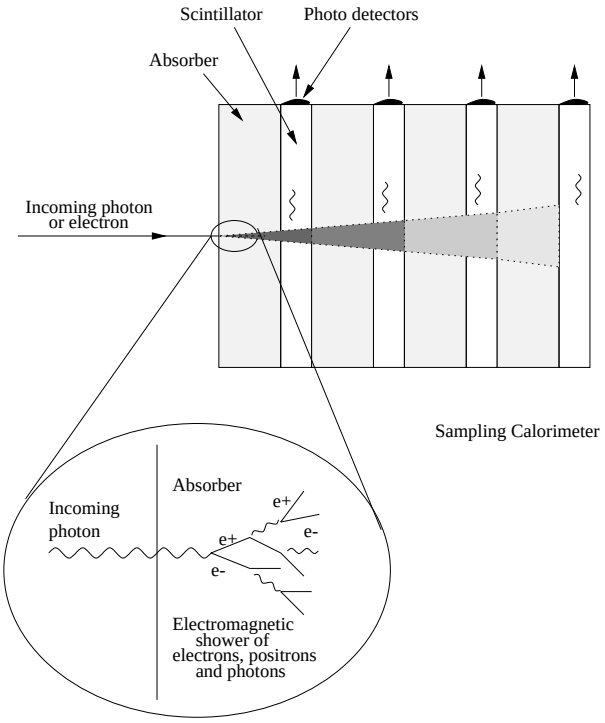

Figure 1.7: An illustration of a sampling calorimeter consisting of sheets of absorbers (to initiate electromagnetic showers) and a charged particle sensitive medium. The calorimeter illustrated is based on scintillation.

A homogeneous calorimeter performs both processes of shower production and charged particle detection within the same material.

CMS has chosen an homogeneous structure for the ECAL, using lead tungstate ($PbWO_4$) crystals. The expected energy resolution for the CMS ECAL is given by equation 1.3 which, for example, yields a mass resolution of $\frac{\sigma_m}{m} = 650$ MeV for a 100 GeV Higgs.

$$\frac{\sigma_E}{E} = \frac{2\%}{\sqrt{E}} \oplus \frac{200MeV}{E} \oplus 0.5\% \tag{1.3}$$

1.1.3 $H^0 \rightarrow \gamma\gamma$ backgrounds and π^0 rejection

Section 1.1.2 has shown that photons from $H^0 \rightarrow \gamma\gamma$ can be detected and their energy measured very precisely in the $PbWO_4$ crystal ECAL. Determining that the photons seen in the ECAL originate from a $H^0 \rightarrow \gamma\gamma$ process and not other known physics processes (backgrounds) is not immediately evident however.

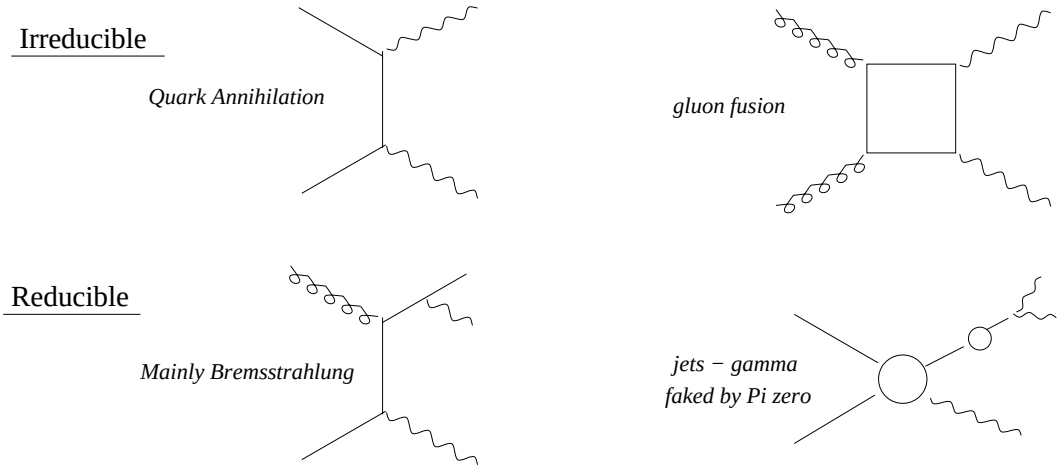

Figure 1.8: The four main backgrounds to the $H^0 \rightarrow \gamma\gamma$ decay channel.

Figure 1.8 shows Feynman diagrams for four background processes [12] that produce photons and could be mistaken for a $H^0 \rightarrow \gamma\gamma$ decay. The first two processes are irreducible (cannot be separately identified and eliminated) while the second two are reducible (can be separately identified and eliminated). Of the reducible pair, the first example produces two photons but one of the photons has other particles in close proximity. Its candidacy for $H^0 \rightarrow \gamma\gamma$ can therefore be eliminated by applying isolation cuts (ignoring photons with other particles in close proximity).

The second reducible process is the decay of a neutral pion (π^0) contained within jets to two very closely spaced photons. In the endcap region of CMS, the distance between these two photons is small (just a few mm). This is below the granularity of the ECAL and appears as a single photon. If paired with another photon it could mimic a $H^0 \rightarrow \gamma\gamma$ decay.

In the barrel region the separation between photons from a π^0 decay is large compared to the endcaps (approximately a cm). With this separation the ECAL is able to resolve two distinct photons and identify it as a π^0 decay for rejection.

In order to resolve two closely spaced photons in the endcap region to enable π^0 rejection, a higher resolution detector must be placed in front of the endcap ECAL. This detector is the Preshower.

1.2 The CMS Preshower

The Preshower is a fine grain detector placed in front of the endcap ECAL. Its function is to detect photons with good spatial resolution and measure their energy in order to enable π^0 rejection.

The purpose of the Preshower detector is to identify two closely spaced photons from a π^0 decay in order to separate these photons from single photons.

The Preshower detector (SE) is located in the endcap region of CMS between the tracker and the ECAL (EE). It is constructed as a disc with an angular coverage of $\eta = 1.653$ to $\eta = 2.6$. The location and coverage of the Preshower detector is illustrated in figure 1.9 [13].

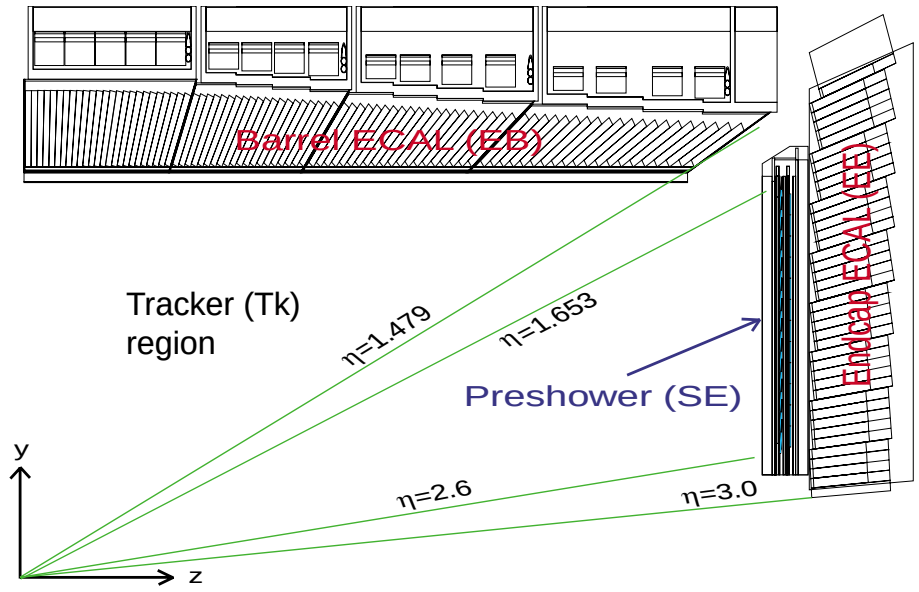

Figure 1.9: Longitudinal view of a CMS quadrant showing the Preshower coverage from $\eta = 1.653$ to $\eta = 2.6$.

The Preshower is designed as a small sampling calorimeter. Photons incident on a lead absorber initiate electromagnetic cascades creating a shower of electrons, positrons and photons. The charged particles can then be detected and the total energy measured. Silicon strip sensors have been chosen as the detecting elements. Two planes of silicon strip sensors, orthogonal to each other, provide the spatial resolution. Silicon also has a linear response to charge deposition, hence the energy deposited in the lead absorbers can be measured precisely and combined with the energy measurement of the ECAL to obtain the total energy of the incident photon.

Figure 1.10 shows the transverse profile of a shower of charged particles as seen by the silicon sensors.

A cross section of Preshower detector system is shown in figure 1.11. Moving in the direction of the incident particle, the first element encountered is a neutron moderator.

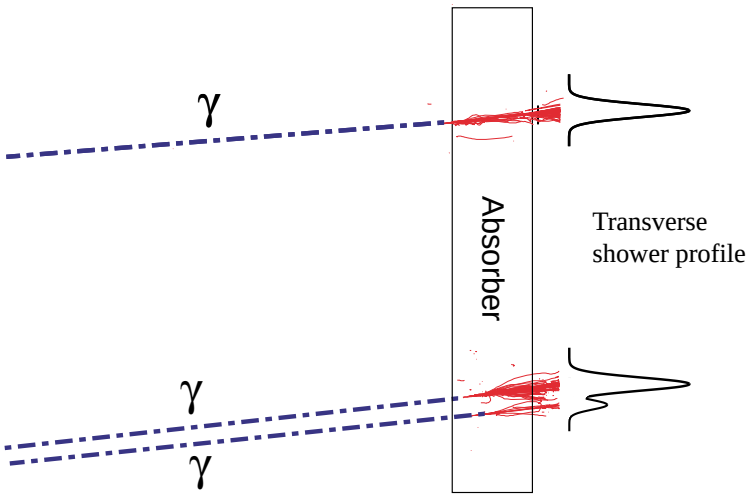

Figure 1.10: The transverse shower profiles resulting from both a single photon and two closely spaced photons

There is a moderator on both sides of the Preshower detector. The moderator (sometimes referred to as a window) has an Aluminium honeycomb structure filled with paraffin wax and sealed by aluminium sheets at the sides. The structure provides mechanical rigidity for the Preshower and protects the tracking region from a high neutron fluence generated inside the ECAL crystals (see chapter 2).

Following the moderator a heating film, insulation foam and cooling block provide control of the external and internal temperatures of the Preshower. The external temperature will be maintained at 18 ^{o}C $\pm$ 0.5 ^{o}C while the internal temperature will regulated to -5 ^{o}C.

Following the cooling block is the first lead absorber. Initial designs of the Preshower detector had one lead absorber followed by two orthogonal planes of silicon. However, subsequent simulations [14] showed that the efficiency of π^0 rejection depended heavily on the distance between the absorber and the silicon sensors. The current design has two planes of lead absorber, each followed directly by its associated plane of silicon sensors. Using this configuration the effective distance between the absorber and the silicon is optimised.

The total thickness of the absorber is 3 radiation lengths (3 X_0) for a particle incident at $\eta = 1.7$. This corresponds to $\sim 90\%$ probability of a photon initiating an electromagnetic shower as given by equation 1.4

$$P = 1 - e^{-(\frac{7}{9}\frac{T}{X_{0(Pb)}})} \tag{1.4}$$

where T is the total thickness (cm) and $X_{0(Pb)}$ the distance in cm corresponding to one radiation length in lead. The 3 X_0 is then divided between the first and second plane by a 2:1 ratio (2 X_0 and 1 X_0 respectively).

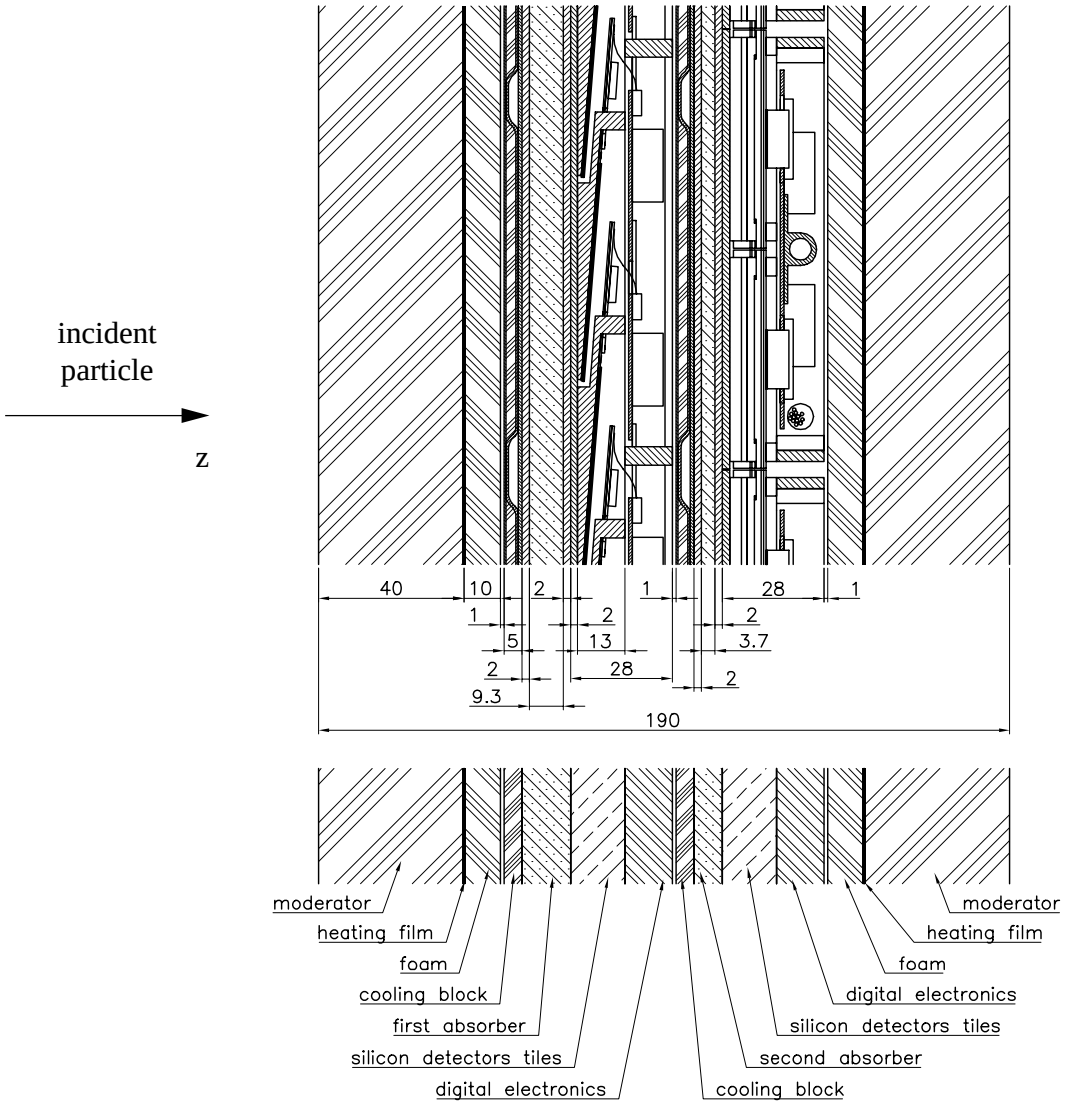

Figure 1.11: Cross section through the Preshower detector identifying the two planes of lead absorber and silicon sensors.

1.2.1 The silicon sensors

Silicon was chosen as the detecting medium because the granularity needed to resolve two closely spaced photons is easily obtainable and the charge response is fast and linear. A single silicon sensor measures 63 mm × 63 mm (the maximum size obtainable from a 4" wafer) and is divided into 32 silicon strips with a 1.9 mm pitch. The dimensions of the strips are very large in comparison to silicon strip sensors used for tracking purposes. This has the advantage of reducing the number of electronic channels to minimum (hence reducing complexity and cost). The disadvantage is high strip capacitance, which increases directly the electronic noise.

A cross section of a Preshower silicon strip sensor is given in figure 1.12.

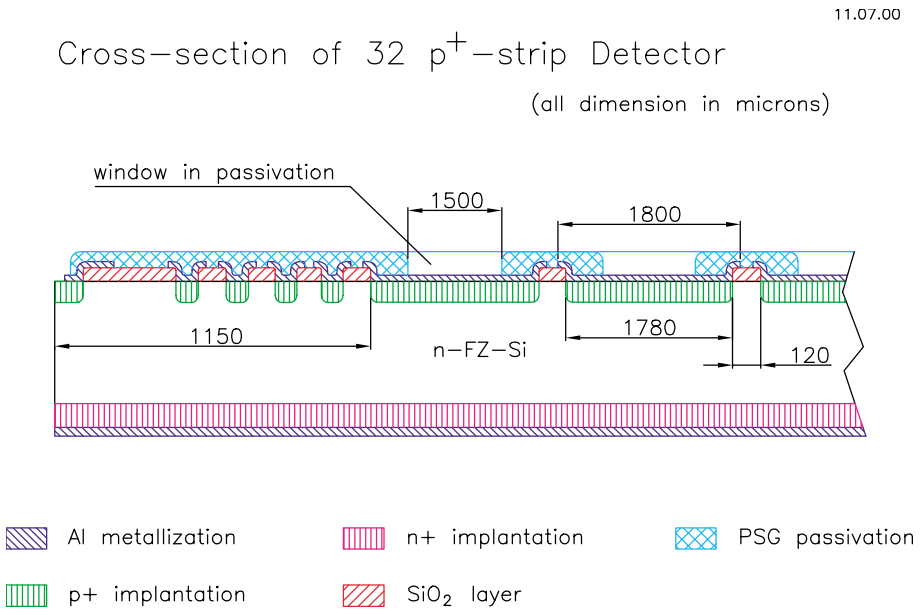

Figure 1.12: Cross section through a Preshower silicon sensor.

The bulk material is n- type silicon with p+ strips. Application of a positive voltage to the back side of the sensor increases the depletion region around the pn junction of each p+ diffusion. Since the p+ strips have much higher doping levels than the n- bulk material the depletion stretches further into the bulk than into the p+ region [15]. With sufficient reverse bias voltage applied across the junction the depletion region can extend right through the bulk to the n+ diffusion on the backside. In this condition the bulk (depleted of majority carriers) displays very high resistivity and has a strong electric field. Charged particles traversing the depletion region create a trail of electron/hole pairs through the process of ionisation. The electrons are quickly swept by the electric field to the backside of the sensor whilst the holes are swept to the closest P+ strip.

The amount of charge produced by a single traversing minimum ionising particle (MIP) depends on the thickness of the depletion region. A common benchmark is a mean of 25000 e ($\sim$ 4 fC of charge) for a fully depleted 300 μm thick silicon sensor.

The amount of voltage needed to deplete fully the detector will change throughout the lifetime of the experiment due to neutron induced radiation damage. Bulk damage tends to create acceptor-like defects that reduce the effective doping level of the n- bulk allowing the depletion region to extend further. This has the effect of lowering the full depletion voltage (V_{fd}). The bulk material eventually becomes intrinsic, passes through type inversion and becomes a p- bulk. Further irradiation increases the effective p doping level therefore increasing the V_{fd}. Figure 1.13 [16] shows the predicted evolution of V_{fd} as a function of the duration of the experiment at constant temperature (-5 ^{o}C). The choice of initial doping determines the point of inversion and maximum V_{fd} that would be required.

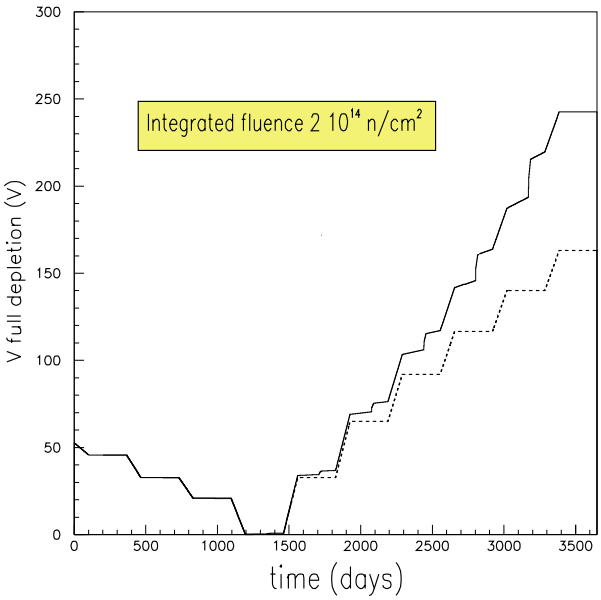

Figure 1.13: Full depletion voltage evolution during the lifetime of LHC (10 years). This is the side effect of type inversion due to bulk radiation damage and corresponds to the most irradiated part of the Preshower detector. The broken line assumes a constant temperature (-5 ^oC) throughout the lifetime of the experiment. The solid line assumes periodic annealing through warming the detector to room temperature as would happen during periods of routine maintenance.

A list of specifications have been defined for the manufacture of the Preshower silicon sensors as given in table 1.3 [17].

Parameter	**Value**
Wafer size	4”
Wafer thickness	0.32 $\pm$ 0.1 mm
Resistivity	3 kΩcm to 4 kΩcm
Polishing	single sided
n^+ layer thickness	> 2.5 μm
Total area	63 $\times$ 63 mm^2
Number of strips	32
Number of guard rings	~ 4
Strip pitch	1.9 mm
p^+ strip width	1.78 mm
Al strip width	1.8 mm
I_{total} at V_{fd}	< 5 μA
I_{total} at $V_{fd} + 150$ V	< 10 μA
Breakdown voltage (V_{br})	> 300 V

Table 1.3: Preshower sensor specifications

The parameters that are important for the front-end electronics are sensor leakage current, sensor capacitance and signal charge for one MIP.

- **Sensor leakage current** After 10 years of operation (2×10^{14} n cm^{-2}) at -5 ^{o}C the leakage current is expected to reach a maximum level of $\sim$ 20 μA per strip (channel).

- **Sensor capacitance** The capacitance per strip has been measured as 40 to 45 pF (backplane) plus 5 to 10 pF (inter-strip). The total capacitance per strip is between 45 pF and 55 pF.

- **Signal charge for a single MIP** A 300 μm fully depleted silicon sensor will produce a mean charge equivalent to 25000 e when traversed by a single MIP. However, the introduction of traps in the bulk material through neutron radiation damage reduces the charge carrier lifetime [18]. Recombination of carriers is responsible for an effective charge loss of approximately 15% after (2×10^{14} n cm^{-2}). This is a linear effect over the lifetime of the LHC experiment.

The implications of these requirements are discussed in section 1.3.

1.2.2 Preshower assembly and coverage

The assembly of the Preshower has three distinct phases each creating a structure that can be tested as an individual part.

The first is a structure that combines a single silicon sensor with the front-end electronics and is known as a "micro-module". Figure 1.14 shows a micro-module. The front-end electronics (labelled as Delta/PACE) are mounted on a daughter board (hybrid) together with surface mounted decoupling capacitors. The hybrid is then mounted together with a silicon sensor to a ceramic support, which in turn is glued to an aluminium "tile". Good thermal conduction is very important since the evacuation of heat from the sensor and electronics is achieved through the absorber plus micro-module structure.

Groups of micro-modules are assembled together in "ladders" (figure 1.15). Up to ten micro-modules are assembled onto one ladder. The ladders are then mounted onto an aluminium base plate. The structure of the tile allows a small overlap (in the direction of the strips). There is however a small gap between sensors perpendicular to the strip direction. Studies have shown [19] that a small gap in one dimension (less than a few mm) will not have a significant effect on the overall performance. The base plate aligns the sensors to an overall precision of 200 μm.

The absorber plus detector structure is in the form of a disc with an inner radius of 0.457 m and an outer radius of 1.23 m . The silicon coverage is therefore $\sim$ 4.1 m^2 for a single disc. In order to cover the Preshower disc as effectively as possible 4 different geometries of ladder have been designed. Figure 1.16 shows how the 4 different ladder structures can be assembled to cover the disc.

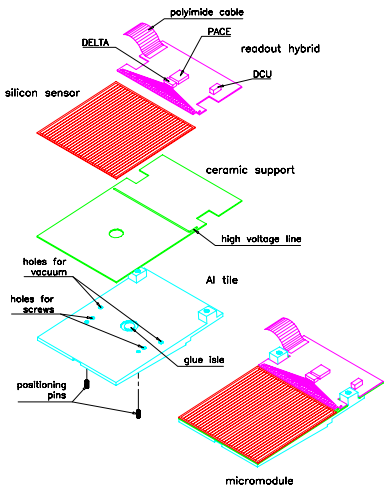

Figure 1.14: Elements of a single micro-module including the silicon detector and Delta/PACE front-end electronics.

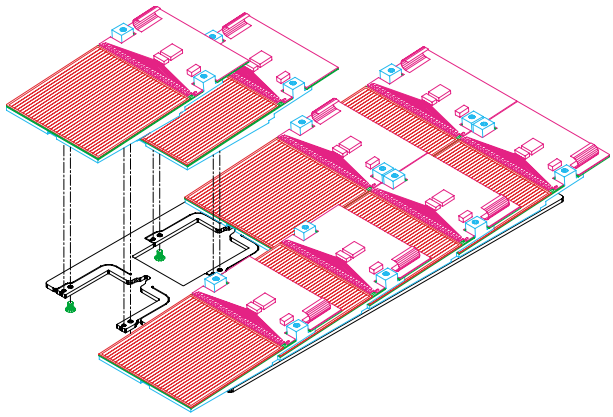

Figure 1.15: Assembly of micro-modules into a "ladder".

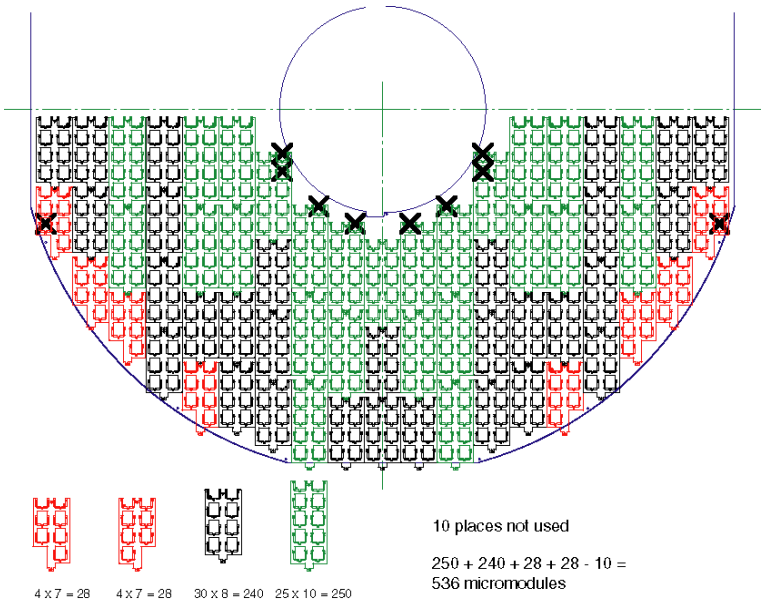

Figure 1.16: The layout of ladder structures to cover the Preshower disc.

There are 4 discs in total (2 planes in each endcap) representing $\sim$ 4300 micro-modules.

The only remaining element of figure 1.11 is the electronics mother board. The mother board supplies power and incoming electronic control signals to the front-end electronics. Also contained on the motherboard are readout electronics that digitise and transmit the data received from the front-end electronics.

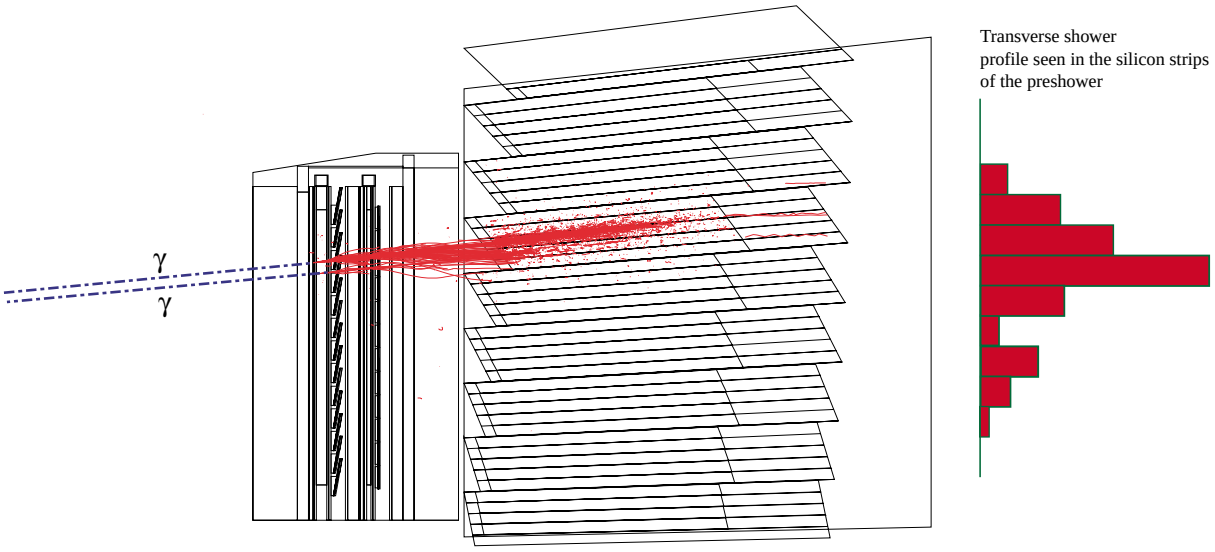

Figure 1.17: Simulation of two photons from the decay of a 30 GeV p_T π^0 incident on the SE and EE.

A simulation of the complete Preshower detector (SE) and ECAL (EE) is shown in figure 1.17. The simulation shows the response for 2 closely spaced photons produced from the decay of a π^0 with transverse momentum (p_T) of 30 GeV incident on the SE and EE.

1.3 Defining the Specifications for the Preshower Front-end Electronics (PACE).

The front-end electronics designed for the CMS Preshower experiment is called PACE (Preshower Analog Cms Electronics), the design of which forms the focus of this thesis. The main function of PACE is to measure accurately charge deposited in the silicon sensors and reduce the resulting quantities of data in time to manageable amounts.

This section gathers the input parameters from the physics in order to define the specifications for PACE. The section starts by considering the maximum signal size that needs to be measured accurately to determine an upper limit to the dynamic range. The lower limit of the dynamic range and the system noise is determined by the smallest signal that needs to be measured. The system noise can then be broken down into the contributions from various parts of the system. From here the resolution of the system can be defined.

The amount of data produced by the Preshower is assessed to define the architecture of PACE and system segmentation.

Together with environmental factors and constraints the section finishes with a summary of the PACE specifications.

1.3.1 Maximum signal size - upper limit to dynamic range.

Simulations using GEANT have been made to study the energy spectrum of electrons and photons incident on the CMS Preshower that could arise from background (minimum bias) events and exotic events [20].

Results from simulations of minimum bias events showed that there is virtually no chance of the Preshower receiving an electron > 300 GeV. Photons > 300 GeV are expected however with their average rate as shown below :

- > 300 GeV ~ 370/day
- > 600 GeV ~ 16/day
- > 1 TeV ~ 4/day

From the simulation, a prediction was made as to the number of strips that would be hit by significant numbers of MIPs. Table 1.4 tabulates the the number of strips exceeding various levels of charge deposition for the two Preshower planes during one day of minimum bias events.

The number of electronic channels per day that receive signals of more than 200 MIPs due to minimum bias events is very low (~ 90). A dynamic range upper limit of 200 MIPs would be sufficient for minimum bias events alone.

The energy of electrons and photons from interesting physics events is not precisely known. It is known however that some physics events will produce very high energy

Level of charge deposition (MIPs)	The number of strips per plane exceeding the stated level of charge deposition per day.	
	1st plane	2nd plane
> 100	60	289
> 150	13	167
> 200	0	90
> 250	0	48
> 300	0	21
> 350	0	7
> 400	0	3

Table 1.4: The number of strips that exceed the stated levels of charge deposition in one day as a result of minimum bias events.

electrons (1 TeV is considered a reasonable upper limit for electrons resulting from exotic physics events). Table 1.5 shows the percentage of events that result in charge levels in strips exceeding charge deposition thresholds of 200, 300 and 400 MIPs. Naturally the second plane is the critical plane due to a larger shower production after the second absorber. A large percentage of events ($> 80\%$) involving high energy electrons will produce charge deposition levels above 200 MIPs. The percentage of events exceeding 400 MIPs is much less ($\sim 40\%$ for 1 TeV electrons and $\sim 14\%$ for 600 GeV electrons).

Incident electron energy	% of events exceeding stated charge deposition threshold					
	200 MIPs		300 MIPs		400 MIPs	
	1^{st} Plane	2^{nd} Plane	1^{st} Plane	2^{nd} Plane	1^{st} Plane	2^{nd} Plane
300 GeV	0.5	44.8	0.0	7.2	0.0	0.3
600 GeV	7.1	79.2	0.1	42.8	0.0	14.3
1 TeV	15.3	89.4	1.6	65	0.0	37.7

Table 1.5: Percentage of events that would exceed the stated charge deposition thresholds for incident electron energies up to 1 TeV

A dynamic range upper limit specification of 400 MIPs for PACE will therefore result in a channel saturating in $\sim 40\%$ of events from a 1 TeV electron. It does not mean however that all the information from these events are lost since neighbouring strips can be used to estimate the charge deposited in the saturated strip. The error on the charge measurement will increase using this neighbouring channel estimation method. However, the amount of energy deposited in the Preshower compared to that deposited in the ECAL is much smaller for high energy particles and hence the weight

of the Preshower energy measurement in the combined Preshower + ECAL energy resolution reduces. An increased error bar on the Preshower measurement for charge deposition > 400 MIPs is not considered critical for the overall energy resolution measurement.

- **An upper limit of 400 MIPs (1600 fC) per channel was chosen for the dynamic range specification.**

Very large signals ($\sim$ 1000 MIPs) may also occur but do not need to be measured by the system. The requirement on the electronics for such a signal is that a quick and reliable recovery from a saturated state is ensured.

1.3.2 Minimum signal size - lower limit to dynamic range, noise, resolution.

The main function of the Preshower is π^0 rejection which is best achieved with clean identification of 1 MIP signals (2 MIPs is still acceptable however and considered the maximum lower resolution) [21]. To achieve this maximum lower resolution, the system noise floor during data taking must not exceed 0.6 MIPs (2.4 fC) and must include the whole electronics readout chain. To add a safety margin the dynamic range for the front-end electronics is set to 0.4 MIP - 400 MIPs requiring a resolution of 10 bits.

Calibration on a channel to channel basis will be necessary to take into account systematic effects. These include charge loss and distortion of signal shape in the sensors and channel to channel variations of gain, pulse shape, and dynamic range in PACE. The only reliable way to calibrate the Preshower will be to use single MIP particles produced from the p-p interaction.

The calibration of the Preshower will therefore impose the strictest requirements in terms of signal to noise (S/N). A S/N > 5 for the total system noise will be necessary to perform accurate calibration. This must also be calculated for the most irradiated region of the Preshower after ten years of operation. It must take into account a 15% charge loss in the sensor due to radiation damage. The upper limit for total system noise (ENC_t) expressed in terms of Equivalent Noise Charge is expressed by equation 1.5.

The concept of ENC, descriptions of noise sources and noise calculations are given in appendix A.

$$ENC_t \leq \frac{25000 \times 0.85}{5} = 4250 \text{ (e) rms} \tag{1.5}$$

As a first approximation the ENC_t is composed of the quadratic sum of the noise generated by the sensor (ENC_{sens}) and the noise generated by the electronics (ENC_{fe}).

The sensor is a diode and displays current dependent shot noise (explained in appendix A) given by equation 1.6, where q is the electron charge and I_{leak} the detector

leakage current. Assuming noise filtering by shaping the signal in PACE, the ENC_{sens} can be expressed as equation 1.7 where t_m is the peaking time after shaping.

$$\frac{\overline{i_{sens}^2}}{\Delta f} = 2qI_{leak} \tag{1.6}$$

$$\overline{ENC_{sens}^2} = \frac{(\overline{i_{sens}^2}/\Delta f)t_m}{3} \tag{1.7}$$

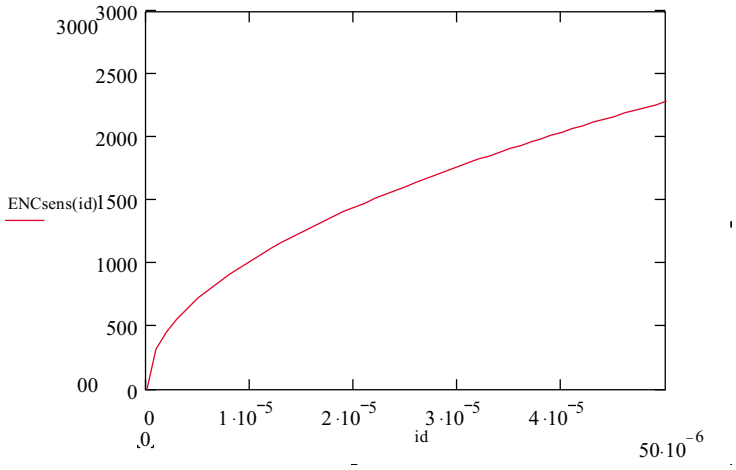

Figure 1.18: The sensor shot noise as a function of sensor leakage current. The noise is expressed as ENC (in number of electrons) and the leakage current (id) is in amps.

Figure 1.18 plots the expected ENC_{sens} as a function of leakage current for $t_m = 25$ ns. At 20 μA (the leakage current expected per strip after irradiation) the $ENC_{sens} \sim$ 1440 e rms.

$$ENC_{fe} \leq \sqrt{\overline{ENC_t^2} - \overline{ENC_{sens}^2}} \approx 4000 \text{ (e) rms} \tag{1.8}$$

The upper limit for the noise of PACE (ENC_{fe}) is given by equation 1.8. This must include additional noise contributions introduced by the sampling technique used. In order to have some safety margin the PACE preamplifier noise has been specified at $<$ 3200 e.

- **The specification of the noise of the PACE preamplifier is $<$ 3200 e (0.16 MIP) with the full sensor capacitance.**

In applications where a large dynamic range is not required, the design of the electronics can be made such that the noise is dominated by the preamplifier and all

other noise sources can be neglected. For large dynamic range applications this is only partly true since the gain has to be kept small making it easy to introduce distortion when sampling on the shaped signal.

Since the full dynamic range is needed only for data taking and not for calibration, two modes of operation can be specified to allow for increased gain during calibration.

- **Data Taking : Dynamic Range 0.4 MIP - 400 MIPs (10 bits)**
- **Calibration : Dynamic Range 0.16 MIP - 50 MIPs (9 bits)**

A specification including two ranges requires that there is a direct correlation between the calibration measurement and measurement made during data taking.

1.3.3 Data reduction and PACE architecture

The Preshower detector has 4300 silicon sensors divided into 32 strips per sensor. The electronics needs to sample the charge from each of the 137600 channels every 25 ns with 10 bit accuracy.

Most of this information is uninteresting and can be ignored. Designing PACE as a microelectronics ASIC enables sophisticated data processing to be located directly next to the sensors. This allows the natural segmentation of one PACE chip per sensor.

To reduce the quantity of information with respect to time, CMS produces a hierarchy of triggers. The first level trigger (LV1) is produced with a latency (delay) of 3.2 μs after the interesting event. PACE therefore needs to sample the charge from the 32 sensor strips every 25 ns, store this information for 3.2 μs (128 clock cycles), discard all information from events not triggered and readout all channels from events that are triggered. An architecture that is suitable to perform this function is that of an analog memory [22, 23, 24]. A much simplified block diagram of the PACE analog memory is shown in figure 1.19

An analog memory has a number of continuously active inputs that are sensitive to charge from silicon sensor strips. At each clock cycle, charge proportional to the input signal is stored on a column of capacitors within a switched capacitor matrix. The following clock cycle will repeat the operation but onto a fresh column of capacitors. Once all columns have been written to then the first column will be overwritten, hence the writing of columns of capacitors is performed in a continuous loop. On receiving a trigger individual columns can be flagged as containing interesting data. These flagged columns are then protected from being overwritten by a mechanism within the control logic that skips the column on successive write loops. A column which has been flagged to be skipped is said to be in "skip" mode. The contents of a column in skip mode are made available to be read at a lower frequency. Each column is encoded into an address and the address stored in a FIFO until the system requires the column to be readout. Once the data has been read the column flag is removed and the capacitors are again available for writing.

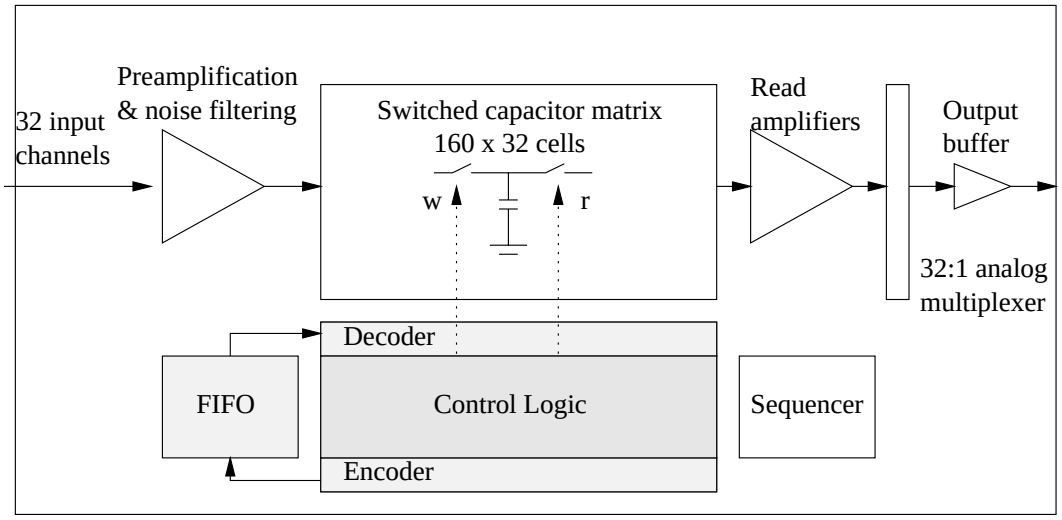

Figure 1.19: Simplified block diagram of the main components in the PACE analog memory.

The depth of the switched capacitor matrix within PACE is determined by the LV1 latency, the number of samples taken per LV1 and the maximum number of triggered events that need to be stored simultaneously.

PACE takes 3 samples/channel for each LV1 in order to precisely measure the charge (discussed in chapter 4). The maximum number of triggered events that need to be stored simultaneously is 8. This is the buffering capacity of PACE needed to ensure smooth running with a maximum LV1 rate of 100 kHz [25] and PACE analog readout frequency of 20 MHz.

The minimum depth of the switched capacitor matrix is therefore $128 + (3 \times 8) = 152$. A depth of 160 was decided in order to be flexible to small changes in LV1 latency.

The maximum LV1 rate also determines an upper limit to the time taken to read one column of capacitors from the switched capacitor matrix. With 3 columns per LV1, each column must be read within $\frac{1}{3 \times 100kHz} = 3.33\ \mu$s. If it takes longer than this, the analog memory would not empty fast enough and the FIFO would become full. For the specification, an upper limit of 2.1 μs was chosen. This can be achieved with a 20 MHz readout frequency. Simulations have shown that with a 100 kHz LV1 rate, 3 columns per LV1, memory depth of 160 and FIFO capacity of 8 triggers that the probability of an overflow is 1×10^{-5} [26].

- **Number of channels : 32**
- **Sampling frequency : 40 MHz**
- **Switched capacitor matrix depth: 160**
- **Number of samples per trigger (LV1): 3**
- **Minimum capacity for simultaneously stored triggered events : 8**

- **Analog readout frequency: 20 MHz**
- **Max readout cycle time for one column: 2.1 μs**

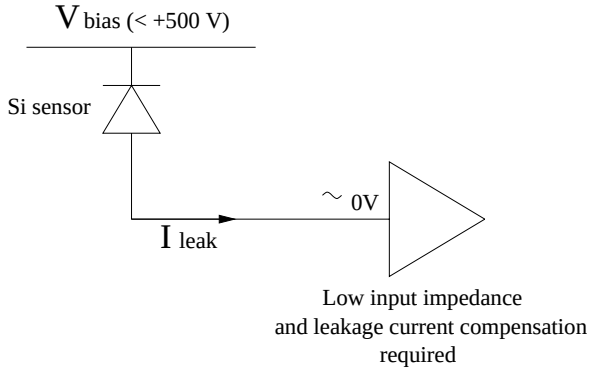

Figure 1.20: Sensor connection to the preamplifiers. Low input impedance and compensation for sensor leakage current is essential.

The Preshower sensors are designed to be directly coupled to the inputs of the preamplifiers in PACE as shown in figure 1.20. The voltage across the sensor diode is between the high voltage bias on the back side of the sensor and the voltage defined by the input impedance of the preamplifiers. It is therefore evident that the input impedance must be very low in order to define a dc input voltage of ~ 0 V. Leakage current from the sensor due to radiation damage will also have to be treated by the preamplifiers in order to avoid saturation and ensure normal operating behaviour. The expected leakage current from each strip is 20 μA after 10 years of operation in LHC. The specification for normal operation of the preamplifiers has been set to 40 μA per channel to provide a safety margin.

- **Preamplifier insensitivity to sensor leakage current < 40 μA**

1.3.4 Environmental considerations and constraints

Placing the PACE chips on the micro-modules means that they will be exposed to high levels of radiation both from charged particles and neutrons. Understanding the effects of radiation damage in electronics and knowledge of design techniques resistant to radiation is extremely important. Chapter 2 is devoted to the study of radiation effects in electronic devices. The specification for PACE is that it must operate after 10 Mrads(Si)[2] of ionising radiation and a neutron fluence of 2×10^{14} cm^{-2}.

- **Radiation tolerance : ionising radiation ... 10 Mrads(Si), neutron fluence ....2×10^{14} cm^{-2}**

[2]The SI unit for absorbed dose is the Gray (Gy) where 1 Gy= 1 joule kg^{-1}. Most physics publications use Gray whilst most engineering publications use the older unit "rad". 1 Gy= 100 rad.

The second major environmental factor is limits on power consumption due to the demands on cooling required to evacuate dissipated heat. Cooling of the PACE chips will be provided through the micro-module and lead absorber to the cooling plane (see figure 1.11). The same cooling path is used for the power dissipated in the silicon sensor and motherboard electronics. Detailed studies have been made on cooling [13] allowing 4 kW per readout plane or 3.7 W per micro-module. 300 mW per micro-module is assigned to thermal leakage through the insulating foam, 1 W to the motherboard, 320 mW for the sensor (assuming V_{fd} =500 V and I_{leak} =20 μA per strip) and 500 mW for PACE giving 2.12 W per micro-module. The remaining 1.58 W provides a safety margin calculated through worse case scenarios. The worst case scenario for PACE is 800 mW.

- **PACE power consumption : 500 mW (15 mW/channel)**

Summary - PACE Specification

The Preshower detector is designed as a small sampling calorimeter with two planes of lead absorber interleaved with two planes of silicon sensors. It is located between the Tracker and ECAL in the endcap regions of the CMS detector currently under construction for the LHC experiment. One of the key physics goals of LHC is to gain greater insight into the nature of mass through the search for the SM Higgs boson. Current predictions point to a relatively light Higgs mass ($H^0 < 215$ GeV) which favours a two photon Higgs signature from a $H^0 \longrightarrow \gamma\gamma$ decay. The Preshower detector will play a key role in the H^0 search by providing $\pi^0-\gamma$ separation for energetic π^0s at high η.

Electromagnetic cascades from photons or electrons incident on the lead absorbers create showers of charged particles depositing charge in the silicon sensors. Each silicon sensor is divided in 32 strips and is assembled together with a PACE front-end electronics chip on a micro-module.

Each PACE must measure the energy deposition in the 32 silicon strips at 25 ns intervals. Since the Preshower is not used in the first level trigger of CMS, PACE needs to store charge information gathered from the strips until selected data is triggered for readout. A suitable architecture for such a design is that of an analog memory. PACE is hence designed as an analog memory which is similar to the electronics needed for a tracking system, however PACE has the added complication of energy measurement over a wide range (the function of a calorimeter).

A summary of the main specifications for PACE are contained within table 1.6.

Further specifications of how PACE interfaces with other electronic components in the system are dealt with in chapter 5.

PACE Specifications	
Number of channels	32
Sampling frequency	40 MHz
Sensor coupling	dc
Insensitivity to sensor leakage current	$< 40\mu A$
Dynamic Range during data taking	0.4 MIP - 400 MIPs (10 bits)
Dynamic Range during calibration	0.16 MIP - 50 MIPs (9 bits)
Preamplifier noise	< 3200 e rms with input cap. (55 pF)
Switched capacitor matrix depth	160 cells
Number of samples per trigger (LV1)	3
Minimum capacity for simultaneously stored triggered events	8
Analog readout frequency	20 MHz
Max. Readout time for one column	2.1 μs
Radiation tolerance	Ionising radiation ... 10 Mrads(Si) Neutron fluence ....2×10^{14} cm^{-2}
Power consumption	<500 mW (15 mW/channel)

Table 1.6: Summary of the specifications for the Preshower front-end electronics ASIC, PACE.

References

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Chapter 2

Radiation Issues

The Preshower silicon sensors and front-end electronics will be exposed to intense radiation and will subsequently degrade in performance due to radiation damage. This chapter explores radiation issues such as the CMS radiation environment in section 2.1, effects of radiation on electronic devices in section 2.2 and technologies available to the designer that can operate in such environments (section 2.3). The chapter concludes with a chosen technology for the PACE design.

2.1 The Radiation Environment

This section examines the main components of the radiation background within an LHC detector, most of which are derived from the p-p interaction itself.

2.1.1 A proton-proton inelastic interaction in the absence of surrounding material and magnetic field

Secondary particles produced from p-p inelastic interactions at LHC will consist mainly of high energy pions. Some other mesons such as kaons may also be produced along with baryons such as energetic protons and neutrons. The charged pions constitute the bulk of the charged particle flux. This flux follows a $\frac{1}{(r_\perp)^2}$ relationship where $r_\perp$ is the distance from the beam. The flux can be expressed as the number of charged particles (N_{ch}) per second (s) per unit area (a) as in equation 2.1 [1].

$$\frac{d}{d_a}N_{ch} = \frac{N_{ch}s^{-1}}{(r_\perp)^2} \tag{2.1}$$

If one plots the number of particles per unit of pseudorapidity however, there is almost a plateau between $\eta = -3.0$ and $\eta = 3.0$ as shown in figure 2.1.

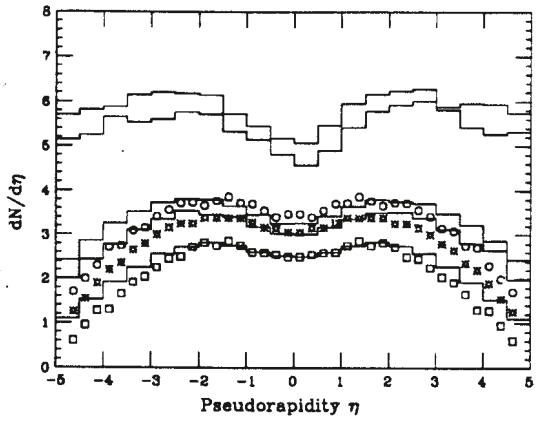

Figure 2.1: Pseudorapidity distributions of charged particles at η =0.54, 0.9, 1.8, 16 and 40 TeV (from bottom to top)[2]

The plateau in figure 2.1 can be approximated to a constant (H) [2] which is ∼6.3 for charged particles in LHC with $\langle pT \rangle = 0.44$ GeV/c.

The number of neutral pions (π^0) produced from the p-p interaction is approximately half that of charged pions. The π^0 has a mean lifetime of 8.4×10^{-17} s and will therefore decay within a distance of 25.2 nm from the interaction point. Although there are many possible decay processes, 98.8% of all π^0 decays will result in 2 photons, $\pi^0 \rightarrow 2\gamma$ [1]. There will therefore be a photon flux of the same magnitude as the charged particle flux. It will have the same distribution with respect to pseudorapidity but only half the mean momentum.

2.1.2 Effects due to the magnetic field

The magnetic field within CMS will be 4 Tesla. This will distort slightly the $\frac{1}{(r_\perp)^2}$ dependence and increase the charged particle flux due to loopers. However, the charged particle flux will be independent with respect to z [3],[4] .

2.1.3 The addition of the tracker and calorimeters

The high energy secondaries will loose some of their energy as they pass through the material of the tracker, ECAL and HCAL through electromagnetic showering and cascade processes. Very little energy from the traversing particles is deposited in the tracker and most is absorbed within the calorimeters.

The products of these processes are low energy neutrons and photons. Most of the photons are quickly reabsorbed in the material , those that escape the material can convert to electrons and positrons. The neutrons will scatter and eventually be captured producing more photons. The time scale for these various processes exceeds the production rate of the secondaries producing an almost uniform and isotropic gas of low energy background particles [5].

Radiation damage in the silicon is severe for these low energies and the sensors and electronics of the tracker would not last very long if left unprotected. Since most of the neutrons are created through hadronic interactions in the ECAL then shielding can be placed between the tracker and the ECAL. The objective is to slow the thermal albedo neutrons from energies in the region of 1 MeV to 100 keV as they reflect back into the tracker region. Neutrons at energies $<$ 100 keV are much less harmful to silicon. The most efficient way to moderate neutrons is by elastic scattering from hydrogen nuclei. A suitable moderating material is therefore one with a high level of hydrogen content and high radiation length (in order not to occupy too much space). Paraffin wax satisfies the criteria.

2.1.4 The CMS radiation environment

Various simulators have been used to generate minimum bias events with LHC energies and luminosity and follow the physical processes throughout the detector. However, the uncertainty of the results could be quite high. The reason for this is that no experimental results exist yet for minimum bias events at $\sqrt{s}$ =14 TeV. The cross section, multiplicity and momentum distribution estimates are expected to carry an error bar of $\sim$ 30%.

Figure 2.2 shows the simulated charged hadron and neutron fluence in the top plot, and radiation dose in the lower plot for CMS. The geometry should be compared with figure 1.9 to identify the relative position of the various macroscopic elements of CMS.

The top plot of figure 2.2 combines fast neutrons ($E >$ 100 keV) and charged hadrons together in one fluence as their effects on silicon are similar. One can see a very intense neutron source in the ECAL endcaps especially at high η . A positive gradient exists in the fluence with respect to η. The effects of the moderators can also be seen on both sides of the Preshower producing steps of approximately a factor of 3. The fluence is dominated by charged hadrons and fast neutrons direct from the p-p interaction for $r_\perp$ <50 cm whereas albedo neutrons dominate for $r_\perp$ >50 cm.

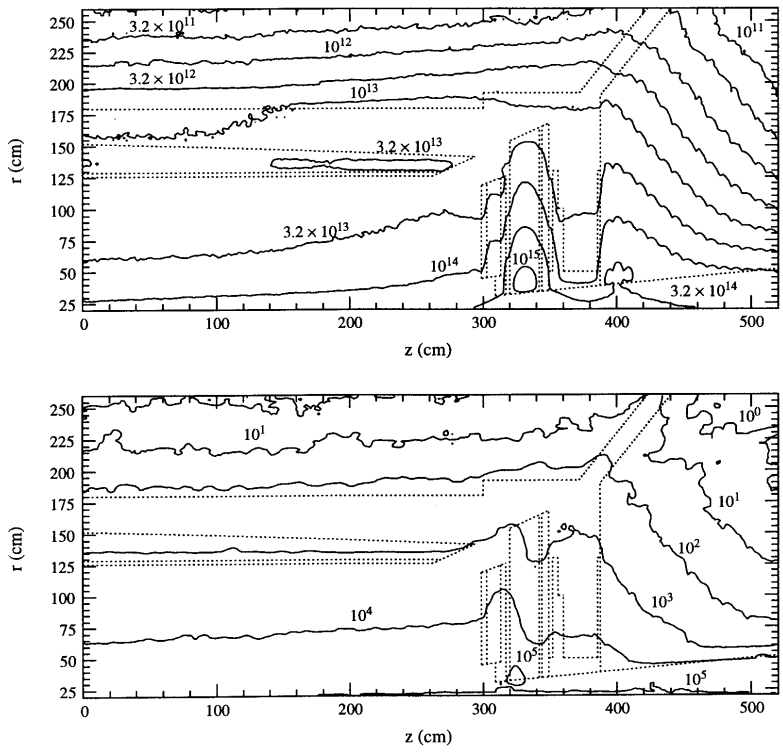

Figure 2.2: Simulated charged hadron and fast neutron fluence in cm^{-2} (top plot) and radiation dose in Gy (lower plot) within CMS [6].

2.1.4.1 The Pixel environment

The detector closest to the interaction point is the Pixel detector. Secondaries from the p-p interaction dominate and the fluence follows the $\frac{1}{(r_\perp)^2}$ relationship. Table 2.1 summaries the pixel environment [4].

	$r_\perp = 4.3$ cm	$r_\perp = 11$ cm
Dose	828 kGy	187 kGy
Charged Hadron Fluence	2×10^{15} cm^{-2}	4×10^{14} cm^{-2}
Neutron fluence (E > 100 keV)	2×10^{14} cm^{-2}	6×10^{13} cm^{-2}

Table 2.1: Radiation values for the CMS pixel detector

2.1.4.2 The Tracker environment

The silicon tracker occupies the region 20 cm $< r_\perp <$ 60 cm and 0 $<$ z $<$ 90 cm, the forward tracker continues to cover the region 90 cm $<$ z $<$ 264 cm. Table 2.2 summaries the radiation values for both the barrel and forward regions [4].

	Barrel		Forward	
	$r_\perp = 22$ cm	$r_\perp = 58$ cm	$r_\perp = 22$ cm z = 90 cm	$r_\perp = 39$ cm z= 264 cm
Dose	66.6 kGy	12.1 kGy		
Charged Hadron Fluence (π, κ, p)	11.9×10^{13} cm^{-2}	1.8×10^{13} cm^{-2}	13.5×10^{13} cm^{-2}	5.6×10^{13} cm^{-2}
Neutron fluence ($E >$100 keV)	3.5×10^{13} cm^{-2}	1.65×10^{13} cm^{-2}	3.6×10^{13} cm^{-2}	6.4×10^{13} cm^{-2}
Thermal neutrons	5.0×10^{13} cm^{-2}	5.09×10^{13} cm^{-2}		

Table 2.2: Radiation values for the silicon tracker

In the barrel the secondary particles (mostly charged pions) dominate the fluence over the albedo neutrons throughout, especially at low $r_\perp$. In the forward region there is a change from dominant charged pions (at low z) to albedo neutrons dominating the fluence near the ECAL endcaps (high z).

2.1.4.3 The Preshower environment

There are two moderators (each of 40 mm thickness) between the ECAL and the tracker. The Preshower is located between these two moderators and therefore has limited protection against the neutron flux of the ECAL compared to the protection given to the tracker. The moderator between the Preshower and ECAL provides a reduction in the albedo neutron fluence by a factor 2-3. Placing more absorbing material in this region (increasing the distance between the Preshower and the ECAL crystals) would compromise the energy resolution performance. The moderator on the tracker side of the Preshower gives further neutron moderation for the tracker but does little to help the Preshower.

Figure 2.3 shows the neutron and charged hadron fluence and absorbed dose as a function of pseudorapidity. Steep gradients are seen increasing with η and the limits are noted in Table 2.3.

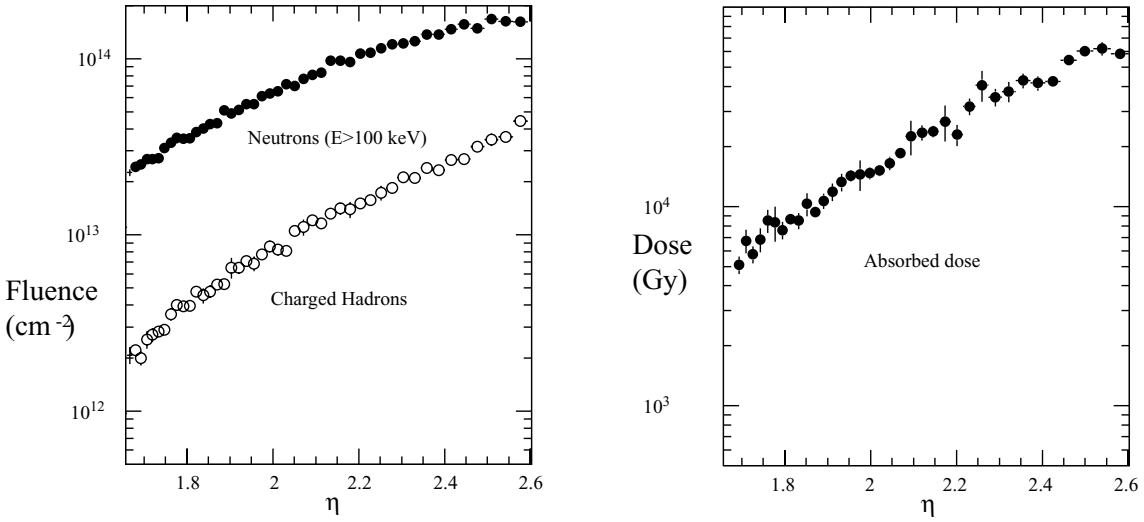

Figure 2.3: Neutron ($E > 100$ keV) and charged hadron fluence and absorbed dose in the Preshower as a function of pseudorapidity.

	$\eta = 1.6$	$\eta = 2.6$
Dose	5 kGy	60 kGy
Charged Hadron Fluence (π, κ, p)	2×10^{12} cm^{-2}	4.5×10^{13} cm^{-2}
Neutron fluence ($E > 100$ keV)	2×10^{13} cm^{-2}	1.8×10^{14} cm^{-2}

Table 2.3: Radiation values for the Preshower.

Further studies have been carried out investigating the energy spectra of particles in the Preshower. Figure 2.4 shows the energy spectra for neutrons, photons and charged hadrons in the Preshower.

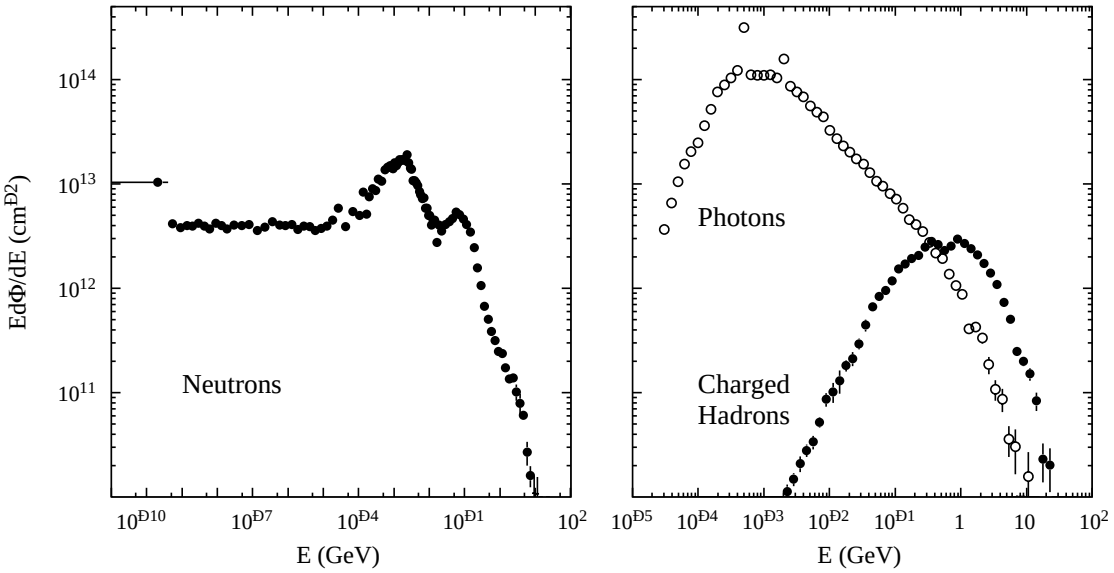

Figure 2.4: Neutron, charged hadron and photon energy spectra in the Preshower.

2.1.4.4 The ECAL and HCAL environments

The ECAL absorbs electromagnetic energy in the crystals through electromagnetic cascades. This continues along the length of the crystals. The dose along a crystal will therefore have a negative gradient. This can be seen in figure 2.5 for the barrel and figure 2.6 for the endcaps.

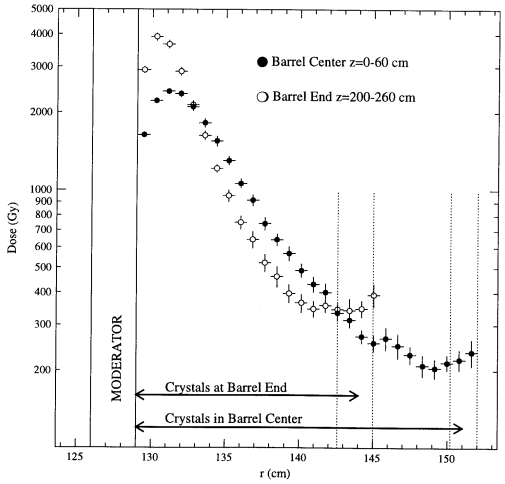

Figure 2.5: Total dose in the crystals at the centre and at the ends of the barrel [6].

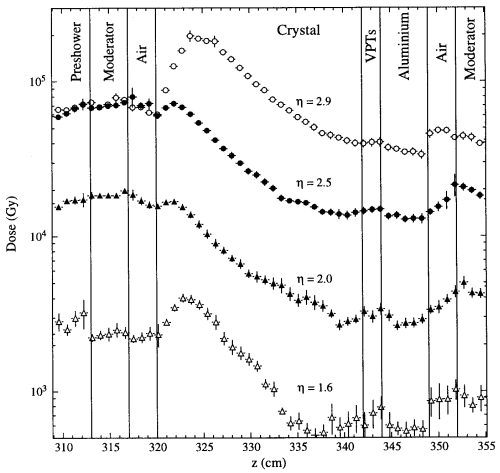

Figure 2.6: Total dose in the endcap crystals [6].

The negative gradient is less in the endcaps when compared to the barrel. This is due to a higher hadronic component which continues through to the HCAL.

The neutron fluence for the entire CMS endcap is shown in figure 2.7. The peak of the neutron source is clearly in the centre of the crystals. From there the neutrons are scattered both forward and back. A further moderator at z = 355 cm limits the neutron fluence for the ECAL electronics.

A second neutron source can be seen in the HCAL. The albedo neutrons from the HCAL are moderated at z = 385 cm again to protect the ECAL electronics.

Summarising radiation values in a table is difficult for the ECAL because of variations in η, z and $r_\perp$. Table 2.4 has been included to show maximum values in order to have some comparison to the other detector regions, precise values for a given region and further clarity can be found in [6].

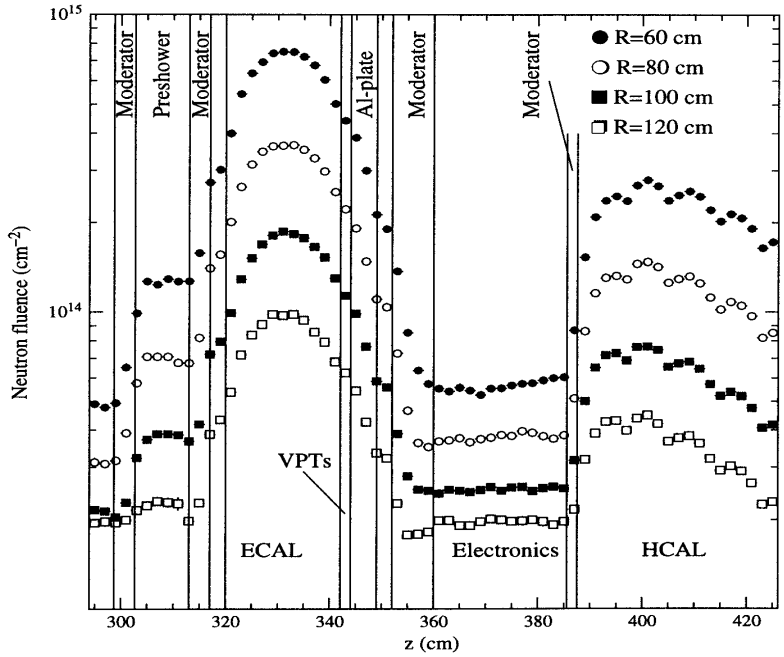

Figure 2.7: Neutron fluence ($E > 100$ kGy) in the CMS endcap calorimeters [6].

	Barrel	Endcaps	
		$\eta = 1.6$	$\eta = 2.9$
Dose	4 kGy	5 kGy	200 kGy
Charged Hadron Fluence (π, κ, p)	3×10^{11} cm^{-2}	3×10^{11} cm^{-2}	5×10^{13} cm^{-2}
Neutron fluence ($E > 100keV$)	1.5×10^{13} cm^{-2}	2×10^{13} cm^{-2}	7×10^{14} cm^{-2}

Table 2.4: Maximum radiation values for the barrel and endcap ECAL.

2.2 Radiation Damage in Electronic Devices

Cumulative[1] radiation damage in silicon devices can be classified into two types of phenomena. These are namely bulk effects and surface effects. Single event [2]induced radiation damage however involves a completely different transient charge deposition phenomena. This section first explores these three basic phenomena and then shows how bipolar and MOS device characteristics are degraded by these effects. It should be noted however that this is a complex subject with much on-going research. This section aims at gathering together the most important general concepts.

2.2.1 Bulk effects

Bulk damage in silicon is caused by disruption of the crystal lattice due to collisions between energetic particles in the radiation field and individual atoms in the silicon. The most abundant particles causing lattice damage in LHC will be neutrons, protons and pions. One such particle entering the silicon may collide with a silicon atom displacing it from it lattice site leaving a vacancy. If enough kinetic energy is transferred, the recoil atom will collide with other atoms in the crystal causing a cascade.

When an atom eventually comes to rest it is likely to be at an interstitial position. The type of defect formed depends on the combination of vacancies, interstitial atoms and/or impurity atoms in the crystal either by doping or contamination. A list of the possible defects is shown in table 2.5 [8] .

Type of defect	Components
Schottky defect	Single vacancy
Interstitial	Si interstitial
Frenkel defect	Interstitial + vacancy
Divacancy	Vacancy + vacancy
Substitutional Impurity	P and B doping, O and C contamination
Impurity-vacancy complex	p- vacancy

Table 2.5: List of possible defects in the silicon crystal lattice

At room temperature a number of these defects are unstable in that some interstitial atoms may soon slip back into a vacancy. However a number of defects remain stable for significant lengths of time.

The defects introduced in silicon by doping with Boron (B) or Phosphorus (P) have the deliberate and finely controlled effect of introducing discrete energy levels within the bandgap which become donor or acceptor levels. Defects due to radiation damage

[1]Cumulative radiation damage is the gradual deterioration of the silicon crystal, SiO_2 and the Si/SiO_2 interface occurring throughout the entire exposure duration of the device to irradiation.

[2]Single event effects (SEE) are due to energy deposition from a single high energy particle passing through the device. The induced damage is therefore instantaneous and can happen at any time during exposure.

can also have energy levels within the bandgap. It is these electrically active defect states (centres) that affect the electrical behaviour of the device.

There are five basic effects that can occur due to the presence of these defect centres and are shown schematically in figure 2.8 [9].

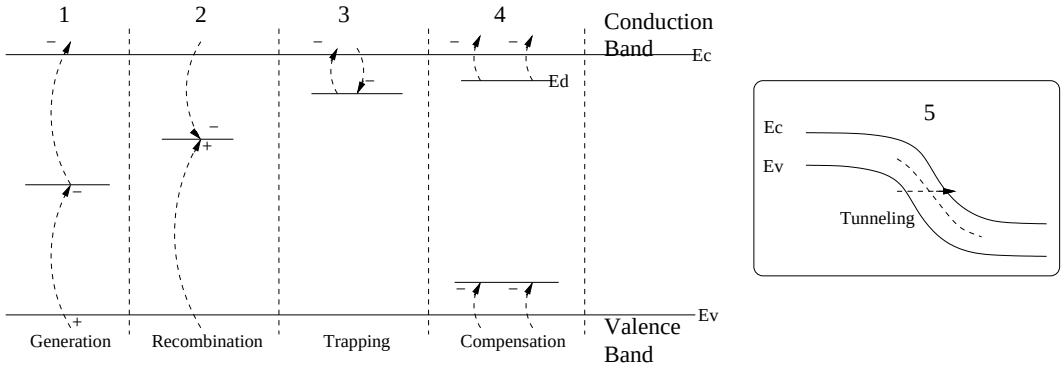

Figure 2.8: Effects of defect centres in silicon

The first of these shows an acceptor level near the middle of the band gap. Thermal excitation can result in electrons gaining enough energy to jump first to the defect centre and then into the conduction band. This is known as carrier generation. The result is free electrons in the conduction band and free holes in the valence band. This is a particularly important mechanism in the depletion region contributing to device leakage currents.

Recombination (shown as the second example) involves the capture of a free carrier (hole or electron) at the defect centre followed by capture of a free carrier of the opposite sign. This has the effect of reducing the mean time that minority carriers spend in the conduction band (minority carrier lifetime τ_b). Since the current gain (β) of a bipolar transistor is proportional to τ_b then β will be reduced due to this effect.

The third effect shows the trapping of free electrons in the conduction band followed by release some time later through thermal excitation.

The fourth effect results in a modification of majority carrier concentration and hence doping profile. In this case the doped donor level is compensated by radiation induced defects acting as acceptors and forming an acceptor level. This reduces the effective doping (N_{eff}) and can eventually reverse the initial doping profile. This is a very important mechanism causing type inversion in silicon sensors.

The fifth example involves defect assisted tunnelling through a potential barrier such as a pn junction. This effect contributes to the reverse leakage current through a junction. It is important to both silicon sensors and bipolar transistors.

2.2.2 Surface effects

Elements in group IV of the periodic table such as silicon, carbon and germanium have four electrons. In order to form a stable configuration of eight, each of the 4 electrons is shared with a neighbouring atom forming covalent bonds. Atoms along the

top plane of the crystal will have unconnected bonds (dangling bonds). If left exposed, impurities will quickly attach themselves to these dangling bonds. If exposed to an atmosphere of oxygen then silicon dioxide (SiO_2) will form on the surface. Silicon dioxide has a large band gap and hence forms a very good insulator for use as a capacitor dielectric, MOS gate oxide and as an insulator between conducting planes.

It is however difficult to form a perfect interface between the silicon and oxygen atoms and often defects occur due to remaining dangling bonds or impurity atoms, figure 2.9 [8].

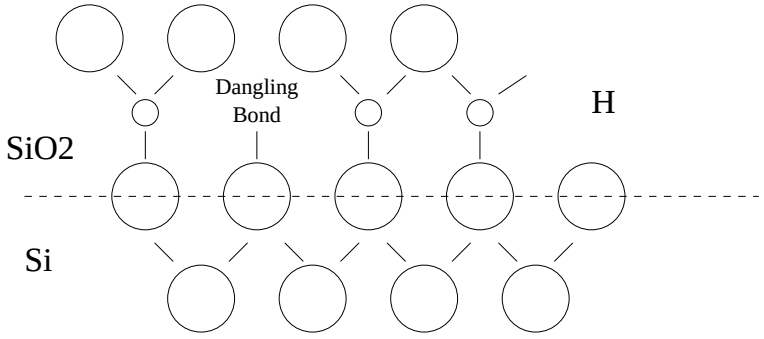

Figure 2.9: Defects at the Si/SiO_2 interface forming interface traps

Defects at the interface form interface traps which contribute to the potential barrier across the dielectric of a MOS capacitor and can act as traps for the minority carriers in a channel close to the surface of the silicon. In a MOS device these two mechanisms alter the threshold voltage (V_t) and carrier mobility (μ) respectively.

Radiation further enhances the charge build-up in the oxide. Consider figure 2.10 [10] which shows the band structure for a MOS capacitor ie. metal, silicon dioxide and silicon from left to right.

Ionising radiation passing through the oxide will produce electron-hole pairs. Free electrons are much more mobile than holes in silicon dioxide and those that do not immediately recombine will be swept by the electric field towards the positive electrode within the order of a pico second. The holes on the other hand will make their way towards the other electrode over a period of time in the order of a second. Continuous radiation results in a continuous build-up of positive charge in the oxide. Some of these holes will eventually recombine and others will become captured by traps in the oxide.

2.2.3 The dominant radiation effects in a MOS transistor

Surface effects are most important in MOS devices. The threshold voltage (V_t) of a MOS transistor is defined as the minimum voltage necessary (as applied to the gate) to cause strong inversion within the silicon under the gate, ie form a channel through which current may flow. Figure 2.11 shows a cross section of an NMOS transistor in strong inversion. In this example there is also a lateral field set up such that the channel in pinched off at the drain. In this condition a maximum current is reached

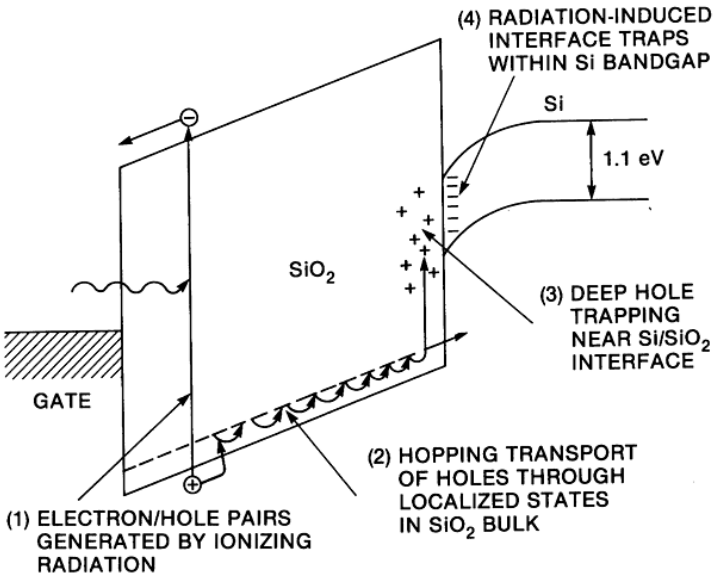

Figure 2.10: Cross section and band model of ionisation and charge transport within a MOS capacitor [10].

for a given gate voltage (V_{gs}). The device is said to be in saturation which occurs when $V_{ds} > V_{gs} - V_t$.

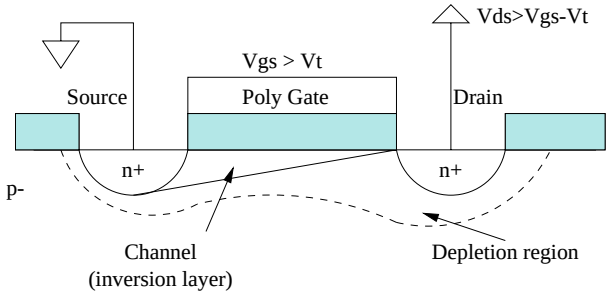

Figure 2.11: Cross section of an NMOS transistor in strong inversion and saturation

In an ideal device the voltage necessary to achieve strong inversion (V_i) is expressed as in equation 2.2 [10].

$$V_i = 2\phi_b + \frac{2\sqrt{qN_A\varepsilon_s\phi_b}}{C_{ox}} \tag{2.2}$$

where:

- $\phi_b = \frac{(E_i - E_f)}{q}$,
- E_i is the intrinsic Fermi level (ie. middle of the band gap),
- E_f is the actual Fermi level,

- q is the electron charge,
- N_A the doping concentration,
- ε_s the permitivity of silicon,
- C_{ox} the capacitance of the oxide such that $C_{ox} = \frac{\varepsilon_{ox}}{T_{ox}} A$,
- ε_{ox} the permitivity of silicon-dioxide,
- T_{ox} the thickness of the oxide,
- A the area of the gate oxide.

In a real device the terms due to potential barriers between the gate and the silicon need to be added. These are the metal-semiconductor work function (φ_{ms}), potential due to trapped charge in the oxide (Q_{ox}) and interface trapped charge (Q_{it}). The threshold voltage (V_t) can then be expressed as equation 2.3.

$$V_t = 2\phi_b + \frac{2\sqrt{qN_A\varepsilon_s\phi_b}}{C_{ox}} + \varphi_{ms} - \frac{Q_{ox}}{C_{ox}} - \frac{Q_{it}}{C_{ox}} \tag{2.3}$$

Q_{ox} is generally positive whilst Q_{it} can be negative since the interface traps may act as acceptors trapping electrons. The balance between the two can change throughout irradiation and annealing. In some cases (where Q_{ox} dominates) a negative shift in V_t can be observed. Further charge build-up could eventually lead to the V_t becoming negative making it impossible to turn off an NMOS transistor as illustrated in figure 2.12.

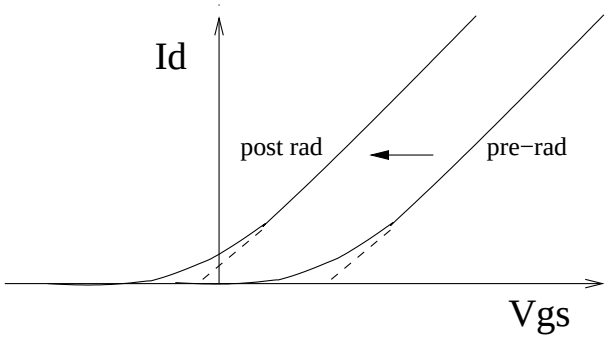

Figure 2.12: NMOS threshold voltage shift through irradiation.

The magnitude of the charge build-up in the oxide depends strongly on the thickness of the gate oxide. At the edge of the transistor (figure 2.13) there is a region known as the "Bird's Beak" region which has a substantial increase in the thickness of the oxide in contact with the p- region. After ionising radiation, charge build-up in this region can be more significant than in the rest of the gate and can cause inversion and hence current flow from source to drain along the edge of the transistor. Effectively

there are a number of parasitic NMOS transistors with reducing V_t in parallel along the edge which will cause leakage sooner than the rest of the device when exposed to ionising radiation.

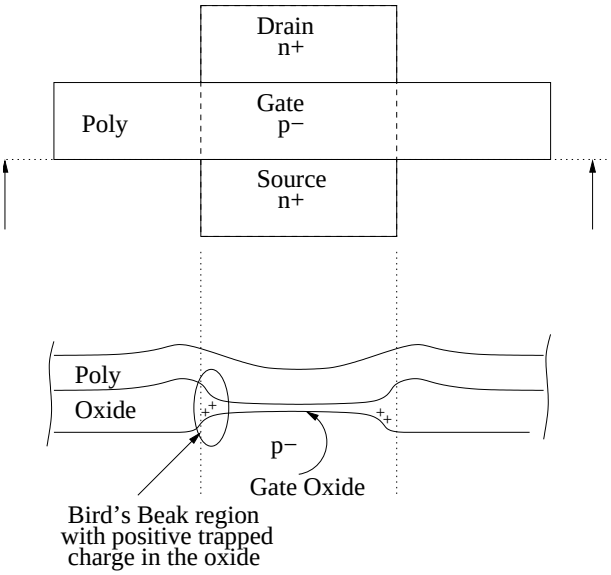

Figure 2.13: Charge build-up through ionising radiation can be more significant in the "bird's beak" region of a transistor than in the gate causing current leakage from source to drain along the transistor edge.

Some processes improve this region by increased p+ doping under the bird's beak region (p+ channel stop). This means that a higher level of charge deposition would be necessary in the oxide to cause inversion.

2.2.4 The dominant effects of radiation in a bipolar device

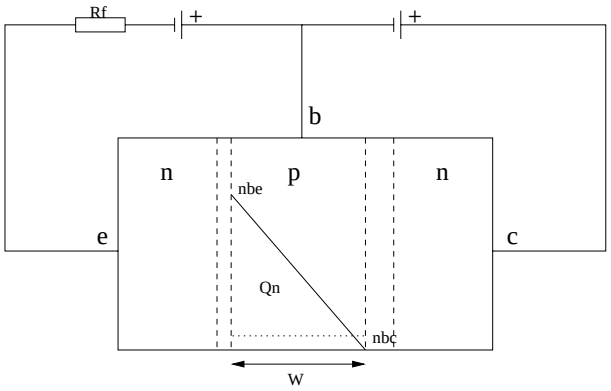

Figure 2.14: An NPN bipolar device with the base/emitter junction forward biased and the base/collector junction reversed biased.

A bipolar device is based on minority carrier current flow through a base (b) region located between two pn junctions, the emitter (e) and collector (c). When an NPN or PNP structure is biased such that the be junction is forward biased and the bc is reversed biased (as in figure 2.14), density gradients of both majority and minority carriers are set up within the base region. Majority carrier current flow is blocked by the reversed biased bc junction and hence no electric field exists within the base ($\frac{dE}{dx} \approx 0$). Space charge neutrality exists and the minority carrier base charge Qb is matched by an equal and opposite majority base charge such that the total base charge is zero. Current flow through the device is through minority carrier diffusion governed by the minority carrier density gradient in the base. This, in turn, is controlled by the base width and bias.

An ideal bipolar device would have infinite base resistance and therefore have infinite current gain (β), ($\beta = \frac{Ic}{Ib} = \infty$).

In reality some of the electrons from the emitter combine with holes within the base region (recombination). A small base current is therefore necessary to replace the lost holes in the base and maintain bias. The effect of recombination is therefore a non zero value for Ib and a definite value for β. A normal NPN device can have a (β) in the range 100-200.

A more analytical way to express this is to refer to minority carrier lifetime [3] (τ_b) which would be infinite in an ideal device but has a finite value due to recombination in a real device. Equation 2.4 shows the relationship between β, τ_b and the minority carrier transit time [4] (τ_t). τ_t itself is given in equation 2.5 where Q_b is the minority carrier base charge, W the base width and D_n the diffusion constant for electrons which is related to mobility (μ) by Einstien's relation 2.6.

$$\beta = \frac{I_c}{I_b} \approx \frac{\tau_b}{\tau_t} \tag{2.4}$$

$$\tau_t = \frac{Q_b}{I_c} \approx \frac{W^2}{2D_n} \tag{2.5}$$

$$\frac{D_p}{\mu_p} = \frac{D_n}{\mu_n} = \frac{kT}{q} \tag{2.6}$$

(β) is the most important bipolar device parameter to monitor when the device is exposed to radiation. Both bulk effects and surface effects play important (but independent) roles in the radiation damage of a bipolar device.

Exposure to neutrons, pions and electrons will lead to increased recombination in the base region due to the creation of traps from displacement damage through the

[3] Minority carrier lifetime (τ_b) is defined as the average time interval between generation and recombination of a minority carrier in a homogeneous semiconductor volume.

[4] Minority carrier transit (τ_t) is the average time it takes for a minority carrier to cross the base region from emitter to collector in a bipolar device.

mechanism described in 2.2.1. This will therefore lead to a decrease in τ_b, an increase in Ib and hence a decrease in β.

The extent of β degradation due to bulk effects can be kept to a minimum by selecting a device structure with a narrow base width. Figure 2.15 shows typical NPN and PNP structures in a bipolar technology optimised for a vertical NPN device. The vertical NPN has a narrow base width whilst the lateral and substrate PNP device have wide base widths. These latter two structures should therefore be avoided in radiation tolerant technologies.

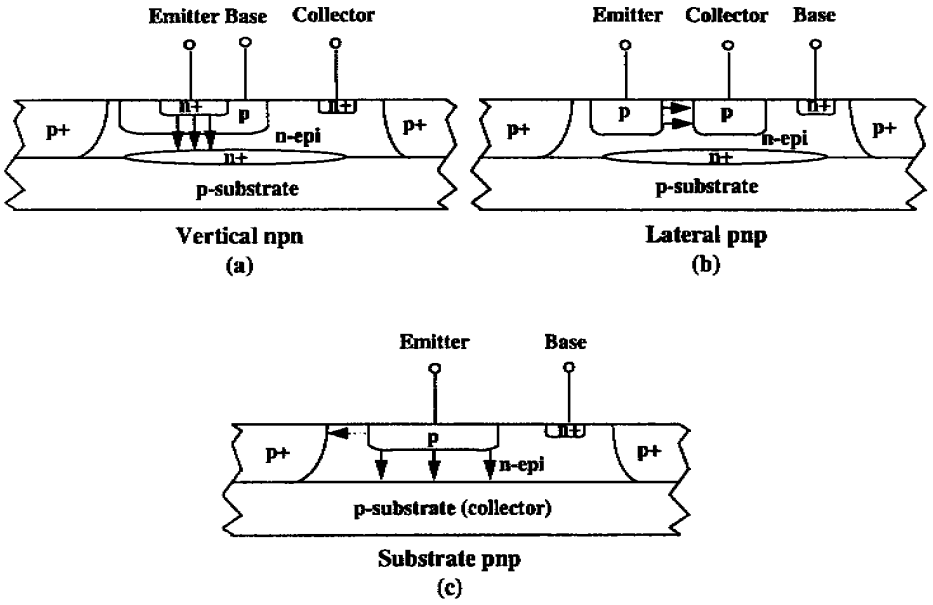

Figure 2.15: Typical structures for a process optimised for the vertical NPN [11].

Surface effects become important when the device is exposed to ionising radiation. Radiation induced positive charge build-up (as described in section 2.2.2) in the SiO_2 can induce an inversion layer in adjacent lightly doped "p type" silicon (p-) in a similar way to that described for a MOS device in section 2.2.3. This can be the case for lateral PNP devices as in figure 2.15 but can also be a problem in less obvious structures. Figure 2.16 shows trapped positive charge in the field oxide of a walled NPN device. An inversion layer in the p- region adjacent to the oxide could form a channel of electrons from emitter to collector. Another source of radiation induced leakage is shown in figure 2.17. Figure 2.17 shows a trench isolation structure between two devices with a p+ channel stop at the bottom. Again positive charge build-up in the thermal oxide can lead to the formation of a conducting channel near the interface producing leakage.

The extent of β degradation due to surface effects can be kept to a minimum by selecting device structures that minimise the p- to SiO_2 interface area. Technological factors that can help are increased doping levels and thin oxides.

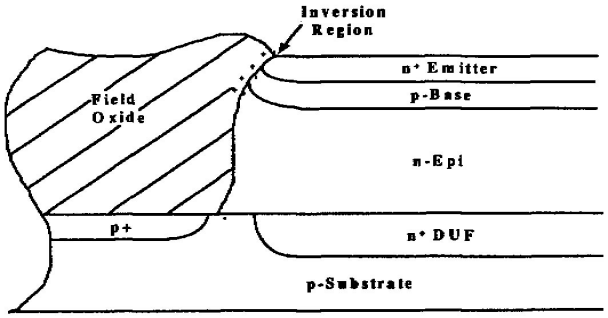

Figure 2.16: Positive charge build-up in a field oxide leading to a conducting channel of electrons from emitter to collector [12].

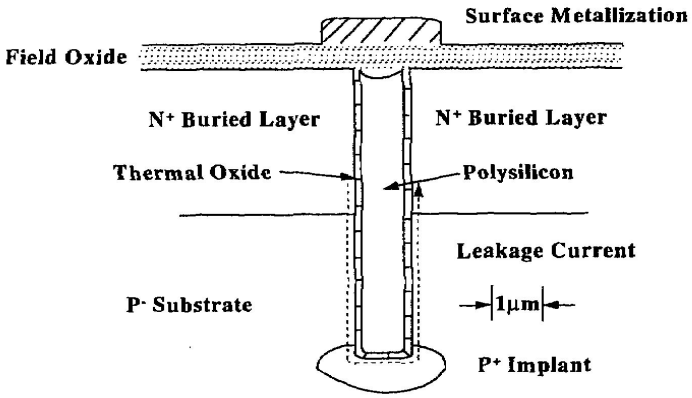

Figure 2.17: Leakage across a trench isolation structure due to positive charge build-up in the SiO_2 forming a conducting channel [13].

2.2.5 Transient behaviour - single event effects

An energetic charged particle passing through material will cause ionisation along its track as already discussed. The amount of ionisation is determined by the stopping power or Linear Energy Transfer (LET) normally expressed in silicon in units of eV $mg^{-1}cm^2$. LET is defined as the local rate of energy deposition along a particle track $\frac{dE}{dx}$ [14]. The key word is "local" since different particles of the same energy may have different LETs due to the spread of energy deposition. The factors that determine the LET are particle energy, atomic number and the material through which the particle passes. Figure 2.18 shows how particles of the same energy can have different LETs.

High LET values are seen for heavy ions in the energy range of 1 MeV. It is difficult to predict how many of these high LET particles will exist in LHC since protons and neutrons may initiate nuclear reactions within material in the experiment producing free ions.

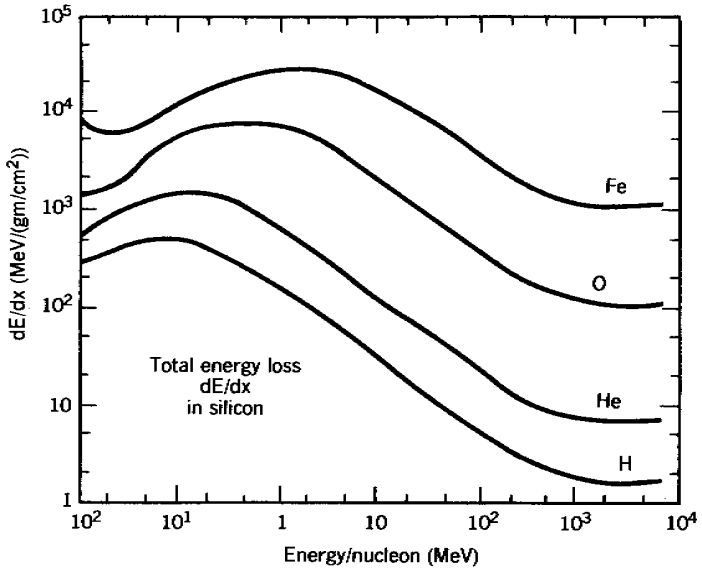

Figure 2.18: LET ($\frac{dE}{dx}$) for ions of increasing atomic numbers (moving upwards) in silicon [15].

Particles with high LET can produce very dense plasma funnels of holes and electrons within the silicon reducing the local resistivity allowing current to flow. The charge may also be picked up by one particular node in the circuit altering the voltage level at that node. These two phenomena can result either in a temporary disturbance to signal levels within the circuit or to short circuit currents which may destroy the chip completely.

2.2.5.1 Single event upset

Figure 2.19 shows an ion passing through the pn junction of the drain of a MOS transistor. Along its track a dense plasma of electrons and holes are produced such that the number of carriers in the funnel exceed the majority carrier concentration of the bulk silicon. Under these conditions electrons and holes that do not recombine will drift in opposite directions due to the electric field. The density of carriers in the funnel will reduce and the resistivity increase causing the drift process to stop. The remaining charge will then be collected via diffusion.

The total charge collected at the drain can change the voltage of that node significantly. In a digital circuit the voltage spike produced could be enough to cause a change of state in a gate attached to that node. The result is possible race conditions or permanently altered states . The later (known as an "upset") can occur if feedback is used in the logic (such as a cross coupled inverter in a memory cell) or if the input to a gate is floating (common in dynamic logic).

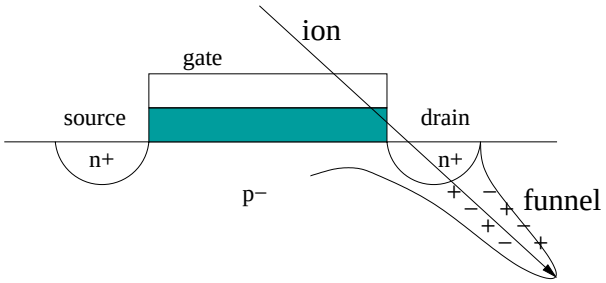

Figure 2.19: Creation of a funnel of electrons and holes.

2.2.5.2 Transient induced latch-up

Latch-up is a destructive phenomena in integrated circuits, the mechanisms of which have been known for a long time [16]. Design engineers have well defined design rules to reduce the probability of latch-up in microelectronic circuits. In a radiation environment however these rules are not sufficient since transient effects can act as a trigger for a latch-up condition. Latch-up is a large uncontrolled current flow between the power supplies of a chip due to a parasitic bipolar Silicon Controlled Rectifier (SCR) circuit that exists in bulk CMOS technologies.

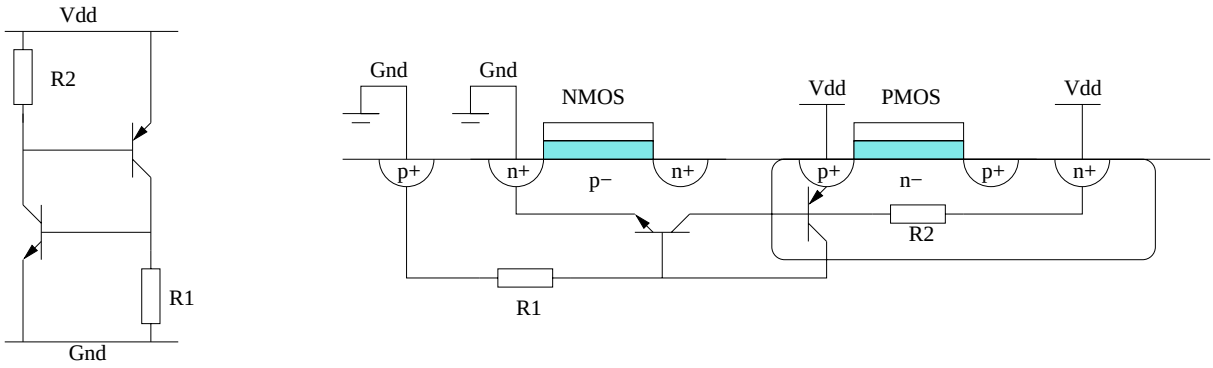

Figure 2.20: Latch-up mechanism, SCR circuit (left), parasitic SCR in bulk CMOS (right).

Figure 2.20 shows both the SCR circuit and a similar parasitic SCR in bulk CMOS. If both transistors are off then the circuit is stable and very little current will flow. If however a junction in one of the bipolar transistors is forward biased then positive feedback can occur switching both devices hard on and effectively short circuiting the power supplies. The conditions for positive feedback are that the product of the β of the two bipolars must be greater than 1 and the resistors high enough to cause a significant voltage drop for a small initiating current. In standard CMOS design the most important design rule is to have many substrate contacts as possible within a minimum distance from the NMOS or PMOS transistor hence keeping R_1 and R_2 to a minimum. The exact rule depends on the doping concentrations of the technology. In a radiation environment where single event effects are possible, minority carriers

may be injected into the base region of one of the parasitic bipolars due to a strike of a high LET particle. The parasitic SCR may then be triggered resulting in circuit malfunction and possibly burn out of the chip. Latch-up triggered by a single event is known as “Single Event Latch-up” (SEL).

2.3 Technological Options with respect to Radiation Tolerance

The evolution of technologies suitable for high radiation environments has been very intensive during the last decade. Ten years ago most of the development of radiation hard technologies took place behind closed doors, funded by individual government defence budgets. The end of the cold war reduced the need for such classification on these projects and HEP labs were able to gain access to some of the technologies. Most however, were digital technologies designed to withstand extremely high dose rates from nuclear explosions.

At this time standard bulk CMOS technologies could only withstand 100 krad(Si) or so of ionising radiation before failure. Various R&D projects were set up within the HEP community to characterise the ex-defence processes for analog performance before and after irradiation similar to that expected within LHC. The bench mark total dose target was 10 Mrad(Si) of ionising radiation.

The various types of technologies that existed at that time were modified bulk processes, thin film Silicon On Insulator (SOI) and thick film SOI.

More recently however, the continued advancement in main stream IC processes (in particular the scaling down of device size and gate oxide) has lead to the possibility of radiation tolerant design in a standard CMOS process providing certain design rules are adhered to.

This section provides a review of the data published on these various technologies and concludes with the strategy adopted for the CMS Preshower.

2.3.1 Modified bulk CMOS

The main goals of a CMOS radiation tolerant process are low V_t shift, no leakage between devices and reduced sensitivity to SEE.

The Harris AVLSIRA [17] technology was a CMOS 1.2 μm process that had an n+ epitaxial layer in an n- substrate to guard against SEL and reduce sensitivity to SEU. Isolation between devices was achieved through a modified LOCOS. The gate oxide thickness and the resulting V_t shifts were reported [18] at T_{ox} =25 nm and ΔV_t <300 mV for a total dose of 10 Mrad.

2.3.2 Thin film SOI technologies

Silicon on insulator (SOI) technologies offer the possibility of completely isolating n and p transistors hence blocking the SCR mechanism that triggers latch-up. SOI technologies can therefore be made "latch-up free" and are hence good candidates for radiation tolerant design.

The starting material is most often a SIMOX wafer which is produced through implantation of oxygen ions to form a buried oxide as in figure 2.21. The film of silicon above the oxide is used for device processing whilst the silicon beneath the oxide is

intended merely as a mechanical support however its charged state can influence the transistor characteristics.

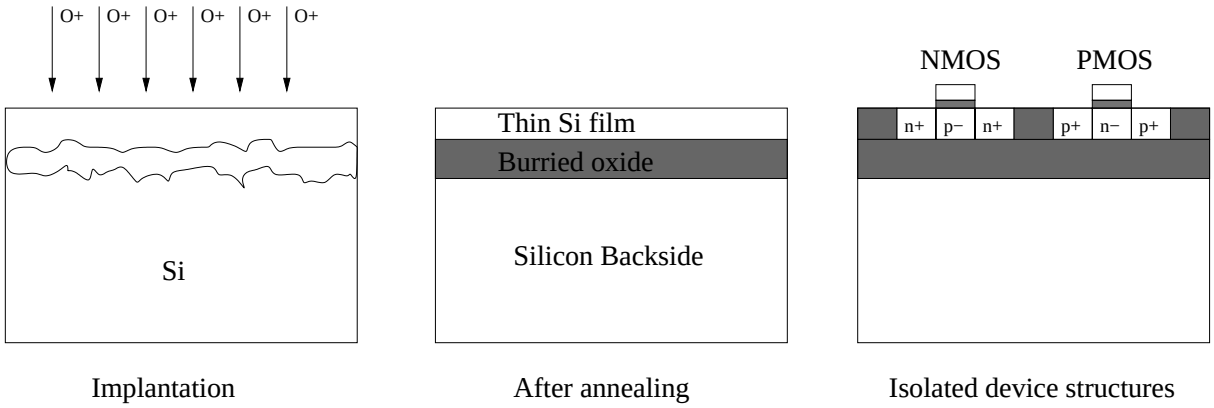

Figure 2.21: Fabrication of CMOS devices on a SIMOX substrate.

Figure 2.21 is a typical cross section of a thin film process. The transistor doping of source, body and drain continue down to the buried oxide. Each transistor is completely isolated from its neighbour eliminating device to device leakage.

One such process was studied at CERN. It was the HSOI3HD [19, 20, 22, 23] process manufactured by Thomson TCS. The process consisted of 1.2 μm minimum gate length CMOS devices in a silicon film of thickness 150 nm. The gate oxide thickness $T_{ox} = 23$ nm and the buried oxide is 380 nm thick.

Measurements showed V_t shifts of ΔV_{tn} =250 mV and ΔV_{tp} =350 mV after 25 Mrad(Si) of ionising radiation and reductions in transconductance of $\Delta gm_n = -44\%$ and $\Delta gm_p = -18\%$.

Source to drain leakage along the bird's beak (as described in section 2.2.3) can be solved by avoiding a continuous edge of the p- body running under the gate from source to drain. There are a number of layout structures that can achieve this using different configurations of two main techniques. The first is by introducing a p+ diffusion interrupt between source and drain touching the p- body. Two examples that include this technique are shown in figure 2.22. Structure (a) is bidirectional in that the source and drain are inter-changeable whereas structure (b) defines the source since the body and source are connected together. The second technique is to use an "edge-less" transistor layout structure which avoids completely a p- edge running under the gate between source and drain. An example of an edgeless device is shown in figure 2.23 where the gate encloses the source/drain completely. All of the transistors used in the design of circuits in this technology were based on these layout techniques.

The nature of the SOI process however, brings complications as well as advantages. The advantages are immunity to SEL and complete device to device isolation. The complications are now described.

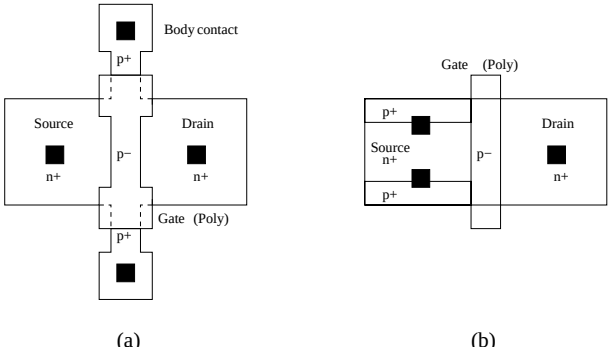

Figure 2.22: Two layout structures for a NMOS device showing the body contacts. Structure (a) is bidirectional (source and drain are inter-changeable), structure (b) defines is unidirectional where the source must be connected to ground.

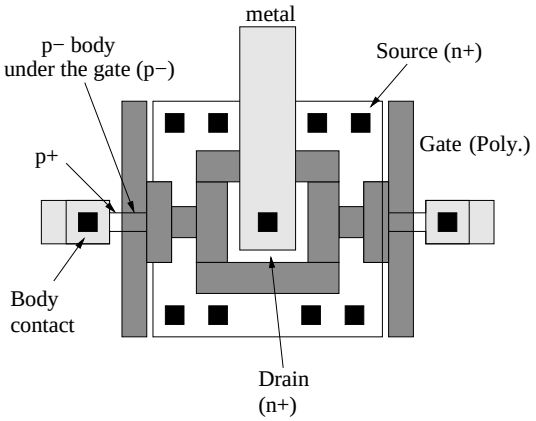

Figure 2.23: An edge-less transistor structure.

An effect known as the kink effect is a sudden increase ("kink") in the drain current (I_d) as the drain-source voltage (V_{ds}) is increased in the saturation region for a given gate voltage (V_{gs}), figure 2.24. The effect occurs in NMOS transistors when the longitudinal electric field accelerates electrons to a high enough velocity to cause the generation of electron/hole pairs near the pinch-off region of the channel. The electrons generated are collected by the drain contact while the holes are forced to enter the body region. If the body is left floating then the injection of holes increase the body potential. An increase in body potential decreases the threshold voltage causing an increase in drain current.

This is not an issue for digital design but makes the control of analog circuits difficult. The effect can be reduced by connecting the body of the transistor to a well defined potential (ie. ground) in order to collect the holes. Figures 2.22 and 2.23 include body contacts.

Whilst solving one problem, the addition of a body contact adds another effect which is a "hump" in the noise spectrum, figure 2.25. Figure 2.25 shows that in addi-

tion to the $1/f$ (flicker) and white noise components there is an additional component which has the shape of a hump.

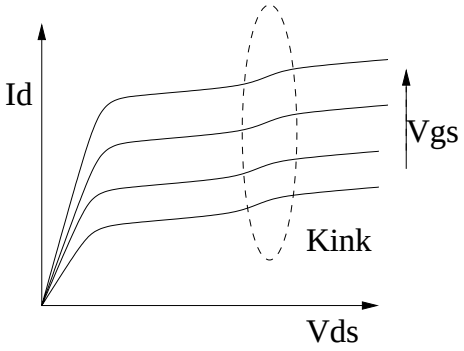

Figure 2.24: "Kink Effect" Evidence of a sudden increase of drain current (I_d) with respect to drain-source voltage (V_{ds}) in the saturation region

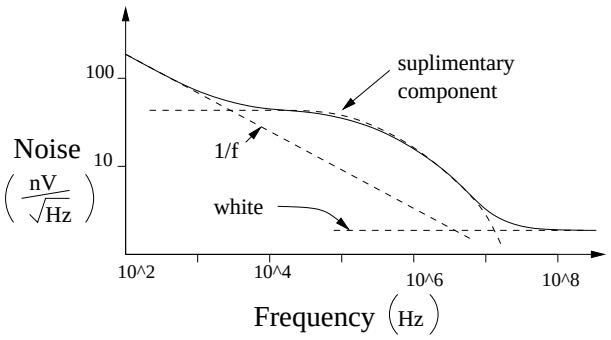

Figure 2.25: Noise spectrum of a transistor in saturation showing the contribution of a third noise component in addition to the 1/f and white noise.

As a demonstrator circuit, a current to voltage amplifier was designed and measured after 20 Mrad(Si) of ionising radiation [21]. The circuit continued working after irradiation showing a gain degradation of 23%, an increase in noise of 34% (parallel noise), and 60% (series noise).

Another thin film process is the Honeywell RICMOS IV CMOS 0.8 μm [24] which has a silicon film thickness of 200 nm, buried oxide thickness of 400 nm and t_{ox} =15 nm. Circuits are reported as functional at 1 Mrad(Si) [25] with threshold shifts of ΔV_{tn} <50 mV at 1 Mrad. A more modern process with minimum gate length of 0.35 μm is now available from the same manufacturer but at high cost.

2.3.3 Thick film SOI technologies

Thick film SOI technologies also generally use a SIMOX substrate. The implantation of the oxygen ions however is deeper leaving a thicker film of silicon for the processing of devices.

In the first half of the 1990's, a thick film BiCMOS technology was developed specifically for H.E.P. applications and applications in space by the French Atomic Agency (CEA). The process is called DMILL. Figure 2.26 shows the cross section of the DMILL technology. NMOS, PMOS, vertical NPN bipolars and PJFETs (not illustrated) are available in the technology. The devices are created in the top layer of the silicon film and do not extend down to the buried oxide. The devices are hence

more like that of a bulk technology on top of a SIMOX substrate. Isolation between devices is obtained by trench isolation. This together with the buried oxide block SEL. The minimum gate length of the technology is 0.8 μm and the gate oxide thickness t_{ox} =18 nm.

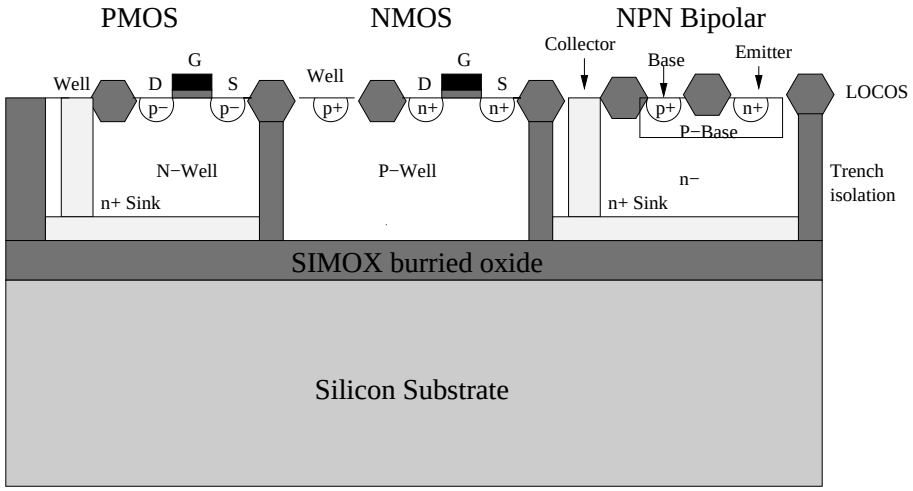

Figure 2.26: Cross section of the DMILL BiCMOS thick film SOI technology.

The resulting radiation tolerance of the technology is reported [27] as ΔV_{tn} <-90 mV and ΔV_{tp} <-130 mV after 10 Mrad. The MOS transconductance reduces by $\Delta g_{mn} = -25\%$ and $\Delta g_{mp} = -6\%$. The current gain β of the NPN device is reported as degrading from 150 to 130 after 10 Mrad(Si) of ionising radiation and $\Delta\beta = -35\%$ after exposure to a neutron fluence of 1×10^{14} n cm^{-}2 with a collector current of 100 μA .

The research in the technology gained support from CERN in the way of a research and development program RD29 [28] with requests to stabilise and then industrialise the technology for use within the HEP community. The process was hence transfered to a 6 inch foundry of MHS in Nantes, France own by TEMIC and made available for HEP use in 1997. TEMIC has since been bought by ATMEL [29].

2.3.4 Deep sub-micron technologies

For CMOS devices, the main physical process that causes degradation after radiation is charge build-up in the oxide (either gate oxide or LOCOS) and the creation of interface states. It is logical therefore to predict that thinner gates will have less total charge in the oxide and will as a consequence show less threshold voltage shift after irradiation. What is not logical however is the effect shown in figures 2.27 and 2.28 which were discovered by Saks et al. [30] when studying radiation induced oxide charge with respect to oxide thickness during the mid 1980's.

The figures show the increase in oxide trapped charge measured through flatband voltage shifts (ΔV_{fb}) for MOS capacitors of different oxide thickness. For t_{ox} >20 nm, $\Delta V_{fb} \propto t_{ox}^2$ but for $t_{ox} < 10$ nm the measured ΔV_{fb} values were orders of magnitude

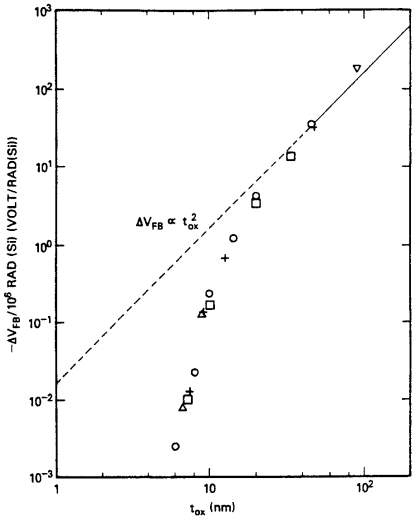

Figure 2.27: Flatband voltage shift per Mrad(Si) measured for MOS capacitors of different oxide thicknesses. The measurements were made at $80^o k$, [30]

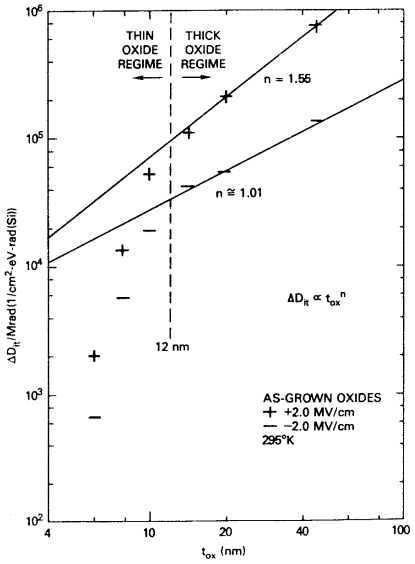

Figure 2.28: The density of interface states per Mrad(Si) for MOS capacitors of different oxide capaictors, measure at $80^o k$, [31]

less than would have been expected. Further studies on the increase of interface states for very thin oxides showed a similar behaviour, figure 2.28 [31]. The explanation given was that for very thin oxides, electrons can tunnel into the oxide from either the polysilicon gate or the silicon substrate neutralising the trapped holes. Threshold voltage shifts for thin oxides should therefore reduce dramatically for very thin oxides. It was hence predicted at this time that future microelectronics technologies with oxides <10 nm would be more resistant to radiation.

Technological advancement within the microelectronics industry has shown the number of minimum cost components per IC doubling each 18 months following Moore's Law [32, 33] from approximately ten thousand devices in 1975 to more than ten million transistors in 2000 and is predicted to continue the trend to ten billion in 2014 [34]. The scaling down of device size and power supply voltage in order to meet this expansion of component density includes the thinning of the gate oxide. A few years ago mainstream commercial CMOS processing reached 0.25 μm minimum gate length. The gate oxide thickness was 5.5 nm and hence within the low ΔV_{fb} region shown above.

A study of the radiation hardness properties of these "Deep Sub Micron" technologies was started at CERN. The process studied was a twin well CMOS technology

with shallow trench isolation between devices. The minimum. gate length was 0.25 μm, t_{ox} =5.5 nm and power supply voltage = 2.5 V.

Edgeless transistors structures (as described in section 2.3.2 figure 2.23 but without the need for body contacts) to avoid leakage along the bird's beak (section 2.2.3)were used. In addition, a p+ diffusion guardring around each NMOS transistor is necessary to block a radiation induced leakage path from one device to another. Figure 2.29 shows the layout of an inverter [37].

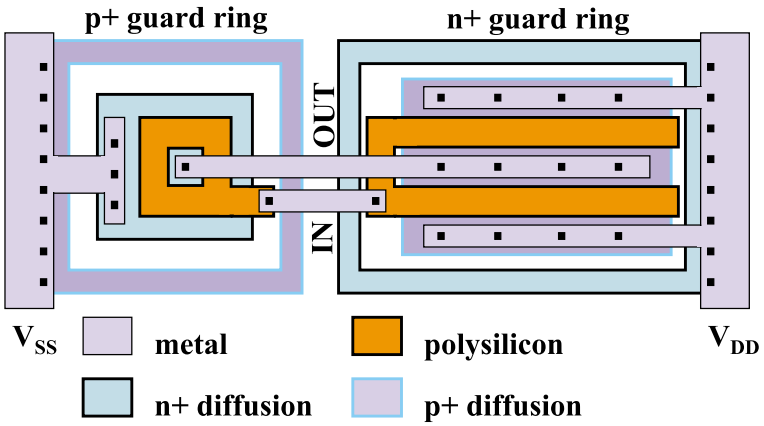

Figure 2.29: Layout of an inverter using an NMOS edge-less device structure surrounded by a p+ guardring [37].

The resulting radiation hardness is quite remarkable [35]. The threshold voltage shifts were measured at: ΔV_{tn} =15 mV and ΔV_{tp} =-30 mV for a total dose 10 Mrad(Si) and ΔV_{tn} =35 mV and ΔV_{tp} =-70 mV for 30 Mrad. The gm_n degradation was 6% at 30 Mrad. The increase in noise after 100 Mrad(Si) was 15% for a n-channel and 7% for a p- channel, dominated by the white noise component.

The resistance to single event effects was reported in [36]. Several types of shift registers were designed and exposed to heavy ions with an LET adjusted from 3.2 to 89 MeV cm^{2}mg^{-1}. Test patterns were clocked in and out of the registers at 30 MHz and the errors counted for different LET settings in order to assess the sensitivity to SEU. The cross section (σ) of the circuit can then be calculated as in equation 2.7 where N_{events} is the number of events counted, N_{bits} the number of storage nodes in the circuit and Φ the fluence. The units are cm^2/bit.

$$\sigma = \frac{N_{events}}{\Phi N_{bits}} \tag{2.7}$$

The cross section (σ) was then plotted against the LET with a fit to a Weibull curve and the results are shown in figures 2.30 and 2.31.

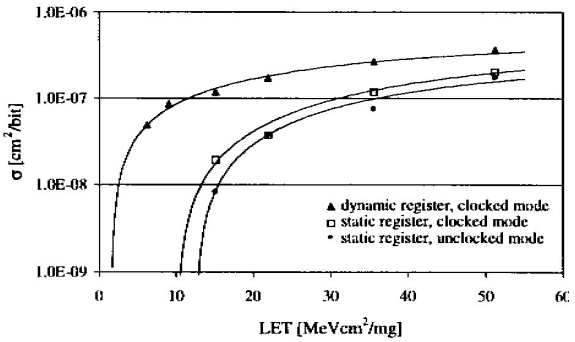

Figure 2.30: Measured cross section (σ) verses LET for both dynamic and static shift registers within an ion beam [36].

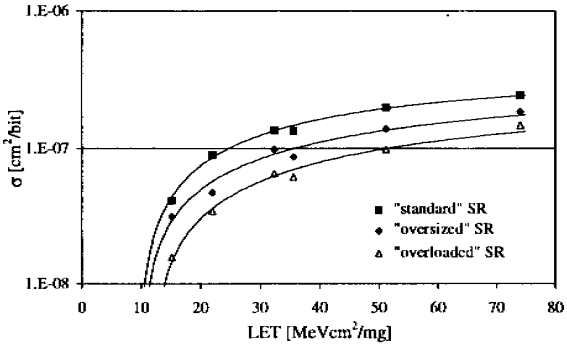

Figure 2.31: Measured cross section (σ) verses LET for different static designs within an ion beam [36].

No latch-up was observed during the duration of the entire exposure. A high level of resistance to SEL is expected due the fortunate side effects of modern processing techniques, such as an epitaxial substrate, retrograde wells and trench isolation [5] [37].

[5] An epitaxial substrate is a highly doped substrate on top of which lies a lightly doped region for the processing of the electronics. This reduces the resistance of the substrate ie. reduces the values of the parasitic SCR resistors (2.2.5.2). It also limits the depth of charge collection and hence amplitude in the case of a particle strike. Retrograde wells have a progressively higher doping towards the bottom of the well and hence provide similar benefits to the epitaxial substrate. Trench isolation (used to increase density) reduces the lateral gain of the parasitic bipolar device in the SCR.

Summary - Preshower Technology Choice

The radiation environment created within an LHC experiment is extreme and will cause many materials to undergo a change in their electrical or optical properties. Silicon is no exception and the performance of both the silicon sensors and the front-end electronics will be degraded over time due to radiation damage. The extent of degradation can be reduced both through processing techniques and design. A knowledge of the radiation environment and radiation damage mechanisms in devices is therefore necessary in order to design a front-end electronics chip such as PACE.

This section has examined the radiation environment within CMS summarising the environments of the Pixel, Tracker, Preshower and ECAL in the tables 2.1 to 2.4 respectively. In the endcap region the charged particle flux and neutron fluence follow a positive gradient as η increases. The expected absorbed dose of ionising radiation over ten years is from 0.5 Mrad(Si) (at η =1.6) to 6 Mrad(Si) (at η =2.6). The expected neutron fluence is from 2×10^{13} n cm^{-2} to 1.8×10^{14} n cm^{-2}. The specification for radiation tolerance of the electronics has therefore been specified at 10 Mrad(Si) of ionising radiation and a neutron fluence of 2×10^{14} n cm^{-2}.

Radiation effects in bipolar and CMOS devices have been discussed as well as design techniques that can help radiation tolerance in various technologies.

The strategy adopted by the Preshower was to first develop an architecture in a standard CMOS technology, build prototypes with this "rad soft" option in order to prove the feasibility of the system. Only then would the architecture be ported to a "radiation tolerant" technology.

The chip developed for the rad soft version was called PACE1 and was designed in Mietec 0.7 μm CMOS. The development of Delta and PACE2 (subjects of chapters 4 and 5) was made in DMILL technology. DMILL was chosen because at that time it was the only existing technology with proven radiation tolerance adequate for application in the Preshower.

The excellent results of deep sub-micron technologies emerged later. Porting the PACE2 design to deep sub-micron to create PACE3 is a possibility for the future. Whether to proceed with this step will depend on PACE2 results after irradiation which at the time of writing do not exist.

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Chapter 3

PACE1

PACE1 was the first PACE prototype ASIC designed for the Preshower. It was designed as an analog memory based on current integration and fabricated in a standard (non radiation tolerant) bulk 0.7μm CMOS process. The design aimed to demonstrate the Preshower analog architecture and provide a chip that could be used to build an electro-mechanical prototype of a Preshower system which could subsequently be tested in a particle beam. Some of the specifications of table 1.6 were relaxed for PACE1 such as the upper limit for the dynamic range, which was 250 MIPs instead of the required 400. PACE1 did not attempt to address the issues of radiation hardness or interface protocols. These issues were to be addressed later in PACE2 (chapter 5).

In this chapter, the first section outlines the main concepts in the design of PACE1. The front-end amplifier designed for PACE1 was called FCICON and was first fabricated and measured on a test chip. The design and measured results of the front-end amplifier (FCICON) are discussed. The second section deals with the results from PACE1, which revealed an important flaw in the design of an analog memory based on current integration. The third section describes the Preshower electro-mechanical prototype and the results obtained during beam tests.

3.1 The PACE1 Design

3.1.1 The analog channel

The principle behind the analog architecture of PACE1 is shown in figure 3.1. Charge from the sensor is converted to a proportional current pulse. The current pulse is then integrated onto a capacitor by connecting a capacitor from the switched capacitor matrix in the feedback of a write amplifier. A read operation can then convert the charge stored on the capacitor into a voltage.

Digital control logic switches from one capacitor to the next at the LHC bunch crossing rate of 40 MHz. The duration of the current pulse from the pre-amplifier is

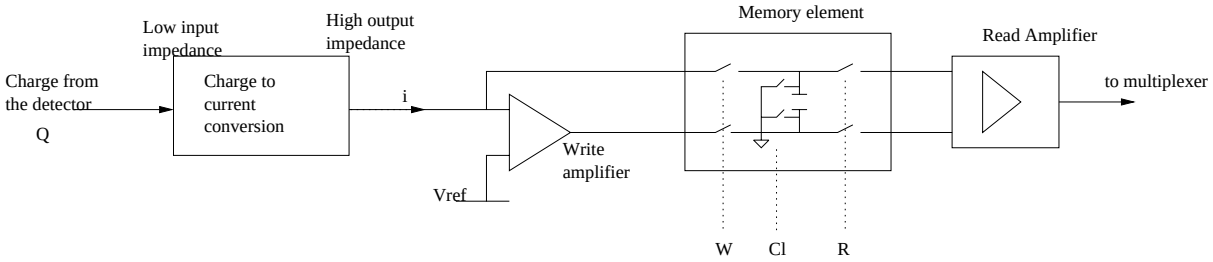


Figure 3.1: The analog channel for PACE1.

greater than 25 ns and hence is integrated onto more than one capacitor. Figure 3.2 shows a diagram of a current pulse being integrated onto 3 successive capacitors and the resulting voltage readings from those three capacitors.

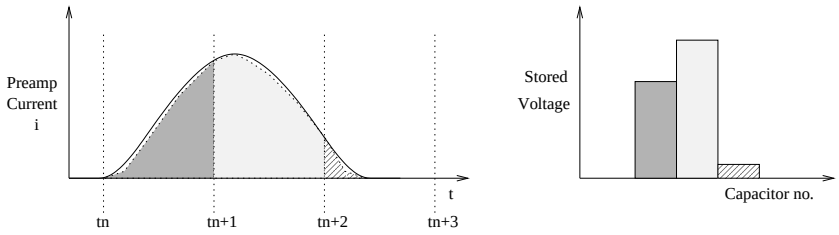


Figure 3.2: Charge to voltage conversion through current integration onto the analog memory capacitors

The sum of the voltage of the three capacitors will hence give the total charge delivered by the sensor. This scheme was considered extremely attractive for the Preshower since it meant simple charge reconstruction and a system that would be robust against phase variations, clock jitter and small variations in pulse shape with respect to other channels and over time.

Figure 3.3 shows a block diagram of the full PACE1 architecture. PACE1 has one channel for each strip of the Preshower sensor hence 32 active channels; in addition there are 4 dummy channels that will be mentioned later. Each channel consists of a pre-amplifier with a leakage current compensation circuit, write amplifier, a series of capacitors and a read amplifier as shown in figure 3.1. Following the read amplifiers is a 20 MHz analog multiplexer to serialise the analog output from each channel into a stream of analog values. An illustration of the streamed analog output is shown in figure 3.4.

The length of the capacitor matrix was consistent with table 1.6 at 160 but the maximum number of LV1s that could be simultaneously stored was 4 due to the capacity of the FIFO.

The biasing of the analog blocks was achieved through internal DACs that were programmable through a serial interface. Other programmable features included : internal latency, multiplexer frequency (20 MHz, 10 MHz, 5 MHz and 2.5 MHz) and independent channel selection for calibration.

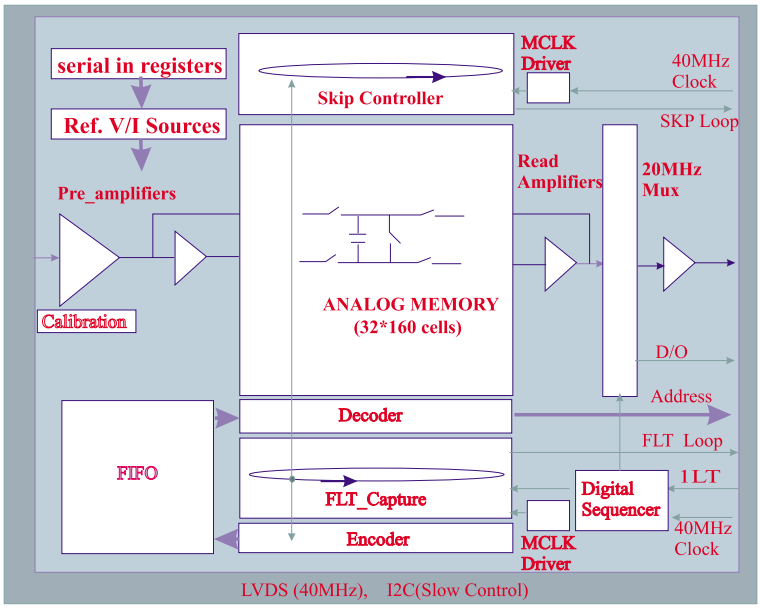


Figure 3.3: Block diagram of the PACE1 architecture

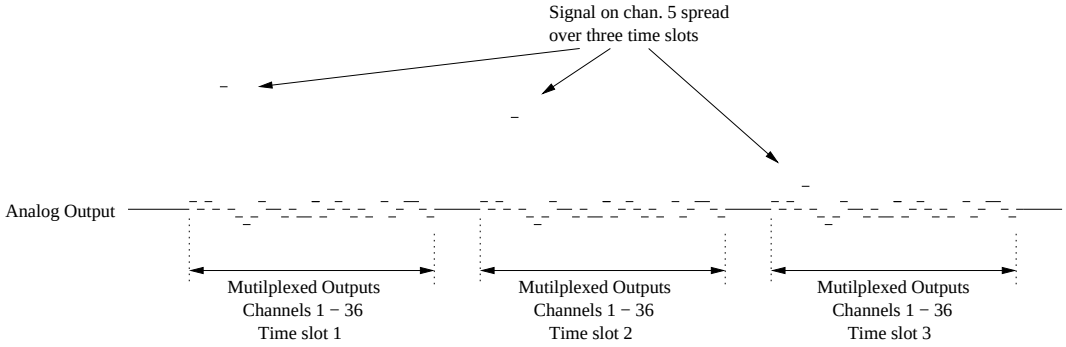


Figure 3.4: An illustration of how the multiplexed analog data appears at the PACE1 analog output for a single LV1 trigger. The data of all channels in three times slots are serialised. A signal can be seen on channel 5 and is spread over the three time slots.

3.1.2 The PACE1 pre-amplifier - FCICON

The pre-amplifier designed for PACE1 is known as FCICON and fulfilled the role of charge to current conversion shown in figure 3.1. The design goals of the circuit were to have very low input impedance, high output impedance and a linear response from 1 to 250 MIPs input signal (4 fC to 1 pC of charge).

The FCICON structure is based on a current conveyer principle [3] and the circuit diagram is shown in figure 3.5.

It is a symmetric structure with common gate input transistors M_{ni} and M_{pi} offering a very low input impedance at the input node (V1). The signal passes symmetrically through cascode transistors M_{nc} and M_{pc} before being transferred to two output

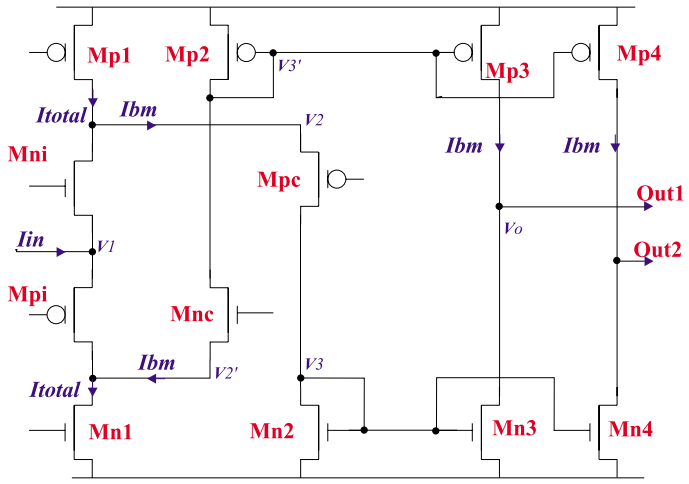


Figure 3.5: Circuit diagram of the FCICON pre-amplifier

branches through current mirrors M_{n2} and M_{p2}. The imbalance between the currents in the two branches is proportional to the signal and is mirrored to two output branches (Out1 and Out2). Transistors M_{p1} and M_{n1} are current sources controlling I_{total} and the cascode transistors are biased in such a way as to control I_{bm}. The two input transistors therefore receive a dc current of $I_{total} - I_{bm}$. Transistors M_{n3}, M_{n4}, M_{p3} and M_{p4} are the current sources for the output branches each having a dc current I_{bm}.

To have a fast signal response it is necessary to have a fast time constant ($\tau = R_i C_i$) at the input. The input resistance (R_i) is therefore designed to be as small as possible since the Preshower sensor capacitance (the dominant component of the input capacitance C_i) is large. Applying the input signal to the source of the input transistors makes R_i an inverse function of the transconductance (g_m) of the two input transistors in parallel as in equation 3.1. The output resistance is an inverse function of the drain conductances (g_{ds}) of M_{n3} and M_{p3} as in equation 3.2.

$$R_i = \frac{1}{g_{m_{ni}} + g_{m_{pi}}} \tag{3.1}$$

$$R_o = \frac{1}{g_{ds_{n3}} + g_{ds_{p3}}} \tag{3.2}$$

In the saturation region, the transconductance of a CMOS device is given by equation 3.3 and the drain conductance by equation 3.4.

$$g_m = \frac{\Delta I_d}{\Delta V_{gs}} \approx \sqrt{2\mu C_{ox} \frac{W}{L} |I_d|} \tag{3.3}$$

$$g_{ds} = \frac{\Delta I_d}{\Delta V_{gs}} = \frac{I_d \lambda}{1 + \lambda V_{ds}} \approx I_d \lambda \tag{3.4}$$

where :

- I_d is the device drain current,
- V_{gs} is the voltage between the gate and source of the device,
- μ is the mobility of the carriers in the channel,
- C_{ox} is the capacitance of the gate oxide,
- $\frac{W}{L}$ is the ratio of gate width over length,
- V_t is the threshold voltage,
- V_{ds} is the voltage between drain and source of the device.
- λ is the channel length modulation parameter. It is given by the gradient of I_d against V_{ds} for a given V_{gs} in the saturation region. Ideally it should be zero but in reality there is a gradient which increases with very short gate lengths. $\lambda \propto \frac{1}{L}$.

Equation 3.3 shows that the MOS designer has two handles to control g_m namely $\frac{W}{L}$ and I_d. The input transistors have therefore been designed with large W, small L and reasonably high I_d in order to have a large g_m. The resulting input impedance calculates to $R_i = 49\ \Omega$. The most important factor to obtain high output impedance (very low g_{ds}) is to ensure a low λ by keeping the gate lengths much higher than the minimum allowed by the technology. The output impedance obtained was $R_o = 54$ MΩ.

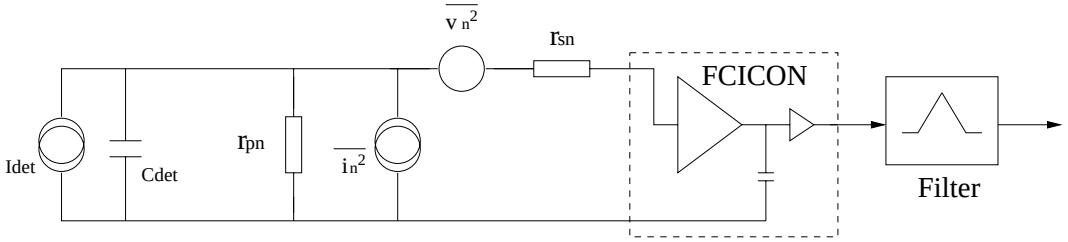


Figure 3.6: Noise model for the FCICON

Figure 3.6 shows the noise model for the FCICON circuit. The calculation of noise follows the techniques described in the appendix A. Referring all noise sources in FCICON to the input gives series and parallel equivalent noise resistances (R_{sn} and R_{pn}) as in equations 3.5 and 3.6 respectively.

$$R_{sn} = \frac{2\Gamma}{3(g_{m_{ni}} + g_{m_{pi}})} \tag{3.5}$$

$$R_{pn} = \frac{2\Gamma}{3(\sum_{x=1}^{x=4} g_{m_{n(x)}} + \sum_{x=1}^{x=4} g_{m_{p(x)}})} \tag{3.6}$$

where :

- Γ is the excess noise factor.

There is no amplification across the input transistors which means that the full thermal noise of all the current sources in the circuit combine at the input to form R_{pn}.

The equivalent series and parallel noise spectral densities equate to equations 3.7 and 3.8.

$$\frac{\overline{v_n^2}}{\Delta f} = 4kTR_{sn} = \frac{8kT\Gamma}{3(g_{m_{ni}} + g_{m_{pi}})} \tag{3.7}$$

$$\frac{\overline{i_n^2}}{\Delta f} = \frac{4kT}{R_{pn}} = \frac{6kT}{\Gamma}(\sum_{x=1}^{x=4} g_{m_{n(x)}} + \sum_{x=1}^{x=4} g_{m_{p(x)}}) \tag{3.8}$$

where :

- k is Boltzmann's constant,
- T is temperature.

A triangular weighting (as explained in the appendix A) can then be used to find the ENC.

$$\overline{ENC_s^2} = \frac{(\overline{v_n^2}/\Delta f)C_i^2}{t_m} \tag{3.9}$$

$$\overline{ENC_p^2} = \frac{(\overline{i_n^2}/\Delta f)t_m}{3} \tag{3.10}$$

where :

- t_m is the peaking time given by the filter,

- C_i is the total input capacitance.

It can be seen from these equations that the series noise component ($\overline{ENC_s^2}$) is inversely proportional to the sum of the input transistors transconductance. The parallel noise ($\overline{ENC_p^2}$) is proportional to the sum of the transconductances of the transistors used for the current sources and current mirrors. The design aimed to maximise the transconductance of M_{ni} and M_{pi} and minimise the transconductance of M_{p1} to M_{p4} and M_{n1} to M_{n4}.

The W/L values chosen for the design are given in table 3.1.

Transistor	Mni	Mpi	Mn1	Mp1	Mnc	Mpc	Mn2,3 &4	Mp2,3 &4
W/L ($\frac{\mu m}{\mu m}$)	$\frac{980}{0.7}$	$\frac{2940}{0.7}$	$\frac{60}{5}$	$\frac{180}{5}$	$\frac{98}{0.7}$	$\frac{294}{0.7}$	$\frac{20}{5}$	$\frac{60}{5}$

Table 3.1: W/L values used in the FCICON design.

To evaluate the FCICON design a multi-channel test chip called LDR$_{amp}$ was fabricated and measured. To facilitate the measurements the current output from FCICON was turned into a voltage by a resistive termination to ground. Simulations showed that a termination resistance of 10 kΩ produced a voltage pulse with the same shape as the current pulse produced by FCICON. A source follower was then used to buffer out the signal.

Figure 3.7 shows a schematic diagram of an LDR$_{amp}$ channel and figure 3.8 shows the resulting measured pulse shape. One can see that the peak of the pulse arrives at ∼20 ns but the tail continues until almost 80 ns. A single current pulse will therefore be integrated onto 3 successive memory cells at 40MHz.

The gain with a 10 kΩ termination resistor is 1.8 mV/MIP and the signal response is linear for ±800 fC (±200 MIPs) of input charge as shown in figure 3.9. The integral non-linearity (INL) = 0.05mV (2.8%) as expressed in terms of standard deviation from the mean gain.

The measured noise of FCICON is shown in figure 3.10 as a function of added input capacitance. A linear fit to the measured data gives an ENC = 1800 e + 41 e/pF. For an input capacitance of 40 pF the ENC ≈ 3440 e.

The gain and dynamic range will be altered when FCICON is connected to an analog memory due to a different load impedance.

3.1.3 The PACE1 analog memory

In PACE1 the current pulse produced from FCICON is integrated during periods of 25 ns onto successive capacitors within a switched capacitor matrix by switching the memory capacitors into the feedback of a write amplifier. It is important however to ensure that the capacitor is discharged completely before the signal current is integrated onto it. Two NMOS transistors are included in the memory cell in order to

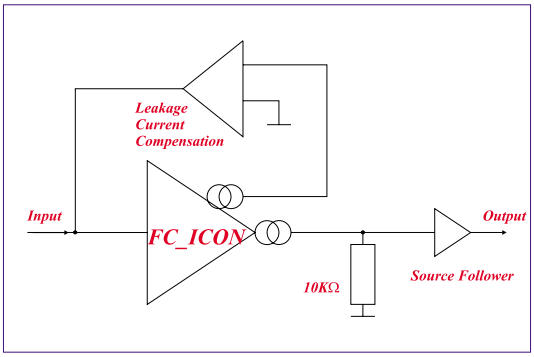


Figure 3.7: A schematic diagram of one channel of the LDR$_{amp}$ chip. The current output from FCICON is terminated with a resistance in order to view the pulse shape as a voltage.

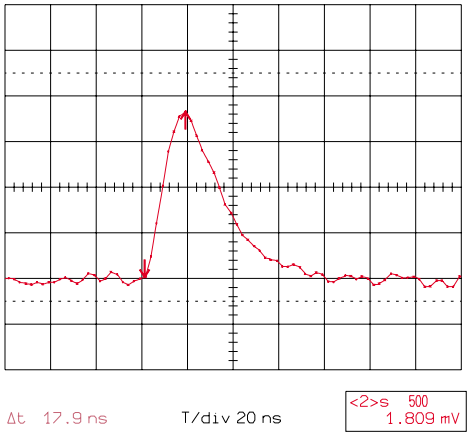


Figure 3.8: FCICON signal response to 1 MIP viewed as a voltage.

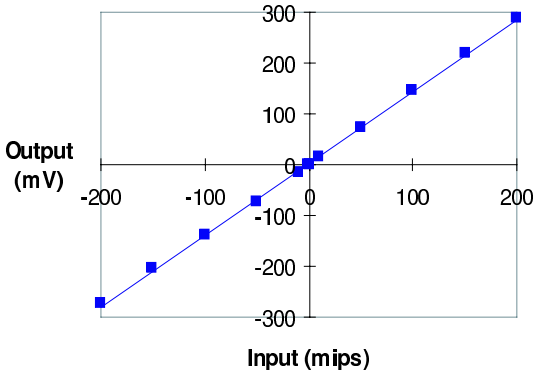


Figure 3.9: The linearity of FCICON for ±800 fC (400 MIPs) of input charge.

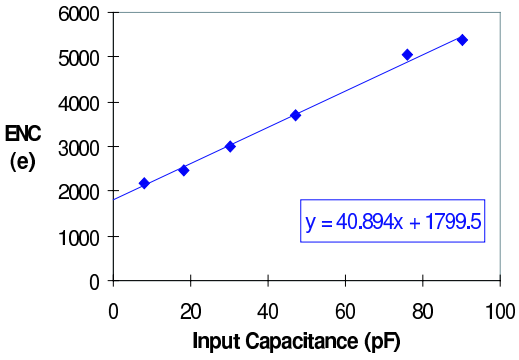


Figure 3.10: The measured noise performance of FCICON as a function of added input capacitance.

discharge both terminals of the capacitor before a write operation is performed. Figure 3.11 shows a schematic diagram of the analog memory cell. It contains 6 NMOS transistors and 1 capacitor.

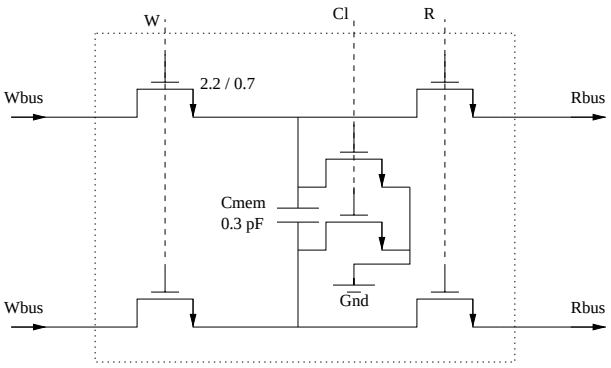
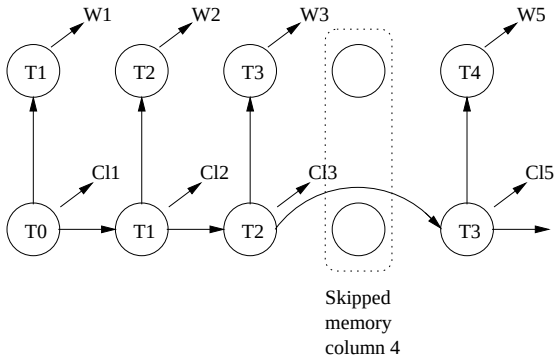
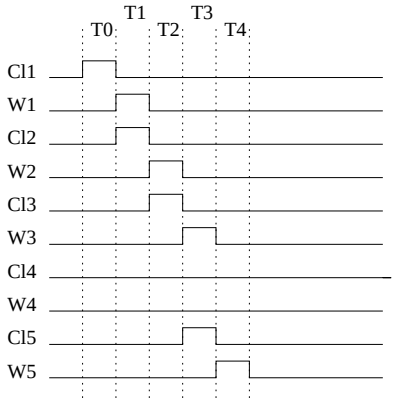


Figure 3.11: The analog memory cell for PACE1. It contained 6 NMOS transistors used as switches and a 0.3 pF capacitor.

The control logic within PACE1 is designed to provide "clear" (Cl), "write"(W) and "read"(R) pulses to each column of memory cells. It was designed as a shift register with 2 d flip-flops per column with a horizontal and vertical shift mechanism as shown in figure 3.12. Using this shift mechanism the control logic can provide a Cl pulse one clock period before a W pulse to a particular column. This means that in any one time period (T) column x will receive a W pulse and column x+1 will receive a Cl pulse providing column x+1 has not previously been triggered and set to skip mode. If column x+1 is in skip mode then the shifting mechanism will produce a Cl pulse in the next available memory column without losing synchronisation.



Horizontal & vertical shift register system



Timing diagram of the Clear (Cl) & write (W) signals generated for each column.

Figure 3.12: The principle of horizontal and vertical shift mechanisms to ensure a column receives a clear pulse (CL) one clock period before applying a write pulse (W).

The signal shaping of the pulse from FCICON is determined by the load impedance (R_l). When connected to an analog memory the load impedance is determined by the continuous switching of capacitors such that $R_l \approx \frac{1}{fC_{mem}}$ where f is the frequency of switching capacitors (40 MHz) and C_{mem} the value of capacitance inside a memory element (0.3 pF). The effective load resistance is therefore $R_l \approx 83$ kΩ.

The layout of PACE1 is shown in figure 3.13. It contains approximately 100 000 transistors. The channel inputs are on the left side connecting to 36 identical channels. Only 32 channels were connected to the silicon strips leaving 4 channels unconnected to sense dc offsets and common mode pick-up.

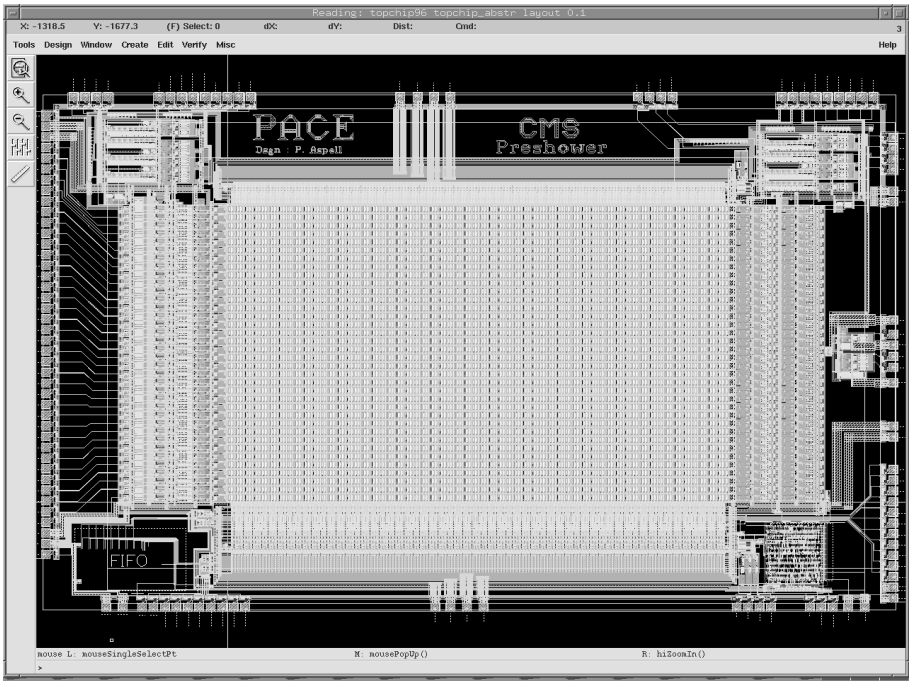


Figure 3.13: The full layout of the PACE1 chip.

The central section is a switched capacitor matrix of 36 × 160 memory cells with the read amplifiers connected on the right. The output buffer can be seen as a small block in the middle of the extreme right. In the top left and right corners are the DACs to control biasing conditions for the write and read amplifier sections. Directly above and below the central capacitor matrix is the control logic including the column decoder and encoder. The FIFO is located in the lower left corner and the sequencer in the lower right. The overall dimensions are 9.6 mm by 6.7 mm with a total area of 64.3 mm^2.

A detailed description of the design of the individual building blocks of PACE1 can be found in [2].

3.2 PACE1 Measured Results

The results from the functionality tests of PACE1 showed correct and expected behaviour for almost all the control circuits. These included the control logic, sequencer, serial link, FIFO, programmable multiplexer, programmable DACs, independent channel selection for calibration, programmable latency and programmable number of skipped cells per trigger. The column encoder however, had a speed problem when run at 40 MHz which resulted in an erroneous column address being written into the FIFO for the first column per LV1. The maximum frequency with the correct behaviour was observed to be 33 MHz. The source of the limitation in speed was traced to an undersized transistor within the encoder. It would be a straight forward design change to correct in a future design. For PACE1 however, the speed of operation was limited to 33 MHz.

Figure 3.14 shows the multiplexed analog output for 4 time slots. A charge equivalent to 100 MIPs was injected into one channel. The channel containing the signal is clearly evident in times slots 2, 3 and 4 as a negative value relative to the baseline. The total charge is hence the summation of these 3 values.

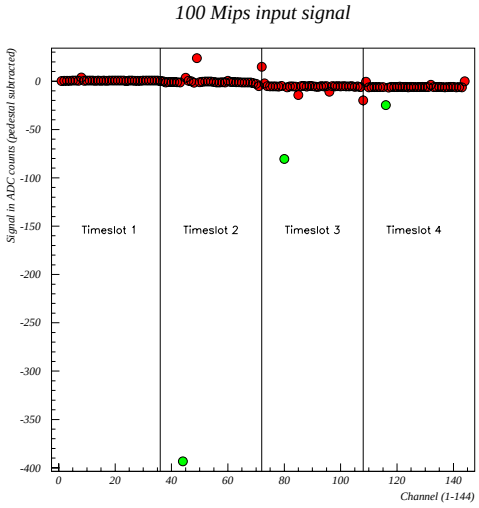


Figure 3.14: A 100 MIP signal is distributed into 3 time slots starting in the second. The signal is seen as negative because of an inverting amplifier used in the readout.

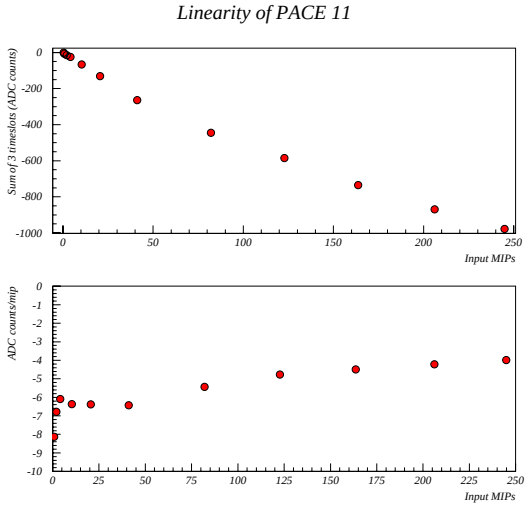


Figure 3.15: The dynamic range of the memory is 250 MIPs. The response has a small gain decrease from 6 mV/MIP to 4.5 mV/MIP over the full range.

The dynamic range of PACE1 (shown in figure 3.15) is from 1 to 250 MIPs. The response shows a small decrease in gain from 6 mV/MIP to 4.5 mV/MIP over the full range.

The pedestal variation (σ_{ped}), defined as the standard deviation of sampled values from capacitors in one channel over a period of time, within the analog memory is a very important parameter for the Preshower. This is because the gain in PACE has been kept low in order to obtain a large dynamic range. A low gain however, means that small distortions in the sampled analog values after the pre-amplifier will contribute strongly to the overall noise of the system.

Analysis of the data from PACE1 taken without an input signal but applying random triggers showed a very large pedestal variation (σ_{ped} =5.8 mV). It was noted that cyclic patterns emerged in the data. These cyclic patterns coincided with some digital operations in a state machine within the sequencer. It was therefore hypothesised that the disturbance of data in PACE1 came from charge coupling through the substrate from the digital part to the analog part.

In order for charge to couple into the analog signal path there would need to be a sensitive node with relatively large parasitic capacitance to the substrate and have a relatively high impedance. A strong candidate for this node was the output from FCICON. It is driving a current and is therefore high impedance, it also has a large parasitic capacitance to the substrate since it is a metal line running the full length of the capacitor matrix. Furthermore it was realised that the combination of this parasitic capacitance (C_p), the write amplifier and the capacitance of the analog memory cell (C_{mem}) form a circuit that amplifies substrate noise. Figure 3.16 shows the location C_p which has a value in the order of 2 pF. Noise in the substrate would hence be amplified by the ratio $\frac{C_p}{C_{mem}}$ which is ≈ 7 since $C_{mem} = 300$ fF. This discovery highlighted a fundamental flaw in the design of a current integration analog memory.

To test this idea connections were made to the metal lines entering the capacitor matrix and bonding pads deposited using a focused ion beam (FIB). The location of the FIB pads is shown in figures 3.16 and 3.17. A low impedance voltage was then applied and a measurement taken. The cyclic patterns of charge pick-up were not observed. Figure 3.18 shows the cell to cell pedestal variation before and after FIB intervention.

The conclusions from the laboratory tests were that PACE1 could be used in the development of an electro-mechanical prototype of the Preshower detector but that a fundamental flaw exists in the design of an analog memory based on current integration. A review of the analog memory sampling technique and the design of the front-end amplifiers would be needed to reduce sensitivity to charge pick-up.

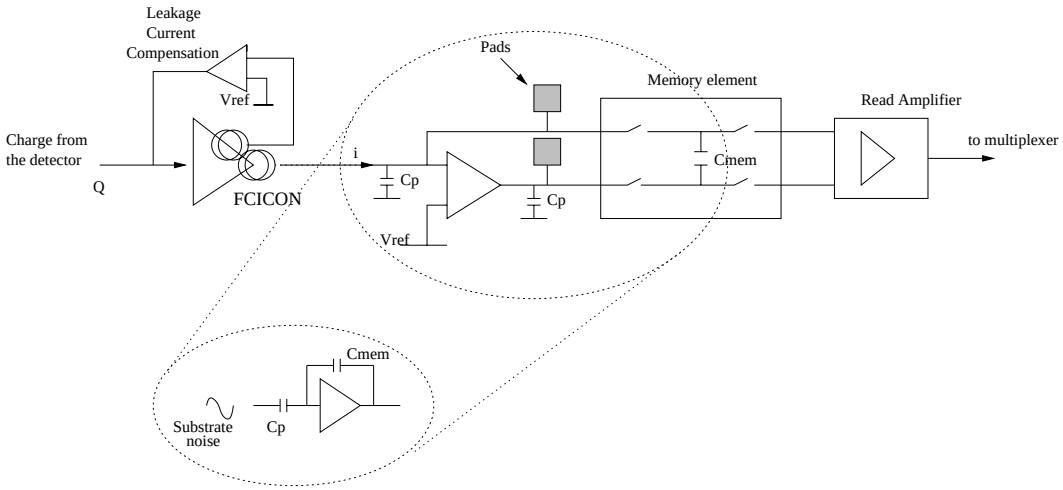


Figure 3.16: The parasitic capacitance (C_p) associated with the write bus combined with the write amplifier and memory capacitor (C_{mem}) creates a circuit which is sensitive to noise in the substrate. This was the expected path through which noise injected into the substrate from the digital section could couple through into the analog signal path and disturb the pedestal distribution. The idea was tested by gaining access to the write bus through deposition of pads using a focused ion beam (FIB).

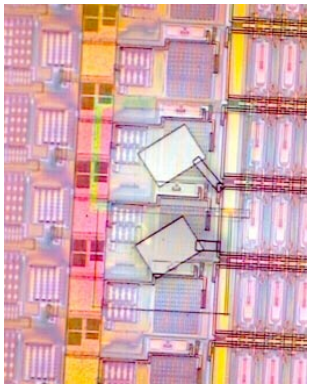


Figure 3.17: A photograph of the pads deposited as illustrated in figure 3.16.

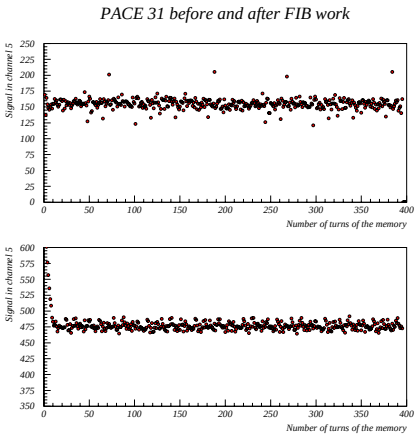


Figure 3.18: The cell to cell pedestal variation in PACE1 before and after FIB intervention. Charge pick-up observed before FIB intervention (top plot) was absent in the measurement after (lower plot).

3.3 The Preshower Electro-mechanical Prototype and Beam Test Results

As a demonstrator of a Preshower system, an electro-mechanical Preshower prototype was developed. The aim of the prototype was first to develop a system including absorbers, sensors, electronics and cooling so that any potential mechanical or electrical problems could be identified. The second aim was to place the Preshower prototype in an electron beam together with an ECAL prototype. Measured data could then be used to verify GEANT 3 simulations that have been used to design the structure of the Preshower.

3.3.1 The Preshower prototype

The Preshower prototype consisted of 2 planes of absorber constructed from a steel-lead-steel sandwich each equipped with a 2×2 array of silicon sensors. The total radiation length (as seen by a normally incident particle) was 3.24 X_0 (2.06 X_0 + 1.18 X_0) which is slightly more than the specification of 2 X_0 + 1 X_0. The silicon sensors were full size measuring 60×60 mm^2 and were divided into 32 silicon strips. The silicon sensors were mounted on a ceramic plate that also supported the electronic daughter board containing PACE1 plus a few surface mounted passive components. The ceramic plate was then mounted on a wedge-shaped aluminium tile to form a micro-module. Figure 3.19 shows a micro-module, PACE1 is located under a plastic cover in the centre of the electronics board. Control and readout signals were delivered by a flat cable (not shown) to a connector on the right.

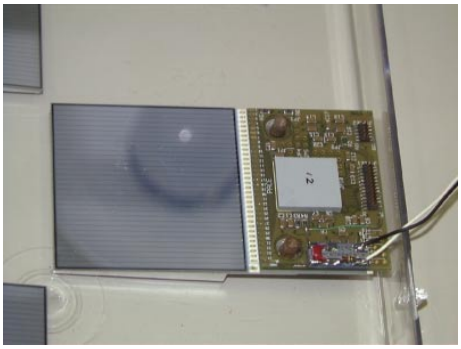


Figure 3.19: A photograph of a single micro-module.

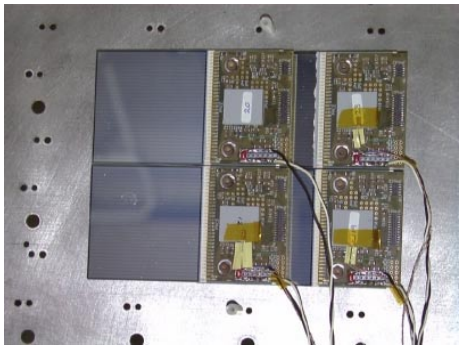


Figure 3.20: Photograph of a 2×2 array of micro-modules assembled for one plane of the Preshower prototype.

The micro-modules were assembled in a 2×2 array as shown in figure 3.20 and mounted on a steel plate. The wedge-shape tile allows the overlapping of sensors in the direction of the strips. There is a gap ($\sim$ 2 mm) between adjacent sensors parallel to the strip direction.

A motherboard containing control logic and an ADC for each PACE1 chip was mounted on top of each plane. The two planes were then slotted vertically into the Preshower prototype already containing absorbers and cooling.

The cooling was provided by water flowing through an aluminium plate machined with a serpentine path. A cooling plate was attached to each absorber which in turn was attached to the steel plate supporting the micro-modules. Care has been taken to ensure good thermal conduction from PACE1 through to the cooling plane in the same manner as foreseen for the final Preshower design.

The orientation of the micro-modules was rotated by 90^o from one plane to the other. The first plane (most upstream in the beam) has its strips mounted in the vertical direction and is known as the "V plane". The second plane has been mounted in the horizontal direction ("H plane").

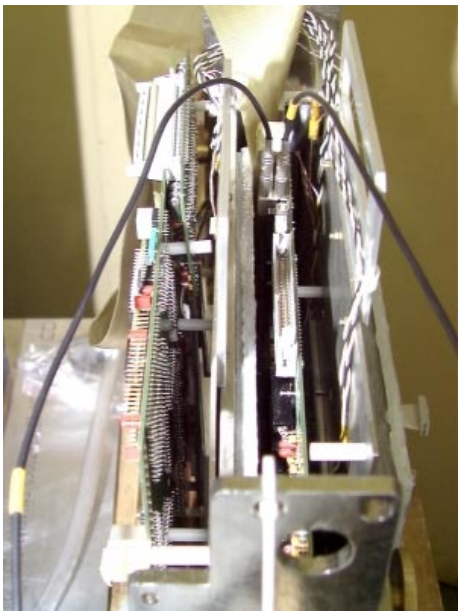


Figure 3.21: Top view of the Preshower prototype.

Figure 3.21 shows a photograph of the 2 planes inserted into the prototype. An electrical environmental shield made from a copper coated pcb plate was then used to encase the system. In order to prevent humidity and to aid cooling of the mother board dry nitrogen was flushed through the prototype.

Figure 3.22 shows the completed Preshower prototype situated in front of the ECAL endcap prototype containing a 5×5 crystal array plus readout electronics.

Figure 3.22: Photograph showing the Preshower prototype placed in front of the ECAL endcap box.

3.3.2 Beam test results

Figure 1.9 shows an illustration of the endcap Preshower together with ECAL crystals as foreseen in CMS. The crystal orientation is not perpendicular to the Preshower but varies for different values of η such that the crystals always point in the general direction of the beam. As a result the gap between the crystals and the Preshower increases as η decreases. Also the thickness of absorber in the Preshower seen by particles from the interaction will increase as η decreases. Both of these effects will result in a decreased energy resolution for low η.

In order to replicate the different regions with respect to η the Preshower prototype had a pivot fitted in one corner around which it could rotate through varying angles with respect to the beam. The crystals however remain oriented in the direction of the beam. Figure 3.23 shows a schematic top view of the system indicating the point of rotation.

The complete system was then positioned in the H4 test beam at CERN. An on-line LabView monitoring system was developed in which the analog output of an individual PACE1 chip could be viewed. The column address could also be monitored. This was useful during the set-up period when the PACE1 latency had to be matched with the trigger delay in the test beam. Figure 3.24 shows a screen dump of the on-line display when the prototype was hit by a 120 GeV electron beam. The signal is evident in time slots 2 and 3 (spread over several strips), there are 4 time slots shown. This is similar to figure 3.14. The column numbers for the 4 time slots are also displayed.

The number of MIPs deposited in each plane (E_1 and E_2) for an 80 GeV electron beam is shown in figure 3.25. The measured values are compared with the simulated values showing excellent agreement. Each is the sum over 3 time slots in 5 strips centred on the most energetic strip of the plane.

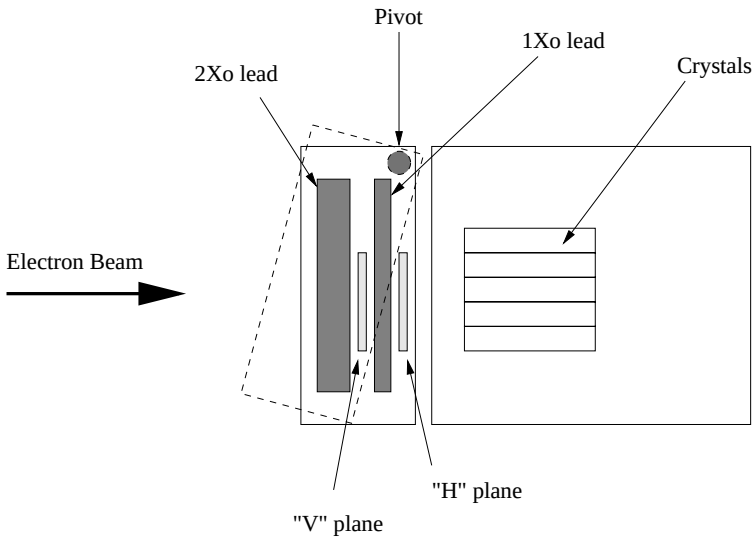


Figure 3.23: Top view schematic showing how the Preshower prototype could be placed at different angles with respect to the beam and the crystals. This is to replicate Preshower regions at different η.

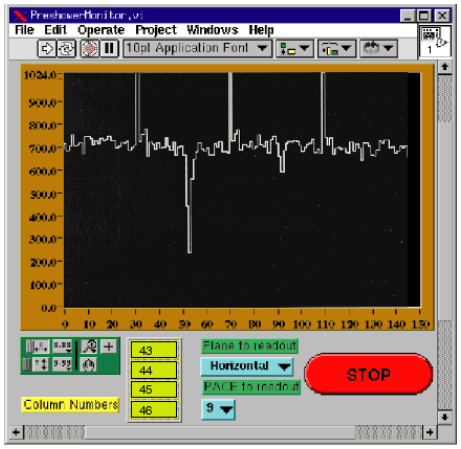


Figure 3.24: Screen dump of the on-line monitoring display when the Preshower prototype was hit by 120 GeV electrons. The analog output of 4 time slots from a single PACE1 is shown. The signal is evident in time slots 2 and 3.

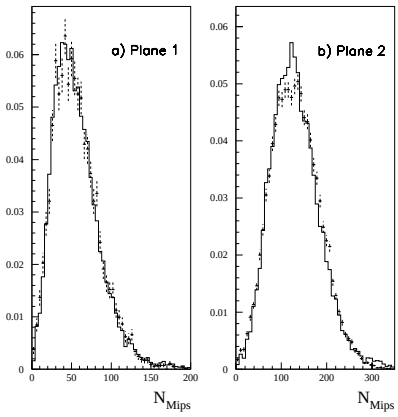


Figure 3.25: Comparison between the simulation and measured result for the number of MIPs deposited in each plane for an 80 GeV electron beam. The simulation is the solid histogram whilst the measured values are plotted by dashed lines with error bars.

The sum of the energy measured in nine crystals (E_9) was used to measure the energy resolution. Equation 3.11 is the measured energy resolution of the crystals alone (excluding the noise contribution). The result from simulation is given in equation 3.12. The difference in the stochastic term is due to photostatics that are not included in the simulation. To enable direct comparisons between the data and the simulations a value is thus added by hand to the simulated stochastic term equivalent to $(4.1^2 - 1.4^2)^{1/2} = 3.85\%$.

$$\frac{\sigma_E}{E} = \frac{4.1\%}{\sqrt{E}} \oplus 0.25\% \tag{3.11}$$

$$\frac{\sigma_E}{E} = \frac{1.4\%}{\sqrt{E}} \oplus 0.25\% \tag{3.12}$$

The total energy deposited in the system is the sum of the energy deposited in Preshower (E_{presh}) plus E_9 as given in equation 3.13.

$$E_{tot} = E_{presh} + E_9 \tag{3.13}$$

$$E_{presh} = \gamma(E_1 + \alpha E_2) \tag{3.14}$$

E_{presh} is given by the energy measured in each plane (E_1 and E_2) and the two coefficients α and γ as in equation 3.14. α defines the relative weight between the two planes and is adjusted to get the best energy resolution and γ is obtained from a plot of E_9 as a function of $E_1 + \alpha E_2$ as shown in figure 3.26. γ is the calibration factor needed to obtain a constant horizontal line for total energy deposited in the system.

The distribution of E_9 for a beam energy of 180 GeV shows a σ of 1.15%. This improves to $\sigma = 0.62\%$ when the Preshower energy is added according to equation 3.13. The comparison of the measured distributions is shown in figure 3.27.

The energy resolution for angles of incidence of 0^o and 20^o are shown in figures 3.28 and 3.29 alongside the respective simulation results.

These measurements, and further measurements including energy deposited in the Preshower as a function of angle and spatial precision as a function of angle are reported in [5]. All results compare very well with predictions from simulation. This gives confidence both in the hardware developed so far in the experiment and on the validity of the simulations used to define the Preshower specifications.

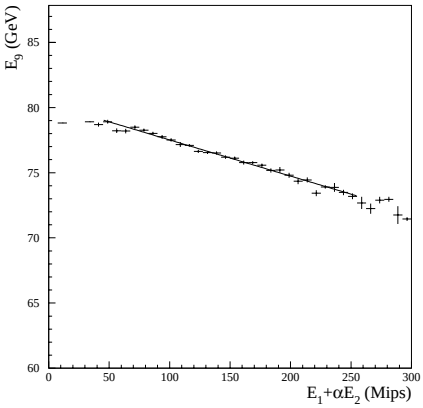


Figure 3.26: Total energy deposited in the 9 ECAL crystals (E_9) verses the total energy deposited in the two Preshower planes ($E_1 + \alpha E_2$).

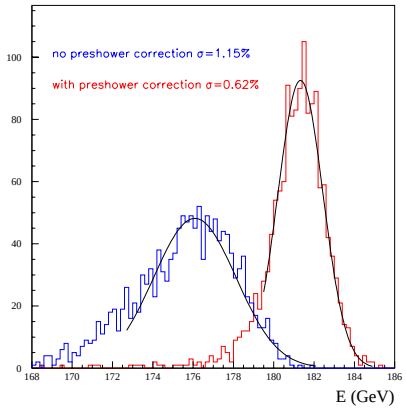


Figure 3.27: Distribution of the energy measured in the crystals alone (E_9) compared to the total energy measurement (E_{tot}) with the Preshower contribution added.

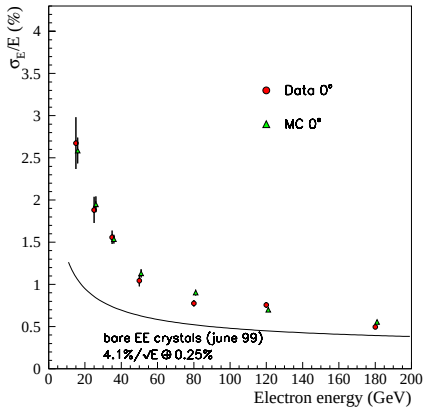


Figure 3.28: Energy resolution after noise subtraction for an incidence of 0^o.

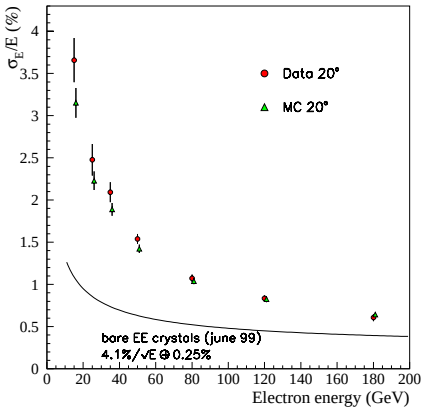


Figure 3.29: Energy resolution after noise subtraction for an incidence of 20^o.

Summary

PACE1 represented the first PACE prototype developed for the CMS Preshower. The architecture was that of a large dynamic range analog memory based on current integration. The dynamic range was measured from 1 to 250 MIPs. The pre-amplifier stage was based on the FCICON current conveyer design which converted charge to current. FCICON was first designed and fabricated on a test chip. The measured noise performance was ENC = 1800 e + 41 e/pF. The noise of PACE1 however was completely dominated by large pedestal disturbances of the analog memory that appeared to be correlated with digital functions within the logic. Further investigation showed a parasitic path that could amplify substrate noise onto the storage capacitor within the analog memory cell. This parasitic path is inherent within an analog memory design based on current integration.

The conclusions from the measurements were that PACE1 could be used in the development of an electro-mechanical prototype of the Preshower detector but that a review of sampling technique and front-end architecture would be needed before the development of the next PACE design.

As a demonstrator of a Preshower system, an electro-mechanical Preshower prototype was developed involving absorbers, sensors, electronics and cooling. The Preshower prototype consisted of 2 planes of absorber constructed from a steel-lead-steel sandwich each equipped with a 2×2 array of micro-modules, each micro-module consisting of a silicon sensor plus a PACE1 chip. It was placed in front of an ECAL prototype and the two units placed in an electron beam. The Preshower prototype had a pivot located in one corner which allowed it to have a variable angle with respect to the beam and the ECAL crystal orientation. By doing so, the different regions of the Preshower with respect to η could be replicated.

The measured energy deposition in the two Preshower planes (E_1 and E_2) for a given electron beam energy was consistent with expectations from simulation. The energy measured in the Preshower was then added to the energy measured in a group of 9 crystals in the ECAL prototype. The result was a reduction in the distribution of energy measured from $\sigma = 1.15\%$ for the ECAL crystals alone to $\sigma = 0.62\%$ when the contribution from the Preshower had been added for a beam energy of 180 GeV.

These measurements, and further measurements including energy deposited in the Preshower as a function of angle and spatial precision as a function of angle are reported in [5]. All results compare very well with predictions from simulation. This gives confidence both in the hardware developed so far in the experiment and on the validity of the simulations used to define the Preshower specifications.

References

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[4] F.Anghinolfi, P.Aspell, R.Bonino, D.Campbell, M.Campbell, A.G.Clark, E.Heijne, P.Jarron, JC.Santiard, H.Verweij *DYN1: A 66MHz front end analog memory chip with first level trigger capture for use in future high luminosity particle physics experiments.* (Nucl. Inst. & Methods in Physics Research A 344 (1994) 173-179, North Holland)

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Chapter 4

Voltage Sampling - The Development of DELTA and DeltaStream

This chapter documents a radical change in signal processing within PACE from current integration (as in PACE1) to voltage sampling. The motivation was to lower the line impedance into the switched capacitor matrix and therefore reduce its sensitivity to charge pick-up from the substrate. The chapter is in 4 sections. The first examines charge reconstruction using voltage sampling, the second explores different circuit architectures, the third details the chosen circuit design (DELTA) and the fourth describes a multiple channel chip based on the DELTA design.

4.1 Charge Reconstruction

Current integration was initially chosen for the Preshower due to simple charge reconstruction (the sum of the charge integrated over 3 times slots) and its insensitivity to sampling phase and clock jitter (see chapter 3).

This section looks at charge reconstruction using voltage sampling to determine if the benefits of current integration would be lost.

A common approach for charge to voltage conversion in H.E.P. is that of a charge amplifier followed by a signal shaping stage (filter). Figure 4.1 shows a block diagram of an ideal circuit.

The charge delivered by the sensor (Q) is stored across the feedback capacitor (C_f) of a charge amplifier. A shaping stage then follows in order to limit the noise to the desired frequency range and provide the signal voltage at the output with a return to zero. A $CR - RC^n$ filter, commonly used in H.E.P., is assumed.

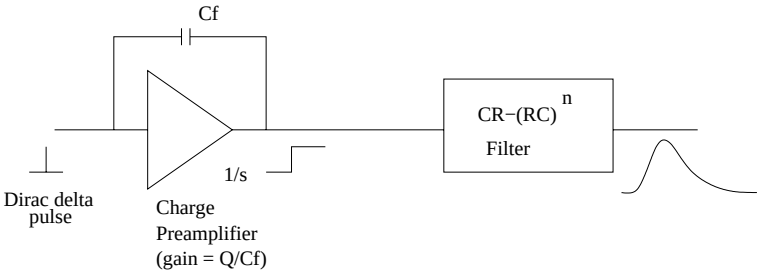

Figure 4.1: Charge amplifier followed by a $CR - RC^n$ filter

The $CR - RC^n$ filter has a transfer function ($H_{(s)}$) as expressed in equation 4.1 [1], [2]. The charge delivered by the sensor, in its ideal form, can be approximated to a Dirac delta function producing a step response ($1/s$) at the pre-amplifier output with gain Q/C_f. The resulting output voltage is given by $V_{o(s)}$ of equation 4.2 in the frequency domain and (after inverse Laplace transformation) by $V_{o(t)}$ of equation 4.3 in the time domain.

$$H_{(s)} = \left[\frac{s/\omega_c}{1 + s/\omega_c}\right]\left[\frac{A}{1 + s/\omega_c}\right]^n \tag{4.1}$$

$$V_{o(s)} = \frac{Q}{s\,C_f}\left[\frac{s/\omega_c}{1 + s/\omega_c}\right]\left[\frac{A}{1 + s/\omega_c}\right]^n \tag{4.2}$$

$$V_{o(t)} = \frac{Q\,(\,A\,\omega_c\,t\,)^n}{C_f\,n!\,e^{(\,\omega_c\,t\,)}} \tag{4.3}$$

where :

- Q is the charge delivered at the input.
- C_f is the capacitance in the feedback of the pre-amplifier.
- A is the gain of the filter.
- n is the order of the filter.
- ω_c is the central frequency of the filter and is related to the peaking time (τ_p) by equation 4.4. τ_0 is the time constant of the filter.

$$\omega_c = \frac{1}{\tau_0} = \frac{n}{\tau_p} \tag{4.4}$$

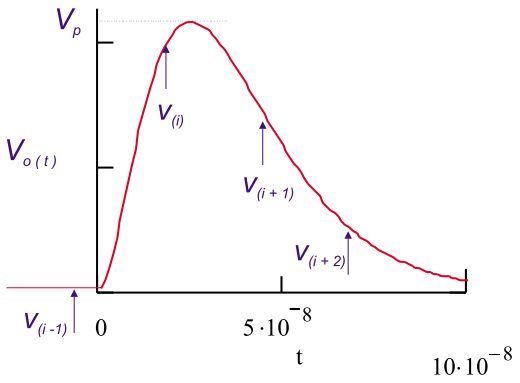

Figure 4.2: $V_{o(t)}$ plotted with examples of sampled voltages (v_i spaced by 25 ns).

The function $V_{o(t)}$ gives the output voltage of the filter as shown in figure 4.2 for second order filter ($CR - RC^2$) of peaking time ($\tau_p = 25$ ns).

Also added to the plot of figure 4.2 are sample points v_i spaced by 25 ns intervals but without a specific phase relation.

The Preshower needs to be able to determine the bunch crossing event in time, and peak voltage (V_p) (since $Q \propto V_p$) from these sampled voltages.

A deconvolution technique (described in [3]) uses 3 samples to resolve timing resolution and charge. The technique uses 3 voltage samples (v_1, v_2, v_3) taken at known points in time on a well defined function. A set of linear equations (4.5, 4.6 and 4.7) can be used to determine a set of 3 weights (Y_1, Y_2, Y_3).

$$\alpha = Y_1\, v_0 \tag{4.5}$$
$$\beta = Y_1\, v_1 + Y_2\, v_0 \tag{4.6}$$
$$\gamma = Y_1\, v_2 + Y_2\, v_1 + Y_3\, v_0 \tag{4.7}$$

The weights can be found such that samples v_i, v_{i+1} and v_{i+2} (as shown in figure 4.2) give $\alpha = Q$, $\beta = 0$, and $\gamma = 0$.

If the signal is in the following bunch crossing ie. the 3 sampled voltages are represented by v_{i-1}, v_i and v_{i+1} then α, β and γ result in (0, Q, 0).

Likewise, if the three voltages sampled have the form v_{i-2}, v_{i-1} and v_i then α, β and γ result in (0, 0, Q).

The deconvolution principle is very nice from a mathematical point of view. The problem is that relies on very precise timing and knowledge of the pulse shape in order to determine Q.

The real world will consist of noise, slight variations of pulse shape due to radiation damage of sensors and electronics, jitter on the clock signal and a small uncertainty on absolute phase of sampling.

Internal studies within the Preshower group have shown that the deconvolution method is able to determine the timing resolution despite distortions in the pulse shape. However, a slowing down of the pulse shape by 11% results in a 12% error in the value of Q.

Hence, on its own, deconvolution would not satisfy the specifications of the Preshower for charge reconstruction.

The approach proposed by the Preshower group [4] is to use deconvolution to resolve the bunch crossing number only. In addition, another set of weights W_1, and W_2 can be found to satisfy equation 4.8 and resolve Q.

$$Q = W_1\, v_1 \,+\, W_2\, v_2 \tag{4.8}$$

This assumes 3 samples in the relative timing positions v_{i-1}, v_i and v_{i+1}. v_{i-1} is not used in determining the weights. Its value can be used to subtract a common mode offset. v_1 is hence represented by v_i and v_2 by v_{i+1}.

The weights can be found using a χ^2 fit minimisation such that Q represents the deposited charge.

In the study [4] the electronics noise was exaggerated to 1/4 MIP, weights W_1, and W_2 were optimised for phase variations within ± 2 ns. The accuracy of Q was then determined with a phase variation of ± 2 ns and with a jitter on an individual sample of ± 0.5 ns. In all cases Q is resolved to within 1% of the charge deposited. This compares to 10% if the deconvolution method is used in isolation to resolve Q.

To conclude this section, voltage sampling is an option for the Preshower front-end electronics. Both the bunch crossing and charge information can be resolved from 3 voltage samples.

4.2 Voltage Sampling Channel Options

The basic specifications for the front-end electronics in a voltage sampling system are unchanged from 1.6. The dynamic range requirements are up to 400 MIPs during data taking and up to 50 MIPs during calibration. This allows the development of a two gain system.

A "high gain" mode can be used to boost the signal amplitude and hence raise the signal above the sampling noise of the analog memory. In this mode the noise of the front-end pre-amplifier will dominate and discrimination of a single MIP will be possible.

A "low gain" mode (having the same shaping time constants as the high gain) is used to obtain a 400 MIP dynamic range needed for π^0/γ separation during the normal data taking period.

Assuming a 2 gain system, a further set of electrical specifications can be written:

- Leakage current compensation: >40 μA (specified as twice that necessary).
- Calibration mode (High Gain) 0.1-50 MIPs over 1.5 V, gain = 30 mV/MIP.
- Run Mode (Low Gain) 0.6-400 MIPs over 1.6 V, gain = 4 mV/MIP.
- Technology: DMILL technology to achieve radiation tolerance, BiCMOS, 5 V power supply.

There are a number of ways of designing the front-end electronics to achieve these specifications. Three different channel architectures were studied, all of which satisfy the specifications listed above. These consisted of a "dual gain system" and two types of switched gain systems. The block diagrams for these different channel architectures are shown in figure 4.3.

Designs were made of each channel type and a test chip submitted in DMILL technology. The results showed that the main design criteria were met in all three cases. Below is a brief description of each channel option along with their respective advantages and disadvantages. Section 4.3 explains in detail the design and results of the chosen channel architecture.

4.2.1 Dual gain

The dual gain structure, illustrated as channel (a) in figure 4.3, includes two shapers with different gains. Both shapers are continuously sensitive to the output of a single charge pre-amplifier.

Advantages The main advantage with a dual gain system is that discrimination on a single MIP would be possible during normal operation as well as during calibration.

Disadvantages Unfortunately there are a number of disadvantages with a dual gain system.

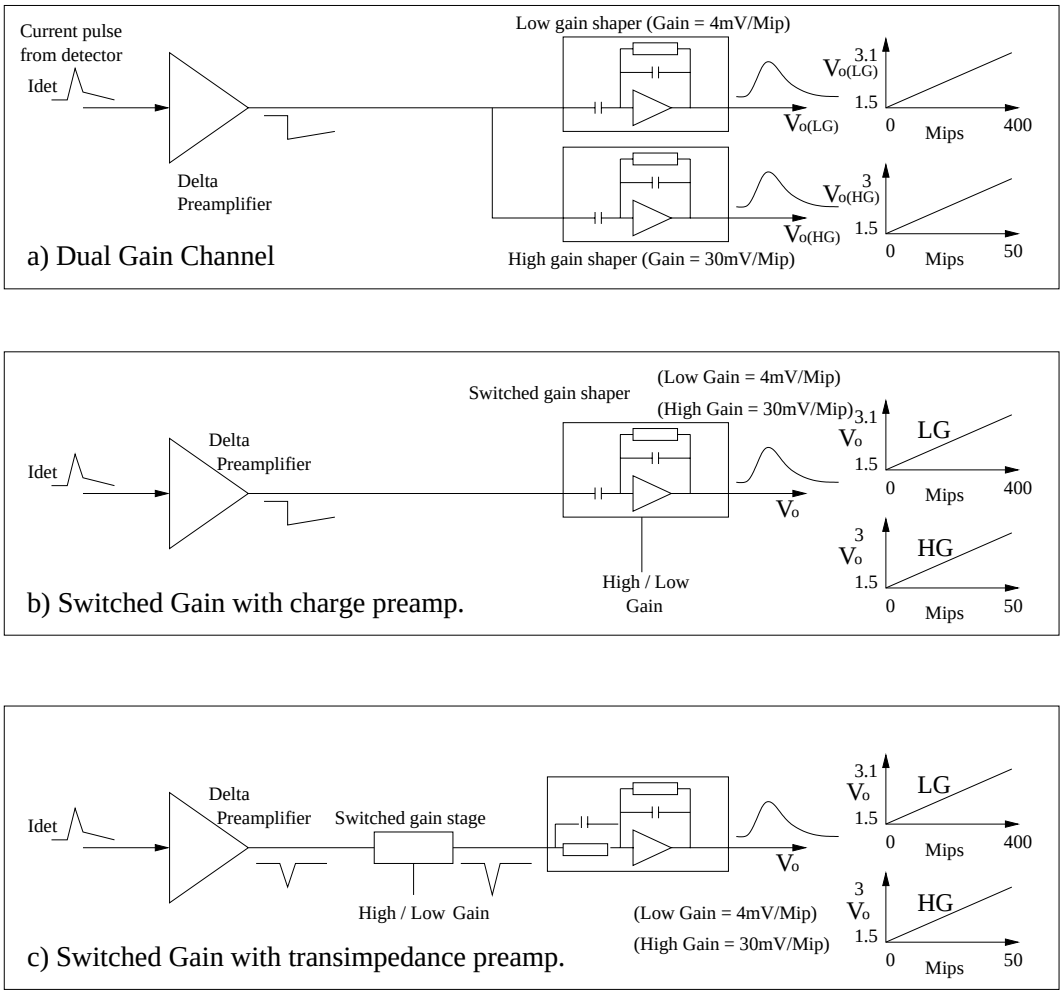

Figure 4.3: Block diagrams of the 3 channel configurations considered.

1 A dual gain system would require two rows of memory capacitors in the capacitor matrix (one for each gain, $V_{o(LG)}$ and $V_{o(HG)}$). This would result in a substantial increase in the area of the chip, which would impact badly on yield.

2 The maximum readout time per trigger is not sufficient to be able to multiplex both $V_{o(LG)}$ and $V_{o(HG)}$ for all channels of an analog memory. A comparator would hence be needed to select the appropriate output on a sample by sample basis. As well as complicating the read procedure, charge reconstruction would be very difficult since the 3 voltage samples (v_{i-1}, v_i and v_{i+1} from figure 4.2) would come from different shapers for large signals.

3 The power consumption would be increased significantly since there are two shapers per channel, also two read amplifiers per channel and a comparator.

4 The measured results from the test chip showed coupling from the high gain shaper into the low gain shaper for large signals. Saturation of the high gain shaper occurs for input signals >50 MIPs, subsequent recovery from saturation distorts $V_{o(LG)}$ appearing as a bump in the tail of the waveform.

4.2.2 Switched gain with a charge pre-amplifier

The switched gain structure, illustrated as channel (b) in figure 4.3, comprises a charge pre-amplifier and a single shaper with 2 selectable gains.

A charge pre-amplifier produces a fast initial edge followed by a slow return to its operating point and is sensitive over the whole 400 MIP range. The 2 shapers of the dual gain system are merged together in a switched gain system such that common components are used in both gain options. Switches then introduce extra passive and active components to increase the gain and match the bandwidths.

Advantages All specifications are satisfied in both gains.

Disadvantages The pedestal non uniformity expected in the analog memory is likely to be at best 0.8 mV_{rms}. With a single MIP giving only 4 mV the distortion due to the pedestals in the analog memory will dominate the noise and prevent MIP detection during normal data taking. This point is accepted in the Preshower specification however. Care needs to be taken to ensure that the slow return to zero on the output of the charge pre-amplifier does not introduce a problem due to pile-up.

4.2.3 Switched gain with a transimpedance pre-amplifier

The switched gain structure with a transimpedance pre-amplifier, illustrated as channel (c) in figure 4.3. A transimpedance pre-amplifier produces a very fast symmetrical pulse at the pre-amplifier output proportional to the signal charge. A fast gain stage is switched in and out of the circuit to achieve the different gains. The signal is then shaped by a shaping stage.

Advantages All the design criteria are met by the transimpedance option. In addition a fast signal and fast return to zero (within 25 ns) in the pre-amplifier means that pile up at this level cannot happen.

Disadvantages The resistance in the feedback of the pre-amplifier is quite low which means that only small voltage differences can be achieved between the input and output of the amplifier without applying a large dc current through the feedback. A third mid range dc power supply voltage is needed in order to obtain dc conditions such that a low resistance can be used in the feedback and maintain a large operating range to be sensitive to 1-400 MIPs.

A third power supply would complicate the design of the Preshower system.

4.2.4 Conclusion of channel type

While all 3 channel architectures satisfy the specifications, only the switched gain option with a charge pre-amplifier does so without introducing additional complications.

For this reason the "switched gain with charge sensitive pre-amplifier" option has been chosen by the Preshower as the front-end architecture. The details of the design and measured results are presented in section 4.3.

4.3 DELTA

The name given to the front-end pre-amplifier and switched gain shaper in the Preshower is "DELTA". This section provides details of the design and measured results for DELTA. Most of the details in this section are published in [5].

4.3.1 The DELTA pre-amplifier design

The schematic diagram of DELTA is shown in figure 4.4. The design uses a BiCMOS folded cascode input stage to amplify the signal through T_1 and M_{pc} to node b. An emitter follower then replicates the voltage at b onto a low impedance output node (Out) . The sensor charge is stored as a voltage across capacitors C_{f1} and C_{f2}. The stored charge then decays through R_f restoring the amplifier to its operating point.

For large dynamic range careful consideration needs to be taken with respect to the dc operating conditions. The signal voltage level at the output has a lower limit defined by the saturation voltage $V_{ds_{sat}}$ of $Mn2$ which is 400 mV. The upper limit is defined by $V_{dd} - (Mp1_{Vds_{sat}} + Mpc_{Vds_{sat}})$ which is 3.3 V (assuming V_{dd} =5 V) allowing a total possible negative signal swing of 2.9 V. The pre-amp. gain is set to 6.4 mV/MIP which gives a total possible pre-amp. dynamic range of 450 MIPs.

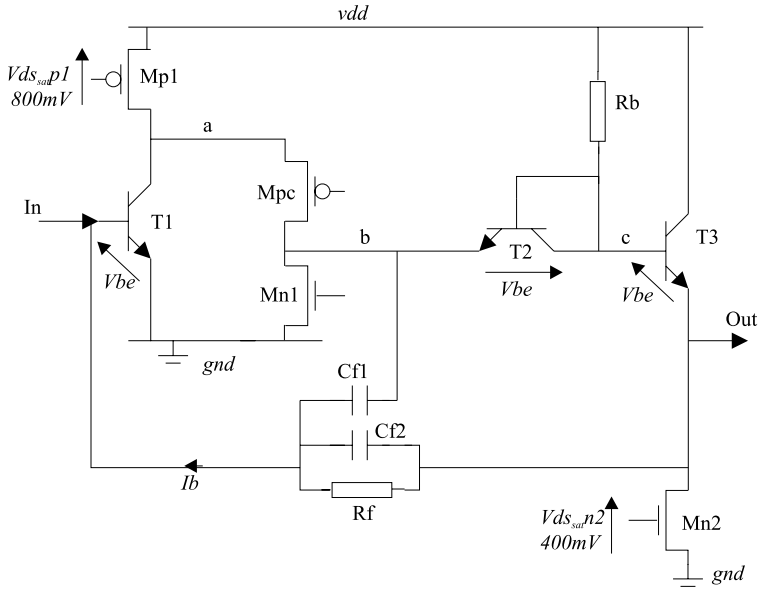

Figure 4.4: The DELTA pre-amplifier circuit.

4.3.2 The leakage current compensation (LCC) circuit

The leakage current compensation (LCC) circuit monitors and subtracts sensor leakage current from the DC coupled input enabling the pre-amplifier to operate despite sensor leakage currents induced by radiation damage.

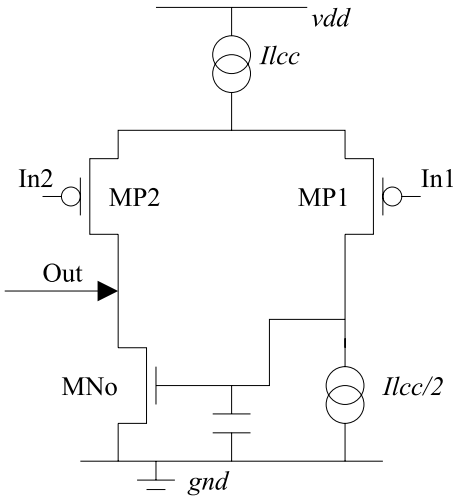

Figure 4.5: The leakage current compensation circuit (LCC)

The LCC circuit is an Operational Transconductance Amplifier (OTA) connected in the feedback of the pre-amplifier [6]. Figure 4.5 shows the schematic diagram of the LCC unit.

Leakage current is compensated by comparing the DELTA output voltage with a reference voltage V_{ref} shown in figure 4.6. Any tendency of the DELTA output voltage to drift to a new operating value is corrected by diverting leakage current from the input of DELTA into the output of the LCC. The main design criteria for an efficient LCC circuit is extremely low bandwidth, very high output impedance and minimum parallel noise contribution from MNo.

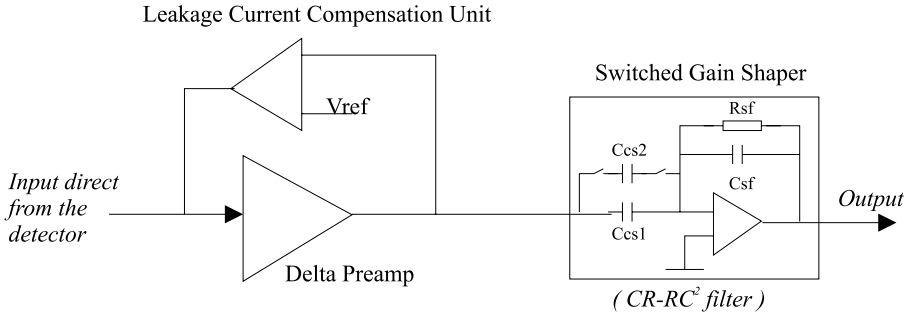

Figure 4.6: The DELTA channel architecture with leakage current compensation (LCC).

4.3.3 The switched gain shaper

The shaper is a second order $CR-RC^n$ filter. The coupling capacitance C_{cs} during normal operation (low gain) is C_1. Increased gain is achieved by switching in extra coupling capacitance C_2 in parallel with C_1 (see figure 4.7).

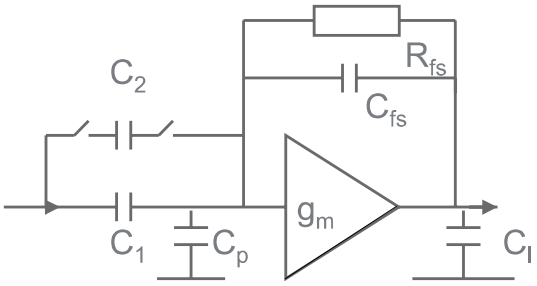

Figure 4.7: The switched gain shaper.

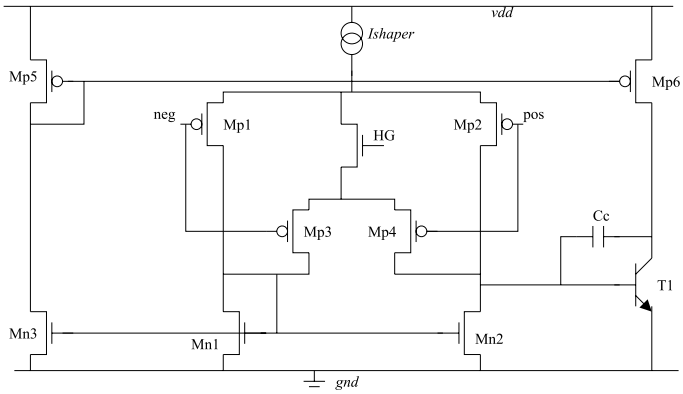

Figure 4.8: Circuit diagram of the opamp used in the shaper with switchable input transconductance.

It is important to match the central frequency (ω_c) and hence peaking time (T_p) in both high and low gains. The equation for ω_c [1] is given by equation 4.9.

$$\omega_c = \frac{1}{T_p} = \frac{1}{C_t}\left(\frac{g_m C_{fs}}{C_o} + \frac{1}{R_{fs}}\right) \tag{4.9}$$

where $C_t = C_{cs} + C_{fs} + C_i + C_p$, $C_o = C_l + C_{fs}$, R_f the feedback resistance and g_m the input transconductance of the shaper amplifier. The condition to match peaking times $\omega_{cHG} = \omega_{cLG}$ can be approximated to equation 4.10.

$$\frac{g_{mHG}}{C_{tHG}} = \frac{g_{mLG}}{C_{tLG}} \tag{4.10}$$

Figure 4.8 shows the circuit diagram for the amplifier used in the shaper. The change in g_m is achieved by switching in an extra differential pair (transistors $Mp3$

and $Mp4$) in parallel with transistors $Mp1$ and $Mp2$, hence increasing the effective W/L ratio of the input transistors therefore increasing the g_m.

4.3.4 Noise analysis

The noise model for the channel is shown in figure 4.9.

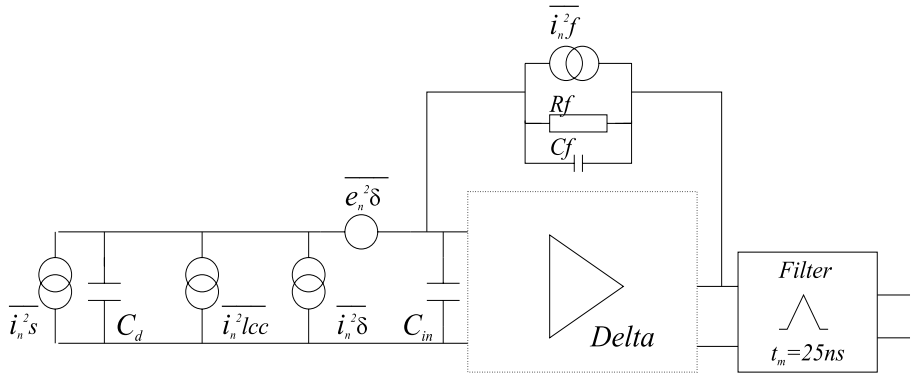

Figure 4.9: The DELTA channel noise model with an ideal filter.

Equations 4.11 to 4.15 show the rms equivalent noise current and voltage generators when referred to the input. Equations 4.11 and 4.12 refer to DELTA and are defined on the properties of the input NPN transistor (T_1) where :

- i_b is the base current,
- R_{eq} its equivalent noise resistance,
- $r_{bb'}$ its extrinsic base resistance,
- g_m its transconductance,
- (q) is the electron charge,
- (k) Boltzmann's constant,
- T is temperature.

Equation 4.13 shows the contribution from the feedback resistor which is made negligible with a high value R_f. The contribution from the LCC unit is shown in equation 4.14 and is made negligible due to a low $g_{m(Lcc_{Mno})}$. The rms equivalent noise current generator from the sensor is given in equation 4.15. The noise may then be expressed as Equivalent Noise Charge (ENC) as in equations 4.16 (for parallel noise) and 4.17 (for series noise) where I_1 and I_2 are weighting functions relating to the filter characteristics (explained in the appendix A). The total ENC_t is the quadratic sum of these two components, equation 4.18.

$$\frac{\overline{i_{n\delta}^2}}{\Delta f} = 2\,q\,i_b \;\; where \;\; i_b = \frac{i_c}{\beta} \tag{4.11}$$

$$\frac{\overline{e_{n\delta}^2}}{\Delta f} = 4\,k\,T\,R_{eq} \;\; where \;\; R_{eq} = r_{bb'} + \frac{1}{2\,g_m} \tag{4.12}$$

$$\frac{\overline{i_{nf}^2}}{\Delta f} = \frac{4\,k\,T}{R_f} + \frac{(\overline{e_{n\delta}^2}/\Delta f)}{R_f^2} \tag{4.13}$$

$$\frac{\overline{i_{nlcc}^2}}{\Delta f} = 4\,k\,T(\frac{2}{3})\,g_{mlcc(MNo)} \tag{4.14}$$

$$\frac{\overline{i_{ns}^2}}{\Delta f} = 2\,q\,i_s \tag{4.15}$$

$$\overline{ENC_p^2} = \frac{\sum(\overline{i_n^2}/\Delta f)}{2}\,I_2 \tag{4.16}$$

$$\overline{ENC_s^2} = \frac{\overline{(e_{n\delta}^2}/\Delta f)\,(C_d + C_f + C_{in})}{2}\,I_1 \tag{4.17}$$

$$\overline{ENC_t} = \sqrt{\overline{ENC_p^2} + \overline{ENC_s^2}} \tag{4.18}$$

There are important implications in the design of the input transistor T_1 for optimising the ENC for a given input capacitance. Note that $\overline{e_{n\delta}^2}/\Delta f$ is proportional to $r_{bb'}$ which could be reduced by increasing its emitter area.

Also $\overline{i_{n\delta}^2}/\Delta f$ is inversely proportional to the β of T_1 . β however degrades through irradiation, the magnitude of which depends on its current density. Reducing the emitter area of T_1 increases current density resulting in a less severe β degradation after irradiation. Therefore minimum $\overline{i_{n\delta}^2}/\Delta f$ is achieved with minimum emitter area.

In the test chip various channels were designed with different size input transistors to investigate this effect. A well modelled NPN device in DMILL technology is called "DNPN10" which has an emitter area of 12 μm^2. Channels were designed with 1, 2, 4 and 8 of these devices in parallel to make up T_1. The number of devices in parallel (n) is therefore an important design parameter to optimise noise.

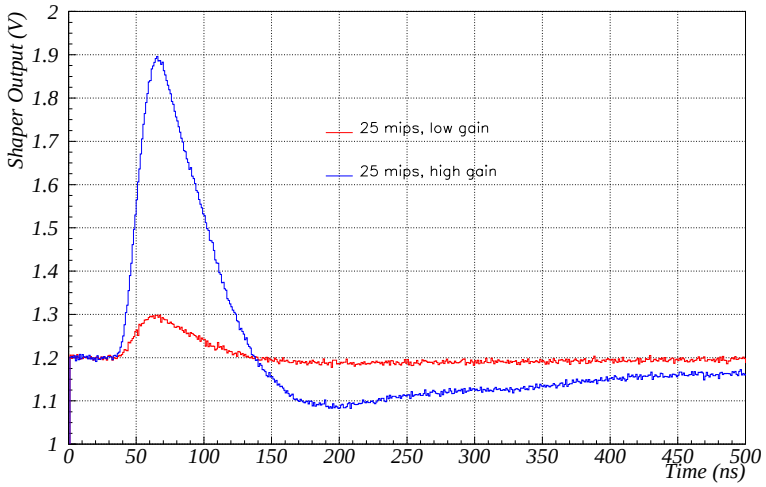

Figure 4.10: Signal response in both high and low gain for 100 fC of input charge.

4.3.5 Measured results before irradiation

All measurements have been made using test pulses to inject charge corresponding to 4 fC for each equivalent 1 MIP. Unless otherwise stated the input loading capacitance is 58 pF.

The signal response for both high and low gains is shown in figure 4.10 for 100 fC of input charge corresponding to 25 MIPs. The undershoot is approximately 14% and returns to the operating point after ∼600 ns.

Peaking times in both gains are matched to 25 ns. The rise time for both gains was measured, the results being shown in figures 4.11 and 4.12. The rise time is shown to be constant within the operating range of both gains. There is a difference of 2 ns however between the two gains. Crosstalk has been measured at $< 2\%$ worst case to the nearest neighbour.

Pile up conditions have been tested using an input pulse corresponding to 20 MIPs at a rate of 5 MHz with no adverse effects on performance. Pythia simulations show the maximum expected pile up condition in the CMS Preshower to be 2 MIPs at 2 MHz average.

The dynamic range for both gains can be seen in figure 4.13. The required dynamic ranges are met i.e. 50 MIPs for high gain and 400 MIPs for low gain. The channel gain is approximately 30 mV/MIP in high gain and 4 mV/MIP in low gain. It is not perfectly linear. The gain/MIP (shown in figure 4.14) increases by approximately 7% over the full signal range. This is due to an increase of g_m in T_1 for large input signals as predicted by simulation. A slight non linearity on the signal response is not a concern for the Preshower and will be discussed further in chapter 5.

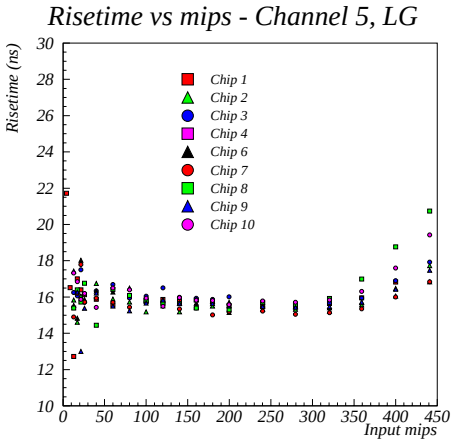

Figure 4.11: Rise time (measured between 10% and 90% of peak voltage) as a function of input signal in low gain.The rise time is constant over the signal range at $\sim$ 16 ns

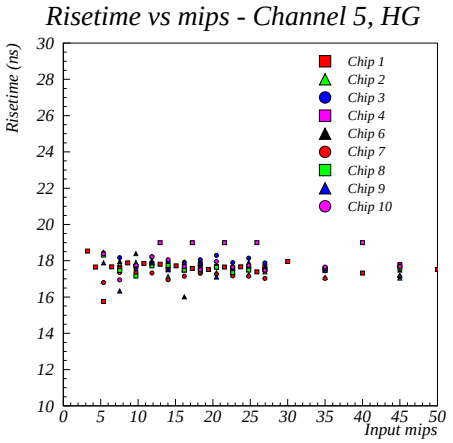

Figure 4.12: Rise time (measured between 10% and 90% of peak voltage) as a function of input signal in high gain.The rise time is constant over the signal range at $\sim$ 18 ns

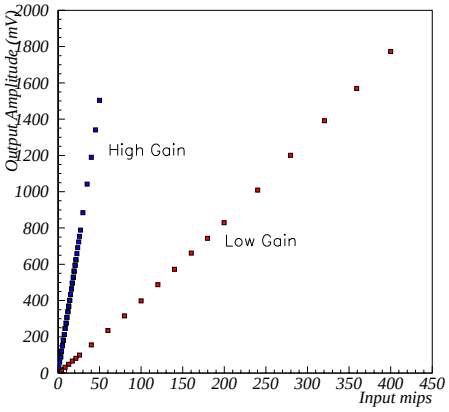

Figure 4.13: Dynamic range for both high and low gain.

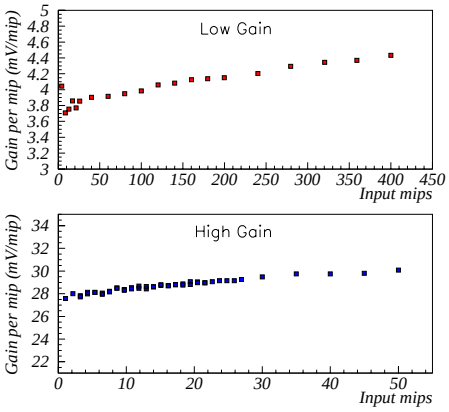

Figure 4.14: Gain per MIP over the full dynamic range.

Figure 4.15 shows the normalised gain verses sensor leakage current. The gain remains virtually constant for up to 150 μA of leakage current. This is well beyond the requirement of the Preshower which is 20 μA per strip after 10 years of operation at LHC.

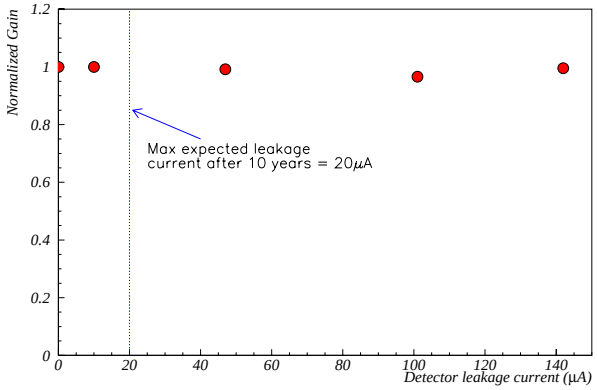

Figure 4.15: Normalised gain verses sensor leakage current. The gain remains almost constant for I_{leak} <150 μA. The Preshower specification of $I_{leak(max)}$ =20 μA is also indicated.

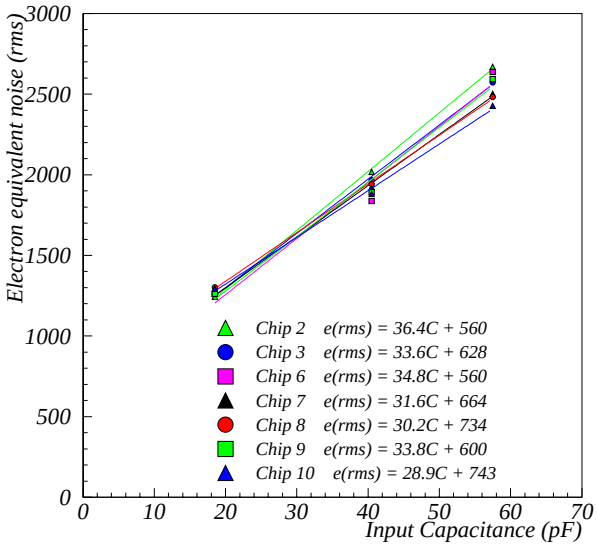

Figure 4.16: Noise performance expressed as ENC for different levels of total input capacitance (measured in high gain). A linear fit has been made to each chip measured where C represents the input capacitance in pF.

The noise performance (measured in high gain) before irradiation is shown in figure 4.16. The ENC of 7 chips are plotted against input capacitance. The average ENC is 640 e + 33 e/pF rms based on a linear fit. This shows that to achieve a $S/N > 10$ the total input capacitance should be < 56 pF.

4.3.6 Measured results after irradiation

Two chips were measured after exposure to ionising radiation up to a total dose of 10 Mrads(Si) using an Xray source. Another two chips were irradiated with neutrons to a fluence of 4×10^{13} n cm^{-2}. Measurements were made shortly after irradiation with no attempt to anneal.

The effect on signal response can be seen in figures 4.17 and 4.18. In both cases the basic shape of the response is unchanged. The gain is affected however. After ionising radiation the gain has increased by 17% and after neutron irradiation the gain has decreased by 14%. The gain decrease is due to β degradation and should affect the result for both types of irradiation. The apparent increase in gain after ionising radiation was found to be due to an increase in the DELTA feedback resistance R_f . A test structure on the chip enabled precise measurement of this resistor showed an increase in resistance of 50% after ionising radiation but no change after neutron irradiation. This type of resistor (RHV) in DMILL technology is therefore not radiation tolerant and should not be used. Another type of resistor exists which is radiation tolerant and was chosen to be used in subsequent designs.

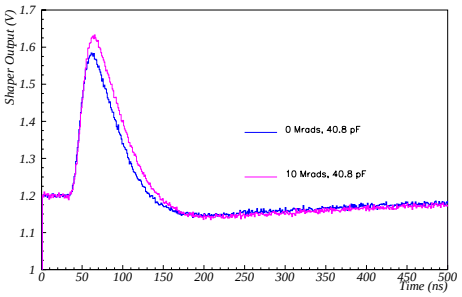

Figure 4.17: Signal response after 10 Mrads(Si) of ionising radiation

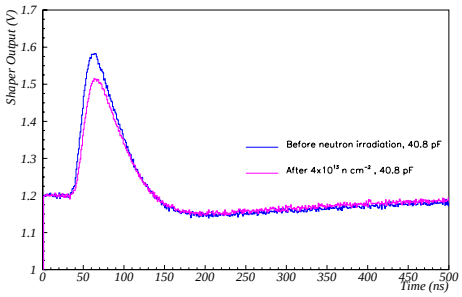

Figure 4.18: Signal response after exposure to a neutron fluence of $4 \,.\, 10^{13}\, n\, cm^{-2}$

4.3.7 Optimisation of the input bipolar transistor

The most important device in the circuit from a noise point of view is the input NPN transistor T_1. The β of this device was expected to degrade after irradiation and test structures were placed in the chip in order to measure this. Figures 4.19 and 4.20 plot β as a function of collector current (I_c) before and after irradiation. The extent of β degradation due to ionising and neutron irradiation is tabulated in table 4.1. The equivalent value of n for T_1 is indicated to correspond with the current density.

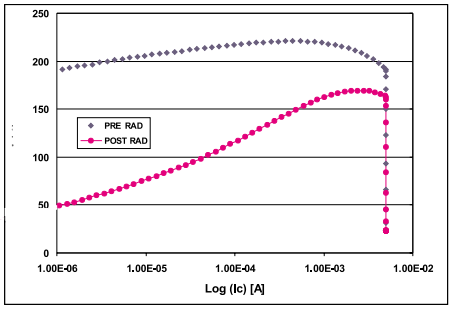

Figure 4.19: β against collector current before and after 10 Mrads(Si) of ionising radiation

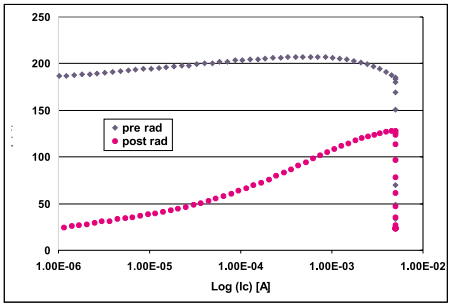

Figure 4.20: β against collector current before and after a neutron fluence of $4{\times}10^{13}$ n cm^{-2}

n	Current density	β w.r.t. ionising radiation			β w.r.t. neutron irradiation		
		pre-rad.	10 Mrad(Si)	degradation	pre-rad.	4×10^{13} n cm^{-2}	degradation
1	400 μA	220	145	-34%	207	90	-57%
2	200 μA	219	130	-40%	206	76	-63%
4	100 μA	217	117	-46%	204	66	-68%
8	50 μA	213	102	-52%	201	53	-74%

Table 4.1: β before and after radiation as a function of the number of NPND10 devices in parallel (n).

Figures 4.21 and 4.22 show the measured ENC at C_{in} = 58 pF for 4 channels designed with different values of n for T_1 both before and after irradiation.

The effect on the series noise due to the increase in $r_{bb'}$ as n tends to 1 is dramatic for large values of input capacitance. The increased noise after irradiation due to β degradation is hardly visible. The series noise component dominates by far. Based on these results one can conclude that a suitable design value for n is 3 or 4, which maintains low noise with moderate β degradation after irradiation.

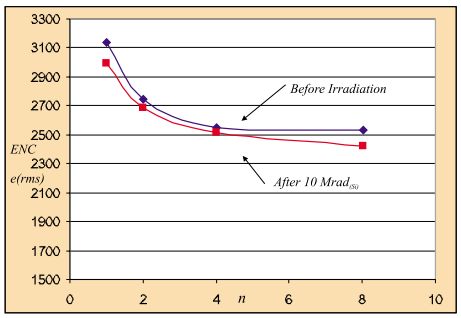

Figure 4.21: Measured ENC at $C_{in} = 58$ pF for channels designed with different numbers of input devices in parallel (n) before and after ionising radiation.

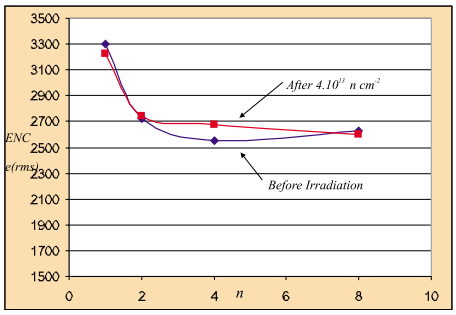

Figure 4.22: Measured ENC at $C_{in} = 58$ pF for channels designed with different numbers of input devices in parallel (n) before and after neutron irradiation.

4.3.8 Conclusions from measurements of DELTA

This section has presented the design and results of the DELTA preamplifier and switched gain shaper. The results show that DELTA is suitable for silicon strip readout with a $S/N > 10$ for a total input capacitance < 56 pF.

The optimum number of NPND10 devices to use for T1 is n = 3 or 4.

Radiation hardness is demonstrated up to 10 Mrads(Si) of ionising radiation and 4×10^{13} n cm^{-2}.

All design requirements for the Preshower front-end are met with the exception of neutron radiation hardness. Further irradiation tests will be necessary to a fluence beyond 2×10^{14} n cm^{-2} before this can be confirmed.

DELTA is suitable to be used as the Preshower front-end amplification stage. It will be used for a new PACE design (PACE2) in DMILL, which is the subject of chapter 5.

4.4 DeltaStream

The Preshower silicon sensors are to be produced in up to 4 regional centres. The regional centres will also be responsible for production testing and construction of the micro-modules.

In order to maintain consistency between test methods and results a common silicon sensor test system is under development. The test system involves a laser that can activate a single sensor channel with a given energy. In this way noisy channels can be identified.

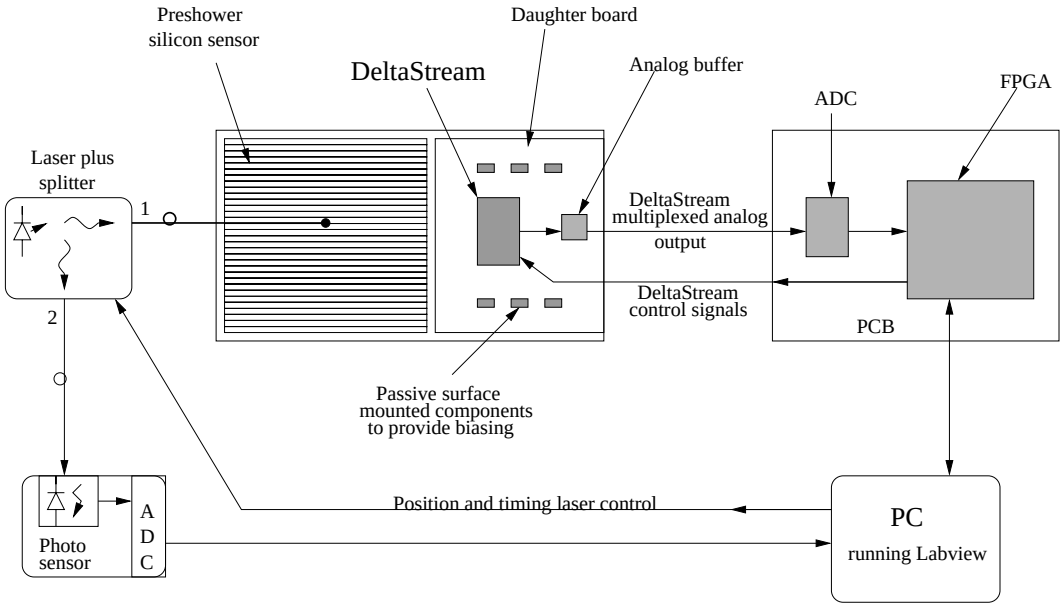

Figure 4.23: Silicon sensor laser measurement system using DeltaStream

Figure 4.23 shows a block diagram of the sensor test system. A laser is used to generate pulses of light with wavelength 1060 nm at frequencies in the kHz region [7]. A passive "splitter" is used to divide the light into two parts. Fibre optic cables are used to direct the light of the two parts towards a photo sensor and a well focused region on the silicon sensor. The light spot on the silicon sensor has a diameter of <20 μm which is well within the strip width of 1.74 mm. Windows have been made in the aluminium on the silicon sensors to allow the light to penetrate the silicon without severe reflection. The light then generates electron / hole pairs as it passes through the full depth of the depletion region. The attenuation length of 1060 nm light in silicon is 1 mm and the sensor thickness is 300 μm.

DeltaStream is the front-end electronics used to convert charge gathered on each sensor strip into a stream of analog voltage values that can be digitised by an ADC. In parallel, the photo sensor produces a voltage proportional to the light contained in the second branch of the splitter, which is also digitised. The data from the two branches are compared off-line to study the charge collection from each strip in the silicon sensor.

4.4.1 DeltaStream design details

The electronics needed in such a test system ideally had to have the same analog properties as PACE2. PACE2 itself could be used but its complexity is far beyond that needed for the tests. For this reason a chip called "DeltaStream" was developed in DMILL technology, which contained the same analog properties as PACE but without the complexity.

Figure 4.24 shows the block diagram for DeltaStream. DeltaStream followed an architecture used in the AMPLEX family of ASICs [8] [9]. DeltaStream differed from these other designs in its analog properties and speed of multiplexed readout.

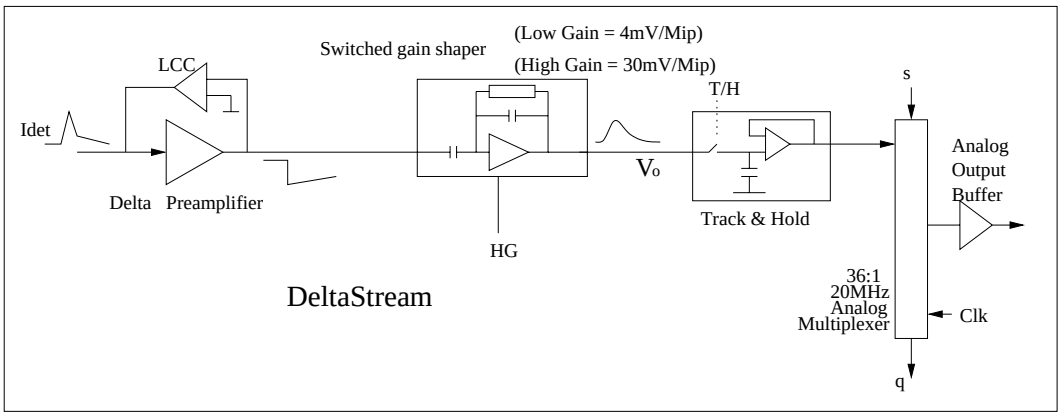

Figure 4.24: Block diagram of DeltaStream. DeltaStream consists of 36 identical channels including the DELTA pre-amplifier and switched gain shaper plus a track & hold stage. A 36:1 multiplexer feeds to a single analog buffered output.

DeltaStream consists of 36 identical channels consisting of the DELTA pre-amplifier and switched gain shaper plus a "track & hold" circuit. The outputs from the 36 track & hold circuits feed into an analog multiplexer. The multiplexer serialises the sampled analog voltage from each channel into a stream of analog values. The stream of analog samples are then buffered to a single analog output.

The DELTA amplifier and shaper is identical to the design explained in section 4.3 with the exception of one small modification. The modification involves the substitution of a different type of resistor structure (for R_f in figure 4.4) in place of the previous high value RHV resistor. The reason is to avoid the gain drop observed after neutron irradiation shown in figure 4.18. The substituted resistance has the same absolute value but has a lower resistance value per square. This results in a larger layout area and hence larger parasitic capacitance to the substrate. Simulations have shown that the extra capacitance has a small speed impact on the response from the DELTA pre-amp. but that the pulse shape after shaping remains unchanged. The analog signal response from the shaper in DeltaStream should therefore be the same as explained in section 4.3.

4.4.2 The track & hold circuit plus a 20MHz multiplexer.

The complexity of a large analog memory and associated control circuitry is reduced to a single storage element in the form of a track & hold circuit.

Figure 4.25 shows in a simplified schematic form the track & hold circuit followed by the multiplexer and output buffer.

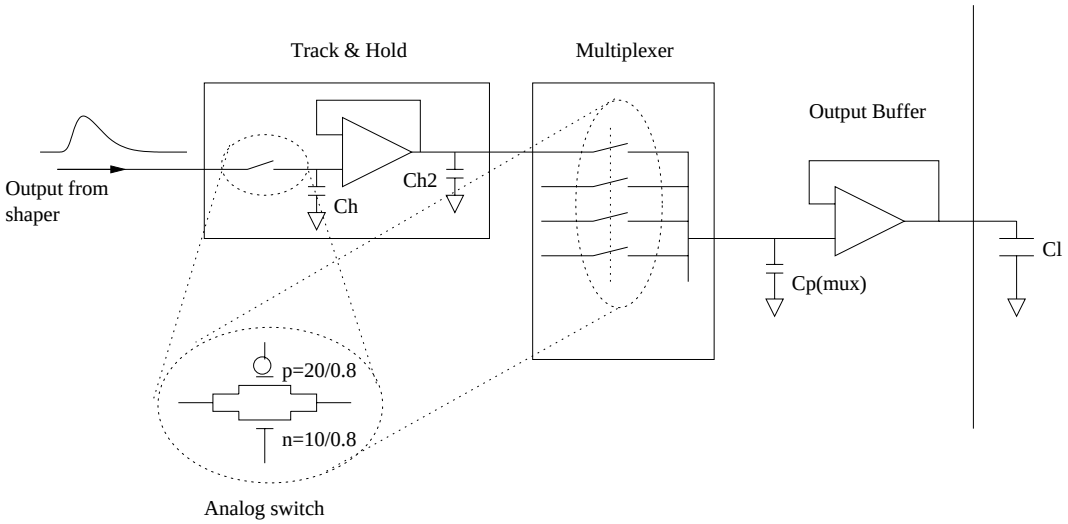

Figure 4.25: The track & hold plus multiplexer circuit.

The track & hold circuit contains a switch, storage capacitor (C_h) and an amplifier. If the switch is closed the amplifier output follows the signal shape at the input "Track", if the switch is open the amplifier output maintains the voltage stored on C_h, "Hold".

In order to faithfully reproduce the shaper voltage on C_h and maintain the dynamic range of DELTA, care has to be taken in the design of the analog switch. A closed switch followed by C_h can be thought of as a resistor and parallel capacitor, hence a low pass filter. It is clear that the RC time constant should be small to allow the voltage on C_h to track the shaper output which has a rise time of 25 ns. A single MOS transistor operating in the linear region could be used as a switch which has an "on" resistance R_{on} as given in equation 4.19.

$$R_{on} = \frac{1}{\frac{W}{L}\mu_n C_{ox}(V_{gs} - V_t)} \tag{4.19}$$

where :

- $\frac{W}{L}$ is the ratio of transistor gate width over gate length
- μ is the electron mobility in the channel region (μ_p if the transistor is a PMOS)
- C_{ox} is the capacitance of the gate oxide
- V_{gs} the gate voltage with respect to the source

- V_t the transistor threshold voltage ($\sim$ 0.8 V).

μ, C_{ox} and V_t of equation 4.19 are all process dependent parameters leaving $\frac{W}{L}$ and V_{gs} as handles for the designer. The $\frac{W}{L}$ ratio of the transistor can be increased to lower R_{on} however, doing so increases the parasitic capacitive coupling between the gate and the source. On turning off the switch, charge is injected from the gate to the storage node of C_h causing an error on the sampled voltage. The $\frac{W}{L}$ value should hence be chosen to reduce R_{on} sufficiently without causing severe disruption of the sampled signal.

V_{gs} is predetermined by the gate voltage (V_g) minus the voltage on the shaper output (V_{sh}) which is in the range: $1V < V_{sh} < 3V$. $V_{gs} - V_t$ will hence vary from 1.2V to 3.2V causing a strong variation in R_{on} depending on the signal value (V_{sh}), introducing distortion.

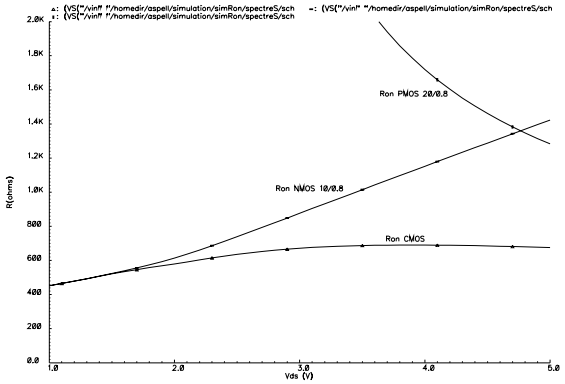

Figure 4.26: The "on" resistance (R_{on}) of the CMOS analog switch.

Combining both an NMOS and a PMOS transistors in parallel to form a CMOS analog switch allows a relatively constant "on" resistance to be achieved as one device compensates the other.

Figure 4.26 shows a simulation of "on" resistance for NMOS and PMOS devices with $\frac{W_n}{L_n} = \frac{10\mu m}{0.8\mu m}$ and $\frac{W_p}{L_p} = \frac{20\mu m}{0.8\mu m}$ respectively. Both individual resistances and the combined R_{on} are plotted. The combined devices show R_{on} $\sim$620 Ω.

With $R_{on} = 620\ \Omega$, the RC time constant ($\tau = 620$ ps). Simulations have shown that the dynamic range can be maintained through this switch when sampling on the peak of the shaper pulse shape.

The opamps used in the track & hold circuit and the output buffer both have the same internal structure as shown in figure 4.27. The opamp is based on a differential PMOS input stage and a pseudo class AB output stage [10]. This type of opamp is a very versatile structure that can be used for a number of different circuit configurations. A full analysis of the circuit and design equations are given in [11].

The requirements on the output buffer are that it should drive a 15 pF load with a 2 V swing without prolonged ringing. Since the multiplexer is running at 20 MHz the signal value should be stable after 40 to 50 ns for sampling by an ADC. This means

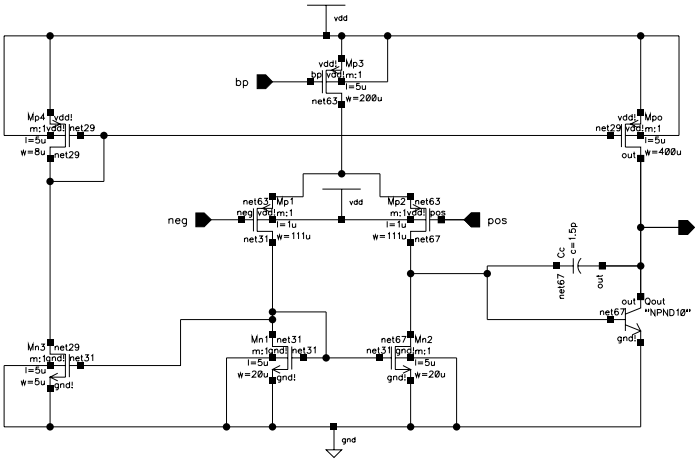

Figure 4.27: Basic two stage opamp structure as used in the track & hold circuit and the output buffer. The transistor $\frac{W}{L}$ values and compensation capacitor C_c are as for the Output buffer.

the amplifier needs to have a sufficiently large gain bandwidth (GBW >50 MHz) but also be sufficiently damped (phase margin ϕM > 45^o).

The opamp used in the track & hold circuit needs to be fast if one wishes to use it to read out the full pulse shape on a single channel (see "single channel mode in section 4.4.3). Otherwise the speed of operation is determined by the time interval between the sampling of V_{sh} on C_h and the start of the multiplexing (see "multiplex mode" in section 4.4.3) . This enables the speed requirements on the opamp to be relaxed reducing the power consumption.

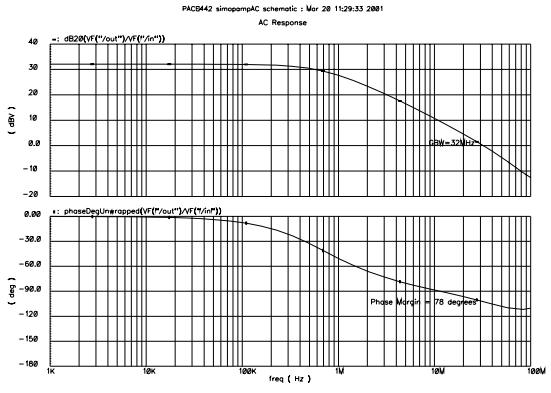

Figure 4.28: Bode diagram for the opamp used in the track & hold circuit.

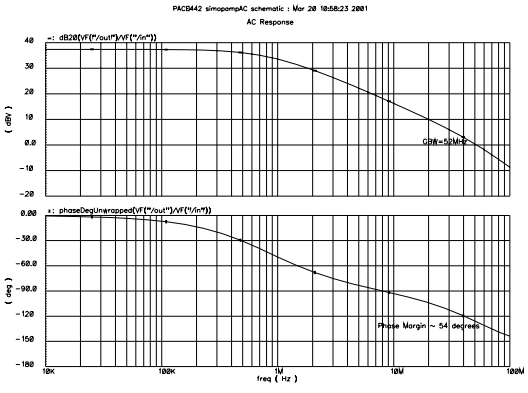

Figure 4.29: Bode diagram for the output buffer opamp.

Figures 4.28 and 4.29 show the frequency response for the two operational amplifier circuits and table 4.2 summarises the readings from the curves.

Circuit	**Gainbandwidth (GBW)**	**Phase Margin (ϕM)**	**Power Consumption**
Output Buffer	52 MHz	54^o	7.4 mW (bias I = 200 μA)
T/H	32 MHz	78^o	7.4 mW (bias I = 200 μA)
T/H (low power)	7 MHz	102^o	740 μW (bias I = 20 μA)

Table 4.2: Performance of the opamps used in the track & hold (T/H) and Output buffer circuits.

The drain capacitance of one analog switch is 42 fF. The output node of the multiplexer is connected to each channel by a metal line which has a calculated parasitic capacitance of 462 fF. The total parasitic capacitance of the multiplexer output node including the metal line and 36 drains is approximately 2 pF and represented by $C_{p(mux)}$ in figure 4.25. $C_{p(mux)}$ is therefore charged up and down during 50 ns cycles with up to 2 V. The parasitic capacitance on the output node of the multiplexer is naturally much greater than the parasitic capacitance on the inputs to the multiplexer. This can cause a problem when switching from one channel to another. Charge sharing from $C_{p(mux)}$ couples through the switch and disturbs the voltage on the newly selected channel.

Increasing the current sink and source capability of the track & hold opamp is one possibility but this increases power consumption. An easier method is to deliberately load the output node of the track & hold circuit with a capacitor to equilibrate the capacitive imbalance between the two sides of the multiplexer. This is the method chosen in this design where C_{h2} represents the load capacitor on the track & hold opamp. The track & hold opamp can then slowly charge C_{h2} keeping the power consumption low before fast multiplexing begins.

Figure 4.30 shows the layout for DeltaStream. The 36 channel inputs are on the left. The power supply and biasing is applied externally through the pads located at the top and bottom of the chip. The analog readout buffer is located in the middle of the right side of the chip.

The multiplexer has its own power supply which together with the multiplexer control signals arrives in the lower right side of the chip. A guardring surrounds the multiplexer to protect the analog part of the chip from charge injected into the substrate from the digital signals.

The overall dimensions of the chip are 3.115 mm $\times$ 5.106 mm = 15.9 mm^2.

4.4.3 DeltaStream measured results

Before entering into the description of the measurements a short description of the measurement board is necessary. The DeltaStream chip is mounted without packaging on a daughter board which itself is plugged into a mother board. Figure 4.31 shows

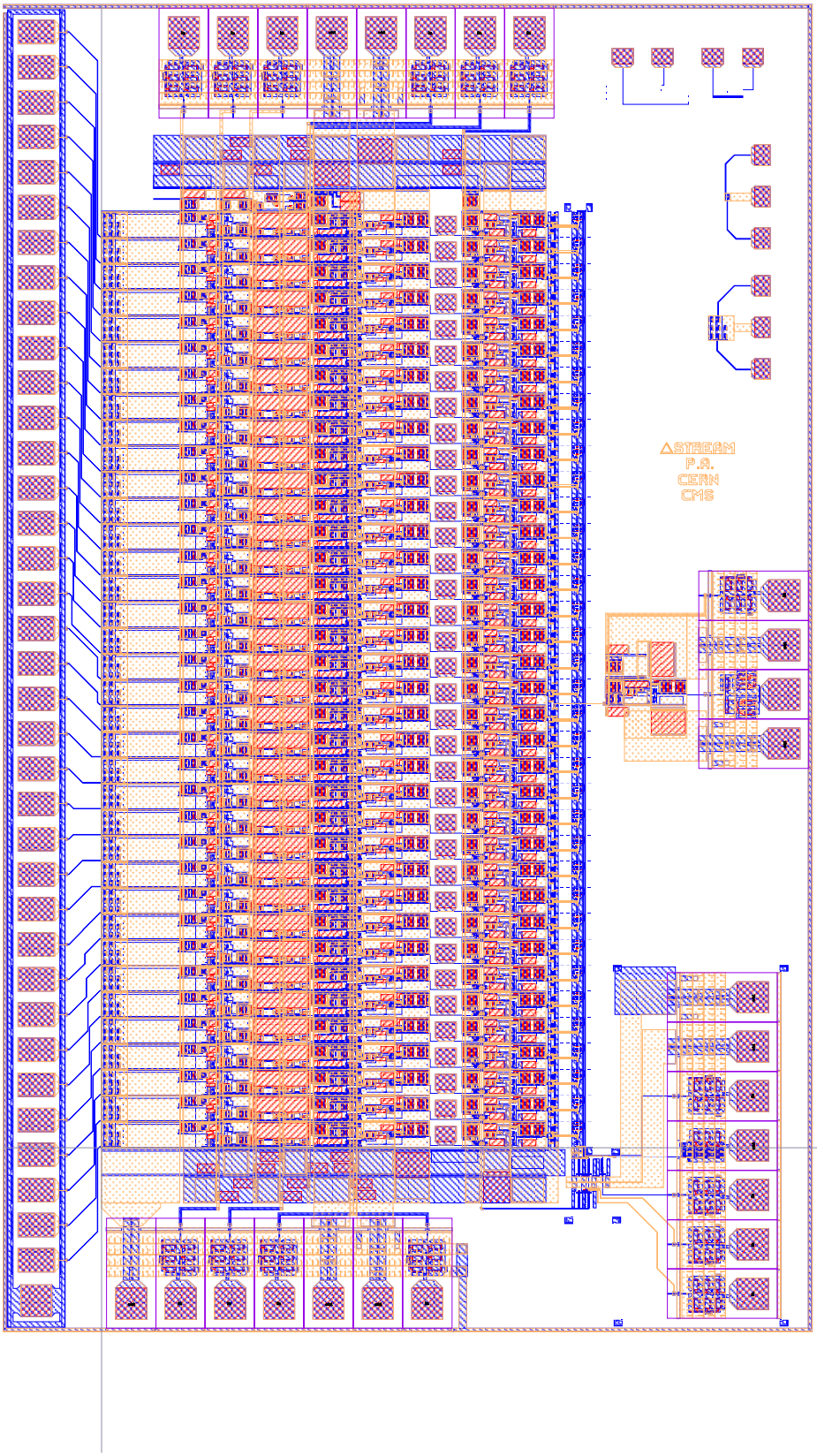

Figure 4.30: Layout of DeltaStream.

the two boards together, a glass shield has been placed over DeltaStream to protect it from accidental damage.

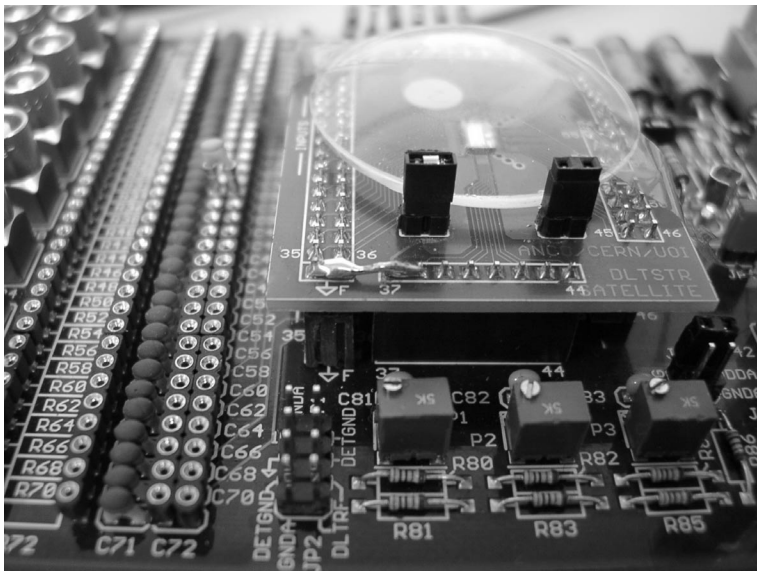

Figure 4.31: DeltaStream measurement board.

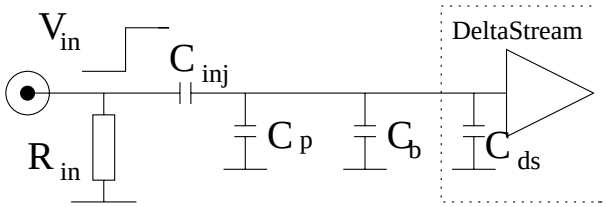

Figure 4.32: Schematic diagram of the input to each channel in DeltaStream.

The input signal is provided by a step voltage pulse injected into a series capacitor to provide the signal charge of 4 fC to 1600 fC (the equivalent of 1 to 400 MIPs). The parasitic capacitances associated with the input are important to determine since a number of measurements (in particular the noise) depend on total input capacitance. Figure 4.32 shows a schematic diagram of the input stage where :

- C_{inj} is the series capacitance used to generate a charge when a step voltage is applied. There is one (1.8 pF) capacitor per channel seen in figure 4.31 as a long line of capacitors above the label C71.

- C_b represents the parasitic capacitance of the mother and daughter board together. Due to a fan-in there is increasing capacitance towards the outer channels (channels 1,2 and 35, 36) compared to the middle (channels 18, 19). The outer channels have been measured at $\sim$ 11 pF while the middle are $\sim$ 10 pF. The average value across all channels is $C_b = 10.6$ pF.

- C_p is additional parallel capacitance that can be deliberately inserted in order to load the input with capacitance similar to that of a silicon sensor.

- C_{ds} is the input capacitance of a channel in DeltaStream due to the input bipolar transistor which has been calculated at $C_{ds} = 770$ fF.

- R_{in} is the termination resistance for the incoming voltage pulse. R_{in} =50 Ω.

The inherent board capacitance is defined as $C_i = C_{inj} + C_b + C_{ds} = 13.2$ pF ±0.8 pF depending on the channel number.

Measurements are therefore made with a total input capacitance (C_{in}) of $C_{in} = 13.2$ pF ±0.8 pF $+C_p$. A number of the following plots show measured results for additional capacitance values of $C_p = 0$ pF and $C_p = 39$ pF resulting in $C_{in} = 13.2$ pF ±0.8 pF and $C_{in} = 52.2$ pF ±0.8 pF respectively.

DeltaStream can be operated in two modes with respect to the use of the multiplexer. The two modes of operation are called "Single channel mode" and "Multiplex mode".

- **Single channel mode** A static shift register is used within the multiplexer to switch from one channel to the next. Since the shift register is composed of static flip-flops, the clock may be stopped and the corresponding channel will be connected through to the output buffer indefinitely. The multiplexer can hence be used to select a single channel. If the track & hold circuit is put in continuous track mode then the full pulse shape from the shaper may be observed on the output.

- **Multiplex mode** Multiplex mode is using the track & hold circuit plus multiplexer as already described. The pulse shape from the shaper is sampled on the peak and then the sampled values of all 36 channels are multiplexed into a single analog stream at 20 MHz.

Figure 4.33 shows the timing of DeltaStream control signals for the two modes of operation.

Figure 4.34 shows the oscilloscope image in single channel mode. In this case 36 clocks were delivered to the chip to select the last channel (chan. 36). The chip was then placed into a "track" condition and stimulated with a charge pulse of 4 fC (1 MIP) at the input. The resulting pulse shape is evident.

The dc offset of each channel is shown in Figure 4.34 during the multiplexing operation. This can be compared with graph of baselines (figure 4.37 taken when individually selecting different channels).

To demonstrate the track & hold circuit, figure 4.35 shows the output when the transition from track to hold occurs on the peak of the signal response.

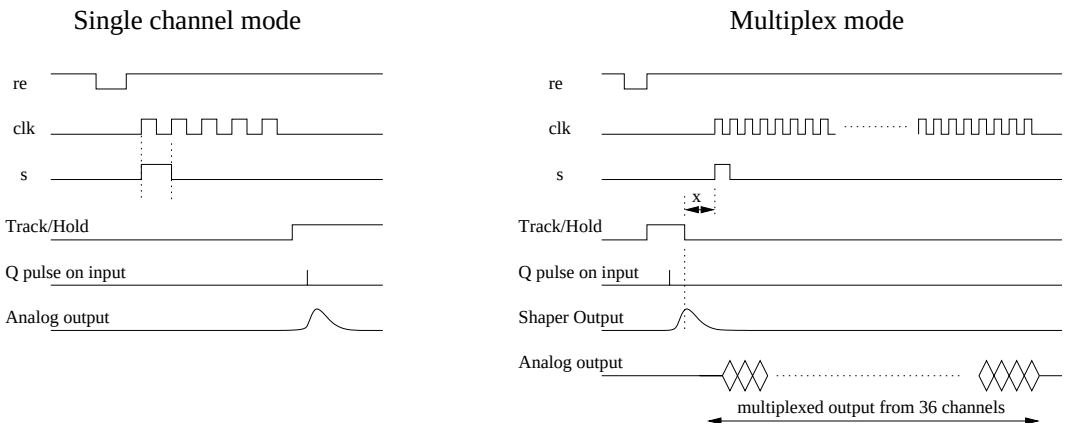

Figure 4.33: Operating DeltaStream in "single channel mode" and "multiplex mode".

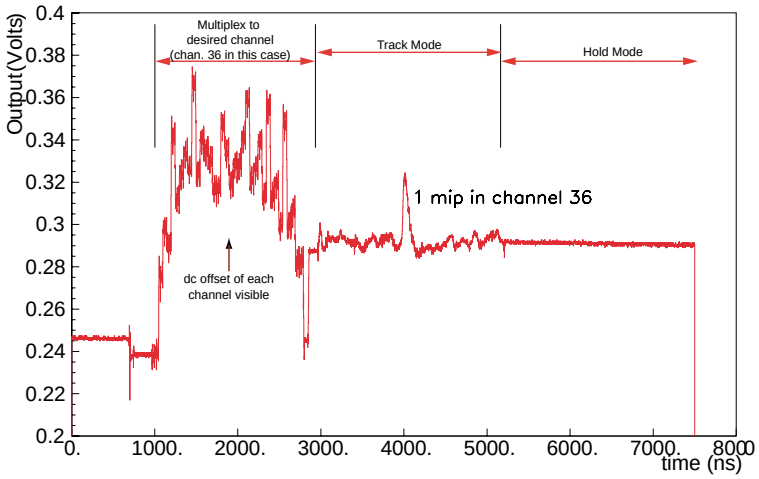

Figure 4.34: DeltaStream in single channel mode.

The signal response for 1 MIP is shown in 4.36. The measurement is the average result of a number of synchronous 4 fC input signals with the circuit in single channel mode. The gain is measured from the baseline to the peak and the rise time from 10% to 90% of the signal amplitude.

Of particular interest in DeltaStream compared to the DELTA test chip of section 4.3 is channel to channel variation of parameters. The following plots of parameters such as baseline dc levels, rise time, gain, linearity and noise have been measured for a number of channels on the chip and their variation about a mean value calculated.

Variations in the baseline are examined in figure 4.37 which shows the measured dc level for each channel. The peak to peak baseline variation is 91 mV in low gain (LG) and 69 mV in high gain (HG). In both cases there is a pattern in the form of a hump. The most likely explanation for this hump is a progressive voltage drop on the power lines which run vertically from channel to channel. Since the layout

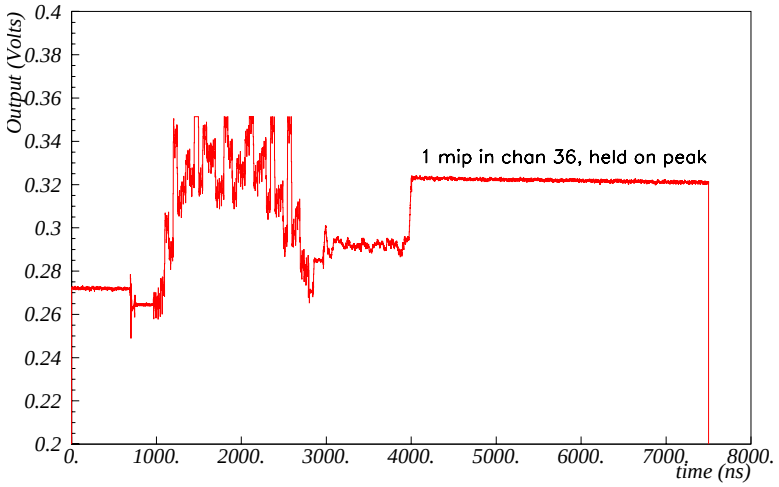

Figure 4.35: Track and hold on the signal peak.

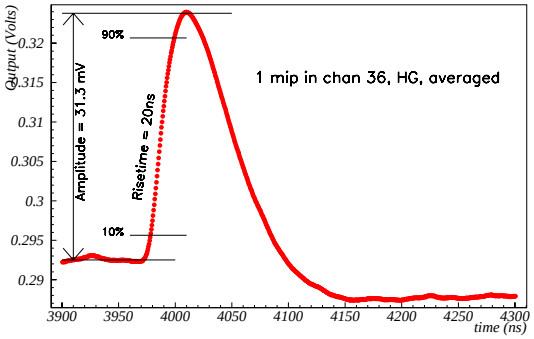

Figure 4.36: The signal response for 1 MIPs in high gain.

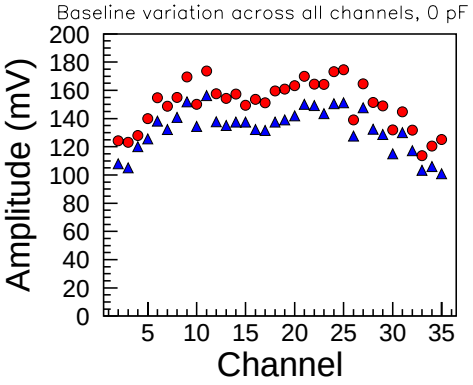

Figure 4.37: Form of dc variations from channel to channel (triangles are measured in low gain, circles in high gain).

feeds power to both the top and the bottom, the region with the largest power supply voltage drop will be the centre. The power lines have been made in an upper metal layer flowing over the top of the active components and have been laid out with the maximum possible width to try to minimise the series resistance. A star distribution of power would be the ideal method to maintain the same conditions for each channel but this would require a much larger surface area. A compromise between the two

layout techniques may be the solution for the final design to obtain a flatter pedestal profile. Measurements of the baseline were made with $C_p = 0$ pF and $C_p = 39$ pF with no apparent effect due to input capacitance.

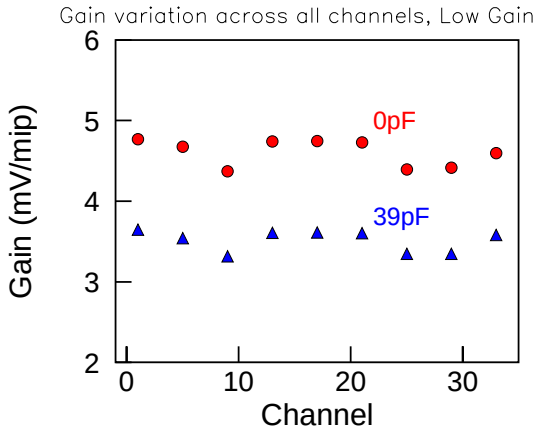

Figure 4.38: The measured gain spread (in low gain) against channel number.

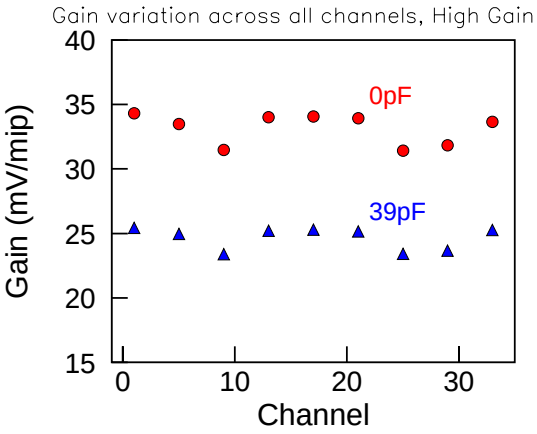

Figure 4.39: The measured gain spread (in high gain) against channel number.

Figures 4.38 and 4.39 show the gain measured for each channel in low and high gain. The mean gain in LG is 4.62 mV with $C_p = 0$ reducing to 3.44 mV with $C_p = 39$ pF. In HG the mean gain is 33.12 mV with $C_p = 0$ reducing to 24.57 mV with $C_p = 39$ pF. Channel to channel variation of gain has been calculated as the standard deviation (σ) around the mean which is $\sim$100 μV (LG) and $\sim$1 mV (HG). The exact values are given in the summary table 4.3.

Figures 4.40 and 4.41 show the rise times measured for each channel in low and high gain for $C_p = 0$ pF and $C_p = 39$ pF. The mean rise times are shown on the plots and the standard deviation is $\sim$ 0.2 ns.

The linearity for the two gains and capacitive loadings is shown in figures 4.42 and 4.43. With $C_p = 39$ pF the low gain mode is linear to 400 MIPs and the high gain curve to 60 MIPs. This is demonstrated more clearly by figures 4.44 and 4.45 which show the gain per MIP as a function of signal size in MIPs.

Noise has been measured for different values of input capacitance on each channel. The ENC with respect to C_{in} of each channel is plotted in figure 4.46. The ENC measurements are bunched together showing no abnormal deviation from the expected result measured in the previous DELTA test chip. The mean values for intercept and slope give the mean ENC for the chip of ENC = 676 e+ 28 e/pF.

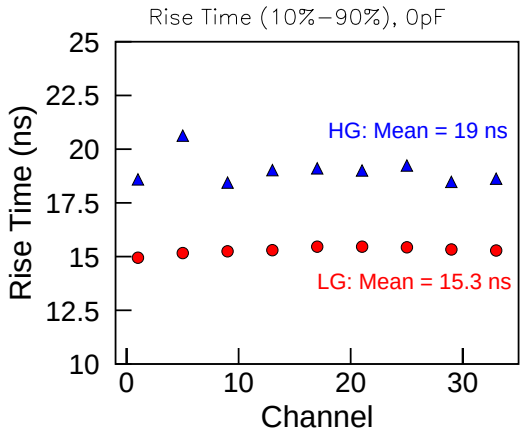

Figure 4.40: Measured rise time (10% to 90% of peak voltage) against channel number for $C_p = 0$ pF.

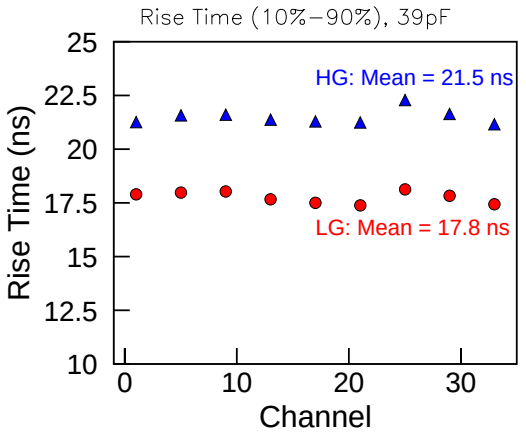

Figure 4.41: Measured rise time (10% to 90% of peak voltage) against channel number for $C_p = 39$ pF.

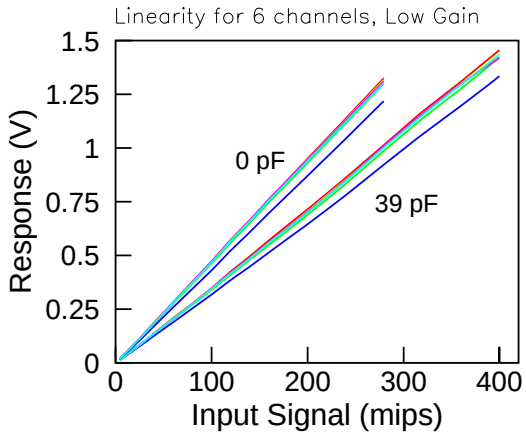

Figure 4.42: The measured linearity for 6 channels in low gain.

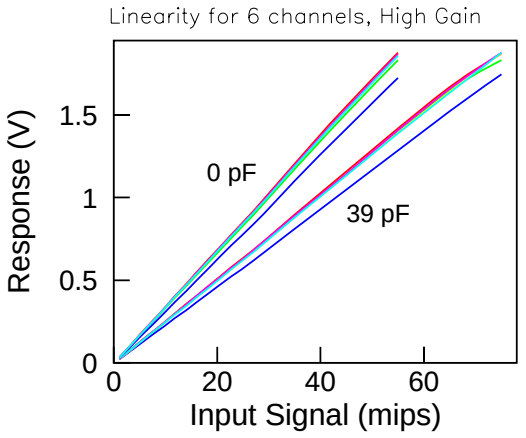

Figure 4.43: The measured linearity for 6 channels in high gain.

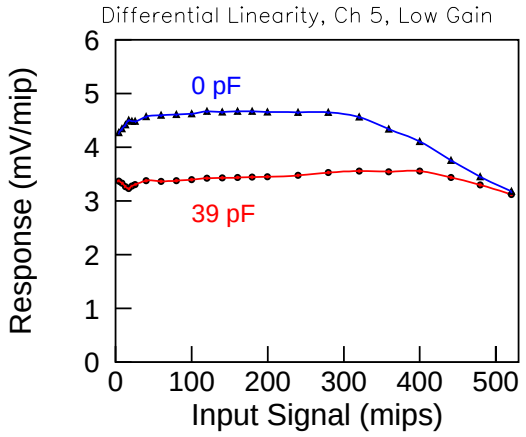

Figure 4.44: The gain per MIP in low gain as a function of the input signal in MIPs.

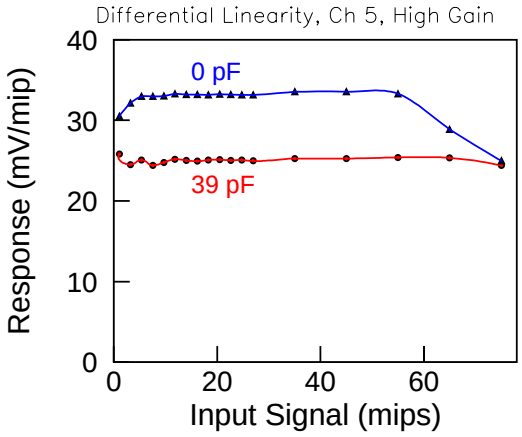

Figure 4.45: The gain per MIP in high gain as a function of the input signal in MIPs.

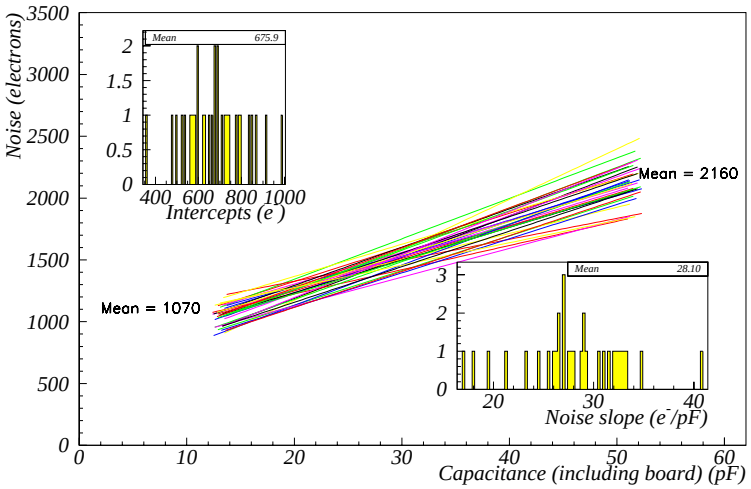

Figure 4.46: Measured noise as a function of the total input capacitance (C_{in}) for all 36 channels.

Figure 4.47 shows an oscilloscope image of the output from DeltaStream in "multiplexer mode". The pattern of the dc baselines is evident as is a 10 MIP signal injected onto channel 18. Looking closely at the signal channel, one can see that the output

amplifier has a fast response, overshooting slightly the required value. The signal settles within the first 25 ns of the 50 ns period available for multiplexing at 20 MHz, allowing the last 25 ns to be used for sampling by an ADC.

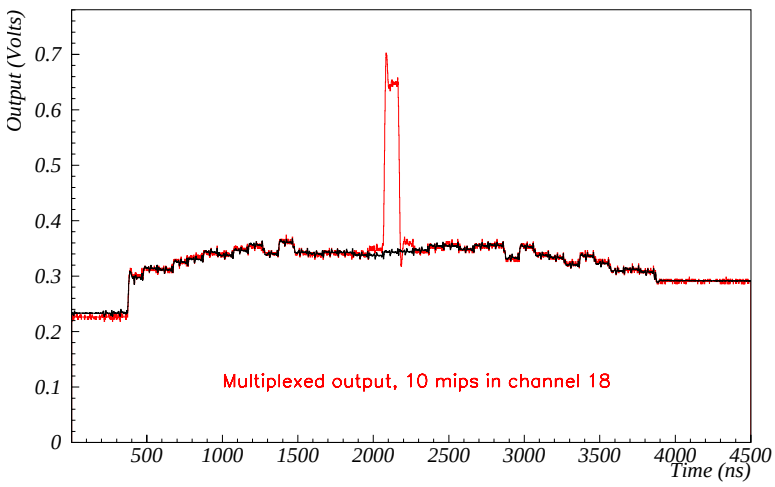

Figure 4.47: DeltaStream in multiplex mode. Signal seen on ch.18.

Measurements of linearity have been made in both single channel and multiplex mode. The results are identical showing that the dynamics of operating the multiplexer at 20 MHz do not degrade the dynamic range.

4.4.4 Conclusion from DeltaStream measurements.

DeltaStream provides a suitable readout chip for the test and measurement of silicon sensors produced for the Preshower. DeltaStream has also provided a test vehicle for the development of a 20 MHz large dynamic range multiplexer. In addition DeltaStream has provided very useful information relating to channel to channel parameter variations. Table 4.3 provides a summary of the channel to channel variations. The rms variation in low and high gain is $\sim 4\%$ for gain and $\sim 2\%$ for risetime. These are acceptable results and give no cause for concern.

Measurement type & additional Cap.	Low Gain			High Gain		
	pp	mean	σ	pp	mean	σ
Baseline (0 pF)	91 mV		21 mV	69 mV		18 mV
Gain (0 pF)		4.62 mV	159 μV		33.12 mV	1.16 mV
Gain (39 pF)		3.44 mV	112 μV		24.57 mV	925 μV
Risetime (0 pF)		14.5 ns	0.21 ns		18.9 ns	0.27 ns
Risetime (39 pF)		17.5 ns	0.23 ns		21.8 ns	0.38 ns
Noise	ENC=676e + 28e/pF					

Table 4.3: Summary of channel to channel variations of baseline, gain and rise times. Results of all 36 channels are included.

There is some cause for concern about the baseline variation which has a structure that seems to be compatible with a power supply voltage drop along the power lines. Layout modifications could be used to flatten the observed hump in a future design at the expense of chip area. In reality, the sampling technique described in section 4.1 based on 3 samples will measure the baseline in the first sample and hence baseline variation will not degrade the charge reconstruction.

Summary

The first section of chapter 4 looked at charge reconstruction using a voltage sampling technique as opposed to a current integration technique as used in PACE1. Current integration was very attractive since each memory cell acted as a charge bucket being filled by a current pulse from FCICON, the sum of 3 buckets representing the total charge. This method was inherently robust against timing fluctuations either in phase or due to jitter. Unfortunately it also meant that the system was susceptible to digital charge pick-up from the substrate increasing the overall noise of the system.

A study of voltage sampling [4] showed that taking 3 samples from a classic CR-RC^2 pulse shape could also be made robust against timing fluctuations providing two separate techniques were used to resolve time and charge.

A deconvolution technique (described in [3]) can be used taking three samples (inter-spaced by 25 ns) to resolve the timing resolution. It can also be used to resolve the charge but significant errors arise if variations on signal shape and timing properties are included. The Preshower plans to use deconvolution to resolve the bunch crossing number only. In addition, another set of weights can be found using a χ^2 fit minimisation such that Q represents the deposited charge.

In the study the electronics noise was exaggerated to 1/4 MIP. The accuracy of Q was determined with a phase variation of ± 2 ns and with a jitter on an individual sample of ± 0.5 ns. In all cases Q was resolved to within 1% of the charge deposited. This compares to 10% if the deconvolution method is used in isolation to resolve Q.

The overall Preshower electronic specifications of table 1.6 state that two dynamic ranges are required (1 - 400 MIPs during data taking and 0.1 - 50 MIPs during calibration). This allows the development of a two gain system ie. high gain (HG) for calibration and low gain (LG) for normal operation.

Three different versions of a dual gain systems were designed and fabricated in a DMILL test chip. These included: a "dual gain" circuit with two simultaneous outputs per channel (LG and HG), a charge pre-amplifier followed by a switched gain shaper and a transimpedance pre-amplifier followed by a switched gain shaper. The positive and negative points of each circuit type are discussed in the section 4.2. All circuit variations satisfied the specifications of the table 1.6. The circuit that was eventually chosen for the Preshower was the charge pre-amplifier followed by a switched gain shaper called DELTA, the design of which is described in section 4.3.

The measured results of DELTA showed a signal response for both gains with a peaking time of ~ 25 ns and a constant rise time with respect to signal size across the dynamic range. The required dynamic ranges are met i.e. 50 MIPs for HG and 400 MIPs for LG. The channel gain is approximately 30 mV/MIP in HG and 4 mV/MIP in LG. Pile up conditions have been tested using an input pulse corresponding to 20 MIPs at a rate of 5 MHz with no adverse effects on performance. Pythia simulations show the maximum expected pile-up condition in the CMS Preshower to be 2 MIPs at 2 MHz average. The gain measured as a function of increasing sensor leakage current

showed the gain constant for I_{leak} <150 μA, well beyond the Preshower specification of I_{leak} <20 μA.

Expressions for noise are developed in the text and reveal important implications for the design of the input bipolar transistor. The series noise is shown to be proportional to the base resistance which itself is inversely proportional to emitter area. The parallel noise is inversely proportional to the β but the β is degraded after irradiation the magnitude of which is inversely proportional to emitter area. Hence large emitter area is desired for low noise before irradiation but an optimum emitter area will exist for optimum noise performance after irradiation. The prototype chip contained channels with varying sizes of emitter area to test this theory. Also included on the test chip was individual bipolar transistors of different emitter areas to allow a study of the β degradation with respect to irradiation.

The noise performance (measured in HG) before irradiation showed an average ENC of 640 e + 33 e/pF with the predicted increase in series noise for the circuits with input transistors having lower emitter areas.

Two chips were then exposed to 10 Mrads(Si) of ionising radiation and another two chips exposed to a neutron fluence of 4×10^{13} n cm^{-2}. The effect on signal response after irradiation was seen only in the gain. The gain increased by 17% after ionising radiation and decreased by 14% after neutron radiation. The gain decrease is due to β degradation and should affect the result for both types of irradiation. The apparent increase in gain after ionising radiation was found to be due to an increase in DELTA feedback resistance R_f . A test structure on the chip enabled precise measurement of this resistor and showed an increase in resistance of 50% after ionising radiation but no change after neutron irradiation. This type of resistor (RHV) in DMILL technology is therefore not a reliable radiation tolerant component and should not be used.

The noise results after irradiation showed little difference to that measured before irradiation however the bipolar test structures showed severe β degradation (> 50%) for large emitter area devices. An optimum emitter area was evident in order to achieve reliable radiation tolerant behaviour and low noise performance.

Section 4.4 gave the design details and measured results of a 36 channel chip called DeltaStream designed to aid the production testing of the silicon sensors. Each DeltaStream channel contains the DELTA pre-amplifier and switched gain shaper plus a track & hold circuit. The outputs of each channel are then serialised by a 36:1 20 MHz multiplexer designed to maintain the dynamic range.

The text describes the design of the track & hold circuit plus 20 MHz multiplexer in order to maintain the dynamic range. Complementary switches are used to pass the signal with an almost flat on resistance (R_{on}) with respect to signal voltage.

Measurements from DeltaStream showed similar analog performance to that measured on the previous test chip. Of interest in DeltaStream was the channel to channel variations of dc values, gain and noise and the influence of the multiplexer on the dynamic range. The results showed a hump in the dc levels across the 36 channels of DeltaStream. The peak to peak baseline variation is 91 mV in LG and 69 mV in HG. The most likely explanation for this hump is a progressive voltage drop on the power

lines which run vertically from channel to channel. Since the layout feeds power to both the top and the bottom, the region with the largest power supply voltage drop will be the centre. Channel to channel variation of gain has been calculated as the standard deviation (σ) around the mean which is $\sim$100 μV (LG) and $\sim$1 mV (HG). The exact values can be found in the text.

The noise performance in HG was measured for each channel, the mean values for intercept and slope give the mean ENC for the chip of ENC = 676 e + 28 e/pF. The linearity was measured both with the multiplexer working in a static mode and running at 20 MHz with no observable difference between the two.

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Chapter 5

PACE2

PACE2 was designed during 2000 in DMILL technology. It was intended to be a complete PACE prototype (perhaps the final prototype before production) fulfilling all of the specifications listed in table 1.6.

The first point to notice about PACE2 is that it is not a single ASIC but two. It was decided to divide PACE2 into 2 parts separating the front-end amplifiers from the analog memory. The chip containing the front-end amplifiers is called Delta and the second chip containing the analog memory is called PACE-AM. The combination of the two chips is PACE2 sometimes referred to as the PACE2 assembly (figure 5.1).

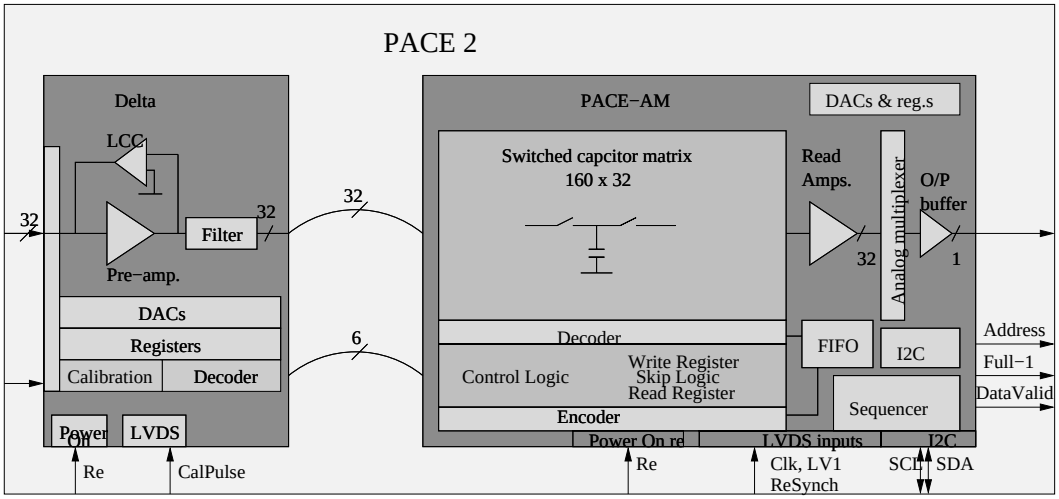


Figure 5.1: Block diagram of the PACE2 assembly.

The division of PACE2 into 2 chips was made for 3 reasons:

- **Reduce charge coupling through the substrate.** Results from PACE1 (chapter 3) showed significant charge coupling through the substrate from active

logic regions of the chip into the analog signal path. Chapter 4 explained that this was the main reason to move to a voltage sampling system and initiate the design of the Delta front-end which produced low impedance signals into the switched capacitor matrix. Breaking the design into 2 physical parts and locating all the sensitive pre-amplifiers in one chip and the 40 MHz active logic in the other will block a parasitic path through the substrate between the two. Other layout techniques have also been applied such as separate power supplies for digital and analog circuits as well as guard rings around each major sub-block of the design.

- **Improve yield.** Modern mainstream electronics technologies have huge production capacities with a continuous flow of wafers passing through the fabrication process. This enables a very stable process and yields are generally high. DMILL, on the other hand, is a specialised process with a very small market consisting of HEP and space applications. The fabrication process is not continuous and relatively large fluctuations of process parameters have been observed. Due to this the DMILL yield is significantly less than mainstream processes. Care has to be taken therefore in the design of DMILL chips to limit the overall size since yield is inversely proportional to chip area. The area of Delta is $\sim$20 mm^2 and the area of PACE-AM is $\sim$60 mm^2. DMILL projected yields fall sharply after 60 mm^2 hence the benefit of two separate chips.

- **Improve testability.** Testability improves with two separate chips enabling direct access to the output of each pre-amplifier stage. This can be a added benefit during wafer testing in the production phase.

This chapter outlines the main design issues relating to PACE2. The chapter starts with an overview of the Preshower electronic system to define how PACE2 should interact with the other system components. Design issues relating to analog blocks such as a large dynamic range analog memory, analog readout of the memory and a calibration circuit are discussed. This is followed by a description of the digital functionality of the chip and its modes of operation.

5.1 The Preshower Electronic System

A block diagram of the Preshower electronics system is shown in figure 5.2.

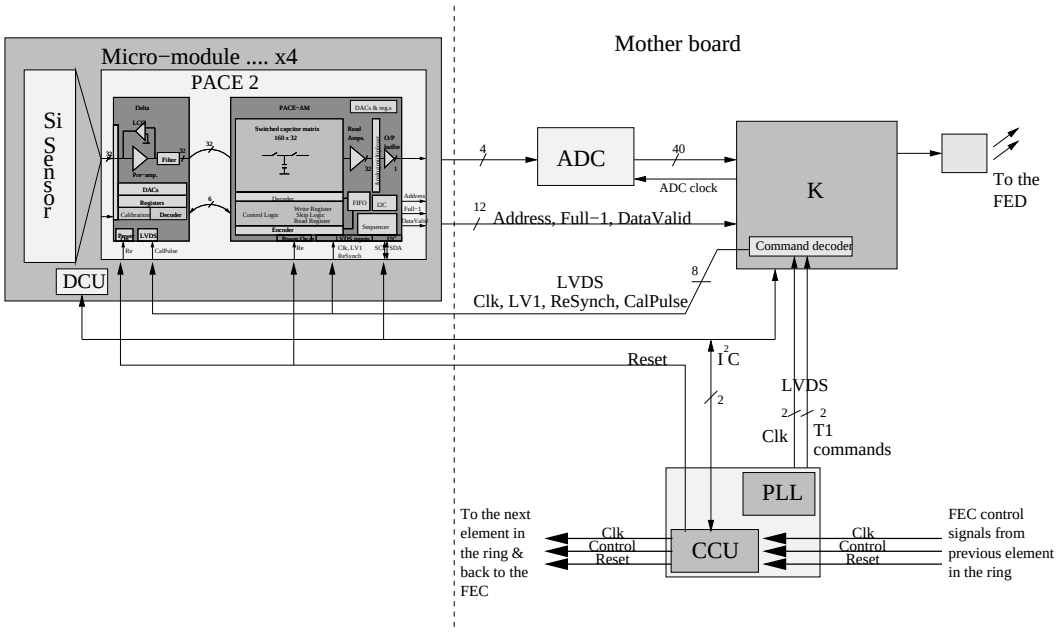


Figure 5.2: Block diagram at system level of the Preshower electronic system

The data path starts at the silicon sensor. Each micro-module contains one silicon sensor and one PACE2 assembly. The analog output of PACE-AM is connected to an ADC located on the mother board. There is one ADC per micro-module. A data concentrator chip (labelled "K" in figure 5.2) receives the digitised data from 4 ADCs. The "K" chip formats the data into packets containing additional timing information about the event and delivers a digital data stream to an optical driver also located on the mother board. From here the data exits the central CMS detector via optical links to data processing electronics (FED) in the counting room.

The control circuitry is located on the mother board in the form of two digital ASICs called the communication control unit (CCU) and a phase locked loop (PLL). Control signals arrive from the Front End Controller (FEC) located in the counting room via fibre optic cables. Electrical low voltage differential signals (LVDS) are then used to distribute these signals to the CCU chips on the mother boards. The distribution mechanism is a ring with one CCU passing the control signals to the next. Up to 8 CCU chips exist in one ring. Redundancy in the connections from one CCU to the next is built in to avoid the problem of one CCU failure affecting the entire ring. All signals at this level are synchronous with a 40 MHz clock. The system modularity depends on which part of the Preshower is considered since there are 4 mother board designs. Each mother board contains 1 CCU+PLL, between 7 and 10 micro-modules with equivalent number of ADCs and 2 to 3 K chips with associated optical links.

The control signals are divided into two groups depending on their timing requirements.

Fast time critical signals include the first level trigger (LV1), synchronisation pulse (ReSynch), calibration pulse (CalPulse) and bunch crossing identification (BC0). These signals are encoded into a 40 MHz clock by missing any one of three consecutive clock levels and are called the T1 commands. The CCU passes the encoded clock to the PLL which separates the clock from the T1 commands. The encoded T1 commands are shown in table 5.1. More than one LV1 within three consecutive clock cycles is forbidden in CMS to allow for this encoding.

T1 commands	
First level trigger (LV1)	100
Test pulse for calibration (CalPulse)	110
Synchronous reset (ReSynch)	101
Bunch crossing zero (BC0)	111

Table 5.1: Table of T1 encoded commands

The encoded T1 commands and a phase adjusted 40 MHz clock are sent from the PLL to the K chips in LVDS format. A command decoder inside the K chip separates the encoded signals into individual LVDS lines for each command which are then sent to the Delta and PACE-AM chips on the micro-modules.

The LVDS format used for the T1 commands is an industrial standard defined by the IEEE for high speed data transmission [1]. Differential data transmission ensures common mode rejection of noise picked up on the data lines since the receiver must respond to differences between the data lines. The voltage level is defined as a 400 mV swing around a common mode voltage (V_{CM}) of 1.2 V. The receivers are designed to be sensitive to a 400 mV swing around a a common mode voltage that can vary between 0.2 V and 2.2 V. These levels are shown in figure 5.3.

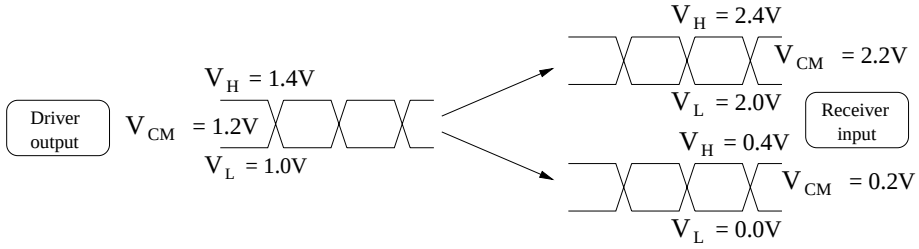


Figure 5.3: Low Voltage Differential Signal (LVDS) voltage levels.

LVDS is particularly suitable for use in low noise mixed analog-digital designs where analog performance could be degraded by coupling from fast digital signals on

capacitive nodes such as the pads. There are 3 LVDS receivers in PACE-AM and 1 in Delta for the Clk, LV1, ReSynch and CalPulse signals respectively.

Slow control signals provide system programmable features and can also monitor the system status.

A communication protocol called I^2C [2] has been adopted by the CMS tracker and Preshower. The CCU communicates with all the other ASIC chips shown in figure 5.2 via the I^2C connection. It is capable to down-load dedicated parameter settings into internal registers of an individual chip. It can also read back status information from these registers. Delta and PACE-AM make extensive use of the I^2C protocol for programmable settings of bias values and changing between various operational modes.

The I^2C protocol uses two signal lines labelled SCL (serial clock) and SDA (serial data). There is a single I^2C address per PACE2 assembly which is located on the PACE-AM chip. An internal bus system allows PACE-AM to access registers located within Delta. This is because the I^2C data lines need to be sampled by a high frequency clock (40 MHz) which is undesirable to have on the same chip as the pre-amplifiers. The type of I^2C implemented in PACE2 is able to work at "Normal Speed" (100 kHz) and "Fast Speed" (400 kHz).

5.2 PACE2 Analog Signal Path and Analog Design Issues

The signal path through PACE2 is shown in figure 5.4 via a block diagram of a single channel.

The input is directly connected to the silicon sensor strip. The pre-amplifier and shaper are identical to the Delta switched gain design explained in chapter 4 and used in the DeltaStream chip. The number of NPND10 bipolar devices used for T1 in figure 4.4 is n=3 in accordance with the conclusions of chapter 4. The Delta design will provide 30 mV/MIP in HG and 4 mV/MIP in LG with dynamic ranges 0.1-50 MIPs and 1-400 MIPs respectively. The active signal range at the output of the shaper is 1.6 V for the signal range plus 200 mV undershoot. A further 200 mV (for dc variations) has been added to define a specification of 2 V active signal range for the elements that follow the shaper. A calibration circuit is included on the Delta chip to enable calibration of individual channels from internally generated test pulses.

The output of each shaper drives directly the analog memory cells in the switch capacitor matrix through a bond connecting the two chips. The switched capacitor matrix is 160 cells deep providing a buffering capability of 4 μs. Triggered columns are then read and multiplexed into an analog data stream.

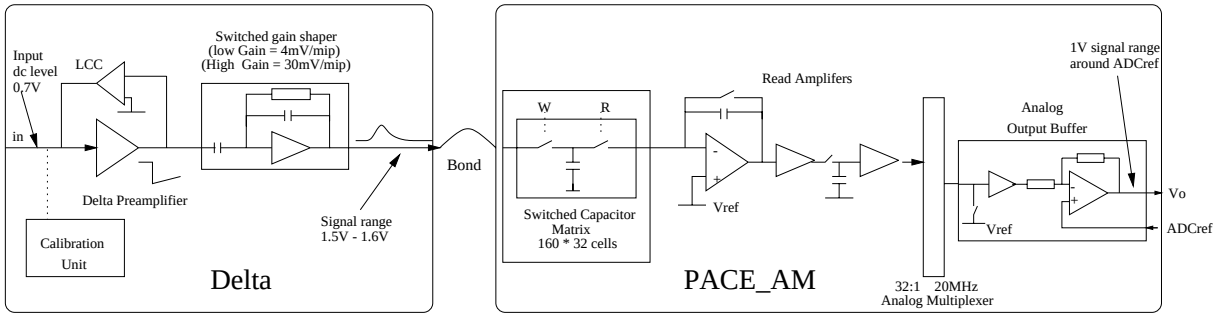


Figure 5.4: Block diagram of the analog signal path through one channel in PACE2.

The design of the pre-amplifier, shaper and multiplexer have been covered in chapter 4. This section focuses on the design of the remaining important analog functions. In particular the principles behind writing to and reading from an analog memory cell with large dynamic range and internal electronic calibration.

5.2.1 Writing to an analog memory cell

In voltage sampling the analog memory cell performs the function of a track & hold circuit. Each successive memory cell tracks a different 25 ns period of the shaped output signal from Delta retaining the instantaneous voltage at the end of the period.

A signal that passes through an analog memory cell will be subject to errors on the sampled value. Some errors will result in distortion of the signal and some will result in the introduction of noise. The choice of the components to use in the memory cell

and its layout is of vital importance to electrical properties of the memory as is the quality of the fabrication process.

Consider the most basic track & hold circuit possible and ignore (for the moment) the need for large dynamic range. The cell would consist of 1 MOS transistor used as a switch and 1 capacitor (C_{mem}) for the storage element as in figure 5.5.

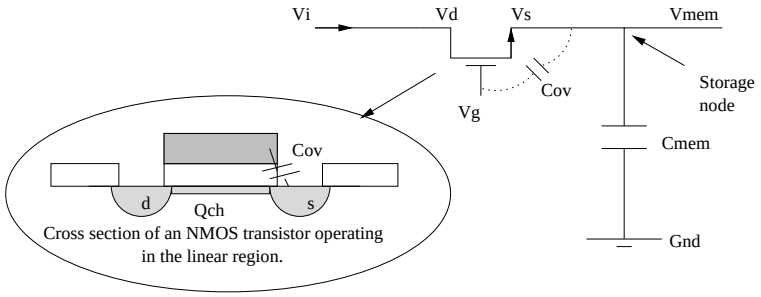


Figure 5.5: A simple storage cell

The first effect to consider is charge injected from the MOS device onto the storage node at the moment the device switches off. The charge injected is the combination of two charge mechanisms and will result in error of the stored voltage.

When a MOS device is "on" ($V_{gs} > V_t$) and $V_{ds} < V_{dsat}$ (where $V_{dsat} = V_{gs} - V_t$) as in the case of a switch when $V_d \approx V_s$, the device is said to be operating in the linear region. The channel is almost flat and the channel charge is given by equation 5.1. As the gate voltage falls mobile carriers in the channel exit through both the source and the drain. If this is a rapid fall then equal amounts of the channel charge flow into both source and drain nodes [3, 4]. The induced error in the sampled voltage due to channel charge injection (V_{ch}) is given by equation 5.2. V_{ch} is proportional to the signal value (V_i) and hence a non linear component is introduced.

$$Q_{ch} = WLC_{ox}(V_{gs} - V_t) = WLC_{ox}(V_g - V_i - V_t) \tag{5.1}$$

$$V_{ch} = \frac{Q_{ch}}{2C_{mem}} \tag{5.2}$$

As the gate voltage falls below $V_i + V_t$ the channel ceases to exist. Further charge is injected into the storage node through a capacitive coupling to the gate via the gate overlap capacitance (C_{ov}). C_{ov} is a linear function of the gate width multiplied by a capacitance parameter given by the foundry in F/m. The amount of charge injected onto the storage node is dependent on the rate of change of V_g (ΔV_g). Assuming a rapid falling edge (worst case condition) the maximum voltage change that can be induced through the injected charge is given by equation 5.3 [5]. The injected charge will be negative for an NMOS switch and positive for a PMOS denoted by a falling or rising edge for ΔV_g.

$$V_{ov} = \frac{\Delta V_g C_{ov}}{C_{ov} + C_{mem}} \tag{5.3}$$

Equation 5.3 assumes a worst case scenario using the full rail to rail voltage swing on the gate which makes the result independent of the signal. In reality it is likely that a portion of the charge injected onto the storage node while the channel still exists is absorbed by the channel resulting in a reduced but signal dependent effect.

The resulting error on the stored value will be the sum of equations 5.2 and 5.3. Both effects can be kept to a minimum by keeping the W and L values as small as possible and the capacitance value (C_{mem}) as large as possible.

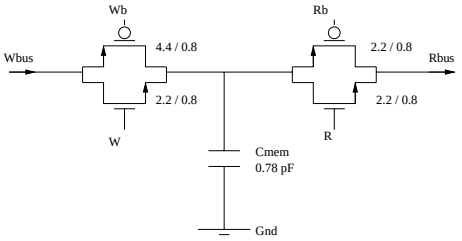


Figure 5.6: The schematic diagram of a single analog memory cell.

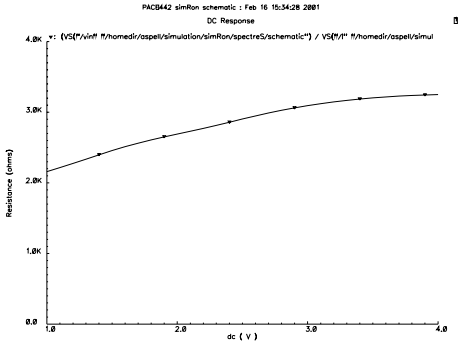


Figure 5.7: The combined "on" resistance "R_{on}" as a function of signal voltage.

A single transistor as a switch however, will not achieve the desired dynamic range. Section 4.4.2 discussed the necessity of using both NMOS and PMOS devices for the sampling switch in order to have a near uniform resistance "R_{on}" over a wide voltage range. The memory cell must therefore include 2 NMOS and 2PMOS devices plus a capacitor. Figure 5.6 shows the schematic diagram of the memory cell as designed for PACE-AM. The minimum size (from a layout point of view) for an NMOS device is $\frac{W}{L} = \frac{2.2}{0.8}$ μm, the PMOS is a factor 2 larger to take into account the difference in mobility. The combined R_{on} is shown in figure 5.7 varying between $\sim$2.2 kΩ and $\sim$3 kΩ over the signal range of 1 V to 3 V. Combining these devices plus two devices for the read operation into a cell area of 35 μm $\times$ 100 μm leaves enough room for a 0.78 pF storage capacitor. Figure 5.8 shows the corresponding layout.

The total effect of charge injection is given by equation 5.4 where V_{inj} represents the total voltage change due to the channel charge injection (V_{chn} and V_{chp}) plus the sum of the n and p overlap charge injection ($V_{ovn} + V_{ovp}$).

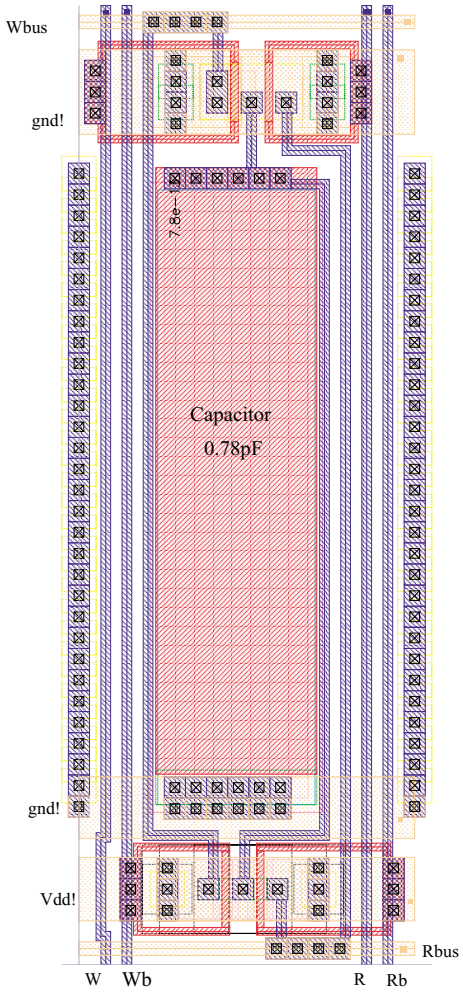


Figure 5.8: Layout of one analog memory cell. The vertical pitch is 100 μm and the horizontal pitch is 35 μm.

$$V_{inj} = V_{chn} + V_{chp} + V_{ovn} + V_{ovp} \tag{5.4}$$

Figure 5.9 plots the components of equation 5.4 against signal voltage V_i where $V_{ovnp} = V_{ovn} + V_{ovp}$. Over the signal range of interest the total voltage induced on the storage node through charge injection varies from ∼9 mV to ∼14 mV. It is also evident that the channel charge components dominate over the overlap components. If both n and p transistors had the same size then the overlap component would be zero and V_{inj} would be flat. This would not improve the linearity however since gradient of R_{on} against V_i would become steeper.

The principle of voltage sampling does not depend on the value of C_{mem} however, the error on the sampled voltage due to charge injection does. Fluctuations in capacitance value from cell to cell will therefore introduce a fluctuation in the offset

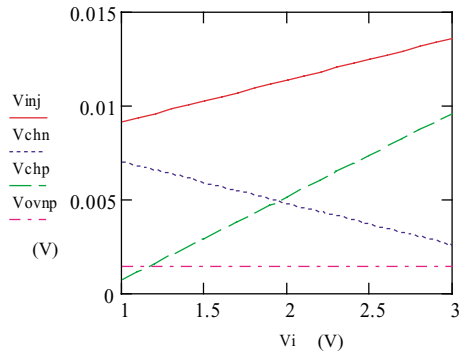


Figure 5.9: The change in voltage induced by charge injection as a function of signal voltage.

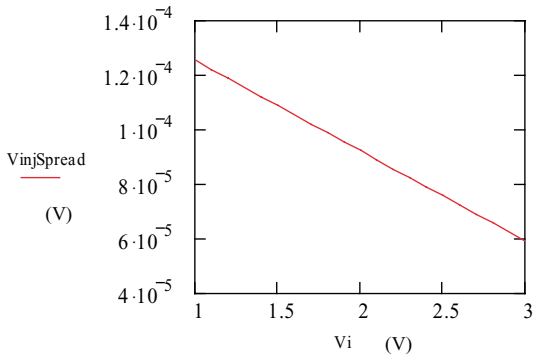


Figure 5.10: The uncertainty in the voltage induced by charge injection due to capacitor mismatch.

voltage introduced through charge injection. The matching of capacitors calculates to $\frac{\Delta C}{C} = 0.74$ %. Figure 5.10 plots the difference between V_{inj} for C_{mem} $\pm 0.74\%$. The maximum uncertainty on the measured value due to capacitor mismatch is therefore $\sim$120 μV.

The linearity of the analog memory is affected by both charge injection and a low pass filter effect. The charge injection could be made almost signal independent by using the same $\frac{W}{L}$ for both n and p transistors. Another technique for making the injected charge signal independent is to use switches on both sides of the capacitor [6]. Turning off the switch on the voltage reference side a few ns before the switch on the signal side ensures that the capacitor only retains the charge injected by the first switch which has a constant relationship between the voltage reference and $V_{gs} - V_t$ hence a constant level of injected charge. The penalty to pay for this type of design is reduced capacitor value since cell area is needed for the extra transistor and clock lines.

Obtaining a perfectly linear analog memory is not absolutely essential for the Preshower experiment since the signal response for each channel over the entire dynamic range will be periodically calibrated. More important is to limit as much as possible uncertain pedestal variations within one channel that contribute to the noise.

The design of the analog memory cell reflects this approach choosing a limited number of complementary switches and maximising the value of C_{mem}.

A low pass filter effect occurs in track mode due to the series resistance R_{on} and the storage capacitor. A simulation involving the Delta pre-amplifier and shaper followed by 160 memory cells was performed to study the sampling behaviour and the driving

capability of the front-end. Figure 5.11 shows the signal from the shaper and the voltages on 3 successive capacitors in separate analog memory cells of the analog memory. The first (Vmemcap-0) is sampled before the signal begins to rise. The second (Vmemcap-1) tracks the signal and then samples near the peak. The third (Vmemcap-2) samples 25 ns later on the tail.

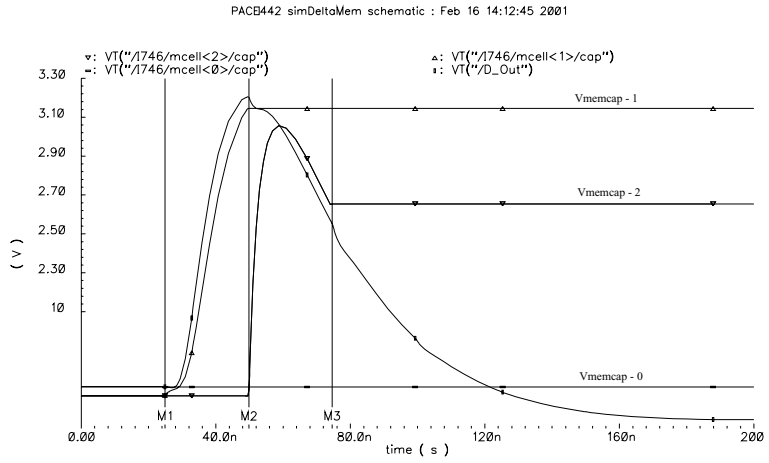


Figure 5.11: memsamples

The memory cell is sampling below a rising edge and above a falling edge with the magnitude of the offset dependent on the gradient of the signal. The effect is a compression of the signal. One can calculate the effective worst case signal loss with equation 5.5 and by considering the steepest part of the curve ie. $\omega = 2\pi f$ where $f =$ 20 MHz (half period = 25 ns).

$$V_{mem} = \frac{1}{(1 + \omega^2 R_{on}^2 C_{mem}^2)^{\frac{1}{2}}} \times V_i \tag{5.5}$$

$V_{mem} = 0.97 \times V_i$ for $R_{on} = 2.5$ kΩ and $C_{mem} = 0.78$ pF.

Reducing the signal loss would mean decreasing R_{on} (by increasing the $\frac{W}{L}$ of the transistor) or decreasing C_{mem}. Both options would increase the errors due to charge injection. It was hence decided to optimise for charge injection and accept a 3% signal loss.

5.2.2 Reading from an analog memory cell

Before a read operation begins the analog memory cells are isolated and the read amplifiers are in a unity gain condition with their outputs shorted to their inputs via a reset switch.

Box 1 of figure 5.12 shows the circuit configurations of a memory cell and read amplifier during this initial phase. There are two independent storage nodes labelled "a" and "b". Expressions for the charge stored on these two nodes (Q_a and Q_{b1}) are given in equations 5.6 and 5.7.

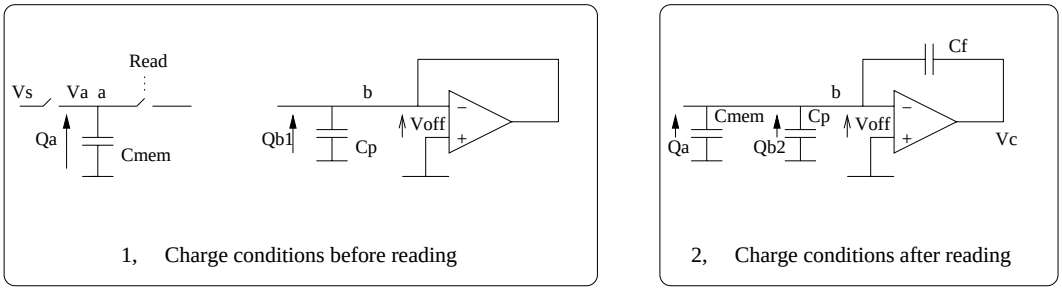


Figure 5.12: Principle of the read amplifiers

$$Q_a = V_a C_{mem} \tag{5.6}$$

$$Q_{b1} = V_{off} C_p \tag{5.7}$$

where :

- C_{mem} is the storage capacitance in the memory cell ($\sim$ 0.78 pF),
- V_a is the sampled signal voltage stored on C_{mem},
- V_{off} is the offset voltage of the read amplifier,
- C_p is the parasitic capacitance of node "b" to the substrate which includes the read bus and the parasitic capacitance associated with the bottom plate of the read amplifier feed back capacitor. C_p is large, in the order of a few pF.

Box 2 shows the circuit configuration after the reset switch has opened and the memory cell been connected to the read amplifier. Nodes a and b are now connected together. As a first approximation the total charge contained within box 2 is the same as in box 1 hence the charge at node b (Q_{b2}) is the sum of Q_a and Q_{b1} and given by equation 5.8. By inspection of the circuit in box 2 the charge Q_{b2} may also be written as equation 5.9.

$$Q_{b2} = Q_a + Q_{b1} = V_a C_{mem} + V_{off} C_p \tag{5.8}$$

$$Q_{b2} = (V_{off} - V_c) C_f + V_{off} C_p + V_{off} C_{mem} \tag{5.9}$$

where :

- V_c is the voltage at the read amplifier output

- C_f is read amplifier feedback capacitance

Equating expressions 5.8 and 5.9 enables an expression for the resulting voltage at node c as given by equation 5.10.

$$V_c = V_{off} - \frac{C_{mem}}{C_f}(V_a - V_{off}) \tag{5.10}$$

The important points to note are that V_c is not dependent on the parasitic capacitance C_p and that the gain is determined by the ratio $\frac{C_{mem}}{C_f}$. In this design $C_f = C_{mem}$ and hence the gain from node "a" to node "c" is 1.

In the above analysis charge injection from turning off the switches has not been considered. If V_c is sampled before disconnecting the memory cell then charge injection from the read switch will not play a role. However, charge injection from the read amplifier reset switch will contribute an additional term to equation 5.8. The reset switch is composed of both an NMOS and a PMOS transistor in parallel hence the additional term will be the sum of the charge injected by the NMOS and PMOS transistors ($Q_{injN} + Q_{injP}$). The resulting expression for V_c including the effect of the reset switch charge injection is given in equation 5.11.

$$V_c = V_{off} - \frac{C_{mem}(V_a - V_{off}) + Q_{injN} + Q_{injP}}{C_f} \tag{5.11}$$

$$Q_{inj} = \frac{WLC_{ox}(V_{gs} - V_t)}{2} - V_{dd}C_{ov} \tag{5.12}$$

The injected charge from a MOS device is composed of the channel charge plus charge injected via the overlap capacitance as explained in section 5.2.1 and is given by the general equation 5.12.

where :

- V_{gs} is the difference in voltage between gate and source.
- **W & L** are the gate width and length, $\frac{2.2}{0.8}$ and $\frac{4.4}{0.8}$ for the NMOS and PMOS devices respectively.
- V_t the device threshold voltage
- C_{ov} the overlap capacitance between gate and source.

Figure 5.13 shows the complete signal path from the analog memory cell through to the output.

Following on from the read amplifier is a P-type source follower (SF1) that buffers V_c onto node "d" which is a storage node for a track & hold circuit. Once V_c has settled, the track & hold circuit switches from track to hold mode storing the signal

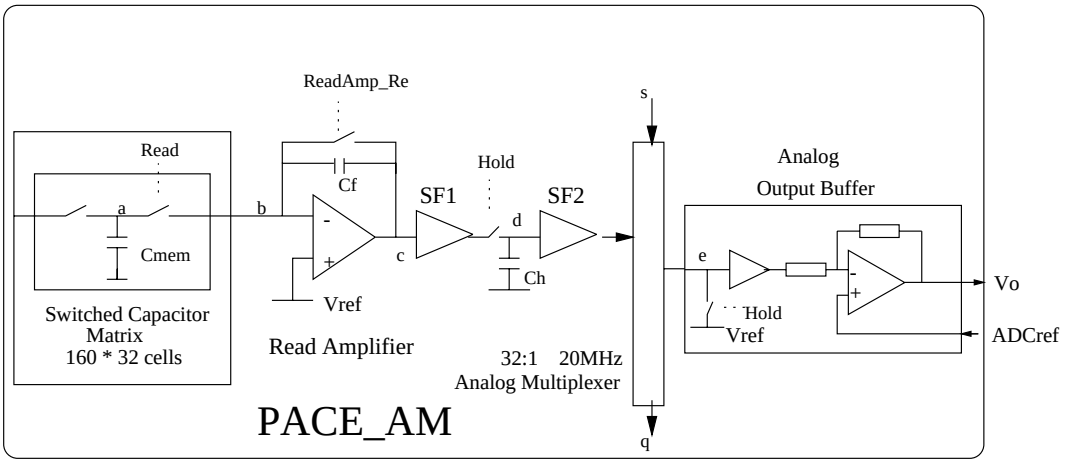


Figure 5.13: Schematic diagram of PACE-AM indicating the signal path for the Read operation.

on node "d". From this moment on the read amplifier can be disconnected from the analog memory cell and placed back into unity gain mode. The signal voltage on node "d" is buffered once more through an N-type source follower (SF2) to the multiplexer. The multiplexed signals from all the channels then pass through the output buffer to the ADC (Analog to Digital Converter). The output buffer has been specifically designed to drive the Analog Devices AD9042 12 bit ADC [7] which has a 1 V input range centred on a reference voltage (ADCref ∼2.4 V). ADCref is generated by the ADC and connected to PACE2. The output buffer inside PACE-AM divides the 2 V signal range by 2 and then centres the output on the analog reference provided by the ADC. The ADC (although not specified as radiation tolerant) has been extensively tested under irradiation [8]. The results show radiation tolerance up to 2 Mrad of ionising radiation and 2×10^{14} n cm^2.

A state machine within the sequencer generates the necessary control signals to apply to the switches in figure 5.13. The timing of these control signals are shown in figure 5.14. The initial condition has the ReadAmp-Re and Hold signals high. This ensures a stable dc condition both before and after the multiplexer. The read sequence begins by the ReadAmp-Re falling and the address of the required column of analog memory cells being popped from the FIFO and decoded. A Read signal is then applied to the column connecting the memory cells to the read amplifiers. The read amplifiers are given time to settle before the Hold signal falls to store the signal voltage on Ch. The time interval between these two pulses is 9.5 clock cycles allowing 237.5 ns for the read amplifiers to settle. The bias current for the read amplifiers can be adjusted to match this settling time optimising the power consumption. The Read signal then falls disconnecting the column of analog memory cells and the read amplifiers are reset by the ReadAmp-Re signal returning to a high state. From this point onwards the column of analog memory cells may be reused for storing charge delivered by Delta. The Unlock signal is generated to notify the control logic that the "Skip" flag associated with the column may be reset. The 20 MHz multiplexer clock

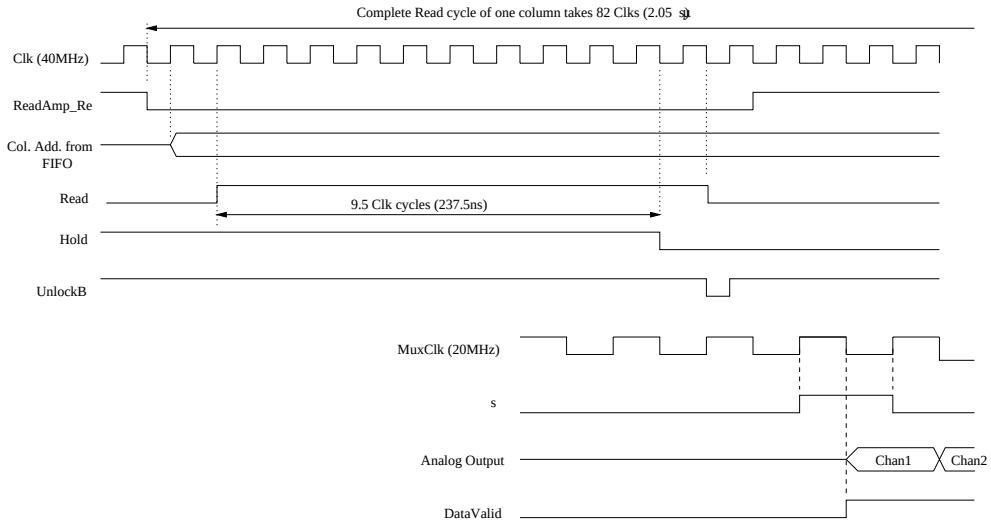


Figure 5.14: Timing diagram for the read sequence, waveforms are as applied to NMOS devices of the switches ie. 1 = "on" and 0 = "off".

(MuxClk) for the analog multiplexer runs continuously but the multiplexer is triggered by an input pulse "s". This is generated by the sequencer and the multiplexer switches between channels on each negative edge of the MuxClk. At the start of multiplexing a DataValid flag is generated and sent to an output pad. The analog output then changes from channel to channel as dictated by the multiplexer. After multiplexing the last channel the DataValid falls and the Hold signal rises reestablishing the initial dc conditions ready for repeating the cycle with another column of analog memory cells.

The time needed to complete a read cycle is 82 clock periods hence 2.05 μs, within the specification of 2.1 μs given in table 1.6.

5.2.3 PACE2 calibration

The signal response will vary slightly from channel to channel due to subtle differences in the charge delivered by the sensor or due to imperfect matching in the electronics. These differences will become progressively larger throughout the lifetime of the experiment due to radiation damage. Recall from chapter 2 that the radiation is not uniform across the endcap, detectors and electronics located at $\eta = 2.6$ will be exposed to higher levels of both ionising and neutron irradiation compared to those located at low η. Periodic calibration of each channel will therefore be performed using single MIP particles throughout the lifetime time of the experiment to take into account these effects.

In addition the signal response is not perfectly linear across the full dynamic range as explained in section 5.2.1. Each channel will therefore require calibration over the full signal range up to 400 MIPs. It is intended to perform this calibration with an internally generated test pulse. The test pulse will be a step voltage applied to one terminal of a capacitor with the other terminal connected to the input of a Delta

channel. If the rising edge of the voltage step is fast, the charge delivered to the channel will be given by Q=CV.

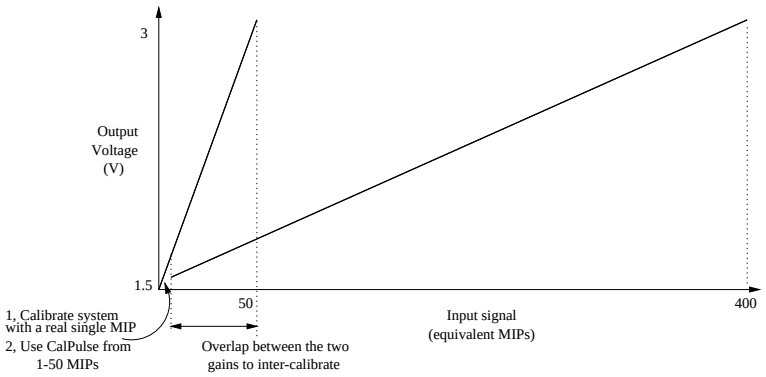


Figure 5.15: Inter-calibration of ranges.

The magnitude of the test pulse will first be calibrated against the signal response in HG from a real single MIP. From there a linear relationship will hold for the test pulse up to 50 MIPs. There is an overlap between the two ranges of approximately 49 MIPs. This region will be used to inter-calibrate the two ranges. Calibration in LG up to 400 MIPs may then be performed. The use of the two gain ranges for calibration is shown in figure 5.15.

An internal electronic calibration circuit has been developed for PACE2 and is located in the Delta chip. It contains programmable features such as individual channel selection and magnitude of the test pulse.

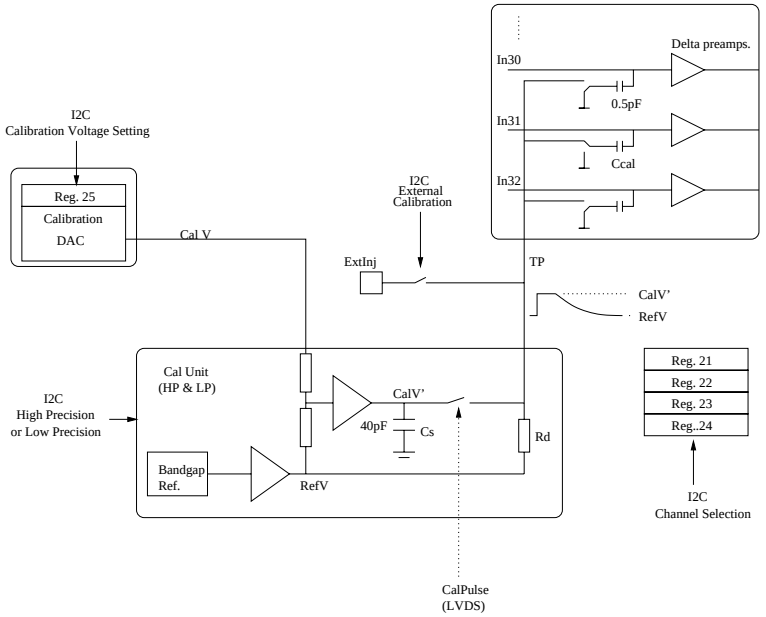


Figure 5.16: Block diagram of the calibration circuit.

Figure 5.16 shows a block diagram showing the main elements used in the calibration circuit. A 0.5 pF capacitor (C_{cal}) is connected to the input of each Delta channel. Under normal operating conditions the opposite terminal of the capacitor is connected to ground. To perform a calibration, a particular channel is connected through a complementary switch and C_{cal} to a common line (TP) to which a test pulse is applied.

The principle of the calibration circuit is as follows: A DAC (digital to analog converter) is used to define the amplitude of the test pulse. The voltage from the DAC (CalV) is scaled with respect to a band-gap reference voltage (RefV) and is buffered onto a large internal capacitor (C_s). An external digital signal (CalPulse) synchronous with the 40 MHz clock is applied to a switch connecting CalV' to TP. Tp is initially biased at RefV through resistance Rd. The voltage at TP rises quickly due to the capacitive imbalance between C_s and C_{cal} which is 80:1. After the initial rise, the voltage at TP is driven to CalV' by the buffer.

To calibrate accurately the signal response equivalent to 1 MIP it is important that the accuracy of the test pulse is better than the system noise ($< \frac{1}{10}$ MIP). A step voltage of 8 mV applied across the 0.5 pF capacitor will produce 4 fC of charge equivalent to 1 MIP. The minimum step voltage required is therefore 800 μV. The maximum step voltage required to produce a charge of 1600 fC (equivalent to 400 MIPs) is 3.2 V. This implies a DAC resolution of 12 bits to calibrate the entire range. A single circuit designed to this specification would be an over-design since high resolution is only needed at the 4 fC level.

The circuit used to generate the test pulse has therefore been divided into two 8 bit ranges for high precision (HP) at the 4 fC level and low precision (LP) for up to 400 MIPs.

- **High Precision (HP)** The linear range from the DAC is 3.6 V divided into 14 mV steps. This is applied to a 20:1 resistive divider to give 180 mV linear range with steps of 700 μV around the reference voltage RefV (1.288 V). The buffer is an opamp in a unity gain configuration with a low offset voltage ($\sim$10 mV) . The simulated range of CalV' is -32 mV to 136 mV with respect to RefV with a minimum step size (lsb) of 0.6 mV. The range is suitable for electrical calibration equivalent to -4 MIPs to 17 MIPs with an lsb of < 0.1 MIP.

- **Low Precision (LP)** In LP mode the full 3.6 V range of the DAC is used to charge C_s. RefV is reduced to $\sim$0.6 V by using an emitter follower instead of an opamp. The simulated linear range for CalV' in LP is -500 mV to 3.376 V with respect to RefV with an lsb of 19 mV. LP mode is hence suitable for electrical calibration equivalent to -60 MIPs to 422 MIPs with lsb $\sim$2.4 MIPs.

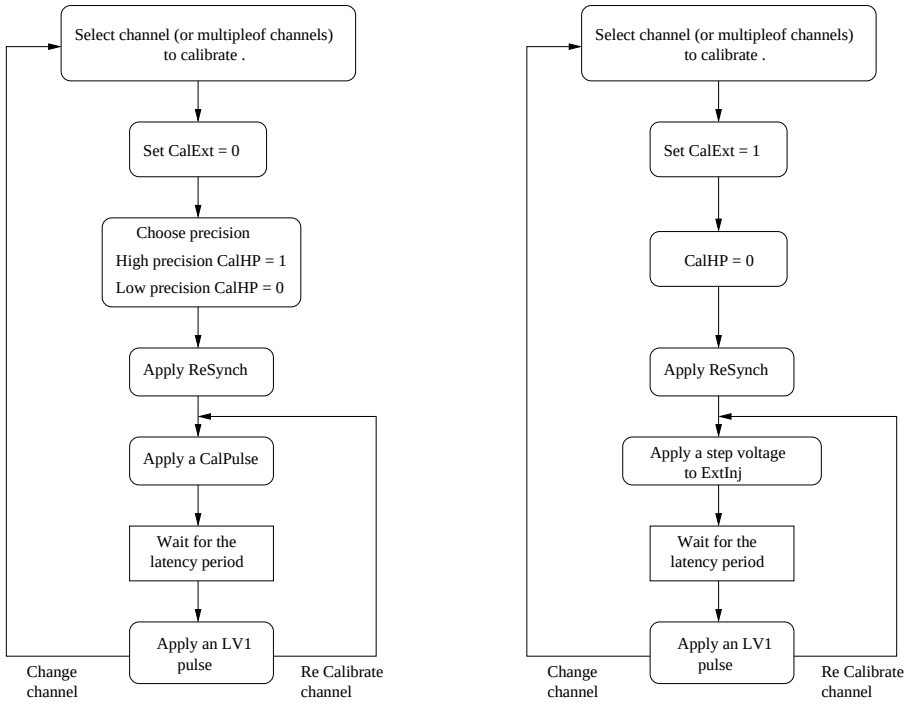
The $\frac{W}{L}$ dimensions for the NMOS and PMOS transistors used in the complementary switch are very important and are different for HP and LP. In HP, charge injection from the switch must be kept to a minimum. Both NMOS and PMOS transistors have the same dimensions to minimise the overlap charge injection. Simulation including all parasitic capacitances shows ($\frac{W}{L} = \frac{8\mu m}{0.8\mu m}$) optimal for calibration at the MIP level.

For LP, the step size is much larger making the effect of charge injection negligible. The $\frac{W}{L}$ values are large to reduce R_{on}. The chosen values are $\frac{W}{L} = \frac{20\mu m}{0.8\mu m}$ for the NMOS device and $\frac{W}{L} = \frac{40\mu m}{0.8\mu m}$ for the PMOS.

The resistor Rd allows the node TP to decay slowly back to RefV when disconnected from CalV'.

Also included on Delta is direct access to node TP such that an external calibration pulse may be injected. This method is intended for use during the lab testing and perhaps during production tests of the chip. It involves a separate mode (ExtCal) in order to connect TP to an input pad.

The procedure for both internal and external calibration is shown diagrammatically in figure 5.17.



a) Internal Calibration

b) External Calibration

Figure 5.17: Flowcharts showing the calibration procedure for both internal and external calibration.

5.3 Digital Control Functions & Modes of Operation

PACE2 is a mixed analog and digital design. The digital design is substantial and detailed descriptions of the design of the Control Logic, Sequencer and I^2C logic can be found in references [9, 10]. In this section the functionality of the digital control circuitry is described followed by PACE2 modes of operation.

5.3.1 Digital control functions

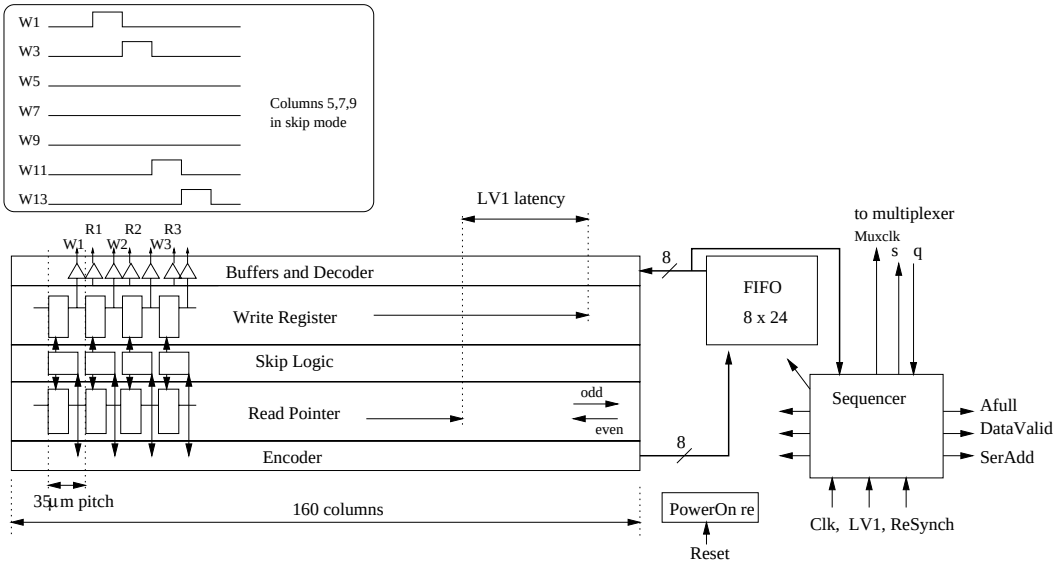


Figure 5.18: Block diagram of the Control Logic plus the FIFO, Sequencer and PowerOn reset circuits

Figure 5.18 shows a block diagram of the main elements involved in the control of the analog signal path. The Control Logic block provides the pointers to the switched capacitor matrix to determined which column of analog memory cells are written to and which column are read. It is subdivided into a write and read shift register, skip logic and an encoder and decoder. The Write Register is a shift register composed of 160 specially design D-flipflops that provide a shifting pulse from one column to the next for every clock cycle. This shifting pulse is buffered and sent to the corresponding column of analog memory cells to provide the Write signal marked "W" in figure 5.6. In this way the voltage of each channel is sampled and stored each 25 ns. The shift register is designed to shift a pulse from left to right along the odd numbered columns and from right to left along the even numbered columns. When the pulse arrives back at the beginning it continues indefinitely overwriting the previous data with new data. The Read Register is an identical design to the Write register however its function is different. It is started with a delay equal to the LV1 latency and maintains a constant delay with respect to the Write pointer as it shifts through the cells. At any one

moment the position of the Read pointer indicates the column containing stored data of the event signalled by an incoming trigger. A coincidence is made between the trigger and the pulse position in the Read Register to flag the column corresponding to the trigger. The flag is sent to encoder which creates an 8 bit address which is sent to the FIFO and stored. At the same time the column flag protects the column against further write pulses and puts the D-flipflops of the Write and Register into "Skip" mode for that column only. Skip mode means that the D flip-flop will pass the pulse arriving at its input directly to its output without shifting the pulse by one clock. The effectively length of the analog memory becomes one column less (159) and contains one column of protected data. The timing diagram in figure 5.6 shows a shifting write pulse skipping 3 triggered columns. The data in a triggered column is read by popping the column address from the FIFO, decoding the address in the decoder and applying a Read pulse to the appropriate column.

The timing of these signals is controlled within the Sequencer. The Sequencer is the central unit that coordinates the 40 MHz timing signals within PACE-AM. Immediately following a reset signal it starts the Write Register. It then waits for a preprogrammed number of clock cycles (the LV1 latency) before starting the Read register. On receiving an LV1 pulse the Sequencer generates 3 successive internal triggers to take 3 samples per LV1. It then controls the FIFO as the column addresses for the 3 samples are written. A separate state machine controls the read cycle generating the timing signals shown in figure 5.14 for the FIFO, read amplifiers and multiplexer.

5.3.2 Modes of operation

Figure 5.19 shows a flowchart of the operation cycle of PACE2.

On applying power to PACE2 a "PowerOn Reset" circuit generates a reset signal which puts PACE2 directly into "Sleep Mode". This means that both chips will be in a stable and minimum power consuming state. The only circuit that is responsive to external signals during Sleep Mode is the I^2C circuit. There is a PowerOn Reset circuit in both Delta and PACE-AM to take care of small time differences between the power being applied to each chip.

PACE2 contains a number of internal registers that are used to contain programmable settings. The settings are used to control bias currents and voltages delivered by internal DACs and to control various modes of operation.

The registers can be loaded with their normal "Run Mode" settings while PACE2 is in Sleep Mode. The values can then be read back through to I^2C interface to check the register contents before entering into "Run Mode"

The last bit to load through the I^2C should be the Sleep/Run bit which changes the mode of PACE2 from Sleep to Run. At this moment the contents of the registers are applied to the various internal circuits and PACE2 assumes its normal running conditions and power consumption.

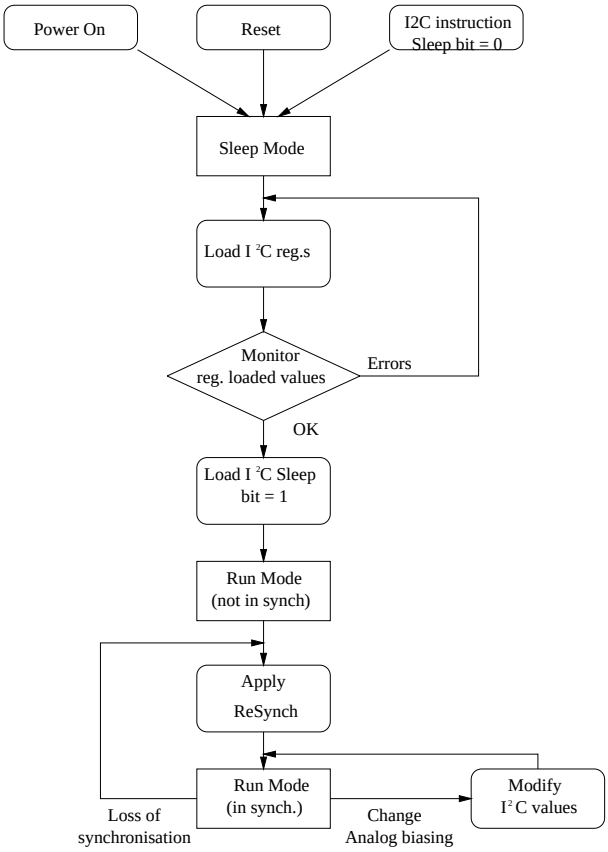


Figure 5.19: Flowchart of the operation cycle of PACE2

PACE2 is then in Run Mode which means that the inputs of Delta are sensitive and data is being written onto capacitors within PACE-AM . It is not synchronised however. This is because the instruction to enter Run Mode is delivered by the I^2C which is not a fast synchronised command.

To synchronise PACE2, a ReSynch pulse must be applied. The ReSynch pulse is delivered through an LVDS interface. After application of the ReSynch, PACE2 will be synchronised and will be in its normal Run Mode. From this moment on it is ready to receive LV1 commands and readout data.

In principle PACE2 should stay synchronised following the application of the ReSynch pulse. In reality it is possible for PACE2 to become "out of synch." due to single event upsets or spurious glitches somewhere in the system.

If PACE2 loses synchronisation then another ReSynch pulse should be applied. Application of the ReSynch signal means that any triggered data stored with PACE2 at that moment will be erased.

Bias settings may be adjusted while in Run Mode through I^2C commands. It is unlikely however, that we would want to do this while data taking. Hence any changes in register settings through the I^2C would normally be followed by a ReSynch pulse.

PACE2 may be put back into Sleep Mode by changing the Sleep/Run bit through the I^2C interface. Alternatively a separate pin labelled Reset provides a hardwired approach to reset the chips. Application of the Reset signal will put PACE2 directly into Sleep Mode.

Details of internal register addresses and DAC settings are contained within [11].

5.4 Completed PACE2 Design

Figure 5.20 shows the pin diagram for the two chips. The relative positioning of the pins is compatible with the layouts. Many of the pins are used for production test purposes only. For example; a special "test mode" allows access to each DAC voltage and the internal digital control signals from the sequencer and Control Logic. Also a "Scan mode" configures all the flipflops of the Sequencer and I^{2}C logic into a scan chain. Details of these special modes are contained within [11].

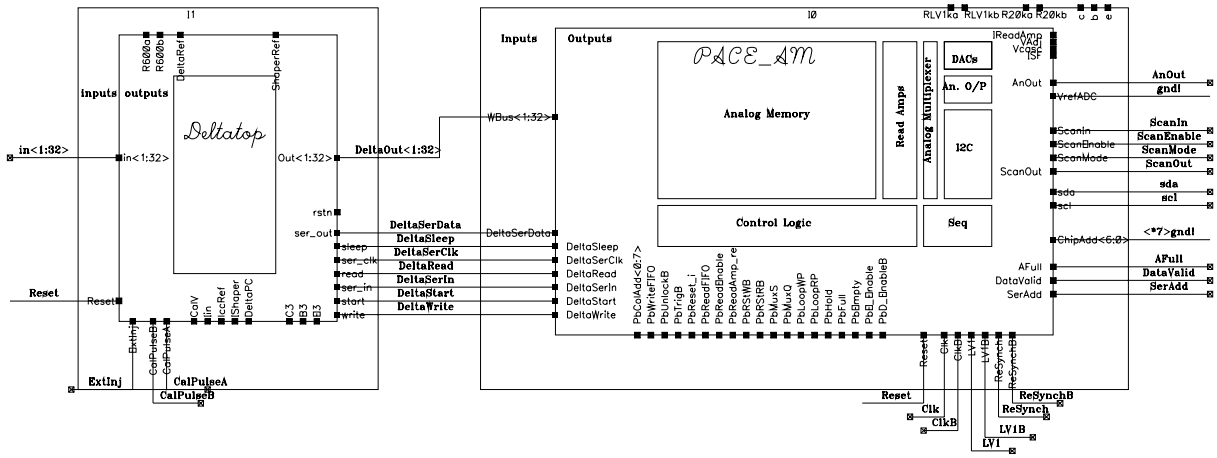


Figure 5.20: Pin names for PACE2

The layouts of the two chips are shown in figure 5.21 for Delta and figure 5.22 for PACE-AM.

Delta (figure 5.21) measures 3.5 mm × 6 mm occupying 21 mm^2 of silicon. The 32 channels are located in the top half of the chip whilst the lower section contains the calibration unit, DACs and registers used for DAC settings. The channel to channel pitch is 100 μm. The input pads are spaced on a pitch of 135 μm and have a grounded NWell shield beneath them to protect against unwanted pickup from the substrate. The same pad structure is also used for the 32 channel outputs.

PACE-AM (figure 5.22) measures 9.6 mm × 6.3 mm occupying $\sim$ 60 mm^2 of silicon. PACE-AM is divided into 5 independent sections. Each section has its own power supply and is surrounded by a guard ring. The aim is to contain digital noise within digital sections and keep the analog sections as free from charge coupling through the substrate as possible.

The first section is the switched capacitor matrix located in the upper left quadrant. The input pads have the same structure as the output pads of Delta to allow direct bonding. The Control Logic section occupies the lower third of the chip and forms the second section. The Control Logic guard ring extends around the multiplexer and sequencer (located in the lower right corner). Top right is the Read Amplifier section including 4 DACs for biasing. Moving down is small section encompassing the readout amplifier followed by a much larger section containing the I^{2}C logic. The I^{2}C logic

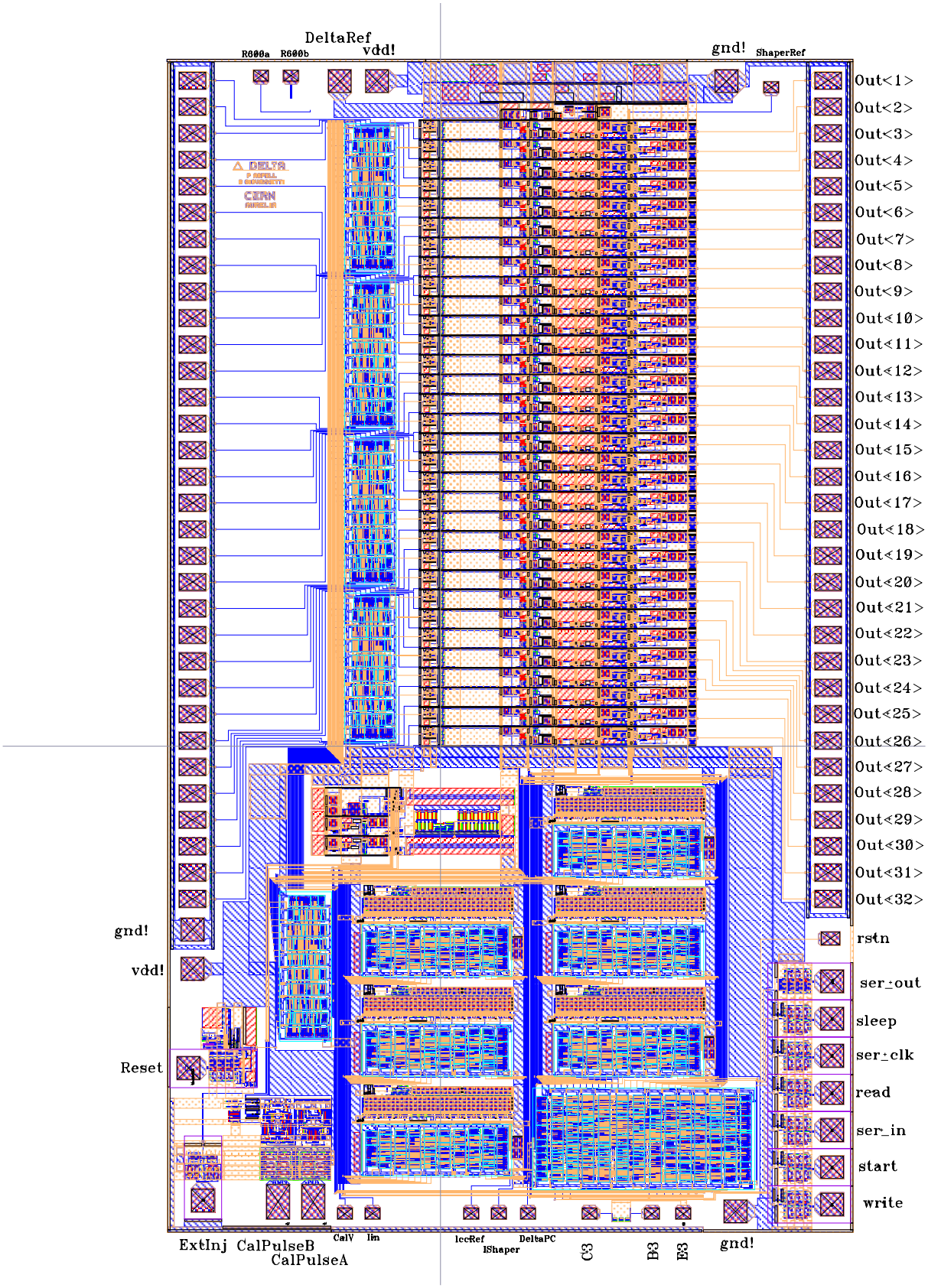


Figure 5.21: Delta layout

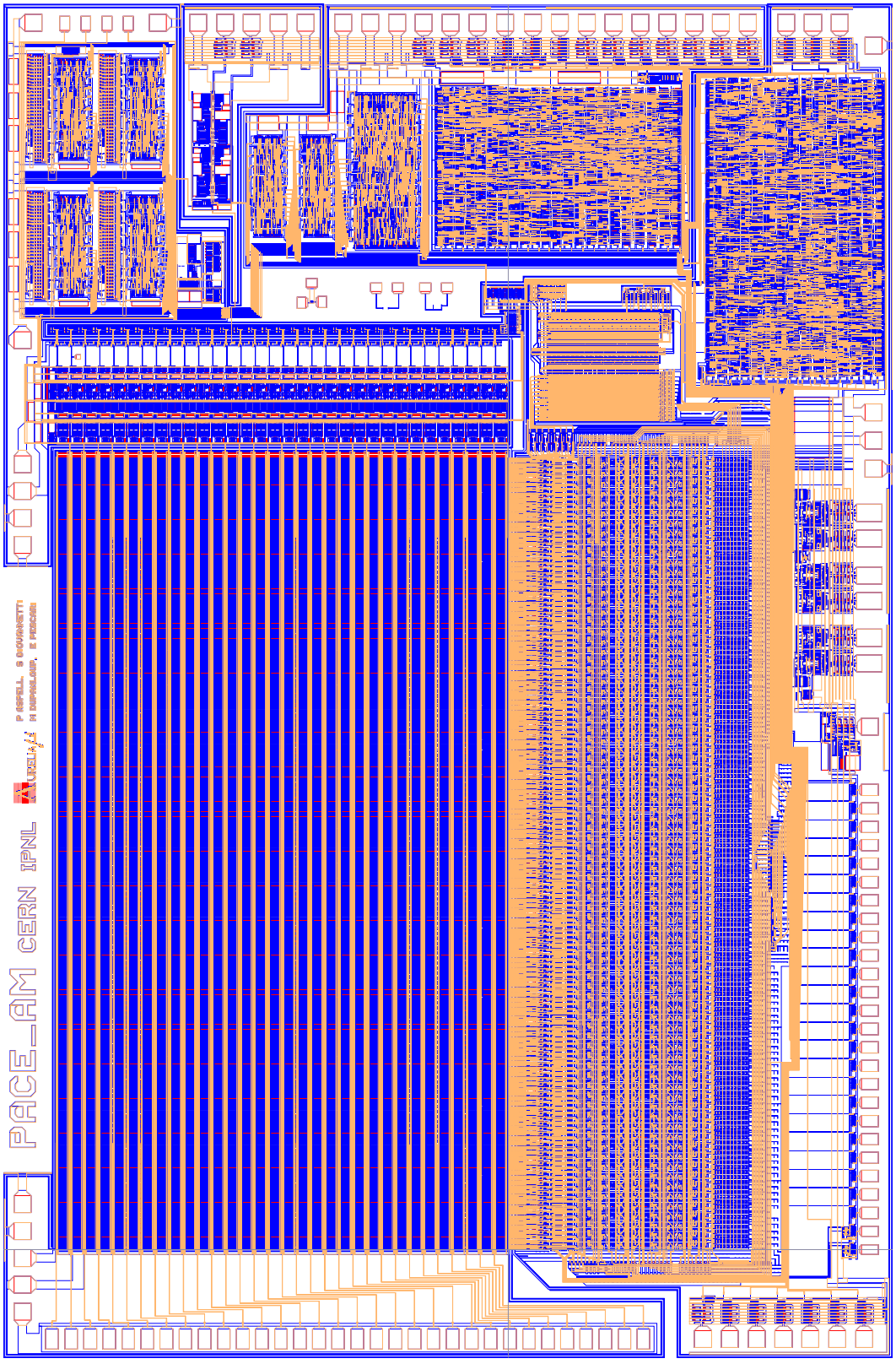


Figure 5.22: PACEAM layout

is quiet during normal operation, there is hence quite some separation between the active Control Logic and the readout amplifiers.

A photograph showing the two chips bonded together is shown in figure 5.23.

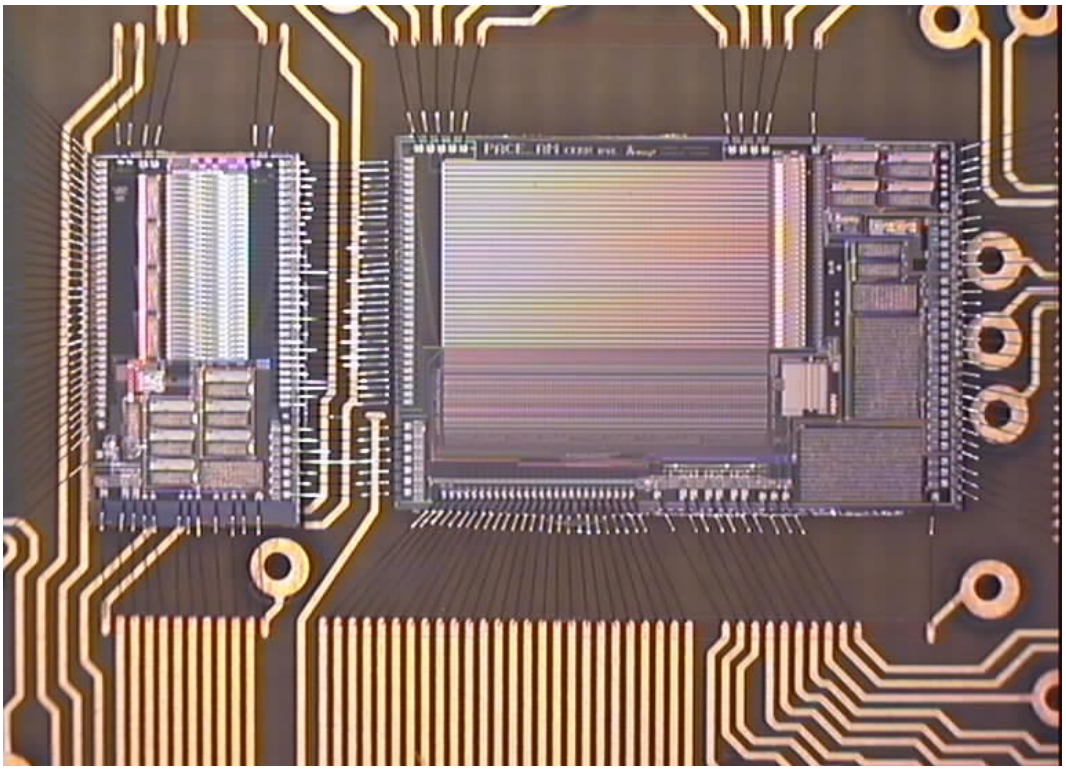


Figure 5.23: Photograph of the PACE2 assembly.

Summary

PACE2 represents the complete front-end electronics for the Preshower detector designed to meet all of the specifications of table 1.6. It combines the Delta development of chapter 4 with a voltage sampling analog memory. PACE2 is divided into two ASICs to separate the front-end amplifiers from the logic circuits that control the write and read functions. The chip containing the pre-amplifiers is called Delta and the chip containing the analog memory is called PACE-AM.

The analog properties of Delta have already been verified through the design of the Delta test chip and DeltaStream of chapter 4. This chapter has focused on the design of the analog signal processing elements of the PACE-AM chip. In particular the effects of charge injection onto a storage node of an analog memory cell capacitor when using complementary switches to maintain the large dynamic range. Whilst absolute charge injection is increased by the use of complementary switches the uncertainty of the charge injected is governed by the size of the storage capacitor. It is the uncertainty of injected charge that contributes to the noise of the system and hence the design of the analog memory cell minimises the number of complementary switches and maximises the memory cell capacitance. Also included is a description of the calibration circuit designed and incorporated within the Delta chip.

There are many digital circuits within PACE2 some for the control of the analog signal path and others for interfacing with the rest of the Preshower system. The function of these circuits and various possible operation modes are explained.

PACE2 is designed to meet all the requirements of table 1.6 and interface correctly with the rest of the Preshower system.

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Conclusions

The design and development of PACE (the front-end electronics for the CMS Preshower) has been presented.

The Preshower detector is designed as a sampling calorimeter with two planes of lead absorber interleaved with two silicon sensor planes one orthogonal to the other. There are ∼4300 silicon sensors each divided into 32 strips representing a single channel. Electrons or photons incident on the lead absorbers initiate electromagnetic cascades producing a shower of charged particles. The energy contained within the shower is proportional to the incident electron or photon and is measured by charge deposition in the silicon sensors. The granularity of the sensors allows two closely spaced photons to be resolved and hence separate background decays of a π^0 from a possible $H^0 \longrightarrow \gamma\gamma$.

The Preshower is not used in the first level trigger of CMS and hence needs to store all information gathered from the sensors until selected data is triggered for readout. PACE therefore has to perform the same general functions as that needed for a tracking system but at the same time perform as a calorimeter with the added complication of energy measurement over a wide range.

PACE has been designed through a series of prototype chips. The first (PACE1) realised PACE as an analog memory based on the technique of current integration. This lead to the design of a Preshower electro-mechanical prototype detector containing two planes of lead absorbers interleaved with silicon sensors and PACE1 chips. The prototype was used in electron beam tests to verify the physical design of the Preshower detector.

The technique of current integration had some inherent problems which degraded the noise performance of PACE1. A review of the sampling technique showed voltage sampling to be more attractive for use in PACE due to lower front-end noise and less susceptibility to charge cross coupling from the digital logic to the analog signal. A charge pre-amplifier and switched gain shaper (Delta) was designed and realised in a radiation tolerate technology (DMILL). Delta is designed to measure charge from 4 fC to 1.6 pC in low gain and from 0.4 fC to 200 fC in high gain.

A 36 channel Delta chip was designed for the measurement of Preshower silicon sensors during the sensor production. The chip was called DeltaStream and in addition to the Delta pre-amplifier and shaper it contained a track & hold circuit and a 20 MHz large dynamic range multiplexer. The chip can be used for multichannel charge readout of capacitive sensors with low noise and large dynamic range.

The Delta pre-amplifier and shaper was coupled together with a voltage sampling analog memory in the design of PACE2. PACE2 is capable of measuring charge from 4 fC to 1.6 pC (equivalent charge deposition from 1 to 400 MIPs) which corresponds to the range of charge deposition expected in a single Preshower silicon strip during LHC minimum bias events at high luminosity (L $\sim$ 10^{34} $cm^{-2}s^{-1}$). The high gain mode of Delta is intended for use during system calibration using real single MIPs. A programmable internal test pulse generator is used to inter calibrate the two ranges. PACE2 represents a complete PACE design incorporating all of the needs of the Preshower front-end electronics.

At the time of writing PACE2 has just returned from foundry. An intensive test program has started in order to verify if all the specifications are met. It is too soon to say if PACE2 in DMILL technology will be the final chip to go into the Preshower experiment. Of particular concern is the stability and yield of the DMILL process. A study is currently underway to investigate the possibility of porting the PACE2 design to a deep sub-micron technology to create PACE3. The advantages of doing so would enable greater memory depth, lower digital power consumption and possibly lower cost.

Appendix A

Noise

The accuracy to which one can measure particle energy deposited in a silicon sensor is ultimately limited by the noise of the measurement system.

This appendix covers the main concepts of noise. The first section (A.1) examines the different noise mechanisms that exist in electronic circuits. The second section (A.2) considers the noise models for active devices commonly used in electronic circuits. The calculation of noise in an electronic circuit is considered in the third section (A.3). Particular emphasis is given to the concept and calculation of Equivalent Noise Charge (ENC) which is the most common way to express the noise of particle detection circuitry.

A.1 Noise Sources

A.1.1 Shot noise

The original of shot noise can be explained when considering how direct current flows through a pn junction. The direct current in a forward biased pn junction is composed of majority carriers (from both sides of the junction) that gain enough energy to cross the potential barrier at the junction and then diffuse as minority carriers [1]. The energy of each individual carrier is random and hence the total current is the average of many small current pulses. On a small enough scale the fluctuation in the current can be seen as noise, shot noise.

Shot noise is proportional to direct current flow, if there is no current flow in a device then the shot noise component will be zero.

Shot noise can be modelled by a current source with a mean square value as in equation A.1 with units (A^2).

$$\overline{i^2} = 2qI_D\Delta f \tag{A.1}$$

where :

- q is the electron charge,
- Δf the bandwidth in hertz.

Dividing equation A.1 by Δf gives the noise current spectral density as in equation A.2 with units ($\frac{A^2}{Hz}$).

$$\frac{\overline{i^2}}{\Delta f} = 2qI_D \tag{A.2}$$

Equation A.2 shows that shot noise is flat with frequency response. The term "white noise" is used to group noise sources that are independent of frequency and hence shot noise is a type of white noise.

A.1.2 Thermal noise

Thermal noise is due to thermal excitation of charge carriers in a conductor with resistance (R). It is unaffected by the bias applied or the presence of current flow. In a resistor, thermal noise can be modelled by either a series voltage generator or by a parallel current generator (as shown in figure A.1). The mean square expressions for both generators are given in equations A.3 and A.4.

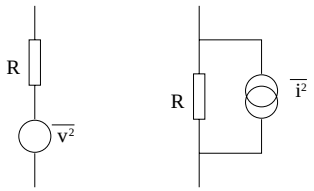

Figure A.1: Thermal noise represented as either a series voltage generator or a parallel current generator.

$$\overline{v^2} = 4kTR\Delta f \tag{A.3}$$

$$\overline{i^2} = 4kT\frac{1}{R}\Delta f \tag{A.4}$$

where:

- k is the Boltzmann constant,
- T is absolute temperature,
- R the resistance.

The resulting spectral densities, equations A.5 and A.6, also show thermal noise to be flat in the frequency spectrum and hence be white noise.

$$\frac{\overline{v^2}}{\Delta f} = 4kTR \tag{A.5}$$

$$\frac{\overline{i^2}}{\Delta f} = 4kT\frac{1}{R} \tag{A.6}$$

A.1.3 Flicker ($\frac{1}{f}$) noise

Flicker noise is also known (perhaps more commonly) as $\frac{1}{f}$ noise because the noise spectral density displays a $\frac{1}{f^\alpha}$ frequency dependence.

The origin of $\frac{1}{f}$ noise is believed to be the capture and release of carriers by traps in a semiconductor. These traps can be due to crystal defects or due to interface traps between the silicon and silicon dioxide. $\frac{1}{f}$ noise occurs in all active devices but is often more severe in MOS devices. This is thought to be due to the fact that the channel in a MOS device lies just below the Si/SiO_2 interface exposing the carriers to interface traps.

The noise current generator has a mean square expression as in equation A.7 and noise spectral density as in equation A.8

$$\overline{i^2} = KI^\gamma\frac{1}{f^\alpha}\Delta f \tag{A.7}$$

$$\frac{\overline{i^2}}{\Delta f} = KI^\gamma\frac{1}{f^\alpha} \tag{A.8}$$

where K is a device specific constant, I is direct current, α a constant close to 1 and γ a constant between 0.5 and 2.

A.2 Noise models for devices

A.2.1 Diode

A diode simply contains shot noise which can be represented by a parallel noise current generator as in equation A.9.

$$\frac{\overline{i_d^2}}{\Delta f} = 2qI_d \tag{A.9}$$

A.2.2 Bipolar

Figure A.2 shows the small signal model of a bipolar transistor together with its noise components.

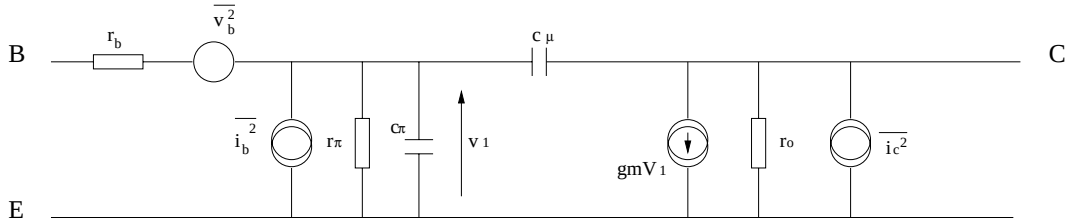

Figure A.2: Small signal model of a bipolar transistor complete with noise sources.

Considering first the base region; thermal noise will exist due to the base resistance r_b and is represented by $\overline{v_b^2}$ in equation A.10. The base current (I_b) is subject to both shot noise and $\frac{1}{f}$ noise which are combined into $\overline{i_b^2}$ as in equation A.11.

The collector current (I_c) also exhibits shot noise due to the passage of minority carriers through the base collector junction and is represented by $\overline{i_c^2}$ of equation A.12.

$$\overline{v_b^2} = 4kTr_b\Delta f \tag{A.10}$$

$$\overline{i_b^2} = 2qI_b\Delta f + K\frac{I_b^\gamma}{f}\Delta f \tag{A.11}$$

$$\overline{i_c^2} = 2qIc\Delta f \tag{A.12}$$

Referring these noise sources to the base of a noiseless device (as in figure A.3) gives the series and parallel equivalent noise sources A.13 and A.15 [4].

$$\frac{\overline{v_i^2}}{\Delta f} = 4kTR_{eq} \tag{A.13}$$

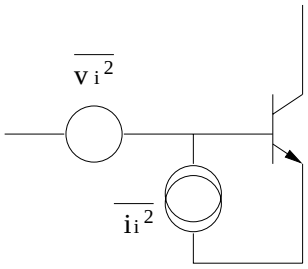

Figure A.3: Equivalent series and parallel noise sources of a bipolar transistor

where the equivalent noise resistance is given by equation A.14.

$$R_{eq} = r_b + \frac{1}{2g_m} \tag{A.14}$$

$$\begin{aligned} \frac{\overline{i_i^2}}{\Delta f} &= 2q(I_b + \frac{K' I_b^\gamma}{f} + \frac{I_c}{|\beta(f)|^2}) \\ &= 2qI_b \quad \text{if} \quad f_c < f < f_b \end{aligned} \tag{A.15}$$

where $K' = \frac{K}{2q}$.

The spectrum of equation A.15 shows a $\frac{1}{f}$ frequency dependence at very low frequencies defined by the second term, and a f^2 dependence at very high frequencies defined by the third term. In most cases the device will be working between these two extremes which has a flat response due to the first term. In such cases equation A.15 can be simplified as shown where f_c is the corner frequency [1] and $f_b = \frac{f_t}{\sqrt{\beta}}$ [2].

A.2.3 MOS

The channel of a MOS device is resistive and hence has a thermal noise component. This is the most dominant component of noise in a MOS device and is represented by a parallel noise source in figure A.4 (a) and expressed as $\overline{i_d^2}/\Delta f$ in equation A.16. The $\frac{1}{f}$ noise current spectral density of A.8 can be referred to the input by dividing by g_m^2 and expressed as a voltage noise source in series with the gate, $\overline{v_{gf}^2}/\Delta f$ in equation A.17. The area of the channel and C_{ox} both affect strongly the $\frac{1}{f}$ noise in a MOS device and hence the $\frac{1}{f}$ noise is frequently expressed as in the second form of A.17. Equation A.17 is correct for $\gamma = 2$; if $\gamma < 2$ then K must be expressed in units $A^{(\gamma-2)}$.

[1] The corner frequency is the intersection between the $\frac{1}{f}$ noise slope and the white noise in the noise spectrum.

[2] f_t is the transition frequency define by $f_t = \frac{1}{2\pi} \frac{g_m}{C\pi + C\mu}$

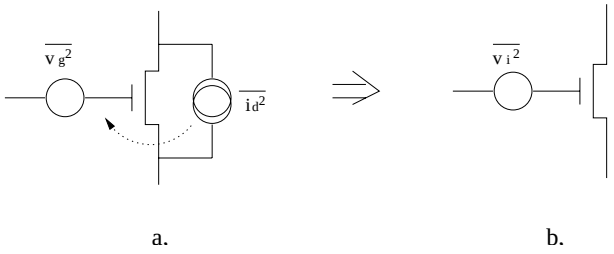

Figure A.4: MOS noise model and its equivalent series noise source.

$$\frac{\overline{i_d^2}}{\Delta f} = 4kT(\frac{2}{3}g_m) \tag{A.16}$$

$$\frac{\overline{v_{gf}^2}}{\Delta f} = \frac{KI_d^\gamma}{g_m^2 f} = \frac{K_f}{WLC_{ox}f} \tag{A.17}$$

where :

- g_m is the transconductance,
- K_f is a technology dependent constant with units V^2F,
- W and L represent the transistor channel width and length,
- C_{ox} the capacitance of the gate oxide.

The channel thermal noise ($\overline{i_d^2}$) can be referred to the gate by dividing by g_m^2 since $i_d = g_m v_g$ hence $\overline{v_g^2} = \frac{\overline{i_d^2}}{g_m^2}$ as in figure A.4 [2]. The equivalent input series voltage noise then becomes as in equation A.18 which is nicely separated into thermal and $\frac{1}{f}$ components.

$$\begin{aligned} \frac{\overline{v_g^2}}{\Delta f} &= 4kT(\frac{2}{3g_m}) + \frac{K_f}{WLC_{ox}f} \\ &= 4kTR_{eq} \quad \text{where} \quad R_{eq} = \frac{2}{3g_m} \quad \text{if} \quad f > f_c \end{aligned} \tag{A.18}$$

If the frequency of the operation of the circuit is higher than the corner frequency (f_c) , then the $\frac{1}{f}$ component is negligible and the equation can be simplified to just the thermal component.

Equation A.18 can then be expressed in terms of equivalent noise resistance as shown.

The equivalent input parallel noise source can also be calculated but it results in an expression which is proportional to the gate leakage current (I_g) which is so small the entire term can be neglected.

A.3 Calculation of Equivalent Noise Charge (ENC)

Expressing noise as an absolute value of voltage (such as mV rms similar to a measurement on an oscilloscope), on its own, is not very useful in understanding the noise performance of the system.

A better way is to express a signal to noise ratio (S/N) for the smallest signal that needs to be measured. In particle detection the charge delivered by a single MIP (4 fC) is often used to represent the smallest signal. Hence, if the gain of a system is 10 mV/MIP and the noise is 1 mV rms then the S/N = 10.

One could also say that the noise represents $1/10^{th}$ of a MIP (0.4 fC). In stating this last phrase the noise of the circuit has been expressed in terms of the minimum equivalent input signal that would be required to generate a response of the same magnitude as the noise. This is the definition of Equivalent Noise Charge (ENC).

In H.E.P. it is common to express ENC in terms of number of electrons. This is because a single MIP traversing a 300 μm silicon sensor delivers 25000 electrons making up a total charge of $\sim$ 4 fC. This hypothetical example would therefore have an ENC = 2500 e.

A calculation of ENC starts with an analysis of the pre-amplifier circuit. Each noise source associated with the components of the circuit can be referred back to the input. The input referred noise sources can then be combined to produce a single equivalent series voltage noise source ($\overline{v_n^2}/\Delta f$) and a equivalent parallel current noise source ($\overline{i_n^2}/\Delta f$) expressed in terms of their equivalent noise resistances. The expressions for $\overline{v_n^2}/\Delta f$ and $\overline{i_n^2}/\Delta f$ are given in equations A.19 and A.20 [4].

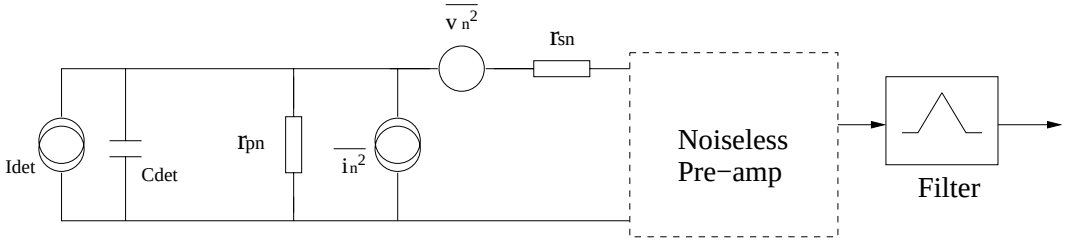

Figure A.5: General noise model

Figure A.5 is the noise model for a circuit which has had its individual internal noise sources referred to the input. The model contains the signal source, equivalent series voltage and parallel current noise sources, a noiseless pre-amplifier and a filter which represents the overall transfer function of the circuit.

$$\frac{\overline{v_n^2}}{\Delta f} = 4kTR_{sn} \qquad (\frac{V^2}{H_z}) \tag{A.19}$$

$$\frac{\overline{i_n^2}}{\Delta f} = \frac{4kT}{R_{pn}} \qquad (\frac{A^2}{H_z}) \tag{A.20}$$

The filter of figure A.5 represents any pulse shaping or analog signal processing that follows the amplification stage. With knowledge of the full transfer function the resulting noise after filtering could be calculated in the frequency domain. However, the approach adopted here simply requires a knowledge of the signal shape in the time domain.

If the filter represents a pulse shaping stage then the system is a "time invariant system" [3] Such a system is described completely by its impulse response [3].

The series ENC ($\overline{ENC_s^2}$) and parallel ENC ($\overline{ENC_p^2}$) can be worked out simply with a knowledge of peaking time (t_m) and the total input capacitance (C_i) as in equations A.21 and A.22.

$$\overline{ENC_s^2} = \frac{(\overline{v_n^2}/\Delta f)C_i^2}{t_m} \qquad (C^2) \tag{A.21}$$

$$\overline{ENC_p^2} = \frac{(\overline{i_n^2}/\Delta f)t_m}{3} \qquad (C^2) \tag{A.22}$$

This is derived from the application of a triangular weighting function explained in the note at the end of this section.

If the filter represents a switched capacitor circuit or involves multiple samples then the system is a "time variant system" [4] The filtering properties of a time variant system are described by its weighting function $w_{(t)}$[5] as expressed in equations A.23 and A.24 [4].

$$\overline{ENC_s^2} = \frac{1}{2}(\overline{v_n^2}/\Delta f)C_i^2 \int_{-\infty}^{\infty} [w'(t)]^2 + \frac{1}{\tau_{in}^2}[w(t)]^2 dt \tag{A.23}$$

$$\overline{ENC_p^2} = \frac{(\overline{i_n^2}/\Delta f)}{2} \int_{-\infty}^{\infty} w^2(t) dt \tag{A.24}$$

[3] A time invariant system is system in which "there are no variations with time in the system parameters during the measurement, and a single measurement of amplitude or time is performed" [3].

[4] A time variant system is system in which there are variations with time in the system parameters during the measurement such as capacitor switching and multiple sampling of the signal.[3].

[5] The weighting function describes the contribution that a noise impulse, occurring at time t, makes at the measurement time T_m. A weighting function $w_{(t)}$ for a time invariant system is the mirror image of the impulse response $h_{(t)}$ [3].

The second term of equation A.23 can be neglected if $\frac{t_m}{\tau_{in}} << 1$ where $\tau_{in} = C_{in}R_p$.

A good approximation of the integrals in equations A.23 and A.24 can be obtained from a knowledge of the impulse response signal shape. Figure A.6 and equations A.25 and A.26 show how to obtain values for the solutions of the integrals which are now referred to as constants I_1 and I_2..

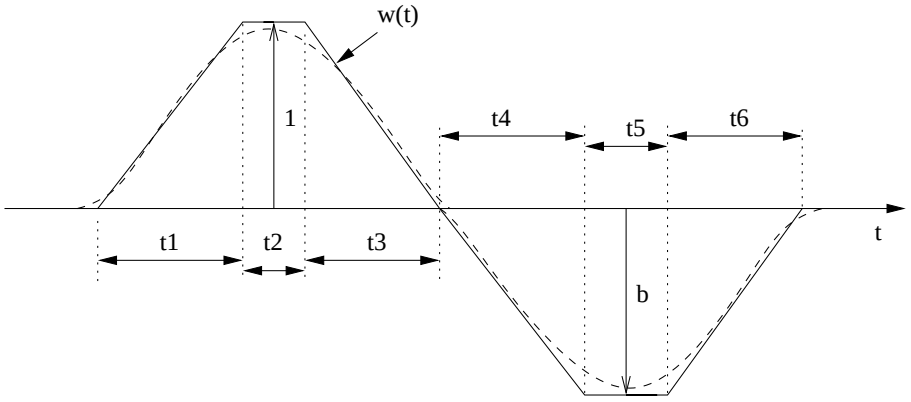

Figure A.6: Weighting function parameters used for a bipolar response of a time invariant filter.

$$I_1 = \int_{-\infty}^{\infty} [w'(t)]^2 dt \approx \frac{1}{t_1} + 0 + \frac{1}{t_3} + b^2\frac{1}{t_4} + b^2\frac{1}{t_6} \tag{A.25}$$

$$I_2 = \int_{-\infty}^{\infty} w^2(t) dt \approx \frac{t_1}{3} + t_2 + \frac{t_3}{3} + b^2\frac{t_4}{3}b^2 t_5 + b^2\frac{t_6}{3} \tag{A.26}$$

I_1 and I_2 may now be substituted in to equations A.23 and A.24 to obtain straight forward expressions for the ENC, equations A.27 and A.28.

$$\overline{ENC_s^2} = \frac{(\overline{v_n^2}/\Delta f)C_i^2 I_1}{2} \tag{A.27}$$

$$\overline{ENC_p^2} = \frac{(\overline{i_n^2}/\Delta f)I_2}{2} \tag{A.28}$$

Note: If one considers a unipolar impulse response (one without an undershoot) a triangular shaping function can be used. For such a function: $t_1 = t_3 = t_m$ and $t_2 = 0$. Hence t_m is the peaking time.

The weighting function approximations equate to $I_1 = \frac{2}{t_m}$ and $I_2 = \frac{2}{3}t_m$.

Substituting I_1 and I_2 into equations A.27 and A.28 give the equations A.21 and A.22 for a time invariant system.

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[4] V.Radeka *Signal, Noise and Resolution in Position Sensitive Detectors* (IEEE Trans. on Nucl. Sci. Vol 21, No. 1 pp 51 to 64, Feb 1974)

Glossary

- **ASIC** Application Specific Integrated Circuit
- **Bosons** Class of particles possessing integer spin such as $0, 1, ...$ Bosons do not obey the Pauli exclusion principle. Force carrying particles such as photons and gluons are bosons.
- **CERN** European Organisation for Nuclear Research
- **CP violation** The product CP is a mathematical concept of symmetries where C (charge conjugacy) represents particle - anti particle interchange) and P (parity) represents space inversion. The symmetries C and P hold independently for strong and electromagnetic interactions but not for weak interactions. In 1964 the product CP was found not to hold since CP violation was observed in the decay of neutral Kaons (K^0). The product of CPT where T represents time reversal is thought to always hold true for all interactions.
- **eV -(electron volts)** The kinetic energy acquired by an electron passing through a potential difference of 1V in a vacuum; 1 eV $\approx 1.602 \times 10^{-19}$ J, 1 TeV = 1000 GeV $= 1 \times 10^{12}$ eV.
- **Fermions** Class of particles possessing half integer spin (intrinsic angular momentum measured in terms of $\frac{h}{2\pi}$, where h is Planck's constant) such as $\frac{1}{2}, \frac{3}{2}.....$ This property means that fermions obey the Pauli exclusion principle and therefore cannot occupy the same quantum state. Quarks, leptons, electrons, protons and neutrons are examples of fermions.
- **Gray** The SI unit for absorbed dose is the Gray (Gy) where 1 Gy= 1 joule kg^{-1}. Most physics publications use Gray whilst most engineering publications use the older unit "rad". 1 Gy= 100 rad.
- **Hadron** A particle who's constituents interact via the "strong" force.
- **Jets (j)** A jet is a cluster of particles (mostly mesons and baryons) emerging from a collision at high momentum and moving in roughly the same direction.
- **Integral non-linearity (INL)** The maximum non-linearity (deviation over the specified range from a linear response) usually expressed as a percentage of the maximum pulse amplitude (signal range).
- **Kaon** A meson containing an s (strange) quark and an anti quark (up or down), or an anti s quark together with an up or down quark. The two types of Kaon are written K^0 and $\overline{K^0}$.
- **Lepton** A particle that does not interact via the strong force.
- **Linear energy transfer (LET)** The amount of energy deposited by an incident particle in a particular material (units eV mg^{-1} cm2).
- **Luminosity** A measure of the rate of interaction. At LHC the low luminosity period (L $\approx 10^{33}$ cm^{-2}s^{-1}) will provide on average 2 to 3 proton - proton interactions per bunch crossing (bunch crossings will occur every 25ns). At high luminosity this will increase to an average value of 20 interactions per bunch crossing.
- **Meson** A hadron made from an even number of quark constituents. The basic structure of mesons is one quark and one anti quark.

- **Minimum ionising particle (MIP)**. This is the term used to describe a single charged particle. It is often used to describe a unit of charge deposited in a sensor due to the passage of a charged particle. In a 300 μm thick silicon sensor, 1 MIP induces $\sim$ 25000 electrons which corresponds to $\sim$4 fC of charge.
- **Natural width** Natural width is the range of uncertainty of measured energy in GeV for a particle at a given energy. This is due to Heisenberg's uncertainty principle: $\Delta E \Delta t \approx h$ (more commonly written $\Delta x \Delta p_x \approx h$) where E is energy, t is time, h is Planck's constant, x is position and p momentum.
- **Neutron** A baryon with a basic structure of two "down" quarks and one "up" quark bound together by gluons (udd). A neutron has zero electric charge.
- **Pion (π)** The least massive meson. Pions can have electric charges $\pm$1 and 0.
- **Proton** A baryon (hadron composed of 3 quarks and gluons) with a basic structure of two "up" quarks and one "down" quark bound together by gluons (uud). A proton has electric charge +1.
- **Pseudorapidity (η)** is an angular variable defined by $\eta = -ln\ tan(\frac{\theta}{2})$ where θ is the angle between the particle being considered and the undeflected beam.

  Listed here is a table showing the relation between θ and η.

$\theta(^o)$	90	45	40.4	15.4	15	10	5.7	2.1
η	0	0.88	1	2	2.03	2.44	3	4

- **Radiation length (X_0)** The distance over which an electron looses $(1 - \frac{1}{e})$ of its energy as it passes through the material.

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In writing these acknowledgements, as I am doing now, I am wondering in my mind back through a long and rather unconventional route through my academic studies from childhood to the present. Each period as important as the next in providing the understanding for what should follow both professionally and, most importantly, for life in general. For me this is the essence of education and continues throughout life in many different areas of interest.

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RESUME en Français :

Les collisionneurs de particules utilisés dans les expériences modernes de physique des hautes énergies, sont entourés de très gros détecteurs comprenant un nombre important de capteurs qui mesurent la charge des particules les traversant. Le détecteur Preshower (détecteur de pied de gerbe) de l'expérience CMS est un calorimètre électromagnétique à échantillonnage qui produit des gerbes électromagnétiques quand il est traversé par des électrons ou des photons provenant des interactions proton-proton dans le LHC. Sa raison d'être est l'identification des photons issus de la désintégration des pions neutre, afin de les discerner des photons issus de la désintégration la plus probable du boson de Higgs, $H^0 \longrightarrow \gamma\gamma$. Ce détecteur comporte ∼4300 capteurs silicium de 32 canaux et couvre une surface totale de 16.4 m^2. Les circuits intégrés qui constituent l'électronique de lecture frontale (PACE), assurent la mesure de la charge de chaque canal individuellement avec une grande précision, un bruit faible, sur une grande gamme dynamique (4 fC à 1.6 pC), à la fréquence de 40 MHz et dans un environnement radiatif intense. Cette thèse présente la conception et la mise au point de ces ASICs. Le premier chapitre présente le détecteur Preshower et définit les spécifications dictées par la physique. Le deuxième chapitre a trait aux radiations, leurs effets sur les composants électroniques et les moyens de durcissement (méthodes de conception/choix des filières technologiques) pour résister à la radioactivité du LHC. Les chapitres 3 à 5 présentent la conception et les résultats de mesures de deux développements de PACE. Deux architectures de mémoire analogique sont notamment discutées, l'une basée sur une technique d'intégration de courant, l'autre sur une technique de tension échantillonnée. Des résultats expérimentaux obtenus sur un prototype électromécanique de Preshower, monté sur faisceau test, sont également présentés.

TITRE en anglais : The Design and Development of the Front-End Electronics for the CMS Preshower Detector.

RESUME en anglais :

Modern particle physics collider experiments consist of a number of macroscopic modules each consisting of large number of sensors measuring charge deposition from traversing particles. The CMS Preshower detector is designed as a sampling calorimeter producing electromagnetic showers for incident electrons and photons resulting from LHC p-p interactions. The ultimate aim is provide π^0/γ separation reducing the background to the most promising Higgs channel, $H^0 \longrightarrow \gamma\gamma$. The detector has ∼4300 silicon sensors each subdivided into 32 channels with a total sensitive area of 16.4 m^2. Front-end microelectronics ASICs must measure the charge of each channel accurately with low noise and over a wide dynamic range (4 fC to 1600 fC) at the rate of 40 MHz within a harsh radiation environment. This thesis presents the design and development of the Preshower front-end electronics ASIC development, PACE. The first chapter introduces the Preshower experiment and defines the specification for PACE as derived from the physics. The second chapter examines the radiation environment, its effect on electronic devices, and design techniques / technologies that can resist to LHC radiation levels. Chapters 3 to 5 present the design and results of two PACE developments examining analog memories based on current and voltage sampling techniques. Experimental results from a Preshower electro-mechanical prototype tested in a particle beam are also given.

DISCIPLINE : Microélectronique

MOTS-CLES : PACE, CMS, détecteur de pied de gerbe, grande gamme dynamique, Preshower, large dynamic range, front-end electronics.

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