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**Performance characterization of the NSW Micromegas detector, services
design and development of the Slow Control Adapter for the ATLAS
upgrade**

A dissertation presented by

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Performance characterization of the NSW Micromegas detector, services design and development of the Slow Control Adapter for the ATLAS upgrade

PhD Thesis

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35 Απαγορεύεται η αντιγραφή, αποθήκευση και διανομή της παρούσας εργασίας, εξ ολοκλήρου ή τμήματος αυτής, για εμπορικό σκοπό. Επιτρέπεται η ανατύπωση, αποθήκευση και διανομή για σκοπό μη κερδοσκοπικό, εκπαιδευτικής ή ερευνητικής φύσης, υπό την προϋπόθεση να αναφέρεται η πηγή προέλευσης και να διατηρείται το παρόν μήνυμα. Ερωτήματα που αφορούν τη χρήση της εργασίας για κερδοσκοπικό σκοπό πρέπει να απευθύνονται προς τον συγγραφέα.



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ΕΘΝΙΚΟ ΜΕΤΣΟΒΙΟ ΠΟΛΥΤΕΧΝΕΙΟ
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Αθήνα, Μάιος 2019



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Αθήνα, Μάιος 2019

Στην οικογένειά μου

Περίληψη στα ελληνικά

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Το πείραμα ATLAS είναι ένα από τα μεγαλύτερα πειράματα στον επιταχυντή LHC στο CERN. Είναι ένα πείραμα με γενικό σκοπό την ανίχνευση σωματιδίων που παράγονται από συγκρούσεις πρωτονίων στο κέντρο του. Η παρούσα διατριβή έγινε στα πλαίσια της αναβάθμισης του ανιχνευτή ATLAS και συγκεκριμένα του φασματομέτρου μιονίων, μέσω της αντικατάστασης του Small Wheel με το New Small

Wheel, της οποίας σκοπός είναι να μπορεί το πείραμα να ανταπεξέλθει στις νέες απαιτήσεις που θα επέλθουν με την επανέναρξη της λειτουργίας του LHC.

Στα κεφάλαια που ακολουθούν θα δοθεί σύντομη περιγραφή του ATLAS και του τρόπου λειτουργίας του. Ύστερα, επίκεντρο θα είναι η παρουσίαση της δουλειάς που έγινε στα πλαίσια της παρούσας διατριβής. Συγκεκριμένα:

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- το **κίνητρο για την αναβάθμιση** New Small Wheel και η δομή της.
- η **λειτουργία των ανιχνευτών Micromegas**, που περιλαμβάνονται στο New Small Wheel. Θα γίνει περιγραφή της αρχής λειτουργίας αλλά και της δοκιμής πολλαπλών πρωτοτύπων του ανιχνευτή, κατά τη διάρκεια της έρευνας και ανάπτυξης του ανιχνευτή ώστε να ανταπεξέλθει στις απαιτήσεις του αναβαθμισμένου HL-LHC.
- η δομή του συστήματος ελέγχου του ATLAS, και συγκεκριμένα η **ανάπτυξη λογισμικού για τον έλεγχο και παρακολούθηση** των συστημάτων του New Small Wheel. Σε αυτή την ενότητα έγινε μελέτη του ολοκληρωμένου κυκλώματος Slow Control Adapter το οποίο θα χρησιμοποιηθεί για τον αργό έλεγχο και την παρακολούθηση των ηλεκτρονικών στο πείραμα ATLAS. Επιπλέον έγινε ανάπτυξη λογισμικού για την προετοιμασία πακέτων και επικοινωνία με το κύκλωμα αυτό. Τέλος
- ο σχεδιασμός των υπηρεσιακών συστημάτων της αναβάθμισης New Small Wheel. Το σύστημα αυτό αναπτύχθηκε σε συνεργασία με πολυάριθμες ομάδες ειδικών για συστήματα αερίου, ψύξης, οπτικών ινών, υψηλής τάσης και άλλων. Θα γίνει περιγραφή όλων των συστημάτων και μελετών που έγιναν κατά τη διάρκεια της διατριβής αυτής.

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Abstract

The ATLAS experiment is one of the largest LHC experiments at CERN. It is a general purpose experiment that detects particles originating from proton collisions at its center. This thesis was carried out in the frame of an ATLAS upgrade, namely the New Small Wheel, which is meant to allow ATLAS to cope with higher requirements when the LHC starts up again.

95 In the following chapters, a brief description of ATLAS and its operation will be given. Then, the focus will be presenting the work for this thesis. Namely:

- the motivation for the New Small Wheel upgrade and its composition.
- the operation of Micromegas detectors, which are included in the New Small Wheel. This will include description of the principle of operation as well as the multiple tests of prototypes and production modules of this detector during the development phase in order to create a system to cope with the requirements of the HL-LHC upgrade.
- the outline of the control system of ATLAS, focusing on software development for this system. This module includes study of the Slow Control Adapter integrated circuit, which will be used for configuration and monitoring of the front-end electronics in ATLAS. Moreover, it includes software development for preparation of the corresponding packets and communication with the integrated circuit. Finally, there were tests and demonstrator cases for the operation of the software with the chip and electronics.
- the design of the services system of the New Small Wheel upgrade. This system was developed in cooperation with multiple expert teams on gas, cooling, fiber optics, high voltage and other sub-systems. Their design, requirements and limitations will be described.

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Chapter 1

The Large Hadron Collider and the ATLAS experiment

1.1 CERN

CERN, the European Organization for Nuclear Research, is an intergovernmental organization with over 20 Member States [1]. Its seat is in Geneva but its premises are located on both sides of the French-Swiss border (<http://cern.ch/fplinks/map.html>).

CERN's mission is to enable international collaboration in the field of high-energy particle physics research and to this end it designs, builds and operates particle accelerators and the associated experimental areas. At present more than 11 000 scientific users from research institutes all over the world are using CERN's installations for their experiments. The accelerator complex at CERN is a succession of machines with increasingly higher energies. Each machine injects the beam into the next one, which takes over to bring the beam to an even higher energy, and so on. The flagship of this complex is the Large Hadron Collider (LHC) as presented below:

Further information is available on the CERN website: <http://cern.ch>

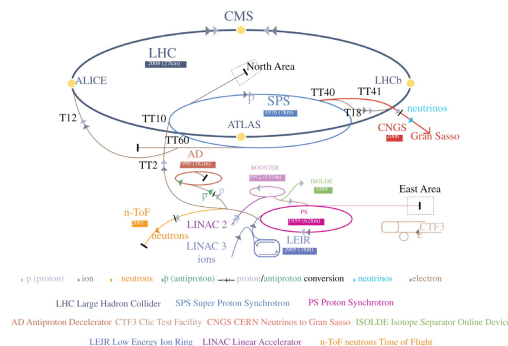


Figure 1.1: The accelerator complex at CERN.

1.2 ATLAS

ATLAS, or A Toroidal LHC ApparatuS (www.atlas.ch), is a particle physics experiment at the Large Hadron Collider (LHC) at CERN. The ATLAS detector is designed and constructed to make new particle discoveries resulting from head-on collisions of protons produced by the LHC of extraordinarily high energy. ATLAS will investigate the basic forces that have shaped our Universe since the beginning of time and that will determine its fate. Among the possible discovery candidates are confirmation of the existence of extra dimensions in space, unification of fundamental forces, and evidence of dark matter in our Universe. The ATLAS detector is located in an underground cavern on the Swiss part of CERN. The experiment is in operation and produces physics results. The ATLAS collaboration involves more than 3000 scientists from 182 institutions in 38 countries.

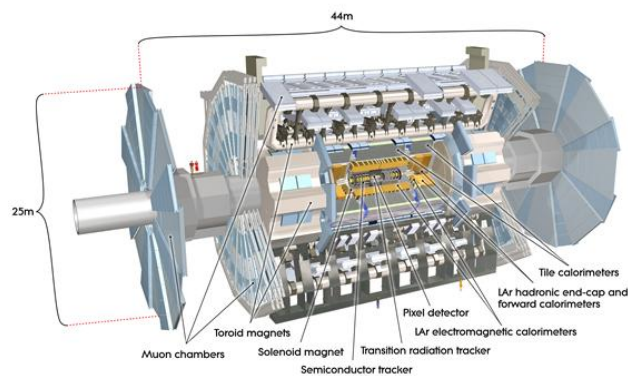


Figure 1.2: A 3D cut-out view of the ATLAS detector.

1.2.1 Inner Detector

The Inner Detector (ID) is the first part of ATLAS to detect the decay products of the collisions. It is very compact and highly sensitive. It consists of three different systems of sensors, all in a magnetic field parallel to the beam axis. The ID measures the direction, momentum, and charge of electrically-charged particles produced in each proton-proton collision. The main sub-detectors of the ID are: Pixel Detector, Semiconductor Tracker (SCT), and Transition Radiation Tracker (TRT).

- **Pixel:** The Pixel detector consists of some 80 million pixels (channels) and a resolution of $14 \times 115 \mu\text{m}^2$.
- **SCT:** The SemiConductor Tracker (SCT) is a set of silicon microstrips (6 million channels), each placed $80 \mu\text{m}$ from the other, achieving resolution of $17 \mu\text{m}$.
- **TRT:** The Transition Radiation Tracker (TRT) detector consists of about 300,000 straw tubes with a gold-plated tungsten wire in the center. There are straws parallel and perpendicular to the beam-line, ultimately reaching $170 \mu\text{m}$ particle tracking resolution.

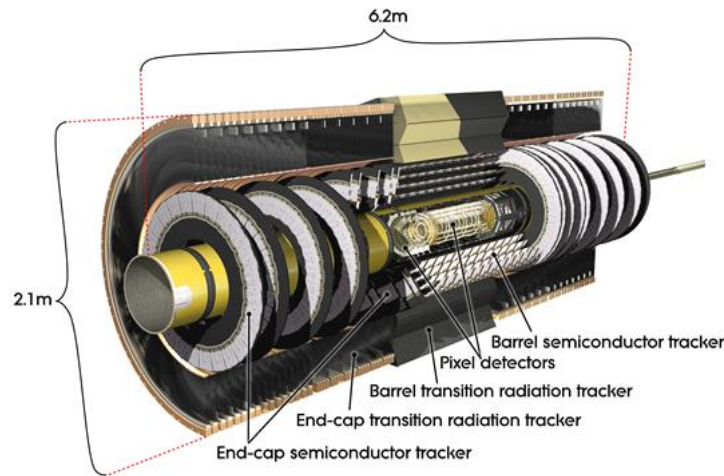


Figure 1.3: A 3D cut-out view of the ATLAS Inner Detector.

1.2.2 Calorimeter

Calorimeters measure the energy a particle loses as it passes through the detector. Designed to absorb energy of most particles coming from a collision, forcing them to deposit all of their energy within the detector. Calorimeters typically consist of layers of “passive” or “absorbing” high-density material – for example, lead – interleaved with layers of an “active” medium such as solid lead-glass or liquid argon.

Electromagnetic calorimeters measure the energy of electrons and photons as they interact with matter.

Hadronic calorimeters sample the energy of hadrons (particles that contain quarks, such as protons and neutrons) as they interact with atomic nuclei. Calorimeters can stop most known particles except muons and neutrinos.

The components of the ATLAS calorimetry system are: the Liquid Argon (LAr) Calorimeter and the Tile Hadronic Calorimeter.

- **Tile Hadronic Calorimeter:** Consisting of a central barrel made of 64 wedges, each 5.6 m long and weighing 20000 kg, and two extended barrels each with 64 wedges, each 2.6 m long and weighing 9600 kg. All of this amounting to 500,000 plastic scintillator tiles.
- **Liquid Argon (LAr) Calorimeter:** Consisting of a barrel 6.4 m long, 53 cm thick, and 110,000 channels. Works with Liquid Argon at -183°C LAr endcap consists of the forward calorimeter, electromagnetic (EM) and hadronic endcaps. EM endcaps each have thickness 0.632 m and radius 2.077 m. Hadronic endcaps consist of two wheels of thickness 0.8 m and 1.0 m with radius 2.09 m. Forward calorimeter has three modules of radius 0.455 m and thickness 0.450 m each.

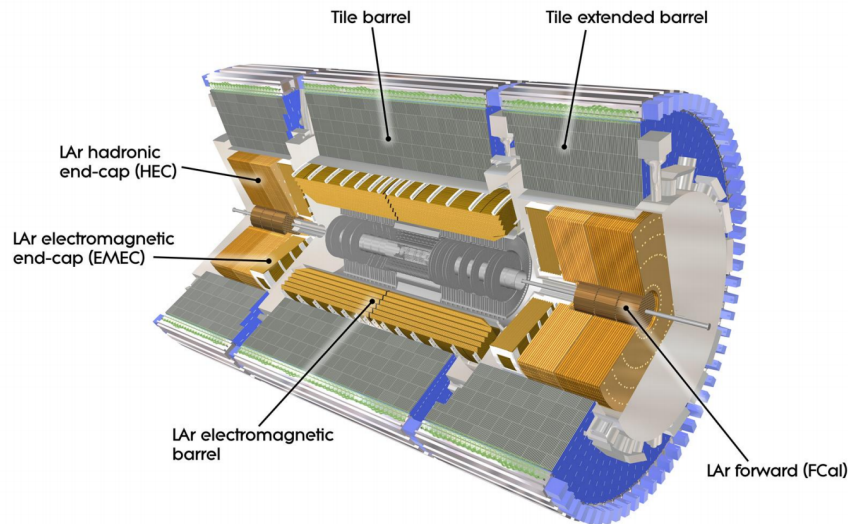


Figure 1.4: A 3D cut-out view of the ATLAS Calorimeter.

1.2.3 Muon spectrometer

The Muon Spectrometer is the outer part of the geometry. Its purpose is identifying their momentum and track, which is bent from the Magnet system. The detector technologies used are:

- **Monitored Drift Tubes (MDT):** Thousands of tubes cover the majority of ATLAS' solid angle. The building block is an aluminum tube, with a wire in the center. The passing particle ionizes the gas (Ar:CO₂ mix, 93:7), which results into multiple ionizations, due to the voltage difference applied between the tube and the wire. This "avalanche" of charge induces a signal on the wire, which is read-out on the end of the wire. The signal times correspond to radius inside the tube, since the drift in the gas is well studied. Combining all tubes, we deduce the track of the passing particle. See Fig. 1.5.
- **Cathode Strip Chambers (CSC):** The main purpose is precision tracking in the small-radius region, where particle rates are beyond MDT limits ($> 150 \text{ Hz/cm}^2$). Belonging to the category of multi-wire proportional chambers (MWPC), operating with a gas mixture of Ar:CO₂ (80:20), they utilize cathode strips and anode wires achieving $60 \mu\text{m}$ resolution on the precision coordinate and 5 mm on the secondary. See [2] for more details on operation, installation and performance in ATLAS.
- **Thin Gap Chambers (TGC):** Mainly a Triggering detector, for ATLAS, operating on a gas mixture of CO₂:n-pentane (55:45), built similar to the CSC, with an anode wire in the middle of the gas gap. On each side the graphite cathode boards complete the gas gap, followed by the read-out strips. Performance and production for ATLAS can be found at [3].
- **Resistive Plate Chambers (RPC):** These chambers are composed of two parallel resistive plates forming a gap filled with C₂H₂F₄-IsoC₄H₁₀-SF₆ (94.7-5-0.3) gas mixture. The plates are covered with readout strips at their back which are perpendicular to each other so that an $\eta - \phi$ measurement is possible. The electric field between the plates is of about 9800 V. They have a spatial resolution of 1 cm and timing resolution of 2 ns.

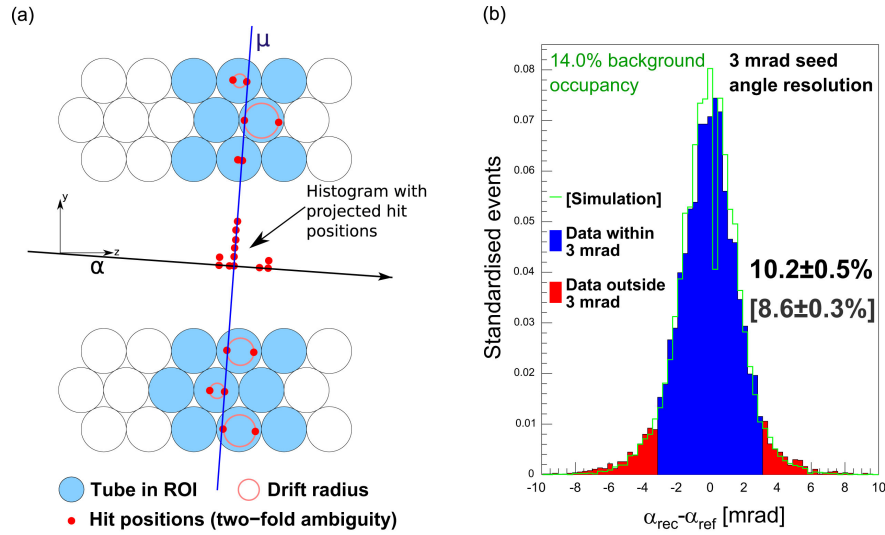


Figure 1.5: (a) Illustration of the histogram based pattern recognition method which projects the measured drift radii of the MDT tube layers perpendicular to the expected track direction. (b) Results of the MDT trigger demonstrator test at the CERN Gamma Irradiation Facility for the maximum background occupancy expected at HL-LHC. The results presented in black indicate the fraction of low-quality tracks, while these given in parentheses correspond to the Geant4 simulation output. Taken from [4].

1.2.4 Magnet System

The magnet system of ATLAS bends particles around the various layers of detector systems, making it easier to contain the tracks of particles. It consists of:

- the Central Solenoid, which provides a magnetic field for the ID
- the air-core Barrel Toroid (BT) and
- two air-cored Endcap Toroids (ECT) providing a toroidal field configuration for the muon spectrometer.

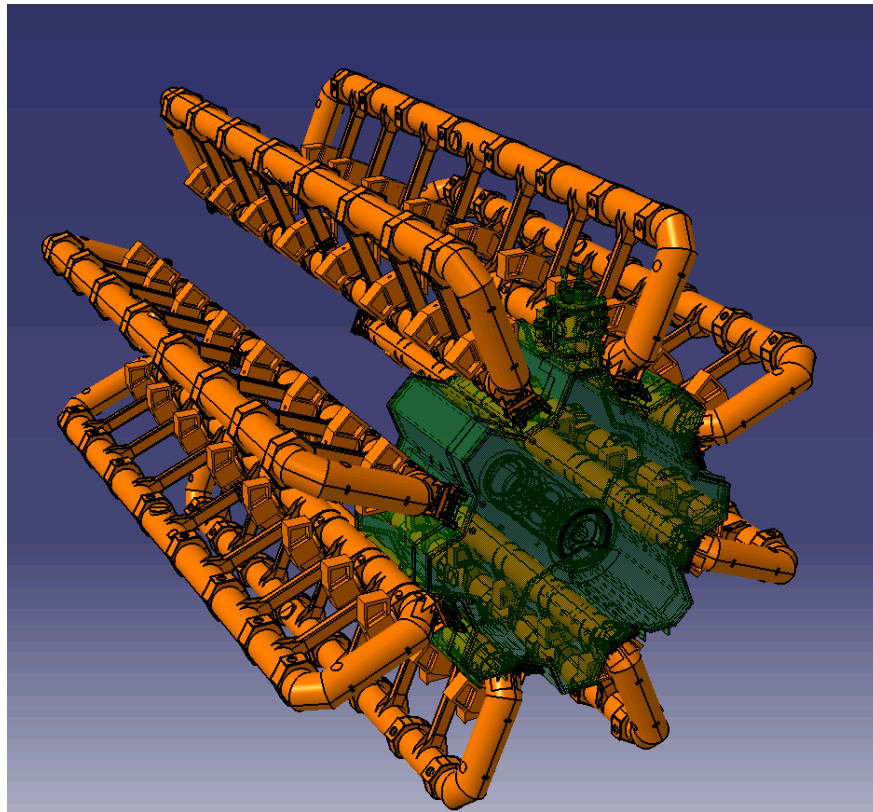


Figure 1.6: A 3D representation of the ATLAS Barrel and Endcap Toroid assembly.

1.2.5 Operation

The detector is operated from the control room, on the surface. Shifters monitor and control the state of the detector night and day for operation but also for safety reasons. As long as the LHC provides collisions every 25ns, ATLAS needs to cope with the amount of data produced in the detectors. This is done with the Trigger system, followed by the Data Acquisition, and final storage.

- **Trigger:** It is a system of three levels of event selection, at each step refining this process. The initial rate is 20MHz, which needs to be reduced to a few hundred Hz of events in order to arrive to permanent storage. The Level-1 Trigger is responsible for the first refinement, hardware based, using a limited amount of information from the detectors, to make a decision within 2.5us, and finally reduce the rate to 100kHz. Next, the High Level Trigger (HLT) is the Level-2, software trigger, which leads to the last level, called Event Filter (EF), which processes full events and produces 300Hz of event data to be stored.
- **Data Acquisition (DAQ):** This system retrieves the data from the front-end electronics, which is assembled in events, synchronized to the main clock of the experiment (TTC). Communicating with the Trigger, in many levels, the data is further filtered down to a rate of 300Hz, then forwarded for persistent storage.

More details on Trigger and DAQ at [5].

1.3 New Small Wheel upgrade for ATLAS

270 The goal of the New Small Wheel (NSW) Upgrade project of ATLAS is to replace the innermost station of the endcap muon system with new detectors during the next long shutdown in 2019/20. For particle detection, tracking and triggering, two different detector technologies will be used: MicroMesh Gaseous Structure (Micromegas, or MM) and small-strip Thin Gap Chambers (sTGC). Both are capable of operating under the high background rates expected during future LHC operation. Trapezoidal detector compound
 275 wedges of two sizes will be arranged on a wheel-like structure of 10m diameter. See more details in the NSW Technical Design Report [6].

1.3.1 Performance

The motivation for building the NSWs is improved performance of ATLAS during the High Luminosity operation of the LHC. This revolves around the following two points:

- 280 • **Trigger:** Studies on the data from the first years of ATLAS operation have shown an unexpectedly high rate of fake triggers in the end-cap region. This originates from low-energy particles generated between the inner and middle end-cap station, which are then detected by the trigger chambers, in an angle similar to real high momentum muons. This effect can be seen in Fig. 1.7. The NSW should provide better angular track resolution, in order to reduce this mismatch in the end-caps.

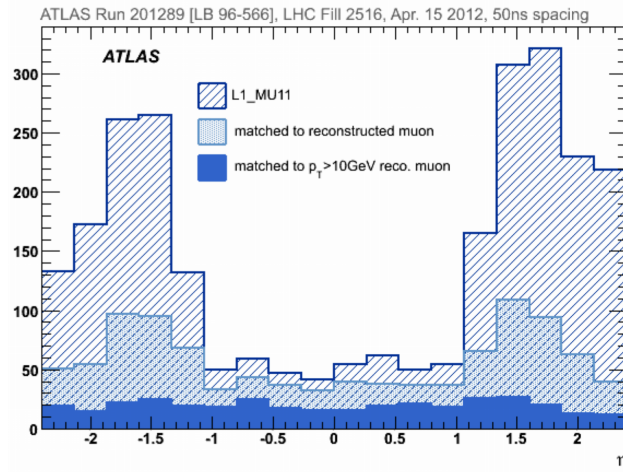


Figure 1.7: η -distribution of the L1 muon signal ($p_T > 10$ GeV) with the subset of matched muon candidates, $p_T > 3$ GeV and $p_T > 10$ GeV.

- 285 • **Tracking on high rate:** The current tracking chambers of the endcap are the MDT, which will not be able to maintain their tracking efficiency at the rates of HL-LHC (Fig. 1.8).

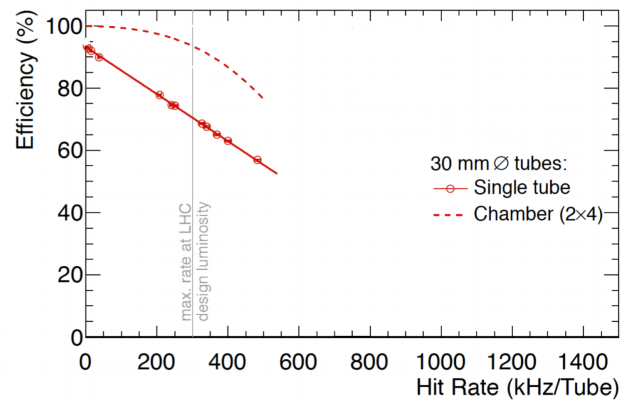


Figure 1.8: Testbeam data, showing the MDT efficiency as a function of the incoming particle rate.

These two points must be dealt with by the NSW. The next section shows how the chosen detector technologies accomplish that.

1.3.2 Detector Technologies

The NSW consists of two detector technologies, the Micromegas (MM) and the sTGC. Their principle of operation and features are described below.

- **Micromegas (Micro-mesh Gaseous Structure)** is the primary tracking chamber, also with very good triggering capabilities. It belongs to the family of Micro-pattern gaseous detectors with strips. The gas used is a mixture of Argon and CO₂, and the strips are placed every 450 μm . The measurement precision for this technology is $O(70 \mu\text{m})$ for normal tracks, and just a bit worse for inclined tracks. The fast signals allow a response time of a few ns for a signal over the threshold. Further details will be given in a next chapter, since the detector is a main part of this thesis.
- **sTGC (small-strip Thin Gap Chambers)** is the primary triggering chamber, also with very good tracking capabilities. The schematic structure of the sTGC is shown in Fig. 1.9 . It consists of a gold-plated tungsten wire with diameter of 50 μm and spacing of 1.8 mm, operating at 2.9 kV. The anode wire is in the middle of the two cathode plates, 1.4 mm from either of them. The cathode is made of a 200 μm thick FR4 insulation layer with graphite coating. Signal pick-up copper strips or pads are located behind the insulation layer and 1.3 mm FR4 boards are the support of the insulation layer.

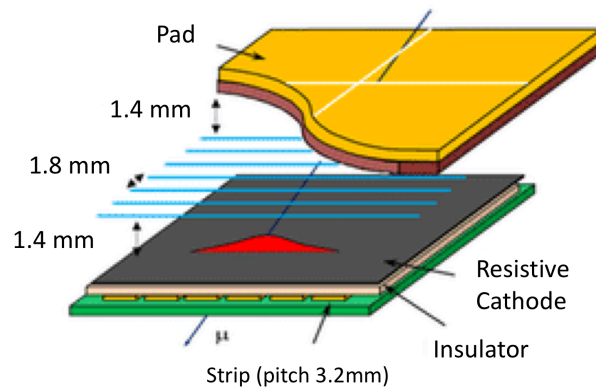


Figure 1.9: sTGC detector structure.

1.3.3 Design Layout

305 In this section the NSW mechanical layout is described, internally but also within the ATLAS system. As shown in Fig. 1.10 (an exploded view of a NSW), the layout is as follows:

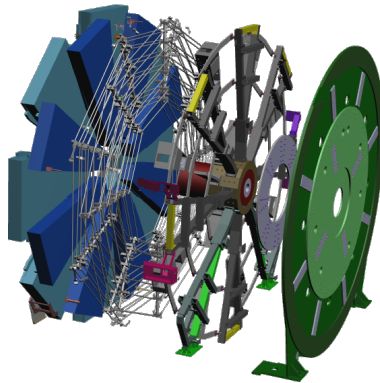


Figure 1.10: NSW exploded view.

- The new JD (NJD) is the endcap shielding disk for ATLAS. Its primary purpose is to stop the majority of hadrons from reaching the muon chambers and the rest of the cavern. It also acts as the main support for the NSW structure and chambers. It is an iron disk, ~ 10 m in diameter, carefully designed to support the ~ 100 ton wheel, but also provide access points for alignment features.
- The NSW structure, consisting of bicycle-like spokes, fixed on the NJD, which in turn will be the support of the detectors. In this aluminum structure, the alignment bars are also housed.
- The alignment bars are equipped with cameras facing each other, in order to detect very small movements of the chambers (due to temperature, humidity, misalignment, mistakes), which is crucial for later software corrections.
- The sectors, each being 1/16th of the NSW, are smaller assemblies of chambers. Each sector consists of two sTGC wedges (outside), two MM wedges (inside) and one Spacer Frame (middle support).

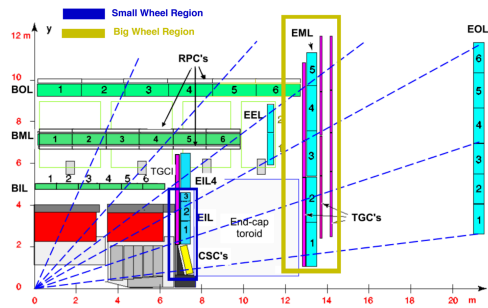


Figure 1.11: ATLAS cross section, focusing on the Muon chambers layout.

The NSW is located at the inner endcap of the ATLAS barrel. A cross section is shown in Fig. 1.11. The barrel trigger chambers (RPC), the Big Wheels with MDT and TGC at the middle and outer endcap, and lastly part of the magnet system (barrel and endcap toroid) are also shown in the picture.

Chapter 2

Micromegas detector

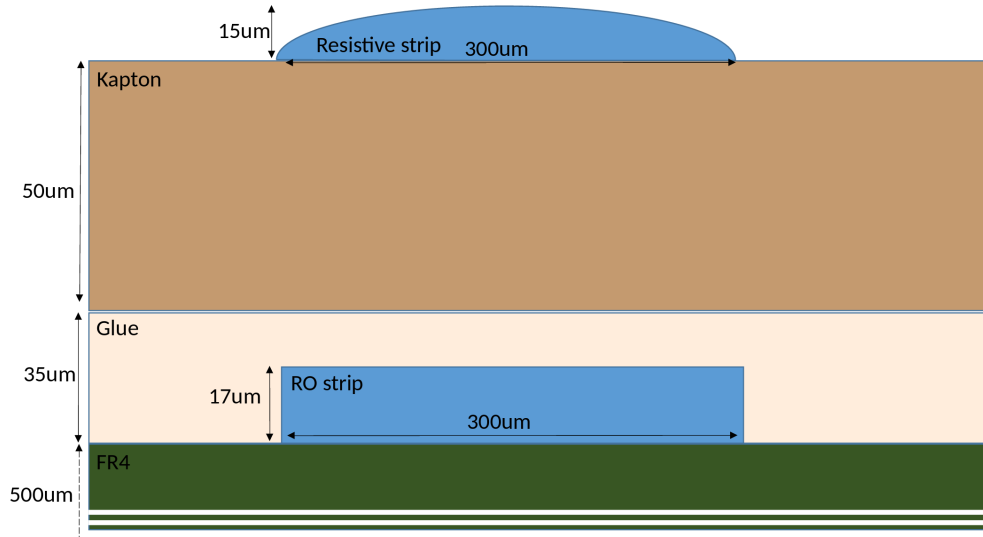


Figure 2.1: Close-up sketch of the resistive Micromegas readout PCB geometry.

2.1 Operation outline

325 The Micromegas technology was developed in the 90s, as part of the micropattern gaseous particle detectors family. The generic idea behind this family of detectors is the ionization of the gas due to a passing particle. The movement of the produced ions induces current on a set of copper wires/strips, forming a strong readable signal [7].

The MM principle of operation, as illustrated in Fig. 2.2, can be explained through the following steps:

- a particle passes through the detector, ionizing the gas atoms (primary ionization)
- 330 • the electrons and ions traverse the drift gap, in some 100 ns.

- electric field ($\sim 0.6 \text{ kV/cm}$) separates the ions further and brings the electrons to the amplification gap
- higher electric field ($\sim 50 \text{ kV/cm}$) induces an avalanche effect on the ions, creating 10^4 ions for each primary ionization
- ions moving towards the cathode induce charge on the Readout strips below
- the induced charge is readout as a pulse at the end of the strip by electronics
- the measured charge distribution, along with the timing of each signal, is converted to position and timing of the track

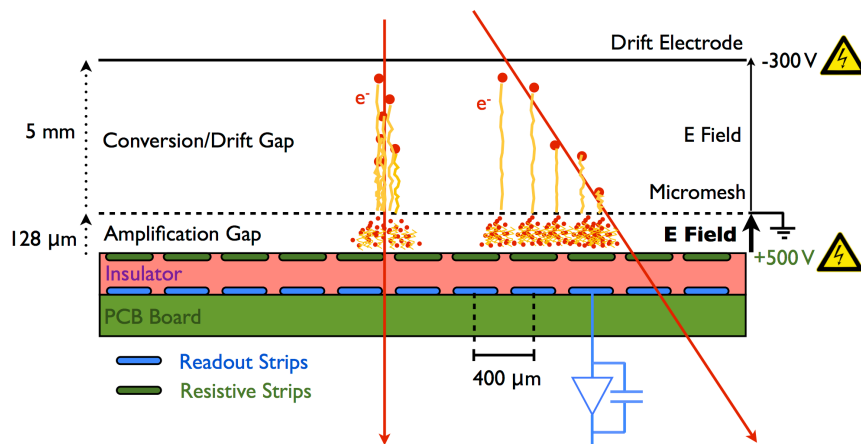


Figure 2.2: The Micromegas operation principle

The MM technology is a robust combination of tracking and trigger detector, due to the good spatial ($100 \mu\text{m}$) and timing (100 ns) resolution. As described in [6], such values are a requirement for the high rate that ATLAS will have to cope with in Run 3 [8].

In the next few sections a detailed look into the principles of operation is presented.

2.2 Particle interactions to signal formation

The operation principle of any particle detector is based on the interaction between the incoming particles and the molecules/atoms of the detection medium that results in a detectable signal. For Pixel and SCT detectors the medium is a semi-conductor sensor, for Calorimeters it's a scintillating material (e.g. liquid noble gases, plastic), and for gas detectors, obviously, a gas. Usually the interaction is the ionization of the gas atoms, resulting in free ions and electrons. Applying an electric field, the ions are moving, inducing charge on the nearby conductors. This charge is then sampled in special electrical circuits and transformed to a signal.

Important principles are :

- the energy loss of particles in the medium: For particles heavier than the electron, this is described in

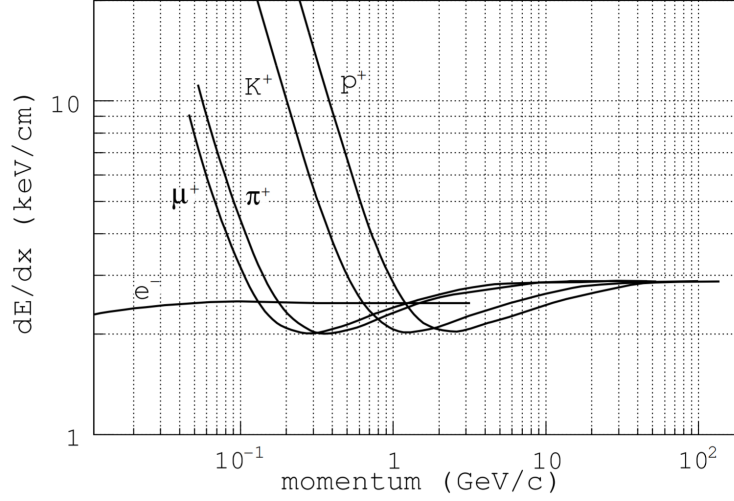


Figure 2.3: Mean energy loss per unit length dE/dx in argon at normal conditions as a function of the momentum for various particles [9]

the well-known Bethe-Bloch equation 2.1.

$$\left\langle \frac{dE}{dx} \right\rangle = \frac{4\pi}{m_e c^2} \frac{n z^2}{\beta^2} \left(\frac{e^2}{4\pi\epsilon_0} \right)^2 \left[\ln \left(\frac{2m_e c^2 \beta^2}{I(1 - \beta^2)} \right) - \beta^2 \right] \quad (2.1)$$

where n is the electron density of the material, z the charge of the incident particle, Z and A the atomic number and mass of the absorber, and I the mean excitation energy of the atoms in the absorber material. Here we omit the δ -term which is negligible for gases.

This equation shows that the energy loss initially decreases like $1/\beta^2$ and goes through a minimum at $\beta \sim 3.2$. Particles with energies close to this minimum are called minimum ionizing particles (MIPs). At higher velocities, the field of the incoming particle becomes stronger and spreads across the medium. Moreover, the maximum energy transfer increases too and the energy loss per unit length rises again. At larger values of $\beta\gamma$, the medium becomes polarized by the particle field which is shielded by the polarization field. The energy loss saturates and reaches the so-called Fermi plateau. The dependence of dE/dx on the particle momentum and type is illustrated in Fig. 2.3. Over certain momentum ranges, the energy loss depends significantly on the particle type and can be used for particle identification purposes.

- the probability of ionization: Atoms near the path of the particle (e.g. muon) "see" a short pulse of E field. There is some probability that an electron in the atom will be excited to a higher level or thrown right out of the atom - primarily ionized. Ionization is the main mechanism of energy loss of the muon in matter. An example: Assuming a gas at STP, atom size 10^{-10} m, density ~ 1000 th of liquid, ergo path length 10^{-7} m. In 1 cm of Argon the muon will pass within $1 \text{ \AA}$ of 8 400 atoms but on average only 25 will be ionized and even fewer excited. "Large number of opportunities for low probability events". In other words primary ionization follows Poisson statistics.

2.2.1 Movement in gas

An ionized atom (ion) or freed electron can move around the gas, but soon recapture each other. An external electric field can put them on a path towards the cathode/anode. This drift velocity is shown in Fig. 2.4, taken from simulation [10]. Also more detailed descriptions of ion and electron mobility in [11].

2.2.2 Signal formation

When charges are moving in front of a conductor, a proportional charge is induced on the conductor. The Micromegas geometry, as shown in Fig. 2.2, contains the amplification gap, where the electric field is up to 50 kV/cm. This gives rise to an avalanche effect of ion-electron pairs being created due to successive ionizations.

In a first simplified approach, assuming a Micromegas geometry, with a single strip under voltage, for a point charge q the induced current is:

$$I_a = -q \frac{\mathbf{E}_A \cdot \mathbf{u}}{V_a} \quad (2.2)$$

where E_A is the electric field at the position of the charge, u the velocity of the charge, and V_a the potential of the strip. Taking all charges into account, as a current density term, $J(x, t)$, the induced current takes the form:

$$I_a = -\frac{1}{V_a} \int \mathbf{J}(x, t) \cdot \mathbf{E}(x) d^3x \quad (2.3)$$

To derive the total signal formation, we need to insert the evolution of charge over time. The charge multiplication depends on the (first) Townsend coefficient α which in general, among other things, is a function of the electric field. If n is the number of one type of charged particles at a certain point, then at a nearby point along the path of the moving charge the increase of the charges will be expressed as $dn = \alpha n dr$, where dr is the distance between the two points. In order to calculate the charge increment one has to integrate the above formula. Assuming some simplifications, the following formula can be easily derived:

$$I(t) = -q_0 \frac{\alpha \beta e^{\alpha \beta u_p t} u_p}{V_a} \int_0^{z_1} E_z(z) e^{\alpha \beta z} dz, \quad \beta = \frac{u_n}{u_n + u_p} \quad (2.4)$$

where q_0 is the initial charge (one e^-), $u_{p/n}$ the velocity of the ions/electrons, E_z the z-component of the electric field. The derived current as a function of time is also drawn in Fig. 2.5. Detailed derivation is in [12].

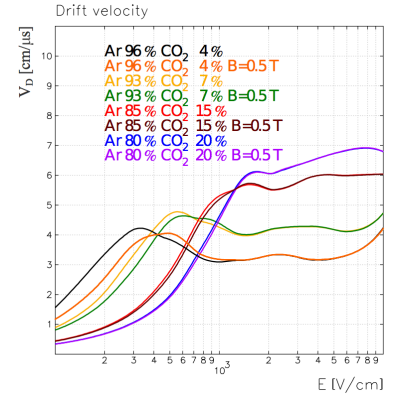


Figure 2.4: Electron drift velocity for Ar:CO2 mixtures

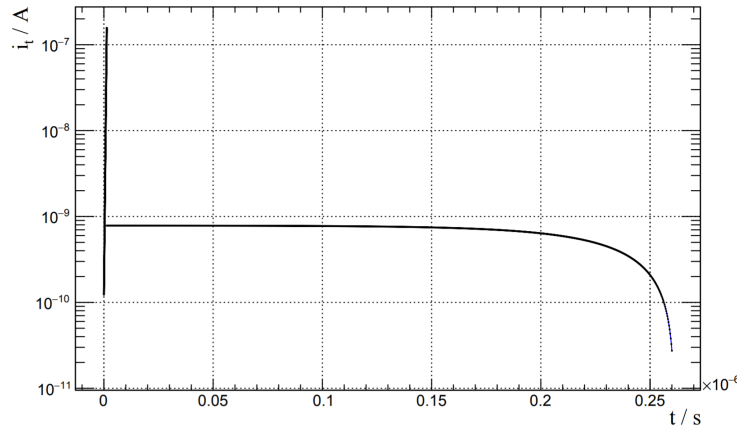


Figure 2.5: Total induced current as a function of time. The peak at the origin for times less than 2 ns is due primarily to the electrons movement while after the 2 ns the distribution is due to the ion drifting towards to the mesh.

Fig. 2.5 beautifully illustrates the pulse expected on the strips and read-out electronics. A short under-shoot due to the electrons in the very beginning, and later an increasing pulse peaking before 200ns.

2.2.3 Capacitance

This signal induced on the resistive strips is capacitively mirrored onto the readout strips, allowing it to then reach the readout electronics at their edge. However, the charge is also induced on the neighbouring strips, what is called **cross-talk**. This mechanism essentially spreads the incoming induced charge over more than one strip, creating a smearing effect on the charge profile. This has been studied in the past with small prototype Micromegas chambers (T-type, see table 2.1), with the charge sharing ratio resulting to around 16%. This is indicated also in Fig. 2.6, taken from K. Ntekas' thesis [11], where the charge ratio at the edges of the cluster is filled in a histogram. The peak at 5-6 on the first graph shows that the first strip of the cluster is systematically less active than the second, which indicates cross-talk behavior at the level of 16%, agreeing with simulations.

Another important effect of capacitance between strips is the induced noise. In this frame, noise signifies what is readout by the front-end electronics (or an oscilloscope) when no signal is expected (no particle passing). Since, in reality, every system has an expected noise originating from the intrinsic capacitance, the Micromegas will also have its own effects, to be discussed below.

In the large Micromegas chambers, as tested in summer of 2018, the corresponding results are shown in Fig. 2.7. It is shown that for the large chamber, the charge ratio peaks closer to 2 for the **edge of the cluster**, indicating higher cross-talk effect, in the order of 50%. This means that the cluster deposited over the strips of a cluster is smeared over the strips, resulting in a distorted interpretation of the measured charges for each strip. In the **middle of the cluster** the ratio remains at 1, as expected, given the random distribution of charges in any direction in the cluster. In the **end of the cluster** the ratio is a bit more spread (as in the small chambers), due to larger travel times, allowing diffusion and, therefore, uncertainty in the distribution. Note that the beginning of the cluster is defined as the side with the fastest firing strips of the cluster (for example

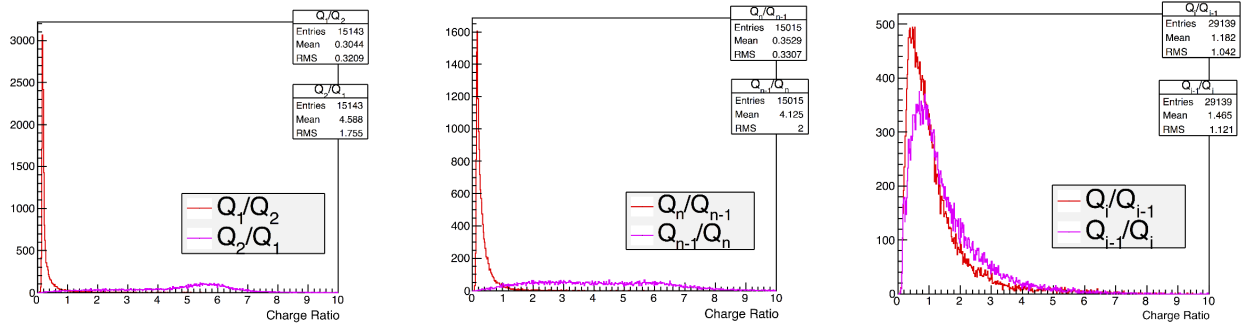


Figure 2.6: Strip charge ratios for 30 degree tracks at the beginning (left), end (middle) and middle (right) of the cluster, on a run with the small T-chambers. Taken from K. Ntekas' thesis [11].

in Fig. 2.2 the right ones).

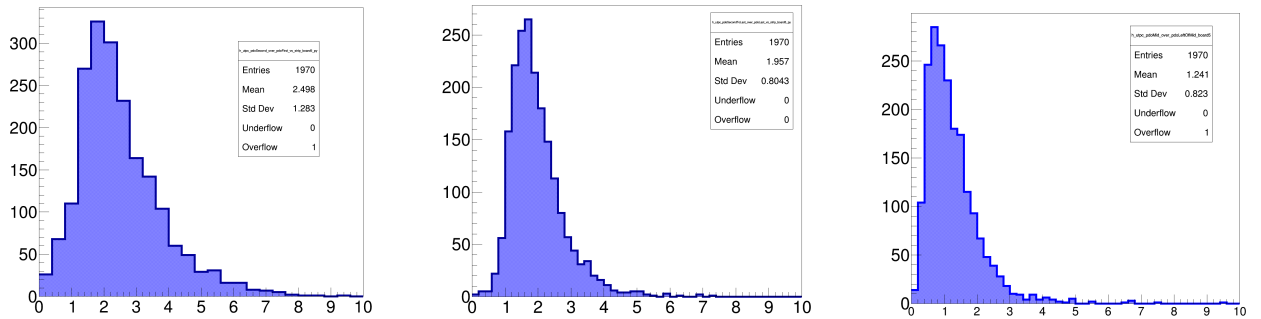


Figure 2.7: Strip charge ratios for 30 degree tracks at the beginning (left), end (middle) and middle (right) of the cluster, on a run with the large SM2 module. Taken from K. Ntekas' thesis [11].

2.3 Signal response simulation

425 In order to validate the cluster-edge charge ratios, we compare the experimental data with the simulation results, considering the detector as an electrical circuit. This simulation uses proprietary software by Ansoft (later ANSYS), namely Maxwell and Simplorer (all later incorporated into Electronics Desktop [13]).

2.3.1 Capacitance calculation with simulation

430 The first step is to extract the capacitance of the system. This is done by replicating the Micromegas geometry in the Maxwell software, either in 2D or 3D, representing the materials as insulators or conductors, with the correct dielectric constant. A complete example of the geometry, along with the resulting values is shown in Fig. 2.8, for the large Micromegas chambers (SM and LM).

435 Values of interest here are: the coupling of a resistive strip with the readout strip underneath it (160 pF/m), the coupling of a strip with its neighbor (30 pF/m for LM, 38 pF/m for SM). Especially the second one, gives a very good indication of the charge sharing, showing 30% difference from LM to SM. This particular

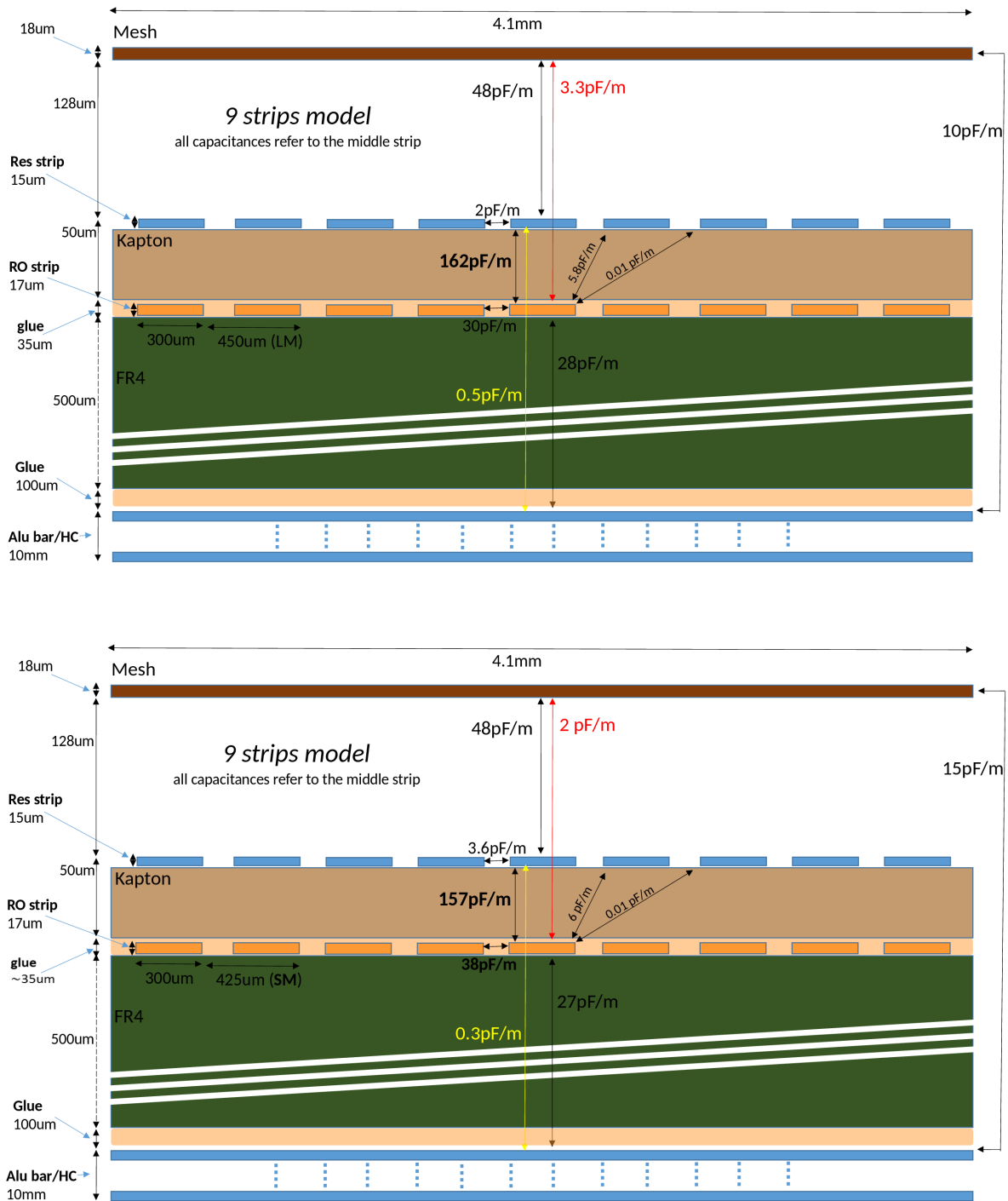


Figure 2.8: Overview of the strip capacitances for the NSW-type Micromegas chambers.

result has been validated also in the lab with measurements on a real chamber (type SM2), where the strip length is a bit less than 2m and a measured capacitance of 300 pF/m. As expected, this difference is mirrored also in the noise measurements in the lab.

The reason for this is that the SM-type chambers have smaller strip pitch (425 μm) than the LM-type (450 μm), which clearly increases the capacitance between neighboring strips.

2.3.2 Equivalent circuit simulation

This is the second step for the Micromegas signal simulation. Taking the capacitance values from the previous step, a simulated circuit is adapted to them while given a simple square pulse as input signal to the resistive strip. The output is a simplified pulse that the electronics would see. The range of the simulation is from three to nine strips, focusing on the middle one. The simplified circuit of Fig. 2.9 is adapted and repeated, implementing the capacitive couplings between strips and mesh. Part of this extended circuit is shown in Fig. 2.10.

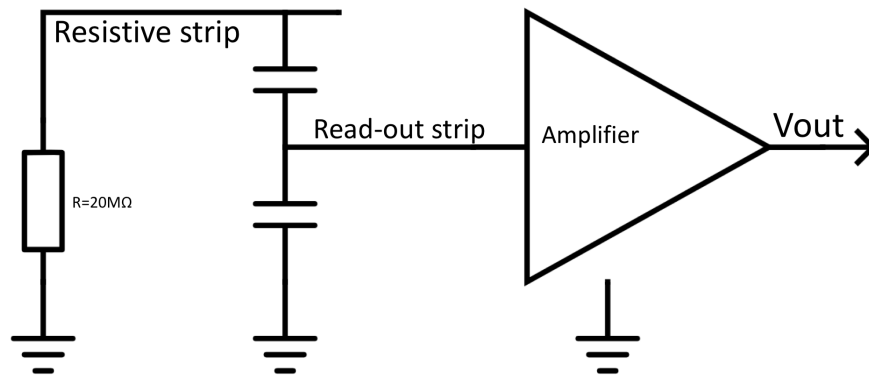


Figure 2.9: A single read-out and resistive strip pair as a simplified circuit. The resistive is shown as a 20 MΩ resistance, capacitively coupled to the readout. The readout is also coupled to the ground (the mesh), and then led to an amplifier and shaper circuit.

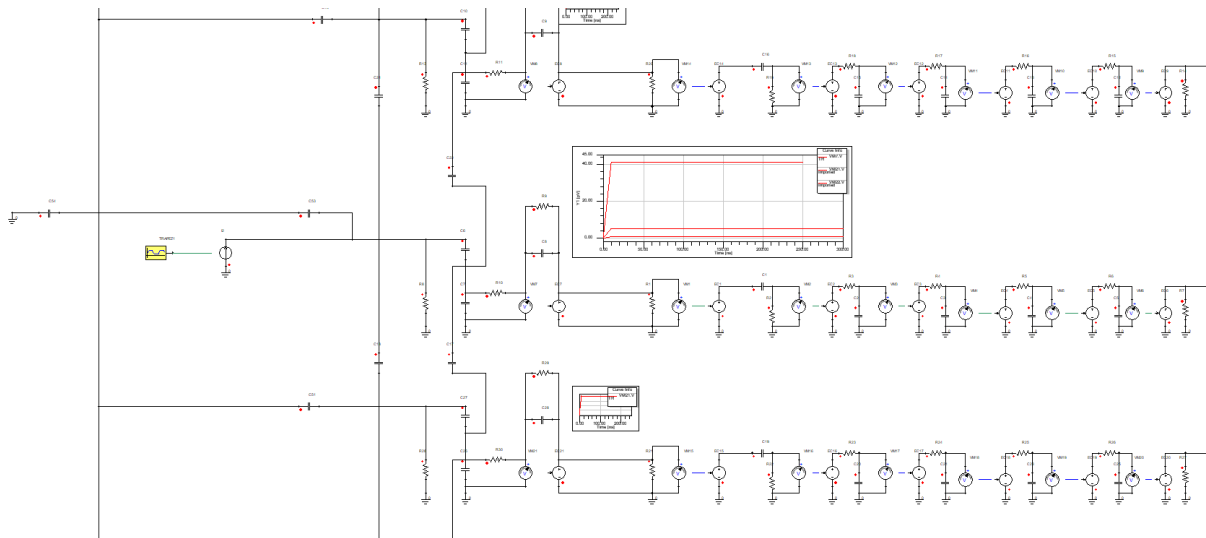


Figure 2.10: Sketch of the simulated circuit for three strips (arrange in three rows), as a screenshot from the Simplorer software. The bigger part on the right is an implementation of the CRRC, while the left portion is mainly the simplified circuit from Fig. 2.9. This implementation was initially done by K. Petrolis in his thesis.

2.4 Test with beam

MM prototypes have been tested in beams for many years. Several studies to understand and further characterize the technology have been performed during these tests. Part of this work is described in this section.

2.4.1 Chambers tested

Numerous MM prototypes have been tested. An indicative list is shown in Table 2.1. This series of tests was done in parallel to the design and development of the NSW MM, in order to optimise the final parameters. Several studies pointed to better or worse results, as seen in the following subsections.

MM chamber	Strip width/ pitch [μm]	Resistivity [$\text{M}\Omega/\text{cm}$]	Mesh wire $\varnothing$ / Opening [μm]	Pillars $\varnothing$ /pitch [mm]
TmmX	150/250	25	18/45	0.3/2.5
TmmY	80/250			
T1-4	300/400	25	18/45	0.3/2.5
T5-8	300/400	8	18/45	0.3/2.5
T4C	320/400	25	18/45	0.3/2.5
	220/400			
	120/400			
	80/400			
ExMe	300/450	25	18/45	0.5/5.0
			18/60	0.5/7.0
			30/50	0.5/8.0
			30/71	0.5/10.0
MMSW	300/415	1	30/50	0.3/2.5
MMS1/2 ¹	3250/3500	1 (perp. to RO)	18/45	0.3/2.5
TQF	300/400	25	18/45	0.5/5.0
Tmb X	150/250	25	18/45	0.5/5.0
Tmb Y	80/250			
TLP*	80/400	1	18/45	0.3/2.5
J*	30/400	25	18/45	0.3/2.5
TZ*		25	18/45	0.3/2.5
SM (NSW)	300/425	1	18/45 ²	0.3/2.5
LM (NSW)	300/450	1	18/45 ³	0.3/2.5

Table 2.1: Micromegas chamber characteristics

2.4.2 Definitions

Several terms will be used, so they are clarified here:

- **cluster** is a set of RO strips that fired in the same event, and are consecutive in the detector. In general, a maximum of 1 empty strip is allowed in a cluster.
- **cluster size** (width) is the number of strips that fired. Unless noted, the empty (not fired) strips are not included in the counting.
- **cluster charge** is the PDO sum of the cluster strips.
- strip/cluster **cuts** are applied on several variables, in order to filter out noise and mis-reconstructed clusters.
- **residuals** are the differences between two test planes, in order to identify the statistical deviation and offset of the measurement.
- **double gaussian fit** will be used on the residual distributions to identify the real resolution of the measurement plane, and differentiate from other background factors such as misalignment.
- **stereo** strips are like the standard eta strips of the MM, except they are rotated by ± 1.5 degrees. This allows reconstruction of the second coordinate (ϕ), clearly with worse resolution.

2.4.3 Testbeam setups timeline

Through the years, micromegas prototypes were tested, both in PS and SPS extraction lines. Given that R&D for MM was ongoing, several different configurations were tested, in the scope of optimising the technology. The prototypes and tests, which were carried out in the timeframe of this thesis (2014-2018), are described below.

The test beams used at CERN:

- PS lines - T9,T10: The beam lines are derived from the 24 GeV/c primary beam from the PS. The T9 beam is a secondary beam that delivers secondary particles up to 15 GeV/c, whereas T10 reaches 7 GeV/c. There are Multiwire Proportional Chambers (MWPC) installed upstream, providing beam diagnostics. The main target (electrons) is 200 mm Beryllium and 3 mm Wolfram. The hadron target is 200mm of Aluminum.
- SPS lines - H4,H6,H8: The SPS extraction lines are located in EHN1. The H* lines are derived from the same target. They comprise high energy, high-resolution general purpose beams used for experiments and tests. Maximum momentum is 400 GeV/c.
- GIF++ is also housed in EHN1, but is primarily a gamma irradiation test facility. A ^{137}Cs source, embedded between two Tungsten blocks, can be moved in the middle of the area, resulting in exposure of almost 1 Gy/h, at a distance of 1m. Lead and steel attenuators are also available offering flux reduction with a factor up to 50 000.

2014 marked the start of Run2 for the CERN accelerator complex, which also allows running testbeams at CERN. At this time, a long set of testbeams started, carried out every year on Micromegas prototypes to understand further their operation as well as the electronics.

PS complex - T9 and T10 line, SPS complex H6 and H4 lines - 2014

In 2014, the studies focused on:

- Re-establishing the expected results from the Tmm* and T* chambers. The expected position resolution of 60 μm is confirmed.
- Understanding the effect of misalignment between resistive and RO strips, using the TQF chambers.
- Study of the first MMSW chambers, constructed to approach the final size of the NSW MM, to later run inside the ATLAS cavern for further testing.

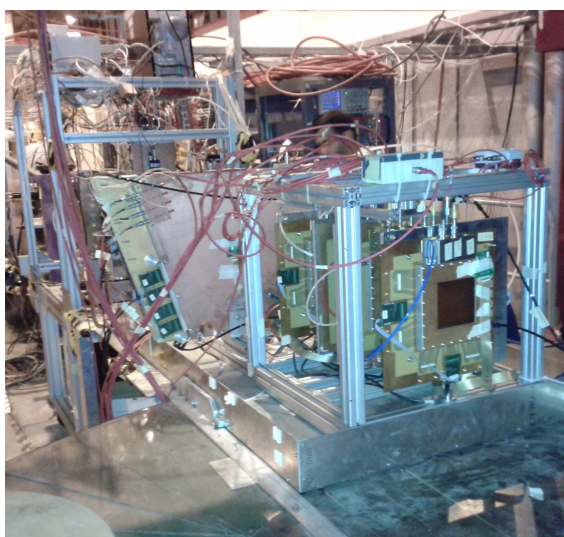


Figure 2.11: Testbeam setup at H4, October 2014.

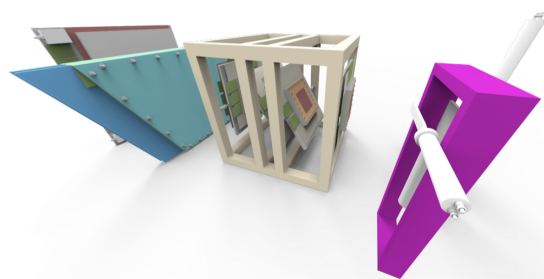


Figure 2.12: 3D model of the setup at H6 2014.

SPS, H6 - 2015

The ExMe (exchangeable mesh) chamber was made to allow easy and safe replacement of the mesh, allowing to test different types of meshes without the need to retension the mesh. Additionally, the T4C chamber was produced, designed with four different regions of strip width, while maintaining the pitch, in order to understand the capacitance effect from strip to strip and its effect on noise and charge spreading.

The J-chambers, produced in Japan, featured a floating mesh, which is supported on the pillars, and finally kept in place thanks to the voltage difference. The main purpose for the J chambers was to validate the type of material selected for the insulating layer between readout and resistive strips, the Kapton.

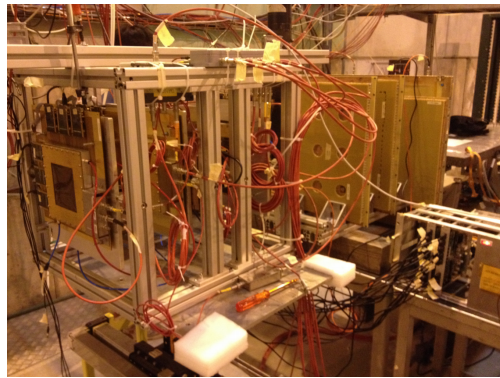


Figure 2.13: Testbeam setup at H6, October 2015.

SPS - H4 - 2015

The MMS chamber was tested in B-field, inside the Goliath magnet, in order to study the effect on a chamber with larger pitch. Also two T-chambers were installed to run with mini2-VMM electronics.

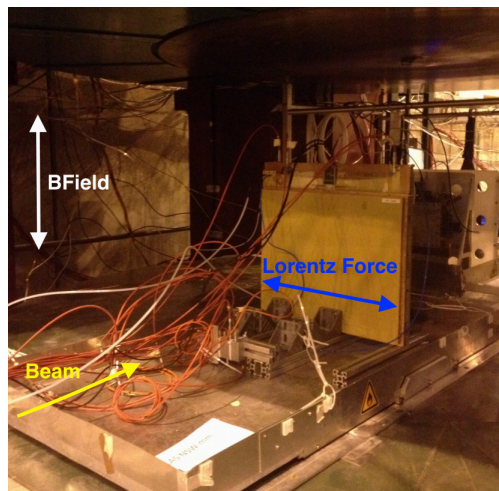


Figure 2.14: Testbeam setup at H4, October 2015.

510 SPS - H6 - 2015

In September 2016, the scheduled studies/tests include:

- the established T* and Tmm* as reference telescope
- different types of Kapton foils, using the J-chambers
- pillar effects with the ExMe (exchangeable mesh) chamber
- different strip widths with the T4C

515

- stereo strips with 3.5mm pitch with the MMS

The ExMe chamber components are shown in Fig. 2.15.

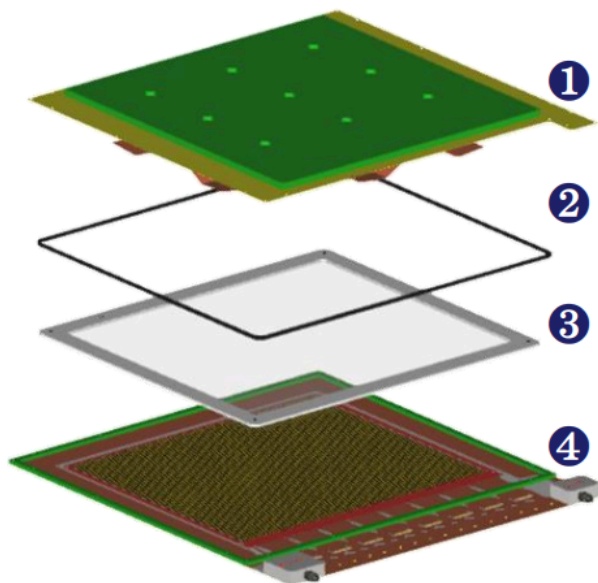


Figure 2.15: Exploded view of the ExMe micromegas chamber. The components shown are 1) the drift panel (stiff-back and drift cathode), 2) the o-ring, 3) the mesh frame and 4) the readout panel.

SPS - H8B - 2016

In May-June 2016, the first big MM module arrives at CERN for testing, the SM1. Testbeam goals:

- SM1 Module0 characterization
- TLP chambers test
- test mini2 card with VMM2 on T* chambers

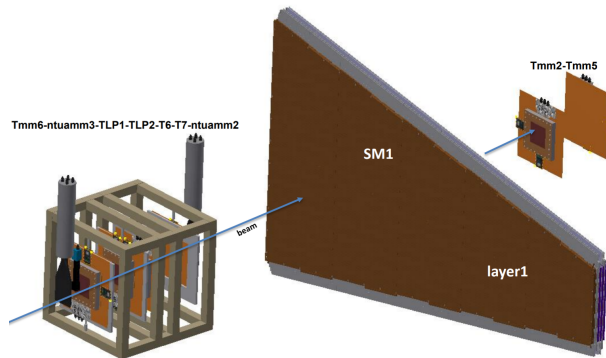


Figure 2.16: Testbeam setup at H8, May 2016.

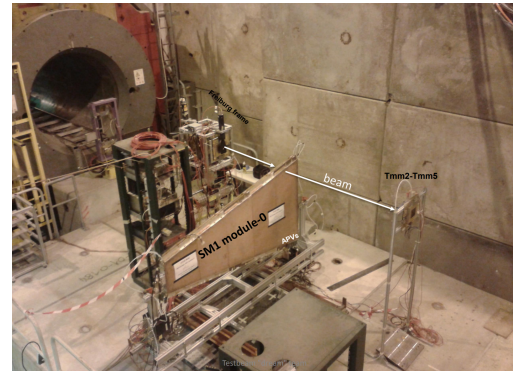


Figure 2.17: 3D model of the setup at H8 2016.

SPS - H8C - 2017

The LM2 module-0 is delivered to CERN during Spring 2017 to be tested with beam in June.

- LM2 readout with APV electronics and later with VMM
- get reference track from frame of scintillators
- TZ chambers with MMFE8-vmm3 boards

SPS - H8C - 2018

The first production module of Micromegas SM2 type is tested in beam, using small T- and Tmm-chambers for tracking, all using MMFE8 cards.

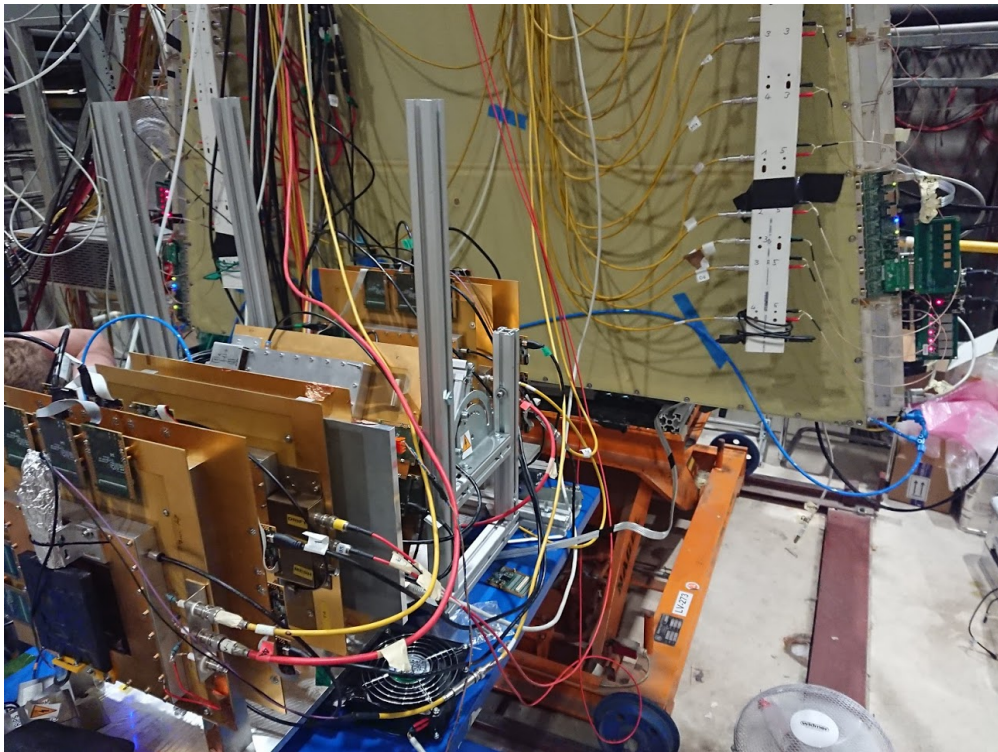


Figure 2.18: The 2018 H8C setup.

2.4.4 T chambers - typical results

The small Micromegas prototypes have been extensively tested since 2010. Here we will go through some of the expected results and ones that we have confirmed throughout the testbeam periods. Especially the first histograms that will be shown serve as reference plots to confirm that the combination of chamber and electronics are running well.

First, in Fig. 2.19, for each electronics board (here, column) we have row by row:

- the beam profile: simply showing which strips fired. This usually resembles the profile we see on the beam monitors from the wire scanners.
- PDO distribution: showing all the PDO values of the run, normally similar to a Landau distribution, along with some accumulation spikes which originate in the VMM ADC.
- TDO distribution: again showing the entire value range, which will make more sense later in the time calibration.
- BCID distribution: Here the relative BCID is shown, since the electronics were running in L0 mode, which with an incoming trigger opens an 8 BC window of readout and it looks for hits in this window. Depending on the delays and settings set, this distribution should be centered and symmetric.
- Strips per event: Again, depending on the noise and chamber size we expect the strips per event to peak at small numbers.

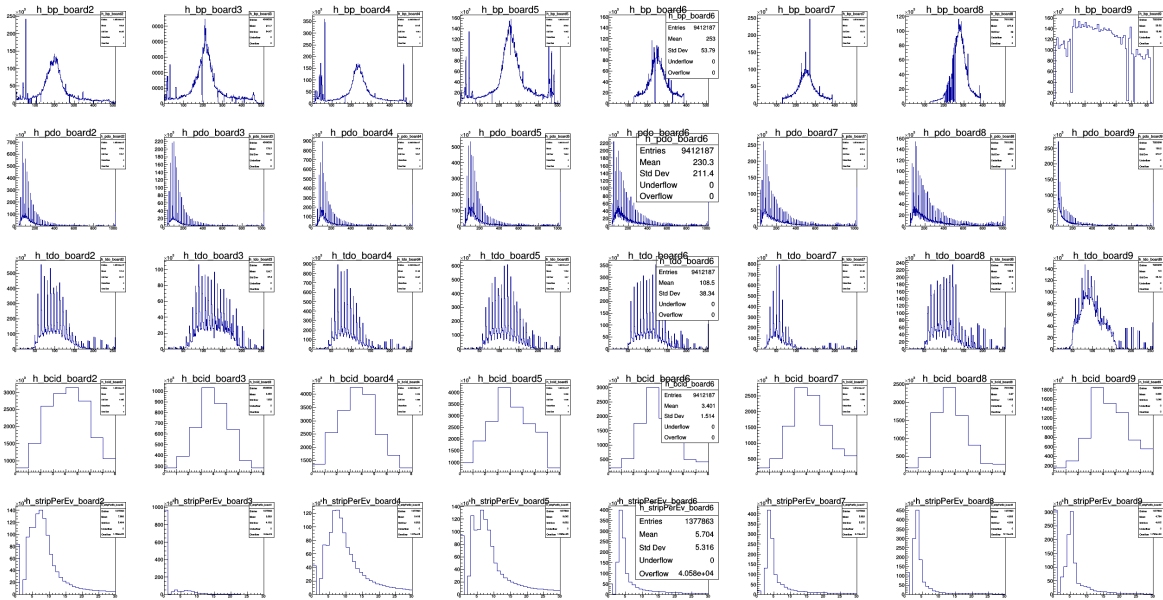


Figure 2.19: Typical raw data statistics from the testbeam. The first four columns correspond to four SM2 layers, while the rest are from the T and Tmm chambers in the telescope (as in already shown setups).

Second, in Fig. 2.20, again for each board, we have row by row:

- numbers of clusters per event: This should be peaking at 1. The events with 0 clusters should be very few, originating either from inefficiencies or noisy events. Those with 2 or more clusters can come from multi-track events, while the much larger numbers are most likely from events with delta electron ray or from cases of distributed noise.
- beam profile, this time using the cluster reconstructed position, using centroid method
- cluster charge, this time following much better the Landau distribution
- cluster size, for single cluster events only
- cluster size, for all clusters. The cluster size should peak at 2-4 for normal tracks, and at 5-8 for inclined tracks, depending on the angle and VMM parameters.

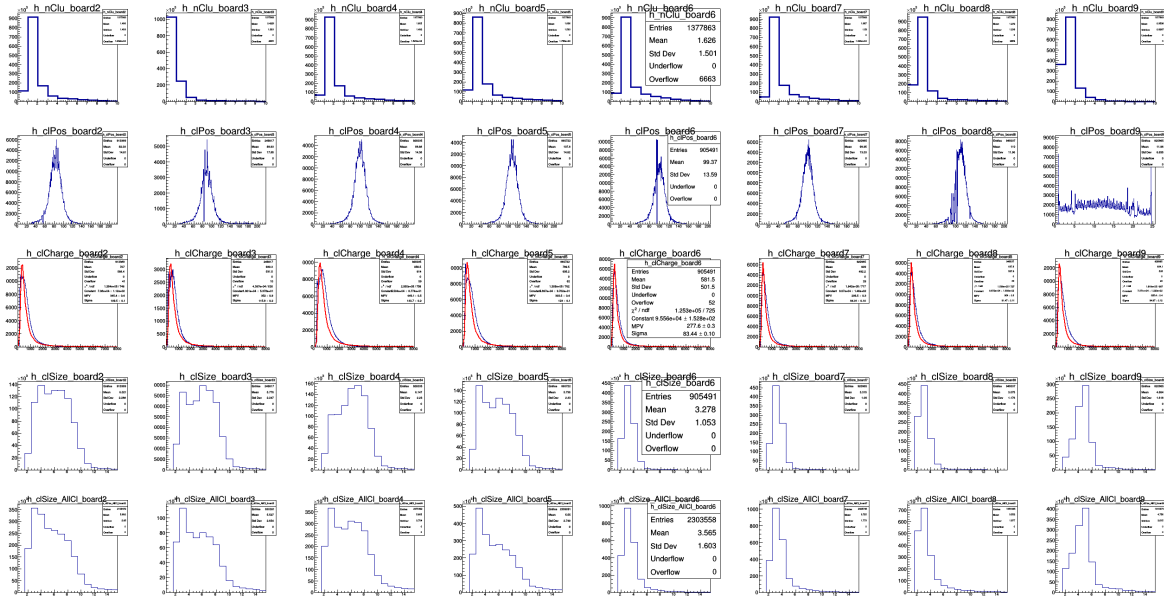


Figure 2.20: Typical cluster data statistics from the testbeam. The first four columns correspond to four SM2 layers, while the rest are from the T and Tmm chambers in the telescope (as in already shown setups).

2.4.5 MMS - large pitch

Another effort to optimize the Micromegas architecture was the MMS chambers. The idea is to study the behavior of a Micromegas with larger strip pitch, to test how the resolution, capacitance, cross-talk, and HV behavior change. Another motivation is to test the eta correction algorithm from [14], which has potential to improve small clusters (2-3 strips).

Eta correction

This algorithm has been used in Pixel detectors, where there is high number of small clusters [14]. It was also studied by K. Ntekas in [11].

It starts with the following problem: In small clusters, there is a systematic preference for a single strip to gather the majority of the charge, while the neighbors gather considerably less than 10% of the total charge. This results in a biased reconstructed position in the middle of the strips (or between the strips for even-sized clusters). The eta correction aims at restoring this imbalance. The position along the pitch is corrected according to the charge ratio, which should also follow a smooth curve, without preference towards the middle of strips. This is not as simple to implement correctly, since clusters are not always perfect and strips are missing. The algorithm first gathers all data from the chamber, from one run, and creates the histogram with all ratios of charges for the two-strip clusters. Then, it re-processes each cluster by applying a correction from the global statistics histogram from the previous step, in order to smoothen the distribution and tackle the bias.

As in [11], for the small MM prototypes, this correction gave a small improvement, but not as significant

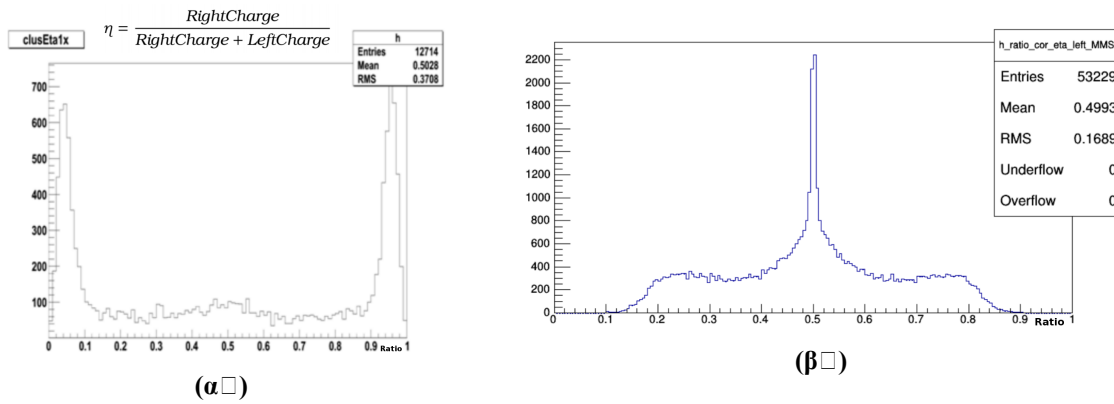


Figure 2.21: Eta ratio distribution for early T-type chambers (left) and MMS chamber (right). The largely different behavior of the ratio is clear, and originates from the different capacitive coupling on the large MMS strips. The avalanche "sees" the strips much differently on these two chambers (see also Fig. 2.22).

as expected, compared to the Pixel detector application. In particular for the MMS chamber, this correction could not be applied properly. The ratio behavior was opposite from what expected (See Fig. 2.21). The charge ratio is biased towards 50%, meaning the two strips have usually the same charge, rather than always having one of the two being less than 10% of the other.

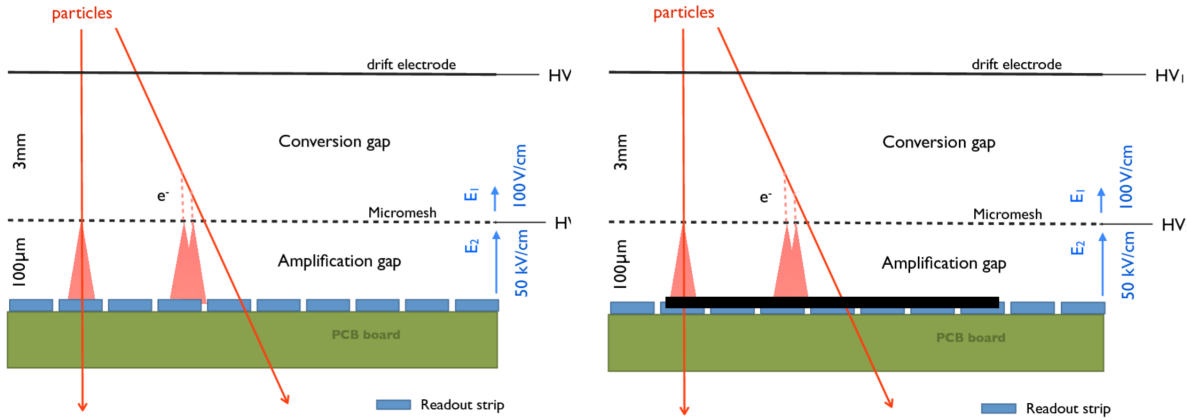
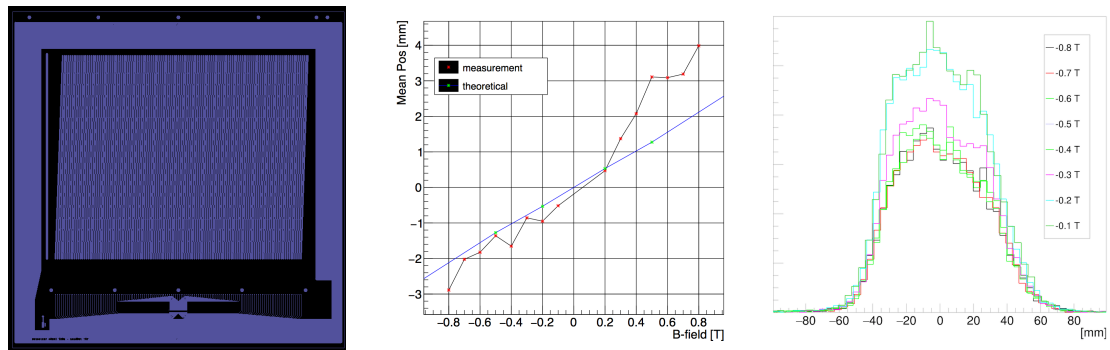


Figure 2.22: Comparison of the geometry that the electron avalanche affects, showing the different strip widths. The charge

Apparently, due to the different physics of charge induction on the Micromegas strips, the eta correction does not yet provide notable improvement on the position reconstruction performance of the detector.

The MMS chamber

The MMS chamber gerber file can be seen in Fig. 2.23. This chamber consists of two layers of 128 strips, 4 degrees inclined with respect to each other. The main difference compared to the usual prototypes is that the strip pitch is 3.5mm. The chamber was tested also in B-field, to understand potential misbehavior



(α) View of the strip pattern of the MMS chamber. (β) MMS mean position vs B-field value (parallel to RO strips). (γ) MMS beam profiles for different B-field values.

Figure 2.23: MMS chamber strip patterns and reconstructed position B-field dependence.

due to the unusual geometry (see Fig. 2.23). In the mentioned figure, the theoretical curve is also shown. Difference in positive values is due to non-linear behavior in the magnet field set values. An interesting effect is reconstructing the position for even or odd sized clusters. The two different cases are producing beam profiles with preferred reconstruction on the middle of the strip (odd) or between the strips (even) (See Fig. 2.25). This effect is actually explained in reverse: When the charge deposition is closer to the middle of a strip, then an odd sized cluster is more likely, since the charge will be slightly but equally shared to the neighbouring strips. On the other hand, when a particle passes between two strips, then the charge is mainly shared between the two strips, and then with their respective neighbours, similarly resulting in an even sized cluster. This effect is pronounced for the MMS chamber (2.25), due to its geometry, however it is also visible in the regular pitch Micromegas. This is shown later along with the results from the big chambers, but also the cluster statistics study.

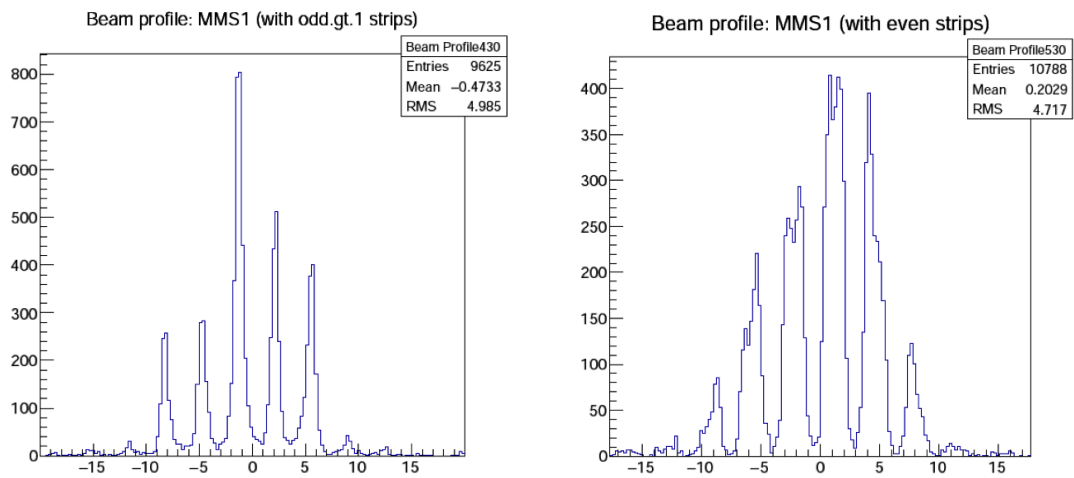


Figure 2.24: MMS layer 1 beam profile, **LEFT:** using only clusters with odd number of strips (>1), **RIGHT:** only clusters with even number of strips.

Another interesting calculation is to extrapolate the expected resolution from a strip chamber like the MMS. We know for the small chambers with 250μm pitch that the residual sigma is around 100μm. This means

that with the Micromegas, we can roughly reconstruct the position 2.5 times better than the strip pitch. For the MMS scale, this translates to an expected resolution around 900 μ m.

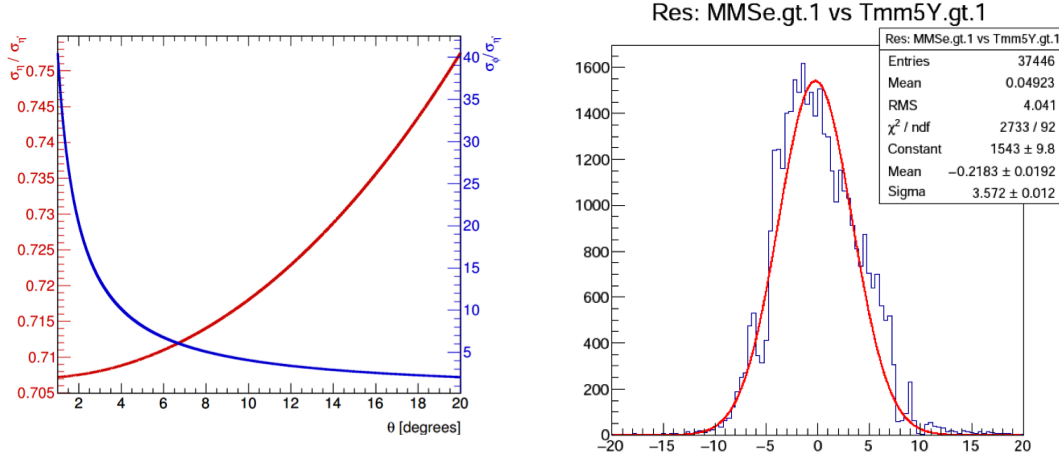


Figure 2.25: LEFT: Expected resolution after reconstruction from two inclined strip layers as a function of the inclination to the resistive strips, **RIGHT:** residual distribution for MMS and Tmm5Y.

2.4.6 T4C: Width scan & simulation

One of the main parameters studied was the effect of the RO strip width. This is done with the T4C chamber. The underlying feature here is the capacitance, since the chamber geometry is basically a collection of capacitors. As explained in the MM operation above, the signal is induced on the strips, which are capacity-coupled with each other. Due to this coupling, cross-talk is introduced. This means that charge is induced on the strips not only by the drifting ions, but also by the nearby strips.

This collection of capacitors was simulated to identify the expected capacity, signal response, and cross-talk.

Capacitance map

The T4C chamber has four areas with different strip width. In the gerber file (PCB drawing file) the arrangement of the different areas is shown (Fig. 2.26).

2.4.7 Timing studies

The J chambers were used at the H6 line, in order to understand the timing properties of the chamber. For this study, the legacy APV electronics were used [15]. These chambers feature a floating mesh, instead of the usual bulk-type prototype MM, where the mesh is embedded in the pillars for increased stability. We study the timing features of these chambers to understand how the floating mesh affects the expected results. The methods for understanding the timing have been previously studied by K. Ntekas [11].

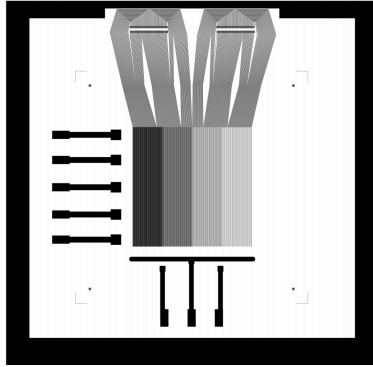


Figure 2.26: View of the strip pattern of the T4C chamber, from a gerber file.

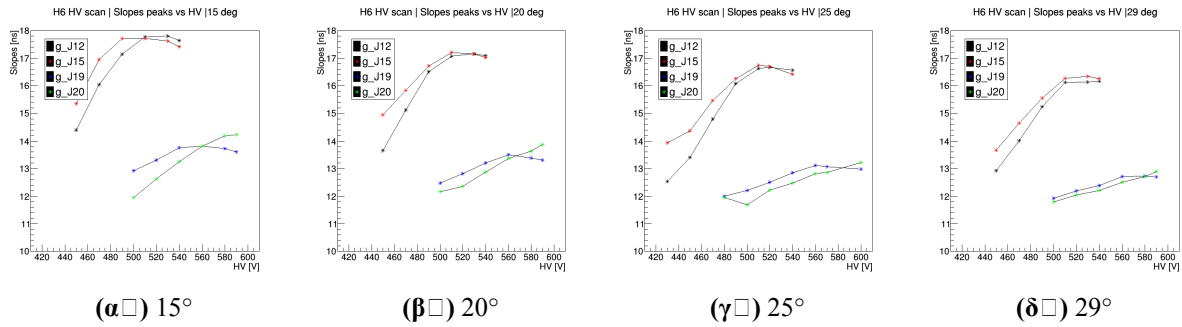


Figure 2.27: Summary plots of High Voltage scans of the J chambers for different incident track angles, showing the response of the most probable value of the slope for each point.

The APV electronics, contrary to the newer VMM chip, do not provide the peak charge and timing information of the signal. The data read-out is actually the sampled data of the signal, in 25 ns steps. So, before any clusterisation starts, pre-processing must be done in order to produce the hit charge and timing. In particular the timing is done by fitting the signal histogram with a Fermi-Dirac function, and then attributing the time of the inflection point to the time of the hit. The fit function used is given in Eq. 2.5 .

$$q = q_{\text{base}} + \frac{q_{\text{max}}}{1 + e^{-(t-t_{FD})/\tau}} \quad (2.5)$$

The t_{FD} is the time corresponding to the inflection point, while the τ is a scale factor which we call "slope", corresponding to how fast the fit function rises.

2.4.8 VMM - parameter scan

The VMM chip is the main electronic chip that needs to be understood to fully optimise the detector operation and the later data processing. For this reason we embark on a parameter scan of the VMM settings. In Fig. 2.32 the neighbor logic effect is shown in the size of the clusters. The neighbor logic is an internal setting of the VMM, which triggers the readout of strips that are below the threshold and next to a strip that is over the threshold and normally read-out.

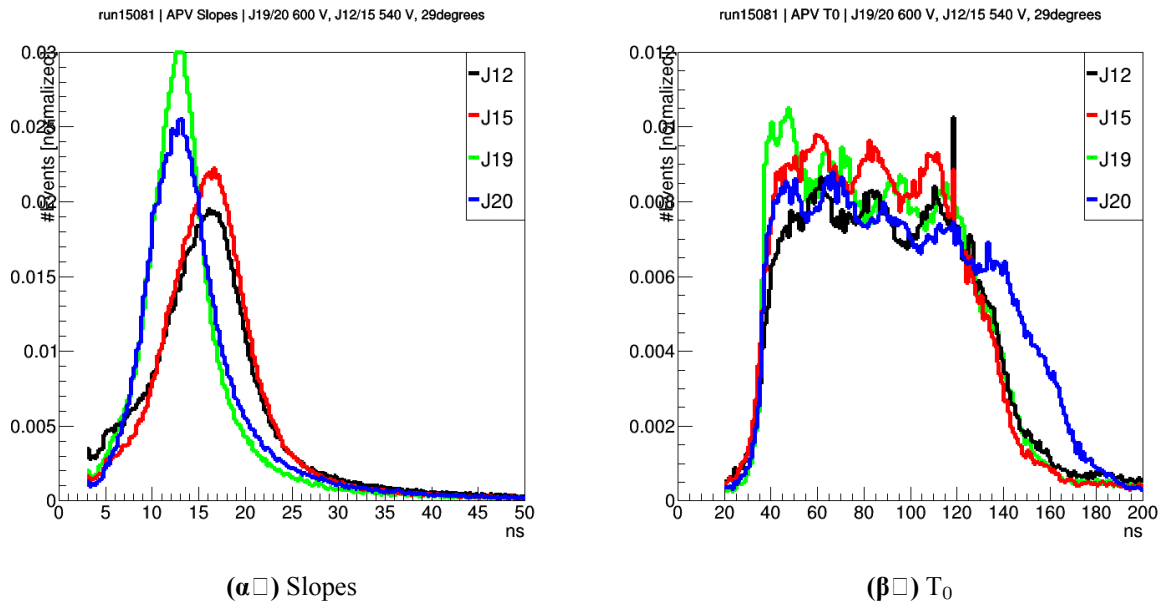


Figure 2.28: Plots from one step of the High Voltage scan of the J chambers. On the left, the measured slopes (values of τ) from the Fermi-Dirac function. On the right, the measured inflection points (t_{FD}). It's interesting to see the range of values of times, which give the time-window of the drift gap; i.e. the shortest and longest drift times that we can measure, which correspond to the 5 mm of drift, translated to ns using the drift velocity as measured in past experiments.

The resolution comparison for different threshold f-factors, peaking times and neighbor logic is shown in Fig. 2.32.

- For larger threshold cuts (x8) it seems that the neighbor logic recovers good strips which would not have been readout. For smaller threshold factors (x6) the noisy testbeam environment at the time seems to prevail and the neighbor logic doesn't help.
- The fast peaking time (100 ns) works better by giving better timing, while the 200 ns seem to gather more of the non-gaussian noise at the testbeam environment.
- It's important to note that indeed in that particular testbeam, the noise measured on the detector was not yet at final levels of understanding. As described in a later section about calibration, the threshold measurements were performed but showed that the noise had several components not so easy to get rid of, without losing significant portion of the real charge.

2.4.9 Large Micromegas

Strip alignment

Another example of probing the mechanical properties of the detector is by checking the strip alignment. When constructing a Micromegas quadruplet, the eta planes should be perfectly aligned. Of course this is not possible due to the tolerances of production. The nominally accepted misalignment is 20 μm . This

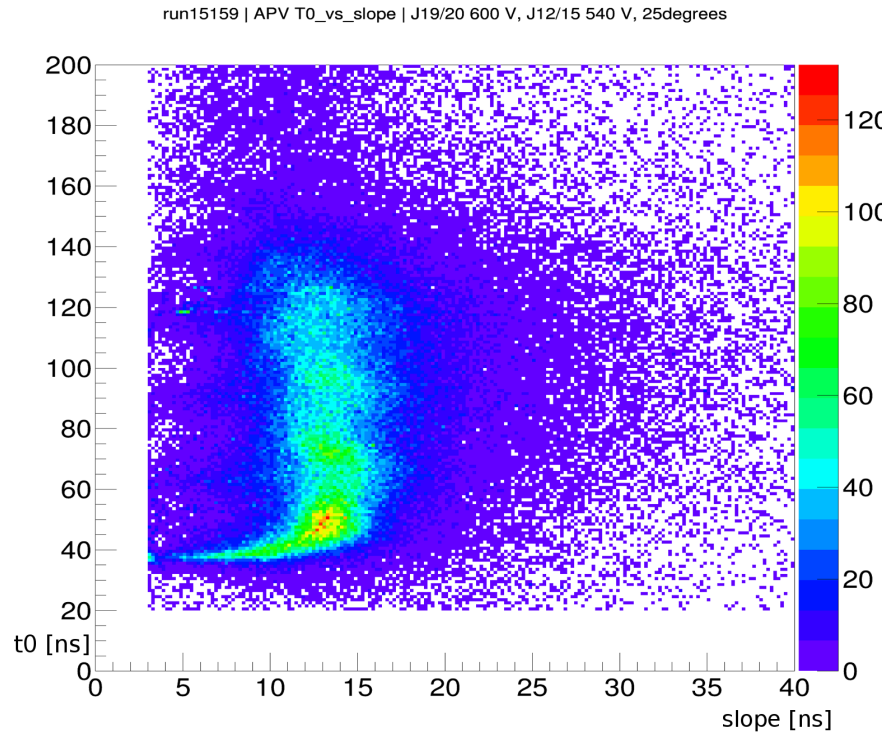


Figure 2.29: As in many cases, it helps to study potential correlations of measured values, in order to use for later corrections in operation. Here we see a dependency of the two quantities for small t_0 values.

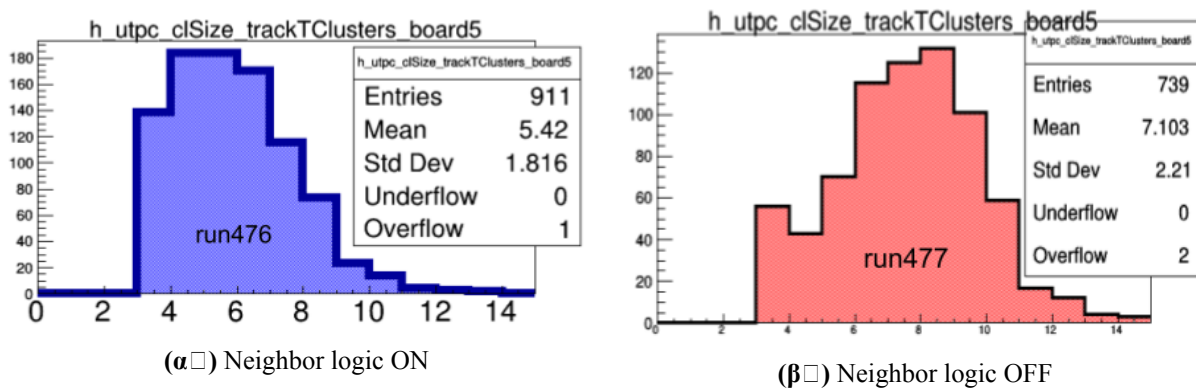


Figure 2.30: Comparison of the cluster size on the SM2 chamber for the different setting of the VMM neighbor logic.

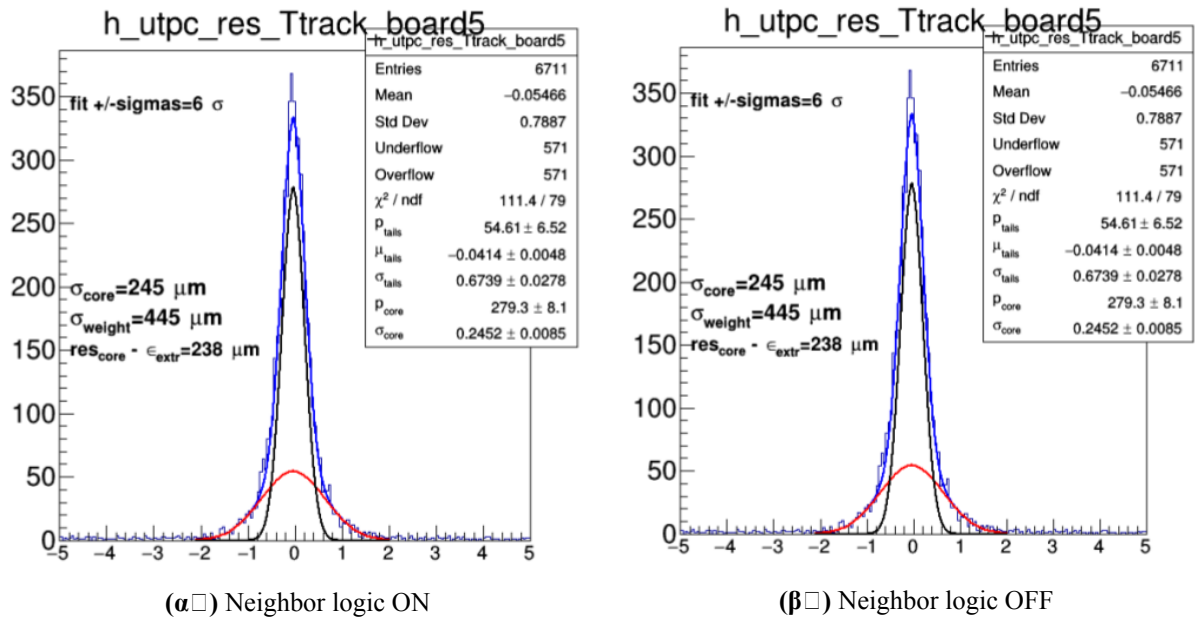


Figure 2.31: Comparison of the resolution on the SM2 chamber for the different setting of the VMM neighbor logic (peaking time 100 ns).

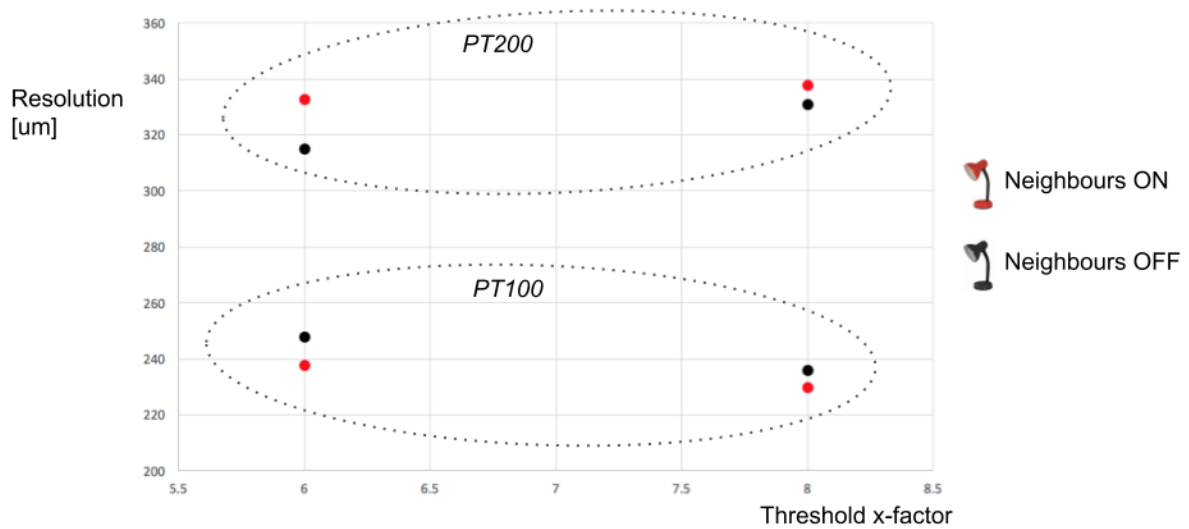


Figure 2.32: Comparison of the resolution on the SM2 chamber for the different setting of the VMM neighbor logic and peaking time.

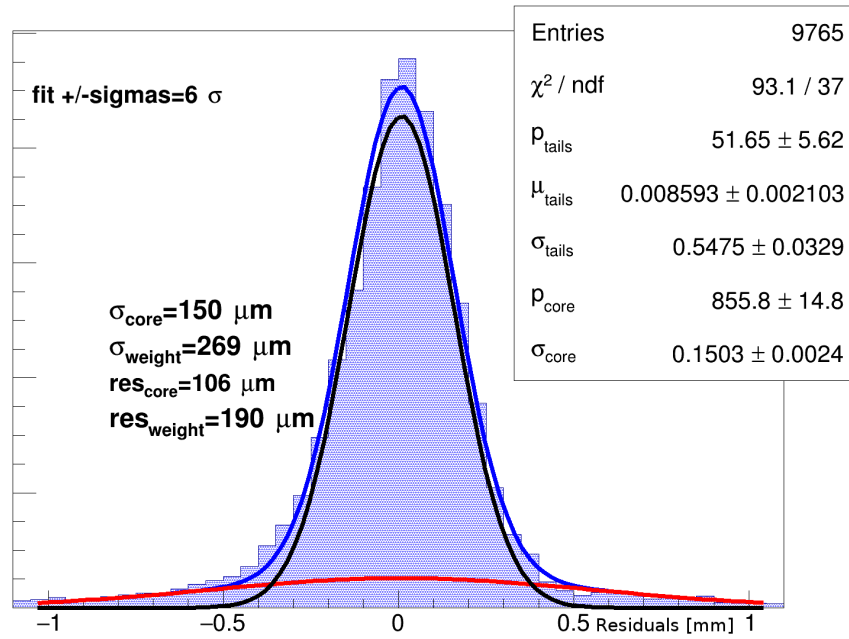


Figure 2.33: Residual distribution for two eta layers of SM2-Mod1, without offset application (run236, summer 2018).

offset is validated at the construction sites with x-ray scans, but we present another way to validate it, post-production.

Thanks to the high rate in the test-beam environment, we are able to take enough data to measure the strip misalignment. We examine normal tracks, and we measure the hits in both eta planes. Normally, in the analysis, we apply offsets to align the coordinate systems of all chambers. However, here we purposely do not apply any offset. Taking the difference in position of the two planes we obtain a usual residual distribution, with the expected sigma which corresponds to the Micromegas resolution. However, the mean of this distribution shows the strip misplacement between the two layers. In two examples, SM1-Mod0 (2016) and SM2-Mod1 (2018), we find this offset to be around 17 μm and 8 μm (see Fig. 2.33), well in the limit of 20 μm .

2.4.10 Cluster heatmap and statistics

The position reconstruction performance is one of the main subjects of optimisation for the MM operation. Since our interpretation of the position is derived from the charge distribution in a cluster, it makes sense to try and further understand this process. For this reason I tried to study the cluster shape size-by-size, and look for internal patterns that can lead to an improved handling of each type of cluster; see Fig. 2.34.

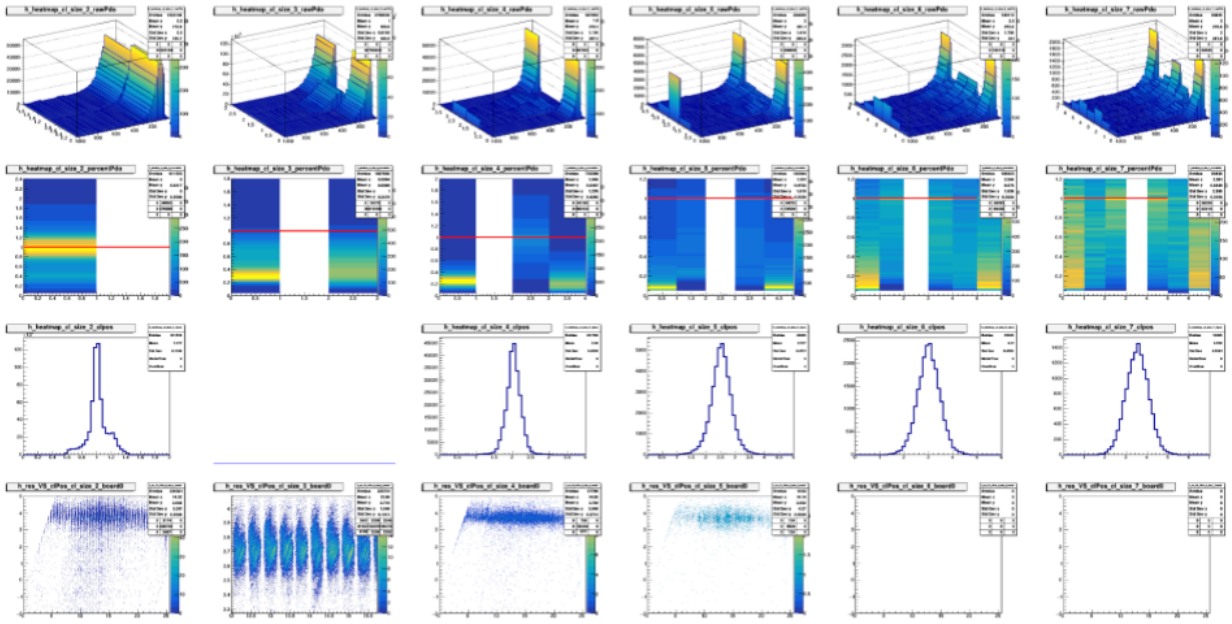


Figure 2.34: Preliminary study of clusters by size. The first column of histograms is for clusters with 2 strips, while the last is for clusters with 7 strips. The first row shows the strip charge distributions of the cluster. The second row shows the relative charge, assuming the middle-most strip as maximum. The third row histogram aggregates the centroid position of all corresponding clusters. Finally the last row shows a 2D histogram with the reconstructed position on the x-axis and the residuals from another chamber on the y-axis.

Some observations from this first attempt:

- for small size clusters, there is a tendency for the left channels to have more consistently low charge, compared to the right ones.
- clusters are generally well balanced (as expected, for normal tracks).
- 2-strip clusters have charges that are more similar than not. This is important especially for cases with neighbor logic on, where smaller side charges can appear, even if below threshold.
- 3 and 4-strip clusters seem well balanced and with normal charge response in all strips. Similar response is assumed from the larger clusters where the middle strips even saturate the ADC, pointing towards a cluster that formed from a larger charge (than a smaller size cluster).
- the position reconstruction looks similar to the MC expectation, and to the one expected from the diffusion parameter. Except for the 2-strip clusters, where there is a clear bias towards the middle of the two strips. This can be explained as positions far from the space between would result in 3-strip clusters. However, based on all other sizes, one would assume that also for two strips there would be similar distribution. This bias is what we try to correct with the eta-correction, mentioned earlier, which didn't prove useful in the end.

Using Monte Carlo simulation we have data showing the expected diffusion of drift electrons, as well

as distribution of charge among the strips. The diffusion is expected to follow a standard deviation of $400 \mu\text{m}/\text{cm}$. As in Fig. 2.35 by Chara Kitsaki, the projected position of the electrons compared to their initial position follows a gaussian distribution. We tried to further understand the charge distribution mechanism, by combining the diffusion parameters with the actual measured clusters. This study however is still in preliminary phase, and hasn't reached final conclusions yet.

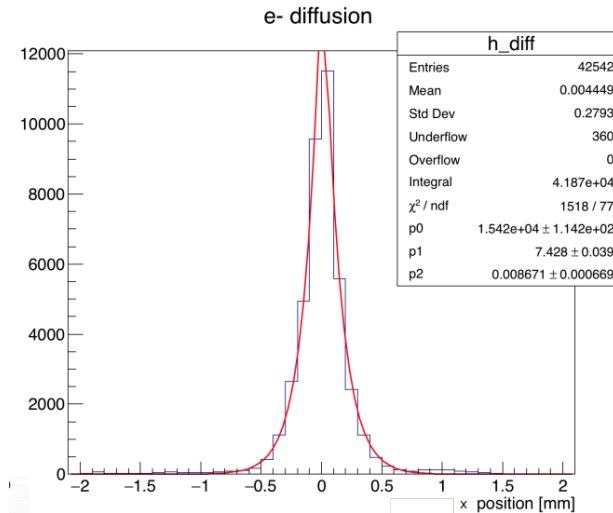


Figure 2.35: Histogram showing the electron position difference after drifting in the MM gap, here fit with an exponential function.

2.4.11 uTPC, cuts and calibration

The results shown above pertain mainly to perpendicular tracks, which have been tested extensively with the small chambers, and as shown, also validated with larger chambers, while meeting the same levels of position reconstruction resolution. However, in the experiment, the detector will mostly have to reconstruct particles on inclined tracks. The reconstruction of inclined tracks is not done with the standard centroid method but rather with a method used in Time Projection Chambers, here called microTPC. The microTPC reconstruction method allows to reconstruct the three dimensional particle position as in a traditional Time Projection Chamber, but within a drift gap of a few millimeters. The main idea is to combine the micro-pattern information which provides the position in one or two dimensions (one for MM) with the timing information of the hits, which can be translated to position in the drift gap.

The algorithm implementation, step-by-step, is described in Appendix B, focusing on the actual steps of the method. However preparation is necessary when first running the algorithm. The main parts before analyzing the data are calibration and definition of errors.

Calibration

The electronics response to the detector signal needs calibration, both for charge and timing response. The steps for calibrating the charge response are described in the DCS chapter, however are not relevant for

the microTPC since the charge information is not used. The timing information, though, is crucial for the microTPC method.

The timing calibration refers to the internal Time to Amplitude Converter (TAC) of the VMM, which produces the TDO output. The TDO corresponds to the fine timing measurement which is relative to the coarse measurement of the relative BCID (relbcid). The relbcid corresponds to the 25 ns clock. The TAC is basically a capacitor that starts ramping as soon as a condition is met (signal peak found or signal threshold crossed). This happens asynchronously, usually between two BC clocks (CKBC). The TAC starts at that time, then arms at the next rising edge of the clock, and finally latches (and stops ramping) on the next falling edge of the clock. This process, also shown in Fig. 2.36, limits the TDO values to a real time range of 12.5 to 37.5 ns.

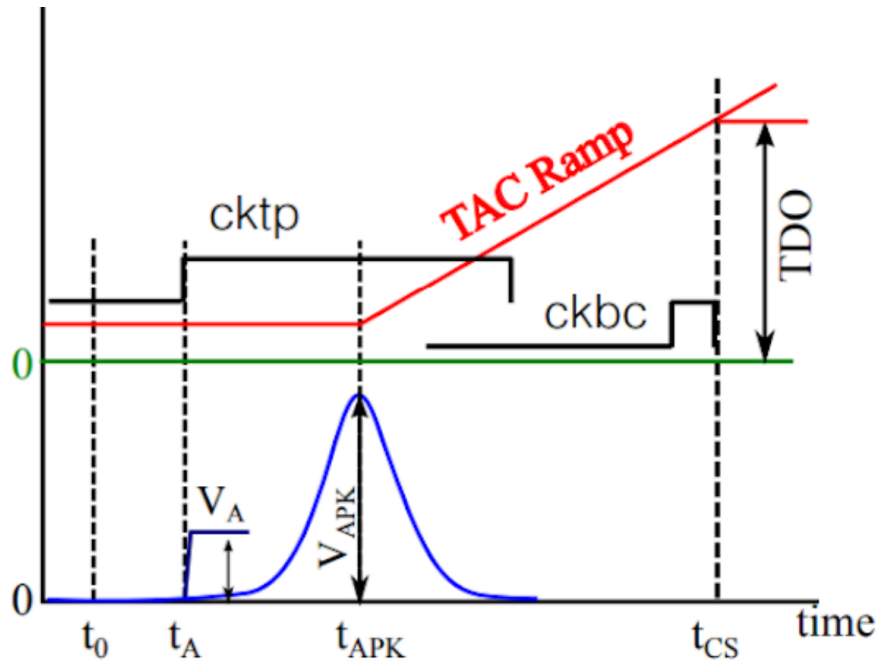


Figure 2.36: The operation of the Time-to-Amplitude Converter (TAC) in the VMM [10].

In order to calibrate this response, the internal pulser is used, which runs on a separate clock, the CKTP. The phase difference between CKTP and CKBC is scanned, in a similar way as in the charge calibration. The TDO is readout each time, knowing the phase difference, and consequently the corresponding time difference in ns. The resulting data is filled in a histogram for each channel of each VMM. An example is shown in Fig. 2.37, along with a set of plots for several channels. These histograms need to be processed to allow proper fitting (simple shift is enough). The reason that the shift is needed is that the VMM registers some hits on the next BCID, but the TDO is still smaller, which means they appear on the lower values of the x-axis. After linear fitting, we have the slope of the TAC, which is measured in counts per ns. This value is configurable in the VMM, to a few discrete values, which actually correspond to the maximum ramp duration. For the microTPC, the one used is 60 ns, the smallest available. In this case, the smallest value is the best choice in order to achieve the best time resolution. The TDO output has a set range of 0 to 256 counts. These counts,

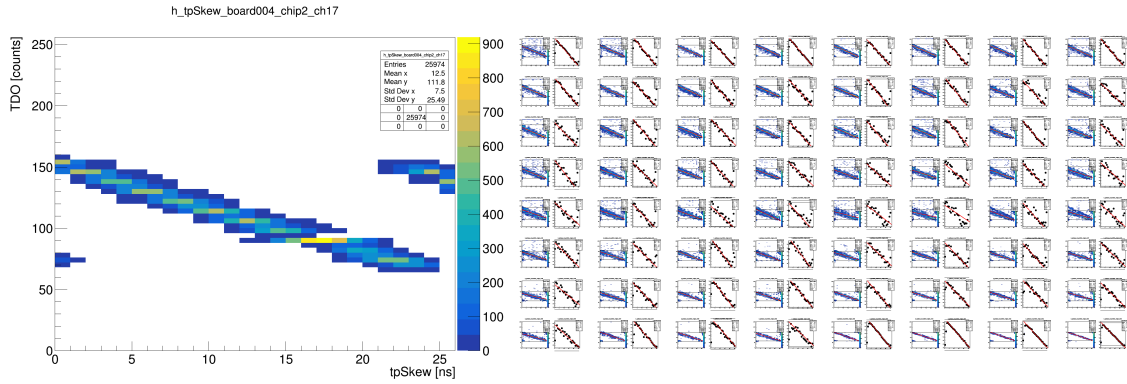


Figure 2.37: TDO-versus-tpSkew distributions for one channel (left) and for an entire chip (right).

are distributed to the ramp duration, i.e. leading to the formula:

$$\text{TAC}_{\text{slope}} = \frac{60 \text{ ns}}{256 \text{ counts}} = 0.23 \text{ ns/count} \quad (2.6)$$

It is obvious that larger TAC duration values lead to worse timing resolution.

After following this procedure for each channel, we study the uniformity of the measured slope along the chip, as in Fig. 2.38. Ideally, the distribution should be uniform, but in this test we didn't use the final electronics. A closer to ideal result is shown in the same figure (from [10]).

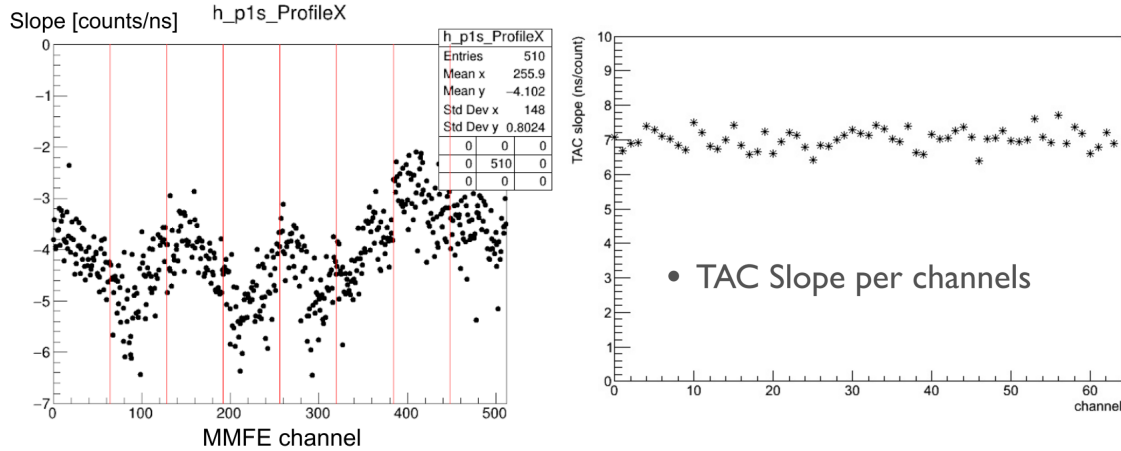


Figure 2.38: Distributions of calculated TAC slopes from the calibration plot fits. LEFT: VMM3; The structure was not understood at the time of this thesis, but seems to be board-wide. RIGHT: VMM1; Clearly there is not structure or oscillation on the values [10].

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Regardless of the quality of the calibration data, it must be used as is to translate the raw data (BCID and TDO) to real time. The formulas used, for each hit is:

$$\text{TDO}_{\text{duration}} = \frac{\text{TDO}_{\text{counts}} - \text{TDO}_{\text{pedestal}}}{\text{TAC}_{\text{slope}}} \quad (2.7)$$

$$\text{strip time} = \text{relbcid} \times 25 - \text{TDO}_{\text{duration}} \quad (2.8)$$

The distributions we get are shown in Fig. 2.39 (both for TDO durations and for strip times). Also in the same

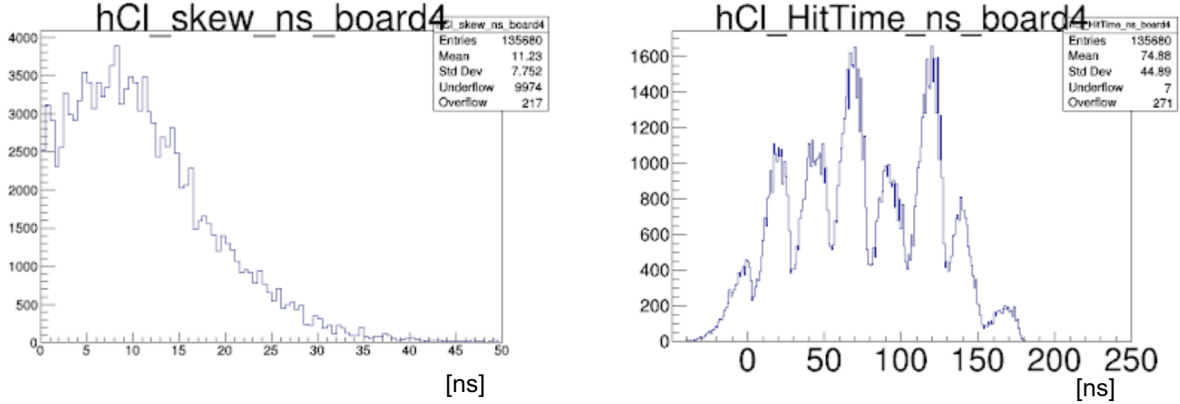


Figure 2.39: TDO skew and total time, as calculated with the real calibration files. The heavy bias on the BCID clock frequency is shown.

figure the first time is shown. This corresponds to the time of the first strip that fired in the cluster.

Due to not having the final electronics, timing calibration data was not as expected. The distributions were as shown in Fig. 2.39; not well distributed and with heavy bias on the BC clock. For this reason we tried an alternative method of calibration that was possible thanks to the large amount of data available from the testbeam: self-calibration. This method consists of scanning the raw TDO data for every VMM channel, and filling it into separate histograms. Then, each histogram is fitted with two Fermi-Dirac functions, as in Fig. 2.40, in order to compute the real range of the particular channel TAC. The minimum and maximum values, defined as the mid-points (inflection points) of the Fermi-Dirac functions, are assumed to be the proper TDO range, measured in counts. This range is then scaled to the range of 12.5 to 37.5 ns, as in the TDO duration above, and this now provides the TAC slope value. The microTPC results shown have been produced using the self-calibration method, after observation of improved results compared to the normal method which produced unphysical results.

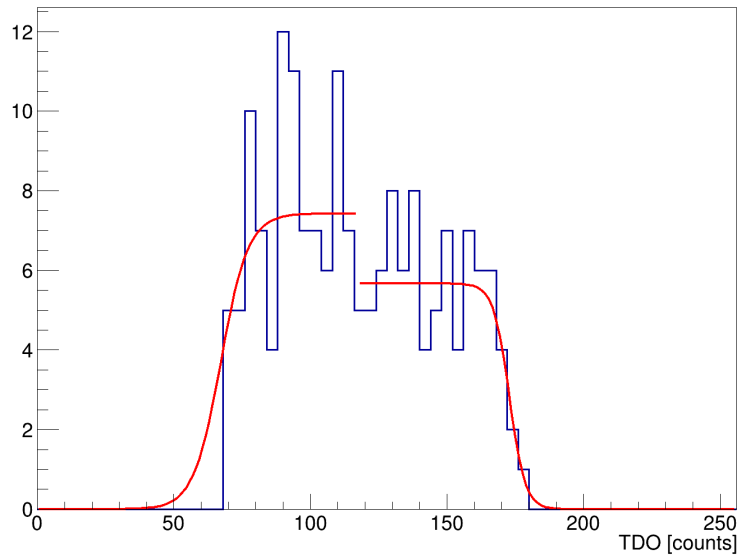


Figure 2.40: A TDO distribution for a single channel, from one run. The edges are fitted with Fermi-Dirac functions, to dynamically and repeatedly find the minima and maxima of the distribution, while ignoring potential noisy values.

Corrections

There were some key cuts applied to the data in order to achieve improved resolution.

- Cut on the first bin of the chi2 probability distribution. This is done to remove the few events where the fit has a very low probability, which means that the fit didn't work properly. The relevant histogram is shown in Fig. 2.41 (left).
- Correction on the relation of resolution with the cluster time. There is a correlation between the two, visible in Fig. 2.41 (middle). Such "alignment" type corrections are hardware-dependent and thus valid to apply, since there is no bias to particular events in the measurement.
- Cut on the cluster time width. It was observed that clusters with small time width (time difference between earliest and latest strip) are reconstructed poorly. This was seen to originate mostly from clusters with three strips. Clusters with very small time width are rejected, because they will naturally reconstruct to a line that is closer to horizontal than the expected 28 degrees of inclination, which would be unphysical. Clearly there needs to be a way of properly processing these clusters, but this was not dealt with yet. See Fig. 2.41 (right) for the relevant distribution and the comparison per cluster.

Results

After applying the mentioned cuts and corrections, we managed to bring the resolution down to the order of 200 μm . Accompanying the position residuals is the angle residuals, peaking at the expected 28 degrees. The relevant results are shown in Fig. 2.42.

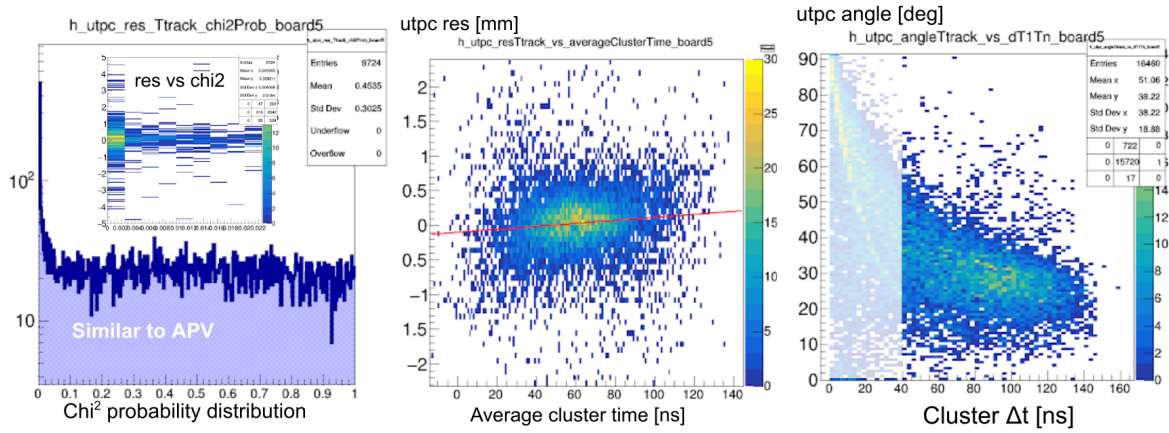


Figure 2.41: Cuts applied on the microTPC analysis.

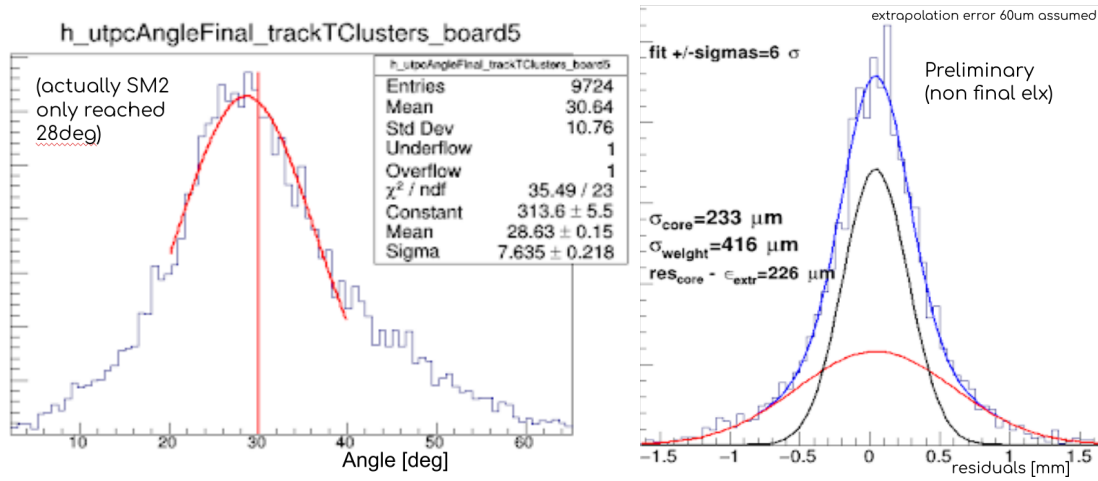


Figure 2.42: The microTPC analysis results for angular and position resolution.

Future improvements

Clearly, compared to results with the small chambers from the past (as in [11]) the microTPC resolution here is not at the level of the design specification. But with the semi-final electronics, on the large MM chamber, these are basically the first results. Moreover, results from a large chamber (SM2) with the legacy APV electronics, which had been used to establish the results, are at the same level. This points to the detector construction parameters, and mainly the capacitance, which seems to not allow better precision on the position reconstruction. Some points with potential for improving the position reconstruction:

- Final version of front-end electronics
- Final version of back-end electronics
- Noise and grounding: In that particular testbeam, there was increased noise measured on the electronics, which led the thresholds in the VMs to be set higher than ideal. This, in turn, led to a loss of measured charge, which has been shown to reduce resolution [10].

- Calibration before data-taking (instead of after). This would have helped to identify problems on the spot, and also avoid the doubt of potential changes in the calibration parameters over time and use of the electronics.
- Identifying method for smaller size clusters and smaller time width clusters, in order to improve performance. The cuts described really cut down the performance of the algorithm, which should be improved by an improved algorithm that takes them into account properly.
- Detector HV performance
- Algorithm modification to adapt to different cluster creation behavior

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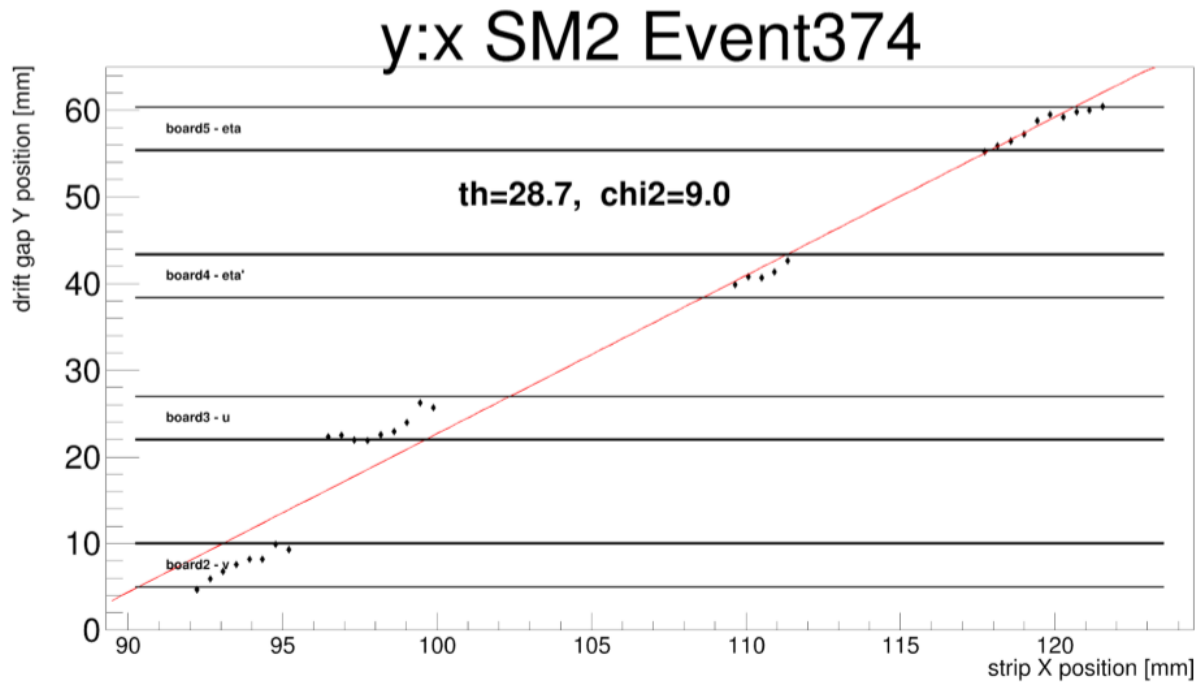


Figure 2.43: SM2 event from H8C in July 2018. The four layers are drawn as horizontal black lines, with the thicker one indicating the location of the readout strips. The y-axis is showing the real scale detector dimensions. For each hit in the event, a diamond is plotted in the corresponding x-axis position, where the strip is in reality. The height within each drift gap is calculated from the uTPC method using the drift time and velocity. The red line is the reconstructed pion track. The u and v layers are offset from the expected position, as expected, due to the strip rotation.

Chapter 3

NSW Services

The NSW, as a physical object, consists of the chambers, which are prepared in the construction sites, and later assembled into (double) wedges in the integration sites, the NJD shielding and spoke supports, which are designed by the ATLAS Design Office, and manufactured by industry, and finally the services, which concerns all the sub-systems required to make the chambers operational. Clearly, in the end, everything is controlled by software.

In this chapter I will outline the services system of the New Small Wheel, to which I contributed significantly with conceptual and technical design as well as coordination. There are two main ways to breakdown the services system: by area, and by sub-system. First, I will briefly go over the system, area-by-area, and then go into details per sub-system. Services coordination, among other things, was led by Agostino Lanza. The very important and challenging task of actually installing the services on the wheel was taken by Konstantinos Iakovidis and a team of technicians. Collaboration with the ATLAS Design Office should also be acknowledged, for their help, cooperation, advice, hosting, and many useful conversations.

3.1 Envelope

3.1.1 NSW envelope

The NSW envelope is defined by ATLAS Technical Coordination (TC). Views of the envelope are shown in Fig. 3.1.. The shape is defined partly by the old Small Wheel shape, and partly by the environment. The main parts of the surrounding are:

- the end-cap toroid (ECT) magnet. This defines the limit on the HO side of the NSW. This area is not very interesting since the NSW limits are exactly at the surface of the large sectors. There is no particular detail relevant for the services.
- the extended barrel calorimeter (LAr and Tile). This defines the limit on the IP side of the NSW. The electronics crates of the calorimeters are protruding up to the Rim area, which is why the NSW Rim is usable for electronics boxes.

- the LAr pipe. On sectors 6 and 7, a pipe brings the liquid argon to the calorimeter. This is mirrored on the NSW envelope.
- the EIL4 TGC chambers, which are installed in the odd-numbered sectors, define the outer radius of the NSW in these areas. In fact they are even moved towards the NSW during operation to cover the dead areas of the detector.
- the BIS78 chambers, which are also a Phase-I upgrade of the ATLAS Muon system. Placed only in the even-numbered sectors, they come extremely close to the NSW, thus pushing the envelope of the wheel almost to the outer surface of its small sectors.

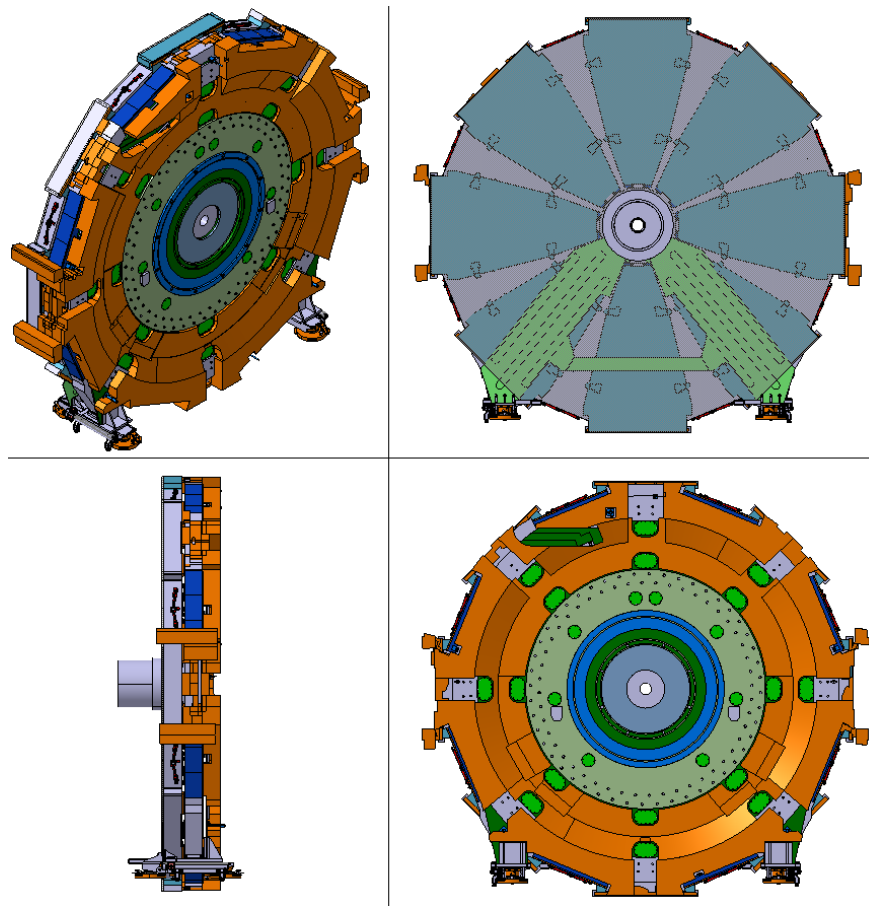


Figure 3.1: NSW envelope. Internal envelopes shown: services (orange), structure (gray), small sectors (blue), large sectors (pale teal), A-plate (light green).

3.1.2 Services envelope

The NSW Services envelope follows the main one, and has often been the reason of its extension. It is shown in Fig. 3.2. The services envelope can be divided in the following parts:

- Rim: The disk that makes up the NSW Rim is almost 560 mm wide (along the radius) and 244 mm thick (along the beam direction). It includes a triangular disk area, between the main Rim area and the

NJD envelope.

- NJD: The envelope here is defined by the LAr calorimeter, and particularly from its electronic boxes. For the top half wheel, this envelope is a simple disk, allowing roughly 50 mm of usable area from the surface of the NJD. For the bottom half, however, the calorimeter electronics positioning require a reduction of the envelope. This particular reduction made the pipe routing on the NJD surface more challenging.
- Brackets: This envelope is also a bit intricate, considering how they protrude from the wheel, in order to reach the flexible chain platform. Moreover, the BIS78 chambers come close to the NSW brackets as well.

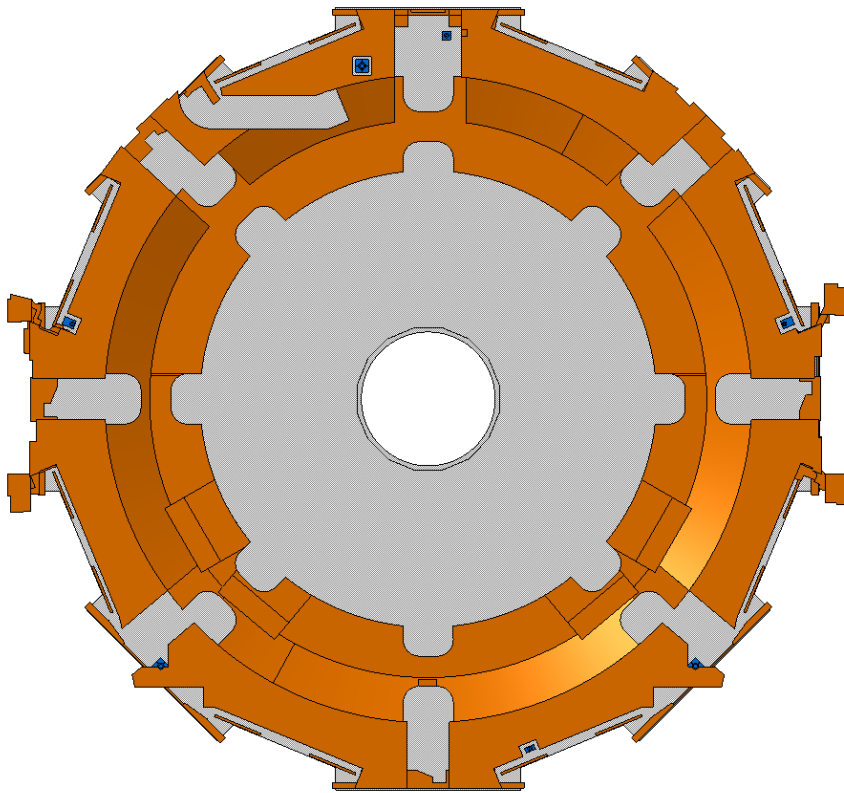


Figure 3.2: NSW services envelope.

3.1.3 Sector envelope

The NSW sector envelope has passed several iterations while the detector design evolved. It is shown in Fig. 3.3. It is a combination of the outer edge of the Micromegas and sTGC wedges, along with their services and mounting components. As already discussed, the upper edge of the small sectors doesn't allow any services or components.

An important part of the access requirements, from the side of TC, is the NSW sector kinematic mounts, which is described later.

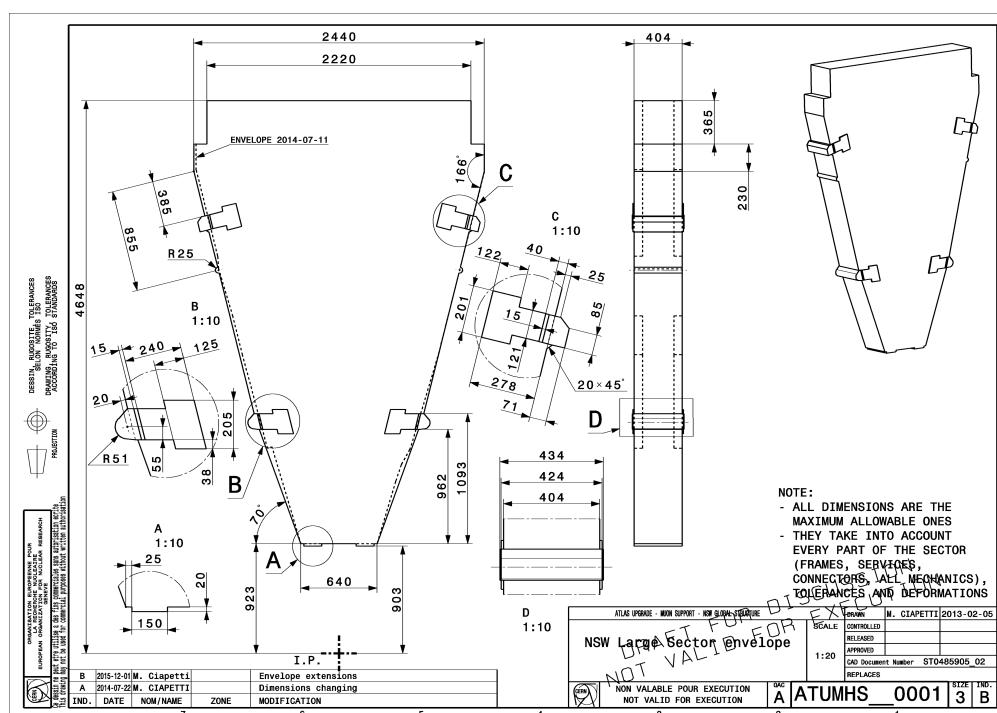


Figure 3.3: NSW large sector envelope drawing from 2013. Some small but important changes have been introduced since then.

3.2 Services by area

The general areas, relevant to the NSW, are the service caverns (USA15, US15), the experimental cavern (UX15) and the wheel itself, which of course is physically located in UX15. It is important to keep in mind that for every two areas or envelopes there is an interface node. These interfaces will be identified as well.

One relevant classification used for routables of the NSW is splitting the types per location. This was the first use of the terms "Type-1" for UX15 routables, "Type-2" for NJD routables, and "Type-3" for on-sector routing. Later, "Type-2.5" was introduced for cables between Rim and sector.

3.2.1 Service caverns

The interface between US(A)15 and UX15 is concrete walls, a few meters thick, acting as radiation protection, allowing experts to freely intervene inside USA15 during beam circulation.

3.2.2 Experimental cavern

The interfaces between the cavern and the wheel are the flexible chains. These can be seen in Fig. 3.4. They consist of many links, which include thin bars acting as separators, allowing cables to comfortably wiggle

when the chain is moved. The reason for the flexible chain is to allow the Small Wheels to move ~7 m from the run position to the parking position, during year-end technical stops (YETS), so that the chambers and electronics can still be operated.

The layout of the flexible chains, with the NSW cables, has passed through several iterations throughout the last years, given uncertainties in the system and optimizations necessary to respect the envelope.

3.2.3 On-wheel

The on-wheel services are clearly split into the sub-locations: brackets, NJD, Rim and on-sector.

Brackets

The brackets are structures, fixed on the NSW spokes, and are a part of the NSW. In UX15, the flexible chains are fixed on the brackets, so that when the wheel moves, it can pull the flexible chain with the bracket, thus avoiding mechanical strain on the routed cables. A bracket on US side is a plate with holes, used as a patch panel to connect on one side the pipes routed on the NJD, and on the other the ones routed in UX15. On USA15 side, the bracket is closer to a cage-like enclosure, giving space for fixation of dedicated patch panels for the corresponding cabled services.

Models of both the old and the new Small Wheel brackets are shown in Figs 3.4, 3.5 and 3.6.

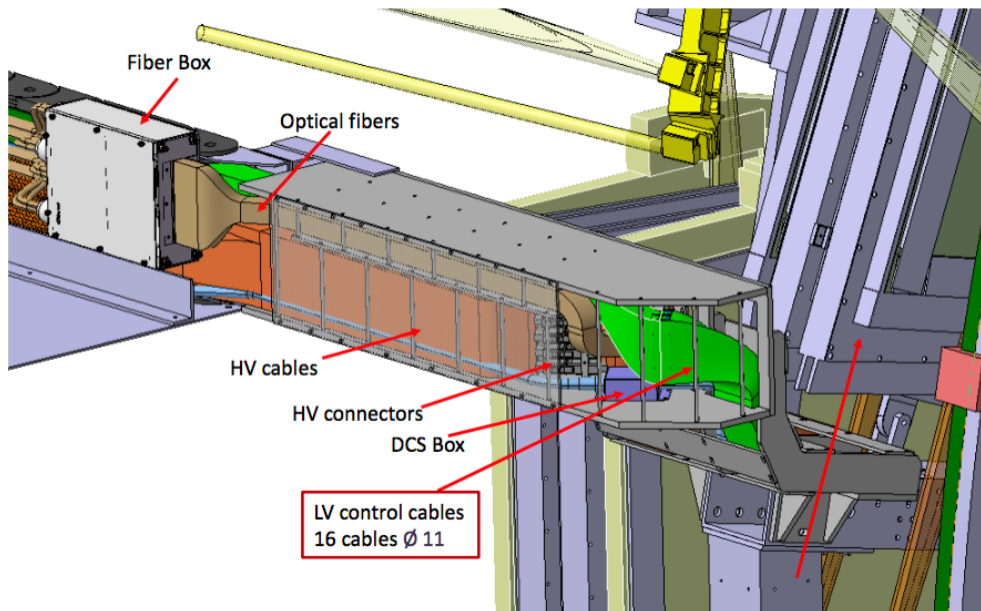


Figure 3.4: NSW top chain arrangement in sector 9.

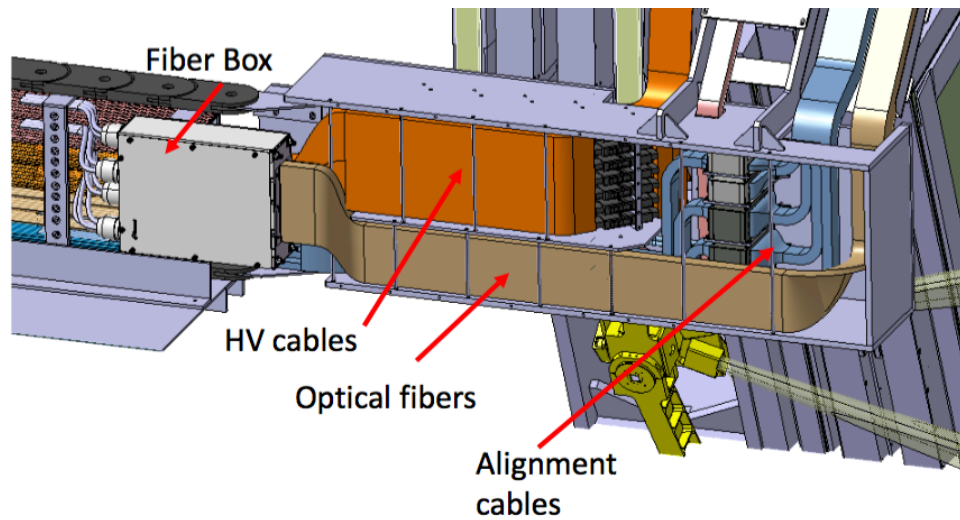


Figure 3.5: NSW bottom chain arrangement in sector 9.

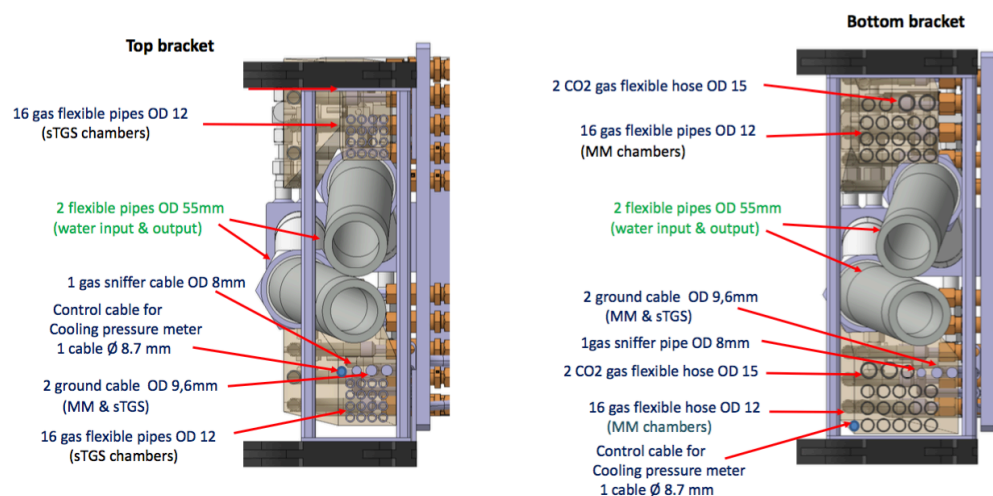


Figure 3.6: NSW chain arrangement in sector 1.

NJD

The NJD (aka nJD or new JD) is the iron shielding disk which holds the spokes supporting the chambers. Most services items are routed from the bracket to the next level box, be it a manifold or a crate, through the NJD. Both IP and HO sides are used for the routing; in principle: cables on HO, pipes on IP.

Cable trays are placed on both sides of the disk, with the idea to follow circular routing. On IP side the trays cover all the area allowed by the envelope. The elliptical covered windows in the middle of the large sector areas are "portholes", allowing access to the alignment bars installed inside the SS spokes. These windows need to be kept uncovered, since access can be required at any time after installation. On HO side the trays go around the disk in three rings, called outer, middle and inner, and also include radial trays which are

also split in inner and outer radius groups. This categorization helped prepare installation documentation to provide to the installation team, which will be detailed in another section.

On HO side, there's only cable routing happening. On IP side, apart from the pipe routing, there are gas manifolds installed, from where even more pipes are routed to the chambers. Initially, all routed services were on HO side, but after common agreement, it was decided to move the pipes on the accessible IP side, since the gas connections and manifolds are usually prone to leaks and connections that deteriorate with time and radiation.

The rim is technically part of the NJD so there is no particular interface, but it is mentioned differently due to the different density.

Rim & access

The "Rim" is the rim of the NJD; namely the outer ~56 cm (radially) of the disk. Many electronics boxes are supported on it, serving as intermediate connections between the "bulkier" connections from the racks and the higher granularity connections on the chamber side. The popularity originates from its accessibility. Especially the large sectors are accessible when the wheels are in run position. Unfortunately, this access is not as simple as walking to a rack and changing a HV board, as is common practice in the Muon system. There are several platforms around the wheel, from which the Rim can be reached by hand, or almost two meters away, in some cases. See Fig. 3.7 for some 3D model views of the access situation.

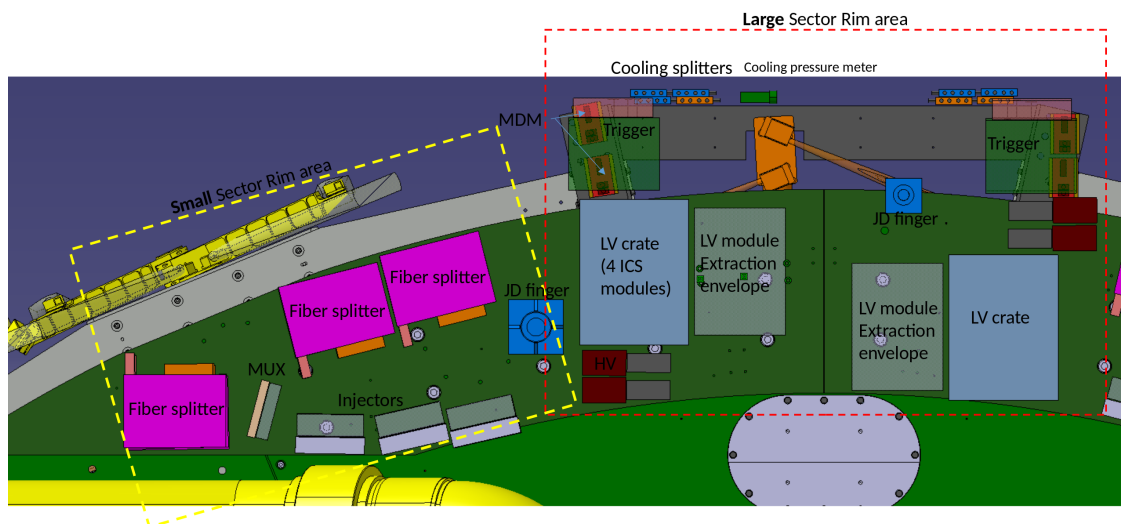


Figure 3.7: NSW Rim boxes 3D arrangement. This is a view of sector 5 and 6 of NSW-C.

Access needs to be maintained and improved for the NSW. This is ensured with the precious help of the Design Office, who shall design additional platforms to enable access to at least all large sectors, as expected. The access requirement is a crucial one for the NSW, given the importance of electronics placed at the Rim. Even for the order of placement on the Rim, the accessibility requirements were compared as a risk mitigation action. Namely, the expected failure rates, chamber granularity loss in case of failure, cooling needs and B-field sensitivity. See Fig. 3.8 for the initial comparison.

ITEM	Has Cooling	RELIABILITY	Rate of Failure	DECREASE OF PERFORMANCE	Failure severity in layers	WEIGHT	MAGNETIC SENSITIVITY	Magnetic sensitivity	ACCESSIBILITY	Accessibility
Trigger box	YES	Not known (no tests done). No redundancy	2	One board failing will kill one layer (Router) or one sector (Pad Trigger)	1	Not known, Could be of the order of 10 kg	Should be quite insensitive	1	Must be the highest possible	4
ICS (MM)	YES	Should be high (if commercial components)	1	One failing channel will kill one layer (for both sTGC and MM)	1	Not known. Order of a few kg	Limited to 1k G, this limit could be increased to 2k G if necessary	2	Very good	3
HV splitters	NO	Very high (passive components)	0	One failing channel should compromise some regions of a layer	0.5	Order of 1 kg	Not sensitive	0	Not necessarily good	2
LV splitter (sTGC)	NO?	Very high (passive)	0	At the level of single FE boards	0.1	Order of 1 kg	Not sensitive	0	Poor	1
Fiber splitters	NO	Very high	0	Should be a small part of a layer	0.5	Order of some hundreds grams	Not sensitive	0	Poor	1
ELMB	NO	Quite high	1	T and B sensors affected	1	Order of 1 kg	Should be 1k G (to be verified)	2	Good	3
Gas splitters	NO	High	0	-	-	Order of 1 kg	Not sensitive	0	Poor	1
Alignment mux	NO	High	1	Alignment affected	1	Order of 1 kg	I don't know	1	Not necessary	0
Alignment injector	NO	High	1	Alignment affected	1	Order of 1 kg	I don't know	1	Not necessary	0

Figure 3.8: NSW Rim boxes accessibility requirement study summary. Black font indicates known or defined information. Red font indicates estimate. The scale used is arbitrary, simply to compare the boxes in terms of expected failure rate, failure severity in terms of detector functionality (in units of sector) and sensitivity to magnetic field. The last column is the resulting order of accessibility, which reflects the positioning on the wheel.

For the ICS LV modules the **B-field** was an important parameter, which will define their performance during operation. For this reason we needed a B-field map of the Rim. With simulation data from the Opera software, provided by JINR, a color map was prepared, to indicate the allowed positions for the ICS boxes, which were specified to operate up to 0.5T (5kGauss) with at least 80 % efficiency. See Fig. 3.9 for the color map. More recently a Qt and Root application was created for enhanced and independent views of the B-field in the NSW area. See Appendix D.

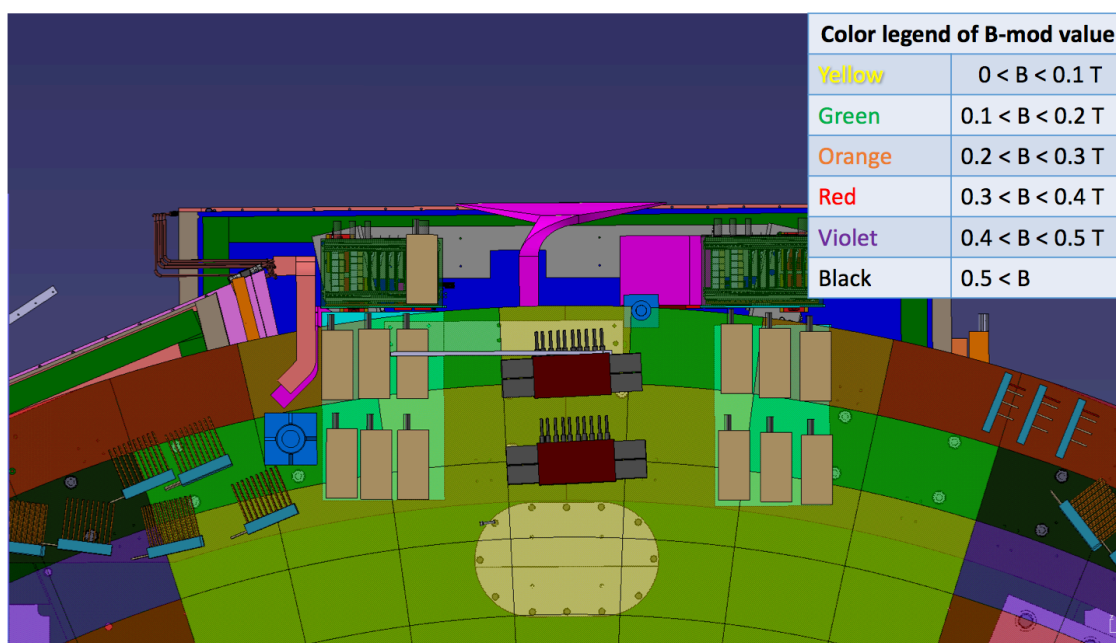


Figure 3.9: NSW-C sector 5 and 6 Rim B-field map, in a preliminary study. The important part was to identify areas with more than 0.5T, in order to appropriately place the LV power supplies, to avoid performance degradation.

An important milestone was the removal of the **"Magnetic flux return ring"**, which is installed on the current Small Wheel. This is a series of iron plates, fixed on the Rim, which were initially installed to act as a shield for the Calorimeter electronics against the end-cap toroid field. After re-iterating with the corresponding groups, it was decided that this element would not be required for the NSW. This was a great relief for the services design, due to the extreme space restriction it was introducing. However, even with this removal, there were always more things to add to the Rim, while we were always trying to shuffle boxes and find space.

This is how the two contradictory phrases came to be: *"There is always space"* and *"There is no space"*.

The interfaces between the Rim and the sectors are mainly the spokes and trays installed on them.

On-sector

The NSW sectors consist of the Spacer Frame, which is the main support structure of the sector, two Micromegas wedges, and two sTGC wedges. Services are distributed among all of them. The Spacer Frame was designed by Hansdieter Schweiger, while the sTGC wedge services have been designed principally by Weizmann. The MM services design was a responsibility of the NTUA team, however several changes have been done during implementation at the integration site (BB5).

The **Spacer Frame** includes only MM services. Namely gas pipes and twinax cables. In Fig. 3.10 the spacer frame is shown, along with some cross sections for the pipe routing. The twinax cable system is described later.

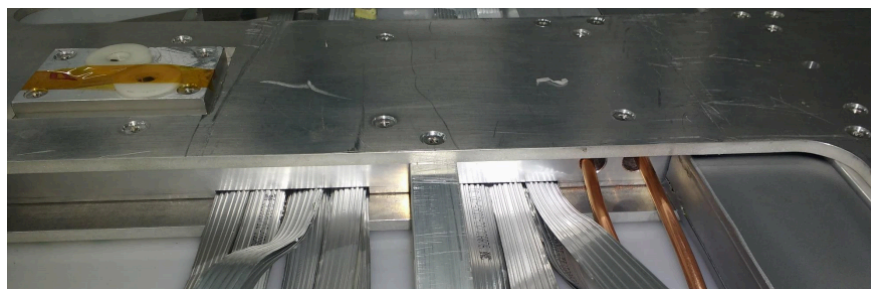


Figure 3.10: NSW spacer frame central bar with the cutouts for twinax crossing and pipe routing.

The **MM wedge** construction allows for some space next to the cooling bars, which is used for routing cables. On one side of the wedge there are four layers of eight MMFE8 boards, along with four pairs of L1DDC-ADDC boards, one per layer. These cards are spread over the eight PCBs. In Fig. 3.11 the card layout is shown. In Fig. 3.12 the cable cross-section evolution along the wedge is shown. There are also Low Voltage Distribution Boards (LVDB) which act as splitters for the incoming cables from the ICS.

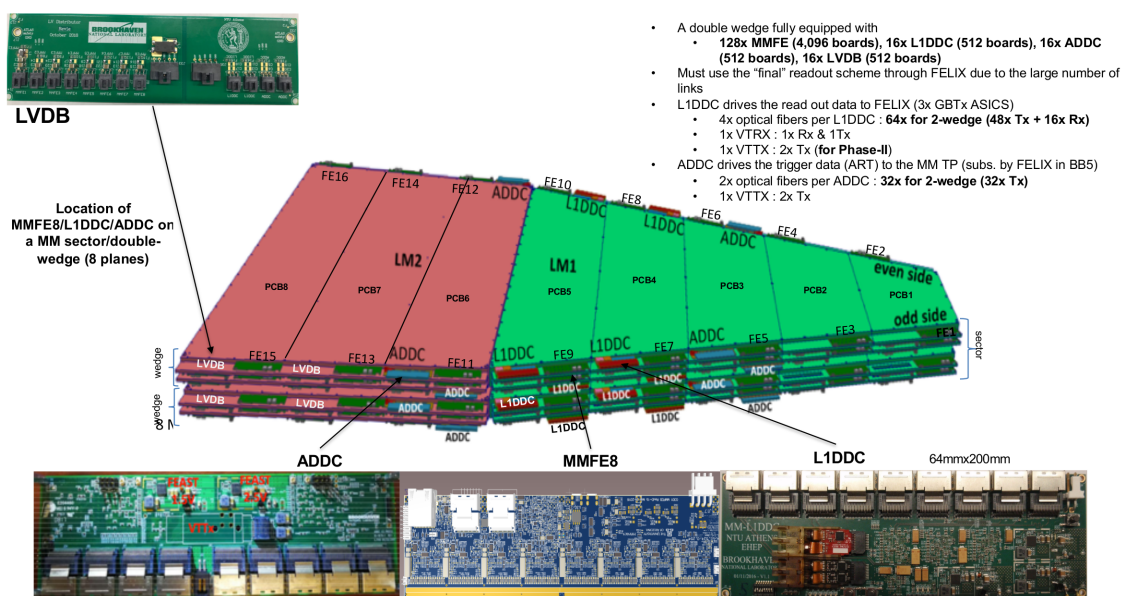


Figure 3.11: NSW Micromegas double wedge, showing the locations of electronics cards. Below are shown the pictures of early prototypes of the boards. On the top left the LVDB is shown [16]

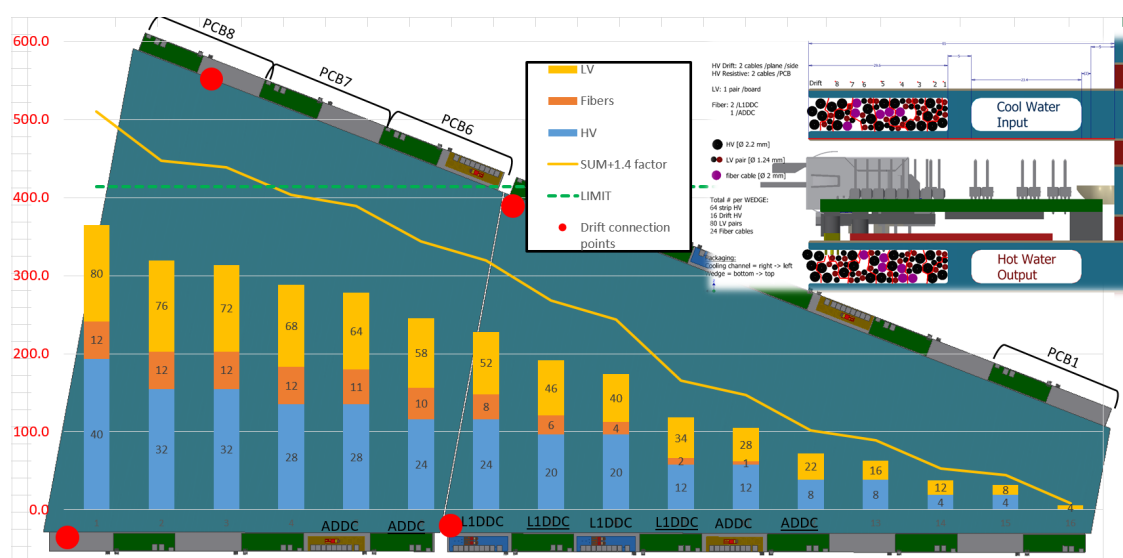


Figure 3.12: NSW Micromegas wedge, with a graph showing the distribution of cabling along its side.

925 The area between **xM1** and **xM2** is also slightly particular, given the protruding cooling connections and the envelope limitations. A study was done to identify potential restrictions on cable selection and bending radii; example shown in Fig. 3.13.



Figure 3.13: NSW Micromegas mockup of SM1 and SM2 in 2016 during an effort to emulate the final routed services, which at the time were out of defined envelopes.

Another study done was for the **access of the Kinematic mounts (KM)** of the sector. There are three mounts on each sector, while there are a few different types of KM. Most of the KM need to be adjusted during sector

930 installation, in order to align the sectors with respect to each other and their nominal positions. Mechanical deformations are the main origin of such misalignments. The KM adjustment is done using a 'cric' tooling - jack. This tool needs to enter from the outer radius, between the spoke and the sector, to be attached to the KM using a pin, and then to be operated with a special wrench key from the outer radius. The tool and a KM are shown in Fig. 3.14 The services exiting the sector need to bend and cross over the KM to be routed towards the Rim. The first step of this routing, however, can obstruct the insertion of the cric tool. In Fig. 935 3.15 some screen-shots are shown from the indicated routing to allow usage of the tool.

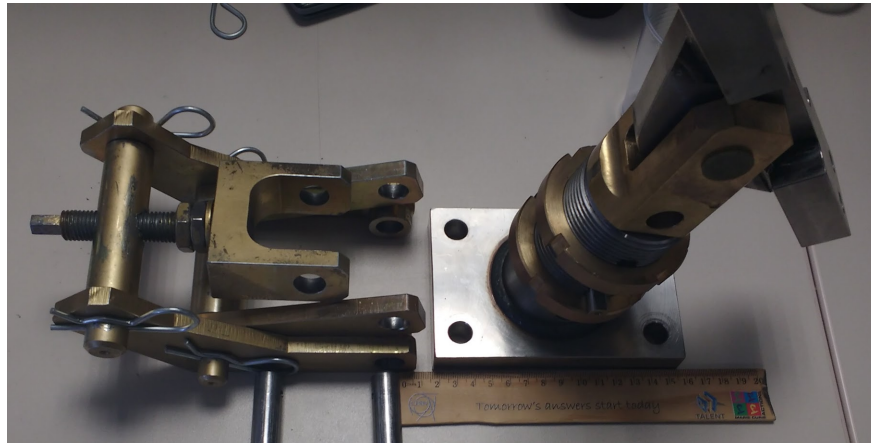


Figure 3.14: NSW sector kinematic mount with the adjusting tool.

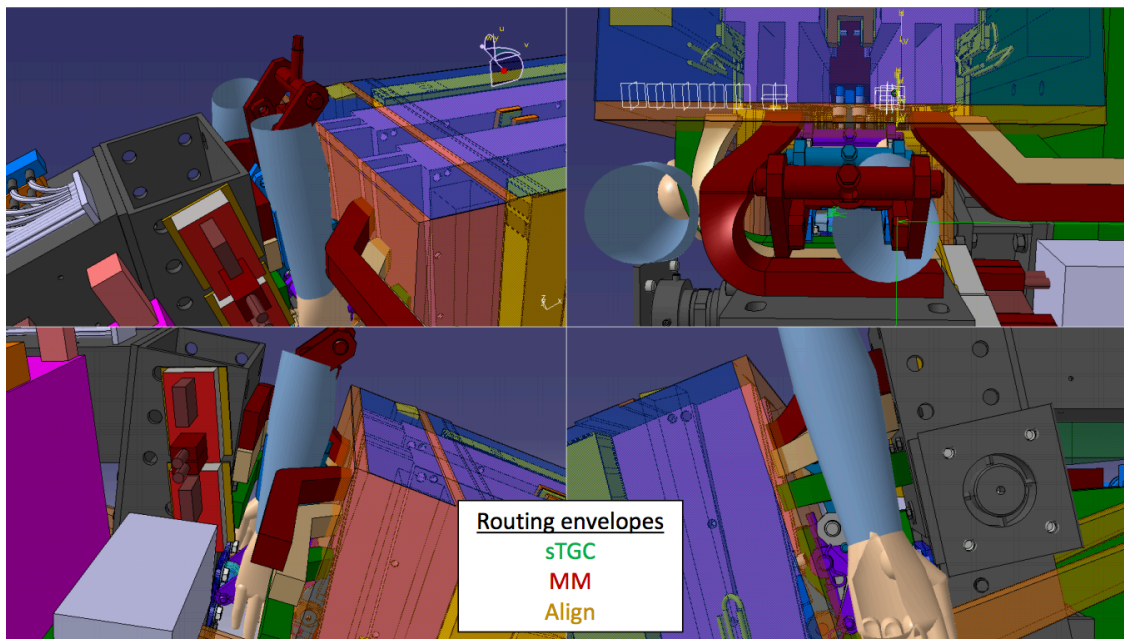


Figure 3.15: NSW 3D model, with the KM and cric tool, along with simulated human to understand the access difficulties and how they affect the services paths.

3.3 Gas

For the Gas system, NTU Athens did the main design for Micromegas. The gas used is Ar:CO₂ (93:7), as a baseline, for MM, and n-pentane:CO₂ (45:55) for sTGC. Important details for the sTGC gas is that it is flammable. This introduces clearly restriction on its use.

A channel always consists of two pipes, the supply and the return.

The gas is delivered by a company into big dewars on surface. There are dedicated mixers and pressure regulators for each type, which are operated by ATLAS Gas group. From there, the gas is supplied to racks, which sit in UX15, US-side, level 4 (for the small wheel). Then, the supply is split into channels and copper pipes are routed to the flexible chain, where they connect to flexible metallic pipes, which finally connect to the bracket. The NSW responsibility starts here.

3.3.1 Micromegas

A single NSW has 16 gas channels for MM. The number can be translated to one per sector, but technically it's not correct, since one channel feeds two wedges from different sectors; two consecutive, same-type sectors. A complete scheme of a single channel is shown in Fig. 3.16. The copper pipes on the NJD start from the bracket and are routed around the disk to reach the manifolds. Each channel reaches the input and output manifolds which are placed on top of each other. The manifolds are 1-to-4, which allows one pipe to feed two corners of two wedges (both small or both large). The same applies for the return. From the manifolds, the so-called secondary pipes are routed radially outwards, between the rim boxes and are then bended towards the sectors where they will be connected with fittings.

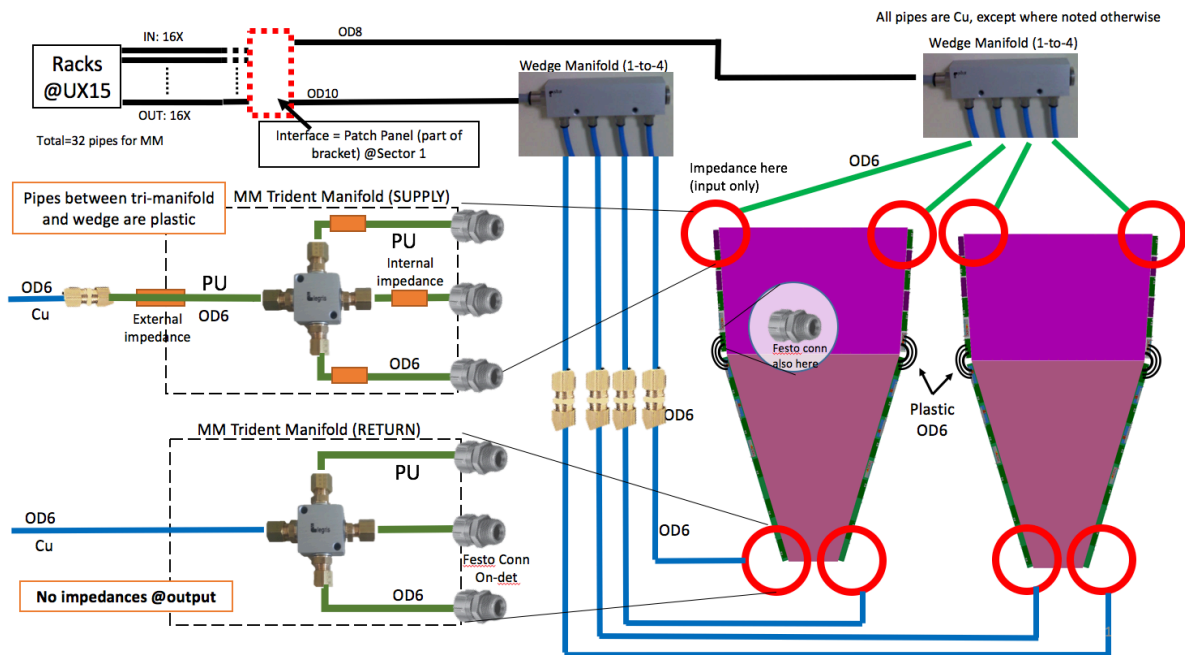


Figure 3.16: A Micromegas gas channel, as split in two consecutive wedges of same type sector.

On the spacer frame there are smaller 1-to-3 manifolds installed, which split the incoming secondary pipe to three plastic pipes. The MM modules are built in such a way to expect three gas pipes; one for each outer drift panel and one for the middle double drift, which is then internally distributed to the middle gas gaps with an internal splitter. Simple plastic tubes are used to join in series the same three connections between xM1 and xM2. The main return pipes are a bit larger to reduce the impedance after the chambers.

Hardware

The material used for the MM system is noted here.

- Main and secondary pipes are medical grade copper pipes, from Siso. A sample was initially also tested in a CERN lab (TE-VSC-SCC), chemically but also with a spectrometry (FTIR) method. Thus it was ensured that there were no contaminating substances such as grease, other hydrocarbons or silicon.
- Plastic pipes are made of polyurethane (PUN) which is considered radiation resistant and is already in use in ATLAS; from Festo.
- Wedge manifolds are machined aluminum blocks, from Legris.
- Trident (1-to-3) manifolds are similar but smaller pieces, from the same company.
- Fittings are brass, delivered with some type of NBR plastic o-ring, from Legris.
- O-rings turned out to be a complicated task, due to the plurality of opinions on appropriate rad-hard materials with various experts. Materials considered were NBR, FKM (Viton) and the final choice: EPDM, which is also used in the current ATLAS MDT o-rings. It was also time-consuming to manage to produce them in industry. Contrary to the MDT, where the o-ring consists only of plastic - EPDM, for the MM fittings we used bonded seals, which is a flat steel o-ring with a radially internal plastic component. In the end, Eastern Seals UK produced the rings in a custom production.

Flow requirements and rack upgrade

The baseline gas strategy for operation for ATLAS Micromegas was defined to be four renewals per day. The total MM gas volume of both wheels is 6m^3 . This translates to 24m^3 per day, or 1000 litres per hour. In addition, the option to add a few ppm of water in the mix was considered, in order to potentially improve the spark behaviour.

The current CSC gas system is going to be repurposed for the MM. However, given the flow requirements of the MM, the CSC rack needed modification, which will be done by ATLAS Gas group. The rack modification and comparison can be found on EDMS page (document [1828606](#)).

3.3.2 sTGC

A single NSW has 16 channels for sTGC. The number can be translated to one per sector, but the actual distribution is more complicated. In order to maintain redundancy, the sTGC follow a similar split to the MM, spreading the channel among more than one sector. One gas channel is split among eight sectors,

feeding a single layer from each sector. This scheme provides extremely high redundancy, but at the cost of routing complexity.

Hardware

The sTGC only have wedge manifolds, which are 1-to-8. The connections are equipped with flow restrictors to balance the different sizes and pipe lengths. The manifolds are machined aluminum pieces. The o-rings are metallic and are fixed on the manifolds after proper surface polishing to ensure good leakless contact, which is then validated by spraying the connections with foam and waiting for bubbles to appear.

Flow requirements and rack upgrade

The sTGC system gas volume sums up to 3m^3 . Similar gas renewals per day to the MM were decided, bringing the required flow to about 640 litres per hour.

The sTGC will reuse the TGC rack, which currently feeds the SW TGC and the EIL4 chambers. The main modification required is to add flow sensors and regulators, to increase the channels. The current SW MDT pipes will be used for the sTGC. The EIL4 chambers will still operate, so the upgraded rack shall be able to keep serving them.

CO₂ distribution

The sTGC operational gas is flammable. This is an important detail, which necessitates extra safety measures. The sTGC wedges include an enclosure, called CO₂-envelope, which surrounds the edges of the detector. This gas volume is flushed with CO₂, so that a potential leak of flammable gas will first be detected in the return of this volume.

The connectivity scheme for the CO₂ envelope is very simple. All sectors of half a wheel are connected in series as one channel.

3.4 Cooling

For the cooling sub-system, simulations and component design was done by Freiburg University.

The NSW cooling system consists of two channels, retaining the external scheme of the current SW. However, most infrastructure must be renewed.

3.4.1 Cooling stations

The current Muon cooling stations serve mostly muon chambers and racks, along with some other equipment. However, by introducing the NSW in the system, the power requirements greatly increase (see section "Low Voltage"), and along with them the heat dissipation as well. Taking into account the efficiencies of power

supplies and heat losses from all electronics on the wheels, the total power to be removed with the cooling water is 65kW per wheel. See more details on the requirements document [1703449](#) on EDMS.

Surface cooling plant

For the purpose of commissioning the wheel, we will need to operate the detector on surface, before transporting to the UX15 cavern and connecting to the final services. This operation will happen in building 191. Since it is not possible to recreate the entire infrastructure, it was decided to be prepare enough to operate up to two sectors at a time. Among other services to be prepared, one was cooling, for which a small cooling plant was prepared by ATLAS Cooling group in collaboration with EN-CV. The requirements defined were:

- The expected power consumption is 9.5kW, with margins included.
- Supply of water at 17° C with a flux of 1.4 m³/hour at a pressure of at least 3 bar absolute.
- Return temperature would be approximately 23° C.
- Pump to drive the closed circuit
- Vacuum pump with a vessel to run the system in “leak-less” mode.
- Two manual regulation valves, one in the supply line and one in the return line.
- Flow meter.
- Two manometers to monitor the absolute pressure at the supply and return of the circuit.

After the station was prepared and commissioned, it was installed in b191, and until the commissioning activities start we can monitor its operation; example shown in Fig. 3.17.

3.4.2 Distribution

The NSW will also use two channels from the upgraded cooling station, but with slightly larger diameters to allow higher flow. The pipes in the flexible chain will be rearranged from the current situation - both channels in bottom chain - to have a symmetric routing for the top and bottom half of the wheel.

Each channel is split in 20 sub-channels. There is one sub-channel for each detector technology per sector, plus an additional sub-channel per large sector to cool the rim electronics. Ergo the 16+4 sub-channels per half wheel. See in Fig. 3.18 the bracket splitters. They are equipped with flow regulators for supply and return of each sub-channel, but also a pressure sensor for the channel return. Before operation they will need to be adjusted to equalize the flow in all sub-channels.

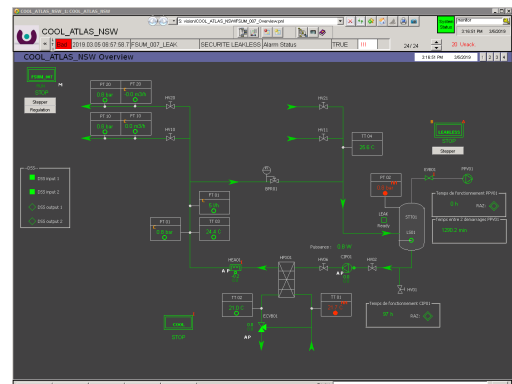


Figure 3.17: The NSW surface cooling plant monitoring panel

A rim sub-channel is routed on the NJD reaching the lower radius of the rim, where the first connection is made. The boxes are connected in series (two LV ICS crates and two sTGC Trigger crate).

A detector sub-channel arrived on top of the small sector spokes, where the cooling manifolds are fixed. These manifolds, 1-to-4, feed two sides from adjacent sectors, one large and one small, see Fig. 3.18. Each wedge has one cooling channel along its side, which leads to the total number of four channels for this area. The return follows the same scheme.

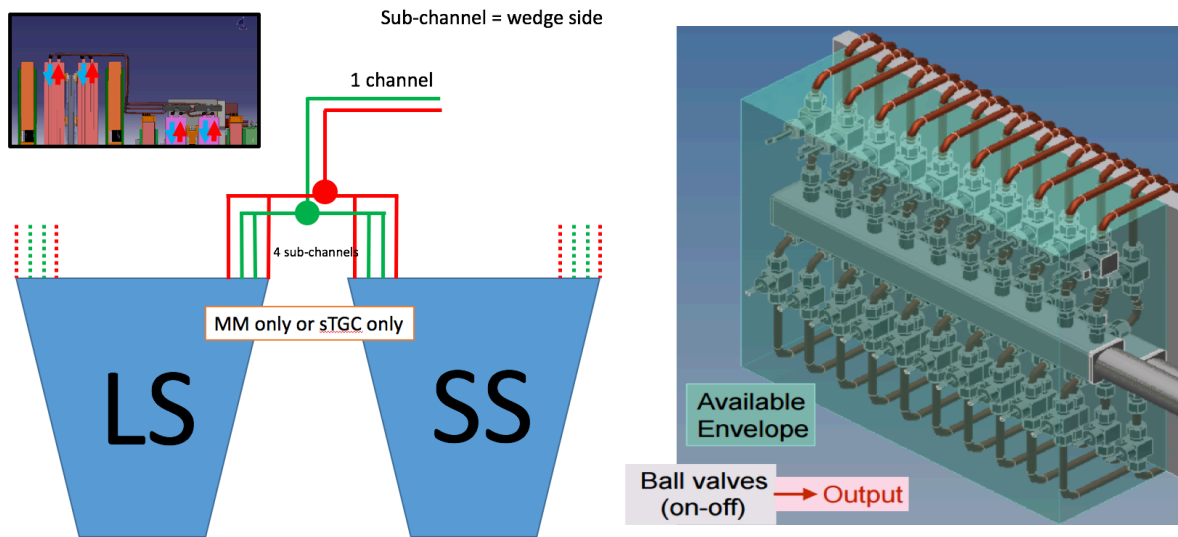


Figure 3.18: Distribution scheme of a single cooling sub-channel (left); cooling manifold design (right).

Accessibility is an important feature in general, but even more so for the cooling system. Even with a leak-less system, loss of a cooling channel is a big part of the detector, and a bad connection can appear at any time. An example from current operations is the CSC detector who, in the end of Run 2, have had a cooling issue with a few sectors, which was not certainly a leak, but could also be a connector jamming due to bad connection or simply obstructed by some residue. Similar difficulties with leaks have been experienced in the Tile Calorimeter community, with several occasions of needing people to squeeze through impossibly small holes to reach and fix a bad connection. The lesson learned is that cooling connections should be as accessible as the most important electronics. This is why the manifolds are placed in the edges of the small sector spokes, in the large spoke area, where accessibility is best, even in run position.

Pressure sensors

The cooling system is working in under-pressure, in order to avoid spills in case of leak; thus it is a leak-less system that takes in air instead of losing water. But we also need to make sure that there is enough pressure to avoid creating vacuum at the top of the wheel. For this reason we will also employ a pressure sensor in sector 5.

The total number of sensors is three per wheel; one on each bracket in sector 1, and one on top of sector

5. The sensor cables are routed through the flexible chain and then towards USA15 level 2, to the cooling racks, to allow monitoring.

3.5 High Voltage

The power systems were mainly defined by INFN and Freiburg.

1080 The high voltage system for the NSW is also demanding in terms of numbers of channels and cables. It consists of primary 48V generators, which provide the service voltage and power to the HV boards, the mainframes, acting as the communication hub, and lastly branch controllers, power factor correctors, and crates for the boards. The cable assembly scheme is shown in Fig. 3.19.

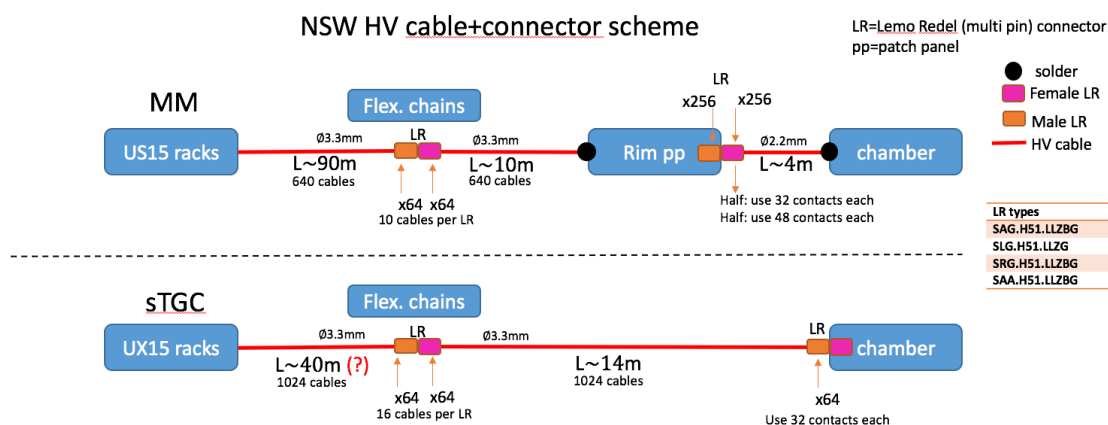


Figure 3.19: The NSW HV bundles definition, showing the numbers and connections of the HV system.

3.5.1 Micromegas

1085 The Micromegas detector requires two different voltages to operate, as already explained; the Resistive one for the amplification gap, and the Drift one for the drift gap.

- Resistive: A Micromegas layer consists of eight PCBs, each of which can have its own HV line. That would lead to an enormous amount of independent channels, which is impractical to apply. Therefore, the layers are instead split in two; the xM1 and xM2 modules' layer equivalent. This means that a wedge has two channels per layer, or 16 in total.
- Drift: The drift voltage is generally not prone to stability issues, contrary to the resistive one. For this reason it is acceptable to group more layers together. Namely, the grouping is per quadruplet, which means there are two drift channels per MM wedge.

1095 The channels mentioned are independently controllable channels. This corresponds to the cables from the HV boards to the splitter on the rim. In total, there are 512 Resistive and 128 Drift HV channels for MM.

HV splitter

The MM HV splitter is necessary to multiplex the many PCB connections to the incoming channels. A prototype of the splitter is shown in Fig. 3.20, along with a schematic in Fig. 3.21.

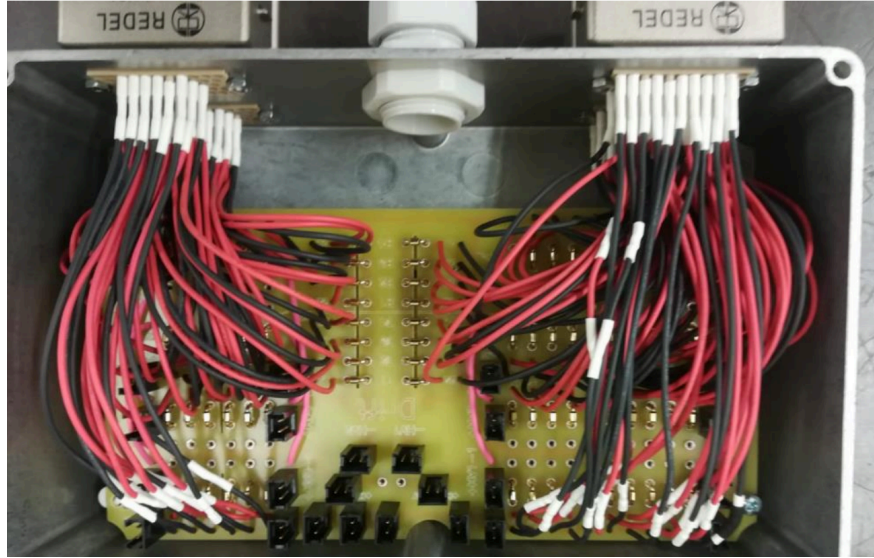


Figure 3.20: The MM HV splitter prototype.

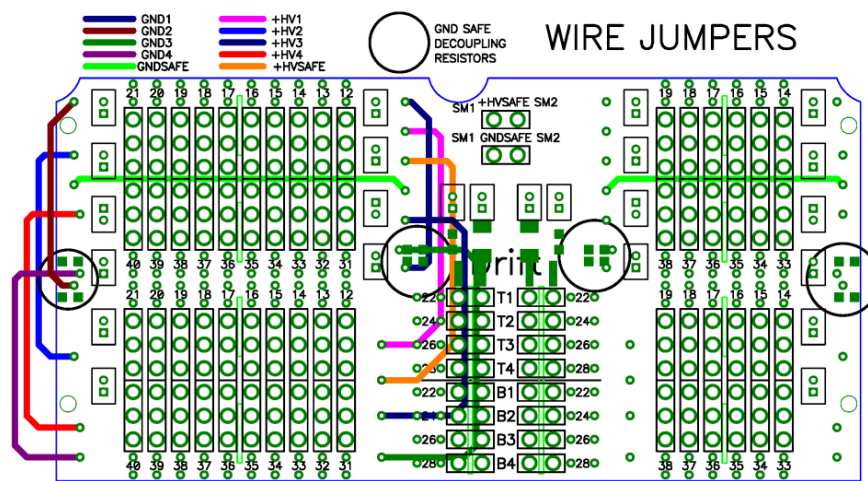


Figure 3.21: The MM HV splitter close-to-final schematic, showing the necessary connection for the spare line, along with all the jumpers for each PCB connection.

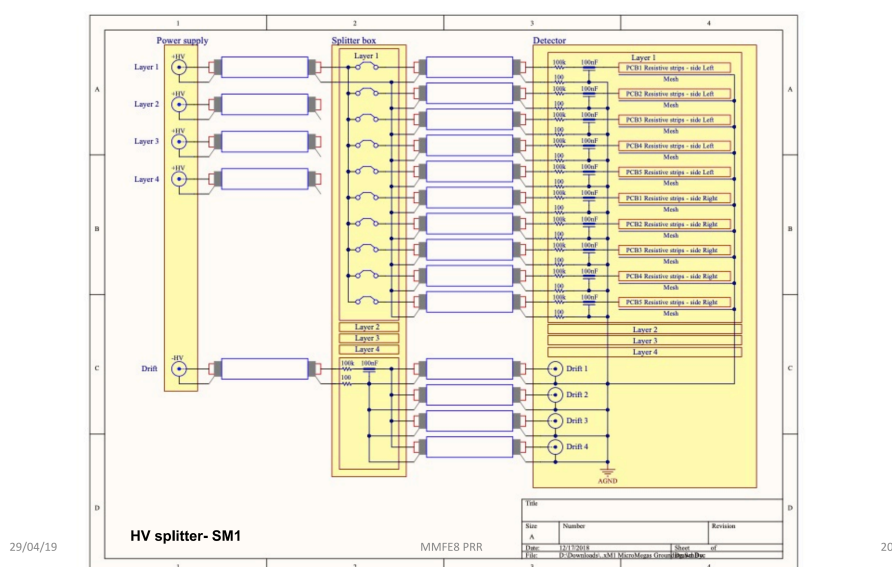


Figure 3.22: The MM HV splitter connectivity scheme, between the HV power supplies and the detector.

Due to the MM HV stability issues, it was suggested to use the routed spare channel as a "hospital line", to allow grouping pathological sectors that cannot operate to the optimal operational voltage. Even more radical designs were suggested, such as grouping arbitrary sections together to achieve the absolute optimal voltage for each section. However this would imply completely changing the design and enclosure of the already procured HV splitters, which is why this is for now rejected. Later in the commissioning phase, there will be possibility to reevaluate the need for this.

Hardware

The hardware was selected and purchased early on, by CAEN. The HV board chosen is the A7038 which has both positive and negative versions, both required. The standard mainframe SY4527 will house the boards, in US15, thus completing the scheme. In Fig. 3.23 the locations and connections are shown, between the service and the experimental cavern.

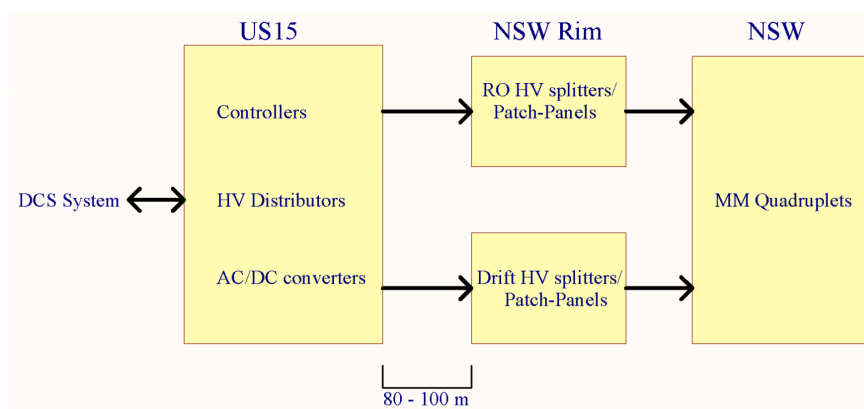


Figure 3.23: The MM HV locations.

3.5.2 sTGC

The sTGC detector requires a single voltage level for operation. The independent HV channels match the on-sector connections, which correspond to one layer per quadruplet, with the exception of the innermost quadruplet which has two channels. This amounts to 16 channels per wedge, or 32 per sector, or 1024 in total. On one hand the cables necessary are more than the MM, but at least the connection is easier due to lack of splitter box. The connection happens directly on the wedge edge, with a Lemo Redel connector.

Hardware

The hardware is also from CAEN, but a bit scaled up from the MM solution. The main connection is the mainframe, with generators providing service and power voltage. But the HV boards are inserted in EASY crates, located in UX15 racks. Due to the number of boards, Branch Controllers are used. The layout is shown in Fig. 3.24.

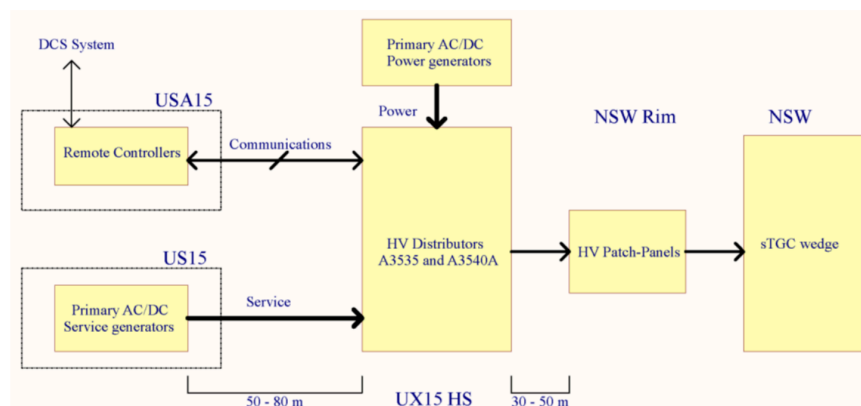


Figure 3.24: The sTGC HV locations.

3.6 Low Voltage

The Low Voltage system consists of all electronics and connections to bring electrical power to the front-end electronics. The general layout is shown in Fig. 3.25. The power comes from US15, while controls are in USA15. The generators produce 300V, which is delivered to module, called Intermediate Conversion Stage (ICS), which produce up to 12V for the electronic boards, where there are on-board DC-DC converters that transform the 12V to 1-2V for the integrated circuits.

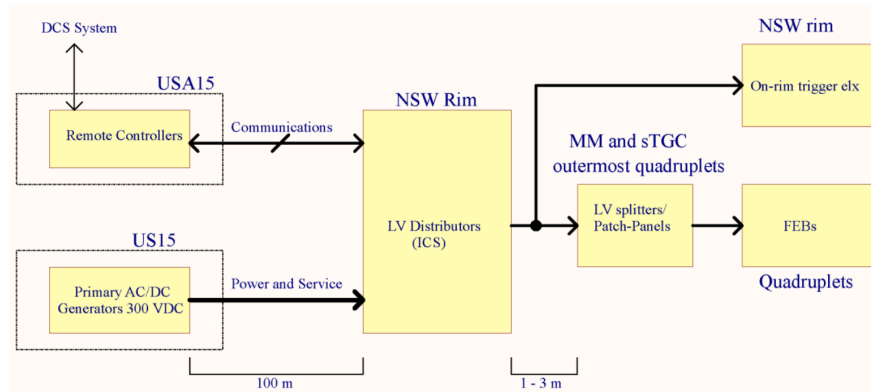


Figure 3.25: The NSW LV locations.

3.6.1 Scheme

From US15 the primary cables will enter one of the holes in the wall, to reach UX15. Then they are routed to sector 13, where there will be a secured patch panel with 22 heavy duty connectors. Each connector can include at most two to three primary cables, due to the amount of copper permitted in the shell. The patch panel will include a safety switch, connected to a control system that will automatically cut power in case the cover is opened. This is necessary considering the high current passing from these connectors. After routing on the NJD, the cables reach the ICS modules, which are assembled in groups of four, into ICS crates. Each of the eight ICS channels is software controllable. The ICS channel is connected to passive splitter boards which distribute the power to up to eight boards.

3.6.2 Consumption

Power consumption has many levels to consider. There is big difference between the power provided to the main generators and the power actually required by the front-end electronics. The front-end electronics power consumption is shown in Fig. 3.26. This should take into consideration losses from the on-board DC-DC converter, which is a CERN-made ASIC, called FEAST [17]. Since the first iterations, the suggested power supply was an active one, on the rim, which would provide eight channels per module. The total power of almost 150kW would have to be distributed among those supplies. Losses are expected on every converter, so these are also taken into account. Also, in certain cases there is significant voltage drop along the cable, depending on the power and copper cross section.

	Boards	Power/ board (W)	Board/ Layer L	Board/ Layer S	Board/ Sector L	Board/ Sector S	Board/ Wheel	Total boards	Total power /board (kW)
MM	MMFEB	18,80	16	16	128	128	2048	4096	77,01
	ADDC	9,90	2	2	16	16	256	512	5,07
	L1DDC	13,80	2	2	16	16	256	512	7,07
	Power (W)		348	348	2786	2786	44573	89146	89,15
sTGC	pfEB (8 VMM)	26,06	3	3	24	24	384	768	20,02
	pfEB (3 VMM)	9,05	3	3	24	24	384	768	6,95
	L1DDC pad	9,50	1	1	8	8	128	256	2,43
	L1DDC strip	10,20	1	1	8	8	128	256	2,61
	Rim-L1DDC	10,20	0	0	1	1	16	32	0,33
	Router	26,00	1	1	8	8	128	256	6,66
	Pad Trigger	30,00	0	0	1	1	16	32	0,96
	Power (W)		151	151	1249	1249	19977	39954	39,95
	Total power (W)		499	499	4034	4034	64550	129100	129,10

Figure 3.26: The expected NSW LV power consumption.

1145 In US15, several racks will need to be used for the generators. Each generator will give up to 7.5kW, while there is a limit of 25kW of power per rack.

3.6.3 ICS

1150 The ICS was initially defined having a space envelope of 200x200x90 mm³. Later this evolved in having four modules together, in a commonly cooled crate with envelope 400x300x240 mm³. The projected power output is around 1.2kW per module, distributed among eight channels. Two companies, Wiener and CAEN participated in the enquiry, both of which prepared prototypes for testing.

1155 The prototypes were tested in B-field in the MNP17 magnet facility at CERN, but also in the CHARM facility, at CERN, for high radiation. Both prototypes passed the B-field test, which consisted of reaching at least 80% performance in a field of maximum 0.5T. The radiation test was more eventful, with both first prototypes failing for different reasons. In the end, the one from CAEN, after small modifications, was the one that survived the test.

Channel grouping

1160 The first iterations of defining the design did not take into account any redundancy and simply distributed the ICS channels to the sectors; example in Fig. 3.27. However this scheme would be impossible to cable in practice, and also a big part of the sTGC trigger electronics was powered, which was bad on the side of risk management. There were many attempts to optimise the distribution of ICS channels to the sectors; this is discussed in further detail in the "Risk analysis" section. In the end, we decided to couple two ICS crates with two sectors. This results in a total of eight ICS modules, five of which serve two MM sectors, and the other three serve two sTGC sectors. Note that this refers only to the on-wedge electronics. The sTGC Rim crate is powered by "remote" ICS, which are placed on the ATLAS structure, just off the rim of NSW Sector 3. 1165 Another important detail was the decision to separate the two technologies at the level of ICS modules.

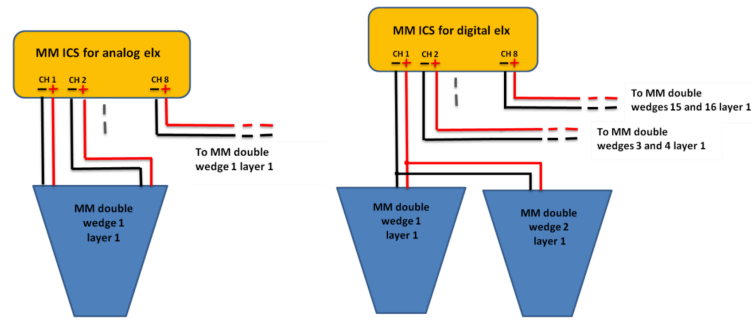


Figure 3.27: Initial LV scheme example for the digital on-board boards.

The simplified scheme of only two ICS crates is shown in Fig. 3.28. Note the color coding, where the darker colored channels correspond to powering the digital-only electronics, i.e. *DDC cards. Also note that some sTGC channels are noted as spares. One of the spare channels will probably be used for the sTGC repeaters, which were added later in the design phase.

The same scheme is shown in Fig. 3.29, but demonstrating the real channel distribution among the ICS, i.e. channel by channel, giving the name of the corresponding LVDB that is powered.

	ICS13	ICS14	ICS15	ICS16	ICS17	ICS18	ICS19	ICS20
1								
2	2 layers	2 layers	2 layers	2 layers	2 layers	2 layers over 2 sectors	2 layers over 2 sectors	2 layers over 2 sectors
3								
4								
5								
6						spare		
7	2 layers		2 layers				spare	
8						2 layers over 2 sectors		

Figure 3.28: The NSW LV ICS split to channels (simplified view).

	ICS13	ICS14	ICS15	ICS16	ICS17	ICS18	ICS19	ICS20
1	MD-S3-L12	MD-S3-L34	MD-S3-L56	MD-S3-L78	MD-S4-L12	SD34-L13	SD34-L24	SD34-L57
2	MA-S3-L12-LL	MA-S3-L34-LL	MA-S3-L56-LL	MA-S3-L78-LL	MA-S4-L12-LL	SA3-1	SA3-2	SA3-5
3	MA-S3-L12-LR	MA-S3-L34-LR	MA-S3-L56-LR	MA-S3-L78-LR	MA-S4-L12-LR	SA3-3	SA3-4	SA3-7
4	MA-S3-L12-RL	MA-S3-L34-RL	MA-S3-L56-RL	MA-S3-L78-RL	MA-S4-L12-RL	SA4-1	SA4-2	SA4-5
5	MA-S3-L12-RR	MA-S3-L34-RR	MA-S3-L56-RR	MA-S3-L78-RR	MA-S4-L12-RR	SA4-3	SA4-4	SA4-7
6	MD-S4-L34	MA-S4-L34-RL	MA-S4-L56-LL	MA-S4-L56-RR	MA-S4-L78-LR	spare	SD34-L68	spare
7	MA-S4-L34-LL	MA-S4-L34-RR	MA-S4-L56-LR	MD-S4-L78	MA-S4-L78-RL	SA3-6	spare	SA4-6
8	MA-S4-L34-LR	MD-S4-L56	MA-S4-L56-RL	MA-S4-L78-LL	MA-S4-L78-RR	SA3-8	spare	SA4-8

Figure 3.29: The NSW LV ICS split to channels (detailed).

Board grouping

The power consumption per board was shown above, but we still need to define the exact number and types of cards to be grouped into channels, and consequently be powered by the same LVDB board. Looking at the requirement, we deduce the rule that a single ICS channel should feed 6-8 electronics boards. This roughly translates to eight MMFE8, or six FEB, or eight *DDC cards. Also, it makes sense to group similar boards together, rather than mix different functionalities. The grouping table is shown in Fig. 3.30. along with the corresponding total consumption and channel usage, which is important in order to avoid extreme usage.

	BOARD GROUPING		For V=10V, => 144W max power		channel usage	
	[W]/board	#boards/ch	ch name	[W]	%	
MMFE	15.8	8	MA	126.4	88%	
MM-L1DDC	7	4	MD	52	36%	
ADDC	6	4				
sFEB	22	3	SA	93	65%	
pFEB	9	3				
sTGC-L1DDC	5	8	SD	40	28%	

Figure 3.30: The NSW LV ICS split to channels (simplified view).

The board grouping also needs to be mapped on the detector geometry. This is a critical process, with great impact on redundancy. If the eight MMFE boards are on the same PCB among eight layers, then loss of a single ICS channel corresponds to loss of 8 layers of MM in a single location, which is not acceptable. Therefore, the boards are spread, as possible, among the same layer, and among sectors, to maximize redundancy, while retaining some ease for the cable installation. Fig. 3.31 shows the ICS channel to LVDB and functionality correspondence.

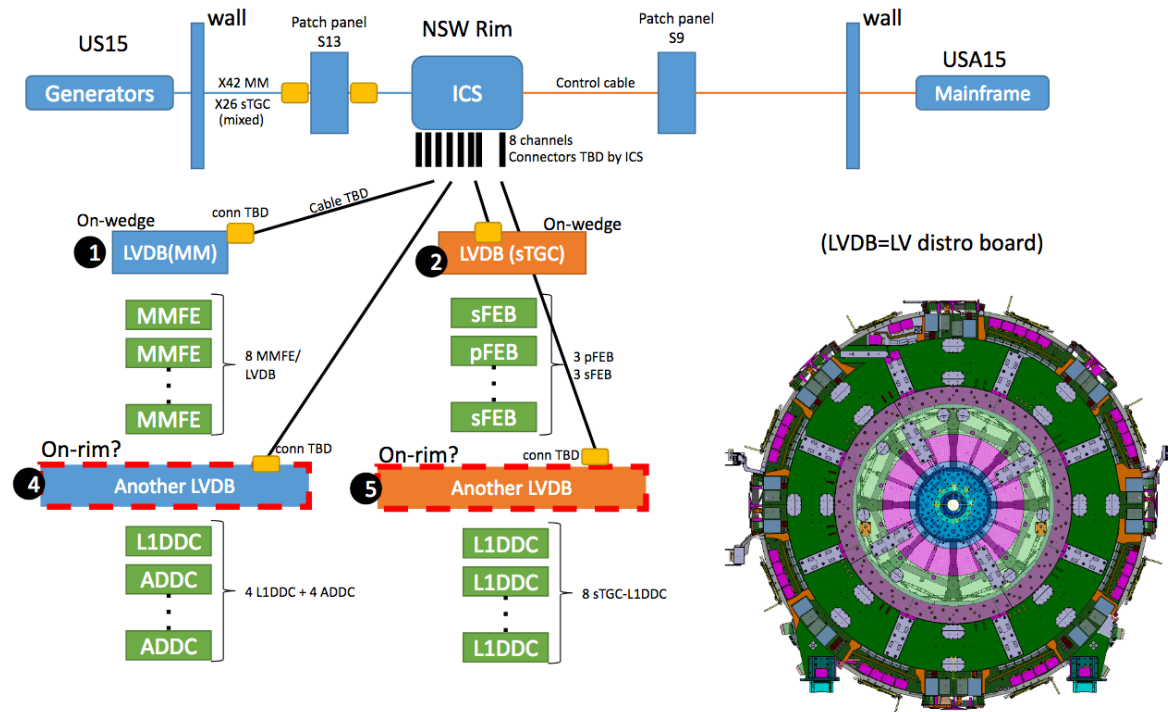


Figure 3.31: The NSW LV ICS split to channels (simplified view).

Control

Communication with the modules is achieved through a standard serial connector. The modules will be daisy-chained, allowing to reduce the number of cables necessary.

Interlock

The ICS modules carry significant power and, in case of communication loss, we should be able to power them off "manually". This is achieved by adding lemo-type connections to the modules, where an interlock is implemented internally. This means that the module cannot be turned on unless there is connection at the interlock connection. The actual cabling is routed to the service cavern, on a patch panel that is accessible at all times, so that a user can simply disconnect the appropriate cable to shut down or reset a malfunctioning module.

Cooling

The ICS modules need cooling, which will be provided by structural backplates. Each ICS crate shall have an input and output water pipe connection, which is internally connected to the backplates. In the initial design, the modules were in small crate-like boxes, with their own cooling connections, which would be disconnected when replacing a power supply. This was later changed, to allow easier swapping of the modules. This system is still in development in early 2019.

Removability

The power supplies inside the experimental cavern, and namely inside the Toroid area, are exposed to a certain level of radiation, depending on the distance from the beam pipe. For this and other normal reasons, power supplies can malfunction, so they need to be easily replaceable. A user shall be able to approach the crate and unscrew the module connections, remove it and carry it out. In the first designs, which included the cooling system in the module, it would be very difficult to replace an almost 15kg module, while hanging from scaffolding. Luckily, improved removability was achieved by shifting the cooling plate to the crate structure.

Access & Tile

Access to the crates is also not a given, since the NSW is surrounded by other detectors, and when not, it is not simply in a rack that can be routinely accessed. In particular the ICS crates need also space for the removal of the modules in front, which is often shown in the 3D models as a semi-transparent box envelope in front of the ICS crate. This requirement was nicely combined with the requirement from Tile calorimeter to have a corridor to access their electronics boxes.

Rim crate power from Sector 3

An important part of electronics, not included in the ICS tables of the last sub-sections, is the sTGC Rim crate. Powering these crates was a concern, given that a single rim crate is a single point failure for an entire sTGC sector. Initially, we would have the ICS power supplies for the rim crates on a rack in UX15, level 7 US-side, which would offer optimal accessibility. A rack is normally reachable to operate on and swap a board during a 1-2 hour access. Meanwhile, the NSW accessible areas, the large sectors, are in principle also accessible within the same time-frame; however manual operation there is a bit hindered by the fact that a person needs to hang from a platform or reach from uncomfortable positions, which is why a better solution was looked for.

Unfortunately, the space available is not only for the NSW. This made routing the cables from the designated rack to an on-wheel patch panel on sector 3 very challenging and space-consuming. A better middle-ground solution was identified then. The ICS crates, one per side, are to be placed on the ATLAS structure, a couple meters from the sector 3 patch panel on the wheel, inside the toroid. This location solves most problems since:

1. it is next to an accessible ladder, allowing operation by a person standing up or sitting down on the steps
2. it is accessible during a few hour access
3. it eliminates the need of passing thick low voltage cables through the packed toroid cable trays
- 1235 4. cooling is reachable thanks to existence of RPC thermal screens in the vicinity
5. voltage drop is minimized

One additional detail is that these power cables are connecting directly on the wheel instead of going through a flexible chain, which means that it adds a step in the yearly shutdown for the wheel movement to the parking position. The problems solved outweigh the extra step for the opening process.

- 1240 Last, since there is no flexible chain to permit maintaining connection to the wheel when in the parking position, extension cables will be installed, from the ICS to the corresponding position of the sector 3 patch panel, but on the NSW parking position. So, depending on the NSW position, different cables will be connected on it.

3.6.4 LVDB

- 1245 Between the ICS modules and the on-chamber electronics there is need to introduce a splitter board for the power, in order to distribute a single channel to up to eight boards. These are called Low Voltage Distribution Boards (LVDB), and the following types are needed:

- 1250 • Micromegas: on the Micromegas wedges, the LVDB will be placed on existing slots, sized 60x210mm³, next to the MMFE8 boards, in PCB2 and PCB7. The initial placement was on the top of the wedge, for better accessibility and less worries for radiation hardness. However, during the services routing exercises it was shown that the available space was not enough. For this reason, one of the LVDBs was moved to the inner radius. Each wedge utilizes eight LVDB. The board has two input connectors to distribute power to one channel of MMFE and one channel of *DDC boards. The inner radius LVDB are only used for MMFE cards. The final distribution scheme is: one channel of eight MMFE boards is shared over two layers, four PCBs of one wedge side.
- 1255 • sTGC (FEB): Each sTGC layer has six Front End Boards (FEB), which are grouped into an LV channel. The on-wedge LVDB stack is placed on one side of the wedge only, and then the cables are internally routed.
- 1260 • sTGC (L1DDC): The sTGC have one L1DDC per layer per side, just like MM. Between the two choices of spreading the cables among too many sectors, and powering an entire wedge with a single channel, the sTGC L1DDC low voltage is grouped in two layers of two consecutive sectors. This naturally places the corresponding LVDB off-sector. At the time, the board is not designed yet, but it is expected to be placed close to the spoke corner, in the middle of a large and a small sector.
- 1265 • sTGC (Rim): The Rim crate ICS channels were discussed above. However, splitting is still necessary. A board, not designed yet, is going to be placed as close as possible to the rim crate, perhaps even fixed on its outer surface, to allow 1-to-4 splitting of the power.

- Repeaters: The repeaters system is discussed under the Twinax cable subsection later. These boards will also require some type of LVDB to be produced and located near them, on top of the spokes.

3.7 Fibers

1270 The Fiber system was mainly defined by Weizmann Institute.

The NSW Fiber system consists of all optical readout fibers, installed on the wedges, on the rim, routed on the NJD, reaching USA15, where they are plugged into FELIX and Trigger Processor machines. The main categories are readout and trigger. The global fiber plan is shown in Fig. 3.32 and 3.33.

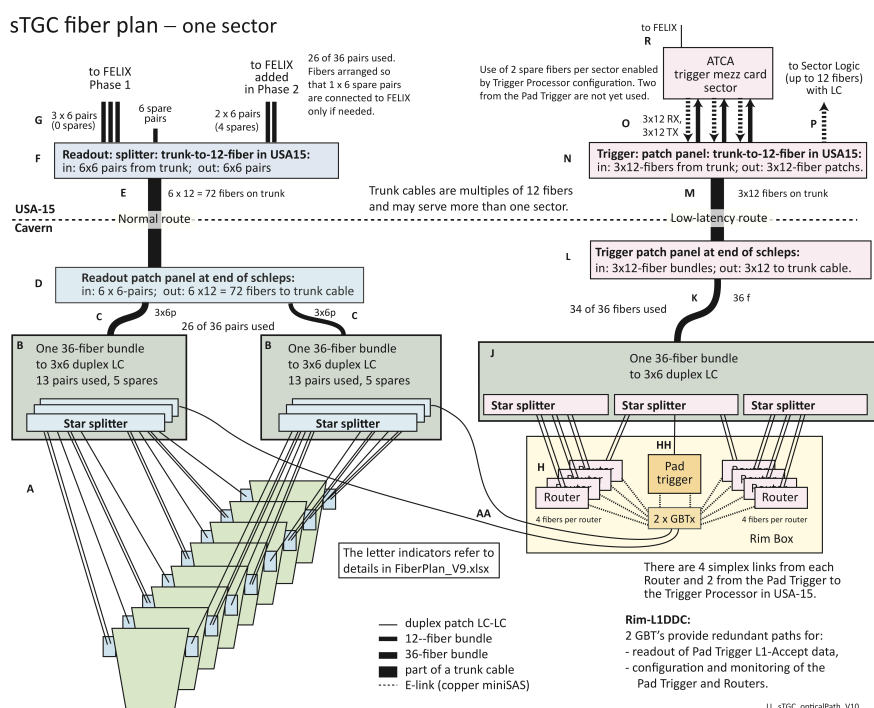
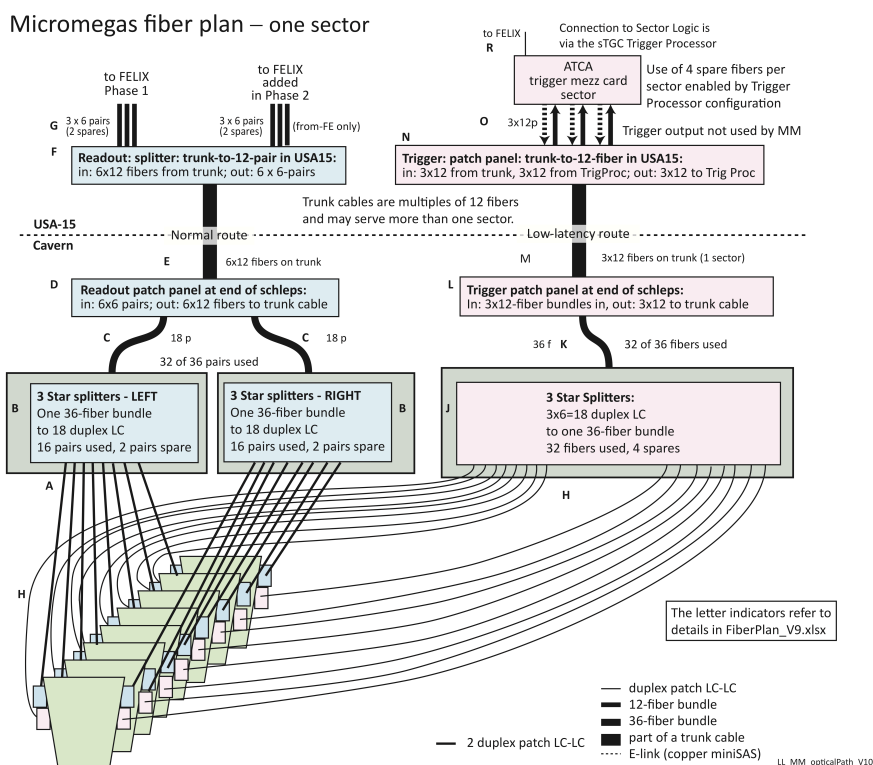


Figure 3.32: The stGC fiber plan.



3.7.1 Connection scheme

The NSW readout scheme has been described in the introductory chapters. Fiber patch cords are used to send data from the *DDC and sTGC Rim create cards. First, these single cable fiber pairs are routed from the boards, through the cooling channel (MM), to the wedge corner. From there, they follow the installed cable trays to the "Small Fiber Boxes" on the rim. These boxes function as 1-to-36 splitters. Incoming fibers are connected on one of the three "star modules" inside the box, each of which provides 12 fiber connections, which are assembled into a 12-fiber bundle. Then the three bundles are assembled in a 36-fiber bundle which is routed on the NJD to reach the "Large Fiber Boxes" on the bracket. There we have a further grouping of fibers to 144-fiber bundles. However, an important regrouping is done, as shown in the table of Fig. 3.34.

Underground				MTP (USA15)		MM		sTGC	
Trunk	small box	group	TxRx pair #	MTP #	TxRx pair #	Phase		Phase	
MM: RMA1..8 or RMMC1..8	small sector left	A	1-6	A	1 - 6		incl 1 spare		
		B	1,2,3	E	1 - 3			spare	
		C	4,5,6	F	1 - 3	Phase 2	incl 1 spare	Phase 2	incl 2 spares
	small sector right	A	1-6	A	7 - 12		incl 1 spare		
		B	1,2,3	E	4 - 6			spare	
		C	4,5,6	F	4 - 6	Phase 2	incl 1 spare	Phase 2	incl 2 spares
	large sector left	A	1-6	B	1 - 6		incl 1 spare		
		B	1,2,3	E	7 - 9			spare	
		C	4,5,6	F	7 - 9	Phase 2	incl 1 spare	Phase 2	incl 2 spares
sTGC: RSTA1..8 or RSTC1..8	large sector right	A	1-6	B	7 - 12		incl 1 spare		
		B	1,2,3	E	10 - 12			spare	
		C	4,5,6	F	10 - 12	Phase 2	incl 1 spare	Phase 2	incl 2 spares
	large sector left	A	1-6	B	1 - 6		incl 1 spare		
		B	1,2,3	E	7 - 9			spare	
		C	4,5,6	F	7 - 9	Phase 2	incl 1 spare	Phase 2	incl 2 spares
	large sector right	A	1-6	B	7 - 12		incl 1 spare		
		B	1,2,3	E	10 - 12			spare	
		C	4,5,6	F	10 - 12	Phase 2	incl 1 spare	Phase 2	incl 2 spares

Figure 3.34: The RO fiber mapping from on-wheel to off-wheel parts.

The readout fibers are routed to the bottom of UX15, following the long path to USA15, through the galleries, where they will end on connections to FELIX. The trigger fibers are routed towards z-0 (center of the detector) and then almost straight out through the wall and into USA15, to reach the first row of racks and connect to the NSW Trigger Processors.

3.7.2 Trigger Latency

During physics run, the Central Trigger Processor expects trigger data within a certain time-window, in order to include them in the event. This time-window basically defines a deadline of a few ms for the detector to process its trigger data and bring it to the CTP. To calculate this Trigger latency, we sum the various time-components, from the very beginning of the particle and its Time-of-Flight, through all electronics signal processing, and signal routing times on copper or fiber. The tables show the sum for MM and sTGC, where it is shown that MM are very low in latency, far from the limit, which is a great achievement, and is justified from the simplicity of the connectivity design.

However, the sTGC latency budget is on the limit of the deadline, with a slight margin of a few ns. To reach this number, all existing algorithms had to be timed in reality or simulation, while all cable lengths had to be minimized.

One campaign was the fiber lengths. Many visits in-situ had to be arranged to identify the optimal route for the trigger paths, in order to reach the now used 42m of a path.

Another campaign was the TwinAx lengths. More details on the cables themselves will follow. The drawback of the sTGC trigger design, with the back-and-forth data path from pFEB to PadTrigger to sFEB to Router, which has a great effect on the sum.

3.7.3 Radiation hardness

The fiber type selection included testing the fibers under radiation (done by Weizmann). In Fig. 3.35, the expected total ionizing dose is shown on a large sector, to understand in each board position, and especially the ones with fiber connections, how close the expected radiation is to the limit. The tested fiber was exposed

to around 100Gy, having in the end a signal loss of almost 1dB, which will be acceptable for the NSW use case.

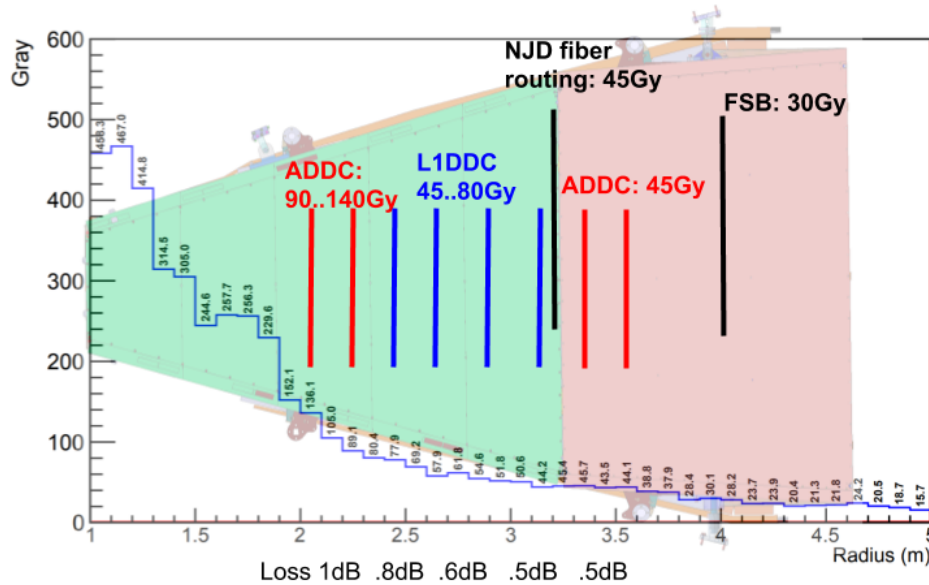


Figure 1: The simulated TID dose for the NSW (Gy/10yr). The values are scaled to an LHC luminosity of $\mathcal{L} = 3 \times 10^{34} \text{ cm}^{-2} \text{ s}$

Figure 3.35: TID of NSW as function of distance from beam pipe.

3.8 Alignment

The Alignment system, as a whole, is a responsibility of Brandeis University. The services and system are described here for completeness.

The existing alignment system, up to the cables reaching the NSW brackets will be reused. This part consists of a set of 100m network-type custom cables which connect on the corresponding PCs in USA15, where the data processing is done. In principle, special cameras are placed in specified positions on the detectors, which then monitor the exact location of particular targets, such as fixed light-emitting fibers. The camera data is then combined with the other cameras, and the software estimates the real position of the objects, within a few microns of precision.

On the NSW, the bracket employs simply a one-to-one patch panel for the alignment cables, with RJ45 type connectors. After the usual NJD routing, some of these cables (called ROOT cables) reach the alignment bars. The rest reach the Rim area. In both cases the end connection is a Multiplexer box, which acts as a communication hub for the next level, which is the cameras on the bar or the "36-way injectors" on the rim. The injectors include the LED diodes, over which the alignment fibers are connected. These fibers are routed on the wedge surface, where they are inserted on precisely produced and positioned platforms, allowing the exiting light to be visible to the cameras. This simple scheme allows for great precision on positioning, much like the methods already used for the Monitored Drift Tubes in ATLAS.

3.9 DCS

The hardware part of the DCS system is a responsibility of NIKHEF. Usually the term DCS is connected with software, but it also includes the on-detector hardware part which will be described here.

1330 The main component is the ELMB board, which is housed inside a robust enclosure. The ensemble is called MDT DCS Module (MDM). Due to its versatility and performance, it will be used for the NSW, placed on the outer radius of the spokes, where it can be accessible for future fixes or replacements.



Figure 3.36: MDM modules installed on NSW spokes.

The ELMB provides several interfaces [18] of which only two are used for the NSW case. The 30 connections for temperature sensors and two connections for dual B-field sensor readout. The cables connect the ELMBs with the sensors which are installed on the surface of the wedges, but also on the cooling channels (temperature only). The T-sensor and B-sensor locations are shown in Fig. 3.37.

1335



Figure 3.37: MDM modules installed on NSW spokes.

The ELMB communication protocol is CANbus. A control PC in USA15 connects to two Junction Boxes per wheel next to the bracket. Each Junction Box has two connections, each of which connects to a line of ELMBs, in daisy-chain. The last ELMB in the line has a terminator CANbus connection on its output, so that the chain is closed there. The placement of the ELMBs is shown on Fig. 3.36.

3.10 TwinAx cables

The NSW upgrade brings a new level of readout channel density and number. This number has to be reflected on the complexity of the system. There are numerous connections within all the electronics. Since the early tests in 2012, the cable with the best performance in terms of dB loss and form factor was the TwinAx, as produced by 3M. More than 40km of the cable are used for the NSW, in many difficult places and with several restrictions, which merits the separate mention here.

3.10.1 The ribbon

The cable consists of a ribbon and two connectors. The lines in the extremities are called side-bands which are not always used. In the NSW case, they are not used. This leaves the existing 8 pairs of copper to be used for differential signal transmission. A picture of the drawing is shown in Fig. 3.38.

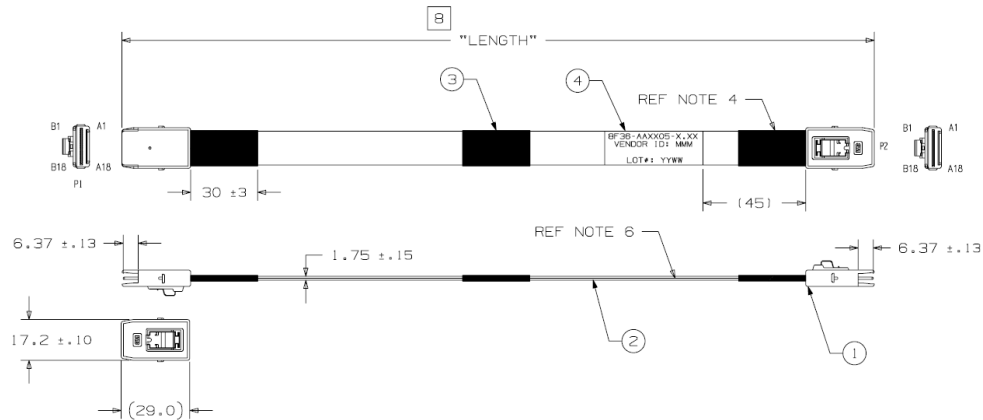


Figure 3.38: TwinAx cable drawing.

3.10.2 Micromegas case

For MM it is only used at the wedge level. Each L1DDC board connects to eight MMFE boards of the same layer side. Each ADDC board connects to eight MMFE board of the same layer side. Also, each L1DDC and ADDC pair are connected with a cable. All these cable are stored inside the spacer frame for a Micromegas double wedge, amounting to 272 cables inside the frame. Routing these cables is challenging, due to the limited space, the addition of structural bars between the frame plates and the central bar which doesn't allow easy crossing. A picture of a final routing prototype is shown in Fig. 3.39 (BB5 team). As seen in the ribbon cross-section, the cable has part of the shielding exposed on the edges, which can lead to ground loops in the system. To avoid this, the ribbons are covered with Kapton tape, which gives them this golden color in the picture.

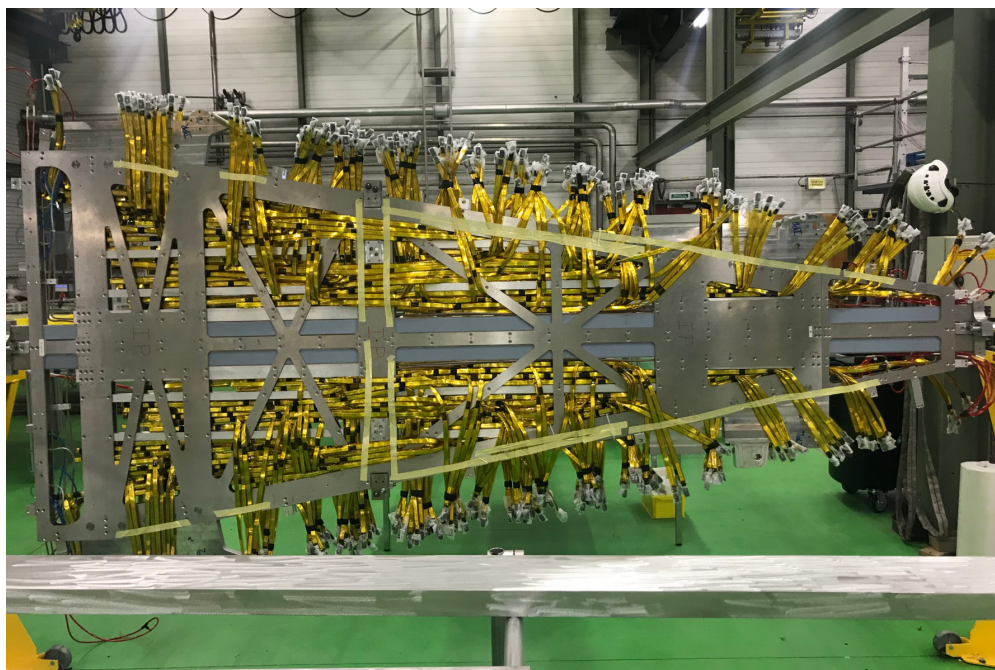


Figure 3.39: TwinAx cable routing, on a complete Spacer Frame.

Lower radius envelope

The sector envelope is meant to limit the chamber dimensions to allow safe margin of movement for precise positioning and installation. The lower radius MM envelope is too close to the spoke. For this reason the TwinAx connectors need to be machined to stay in the envelope. An example is shown in Fig. 3.40 from an early cutting session.

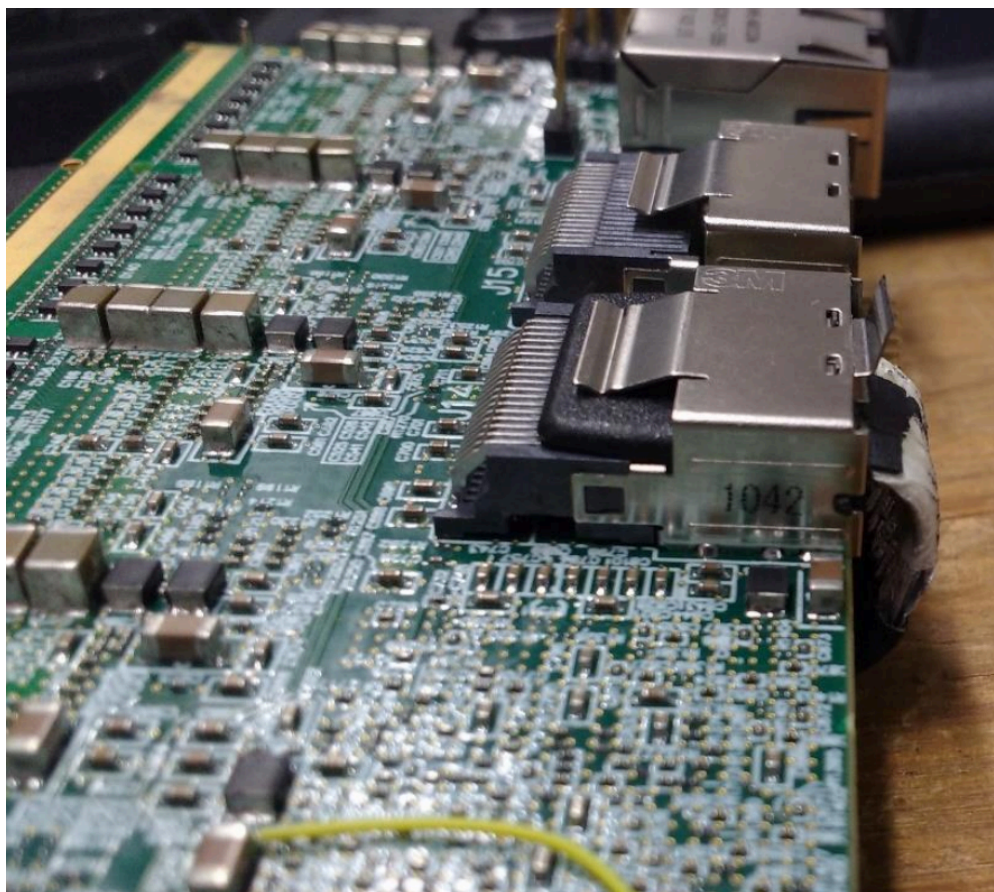


Figure 3.40: TwinAx cable connected on a MMFE8 board, while half of the plastic connector has been sawed off to allow minimal envelope violation.

3.10.3 sTGC case

For sTGC, it is used both at the wedge level and for routing to the Rim. The on-wedge part is simpler, as there is only L1DDC cards connecting to three FEBs. The TwinAx are routed in the service tray on the side of the wedge.

1370 There is also an off-wedge part, which corresponds to the trigger path. In brief, the pFEB on the chamber send the pad hit data to the PadTrigger board on the Rim. The PadTrigger combines the sTGC sector hits and sends the info to the corresponding sFEB to send the strip data to the Router boards on the Rim. This back-and-forth data path was mentioned also in the Trigger Latency sub-section.

1375 Initially these cables would be between six and eight meters, from the on-wedge FEB to the Rim. In parallel, the corresponding electronics connections were being tested, and it was discovered that long cables (more than three meters) had stability issues, resulting in many errors in tests such as PRBS (pseudo-random binary sequence). This led to the need of employing signal repeaters for the long lines. For this and latency reasons the lengths were shortened to a maximum of six meters.

All three parts of the data path needed repeaters, two of which are "Serial" while the other is "LVDS". The

distinction and locations are shown in Fig. 3.41.

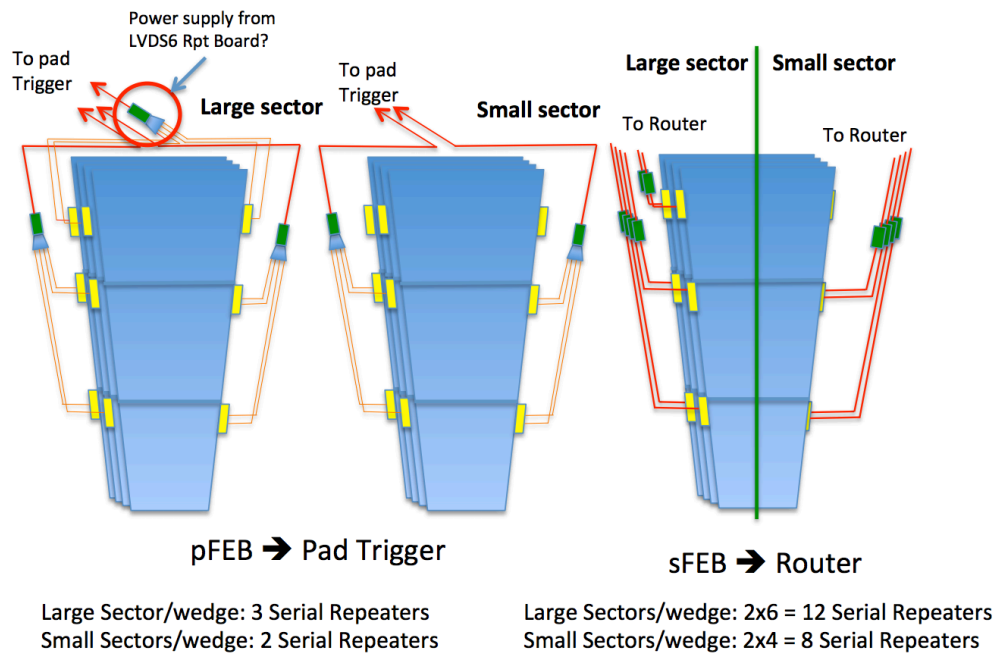


Figure 3.41: sTGC repeater scheme.

The LVDS repeater boards shall be placed on the spoke, while the Serial ones will be included in the sTGC wedge, fixed next to the L1DDC boards. Several restrictions made this design a bit complex:

- the repeater board needs power, which they will get from the usual FEAST DC-DC converters, as used in the other boards. Serial repeaters will take power from the sTGC-L1DDC boards, due to ease and proximity. LVDS repeaters will be bundled on a new PCB, called LVDS6, housing six repeaters, with dedicated FEAST modules.
- the LVDS6 needs cooling for the FEAST modules. This requires positioning closer to the cooling system on the spokes.
- due to a clock restriction from the Router board, the signals from the PadTrigger to the Router need to arrive to the Router with difference of multiple of 3.125ns. This corresponds to length differences of 62.5cm.
- ideally, the lengths would be exactly what we measure on the 3D models, but we have to take into account optimisation for logistics for our own organisation. For this reason we try to group the cable lengths to a manageable level of different part numbers.
- similar to the last item, the length groups need to comply with what the producers and distributors prefer. Otherwise big delays will hinder progress.

With all the restrictions taken into consideration, the final cable lengths and groups for each connection is shown in the table of Fig. 3.42.

pFEB-to-Pad		Serial				
	pFEB	L SATA [m]	L MS [m]	rep	L [m] MST	Pad
QL1		2	0.5		3	
QL2		1	0.5		3	
QL3		3	1		0	
QS1		2	0.5		3	
QS2		1	0.5		3	
QS3		3	1		0	
pad-to-sFEB		LVDS				
	Pad	L [m]		rep	L [m]	sFEB
QL1		4.25			2	
QL2		4.25			2	
QL3		3			2	
QS1		3.5			2.5	
QS2		3.5			2.5	
QS3		3			3	
sFEB-to-Router		Serial				
	sFEB	L [m]		rep	L [m]	sFEB
QL1		3			3	
QL2		3			3	
QL3		3			3	
QS1		2.5			3	
QS2		2.5			3	
QS3		3			0	

Figure 3.42: sTGC repeater cabling lengths.

3.11 Grounding

1400 Proper grounding connections are essential for a detector to work correctly. Loose ground connections worsen the signal/noise ratio, due to pick-up and can sometimes lead to ground-loops, which can also stop a detector from working properly.

The NSW grounding comes from four densely braided cables which connect to a main ATLAS ground. The idea is to have the common connection as far as possible between various connections. This is why MM and
1405 sTGC have also separated ground connections, but clearly all MM are connected together. The wedges have connection points on their outer edge, and each wedge is connected to the next, like a daisy-chain.

It is also important to keep the different grounds separated. There is the main ATLAS Safety ground, but also the power supply ground. In the MM grounding scheme ([EDMS document ATL-M-ES-0025](#)) the separation is defined, here shown in Fig. 3.43.

1410 LV distribution

From the mentioned document, we see from Fig. 3.43 many details, of which some are pointed out:

- The resistive strips are biased at a positive value of high voltage and must be bypassed with capacitors to prevent pickup. The bypass capacitors should go to analog ground (AGND) shown as a green triangle.
- 1415 • The drift planes are biased at a negative value of high voltage and must be also bypassed with capacitors. Both positive and negative high voltages are provided to the resistive strips and drift planes by 1 M Ω resistors, respectively.
- The return high voltage lines (HV GND) are tied to the AGND using 100 Ω resistors.
- The mesh, drift and readout panels should be kept and connected to AGND.
- 1420 • The outer Al honeycomb drift planes are tightly connected to the ATLAS ground.
- The Cu Cooling Profiler is connected to AGND.
- The Spacer Frame is isolated from the Micromegas quadruplet but connected to the ATLAS GND.
- For the HV of the drift planes, one HV filter per quadruplet is used. All four drift planes are connected via a zero resistance low inductance connection.
- 1425 • For the HV of the resistive strips, two HV filters per board are used.
- The Analog Ground of the MMFE boards connects to the AGND plane of the Micromegas via a zero resistance low inductance connection. This is accomplished through the aluminum bar that presses and holds the MMFE in place after installation on the chamber. The return line of the MMFE low voltage (DGND) is connected to the AGND via inductors.

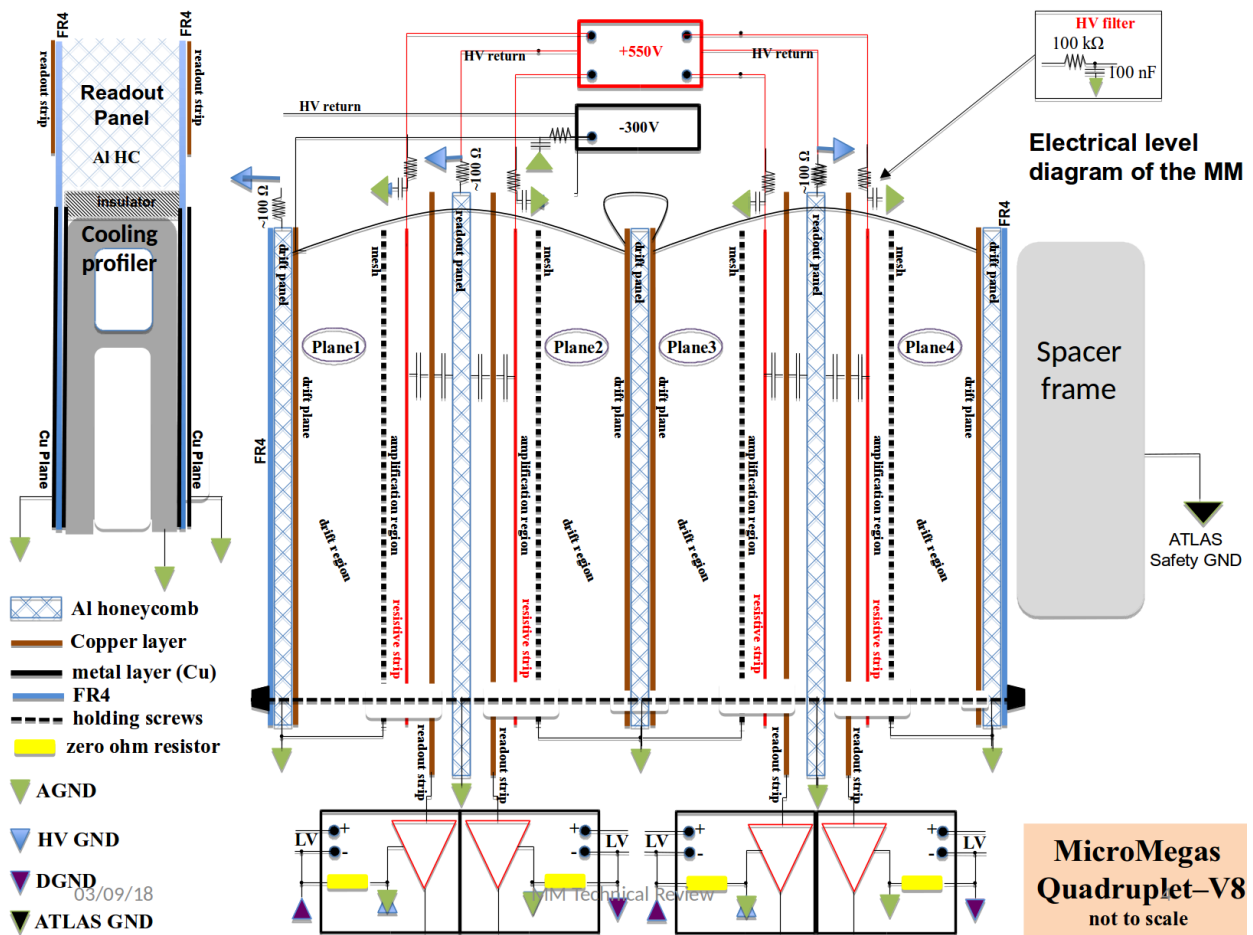


Figure 3.43: NSW Micromegas grounding scheme.

HV distribution

The High Voltage distribution follows the guidelines described in the document “ATLAS Muon Grounding”. The two main guidelines, as written by the Grounding group, are:

- For safety reasons, the bulk HV supply’s GND terminal should not be allowed to float as this could lead to an unsafe condition.
- The HV cable’s “GND” conductor is connected to detector elements through a “ground breaking resistor”, typically of the order of 1 kΩ. This resistor will typically drop only a few mV since the currents are so low.

3.12 Sniffers

An important addition to the safety systems is this network of open ended flexible pipes which are put under under-pressure, in order to “sniff” air from the experimental cavern, and analyze it for smoke particles and

flammable gases. This offers a method to detect fire and important gas leaks respectively. This system is in hands of TC, and installation on the wheel will be done later in LS2. The expected scheme for the NSW follows the one of the SW, shown in Fig. 3.44. The main idea is that flammable gas (n-pentane) is likely to leak from the detectors, i.e. HO side of the NJD, and it would go down, being heavier than air. On the other side, smoke particles would go higher, which is where they will be sniffed for. The Rim electronics are more likely to be a hazard, mostly due to the magnitude of power they handle (mainly ICS).

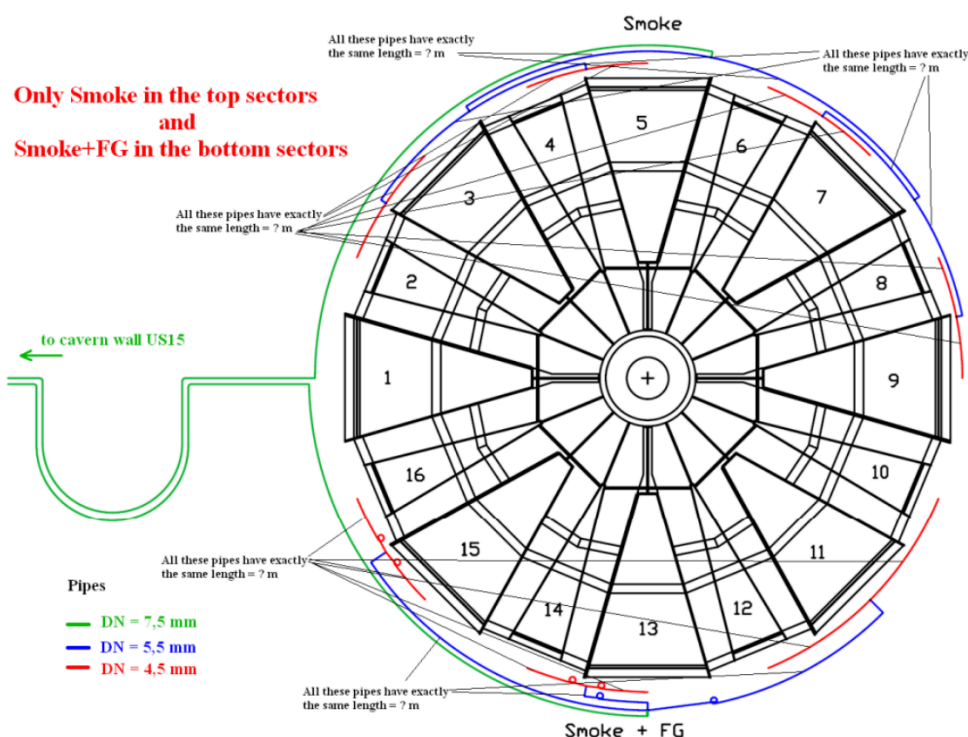


Figure 2: Sniffer layout for Small Wheel with some relevant information

Figure 3.44: The old SW sniffer system.

3.13 RadMon

In the late installation phase of the services, it was brought up that the NSW need to install radiation monitoring sensors, similar to the old Small Wheel. This is useful, both for the detectors to have an idea of the real radiation that the newly installed material is experiencing, but also the control systems to compare and calculate the expected luminosity, especially in view of HL-LHC. The design is out NSW hands at the time that this is written.

3.14 Failure modes and risk analysis

For the various NSW sub-systems, failure modes have been studied when designing the services systems, in order to optimise operation in case of mechanical or other failures. As mentioned in other sub-sections, it is sub-optimal to couple detector functionality in a way that a single point failure can cause loss of efficiency in a concentrated area. Especially for the NSW case, which provides 16 layers of tracking and triggering, the system connectivity should not allow many layers of the same sector to be lost in case of service channel failures. Instead, the effect should be spread among several sectors, so as to retain performance.

As specified in the NSW TDR [6], *"Any service distribution which is necessary for the recovery of larger detector parts in case of failures will be located at the rim of the NSW, preferably in the large sectors which are easily accessible"*. The baseline for such risk management for the NSW has been to maintain single layer loss in case of single point failure. However, as the design of the system progressed, it was more and more difficult to stick to the baseline, partly due to costs and partly due to complexity.

3.14.1 Specific cases

Low Voltage distribution

Several iterations have been done for grouping the LV channels. Some attempts are shown in Fig. 3.45. Many degrees of freedom were taken into account, which in some cases resulted in complicated connection scheme, but in extremely improved redundancy.

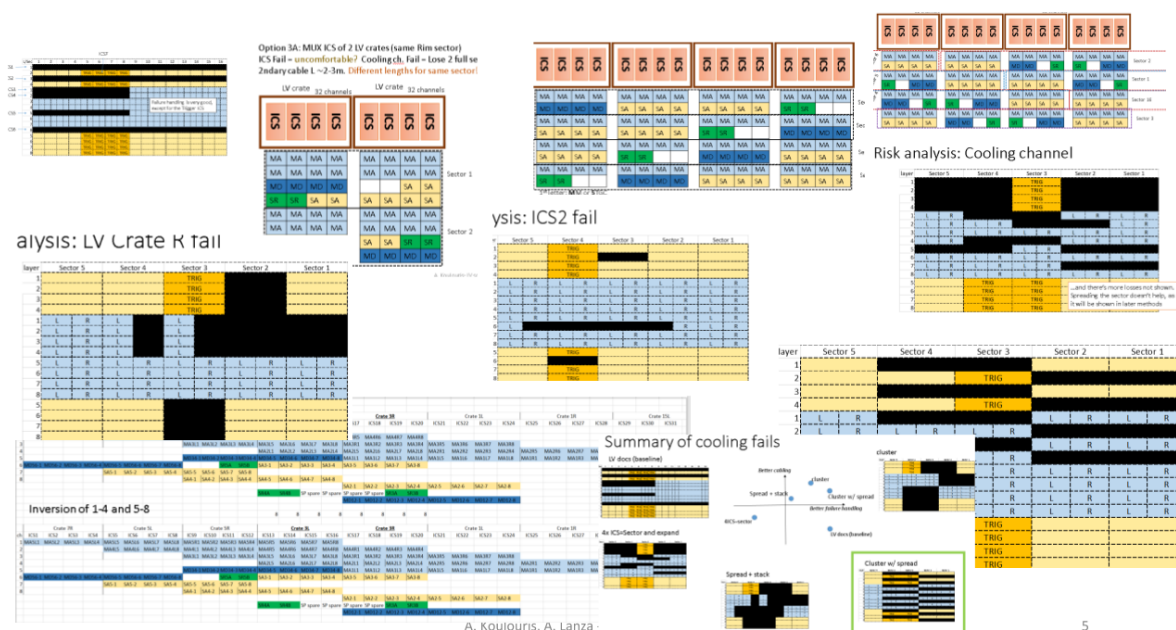


Figure 3.45: Some examples of LV schemes considered before the final. Initially, the main requirement was redundancy. This could reach extreme levels, with appropriate combination of channels and ICS modules, among crates, while keeping the routing sensible. However, since it was decided that the two technologies had to be separate, and that only two sectors would be served by the two ICS crates, a much simpler scheme was chosen.

1470 Multiple failure modes were considered, and graphed for several cases, e.g. Fig. 3.46, to visually show how an ICS malfunction affects the detector data-taking, in terms of number of layers looking at the beam.

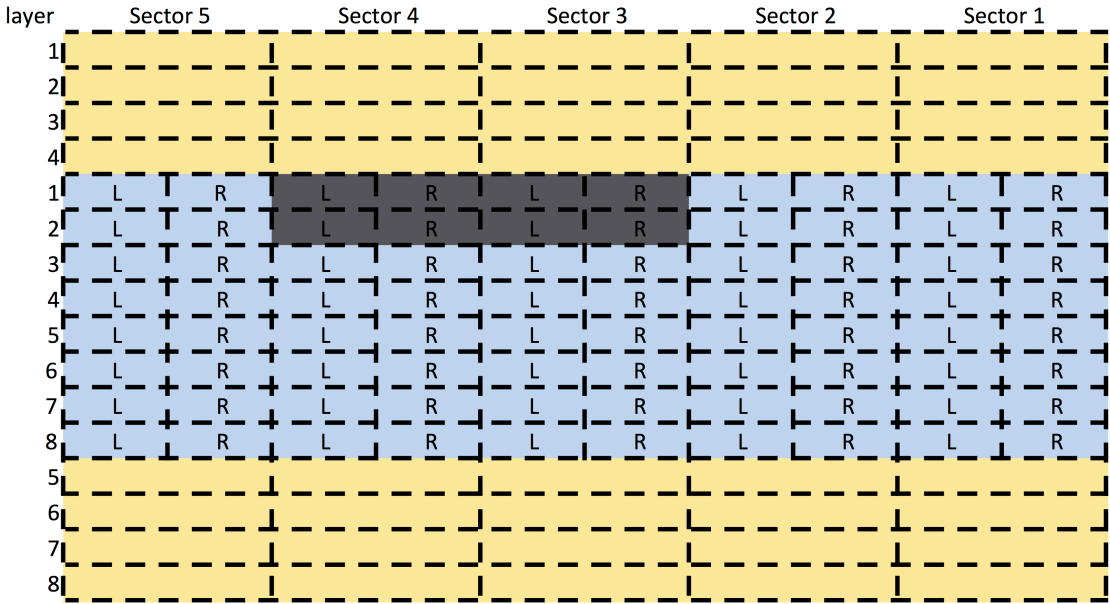


Figure 3.46: Graphic representation of five NSW sectors, showing 16 layers for each one. The yellow are sTGC, while the light blue are MM. The grayed out cells correspond to the part that is lost in case of a MM ICS failure.

High Voltage - Drift

The resistive high voltage connections are too many to have single channel for each one of them. The grouping per layer, as already mentioned, allows a sensible scheme. The single channel is software controllable, so the HV is not an issue in terms of risk and connectivity.

For the drift voltage there is only one channel per quadruplet, since it is a low risk item both for the detector safety and on the hardware side. However, since the final connection on the quadruplet is soldered, and the cable can be damaged, two connections are implemented for each quadruplet, but only one is used at a time.

Cooling distribution

The cooling sub-system offers a relatively large number of sub-channels. The detector design allows for a maximum granularity of wedge side for a cooling connection. This means that a sub-channel that splits to four lines on the rim cooling manifolds can supply two wedges, with cooling connections on each side. This translates to one wedge over two sectors, which would be lost in case of cooling channel problem.

This connection is already slightly problematic, since routing copper pipes across wedges would complicate the design. To optimise the situation, it was decided to have the cooling manifolds as accessible as possible, so that any problem with them would be solvable by accessing the large sectors. In Fig. 3.47 the corresponding wedge losses are shown. In the end, 4 wedge sides would be supplied by one sub-channel.

color code: saves money/energy/detector long term saves low risk saves high risk									
If we lose this channel	Then we turn off these channels:								
Micromegas	gas	gas sub-	water	water sub-	LV MMFE	LV Digital	HV Res	HV Dri	comment
Gas channel	itself	4 included	-	4 included	16 included	4 included	16 included	4 included	lose 2 wedges (gas sub- accessible in open position)
Gas sub-channel	-	itself	-	-	-	-	-	-	affected wedge can still operate
Cooling channel	-	-	itself	4 included	16 included	4 included	-	-	losing two half sectors. Other half can still operate
Cooling sub-channel	-	-	-	itself	4 included	1 included	-	-	losing half wedge. Rest can operate
LV MMFE channel	-	-	-	-	itself	-	-	-	
LV DigitalELX channel	-	-	-	1 included	4 included	itself	-	-	
HV Res channel	-	-	-	-	-	-	itself	-	
HV Drift channel	-	-	-	-	-	-	4 included	itself	
If we lose this channel	Then we turn off these channels:								
STGC	gas	gas sub-	water	water sub-	LV on-det	LV Rim	HV	-	comment
Gas channel	itself	8 included	-	-	-	-	32 included	-	lose 1 layer from 8 sectors
Gas sub-channel	-	itself	-	-	-	-	4 included	-	1 layer affected
Cooling channel	-	-	itself	4 included	8 included	-	-	-	losing two half sectors. Other halves can still operate
Cooling sub-channel	-	-	-	itself	2 included	-	-	-	losing half wedge. Rest can operate
LV on-det channel	-	-	-	-	itself	-	-	-	
LV Rim channel	-	8 included	-	4 included	8 included	itself	8 included	-	assuming loss of both Rim LV channels (unlikely)
HV channel	-	-	-	-	-	-	itself	-	
Cooling channel (Rim)	-	-	-	32 LV channels (dig/ana)	2 RimTrigger	-	-	-	LV channels depend on which ICS is affected
36Fiber-bundle (L1)	-	-	-	-	-	-	-	-	lose a sector side (readout), but still have trigger
36Fiber-bundle (Rim)	-	-	-	-	-	-	-	-	from other technology!
Ground cable	-	-	-	-	-	-	-	-	we care?

Figure 3.48: Table showing the initial study of operation automation requirements and restrictions for services channels grouping.

Chapter 4

Detector Control System developments

ATLAS is one of the largest experiments at the LHC. Control, configuration and monitoring of all the systems along with the experimental infrastructure is required. This is carried out by the ATLAS Detector Control System (DCS). The basics and infrastructure of the ATLAS DCS will be described in this chapter. Some more information will be given for the MDT and CSC subsystems, which were supported for throughout the duration of this PhD. Furthermore, the incorporation of the Slow Control Adapter (SCA) ASIC into ATLAS DCS will be discussed. This includes development of a C++ software to allow communication from the control room to the SCA chips in the front-end electronics.

4.1 General

The term **SCADA** (supervisory control and data acquisition) refers to a category of industrial control systems. Using local controller units, which monitor and control a particular infrastructure, connected to a central station, the information is communicated locally or remotely through the network. The Joint Control Project (**JCOP**) is a committee, formed to define the frame of SCADA usage at the four large LHC experiments. Its mission is the selection, development and maintenance of the necessary tools, used by the experiments. Initially, in 1999, the PVSS package was chosen as the development tool. After a series of corporate-based actions, the Siemens company is now offering **WinCC-OA**, previously known as PVSS. Note that WinCC is not a control system itself, but merely the development tool (IDE) allowing to create control systems. This allows specific software development allowing running instances in distributed systems, using interdependent control processes (managers), running custom scripts, creating panels for control and data visualization (e.g. alarm screens) and data storage in databases.

4.2 ATLAS DCS

The DCS infrastructure starts at the detector, with electronics that read/assert signals on the front-end electronics (e.g. SCA [19], ELMB [20]). This communication path follows the read-out data to the service cavern for pre-processing and distribution to servers. Then, the servers handle the DCS data between

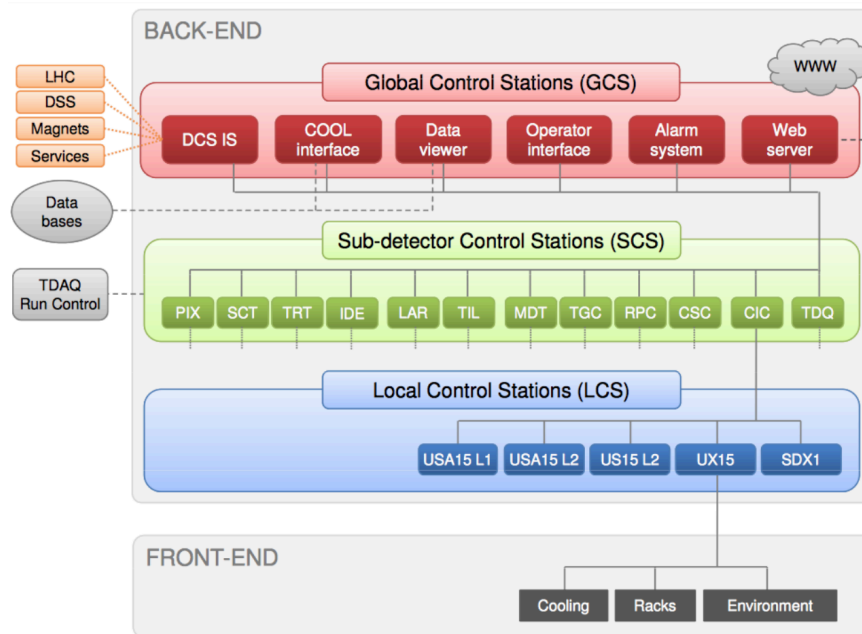


Figure 4.1: The ATLAS DCS system (by Stefan Schlenker).

themselves and the clients, which usually sit in the control room. This is where the final user (shifter) operates the GUI.

The ATLAS DCS was developed within the JCOP framework. Figure 4.1 shows a diagram of the system, split into Front-End (FE) and Back-End (BE). The FE is the detector hardware and infrastructure, while the BE is the software running on the computers, communicating with the FE. The main communication protocols are CAN [21] and OPC-UA [22].

The BE part is organized hierarchically in three layers:

- The Local Control Stations (LCS), that represent the local back-end which are responsible for the connection and readout of the subsystem front end.
- The Sub-detector Control Stations (SCS) perform the high-level control of a sub-detector allowing its standalone operation.
- The Global Control Stations (GCS) combines all the subsystems into a common ATLAS DCS and offers a high-level supervision of the full tree through service applications and operator interfaces.

Finite State Machine (FSM)

An FSM or simply a state machine, is a mathematical model of computation. It is an abstract machine that can be in exactly one of a finite number of states at any given time. The FSM can change from one state to another in response to some external inputs; the change from one state to another is called a transition. An FSM is defined by a list of its states, its initial state, and the conditions for each transition.

The ATLAS DCS FSMs are created and modified via the JCOP FSM toolkit. The original State Manager

S	Dir.	Description	Alarm text	Online Value	Ack	Time	Col
W	CAME	TGC A THRESHOLD M2 sector08 phi3 E4 L1 thresholdw00 not reporting	WARNING	15		2018.11.27 12:21:26.502	
W	CAME	RPC Sector 14 Vpd BOG0_14	Channel OverCurrent	9		2018.11.27 12:22:08.815	
W	CAME	RPC Sector 8 Vpd BMS3C08	Channel OverCurrent	9		2018.11.27 12:22:28.564	
E	CAME	TGC A THRESHOLD M2 sector08 phi3 E4 L1 thresholdw00 not reporting	ERROR	15		2018.11.27 12:23:36.697	

Figure 4.2: An example of a DCS alarm screen.

concept employs the SML language [23] for defining the object model along with states, actions and associated conditions.

Each FSM node has a unique **name** based on the subsystem name and its functionality following the ATLAS DCS conventions. The **state** is defined internally in the software. The FSM object **type** defines the basic functionality of the node and its sub-elements.

Using the JCOP FSM toolkit, the following types are defined:

- The Device Units are the low-level interfaces with the hardware and provide its actual state and status. This is achieved through direct hardware readings.
- The Logical Units are found one level higher, composed of several Device Units (children) and their states/statuses are the result of boolean calculations on the children's states.
- The Control Units are similar to the previous types, except that their functionality is governed by a control script that runs on the background and implements more complex state determination decisions on top of the boolean expressions based on their sub-elements.

In ATLAS DCS, units are structured in a tree-hierarchy. The top node shows the global state, while the lower levels are the detector sub-systems, followed by detector sub-groups etc. The tree hierarchy handles the state changes bottom-up. This means that when a node state changes, this is propagated to all parent nodes. The control commands, however, are handled top-to-bottom. This means that when a particular command is triggered by the user on a node, then this command is also passed on to all children, where applicable. The most usual states in the ATLAS DCS FSM are READY, STANDBY, NOT_READY, SHUTDOWN, TRANSITION and UNKNOWN. This set of states and commands is common within ATLAS, in order to improve the user experience in the control room.

Alarm screen

The alarm screen is a panel used in ATLAS DCS, along the main FSM one, in order to show at each moment which alarms are active or need attention (Fig. 4.2). These alarms may originate from any high/low-level node and can have three values of severity (WARNING, ERROR, FATAL). The alarm screen is important for the shifters and experts observing the FSM, to immediately know the content and origin of a current malfunction of a system.

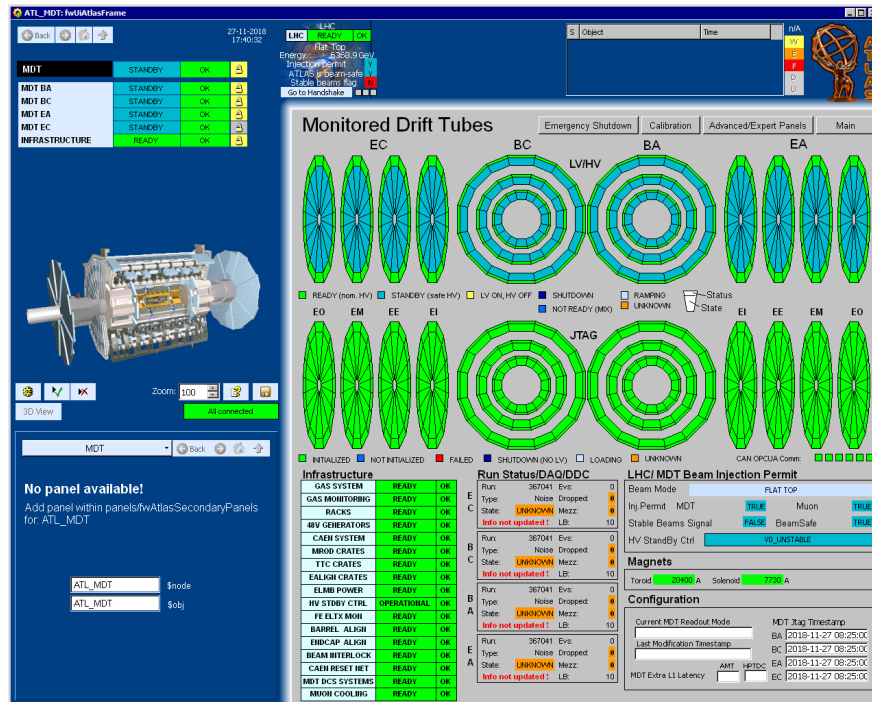


Figure 4.3: The MDT DCS FSM panel.

4.2.1 Muon DCS

The Muon DCS includes the muon sub-detector FSM panels, CSC, MDT, TGC and RPC. After LS2 it will include a NSW node as well (see FSMs in Fig. 4.3, 4.4). The main panels show an overview of all chambers of the barrel and end-cap. The overview is color-coded, showing the status of the HV, LV and electronics configuration. When not in a collision run, the HV is usually in STANDBY, which represents a value slightly lower than the normal operational. This is done in order to prevent unwanted discharges in the detector, which could come from high energy stray beam protons during beam stabilisation. The LV and configuration should go to READY when the warm start is finished, that is when the main ATLAS DAQ partition is prepared for data taking. The infrastructure nodes refer mostly to rack control, such as gas mixer and distribution systems, power supplies for ELMB and generators. When the NSW will be included in the system, similar panels will be developed. Examples are shown in Fig. 4.5, 4.6, 4.7.

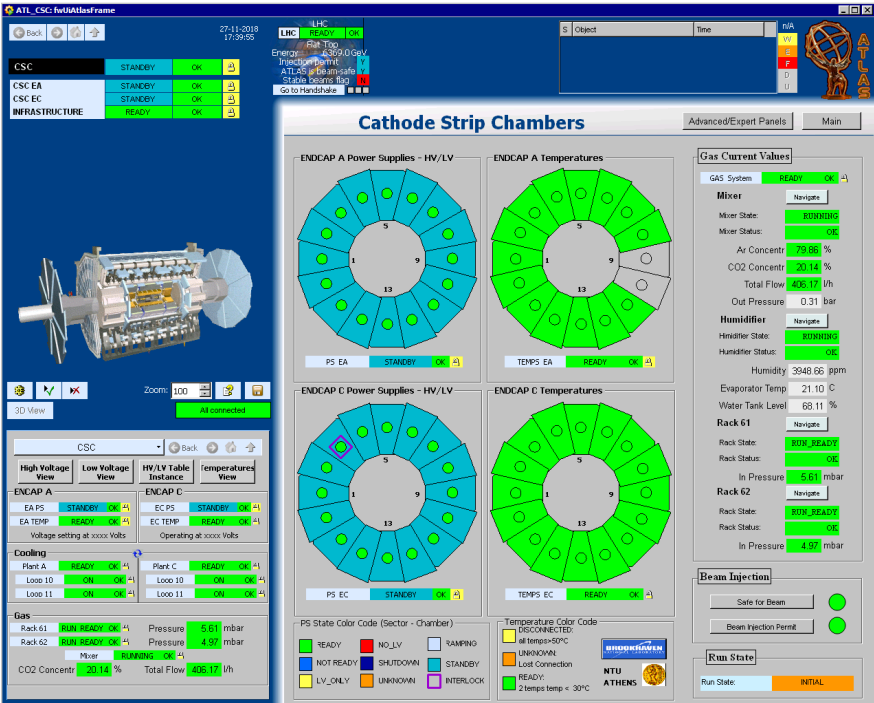


Figure 4.4: The CSC DCS FSM panel.

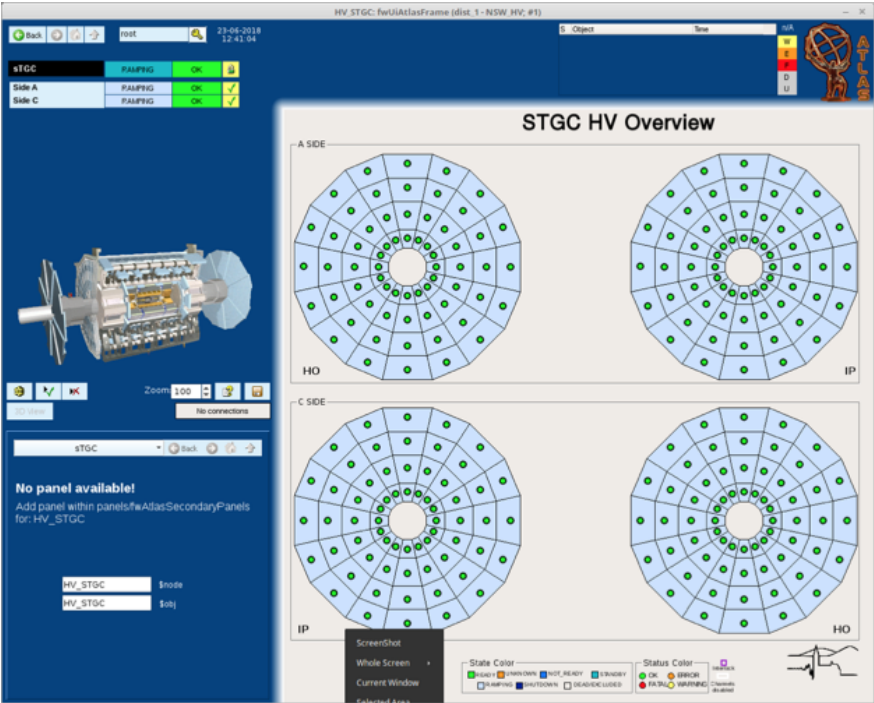


Figure 4.5: An example concept of the sTGC DCS FSM panel.

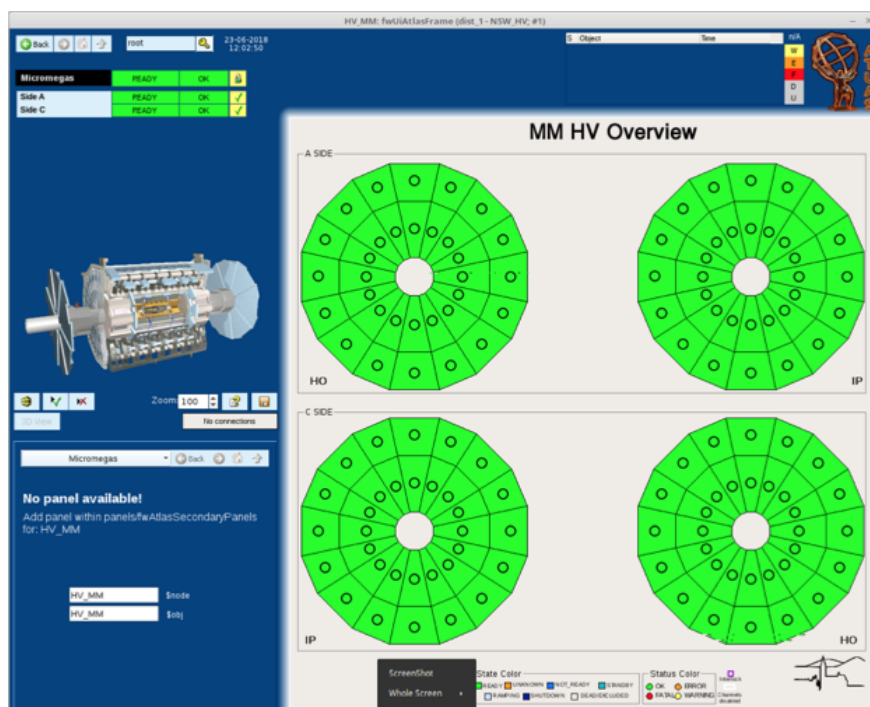


Figure 4.6: An example concept of the Micromegas DCS FSM panel.

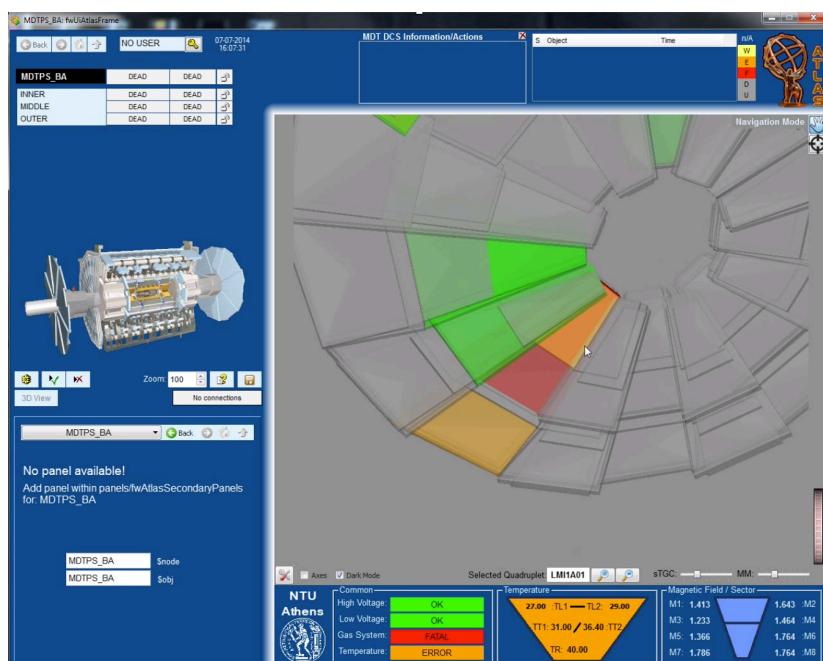


Figure 4.7: An example concept of the NSW DCS FSM panel, incorporating 3D viewer [24].

4.2.2 Current solution: ELMB



Figure 4.8: Two MDM boxes with ELMB, side by side. Each has two slots for B-field sensors, 30 slots for temperature sensors, and a few more slots for JTAG and SPI communication. Connection is based on CANbus, and allows daisy-chained schemes [20].

The current front-end solution for DCS operations of the Muon collaboration is the ELMB-based MDM box (Fig. 4.8). The Embedded Local Monitor Board (ELMB) [20] is a plug-on board, general-purpose CAN-bus based building block for control and monitoring tasks in the LHC experiments. The ELMB's low cost and low power consumption have made the ELMB the solution of choice in a wide variety of control and monitoring applications. For the LHC experiments around 10000 pieces have been produced.

Given the scale of electronics at the NSW, the ELMB is not a viable option, except for the environmental monitoring. Instead, the SCA is used, as an integrated circuit, described in a next section.

4.2.3 OPC-UA and Quasar

OPC-UA is the interoperability standard for the secure and reliable exchange of data in the industrial automation space and in other industries. The OPC Foundation is responsible for the development and maintenance of this standard, since the 90s. Due to increasing needs of service-oriented architectures in manufacturing systems and new challenges in security and data modeling, OPC UA was developed with specifications to address these needs and provide an open-platform architecture that was future-proof and scalable.

Quasar The quasar framework is a collaborative, open source effort, for rapid, model-driven development of OPC-UA servers. This framework was used for the server development of the SCA, as will be further described below.

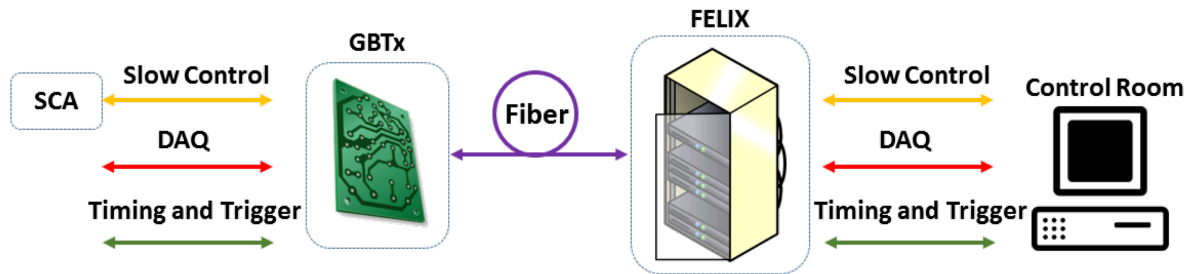


Figure 4.9: GBT simplified scheme.

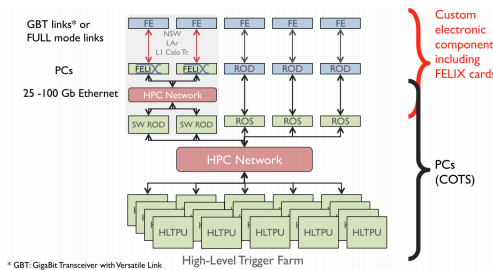


Figure 4.10: FELIX along the existing read-out scheme.

4.2.4 Upgrade and Development

ATLAS DCS needs to grow, following the detector closely. The increasing demand for data through-put comes with an increase in the need to monitor and control the electronics that handles all the through-put. For this reason, a new family of chips is introduced, to provide a new generation of electronics to achieve the goal. This is the GBT family of chips; developed by the CERN-EP-ESE group for usage in the large experiments.

The GBT Project

The “GBT Project” is part of the “Radiation Hard Optical Link Project” [25] which aims at developing a radiation hard bi-directional optical link for use in the LHC upgrade programs. The link targets data transmission between the on-detector and off-detector electronics serving simultaneously applications such as data acquisition, timing, trigger and experiment control. The GBT Project itself aims at the development of radiation hard chipset that will allow the implementation of such a link. The project aims also at the development of HDL code to enable FPGAs to interface directly with the links based on the GBT chip set. Following Fig. 4.9, the GBT ASICs are targeted primarily for the front-end electronics (GBTx, SCA etc), while the firmware counterpart runs in the service cavern (non-hostile environment) on back-end machines (FELIX). Further communication is then based on standard network infrastructure.

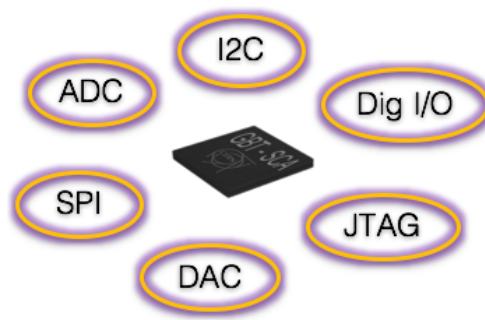


Figure 4.11: Sca feats

1615 Front-end Link Exchange (FELIX)

For the Phase-I upgrade of ATLAS, some 2000 new fibers are introduced, which require a new system for readout. As in [26] and Fig. 4.10, the new system, FELIX, is combining functionality from the RODs and partly from the DCS PCs.

- **Readout** is done by direct fiber connection to the front-end GBT-aggregator boards (for NSW: L1DDC). Event fragments are assembled and forwarded to the software read-out drivers (swROD).
- **Timing** and control (TTC) also passes from FELIX. The clock is distributed through fibers to the front-end GBT chips.
- **Configuration** data and **monitoring** requests reach FELIX to be forwarded to the same electronics, to be distributed appropriately later downstream (e.g. SCA)

1625 4.3 The Slow Control Adapter ASIC

The Slow Control Adapter GBT-SCA ASIC, part of the GBT chip-set, developed by CERN-EP-ESE, is made for distributing control and monitoring signals to the on-detector front-end electronics, as well as performing monitoring operations of detector environmental parameters. In order to make it a good communication hub for various front-end ASICs used in the experiments, it provides various user-configurable interfaces capable to perform simultaneous operations. It is designed employing radiation tolerant design techniques to ensure robustness against SEUs and TID radiation effects and is implemented in a commercial 130 nm CMOS technology.

4.3.1 SCA features

The SCA principally connects to an electrical port of a GBTx, with an expected rate of 80Mb/s. The slow control packets, meant to reach the SCA, are packed within the GBT frames on the counting room side (FELIX). Upon arrival at the GBTx, the data is decoded and sent to the SCA. Two e-ports are available, for redundancy. The clock also arrives through these ports.

The interfaces provided are:

- **GPIO:** provides 32 general purpose input/output channels of programmable lines (voltage high is 1.5V)
- **I2C:** 16 independent I2C master channels, each with programmable transmission speed and address mode.
- **SPI:** One master line with eight SPI slave channels, similarly programmable.
- **JTAG:** One master channel allowing single transactions of 128 bits, up to 20MHz (not including a JTAG state machine).
- **ADC:** Includes 32 multiplexed inputs to a 12-bit Analog-to-Digital Converter (ADC). 31 are usable, while one reads a temperature sensor. Offset cancellation and gain correction logic is included.
- **DAC:** Four channels, able to produce voltage of up to 1V, with 8 bit resolution.

Communication and frames

Communication is established through the e-ports, accomplishing so called electronics links (e-link). The protocol is described with the SCA frame, which is packaged on the GBTx (from GBT frame chunks). As in Fig. 4.14, the SCA frame is based on the HDLC protocol, with start-of-frame and end-of-frame bytes surrounding the address, control, payload and frame check sequence.

4.3.2 SCA in ATLAS and NSW

The SCA was introduced, along with the GBT family, aiming the Phase-I upgrades of the large LHC experiments. For ATLAS, the first users are NSW and BIS78. The NSW has SCA chips on all front end boards for the configuration of the front-end ASICs. In some additional cases for FPGA or other configuration, SCAs are found on-detector, but downstream. Specifically, the use cases are briefly listed below.

Front end boards

- **VMM SPI configuration:** A single VMM chip expects a set of bits for setting global registers as well as channel specific. Namely. this configuration is sent through SPI, in 18 groups of 96 bits.
- **ROC I2C configuration:** The Read-Out Companion ASIC configuration includes setting latency and trigger window width, among others, as well as elink speeds and other timeouts.
- **TDS I2C configuration:** Some 1300 bits of configuration, including BCID offset, clock phase and channel enables.
- **ADC calibration and voltage monitoring:** On each VMM channel there is an ADC which needs to be calibrated with respect to the incoming signal. This will be accomplished by measuring the counts on the VMM and comparing to the SCA ADC, in order to define correct thresholds and the internal ADC linearity.

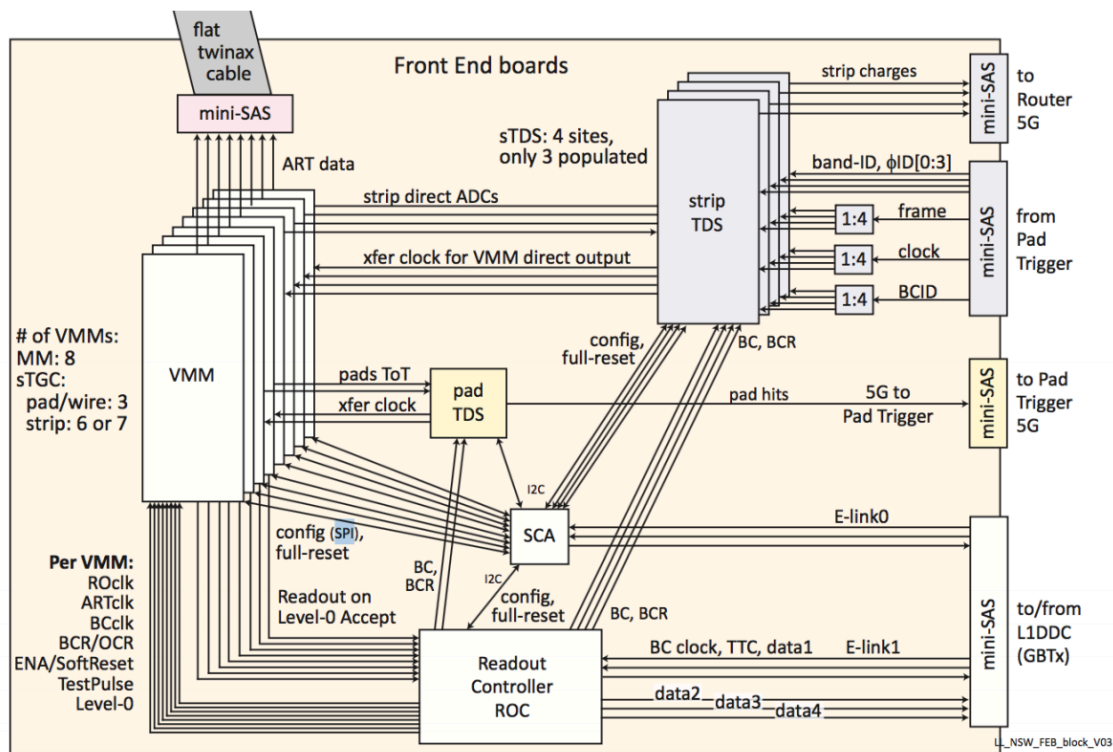


Figure 4.12: Connectivity scheme on the FEBs (by Lorne Levinson).

- location ID with GPIO: A few unused detector strips are routed to the GPIO lines of the SCA, in order to be used later for location identification, depending on the strips combination.

Aggregator and Trigger boards

- ART I2C configuration: On the ADDC, the ART chip receives through configuration the configurable dead-time per channel.
- GBTx and VTTX I2C configuration: In some cases, the GBTx can be configured through the IC bits in the GBT frames, however I2C can also be used, to write 8-bit words on addressed registers.
- Temperature monitoring with ADC.
- LV monitoring with ADC.
- FPGA programming for Router (Artix7) and PadTrigger (Kintex7) boards, using standard JTAG connection, following Xilinx (c) FPGA protocol.

4.3.3 Communication protocol

GBT frame

1685 The GBT frame is a fixed 120-bit packet delivered with a rate of 4.8Gbps. Four bits are used for the frame header (H), two for internal GBT control and configuration (IC), two for external control (SCA, EC) resulting in the fixed 80Mbps rate, 32 for forward error correction (FEC) and 80 bits for user data (D).

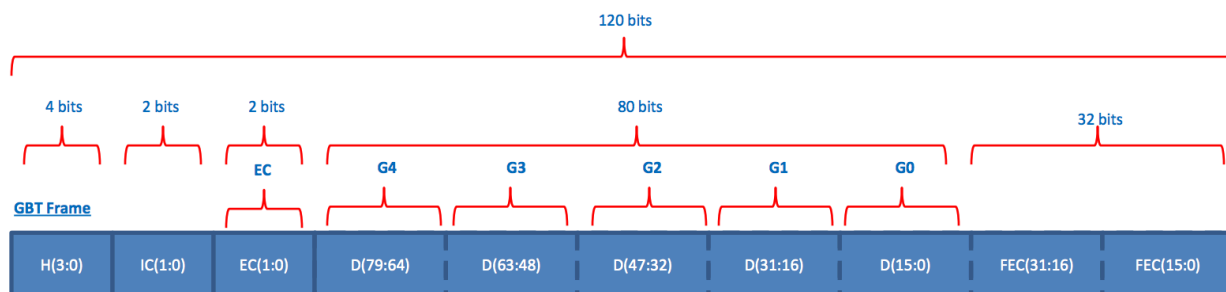


Figure 4.13: The GBT frame [25].

SCA frame

1690 The SCA frame is part of an HDLC frame which is exchanged between the GBTx and the SCA. The HDLC includes start- and end-of-frame bytes, along with address (not used), control (not used) and frame check sequence (FCS) bytes. The data is engulfed in the frame in pairs of bytes.

1695 The protocol for the SCA simply includes a transaction ID number, which increments at every transaction, in order to allow the user to control the received replies from the chip. Then there is the channel ID which is unique for each SCA interface (e.g. GPIO, SPI). One channel ID is reserved for the SCA node commands, which are the SCA internal configuration commands, such as reset. The frame also includes a length byte denoting the number of bytes included in the data field. Last, there is a command byte, which corresponds to a specific command of the defined channel. For example, the JTAG_GO command is 0xA2. The replies have an error byte instead of command denoting potential errors in execution of the command.

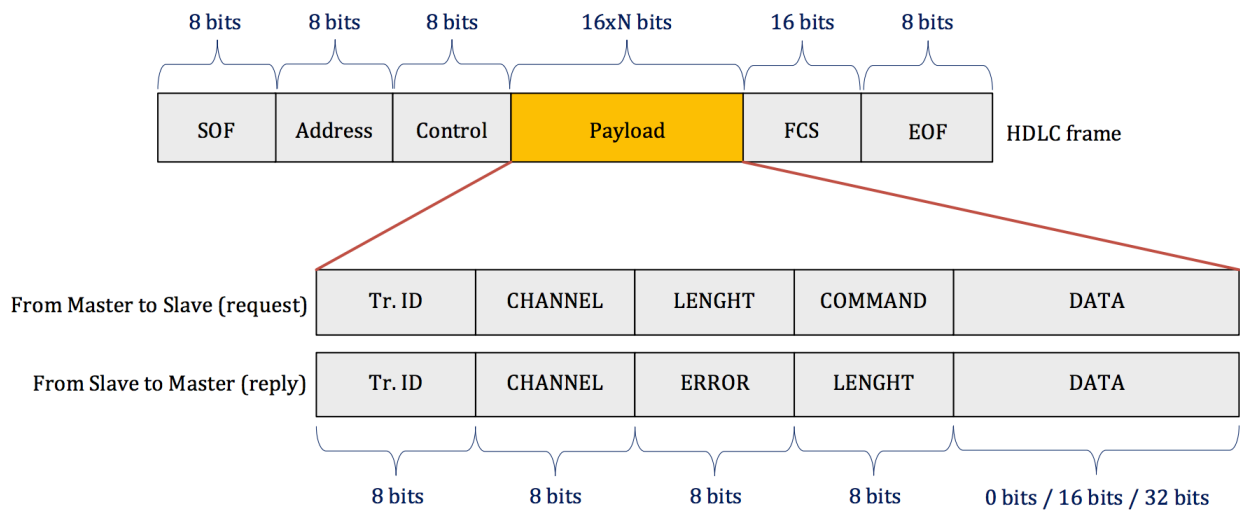


Figure 4.14: The SCA frame [27].

4.4 SCA Software

[disclaimer]The SCA Software library as well as SCA OPC-UA server that is referred to in this thesis is an effect of work of multiple persons including Paris Moschovakos, Stefan Schlenker, Piotr Nikiel, Henk Boterenbrood. The contribution of the author of this thesis is in extension of SCA Software as well as the OPC-UA server to support GPIO, DAC and partly JTAG components of the SCA chip. Part of the work was presented in [28].

The SCA offers a collection of communication interfaces (Fig. 4.12), each with its own protocol, registers and configuration. The ScaSoftware is used to prepare SCA frames (Fig. 4.14), to be sent to a designated back-end. Each interface class provides "get-set-go" methods for the respective channel (e.g. SPI). These methods assemble commands into frames with the corresponding binary words and channel addresses. The code lives in gitlab (<https://gitlab.cern.ch/atlas-dcs-common-software/ScaSoftware>).

An example usage can be seen below, as part of a demonstrator. A new SCA object is created, which contains objects from the interface classes, which will pass the commands to that SCA object, to be sent to the selected backend (as seen in the constructor of SCA).

```
//config is a struct defined from the program options
Sca::Sca sca ( config.address ) ;
//the gpio object method 'setRegister' used to set direction of
//all pins to output
sca.gpio().setRegister (::Sca::Constants::GpioRegisters::Direction ,
0xffffffff);
//the direction of pin 10 is written to the variable testValue
uint32_t testValue = sca.gpio().
getRegisterBitValue (::Sca::Constants::GpioRegisters::Direction ,10);
```

Available backends have been:

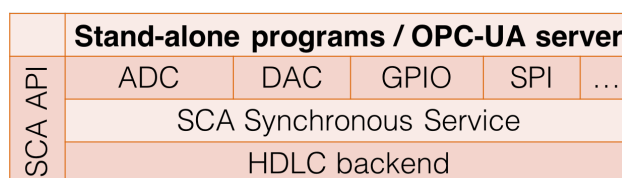


Figure 4.15: SCA Software simplified architecture (image by Piotr Nikiel).

- **ScaSimulator:** This is part of the delivered ScaSoftware. It consists of a set of classes, which emulate the expected responses of the SCA, as understood from its design [19]. Useful for initial debugging and demonstrators.
- **Genesys board (USB):** Used during first stages of development, as it was the only available hardware equipped with SCA.
- **Netio:** This is the network library used by the FELIX software, which runs on the FELIX machines [29].

The main classes are briefly described below:

- **SCA:** This is the base class, an SCA object .
- ***Impl:** The implementation of the base methods for each interface (*). Example: JtagImpl.cpp.
- **Synchronous Service:** This class provides the connection between the SCA Software and the selected backend through the base method "SendAndWaitReply".
- **Backends included:** mentioned above.

4.4.1 The interface classes

SCA

The main SCA object class includes registering all channels in the synchronous service, trying to read the chip ID and offering methods to disable channels in the service.

Implementation classes

For each interface there is an implementation class, e.g. I2cImpl.cpp, which includes the basic getter and setter methods for the interface. Each interface includes configuration registers which can be set from these classes. Communication interfaces include methods for communication settings but also for giving the chip the command to actually initiate transmission (e.g. JTAG-GO).

GPIO

1745 The General Purpose Input/Output interface (GPIO) of the SCA has 32 pins which can be set as input or output, and accordingly read or written. The configuration registers on the chip are:

- DATAOUT: It drives the GPIO pins, as long as they are defined as output.
- DATAIN: It stores the value of the GPIO pins, as long as they are defined as input.
- DIRECTION: Drives the direction of the GPIO pins. Logical '1' is output, while '0' is input.
- 1750 • INTENABLE: Can allow the GPIO interface to trigger Interrupt signals downstream.
- INTSEL: Sets the pins to be allowed or not to act as interrupt signals (input pins only).
- INTTRIG: Defines on which clock edge a pin will generate the interrupt signal.
- CLKSEL: Defines if the chip runs on the internal 40MHz clock or an external strobe coming from a dedicated pin.
- 1755 • EDGESEL: Defines the external strobe edge used to latch the data.

The software allows the user to set pins' direction or value, as for all registers. Also ranged commands are available.

DAC

1760 The Digital-to-Analog Converter interface of the SCA comprises four sub-channels, which are independent converters. The measurement resolution is 8 bits, which means that the converter can have $2^8 = 256$ different levels along its range. The voltage level output range is [0..1V]. The input value 0x00 corresponds to 0V output, while 0xFF to 1V.

In the lab, we have measured that the value 0xFF gives about 1.1V, which was later corrected in our software, to allow more precise operation.

1765 data here:

The software provides methods for setting each of the four channels. In addition, there are user functions for directly setting a particular voltage level, letting the software calculate the correct binary input. Finally, there is also a step function, which increases the previous set value by one bit, thus providing the smallest available increase in the converter output.

1770 JTAG standard

JTAG (named from the Joint Test Action Group which established it) is an industry standard for verifying designs and testing printed circuit boards after manufacture, also widely used for configuration and monitoring of FPGAs.

The signals that comprise the standard are four: TDO, TDI, TMS and TCK.

- 1775 • TDO is the digital line which is the output of a node.

- TDI is the input digital line on a node.
- TMS is the state clock, which determines when a state should change or not.
- TCK is the clock, which needs to be sent whenever the user wants the JTAG client to parse the incoming TMS/TDO and potentially act on the TDI.

1780 JTAG usually has a master node which drives the clock and the JTAG slaves, which in our case is only one, but in many cases they are daisy chained into a series of nodes, each taking as TDI the TDO of the previous node.

Programming a particular FPGA is done through a series of steps. In our use, we have the Virtex7 series, which expects the steps shown in table [4.16](#).

TAP Controller Step and Description		Set and Hold		# of Clocks
		TDI	TMS	TCK
1.	On power-up, place a logic 1 on the TMS, and clock the TCK five times. This ensures starting in the TLR (Test-Logic-Reset) state.	X	1	5
2.	Move into the RTI state.	X	0	1
3.	Move into the SELECT-IR state.	X	1	2
4.	Enter the SHIFT-IR state.	X	0	2
5.	Start loading the JPROGRAM instruction, LSB first:	01011 ⁽⁴⁾	0	5
6.	Load the MSB of the JPROGRAM instruction when exiting SHIFT-IR, as defined in the IEEE standard.	0	1	1
7.	Place a logic 1 on the TMS and clock the TCK five times. This ensures starting in the TLR (Test-Logic-Reset) state.	X	1	5
8.	Move into the RTI state.	X	0	10,000 ⁽¹⁾
9.	Start loading the CFG_IN instruction, LSB first:	00101	0	5
10.	Load the MSB of CFG_IN instruction when exiting SHIFT-IR, as defined in the IEEE standard.	0	1	1
11.	Enter the SELECT-DR state.	X	1	2
12.	Enter the SHIFT-DR state.	X	0	2
13.	Shift in the FPGA bitstream. Bit _n (MSB) is the first bit in the bitstream ⁽²⁾ .	bit ₁ ... bit _n	0	(bits in bitstream)-1
14.	Shift in the last bit of the bitstream. Bit ₀ (LSB) shifts on the transition to EXIT1-DR.	bit ₀	1	1
15.	Enter UPDATE-DR state.	X	1	1
16.	Move into RTI state.	X	0	1
17.	Enter the SELECT-IR state.	X	1	2
18.	Move to the SHIFT-IR state.	X	0	2
19.	Start loading the JSTART instruction (optional). The JSTART instruction initializes the startup sequence.	01100	0	5
20.	Load the last bit of the JSTART instruction.	0	1	1
21.	Move to the UPDATE-IR state.	X	1	1
22.	Move to the RTI state and clock the startup sequence by applying a minimum of 2000 clock cycles to the TCK.	X	0	2000
23.	Move to the TLR state. The device is now functional.	X	1	3

Figure 4.16: The JTAG message steps, taken from the Xilinx document "7 Series FPGAs Configuration". Find it [here](#)

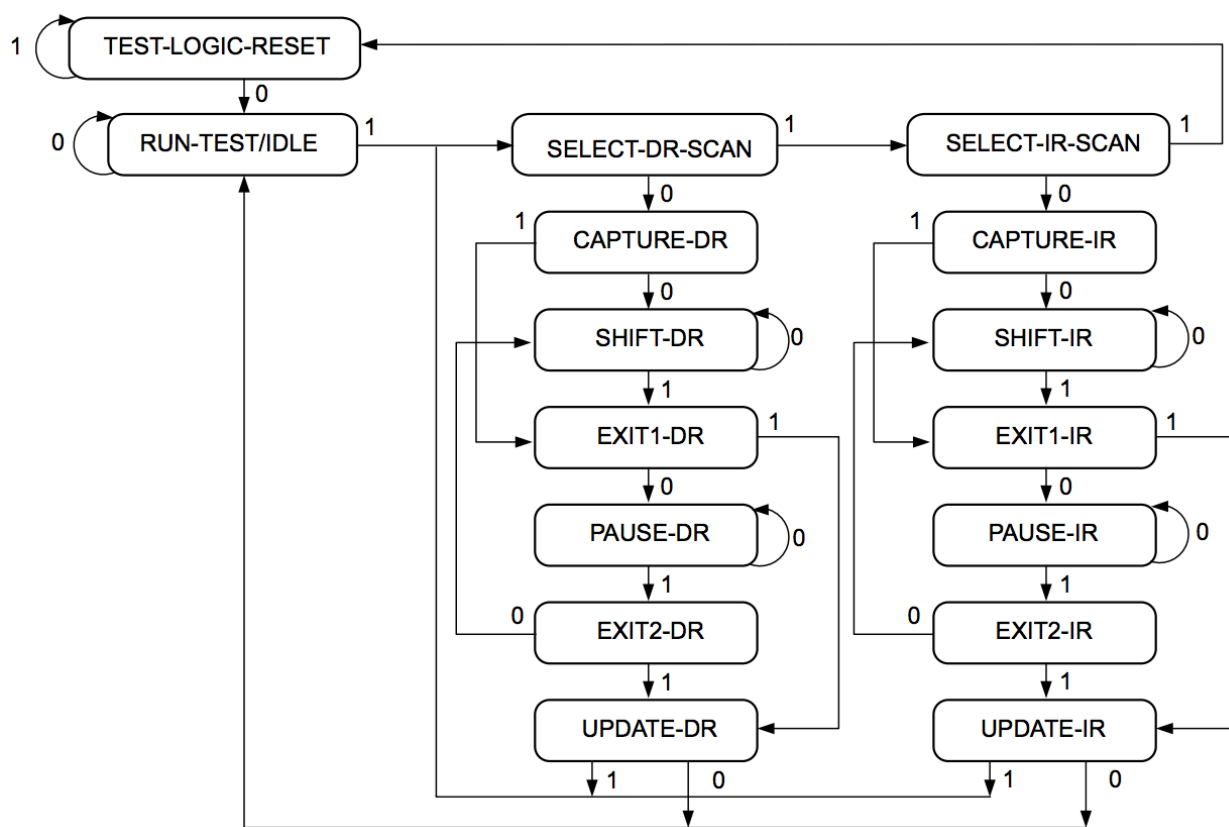


Figure 4.17: The JTAG states including the required TMS values for advancing to the next, taken from the Xilinx document "7 Series FPGAs Configuration". Find it [here](#)

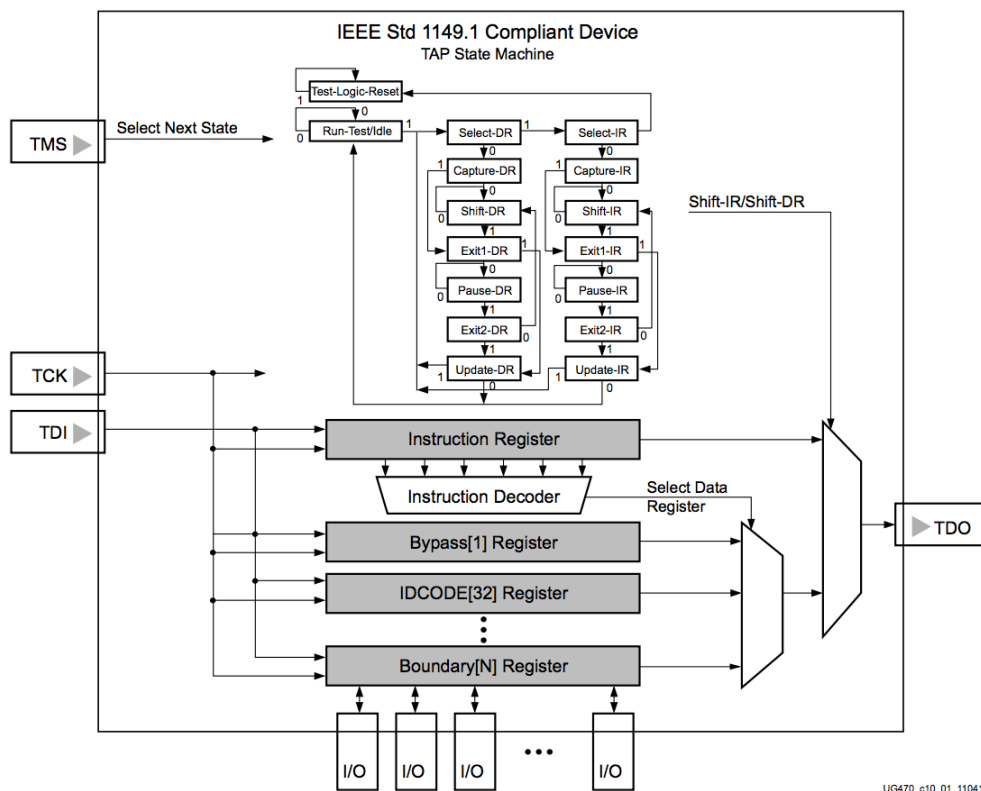


Figure 4.18: The JTAG state machine of each slave node is connected to the internal boundary registers, as shown here. According to the instruction sent to the node, the appropriate data register is passed on the TDO (taken from the Xilinx document "7 Series FPGAs Configuration". Find it [here](#))

1785 According to the JTAG operation mechanisms shown in this subsection, the software had to accordingly follow the steps to arrive to a programmed FPGA. The lower level commands were used to send grouped bits on TDO and TMS, while the TCK is handled by the Sca chip itself.

Unfortunately, the implementation did not work as expected, which is why in the end we used Henk Boterenbroods's code for the higher level part.

1790 4.4.2 Synchronous Service

Since the SCA chip can only process one command at a time, we should only send one command at a time. For this reason we have the SynchronousService class, which provides a center node for all channels to send requests and commands to the SCA, while getting replies from that same node. This service includes a nested class, SynchronousChannel, which is the actor for allocating the Transaction IDs (TID).

4.5 OPC-UA SCA server

An OPC-UA server was developed, using Quasar, in order to provide a node of communication between the OPC-UA clients in the control room and the FELIX machines which exchange all messages with the front-end. This server will run either on a separate machine, or more likely on the FELIX machine in order to eliminate delays. The architecture is mostly pre-defined by the Quasar design, while allowing extension of the code, mainly for higher level command grouping. The server uses the SCA Software in order to send "smarter" groups of commands, as requested by the client. For example, when configuration of a few thousand VMM chips is requested by the client, then the server finds the appropriate configuration info from the database, and knows to call all the right SCA Software commands to send the appropriate SPI commands upstream. The OPC-UA server code lives in <https://gitlab.cern.ch/atlas-dcs-opcua-servers/ScaOpcUa>.

The main classes developed are shown in the diagram of Fig. 4.19. Each box denotes a class, and the arrows are showing subsequent classes. Each class arrow is followed by a range of allowed instances of this object.

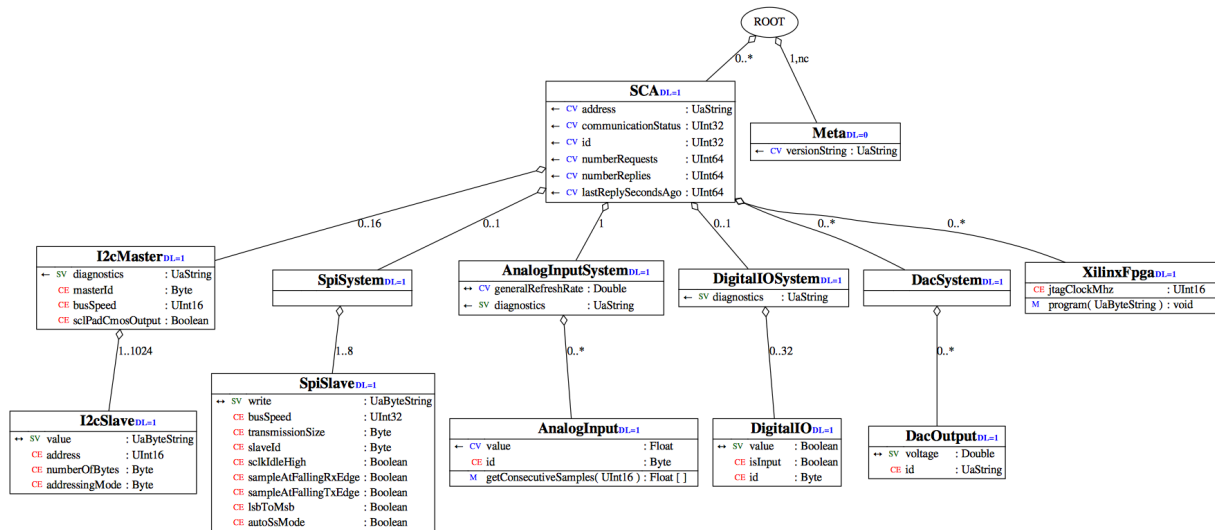


Figure 4.19: The OPC-UA server diagram, as produced by Quasar (2018).

These classes are created based on a configuration .xml file, which corresponds to the hierarchy shown in the diagram. The constraints and variable types are defined in the same file. Then, Quasar prepares the Device classes accordingly for each device (i.e. Sca, or Sca interface).

For example, the DAC device **system**, as prepared by Quasar, is merely a parent class to the DacOutput, which includes the code implementation of "mapping" user-level commands to ScaSoftware functions. The function used to read the voltage on a particular DAC channel is shown below.

```

UaStatus DDacOutput::readVoltage (
    OpcUa_Double &value ,
    UaDateTime &sourceTime
)

```

```

{
    sourceTime = UaDateTime::now();
1820    try
    {
        value = sca()->dac().getVoltageEstimateAtRegister( m_id );
        return OpcUa_Good;
    }
1825    catch (std::exception &e)
    {
        LOG(Log::ERR) << "In reading back the DAC output: " << e.what();
        return OpcUa_BadOutOfService;
    }
1830 }

```

4.5.1 Testing and operating the software

The Sca Software and the OPC-UA server have been tested in the lab on many occasions, at the New Small Wheel Vertical Slice lab setup.

4.6 Use cases

1835 During commissioning and operation of the NSW, we will need to use the SCA for calibration, configuration and monitoring processes. Here we will describe the method for these operations, thus indicating the use cases of the SCA chip in the NSW upgrade and the other upgrades of ATLAS.

4.6.1 Calibration

1840 The main calibration operation for the NSW is that of the VMM chip. The VMM includes a number of converters (DAC and ADC), which need to be understood in order to properly interpret the signal. There is possibility for the VMM to internally route analog signals to its "monitor output" (MO) for direct measurement by scope or external ADC. In the final NSW case, the external ADC is one of the interfaces of the SCA, which is calibrated after production and before integration on the front-end boards. Technical details can be found in the specification of the VMM chip [30].

1845 The VMM calibration procedure includes the following steps:

- Threshold DAC calibration: The VMM has the possibility to apply thresholds to the analog signal input. Intrinsic noise or misbehaving strips need to be taken into account when reading analog signals. So, to avoid reading out the noise, we need to apply a threshold. If the incoming signal is lower than the threshold it is ignored (except neighbour logic, mentioned in uTPC analysis chapter). In the VMM, 1850 this is set using the threshold DAC, which applies to all channels on a VMM chip.

First, the threshold DAC is set to the monitor output of the VMM. Then the DAC set values are scanned (0-1024) and for each value the SCA ADC is read a few hundred times. The data, read-out through the

OPC-UA path, is stored into a histogram which can then be fitted with a line to identify the behaviour of the DAC. Such a histogram for each VMM allows extraction of the relation:

$$\text{DAC}_{\text{Th}} [\text{mV}] = f(\text{DAC}_{\text{th}} [\text{cnts}]) \quad (4.1)$$

- Take threshold run: The behavior of each channel needs to be understood. For this reason, we need to measure the raw signal that the channel sees, with the external ADC. This is done for each individual channel. One by one, we route a channel output to the monitor output of the VMM, and read the corresponding SCA ADC a few hundred times and fill the data in a histogram. The result will be a - hopefully - consistent random-looking distribution of the average response of this channel to "nothing". Normally one needs to reverse trigger incoming particles, in order to avoid reading real signals during the threshold run. In the testbeam, this is done thanks to a triggering setup of scintillators, which allows calibration data to be taken only when a trigger is not raised. For ATLAS, we will have to check how many cosmic muons pass, and potentially to use trigger info to reverse trigger appropriately.

The histogram result, which will look like Fig. 4.20, allows us to take a single value, the average value, to be set for the chip as threshold.

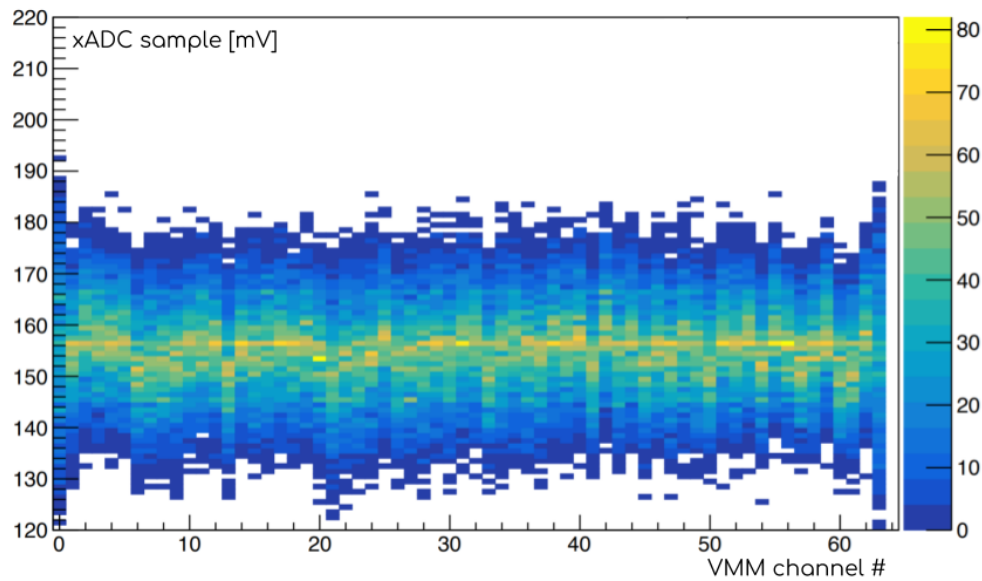


Figure 4.20: Histogram with the samples of each VMM channel on an SM2 chamber. The readout of the channel is routed to the external ADC

- Adjust trimmers run: The threshold setting is a coarse definition of the readout limit for all channels on a chip. The trimmers offer a fine adjustment of the threshold, channel by channel, in order to approach the correct threshold even more.
- Pulser DAC calibration: The final step before we complete the picture of the calibration, is the calibration of the pulser DAC. This internal pulser is used to inject a charge to the input of each channel. Since this also needs to be calibrated, it is routed to the VMM MO, and similar to the threshold DAC, we get a plot for every channel, similar to Fig. 4.21.

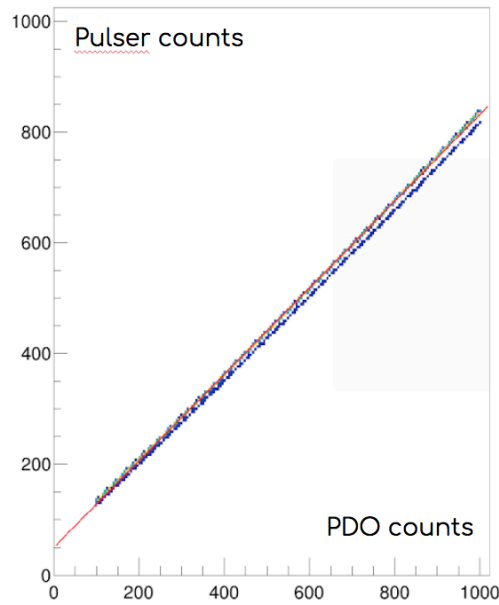


Figure 4.21: Histogram with the pulser DAC data, as read by an external ADC (xADC), fitted with a line.

- ADC calibration: Finally, the real VMM ADC calibration can be done, after all the internal steps mentioned. For every channel, having set the thresholds and trimmers, the pulser is activated and its range of values scanned. The channel response is set to come out at the monitor output of the chip, where it is measured by the SCA ADC. Thus, we end up with yet another plot, as Fig. 4.22 for example, from which we extract the last formula:

$$\text{ADC}_{\text{in}} [\text{mV}] = \text{ADC}_{\text{out}} [\text{PDOcounts}] \quad (4.2)$$

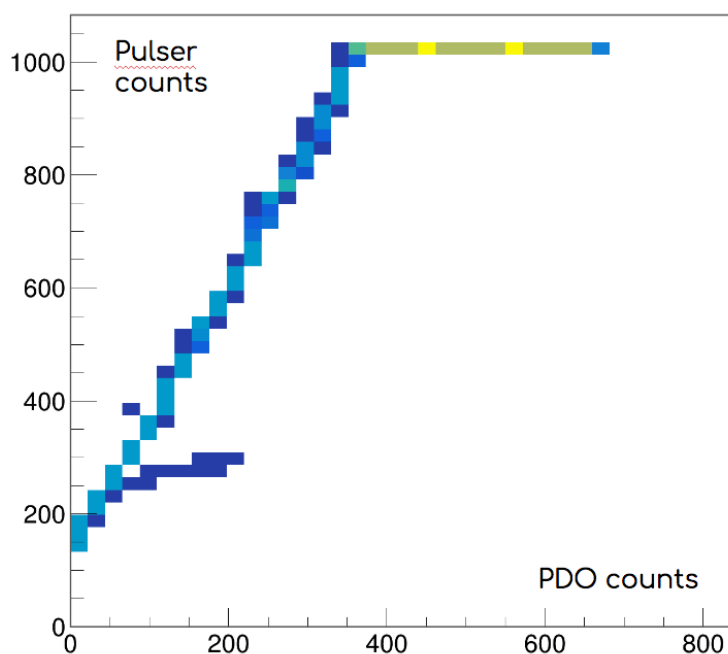


Figure 4.22: Histogram with the ADC data, as read by the VMM, sent out as PDO counts.

4.6.2 Configuration

It was already mentioned that the SCA is used for configuring front-end ASICs. The configuration files will be created during commissioning and in the first days of operation. Clearly as the detector operates longer, the configuration files will be adapted and optimised. Some configuration files will be stored in the configuration database OKS of ATLAS, or a similar maintained database.

The OPC-UA client from the control room provides to the OPC-UA server the location of the configuration file. Then the OPC-UA server loads the configuration file to memory and sends it to the SCA in many parts, as allowed by the interface limits.

The configuration is a single step operation, sometimes followed by configuration read-back for validation.

4.6.3 Monitoring

Periodic monitoring of the front-end electronics is clearly important to ensure good and controllable operation. The main operation consists of frequently sending read requests to the SCA ADC channels, those which are connected to temperature sensors.

One visible potential conflict here is that we constantly want to monitor temperatures and perhaps other voltages, but the ADC interface will also be used for calibration. Given the SCA design, where an interface is busy as long as it is in use, we could end up not having monitoring data during calibration for certain boards. The final implementation of the OPC-UA client and server will need to take such potential conflicts into account to ensure smooth operation and monitoring.

4.6.4 FEAST control

When the SCA features and their potential were starting to reflect on the requirements of the NSW upgrade, there was an issue raised concerning safety of electronics and improvement of low voltage risk management. Namely, the FEAST DC-DC converter, which is on-board most front-end electronics, can be enabled or disabled through an external pin, which can be set by an external general purpose I/O driver, for example the GPIO of the SCA. So, since it is possible for a single board to overheat or misbehave, it would be a pity to be forced to kill the entire voltage channel, including up to 8 boards. The alternative proposed was to use the SCA features to control the FEAST enable, for all on-board FEASTS, except the ones powering the SCA, obviously. In the end, this suggestion was not endorsed, given the already existing complexity in the design of the board, and in order to avoid the opposite risk, i.e. a misbehaving SCA denying power to a well-working front-end board.

Appendix A - Future ideas

...or what we would like to do if we had more time, money, summer students etc

A.1 Detector hardware

- 1910 1. Circular(+other) resistive strip to spread charge on RO strips. Experiment with different charge sharing media.
2. MM strip readout from both ends (probably need better elx). One VMM on one side reads the "pos pulses", and other VMM on other side reads the "neg pulses". Then we could take TDO diff, to extract 2nd coordinate with extreme precision.
- 1915 3. What if we use LAr for Micromegas. Drift velocity and/or ionizations are similar for LAr, as in gaseous Ar. Could make Calorimetric MM.
4. Micromegas, mapped on MDT surface, giving the MDT the precision coordinate on the plane that is missing. For MDT ref, see links [this](#), or [this](#).
- 1920 5. Micromegas HV stability debugging: Double pillar height, same amplification E-field (=> more uniform E-field lines).
6. Micromegas HV stability debugging: put many times (like 5x) more pillars, on a big chamber, to rule out mesh being too close to strips.
- 1925 7. Self-passivating Micromegas (or MPGD in general). Either with a special gas mix, OR with a particular thin layer over the resistive strips that passivates the area when "burned" by a spark. Perhaps similar to the carbon layer of TGC.

A.2 uTPC & analysis ideas

1. Heat-map of clusters (only 3-strip e.g.) to see how most clusters look. Make a 3-strip cluster heat map, with mid strip in the middle. and second highest strip to the right and see how diff/same all the clusters are. Study started as in MM chapter.

- 1930 2. Legendre transformation extensions for strip detectors. Like the MDT Legendre, but in 3D, not tracks, but ARCS (parametrize with 2 points, theta, and R. (one point is 0.0 perhaps) and the other is the under test, and theta, R = parameter space.
3. Instead of Hough, do it like in Reco: use tracking line to clean points.
4. uTPC performance study
- 1935 5. instead of Hough, do Kalman for finding tracklet/segment.
6. Remember MDT plot in this thesis (Fig. 1.5). Maybe something similar for MM. Rotating your axes, until you have a clear peak (when adding your hits) in a certain x' axis, which is the x axis, rotated a certain theta. Probably can be found very coarse first, and then redo finely (similar to fine R histogram as in uTPC method described above).
- 1940 7. Revisit expected signal approach (with Vinnie, Theo and Chara at Demokritos). From both MC of Chara and from the expected shape (somehow) we had this 2D function (expo) for the charge distribution over the strips. This distro, we were trying to map on the strips and make something out of it. But maybe what was wrong is that we were doing it 2D, while this should need a 3D rotation and then appropriate mapping on the strips. Need to do 3D rotation of the diffusion.

1945 A.3 Simulation

1. Wavelet simulation (see youtube video by SpaceX). Basically smart space meshing, only close to interesting areas. Applicable for simple HV simulation: but this is static so maybe not applicable. However, for Garfield can be used. Making fine mesh around the particles only. Maybe also for gas diffusion, can only simulate "edges".
- 1950 2. Detector signal simulation, lower level than what was done with Maxwell software. For example, Meep is a software that simulates signals on conductors on a lower level.

Appendix B - uTPC method for Micromegas

1955 The uTPC method has several applications and implementations as a pattern recognition mechanism, particularly for image processing and track identification. A particular implementation is shown here, applicable for tracking on a Time Projection Chamber (TPC), as used for Micromegas analysis. The inputs to the process are the active strips in the dimension we measure and their corresponding times of arrival. The outcome is a subset of the input, which satisfies a given divergence from linearity, which is parametrized. An outline of the steps is:

- 1960
 - prepare input for actual coordinate system (e.g. time to space scaling)
 - transform into Hough space
 - identify peak in Hough space
 - extract solution estimate from peak
 - clean input set from noise, using estimate and cutoff limit (input parameter)
- 1965
 - re-process clean sub-set
 - give result as output of the process

The purpose of uTPC for Micromegas is the estimation of the incoming tracks parameters, angle and intercept, using the timing information.

1970 In the current method, uTPC is run only on one layer of measurement. It can be applied on the entire layer or on clusters of strips. Running on an entire layer means that the algorithm needs to adapt for multi-track events and search for multiple peaks in the Hough space, which is probably more CPU-intensive. It's possible, but we will focus on cluster processing, where the clusterization pre-processing is faster.

The method presented here is not the only one used for Micromegas, but rather the one used in the frame of this thesis.

1975 B.1 Prepare input

The raw data for each cluster consists of the strip IDs, and their corresponding PDO, TDO, relBCID etc data.

- the strips should be transformed to real length values. This is done simply by multiplying the strip number with the corresponding pitch of the detector (usual convention is to use mm).
- The TDO and BCID should be transformed into real time in nanoseconds, instead of counts. The BCID corresponds to a coarse timing measurement and the TDO to a finer local one. This can be understood with the scheme in Fig. B.23.

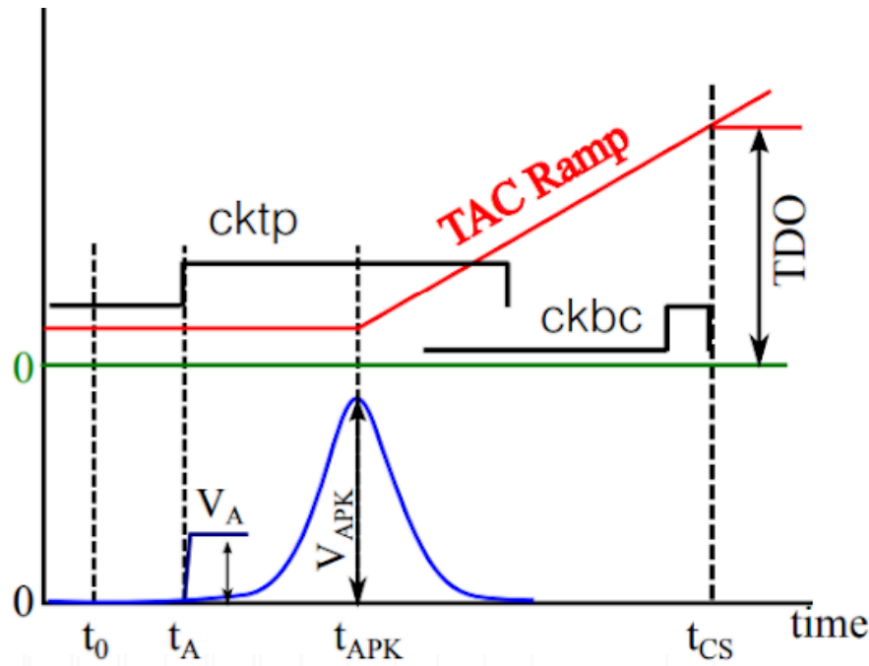


Figure B.23: The peak, either from pulser or from real signal, peaks at some time during a particular BCID, which provides the coarse measurement in units of 25 ns. The TAC starts asynchronously as soon as the peak or threshold is crossed. The TAC charges up a capacitor, which needs a configurable duration of at least 60 ns. The TAC charges up, but needs to arm on the first BC rising edge, and then stops at the next BC clock (ckbc) falling edge. This translates to a TAC duration between 12.5 and 37.5 ns. This TAC duration, referred to as TDO when digitized, provides the time between the peak and the next BC clock, which gives a fine timing measurement in the BC reference.

The BCID is a running clock, with a period of 25 ns. When a trigger is received, the electronics open a "window" of 8 BCs (three in the past, one as the current, and four in the future) wherein the data is kept. These 8 BCs correspond to the relative BCID range.

The TDO is a fast timer, which starts when the signal peak is found, and ends at the next falling edge (after at least one rising edge). This means that in the real time frame the TDO is measuring times between 12.5 ns and 37.5 ns before the next BC. With this logic, the formula to extract the time is:

$$t[\text{ns}] = \text{relbcid} * 25 - \text{tdo}_{\text{duration}} + c$$

where c is a constant used to shift the times. This is important for estimating the right position of the track, but depends on the definition of $t = 0 \text{ ns}$ and the timing of the events in respect to the real time that the track passed.

The output of this process is a series of $[x,y]$ pairs, given as input to the next step.

1990

B.2 Error estimation

This step is more important than usually treated. If the errors are not included, or even not well adjusted, the fitting will not work properly (see next sections). For each $[x,y]$ pair a $[\delta x, \delta y]$ pair is created. The diffusion sigmas and the drift velocity are taken from simulations. See [10]. Indicative values are:

$$\begin{aligned}\sigma_{\text{trans}} &= 370 \text{ } \mu\text{m}/\text{cm}, & \sigma_{\text{long}} &= 250 \text{ } \mu\text{m}/\text{cm} \\ \text{pitch} &= 425 \text{ } \mu\text{m} \text{ (SM)}, & v_{\text{drift}} &= 4.7 \text{ cm}/\mu\text{s} \\ \sigma_{\text{const}} &= 10.5 \text{ ns}\end{aligned}$$

B.2.1 x-Errors

Along the strip-measuring dimension (perpendicular to the strips) the errors included are the uncertainty of a uniform distribution along one strip pitch and the longitudinal diffusion standard deviation (scaled to the corresponding height). This gives the terms:

$$\delta x = \sqrt{(\text{pitch}/\sqrt{12})^2 + (\sigma_{\text{trans}} y)^2}$$

B.2.2 y-Errors

Along the y-direction (time) we have of course the longitudinal diffusion, but also the timing uncertainty from the detector and electronics. These terms are expressed as:

$$\delta y = \sqrt{(v_d \sigma_{\text{const}})^2 + (\sigma_{\text{long}} y)^2}$$

In past bibliography another term appears in this error, which originates from the use of APV electronics [15], where the signal peak finding happened during data analysis. There, the error of finding the inflection point by fitting with a Fermi-Dirac function could be used.

1995

B.3 Hough Transform

This step turns the $[x,y]$ pairs into $[r,\theta]$ pairs and fills a 2D histogram. This transformation is simply defined as

$$r = x \cos\theta + y \sin\theta$$

One can easily prove that the signs can change and still allow a proper Hough transformation. This depends solely on the angle definition.

By this logic, each point (i.e. pair of $[x,y]$) is represented by all lines passing from this point, which appears as a curve in the $[r,\theta]$ space. For example see Fig. B.24 and Fig. B.25. If we find the correct peak (point in $[r,\theta]$) in the Hough space histogram, it corresponds to the line (in $[x,y]$) with the most points, excluding out-liers.

2000

2005 The granularity of the Hough space can make a difference. Effectively, this is the parameters of the 2D histogram, namely the hi-/lo-limits and the number of bins in both dimensions. If very few bins, the histogram peak is easy to identify, but its wide limits don't help in achieving higher accuracy in the estimate. If too many bins, then the curves will not intersect, since the points are not absolutely colinear. Clearly, if at least a sub-set of the points were completely co-linear, then the peak would always be found, regardless of number of bins. The particular parameters chosen here are justified in the next steps, where the peak finding algorithm is described.

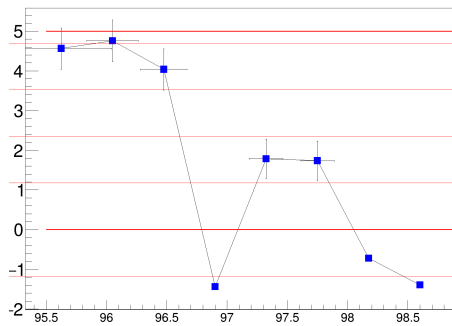


Figure B.24: Points in $[x,y]$ space.

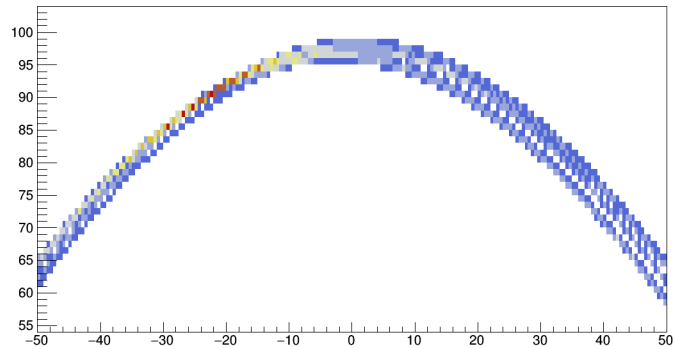


Figure B.25: Same points in $[r,\theta]$ space.

2010 B.4 Peak finding

The purpose of this step is to find the best track estimate given the Hough space of the points. First, the equal peaks are isolated (Fig. B.26). They are projected in θ and the largest cluster is found. Then, for this cluster position, we scan the r -dimension with a finer step (Fig. B.27), in order to identify the best r -peak within the "correct" angle range. Now we have the track estimate, defined as a single $[r,\theta]$ pair.

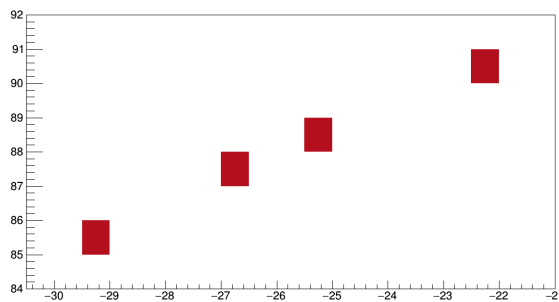


Figure B.26: Isolated peaks in Hough space.

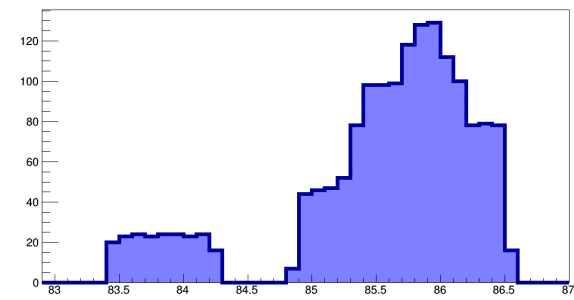


Figure B.27: Projection of the Same points in $[r,\theta]$ space.

2015 In addition to this, the corresponding errors are created, which will be used later to define cut-off range for out-lying points. For θ the error is the size of the bin, while for r it is the standard deviation of its cluster in the fine space.

B.5 Clean input & fit

2020 This step consists of simply scanning the initial set of points and removing the ones that are further from the track estimate, $\pm$ the errors defined. For example, the points of Fig. B.24 are cleaned as shown in Fig. B.28

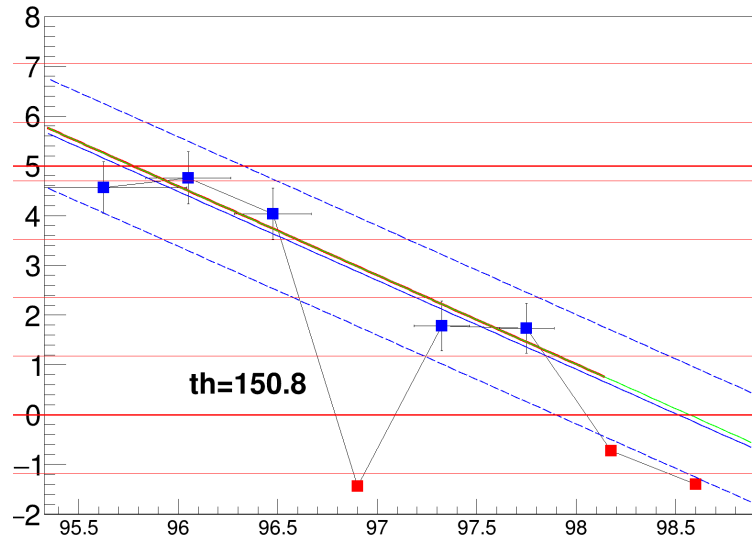


Figure B.28: Points with red are discarded by the cleaning algorithm. The lines drawn are the estimate (blue-continuous), the error limits (blue-dashed). The fit on the clean points gives an angle of 150.8 corresponding to the expected 30 degrees for a back-to-beam chamber.

This last step is to fit the clean data with a line.

B.6 Fit quality

2025 As already mentioned, the errors are important for correct fitting of the clean points. This effect is seen on the probability of the χ^2 value of the fit. This variable shows the probability of the fit result to be correct. An example of the distribution over a run is shown in Fig. B.29. In case of error over-/under-estimation there will be rising tail around the edges of the distribution.

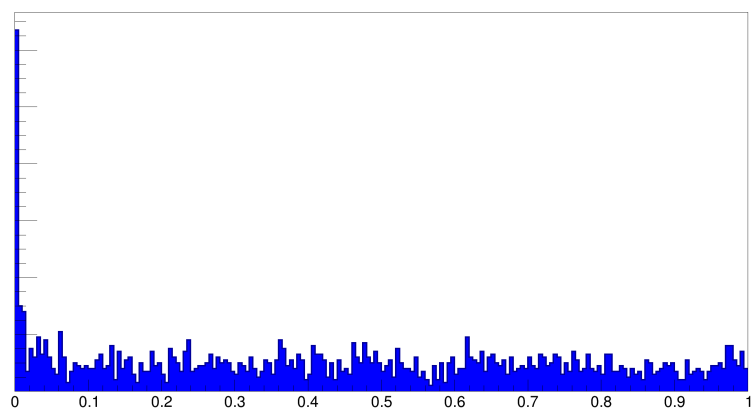


Figure B.29: Chi2 distribution example.

Appendix C - vmm-mon: Monitoring VMM data

2030 A C++ monitoring application was developed to interface with the VMMDAQ/VERSO application. The
code can be found at CERN Gitlab: <https://gitlab.cern.ch/aikoulou/vmm-mon>. It uses ROOT libraries for
the histograms and canvases, and Qt for the user interface. The opening interface is shown in Fig. C.30.
The monitoring performance is limited mainly by the UDP exchange speed and the single histogram fill
operations. For this reason, a grouped messaging approach was adopted. This allows multiple hits to be sent
2035 with one message, and multiple fill operations to be done for the same histogram. This optimization allows
performance to climb over kHz.

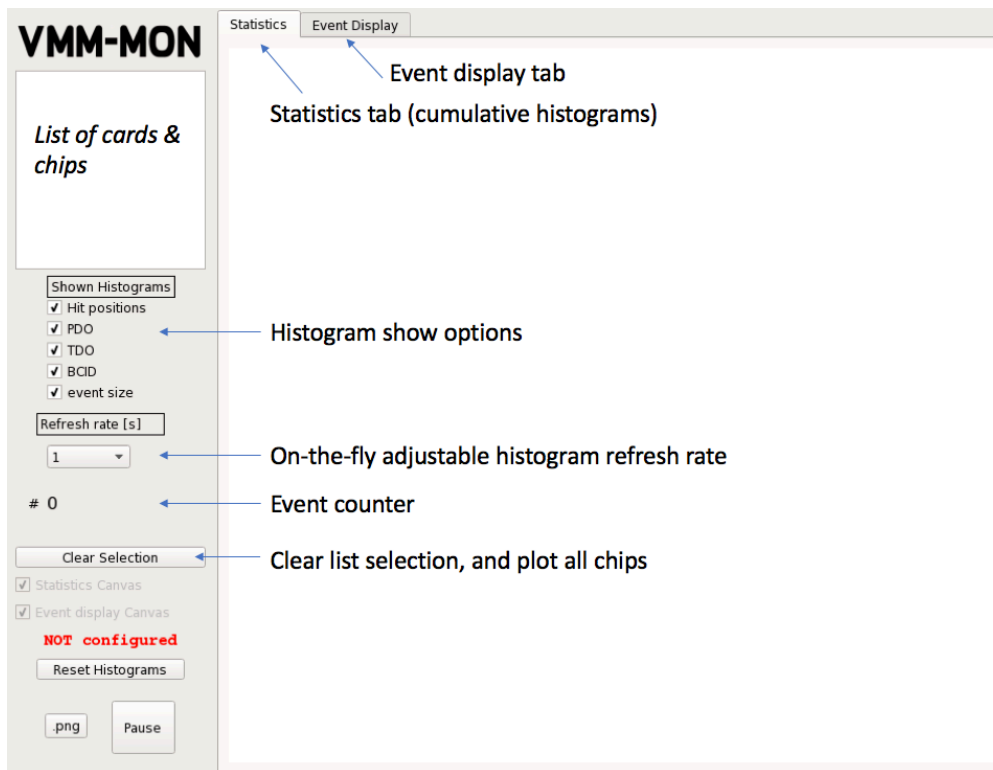


Figure C.30: Opening state of the vmm-mon application.

C.1 Diagram

The application functionality is simple. Assuming VERSO is already running, opening vmm-mon will connect to the UDP port. As soon as configuration is received, the histograms are drawn and setup (hint: if empty histograms not plotted, configuration not done properly). Then, every time that data is received, the appropriate histograms are filled, and the canvases separately refreshed at a given interval. The functionality flow chart is shown in Fig. C.31.

C.2 Communication & configuration

Communication with the VERSO software is done through a local UDP socket, exchanging datagrams of messages.

The configuration required consists of the names and groups of VMM chips. This is passed with some kind of SOF and EOF messages, surrounding messages with groups of VMM and the card/chamber on which they belong. This information is setup specific, and so expected by the DAQ application. For example:

```
"config_start"
"config_MMFE1_VMM1_VMM2"
"config_MMFE2_VMM3_VMM4"
"config_MMFE3_VMM5_VMM6"
"config_end"
```

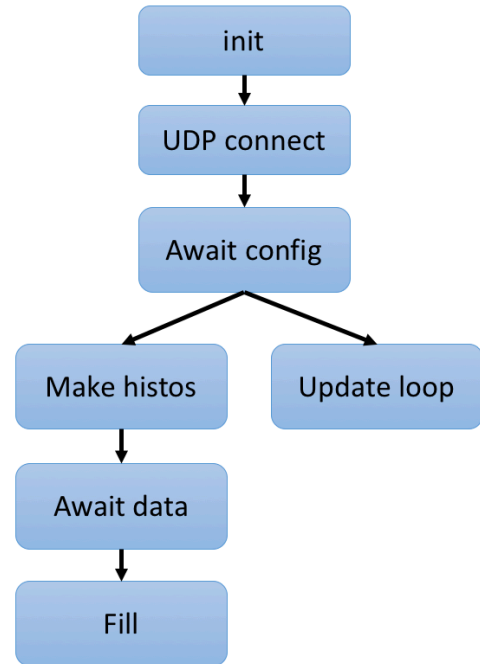


Figure C.31: Flow chart for vmm-mon.

C.3 Data format

After receiving a well-formatted configuration stream, the application will indicate good configuration with a green label "Configured", and is ready to accept data. The data format expected is: "Trigger count, VMM-ID, strip#, PDO, TDO, BCID". For example:

```
"322_VMM1.0_34_450_100_2056"
```

C.3.1 Debugging

Along with the vmm-mon, another application is included, which acts as a dummy data server, that simply sends random data to the monitoring. This can be used as a base for server replication, as debugging aid, and as benchmarking tool for the monitoring capabilities.

C.4 Run

2070 After all the above, there's no other action required by the user. Monitoring is running. A snapshot of the application in running mode is shown in Fig. C.32.



Figure C.32: Configured and running state of the vmm-mon application.

Appendix D - NSW B-field environment

2075

For several cases, the B-field values in the cavern are necessary. Of course there are many sensors measuring it, but not everywhere. When looking to place power supplies in new locations, we need to know the expected B-field values in certain positions, and since there is not already an accessible application with the data, a simple one was made, to simply plot the data using root, permitting many other essential checks. The data was provided by Alexey Vorozhotsov. An example snapshot is shown in Fig. D.33. The code, along with the data, can be found at <https://gitlab.cern.ch/aikoulou/bfield>.

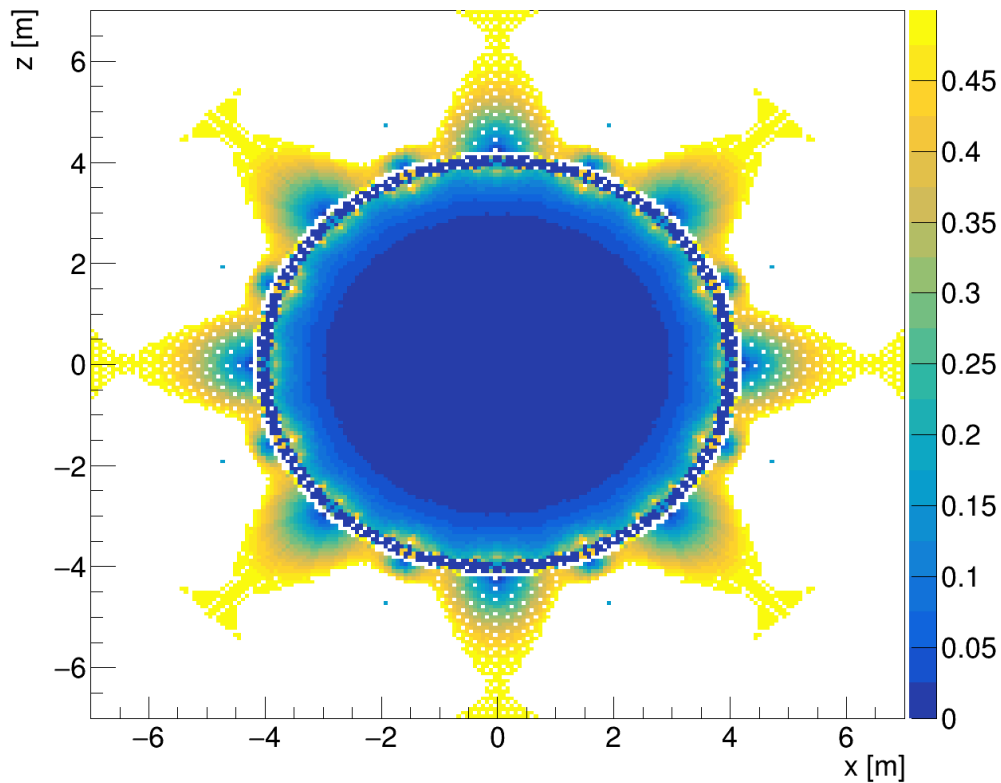


Figure D.33: An example view of the bfield application, showing the outline of the 0.5T limit.

Appendix E - Services documentation

E.1 TwinAx installation order & mapping

As part of demystifying the TwinAx routing, a one-page manual was made as guide to the installation team (Fig. E.34). The top shows the board layout of the xM2 and xM1 MM modules. Below, the routing of each cable is shown, for a single wedge side, i.e. one quarter of the TwinAx. The columns are showing

- the cable ID, simple running number.
- a flag for the ones that have to cross the central bar of the spacer frame. These are routed first, since they are the ones with the most critical path and length restriction.
- the label, which consists of five characters. First is [A/L] for ADDC or L1DDC connection. Then L* shows which MMFE8 layer the cable serves. Then P* shows which PCB the cable serves. Exception are the few LTA (L1DDC-to-ADDC) cables.
- the routing, per half PCB, which is the highest useful granularity for this routing. The colors and numbers correspond to the defined routing areas as shown in Fig. E.35.
- the number of half PCBs that the cable traverses.
- the assigned length [m].
- the effective, i.e. used, length [m]. as calculated from the number of PCBs traversed.
- a length grouping and optimisation dubbed "July2018".
- the length of the cable to be looped.
- a flag for the cables corresponding to lower radius MMFE8, thus needing machining of the connector, as mentioned in the Services chapter.
- installation order, optimised to have first the cables with least loops, and the ones that cross the bar.
- the order in which they are installed in the central bar, which corresponds to location identification as shown in Fig. E.36.

Figure E.34: The TwinAx installation guide.

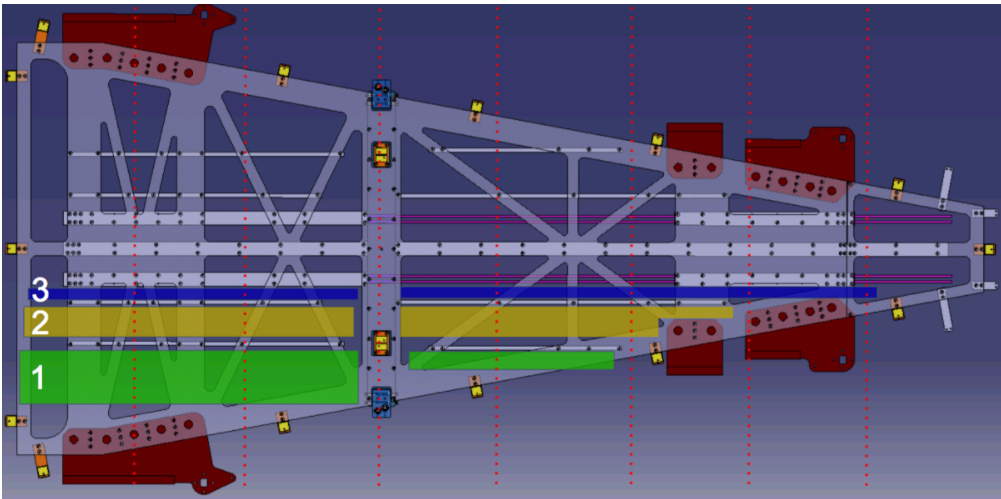


Figure E.35: The TwinAx installation guide.

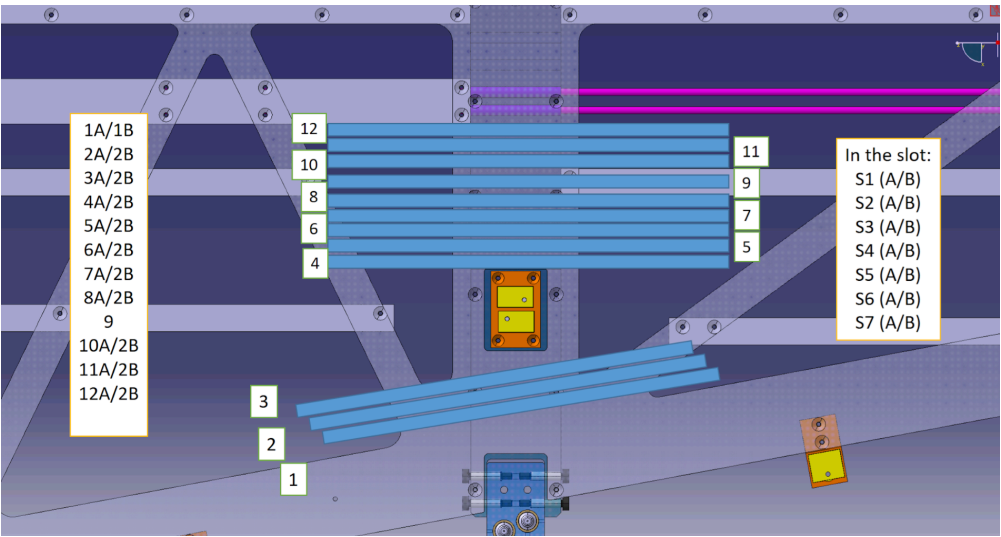


Figure E.36: The TwinAx installation guide.

E.2 NJD routing

Similar to the TwinAx table, tables were made to help guide installation of services on the NJD in building 191. Fig. E.37 shows the cable tray naming used in the following tables.

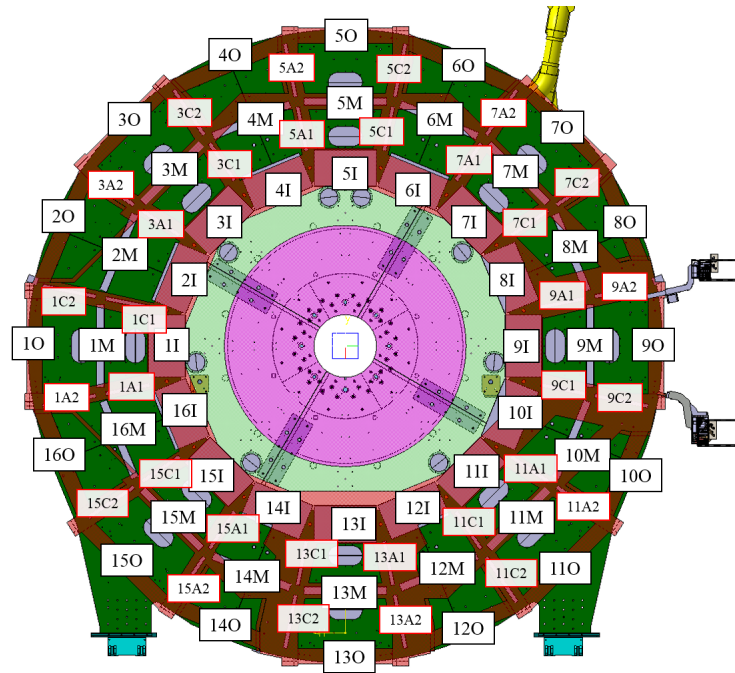


Figure E.37: Cable tray naming on NJD HO side. The numbers correspond to sectors. The letters mean inner, middle or outer part, when angular, and clock-/anti-clock-wise when tray is radial.

E.2.1 Cabling global table

For the NJD HO routing (cabling), a single table was prepared (Fig. E.38). For each cable bundle (even single cables) a row is added, showing the size of the bundle in outer diameter (OD) and number. The top row displays the NJD cable tray names in circular order, as installed. The final columns to the right show the calculated length for each bundle, split in components: NJD part, on-detector, on-Rim, and bracket-part.

type	OD [mm]	bundle size [#]	#sector															Brac2Rim	JD comp	extra for trays	overJD	from t	SUM Single	Sum Bundle [m]
Alignment	5	2	10,9	-														1.7	0	0	0.1	1	2.80	5.60
		2	12,11	9C2	9C1	10I	11I	11C1	11C2	-								1.7	6	0.3	0.1	0.6	8.70	17.40
		2	14,13	9C2	9C1	10I	11I	12I	13I	13C1	13C2	-						1.7	8	0.4	0.1	0.5	10.70	21.40
		2	16,15	9C2	9C1	10I	11I	12I	13I	14I	15I	15C1	15C2	-				1.7	10	0.5	0.1	2	14.30	28.60
		2	8,7	9C2	9C1	9I	8I	7C1	7C2	-								1.7	6	0.3	0.1	0.5	8.60	17.20
		1	6	9C2	9C1	9I	8I	7I	6I	5C1	5C2	-						1.7	8	0.4	0.1	1.7	11.90	11.90
		3	3,4,5	9C2	9C1	9I	8I	7I	6I	5I	4I	3C1	3C2	-				1.7	10	0.5	0.1	0.7	13.00	39.00
		2	2,1	9C2	9C1	9I	8I	7I	6I	5I	4I	3I	2I	1C1	1C2	-		1.7	12	0.6	0.1	2.5	16.90	33.80
		3	1	9C2	9C1	9I	8I	7I	6I	5I	4I	3I	2I	1C1	1M	-		1.7	12.3	0.615	1.8		16.42	49.25
		3	2	9C2	9C1	9I	8I	7I	6I	5I	4I	3C1	3M	-				1.7	10.3	0.515	4		16.52	49.55
Bars	3	3	9C2	9C1	9I	8I	7I	6I	5I	4I	3C1	3M	-				1.7	10.3	0.515	1.8		14.32	42.95	
	3	4	9C2	9C1	9I	8I	7I	6I	5C1	5M	-						1.7	8.3	0.415	4		14.42	43.25	
	3	5	9C2	9C1	9I	8I	7I	6I	5C1	5M	-						1.7	8.3	0.415	1.8		12.22	36.65	
	3	6	9C2	9C1	9I	8I	7C1	7M	-								1.7	6.3	0.315	4		12.32	36.95	
	3	7	9C2	9C1	9I	8I	7C1	7M	-								1.7	6.3	0.315	1.8		10.12	30.35	
	3	8	9C2	9M	-												1.7	2.3	0.115	4		8.12	24.35	
	3	9	9C2	9M	-												1.7	2.3	0.115	1.8		5.92	17.75	
	3	10	9C2	9M	-												1.7	2.3	0.115	4		8.12	24.35	
	3	11	9C2	9C1	10I	11A	11M	-									1.7	5.3	0.265	1.8		9.07	27.20	
	3	12	9C2	9C1	10I	11A	11M	-									1.7	5.3	0.265	4		11.27	33.80	
	3	13	9C2	9C1	10I	11I	12I	13A	13M	-							1.7	7.3	0.365	1.8		11.17	33.50	
	3	14	9C2	9C1	10I	11I	12I	13A	13M	-							1.7	7.3	0.365	4		13.37	40.10	
	3	15	9C2	9C1	10I	11I	12I	13I	14I	15A1	15M	-					1.7	9.3	0.465	1.8		13.27	39.80	
	3	16	9C2	9C1	10I	11I	12I	13I	14I	15A1	15M	-					1.7	9.3	0.465	4		15.47	46.40	

This long table is then supplemented by a summary table, shown in Fig. E.39. The summary table shows each cable tray, with the cables that are expected to be routed in it, split in categories, and then summed up in cross-section, comparing the sum with the cable tray definition. Thus, the most densely populated trays can be instantly identified. This proved very useful during the design phase as well, since system restrictions were often changing, which led to necessary changes in routing. This table was automated with table equations and merely needed the routing path as input to calculate the required lengths to order, even per bundle, and then to provide the summary for cross-checks during installation.

kg/m:	0.0162	0.2	0.2	0.072	0.072	0.06	0.1												
OD:	3.3	10.7	10.7	5	5	5	15.6												
[T-HO]-name	sTGC HV	MM LV	sTGC LV	RO Fibers	Trig Fibers	Alignment	DCS	TOTAL#	TOTAL [mm cs/50	L [m]	[kg/m]	W [kg]	#fix.	W/fix.point [kg]					
1I	0	16	0	0	0	0	0	16	3663.68	73	1	3.20	3.2	2	1.6				
2I	32	8	0	0	0	0	5	65	3214.4	64	1	2.74	2.7424	2	1.3712				
3I	64	8	0	0	0	0	5	117	4346.96	87	1	3.58	3.5848	2	1.7924				
4I	96	0	0	0	0	14	0	170	4097.68	82	1	3.37	3.3672	2	1.6836				
5I	128	0	0	0	0	14	0	222	5230.24	105	1	4.21	4.2096	2	2.1048				
6I	160	8	0	0	0	21	0	289	8544.64	171	1	7.07	7.072	2	3.536				
7I	192	8	0	0	0	21	0	341	9677.2	194	1	7.91	7.9144	2	3.9572				
8I	224	16	0	0	0	29	0	409	13041.6	261	1	10.84	10.8368	2	5.4184				
9I	0	16	0	0	0	29	0	45	5113.68	102	1	4.94	4.94	2	2.47				
10I	224	24	0	0	0	24	0	412	14623.44	292	1	12.14	12.1368	2	6.0684				
11I	192	24	0	0	0	18	0	354	13190.88	264	1	10.93	10.9344	2	5.4672				
12I	160	32	0	0	0	16	0	308	13790.16	276	1	11.57	11.572	2	5.786				
13I	128	0	0	0	0	10	0	218	5030.24	101	1	3.97	3.9696	2	1.9848				
14I	96	24	0	0	0	8	0	188	9293.2	186	1	7.81	7.8072	2	3.9036				
15I	64	24	0	0	0	2	0	130	7860.64	157	1	6.60	6.6048	2	3.3024				
16I	32	16	0	0	0	0	0	68	4796.24	96	1	4.04	4.0424	2	2.0212				
1M	0	0	0	0	0	3	0	3	150	3	1.3	0.18	0.234	2	0.117				
2M	0	0	0	10	1	0	0	11	550	11	1.3	0.79	1.0296	2	0.5148				
3M	0	0	0	10	2	6	0	18	900	18	1.3	1.22	1.5912	2	0.7956				
4M	0	0	0	21	3	0	0	24	1200	24	1.3	1.73	2.2464	2	1.1232				
5M	0	0	0	21	4	6	0	31	1550	31	1.3	2.16	2.808	2	1.404				
6M	0	0	0	30	5	0	0	35	1750	35	1.3	2.52	3.276	2	1.638				
7M	0	0	0	30	6	6	0	42	2100	42	1.3	2.95	3.8376	2	1.9188				
8M	0	0	0	40	7	0	0	47	2350	47	1.3	3.38	4.3992	2	2.1996				
9M	0	0	0	0	0	9	0	9	450	9	1.3	0.54	0.702	2	0.351				
10M	0	0	0	30	7	0	1	38	2336.72	47	1.3	2.76	3.5932	2	1.7966				
11M	0	0	0	30	6	6	1	43	2586.72	52	1.3	3.05	3.9676	2	1.9838				
12M	0	0	0	20	5	0	1	26	1736.72	35	1.3	1.90	2.47	2	1.235				
13M	0	0	0	20	4	6	0	30	1500	30	1.3	2.09	2.7144	2	1.3572				
14M	0	0	0	10	3	0	0	13	650	13	1.3	0.94	1.2168	2	0.6084				
15M	0	0	0	10	2	6	0	18	900	18	1.3	1.22	1.5912	2	0.7956				
16M	0	0	0	0	1	0	0	1	50	1	1.3	0.07	0.0936	2	0.0468				

Figure E.39: Part of the cabling table routing map summary. The columns to the right show the total cross-section, the effective cable tray width assuming 50mm of tray height, the tray length, the weight per meter, the number of fixation points for a cable tray and the weight per fixation point. This table is normally longer and includes a row for each tray shown in E.37.

E.2.2 Piping installation

Similar to the cabling map of NJD HO side, routing maps were made for each type of pipe routing on the NJD IP side. Namely, cooling, sTGC Gas, MM Gas, primary and secondary pipes included, separate files were made, showing the naming scheme, the manifold locations and corresponding cable trays, and finally the **routing for each pipe**. Only one example is shown, in Fig. E.40, where the sTGC secondary pipes extreme routing is shown.

										Tray equiv lengths																			
										900 67 90 37 90 67 90 37 90 67 90 37 90 67 90																			
										assuming the radial passages are on the flank										TOP routing									
these should correspond to 'naming scheme' sheet																													
gas manifold name	tray of start	pipe name	sector	layer	t/b	dir	A	M	C	-	A	M	C	-	A	M	C	-	A	M	C	-	A	M	C	-	A	M	C
STGC-GM-IN-TOP-1	T-IP-5C	STGC-IN-S2-L1	2	1	TOP	IN																							
		STGC-IN-S3-L1	3	1	TOP	IN																							
		STGC-IN-S4-L1	4	1	TOP	IN																							
		STGC-IN-S5-L1	5	1	TOP	IN																							
		STGC-IN-S6-L1	6	1	TOP	IN																							
		STGC-IN-S7-L1	7	1	TOP	IN																							
		STGC-IN-S8-L1	8	1	TOP	IN																							
		STGC-IN-S9-L1	9	1	TOP	IN																							
		STGC-IN-S2-L2	2	2	TOP	IN																							
STGC-GM-IN-TOP-2	T-IP-5C	STGC-IN-S3-L2	3	2	TOP	IN																							
		STGC-IN-S4-L2	4	2	TOP	IN																							
		STGC-IN-S5-L2	5	2	TOP	IN																							
		STGC-IN-S6-L2	6	2	TOP	IN																							
		STGC-IN-S7-L2	7	2	TOP	IN																							
		STGC-IN-S8-L2	8	2	TOP	IN																							
		STGC-IN-S9-L2	9	2	TOP	IN																							
		STGC-IN-S2-L3	2	3	TOP	IN																							
		STGC-IN-S3-L3	3	3	TOP	IN																							
STGC-GM-IN-TOP-3	T-IP-5C	STGC-IN-S4-L3	4	3	TOP	IN																							
		STGC-IN-S5-L3	5	3	TOP	IN																							
		STGC-IN-S6-L3	6	3	TOP	IN																							
		STGC-IN-S7-L3	7	3	TOP	IN																							
		STGC-IN-S8-L3	8	3	TOP	IN																							
		STGC-IN-S9-L3	9	3	TOP	IN																							
		STGC-IN-S2-L4	2	4	TOP	IN																							
		STGC-IN-S3-L4	3	4	TOP	IN																							
		STGC-IN-S4-L4	4	4	TOP	IN																							
STGC-GM-IN-TOP-4	T-IP-5C	STGC-IN-S5-L4	5	4	TOP	IN																							
		STGC-IN-S6-L4	6	4	TOP	IN																							
		STGC-IN-S7-L4	7	4	TOP	IN																							
		STGC-IN-S8-L4	8	4	TOP	IN																							
		STGC-IN-S9-L4	9	4	TOP	IN																							

Figure E.40: Part of the sTGC secondary pipe routing guide. Here, four gas supply manifolds are shown, each with its eight corresponding pipes.

E.3 Weight and CoM study

The Project office engineers carried out a study, early on, to determine the expected center of mass (CoM or CoG) of the NSW. From the services side, a table was made at the time, when the final design of components was still many months in the future. The estimated numbers used in that study are:

- Rim boxes: 560 kg
- Pipes: 480 kg
- Cables: 850 kg

With a total estimate, after margins, of 2.2 t.

E.4 Useful links

Some useful links are gathered here, for future reference, and to give a chance to the reader to look back at every stage of the design and appreciate the complexity.

2135 The services installation meetings can be found under the NSW Services category:

<https://indico.cern.ch/category/7850/>

A Twiki page was started to gather documentation, which later would be kept as reference. It hasn't been updated in a while, but useful information might be found:

<https://twiki.cern.ch/twiki/bin/viewauth/Atlas/NSWServices>.

2140 In the same Twiki page, at the bottom, you can find links for the Services sessions at multiple ATLAS Muon weeks.

E.4.1 Reviews

2145 Similar to the rest of the sub-systems, the NSW services had to undergo thorough review by internal and external associates. The first one was in July of 2016, whose type was considered to be between the usual PDR and FDR. The second one was a year later, July 2017, and was closer to a PRR, which still doesn't properly match the spirit, since it concerned basically the assembly and production of a single object.

- Services PDR 2016.

Indico link: <https://indico.cern.ch/event/507106/>

EDMS documents: <https://edms.cern.ch/project/ATL-0000010521>

- 2150
- Services FDR 2017.

Indico link: <https://indico.cern.ch/event/638387/>

EDMS documents: <https://edms.cern.ch/project/ATL-0000010772>

Appendix F - Acronyms

ADC	Analog to Digital Converter
ADDC	ART Data Driver Card
ART	Address in Real Time
ATLAS	A Toroidal LHC ApparatuS
ASIC	Application-Specific Integrated Circuit
BCAM	Brandeis Charge-Coupled Device Angular Monitor
BW	Big Wheel
CERN	Conseil Europeen pour la Recherche Nucleaire, or European Organization for Nuclear Research
CSC	Cathode Strip Chamber
DAC	Digital to Analog Converter
DAQ	Data Acquisition
DCS	Detector Control System
EDMS	Engineering & Equipment Data Management Service
FSM	Finite State Machine
JCOP	Joint Control Project
JTAG	Joint Test Action Group
LIDDC	Level-1 Data Driver Card
LVDB	Low Voltage Distribution Board
MDT	Monitored Drift Tube
Micromegas	Micro-mesh Gaseous Structure
MMFE	Micromegas Front-end card
NSW	New Small Wheel
OPC	Open Platform Communications
PDO	Peak Detector Output
SCA	Slow Control Adapter
sTGC	small-strip Thin Gap Chamber
TAC	Time to Amplitude Converter
TDO	Time Detector Output
TTC	Timing, Trigger and Control
μTPC	micro Time Projection Chamber
VMM	Venetis MicroMegas

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