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Control, commissioning, operation and performance of the Phase-I upgrade of the LAr calorimeter electronics of the ATLAS detector

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Affidavit

I, undersigned, Florent BERNON, hereby declare that the work presented in this manuscript is my own work, carried out under the scientific direction of Emmanuel MONNIER and Luis HERVAS, in accordance with the principles of honesty, integrity and responsibility inherent to the research mission. The research work and the writing of this manuscript have been carried out in compliance with both the french national charter for Research Integrity and the Aix-Marseille University charter on the fight against plagiarism.

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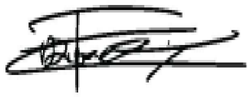

Liste de publications et participation aux conférences

Liste des publications réalisées dans le cadre du projet de thèse:

1. G. Aad et al., “The Phase-I trigger readout electronics upgrade of the ATLAS Liquid Argon calorimeters”, JINST, vol. 17, no. 05, P05024, 2022. DOI: 10.1088/1748-0221/17/05/P05024. arXiv: 2202.07384 [physics.ins-det] (cit. on p. 3) [1]

2. G. Aad et al., “The ATLAS Experiment at the CERN Large Hadron Collider: A Description of the Detector Configuration for Run 3”, May 2023. arXiv: 2305.16623 [physics.ins-det] (cit. on p. 4). [2]

3. G. Aad et al., “The ATLAS Trigger System for LHC Run 3 and Trigger performance in 2022”, Jan. 2024. arXiv: 2401.06630 [hep-ex] (cit. on p. 4). [3]

Participation aux conférences et écoles d’été au cours de la période de thèse:

1. TWEPP 2021: Poster, ATLAS LAr Calorimeter Commissioning for LHC Run-3, https://indi.to/bCcDk

2. XV ICFA School on Instrumentation in Elementary Particle Physics, https://www.tifr.res.in/ icfa2023/index.html

3. TWEPP 2023: Talk, ATLAS LAr Calorimeter Commissioning for LHC Run-3, https://indi.to/wNVNz

Résumé

La recherche en physique des hautes énergies vise à révéler les constituants fondamentaux de la matière et à élucider les principes régissant leurs interactions. Cette quête repose sur des accélérateurs de particules sophistiqués. Le plus puissant est actuellement le grand Collisionneur de Hadrons (LHC) situé au CERN (l'organisation européenne pour la recherche nucléaire). Le LHC accueille quatre expériences, dont ATLAS, un détecteur de particules polyvalent concu pour sonder les phénomènes rares au sein des données de collision et en particullier rechercher le boson de Higgs. Après 15 ans de fonctionnement et une moisson de résultats scientifiques dont la decouverte du boson de Higgs dans les collisions proton-proton, le LHC se prépare à deux phases de mise à niveau pour augmenter sa luminosité et son taux de collision. Des mises à niveau correspondantes du détecteur ATLAS sont impératives pour maintenir une acquisition des données et des performances optimales en physique.

La première phase de mise à niveau, nommé Phase-I, installée avant le démarrage du "Run 3" en 2022, intègre entre autres un nouveau chemin de données dans le système de déclenchement du calorimètre à argon liquide. Ce système numérique, détaillé dans cette thèse, remplace l'ancien système basé sur une électronique analogique. Contrôlé et configuré par des systèmes basés sur des serveurs OPC-UA (Open Platform Communications Unified Architecture), l'installation de ce système amélioré a été finalisée en mars 2022. En regardant vers l'avenir, la deuxième phase de mise à niveau, lors de l'arrêt prolongé du LHC débutant en 2026, révisera l'ensemble de la chaîne électronique du calorimètre, permettant de nouvelles capacités de calcul et de traitement du signal.

Cette thèse détaille le contrôle, l'exploitation, les essais et l'évaluation des performances de cette nouvelle électronique mise à niveau lors de cette Phase-I pour les calorimètres à argon liquide du détecteur ATLAS. L'arrivée du faisceau pour le début du "Run 3" implique une fin d'intégration de manière transparente dans les opérations d'ATLAS. Un point crucial sera l'appréciation et la certification des performances du nouveau système de déclenchement par rapport au déclencheur analogique du calorimètre. Cette thèse décrit le travail effectué pour l'amélioration des performances ainsi que la stabilité des cartes électroniques installées sur le détecteur lors de cette Phase-I.

Mots-clés : LHC, ATLAS, Calorimètre à Argon liquide, Déclenchement et acquisition de données, Système de contrôle, mise à niveau Phase-I.

Abstract

Research in high-energy physics aims to reveal the fundamental constituents of matter and elucidate the principles governing their interactions. This quest relies on sophisticated particle accelerators. The most powerful and currently the largest is the Large Hadron Collider (LHC) located at CERN (the European Organization for Nuclear Research). The LHC hosts four experiments, including ATLAS, a versatile particle detector designed to probe rare phenomena within collision data such as the search for the Higgs boson. After 15 years of running and a harvest of scientific results including the discovery of the Higgs boson in proton-proton collisions, the LHC is preparing two upgrade phases to increase its luminosity and collision rate. Corresponding upgrades of the ATLAS detector are imperative to maintain optimal data acquisition and performance in physics.

The first upgrade phase, known as Phase-I, installed before the start of "Run 3" in 2022, incorporates among other things a new data path in the liquid argon calorimeter trigger system. This digital system, detailed in this thesis, replaces the old analog electronic trigger. Controlled and configured by systems based on OPC-UA (Open Platform Communications Unified Architecture) servers, the installation of this upgraded system was completed in March 2022. Looking forward, the second upgrade phase, during the extended shutdown of the LHC starting in 2026, will revise the entire electronic chain of the calorimeter, promising new computing and signal processing capabilities.

This thesis details the control, operation, testing, and performance evaluation of this new upgraded electronics during this Phase-I for the liquid argon calorimeters of the ATLAS detector. The arrival of the beam for the start of "Run 3" implies a seamless integration into ATLAS operations. A crucial point will be the assessment and certification of the performance of the new triggering system compared to the analog trigger of the calorimeter. This thesis describes the work done to improve the performance as well as the stability of the electronic boards installed on the detector during this Phase-I.

Keywords: LHC, ATLAS, Liquid Argon Calorimeter, Trigger and data acquisition, control system, Phase-I upgrade.

Synthèse en français

0.1 Introduction

La recherche en physique moderne vise à élucider et unifier les forces fondamentales gouvernant l'univers. Malgré le succès remarquable du Modèle Standard de la physique des particules, qui décrit les forces fortes, faibles et électromagnétiques à travers les fermions, les bosons de jauge et le boson de Higgs, il reste incomplet. Nous pouvons notamment parler de la gravité qui reste en dehors de son champ d'application, aux côtés d'autres phénomènes inexpliqués tels que l'existence de trois générations de quarks et de leptons, les masses des neutrinos, la matière noire et l'énergie sombre. Ces lacunes soulignent le besoin d'une théorie plus complète.

Dans cette quête d'une compréhension plus approfondie, des institutions comme le CERN (Conseille Européenne pour la Recherche Nucléaire) jouent un rôle important. Le CERN abrite le Grand Collisionneur de Hadrons (LHC), l'accélérateur de particules le plus puissant au monde avec une énergie de collision au centre de masse allant jusqu'à 14 TeV, où des expériences de pointe sont menées pour explorer les frontières de la physique des particules.

Ces expériences sont basées sur quatre points du LHC. Sur chacun de ces points, un détecteur est installé, ATLAS, CMS, LHCb et ALICE, contribuant chacun de manière distincte à une mission scientifique. ATLAS et CMS sont les deux expériences généralistes, impliquées dans la découverte du boson de Higgs en juillet 2012. Elles ont également été conçues pour rechercher des preuves de théories de la physique des particules au-delà du Modèle Standard (SM). LHCb est une expérience de physique conçue principalement pour mesurer les paramètres de la violation de CP dans les interactions d'hadron-b. Et enfin, ALICE est conçue pour étudier le plasma de quarks et de gluons, dans les collisions d'ions lourds.

Le détecteur ATLAS a été minutieusement conçu pour mener une grande variété de mesures, allant des évaluations fondamentales du SM aux examens de précision du boson de Higgs et de nouvelles particules. Situé 100m sous terre, ATLAS fonctionne à des luminosités de 2 à 3 $\times 10^{34} cm^{-2} s^{-1}$, avec un taux de collision de 40 MHz à 13,6 TeV. Pour optimiser la détection des particules et minimiser les pertes d'énergie, ATLAS utilise un système de déclenchement sophistiqué en trois niveaux, crucial pour l'acquisition et l'analyse des données.

Afin de rechercher davantage de preuves de nouvelles physiques et de poursuivre les études sur le boson de Higgs, il a été décidé de mettre à jour le LHC avec les dernières technologies, c'est la mise à niveau HL-LHC. Avec cette modernisation, le LHC vise une luminosité beaucoup plus élevée et une légère augmentation de l'énergie à 14 TeV. Pour faire face à cette nouvelle luminosité, deux phases de mise à jour du détecteur ATLAS sont prévues : la première phase a été installée entre 2019 et début 2022, et la seconde phase est prévue pour le début de 2026 jusqu'à fin 2028. Ces développements permettront au HL-LHC d'avoir une luminosité intégrée pouvant aller à 4000 fb^{-1}, multipliant ainsi par dix la quantité de données qu'ATLAS pourra enregistrer. Ces nouvelles données permettront d'étudier des événements plus rares et de fournir une plus grande précision jamais obtenue auparavant.

En regardant vers l'avenir, la prise de données en cours dite "Run 3", et les installations HL-LHC subséquentes promettent de repousser les limites de l'exploration scientifique, avec des luminosités prévues allant jusqu'à 7 $\times 10^{34} cm^{-2} s^{-1}$. Ces développements représentent d'importantes opportunités pour explorer les mystères de l'univers et faire avancer notre compréhension de la physique fondamentale.

0.2 Le sous détecteur à argon liquide d'ATLAS

Le détecteur ATLAS, illustré dans la Figure 0.1, est le plus grand détecteur de particules jamais construit. Il mesure 44 mètres de long, 25 mètres de hauteur, 25 mètres de largeur et pèse 7000 tonnes. Il est situé dans une caverne souterraine, à 100 mètres de profondeur, près du site principal du CERN et de la ville de Genève, en Suisse. Avec CMS, il constitue l'un des deux détecteurs polyvalents du LHC. Il permet d'étudier un large éventail de domaines de la physique, de la recherche du boson de Higgs à l'existence de dimensions supplémentaires dans l'espace-temps, ainsi que des particules pouvant constituer la matière noire. Plus de 6000 membres provenant de 182 instituts, représentant 42 pays, travaillent sur l'expérience ATLAS.

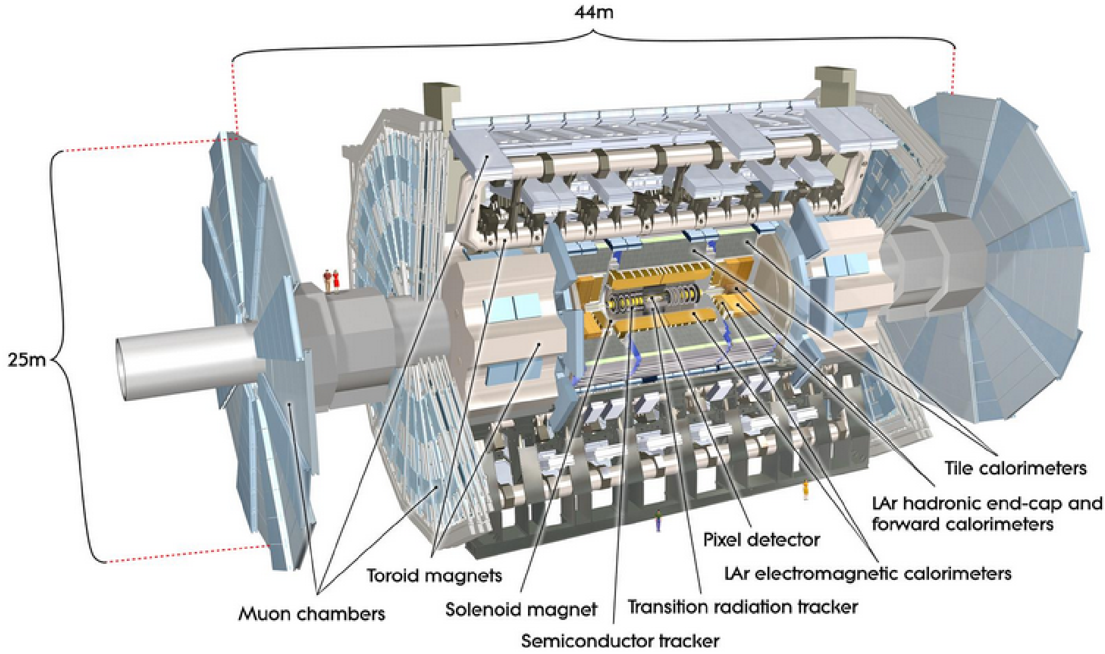

FIGURE 0.1 : Le détecteur ATLAS et ses sous détecteurs[4]

Les faisceaux de particules du LHC entrent en collision au centre de ce détecteur, avec une énergie de 13.6 TeV et une fréquence de collision de 40 MHz. Ces faisceaux produisent une multitude de nouvelles particules qui émergent du point de collision dans toutes les directions. Six sous-systèmes de détection différents disposés en couches autour du point de collision enregistrent un événement composé de la trajectoire, de la quantité de mouvement et de l'énergie des particules nouvellement émises. Ces informations permettent l'identification des particules et la reconstruction de l'événement. Une énorme quantité de données est générée dans le processus, environ 2.5Mo par événement brut, multipliée par 40 millions de collisions par seconde (40 MHz). Cela produit un total de 100 Téraoctets de données brutes par seconde. Il n'est pas possible de stocker et d'analyser toutes ces données produites. Par conséquent, ATLAS dispose d'un système de déclenchement qui détermine la pertinence des événements, les enregistrant ou les ignorant, pour passer d'un taux de 40 MHz à 100 kHz après le premier niveau de déclenchement. Ensuite, le déclencheur de haut niveau réduira le taux d'événements de 100 kHz à 4 kHz. Les données restantes, sont stockées pour des analyses ultérieures. Des systèmes de calcul sont ensuite utilisés pour analyser ces événements, sur de nombreux serveurs répartis dans le monde entier.

Le système de calorimètres à argon liquide (LAr), [5] illustré en Figure 0.2, remplit la fonction de mesurer l'énergie des électrons, des photons et des hadrons. Caractérisé par des couches de métal - tungstène, cuivre ou plomb - qui capte l'énergie des particules entrantes, les transformant ensuite en une gerbe de nouvelles particules de plus basse énergie, ce système repose sur l'ionisation de l'argon liquide intercalé entre les couches induites par cette gerbe de particules. Le courant d'ionisation résultant est ensuite mesuré, permettant de déterminer l'énergie de la particule initiale ayant impacté le détecteur. La région centrale du calorimètre appelée "tonneau" et la partie éloigné le "bouchon" sont conçue pour l'identification des électrons et des photons. Elle présente une structure d'accordéon distinctive pour garantir une capture complète des particules.

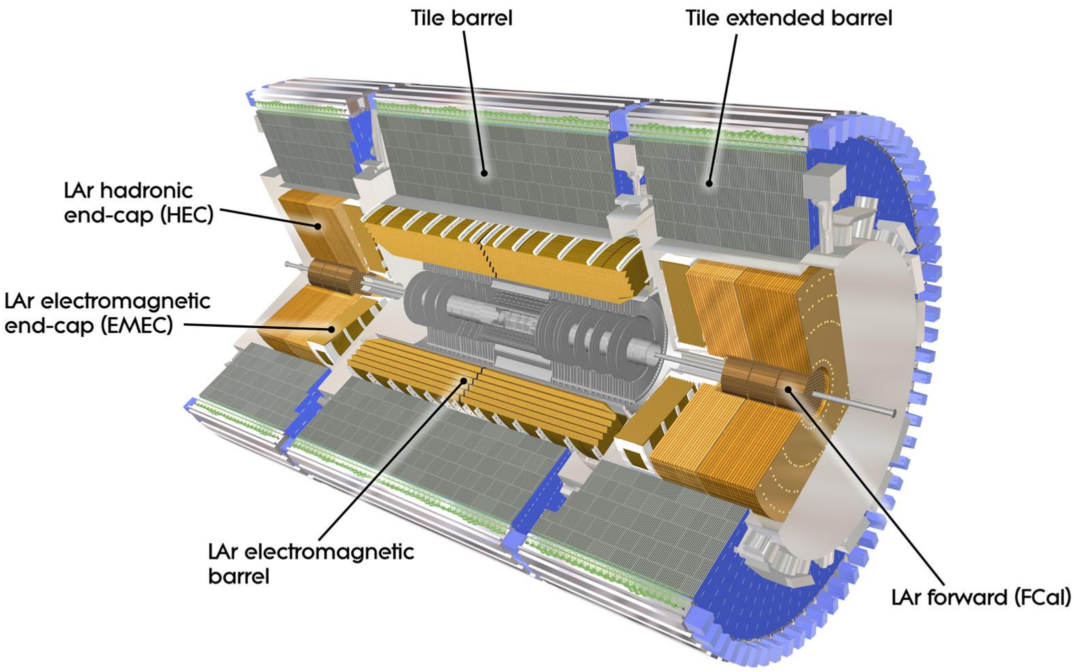

FIGURE 0.2 : Calorimètre à Argon liquide d'ATLAS. [5]

0.3 Mise à niveau de l'électronique Phase-I du système de déclenchement du détecteur à Argon liquide

La mise à niveau de la Phase-I de l'électronique de déclenchement du calorimètre à argon liquide (LAr) d'ATLAS représente une avancée significative dans les capacités de détecter et mesurer les particules produites lors de collision à haute énergie. Cette mise à niveau vise à améliorer les performances du système de calorimétrie LAr pour répondre à l'augmentation de la luminosité du LHC et aux besoins évolutifs de la recherche en physique des particules.

Les principaux objectifs de la mise à niveau de la Phase-I comprennent l'amélioration de la résolution du détecteur, le maintien de son efficacité dans l'identification des particules et l'amélioration de sa capacité à supporter les taux de collisions plus élevés attendus lors des phases futures du LHC.

La mise à niveau Phase-I est centrée sur la modernisation du système électronique de déclenchement des calorimètres LAr. Cela implique la mise en œuvre d'électroniques et de systèmes de lecture de pointe pour améliorer la collecte, le traitement et la transmission des données ainsi que les capacités de déclenchement.

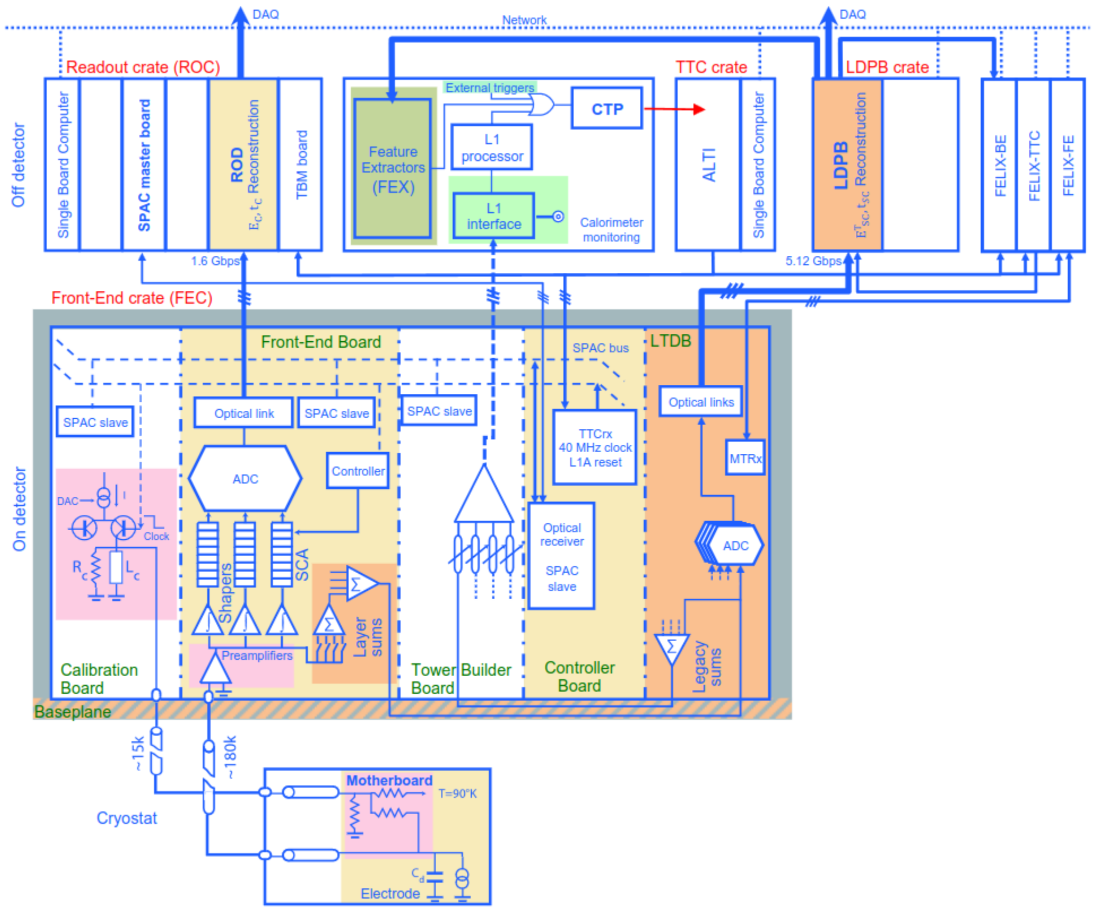

FIGURE 0.3 : Diagramme schématique de l'électronique de lecture LAr actuelle avec les composants de la mise à niveau de la Phase-I mis en évidence en orange.

Avec l'augmentation de la granularité d'un facteur dix, cela permet une segmentation plus fine des cellules appelée Super Cellules (SC). Pour traiter les signaux des Super Cellules, une nouvelle carte est installée sur le détecteur c'est la LAr Trigger Digitizer Board (LTDB). Les LTDB numérisent les signaux des Super Cellules et les transmettent à l'électronique hors détecteur. Le système de traitement numérique LAr, est composé de plusieurs cartes LAr Digital Processing Board (LDPB), avec notamment les LAr Trigger prOcessing MEzzanine (LATOME) qui calculent et reconstruisent les énergies pour enfin les envoyer au système de déclenchement de premier niveau. La Figure 0.3 illustre ce cheminement (partie orange du schéma).

0.4 Amélioration de la performance de l'électronique Phase-I sur le détecteur

La carte LTDB est un composant essentiel de la mise à niveau Phase-I. Au cours de la période de mise en service et de validation, elle a été confrontée à plusieurs problèmes majeurs qui ont affecté sa stabilité et son efficacité : notamment des problèmes de convertisseur analogique numérique (CAN) (étalonnage, sauts de piédestaux dynamiques), ou encore, un décalage temporel induit sur le déclencheur numérique avec un impact sur l'efficacité du calcul et de la reconstruction des énergies mais aussi sur le déclencheur de premier niveau. Des effets de radiation ont également été observés sur les composants LTDB causant des pertes de puissance optique sur les fibres des LTDBs. L'amélioration de la stabilité de l'algorithme de calibration pour permettre une transmission optimale des données à l'électronique hors détecteur a aussi été un aspect important de cette mise en service.

Ce chapitre résume ces problèmes, en expliquant leurs causes et leurs impacts, ainsi que leurs solutions.

0.4.1 CAN

La numérisation du signal est désormais effectuée par les CANs de la LTDB. Le développement d'un circuit intégré spécifique (ASIC) personnalisé fut développé spécialement pour la LTDB. Ce CAN de 12 bits comprend 4 étages avec des multiplicateur de convertisseurs numériques analogiques (MDAC) de 1,5 bit et un registre d'approximation successive (SAR) de 8 bits, offrant une haute précision. La calibration des MDAC est cruciale pour éviter les erreurs de non-linéarité dans la numérisation du signal et donc affecter négativement les performances du déclencheur. Il est donc nécessaire de calibrer tous les MDAC des LTDBs. Pour ce faire le processus de calibration est le suivant : La tension de sortie du MDAC est comparée à celle de l'entrée pour établir le gain qui doit idéalement être de 2. Cependant il est possible de corriger ce gain à l'aide de constante, ces constantes seront donc calculées et ajustée pour que le gain se rapproche le plus possible de deux. Une longue étude a laquelle j'ai activement pris part, a été faite pour obtenir les constantes de calibration des MDAC afin de régler correctement tous les canaux pour avoir une efficacité optimale sur la numérisation du signal du détecteur. Une fois ce problème résolut un autre problème est apparu. Le changement dynamique de piédestaux, qui pendant une prise de donnée a un impact direct sur le système de déclenchement. Ce problème est en cours d'investigation, il semblerai être lié à un problème analogique des CAN puisque les 4 canaux du CAN sont affectés de la même manière. Un correctif a été mise en place dans le firmware de la LATOME pour minimiser son impact sur le système de déclenchement. Les figures 0.4 illustrent ces deux phénomènes.

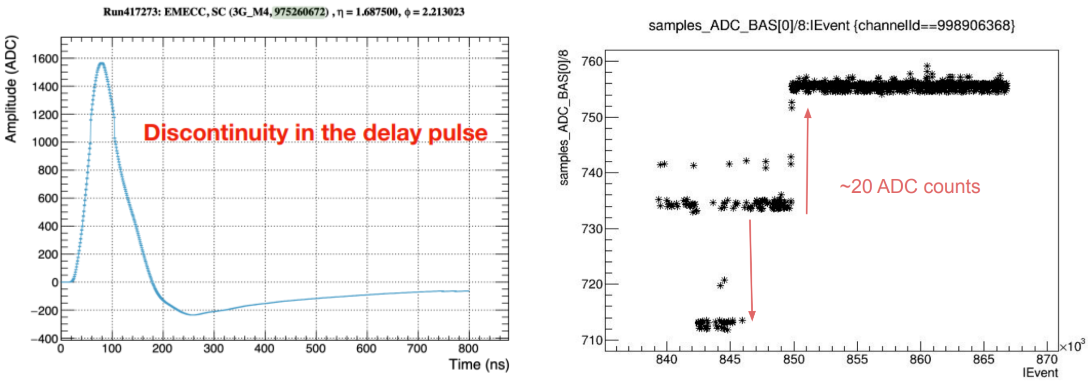

FIGURE 0.4 : A gauche discontinuité dans l'impulsion du CAN due à une mauvaise constante du MDAC; A droite mesure de la réponse d'une super cellule dans laquelle le CAN a présenté des sauts de piédestal.

0.4.2 Décalage temporel

La reconstruction de l'énergie déposée dans les cellules du calorimètre est réalisée par l'algorithme des coefficients de filtrage optimaux (OFC) [6]. Afin d'avoir une reconstruction optimale de l'énergie, la phase des OFC a été choisie au plus près de l'amplitude maximum de l'énergie pour tous les canaux du déclencheur numérique. Des calibrations sont nécessaires pour effectuer cet ajustement. La Figure 0.5 illustre un échantillonnage idéal. Cependant, lors d'une analyse de donnée de calibration quotidienne, un problème de positionnement a été observé sur plusieurs Super Cellules. Plus précisément, le pic de l'échantillonnage de certains canaux a montré un décalage temporel de quelques nanosecondes que l'on appellera τ. Ce décalage temporel signifie que le choix de la phase OFC n'est plus positionné sur l'amplitude maximal de l'énergie déposée dans cette Super Cellule. Ce décalage temporel est susceptible d'impacter les performances du système de déclenchement numérique. L'étude détaillé ci-dessous explique le travail que j'ai effectué pour identifier la source du problème ainsi que son impact sur le système.

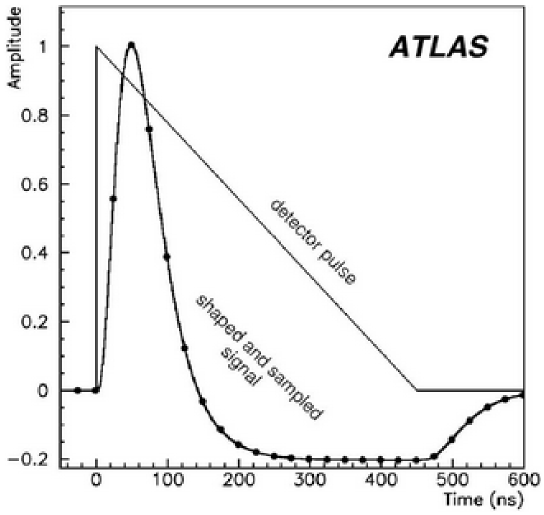

FIGURE 0.5 : Forme de l'impulsion du détecteur avant et après la numérisation.

L'étude a commencé par examiner si le redémarrage avec la coupure d'alimentation des machines FE FELIX LTDB (cartes FLX-712 qui assurent la configuration des LTDBs) provoquait un décalage temporel. La Figure 0.6 illustre la variation du décalage temporel (τ) entre deux runs de calibration pour chaque Super Cellules après une coupure d'alimentation des machines. Le graphique confirme que cette coupure d'alimentation provoque un décalage temporel dans de nombreuses Super Cellules connectées à ces machines. De plus une mesure systématique des valeurs de τ a été effectuée sur l'ensemble du détecteur et par couche, les valeurs de τ se situent dans une plage autour des 5ns.

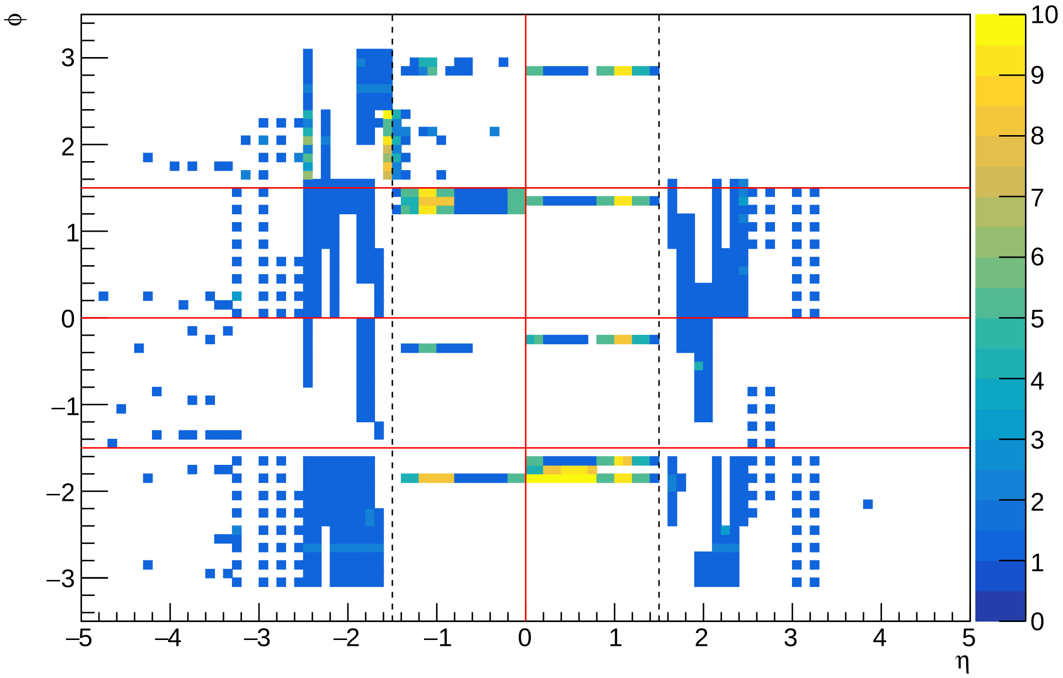

FIGURE 0.6 : Distribution des Super Cellules ayant une valeur de $|\tau| > 3ns$ dans l'espace η/ϕ, l'axe z montre le nombre de Super Cellules. De haut en bas sont les machine FE FELIX LTDBs 05, 04, 07 and 06 couvrant le coté C du détecteur($\eta < 0$). Les machines 01, 00, 03 and 02 couvrant le coté A (η>0). Les lignes noir en pointiller délimite le tonneau du bouchon.

Plusieurs tests ont été menés avec des modifications matérielles/logicielles apportées à l'électronique du détecteur : réinitialisation du composant GBTx, désactivation/activation de la lumière sur le μPOD de la carte FLX-712, désactivation/activation du flux TTC, reproduction du problème sur un banc d'essai et interversion des connecteurs à l'arrière de la carte FLX-712.

Une analyse plus approfondie de ce dernier point a démontré que certains canaux sont plus souvent affectés par ce décalage temporel que d'autres. Ceci a permis d'identifier le problème comme venant de la carte FLX-712.

Une calibration spéciale a été menée pour évaluer l'impact du décalage temporel induits par la coupure d'alimentation des machines FE FELIX LTDB sur la reconstruction des énergies. Pour cela, toutes les Super Cellules ont été pulsées simultanément avec un décalage temporel variables de 0ns à 24ns, cela permet d'obtenir la forme complète de l'impulsion. Ensuite la moyenne des énergies a été calculée pour toutes les valeurs du décalage temporel du pic de l'échantillonnage, pour pouvoir calculer le ratio d'efficacité de la reconstruction d'énergie entre les Super Cellules correctement allignée en temps et celles avec un décalage temporel de ±5ns. Les résultats ont indiqué une perte estimée dans la reconstruction de l'énergie ≈ 1% pour l'EMB, ≈ 1.5%

pour l'EMEC, ≈ 1.1% pour le HEC et ≈ 3.4% pour le FCal. Cependant, lors d'une prise de données avec certaines Super Cellules avec un décalage temporel incorrect, le déclencheur a été significativement impacté, entraînant une perte de performance allant jusqu'à 15% sur certaines régions du détecteur.

La source du problème a été identifiée comme venant du coté FELIX, cependant le problème n'a pas encore été compris et résolut. Le travail en collaboration avec des expert FELIX est toujours en cours.

0.4.3 Effet de radiation sur les fibres

Le suivi de la puissance lumineuse des fibres de données et de contrôle a permis d'identifier une réduction inquiétante de 10% de la puissance lumineuse pour tous les LTDB du tonneau au cours de la prise de données en 2022, affectant à la fois les fibres de données et de contrôle comme illustrés dans la Figure 0.7. Ce phenomène a fait l'objet d'une intense campagne de tests et d'études a laquelle j'ai activement contribuée, pour le comprendre et en cerner l'impact à venir.

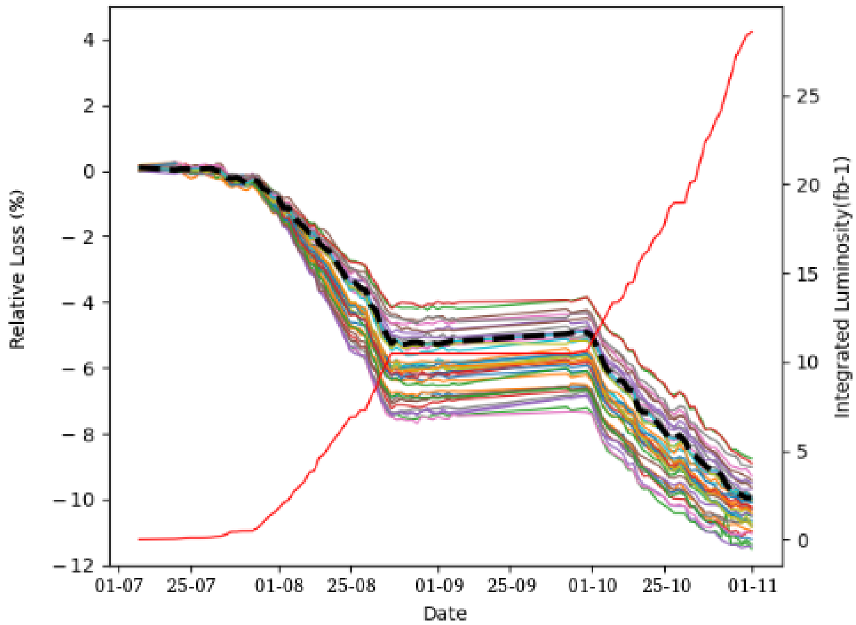

FIGURE 0.7 : Perte de la puissance optique et évolution de la luminosité du LHC en fonction du temps

Cette réduction a été moins observée sur les LTDB du bouchon au moment de la découverte du problème. Cette diminution est potentiellement attribuée à un effet de radiation, comme le suggère son impact plus prononcé sur les LTDB du tonneau par rapport à ceux du bouchon, en raison de leur localisation sur le détecteur. Des tests ont été effectués sur les harnais de fibres à l'intérieur de la LTDB ainsi que sur les fibres entre les LTDBs et les LATOMEs. Des tests sur la composition de la fibre optique à la recherche de phosphore qui pourrait noircir la fibre et donc induire cette réduction de lumière. Des tests de radiation ont aussi été conduits pour voir l'impact des radiations sur ces fibres au fil du temps. Le harnais de fibre de la LTDB et les fibres entre les LTDBs et les LATOMEs ont été mis hors de cause. Les Miniature optical Transmitter (MTx pour les fibres de données et MTRx pour les fibres de contrôle de la LTDB) ont également été testés pour valider que la cause de cette perte optique réside dans ces composants. Les tests de radiation effectués sur des modules de rechange confirment le phénomène observé sur le détecteur. Une perte de puissance initial qui tend vers une stabilisation après environ 40 kRad. Les études de production de ces composants montrent aussi cet effet de perte de puissance initiale qui avais été observé lors des premiers tests d'irradiation effectué pour valider les spécifications de ces composants avant leur production. D'autre part un effet de recuit, ou annealing en anglais, a été observé pendant l'arrêt prolongé du LHC en 2022, en accord avec les observations initiales de préproduction, ce qui confirme nos hypothèses. Maintenant que la cause est identifiée et comprise, aucune action n'est nécessaire et le suivi de la puissance lumineuse des liens de données et de contrôle des LTDB a été amélioré pour une meilleure lecture et un meilleur suivi de ce phénomène.

0.4.4 Sélection de phase pour la transmission de données

Après la numérisation des données reçues par les LTDBs, les données sont encodées et transmises aux LATOMEs. Pour garantir cela, il est nécessaire que l'horloge du CAN et l'horloge interne de l'encodeur LOCic soient déphasées. Pour ajuster la différence de phase entre ces horloges, deux possibilités sont envisagées : ajouter un délai au signal d'horloge du CAN à l'entrée du LOCic ou ajouter un délai au signal d'horloge du GBTx à sa sortie. J'ai activement contribueé aux études de ces deux méthodes de calibration pour effectuer la sélection de phase de façon optimal.

La méthode de calibration LOCx2 scan applique un délai à l'horloge d'entrée du LOCic encoder provenant des CAN. Le processus analyse toutes les valeurs de délai possibles, vérifie le taux d'erreur sur les fibres correspondantes, et varie de 9 à 25 avec chaque pas correspondant à 220 ps. Les taux d'erreur sont observés pendant 5 secondes pour chaque lien. Le meilleur délai est choisi en fonction de la plus grande plage continue sans erreurs. Cependant, cette méthode pourrait ne pas détecter les erreurs à faible taux sans en augmenter significativement la durée de l'analyse. Une approche alternative a été proposée, impliquant d'identifier le délai de plus mauvais cas et de sélectionner celui qui en est le plus éloigné, mais cela ne peut pas être réalisé à l'aide de l'analyse LOCx2 en raison de limitations dans la numérisation de la période complète de l'horloge interne du LOCic.

La méthode de calibration ClkDes scan est illustrée en Figure 0.8. Sur le GBTx, l'horloge peut être retardée par quatre-vingts pas de 48,8 ps. Comme dans la première méthode de calibration, toutes les valeurs de délai possibles sont analysées et le taux d'erreur correspondant est vérifié sur les liens correspondants sur les LATOMEs. Comme l'ensemble de la plage de l'horloge est scannée, l'analyse trouve toujours le plus mauvais délai où le LOCic est mal encodé. Le meilleur délai se situe au milieu de l'intervalle entre les mauvais délais des deux liens utilisant la même horloge GBTx. Cette méthode a réduit la durée de la calibration par rapport à celle du décalage de phase LOCx2. De plus, elle a montré une meilleure stabilité au fil du temps sur le détecteur. Cependant, il était toujours nécessaire de reprendre des calibrations environ une fois par semaine, alors que cela n'aurait du être fait qu'une seule fois après une mise sous tension de la carte LTDB car la PLL du composant LOCx2 ne possède pas de boucle de rétroaction donc elle a besoin d'être configuré à chaque mise sous tension.

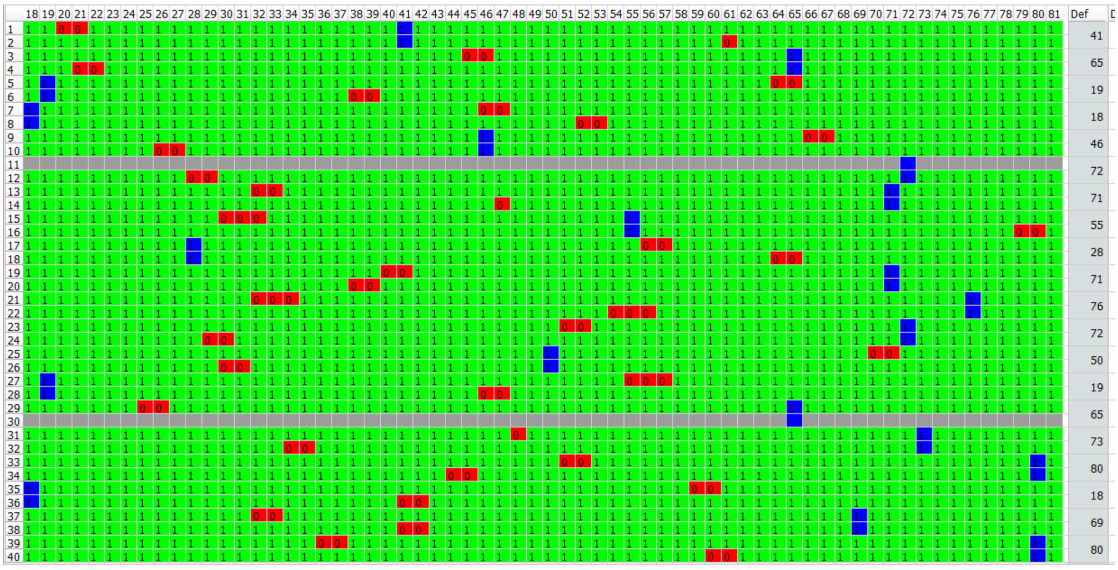

FIGURE 0.8 : Résultats d'une calibration ClkDes scan pour une LTDB. Les cases vertes : les délais sans erreur; les cases rouges : les délais avec des erreurs; les cases bleues représentent le délai final sélectionné par l'algorithme.

Pour ce faire, des améliorations ont été apportées pour résoudre ce problème de stabilité. Plusieurs durées de vérification des erreurs ont été testées, de la vérification instantanée jusqu'à 5 secondes de vérification. Une vérification d'une seconde a été gardée, qui est le parfait mixte entre rapidité et précision. Le temps d'attente avant le changement du délai est passé de 100 ms à 500 ms et la réinitialisation des GBTx sur la LTDB ainsi que des émetteurs-récepteurs des LATOMEs ont été mises en place avant le lancement de la calibration. Cela a permis de gagner en stabilité. Depuis la mise en place de ces améliorations, la sélection de la phase de transmission des données est devenue très stable, elle est effectuée seulement une fois après la mise sous tension de la LTDB.

Remerciements

First and foremost, I would like to express my deepest gratitude to my supervisors, Emmanuel MONNIER and Luis HERVAS, for their unwavering support, invaluable guidance, and insightful advice throughout my three years in the LAr team.

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I would like to acknowledge the LAr operation team for their help in understanding the complex LAr detector, sharing invaluable knowledge on the ATLAS detector and the liquid Argon system.

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Introduction

The pursuit of modern physics is aimed at elucidating and potentially unifying the fundamental forces governing the universe. Despite the remarkable success of the Standard Model of particle physics, which describes the strong, weak, and electromagnetic forces on fermions, via gauge bosons, and the Higgs boson, it remains incomplete. Notably, gravity remains outside its purview, alongside other unexplained phenomena such as the existence of three generations of quarks and leptons, neutrino masses, dark matter, and dark energy. These gaps underscore the need for a more comprehensive theory.

In this quest for deeper understanding, institutions like CERN (European Organization for Nuclear Research) play an important role. CERN is home to the Large Hadron Collider (LHC), the world's most powerful particle accelerator with a center of mass collision energy up to 14TeV, where cutting-edge experiments are conducted to explore the frontiers of particle physics.

These experiments are built around four collision points of the LHC. On each of these points, a detector is installed (ATLAS, CMS, LHCb, and ALICE) contributing with their distinct capabilities to the scientific mission. ATLAS and CMS are the two generalist LHC experiments, involved in the discovery of the Higgs boson in July 2012, and also designed to search for evidences of theories of particle physics beyond the Standard Model. LHCb is a specialized b-physics experiment, designed primarily to measure the parameters of CP violation in the interactions of b-hadrons (strongly interacting particles containing a bottom quark). Such studies can help to explain the matter-antimatter asymmetry of the universe. ALICE is designed to study quark-gluon plasma, in heavy ion collisions.

The ATLAS detector is meticulously designed to conduct a wide variety of measurements, ranging from fundamental Standard Model evaluations to precision examinations of the Higgs boson and potential new particles. Located underground, ATLAS operates at peak luminosities of $2-3\times10^{34}cm^{-2}s^{-1}$, with a collision rate of 40 MHz at 13.6 TeV. To optimize particle detection, ATLAS employs a sophisticated three-level trigger system, crucial for data acquisition and analysis.

In order to further look for evidence of new physics and continue the studies of the Higgs boson it was decided to upgrade the LHC, the High-Luminosity LHC (HL-LHC) upgrade. With this upgrade, the LHC targets a higher luminosity and an increase of energy to 14 TeV. To cope with this new luminosity the ATLAS detector will be upgraded, the first phase will be installed during the LS2 until the beginning of 2022, and the second phase is scheduled to start in the beginning of 2026. These developments will allow the HL-LHC to have an integrated luminosity up to 4000 fb^{-1}in 10 years, multiplying by an order of magnitude the amount of data compared to previous data acquisition. These new data will allow to study rare events and give greater precision than ever before.

Looking ahead, the forthcoming Run 3 and subsequent HL-LHC installations promise to push the boundaries of scientific exploration, with anticipated luminosities of up to $7 \times 10^{34} cm^{-2} s^{-1}$. These developments represent significant opportunities to explore the mysteries of the universe and advance our understanding of fundamental physics.

1 ATLAS Experiment

Summary

1.1 Standard model

The Standard Model (SM) of the particle physic [7, 8, 9] stands as the cornerstone of modern physics, offering a comprehensive theoretical framework elucidating the electromagnetic, weak, and strong interactions governing elementary particles. This model has achieved remarkable success in explaining diverse phenomena observed in particle physics experiments. At its core are elementary particles, quarks and leptons, which intricately combine to form the building blocks of matter, including protons and neutrons.

Forces within the SM manifest as electromagnetic, weak, and strong forces. The electromagnetic force, governed by Quantum ElectroDynamics (QED), is mediated by photons, elucidating how charged particles interact. The weak force, responsible for processes like beta decay, is mediated by W and Z bosons, and electroweak theory unifies electromagnetism and the weak force. Quantum ChromoDynamics (QCD) describes the strong force, acting on quarks and gluons, binding them within particles like protons and neutrons 1.1.

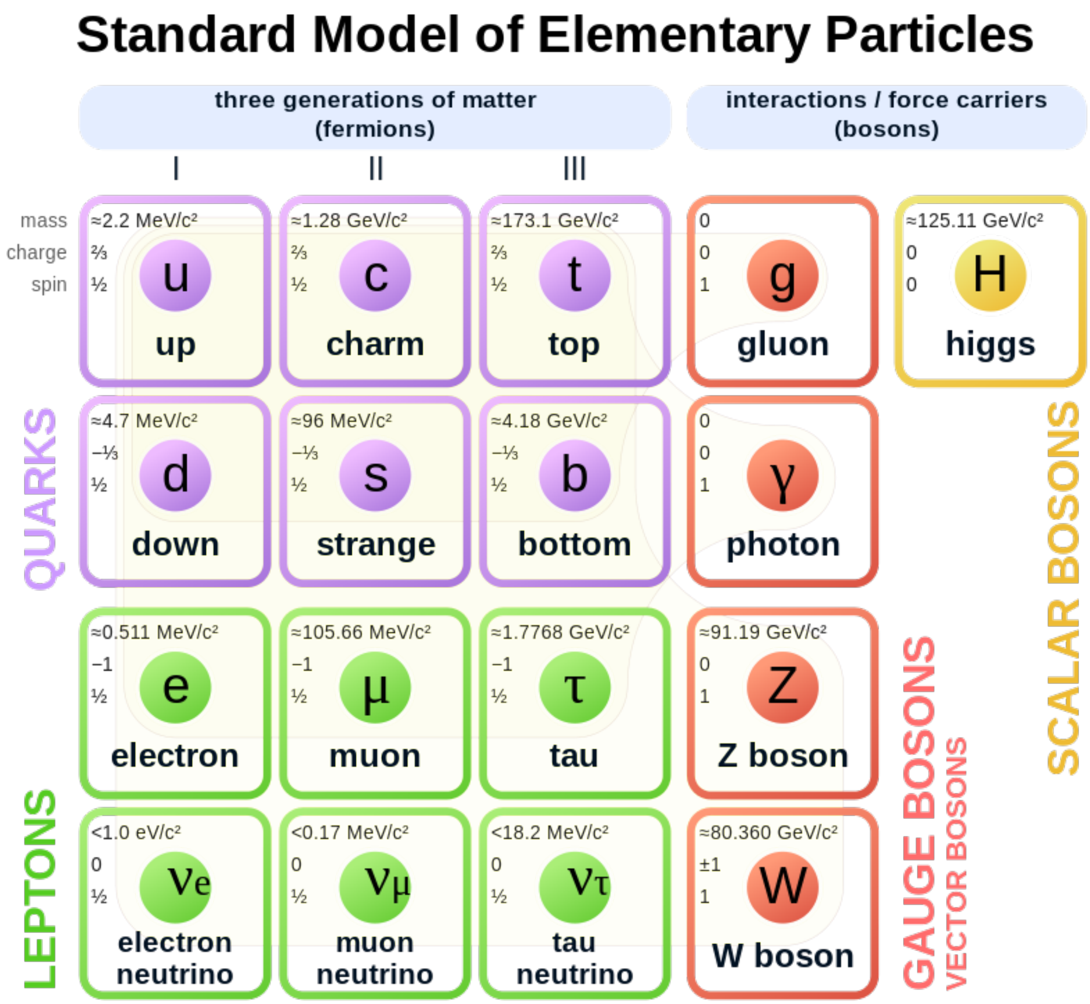


Figure 1.1: Particles of the Standard Model of particle physics [10].

Integral to the model are bosons, including gauge bosons like photons, W and Z bosons [9], and gluons, which facilitate force interactions between particles. The Higgs mechanism introduces the Higgs boson and field, providing insight into the origin of particle mass.

The SM is underpinned by symmetries and conservation laws, such as the conservation of electric charge, lepton number, and baryon number. Experimental validations, including the discovery of W and Z bosons in 1983 [11] and the Higgs boson in 2012 [12, 13] at the European Organization for Nuclear Research (CERN) with the Large Hadron Collider (LHC) [14], have marked pivotal milestones, affirming the model's predictions.

However, the SM faces limitations, lacking an incorporation of gravity and explanations for dark matter and dark energy [15, 16]. Neutrino masses initially assumed to be zero, were found to be small, necessitating model extensions. Contemporary research explores theories like super-symmetry and grand unified theories [17] to address these gaps.

ATLAS (A Toroidal LHC ApparatuS) [18], an integral part of CERN's research endeavors, contributes to diverse goals, from Higgs boson discovery to probing dark matter and phenomena beyond the Standard Model. CERN, with its LHC and ATLAS experiments, remains at the forefront of experimental particle physics. The monumental 2012 discovery of the Higgs boson underscored CERN's pivotal role and ongoing experiments with ATLAS continually refine our understanding of the universe's fundamental particles and forces. In essence, CERN and ATLAS propel global scientific efforts to unravel the mysteries of the universe at its smallest scales.

1.2 CERN

CERN, was founded in 1954. It is the world's largest particle physics laboratory and is located near Geneva, Switzerland.

CERN was established with the aim of creating a collaborative scientific environment where researchers from different countries could come together to study the fundamental properties of matter. At its inception, CERN had 12 member states, but it has since grown to include 23 member states and several non-member states.

One of the primary motivations behind the creation of CERN was to rebuild Europe's scientific infrastructure following the devastation of World War II. By pooling resources and expertise, European countries hoped to make significant advancements in the field of particle physics.

In the early years, CERN focused on building its first particle accelerator, the Proton Synchrotron (PS), which became operational in 1959. This accelerator was a significant milestone in the field of particle physics, as it allowed scientists to study particles at energies never before achieved.

Throughout the following decades, CERN continued to expand its research capabilities and build increasingly powerful particle accelerators. In 1971, the Super Proton Synchrotron (SPS) was completed, followed by the Large Electron-Positron collider (LEP) in 1989.

However, one of CERN's most important achievements was the construction of the Large Hadron Collider(LHC), which began operating in 2008. The LHC is the world's largest and most powerful particle accelerator, capable of colliding protons at unprecedented energies. It has enabled scientists to make groundbreaking discoveries, including the observation of the Higgs boson in 2012.

In addition to its research activities, CERN also plays a crucial role in fostering international collaboration and education in the field of particle physics. It hosts thousands of scientists from around the world who come to conduct research at its facilities and participates in numerous outreach programs aimed at engaging the public in science.

1.3 The accelerator complex

The CERN accelerator complex seen in Figure 1.2 is a series of particle accelerators and associated facilities. These accelerators work together to provide increasingly higher energies for particle collisions.

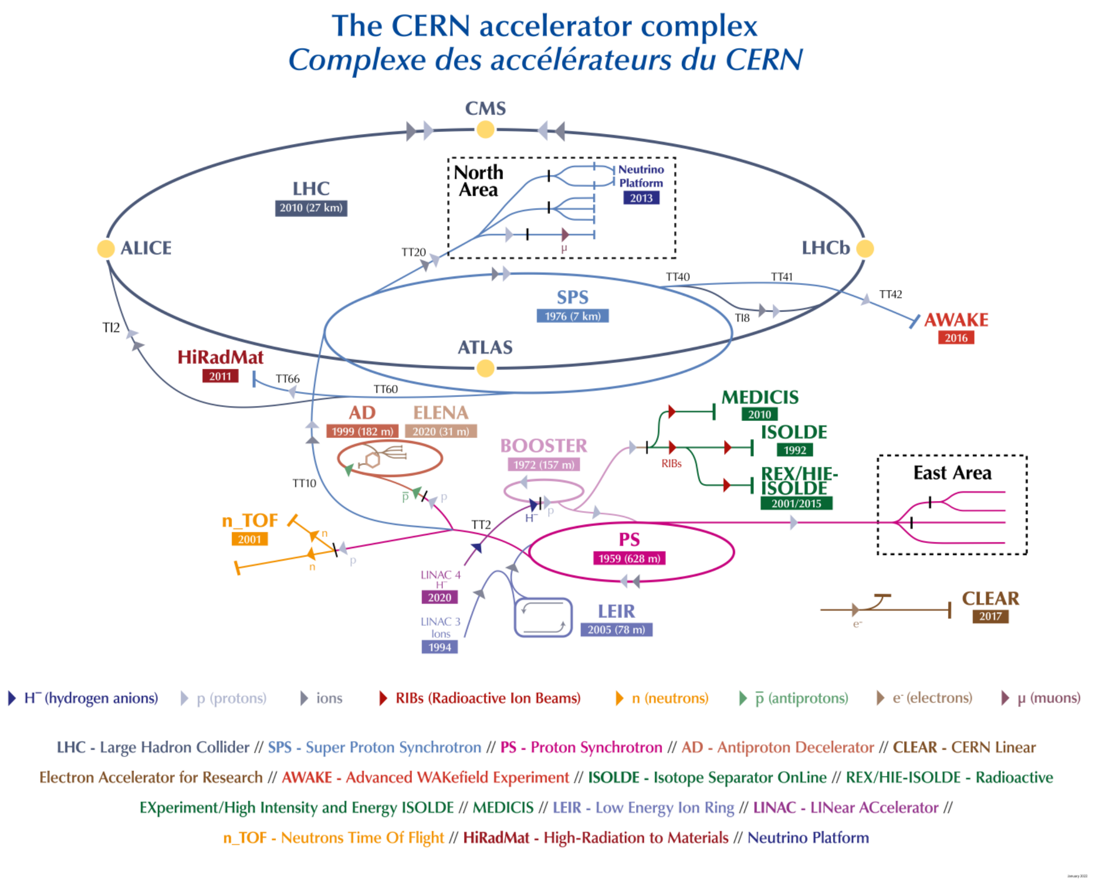


Figure 1.2: CERN accelerator complex [19]

The particle accelerator complex at CERN, depicted in Figure 1.2, comprises a series of machines engineered to propel particles to increasingly higher energies. Each machine in this sequence amplifies the energy of a particle beam before transferring it to the subsequent machine. At the culmination of this chain lies the Large Hadron Collider (LHC), where particle beams are accelerated to an impressive energy level of 6.8 TeV per beam.

In 2020, Linear Accelerator 4 (Linac4) commenced operations as the source of proton beams for the CERN accelerator complex. Linac4 accelerates negative hydrogen ions (H-) to 160 MeV to prepare them for injection into the Proton Synchrotron Booster (PSB). During the injection process from Linac4 to the PSB, these ions undergo stripping, shedding their two electrons and leaving behind protons. These protons are then accelerated to 2 GeV before being injected into the Proton Synchrotron (PS) [20], which further boosts their energy to 26 GeV. Subsequently, the protons are directed to the Super Proton Synchrotron (SPS) [21], where their energy is ramped up to 450 GeV.

Ultimately, the protons are transferred to the two beam pipes of the LHC, with one beam circulating clockwise and the other anticlockwise. Each LHC ring takes 4 minutes and 20 seconds to be filled, and it requires approximately 20 minutes for the protons to reach their peak energy of 6.8 TeV. The particle beams can circulate within the LHC beam pipes for extended periods under normal operating conditions. Inside the LHC, collisions occur within four detectors – ATLAS, CMS [22], ALICE [23], and LHCb [24] – where the collision energy reaches a total up to 13.6 TeV.

However, protons are not the sole particles accelerated within the LHC. Lead ions utilized for experiments within the LHC begin as vaporized lead and enter Linac3. Subsequently, they are gathered and accelerated in the Low Energy Ion Ring (LEIR), following the same energy acceleration pathway as protons.

The accelerator complex at CERN plays a pivotal role in facilitating a diverse array of experimental programs, extending beyond the operations of the LHC. Throughout the accelerator chain, numerous experimental halls are dedicated to conducting experiments at varying energy levels.

The Proton Synchrotron Booster (PSB) supports the functionality of the Online Isotope Mass Separator (ISOLDE) facility, including HIE-ISOLDE, alongside the Medical Isotopes Collected from ISOLDE facility (MEDICIS is dedicated to the production of innovative radioisotopes for medical research and applications, particularly in the field of nuclear medicine) facility.

The Proton Synchrotron (PS) is instrumental in powering the Antiproton Decelerator and facilitates experiments at the neutron time-of-flight (n_TOF) facility. Additionally, it accommodates the East Area, is one of the experimental zones where a variety of fixed-target experiments are conducted using beams of particles produced by the PS. The purpose of these experiments is to explore different aspects of particle physics, nuclear physics, and other related fields.

The Super Proton Synchrotron (SPS) serves as a crucial hub for various experiments located in the North Area. Is another significant experimental zone that hosts a variety of high-energy physics experiments. It utilizes beams from the SPS and serves several important purposes: Fixed-Target Experiments, Heavy-Ion Physics, Neutrino Research, Hadron Structure and Dynamics, Detector Development and Calibration, Interdisciplinary Research and Applications, Training and Education, Collaboration and International Projects.

Meanwhile, the LHC hosts four major experiments - ATLAS, CMS, ALICE, and LHCb. - alongside smaller-scale experiments like TOTEM, LHCf, MoEDAL-MAPP, FASER, and SND@LHC.

1.3.1 Large Hadron Collider

The LHC stands as the world's largest and most potent particle accelerator, marking a monumental addition to CERN's complex since its inauguration on 10 September 2008.

Spanning a colossal 27-kilometre ring, the LHC comprises an array of superconducting magnets [25] and accelerating structures meticulously designed to propel particles to unprecedented energies.

Within the accelerator, two high-energy particle beams travel at nearly the speed of light before colliding. Enclosed within separate ultrahigh vacuum beam pipes, these beams traverse in opposite directions, steered along their circular trajectory by a magnetic field upheld by superconducting electromagnets. Crafted from specialized electric cable coils operating in a superconductive state, these electromagnets conduct electricity with remarkable efficiency, devoid of resistance or energy loss. This necessitates the chilling of the magnets to a temperature of -271.3°C – colder than the void of outer space. Consequently, a comprehensive distribution system of liquid helium is employed to cool the magnets and cater to other essential supply services.

The LHC boasts an extensive array of magnets, each meticulously designed to manipulate the beams' trajectories throughout the accelerator. Among these are the 1232 dipole magnets, 15 meters in length, responsible for deflecting the beams, and the 392 quadrupole magnets, ranging from 5 to 7 meters long, dedicated to focusing the beams. Additionally, specialized magnets are employed just before collision to "squeeze" the particles closer together, increasing the luminosity. The precision required for this task is akin to aiming two needles ten kilometers apart with such accuracy that they converge seamlessly halfway.

Unified within the CERN Control Centre, all the controls governing the accelerator, its auxiliary services, and technical infrastructure converge. From this centralized hub, commands are issued to orchestrate collisions within the LHC at four designated locations encircling the accelerator ring, aligning with the positions of four pivotal particle detectors – namely, ATLAS, CMS, ALICE, and LHCb.

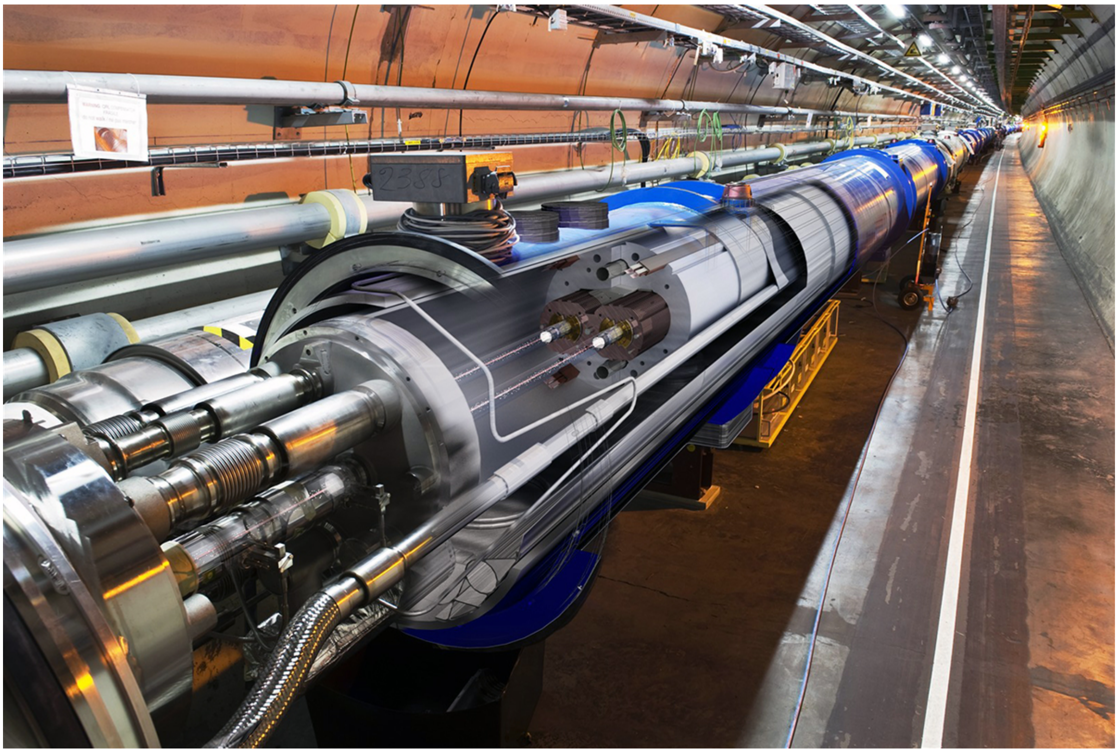


Figure 1.3: View of the LHC tunnel with an artistic cut through a LHC dipole magnet, highlighting the twin magnet coils as well as the two vacuum chambers. [26]

1.3.2 High-Luminosity Large Hadron Collider

The High-Luminosity Large Hadron Collider (HL-LHC) is a major upgrade to the existing LHC facility. The primary goal of the HL-LHC is to boost the luminosity of the LHC by a factor of ten compared to its initial design, thereby increasing the rate of collisions between particles. This increase in luminosity will allow scientists to collect a larger volume of collision data, enhancing their ability to study rare processes and phenomena. To reach such luminosity it requires extensive upgrades to the LHC infrastructure, including improvements to the superconducting magnets, beam focusing systems, and particle detectors. New technologies and innovative engineering solutions are being developed and implemented to meet the demanding requirements of the HL-LHC.

The HL-LHC project has been in development for several years, with planning (see Figure 1.4), design and construction phases underway. The timeline for implementation includes extensive testing and commissioning before the upgraded facility becomes fully operational.

Overall, the HL-LHC represents a significant milestone in the field of particle physics, offering the potential to revolutionize our understanding of the fundamental nature of the cosmos and the laws that govern it.

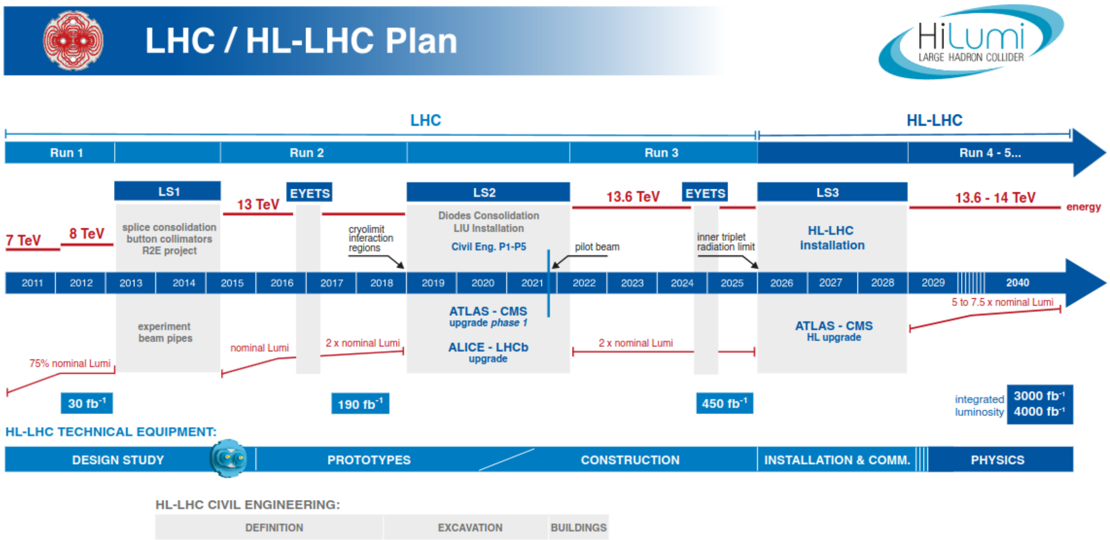


Figure 1.4: The LHC schedule up to the HL-LHC.[27]

1.4 ATLAS

The ATLAS detector shown in Figure 1.5 is the largest particle detector ever constructed. It measures 46 meters in length, 25 meters in height, and 25 meters in width, and weighs 7000 tonnes. It is located in an underground cavern, 100 meters below the surface, near the main site of CERN and the town of Meyrin, Switzerland. Along with CMS, it is one of the two multipurpose detectors of the LHC. It studies a wide range of physics domains, from the search for the Higgs boson to the existence of extra dimensions in space time, as well as particles that could make up dark matter. Over 6,000 members from 182 institutes, representing 42 countries, work on the ATLAS experiment.

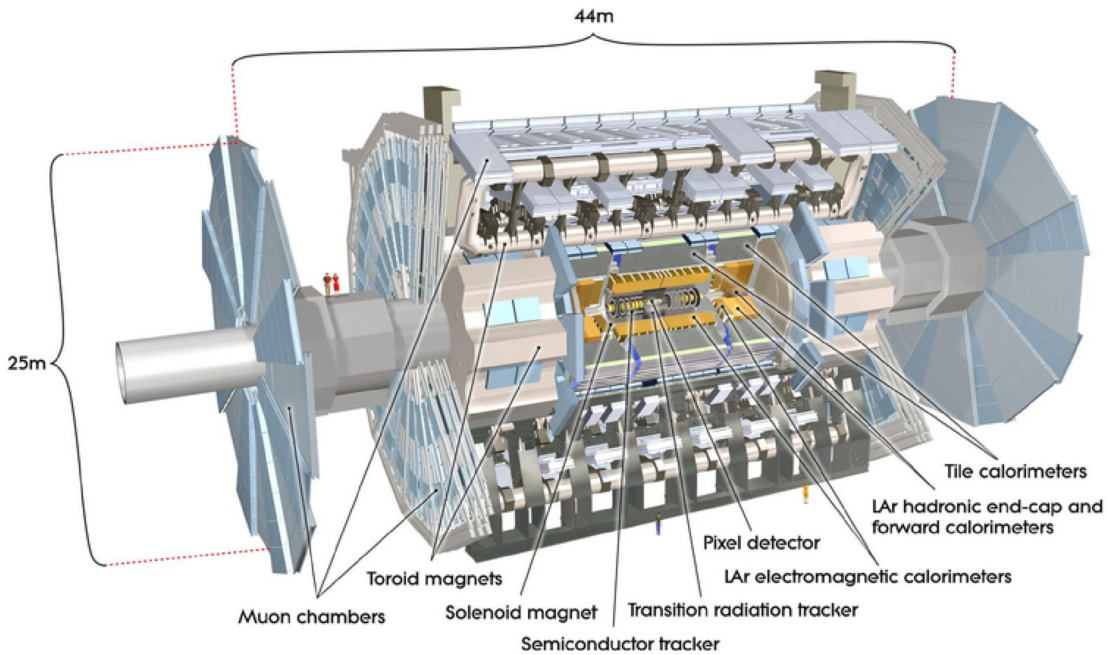


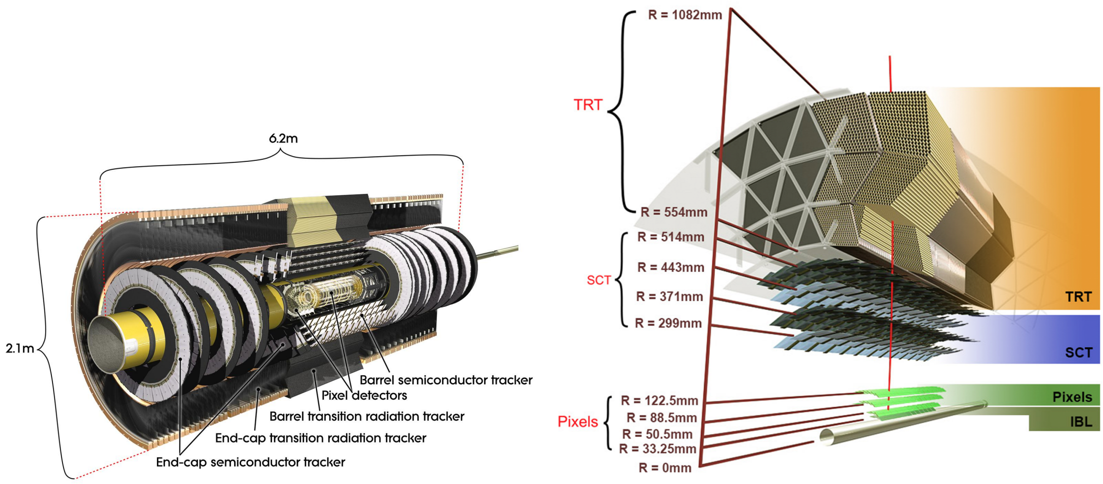
Figure 1.5: ATLAS Detector [4]

The particle beams of the LHC collide at the center of this detector, with an energy of 13.6TeV and a collision frequency of 40 MHz. These beams produce a multitude of new particles that emerge from the collision point in all directions. Six different detection subsystems arranged in layers around the collision point record the trajectory, momentum, and energy of the newly emitted particles, allowing for their identification. This information enables particle identification and event reconstruction. A tremendous amount of data is generated in the process, about 1.4MB per event, multiplied by 40 million beam crossings per second (40 MHz). This produces a total of 56 terabytes (equivalent to 2000 years of MP3-encoded music) of data per second. It is not possible to store and analyze all of this data. Therefore, ATLAS has a trigger system that determines the relevance of events, either recording them or discarding them to pass from a rate of 40 MHz to 100 kHz after the first trigger level. Then the High-level trigger will reduce the rate of events from 100kHz to 4 kHz. The remaining data, corresponding to about 4,000 events per second, are stored for further analysis. Acquisition and computing systems are then used to analyze and store these events, with the calculations distributed across multiple servers.

1.4.1 ATLAS Inner detector

The Inner Detector (ID) [28, 29], positioned a few centimeters away from the proton beam axis and extending to a radius of 2.1 meters, spans a length of 6.2 meters along the beam pipe. Its primary role is to trace the paths of charged particles by detecting their interactions with materials at discrete locations, providing insights into particle types and their momenta. The magnetic field enveloping the entire inner detector induces curvature in charged particles; the direction and degree of this curvature unveil a particle's charge and momentum, respectively. The origins of these particle tracks offer clues for particle identification; for instance, the detection of tracks emanating from a point distinct from the original proton-proton collision may suggest the decay of a hadron containing a heavy flavor quark.

This vital component comprises four distinct parts, elucidated below.



(a) (b)

Figure 1.6: A cross-section of the ATLAS inner detector system [30]

- **Insertable Barrel Layer:** Integrated during Phase-0 (2013 to 2015), the IBL introduced an additional layer near the beam pipe. Its compact design, featuring a mere 0.2 mm insertion gap, addresses potential tracking efficiency losses with higher luminosity.

- **Pixel Detector:** The PD consists of three layers within the barrel region and three disks in the endcap region. With pixels measuring 50 μm × 400 μm, the PD has 80 million channels and 1744 modules, each approximately 250 μm thick. Operating on the principle of a silicon detector, the PD registers the creation of electron-hole pairs as charged particles traverse the silicon, allowing for precise tracking through subsequent analysis.

- **SemiConductor Tracker:** Situated beyond the PD, the SCT features a barrel composed of four cylinders and two endcaps housing nine disks each. Offering 6.3 million readout channels, the SCT employs readout strips with an 80 μm pitch. Similar to the PD, the SCT also is a silicon detector, measuring the energy deposition of charged particles in the silicon for accurate tracking.

- **Transition Radiation Tracker:** Extending beyond the SCT, the TRT covers an extended pseudorapidity range ($|\eta| < 2$) and is constructed with drift tubes or straws filled with Xenon gas. Utilizing transition radiation, the TRT discriminates between particle types, with the smaller diameter of the straws and their isolation enhancing operational efficiency. Although less accurate than the PD and SCT, the TRT significantly contributes to momentum measurement by covering a larger radial area and collecting up to 36 hits per track.

1.4.2 ATLAS calorimeters

The process of quantifying the energy dissipated by a particle traversing the detector constitutes a critical aspect of particle physics experimentation. Specifically designed to stop the majority of particles originating from a collision, the ATLAS calorimeters (Figure 1.7) cause them to lose all their energy and come to a complete halt within the detector. Comprising layers of a high-density "absorbing" material that halts incoming particles and interspersed with layers of an "active" medium for energy measurement, ATLAS calorimeters play a pivotal role in capturing the dynamics of particle interactions.

Electromagnetic calorimeters serve the purpose of gauging the energy imparted by electrons and photons during their interaction with matter. Concurrently, a hadronic calorimeter samples the energy of hadrons—particles containing quarks, such as protons and neutrons—as they interact with atomic nuclei. Notably, the calorimeter can stop of most known particles, with the exceptions being muons and neutrinos. The ATLAS Calorimetry system is composed of two components: the Liquid Argon (LAr) calorimeters and the Tile Hadronic calorimeter.

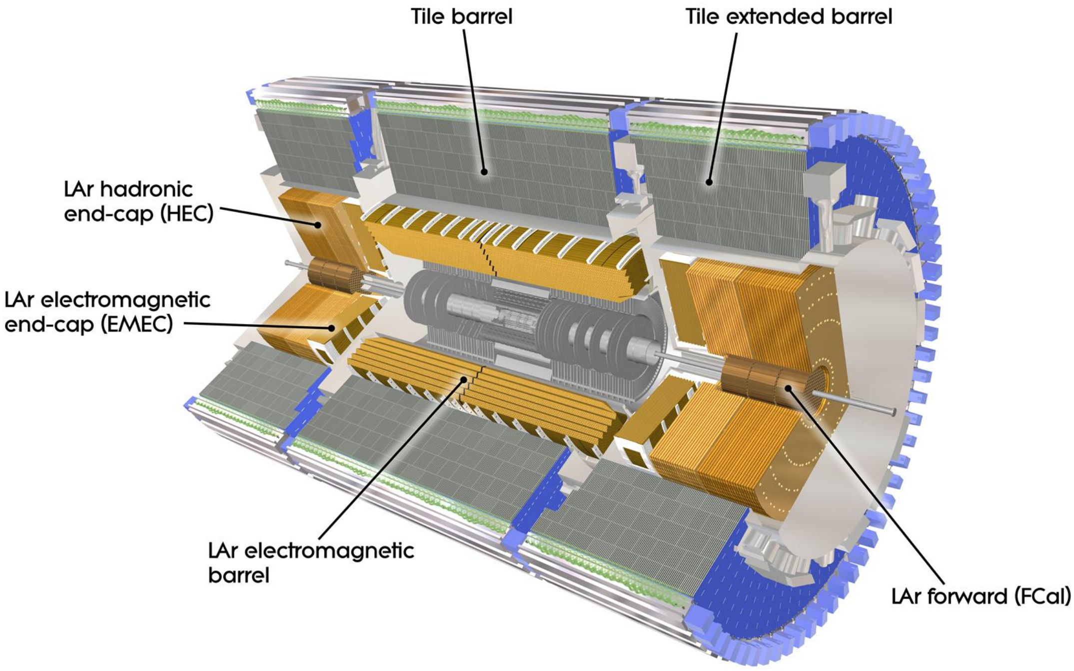


Figure 1.7: ATLAS calorimeters comprising the Liquid Argon electromagnetic calorimeters and the Tile hadronic calorimeter. [5]

Liquid Argon calorimeters:

Encompassing the ATLAS Inner Detector, the Liquid Argon (LAr) calorimeters [5] serve the purpose of quantifying the energy of electrons, photons, and hadrons. Characterized by layers of metal—tungsten, copper, or lead—that absorb incoming particles, subsequently transforming them into a "shower" of new, lower-energy particles, these calorimeters rely on the ionization of liquid argon sandwiched between the layers. The resulting ionization current is then measured, enabling physicists to determine the energy of the initial particle that impacted the detector. The central region of the calorimeter is designed for the identification of electrons and photons, featuring a distinctive accordion structure to ensure comprehensive particle capture. As the LAr calorimeters are the main subject of this thesis there is a more detailed explanation in the subsequent chapter 2 on it.

ATLAS Tile calorimeters:

The Tile calorimeters [31] encompasses the LAr calorimeters, tasked with gauging the energy of hadronic particles that incompletely deposit their energy in the LAr calorimeters. It comprises layers of steel and plastic scintillating tiles. Upon interaction with these layers, particles initiate a cascade of secondary particles, while the plastic scintillators generate photons. These photons are subsequently converted into an electric current, the magnitude of which directly corresponds to the energy of the original particle.

Comprising a synchronized ensemble of approximately 420,000 plastic scintillator tiles, the Tile calorimeters represent the most massive component of the ATLAS experiment, with a mass of nearly 2900 tonnes. The intricately structured central barrel, consisting of 64 wedges each measuring 5.6 meters in length, is complemented by two extended barrels, each featuring 64 wedges with a reduced length of 2.6 meters. This expansive configuration ensures comprehensive coverage and adaptability in capturing the diverse spectrum of hadronic particle interactions.

The core of the Tile calorimeter's functionality lies in its extensive network of scintillating tiles. This substantial array, in conjunction with 9,500 photomultiplier tubes, underlines the precision and robustness of the Tile calorimeter in acquiring data.

1.4.3 ATLAS Muon Spectrometer

The Muon Spectrometer [32] constitutes a pivotal element within the ATLAS experiment, specializing in the detection and momentum measurement of muons within the Pseudorapidity (is a spatial coordinate used in high-energy physics to describe the angle of a particle relative to the beam axis in a collider experiment.) range $|\eta| < 2.7$ and triggering on particles at $|\eta| < 2.4$ (Figure 1.8). The spectrometer's magnetic field of 0.5 to 1 Tesla in the center of each toroid coil, is generated by a large barrel toroid in $|\eta| < 1.4$, complemented by two smaller endcap magnets in $1.6 < |\eta| < 2.7$, resulting in a superposition of magnetic fields within the transition region $1.4 < |\eta| < 1.6$.

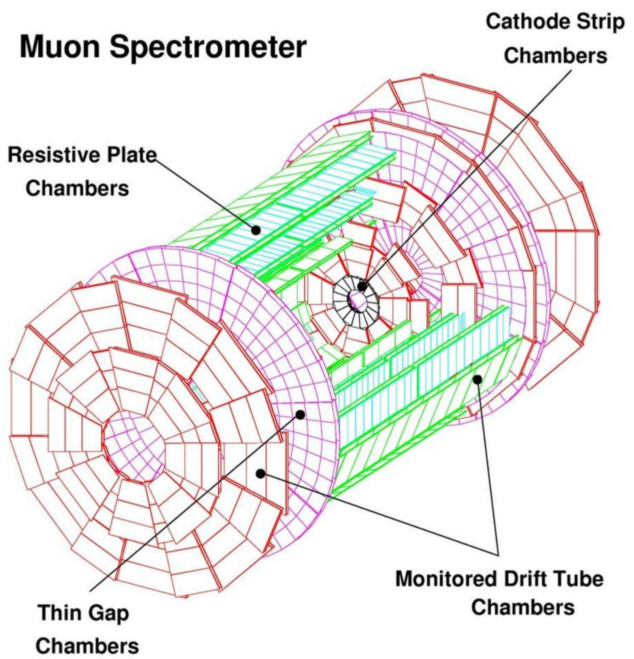


Figure 1.8: Overview of the ATLAS muon spectrometer system [32]

- **Muon Chambers:** The muon chambers are arranged in three cylindrical layers parallel to the beam pipe in the barrel region and perpendicular to the beam in the transition and endcap regions. For precise muon momentum measurements, Thin Gap Chambers (TGCs) [33] and Resistive Plate Chambers (RPCs) [34] are employed. TGCs, positioned in disks in the endcap region ($1.05 < |\eta| < 2.4$), contain two or three 2.8 mm gaps filled with a CO2 and C5H12 mixture. RPCs, utilized for triggering in the central region ($|\eta| < 1.05$), are arranged in three double layers, providing a trigger for muons with transverse momentum in distinct ranges.

- **Monitor Drift Tubes (MDTs) [35] and Cathode Strip Chambers (CSCs) [36]:** For measuring track segments, Monitor Drift Tubes (MDTs) and Cathode Strip Chambers (CSCs) are employed. MDTs consist of aluminum drift tubes filled with a mixture of Argon, CO2, and water vapor, achieving a position resolution of 80 μm per tube layer through a laser alignment system. CSCs cover a region of $2 < |\eta| < 2.7$, utilizing sixteen multi-wire proportional chambers on each endcap disk, filled with a mixture of Argon and CO2. The readout of only cathode strips provides measurements in η and ϕ for each hit.

- **Magnetic Field and Alignment:** The muon spectrometer's magnetic field, essential for the curvature of muon trajectories, is continuously monitored by approximately 1800 Hall sensors distributed throughout the spectrometers. The strength of the magnetic field along muon trajectories is determined with high precision, crucial for accurate momentum measurements. Optical monitoring of deviations from straight lines ensures the required precision in the relative alignment of chambers both within each projective tower and between consecutive layers.

- **Muon Momentum Measurement:** The muon spectrometer facilitates standalone muon momentum measurement with a precision requirement of 30 μm in relative chamber alignment. The alignment process relies on optical monitoring of deviations from straight lines. The initial position accuracy required for the relative positioning of non-adjacent towers is achieved during chamber installation, with further alignment relying on high-momentum muon trajectories when the magnetic field is switched off.

1.4.4 ATLAS Trigger and Data Acquisition system

ATLAS is engineered to monitor an extraordinary rate of up to 40 million proton-proton collisions per second, generating a collective data volume surpassing 50 terabytes per second (40MHz × 3MB = 12×10^{13} B/s = 120 TB/s). Within this voluminous stream of collisions, only a select subset exhibits intriguing characteristics that may lead to novel scientific discoveries. To manage this influx of data effectively, ATLAS employs a specialized event selection system known as the "trigger" (Figure 1.9). The Trigger and Data Acquisition system [37] plays a pivotal role in ensuring optimal conditions for data acquisition, selectively identifying the most interesting collision events for further in-depth study.

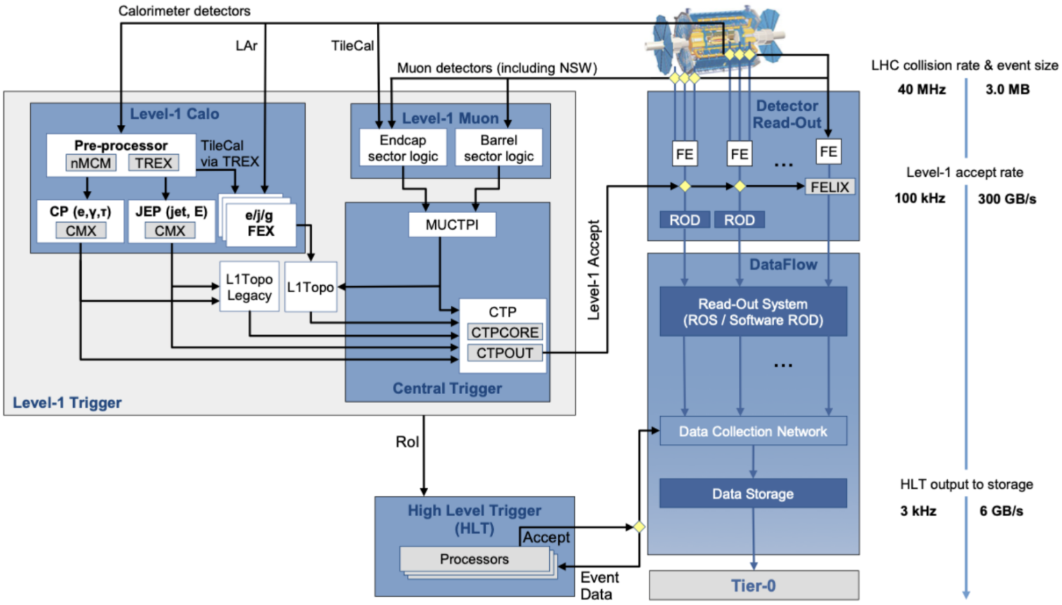


Figure 1.9: Overview of the ATLAS TDAQ infrastructure [37].

Executing this intricate selection process through two distinct stages, the ATLAS trigger system employs a first-level hardware trigger. Crafted with custom-made electronics positioned on the detector, it processes a subset of information sourced from the calorimeter and the Muon Spectrometer. The decision to retain or discard data from an event is made within less than 2.5 microseconds post-event occurrence. During this short interval, the event data is temporarily stored in buffers. If the event is deemed noteworthy, it advances to the second-level trigger, capable of processing up to 100,000 events per second.

Operating on a substantial computational infrastructure featuring approximately 40,000 CPU cores, the second-level software trigger conducts highly detailed analyses of each collision event in just 200 microseconds. Examining closely data from specific detector regions, the second-level trigger selects around 1000 events per second based on these analyses. Subsequently, these chosen events are transmitted to a data storage system, setting the stage for offline analysis and the pursuit of profound scientific insights.

1.4.5 ATLAS Control and Monitoring

The control and monitoring of the ATLAS experiment at CERN rely on several systems, including the Detector Safety System (DSS), Detector Control System (DCS), and the Run Control (RC) application.

- **Detector Safety System (DSS):** The DSS ensures the safe operation of the ATLAS detector by monitoring various parameters such as temperature, pressure, and radiation levels. It continuously checks for any abnormal conditions that could pose a risk to the detector or personnel. In case of emergencies or hazardous situations, the DSS triggers automatic shutdown procedures to prevent damage and ensure the safety of the experiment.

- **Detector Control System (DCS):** The DCS is responsible for the control and monitoring of the ATLAS detector's subsystems and components. It provides real-time monitoring of temperatures, voltages, currents, and other operational parameters. The DCS allows operators to remotely control and configure detector subsystems, perform diagnostic tests, and troubleshoot issues. It also integrates with the DSS to ensure the overall safety and integrity of the detector during operation. More detail about the DCS will be given later.

- **Run Control (RC) Application:** The RC application serves as the central interface for managing the execution of data-taking runs and coordinating activities within the ATLAS experiment. Operators use the RC application to initiate and control data-taking processes, configure detector settings, and monitor the status of data acquisition systems in real-time. It provides a user-friendly interface for starting, pausing, and stopping data acquisition runs, as well as for handling error conditions and managing data storage.

The DCS is structured in a hierarchical manner. The ATLAS DCS organizes top-level commands that cascade down to all sub-systems, ensuring a streamlined approach to control and management. The propagation of errors from sub-systems to the upper-class hierarchy enables efficient issue resolution. The DCS relies on Siemens' Windows control command Open architecture (WinccOa), a Supervisory Control And Data Acquisition (SCADA) software.

Given the heterogeneous nature of different sub-systems, each equipped with distinct hardware, a middleware software layer becomes essential to establish a link between the ATLAS generic SCADA and the specific libraries or protocols of individual sub-systems. The chosen middleware utilizes the Open Platform Communications Unified Architecture (OPC-UA) standard [38], recognized and standardized internationally. This standard aligns seamlessly with the ATLAS architecture's requirements, offering an object-oriented design and platform independence.

To streamline the development, maintenance, and standardization of this middleware, the ATLAS DCS team has developed the Quasar framework, standing for Quick OPC-UA Server generation framework. This framework facilitates server creation, logging, configuration loading, and OPC-UA address space access based on descriptions in "Design" XML files. The address space, accessible to clients, is a crucial component managed by Quasar. While Quasar handles the majority of the framework, the code specific to sub-systems, known as device logic, interfaces with the system's electronics through libraries named device access layer.

Clients interacting with the Quasar server address space connect to it through ethernet connection and OPC-UA protocols. To simplify client development, Quasar can generate a library with an Application Programming Interface (API) named UaoForQuasar, primarily used in C++ clients. This C++ generated library manages low-level ethernet connections and the OPC-UA protocol, providing UA objects that offer methods for reading or writing into the server address space.

For certain OPC-UA clients, particularly DCS clients developed in Wincc Oa, unable to utilize the UaoForQuasar generated library, a specific API named fwQuasar is included in the standard framework, Java Card OpenPlatform (JCOP), of the CERN Wincc OA team. The Quasar-generated servers comprise three layers: the commercial OPC-UA toolkit, the common Quasar layer, and the device-specific layer.

Together, these systems form a comprehensive framework for controlling and monitoring the ATLAS experiment, ensuring its safe and efficient operation during data-taking runs and experimental campaigns at the LHC.

This system is very important and useful to calibrate the system but also during the data taking period to ensure that the system is in good condition. More detail about the LAr control and monitoring system will be given later in Section 2.2.4.

2 The ATLAS Liquid Argon Calorimeter

Summary

2.1 Calorimetry

2.1.1 Physics of calorimetry

2.1.1.1 Energy measurement

Particles traversing the calorimeter undergo energy loss as they ionize the material they pass through such as Liquid Argon (LAr). Within the active material of the calorimeter, electron-ion pairs are generated and then separated by an electric field, then drifted towards the electrodes. Upon reaching the electrodes, these pairs induce a signal whose magnitude corresponds to the number of pairs present. The energy (E) of the incoming particle is directly related to the number of particles (N) within the electromagnetic shower. As N experiences statistical fluctuations, and since the total ionization signal is proportional to N, the variability in the reconstructed energy (ΔE) can be articulated as follows [39]:

$$\frac{\Delta E}{E} \propto \frac{\Delta N}{N} \propto \frac{\sqrt{N}}{N} \propto \frac{1}{\sqrt{N}} \propto \frac{1}{\sqrt{E}} \tag{2.1}$$

Consequently, if one solely considers statistical reasoning, the energy resolution of the calorimeter enhances as particle energy increases. In a real calorimeter, it becomes necessary to accommodate instrumentation effects and noise:

$$\frac{\sigma}{E} = \frac{a}{\sqrt{E}} \bigoplus \frac{b}{E} \bigoplus c \tag{2.2}$$

The term a represents the sampling or stochastic component, typically falling within the range of 8 to 11% [5], directly tied to the sampling frequency. Calorimeters with uniform composition exhibit a minimal stochastic component as the entire shower is absorbed within the active material. However, sampling calorimeters tend to have a higher stochastic component due to energy deposition fluctuations across events. To mitigate this effect at lower energy and compensate for the stochastic energy loss in the upstream dead material, a presampler was introduced in the LAr calorimeters.

The term b encompasses combined noise factors, contingent upon the balance between electronics optimization and pile-up noise, which fluctuate in opposing directions with signal shaping time. Detectors reliant on charged particle collection tend to have higher noise levels due to the necessity of preamplifiers in the electronic readout chain. This noise component significantly influences performance at particle energies below 20 GeV.

The constant term c is very significant at high energies, being particularly sensitive to the inhomogeneities in the detector construction, calibration, and operation. It aggregates effects arising from material inconsistencies, mechanical structure imperfections, temperature gradients, radiation damage, among others.

The symbol $\oplus$ denotes the quadratic sum. Figure 2.1 [40] illustrates the energy resolution for the LAr calorimeter within ATLAS.

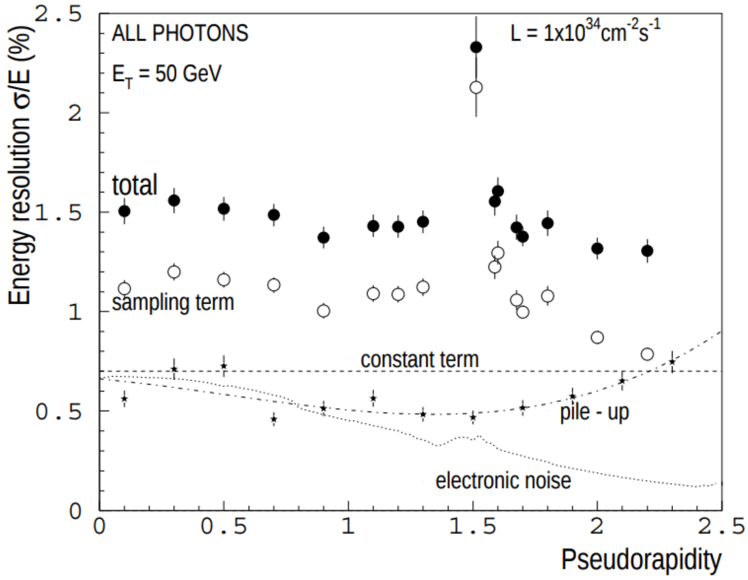


Figure 2.1: The energy resolution, expressed as a fraction of the total energy, is depicted as a function of the Pseudorapidity for 50 GeV E_T photons. [40]

In a sampling calorimeter such as the LAr calorimeter, only a portion of the total energy is deposited within the active section. The ratio of energy deposited in the active material to the total energy deposited is termed the Sampling Fraction:

$$S_f = \frac{E_{active}}{E_{active} + E_{passive}} \tag{2.3}$$

To calculate the total energy deposited in a sampling calorimeter, one must divide the measured energy by the sampling fraction.

2.1.1.2 Electromagnetic showers

When electrons or positrons produced in LHC p-p collisions traverse matter, they interact with the calorimeter primarily through the Bremsstrahlung effect, where emitted photons subsequently induce electron-positron pair production. This process initiates a cascade of particles with decreasing energy until their energy falls below the threshold for pair production. Any remaining energy dissipates through excitation and ionization. Figure 2.2 illustrates the impact of these various processes on the energy loss of photons and electrons/positrons.

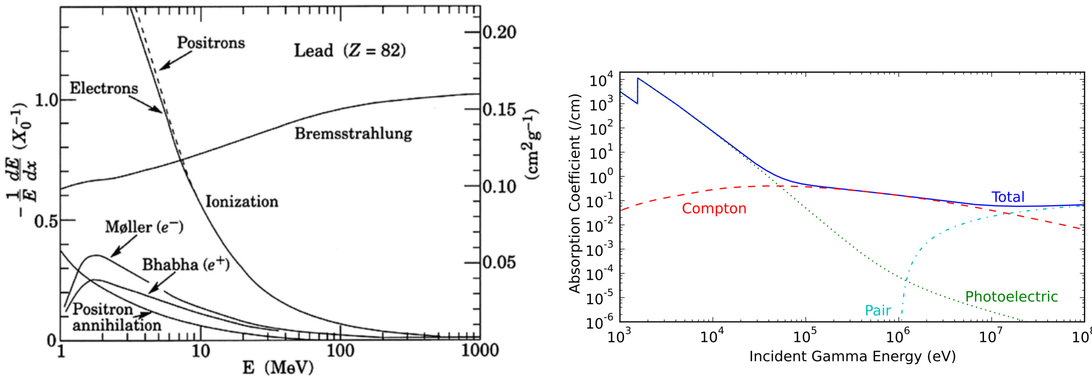


Figure 2.2: The left side displays the fractional energy loss of electrons per radiation length as a function of electron energy[41]. On the right side, the photon absorption coefficient in lead is depicted as a function of energy, illustrating the contributions of various scattering processes [42].

While there are a few tracks that traverse multiple layers of the calorimeter and deposit a portion of their energy in the active region, the majority of incident particles in an electromagnetic shower possess minimal energy and a short range, often smaller than the thickness of the layers [30]. Thus, the depiction of numerous electron tracks passing through several calorimeter layers could be misleading. Conversely, muons traverse many layers, losing a comparatively small fraction of their energy through ionization and generating only a few secondary particles.

The depth of the shower increases logarithmically with the particle's energy, rendering calorimeters relatively compact devices, even for energies in the TeV range at the LHC typicaly around 50cm for LAr. Additionally, electromagnetic showers exhibit transversal spread due to multiple scattering processes of photons and electrons/positrons, with the Moliere radius providing a reliable measure of the lateral shower spread. It can be written as

$$R_M = X_0 \frac{21 MeV}{E_c}. \tag{2.4}$$

Here,E_c represents the critical energy, approximately given by $E_c = 800 MeV/(Z + 1.2)$ [43], and X_0 denotes the radiation length.

2.1.1.3 Radiation length

The radiation length X_0 serves as a characteristic property of each material and offers a practical means to quantify the energy loss of high-energy electromagnetic particles while traversing the material.

For electrons, one radiation length is defined as the average distance over which the energy of a high-energy electron ($E > 1\ GeV$) is attenuated to $1/e$ of its initial value due to bremsstrahlung.

On the other hand, photons predominantly lose their energy via pair production. Therefore, for photons, the energy is reduced to $1/e$ after traveling a mean free path $x = 9/7X_0$. X_0 is typically measured in grams per square centimeter ($g \times cm^{-2}$). For materials composed of a single type of nucleus, X_0 can be approximated as follows:

$$X_0 = \frac{716.4 \times A}{Z(Z+1)ln(287/\sqrt{Z})} g \times cm^{-2} \tag{2.5}$$

where Z represents the atomic number and A is the mass number of the nucleus.

Ensuring the calorimeter is sufficiently thick in terms of radiation lengths is crucial for accurately measuring the energy of an electromagnetic shower. To achieve this, materials with high atomic numbers Z are preferred. For instance, the ATLAS electromagnetic calorimeter possesses a thickness of approximately 22 radiation lengths. To absorb 99% of the energy of a 300 GeV electron in the calorimeter, a thickness of approximately 25 X_0 is sufficient.

2.1.1.4 Performance of the LAr calorimeter

Due to its high granularity, the electromagnetic calorimeter facilitates the identification of electrons and photons while effectively rejecting jet background. The transverse shower shape in the front layer of the calorimeter can be leveraged to differentiate between photons and π^0 particles. Specifically, the strips in the front layer enable π^0 rejection by a factor greater than 3 while maintaining a 90% photon efficiency [44]. With an anticipated jet rejection exceeding 5000 at energies exceeding 20 GeV, the QCD background in the $H \to \gamma\gamma$ channel is expected to be effectively eliminated.

Moreover, these strips contribute to the angular measurement of photons in η with an accuracy of $50mrad/\sqrt{E}$, a crucial aspect for $H \to \tau\tau$ measurements.

However, coherent noise poses a challenge for jet reconstruction and missing E_T determination, as both processes necessitate aggregating a large number of channels.

For the entire ATLAS calorimeter system, the missing p_T resolution for the pseudoscalar supersymmetric Higgs boson $A \to \tau\tau$ is estimated to be approximately 7 GeV for each transverse component, allowing for a mass resolution of about 20 GeV at 150 GeV [19].

2.1.2 Structure of the LAr calorimeter

The Liquid Argon calorimeter is composed of three calorimeters, the Electromagnetic, the Hadronic, and the Forward.

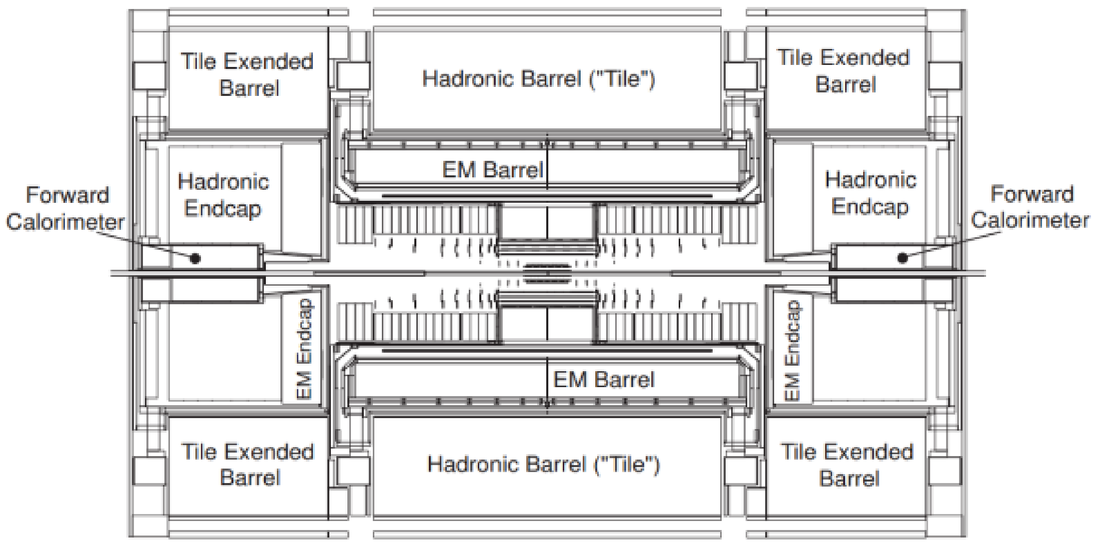


Figure 2.3: Schematic view of the electromagnetic and Hadronic calorimeters in ATLAS. [45]

- **Electromagnetic calorimeter**: The electromagnetic Barrel offers coverage up to $|\eta| = 1.475$, while the electromagnetic Endcaps span from $1.375 < |\eta| < 3.2$ on both sides of the detector. These components are constructed with accordion-shaped lead absorbers interleaved with liquid argon as the active material.

- **Hadronic Endcap calorimeter**: Utilizing liquid argon as the active material, the Hadronic Endcap employs flat copper plates as absorbers instead of accordion-shaped ones. Positioned in the same cryostat as the electromagnetic Endcap, it covers a pseudorapidity range of $1.5 < |\eta| < 3.2$.

- **Forward calorimeter**: Designed for both hadronic and electromagnetic calorimetry in the pseudo-rapidity region between 3.2 and 4.9, the Forward calorimeter is situated around the beam pipe within the inner bore of the Hadronic Endcap. It employs liquid argon technology, with thinner active gaps to handle higher counting rates. Copper and tungsten serve as absorber materials in this component.

These calorimeters are localized into two region the Barrel and the Endcap.

The Barrel component of the LAr stretches to a length of 6.4 meters along the beam axis and possesses a radial thickness of 53 centimeters. Within its structure, a network of 110,000 channels, it is arranged to capture and quantify the energy released during particle interactions. This segment serves as a foundational element in the comprehensive calorimetric measurements conducted by ATLAS.

The LAr Endcap comprises three distinct components: the forward calorimeter (FCal) with 3,524 channels, electromagnetic (EM) Endcaps with 63,312 channels, and Hadronic Endcaps (HEC) with 5,632 channels. The electromagnetic Endcaps, are characterized by a thickness of 63 centimeters and a radius of 2.077 meters. Meanwhile, the Hadronic Endcaps consist of two wheels, each with thicknesses of 0.8 and 1.0 meters, respectively, and share a common radius of 2.09 meters. This comprehensive arrangement ensures the LAr Endcap's efficacy in capturing a broad spectrum of particle interactions.

2.1.2.1 Barrel calorimeter

The electromagnetic barrel of the liquid argon calorimeter plays a fundamental role in the identification, measurement, and analysis of electrons, photons, jets, and missing transverse energy in high-energy collisions at the ATLAS experiment.

The central cryostat houses the Barrel electromagnetic calorimeter, the superconducting solenoid, and supports the tracking system. Integrating the magnet within the same cryostat was aimed at minimizing the material in front of the calorimeter. At $|\eta| = 0$, a traversing particle encounters approximately $2.3X_0$ of material before reaching the calorimeter. As η increases, the amount of material in front of the calorimeter also increases due to the elongation of the particle track and detector services.

The Barrel comprises two identical half-barrels separated by a small gap. Each half-barrel contains 1024 absorbers with readout electrodes positioned between them. Both the absorbers and electrodes are accordion-shaped, with folds oriented approximately perpendicular to the incoming particle tracks. The folding angles decrease with increasing radius, maintaining a constant gap of approximately $4.5mm$ between neighboring absorbers and ensuring uniform azimuthal coverage. Honeycomb spacers center the $300\mu m$ thick readout electrodes within this gap, defining two liquid Argon gaps of $2.1mm$ each.

Readout cells are delineated in η through etching of the readout boards and in ϕ by grouping four adjacent boards together. The readout and calibration signals are transmitted through the cold-to-warm feedthroughs, with 32 feedthroughs present at each end of the Barrel cryostat. The cryostat's geometry and the integration of the calorimeter are illustrated in Figure 2.4.

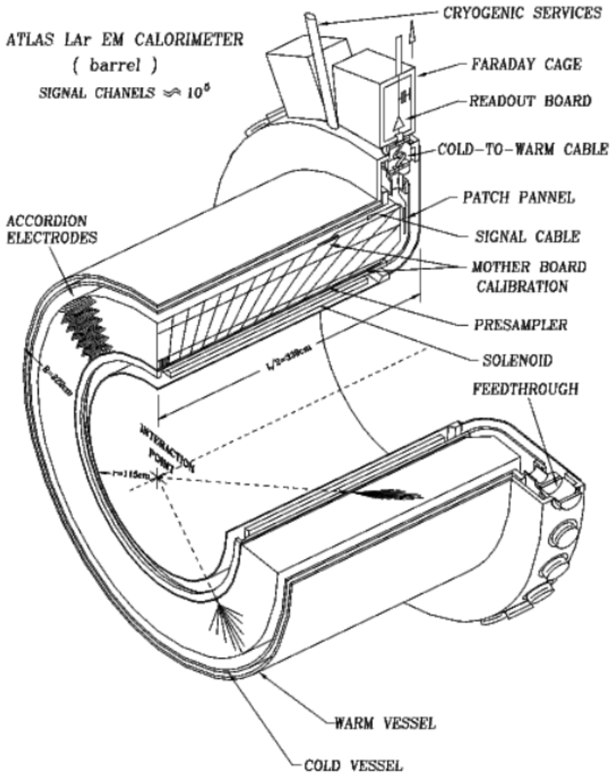


Figure 2.4: Schematic view of the Barrel cryostat. [45]

2.1.2.2 Endcap calorimeters

The electromagnetic (EM) endcaps of the LAr calorimeter are specialized components devoted to the measurement of the energy deposited by electrons and photons. Configured with a thickness of 0.632 meters and a radius of 2.077 meters, these endcaps exhibit a design to enhance the precision and granularity of energy measurements in the forward regions of the calorimeter. Distinguished by their role in capturing the energy of hadrons, the hadronic endcaps constitute an integral element of the LAr calorimeter. Comprising two wheels with respective thicknesses of 0.8 and 1.0 meters, these Endcaps share a common radius of 2.09 meters. This design facilitates the reliable measurement of the energy released during the interactions of hadronic particles within the detector, contributing to the comprehensive understanding of collision dynamics.

The forward calorimeter segment of the LAr calorimeter comprises three distinct modules, each characterized by a radius of 0.455 meters and a thickness of 0.450 meters. Positioned in the forward regions, these modules enhance the calorimeter's capacity to capture particle interactions occurring at extreme angles. The careful design and arrangement of these modules contribute to the efficacy of the LAr calorimeter in providing a complete and detailed picture of energy deposition in a variety of collision scenarios.

2.1.2.3 Temperature and purity monitoring

The signal generated by the calorimeter is primarily influenced by the temperature of the liquid Argon, which affects the liquid density with a sensitivity of approximately 0.5% per Kelvin. Additionally, the signal is directly proportional to the electron drift speed within the gaps, which is also temperature-dependent, with a sensitivity of approximately -2% per Kelvin. Thus, maintaining a uniform liquid temperature bath is crucial. The target is to keep the temperature difference (ΔT) between any two points of the calorimeter below 0.3 Kelvin, corresponding to an energy resolution term of less than 0.2%.

Since electronegative impurities may arise due to the outgassing of calorimeter materials under irradiation, the purity of the liquid Argon is monitored with test cells placed throughout each cryostat for measurements.

2.1.2.4 Calorimeter samplings

Expanding precision physics beyond $|\eta| = 2.5$ poses significant challenges. Hence, the Endcap region exhibits coarser granularity compared to the Barrel, with only two samplings in depth. The characteristics of the three longitudinal samplings are as follows:

- The **Pre-sampler Layer** Designed to correct for energy losses occurring before particles enter the main calorimeter, typically due to interactions with upstream materials. Consists of a thin layer of liquid argon placed ahead of the first active layer of the calorimeter.

- The **front layer** is optimized for π^0 rejection up to $E_T = 50\ GeV$ and for precise measurement of photon pointing. It terminates at approximately $X_0 \approx 6$, including approximately $1.7X_0$ of dead material ahead of the active part of the calorimeter.

- The **middle layer** is optimized to absorb the majority of electromagnetic shower energy, spanning from 6 to $22X_0$.

- The **back layer** extends beyond $22X_0$ (at $\eta \approx 0$, the second sampling is reduced to $22X_0$ to reserve a minimum of $2X_0$ for the third sampling) and primarily captures shower tails.

In the Endcaps, the width of a given η-bin decreases as η increases. Practical considerations limit the strip pitch to $5mm$. For $\eta > 1.8$, the strip size becomes 1/6 of the tower size, and for $\eta > 2.0$, it decreases further to 1/4 of the tower size.

The electromagnetic calorimeter comprises a total of 182,468 channels. In the central region, 60 elementary cells are summed up to form one trigger tower unit, with this number decreasing at high η. For $\eta > 2.5$, 8 elementary cells are combined to form one trigger unit.

In this region, the dimensions of the trigger towers are $\Delta\eta \times \Delta\phi = 0.2 \times 0.2$, while in the central part, they are 0.1×0.1. The granularity of the front, middle, and back layers, as well as the division into trigger towers, is illustrated in Figure 2.5.

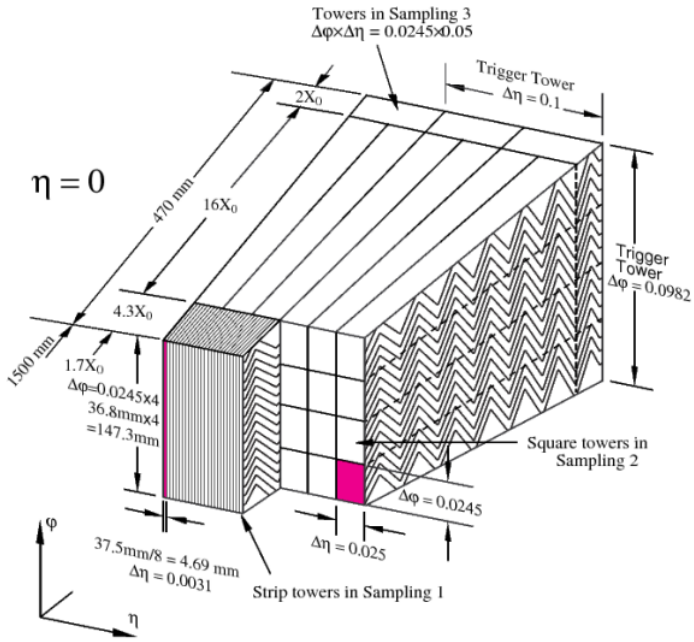


Figure 2.5: The structure of a LAr calorimeter Barrel module is shown. The layers (Pre-Sampler: PS, Front: 1, Middle: 2, Back: 3) can be seen as well as their granularity in ϕ and η [45].

2.1.3 Signal processing

2.1.3.1 Readout electrodes

In the calorimeter, signal electrodes alternate with absorber plates. The readout electrodes consist of three layers of copper separated by polyimide (Kapton), as shown in Figure 2.6. High voltage is applied to the outer layers of the electrode to create an electric field in the gaps. Currents induced capacitively by electrons drifting in the gaps are collected from the central layer. Consequently, the currents from both gaps surrounding the electrode are summed.

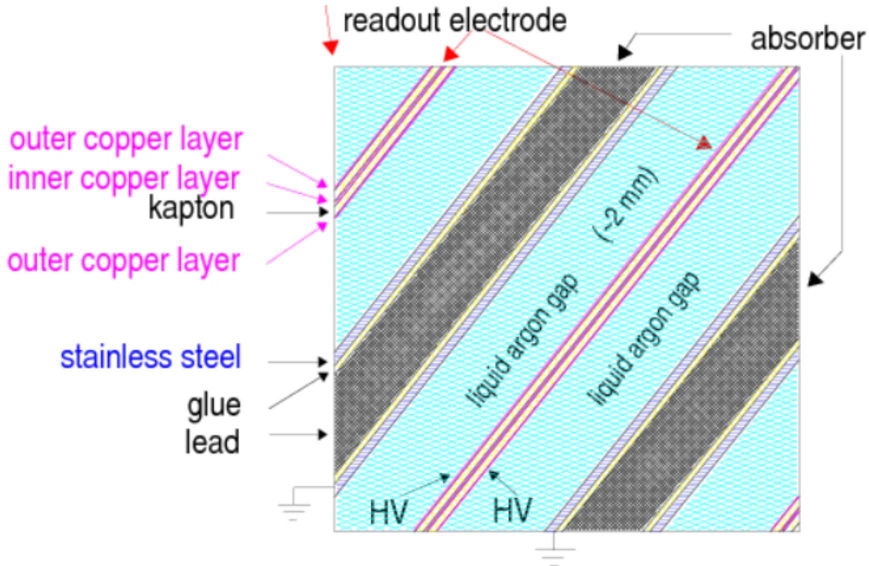


Figure 2.6: The readout electrodes [45]

Printed circuits at the electrode edges establish connections between neighboring electrodes in ϕ to achieve the desired granularity and connect to the output cables. These output cables run toward the feedthroughs over the printed circuits, parallel to the beam axis.

Figure 2.7 illustrates the signal layer of the Barrel electrodes ($0 \leq \eta \leq 1.45$). Each high-voltage line supplies a zone covering $\Delta\eta = 0.2$ and $\Delta\phi = 0.1$. It is routed over the electrode through resistive bridges along a bus of $6mm$. Two resistors in parallel, each with a resistance of $1M\Omega$, connect the bus to each cell in the middle and back layer.

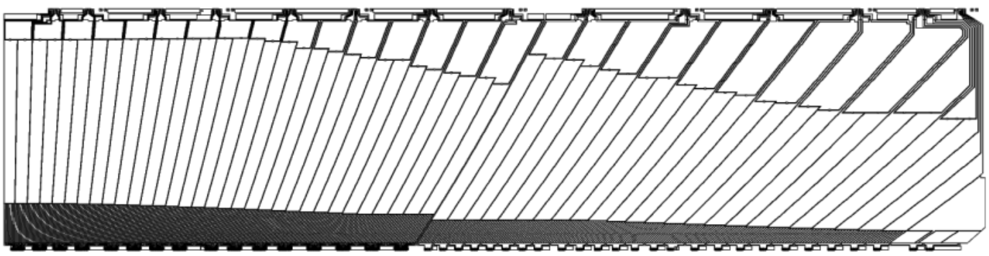


Figure 2.7: Signal layer for Barrel electrodes [45].

2.1.4 Readout electronics

2.1.4.1 Front end readout electronics

The 58 Front End crates are directly mounted on the LAr cryostats, positioned both in the gap between the Barrel and Endcap calorimeters and on the outer face of the Endcap cryostats. High voltage of approximately 2 kV, necessary to power the electrodes, is brought from the outside using warm feedthroughs located on top of each cryostat. On-detector electronics must be radiation-hard and has undergone qualification for radiation tolerance for up to 10 years of operation at the LHC, equivalent to an integrated luminosity of 700 to 1000 fb^{-1}.

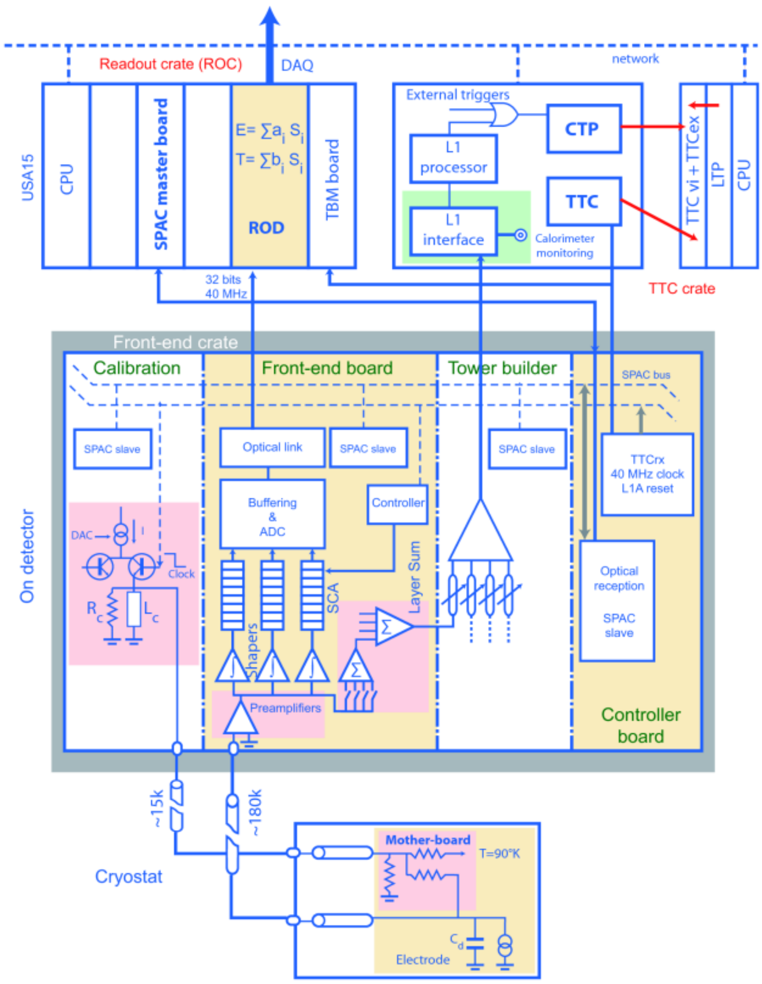


Figure 2.8: Schematic block diagram of the original construction LAr readout electronics [45].

Each FE crate, as illustrated in Figure 2.8, contains:

- **Front End Boards (FEBs)**: These boards are responsible for reading out and digitizing the signals from the LAr calorimeter. Each FEB is a 10-layer printed circuit board (PCB) that processes signals from 128 channels in a specific layer of the calorimeter. The signals undergo analog processing, starting with amplification followed by splitting and further amplification by shaper chips, resulting in three overlapping linear gain scales. Gain selector chips determine the gain for each channel based on the peak sampled value of each signal. Fast bipolar shaping with a time constant τ = RC = 13ns is performed, and the shaped signals are sampled at the LHC bunch crossing frequency of 40 MHz. Switched capacitor array analog pipeline chips hold the signals in a buffer, and upon L1-Trigger acceptance, typically five samples per channel are read out and digitized using a 12-bit analog-to-digital converter (ADC). The digitized data are formatted, multiplexed, serialized, and transmitted optically via a 1.6 Gbps fiber-optic link off the detector to the back end electronics.

- **Layer Sum Boards (LSB)**: These boards sum a portion of the analog signals first in the shapers and then on the LSBs before forwarding them to the TBB via the baseplane.

- **Tower Builder Boards (TBB)**: Analog signal sums from various FEBs are sent over the backplane in the FE crate to the TBB, which aggregates the signals to form trigger towers with a size of $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$. The signals are then routed to the L1 calorimeter trigger system.

- **Calibration Boards**: These boards deliver a pulse to the LAr cells, generating a signal shape similar to the triangular-shaped physics signal but with an exponential decay due to the inductively injected current. These boards are used for the calibration of the detector during the interfill period.

- **Controller Boards**: Responsible for receiving and distributing the 40 MHz LHC clock and other configuration and control signals.

- **Baseplane**: In each end of the Barrel cryostat, there are 32 calorimeter signal feedthroughs positioned around the cylindrical periphery at nearly equal angles. The two end-cap cryostats each have 25 signal feedthroughs distributed around the far end (opposite the collision point) of their periphery. Each feedthrough, consisting of cold and warm flanges connected via vacuum cables, comprises four pin carriers. These carriers contain either seven or eight connectors, each with 64 signal pins. A pedestal spans two adjacent feedthroughs, with a Front End Crate (FEC) mounted on each pedestal. Each FEC is divided into two halves, with a baseplane installed in each half for most of the crates. A cable is used to carry 64 signals from each connector in a pin carrier to a connector on the backside of the baseplane. The pins in this connector extend through to the front side of the baseplane. Each Front End Board (FEB) has two 64-pin signal connectors, mounted in an FEC, which plug into the baseplane. Between the two signal connectors on each FEB lies a third 64-pin connector, returning analog trigger signals to the baseplane, where they are routed to trigger-handling boards, also plugged into the baseplane.

2.1.4.2 Back end readout electronics

The back end electronics are tasked with filtering, formatting, and monitoring the digitized calorimeter signals, and ultimately reconstructing the transverse energy (E_T). Digitized samples are transmitted via a 1.6 Gbps optical link to the back end. The VME-based Readout Driver (ROD) crate contains:

- **Readout Driver Boards (RODs)**: These boards recover the output of the FEBs at the L1-Trigger rate and compute parameters such as energy, time phase, and signal quality. These parameters are then transmitted via optical fibers to the data acquisition (DAQ) system. The memory on RODs is partitioned into sections for writing incoming data and data read by the digital signal processor (DSP). Each DSP can execute 5.7×10^9 instructions per second, ensuring calculations are completed within 13 μs at an L1-Trigger rate of up to 100kHz. An optimal filtering algorithm [6] is employed to calculate the energy deposited in the calorimeter from the digitized samples. Additionally, above a certain energy threshold, the time of energy deposition and the quality of the pulse are estimated. The quality factor assesses whether a pulse matches the expected shape or may have been inaccurately measured.

- **CPU Board**: This VME processor controls the ROD crate. It allows configuration and monitoring.

- **SPAC Master Board**: A module utilized to configure and load parameters into the boards within the FE crate or to read back registers. Configuration and monitoring are performed using the Serial Protocol for ATLAS calorimeters (SPAC) [46].

- **Trigger Busy Module (TBM)**: The TBM receives trigger, timing, and TTC (Timing, Trigger, and Control) signals, including the LHC clock and other synchronous commands.

2.2 Phase-I Upgrade

2.2.1 General and physics motivation

The Phase-I upgrade of the Liquid Argon (LAr) calorimeter trigger electronics at CERN represents a significant advancement in the ATLAS experiment's capabilities to detect and measure particles produced in high-energy collisions at the Large Hadron Collider (LHC). This upgrade focuses on enhancing the performance of the LAr calorimeter system to meet the increase of luminosity of the LHC and the evolving needs of particle physics research.

The primary objectives of the Phase-I upgrade include improving the ATLAS detector's electronics, maintaining its efficiency in identifying particles, and enhancing its ability to withstand the higher collision rates expected during future LHC operation phases. These enhancements are crucial for maintaining the ATLAS experiment's competitiveness in exploring new physics phenomena and achieving greater sensitivity to rare processes.

One important aspect of the Phase-I upgrade is the partial replacement and addition of electronic components within the LAr calorimeter system as illustrated in Figure 2.9. This involves implementing state-of-the-art electronics and readout systems to enhance data collection, processing, and transmission trigger capabilities.

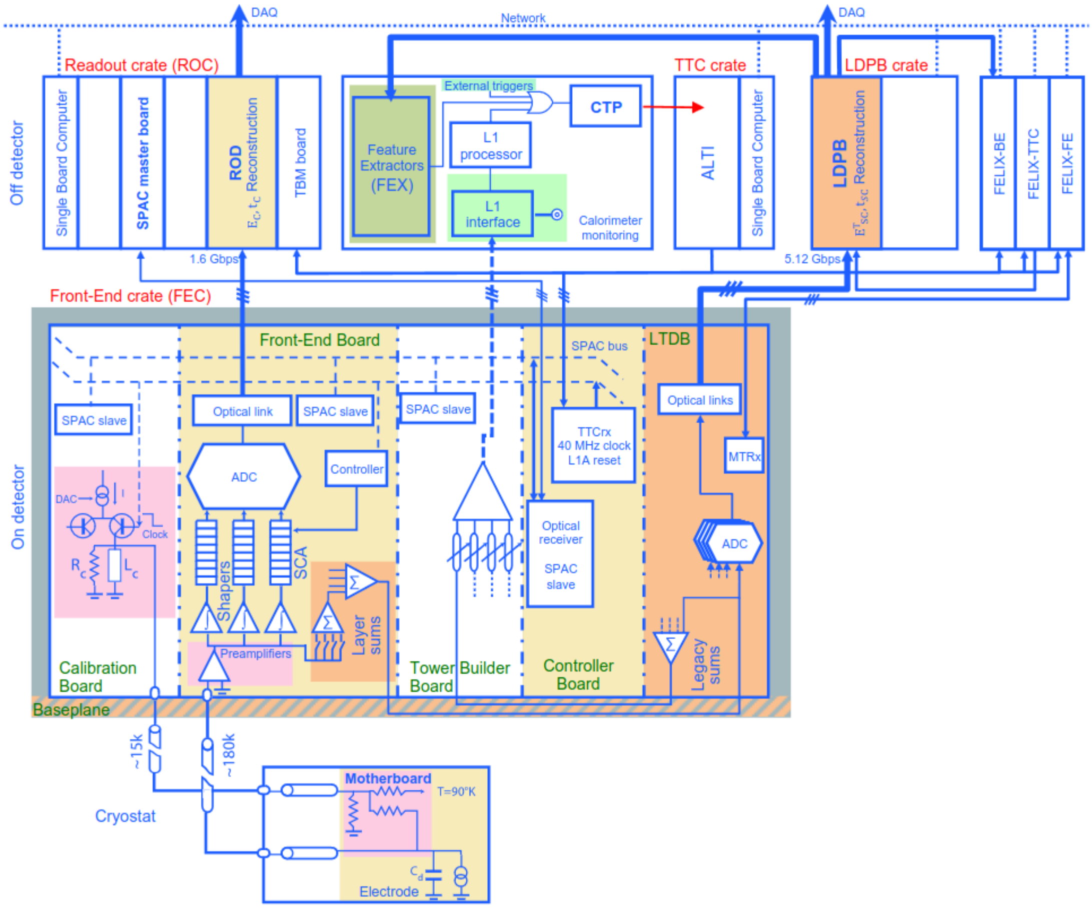


Figure 2.9: Schematic block diagram of the current LAr readout electronics with the Phase-I upgrade electronics highlighted in orange. [1]

The Phase-I upgrade involves the installation of new trigger systems tailored to efficiently select collision events of interest for further analysis. To do so this new trigger systems will have a better granularity increase by a factor of ten compared to the previous one. This better granularity will come from the segmentation of the

180k cells into 34k Super Cells (SCs). This new segmentation will be composed of 4 layers. First layer is the Presampler with 1 information, second layer is the Front layer with 4 information, third layer is the Middle layer with 4 information, and the fourth layer is the Back layer with 1 information. These trigger systems play a crucial role in managing the enormous amount of data produced by the ATLAS experiment, ensuring that only relevant collision events are recorded for subsequent analysis while discarding redundant or uninteresting data.

Overall, the Phase-I upgrade of the LAr calorimeter represents a significant advancement in the ATLAS experiment's capabilities, enabling researchers to explore new frontiers in particle physics and contribute to our understanding of the fundamental laws governing the universe.

2.2.2 New front end electronics

As seen in Section 2.2.1 for the Phase-I upgrade new electronics were needed. The new baseplanes are necessary to accommodate finer trigger segmentation, make room for the LAr Trigger Digitizer Boards (LTDB), while maintaining the legacy Level-1 trigger system. The new mezzanine LSBs, mounted on the existing FEBs, deliver more analog signals than before onto the baseplanes, which are now routed to both the LTDBs and the existing TBBs or TDBs, necessitating additional signal layers on the baseplane PCBs. Due to the LTDB baseplane connectors being wider than those for other boards, there is no space next to an LTDB for the Radio Frequency (RF) shields, which protect the small signal inputs to the FEBs from extraneous noise. More detaill about all these new electronics are given below.

2.2.2.1 Layer Sum Board

The newly integrated LSBs generate signals tailored for the finer granularity Super Cells in the front and middle layers, while preserving the signals necessary for the conventional trigger path. Six different flavour of LSBs have been manufactured:

- **S2x8**: analog summation of two input channels from the Linear Mixer. 896 boards of this type are required for the ElectroMagnetic Barrel (EMB) and 192 for the ElectroMagnetic EndCap (EMEC).

- **S2x8D**: a splitter is added to the S2x8 flavour to propagate the output signal to both the new LTDB and the legacy TBB. 128 boards of this type are necessary for the EMB and 160 for the EMEC.

- **S1x16LN**: no summation function on this board. Serves only as a line driver. 448 boards of this type are needed for the EMB and 544 for the EMEC.

- **S1x12+S6x2**: used for the front section of the EMEC within the range $1.8 < |\eta| < 2.0$. Individual signals are sent to the LTDB and sums of six inputs to the TBB. 128 boards of this type are required for the EMEC.

- **S2x6D+S1x4**: used for the end of the EMB within the range $|\eta| > 1.4$, handle 4 signals from the middle layer to sum and send to the LTDB and 12 signals from the back layer to sum and transmitted to the LTDB and TBB. 128 boards of this type are needed for the EMB.
- **FCal**: sum over a wider η range. To account for varying conversion factors from energy to transverse energy, inputs to FCal LSBs are weighted before summing. This results in a diverse set of LSBs within each FCal module, distinguished by their weighting resistor values. All 56 FCal LSBs have been replaced by the new design.

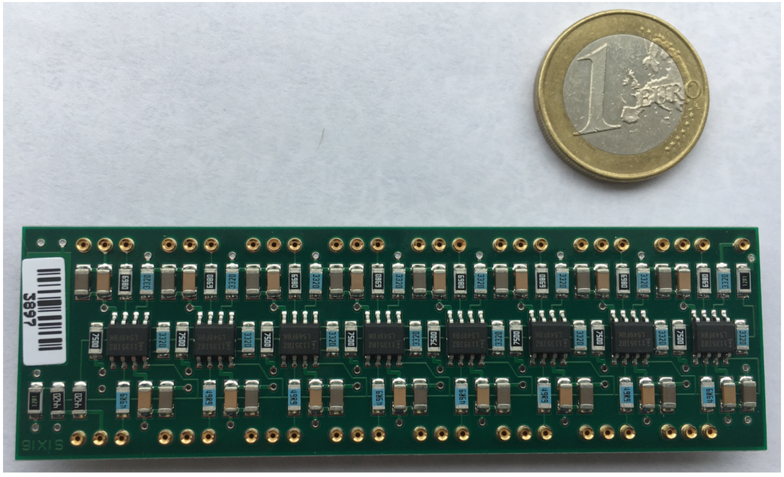


Figure 2.10: Photo of an S1x16LN LSB. Only one side is shown. Half of the components are on the other side. A one-euro coin is shown for scale. [47]

2.2.2.2 Baseplane

A new baseplane is needed to handle the new cards in the FEC, the finer trigger segmentation, and to maintain the existing Level-1 trigger system. The new LSBs are providing more analog signals onto the baseplanes, which are now routed to both the LTDBs and existing TBBs. Five flavour of baseplane have been manufactured:

- **EMB baseplane**: The new EMB baseplane has the same number of slots as the original baseplane (19). Some FEBs have been shifted by one slot to accommodate the LTDB in the middle slot of the baseplane next to the TBB.
- **EMEC standard baseplane**: The EMEC standard crate has baseplanes similar to the EMB but with one fewer FEB, leaving a slot for an additional monitor board.
- **EMEC special baseplane**: The EMEC special baseplane has two LTDBs and extends well beyond the center of the crate.

- **HEC baseplane**: The HEC baseplane on the other side of the crate consequently has room for only 13 slots instead of the normal 19 slots found on the EMB baseplanes and the EMEC standard baseplanes.
- **FCal baseplane**: The new FCal baseplanes have two LTDBs. Integrated into each new FCal baseplane are traces carrying pulses from the calibration board through attenuating injection resistors to those pins on the baseplane connectors which carry FEB signals.

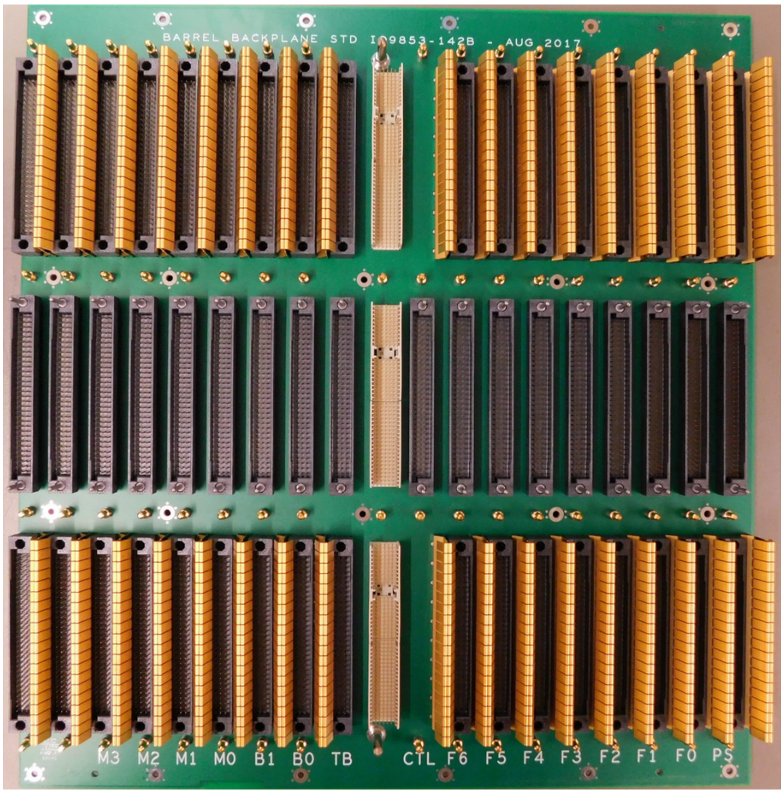


Figure 2.11: Photograph of an EMB Baseplane. The slot with three wider baseplane connectors (white connectors in the middle) is for the LTDB. Just to the left of the LTDB is the slot for the TBB and to the right is the Controller board slot. The calibration board slot is on the far left and next to it is the monitor board slot. The gold-colored RF shields surrounding connectors in the top and bottom rows identify the FEB slots [47]

2.2.2.3 LAr Trigger Digitizer Board

The LTDB, see Figure 2.12, is the central electronics board crucial for the Phase-I upgrade. It is responsible for the digitizing the Super Cells signals as well as generating the legacy layer sum signals (previously formed in the LSBs). Each LTDB is processing up to 320 Super Cell signals.

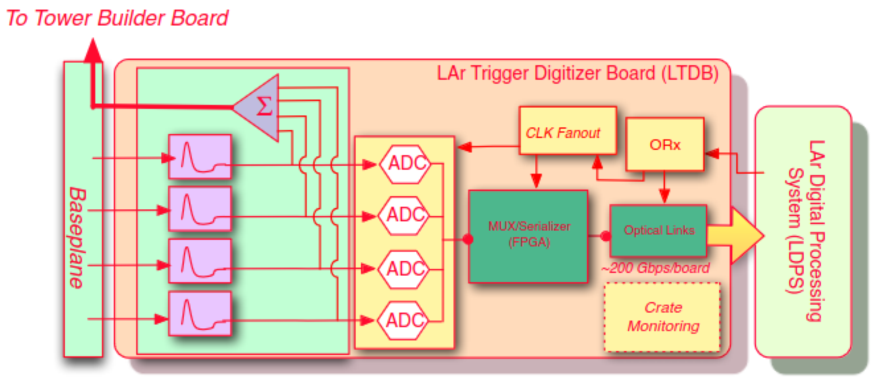


Figure 2.12: Block diagram of the LAr Trigger Digitizer Board (LTDB) on the detector.

Figure 2.13 illustrates the LTDB. The board is composed of three distinct sections: the analog section, the digital section and the Power Distribution Board (PDB) section.

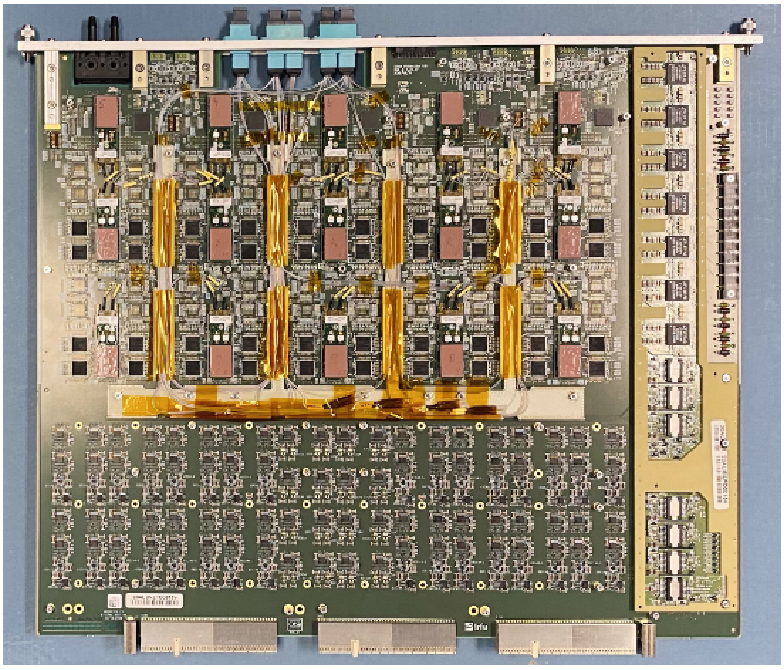


Figure 2.13: Picture of an LTDB. The PDB is on the right. On the bottom is the analog part. On the middle top is the digital section [1].

i. Analog part The analog section corresponds to the bottom of the board (figure 2.13), where three white connectors serve for the plugging to the crate baseplane, receiving analog signals from the LSBs. To maintain compatibility with legacy trigger tower signals, the analog signals received by the LTDB are summed in the analog section before being transmitted via the rear connectors to the tower building boards

(TBBs).
The LTDBs have 7 different flavours distinguished either by the configuration of its subsections or by the treatment of analog signals within those subsections. There is one LTDB per baseplane in each EMB, HEC, and EMEC Standard half Crate. However, in the EMEC Special and FCal crate, two special LTDBs are required labeled "0" and "1". The number of channels to be processed in each type of LTDB, along with the required number of units, is detailed in Table 2.1. A total of 124 LTDB boards were installed in the ATLAS detector. The EMB comprises 64 LTDBs, covering the entire Barrel region. Additionally, the EMEC includes 32 LTDBs, addressing the $1.6 < |\eta| < 2.4$ region. Two specialized configurations, EMECSpec0 and EMECSpec1, each requiring 8 LTDBs, cater to the $1.4 < -|\eta| < 1.6$ and $2.4 < |\eta| < 3.2$ regions respectively in the electromagnetic Endcap. Furthermore, the Hadronic Endcap (HEC) necessitates 8 LTDBs for coverage. Lastly, the Forward calorimeter (FCAL) is comprised of FCAL0 and FCAL1, with 2 LTDBs each, catering to the first and subsequent layers of the forward calorimeter, respectively.

LTDB Type	Channels	LTDB per region
EMB	290	64
EMEC Std	312	32
EMEC Spc 0	240	8
EMEC Spc 1	160	8
HEC	192	8
FCAL 0	192	2
FCAL 1	192	2
Total	34048	124

Table 2.1: Number of channels to be treated in each type of LTDB and the number of boards installed. The EMB, EMEC Standard, and HEC crates require only one LTDB per baseplane but in the EMEC Special and FCal crates two LTDBs per baseplane are required. Suffixes "0" and "1" are used to distinguish the LTDB modules in these two crates.

ii. Digital part The digital section consists of five identical segments, each comprising one control path and four data paths. These data paths are managed by the control paths of their corresponding segment. Situated between the front plate and the analog section, the LTDB's digital components include MTP connectors (in blue in Figure 2.13), each containing 12 optical fibers. The left connector facilitates control paths, while the other four connectors are dedicated to data paths (figure 2.13).

As shown in Figure 2.14, the LTDB is composed of two paths: the slow control path and the data path.

- The input of the **data path** is the analog circuit of the detector with the analog Super Cells.

- The ADCs will digitize the signals from the detector.
- the LOCx2 component receives the serialized ADC data, and encodes the digital signal.
- The MTx is a unidirectional optical transmitter used to send the data stream to the LAr Digital Processing Blade (LDPB) for the reconstruction of the energies.

The slow control path is used for timing the signals with the TTC, as well as the configuration and monitoring of the different ASICs (Application-Specific Integrated Circuits). All this information transits inside the GigaBit Transceiver (GBT) frame of the GBT protocol.

- The MTRx optical transmitter/receiver transmits/receives information between the LTDB and the FELIX LTDB, including the TTC frame clock to the GBTx.
- The GBTx decode/encode this frame. For the TTC data, it will propagate the clock to the LOCx2s and ADCs. The GBTx transmit also a Bunch Crossing Reset to the LOCx2.
- The GBT-SCA will receive information from the OPC-UA to configure the LTDB. The GBT-SCA will propagate the commands to all the other components via the I2C protocol to the ADCs, LOCx2s, MTx, and MTRx.
- The mezzanine board Power Distribution Board (PDB) is composed of many regulators. It is used to provide all the power and the voltages that the LTDB needs to ensure correct operation.

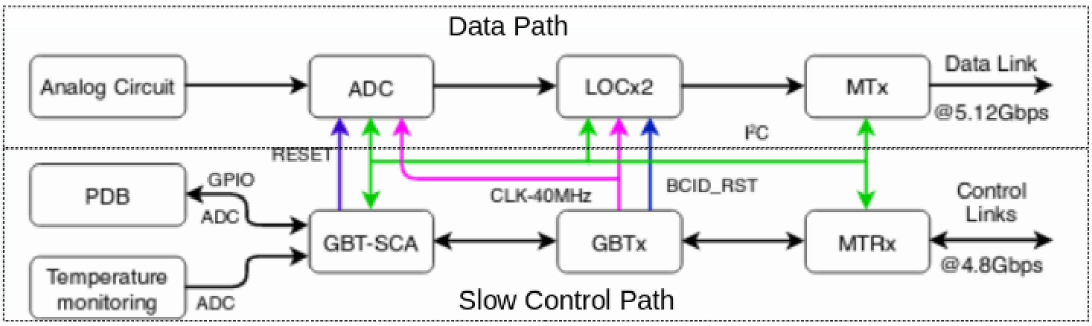


Figure 2.14: Block diagram of the LAr Trigger Digitizer Board (LTDB) [1].

ii.i Slow control path The slow control system, depicted in Figure 2.15, facilitates communication with the Front End Link eXchange (FELIX) (described in Section 2.2.3.1) via 5 pairs of optical fibers linked to optical transceivers (MTRx) [48] on the board. Each fiber pair connects a slow control path to a pair of FELIX links, organized within MTP 12 connectors. To withstand radiation, GBTx components and GBT protocol [49] are utilized in these links, with five GBTx components decoding GBT frames on each board. Each GBTx is linked to two SCAs to provide redundancy in case of issues with one control fiber or MTRx component. The redundancy design features the auxiliary port of the GBT-SCA, enabling recovery of any stuck GBTx during data taking, given at least one operational GBTx. If all GBTx, except GBTx_5, fail, recovery occurs sequentially by resetting adjacent GBTx and GBT-SCA pairs, ensuring continuous operation.

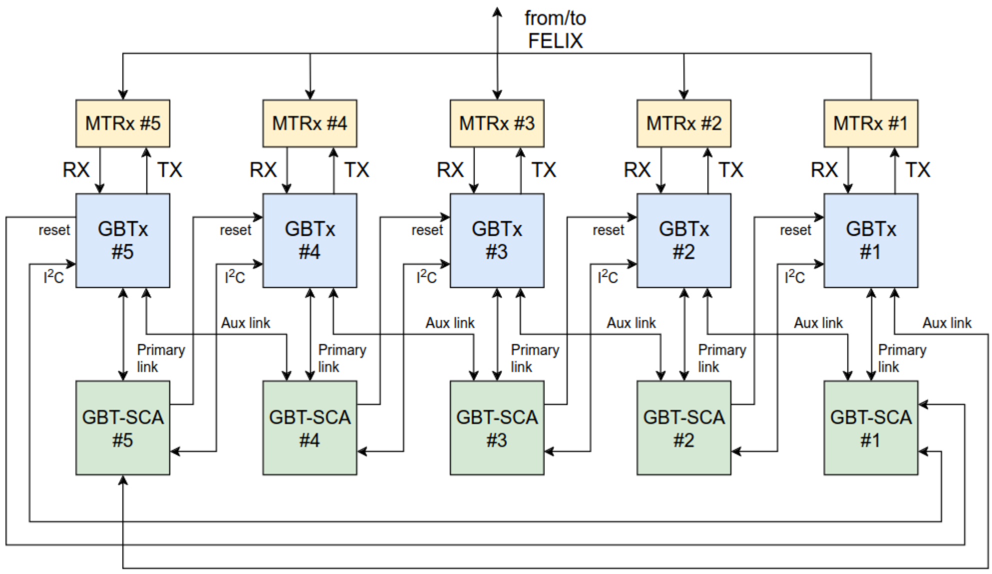


Figure 2.15: Schematic illustrating the slow control components of the LTDB and redundancy design. [47]

The LTDB integrates 5 Slow Control Adapter components (SCA or GBT-SCA) [50], each managing four data paths. The SCAs serve as the primary slow control access points for the LTDB. It offers various interfaces for the board's diverse components, including general-purpose input/output channels (GPIO protocol) for binary signals, I2C buses for register reading/writing, and analog-to-digital converters (ADC) for analog input.

Configuring two critical components—MTRx and GBTx—is essential for SCA access. GBTx configuration is fixed and loaded during reset, with the SCA needing accessibility for operation. To ensure the GBTx is not in the reset path, the AUX SCA controls the reset. MTRx configuration occurs via an I2C connection with the corresponding SCA, with the direct link involving MTRx in its own configuration path. To mitigate this, the auxiliary link is utilized by default, enabling MTRx configuration without obstruction.

Figure 2.15 illustrates a single GBTx I2C bus serving all SCAs and GBTxs, with GBTxs operating as slaves and SCAs as masters. Notably, the SCA does not support multi-master mode, allowing only one SCA to communicate with the bus at a time. By default, only the first SCA acts as a master to prevent conflicts, with the I2C master interface of other SCAs disabled.

ii.ii Data path Figure 2.16 illustrates the data-path schematic of the LTDB. Each data path consists of 16 ADCs chips, 4 LOCx2s, and 4 MTxs mezzanines. One group of data path processes up to 64 Super Cells. One ADC chip digitizes signals from 4 Super Cells, transmitting serial data to the LOCx2 encoding 16 ADCs channels data with 2 LOCics frames. Timing data is added to each frame by the LOCx2 to correlate with collision events. These encoded frames are then transmitted via an dual-channel optical transceiver called MTx. Five data paths make up an LTDB that digitizes up to 320 Super Cells.

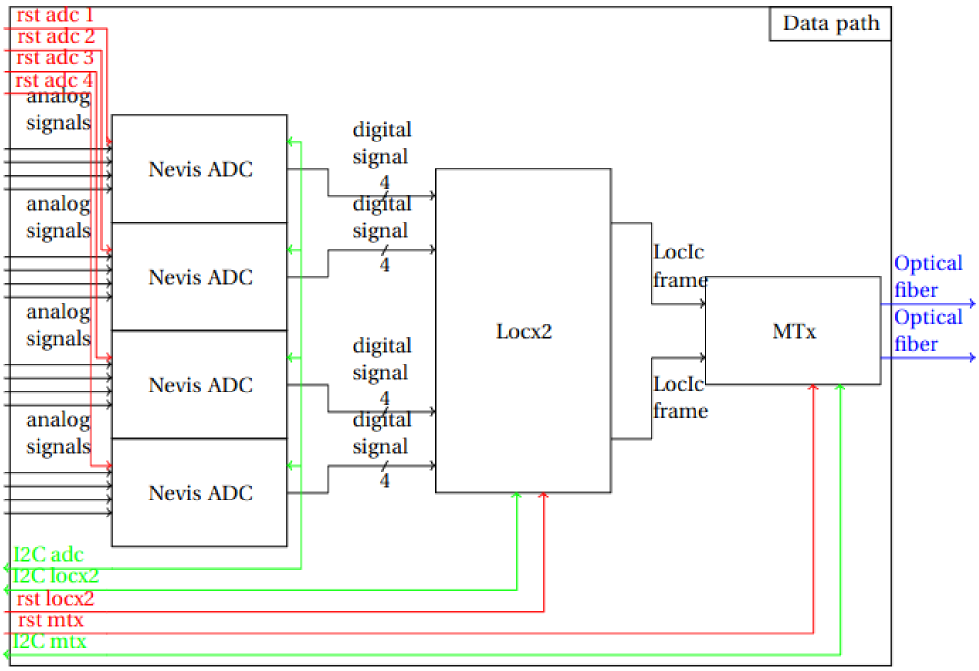


Figure 2.16: Block diagram of the LTDB Data path. Four ADC chips digitize the sixteen analog inputs. The LOCx2 component encodes these data into a frame that is sent to optical fibers by the MTx component.

The Nevis ADC chip[51] comprises four identical channels seen in Figure 2.17, each incorporating four stages of 1.5-bit Multiplying Digital-to-Analog Converter (MDAC) followed by 8-bit Successive Approximation Register (SAR) analog-to-digital converters. The Digital Data Processing Unit (DDPU) aggregates output from these stages to produce a 12-bit output. However, due to capacitor mismatch within the MDAC stages at the precision limit of the CMOS process, the reconstructed output may contain jumps, necessitating digital corrections applied by the DDPU using calibration-derived coefficients. Configuration of the ADC chip occurs via I2C interface, with PLL providing the required clocks.

The ADC serializer comprises a parallel register, filled at 40 MHz with 12-bit words by the DDPU. These words, consisting of the 12-bit DDPU output and four bits set to 0, are transferred to a shift register and read at 640 MHz for serialization. Three signals are then transmitted to the LOCx2: serial_data (DATA), clk (SCK), and frame (FCK).

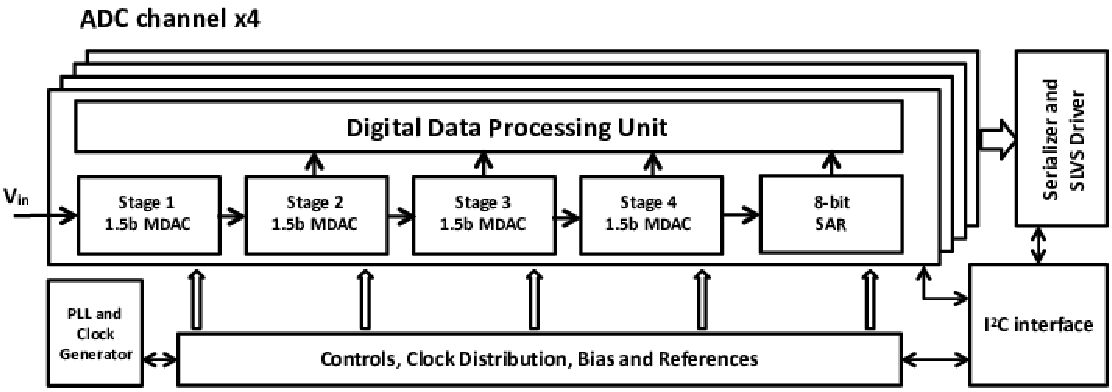


Figure 2.17: Nevis ADC block diagram [47]

The LOCic block as shown in Figure 2.18 is encoding the data coming from 2 ADCs chips. It consists of synchronization FIFOs, PRBS (Pseudo Random Binary Sequence) generators, CRC (Cyclic Redundant Checking) generators, scramblers and a frame builder. The PRBS encodes the Bunch-Crossing Identification (BCID), while the CRC is a checksum for error detection during transmission.

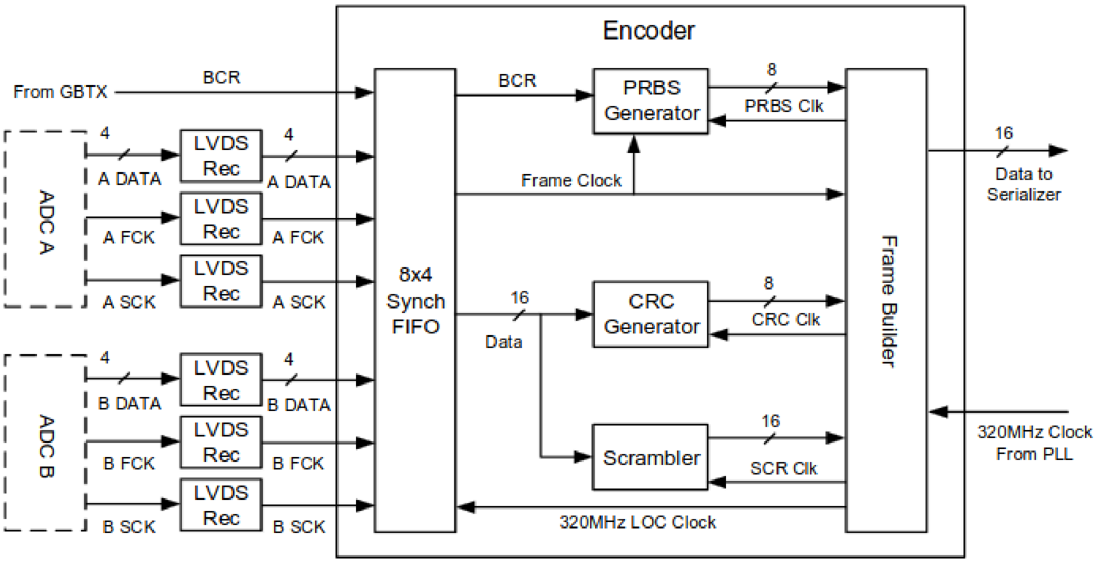


Figure 2.18: The block diagram of the LOCic encoder [52]

The LOCx2 [52] comprises two LOCic blocks, each encoding a frame from two ADCs chips, along with a PLL (Phase-locked loop) for providing clock to the serializer, an I2C slave for slow control, and a driver for frame transmission to the MTx. Each LOCic frame from the LOCx2 is transmitted to one channel of the MTx. Fibers from different MTx are combined into MTP-12 optical fiber links and sent to the LDPB.

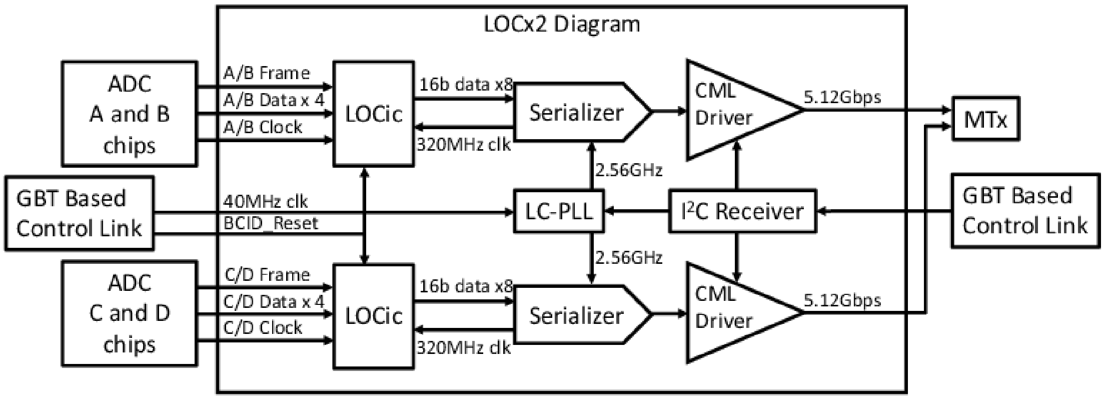


Figure 2.19: LOCx2 block diagram with connections to four ADCs (A, B, C, and D), Control Link and MTx. [52]

2.2.3 New back end electronics

2.2.3.1 Front End Link eXchange

The FELIX [53] is a generic PCI format board made to fulfill the need of several particle physics experiments as illustrated in Figure 2.20.

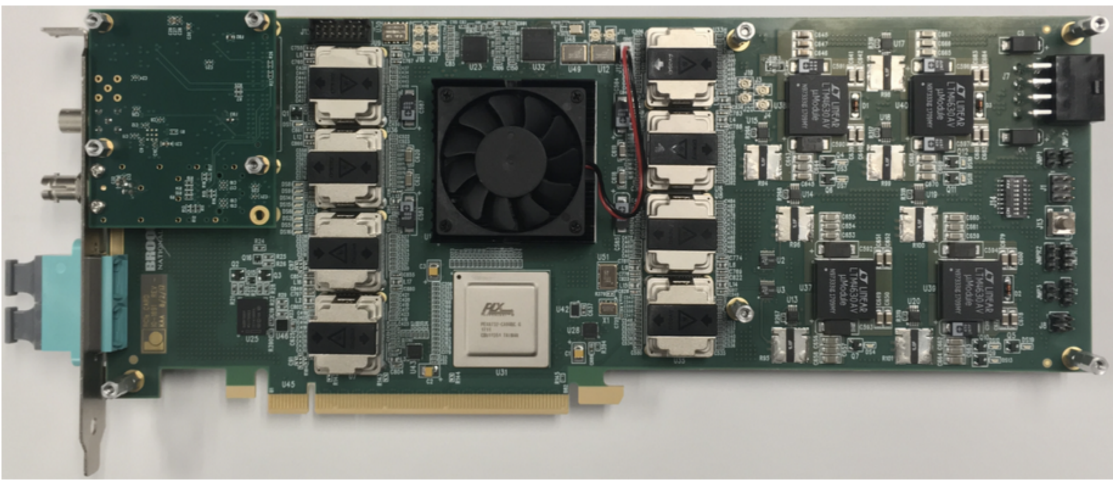


Figure 2.20: The FLX-712 PCIe card used at present for the LAr Phase-I. [54]

The FELIX system encompasses several specialized components tailored to different aspects of data acquisition and transfer. These components include FELIX modules dedicated to the front end, back end, and timing/trigger clock (see Figure 2.21):

- The **FELIX-FE** are receiving the TTC clock and responsible for interfacing directly with the front-end electronics.
- The **FELIX-BE** are typically integrated into the overall data acquisition infrastructure of the experiment. Upon receiving the data, they perform initial data processing tasks such as buffering, formatting, and error checking.
- The **FELIX-TTC** are deployed to ensure accurate timing and synchronization signals are distributed throughout the detector system. These modules generate and distribute clock signals, trigger signals, and other timing signals necessary for coordinating data acquisition and event triggering across the detector subsystems.

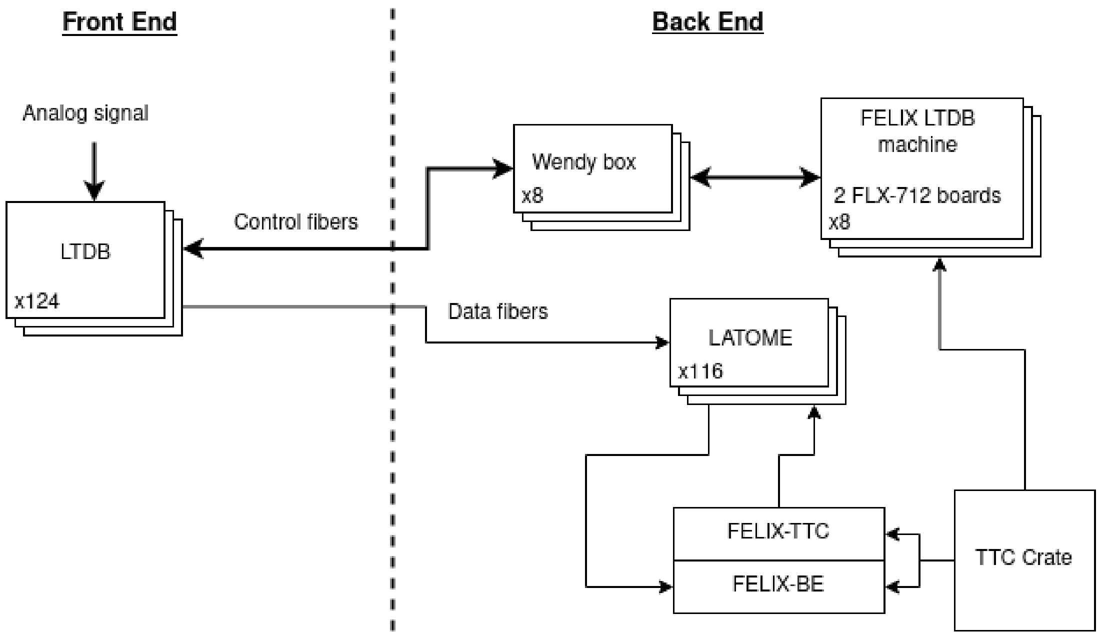


Figure 2.21: FELIX connection production system architecture diagram of the Phase-I upgrade.

The FELIX operates using state-of-the-art communication protocols and hardware to ensure high-speed and reliable data transmission. It employs advanced techniques to handle the large volume of data generated, optimizing throughput and minimizing latency to ensure efficient data processing.

In the context of this document, more details are given on the FELIX LTDB of the LAr calorimeter. The FELIX LTDB serves as a router, connecting various systems such as the DCS and TTC systems to the LTDB, but also as an interface between the different protocols: readout, FE and TDAQ. It features a Xilinx Kintex UltraScale FPGA and incorporates 8 Minipods transceivers, with 4 functioning as 12 transmitting fibers (Tx) and the remaining 4 as 12 receiving fibers (Rx), totalling 48 bidirectional links.

The FELIX LTDB board is equipped with two MTP 48 connectors to interface with the LTDBs through the Wendy boxes. The Wendy box is a patch box to map the fibers coming from the LTDB with a connector of 12 channels to the FLX-712 board with a connector of 48 channels. Despite offering 48 bidirectional links, only 40 are utilized to communicate with up to 8 LTDBs, as each LTDB employs 5 bi-directional links. The communication between the FELIX and the LTDBs is facilitated using the GBT protocol, which is encoded within the FPGA firmware of the FELIX board.

The GBT protocol The GigaBit Transceiver protocol (GBT) [55] is a communication standard developed at CERN to enhance bandwidth between experiment caverns and counting rooms for the LHC's high luminosity upgrade. It utilizes point-to-point duplex links via optical fibers, enabling simultaneous transmission of physics, trigger, and slow-control data.

The GBT frame shown in Figure 2.22, 120 bits in length and transmitted at 40 MHz, offers a total throughput of 4.8 Gb/s. It comprises a 4-bit header, 32 bits for forward error correction, and an 84-bit User field. The forward error correction is crucial for radiation tolerance. Within the User field, 4 bits are allocated for slow control, 16 for Timing and Trigger (TTC), and 64 for data. The User field's flexibility allows different experiment needs, with 2 bits designated as Internal Control (IC) for component-specific slow control and External Control (EC) for external components. The remaining 80 bits are divided into five groups of 16 bits (E-groups), each with 8 E-paths of 2 bits, configurable for various data patterns. E-links identify these fields, containing FELIX board and fiber numbers.

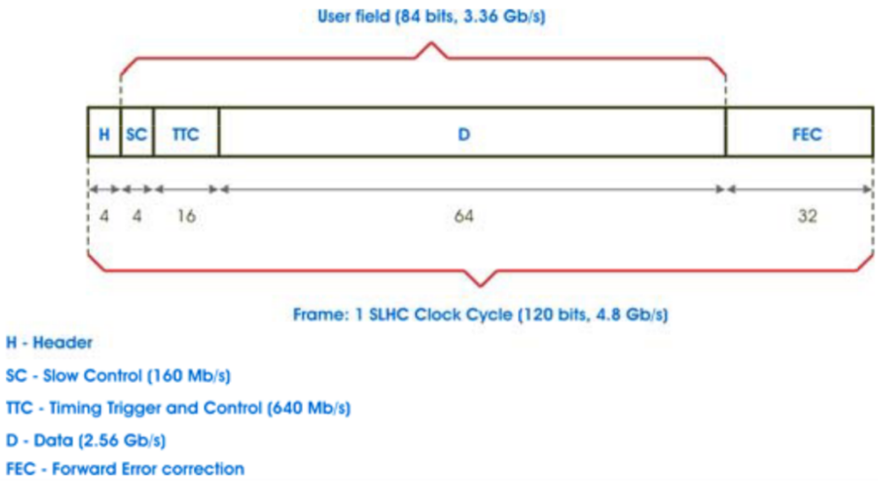


Figure 2.22: The GBT frame composed of 5 fields [55]

For LAr LTDB requirements, a specialized FELIX firmware modifies the GBT frame. It replaces TTC and Data fields with five new 2-bit fields and 70 unused bits. The EC field controls the direct SCA, while one field manages the auxiliary SCA. The other four transmit TTC BCR data to LOCx2 components via GBTx, specifically for down-links. Additionally, two slow control fields serve as up-links to transmit data from SCA to FELIX. As more than 2 bits are needed for SCA instructions, multiple GBT frames (see in Figure 2.23) are used to send packets, then sequentially transmitted to the SCA by GBTx.

field	hdr	IC	EC	Bank 4			Bank 3		Bank 2		Bank 1		Bank 0	FEC
width	4	2	2	2	12	2	14	2	14	2	14	2	16	31
use		IC	SCA	SCA-AUX		BCR		BCR		BCR		BCR		
bits	119-116	115-114	113-112	111-110	109-98	97-96	95-82	81-80	79-66	65-64	63-50	49-48	47-32	31-0

KC_LTDBbits_v01

Figure 2.23: The specific GBT frame for LAr. One 2-bit E-links is used to directly configure the GBTx. Two 2-bit E-links are used to control the SCAs. Four 2-bit E-links are used for TTC BCR (1 per LOCx2).

2.2.3.2 LAr Digital Processing Blade

The LAr Digital Processing Blade (LDPB) illustrated in Figure 2.24 comprises four Advanced Mezzanine Cards (AMCs) known as LAr Trigger prOcessing MEzzanine (LATOME), integrated into the LAr carrier (LArC) ATCA board. Each LATOME is equipped with an Intel Arria 10 FPGA and features four MTP-12 connectors receiving fibers from the LTDB. Its primary function is to calculate deposited energies in the detector computed from the LTDB ADC values.

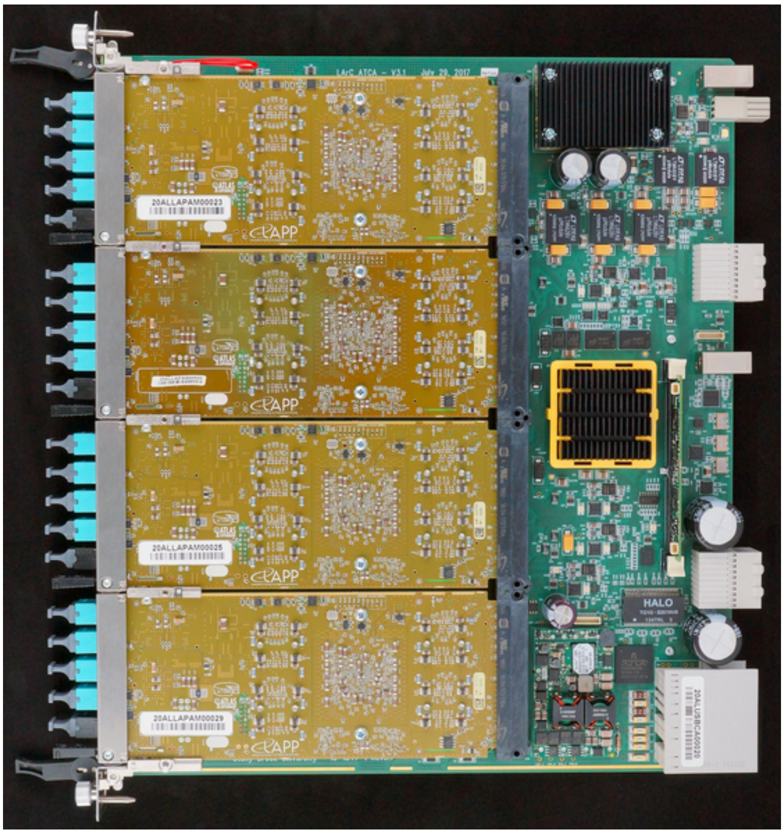


Figure 2.24: A photograph of the LDPB containing a LArC, 4 LATOMEs, an Intelligent Platform Management Controller (IPMC) and a Rear Transition Module (RTM), with the LArC side panels removed.

i. LAr Carrier The LArC is an ATCA standard cut-out blade equipped with a Rear Transition Module (RTM) shown schematically in Figure 2.25. Its primary functions include hosting LATOME processor daughter cards, facilitating data exchange with the readout system, and distributing synchronized clocks and trigger signals aligned with the LHC beam clock. Data connectivity options encompass links to the ATLAS Trigger and Data Acquisition system, standard Ethernet 1 GbE and 10 GbE links via the 10 Gigabit Attachment Unit Interface.

Key data paths on the LArC involve serial Multi-Gigabit Transceiver (MGT) connections for TDAQ data readout, 10 Gbps local monitoring data transfer, Low Voltage Differential Signaling (LVDS) links for clock and trigger distribution, serial transceiver links to optical fibers via Small Form-factor Pluggable (SFP+) modules, and connections between the carrier and other ATCA boards via the backplane.

Clock signals and trigger data are recovered from the TTC data path and distributed across LATOMEs. The Xilinx Virtex-7 FPGA on the LArC serves as the central component, managing all TDAQ and local monitoring data. Clock domains are designated for TDAQ, local monitoring, 1 GbE, and system clock functions.

Additionally, the carrier features GbE connections routed through a BROADCOM switch, connecting various components including LATOME sites, IPMC module, SFP cage on the RTM, and ATCA shelf backplane. An ATLAS standard IPMC provides power and sensor management functions.

The RTM facilitates connectivity for 5 TDAQ channels via SFP+ modules and includes JTAG connectors, an insertion indicator switch for RTM power control, and standard ATCA connectors for data and power connections to the carrier.

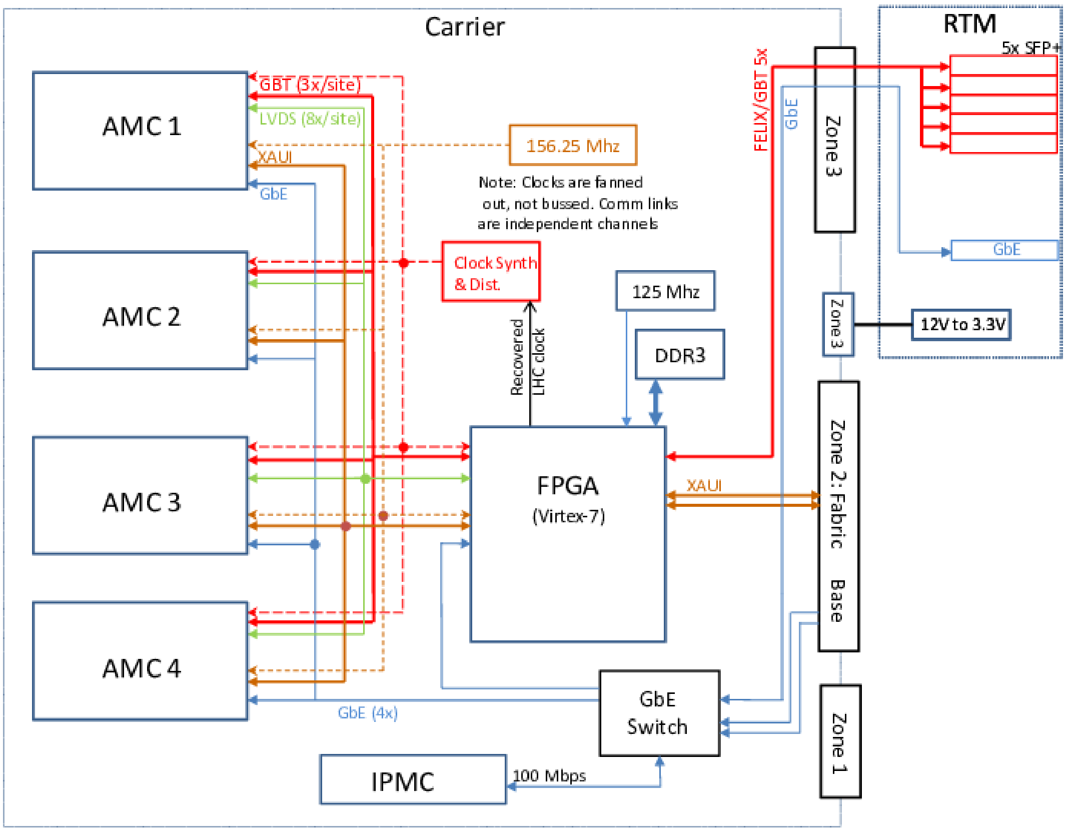


Figure 2.25: Block diagram of the data and clock connections on the LArC.

ii. LATOME The LATOME board show on Figure 2.26 serves as the crucial component in data processing and transmission within the ATLAS system. It reads incoming data from 48 optical links at 5.12 Gbps, processes them using a high-performance FPGA, and transmits the results through 48 optical links at 11.2 Gbps to the Feature Extractors (FEX). Additionally, it connects to standard Ethernet networks (1 GbE and 10 GbE) and the specific ATLAS network (TDAQ) for monitoring and control purposes. Plugged into the LArC, which provides connectivity, the LATOME board adheres to the AMC standard.

At its core, the LATOME board houses an Intel Arria 10 FPGA, with four DC/DC converters managed by a sequencer chip. The FPGA firmware boots from a 1Gb serial flash memory, with two 2Gb DDR3 external memories for data exchange. Clocks required for synchronizing internal FPGA logic are provided by four oscillators.

The front panel of the LATOME board includes five high-density Multi-fiber Push On (MPO) optical connectors, FPGA JTAG and test outputs, MMC JTAG port, reset push button, and status LEDs.

LATOME boards are categorized into six types with distinct mapping configurations, covering various parts of the detector (see Table 2.2).

LATOME type	Description
EMB	Full coverage of the Electromagnetic Barrel, with 4 LATOMEs per quadrant
EMB/EMEC	Covers the shared region between the Barrel and the Endcap LTDBs, with 4 LATOMEs per quadrant
EMEC	Central region of the Electromagnetic end-cap
EMEC/HEC	Forward region of the end-cap and the HEC, with 2 LATOMEs per quadrant
FCAL1	First layer of the forward calorimeter, with 1 LATOME per side
FCAL2	Second and third layers of the forward calorimeter, with 1 LATOME per side

Table 2.2: Description of the different LATOME types

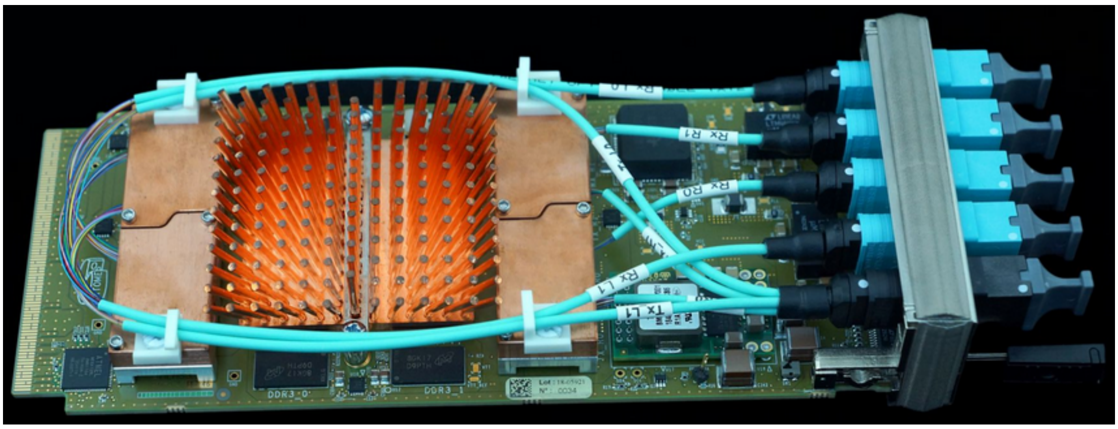


Figure 2.26: LAr Trigger prOcessing MEzzanine (LATOME) board

ii.i LATOME firmware The LATOME firmware consists of several blocks illustrated on Figure 2.27, the input stage block, the configurable remapping block, the user code and the output summing.

- The **input stage** receives and decodes the LTDB data stream, then aligns the input streams from different fibers to ensure they are synchronized to the same Bunch Crossing IDentifier (BCID).

- The **configurable remapping** reorders the data from the input stage block for each Bunch Crossing (BC). It will group the Super Cells that are part of the same Trigger Tower.

- The **user code** block collects Super Cell data from the configurable remapping block and delivers the reconstructed E_T (transverse energy) and data quality bits synchronously to the output summing block, aligning with the relevant BC and maintaining a consistent latency. Several steps are taken to achieve this.
  A BCID pedestal correction is applied to compensate for the imperfect pile-up effect cancellation caused by events at the start of an LHC bunch train. The correction is computed directly on the LATOME FPGA and updated approximately after every 10 seconds for each Super Cell and each BC.
  Finite Impulse Response (FIR) filters are used to compute the total energy E_T and the product of E_T and time ($E_T\tau$) from the ADC input values. A BCID selection algorithm then determines the correct E_T and BCID of the Super Cell signal based on the computed values. The saturation flag is raised for saturated inputs, with specific criteria for identifying the proper bunch crossing. Quality bits are stored along with E_T and BCID data, and in the absence of a physics signal, E_T output is set to zero.

$$E_T = \sum_{i=0}^{3} A_i(S_i - p - b) \tag{2.6}$$

$$E_T\tau = \sum_{i=0}^{3} B_i(S_i - p - b) \tag{2.7}$$

  A_i and B_i are the OFCs stored in a DB (DataBase), S_i correspond to the ADC samples from the LTDB, p for the pedestal level stored in another DB and b is for the baseline correction computed for each BC. More details on the BC identification or the saturation detection can be found in this paper [47] chapter 4.4.2.

- The **output summing** block aims to regroup the data received from the user code in order to calculate sums over specific η/ϕ zones and send the data to the FEX output fibers.

- The **TTC** block receives the TTC signals from the FELIX-TTC. It decodes the relevant TTC information and propagates them to the other firmware block.

- The **TDAQ/Monitoring** block will send the ADC data and the transverse energy data from each Super Cell to two external paths the TDAQ system and the monitoring system. Before sending this transmission the data are buffered until reception of the trigger decision.

- The **IPBUS controller** block serves to load or modify the configuration parameter of the LATOME. It is done using the IPBUS protocol [56].

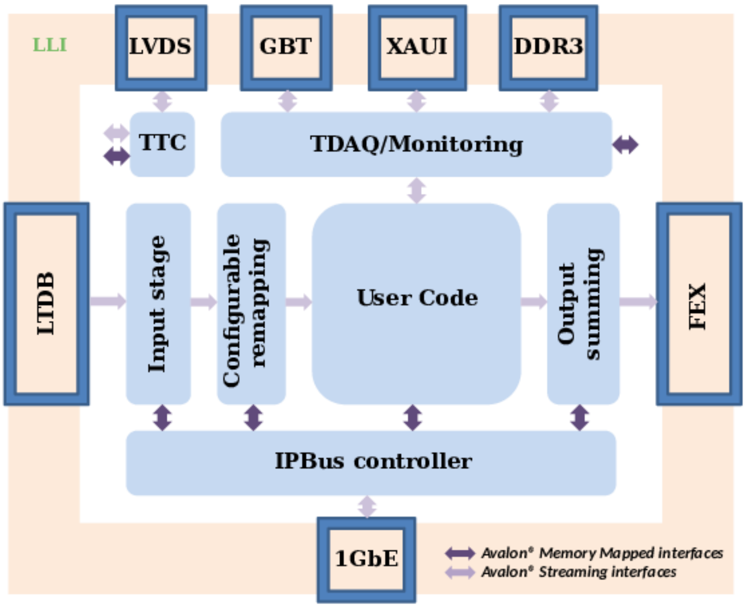


Figure 2.27: LATOME firmware block diagram. The pale brown frame corresponds to the interface with the hardware while the blue boxes correspond to the higher level functional blocks.

iii. IPMC The Intelligent Platform Management Controller (IPMC) shown in Figure 2.28 serves for managing hardware within ATCA boards. It supports intelligent management of power, cooling, and interconnect needs, as well as event monitoring and logging to a central repository. The IPMC also manages mezzanine modules according to user implementations and communicates with the Shelf Manager.

The IPMC is designed in a mini Dual In-line Memory Module (mini-DIMM) form factor, with its mezzanine communicating via local IPMB with the Modular Management Controller (MMC) installed on the LATOME AMC. The board contains two microcontrollers: the IPMC and the IOIF (Input/Output Interface). The IPMC controller is responsible for controlling and monitoring the operations and status of the ATCA carrier board, while the IOIF controller provides an extended I/O interface and handles non-IPMC features.

The IPMC software, based on the Intelligent Platform Management Controller softwARE (ICARE) framework, is loaded onto these microcontrollers. ICARE is fully compliant with ATCA specifications and provides features for managing ATCA requirements, building user code, and generating Field Replaceable Units (FRU) and Sensor Data Records (SDR). It offers command-line and remote command-line interpretation, serves as a firmware upgrade server, and supports Transmission Control Protocol (TCP) and User Datagram Protocol (UDP) echo servers. Additionally, ICARE provides a Xilinx Virtual Cable server.

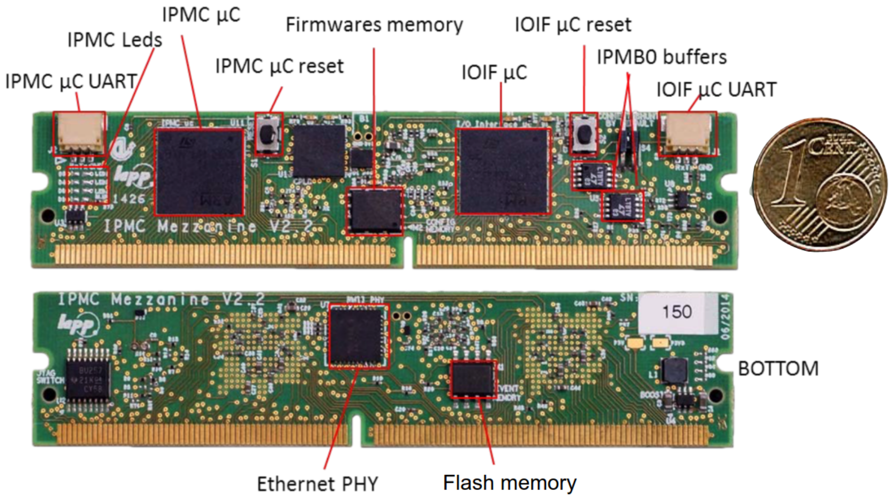


Figure 2.28: Intelligent Platform Management Controller (IPMC) board [57].

2.2.4 Software for control and monitoring of the Phase-I upgrade

Multiple software tools have been developed to oversee, manage, and configure the LTDBs. These tools are categorized into three main groups: generic low-level tools, specific LAr software tools tailored to the needs of the LAr hardware, and user clients that bridge the interface with DCS and TDAQ users. A variety of software packages are utilized to interface the LTDB hardware.

2.2.4.1 Felixcore

Felixcore, developed by the FELIX team, serves as a crucial software package for managing FELIX boards. Acting as a TCP server, Felixcore facilitates the transmission of data between the FELIX boards and their associated E-links. Specifically designed for the LTDB, it establishes a communication interface connecting the OpcUaSca server to the HDLC E-links linked with the SCAs. To enable smooth communication, the FELIX team has designed a dedicated library, called Netio, which integrates optimally with the OpcUaSca server, ensuring efficient data exchange.

2.2.4.2 OpcUaScaServer

The OpcUaSca Server, a development of the ATLAS Central DCS team, serves as a centralized server for managing communication with Slow Control Adapters (SCAs), vital components utilized in controlling and monitoring front end boards within ATLAS subsystems, notably the Liquid Argon calorimeter (LAr) and the New Small Wheel (NSW) detector. These subsystems heavily depend on SCAs for their operational and data acquisition needs.

The OpcUaSca server plays a crucial role in ensuring standardized communication with SCAs across various ATLAS sub-detectors. It acts as a central communication hub, facilitating interactions with SCAs through FELIX boards.

The hierarchical structure and functionalities of the OpcUaSca server are outlined by its communication protocol, configuration settings, and interaction with hardware components. Additionally, it emphasizes the significance of libraries and tools provided to streamline the development and integration processes, ensuring efficient operation and data acquisition within the ATLAS experiment.

2.2.4.3 OpcUaLarLtdbServer

The OpcUaLarLtdb Server [58] was tailored to meet the exacting demands of the LAr sub-detector, specifically for the Liquid Argon Trigger and Digitization Board (LTDB). Equipped with advanced functionalities, it provides high-level methods for the comprehensive monitoring, configuration, and calibration of the LTDB.

This custom server was developed to address the critical needs of the LTDB accessed by both the DCS and TDAQ systems. Updated the server and develop new tools in this framework in order to improve the control, the monitoring and the stability of the LTDB. Engineered with a focus on managing client concurrency, simplifying client interaction, and ensuring effective error handling, the OpcUaLarLtdb server underwent rigorous development, testing, and integration into the DCS and TDAQ systems.

Utilizing the OPC-UA protocol, the server seamlessly communicates with the OPC-UA SCA server, DCS, and TDAQ systems. Developed primarily in C++ and leveraging the Quasar framework, it interfaces with the LTDB and LATOME boards using the IpBus and OPC-UA libraries.

Configuration of the server is facilitated through multiple XML files, encompassing standard configurations for LTDB components, specific LTDB configurations, LATOME descriptions, mapping files for fiber connections, and calibration files. These configurations are designed to accommodate hardware differences and allow for dynamic changes without necessitating server restarts, particularly crucial during commissioning and data-taking periods.

The server's backbone is built upon Quasar-generated C++ code, with hierarchically organized classes addressing various functionalities and hardware components. Innovative workarounds were devised to overcome protocol limitations in DCS client software, expanding the scope of method calls beyond cache and source variable access. Error management is handled by the LogIt module, while a dedicated library streamlines client development, providing direct access to the server's address space.

Employing a multi-threaded implementation, the server ensures efficient handling of SCAs, error detection, and board monitoring. Specialized classes manage specific functionalities, including SCA interaction, component configuration, fiber mapping, calibration tasks, error logging, and data retrieval, contributing to the robust operation of the LTDB within the ATLAS experiment.

2.2.4.4 Monitoring of the LTDB boards

The operation conditions, including digital calibration constants for ADCs, component temperatures, and fiber light levels for back end communication, are read by an OpcUA application. Subsequently, they are sent to the DCS server, as detailed in Section 1.4.5. Initially, a ping operation tests connectivity with the boards, ensuring functional communication and enabling condition analysis.

Big effort was made to integrate the ATLLARLTDB project into the ATLAS DCS system, which organizes the entire detector via a hierarchical node structure. The LTDB boards are housed within the LTDB node, nested within the infrastructure and LAr nodes. This integration allows the FSM system to manage node states and statuses, which propagate upwards, influencing the global state of the detector. Commands executed at higher nodes cascade to affect all sub-nodes. The LTDB system, part of this integration, includes commands for powering boards on or off, and detailed monitoring panels aid in issue identification. These panels depict LTDB states and statuses, with colors reflecting their conditions. They feature essential parameters such as PDB voltages, SCA currents, temperatures, and critical GBTx registers. Additionally, Wincc OA archives SCA and PDB values for display over time, facilitating expert interventions to reset GBTx and SCA components, monitoring of control fibers, and running calibrations like the ClkDes scan.

2.2.4.5 Control of the LTDB boards

The LTDB configuration follows a structured process, consisting of default transitions and recovery steps for boards facing issues. Default configuration steps, known as transitions, alter the LTDB's state. Six transitions manage board control, with certain transitions restricted to the DCS client. These transitions are detailed in Table 2.3.

Transition name	Description
Power On	Activates PDB regulators and sets the state to ON
Init	Validates SCA IDs, configures MTRx control links, loads XML configuration files and mapping, and sets the state to Initialized
Configure	Configures GBTx, MTxs, LOCx2s, ADCs, loads delays and correction coefficients, and sets the state to Configured
UnConfigure	Sets the state back to Initialized
Shutdown	Sets the state to ON
Power OFF	Deactivates regulators and sets the state to OFF (DCS client only)

Table 2.3: Description of possible transitions of the LTDB boards

Before each transition, the OPC-UA LAR LTDB server verifies the board's state compatibility. Five states control the LTDB (see Table 2.4):

LTDB States	Description
Unknown (UNK)	Server cannot determine board state due to various reasons
Off (OFF)	PDB regulators are off
On (ON)	PDB regulators are on
Initialized (INIT)	Board is ready for configuration
Configured (CONFIG)	Board is configured for data acquisition

Table 2.4: Description of the different states that the LTDB can take

To mitigate radiation-induced Single Event Upsets (SEUs), boards are returned to the ON state after each data acquisition run. Frequent temperature changes, resulting from power regulator activation, can damage boards, hence they remain powered on to prevent temperature fluctuations. Initialization prepares the board for data acquisition by configuring control paths and loading configuration files. Reconfiguration before each data run reduces SEU effects. The current state of each LTDB is monitored and provided in the server's address space.

3 Performance of the Phase-I electronics upgrade

Summary

The LAr Trigger Digitizer Board (LTDB) is an essential component of the Phase-I upgrade for the trigger systems. However, during the commissioning period it was confronted with several major problems that affected its stability and efficiency, notably ADC problems (MDAC calibration, dynamic pedestal jumps), timing shift induced on the precision of the digital trigger with an impact on the energy reconstruction but also on the level 1 trigger efficiency, as well as radiation effects observed on LTDB components. Improving the stability of data transmission to the back end electronics is essential.

This chapter looks at these problems, explaining their causes and impacts, as well as their solutions.

3.1 LTDB ADC calibration

In the new trigger readout architecture, the signal digitization was moved to the beginning of the processing chain and is now realized by the LTDB (LAr Trigger Digitizer Board). An ensemble of requirements are imposed on the ADCs present on the LTDBs so that trigger performance matches what is expected. One of the strictest requirements is the radiation hardness. The high intensity of the radiation coming from the particle beam must not affect significantly the electronic performance. While an ADC on the market capable of meeting all these requirements was available, for cost reasons and above all because of the experience gained during development, that could be used for the development of Phase-II chips, which will require greater precision, it was decided to develop an ASIC (Application Specific Integrated Circuit) ADC with a custom architecture for this project.

Nevis ADC, the commissioned converter, is a 12-bit pipeline ADC with 4 stages of 1.5b Multiplying Digital-to-Analogue Converters (MDACs), followed by an 8-bit Successive Approximation Registers (SAR). The calorimeter pulse enters the first MDAC (stage 1) which resolves the Most Significant Bit (MSB) of the digital code (V_{in}) and outputs a residual for the next stage (V_{res}). This procedure continues until stage 4 where the last MDAC resolves its bit and sends a residual for the SAR unit which resolves the 8 last bits. This architecture allows high precision, low energy consumption, and fast sampling rates. A unique feature of the new ADC architecture is that the MDACs need to be calibrated (detailed in the Section below) to prevent non-linearity errors caused by structural imperfections in their components. An uncalibrated MDAC can cause discontinuities in the digital signal as shown in Figure 3.1, causing problems in the data and eventually decreasing trigger performance. The mentioned imperfections can be compensated digitally by applying corrections to the digital output. These corrections are implemented by calibration constants that have to be loaded into the device.

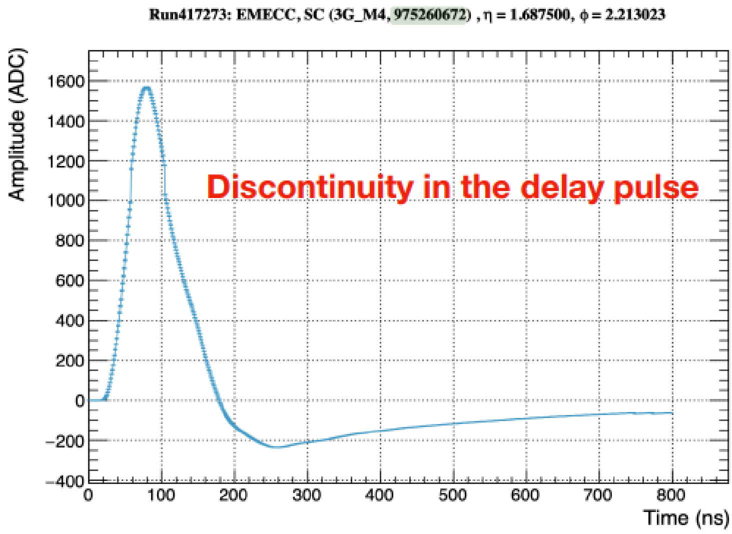


Figure 3.1: Pulse digitized by an ADC with calibration problems. A discontinuity is observed in the bulk of the pulse around the 1000 ADC count amplitude range due to the MDAC scale change.

3.1.1 MDAC calibration

Fig. 3.2 depicts the transfer function of an MDAC stage. The left side plot shows the relationship between V_{res} and V_{in} and the right plot presents the reconstructed digital output for each input voltage. The gain is defined by capacitors at the input and the output of this amplifier. To ensure the proper behavior of the converter, the gain should be as close as possible to two. If the gain diverges too much from this ideal value, discontinuities start to appear in the digital reconstruction. This phenomenon is represented by the dashed lines in the Figure.

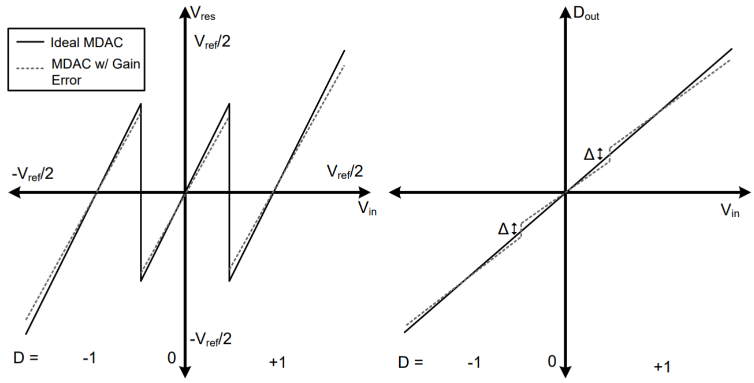


Figure 3.2: MDAC transfer function and simulated reconstructed digital output. The ideal behaviour is presented by a continuous line, while the depiction of an MDAC with gain error is depicted by the dashed line [59].

The gain error is caused by the components of the switching capacitor circuit, whose precision is limited by the CMOS process that produces the MDACs so it cannot be modified. The effects of these errors are mitigated by a digital calibration, where calibration constants are added to the digital output to correct the measure.

To calibrate the MDACs it is necessary to measure the decision level amplitude (discontinuities in the left plot of Fig. 3.2), the necessary correction will be the deviation from the ideal decision level height and its measure. The MDACs can be forced into these levels with a special calibration mode that allows the user to select a desired digital output value.

The calibration procedure is structured as follows:

- Force $V_{in} = -V_{ref}$ and $D = -1$, read $V_{res}^1 = V_{res}$
- Force $V_{in} = -V_{ref}$ and $D = 0$, read $V_{res}^2 = V_{res}$
- $\Delta_1 = V_{res}^2 - V_{res}^1 - V_{ref}/2$
- Force $V_{in} = V_{ref}$ and $D = 0$, read $V_{res}^3 = V_{res}$
- Force $V_{in} = V_{ref}$ and $D = 1$, read $V_{res}^4 = V_{res}$
- $\Delta_2 = V_{res}^4 - V_{res}^3 - V_{ref}/2$
- Finally, convert measure to digital $C_i = 2^{12} \times \frac{\Delta_i}{V_{ref}}$ for $i \in \{1,2\}$

The calibration procedure for the Nevis ADC has 16 modes, where the 2 endpoints of the 2 decision levels of all 4 units are evaluated and stored in a list called *caldata*.

The following equations represent the calculations needed after gathering all calibration data:

$$C_4^1 = 128 + \text{caldata}[1] - \text{caldata}[0] \qquad C_7 = 128 - C_4^1$$
$$C_4^2 = 128 + \text{caldata}[3] - \text{caldata}[2] \qquad C_6 = 256 - C_4^1 - C_4^2$$
$$C_3^1 = (C_4^1 + C_4^2) + \text{caldata}[5] - \text{caldata}[4] \qquad C_5 = 256 - C_3^1$$
$$C_2^3 = (C_4^1 + C_4^2) + \text{caldata}[7] - \text{caldata}[6] \qquad C_4 = 512 - C_3^1 - C_3^2$$
$$C_2^1 = (C_3^1 + C_3^2) + \text{caldata}[9] - \text{caldata}[8] \qquad C_3 = 512 - C_2^1$$
$$C_2^2 = (C_3^1 + C_3^2) + \text{caldata}[11] - \text{caldata}[10] \qquad C_2 = 1024 - C_2^1 - C_2^2$$
$$C_1^1 = (C_2^1 + C_2^2) + \text{caldata}[13] - \text{caldata}[12] \qquad C_1 = 1024 - C_1^1$$
$$C_2^1 = (C_2^1 + C_2^2) + \text{caldata}[15] - \text{caldata}[14] \qquad C_0 = 2048 - C_1^1 - C_1^2$$

In the equations, C_j^i represents the correction measured on the decision level i of MDAC j. These values are later used to calculate the list of calibration constants (C_0 - C_7) that are loaded into the ADC registers (one pair for each MDAC). The list of constants is saved on text files that are read by the LTDB OpcUaLarLtdb server. Table 3.1 presents how the 8 constants present on the files correlate to the MDAC calibration constants.

MDAC	Calibration constants
$MDAC_1$	C_1
	C_0
$MDAC_2$	C_3
	C_2
$MDAC_3$	C_5
	C_4
$MDAC_4$	C_7
	C_6

Table 3.1: NevisADC digital calibration constants organization.

Since the boards are on the detector and cannot be taken out to a test bench while the detector is closed, there was a significant effort to measure and calculate the calibration constants. After a first set of default constants measured at the production of the chips, a second set of constants was computed in the testing bench and a third set of constants was computed directly on the detector. For this, an analysis framework was devised [60], based on a calibration data acquisition run. Calibration pulses with ascending amplitude are injected into the calorimeter cells, covering the ADC's full working range from pedestal to saturation. Using 3000 distinct amplitudes repeated 100 times each, this setup provides comprehensive coverage of the converter's range and ensures sufficient statistical data for accurate analysis.

To conclude on the stability of the MDACs calibration, the fourth set of constants was produced and then analyzed by the framwork. No nonlinearity problems were detected. These calibrations are now used once per year just as verification to see how constant evolve with the time and the radiation. Of course we redo also this calibration when an LTDB need to be exchange due to various problems during the end-of-year shutdown.

3.1.2 Dynamic pedestal jump

Another problem observed with the ADC was a dynamic change in pedestal while in operation as illustrated in Figure 3.3 for one ADC channel. These changes cause the whole measurement to shift up and down affecting the trigger selection, as the amplitude of the pulse peak is misperceived. The source of the problem has still not been identified but as it happens simultaneously in all ADC channels of one chip, it is believed to be an ADC problem.

For now, mitigation solutions are taken on the LATOME firmware side so it doesn't represent a problem to the trigger system anymore. this will be validated after the restart of the third year of run 3. In the meanwhile, the problem is being investigated by experts.

These jumps are not linked to a physics event as the pedestal shift occurs along several consecutive measurements without any particle pulse observed.

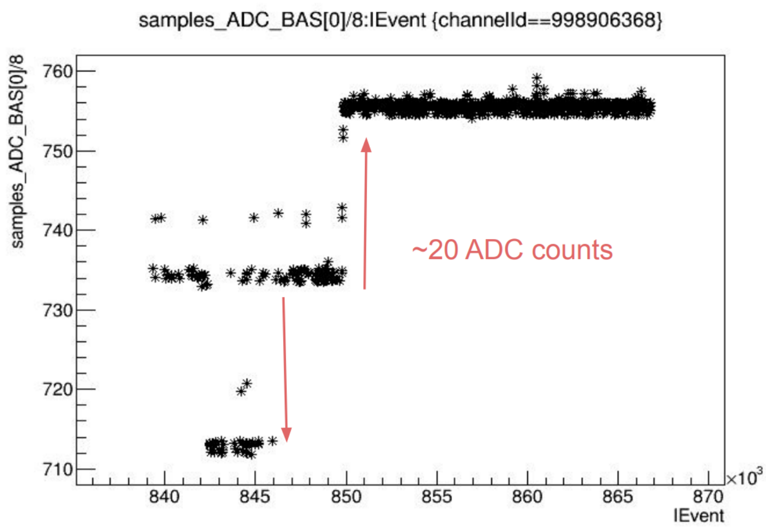


Figure 3.3: Measurement of a Super Cell response in which the ADC presented pedestal jumps.

3.2 Timing shift on the Digital Trigger

3.2.1 Description of the issue

The reconstruction of the deposited energy in the calorimeter cells is performed by an Optimal Filtering Coefficients (OFC) [6] algorithm described in Section 2.2.3.2. To ensure that the timing of the peak sampling remains consistently positioned for all channels of the digital trigger and provides an optimal reconstruction of the energy, some calibration is needed to roughly align the peak ADC sample with the maximum energy. The effect of the mis-alignment, which induces a 2% shift in the energy response of the trigger, will be described later in 3.2.3.8. However, during the analysis of the data obtained from a daily calibration, some issues were observed. Specifically, the peak sampling of certain channels showed a timing shift of a few nanoseconds named τ.
This timing shift is expected to impact on the performance of the digital trigger system. Due to the inconsistency in the alignment of the maximum energy with the peak sample in the ADC pulse (Figure 3.4), the reconstruction of energy will be less optimal.

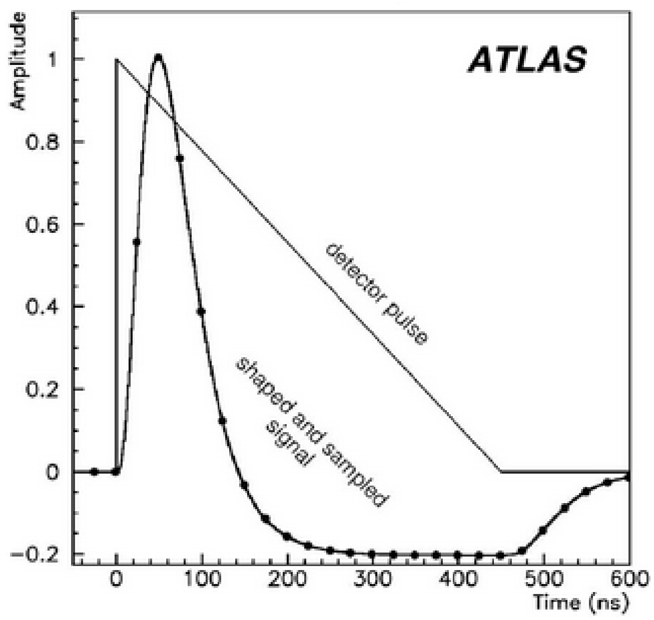


Figure 3.4: Pulse shape from the detector before and the read out after shaping and sampling.

It is worth noting that this type of timing shift was previously observed after replacing one of the FELIX boards. The replacement was necessary e.g. due to an FPGA fan failure on one of the FLX-712 boards installed in the FELIX LTDB machine. It is believed that this timing shift may be induced by the power-cycle of the FELIX LTDB machine.

3.2.2 Description of the setup and procedure used

To investigate the cause of this timing shift, several power-cycles were conducted including disconnection/connection of fibers between the Wendy boxes and the FELIX LTDB machines (see Figure 2.21) between two calibration runs, and the resulting data were analyzed. The Wendy box is a patch box to map the fiber coming from the LTDB with a connector of 12 channels to the FLX-712 board with a connector of 48 channels. The full η/ϕ region of the detector is divided into eight parts, corresponding to the eight FELIX LTDB machines. Using a chess pattern, as shown in Figure 3.5, the eight machines are divided into two groups, to have the same number and type of LTDBs in each group. For all the following tests, the blue group will contain pc-lar-felix-ltdb-00, pc-lar-felix-ltdb-02, pc-lar-felix-ltdb-05, and pc-lar-felix-ltdb-07, and the black group the other four machines pc-lar-felix-ltdb-01, pc-lar-felix-ltdb-03, pc-lar-felix-ltdb-04 and pc-lar-felix-ltdb-06. One of the two groups will be power-cycled and the other one will stay untouched between two calibrations.

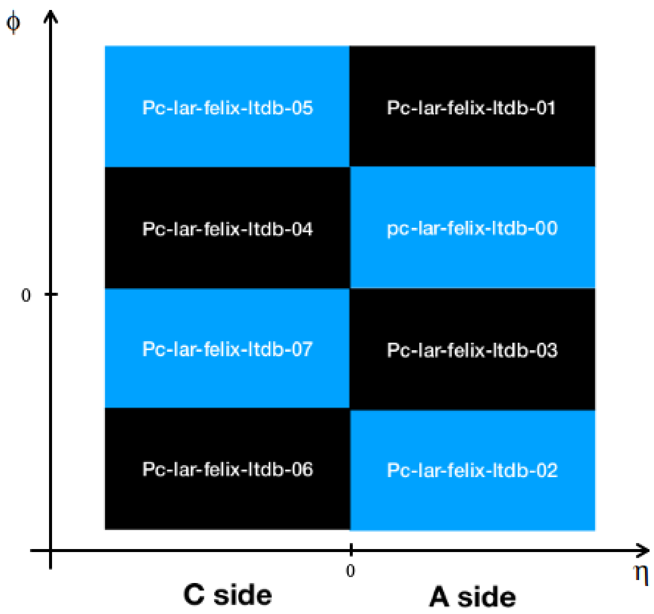


Figure 3.5: Chess pattern used to group FELIX LTDB machines to have all types of LTDBs flavor on the A and C side of the detector for all the different tests done on the digital trigger for the investigation of the timing shift.

As described in Section 2.2.2.3, several flavors of LTDBs exist, and the chess pattern ensures that all flavors of LTDBs are tested consistently across the detector. This is important to obtain reliable and comparable results during the investigation. It allows an easy visualization and identification of the issue. Since the Super Cells within

the blue group are well isolated from the others in the black group, any timing shift or anomalies can be readily observed within the corresponding area. This spatial separation facilitates the detection and analysis of the timing shift, making it easier to pinpoint the specific regions affected.
To analyze the data, the pulse peak before the power-cycle of the FELIX LTDB machine or a disconnection/connection will be subtracted from the pulse peak after the power-cycle of the FELIX LTDB machine or a disconnection/connection to see the impact of these effects on the Digital trigger systems. This method was employed to remove errors induced by residual timing shifts caused by other sources.
The following tests were conducted and will be described in detail later: power-cycling the FELIX LTDB machine, resetting the GBTx component, disabling/enabling the light on the μPOD of the FELIX LTDB machine, disabling/enabling the TTC stream and reproducing the issue in a test bench.

3.2.3 Results

The first step in the investigation was to confirm whether the power-cycle of any FELIX LTDB machine induced a timing shift. Figure 3.6 shows the difference of timing of the peak sampling between two calibration runs (τ) of each Super Cell after a power-cycle of the blue machines. Only the Super Cells with a value of $\tau > 3$ns are displayed on this plot.

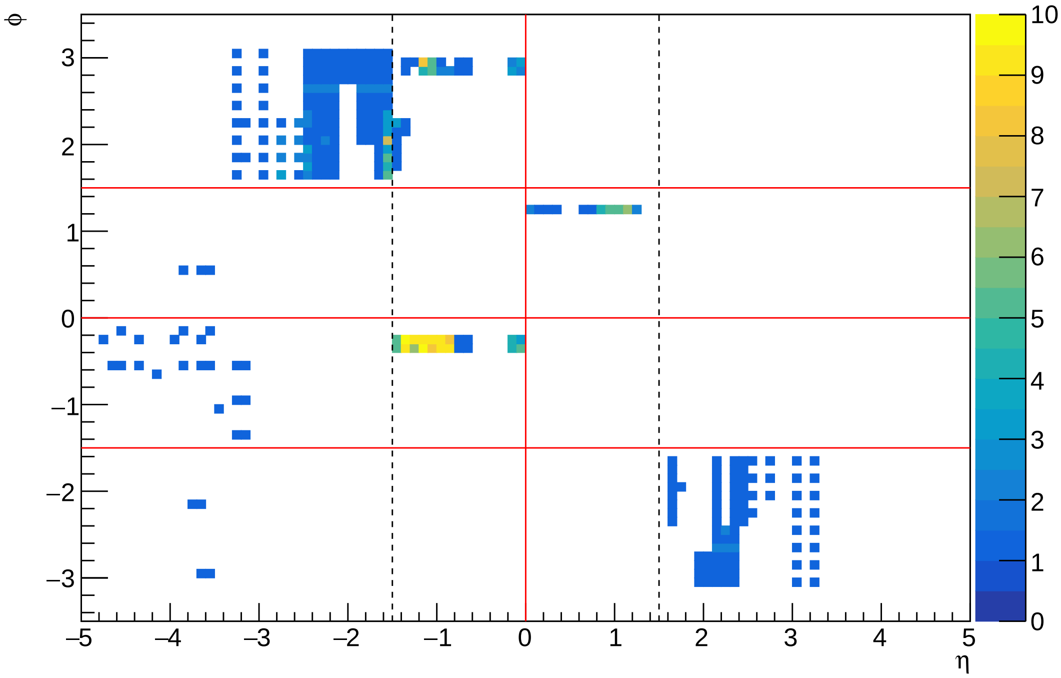
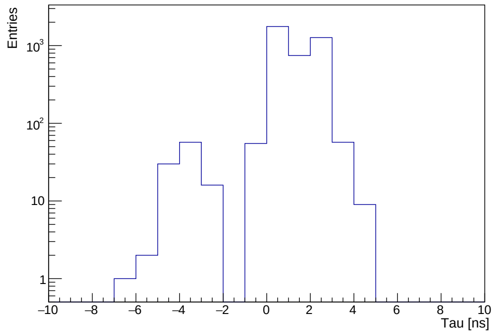
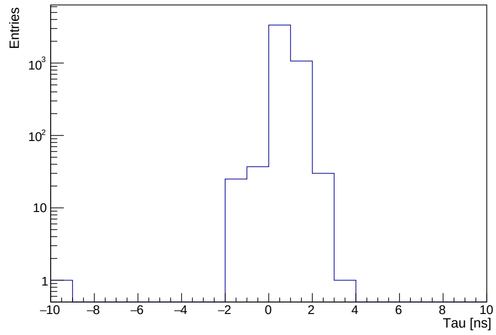


Figure 3.6: Distribution of the number of Super Cells with the value of $|\tau| > 3ns$ in the η/ϕ space. The z-axis shows the number of Super Cells. From top to bottom FELIX LTDB machines 05, 04, 07, and 06 cover the C side ($\eta < 0$) of the detector. The machines 01,00, 03, and 02 cover the A side. The black dashed line in $\eta = \pm 1.5$ delimits the Barrel from the End-Cap Super Cells.

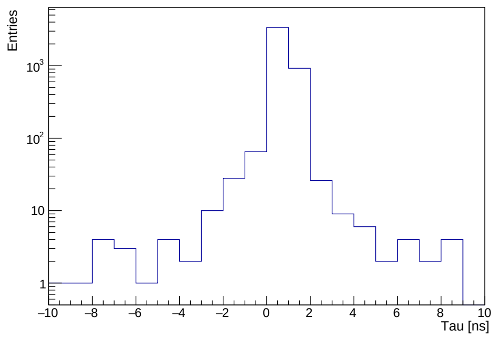
This plot demonstrates that the power-cycle of the FELIX LTDB machine induces a timing shift in many Super Cells connected to this machine (blue machine of Figure 3.5). To double-check this conclusion, a distribution of τ values grouped by the FELIX LTDB machine is shown in Figure 3.7.



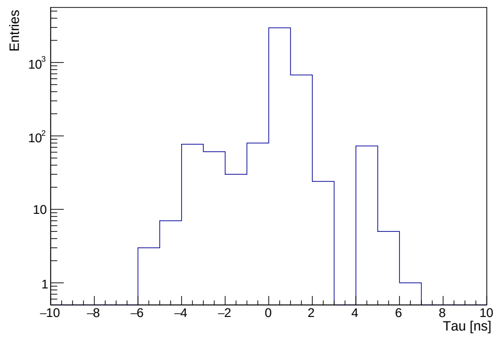
(a) pc-lar-felix-ltdb-00



(b) pc-lar-felix-ltdb-02



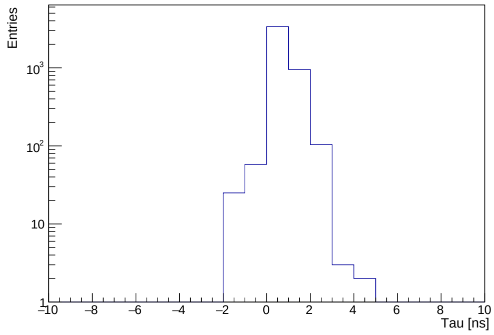
(c) pc-lar-felix-ltdb-05



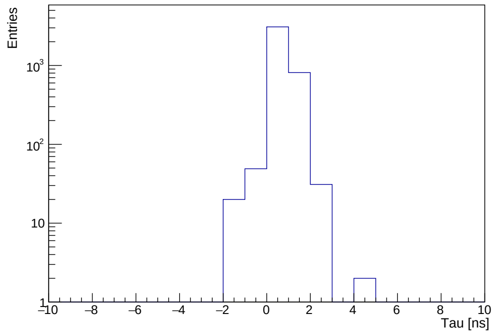
(d) pc-lar-felix-ltdb-07

Figure 3.7: Distribution of τ for all Super Cells per FELIX LTDB machine when a power-cycle is performed.

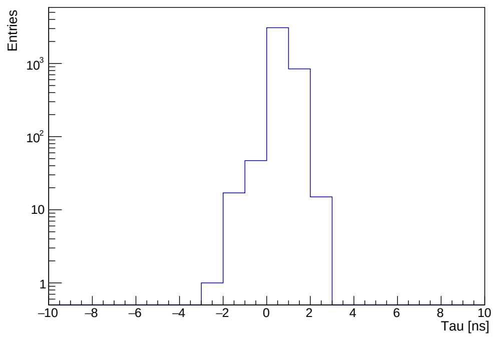
It can be observed that some channels are affected by a timing shift resulting from the power-cycle. Additionally, Figure 3.8 depicts the τ distribution for FELIX LTDB machines that did not undergo a power-cycle.



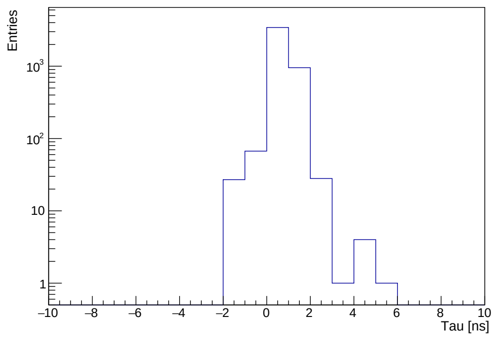
(a) pc-lar-felix-ltdb-01



(b) pc-lar-felix-ltdb-03



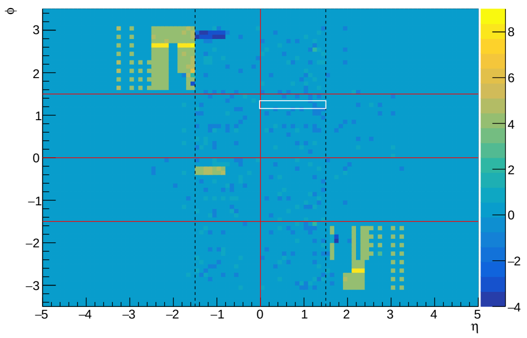
(c) pc-lar-felix-ltdb-04



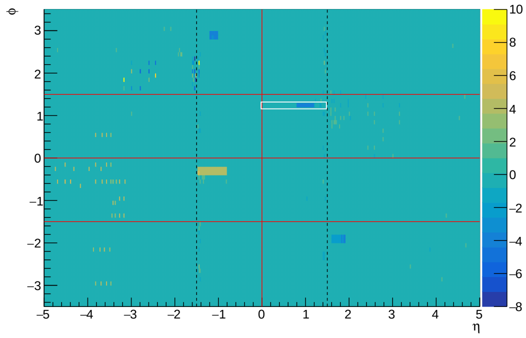
(d) pc-lar-felix-ltdb-06

Figure 3.8: Distribution of τ for all Super Cells per FELIX LTDB machine when no power-cycle is performed.

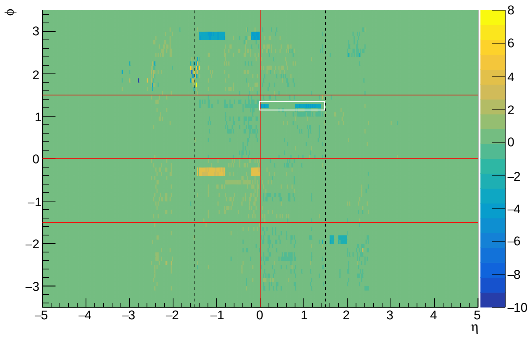
All histograms are centered around zero nanoseconds, and the timing appears to be stable if the FELIX LTDB machines have not been power-cycled. Another important information to extract was the magnitude of the timing shift and whether it remained consistent. To assess the deviation of τ, the τ values were plotted per layer to avoid being misled by the overlap regions of certain Super Cells (Figure 3.9). Most of the τ values fall within a range of $|\tau| \approx 5ns$ for all the calibration runs conducted with power-cycled machines.



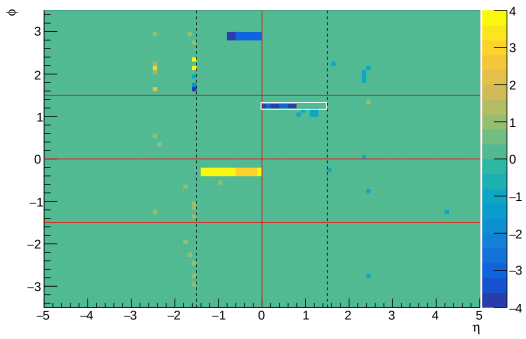
(a) Super Cells of the preSampler layer



(b) Super Cells of the front layer



(c) Super Cells of the middle layer



(d) Super Cells of the back layer

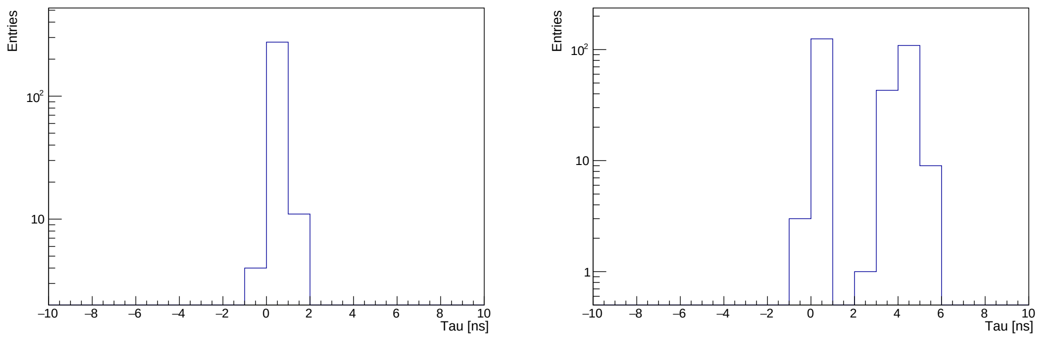
Figure 3.9: Distribution of the τ value in η/ϕ space per layer. The z-axis reflects τ in nanoseconds. power-cycle were performed on FELIX LTDB machines 00, 02, 05 and 07. LTDB I04L used below is identified in the white rectangle in $0.0125 < \eta < 1.4625$ and $1.2241 < \phi < 1.3223$.

Since the timing shift is induced by a power-cycle of the FELIX LTDB machine, the next step was to identify the specific cause. A power-cycle implies various actions such as resetting transceivers, re-locking the PLL (Phase-Locked Loop), cutting off the light from the FLX-712 board to the LTDB, and interrupting the TTC (Timing, Trigger, and Control) stream. To pinpoint the exact cause, each of these actions was tested independently to determine which one was responsible for the timing shift.

3.2.3.1 LTDB side

After examining smaller units than the FELIX LTDB machines, a similar analysis was conducted at the LTDB level, as shown in Figure 3.10. Plotting the τ value separately for each layer, was helpful to identify several hot spots. This suggests that the timing shift issue is not uniformly distributed across all LTDBs but rather localized in certain regions. Furthermore, it is significant to observe that the timing shift is consistent across all flavors of LTDBs. This indicates that the specific type or flavor of the LTDB does not have a significant impact on the timing shift issue. This information helps to

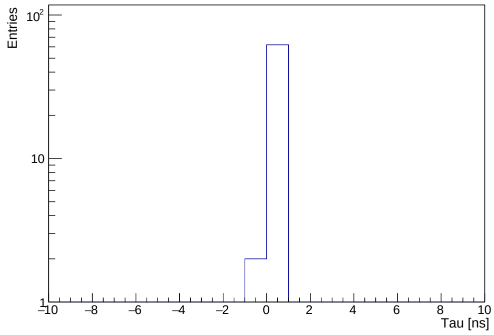
narrow down potential causes and eliminates the possibility that the timing shift is specific to a particular LTDB flavor. Knowing that, the following tests were done on the LTDB I04L which is inside the white rectangle in $0.0125 < \eta < 1.4625$ and $1.2241 < \phi < 1.3223$, as depicted in Figure 3.9.
In Figure 3.10b it can be observed that the timing shift is not present in all channels of the LTDB since some channels remain centered around 0ns.



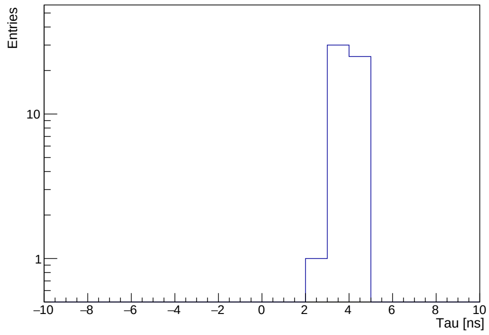
(a) (b)

Figure 3.10: Distribution of τ for all Super Cells connected to the barrel LTDB (I04L). Figure (a) is without a power-cycle and for Figure (b) with a power-cycle of the FELIX LTDB machine.

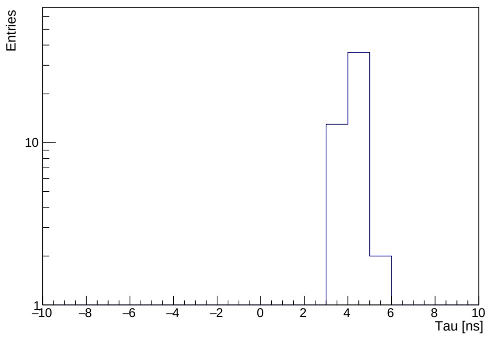
This finding led to the decision to investigate the GBT-SCA component, as it receives the clock from the FELIX board. Remarkably, it was observed that all channels served by the same GBT-SCA have a similar timing shift value, as shown in Figure 3.11.



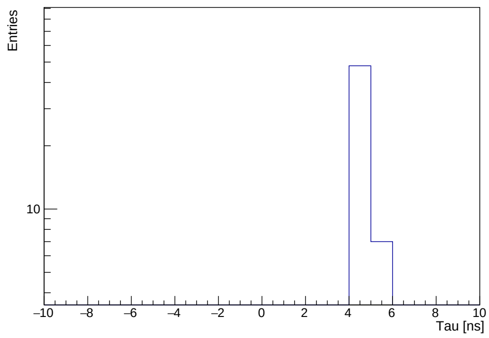
(a) LTDB I04L SCA 1



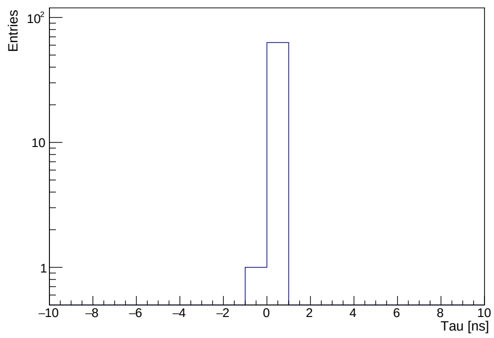
(b) LTDB I04L SCA 2



(c) LTDB I04L SCA 3



(d) LTDB I04L SCA 4



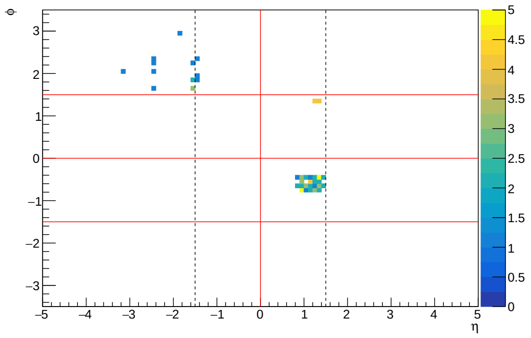
(e) LTDB I04L SCA 5

Figure 3.11: Distribution of τ for all Super Cells connected to the 5 SCAs of the barrel LTDB (I04L) after a power-cycle.

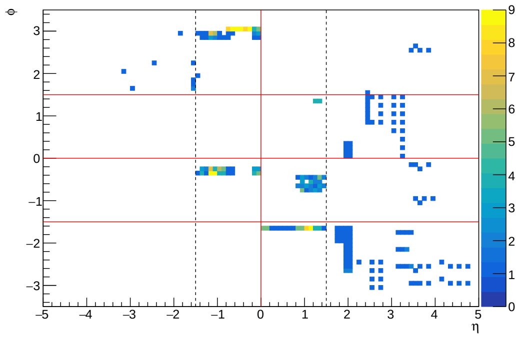
With the understanding that this effect is not seen across the entire LTDB but specifically by these channels connected to one particular component, the GBT-SCA, further tests were conducted to uncover the cause of this issue.

3.2.3.2 GBTx reset

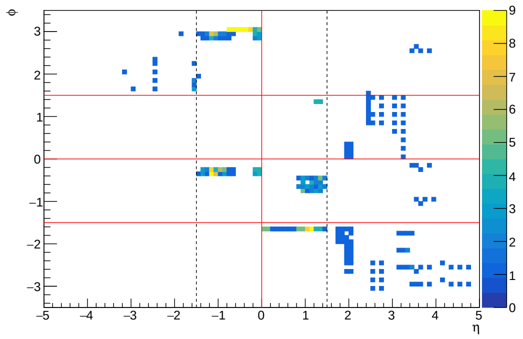
Considering that the GBTx receives the clock from the FELIX board, the hypothesis was that a reset of the GBTx component might be necessary to synchronize the clocks of both electronics after a power-cycle of the FELIX LTDB machine. To validate this hypothesis, a GBTx reset was performed before and after a power-cycle.
Figure 3.12a demonstrates that a GBTx reset does not introduce any significant timing shifts in the system. The small fluctuations observed are within the expected range of precision for our system (on the order of one nanosecond).
A power-cycle was performed on four FELIX LTDB machines (00, 02, 05, 07), as shown in Figure 3.12b. This plot exhibits a distinct trend induced by the power-cycle of the FELIX LTDB machines. Timing shifts are evident in some Super Cells connected to these specific FELIX LTDB machines, indicating that the power-cycle has introduced instability in the timing performance of the detector, along with some minor fluctuations.
To determine if a GBTx reset could resolve the timing shift induced by the power-cycle, another GBTx reset was performed. However, as depicted in Figure 3.12c, the GBTx reset did not correct the timing shift induced by the power-cycle.



(a) After a GBTx reset.



(b) After a power-cycle on blue machines.



(c) GBTx reset post power-cycle.

Figure 3.12: Distribution of the Super Cells with the value of $|\tau| > 3ns$ in the η/ϕ space. The z-axis shows the number of Super Cells. A power-cycle was performed on FELIX LTDB machines 05, 00, 07, and 02.

Based on these observations, it can be concluded that a GBTx reset is not sufficient to mitigate the timing shift caused by the power-cycle.

3.2.3.3 Cut off the light

Another hypothesis was formulated, suggesting that during a power-cycle, the data flow between the FELIX board and the transceiver on the LTDB named MTRx is interrupted and this could cause a timing shift. To investigate this hypothesis, a test was conducted without performing any power-cycles. Instead, the light on these transceivers was disabled and then enabled between two calibration runs.
The results, as shown in Figure 3.13, indicate that disabling and enabling the light of the μPOD of the FELIX LTDB machine does not induce a timing shift. The observed values of τ can be attributed to the fluctuations in timing caused due to the inherent precision.
Hence, it can be concluded that the hypothesis of data flow interruption due to cutting the light of the transceivers does not explain the timing shift observed in the system.

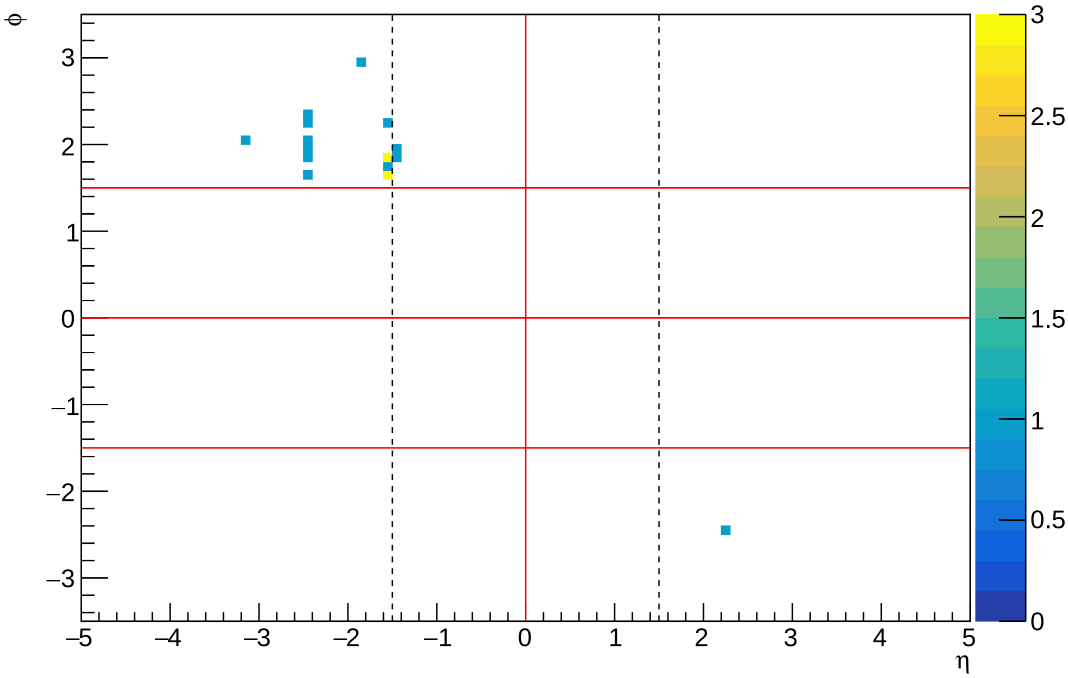


Figure 3.13: Distribution of the number of Super Cells with the value of $|\tau| > 3ns$ in the η/ϕ space. The z-axis shows the number of Super Cells, after an interruption in the light power of all MTRx of the blue FELIX LTDB machines.

3.2.3.4 Cut TTC stream

Another hypothesis was considered, suggesting that the timing shift could be caused by the interruption of the TTC stream, which is received by the FELIX LTDB machines through a fiber plugged into the back of the FLX-712 board. To investigate this hypothesis, the following test was performed:
A calibration run was taken for reference. The TTC fiber was unplugged and then re-plugged on the four selected machines (in this case, the blue machines, as shown in the chess pattern Figure 3.5). Then a second calibration run was taken to observe the effects of this action.
The results of this test, displayed in Figure 3.14, led to the conclusion that cutting the TTC stream at the entrance of the FELIX LTDB machine by unplugging the fiber does not induce any timing shift. The shift observed is different from the one study since only few channels are shifted and not the whole GBT-SCA (up to 320 channels). Moreover, we can see that the value of this timing is around 1ns and not the 5ns previously observed. We can therefore conclude that the interruption of the TTC stream is not the cause of the observed timing shift.

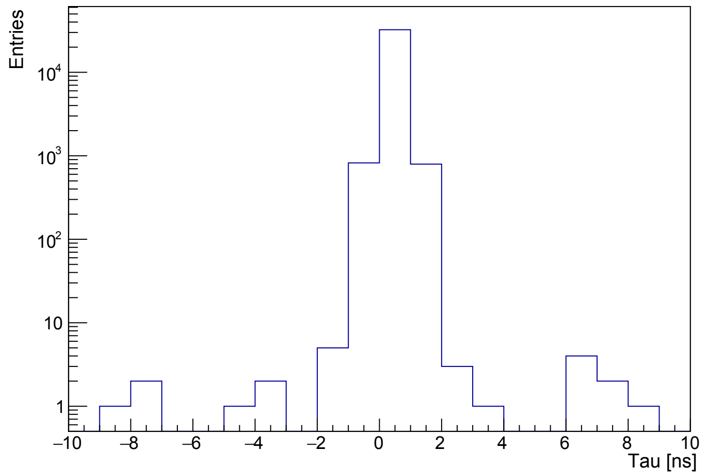


Figure 3.14: Distribution of τ for all Super Cells, after an interruption on the TTC stream of the blue FELIX LTDB machines.

3.2.3.5 FELIX LTDB machine side

At the beginning of the study, a pattern emerged regarding the timing shift. These are the same Super Cells that always seem to be affected by the timing shift. To confirm this hypothesis, power-cycles were perfomed on all the FELIX LTDB machines (see Figure 3.15). To understand why certain Super Cells were consistently impacted by the timing shift, further investigations were conducted.

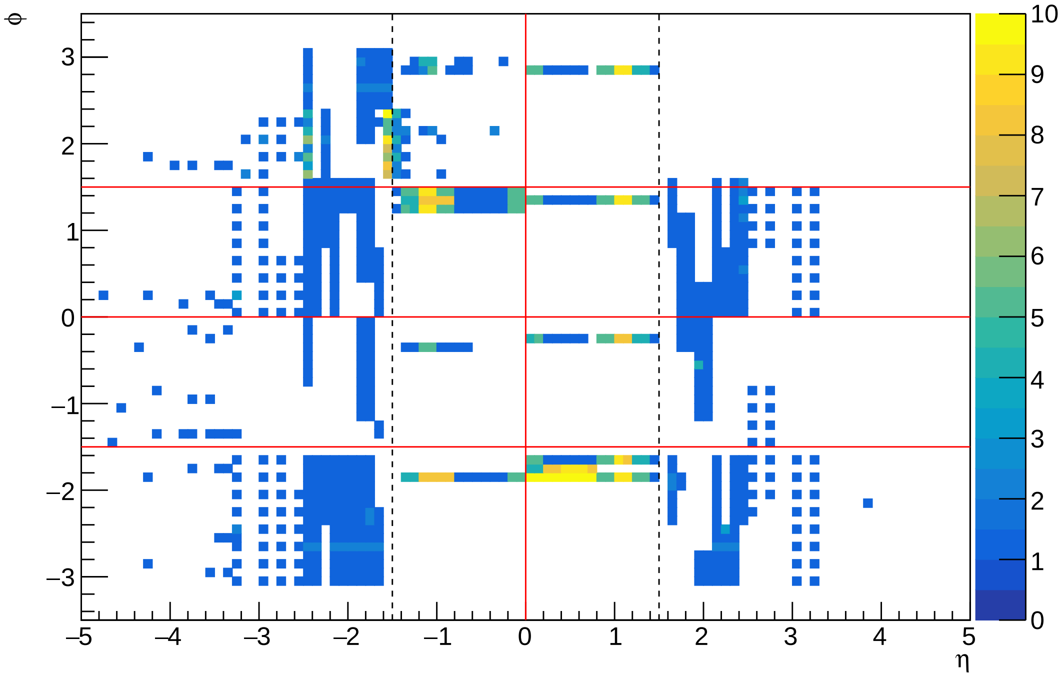


Figure 3.15: Distribution of the number of Super Cells with the value of $|\tau| > 3ns$ in η/ϕ space.The z-axis shows the number of Super Cells after all FELIX LTDB machines are power-cycled.

As described in this Section 2.2.2.3, each LTDB has five control links. The links between the GBTx component on the LTDB and the FPGA on the FLX-712 board used for bidirectional data transmission are called elinks.
To investigate this pattern, the number of Super Cells affected with τ values greater than three nanoseconds was plotted for all 124 LTDBs grouped by elink number using all the calibration runs with power-cycles. The resulting plot, shown in Figure 3.16, indicates that most of the timing shifts are located in the "Device 1" area of each FLX-712 board.

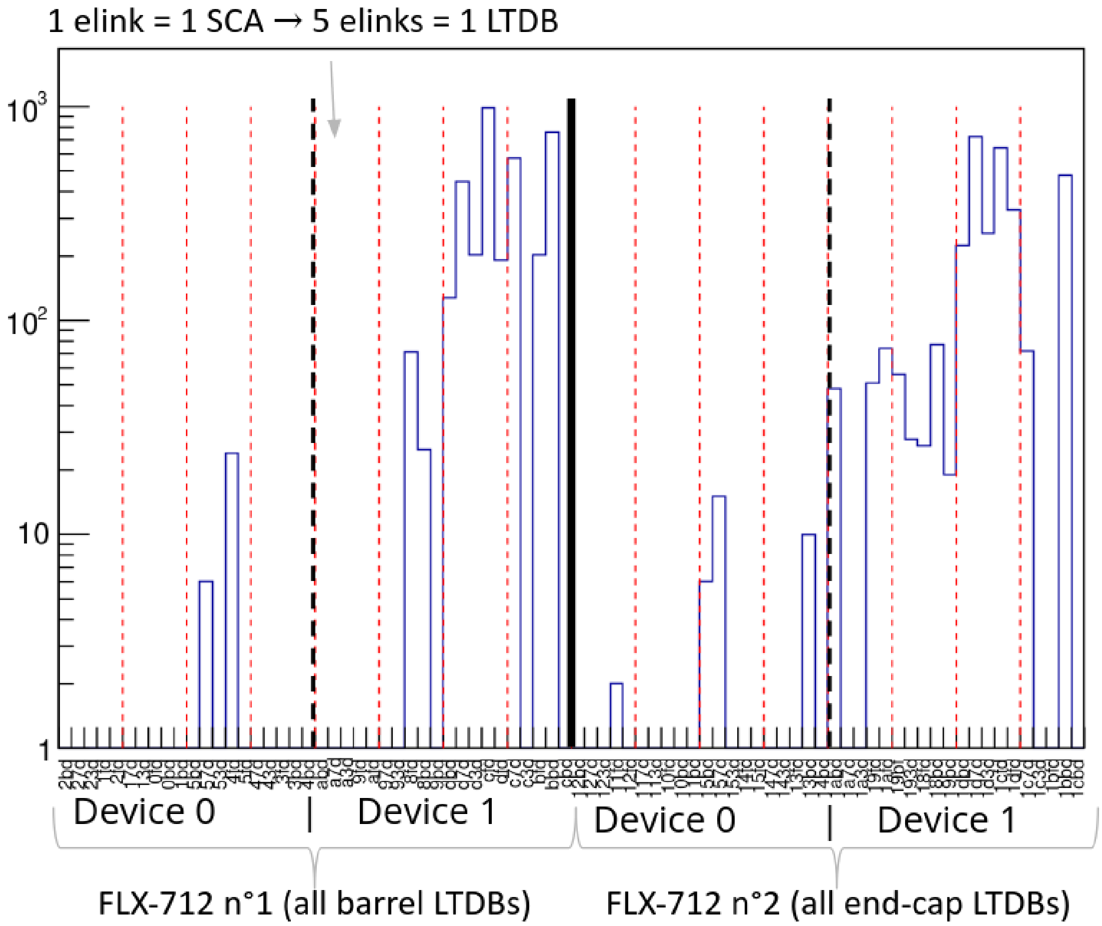
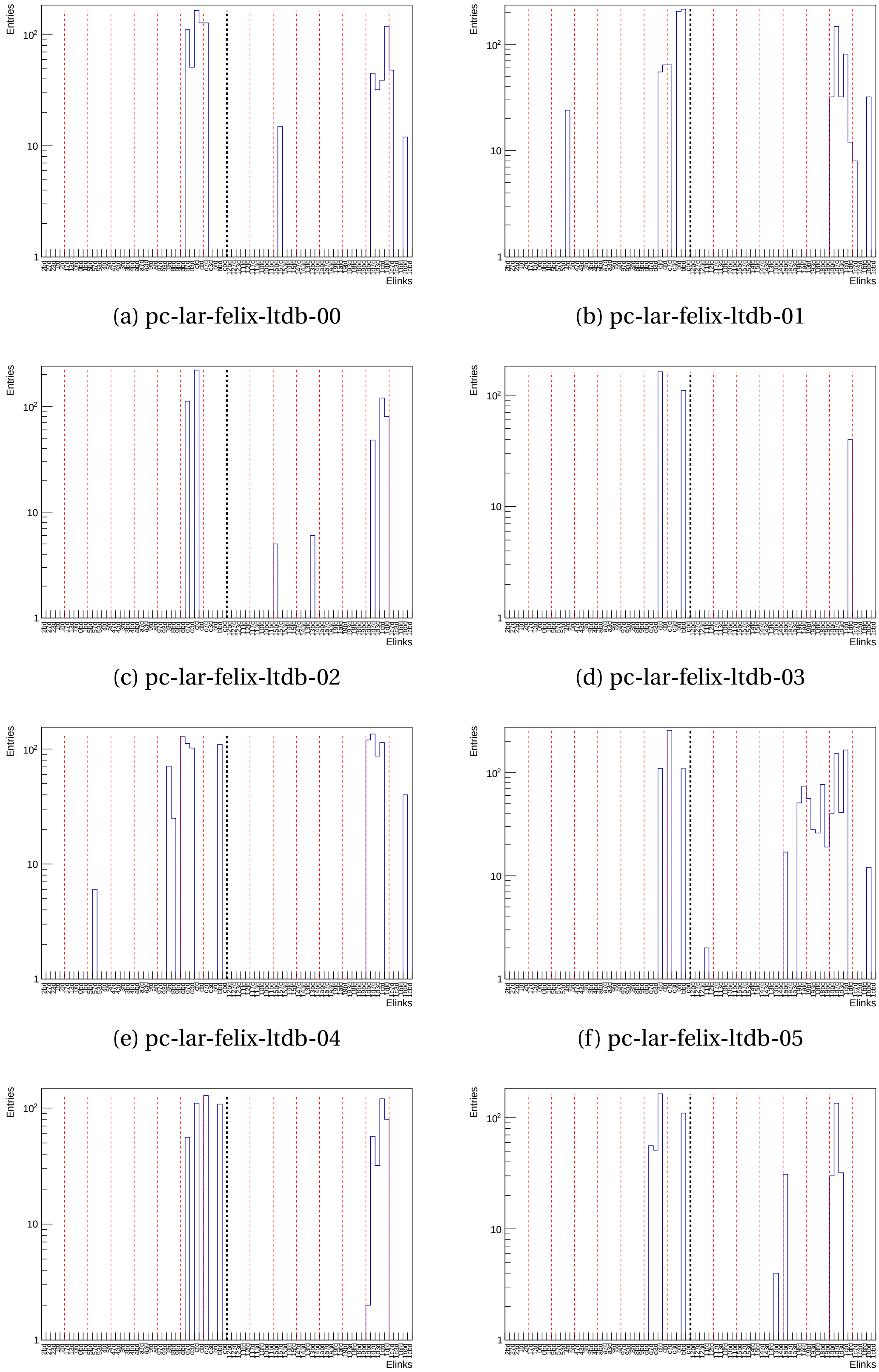


Figure 3.16: Number of Super Cells with a $|\tau| > 3$ nanoseconds per elink for the 8 FELIX LTDB machines and multiple calibration runs with power-cycle. Between two red dashed lines, five elinks represent one LTDB. On the left of the black line are all the LTDBs connected to the first FLX-712 board, and on the right are all the LTDBs connected to the second FLX-712 board.

To determine whether the timing shift originates from the last two LTDBs connected to each FLX-712 board or if it is related to the elinks themselves, the same plot was generated per FELIX LTDB machine. The FELIX LTDB machines with sixteen LTDBs (Figures 3.17a, 3.17b, 3.17e, 3.17f) show that the timing shift mainly occurs on the last two LTDBs of each FLX-712 board. However, in Figure 3.17f, the timing shift is more prevalent on the last four LTDBs of the second FLX-712 board; this effect is not understood for this machine.
For the four other FELIX LTDB machines with fifteen LTDBs (Figures 3.17c, 3.17d, 3.17g, 3.17h), the timing shift is occurring on the last two LTDBs for the first FLX-712 board, but only on the last LTDB for the second FLX-712 board. This effect is related to the number of elinks used on the FELIX card, having one LTDB less on these four cards explains this effect.



(a) pc-lar-felix-ltdb-00

(b) pc-lar-felix-ltdb-01

(c) pc-lar-felix-ltdb-02

(d) pc-lar-felix-ltdb-03

(e) pc-lar-felix-ltdb-04

(f) pc-lar-felix-ltdb-05

(g) pc-lar-felix-ltdb-06

(h) pc-lar-felix-ltdb-07

Figure 3.17: Number of entries for $\tau > 3$ nanoseconds per elink and per FELIX LTDB machines and multiple calibration runs.

Since the elinks have the same ID on the FLX-712 board and in our setup we have two FLX-712 boards, it is not possible to reach a conclusion on this pattern. To obtain a more definitive conclusion, a swap between the fiber on the back of the FLX-712 was required. The planned test involved swapping the fibers between the Wendy boxes and the FELIX LTDB machine, as shown in the diagram 3.18. This test aims to observe on which elink the timing shift consistently appears and gather more insights into the hardware-related causes of the timing shift.

3.2.3.6 Hardware modification to determine the faulty part

After observing a consistent timing shift primarily affecting specific elinks, a new test was performed. It involved taking a calibration run, swapping the two fibers on the FELIX board, power cycling the FELIX LTDB machines, and subsequently conducting another calibration run. The analysis of these two runs aimed to ascertain whether the elink where the timing shifts occurred had changed. A shift in position would suggest that the issue resides within the LTDB, whereas if the shift remained in the same location, it would indicate a problem on the FELIX side. An example of this swap on one FELIX board is illustrated in Figure 3.18.

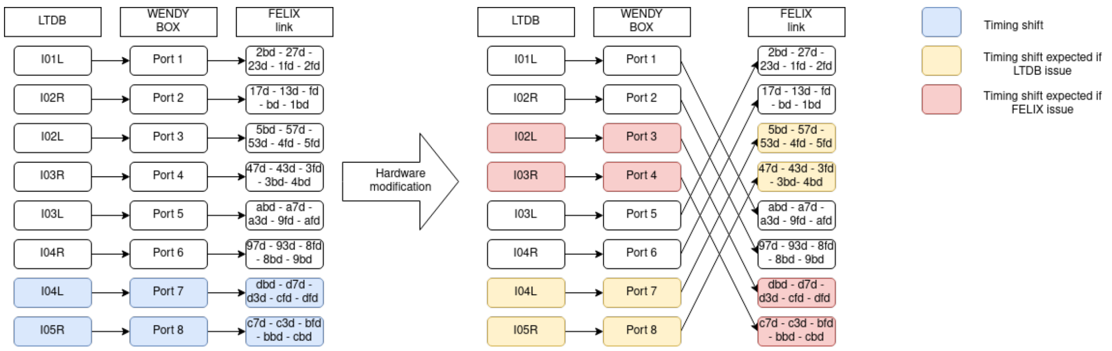
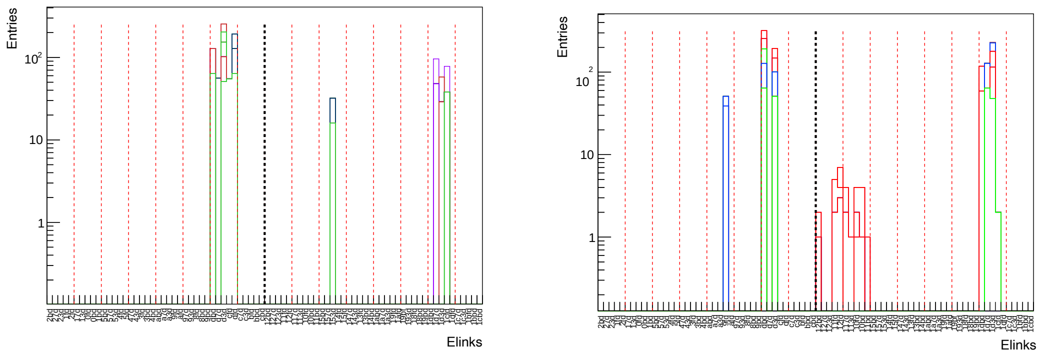


Figure 3.18: Modification of the cabling between the LTDB and the FLX-712 board to determined the source of the timing shift.

For this particular test, the fiber on the blue machines was swapped, while the black machine remained untouched. After performing five power-cycles on both the blue and black machines, with a calibration run between each power-cycle, the resulting plots (see Figure 3.19a and 3.19b) represent the stack of the five power-cycles for each FELIX LTDB machine - four with no swap and four with the swapped fibers. This test allows us to conclude that since the timing shift remained on the same elink between the LTDB and the FELIX FPGA, despite swapping the fiber connectors at the entrance of the FELIX board, the issue originates on the FELIX side.



(a) FELIX LTDB machine not swapped.

(b) FELIX LTDB machine swapped.

Figure 3.19: Number of entries for $|\tau| > 3$ nanoseconds per elink and for 4 FELIX LTDB machines over multiple calibration runs. One color corresponds to one FELIX LTDB. Since the timing shift remains on the same elink despite the movement of the LTDB this confirms that the issue comes from the FELIX side.

3.2.3.7 Reproduction on a test bench

Since this study was conducted during the physics data-taking period, the production setup was not often available. Moreover, each time a power-cycle was performed, it induced a timing shift of five nanoseconds on several channels as we have seen. A mitigation solution is to recompute the timing in the OFC but it takes time to be set up and can not be done during a physics run. To avoid using this solution often to obtain again optimal timing, a lot of effort has been put in place to try to reproduce the issue with a laboratory setup. This setup uses the full chain of data acquisition but with only one Half Front End Crate (HFEC). The setup of the LTDB and FELIX differs slightly since only one LTDB is connected to the FELIX machine, and we only have one FLX-712 board; this is the only difference in terms of hardware. The firmware, the software and the driver are the same as the production system.

To reproduce the issue, the same procedures were used: taking a calibration run, power cycling the FELIX machine, taking another calibration run and doing the subtraction of the two calibration runs to check if $|\tau| > 3ns$ is present on some channels or not. However, it was not possible to reproduce the timing shift even after 40 power-cycles of the FELIX machine (see Figure 3.20).

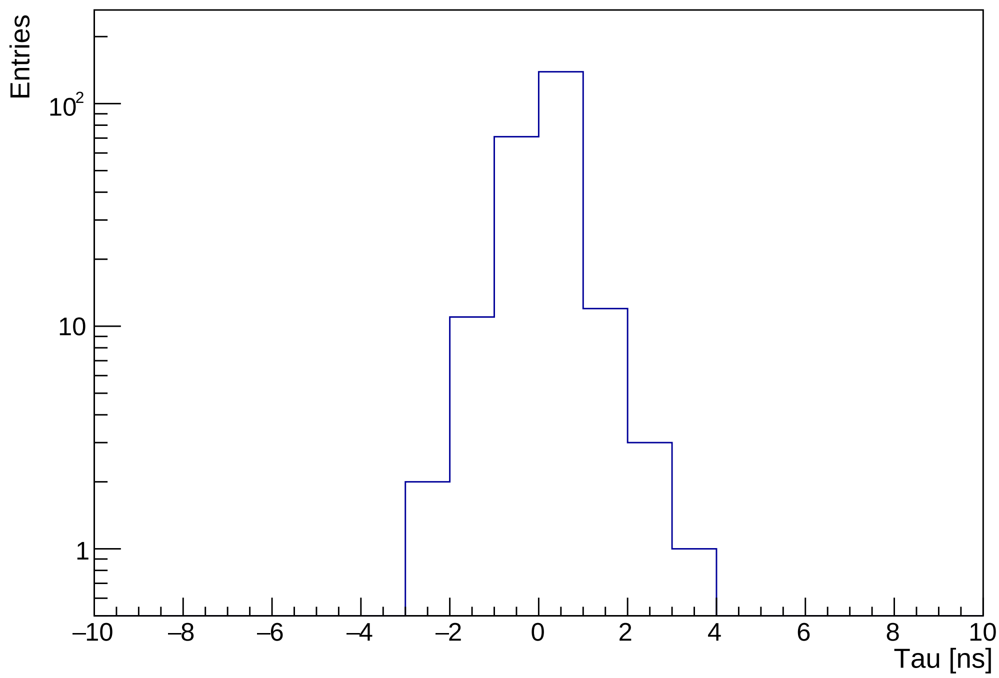


Figure 3.20: Distribution of τ for all the channels of the test bench LTDB.

The only difference between the two setups was the number of LTDBs connected to the FLX-712 board: on the laboratory setup five links are used for only one LTDB, whereas on the production system, 40 links are connected (for one FLX-712) to eight LTDBs. To mitigate this difference, a second FLX-712 board was installed and connected to the 35 unused links of the first FLX-712 board to create some data transmission and be as close as possible to the production system (figure 3.21). Only the channels connected to the LTDB were checked during this test.

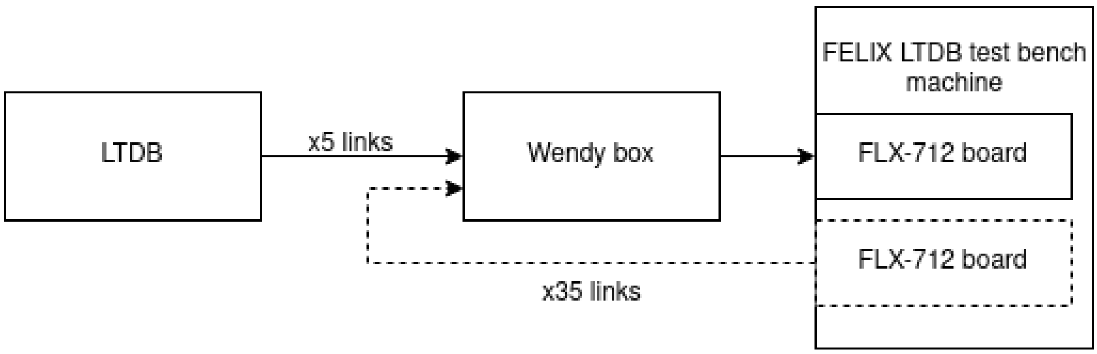


Figure 3.21: Test bench setup with LTDB and FLX-712 board. Drawings with dashed lines represent hardware added to the setup to be as close as possible to the production setup with an FLX-712 with 40 links connected.

With this new setup, several power-cycles and calibrations were retaken, and this time timing shifts of 5ns were observed in some channels(see Figure 3.22). Again all channels of the same GBTx were shifted around a similar value of 5ns, as shown in Figure 3.23d while the other channels connected to different GBTxs are all centered around 0ns (Figures 3.23a, 3.23b, 3.23c, 3.23e).

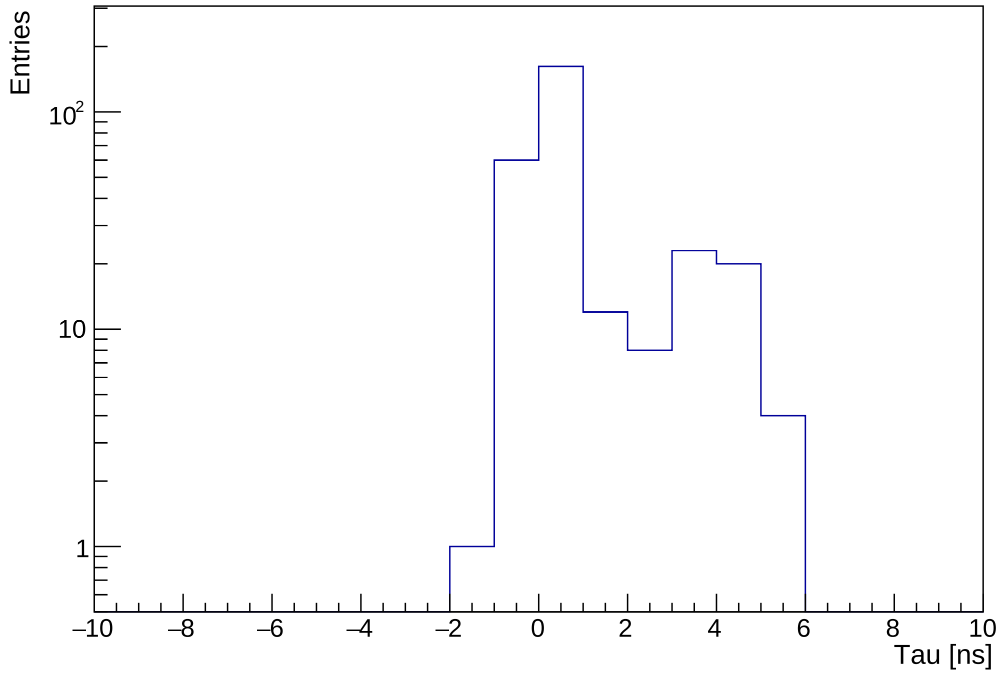
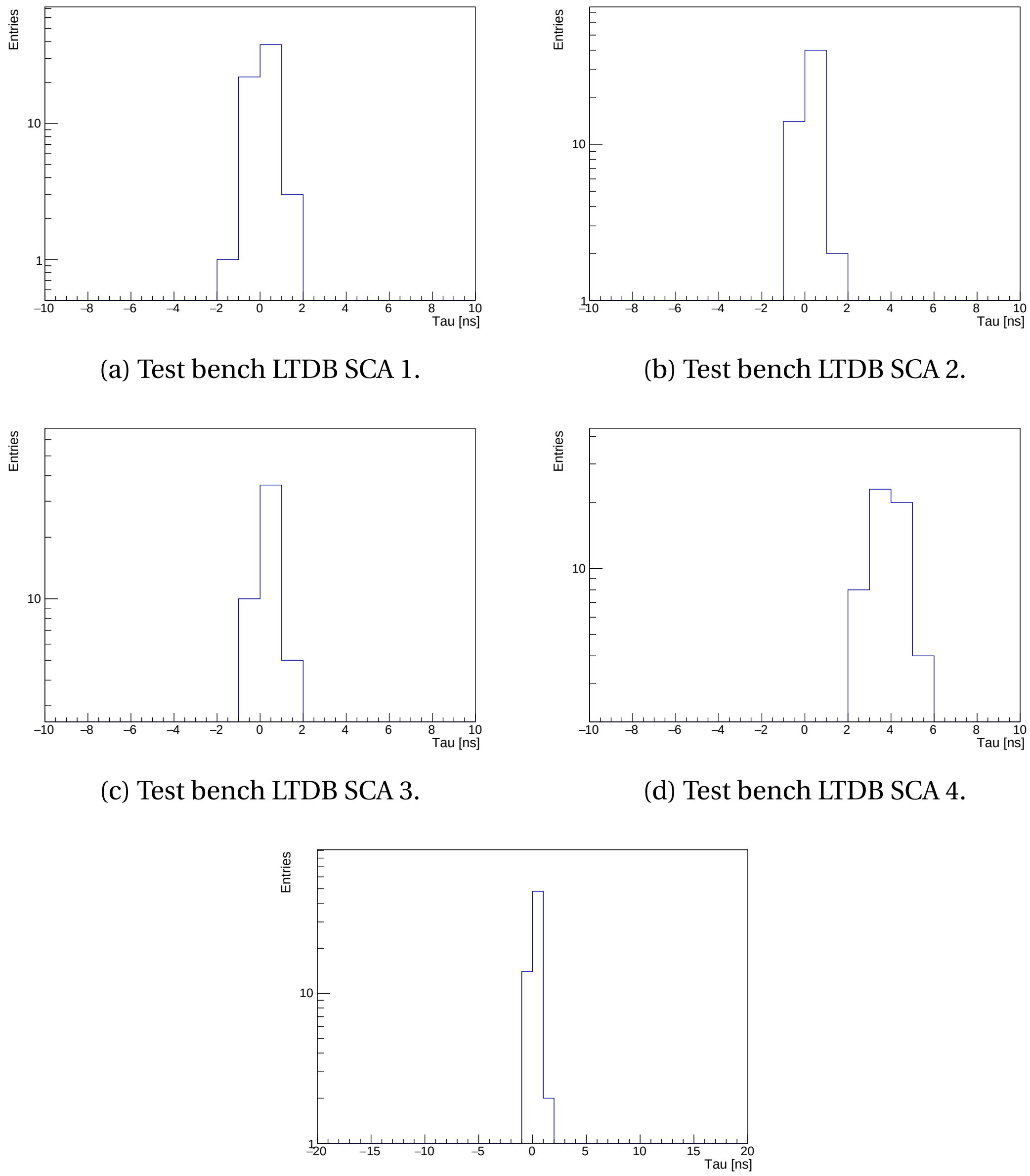


Figure 3.22: Distribution of τ for all the channels of the test bench LTDB, after introducing a second FLX-712 connected to the 35 unused links of the first FLX-712 board.



(a) Test bench LTDB SCA 1.

(b) Test bench LTDB SCA 2.

(c) Test bench LTDB SCA 3.

(d) Test bench LTDB SCA 4.

(e) Test bench LTDB SCA 5.

Figure 3.23: Distribution of τ for all channels connected to the 5 SCAs of the test bench LTDB after introducing a second FLX-712 connected to the 35 unused links of the first FLX-712 board.

The fact that this problem is not visible when only 5 links are in use, but becomes apparent when at least 40 links are connected, provides further indication that the issue is not originating from the LTDB side. Instead, it is likely located on the FLX-712 board or within the FELIX firmware.

3.2.3.8 Impact on energy reconstruction performance

To evaluate the loss of efficiency in energy as a function of the timing shift induced by the power-cycle of the FELIX LTDB machine, a special calibration run was performed. In this run, all Super Cells were pulsed simultaneously with a sufficiently high amplitude to be able to evaluate performance degradation. The sampling phase was shifted in steps of $\approx 1ns$ to obtain the full pulse shape. For each Super Cell, the energies with the same τ value are added together, and then the average energy value for each τ value is calculated. The Figure 3.24 shows the result of this specific calibration for one Super Cell before the computation of the mean energy. To evaluate the impact on the energy reconstruction the ratio as a function of τ=0ns has been computed for a timing shift of -5ns, +5ns, and ±5ns. The results of these three ratios are very similar, so only the result of the ratio at +5ns will be shown.

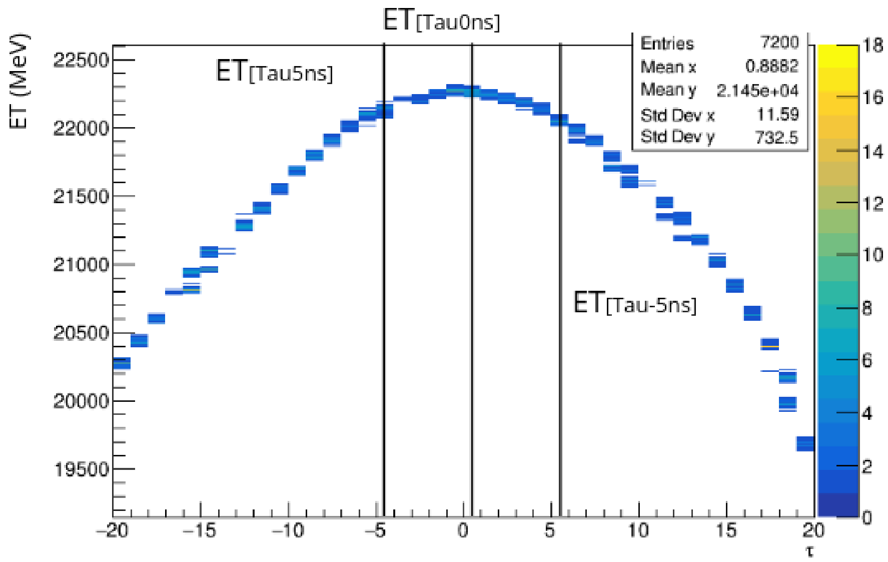


Figure 3.24: Energy computed in one Super Cell as a function of the sample timing τ

Despite the calibration pulse shape being different from the physics one, we assume that the loss in efficiency will be similar in both kinds of runs. The loss in the energy reconstruction for all layers was estimated to ≈ 1% for the EMB (Figure A.1 in annex), ≈ 1.5% for the EMEC (Figure A.2 in annex), ≈ 1.1% for the HEC (Figure A.3 in annex), and 3.4% for the FCal (Figure A.4 in annex). The Figure 3.25 shows the loss

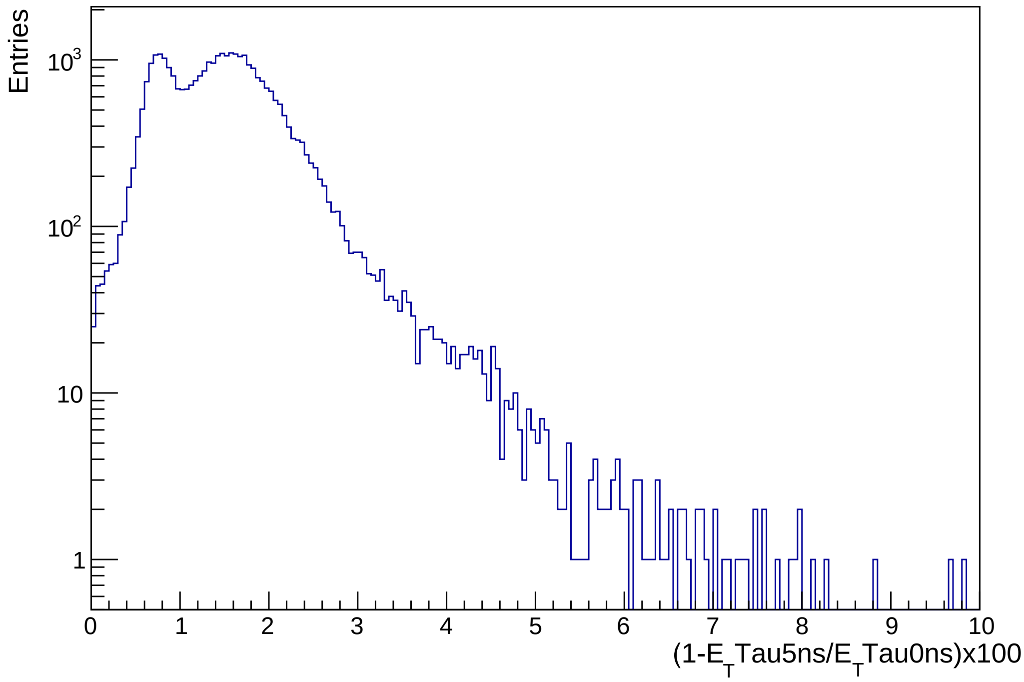


Figure 3.25: Distribution of lost energy ratio for all Super Cells.

3.2.3.9 Impact on the trigger performance

During a physics run with the digital trigger enabled for commissioning purposes, some channels were operated with improper timing. Thanks to the ongoing study aimed at understanding the root cause of the timing shift and since the mitigation method to correct for such a timing shift is long and the time lapse between the two consecutive runs of data taking did not allow to apply it, a study of the impact was made possible. It was observed that the impact of the timing shift on the trigger level turns out to be much more significant than at the level of the reconstruction of the deposited energy as reported in the chapter 3.2.3.8. In Figure 3.26, the turn-on curve of the trigger shows different efficiencies when a timing shift is present on some channels (black curve), compared to when no timing shift is present but the Level 1 trigger is not tuned (red curve) and when the system is correctly timed and tuned (blue curve).

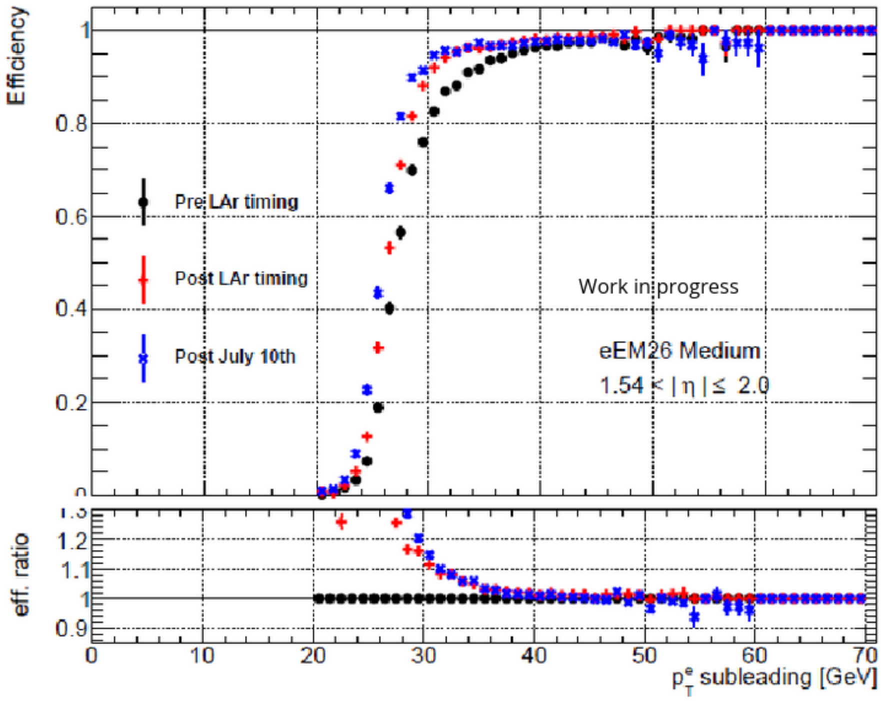


Figure 3.26: Trigger efficiency seen by eFEX in the region $1.54 < |\eta| \leq 2.0$. Work is ongoing to understand why certain regions are more impacted by the timing shift of the Super Cells.

The significant loss in this region could be explained because the triggering efficiency is calculated per Super Cell group. Hence, the number of Super Cells with a timing shift might be more dominant and therefore has a greater impact on the turn-on curve. Figure 3.27 shows the pourcentage of energy loss of all Super Cells in the region where the turn-on curve of the trigger is less efficient due to the timing shift. However, this plot does not allow us to conclude on the higher loss of trigger efficiency in this region, as the loss during energy reconstruction is similar to that in the other detector region (about $\approx 2\%$). This very preliminary study allowed to get an idea of the amplitude of the effect and the need to use the lengthy phase determination calibration to readjust the proper timing.

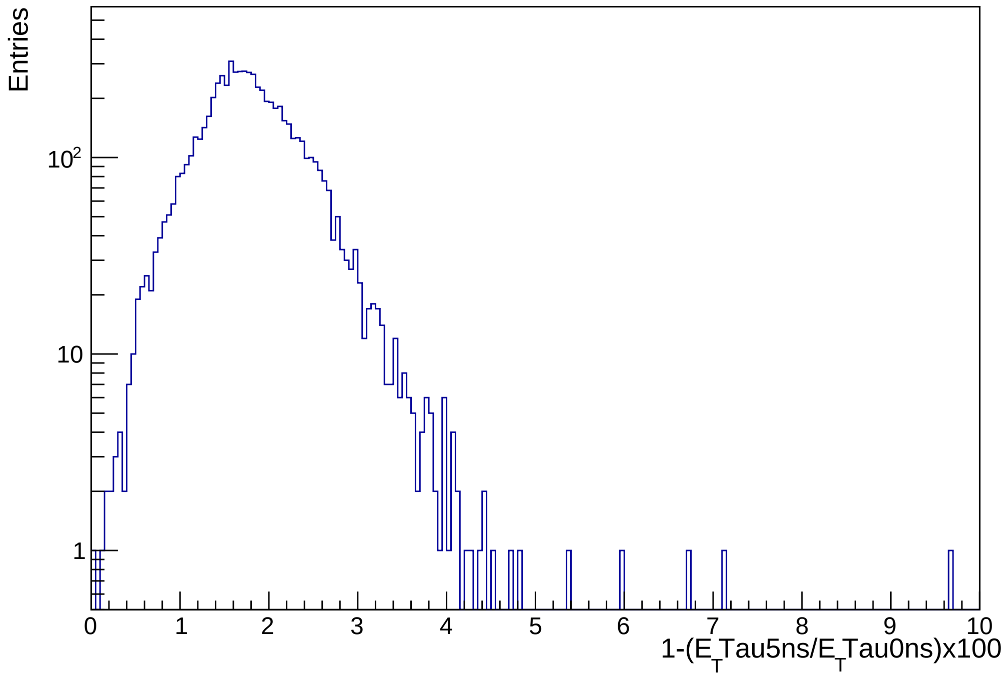
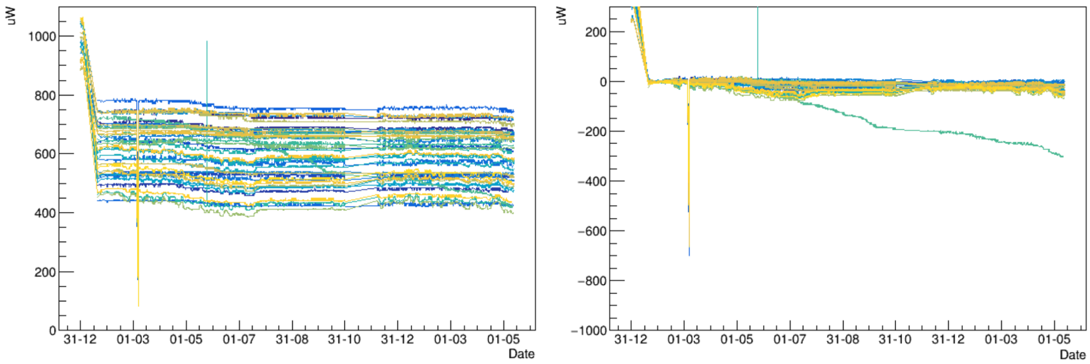


Figure 3.27: Distribution of lost energy ratio for all Super Cells in the region $1.54 < |\eta| =< 2.0$.

3.3 LTDB light power stability

As explained in Section 2.2.2.3, LTDBs have two paths for optical connections. The slow control path with the control fibers configures and monitors the LTDB and the data path with data fibers sends the information of the ADC samples to the LATOME for the energy reconstruction.

A database was set up to monitor and record the light power on all LTDBs fibers (control and data fibers). Through this database, plots were made to see the evolution of the light power for each channel of the Digital Trigger. Two types of plots are produced: the first one shown in Figure 3.28a is the absolute light power value as a function of the time and the second shown in Figure 3.28b is the light power value minus its starting value from the beginning of the data taking in 2022 to observe the relative evolution as a function of the time. On both plots, all fibers of one LTDB, up to 40 fibers depending on the flavor of the LTDB, are represented minus the fibers with unused channels. On these plots, the visualization of a trend of degradation and the identification of which fiber will have an issue with light power is easily spotted.

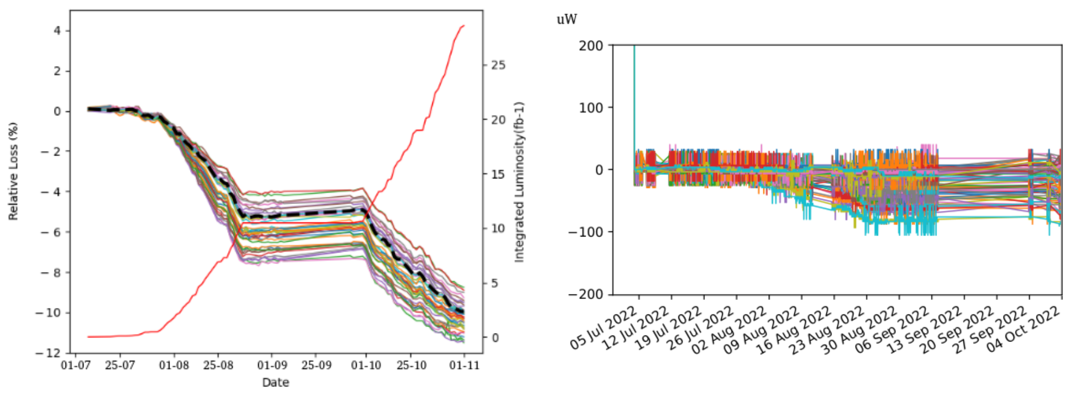


(a) (b)

Figure 3.28: Monitoring of the light power in μW as a function of the time in month-day format. One color per fiber, and one LTDB can contain up to 40 fibers. Figure (a) shows the absolute light power value and Figure (b) shows the relative light power value.

3.3.1 Radiation effect observed

Thanks to the monitoring of the light power of the data and control fibers, it was identified that since the beginning of data-taking in 2022, most fibers show a 10% reduction of the light power for all barrel LTDBs, affecting both data fibers (figure 3.29a) and control fibers (figure 3.29b). The control fibers are grouped by FELIX LTDB machine, with control fibers for barrel LTDBs and control fibers for end cap LTDBs. This is why we can observe stable fibers with no loss of optical power: these are the control fibers for the endcap LTDBs, and fibers that are impacted in the same way as the barrel data fibers: these are the control fibers for the barrel LTDBs.



(a) (b)

Figure 3.29: Light power loss as a function of the time over the 2022 data taking period. Figure (a) shows the average per fiber of the same position over all Barrel and Figure (b) shows all control fibers (Barrel and endcap) of one FELIX LTDB machine.

Figure 3.29a also shows the evolution of the light power and the integrated luminosity of the LHC in function of the time. The relative loss illustrated on this Figure is the mean over all the data fibers at the same position in η. This reduction is for now less pronounced in the End-Cap LTDBs as it will be explained in Section 3.3.1.3. The plateau observed in the Figure 3.29a corresponds to a large downtime of the LHC which started in August. During this period, the light output power increased slightly due to an annealing effect compatible with a small recovery from radiation damage. Upon investigation, it was determined that the time profile of this loss is well-correlated with the time profile of the LHC luminosity. The reduction in light power is potentially attributed to a radiation effect, also as evidenced by its more pronounced impact on the Barrel LTDBs compared to the End-cap LTDBs due to the localization on the detector.

As illustrated in the simplified diagram in Figure 3.30, the problem, being potentially correlated with radiation, does not involve any hardware on the back end electronics. Possible sources of the issue include the fiber harnesses within the LTDBs, the optical transceiver components (MTx, MTRx), or the fiber cables connecting the front end electronics to the back end electronics. When studying the effects of radiation on fiber harnesses, connectors and fibers, it is essential to examine how these components react under such conditions.

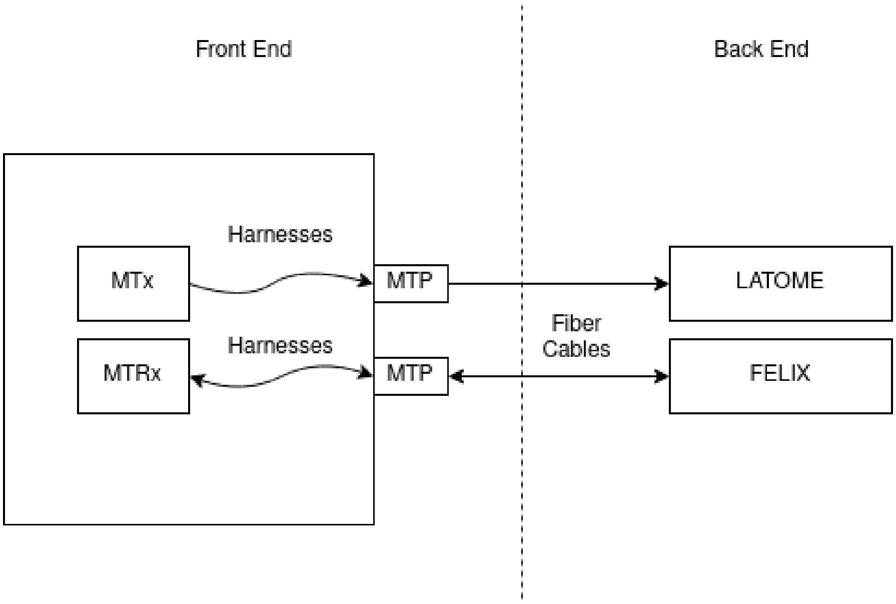


Figure 3.30: Simplified hardware diagram of the optical connection between the LTDB on the detector and the FELIX and the LATOME off the detector.

3.3.1.1 Fibers composition test

As part of the testing conducted on the fiber harnesses, an examination was performed to detect the presence of Phosphor in the fibers. It is well-established that at low doses of radiation, the fiber may turn dark if it contains Phosphor, causing the optical fiber to lose its transparency and resulting in a transmission loss. This phenomenon was previously observed by the muon detector in 2010. In that instance, for a specific batch of fibers, some fiber cables had to be replaced in the ATLAS detector. The existence of Phosphor can be confirmed through Energy-Dispersive X-ray spectroscopy (EDS).

Following the discovery of this optical loss on the LAr system, an EDS test was conducted at CERN on four samples. These samples included fiber harnesses used inside the LTDB, fibers from the Phase-I Barrel cable production (utilized between LTDB and LATOME), fibers manufactured by DRAKA, and fibers made in China—both of which could have been used in the production of LTDB fiber harnesses. Remarkably, the EDS analysis did not reveal any traces of Phosphor in any of the four different samples ruling out this hypothesis.

3.3.1.2 Fibers irradiation test

Another test was conducted on the optical harnesses in the LTDB to study their behavior under radiation. For this purpose, a setup was devised, splicing together ten harness fibers and attaching optical cables at the end of each. Subsequently, a parasitic irradiation was performed using cobalt-60. The radiation exposure ranged from

0.1 Gy to 1 kGy, which is anticipated to represent the radiation levels expected at the position of the harnesses after the High-Luminosity Large Hadron Collider (HL-LHC). The results of this test are depicted in Figure 3.31. For extended exposure, the harness fiber exhibited a loss of 0.1 dB at the end of the HL-LHC, and at the current dose of approximately 3 Gy, the radiation did not manifest any discernible impact on data transmission.

Additionally, the fiber cable connecting the LTDB and the LATOME underwent testing with Co-60. A 60-meter drum was irradiated while connected to an optical power meter to monitor the degradation of light power. Positioned at a distance of 3 meters from the Co-60 source, the drum was exposed for approximately 48 hours. The values observed on the power meter, detailed in Table 3.2, remained unchanged.

MTP12 channel	Light before (dBm)	Light after (dBm)
Channel 1	-7.22	-7.22
Channel 2	-8.93	-9.15
Channel 3	-7.39	-7.63
Channel 4	-10.77	-10.52
Channel 5	-9.09	-9.28
Channel 6	-6.93	-7.51
Channel 7	-10.17	-10.29
Channel 8	-11.20	-10.85
Channel 9	-7.33	-6.90
Channel 10	-10.97	-10.92
Channel 11	-10.00	-9.88
Channel 12	-11.85	-11.82

Table 3.2: Value observed on the power-meter for a 60 meter optical fiber between an LTDB and a LATOME before and after a 48 hour exposure at 3 meter distance to a Cobalt-60 radiation source.

The findings from these tests led to the conclusion that fiber optics were not the source of the observed 10% degradation attributed to radiation induced by the LHC's luminosity.

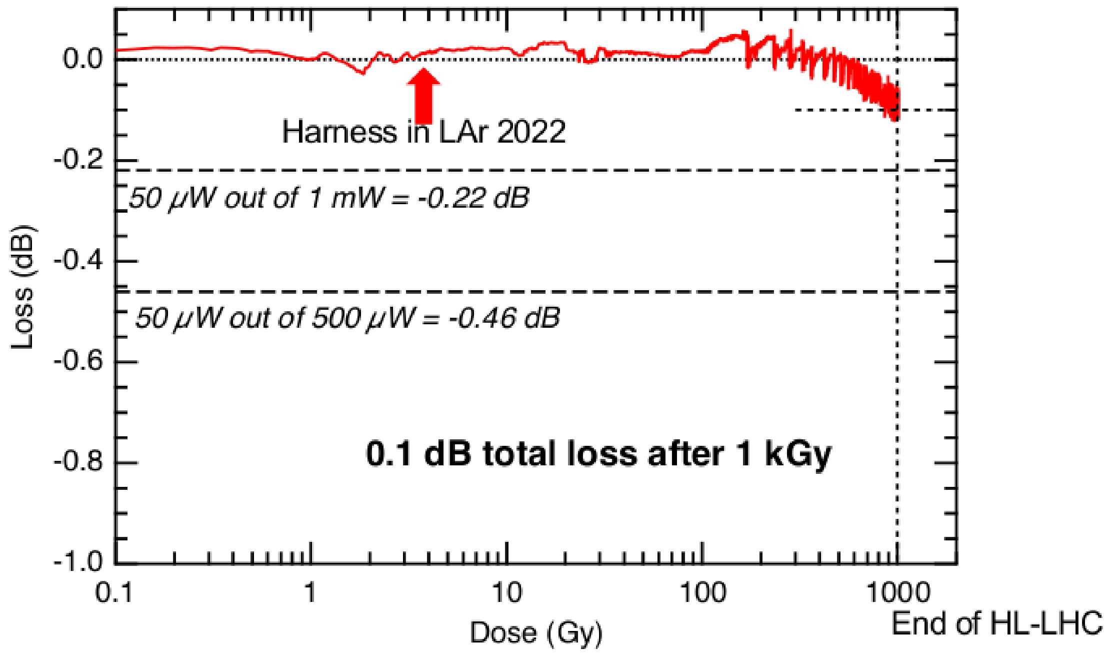


Figure 3.31: Optical power loss in dB as a function of the amount of radiation emitted from a Cobalt-60 source on the LTDB fiber harnesses.

3.3.1.3 Optical transceiver test

The second component that could be the cause of this degradation is the optical transceivers, the Miniature optical Transmitter (MTx) for the data fibers and the MTRx for the control fibers. Since the degradation on the data fiber and on the control fiber are the same, only the study on the MTx will be described here. It was already observed that the barrel LTDBs are more impacted by radiation than the endcap LTDBs due to their proximity to the interaction point. Even variations are observable inside a single LTDB, given that the four MTx components do not share the same radial position and consequently exhibit differing degrees of light power degradation, see Figure 3.32.

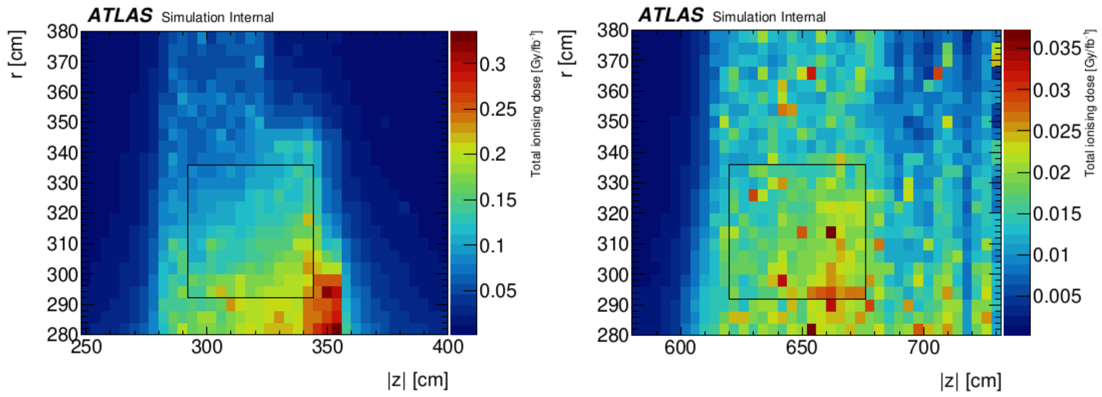


Figure 3.32: Simulation of the Total Ionizing Dose (TID) field for barrel and end cap area crate regions. Barrel locations are 10 times more impacted by the radiation due to their position. The superimposed black box represents the LTDB's location. Figure (a) shows radiation effects on a barrel LTDB and Figure (b) radiation effects on an end cap LTDB.

To confirm that the position of the component inside the LTDB does not have the same radiation effect on the fibers, simulations were carried out as a function of position on the detector. Figure 3.33 shows a picture of the LTDB with its PCB in the red box and the MTx components on both sides of the PCB in the green boxes. The yellow numbers are the fiber number associated with the MTxs. This picture was overlaid in 3.32 with the ATLAS coordinates to be able to properly reproduce the radiation effect in simulation.

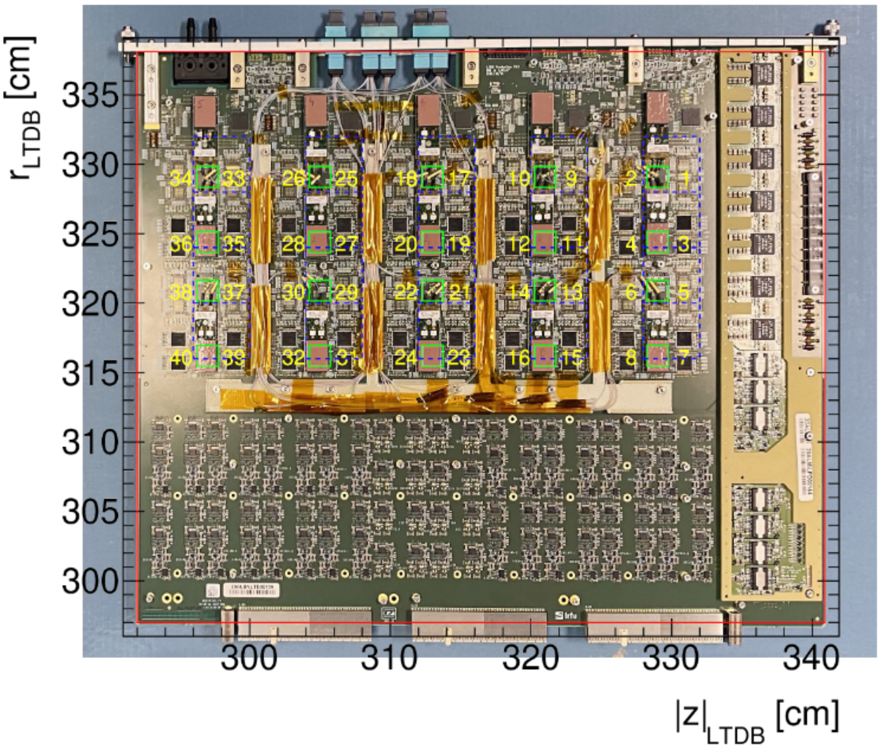


Figure 3.33: Barrel LTDB overlaid with ATLAS coordinates.

The mean of loss for all barrel fibers with the same MTx position was measured for the MTx on the barrel detector and computed for the simulation of the radiation dose with these coordinates. Figure 3.34 show the comparison. The black dots corresponds to the value measured on the MTx of the fiber number of the detector (yellow number on the Figure 3.33) and the green band it is the radiation simulation. Since the scaled simulation values almost match the effect observed on the detector, the pattern of power loss by fiber number and strong correlation with TID at MTx positions points to a TID-weak MTx component as the root cause.

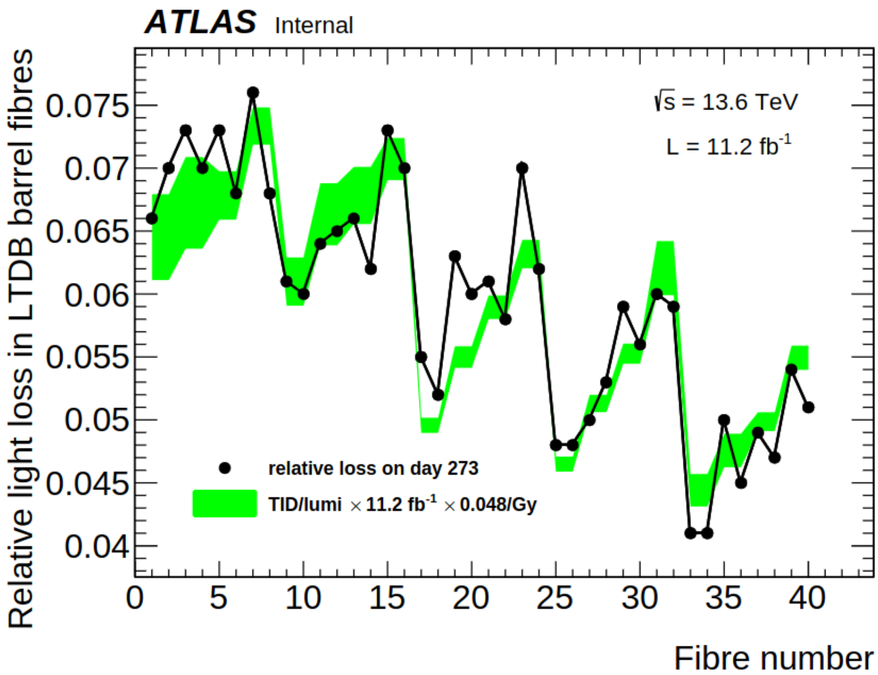
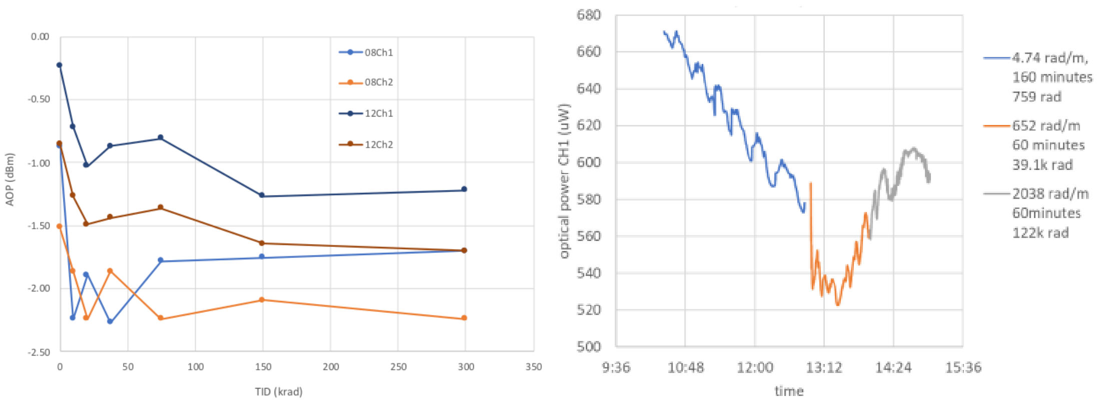


Figure 3.34: Relative light loss in the barrel on day 273 (30 Sep 2022 date is prior to saturation effects becoming visible) as a function of fiber number. Black markers show the average loss over all Barrel LTDBs while the green band shows predicted TID/lumi at the location of the MTx scaled with 11.2 $\text{fb}^{-1} \times 0.048Gy^{-1}$.

In fact, looking at the MTx production test under X-Ray in 2017, the same effect was observed. A loss of 1.5dB was observed and after a TID around 0.3-0.4Gy the loss started to stabilize. Additionally, some Irradiation tests were conducted on spare modules. This test confirms the phenomena observed during the production of the MTx, a loss of light until 0.4Gy, when the light power starts to stabilize. Figure 3.35a shows the production irradiation test in 2017. The irradiation test made on the spare module in 2022 is shown in this Figure 3.35b.



(a) (b)

Figure 3.35: Evolution of the optical power as a function of the amount of radiation received by the MTx module. Figure (a) shows results of a test performed in 2017 and Figure (b) shows results of a test performed in 2022.

The explanation for this loss of light was found in one of the transistors inside the LOC laser driver. The current mirror $I_t = 1.25/R3$ with R3 an external resistor insensitive to the radiation. The biasing current is mirrored by $M7/M8$ with a ratio of 10. Since M7 is much smaller it is more sensitive to the TID. The V_{th} variation in M7 and M8 are not the same and that will cause a change of the mirror ratio, which will lead to I_{bias} variation and will have an impact on the light power at the end. The V_{th} for an n-channel metal-oxide-semiconductor (nMOS) transistor was observed to change before 0.3-0.4Gy and then stabilize. This is exactly the same behavior observed during the irradiation test of the MTx.

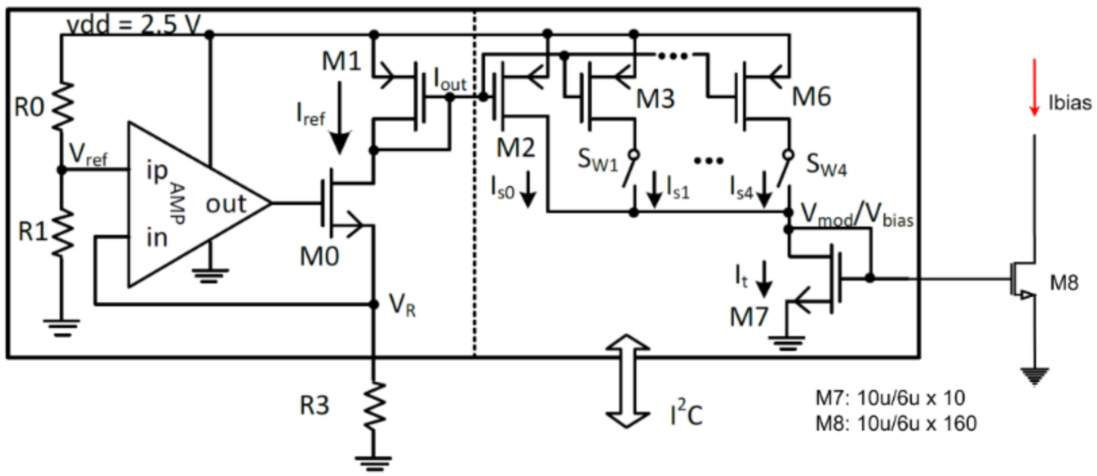
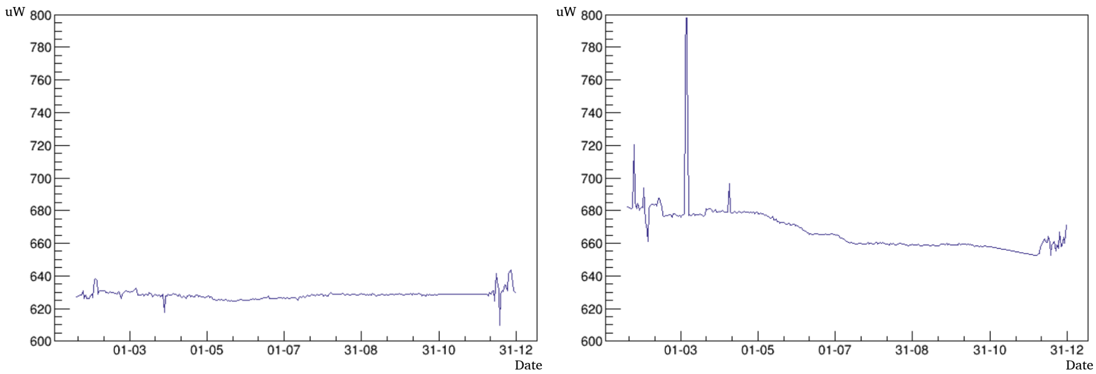


Figure 3.36: Custom-design of the LOC laser driver inside the MTx optical transmitter.

The annealing effect has started to stabilize the loss during the LHC stop as seen in Figure 3.29 and confirms our study. After approximately one year of data taking the

Barrel fibers are stable (see Figure 3.37a) and this effect starts to be observed on the LTDBs fibers of the End Cap (see Figure 3.37b). The status is now that all the LTDBs are stabilized except a few of them that have been replaced due to different issues and since they were not on the detector before they will have the same behavior until the stabilization after a few months of data taking.



(a) (b)

Figure 3.37: Mean of the optical power for the fiber number 1 of all the LTDBs during 2023 data taking. Figure (a) shows all Barrel fibers number 1 and Figure (b) shows all End Cap fibers number 1.

3.3.1.4 Monitoring put in place

This issue was closely monitored due to its critical nature. Since the cause is now identified and understood, no further action is needed. Furthermore, the monitoring of the light power for the control and the data links of the LTDBs has been improved. Now several types of alarms on the light power are in place to alert that a link is losing its optical power below the minimum to send proper data. The history of every fiber link power was put in place in DCS (see Figure 3.38) to quickly see which link loses too much light. Other information was added like different mapping conventions (for example fiber LTDB number, fiber LATOME number) to be clearer for the non-experience d users.

Figure 3.38: DCS panel for monitoring the light power of data fibers.

3.4 Error on the LTDB data fibers

Errors in the data link behavior were found during the operation of the system. This Section lists them with the objective of understanding and anticipating the data fiber faults and integrating alarms to promptly signal abnormal errors. A monitoring was developed to identify pattern errors observed in the data fiber during data taking.

The monitoring put in place is illustrated in Figure 3.39, with the offline script developed to extract certain information like the rates of the different counters, spot abnormal error rates on fibers, spot mis-configurations of LTDBs, dead fibers, raise a red flag depending on the severity of the error to be able to have a quick action taken during a run. Offline scripts were developed to extract patterns of errors over several runs and determine the cause of these patterns.

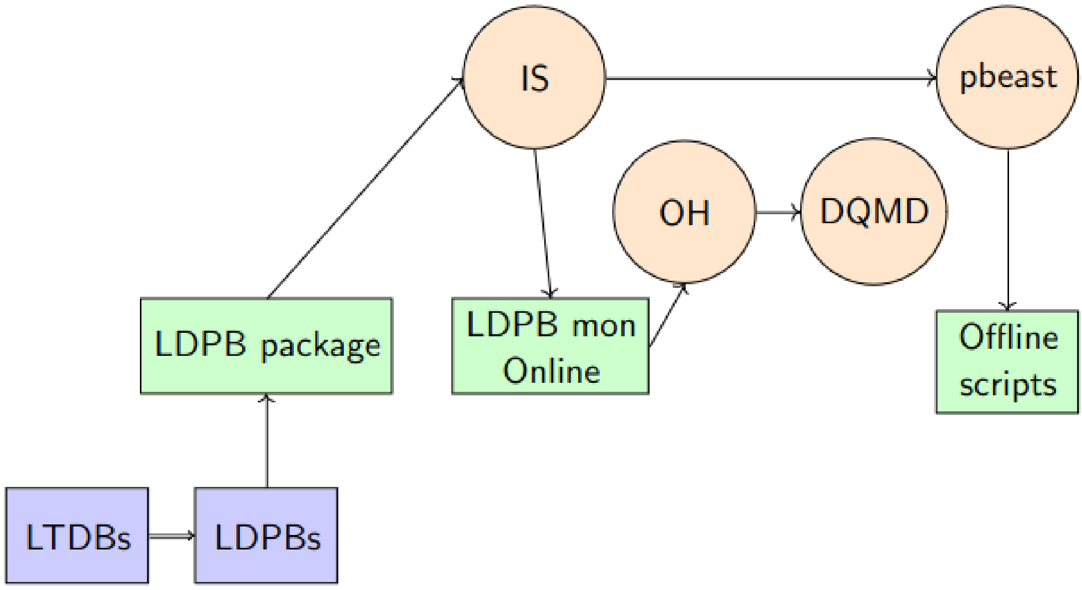


Figure 3.39: Architecture of the monitoring for errors on data fibers.

Table 3.3 lists all the error counters on the LATOME decoding stage.

Error counter name	Description
CRC	CRC check is in error
Channel ready error	The fiber decoding is unlocked a full resynch is needed
Bitslip error	A bitslip occurred
Channel PRBS error	The received PRBS is unexpected
Miss PRBS overflow	BCR not found in PRBS

Table 3.3: Description of the different error counters on the LATOME decoding stage.

Three sources of issues have been found that cause this instability of the data fibers and faulty data transmission:

Radiation Effects: Single Event Upset (SEU): applies radiation, SEU occurring with all error types. Notably, SEUs are more prevalent in barrel fibers, attributed to their higher radiation level due to their location. These effects are uncorrectable and not problematic due to their rareness.

Bad ClkDes Scan: Due to a bad delay applied between the clock as explained in Section 3.5 all types of errors will appear on the pair of fiber attached to this wrong delay. To solve this issue a new calibration needs to be run for this LTDB. Due to the criticality of data integrity and system stability, the improvement of the ClkDes scan calibration explained in the next Section 3.5 completely resolves this issue.

Component Issues:

- LOCx2 malfunctions induce only CRC errors. It was observed that the number of CRC errors is increasing as a function of time in a few fibers, serving as precursors to component failures. An exchange of the LTDB will be needed at some point to solve this issue.

- Optical emitter issue, like for a bad ClkDes scan, all types of errors appear on the data fiber. Since the ClkDes pattern was solved (see Section 3.5.2) it was possible to link this pattern to the anomalies in light power. Depending on the amount of light power the transmission error will be different. It will be also a clear indication that an exchange will be needed for this LTDB.

Monitoring this information will prevent failures, facilitating real-time monitoring and notification of abnormal errors in the LTDB system. Upon detection of anomalies like SEUs, CRC errors, or irregular light transmission, it will be possible to anticipate a failure and thus be able to take action to solve the problem, or to mask this fiber to avoid compromising the quality of the data.

3.5 Phase selection for data transmission

In order to ensure a proper encoding of the LOCic frame, the phase alignment between the edges of the ADC clocks data transmission and the internal clock of the LOCic encoder must be adjusted. The GBTx provides the 40MHz signal to the ADC and the LOCx2. The internal clock of the LOCic encoder operates at 320MHz, derived from this 40MHz. Each GBTx clock serves one LOCic encoder, with each encoder block receiving two ADC clocks at 320 MHz (see Figure 2.18). This work on the phase should be done only once after the power up of the FE crate. Because the PLL between two LOCic encoders does not have a retroactive loop, it needed to be locked at the beginning to work properly. To shift the phase between these clocks, a delay can be introduced. Two possibilities exist to modify the phase between the two clock signals:

- Add a delay to the clock signal coming from the ADC at the input of the LOCic.

- Add a delay to the clock signal from the GBTx at its output.

Two calibration methods were developed to adjust this phase selection, which will be explained in the following paragraphs.

3.5.1 LOCx2 scan calibration

The calibration, called LOCx2 scan, applies a delay to the input clock to the ADCs. This delay is individually selected for each ADC input. The calibration process scans all possible delay values and checks the error rate on the corresponding LATOME LOCic decoder register. Delay values range from 9 to 25 (indicated on the horizontal axis of

Figure 3.40) with a step size of 220 ps. For each delay, the error rate is checked for 5 seconds, and this process is repeated for all 40 fibers of the LTDB (indicated on the vertical axis of Figure 3.40). The results of the LOCx2 scan are shown in Figure 3.40. Values represented as "0" are displayed in red, indicating that errors rate different from zero were observed on the LATOME during the 5 seconds check. Those represented as "1" in green indicate that no errors were observed on the LATOME during the 5 seconds check. Once all delays for the 40 links have been scanned, an algorithm selects for each link the delay located in the center of the largest continuous range of delay values without errors. These selected values are saved and used for the data taking.

9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	Optimal_DLY	ltdb ▲
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	20	1
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	20	2
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	20	3
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	20	4
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	20	5
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	20	6
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	21	7
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	21	8
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	20	9
0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	20	10
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	11
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	20	12
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	19	13
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	19	14
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	20	15
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	20	16
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	19	17
0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	18	18
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	20	19
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	20	20
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	20	21
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	20	22
0	0	0	0	0	0	1	1	0	1	1	1	1	1	1	1	1	22	23
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	20	24
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	20	25
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	20	26
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	19	27
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	19	28
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	20	29
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	30
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	20	31
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	20	32
0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	21	33
0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	21	34
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	20	35
0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	19	36
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	20	37
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	20	38
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	19	39
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	20	40

Figure 3.40: Results of the LOCx2 scan calibration for one LTDB. Fibers in grey are the ones unused (disabled by the mapping). Optimal_DLY column corresponds to the delay selected by the algorithm.

This method was developed because originally the I2C bus of the LTDB was not operational so it was impossible to make a calibration around the GBTx since one can only control it via I2C. The disadvantage of the LOCx2 scan algorithm is that it cannot detect low-rate errors without significantly increasing the scan time. A better method would be to find the worst delay and choose a delay that is as far away as possible from this bad delay. The worst delay corresponds to the delay with the highest number of errors. As you move away from this peak, the error rate decreases. This delay cannot be found by the LOCx2 scan, as it cannot scan the entire 3125 ps period of the LOCic internal clock due to its step size.

3.5.2 ClkDes scan calibration

The method adopted for the operations is called ClkDes scan calibration. This method applies a delay to the 40MHz input clock of the LOCx2 coming from the GBTx. The calibration scans all the delays to identify the worst delay value, which corresponds to the delay with the highest error rate observed on the LATOME. It then selects the delay farthest from this worst delay value. 64 steps of ≈48.8ps will be used to scan the entire period. Similar to the previous calibration method, all delays are scanned, and the error rate is checked for each corresponding LATOME fiber. Figure 3.41 illustrates one result of one calibration. In green "1" indicates delays with no errors, while in red "0" represents delays with errors. As the entire clock range is scanned, the delay with the highest error rate is identified, indicating that both clocks at the input of the encoder are in phase causing an error on the corresponding LATOME fiber. For this calibration, delays are selected in pairs of links that use the same GBTx clock and the same LOCx2. The algorithm chooses the delay situated in the middle of the two blocks of errors observed on the pair of links.

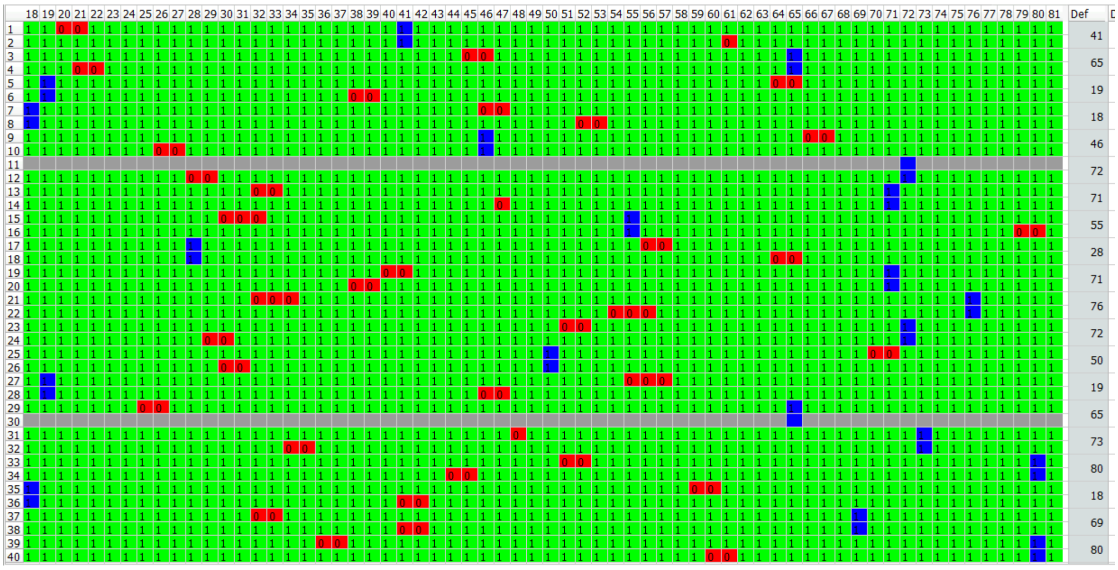


Figure 3.41: Results of the ClkDes scan calibration for one Barrel LTDB. The 40 links present on one LTDB are shown on the vertical axis and the 64 delays on the horizontal axis. Fibers in grey are the ones unused (disabled by the mapping). The blue boxes are the final delay selected by the algorithm.

This calibration method has demonstrated better stability over time on the detector and requires a reduced scan duration compared to the LOCx2 scan calibration. However, it still requires to be used at least at each front end crate (FEC) power-cycle. It has been observed during the 2022 run period that this calibration is needed more frequently for some channels, occurring approximately once per week across the entire detector. A solution for better stability was needed to avoid this during data taking.

Figure 3.42 shows the sum of nineteen scans for one LTDB during 2022 illustrating the evolution of the error rate over time. This study revealed three patterns:

- The normal pattern with only one area of a bad delay (green rectangle).
- The pattern with one area of a bad delay and a tail of bad delays from time to time (orange rectangle).
- The pattern with a lot of bad delays (red rectangle).

The presence of orange and red patterns explains the instability of the ClkDes scan calibration and the need for periodic re-calibration. To solve these instabilities, several parameters were adjusted, including the duration of error checking, the waiting time between delay changes on the LTDB and the moment of its start to check on LATOME the error rate, the reset of the GBTx, and the reset of the LATOME transceivers.

- The difference between instantaneously checking errors and performing a one second error check revealed that for the one second check, the error region was larger. The duration for error checking was tested up to 5 seconds. The analysis concluded that from 1 second to 5 seconds, the results of the ClkDes scan calibration were very similar, indicating that increasing the checking time up to 1 second was enough and saving a lot of time when it is needed to run these calibrations on all the detectors.

- The waiting time between the selected delay set on the LTDB and the time for the LATOME check to start. This waiting time was increased from 100ms to 500ms. It drastically reduces the instabilities of the third pattern (see red rectangle in Figure 3.42) making the result of the ClkDes scan calibration much more stable.

- Before initiating the ClkDes scan calibration, two resets were implemented: the reset of the LATOME transceivers and the reset of the GBTxs. The purpose of these resets is to put the GBTx in a good "state" to start scanning, and for LATOME transceivers, it's to lock in correctly and be ready for calibration. To reset the LATOME transceivers, the LTDBs were divided into three groups, ensuring that only one LTDB in each group was connected to one LATOME. This approach aimed to prevent multiple resets of the same transceiver and to corrupt scans of other LTDBs. Specifically, group 1 comprised all the left LTDBs of the Barrel crate, along with all the End Cap standard LTDBs, all the End Cap special 1 LTDBs, and all the FCal LTDBs. Group 2 consisted of all the right Barrel LTDBs and all the HEC LTDBs, while group 3 included all the End Cap special 0 LTDBs.

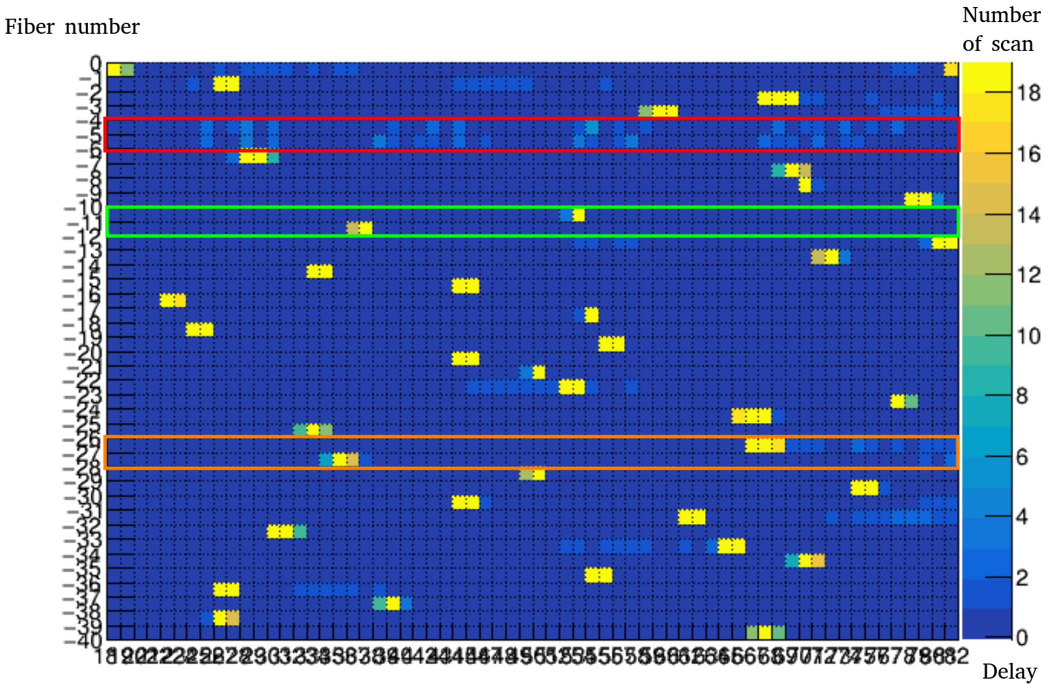


Figure 3.42: Accumulative plot of several ClkDes scan calibrations to observe the evolution of the error rate on the delay over time. Three patterns were observed: the green rectangle shows the expected behavior, a problematic pattern is shown in the orange rectangle and the worst-case scenario in the red rectangle.

Since the implementation of this new calibration along with the tuned parameters and resets, the phase selection for data transmission has become highly stable. This calibration is now executed only after a power-cycle on the corresponding LTDBs. During the last month of year 2 of Run 3, no fibers were found to have a faulty phase selection. It was unnecessary to redo any calibration except for testing or validation purposes.

3.6 Infant mortality of the MTx

Since the installation of all LTDBs on the detector it was observed that a few single MTx components stopped working. For others, it was observed through our monitoring that the light power was decreasing until the appearance of corruption of the data transmitted to the LATOMEs. The cause of this power loss affecting a few MTxs is not the radiation which affects all MTxs and stabilized at around 10% loss, but another effect.

Tests were made on a test bench to understand why some MTx components reduce their optical power. A study was made over 8 months on 64 MTx, where each MTx is connected to an optical spectrum analyzer to know the light power at a fixed point in time as a function of the wavelength. During this test we cycled through all of the MTx channels and took "pictures" of each one's spectrum. After 8 months it was found that of the 64 channels, only one channel was losing power. Figure 3.43 illustrates the degradation of the optical spectrum of this channel over time. All the channels should have a stable spectrum but on this channel, it turns out that the spectrum starts to shrink in width and height meaning that the channels are degrading. The reason for the reduction in optical power is attributed to the narrowing of the spectrum, caused by the migration of "dark line defects" (DLDs) into the active region of the VCSEL (Vertical Cavity Surface Emitting Laser). As the diameter of the VCSEL diminishes, the number and spacing of lateral optical modes decrease. DLDs, which are non-radiative defects, lead to a decrease in the VCSEL's aperture. Consulting experts it was understood that a manufacturing issue for single VCSEL is causing the DLDs to occur from time to time on some of the produced VCSELs. Most of the other produced VCSELs do not show this feature and can be used continuously.

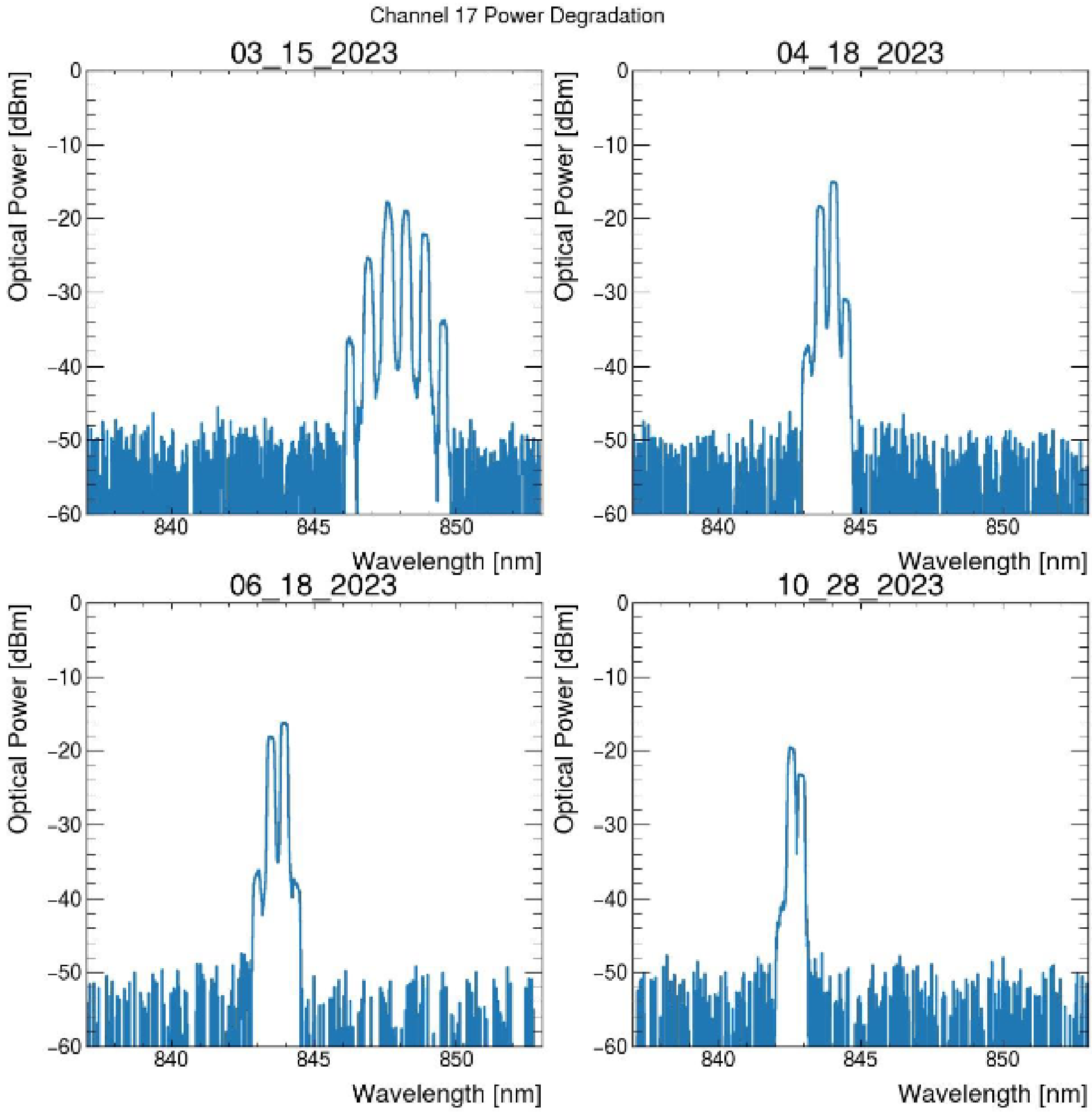


Figure 3.43: Optical power as a function of the wavelength at four times during the test period for one faulty channel of an MTx.

Knowing this, it is expected to have some failures on the MTx components. Replacement of these faulty components will be necessary to have all channels operational. During the 2022 end of year shutdown, we replaced 3 LTDBs due to faulty channels on an MTx. In the 2023 end of year shutdown, it was decided to replace all the MTx showing signs of degradation to avoid future failures, MTxs in 24 LTDBs were exchanged.

Conclusion

This thesis presents the work done after the installation of the Phase-I upgrade electronics on the ATLAS detector, in particular the work done around the LTDB. The LTDB is a crucial component in the ATLAS detector's front end system, consisting of ASIC components responsible for digitizing Super Cell pulses from the detector for the trigger readout system.

The pilot run of Run 3 in October 2021 provided a first validation of the working principle of the LTDB. In the subsequent period, the stability and the performance of the LTBDs were improved. At the end of each year, during the end of year shutdown period of the LHC, faulty pieces of hardware on the detector, including the LTDBs, were refurbished or replaced.

The aim was to reach the same or better performance with the digital trigger system as with the legacy trigger. For this, appropriate monitoring was developed, offering intuitive access to system status and configuration and to archived monitoring values. A big effort was needed in order to make all LTDB channels operational. 99.7% of channels have no issue and return the expected timing and energy. Some dynamic pedestal jumps are yet persisting but a mitigation on the LATOME firmware was put in place in order to prevent an impact on the trigger behaviour.

For the improvement of the fiber stability between the LTDB and the LATOME, a monitoring was put in place to be able to quickly react during data taking and resolve possible failures in-situ. The radiation effects observed on the light power of the control and data fibers have been understood and closely monitored, keeping track of abnormal degradation on some fibers. The LOCx2 scan has been replaced by a more stable and robust calibration procedure that only needs a rerunning after a power cycling.

The timing shift in the clock driving the LTDB ADC upon a power-cycle of a FE FELIX LTDB machine is not yet understood but clearly identified to be coming from the FELIX side. Work from FELIX side is still ongoing on preventing the clock shift in the first place. However, for the time being a mitigation measure adjusting the timing in the OFCs has been put in place.

The LTDB system was successfully validated and the performance improved since its initial deployment. As part of the digital trigger system it will stay operational for all of LHC Run 3 and beyond, providing digitized Super Cell signals to the trigger back end.

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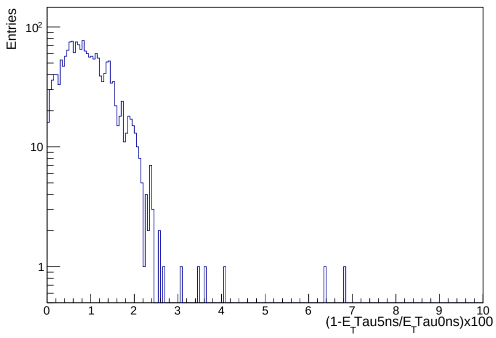
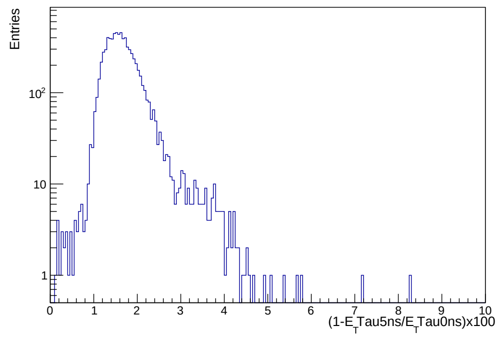
Annex A



(a) PreSampler layer



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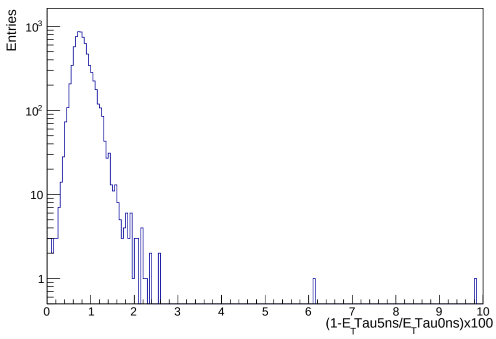
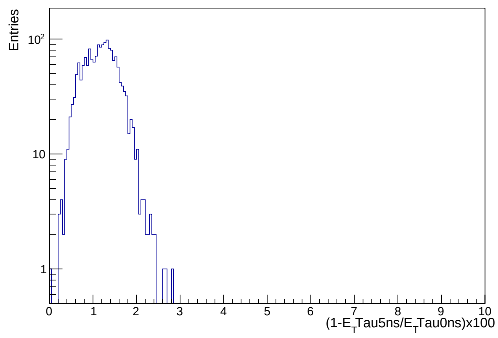
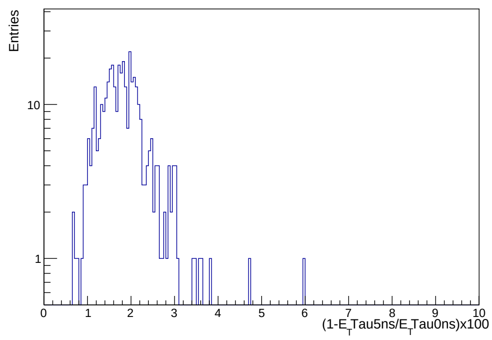


(c) Middle layer

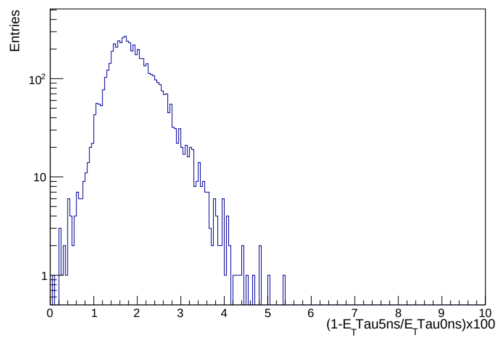


(d) Back layer

Figure A.1: Distribution of lost energy ratio for all Super Cells in the EMB layers.



(a) PreSampler layer



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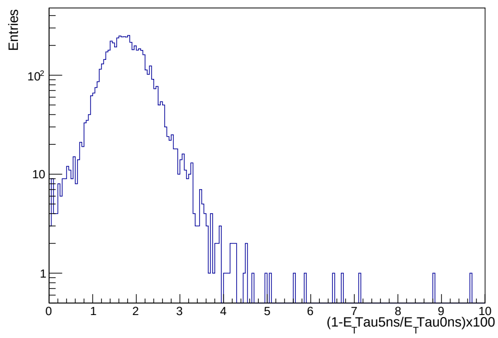

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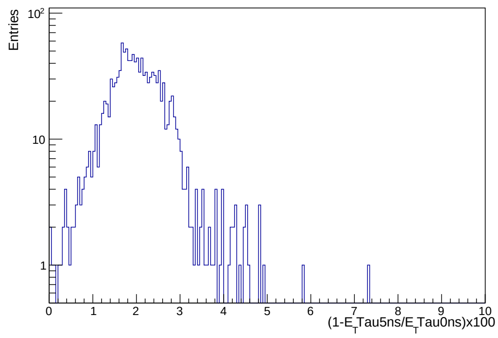

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Figure A.2: Distribution of lost energy ratio for all Super Cells in the EMEC layers.

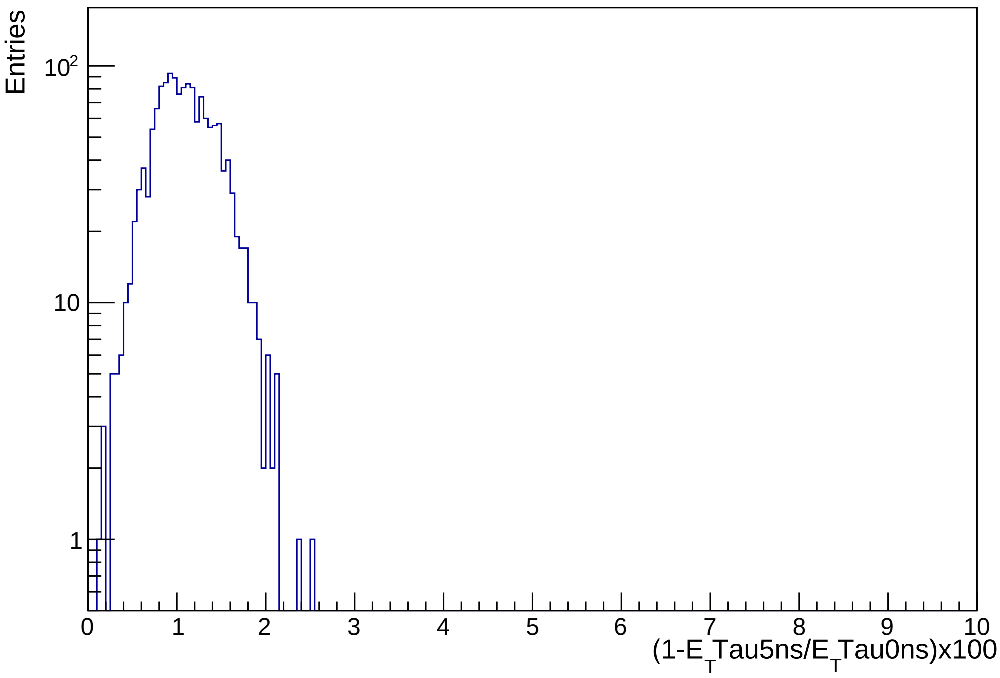
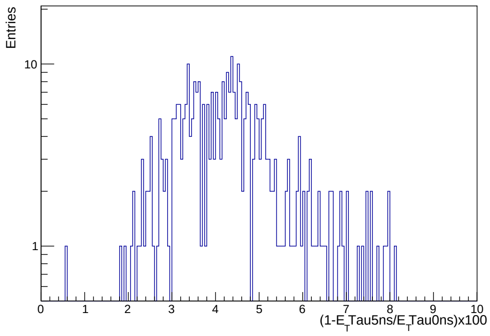
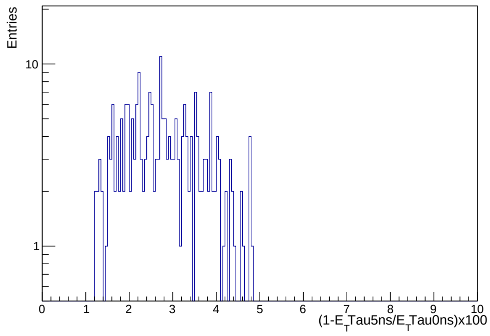


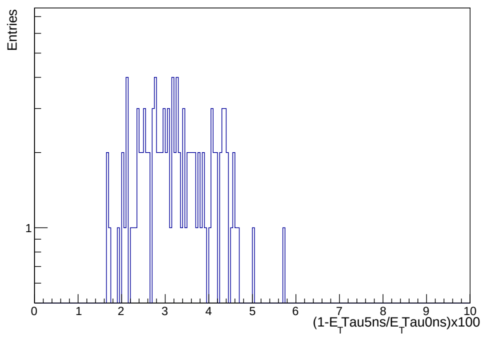
Figure A.3: Distribution of lost energy ratio for all SCs in HEC.



(a) Layer 1



(b) Layer 2



(c) Layer 3

Figure A.4: Distribution of lost energy ratio for all SCs in the FCAL layers.