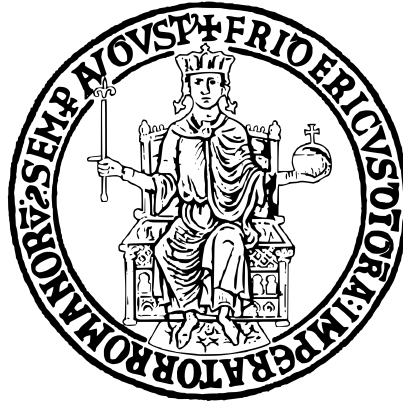


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“FEDERICO II”



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**Development of front-end electronics for Beam Profile
Monitor in IRRAD facility at CERN**

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ABSTRACT

The study of radiation and its effect is of utmost importance in various scientific fields, including particle physics. European Organization for Nuclear Research (CERN) has been at the forefront of advancing our understanding of the fundamental properties of particles and behaviour of particle beams. As part of this research field, IRRAD facility operates at CERN in order to conduct radiation studies to investigate the effects of radiations on different materials and electronic devices. This thesis focuses on the design and development of the front-end electronics which will be part of the beam monitoring system used at the IRRAD facility. The characteristics and functioning of the facility, as well as the operating principle of the beam monitoring sensors used in the experimental areas will be analyzed in order to obtain a series of requirements and specifications useful for the realization of the front-end electronics mentioned above. The aim of this thesis work is to provide a final product that can satisfy all the requirements and that can be easily operated by the facility personnel. In this regard, the whole development process is described in its entirety, including the design and testing parts, providing a general overview of the functionalities of the product and its performance.

ACKNOWLEDGMENT

The presented work was completed during my fascinating journey as a technical student at CERN. I stand here today, at the culmination of a challenging and arduous experience with a deep sense of gratitude and accomplishment. As I reflect on the arduous path that has led me to this moment, I am moved by the countless hours of hard work, unwavering determination and perseverance that have propelled me forward.

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INTRODUCTION

In the realm of cutting-edge scientific research, CERN stands as a beacon of innovation and discovery. The IRRAD facility, located in the east area of CERN, serves as a hub for radiation studies and experimentation. Its purpose lies in providing a controlled environment to investigate the behavior of particle beams and their interaction with materials. The first chapter provides an overview of CERN's accelerator complex, which includes a network of accelerators and experimental areas. Understanding the layout and functionality of this complex is essential to describe the context in which the IRRAD Facility operates. Then, the focus shifts to the IRRAD facility itself, exploring its location, purpose and structural aspects. A key aspect of the thesis is the examination of Beam Profile Monitors (BPMs). These devices are responsible for measuring the characteristics of particle beams. In more details, the BPMs are based on Secondary Electron Emission (SEE) phenomenon, which is explored as well as the hardware and system architecture of SEE-based BPM used at IRRAD facility. The second chapter focuses on the front-end electronics for the BPM. In particular some main requirements and key components will be analyzed. The third chapter describes the project choices and general structure in terms of wiring diagram, including some details of the board. Power supply circuit, clock generation circuit and other main parts will be described as well as the routing process on the PCB. In the final part, the testing process is described, documenting all results obtained. Overall, this work contributed to improve the knowledge in the field of radiation studies and enhance the accuracy and efficiency of the BPM devices in the facility, improving our understanding of the beam behavior and its implications in various scientific scenario.

IRRAD FACILITY AND BEAM PROFILE MONITOR AT CERN

At almost all particle accelerators, Beam Profile Monitors (BPMs) are the non-destructive diagnostics most frequently employed to assess the position and shape of a particle beam in real-time. The position and the shape of the beam are critical parameters that must be controlled precisely during experiments. BPMs deliver the centre of mass of the beam but also act as a monitor for the longitudinal bunch shape. In the first part of this chapter an overview will be done about CERN and its accelerator complex. A focus will follow on IRRAD facility and Proton Synchrotron (PS) accelerator. Finally, a description of the facility with their activities and a short discussion about the BPM devices will be done. This chapter aims to introduce the reader to the BPM technology, to understand why it is very important for the IRRAD facility and what led to the development of a new electronic system for data acquisition. [1]

1.1 Radiation damage studies at CERN

1.1.1 About CERN

The CERN accelerator complex is a sophisticated network of particle accelerators and detectors situated near Geneva, Switzerland. The accelerator complex consists in 7 main interconnected accelerators and beamlines. The basic functioning principle is to use every accelerator to "inject" protons in the next one, creating a chain which gradually produces a higher energy beam. The first stage is the Linear Accelerator 2 (LINAC 2), where protons are accelerated to energies up to 50 MeV. The protons are then sent in the Proton Synchrotron Booster (PSB) in which they are further accelerated to energies of up to 1.4 GeV. Next step to inject the protons is the Proton Synchrotron (PS), which accelerates them to energies up

to 25 GeV. The PS then feeds the protons into the Super Proton Synchrotron (SPS), which accelerates the protons to energies of up to 450 GeV and then injects them into the Large Hadron Collider (LHC).

The LHC is the most powerful and complex accelerator in the world, with a circumference of 27 kilometers and a maximum energy of 14 TeV. It is used to accelerate protons or ions to nearly the speed of light and allowing them to collide each other, producing a shower of particles that are detected by the various experiments located around the LHC ring. [2]

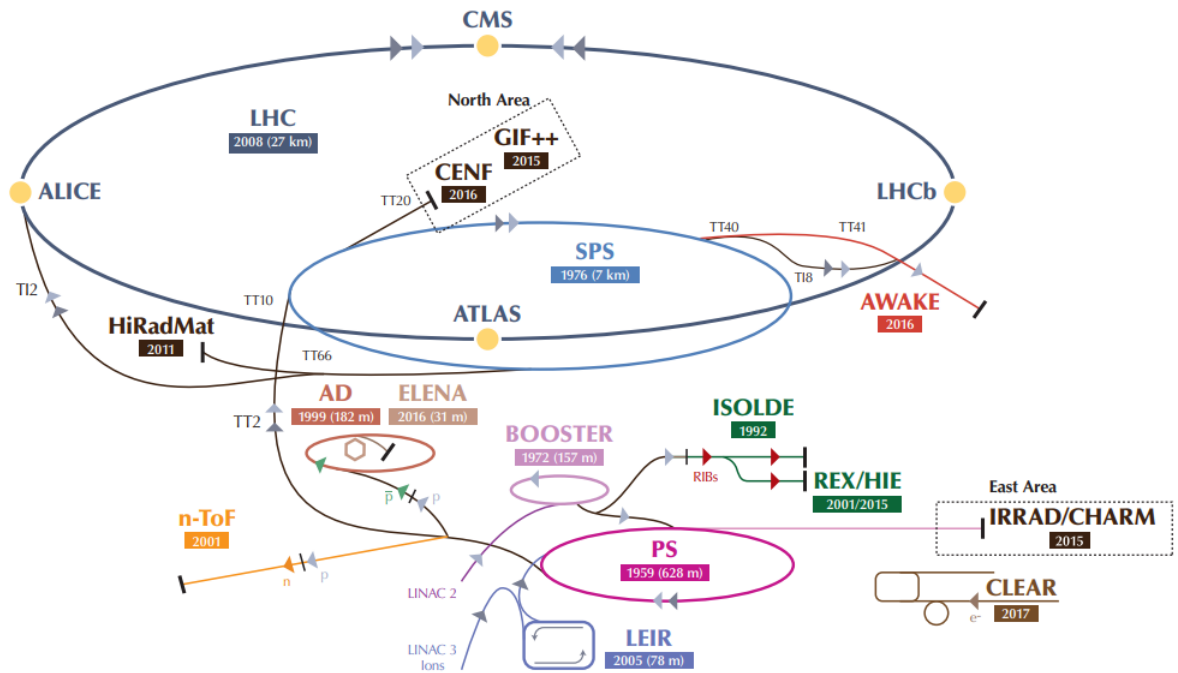


FIGURE 1.1: CERN accelerator complex

In this moment, they are 5 main different experiments running on the LHC:

- CMS
- ATLAS
- ALICE
- LHCb
- TOTEM

Each of them studies collisions between particles using different methods and technologies. Several other experiments are currently underway along the CERN accelerator



complex and it would be appropriate to say a few words about the sensational results obtained during these years. However, these topics will not be part of the elaborate in order to favor the equally interesting treatment of beam monitoring carried out by the IRRAD facility in the east area of CERN.

1.1.2 IRRAD Facility

High Energy Physics (HEP) experiments, as well as the advancements in space applications and in the nuclear energy [3] made it necessary to test and qualify the effects of radiations on particle detector prototypes, materials and electronics. To meet these needs, over the years several irradiation facilities have been set up in the CERN complex, infrastructures in which the components to be tested are exposed to very specific radiation fields. A good radiation tolerance allows detector materials, equipment and electronic systems to be installed and properly operate in HEP experiments such as the Large Hadron Collider (LHC) currently working in CERN. The irradiation facility that will be considered in this work is the IRRAD, built on the T8 beam-line of the east area of the Proton Synchrotron (PS) accelerator. At this facility, an high-energy proton beam with a momentum of 24 GeV/c variable size ranging from $5 \times 5 \text{ mm}^2$ to $20 \times 20 \text{ mm}^2$ is used to irradiate devices and materials. The proton beam is delivered in pulses (spills), with a width of 400ms and the minimum time interval between spills is 2.4s. Independently on the sample size [4], to be sure that the proper particle fluence is delivered to the samples with the required homogeneity, it's very important to control and align correctly the irradiation beam.

1.1.3 Location and structure of the facility

The CERN East-Area is located in the PS complex (Fig.1.2)[5]. The IRRAD facility has undergone several upgrades over the years starting from 1992 with IRRAD1. After the mixed-field irradiation facility (known as IRRAD2) was implemented behind the DIRAC experiment and operated since 1998. Based on previous studies carried out during the years 2007-2010, the need of improved irradiation facilities at CERN based on a slow extracted proton beam was confirmed and consolidated.

After the DIRAC experiment came to an end by the end of 2012, it has been dismantled during the Long Shutdown 1 (LS1) and the latest EA-IRRAD facility has been installed in the following years. The location of the current facility is more and less the same as the previously occupied by the DIRAC target and its upstream detectors, while the mixed-field facility (named CHARM) is constructed downstream of the proton facility. This has several advantages such as the possibility to have independent access to IRRAD, to optimize the

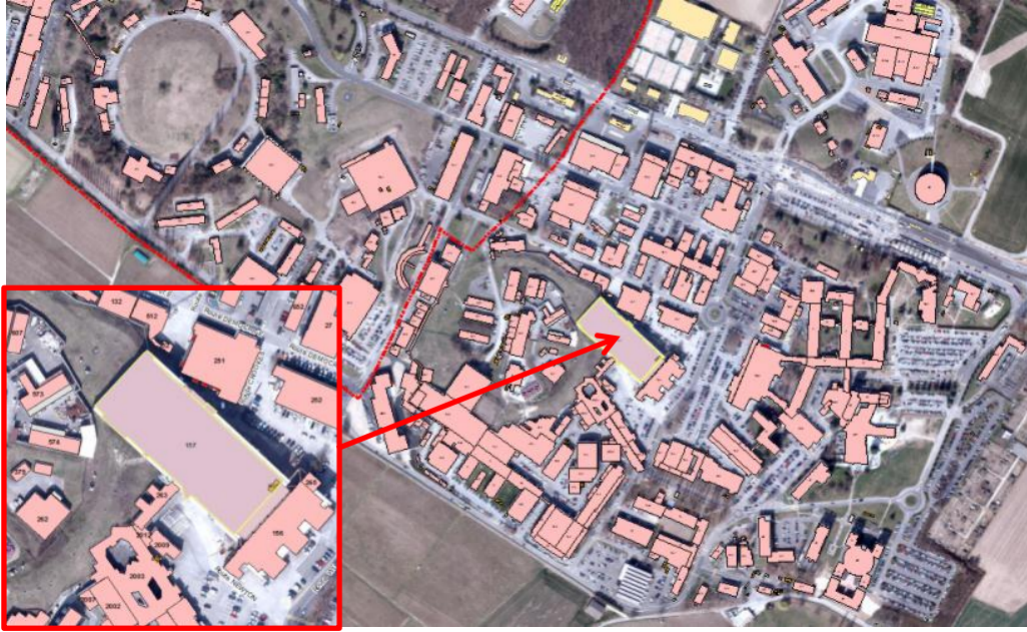


FIGURE 1.2: Geographic location of the PS East Area

facility layout in order to have appropriate solutions for the IRRAD experiments and finally to use the same beamline for both IRRAD and CHARM in the same time. The beam parameters taken for the design of the proton IRRAD facility are the following:

Parameter	Value
Beam Energy [GeV/c]	24
Number of particles per PS spill	$5 \cdot 10^{11}$
Number of spills per super-cycle	6
Typical super-cycle length [sec]	45.6
Number of days per year	200

TABLE 1.1: Beam parameters for IRRAD operation

The IRRAD facility is sub-divided in three zones (going from upstream to downstream) according to the nature of the samples to be irradiated. Each irradiation zone is separated from an 80cm-thick concrete wall (with a hole in order to allow the beam to pass through) whose function is to reduce the radiation background during irradiation and to minimize the ambient equivalent dose to the personnel during the access to the area. Each zone is equipped with remote controlled stages (e.g. the tables) where the IRRAD users can install their material samples (Fig.1.4). These tables can be remotely moved along the X-Y and θ axis and the irradiated samples can have variable sizes from some millimeters to several tens of centimeters. As previously mentioned, in order to study the effects of radiation on certain samples, it is of fundamental importance to know some characteristic parameters

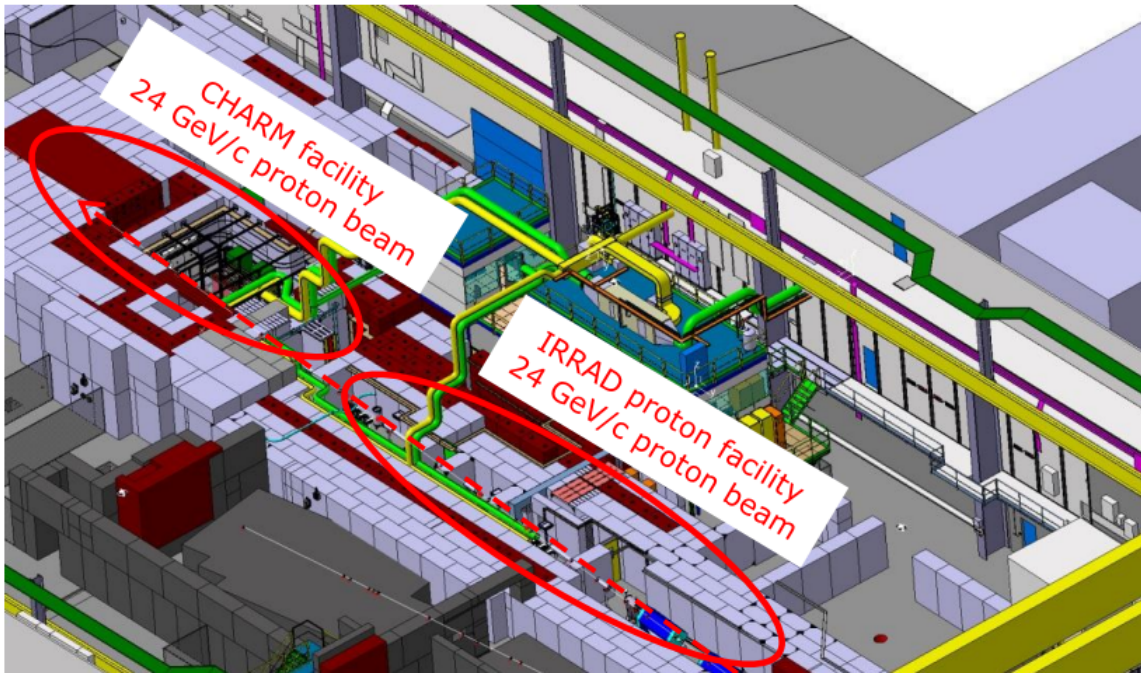


FIGURE 1.3: Layout of the latest EA-IRRAD facility combining IRRAD and CHARM

of the proton beam used, in particular we refer to its transversal and longitudinal profile. In order to achieve this goal a series of Beam Profile Monitor (BPM) is used.

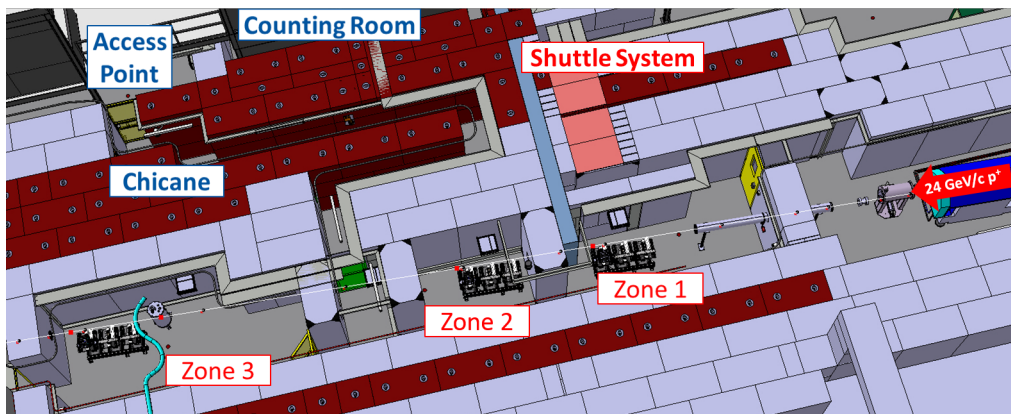


FIGURE 1.4: IRRAD facility irradiation area

1.2 Beam Profile Monitors (BPMs)

The naming *Beam Profile Monitor* indicates a non-destructive diagnostic system (that doesn't affect the beam) which allows the measurement of the position and profile of a particle beam in real-time[6]. Traditional BPMs rely on various techniques such as wire scan-

ners, ionization chambers, or beam position monitors. However this thesis works presents an overview on the secondary electrons emission (SEE) based BPM used in IRRAD and its principles of operation. The SEE-based BPMs offer high-resolution, non-invasive, and real-time monitoring capabilities, making them a promising alternative for beam diagnostics in accelerator facilities.

1.2.1 Beam Instrumentation in IRRAD facility

As discussed before, the IRRAD proton facility is located in the T8 extraction beam-line of the Proton Synchrotron (PS). Fig. 1.5 shows the location of the beam instrumentation devices that are installed in the T8 beam-line with the respect of the IRRAD and the CHARM facilities. There are four BPM detectors along the beam-line inside the facility, two secondary emission chambers (SEC), one ionisation chamber (XION) and a multi-wire proportional chamber (MWPC) downstream the CHARM facility. The XION and the SEC chambers are used to measure the intensity of the beam while the BPMs and the MWPC are used to monitor the beam profile. Further informations about XION, SEC and MWPC can be found in [7] since this work will focus on BPM technology used in the facility.

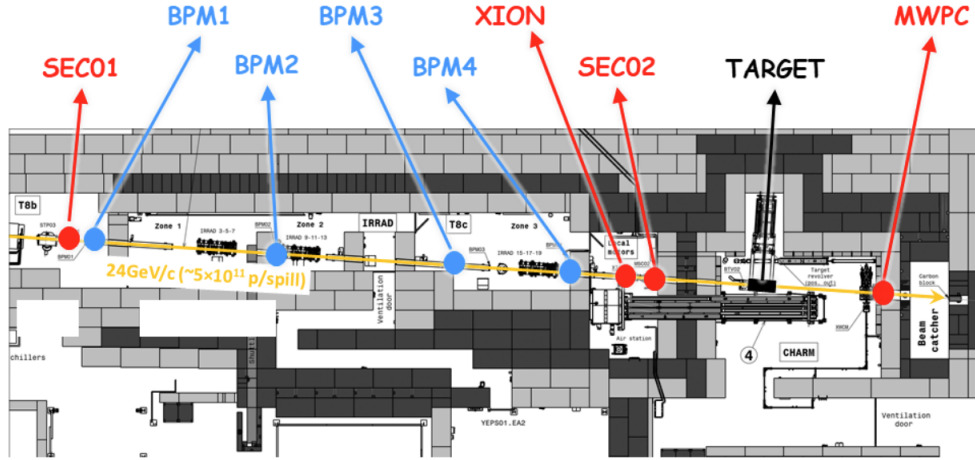


FIGURE 1.5: Beam diagnostics devices used in the T8 beam-line

1.2.2 Physics behind BPM detectors

Interaction of charged particles with matter

When charged particles (electron, protons, ions) traverse a medium, several different effects are produced such as x-rays, backscattered electrons, secondary electrons, auger electrons etc. The impact of the projectile particle makes it transfer a part of its energy to the

electrons of the medium, exciting them to an higher energy level. Generally, the energy loss¹ from the projectile particle is very small (less than 100eV) but still enough to generate heat in the material.

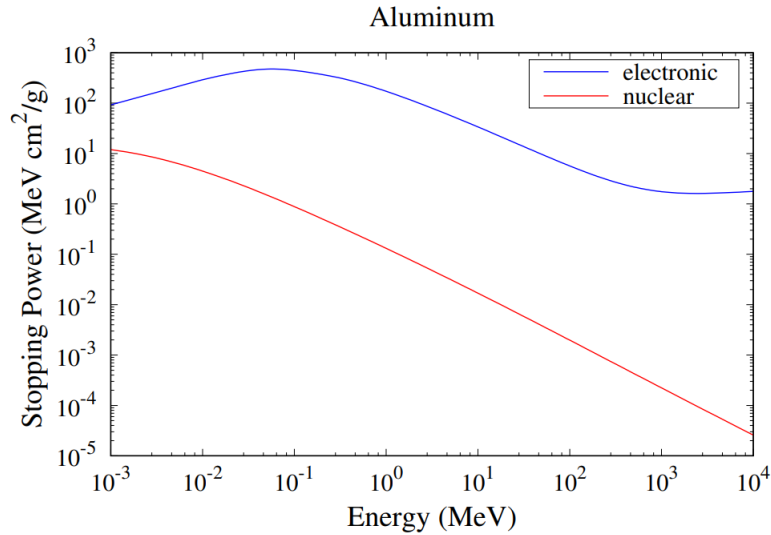


FIGURE 1.6: Stopping power of protons in aluminium as a function of their kinetic energy

Heavy particles at moderately relativistic energy are subject to Coulomb interaction with the atomic electrons and the nuclei. In this case, the Coulomb interaction causes deflection (scattering) of the projectile particle from its initial direction. The more is the projectile particle energy, the less is the deflection. The energy loss caused by Coulomb interaction is called nuclear energy loss and generally is much smaller than the electronic energy loss. The Fig.1.6 shows the difference between nuclear and electronic energy and focuses on the stopping power of protons according to their kinetic energy. The energy loss of charged particles can be due to different phenomena. For example, at higher energy (above few tens of MeV) this is caused by emission of radiation.

1.2.3 The Secondary Electron Emission (SEE) phenomenon

The electron emission mechanism can be induced by several physical processes depending on the source of kinetic energy supplied to the electrons. An example can be the Fowler-Nordheim tunneling effect, also known as Field Emission, when the emission of electrons from a sample surface into the vacuum is made under the action of a high electrostatic field. Another type of emission is the photoelectric emission, when the surface is irradiated with light in the visible or ultraviolet (UV) region. Many other phenomenon can cause electron

¹energy loss refers to the mean rate of energy loss per unit length or mass stopping power.

emission from solids, but the one this document is focussing on is the Secondary Electron Emission. There are different mechanism by which incident electrons with initial energy E_0 can lose their energy when interacting with a solid. The term "secondary electrons" refers to all the electrons emitted by the surface and collected by a positively biased collector. However, secondary electrons are not of a single type but a further differentiation is needed on the basis of the different interactions and the energy loss they undergo during the scattering process. According to this it is possible to distinguish between:

- True secondary electrons
- Elastically scattered secondary electrons
- Inelastically scattered secondary electrons

The true secondary electrons are defined as the electrons emitted by the sample having energy below 50 eV and are the result of a cascade process of electrons in the solid. During this process, electrons are created on the surface (or very close to it), reflecting the topography of the surface itself with good resolution and not giving any information about the inner structure of the material.

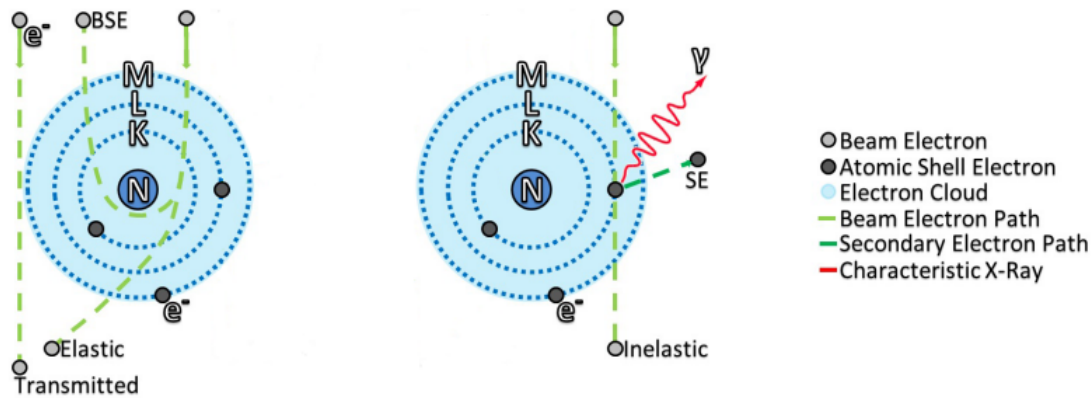


FIGURE 1.7: Interaction between an incident electron with the nucleus N and an electron cloud on the K, L and M shells.

Elastically and inelastically reflected electrons are defined as backscattered electrons (BSE), which have energy higher than 50 eV. When elastic interaction is present, it means that no energy is transferred from the scattered electron to the atom. In this case, an electron can be transmitted very close to the nucleus without interacting at all. When an electron penetrates into the electron cloud of an atom it is attracted by the positive potential of the nucleus by the Coulomb interaction and it is deflected towards the core. In rare case,

even complete backscattering can occur (BSE). In reverse, when collision between the incident electron and the atomic electron happens, there is an inelastic interaction, causing an energy transfer from the incident electron to the atomic one. In this case, the atomic electron will have sufficient kinetic energy to be knocked out by emitting a characteristic photon (γ). The ejected electron in that case is a secondary electron. The Fig.1.7 shows the different interaction processes of an incident electron with a nucleus N. The SEE process is generally summarized as a three-step process and it is defined below:

1. The target absorbs the incident particles and the inner electrons excite. Some of these excited electrons have enough energy to escape from the atoms. The highest energetic ones, or delta rays, can themselves produce secondary ionisation.
2. Through inelastic collision, the secondary electrons diffuse toward the target surface while losing energy. The depth at which the secondary electrons are produced affects their probability of reaching the surface
3. Some of the secondary electrons can go over the surface potential barrier.

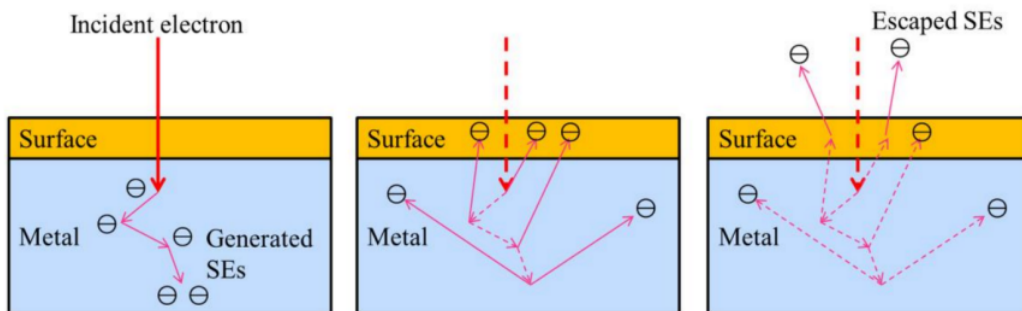


FIGURE 1.8: The three SEE steps from a sample



Secondary Electron Yield

The SEY is a measure of the number of secondary electrons emitted from a material's surface per incident primary particle or electron. It is an important parameter in various fields. The SEY measurement begins with an incident primary particle or electron beam that impinges on the surface of the material of interest. It is determined from the material's surface and normalizing it by the incident primary particle flux or intensity. The measurement is usually performed as a function of the primary particle energy or other relevant parameters. The SEY can depend on several factors, including the incident particle energy, angle of incidence, material properties, surface roughness, temperature, and surface cleanliness. It is important to control these parameters carefully to obtain accurate and reproducible SEY measurements.

The total SEY, including all electrons emitted by the sample, is defined as the ratio of the emission current to the primary electron current impinging on the sample

$$\delta = \frac{I_t(\text{emitted } e^-)}{I_0(\text{primary } e^-)} \quad (1.1)$$

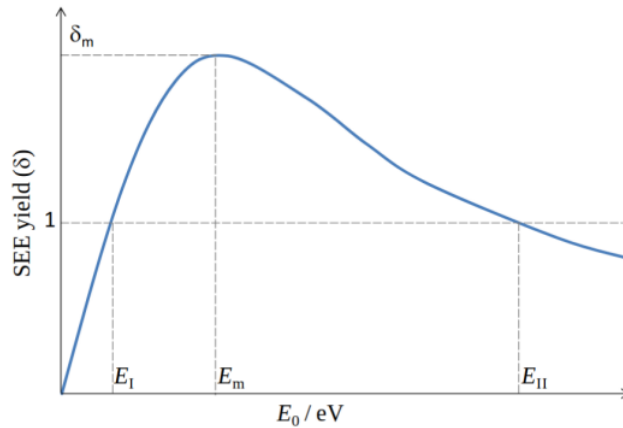


FIGURE 1.9: Variation of SEY as a function of the primary electron energy E_0

In Fig. 1.9 there is a representation of SEY as a function of the primary electron energy E_0 . The curve is bell-shaped and it is possible to individuate three main parameters:

- E_I and E_{II} which are two cross-over energies at which $\delta = 1$
- δ_m which is the maximum yield at an energy E_m .

From the shape of the curve it is possible to understand the relations between the penetration depth of the primary electrons and the escape depth of the secondary electrons. In



case the number of injected and emitted electrons is the same, the net current results to be zero, which means that $\delta = 1$ and this happens at E_I and E_{II} . E_I and E_{II} are not fixed values but they depend by the material, the angle of the incidence beam and the roughness of the surface.

- For $E < E_I$ the incident electrons (primaries) don't have enough energy to penetrate the surface and simply reflect back. An increase of the primary energy causes an increase of secondary electrons emitted.
- For $E_I < E < E_m$ an increase of δ is visible due to the fact that the penetration depth of the primary electrons is shorter than the escape depth of the secondaries. Again, an increase of the primary energy causes an increase of the depth at which secondary electrons are generated. At $E = E_m$ penetration and escape depth become the same.
- For $E > E_m$ the secondary electrons the depth at which secondary electrons are generated is so high that secondary electrons don't have enough energy to escape from the material. Just a little amount of them reaches the surface and overcomes the surface barrier.

SEE from metals and insulators

As said before, when a particle beam hits a medium, secondary electrons are excited and they become ready to escape from the material itself. Some problems related to the primary electrons energy and how this affects the capacity of secondary electrons to escape from the material has already been discussed above. In particular, the primary electrons energy value can affect proportionally the secondary electrons energies and depths of penetration. However, when the medium is a metal, the secondary electrons loose energy mainly by collisions with the electrons in the conduction band, by lattice vibration and defects. Typically, for a metal, the escape depth is $\sim 1nm$, which is a very small one. Same for the minimum escape energy to overcome the energy barrier which is $\sim 10eV$.

Regarding insulators materials, they have a totally different behaviour in respect to metallic ones. In this case they are two main effects:

- Creation of an induced negative charge due to the trapping of a fraction of incident electrons.
- Creation of an induced positive charge due to the emission of secondary electrons.



The coexistence of these two charges creates a surface potential, resulting in a charging process for the material. The reason why metals and insulators have been taken into consideration will be more clear in paragraph 1.4, when the hardware of the SEE-based BPM used in IRRAD facility will be illustrated. For more theoretical considerations about SEE phenomenon, refers to [7].

1.2.4 Main parameters affecting SEE

Primary Energy

The primary energy related to incident particles is the only responsible for the variation of penetration depth value of secondary electrons, which means that SEE phenomenon is independent on the nature of the incident particles (positive or negative). In particular, the penetration depth of the secondary electrons (the maximum depth they are created) increases proportionally to the primary energy and thus, the number of the SE is proportional to the primary energy. So this basically suggests that the higher is the primary-electron energy, the deeper internal SE are originated beneath the surface.

Sensing material

For dosimetry and beam monitoring application, SE emitters are required to be made of a low cost and relatively short activity lifetime material. Moreover, the best kind of materials for a good emission should present high purity (and consequently low amount of defects), thus allowing electrons to move freely inside the lattice. Scattering properties of the material are also important, since the scattering helps to distribute the primary electrons energy among material electrons, resulting in an higher SEE. Foils made of Ni, Rd, Ag, W, Au give stable operation but in certain experiments they cannot be used because of the high γ -background from the bremsstrahlung and the multiple scattering of electrons. Commonly used materials include Al, Au, Cu, stainless steel, CuBe, Ag an Ti.

Surface Conditions

In order to observe a good SEE, the surface must be clean and free from any kind of contaminants like dust, oils and processing residues. According to the material, different cleaning procedures can be applied, including solvents use or ultrasound processes. Another important process which can influence the SEE phenomenon is the oxide layer because of low potential barrier and Mater effect (charging effect). The surface potential



barrier of a metal with oxide is lower than the one without oxide, which means there is higher probability for the electrons to escape from the oxide surface.

Angle of Incidence

Angle of incidence of primary particles can affect the secondary emission. In general, angle of incidence is defined as the angle formed between the incident beam direction and the perpendicular direction to the surface of the material. The equation which describes the relation between the incident angle θ and the total yield can be calculated from the equation:

$$\delta(\theta) = \delta(0)\cos^{-1}\theta \quad (1.2)$$

Figure Fig.1.10 gives an example of angular distribution from a single-crystal sample surface.

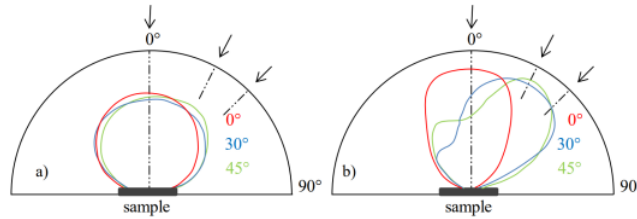


FIGURE 1.10: Angular distribution of (a) SE and (b) BSE emitted from polycrystalline

According to equation 1.2, $\delta(0)$ is the total perpendicular yield. Thus, the presence of a $\cos$ factor suggests that a perpendicular angle of incidence maximize the yield, thus resulting in a larger SEE. A different angle from 90° or 0° creates a lower emission according to the formula. Another important characteristic to take into consideration is the anisotropy of the material. An asymmetry in the structure of the material can cause different secondary emission based on the angle of incidence. For some materials, it can happen that the emission is higher when the angle is not perpendicular to the surface.

Vacuum

Performing the operations inside a vacuum chamber allows to observe a larger SEY and make it easier to collect the electrons generated by the beam as they are flowing in a larger amount from the emitting material.



1.3 IRRAD's BPM - Hardware and system architecture

To successfully measure the profile of the beam, the IRRAD team developed a specific Beam Profile Monitor (BPM) system based on the particle-induced SEE from metallic surface in order to satisfy all the requirements they need and that can provide the performances necessary for the correct evaluation of the beam profile. A list of these parameters is done in subsection 1.3.4. For several years, precisely during the run 2014 to 2018 of IRRAD, the original technology consisted of some flexible Printed Circuit Boards (PCBs) patterned with a matrix of metallic sensing pads on one end and a multi-pin connector on the opposite one. These devices were initially manufactured with a standard flexible PCB technology, composed of multiple copper layers sandwiched with epoxy glue. Different types of BPM sensors are used in the IRRAD facility according to the parameter that need to be used. The basic BPM detector, the so-called *fixed-BPM*, consists of a matrix of 39 sensing pads (pads of $4 \times 4 \text{ mm}^2$ and a pitch of 4.5mm). It is used to tune and steer the beam shape along the T8 beam-line. There are four fixed-BPM detectors in total along the IRRAD facility, they are shown in Fig. 1.11. The BPMs are adjusted on the supporting plastic frame with Kapton®. Position of the four BPMs in the T8 beam-line of the IRRAD facility can be seen in Fig. 1.16.

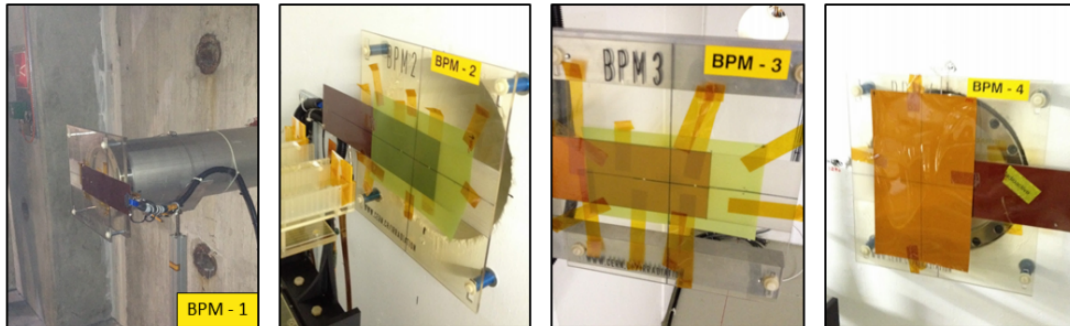


FIGURE 1.11: Installation of the four fixed-BPMs in the IRRAD facility

In addition to the fixed-BPM, there are other devices like the miniBPM, which consists of 9 pads distributed in a cross shape which purpose is to measure the beam profile in two directions (vertical and horizontal). The miniBPM is used to align the remote controlled tables of IRRAD with respect to the beam and thus, precisely position samples across the beam line. Moreover, there is another device, the so-called single-pad BPM, which is literally a single pad device installed on the outer sample holder of each irradiation table. This BPM device is made in a way that the beam spot can be moved by the fixed distance of $\sim 72 \text{ mm}$ with respect to the central position. In this way, this type of BPM can provide a binary signal indicating whether the sample loaded on a given sample holder are inside

or outside the beam line. In this way there is no need of the usage of miniBPMs which requires a nine-channel readout setup to operate. Eighteen single-pad beam monitors in total are used in the facility.

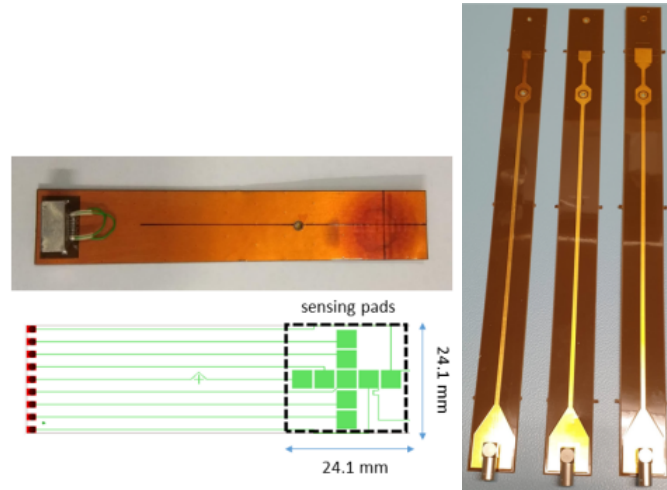


FIGURE 1.12: MiniBPM device (left) and single-pad BPM (right)

MiniBPMs and single-pad will not be further discussed in this work since the final project has been realized in order to work with the fixed-BPM devices. Further information about BPMs manufacturing can be found in [7].

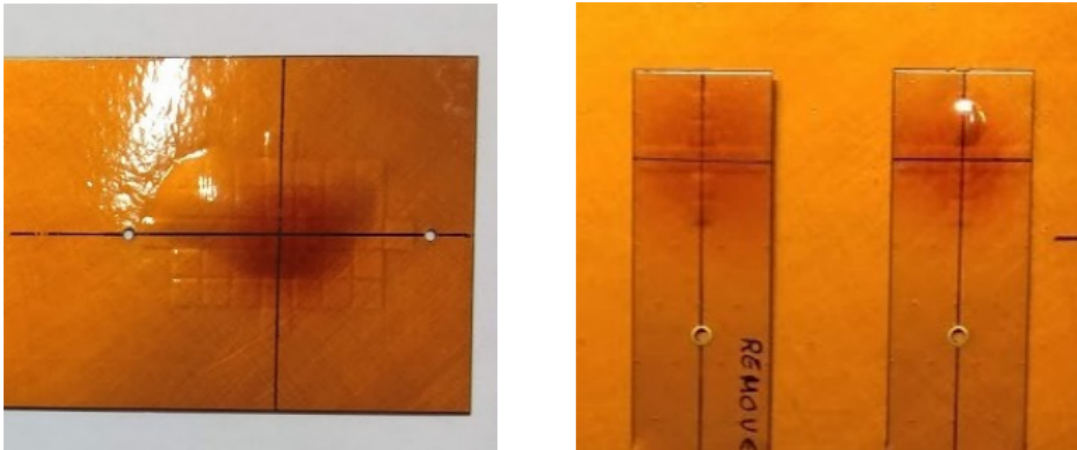


FIGURE 1.13: Damages on BPM sensors after 4 years of operation

Despite the good results obtained, these devices have shown damages (deataching, burning and bumps) on the region traversed by the beam, because of the usage of epoxy glue between the sensing and the isolating layers. Also, the sum of multiple devices in series, created a thickness of almost 2mm of copper and 8mm of polyimide to the total material budget, significantly contributing to the multiple scattering in the beam-line. Finally,

it's also necessary to mention that the devices became highly radioactive after long time exposure, thus creating a problem when the staff had to access the facility to perform some maintenance.

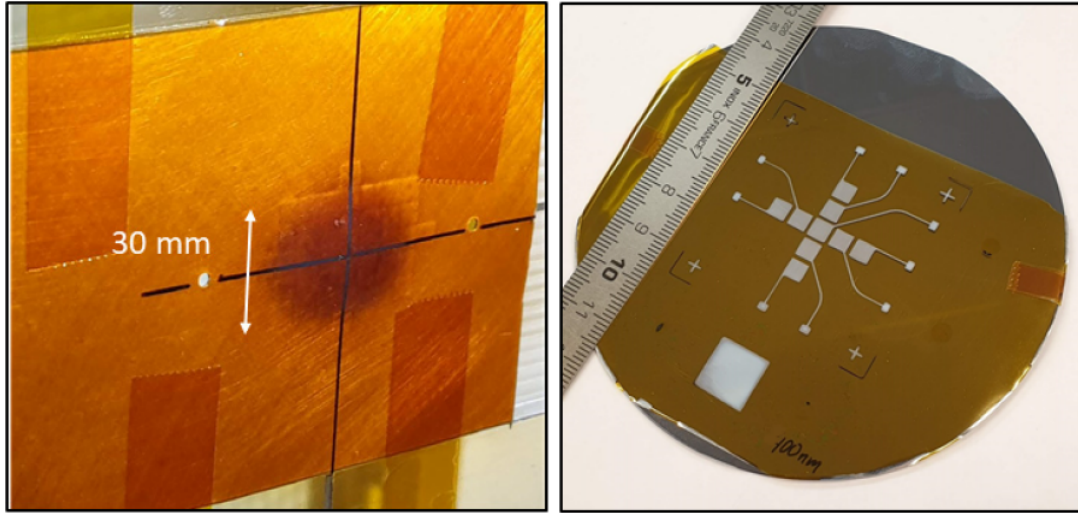


FIGURE 1.14: On the left the old BPM device technology (case of MiniBPM, on the right the new one

According to the results obtained with the BPM system described above, it was necessary to create a new generation of devices which could endure all the new requirements which have been identified in previous experiments: they needed to be fabricated in a different material which can withstand, at least for one year of operation, the proper amount of radiation cumulated, in order to minimize the exposure of the operators and users. Moreover, a smaller thickness was desired in order to reduce the multiple scattering and any interference with the beam. The solution for these requirements was found in Microfabrication techniques. A thin film (down to nanometre scale) can be deposited on rigid substrates with standard techniques, which is a good point as it make it easy the manufacturing process. Initial production was entrusted to the Centre of Micro and Nano technology (CMi) of EPFL in 2018. After several tests on standard Si/SiO_2 wafer substrates, the idea of silicon substrate was replaced by the Polyimide (Kapton). This last material was chosen because of its thermal and chemical stability, low dielectric constant, high electrical resistivity, possibility of getting very thin films and radiation tolerance. Regarding the sensing material, Aluminium was chosen because of the large availability, low cost and higher Secondary Electron Yield (SEY) compared to Copper. The polyimide substrate was treated with oxygen plasma and titanium under vacuum pressure before the metal deposition, in order to improve adhesion properties between the two materials.

The latest version of BPM detector, as in Fig. 1.15, is made with a PCB in the end of

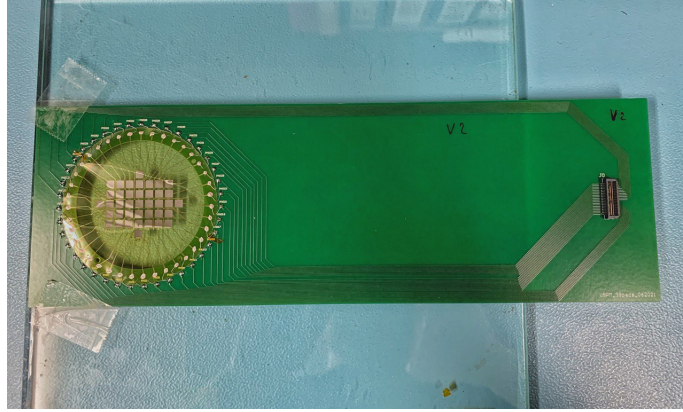


FIGURE 1.15: Latest fixed-BPM detector (39 Aluminium pads)

which there is a circular hole where the layer of Kapton has been placed. It is possible to see the Aluminium pads microfabrication on the Kapton layer, in particular 39 pads have been printed in this case. A series of traces bring the signal to the other part of the PCB, directly connecting the pads to the Samtec female connector. The new BPMs added several improvements with respect to the older version. They resulted to be thinner and more durable, because of material processing. Moreover, an higher response to the beam was also observed. Other experiments were done with the final aim of increasing the SEY, changing the thickness of the metal, adding extra oxide layers or modifying other structural and beam parameters. For details about tests and results refer to [8]



FIGURE 1.16: Position of the four BPMs in IRRAD

1.4 Data Acquisition System (DAQ)

The currently BPM DAQ unit has been designed to measure detector signal in the 10pA-to-500pA range with an adjustable dynamic range. Signal coming from the pads needs to



be integrated first and then converted to digital. Further details about this process will be described in the next chapter. About integrators, the system uses a *Burr Brown ACF2101* to amplify detector signals. After integration a *TI ADS115* analog-to-digital converter (16-bit) subsequently digitizes the charge integrated over the 400 ms proton spills. Finally, a commercially available Arduino® Yùn microcontroller board, based on the ATmega32u4, handles the whole DAQ process, including the timing synchronization and the background noise acquisition. This DAQ can read up to 50 channels in parallel: 40 channels from the main BPM pixel detector through a shielded, high-speed, 40-channel, 50Ω/40ACG micro-coaxial cable from Samtec®[9]. The last 10 channels are auxiliary and they can be connected through LEMO® connectors (visible in Fig.1.17 on the front panel).



FIGURE 1.17: IRRAD BPM Data Acquisition System

The DAQ has three outputs:

- **Analog Output:** provides the inverted output of the integrators and it is used to show the output of a selected integrator channel during operation.
- **Reset Output and Gate Output:** Both used to check in real time the synchronization of the timing parameters of the BPM with the signal provided by the PS accelerator.

About inputs:

- **Trigger:** Used to inform that a proton spill will occur upon its reception (beam trigger).
- **CPS:** This signal informs the microcontroller that, after this input is received, a new super cycle of the PS accelerator begins
- **USB 2.0:** This input is located on the rear panel and it is used to provide external storage media to the Arduino as well as to update the DAQ software.

- **Ethernet:** This connector is located on the rear panel as well and it is used by the MCU to access the CERN network over a wired connection

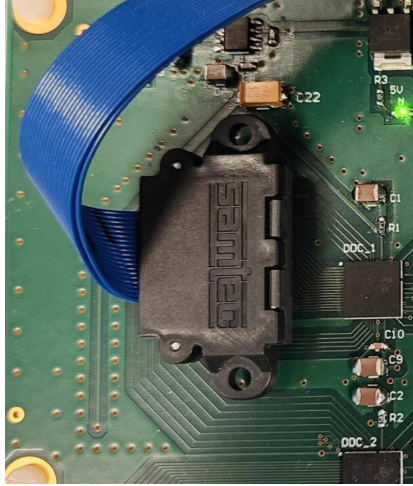


FIGURE 1.18: Samtec Cable 40-channels

Finally, there is a server running a dedicated software in order to collect data and send them to a centralized ORACLE® database where the spill-by-spill beam positions are archived for later analysis.

1.4.1 BPM Data Display

The beam profile information can be visualized in real-time through a dedicated series of CERN web pages². Not only IRRAD facility uses these information for their purposes but the CERN Control Center (CCC) monitors these pages in order to setup and steer the irradiation beam over the T8 beam line. Fig.1.19 shows one of the user interface pages of the web-application which retrieves and displays data from the ORACLE database. This web application is also capable to apply a first level data correction (for instance background compensation). Moreover it is computing the basic information about horizontal (x) and vertical (y) Gaussian beam profiles such as the centroid (x_0, y_0), the sigma ($\sigma_{x,y}$) and the Full Width at Half Maximum (FWHM). Some other web pages are available (not displayed in this document) like the one showing all four BPM 39-channel devices located along the beamline in real-time in order to fully control the beam trajectory over the 30 m long IRRAD facility.

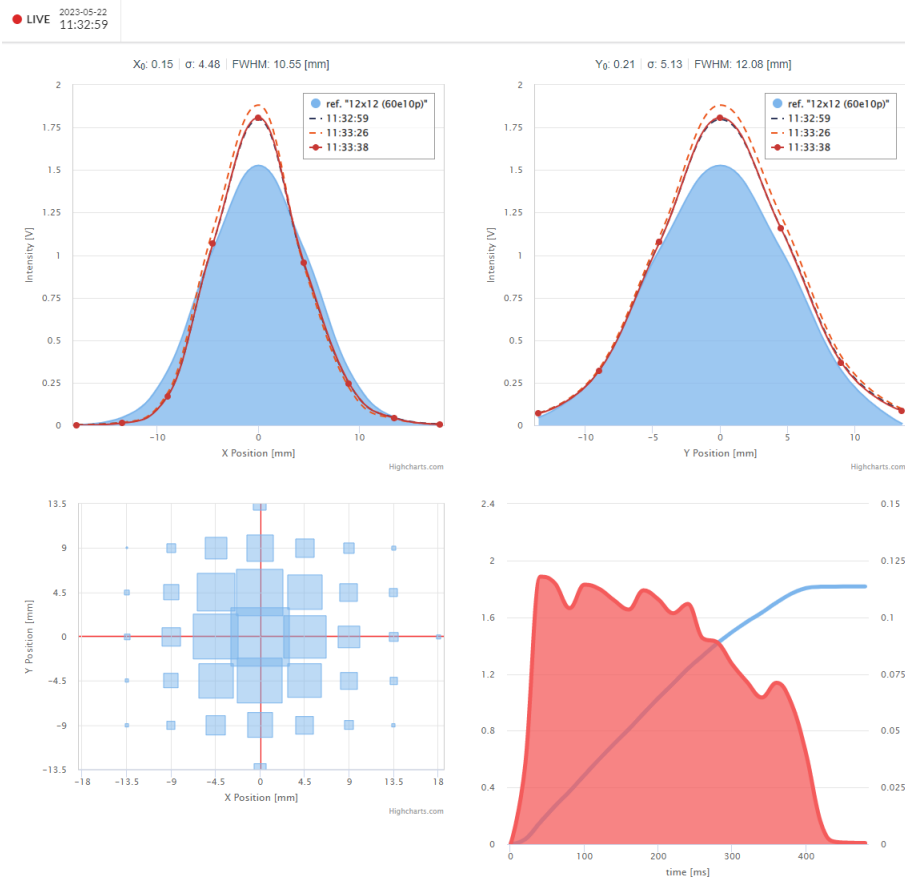


FIGURE 1.19: BPM web display

²www.cern.ch/opwt/irrad

CHAPTER 2

FRONT-END ELECTRONICS: ANALYSIS OF REQUIREMENTS AND FIRST RELEASE

In the previous chapter the IRRAD facility has been described, with a focus on the BPM technology used in order to acquire informations about the profile of the beam. In this chapter, the next step will be described, in particular the evolution of the current signal coming from BPM pads will be analyzed, starting from its integration and A/D conversion processes and finally ending to its elaboration with a microcontroller. After analyzing these theoretical concepts, the document will move on to the analysis of the components that have been selected to fulfill this purpose. Therefore, the functionalities as well as the potential of these objects will be specifically described and how they can be adapted to the system in question will be discussed. Finally the first release of front-end electronic with these components will be shortly discussed, a 64 channel board which has been made as a prototype to test the functionality and the efficiency of the selected components. The results obtained will be discussed, as well as the problems that have arisen, thus leading to the third chapter with the realization of the pivotal project of this document.

2.1 Measurements of the charge from BPM pads

As we said above, when BPMs are exposed to the beam, secondary electrons are emitted from each pad, thus generating a charge proportional to the particle flux crossing the pads. This charge can be measured individually for each pad using a proper readout system. The amount of charge generated by the proton beam as it passes through the aluminium pads of the BPM will depend on various factors such as the energy and intensity of the beam, the size and spacing of the pads, and the material properties of the pads. In general, the charge is relatively small due to several reasons:

- **Amount of charge:** Electrons are very small particles and they carry a relatively



small charge (approximately $1.6 \cdot 10^{-19}$ Coulombs). Due to this small amount of charge generated by the pads, it is necessary to implement a proper electronics which is sensitive to these small values of current.

- **Low amount of electrons generated:** The number of electrons emitted from the material is relatively small, this can be seen in subsection 1.3.3 with particular reference to Fig.1.9.

2.1.1 Charge Sensitive Amplifier

With the name Charge Sensitive Amplifier (CSA) [10] a type of circuit is described which allows to read the charge from a detector using a capacitance. It is possible to obtain an output voltage that is proportional to the charge rather than the current. Wiring diagram is shown in Fig.2.1.

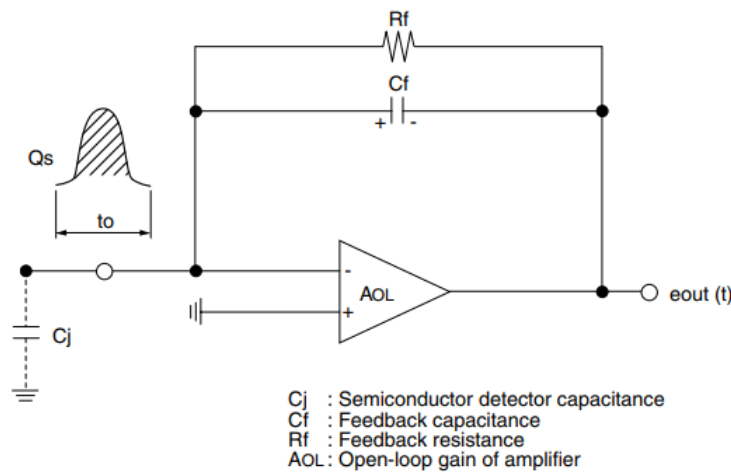


FIGURE 2.1: Principle of operation

As a first approximation it is possible to neglect the feedback resistor R_f in order to consider the amplifier as ideal, which means having the following characteristics:

- Infinite input impedance.
- Zero output impedance.
- Infinite open-loop gain.
- Infinite bandwidth with zero phase shift and infinite slew rate.
- Zero input offset voltage.



C_j and C_f will share the charge generated by the passage of the particle with a total amount of charge corresponding to:

$$Q_{gen} = Q_f + Q_j \quad (2.1)$$

As it is possible to see in Fig.2.1, both capacitors are connected to the input of the amplifier, so it is possible to write an equation for the input voltage:

$$v_{in} = \frac{Q_f}{C_f} = \frac{Q_j}{C_j} \quad (2.2)$$

Thus:

$$Q_f = Q_{gen} \frac{1}{1 + \frac{C_j}{C_f}} \quad (2.3)$$

The output voltage can be calculated as:

$$v_{out} = -\frac{Z_f}{Z_{in}} v_{in} \quad (2.4)$$

Where $Z_f = \frac{1}{sC_f}$ and $Z_{in} = \frac{1}{sC_j}$ are respectively the feedback and input impedances. Replacing the Eq.2.2 in the Eq.2.4 the output voltage can be calculated as:

$$v_{out} = -\frac{C_j}{C_f} \frac{1}{1 + \frac{C_j}{C_f}} Q_{gen} \quad (2.5)$$

So basically the output voltage has been calculated in function of the generated charge. Moreover, the ration between C_j and C_f establish the gain of the amplifier. However, as said before, this is an ideal approximation since this circuit it is not working in real applications due to impossibility to discharge both capacitors in less than several milliseconds, which is definitely a large amount of time for the project presented in this thesis. In fact, if a second signal comes before the capacitor is completely discharged, the collected charge will be added to the charge already present, consequently causing a baseline shift in time and saturation of the amplifier. So, in order to reduce the discharge time, a feedback resistor R_f is added in parallel to the feedback capacitor. This modification allows the amplifier to sustain an high rate of input signals but reduces the gain. Also, to improve the amplifier performances, some additional stages are added to the CSA in order to "shape" the signal.

2.2 Texas Instruments® DDC232

The DDC232 [11] is a 20-bit, 32-channel, current input analog-to-digital (A/D) converter. Thanks to the combination of current-to-voltage and A/D conversion it allows to acquire and 32 separate low-level current output devices, such as the pads of the BPM described above. Some of the features are listed below:

- Low Power: 7 mW/Channel
- Adjustable Full-Scale Range
- Daisy-Chainable Serial Interface.
- Low Noise: 5.3ppm of FSR

2.2.1 Block Diagram

The block diagram of the DDC232 is shown in Figure 2.2.

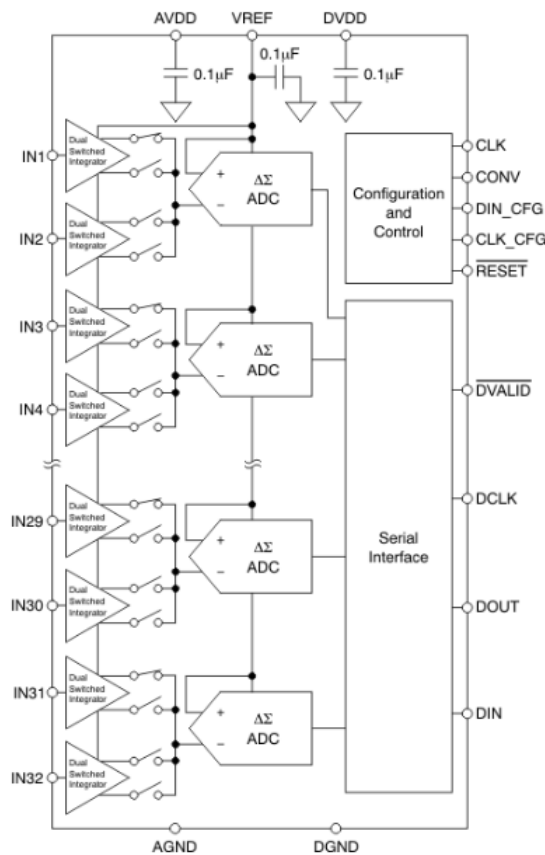


FIGURE 2.2: DDC232 Block Diagram

On the left side is possible to see 32 identical input channels which are Dual Switched Integrators and perform the function of current-to-voltage integration followed by a Sigma-Delta ADC. On each input there are two integrators in order to offer a continue integration in time. The output of the 64 integrators are switched to 16 delta-sigma converters via multiplexers. The basic principle is to digitize the input from one side and to use the other 32 integrators to integrate the next input in the same time. Everything is controlled by a system clock (CLK) and every result is stored in a serial output shift register, through the DOUT pin which gives 20-bit words at every clock signal.

2.2.2 Basic Integration Cycle

As said before, the device is provided with 32 channels, but each channel executes a dual integration process. In the subsection it will be described only one integrator, since the second one is working following the same diagram. Block diagram can be seen in Fig.2.2. The input stage is made of an operation amplifier configured as an integrator. According to what said before, it is necessary to perform the charge amplification and for this reason the OP Amp is equipped with a feedback capacitor network (C_F) and several switches that implement the integration cycle. The capacitor network is made with the purpose to achieve the specified performance for range error of the DDC232. The range control bits change the capacitor value for all the integrators. Consequently, all inputs and both sides of each input will always have the same full-scale range.

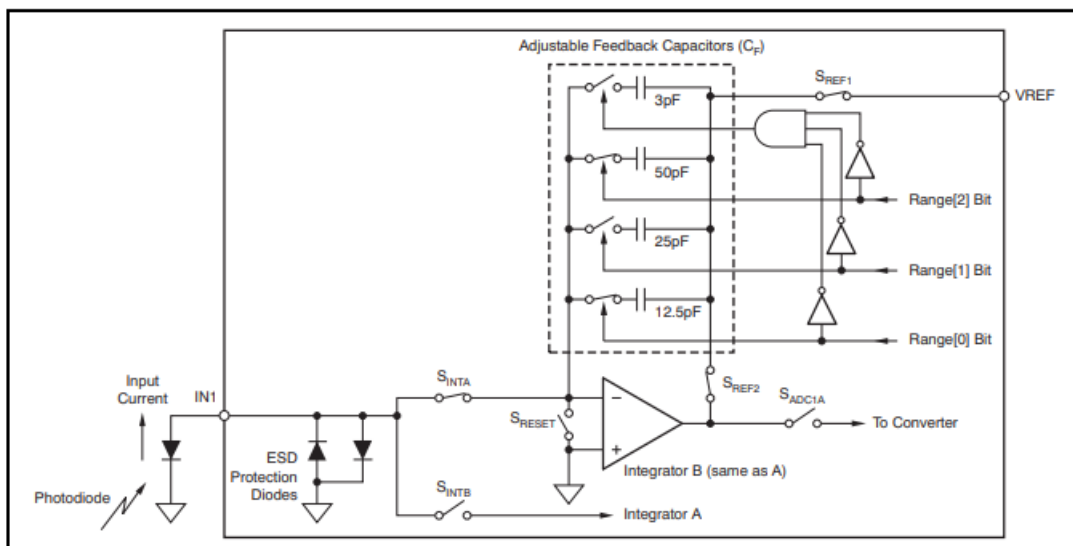


FIGURE 2.3: Basic Integration Configuration

The Fig.2.4 shows the integration timing according to each switch while the Fig.2.5



shows the four different configuration that is possible to realize with switches on the front-end integrators. The internal switching network is directly controlled by the convert pin (CONV) which is synchronized with the rising edge of the clock (CLK) signal. The non-inverting pin of the OP Amp is directly connected to the ground signal and it is specified that the DDC232 analog ground must be the cleanest possible. From the integration timing Fig.2.4 is it possible to see that at the beginning of a conversion, all the switches are set. After the completion of an A/D conversion, the charge on the integration capacitor (C_F) is reset with S_{REF1} and S_{RESET} (Fig.2.5a). During this phase (reset phase) the C_F is charged to the voltage reference (V_{REF}) value. After the C_F is charged, S_{REF1} and S_{RESET} are opened so that V_{REF} is no longer connected to the amplifier. The circuit is now waiting (Fig.2.5b) to begin the integration. When the rising edge of CONV comes, the circuit goes in integrating mode, which means that the switch S_{INTA} closes, making the integration on the side A begin (Fig.2.5c). It's important to notice that in the meantime the side A is integrating, the signal on the side B is being converted into digital and then reset. This allows the component to have a continue integrating process and conversion in the same time with a great reduction of operating time. With the falling edge of CONV, the side B starts integrating the input signal, while the output voltage on the side A operational amplifier (already integrated) is presented in input to the delta-sigma converter (Fig.2.5d)

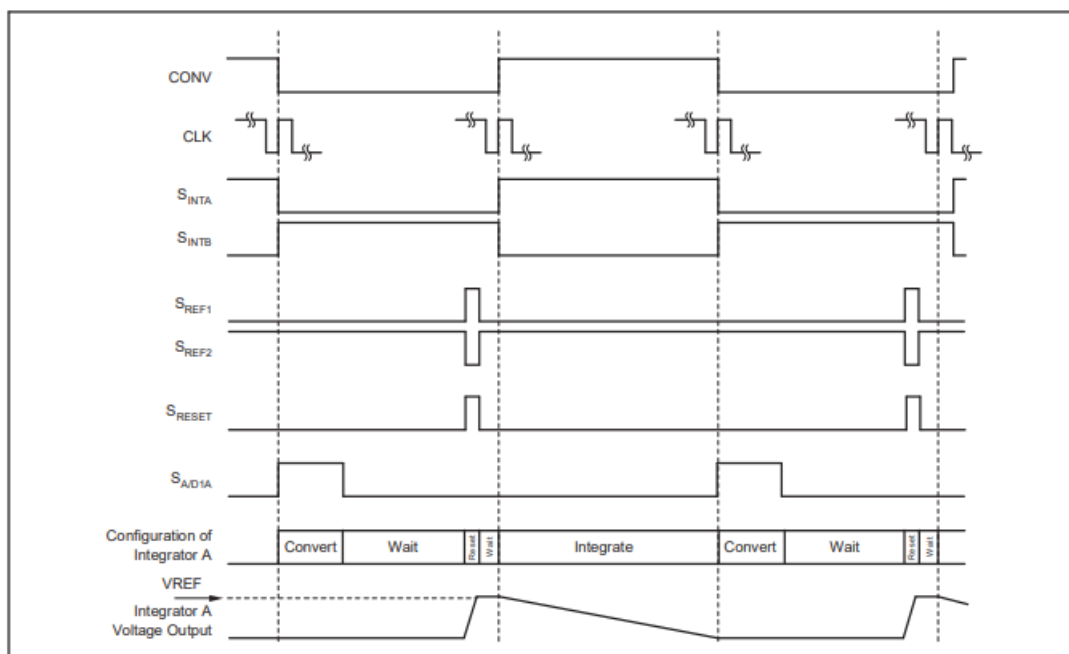


FIGURE 2.4: Integration Timing

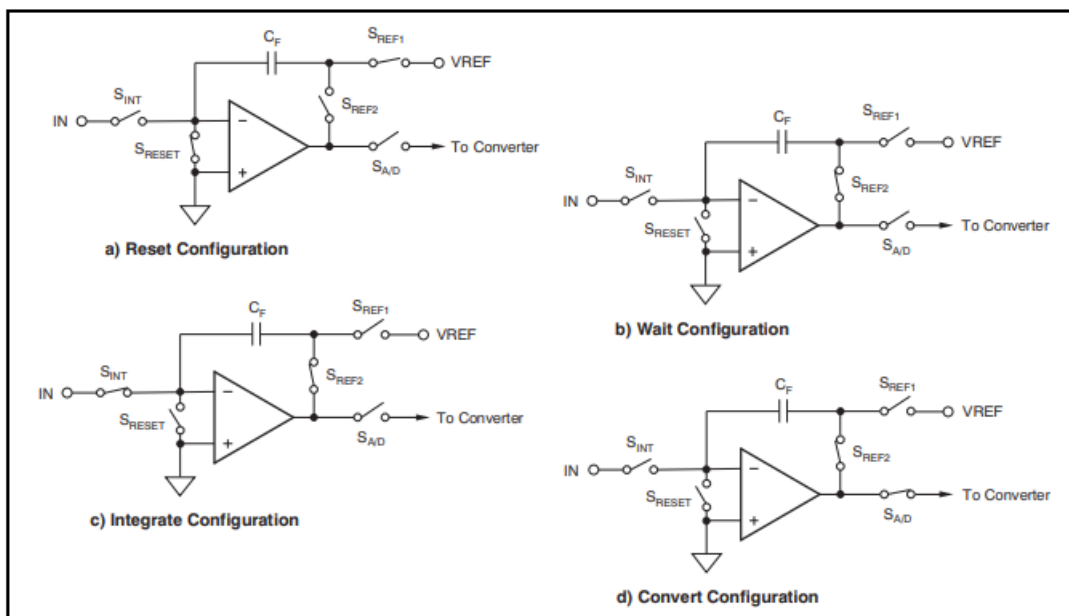


FIGURE 2.5: Four Configurations of the Front-end integrators



2.2.3 A/D Conversion: overview on Delta-Sigma converters

Delta-Sigma converters offer good performances in high resolution, high integration and low price, which make them a good choice for monitoring and process control applications. Main characteristics of Delta-Sigma converters are listed in the following steps:

- Analog part is very simple. Digital part (for filtering and decimation), makes the sigma-delta converters very cheap in term of manufacturing, despite the complexity.
- They offer the possibility of oversampling.
- Noise shaping.
- Digital filtering and decimation.
- Integration (for the reduction of normal mode noise).
- Delta modulation.
- Substitution of the amplitude resolution with temporal resolution thanks to a clock frequency much higher than Nyquist one, and 1 bit quantizer.

Basic structure of a delta-sigma modulator is composed by an differential amplifier, and integrator and a comparator with a feedback circuit containing a 1-bit digital-to-analog (DAC).

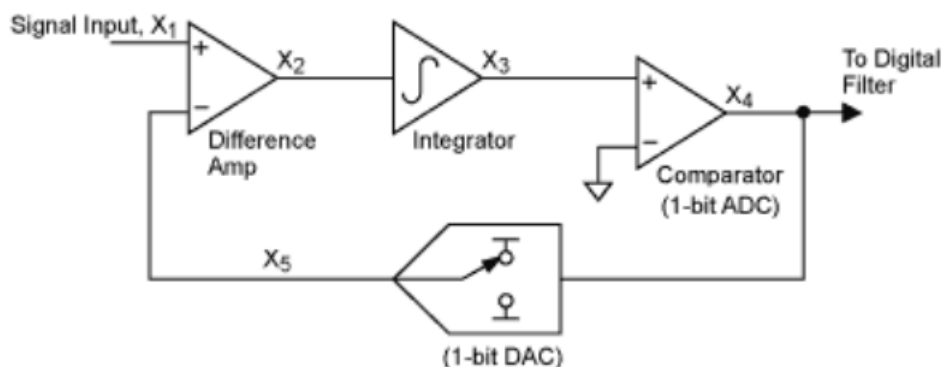


FIGURE 2.6: Basic architecture of a Delta-Sigma modulator

This DAC is basically an Single Pole Double Throw (SPDT) switch connecting the negative pole of the differential amplifier to a reference voltage which can be positive or negative. The basic functioning of this circuit is the delta modulation, which consists in

a simple version of the Differential Pulse Code Modulation (DPCM). This kind of modulation does not transmit the exact binary code of a given sample but his variation (Δ) compared to the previous value. Basically, if the sample taken in an exact moment $t = iT$ is bigger than the previous one, then the output will be increased of a Δ value. If the sample is smaller, then the output will be decreased of the same value. According to the Fig.2.6 the analog voltage which goes out from the 1-bit DAC is subtracted to the signal x_1 in input; the result x_2 is then integrated and send to a 1-bit ADC, or better, a comparator which gives a 1 or a 0 in output according to the reference voltage on the inverting pin. So the DAC gives in output an analog voltage corresponding to this bit which is then subtracted again to the difference amplifier in order to restart the cycle. According to this basic operations, in output there will be a serial row of bits and the amount of "1" or "0" inside it is proportional to the input signal. So for a rising input signal, the comparator will generate an higher number of "1" values. They are several additional features which makes delta-sigma converters a perfect component when an A/D conversion is needed, like the oversampling feature or the possibility to have a very powerful noise shaping mechanism adding more integrators thus resulting in a major order converter. However these topics will not be discussed in the following pages, in order to focus on the remaining structure of the DDC232.

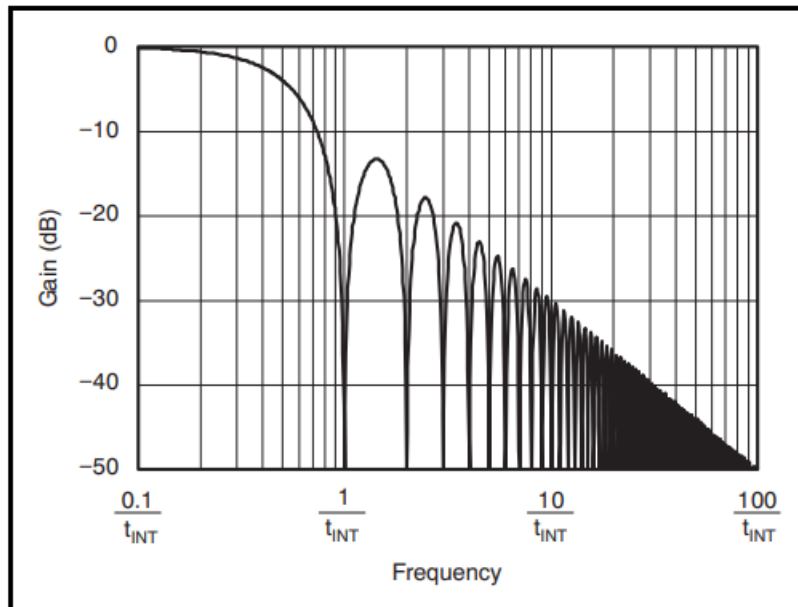


FIGURE 2.7: Frequency Response of a DDC232



2.2.4 Frequency Response

The frequency response of the DDC232 is set by the front-end integrators and is that of a traditional continuous time integrator, as shown in Fig.2.7. By adjusting t_{INT} it is possible to change the 3dB bandwidth and the location of the notches in the response. After the integrator they are the delta-sigma converters which are not influenced by the frequency response of the previous stage because the converters are already sampling a held signal from the integrators (thanks to the continuous mode operation). For this reason the input of the delta-sigma converters is always a DC signal.

2.2.5 Digital Interface

As it's possible to see in Fig.2.2, the block diagram of the DDC232 is also made of a digital interface called *Configuration and Control* since the output is sent through a serial interface. The main pins of this interface are:

- Data Clock - DCLK
- Valid Data - !DVALID (the "!" indicates that this signal is active-low)
- Data Output - DOUT
- Data Input - DIN
- Reset - RST

First of all it's important to notice that CLK and DCLK frequencies are not required to be the same since the integration and conversion process are independent. The DIN pin will not be used since it's required only when multiple converters are cascaded. For this reason it will be put at Digital Ground (DGND) signal. Regarding the clock signal, the system clock (CLK) is supplied to CLK and the data clock is supplied to DCLK. CLK pin must be driven by a free-running clock source. Not every data coming out from the DOUT pin is a valid data to be read, for this reason the !DVALID signal indicates that data are ready. Notice that the pin is active low, which means that lecture can start only when the !DVALID pin is goes low. Fig.2.8 explains very clearly the timing of the single operations. Regarding the CONV signal, this goes low when integration finishes on side A and starts on side B. Immediately after CONV goes low, A/D Conversion starts first on the odd channels and after on the even channels. After both conversions, data are ready to be read, so the !DVALID pin goes low for as long as necessary to read data.

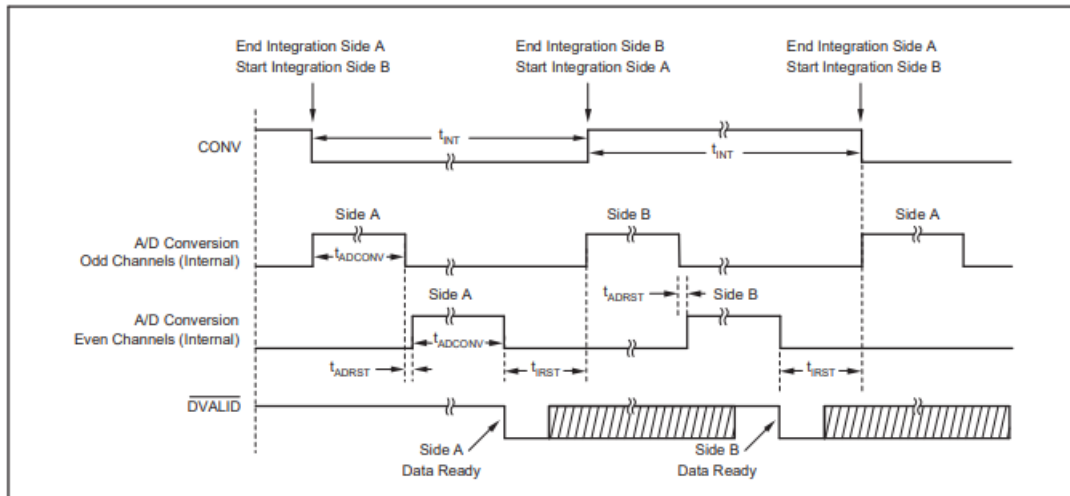


FIGURE 2.8: Internal Operation in Continuous Mode Timing

The !DVALID signal is generated using the internal clock divided down from system clock, CLK. The phase relationship between this internal clock and CLK signal is set when power is first applied and is random. Also with CONV signal the phase relationship is random since CONV phase must be synchronized with CLK.

!RESET signal is used to reset asynchronously the DDC232 every time it gets low. The reset pulse must be at least $1\mu\text{s}$ wide.

2.2.6 Operational Modes

The DDC232 has two main operational modes depending by the time used to make the A/S conversion. The A/D conversion time is primarily a function of the system clock (CLK) speed. In most of the cases, A/D conversion time is shorter than the integration time. If this condition exist, the DDC232 will operate in the continuous mode. When the DDC232 is in the continuous mode, the sensor output is continuously integrated by the one of the two sides of each input. In case the A/D conversion time is higher than the integration time, the DDC232 goes into noncontinuous mode, where the A/D converter is not able to have the same pace with the speed of integration process, which means that integration process is periodically stopped until the A/D conversion is done. The continuous and noncontinuous modes and the relative state diagram are described in the datasheet and their functionalities will not be part of this work. For the continuous operation the reference image is the Fig.2.8, while for the noncontinuous Fig.2.9.

The CONV signal, which establishes the start/end of the integration operations on both sides, ends way before the A/D conversions, which means that the integrators enter in

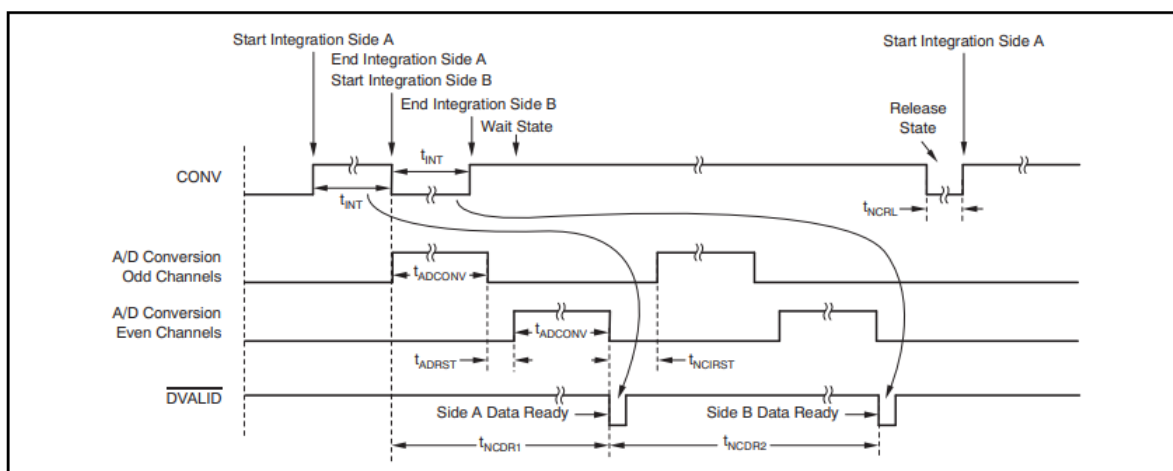


FIGURE 2.9: Internal Operation in Noncontinuous mode timing

INPUT SIGNAL	IDEAL OUTPUT FORMAT = 1	IDEAL OUTPUT FORMAT = 0
$\geq 100\%$ FS	1111 1111 1111 1111 1111	1111 1111 1111 1111
0.001531% FS	0000 0001 0000 0001 0000	0000 0001 0000 0001
0.001436% FS	0000 0001 0000 0000 0010	0000 0001 0000 0000
0.000191% FS	0000 0001 0000 0000 0010	0000 0001 0000 0000
0.000096% FS	0000 0001 0000 0000 0001	0000 0001 0000 0000
0% FS	0000 0001 0000 0000 0000	0000 0001 0000 0000
-0.3955 % FS	0000 0000 0000 0000 0000	0000 0000 0000 0000

TABLE 2.1: Ideal Output Code vs Input Signal

a Wait State before starting a new integration. Further information, such as switching between the two modes or technical specifications on integration and conversion times in the two modes can be found in the datasheet.

2.2.7 Data Retrieval

They are two different type of binary code that can be sent in output according to which selection has been made on the Format bit. The Format bit is located in the configuration register and selects how many bits are used in the output word. If Format bit = 1, then the output word is 20-bit wide, otherwise for Format bit = 0, a 16-bit word is sent in output, truncating the lower 4 bits. An offset is included in the output to allow slightly negative inputs (for example, from board leakages) from clipping the reading.

As already seen in Fig.2.9, in both operational modes, data are available for retrieval when the !DVALID pin goes low, or better on its falling edge. This behaviour is better seen in Fig.2.10. Data are shifted out on the falling edge of the DCLK signal. It's important

not to retrieve data during CONV changes because this can introduce noise (at least $10\mu s$ before or after a CONV transition). Having a Format bit + 0 (then a 16-bit output word) will reduce the time needed to retrieve data by 20%.

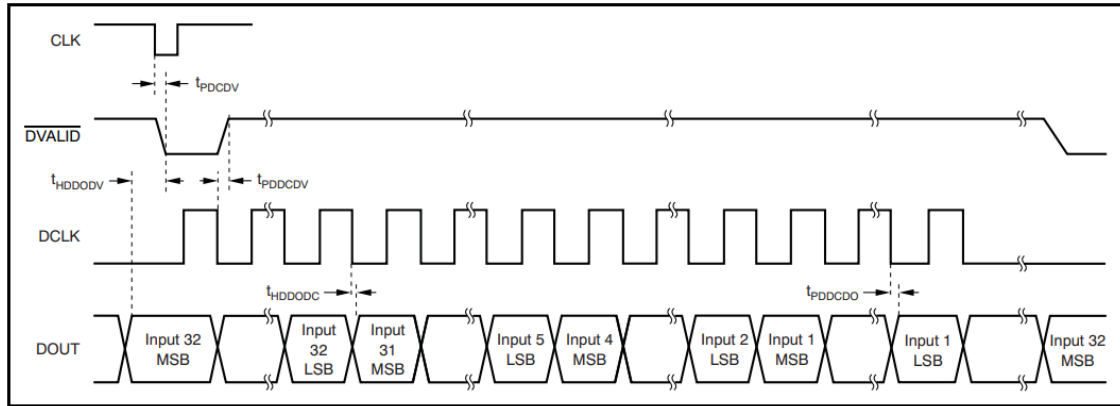


FIGURE 2.10: Timing for Data Retrieval from a Single DDC232

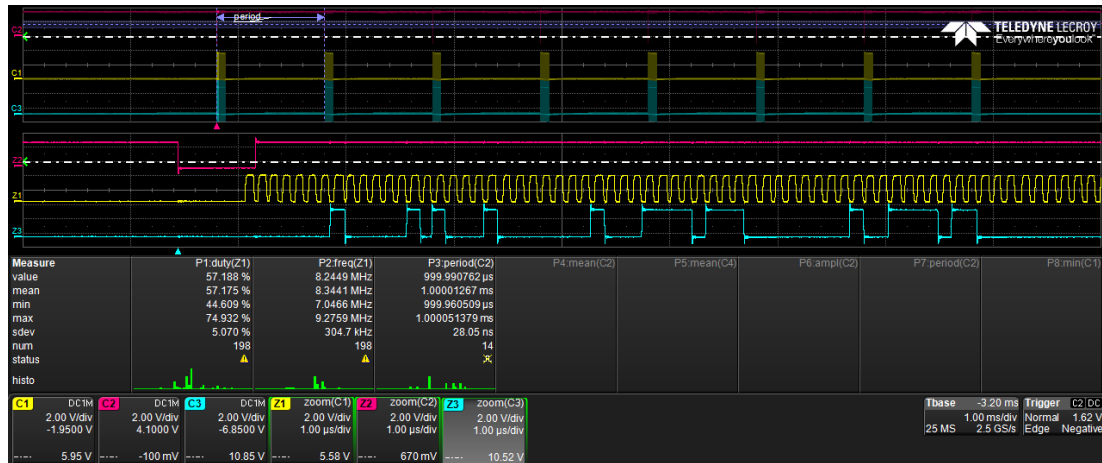


FIGURE 2.11: Oscilloscope screenshot from DDC232's Digital Interface Timing

The Digital Interface Timing has been measured in laboratory using a Teledyne-LeCroy HDO65104-MS oscilloscope and mounting the DDC232 on a prototype board whose characteristics will be discussed in paragraph 2.4. The signals received by the DDC232 have been generated with a microcontroller (MCU), that will be discussed in paragraph 2.3. The Fig.2.11 shows the measurements results where signals were put in the same order as the Fig.2.10, in particular:

- CH2 - Magenta : !DVALID signal
- CH1 - Yellow : DCLK signal

- CH3 - Cyan : DOUT signal

As first, notice that !DVALID (Magenta) goes low in order to communicate that data are valid to be read. After, DCLK signal starts its periodical behaviour and DOUT signal switches consequently. Notice that DOUT only changes on falling edges of DCLK signal. DDC232 behaviour is confirmed from this measurements, in particular a mean operative frequency of 8.3441 Mhz (according to datasheet it can be sped up to 20Mhz, but for this application 8 Mhz were appropriate) has been measured on the DCLK signal with a duty cycle of 57%. The period between one measurement and another (corresponding to the time passing between one falling edge of !DVALID and next one) is 1 ms.

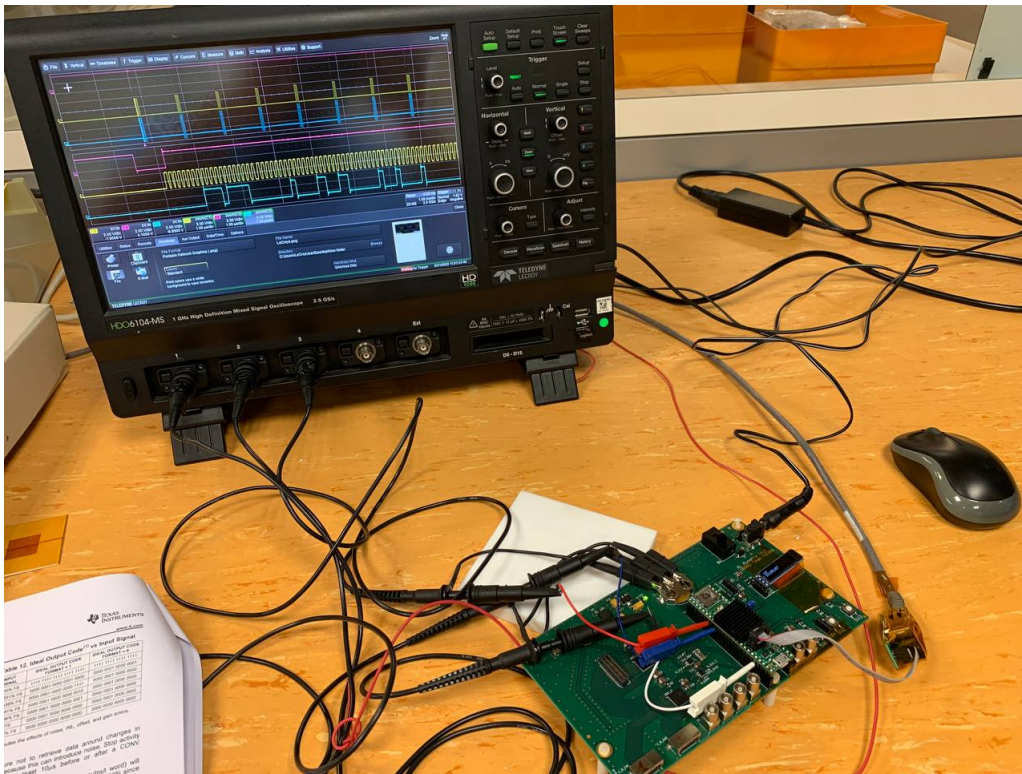


FIGURE 2.12: Oscilloscope setup for DDC232 behaviour measurements

Further considerations will be made below regarding the circuit design necessary for the implementation of the DDC232, with particular reference to the voltage reference circuit, the decoupling of the power supply and grounding.

2.3 PJRC Teensy 4.1

The Teensy 4.1[12] is a powerful microcontroller board designed for high-performance applications, created by PJRC. The board is equipped with the following features:



- **Microcontroller:** The Teensy 4.1 is based on the NXP i.MX RT1062 processor, which has an ARM Cortex-M7 core running at 600 MHz. It also features a floating-point unit (FPU) and a memory management unit (MMU), which enable faster and more efficient processing of data.
- **Memory:** The Teensy 4.1 has 1 MB of Flash memory for program storage and 1 MB (512 Kb tightly coupled). Additionally, it has 4 MB of external Flash memory that can be used for larger programs or data storage and 8 MB of ext. RAM.
- **Input/Output:** It has a total of 55 I/O pins, which can be used for digital input/output, analog input, PWM output and more. It also features 8 hardware serial ports, 3 I2C, 3 SPI ports and 3 CAN Bus (1 with CAN FD) ports, which enable communication with other devices.
- **Communication:** The Teensy 4.1 supports a variety of communication protocols, including USB 2.0, Ethernet and a CAN bus. It also features a built-in MicroSD card reader, which can be used for data storage.
- **Power:** It can be powered through a USB connection or an external power source (5V). It also features a built-in voltage regulator which reduces the 5V VUSB/VIN power to 3.3V.
- **Size:** It offers a 61mm x 18mm board, making it compact and easy to integrate into projects.

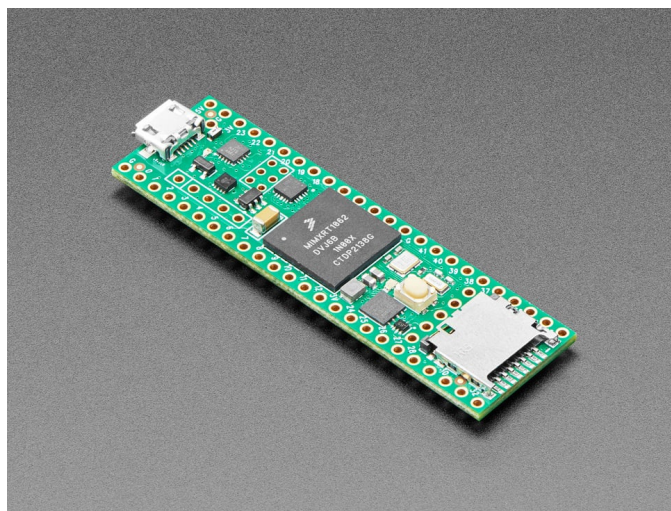


FIGURE 2.13: Teensy 4.1

The Teensy 4.1 was selected as the preferred microcontroller to acquire data from the DDC232 for several reasons. It is well-suited for high data transfer rates due to its powerful ARM Cortex-M7 processor. This allows for quick and efficient data acquisition from the Texas Instruments IC. Moreover, the MCU has low latency, which is crucial in acquiring real-time data. The fast processing speed of the Teensy 4.1 ensures that the data is acquired and processed in a timely manner, without any significant delay. Compatibility with the DDC232 is excellent, making the Teensy 4.1 easy to be integrated into the project and ensuring a seamless and reliable data acquisition process. Of course, the wide range of features and functionalities, such as GPIO pins, analog inputs and serial communication ports, can be used to interface with various sensors and devices. Overall, the combination of all the features mentioned above, made the Teensy 4.1 microcontroller the ideal choice for this project.

2.3.1 Memory Structure

In this section, memory structure of the Teensy 4.1 will be analyzed. It is important to understand this structure in order to make the most of its capabilities. Fig.2.14 represents the main four memory region on Teensy 4.1 and how they are structured:

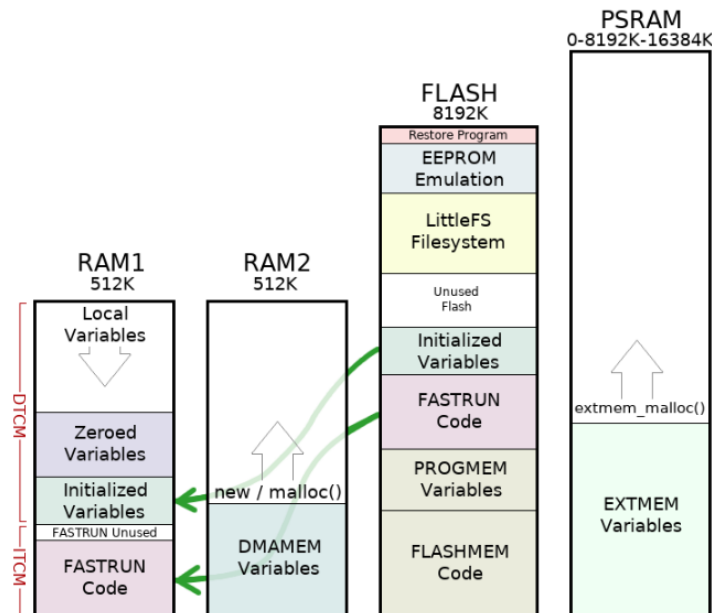


FIGURE 2.14: The Four Memory Regions on Teensy 4.1

- **Program/Flash Memory:** It has 8 Mbyte of flash memory intended for storing the code. The flash memory can also store read-only variables and arrays. The top part



(256 Kbyte) of this memory is reserved for EEPROM emulation data and the LED blink restore program.

- **RAM:** The total amount of RAM is 1024 Kbyte, available for variables and data. Of course is a volatile part of memory and in particular it results to be divided into two halves. Half of this memory (RAM1) is accessed as tightly coupled memory for maximum performance. The other half (RAM2) is optimized for access by DMA. Normally, large arrays and data buffers are placed in RAM2 in order to reserve the RAM1 (which is faster) for normal variables.
- **EEPROM:** 4284 bytes of emulated EEPROM memory is supported. Writing to this memory temporarily stalls code execution from flash. The EEPROM library is usually used to access this memory.
- **QSPI Memory Expansion:** Teensy 4.1 has 2 locations to add 8 pin QSPI memory chips. Both location support 8MB PSRAM chips.
- **RTC RAM:** 16 bytes of memory are located within the RTC. This is really important because using a coin cell connected to VBAT it is possible to preserve the content of this memory even when the power is off.
- **SD Card:** The board is prepared with an SD socket, allowing the user to mount an SD card for large data storage.
- **SPI Flash:** Flash memory chips may be added using the SPI pins.

2.4 Front-End Electronics: First Release

After selecting the main components that could satisfy the requirements of acquisition, conversion and processing of data coming from the BPM pads, the aim was to design and realize a first prototype of front-end electronics that could contain the components and perform the operations mentioned above. As a first approach it was decided to create a board that contained two DDC232, therefore a total of 64 channels that could be read in parallel. In reality, the number of channels needed for the final project is well over 64. Suffice it to say that, as can be seen in Fig. 1.16, the BPMs installed along the facility are at least 4, and it is highly probable that additional ones will be installed. However, being a prototype, having two DDC232 turned out to be an appropriate number. In fact, having more than one IC is helpful to understand if there is any problem regarding the communication and synchronization of the signals that the microcontroller receives from

two ICs simultaneously. Signal delay is a problem to take into consideration as well as clock distribution along the board. Regarding the input connections there is one Samtec® 40-ch connector which is not fully occupied from one DDC232 since this only has 32 channels. The remaining 8 channels were dedicated to the first 8 channel of the second DDC232. All the other channels from the second IC were divided between 2 Samtec® connectors (10 channels each) and 4 LEMO® connectors.

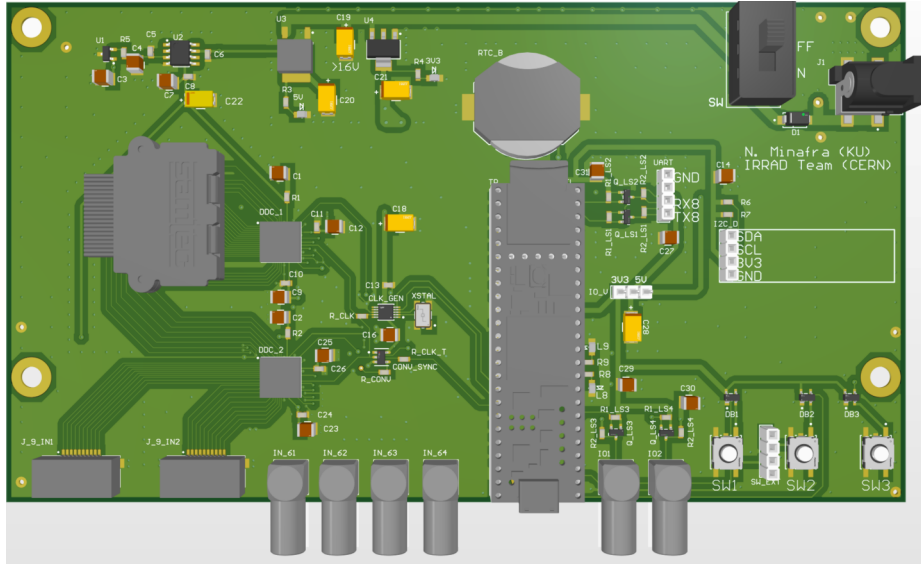


FIGURE 2.15: 2x32 Channel 3D View

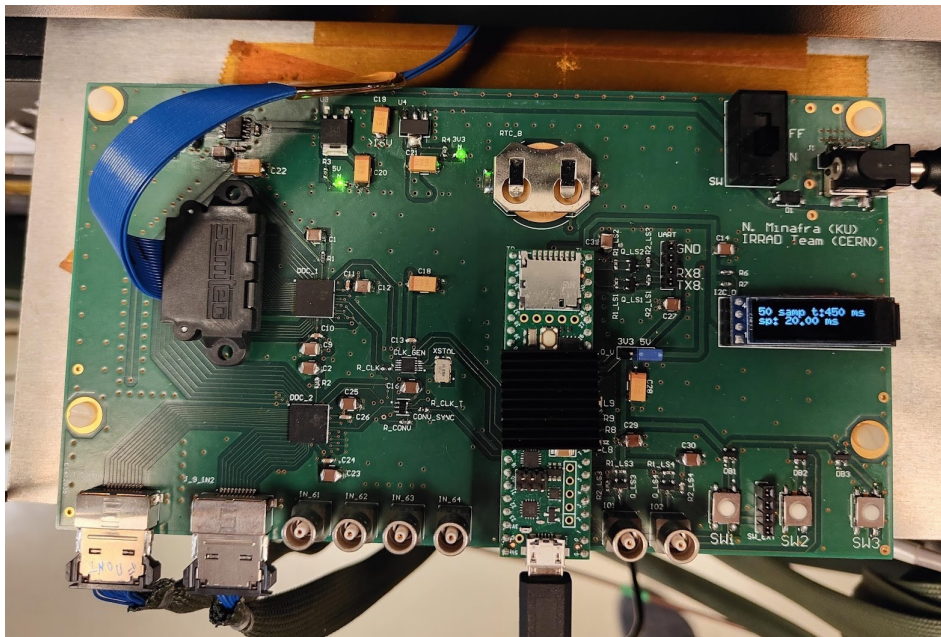


FIGURE 2.16: 2x32 Channel PCB



Wiring diagram of this prototype will not be described since the final project will be an extension of this one. Refer to chapter 3 for any information about the schematic.

IMPLEMENTED DAQ SYSTEM FOR IRRAD

3.1 Project Choices and General Structure

As said in the previous chapters, this thesis work focuses on the development of a front-end electronic system for the IRRAD Beam Profile Monitor (BPM) sensor, which plays a crucial role in many scientific and industrial applications, such as particle accelerators, synchrotrons, and free electron lasers. The system consists of several Printed Circuit Boards (PCBs), including a large motherboard that serves as the central hub, five smaller interposer boards that will be placed as shields, and a panel board that functions as the user interface.

Each interposer board is equipped with a DDC232 Texas Instruments component, which provides analog-to-digital conversion and signal conditioning for the BPM sensor. Since these components are expensive and difficult to manage due to low pitch, using interposer boards allows for easy replacement in case of a malfunction, without the need to replace the entire motherboard or perform complex soldering operations. This approach simplifies maintenance and reduces the cost of repairing the system.

The reason why 5 DDC232 components will be placed on the board becomes clear going back to Fig. 1.16. In fact, as shown in the figure and as discussed in the related paragraph, the number of fixed-BPMs currently in use in the facility is four, but a fifth unit is expected to be installed. Of course, this also explains why the first release, containing only two DDC232 ICs needed to be replaced by an upgraded version.

The motherboard serves as the central hub of the front-end interface for the BPM sensor. It includes several critical components, such as a microcontroller, power supply circuits, clock generation circuits, and various connectors. The microcontroller used in this system, as seen before, is the Teensy 4.1 which is responsible for acquiring the DDC232



output signals from the interposer boards and processing them to generate meaningful sensor readings. It also controls the panel board and manages the user interface, enabling the user, monitor some basic informations on a OLED display and to access to some I/O ports such as LEMO® connectors to send external triggers.

One of the most important features of the motherboard is its power supply circuitry. It provides stable and reliable power to all the components of the system, ensuring that they operate correctly and consistently. In addition, the motherboard includes a Power over Ethernet (PoE) feature, which allows the system to receive power and data through a single Ethernet cable. This feature simplifies the installation and reduces the number of cables needed, making the system more compact and user-friendly. Moreover, if compared with the first release, the PoE feature allows to solve some issues experienced during the testing, since sometimes the boards stopped working and it needed to be reset, but the facility was not accessible due to operational needs or because the issue happened out of working hours.

The motherboard also includes a clock generation circuit, which generates a stable and accurate clock signal for the DDC232 components on the interposer boards. This signal ensures that the analog-to-digital conversion and signal conditioning of the sensor readings are performed correctly and consistently, improving the accuracy and reliability of the system.

The overall design of the system aims to provide a reliable and cost-effective solution for the BPM sensor, with a user-friendly interface for easy operation and maintenance. The use of interposer boards and a modular architecture allows for easy expansion and customization of the system, depending on the specific requirements of each application. This gives to the system a large compatibility not only for IRRAD's BPM operations but also for other beam monitoring applications.



3.2 Power Supply Circuit

For the Power Supply Circuit, two operating voltages were mainly needed: the first at 5V to mainly power the DDC232 (Analog VDD) and other ICs on the board while the second at 3.3V to power the remaining ICs on the motherboard and the digital power supplies of all the DDC232. However the main supply source for the circuit needed to be 12V due to several reasons:

- **Efficiency:** Using a higher voltage to power the circuit and then regulating it down to the required voltage is more efficient than using a lower voltage power supply. This is because the regulator can more easily dissipate excess energy in the form of heat, rather than dropping it across a linear voltage regulator.
- **Voltage drops:** When current flows through wires and traces on a circuit board, there can be voltage drops due to resistance. Using a higher voltage can help to mitigate these voltage drops and ensure that components receive a consistent voltage.
- **Noise:** Using a higher voltage can help to reduce the impact of noise on the circuit. This is because any noise on the power supply line will be a smaller proportion of the total voltage.
- **Compatibility:** Using a 12V voltage also allows to cover any kind of modification on the circuit in case it is needed to add components or to supply some external component such as cooling fans for which specific connectors have actually been provided on the PCB.

3.2.1 Power Consumption

In the following table a power requirements calculation has been done. Notice that some of the components in the table will be described later in the document.

Component	Quantity	Supply Voltage [V]	Current(x4) [A]	Power (W)
DDC232CK	5	5	0.24	6
DDC232CK	5	3.3	0.032	0.528
Teensy 4.1	1	5	0.4	2
SI5351A-B-GTR	1	3.3	0.14	0.462
SN74LVC1G80	1	5	0.128	0.64
REF3140AIDBZT	1	5	0.00054	0.0027
CFM-6015V-122-145-20	2	12	0.116	1.4

TABLE 3.1: Power Requirements



According to the table 3.1 the total amount of power consumption should be around 11W, considering that for every device, a safety factor of 4 was used.

3.2.2 Power Over Ethernet

Power over Ethernet (PoE) [13] is a technology that allows for power to be transmitted over the same Ethernet cable that carries data, which can be useful in a variety of situations, such as when power outlets are not easily accessible or when multiple devices need to be powered from a single source. Several benefits are related to the use of a PoE technology:

- **Cost Saving:** PoE saves time and money by avoiding the need for separate installation of Data and Power infrastructures.
- **Simplicity:** Power is fully integrated with Ethernet infrastructure, so access to rough places for power deployment, such as ceilings, becomes simpler.
- **Simplicity:** Powered devices (PDs) can be easily moved without need for AC outlets, minimizing business disruption. Wherever there is an Ethernet connection, a PD can be easily deployed.
- **Security:** shutting down unnecessary PDs when no one is at office ensures better business security.
- **Control:** SNMP¹ management capabilities provide control and monitor of the PoE device and the powered devices.

According to the tests that were carried out on the first release, one of the main reasons why it was decided to adopt a PoE protocol is the fact that the board often required a restart and it was not always possible to do so due to the fact that the problem occurred during non-working hours or at times when the facility was not accessible. Therefore, the possibility of carrying out remote operations on the circuit makes everything more reliable and controllable.

PoE protocol can work with two different standards[14] defining how power can be transmitted over Ethernet cables:

- IEEE 802.3af (15.4W/port)
- IEEE 802.3at (30.0W/port)

¹Simple Network Management Protocol (SNMP) is a networking protocol used for the management and monitoring of network-connected devices in Internet Protocol networks.

IEEE 802.3af Standard

Typical architecture for this standard consists of a Power Sourcing Equipment (PSE) that delivers electrical power to a connected Pod Devices (PD) over existing copper cables without interfering with the network traffic. Generally PSE device is referring to an Ethernet Switch supporting PoE of a PoE hub. Power is delivered either over data pairs (Alternative A) or spare pairs (Alternative B) of standard CAT-5 cabling (Alternatives A and B will be seen in the next sections according to the adopted solution).

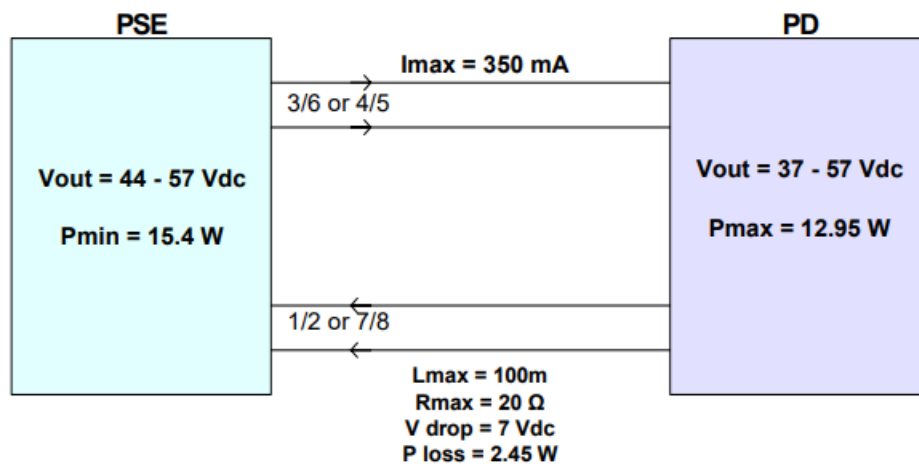


FIGURE 3.1: PSE and PD interconnection

The standard defines some electrical parameters to be kept in PoE design:

- **Operating Voltage:** Is normally 48 VDC, but it may vary between 44 to 57 VDC. In any case should be always be under the maximal SELV requirement of 60 VDC.
- **Maximal Current Generated:** is to vary between 350 and 400 mA. This level protects the Ethernet cables from over heating due to their parasitic resistance.
- **Carried Power:** According to the above values it is possible to reach up to 15.4 W in the PSE's port output. After cable loss, caused by parasitic resistance of about 20Ω for a pair, the maximal power a PD can count on is 12.95 W.

IEEE 802.3at Standard

- **Operating Voltage:** Same as the af standard
- **Carried Power:** Increases the maximum power to 30 W. It is commonly referred to as PoE+ or PoE Plus.

- **Compatibility:** Backwards compatible with IEEE 802.3af standard devices

PoE Module PEM3012C

On the basis of the project specifications and power calculations shown in Table 3.1 it can be seen that both standards satisfy the project requirements since the estimated absorbed power is less than 12W (considering that the estimated power has been greatly overestimated). In order to implement the PoE protocol on the project it was decided to purchase a ready-to-use PoE module, in this case the PEM3012C[15] produced by Infomart IT Solutions®.

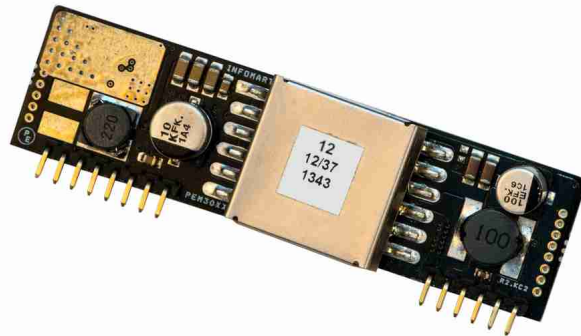


FIGURE 3.2: PEM3012C

There are several advantages to selecting a ready-made PoE module instead of drawing the circuit from scratch:

- **Time-Saving:** Designing a PoE circuit from scratch can be a time-consuming process. Selecting a ready-made module can save you the time and effort required to design and test the circuit.
- **Cost-Effective:** Ready-made modules can be a more cost-effective option since they are designed to be manufactured at scale, which can reduce the cost per unit.
- **Reliability:** These modules are designed and tested by experienced companies, which can result in a more reliable and stable circuit allowing to avoid potential design errors or compatibility issues.



- **Support:** Technical support and documentation, which can be helpful in case of problems during the integration of the module into the project.

The PEM3012C is a PoE Powered Device (PD) which has a complete compliance with the high power IEEE 802.3at PoE+ standard and it is designed to extract power from CAT5 Ethernet cable when sourced by both IEEE 802.3at and IEEE 802.3af compliant Power Sourcing Equipments (PSE). It is equipped with and high efficiency DC-DC converter which provides up to 30W of power in a well regulated, low noise and low ripple output with in-built in-rush current, overload and output short-circuit protection. Product features can be found in the Tab 3.1 and 3.2.

Parameter	Symbol	Units	Min.	Typ	Max.
Input Voltage (DC)	V_{in}	V	36	51	57
Under Voltage Lockout (DC)	V_{UVLO}	V	30	-	36
Input Current (DC)	I_{IN}	mA	100	-	600
Operating Temperature	T_{OP}	Celsius	-20	25	70

TABLE 3.2: PEM3012C Input Characteristics

Parameter	Symbol	Units	Min.	Typ	Max.
Line Regulation	V_{LNRG}			0.2%	
Load Regulation	V_{LDRG}			0.5%	
Output Ripple and Noise	V_{RIP}	mV_{p-p}		150	
Isolation Voltage (DC)	V_{ISOL}	V			1500
Temperature Coefficient (Slope)	TC	ppm/C		100	300
Output Short Circuit Duration		Sec			∞

TABLE 3.3: PEM3012C Output Characteristics

Pin description has been done in the Tab.3.5 . Some feature of this product will not be used, as the AT Detection pin, since they are not useful for this application. The AT Detection pin allows to the device to understand if the Powered Device (PD) is requiring more than 15.4W to the PSE and in this case to switch from IEEE 802.3af to IEEE 802.3at protocol. According to the estimated power consumption of the system, the 15.4W protocol is more than enough to supply the circuit, so it's not necessary to include the additional circuitry to use this feature. Switching to 30W mode is not only useless for this application, but also can make it more difficult to dissipate heat generated. According to thermal performance profile on the datasheet, the module performances start a degrade around $55^{\circ}C$.

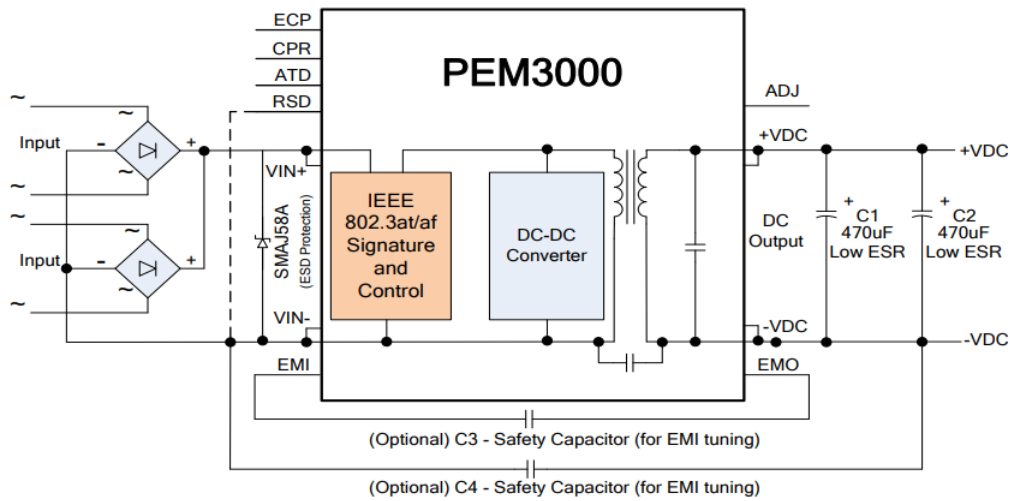


FIGURE 3.3: PEM3000 series block diagram and typical connections

	INPUT	Description
1	EMI	Additional EMI filtration. Must be connected to EMO pin through safety capacitor
2	VIN+	Connected to the positive output of rectifiers
3	VIN-	Connected to the negative output of rectifiers (internally connected to pin 4)
4	VIN-	Connected to the negative output of rectifiers (internally connected to pin 3)
5	ATD	AT Detect Pin. This pin is capable to detect if af or at protocol is used
6	RSD	This pin can be used for remotely shutting down the module from the target device
7	NC	
8	CPR	Remote Shutdown PIN

TABLE 3.4: Input Pin Description

	OUTPUT	Description
9	EMO	Additional EMI filtration. Must be connected to EMI pin through safety capacitor
10	+VDC	Regulated output from DC/DC Converter (internally connected to pin 11)
11	+VDC	Regulated output from DC/DC Converter (internally connected to pin 10)
12	OADJ	The output voltage can be adjusted from its nominal value
13	-VDC	Ground return from the +VDC output (internally connected to pin 14)
14	RSD	Ground return from the +VDC output (internally connected to pin 13)

TABLE 3.5: Output Pin Description

Choosing the Bridge Rectifiers

It's important to correctly choose the bridge rectifiers which appear in Fig.3.3 on the left side. As said before, two ethernet system installation are currently existing[16]:

- Mode A - Data and Power are travelling on the same path (it uses only 2 differential pairs).
- Mode B - Ethernet signal is isolated from power supply using 4 different pairs.

Since there is no standard at the time, to operate correctly in legacy PoE systems, an Ethernet Powered Device (PD) must allow for both Mode A and Mode B connections as well as positive and negative supply polarity. A common way to handle these issues is to use two bridge rectifier diodes, one for Mode A and one for Mode B.

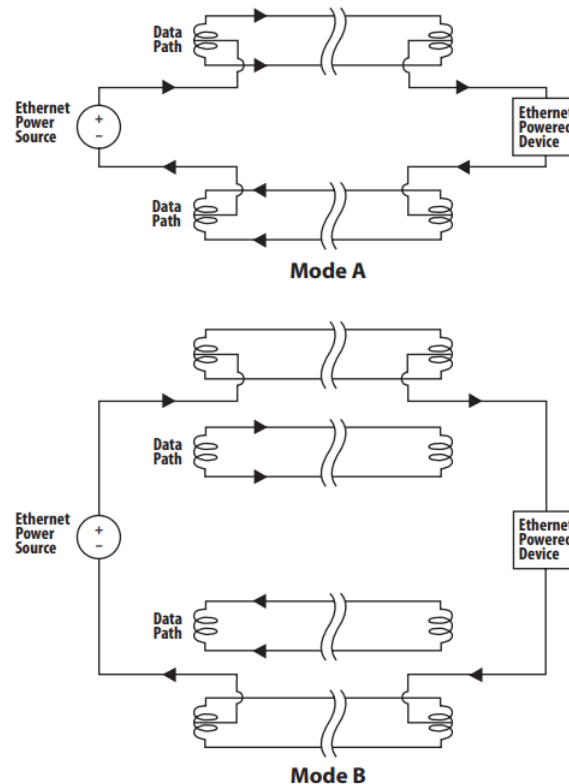


FIGURE 3.4: Mode A and Mode B

The diode bridges allow either supply polarity to be accepted for either mode. Usually, diode rectifiers are used for AC rectification, so the main problem here is to understand how to relate datasheet parameters to operation in a DC system such as PoE. First, the voltage drop across the rectifier diodes must be small. This requires the use of Schottky bridge rectifiers. PoE systems run at 57 VDC (max) so a bridge rated at 100 V will provide plenty of margin. But how much PoE current this bridge rectifier diode supports? What is the Maximum Average Forward Rectified Current rating and how is it measured? During a typical AC cycle where the voltage signal is a sine wave, the diodes charge the load capacitor (visible in figure 7) during each half-cycle. The resistive load draws current from capacitor, reducing the output voltage. At the next cycle, the capacitor is charged up again. Thus, the output voltage is a DC level with a ripple voltage superimposed on it. The average current through the diodes is what is required to replenish the average current drawn by the load. Since this is a full-wave rectifier, only one pair of diodes conducts during each half-



cycle. So, for instance, considering an application where the load circuits require 1A, as result each half-cycle the two conducting diodes must supply an average current of 1A. Since each diode is turned on only half of the time, the long-term average of the current through each diode is only 0.5A. During AC transmission, it's also important to be careful about peak voltage levels since the diode current is extremely pulse-like as it charges the capacitor back to its peak voltage level. This current is very much larger than its average current. But this is not out of care since PoE is DC. Finally, the last thing to consider is that when diodes are conducting, the capacitor is completely discharged, which means that the diodes must tolerate the resulting huge inrush current. As already mentioned, receiving power from PoE is very different power from AC since there is no sinewave. The current is DC (assuming the load is fixed). The maximum average forward rectified current is just the expected DC load current. However, in this case only one of the diode pairs is on and always supplies the entire load on its own. The other half of the bridge is always off (because PoE never changes polarity). So, in this case the single diodes are always carrying 1A (differently from the case of AC where they were carrying an average of 0.5A). So, in this case the entire bridge still supplies the same average current but the individual diodes must support an higher average current. The capacitor will remain charged and mainly acts as a PoE filter.

Type	Power Class	Max. Available PoE Power	Min. Available PoE Power	Max. PoE Current per Pair	Min. Bridge Average Current	Bourns® Suggested Model
1	0	15.4 W	13 W	350 mA	1 A	CD-HD01
1	1	4 W	3.8 W	90 mA	1 A	CD-HD01
1	2	7 W	6.5 W	160 mA	1 A	CD-HD01
1	3	15.4 W	13 W	350 mA	1 A	CD-HD01
2	4	30 W	25.5 W	600 mA*	2 A	CD-HD201
3	5	45 W	40 W	450 mA**	2 A	CD-HD201
3	6	60 W	51 W	600 mA**	2 A	CD-HD201

Table 2 - Suggested Bridges for Various PoE Types and Classes

FIGURE 3.5: Bourns® Suggested rectifiers according to PoE types and Classes

According to this, the chosen rectifier for this application is the 2W01MG from Multi-comp Pro.

Configuration and Testing

PEM3012C supports different power injection options: Data/Signal pair (Mode A) and Spare Pair (Mode B).

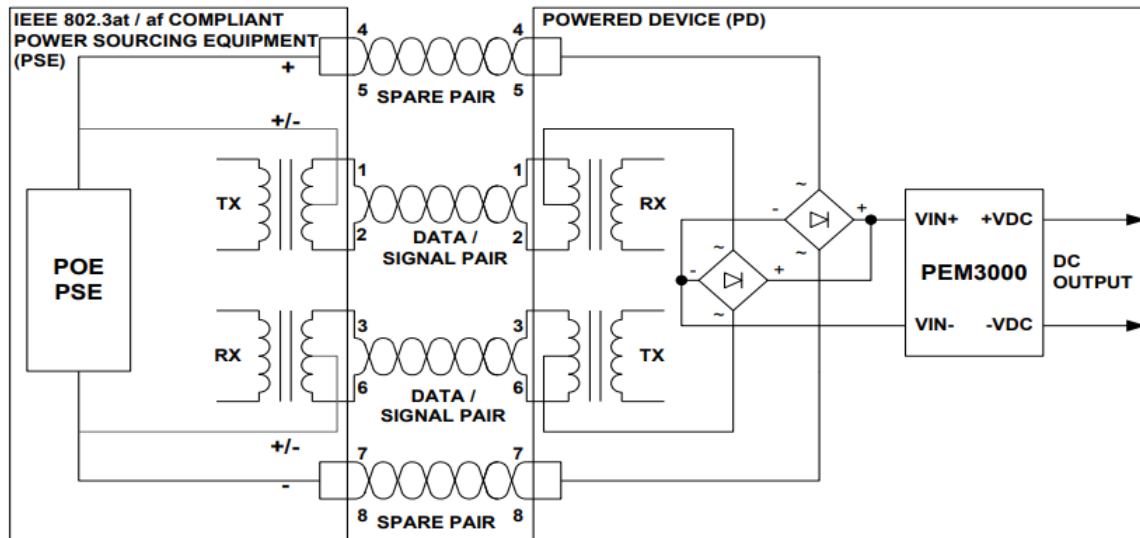


FIGURE 3.6: PEM3000 series typical system configuration

After the analysis of the Fig.3.3 circuit, a prototype has been made in order to test the module functioning. The PEM3012C has been soldered on a testing board and the additional circuitry has been added as in Fig.3.3.

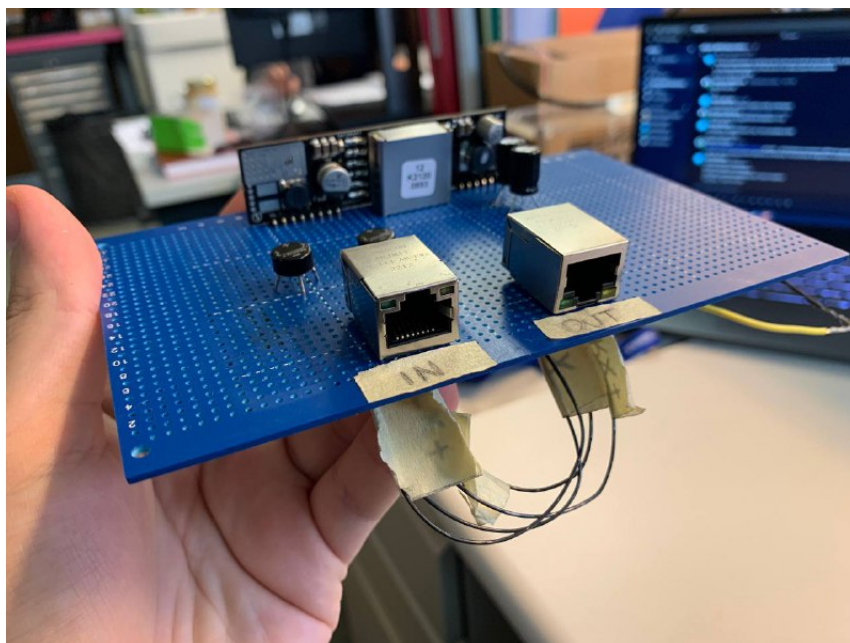


FIGURE 3.7: Test board for PEM3012C



Modes of Operation

PEM3000 series has five operating modes:

- Reset - All PEM3000 blocks are disabled
- Detection - The PEM3000 presents a valid POE PD response to a detection request from an IEEE compliant PSE
- Classification - PEM3000 PD section indicates power requirements to the PSE via Single-Event Classification for IEEE802.3af or a 2-Event Physical Layer (Layer 1) Classification for IEEE 802.3at.
- Idle - The PEM3000 enters this state after Classification and remains until full-power input voltage is applied.
- On - The PEM3000 PD is enabled and supplies power to the DC-DC controller and the local application circuitry.

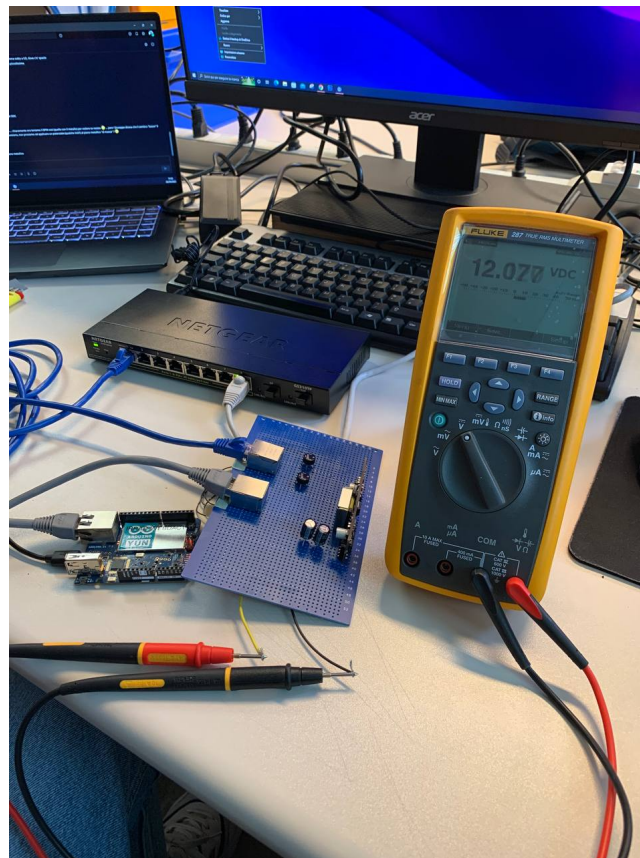


FIGURE 3.8: Test result for PEM3012C

Not only the input connector but the output one as well is an RJ45 one. This has been done in order to test the data communication from the module. The test has been performed using a Netgear GS310TP PoE+ Switch and directly connecting the switch to the input RJ45 port of the circuit. Fig. 3.8 shows how the system is actually working giving in output the expected voltage of 12V. In term of accuracy the output voltage is acceptable since multimeter indicates 12.077V which can perfectly fit with the project specifications. In case it becomes necessary to adjust the output voltage, it is possible to do it through the OADJ pin, which allows the output voltage to be increased or decreased from its nominal value using 1/16W power rating or greater and 1% tolerance resistor. The resistor must be connected between the OADJ pin and either the +VDC or -VDC pin.

Wiring Diagram

The following images are a description of how the PEM3012C has been integrated in the final project. Fig. 3.9 is basically a reproduction of the Fig. 3.3 schematic where components D2 and D3 are rectifiers and C3, C4 are the output capacitances. RSD pin has been configured as well.

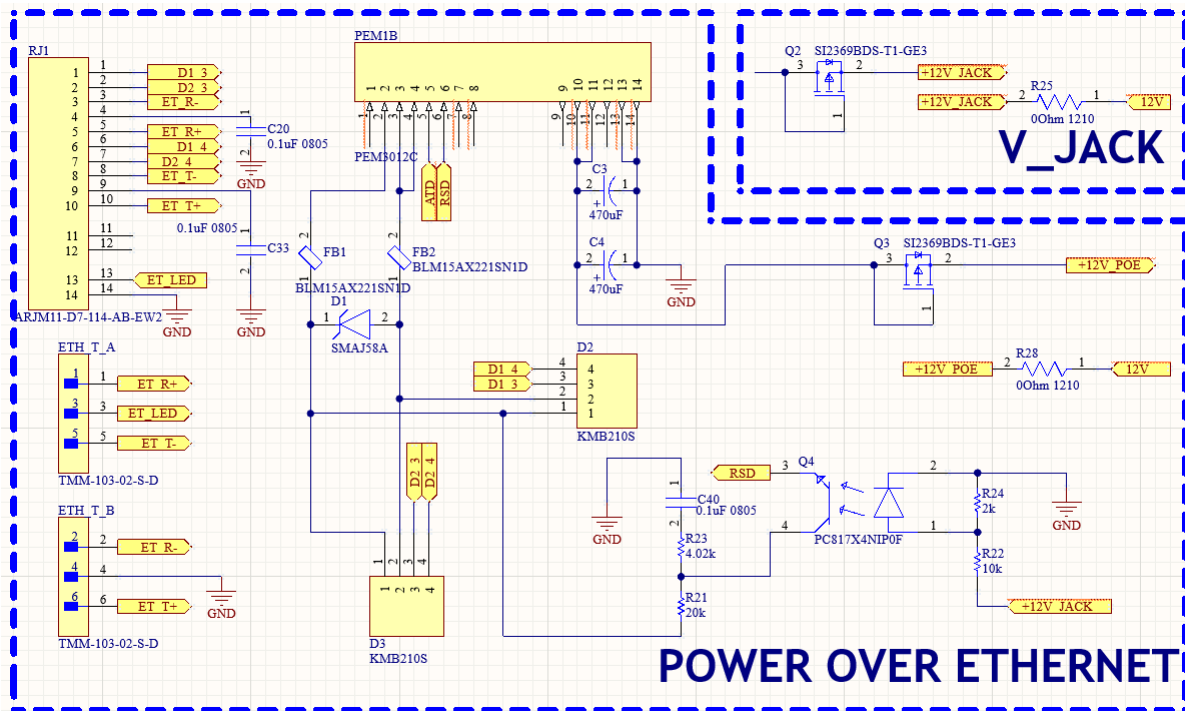


FIGURE 3.9: PEM3012C Wiring Diagram

PCB Design

Fig. 3.10 is a representation of the PCB routing part. PEM3012C is on the top part, while the RJ45 connector is the component RJ1 on the right. Notice that the PCB is a 4 layers one but in this picture the middle layers are hidden in order to have a better view of the routing. According to PEM3012C datasheet a power plane heat sink has been created on the output part (left side between output pins and C3,C4 capacitors). Thermal performances of the PoE module can be improved through the power plane heat sink, which is a relatively simple method to draw some heat away from the module. Output capacitors have been places the closest possible to the output pins, as suggested on the manual.

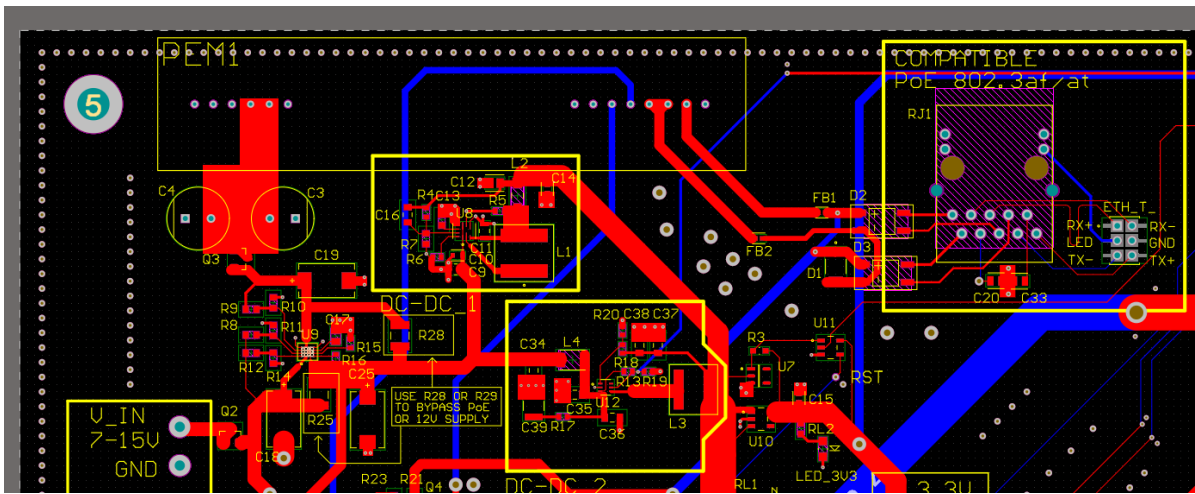


FIGURE 3.10: PCB routing for PEM3012C



FIGURE 3.11: PCB 3D view for PEM3012C

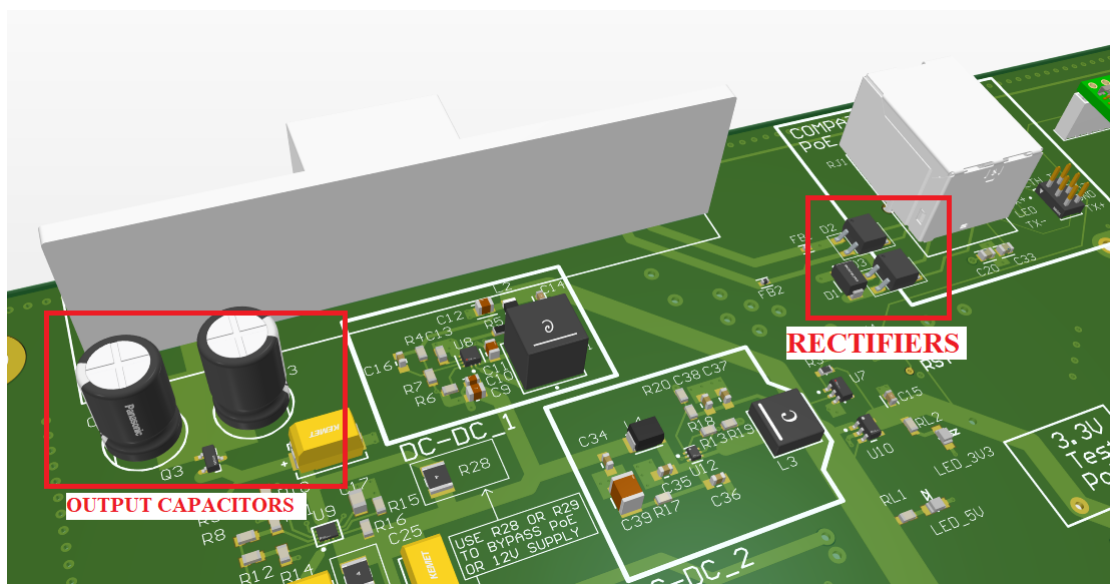


FIGURE 3.12: PEM3012 3d View with focus on output capacitors and rectifiers



3.3 DC Power Supply

Although Power Over Ethernet has been selected as the primary power source, the final project also includes an external power supply connection in case PoE supply is not working properly. The backup solution was implemented to ensure uninterrupted operation of the circuit, particularly in critical situations where downtime can be costly or even dangerous. In addition, the separate input for the backup supply allows for easy switching between the main and backup supplies, ensuring seamless operation in case of power loss or fluctuations. By including a backup power supply in the circuit design, the risk of downtime and associated costs can be mitigated, improving the overall reliability and performance of the system. In addition, the circuit was equipped with a voltage selector ICs, which has made it possible to automate the process of selecting the power supply voltage so that when using PoE, in the event that an external power supply is suddenly connected, the system is able to independently establish which of the two power supplies to use. In particular, it was decided to prefer external power supply over PoE if both are connected at the same time. For additional informations refer to 3.4.1 subsection.

3.3.1 Voltage conversion from 12V to 5V

In order to design the power supply for the circuit, the *WEBENCH Power Designer* tool from Texas Instruments was used. This tool is a web-based design platform that allows users to generate custom power supply designs based on their specific requirements. After entering the necessary input parameters, such as input voltage, output voltage, and load current, the tool recommended two components, the TPS62913RPUR and TPS564247DRLR.

Texas Instruments TPS62913RPUR

The TPS62913RPUR [17] is a high-frequency synchronous buck DC-DC converter designed and manufactured by Texas Instruments. It is designed for use in applications that require high efficiency, small size, and low electromagnetic interference (EMI). It over an input voltage range of 3V to 17V and can provide an output voltage range of 0.8V to 5.5V. The converter can deliver up to 3A of output current and has a high efficiency of up to 95% over a wide load range. The switching frequency of the converter is fixed at 2.2MHz, which helps to reduce the size of the external components required for the design. The TPS6291 is available in a small 6-pin SOT-23 package, making it ideal for use in space-constrained applications such as smartphones, tablets, and other portable devices. With its high efficiency, small size, and advanced features, the TPS6291 is a versatile and reliable

solution for a wide range of power supply applications.

Pin Configurations and Functions

Pin configuration and functions of the TPS62913 are described in the list below:

- EN/SYNC : Enable/Disable pin including threshold comparator. It allows do disable/enable the device connecting it to low/high respectively. When the device is disabled, this pin is internally connected to a $500k\Omega$ pull-down resistor.
- SW : Switch pin of the power stage.
- VO : Output voltage sense pin.
- PGND : Power Ground connection.
- PG : Open-drain power-good output. This pin is pulled to GND when V_{OUT} is below the power-good threshold. It requires a pullup resistor to output a logic high. It can be left open or tied to GND if not used.
- VIN : Power supply input voltage pin.
- PSNS : Power sense ground.
- NR/SS : A capacitor connected to this pin sets the soft-start time and low frequency noise level of the device.
- FB : Feedback pin of the device
- S-CONF : Smart Configuration Pin, to configure different operation modes of the device.

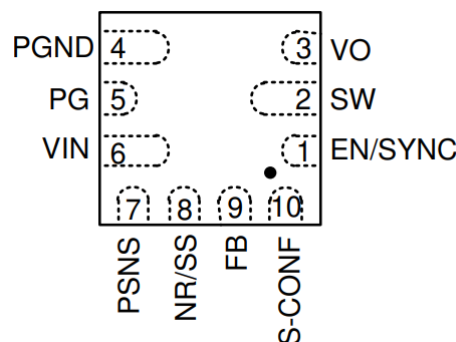


FIGURE 3.13: 10-Pin QFN RPU Package (Top View)

-	NAME	MIN	NOM	MAX	UNIT
V_{IN}	Input Voltage	3.0		17	V
V_{OUT}	Output Voltage	0.8		5.5	V
C_{IN}	Effective Input Capacitance	5	10		uF
L_1	Effective Output Inductance	-30%	2.2 / 4.7	20%	uH
C_{OUT}	Effective Output Capacitance	40	47	80	uF
L_f	Effective Filter Inductance	0	10	50	nH
C_f	Effective Filter Capacitance	20	40	160	uF
I_{OUT}	Output Current for TPS62913	0		3	A
T_J	Junction Temperature	-40		150	°C

TABLE 3.6: Recommended Operating Conditions

Wiring Diagram

Circuit design for the TPS62913RPUR has been done using *WEBENCH Power Designer* tool from Texas Instruments. After inserting the proper specifications, the tool gave as result the circuit in Fig.3.14

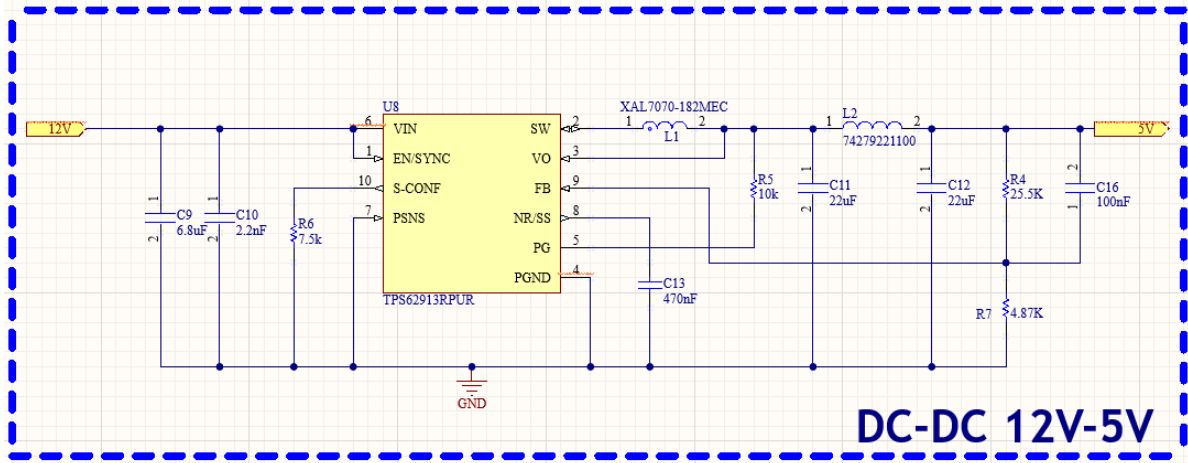


FIGURE 3.14: TPS62913RPUR Wiring Diagram

Texas Instruments TPS56424

The TPS56424[18] is a highly integrated synchronous step-down DC-DC converter manufactured by Texas Instruments. It is designed to provide high efficiency, low EMI, and high reliability in a compact package. It operates over an input voltage range of 3V to 16V and can provide an output voltage as low as 0.6V and up to 7V. The converter can deliver up to

4A of output current and has a high efficiency of up to 95% over a wide load range. The switching frequency of the converter is fixed at 1.2MHz. The device is available in 1.6-mm x 1.6-mm SOT-563 package and has an optimized pinout for easy PCB layout. With its high efficiency, advanced features, and robust protection, the TPS56424 is a versatile and reliable solution for a wide range of power supply applications. The TPS6291 includes a number of built-in protection features such as thermal shutdown, over-current protection, and under-voltage lockout to prevent damage to the device and the system it is powering. The converter also includes a power-good (PG) output to indicate when the output voltage is within regulation.

Pin Configuration and Function

Pin configuration and functions of the TPS56424 are described in the list below:

- VIN : Power supply input voltage pin.
- EN : Enable input to converter. Driving EN high enables the converter.
- SW : Switch node connection between the high-side NFET and low-side NFET.
- GND : Ground pin source terminal of the low-side power NFET as well as the ground terminal for controller circuit.
- AGND : Ground of internal analog circuitry. Connect AGND to the GND plane.
- FB : Converter feedback input. Should be connected to the output voltage with a feedback resistor divider.

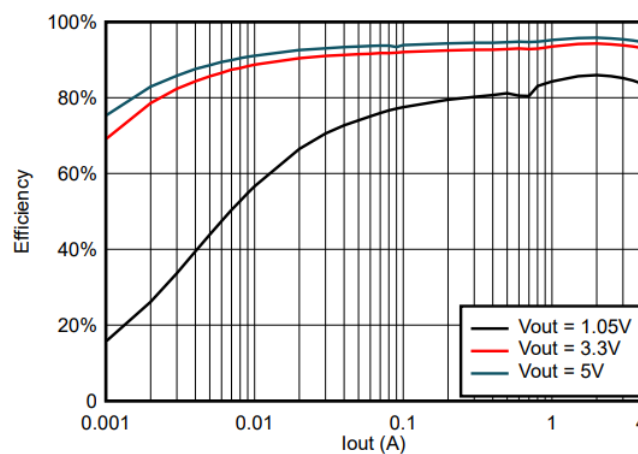


FIGURE 3.15: Efficiency Curve at $V_{IN} = 12V$

-	NAME	MIN	MAX	UNIT
V_{IN}	Input Voltage	-0.3	18	V
EN	Input Voltage	-0.3	6	V
SW	Output Voltage	-2	18	V
SW (< 20 ns)	Output Voltage	-6.5	20	V
T_{STG}	Storage Temperature	-55	150	°C
T_J	Junction Temperature	-40	150	°C

TABLE 3.7: Recommended Operating Conditions

Wiring Diagram

Circuit design for the TPS62913 has been done using *WEBENCH Power Designer* tool from Texas Instruments. After inserting the proper specifications, the tool gave as result the circuit in Fig.3.16

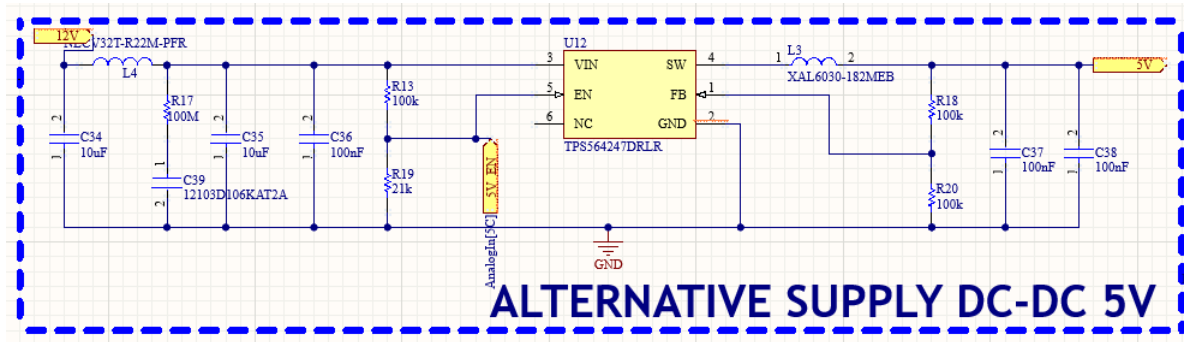


FIGURE 3.16: Schematic View for TPS56424

PCB Design

Fig. 3.17 and 3.18 help to understand how the Power Supply part has been implemented on the final board.

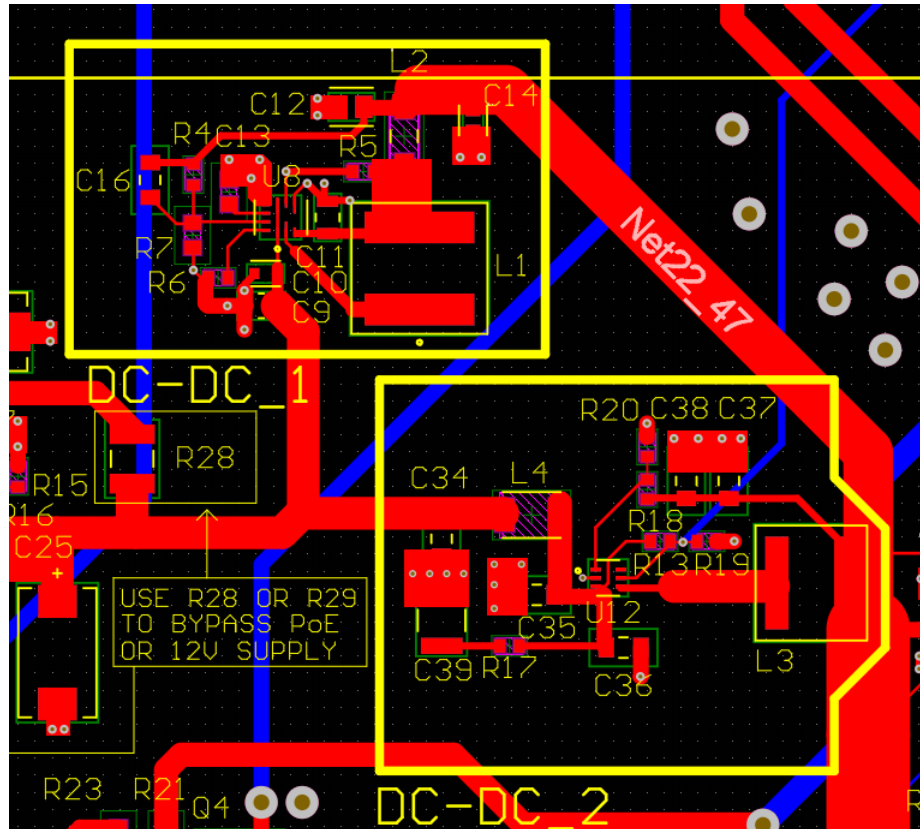


FIGURE 3.17: PCB View for TPS56424

The two supplies have been done in such a way that they could be switched quickly just unsoldering one inductor between L2 and L3. These inductors are directly connected on the main track *Net22-47*, so unsoldering them means disconnecting the whole related supply part. The reason behind this choice is the possibility to have different solutions to supply the circuit in case one of these becomes unavailable, out of stock or any other problem.

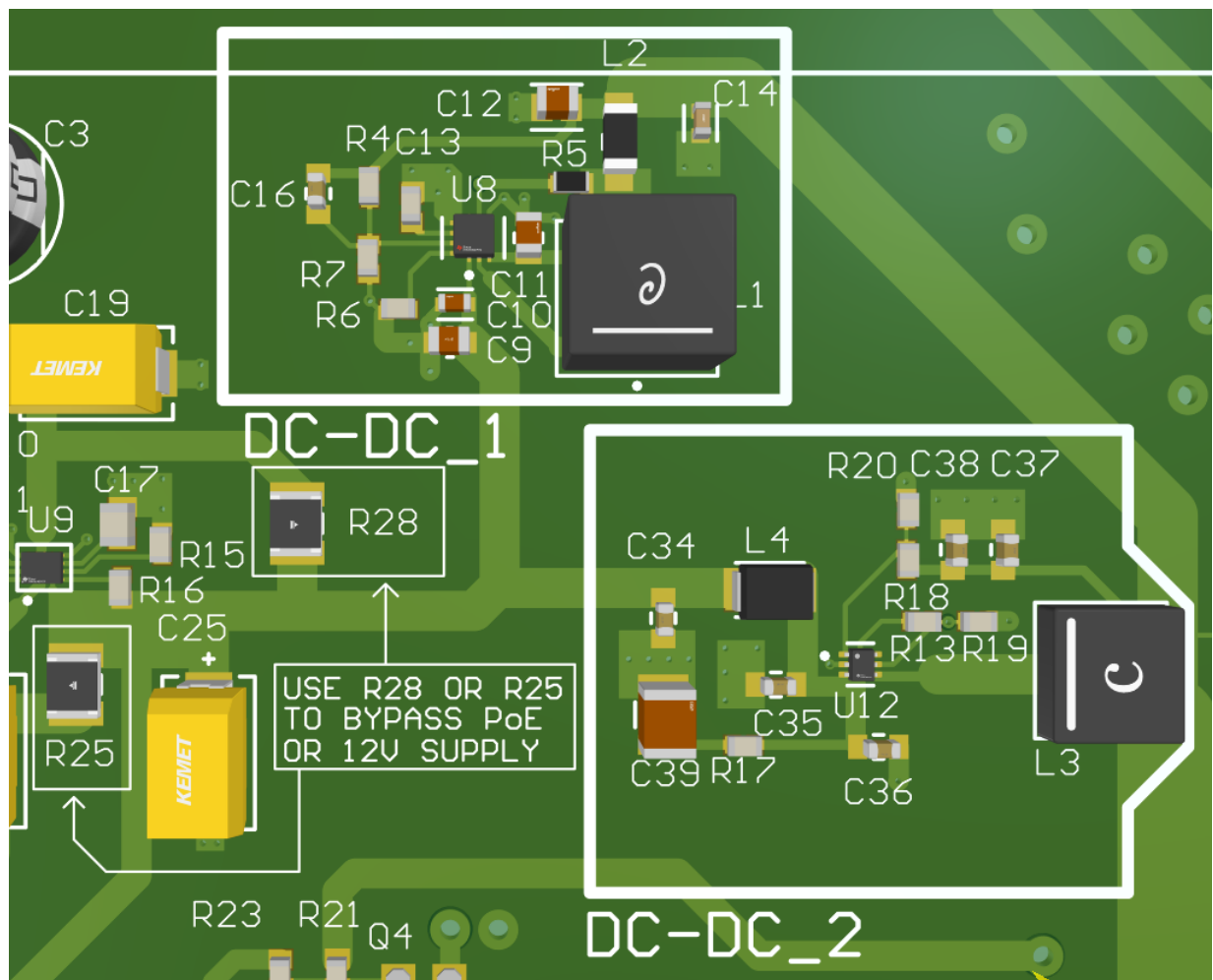


FIGURE 3.18: 3D PCB View for TPS56424

3.4 Low Drop-Out Regulator - 3.3V Supply

As seen above, most of the wiring diagram requires a 5V power supply, but the DDC232 requires a 3.3V digital power supply too. Furthermore, also all digital circuitry to the operation of the DDCs, such as the clock generation circuit or other integrated circuits operates at 3.3V. In order to achieve this result, a Low Drop-Out Regulator has been chosen to reduce the 5V voltage coming from the main supply circuit. The selected LDO for this purpose is an TLV75733PDBVR with excellent performance characteristics, low dropout voltage, and robustness. The TLV75733PDBVR provides a fixed output voltage of 3.3V. It has a low dropout voltage, which is the minimum voltage difference between the input and output of the regulator for it to operate properly and for this is typically around 425mV at a 1A load current. The maximum output current it can deliver is 1A, making it suitable for powering a wide range of low-power devices and it can accept input voltages between 1.45V and 5.5V. Other features and specifications of this LDO can be found in the datasheet [19].

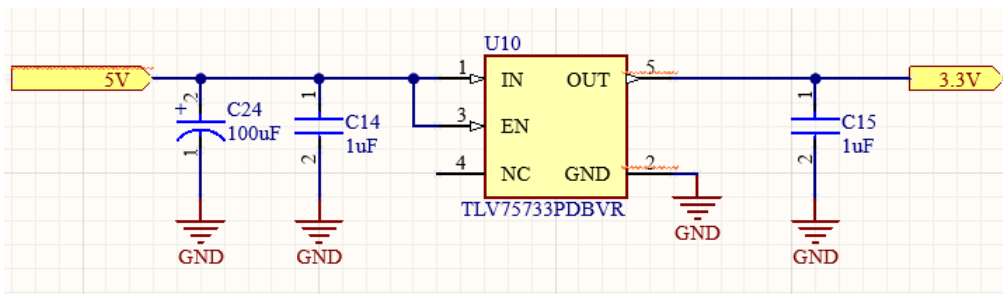


FIGURE 3.19: Typical configuration for TLV757P

3.4.1 Additional Supply Circuits

Supply Selector

As seen before, the primary power source utilized is based on Power over Ethernet (PoE) protocol, which provides power and data transmission over a single Ethernet cable. As a backup measure, a conventional 12V analog power supply has been incorporated.

To enable seamless switching between the PoE and analog 12V supply, a Supply Selector circuit has been employed. Specifically, the TPS2120YFPR component from Texas Instruments has been selected for this purpose. The TPS2120YFPR is designed to automatically switch between two power sources, allowing the circuit to smoothly pass from the PoE to the analog 12V supply. This solution helps preventing any disruptions in the functionality of the board enhancing the overall reliability and performance of the electronic

project[20].

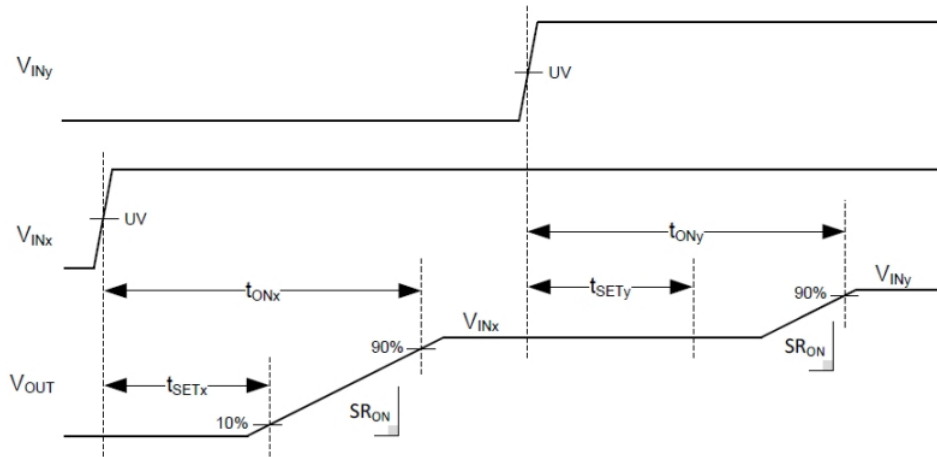


FIGURE 3.20: TPS2120 Timing Diagram

Priority can be automatically given to the highest input voltage or manually assigned to a lower voltage input. The TPS2120 will automatically select the first source to become valid ($INx > UV$ and $INx < OV$). An external capacitor (C_{ss}) will be used as a timer to wait for the input to finish setting (t_{SETx}). When the setting timer has expired, C_{ss} will continue to charge and set the output slew rate (SR_{ON}) for a soft start. After the total turn on time (t_{ONx}), soft start will not be used again for INx until it ceases to be valid ($INx < UV$ or $INx > OV$). When the second source becomes valid ($INy > UV$ and $INy < OV$), the external capacitor will be used again for a second setting time (t_{SETy}). After t_{SETy} , the TPS2120 will decide whether to continue sourcing the first source, or switchover to the second source. If the second source is selected at the end of t_{SETy} , then the C_{ss} will be reused to set the output slew rate (SR_{ON}) for a second soft start. After the total turn on time (t_{ONy}), soft start will not be used again for INy until it ceases to be valid ($INy < UV$ or $INy > OV$). In Fig.3.18 is possible to notice the presence of R28 and R25 resistors. They are very useful since unsoldering or soldering them separately is possible to switch between PoE or normal supply. This solution should not be useful for the application since the supply selector circuit described right now should be already enough for this. However, as already done with other parts of the project, this is a backup solution in case the supply selector circuit is not going to work.

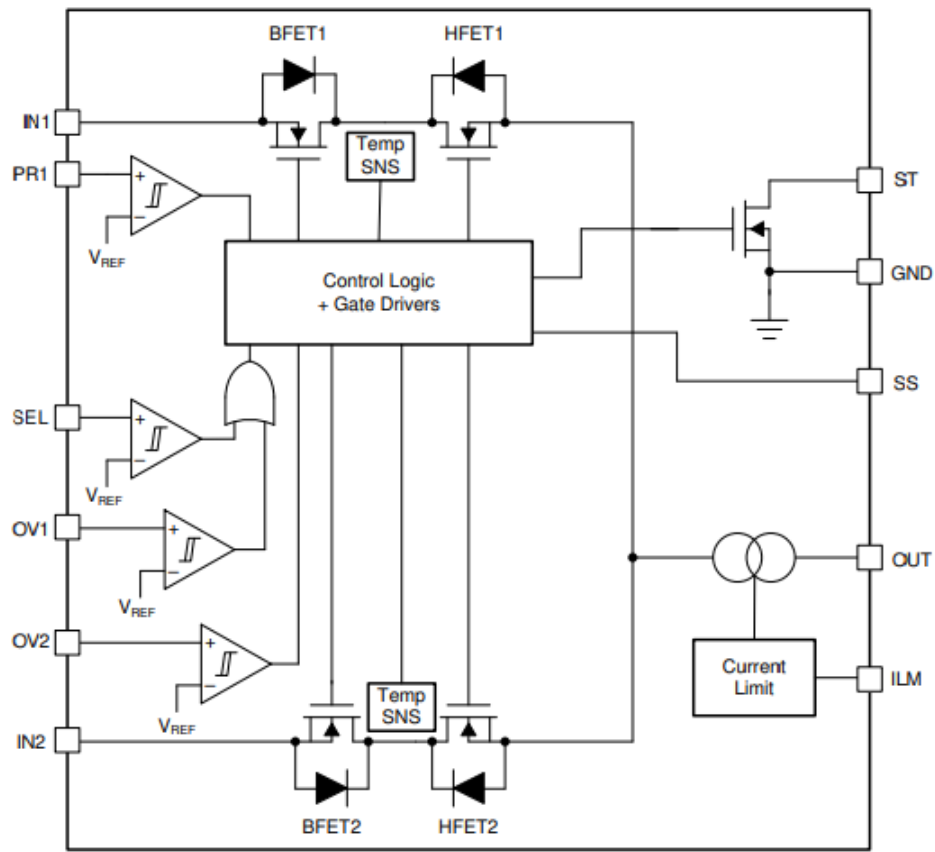


FIGURE 3.21: TPS2120 Functional Block Diagram

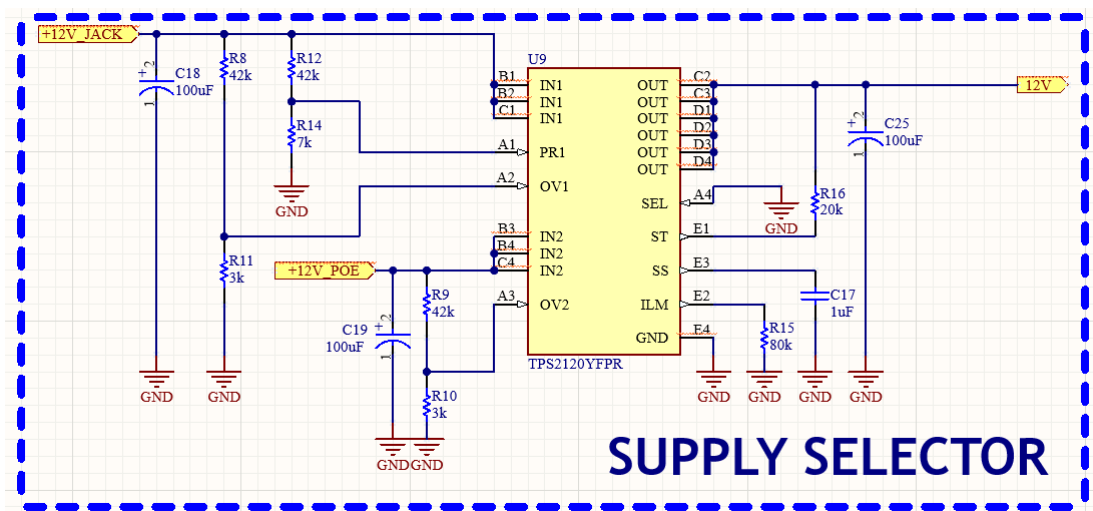


FIGURE 3.22: TPS2120 Schematic

Voltage Supervisor

The inclusion of a voltage supervisor serves a crucial purpose in maintaining the reliability and proper functioning of the system. Fluctuations in the power supply can adversely affect the performance of electronic components, leading to potential data corruption or system failures. By actively monitoring the voltage, the supervisor provides an added layer of protection against such issues.

The voltage supervisor acts as a safeguard, triggering an alert or taking corrective actions if it detects any voltage fluctuations beyond acceptable limits. This real-time monitoring allows for timely intervention and prevents potential damage to the connected devices or critical data loss.

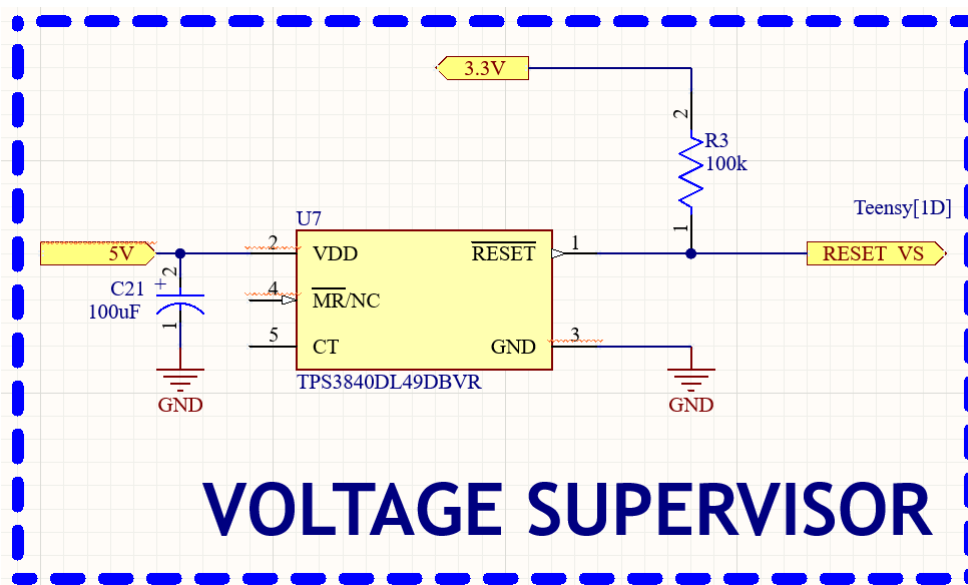


FIGURE 3.23: TPS3840DL49DBVR Schematic

The chosen component for this purpose is a TPS3840DC49DBVR by Texas Instruments, which is a voltage supervisor integrated circuit (IC) that is commonly used to monitor power supply voltages in electronic systems. It ensures the stability and reliability of the system by detecting and responding to voltage fluctuations. The IC is designed for a wide range of applications and offers features such as accurate voltage monitoring, programmable threshold settings, power-on reset functionality, reset timeout capability, low power consumption, and a compact package.

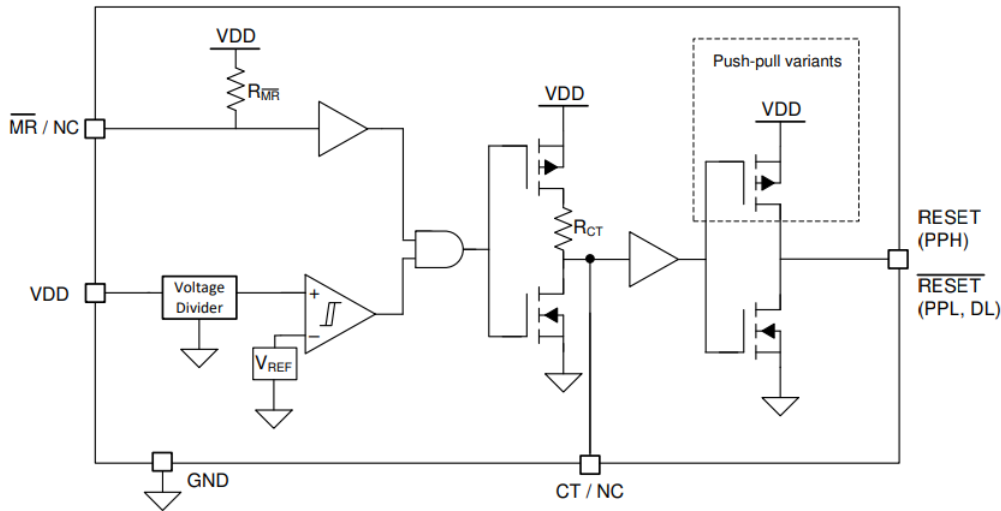


FIGURE 3.24: TPS3840DL49DBVR Block Diagram

As shown in Fig.3.24 the VDD is monitored by the internal comparator on which the inverting terminal is placed at a reference voltage. If the VDD voltage is higher than the reference one, the comparator output is high, activating the AND logic and consequently opening/closing Mosfets on the CMOS inverters after in order to generate a RESET signal. The internal comparator has a built-in hysteresis to avoid erroneous output reset release. Specifications and additional details can be found in the datasheet[21].

3.4.2 Clock Generation Circuit

For the clock generation circuit it is necessary to come back to Chapter 2, where the component DDC232 by Texas Instruments has been described. In particular, the internal switching network in Fig.2.5 is controlled externally with the convert pin (CONV) and the system clock (CLK). As shown in Fig.2.4 CONV signal must be synchronized with the rising edge of CLK. Moreover, the digital interface of the DDC232 outputs results via a synchronous serial interface consisting of a data clock (DCLK) and other digital pins. Consequently, the CLK and DCLK frequencies need not be the same. The clock source must be a free-running one, in order to not start and stop the CLK signal between conversions. Following this discussion, an integrating circuit has been chosen as a clock generation source, in particular the SI5351A-B-GTR by Skywork Solutions Inc.[22]. This is a configurable clock generator that is ideally suited for replacing crystals, crystal oscillators, VCXOs, phase-locked loops (PLLs) and fanout buffers in cost-sensitive applications.

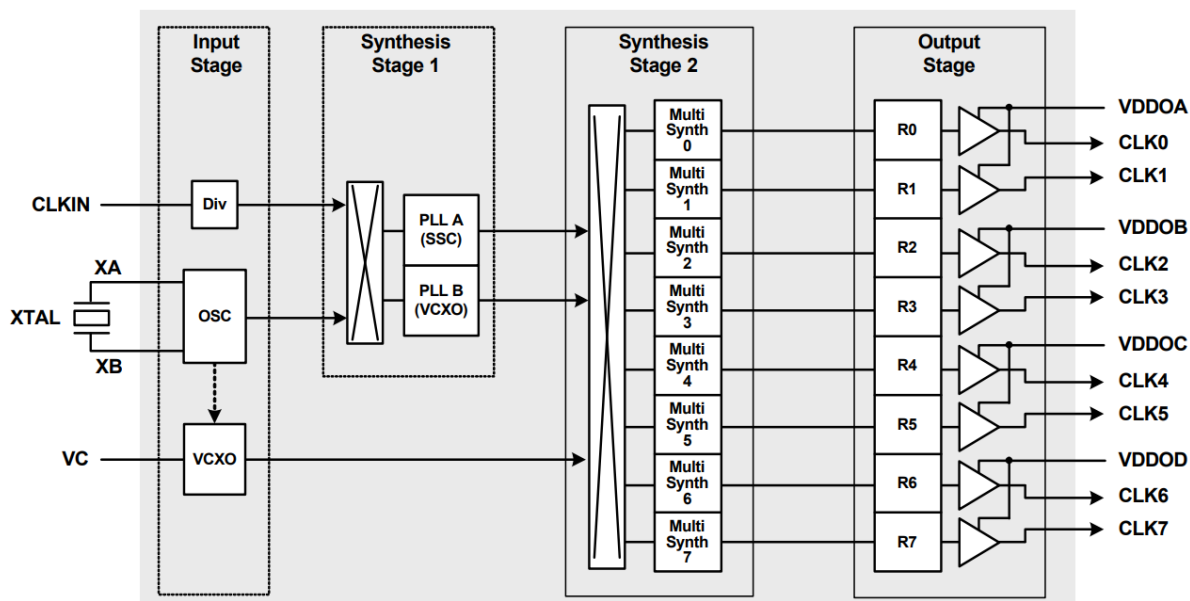


FIGURE 3.25: Si5351 Block Diagram

The input stage (Fig.3.25) needs to be connected to an external crystal (XTAL) and to a control voltage (VC). The IC uses a fixed-frequency standard AT-cut crystal as a reference to the internal oscillator. The output of the oscillator can be used to one or both PLLs in the Synthesis stage 1 for generating asynchronous clocks. The output frequency of the oscillator will operate at the crystal frequency, usually a 25 Mhz or 27 Mhz. There is no need to use external components since the IC is already equipped with internal load capacitors. Regarding the Voltage Control Input (VC), the VCXO architecture allows to eliminate the need for an external pullable crystal. Only a standard, low-cost, fixed frequency (25 Mhz-27 Mhz) AT-cut crystal is required. So this basically allows to generate multiple output frequencies simply controlling with the same control voltage applied to the VC pin.

The first stage uses PLLs to multiply the lower frequency input references to a high-frequency intermediate clock. The second stage uses high-resolution MultiSynth fractional dividers to generate different output frequencies. Each of the PLLs can lock to the CLKIN or the XTAL input thanks to a crosspoint switch at the input on the first stage. This is very important since allows each of the PLLs to lock to a different source in order to generate independent and free-running and synchronous clocks. There is another crosspoint switch on the second stage which allows any of the MultiSynth to connect to PLL A or PLL B. Thanks to this architecture, each output can generate synchronous or no-synchronous clocks, with or without spread spectrum and with the flexibility of generating non-integer related clock frequencies at each output.



Finally, on the output stage, they are additional integer division in order to generate output frequencies as low as 2.5 kHz. Thanks to this high resolution and flexible synthesis architecture, the Si5351 is capable of generating synchronous or free-running non-integer related clock frequencies at each of its outputs.

I²C Interface

Many of the functions and features of the Si5351 are controlled by reading and writing to the RAM space using the I^2C interface. This operates in slave mode with 7-bit addressing and can operate in Standard-Mode (100 kbps) or Fast-Mode (400 kbps) and support burst data transfer with auto address increments. Both the SDA and SCL pins must be connected to the VDD supply via an external pull-up as recommended by the I^2C specification.

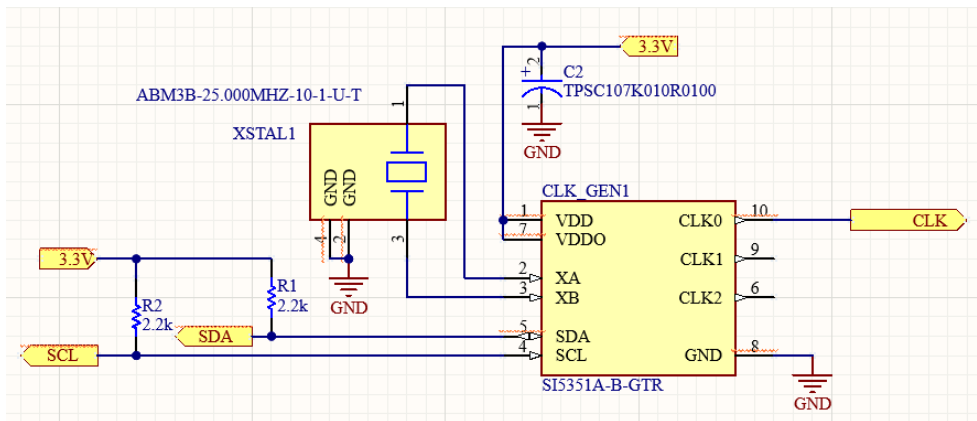


FIGURE 3.26: Si5351 Wiring Diagram

The device's default configuration is stored in a non-volatile memory (NVM). It's a one time programmable (OTP) memory which can store a custom user configuration at power-up. During a power cycle the contents of the NVM are copied into a random access memory (RAM), which sets the device configuration that will be used during normal operation. Any changes to the device configuration after power-up are made by reading and writing in the RAM through the I^2C interface. The register configurations and the write/read operations are described in the datasheet and will not be part of this document.

Fanout Buffer

It must be taken into consideration that the clock signal generated by the component described above needs to be distributed among the various interposer circuits in order to provide a stable clock signal without delays to the 5 DDC232 components. For this reason



it was decided to use a fanout buffer to distribute the clock signal among the various ICs and this solution offer several advantages:

- **Signal Integrity:** A fanout isolates the clock generator from the load, reducing several issues like reflection, impedance mismatches and signal degradation due to capacitive load of each IC's input.
- **Timing Accuracy:** Clock signals are critical for synchronous operations in digital circuits. If the clock edges become distorted due to the load, the timing of different ICs can be affected. A fanout buffer helps preserve the precise timing characteristics of the clock signal by ensuring consistent edges across all outputs.
- **Reduced Cross-Talk:** When multiple ICs share a common clock signal without buffering, the interactions between the loads can introduce cross-talk, which refers to unwanted coupling of signals between close traces or components. A fanout buffer reduces cross-talk by electrically isolating each output, minimizing signal interference.

So in general, using a fanout buffer improves the reliability, accuracy and performance of clock distribution in the circuit. The selected component for the fanout feature was the NB3V1106CDTR2G by On Semiconductors, a modular, high-performance, low-skew, general purpose LVCMOS clock buffer[23].

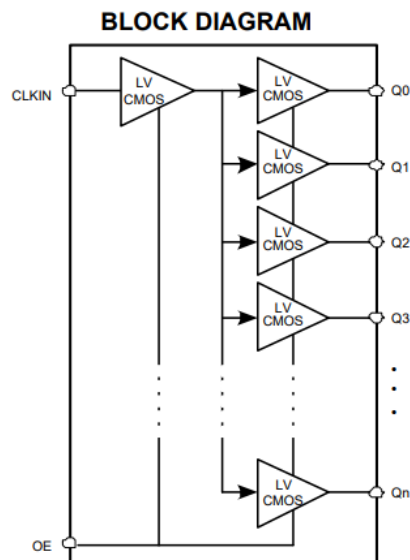


FIGURE 3.27: NB3V1106CDTR2G Block Diagram

Some of the main features of this component are listed below:

- Operating Temperature Range: -40°C to 105°C
- Output-to-Output Skew: $< 50\text{ps}$
- Additive Jitter: $< 200\text{fs}$
- Supply Voltage: 3.3V, 2.5V or 1.8V
- $f_{max} = 250\text{ MHz}$ for 3.3V, 180 MHz for 2.5V, 133 MHz for 1.8V

3.4.3 CONV Signal

According to the DDC232 datasheet, the CONV signal is a really important one, since it puts the DDC232 into the integration mode and consequently allows the integration of the signal before sending it to the Sigma-Delta ADCs. For the best noise performances, it is recommended to synchronize the CONV signal to the rising edge of the CLK, as shown in Fig.2.4. In order to achieve this result, a positive edge triggered D Flip-Flop has been used. In this way, the CONV signal will change his status every time a rising edge of the CLK signal comes, thus respecting the behaviour described in the manual.

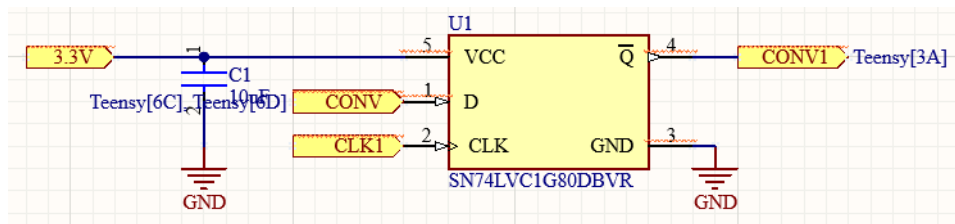


FIGURE 3.28: CONV signal wiring diagram

The final motherboard wiring diagram and pcb is shown in Appendix A at the end of this document.

3.5 Interposer Circuit

As mentioned above, the project includes five smaller interposer boards that will be placed as shields, thus interfacing the motherboard with the DDC232 and allowing communication between them. The choice of creating interposer boards as shields allows to place them easily and quickly, thus simplifying the assembling procedure of the motherboard and providing an easy maintenance in case of malfunctioning. As first, the choice of connector is fundamental since this allows to connect the interposer board to the motherboard and it needs to be an hot-swap connector in order to quickly replace the interposer board in case of damage. MTMM-117-02-S-D-050 and MTMM-110-02-T-D-003 connectors from Samtec have been selected for the interposer connection to the motherboard and consequently the corresponding female connectors have been placed on the motherboard.

Except of the DDC232, the only circuit which has been implemented on the interposer board is the Voltage Reference circuit in Fig.3.30

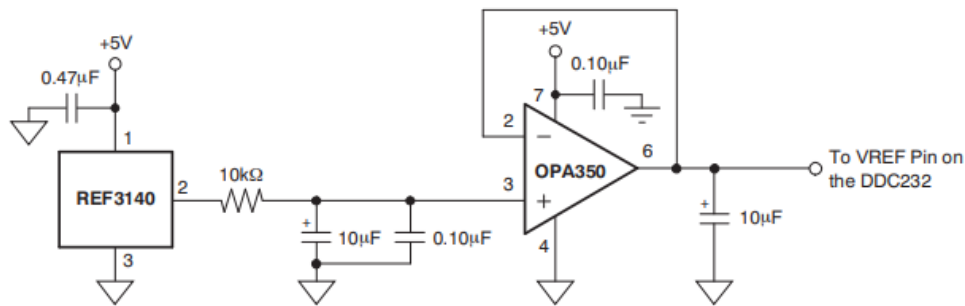


FIGURE 3.29: DDC232 Voltage Reference Circuit

The choice to make 5 different VREF circuits, one for each interposer board, has been done because this is a very noise sensitive circuit. Moreover, this circuit is used by the delta-sigma converters while the converter is measuring the voltage stored on the integrators after an integration cycle ends. During this sampling the external voltage reference must supply the charge needed by the delta-sigma converter. It's critical that VREF signal remains stable during the different modes of operation, because the delta-sigma converter measures the voltage on the integrator with respect to VREF. Since the integrator capacitors are initially reset to VREF, any drop of VREF itself which happens between the time capacitor are reset and the time when the converter measures the integrator output, will introduce an offset. Also, VREF must introduce as little noise as possible.

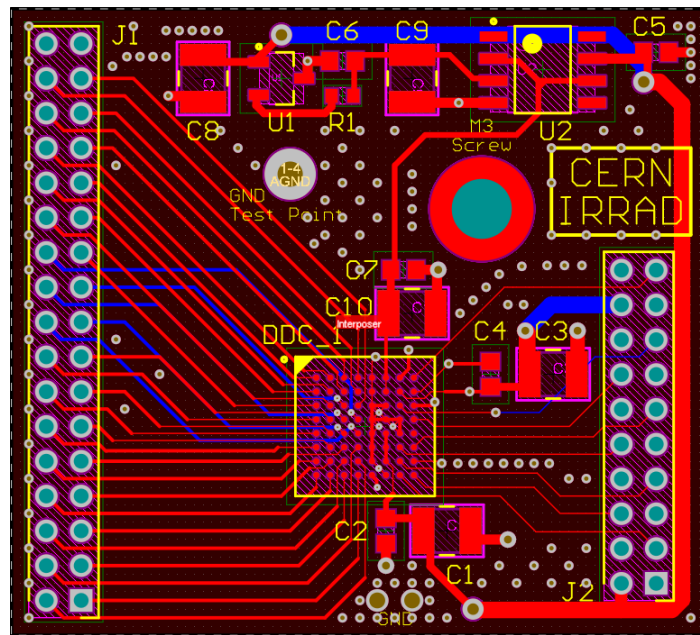


FIGURE 3.30: Interposer Board PCB Routing

Except of some decoupling capacitors on the DDC232 supply pins there are no other parts of the circuit to notice, since all the rest of the wiring diagram is about connecting DDC232 pins with Samtec connectors in order to distribute signals on the motherboard.

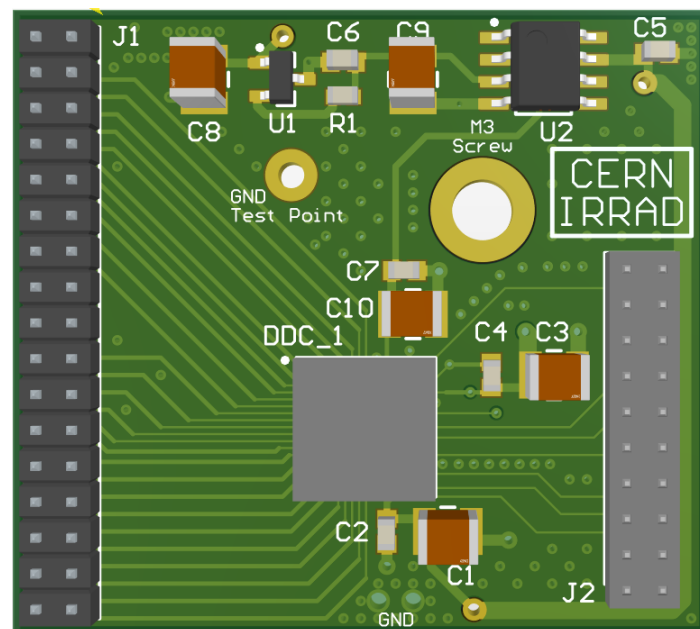


FIGURE 3.31: Interposer Board 3D Front View

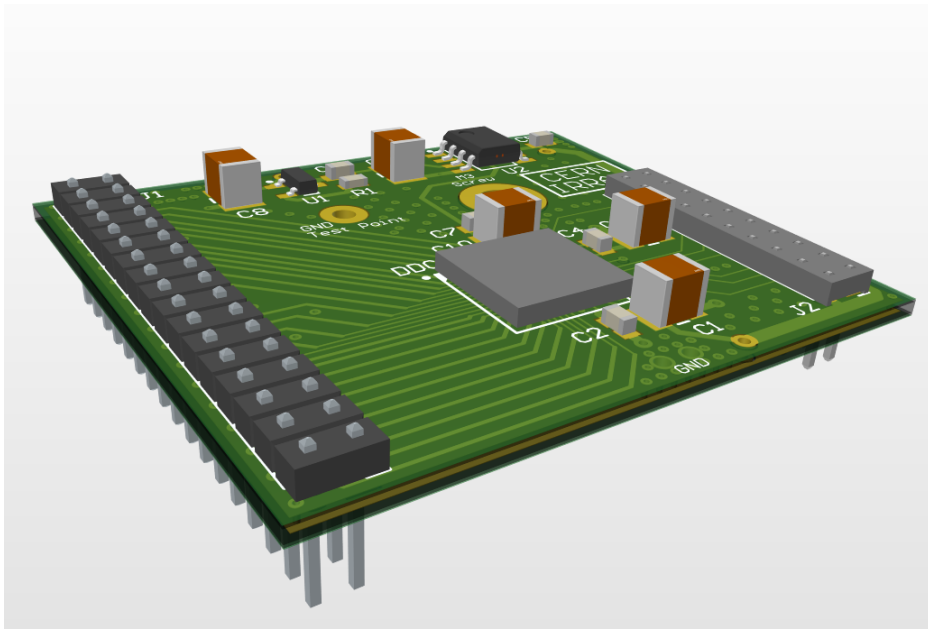


FIGURE 3.32: Interposer Board 3D Lateral View



3.6 Panel Board

The final aim of the project is to include the motherboard in a rack-mounted enclosure. The rack-mounted enclosure serves as the primary housing for the motherboard and associated components. Its design incorporates features such as standardized dimensions and mounting mechanism to ensure compatibility with existing rack infrastructure. The integration of a motherboard in this kind of enclosure offers numerous benefits, including efficient space utilization, improved system organization and simplified maintenance. A possible rack-mounted enclosure solution is shown in Fig.3.33.



FIGURE 3.33: Possible Enclosure type to be used for the final system

However, including the motherboard in this type of enclosure denies the possibility of physically accessing it, resulting in the inability to perform some basic functions, such as simply turning the board on/off. Moreover, some other features has been implemented on the motherboard, such as the possibility to send a manual trigger pulse through the push of a button or the possibility to connect some LEMO connectors to manually send/read signals. Finally, the motherboard can also communicate some basic information through an OLED display and 2 LEDs. In order to perform all these functions, the whole system

will include another PCB, which will be used as a Panel Board on the external part of the rack-mount enclosure. The panel board facilitates the connection of I/O peripherals to the motherboard, allowing users to interact with the system externally.

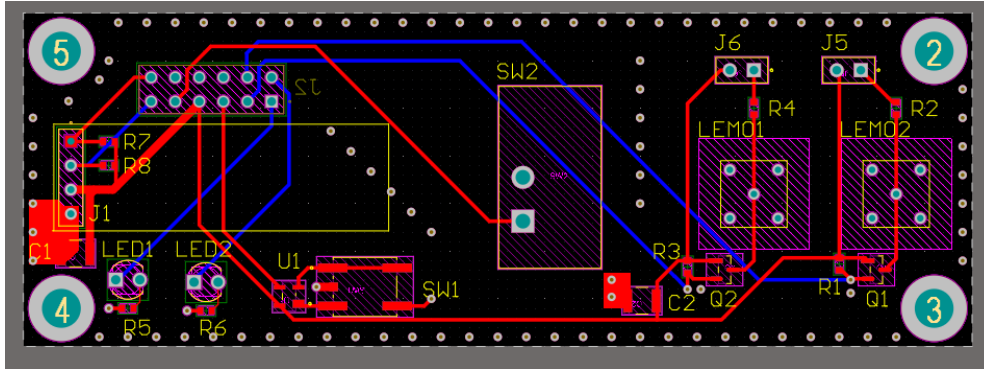


FIGURE 3.34: Panel PCB routing

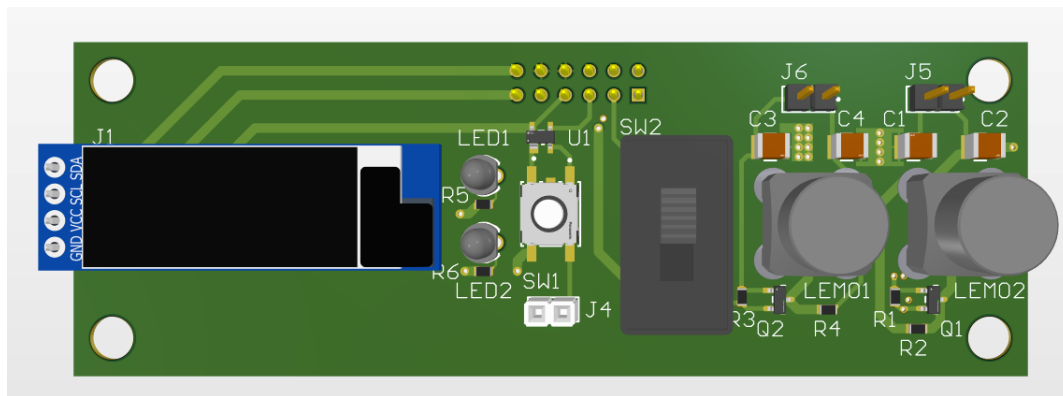


FIGURE 3.35: Panel PCB 3D front view

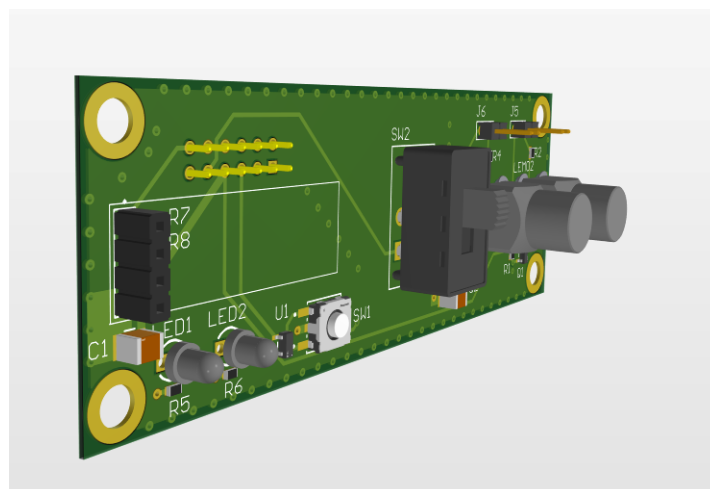


FIGURE 3.36: Panel PCB 3D lateral view

TESTING

Once all the project parameters were defined and the board design was completed, the PCBs were produced. As mentioned before, all PCBs are made with a 4-layer structure, thus including two copper layers at the top and bottom and two other intermediates, adequately separated by layers of FR4, which, is a dielectric material capable of providing the necessary insulation between the various layers of copper. In this last chapter, an accurate description of the testing process will be provided and all the results of the tests performed on the boards created will be reported with the aim of providing detailed documentation on the product performances.

4.1 From manufacturing to troubleshooting

The successful fabrication of the printed circuit boards play a crucial role in their implementation. The boards results to be perfectly consistent with the design created using the software Altium Designer®.

The first step to switch to produce the boards is to create some specifics files known as *Gerbers* that the PCB manufacturer needs for the final realization. Gerber files are a standard file format which contain information about the different layers of the PCB. Each layer, such as the top copper layer, bottom copper layer or intermediate ones, as well as the silkscreen or the soldermask are represented by a separate Gerber file. These files provide detailed information about the copper traces, pads, vias and other elements. Once the Gerbers files were created, they were sent to PCB manufacturer. Gerbers are not the only files needed in order to create the board because some other information and files are necessary such as the "drill file" which specifies the locations and sizes of holes to be drilled on the PCB. Finally the Bill of Materials (BOM) was sent as well. This file contains all the information about components that need to be mounted on the PCB. According to this specifications, manufacturers can realize the boards and (if the customer ask for it) they can



provide mounting services, which basically includes soldering all the components on the boards. This is the case of the Interposer board, on which there is the DDC232 component, which is made of a Ball Grid Array (BGA) package and requires proper instrumentation to be soldered correctly. The Fig.4.1 shows the final result of the motherboard printout while the Interposer and Panel boards are shown in Fig.4.2 and 4.3.

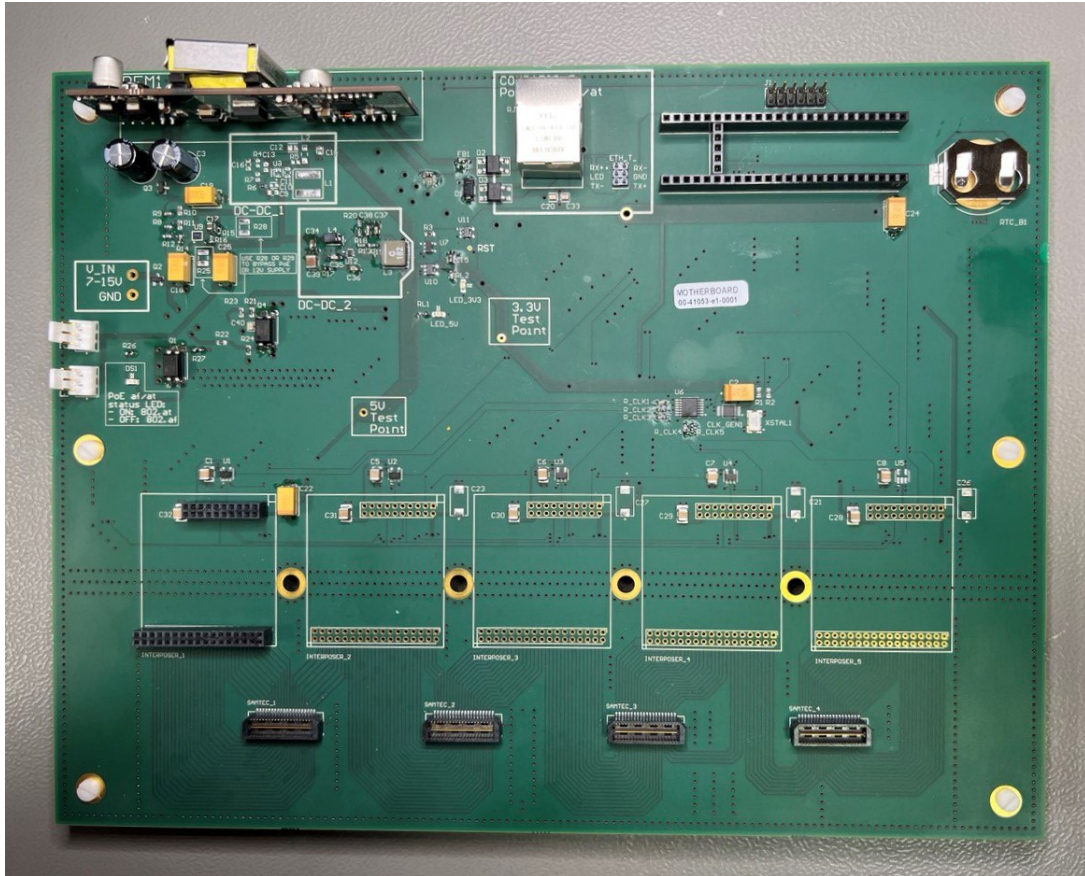


FIGURE 4.1: Motherboard PCB Front View

The first goal to be achieved once the boards were received from the manufacturer was to make sure that they were fully functional and prepared to perform the necessary tests for acquiring signals from the BPM pads. When debugging a PCB, there are several important precautions to keep in mind to ensure safety and prevent damage to the components or the board itself. The laboratory where the debug was performed was equipped with all the necessary safety measures, including anti-static wristband or grounding mat. In addition, the workbench was equipped with all the necessary test equipment, such as a bench multimeter, signal generator and oscilloscope. In order to perform a correct and safe debugging, a systematic and methodical approach was used, breaking down the troubleshooting process into smaller steps or sections, starting from the most basic functionality and gradually mov-



ing towards more complex components or subsystems. All the progresses were recorded on a document in order to keep trace of every problem occurred.



FIGURE 4.2: Interposer PCB Front View

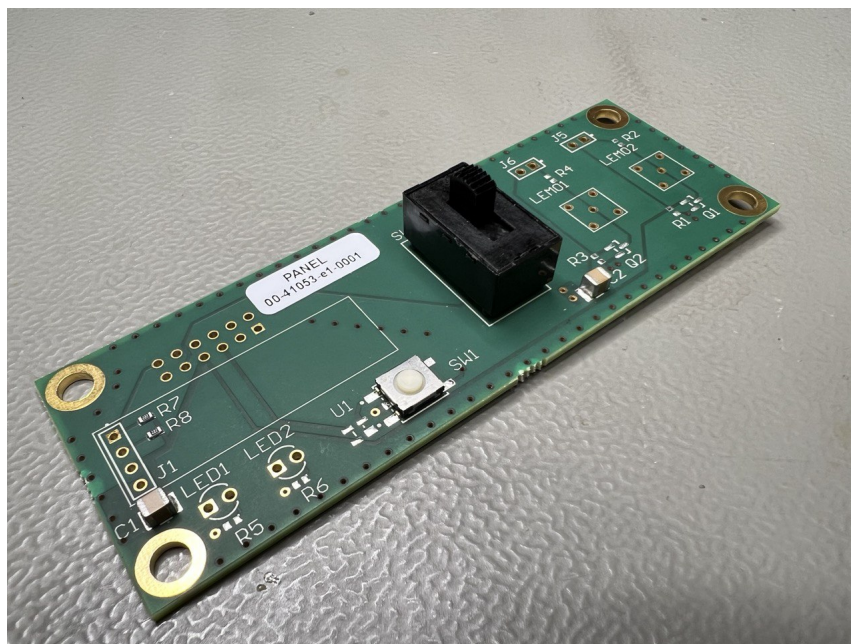


FIGURE 4.3: Panel PCB Front View

Through a combination of rigorous testing methodologies and advanced diagnostic tools, the debugging process efficiently identified and rectified various challenges. However, by effectively isolating and bypassing the issues encountered, the final product demon-



strated its ability to deliver each signal correctly. Fig.4.4 shows the final board fully assembled and functioning, where it is possible to notice that some external wiring and components were mounted, with particular reference to the power supply part which provided for the scaling of the voltage from 12V to 5V. By incorporating this external components, the project showcased adaptability in overcoming obstacles still managing to give the necessary supply voltage to all the downstream circuits.

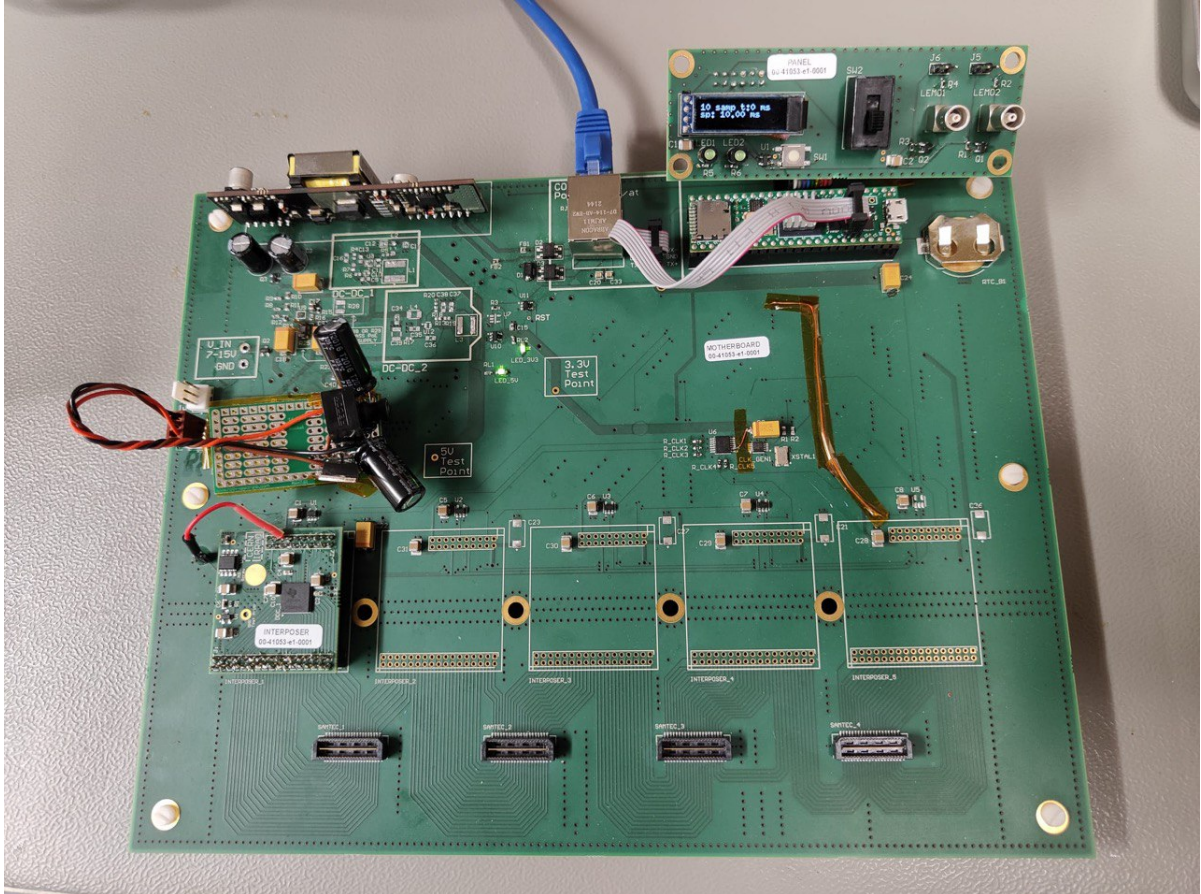


FIGURE 4.4: Final system fully assembled and functioning

4.2 Measurements

The first test conducted was about the clock generation circuit, with the aim of understanding if the integrated circuits used for the clock generation were actually working. As shown in Fig.3.26 the component requires an I2C communication with the microcontroller in order to understand how to generate the clock signal and its timing. After, the clock signal goes into a fanout buffer circuit, which block diagram is shown in Fig.3.27. Fig.4.5 shows the trend of the clock signal measured downstream of each fanout buffer output using a Teledyne-LeCroy®HDO6104-MS oscilloscope. The trend of the clock signal, the duty cycle and the amplitude are consistent with what was expected. Fig.4.6 instead shows a measurement using cursors of the clock frequency. It is possible to see how the frequency is exactly equal to 20MHz, in accordance with what is set in the Teensy®4.1 microcontroller firmware. Subsequently, the operation of several signals associated with the operation of the DDC232 was tested. Considering Fig.2.10 as a reference, in which the timing diagram of the DDC232 is shown, it is possible to see in Fig.4.7 the display of the CONV signal with reference to the DCLK and DOUT signals. Subsequently, Fig.4.8 shows the trend of the DVALID signal again with reference to the DCLK and DOUT signals.



FIGURE 4.5: Clock signal visualization

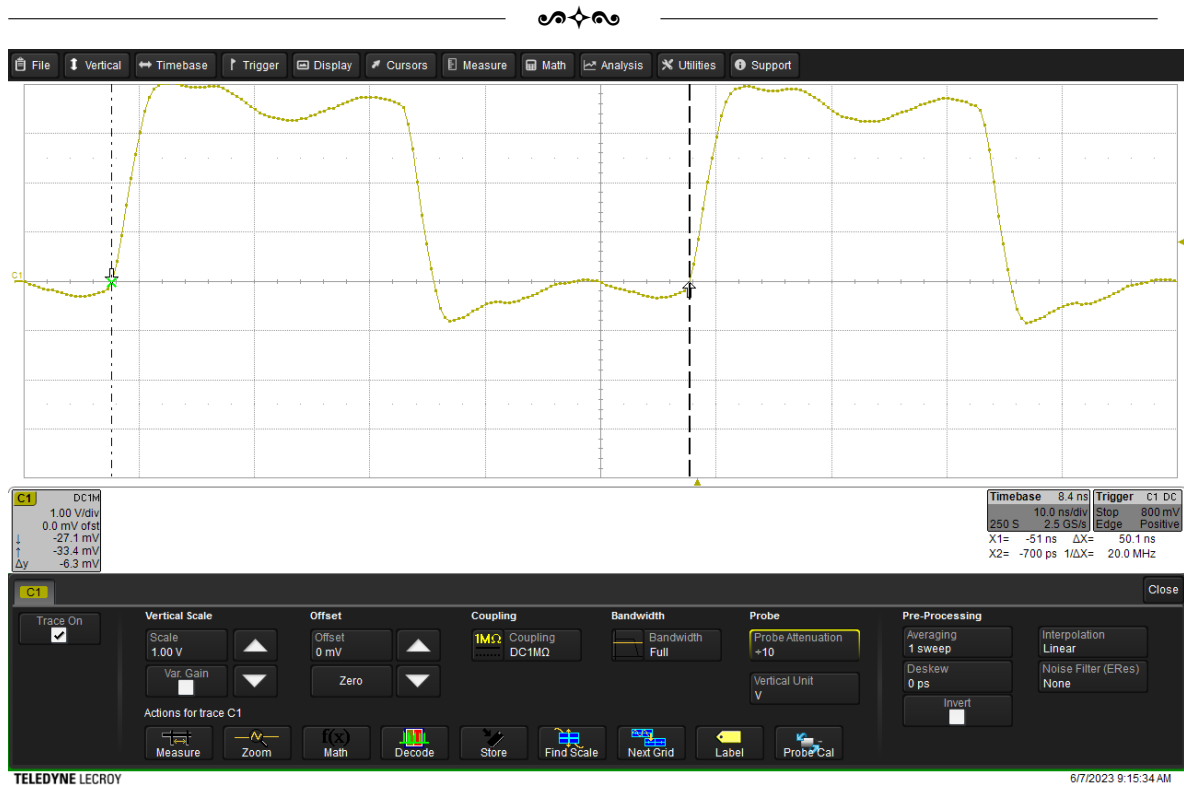


FIGURE 4.6: Clock frequency measurement



FIGURE 4.7: DDC232 timing diagram with reference of CONV signal

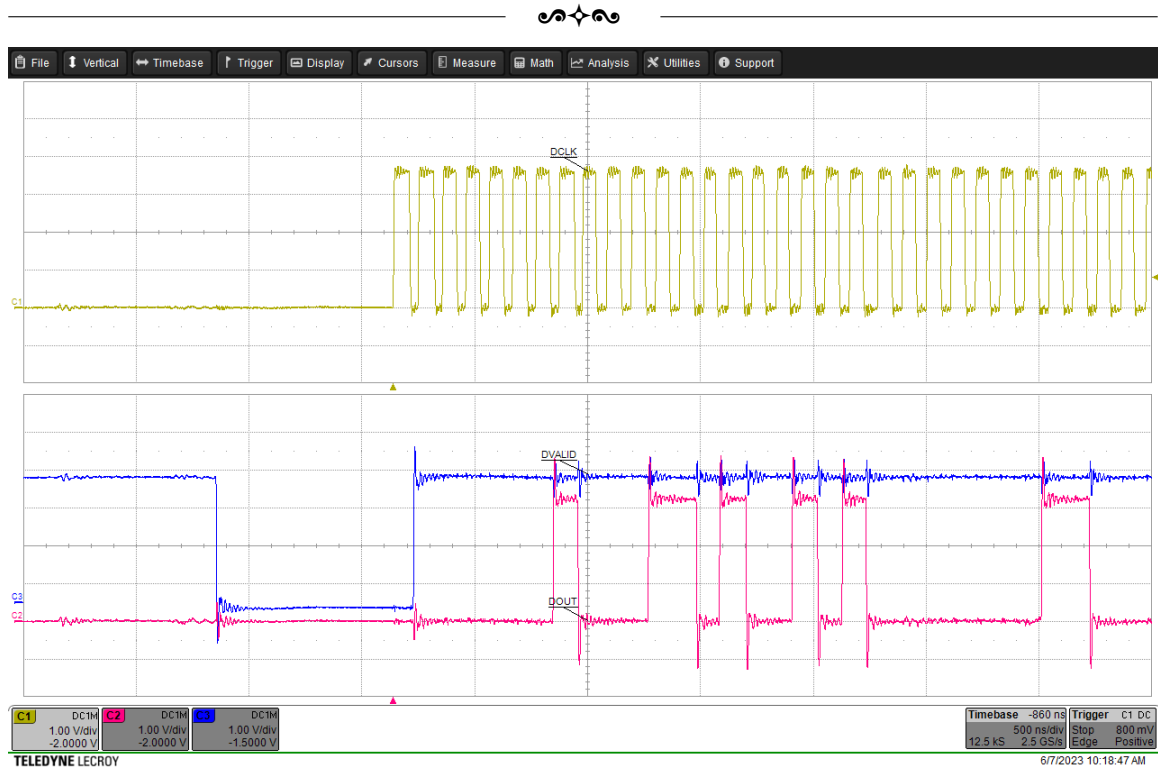


FIGURE 4.8: DDC232 timing diagram with reference of DVALID signal



4.2.1 Test with generated current signals

A comprehensive test was conducted to evaluate the functionality and performance of the board which, as said before, was designed to read 40 current signals on each Samtec® connector. In order to apply the current signals to the PCB, a specially designed test auxiliary board equipped with 40 LEMO® connectors was used. Each connector was connected to an individual channel on the PCB, ensuring precise and separate application of the current signals. The setup is shown in Fig.4.9.

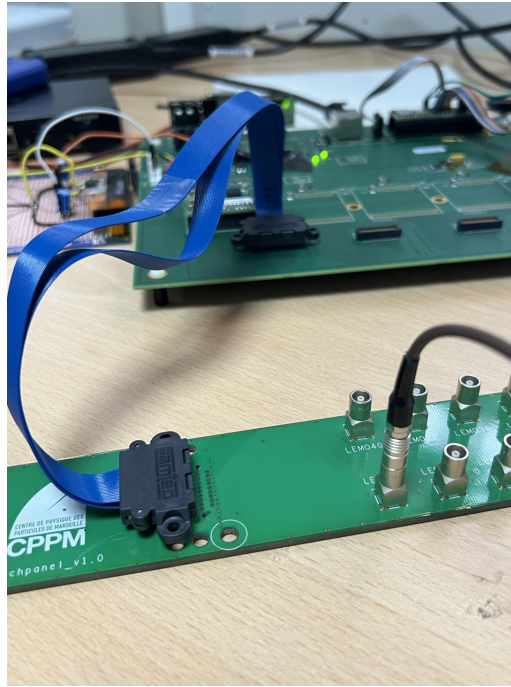


FIGURE 4.9: Testing setup with channel expansion board

The first test operation performed is a connector mapping. In particular, it was ensured that the Samtec® connector was correctly connected to the channels of the interposer board without signal interruptions or short-circuited pins. Once ensured that the connections were consistent, a test for current signal acquisition was performed. Before discussing the test results, it is appropriate to introduce some technical specifications on the functioning of the DDC232 and on the current signal acquisition phase. For the purposes of correct current injection on the DDC232 channels it is necessary to find the right value to apply. Whereas the typical currents generated by BPM sensors by SEE are in the order of nanoamperes, it is complex to be able to generate and create such a low current, even using a very accurate signal generator. For this reason it was decided to proceed in the reverse way using a $1M\Omega$ resistor and varying the applied voltage, so as to be able to obtain the injected current using Ohm's law. Furthermore, it was useful to understand how the DDC232 behaved on

the basis of the variation of different parameters, such as the sampling time and the range. The Range parameter is a specific parameter of the DDC232 which allows to vary the dimensions of the feedback capacity of the integrator. The size of the digital signal output from the DDC232 was therefore plotted on the basis of the current applied in nanoamperes considering 3 combinations of range and sampling time. Specifically, the range assumed the values 0, 4 and 7, while the sampling time was set at 1ms, 10ms and 100ms. The range and sampling time parameters were varied using a web application designed specifically to manage the communication between Teensy® microcontroller and DDC232. Furthermore, a Python application was used to read the acquisitions on the various channels and display the size of the output bit word in real time. Python application is visible in Fig.4.11 and Fig.4.12. In Fig.4.11 there is no current applied, so every channel is showing an ADC count of ~ 8000 , corresponding to the baseline value, which is another parameter configurable through web application. In Fig.4.12 there is a current signal applied to channel 14 (notice that in python application it results to be number 13 because python code start counting from 0).

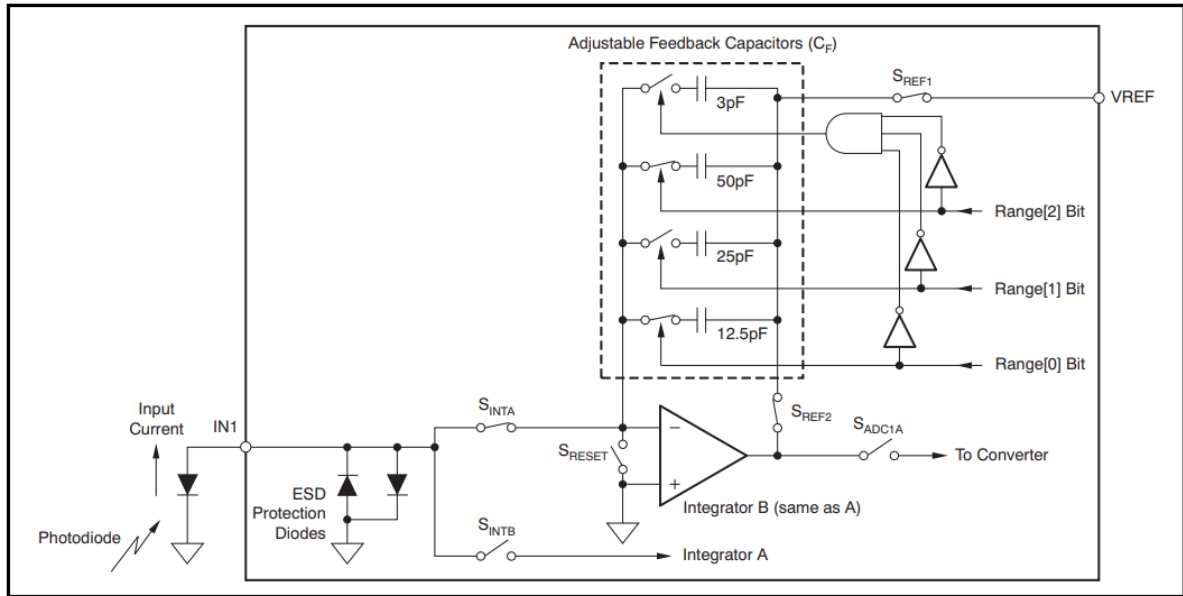


FIGURE 4.10: Basic Integration Configuration for DDC232

The first test was performed in such a way as to be able to understand the output behavior of the DDC232 with very low current values (max 30 nA) for the different settings. Result is visible in Fig.4.13. The second one was performed in order to understand how big could be the current until the saturation was reached i.e. when the DDC232 gives in output the largest word possible (in 20 bits output configuration). Result is visible in Fig.4.14. A graphical representation was performed for both tests showing the saturation curve. In



order to have a good response, the ideal expected characteristic should be linear and space between the baseline and the saturation point, thus covering all the possible values of the output. The closest case to the ideal one is obtained for Range = 7 and Sampling Period = 10 ms. Decreasing the range value results in a smaller feedback capacitance for the integrator, thus including a shorter charging time for the capacitance and consequently a faster saturation for the ADC output word. Same effect can be reached increasing the sampling time value, which means to have a larger time between acquisitions.

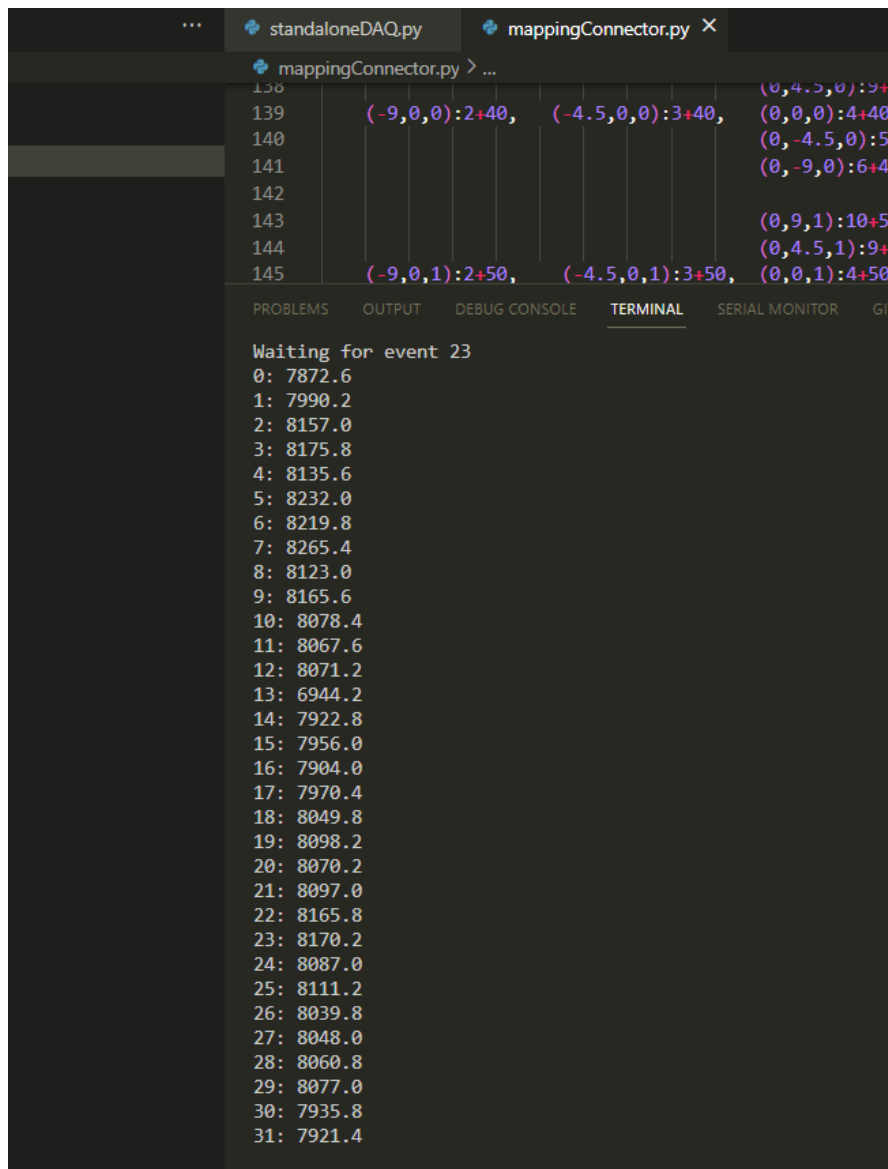


FIGURE 4.11: Visualization of data in absence of current injected



```

... standaloneDAQ.py mappingConnector.py X
mappingConnector.py > ...
138
139 (-9,0,0):2+40, (-4.5,0,0):3+40, (0,4.5,0):9+40, (4.5,
140 (0,0,0):4+40, (0,-4.5,0):5+40,
141 (0,-9,0):6+40,
142
143 (0,9,1):10+50,
144 (0,4.5,1):9+50,
145 (-9,0,1):2+50, (-4.5,0,1):3+50, (0,0,1):4+50, (4.5,

PROBLEMS OUTPUT DEBUG CONSOLE TERMINAL SERIAL MONITOR GITLENS

Waiting for event 94
0: 7912.4
1: 7925.2
2: 8077.2
3: 8106.6
4: 8080.6
5: 8124.4
6: 8169.2
7: 8184.0
8: 8118.4
9: 8138.0
10: 8048.6
11: 8038.4
12: 8057.6
13: 514896.2
14: 7899.6
15: 7879.4
16: 7851.6
17: 7957.4
18: 8055.4
19: 8083.4
20: 8053.6
21: 8082.2
22: 8134.2
23: 8172.0
24: 8080.2
25: 8096.6
26: 8020.8
27: 8033.8
28: 8030.8
29: 8071.2
30: 7916.6
31: 7895.6

```

FIGURE 4.12: Visualization of data with current applied to channel 14

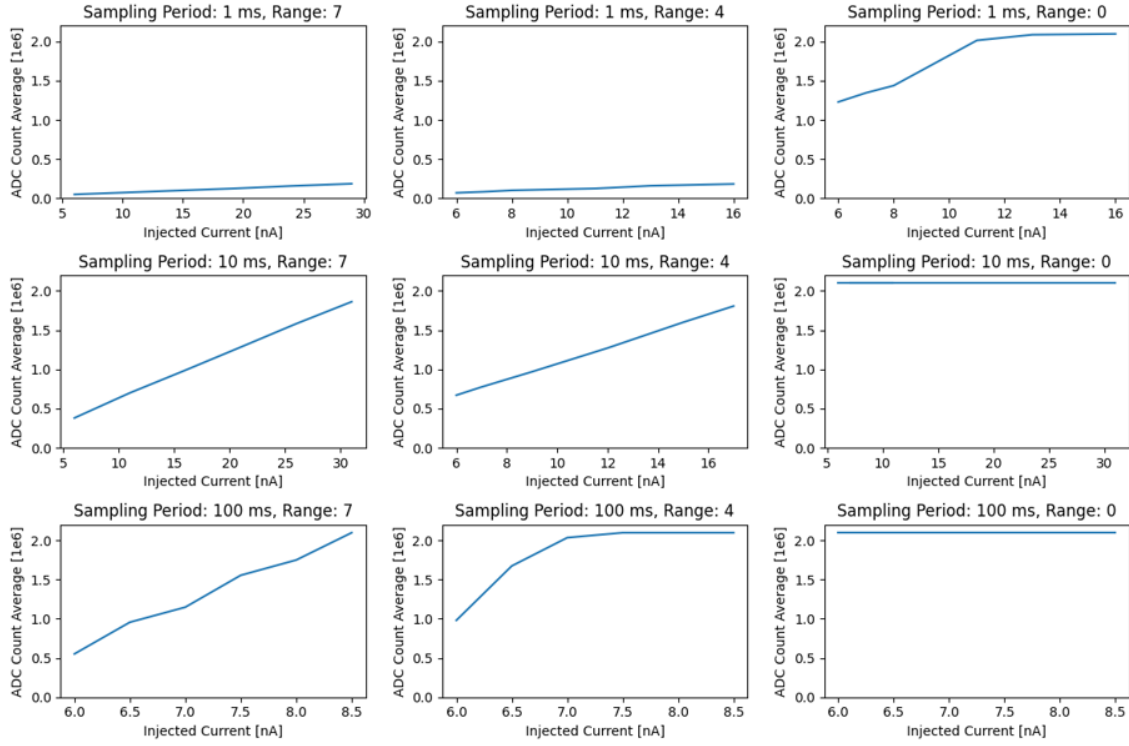


FIGURE 4.13: Graphical visualization of channel n.1 with maximum current of 30 nA

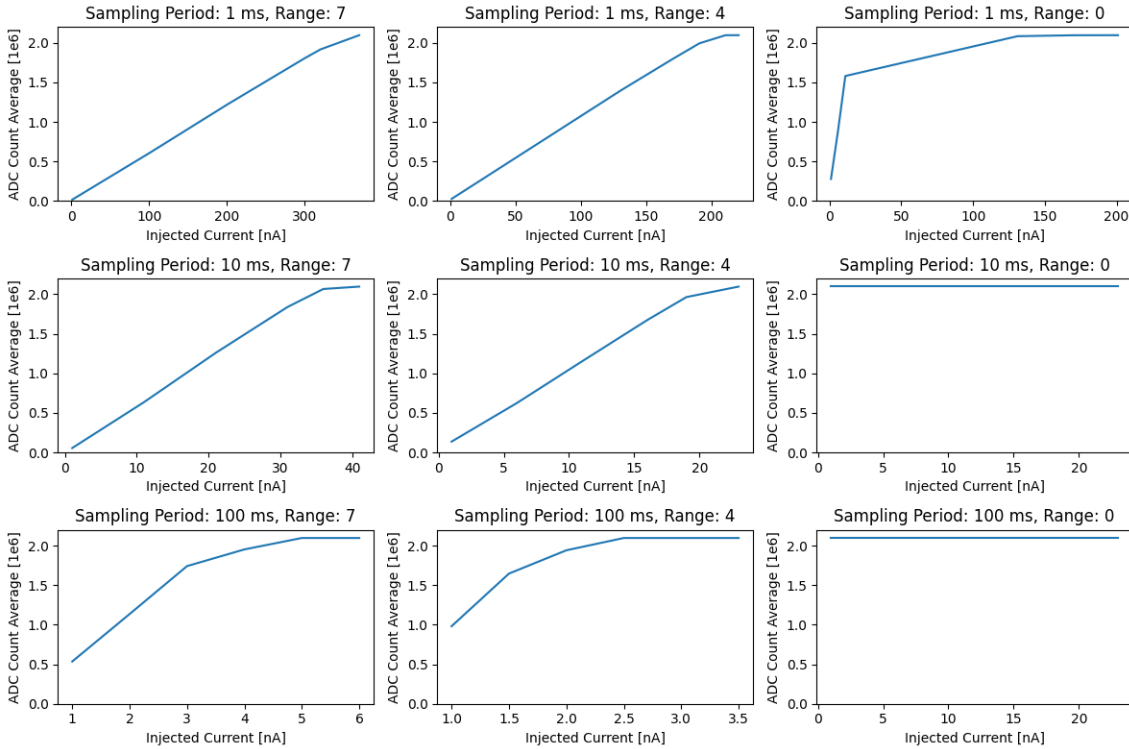


FIGURE 4.14: Graphical visualization of channel n.7 until the saturation point



When the range is maximum (range = 7) and the sampling time is 1 ms, the output word is too small, not allowing to have an accurate measurement due to overlapping of values. Same, but opposite effect is reached with minimum range and bigger sampling time values, where the output word results to be already saturated even with 0 A of injected current. In the second case (Fig.4.14), as already said, an higher current has been injected in order to reach saturation point for all cases. The most significant result is obtained for sampling period of 1 ms, where a current of more than 300 nA is needed in order to reach saturation point.

Noise rejection

During the current injection testing they were two values of current that could be obtained. The first one was an analytical one, calculated using the Ohm's Law through the $1M\Omega$ resistor and voltage applied value. The second one was directly measured through the signal generator (Keithley® 2410), which was showing the exact current injected in the channel. Moreover different measurements were done in two different environments, where the first one was probably influenced by a bigger amount of electronic noise. Apparently, noise really influenced the system, since, in the first case a difference of ~ 6 nA was registered between the analytical calculated current and the real injected one. In the second case, there was almost no difference between the two currents. a graphical representation has been done in the following graphs.

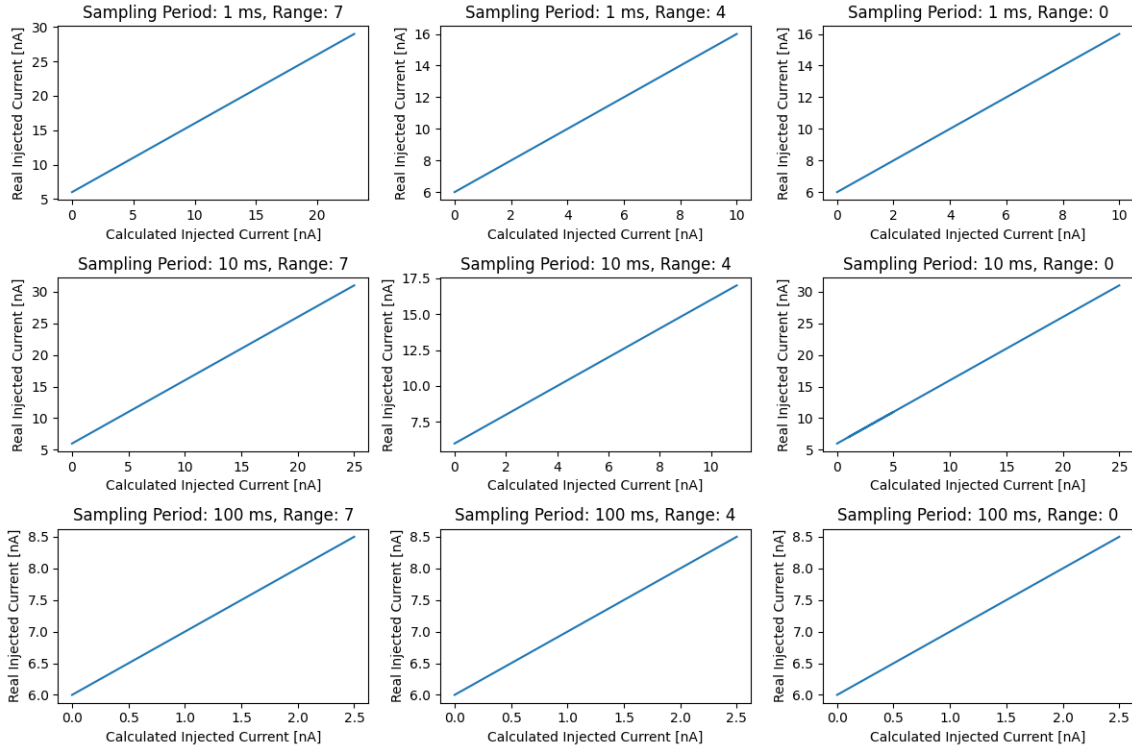


FIGURE 4.15: Current bias in case of a noisy environment

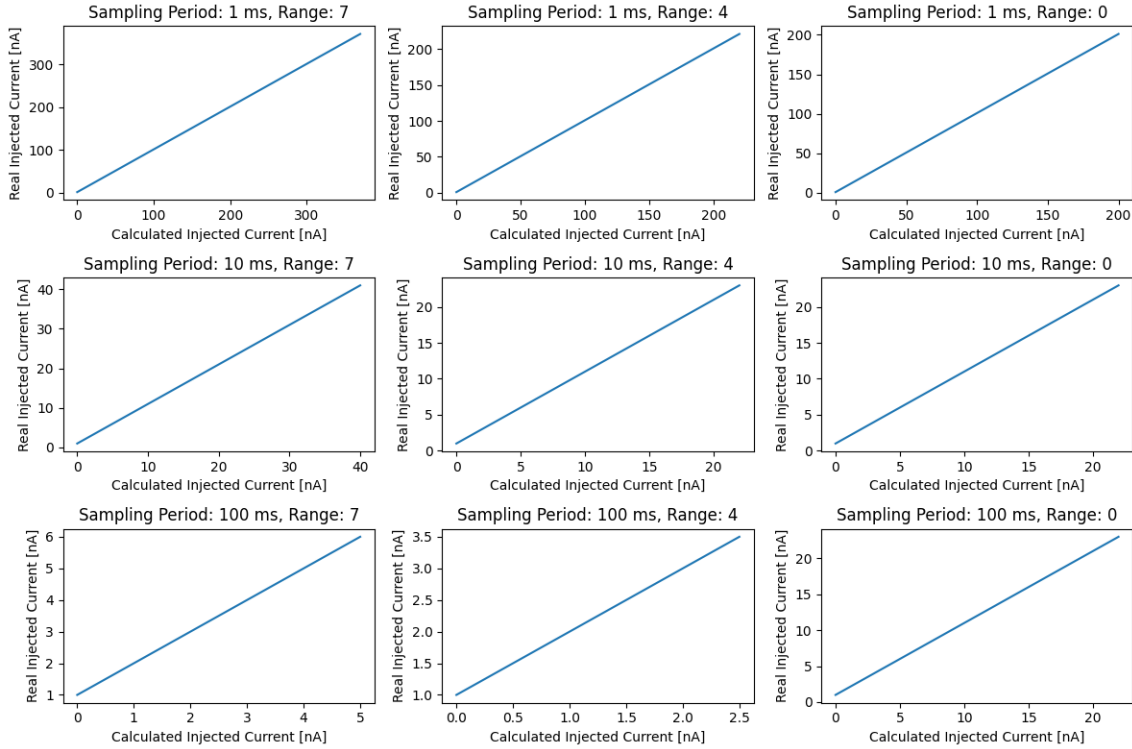


FIGURE 4.16: Current bias in case of a non-noisy environment



4.3 Conclusions

This thesis has explored the design and development of a new readout electronic system for the BPM devices in IRRAD facility. The final system showed promising results and through this research, several key findings and accomplishments have been achieved. During the initial part of the project, the understanding of the general structure of the IRRAD facility and the participation to the day-to-day operations of the facility. This allowed to lay solid foundations to the understanding of the needs of the facility and the specifications of the readout system. Then, the study of the Secondary Electron Emission BPMs and their principles of operation has allowed the understanding the sensors and, above all, the hardware and architecture needed to support them. In this step, some key components and requirements for the front-end electronics were chosen. Subsequently, the project choices and general structure, including the schematics and PCB routing, have been successfully implemented. Lastly, the correct functioning of the system has been carefully studied and minor modifications were evaluated in order to create a second and final revision of the electronics. Finally, some tests on the performance of the system were conducted, documenting the measurements and confirming that the general system is able to correctly acquire the data coming from the BPM sensors. Furthermore, those measurements are an important step for the verification of the linearity and range of the front-end electronics.

This thesis has been completed in the framework of an internship at CERN from August 2022 until July 2023 and the work presented is attributed to both personal and collaborative activities. In the next months, the new electronics will be installed in the IRRAD facility and data coming from it will be fundamental for the facility and for the next generation of users.



EP-DT
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FEDERICO II

APPENDIX **A**

WIRING DIAGRAMS AND PCB VIEW

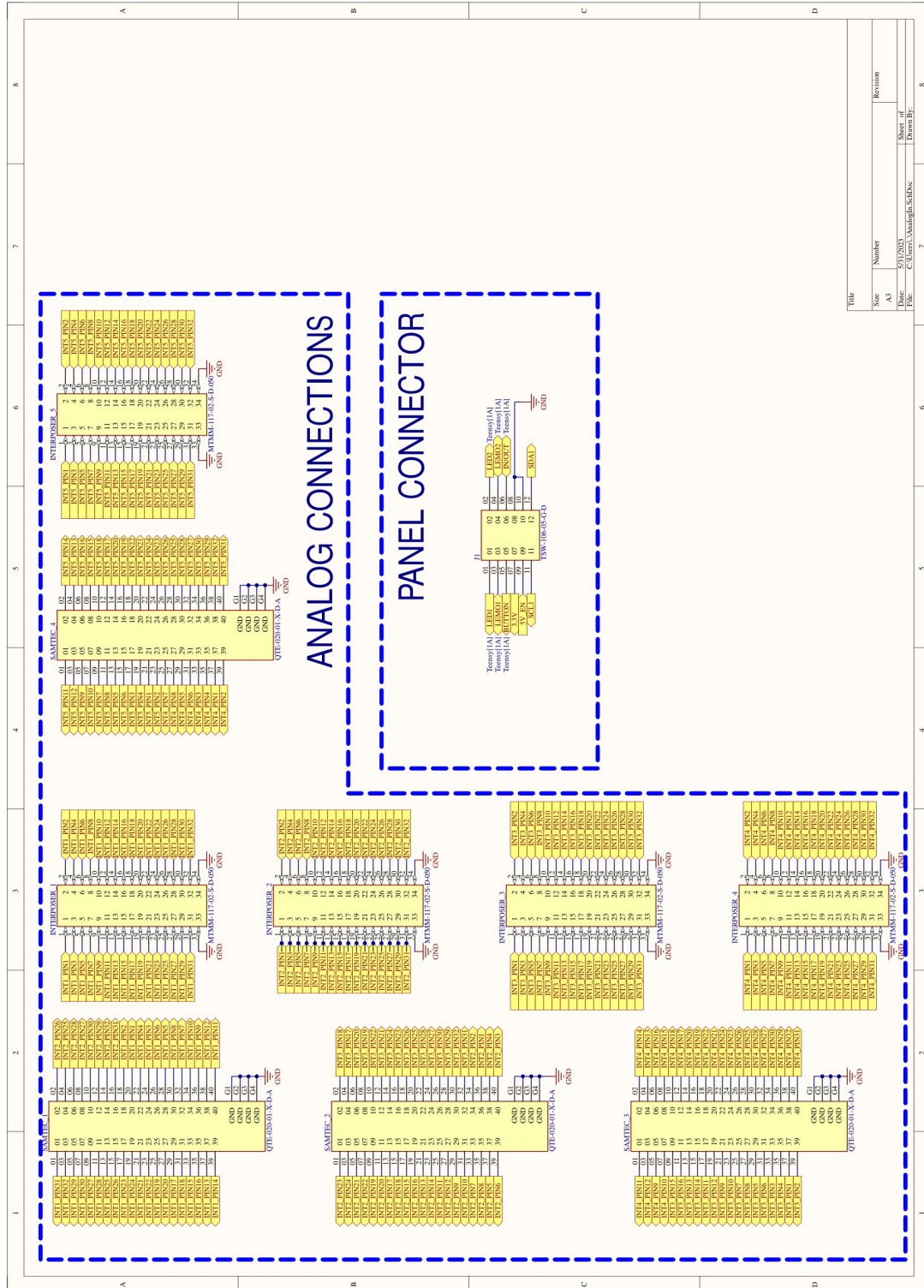


FIGURE A.1: Motherboard Wiring Diagram for Connectors



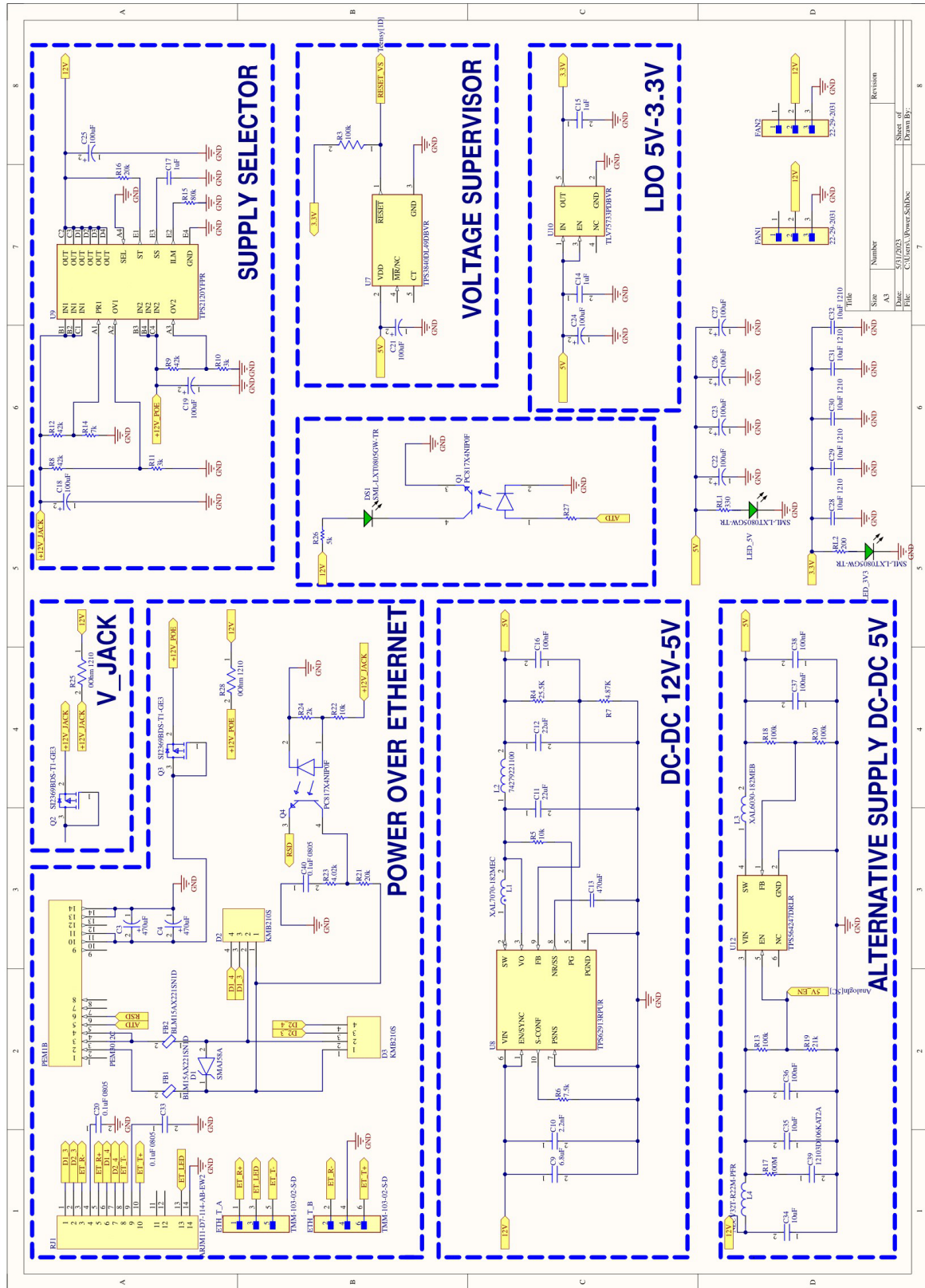


FIGURE A.3: Motherboard Wiring Diagram for Power Supply



95

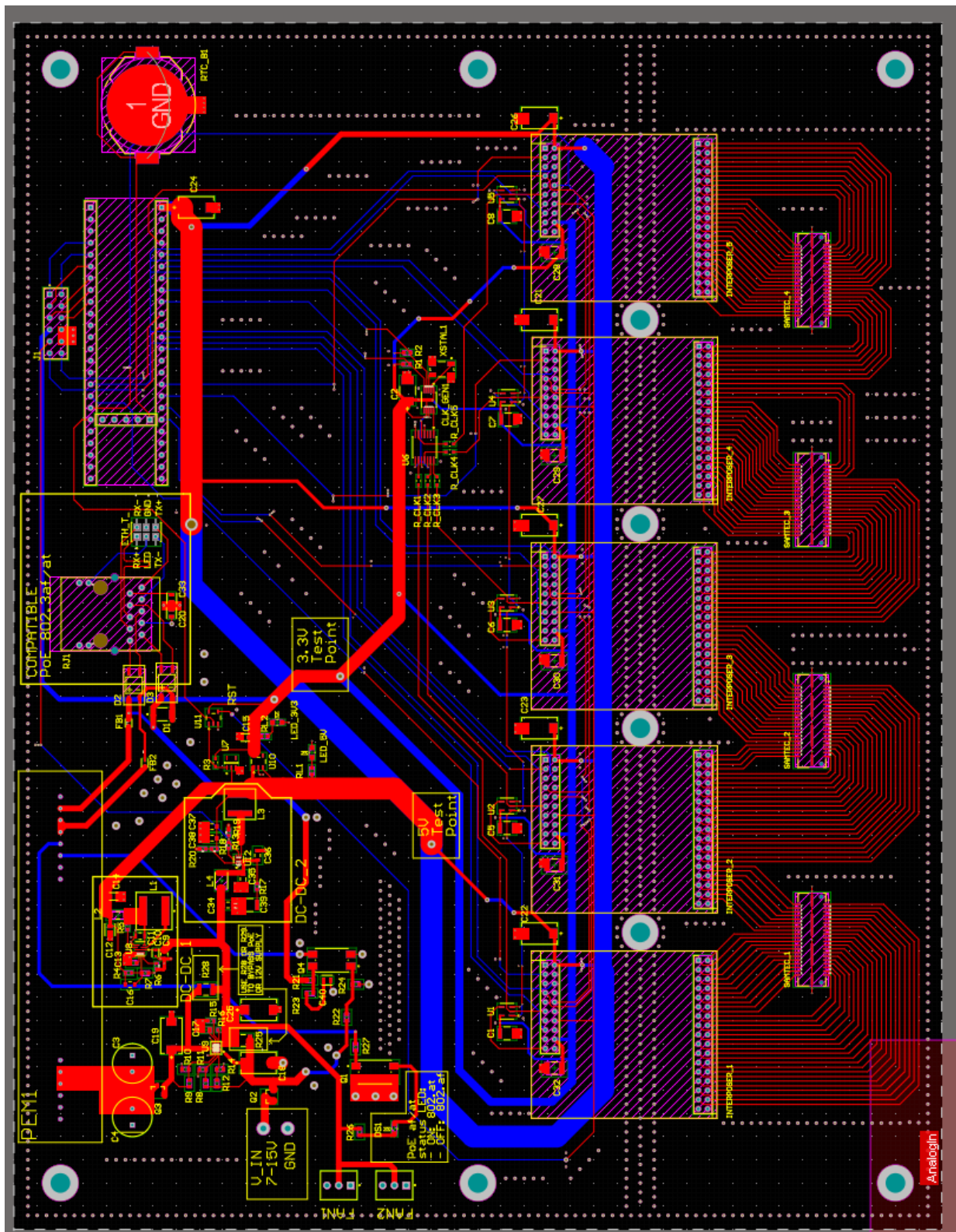


FIGURE A.5: Motherboard Routing

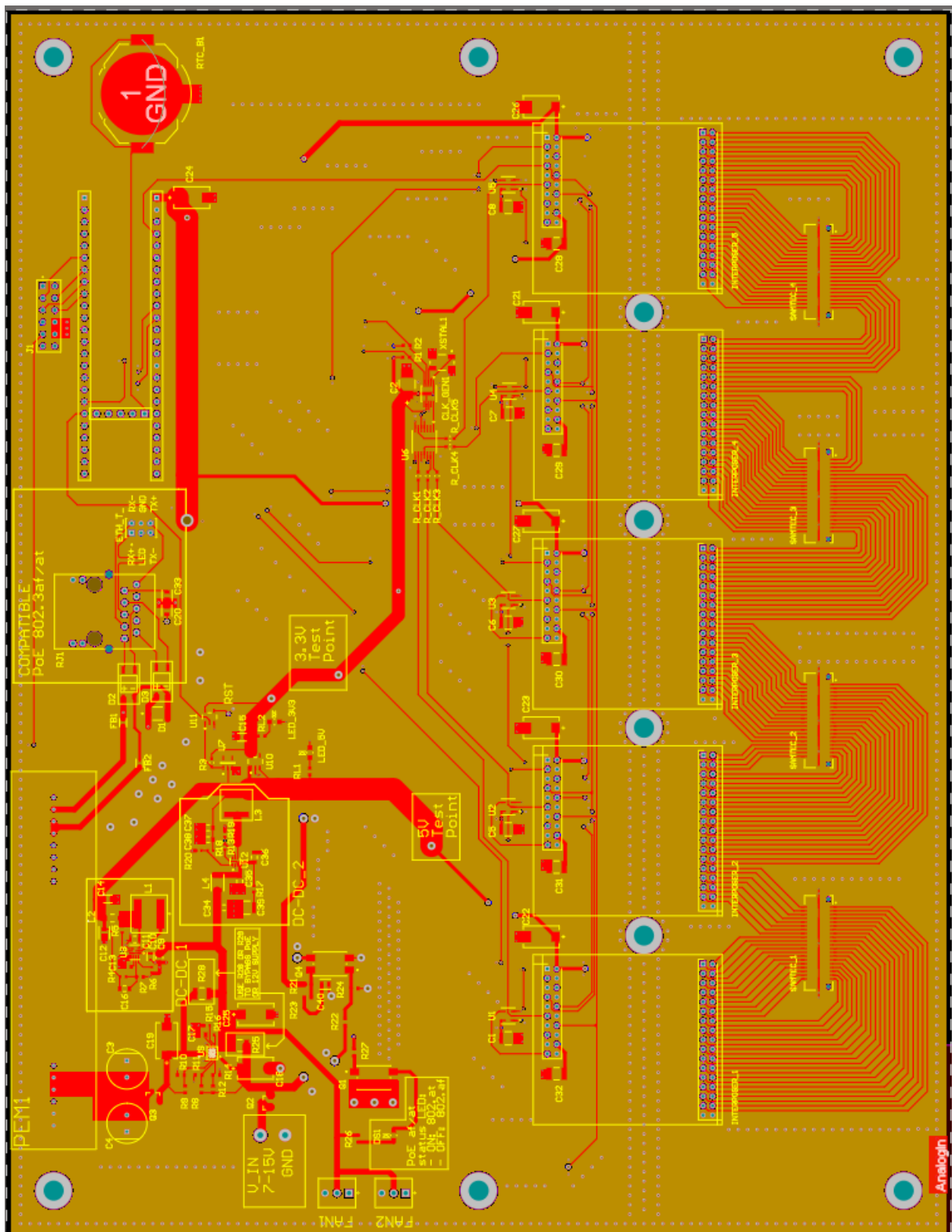


FIGURE A.6: Motherboard routing with Layer 2 visible

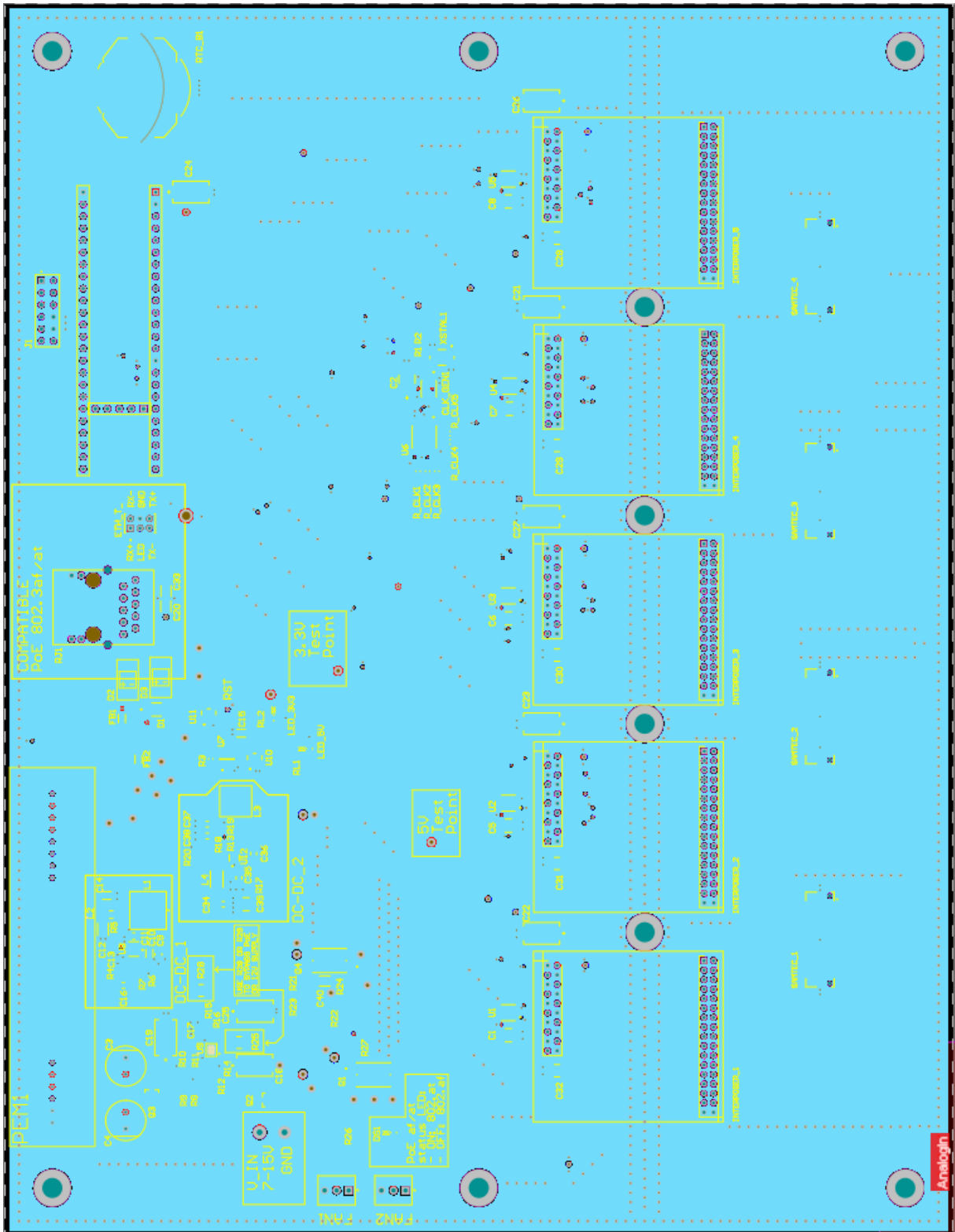


FIGURE A.7: Motherboard routing with Layer 3 visible



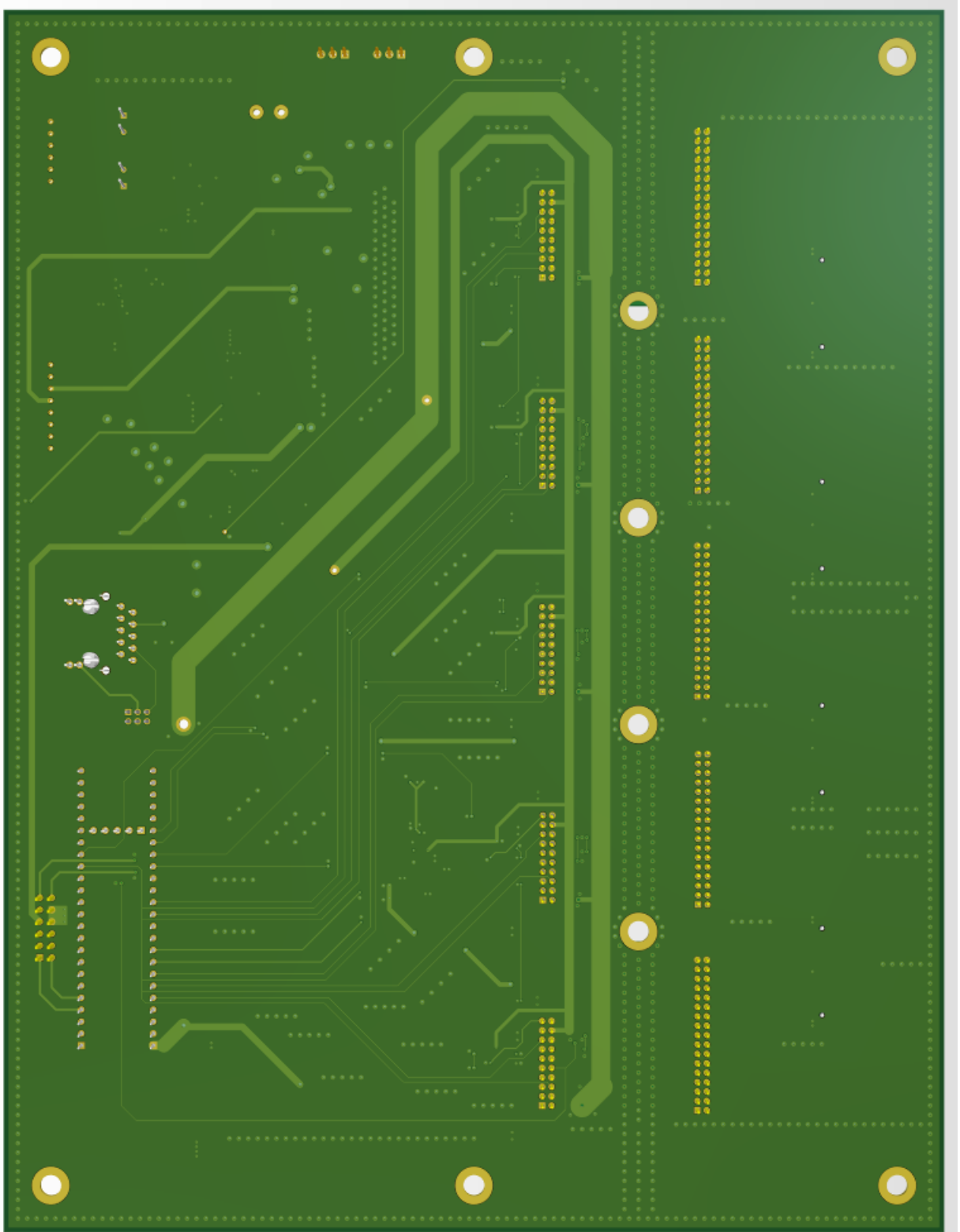


FIGURE A.9: Motherboard 3D model retro view

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