

Characterization of Powerhybrids for the Phase-2 Upgrade of the CMS Detector

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Charakterisierung von Powerhybriden für das Phase-2 Upgrade des CMS-Spurdetektors

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1 Motivation

The Standard Model of particle physics describes all known elementary particles and their fundamental interactions. It is robust in predicting experimental results. However, not all phenomena can be explained by the Standard Model. An example for this is that it does not contain any particles that are possible candidates for dark matter, even though astronomical observations provide strong indications for its existence. Particle accelerators and detectors have played a major role in verifying predictions of the Standard Model and in searching for beyond Standard Model physics.

The CMS¹ experiment is located at the LHC², the largest and most powerful particle accelerator to date. The CMS detector is able to reconstruct the trajectory, energy, charge and momentum of products from proton-proton collisions in the LHC. It contributed greatly to some of the major breakthroughs in modern particle physics, most notably the discovery of a new resonance in 2012, providing the first experimental evidence for the existence of the Higgs boson which was the last missing piece in describing Standard Model processes [1]. In order to study Standard Model events with higher statistical significance and to increase the chances of finding physics beyond the scope of the Standard Model, parts of the LHC will undergo significant upgrades beginning at the end of 2024 [2]. The project is called the “High Luminosity LHC” (HL-LHC). The aim is to achieve a peak instantaneous luminosity of $L_{\text{peak}} = 7.5 \cdot 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ and increase the integrated luminosity more than tenfold, from 350 fb^{-1} to 4000 fb^{-1} . This also necessitates major upgrades for the LHC experiments as they need to be compatible with the high hit rates expected after the HL-LHC upgrade. This thesis was conducted within the framework of the so-called “Phase-2 upgrade” of the CMS experiment. The entire silicon tracking system will be replaced in order to increase radiation hardness and also to significantly improve the tracking capabilities of the detector [3]. The Inner Tracker (IT) will be made up of silicon pixel modules while the Outer Tracker (OT) will use so-called “ p_T modules”, which are able to recognize particles with high transverse momentum. These two-sided modules are made up from either two silicon strip sensors (2S modules) or one silicon strip and one silicon macro-pixel sensor (PS modules). The electronics that are responsible for powering the modules as well as the optical readout are integrated on “service hybrids” - small electronic circuits constructed of individual devices bonded to a PCB³ - that are mounted on the silicon modules.

In this thesis, results of several electrical tests on the newest prototype for the PS module’s power hybrid (PS-POH) will be presented. On the PS-POH the input voltage V_{in} supplied by the low voltage power supply (LVPS) is converted to the lower voltages V_{out} used for powering the front-end electronics. The PS-POH implements a two-stage powering system that uses three DC-DC buck converters, which are used to convert voltage supplied by a direct current (DC) source to a lower voltage. The converters need to comply with the demanding radiation requirements in the detector and are developed at CERN. Studies presented in this thesis were performed for the first time on the newest prototype of the final PS-POH, which uses the newest converter prototypes in both the first and second stage of the powering scheme.

First the LHC and the CMS experiment, as well as their scheduled upgrades, will be briefly summarized (Chapter 1). A more detailed description of the PS-POH and its functionality will

¹Compact Muon Solenoid

²Large Hadron Collider

³Printed Circuit Board

also be given in Chapter 2. It is important that no large spikes in the output voltages of the PS-POH are visible during turn-on and turn-off as well as during sudden large load changes as this might impact the performance of the front-end electronics. Additionally the efficiency of the PS-POH is of interest, as heat dissipated in the detector volume due to power loss in the detector components needs to be kept to a minimum to prevent thermal runaway. Therefore measurements of the dynamic behaviour as well as the efficiency of the prototype will be presented (Chapter 3). Conducted and radiated noise of the converters should be kept as low as possible as they negatively affect the front-end electronics and module's silicon sensors. Studies of both the conducted (Chapter 4) and radiated noise (Chapter 5) produced by the converters were performed. In both these chapters the effects of applying shielding to the PS-POH prototype will be discussed.

2 The HL-LHC and the Phase-2 Upgrade of the CMS experiment

2.1 The Large Hadron Collider

The LHC was constructed in a tunnel, 26.7 km in circumference and approximately 100 m beneath the surface, originally built for the LEP¹ machine at CERN² close to Geneva [4]. Protons as well as heavy ions can be accelerated to almost the speed of light inside the LHC. The protons first pass through a chain of smaller accelerators, namely the linear accelerator Linac2, the Booster and then the Proton Synchrotron as well as the Super Proton Synchrotron, reaching a centre-of-mass energy of 450 GeV before being injected into the LHC. In the accelerator the protons travel in bunches within two rings with counter-rotating beams that circulate at a frequency f_{rev} of about 11 kHz. Their paths are bent around the ring using superconducting twin bore magnets, with the main bending magnets reaching a nominal peak field strength of 8.33 T. Collisions can be observed at four main interaction points in large underground caverns which house the four major experiments: The all purpose detectors CMS and ATLAS³, as well as the LHCb⁴ and the ALICE⁵ experiments focusing on measurements of the quark flavour sector and heavy ion physics, respectively.

2.1.1 The HL-LHC Upgrade

An “event” refers to the products generated during a single collision of two protons. The number of events N_{event} that are generated per second in the collisions is determined by the event cross section σ_{event} as well as the instantaneous luminosity L [4]. The luminosity can be calculated from several beam parameters:

$$N_{\text{event}} = L \cdot \sigma_{\text{event}} \quad \text{where} \quad L = \frac{N_b^2 n_b f_{\text{rev}} \gamma_r}{4\pi \epsilon_n \beta^*} F \quad (2.1)$$

N_b	–	number of particles per bunch	ϵ_n	–	transverse beam emittance
n_b	–	number of bunches per beam	β^*	–	beta function at collision point
f_{rev}	–	revolution frequency	F	–	reduction due to crossing angle
γ_r	–	relativistic gamma factor			

Therefore the number of events generated per second can be maximised by maximising the luminosity of the collider. Since the start of the operation in 2010 the LHC has been continuously upgraded in order to maximise its luminosity (Fig. 2.1). During Run 1 and Run 2 a combined integrated luminosity of more than 190 fb^{-1} was achieved. By the end of Run 3 the LHC is expected to have generated an integrated luminosity of over 355 fb^{-1} . During a “Long Shutdown” (LS) starting at the end of 2024 (LS3) the LHC will be upgraded to the so-called “High Luminosity LHC” (HL-LHC). The main objectives of the upgrade project are to extend the lifetime of the LHC machine and to drastically increase the achievable luminosity, ultimately aiming at

¹Large Electron-Positron Collider

²Conseil Européen pour la Recherche Nucléaire (European Organization for Nuclear Research)

³A Toroidal LHC Apparatus

⁴LHC beauty

⁵A Large Ion Collider Experiment

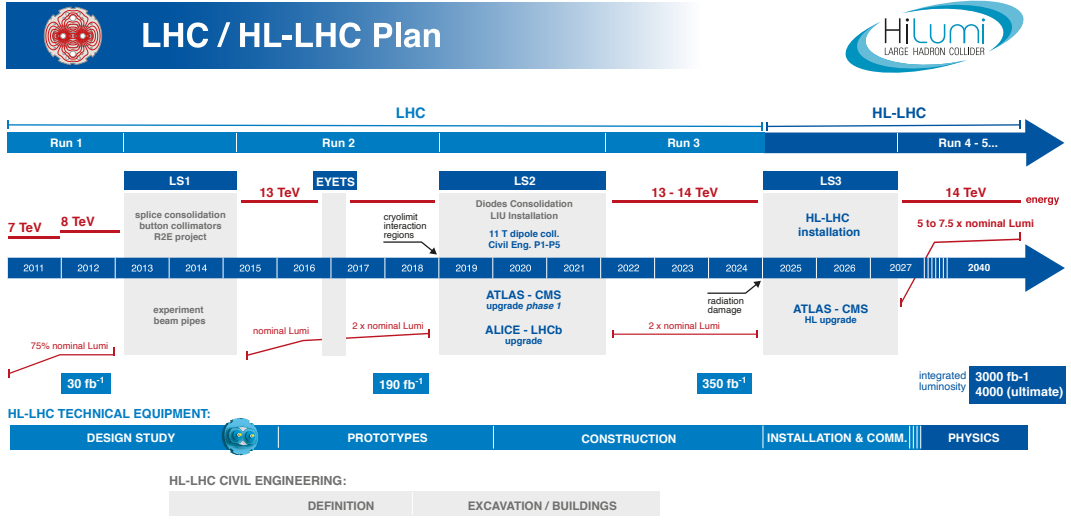


Figure 2.1: Timeline for the HL-LHC upgrade as well as overview over previous Runs and Long Shutdowns of the LHC [5].

an integrated luminosity of up to 4000 fb^{-1} during the projected lifetime of ten years [2]. The most significant change will be the replacement of the inner triplet quadrupole magnets in the insertion regions. Newly developed niobium-tin (Nb_3Sn) magnets reaching a peak field of nearly 12 T near the coils will be used. These magnets are stronger and have a larger aperture, thus reducing the beta function β^* and consequently increasing the luminosity (Eq. 2.1). However, a reduction of β^* requires a larger crossing angle, in turn also reducing F . This effect can be mitigated using superconducting RF crab cavities that tilt the bunches by half the crossing angle so that they overlap completely at the interaction point. Additionally constraints need to be put on the peak luminosity to limit the number of simultaneous collisions (pileup) during a single bunch crossing in the detectors. Therefore a compromise must be made between increasing the luminosity as much as possible, while keeping pileup as low as necessary for efficient distinction between events within the LHC detectors. Accepting pileup of up to 200 would allow for a peak instantaneous luminosity of $L_{\text{peak}} = 7.5 \cdot 10^{34} \text{ cm}^{-2}\text{s}^{-1}$.

2.2 The CMS experiment at the LHC

Figure 2.2 (left) shows a schematic drawing of the CMS detector. The magnetic field is generated by a superconducting solenoid consisting of a four layer winding made from a stabilised reinforced niobium-titanium (NbTi) conductor that is able to generate a homogeneous magnetic field of 3.8 T at its centre [6]. The magnet is connected to a cryoplant keeping it at an operating temperature of 4.5 K. The cold mass amounts to 220 t and the iron return yoke the magnet is embedded in weighs an additional 10,000 t.

The coordinate system adopted by CMS (Fig. 2.2, right) is centred at the nominal collision point, with the x -axis pointing towards the centre of the LHC tunnel, the y -axis pointing upwards and the z -axis pointing along the beam direction. The azimuthal angle ϕ is measured from the x -axis in the x - y plane, while the polar angle θ is measured from the z -axis. The pseudorapidity is defined as $\eta = -\ln \tan(\theta/2)$. Two regions are distinguished: The barrel region, which includes the parts of the detector that are placed parallel to the beam axis in concentric layers, and the

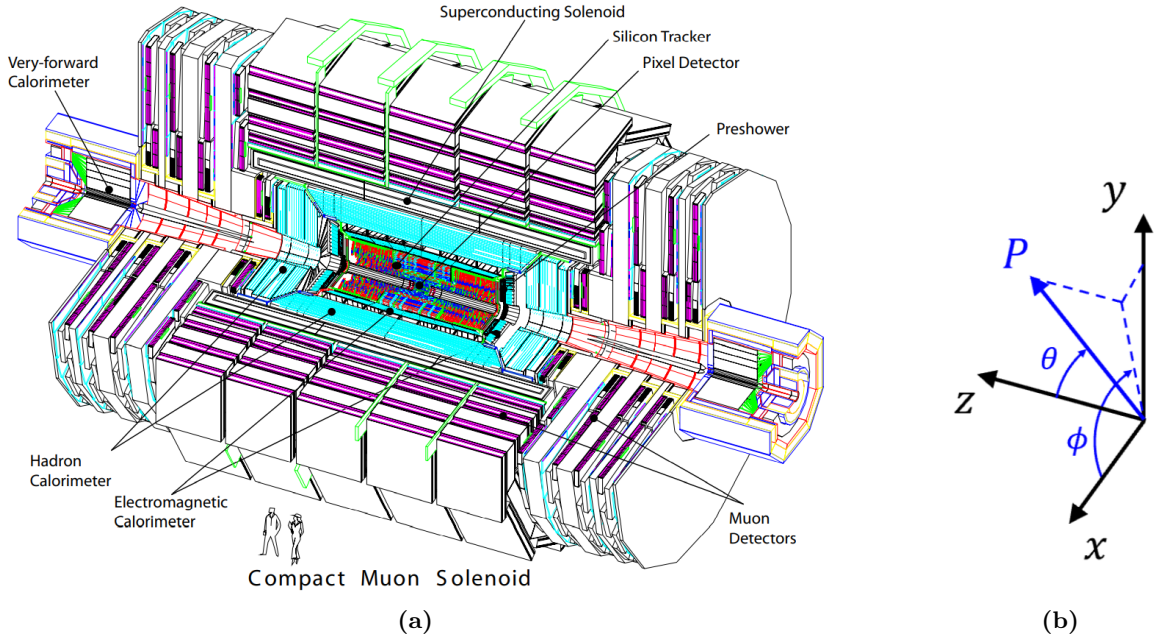


Figure 2.2: Schematic drawing of the CMS detector [6] (a) and right-handed coordinate system adopted by CMS, where θ refers to the polar and ϕ to the azimuthal angle (b) (adapted from Ref. [3]).

endcap regions at either end of the barrel, that lie orthogonal to the beam axis. The detector consists of several subdetectors in order to reconstruct trajectories, energy, charge and momentum of products of the proton-proton collisions. The subdetectors will be briefly introduced in the following paragraphs:

Muon system: The outermost part of the detector is the muon system that consists of about $25,000 \text{ m}^2$ of detection planes integrated into the iron return yoke. Three different types of gas filled chambers are used for muon detection. Drift tubes are used in the barrel region, while cathode strip chambers are used in the endcaps. Additionally resistive plate chambers are used in both regions to provide a fast and independent information for the trigger.

Calorimeters: To determine the energy of particles emerging from LHC collisions two calorimeters are placed within the solenoid. The hadronic calorimeter (HCAL) is positioned furthest away from the beam. Several layers of brass absorber plates and plastic scintillators are grouped into wedges around the barrel. The scintillator signals are read out using optical fibres. An optical decoding unit is used to bring the light to a hybrid photodiode, where the deposited energy is measured. An additional hadronic calorimeter is placed outside the solenoid in the forward region. Here the energy is measured through Cherenkov light. The electromagnetic calorimeter (ECAL) consists of over 60,000 lead tungstate (PbWO_4) crystals in the barrel region and over 7,000 in each of the endcaps. Scintillation photons emitted by the crystals are detected by avalanche photodiodes and vacuum phototriodes in the barrel and endcaps, respectively.

Tracker: The innermost subdetector is a tracking system based exclusively on silicon detector technology in order to provide precise and efficient measurement of trajectories of charged particles passing through the detector. The current CMS tracker is 5.8 m long and has a diameter of 2.5 m. It is composed of several layers of individual modules featuring silicon sensors. The part of the detector that is closest to the beam pipe is a pixel detector composed of four layers of pixel

modules that deliver precise points on each charged particles trajectory. The area around the pixel detector is occupied by the silicon strip tracker. It consists of single-sided strip modules as well as double-sided modules composed of two back-to-back silicon strip sensors with a stereo angle of 100 mrad that are arranged around the pixel detector. Efficient tracking is possible in a pseudorapidity region of $|\eta| \approx 2.5$.

Trigger: In the accelerator the high revolution frequency f_{rev} and the large number of bunches n_b per beam lead to a collision rate of 40 MHz. The amount of data that can be sent out of the detector and transferred to the back-end data processing system is limited by the bandwidth that can be provided by the electrical and optical data links. In order to limit the amount of data the detector has a two-staged trigger system. A pre-selection is made by the level one (L1) trigger with a trigger frequency of 100 kHz and the decision is propagated to the front-end. In the second stage - the High Level Trigger (HLT) - the full event information is available and a further differentiation is made. Events are stored for offline analysis at a rate of presently 1 kHz.

2.2.1 CMS Phase-2 Tracker Upgrade

To cope with the increased requirements posed by the HL-LHC upgrade the CMS detector will undergo extensive updates during LS3. In particular the entire silicon tracking system will be replaced. The radiation hardness will be improved. Additionally more pileup will increase the particle density and therefore also necessitate an increase of the granularity of the detector. Other changes include [3]:

- **Reduced material in the tracking volume:** A main focus when designing detector components is to disturb the trajectory of the particles as little as possible. Additional material in the tracking volume will also increase the “fake rate” (fraction of fake tracks in the set of all reconstructed tracks) e.g. due to multiple scattering of the particles. This will also impact the performance of other detector subsystems like the calorimeters. Therefore materials used in the detector should be as light as possible and should have a large radiation length.
- **Extended tracking acceptance:** The new layout of the detector is shown in Figure 2.3. The so-called “Inner Tracker” (IT) consists of four layers of pixel modules (green and yellow), while the “Outer Tracker” (OT) is made up of PS modules (blue) and 2S modules (red). The new design ensures that particles from the luminous region traverse on average more than six layers of modules up to $|\eta| \approx 4$. Therefore efficient tracking will be possible in a pseudorapidity region of up to $|\eta| \approx 4$ compared to presently $|\eta| \approx 2.5$.
- **Contribution to the L1-trigger:** Presently, only information from the muon chambers and the calorimeters are included in the L1-trigger. After the upgrade tracking information will also be included in the first trigger level. For this purpose new modules have been designed for the OT which will be explained in more detailed in the following sections.

The IT will be subjected to the harshest conditions as it is closest to the beam pipe. Silicon sensors segmented into pixels will be used to deliver the desired performance and radiation tolerance. The IT will be installed on inclined rails, so that the detector can be extracted without removing the beam pipe itself. This enables the replacement of degraded parts during an extended year-end technical stop.

The driving factor in the development of the module concept for the OT is the inclusion of tracking information in the L1 trigger. For this purpose two types of double-sided modules were designed, that are capable of rejecting signals from particles with low transverse momentum p_T (“ p_T modules”):

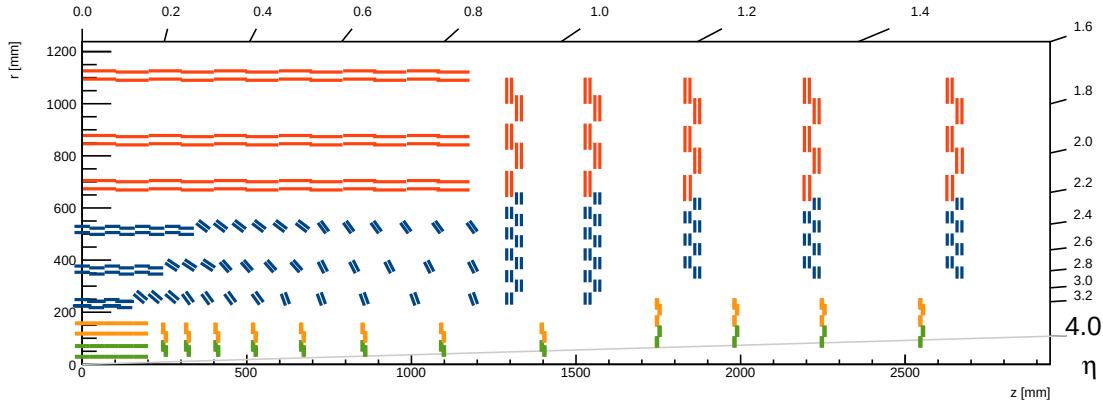


Figure 2.3: One quarter of the Phase-2 tracker layout. Pixel modules of the Inner Tracker are shown in green and yellow. PS modules are shown in blue and 2S modules in red (adapted from Ref. [3]).

- **2S modules:** These modules are equipped with two silicon strip sensors (2S) with the strips on the bottom and top sensor being parallel to each other. The direction of the strips is either parallel to the z -axis (barrel) or nearly radial (endcaps).
- **PS modules:** These modules are equipped with a strip sensor (PS-s sensor) on one and a macro-pixel sensor (PS-p sensor) on the other side. This makes it possible to constrain the z -coordinate and r -coordinate in the barrel and the endcaps, respectively. A more detailed description of the PS module is given in Chapter 2.2.2 as studies presented in this thesis were performed on the power hybrid of the PS module.

When a particle passes through a detector module, hits are registered in both sensors on either side of the module. The sensors are read out by on-module chips that correlate the hits in both sensors and a partial track of the particle through the module can be reconstructed. The trajectory of a particle with high transverse momentum p_T is less curved in the magnetic field of the CMS detector than that of a particle with lower transverse momentum. If the transverse momentum p_T of the particle is above a certain threshold hits in both sensors are registered within a programmable acceptance window and its track through the module forms a so-called “stub”. For this to work effectively in all regions of the tracker, modules with different gaps between the two sensors need to be assembled: 1.8 mm and 4.0 mm gaps for the 2S modules as well as 1.6 mm, 2.6 mm, and 4.0 mm gaps for the PS modules, respectively. Additionally, the PS modules in the barrel region are progressively tilted in order to increase the stub finding efficiency (Fig. 2.3).

2.2.2 The PS module

An exploded view of the PS module is shown in Figure 2.4. It has two rows of 2.4 cm long strips (1, PS-s sensor) on one side and 32 rows of 1.5 mm long macro-pixels (2, PS-p sensor) on the other side [3]. N-in-p sensors in which the signal is mostly generated by drifting electrons are used. The strip sensors are wire bonded directly to the FEH⁶ (3), where they are read out by eight Short Strip ASICs⁷ (SSA). The macro-pixel sensors are read out via Macro-Pixel ASICs (MPAs) that are bump bonded directly onto the pixelated sensor and connected to the FEH through wire bonds. The Concentrator Integrated Circuit (CIC) implemented on the FEH formats the signal in data packets containing trigger information as well as raw data from events that passed the L1 trigger. The data is then passed on to the LpGBT⁸ which is located on the

⁶Front-End Hybrid

⁷Application Specific Integrated Circuit

⁸Low-power GigaBit Transceiver

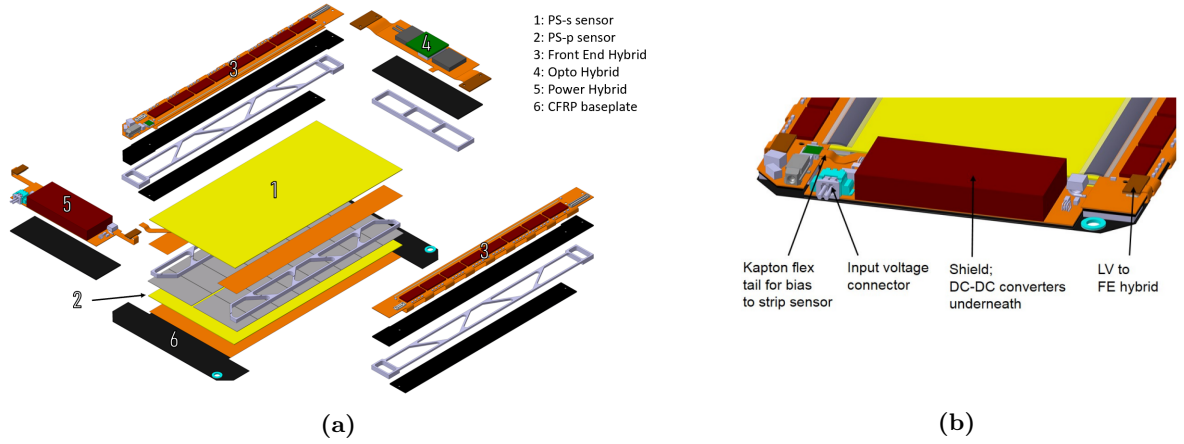


Figure 2.4: CAD drawings of an exploded view of the PS module (a) and the PS-POH (b) (adapted from Ref. [3]).

Opto Hybrid (4). The LpGBT serializes the data and passes it on to the VTRx+⁹ optoelectronic transceiver that is responsible for the connection to the back-end. The necessary voltages for the front-end electronics are supplied by the PS-POH (5) via kapton flex tails (Fig. 2.4, b). The module is cooled through a baseplate (6) made from CFRP¹⁰ that is glued onto the supporting structure, through which the cooling pipe runs.

A two-stage powering scheme (Fig. 2.5, b) is used to power the module. One DC-DC converter is used in the first stage to convert the 7.5 V input voltage V_{in} to the required 2.55 V for the optoelectronics. In the second stage two additional DC-DC converters convert the 2.55 V to the 1.0 V and 1.25 V that are required for the front-end electronics. The DC-DC converters used are buck converters developed at CERN (bPOL12V¹¹ in the first and bPOL2V5 in the second stage) [7, 8]. Power loss on the supply cables is proportional to the square of the current I^2 passing through the cable. Supplying power to the front end at a higher voltage V_{in} reduces the feed current I by the conversion ratio $r = V_{in}/V_{out}$ of the DC-DC converters. Consequently the power loss along the cable can be reduced by the square of the conversion ratio r^2 . This enables the use of supply cables up to 80 m in length which makes it possible to locate the power supplies in more remote areas like the galleries of the experimental cavern, where the radiation requirements are less strict. Each low voltage power supply (LVPS) is expected to feed up to 12 silicon front-end modules. A trunk cable (cable 1) providing both the high voltage (HV) and low voltage (LV) is connected to the power supply. From the break point at tracker patch panel 1 (PP1), a lighter cable (cable 2) brings the power inside the OT volume. At patch panel 0 (PP0), cable 2 is fanned out to feed the individual modules (Fig. 2.5, a).

⁹Versatile **T**Ransceiver plus

¹⁰Carbon **F**ibre **R**einforced **P**olymer

¹¹The name bPOLy-Vz.# is composed of the maximum input voltage rating (y), the voltage rating of the technology used for the design (z), and the version number (#). bPOL stands for the converter topology, in this case “buck **P**oint **O**f **L**oad”.

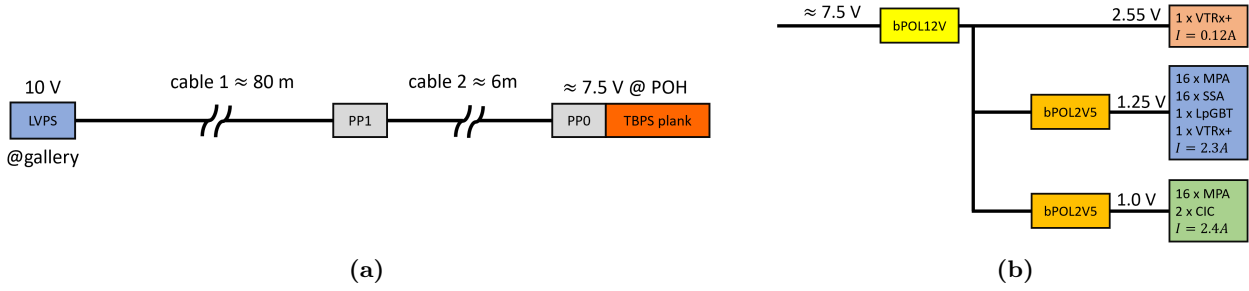


Figure 2.5: Sketch of the powering scheme in the detector: example of power distribution line for a PS barrel plank (a) and two-stage powering scheme used to power the PS front-end electronics (b) (adapted from Ref. [3]).

2.3 DC-DC converters

The DC-DC converters used on the PS-POH are so-called synchronous step-down buck converters, i.e. the output voltage is always smaller than the input voltage. The basic circuit of the DC-DC converter is highlighted in blue in Figure 2.6. The main components are an inductor with inductance L used for energy storage and a capacitor with capacitance C_{out} to smoothen the output voltage. Synchronous DC-DC converters use two switches which are realized in the bPOL technology using N- and P-channel MOSFETs¹² (NMOS and PMOS). Depending on the state of the switches two circuit configurations are realized [9]:

- If the high side switch (PMOS) is ON and the low side switch (NMOS) is OFF energy is delivered to the inductor L . The magnetic field generated by the inductance delays the current flow through the load R_{Load} .
- When the high side switch (PMOS) is OFF and the low side switch (NMOS) is ON, the voltage source is disconnected and the current at the load decreases. The inductor now acts as a current source and the stored energy is pushed into the output.

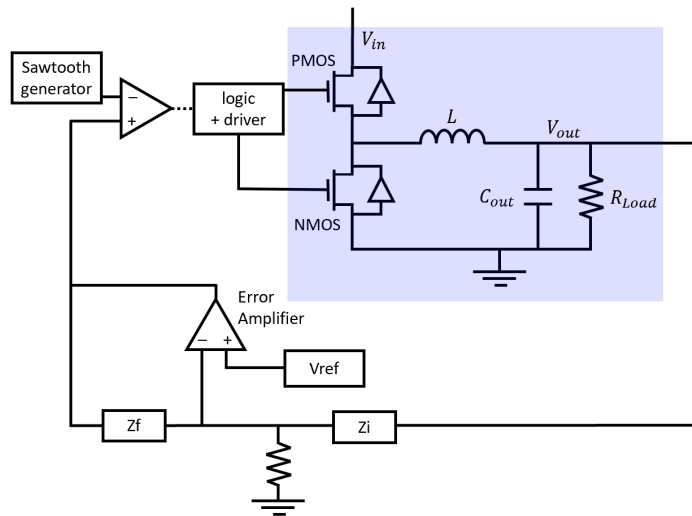


Figure 2.6: Block diagram of a typical buck converter (blue) with embedded voltage mode control loop (adapted from [10]).

¹²Metal-Oxide-Semiconductor Field-Effect Transistor

Switching continuously between these configurations leads to a square wave voltage at the input and output of the inductor (Fig. 2.7, top). If the switching frequency f is high enough the time constant τ of the LC circuit is much larger than the switching period $T = 1/f$ of the converter the inductor never fully saturates during the switching cycle. In this case a linear current flow through the inductor can be assumed and the output current is a direct current I_{out} with a triangular modulation (Fig. 2.7, bottom).

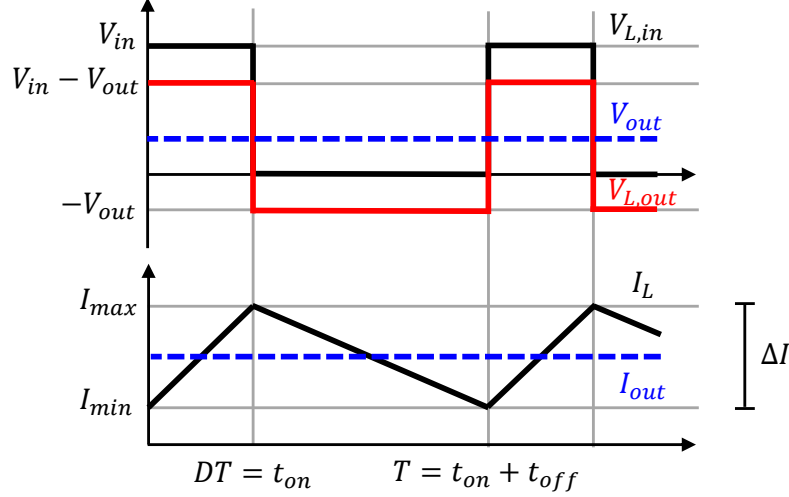


Figure 2.7: Time dependent behaviour of the current (bottom) and voltages (top) generated in the inductor of an ideal step-down converter.

The voltage V_L across the inductor is correlated to the change in current:

$$V_L = \frac{dI_L}{dt} L \quad . \quad (2.2)$$

The energy stored in the inductor at the beginning of the cycle $t = 0$ must be the same as at the end of the cycle $t = T$. Therefore the increase in current ΔI_{ON} in the time t_{on} in which the PMOS is switched on must be equal to the decrease ΔI_{OFF} in current in the time t_{off} in which the PMOS is switched off. Using Equation 2.2 and integrating over t yields:

$$0 = \Delta I_{ON} + \Delta I_{OFF} = \frac{V_{in} - V_{out}}{L} t_{on} - \frac{V_{out}}{L} t_{off} \quad . \quad (2.3)$$

This can be solved for V_{out} :

$$V_{out} = \frac{t_{on}}{t_{on} + t_{off}} V_{in} = \frac{t_{on}}{T} V_{in} = D V_{in} \quad (2.4)$$

where D is the so-called "duty cycle". This also means that the peak to peak current ΔI can be expressed as:

$$\Delta I = \frac{V_{in} - V_{out}}{L f} D \quad . \quad (2.5)$$

Equation 2.5 also illustrates that a high switching frequency allows for smaller values for the inductance L and consequently a smaller inductor while ΔI stays constant [9]. This is desirable as the design of all detector components must comply with the material budget of the experiment.

2.3.1 The bPOL topology

The ASICs that are used on the POH need to work reliable in the harsh radiation conditions within the detector. Therefore they are developed by CERN specifically for use in the LHC

experiments. They are fully integrated buck converters with an embedded voltage mode control loop [7, 8]. The converter is enabled when sufficient voltage is supplied to the enable pin. A predefined soft-start procedure is implemented to avoid large inrush currents at the startup of the converter. Additionally protection features are implemented that disable the converter if the current is too high or too low (OCP_pos and OCP_neg: positive and negative Over-Current Protection), if the operating temperature is too high (OTP: Over-Temperature Protection) or if the input voltage is too low for the on-chip regulators to function correctly (UVL: Under-Voltage Lockout). The thresholds for these protections as well as those for regular turn-on and turn-off of the converters are summarized in Table 2.1. A simplified block diagram of the bPOL

		bPOL12V	bPOL2V5
Parameters for Enable/Disable			
Enable	Enable start threshold	800 mV	810 mV
	Enable stop threshold	500 mV	360 mV
Duration of soft-start		520 μ s	410 μ s
Protection Features			
Over-Current Protection	OCP_pos	7.2 A	4.7 A
	OCP_neg	—	-0.9 A
Over-Temperature Protection	T rising trip level	120 °C	102 °C
	T falling trip level	80 °C	96 °C
Under-Voltage Lockout	V _{in} rising trip level	5.5 V	1.82 V
	V _{in} falling trip level	5 V	1.63 V

Table 2.1: Summary of parameters relevant for enabling/disabling of bPOL12V and bPOL2V5 as well as thresholds for protection features [7, 8].

topology is shown in Figure 2.6. The control loop is used to determine the on- and off-times of the transistors. In the Error Amplifier the output voltage of the converter is compared to a reference voltage¹³ and the difference is propagated to a comparator where it is compared to the output of the sawtooth generator. If the output voltage is too low the difference is higher than the sawtooth signal for a longer period of time and the PMOS is turned on for a longer time as well, consequently increasing the output voltage (Eq. 2.4), and vice versa. This is called “Pulse width modulation”.

Different modes of operation depending on the current flow through the inductor can be distinguished when discussing the optimization of the DC-DC converter. The mode of operation in which the current through the inductor never falls to zero is called “continuous mode”. Additionally small negative currents are allowed during continuous operation. This special case of the continuous mode operation is called Quasi Square Wave (QSW). In order to prevent the converter from short-circuiting the PMOS and NMOS transistors must never be turned on at the same time. The time during which both converters are turned off is called “dead-time”. On the bPOL an adaptive logic is implemented to reduce the dead-time as much as possible in QSW mode to optimize the efficiency of the converter [10].

2.4 The PS Power Hybrid

In this thesis electrical testing was performed on the most recent prototype of the PS-POH which was developed by the I. Physikalisches Institut B at RWTH Aachen University. Figure 2.8

¹³This is implemented using a bandgap reference which generates a temperature independent voltage, that is close to the theoretical bandgap of silicon.

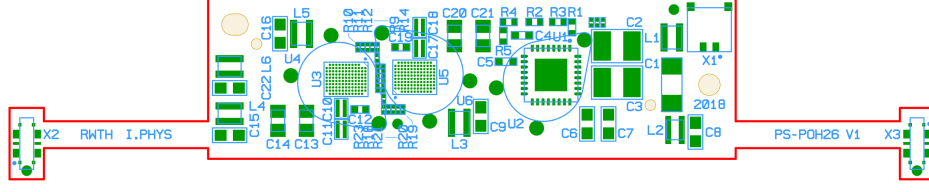


Figure 2.8: *Layout of the PS-POH prototype.*

shows the layout of the prototype. Additionally a photograph of the prototype is provided in Figure 2.10. As described above buck point of load converters developed at CERN are used. This is the first prototype that uses the bPOL12V_v25.4 converter in the first stage providing the 2.55 V voltage needed to feed the second stage converters and the optoelectronics. In the second stage the newest version of the bPOL2V5 converter - the bPOL2V5_v3.2¹⁴ - is used. Detailed schematics of the implementation of all three chips on the PS-POH prototype are provided in Figures A.1 and A.2 in Appendix A. A few relevant details will be pointed out in the following paragraphs.

Figure 2.9 shows how the bPOL12V is integrated on the PS-POH prototype. Pi-Filters (red) are placed before and after the converters to reduce voltage ripple. The switching frequency can be varied by changing a resistor (green) placed at pin 1 of the converter. In this case the 130 kΩ resistor sets the switching frequency to 1.99 MHz [7]. bPOL12V is enabled via a voltage divider (blue) so that the necessary input voltage U_{in} can be calculated from the voltage applied to the enable pin U_{BUCK_ENABLE} :

$$U_{in} = \frac{R_{25} + R_{24}}{R_{25}} \cdot U_{BUCK_ENABLE} \quad (2.6)$$

Consequently, the input voltages required for enabling and disabling the converter can be changed by changing the value of resistor R_{25} . Thresholds for two different voltage dividers studied in this thesis are summarized in Table 2.2.

Supply voltages of 1.25 V and 1.0 V are necessary to feed the front-end electronics. In the course of an ongoing master thesis at RWTH Aachen university significant voltage drops across the PCB were discovered and characterized. To compensate for these voltage drops across the PCB the output voltages of the second stage converters have been raised to 1.5 V and 1.3 V by changing resistors R_{14} and R_{23} in the voltage dividers placed at the outputs of the bPOL2V5 converters to 301 kΩ and 249 kΩ, respectively. Similarly to bPOL12V the switching frequency of bPOL2V5 is also set by a resistor. The 69.8 kΩ resistor used for both bPOL2V5 converters leads to a switching frequency of about 3.8 MHz. Likewise Pi-Filters are used at the input and output of the bPOL2V5 converters to reduce voltage ripple.

In total three PS-POH prototypes were assembled for this thesis. Two POHs (POH 1 and

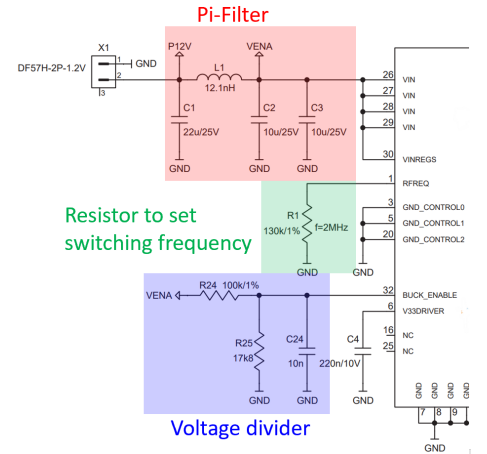


Figure 2.9: *Schematic of bPOL12V on the PS-POH prototype. Parts of the circuit described in the text are highlighted.*

¹⁴The “v3” in the name is short for 3.3 V.

POH 2) were assembled using $R_{25} = 17.8 \text{ k}\Omega$ in the enable voltage divider of bPOL12V. However this leads to enable/disable thresholds that are very close to the thresholds for UVL (Tab. 2.1). Therefore a third POH (POH 3) was assembled using $R_{25} = 9.09 \text{ k}\Omega$ instead.

		Enable threshold / V	Disable threshold / V
R_{25}	17.8 k Ω	5.3	3.3
	9.09 k Ω	9.6	6.0

Table 2.2: Nominal enable and disable thresholds with regards to the value of resistor R_{25} placed in the voltage divider.

The output voltages of the converters are brought to the front-end electronics using flex tails that wrap around the FEHs outside edge. During testing nominal loads were applied to connectors at the end of these flex tails (Tab. 2.3). All three converters require air-core inductors

Output	Load
P1V3	1198 mA per side
P1V5	1135 mA per side
P2V55	70 mA at X_2

Table 2.3: Nominal loads at each converter output. X_2 refers to Figure 2.8.

as energy storage, because ferrite inductors would saturate in the magnetic field of the CMS detector. On the prototype one 220 nH and two 100 nH toroids are used for the first and second stage converters, respectively. During previous studies the DC-resistance of these coils was measured to be approximately 50 m Ω and 31 m Ω , respectively. To protect the silicon sensors from electromagnetic radiation from the converters a 150 μm thick aluminium shield is soldered to the POH. The shield is soldered completely along the long edges. All components are placed on a 4-layer flex PCB with nominally 15 μm copper thickness. Figure 2.10 shows a photograph of the prototype both without and with the shield soldered to the PCB.

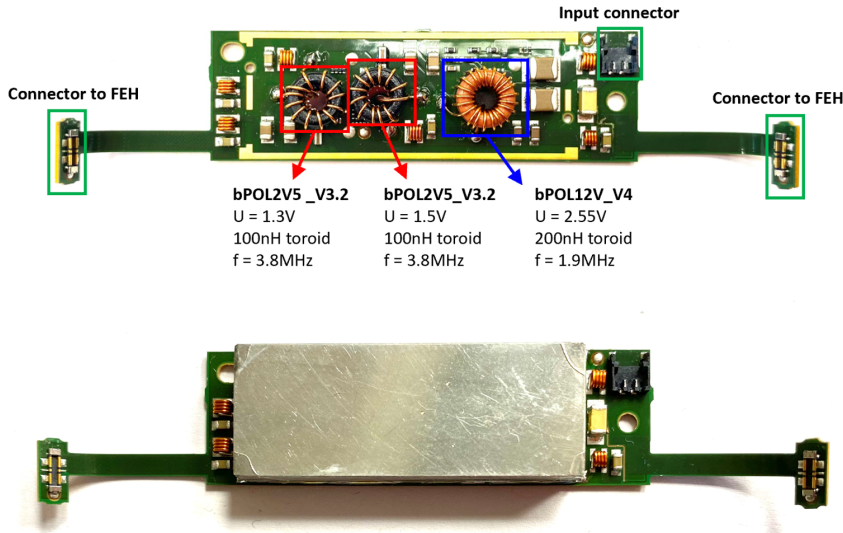


Figure 2.10: Photograph of a PS-POH prototype without shield (top) and with shield (bottom).

3 Dynamic behaviour and efficiency of the PS-POH

In the following chapter measurements of the dynamic behaviour of the PS-POH prototype and its efficiency will be presented. Dynamic measurements not only ensure the two stage powering scheme outlined above works as expected but also reveal details about the current consumption of the prototype during turn-on and turn-off which is important for the development of the power supply. Additionally it is important confirm that no spikes in the output voltages of the converters are visible during these measurements as this might impact the front-end electronics. The efficiency is another important measure used to characterize the PS-POH prototype. Power losses on the PS-POH will lead to more heat dissipated in the tracking volume which might ultimately affect the performance of the silicon sensors. In some of these measurements the DC-DC converters on the PS-POH prototype did not behave as expected. These behaviours have been improved upon in newer versions of the converters and are summarized at the end of the chapter.

3.1 Experimental Setup

Figure 3.1 shows the setup used for the dynamic and efficiency measurements. In Figure 3.2 a schematic drawing of the setup is provided. The POH is placed on an aluminium plate and clamped down using 3D-printed spacers of 6-7 mm height (1). This plate is then placed on Peltier Modules which are connected to the corresponding controller (2, BELEKTRONIG Temperature Controller [11] connected to BELEKTRONIG OEM Peltier Modules [12]). This is relevant for the efficiency measurements that will be discussed later, as previous studies have shown a temperature dependence of the efficiency [13]. The controller is turned off during the dynamic measurements to minimise noise in the output voltages.

The output connectors of the POH are connected to a so-called “crossover board” (3, developed at RWTH Aachen - schematics in Figures A.3 and A.4 in Appendix A) at which the output voltages can be measured using passive oscilloscope probes (4, Teledyne LeCroy PP009 passive probe [14]). Because of the amount of relevant traces measurements are performed in parallel with a WaveRunner oscilloscope (5, Teledyne LeCroy WaveRunner [15]) and a PicoScope (6, PicoScope [16]). To measure the input current, a current clamp (7, Teledyne LeCroy CP031 Current Probe [17]) is used. Various loads can be applied at the output connectors of the POH via a Patch Panel (8) that is connected to a Load Board (9). The Load Board is powered by a power supply (10, ROHDE&SCHWARZ HMP4040 Four-Channel Power Supply [18]) and cooled using an external fan. The corresponding Load Board Interface (11) is used to connect the Load Board to a computer where loads applied to the individual channels can be controlled using a LabView VI¹. The Load Board and Load Board Interface as well as the Patch Panel were developed at RWTH Aachen and their schematics can be found in Appendix B.

The powering scheme (Fig. 3.3) is implemented such that it represents the powering scheme in the detector (Fig. 2.5) as close as currently possible. The POH is powered using a floating power supply (CAEN Mod. A1516 B 6 Ch. floating low voltage board [19]) housed in a crate (CAEN SY2527 Universal Multichannel Power Supply System [20]) and controlled through the

¹Virtual Interface

corresponding software interface. The POH is connected to an adapter that connects to a 65 m long prototype of the PS-PP1 cable (HABIA CABLE, CERN LVPS-PP1 [21]) which in turn is connected to the power supply. The Low Voltage cores used to supply power to the POH prototype and their return are marked in orange and blue, respectively. Alternatively measurements without the PS-PP1 cable can be performed, by plugging the adapter directly into the power supply. In the detector the power supply will be turned on and turned off at a speed of 100 V/s [22]. This is not possible with this setup due to specifications of the CAEN power supply [19]. The fastest possible controlled ramp speed of the power supply is 29 V/s. During this controlled ramp the power supply will increase/decrease its output voltage in steps of around 0.5 V until it reaches its final value. When not specifying a fixed ramp speed the power supply ramps as fast as possible at ~ 1000 V/s.

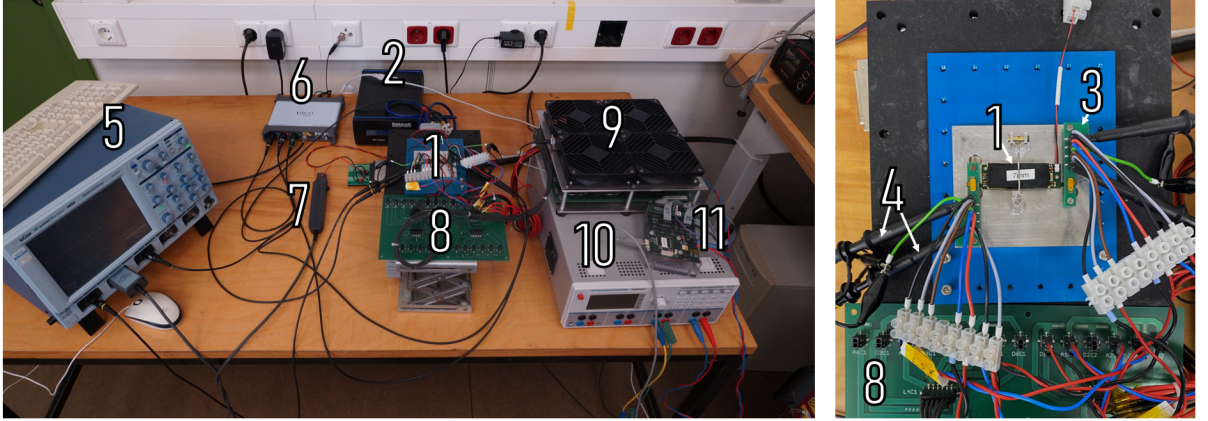


Figure 3.1: Setup for electrical testing. Details are given in the text.

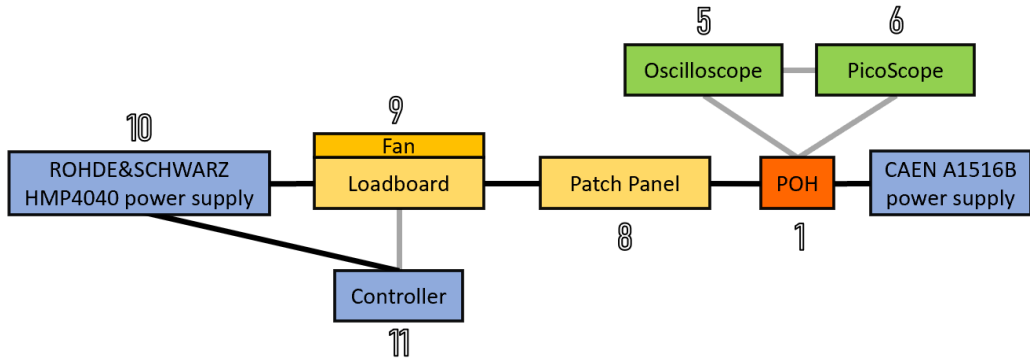


Figure 3.2: Schematic drawing of the setup used for electrical testing of the POH prototype. Power lines are marked in black, while lines for transfer of data are marked in grey.

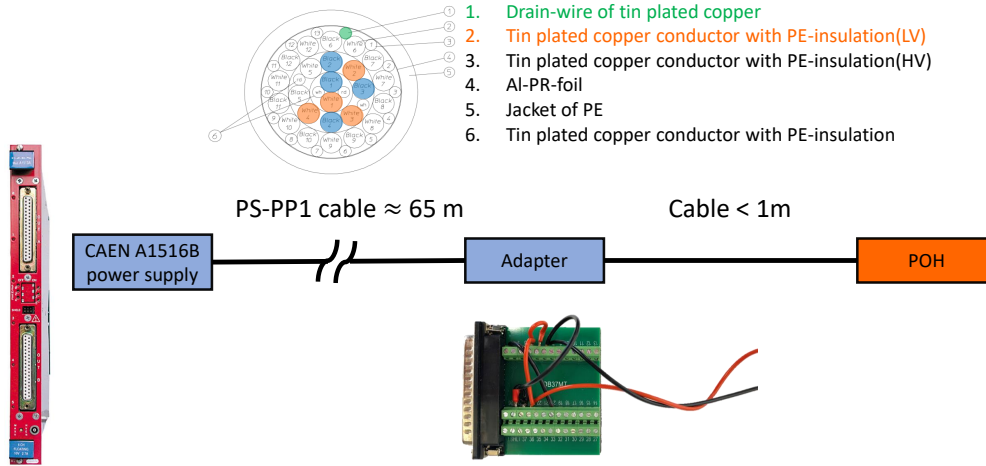


Figure 3.3: Schematic drawing of the powering scheme used for electrical testing of the POH prototype. A cross-section of the PS-PP1 cable is shown above with low voltage cores and their returns marked in orange and blue, respectively.

3.2 Dynamic behaviour

For this thesis a multitude of dynamic measurements was performed and analyzed. Turn-on and turn-off sequences as well as sudden large load changes were examined. Measurements were performed on all three of the assembled prototypes both with and without nominal loads (Tab. 2.3) applied at the output connectors. All of these measurements were repeated with and without the PS-PP1 cable as well as with and without the controlled power supply ramp discussed previously. In the following sections a few selected measurements will be discussed in detail. An overview of the results will be given at the end of Chapter 3.2.

3.2.1 Turn-on sequence

As discussed in Chapter 2.4, bPOL12V is enabled via a voltage divider when the input voltage passes a certain threshold (Tab. 2.2). The output voltage of bPOL12V serves the second stage converters. Consequently they are enabled once the output voltage of bPOL12V is sufficiently high (Tab. 2.1). To characterise the turn-on sequence the output voltages of all three converters as well as the Power Good signal were measured. The Power Good output pin is used to signal that bPOL12V is working correctly. If any of the protection features described above is triggered or if the converter is disabled the voltage at the Power Good pin will be zero. Additionally the input voltage and input current were recorded. The oscilloscopes are triggered once the positive edge of the input voltage surpasses 5 V. Nominal loads (Tab. 2.3) were applied at the output connectors. Two measurements of the turn-on sequence will be discussed in the following sections. During the first measurement neither the PS-PP1 cable nor a controlled power supply ramp were used. The second measurement more closely resembles the conditions in the detector as both the PS-PP1 cable and the 29 V/s power supply ramp described above were used.

1. Turn-on sequence without PS-PP1 cable and without power supply ramp

Figure 3.4 shows the turn-on sequence of the POH. The output voltages of the three converters increase gradually until they reach their nominal value. The gradual increase is due to the soft-start procedure of the converters, that limits the inrush current.

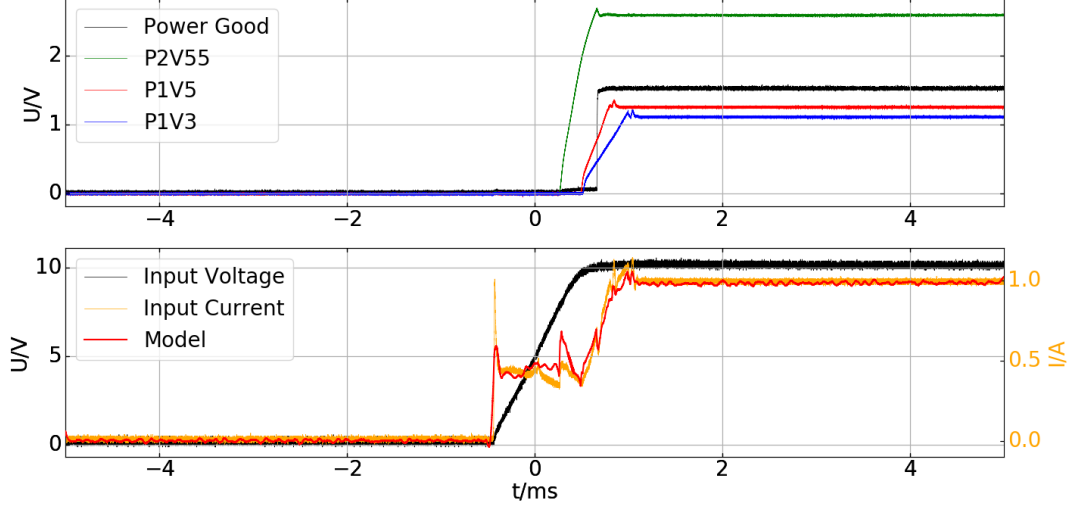


Figure 3.4: Turn-on sequence of POH 2 using a fast power supply ramp as well as a short supply cable. The input current (yellow) and voltage (black) as well as the model discussed in the text (red) are shown in the lower plot, while the upper plot shows the output voltages (bPOL12V in green; bPOL2V5 in red/blue) as well as the Power Good flag (black). The same colour scheme will be used in all following measurements.

The times for the soft-start procedure are determined from the turn-on sequences for all three POH prototypes (Tab. 3.1) by taking the difference of the time at which the output voltage of the converter first increases above zero and the time at which the output voltage reaches its first peak. The duration of the soft-start of bPOL2V5 is always a bit shorter for the converter with the 1.5 V output voltage than for the converter with 1.3 V output voltage, even though no dependence of the soft-start duration on the output voltage is specified in the data sheet [8]. The nominal values for the soft-start duration are 520 μs for bPOL12V and 410 μs for bPOL2V5 (Tab. 2.1). However, when comparing the results to the nominal values it is important to note that it is not stated in the data sheet how much variation is expected or acceptable. The duration of the bPOL12V soft-start procedure is around 100 μs less than the nominal value for all three prototypes. The duration of the bPOL2V5 soft-start procedure varies by 150 μs around the nominal value.

	bPOL12V	bPOL2V5 ($U_{\text{out}} = 1.5 \text{ V}$)	bPOL2V5 ($U_{\text{out}} = 1.3 \text{ V}$)
POH 1	410 μs	340 μs	510 μs
POH 2	400 μs	310 μs	480 μs
POH 3	430 μs	550 μs	580 μs

Table 3.1: Summary of the duration of the soft start procedures for each converter and all POH prototypes. Each value is measured multiple times across several measurements. The uncertainty of these values can be estimated to $\sigma \approx 10 \mu\text{s}$.

In all three converters a small decrease in output voltage can be observed at the end of the

soft-start procedure. This happens because the reference to the Error Amplifier is switched to the bandgap reference (the Error Amplifier is part of the voltage mode control loop depicted in Fig. 2.6). In the output voltages of the bPOL2V5 converters a second peak can be observed. This happens because the low side switch operates significantly slower during the soft-start. After the soft-start the turn-on/-off time of the low side switch is decreased again to optimize the efficiency. This causes the second voltage step [23].

The POH experiences a large inrush current once the power supply is turned on (Fig. 3.4, bottom). This can be explained by the charging of capacitors with capacitance C placed before the first stage converter:

$$I_{\text{in}} = \frac{dU_{\text{in}}}{dt} \cdot C \quad . \quad (3.1)$$

Similarly once the bPOL12V is enabled capacitors with capacitance C' placed before the bPOL2V5 converters are charged. Once all converters are enabled the capacitors C'' placed at the output of bPOL2V5 are charged as well. Assuming lossless ($P_{\text{in}} = P_{\text{out}}$) operation of the converters themselves the current I_{out} generated by the charging of capacitors after the converter influences the input current I_{in} as follows:

$$P_{\text{in}} = I_{\text{in}} \cdot U_{\text{in}} \stackrel{!}{=} P_{\text{out}} = I_{\text{out}} \cdot U_{\text{out}} \quad \Rightarrow \quad I_{\text{in}} = I_{\text{out}} \cdot \frac{U_{\text{out}}}{U_{\text{in}}} \quad . \quad (3.2)$$

This can be expressed using only the input voltage U_{in} and nominal output voltage U_{out} of the converters using Equation 3.1:

$$I_{\text{in}} = \frac{dU_{\text{out}}}{dt} \cdot \frac{U_{\text{out}}}{U_{\text{in}}} \cdot C \quad . \quad (3.3)$$

The load applied at the output of the POH also influences the input voltage. Inefficiencies due to the large voltage drops across the flex tails of the POH need to be taken into account when dealing with the absolute values of the output voltages measured at the output connectors. Therefore an efficiency of $\eta \approx 54\%$ for the whole POH was estimated. Assuming nominal loads (Tab. 2.3) at the output connectors, the output power P_{out} can be calculated at each point by multiplying each measured output voltage with the corresponding nominal load:

$$I_{\text{in}} = \frac{P_{\text{out}}}{U_{\text{in}} \cdot \eta} \quad \text{where} \quad P_{\text{out}} = U_{\text{P2V55}} \cdot 70 \text{ mA} + U_{\text{P1V5}} \cdot 2270 \text{ mA} + U_{\text{P1V3}} \cdot 2396 \text{ mA} \quad (3.4)$$

From these considerations the following model can be extracted to predict the input current:

$$I_{\text{in,model}} = \frac{dU_{\text{in}}}{dt} \cdot C + \frac{dU_{\text{P2V55}}}{dt} \cdot \frac{2.5 \text{ V}}{10 \text{ V}} \cdot C' + \left(\frac{dU_{\text{P1V3}}}{dt} \cdot \frac{1.3 \text{ V}}{10 \text{ V}} + \frac{dU_{\text{P1V5}}}{dt} \cdot \frac{1.5 \text{ V}}{10 \text{ V}} \right) \cdot C'' + \frac{P_{\text{out}}}{U_{\text{in}} \cdot \eta} \quad (3.5)$$

The values for the capacities are given in the schematics (Figures A.1 and A.2 in Appendix A). All capacitors are placed in parallel to each other. Therefore the total capacity is given by the sum of the individual capacities, which yields $C = C'' = 42 \text{ pF}$ and $C' = 74.8 \text{ pF}$. This model is plotted in red in Figure 3.4. In order to calculate the derivative of the output voltages the signal is first smoothed using a Savitzky-Golay filter ². The derivative is then determined by calculating the slope between two successive data points. The sharp increase in current once the power supply is turned on is modelled correctly. Similarly the sharp increase in current once the first stage turns on can be modelled. The slower incline caused by the gradual increase in the output voltages of the converters during soft-start is reflected in the model as well. Even small peaks in the input current due to the peaks at the end of the soft-start procedure of the converters are represented by the model.

²A third order polynomial is fitted to successive subsets of 1,001 data points.

2. Turn-on sequence using the PS-PP1 cable and a 29 V/s power supply ramp

The measurement (Fig. 3.5) performed with the 65 m long PS-PP1 cable and the 29 V/s power supply ramp simulates the conditions of the powering scheme in the detector more accurately. Due to the threshold for UVL being very close to the enable threshold of the bPOL12V converter, the voltage drop across the supply cable once the converters are enabled is sufficient to trigger UVL and the bPOL12V disables, consequently also disabling the second stage converters. Once the converters are disabled the input voltage increases and the bPOL12V converter as well as the bPOL2V5 converters enable again. This leads to a series of consecutive turn-ons and turn-offs of the converters (a zoomed in view is shown in Fig. 3.5) which only stops once the input voltage is high enough above the UVL threshold.

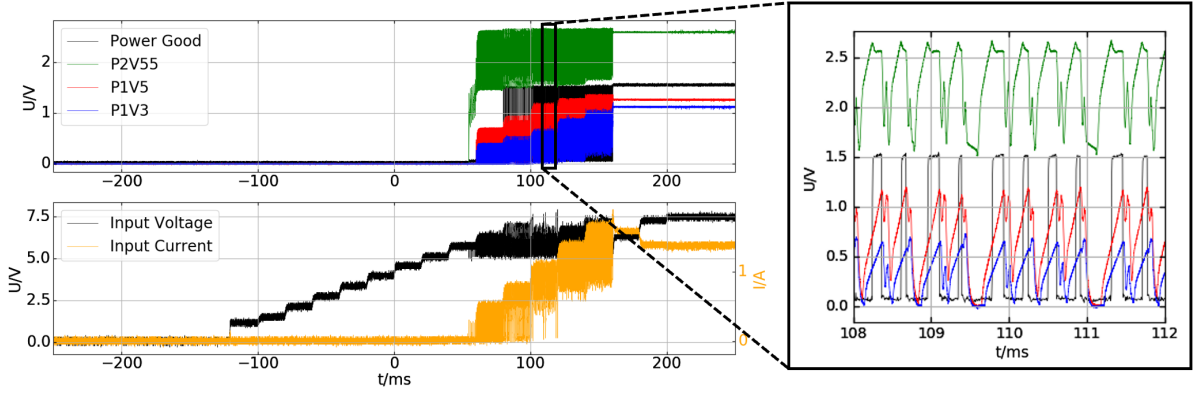


Figure 3.5: Turn-on sequence of POH 2 using a slow 29 V/s power supply ramp and the PS-PP1 supply cable (left) as well as enlarged view of consecutive turn-on/-off of converters due to UVL (right).

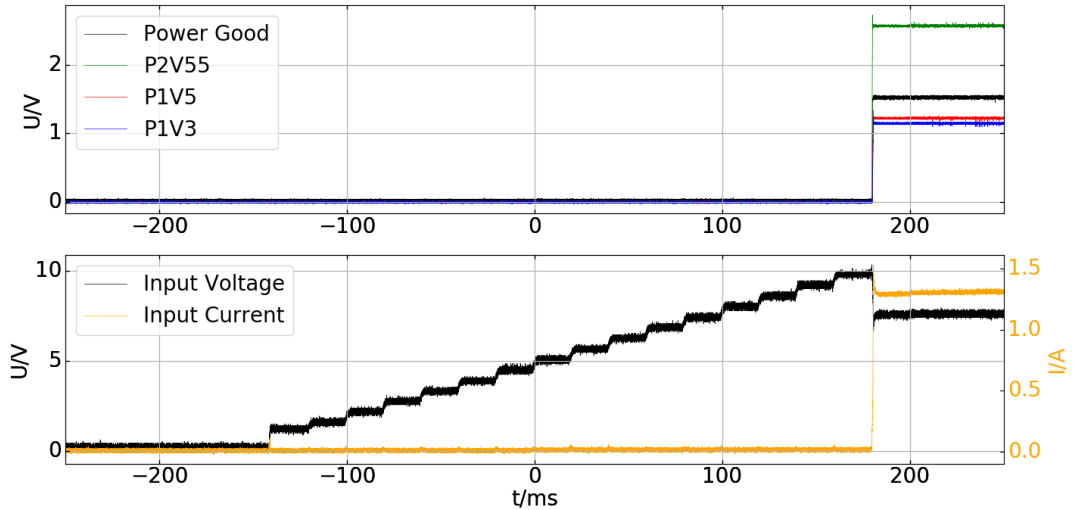


Figure 3.6: Turn-on sequence of POH 3 using a slow 29 V/s power supply ramp and the PS-PP1 supply cable.

The effect does not occur on POH 3 where R_{25} has been changed to 9.09 k Ω in the voltage divider used to enable bPOL12V. The enable threshold is much higher (Tab. 2.2) and the voltage drop across the supply cable is no longer sufficient to disable the converters immediately after

turn-on (Fig. 3.6).

The input voltage required to enable bPOL12V via the enable voltage divider (Fig. 2.9) was calculated previously (Tab. 2.2). However, when considering the fast turn-on sequence the input voltage at which the converter enables seems much higher (Fig. 3.4). This happens because Capacitor C_4 placed after the enable voltage divider causes a delay between the voltage applied at the input of the POH and the voltage applied to the enable pin. The voltage across a capacitor over time can be modelled using an exponential function:

$$U_C(t) \propto e^{-\frac{t}{\tau}} \quad \text{where} \quad \tau = R \cdot C \quad . \quad (3.6)$$

In this case a 10 nF capacitor is charged through the 100 k Ω resistor of the voltage divider, which leads to $\tau = \mathcal{O}(1 \text{ ms})$. It is therefore difficult to extract exact values for the enable threshold from the fast turn-on sequences discussed previously. They can however be extracted from the slower turn-on sequences. The results as well as the corresponding values at the enable pin (calculated using Eq. 2.6) are summarized in Table 3.2.

	U_{in} / V	$U_{\text{BUCK_ENABLE}} / \text{mV}$
POH 1	5.9 ± 0.1	$892 \pm 15(\text{stat.}) \pm 11(\text{sys.}) = 892 \pm 19$
POH 2	5.7 ± 0.1	$862 \pm 15(\text{stat.}) \pm 10(\text{sys.}) = 862 \pm 18$
POH 3	10.2 ± 0.1	$849.9 \pm 8.3(\text{stat.}) \pm 11.0(\text{sys.}) = 850 \pm 14$

Table 3.2: Measured enable voltages for all POH prototypes as well as corresponding voltage applied to the enable pin. Uncertainties on U_{in} result from inaccuracies when reading from the plots and were treated as statistical uncertainties, while the systematic uncertainties on $U_{\text{BUCK_ENABLE}}$ result from the uncertainties on the value of the resistors.

When comparing these values to the nominal values (Tab. 2.2) the enable threshold is around 0.5 V higher than nominal in all three power hybrids. As indicated in the table this could be explained by a threshold higher than the nominal 800 mV at $U_{\text{BUCK_ENABLE}}$. Another possibility is that the resistor deviates further from its nominal value than the uncertainty that is stated in the schematics (A.1 in Appendix A).

3.2.2 Turn-off sequence

The bPOL12V converter disables when the input voltage falls below the disable threshold (Tab. 2.2). However, with the original voltage divider ($R_{25} = 17.8 \text{ k}\Omega$) the bPOL12V will always be disabled via UVL, because the nominal disable threshold is lower than the threshold for UVL (Tab. 2.1). Once bPOL12V is disabled its output voltage decreases, consequently disabling the second stage converters as well. The voltages and currents are measured using the same setup as used for the turn-on sequences. The only difference is that the trigger level is set to 5 V on the negative edge of the input voltage. In the following paragraphs two variations of the turn-off sequence will be discussed, both using the PS-PP1 cable. The first measurement does not use a controlled power supply ramp while the second measurement was performed using the 29 V/s controlled power supply ramp described previously.

1. Turn-off sequence without controlled supply ramp

Figure 3.7 shows the turn-off sequence of the POH. As expected bPOL12V disables first and the second stage converters turn-off shortly afterwards. All three converters turn-on again briefly after turn-off, which manifests itself in small voltage peaks during the turn-off procedure. This happens because the threshold for UVL (Tab. 2.1) through which bPOL12V is disabled is close to the nominal enable threshold (Tab. 2.2). Once the converters turn off the voltage drop across

the PS-PP1 cable is much smaller and the voltage at the input increases enough to enable bPOL12V and consequently bPOL2V5 again.

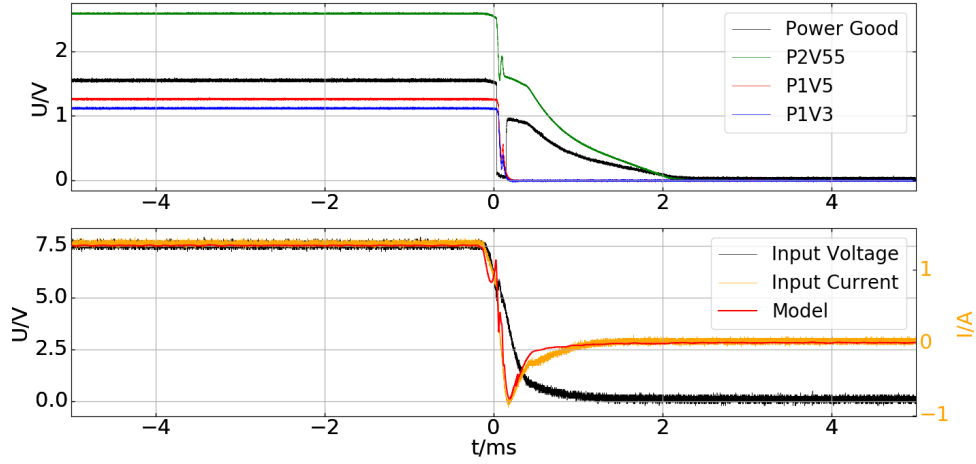


Figure 3.7: Turn-off sequence of POH 2 using a fast power supply ramp as well as the PS-PP1 supply cable.

These peaks are not visible in the turn-off sequence of POH 3 (Fig. 3.8), where the voltage divider has been adjusted in such a way that the enable threshold is high enough above the threshold for UVL so that the increase in input voltage, when the converters are disabled, is not sufficient to enable bPOL12V again.

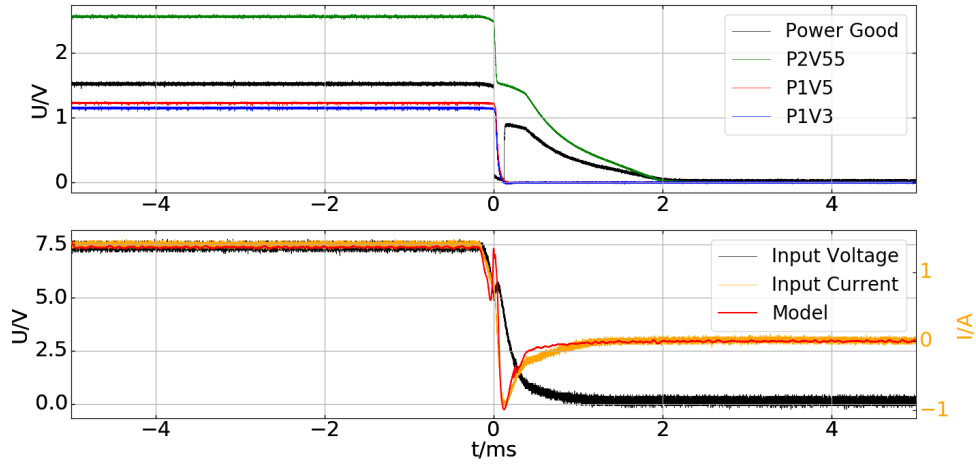


Figure 3.8: Turn-off sequence of POH 3 using a fast power supply ramp as well as the PS-PP1 supply cable.

In both figures the model (Eq. 3.5) developed to simulate the input current during the turn-on sequences is plotted. It accurately depicts the large negative current that can be observed during turn-off as well as the small increase in current corresponding to the increase in input voltage once the converters are disabled. Therefore the input current during the turn-off sequence can be explained through the discharging of capacitors on the PCB in the same way the current during turn-on can be explained by the charging of those capacitors.

One may also note that the Power Good signal does not remain zero once the converters are disabled. This happens because the logic for the linear regulators is disabled when the input voltage falls below 4.2 V and the Power Good signal is no longer clamped to zero.

2. Turn-off sequence using long cable, slow power supply ramp

As discussed during the turn-on sequences, using the original voltage divider in combination with a slower ramp-down will lead to consecutive enabling and disabling of the converters. Figure 3.9 shows the turn-off sequence with the 29 V/s power supply ramp for POH 3, where the nominal disable threshold is far enough above the threshold for UVL to prevent these consecutive turn-ons.

Similarly to the turn-on sequences the slow turn-off sequences make it possible to determine precise voltages for the disable threshold, as the time necessary for the charging of capacitor C_4 placed before bPOL12V (Fig. 2.9) is one order of magnitude lower than that for each voltage step during the controlled power supply ramp. The measured disable voltage as well as the corresponding value for $U_{\text{BUCK_ENABLE}}$ (Eq. 2.6) for POH 3 are summarized in Table 3.3. As POH 1 and POH 2 are disabled via UVL a discussion of the voltages applied to the enable pin is not meaningful. The measured value is compatible with the nominal value of 500 mV within three standard deviations.

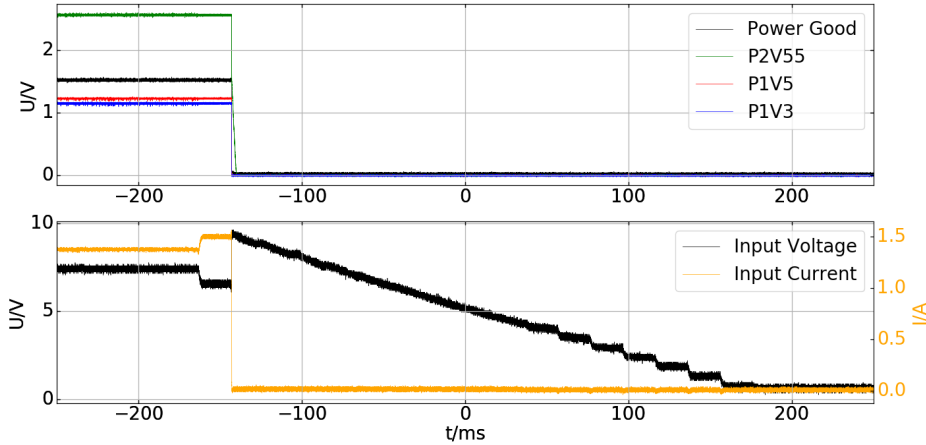


Figure 3.9: Turn-off sequence of POH 3 using a slow 29 V/s power supply ramp as well as the PS-PP1 supply cable.

	U_{in} / V	$U_{\text{BUCK_ENABLE}} / \text{mV}$
POH 1	5.2 ± 0.1	—
POH 2	5.2 ± 0.1	—
POH 3	6.4 ± 0.1	532 ± 14

Table 3.3: Disable voltages for all POH prototypes as well as the corresponding voltage applied to the enable pin (calculated using Eq. 2.6).

3.2.3 Large load changes

The behaviour of the POH needs to be robust under large load changes, which can occur during operation in the detector. In this section the effects of a sudden increase from no load to nominal

loads (Tab. 2.3) applied at the output connectors of the POH will be presented. Voltages and currents were measured in the same way as discussed during the turn-on and -off sequences. Two channels of the power supply (ROHDE&SCHWARZ HMP4040 Four-Channel Power Supply [18]) are connected to the load board (Fig. B.3 in Appendix B). In addition to the channel responsible for powering and supplying current to the Load Board another channel of the power supply is connected to the Load Board at X9. Both of these channels are connected to a so-called “NAND gate” which only produces an output if one of the channels is not powered. At first both of these power supply channels are turned on. In order to suddenly apply loads to the POH output the second channel is turned off. The trigger level of the oscilloscope is set to the positive edge of the input current.

Figures 3.10 and 3.11 show the behaviour of the POH during a sudden increase from zero to nominal loads without and with the PS-PP1 cable, respectively³. To compare the drop in input voltage the y-axis has been scaled in the same way for both plots. While almost no voltage drop occurs using the short supply cable, the DC-resistance of the PS-PP1 cable leads to a significant voltage drop of around 2.5 V. To verify that this voltage drop is mainly due to the DC-resistance of the supply cable the resistance is calculated from the voltage drop. Assuming signal- and return-line have the same DC-resistance R_{DC} it can be calculated from the length of the cable l as well as the voltage drop $\Delta U = 10\text{ V} - U_{in}$ along the cable and the current I_{in} measured at the input of the POH:

$$\Delta U = 2l \cdot I R_{DC} \quad \Rightarrow \quad R_{DC} = \frac{10\text{ V} - U_{in}}{2l \cdot I_{in}} \quad . \quad (3.7)$$

The results for the DC-resistance of the cable are summarized in Table 3.4. The input voltage and current were determined by averaging the corresponding traces over 3000 data points. Systematic uncertainties arise from the amplitude accuracy of the instruments which are specified in the manufacturer’s manuals (1 % of reading) [14, 17]. The results for all three POH prototypes are in agreement with one another. Within the uncertainties a final value for the DC-resistance can therefore be estimated by taking the weighted mean of the three results:

$$R_{DC} = (13.91 \pm 0.33(\text{stat.}) \pm 0.25(\text{sys.})) \frac{\Omega}{\text{km}} = (13.91 \pm 0.41) \frac{\Omega}{\text{km}} \quad .$$

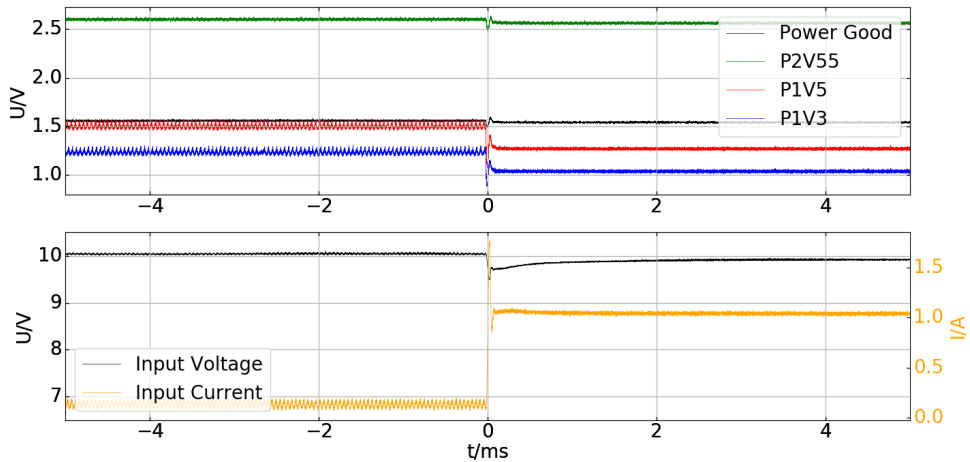


Figure 3.10: *Sudden increase from no load to nominal loads with short supply cable.*

³Without load applied to the connectors an unstable output voltage of the second stage converters can be observed. This will be discussed in Chapter 3.4.

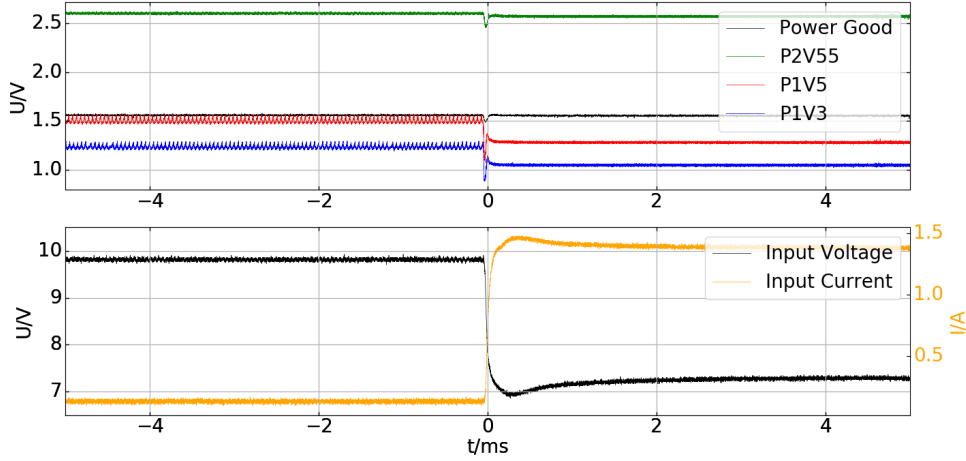


Figure 3.11: Sudden increase from no load to nominal loads with long supply cable.

	U_{in} / V	I_{in} / A	$R_{\text{DC}} / \frac{\Omega}{\text{km}}$
POH1	7.55 ± 0.10	1.37 ± 0.03	$13.7 \pm 0.6 \pm 0.4$
POH2	7.54 ± 0.09	1.37 ± 0.02	$13.9 \pm 0.5 \pm 0.5$
POH3	7.43 ± 0.010	1.40 ± 0.02	$14.1 \pm 0.6 \pm 0.4$

Table 3.4: Voltage and current measured at the input connector of the POH as well as calculated DC-resistance of the cable. Statistical uncertainties are stated ahead of systematic uncertainties.

All values are below the maximum rating for the DC-resistance of the cable of $16 \frac{\Omega}{\text{km}}$ which is provided by the manufacturer [21]. Additionally the DC-resistance of the cable is measured directly with a multimeter using four-terminal sensing to be $14.1 \frac{\Omega}{\text{km}}$. This is in agreement with the value determined from the voltage drop of the input voltage.

Voltage drops are also visible in the output voltages of the converters, especially the second stage converters, where the load is much higher (Table 2.3). This is due to voltage drops across the PCB. Without using the PS-PP1 supply cable a spike can be observed in the input current once the load is applied. Using the longer cable no distinct spike is visible. Instead the current rises to 1.5 A, just after the load is applied, and then slowly decreases to its final value of approximately 1.4 A. This is probably due to the inductance of the longer supply cable that dampens any sharp increases and decreases of the input current.

3.2.4 Summary

The PS-POH prototypes behaved mostly as expected during turn-on and turn-off when not using the PS-PP1 supply cable and without the controlled 29 V/s power supply ramp. However, POH 1 and POH 2 that were assembled using $R_{25} = 17.8 \text{ k}\Omega$ are always disabled via UVL. Because the UVL and the nominal enable threshold are very close together the voltage drop when using the PS-PP1 supply cable in combination with the slower 29 V/s supply cable is sufficient to disable the converters again. This leads to a series of consecutive turn-ons and turn-offs of the converters. This was observed on both prototypes in the turn-on as well as the turn-off sequences. Some undesired disabling/enabling of the converters due UVL could also be observed when using the PS-PP1 supply cable or the long 29 V/s power supply ramp separately. All of the issues can be solved by using $R_{25} = 9.09 \text{ k}\Omega$ in the voltage divider.

3.3 Efficiency measurements

An important measure to consider in any electrical application is the electrical efficiency. It is defined as the ratio between the power at the output of the DC-DC converter and the input:

$$\eta = \frac{P_{\text{out}}}{P_{\text{in}}} = \frac{U_{\text{out}} \cdot I_{\text{out}}}{U_{\text{in}} \cdot I_{\text{in}}} \quad . \quad (3.8)$$

In a lossless circuit the efficiency is 100 %. However, in any real application power loss occurs due to a variety of reasons. In the case of DC-DC converters factors contributing to the power loss include [24]:

- Conduction loss caused by the DC-resistance of the inductor as well as the resistance of the MOSFETs. These losses increase with load.
- Losses due to switching between the on- and off-state. These losses are usually proportional to the switching frequency [9]. Examples are switching losses in the transistors due to the finite time necessary for the switch to turn on/off and losses due to the (dis-)charging of the gate that behaves like a simple input capacity during switching [25].

When the whole POH is considered, additional losses occur due to the DC-resistance of the PCB. The power dissipated due to these losses generates heat. This additional heat load needs to be removed as the silicon sensors must be maintained at a temperature of at most -20 °C [3]. If the temperature exceeds this value the sensor temperature will continue to rise in a positive feedback loop as the leakage current increases with temperature. This is called “thermal runaway”.

To distinguish between efficiency losses due to the voltage drop across the PCB and inefficiencies of the converters themselves, the efficiency of the POH is measured at different capacitors on the PCB (Tab. 3.5). The capacitors are marked in Figure 3.12. The voltages are measured using a digital multimeter (VOLTcraft Digital Multimeter VC276 TRMS [26]) as the multimeter can be used in combination with test probes that have very thin tips and are thus ideal for measuring voltages across small capacitors. Additionally the voltages are also measured at the output connectors, where the passive oscilloscope probes from the previous studies are used. During all measurements the POH was cooled to 18 °C using the Peltier controller. In the following sections measurements of the efficiencies of the individual converters (Chapter 3.3.1) as well as measurements of the efficiency of the POH as a whole (Chapter 3.3.2) are presented. The currents are measured using a current clamp (Teledyne LeCroy CP031 Current Probe [17]).

	V_{in}	V_{2V55}	V_{1V5}	V_{1V3}
Capacitors outside of shield	C_1	C_8	C_{22}	C_{15}
Capacitors closest to chip	C_3	C_6	C_{18}	C_{11}

Table 3.5: *Capacitors at which input and output voltages of the converters are measured.*

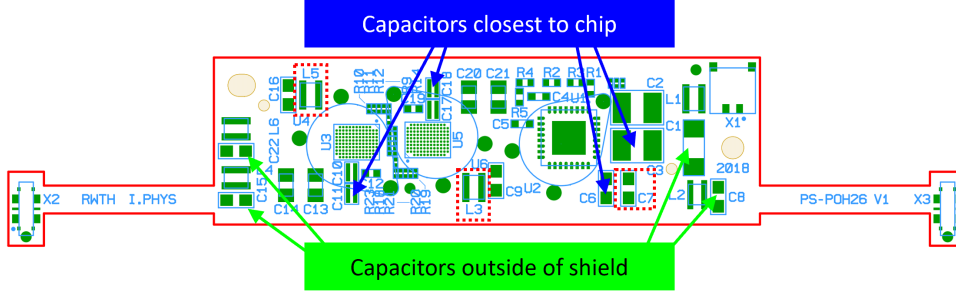


Figure 3.12: Layout of the PS-POH in which the capacitors closest to the chip (blue) and the capacitors outside of the shield (green) are marked. Additionally the Pi-filter coils that were removed for the individual efficiency measurements and capacitor C_7 at which cables were soldered are marked (red).

3.3.1 Efficiency of bPOL12V and bPOL2V5

To characterize the efficiency of a single converter, the others are disconnected by removing the coils from the Pi-filter. Coils L_3 and L_5 are removed to disconnect the bPOL2V5 with 1.3 V and 1.5 V output voltage, respectively (Fig. A.2 in Appendix A). Additionally cables are soldered at capacitor C_7 (Fig. 3.12). These cables are used to either apply loads of up to 3.5 A to bPOL12V or to power bPOL2V5. Voltages are measured at the capacitors closest to the chip. The input voltage at which the measurements are performed is 10 V for the bPOL12V efficiency and 2.5 V for the bPOL2V5 efficiencies.

One of the main contributing factors to power loss when considering the single converters is the loss due to the DC-resistance of the coil [24]. The average power loss in the inductor P_L is proportional to the square of the RMS⁴ current I_{RMS}^2 flowing through the coil [27]. The RMS current can be calculated by integrating the time dependent current shown in Figure 2.7 over a whole switching cycle T :

$$I_{\text{RMS}} = \sqrt{\frac{1}{T} \int_0^T I(t)^2 dt} \quad . \quad (3.9)$$

On the falling edge the current $I(t)$ can be expressed as a linear function of t :

$$I(t) = I_{\text{max}} - \frac{\Delta I}{T/2} \cdot t \quad \text{where} \quad I_{\text{max}} = I_{\text{out}} + \frac{\Delta I}{2} \quad . \quad (3.10)$$

The integration can be simplified by assuming $t_{\text{on}} = t_{\text{off}}^5$ and integrating over half of the period:

$$\begin{aligned} I_{\text{RMS}}^2 &= \frac{2}{T} \int_0^{T/2} \left(I_{\text{max}} - \frac{\Delta I}{T/2} \cdot t \right)^2 dt = \frac{2}{T} \left[I_{\text{max}}^2 t - 2 \frac{\Delta I \cdot I_1}{T} t^2 + \frac{4}{3} \frac{\Delta I^2}{T^3} t^3 \right]_0^{T/2} \\ &= I_{\text{max}}^2 - \Delta I \cdot I_{\text{max}} + \frac{\Delta I^2}{3} = I_{\text{out}}^2 + \frac{\Delta I^2}{12} \quad . \end{aligned} \quad (3.11)$$

With this the loss P_L in the inductor due to its DC-resistance R_L can be expressed as:

$$P_L = R_L \cdot I_{\text{eff}}^2 = R_L \cdot \left(I_{\text{out}}^2 + \frac{\Delta I^2}{12} \right) \quad . \quad (3.12)$$

In the following sections the efficiency of bPOL2V5 and bPOL12V will be discussed. The results are summarized at the end of the chapter.

⁴Root Mean Square

⁵As the area of a triangle is only dependent on the height (in this case ΔI) and the base (in this case $T = t_{\text{on}} + t_{\text{off}}$) the result of the integral remains the same under this assumption.

Efficiency of bPOL2V5

Figures 3.13 (left) and 3.14 (left) show the measured efficiency for bPOL2V5 with 1.3 V and 1.5 V output voltage, respectively. In addition to the measurements at the capacitors closest to the chip (black) measurements at the output connectors (green) are shown. In these measurements the load applied to the converter was varied between 0 A and 3 A. A clear dependence of the efficiency on the output current is visible. The efficiency increases steeply with rising output current until about 500 mA. Then it flattens out and reaches its maximum at around 1.5 A. After the maximum the efficiency decreases slightly, as conduction losses caused by the increasing output current dominate. In this region the efficiencies measured at the output connector decrease more rapidly because of the additional DC-resistance of the PCB. This will be discussed in more detail in Chapter 3.3.2. To obtain the uncertainty on the efficiency, the uncertainties on the voltages and currents were propagated using Gaussian error propagation.

For bPOL2V5 detailed measurements of the chip efficiency are given in the data sheet [8]. The data sheet contains measurements of the efficiency as a function of the output current as well as measurements as a function of the output voltage. The current dependent measurement in the data sheet was performed with a converter with 1.2 V output voltage. Therefore this measurement needs to be shifted upwards in order to be comparable to converters with an output voltage of 1.3 V or 1.5 V. The voltage dependent measurement in the data sheet shows a near linear dependence of the efficiency on the output voltage, regardless of load, between 1.2 V and 1.5 V. From the data sheet an increase of 2 % per additional 0.3 V of output voltage is determined. The nominal values η_0 cited in the following considerations were calculated by shifting the current dependent measurement in the data sheet upwards by $(V_{\text{out}} - 1.2 \text{ V})/0.3 \text{ V} \cdot 2 \%$. The current dependent measurement in the data sheet shows the efficiency for several samples of bPOL2V5. From this a systematic uncertainty on the nominal values of $\sigma_\eta \approx 0.3 \%$ can be estimated, when considering the spread of the measurements. The nominal values are plotted in red in Figures 3.13 (left) and 3.14 (left).

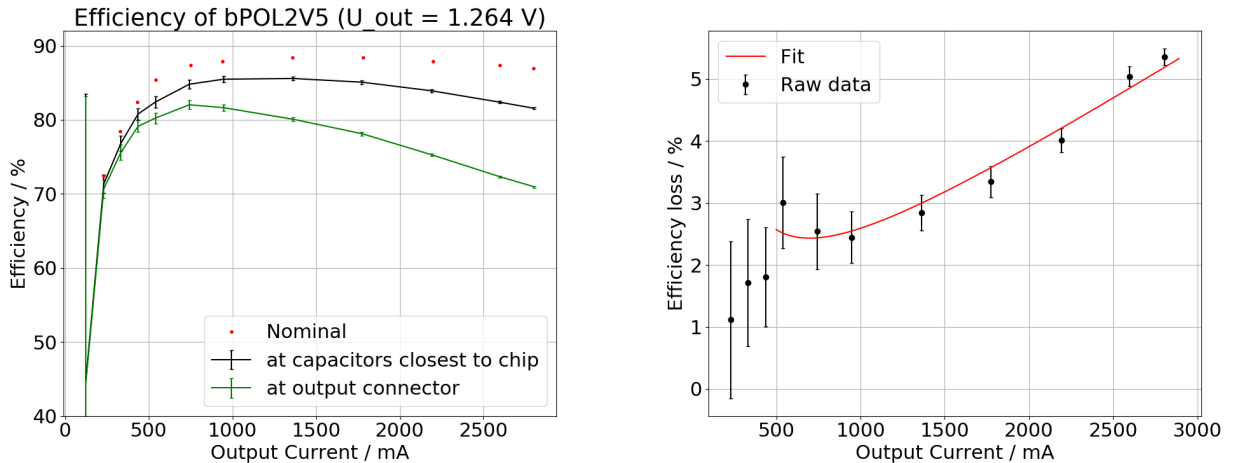


Figure 3.13: Efficiency measurements of bPOL2V5 with 1.3 V output voltage (left). Measurements at the capacitors closest to the chip (black) and at the output connectors (green) are shown. Additionally nominal values are plotted (red). Fit of efficiency loss due to conduction losses in the inductor (right). The efficiency loss $\Delta\eta$ when compared to the nominal values (black) as well as the result of the fit (red) are shown. The error bars result from statistical uncertainties on the voltages and currents.

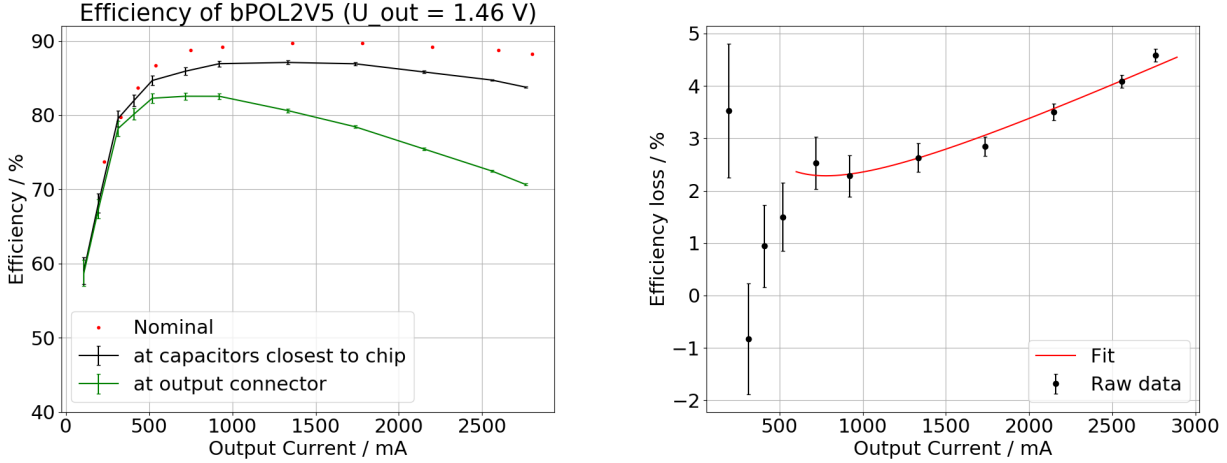


Figure 3.14: Efficiency measurements of bPOL2V5 with 1.5 V output voltage (left) and fit of efficiency loss due to conduction losses in the inductor (right). The colour scheme is identical to Figure 3.13.

The measured efficiency η is systematically lower than these nominal values η_0 . This difference in efficiency can be explained in part through additional ohmic losses in the inductor:

$$\Delta\eta = \eta - \eta_0 = \frac{P_L}{P_{in}} \approx \frac{P_L}{P_{out}} = \frac{P_L}{U_{out} \cdot I_{out}} \stackrel{(3.12)}{=} \frac{\Delta R_L}{U_{out}} \cdot \left(I_{out} + \frac{\Delta I^2}{12 I_{out}} \right) \quad (3.13)$$

To determine the additional DC-resistance ΔR_L of the inductor the difference between the points taken from the data sheet and the measured efficiency is plotted against the output current and a fit is performed with ΔR_L and ΔI being the two free parameters (Eq. 3.13). Points below 600 mA were discarded for this analysis as it is to be assumed that differences in switching losses dominate in this area⁶. The results of the fits are shown in Figures 3.13 (right) and 3.14 (right). Statistical uncertainties on the fit parameters are several magnitudes lower than the systematical uncertainties⁷. Therefore only systematic uncertainties will be cited when discussing the results of this analysis.

Efficiency of bPOL12V

Figure 3.15 (left) shows the measured efficiency of bPOL12V. The same general dependence on the output current as the bPOL2V5 can be observed. At low output currents the efficiency increases steeply until about 1 A. Then the curve flattens reaching its maximum at around 2 A. At higher output currents the efficiency decreases again. The preliminary data sheet of bPOL12V [7] does not yet include measurements of the efficiency but such measurements were presented during the Topical Workshop on Electronics for Particle Physics (TWEPP) in 2019 [28]. These measurements are also shown in the plot (red). However, both the inductivity of the coil as well as the switching frequency of the converter are different to those used on the POH prototype. These are relevant at low currents when conduction losses due to ΔI , which is dependent on L (Eq. 2.5), as well as differences in switching losses, which are dependent on the switching frequency f , dominate. Therefore the fit was only performed at higher currents,

⁶Differences in switching losses are inevitable as most switching losses are proportional to the switching frequency, which is slightly different for the converters under test compared to those the measurements were performed on in the data sheet.

⁷The systematic error was obtained by repeating the analysis with all data points shifted up-/downwards by their respective systematic errors. The largest deviation from the original result was then used as the systematic uncertainty.

where these effects can be neglected. Under these assumptions Equation 3.12 can be further simplified:

$$P_L \frac{\Delta I^2/12}{I_{\text{out}}^2} \ll 1 \quad P_L \approx R_L \cdot I_{\text{out}}^2 \quad (3.14)$$

This leads to a simple linear dependency of the efficiency loss on the output current. Figure 3.15 (right) shows both the raw data and the linear fit.

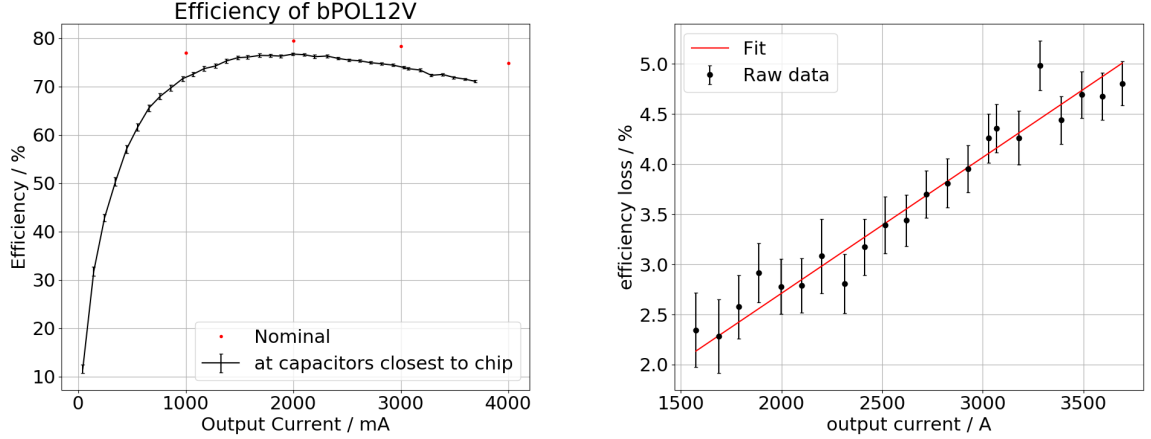


Figure 3.15: Efficiency measurements of bPOL12V (left) and fit of efficiency loss due to conduction losses in the inductor (right).

Results

The results of the analysis are summarized in Table 3.6. For bPOL2V5 the nominal value $\Delta I_{\text{nominal}}$ can be calculated from the nominal inductance L , the voltages cited in the table as well as the switching frequencies determined during the studies of conducted noise (Fig. 4.4) using Equation 2.5. This yields $\Delta I_{\text{nominal}} \approx 1.8$ A which is about two standard deviations lower than the values determined from the fit. Due to the skin effect the alternating part of the current I_{eff} flows mainly within the outer layer of the wire. Therefore the resistance presented to the alternating current ΔI by the inductor might be slightly higher than that affecting the direct current I_{out} . In the fit this effect will be absorbed into the fit parameter ΔI which would explain a slightly higher value than nominal. The values calculated for the additional DC-resistance of the inductor used on bPOL2V5 are the same for both converters within one standard deviation. The measurements performed at CERN used commercial air core solenoids. For example in commercial coilcraft air core solenoids with 90 nH and 222 nH the maximum DC-resistance is 15 m Ω and 35 m Ω , respectively [29]. Comparing these values with the resistances of the air core toroids used on the prototype (31 m Ω for the 100 nH inductor and 50 m Ω for the 220 nH inductor) the differences in DC-resistance determined from the fit is of a realistic order of magnitude.

U_{out}	$\Delta R_L / \text{m}\Omega$	$\Delta I / \text{A}$	$\frac{\chi^2}{\text{ndof}}$
1.264	22.45 ± 1.02	2.20 ± 0.33	0.79
1.460	22.03 ± 1.16	2.42 ± 0.29	0.95
2.625	35.59 ± 2.56	—	0.54

Table 3.6: Additional DC-resistance ΔR_L of the inductor as well as amplitude ΔI of the triangular current flowing through the inductor.

The DC-resistance of the PCB might also lead to some additional DC-resistance in these measurements.

3.3.2 Efficiency of the PS-POH

Measurements of the efficiency across both the first and second stage converter were performed. The voltages are measured at different capacitors on the PCB (Tab. 3.5) as well as at the output connectors of the POH. Nominal loads (Tab. 2.3) were applied at the output connectors. Figure 3.16 shows the results of these efficiency measurements for different input voltages. Sta-

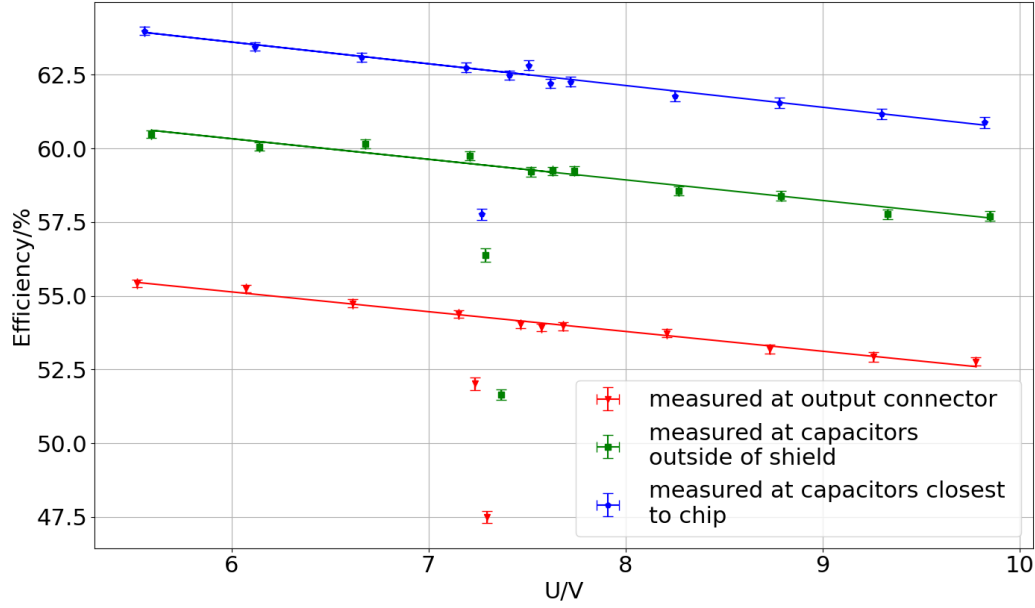


Figure 3.16: Measurements of the efficiency across the whole POH. Measurements were performed at the capacitors closest to the chip (blue), at the capacitors outside of the shield (green) as well as at the output connectors (red) (Tab. 3.5). Points between 7.2 V and 7.4 V were omitted when fitting the linear functions. For each data set the linear fit is plotted in the corresponding colour.

tistical uncertainties as well as systematic uncertainties due to the amplitude accuracy of the instruments were considered. The efficiency at an input voltage of 10 V and at the capacitors closest to the chip is measured as:

$$(60.88 \pm 0.19(\text{stat.}) \pm 1.27(\text{sys.})) \% = (60.88 \pm 1.27) \%$$

In this case efficiency losses across the PCB are negligible and only the efficiency of the converters is relevant. The efficiencies for the individual converters can be determined from the efficiency measurements discussed in the previous section. For bPOL2V5 the efficiency at nominal loads is determined from Figures 3.13 and 3.14 to be 83.1 % and 85.5 % for the converter with 1.3 V and 1.5 V output voltage, respectively. Assuming the load applied to both converters is roughly the same the efficiency of the second stage can be approximated to $\frac{83.1\% \cdot 85.5\%}{2} = 84.3\%$. To determine the efficiency of bPOL12V at nominal loads the efficiency is plotted against the input current instead of the output current (Fig. 3.15). As the input current of the POH with all converters active at nominal loads is known ($I_{\text{in}} = 1.09 \text{ A}$) the efficiency of bPOL12V can be determined to be 73.5 %. An estimate of the total efficiency can then be calculated by multiplying

the efficiencies of the both stages: $73.5\% \cdot 84.3\% = 62\%$. The measured efficiency is compatible with this result.

Figure 3.16 also shows a decrease in efficiency with increasing input voltage. This is plausible as a higher input voltage increases the current ΔI (Eq. 2.5) flowing through the inductor. This increases ohmic losses in the inductor (Eq. 3.12) and therefore decreases the efficiency. Neglecting the unexpected drop in efficiency between input voltages of 7.2 V and 7.4 V⁸ linear functions can be fit to the data points excluding this region. The results are summarized in Table 3.7.

data set	slope / $\frac{\%}{V}$	y-intercept / %	$\frac{\chi^2}{ndof}$
at output connector	-0.69 ± 0.05	59.1 ± 0.4	0.21
at capacitors outside of shield	-0.70 ± 0.04	64.5 ± 0.3	1.37
at capacitors closest to chip	-0.74 ± 0.04	68.0 ± 0.3	0.55

Table 3.7: Results of the linear fits to measurements of the efficiency as a function of the input voltage. The uncertainties stated are the errors on the parameters resulting from the fit.

Taking the weighted arithmetic mean of the slopes calculated for the three data sets yields an efficiency drop of

$$(0.7068 \pm 0.0239(\text{stat.}) \pm 0.0089(\text{sys.})) \% = (0.707 \pm 0.026) \%$$

per additional volt of input voltage.

Comparing the different data sets in Figure 3.16, it is obvious that the voltage drop across the PCB drastically influences the efficiency. While at 10 V input voltage the efficiency at the capacitors closest to the chips is still around 60.8 %, it drops to around 52.5 % when measured at the output connectors. This inefficiency is due to problems in manufacturing of the PCB regarding the copper thickness as well as due to the geometry of the flex tails. To lessen this effect the geometry of the flex tails will be changed in newer PS-POH prototypes.

⁸This efficiency drop is related to a malfunctioning of the adaptive logic of bPOL12V and will be discussed in Chapter 3.4.

3.4 Expected improvements with bPOL12V_V6 and bPOL2V5_V3.3

While performing the electrical tests several unexpected effects were observed that can be ascribed to the converter prototypes used on the POH. These effects will be briefly summarized in the following paragraphs.

Low clamp voltage in bPOL12V_V4

A voltage can be measured at the output of bPOL12V before the converter is turned on (Fig. 3.17). The output voltage gradually increases with the input voltage until it reaches a value of around 250 mV. At this point the input voltage reaches 4.2 V, the on-chip logic for the linear regulators is enabled and the Power Good signal is tied to zero. Similarly the output voltage of bPOL12V should also be tied to zero. However, the voltage clamp, which is operative once the linear regulators are switched on, is not strong enough, tying the voltage to a value of about 250 mV instead. This will be addressed in a newer version of bPOL12V by increasing the clamp voltage [30].

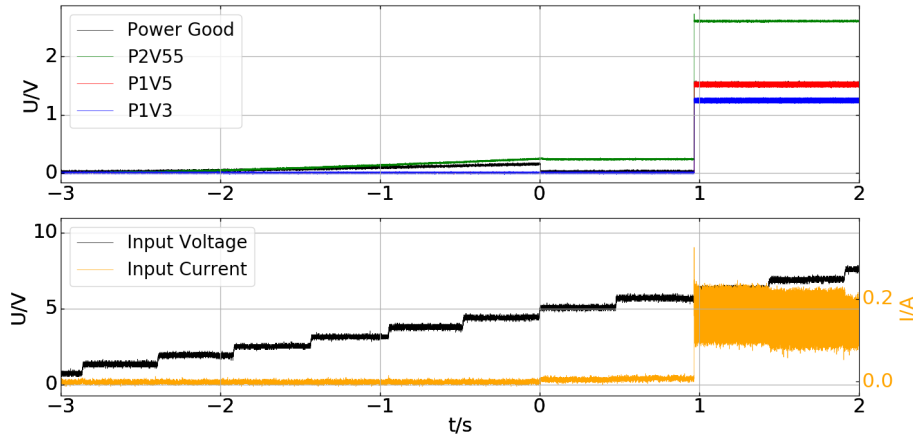


Figure 3.17: Increase in output voltage of bPOL12V (green) before the chip is enabled at around 1 ms.

Malfunctioning of the adaptive logic in bPOL12V_V4

On the current prototype of bPOL12V the adaptive logic malfunctions at certain input voltages. This was observed in the efficiency measurements (Fig. 3.16), where a significant drop in efficiency is visible between 7.2 V and 7.4 V. The adaptive logic has been designed to optimize the dead-time of the transistors. The “Phase” in Figure 3.18 refers to the voltage through in the inductor. The Phase voltage is modified slightly when compared to that of an ideal converter (V_L in Fig. 2.7), due to charging and discharging of a parasitic capacitance by the inductor current during the dead-time: The Phase voltage rises to a value slightly above V_{in} after the NMOS is turned off because the parasitic Phase node capacitance is charged and falls below zero when the PMOS is turned off and the capacitance is discharged. This in turn leads to conduction losses in the body diodes of PMOS and NMOS. The adaptive logic shortens the time during which the body diodes conduct current.

Instead of a fixed dead-time the adaptive logic uses two comparators to determine when the transistors should be switched on. If the Phase voltage exceeds $V_{in} - 2.1\text{ V}$ the PMOS is turned on (HS comp). Similarly, the NMOS is enabled if the phase voltage is lower than 1.5 V (LS comp). At low input voltages the Phase is close to $V_{in} - 2.1\text{ V}$. A bit of noise at HS comp is sufficient to produce a noisy output of the comparator which leads to uncontrolled switching of the transistors.

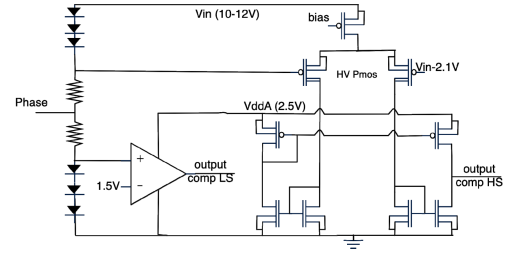


Figure 3.18: Circuit of the high and low side comparators of the adaptive logic [10].

In this state the chip consumes significantly more current, which explains the unexpected decrease in efficiency [30]. This increase in current is much larger when the input voltage is increased than when it is decreased. Additionally sinusoidal modulation of the output voltage of bPOL12V can be observed. Both of these effects can be seen in Figure 3.19. In the newer versions of bPOL12V the reference to the HS comp was changed to $V_{in} - 1.8\text{ V}$ which prevents this issue.

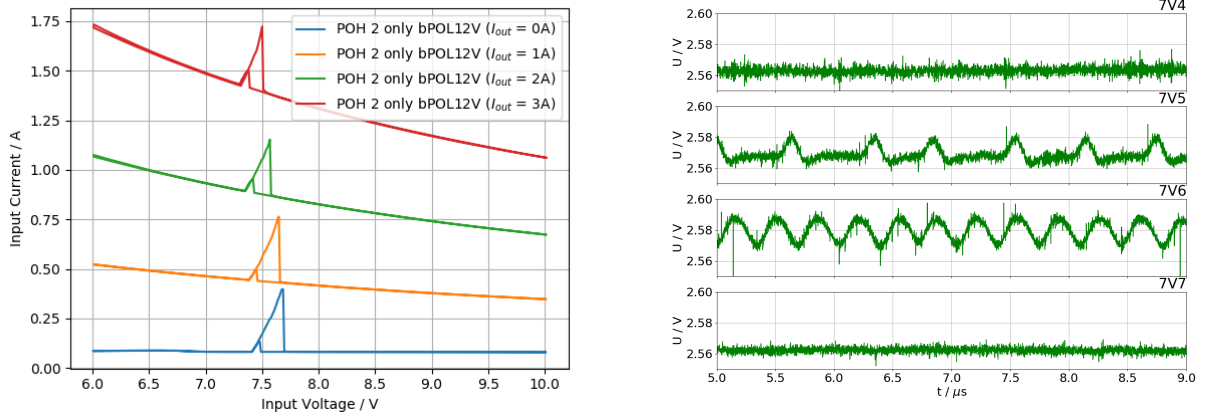


Figure 3.19: Increased current consumption of bPOL12V around 7.5 V input voltage measured with a short cable at the power supply using a LabView VI (left) and output voltage of bPOL12V at different input voltages (right).

Negative over current protection in bPOL2V5_V3.2

In bPOL2V5 the Negative Over-Current Protection triggers at low loads (Thresholds in Tab. 2.1). Because of the triangular form of the alternating current in the inductor (Fig. 2.7) the current reaches negative values when no or little load is applied to the converter. This in turn triggers OCP_{neg} which leads to oscillations of about 20 kHz in the output voltages of the converters (Fig. 3.20).

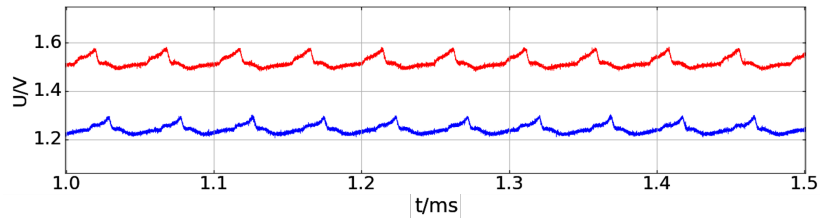


Figure 3.20: *Output voltage of bPOL2V5 with a nominal output voltage of 1.3 V (blue) as well as 1.5 V (red).*

In the current version of the bPOL2V5 the threshold for the positive and the negative over current protection is set with the same resistor, so that decreasing the threshold of OCP_neg comes at the cost of increasing the threshold of OCP_pos. Therefore a separate resistor will be used to set the threshold for OCP_neg [31] in newer versions of the converter.

4 Conducted noise

In applications using DC-DC converters small high-frequency modulations can be observed in the direct current at the output and input of the converter. These alternating currents occur at the switching frequency of the converter as well as its higher harmonics. When discussing conducted interference a distinction is made between common-mode (CM) and differential-mode (DM) currents. The equivalent circuit diagrams are shown in Figure 4.1 (right):

- **Differential-mode** current is created by a noise source within the circuit. It is present in both the signal and the return path in opposite direction and equal in amplitude. Ideally fields created by DM currents will cancel each other out [32].
- **Common-mode** current is generated by a noise source outside the circuit. It is propagated via capacitive leakage paths to ground [9]. In this case the currents present in signal and return path are in phase. As electromagnetic fields generated by CM currents do not cancel each other out they are a major contributing factor to electromagnetic radiation. CM currents are difficult to predict as they depend on parasitic parameters present within the PCB structure. Models have been previously developed for the buck DC-DC converters developed for the HL-LHC [33]. These studies also outline the importance of a standardized testing procedure, which will be discussed in Section 4.1.

In order to measure CM and DM noise separately the signal and return cable must be routed differently through a current clamp (Fig. 4.1, right). DM currents can be measured by routing the signal (brown) and return (black) cable anti-parallel to each other through the current clamp:

$$\frac{1}{2}I_{\text{CM}} + I_{\text{DM}} - \left(\frac{1}{2}I_{\text{CM}} - I_{\text{DM}}\right) = 2 \cdot I_{\text{DM}} \quad . \quad (4.1)$$

CM currents can be measured by routing the signal (red) and return (black) cable parallel to each other through the current clamp:

$$\frac{1}{2}I_{\text{CM}} + I_{\text{DM}} + \left(\frac{1}{2}I_{\text{CM}} - I_{\text{DM}}\right) = I_{\text{CM}} \quad . \quad (4.2)$$

From these considerations it is clear that two times the generated DM noise will be measured by the current clamp, which needs to be taken into account when discussing absolute values.

4.1 Experimental Setup

To ensure reproducible measurements it is important to adapt a standardized testing procedure. The setup used in Aachen is based on measurements performed at CERN [33] and was developed by Rüdiger Jussen during his diploma thesis [34].

Figure 4.2 shows the setup used for measuring conducted noise at the output and input of the POH. A schematic drawing of the setup is provided in Figure 4.3. All components of the setup are placed on a grounded copper plate, which provides a reference potential. The converter position is fixed at 40 mm above the ground plane (1) to ensure that any parasitic capacitances with respect to earth stay the same during all measurements. A laboratory power supply (2, Agilent E3634A DC power supply [35]) is used to provide the 10 V input voltage for the POH. A line impedance stabilization network (LISN) (3, HAMEG Instruments HM6050-2 [36]) is used

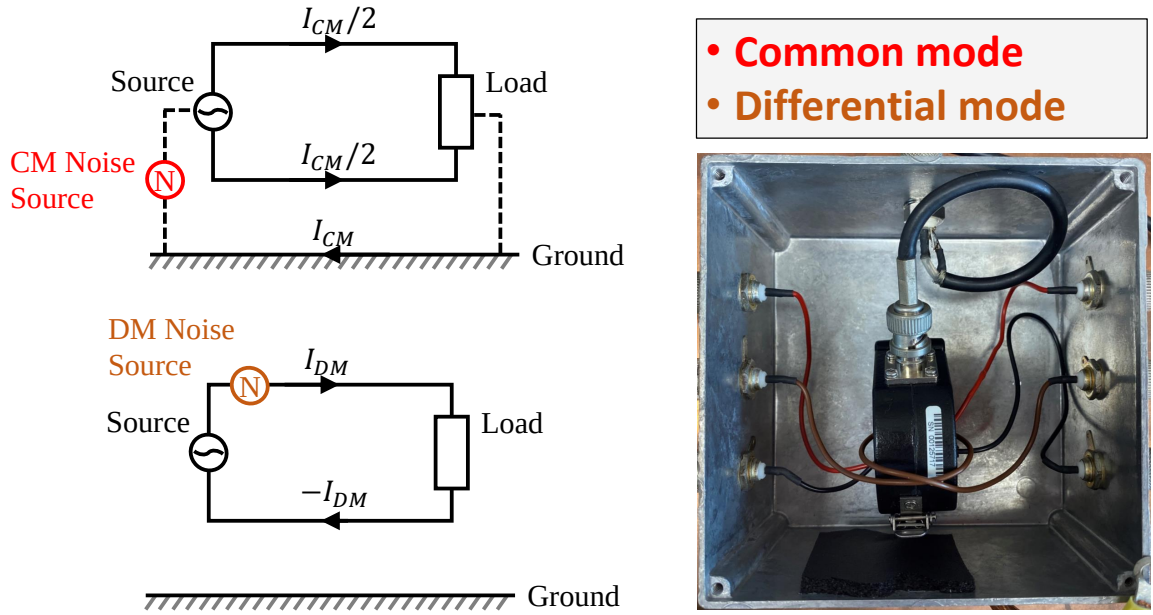


Figure 4.1: Circuit diagrams illustrating the difference between DM and CM currents (left) and routing through current clamp to measure DM and CM noise separately (right).

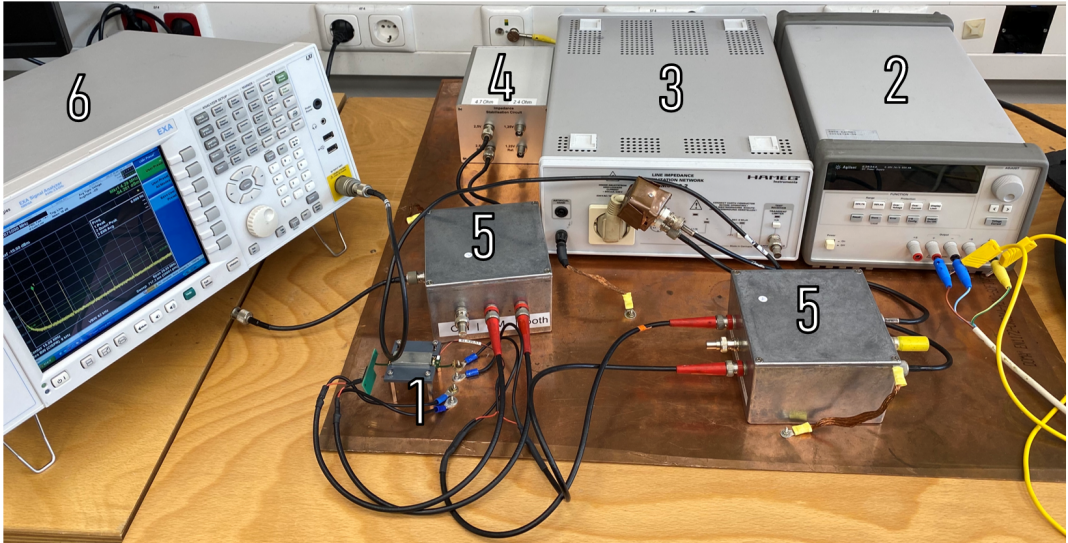


Figure 4.2: Photograph of the setup used to measure DM and CM noise of POH prototypes. Details are given in the text.

to smoothen the input voltage and to prevent propagation of noise from the voltage source or the power grid into the testing environment. It also prevents the reflection of converter noise. The load at the output of the converters is provided by an impedance stabilised load (ISL) (4, custom-built at RWTH Aachen). It is terminated using a 50Ω resistor to avoid reflections of noise back into the testing environment. Cables used in the setup are BNC coaxial cables with a resistance of 50Ω whose metal shield has been connected to the copper ground plate to prevent inductive couplings. However, a short part of the cable providing the input voltage to the POH does not have a metal shield. At the output connector of the POH the crossover board (Fig. A.3 in Appendix A) is used to connect the BNC cables to the POH. The current clamps

(Lindgren Mod. 94430-1 [37]) are located in metal boxes (5), which have also been grounded to the copper plate. To pick up both CM and DM noise separately, wires are routed through the current clamp in the manner described above (Fig. 4.1). The inductive signal produced by the current clamps is measured using a spectrum analyzer (6, Agilent Technologies EXA N9010A signal analyzer 9 KHz-3.6 GHz [38]) that is connected to the clamp using a 50Ω BNC cable. Depending on which box is connected to the spectrum analyzer, the noise is measured at the input or at the output connectors of the POH. In order to pick up even the smallest components of the conducted noise the mechanical attenuation of the spectrum analyzer is set to zero. To ensure accurate measurements of frequencies below 10 MHz the spectrum analyzer is DC-coupled.

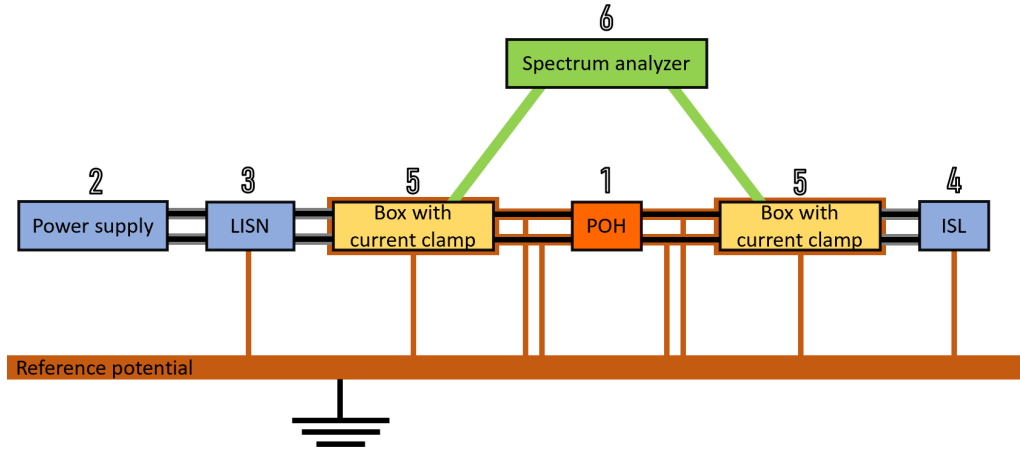


Figure 4.3: Schematic drawing of the setup to measure DM and CM noise (adapted from Ref. [39]).

Measuring alternating currents using the spectrum analyzer

The spectrum analyzer measures the absolute power ratio of the noise L_P in units of decibel-milliwatts (dBm). It can be expressed through the ratio of the power of the noise P_{noise} to a reference power of 1 mW:

$$L_P[\text{dBm}] = 10 \cdot \log \left(\frac{P_{\text{noise}}}{1 \text{ mW}} \right) \quad . \quad (4.3)$$

Similarly the absolute voltage ratio (absolute current ratio) is defined through the ratio of the voltage V_{noise} (current I_{noise}) generated by the noise to a reference voltage (current) of 1 μV (1 μA):

$$L_V[\text{dB}\mu\text{V}] = 20 \cdot \log \left(\frac{V_{\text{noise}}}{1 \mu\text{V}} \right) \quad \text{and} \quad L_I[\text{dB}\mu\text{A}] = 20 \cdot \log \left(\frac{I_{\text{noise}}}{1 \mu\text{A}} \right) \quad . \quad (4.4)$$

The voltage ratio can be calculated from the absolute power ratio by applying the definition of electrical power $P = \frac{V^2}{R}$, where R is the impedance of the BNC cable ($R = 50\Omega$) and expanding with 1 μV :

$$\begin{aligned} L_P[\text{dBm}] &= 10 \cdot \log \left(\frac{V_{\text{noise}}^2}{1 \text{ mW} \cdot R} \right) = 20 \cdot \log \left(\frac{V_{\text{noise}}}{\sqrt{1 \text{ mW} \cdot R}} \cdot \frac{1 \mu\text{V}}{1 \mu\text{V}} \right) \\ &= 20 \cdot \log \left(\frac{V_{\text{noise}}}{1 \mu\text{V}} \right) - 20 \cdot \log \left(\frac{\sqrt{1 \text{ mW} \cdot R}}{1 \mu\text{V}} \right) \\ &= L_V[\text{dB}\mu\text{V}] - 106.989 \quad . \end{aligned} \quad (4.5)$$

The manufacturer of the current clamp provides the transfer function of the current clamp detailing the transfer impedance Z as a function of frequency [37]. With this the power ratio can be converted into a current ratio [39]:

$$L_I[\text{dB}\mu\text{A}] = L_V[\text{dB}\mu\text{V}] - Z[\text{dB}\Omega] = L_P[\text{dBm}] + 106.989 - Z[\text{dB}\Omega] \quad . \quad (4.6)$$

The current induced in the current clamp can be calculated by applying Equation 4.4:

$$I[\mu\text{A}] = 10^{\left(\frac{L_I[\text{dB}\mu\text{A}]}{20}\right)} \cdot 1 \mu\text{A} \quad . \quad (4.7)$$

4.2 Comparison of noise with and without shield

The conducted noise of the POH is measured both with and without shield. Measurements were performed at all output connectors of the POH using the crossover board. Frequency and amplitude of the noise are sensitive to the temperature of the converters as well as the precise position of the POH in the setup. To account for these effects each measurement was repeated five times. The POH was moved between measurements and it was ensured that enough time elapsed between measurements to let the converters cool down. Statistical uncertainties were calculated by repeating the full analysis for each measurement and then calculating the mean and standard deviation.

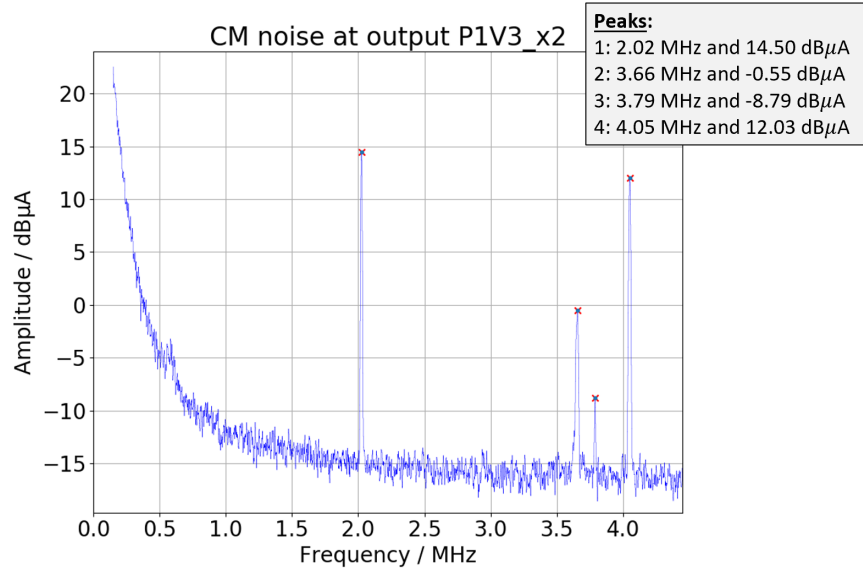


Figure 4.4: First four peaks in the measured common mode spectrum at the 1.3 V output of the POH without shield.

The first four peaks visible in the CM noise spectrum measured at the 1.3 V output connector of the POH without shield are shown in Figure 4.4. The noise floor decreases with increasing frequency. Single peaks stand out from this noise floor. The first three peaks correspond to the switching frequencies of the converters while the fourth peak can be ascribed to the first order harmonic of the bPOL12V switching frequency. To quantitatively compare noise between measurements the height of these peaks is used. This is justified as, considering the peaks are only a few bins wide and taking into account the logarithmic scale, the bulk of the signal is contained within a single bin for each peak.

Only very little noise is present at the output of the POH once the shield is applied. This

shows that the measurements are very sensitive to any additional signals propagating at high frequency within the testing environment. In an effort to prevent these signals from influencing the result a background measurement, during which the POH is not powered, is performed and subtracted from the actual measurement. For this both the background measurement and the signal spectrum are converted into linear units (Eq. 4.7) and the difference of the two is calculated. An additional benefit of this method is that subtracting background events allows for more sensitive peak finding, which is especially important when the peaks are low in amplitude. The following measurements (e.g. Fig. 4.5) illustrate the effectiveness of this method: For frequencies above 1 MHz no background is visible in the spectra and the peaks corresponding to the switching frequencies of the converters stand out distinctly from the noise floor.

Figure 4.5 shows different CM measurements at the 1.5 V output connector of the POH over a frequency range from 15 kHz to 30 MHz. When measured without shielding a lot of CM noise is present at the output. The CM noise is significantly reduced once the shield is soldered to the POH. This can be explained as CM noise is created by inductive coupling into the part of the supply cable that is not grounded to the copper plate. Adding shielding to the converters reduces this effect. The CM spectra are dominated by the switching frequency of the bPOL12V as well as its higher order harmonics. The switching frequencies of the second stage converters are also visible but their peaks are significantly lower than those corresponding to the bPOL12V switching frequency. Previous studies outlined that noise created by DC-DC converters is dependent on the conversion ratio $r = \frac{V_{\text{out}}}{V_{\text{in}}}$ and the switching frequency f [34]. The noise at the output is proportional to the conversion ratio and inversely proportional to the square of the switching frequency: $\delta V_{\text{out}} \propto \frac{r}{f^2}$. Considering the switching frequency of bPOL12V is approximately half and its conversion ratio is approximately double that of bPOL2V5 the noise of bPOL12V is expected to be eight times that of bPOL2V5 and therefore the peaks corresponding to the bPOL12V dominate the spectrum.

Almost no noise peaks are visible in the DM measurements (Fig. 4.6). Comparing the DM measurements with and without shield the only significant difference is the frequency peak at approximately 28 MHz that is only visible in the spectrum without shielding. This is not fully understood but might be an effect involving all three converters, as 28 MHz corresponds to the first common multiple of the switching frequency of all three converters: $f = (2.02 \cdot 3.66 \cdot 3.79) \text{ MHz} \approx 28.02 \text{ MHz}$.

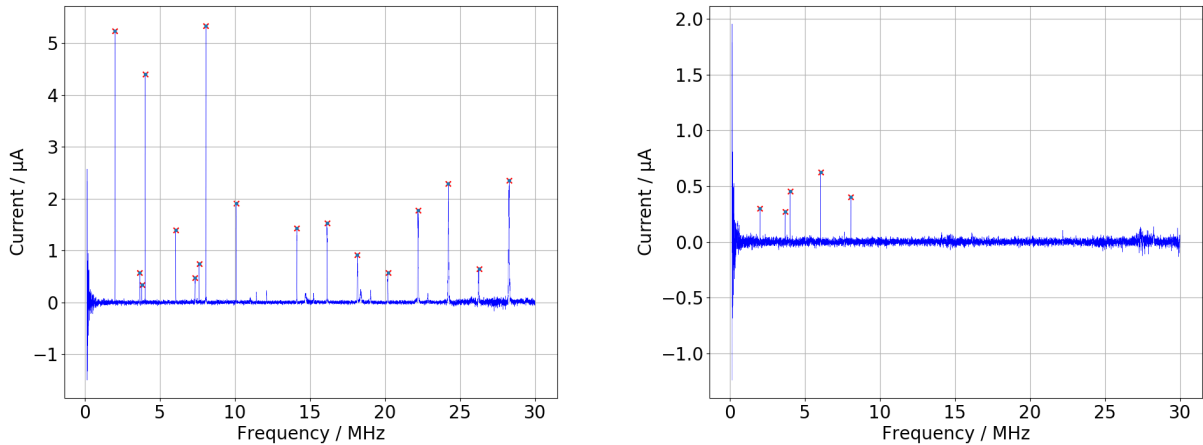


Figure 4.5: CM noise spectra measured at the 1.5 V output connector of the POH on X_2 side without (left) and with (right) shield applied to the POH.

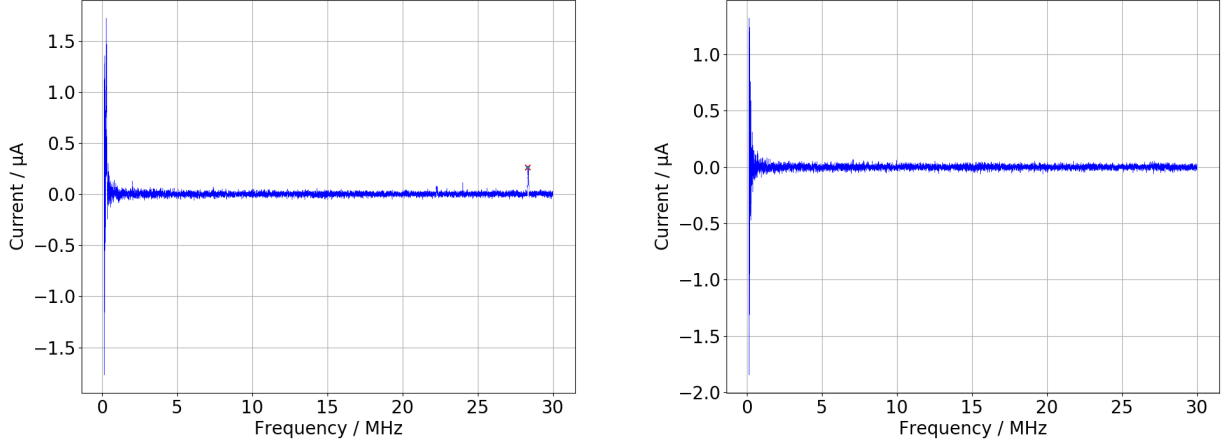


Figure 4.6: *DM noise spectra measured at the 1.5 V output connector of the POH at X_2 side without (left) and with (right) shield applied to the POH.*

To quantitatively compare these measurements the quadratic sum $\sqrt{\sum_i I_i^2}$ of the amplitudes of all frequency peaks visible in the noise spectrum is taken. Figure 4.7 shows the results for CM and DM noise at all output connectors¹ of the POH. As discussed above a significant reduction in CM noise is visible when shielding is applied to the converters. The CM noise at X_2 is approximately 1/10 of its original value once the shield is applied to the POH. This confirms that the high CM noise is a result of inductive coupling into the supply cable which is located at X_2 . This also explains why without the shield the CM noise measured at X_3 is significantly lower than the noise measured at X_2 . DM noise is low regardless of shielding. When considering the 1.3 V and 1.5 V output connectors of the POH DM noise can only be measured at X_3 . The reverse is true for the 2.55 V output connectors where DM noise can only be measured at X_2 . This is due to the fact that the bPOL2V5 converters are located closer to X_3 while the bPOL12V converter is located closer to X_2 on the PCB. When considering the height of the first peak visible in the spectrum which corresponds to the bPOL12V switching frequency (Fig. 4.8), the same effects can be observed.

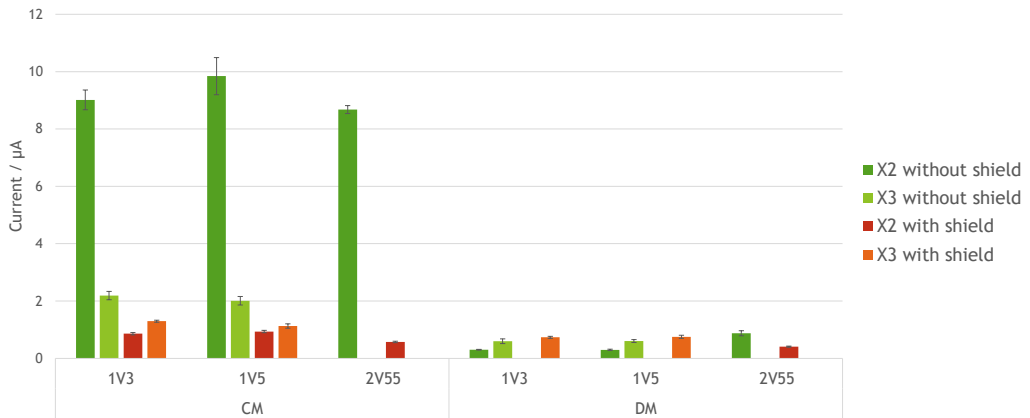


Figure 4.7: *Summarized results for the quadratic sum at the output connectors of the POH.*

¹Sides are denoted by X_2 and X_3 as introduced in Figure 2.8.

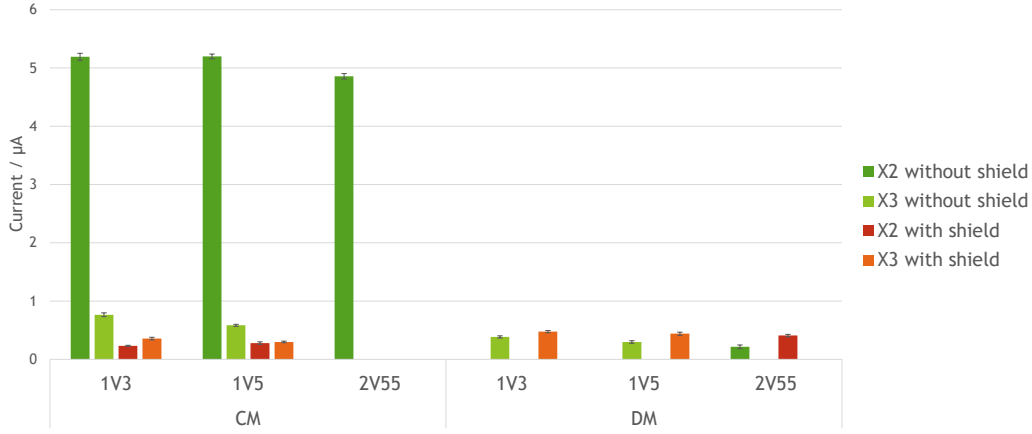


Figure 4.8: Summarized results for the height of the first peak (bPOL12V switching frequency) at the output connectors of the POH.

Additionally measurements at the common input of the POH were performed. The results of these measurements are shown in Figure 4.9 (CM noise) and 4.10 (DM noise). CM noise is significantly reduced by adding shielding to the POH while DM noise remains roughly the same. If conducted noise is indeed created by coupling of electromagnetic radiation of the converters into parts of the setup that are not properly grounded, this might be indication that the electromagnetic radiation of the converters is mainly produced by CM currents. In both the CM and DM noise measurements alternating currents at the switching frequency of the bPOL12V and higher harmonics dominate the spectrum. Noise generated at the input of a DC-DC converter is proportional to the conversion ratio and antiproportional to the switching frequency: $\delta V_{in} \propto \frac{r}{f}$ [34]. Therefore the noise of bPOL12V is only expected to be roughly four times that of bPOL2V5 at the input of the POH. Consequently peaks corresponding to the switching frequency of bPOL2V5 are more visible in the CM spectrum at the input than at the output of the POH and even higher harmonics can be observed.

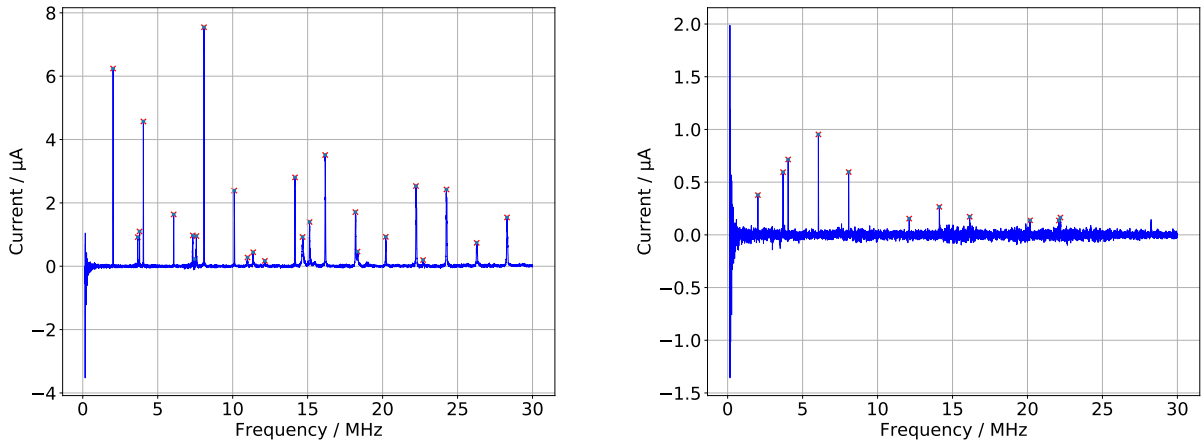


Figure 4.9: CM noise spectra measured at the input connector of the POH without (left) and with (right) shield applied to the POH.

Similar to the measurements at the output connectors of the POH in the CM noise spectrum without shield the peaks corresponding to the bPOL12V switching frequency and its third order harmonic are significantly higher than the other peaks visible in the spectrum. Once the shield is applied the amplitude of both these peaks is significantly reduced. The highest peak visible

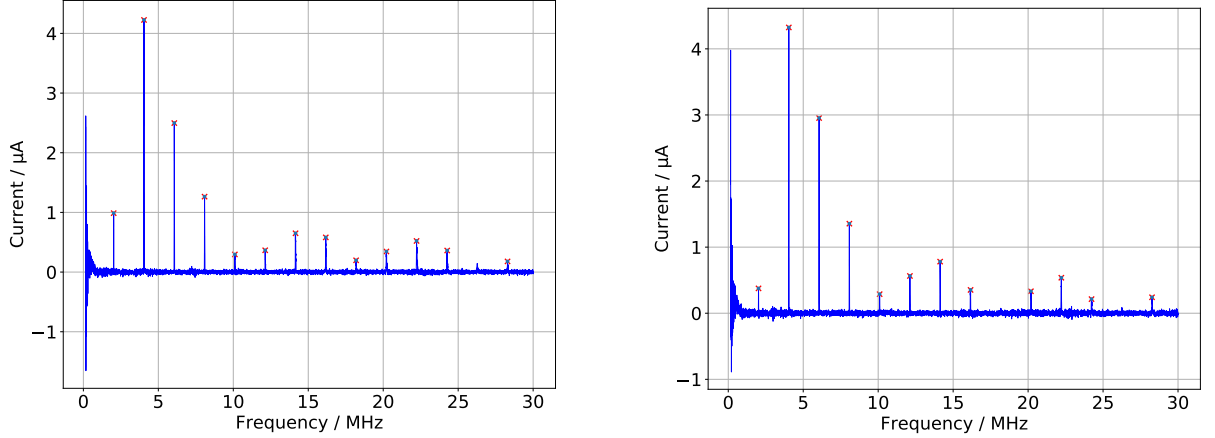


Figure 4.10: *DM noise spectra measured at the input connector of the POH without (left) and with (right) shield applied to the POH.*

in the spectrum is now the second order harmonic of the bPOL12V switching frequency. The highest peak visible in the DM spectrum measured at the input connector is the first order harmonic of the bPOL12V switching frequency.

The quadratic sums of all measurements of the CM and DM noise of the POH are summarized in Tables 4.1 and 4.2, respectively.

		P1V3	P1V5	P2V55	Input
Without shield	X_2	9.01 ± 0.35	9.84 ± 0.65	8.68 ± 0.14	11.78 ± 0.78
	X_3	2.19 ± 0.14	2.01 ± 0.15	—	
With shield	X_2	0.86 ± 0.04	0.94 ± 0.04	0.57 ± 0.02	1.55 ± 0.02
	X_3	1.30 ± 0.03	1.13 ± 0.08	—	

Table 4.1: *Summary of quadratic sums of CM noise in μA .*

		P1V3	P1V5	P2V55	Input
Without shield	X_2	0.30 ± 0.01	0.30 ± 0.02	0.88 ± 0.09	5.28 ± 0.28
	X_3	0.60 ± 0.08	0.60 ± 0.05	—	
With shield	X_2	—	—	0.41 ± 0.02	5.43 ± 0.17
	X_3	0.74 ± 0.03	0.75 ± 0.06	—	

Table 4.2: *Summary of quadratic sums of DM noise in μA .*

In summary very little conducted noise was measured. Most importantly almost no DM noise was measurable at the output connectors of the POH once the shield was soldered to the prototype. This is beneficial for use in the detector as ripples in the output voltages of the converters would negatively impact the performance of the front-end electronics [40]. Additionally these tests revealed that bPOL12V seems to generate more noise at the X_2 while the second stage converters generate noise at X_3 . As expected the peaks attributed to the bPOL12V switching frequency and its harmonics were generally higher than those attributed to the switching frequencies of the bPOL2V5 converters.

5 Radiated noise

In addition to noise conducted through the cables, noise radiated from the converters is of interest in applications involving DC-DC converters. The alternating current (Eq. 2.5) flowing through the inductor at the switching frequency generates a switching magnetic field which can be measured inductively using a pickup coil. The magnetic field of an ideal toroidal inductor is contained within the inductor. However in real world applications a magnetic field outside the inductor is still measurable due to current flux along the single-turn loop around the central hole of the toroid. A parasitic field through the centre of the toroid will be generated. This does not impact the inductance of the coil or the energy stored within the inductor [41].

5.1 Experimental Setup

Figure 5.1 shows the setup used to measure the electromagnetic radiation of the POH. A schematic drawing of the setup is provided in Figure 5.2. The POH (1) is powered using a laboratory power supply (2, Agilent E3633A DC power supply [35]). For all measurements the input voltage is set to 10 V. A pick-up coil (3, ETS-Lindgren model 7405-703 [42]) is used to measure the magnetic field radiated from the converters. BNC cables connect the pickup coil to a spectrum analyzer (4, Agilent Technologies EXA N9010A signal analyzer 9 KHz-3.6 GHz [38]), where the induced voltage is measured. A controller unit (isel CNC controller C142-4 [43]) steering a xyz-stage (5, two isel LES 4 linear units and one isel LES 5 linear unit [44] driven by two MS160 and one MS300 two-phase step motors [45]) is used to move the pick-up coil over the POH in a 1 mm by 1 mm grid. Across all measurements the distance of the coil to the POH in z remained constant at approximately 1 mm above the coil.

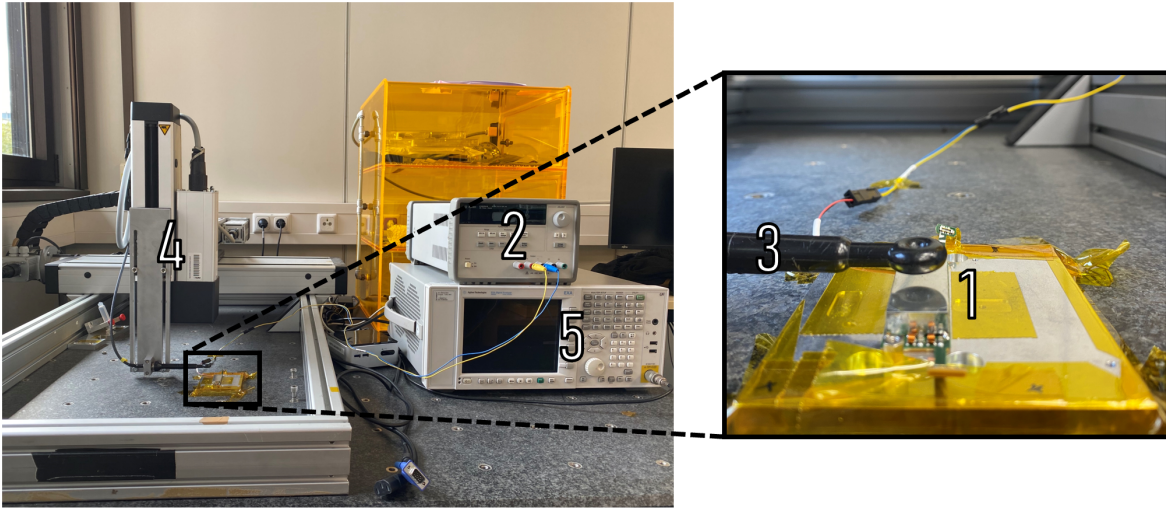


Figure 5.1: *Setup for measuring radiated noise of electrical components.*

Measuring magnetic fields using the spectrum analyzer

The spectrum analyzer measures the absolute power ratio L_P picked up by the coil in units of decibel-milliwatts (dBm). For each point of the grid the coordinates as well as the maximum

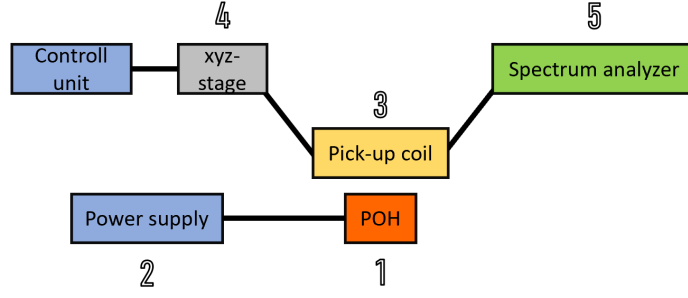


Figure 5.2: Schematic drawing of the setup used to measure radiated noise from the POH.

power ratio within a given frequency band is recorded. To calculate the absolute magnetic field strength H_{rad} from the power ratio L_P it is first converted to the absolute voltage (Eq. 4.6). The manufacturer of the current probe specifies in the manual [42] that the ratio of the field strength L_H can be obtained by adding the so-called “Probe Performance Factor” (PPF), which is defined as the ratio of the field to the voltage developed by the probe at the BNC connector, to the voltage ratio:

$$L_H[\text{dB}\mu\text{A}/\text{m}] = 20 \cdot \log \left(\frac{H_{\text{rad}}}{1 \mu\text{A}/\text{m}} \right) = L_V[\text{dB}\mu\text{V}] + PPF - 51.52 \quad . \quad (5.1)$$

The PPF is approximately 100 dB in the frequency range of interest. The pick-up probe was characterized in a transverse electromagnetic mode cell, which presented a field with a 377Ω impedance (= impedance of air). Therefore, to graph the corresponding H-field response, an additional factor of $51.52 \text{ dB} = 20 \cdot \log \left(\frac{377 \Omega}{1 \Omega} \right)$ must be subtracted from the voltage ratio. The absolute magnetic field can be calculated by solving this equation for the magnetic field strength H_{rad} :

$$H_{\text{rad}}[\mu\text{T}] = 10^{\left(\frac{L_V[\text{dB}\mu\text{V}] + 100 - 51.52}{20} \right)} \cdot 1 \mu\text{T} \stackrel{(4.6)}{=} 10^{\left(\frac{L_P[\text{dBm}] + 106.989 + 100 - 51.52}{20} \right)} \cdot 1 \mu\text{T} \quad . \quad (5.2)$$

5.2 Comparison of electromagnetic radiation with and without shield

The electromagnetic radiation of three converters without and with the shield soldered to the PCB was measured. To ensure that only one converter frequency is picked up by the coil, the frequency band the measurements are performed in is chosen to be 0.35 MHz wide and the frequency around which this interval was centred (centre frequency = cf) is chosen accordingly. When interpreting the results it is important to consider that these measurements only show components of the magnetic field propagated in z-direction.

Figure 5.3 shows the electromagnetic radiation of each of the three converters without the shield. An image of the POH is superimposed on the measurements. The shape of the parasitic magnetic field is consistent with previous studies of air-core toroidal coils and can be explained by the current flux along the single-turn loop around the central hole of the toroid [41]. Therefore the maximum magnetic field is measured above the centre of the inductor. It rapidly decreases at points in the grid further away from the inductor.

5.2. COMPARISON OF ELECTROMAGNETIC RADIATION WITH AND WITHOUT SHIELD

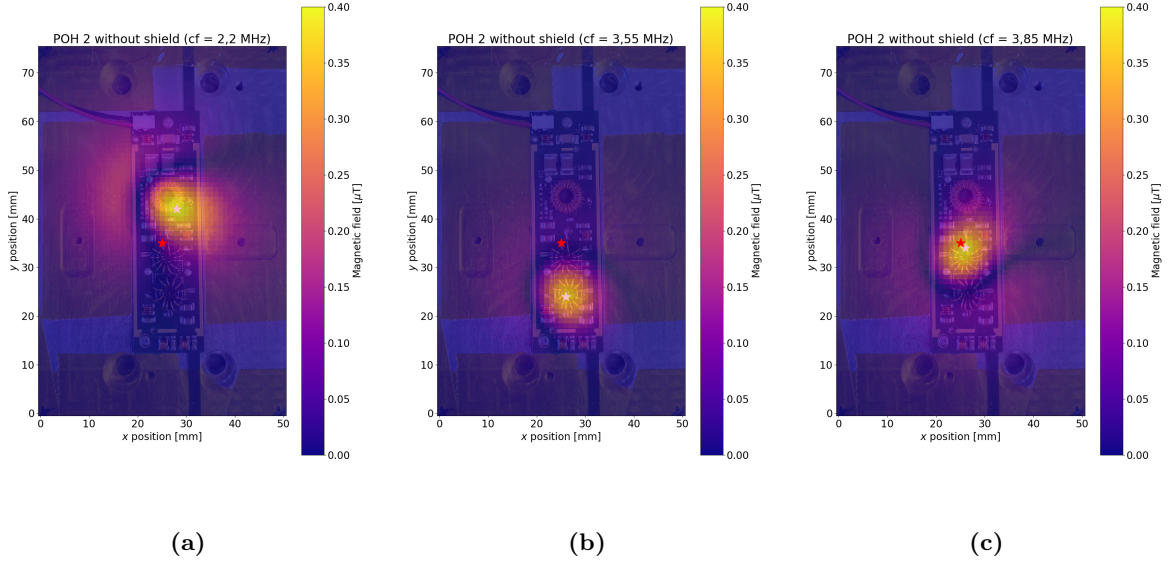


Figure 5.3: Measurements of the radiated magnetic field of the POH without shield. The measurement was performed at a centre frequency of 2.2 MHz (a) for bPOL12V and for the bPOL2V5 converters at centre frequencies of 3.55 MHz (b) and 3.85 MHz (c).

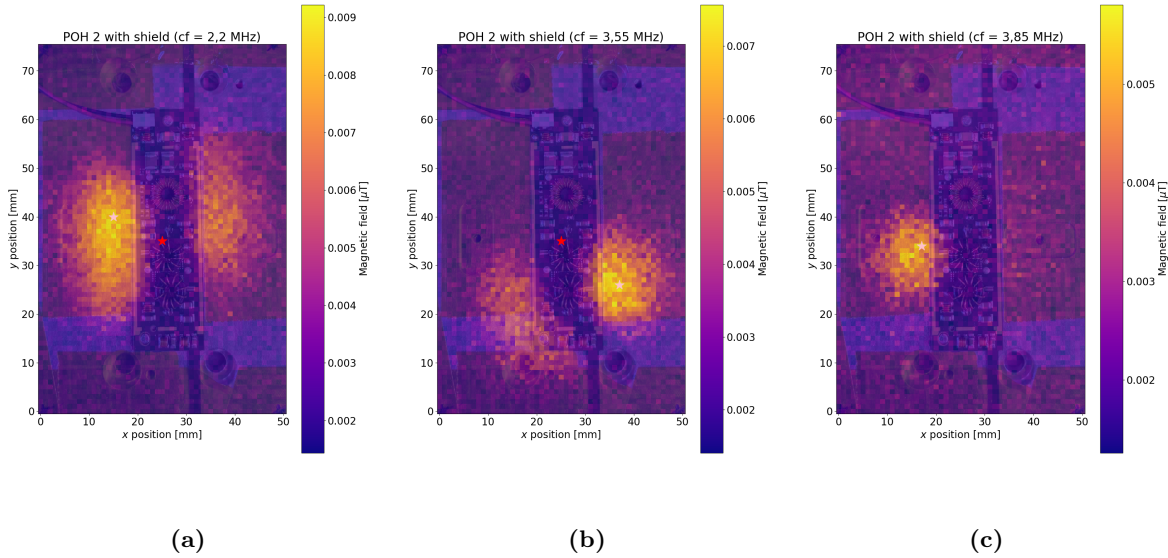


Figure 5.4: Measurements of the radiated magnetic field of the POH with shield. The measurement was performed at a centre frequency of 2.2 MHz (a) for bPOL12V and for the bPOL2V5 converters at centre frequencies of 3.55 MHz (b) and 3.85 MHz (c).

Figure 5.4 shows the electromagnetic radiation of each of the three converters with the shield soldered to the POH. When considering the scale of the plots it is apparent that the radiated noise is drastically reduced once the shield is applied to the POH. Compared to the measurements without shield (Fig. 5.3) the measurement appears grainy. This is because the electromagnetic radiation of the converters is so low that background noise becomes relevant. However, some emission of the converters remains, even with the shield applied to the POH. The magnetic field

is no longer contained in a single spot above the converter. Instead it spreads along the whole edge of the POH where the shield is soldered. The remaining electromagnetic radiation is dominated by the bPOL12V. This can be seen in the measurements, as the emission corresponding to the bPOL12V switching frequency covers a much larger area than that of the second stage converters.

The results for the maximum magnetic field strength as well as the average of the magnetic field across the whole grid can be found in Table 5.1. The average magnetic field is calculated by taking the mean of all data points in the grid. Without shielding the maximum magnetic field strength is about the same for all three converters. Once the shield is applied the maximum radiated emission is reduced by a factor of about 50 while the average magnetic field strength is only reduced by a factor of approximately 15. This in addition to the qualitative reasoning described above shows that the bulk of the field is no longer contained within the small area above the inductors but rather more spread out over a larger portion of the grid.

Centre frequency / MHz	$H_{\text{rad, max}} / \mu\text{T}$		$H_{\text{rad, avg.}} / \mu\text{T}$	
	without shield	with shield	without shield	with shield
2.2	0.42	0.0092	0.039	0.0029
3.55	0.38	0.0076	0.019	0.0024
3.85	0.39	0.0058	0.028	0.0020

Table 5.1: *Summary of the maximum and average magnetic field strengths measured in the scans.*

In summary these measurements show that the magnetic radiation of the converters can be drastically reduced by soldering the aluminium shield to the POH. Additionally the shape of the radiated magnetic field is consistent with previous studies of the magnetic field of toroid inductors.

6 Summary and Outlook

In this thesis studies of the electrical properties of the PS-POH prototype with the newest versions of the converter chips are presented for the first time. Measurements of the dynamic behaviour during turn-on and turn-off as well as of the efficiency were performed. Additionally the conducted and radiated noise of the prototype was characterized.

The dynamic behaviour of the prototype during the slower ramp-up/-down time of 29 V/s revealed that, in order to prevent unintentional turn-on/-off of the converters due to UVL, resistor R_{25} in the voltage divider should be changed from 17.8 k Ω to 9.09 k Ω . Except from this issue the dynamic behaviour of the prototype is satisfactory. Spikes in the input current can occur due to the (dis-)charging of capacitors on the PCB. As each LVPS will feed more than one PS module in the detector, further studies with more than one POH are needed to gauge how this will affect the current flow along the common return line of these modules.

The efficiency loss due to the DC-resistance of the toroidal coils, used on the prototype was characterized. The efficiency of the entire PS-POH was determined to be $\approx 61\%$ at 10 V input voltage. It was established that the efficiency drops around 0.71 % per additional volt of input voltage. Further 8 % points of efficiency are lost when measuring at the output connectors of the POH due to the voltage drops across the PCB. In the context of these measurements a malfunction of the adaptive logic of bPOL12V was discovered. It has been changed in the newer version of the ASIC.

Conducted and radiated noise of the prototype are generally low. Almost no DM noise is generated at the output of the converters. Applying the aluminium shield to the POH drastically reduces both CM noise and radiated noise of the converters. The low DM noise at the output connectors will most likely benefit the front-end electronics. More comprehensive test with fully assembled PS modules are needed to further assess these results.

Several PS-POH prototypes with the improved voltage divider are being distributed to the CMS Collaboration. They will be used to assemble prototypes of the complete PS module and subjected to further testing. In the future the PS-POH prototypes will be developed at CERN and will be available in 2021.

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Appendices

Appendix A: PS-POH schematics

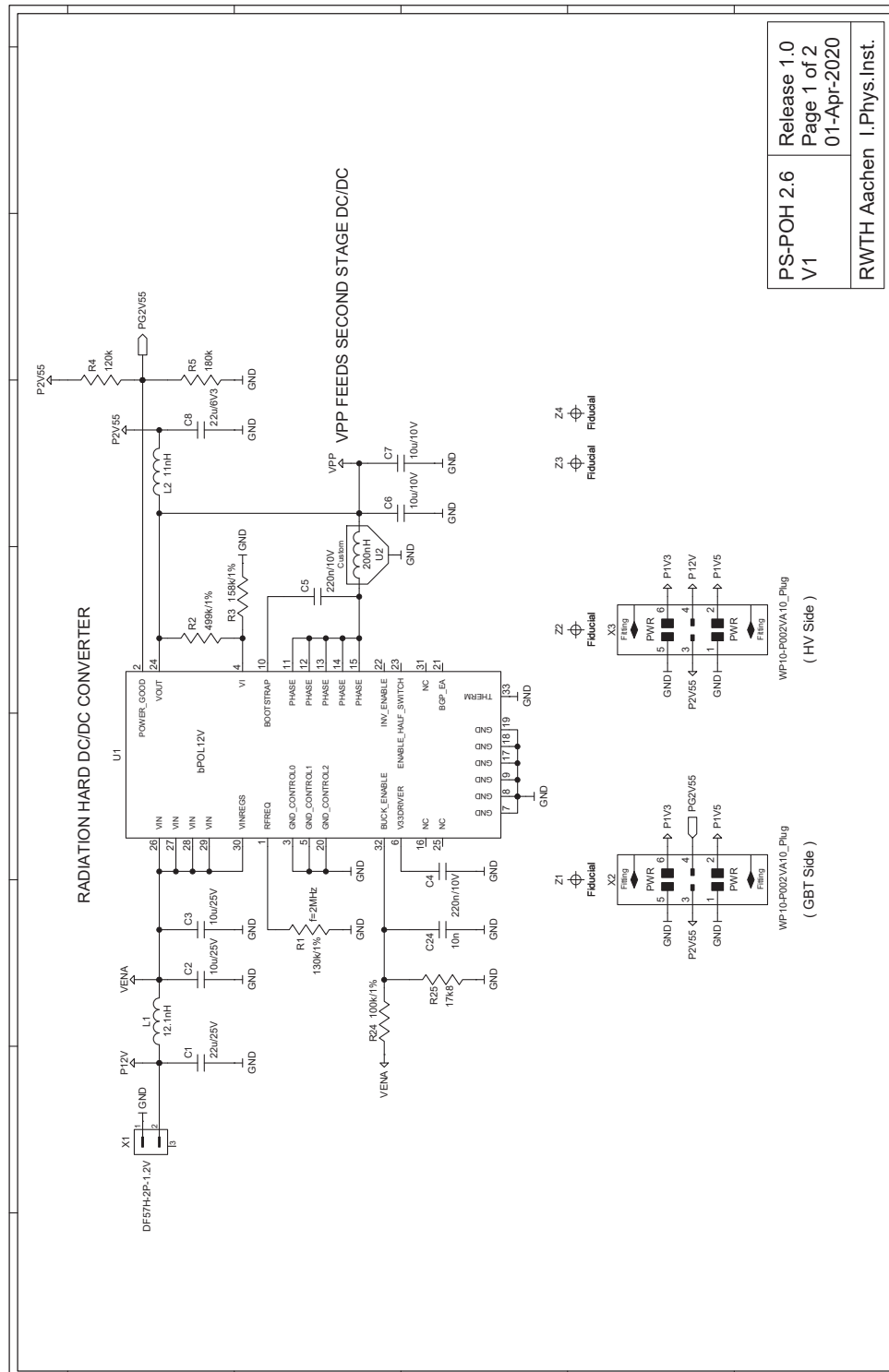


Figure A.1: *Page 1 of the PS-POH schematics.*

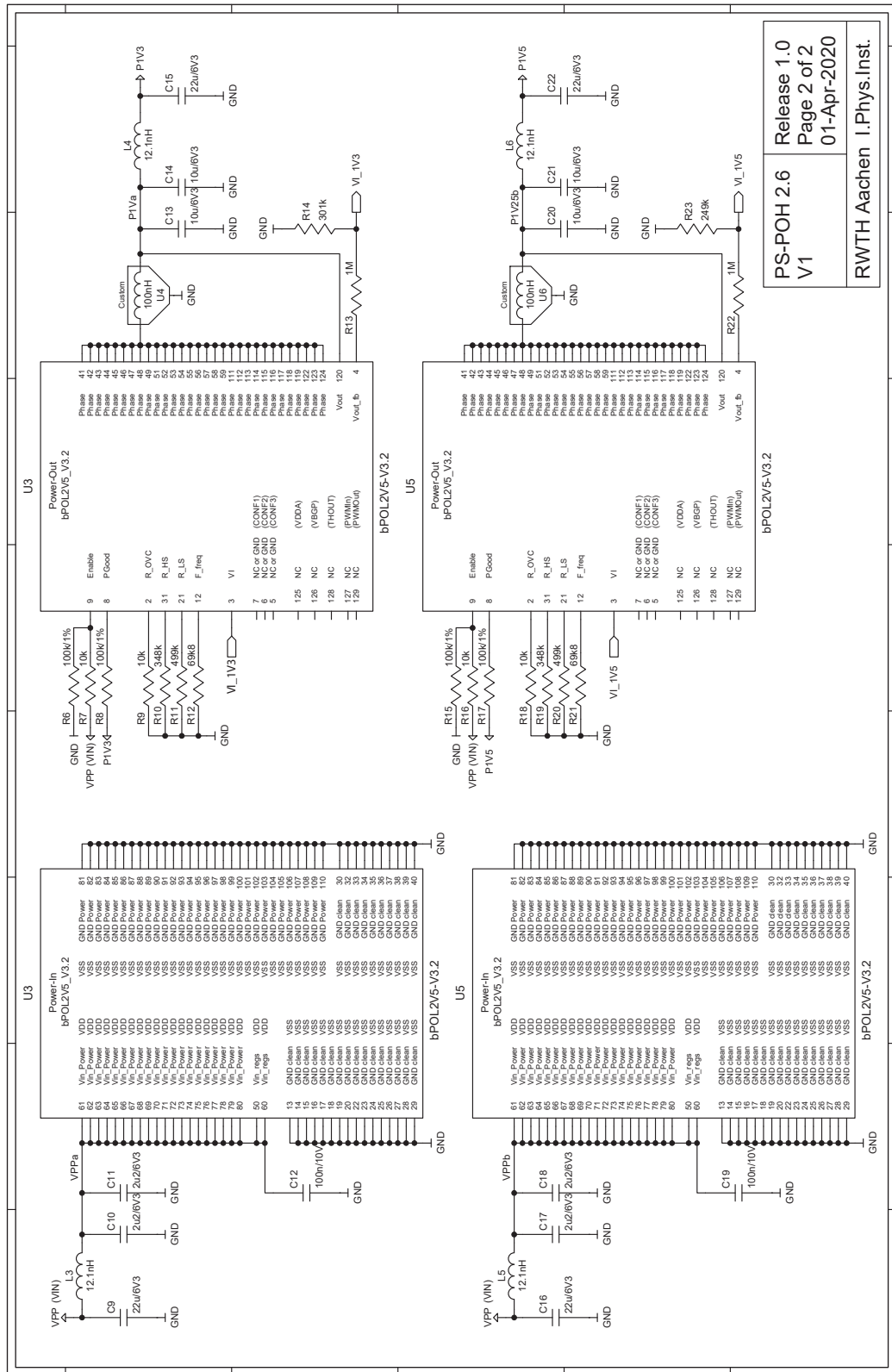


Figure A.2: Page 2 of the PS-POH schematics.

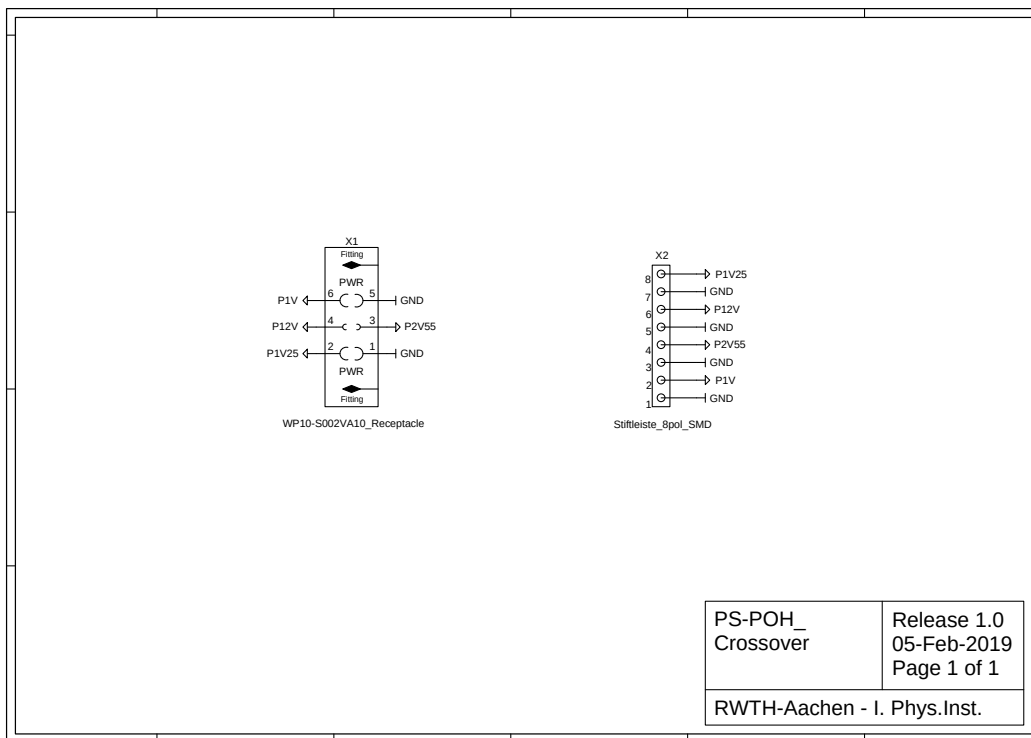


Figure A.3: Page 1 of the PS-POH Crossover schematics.

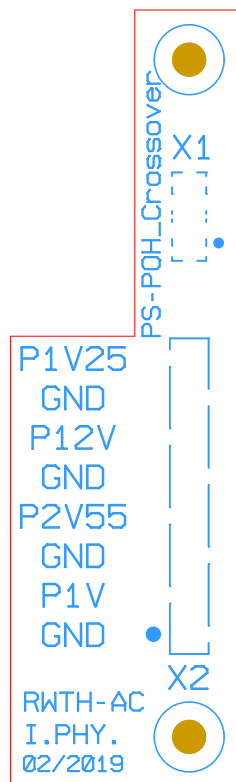


Figure A.4: Layout of the PS-POH Crossover.

Appendix B: Loadboard schematics

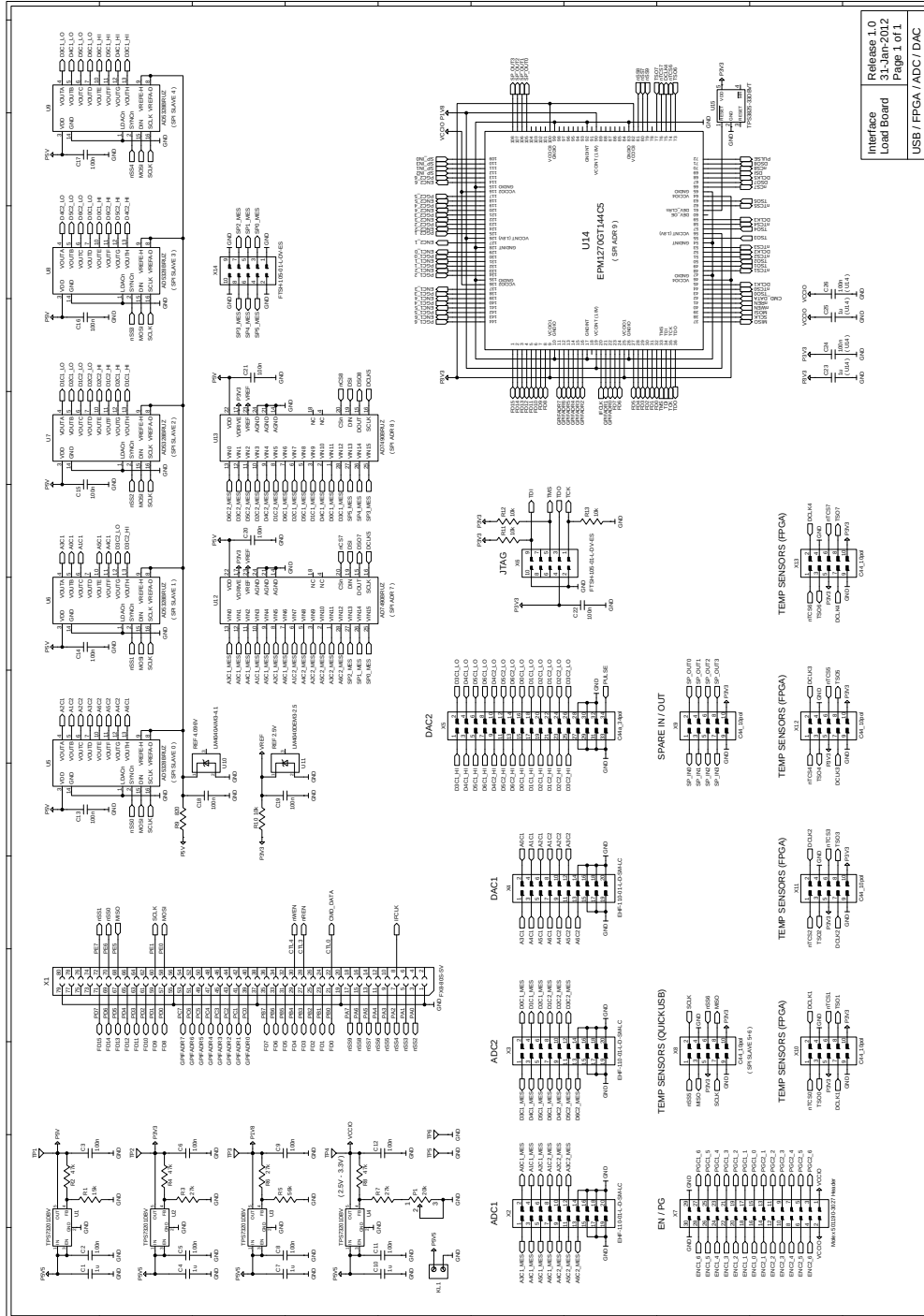


Figure B.1: Schematics of the Load Board Interface.

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Ich versichere, dass ich die Arbeit selbstständig verfasst und keine anderen als die angegebenen Quellen und Hilfsmittel benutzt sowie Zitate kenntlich gemacht habe.

Aachen, den 27.10.2020