

SEMINARS SEMINAIRES

Monday 30 September

AC SEMINAR

at 11.00 hrs – AT Auditorium

bldg 30, 7th floor

News from the Superconducting Super Collider

by E.J.N. WILSON / CERN/PS

The detailed design and specification of the major components of the SSC is now well under way and the manufacture of full length magnet prototypes for a test cell is in full swing. There is much to interest designers of CERN's LHC as well as those responsible for room temperature machines. The speaker, who recently visited Dallas where much of this work is going on, will summarise the present status of the Collider and the three rings in the injector chain and describe the salient features of their design.

Mardi 1er octobre

PRESENTATION

09.30–12.00 h – Amphithéâtre CN

bât. 31/3-005

Les réseaux logiques programmables (FPGA) d'Actel

Andy BIDDLE / ACTEL European Technical Manager (GB) & Pascal FERNANDEZ, Société SCAIB (F)

ACTEL CORPORATION, basée à Sunnyvale en Californie est l'inventeur du procédé antifusible PLICE™. Cette société propose les familles FPGA (Field Programmable Gate Array) ACT1™ et ACT2™ équivalentes à des architectures "gate arrays" de 1200 à 8000 portes. La programmation sur site permet de configurer ces composants FPGA en quelques minutes. Sur une station de travail type APOLLO™, SUN3/4™, ou PC386, avec les plateformes CAE telle que Mentor Graphics™, Orcad™, Viewlogic™, Valid™, Ales™, le logiciel propriétaire ALS (Action Logic System) d'ACTEL permet le placement routage à 100% automatique ainsi que des moyens sophistiqués de diagnostics aidant à la vérification de la conception. En dehors de ces configurations station de travail plus logiciel supportées par ACTEL, un grand nombre de sociétés ont développé une passerelle vers le logiciel ALS, en collaboration étroite avec ACTEL.

- Principes de l'architecture ACTEL
- Famille ACT1 (1200 et 2000 portes)
- Famille ACT2 (8000, 4000 et 2500 portes)
- Logiciel de développement ALS
- Démonstration

Responsable : J.-M. Sainson / CN

Mardi 1er octobre

PRESENTATION TECHNIQUE

14.00-17.00 h – bât. 865/2-A04

Tekelec Airtronic (F), spécialisé dans les périphériques informatiques standards et spécifiques, présente les terminaux X-WINDOWS NCD (USA) connectables sur port Ethernet thin et thick ou 10 base T: NCD 16 E résolution écran 1024 × 1024, processeur 68020 à 15 MHz, mémoire extensible jusqu'à 8 Mo; NCD 14 C résolution écran 1280 × 768, processeur 68020 à 20 MHz, 2 coprocesseurs graphiques, mémoire extensible jusqu'à 8 Mo; NCD 19 C résolution écran 1280 × 1024, processeur 8800 à 20 MHz, 2 coprocesseurs graphiques, mémoire extensible jusqu'à 40 Mo au total.

Langues: français, anglais

Renseignements : M. Diraison / FI / 4585

Wednesday 2 October

PRESENTATION

at 10.30 hrs – CN Auditorium

bldg 31/3-005

ONTOS – Architecture and Functionality of an Object-Oriented Database Management System

by Stefan SCHNEIDER / GOPAS Software GmbH (Senior consultant and specialist)

ONTOS DB is a flexible, full function, distributed object database management system designed for C++ programmers developing complex modeling applications. Schema definition, object manipulation, and application implementation are all performed in the C++ language. ONTOS provides an integrated C++ environment for application development, as well as graphical tools for interactive access with the object database. ONTOS also features a complete set of meta-classes, flexible and optional transaction and concurrency control models, extensible storage management, and an integrated object SQL. A DBDesigner tool can be used to interactively define database schema and subsequently generate the corresponding C++ class definition files from it for use in the application. DBDesigner can additionally be used to create, modify and browse the database schema and object instances. Databases are administered using the DBATool. The presentation will give an overview of the functionality and the architecture of ONTOS

Organizer : R.Jones / ECP / jones@vxcern.cern.ch

Wednesday 2 October

THEORETICAL SEMINAR

at 14.00 hrs – TH Conference Room

Speaker and title to be announced

Wednesday 2 October

COMPUTER FORUM

at 16.00 hrs – CN Auditorium

bldg 31/3-005

The SHIFT Project

by Bernd Panzer STEINDEL / CERN-PPE &
Thierry MOUTHEY / Indiana

The OPAL/CN SHIFT project is a distributed computing system for DST analysis with online access to about 100Gb of data. The OPAL environment and the use of SHIFT by OPAL physicists will be described; CN experts will be on hand for the discussion.

Organizer: M. Metcalf/CN

Vendredi 4 octobre

PRESENTATION TECHNIQUE

08.00-16.00 h – Hydrosystème SA, 107, rte du Nant
d'Avril, Meyrin

Hultegger & Cie S.A. (CH), technique de soudage et découpage, propose une démonstration de machines et matériel de soudage dans les locaux de Hydrosystème S. A. / Meyrin. Contenu de la présentation : installations de soudage MIG/MAG, MAG pulsé, TIG, TIG pulsé, à l'arc, coupage plasma, électrodes enrobées 'MUERO', baguettes TIG, fils pleins MIG/MAG, fils fourrés, accessoires de soudage.

Fabricants : Kemppi OY (SF), Migatronik A/S (DK), OTC Daihen (J), SAF (F), Tesch Orbital System (D), + divers (CH).

Langues : allemand, anglais, français

Renseignements : M. Diraison / FI / 4585

Friday 4 October

DETECTOR SEMINAR

at 11.00 hrs – ECP Conference Room

bldg 13/2-005

Recent developments in spark counters

by Yuri PESTOV / INP, Novosibirsk

Friday 4 October

MEETING ON PARTICLE PHYSICS PHENOMENOLOGY

at 14.00 hrs – TH Conference Room

Charmed and beauty baryon masses

by Peter VOLKOVITSKY / ITEP, Moscow

Friday 4 October*

COMPUTING SEMINAR

at 14.00 hrs – ECP Auditorium

bldg 13/2-005

The Cesar Computer Architecture

Introducing a new level of vector processing

Morten Toverud / Norwegian Defense Research
Establishment

The presentation will give an introduction to the Cesar computer system, in which parallelism and pipelining are combined at different levels to achieve a programmable 'algorithm processor' for computationally intensive vector problems. Driven by one specific application, the processing of images from Synthetic Aperture Radar (SAR), the Cesar computer is a result of research and development activities at the Norwegian Defense Research Establishment over the past decade. The excellent sustained performance is made possible through a high degree of parallelism with no communication overhead. The system is implemented using custom integrated circuits, resulting in compact and aircooled hardware. The programming environment on a standard Unix workstation allowing the use of several general purpose programming languages will also be covered. Some of the current and potential applications will be discussed, and performance measures will be presented.

Mr Toverud has been working at NDRE with computer architecture and design of VLSI circuits since 1981. From 1986 he has been project manager and responsible for the development of the Cesar vector processor. He is also project manager for a technology study on SAR processing performed for ESA, and chairman of the management group for a Research Technology Project in EUCLID on real time processing and data handling in remote sensing. Mr Toverud is also giving lectures at the University of Oslo in graduate courses in computer science.

Organizer: J.P. Matheys / ECP / Matheys@online.cern.ch

* Note the unusual day, time and place

Tuesday* 8 October

CERN COMPUTER COLLOQUIUM

at 16.30 hrs – Council Chamber

Optical Wavelength Division Communications Technology

by P.E. Green / IBM Research, Yorktown Hts

Organizer: F. James/CN

* Please note unusual day and room