



COMMUNICATIONS OFFICIELLES

Les membres du personnel sont censés avoir pris connaissance des communications officielles ci-après.

La reproduction même partielle de ces informations par des personnes ou des institutions externes à l'Organisation exige l'approbation préalable de la Direction du CERN.

OFFICIAL NEWS

Members of the personnel shall be deemed to have taken note of the news under this heading.

Reproduction of all or part of this information by persons or institutions external to the Organization requires the prior approval of the CERN management.

PRESTATIONS DE SOURCES EXTERIEURES

Il est rappelé aux membres du personnel qu'ils ont l'obligation de déclarer le montant de toute prestation reçue de sources autres que l'Organisation (article R IV 1.02 du Règlement du Personnel).

En particulier, les membres du personnel ayant bénéficié des récentes hausses d'allocations familiales en France et en Suisse sont invités à les notifier sans délai au Bureau des Dossiers de la Division du Personnel par l'intermédiaire de leur secrétariat de Division.

Division du Personnel
Tél. 3238-3903

BENEFITS FROM OUTSIDE SOURCES

Members of the personnel are reminded that they must declare the amount of any benefits they receive from sources outside the Organization (article R IV 1.02 of the Staff Regulations).

In particular, members of the personnel who benefited from the recent increases in French and Swiss family allowances are invited to inform the Staff Records Office of Personnel Division through their Divisional secretariat, without delay.

Personnel Division
Tel. 3238-3903

SEMINARS SEMINAIRES

Monday 26 March

EF SEMINAR

at 11.00 hrs – EF Conference Room
bldg 13, 2-005

**The Microprocessor of the Year 2000 –
VLSI technology and architectures in the LHC
era**

by Alessandro MARCHIORO / CERN

The evolution of VLSI technology and of the architectures of commercial processors will be examined. Based on current trends, projection for

the next decade technology will be made. Sub-micron processes will push integration levels to multi-million transistor devices. Such technologies present a totally new set of problems both to technologists and chip designers and profoundly influence choices of future architectures. Optimal systems can be designed only if all aspects of integration, interconnection and packaging are taken into account. The utilization of the new integration technologies for the design of the next generation of processors will be discussed together with the implications for the design of special devices for HEP.