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A CAMAC SYSTEM-CRATE INTERFACE
BASED ON EUR 6100 STANDARDS

by

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Abstract

Three CAMAC Serial Highways are installed in the Intersecting Storage Rings control system, driven by commercial units which are themselves constructed as CAMAC Modules. The drivers are housed in "system crates" interfaced to the Argus and Nord control computers. The system crate controllers are implemented as auxiliary crate controllers compatible with the Type L serial CAMAC equipment, and are PROM based to allow N, A and F to be generated from a small range of computer addresses and to be substantially transparent to the host computer. The concept has enabled standard modules and techniques taken from the Serial Highway system to be adopted for use in the system crates.

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1. Introduction

When the CAMAC Serial Highway became available in 1975 it was decided to apply it to extension of the control system of the CERN Intersecting Storage Rings, which, at that time, used a mixed interfacing system including some equipment supplied by the computer manufacturers, some CERN-developed interfaces and a few crates on the CAMAC Branch Highway. CAMAC equipment was restricted to the building housing the control centre, and was not available in the remote equipment buildings, up to 1 km from the control room. In view of the complexity of the Serial Highway Driver it was considered that it would be wise to purchase a commercial unit rather than develop one. A driver was selected, and for the first tests of the system it was operated in a crate on the CAMAC Branch (parallel highway). These trials had been performed on a Branch Highway which itself was interfaced to the computers in an indirect and unsatisfactory manner, so it was decided to install both parallel and serial system drivers in a new CAMAC system crate, housing commercial drivers which were themselves constructed as CAMAC modules.

The solution adopted for the Argus is described in the following sections. Two years later, when a major improvement of the ISR control system required that two additional serial highways be driven from Nord-10 computers, the same approach was adopted for the CAMAC system crate interface, with excellent results, and it is clear that the concept could be adapted to other types of mini-computer.

2. Main Features

2.1. Specification of CAMAC Operations in Small Address Fields

A single CAMAC crate controller must specify the required dataway cycle in some detail:

- Station number 5 bits
- Function 5 bits
- Sub-address 4 bits
- Data for write operations, normally 8, 16 or 24 bits.

The typical computer interface presents a data field, a short address field and sometimes one or two bits to specify a class of operation. It is clear that a system in which the operation can be specified in the address field can provide an attractive solution, able to perform the entire dataway cycle in one input/output cycle. Unfortunately,

few computers provide a full 14 bit field to specify N,A and F. Furthermore, part of the address range must often be reserved for other equipment, and perhaps for other CAMAC crates. This obliges the designer to install a register to hold one or more components of the N,A,F field. Pre-loading of the register removes the potential transparency from the interface, and requires a non-interruptible sequence for the simplest CAMAC operation.

A study of the range of CAMAC modules so far available indicates that for a given module, very few combinations of function and sub-address are used out of the 512 which may be specified. The combinations which are used are different for each module. In the case of the serial and parallel branch highway drivers, including the F1R0 for demand messages in the serial system, the total number of combinations of N,A and F which are implemented in the hardware is 66.

It was consequently decided to construct system-crate interfaces capable of performing any operations taken from a list of 256 operations programmed in a PROM within the interface module. The PROM address is taken from the lower 6 bits of the address specified in the computer I/O address, and the upper 4 bits of this address used to select a block of addresses for the particular crate. The memory circuits used for the PROM are 8-bit 32-word fusible link type, and the output of 16 bits is used to generate N,A,F and two internal control lines.

2.2. System Crates Based on Serial System Specifications

The Serial CAMAC Crate Controllers type L specified in EUR-6100 are provided with facilities for auxiliary controllers in the crate. As part of development for the serial system for the ISR, auxiliary access units had been designed, and a protocol defined for operation of one or more such units as auxiliary controllers operating in conjunction with the Type L crate controller (REF 1). It was realised that a similar scheme could be employed as a CAMAC system crate, in which the computer interface was acting as an auxiliary controller. By this means, development and testing of the new system could be simplified, as the crate could be driven from another computer either through an auxiliary access unit or from a working serial highway.

It was unfortunate that the definition of the Auxiliary Controller Bus by ESONE came too late for use in the ISR and that we had to define a protocol compatible with the original L-1 crate controller and using the

52-pin connectors.

3. The Argus 500 System Crate Interface.

The SCC-500 is implemented as three single-width modules. The control module deals with address and timing signals, contains the PROM and handles computer interrupts. A "data write" module contains a 24-bit register which is loaded from the computer just before the start of the CAMAC dataway cycle, and drives the W lines. A "data read" module contains a register loaded at S1 in read cycles, which passes data to the computer. It also contains a 4 bit status register and a 20 bit LAM register. The computer input/output highway is connected to each of these modules by 50 pin D type connectors, while they are interconnected by means of 15 pin connectors. At the rear, the auxiliary controller and LAM connector of the Type L or equivalent controller is linked to the control module (a double-width rear panel providing the loop-through on two 52-pin connectors) and to the data read module.

Four status signals are produced by each dataway cycle. These are:

- Q status bit, true
- X error, i.e. 1 when X=0
- off line
- auxiliary controller lockout

After a write operation, or after a 24-bit read operation, these status signals must be read from a register in a subsequent operation. In control operations, normally programmed as "read" and in read operations when 20 or fewer data bits are required, the 4 status indications are packed into the top 4 bits of the 24 bit word.

An auxiliary controller adaptor - an L-1 without the serial highway connection - provides line termination, N decode and LAM access for the SCC-500. Station 1 of the crate, as for all other on-line crates in the ISK, is occupied by a dataway service module which permits very comprehensive on-line tests to run without disturbing the remaining parts of the system. The test program, written in CORAL 66, is essentially the same for crates on the parallel highway, the serial highway or the system crate.

In addition to the system crate housing the CAMAC serial and parallel branch drivers, the Argus computers each have two other system crates attached. These are used for connections to terminals in the ISK control room, serial data links to Nord-10 computers, drivers for line printers and electrostatic graphics hard-copy units, etc. Many of the interface modules are compatible with the original Argus software routines and were thus easily integrated into the operating software, on account of the transparent nature of the SCC-500 interface.

All crates in the serial system

are fitted with SGL encoders of standard type. The serial highway driver has a 256-word FIFO memory so as to minimise the chance of missing demand messages, and this works well enough for us to regard a hung demand message as indicating a serious malfunction.

The SCC-500 interface was developed over the period March - December 1976, and put into full operational use in 1977.

4. The Nord 10 System Crate Interface.

The Nord-10 I/O interface is asynchronous and thus permits the full auxiliary controller protocol to be employed. A special feature is that all input and output is via a single accumulator, the direction being specified by the external equipment in its response to the request line from the computer. As the response of the external equipment, including the setting of the "INPUT" line where appropriate, may be delayed for a few microseconds, output from the computer and input to it can be combined in a single IOX operation.

The design of the control module, with its 256-word 16 bit PROM holding N,A,R and the two auxiliary control bits, is similar to that of the Argus equivalent. A single data module is employed, connected to the 16-bit bidirectional data bus of the Nord-10. The mapping of the 24-bit CAMAC operations on the 16-bit computer IOX operations is achieved in the following ways:

- for control operations, the 4 bit status register returns Q,X and validation bits to the A register of the Nord.
- for write operations, a high-byte register may be loaded previously if more than 16 bits are required, and the main IOX operation writes the less significant data to W 1-16 and status to the A register.
- for read operations requiring more than 12 bits, the IOX operation loads the high byte and the status lines into the A register. A second IOX reads the less significant 16 data lines.
- for read operations using 12 or fewer bits, the IOX places R 1 to 12 plus the status bits in the A register.

These facilities can be seen to provide a complete interface with minimum numbers of IOX operations, and many dataway operations may be performed with a single IOX.

Interrupt handling is based on the SGL Encoder designed for the serial system. LAMs originating in the system crate generate SGL codes of 5 bits, which pass through a 32-word PROM to give 8-bit interrupt vector codes to the computer. Thus the interrupt handling required almost no

hardware development, as the SGL Encoder was already available.

The Nord-10 I/O bus signals at the external bus connectors are in balanced tri-state form, similar to the RS-422 standards employed on the D-ports of the serial highway. These are connected directly to the two single-width modules of the SCC-10. The connections are about 1m long, and even so care has had to be taken with the wiring. The most critical point is the interrupt system. The interrupt lines provided for the several levels must be driven in a wired-or fashion, and are in a high-impedance state when not being driven. Consequently the noise immunity of these lines is less than that of the other parts of the interface.

The total number of integrated circuits used in the two modules of the SCC-10 is 102 and this number, added to the 66 of the SGL Encoder, compares well with other designs of programmed I/O single-crate interface. Standard features of the system, such as the dataway service module in Station 1, the possible use of standard monitor units, the very simple protocol for access to the dataway and the possibilities for testing the parts of the system in several ways has made the design, commissioning and maintenance of the system very easy. The Nord 10 CAMAC system was developed in 1976-77 and put into full operational use in 1978.

Although in the ISR control system we do not require DMA at present, a prototype DMA system is under test in the Nord 10 system crate. This uses a micro-computer based auxiliary controller operating in conjunction with the SCC-10 to perform the DMA functions. The special module required to handle the DMA address and control signals is a slave unit which obeys standard CAMAC dataway commands, so that any mini-computer may emulate the final micro-computer via an auxiliary access port or even the SCC-10. An interesting feature of this approach

is that DMA block transfers could be performed over the serial highway, and even a sparse data scan could be performed without involving the control computer in all the individual tests. The DMA system is intended to be used for development work with high speed data links using X.25 protocol, and may never be applied to the ISR control system.

5. Conclusions

The CAMAC system crate described in the paper has been highly reliable and successful as a concept, from the hardware and software points of view. The ISR Division of CERN has been able to combine major control system extensions, involving the installation of over 50 crates on Serial Highways and the introduction of new control computers, with a significant rationalisation of the old equipment.

6. Acknowledgements

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7. References

1. C.Parker, P.Wolstenholme, "Some Implementations of Local Intelligence in CAMAC" Paper 7.3.b-3 at this Symposium.

