

- un sentier pour piétons a été aménagé; celui-ci passe derrière la guérite et fournit l'accès à tout moment au secteur Coopin / Interfon / dortoirs depuis l'intérieur du domaine
- un portail à serrure a été installé sur le chemin qui lie la route Bohr au secteur Coopin / Interfon / dortoirs pour permettre la protection de ce dernier
- désormais, le bus no 15 des TPG pourra accéder au terminus par la porte A à tout moment de la journée.

D'ici le printemps, il est prévu de mettre en marche les lecteurs de cartes prévus dans le projet d'amélioration de l'accès, dispositifs qui permettront de passer par la porte A en dehors des heures de présence du gardien (les cartes d'accès standard nécessaires seront mises à disposition des personnes autorisées le moment venu). Vous serez informé de la date de mise en opération en temps voulu.

En attendant, et à partir du lundi 16 janvier, les dispositions en vigueur à la porte A sont les suivantes :

- les portails seront ouverts et gardés, comme par le passé, de 7.00 à 9.00 h, de 11.30 à 14.00 h et de 16.30 à 18.30 h du lundi au vendredi
- contrairement aux restrictions du passé, les portails seront ouverts dans les *deux* sens
- en dehors des heures d'ouverture, il est conseillé aux utilisateurs de passer par la porte principale (B)
- le portail donnant accès au secteur Coopin / Interfon / dortoirs sera ouvert entre 7.00 et 19.00 h du lundi au vendredi. L'accès à pied est possible à tout moment en passant à côté de la guérite. Les occupants des dortoirs qui ont une voiture sont priés, en dehors des heures d'ouverture, de garer leur voiture sur le parking devant le bâtiment 4.

Groupe des Services généraux / DA
Tél. 3333

- a footpath has been laid, passing behind the guard hut and providing permanent access to the Coopin / Interfon / dormitory sector from inside the site
- a lockable gate has been installed on the road linking the Bohr Road to the Coopin / Interfon / dormitory sector, providing protection for this area
- henceforth, the 15 bus will be able to reach the terminus via gate A at all times of day.

It is planned to put the card readers, which form part of the access improvement project, into operation in the Spring. This will enable the use of gate A outside guarded hours (the necessary standard cards will be made available to authorized users in good time). You will be informed of the starting date well in advance.

In the meantime, and from Monday 16 January, arrangements at gate A are the following :

- the gates will be open and guarded, as in the past, from 7.00 to 9.00 hrs, from 11.30 to 14.00 hrs and from 16.30 to 18.30 hrs Monday to Friday
- in contrast to past restrictions, the gates will be open in *both* directions
- outside opening hours, users are advised that they should use the main gate (B)
- the gate giving access to the Coopin / Interfon / dormitory sector will be open from 7.00 to 19.00 hrs Monday to Friday. Access on foot is possible at any time alongside the guard hut. Dormitory occupants who have a car are asked to park their cars outside opening times on the car-park opposite building 4.

General Services Group / DA
Tel. 3333

SEMINARS SEMINAIRES

Monday 23 January

PRESENTATION

09.00 to 12.00 hrs and 14.00 to 15.00 hrs

Presentation : DD Auditorium, bldg 31, 3-005

Demonstration : DD Conf. Room, bldg 600, R-017

CADRE / MicroCASE seminar

by Pierre SCHMIT & Markus WACHSMUTH /
CADRE Technologies Europe &

Achilles STAMATIADES / MicroCASE Europe

Teamwork from CADRE is a software development system which can be tailored to the needs of programmers developing software for real-time

microprocessor environments. The Software Analysis Workstation (SAW) from MicroCASE enables programmers to monitor the real-time execution of their code in a non-intrusive manner. The combined Teamwork and Software Analysis Workstation environment is named Unified CASE and it enables full system lifecycle support from requirements specification through to testing and maintenance. Representatives of CADRE and MicroCASE will present their products and discuss how they may be integrated into the CERN environment. The seminar will be split into two parts, a presentation of the products in the morning, followed by demonstrations in the afternoon.

- 09.00 Graphical methods for object orientated design
- 10.00 Hardware and software simulation
- 10.30 Code generation for ADA and C
- 11.00 Unified CASE for embedded systems
- 14.00 Demonstration of Teamwork
- 15.00 Demonstration of Software Analysis Workstation

Information : J. Caves / DD / 3511 / JON@PRIAM

Wednesday 25 January

DEC SYSTEM MANAGERS' MEETING

at 10.00 hrs – DD Auditorium
bldg 31, 3-005

Wednesday 25 January

TECHNICAL PRESENTATION

14.00 to 16.00 hrs – PS Auditorium
bldg 6, 2-024

High speed ASIC Seminar

by Matthias VOIGT / NEC Germany

NEC Electronic Components (J/D), represented by Memotec AG (CH), will present its high speed ASIC-Components in ECL, BI-CMOS and CMOS technology. Professional design possibilities are given by a broad CAE-support, e.g. Daisy, Mentor, HP, Valid as well as the well-equipped design centre of Memotec.

Languages : English (+ French & German
for questions)

Information : M. Diraison / FI / 4585

Wednesday 25 January

THEORETICAL SEMINAR

at 14.00 hrs – TH Conference Room

Signals for new and old physics in $p\bar{p}$ collisions

by D. ZEPPEFELD / Madison

In addition to squark and gluino production there are other potential sources for p_{T-miss} events at the Sp $\bar{p}$ S and Tevatron colliders : leptoquarks, leptogluons and cosmion models are elaborated on. Among possible backgrounds emphasis is put on W or Z events with associated QCD jet(s). Expected background rates are also compared to possible WW, WZ and ZZ signals.

Wednesday 25 January

COMPUTER SEMINAR

at 16.00 hrs – Auditorium*

The design of the Berkeley RISC II processor

by Manolis KATEVENIS / Computer Science
Institute, FORTH, Crete

The Reduced Instruction Set Computer (RISC) project at UC Berkeley (1980-83) investigated the implications of simplifying the instruction set of a general-purpose computer. For a VLSI implementation, such an approach makes effective use of the limited on-chip silicon resources by devoting them to those tasks which are used most frequently. In this talk, after a brief review of the general RISC ideas, we discuss the micro-architecture of RISC II, the second NMOS implementation of the Berkeley RISC architecture (very similar to the Sun 'SPARC' architecture). The RISC II chip was designed with the goal of attaining the highest performance in a register-to-register architecture, using a three-stage pipeline. We discuss the pipeline, the datapath and the timing, and we present the organization of the control section, showing how its area was drastically reduced owing to the simple instruction set. Design metrics of RISC II are given.

Manolis Katevenis received the Diploma degree in Electrical Engineering from the National Technical University of Athens, Greece, in 1978, and the MSc and PhD degrees in Electrical Engineering and Computer Science from the University of California, Berkeley, in 1980 and 1983, respectively. From January 1984 to March 1985 he was Assistant Professor of Computer Science at Stanford University, Stanford, California. Since September 1985 he has been Assistant Professor of Computer Science at the University of Crete, Heraklio, Greece. From 1980-83, he worked on the design of the RISC II single-chip NMOS processor, at UC Berkeley. From 1984-85, he worked on Switch Design for Soft-Configurable Wafer-Scale Integrated Systems, in CSL and CIS, Stanford University. Since 1985, he has been working on Digital Switching Systems, Computer Workstation Architectures and Graphics Editors and Languages for CAD in the Computer Science Institute of FORTH, in Crete, Greece.

* Coffee and tea will be served at 15.30 hrs

Friday 27 January

PRESENTATION

10.00 to 12.00 hrs & 14.00 to 16.00 hrs
DD Auditorium, bldg 31, 3-005

Single Height VMEbus Products

by N. HAUSER / PEP Modular Computers, West
Germany

Single height VMEbus provides a cheaper alternative to the more usual dual-height VMEbus in systems where board space and performance can be traded for a reduction in cost. This approach, although necessarily limited to 16 data and 24 address lines, has full upward compatibility with 32-bit VMEbus with a smaller reduction in processing or input/output performance than may be imagined. PEP, who specialize in single

height VMEbus, will present their company and its product range, both hardware and software. The afternoon session will be devoted to practical demonstrations and informal discussions.

- 10.00 Introduction
- 10.10 VMEbus product range and future strategy
- 10.50 VMEbus CPUs (from 68000 to 68020 with 2Mbyte SRAM for $\ll$ 1000 SFr)
- 11.00 OS-9 and communication to networks and intelligent I/O
- 11.30 VIOXROM : the real-time multi-processing solution for intelligent I/O modules
- 12.00 Lunch
- 14.00 Demonstrations and informal discussions (bldg 600, Conference Room no. 2)

Language : English

Information : C. Parkman / DD / 3963
PMN@CERNVM

Friday 27 January

ELECTRONICS SEMINAR

at 14.00 hrs – TH Conference Room

Custom VLSI development and data acquisition system for VENUS

by Y. ARAI / KEK, Japan

Tuesday 31 January

SPS EXPERIMENTS COMMITTEE

at 09.00 hrs – Auditorium

Open session

1. Status report on WA82 (Charm hadroproduction; L. Rossi).
2. Status report on WA84 (Production and decay of beauty flavoured hadrons; G. Martellotti).
3. Investigation of the energy- and Angular dependence of ultrashort radiation lengths in Si, Ge and W single crystals (Aarhus - CERN - Strasbourg - Stuttgart collaboration; SPSC 88-36/P 234 Add 1 and 88-39/P 234 Add.2; E. Uggerhoj)
4. Darmstadt on Hunting in the interaction γ -crystal (Annecy - Lyon - Turin collaboration; SPSC 88-50/P 241 Add.1; D. Sillou)
5. Proposal for an emulsion-hybrid set-up for the study of sulphur-nucleus collisions at 200 GeV/N (Bari - CERN - Dublin - Huntsville (Univ. of Alabama and Marshall Space Flight Center) - London (Univ. College) - Nagoya - Rome - Salerno - Turin collaboration; SPSC 89-1/P 243; G. Romano).

6. Study of beauty physics at the SPS-collider with real-time use of silicon microvertex information (Los Angeles (Univ. of California) - Collège de France - Ferrara - Perugia - Saclay - Serpukhov - Turin collaboration; SPSC 88-33/P 238; P. Schlein).
7. Measurement of the spin-dependent structure functions of the neutron and proton (Amsterdam (NIKHEF - FOM and Free Univ.) - Bielefeld - CERN - Delft - Dubna - Freiburg - Houston - Los Angeles (Univ. of California) - Mons - Northeastern Univ. - Rice Univ. - Uppsala - Univ. of Virginia - Warsaw (Univ. and Inst. for Nuclear Studies) - Yale Univ. - Zurich (ETH) collaboration; SPSC 88-47/P 242; V.W. Hughes).
8. Search for low-mass short-lived particles decaying into electron-positron pairs (Grenoble - Orsay - Paris (LPNHE) - Saclay collaboration; SPSC 89-8/P 245; M. Davier).
9. Research and development program on a fast trigger system of heavy flavour tagging in fixed target and collider experiments (Catania - Pisa - Sassari collaboration; SPSC 89-5/P 244; S.R. Amendolia).

Closed session

Tuesday 31 January at 16.30 hrs

Conference Room, 6th floor, Main building

(to be continued on Wednesday 1 February at 09.00 hrs.)

Tuesday 31 January

PRESENTATION

at 10.00 hrs – TH Conference Room

The ORACLE Computer Aided Software Engineering (CASE) product

by Ian FISHER & Cliff LONGMAN / ORACLE, UK

Tuesday 31 January

CERN PARTICLE PHYSICS SEMINAR

at 16.30 hrs – Auditorium

A new intermediate range force ?

by Christof WETTERICH / DESY

EF SPRING SEMINARS 1989

EF Division is organizing a new series of seminars to take place this spring.

Preliminary programme :

20 January	The CDF online system	David R. QUARRIE / Fermilab
6 March	Gravity and other matters	John EADES / CERN-EF
13 March	R&D in silicon detectors and micro-electronics	Erik HEIJNE / CERN-EF
3 April	Use of an expert system for monitoring & control of the L3 experiment	Jean-Marie LE GOFF / CERN-EF
10 April	Fast RICH with VLSI electronics	François PIUZ / CERN-EF
17 April	The ALEPH TPC	John CONWAY / Univ. of Wisconsin
29 May	Design of a VLSI RISC processor for Fastbus	Sandro MARCHIORO / CERN-EF

Unless otherwise indicated, the seminars will take place on Mondays from 11.00 to 12.00 hrs in the EF Conference Room, bldg 13, 2-005.

SEMINAIRES EF DE PRINTEMPS 1989

Au printemps, la division EF organise une nouvelle série de séminaires.

Programme préliminaire :

Sauf avis contraire, les séminaires auront lieu le lundi de 11.00 à 12.00 h dans la Salle de Conférence EF, bât. 13, 2-005.

TRAINING AND *EDUCATION* *ENSEIGNEMENT*

ENSEIGNEMENT GENERAL
Tél. 2844-5811

Jeudi 26 janvier
de 13.00 h à 13.30 h – Auditorium
Science pour tous
par R. CARRERAS

ACADEMIC TRAINING
Tel. 2844-2460

25, 26 & 27 January
11.00 to 12.00 hrs – Auditorium
Calorimetry in high-energy physics
by R. WIGMANS / CERN-EF