# Scalable Readout System

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**Gaseous detector development group**

**RD51 Collaboration**

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# Introduction

This project is done in the RD51 collaboration at CERN, which is involved in the development of gaseous detectors technologies and read out electronics systems. Main focus of Gaseous Detector development Group (GDD) is on development of micropattern gaseous detectors and its readout electronics. To get the best output from detector and to match the high rate capability an efficient and up to date readout electronic system is required to process the current generated by detector into an analogue signal and later to an understandable data which would be used to understand physics of particles. To achieve this target, Scalable Readout System (SRS) is developed by RD51 collaboration.

# 1 Scalable Readout System (SRS)

Many different types of detectors are developed at CERN. Ranging from gaseous detectors to semiconductor detectors, based on the applications, different types of detectors with different specifications are built to achieve different targets. The detection mechanism of these detectors is similar. Charges are produced when a particle interacts with detector and these charges are collected using an electric field. The collected charges are then amplified and electrical signal is created. This electrical signal helps us to understand physics of particles. This basic detection mechanism is common to most of the detectors. The difference in the specifications and applications of detectors leads to the requirement of user specific readout electronic system for different detector. Most of the times the components used in readout electronics systems are not available commercially. All these factors make the instrumentation of readout electronics a costly and challenging task. SRS is a unique solution to this issue. Only front end of the electronics needs to be user specific, SRS provides a common back end electronics system which supports many different types of front ends. Prototype of SRS is shown in the Figure 1 below.

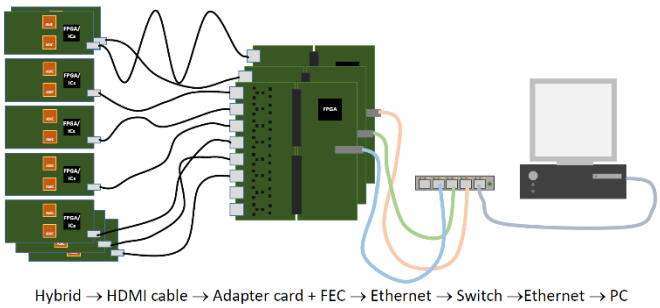



**Figure 1 schematic view of SRS**

## 1.1 Hybrid

Hybrid is the interface between detector and readout electronics. ASIC is implemented in hybrid. It also provides the inputs needed by the chip for example power, clock and slow control signals and transmits the data to adapter card. Figure 2 shows hybrid with two VMM3 ASICs installed in it. Spartan-6 FPGA card is used. Power and data connections can also be seen in the Figure 2 below.

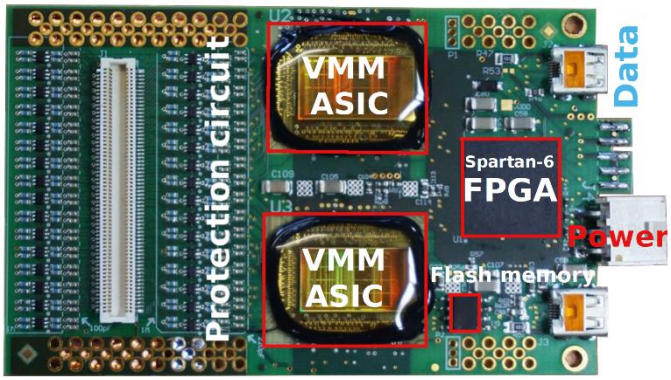



**Figure 2 Hybrid**

## 1.2 The Adapter Card

As the hybrid, the design of the adapter card is specific on the front end ASIC employed. By default, the connection to hybrid is provided by HDMI cables for most implementations. Depending on the type

of the front end technology (analogue, digital, pixel, ASIC), the components and the logic on the adapter card may vary significantly. The adapter card connects to the FEC via one or two PCI connectors depending on its size and specific implementation. Adapter card can be seen below in Figure 3.

## 1.3 The Front-End Concentrator Card (FEC)

As core of the back-end, the FEC provides communication with a computer by Gigabit Ethernet. The FEC card front-panel implements 2 x RJ45 for trigger and external clock, 2 x SFP as data links, 2 x LEMO-50 ohm trigger in- and outputs, 1 x differential multi purpose input and a nine way connector for power as can be seen in figure. Up to eight FECs can be housed in a 19-inch ATX-powered Eurocard chassis.

The FEC card holds power converters, flash memory, a slot for DDR3 memory card and a Virtex-6 FPGA. The firmware of the FEC is individual for different types of front ends. FEC card of SRS can be seen below in Figure 3.

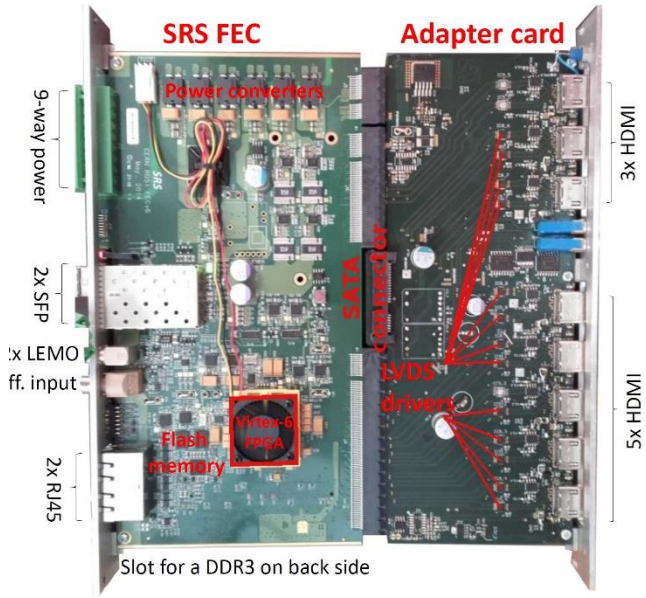



**Figure 3 Adapter and FEC card**

## 1.4 Slow Control Software

The Graphical user interface (GUI) of the current software version is shown in Figure 4 below.

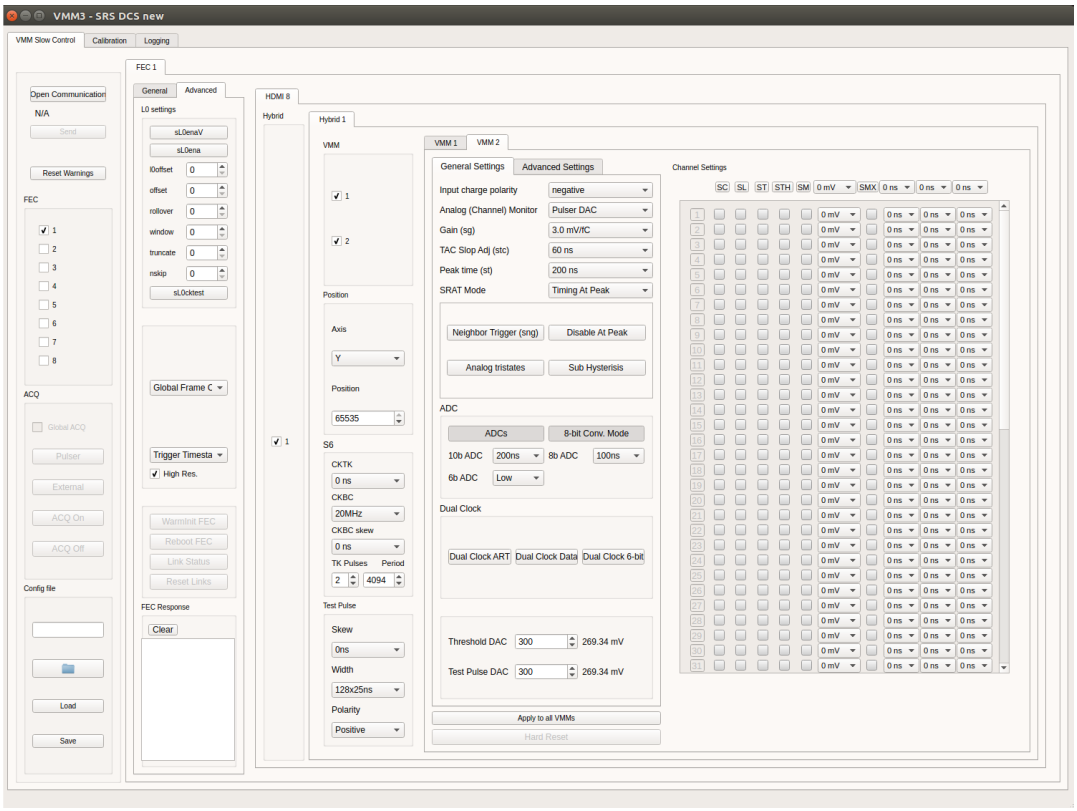



**Figure 4 slow control software**

The VMM slow control allows to modify the settings of the VMM chips, the Spartan 6 on the hybrid and the FEC. It also allows us to start and stop data acquisition. The format of the saved data is shown in Figure 5 below.

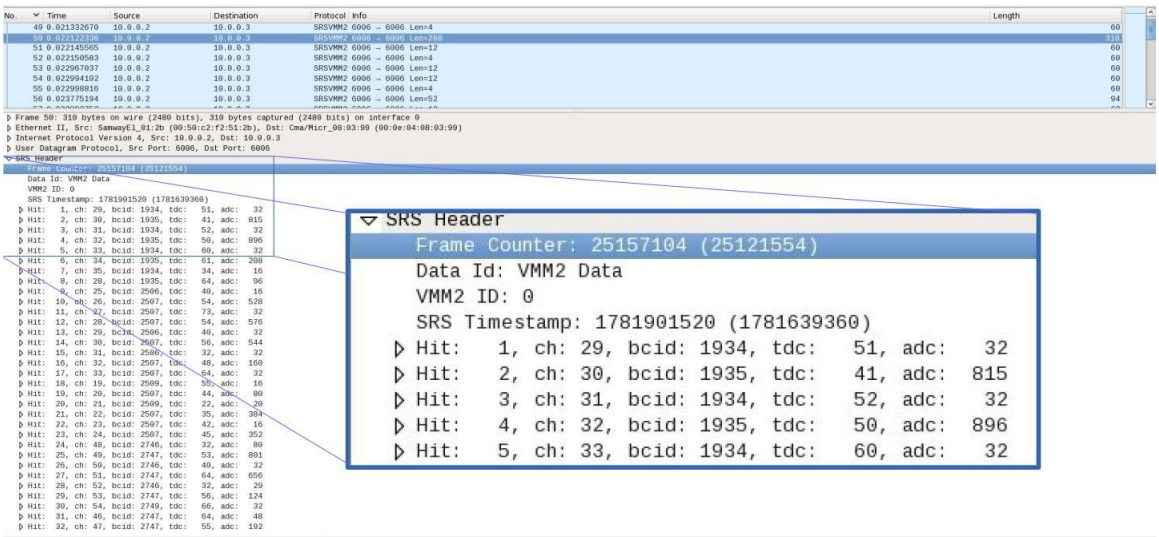



**Figure 5 Readout Data Format in Wireshark**

For each channel, the channel number, bcid , tdc and adc values are saved.

## 1.5 Experimental setup

The Figure 6 below shows the complete table top setup of a detector with SRS. Hybrids with VMM are connected to detector. Adapter card and FEC card are also connected to hybrid with HDMI cable. Power supply is provided through SRS crate. FEC card is connected to computer through ethernet cable. Computer has slow control software installed in it which is used for data acquisition and configure the readout electronics.

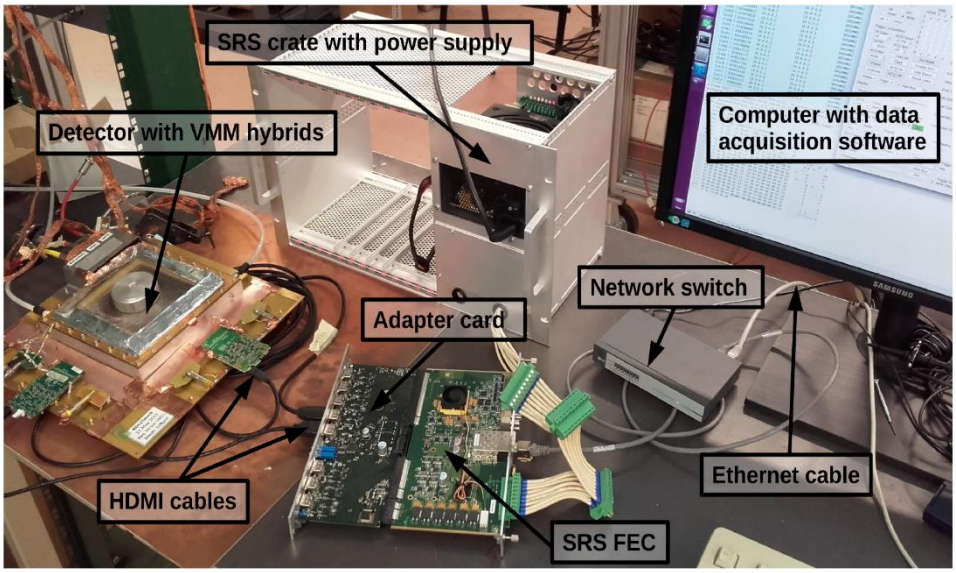



**Figure 6 Table Top Experimental Setup**

# 2 VMM ASIC

VMM was initially developed for the New Small Wheel upgrade of ATLAS experiment at the LHC by Brookhaven laboratory. The overall task of VMM is to filter and convert the analogue output from the detector into streams of digital data. Figure 7 below shows the architecture of the VMM3. Going from left to right, the incoming analogue signal from the corresponding detector anode strip is first amplified by a charge amplifier and then shaped and changed in width by a shaper. The width can be adjusted by choosing different peaking times. A discriminator compares the height of the signal to a given threshold. If the threshold is crossed, the peak amplitude and time are recorded using a peak and time detector. The threshold can be adjusted individually for each of the channels using the trimmer. The discriminator is also connected to a neighbouring logic. If neighbouring is enabled and a hit is recorded in one of the channels, the read-out of the two adjacent channels is forced as well, even if their threshold was not crossed. The peak detector saves the peak amplitude of the signal to analogue memory,

which is converted to a digital signal by a 10 bit analogue to digital converter (ADC). It is designed according to characteristics of detector. The timing and resolution requirements of VMM ASIC are according to the physics and trigger scheme of ATLAS experiment. Different versions of VMM are tested with different detectors. We used VMM3 and VMM3a in this project.

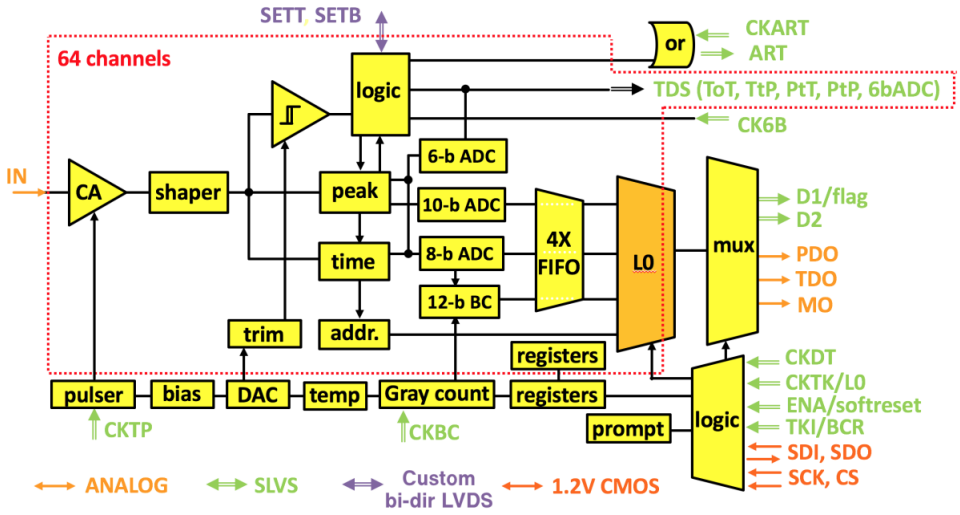



**Figure 7 Architecture of VMM3 ASIC**

The VMM ASIC is designed in 130nm technology and has 64 input channels, each with a preamplifier, shaper, a peak detector and several ADCs. The digitised data set of 38 bits per hit is multiplexed and can be read out on two lines double data rate with a clock frequency of up to 200MHz. The chip can be programmed via two digital lines (data and clock). As in the application in the New Small Wheel Upgrade (NSW), positive as well as negative charge will be detected, the analogue part is designed for both polarities. A detector capacitance between a few pF and 3nF can be adjusted and this allows VMM to be used with different types of detector designs such as pads, anode strips and wires. The input charge acceptance also ranges from 0.1pC to 2pC with a resolution smaller than 1fC rms. This also allows VMM to be used with a range of different detection systems. The chip is designed with low power consumption and can be programmed for a wide range of applications due to an adjustable gain, peaking time, polarity, threshold and timing precision.

It includes a dedicated test pulse circuit per channel and single-channel threshold trimming. Only the arrival time (time at the peak or time of threshold crossing) and 100 amplitude of the analogue input signal are measured, digitised and multiplexed with the number of the hit channel into a data stream. For triggering, the channel number of the firrst hit is provided with a minimal delay (address in real time, ART). Additionally for each channel, a direct and fast digital output signal can be generated, which can be the Time over Threshold (ToT), Time to Peak 105 (TtP), Peak to Threshold (PtT), Peak to Peak (PtP) or a 6-bit low-resolution ADC value of the amplitude with a conversion time of 25 ns.Figure below illustrates the treatment of an analogue signal over threshold in the VMM in case of a configuration to measure the arrival time at the peak position. To measure the amplitude, the Peak Detector Output (PDO) signal rises with the input pulse. When the peak is detected, PDO stays at this level and the amplitude is later digitised by a 10-bit ADC. For timing, a voltage ramp of the Time Detector Output (TDO) starts to increase linearly from the time of the peak until the next falling edge of a clock. The

same clock also increments a 12-bit counter, which serves as coarse timing. For the fine timing between clock cycles, the value of TDO is digitised by an 8-bit ADC. The VMM has an option to enable the readout of data from channels, for which the threshold has not been reached, but which are adjacent to a channel with a signal over threshold, a so called neighbouring logic. This way, shared 120 charge can still be detected, even though it is not enough to surpass the threshold. After the conversion time (in the order of 250 ns), the channel is reset and the data set (38-bit per hit) is latched onto a four hit deep buffer in continuous mode. Theoretically, the per channel hit rate can achieve up to 4 MHz, which however can be reduced by the return to baseline in the anlogue part of the ASIC. By using a token scheme, the data set is pushed out of the VMM on two data lines by another clock (CKDT).

The measurement of the time consists of two different values. The BCID is given by a counter which is increased at each tick of the CKBC clock. For the CKBC clock frequency values of 10, 20 or 40MHz are usually chosen. The resolution of the counter is 12 bit resulting in BCID values between 0 and 4095. The read-out frequency has to be adapted to the CKBC frequency in order to avoid overow of the BCID values. The time resolution given by the BCID depends on the CKBC clock frequency. The CKBC values given above correspond to a period of 100, 50 or 25ns between two BCIDs. In this Project we used the CKBC value of 40 MHz which corresponds of a period of 50ns between two BCIDs. In order to achieve higher precision time to amplitude converter (TAC) or time to digital converter (TDC) is used. We have a choice of either to start the TAC slope when the signal crosses the threshold or when the siganl reaches its peak. In this Project we chose to start the TAC (will be referred as TDC from now on) slope from the point when signal reaches at its peak. The voltage level at the end of the ramp is digitalised using an 8 bit ADC, resulting in TDC values between 0 and 255. The data is sent out in two simultaneous data streams to enable higher rates. The first bit of the DATA0 stream is an event flag that announced the incoming datastream. The second datastream begins with the over threshold bit, which indicates whether the event crossed the threshold or the read-out was forced through the neighbouring logic. The stream also contains the channel, time and amplitude information for the event corresponding to a total of 38 bits.

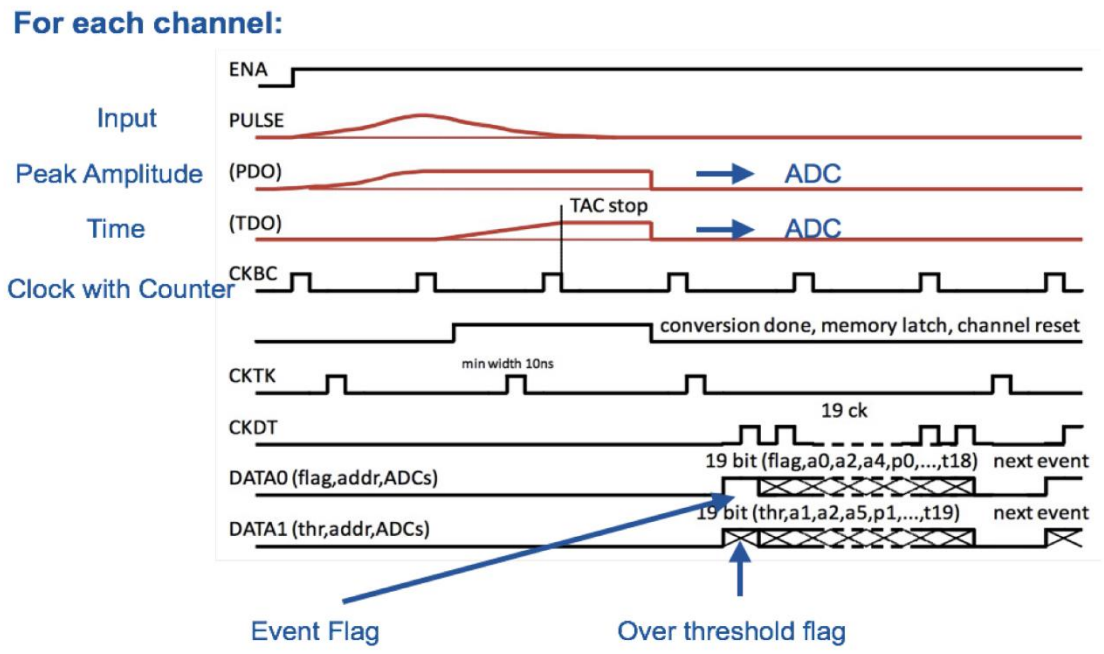
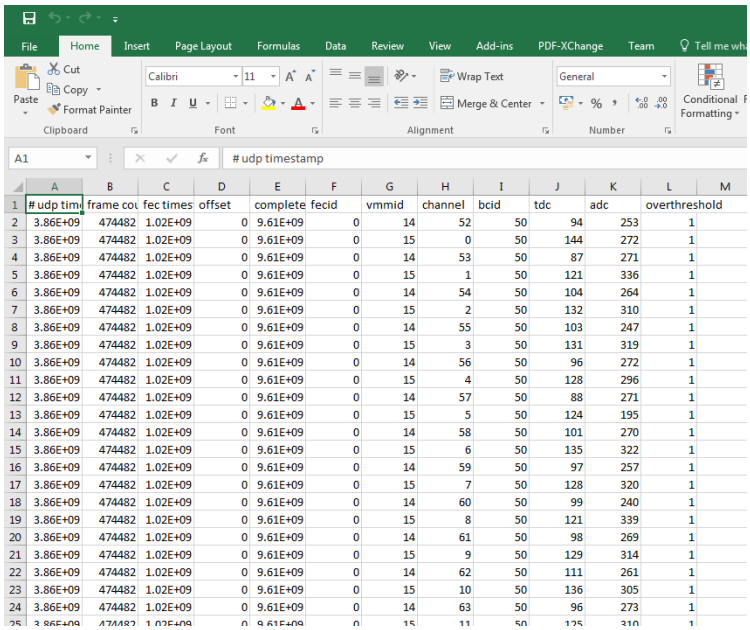



**Figure 8 Time Measurement**

For testing and calibration purposes, the VMM3 also contains a pulser which sends test pulses to the channels at given intervals. For data acquisition the VMM3 provides two different modes, a continuous and an external trigger based mode. While in the continuous mode, data is read out in a given interval of time, in the external trigger mode, read-out occurs only after a signal from an external trigger detector [VMM]. The datastream from the VMM3 hybrid is sent out to the next step of the read-out chain, the scalable read-out system (SRS). The SRS perform further processing, adds an additional SRS timestamp for each read-out period and sends the data to a computer in UDP packages. The data from the UDP packages is then written into .csv files, the format of which is shown in Figure 9 below.



| # udp time | frame co | fec times | offset | complete | fecid | vmmid | channel | bcid | tdc | adc | overthreshold |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 3.86E+09 | 474482 | 1.02E+09 | 0 | 9.61E+09 | 0 | 14 | 52 | 50 | 94 | 253 | 1 |
| 3.86E+09 | 474482 | 1.02E+09 | 0 | 9.61E+09 | 0 | 15 | 0 | 50 | 144 | 272 | 1 |
| 3.86E+09 | 474482 | 1.02E+09 | 0 | 9.61E+09 | 0 | 14 | 53 | 50 | 87 | 271 | 1 |
| 3.86E+09 | 474482 | 1.02E+09 | 0 | 9.61E+09 | 0 | 15 | 1 | 50 | 121 | 336 | 1 |
| 3.86E+09 | 474482 | 1.02E+09 | 0 | 9.61E+09 | 0 | 14 | 54 | 50 | 104 | 264 | 1 |
| 3.86E+09 | 474482 | 1.02E+09 | 0 | 9.61E+09 | 0 | 15 | 2 | 50 | 132 | 310 | 1 |
| 3.86E+09 | 474482 | 1.02E+09 | 0 | 9.61E+09 | 0 | 14 | 55 | 50 | 103 | 247 | 1 |
| 3.86E+09 | 474482 | 1.02E+09 | 0 | 9.61E+09 | 0 | 15 | 3 | 50 | 131 | 319 | 1 |
| 3.86E+09 | 474482 | 1.02E+09 | 0 | 9.61E+09 | 0 | 14 | 56 | 50 | 96 | 272 | 1 |
| 3.86E+09 | 474482 | 1.02E+09 | 0 | 9.61E+09 | 0 | 15 | 4 | 50 | 128 | 296 | 1 |
| 3.86E+09 | 474482 | 1.02E+09 | 0 | 9.61E+09 | 0 | 14 | 57 | 50 | 88 | 271 | 1 |
| 3.86E+09 | 474482 | 1.02E+09 | 0 | 9.61E+09 | 0 | 15 | 5 | 50 | 124 | 195 | 1 |
| 3.86E+09 | 474482 | 1.02E+09 | 0 | 9.61E+09 | 0 | 14 | 58 | 50 | 101 | 270 | 1 |
| 3.86E+09 | 474482 | 1.02E+09 | 0 | 9.61E+09 | 0 | 15 | 6 | 50 | 135 | 322 | 1 |
| 3.86E+09 | 474482 | 1.02E+09 | 0 | 9.61E+09 | 0 | 14 | 59 | 50 | 97 | 257 | 1 |
| 3.86E+09 | 474482 | 1.02E+09 | 0 | 9.61E+09 | 0 | 15 | 7 | 50 | 128 | 320 | 1 |
| 3.86E+09 | 474482 | 1.02E+09 | 0 | 9.61E+09 | 0 | 14 | 60 | 50 | 99 | 240 | 1 |
| 3.86E+09 | 474482 | 1.02E+09 | 0 | 9.61E+09 | 0 | 15 | 8 | 50 | 121 | 339 | 1 |
| 3.86E+09 | 474482 | 1.02E+09 | 0 | 9.61E+09 | 0 | 14 | 61 | 50 | 98 | 269 | 1 |
| 3.86E+09 | 474482 | 1.02E+09 | 0 | 9.61E+09 | 0 | 15 | 9 | 50 | 129 | 314 | 1 |
| 3.86E+09 | 474482 | 1.02E+09 | 0 | 9.61E+09 | 0 | 14 | 62 | 50 | 111 | 261 | 1 |
| 3.86E+09 | 474482 | 1.02E+09 | 0 | 9.61E+09 | 0 | 15 | 10 | 50 | 136 | 305 | 1 |
| 3.86E+09 | 474482 | 1.02E+09 | 0 | 9.61E+09 | 0 | 14 | 63 | 50 | 96 | 273 | 1 |

**Figure 9 Readout Data in .csv Format**

The incoming UDP packages are monitored using a designated wireshark plugin. This shows the number of hits as well as all the information associated with them. The wireshark tool is mainly used for short tests of the using test pulses in the lab or during setup at the test beam.

# 3 TDC CALIBRATION

As mentioned above, when the signal reaches the peak value, a Bunch Crossing id (BCID) is assigned to it. The clock running has a frequency of 20MHz which means after each 50ns a new BCID is assigned to incoming signal.

The issue that prevents us from getting the best time resolution is that the clock is not synchronized with the incoming signal. So the signals that comes between the two 50ns BCIDs has to wait until the brunch crossing id is assigned to it. This wait is called input delay. When the peak of the signal is reached and if it is not synchronized with the BCID clock, then a slope starts to rise and it keeps rising until the falling edge of next BCID is reached. The amplitude of that slope is then saved, as

mentioned above, as TDC value. This value tells us how much the input delay is. Figure below shows the procedure.

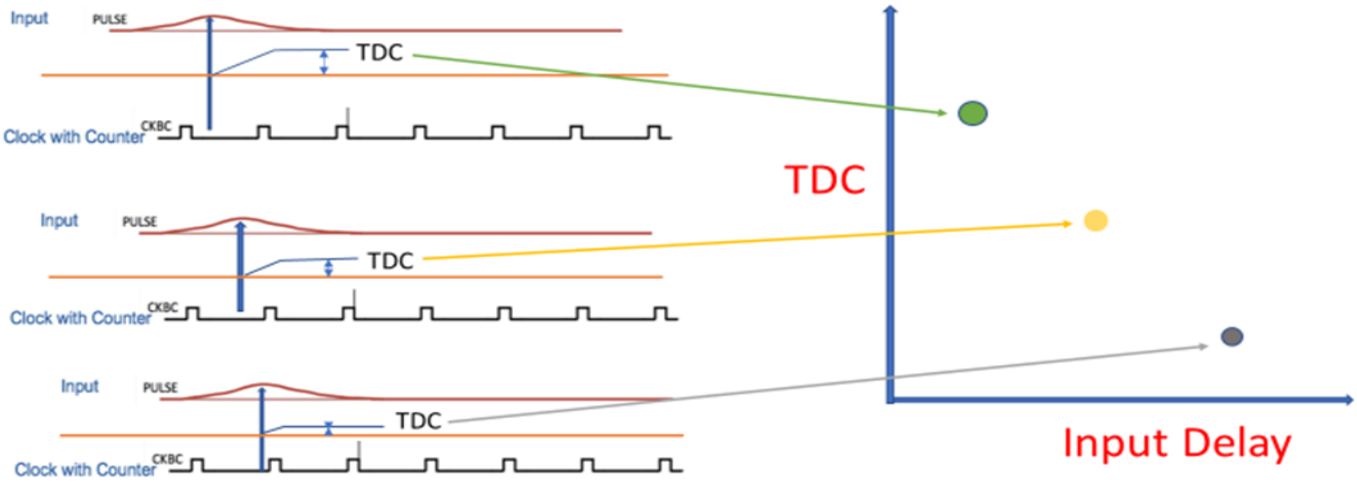


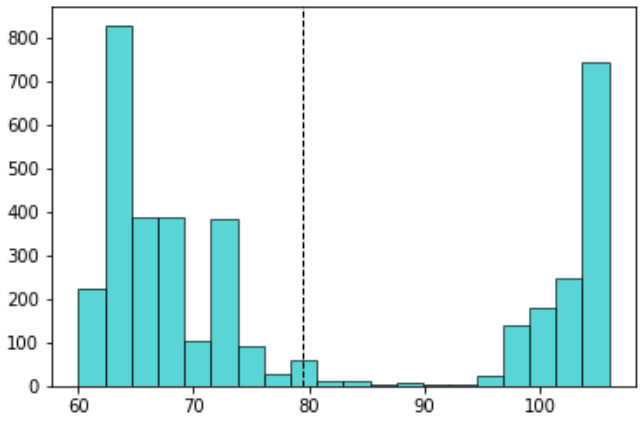

**Figure 10 Input Delay**

Each channel has different values for TDC and baseline is also different for every channel. This is a huge barrier in getting a good time resolution and we need to calibrate it. ATLAS group at CERN has calibrated the TDC values for each channel and has reported much better time resolution. To achieve the same target we decided to calibrate TDC values and to implement automated TDC calibration in our slow control software.

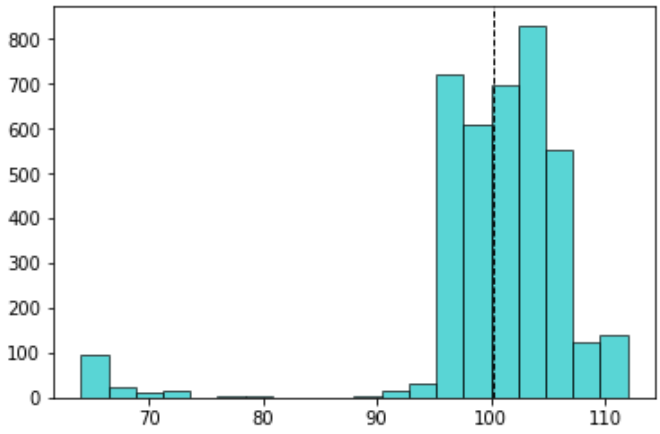
To analyze the values of TDC for the different intervals between 0 and 50ns we did some data analysis. We took the values with the interval of 3.125ns and we expected TDC value to decrease linearly from 0 to 50ns.

We started with drawing the histograms of TDC values of each channel for each time interval to see what are the mean TDC values we have for every channel and how are the TDC values distributed for each channel. Some results are shown below.

Time : 0ns channel : 1
Mean = 79.4486584107




Time : 0ns  channel : 2
Mean = 100.244066047




Time : 0ns  channel : 2
Mean = 90.9969040248

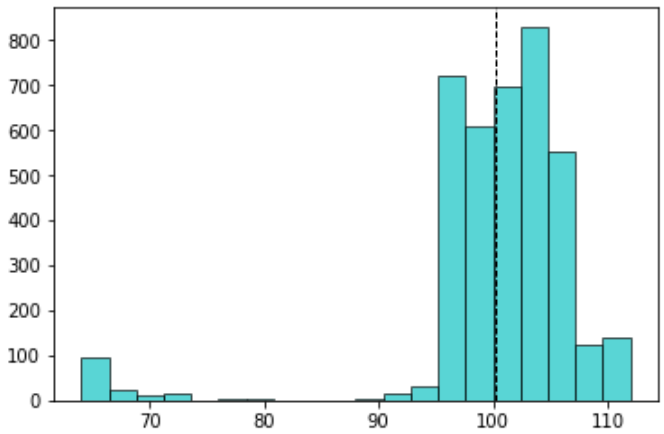



**Figure 11 Histograms of TDC Value Distribution**

We then plotted the TDC values of each channel for all 16 time intervals between two BCID values. Base line and slope of each channel is different then others. These two corrections need to be implemented and data should be calibrated. The Figure 12 shown below has only baseline correction implemented not the slope correction.

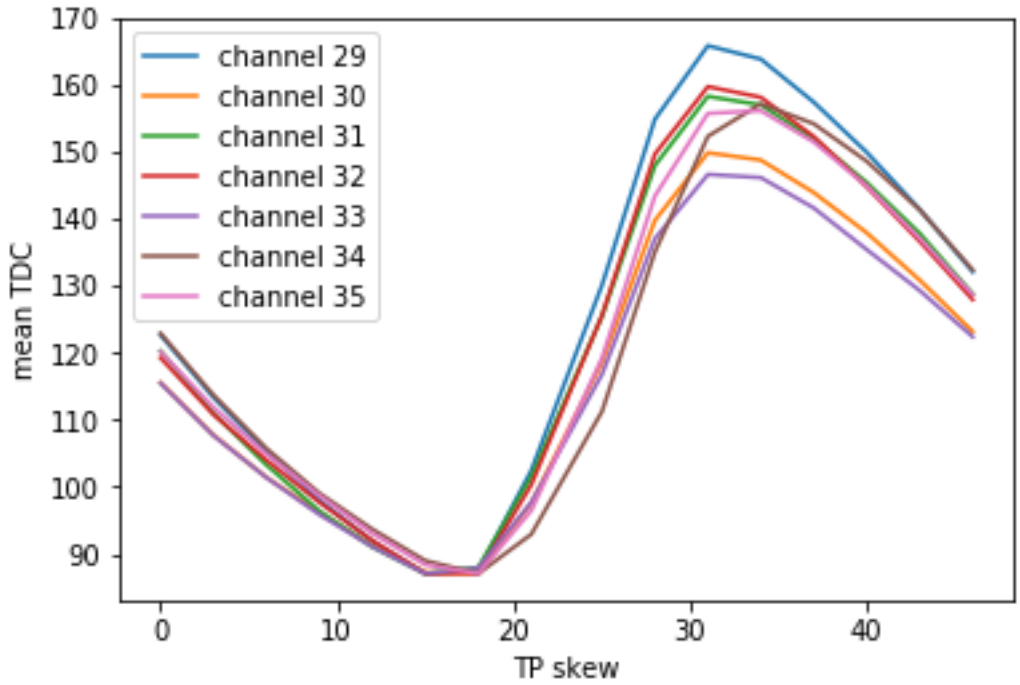



**Figure 12 Mean TDC value with Both BCID mixed**

As mentioned before we expected the mean TDC values to drop linearly from 0 to 50ns but in our plots we see a linear decline first but a sharp rise then decline again. This part kept us confused for several days but then we found out that mistake we are making is that we are mixing data from two different BCID values and this causes the mean values to increase sharply at points where number of data points from one BCID is greater then the other.

We decided to seperate the data from different BCID values and plot the results.The plot we obtained are shown in Figure 13 below. The mean TDC values fall linearly but then there are some discrepencies at some points. It was found out that number of data points at those points are not enough. If we set a threshold to only plot the points where the data is enough we get a plot like shown in Figure 14 below.

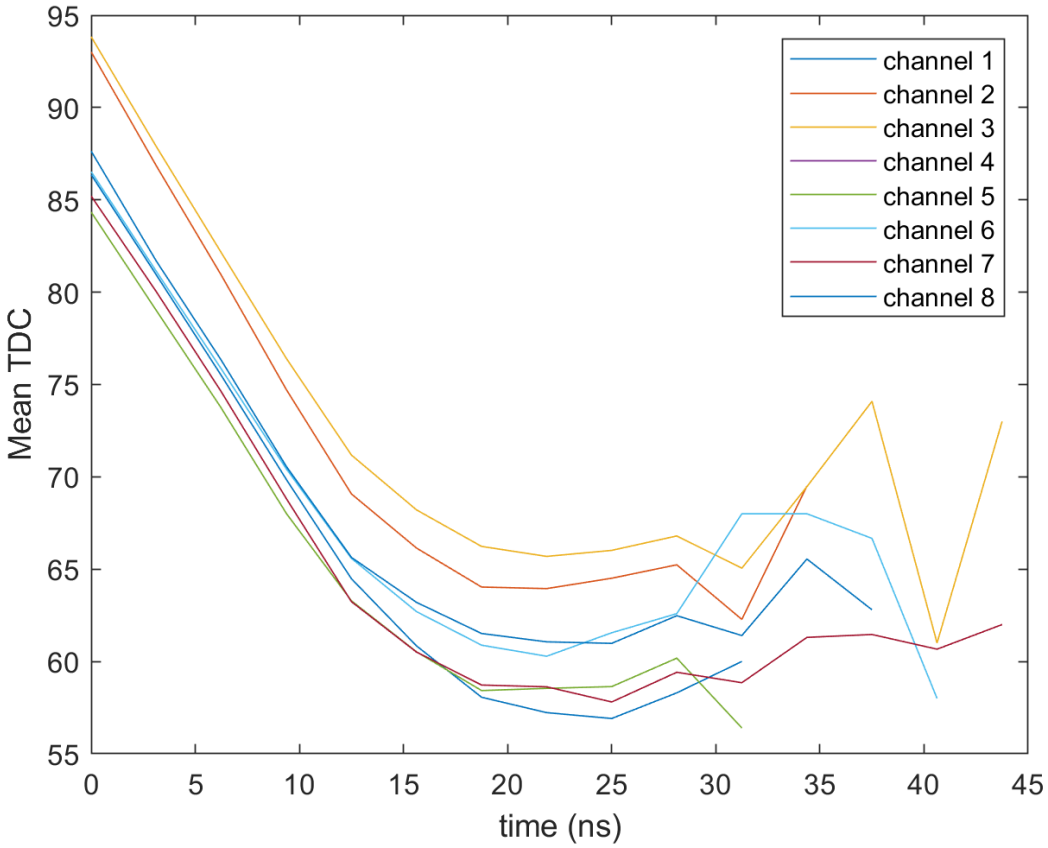



**Figure 13 Mean TDC value with values from only BCID : 50**

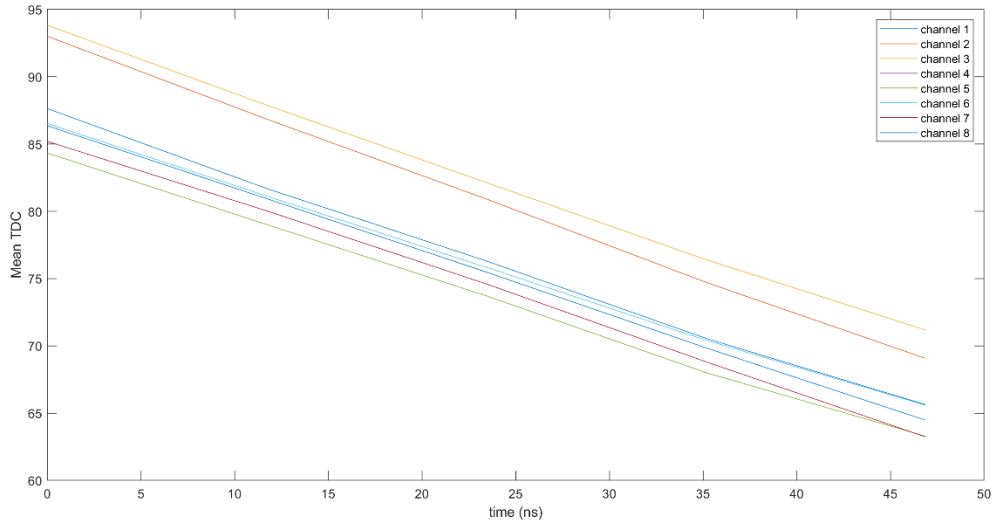



**Figure 14 Mean TDC value after points with less data removed**

# 4 RD51 Test Beam

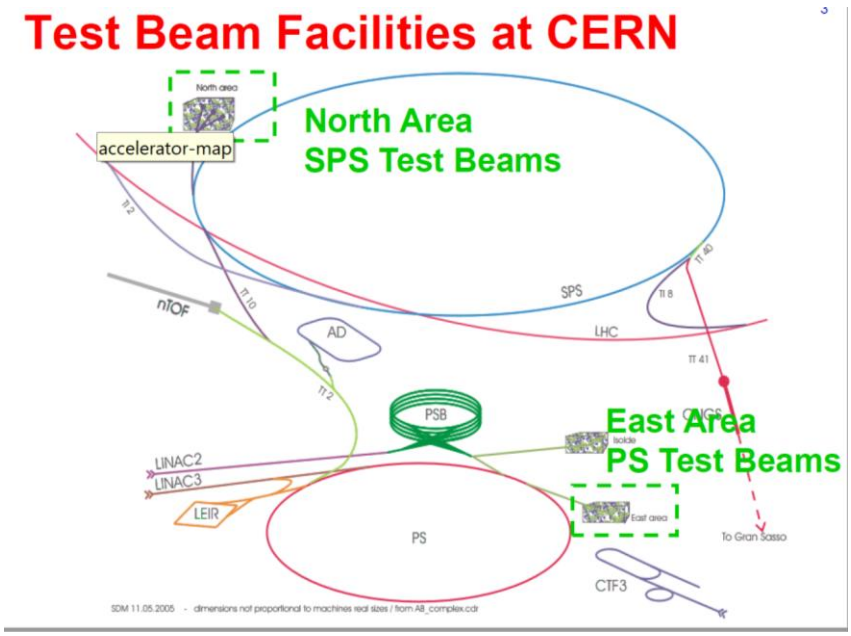



**Figure 15 Test Beam**

CERN has a unique set of experimental areas that can provide a wide spectrum of particle beams for FT experiments and R&D projects. The Super Proton Synchrotron (SPS) is the second-largest machine in CERN's accelerator complex. Measuring nearly 7 kilometres in circumference, it takes

particles from the Proton Synchrotron and accelerates them to provide beams for the Large Hadron Collider, the NA61/SHINE and NA62 experiments, the COMPASS experiment. It will also soon feed the AWAKE experiment which aims to test new techniques for accelerating particles. SPS Test Beams are also used by different groups for the test of different instruments and detectors. During my internship at CERN, I was very fortunate to be a part of such an amazing experience. RD51 collaboration used test beams to test the new devices that have been recently developed by RD51 collaborators.

The latest version of VMM ASIC, VMM3a, arrived in July 2018. To test the performance of VMM3a we used it in the test beam organized by RD51 collaboration at CERN. Before installing the detector in test beam area we tested it with radioactive soure (Fe) in the lab at CERN. The setup is shown in the Figure 16 below.

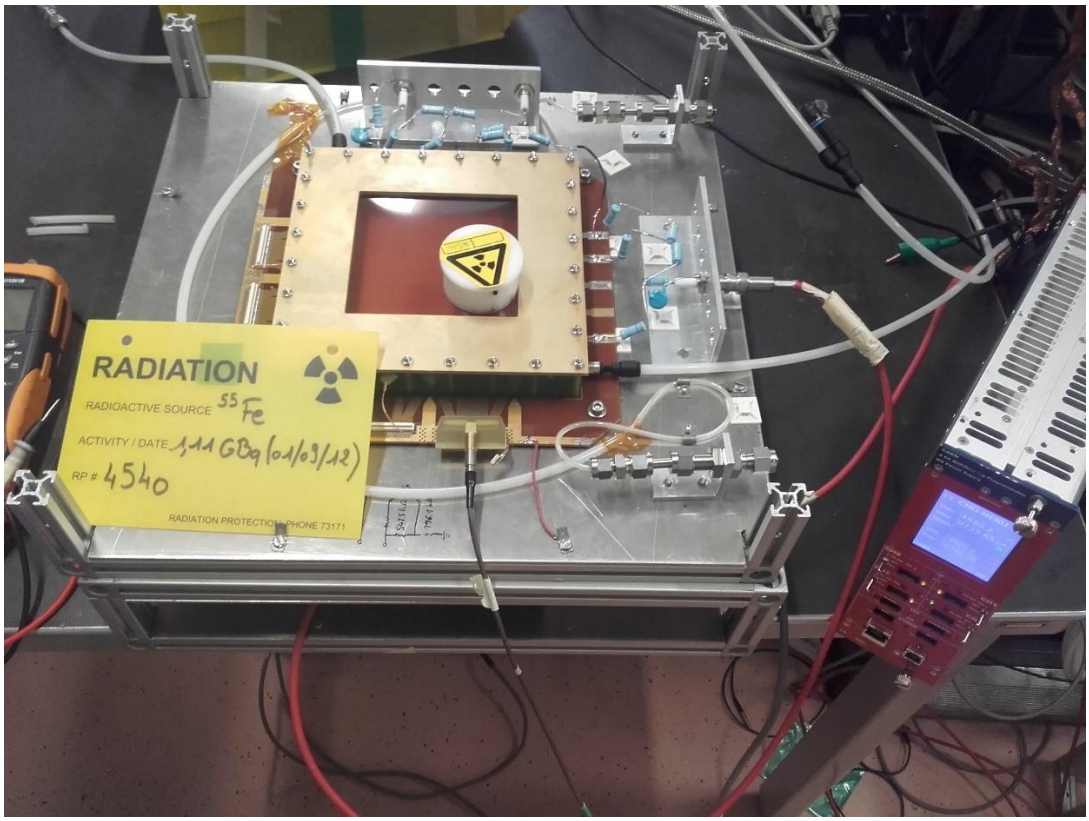



**Figure 16 Detector Test in GDD Lab with iron (Fe) source**

After successful test, we proceeded to the instalment of detector in test beam area where the detector was exposed to muon and pion test beams. Setup after instalment is shown in the Figure 17 below.

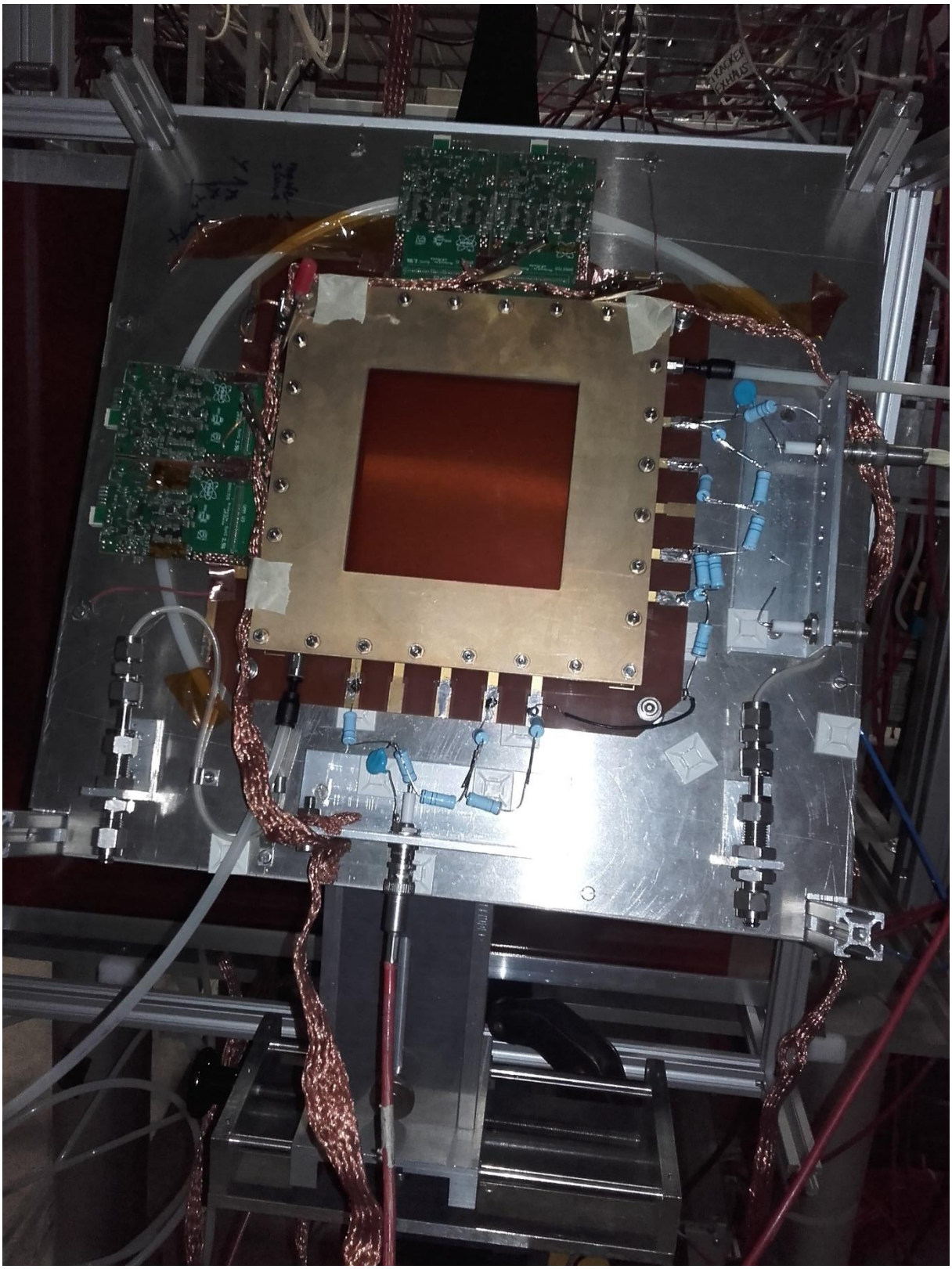


**Figure 17 Detector after installation in Test Beam Area**

As seen in the figure above, 4 hybrids are connected to standard GEM detector. Each hybrid has two VMM3a installed in it and each VMM3a has 64 channels. In total we have 8 VMM3a and 512 readout channels. Hybrids are connected to SRS through HDMI cables and this setup is shown in the Figure 18 below which shows the side view of the setup.

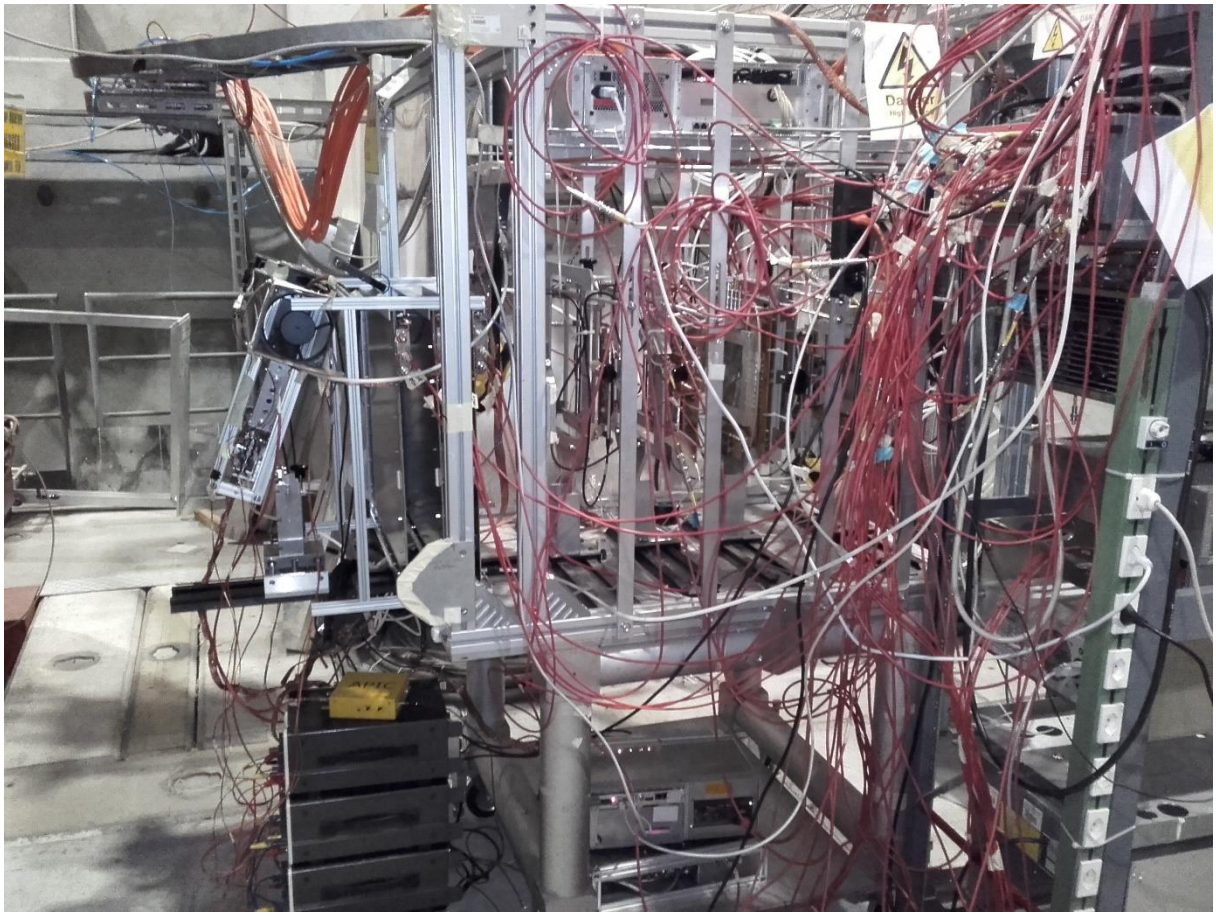


**Figure 18 Full setup of Detector after installation in Test Beam Area**

# References

S. Martoiu, Member, IEEE, H. Muller, and J. Toledo, “Front-end electronics for the Scalable Readout System of RD51”, 2011 IEEE Nuclear Science Symposium Conference Record N43-5.

M. Lupberger, L. Bartel, F. M. Brunbauer, M. Guth, S. Martoiu, H. Müller, E. Oliveri, D. Pfeiffer, L. Ropelewski, A. Rusu, P. Thuiner, “Implementation of the VMM ASIC in the Scalable Readout System”, Nuclear Instruments and Methods in Physics Research Section A, May 9, 2018.

Lara M. Bartels “Characterisation of the VMM3 Front-end read-out ASIC” Summer Student Project report 2017.

Manuel Guth, “Software Manual for VMM3 Slow Control”, Summer Student Project report 2017.