EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH
EP-CMD

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Testing of custom electronics modules – TCDS adapters for CMS experiment

CERN Summer Student Report

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Geneva 2018

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The Compact Muon Solenoid's Data Acquisition & Trigger (CMS DAQ & Trigger) system has shown a very good reliability. In order to maintain the very high degree of reliability of CMS detector and data taking - any new hardware have to be thoroughly tested and any detected failures understood and fixed before the new hardware is commissioned.

The aim of this project was to test TCDS adapters, which will be installed in CompactPCI crates 100 meters underground and are replacing old trigger and control infrastructure based on LEMO cables with a new infrastructure based on optical fibres (TCDS).

Introduction

My task was to create software solution, that allows to test all ports and buttons of the printed circuit board (PCB) and its logic (clocks and counters).

Project started with introductory exercises related to embedded systems. I used Altera Quartus software to generate hardware schematics and the code was written in C language, using Nios II Software Build Tools for Eclipse as an IDE.

I also had to solder some components, which were for some reason unmounted in an assembly company factory.

Solution was tested by me and my supervisor. Developed tests are uploaded into CERN GitLab website, where one can use them freely: https://gitlab.cern.ch/hardware/tcds_adapter/testbench1/.

Project consists of 141 lines of code written in C: https://pastebin.com/8bddR0p2, schematic done in Quartus (appendix 1), and software developed by my supervisor (test design 2).

Distribution of tests

In total I had to test 98 PCB-s. Testing was divided into two parts – firstly test design 1 and afterwards test design 2.
Test design 1 (firmware) is intended to test circuit board's electrical wellbeing. During the test I tested if 1.1V and 2.5V power arrays had respective values via Fluke multimeter, measured board's power consumption, tested if LED's are working and if PCI buses are operating like they should. For PCI bus testing my supervisor created mechanical bridge, so it would be possible to write some binary value into one bus (J5) and read that same value from another bus (J6).
From test design 1 only one circuit board failed the test. It had only 0.7V in 1.1V power array. Later it turned out, that problem is in 2 resistors that were not mounted in the assembly company. In addition, 5 boards were un-cutted, meaning that boards did not have that custom shape, but were still part of the larger plate.
For another board production factory also forgot to assemble one transistor near the LED (for that reason LED CONF_DONE did not light up). That missing transistor were mounted to the board by me. During the test design 1 I also placed onto every board a serial number sticker and saved that serial number into board's EEPROM.

Test design 2 (firmware) is intended to test SFP Transceiver ports, temperature sensor in RJ45 port and internal memory logic. Memory logic testing involved testing clocks and counters. From that test also only one failed and the failure was in SFP Transceiver port, which internal counter could not be resetted – it increased incredibly fast and bit rate at the same rate stayed 0 bit/s.

Lastly, I conducted a final board test with my supervisor in CompactPCI crate. Test embraced testing of random boards PCI bus without JTAG connection. It was intended to test pins, that were untested during test design 1 due to mechanical bridge. Namely, mechanical bridge purposefully did not connect all the pins in J5 bus to all the pins with J6 bus, because that may have caused a short circuit. Random selection did not discover any faulty PCB's.

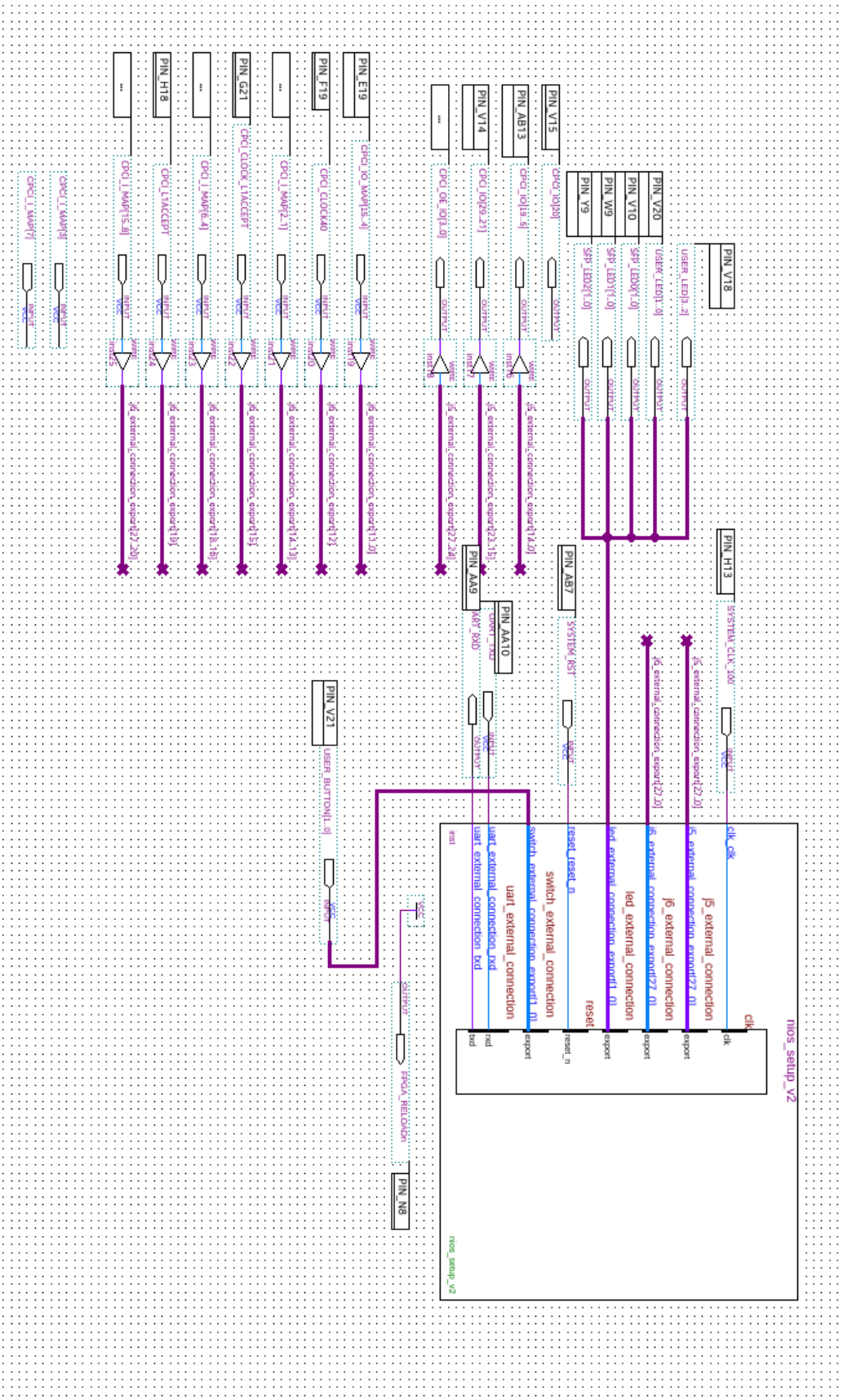
Conclusion

In total I had to test 98 PCB-s. From test design 1 only one PCB failed, from test design 2 also one PCB was faulty. Test 3 did not return any faulty boards.

Since it was my first hands-on experience with FPGA engineering and embedded systems, it was very enjoyable. For example, I got more aware of the definitions like Verilog and VHDL, which were unknown for him before this summer.

I am very grateful for that superior experience and is sure that the experiences he acquired during his stay in CERN will find use in yet unknown area in the future.

Appendix 1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reset_reset_n
switch_external_connection
uart_external_connection
led_external_connection
j6_external_connection
j5_external_connection
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PIN_AB7
PIN_AA9
PIN_AA10
PIN_V21
PIN_N8
PIN_V18
PIN_V20
PIN_V10
PIN_W9
PIN_Y9
PIN_V15
PIN_AB13
PIN_V14
PIN_H18
PIN_G21
PIN_F19
PIN_E19