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DISSERTATION

Silicon Sensor Process Quality Control for the CMS Phase-2 Upgrade

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KURZFASSUNG

Der Start des High Luminosity Large Hadron Colliders (HL-LHC) der Europäischen Organisation für Kernforschung (CERN) im Jahr 2027 wird eine neue Era für die Hochenergie-Teilchenphysik einläuten. Zur Vorbereitung auf die Herausforderungen, die mit der wesentlich erhöhten Luminosität einhergehen, werden die Physikexperimente am LHC zwischen 2025 und 2027 einem großangelegten Upgrade unterzogen.

Für das CMS (Compact Muon Solenoid) Experiment bedeutet das Upgrade unter anderem den vollständigen Tausch des Siliziumspurdetektors und der Kalorimeter-Endkappen. Zwischen 2020 und 2023 gehen deshalb mehr als $50\,000$ großflächige, positionssensitive Siliziumsensoren in Produktion und werden anschließend in den äußeren Spurdetektor und das neue High Granularity Calorimeter (HGCAL) eingebaut.

Die Sensoren unterliegen während des gesamten Produktionszeitraums einer genauen Qualitäts- und Stabilitätskontrolle. Die vorliegende Dissertation befasst sich mit der von CMS verfolgten Strategie der Prozessqualitätskontrolle. Die Überwachung kritischer Prozessparameter erfolgt mithilfe von Teststrukturen, die auf denselben Wafern gefertigt werden, wie die zu testenden Sensoren. Dadurch wird gewährleistet, dass Teststrukturen und Sensoren dieselben Eigenschaften aufweisen. Die Teststrukturen erlauben einen einfachen Zugang zu Prozessparametern, darunter auch solche Parameter, die auf den Sensoren nicht direkt bestimmbar sind (z.B. die Konzentration fixer Ladungsträger im Oxid oder die Rekombinationsgeschwindigkeit von Ladungsträgern an der Halbleiteroberfläche) sowie Parameter, die destruktive Messmethoden erfordern (z.B. die Durchbruchspannung des Oxids).

Den Kern dieser Arbeit bildet das Design eines Sets von Teststrukturen zur automatisierten Kontrolle aller relevanten Prozessparameter für die Serienproduktion von CMS Siliziumsensoren. Das Set ermöglicht die Erhebung der wichtigsten Prozessparameter in rund 30 Minuten pro Wafer und erlaubt eine tiefergehende Analyse im Fall von Problemen. Das Set ist auf automatisierte Messungen mit einer Nadelkarte zugeschnitten.

Für die Entwicklung des Sets wurden unterschiedlichste Teststrukturen, produziert von zwei verschiedenen Halbleiterherstellern, elektrisch vermessen und Simulationen durchgeführt. Dabei wurde ein besonderer Fokus darauf gelegt, im finalisierten Set mehrere verschiedene Teststrukturen anzubieten, um einzelne Prozessparameter zu extrahieren und so einander gegenseitig ergänzende Messansätze bereitzustellen.

Die ersten realen Instanzen des Sets auf Produktionswafern für den äußeren CMS Spurdetektor und Wafern mit HGCAL Prototypsensoren wurden einer systematischen Analyse unterzogen. Damit konnte die Funktionalität des Sets und aller enthaltenen Teststrukturen gezeigt werden. Diese Ergebnisse erlauben es, die Unterschiede der Produktionsprozesse für den äußeren CMS Spurdetektor und HGCAL zu quantifizieren. Zusätzlich geben die Messungen Aufschluss über Defizite des aktuellen Designs des Sets und bereiten die Grundlage für entsprechende Verbesserungsmaßnahmen.

Das Teststrukturset und die hier präsentierten Ergebnisse emöglichen die Standardisierung der CMS Prozessqualitätskontrolle. Die Vergleichbarkeit der Messungen zwischen den verschieden CMS Testzentren kann so über die gesamte Laufzeit der Produktion gesichert werden. Zusammen mit direkten Sensormessungen und Tests nach Bestrahlung, sichert die hier dargelegte Methode zur Prozessqualitätskontrolle die Qualität der Siliziumsensoren, die in den CMS Spurdetektor und HGCAL eingebaut werden und leistet letztendlich einen nicht unwesentlichen Beitrag für die künftige Suche nach neuer Physik am HL-LHC.

Abstract

The start of the High Luminosity Large Hadron Collider (HL-LHC) at the European Organization for Nuclear Research (CERN) scheduled for 2027 will herald a new era for high energy particle physics. The physics experiments located at the LHC will undergo a major upgrade between 2025 and 2027 to ready for the challenging conditions of the new high luminosity environment.

As part of this upgrade, the CMS (Compact Muon Solenoid) experiment will see the complete replacement of the full silicon tracker and the calorimeter endcaps. Over $50\,000$ large-area, position-sensitive silicon sensors will be produced between 2020 and 2023 to be integrated into the CMS Outer Tracker and the new High Granularity Calorimeter (HGCAL).

This thesis presents the CMS strategy to monitor the quality and stability of the sensor manufacturing process throughout production time. The process quality control procedure relies on tracking critical process parameters on test structures. The structures are manufactured on the same wafers as the sensors and, hence, share the same properties. They provide easy access to many process parameters, including parameters that are not directly accessible on sensors (e.g. oxide charge concentration and surface generation velocity) and parameters that require destructive measurements (e.g. dielectric breakdown voltage).

The main part of this thesis establishes a set of test structures designed to allow automated assessment of a comprehensive set of process parameters. This test structure set constitutes the basis of CMS silicon sensor process quality control. It facilitates quick assessment of critical process parameters in about 30 minutes per wafer and provides the means for in-depth analysis in case of any irregularities detected. Measurements of the set utilize a 20-needle probe card and an automated positioning stage.

The development process of the test structure set combined electrical measurements on individual test structures manufactured on prototype wafers by two different foundries and simulations of test structure response to the variation of different process parameters. Specific emphasis was put on investigating the capability of different test structures to access the same process parameters, aiming at providing complementary measurement methods within the finalized set.

Measurements of the first instances of the set produced on CMS Outer Tracker production wafers and HGCAL prototype wafers have demonstrated the functionality of the set and the included test structures. The results serve to quantify process related differences of the wafer material for the CMS Outer Tracker and HGCAL. Based on these measurements, the shortcomings of the current design of the test structure set are identified and mitigation measures are proposed.

The test structure set and the results presented in this thesis have served to standardize the process quality control procedure and to ensure cross-comparability between different test centers within the CMS silicon sensor working groups and over the full series production time. Together with direct electrical measurements of the manufactured sensors and irradiation tests, the presented process quality control procedure will ensure the quality of the silicon sensors integrated into the CMS Outer Tracker and HGCAL and, ultimately, will aid the search for new physics at the HL-LHC.

Acknowledgements

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This work has benefited from the collaborative environment within the silicon sensor working groups of the CMS Outer Tracker and HGCAL. I would like to pay my special regards to Dr. Francesco Moscatelli for sharing his immensely valuable expertise on semiconductor test structures, for many insightful discussions on test structure properties, design considerations, and measurement techniques, and for contributing measurement results of the PQC test structure set. To Dr. Andrei Korotkov, I would like to express my gratitude for his many helpful insights into measurement techniques and automation and for his dedication in contributing measurement results of the test structure set. I wish to thank Dr. Arianna Morozzi for her valuable input on simulations. Furthermore, I am indebted to Jan-Ole Müller-Gosewisch for providing data of resistance measurements on diodes. Lastly, I sincerely wish to show my appreciation to every member of the working group who participated in meetings, workshops, and offline discussions, who asked valuable questions and shared suggestions. Their contributions to the success of this project are greatly appreciated.

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Zuletzt möchte ich meiner gesamten Familie und allen Freundinnen und Freunden, die mich immer bedingungslos unterstützt haben, herzlichst danke sagen. Ohne euch wäre ich nicht hier!

Mama, Papa, Isabella ... ich kann gar nicht sagen, wie unglaublich dankbar ich bin. Für euer Vertrauen, eure Liebe und all eure Unterstützung. Ich kann das unmöglich aufwiegen.

Von ganzem Herzen ... Danke!

Contents

Chapter 1

Introduction

Before beginning a Hunt, it is wise to ask someone what you are looking for before you begin looking for it.

A. A. Milne, Winnie-the-Pooh

A hunt begins with a question. Only, when we have a question, we may know how to go looking for the answer. Science – physics, in this case – follows the same path. And, thankfully, there is no shortage of questions.

Particle physics has been asking a number of very ambitious questions. What are the fundamental constituents of matter? Which forces hold them together? And how to describe the underlying mechanisms?

Throughout the twentieth century, the hunt for answers to these questions (and a generous amount of new questions arising with it) has been a remarkable success story. Starting with the discovery of the *electron* by J.J. Thomson in 1897 [1] and E. Rutherford's famous scattering experiment in 1909, which led to the discovery of the atomic nucleus and the *proton* [2], and spanning the discovery of the *neutron* by J. Chadwick in 1932 [3] and the infamous era of an ever growing particle zoo during the middle of the last century, our current understanding of particle physics culminated in the formulation of the *Standard Model of particle physics* in the 1970s. Finally, with the experimental discovery of a *Higgs boson* at the Large Hadron Collider (LHC) experiments ATLAS and CMS at CERN in 2012 [4, 5], all fundamental components of the Standard Model have been verified.

The Standard Model currently stands as the best answer to the above mentioned questions and continues to prove remarkably accurate in its predictions of experimental quantities such as Higgs couplings to Standard Model particles and rare decays [6]. It describes normal matter as composed of twelve fundamental *fermions* (i.e. particles with half-integer spin that obey Fermi-Dirac statistics): six *leptons* and six *quarks*. Both types are grouped into three families, or generations, with increasing mass. A lepton family is made up of a negatively charged lepton and the corresponding neutrino. The three fundamental leptons are the electron, the muon, and the tau. The quarks are named up, down, charm, strange, top, and bottom (historically, top and bottom have also been denoted as truth and beauty) and are grouped in families containing an up- and a down-type quark each. All stable matter is made up of quarks and leptons of the lightest family; protons and neutrons consist of up and down quarks, and, together with electrons, they form atoms.

In addition to the fundamental fermions that constitute matter, the Standard Model describes three *fundamental forces* and the corresponding mediator particles, called *gauge bosons*. Bosons are particles with integer spin that obey Bose-Einstein statistics. The massless *photon* mediates the *electromagnetic interaction*, a force with infinite range that causes phenomena such as the binding of electrons to atomic nuclei and intermolecular forces in liquids and solids. Eight massless *gluons* mediate the *strong interaction*, the short-range force that holds together atomic nuclei and confines quarks inside protons and neutrons. Lastly, three massive bosons (W^-, W^+, and Z^0) mediate the *weak interaction*, a short-range force responsible for, e.g., radioactive decays. The forth fundamental force, *gravitation*, is not included in the

Standard Model of particle physics. Because of its extremely small strength compared to the relative strengths of the other three fundamental forces, gravitation only becomes relevant in the presence of extremely large masses such as planets or stars and does not play a significant role in microscopic particle interactions.

The Brout-Englert-Higgs theory, finally, describes the process through which W and Z bosons acquire mass [7–9]. It is associated with the Higgs field, the quantum excitations of which give rise to a fundamental particle with spin zero, the *Higgs boson*.

Despite its tremendous success, the Standard Model leaves many questions unanswered. Questions such as those about the nature of dark matter or the observed but not fully understood asymmetry of matter and antimatter at the origin of the universe require probing beyond the Standard Model. Particle physics, today, is preparing to embark on the hunt opened by these (and many more) fundamental questions.

On the search for evidence of physics beyond the Standard Model, modern particle accelerators such as the LHC at CERN are important tools. To improve the sensitivity for observations pointing to new physics, in 2027, the LHC will increase its collision rate by a factor of five compared to the present [10]. And the experiments situated at the collider, such as ATLAS [11] and CMS [12], will need to adapt their detector technologies to face the challenges of the new high luminosity environment. The necessary upgrade of the experiments will take place during the third long shutdown of the LHC, between 2025 and 2027.

As an integral part of the upgrade, the CMS detector will see a complete replacement of the silicon tracker and the Endcap Calorimeter [6]. The full CMS Outer Tracker and parts of the new High Granularity Calorimeter (HGCAL), which will replace the current calorimeter endcaps, will use large-area, position-sensitive silicon sensors as active detector material, covering at total area of about $800\,\mathrm{m}^2$. Consequently, between 2020 and 2023, over $50\,000$ silicon sensors will be manufactured to be integrated in the CMS Outer Tracker and HGCAL.

This thesis deals with the development of a dedicated plan to ensure the quality of the manufactured silicon sensors and to continuously monitor the stability of the sensor production process. It focuses on building a strategy to track important process parameters over the course of sensor series production. The process parameters are extracted using specialized test structures that are manufactured on the same wafers as the silicon sensors and, hence, share the same properties. With test structures, it is possible to measure parameters that are not directly accessible on the sensors, including parameters that require destructive measurements.

My work on the development of the strategy for CMS process quality control encompassed the following main steps:

1. I electrically characterized a large variety of different test structures manufactured on prototype wafers by different semiconductor companies to investigate the feasibility of individual test structures to extract certain process parameters of interest.

2. Based on measurement results, I conducted computer simulations to reproduce measured test structure characteristics and gain a deeper understanding of the response of test structure properties to the variation of characteristic process parameters.

3. Building on the results obtained from test structure measurements and simulations, I developed a set of test structures that constitutes the basis of the CMS process quality control strategy. The set facilitates the automated assessment of a comprehensive set of process parameters and allows the evaluation of the most important parameters in about 30 minutes per wafer.

4. In parallel with the above mentioned steps and in close collaboration with scientists and technicians at the Institute of High Energy Physics (HEPHY) in Vienna, I commissioned a new probe station at the HEPHY cleanroom to provide the means for automated measurements of the set of test structures utilizing a 20-needle probe card and prepare for the upcoming CMS silicon sensor series production.

Chapters 2 and 3 briefly introduce the background of the work presented in this thesis, including the LHC at CERN and the CMS Phase-2 Upgrade, the basis of semiconductor physics, and the working principles of silicon sensors for high energy particle physics. The silicon

sensors for the CMS Outer Tracker and HGCAL, as well as sensor design considerations and the quality control procedure, are described in chapter 4. Chapter 5 presents the newly commissioned measurement setup in the HEPHY cleanroom and introduces the software framework used for simulations. Finally, chapters 6 and 7 constitute the central parts of this thesis. Chapter 6 discusses in detail the investigated test structures and the corresponding process parameters. It relates measurement results and simulations and presents conclusions on the capabilities of different test structures to determine the same process parameter with the aim to establish complementary parameter extraction methods. The newly developed set for automated CMS process quality control is presented in chapter 7. The chapter describes all components of the set and discusses measurement results of the first instances of the set on CMS Outer Tracker production and HGCAL prototype wafers.

I published a brief summary of the CMS quality control procedure and some of the main findings of this thesis in [13]. Some parts of this publication are referred to in chapters 4, 6, 7, and 8. Further, I have previously published some results included in chapter 6 in [14] and [15].

CHAPTER 2

EXPERIMENTAL HIGH ENERGY PARTICLE PHYSICS AT CERN

The European Organization for Nuclear Research (CERN[1]), located at the French-Swiss border near Geneva, is one of the largest scientific research centers in the world. It operates the world's largest particle physics laboratory and houses a diverse community of permanent and visiting scientists and engineers as well as thousands of scientific users from its 23 member states and many more countries all over the world.

Since its establishment in 1954, CERN has provided the environment and infrastructure for many important scientific discoveries such as the discovery of W and Z bosons in 1983 [16–19], the first creation of antihydrogen atoms in 1995 [20], the discovery of direct CP violation in 1999 [21], and, most recently in 2012, the discovery of a boson with mass $125\,\mathrm{GeV}/c^2$ consistent with a Higgs boson [4, 5]. Along with these milestones in particle physics, the scientific research at CERN has fostered diverse advancements for society at large. The World Wide Web was born at CERN, and CERN scientists have made important contributions to the development of tools for medical diagnostics, imaging, and treatments such as the positron emission tomography (PET) scans and hadron cancer therapy.

The following sections give a brief overview of particle physics experiments at the CERN Large Hadron Collider, focusing on the CMS experiment and the upgrade towards the High Luminosity LHC era.

2.1 The Large Hadron Collider

The Large Hadron Collider (LHC) [22] is the world's largest particle accelerator. Built in the underground cavern of the former Large Electron Positron Collider (LEP), the $\sim 27\,\mathrm{km}$ long synchrotron storage ring makes up the last stage of a powerful accelerator complex (Figure 2.1). At the end of the acceleration stages, protons (p) collide within the LHC at a nominal center of mass energy of $\sqrt{s} = 13\,\mathrm{TeV}$. One month per year, the LHC collides lead nuclei (Pb-Pb) at a center of mass energy per nucleon of $\sqrt{s_{\mathrm{NN}}} = 5.02\,\mathrm{TeV}$. Also, asymmetric p-Pb collisions and collisions of xenon nuclei (Xe-Xe) have been conducted [23].

The four large-scale physics experiments ATLAS[2], CMS[3], LHCb[4], and ALICE[5] are located at four interaction points along the LHC, where the two counter-rotating proton beams intersect. These experiments measure the particles produced in LHC collisions. While ATLAS and CMS are general-purpose detectors that measure a wide range of particles and search for new physics, LHCb mainly probes for CP-violation and rare decays involving bottom and charm quarks, and ALICE operates with heavy-ion collisions investigating quark-gluon-plasma.

[1] CERN: Conseil Européen pour la Recherche Nucléaire
[2] ATLAS: A Toroidal LHC Apparatus [11]
[3] CMS: Compact Muon Solenoid [12]
[4] LHCb: LHC-beauty experiment [25]
[5] ALICE: A Large Ion Collider Experiment [26]

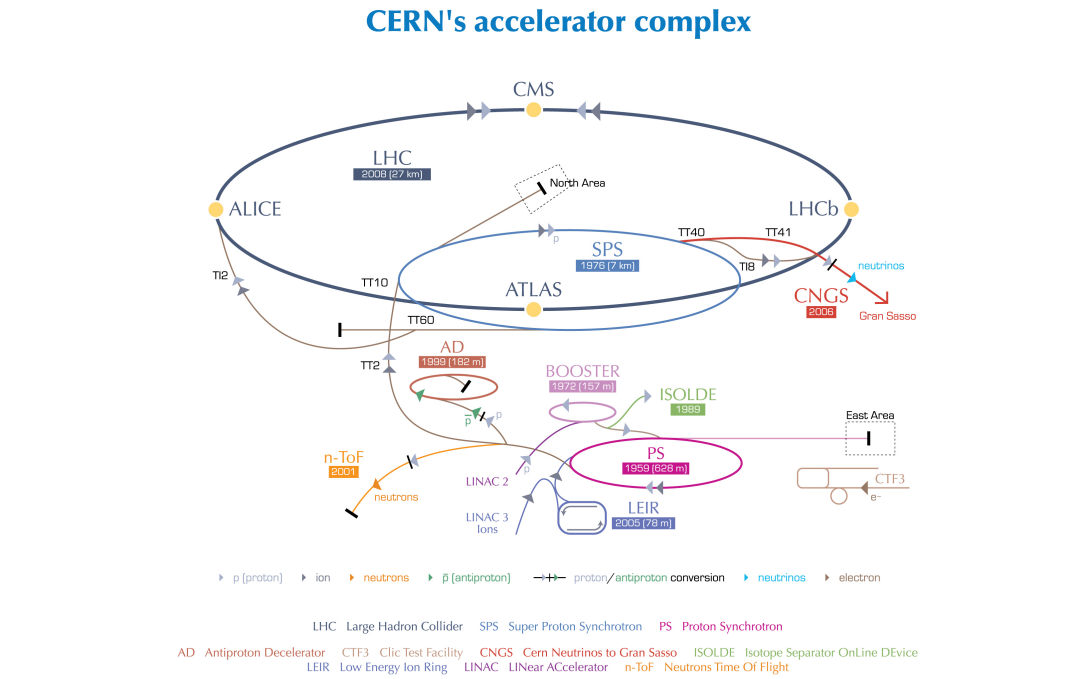


FIGURE 2.1: The CERN accelerator complex including the LHC, pre-accelerators, and the four large experiments located at LHC collision points. Figure taken from [24].

Protons are filled into the two counter-rotating beams of the LHC in bunches with $\sim 10^{11}$ protons each. Each beam contains 2808 bunches in regular intervals. The proton bunches are kept on their circular tracks using 1232 superconducting dipole magnets that generate a magnetic field of up to 8.33 T. 392 quadrupole magnets are used to focus the beams, and eight radio-frequency (RF) cavities per beam accelerate the particles and ensure high luminosity [27].

The luminosity $\mathcal{L}$ of a particle collider is an important parameter indicating the quality of the machine as it, essentially, describes the number of collision events per second. For a process with a given cross section σ_p, the event rate per second $\mathcal{R}_\mathrm{p}$ is given by

$$\mathcal{R}_\mathrm{p} = \mathcal{L} \cdot \sigma_\mathrm{p} \,. \tag{2.1}$$

The luminosity only depends on the beam parameters and is given by

$$\mathcal{L} = \frac{N_\mathrm{b}^2 n_\mathrm{b} f \gamma}{4\pi \varepsilon_\mathrm{n} \beta^*} F \,, \tag{2.2}$$

where N_b is the number of particles per bunch, n_b is the number of bunches per beam, f is the revolution frequency of the bunches, γ denotes the relativistic Lorentz factor, ε_n is the normalized transverse beam emittance, β^* is the betatron function at the collision point, and F represents a geometric luminosity reduction factor accounting for the crossing angle at the collision point [22]. The LHC design luminosity is $1 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$. Before the second long shutdown of the machine at the end of 2018, the LHC reached a peak luminosity of $2 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$.

The integrated luminosity describes the luminosity accumulated over a certain time. At the end of 2018, the total integrated luminosity since the beginning of LHC operation was $190\,\mathrm{fb}^{-1}$. That value is expected to reach $350\,\mathrm{fb}^{-1}$ at the end of LHC Run 3 in 2024.

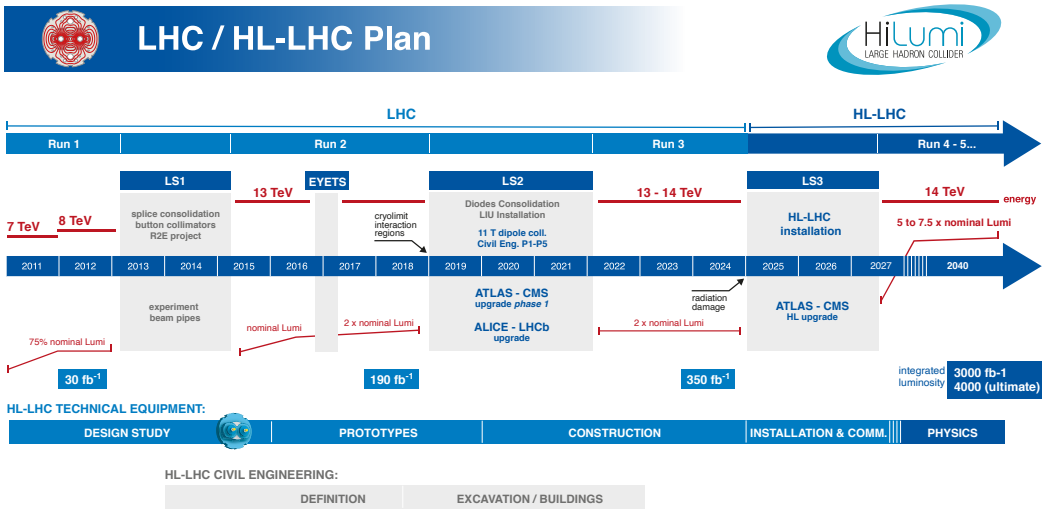


FIGURE 2.2: LHC project schedule including the plan for the upcoming high luminosity upgrade. Figure taken from [28].

2.1.1 The High Luminosity LHC Upgrade

During the third long shutdown (LS3) of the LHC, scheduled from 2025 to 2027, the accelerator will undergo a major upgrade to reach an instantaneous luminosity of $5 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ and up to $7.5 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$. The era after LS3 is denoted as the High Luminosity LHC (HL-LHC) era (Figure 2.2). Up until 2037, the HL-LHC will accumulate a total integrated luminosity of $3000\,\mathrm{fb}^{-1}$ ($4000\,\mathrm{fb}^{-1}$ in the ultimate scenario). The increased luminosity will provide much higher data rates and event statistics, enabling precision studies of Higgs properties and rare events and the search for physics beyond the Standard Model of particle physics.

The current experiments and detector systems at the LHC are not suited to operate in the challenging environment of the HL-LHC. Consequently, the experiments will undergo substantial upgrades during LS3. The corresponding upgrade of the CMS detector is referred to as the CMS Phase-2 Upgrade.

2.2 The Current CMS Experiment

The CMS experiment (Figure 2.3) is one of the two general purpose experiments at the LHC. It is composed of different sub-detectors that make up the layers of the hermetic, barrel-shaped detector. Starting from the collision point at the center of the detector, each layer serves a different purpose. In conjunction, they allow the identification of the physical processes happening in the collisions.

One of the main characteristics of the CMS detector is the large superconducting *solenoid magnet*, which produces a magnetic field of nearly $4\,\mathrm{T}$. The magnetic field bends the tracks of charged particles. Because the curvature of the tracks depends on the particle momentum, the solenoid is an integral ingredient for successful particle and event identification. The iron return yoke of the magnet alone contributes $12\,500$ tons to the total detector weight of $14\,000$ tons.

Starting from the interaction point, the *silicon tracking detector* [30] makes up the innermost layer of the CMS experiment. It records the trajectories of charged particles, from which the particle momenta can be deduced. The active elements of the CMS tracker are silicon pixel sensors in the center close to the beam axis and silicon micro-strip sensors in the outer layers. In total, the silicon sensors cover an area of $\sim 200\,\mathrm{m}^2$ up until pseudorapidity $|\eta| < 2.5$.

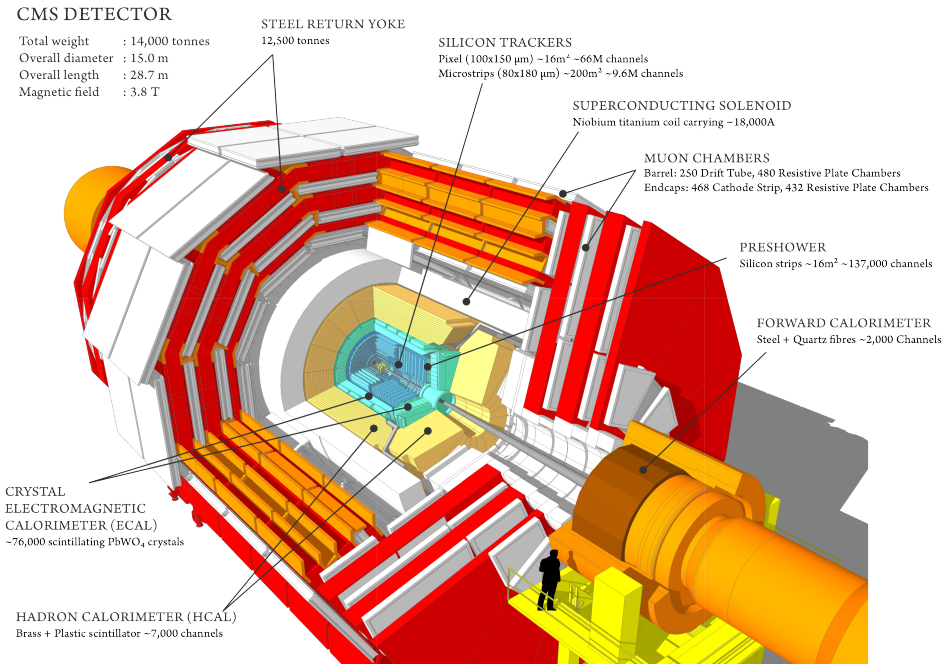


FIGURE 2.3: Schematic drawing of the CMS experiment illustrating the various sub-detectors. Figure taken from [29].

The inner pixel detector is exposed to a particle rate of about 10 million $\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ at a distance from the beam line of $8\,\mathrm{cm}$. To provide sufficiently high granularity, the pixel detector contains about 66 million pixels covering an active area of $\sim 1\,\mathrm{m}^2$.

The barrel of the silicon micro-strip tracker consists of ten overlapping layers of silicon strip sensors – four in the inner barrel (TIB) and six in the outer barrel (TOB). In forward direction, the barrel is closed off by two inner disks (TID) and two end-caps (TEC). The entire tracking system is cooled to $-20\,^{\circ}\mathrm{C}$ to mitigate the effects of radiation damage. The silicon strip tracker offers about 10 million individual strips contained in a total of 15 200 sensor modules including between one and two sensors per module. Among the sensors, different shapes and sizes are realized. Sensors with shorter strips and higher granularity are located closer to the beamline, while larger sensors with longer strips make up the outer tracker layers.

The *electromagnetic calorimeter* (ECAL) surrounds the CMS tracker. It measures the energy of particles such as photons and electrons, which interact via the electromagnetic force. The interactions of these particles with the calorimeter material generate electromagnetic showers, through which the full energy of the initial particles is deposited. Consequently, the particles are stopped in the calorimeter. ECAL is a homogeneous calorimeter made up of 68 524 scintillating lead tungstate ($PbWO_4$) crystals as active material, which are read out by avalanche photodiodes and vacuum phototriodes. The light output of the scintillators is proportional to the deposited energy.

Hadrons such as protons, neutrons, and pions penetrate the electromagnetic calorimeter and are only stopped in the subsequent calorimeter stage, the *hadronic calorimeter* (HCAL). HCAL is a sampling calorimeter composed of alternating layers of brass absorbers and plastic scintillators with wavelength shifting fibers as active material read out by hybrid photodiodes. The entering hadrons produce hadronic showers that stop inside the calorimeter volume.

The *forward calorimeter* (HF) in the pseudorapidity range $3 \leq |\eta| \leq 5$ is based on a steel absorber with embedded fused-silica-core optical fibers that detect the Cherenkov light of showering particles as active material [31]. The material offers high radiation tolerance, an essential characteristic needed to cope with the high particle flux in forward direction.

The *muon chambers* of CMS are embedded into the steel return yoke of the magnet. They use different gas detector technologies, namely drift tubes, resistive plate chambers, and

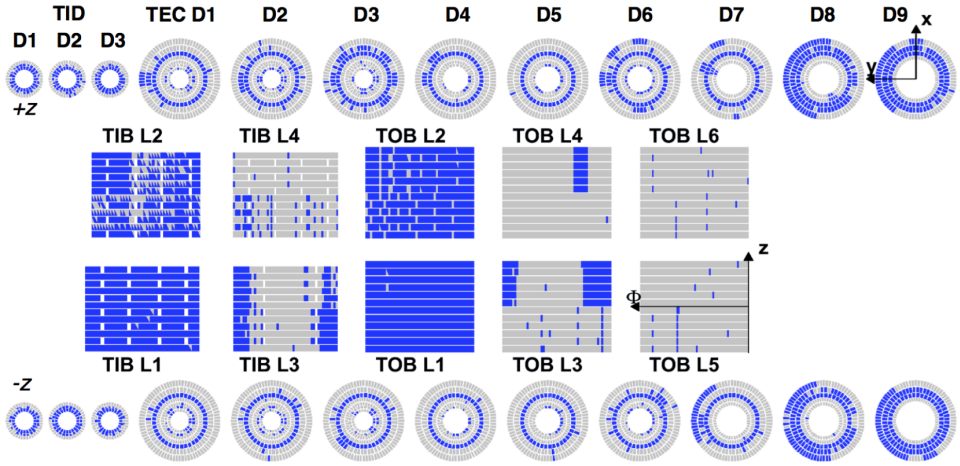


FIGURE 2.4: Map of non-functional modules (blue) in the current CMS Tracker simulated for $1000\,\mathrm{fb}^{-1}$ integrated luminosity. Figure taken from [6].

cathode strip chambers. The detectors measure position and momentum of muons, which (aside from neutrinos) are the only particles that penetrate both calorimeters. The muon system ensures that the CMS detector is hermetic for all particles except neutrinos and, hence, plays an important role for the indirect detection of neutrinos via missing transverse energy.

CMS employs two *trigger* stages to reduce the produced data rate and select events of high physical interest for storage. The level-1 (L1) stage is a hardware trigger that reduces the original data rate corresponding to the $40\,\mathrm{MHz}$ LHC bunch crossing frequency to $100\,\mathrm{kHz}$. For this purpose, the L1 trigger combines information from the calorimeter system and the muon chambers and produces a trigger signal within $3\,\mu\mathrm{s}$. The second triggering stage, the High Level Trigger (HLT), is a pure software trigger that performs event reconstruction using a streamlined version of CMS offline reconstruction software running on a computer farm. It makes the final decision whether an event is stored or discarded, reducing the rate to $\sim 1\,\mathrm{Hz}$ [32].

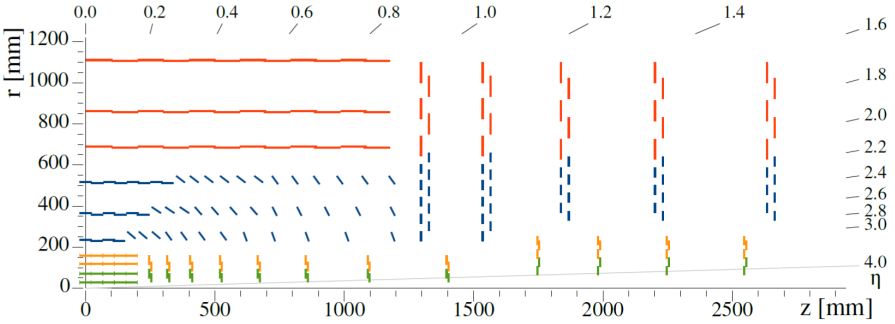
2.3 The CMS Phase-2 Upgrade

The CMS Phase-2 Upgrade [6] will take place during LS3 between 2025 and 2027 and will prepare the full CMS detector for the challenges of the HL-LHC environment. The new detector must be able to withstand substantial radiation levels, provide increased granularity to cope with a pileup of 140 (200 in the ultimate scenario), increase bandwidth to accommodate higher data rates, and improve the trigger performance. Consequently, the upgrade will concern all sub-detector systems, readout electronics, and the L1 trigger.

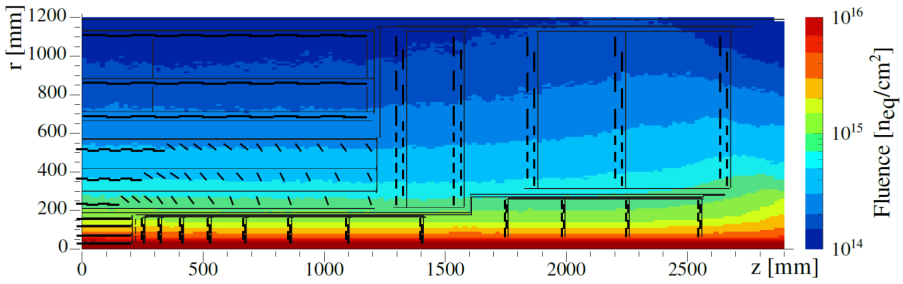
The muon system will see the improvement of the currently implemented gas detectors. Gas electron multiplier (GEM) detectors will be added in the forward region. ECAL and HCAL will only undergo minor upgrades such as the replacement of the HCAL hybrid photodiode readout with silicon photo multipliers (SiPM). In contrast to the other sub-detectors, the CMS silicon tracker and the calorimeter endcaps will experience extensive upgrades. The CMS tracker will have accumulated substantial radiation damage by 2024 (Figure 2.4) and will need to be replaced entirely. Similarly, the current forward calorimeter will not be able to retain adequate performance beyond $500\,\mathrm{fb}^{-1}$ and will be replaced by the High Granularity Calorimeter (HGCAL).

2.3.1 Tracker Upgrade

The new CMS tracker [33] will provide increased radiation hardness, an improved layout, a new module design in the Outer Tracker that enables contribution to the L1 trigger, reduced material budget, and extended coverage in the forward region. It is separated into two



(A) Schematic of one quarter of the CMS Tracker layout in r-z view. Pixel modules of the Inner Tracker are represented in green (featuring two readout chips) and yellow (four readout chips). The Outer Tracker contains modules comprised of two strip sensors (2S, red) and modules comprised of one strip sensor and one macro-pixel sensor (PS, blue) that enable discrimination of tracks with low transverse momentum.



(B) FLUKA simulation of the integrated particle fluence in 1 MeV n_{eq}/cm^2 in a quarter of the Phase-2 CMS Tracker at 3000 fb^{-1} integrated luminosity.

FIGURE 2.5: Schematic layout (A) and simulated particle fluence (B) for the upgraded CMS Tracker. Figures taken from [33].

sub-detectors, the Inner Tracker, which consists of small-size silicon pixel sensors, and the Outer Tracker, which is comprised of silicon macro-pixel sensors and strip sensors.

Tracker Layout and Sensor Modules

The layout of the upgraded tracker (Figure 2.5a) is designed to offer robust tracking and extended forward coverage while maintaining a low material budget.

The Inner Tracker contains four barrel layers and twelve discs on each end ensuring a forward coverage up to $\eta = 4$. The pixel modules cover a total active area of $4.9\,m^2$.

Six barrel layers and five discs on each end make up the Outer Tracker. The Outer Tracker features two different types of modules. In the inner parts of the Outer Tracker, modules consist of a silicon macro-pixel sensor and a silicon strip sensor and are denoted "PS modules". The modules of the outer layers are composed of two silicon strip sensors and are denoted "2S modules". To facilitate tracking and triggering efficiency and to reduce the overall material budget, some of the PS modules in the barrel are tilted so that the angle of particle impact remains mostly identical for all PS modules in the barrel.

At an integrated luminosity of $3000\,fb^{-1}$, the maximum particle fluence in the Inner Tracker is expected to amount to $2.3 \times 10^{16}\,n_{eq}/cm^2$ (Figure 2.5b). Outer Tracker PS modules will have to withstand a maximum fluence of about $1 \times 10^{15}\,n_{eq}/cm^2$ and the innermost 2S modules (at $r = 676\,mm$) will see a maximum fluence of about $3 \times 10^{14}\,n_{eq}/cm^2$. On the basis of extensive radiation campaigns [34, 35], CMS has decided to use *p* type silicon as sensor baseline material. Section 4.1 gives a detailed description of the sensor material and design for the CMS Outer Tracker.

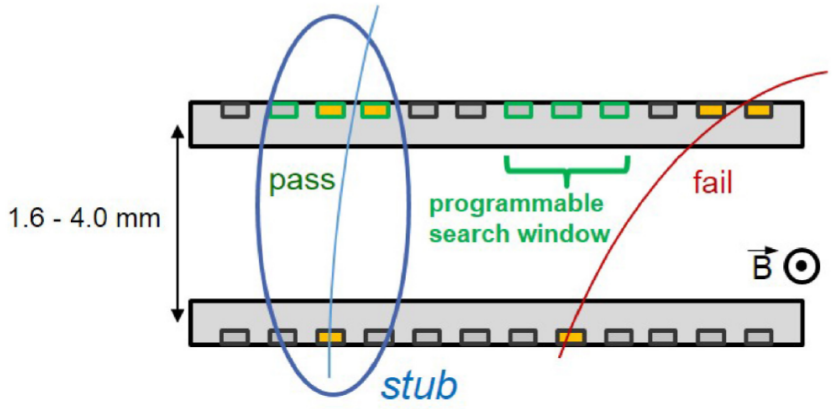


FIGURE 2.6: Illustration of the p_T track trigger module concept. Boxes represent individual sensor pixels or strips. The correlation of signals between two closely-spaced sensors of a module enables rejection of particle tracks with low transverse momentum p_T. Figure taken from [36].

Trigger Input

The PS and 2S modules of the Outer Tracker are designed to allow transverse momentum (p_T) discrimination at module level (Figure 2.6). Both types of modules comprise two closely stacked, parallel oriented sensors. The hit positions on both sensors of each module are correlated by the specialized readout chips to determine the particle p_T. The hit matching search window can be programmed with respect to the module location and trigger requirements. Tracks that fall within the search window correspond to a p_T threshold of $\sim 2\,\mathrm{GeV}$ and are denoted as stubs. Stubs are transmitted at bunch crossing frequency to the back-end electronics of the Outer Tracker, where they are fed into specialized tracking algorithms that reconstruct tracks. The reconstructed tracks are included into the L1 trigger decision, enabling a L1 acceptance rate of $\leq 750\,\mathrm{kHz}$ without physics performance degradation.

2.3.2 High Granularity Calorimeter

The CMS High Granularity Calorimeter (HGCAL) [37] will offer high radiation tolerance, unprecedented transverse and longitudinal granularity, precise measurement of the time of high energy showers, and the ability to contribute to the L1 trigger decision.

HGCAL will be built as a sampling calorimeter with silicon sensors and scintillating tiles as active material (Figure 2.7). The calorimeter is separated into an electromagnetic compartment (CE-E), which uses entirely silicon as active material, and a hadronic compartment (CE-H), which uses both silicon and plastic scintillators read out by SiPMs. CE-E employs copper, copper-tungsten, and lead plates clad in stainless steel as absorber material, while CE-H uses only stainless steel. The whole calorimeter volume is thermally shielded and maintained at $-35\,^{\circ}\mathrm{C}$.

The silicon base material for HGCAL are hexagonal *p* type sensors, which come in two different granularities and three different thicknesses (i.e. $300\,\mu\mathrm{m}$, $200\,\mu\mathrm{m}$, and $120\,\mu\mathrm{m}$) accounting for regions of different fluence within the detector volume (Figure 2.8). At an integrated luminosity of $3000\,\mathrm{fb}^{-1}$, the respective maximum fluence values are 5×10^{14}, 2.5×10^{15}, and $7 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$ for the $300\,\mu\mathrm{m}$, $200\,\mu\mathrm{m}$, and $120\,\mu\mathrm{m}$ thick sensors. Also, the usage of silicon or scintillators as active material is related to the expected fluence. Silicon is used in the high fluence regions of the calorimeter volume, and scintillators are used in regions with lower fluence. The total area covered by silicon amounts to $\sim 620\,\mathrm{m}^2$. A more detailed description of the HGCAL silicon sensors is given in section 4.1.4.

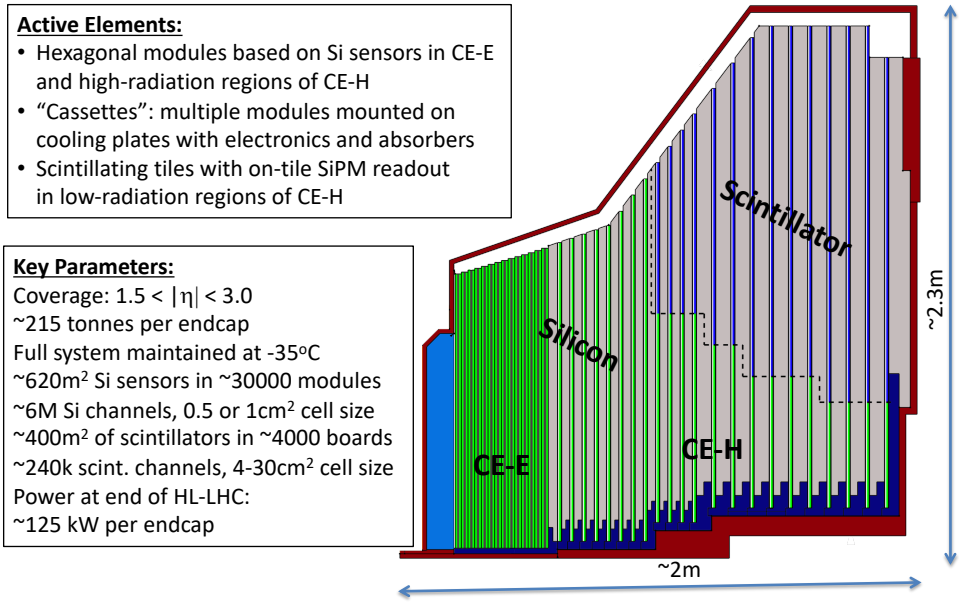


FIGURE 2.7: Cross section of CMS HGCAL. Figure taken from [38].

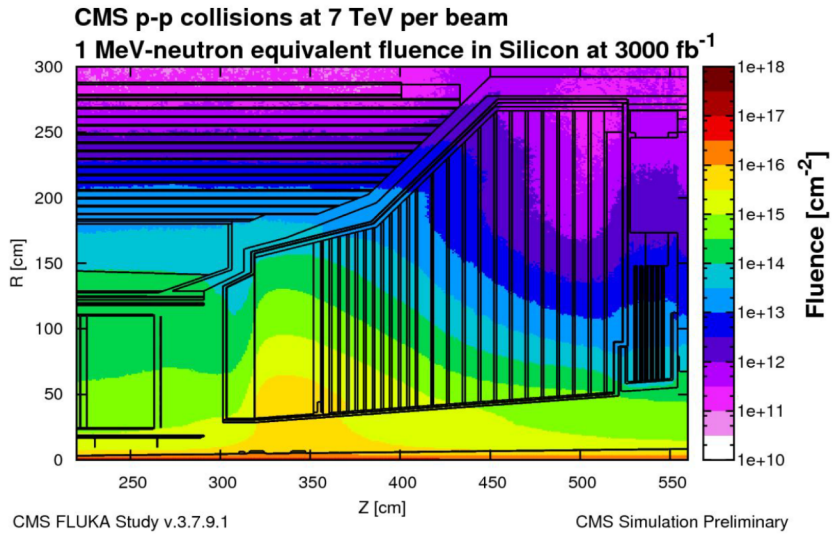


FIGURE 2.8: FLUKA simulation of the particle fluence in $1\,\mathrm{MeV\,n_{eq}/cm^2}$ accumulated in HGCAL after an integrated luminosity of $3000\,\mathrm{fb^{-1}}$. The layout is shown in in r-z view. Figure taken from [37].

CHAPTER 3

SILICON SENSORS FOR HIGH ENERGY PARTICLE PHYSICS

Silicon sensors are important building blocks of many particle physics experiments today. The comparatively low ionization energy of silicon in combination with the high density of the semiconductor material, allow for high signals induced by the passage of charged particles, even in a comparatively thin sensor. Additionally, because of the relatively slow diffusion of the induced charge carriers, the achievable position resolution is high (i.e. less than $10\,\mu\mathrm{m}$). Furthermore, silicon offers a high intrinsic radiation hardness, which makes it particularly suited for the application in high-radiation environments such as the detectors at the HL-LHC. Physics applications can draw from the vast experience of the microelectronics industry, which allows well-functioning, cost-effective silicon sensors to be produced by different industrial partners.

The following sections briefly introduce the physical background of silicon detectors for high energy particle physics applications. Comprehensive, in-depth discussions about semiconductor devices in general and silicon particle detectors in particular can be found in textbooks such as those by Sze [39, 40], Lutz [41], Kolanoski and Wermes [42], and Schroder [43].

The explanations of some of the general concepts in this chapter have been adapted from an introductory chapter on the topic of silicon sensors, which I have previously published in [44].

3.1 Semiconductor Physics

Silicon, as a group IV element, has four valence electrons that, in the solid state, form covalent bonds to the four nearest neighbors, resulting in a diamond lattice crystal structure. Within the crystal, the discrete energy levels of electrons in individual atoms degenerate to continuous *energy bands*. At low temperatures (i.e. effectively only at $T = 0\,\mathrm{K}$) and in the absence of impurities, all electrons are bound to the crystal lattice, and no conduction is possible. For temperatures $T > 0\,\mathrm{K}$, covalent bonds may be broken by thermal vibrations lifting electrons from the *valence band* into the *conduction band*. A free electron leaves a vacancy that may be filled by a neighboring electron and thereby can move through the lattice. The mobile vacancy corresponds to a positive charge carrier in the valence band, a *hole*. The upper edge of the valence band is denoted E_v, and the lower edge of the conduction band is denoted E_c. The difference $E_\mathrm{c} - E_\mathrm{v}$ is referred to as the *band gap* E_g. For silicon, $E_\mathrm{g} = 1.12\,\mathrm{eV}$ [40].

The probability that an electron occupies a state with energy E is given by the Fermi-Dirac distribution function [40]

$$F(E) = \frac{1}{1 + \exp\left[(E - E_\mathrm{F})/kT\right]}\,. \tag{3.1}$$

Here, k denotes the Boltzmann constant, and E_F is the *Fermi level*, the energy at which the

occupation probability is exactly one-half. For semiconductors, the band gap is small enough that some electrons can already occupy energy states within the conduction band at room temperature.

Semiconductors that contain only a negligible amount of impurities in the crystal lattice are called *intrinsic semiconductors*. At thermal equilibrium, the number of free electrons per unit volume n is equal to the number of free holes per unit volume p, i.e. $n = p = n_\mathrm{i}$. The *intrinsic carrier density* n_i is given by [39]

$$n_\mathrm{i} = \sqrt{N_\mathrm{c} N_\mathrm{v}} \cdot \exp(-\frac{E_\mathrm{g}}{2kT}) \,, \tag{3.2}$$

where N_c and N_v are the effective densities of states in the conduction band and valence band, respectively. An easy empiric formula for the intrinsic carrier concentration in silicon as a function of temperature is given in [45]:

$$n_\mathrm{i}(T) = 5.29 \times 10^{19} (T/300)^{2.54} \exp(-6726/T) \,. \tag{3.3}$$

The Fermi level of an intrinsic semiconductor E_i is given as

$$E_\mathrm{i} = \frac{E_\mathrm{g}}{2} + \frac{kT}{2} \ln(\frac{N_\mathrm{v}}{N_\mathrm{c}}) \,. \tag{3.4}$$

Since, at room temperature, the latter term is much smaller than E_g, the intrinsic Fermi level of an intrinsic semiconductor lies very close to the middle of the band gap [40].

3.1.1 Doping

If the properties of intrinsic semiconductors are intentionally altered by introducing impurities into the crystal (i.e. doping), the semiconductor becomes *extrinsic*. Silicon is either doped with elements from group V of the periodic table (e.g. phosphorus or arsenic), creating an n type semiconductor, or elements from group III (e.g. boron, gallium, or indium), resulting in p type silicon. In case of n type doping, the dopant contributes four of its valence electrons to the covalent bonds with the neighboring silicon atoms and leaves a weakly bound fifth electron that can be easily lifted into the conduction band. Hence, the impurity is referred to as *donor* impurity because it introduces additional states at the upper edge of the forbidden band gap that can easily "donate" electrons to the conduction band. Similarly, an *acceptor* impurity introduces additional states near the lower edge of the band gap that can easily "accept" electrons from the valence band and leave behind holes. The introduction of these additional states leads to a shift of the Fermi level compared to the intrinsic case (Figure 3.1).

If the additional energy states lie close to the band edges, all impurities are ionized at room temperature. In this case, the concentration of majority dopants (i.e. the donor concentration N_D in case of *n* type and the acceptor concentration N_A in case of *p* type) is equal to the majority carrier density (i.e. the electron density n for *n* type and the hole density p for *p* type).

The resistivity ρ of a semiconductor depends on the densities n and p of free electrons and holes and the electron and hole mobilities μ_n and μ_p according to [43]

$$\rho = \frac{1}{q(n\mu_n + p\mu_p)} \,. \tag{3.5}$$

Under complete ionization condition, (3.5) can be simplified to

$$\rho = \frac{1}{q\mu_p N_\mathrm{A}} \quad \text{and} \quad \rho = \frac{1}{q\mu_n N_\mathrm{D}} \tag{3.6}$$

for *p* type and *n* type extrinsic semiconductors, respectively.

3.1.2 Charge Carrier Transport

Electrons and holes move through the semiconductor under the influence of external electric fields and in response to carrier concentration gradients. The corresponding transport

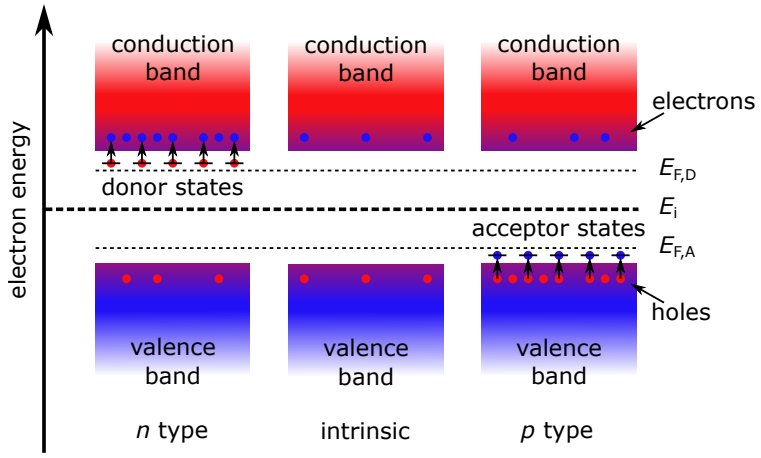


FIGURE 3.1: Schematic representation of the energy band model for extrinsic n type (left) and p type (right) semiconductors compared to an intrinsic semiconductor (center). In an n type material, the Fermi level $E_{F,D}$ shifts closer to the edge of the conduction band, whilst for p type material the Fermi level $E_{F,A}$ shifts closer to the valence band edge. Figure adapted from [44].

mechanisms are referred to as drift and diffusion.

Drift

Under the influence of an external electric field, charge carriers are accelerated in-between random collisions in a direction determined by the electric field. The drift velocity is given by the product of the electric field strength E and the carrier mobility μ, i.e. [39]

$$v_n = -\mu_n \cdot E \quad \text{and} \quad v_p = \mu_p \cdot E \tag{3.7}$$

for electrons and holes, respectively. The mobility depends on temperature, the effective mass of the charge carriers, as well as the doping concentration and, hence, electron mobility is generally higher than hole mobility. Empirical relationships for electron and hole mobilities as a function of carrier concentration and temperature are given in [46].

Diffusion

In response to a gradient of carrier concentration, charge carriers diffuse from the region of high concentration toward the region of low concentration. The flux of charge carriers is governed by Fick's law [39]

$$\left.\frac{\mathrm{d}\Delta n}{\mathrm{d}t}\right|_x = -D_n \frac{\mathrm{d}\Delta n}{\mathrm{d}x} \quad \text{and} \quad \left.\frac{\mathrm{d}\Delta p}{\mathrm{d}t}\right|_x = -D_p \frac{\mathrm{d}\Delta p}{\mathrm{d}x} \tag{3.8}$$

for electrons and holes, respectively. Here, Δn and Δp denote the differences in electron concentration and hole concentration, respectively, and $D_{n,p}$ are the diffusion coefficients for electrons and holes.

The combined effects of drift and diffusion give the total current density [39]

$$\vec{J}_n = q\mu_n n\vec{E} + qD_n\vec{\nabla}n \tag{3.9}$$

for electrons and

$$\vec{J}_p = q\mu_p p\vec{E} - qD_p\vec{\nabla}p \tag{3.10}$$

for holes, whereby q denotes the elementary charge. In both cases, the first term describes the drift, and the second term describes the charge carrier diffusion.

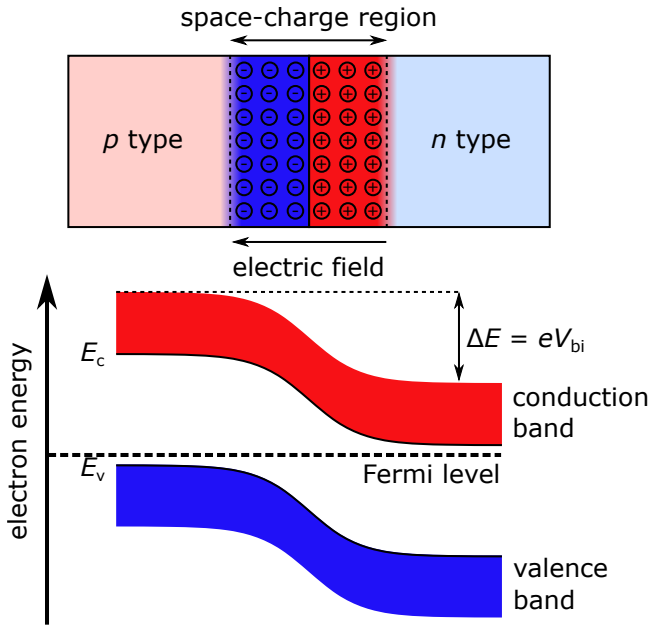


FIGURE 3.2: Schematic of a symmetric, abrupt *p-n* junction in thermal equilibrium, displaying the shift of the energy bands. Figure adapted from [44].

3.1.3 The *p-n* Junction

If *n* and *p* type materials are brought into contact, they form a *p-n* junction, or diode (Figure 3.2). As a result to the charge carrier concentration gradient, electrons diffuse from the *n* side into the *p* doped region and recombine with holes. For holes of the *p* type region, the same is true in the opposite direction. Consequently, an excess negative charge is established in the *p* type region and an excess positive charge in the *n* type region. The excess charges cause an electric field across the junction that induces a drift counteracting the diffusion movement. In thermal equilibrium, drift and diffusion are balanced and a region that is depleted of any free charge carriers forms around the *p-n* junction. This region is generally referred to as *space-charge region* or *depletion region*.

In thermal equilibrium, the Fermi levels must coincide on both sides of the junction. Consequently, the energy bands bend across a *p-n* junction (Figure 3.2). The corresponding potential difference across the space-charge region is denoted the built-in voltage V_{bi} of the junction, and is given by [39]

$$V_{\mathrm{bi}} = \frac{E_{\mathrm{F,D}} - E_{\mathrm{F,A}}}{q} = \frac{\Delta E}{q} = \frac{kT}{q} \ln\left(\frac{N_{\mathrm{A}} N_{\mathrm{D}}}{n_{\mathrm{i}}}\right). \tag{3.11}$$

The width W of the space-charge region depends on the doping concentrations of the conjoined materials and will stretch farther into the region with the lower doping concentration. In the unbiased case, it is given by the sum of the respective widths in the *p* and *n* type regions [39]:

$$W = W_p + W_n = \sqrt{\frac{2\varepsilon_{\mathrm{Si}}}{q} \frac{N_{\mathrm{D}} V_{\mathrm{bi}}}{N_{\mathrm{A}}(N_{\mathrm{A}} + N_{\mathrm{D}})}} + \sqrt{\frac{2\varepsilon_{\mathrm{Si}}}{q} \frac{N_{\mathrm{A}} V_{\mathrm{bi}}}{N_{\mathrm{D}}(N_{\mathrm{A}} + N_{\mathrm{D}})}}. \tag{3.12}$$

Here, $\varepsilon_{\mathrm{Si}} = \varepsilon_0 \varepsilon_{\mathrm{r,Si}}$ denotes the permittivity of silicon, composed of the vacuum permittivity ε_0 and the relative permittivity of silicon $\varepsilon_{\mathrm{r,Si}}$, for which the value $\varepsilon_{\mathrm{r,Si}} = 11.68$ is used for all calculations in this thesis.

If an external bias voltage V is applied across the *p-n* junction, the space-charge region either grows (i.e. *reverse bias*) or diminishes until it vanishes when $V = -V_{\mathrm{bi}}$ (i.e. *forward bias*). For a one-sided abrupt n^+-*p* junction with $N_{\mathrm{D}} \gg N_{\mathrm{A}}$, the depletion width under reverse bias

is obtained from (3.12) as

$$W \approx \sqrt{\frac{2\varepsilon_{\mathrm{Si}}}{qN_{\mathrm{A}}(V_{\mathrm{bi}}+V)}}\,. \tag{3.13}$$

The *p-n* junction only conducts current under forward bias. Under reverse bias, only a much smaller *leakage current* flows, which is composed of a diffusion component from charge carriers outside of the depletion region and a generation component from within the space-charge region (refer to section 6.1.4 for a detailed discussion of generation-recombination processes and the associated carrier lifetimes).

For an ideal device, the diode current as a function of the applied bias voltage is given by the Shockley equation [39]

$$I(V) = I_0\big[\exp(\frac{qV}{kT}) - 1\big]\,. \tag{3.14}$$

In case of forward bias (i.e. $V > 0$) the current increases exponentially. Under reverse bias (i.e. $V < 0$), it saturates at I_0. If the reverse voltage is increased further, eventually, *junction breakdown* results and the current increases drastically. The voltage at which this happens, is referred to as the *breakdown voltage* V_{bd}. At high enough electric fields, accelerated charge carriers may break open other covalent bonds and cause *avalanche multiplication*. Thermal instabilities and tunneling may cause junction breakdown as well. In contrast to avalanche breakdown, which has a positive temperature coefficient, tunneling has a negative temperature coefficient and becomes relevant mainly at low temperatures [39].

An in-depth discussion of diode characteristics is given in section 6.1.

3.2 Signal Generation

A charged particle passing through a semiconductor detector creates electron-hole pairs, whereby it loses some of its kinetic energy. The mean ionization energy for silicon is $3.6\,\mathrm{eV}$. Because silicon features an indirect band gap, the minimum energy needed for ionization is larger than the band gap. In addition to the energy difference of the minimum band gap, a change of crystal momentum is necessary to lift an electron from the valence band into the conduction band. For the transition of the electron, a two-step process, in which a phonon transfers the additional momentum, is necessary. Also, a transition via crystal defects that introduce intermediate levels within the band gap is possible.

3.2.1 Interactions of Charged Particles with Matter

Moderately relativistic, heavy, charged particles traveling through matter mainly transfer energy to the surrounding material via multiple processes of elastic Coulomb scattering with electrons. For particles with $0.1 < \beta\gamma < 100$, where $\beta = v/c$ denotes the particle velocity v with respect to the speed of light and γ is the Lorentz factor, the Bethe-Bloch curve [47] (Figure 3.3) describes the mean energy loss (mass stopping power) in units of $\mathrm{MeV\,cm^2/g}$. Particles that fall in the regime of the minimum of the curve, are referred to as *minimum ionizing particles* (MIP). Most particles produced in LHC collisions fall into that category.

The energy transfer per interaction is subject to statistical fluctuations. Interactions with small energy transfer are more probable. For thin absorbers such as silicon sensors, the probability is best described by a Landau distribution [48]. This distribution is not symmetric around a mean value but, instead, features a characteristic tail toward higher energies, which takes into account that direct knock-on interactions may produce high-energetic δ-electrons that can cause further ionization in the material. As a main consequence, the mean energy transfer is not equal to the most probable energy transfer.

3.2.2 Signal Generation in Segmented Silicon Sensors

A position-sensitive silicon sensor, in essence, is composed of the more lightly doped silicon base material (*p* type in case of the sensors for the CMS Phase-2 Upgrade) and more heavily doped strips or pixels with the opposite polarity (n^+ for CMS Phase-2). Hence, in principle, the sensor is made up of many individual n^+-*p* junctions that are operated under reverse bias.

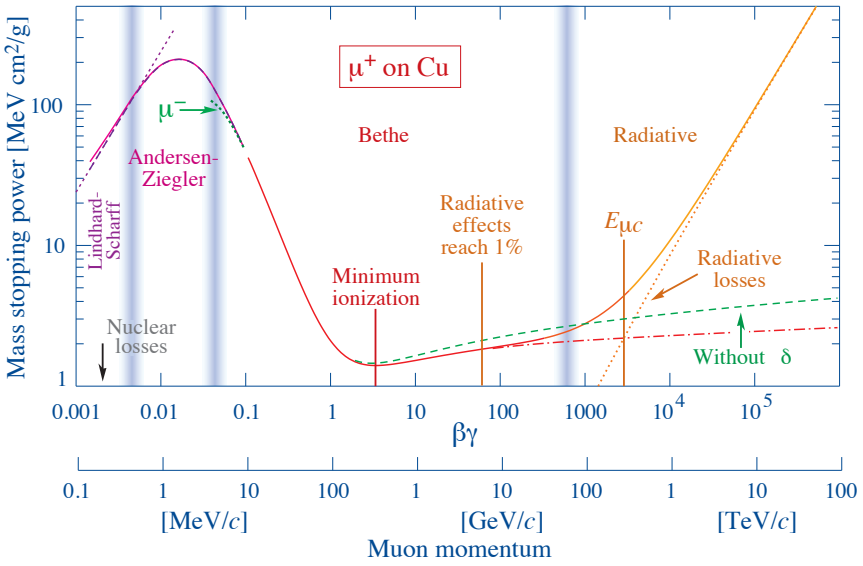


FIGURE 3.3: Mean energy loss (mass stopping power) $\langle \mathrm{d}E/\mathrm{d}x \rangle$ for positive muons in copper as a function of $\beta\gamma = p/Mc$. Figure taken from [47].

A traversing charged particle generates electron-hole pairs along its path through the sensor (Figure 3.4). Charge carriers created in the space-charge region of the n^+-p junctions drift in the electric field of the sensor and are collected by the electrodes, whereas the charge generated outside of the space-charge region is lost to recombination with free carriers. Consequently, sensors are predominantly operated under *full depletion*, that is, at a reverse bias voltage high enough that the space-charge region extends over the full width of the p type silicon bulk. The minimum voltage at which this condition is fulfilled is called *full depletion voltage* V_{dp}.

The drift of the generated charge carriers in the electric field of the reverse-biased sensor induces a current signal in the electrodes closest to the particle track. To derive the current signal induced on an individual electrode i, we calculate the weighting field $\vec{E}_{w,i}$ of the electrode from the weighting potential $\phi_{w,i}(\vec{r})$ as discussed in [42]. The total potential of k electrodes can be expressed as a superposition of the potential configurations $\phi_i(\vec{r})$, in which the potentials at all electrodes are set to zero except for the potential at electrode i, which is set to U_{i}:

$$\phi_0(\vec{r}) = \sum_{i=1}^{k} \phi_i(\vec{r})\,. \tag{3.15}$$

The weighting potential and the weighting field with respect to electrode i are then obtained as

$$\phi_{w,i}(\vec{r}) = \frac{\phi_i(\vec{r})}{U_i}\,, \qquad \vec{E}_{w,i} = -\vec{\nabla}\phi_{w,i}\,. \tag{3.16}$$

According to the Shockley-Ramo theorem [49, 50], the signal current $i_{S,i}$ induced at electrode i by a point charge q drifting with velocity $\vec{v}$ is given by the weighting field of the potential configuration $\phi_i(\vec{r})$ as

$$i_{S,i} = q\vec{E}_{w,i}\vec{v}\,. \tag{3.17}$$

The total signal current $I(t)$ is given by the sum of the individual currents induced by the drifting electrons and holes:

$$I(t) = q\vec{E}_{w,i}\Big(\sum_{i=1}^{N_{\mathrm{e}}(t)} \vec{v}_{\mathrm{e,i}}(t) + \sum_{j=1}^{N_{\mathrm{h}}(t)} \vec{v}_{\mathrm{h,j}}(t)\Big)\,, \tag{3.18}$$

where $N_{\mathrm{e}}(t)$ and $N_{\mathrm{h}}(t)$ are the time-dependent numbers of electrons and holes, respectively, and $\vec{v}_{\mathrm{e}}(t)$ and $\vec{v}_{\mathrm{h}}(t)$ denote the time-dependent electron and hole drift velocities.

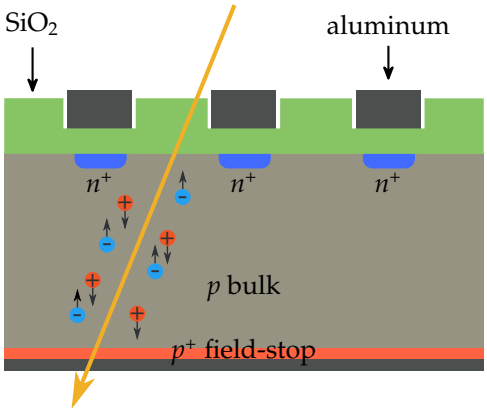


FIGURE 3.4: Signal generation in the space-charge region of a segmented p type silicon sensor by a passing charged particle. The generated electron-hole pairs drift in the electric field and induce a signal at the n^+ readout electrodes. Figure adapted from [44].

Consequently, the signal current does not depend on the electric field strength between the electrodes or the applied voltage. The electric field, however, does determine the signal shape. In particular, a higher electric field results in faster charge collection and, hence, a shorter signal pulse. Sensors are typically operated beyond full depletion voltage to improve charge collection time. Due to their differing mobilities, the signal shapes are distinctly different for electrons and holes. The electron signal is initially high and falls quickly as the electrons are collected at the n^+ electrode. The hole signal, in contrast, is initially lower and falls over a longer time because the holes move slower through the semiconductor. The total signal is given by a superposition of electron and hole signals, whereby the signal amplitude is determined by the number of generated electron-hole pairs.

The possible position resolution of a segmented silicon sensor is mainly determined by the type of data readout and the pitch p between strips or pixels. For digital readout, the position resolution is limited to

$$\langle \Delta x^2 \rangle = \frac{1}{p} \int_{-p/2}^{p/2} x^2 \mathrm{d}x = \frac{p^2}{12} \rightarrow \langle \Delta x \rangle = \frac{p}{\sqrt{12}} \,, \tag{3.19}$$

where x is the position of the particle track [41].

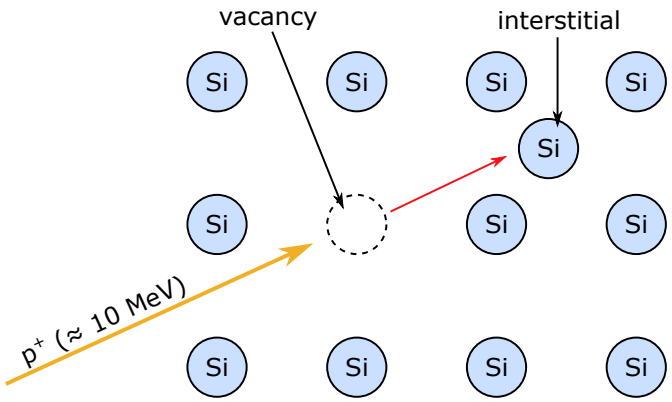
Analogue readout typically achieves better resolution because it makes use of charge sharing between multiple electrodes. Due to the diffusion of the charge cloud, the deposited charge is taken up by more than one electrode, and the position of the traversing particle can be found by interpolation, e.g., by calculating the center of gravity of the signal. In this case, the resolution is limited by the noise of the involved channels. It is proportional to the channel pitch and inversely proportional to the signal-to-noise ratio (SNR):

$$\langle \Delta x \rangle \propto \frac{p}{\mathrm{SNR}} \,, \tag{3.20}$$

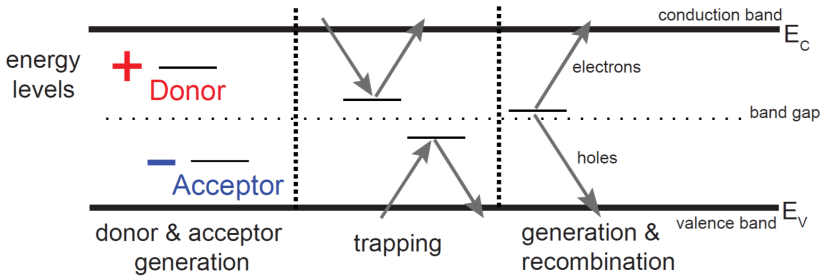
whereby the signal-to-noise ratio is defined as the ratio between signal and equivalent noise charge (ENC).

3.3 Radiation Damage

Apart from the wanted and mostly reversible effect of ionization due to traversing charged particles, interactions of energetic charged and neutral particles with the detector material can cause permanent damage that degrades the detector performance. In the following, a brief discussion of the most important defect mechanisms and their effects on sensor properties is given. For a more detailed account, the reader is referred to references [51–53].



(A) Vacancy and interstitial in the silicon lattice ("Frenkel defect").



(B) Different types of radiation induced defects in the silicon band gap. Figure taken from [53].

FIGURE 3.5: Microscopic defects in silicon caused by non-ionizing radiation. Point defects in the silicon lattice (A). Different types of defects in the forbidden band gap (B).

Radiation effects in silicon detectors are distinguished into bulk effects and surface effects. While bulk defects are mainly caused by heavy particles such as neutrons, protons, or pions, surface damage is mainly caused by photons and charged particles.

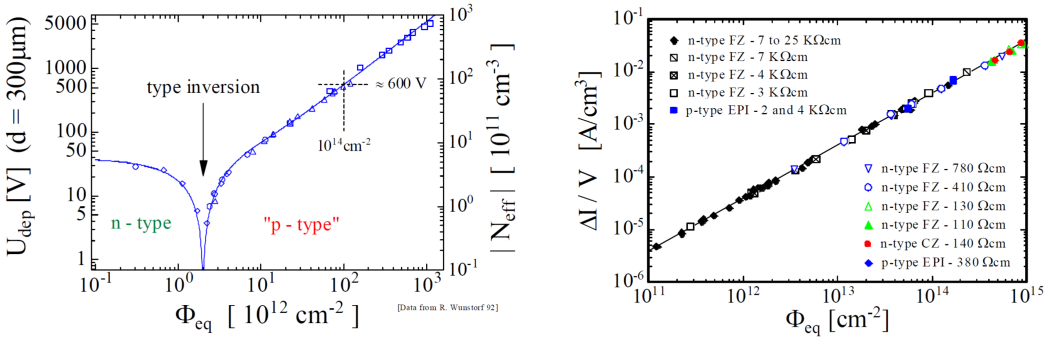
The main effect responsible for radiation damage in the silicon bulk are elastic collisions of heavy particles with the atomic nuclei of the crystal lattice. Depending on the transferred energy at the primary impact, the collisions can dislocate individual atoms, causing point defects, or cause a cascade of dislocations that result in a cluster defect.

If a lattice atom is knocked off its initial position, it creates a silicon interstitial and a left-over vacancy (Figure 3.5a). This basic defect is called a *Frenkel pair* [51]. At room temperature, both vacancy and interstitial can migrate through the lattice and either fall back to their initial positions (beneficial annealing) or form stable point defects with impurity atoms.

A way to quantify and scale the radiation damage caused by incident particles is provided by the *non-ionizing energy loss (NIEL) hypothesis* [51]. The main assumption of the NIEL hypothesis is that any radiation damage to a material due to lattice displacements is linear proportional to the non-ionizing energy loss of the traversing particles, which scales linearly with the energy transferred in displacing collisions (displacement energy). Consequently, the damage induced by different particles can be scaled using the NIEL hypothesis. It is common to scale the fluence Φ of any particle to the equivalent fluence Φ_{eq} of monoenergetic $1\,\mathrm{MeV}$ neutrons that would induce the same damage using

$$\Phi_{\mathrm{eq}} = \kappa \cdot \Phi \,, \tag{3.21}$$

with the hardness factor κ that essentially describes the severity of the damage induced by a



(A) Full depletion voltage and effective doping concentration as a function of the 1 MeV neutron equivalent fluence Φ_{eq}.

(B) Leakage current difference ΔI per volume as a function of the 1 MeV neutron equivalent fluence Φ_{eq} for samples with different resistivity and bulk polarity.

FIGURE 3.6: Effects of non-ionizing radiation on silicon sensor effective doping concentration (A) and leakage current (B). Figures taken from [54].

specific type of particle radiation [51].

3.3.1 Radiation Effects on Sensor Properties

Displacement defects in the lattice create additional energy levels in the forbidden band gap (Figure 3.5b). Shallow defects close to the edges of the band gap act as donors or acceptors, and result in a change of the effective doping concentration. Deep defects close to the center of the band gap, on the other hand, act as trapping centers or centers for generation-recombination processes. These microscopic defects have macroscopic effects on sensor properties.

In terms of shallow defects, irradiation mainly produces acceptor-like states and removes donor-like ones [41]. In n type silicon, this effect leads to a decrease of the effective doping concentration until, at a certain fluence, n type becomes p type and the effective doping concentration increases again (Figure 3.6a). Consequently, the full depletion voltage first decreases until, at *type inversion*, it reaches effectively zero and increases again under further irradiation. After inversion, the space-charge region grows from the opposite side than before irradiation for an originally n type sensor, and the sensor cannot be operated below full depletion voltage. In case of p type material, no type inversion occurs. However, the full depletion voltage increases with increasing particle fluence. The resulting high operation voltages pose a challenge for sensor power supplies and necessitate cooling measures to counteract power dissipation.

Deep level trapping centers negatively affect the charge collection efficiency, whereas generation-recombination centers cause an increase of the sensor leakage current (Figure 3.6b). The leakage current increase ΔI scales linearly with the particle fluence according to [51]

$$\Delta I = \alpha \Phi_{eq} V \,. \tag{3.22}$$

The proportionality factor α is denoted the *current-related damage rate* and is independent of material properties such as resistivity and polarity.

3.3.2 Surface Effects

Surface damage in silicon sensors is mainly caused by photons and charged particles that generate electron-hole pairs through ionization. Inside the semiconductor, the excess charge carriers can recombine or are swept off toward the electrodes and, consequently do not cause permanent damage. Ionization in the amorphous oxide on top of the sensor, however, leads to the increase of fixed oxide charges and interface traps, whereby the severity of the effect depends on the bias voltage applied to the oxide [55]. Positive oxide charges attract minority

electrons from the bulk of a *p* type sensor and, as the main consequence, affect the isolation between individual sensor channels.

A detailed discussion of radiation effects on SiO_2 and the Si-SiO_2 system can be found, e.g., in [56].

3.4 Manufacturing Process

Silicon sensors are manufactured by specialized semiconductor companies, utilizing the same processes and equipment that are used for the manufacturing of microelectronic devices. Companies use high-purity silicon wafers as base material. The wafers are cut from single crystal silicon ingots and, subsequently, undergo many different process steps such as lithographic structuring and edging, thermal diffusion, ion implantation, and sputtering.

In the following, crystal growth and the most important processing steps toward a finished silicon sensor are briefly discussed. A more in-depth account of semiconductor manufacturing techniques can be found in [40].

3.4.1 Silicon Crystal Growth

The starting material for silicon crystal growth is silicon dioxide (SiO_2) in the form of quartzite sand, which is chemically processed to acquire high-purity polycrystalline silicon also called electronic-grade silicon (EGS). From this high-purity base material, a single silicon crystal is grown.

Czochralski Technique

In the most commonly used technique for silicon crystal growth, the Czochralski technique, the single crystal is pulled from a melt of EGS. The EGS is melted inside a crucible, and a rotating silicon seed crystal is inserted into the melt and slowly withdrawn. At the liquid-solid interface, a single crystal grows. Rotation speed, temperature of the melt, and the pull speed are used to control the crystal growth. Dopants can be introduced into the EGS melt to achieve a doped ingot.

Float-Zone Process

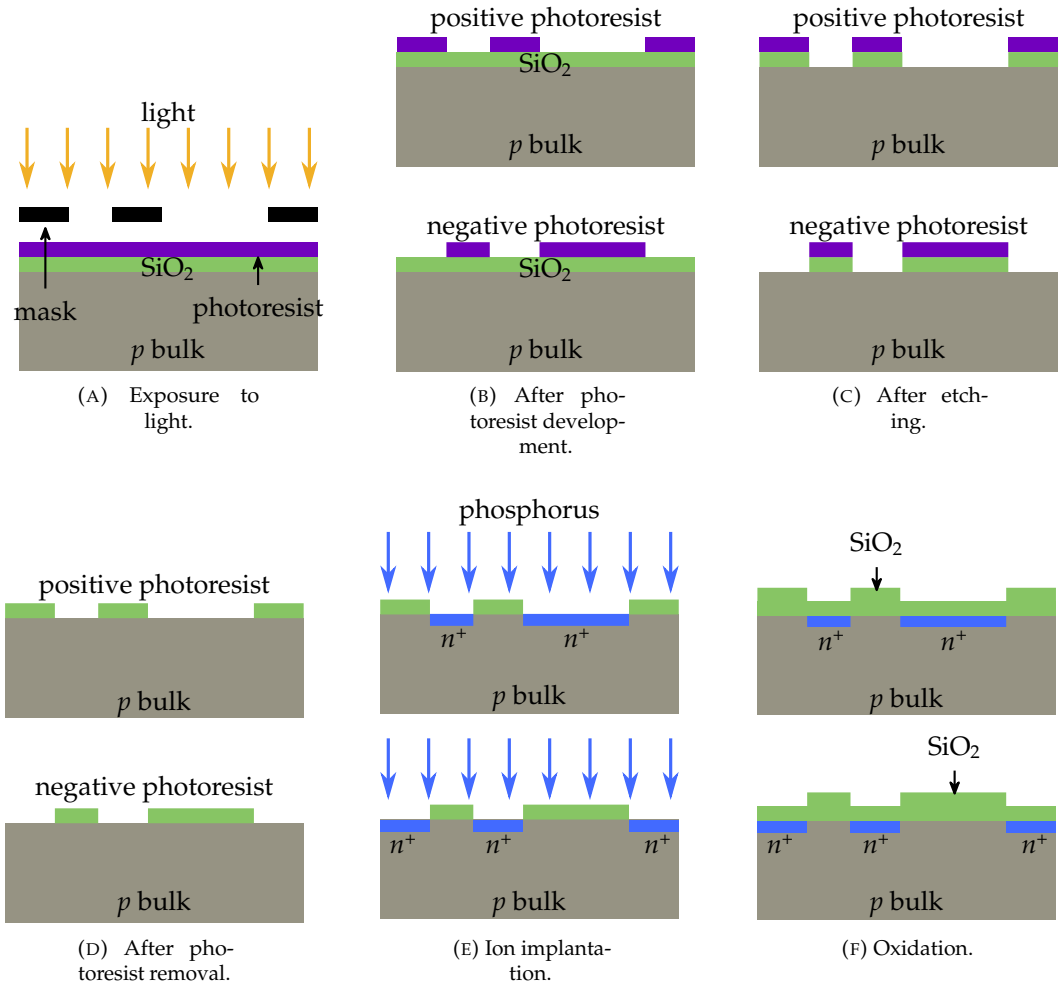
The float-zone process is used to achieve lower contaminations than those typically obtained from the Czochralski technique. A rotating high-purity polycrystalline silicon rod is contacted to a seed crystal at the bottom, and a small zone of the rod is melted with a radio-frequency (RF) heater. Starting at the seed crystal, the RF heater is slowly moved up along the rod causing it to melt locally. At the bottom end of the molten zone, a single silicon crystal grows. Impurities accumulate in the melt and move to the end of the rod along with the RF heater. For doping during crystal growth, dopants are added into the ambient gas volume.

Epitaxial Growth

Epitaxial growth is different from the above described crystal growth processes in that a substrate wafer acts as the seed crystal and growth happens at lower temperatures. Common techniques for epitaxial growth include chemical-vapor deposition (CVD) and molecular-beam epitaxy (MBE).

In case of CVD, the epitaxial layer forms on the substrate wafer from a chemical reaction between gaseous compounds. For silicon, commonly, silicon tetrachloride ($SiCl_4$) is used as the gaseous source for epitaxial growth. The dopant is introduced together with $SiCl_4$ in the gaseous phase. For *p* type doping, e.g., diborane (B_2H_6) is used.

MBE is a physical deposition process. One or more thermal atom or molecule beams react with the surface of the substrate wafer in ultrahigh vacuum. While MBE is a very precise deposition technique, growth rates are very slow ($\sim 1\,\mu\mathrm{m/h}$) [40].



(A) Exposure to light.

(B) After photoresist development.

(C) After etching.

(D) After photoresist removal.

(E) Ion implantation.

(F) Oxidation.

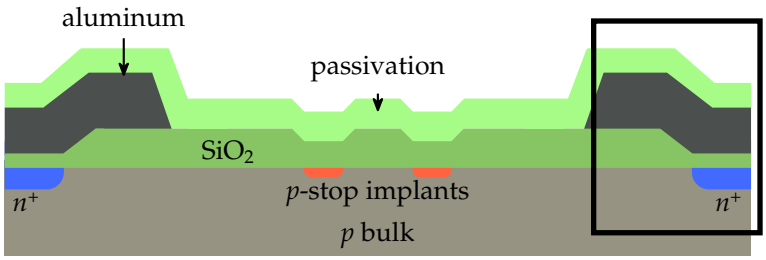
FIGURE 3.7: Schematic representation of the lithography and ion implantation process for positive and negative photoresist.

3.4.2 Wafer Processing Steps

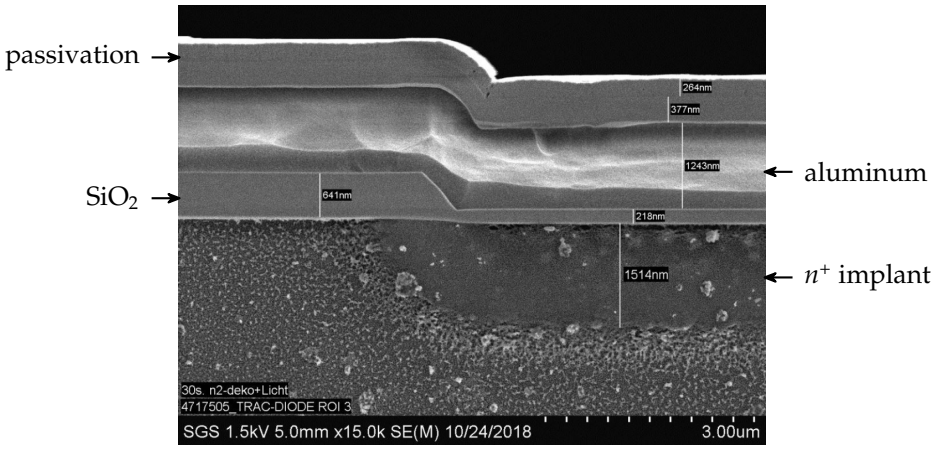
The raw wafer undergoes several process steps to produce silicon sensors and test structures. A detailed, step-by-step account of the production process of an n type silicon sensor is given, e.g., in [57].

The typical layer of SiO_2 at the surface of many semiconductor devices is formed by *thermal oxidation*. Oxygen reacts with the silicon surface in a furnace and forms SiO_2. The growing SiO_2 consumes part of the silicon surface, which alters the initial thickness of the silicon wafer. In particular, an oxide growth of thickness x consumes a layer of silicon that is $0.44x$ thick [40]. Typical oxide thicknesses are on the order of a few hundred nanometers.

The structuring of the wafer surface is achieved using *optical lithography*. A layer of a radiation-sensitive compound is uniformly deposited on the wafer surface. This so-called photoresist alters its solubility when exposed to radiation. One distinguishes positive and negative photoresists. While the solubility of a *positive photoresist* increases under radiation exposure, a *negative photoresist* decreases its solubility when exposed to radiation. The wafer with the photoresist coating is aligned with respect to a lithography mask and exposed to UV light (Figure 3.7a). Subsequently, the photoresist is developed (Figure 3.7b), which either dissolves the parts that were exposed to light (positive photoresist) or the parts that were not exposed (negative photoresist). After the development of the photoresist, the exposed SiO_2 layer is etched off (Figure 3.7c), and the photoresist is removed (Figure 3.7d). At this point, the wafer is ready for the introduction of further dopants.



(A) Schematic cross-section of the surface region between two n^+ electrodes, illustrating the variable thickness of the SiO_2 layer atop implanted and non-implanted regions. The black square marks the region magnified in (B).



(B) Electron microscopy image of an Outer Tracker prototype wafer, depicting the surface region around an n^+ implant as marked in (A) and featuring different oxide thicknesses.

FIGURE 3.8: Surface cross-section of a segmented silicon sensor after full processing. The schematic cross-section of the region between two n^+ electrodes (A) is compared to a close-up electron microscopy image of a single electrode (B).

Doping is achieved by *diffusion* or *ion implantation*. Often, both processes are applied in the fabrication of common microelectronic devices as they complement each other [40]. The achieved doping profiles vary depending on the doping method. Ion implantation is suitable for generating shallow junctions. It introduces energetic, charged particles into the silicon substrate (Figure 3.7e). The energy of the charged particles controls the implantation depth. After implantation (or diffusion), the wafer is *annealed* at high temperatures to activate the dopants, cancel defects introduced by ion bombardment, and restore key material parameters such as carrier mobility and lifetime.

After lithography and doping steps, the surface of the wafer may be oxidized again (Figure 3.7f), and the previous steps may be repeated to introduce regions with different doping polarity. In case of a p type silicon sensor, in the last oxidation step a thin, high-quality oxide layer is added atop n^+ implants, which serves as the coupling dielectric between implants and metal readout electrodes (see section 4.1.1). Consequently, the oxide layer atop a processed silicon wafer is not uniformly thick across the whole wafer surface (Figure 3.8).

In addition to the above described process steps, aluminum metallizations or polysilicon films may be added. Typically, the deposition of these or similar thin layers is achieved via chemical-vapor deposition or sputtering.

After processing, the wafer is sawed (also referred to as dicing) along pretreated dicing lines to obtain the finalized silicon sensor or microelectronic device.

Chapter 4

Silicon Sensors for the CMS Outer Tracker and HGCAL

The Phase-2 Upgrade of the CMS Outer Tracker and the CMS High Granularity Calorimeter (HGCAL) will encompass over $50\,000$ silicon sensors covering a total detector area of about $800\,\mathrm{m}^2$. Operation in the HL-LHC environment puts stringent constraints on silicon sensor material and design in terms of radiation tolerance and detector resolution [33, 37]. CMS has conducted extensive radiation campaigns to determine a suitable baseline material and decide on sensor layout parameters [34, 35]. Also, much expertise is drawn from experience with the sensors of the current CMS Tracker. Many a design feature of the Phase-2 Upgrade sensors has been tried and tested within the framework of the current Tracker, and the strategy employed to ensure the quality of the sensor material for the Phase-2 Upgrade has been adapted and extended from procedures that were already in place during the commissioning of the current CMS silicon tracker [57–59].

Because of its superior performance under irradiation in contrast to the *n* type material of the current CMS Tracker, which shown strong non-Gaussian noise after irradiation [34], the Phase-2 Upgrade will utilize *p* type silicon as detector baseline material for both the Outer Tracker and HGCAL. R&D and prototyping campaigns have been carried out with different manufacturing companies to evaluate the capabilities of the vendors to provide sensors that conform to CMS specifications and to finalize wafer layouts and process specifics, such as sensor active thickness and backplane processing technique. The prototyping phase was utilized to establish a dedicated quality assurance strategy that will be employed during series production to ensure that the delivered sensor material is suitable to be integrated into the detector.

Sensor production for the Outer Tracker started in 2020 and is expected to run until 2024. The start of the HGCAL series production is expected for 2021. During the full production time, every sensor will be pretested by the vendor, and, subsequently, a flexible subset of sensors from each delivered batch will be subjected to extensive tests, and the quality of the production process will be monitored on dedicated test structures. The individual tasks of this quality assurance procedure will be shared among test centers represented by various scientific institutions within the CMS Outer Tracker and HGCAL collaborations. On the basis of these tests, CMS will decide to accept or reject the full batch (assuming homogeneity of the material within a single batch). Eventually, only sensors from batches that are found to comply with preset specifications will be accepted for module assembly and subsequently integrated into the CMS detector.

This chapter discusses the design considerations for the silicon sensors of the CMS Outer Tracker and HGCAL, specifically with regard to spacial resolution, high voltage stability, sensor noise, and the interplay of these parameters, and introduces the quality assurance procedure the sensors will be subjected to. Finally, a section is dedicated to the wafer material that was produced for the CMS Outer Tracker and HGCAL, including prototyping and production batches. It covers process specifics and wafer layout of the material investigated as part of this thesis.

4.1 Sensor Design

The silicon sensors for the CMS Outer Tracker and High Granularity Calorimeter need to cope with the HL-LHC environment whilst producing high-quality, exploitable physics output. They must provide high spatial resolution and granularity to effectively resolve physics objects and contribute to the level-1 trigger, and they must withstand the radiation dose accumulated over the projected detector lifetime [33, 37]. To meet these requirements, the sensor design must factor in a large number of variables, e.g., material choices, sensor segmentation, signal-to-noise performance, operating conditions, radiation damage, expected sensor lifetime, and cost, but also account for means to test the sensor performance and radiation tolerance before the sensors are integrated into the detector.

The following sections discuss the basic design elements of silicon sensors and introduce the layout parameters of Outer Tracker and HGCAL sensors.

4.1.1 General Design Elements

Both, the CMS Outer Tracker and HGCAL, will utilize silicon sensors manufactured on high resistive *p* type substrate. Signal output and noise performance of *p* type material after irradiation have been shown to be superior to *n* type silicon [34, 35]. In particular, the investigated *n* type sensors showed strong non-Gaussian noise effects (i.e. fake hits) after irradiation related to high electric fields. The choice of *p* type silicon over *n* type material reflects on sensor design choices. In the following, some of the basic design elements of *n*-in-*p* type silicon sensors are discussed. While some elements are applicable for both *n* and *p* type sensors, others, as for example additional means for electrode isolation, are specific for *p* type sensors.

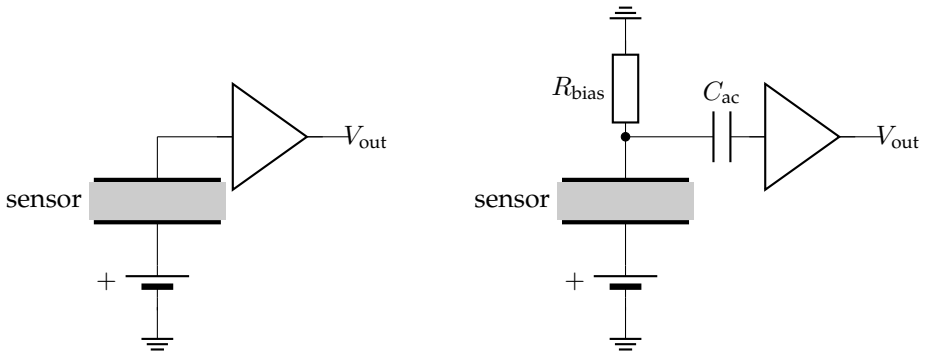
Signal Coupling

Current signals induced at the sensor electrodes by charged particles can be transferred to the readout electronics in two ways (Figure 4.1).

The *DC-coupled* configuration (Figure 4.1a) directly connects the sensor electrodes to the amplifiers of the readout chip. In this case, the AC current signal induced by the drift of generated charge carriers is transferred together with the DC sensor leakage current. While DC-coupling is easy to realize, it poses a challenge for readout electronics, especially in cases of high sensor leakage current because the amplifiers have to deal with the constant DC current component. The electronics requirements become limiting for sensors with high active thickness, large-area electrodes, and, particularly, after irradiation, which significantly increases the leakage current. Even if the amplifiers are able to sustain the high DC current, a DC-coupled readout configuration will impact the sensor signal-to-noise performance. DC-coupling is most feasible for sensors with small electrodes and negligible leakage current, as well as in cases where the expected signal is high compared to the sensor noise (e.g. pixel sensors with pixel sizes $\ll 1\,\mathrm{mm}^2$).

To decouple the DC sensor bias circuit from the readout amplifiers, a high-pass filter can be introduced in front of the amplifiers. The AC current signal then couples capacitively into the readout chip, and the DC bias current is shunted over dedicated bias resistors (Figure 4.1b). This method is referred to as *AC-coupling*. Generally, the decoupling of the circuits is realized directly on the sensor. A thin layer of high-quality silicon-dioxide (SiO_2) serves as the coupling dielectric between the n^+ implant and the aluminum readout electrode on top. Metal *contacts* to implanted sensor areas are routed through the oxide layer for testing purposes, biasing, and in case of DC-coupled readout. AC-coupled silicon strip sensors typically contain an AC-coupled readout electrode and an electrode with direct contact through the oxide for measurements of individual strip properties. In case of the Outer Tracker strip sensors, these electrodes are referred to as *AC-pad* and *DC-pad*, respectively.

The signal electrodes are connected to the readout chip hybrid via wire bonds in case of most silicon strip sensors. Hybrid pixel sensors generally realize the connections between sensor and readout chip via bump bonding, while active monolithic pixel sensors integrate CMOS readout electronics into the sensing devices. The CMS Outer Tracker strip sensors and HGCAL sensors employ wire bonds, while the CMS Outer Tracker macro-pixel sensors are bump bonded to the readout hybrid.



(A) DC-coupled readout. (B) AC-coupled readout.

FIGURE 4.1: Sensor signal circuit and readout schematics. In case of DC-coupled readout (A), the sensor DC current and the AC signal are directly transferred to the readout amplifier. The AC-coupled configuration (B) decouples the sensor DC current from the AC readout signal via the coupling capacitor C_{ac}. The sensor bias current is shunted over the resistor R_{bias}. The decoupling elements C_{ac} and R_{bias} are part of the sensor.

Sensor Bias

To deplete the active volume of a silicon sensor, the necessary bias potential difference has to be applied between front and back electrodes. Typically, ground potential is applied to the readout electrodes at the sensor front, and the sensor backplane is set to high potential. To provide a good ohmic connection between the backside metalization and the silicon substrate, the backplane features a region of low resistivity p^+ doping. This region is also referred to as *field-stop* because it prevents high electric field densities from reaching the sensor backplane and causing avalanche breakdown in case of over depletion.

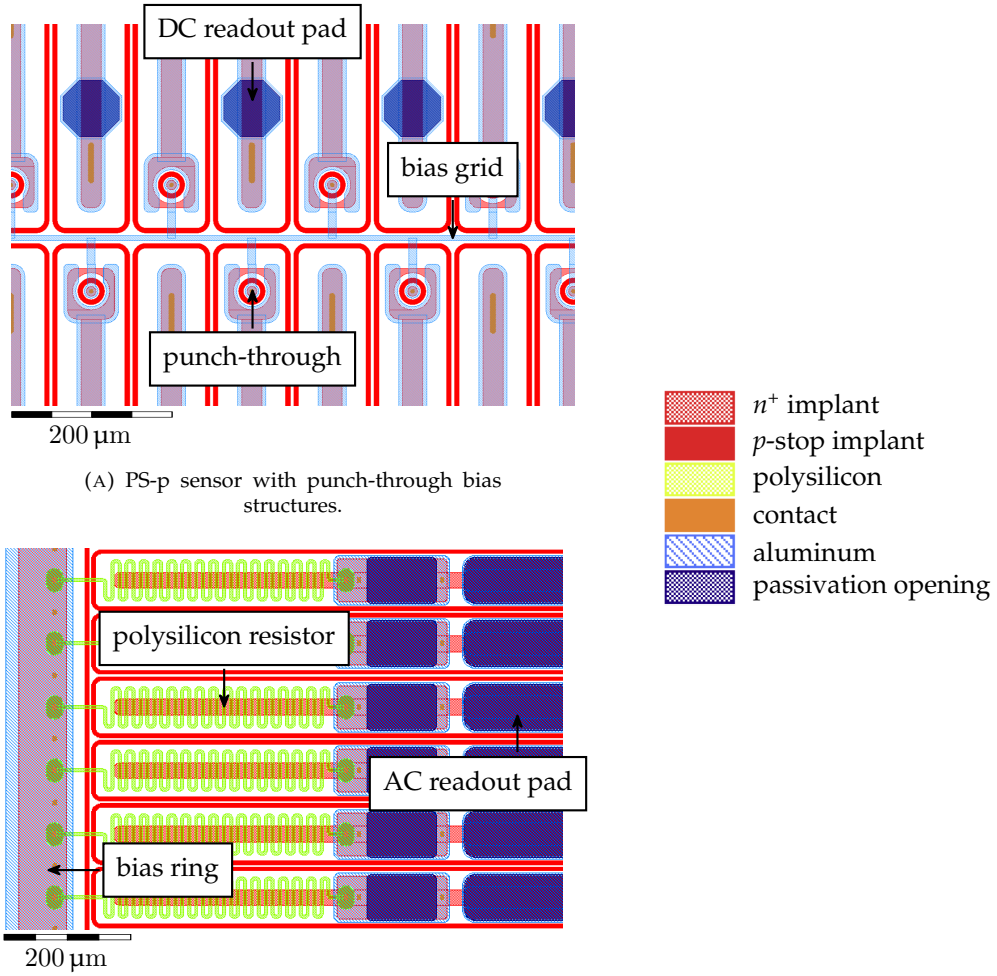
In case of DC-coupled sensor readout, the bias ground potential is supplied to each individual electrode via the readout chip. This configuration, however, requires additional means to bias the sensor during testing, when the sensor has not yet undergone module assembly and is thus not connected to the readout chip. The macro-pixel sensors of the CMS Outer Tracker feature a common bias grid that allows to provide the bias potential to all pixels via *punch-through* structures (Figure 4.2a). The HGCAL sensors, in contrast, do not include a common biasing structure. During testing, the bias potential is provided to all sensor cells with a dedicated probe card and switching matrix system [60].

AC-coupled strip sensors are commonly biased via *polysilicon resistors* (Figure 4.2b). These structures, made of doped polycrystalline silicon, connect every individual strip to a common n^+ bias line that surrounds all sensor strips and is referred to as *bias ring*. The resistance value of the bias resistors is an important parameter that influences the sensor performance. The resistors serve to electrically isolate the sensor strips and act as current limiter in case of individual strips with high leakage current or beam-loss scenarios, during which the sensors are exposed to high particle flux that induces high currents in the sensors. Additionally, exposure to high radiation doses effectively decreases the inter-strip resistance. To ensure strip isolation in high radiation environments, the inter-strip resistance must remain significantly higher than the polysilicon bias resistance. Typical polysilicon resistance values are on the order of $1\,\mathrm{M\Omega}$. The absolute value can be adjusted via implantation dose and length-to-width ratio of the polysilicon structures. Typically, the structures are realized with a meandering shape to achieve higher resistance values.

High Voltage Stability

To ensure a sufficiently high signal-to-noise ratio, the silicon sensors must be operated at or beyond full depletion. For the sensors in the high radiation environment of the HL-LHC, this means operation voltages $> 600\,\mathrm{V}$ near the end of the designated detector lifetime[1]. It is

[1] In individual cases, operation voltages up to $800\,\mathrm{V}$ are foreseen.



(A) PS-p sensor with punch-through bias structures.

(B) PS-s sensor with polysilicon bias resistors.

FIGURE 4.2: Layout closeup of Outer Tracker sensors, illustrating the differences between the AC-coupled PS-s (A) and the DC-coupled PS-p (B) processes. Figures adapted from [13].

thus absolutely crucial that the sensors can sustain the necessary operation voltages without running into breakdown.

The critical electric field strength for avalanche breakdown in the sensor is determined by the doping concentration of the silicon substrate and is about $300\,\mathrm{kV/cm}$ for high resistive silicon (i.e. $\rho \geq 1\,\mathrm{k\Omega\,cm}$) [40]. Junctions with sharp corners (i.e. small corner radii) and acute angles cause local peaks of the electric field strength that may exceed the critical field and lead to micro-discharge effects[2] and premature breakdown. Sensor design must avoid such configurations wherever possible. For the CMS silicon sensors, every implant corner is designed with a radius $r \geq 5\,\mu\mathrm{m}$ and all metal electrodes are extended by at least $5\,\mu\mathrm{m}$ beyond the implantation region below. The latter design measure is referred to as *metal overhang* and extends the high electric field densities at the metal edges out into the oxide and away from electrode implants, where they could promote micro-discharge.

Crystal impurities and damages that promote breakdown are most prevalent at the sensor edges. They are introduced when the sensor is cut out of the wafer (i.e. dicing). To protect the sensor against these defects, a ring of p^+ implantation surrounds the sensor along its edges. Similarly to the function of the backplane field-stop, this so-called *edge ring* prevents the space charge region from extending beyond the implanted region and reaching any defects at the sensor edges. Additionally, the p^+ implant prevents surface currents across the dicing region. As a side effect of this configuration, a conductive interconnection is formed between the sensor backplane and the edge ring. The connection allows to apply the high voltage bias from the sensor front by contacting the edge ring (i.e. front-side biasing [61]), which is helpful if the sensor backside needs to be protected during testing. Pulling high potential to the sensor front, however, introduces a potential gradient between the p^+ edge ring and the n^+ implants that can promote breakdown if the distance between p^+ and n^+ regions becomes too narrow. As a countermeasure, one or more n^+ *guard rings* are introduced between sensor n^+ electrodes and edge ring. During operation, the floating guard ring forms the lateral electric field and decreases the potential gradient at the sensor periphery. The Outer Tracker and HGCAL sensors include two guard rings: an inner guard ring that is kept on ground potential and functions as bias ring in case of the Outer Tracker sensors, and an outer ring on floating potential that acts as the field forming guard ring.

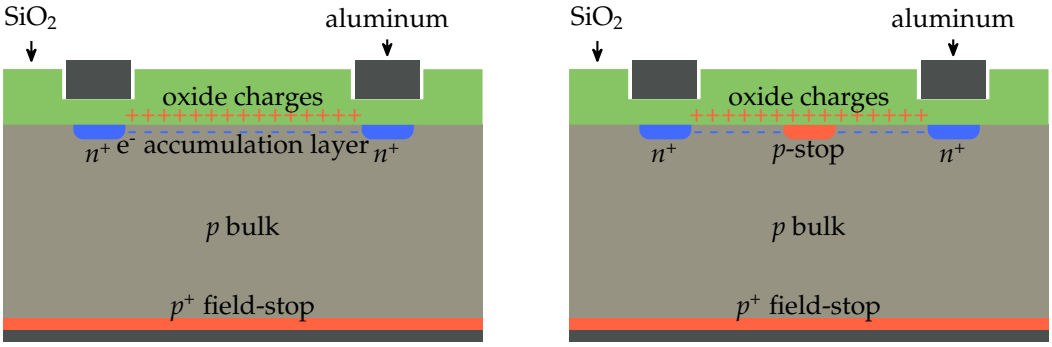
A higher concentration of fixed positive charges in the oxide reduces the electric field strength in underlying p type silicon bulk and, hence, is beneficial for the high voltage stability of n-in-p sensors [34, 62]. However, a high fixed oxide charge concentration has negative consequences on the inter-channel resistance and the presence of the oxide charges necessitates special measures for electrode isolation. In turn, the measures for electrode isolation as well as the dimensioning of the inter-channel region affect the sensor high voltage stability. The following sections discuss these aspects in more detail.

Electrode Isolation

To ensure accurate position resolution, individual sensor electrodes have to be electrically isolated from each other. Initial resistances between electrodes should be well beyond $10\,\mathrm{G\Omega\,cm}$ to allow for sufficient isolation also after irradiation. In case of p^+ type electrodes embedded in n type substrate (p-in-n sensors), electrode isolation is achieved by default. Sensors based on n^+ electrodes implanted in p type substrate (p-in-n sensors), in contrast, do not automatically achieve electrode isolation. Positive fixed charges in the silicon-dioxide layer attract minority carrier electrons from the p type bulk to the Si-SiO_2 interface. This process creates an electron accumulation layer at the sensor surface that effectively shortens the n^+ electrodes (Figure 4.3a). To achieve electrode isolation for n-in-p sensors, the electron accumulation layer must be interrupted.

P^+ implants between the n^+ electrodes serve to disrupt the electron layer at the sensor surface. If the p^+ doping is applied uniformly across the whole wafer, the method is referred to as *p-spray*. The p-spray method does not require additional lithography masks and is comparatively cheap. However, the uniform p^+ implantation increases the risks of high

[2]Micro-discharge refers to localized high field strengths causing avalanche multiplication of thermally generated charge carriers that may lead to sensor breakdown if the applied voltage is too high. Aside from premature breakdown, local micro-discharge effects can also mimic the signal generated by a traversing particle, which manifests as non-Gaussian noise tails [34].



(A) Electron accumulation layer forming between n^+ implants because of positive oxide charges.

(B) *P*-stop electrode isolation.

FIGURE 4.3: Schematic cross section of an AC-coupled *p*-in-*n* sensor illustrating the concept of electrode separation. Positive oxide charges attract electrons from the silicon bulk that form a conductive interconnection between individual n^+ implants (A). The n^+ implants can be isolated from each other by introducing a *p*-stop implant in-between (B). Figures adapted from [44].

electric field densities at the junctions with the n^+ electrodes. Also, the exact implantation dose is crucial and not easy to control during manufacturing.

Alternatively, localized areas of p^+ implantation that surround and separate the individual n^+ electrodes can be introduced. This method is referred to as *p-stop* (Figure 4.3b). It requires an additional lithography mask during production but reduces the risk of high lateral electric field densities.

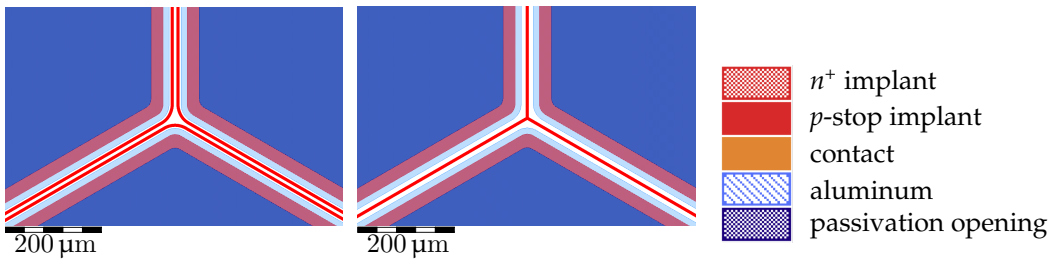
P-stop layout, doping concentration, and implantation depth influence the resistance and the electric field configuration between neighboring electrodes and affect the sensor performance after irradiation [62]. The *p*-stop process parameters have to be selected carefully to achieve certain resistance values [34]. The doping concentration must be high enough to prevent effective shorts between electrodes after irradiation. On the other hand, it has been shown [63, 64] that concentrations above $1 \times 10^{17}\,\mathrm{cm}^{-3}$ might lead to excessive electric field densities at the *p*-stop implants that could promote avalanche breakdown and degrade sensor performance. With regard to high voltage stability, thin *p*-stop implants [65] and a large distance between *p*-stop and n^+ implant [62, 65] have been found to be beneficial.

All CMS Outer Tracker and HGCAL sensors utilize *p*-stop implants for electrode isolation. The Outer Tracker sensors employ a *p*-stop configuration, referred to as *p-stop atoll*, where each individual strip or pixel is surrounded by a separate *p*-stop ring and another ring separates the collective of strips or pixels from the bias ring. The *p*-stop implants are positioned such that the distance between *p*-stop and n^+ implant edge is kept as large as possible. With regard to production specific design constraints, this leaves a *p*-stop width of $6\,\mu\mathrm{m}$ with a gap of $4\,\mu\mathrm{m}$ between adjacent *p*-stops [33].

For the HGCAL project, two different *p*-stop layouts are produced (Figure 4.4): a version, referred to as *p-stop atoll* or *p-stop individual* (Figure 4.4a), where every cell is surrounded by an individual *p*-stop ring and a larger ring separates the cells and the inner guard ring, and a layout version, referred to as *p-stop common* (Figure 4.4b), where the individual cells and the inner guard ring are separated by a common *p*-stop grid. *P*-stop width and distance in case of the individual configuration have been chosen identical to the values of the CMS Outer Tracker sensors. The decision which *p*-stop layout eventually will be used in the detector will be made according to the performance of the produced prototype material.

Inter-Channel Dimensioning

The dimensioning of the sensor layout between strips, pixels, or cells has significant influence on the noise load for the readout chip and on the high voltage stability of the sensor.



(A) *P*-stop individual.

(B) *P*-stop common.

FIGURE 4.4: HGCAL *p*-stop layout configuration between three neighboring cells. The *p-stop individual* layout version (A) encircles every sensor cell with an individual *p*-stop implant, while the *p-stop common* version (B) realizes cell separation via a common *p*-stop grid between the cells.

The intrinsic amplifier noise scales with the capacitive load. The total capacitance of a sensor channel is composed of the capacitance between the channel and the sensor backplane (i.e. backplane capacitance) and the capacitance between the channel and its neighbors (i.e. inter-channel capacitance)[3]. These two components have different impact on the total capacitance depending on the channel layout. If the area of the channel (i.e. by approximation the area of the n^+ implant) is large compared to the circumference, the backplane component dominates. Whereas, if the relative influence of the circumference increases, the inter-channel capacitance dominates the total capacitance.

The latter situation holds for both, the CMS Outer Tracker strip and macro-pixel sensors. In this case, the total capacitance is largely governed by the width-to-pitch ratio w/p of strips or macro-pixels and becomes lower for small values of w/p [66]. In case of the HGCAL sensors, on the other hand, $w/p \sim 1$ and the total capacitance is governed by the backplane capacitance. While, even in this case, different cell distances do effect the inter-cell capacitance, the absolute contribution to the total capacitance remains small [37].

With regard to inter-channel dimensioning, maximizing the high voltage stability of the sensor presents as somewhat of an antithesis to minimizing the capacitive load of the amplifier. While the inter-channel capacitance decreases with lower width-to-pitch ratio, the sensor breakdown voltage increases with a higher ratio [33]. The eventual layout decision comes down to a trade-off between high voltage stability and capacitive load. For the CMS Outer Tracker sensors, a ratio of $w/p = 0.25$ was chosen as it presents a satisfactory compromise [33, 66]. For HGCAL sensors, in contrast, considerations regarding the capacitance play a less significant role for the inter-channel layout than high voltage stability and the avoidance of non-Gaussian noise. The HGCAL inter-cell distance and the *p*-stop layout have yet to be decided, taking into account inter-cell resistance, high voltage stability, and non-Gaussian noise, particularly after irradiation.

Passivation

To protect the sensor from environmental influences and damage and to electrically isolate the structures at the sensor front, a passivation layer covers the top of the sensor. Typical materials used for passivation include silicon dioxide (SiO_2), silicon nitride (Si_3N_4), and phosphor silicate glass (PSG) [67]. Openings etched into the passivation layer allow to contact the aluminum electrodes for sensor readout, biasing, and electrical tests. The placement of the passivation openings accommodates to the requirements of module assembly and considerations of high voltage stability. Openings are placed such that paths for wire bonding to the readout hybrids are kept short. Openings above structures that lie on different electrostatic potentials during operation (e.g. p^+ edge ring and n^+ guard rings) should be kept far apart to avoid sparking.

[3]These components are also referred to as planar capacitance and edge capacitance (see section 6.1.3).

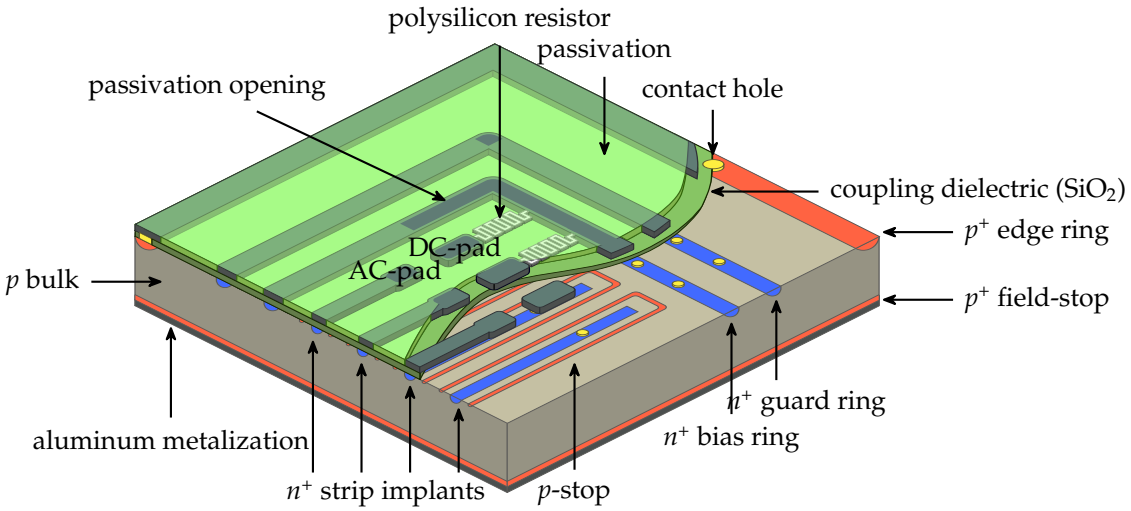


FIGURE 4.5: 3D model of an AC-coupled n-in-p silicon strip sensor (not to scale). The labeled components are described in section 4.1.1. Figure adapted from [68].

4.1.2 Outer Tracker Silicon Strip Sensors (2S and PS-s)

The Outer Tracker of CMS includes two types of AC-coupled silicon strip sensors: the larger 2S sensor, which will be implemented in the 2S modules in the outer part of the Outer Tracker (i.e farther away from the interaction point), and the smaller PS-s sensor, which will be part of the PS modules in the inner part of the Outer Tracker. Both types of strip sensors share the same general design features (Figure 4.5). Their layout parameters (Table 4.1) are identical except for the outer dimensions and strip geometry [33].

The 2S sensor measures about $10 \times 10\,\mathrm{cm}^2$ and consists of 1016 parallel strips that are segmented into two approximately $5\,\mathrm{cm}$ long strips each, resulting in a total of 2032 channels. The strip pitch is $90\,\mu\mathrm{m}$. PS-s sensors, with a size of $10 \times 5\,\mathrm{cm}^2$, are about half as large. Every PS-s sensor consists of 960 strips segmented into two $2.35\,\mathrm{cm}$ long strips each and a pitch of $100\,\mu\mathrm{m}$. The width-to-pitch ratio of 0.25 is the same for both sensor types.

2S and PS-s sensors share a common periphery layout that is also identical for the Outer Tracker macro-pixel sensor (PS-p). A $75\,\mu\mathrm{m}$ wide n^+ bias ring with asymmetric metal overhangs encircles the active sensor area. The bias ring accommodates passivation openings for wire bonding and testing and the contacts to the polysilicon bias resistors. At an implant distance of $70\,\mu\mathrm{m}$, a floating guard ring with asymmetric metal overhangs and passivation openings in the corners surrounds the bias ring to improve high voltage stability. An at least $500\,\mu\mathrm{m}$ wide p^+ edge ring encircles the sensor at the outer edges to ensure a well-defined depletion region and protect against imperfections along the dicing lines. The edge ring metalization houses alignment marks and the counter-clockwise strip numbering.

At the end of each strip, a small probe pad with direct contact to the n^+ implant (DC-pad) is located. Widened parts of the strip metalization with opened passivation (AC-pads) serve as contact areas for wire bonding and strip readout. For easy contacting, all pads are at least $62\,\mu\mathrm{m}$ wide. The strip metalization extends $5\,\mu\mathrm{m}$ beyond the strip implant on all sides. P-stop rings of $6\,\mu\mathrm{m}$ width and $4\,\mu\mathrm{m}$ distance between adjacent p-stops surround each individual strip, and an additional p-stop ring separates the active sensor area from the bias ring (compare Figure 4.1b).

4.1.3 Outer Tracker Silicon Macro-Pixel Sensor (PS-p)

The layout parameters of the Outer Tracker macro-pixel PS-p sensor (Table 4.2) are largely identical to those of the PS-s sensor. For easy alignment of the PS-s and PS-p sensors during module assembly, the PS-p sensor is $300\,\mu\mathrm{m}$ wider than the PS-s sensor on each side so

TABLE 4.1: Layout parameters for the Outer Tracker strip sensors. The sensor length is defined as the dimension parallel to the strips.

Parameter	2S	PS-s
Length	102 700 µm	49 160 µm
Width	94 183 µm	98 140 µm
Strip pitch	90 µm	100 µm
Width-to-pitch ratio	0.25	0.25
Strip length	50 300 µm	23 500 µm
Number of strips	(2 × 1016)	(2 × 960)
P-stop width	6 µm	6 µm
Width of bias ring implant	75 µm	75 µm
Width of guard ring implant	40 µm	40 µm
Minimum width of edge ring implant	500 µm	500 µm
Distance bias ring to guard ring	70 µm	70 µm
Distance guard ring to edge ring	300 µm	300 µm
Metal overhang strips	5 µm	5 µm
Inner metal overhang bias ring	10 µm	10 µm
Outer metal overhang bias ring	20 µm	20 µm
Inner metal overhang guard ring	20 µm	20 µm
Outer metal overhang guard ring	50 µm	50 µm
Inner metal overhang edge ring	50 µm	50 µm

that the alignment marks on the edges are still visible with the PS-s sensors situated on top. The pixel pitch of $100\,\mu\mathrm{m}$ is the same as the strip pitch of the PS-s sensor, but the strips are segmented into 32 rows of $100 \times 1467\,\mu\mathrm{m}^2$ DC-coupled macro-pixels. Each macro pixel features a metal overhang of $5\,\mu\mathrm{m}$ and includes a hexagonal bump bond pad with a $70\,\mu\mathrm{m}$ wide passivation opening. The individual pixels are encircled by *p*-stop structures with identical dimensions as for the Outer Tracker strip sensors and are connected to the common bias grid via punch-through structures (compare Figure 4.1a). The two neighboring pixels situated at the corners of every MPA readout chip [69] are merged into a single pixel with size $200 \times 1467\,\mu\mathrm{m}^2$ to allow for signal collection in areas that would otherwise be located below inactive areas of the readout chips [33].

4.1.4 HGCAL Silicon Pad Sensors

The CMS High Granularity Calorimeter [37] will employ planar, DC-coupled, hexagonal *n*-in-*p* silicon pad sensors manufactured on $8''$ wafers. The hexagonal shape was chosen because it is the largest tileable polygon and efficiently exploits the circular wafer area, which significantly reduces the overall production costs. To accommodate space for the mounting and fixation system, the hexagons feature truncated tips referred to as "mouse-bites". Aside from the full-size hexagonal sensors, the production will also include sensor partials that represent cut parts of the original hexagon needed to fill out the edges at the wedge-shaped subassembly modules ("cassettes") of the calorimeter.

The sensors will come in three different active thicknesses ($300\,\mu\mathrm{m}$ and $200\,\mu\mathrm{m}$ produced on float-zone wafers, and $120\,\mu\mathrm{m}$ utilizing an epitaxial production process) and two different cell granularities, namely, a low density (LD) layout with 192 cells and a high density (HD) layout with 432 cells, accounting for regions of different fluence within the detector volume. LD and HD layout parameters are largely identical (Table 4.3) except for the cell size and the resulting shapes of cells at the sensor edges.

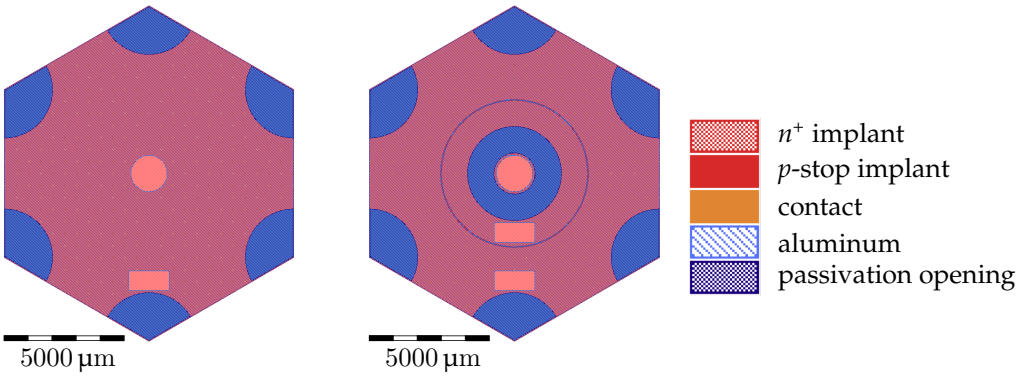
The active sensor elements are individual hexagonal DC-coupled diodes (Figure 4.6) with approximate areas of $1.18\,\mathrm{cm}^2$ (LD) and $0.52\,\mathrm{cm}^2$ (HD). In addition to the hexagonal standard cells (Figure 4.6a), the sensors include a number of smaller circular cells with lower capacitance for MIP calibration (Figure 4.6b). The LD design includes six calibration cells; the HD design includes 12. To improve high voltage stability, the metalization of each cell extends $12.5\,\mu\mathrm{m}$ on all sides beyond the n^+ implant. Every cell includes passivation openings at every corner to enable wire bonding to the readout board ("hexaboard") and contacting

TABLE 4.2: Layout parameters for the Outer Tracker macro-pixel sensor. The sensor length is defined as the dimension parallel to the long edge of the macro-pixels.

Parameter	PS-p
Length	49 160 µm
Width	98 740 µm
Pixel width	100 µm
Pixel width (edge cells)	200 µm
Pixel cell length	1467 µm
Number of pixels	(32×960)
P-stop width	6 µm
Width of bias ring implant	75 µm
Width of guard ring implant	40 µm
Minimum width of edge ring implant	500 µm
Distance bias ring to guard ring	70 µm
Distance guard ring to edge ring	300 µm
Metal overhang pixels	5 µm
Inner metal overhang bias ring	10 µm
Outer metal overhang bias ring	20 µm
Inner metal overhang guard ring	20 µm
Outer metal overhang guard ring	50 µm
Inner metal overhang edge ring	50 µm

TABLE 4.3: Layout parameters for the full-size HGCAL sensors, comparison of low-density (LD) and high-density (HD) layout. The quoted total numbers of cells include calibration cells.

Parameter	LD		HD	
Total sensor area	1 561 880	mm^2	1 561 880	mm^2
Size of full cell	118	mm^2	52	mm^2
No. of cells	198		444	
No. of calibration cells	6		12	
Inter-cell distance	50	µm	50	µm
P-stop width	6	µm	6	µm
Width of inner guard ring implant	131.5	µm	131.5	µm
Width of outer guard ring implant	18	µm	18	µm
Minimum width of edge ring implant	400	µm	400	µm
Distance guard rings	44.5	µm	44.5	µm
Distance guard ring to edge ring	209.5	µm	209.5	µm
Metal overhang cells	12.5	µm	12.5	µm
Inner metal overhang inner guard ring	12.5	µm	12.5	µm
Outer metal overhang inner guard ring	10	µm	10	µm
Inner metal overhang outer guard ring	10	µm	10	µm
Outer metal overhang outer guard ring	50	µm	50	µm
Inner metal overhang edge ring	50	µm	50	µm



(A) Standard sensor cell.

(B) Calibration cell.

FIGURE 4.6: Cell layout of the 192-cell HGCAL sensor. Standard cells are hexagonal (A). For signal calibration, a number of hexagonal cells contain smaller, circular cells (B). Because of their smaller size, the calibration cells are less affected by capacitance related parts of electronic noise and are thus well suited for MIP signal calibration.

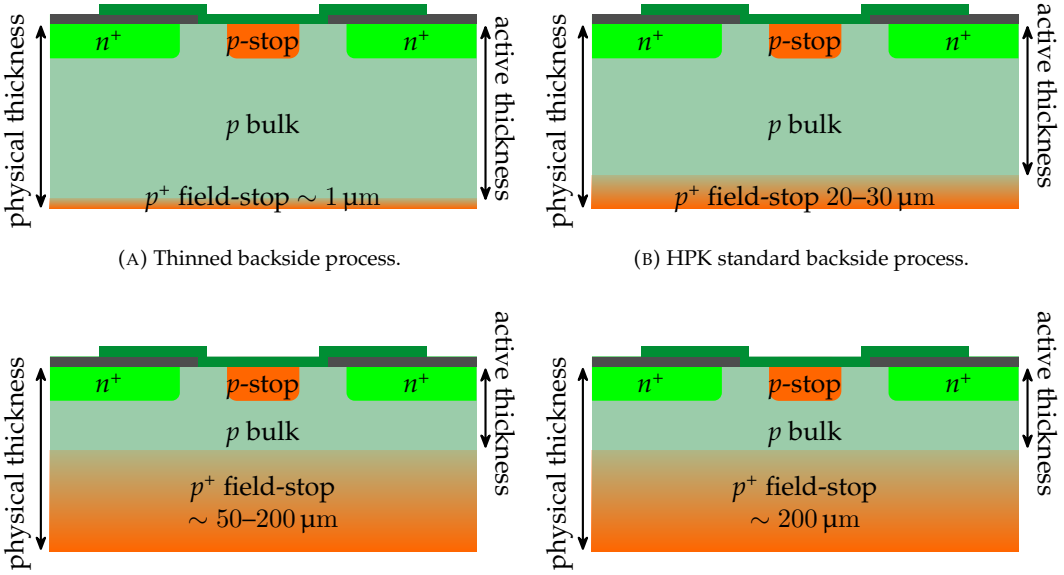
during sensor testing. Cell n^+ implants are spaced at $50\,\mu\mathrm{m}$ distance. The dimensioning of the p-stop cell isolation is identical to the Outer Tracker design. However, the final decision between common and individual layout variants (compare Figure 4.4) has yet to be made. In contrast to the DC-coupled macro-pixels of the CMS Outer Tracker, the HGCAL cells are not connected to a common biasing structure. This feature reduces complexity but necessitates additional measures for sensor testing (see section 4.3.1) and mitigation of cell breakdown effects at module level.

The periphery of the HGCAL sensors is based on the design of the Outer Tracker sensors, but absolute dimensions differ slightly. Two guard rings with asymmetric metal overhangs surround the active sensor area. During operation, the inner guard ring is kept on ground potential while the outer guard ring is floating to ensure high voltage stability. Finally, the sensor is surrounded by a p^+ edge ring that ensures a well-defined depletion region and protects the dicing lines from electric fields. The most recent design iterations of the HGCAL sensors include extensions to the inner guard ring and edge ring. These extensions take away some of the active sensor area but are required for sensor testing. Because $300\,\mu\mathrm{m}$ and $200\,\mu\mathrm{m}$ thick sensors only feature a thin field-stop region at the back, which is related to the $8''$ process (see section 4.2), they are sensitive to scratches at the backside introduced during handling, which cause early breakdowns of individual sensor cells. The issue has to be mitigated by protection of the sensor backside during testing, which necessitates measures to provide the bias voltage from the sensor front [70].

4.2 Wafer Material

All wafers discussed in this thesis were produced by the semiconductor manufacturers *Infineon Technologies AG* (IFX) and *Hamamatsu Photonics K.K.* (HPK). The investigated material includes prototype wafers intended for R&D purposes and the final production material for the CMS Outer Tracker. The R&D material varies in terms of active thickness and backside processing. Additionally, some wafer batches feature different process variations within a batch and different p-stop lithography masks in case of the HGCAL wafers.

To reach the target active thickness, the manufacturers employ different processing techniques for the field-stop implant at the wafer backside (Figure 4.7). However, neither manufacturer discloses details about the process steps. Infineon wafers generally feature a thin (i.e. $\sim 1\,\mu\mathrm{m}$) field-stop implant at the backside (Figure 4.7a). After front side processing, the wafer is physically *thinned* to the target thickness, and the field-stop implant is added. The Hamamatsu $6''$ *standard* material, in contrast, does not undergo backside thinning. It is



(A) Thinned backside process.

(B) HPK standard backside process.

(C) Deep diffused backside process.

(D) Epitaxial process.

FIGURE 4.7: Backside processing methods on p type sensors (schematic not to scale). The wafer is thinned to the target active thickness, and a thin backside field-stop implant of $\sim 1\,\mu m$ is added (A). The HPK standard material features a 20–30 µm thick field-stop implant (B). Low active thickness is achieved via a deep diffused backside implant (C) or via epitaxial growth of low resistive silicon on a high resistivity carrier wafer (D).

320 µm thick and features a 20–30 µm thick field-stop implant, yielding an active thickness between 290 µm and 300 µm (Figure 4.7b). The backside implant of *deep diffused* wafers (Figure 4.7c), in contrast, is much thicker (up to 200 µm) and is used to achieve low active thicknesses on wafers with high physical thickness. On 8″, the Hamamatsu standard material with 20–30 µm thick field-stop implant is not available. Instead, wafers with 300 µm and 200 µm active thickness are physically thinned to the target thicknesses after front side processing, similar to the Infineon process. Hamamatsu achieve low active thicknesses of 120 µm via an *epitaxial* process where high resistive silicon is grown on a carrier wafer with low resistivity (Figure 4.7d).

The layout is qualitatively similar for all wafers (Figure 4.8). The sensors take up the main (usually central) part of the wafer to minimize production costs and maximize the active detector area. Otherwise empty parts of the wafer (i.e. predominantly at the wafer periphery) contain test structures and mini sensors that are intended for quality assurance and irradiation tests. Due to their shape after dicing, the wafer cutoffs containing test structures and mini sensors are referred to as "halfmoons".

The following sections provide an overview on design and production specifics of prototype and production wafers for the CMS Outer Tracker and High Granularity Calorimeter. The quoted lists of wafer material are not intended to be comprehensive but to highlight the different types of produced wafers and to provide context for the results presented in later chapters of this thesis.

4.2.1 Outer Tracker

The silicon material produced to date for the CMS Outer Tracker includes R&D and production batches of predominantly 6″ wafers with active thickness ranging between 200 µm and 300 µm (Table 4.4).

Infineon Technologies produced six prototyping batches. Every batch comprises between 14 and 25 individual wafers that feature different process variations, including but not limited to p-stop implantation dose and diffusion time, front side spray implantation, back

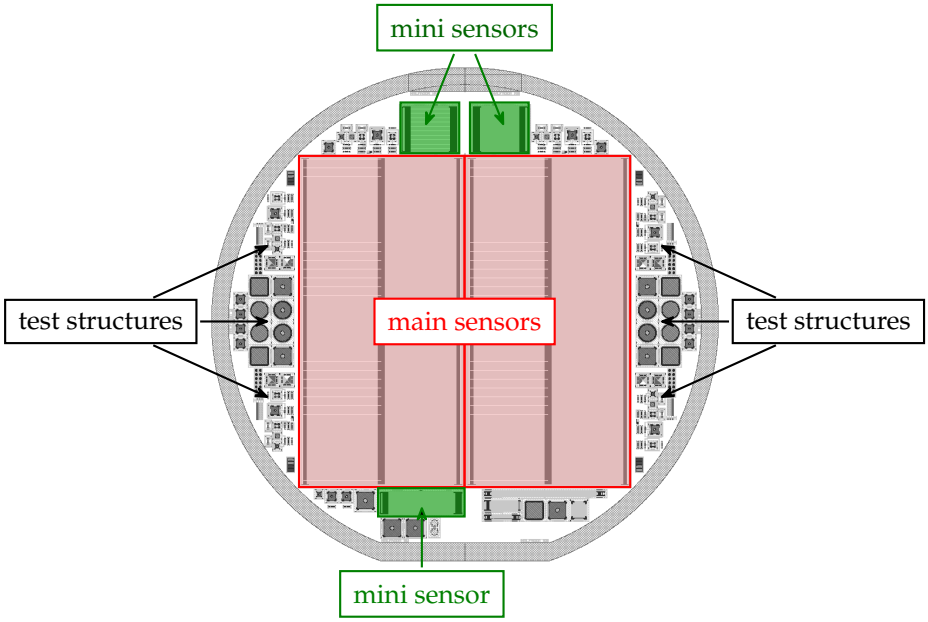
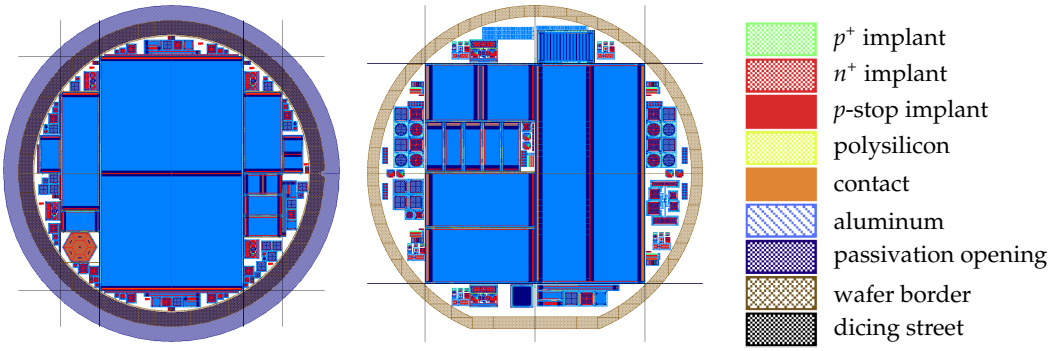


FIGURE 4.8: Qualitative components of the wafer layout for the CMS Phase-2 Upgrade, superimposed on the Outer Tracker PSS production layout.

TABLE 4.4: Wafer material of Tracker R&D and production runs. The list focuses on the material investigated as part of this work and is not otherwise exhaustive. All Infineon batches feature different process variations, including but not limited to *p*-stop implantation dose and diffusion time, various front side spray implantations, back side metalization type, and field-stop diffusion mechanism.

Name	Manufacturer	Size (in)	Sensor	Batch no.	Active thickness (µm)	Backside
Infineon 2SProto	IFX	8	2S	VE525852	200	thinned
				VE543425	200	thinned
				VE711408	300	thinned
Infineon PSSProto	IFX	6	PS-s	VC740654	240	thinned
				VC740655	240	thinned
				VC811929	240	thinned
2SProto	HPK	6	2S	VPX18592	240	deep diffused
				VPX21779	200	deep diffused
2SProto FZ290	HPK	6	2S	VPX28441	290	standard
2SProto thFZ240	HPK	6	2S	VPX28442	240	thinned
Pre-Series	HPK	6	PS-s	VPX33234	290	standard
Pre-Production	HPK	6	PS-s	VPX34252	290	standard
				VPX34253	290	standard
			2S	VPX34352	290	standard
				VPX34353	290	standard



(A) 8″ 2S prototype (Infineon 2SProto).

(B) 6″ PSS prototype (Infineon PSSProto).

FIGURE 4.9: Layout schematics of Infineon prototype wafers for the CMS Outer Tracker with marked dicing streets.

side metalization type, and field-stop diffusion mechanism. Where the process variations are relevant for the results presented in this thesis, details are given in later chapters.

The Infineon 2S prototypes (Figure 4.9a) are a noteworthy exception to the 6″ Tracker process. These batches constitute the world's first AC-coupled silicon strip sensors produced on 8″ wafers. Results and performance of sensors and test structures of batches *VE525852* and *VE543425* are discussed in [67, 71]. Sensor results of the remaining 8″ batch *VE711408* and the 6″ PS-s prototype batches *VC740654*, *VC740655*, and *VC811929* (Figure 4.9b) are presented in [72]. In general, the Infineon prototypes were of good quality and met most CMS specifications. However, the sensors were prone to premature breakdowns related to backside processing. The issue was addressed by the vendor and a number of potential solutions were proposed. However, no new prototypes were produced due to the discontinuation of the contract between Infineon and CMS because of the high R&D and production costs. A report of the sensor prototyping project with Infineon is given in [73].

Outer Tracker prototype and production batches manufactured by Hamamatsu Photonics all utilize a 6″ wafer process. All prototype wafers feature the same layout with a 2S sensor in the wafer center (Figure 4.10a). The individual batches vary in terms of active thickness between 200 µm and 290 µm and backside processing techniques.

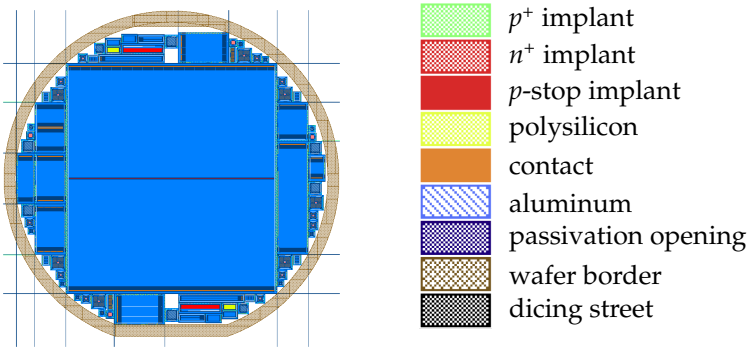
CMS chose the Hamamatsu 290 µm standard material as baseline for the Outer Tracker Series production [74, 75]. The final wafer layout is largely identical for 2S (Figure 4.10b), PS-s (Figure 4.10c), and PS-p sensors (Figure 4.10d). Because of the larger area of the 2S sensor compared to PS-s and PS-p sensors, the size of mini sensors and diodes in the upper and lower parts of the wafer is reduced, and a small sensor for the CMS Beam Radiation Instrumentation and Luminosity (BRIL) project[4] is omitted in the 2S wafer layout. While a single 2S sensor fits on one wafer, each PS-s and PS-p wafer contains two sensors of the same type.

The CMS Outer Tracker *Pre-Series* comprises 40 wafers with PS-s layout that were produced and delivered ahead of the official production start. The wafers were distributed and tested among the quality assurance test centers to give green light for the series production. The four-year production phase for the Outer Tracker started in 2020 with a four-month *Pre-Production* phase, during which production and delivery rates were gradually ramped up. Various Pre-Production batches have been distributed and tested. Results of sensor tests on the Hamamatsu Outer Tracker material are discussed in [72].

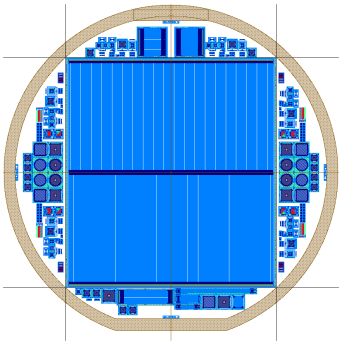
4.2.2 High Granularity Calorimeter

To date, the HGCAL project is in the prototyping phase. HGCAL sensors are produced on 8″ p type wafers. Before the decision was made to run with 8″, a number of prototypes

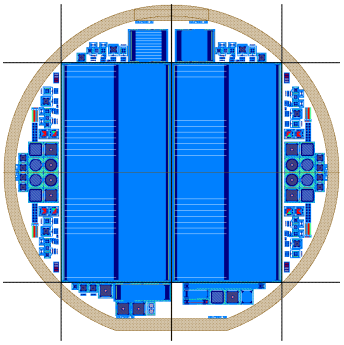
[4]The Outer Tracker production wafers include a set of two AC-coupled diodes that will be used as sensors for the all-silicon Fast Beam Conditions Monitoring system (BCM1F) during LHC Run 3 by CMS BRIL.



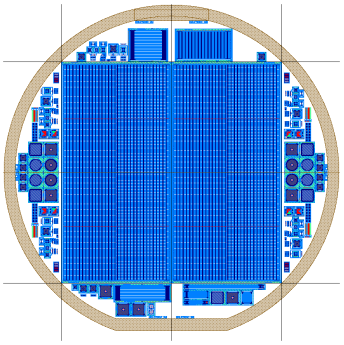
(A) 6″ 2S prototype (2SProto).



(B) 6″ 2S production layout.



(C) 6″ PS-s production layout.



(D) 6″ PS-p production layout.

FIGURE 4.10: Layout schematics of Hamamatsu CMS Tracker prototype and production wafers with marked dicing streets.

TABLE 4.5: Wafer material of HGCAL prototype runs. The list provides an overview on all types of wafers produced to date but is not otherwise exhaustive.

Name	Manufacturer	Size (in)	Batch	Bulk	Active thickness (µm)	Cells	*p*-stop	Backside
8inch Infineon	IFX	8	VE628925	*p*	140	237	individual	thinned
					200	237	common, individual	thinned
					300	237	common	thinned
					350	237	common, individual	thinned
			VE641657	*p*	200	237	common, individual	thinned
6inch 135-cells	HPK	6	S10938-4958	*n*	300	135		standard
			S10938-5896	*p*	300	135	common	standard
			S10938-5897	*p*	300	135	individual	standard
6inch 239-cells	HPK	6	S10938-4957	*n*	120	239		deep diffused
			S10938-5894	*p*	120	239	common	deep diffused
			S10938-5895	*p*	120	239	individual	deep diffused
8inch 272-cells (stepper)	HPK	8	S10938-6063	*p*	200	272	individual	thinned
8inch LD 2018	HPK	8	S10938-6097	*p*	300	198	common, individual	thinned
			S10938-6096	*p*	200	198	common, individual	thinned
			S10938-9090	*p*	120	198	common, individual	epitaxial
8inch LD 2019	HPK	8	S15591-01	*p*	300	198	common, individual	thinned
			S15591-02	*p*	200	198	common, individual	thinned
8inch HD 2019	HPK	8	*undisclosed*	*p*	120	444	common, individual	epitaxial

were produced on 6″ wafers. All sensors feature either *p*-stop common or *p*-stop individual layout, and active thicknesses range between 120 µm and 350 µm (Table 4.5).

Infineon produced two batches of *p* type 8″ wafers with a sensor prototype with 237 cells and four sectors with different inter-cell geometries (Figure 4.11). The batches, comprising 21 wafers in total, constitute the first ever HGCAL prototypes on 8″ wafers. Individual wafers feature different active thicknesses, *p*-stop layout, and process variations related to *p*-stop doping concentration, implantation depth, and wafer sawing technique. Some results of sensors and test structures of the Infineon prototypes are shown in [76].

Hamamatsu provided seven batches of 6″ *n* and *p* type wafers with two different sensor layouts for the HGCAL prototyping campaign. For the sensor design with 135 cells (Figure 4.12a), two *n* type and two *p* type batches with 300 µm active thickness were delivered. One *n* type and two *p* type batches with 120 µm active thickness were produced of the sensor layout with 239 cells (Figure 4.12b) on 6″ wafers.

When CMS decided that the HGCAL project would use 8″ wafers to reduce production

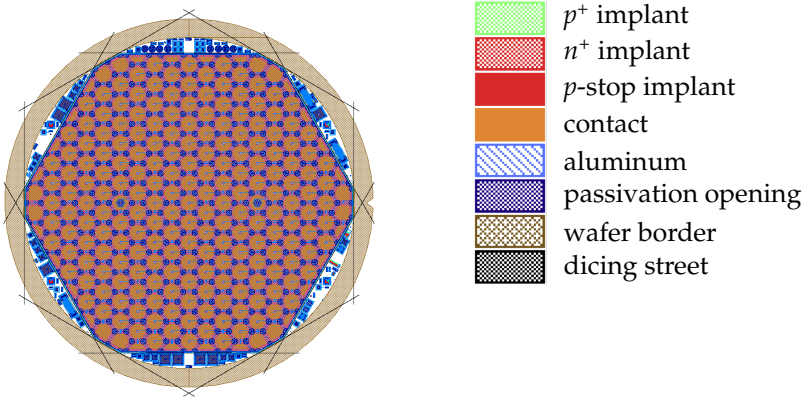
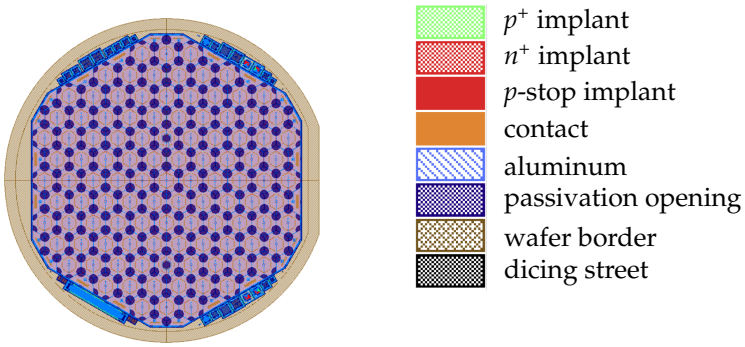
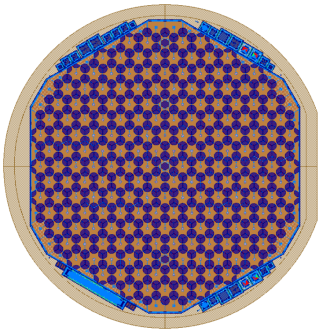


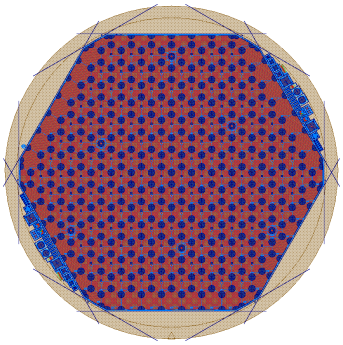
FIGURE 4.11: Layout schematics of the Infineon 237-cell 8″ HGCAL prototype (8inch Infineon) with marked dicing streets.



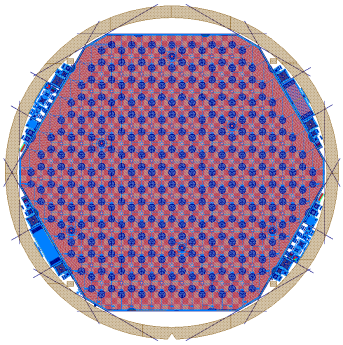
(A) 6″ HGCAL prototype layout with 135 cells.



(B) 6″ HGCAL prototype layout with 239 cells.



(C) 8″ HGCAL prototype layout with 198 cells (LD 2018).



(D) 8″ HGCAL prototype layout with 198 cells (LD 2019).

FIGURE 4.12: Layout schematics of Hamamatsu HGCAL prototype wafers with marked dicing streets. Empty halfmoon cutoffs contain undisclosed test structures for testing at the vendor.

costs and the necessary amount of sensor tests, Hamamatsu produced the first 8″ prototypes with 272 active cells utilizing a stepping technique for wafer lithography. In this case, instead of full-size lithography masks, smaller rectangular masks are replicated ("stepped") along the wafer to cover the full area. With this technique, three wafer batches with active thickness 300 µm, 200 µm, and 120 µm were produced. Only the batch with 200 µm active thickness is present in Vienna and listed in Table 4.5. Because of the stepper technique, the wafers do not include test structures. Results of electrical sensor characterization of these early Hamamatsu prototypes are presented in [77].

For subsequent runs, Hamamatsu adapted their procedures to provide 8″ wafers manufactured with full-size lithography masks. In 2018, three batches of 8″ prototypes with 192 regular cells and 6 calibration cells (Figure 4.12c) and active thickness 300 µm, 200 µm, and 120 µm were produced, amounting to 44 wafers total. Two batches containing 56 wafers in total with a new, adapted layout and 192 regular cells and 6 calibration cells (Figure 4.12d) and a third batch featuring the same adapted layout with 432 regular cells and 12 calibration cells were ordered in 2019. Active wafer thickness is 300 µm, 200 µm, and 120 µm for the three batches, respectively. The wafers feature process variations that affect Si-SiO_2 flat-band voltage, oxide quality, and p-stop doping concentration.

4.3 Sensor Quality Assurance

All sensors integrated into the CMS Outer Tracker and High Granularity Calorimeter must meet predefined quality standards. To this end, CMS follows a dedicated quality assurance plan (Figure 4.13).

Firstly, all sensors are pretested by the vendor. Only the sensors found to meet the

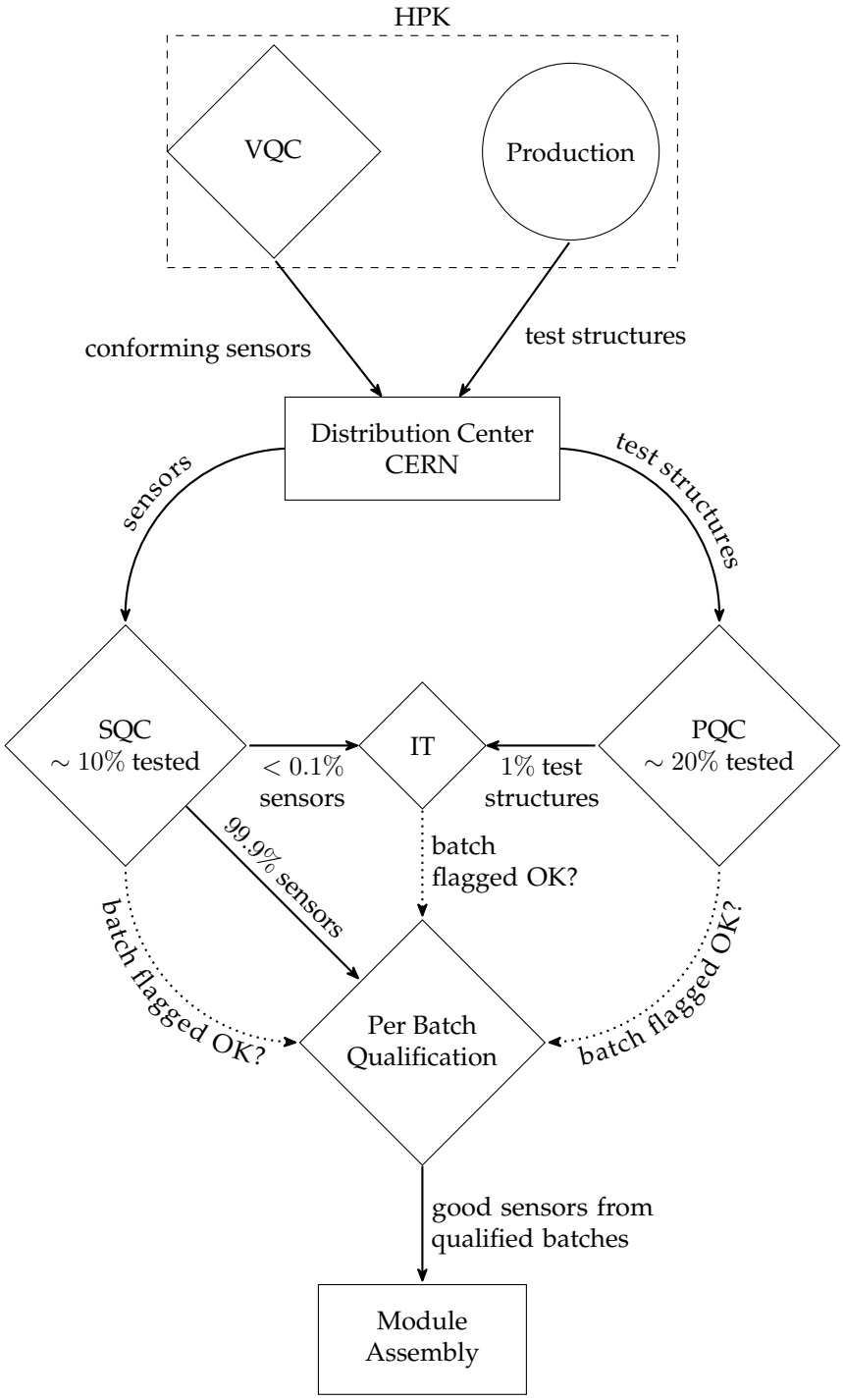


FIGURE 4.13: Process flow of the sensor quality assurance for the Phase-2 Upgrade of the CMS Outer Tracker. For CMS HGCAL, an analogous procedure will be applied, but exact numbers and goals have yet to be decided.

specifications during *Vendor Quality Control (VQC)* and all corresponding test structures are delivered to the distribution center at CERN. From there, sensors and test structures are distributed to the quality control test centers. Test centers are scientific institutions that are part of the CMS Outer Tracker and/or HGCAL collaboration and that can provide the necessary equipment and infrastructure to perform the quality control test procedures. Outer Tracker quality control is performed at Brown University (Providence, RI) and Rochester Institute of Technology in the US, Karlsruhe Institute of Technology (Germany), the Institute of High Energy Physics in Vienna (Austria), INFN Perugia (Italy), NCSR Demokritos in Athens (Greece), the University of Delhi (India), and NCP Pakistan. Institutions involved with the HGCAL project include Brown University, the University of California, Texas Tech University, Florida State University, and Fermi National Accelerator Laboratory in the US, CERN, Karlsruhe Institute of Technology, and the Institute of High Energy Physics (HEPHY) in Vienna.

The test centers perform the three main quality control procedures, *Sensor Quality Control (SQC)*, *Process Quality Control (PQC)*, and *Irradiation Tests*. The results of these quality control procedures are combined to qualify each delivered wafer batch. Because irradiation tests have a comparatively long lead time, the initial decision about the acceptance of a delivered batch relies mainly on SQC and PQC results. Irradiation results are monitored separately to ensure radiation hardness of the material.

With the aforementioned quality control procedures, CMS tests if the material fulfills a set of acceptance limits that were defined in collaboration with the vendor for every sensor type. These specifications are based on previous sensor qualification and irradiation campaigns [34]. The experience from these campaigns allows to infer the expected parameter development after irradiation from SQC and PQC results.

If the material does not conform to the limits, the corresponding batches are rejected. Aside from comparing results to the predefined hard rejection criteria, quality control procedures can detect trends or deviations of parameters that are not covered by the specifications or remain within the limits. If any such issue is detected, CMS will decide on a case to case basis if it needs to be communicated to the vendor to request a solution.

In the following, the three quality control mechanisms and predefined parameter specifications are discussed.

4.3.1 Sensor Quality Control

Sensor Quality Control (SQC) characterizes individual sensors through electrical measurements and optical inspection to ensure that the sensors fully satisfy specifications. Test centers perform the measurements on a sample of sensors out of each delivered batch to verify the quality of the batch and approve the sensors for module assembly and integration into the detector. The procedure and measured parameters differ for Outer Tracker and HGCAL sensors.

Outer Tracker

In case of the Outer Tracker, a minimum of two strip sensors (i.e. 2S and PS-s sensors) per batch undergo SQC. The macro-pixel sensors are not qualified with SQC. Instead, CMS relies on VQC and PQC to judge the quality of the PS-p batches.

The optical inspection consists of a manual scan of front and back of the sensor under a microscope. The edge of the sensor receives special attention to evaluate the quality and precision of the dicing cut. Stitched photographs of the full sensor area are stored for later reference in case of problems.

Electrical characterization of strip sensors is divided into global characterization of the full sensor and individual characterization of single-strip and inter-strip parameters. Global characterization evaluates the current-voltage (*I*-*V*) and capacitance-voltage (*C*-*V*) behavior of the full sensor. For a full characterization, single-strip parameters (i.e. strip current I_{strip}, resistance of the polysilicon bias resistor R_{poly}, coupling capacitance C_{ac}, and current through the dielectric I_{diel}) are measured on every strip, and inter-strip parameters (i.e. inter-strip resistance R_{int} and inter-strip capacitance C_{int}) are extracted for a limited number of strips in addition to global characteristics.

TABLE 4.6: Sensor qualification specifications and acceptance limits for the CMS Outer Tracker series production.

Parameter	CMS specification
Substrate resistivity, ρ	$> 3.5\,\mathrm{k\Omega\,cm}$
Physical thickness, t_p	$320\,\mu\mathrm{m}$
Active thickness, t_a	$290\,\mu\mathrm{m}$
Thickness tolerance	$< \pm 5\%$
Full depletion voltage, V_dp	$< 350\,\mathrm{V}$ at $290\,\mu\mathrm{m}$ active thickness
Current at $600\,\mathrm{V}$, I_{600}	$\leq 2.5\,\mathrm{nA/mm^3}$
Current at $800\,\mathrm{V}$, I_{800}	$< 2.5 \times I_{600}$
Breakdown voltage, V_bd	$> 800\,\mathrm{V}$
Longterm stability	$\lvert\langle\Delta I_{600}\rangle / \langle I_{600}\rangle\rvert < 20\%$ in $48\,\mathrm{h}$ at $600\,\mathrm{V}$ and $< 30\%\mathrm{rH}$
Strip current, I_strip	$< 2\,\mathrm{nA/cm}$
Bias resistor, R_poly	$1.5 \pm 0.5\,\mathrm{M\Omega}$
Coupling capacitance, C_ac	$> 1.2\,\mathrm{pF/cm}$
Current through dielectric, I_diel	$< 100\,\mathrm{pA}$ at $10\,\mathrm{V}$
Inter-strip resistance, R_int	$> 10\,\mathrm{G\Omega\,cm}$
Inter-strip capacitance, C_int	$< 0.5\,\mathrm{pF/cm}$
Percentage of bad strips	$\leq 1\,\%$ per sensor
Clustering of bad strips	≤ 2 in any set of 5 consecutive strips

A limited number of sensors are subjected to longterm stability tests inside a controlled environment. The sensors are biased at $600\,\mathrm{V}$ and kept at a constant temperature of $21 \pm 1°\mathrm{C}$ and relative humidity $< 10\%$ (e.g. inside a climatic chamber). In this environment, the sensor current is monitored over a minimum duration of two days with measurements taken at $60\,\mathrm{s}$ intervals.

All SQC results are checked for consistency and compared to the predefined specifications (Table 4.6). Details on the Outer Tracker SQC procedure and measurements can be found in [72].

High Granularity Calorimeter

Currently, the quality assurance plan for HGCAL sensors is not fixed. Tested sensor quantities and procedures have yet to be decided. However, similar to the Outer Tracker procedure, optical inspection and electrical characterization of sensors will be performed as part of SQC.

In contrast to the AC-coupled strip sensors of the Outer Tracker, the DC-coupled HGCAL sensors lack a common biasing structure. This factor complicates sensor testing because all sensor cells and the inner guard ring must be biased during testing in order to correctly reproduce the electric field configuration during detector operation. HGCAL sensor quality control thus utilizes a probe card and switching matrix system, named ARRAY (switching mAtRix pRobe cArd sYstem), to contact all sensor cells simultaneously [60]. Parameters extracted from sensor measurements include global and single-cell I–V and C–V characteristics, inter-cell resistance R_int, and inter-cell capacitance C_int. Some specifications for the sensor material have been set (Table 4.7) but may be subject to change.

4.3.2 Process Quality Control

Process Quality Control (PQC) tracks the quality and stability of the sensor production process by measuring process parameters on test structures. The structures are produced on the same wafers as the sensors and go through the same production process. Thus, test structures exhibit the same properties as the sensors and provide the means to investigate sensor and process parameters without having to measure the sensors directly. Specific test structures exist for each individual parameter. Because the measurements of individual test structures are generally quick, PQC allows to qualify a larger sample of wafers per batch than SQC. Furthermore, test structures allow to assess parameters that cannot be measured directly on the sensors, including parameters that require potentially destructive measurements. Because the same test structures are placed multiple times on one wafer, PQC can track process parameter variations along the wafer area.

TABLE 4.7: Sensor qualification specifications and acceptance limits for the CMS HGCAL. Parameters may be subject to change.

Parameter	CMS specification
Substrate resistivity, ρ	$> 3.0\,\mathrm{k\Omega\,cm}$
Physical thickness, t_p	300 µm, 200 µm, 300 µm
Active thickness, t_a	300 µm, 200 µm, 120 µm
Thickness tolerance	$< \pm 10\,\mu\mathrm{m}$
Full depletion voltage, V_dp	300 µm type: $< 370\,\mathrm{V}$ 200 µm type: $< 160\,\mathrm{V}$ 120 µm type: $< 70\,\mathrm{V}$
Current at 600 V (normalized to 20 °C), I_{600}	$\leq 100\,\mu\mathrm{A}$ integrated over sensor and guard rings
Current at 800 V, I_{800}	$< 2.5 \times I_{600}$
Breakdown voltage, V_bd	$> 800\,\mathrm{V}$
Longterm stability	$\lvert\langle\Delta I_{600}\rangle / \langle I_{600}\rangle\rvert < 30\%$ in 48 h at 600 V and $< 30\%\mathrm{rH}$
Single-cell current at 600 V, I_pad	$\leq 100\,\mathrm{nA/pad}$
Inter-cell resistance, R_int	$> 100\,\mathrm{M\Omega}$ at $V_\mathrm{fd} + 50\,\mathrm{V}$ and room temperature
Inter-cell capacitance, C_int	$< 1.5\,\mathrm{pF/cm}$ at $V_\mathrm{fd} + 50\,\mathrm{V}$ and room temperature
Number of bad cells	≤ 8 per full-size sensor
Clustering of bad cells	≤ 2 adjacent bad cells

The PQC strategy is largely the same for the Outer Tracker and HGCAL. Both projects utilize the same set of test structures that allows automated measurements with a 20-needle probe card. However, because of the lower complexity of the DC-coupled process, the HGCAL procedure looks at fewer process parameters than Outer Tracker PQC measurements. In general, a predefined set of process parameters are measured on a selected number of wafers per batch and compared to the specifications. In case of the Outer Tracker, about $20\,\%$ of the wafers in one batch undergo a condensed PQC procedure, in which the most important parameters are assessed on two positions along the wafer area, and for at least one wafer per batch the full set of process parameters accessible via the test structure set are measured.

Chapters 6 and 7 in detail discuss specialized test structures, process parameters and specifications, the PQC procedure, and the test structure set used for automated PQC for the Outer Tracker and HGCAL projects.

4.3.3 Irradiation Tests

Irradiation tests ensure that the radiation hardness of the sensors does not change over production time. These tests, however, are not used to qualify individual wafer batches and are not required to be concluded to release a batch.

The procedure is qualitatively similar for the Outer Tracker and HGCAL projects. Dedicated test sensors, test structures, and a small number of full-size sensors are selected for irradiation. Usually, all selected structures undergo electrical characterization before irradiation to ensure normal behavior. Subsequently, the structures are irradiated with neutrons and/or protons to target fluences corresponding to the maximum expected fluences in selected parts of the detector volume. In case of the Outer Tracker, 2S wafers are irradiated to $4 \times 10^{14}\,\mathrm{n_{eq}/cm^2}$ and PS-s and PS-p wafers to a target fluence of $1.1 \times 10^{15}\,\mathrm{n_{eq}/cm^2}$. Additionally, a limited number of structures are subjected to X-ray irradiation to check potential surface property changes. After irradiation, the structures undergo a specified annealing procedure (generally, 20 minutes at 60°C) and are electrically characterized at stable, low temperature (i.e. $\sim -20\,°\mathrm{C}$ for the Outer Tracker and $\sim -30°\mathrm{C}$ in case of HGCAL) to prevent further annealing and thermal runaway and at low dew point to prevent condensation and icing. In case of Outer Tracker sensors, a full characterization, including global I–V and C–V characteristics, single-strip and inter-strip measurements, is performed.

After electrical characterization, Outer Tracker sensors are subjected to signal measurements at bias voltages from 300 to 900 V in 100 V steps. The signal measurement is repeated five times with subsequent annealing steps (i.e. as is, 60 min at 60 °C, 120 min at 60 °C, 30 min at 80 °C, and 60 min at 80 °C). After completed signal measurements, the sensors undergo

TABLE 4.8: Performance specifications after irradiation for CMS Outer Tracker sensors.

Parameter	CMS specification
Breakdown voltage, V_{bd}	$> 800\,\text{V}$
Current at $800\,\text{V}$	$< 2.5 \times I_{600}$
Maximum current at $800\,\text{V}$	$< 1\,\text{mA}$
Inter-strip resistance, R_{int}	$> 100\,\text{M}\Omega\,\text{cm}$ (at $600\,\text{V}$ bias)
Inter-strip capacitance, C_{int}	$< 0.5\,\text{pF/cm}$
Minimum charge collected at $600\,\text{V}$	2S sensors: $12\,000$ electrons
	PS-s and PS-p sensors: 9600 electrons
Percentage of bad strips	$\leq 1\,\%$ per sensor
Clustering of bad strips	≤ 2 in any set of 5 consecutive strips

TABLE 4.9: Performance specifications after irradiation for CMS HGCAL sensors. The parameter set may be subject to change.

Parameter	CMS specification
Breakdown voltage, V_{bd}	$> 800\,\text{V}$
Sensor current at $800\,\text{V}$, $I_{\text{sensor,800}}$	$< 2.5 \times I_{\text{sensor,600}}$
Single-cell current at $800\,\text{V}$, $I_{\text{pad,800}}$	$< 2.5 \times I_{\text{pad,600}}$
Inter-cell resistance, R_{int}	$> 100\,\text{M}\Omega\,\text{cm}$ (at $600\,\text{V}$ bias)
Inter-cell capacitance, C_{int}	$< 1.5\,\text{pF/cm}$
Number of bad cells	≤ 8 per full-size sensor
Clustering of bad cells	≤ 2 adjacent bad cells

another full strip characterization. For HGCAL sensors, a similar procedure will be applied but has yet to be decided.

The results of irradiation tests are compared to the respective specifications (Table 4.8 and 4.9).

CHAPTER 5

TOOLS AND METHODS

Aiming at developing a strategy for process quality control (PQC) for the Phase-2 Upgrade of the CMS Outer Tracker and High Granularity Calorimeter (HGCAL), the work presented in this thesis utilized electrical measurements of a large number of different test structures and complementary device simulations. To facilitate the necessary measurements and, simultaneously, ready the PQC test center at the Institute of High Energy Physics (HEPHY) Vienna for the upcoming Outer Tracker and HGCAL series production phases, a custom-made probe station for automated PQC was designed and commissioned.

The following sections address the setup and components of the probe station for automated PQC implemented in the cleanroom of HEPHY Vienna, including circuitry, measurement instruments, and measurement software, and introduce the software package used for device simulations performed within the framework of this thesis.

5.1 Automated PQC Probe Station

The probe station for automated PQC (Figure 5.1) in the cleanroom of HEPHY Vienna was custom-made and adapted from its predecessor (see e.g. [76]), which was mainly used for measurements using manual micropositioners. The new probe station provides the possibility for both manual measurements using micropositioners and automated measurements using a 20-needle *probe card*.

The main component of the probe station is a light-tight metal enclosure that also isolates the setup from stray electric fields. It houses a fixed mount for the probe card at the back of the box and stages for microspositioners in front. The *vacuum jig* (Figure 5.2), on which the devices under test (DUT) are mounted during measurement, is fixed to a programmable x-y-z stage that allows movement along all three axes with micrometer precision. The jig is realized with a guard concept and provides the high voltage contact to the backplane of the DUT. It features separately switchable vacuum leads and can simultaneously house up to four "halfmoon"-type wafer cutoffs. Further, the jig provides the means for cooling and heating using Peltier elements and a coolant loop to an external chiller. A *camera* aligned with the probe card needles allows positioning and contacting of test structures with the probe card. Additionally, the probe station includes a *microscope* with a mounted camera for positioning and contacting during measurements using the manual micropositioners. The standard micropositioners used as part of the PQC setup are four *MP40 MicroPositioners* from *MPI Corporation*.

An *Arduino*-based, custom-made *environment control* system monitors temperature and relative humidity inside the light-tight box. It is connected to the *controlling PC* and allows to flush the box with dry air if the relative humidity exceeds critical levels. This is important to ensure stable measurement conditions and avoid damage to the tested semiconductor devices, especially, in conjunction with cold measurements, during which icing can become a problem. The environment control unit also controls various light sources within the box, probe card and microscope cameras, and a laser switch that prevents the motorized x-y-z stage from crashing into the probe card when performing measurements with manual

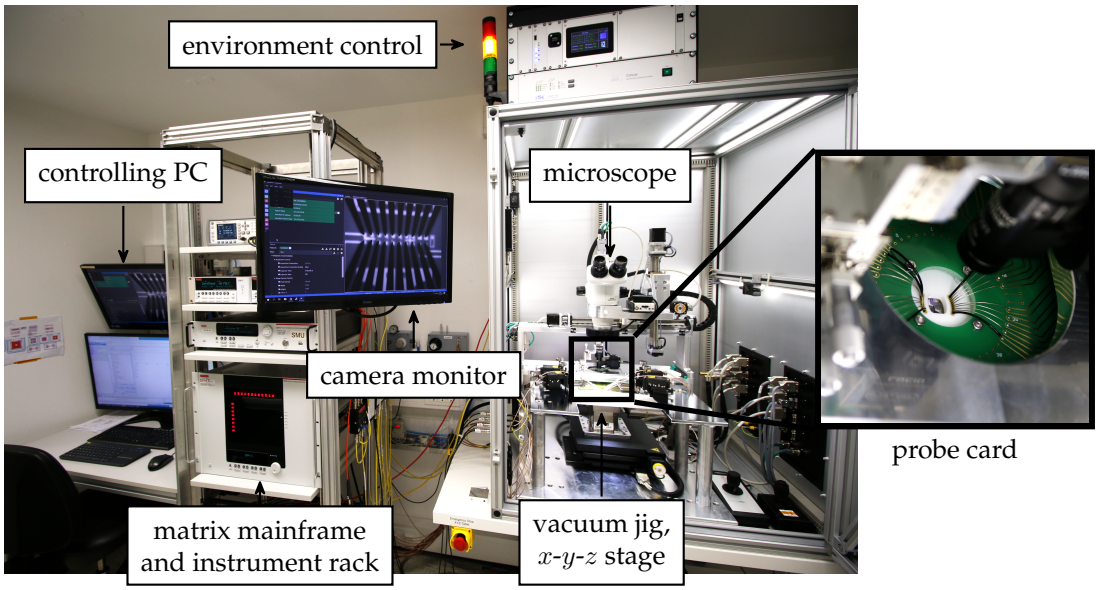


FIGURE 5.1: Custom-made probe station for automated and manual PQC in the cleanroom at HEPHY Vienna.

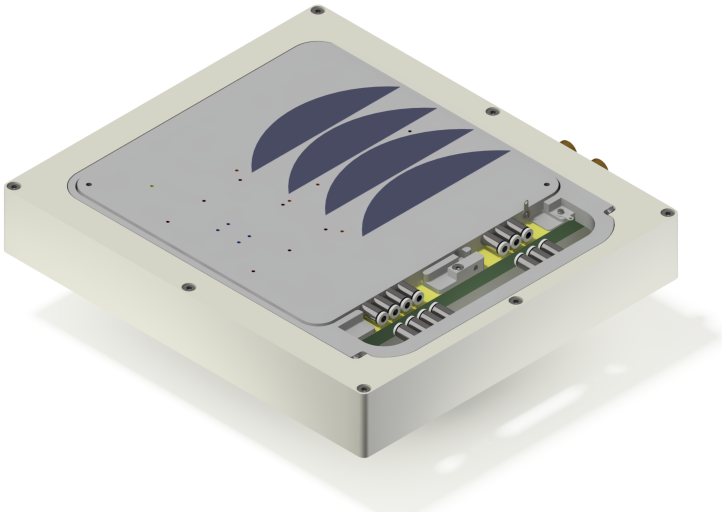


FIGURE 5.2: CAD drawing of the vacuum jig for automated PQC with four mounted "halfmoon" wafer cutoffs.

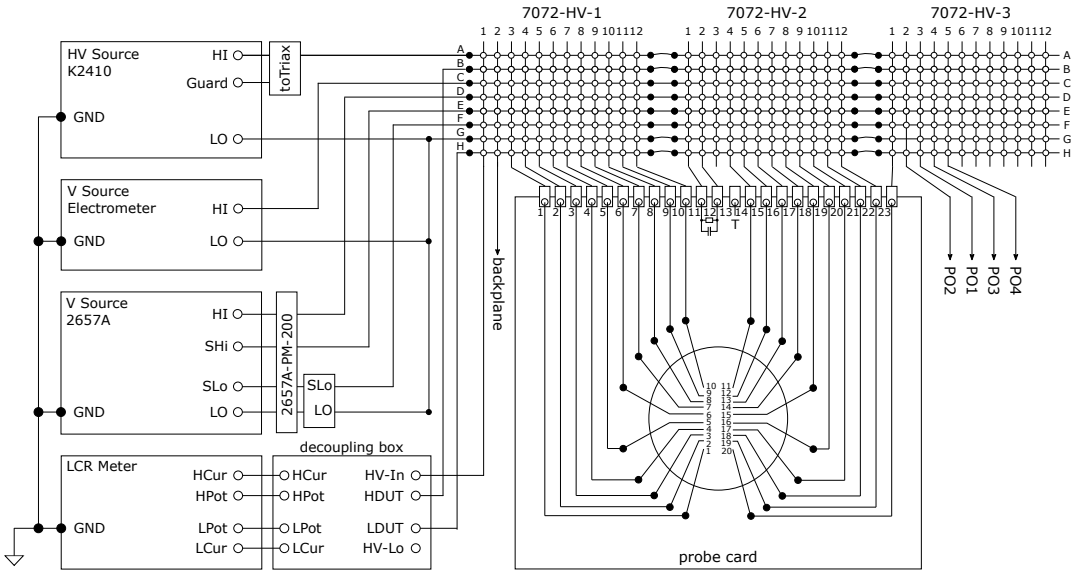


FIGURE 5.3: Schematic of the PQC setup in the cleanroom of HEPHY Vienna, including connections between instruments and switching system comprised of three *Keithley 7072-HV* matrix cards, 20-needle probe card, and four manual positioners "PO1"–"PO4".

positioners.

All measurement instruments, including the matrix switching system, are contained in a *movable rack* outside of the light-tight box. The rack also supports a monitor on which the camera picture of the probe card needles can be displayed.

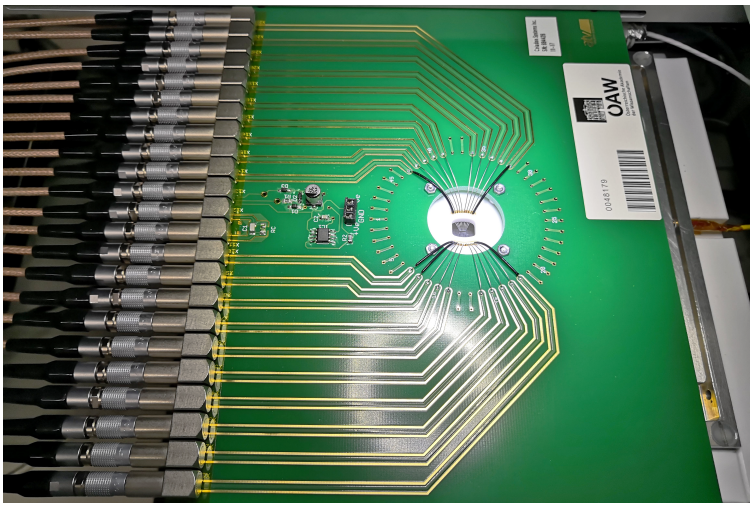
In the following, the main components of the PQC setup, probe card, test structure contacts, measurement instruments, and circuitry (Figure 5.3) are discussed in detail.

5.1.1 Probe Card

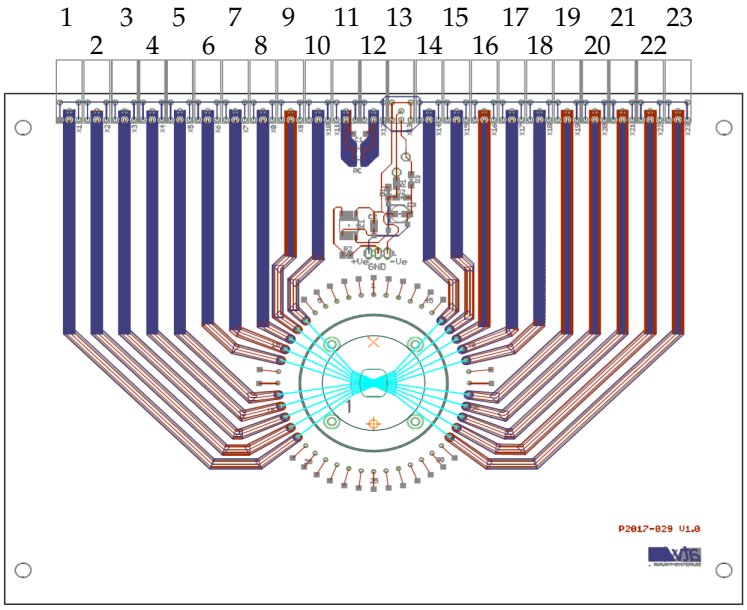
A 20-needle probe card (Figure 5.4) is used to contact test structures during automated PQC. The probe card consists of a printed circuit board (PCB) that provides all connections and circuitry and a mount for the probe needles fixated to the PCB. The probe needles are spaced such that the tips align perpendicular to the contacting surface in two rows of 10 needles each with a distance of $200\,\mu\mathrm{m}$ between closest neighbors. Up until the probe needles, all connections and circuitry are realized with a triax guard concept. The board provides 23 triax LEMO connectors, 20 of which are routed to the probe needles via the PCB. One (no. 13) connects to a temperature and humidity sensor integrated in the PCB, and the remaining two connectors (no. 11 and 12) lead to an RC test circuit consisting of a $100\,\mathrm{M}\Omega$ resistor and a $10\,\mathrm{pF}$ capacitor. Except for no. 13, all connectors are routed through the switching matrix. Currently, two probe cards with the same PCB design are present at HEPHY Vienna. They differ only in terms of the probe needle material. One card features probe needles out of tungsten while the second card uses tungsten-rhenium needles. Tungsten needles are harder and, hence, preferable for easier contacting, while the tungsten-rhenium needles are softer and, hence, reduce the risk of damaging the structures while contacting.

5.1.2 Test Structure Contacts - "Flutes"

While, during manual testing, test structures can be contacted with manual probe needles everywhere where there is a passivation opening, automated tests utilizing the 20-needle probe card require dedicated structures for contacting. For this purpose, test structures are arranged around and connected to arrays of 2×10 contact pads, denoted "flute" (Figure 5.5). Each individual contact pad consists of a $(100 \times 100)\,\mu\mathrm{m}^2$ metalization with a centered $(90 \times 90)\,\mu\mathrm{m}^2$ passivation opening. Pads are spaced with $200\,\mu\mathrm{m}$ pitch, corresponding to

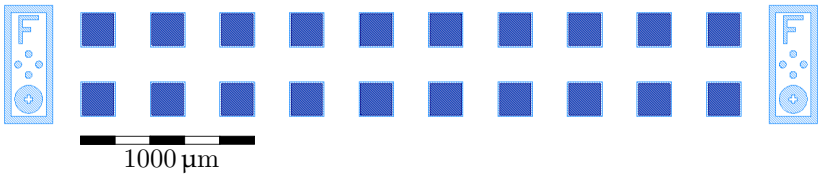


(A) Top view photograph of the PQC probe card with triax cables and LEMO connectors.

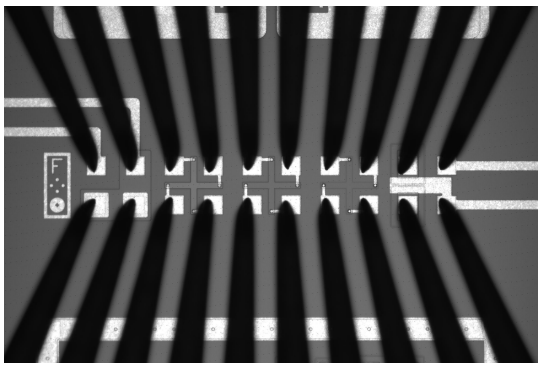


(B) Schematic of the PQC probe card with numbered connectors.

FIGURE 5.4: 20-needle probe card for automated PQC.



(A) Layout of a "flute" with alignment marks on both sides.



(B) Microscope image of probe card needles atop a "flute" with connected test structures.

FIGURE 5.5: Array of 2×10 contact pads ("flute") for use with a 20-needle probe card.

the probe card needle spacing. As orientation and alignment reference points, some flutes include one or more alignment marks.

5.1.3 Instruments and Switching System

The instruments of the PQC setup (see Figure 5.3) are chosen to enable quick, economic, and precise measurements of all process parameters. The setup includes two source measure units (SMU), a high-precision electrometer, and a precision LCR meter. The instruments are connected to the probe card and manual micropositioners via a switching system featuring three 8×12 matrix cards. Wherever possible, all connections are realized via triaxial cables and connectors, maintaining a common guard concept.

The following sections provide details on all measurement instruments and their specifications.

Source Measure Units (SMU)

The PQC setup includes two different source measure units (SMU) that are capable of sourcing and measuring voltage and current.

A *Keithley 2410* (K2410) SMU serves as the high voltage source, which is used if voltages $> 200\,\mathrm{V}$ need to be supplied, e.g., for diode current-voltage (I–V) and capacitance-voltage (C–V) measurements. It sources voltage from $5\,\mu\mathrm{V}$ to $1100\,\mathrm{V}$ and current from $50\,\mathrm{pA}$ to $1\,\mathrm{A}$. The measurement range for voltage extends from $1\,\mu\mathrm{V}$ to $1100\,\mathrm{V}$, and the device can measure current from $10\,\mathrm{pA}$ to $1\,\mathrm{A}$. Because the SMU model only provides banana sockets for all outlets, a custom-made adapter is used to transfer the signals of "HI" and "Guard" to a common triaxial cable that is connected to the switching matrix.

For four-terminal measurements, the setup includes a *Keithley 2657A* high-power SMU. The instrument will source voltage from $5\,\mathrm{mV}$ to $3030\,\mathrm{V}$ and current from $30\,\mathrm{fA}$ to $120\,\mathrm{mA}$. It measures voltage from $1\,\mathrm{mV}$ to $3030\,\mathrm{V}$ and current from $20\,\mathrm{fA}$ to $120\,\mathrm{mA}$. Because, for this purpose, the instrument "HI", "LO", "Sense-HI" and "Sense-LO" terminals are connected to general purpose lines of the switching matrix card, a protection module that prevents accidental sourcing of voltages $\geq 200\,\mathrm{V}$ is included in front of the switching matrix.

Electrometer

The PQC setup includes a *Keithley 6517B* electrometer for high-precision current measurements. The instrument provides reliable measurements of current levels down to $10\,\mathrm{aA}$, charge levels down to $1\,\mathrm{fC}$, and the highest resistance measurements available up to $10^{18}\,\Omega$. The electrometer is also capable of measuring the largest voltage range – up to $200\,\mathrm{V}$ – with an input impedance exceeding $200\,\mathrm{T}\Omega$.

LCR Meter

For capacitance measurements, the PQC setup includes a *Keysight 4980A* precision LCR meter. The instrument has a signal frequency range from $20\,\mathrm{Hz}$ to $2\,\mathrm{MHz}$ and a maximum AC signal voltage level of $2\,\mathrm{V}$. It can supply a DC bias voltage of up to $40\,\mathrm{V}$. Hence, the instrument requires an upstream decoupling box to protect it from DC bias voltages supplied by the high-voltage source that exceed the instrument limit. Even though such high voltages are not required for all C–V measurements, the decoupling box is included for all measurements and the DC bias voltage is always supplied by an external SMU to simplify switching and measurement configurations.

Instruments and cabling introduce non-negligible stray impedance that affects the measured capacitance. The respective parallel and serial impedance must be determined before a measurement and subtracted from the corresponding measurement value. For this purpose, the instrument allows to perform "OPEN" and "SHORT" corrections, store the respective correction values, and automatically subtract them for each measurement. Alternatively, it is also possible to perform a "LOAD" correction if the expected measurement value is known.

Switching Matrix

The probe card and all manual positioners are connected to three 8×12 *Keithley 7072-HV* matrix cards (Figure 5.6) inserted into a *Keithley 707B* six-slot mainframe, allowing quick automatic connection of different instruments. Each card has eight rows, marked with letters "A" to "H", and twelve columns, numbered "1" to "12". The matrix cards are connected such that an effective 8×36 matrix results. The instruments are connected to the eight rows. The columns, in turn, connect the instruments to the needles of the probe card, the manual positioners, and two outlets for the high voltage signal leading to the decoupling box high voltage input and the vacuum jig that contacts the backplane of the device under test (DUT). The channel between a row and a column is identified by a four-character string, consisting of slot number, row letter, and two-digit column number (e.g. "1A12", "2D01").

All rows and columns are terminated with 3-lug triaxial connectors. Rows A and B of the 7072-HV matrix card and all columns are capable of sustaining voltage up to $1.3\,\mathrm{kV}$[1]. All remaining rows (i.e. C–H) can only sustain voltages $< 200\,\mathrm{V}$, and care must be taken to protect these rows from voltages exceeding this limit because such an event can destroy the cards or the entire switching matrix. Rows C to F are shared between the slots by the mainframe, while rows A and B (as well as G and H) are not shared by default and have to be connected between cards with coaxial jumpers. Rows G and H are low-noise paths with connected guard and ground lines originally intended for C–V measurements.

5.1.4 Measurement Software

The PQC measurements are controlled using a custom made Python software (Figure 5.7) [79]. The software was designed with focus on automated measurements utilizing the 20-needle probe card and the test structure set for automated PQC (see section 7.2). It allows to define custom *measurement sequences* using YAML configuration files. Each measurement sequence can be composed using nine predefined measurement types (e.g. "IV Ramp", "IV Ramp 4-Wire", "CV Ramp (HV Source)") that can be named and ordered as required by the user. Each measurement can be defined with dedicated parameters, including a preset switching configuration of the matrix. The sequences of any loaded configuration file will appear in the measurement tree of the graphic user interface (GUI). Via the GUI, the loaded sequence can

[1] The probe card itself and cables are tested to $1\,\mathrm{kV}$.

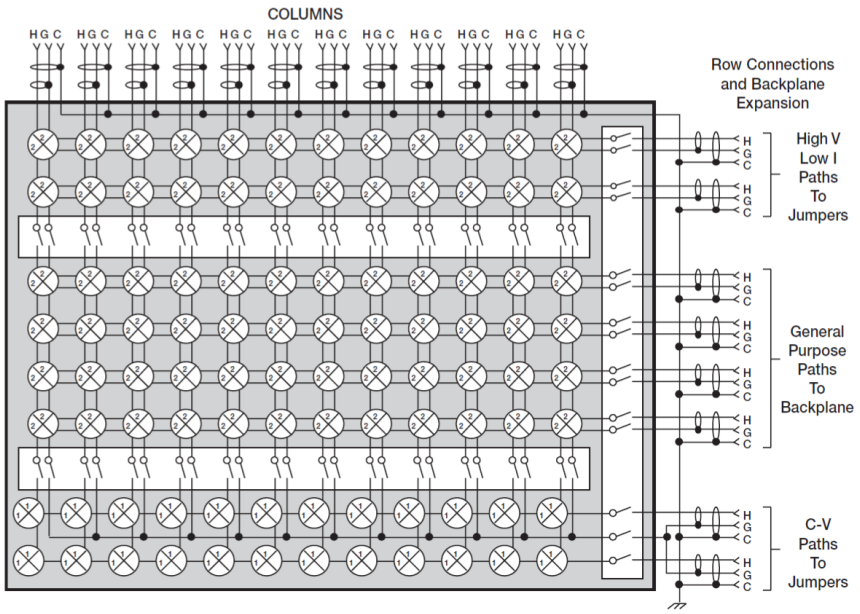


FIGURE 5.6: Schematic of *Keithley 7072-HV* matrix card [78].

be adapted and parameter settings of individual measurements can be customized directly within the *measurement settings* panel.

From within the measurement tree, both individual measurements and full sequences can be started by clicking "Start", depending on the currently active element in the tree. If an individual measurement (e.g. "GCD") is active at the time of start, only this measurement will run. If, instead, a parent category in the tree (e.g. "PQC Flute 1") is active, the software will run the full sequence within the active category, performing every measurement that features an enabled checkbox. Hence, with this feature, it is also possible to perform individual measurements using manual positioners instead of the probe card.

Measurement results are displayed live in form of one or more *data graphs*, and individual readings of instruments and environment parameters such as temperature and relative humidity are displayed in the *measurement readings* panel. At the end of the measurement, screenshots of the respective data graphs are saved together with JSON and plain text files containing all measurement data.

In addition to measurement configuration and control, the software allows to control different light sources within the light-tight box, probe card and microscope cameras, the safety laser switch, and the movement of the x-y-z stage using a dedicated *control panel* in the GUI. Automated movement of the x-y-z stage between individual flutes and automated contacting are currently not implemented out of safety reasons. However, such a feature might still be added after enough experience has been gained with the probe card and automated x-y-z stage.

5.2 Device Simulations

To complement electrical measurements and to investigate the behavior of different types of test structures if, e.g., certain process parameters are varied, this work includes device simulations, which utilize the commercial software package *Synopsys TCAD* [80]. The following section gives a brief introduction to the main functionalities of this semiconductor simulation tool with the aim to provide a basis to understanding the simulation workflow and the capabilities of the tool but also to point out the limitations of the method with regard to test structure simulations.

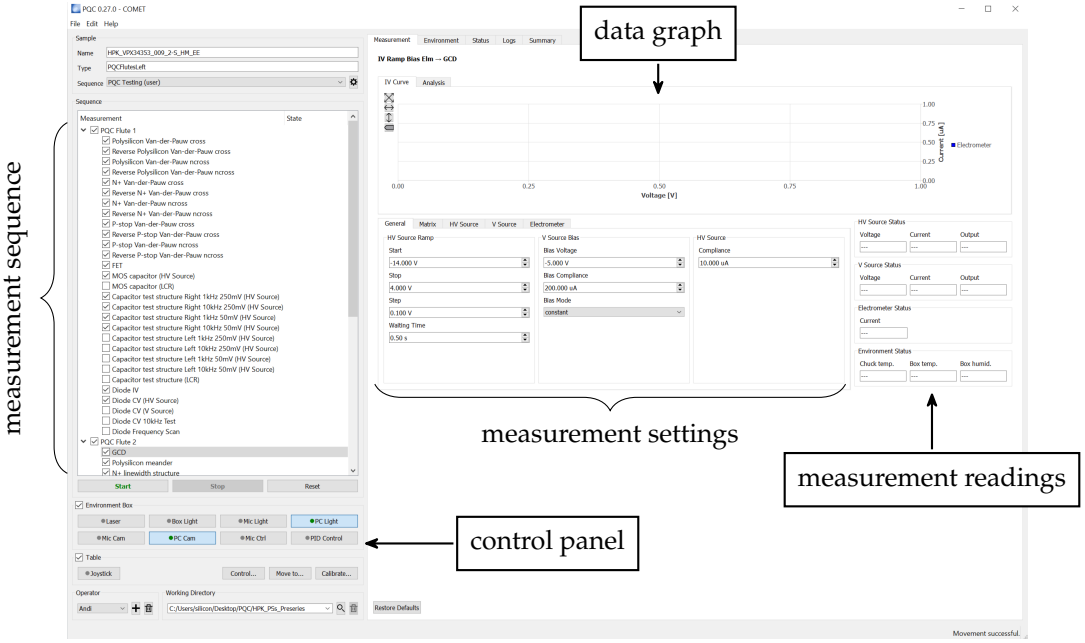


FIGURE 5.7: "COMET PQC" measurement software for automated PQC.

5.2.1 Synopsys TCAD

Synopsys TCAD is a commercial software package for semiconductor process and device simulation that is widely used in semiconductor industry. It allows 2D and 3D simulations of virtually any user-defined semiconductor device. Simulations utilize the *finite element method*, solving Poisson and continuity equations for electrons and holes at discretized points across the device and interpolating in the regions between. The discretized points are given as nodes of a mesh that encompasses the simulated device and can be defined manually by the user but also by utilizing meshing and refinement algorithms available within the framework. Size and refinement of the mesh critically affect simulation time and accuracy and influence the convergence behavior and, ultimately, the success of a simulation. As a rule of thumb, the mesh should always be chosen reasonably coarse with additional refinements in areas of, e.g., high field gradients and carrier activity such as implantation regions and interfaces.

While the Synopsys TCAD suite provides a large number of tools for process and device simulation, refinement, and data visualization, the simulations performed as part of this thesis mainly utilize two tools, namely the *Sentaurus Structure Editor* (SDE) and *Sentaurus Device* (SDEVICE).

SDE is used to define and render the geometry of the semiconductor device. In the respective command file, materials, contacts, and implantation profiles can be defined. Parameters can be defined as variables that can be varied to produce different geometries or implantation profiles in different instances of the same simulation, denoted "experiments". Lastly, SDE allows to define the mesh used to compute simulation results along the device. As output, SDE produces a file that contains the device geometry, including variable parameters, and the computed mesh.

The file resulting from SDE is subsequently used as input for SDEVICE, which performs the finite element analysis as defined by the user. For this purpose, SDEVICE requires an additional input file that defines the physics models and parameters (e.g. carrier lifetimes) to be used for the calculations, circuitry, contact boundary conditions (i.e. voltage settings, ohmic, or floating contacts), and further specifications about which computations will be performed. Synopsys TCAD provides a large variety of physics models for different types of applications and devices (e.g. mobility, generation-recombination, and avalanche models), which should be selected according to purpose and focus of the respective simulation. SDEVICE allows to define voltage ramps at selected electrodes and computes voltages,

currents, and charge distribution at all contacts.

Subsequently, SDEVICE produces two kinds of output files. Firstly, it produces files containing the device geometry and results for various physical quantities (e.g. electrostatic potential, electron and hole densities, current densities) across the full device. Such files can be saved for any number of user-defined points during, e.g., a certain voltage ramp. Secondly, files containing electrical parameters (i.e. voltages, currents, and charge) for each contact are produced. From these files, it is possible to extract characteristics such as current-voltage (I–V) curves or capacitance-voltage (C–V) curves, depending on the defined simulation. The such produced files can be visualized using the tool Sentaurus Visual (SVISUAL) and directly exported to graphic or text files.

To control and design any set of simulation experiments, the Synopsys TCAD suite provides a graphical user interface (GUI), named *Sentaurus Workbench*. The GUI allows to generate and delete individual experiments, vary input parameters, combine simulation tools such as SDE and SDEVICE, and start and stop simulations of one or more individual experiments.

Generally, Synopsys TCAD is a powerful tool that provides the means to carry out fast and cost-effective experiments on self-defined semiconductor devices, however, to arrive at quantitative results in agreement with measurement results, many parameters have to be taken into account. Aside from the required knowledge of input parameters such as doping profiles and trapping models, the main limitations to consider are meshing and computation time, boundary conditions, and physics models. All of these areas require careful fine-tuning and trade-offs. With regard to these limitations, the simulations performed as part of this thesis mainly aim at modeling the qualitative behavior of test structures and, naturally, raise no claim to quantitative congruency with measurement results on real physical devices.

CHAPTER 6

TEST STRUCTURES FOR PROCESS QUALITY CONTROL

CMS process quality control (PQC) relies on test structure measurements to extract process parameters needed to monitor the quality and stability of the sensor production process. Test structures provide the means to comprehensively assess material quality and process stability without direct sensor measurements. The structures are manufactured on the same wafers as the main sensors, utilizing the empty space at the wafer periphery, and share the properties of the main sensors. Measurements of test structures are generally quick and less complicated than sensor measurements, and they can access parameters that are not accessible on the main sensors, including parameters that require destructive measurements.

The use of test structures for semiconductor characterization and process quality monitoring is well established in modern semiconductor industry. Device technology and structure design continue to rapidly advance, and structure types and measurement techniques have become manifold. An extensive discussion of devices and methods to determine semiconductor characteristics is provided in [43].

The PQC strategy for the CMS Phase-2 Upgrade draws from this wide variety of test structures and utilizes both well-understood standard test structures and structures developed and adapted for the requirements of high energy particle physics sensor production (Table 6.1). Part of the test structures are adapted from previous designs for the current CMS Tracker [58], including diodes, MOS capacitors, and gate-controlled diodes. CMS Phase-2 adds to this mix a number of standard and newly developed structures to allow for a more in-depth analysis of individual parameters that were not covered previously during CMS silicon sensor series production, including, but not limited to, van-der-Pauw type structures for measurement of the sheet resistance of different sensor layers, four-terminal structures to measure the bulk resistivity, MOSFET test structures to assess inter-channel properties, and cross-bridge Kelvin resistors to determine the contact resistance between metal and sensor implants.

The following sections discuss all process parameters that need to be evaluated to arrive at a comprehensive assessment of sensor and process quality in conjunction with the corresponding test structures. Each section focuses on a specific type of test structure and discusses the general function of the structure and the process parameters that can be extracted. Measurement results are presented and compared to simulations, and the feasibility of individual test structures to extract specific process parameters is discussed.

6.1 Diode

The *p-n* junction or diode is the most basic – while, arguably, the most important – test structure implemented for process quality control. Diodes constitute the basic building blocks of not only high-energy physics silicon sensors but of many other semiconductor devices. The electrical measurement of diodes is considerably simple, and the physical properties of the devices have been thoroughly investigated and are well understood. As

TABLE 6.1: Overview on test structures and process parameters that can be accessed with each structure. For each structure, the respective section number in the text is listed.

Section	Test structure	Process parameters
6.1	Diode	Leakage current, full depletion voltage, bulk resistivity, bulk carrier concentration, doping profile, bulk recombination lifetime, bulk generation lifetime
6.2	MOS capacitor (MOS-C)	Flatband voltage, fixed oxide charge concentration, oxide trapped charge, mobile oxide charge, interface trapped charge, oxide thickness, bulk carrier density
6.3	Gate-controlled diode (GCD)	Surface generation velocity, interface trap density, bulk generation lifetime
6.4	Van-der-Pauw structures	Sheet resistance of thin films, implant resistivity and doping concentration, line width
6.5	Meander	Sheet resistance
6.6	Four-terminal resistivity test structure	Bulk resistivity
6.7	MOSFET	Threshold voltage, p-stop doping concentration and implantation depth, inter-channel resistance
6.8	Cross-brigde Kelvin resistor (CBKR)	Contact resistance, specific contact resistivity
6.9	Contact chain	Process quality of contacts
6.10	Dielectric breakdown test structure	Breakdown voltage of the coupling dielectric
6.11	Capacitor with n^+ implant	Coupling capacitance, thickness of the coupling dielectric
6.12	Mask misalignment test structure	Relative misalignment of lithography masks
6.13.1	SRP test structure	Carrier density profile
6.13.2	SIMS test structure	Dopant concentration profile

such, diodes are well suited to study critical process parameters on silicon sensor production wafers. The devices provide access to wafer leakage current and full depletion voltage and, consequently, allow the extraction of substrate resistivity and doping concentration, active wafer thickness, and the doping profile as a function of depth from the semiconductor surface. Furthermore, diode measurements can give information about recombination and generation lifetimes.

While many diodes with different layouts are implemented on the CMS prototype and production wafers (Figure 6.1, Table 6.2), the basic design remains the same for all (Figure 6.1a). A planar n^+ implantation forms a p-n junction with the silicon substrate, and an n^+ guard ring and a p^+ edge ring surround the structure. The metalization atop all implants is extended beyond the implant edges to improve the high voltage stability of the device. Generally, this metal overhang is larger between guard ring and edge ring than between guard ring and n^+ pad because of the higher electric field in the region between edge ring and guard ring. A variation of the standard design features an additional p-stop implant between n^+ pad and guard ring (Figures 6.1b and 6.1d) that maintains isolation between diode pad and guard ring if they are kept on the same potential during current-voltage measurements (see section 6.1.1). The tracker wafers include both design versions, while the calorimeter wafers only feature the standard version without p-stop. In general, the periphery of all diodes is the same (i.e. distance between pad and guard ring, width of the guard ring implant, distance between guard ring implant and edge ring implant, and the width of the edge ring implant). In some cases, however, the width of the edge ring implant had to be decreased because of the limited space on the wafer. In particular, the edge ring is thinned down to a minimum width of $0.13\,\mathrm{mm}$ for a pair of $(5 \times 5)\,\mathrm{mm}^2$ diodes, with and without p-stop implant, located on the cut-off intended for irradiation on the CMS Tracker PS-p and PS-s production wafers. A set of six diodes with opened edge ring implants to enable metal connections to probe card contacts, labeled "QuadroDiodi" (Figure 6.2), is included on the Infineon PS-s prototype wafers. Additionally, all Infineon wafers include a diode with opened edge ring and probe card contacts, labeled "DiodeSetProto", that is part of the first prototype of a set of test structures for PQC (see section 7.1). The final version of the test

TABLE 6.2: List of diodes implemented on CMS prototype and production wafers and their design parameters, pad side lengths a and b and corner radius r_c for square and rectangular diodes, pad radius r for round diodes, radius r_{mo} of the metalization opening for laser signal injection, distance d_{ER} between guard ring implant and edge ring implant, minimum width w_{ER} of the edge ring implant, width w_{ps} of the *p*-stop implant for diodes with *p*-stop between pad and guard ring, and minimum metal overhang Δw_m. The distance d_{GR} between pad and guard ring and the width w_{GR} of the guard ring implant are $0.1\,\mathrm{mm}$ for all diodes.

	a (mm)	b (mm)	r_c (mm)	r (mm)	r_{mo} (mm)	d_{ER} (mm)	w_{ER} (mm)	w_{ps} (µm)	Δw_m (µm)
DiodeStandard	5		0.4		0.5	0.35	0.32		20
DiodePStop	5		0.4		0.5	0.35	0.13	6	20
DiodeHalf	2.5		0.5		0.2	0.35	0.32		20
DiodeHalfPStop	2.5		0.5		0.2	0.35	0.32	6	20
DiodeHalfPQC	2.5		0.2		0.2	0.35	0.25		20
DiodeQuarter	1.25		0.05		0.15	0.35	0.32		20
DiodeRound				2.5	0.5	0.35	0.32		20
DiodeRoundHalf				1.25	0.2	0.35	0.32		20
DiodeSetProto	10.8	2.46	0.4		0.5	0.3	0.15		22
QuadroDiodiN	11.17	1.43	0.4		0.25	0.35	0.37		20
QuadroDiodiNW	4		0.4		0.25	0.35	0.37		20
QuadroDiodiNE	2.56		0.4		0.25	0.35	0.37		20
QuadroDiodiSW	5		0.4		0.25	0.35	0.37		20
QuadroDiodiSE	3.2		0.4		0.25	0.35	0.37		20
QuadroDiodiS	10.2	2.45	0.4		0.25	0.35	0.37		20

structure set for automated PQC (see section 7.2) contains a diode of size $(1.25 \times 1.25)\,\mathrm{mm}^2$ with opened edge ring ("DiodeQuarter") and a diode of size $(2.5 \times 2.5)\,\mathrm{mm}^2$ with opened edge ring ("DiodeHalfPQC") that differs from the standard "DiodeHalf" (Figure 6.1c) only by the corner radius and the width of the edge ring implant. All diodes feature a circular opening in the aluminum metalization that supports the injection of a laser signal for testing.

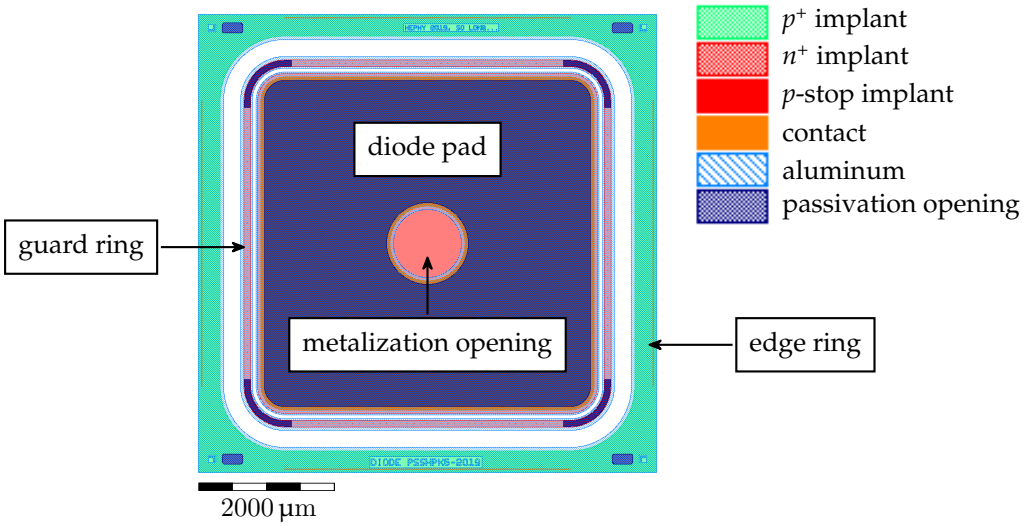
The following sections discuss all process parameters that are extracted from diodes as part of CMS process quality control and the functionality of diode measurements to assess these parameters.

6.1.1 Leakage Current

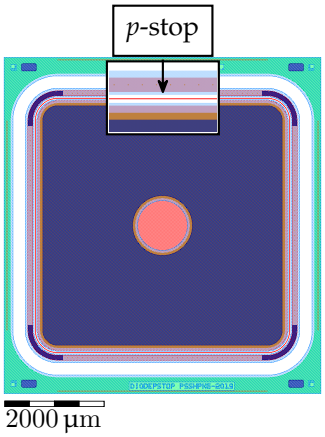
Diode leakage current directly relates to sensor leakage current and, consequently, is an important parameter to judge the quality of the delivered sensor material. The leakage current of a reverse-biased diode is caused by charge carrier diffusion from the neutral region into the diode space-charge region and carrier generation within the space-charge region. Especially after irradiation, which generates deep-level impurities that promote thermal generation of electron-hole pairs leading to a drastic increase of leakage current [51], the parameter critically affects sensor performance. Leakage current affects the signal-to-noise ratio of the sensor channels, which ultimately determines the position resolution. For DC-coupled sensors in particular, leakage current factors into the design of the readout electronics. The amplifiers of the readout chip must be able to cope with the constant DC current component. During detector operation, the sensors must be cooled to limit the leakage current and remove the power dissipation that would otherwise cause thermal runaway[1]. The silicon sensors in the CMS Outer Tracker are cooled to $\sim -20°\mathrm{C}$ [33] while the HGCAL sensors are operated at $\sim -30°\mathrm{C}$ [37].

Measurements of diode current-voltage (I–V) characteristics access the leakage current under reverse bias. Additionally, they allow to determine the breakdown voltage of the device. This parameter, however, can only serve as a tentative indicator of sensor high-voltage stability. Defects along the sensor area and layout effects that cause local peaks of the

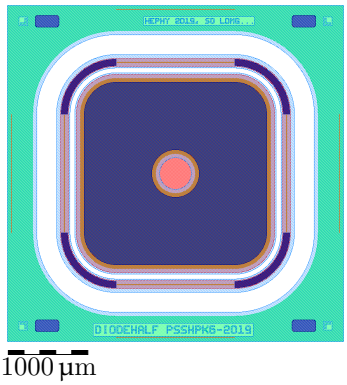
[1] If the power dissipation of the sensors is not removed by cooling, the steadily increasing temperature causes a concurrent increase of the leakage current. This positive feedback loop, which eventually causes the leakage current to grow beyond any limitations, is referred to as thermal runaway.



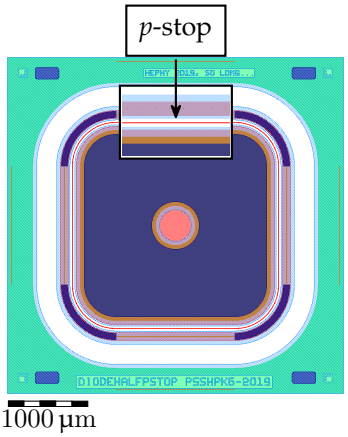
(A) $(5 \times 5)\,\mathrm{mm}^2$ diode ("DiodeStandard").



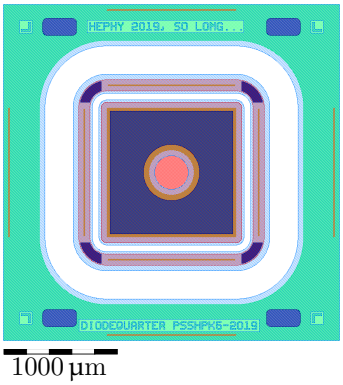
(B) $(5 \times 5)\,\mathrm{mm}^2$ diode with p-stop implant between n^+ pad and guard ring ("DiodeP-Stop").



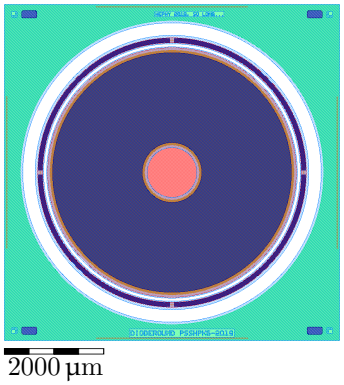
(C) $(2.5 \times 2.5)\,\mathrm{mm}^2$ diode ("DiodeHalf").



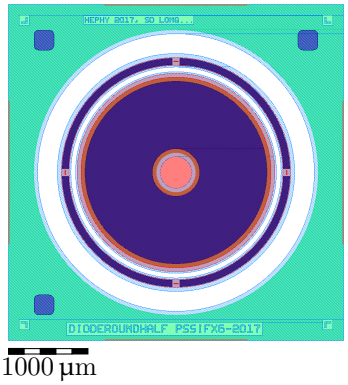
(D) $(2.5 \times 2.5)\,\mathrm{mm}^2$ diode with p-stop between pad and guard ring ("Diode-HalfPStop").



(E) $(1.25 \times 1.25)\,\mathrm{mm}^2$ diode ("DiodeQuar-ter").



(F) Round diode with radius 2.5 mm ("DiodeRound").



(G) Round diode with radius 1.25 mm ("DiodeRoundHalf").

FIGURE 6.1: Types of diodes implemented on CMS prototype and production wafers. Full list in Table 6.2.

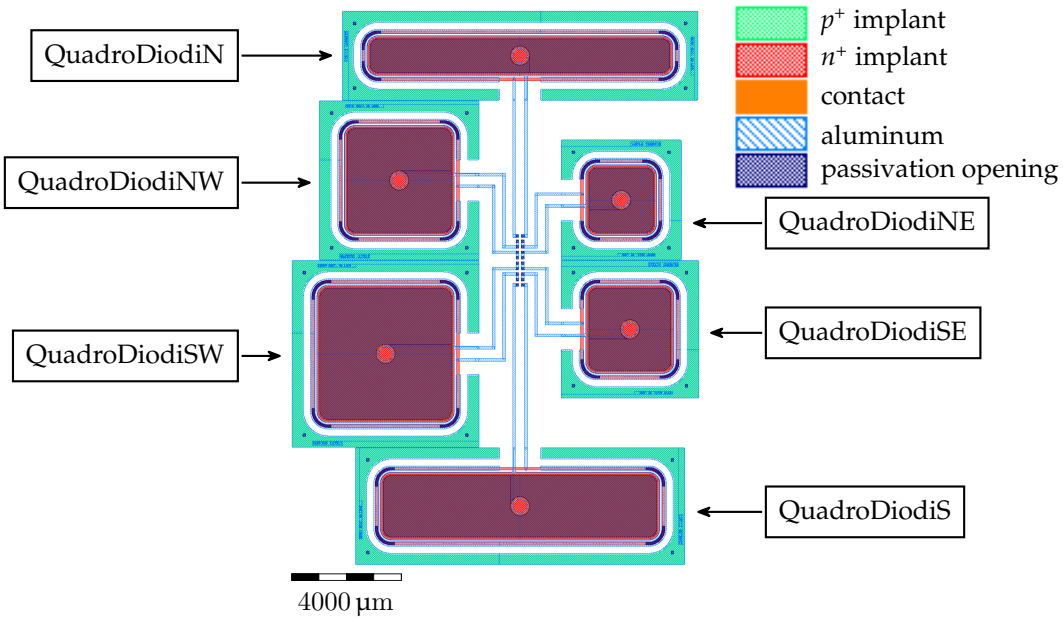
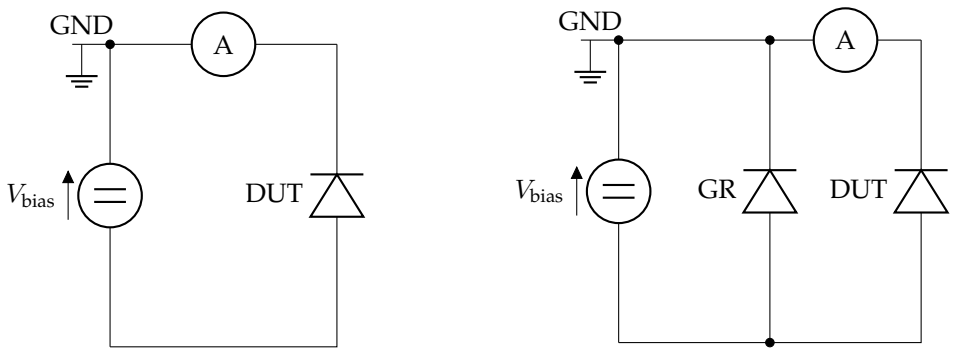


FIGURE 6.2: Set of six diodes with opened edge rings and probe card contacts in the center ("QuadroDiodi") included on Infineon PS-s prototype wafers.

electric field above the critical strength for avalanche breakdown (i.e. $\sim 300\,\mathrm{kV/cm}$) cannot be reproduced on test structure diodes and need high statistics to identify.

To measure the diode I–V characteristics, negative high voltage is ramped at the diode backplane, while the n^+ electrode on the front is kept on ground potential. If the same SMU sources the voltage and measures the current, parasitic currents that are introduced via the vacuum jig can distort the measurement. To limit the current measurement only to the diode current, an additional ammeter can be introduced between the diode n^+ electrode and ground (Figure 6.3a). If not stated otherwise, all I–V measurements presented in this thesis are performed using an ammeter in the voltage return path.

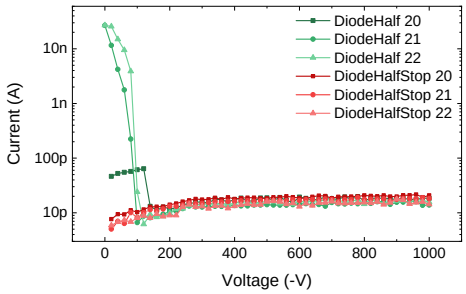
In case of large currents that are introduced via the diode periphery (compare section 7.3.1) and to limit the diode area, especially for measurements of irradiated devices, it can be beneficial to contact the diode guard ring during I–V measurements. In this case, the guard ring is kept on the same potential as the diode pad, and the ammeter between diode pad and ground is used to measure the diode current (Figure 6.3b). Parasitic currents that are introduced via the diode periphery are taken up by the guard ring and not measured at



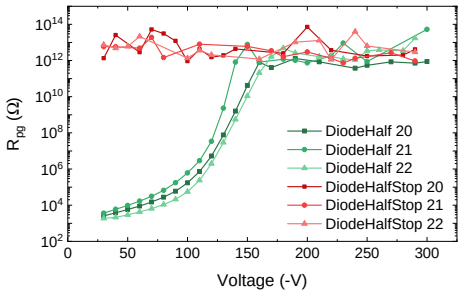
(A) Diode I–V measurement with floating guard ring.

(B) Diode I–V measurement with guard ring (GR) on ground potential.

FIGURE 6.3: Schematic of diode current-voltage (I–V) measurement.



(A) Current measured at the diode pad, with the guard ring kept at the same potential, as a function of the reverse bias voltage.



(B) Resistance between diode pad and guard ring (R_{pg}) as a function of the reverse bias voltage.

FIGURE 6.4: Diode I–V characteristics with guard ring kept at the same potential as the diode pad (A) and resistance between diode pad and guard ring (B), compared for diodes with (red) and without (green) p-stop implant between pad and guard ring. The measurements were performed on six square diodes with size $(2.5 \times 2.5)\,\mathrm{mm}^2$ on three different wafers (no. 20, 21, and 22) of the Tracker Pre-Series run. On each wafer, a diode without p-stop implant between pad and guard ring ("DiodeHalf") is compared to the diode with the same size featuring a p-stop implant between pad and guard ring ("DiodeHalfStop").

the diode pad. This assumption, however, only holds true if the guard ring is electrically isolated from the diode pad. This is naturally the case for p-on-n diodes. For n-on-p diodes, an additional p-stop implant is required between guard ring and diode pad to prevent a conductive interconnection as it would otherwise occur if the guard ring is kept on the same potential as the diode pad during current-voltage measurements. Without the additional p-stop implant between guard ring and diode pad, high currents are measured at the diode pad up until the point when the bias voltage is high enough that the depletion of the device establishes electrical isolation between diode pad and guard ring (Figure 6.4). For the Tracker Pre-Series, isolation between guard ring and n^+ pad is achieved at about $150\,\mathrm{V}$ reverse bias for diodes without p-stop implant.

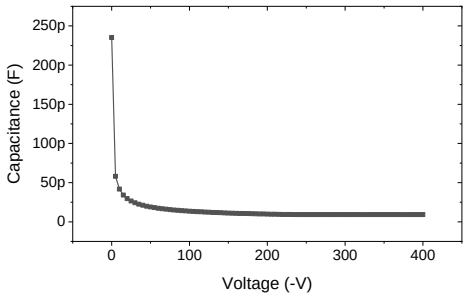
6.1.2 Full Depletion Voltage and Substrate Resistivity

Similar to the leakage current, full depletion voltage critically affects sensor operation under high radiation conditions. Radiation damage increases the effective doping concentration of p type sensors through a combination of donor removal and acceptor generation [51]. Consequently, the full depletion voltage increases with increasing radiation fluence. Additionally, radiation decreases the charge collection efficiency by introducing deep level traps [51], and sensors need to be operated beyond full depletion to compensate for the loss of charge collection efficiency and ensure a sufficiently high signal-to-noise ratio. The power supplies of the CMS Outer Tracker and HGCAL support a maximum operation voltage of $-800\,\mathrm{V}$ [33, 37]. With this in mind, appropriate limits must be set on the resistivity and full depletion voltage of the sensor base material to ensure sufficient signal output throughout detector lifetime.

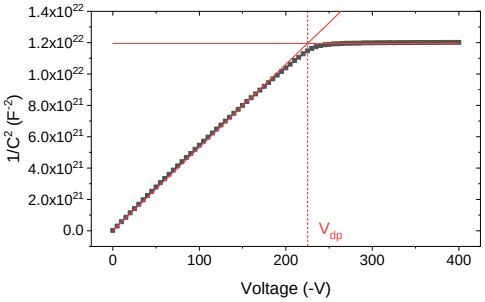
The full depletion voltage V_{dp} is extracted from diode capacitance-voltage (C–V) characteristics (Figure 6.5). For this purpose, the diode can be viewed as a simple parallel plate capacitor with the depletion region effectively acting as a dielectric between n and p type electrodes. The capacitance of a parallel plate capacitor is given by

$$C = \varepsilon_{\mathrm{Si}} \frac{A}{t} \,. \tag{6.1}$$

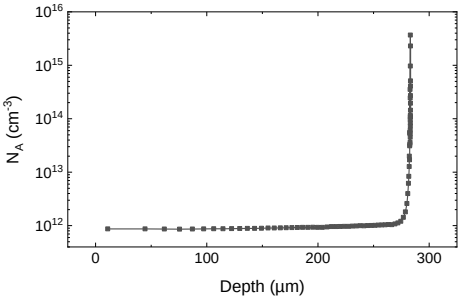
Here, A is the plate area, t is the thickness of the dielectric, and $\varepsilon_{\mathrm{Si}} = \varepsilon_0 \varepsilon_{\mathrm{r,Si}}$ denotes the



(A) Diode capacitance as a function of the reverse bias voltage.



(B) Full depletion voltage V_{dp} determined as the intersection point of two linear fits to $1/C^2$ as a function of the reverse bias voltage.



(C) Doping concentration N_{A} as a function of depth from the n^+-p junction.

FIGURE 6.5: Diode capacitance-voltage (C–V) characteristics (A), extraction of the full depletion voltage from the $1/C^2$-versus-V curve (B), and the resulting doping profile (C).

permittivity of silicon, composed of the vacuum permittivity ε_0 and the relative permittivity of silicon $\varepsilon_{\mathrm{r,Si}} = 11.68$.

Substituting the plate area with the area of the diode n^+ electrode and t with the depletion width of a one-sided abrupt n^+-p junction under reverse bias given in (3.13) yields the diode capacitance as a function of the bias voltage V:

$$C = A\sqrt{\frac{q\varepsilon_{\mathrm{Si}}N_{\mathrm{A}}}{2(V_{\mathrm{bi}}+V)}}\,. \tag{6.2}$$

With increasing reverse bias voltage, the depletion region and, thus, the effective thickness of the dielectric grows until it spans the active thickness of the silicon bulk. Correspondingly, the capacitance decreases with increasing reverse bias voltage until it reaches its minimum value C_{min} at full depletion (Figure 6.5a). If the reverse bias voltage is increased beyond V_{dp}, the capacitance does not decrease any further but retains a constant value. Consequently, the active thickness of the diode can be calculated from the minimum capacitance after full depletion using (6.1).

Plotting $1/C^2$ as a function of V produces a linear function for $V < V_{\mathrm{dp}}$. From (6.2) follows that the slope of the linear function gives the doping concentration

$$N_{\mathrm{A}} = \frac{2}{A^2 q\varepsilon_{\mathrm{Si}}\frac{\mathrm{d}(1/C^2)}{\mathrm{d}V}}\,, \tag{6.3}$$

and the intercept at $1/C^2 = 0$ gives an estimate[2] of the built-in potential V_{bi}. The full depletion voltage can be obtained from the $1/C^2$-versus-V characteristics as the intersection point of two linear fits in the regions below ($V < V_{\mathrm{dp}}$) and above ($V > V_{\mathrm{dp}}$) full depletion (Figure 6.5b).

With the extracted value of V_{dp}, the resistivity of the silicon bulk can be calculated by combining (3.6) and (3.13) as

$$\rho = \frac{t_{\mathrm{a}}^2}{2\varepsilon_{\mathrm{Si}}\mu_{\mathrm{p}}V_{\mathrm{dp}}}\,. \tag{6.4}$$

Here, t_{a} denotes the active thickness or maximum depletion width of the diode.

From (6.1), the depletion width W as a function of the bias voltage is

$$W(V) = \frac{\varepsilon_{\mathrm{Si}}A}{C(V)}\,. \tag{6.5}$$

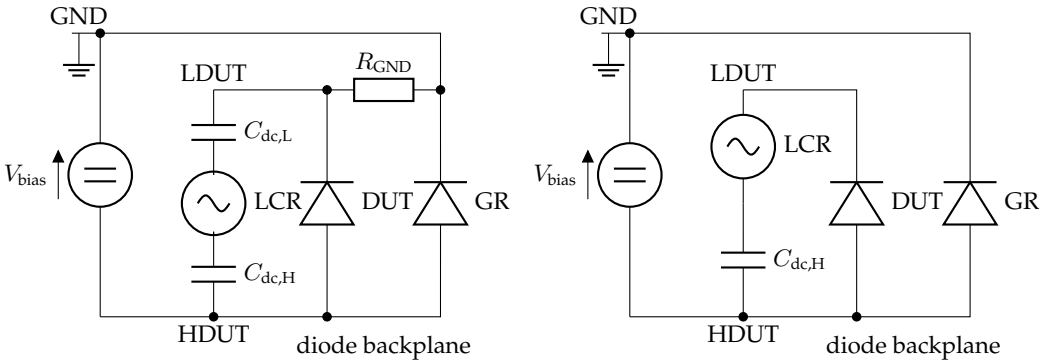
The doping profile of the diode can be extracted from the C–V characteristics by plotting the doping concentration $N_{\mathrm{A}}(V)$ for every bias voltage step versus the depletion width $W(V)$ (Figure 6.5c).

Approximating the diode capacitance with the capacitance of a parallel plate capacitor is only valid if the capacitive component of the diode periphery can be neglected. In that case, the accuracy of the process parameters extracted from C–V measurements depends on the accuracy with which the plate area A is known. Tying the guard ring to ground limits the influence of periphery capacitances and allows to better define the effective plate area. Essentially, two different measurement configurations for diode C–V characteristics with the guard ring tied to ground were implemented (Figure 6.6). In the first version, the reference ground of the guard ring is connected to the return path of the LCR meter via the ohmic element R_{GND} (Figure 6.6a). The second version of the schematic leaves out the connection between the parallel return paths of the DC bias voltage and the LCR meter, which effectively corresponds to $R_{\mathrm{GND}} = \infty$ (Figure 6.6b).

If, as in the first version of the circuit, the return paths of the DC bias and the LCR meter are connected, and $R_{\mathrm{GND}} = 0$, the guard ring capacitance affects the capacitance measurement, and the total measured capacitance is larger than for floating guard ring[3]

[2] Note that the intercept at $1/C^2 = 0$ systematically underestimates the built-in potential, typically by between 0.1 V and 0.4 V, and that the approximation in (6.2) introduces an error of the slope at low bias voltages that becomes more prevalent for strongly asymmetrical *p-n* junctions [81].

[3] Note that the measurement with $R_{\mathrm{GND}} = 0$ only works reliably if the "low" terminal of the LCR meter is capacitively decoupled from the DC voltage return path (by introducing $C_{\mathrm{dc,L}}$ in Figure 6.6a).



(A) Diode C–V measurement circuit with connected return paths. The resistor R_{GND} increases the impedance in the parallel path and suppresses the influence of the guard ring capacitance on the measurement result.

(B) Diode C–V measurement circuit with decoupled return paths ($R_{GND} = \infty$). The return path of the LCR meter (LDUT) has no direct connection to the reference ground (GND).

FIGURE 6.6: Schematic of diode capacitance-voltage (C–V) measurement with guard ring (GR) tied to ground. Juxtaposition of the circuit with connected voltage return paths (A) and circuit with decoupled return paths (B). The "high" and "low" terminals of the LCR meter are labeled "HDUT" and "LDUT", respectively. The capacitors $C_{dc,H}$ and $C_{dc,L}$ decouple the LCR meter from the applied DC voltage. $C_{dc,L}$ is only required if the return paths are connected and $R_{GND} = 0$. In the laboratory, the decoupling of the LCR meter is realized via a more complex decoupling circuit.

(Figure 6.7a). Introducing a sufficiently large resistor R_{GND} increases the impedance in the parallel path and suppresses the influence of the guard ring capacitance on the measurement result (Figure 6.7b). In that case, the measured capacitance is smaller than for floating guard ring, and periphery effects are effectively suppressed. The value of R_{GND} required to achieve a satisfactory suppression of the guard ring capacitance depends on the LCR meter AC frequency. At high frequencies, a lower value of R_{GND} achieves the same effect as a higher value of R_{GND} at low frequencies. For testing purposes, a value of $R_{GND} = 2\,\mathrm{M\Omega}$ was chosen. This configuration achieved comparable results at frequencies $1\,\mathrm{kHz}$, $10\,\mathrm{kHz}$, and $100\,\mathrm{kHz}$.

If the LCR return path is disconnected from the reference ground, as in the second version of the circuit, and R_{GND} is effectively increased to $R_{GND} = \infty$, the potential on the LCR return path is not known a priori. The results of capacitance measurements, however, are the same as with a $2\,\mathrm{M\Omega}$ resistor connecting the parallel return paths (Figure 6.7b). For this reason, and because this version of the circuit eliminates the influence of the guard ring on the capacitance measurement for all frequencies, the measurement configuration with the guard ring tied to ground and disconnected return paths (Figure 6.6b) was chosen for all measurements presented in this thesis unless stated otherwise.

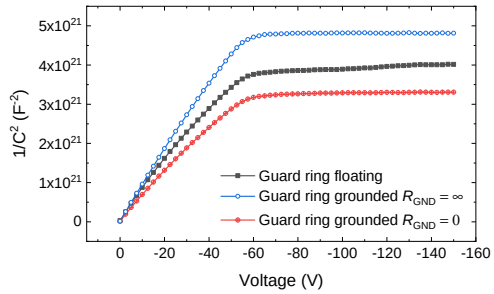
To achieve a satisfactory estimation of the effective plate area, the lateral spread of the depletion region below the *p*-*n* junction must be taken into account. The area of a square diode with rounded corners is given by

$$A = a^2 + r^2(\pi - 4)\,, \tag{6.6}$$

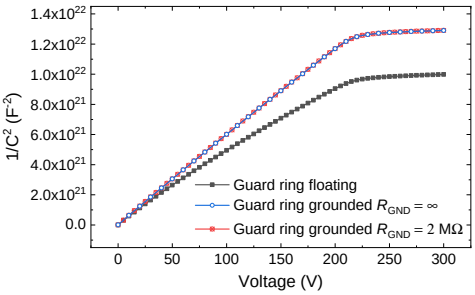
where a denotes the side length and r denotes the corner radius of the n^+ electrode. If the lateral spread of the depletion region of the diode under reverse bias $V > V_{dp}$ is denoted x, the effective plate area A_{eff} can be expressed as

$$A_{eff} = (a + 2x)^2 + (r + x)^2(\pi - 4)\,, \tag{6.7}$$

which simplifies to $A_{eff} = (r + x)^2\pi$ for a round diode with radius r. If the active thickness of the diode is known and the effects of the periphery are neglected, A_{eff} can be calculated from



(A) Floating guard ring compared to guard ring grounded with $R_{\text{GND}} = \infty$ and guard ring grounded with shorted return paths ($R_{\text{GND}} = 0$).



(B) Floating guard ring compared to guard ring grounded with $R_{\text{GND}} = \infty$ and guard ring grounded with connected return paths ($R_{\text{GND}} = 2\,\text{M}\Omega$).

FIGURE 6.7: $1/C^2$ as a function of the reverse bias voltage compared for floating guard ring (grey), guard ring grounded with decoupled return paths (blue), and guard ring grounded with connected return paths (red). Results are shown measured on a $(5 \times 5)\,\text{mm}^2$ diode of the Infineon $8''$ prototype run *VE543425* (A) and of the *n* type material of the current CMS Tracker (B).

TABLE 6.3: Effective plate area A_{eff} and lateral spread of the depletion region x for different diode sizes as calculated from C–V measurements on two 200 µm thick wafers (*2101* and *2103*) of the LD 2019 HGCAL protoype run. The statistical uncertainty of the capacitance at full depletion ΔC_{min} is estimated by averaging the results of the two wafers. The errors ΔA_{eff} and Δx are determined through propagation of ΔC_{min}.

Diode size	a (µm)	r (µm)	$C_{\text{min}} \pm \Delta C_{\text{min}}$ (pF)	$A_{\text{eff}} \pm \Delta A_{\text{eff}}$ (mm^2)	$x \pm \Delta x$ (µm)
Standard	5000	400	13.195 ± 0.035	25.519 ± 0.068	33.78 ± 0.35
Half	2500	500	3.415 ± 0.013	6.604 ± 0.024	60.87 ± 0.25
Quarter	1250	50	0.987 ± 0.002	1.91 ± 0.03	68.1 ± 0.6

(6.1). The lateral spread of the depletion region is then obtained by solving (6.7) for $x > 0$.

For the physically thinned HGCAL wafers, the active thickness equals the physical thickness minus the thickness of the aluminum layers. The manufacturer quotes the accuracy of the sensor thickness with $\pm 5\%$, while thickness measurements on test structures found $\pm 1\%$. With the known active thickness, the effective plate area and resulting lateral spread of the depletion region were calculated from diode C–V measurements on two 200 µm thick HGCAL wafers for three different diode sizes (Table 6.3). Even with the guard ring tied to ground, the calculated lateral spread of the depletion region strongly depends on the diode size. While the measurement of the standard ($(5 \times 5)\,\text{mm}^2$) diode yields a lateral extension of $x \approx 34\,\mu\text{m}$, the spread for the $(1.25 \times 1.25)\,\text{mm}^2$ diode, $x \approx 68\,\mu\text{m}$, is twice as large. The lateral spread for the half-sized diode ($(2.5 \times 2.5)\,\text{mm}^2$) falls closer to the value of the quarter-sized diode with $x \approx 61\,\mu\text{m}$. The observed dependency on diode size illustrates the effect of the periphery capacitance. This component of the diode capacitance scales with the circumference of the diode pad. For smaller diodes, the ratio of circumference/area is larger, and periphery effects play a more significant role. Particularly for small diodes, it becomes necessary to separate periphery effects from the planar capacitance component in order to extract active thickness and doping profile with sufficient accuracy.

The following section discusses the separation of planar capacitance and periphery capacitance.

6.1.3 Correction of Periphery Effects

The total capacitance C_{tot} of a diode is the sum of the backplane capacitance C_{back} and the periphery capacitance C_{peri}. Assuming that these two components scale with the area A of the n^+ pad and the circumference S of the n^+ pad, respectively, the total capacitance can be

written as

$$C_{\text{tot}} = C_{\text{back}} + C_{\text{peri}} = A \cdot C_{\text{planar}} + S \cdot C_{\text{edge}} \,. \tag{6.8}$$

The planar component of the capacitance is then given as the capacitance of a parallel plate capacitor with thickness t:

$$C_{\text{planar}} = \frac{\varepsilon_{\text{Si}}}{t} \,. \tag{6.9}$$

If the active thickness of the diode is known, the edge or perimeter component of the capacitance after full depletion can be calculated from the total capacitance and the planar capacitance after full depletion as

$$C_{\text{edge}} = \frac{C_{\text{tot}} - A \cdot C_{\text{planar}}}{S} \,. \tag{6.10}$$

Below full depletion, however, and if the active thickness is not a priori known, as is the case for the standard tracker material and the epitaxial HGCAL wafers, separating the planar and edge components becomes more challenging. For these cases, the method proposed in [82] allows to separate the capacitance components without knowledge of the active thickness:

If the capacitance is measured on two diodes with the same thickness and periphery layouts but different electrode areas A_{L} and A_{S} and circumferences S_{L} and S_{S}, the planar and edge components can be extracted as

$$C_{\text{planar}} = \frac{S_{\text{S}} \cdot C_{\text{L}} - S_{\text{L}} \cdot C_{\text{S}}}{S_{\text{S}} \cdot A_{\text{L}} - S_{\text{L}} \cdot A_{\text{S}}} \quad \text{and} \quad C_{\text{egde}} = \frac{A_{\text{S}} \cdot C_{\text{L}} - A_{\text{L}} \cdot C_{\text{S}}}{A_{\text{S}} \cdot S_{\text{L}} - A_{\text{L}} \cdot S_{\text{S}}} \,. \tag{6.11}$$

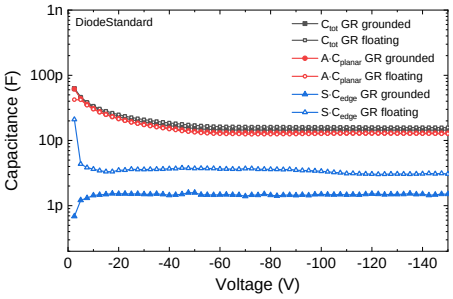
For two square diodes with side lengths a_{L} and a_{S} and neglected rounding of the corners, (6.11) becomes

$$C_{\text{planar}} = \frac{\frac{C_{\text{S}}}{a_{\text{S}}} - \frac{C_{\text{L}}}{a_{\text{L}}}}{a_{\text{S}} - a_{\text{L}}} \quad \text{and} \quad C_{\text{edge}} = \frac{\frac{a_{\text{L}}}{a_{\text{S}}} C_{\text{S}} - \frac{a_{\text{S}}}{a_{\text{L}}} C_{\text{L}}}{4(a_{\text{L}} - a_{\text{S}})} \text{ [82].} \tag{6.12}$$

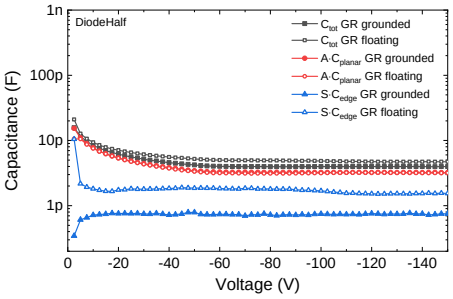
As briefly discussed in section 6.1.2 and demonstrated in [82], tying the guard ring of the diode to ground limits the influence of periphery capacitances. This effect is easily visualized by separating the planar and edge capacitance contributions from C–V measurements with floating guard ring and grounded guard ring on two diodes with different sizes (Figure 6.8). The measurement was performed on a standard diode ($A = (5 \times 5)\,\text{mm}^2$) and a diode with half the standard side length ($A = (2.5 \times 2.5)\,\text{mm}^2$) of the Infineon 2S prototype run *VE543425*. For the configuration with floating guard ring, the edge capacitance is more than twice as large as in the case of the guard ring grounded. The planar capacitance, on the other hand, retains a similar value in both cases. Since the edge capacitance scales with the circumference of the diode while the planar contribution scales with the diode area, the relative influence of the edge capacitance increases for the smaller diode (i.e. the diode with the higher circumference/area ratio).

To reliably extract the planar and edge contributions of the capacitance, the ratios of circumference/area must differ for the two diodes used for calculation. The influence of the diode size and the relative circumference/area ratio $(A_{\text{L}} \cdot S_{\text{S}})/(S_{\text{L}} \cdot A_{\text{S}})$ on the calculated planar and edge capacitance values was investigated on one wafer of the Infineon PS-s prototype run *VC811929* and one $200\,\mu\text{m}$ thick wafer (*2103*) of the LD 2019 HGCAL protoype run (Figure 6.9). On the Infineon PS-s prototype wafer, four different diode sizes were used for the calculation of the planar and edge capacitance: the standard square diode with side length $a = 5\,\text{mm}$, the standard round diode with radius $r = 2.5\,\text{mm}$, the half-size square diode with side length $a = 2.5\,\text{mm}$, and the half-size round diode with radius $r = 1.25\,\text{mm}$. On the $200\,\mu\text{m}$ HGCAL wafer, three square diodes were used: the standard diode, the half-size diode, and the quarter-size square diode with side length $a = 1.25\,\text{mm}$. For all square diodes, the rounding of the corners was taken into account and (6.11) was used for calculations.

For most combinations of diodes on one wafer, the results for planar and edge capacitances at $400\,\text{V}$ reverse bias (i.e. beyond full depletion) are consistent (Figures 6.9a, 6.9b). Significant variations are only observed if the sizes of the two diodes are very similar, as

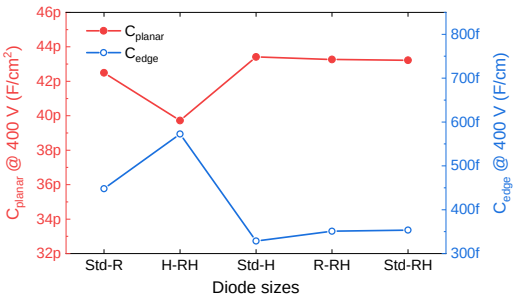


(A) Capacitance contributions of the $(5 \times 5)\,\mathrm{mm}^2$ diode ("DiodeStandard").

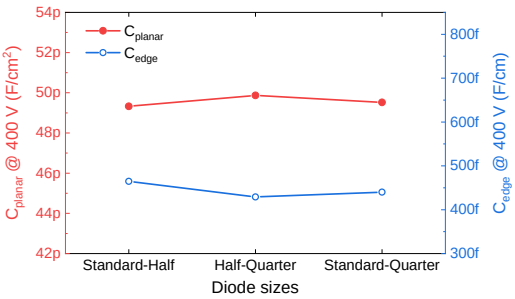


(B) Capacitance contributions of the $(2.5 \times 2.5)\,\mathrm{mm}^2$ diode ("DiodeHalf").

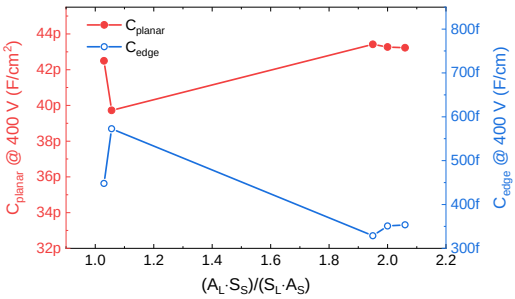
FIGURE 6.8: Planar (red circles) and edge (blue triangles) capacitance contributions on a $(5 \times 5)\,\mathrm{mm}^2$ diode (A) and a $(2.5 \times 2.5)\,\mathrm{mm}^2$ diode (B) for grounded and floating guard ring. The measurement was performed on diodes of the Infineon 8″ Tracker prototype run *VE543425*, and the simplified formula (6.12) was used to calculate the planar and edge contributions.



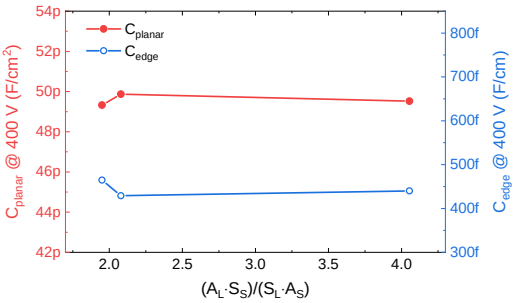
(A) Planar and edge capacitance measured on one Infineon PS-s wafer for every pair out of four different diodes: DiodeStandard (Std), DiodeRound (R), DiodeHalf (H), and DiodeRoundHalf (RH).



(B) Planar and edge capacitance measured on one 200 µm thick HGCAL wafer for every pair out of three different diodes: DiodeStandard (Standard), DiodeHalf (Half), and DiodeQuarter (Quarter).

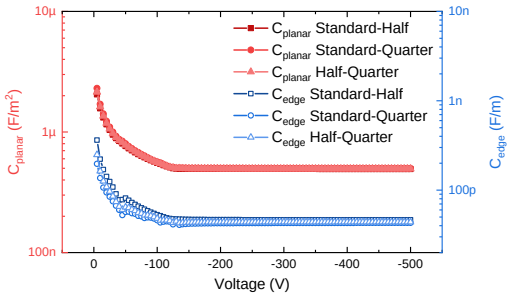


(C) Planar and edge capacitance as a function of the relative circumference/area ratio of the diodes used for calculation (Infineon PS-S).

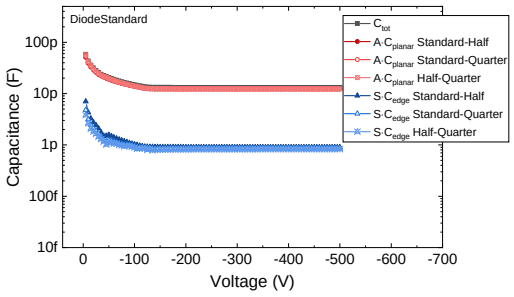


(D) Planar and edge capacitance as a function of the relative circumference/area ratio of the diodes used for calculation (200 µm HGCAL).

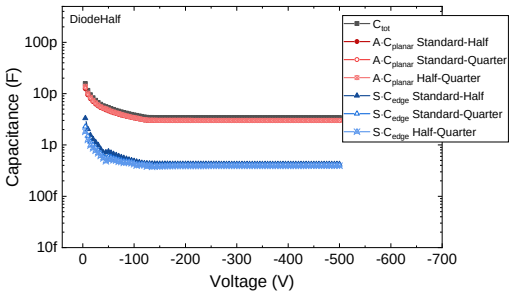
FIGURE 6.9: Planar (red, left y-axis) and edge (blue, right y-axis) capacitance components at 400 V reverse bias, calculated from C–V measurements on diodes with different sizes on one wafer of the Infineon 6″ PS-s prototype run *VC811929* (A, C) and one 200 µm thick wafer (*2103*) of the LD 2019 HGCAL protoype run (B, D). The results are compared with respect to the diode sizes (A, B) and the relative circumference/area ratio (C, D).



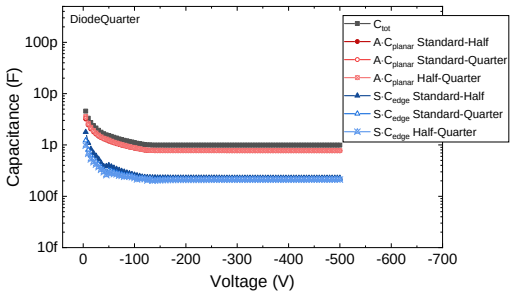
(A) Planar (left y-axis) and edge capacitance (right y-axis).



(B) Planar and edge capacitance of the $(5 \times 5)\,\mathrm{mm}^2$ diode ("DiodeStandard").



(C) Planar and edge capacitance of the $(2.5 \times 2.5)\,\mathrm{mm}^2$ diode ("DiodeHalf").



(D) Planar and edge capacitance of the $(1.25 \times 1.25)\,\mathrm{mm}^2$ diode ("DiodeQuarter").

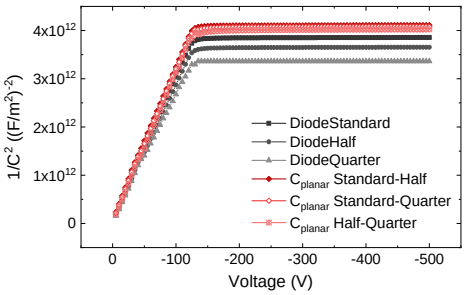
FIGURE 6.10: Planar (red) and edge (blue) capacitance components calculated from C–V measurements on three diodes with sizes $(5 \times 5)\,\mathrm{mm}^2$, $(2.5 \times 2.5)\,\mathrm{mm}^2$, and $(1.25 \times 1.25)\,\mathrm{mm}^2$ on one 200 µm thick wafer (*2103*) of the LD 2019 HGCAL protoype run. The capacitance components (A) are calculated for every pair out of three diodes and are compared for each diode size (B–D).

is the case if the standard square diode is combined with the standard round diode or if the half-size square diode is paired with the half-size round diode (Figure 6.9a). For these combinations of diodes, the ratio $(A_\mathrm{L} \cdot S_\mathrm{S})/(S_\mathrm{L} \cdot A_\mathrm{S}) \approx 1$, while in all other cases $(A_\mathrm{L} \cdot S_\mathrm{S})/(S_\mathrm{L} \cdot A_\mathrm{S}) \approx 2$ or greater (Figures 6.9c, 6.9d). It can be concluded that diodes with a relative circumference/area ratio $(A_\mathrm{L} \cdot S_\mathrm{S})/(S_\mathrm{L} \cdot A_\mathrm{S}) \geq 2$ are preferable to reliably separate the planar and edge capacitance contributions[4].

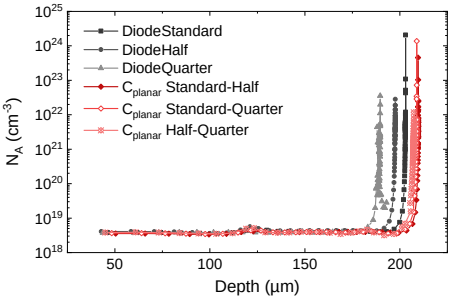
If $(A_\mathrm{L} \cdot S_\mathrm{S})/(S_\mathrm{L} \cdot A_\mathrm{S}) \geq 2$ is fulfilled, the extracted planar and edge capacitance values as a function of the reverse bias voltage are largely independent of the diode pair used for calculation. This observation is illustrated below for all combinations of three diodes on the $200\,\mu\mathrm{m}$ thick HGCAL wafer (Figure 6.10a). The low influence of the chosen diode pair holds true also for the backplane and periphery components ($A \cdot C_\mathrm{planar}$ and $S \cdot C_\mathrm{edge}$) for all diode sizes (Figure 6.10b–6.10d). Minor deviations that depend on the combination of diodes are observed for voltages below full depletion. The $1/C^2$-versus-V characteristics of the planar component (Figure 6.11a) and the resulting doping profiles (Figure 6.11b), however, are largely consistent for all diode combinations.

Without applying edge corrections, C–V characteristics of single diodes systematically overestimate the capacitance after full depletion (Table 6.4). The resulting error affects the calculation of the active thickness and the extracted doping profiles (Figure 6.11b). It also has a notable, albeit less substantial, influence on the extracted substrate resistivity and doping concentration. The effect is especially pronounced for smaller diodes, for which the relative effects of edge capacitances are greater. The full depletion voltage, on the other hand, is extracted with sufficient accuracy also from single diode measurements and a correction of

[4]Note that, with the available set of diodes, no statement can be made about the range $1 < (A_\mathrm{L} \cdot S_\mathrm{S})/(S_\mathrm{L} \cdot A_\mathrm{S}) \leq 2$. The data can only support the reliability of the extraction of planar and edge capacitances using diode pairs for which $(A_\mathrm{L} \cdot S_\mathrm{S})/(S_\mathrm{L} \cdot A_\mathrm{S}) \geq 2$.



(A) $1/C^2$ values normalized to $1\,\mathrm{m}^2$ as a function of the reverse bias voltage.



(B) Acceptor concentration N_A as a function of depth from the n^+-p junction.

FIGURE 6.11: $1/C^2$ (A) and doping profiles (B) extracted from the measured total capacitance (grey) and from the planar capacitance components (red). The planar capacitance is calculated for each pair out of three diodes with sizes $(5 \times 5)\,\mathrm{mm}^2$, $(2.5 \times 2.5)\,\mathrm{mm}^2$, and $(1.25 \times 1.25)\,\mathrm{mm}^2$ on one $200\,\mu\mathrm{m}$ thick wafer (*2103*) of the LD 2019 HGCAL protoype run. The effective area used for the normalization of the $1/C^2$ curves and the calculation of the doping profile assumes a lateral extension of the depletion zone to 50% of the distance between diode pad and guard ring. A summary of the process parameters extracted from the measurements is given in Table 6.4.

TABLE 6.4: Full depletion voltage V_dp, capacitance after full depletion C_min, active thickness t_a, substrate resistivity ρ, and effective doping concentration N_A extracted from C–V measurements of three different diodes on one $200\,\mu\mathrm{m}$ thick wafer (*2103*) of the LD 2019 HGCAL protoype run. The results from C–V measurements on single diodes with sizes $(5 \times 5)\,\mathrm{mm}^2$ ("DiodeStandard"), $(2.5 \times 2.5)\,\mathrm{mm}^2$ ("DiodeHalf"), and $(1.25 \times 1.25)\,\mathrm{mm}^2$ ("DiodeQuarter") are compared to the process parameters extracted from the planar capacitance component calculated for every possible pair of diodes. The calculations using the single diode measurements assume a lateral extension of the depletion zone to 50% of the distance between diode pad and guard ring.

	V_dp (V)	C_min (pF/cm^2)	t_a (µm)	ρ (kΩ cm)	N_A (10^{12}cm^{-3})
DiodeStandard	125.4	52.97	203	3.32	3.93
DiodeHalf	125.8	56.41	197	3.14	4.17
DiodeQuarter	124.1	63.39	190	2.94	4.46
C_planar Standard-Half	124.4	49.35	210	3.58	3.66
C_planar Standard-Quarter	125.8	49.56	209	3.51	3.73
C_planar Half-Quarter	127.2	49.94	207	3.42	3.83

edge effects is not strictly necessary if only this parameter is of interest.

The study in [82] finds that the exact choice of the diode area and circumference used for separating planar and edge contributions does not have a significant impact on results. This observation can be confirmed with the results presented in this thesis. If, instead of the diode pad area, a lateral extension of the area to 50% of the distance between diode pad and guard ring is assumed and the planar and edge contributions are calculated using the resulting area and circumference, the active thickness of the $200\,\mu\mathrm{m}$ thick HGCAL wafer becomes $209\,\mu\mathrm{m}$, $208\,\mu\mathrm{m}$, and $206\,\mu\mathrm{m}$, respectively, for the diode combinations Standard-Half, Standard-Quarter, and Half-Quarter (compare Table 6.4). This low impact of the exact area and circumference values, however, only holds true if the circumference/area ratio is not affected. If, for square diodes, the rounding of the corners is neglected and a perfect square is assumed, the circumference/area ratio changes by 3%, 5%, and 2% for the $(5 \times 5)\,\mathrm{mm}^2$, $(2.5 \times 2.5)\,\mathrm{mm}^2$, and $(1.25 \times 1.25)\,\mathrm{mm}^2$ diodes, respectively. In these cases, the impact on the doping profile extracted from the planar capacitance contribution becomes significant (Figure 6.12). The active thickness extracted assuming a perfect square deviates from the value obtained when taking into account the rounded corners by 3%, 0.5%, and 10% for the $(5 \times 5)\,\mathrm{mm}^2$, $(2.5 \times 2.5)\,\mathrm{mm}^2$, and $(1.25 \times 1.25)\,\mathrm{mm}^2$ diodes, respectively. For accurate extraction of the active thickness and the doping profile, it is thus recommended to take into

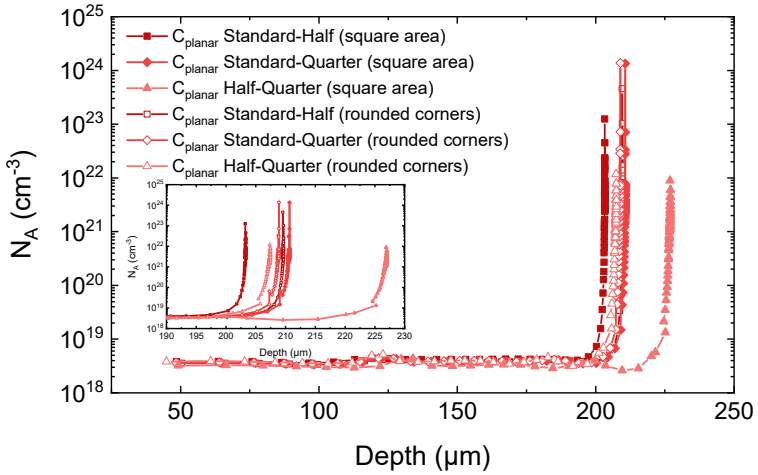


FIGURE 6.12: Influence of the definition of the diode area on the doping profile extracted using the planar capacitance component. The planar capacitance is calculated for all possible pairs out of three square diodes with sizes $(5 \times 5)\,\mathrm{mm}^2$ ("DiodeStandard"), $(2.5 \times 2.5)\,\mathrm{mm}^2$ ("DiodeHalf"), and $(1.25 \times 1.25)\,\mathrm{mm}^2$ ("DiodeQuarter") on one $200\,\mu\mathrm{m}$ thick wafer (*2103*) of the LD 2019 HGCAL protoype run. Results assuming a perfect square area are compared to the results that take into account the rounded corners.

account the rounded corners of square diodes.

6.1.4 Carrier Lifetimes

Carrier lifetimes are a measure for the defect density in semiconductor material and, thus, are frequently used to monitor the "cleanliness" of the semiconductor production process [43]. Lifetimes are separated into *recombination lifetimes* and *generation lifetimes* [83].

A semiconductor in thermal equilibrium satisfies the relation $pn = n_\mathrm{i}^2$. If excess carriers are introduced to the semiconductor and $pn > n_\mathrm{i}^2$ (e.g. in a forward-biased *p-n* junction), the system strives to restore equilibrium through recombination of excess carriers. Conversely, if there is a lack of carriers and $pn < n_\mathrm{i}^2$ (e.g. in the space-charge region of a reverse-biased *p-n* junction), carriers will be generated to restore equilibrium. The average time after which an electron-hole pair ceases to exist is given by the recombination lifetime τ_r. Generation lifetime τ_g, on the other hand, refers to the time it takes on average to generate an electron-hole pair. The lifetimes τ_r and τ_g characterize recombination and generation events that occur in the semiconductor bulk. At the semiconductor surface, these events are characterized by the *surface recombination velocity* s_r and the *surface generation velocity* s_g, which is sometimes also designated as s_0.

Considering a *p* type semiconductor, recombination lifetime is defined as

$$\tau_\mathrm{r} = \frac{\Delta n}{R}\,, \tag{6.13}$$

where Δn is the excess electron density, which in the absence of trapping is equal to the excess hole density Δp, and R is the bulk recombination rate, which depends nonlinearly on Δn [43]. The main recombination mechanisms determining the lifetime are *Shockley-Read-Hall* (SRH) or *multiphonon* recombination, *radiative* recombination, and *Auger* recombination. From these contributions, the recombination lifetime is determined as

$$\frac{1}{\tau_\mathrm{r}} = \frac{1}{\tau_\mathrm{SRH}} + \frac{1}{\tau_\mathrm{rad}} + \frac{1}{\tau_\mathrm{Auger}}\,. \tag{6.14}$$

SRH recombination [84, 85] takes place via deep-level impurities (i.e. traps), and the liberated energy is dissipated by lattice vibrations (i.e. phonons). It is independent of Δn. Radiative

recombination [86, 87] is a band-to-band process in which the energy is carried away by a photon. It depends inversely on Δn because both electrons and holes must be present simultaneously. During Auger recombination, the energy is absorbed by a third carrier (i.e. an electron or a hole), and the lifetime, thus, depends inversely on $(\Delta n)^2$. For an indirect semiconductor such as silicon, radiative recombination plays almost no role. Auger recombination dominates at high carrier densities. For low carrier densities, SRH recombination is by far the dominant process, and the *bulk recombination rate* is given by

$$R = \frac{(pn - n_\mathrm{i}^2)}{\tau_p(n + n_1) + \tau_n(p + p_1)} \,. \tag{6.15}$$

Here, τ_n and τ_p are electron and hole lifetimes, given by the respective carrier capture cross-sections σ_n and σ_p, the deep-level trap density N_T, and the electron thermal velocity v_th as

$$\tau_n = \frac{1}{\sigma_n v_\mathrm{th} N_\mathrm{T}} \quad \text{and} \quad \tau_p = \frac{1}{\sigma_p v_\mathrm{th} N_\mathrm{T}} \,, \tag{6.16}$$

and n_1 and p_1 are defined as

$$n_1 = n_\mathrm{i} \exp(\frac{E_\mathrm{T} - E_\mathrm{i}}{kT}) \quad \text{and} \quad p_1 = n_\mathrm{i} \exp(-\frac{E_\mathrm{T} - E_\mathrm{i}}{kT}) \,, \tag{6.17}$$

where E_T is the trap energy level and E_i is the intrinsic Fermi level.

Generation mechanisms, in principle, are the inverse counterparts of the processes relevant for recombination. Thermal generation of electron-hole pairs via intermediate energy levels is the inverse process of SRH recombination. The counterparts for radiative recombination and Auger recombination are optical generation and impact ionization or avalanche multiplication. The latter two processes are largely negligible for a device in the dark and under low field conditions.

For $pn < n_\mathrm{i}^2$, generation dominates compared to recombination. In this case, the recombination rate in (6.15) becomes negative and is designated as the *bulk generation rate*

$$G = -R = \frac{n_\mathrm{i}^2}{\tau_p n_1 + \tau_n p_1} = \frac{n_\mathrm{i}}{\tau_\mathrm{g}} \tag{6.18}$$

for $pn \approx 0$. Generally, the generation lifetime τ_g is higher than the recombination lifetime τ_r. For silicon devices, in particular, τ_g has been found to be about 50 to 100 times higher than τ_r [43].

In analogy to the bulk lifetimes, the *surface recombination velocity* s_r and *surface generation velocity* s_g are defined as

$$s_\mathrm{r} = \frac{R_\mathrm{s}}{\Delta n_\mathrm{s}} \tag{6.19}$$

and, with $p_\mathrm{s} n_\mathrm{s} < n_\mathrm{i}^2$ at the surface,

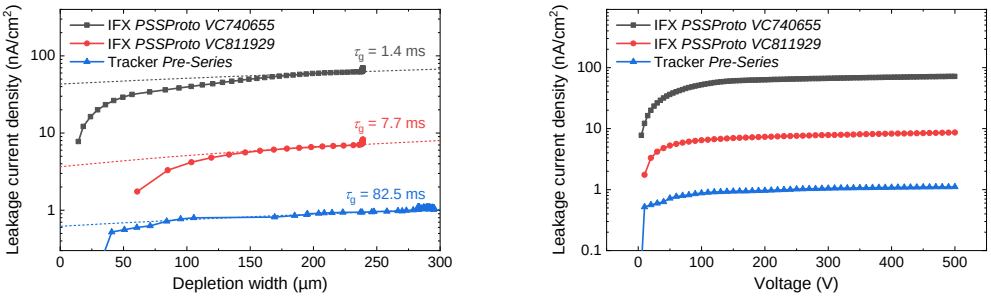
$$s_\mathrm{g} = \frac{G_\mathrm{s}}{n_\mathrm{i}} \,. \tag{6.20}$$

Here, the subscript "s" refers to the appropriate quantity at the semiconductor surface.

A method to extract bulk recombination and generation lifetime from diode I–V and C–V measurements is presented in [88]. The total leakage current J_tot of a *p-n* junction is composed of a diffusion component J_diff, caused by generation in the neutral region and diffusion into the space-charge region, a bulk generation component J_g, caused by generation in the space-charge region, and a surface generation component J_sg:

$$J_\mathrm{tot} = J_\mathrm{diff} + J_\mathrm{g} + J_\mathrm{sg} \,. \tag{6.21}$$

For sufficiently large junctions (i.e. $\sim 1\,\mathrm{mm}^2$), J_sg can be neglected. J_diff and J_g can then be extracted by plotting the total leakage current density J_tot as a function of the depletion width W and fitting a linear function to the J–W characteristics. The extrapolated value at $W = 0$ corresponds to the diffusion current component J_diff, and the generation component



(A) Diode J–W characteristics and extracted τ_g.

(B) J–V characteristics of reverse biased diodes.

FIGURE 6.13: Extraction of generation lifetime τ_g from diode leakage current density J versus depletion width W characteristics (A) calculated from J–V (B) and C–V measurements according to [88]. A linear function is fitted to the approximately linear end of the J–W curve. The intercept at $W = 0$ corresponds to the diffusion current component J_{diff}, and the slope relates to τ_g via (6.23). Measurements are compared for three wafers of the Infineon *VC740655* and *VC811929* PS-s prototype runs and Tracker Pre-Series. W is calculated from the planar capacitance component, using "DiodeRound" ($r = 2.5\,\text{mm}$) and "DiodeRoundHalf" ($r = 1.25\,\text{mm}$) in case of the Infineon wafers and "DiodeStandard" ($(5\times5)\,\text{mm}^2$) and "DiodeHalf" ($(2.5\times2.5)\,\text{mm}^2$) in case of the Tracker Pre-Series wafer. J is calculated from the leakage current of the larger diode of each pair, assuming an effective area extending to the outer edge of the guard ring implant. Extracted parameters are summarized in Table 6.5. Note the logarithmic scaling of the current axes.

J_g as a function of the applied voltage V can be calculated as

$$J_g(V) = J_{\text{tot}}(V) - J_{\text{diff}}\,. \tag{6.22}$$

The slope g of the linear function fitted to the J–W characteristics relates to the generation lifetime τ_g via

$$\tau_g = \frac{q n_i}{g}\,, \tag{6.23}$$

where q denotes the elementary charge. Lastly, if the electron diffusion constant D_n is known, the recombination lifetime can be calculated from the diffusion current component J_{diff} and the carrier density N_A as

$$\tau_r = \frac{q^2 n_i^2}{J_{\text{diff}}^2 N_A^2} D_n\,. \tag{6.24}$$

The method was applied to three wafers of the Infineon *VC740655* and *VC811929* PS-s prototype runs and the Tracker Pre-Series (Figure 6.13). The J–W plot (Figure 6.13a) was calculated combining I–V and C–V measurements of the same diodes on each wafer. The leakage current density J_{tot} was obtained from diode I–V measurements on "DiodeRound" ($r = 2.5\,\text{mm}$) in case of the Infineon wafers and "DiodeStandard" ($(5 \times 5)\,\text{mm}^2$) in case of the Tracker Pre-Series wafer (Figure 6.13b). The current was normalized to the effective area of the junction (i.e. taking into account the lateral extension of the space-charge region). In all cases, an effective area extending to the outer edge of the guard ring implant was assumed. The depletion width W was calculated from diode C–V characteristics, using (6.5). To accurately calculate W from C–V data, periphery and parasitic capacitances must be eliminated [89, 90]. For this purpose, C–V data were measured for two diodes of different sizes on each wafer, and the planar capacitance component (see section 6.1.3) was used to derive W. For the Infineon wafers, "DiodeRound" ($r = 2.5\,\text{mm}$) and "DiodeRoundHalf" ($r = 1.25\,\text{mm}$) were used; and "DiodeStandard" ($(5 \times 5)\,\text{mm}^2$) and "DiodeHalf" ($(2.5 \times 2.5)\,\text{mm}^2$) were used in case of the Tracker Pre-Series wafer.

Contrary to results shown in [88–90], the obtained J–W characteristics exhibit distinctly

TABLE 6.5: Total current density J_{tot}, diffusion component J_{diff}, generation component J_{g}, and generation lifetime τ_{g} extracted from diode J–W characteristics calculated from diode J–V and C–V measurements on three wafers of the Infineon *VC740655* and *VC811929* PS-s prototype runs and Tracker Pre-Series (compare Figure 6.13). Current densities are calculated at full depletion voltage V_{dp} for each wafer, respectively.

Wafer type	V_{dp} (V)	J_{tot} (nA/cm^2)	J_{diff} (nA/cm^2)	J_{g} (nA/cm^2)	τ_{g} (ms)
VC740655	185	62.48	43.13	19.35	1.4
VC811929	160	7.04	3.65	3.39	7.7
Pre-Series	260	1.02	0.62	0.40	82.5

nonlinear behavior, which may be attributed to periphery effects and the largely unknown lateral extension of the space-charge region during I–V measurements[5]. The influence of these effects is expected to be greater at lower bias voltages. To minimize the impact of these effects on parameter extraction, the linear function was fitted to the approximately linear high-voltage end of the J–W characteristics. The extracted parameters are summarized in Table 6.5. The generation lifetimes extracted for the Infineon wafers are comparable to results from gate-controlled diode measurements on the same wafers (see section 6.3), indicating that the extraction of τ_{g} from diode I–V and C–V measurements was successful despite the observed nonlinearity of J–W characteristics.

6.2 Metal-Oxide-Semiconductor Capacitor

Metal-oxide-semiconductor capacitors (MOS-C) are standard tools for determining general properties of the Si-SiO_2 interface [43]. Fixed oxide charge, oxide trapped charge, mobile oxide charge, interface trapped charge, and oxide thickness can be extracted from MOS-C capacitance–voltage (C–V) characteristics. In addition, MOS-C characteristics can provide an estimate of the carrier concentration of the silicon bulk.

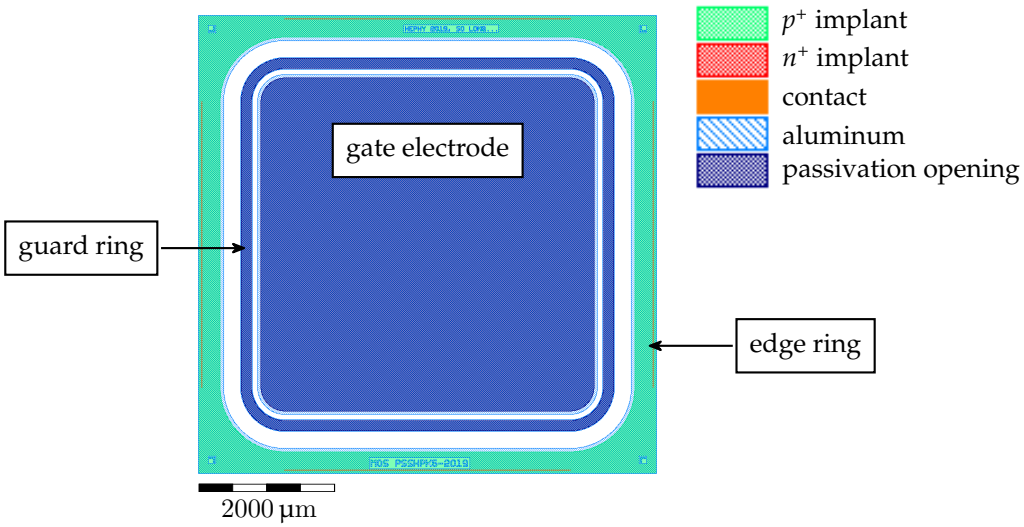
In principle, a MOS-C consists of an insulating SiO_2 layer sandwiched between the silicon bulk and a metal gate electrode. Further, a guard ring and a p^+ edge ring may be part of the design to shield the device against influences from surrounding structures. The MOS-C implemented on CMS prototype and production wafers vary in terms of shape and size of the gate electrode and guard ring design (Figure 6.14, Table 6.6). For most prototype wafers, the guard ring models the diode design (see section 6.1) and includes an n^+ implant. This implant is removed from the design for all production wafers and more recent HGCAL prototypes to avoid distortion of measurement results caused by the depletion of the device in case the guard ring needs to be tied to ground. Infineon 2S prototype wafers include a MOS-C without guard ring and edge ring, labeled "MOSSetProto2S", that is part of the first prototype of a PQC test structure set [67]. The adapted version of the set (see section 7.1) includes a smaller MOS-C with slimmed down guard rings, labeled "MOSSetProtoPSs". The final version of the test structure set for automated PQC (see section 7.2) contains an MOS-C with gate size $(1.29 \times 1.29)\,\text{mm}^2$ and opened edge ring, labeled "MOSQuarter".

The following sections discuss the functionality of MOS-C to extract the fixed oxide charge concentration, oxide thickness, and bulk carrier concentration.

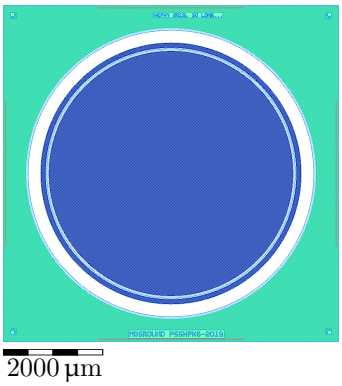
6.2.1 Flatband Voltage and Fixed Oxide Charge Concentration

Fixed oxide charge refers to positive charges in the oxide near the Si-SiO_2 interface. In contrast to interface trapped charge, fixed oxide charge is not in electrical communication with the underlying silicon bulk. While interface traps can be charged and discharged by carriers at the silicon surface, fixed oxide charges remain "fixed". The concentration of fixed oxide charges is an important indicator for the quality of the Si-SiO_2 interface. An initially high concentration of fixed oxide charges increases more strongly under irradiation [91],

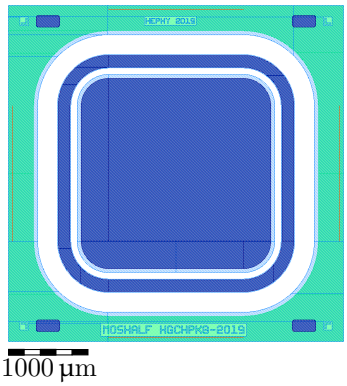
[5]Tying the guard ring to ground during the I–V measurement would likely limit the error introduced by the lateral extension of the space-charge region and the error resulting from normalization to an assumed effective area of the junction. However, because most diode types lack a p-stop implant between diode pad and guard ring, a feasible measurement with the guard ring tied to ground is not possible (compare section 6.1.1).



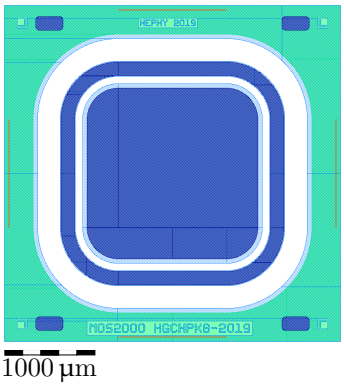
(A) $(5 \times 5)\,\mathrm{mm}^2$ MOS-C ("MOSStandard").



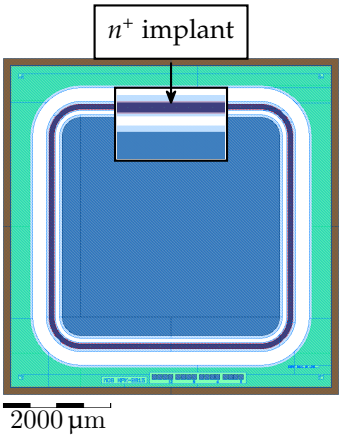
(B) Round MOS-C with radius 2.5 mm ("MOSRound").



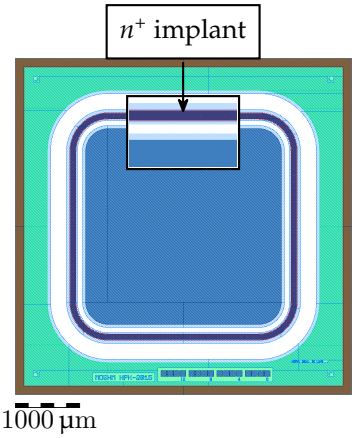
(C) $(2.5 \times 2.5)\,\mathrm{mm}^2$ MOS-C ("MOSHalf").



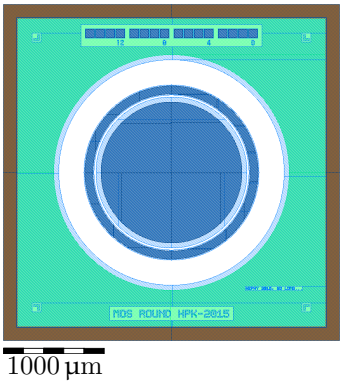
(D) $(2 \times 2)\,\mathrm{mm}^2$ MOS-C ("MOS2000").



(E) $(4.16 \times 4.16)\,\mathrm{mm}^2$ MOS-C with n^+ guard ring ("MOSHPK").



(F) $(3.16 \times 3.16)\,\mathrm{mm}^2$ MOS-C with n^+ guard ring ("MOSHMHPK").



(G) Round MOS-C with radius 0.75 mm ("MOSRoundHPK").

FIGURE 6.14: Types of MOS-C implemented on CMS prototype and production wafers. On all prototype wafers, MOS capacitors (A)–(D) include an n^+ implant below the guard ring metalization. Full list in Table 6.6.

TABLE 6.6: List of MOS capacitors implemented on CMS prototype and production wafers and their design parameters, gate side length a, b, and corner radius r_c for square and rectangular MOS-C, gate radius r for round MOS-C, distance d_{GR} between metal gate and guard ring metalization, width w_{GR} of the guard ring metalization, width w_{n^+} of the guard ring implant for earlier prototype designs, distance d_{ER} between guard ring metalization and edge ring implant, and minimum width w_{ER} of the edge ring implant.

	a (mm)	b (mm)	r_c (mm)	r (mm)	d_{GR} (mm)	w_{GR} (mm)	w_{n^+} (mm)	d_{ER} (mm)	w_{ER} (mm)
MOSStandard	5		0.4		0.08	0.17	0.1	0.3	0.32
MOSRound				2.5	0.02	0.1		0.3	0.45
MOSHalf	2.5		0.4		0.08	0.17	0.1	0.3	0.32
MOS2000	2.5		0.4		0.08	0.17	0.1	0.3	0.32
MOSQuarter	1.29		0.05		0.06	0.17		0.3	0.32
MOSSetProto2S	2.34	2.6	0.42						0.35
MOSSetProtoPSs	1.25		0.2		0.05	0.09	0.05	0.15	0.19
MOSHPK	4.16		0.4		0.08	0.17	0.1	0.3	0.37
MOSHMHPK	3.16		0.4		0.08	0.17	0.1	0.3	0.37
MOSRoundHPK				0.75	0.02	0.1		0.3	0.37

which negatively effects electrode isolation and, consequently, the position resolution of silicon sensors. It has to be noted that the presence of interface traps and, to a lesser degree, oxide trapped charge and mobile oxide charge affects the determination of fixed oxide charge concentration. Hence, low interface trap densities are beneficial to accurately determine the fixed oxide charge concentration [43].

Assuming a negligible role of interface trapped charges, the fixed oxide charge concentration N_{ox} can be determined from C–V sweeps on MOS-Cs. If ground potential is applied at the device backplane and the potential at the gate electrode is ramped from small negative voltages to small positive voltages[6], three characteristic regimes can be identified (Figure 6.15a) that determine the measured capacitance (Figure 6.15b).

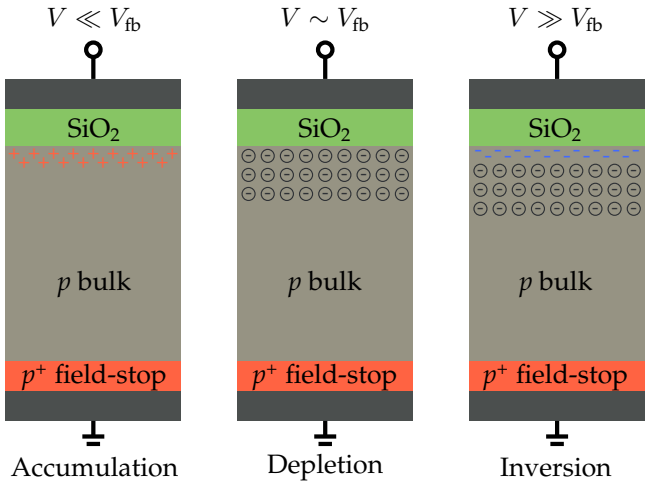
If the gate voltage is negative enough, positive majority carriers (i.e. holes) *accumulate* at the semiconductor surface and the measured capacitance is the oxide capacitance C_{ox} only. This regime, in which the capacitance remains largely constant at its maximum value, is referred to as *accumulation*. In the energy band picture, the bands bend upward near the surface in accumulation [39].

With increasing gate voltage, the band bending lessens until the intrinsic Fermi level at the surface coincides with the intrinsic Fermi level in the bulk. The configuration in which the energy bands are flat is referred to as *flatband condition*. The corresponding gate voltage is denoted as the *flatband voltage* V_{fb}. If the voltage is increased beyond V_{fb}, the energy bands bend downward and the system enters the *depletion* regime as the bulk under the gate begins to deplete. The measured capacitance in depletion is given by the oxide capacitance in series with the capacitance of the depleted silicon bulk and decreases with increasing depletion width.

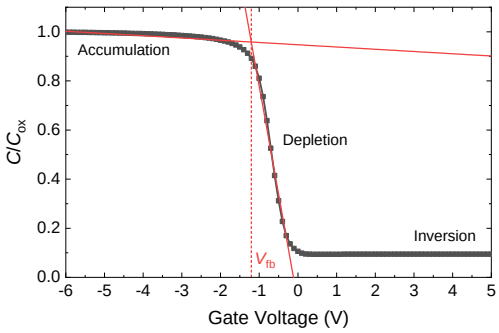
At the point at which the applied voltage becomes so high that the intrinsic Fermi level E_i at the surface bends below the constant Fermi level E_F of the semiconductor, the number of minority carriers (i.e. electrons) at the surface exceeds the number of holes, and the surface becomes *inverted*. Following the onset of inversion, which is referred to as *weak inversion*, the inversion charge at the surface increases driven by further increasing gate voltage. If the number of electrons at the surface exceeds the majority carrier density N_A of the bulk, the system reaches *strong inversion*. The inversion layer that forms at the surface effectively hinders any further extension of the space-charge region and the depletion width reaches a maximum.

The capacitance measured in inversion depends on the AC measurement frequency and the sweep rate of the DC gate voltage (Figure 6.15c). If the AC frequency is low enough that the inversion charge can follow the variation of the gate charge caused by the AC voltage

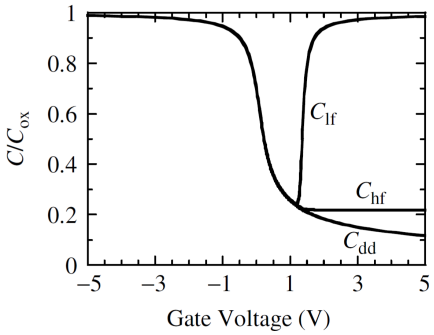
[6]This is the common sign convention in literature (e.g. [43]). Measurements presented in this thesis adopt the opposite sign because the gate electrode is kept at ground potential and high potential is applied at the device backplane.



(A) Schematic cross section of a p substrate MOS-C illustrating the charge distribution in the semiconductor during accumulation, depletion, and inversion. Figure adapted from [67].

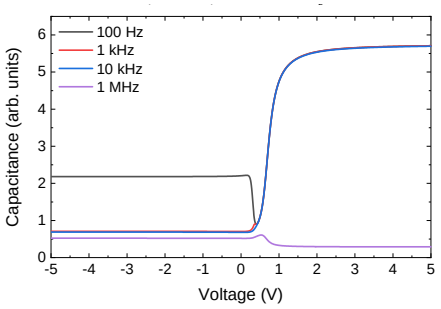


(B) Normalized high-frequency MOS-C C–V characteristics and flatband voltage determined as the intersection point of two linear fits in the accumulation and depletion regimes.

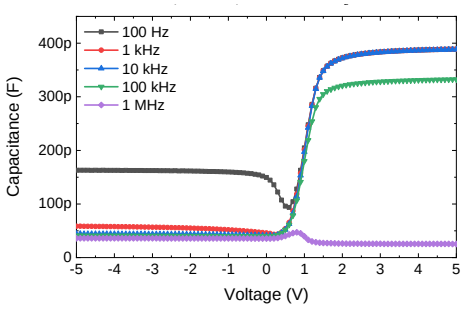


(C) Normalized low-frequency (lf), high-frequency (hf), and deep-depletion (dd) C–V characteristics of a p substrate MOS-C. Figure taken from [43].

FIGURE 6.15: Charge distribution in an MOS-C for various bias conditions (A), capacitance behavior as a function of the bias voltage for high probe frequencies and graphic extraction of the flatband voltage (B), and comparison of MOS-C capacitance characteristics for high and low probe frequencies and for the device driven into deep depletion (C).



(A) Simulated dependence of MOS-C characteristics on probe frequency. Simulation parameters: $t_a = 200\,\mu m$, $N_A = 1.9 \times 10^{12}\,cm^{-2}$, $t_{ox} = 0.6\,\mu m$, $N_{ox} = 2.5 \times 10^{10}\,cm^{-2}$.



(B) MOS-C C–V characteristics for different probe frequencies measured on a $(2.34 \times 2.6)\,mm^2$ ("MOSSetProto2S") structure on one wafer of the Infineon *VE711408* 2S prototype run.

FIGURE 6.16: Frequency dependency of MOS-C C–V characteristics. The simulation (A) qualitatively reproduces the measurements (B). For 100 Hz probe frequency, the C–V curves show low-frequency characteristics as some of the inversion layer carriers are able to follow the AC frequency. Similar behavior, albeit less pronounced, is observed for the measurement at 1 kHz. The curve at 10 kHz exhibits the typical high frequency shape of MOS-C characteristics. For higher frequencies, the series resistance of the silicon bulk and wafer backside begin to affect the capacitance measured in accumulation. A converging simulation result at 100 kHz could not be obtained and is not displayed.

variation (i.e. if charge carriers at the surface can be generated and recombined at the same rate at which the voltage varies), the *low-frequency* capacitance curve C_{lf} is measured. In this case, the capacitance increases again in inversion until in strong inversion it reaches the same maximum value as in accumulation. The *high-frequency* curve results if the inversion charge cannot follow the AC measurement frequency. Instead, the majority carriers at the edge of the space-charge region are able to follow the AC signal and constitute the necessary displacement charge. As a result, the capacitance C_{hf} in the high-frequency case remains constant at a minimum value given by the oxide capacitance in series with the capacitance of the space-charge region at maximum depletion width. Regardless of the AC measurement frequency, if the sweep rate of the DC gate voltage is so high that inversion charge cannot form during the sweep, the system is driven into *deep depletion*. In this case, the space-charge region extends beyond its maximum width and the measured capacitance C_{dd} continues to decrease with increasing gate voltage.

The rate at which the AC voltage can be varied so that low-frequency characteristics are measured is proportional to the intrinsic carrier density n_i and indirectly proportional to the generation lifetime τ_g and the oxide capacitance C_{ox} [43]. Additionally, the response time of the inversion layer can be affected by an inversion layer beyond the gate caused by positive oxide charges, surface currents because of moisture, or *p-n* junctions in the vicinity of the gate that act as minority carrier sources. Such effects may cause low-frequency behavior even at higher measurement frequencies [92].

The pronounced frequency dependency of MOS-C characteristics can be observed both in simulations (Figure 6.16a) and measurements (Figure 6.16b). While intermediate frequencies between 1 kHz and 10 kHz yield typical high-frequency characteristics, the curve at 100 Hz exhibits low-frequency characteristics for both measurement and simulation. At higher frequencies, the series resistance of the silicon bulk and wafer backside begin to affect the capacitance measured in accumulation, until, at 1 MHz, the effective capacitance measured in accumulation falls below the level of the capacitance in inversion. If not stated otherwise, the MOS-C C–V characteristics presented in this thesis were measured at an AC probe frequency of 10 kHz.

The ideal shape of MOS-C C–V characteristics is affected by the presence of oxide charges. While interface traps, generally, lead to a stretching of MOS-C curves in the

voltage direction, fixed oxide charges lead to a shift of the flatband voltage [39]. For ideal MOS-C without any oxide charges and neglecting the metal–semiconductor work function difference ϕ_{MS}, flatband condition occurs at $V = 0$. The presence of fixed oxide charges shifts the flatband voltage because, with additional charges present at the interface, the surface potential is altered compared to the ideal case. Consequently, the flatband voltage shift of an experimental MOS-C curve compared to an ideal curve can be used to determine the fixed oxide charge concentration N_{ox} using[7]

$$N_{\mathrm{ox}} = \frac{C_{\mathrm{ox}} \left(\phi_{\mathrm{MS}} - V_{\mathrm{fb}}\right)}{q A_{\mathrm{G}}} \,. \tag{6.25}$$

Here, C_{ox} denotes the oxide capacitance in accumulation, V_{fb} refers to the flatband voltage, q denotes the elementary charge, and A_{G} denotes the gate area. The metal–semiconductor work function difference $\phi_{\mathrm{MS}} = \phi_{\mathrm{M}} - \phi_{\mathrm{S}}$ is given by the work functions of the aluminum gate $\phi_{\mathrm{M}} = 4.08\,\mathrm{V}$ and the semiconductor

$$\phi_{\mathrm{S}} = \chi + \frac{E_{\mathrm{g}}}{2} + \frac{kT}{q} \ln(\frac{N_{\mathrm{A}}}{n_{\mathrm{i}}}) \tag{6.26}$$

where $\chi = 4.05\,\mathrm{eV}$ is the electron affinity of silicon and $E_{\mathrm{g}} = 1.12\,\mathrm{eV}$ is the silicon band gap.

In literature and in practice, different methods are applied to determine the flatband voltage V_{fb}. By definition, V_{fb} is the voltage corresponding to the flatband capacitance C_{fb} of the MOS-C. C_{fb} is given by the oxide capacitance C_{ox} in series with the semiconductor capacitance C_{S} in flatband condition:

$$C_{\mathrm{fb}} = \frac{C_{\mathrm{ox}} C_{\mathrm{S}}}{C_{\mathrm{ox}} + C_{\mathrm{S}}} \,. \tag{6.27}$$

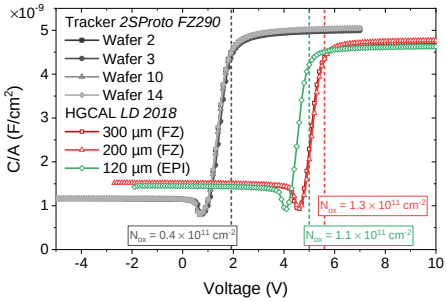
The semiconductor capacitance in flatband condition can be calculated from [43]

$$C_{\mathrm{S}} = A_{\mathrm{G}} \sqrt{\frac{q^2 \varepsilon_{\mathrm{Si}} N_{\mathrm{A}}}{kT}} \,. \tag{6.28}$$

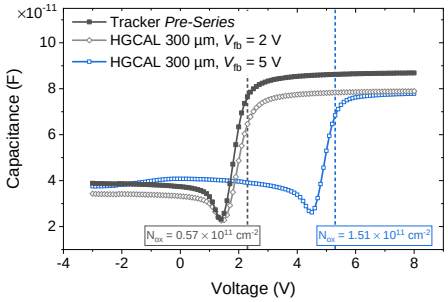
As an alternative to calculating the flatband capacitance and extracting the corresponding voltage from the measurement, the flatband voltage can also be determined from the extremum of the $\mathrm{d}^2V/\mathrm{d}(1/C_{\mathrm{hf}}^2)^2$ characteristics that occurs at flatband condition [43]. The second derivative, however, is prone to noise and may necessitate smoothing of the data. Because of these limitations, the flatband voltage may be approximated graphically. One possibility is to calculate the inflection point of the high-frequency C–V curve. Alternatively, V_{fb} can be approximated as the intersection point of two linear fits to the high-frequency curve in accumulation and depletion (Figure 6.15b). Both methods produce similar results in case of low interface trap densities, but results may differ significantly for irradiated structures. Because of simplicity and the general robustness of the linear fits, the linear fit method is used for non-irradiated MOS-Cs during CMS Outer Tracker and HGCAL PQC. Correspondingly, the linear fit method was used to extract V_{fb} for all MOS-C results presented in this thesis.

The fixed oxide charge concentration extracted from the flatband voltage of MOS-C characteristics was compared for Outer Tracker and HGCAL wafer material (Figure 6.17). Comparing the Outer Tracker 2S prototype FZ290 material (*VPX28441*) to the LD 2018 HGCAL wafer runs, N_{ox} is found to vary substantially for different wafer production processes (Figure 6.17a) [13]. While the Outer Tracker wafers consistently exhibit a fixed oxide charge concentration of $N_{\mathrm{ox}} = 4 \times 10^{10}\,\mathrm{cm}^{-2}$, N_{ox} is on average three times higher for HGCAL wafers. Furthermore, a difference between HGCAL float zone wafers and wafers subjected to an epitaxial process was observed. For the float zone process, $N_{\mathrm{ox}} = 1.3 \times 10^{11}\,\mathrm{cm}^{-2}$ was measured. The value found for epitaxial wafers ($N_{\mathrm{ox}} = 1.1 \times 10^{11}\,\mathrm{cm}^{-2}$) is about $20\,\%$ smaller. The observed difference between epitaxial and float zone wafers may be attributed to the different base materials and possible differences in the fabrication processes.

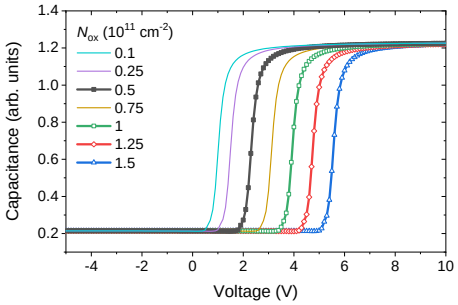
[7] Strictly speaking, the such determined charge density is only an effective density N_{eff} that also includes mobile oxide charge Q_{m} and oxide trapped charge Q_{ot} in addition to fixed oxide charge. However, because Q_{m} and Q_{ot} are usually located farther away from the Si-SiO_2 interface and the presented formula assumes that the charge is located in a sheet at the interface, the relative influence of Q_{m} and Q_{ot} is low.



(A) Tracker 2SProto FZ290 prototype run compared to HGCAL LD 2018. Characteristics were measured on MOS-C of sizes $(4.16 \times 4.16)\,\mathrm{mm}^2$ ("MOSHPK") for the Tracker material and $(2.5 \times 2.5)\,\mathrm{mm}^2$ ("MOSHalf") for HGCAL and are displayed normalized to the gate area. Figure adapted from [13].



(B) Tracker Pre-Series compared to HGCAL LD 2019. Characteristics were measured on the $(1.29 \times 1.29)\,\mathrm{mm}^2$ ("MOSQuarter") structures that are part of the "PQCFlutes" test structure set (see section 7.2).



(C) Simulated dependency of MOS-C flatband voltage on N_{ox}. Simulation parameters: $t_{\mathrm{a}} = 290\,\mu\mathrm{m}$, $N_{\mathrm{A}} = 3.8 \times 10^{12}\,\mathrm{cm}^{-2}$, $t_{\mathrm{ox}} = 0.7\,\mu\mathrm{m}$, measurement frequency $\nu = 1\,\mathrm{kHz}$.

FIGURE 6.17: Extraction of fixed oxide charge concentration N_{ox} from MOS-C C–V characteristics. N_{ox} for HGCAL wafers from the LD 2018 prototype run is about three times higher than for the Tracker 2SProto FZ290 wafers (A). The difference is attributed to the different production processes for Tracker and HGCAL wafers. For the LD 2019 run, HPK produced process splits with varying target flatband voltages. N_{ox} of the split with $V_{\mathrm{fb}} = 2\,\mathrm{V}$ compares to the results obtained on wafers of the Tracker Pre-Series run (B). The approximated N_{ox} values corresponding to the measurements are highlighted in a qualitative simulation (C).

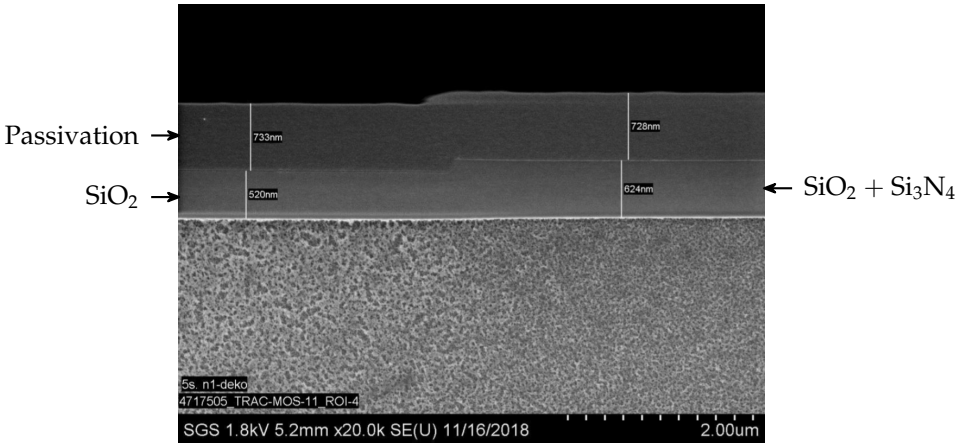


FIGURE 6.18: Electron microscopy image of an MOS-C on a wafer of the Infineon PS-s prototype run *VC811929*; close-up of the transition from a SiO_2-dielectric to a thicker dielectric layer composed of SiO_2 and Si_3N_4 that is included by the manufacturer to improve the quality of the dielectric above regions with n^+ implantations. An oxide thickness of $520\,\mathrm{nm}$ is measured. MOS-C measurements on two different positions on the same wafer yield an oxide thickness of $(539 \pm 1)\,\mathrm{nm}$.

The observed high values of N_{ox} for the HGCAL LD 2018 material were communicated to the vendor, and, in the subsequent LD 2019 run, wafers with different target flatband voltages, namely $2\,\mathrm{V}$ and $5\,\mathrm{V}$, were produced. MOS-C characteristics of the $2\,\mathrm{V}$ HGCAL material agree well with MOS-C characteristics of the Outer Tracker Pre-Series (Figure 6.17b). The fixed oxide charge concentration calculated for the Outer Tracker Pre-Series and the HGCAL LD 2019 $2\,\mathrm{V}$ material is $N_{\mathrm{ox}} = 5.2 \times 10^{10}\,\mathrm{cm}^{-2}$. For the HGCAL LD 2019 $5\,\mathrm{V}$ material, $N_{\mathrm{ox}} = 1.5 \times 10^{11}\,\mathrm{cm}^{-2}$ was found.

6.2.2 Oxide Thickness

From the oxide capacitance C_{ox} in accumulation, the oxide thickness t_{ox} can be calculated using the parallel plate capacitor formula

$$t_{\mathrm{ox}} = \varepsilon_{\mathrm{SiO_2}} \frac{A_{\mathrm{G}}}{C_{\mathrm{ox}}} \tag{6.29}$$

where $\varepsilon_{\mathrm{SiO_2}} = \varepsilon_0 \varepsilon_{\mathrm{r,SiO_2}}$ is the permittivity of SiO_2 with the relative permittivity of $\varepsilon_{\mathrm{r,SiO_2}} = 3.9$.

The accuracy of this extraction method for t_{ox} was evaluated for the Infineon *VC811929* PS-s prototype run by comparison with scanning electron microscopy[8] images (Figure 6.18). Electron microscopy of a vertical cut through an MOS-C yielded $t_{\mathrm{ox}} = 520\,\mathrm{nm}$. In comparison, the average over capacitance measurements on similar MOS-Cs on the same wafer yielded $t_{\mathrm{ox}} = (539 \pm 1)\,\mathrm{nm}$. A number of factors my contribute to the observed discrepancy of $\sim 3.5\,\%$. Firstly, electron microscopy was not performed on the same structure as the capacitance measurements, and some variation of the oxide thickness across the wafer may be possible. Additionally, errors of the gate area assumed for calculation of t_{ox} from capacitance measurements and potential effects of the MOS-C periphery may contribute. Thirdly, measurement errors and stray capacitances, as well as the series capacitance of the silicon bulk, may affect the measured capacitance. With regard to all potential error sources and measurement uncertainties, the agreement of electron microscopy and MOS-C C–V measurements within $\sim 3.5\,\%$ presents a satisfactory result. It can be concluded that high-frequency MOS-C measurements are well suited to determine the oxide thickness.

[8]The electron microscopy measurements were performed by the external provider *SGS Institut Fresenius* [93].

6.2.3 Bulk Carrier Density

The width W of the space-charge region under the gate of an MOS-C at a given gate voltage depends on the carrier density N_A of the bulk as per

$$W = \sqrt{\frac{2\varepsilon_\mathrm{Si}\phi_\mathrm{s}}{qN_\mathrm{A}}} \tag{6.30}$$

where ϕ_s is the surface potential at the given gate voltage. Hence, the maximum extension of the depletion region in strong inversion W_inv is a function of N_A (Figure 6.19):

$$W_\mathrm{inv} = \sqrt{\frac{2\varepsilon_\mathrm{Si}\phi_\mathrm{s,\,inv}}{qN_\mathrm{A}}}\,. \tag{6.31}$$

The surface potential in inversion $\phi_\mathrm{s,\,inv}$ is frequently approximated as $\phi_\mathrm{s,\,inv} \approx 2\phi_\mathrm{F}$ [43], where ϕ_F is the Fermi potential, and W_inv is given as

$$W_\mathrm{inv} = \sqrt{\frac{2\varepsilon_\mathrm{Si}2\phi_\mathrm{F}}{qN_\mathrm{A}}}\,. \tag{6.32}$$

From (6.32), follows the semiconductor capacitance in inversion $C_\mathrm{S,\,inv}$. With the measured capacitance in inversion C_inv given as the oxide capacitance C_ox in series with $C_\mathrm{S,\,inv}$ as per (6.27), the carrier density N_A can be expressed as

$$N_\mathrm{A} = \frac{4\phi_\mathrm{F}}{q\varepsilon_\mathrm{Si}A_\mathrm{G}^2}\frac{C_\mathrm{inv}^2}{(1-C_\mathrm{inv}/C_\mathrm{ox})^2}\,. \tag{6.33}$$

An analytic solution to this relationship is tedious because $\phi_\mathrm{F} = (kT/q)\ln(N_\mathrm{A}/n_\mathrm{i})$ itself is a function of N_A. An empirical relationship between C_inv and N_A for silicon at room temperature is given by [43]

$$\log(N_\mathrm{A}) = 30.38759 + 1.68278\log\left(\frac{C_\mathrm{inv}}{A_\mathrm{G}(1-C_\mathrm{inv}/C_\mathrm{ox})}\right) - 0.03177\left[\log\left(\frac{C_\mathrm{inv}}{A_\mathrm{G}(1-C_\mathrm{inv}/C_\mathrm{ox})}\right)\right]^2 \tag{6.34}$$

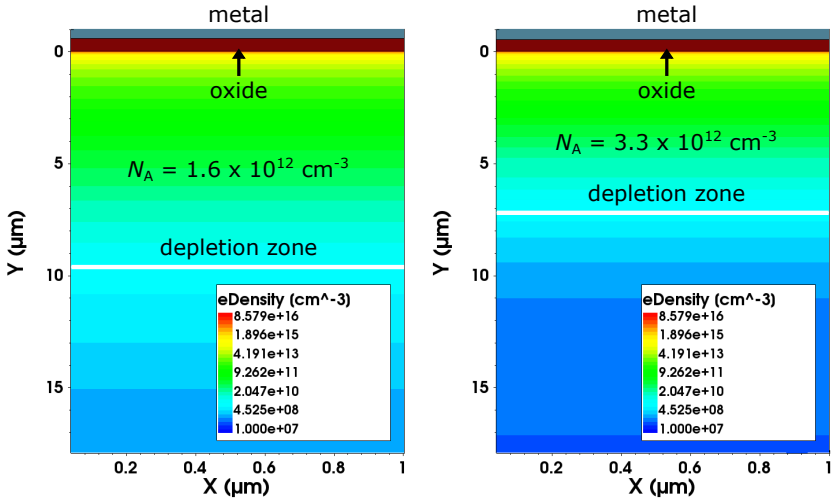
where "log" is the logarithm to base 10, capacitances are in units of F, A_G is in units of cm^2, and N_A is in units of cm^{-3}. From this relationship, N_A can be estimated by comparison of MOS-C capacitance in strong accumulation and strong inversion.

Alternatively, N_A can also be derived from the slope of MOS-C $1/C^2$ vs. V characteristics in depletion using (6.3). The sign of the slope relates to the polarity of the silicon bulk. Assuming the standard sign convention in literature (compare Figure 6.15), a positive slope indicates acceptors and a negative slope indicates donors.

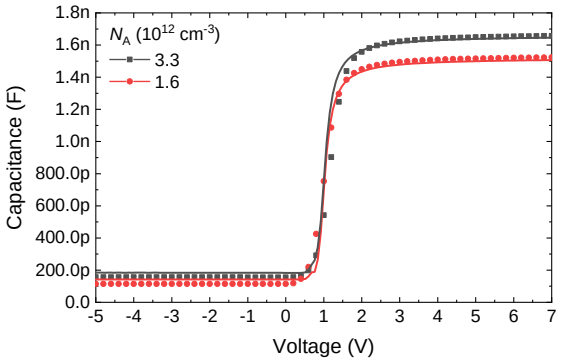
N_A was calculated from MOS-C measurements on two different wafers of the Infineon 2S prototype batches *VE543425* and *VE711408* using the empirical relationship (6.34) and the slope of $1/C^2$ vs. V characteristics in depletion (Figure 6.19b, Table 6.7). The extracted values are labeled $N_\mathrm{A,\,inv}$ and $N_\mathrm{A,\,slope}$, respectively. To evaluate the accuracy of the extraction methods, the measurement results were compared to $N_\mathrm{A,\,diode}$ as derived from the depletion voltage extracted from diode C–V measurements on the same wafers.

The values for $N_\mathrm{A,\,inv}$ are $44\,\%$ and $29\,\%$ lower than the values extracted from diode measurements for *VE543425* and *VE711408*, respectively. The large discrepancy may be attributed to inaccuracies of the empirical relationship and the above mentioned approximation of $\phi_\mathrm{s,\,inv} \approx 2\phi_\mathrm{F}$. Additionally, for bulk doping densities in the order of $1\times10^{12}\,\mathrm{cm}^{-3}$, small variations of the ratio $C_\mathrm{inv}/C_\mathrm{ox}$ translate to large differences in $N_\mathrm{A,\,inv}$ [43]. Hence, small measurement errors may have significant influence on the calculated results for the investigated high-resistivity material. With regard to these error sources, (6.34) can only be recommended to provide an estimate for the bulk doping density.

Depth-dependent features because of spatial variations of the doping density, which MOS-C measurements are not sensitive to, may constitute another reason for the observed discrepancy between $N_\mathrm{A,\,inv}$ and $N_\mathrm{A,\,diode}$. This explanation, however, loses credibility when comparing $N_\mathrm{A,\,inv}$ to $N_\mathrm{A,\,slope}$. The doping densities extracted from the slope of the $1/C^2$ vs.



(A) Electron densities and extension of the depletion zone in a MOS-C in strong inversion, simulated for doping densities $N_A = 1.6 \times 10^{12}\,\mathrm{cm}^{-3}$ (left) and $N_A = 3.3 \times 10^{12}\,\mathrm{cm}^{-3}$ (right). A cutout of the bulk area below the Si-SiO_2 junction is shown. A white line indicates the lower edge of the depletion zone.

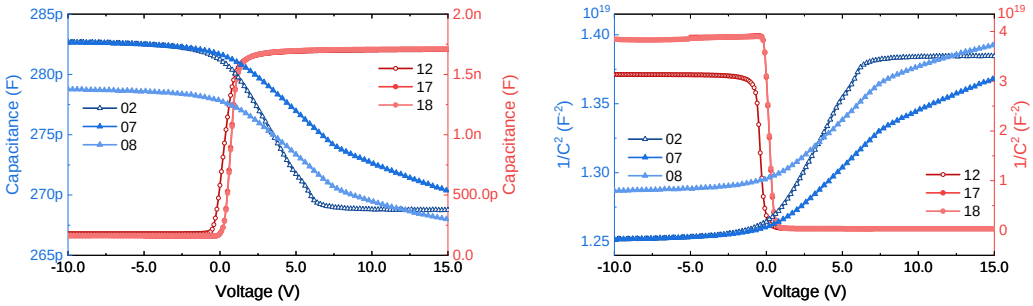


(B) MOS-C characteristics of two samples with different bulk carrier densities out of the Infineon 2S prototype batches *VE543425* and *VE711408* (dotted curves) compared to TCAD simulation for the same parameters (lines). The different absolute values of the capacitance in strong accumulation are attributed to different oxide thicknesses.

FIGURE 6.19: Influence of bulk carrier density on MOS-C characteristics. The maximum depth of the depletion zone in strong inversion extends further into the semiconductor for low carrier densities (A), which affects the ratio between capacitances in strong inversion and strong accumulation $C_{\mathrm{inv}}/C_{\mathrm{ox}}$ (B). The effect is found in measurements and simulation and can be used to determine the bulk carrier density in the MOS-C depletion region (Table 6.7). Figures adapted from [14].

TABLE 6.7: Bulk carrier density N_A extracted for two different wafers out of the Infineon 2S prototype batches *VE543425* and *VE711408*. The carrier density values used as input for the simulation $N_{A,\,sim}$ are compared to carrier densities extracted from diode C–V characteristics $N_{A,\,diode}$, the ratio of MOS-C capacitance in strong inversion and strong accumulation $N_{A,\,inv}$, and the slope of MOS-C $1/C^2$ vs. V characteristics in depletion $N_{A,\,slope}$. The values were obtained by averaging over measurements at three different positions on each wafer.

Wafer type	$N_{A,\,sim}$ $(10^{12}\mathrm{cm}^{-3})$	$N_{A,\,diode}$ $(10^{12}\mathrm{cm}^{-3})$	$N_{A,\,inv}$ $(10^{12}\mathrm{cm}^{-3})$	$N_{A,\,slope}$ $(10^{12}\mathrm{cm}^{-3})$
VE543425	1.6	1.63 ± 0.05	0.92 ± 0.03	1.55 ± 0.02
VE711408	3.3	3.29 ± 0.04	2.32 ± 0.67	3.29 ± 0.19



(A) MOS-C C–V characteristics.

(B) MOS-C $1/C^2$ vs. V characteristics.

FIGURE 6.20: MOS-C C–V (A) and $1/C^2$ vs. V (B) characteristics for wafers with different net carrier densities in the MOS-C depletion region, measured for wafers of the Infineon PS-s prototype run *VC740654*. Carrier densities and polarities vary because of different spray implantations on the wafer surface. Wafers with different doses of *n*-spray implantation (no. 07 and 08 received the same implantation dose, no. 02 received a lower dose) are compared to wafers with *p*-spray (no. 12) and without spray implantation (no. 17 and 18). The slope of MOS-C $1/C^2$ vs. V characteristics in depletion is sensitive to the carrier density of the semiconductor material along the depth of the depletion region. The polarity of the material is given by the sign of the slope. Extracted carrier densities are summarized in Table 6.8.

V characteristics in depletion agree with diode measurements within $5\,\%$ for *VE543425* and within the measurement errors for *VE711408*. It can be concluded that the method using the slope of the $1/C^2$ vs. V characteristics in depletion is better suited to extract N_A from MOS-C measurements than (6.34).

In contrast to diode C–V characteristics, MOS-C C–V characteristics are only sensitive to the bulk doping density in the depletion region right below the gate. Hence, MOS-C characteristics can be utilized to provide an estimate of the doping density of thin surface layers such as additional spray implantations. The functionality was investigated for wafers of the Infineon PS-s prototype run *VC740654* (Figure 6.20, Table 6.8). These wafers feature various spray implantations, including *p*-spray (wafer no. 12), two different doses of *n*-spray (wafer no. 02, 07, and 08), and wafers without spray implantations (wafer no. 17 and 18).

Wafers with *n*-spray are well distinguishable from those with *p*-spray and without spray implantation by the shape of the MOS-C C–V curves (Figure 6.20a). Looking at the respective $1/C^2$ vs. V characteristics (Figure 6.20b), the discrepancies are even more evident, and the wafer with *p*-spray can be well distinguished from the wafers without spray implantation. Moreover, the slopes in depletion of the *n*-spray curves indicate that wafer no. 07 and 08 received the same implantation dose while wafer no. 02 received a lower dose.

The doping densities N_A (for net *p* polarity) and N_D (for net *n* polarity) were extracted from the slope of the $1/C^2$ vs. V curves in depletion for all wafers (Table 6.8). Wafers with *n*-spray exhibit doping densities on the order of $1 \times 10^{15}\,\mathrm{cm}^{-3}$, whereby N_D of wafer no. 02 is almost $50\,\%$ lower than N_D of wafer no. 07 and 08. Similarly, wafer no. 12 exhibits an about $30\,\%$ higher doping density than wafer no. 17 and 18. The qualitative

TABLE 6.8: Bulk carrier density N_D (for net *n* polarity) or N_A (for net *p* polarity) extracted from the slope of MOS-C $1/C^2$ vs. V characteristics in depletion for six wafers with different spray implantations out of the Infineon PS-s prototype run *VC740654*. The values were obtained by averaging over at least two measurements at different positions on each wafer.

Wafer no.	Spray type	N_D, N_A (cm^{-3})
02	*n*	$(9.72 \pm 0.09) \times 10^{14}$
07	*n*	$(1.84 \pm 0.02) \times 10^{15}$
08	*n*	$(1.88 \pm 0.02) \times 10^{15}$
12	*p*	$(4.38 \pm 0.27) \times 10^{12}$
17		$(3.43 \pm 0.12) \times 10^{12}$
18		$(3.44 \pm 0.11) \times 10^{12}$

results regarding the different spray implantations agree well with the information that was disclosed by the manufacturer. However, a quantitative comparison was not possible because the corresponding doping profiles were not disclosed. Because of the depth-dependent variations of the doping profile below the gate for all wafers with spray implantations, the values for the doping density presented in Table 6.8 can only be understood as average values of the doping density within the MOS-C space-charge region.

6.3 Gate-Controlled Diode

Gate-controlled diodes (GCD) are fundamental test structures that are primarily used to access the surface generation current and disentangle it from the bulk generation current component [94]. The devices allow the extraction of both the surface generation velocity s_g, which relates to the density D_it of surface recombination-generation centers (i.e. interface traps) and is a measure of the quality of the Si-SiO_2 interface, and, albeit with layout-related limitations [95], the bulk generation lifetime τ_g.

In principle, a GCD consists of a *p*-*n* junction bordered by a gate electrode atop a non-implanted region of the silicon substrate. The diode contact is routed directly through the SiO_2 layer, while the gate electrode is separated from the bulk by the oxide layer. Thus, a GCD combines the properties of a diode and an MOS-C.

The GCDs implemented on CMS prototype and production wafers (Figure 6.21, Table 6.9) all feature the same design (Figure 6.21a). A comb-shaped gate electrode is surrounded by a complementary diode region, and an n^+ guard ring and a p^+ edge ring encircle the gate-diode structure. Another version of the design, labeled "GCDPStop" (Figure 6.21b), includes a *p*-stop implant between the diode implant and the guard ring, which allows to set the guard ring on the same potential as the diode contact during measurement and limit the influence of peripheral currents. In addition to a standard GCD with aluminum gate electrode, the Hamamatsu 2S prototype wafers include a GCD with polysilicon gate (Figure 6.21d). The final version of the test structure set for automated PQC (see section 7.2) contains two GCDs with *p*-stop, opened edge ring, and different gate width-to-pitch ratios, labeled "GCDPQC" and "GCD05".

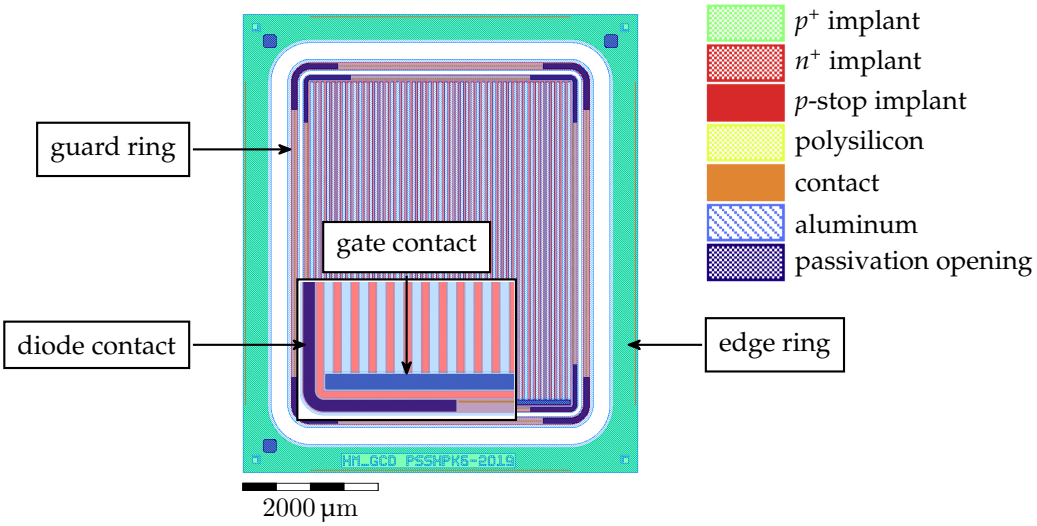
The following sections discuss the extraction of s_g and τ_g from GCD current-voltage characteristics.

6.3.1 Surface Generation Velocity

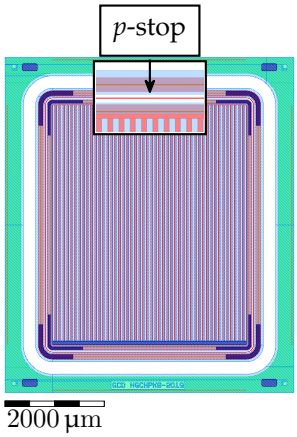
To measure GCD current-voltage (I–V) characteristics, the diode is reverse biased at a fixed voltage V_bias and the gate voltage V_gate is varied from accumulation to inversion (Figure 6.22a). The current I measured at the diode contact is composed of the leakage current of the diode space-charge region I_J, the generation current of the space-charge region beneath the gate I_g, and the surface generation component of the depleted surface under the gate I_sg:

$$I = I_\mathrm{J} + I_\mathrm{g} + I_\mathrm{sg}\,. \tag{6.35}$$

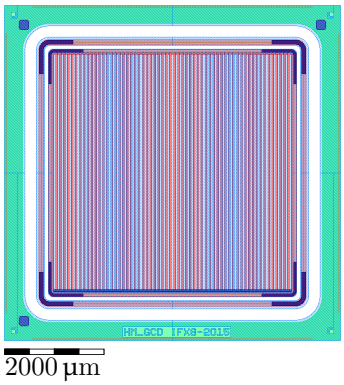
Depending on the gate voltage, the individual components contribute differently to



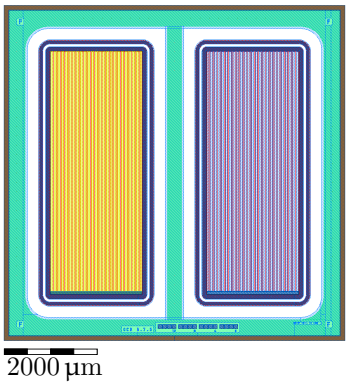
(A) "GCDStandard".



(B) GCD with p-stop implant between diode n^+ implant and guard ring ("GCDPStop").



(C) "GCDIFX2S".

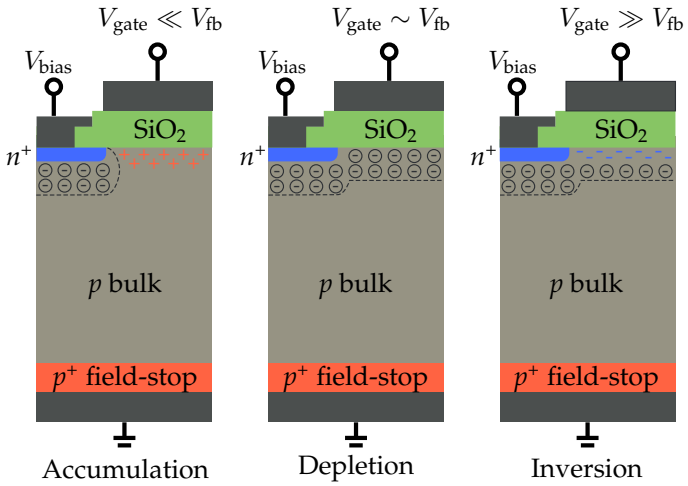


(D) GCD set with polysilicon and aluminum gates on HPK prototype wafers ("GCDHPK").

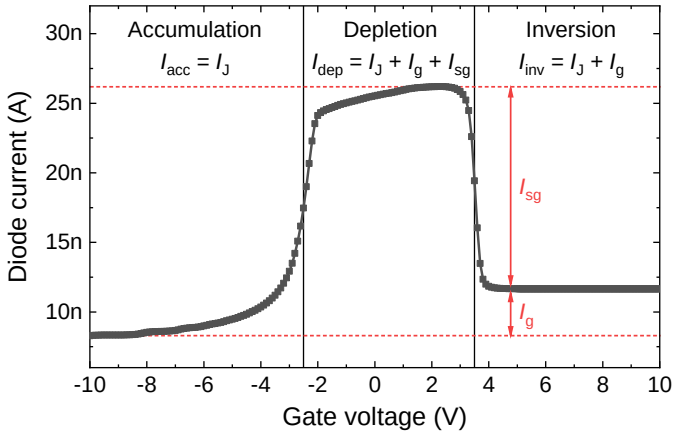
FIGURE 6.21: Types of GCD implemented on CMS prototype and production wafers. Full list in Table 6.9.

TABLE 6.9: List of GCD implemented on CMS prototype and production wafers and their design parameters, gate area A_G, diode area A_D, width of a gate finger w_G, width-to-pitch ratio w/p of the gate fingers, gate metal overhang Δw_m, width w_{ps} of the p-stop implant for GCD with p-stop between diode implant and guard ring, distance d_{GR} between diode implant and guard ring implant, width w_{GR} of the guard ring implant, distance d_{ER} between guard ring implant and edge ring implant, and width w_{ER} of the edge ring implant.

	A_G (mm^2)	A_D (mm^2)	w_G (µm)	w/p	Δw_m (µm)	w_{ps} (µm)	d_{GR} (mm)	w_{GR} (mm)	d_{ER} (mm)	w_{ER} (mm)
GCDStandard	10.9	9.6	40	0.5	5		0.09	0.1	0.35	0.37
GCDPStop	10.9	9.6	40	0.5	5	6	0.09	0.1	0.35	0.37
GCDIFX2S	13.5	11.9	40	0.5	5		0.1	0.1	0.33	0.37
GCDHPK	6.4	5.3	40	0.5	5		0.07	0.075	0.3	0.345
GCDSetProto	8.1	7.1	40	0.5	5					0.35
GCDPQC	0.5	0.8	40	0.5	5	6	0.09	0.1	0.35	0.32
GCD05	0.7	0.6	60	0.75	5	6	0.09	0.1	0.35	0.32

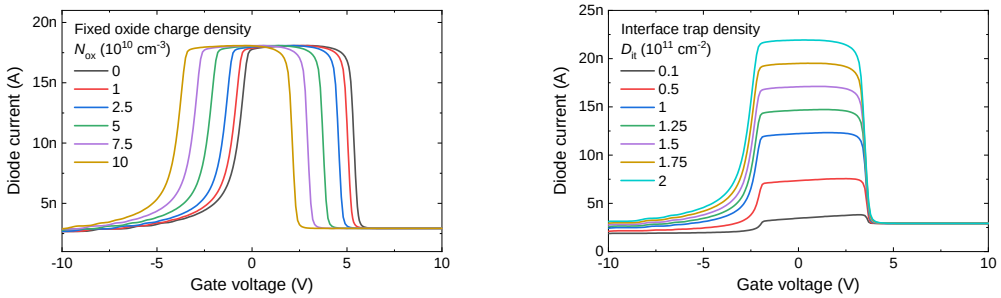


(A) Schematic cross section of a p substrate GCD illustrating the charge distribution in accumulation, depletion, and inversion regimes.



(B) Current components contributing to the I–V characteristics of an ideal GCD.

FIGURE 6.22: Charge distribution in a GCD during a gate voltage sweep (A) and ideal current-voltage characteristics (B).



(A) GCD I–V characteristics for varied N_{ox}.

(B) GCD I–V characteristics for varied D_{it}.

FIGURE 6.23: Simulated GCD characteristics for varying fixed oxide charge density N_{ox} (A) and interface trap density D_{it} (B); simulation parameters: $t_a = 290\,\mu m$, $t_{ox} = 0.7\,\mu m$, $N_A = 3.8 \times 10^{12}\,cm^{-3}$, $T = 296\,K$, $N_{ox} = 5.7 \times 10^{10}\,cm^{-2}$, $D_{it} = 1.6 \times 10^{11}\,cm^{-2}$, $\tau_{max} = 200\,\mu s$, and $A_G/A_D = 1$ (non-varied parameters are fixed to these values). Interface traps are simulated according to the Perugia surface trap model [96].

the total measured current (Figure 6.22b). In accumulation, only the leakage current of the diode space-charge region contributes, and $I_{acc} = I_J$. At flatband condition, the total current increases rapidly as the region under the gate begins to deplete, and all three current components contribute to the total current in depletion I_{dep} as in (6.35). Equivalent to MOS-C characteristics, the flatband voltage shifts depending on the density of fixed oxide charges (Figure 6.23a). Under ideal conditions, the current in depletion increases slightly with increasing gate voltage as the volume of the space-charge region under the gate increases. Finally, the inversion of the surface under the gate causes a screening of the surface states, and the measured current drops abruptly as the surface generation component no longer contributes ($I_{inv} = I_J + I_g$). The point at which inversion is reached depends on the applied bias voltage. If the gate voltage is increased further, the measured current remains largely constant as the space-charge region under the gate has reached its maximum extension. The surface generation current can then be obtained as the difference between the current in depletion and the current in inversion:

$$I_{sg} = I_{dep} - I_{inv}\,. \tag{6.36}$$

From I_{sg}, the surface generation velocity s_g is obtained as [43]

$$s_g = \frac{I_{sg}}{q n_i A_G} \tag{6.37}$$

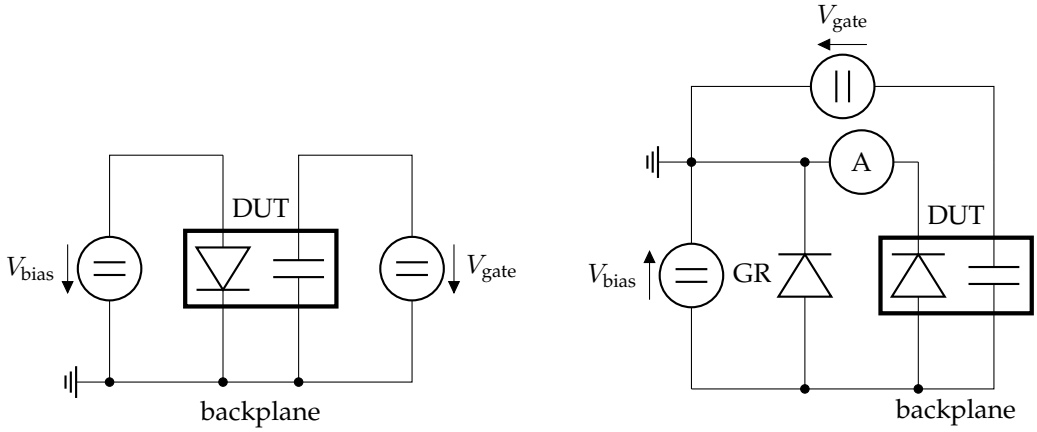
where A_G is the gate area.

The expression for s_g in (6.37) represents a generalized form of the expression derived in [94] for s_0. In their publication, Grove and Fitzgerald assume a uniform distribution of traps centered around the middle of the band gap (or, equivalently, a single-level trap at E_i) and denote s_0 as surface recombination velocity, which, in that context, can be understood synonymously with the surface generation velocity s_g. Without these restrictions on s_0 (i.e. if the trap level $E_{it} \neq E_i$), the surface recombination velocity, now denoted s_r, is generally larger than the surface generation velocity s_g [43].

If a uniform distribution of traps as in [94] is assumed, s_0 relates to the interface trap density D_{it} according to

$$s_0 = \sigma_s v_{th} \pi k T D_{it} \tag{6.38}$$

where $\sigma_s = \frac{1}{2}\sqrt{\sigma_{sn}\sigma_{sp}}$ is the effective capture cross-section of the interface trapping centers for electrons and holes, and v_{th} is the thermal velocity of the minority carriers. The underlying assumption has been shown to be justified for silicon devices with impurity concentrations above $1 \times 10^{14}\,cm^{-3}$ [97]. However, as indicated by studies such as [96], a uniform distribu-



(A) GCD measurement with floating guard ring and ground potential at the device backplane.

(B) GCD measurement with guard ring (GR) on ground potential and high potential supplied to the device backplane.

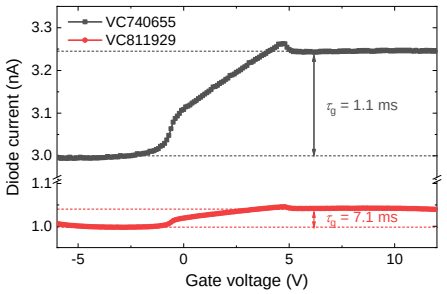
FIGURE 6.24: Schematic of GCD current-voltage (I–V) measurement. The GCD is represented by a diode and a capacitor symbolizing the gate contact.

tion of traps centered around the middle of the band gap may not be perfectly accurate for high-resistivity material with impurity concentrations $\sim 1 \times 10^{12}\,\mathrm{cm}^{-3}$ as used for the CMS Outer Tracker and HGCAL, especially after irradiation. In such cases, D_{it} cannot be reliably obtained from (6.38). However, the surface generation velocity s_{g} remains proportional to D_{it} (Figure 6.23b) and provides a measure for the quality of the Si-SiO_2 interface.

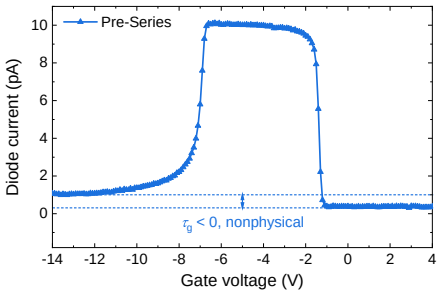
Depending on the size of the GCD, the quality of the silicon base material, carrier lifetimes, substrate doping concentration, and the interface trap density, measured currents can be quite low (i.e. $\sim 1\,\mathrm{pA}$). To accurately measure currents in that order of magnitude, it is preferable to set up the measurement such that parasitic currents originating from the device backplane and vacuum jig do not add to the measured diode current (Figure 6.24). Generally, two SMUs are needed to perform the measurement. One SMU supplies the constant bias voltage V_{bias} and measures the diode current, and a second SMU performs the gate voltage ramp. For *n*-in-*p* devices, typically, positive high potential is supplied at the front of the device under test (DUT), and the device backplane is kept on ground potential (Figure 6.24a). That way, parasitic currents at the backplane do not influence the current measurement at the front. This configuration, however, does not allow to screen against currents introduced from the device periphery, which are especially relevant for devices with opened edge ring. In order to limit the influence of peripheral currents and achieve a well-defined space-charge region, the guard ring must be set to the same potential as the diode pad (Figure 6.24b). In this case, guard ring and diode contact at the front are set to ground potential, and negative high potential is applied at the device backplane. An additional ammeter between diode contact and ground measures the diode current to avoid influence of parasitic currents from the backplane. For this configuration to work on *n*-in-*p* devices, a layer of *p*-stop is required to electrically isolate the guard ring from the diode pad.

GCD measurements presented in this thesis, in most cases, were performed using the configuration without contacted guard ring (Figure 6.24a). The configuration with connected guard ring (Figure 6.24b) was used for measurements of the GCDs with opened edge ring that are part of the test structure set for automated PQC (see section 7.2). If not stated otherwise, the bias voltage was always set to $|V_{\text{bias}}| = 5\,\mathrm{V}$.

The surface generation current I_{sg} and the surface recombination velocity s_{g} were extracted from GCD I–V measurements on three wafers of the Infineon PS-s prototype runs *VC740655* and *VC811929* and the Outer Tracker Pre-Series (Table 6.10). For the Infineon wafers, s_{g} is up to two orders of magnitude lower than for the Pre-Series material. This discrepancy is attributed to differences in the production processes, particularly with regard to the coupling dielectric and the Si-SiO_2 interface, between the two manufacturing companies. The low s_{g} values of the Infineon material indicate a considerably low concentration of



(A) GCD I–V characteristics measured on "GCDSetProto" ($A_G = 8.1\,\mathrm{mm}^2$) of the Infineon *VC740655* and *VC811929* PS-s prototype runs.



(B) GCD I–V characteristics measured on GCD05 ($A_G = 0.7\,\mathrm{mm}^2$) on an Outer Tracker Pre-Series wafer.

FIGURE 6.25: Extraction of bulk generation lifetime τ_g from GCD characteristics measured on two wafers of the Infineon *VC740655* and *VC811929* PS-s prototype runs (A) and one wafer of the Outer Tracker Pre-Series run (B). τ_g is inversely proportional to the bulk generation current beneath the gate I_g, given by the difference of currents in inversion and accumulation. As a result of the high generation lifetime of the Pre-Series material (compare section 6.1.4), the GCD measurement cannot be used to extract τ_g for these wafers because it yields nonphysical results (i.e. $\tau_g < 0$). Measurement results are summarized in Table 6.10.

interface trapping centers.

6.3.2 Bulk Generation Lifetime

The bulk generation lifetime τ_g in the space-charge region beneath the gate of a GCD relates to the generation current I_g as per [95]

$$\tau_g = \frac{q n_i A_G (W_G - W_{G0})}{I_g} \tag{6.39}$$

where

$$W_G = \sqrt{\frac{2\varepsilon_{Si}(V_{bias} + 2\phi_F)}{qN_A}} \quad \text{and} \quad W_{G0} = \sqrt{\frac{2\varepsilon_{Si} 2\phi_F}{qN_A}} \tag{6.40}$$

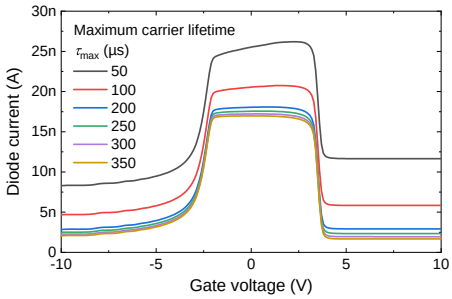
are the depletion widths of the space-charge region under the gate in strong inversion at the given reverse bias voltage V_{bias} and zero bias, respectively. The Fermi potential is given as $\phi_F = (kT/q)\ln(N_A/n_i)$, and the generation current can be obtained from GCD I–V characteristics (Figure 6.22b) as the difference between the current in inversion and the current in accumulation:

$$I_g = I_{inv} - I_{acc}\,. \tag{6.41}$$

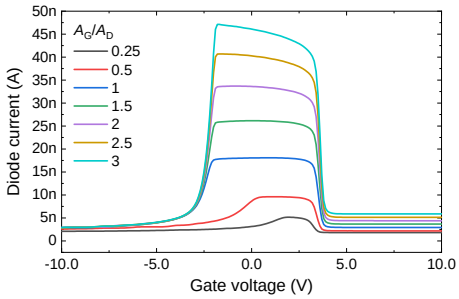
The method was applied to GCD I–V measurements on three wafers of the Infineon PS-s prototype runs *VC740655* and *VC811929* and the Outer Tracker Pre-Series (Figure 6.25, Table 6.10). The values of τ_g extracted for the Infineon material (Figure 6.25a) agree well with the values obtained from diode measurements on the same wafers (compare section 6.1.4, Table 6.5). The measurements of the Outer Tracker Pre-Series material (Figure 6.25b), in contrast, yield nonphysical results for the generation lifetime (i.e. $\tau_g < 0$) because, contradictory to what the idealized theory predicts, the current in accumulation is higher than the current in inversion. In [95], this behavior is largely attributed to unscreened interface states caused by the lateral extension of the diode space-charge region into the volume below the gate in accumulation. These interface states contribute a surface component to the current in accumulation, which is screened in inversion and, hence, results in the observed non-ideal behavior. It is shown that the importance of this effect is influenced by the absolute value of τ_g and the length of the gate relative to the length of the diode. The effect is more prevalent

TABLE 6.10: Current components I_{sg} and I_g, surface generation velocity s_g, and bulk generation lifetime τ_g extracted from GCD I–V measurements on three different wafers of the Infineon PS-s prototype batches *VC740655* and *VC811929* and the Outer Tracker Pre-Series. Values were obtained by averaging over at least two measurements at different positions on each wafer. As a result of the high generation lifetime of the Pre-Series material (compare section 6.1.4), the GCD measurement cannot be used to extract I_g and τ_g for these wafers because it yields nonphysical results (i.e. $I_g, \tau_g < 0$).

Wafer type	A_G (mm^2)	N_A (10^{12}cm^{-3})	I_{sg} (pA)	s_g (cm/s)	I_g (pA)	τ_g (ms)
VC740655	8.1	3.2	16 ± 3	0.18 ± 0.03	256 ± 23	1.1 ± 0.2
VC811929	8.1	3.5	3 ± 1	0.04 ± 0.01	43 ± 1	7.1 ± 0.1
Pre-Series	0.7	3.8	10 ± 1	1.19 ± 0.02		



(A) GCD I–V characteristics for varied τ_{max}.



(B) GCD I–V characteristics for varied A_G/A_D.

FIGURE 6.26: Simulated GCD characteristics for varying maximum carrier lifetime τ_{max} (A), and ratio of gate and diode area A_G/A_D (B); simulation parameters: $t_a = 290\,\mu m$, $t_{ox} = 0.7\,\mu m$, $N_A = 3.8 \times 10^{12}\,cm^{-3}$, $T = 296\,K$, $D_{it} = 1.6 \times 10^{11}\,cm^{-2}$, $N_{ox} = 5.7 \times 10^{10}\,cm^{-2}$, $\tau_{max} = 200\,\mu s$, and $A_G/A_D = 1$ (non-varied parameters are fixed to these values). Interface traps are simulated according to the Perugia surface trap model [96].

for both higher lifetime values and shorter gates [95].

2D TCAD simulations were performed to visualize the effect of the minority carrier lifetimes and the ratio of gate and diode area on GCD I–V characteristics (Figure 6.26). In the simulation, the GCD was represented by a single $20\,\mu m$ wide diode next to a single gate electrode with a metal overhang of $5\,\mu m$. For the diode n^+ implant, a doping concentration of $1 \times 10^{19}\,cm^{-3}$ and an implantation depth of $1\,\mu m$ were assumed. The carrier lifetime was varied using the parameter τ_{max}, which can be specified for both electrons and holes in the parameter set `Scharfetter` if the model `SRH(DopingDependence)` is specified with the `Recombination` keyword. The parameter was set equal for electrons and holes and can be assumed as half of the generation lifetime τ_g [95]. The ratio of gate and diode area A_G/A_D was varied by varying the gate length while the diode length was kept constant at $20\,\mu m$.

Clearly, the inversion current becomes lower with respect to the current in accumulation for higher values of τ_{max}, corresponding to higher values of τ_g (Figure 6.26a). Similarly, lower values of A_G/A_D, which correspond to lower gate lengths, are found to result in lower inversion currents with respect to the current in accumulation (Figure 6.26b). Both simulations qualitatively reproduce the behavior observed in measurements and stress the fact that, in order to extract high generation lifetimes with accuracy, a high A_G/A_D ratio is beneficial. This requirement, however, is contradictory to the accurate extraction of s_g, which favors short gate lengths [95]. In order to extract both parameters with sufficient accuracy, two GCD designs with different gate lengths are beneficial.

6.4 Van-der-Pauw Structure

Van-der-Pauw structures – named after L. J. van der Pauw – are basic test structures used to determine the sheet resistance of thin films such as ion implantation layers, metal sheets, or polysilicon films. If the thickness of the sheet is known, the resistivity and, consequently, the average doping density of implantation layers can be determined from van-der-Pauw measurements.

CMS prototype and production wafers include a large variety of different van-der-Pauw structures (Figure 6.27) for different implantation types and sensor layers. Structures exist for the p^+ (edge) layer, n^+ layer, p-stop implant, polysilicon layer, and the aluminum metalization. With regard to the available space on the wafer and the intended purpose of the structure, different shapes are implemented. Dimensions and shapes vary for the different wafer layouts (compare section 4.2).

The most basic form of a van-der-Pauw structure is shaped like a Greek cross (Figure 6.27b) with a contact at the end of each of the four arms. This structure allows to directly measure the sheet resistance via a four-terminal resistance measurement. A version of the cross, designated as "cross-bridge", that is elongated on one side and features six contacts (Figure 6.27a) allows to measure the sheet resistance and the line width. On the CMS Outer Tracker production wafers and newer HGCAL designs, individual bridge type structures without the characteristic van-der-Pauw crosses (Figure 6.27c and 6.27d) are implemented. These structures are designated as "line width structures" and are intended to be used in conjunction with sheet resistance measurements on van-der-Pauw crosses to determine the line width of the corresponding sensor layer. They were introduced as a space-saving alternative to cross-bridge structures to optimize the allocation of contacts within the flute arrays for automated PQC. In addition to standard cross structures, cloverleaf structures of the metal layer (Figure 6.27e) are implemented. For the aluminum sheet resistance, particularly low values $\sim 30\,\mathrm{m\Omega/sq}$ are expected, and the cloverleaf structures are included to minimize the measurement error introduced by non-ideal contacts [43]. Infineon and Hamamatsu prototype wafers for the Outer Tracker include van-der-Pauw cross (Figure 6.27f) and cross-bridge (Figure 6.27g) structures that are encircled with implants of different polarity than the layer under test (i.e. n^+ implant surrounding p-stop van-der-Pauw and vice versa). These design variations were included for R&D purposes to provide isolation from the surroundings and test the influence of the layout on the measurement result.

The following sections discuss the principles of sheet resistance and line width measurements and compare the parameters extracted for different wafer runs.

6.4.1 Sheet Resistance of Thin Films

Sheet resistance is a concept that is commonly used to characterize the resistance of thin layers [43]. The sheet resistance R_{sh} relates to the resistivity ρ of the layer via the layer thickness t according to

$$R_{\mathrm{sh}} = \frac{\rho}{t}\,. \tag{6.42}$$

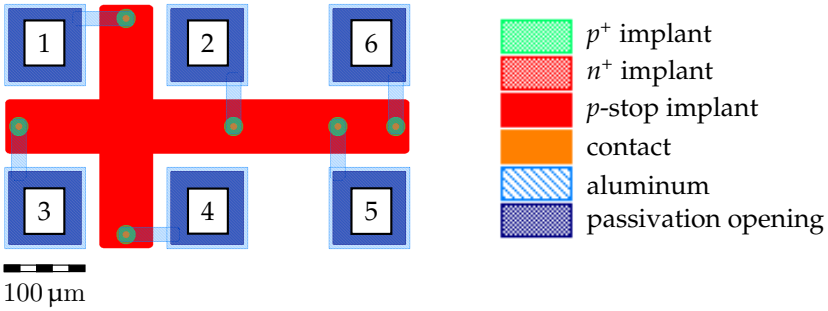
R_{sh} is expressed in units of ohms per square (Ω/sq). A square refers to the ratio of the layer length L to the layer width W (i.e. L/W). The resistance R of a sample is then given by the sample sheet resistance multiplied by the number of squares:

$$R = R_{\mathrm{sh}}\frac{L}{W}\,. \tag{6.43}$$

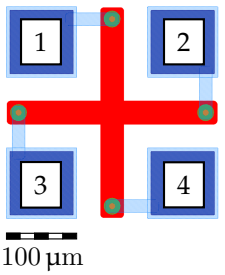
In 1958, L. J. van der Pauw proposed a method to determine the specific resistivity of arbitrarily shaped flat samples without having to know the current pattern in the sample [98]. Based on the proposed method, the resistivity of a symmetrical structure such as the cross resistor in Figure 6.27b is

$$\rho = \frac{\pi}{\ln(2)}t\frac{V_{34}}{I_{12}} \tag{6.44}$$

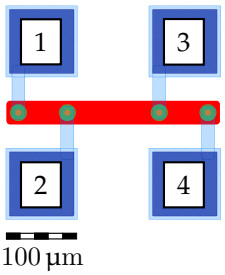
where the current I_{12} flows from contact 1 to contact 2 and V_{34} is the voltage between contacts



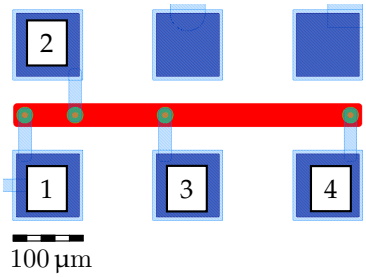
(A) Standard van-der-Pauw cross-bridge structure for sheet resistance and line width measurement of the p-stop layer.



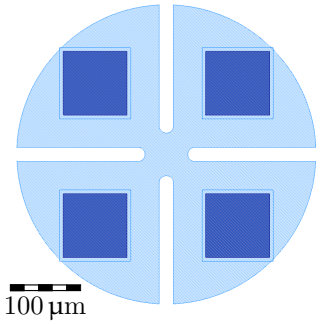
(B) Standard van-der-Pauw cross.



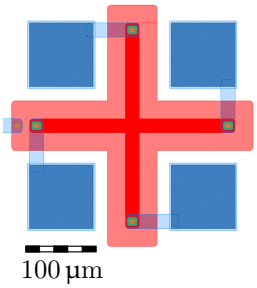
(C) Symmetric bridge type line width structure.



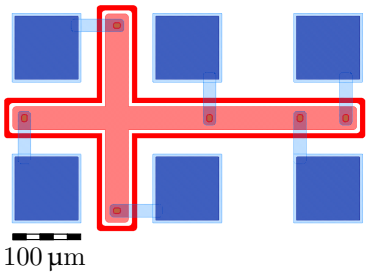
(D) Asymmetric bridge type line width structure.



(E) Cloverleaf van-der-Pauw for the aluminum layer.



(F) P-stop van-der-Pauw cross with surrounding n^+ implant.



(G) N^+ van-der-Pauw cross-bridge with surrounding p-stop implant.

FIGURE 6.27: Types of van-der-Pauw structures implemented on CMS prototype and production wafers. General overview. Numerous variants for different layers and with different line widths exist. Contact numbering is equivalent to (A) for all cross-bridge type structures, equivalent to (B) for all cross type structures, and equivalent to (C) and (D) for all bridge type structures.

TABLE 6.11: Sheet resistance of different thin layers measured on van-der-Pauw cross and cross-bridge structures on four wafers of the Infineon PS-s prototype run *VC811929*, one wafer of the Hamamatsu 2S prototype run *VPX28442*, and three 200 µm thick wafers of the LD 2018 HGCAL prototype run. Values are obtained by averaging over multiple measurements of structures at at least two different locations on all wafers of each run.

	n^+ implant R_{sh} (Ω/sq)	p^+ implant R_{sh} (kΩ/sq)	p-stop R_{sh} (kΩ/sq)	polysilicon R_{sh} (kΩ/sq)	metal R_{sh} (mΩ/sq)
VC811929	58.8 ± 1.1	0.77 ± 0.01	22.2 ± 0.6	3.56 ± 0.04	15.9 ± 0.4
VPX28442	35.5 ± 1.1		24.7 ± 2.5	2.28 ± 0.19	
LD 2018	38.2 ± 1.5	1.41 ± 0.03	26.2 ± 0.6		24.2 ± 0.5

TABLE 6.12: Doping density N_{A} (p polarity) and N_{D} (n polarity) calculated from van-der-Pauw sheet resistance measurements (Table 6.12). The sheet thickness t was estimated from SRP measurements of standard Infineon and Hamamatsu prototype wafers (see section 6.13.1). Values represent the average doping density across the given layer thickness.

	n^+ implant		p^+ implant		p-stop	
	t (µm)	N_{D} ($10^{18}\,\mathrm{cm}^{-3}$)	t (µm)	N_{A} ($10^{16}\,\mathrm{cm}^{-3}$)	t (µm)	N_{A} ($10^{15}\,\mathrm{cm}^{-3}$)
VC811929	3	2.09 ± 0.04	3	7.02 ± 0.06	2	2.98 ± 0.08
VPX28442	2	7.91 ± 0.24			1	5.39 ± 0.55
LD 2018	2	7.21 ± 0.28	1.6	7.02 ± 0.14	1	5.07 ± 0.11

3 and 4. Consequently, the sheet resistance becomes

$$R_{\mathrm{sh}} = \frac{\rho}{t} = \frac{\pi}{\ln(2)} \frac{V_{34}}{I_{12}} \,. \tag{6.45}$$

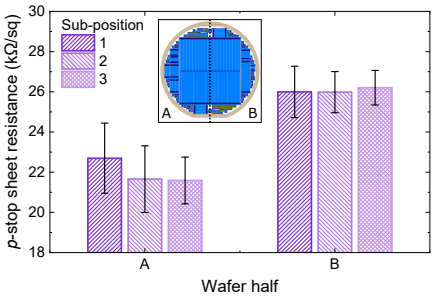
Because only the sheet resistance of the central square is measured, the cross configuration is largely independent of the actual dimensions of the cross. However, it has to be noted that surface leakage can affect the measurement if the length of the arms is too large [43]. To cancel errors that may be introduced by imperfect contacts, it is possible to perform the resistance measurement in a rotated configuration (e.g. V_{13}/I_{24}) in addition to the standard configuration of (6.45) and calculate the average between the two measurements.

If the layer thickness t is known, the resistivity ρ can be calculated from (6.44) and the doping density can be obtained using (3.6).

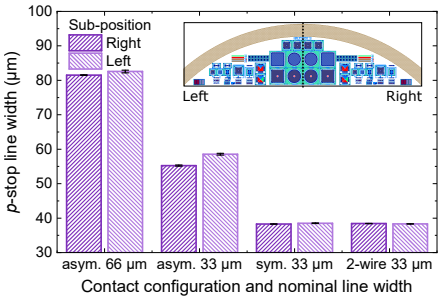
The sheet resistance of different layers was measured on wafers of the Infineon PS-s prototype run *VC811929*, the Hamamatsu 2S prototype run *VPX28442*, and the Hamamatsu LD 2018 HGCAL prototype run (Table 6.11), and the respective doping densities were calculated for n^+, p^+, and p-stop implant layers (Table 6.12). The respective sheet thicknesses were estimated from Spreading Resistance Profiling (SRP) measurements of sample wafers from each manufacturer (see section 6.13.1). Because the Hamamatsu 2S prototype design does not include p^+ and metalization van-der-Pauw structures, the sheet resistance of these layers could not be measured on the wafers of the *VPX28442* run. Furthermore, because of the DC-coupled process, the HGCAL wafers do not contain a polysilicon layer.

Generally, sheet resistance values of each respective layer are similar for both investigated Hamamatsu batches, while the values of the Infineon batch deviate compared to the Hamamatsu runs. However, in case of the p^+ implant, the observed differences can be entirely attributed to the different implantation depths, whereas the calculated doping density is notably similar. Note that the doping density varies many orders of magnitude along the estimated sheet thickness, and the quoted values of N_{D} and N_{A} constitute the average doping density along the given depth. Sheet resistance measurements, naturally, cannot provide information on the doping profile.

Another notable feature of the presented results is the considerable variation of the p-stop sheet resistance for *VPX28442* wafers. The value quoted in Table 6.11 is the average over multiple measurements of different structures at different positions across the wafer area. When looking at the values measured at each individual test structure, a distinct dependence



(A) Sheet resistance of the *p*-stop implant measured on van-der-Pauw cross-bridge structures at three sub-positions on both halves of a wafer of the 2S prototype run *VPX28442* (illustrated in the insert). Half A exhibits lower sheet resistance values than half B. Consistent behavior is found for all wafers of the batch, indicating that the location dependency of the sheet resistance is an attribute of the production process [13].



(B) *P*-stop line width measured on both halves of a "halfmoon" cutoff (see insert) of the Outer Tracker Pre-Series run. The cross-bridge and bridge structures with asymmetric contact placement (Figure 6.27a and 6.27d) systematically overestimate the nominal line width. Bridge structures with symmetric contacts (Figure 6.27c) yield results close to the nominal value. If structures are measured with a 2-wire configuration instead of the standard 4-wire configuration, results close to the nominal value are obtained. Results are consistent for all wafers of the batch.

FIGURE 6.28: Location and contact symmetry dependent variations of *p*-stop van-der-Pauw measurement results. Wafers of the 2S prototype run *VPX28442* exhibit different sheet resistance values depending on the location of the measured structure on the wafer (A). Cross-bridge and line width structures of the Outer Tracker Pre-Series run yield different line width results for asymmetric and symmetric placement of the four contacts (B).

on the location of the test structure on the wafer can be observed (Figure 6.28a). If the wafer is divided along the axis parallel to the strips of the main sensor into halves A and B, half A exhibits lower sheet resistance values than half B (i.e. $R_{\mathrm{sh}} \approx 22\,\mathrm{k\Omega/sq}$ and $R_{\mathrm{sh}} \approx 26\,\mathrm{k\Omega/sq}$, respectively). Consistent behavior is found for all wafers of the batch. These results indicate that production process specifics cause a dispersion of the *p*-stop sheet resistance across the wafer area. A similar dispersion was not observed for n^+ and polysilicon sheet resistances. Compared to *p*-stop sheet resistance, the sheet resistance of these layers is low, and, hence, variations are difficult to detect with sufficient accuracy [13].

6.4.2 Line Width

The line width of an implant or layer refers to the smaller of the two lateral dimensions. To distinguish the parameter from the depletion width W, it is denoted w in the following.

Cross-bridge structures as in Figure 6.27a are used to electrically determine the line width of a given layer [43]. The sheet resistance of the structure can be determined from the cross resistor (i.e. contacts 1–4) using (6.45). Making the key assumption that the sheet resistance is the same across the whole cross-bridge structure, the line width is determined from the bridge resistor as

$$w = \frac{R_{\mathrm{sh}} d_{25}}{V_{25}/I_{36}} \tag{6.46}$$

where d_{25} is the distance between contacts 2 and 5, the current I_{36} flows between contacts 3 and 6, and the voltage V_{25} between contacts 2 and 5 is measured.

In case of the stand-alone line width structures of Figure 6.27c and 6.27d, the current flows between contacts 1 and 4 and the voltage is measured between contacts 2 and 3. Hence, the line width is determined as

$$w = \frac{R_{\mathrm{sh}} d_{23}}{V_{23}/I_{14}} \tag{6.47}$$

TABLE 6.13: Line width of different thin layers extracted from van-der-Pauw cross-bridge structures on four wafers of the Infineon PS-s prototype run *VC811929* and one wafer of the Hamamatsu 2S prototype run *VPX28442*. Nominal design values of the *VC811929* run are $33\,\mu\mathrm{m}$ for the n^+, p^+, and *p*-stop implant, and polysilicon layer and $20\,\mu\mathrm{m}$ for the metalization layer. For *VPX28442*, the nominal value is $40\,\mu\mathrm{m}$ for all measured layers.

	n^+ implant w (µm)	p^+ implant w (µm)	*p*-stop w (µm)	polysilicon w (µm)	metal w (µm)
VC811929	33.2 ± 0.7	33.8 ± 0.3	51.7 ± 1.8	39.8 ± 0.6	22.7 ± 0.8
VPX28442	43.2 ± 0.3		37.6 ± 0.7	42.3 ± 7.2	

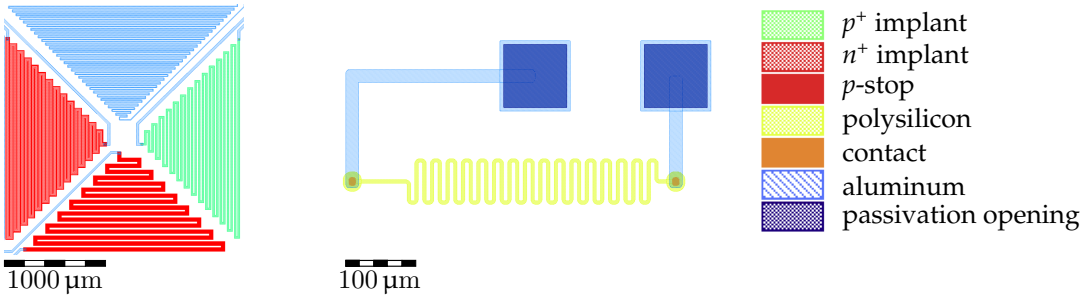
where R_{sh} must be determined from another structure (e.g. a van-der-Pauw cross) and it is assumed that the sheet resistance of the line width structure is the same.

The line width of different layers was measured on wafers of the Infineon PS-s prototype run *VC811929* and the Hamamatsu 2S prototype run *VPX28442* (Table 6.13). According to the layout design, n^+, p^+, *p*-stop, and polysilicon structures on the *VC811929* wafers have a nominal line width of $33\,\mu\mathrm{m}$, the metalization layer has a nominal line width of $20\,\mu\mathrm{m}$, and all measured structures of the *VPX28442* run have a nominal line width of $40\,\mu\mathrm{m}$. The measured values are reasonably close to the nominal values for almost all layers on both wafer runs – n^+ and p^+ values of the *VC811929* batch being particularly accurate. The line width of the *p*-stop layer on *VC811929* wafers, however, is a notable exception. In this case, the measured $w \approx 52\,\mu\mathrm{m}$ deviates from the nominal line width by about $58\,\%$.

Similar deviations of the measured *p*-stop line width from the nominal value of the layout design were observed on wafers of the Outer Tracker Pre-Series run (Figure 6.28b). Optical checks under a microscope could not reproduce the measured discrepancies and, instead, found line widths close to the design values.

The influence of the nominal line width and the contact configuration on the measured line width values was investigated on van-der-Pauw cross-bridge (Figure 6.27a) and bridge type line width structures (Figure 6.27c and 6.27d) with different nominal line widths. The line width extracted from a four-terminal resistance measurement using contacts 3, 2, 5, and 6 on a nominally $66\,\mu\mathrm{m}$ wide *p*-stop cross-bridge structure is about $24\,\%$ higher than the nominal value. Four-terminal measurements using contacts 1–4 on the elongated line width structure (Figure 6.27d) with nominal line width $33\,\mu\mathrm{m}$, on the other hand, yielded a discrepancy between measured and nominal value of almost $72\,\%$. In both cases, the direction in which the current flowed through the structure had no influence on the result. For both of these structures, the contacts to the *p*-stop layer are not spaced symmetrically with respect to a common central axis. In particular, the distance between the outer contacts and the closest inner contact is $265\,\mu\mathrm{m}$ on one side and $71.5\,\mu\mathrm{m}$ on the other. The line width extracted from four-terminal measurements on the shorter line width structure with symmetric contact placement (Figure 6.27c), however, deviates from the nominal value of $33\,\mu\mathrm{m}$ only by about $16\,\%$. If the line width is extracted from a two-terminal resistance measurement instead of the typical four-terminal measurement (e.g. measuring V_{23}/I_{23}), the obtained value is close to the nominal value in all cases. Consistent results were found across different wafers of the same batch and independently at different PQC test centers. These results strongly suggest that an asymmetric placement of the four contacts affects the resistance measurement in a way that causes a significant systematic overestimation of the such extracted line width. Further, this effect is stronger for structures with smaller nominal line width.

The reason for this dependence of the extracted line width on contact placement, independently observed by different experiments and on wafers of different manufacturers, is not understood. However, it is likely that a number of different effects contribute. Firstly, the *p*-stop van-der-Pauw structures include under the contacts small regions of high density p^+ doping that were introduced to provide an ohmic contact between metal and semiconductor (i.e. avoiding Schottky type contacts). The influence of these implants on the electric field distribution and on the accuracy of the van-der-Pauw method, which has as a key assumption the uniformity of the sample resistivity, will need to be investigated. Secondly, it has to be noted that on wafers of batch *VPX28442* a notable influence of the contact asymmetry is not observed (Table 6.13). In contrast to the van-der-Pauw structures of the other investigated



(A) Metal, n^+, p^+, and p-stop meander.

(B) Polysilicon meander modeled on polysilicon bias resistors for AC-coupled strip sensors.

FIGURE 6.29: Types of meander test structures implemented on CMS prototype and production wafers.

wafer batches, structures of batch *VPX28442* are surrounded by an additional n^+ implant similar to Figure 6.27f. Further, p^+ implants under the contacts are smaller than for the structures on the other investigated batches. Finally, it has to be taken into account that compared to all other layers accessible with van-der-Pauw resistance measurements, the nominal sheet resistance of the p-stop layer is considerably high. Consequently, effects that may not be possible to resolve on other structures may manifest more strongly on structures probing the p-stop layer.

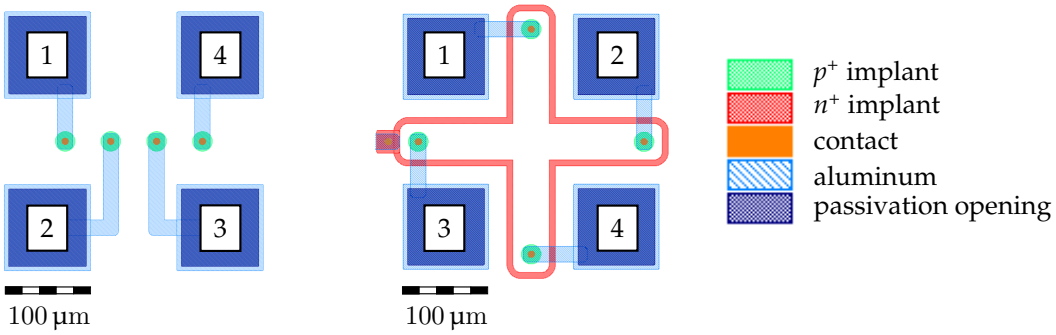
6.5 Meander

Complementary to van-der-Pauw structures, CMS prototype and production wafers include meander-shaped structures (Figure 6.29) to determine the sheet resistance of different sensor layers. The meanders are designed with a large length-to-width ratio (i.e. a large number of squares). By measuring the resistance of a meander and dividing the result by the number of squares, the sheet resistance can be determined. Particularly, for layers with low resistivity such as the aluminum metalization, it is easier to measure the comparably large resistance of meanders than to accurately determine the sheet resistance from van-der-Pauw type measurements. If both van-der-Pauw and meander measurements can be performed accurately, comparing the determined sheet resistances allows to detect deviations of the meander line width from the target line width, caused by, e.g., over etching or lateral diffusion of dopant ions during wafer processing. When determining the number of squares from the length-to-width ratio of a meander, corner squares must be counted as 0.56 [67].

Most prototype and production wafers include metal, n^+, p^+, and p-stop meanders that are arranged in square shapes (Figure 6.29a) as part of early prototypes of test structure sets for PQC (see section 7.1). For all types of implant meanders, versions with and without surrounding n^+ or p-stop implants are implemented. A notable exception are Hamamatsu 2S prototype wafers, which include n^+, p-stop, and metal meanders with different line widths but no p^+ meanders. All p-stop and n^+ meanders on Hamamatsu 2S prototype wafers are surrounded by isolating implants of n^+ and p-stop, respectively. Outer Tracker production wafers additionally include polysilicon meanders modeled on polysilicon bias resistors for AC-coupled strip sensors (compare section 4.1.1). Further, Infineon 2S prototype wafers include a set of polysilicon meanders with different lengths and line widths.

6.6 Four-Terminal Resistivity Test Structure

Four-point probe techniques are a common industry standard to determine the wafer resistivity [43]. To provide an alternative to C–V measurements on diodes, CMS prototype and production wafers include test structures designed to allow a four-terminal resistivity measurement of the silicon bulk. With regard to the probe placement, two different designs



(A) Standard four-terminal resistivity test structure

(B) Four-terminal resistivity test structure with contacts in van-der-Pauw configuration and surrounding n^+ implant.

FIGURE 6.30: Types of four-terminal test structures for measuring bulk resistivity implemented on CMS prototype and production wafers.

are implemented (Figure 6.30). The first design is composed of four equally spaced contacts to the silicon bulk that are routed to probe needle landing pads (Figure 6.30a). The contact spacing varies slightly for different wafer designs. On Outer Tracker production wafers and HGCAL LD 2019 wafers, spacings of $53\,\mu m$, $133\,\mu m$, and $600\,\mu m$ are implemented. The second design version applies a van-der-Pauw type contact placement with contacts positioned at the four corner points of a square. For Outer Tracker production wafers and HGCAL LD 2019 wafers, the square side length is $187\,\mu m$. To facilitate biasing, some of the van-der-Pauw type structures include a thin n^+ implant surrounding the contacts in a Greek cross shape (Figure 6.30b). The standard implementation of both design versions includes p^+ implants under the contact holes to improve the ohmic contact to the bulk. In addition to these standard versions, Outer Tracker production wafers and HGCAL LD 2019 wafers include four-terminal test structures in the aligned design without p^+ implants under the contacts.

For four in-line probes with equal probe spacing s as in Figure 6.30a, the resistivity ρ is given by

$$\rho = 2\pi s F \frac{V_{23}}{I_{14}} \tag{6.48}$$

where I_{14} is the current flowing between contacts 1 and 4, and V_{23} is the voltage measured between contacts 2 and 3. F denotes a product of correction factors that account for finite sample geometries, including probe location near sample edges, sample thickness, sample diameter, probe placement, and sample temperature [43]. Correction factors for probe placement relative to the sample edges and for lateral sample dimensions can be neglected for large samples. Sample thickness, however, must be corrected since, in many cases, the thickness is on the order of the probe spacing. For a conducting bottom wafer surface, the correction factor is given as [43]

$$F = \frac{t/s}{2\ln\{[\cosh(t/s)]/[\cosh(t/2s)]\}} \tag{6.49}$$

where t denotes the sample thickness. For a wafer thickness of $t = 300\,\mu m$ and probe spacings $s = 53\,\mu m$, $s = 133\,\mu m$, and $s = 600\,\mu m$ the correction factors are $F = 1.0012$, $F = 1.0854$, and $F = 2.8032$, respectively. It has to be noted that for samples thicker than the probe spacing, the individual correction factors contained in F are no longer independent because of interactions between sample thickness and edge effects [43] and (6.48) can only provide an estimate of the bulk resistivity[9].

[9] Industry four-terminal probe techniques usually use wider probe spacing and calculate well defined correction factors to accurately determine the sample resistivity.

For resistivity measurements in the van-der-Pauw configuration of Figure 6.30b, the probe placement must be taken into account. The voltage V at a distance r from a probe inducing the current I is given by [43]

$$V = \frac{I\rho}{2\pi r}\,. \tag{6.50}$$

Hence, if current enters the sample through contact 1 and leaves through contact 2, the voltage at contact 3 and the voltage at contact 4 become

$$V_3 = \frac{I\rho}{2\pi}\left(\frac{1}{s} - \frac{1}{\sqrt{2}s}\right) \quad \text{and} \quad V_4 = \frac{I\rho}{2\pi}\left(\frac{1}{\sqrt{2}s} - \frac{1}{s}\right), \tag{6.51}$$

respectively. Here, s denotes the side length of the square with a contact at each corner, and the minus sign accounts for the current leaving through contact 2. The voltage measured between contacts 3 and 4 is

$$V_3 - V_4 = \frac{I\rho}{2\pi}\left(\frac{2-\sqrt{2}}{s}\right), \tag{6.52}$$

and the resistivity is given as

$$\rho = \frac{2\pi s F}{2-\sqrt{2}}\frac{V_{34}}{I_{12}}\,. \tag{6.53}$$

For a wafer thickness of $t = 300\,\mu\mathrm{m}$ and probe spacing $s = 187\,\mu\mathrm{m}$, the correction factor in (6.49) becomes $F = 1.218$.

6.7 Metal-Oxide-Semiconductor Field-Effect Transistor

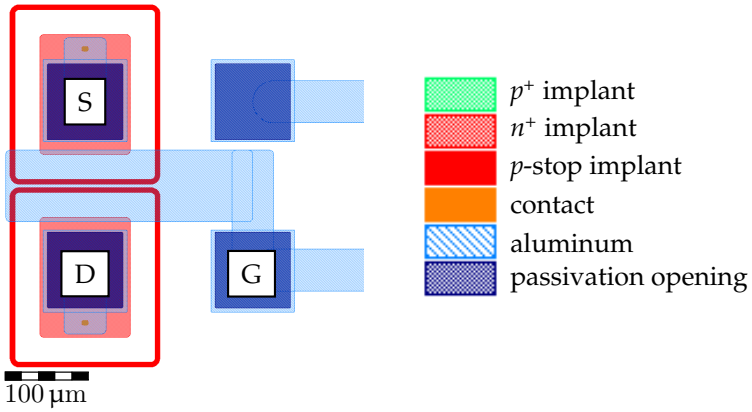
The Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is well established as the most important device in semiconductor electronics. Its low power consumption, high production yield, and ability to be readily scaled down continue to drive the development of complex integrated circuits of increasingly small size and improving performance. The application of MOSFET test structures for particle physics detector development and process quality control, however, is a comparatively new advancement [67, 99].

MOSFET test structures are implemented on CMS prototype and production wafers to assess inter-channel properties such as the resistance between neighboring sensor channels, *p*-stop doping concentration, and implantation depth. While a quantitative analysis of these parameters with the implemented MOSFET test structures has not yet been achieved, it has been shown that MOSFET threshold voltage is sensitive to process related variations of *p*-stop properties and, consequently, provides a simple tool to qualitatively evaluate the inter-channel resistance [15, 99].

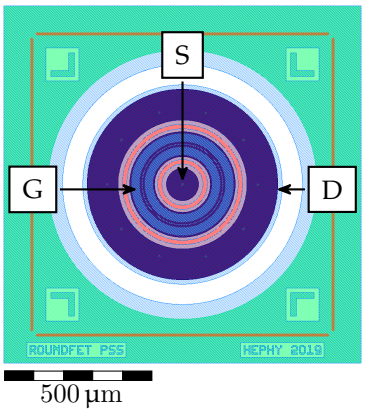
The standard design of the MOSFET test structures (Figure 6.31a) is composed of rectangular n^+ source (S) and drain (D) electrodes and a common gate electrode (G). Source and drain are spaced such that the MOSFET inter-channel region replicates the layout of the sensor inter-channel region, including *p*-stop implants that encircle drain and source electrodes. Different inter-channel spacings and *p*-stop layouts have been implemented. In particular, Outer Tracker production wafers and HGCAL LD 2019 wafers include MOSFET test structures with inter-channel design mirroring PS-s, 2S and HGCAL inter-channel layout.

In addition to the standard design that is optimized for small size and automated probe card measurements but is prone to edge effects, the wafers include circular MOSFET test structures that eliminate edge effects (Figure 6.31b). Similar to the standard structures, the circular MOSFETs replicate the inter-channel layout of different sensor types and include circular *p*-stop implants under the gate. Additionally, structures with the same inter-channel spacing but without *p*-stop implants are implemented to allow to quantify the influence of the *p*-stop implants on channel isolation and threshold voltage. Oval MOSFET test structures that agree with the 2×10 pad probe card standard and replicate 2S and PS-s inter-channel layout with and without *p*-stop implants (Figure 6.31c) are included in the set for automated PQC on Outer Tracker production wafers and HGCAL LD 2019 wafers.

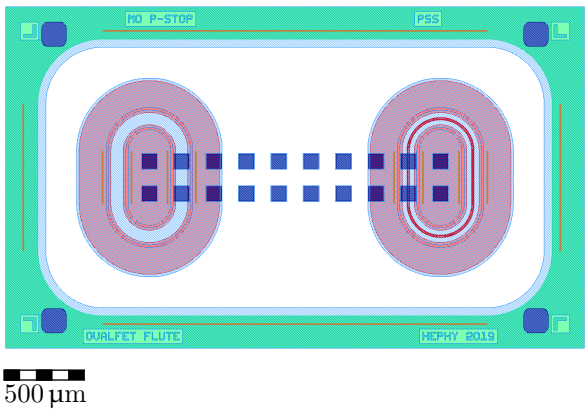
The threshold voltage V_{th} is extracted from MOSFET transfer characteristics in the linear region. For this purpose, a small bias voltage V_{DS} is applied between source and drain,



(A) Standard MOSFET test structure with probe card contacts.

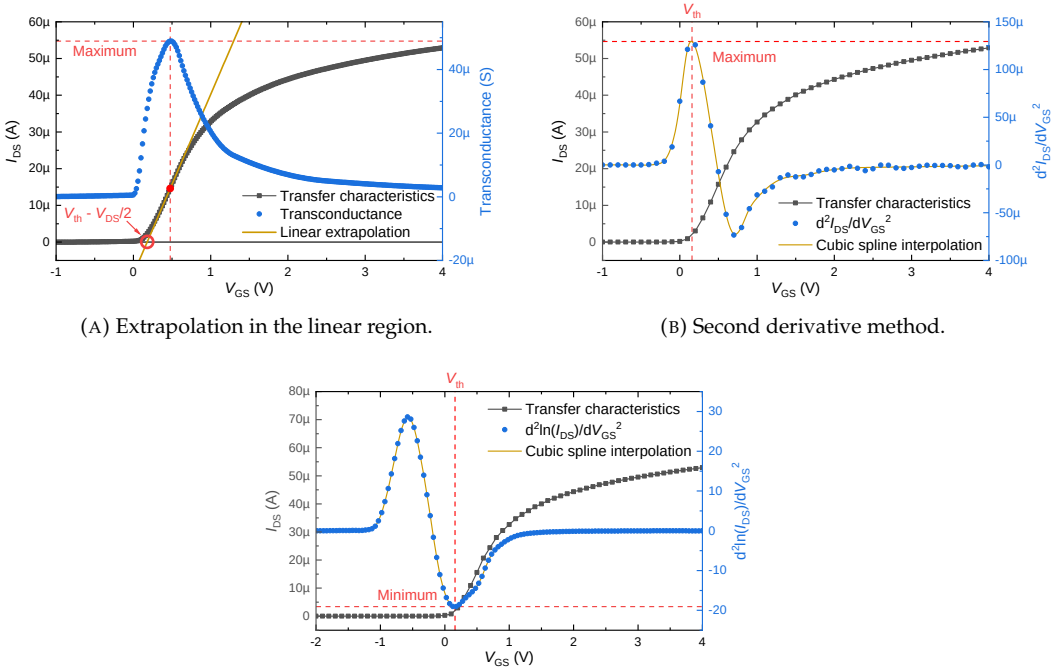


(B) Round MOSFET with p-stop implants between source and drain.



(C) Pair of oval MOSFET test structures with probe card contacts modeled on PS-s inter-channel layout with and without p-stop implants .

FIGURE 6.31: Types of MOSFET test structures implemented on CMS prototype and production wafers. General overview. Source, drain, and gate are labeled "S", "D", and "G", respectively. Variants with different inter-channel layouts modeled after sensor inter-channel layouts exist.



(A) Extrapolation in the linear region.

(B) Second derivative method.

(C) Second derivative logarithmic method.

FIGURE 6.32: Methods to extract MOSFET threshold voltage V_{th} from MOSFET transfer characteristics.

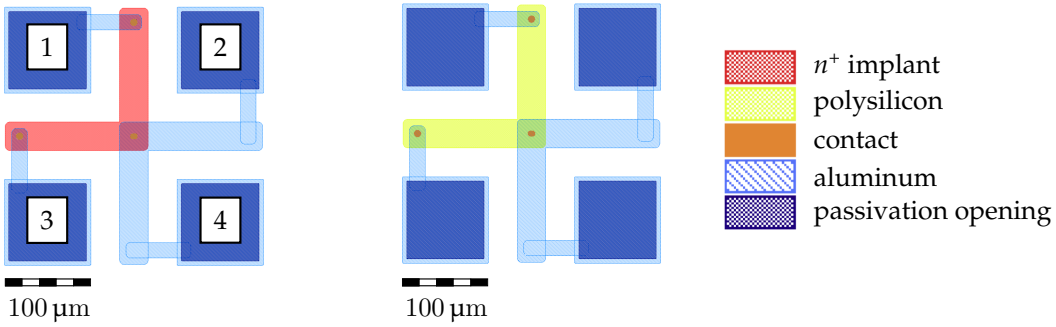
the voltage between gate and source V_{GS} is scanned from small negative voltages to small positive values, and the drain current I_{DS} is measured as a function of V_{GS}. Typical values used for PQC are $V_{DS} = 100\,\text{mV}$ and $V_{GS} = -5\,\text{V}$ to $10\,\text{V}$. A more in-depth discussion of the measurement scheme is given in [15].

For a given drain-source voltage, V_{th} is defined as the minimum gate-source voltage at which a conductive interconnection between source and drain is established. Different methods exist to extract V_{th} from MOSFET transfer characteristics (Figure 6.32) [43, 100, 101].

Perhaps the most popular extraction method, referred to as "extraction in the linear region" (ELR), determines V_{th} from the gate voltage axis intercept of the linear extrapolation of the I_{DS}–V_{GS} curve at the point of maximum transconductance (Figure 6.32a). The transconductance is given by the first derivative of the I_{DS}–V_{GS} curve. From the intercept of the linear extrapolation at $I_{DS} = 0$, the threshold voltage is determined by adding $V_{DS}/2$. While the ELR method is comparatively robust, its accuracy may be affected by parasitic series resistances at drain and source contacts. PQC for Outer Tracker and HGCAL primarily applies the ELR method to extract the MOSFET threshold voltage.

Alternatively, the second derivative (SD) method (Figure 6.32b) or the second derivative logarithmic (SDL) method (Figure 6.32c) can be applied. The SD method determines V_{th} as the maximum of the second derivative of the I_{DS}–V_{GS} curve. The SDL method, in contrast, defines V_{th} as the gate voltage at which drift and diffusion drain currents are equal. This point is determined as the minimum of the second derivative of the logarithm of the drain current. While both methods avoid the problems of parasitic series resistance, because both apply a second derivative, they are prone to measurement noise. In many cases, a smoothing filter must be applied and the measured characteristics must be interpolated to achieve a satisfactory result.

CMS PQC utilizes MOSFET threshold voltage to detect process variations that affect inter-channel isolation. In particular, for Outer Tracker prototype and production material, values of $V_{th} \geq 2\,\text{V}$ indicate inter-channel resistance values $> 100\,\text{G}\Omega$. Measurement results and TCAD simulations relating MOSFET threshold voltage and sensor inter-strip resistance on the Infineon PS-s prototype wafer run *VC740655* and discussion have been published



(A) Metal to n^+ CBKR. (B) Metal to polysilicon CBKR.

FIGURE 6.33: Four-terminal Cross-Bridge Kelvin Resistors (CBKR) implemented on CMS prototype and production wafers.

in [15].

6.8 Cross-Bridge Kelvin Resistor

The four-terminal Cross-Bridge Kelvin Resistor (CBKR) is commonly used to measure the specific contact resistivity ρ_c of metal-semiconductor contacts while eliminating the influence of the underlying semiconductor or the contacting metal conductor [43]. CMS prototype and production wafers include, essentially, two different CBKR test structures – one to measure the metal-n^+ contact resistance (Figure 6.33a) and one to determine the contact resistance between metal and polysilicon (Figure 6.33b).

Across the test structure, the voltage is measured between contacts 2 and 3 perpendicular to the current path between contacts 1 and 4. The specific contact resistivity ρ_c relates to the contact resistance R_c via $R_c = \rho_c/A$ where A is the contact area. The one-dimensional Kelvin model approximates $R_c = V_{23}/I_{14}$. However, this model is only accurate for large specific contact resistivity as it does not account for the current flowing in the overlap region between the contact edge and the sidewall of the n^+ diffusion region. In case of low specific contact resistivity, a two-dimensional model [102] that describes the measured resistance $R_k = V_{23}/I_{14}$ as the sum of the resistance R_c due to the voltage drop across the actual contact and the resistance R_{geom} due to the current flow around the contact in the overlap region yields more accurate results. Applying this model, the contact resistance is determined as

$$R_c = R_k - R_{geom} = \frac{V_{23}}{I_{14}} - \frac{4R_{sh}d^2}{3w^2}\left(1 + \frac{d}{2(w-d)}\right) \tag{6.54}$$

where R_{sh} is the n^+ or polysilicon sheet resistance, w is the respective line width, and d denotes the distance between the contact edge and the edge of the overlap region.

6.9 Contact Chain

CMS prototype and production wafers include contact chain test structures to determine the quality of the metal-n^+, metal-p^+, and metal-polysilicon contacts and to asses the frequency at which faulty contacts are produced. The basic layout is the same for every contact chain (Figure 6.34). Consecutive regions of implant or polysilicon are connected to overlying metal bridges with small contact holes at each end, forming chains. To isolate neighboring implant regions, the n^+ contact chain includes a p-stop encasing and the p^+ contact chain is surrounded by n^+ implants.

The process quality of the contacts is assessed by measuring the resistance of the contact chain. A single faulty contact will result in a significant increase of the measured resistance.

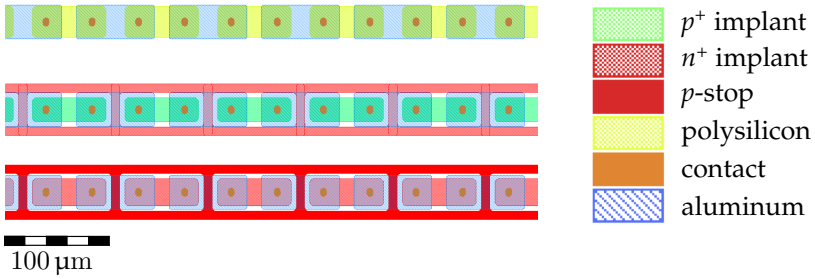


FIGURE 6.34: Polysilicon, p^+, and n^+ contact chains implemented on CMS prototype and production wafers.

The measured resistance can be compared to the expected value approximated considering measured metal, implant, and polysilicon sheet resistances. Alternatively, a relative comparison of the resistance measured on different wafers allows to determine an expected value and to detect outliers that indicate faulty contacts.

6.10 Dielectric Breakdown Test Structure

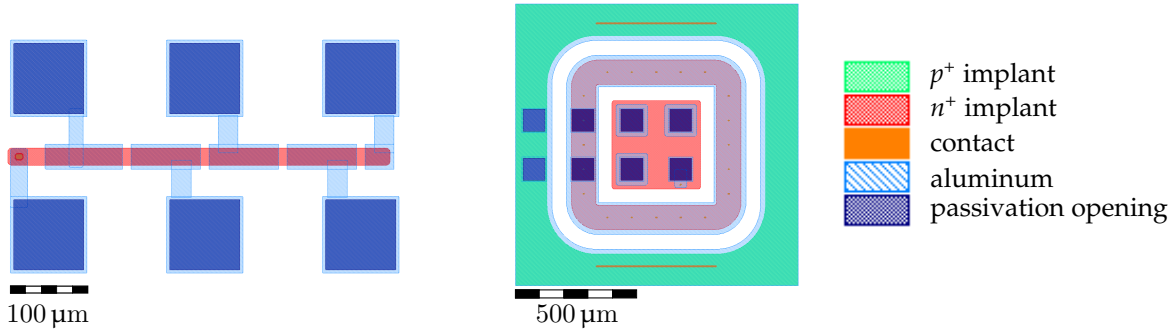
The breakdown voltage of the coupling dielectric is an important parameter that affects the high voltage stability of a silicon sensor. It is defined as the maximum voltage that can be applied across the dielectric before a substantial current flows between the n^+ implant and the metal pad. Contrary to the breakdown of the silicon bulk, which is caused by avalanche effects of the charge carriers, the breakdown of the dielectric is caused by stripping electrons from their atoms. Every impurity of the oxide can serve as the nucleation point for this breakdown effect. Breakdown at very low voltages is usually caused by gross defects such as pinholes or scratches.

Various test structures are implemented on CMS prototype and production wafers. While the design differs (Figure 6.35), the concept and measurement principle are the same for all structures. One contact pad is connected through the oxide to the underlying n^+ implant and a number of segmented metal electrodes form small capacitors with the underlying n^+ region. During measurement, ground potential is applied at the contact to the n^+ implant, and a positive voltage ramp is applied to one of the overlying metal electrodes. The voltage is increased until a current limit and, thus, dielectric breakdown is reached. Because the breakdown inflicts irreversible damage on the crystal structure of the oxide, this test cannot be performed on the main sensor. Consequently, a voltage ramp toward the onset of breakdown can only be performed once on any pair of n^+ and metal contacts.

6.11 Capacitor with Implant

The capacitance of the coupling dielectric is an important parameter that affects the readout noise of AC-coupled sensors. But also for DC-coupled sensors, the capacitance of the oxide atop n^+ implants proves useful because it allows to determine the thickness of the oxide, which, as a result of the production process, is notably smaller than the oxide thickness of a standard MOS-C without underlying n^+ implant. Monitoring this particular parameter over production time allows to detect process related thickness variations of the coupling dielectric.

The test structures implemented to measure the capacitance of the "thin oxide" or coupling dielectric are based on the same design as the structures intended to measure the breakdown voltage of the dielectric (Figure 6.36). One electrode provides the contact through the oxide to the underlying n^+ implant, and the capacitance is measured between this contact and a second electrode atop the oxide. To allow multiple measurements at varying locations



(A) Small standard implemented on early prototypes.

(B) New standard including guard and egde rings implemented on Outer Tracker production wafers and more recent HGCAL prototypes.

FIGURE 6.35: Types of dielectric breakdown test structures implemented on CMS prototype and production wafers.

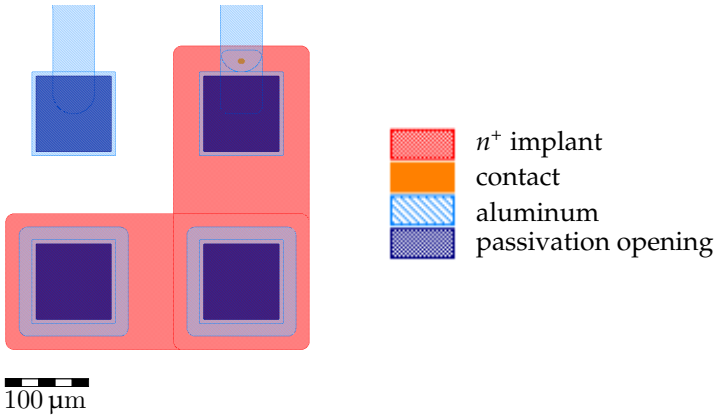


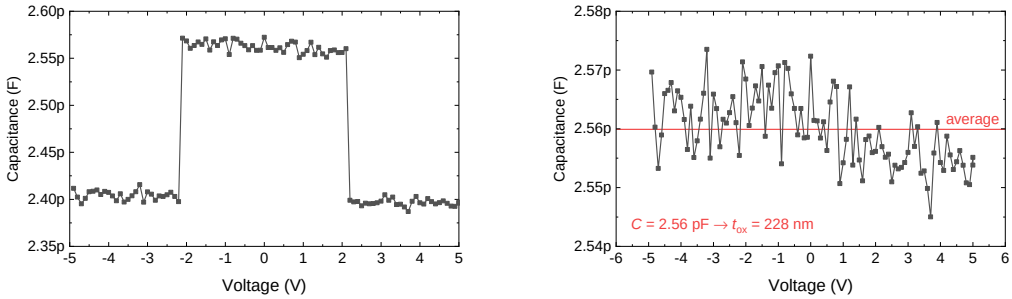
FIGURE 6.36: Capacitor test structure with n^+ implant.

atop the same n^+ implant, the test structures typically include more than one electrode atop the oxide.

To determine the coupling capacitance, the n^+ electrode is set to ground potential and a small symmetrical voltage ramp (e.g. $-5\,\mathrm{V}$ to $5\,\mathrm{V}$) is applied to the second electrode. At each voltage step, the capacitance is recorded. The coupling capacitance is then determined by averaging over the recorded capacitance values (Figure 6.37).

Because the structures are comparatively small, typical capacitance values are very low (i.e. on the order of $\sim 1\,\mathrm{pF}$). The absolute value of the measured capacitance depends on the LCR probe frequency and amplitude and is affected by stray capacitances. In particular, care must be taken to ensure that stray capacitances introduced via the voltage supply are corrected. Depending on the set source voltage range, the impedance of the voltage supplying SMU may vary. If the range setting of the SMU is set to "*AUTO*", the internal range of the device and, hence, the impedance may vary during the voltage scan, which can result in substantial variations of the measured capacitance depending on the applied DC voltage (Figure 6.37a). To avoid this problem, the source range of the SMU should be set to a fixed value, for which the stray capacitance at a given probe frequency should be prerecorded and subtracted from the measured capacitance (Figure 6.37b).

During Outer Tracker Pre-Series PQC, different settings for the AC probe frequency and amplitude were tested, and measurement results were found to be most stable at a probe frequency of $10\,\mathrm{kHz}$ and signal amplitude of $250\,\mathrm{mV}$. The measurement was corrected for stray capacitances and the oxide thickness t_{ox} was calculated using (6.29). Averaging over measurements on all wafers of the Outer Tracker Pre-Series, the thickness of the coupling



(A) The automatic range switching of the voltage source SMU during voltage scan changes the system impedance and causes symmetric jumps of the measured capacitance by $\sim 150\,\mathrm{fF}$ at $-2.1\,\mathrm{V}$ and $2.1\,\mathrm{V}$.

(B) Measurement corrected for stray capacitances.

FIGURE 6.37: Coupling capacitance measured on capacitor test structures with n^+ implant on an Outer Tracker Pre-Series wafer at probe frequency $10\,\mathrm{kHz}$ and signal amplitude $250\,\mathrm{mV}$. Effects of stray capacitance introduced via the voltage source (A). Corrected measurement (B).

dielectric was determined as $t_{ox} = (221 \pm 12)\,\mathrm{nm}$. This value is in good agreement to electron microscopy measurements performed on a Hamamatsu 2S prototype wafer, where $t_{ox} = (214 \pm 4)\,\mathrm{nm}$ was found.

6.12 Mask Misalignment Test Structure

In addition to test structures for electrical measurement, CMS prototype and production wafers include a dedicated test structure for optical evaluation of the alignment of the lithography masks for the individual sensor layers (Figure 6.38). The design of the most recent version of the structure (Figure 6.38a) was adapted from the original version [67] introduced as part of the first prototype of a test structure set for automated PQC (see section 7.1).

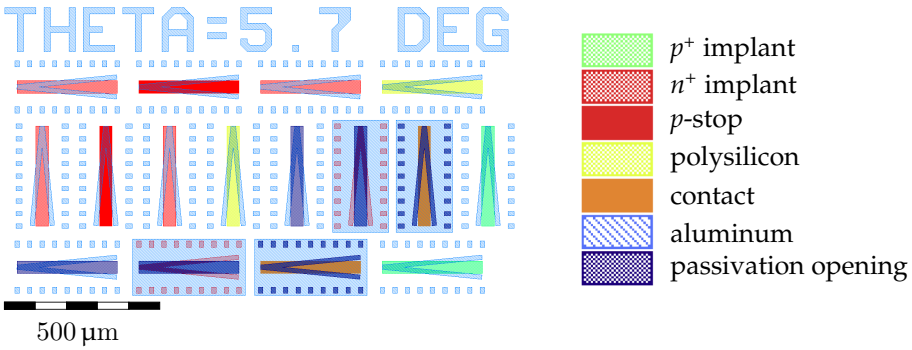
The structure allows to determine the mask misalignment for p^+, n^+, and p-stop implants, polysilicon layer, and passivation opening relative to the aluminum metalization layer. Additionally, a structure exists referring the misalignment of the passivation opening to the n^+ implant. The misalignment of the contact mask is referred to the passivation opening because the contact mask requires an uninterrupted metalization layer on top and, hence, cannot be referred to the metal layer, directly.

For each layer, the mask misalignment can be determined in two perpendicular directions (i.e. x and y directions). A misalignment ΔL of a layer relative to the "V"-shaped reference layer in any of these directions, expresses as a shift of the intersection points of the layer edges with the edges of the reference "V" (Figure 6.38b). The mask misalignment in the given direction can then be determined from the ratio of the distance between the intersection points L_1 and the measured distance between two small reference rectangles $L_{2,\,\mathrm{meas}}$ as per [67]

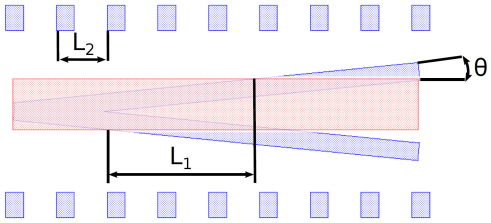
$$\Delta L = \frac{L_1}{L_{2,\,\mathrm{meas}}} \frac{L_{2,\,\mathrm{des}} \tan(\theta)}{2} \tag{6.55}$$

where $L_{2,\,\mathrm{des}}$ is the nominal distance between two small rectangles given by the GDS design file, and θ is the opening angle of the reference "V"-shape. By design, $L_{2,\,\mathrm{des}} = 20\,\mu\mathrm{m}$ and $\theta = 5.7°$ and (6.55) reduces to

$$\Delta L = \frac{L_1}{L_{2,\,\mathrm{meas}}}\,. \tag{6.56}$$



(A) Full layout.



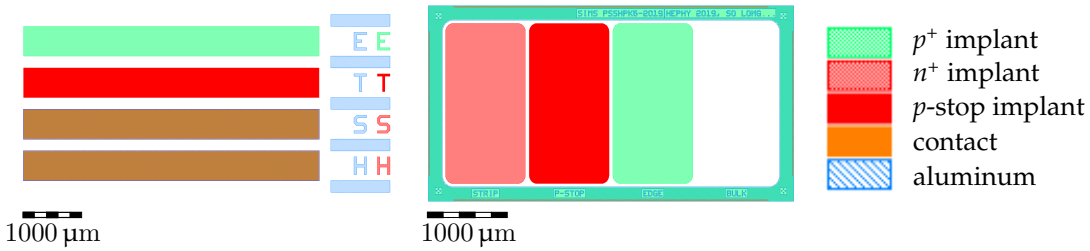
(B) Principle of misalignment calculation. Picture taken from [67].

FIGURE 6.38: Mask misalignment test structure implemented on CMS prototype and production wafers.

6.13 Structures for Mechanically Destructive Tests

CMS prototype and production wafers include test structures for Spreading Resistance Profiling (SRP) (Figure 6.39a) and Secondary Ion Mass Spectrometry (SIMS) (Figure 6.39b). While SRP measurements access the resistivity and, hence, the carrier density profile of a sample, SIMS measures the composition of the sample and, hence, yields the dopant concentration profile. Both measurement techniques require mechanical and chemical preparation of the sample and cannot be performed on a sensor without destroying its functionality.

The layout of the test structures for SRP and SIMS measurements is qualitatively similar. Both structures consist of separate regions of n^+, p^+, and p-stop implantation and include labels in the metalization corresponding to each layer. However, the SIMS test structure includes passivation openings above each rectangular segment to facilitate access to the silicon below, and the SRP structure features longer strips to support the necessary beveling of



(A) SRP test structure.

(B) SIMS test structure.

FIGURE 6.39: Test structures for SRP (A) and SIMS (B) implemented on CMS prototype and production wafers. The SIMS test structure includes above each rectangular segment passivation openings, which are omitted for clarity.

the surface. Both types of structures are included on Outer Tracker prototype and production wafers except for $8''$ Infineon and Hamamatsu 2S prototypes, which only include SIMS test structures. Similarly, all HGCAL prototypes only include the SIMS test structure, accounting for the limited space on the wafer. For these wafers, the SIMS test structure is utilized for both SRP and SIMS measurements.

The following sections briefly discuss the principles of SRP and SIMS measurements and present carrier density and dopant depth profiles extracted on different wafers.

6.13.1 Spreading Resistance Profiling

Spreading Resistance Profiling (SRP) [103, 104] is an electrical measurement technique that is mainly used to generate resistivity and carrier density depth profiles. For this purpose, the surface of the semiconductor sample is beveled at a shallow angle and two closely spaced, carefully aligned probe tips are stepped along the beveled surface to measure the resistance at each step. From the such obtained spreading resistance profile, the resistivity profile is determined by comparison with calibration samples. Typically, the measured spreading resistance is about 10^4 times higher than the semiconductor resistivity [43].

The resistivity profile can be converted into a carrier density depth profile. It has to be noted that, although they are often similar, the carrier density profile is not the same as the dopant density or doping profile. Carrier spilling at shallow junctions and wafer processing techniques such as annealing times and temperatures can cause the carrier density profile to be quite different from the dopant density profile [43].

Carrier density depth profiles of the n^+, p^+, and p-stop implants at the wafer front were determined from SRP measurements[10] on two wafers of the HGCAL LD 2019 run with target flatband voltages $V_{\text{fb}} = 2\,\text{V}$ and $V_{\text{fb}} = 5\,\text{V}$ (Figure 6.40). The process variation the manufacturer used to achieve the different target flatband voltages does not manifest in any obvious discrepancies of the carrier density profiles as the data are largely congruent for both wafers, in particular for n^+, p^+ implants. The p-stop profile shows some differences of the effective carrier density near the surface in accordance with the alteration of the equilibrium surface potential depending on the target flatband voltage. For the $5\,\text{V}$ material, more electrons accumulate at the surface, causing an effective drop of the net carrier density.

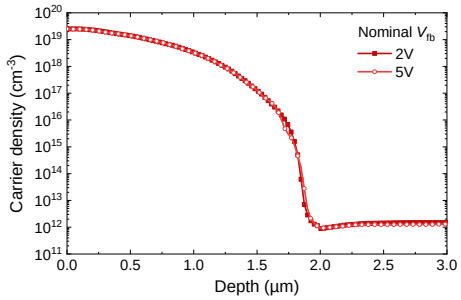
6.13.2 Secondary Ion Mass Spectrometry

In contrast to SRP, Secondary Ion Mass Spectrometry (SIMS) [105] is an analytical technique that accesses the impurity concentration of a semiconductor sample. While SRP extracts only the electrically active dopant profile, SIMS detects the total impurity density, which can be quite different.

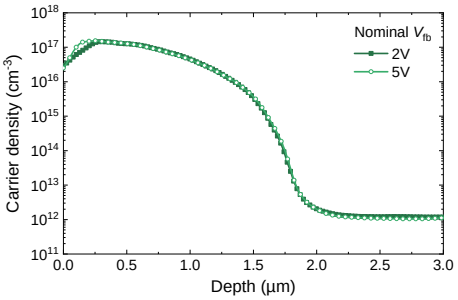
SIMS is a destructive method that utilizes a focused ion beam to eject secondary ions from the sample by sputtering. The ejected material is analyzed in a mass spectrometer. The secondary ion signal of a given dopant as a function of time is converted into a dopant density depth profile by measuring the depth of the sputtering crater at the sample surface. SIMS is sensitive to dopant concentrations as low as $10^{14}\,\text{cm}^{-3}$ [43].

The difference between carrier density and dopant density becomes apparent when comparing SRP profiles to depth profiles determined from SIMS measurements. Both techniques were applied to determine the profile of the p^+ implant at the back of an LD 2018 HGCAL wafer (Figure 6.41). While the SRP profile plateaus at a maximum carrier density of $\sim 10^{17}\,\text{cm}^{-3}$, the SIMS measurement yields boron concentrations as high as $\sim 10^{20}\,\text{cm}^{-3}$. The service provider[11] quotes a measurement inaccuracy of $10\,\%$ for both methods, which does not account for the observed discrepancies of up to three orders of magnitude. Hence, it has to be concluded that in case of the examined wafer the total dopant density is much larger than the density of electrically active dopants. The electrical activation of the implanted dopant ions is driven by wafer processing steps, in particular annealing conditions, and, depending on the respective process, SIMS and electrical measurement results can be very different [43].

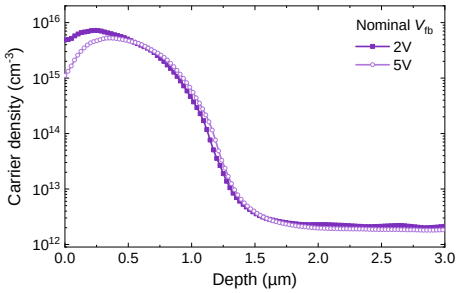
[10] The measurements were performed by *SGS Institut Fresenius*.
[11] *SGS Institut Fresenius*.



(A) Carrier density profile of the n^+ implant.



(B) Carrier density profile of the p^+ implant.



(C) Carrier density profile of the p-stop implant.

FIGURE 6.40: Carrier density depth profiles of the n^+ (A), p^+ (B), and p-stop layer (C) determined from SRP measurements on two wafers of the HGCAL LD 2019 run with target flatband voltages $V_{fb} = 2\,V$ and $V_{fb} = 5\,V$.

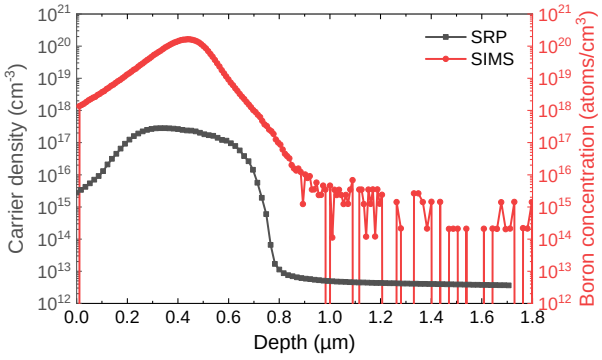


FIGURE 6.41: Comparison of the carrier density measured with SRP and the boron concentration depth profile measured with SIMS of the p^+ implant at the back of an LD 2018 HGCAL wafer.

CHAPTER 7

TEST STRUCTURE SET FOR AUTOMATED PROCESS QUALITY CONTROL

Process quality control (PQC) for large-scale silicon sensor productions, such as the CMS Outer Tracker and HGCAL, requires an efficient and stable measurement procedure that ensures comparability of results across wafer batches, test centers, and over the full production time. Ideally, the procedure should allow to track the evolution of relevant process parameters and detect trends indicating potential future problems. To this end, the PQC procedure works with a set of test structures that provide access to all relevant process parameters. The set was designed as a central part of this thesis and is implemented on all current and future Outer Tracker production wafers as well as the most recent HGCAL prototypes.

Within the set, test structures are grouped such that the most important process parameters can be accessed using a quick subset of measurements and additional test structures provide the possibility for in-depth analysis in case of any arising irregularities. The set facilitates automated measurements using a 20-needle probe card but can also be operated using individual probe needles. It is designed such that the assessment of the most important process parameters is possible in about 30 minutes.

The following sections illustrate the development of the set of test structures that will be used for CMS Outer Tracker and HGCAL PQC. A brief introduction is given on the first prototypes that were implemented on Outer Tracker prototype wafers. Subsequently, the final version of the set and its components are discussed in detail. Lastly, results of PQC tests using the set are presented, including a comprehensive look on the Outer Tracker Pre-Series batch and a smaller number of test structures on HGCAL LD 2019 and HD 2019 prototypes.

7.1 First Prototypes

The first prototype of a test structure set for the usage with probe cards was introduced in [67]. It is included in its original form on all $8''$ Infineon 2S prototype wafers. For the subsequent production of $6''$ PS-s prototype wafers, the set was adapted (Figure 7.1). Main changes include the addition of a guard and an edge ring around the central MOS-C and the inclusion of various capacitors with n^+ implant.

The set consists of 12 arrays of 2×10 contact pads, denoted "flute", to which the test structures are connected. It is grouped into three squares of four flutes each, whereby half of the flutes are rotated by $90°$. This design was chosen to enable the use of larger probe cards that would allow to contact four flutes at once and speed up the measurement process during production. However, due to the added complexity and cost considerations, the full-size version of the rotated design was abandoned for the final PQC strategy in favor of a design with parallel flutes optimized for 20-needle probe cards (see section 7.2). However,

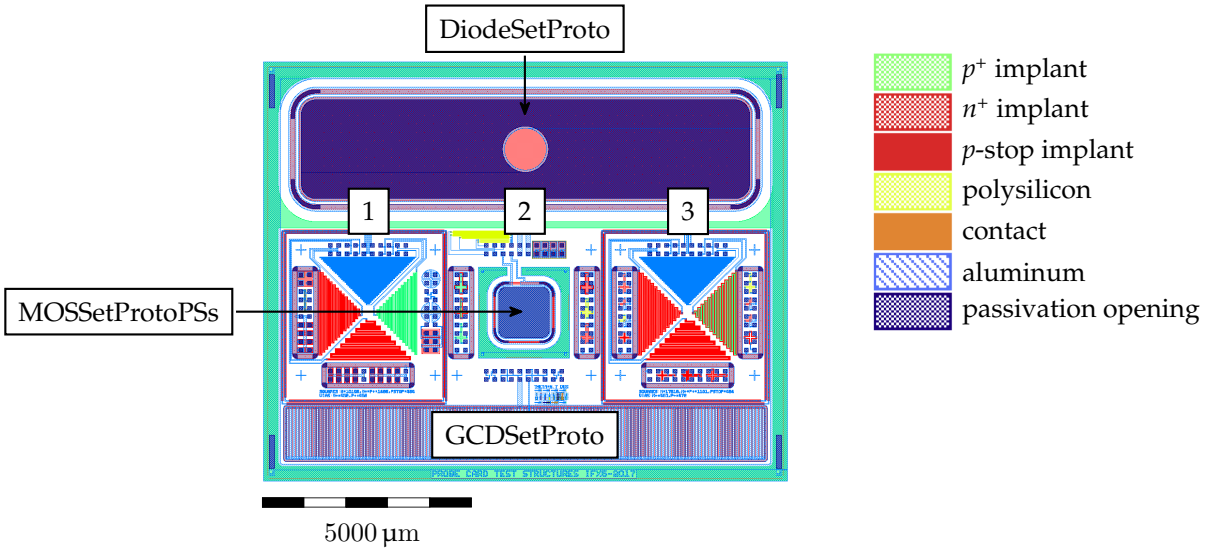


FIGURE 7.1: Prototype of a test structure set for automated PQC as implemented on Infineon PS-s prototype wafers. The set was adapted from the initial version introduced in [67]. It consists of three sets of four flutes each, labeled "1–3", enclosed by a common edge ring. Set "1" includes four meander structures, capacitors with n^+ implant, a dielectric breakdown test structure, various MOSFET test structures, cloverleaf-shaped metal van-der-Pauw structures, and a four-terminal bulk resistivity test structure. Set "2" contains a rectangular diode (labeled "DiodeSetProto"), an MOS-C (labeled "MOSSetProtoPSs"), a GCD (labeled "GCDSetProto"), various van-der-Pauw cross-bridge structures, four-terminal resistivity test structures, polysilicon meanders, capacitors with n^+ implant, and a mask misalignment test structure. Set "3" includes four meander structures, various van-der-Pauw structures, a van-der-Pauw type bulk resistivity test structure, and various CBKR structures.

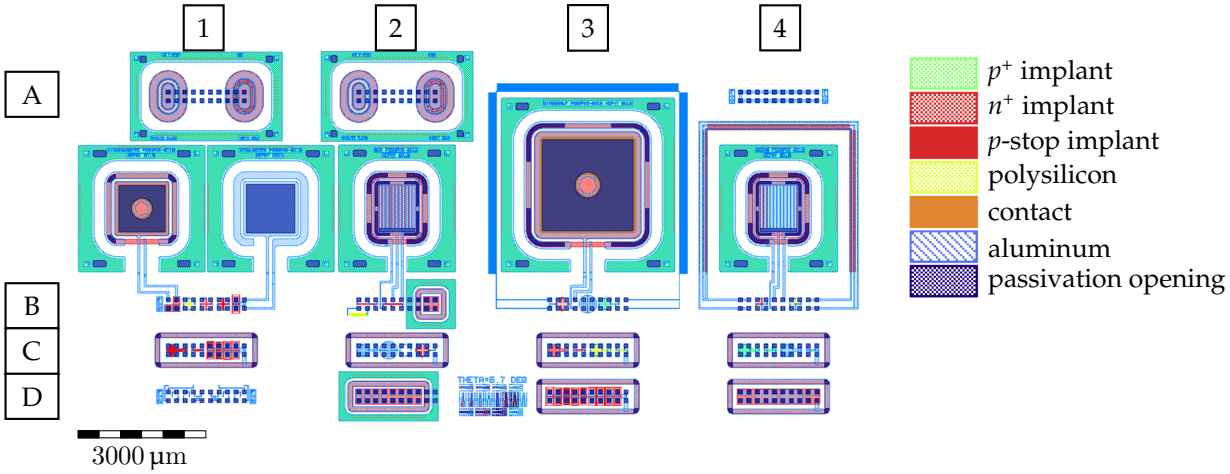


FIGURE 7.2: Test structure set for automated PQC. Test structures are connected to 15 arrays of 2×10 contact pads each (denoted "flute") that facilitate measurement using a 20-needle probe card. Flutes are arranged in four rows (labeled "A"–"D") and four columns (labeled "1"–"4"). The four main flutes, "B1"–"B4" access all relevant process parameters and are denoted "PQC1"–"PQC4". Additional flutes are intended for alignment, contact verification, and in-depth analysis of dedicated process parameters. Test structures contained in each flute are listed in Table 7.1.

aside from the new set, HGCAL prototype and Outer Tracker production wafers include smaller sets mirroring squares 1 and 3 of the rotated design to both maintain comparability with earlier prototypes and increase the variety of test structures accessible on every wafer.

7.2 A Set for Automated PQC

The test structure set developed as part of this thesis constitutes the basis of automated PQC for the Outer Tracker and HGCAL silicon sensor series productions. It advances the prototypes introduced in section 7.1 and draws on the experience gained from measurements and simulations of the test structures discussed in chapter 6. The design prioritizes the quick assessment of the most relevant process parameters and a compact size to allow comfortable placement on the limited space of the wafer periphery. Consequently, typically large devices such as diodes and GCDs are sized down as far as reasonably possible, and the number of flutes needed to obtain a complete picture of the wafer quality is kept as low as possible. Four dedicated flutes provide access to all relevant process parameters, while the measurement of two of these flutes suffices for a satisfactory overview of the wafer quality. In combination with an automated measurement setup, the set can support the assessment of the two main flutes in about 30 minutes.

The following sections introduce the layout of the set and the included test structures and discuss the general measurement procedure of automated PQC.

7.2.1 Layout and Test Structures

The set for automated PQC consists of 15 flutes arranged in a grid of 4×4 (Figure 7.2). Flutes are spaced in integral multiples of horizontal distance $4.5\,\mathrm{mm}$ and vertical distance $1.086\,\mathrm{mm}$, except for rows labeled "A" and "B", which feature a vertical distance of $4.5 \times 1.086\,\mathrm{mm}$. The first row contains only three flutes located in columns 1, 2, and 4, respectively. The test structures contained in the set (Table 7.1) allow a comprehensive assessment of the process quality and provide the means for in-depth analysis of individual process parameters.

Four main flutes, labeled "PQC1"–"PQC4" (Figure 7.3), access all relevant process parameters. The first two of these, flutes "PQC1" and "PQC2", suffice to provide a satisfactory overview of wafer properties. They access full depletion voltage, bulk resistivity, MOS-C

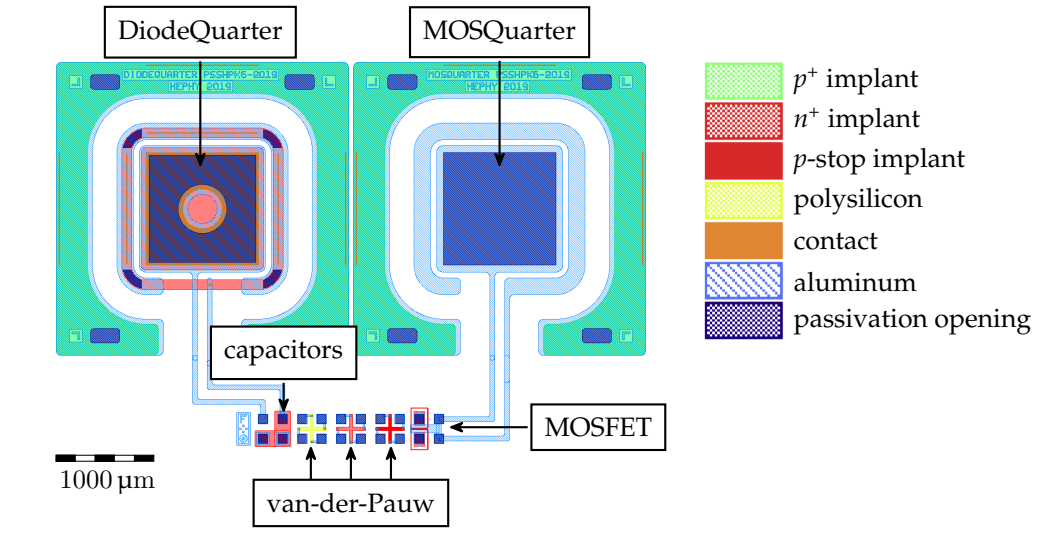
TABLE 7.1: Test structures and functions listed for each individual flute of the set for automated PQC. Rows and column numbers refer to the scheme in Figure 7.2. For an overview of process parameters that can be extracted with each test structure, refer to Table 6.1.

Row	Column	Name	Test structures
A	1		Oval MOSFETs with 2S inter-channel dimensions
	2		Oval MOSFETs with PS-s inter-channel dimensions
	4		Flute for alignment and contact verification
B	1	PQC1	Diode ("DiodeQuarter"), MOS-C ("MOSQuarter"), capacitors with n^+ implant, polysilicon, n^+, and p-stop van-der-Pauw crosses, MOSFET
	2	PQC2	GCD with $w/p = 0.5$ ("GCDPQC"), polysilicon meander (476 squares), n^+ and p-stop line width structures, dielectric breakdown test structures
	3	PQC3	Diode ("DiodeHalf"), metal meander ($12\,853$ squares), van-der-Pauw type four-terminal bulk resistivity test structure, metal cloverleaf van-der-Pauw, p^+ van-der-Pauw cross-bridge
	4	PQC4	GCD with $w/p = 0.75$ ("GCD05"), polysilicon, p^+, and n^+ contact chains with 228 contacts each, and n^+ and polysilicon CBKRs
C	1		P-stop van-der-Pauw cross-bridge and line width structure, MOSFETs with 2S, PS-s, and HGCAL inter-channel dimensions
	2		Metal van-der-Pauw cross-bridge and cloverleaf, van-der-Pauw type four-terminal bulk resistivity test structures with and without surrounding n^+
	3		N^+ and polysilicon van-der-Pauw cross-bridges and line width structures
	4		P^+ and metal van-der-Pauw cross-bridges and line width structures
D	1		Collinear four-terminal resistivity test structures with different contact distances, with and without p^+ implants under the contacts
	2		Dielectric breakdown test structures
	3		MOSFET test structures with different inter-channel dimensions
	4		Capacitors with common n^+ implant

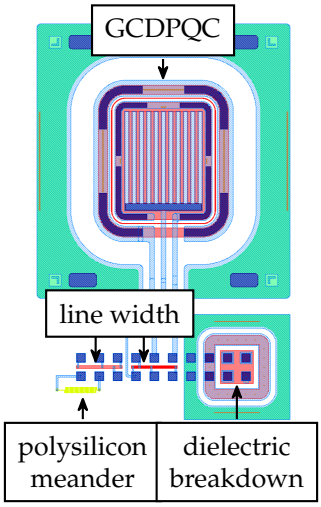
flatband voltage, fixed oxide charge concentration, oxide thickness, coupling capacitance, polysilicon, n^+, and p-stop sheet resistance, MOSFET threshold voltage, surface generation velocity, bias resistance, n^+ and p-stop line width, and dielectric breakdown voltage. Flutes "PQC3" and "PQC4" complete the parameter set, covering metal and p^+ sheet resistance, bulk resistivity, bulk generation lifetime, contact quality, and contact resistance. The set includes two diodes, located in flutes "PQC1" and "PQC3", to enable the correction of edge effects (see section 6.1.3). Diodes, MOS-C, and GCDs all feature an opening in their respective edge ring p^+ implant and metalization to allow the passage of metal connections to flute pads. In particular, the opening of the p^+ implant was implemented because previous studies [67] found improved high voltage stability of this configuration compared to a configuration where only the edge ring metalization was partially removed.

The remaining 11 flutes of the set allow for in-depth analysis of individual process parameters. The flutes contain multiple versions of different test structures with varied geometry. Flutes in row "C" are dedicated to sheet resistance and line width measurements and the evaluation of inter-channel isolation. They include van-der-Pauw type structures of all sensor layers and MOSFET test structures with different nominal line widths and inter-channel geometries. The four flutes of row "D" each provide various test structures to access a different process parameter, namely, bulk resistivity, dielectric breakdown voltage, inter-channel isolation and coupling capacitance. Furthermore, the set includes two flutes with oval MOSFET test structures in row "A". The oval MOSFET flutes replicate the inter-strip geometry of the Outer Tracker 2S and PS-s sensor, respectively. Additionally, row "A" contains a flute framed by alignment marks to facilitate the automated alignment with respect to the probe card. The individual pads of the flute are connected with a common metal line to facilitate automated contact verification via resistance measurements between all probe needles. Flutes "PQC1" and "D1" also feature alignment marks to allow relative alignment with respect to different points in the set.

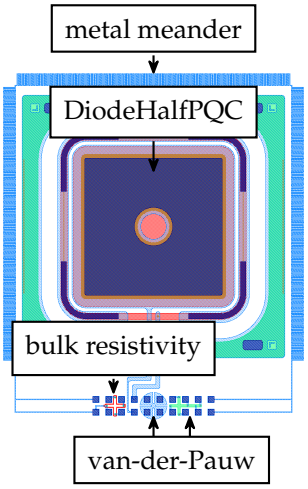
In addition to test structures for electrical measurements, the set contains an optical test structure to measure the alignment accuracy of the lithography masks (see section 6.12)



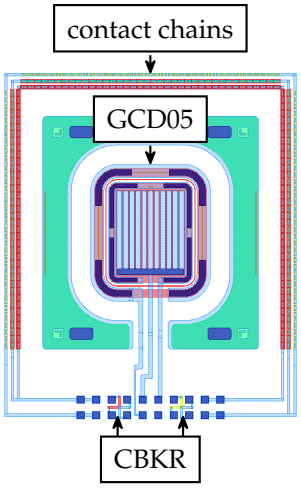
(A) Flute "PQC1".



(B) Flute "PQC2".

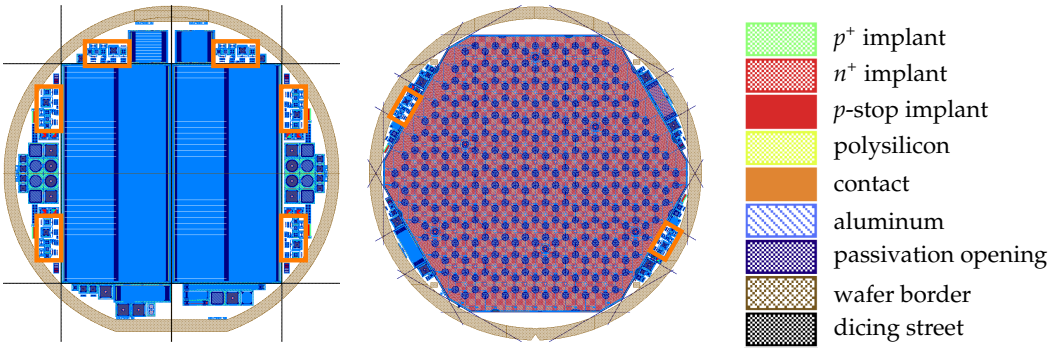


(C) Flute "PQC3".



(D) Flute "PQC4".

FIGURE 7.3: Four main flutes for automated PQC. Flutes "PQC1" (A) and "PQC2" (B) access the most relevant process parameters that allow a satisfactory overview on wafer properties. Flutes "PQC3" (C) and "PQC4" (D) complete the parameter set. In conjunction, the four flutes allow a complete assessment of all process parameters. The standard PQC procedure foresees only the measurement of flutes "PQC1" and "PQC2" on each tested wafer, while the full set of four flutes is tested at least once per delivered wafer batch.



(A) Outer Tracker. (B) HGCAL.

FIGURE 7.4: Instances of the PQC set (highlighted in orange) in the layout of Outer Tracker (A) and HGCAL (B) wafers. Tracker wafers contain six instances of the set, and HGCAL wafers contain two instances on opposite sides, allowing for tracking of process parameter variations across the wafer area. Figures adapted from [13].

located in the center of row "D".

To allow for tracking of process parameter variations across the wafer area, the set is implemented six times on all Outer Tracker wafers and twice on all HGCAL wafers (Figure 7.4). Because every wafer features the same design of the set, cross-comparability between production batches, test centers, and over the full three-year production time is maintained.

7.2.2 Measurement Procedure

PQC for the Outer Tracker series production aims to test a minimum of $20\,\%$ of all wafers per delivered batch. The standard procedure foresees the measurement of all process parameters on flutes "PQC1" and "PQC2" on two locations of each tested wafer. Depending on measurement settings such as number of voltage steps and waiting time in-between steps, as well as the time it takes to move between flutes, the measurement of "PQC1" and "PQC2" takes between 30 minutes and 1 hour. Generally, all measurements are performed on the large "halfmoon" cutoffs west and east of the main sensors (compare Figure 7.4a). To efficiently detect parameter variations across the wafer area, the two measured sets are chosen such that their distance becomes maximal (i.e. either the upper set on the western halfmoon is measured together with the lower set on the eastern halfmoon or the lower set on the western halfmoon is measured in conjunction with the upper set on the eastern halfmoon). The remaining four test structure sets are not tested by default but serve as backup in case of any irregularities detected during the standard measurement. A comprehensive characterization of all process parameters, utilizing flutes "PQC1"–"PQC4" and the optical mask misalignment test structure, is performed at least once per delivered wafer batch. With an automated setup, a measurement of all four PQC flutes takes between 1 and 1.5 hours.

HGCAL has not decided on the official PQC procedure for series production. However, it may be feasible to adopt a procedure similar to the Outer Tracker series production and measure flutes "PQC1" and "PQC2" on both instances of the set on each tested wafer and perform a full measurement of flutes "PQC1"–"PQC4" once per delivered wafer batch. Measurement times for HGCAL would likely be shorter than those for the Outer Tracker because structures targeting the polysilicon layer are not included in the HGCAL process and structures such as capacitors with n^+ implant might be skipped as they are not immediately required to judge HGCAL process quality.

TABLE 7.2: Summary of results for Outer Tracker Pre-Series PQC and comparison to predefined qualification parameter limits. The results of parameters without predefined limits provide the basis for expectation limits during series production.

Process parameter	Limit	Pre-Series results	
Full depletion voltage, V_{dp}	$< 350\,\mathrm{V}$	260 ± 14	V
Bulk resistivity, ρ	$> 3.5\,\mathrm{k\Omega\,cm}$	3.14 ± 0.45	$\mathrm{k\Omega\,cm}$
Flatband voltage, V_{fb}	$< 5\,\mathrm{V}$	2.34 ± 0.07	V
Fixed oxide charge concentration, N_{ox}		$5.28 \pm 0.22 \times 10^{10}$	$\mathrm{cm^{-2}}$
Oxide thickness, t_{ox}		676 ± 6	nm
Coupling capacitance, C_{ac}	$> 12\,\mathrm{nF\,cm^{-2}}$	15.86 ± 0.95	$\mathrm{nF\,cm^{-2}}$
MOSFET threshold voltage, V_{th}		4.43 ± 0.08	V
Dielectric breakdown voltage, V_{bd}	$> 150\,\mathrm{V}$	213 ± 4	V
Surface generation velocity, s_{g}		1.11 ± 0.11	cm/s
Sheet resistance n^+, $R_{\mathrm{sh},\,n^+}$	$< 250\,\Omega/\mathrm{sq}$	36.1 ± 0.9	Ω/sq
Sheet resistance p-stop, $R_{\mathrm{sh},\,p\text{-stop}}$		19.29 ± 0.35	$\mathrm{k\Omega/sq}$
Sheet resistance polysilicon, $R_{\mathrm{sh,\,poly}}$		2.43 ± 0.11	$\mathrm{k\Omega/sq}$
Sheet resistance aluminum, $R_{\mathrm{sh,\,alu}}$	$< 30\,\mathrm{m\Omega/sq}$	20.3 ± 0.2	$\mathrm{m\Omega/sq}$
Sheet resistance p^+, $R_{\mathrm{sh},\,p^+}$		1.36 ± 0.05	$\mathrm{k\Omega/sq}$
Bias resistance, R_{poly}	$< (1.5 \pm 0.5)\,\mathrm{M\Omega}$	1.91 ± 0.17	$\mathrm{M\Omega}$
Resistance metal meander, R_{alu}		416 ± 37	Ω
Line width n^+, w_{n^+}		37.5 ± 0.9	µm
Line width p-stop, $w_{p\text{-stop}}$		37.6 ± 2.2	µm
Line width p^+, w_{p^+}		36.1 ± 0.8	µm
Contact resistance n^+, $R_{\mathrm{c},\,n^+}$		66 ± 75	Ω
Contact resistance polysilicon, $R_{\mathrm{c,\,poly}}$		111.5 ± 43.4	$\mathrm{k\Omega}$
Resistance contact chain n^+, $R_{\mathrm{cc},\,n^+}$		71.1 ± 10.6	$\mathrm{k\Omega}$
Resistance contact chain p^+, $R_{\mathrm{cc},\,p^+}$		70.2 ± 1.2	$\mathrm{k\Omega}$
Resistance contact chain polysilicon, $R_{\mathrm{cc,\,poly}}$		30.3 ± 2.5	$\mathrm{M\Omega}$

7.3 Results and Discussion

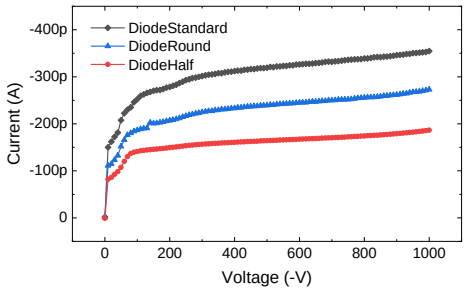
The set of test structures for automated PQC was first included in the wafer design for Outer Tracker Pre-Series and the HGCAL LD 2019 and HD 2019 prototype runs. Wafers for these designs were delivered in 2020. The Outer Tracker Pre-Series wafers were subjected to a detailed analysis with the premise to both gain in-depth understanding of the wafer material and develop the PQC routine in all test centers. Consequently, PQC measurements included flutes "PQC1"–"PQC4" on all wafers of the Pre-Series batch and on at least two different locations per individual wafer. In case of HGCAL, measurements were performed on a limited number of wafers and test structures.

In the following, results for Outer Tracker Pre-Series, HGCAL LD 2019 and HD 2019 wafers are presented. Outer Tracker results are compared to predefined parameter specifications. The results provide the basis for expectation limits for PQC during Outer Tracker series production, particularly, for parameters for which no hard limits have been set with the vendor.

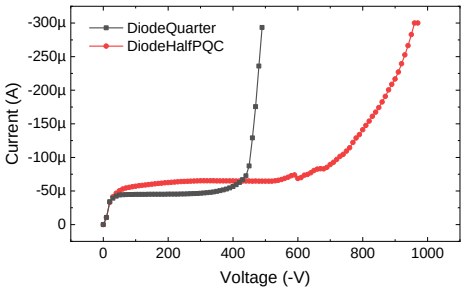
In contrast to the Outer Tracker, the HGCAL wafer design and production process are currently still subject to change. The presented results, hence, cannot be used to specify official process parameter ranges, but they can provide an estimate of the quality of the current prototypes and help determine the feasibility of the test structure set and the automated measurement setup for future HGCAL PQC.

7.3.1 Outer Tracker Pre-Series

The 40 wafers comprising the CMS Outer Tracker Pre-Series were subjected to PQC at test centers Brown University, INFN Perugia, NCSR Demokritos, and HEPHY Vienna. 10 wafers, labeled "16"–"26" (no. "25" was not included in the delivery) were tested in Vienna. Measurements were performed on the large "halfmoon" cutoffs west (labeled "WW") and east (labeled "EE") of the main sensor (compare Figure 7.4a). As each cutoff contains two instances of the set for automated PQC, the individual sets are labeled "Left" and "Right"



(A) I–V curves for diodes with closed edge ring and floating guard ring.



(B) I–V curves for diodes in the PQC set with opened edge ring and floating guard ring.

FIGURE 7.5: Influence of opened edge ring on diode I–V characteristics for Outer Tracker Pre-Series. Compared to standard diodes with closed edge ring and floating guard ring (A), I–V measurements of diodes with opened edge ring (B) exhibit currents higher by five orders of magnitude.

with respect to central symmetry axis of the respective cutoff and the dicing line facing south. The smaller cutoffs located at the top of the wafer and labeled northwest ("NW") and northeast ("NE") were not tested systematically.

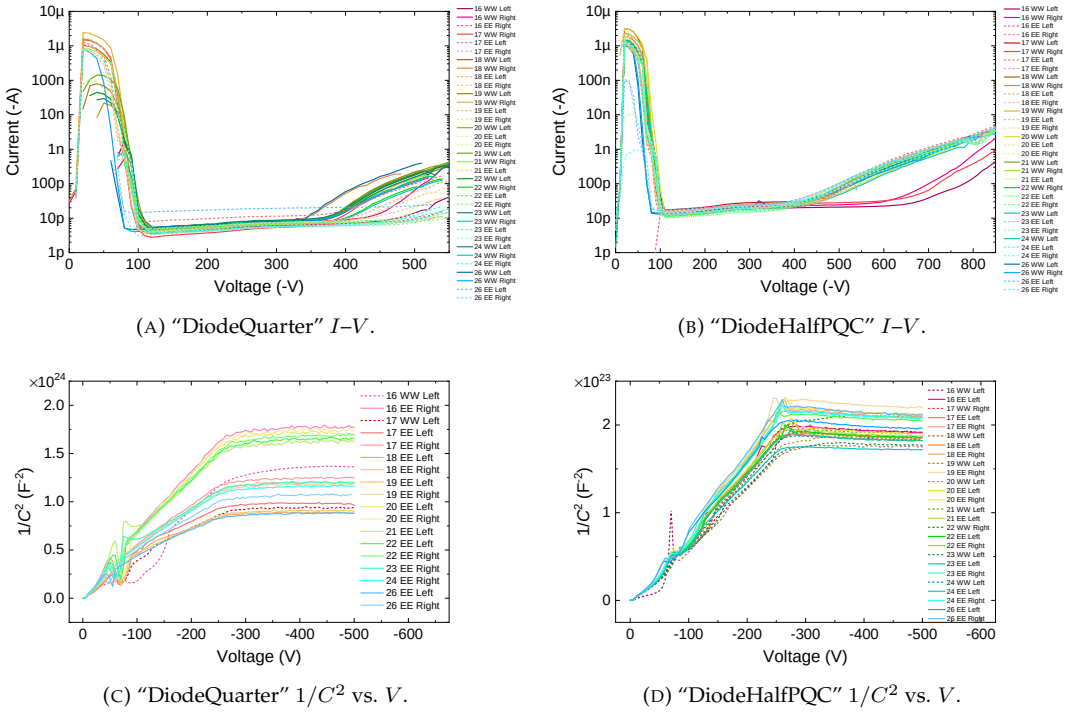
Generally, the PQC results of the Outer Tracker Pre-Series proved a satisfactory quality of the wafer material (Table 7.2). Process parameters were consistent between different wafers and largely lay well within predefined limits. Results agreed well between test centers. Consequently, where significant deviations occurred, they could be attributed to differences in the measurement setups of the respective test centers. In particular, by comparison with results from other PQC test centers, issues with the measurement of metal cloverleaf van-der-Pauw structures and four-terminal van-der-Pauw type bulk resistivity test structures were found for the setup in Vienna.

The following sections present the results obtained on all 10 Pre-Series wafers tested in Vienna for each individual type of test structure.

Diodes

During the first measurements of diodes on Outer Tracker Pre-Series wafers, it was observed that I–V characteristics of the diodes with opened edge ring that are part of the set for automated PQC exhibited extremely high currents on the order of 50 µA. This value was higher than the current measured on regular diodes with closed edge rings on the same wafers by five orders of magnitude (Figure 7.5). Similar influences of that magnitude were not observed for previous prototypes of diodes with opened edge rings such as those of Figure 6.2. Furthermore, the diodes of the PQC set showed early breakdowns that were not seen on regular diodes. It was concluded that the opened edge ring allowed the introduction of parasitic currents from surrounding structures and defects at the wafer dicing edge. Consequently, I–V measurements of diodes with opened edge ring were performed with the guard ring connected to ground (compare section 6.1.1, Figure 6.3b).

Diode I–V characteristics were measured on "DiodeQuarter" (Figure 7.6a) and "DiodeHalfPQC" (Figure 7.6b) with the guard ring connected to ground potential. Because no p-stop implant is included between diode pad and guard ring (compare section 6.1.1), the I–V characteristics exhibited high currents in the range between 0 V and about 100 V for both diodes. For higher voltages, low currents on the order of 10 pA were measured until a soft breakdown occured at about 400 V for most measured diodes. While the measured current between 100 V and 400 V was about the same for diodes with closed edge ring, these diodes showed stable I–V curves without breakdown up until 1000 V (compare Figure 6.4a). Hence, it is concluded that the premature breakdowns observed for the diodes in the PQC set were solely caused by the altered geometry with respect to standard diodes and are not an inherent property of the wafer material. As a consequence, however, it has to be noted that



(A) "DiodeQuarter" I–V.

(B) "DiodeHalfPQC" I–V.

(C) "DiodeQuarter" $1/C^2$ vs. V.

(D) "DiodeHalfPQC" $1/C^2$ vs. V.

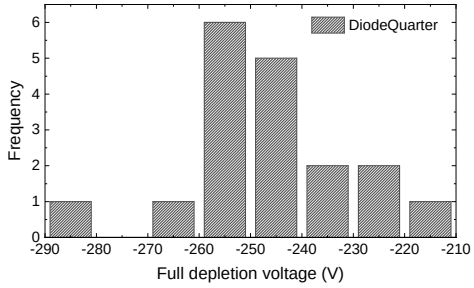
FIGURE 7.6: Outer Tracker Pre-Series PQC: diode I–V and $1/C^2$ vs. V results.

I–V measurements of diodes that are part of the PQC set cannot provide a reliable estimate of the sensor leakage current, which, according to specifications, would have to be measured at $600\,\mathrm{V}$.

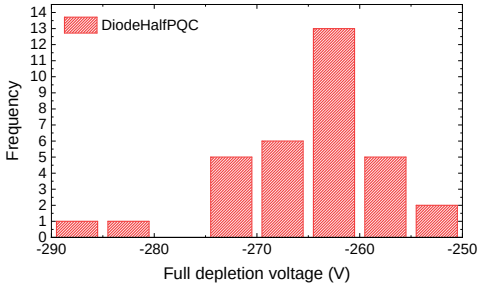
C–V characteristics with grounded guard ring (Figure 7.6c and 7.6d) also demonstrated an influence of the opened edge ring. Curves generally showed irregular behavior below about $150\,\mathrm{V}$. However, in most cases, the range around full depletion was not affected and it was possible to accurately extract the full depletion voltage $V_{\mathrm{dp}} = (260 \pm 14)\,\mathrm{V}$ and calculate the bulk resistivity $\rho = (3.14 \pm 0.45)\,\mathrm{k\Omega\,cm}$ from $1/C^2$ vs. V characteristics (Figure 7.7). On average, measurements were more reliable for the larger "DiodeHalfPQC" than for "DiodeQuarter". The smaller "DiodeQuarter" generally showed a large spread of the measured minimum capacitance after full depletion, and, for nearly $50\,\%$ of all measurements (particularly prevalent on the western halfmoon), "DiodeQuarter" characteristics did not yield the typical $1/C^2$ vs. V behavior detailed in section 6.1.2. Instead, curves showed a strong voltage dependency of parasitic capacitances, likely related to high peripheral currents and the capacitive coupling of surrounding test structures via the probe card contacts. Consequently, a reliable extraction of the full depletion voltage was not possible for about $50\,\%$ of all measurements of "DiodeQuarter". It is concluded that the larger "DiodeHalfPQC", which is part of flute "PQC3", is better suited to determine the full depletion voltage and, subsequently, calculate the bulk resistivity. As a consequence, the standard PQC procedure may need to be adapted to include flute "PQC3". However, the probe card measurement introduces additional parasitic capacitances also to the measurement of "DiodeHalfPQC", and the resulting minimum capacitance above full depletion is not suited to correctly determine the active thickness of the wafer. Furthermore, because of the general irregular behavior of the measured C–V characteristics and the significant influence of unknown parasitic capacitances, a correction of edge effects by combining results of "DiodeQuarter" and "DiodeHalfPQC" was not feasible.

MOS-C

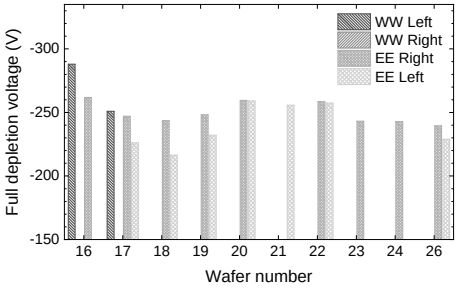
MOS-C C–V characteristics were very uniform for all measured wafers (Figure 7.8a). The extracted flatband voltages varied between $2.1\,\mathrm{V}$ and $2.5\,\mathrm{V}$ (Figure 7.8b, 7.8c), the resulting



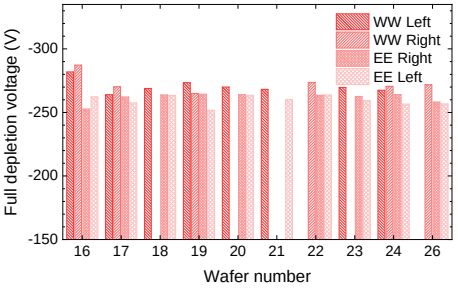
(A) "DiodeQuarter" V_{dp} histogram.



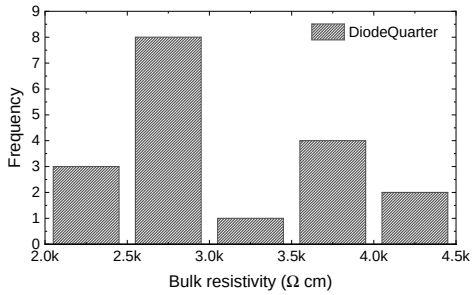
(B) "DiodeHalfPQC" V_{dp} histogram.



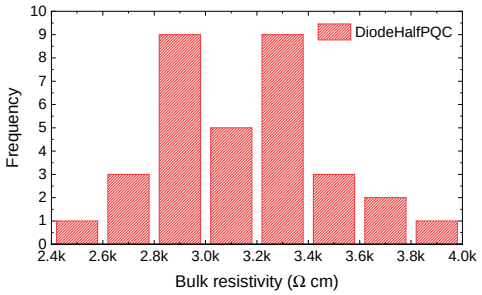
(C) "DiodeQuarter" V_{dp} wafer map.



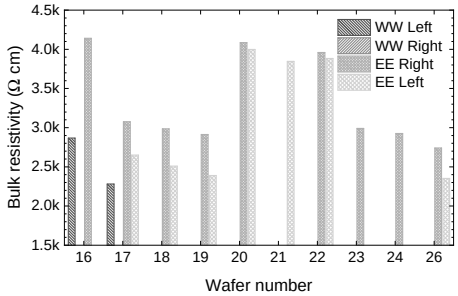
(D) "DiodeHalfPQC" V_{dp} wafer map.



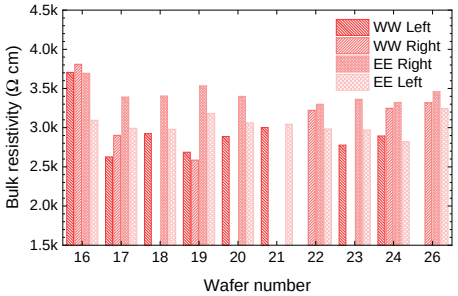
(E) "DiodeQuarter" ρ histogram.



(F) "DiodeHalfPQC" ρ histogram.



(G) "DiodeQuarter" ρ wafer map.



(H) "DiodeHalfPQC" ρ wafer map.

FIGURE 7.7: Outer Tracker Pre-Series PQC: full depletion voltage V_{dp} and bulk resistivity ρ extracted from diode C–V measurements.

fixed oxide charge concentration amounted to $(5.28 \pm 0.22) \times 10^{10}\,\mathrm{cm}^{-2}$ (Figure 7.8d, 7.8e), and an average oxide thickness of $(676 \pm 6)\,\mathrm{nm}$ was obtained (Figure 7.8f, 7.8g).

GCD

I–V characteristics were measured on both structures that are part of the set for automated PQC, "GCDPQC" (Figure 7.9a) and "GCD05" (Figure 7.9b). To shield the measurement from high currents introduced via the opened edge ring and to better define the effective diode area, the guard ring was kept on ground potential and negative bias voltage was applied at the device backplane (compare Figure 6.24b). The measured currents are displayed inverted in Figure 7.9a and 7.9b to improve readability.

The results were largely uniform for all wafers, and the measured currents were low (i.e. $\sim 1\,\mathrm{pA}$). Measurements yielded similar results for the surface generation velocity s_g for both GCD types (Figure 7.9c–7.9f), the average over all measurements on all 10 wafers amounting to $s_\mathrm{g} = (1.11 \pm 0.11)\,\mathrm{cm/s}$.

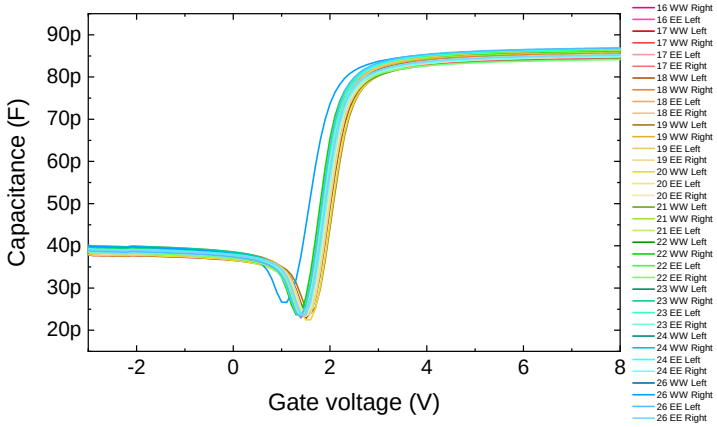
Originally, "GCDPQC", featuring a gate width-to-pitch ratio $w/p = 0.5$, was intended for extraction of s_g, while "GCD05", with $w/p = 0.75$, was intended to facilitate extraction of the bulk generation lifetime τ_g (compare section 6.3.2). However, while both structures worked well for the extraction of s_g, results for τ_g were nonphysical (i.e $\tau_\mathrm{g} < 0$) for both structures. As detailed in section 6.3.2, this effect is attributed to the high generation lifetime of the Pre-Series material ($\sim 100\,\mathrm{ms}$ as estimated from diode J–W characteristics in section 6.1.4). As a result, unscreened surface states at the gate edge in accumulation overshadow the effect of bulk generation under the gate in inversion, even if the gate width-to-pitch ratio is increased to $w/p = 0.75$. To gain an estimate of τ_g from GCD measurements, structures with $w/p \gg 0.75$ would be required. However, even if no absolute value of τ_g could be determined from GCD measurements, the fact that the current in inversion is smaller than the current in accumulation indicates a comparably high value for τ_g. Consequently, the shape of measured GCD characteristics in combination with the extracted value of s_g can be utilized as a qualitative indicator for the magnitude of the bulk generation lifetime.

Van-der-Pauw Structures

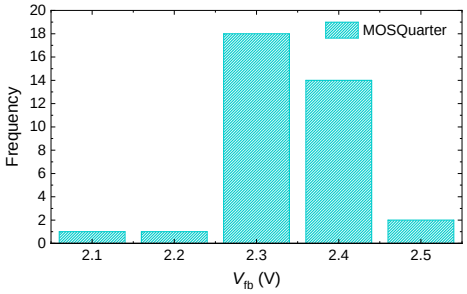
The sheet resistances of the n^+ (Figure 7.10a and 7.10b), p-stop (Figure 7.10c and 7.10d), polysilicon (Figure 7.10e and 7.10f), and p^+ layer (Figure 7.10g and 7.10h) were extracted from measurements of van-der-Pauw cross structures in flutes "PQC1" and "PQC3" for all 10 wafers. Results were generally very uniform, finding $R_{\mathrm{sh},\,n^+} = (36.1 \pm 0.9)\,\Omega/\mathrm{sq}$, $R_{\mathrm{sh},\,p\text{-stop}} = (19.29 \pm 0.35)\,\mathrm{k}\Omega/\mathrm{sq}$, $R_{\mathrm{sh,\,poly}} = (2.43 \pm 0.11)\,\mathrm{k}\Omega/\mathrm{sq}$, and $R_{\mathrm{sh},\,p^+} = (1.36 \pm 0.05)\,\mathrm{k}\Omega/\mathrm{sq}$. One notable outlier was observed for the polysilicon sheet resistance in one measurement on wafer no. 22. A distinct dependence of the p-stop sheet resistance on the location on the wafer, as was observed for earlier Hamamatsu 2S prototypes *VPX28442* (see section 6.4.1 and Figure 6.28a), was not confirmed for the Pre-Series batch.

Measurements of the metal cloverleaf van-der-Pauw structure included in flute "PQC3" produced no reliable results with the setup in Vienna. This issue was attributed to measurement uncertainties at the expected low voltages and the influence of the probe needle contact resistance. The initially implemented measurement procedure attempted to limit the measurement current and utilized a current scan from $-10\,\mathrm{mA}$ to $10\,\mathrm{mA}$ with a current step of $500\,\mu\mathrm{A}$. Assuming an aluminum sheet resistance on the order of $10\,\mathrm{m}\Omega/\mathrm{sq}$, the measured voltages are on the order of $10\,\mu\mathrm{V}$ with this setting and measurement errors dominate the result. A scan range from $-100\,\mathrm{mA}$ to $100\,\mathrm{mA}$ would mitigate these effects by only requiring a voltage resolution on the order of $100\,\mu\mathrm{V}$. This assumption is supported by the results obtained at other PQC test centers. Utilizing a current scan from $-100\,\mathrm{mA}$ to $100\,\mathrm{mA}$ with a $5\,\mathrm{mA}$ step, test centers at Brown University and INFN Perugia found $R_{\mathrm{sh,\,alu}} = (20.3 \pm 0.2)\,\mathrm{m}\Omega/\mathrm{sq}$ for the Outer Tracker Pre-Series. Consequently, for future measurements of the aluminum cloverleaf van-der-Pauw structure at the PQC setup in Vienna, a current scan range of $-100\,\mathrm{mA}$ to $100\,\mathrm{mA}$ is recommended.

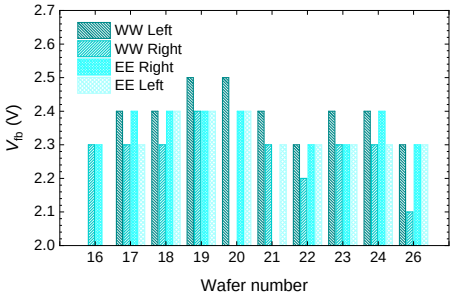
In addition to setting an appropriate current range, care must be taken to establish proper contact between the van-der-Pauw structure and all four probe needles. Particularly, for structures with low sheet resistance such as the aluminum layer, the contact resistance can affect the measurement result. If the contact pressure between probe card and metal pads was



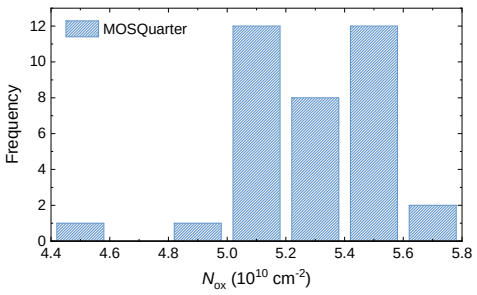
(A) "MOSQuarter" C–V.



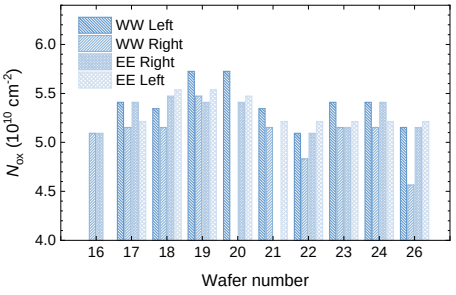
(B) "MOSQuarter" V_{fb} histogram.



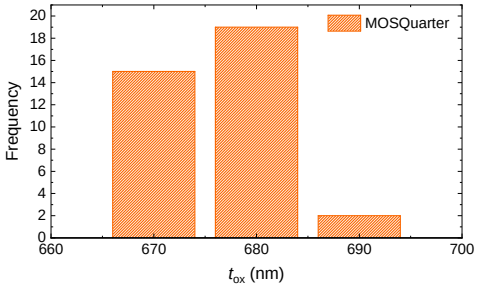
(C) "MOSQuarter" V_{fb} wafer map.



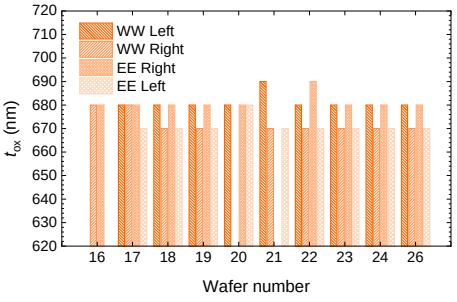
(D) "MOSQuarter" N_{ox} histogram.



(E) "MOSQuarter" N_{ox} wafer map.

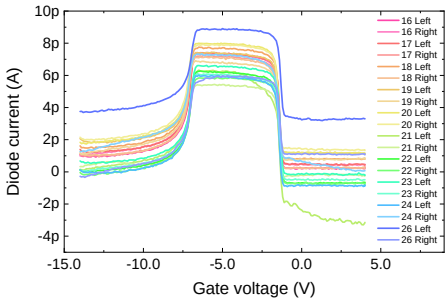


(F) "MOSQuarter" t_{ox} histogram.

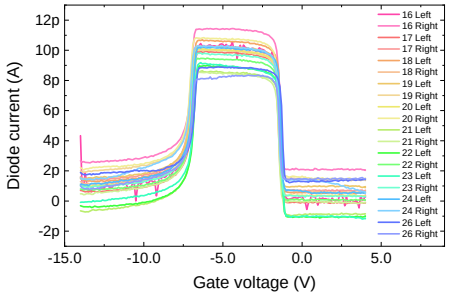


(G) "MOSQuarter" t_{ox} wafer map.

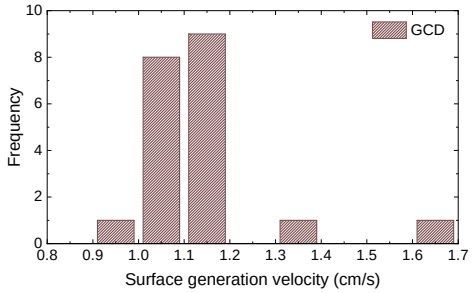
FIGURE 7.8: Outer Tracker Pre-Series PQC: flatband voltage V_{fb}, fixed oxide charge concentration N_{ox}, and oxide thickness t_{ox} extracted from MOS-C C–V measurements.



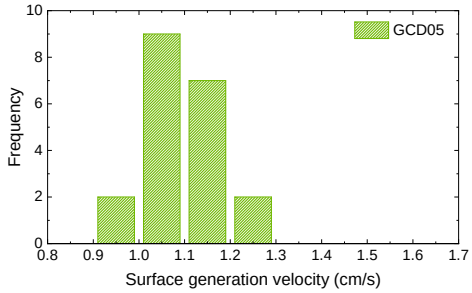
(A) "GCDPQC" I–V.



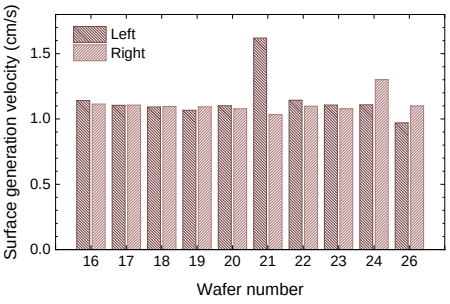
(B) "GCD05" I–V.



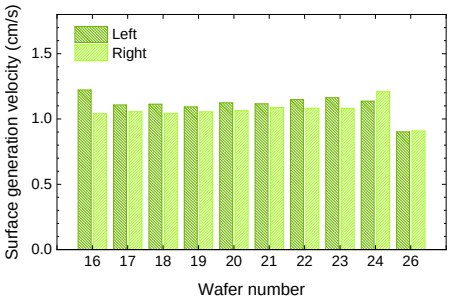
(C) "GCDPQC" s_g histogram.



(D) "GCD05" s_g histogram.

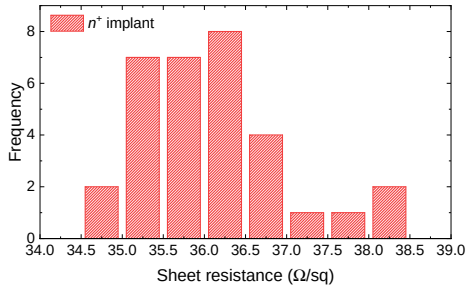


(E) "GCDPQC" s_g wafer map.

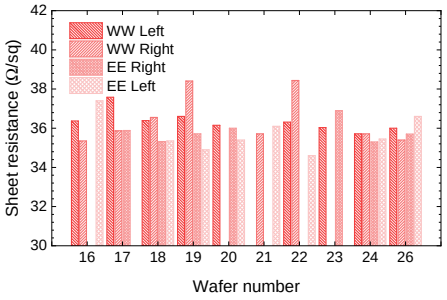


(F) "GCD05" s_g wafer map.

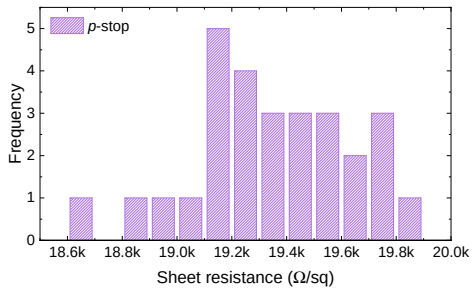
FIGURE 7.9: Outer Tracker Pre-Series PQC: surface generation velocity s_g extracted from GCD measurements on the eastern (EE) "halfmoon" cutoff of each wafer.



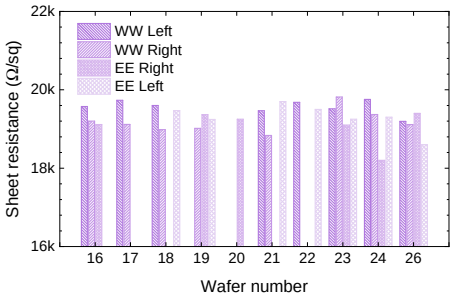
(A) R_{sh} n^+ implant histogram.



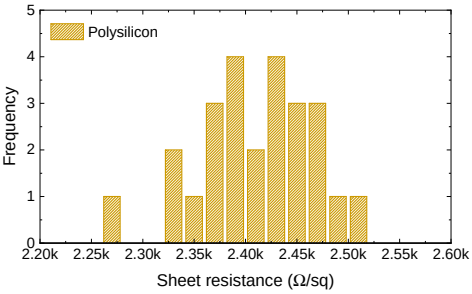
(B) R_{sh} n^+ implant wafer map.



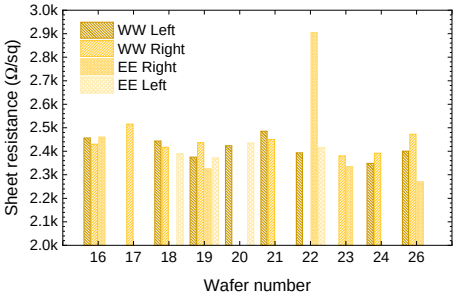
(C) R_{sh} p-stop histogram.



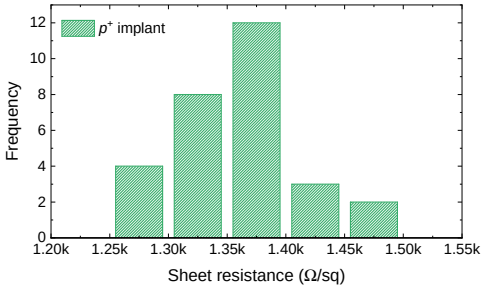
(D) R_{sh} p-stop wafer map.



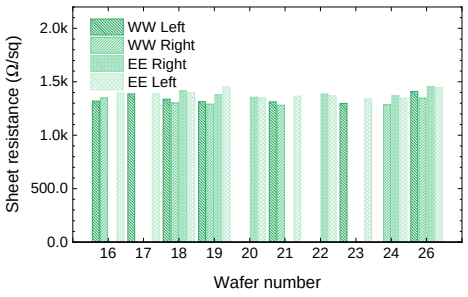
(E) R_{sh} polysilicon histogram.



(F) R_{sh} polysilicon wafer map.



(G) R_{sh} p^+ implant histogram.



(H) R_{sh} p^+ implant wafer map.

FIGURE 7.10: Outer Tracker Pre-Series PQC: n^+, p-stop, polysilicon, and p^+ sheet resistance R_{sh} extracted from van-der-Pauw measurements.

kept low – close to lift-off of the needles – aluminum sheet resistances as high as $\sim 30\,\Omega/\mathrm{sq}$ were measured with the setup in Vienna.

On the other hand, the contact pressure of the probe card should not be chosen too high because the overdrive can cause damage to the probe needles and amount to a shifting of the original needle positions. At the end of Outer Tracker Pre-Series PQC, a visible inward shift of the probe card needles was observed compared to the status before the start of serial testing, suggesting an issue with the contact pressure. The shift of the probe needles was significant enough that it became increasingly difficult to establish a reliable contact of all 20 flute pads. PQC tests of n^+ and p-stop van-der-Pauw structures on HGCAL LD 2019 wafers, which were attempted after Outer Tracker Pre-Series PQC, largely showed unreliable results with non-ohmic current-voltage characteristics, supporting the assumption that the previously observed shift of the probe needles critically affected the four-terminal measurements. Further optimization of the contact pressure and the handling of the measurement setup in Vienna will be necessary to achieve reliable results in future four-terminal measurements.

The line width of the n^+ (Figure 7.11a and 7.11b), p-stop (Figure 7.11c and 7.11d), and p^+ implant (Figure 7.11e and 7.11f) was measured on the line width structures of flute "PQC2" and the van-der-Pauw cross-bridge of flute "PQC3". In case of the p-stop line width structure, a two-terminal measurement was applied because it was found to produce more reliable results (compare section 6.4.2 and Figure 6.28b). All other measurements utilized a standard four-terminal technique. The measured line widths were generally between $3\,\mu\mathrm{m}$ and $7\,\mu\mathrm{m}$ larger than the design line width of $33\,\mu\mathrm{m}$, suggesting some additional lateral dopant diffusion during wafer processing.

Meander

Measurements of the polysilicon meander of flute "PQC2" (Figure 7.12a and 7.12b), which was designed to mirror the bias resistors of AC-coupled strip sensors, yielded an average bias resistance of $(1.91 \pm 0.17)\,\mathrm{M}\Omega$. With a polysilicon sheet resistance of $(2.43 \pm 0.11)\,\mathrm{k}\Omega/\mathrm{sq}$ as extracted from van-der-Pauw measurements, and considering the contact resistance of $(111.5 \pm 43.4)\,\mathrm{k}\Omega$ extracted from CBKR measurements, an approximate number of 740 squares was calculated for the polysilicon resistor. In comparison with the design value of 476 squares, this results translates to a line width of $3.2\,\mu\mathrm{m}$ of the polysilicon resistor instead of $5\,\mu\mathrm{m}$ as designed.

For the metal meander of flute "PQC3", an average resistance of $(416 \pm 37)\,\Omega$ was measured (Figure 7.12c and 7.12d). In combination with an aluminum sheet resistance of $(20.3 \pm 0.2)\,\mathrm{m}\Omega/\mathrm{sq}$, this result amounts to $20\,800$ squares instead of the designed $12\,853$ squares. Consequently, a meander line width of $6\,\mu\mathrm{m}$ instead of $10\,\mu\mathrm{m}$ was estimated.

Four-terminal Resistivity Test Structures

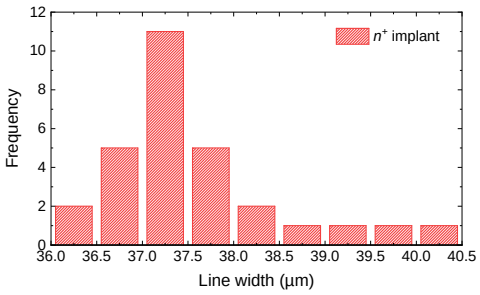
With the PQC setup in Vienna, a bulk resistivity of $(7.0 \pm 0.3)\,\mathrm{k}\Omega$ was measured on the van-der-Pauw type four-terminal structures of flute "PQC3" (Figure 7.13a and 7.13b). This result deviates from the bulk resistivity obtained from diode C–V measurements roughly by a factor 2 (Figure 7.13c). Measurements of the same structure at other test centers, in contrast, yielded results close to diode C–V measurements (Figure 7.13d). These observations indicate that the discrepancy observed in Vienna is likely due to setup related problems such as the current range chosen for the measurement.

MOSFET

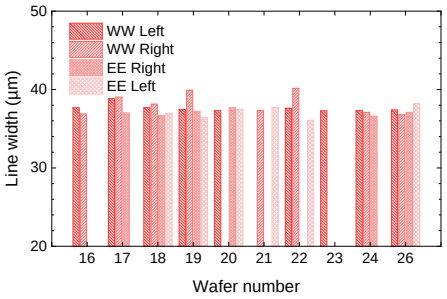
Measurements of MOSFET transfer characteristics on flute "PQC1" yielded an average threshold voltage of $(4.43 \pm 0.08)\,\mathrm{V}$ (Figure 7.14). This high value indicates a satisfactory inter-channel resistance.

Capacitor with Implant

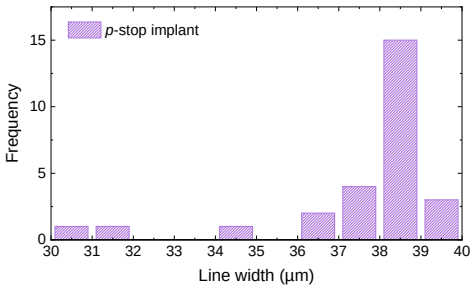
Measurements of capacitors with n^+ implant included in flute "PQC1", yielded an average capacitance of $(2.65 \pm 0.16)\,\mathrm{pF}$ (Figure 7.15a and 7.15b). From this value, the coupling capacitance and the dielectric thickness of the Outer Tracker Pre-Series material were determined



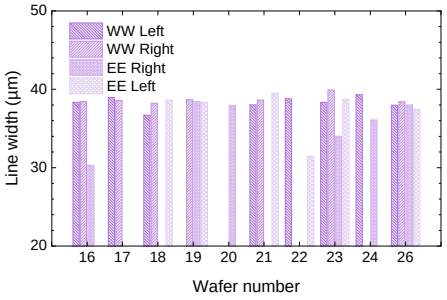
(A) Histogram of n^+ implant line width.



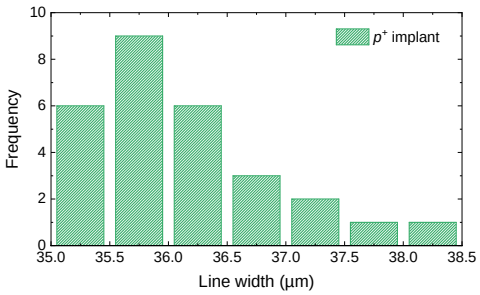
(B) Wafer map of n^+ implant line width.



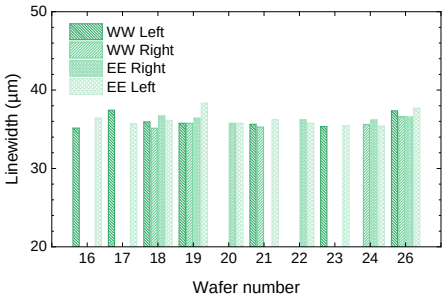
(C) Histogram of p-stop line width.



(D) Wafer map of p-stop line width.

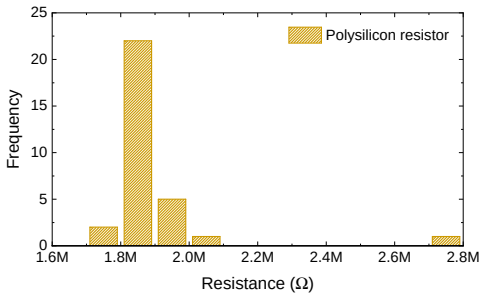


(E) Histogram of p^+ implant line width.

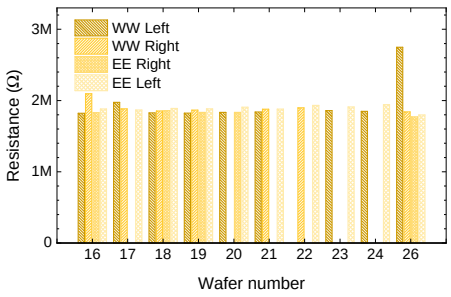


(F) Histogram of p^+ implant line width.

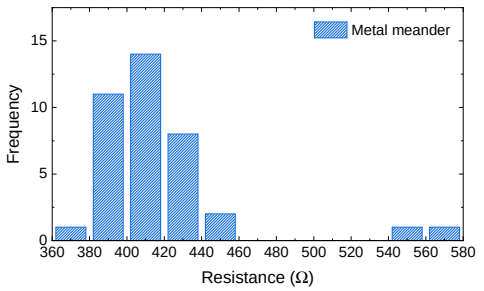
FIGURE 7.11: Outer Tracker Pre-Series PQC: n^+, p-stop, and p^+ line width.



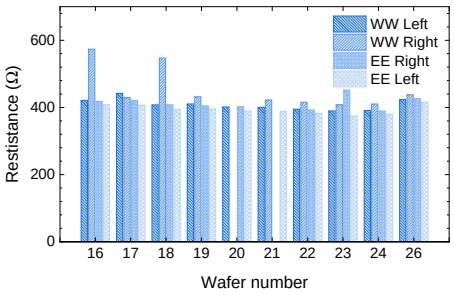
(A) Polysilicon bias resistance histogram.



(B) Polysilicon bias resistance wafer map.

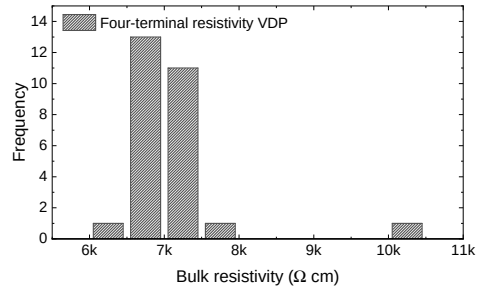


(C) Metal meander resistance histogram.

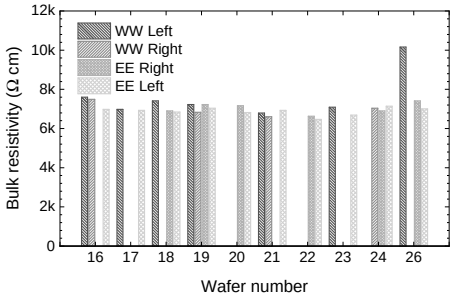


(D) Metal meander resistance wafer map.

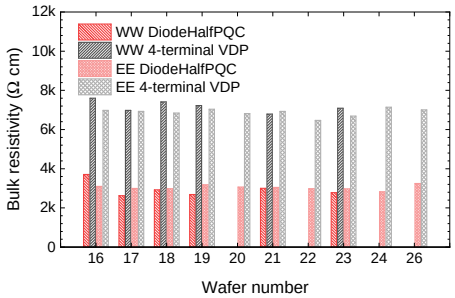
FIGURE 7.12: Outer Tracker Pre-Series PQC: resistance of polysilicon and metal meander structures.



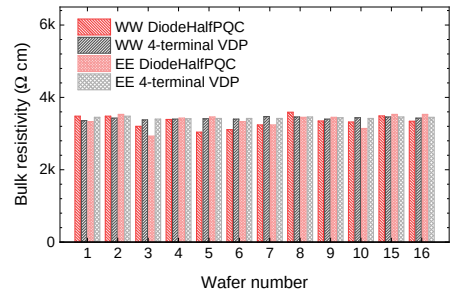
(A) Four-terminal bulk resistivity histogram.



(B) Four-terminal bulk resistivity wafer map.

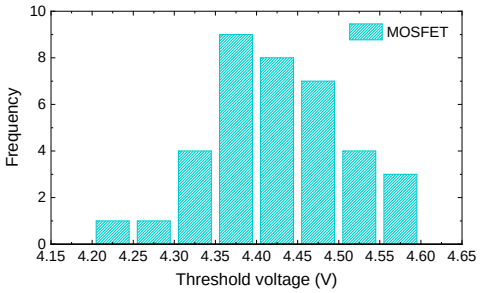


(C) Comparison "DiodeHalfPQC" and four-terminal structure measured in Vienna.

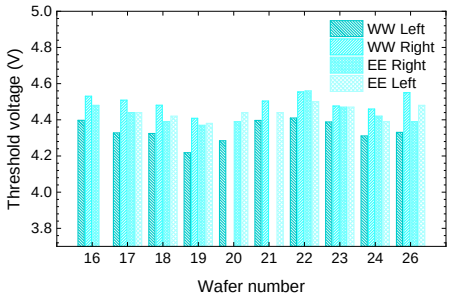


(D) Comparison "DiodeHalfPQC" and four-terminal structure on Outer Tracker *Pre-Production* wafers measured at Brown University.

FIGURE 7.13: Outer Tracker Pre-Series PQC: bulk resistivity ρ extracted from four-terminal resistivity test structures.

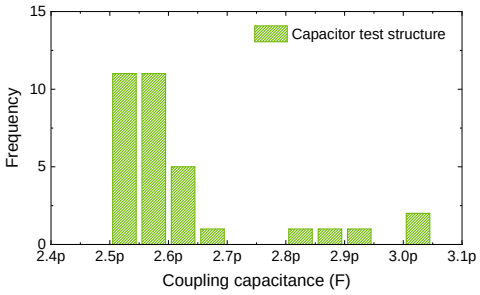


(A) MOSFET threshold voltage histogram.

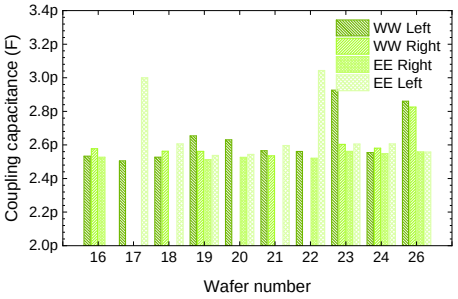


(B) MOSFET threshold voltage wafer map.

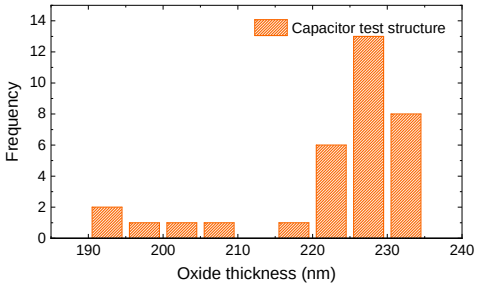
FIGURE 7.14: Outer Tracker Pre-Series PQC: MOSFET threshold voltage.



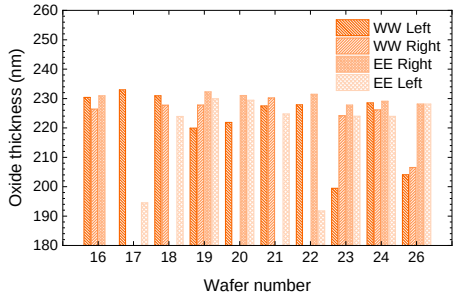
(A) Coupling capacitance histogram.



(B) Coupling capacitance wafer map.



(C) Coupling dielectric thickness histogram.



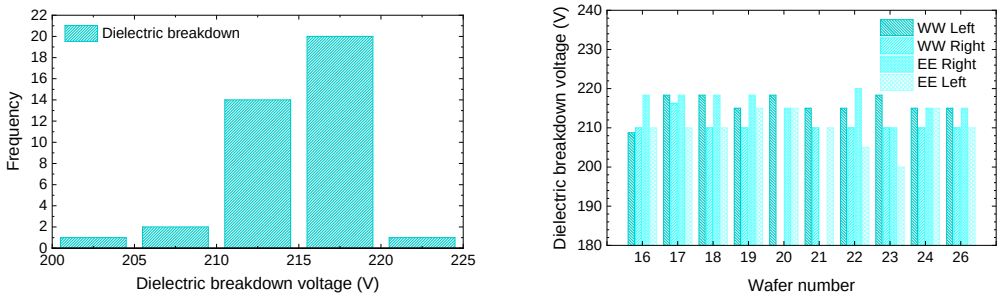
(D) Coupling dielectric thickness wafer map.

FIGURE 7.15: Outer Tracker Pre-Series PQC: coupling capacitance and thickness of the coupling dielectric extracted from capacitors with n^+ implant.

as $(15.86 \pm 0.95)\,\mathrm{nF\,cm^{-2}}$ and $(221 \pm 12)\,\mathrm{nm}$ (Figure 7.15c and 7.15d), respectively, which is well within specifications.

Dielectric Breakdown Test Structures

From measurements of the dielectric breakdown test structures included in flute "PQC2", the average dielectric breakdown voltage of the Outer Tracker Pre-Series material was estimated as $(213 \pm 4)\,\mathrm{V}$ (Figure 7.16). For each measurement, the breakdown voltage was assumed as the voltage at which the current compliance of $100\,\mathrm{nA}$ was reached. The such determined dielectric breakdown voltage lay well within specifications, which define the limit for dielectric breakdown as $V_{\mathrm{bd}} > 150\,\mathrm{V}$.



(A) Dielectric breakdown voltage histogram.

(B) Dielectric breakdown voltage wafer map.

FIGURE 7.16: Outer Tracker Pre-Series PQC: Dielectric breakdown voltage.

CBKR

The contact resistance between n^+ implant and aluminum electrodes and between polysilicon and aluminum was determined using the CBKR structures included in flute "PQC4". For n^+ CBKR structures (Figure 7.17a and 7.17b), the median of the measured contact resistance lay at $26.6\,\Omega$. However, 10 structures showed significantly higher values up to $\sim 350\,\Omega$, amounting to an average of $(66 \pm 75)\,\Omega$. These results may indicate inconsistencies of the general contact quality, an assumption which is supported by the comparably high resistances measured on contact chains (see following section).

The measured contact resistance between polysilicon and aluminum was unexpectedly high. Measurements on CBKR structures yielded an average of $(111.5 \pm 43.4)\,\mathrm{k}\Omega$. Similar to n^+ CBKR structures, a number of distinct outliers with more than twice as high contact resistance were found.

For both types of CBKR structures, the variety and magnitude of the measured contact resistances agreed well with results obtained at other PQC test centers.

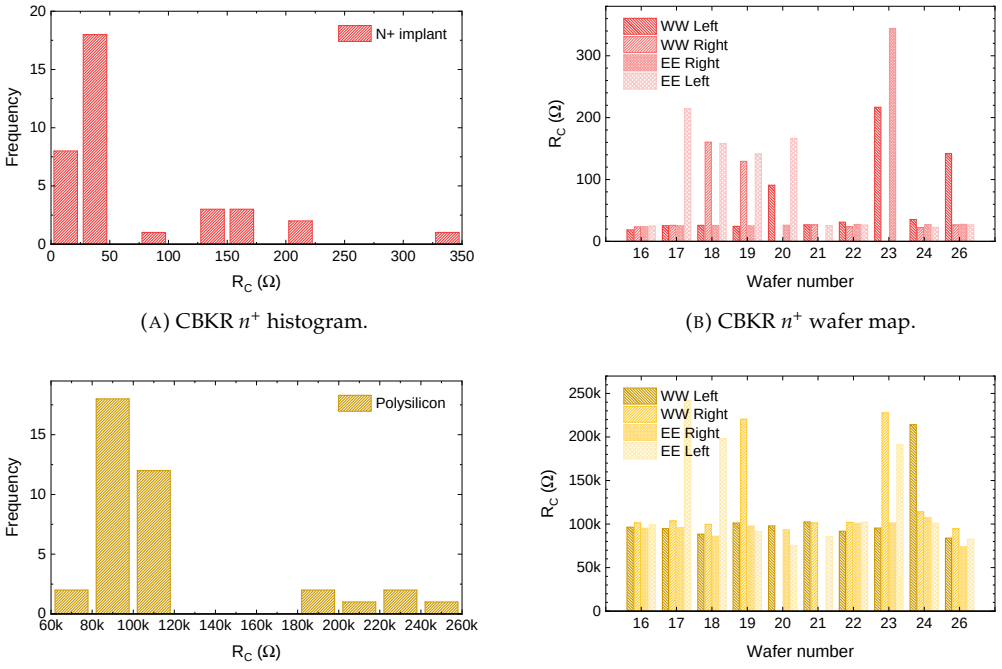
Contact Chains

The resistance of n^+ (Figure 7.18a and 7.18b), p^+ (Figure 7.18c and 7.18d), and polysilicon contact chains (Figure 7.18e and 7.18f) included in flute "PQC4" was measured to estimate the process quality of contacts. The respective average resistances of the full contact chains were $(71.1 \pm 10.6)\,\mathrm{k}\Omega$ for n^+, $(70.2 \pm 1.2)\,\mathrm{k}\Omega$ for p^+, and $(30.3 \pm 2.5)\,\mathrm{M}\Omega$ for polysilicon. While polysilicon results showed a larger overall variation of results, n^+ and p^+ contact chains exhibited a small number of distinct outliers with roughly twice as high resistance than the rest of the measured values. A rough estimate of the expected resistance of contact chains with 228 contacts, taking into account measured values of n^+ and polysilicon contact resistances as well as n^+, polysilicon, and aluminum sheet resistances, is given by

$$R_{\mathrm{cc},\,n^+} = 228 \cdot R_{\mathrm{c},\,n^+} + \frac{228}{2} \cdot 2.5(R_{\mathrm{sh},\,n^+} + R_{\mathrm{sh,\,alu}}) \approx 25\,\mathrm{k}\Omega \quad \text{and} \tag{7.1}$$

$$R_{\mathrm{cc,\,poly}} = 228 \cdot R_{\mathrm{c,\,poly}} + \frac{228}{2} \cdot 2.5(R_{\mathrm{sh,\,poly}} + R_{\mathrm{sh,\,alu}}) \approx 26\,\mathrm{M}\Omega\,. \tag{7.2}$$

While this estimation agrees reasonably well with the value measured for the polysilicon contact chain, the estimate for the n^+ contact chain is lower than the measured value by almost a factor 3. This result coincides with above presented results of n^+ CBKR structures that reported a large variety of the contact resistance between aluminum and n^+ implant. Additionally, considering the similar results for n^+ and p^+ contact chains and taking into account that the measured sheet resistance of the p^+ implant was higher than that of the n^+ implant by almost a factor 40, it can be concluded that the contact resistance between aluminum and p^+ implant is significantly lower than the contact resistance between aluminum and n^+ implant.



(A) CBKR n^+ histogram.

(B) CBKR n^+ wafer map.

(C) CBKR polysilicon histogram.

(D) CBKR polysilicon wafer map.

FIGURE 7.17: Outer Tracker Pre-Series PQC: contact resistance extracted from metal-n^+ and metal-polysilicon CBKR structures.

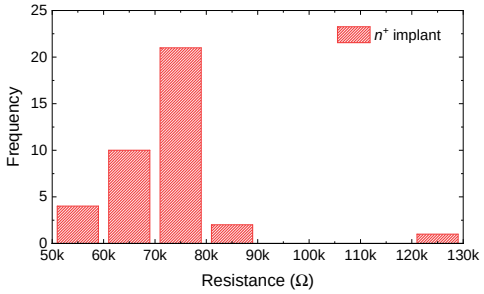
7.3.2 HGCAL Prototypes

First tests of automated PQC were performed on HGCAL LD 2019 and HD 2019 wafers at the setup in Vienna. The wafers feature two different target flatband voltages, active thicknesses $300\,\mu\mathrm{m}$, $200\,\mu\mathrm{m}$, and $120\,\mu\mathrm{m}$, and p-stop configurations individual and common (compare Figure 4.4). Individual wafers are numbered according to "XYnn". The first digit "X" refers to the active thickness; "1" indicates $300\,\mu\mathrm{m}$, "2" corresponds to $200\,\mu\mathrm{m}$, and "3" marks wafers with $120\,\mu\mathrm{m}$ active thickness. The second digit "Y" refers to the p-stop configuration, with "0" indicating p-stop individual and "1" corresponding to p-stop common. The two-digit number "nn", finally, represents the consecutive numbering of individual wafers. All measurements were performed on the test structure set located at the upper-left "halfmoon" cutoff of each wafer (compare Figure 7.4b).

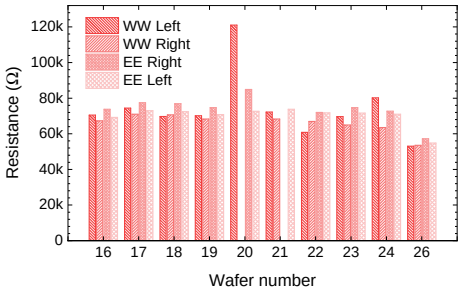
Since prototyping for HGCAL is currently still in progress, the wafers were not subjected to a detailed analysis as was applied for the Outer Tracker Pre-Series, and not all accessible process parameters were investigated. Nonetheless, the following results present a first overview on the quality of the HGCAL material and the variations between the individual process splits.

MOS-C

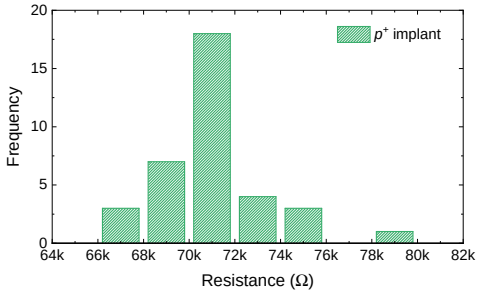
MOS-C C–V characteristics of the HGCAL LD 2019 and HD 2019 material measured on "MOSQuarter" included in flute "PQC1" showed a clear distinction between the process splits with target flatband voltage $2\,\mathrm{V}$ and $5\,\mathrm{V}$ (Figure 7.19). While curves of MOS-C with target flatband voltage $2\,\mathrm{V}$ were very uniform for $300\,\mu\mathrm{m}$ and $200\,\mu\mathrm{m}$ thick wafers, a larger spread was observed for wafers with target flatband voltage $5\,\mathrm{V}$ (Figure 7.19a and 7.19b). The spread within the $5\,\mathrm{V}$ wafers can be attributed to additional process splits varying the p-stop doping concentration and different types of oxide quality. Details about these process variations were not communicated by the vendor. In case of the $120\,\mu\mathrm{m}$ thick wafers (Figure 7.19c), variation was observed for both $2\,\mathrm{V}$ and $5\,\mathrm{V}$ target flatband voltages. The observed shifting of MOS-C characteristics for certain wafers correlates with a process split in which the p-stop doping concentration was varied. It seems interesting to note that, even



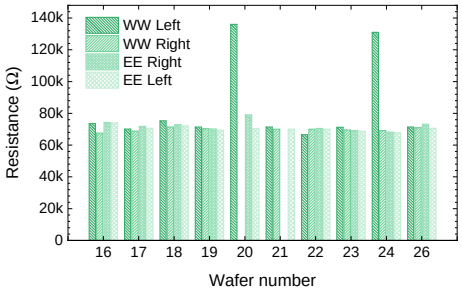
(A) Contact chain n^+ histogram.



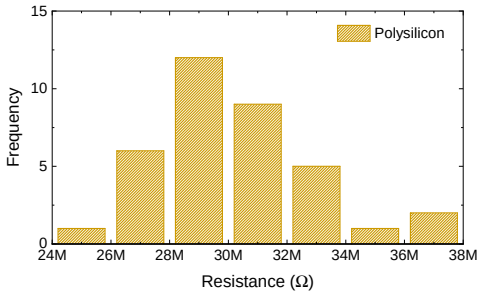
(B) Contact chain n^+ wafer map.



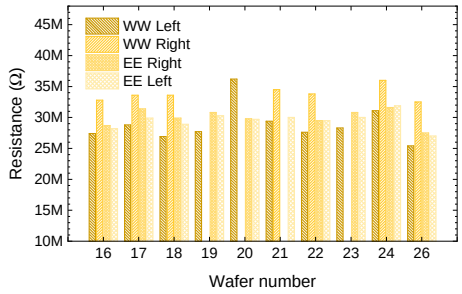
(C) Contact chain p^+ histogram.



(D) Contact chain p^+ wafer map.

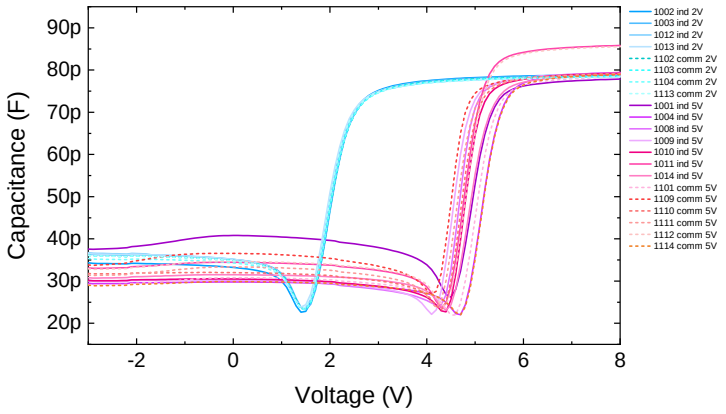


(E) Contact chain polysilicon histogram.

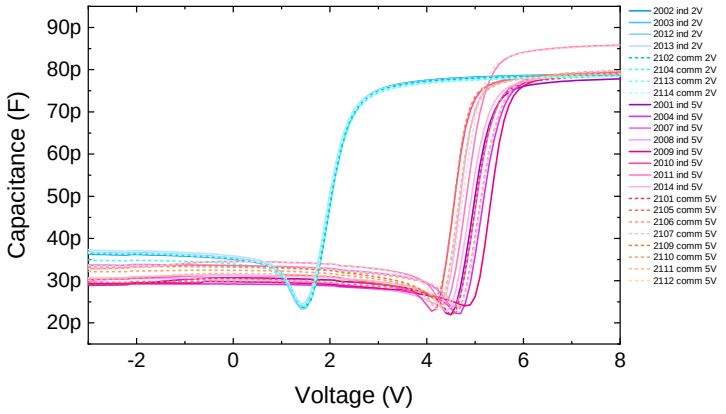


(F) Contact chain polysilicon wafer map.

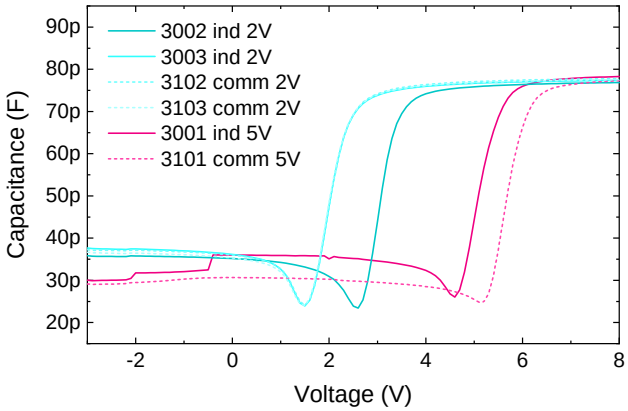
FIGURE 7.18: Outer Tracker Pre-Series PQC: n^+, p^+, and polysilicon contact chain resistance.



(A) "MOSQuarter" C–V of 300 µm float-zone wafers.

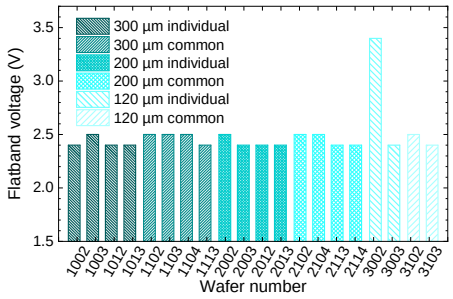


(B) "MOSQuarter" C–V of 200 µm float-zone wafers.

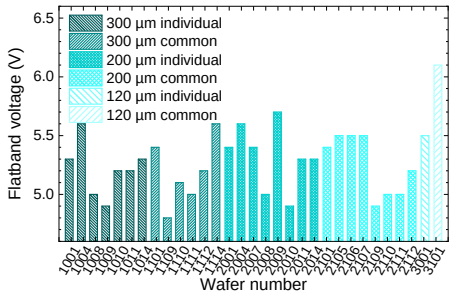


(C) "MOSQuarter" C–V of 120 µm epitaxial wafers.

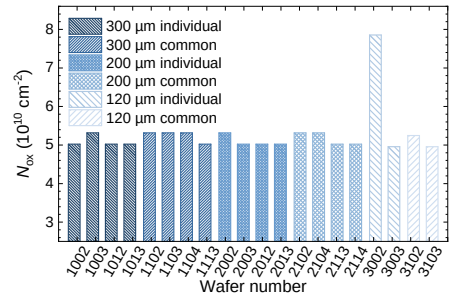
FIGURE 7.19: PQC of HGCAL LD 2019 and HD 2019 prototypes: MOS-C C–V characteristics for 300 µm, 200 µm, and 120 µm thick wafers with individual and common p-stop configuration.



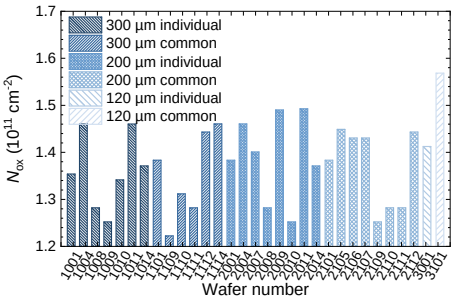
(A) "MOSQuarter" V_{fb} wafer map (target $V_{\mathrm{fb}} = 2\,\mathrm{V}$).



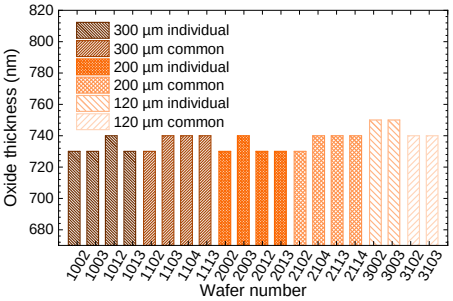
(B) "MOSQuarter" V_{fb} wafer map (target $V_{\mathrm{fb}} = 5\,\mathrm{V}$).



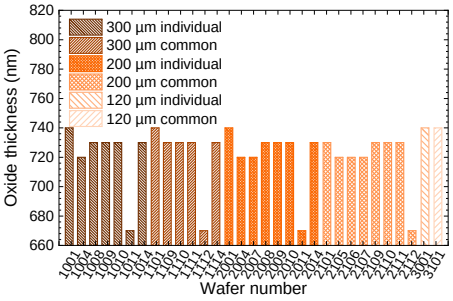
(C) "MOSQuarter" N_{ox} wafer map (target $V_{\mathrm{fb}} = 2\,\mathrm{V}$).



(D) "MOSQuarter" N_{ox} wafer map (target $V_{\mathrm{fb}} = 5\,\mathrm{V}$).



(E) "MOSQuarter" t_{ox} wafer map (target $V_{\mathrm{fb}} = 2\,\mathrm{V}$).

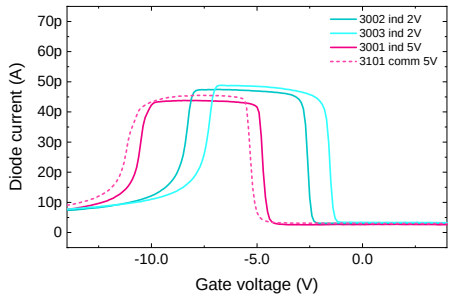


(F) "MOSQuarter" t_{ox} wafer map (target $V_{\mathrm{fb}} = 5\,\mathrm{V}$).

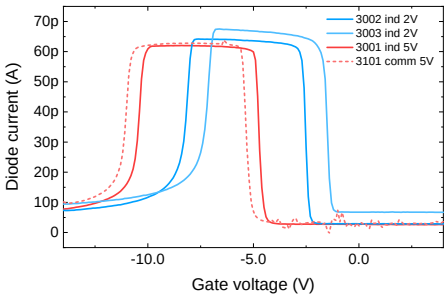
FIGURE 7.20: PQC of HGCAL LD 2019 and HD 2019 prototypes: flatband voltage V_{fb}, fixed oxide charge concentration N_{ox}, and oxide thickness t_{ox} extracted from MOS-C C–V measurements of wafers with individual and common p-stop configuration and target flatband voltage 2 V and 5 V.

though the MOS-C test structures do not include any p-stop implantation, process variations affecting the p-stop doping concentration still had an impact on MOS-C flatband voltage.

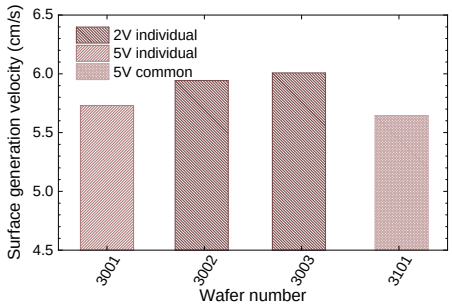
For material with target flatband voltages of 2 V and 5 V, respectively, average flatband voltages of $(2.5 \pm 0.2)\,\mathrm{V}$ and $(5.3 \pm 0.3)\,\mathrm{V}$ (Figure 7.20a and 7.20b) corresponding to fixed oxide charge concentrations of $(5.27 \pm 0.61) \times 10^{10}\,\mathrm{cm}^{-2}$ and $(1.38 \pm 0.09) \times 10^{11}\,\mathrm{cm}^{-2}$ (Figure 7.20c and 7.20d) were found. Similarly, oxide thicknesses were largely very uniform for all wafers, amounting to $(737 \pm 6)\,\mathrm{nm}$ for the 2 V wafers and $(730 \pm 6)\,\mathrm{nm}$ for the 5 V wafers (Figure 7.20e and 7.20f). The latter value excludes wafers 1011, 1112, 2011, and 2112, which all featured a lower oxide thickness of 670 nm. All four wafers were subjected to a process variation targeting the oxide quality, labeled "Type E" by the manufacturer. It can be concluded that this particular process variation affected either the physical thickness or the relative permittivity of the oxide compared to the other process variations.



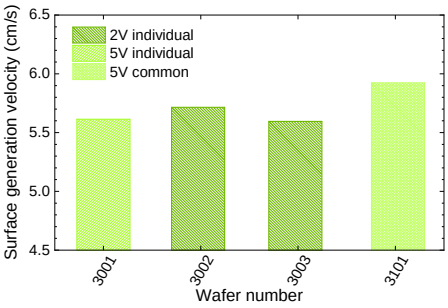
(A) "GCD" I–V.



(B) "GCD05" I–V.

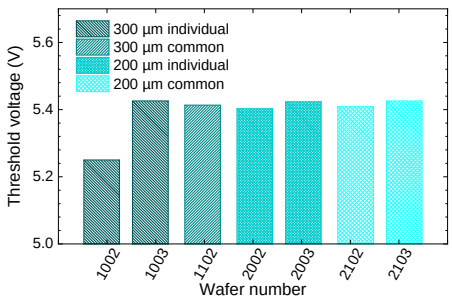


(C) "GCD" s_g wafer map.

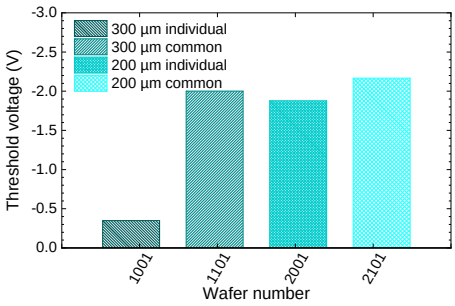


(D) "GCD05" s_g wafer map.

FIGURE 7.21: PQC of HGCAL HD 2019 prototypes: surface generation velocity s_g extracted from GCD measurements of wafers on $120\,\mu m$ thick wafers with individual and common p-stop configuration and target flatband voltage $2\,V$ and $5\,V$.



(A) MOSFET threshold voltage wafer map (target $V_{fb} = 2\,V$).



(B) MOSFET threshold voltage wafer map (target $V_{fb} = 5\,V$).

FIGURE 7.22: HGCAL LD 2019 PQC: MOSFET threshold voltage V_{th} of $300\,\mu m$ and $200\,\mu m$ thick wafers with individual and common p-stop configuration and target flatband voltage $2\,V$ and $5\,V$.

GCD

Measurements of GCD I–V characteristics were performed for HGCAL HD 2019 wafers on the structures labeled "GCDPQC" and "GCD05" included in flutes "PQC2" and "PQC4" (Figure 7.21). The extracted surface generation velocity was similar in all cases, for both $2\,V$ and $5\,V$ target flatband voltages, amounting to $(5.77 \pm 0.15)\,cm/s$ on average. This value is notably larger by about a factor 5 than the value found for the Outer Tracker Pre-Series material, indicating distinct differences of the respective production processes that affect the quality of the Si-SiO_2 interface.

MOSFET

Transfer characteristics measured on the MOSFET test structures included in flute "PQC1" for HGCAL LD 2019 wafers exhibited distinctly different threshold voltages depending on the target flatband voltage of the respective wafers (Figure 7.22). While the average threshold voltage of the $2\,\mathrm{V}$ wafers was $(5.4 \pm 0.1)\,\mathrm{V}$, negative threshold voltages of $(-1.6 \pm 0.7)\,\mathrm{V}$ on average were measured on $5\,\mathrm{V}$ wafers. By comparing these results to earlier results measured on Infineon PS-s prototype wafers and published in [15], the negative threshold voltages of the $5\,\mathrm{V}$ material might indicate insufficient inter-channel isolation. However, direct measurements of the inter-cell resistance on the respective wafers will be necessary to verify this assumption. Additionally, as is evident from the data of the $5\,\mathrm{V}$ wafers, the threshold voltage measured for *p*-stop common configuration was consistently lower than the threshold voltage measured for *p*-stop individual, indicating a generally higher inter-channel resistance for the *p*-stop individual configuration.

CHAPTER 8

SUMMARY AND OUTLOOK

8.1 Silicon Sensor Quality Assurance for the CMS Phase-2 Upgrade

With the Large Hadron Collider (LHC) at CERN about to embark into an era of high luminosity in 2027, LHC experiments are preparing to meet the challenges of the new High Luminosity LHC (HL-LHC). The high luminosity environment entails an average pileup of 140 events (200 for the ultimate luminosity scenario) and unprecedented radiation levels of $2.3 \times 10^{16}\,\mathrm{n_{eq}/cm^2}$ and a total ionizing dose of $12\,\mathrm{MGy}$ in the center of the CMS detector at $3000\,\mathrm{fb}^{-1}$ integrated luminosity [33]. These conditions put forward stringent constraints on detector resolution and radiation tolerance. To meet these requirements, various subdetectors of the CMS experiment – most notably, the CMS Tracker and the Endcap Calorimeter – will undergo an extensive upgrade during the third long shutdown (LS3) of the LHC, scheduled to start in 2025. This upgrade is generally referred to as the CMS Phase-2 Upgrade.

By the end of LHC Run 3 in 2024 (i.e. immediately before LS3), the CMS Tracker will have reached the end of its designated lifetime and will no longer be able to operate without significant efficiency loss. Consequently, the full tracker volume will be replaced during LS3. The new tracker will feature an improved layout, a new module design in compliance with the level-1 trigger, reduced material budget, and extended coverage in the forward region [33]. Similarly, the CMS Endcap Calorimeter will not remain functional after an integrated luminosity of $500\,\mathrm{fb}^{-1}$ and will be replaced completely by the new High Granularity Calorimeter (HGCAL). HGCAL will offer unprecedented transverse and longitudinal granularity, timing precision, and the ability to contribute to the level-1 trigger decision [37].

The full volume of the CMS Tracker and parts of HGCAL will utilize silicon sensors as active material. For the combined upgrades of these detector parts, over $50\,000$ silicon sensors will be manufactured between 2020 and 2023. CMS employs a dedicated quality assurance plan to ensure that the delivered sensor material complies with specifications and will operate well under high irradiation conditions. The strategy relies on three main quality control mechanisms: sensor quality control (SQC), process quality control (PQC), and irradiation tests. While SQC measures a set of qualification parameters on a limited number of sensors, PQC tracks critical process parameters on dedicated test structures. Parameters extracted from test structure measurements include parameters that cannot be accessed directly on the main sensors and parameters requiring destructive measurements.

8.2 Studies of Test Structure Functionalities

In this thesis, I have laid out the basis for the PQC strategy of the CMS Outer Tracker and HGCAL silicon sensor series productions for the CMS Phase-2 Upgrade. To this end, I conducted extensive electrical measurements on a large variety of test structures produced by the semiconductor manufacturers Hamamatsu Photonics and Infineon Technologies and performed computer simulations to investigate the response of test structure properties

to the variation of characteristic process parameters. The studied test structures were, in part, adapted from previous designs for the current CMS Tracker [58] and, to another part, included well-established standard test structures and structures newly developed for the requirements of high energy physics silicon sensor quality assurance. These test structures include diodes, metal-oxide-semiconductor capacitors (MOS-C), gate-controlled diodes (GCD), van-der-Pauw type structures and meander structures for sheet resistance measurements, four-terminal structures to measure the silicon bulk resistivity, metal-oxide-semiconductor field-effect transistor (MOSFET) test structures to probe the isolation properties between neighboring sensor channels, cross-bridge Kelvin resistors (CBKR) to determine contact resistances, contact chains to assess the overall quality of contacts, test structures to measure the breakdown voltage of the coupling dielectric and the coupling capacitance, a structure to determine the misalignment of lithography masks, and structures intended for spreading resistance profiling (SRP) and secondary ion mass spectrometry (SIMS).

Particular concern was put on assessing the capability of different test structures to determine the same process parameter. The aim was to establish complementary parameter extraction methods as part of the PQC procedure. The most important results are summarized in the following:

- The conducted studies confirmed that bulk leakage current vs. depletion width (J–W) characteristics of diodes and current-voltage (I–V) characteristics of GCDs can be used to extract the bulk generation lifetime τ_{g}. Both methods yielded comparable results on the investigated wafers. However, particularly for material with high τ_{g}, measurements on GCDs may yield nonphysical results (i.e. $\tau_{\mathrm{g}} < 0$). This effect is caused by unscreened surface states at the gate edge in accumulation that contribute a larger current component than the bulk generation current under the gate in inversion [95]. Consequently, the current in accumulation is higher than the current in inversion and the value for τ_{g} becomes nonphysical. To mitigate this effect, the design of GCDs can be adapted by increasing the ratio of gate to diode area or, equivalently, the width-to-pitch ratio of the gate fingers.

- To provide an alternative to diode capacitance-voltage (C–V) measurements, I studied different methods to determine the bulk resistivity ρ or, equivalently, the bulk carrier density N_{A} of the wafer material. The values of N_{A} extracted from the slope of MOS-C $1/C^2$ vs. V characteristics in the depletion regime were in good agreement with those extracted from diode C–V characteristics on the same wafers. The MOS-C slope in depletion allows to determine an estimate of the carrier density near the surface of the semiconductor, which is especially useful to assess different types of spray implantations. Additionally, bulk resistivity values comparable to those extracted from diode C–V measurements were obtained using simple resistance measurements on dedicated four-terminal test structures. The measurement results from these four-terminal structures need to be corrected for sample thickness and probe placement to achieve an accurate estimate of ρ. The main advantage of MOS-C and four-terminal methods compared to diode C–V characteristics is that they do not require high voltage ramps.

- I investigated the capability of MOSFET test structures to assess sensor inter-channel properties. Building on results published in [67] and [99] that indicated the sensitivity of MOSFET threshold voltage to p-stop doping concentration and implantation depth, I demonstrated the qualitative relationship of MOSFET threshold voltage and sensor inter-channel resistance [15]. Consequently, it is established that MOSFET test structures provide a simple tool to detect process related variations of p-stop properties that affect sensor inter-channel resistance and will be employed during CMS PQC [13].

8.3 A Test Structure Set for Automated PQC

Building on the results obtained from test structure measurements and simulations, I developed a new set of test structures optimized for automated assessment of a comprehensive set of process parameters during CMS PQC. In combination with a 20-needle probe card for contacting and a switching system, the set allows an initial evaluation of the most important

process parameters in about 30 minutes per wafer. The set constitutes the basis for Outer Tracker and HGCAL PQC and will be implemented on all current and future Outer Tracker and HGCAL production wafers.

Following the development of the test structure set and the commissioning of the corresponding measurement setup in the cleanroom of HEPHY Vienna, I evaluated the first measurement results obtained on the newly produced test structure set on the Outer Tracker *Pre-Series* wafer batch and the HGCAL *LD 2019* and *HD 2019* prototype batches. The conclusions drawn from these measurements can be divided in *material related results*, including process related differences of Outer Tracker and HGCAL wafers, and results relating to the general *behavior and functionality* of the test structures included in the set.

Regarding the *quality of the delivered material* and observed specifics for Outer Tracker and HGCAL wafers, the following main conclusions can be drawn:

- PQC results of the Outer Tracker Pre-Series batch proved a satisfactory quality of the wafer material and found process parameters complying well with predefined limits.
- Diode C–V measurements on Outer Tracker Pre-Series wafers, particularly those conducted on the smaller "DiodeQuarter", displayed a soft dependency on the location of the measured structure on the wafer. Structures located on the western "halfmoon" cutoff were more likely to yield characteristics differing strongly from the expected $1/C^2$ vs. V behavior, whereas measurements of structures located on the eastern cutoff were more likely to exhibit reliable characteristics that allowed extraction of the full depletion voltage. The reason for this discrepancy and whether it is related to process variations across the wafer area is not clear. However, the effect of irregular C–V characteristics is likely related to high peripheral currents introduced via an opened edge ring and capacitive coupling of surrounding structures.
- The dependency of the *p*-stop sheet resistance on the location on the wafer, which had been observed for wafers of earlier Outer Tracker prototype runs [13], was not confirmed on Outer Tracker Pre-Series wafers.
- Earlier HGCAL prototype wafers of the LD 2018 run exhibited an, on average, three times higher fixed oxide charge concentration N_{ox} than Outer Tracker prototypes [13]. This issue was addressed in subsequent HGCAL prototype runs LD 2019 and HD 2019, and two different types of wafers with target flatband voltages $2\,\text{V}$ and $5\,\text{V}$ were produced. N_{ox} extracted from wafers with a target value of $2\,\text{V}$ agreed well with the average value of N_{ox} found for the Outer Tracker Pre-Series material.
- The surface generation velocity extracted from GCD measurements was larger by about a factor five for epitaxial HGCAL HD 2019 wafers than the value found for Outer Tracker Pre-Series wafers, indicating distinct differences of the respective production processes that affect the quality of the Si-SiO_2 interface.
- Measurements of MOSFET test structures on HGCAL LD 2019 wafers with target flatband voltage $5\,\text{V}$ indicated a generally higher inter-channel resistance for wafers with the *p*-stop configuration denoted "individual" than for wafers featuring the *p*-stop "common" configuration.

With respect to *behavior and functionality* of individual test structures included in the set for automated PQC, the main results are:

- Test structures included in the set generally function as intended and are able to produce reliable results for all process parameters of interest. A notable exception are I–V measurements on diodes, which displayed issues related to the edge ring design.
- Opened edge rings around diodes and GCDs, which are necessary to allow the routing of metal connections to the "flute" structures for contacting, were found to introduce significant parasitic currents. Consequently, the guard ring of the structures had to be put on ground potential during measurement to draw off the additional currents. However, because the diodes do not feature a *p*-stop implant between diode pad and guard ring, I–V measurements with contacted guard ring yielded unreasonably high currents in the range between $0\,\text{V}$ and $100\,\text{V}$ where diode pad and guard ring are

not isolated from each other. Additionally, in contrast to measurements on regular diodes, all I–V measurements of diodes in the set for automated PQC featured a soft breakdown at about $400\,\mathrm{V}$, making them unsuitable for determining a reliable estimate of the sensor leakage current for the current CMS production, which requires measurements at $600\,\mathrm{V}$.

- Both GCDs included in the set for automated PQC yielded nonphysical results for the generation lifetime τ_g (i.e. $\tau_\mathrm{g} < 0$). This issue is related to the comparatively high value of τ_g ($\sim 100\,\mathrm{ms}$) and the design of the structures. Even though "GCD05" was included with an intentionally high width-to-pitch ratio of $w/p = 0.75$, that value was not sufficient to compensate for the effect of unscreened surface states in accumulation. Consequently, a larger value $w/p \gg 0.75$ would be required to accurately extract τ_g for the investigated wafer material. However, the general fact that for both GCD versions implemented in the set a nonphysical value for τ_g was observed, serves as a compelling indicator toward a comparatively high value of τ_g.

- The line width of the *p*-stop implant extracted from four-terminal measurements of van-der-Pauw cross-bridge and bridge type structures was significantly overestimated if the structures featured an asymmetric contact placement. This effect may be related to the additional p^+ implants that are added below contacts to provide an ohmic contact between metal and semiconductor. Two-terminal measurements of the same structures produced more accurate line width results in agreement with optical measurements using a microscope.

8.4 Outlook

The silicon sensor series production for the CMS Outer Tracker started in 2020 and is scheduled to run until 2023. SQC and PQC results of the Pre-Series batch and subsequent Pre-Production batches showed excellent quality of sensors and wafer material [72].

HGCAL silicon sensor series production is scheduled to start later in 2021. As of now, the final wafer layout is still subject to change, and final decisions have yet to be made regarding the *p*-stop configuration and specifications for the PQC procedure and corresponding parameter limits. The results presented in this thesis will provide valuable input for these decisions.

Additionally, because the wafer design for HGCAL, in contrast to the Outer Tracker, is not yet finalized, it is possible to implement layout changes on future HGCAL wafers that address some of the issues found for the test structure set for automated PQC. These include the following possible adaptations:

- The introduction of additional edge rings around "flutes" featuring diodes may mitigate the effects of parasitic currents that were found to reduce the functionality of the diodes, particularly for I–V measurements. Alternatively, a common edge ring surrounding the entire set of test structures may be introduced.

- A *p*-stop implant between diode pad and guard ring will eliminate the issue of high currents measured in the region between $0\,\mathrm{V}$ and approximately $100\,\mathrm{V}$ when the guard ring is connected to ground. This measure will be particularly beneficial if the effective diode area need be well defined during I–V measurements, e.g., to accurately extract the generation lifetime from diode measurements.

- To facilitate extraction of the generation lifetime from GCD measurements, the width-to-pitch ratio of "GCD05" may be increased.

For the Outer Tracker series production, no layout changes are possible. To mitigate the irregularities of diode measurements related to the opened edge rings, it is recommended to include the larger "DiodeHalfPQC" into the standard PQC procedure because the structure was found to produce more reliable results than the smaller "DiodeQuarter".

PQC of the Outer Tracker and HGCAL series productions will generate a significant amount of data that will be very useful for further in-depth evaluation of test structure functionalities. In particular, the extraction of MOSFET threshold voltage together with

direct measurements of the sensor inter-channel resistance can be used to determine a quantitative relationship between the two parameters.

Over the course of three years of silicon sensor series production, it will be especially important to detect trends that indicate gradual variation of process parameters. Such trends may provide early warnings for potential issues within the production process. For this reason, SQC and PQC results of the ongoing production for the Outer Tracker are monitored and discussed at a weekly basis within the Outer Tracker sensor working group, and a similar procedure may be established for HGCAL.

The PQC strategy developed over the course of this thesis provides a valuable tool to detect issues at an early stage and, thus, ensure the quality of the silicon sensors integrated into the CMS detector. Ultimately, in conjunction with the efforts of thousands of scientists and engineers around the world, this work will contribute a fraction to laying the basis for, hopefully, many exciting physics results within the Standard Model of particle physics and beyond.

List of Figures

List of Tables

Bibliography

[1] J. J. Thomson. "Cathode Rays". In: *The London, Edinburgh, and Dublin Philosophical Magazine and Journal of Science* 44.269 (1897), pp. 293–316. DOI: 10.1080/14786449708621070.

[2] E. Rutherford. "The scattering of alpha and beta particles by matter and the structure of the atom". In: *The London, Edinburgh, and Dublin Philosophical Magazine and Journal of Science* 21.125 (1911), pp. 669–688. DOI: 10.1080/14786440508637080.

[3] J. Chadwick. "The Existence of a Neutron". In: *Proceedings of the Royal Society of London. Series A, Containing Papers of a Mathematical and Physical Character* 136.830 (1932), pp. 692–708. DOI: 10.1098/rspa.1932.0112.

[4] ATLAS Collaboration. "Observation of a new particle in the search for the Standard Model Higgs boson with the ATLAS detector at the LHC". In: *Physics Letters B* 716.1 (2012), pp. 1–29. ISSN: 0370-2693. DOI: 10.1016/j.physletb.2012.08.020.

[5] CMS Collaboration. "Observation of a new boson at a mass of 125 GeV with the CMS experiment at the LHC". In: *Physics Letters B* 716.1 (2012), pp. 30–61. ISSN: 0370-2693. DOI: 10.1016/j.physletb.2012.08.021.

[6] D. Contardo et al. *Technical Proposal for the Phase-II Upgrade of the CMS Detector*. Tech. rep. CERN-LHCC-2015-010. LHCC-P-008. CMS-TDR-15-02. Geneva, 2015. URL: https://cds.cern.ch/record/2020886.

[7] P. W. Higgs. "Broken Symmetries and the Masses of Gauge Bosons". In: *Phys. Rev. Lett.* 13 (16 1964), pp. 508–509. DOI: 10.1103/PhysRevLett.13.508.

[8] F. Englert and R. Brout. "Broken Symmetry and the Mass of Gauge Vector Mesons". In: *Phys. Rev. Lett.* 13 (9 1964), pp. 321–323. DOI: 10.1103/PhysRevLett.13.321.

[9] G. S. Guralnik, C. R. Hagen, and T. W. B. Kibble. "Global Conservation Laws and Massless Particles". In: *Phys. Rev. Lett.* 13 (20 1964), pp. 585–587. DOI: 10.1103/PhysRevLett.13.585.

[10] Apollinari G. et al. *High-Luminosity Large Hadron Collider (HL-LHC): Technical Design Report V. 0.1*. CERN Yellow Reports: Monographs. Geneva: CERN, 2017. DOI: 10.23731/CYRM-2017-004.

[11] ATLAS Collaboration. "The ATLAS Experiment at the CERN Large Hadron Collider". In: *JINST* 3 (2008), S08003. 437 p. DOI: 10.1088/1748-0221/3/08/S08003. URL: https://cds.cern.ch/record/1129811.

[12] CMS Collaboration. "The CMS experiment at the CERN LHC". In: *Journal of Instrumentation* 3.08 (2008), S08004–S08004. DOI: 10.1088/1748-0221/3/08/s08004.

[13] V. Hinger. "Process quality control strategy for the Phase-2 Upgrade of the CMS Outer Tracker and High Granularity Calorimeter". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 982 (2020), p. 164563. ISSN: 0168-9002. DOI: 10.1016/j.nima.2020.164563.

[14] V. Hinger et al. "Process quality control for large-scale silicon sensor productions". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 924 (2019). 11th International Hiroshima Symposium on Development and Application of Semiconductor Tracking Detectors, pp. 38–43. ISSN: 0168-9002. DOI: 10.1016/j.nima.2018.07.082.

[15] V. Hinger et al. "Field effect transistor test structures for inter-strip isolation studies in silicon strip detectors". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 958 (2020). Proceedings of the Vienna Conference on Instrumentation 2019, p. 162233. ISSN: 0168-9002. DOI: 10.1016/j.nima.2019.05.074.

[16] G. Arnison et al. "Experimental observation of isolated large transverse energy electrons with associated missing energy at $s = 540$ GeV". In: *Physics Letters B* 122.1 (1983), pp. 103–116. ISSN: 0370-2693. DOI: 10.1016/0370-2693(83)91177-2.

[17] M. Banner et al. "Observation of single isolated electrons of high transverse momentum in events with missing transverse energy at the CERN pp collider". In: *Physics Letters B* 122.5 (1983), pp. 476–485. ISSN: 0370-2693. DOI: 10.1016/0370-2693(83)91605-2.

[18] G. Arnison et al. "Experimental observation of lepton pairs of invariant mass around 95 GeV $/c^2$ at the CERN SPS collider". In: *Physics Letters B* 126.5 (1983), pp. 398–410. ISSN: 0370-2693. DOI: 10.1016/0370-2693(83)90188-0.

[19] P. Bagnaia et al. "Evidence for $Z^0 \to e^+e^-$ at the CERN pp collider". In: *Physics Letters B* 129.1 (1983), pp. 130–140. ISSN: 0370-2693. DOI: 10.1016/0370-2693(83)90744-X.

[20] G. Baur et al. "Production of antihydrogen". In: *Physics Letters B* 368.3 (1996), pp. 251–258. ISSN: 0370-2693. DOI: 10.1016/0370-2693(96)00005-6.

[21] V. Fanti et al. "A new measurement of direct CP violation in two pion decays of the neutral kaon". In: *Physics Letters B* 465.1 (1999), pp. 335–348. ISSN: 0370-2693. DOI: 10.1016/S0370-2693(99)01030-8.

[22] L. Evans and P. Bryant. "LHC Machine". In: *Journal of Instrumentation* 3.08 (2008), S08001–S08001. DOI: 10.1088/1748-0221/3/08/s08001.

[23] J.M. Jowett. "Colliding Heavy Ions in the LHC". In: *Proc. 9th International Particle Accelerator Conference (IPAC'18), Vancouver, BC, Canada, April 29-May 4, 2018*. International Particle Accelerator Conference 9. JACoW Publishing, 2018, pp. 584–589. ISBN: 978-3-95450-184-7. DOI: 10.18429/JACoW-IPAC2018-TUXGBD2.

[24] C. Lefèvre. "The CERN accelerator complex. Complexe des accélérateurs du CERN". Accessed: 2021-01-25. 2008. URL: https://cds.cern.ch/record/1260465.

[25] The LHCb Collaboration. "The LHCb Detector at the LHC". In: *Journal of Instrumentation* 3.08 (2008), S08005–S08005. DOI: 10.1088/1748-0221/3/08/s08005.

[26] The ALICE Collaboration. "The ALICE experiment at the CERN LHC". In: *Journal of Instrumentation* 3.08 (2008), S08002–S08002. DOI: 10.1088/1748-0221/3/08/s08002.

[27] "LHC Guide". 2017. URL: https://cds.cern.ch/record/2255762.

[28] CERN. "HL-LHC Project Schedule". Accessed: 2021-01-25. 2020. URL: https://project-hl-lhc-industry.web.cern.ch/content/project-schedule.

[29] CMS Collaboration. *CMS public website*. http://cms.web.cern.ch/. Accessed: 2017-01-24. 2011.

[30] V. Karimäki et al. *The CMS tracker system project: Technical Design Report*. Tech. rep. Geneva: CMS Collaboration, 1997. URL: http://cds.cern.ch/record/368412.

[31] G. Baiatian et al. *Design, Performance and Calibration of the CMS Forward Calorimeter Wedges*. Tech. rep. CMS-NOTE-2006-044. Geneva: CERN, 2006. DOI: 10.1140/epjc/s10052-007-0459-4.

[32] *The Phase-2 Upgrade of the CMS L1 Trigger Interim Technical Design Report*. Tech. rep. CERN-LHCC-2017-013. CMS-TDR-017. Geneva: CERN, 2017. URL: https://cds.cern.ch/record/2283192.

[33] CMS Collaboration. *The Phase-2 Upgrade of the CMS Tracker*. Tech. rep. CERN-LHCC-2017-009. CMS-TDR-014. Geneva: CERN, 2017. URL: https://cds.cern.ch/record/2272264.

[34] W. Adam et al. "P-Type Silicon Strip Sensors for the new CMS Tracker at HL-LHC". In: *Journal of Instrumentation* 12.06 (2017), P06018–P06018. DOI: 10.1088/1748-0221/12/06/p06018.

[35] W. Adam et al. "Experimental study of different silicon sensor options for the upgrade of the CMS Outer Tracker". In: *Journal of Instrumentation* 15.04 (2020), P04017–P04017. DOI: 10.1088/1748-0221/15/04/p04017. URL: https://doi.org/10.1088%2F1748-0221%2F15%2F04%2Fp04017.

[36] W. Adam et al. "Beam test performance of prototype silicon detectors for the Outer Tracker for the Phase-2 Upgrade of CMS". In: *Journal of Instrumentation* 15.03 (2020), P03014–P03014. DOI: 10.1088/1748-0221/15/03/p03014.

[37] CMS Collaboration. *The Phase-2 Upgrade of the CMS Endcap Calorimeter*. Tech. rep. CERN-LHCC-2017-023. CMS-TDR-019. Geneva: CERN, 2017. URL: https://cds.cern.ch/record/2293646.

[38] D. Barney and CMS Collaboration. *Overview slide of CE with main parameters*. https://cms-docdb.cern.ch/cgi-bin/PublicDocDB/ShowDocument?docid=13251. Accessed: 2021-01-23. 2019.

[39] S.M. Sze and Kwok K. Ng. *Physics of Semiconductor Devices*. John Wiley & Sons, Inc., 2006. DOI: 10.1002/9780470068328.fmatter.

[40] S.M. Sze. *Semiconductor Devices: Physics and Technology*. John Wiley & Sons, Inc., 2002.

[41] G. Lutz. *Semiconductor Radiation Detectors*. Springer-Verlag Berlin Heidelberg, 2007. DOI: 10.1007/978-3-540-71679-2.

[42] H. Kolanoski and N. Wermes. *Teilchendetektoren. Grundlagen und Anwendungen*. Springer-Verlag Berlin Heidelberg, 2016. DOI: 10.1007/978-3-662-45350-6.

[43] D. K. Schroder. *Semiconductor Material and Device Characterization*. John Wiley & Sons, Inc., 2005. ISBN: 9780471749097. DOI: 10.1002/0471749095. URL: http://dx.doi.org/10.1002/0471749095.

[44] V. Hinger. "Charge Sharing Studies of Silicon Strip Sensors for the CMS Phase II Upgrade". Master's Thesis. Vienna University of Technology, 2017. URL: https://catalogplus.tuwien.at/permalink/f/8j3js/UTW_alma2150984030003336.

[45] K. Misiakos and D. Tsamakis. "Accurate measurements of the silicon intrinsic carrier density from 78 to 340 K". In: *Journal of Applied Physics* 74.5 (1993), pp. 3293–3297. DOI: 10.1063/1.354551.

[46] N. D. Arora, J. R. Hauser, and D. J. Roulston. "Electron and hole mobilities in silicon as a function of concentration and temperature". In: *IEEE Transactions on Electron Devices* 29.2 (1982), pp. 292–295. ISSN: 0018-9383. DOI: 10.1109/T-ED.1982.20698.

[47] P. A. Zyla (Particle Data Group) et al. "Review of Particle Physics". In: *Progress of Theoretical and Experimental Physics* 2020.8 (Aug. 2020). 083C01. ISSN: 2050-3911. DOI: 10.1093/ptep/ptaa104.

[48] L. Landau. "On the energy loss of fast particles by ionization". In: *J. Phys.(USSR)* 8 (1944), pp. 201–205.

[49] W. Shockley. "Currents to Conductors Induced by a Moving Point Charge". In: *Journal of Applied Physics* 9.10 (1938), pp. 635–636. DOI: 10.1063/1.1710367.

[50] S. Ramo. "Currents Induced by Electron Motion". In: *Proceedings of the IRE* 27.9 (1939), pp. 584–585. DOI: 10.1109/JRPROC.1939.228757.

[51] M. Moll. "Radiation Damage in Silicon Particle Detectors". PhD Thesis. Universität Hamburg, 1999. URL: https://mmoll.web.cern.ch/mmoll/thesis/pdf/moll-thesis.pdf.

[52] F. Hönniger. "Radiation damage in silicon: Defect analysis and detector properties". PhD thesis. Universität Hamburg, 2007. DOI: 10.3204/DESY-THESIS-2008-002. URL: https://inspirehep.net/literature/779269.

[53] A. Junkes. "Influence of radiation induced defect clusters on silicon particle detectors". PhD Thesis. Universität Hamburg, 2011. URL: https://inspirehep.net/literature/940715.

[54] M. Moll. *Radiation Damage in Silicon Detectors*. https://ssd-rd.web.cern.ch/seminar/transparencies/01-02-14-ssd-michael-moll.pdf. Accessed: 2021-01-21. CERN EP-TA1-SD Seminar 14.2.2001.

[55] J. Zhang et al. "Investigation of X-ray induced radiation damage at the Si-SiO_2 interface of silicon sensors for the European XFEL". In: *Journal of Instrumentation* 7.12 (2012), pp. C12012–C12012. DOI: 10.1088/1748-0221/7/12/c12012.

[56] I. Kopsalis. "Surface Effects in Segmented Silicon Sensors". PhD Thesis. Universität Hamburg, 2017. URL: https://bib-pubdb1.desy.de/record/322130/files/Ioannis_Kopsalis_Dissertation_2017.pdf.

[57] M. Dragicevic. "The New Silicon Strip Detectors for the CMS Tracker Upgrade". PhD Thesis. Vienna University of Technology, 2010. URL: https://catalogplus.tuwien.at/permalink/f/8j3js/UTW_alma2166705480003336.

[58] T. Bergauer. "Process Quality Control of Silicon Strip Detectors for the CMS Tracker". Master's Thesis. Vienna University of Technology, 2004. URL: https://catalogplus.tuwien.at/permalink/f/8j3js/UTW_alma2164080260003336.

[59] T. Bergauer. "Design, Construction and Commissioning of the CMS Tracker at CERN and Proposed Improvements for Detectors at the Future International Linear Collider". PhD Thesis. Vienna University of Technology, 2008. URL: https://catalogplus.tuwien.at/permalink/f/8j3js/UTW_alma2165895810003336.

[60] E. Brondolin et al. "ARRAY: An open source, modular and probe-card based system with integrated switching matrix for characterisation of large area silicon pad sensors". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 940 (2019), pp. 168–173. ISSN: 0168-9002. DOI: 10.1016/j.nima.2019.06.007.

[61] M. Baselga et al. "Front-side biasing of n-in-p silicon strip detectors". In: *Journal of Instrumentation* 13.11 (2018), P11007–P11007. DOI: 10.1088/1748-0221/13/11/p11007.

[62] M. Printz. "Development of radiation-hard n-in-p type silicon detectors and studies on modules with transverse momentum discrimination for the CMS detector at the LHC". PhD Thesis. KIT, Karlsruhe, 2016. DOI: 10.5445/IR/1000052766.

[63] R. Dalal et al. "Combined effect of bulk and surface damage on strip insulation properties of proton irradiated n-p silicon strip sensors". In: *Journal of Instrumentation* 9.04 (2014), P04007–P04007. DOI: 10.1088/1748-0221/9/04/p04007.

[64] M. Printz. "P-stop isolation study of irradiated n-in-p type silicon strip sensors for harsh radiation environments". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 831 (2016). Proceedings of the 10th International "Hiroshima" Symposium on the Development and Application of Semiconductor Tracking Detectors, pp. 38–43. ISSN: 0168-9002. DOI: 10.1016/j.nima.2016.05.103.

[65] Y. Unno et al. "P-stop designs for reducing electric field strength at implant edges". In: *2008 IEEE Nuclear Science Symposium Conference Record*. 2008, pp. 2507–2512. DOI: 10.1109/NSSMIC.2008.4774864.

[66] S. Braibant et al. "Investigation of design parameters for radiation hard silicon microstrip detectors". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 485.3 (2002), pp. 343–361. ISSN: 0168-9002. DOI: 10.1016/S0168-9002(01)02120-9.

[67] A. König. "Planar Silicon Strip Sensors for the CMS Phase-2 Upgrade". PhD Thesis. Vienna University of Technology, 2017. URL: https://permalink.catalogplus.tuwien.at/AC14526557.

[68] F. Hartmann. *Evolution of Silicon Sensor Technology in Particle Physics*. Vol. 275. Springer Tracts in Modern Physics. Springer, 2017. ISBN: 978-3-319-64434-9, 978-3-319-64436-3. DOI: 10.1007/978-3-319-64436-3.

[69] D. Ceresa et al. "A 65 nm pixel readout ASIC with quick transverse momentum discrimination capabilities for the CMS Tracker at HL-LHC". In: *Journal of Instrumentation* 11.01 (2016), pp. C01054–C01054. DOI: 10.1088/1748-0221/11/01/c01054.

[70] P. Paulitsch. "The silicon sensors for the High Granularity Calorimeter of CMS". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 978 (2020), p. 164428. ISSN: 0168-9002. DOI: 10.1016/j.nima.2020.164428.

[71] T. Bergauer et al. "First thin AC-coupled silicon strip sensors on 8-inch wafers". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 830 (2016), pp. 473–479. ISSN: 0168-9002. DOI: 10.1016/j.nima.2016.05.076.

[72] D. Blöch. "Silicon Strip Sensors for the CMS Phase-2 Upgrade". Forthcoming. PhD Thesis. Vienna University of Technology, 2021.

[73] T. Bergauer et al. "History, status and prospects of producing silicon sensors for HEP experiments at Infineon Technologies". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 924 (2019). 11th International Hiroshima Symposium on Development and Application of Semiconductor Tracking Detectors, pp. 1–6. ISSN: 0168-9002. DOI: 10.1016/j.nima.2018.06.069.

[74] M. Metzler. "Irradiation studies on n-in-p silicon strip sensors in the course of the CMS Phase-2 Outer Tracker Upgrade". PhD thesis. Karlsruhe Institute of Technology (KIT), 2020. URL: https://publish.etp.kit.edu/record/21943.

[75] S. R. Chowdhury. "The Phase-2 Upgrade of the CMS Outer Tracker". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 979 (2020), p. 164432. ISSN: 0168-9002. DOI: 10.1016/j.nima.2020.164432.

[76] E. Pree. "Development of Large Area Silicon Sensors for the High Granularity Calorimeter at CMS". PhD Thesis. Vienna University of Technology, 2018. URL: https://permalink.catalogplus.tuwien.at/AC15192834.

[77] F. M. Pitters. "Silicon Detector Technologies for Future Particle Collider Experiments". Presented 2020. PhD Thesis. 2019. URL: https://cds.cern.ch/record/2714709.

[78] *7072-HV High Voltage Semiconductor Matrix Card*. http://legacy.libertytest.com/assetmanager/uploaded/pdf-20111025-141257-7072-hv.pdf. Accessed: 2021-01-16.

[79] *COMET PQC – Process Quality Control for CMS Tracker*. https://hephy-dd.github.io/comet-pqc/. Accessed: 2021-01-17.

[80] *Synopsis TCAD webpage*. https://www.synopsys.com/silicon/tcad.html. Accessed: 2019-03-29.

[81] Y.F. Chang. "The capacitance of p-n junctions". In: *Solid-State Electronics* 10.4 (1967), pp. 281–287. ISSN: 0038-1101. DOI: 10.1016/0038-1101(67)90014-7.

[82] E. Fretwurst et al. "The influence of edge effects on the determination of the doping profile of silicon pad diodes". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 867 (2017), pp. 231–236. ISSN: 0168-9002. DOI: 10.1016/j.nima.2017.04.020.

[83] D. K. Schroder. "The concept of generation and recombination lifetimes in semiconductors". In: *IEEE Transactions on Electron Devices* 29.8 (1982), pp. 1336–1338.

[84] R. N. Hall. "Electron-Hole Recombination in Germanium". In: *Phys. Rev.* 87 (2 1952), pp. 387–387. DOI: 10.1103/PhysRev.87.387.

[85] W. Shockley and W. T. Read. "Statistics of the Recombinations of Holes and Electrons". In: *Phys. Rev.* 87 (5 1952), pp. 835–842. DOI: 10.1103/PhysRev.87.835.

[86] Y. P. Varshni. "Band-to-Band Radiative Recombination in Groups IV, VI, and III-V Semiconductors (I)". In: *Phys. Stat. Sol.* 19.2 (1967), pp. 459–514. DOI: 10.1002/pssb.19670190202.

[87] Y. P. Varshni. "Band-to-Band Radiative Recombination in Groups IV, VI, and III-V Semiconductors (II)". In: *Phys. Stat. Sol.* 20 (1967), pp. 9–36. DOI: 10.1002/pssb.19670200102.

[88] Y. Murakami and T. Shingyouji. "Separation and analysis of diffusion and generation components of pn junction leakage current in various silicon wafers". In: *Journal of Applied Physics* 75.7 (1994), pp. 3548–3552. DOI: 10.1063/1.356091.

[89] E. Simoen et al. "Accurate extraction of the diffusion current in silicon p-n junction diodes". In: *Applied Physics Letters* 72.9 (1998), pp. 1054–1056. DOI: 10.1063/1.120962.

[90] A. Czerwinski et al. "Optimized Diode Analysis of Electrical Silicon Substrate Properties". In: *Journal of the Electrochemical Society* 145 (June 1998), pp. 2107–2112. DOI: 10.1149/1.1838604.

[91] V. Mariani et al. "Measurements of surface and bulk radiation damage effects in silicon detectors for Phase-2 CMS Outer Tracker". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 980 (2020), p. 164423. ISSN: 0168-9002. DOI: 10.1016/j.nima.2020.164423.

[92] E. H. Nicollian and J. R. Brews. *MOS (Metal Oxide Semiconductor) Physics and Technology*. John Wiley & Sons, Inc., 1982. ISBN: 0471085006.

[93] *SGS Institut Fresenius GmbH*. https://www.institut-fresenius.de/en/. Accessed: 2020-12-14.

[94] A.S. Grove and D.J. Fitzgerald. "Surface effects on p-n junctions: Characteristics of surface space-charge regions under non-equilibrium conditions". In: *Solid-State Electronics* 9.8 (1966), pp. 783–806. ISSN: 0038-1101. DOI: 10.1016/0038-1101(66)90118-3.

[95] G. Verzellesi et al. "On the accuracy of generation lifetime measurement in high-resistivity silicon using PN gated diodes". In: *IEEE Transactions on Electron Devices* 46.4 (1999), pp. 817–820. DOI: 10.1109/16.753724.

[96] F. Moscatelli et al. "Measurements and simulations of surface radiation damage effects on IFX and HPK test structures". In: *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment* 958 (2020). Proceedings of the Vienna Conference on Instrumentation 2019, p. 162794. ISSN: 0168-9002. DOI: 10.1016/j.nima.2019.162794.

[97] D.J. Fitzgerald and A.S. Grove. "Surface recombination in semiconductors". In: *Surface Science* 9.2 (1968), pp. 347–369. ISSN: 0039-6028. DOI: 10.1016/0039-6028(68)90182-9.

[98] L. J. van der Pauw. "A Method of Measuring Specific Resistivity and Hall Effect Discs of Arbitrary Shape". In: *Philips Research Reports* 13 (Feb. 1958), pp. 1–9.

[99] A. König et al. "Field effect transistor test structures for p-stop strip isolation studies". In: *Journal of Instrumentation* 12.02 (2017), p. C02067. URL: http://stacks.iop.org/1748-0221/12/i=02/a=C02067.

[100] K. Terada, K. Nishiyama, and K.I. Hatanaka. "Comparison of MOSFET-threshold-voltage extraction methods". In: *Solid-State Electronics* 45.1 (2001), pp. 35–40. ISSN: 0038-1101. DOI: 10.1016/S0038-1101(00)00187-8.

[101] A. Ortiz-Conde et al. "A review of recent MOSFET threshold voltage extraction methods". In: *Microelectronics Reliability* 42.4 (2002), pp. 583–596. ISSN: 0026-2714. DOI: 10.1016/S0026-2714(02)00027-6.

[102] T. A. Schreyer and K. C. Saraswat. "A two-dimensional analytical model of the cross-bridge Kelvin resistor". In: *IEEE Electron Device Letters* 7.12 (1986), pp. 661–663. DOI: 10.1109/EDL.1986.26511.

[103] R. G. Mazur and D. H. Dickey. "A Spreading Resistance Technique for Resistivity Measurements on Silicon". In: *Journal of The Electrochemical Society* 113.3 (1966), p. 255. DOI: 10.1149/1.2423927. URL: https://doi.org/10.1149/1.2423927.

[104] T. Clarysse et al. "Characterization of electrically active dopant profiles with the spreading resistance probe". In: *Materials Science and Engineering: R: Reports* 47.5 (2004), pp. 123–206. ISSN: 0927-796X. DOI: 10.1016/j.mser.2004.12.002.

[105] A. Benninghoven. "The Analysis of Monomolecular Layers of Solids by Secondary Ion Emission". In: *Z. Phys.* 230 (Jan. 1970). In German, pp. 403–417. URL: https://www.osti.gov/biblio/4754683.