Threshold measurements on MALTA Pixel detector prototype

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Abstract
Monolithic silicon Pixel detector MALTA is now being developed using CMOS technology by TowerJazz for ATLAS experiment. The first threshold measurement for MALTA was carried out in this project.

Keywords
CERN Summer Student; ATLAS ITk

1 ATLAS ITk

The ATLAS Inner Tracker (ITk) will be the new all-silicon Inner detector of the ATLAS experiment for the Phase-II upgrade of the LHC. it will have to cope with extreme radiation damage, with low material budget, high granularity, and tracking coverage up to $|\eta|$ = 4.0. The central region composed of 5 Pixel and 4 Strip layers up to 1 m radial distance. Forward region composed of disks up to z = 3 m. Baseline Pixel detectors will be 3D sensors for inner most layer and planar sensors everywhere else. These layouts are shown in Fig. 1. For the upgrade of the Pixel detector, we are developing new radiation hard detector, MALTA. MALTA could be the outermost layer of the 5 Pixel detector layers.

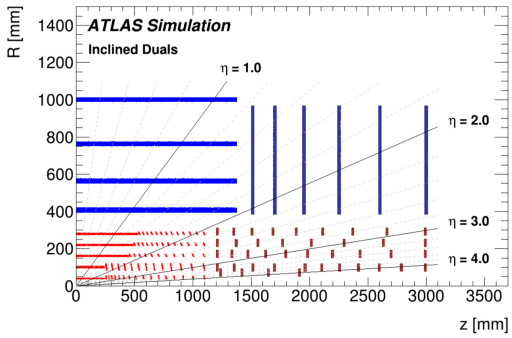

Fig. 1: Schematic layout of the ITk for the Phase-II upgrade. Pixel detectors are shown in red. [1]

2 MALTA

MALTA is monolithic silicon Pixel detector made in CMOS technology by TowerJazz using 180nm size transistors. A schematic cross-section of one pixel of MALTA is showed in Fig. 2.

Conventional hybrid pixel detector is made by joining silicon pixel sensor and read-out chip after fabricating each of them, while in monolithic silicon pixel detector the readout circuitry is combined in one piece of silicon. This makes the pixel detector thicker (about 100 μm) and low amount of material. Other advantage is the fact that we can deplete the chip with low voltage hence lower power consumption. As shown in Fig. 2, an ionizing particle generates electron/hole pairs in a depleted zone, and this charge is collected by an n-well electrode. The collection electrode of 3 μm^2 is shown in Fig. 3, and this small electrode makes noise lower.

One MALTA chip consists of 8 sectors of 64 columns $\times$ 512 rows: 512 $\times$ 512 pixels with a pitch of 36.4μm. It aims to be operational after 1×10^{15} n_{eq}/cm^2.

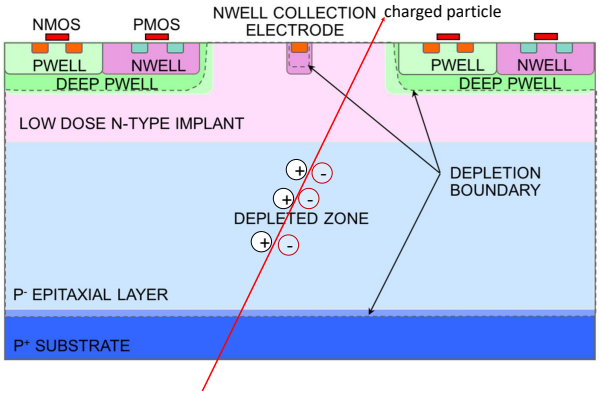

Fig. 2: Schematic cross-section of one pixel of MALTA [2] [3]

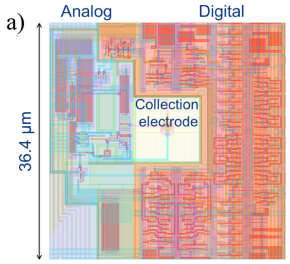

Fig. 3: The MALTA pixel [4]

3 Threshold Measurement

Each pixel of MALTA has an analog front-end which contains a shaper-amplifier to integrate current and a discriminater which produce a digital output when an analog input exceeds a fixed value, so called threshold. To keep the electronics in the pixel small, we can only act on global chip configuration which is common to all the front-end. Therefore, the investigation is necesarry to check how uniform the pixel-by-pixel response is. Few threshold scans of MALTA have been conducted so far. In this project, we improved the C++ and python codes for threshold measurement of MALTA and measured the threshold on different samples.

3.1 Setup and Procedure

We performed threshold scan for three MALTA chips (W7R19, W7R8, W7R6) using two power supplies and one FPGA board. The setup is shown in Fig. 4.

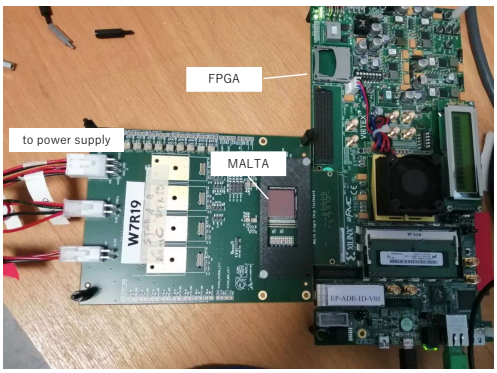

Fig. 4: MALTA chip on the test board and FPGA board.

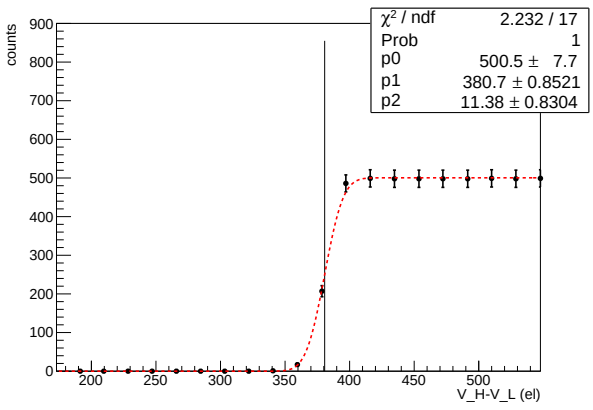

Fig. 5: One scanning result of W7R6. Number of hits as a function o injected charge.

We can inject analogue signal pulses before the discriminator of each chip. The amplitude of these pulses are governed by the difference between V_{high} and V_{low}. In this threshold scan we fixed the former, changed the latter and read if the pulse made a hit or not. The procedure of threshold scan for each pixel is as follows.

1. Injected 500 pulses into the one pixel changing amplitude of V_{low}.

2. Counted the number of hits.
3. As amplitude of V_{low} become lower which means amplitude of the pulse become higher, the number of hits increase.
4. Fit error function with three parameters: pedestal, threshold and noise.

Fig. 5 shows a typical threshold scan for one pixel. The fitting parameters, p0, p1 and p2, correspond to pedestal, threshold and noise, respectively. This whole procedure took about 90 secs for one pixel, and we could scan only one pixel at the same time due to the hits interfering with each other. Each value of configuration parameters is shown in Table 1. Among these parameters the value of IDB has a direct effect on threshold.

Table 1: Configuration of each chip

	W7R19 left	W7R19 right	W7R8	W7R6-1	W7R6 -2
ICASN	10	10	10	10	10
IBIAS	50	50	80	80	80
ITHR	10	10	30	30	30
IDB	15	15	60	60	40
IRESET*	127	10	30	30	30 (16, 5, 2)
VCASN	64	64	64	64	64
VRESET_P*	127	32	45	45	45
VRESET_D	58	58	65	65	65
VPLSE_HIGH	90	90	90	90	90
VPLSE_LOW	5	5	5	5	5
VCLIP	127	127	127	127	127

* IRESET and VRESET have no effect on left side of chip (1-4th sector)

3.2 Results and Consideration

3.2.1 Threshold

Threshold scans were performed for W7R19 in the top (503-512th row of 1-4th sector) and bottom (1-10th row of 1-8th sector) region, and for W7R8 and W7R6 in the bottom region (1-10th row of 1-8th sector).

Fig. 6 shows the bottom result of W7R19 as an example: top three figures are result of threshold and bottom three figures are of noise. In each sector RMS and the means of threshold and noise were extracted by fitting these histograms with a Gaussian distribution. It must be mentioned that the fitting range of noise is from $4.0\,\mathrm{electrons}$. In Fig. 7, RMS, the mean values of threshold and noise in every chip are shown as a function of sector. From these results, we can say these three MALTA chips have similar threshold, which means there is no significant difference between each sector. The thresholds of the top region of W7R19 are only $10\mathrm{electrons}$ lower than ones of the top region. Also, the RMS of the various sectors is consistent with the old results on Malta chips. In terms of the comparison between two different chips, when the two chips (W7R8 and W7R6) have the same configuration they have similar thresholds and noises.

However, Regarding the noise there is non-negligible difference between first 4 sectors (left side) and latter 4 sectors (right side). This will be discussed in 3.2.2.

3.2.2 Noise vs IRESET

As being mentioned in 3.2.1, the noise of the right side is twice as high as of the left side. This is due to the difference of electric circuit on front-end between the right and left side. In Fig. 8, the difference

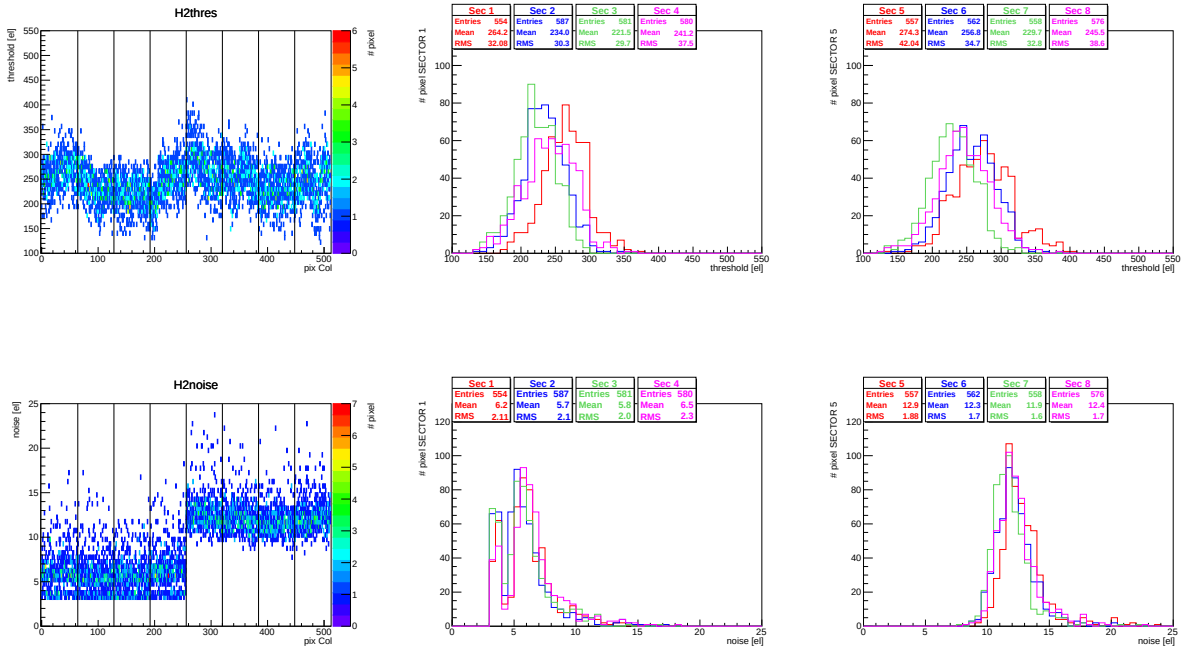

Fig. 6: The threshold scan result of the bottom region of W7R19 : (top left) 2D map of threshold of each colomun, (top middle+right) projection into threshold, (bottom left) 2D map of noise of each colomun, (bottom middle+right) projection into noise

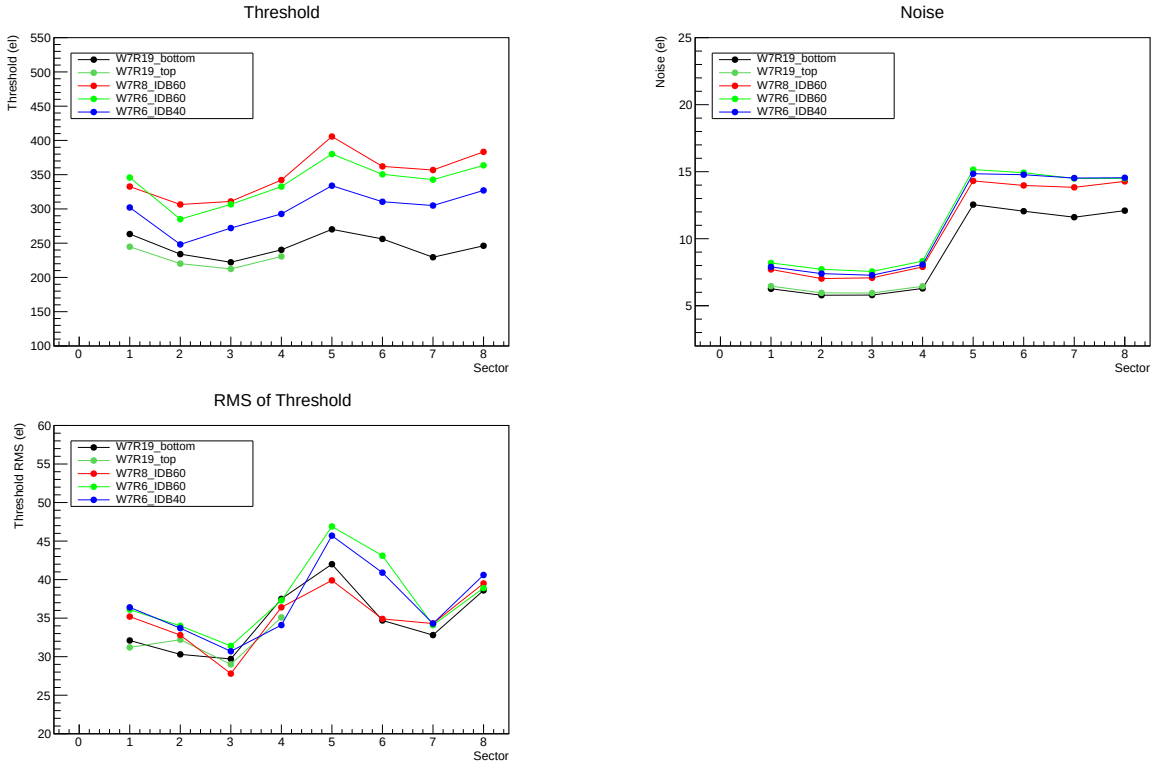

Fig. 7: The threshold scan result of all chips as a function of sector. (top left) the mean value of threshold, (bottom left) RMS of threshold, (right) the mean value of noise

between them is shown : the right side has a transistor which has electric current I_{reset}. It is speculated that noise is governed by $\sqrt{2}\, I_{\mathrm{leak}}$ in the left side and by $\sqrt{I_{\mathrm{leak}}^2 + I_{\mathrm{reset}}^2}$ in the right side. In this section, we refer to the result of threshold scans with four IRESETs (the configuration value for I_{reset}).
Threshold scans with four IRESETs were performed for 5th and 6th sector of W7R6 chip. Each IRESET value is shown in Table 1. Fig. 9 shows how the noise changed as a function of IRESET and Fig. 10 shows how the threshold changed.

We obserbed that the lower the IRESET, the lower the noise. On the other hand, the threshold did not

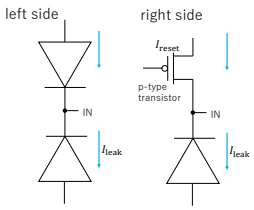

Fig. 8: the difference of electrical circuit on front-end between the right and left side of a MALTA chip

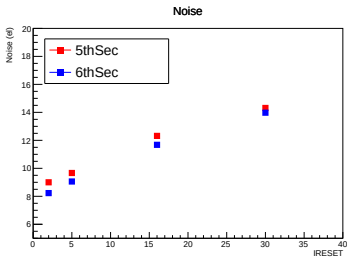

Fig. 9: the mean of noise in 5th and 6th sector as a function of IRESET.

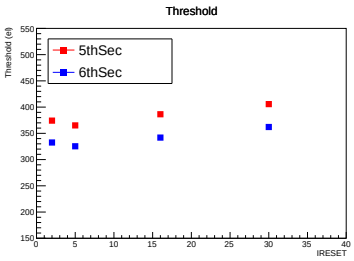

Fig. 10: the mean of threshold in 5th and 6th sector as a function of IRESET.

change so much. These results suggest that IRESET is an immediate cause to the noise but not to the threshold.

3.2.3 Analog scan

Although threshold scan was not performed for the whole chip, the analogue scan was performed for whole W7R6 chip instead. This test was for the purpose of investigation of the response from every pixel, and completely the first test until now. In the analogue scan, 500 pulses which have higher amplitude than threshold were injected to each pixel and the number of hits was counted.
The result of the analogue scan is shown in Fig. 11. It was revealed that almost all pixels of this chip responded properly.

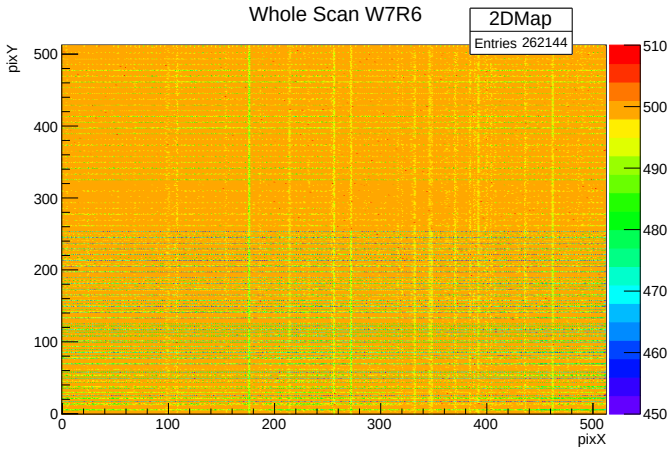

Fig. 11: 2D map of the analogue scan for W7R6 chip. Z axis is the number of hits when injected 500 pulses.

3.3 Conclusions

In this project, the first precise threshold measurements for MALTA were performed. It became clear that MALTA was reliable in terms of the threshold stability. Regarding the noise of the right side of the chip, it was revealed that the IRESET has a direct effect on it. However, the threshold scan for a whole chip has not been carried out. This is mainly because it takes $90\ \mathrm{sec}$ to scan one pixel. Improvement of the way of threshold scan is a task in a future.

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