

Volkan Vatansever

Zuverlässigkeitsanalyse der neuen Verbindung zwischen dem Beam Interlock System und dem LHC Beam Dumping System

Reliability Analysis of the new Link between the Beam Interlock
System and the LHC Beam Dumping System

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Abstract

The nominal stored energy in each LHC beam is 360 MJ, surpassing the beam energy of other accelerators by orders of magnitude. This energy threatens to damage accelerator components in case of uncontrolled beam losses

To avoid damage of accelerator equipment due to impacting beam, the controlled removal of the LHC beams from the collider rings towards the dump block must be guaranteed at all times. Therefore, the LHC Beam Dumping System was built according to high reliability standards. To further reduce the risk of incapability to dump the beams in case of correlated failures in the redundant system, a new direct link from the LHC Beam Interlock System to the Re-triggering Lines of the LHC Beam Dumping System will be implemented for the start-up with beam in 2015. This link represents a diverse redundancy to the current implementation, which should neither significantly increase the risk for so-called Asynchronous Beam Dumps nor compromise machine availability. Therefore, a reliability analysis down to the component level has been performed for this new link. In this thesis the applied methods and the results of this analysis will be discussed in detail. The hardware implementation and the system integration will be analysed.

Übersicht

Die in den beiden Protonenstrahlen des LHC gespeicherte Energie übertrifft mit 360 MJ diejenige anderer Beschleuniger um mehrere Größenordnungen. Im Falle unkontrollierter Strahlenverluste können daher Komponenten des Beschleunigers ernsthaft beschädigt werden.

Zur Vermeidung der Zerstörung von Teilen des Beschleunigers durch Teilchenverluste muss die sichere Extraktion des gespeicherten Teilchenstrahles in einen speziellen Strahlauffänger zu jeder Zeit des Beschleunigerbetriebs garantiert sein. Um dies zu gewährleisten, wurde das Strahlextraktionssystem des LHC nach höchsten Zuverlässigkeitsstandards gebaut.

Im Falle von korrelierten Fehlern in diesem redundanten System besteht das Risiko, dass der Teilchenstrahl nicht extrahiert werden kann. Deswegen wird bis zur Wiederaufnahme des Strahlbetriebs am LHC im Jahre 2015 eine neue Verbindung zwischen dem Strahlsicherheitssystem des LHC und eines Teils des Strahlextraktionssystems installiert. Diese, zum bestehenden System redundante Verbindung soll dabei weder das Risiko einer sogenannten asynchronen Strahlextraktion signifikant erhöhen, noch die Verfügbarkeit des Beschleunigers wesentlich reduzieren. Deshalb wurde eine Zuverlässigkeitsanalyse dieser neuen Verbindung bis zur Ebene der elektronischen Bauteile durchgeführt. Die dabei verwendeten Methoden und die erzielten Ergebnisse werden in der vorliegenden Diplomarbeit ausführlich diskutiert. Ferner werden die Implementierung der Hardware und die Systemintegration der neuen Verbindung analysiert.

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Formula symbols and acronyms

Formula Symbol

Formula Symbol	Explanation	Unit
b	Shape Factor	-
c	Speed of Light	m/s
E	Energy	J
$f(t)$	Density Function	-
$F(t)$	Failure Probability	-
I	Current	A
L	Inductance	H
MTTF	Mean Time to Failure	Years
n_B	Number of Bunches	-
N	Intensity per Bunch	-
$R(t)$	Survival Probability	-
s	Standard Deviation	-
s^2	Variance	-
t	Time	s
T	Characteristic Lifetime	-
α	Mode Probability	%
β	Severity Class	-
λ	Failure Rate	FIT
μ	Mean	-
π	Adaption Factor	-
σ	Scale Parameter	-
ξ_p	Energy of one Charged Particle	TeV

Acronyms

Acronym	Explanation
ALICE	A Large Ion Collider Experiment
ABD	Asynchronous Beam Dump
ALICE	A Large Ion Collider Experiment
ATLAS	A Toroidal LHC Apparatus
BEMS	Beam Energy Meter System
BETS	Beam Energy Tracking System
BIC	Beam Interlock Controller
BIS	Beam Interlock System
BLM	Beam Loss Monitor
BPF	Beam Permit Flag
BPM	Beam Position Monitor
CCC	CERN Control Centre
CERN	European Organization for Nuclear Research
CIBDS	Beam Interlock Controller Dumping System
CIBU	Beam Interlock Controller User Interface
cm	Centimetre
CMS	Compact Muon Solenoid
CPLD	Complex Programmable Logic Device
FIT	Failures In Time
FMECA	Failure Mode, Effects, and Criticality Analysis
FTA	Fault Tree Analysis
GeV	Gigaelectron Volt
HDBK	Handbook
IC	Integrated Circuit
IP	Interaction Point
IR	Interaction Region
K	Kelvin
LBDS	LHC Beam Dumping System
LEIR	Low Energy Ion Ring
LEP	Large Electron-Positron Collider
LHC	Large Hadron Collider
LHCb	Large Hadron Collider beauty
LHCf	Large Hadron Collider forward
LINAC	Linear Accelerator
LS1	Long Shutdown 1
m	Metre
MAN	Manufacturer
MIL	Military
MJ	Mega Joule
MKB	Diluter Magnet
MKD	Kicker Magnet

Acronym	Explanation
mm	Millimetre
MPS	Machine Protection System
ms	Milliseconds
MSD	Ejection Dump Septum
MTBF	Mean Time between Failure
MTTF	Mean Time to failure
ns	Nanoseconds
PLC	Programmable Logic Controller
PS	Proton Synchrotron
PSB	Proton Synchrotron Booster
PTU	Power Transfer Unit
Q	Quadrupole Magnet
QGP	Quark-gluon Plasma
QPS	Quench Interlock System
RF	Radio frequency
RTB	Re-triggering Box
RTS	Re-triggering System
SBD	Synchronous Beam Dump
SIL	Safety Integrity Level
SPS	Super Proton Synchrotron
STD	Standard
T	Tesla
TCDQ	Target Collimator Dump Quadrupole
TCDS	Target Collimator Dump Septum
TDC	Trigger delay circuit
TDE	Dump Block
TDIC	Trigger delay interlock circuit
TDU	Trigger Delay Unit
TDU250	250 μ s Trigger Delay Unit
TeV	Teraelectron volt
TFOR	Trigger Fan-Out Receiver
TFOT	Trigger Fan-Out Transceiver
TOTEM	Total Elastic and diffractive cross section Measurement
TSU	Trigger Synchronisation Unit
VHDL	VHSIC Hardware Description Language

1 Introduction to the European Organization for Nuclear Research (CERN)

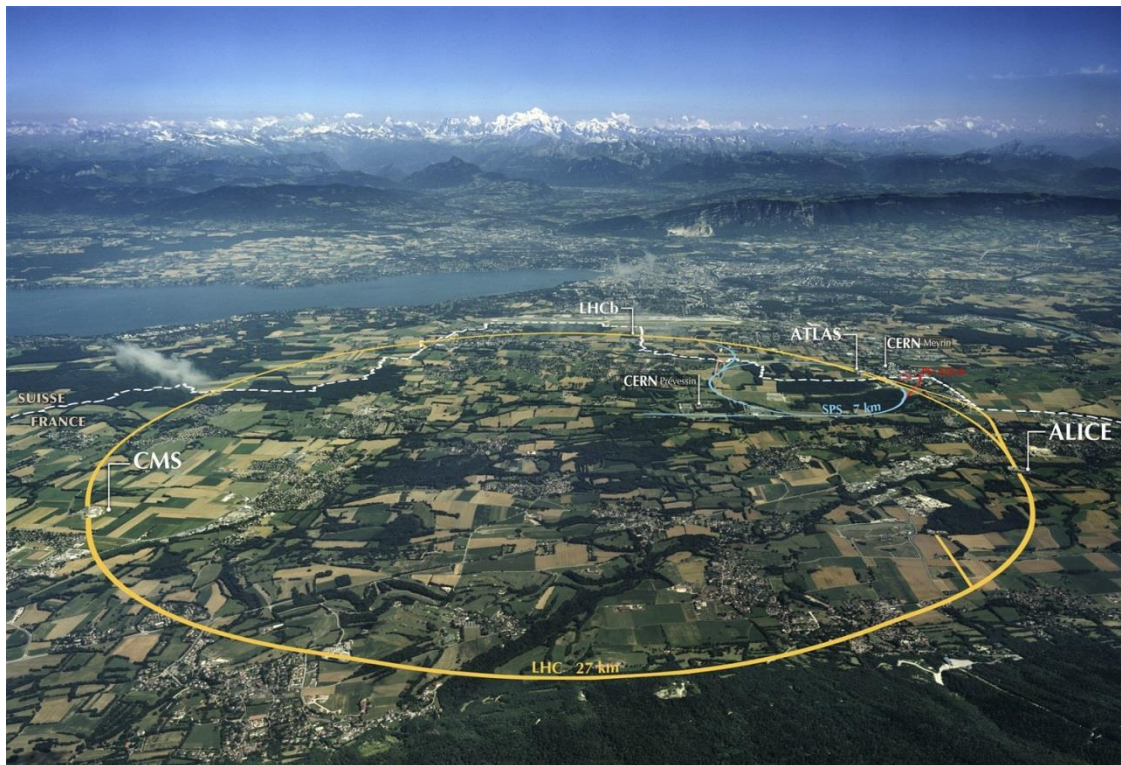


Figure 1.1: Aerial View of CERN with the Alps Mountains in the background. The yellow circle shows the LHC tunnel [1].

Shortly after World War 2 European scientists imagined creating a European atomic physics laboratory to combine knowledge but also to share the increasing costs of nuclear research. The French physicist Louis de Broglie made the first official proposal for a European laboratory at the European Cultural Conference in Lausanne on the 9th of December 1949. Three years later eleven countries signed an agreement establishing a provisional council. Founded in 1954, CERN is located in Geneva, Switzerland, on the Franco-Swiss border.

Nowadays CERN has grown to one of the biggest institutions for scientific research with 20 member states, operating the world's largest particle accelerator, the Large Hadron Collider (LHC). More than 2500 staff members, 500 fellows and about 11000 visiting researchers, over 500 universities and people from over 80 different countries have become part of CERN and set a prime example of intercultural and scientific collaboration [1], [2].

Several milestones in Particle Physics have been achieved at CERN, such as the discovery of neutral currents, W and Z bosons, the first creation of antihydrogen atoms and recently the discovery of the Higgs boson.

CERN has not only pushed the technology for accelerators and particle detectors to new dimensions over the years, but also created spin-off technologies, as for example in the field of hadron therapy for cancer [3], non-destructive testing and simulation programs and one of the most important inventions of the ‘information age’, the World Wide Web [4].

Table 1.1: CERN Member States by 2014 [5].

Member State	Status since	
Belgium	1954	
Denmark	1954	
France	1954	
Germany	1954	
Greece	1954	
Italy	1954	
Netherlands	1954	
Norway	1954	
Sweden	1954	
Switzerland	1954	
United Kingdom	1954	
Austria	1959	
Bulgaria	1999	
Czech Republic	1993	
Finland	1991	
Hungary	1992	
Israel	2014	
Portugal	1986	
Poland	1991	
Slovakia	1993	
Spain	1983	

2 CERN Accelerator Complex

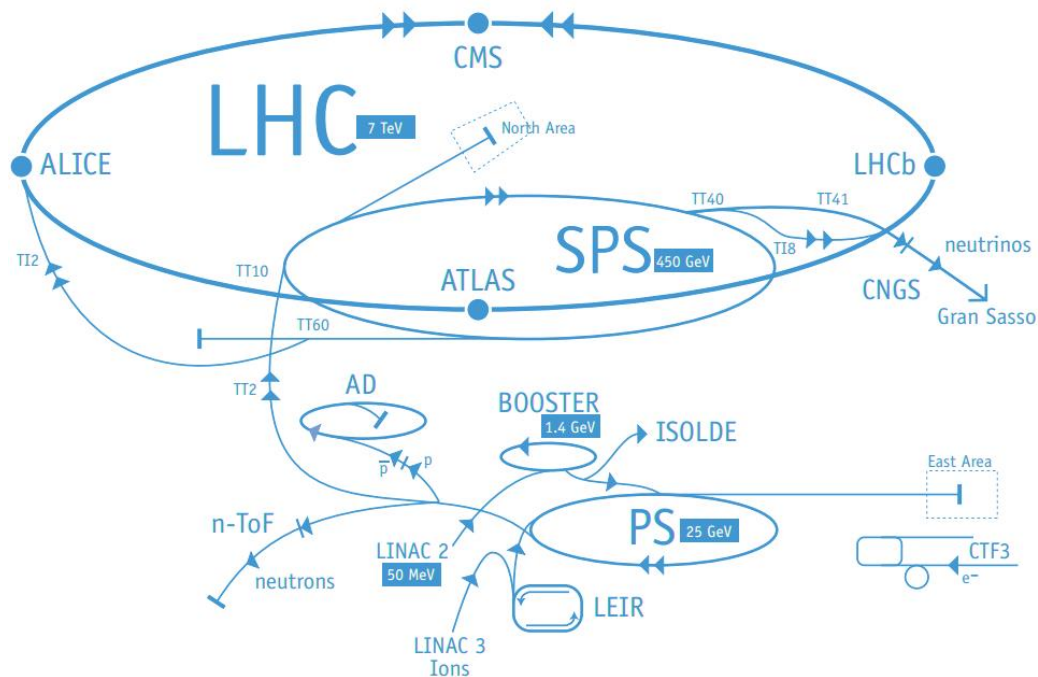


Figure 2.1: The CERN accelerator complex [6].

The LHC is the last accelerator in a chain of machines with increasingly higher energies. Figure 2.1 shows the CERN accelerator complex with the LHC and its pre-accelerators. The proton source is a bottle of hydrogen gas. Starting at LINAC2 (Linear Accelerator 2) the protons are packed in bunches, accelerated to the energy of 50 MeV. In the next step the protons enter the Proton Synchrotron Booster (PSB) from which they are transferred at the energy of 1.4 GeV into the Proton Synchrotron (PS). The PS can accelerate both protons and heavy ions from Low Energy Ion Ring (LEIR). At 25 GeV the particles enter the Super Proton Synchrotron (SPS). Nearly 7 kilometres in circumference, the SPS is the second-largest machine in CERN's accelerator complex and the last step of pre-acceleration before the particles are injected into the LHC. At this point the energy is increased to 450 GeV [7].



Figure 2.2: left to right: CERN pre-accelerators LINAC2, PS and SPS.

In the LHC a nominal beam contains up to 2808 bunches with 1.15×10^{11} protons. The single bunches are separated by 25 ns, which equals around 7.5 m of distance [7], [8].

The LHC is the world's largest particle collider. The 27 km long - approximately circular - tunnel is located on average 100 m below ground level with a total inclination of 1.4 %.

Two beams are counter rotating in ultrahigh vacuum inside two beam pipes at 0.999999991 % the speed of light and brought into collision in the so-called Interaction Regions (IRs) IR1, IR2, IR5 and IR8 at the main experiments of the LHC: ATLAS, ALICE, CMS and LHCb, see Figure 2.3.

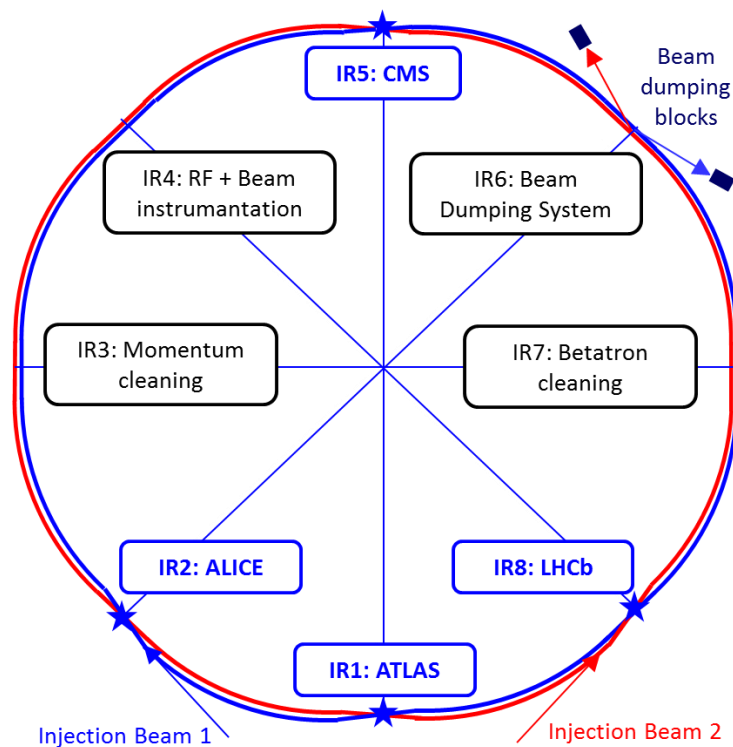


Figure 2.3: LHC schematic layout with the four main experiments: ATLAS, ALICE, CMS and LHCb [1].

At the experiments the particles collide with a total nominal energy of 14 TeV, 7 TeV per beam. The nominal intensity is 3×10^{14} protons per beam, therefore the stored energy per beam adds up to 360 MJ, comparable with the energy of about 90 kg TNT.

The two beams are injected in opposite directions in IR2 and IR8. The ‘beam cleaning’ is performed by collimators in IR3 and IR7. The LHC Beam Dumping System (LBDS) is located in IR6, where the beams can be safely extracted. The two opposing beams are accelerated by Radio Frequency (RF) cavities - eight per beam – installed in IR4. The beams are bent in the arc sections by superconducting dipole magnets. Table 2.1 provides an overview of some LHC parameters [9].

Table 2.1: Overview of LHC parameters [6], [9].

LHC Geometry		
Ring circumference	[m]	26658.883
Magnets		
Number of magnets		9593
Number of main dipoles		1232
Length of main dipoles	[m]	12.3
Dipole operating temperature	[K]	1.9
Peak magnetic dipole field	[T]	8.33
Number of main quadrupoles		392
Beam Data		
Nominal proton energy at collision	[TeV]	7
Number of particles per bunch		1.15×10^{11}
Number of bunches		2808
Stored energy per beam at collision	[MJ]	362

By 2013 the nominal proton energy at collision per beam was not reached. The maximum energy per beam collision was 3.5 TeV. During Long Shutdown 1 (LS1) from February 2013 to November 2014 the LHC operation is stopped for numerous projects and activities to maintain and upgrade the LHC to reach higher beam energy up to 6.5 TeV in 2015.

The main goal for the LHC experiments is to confirm the validity of the Standard Model, which explains electromagnetic, weak, and strong nuclear interactions. Further and theories, like Supersymmetry, not described in the Standard Model, are also part of the research fields of the LHC experiments.

A few of the unsolved questions to be examined at CERN are:

- What is the origin of mass?
- Is there Supersymmetry?
- What is Dark Matter?
- Why is the observable universe apparently composed almost entirely of ordinary matter?

- What happened at the Big Bang? [6].

The different LHC experiments are built to provide answers to these questions. An overview of the experiments can be found in the Appendix Chapter 8.5.

3 Machine Protection

The large amount of energy stored in the two beams and the superconducting magnet system of the LHC requires for a powerful machine protection system. Consequences of failures during the LHC operation might result in downtime, radioactive contamination, damage of accelerator equipment or damage of the LHC beyond reparability. To prevent these consequences the uncontrolled release of energy must be avoided. The LHC Machine Protection System (MPS) ensures a safe operation of the LHC [10].

This chapter gives an overview of the risks involved in the operation of the LHC and how they are mitigated with focus on risks and protection related to the beam of charged particles.

3.1 Stored Energy and Risks at the LHC

The bulk of the energy at the LHC is stored in the magnets and the two beams. Table 3.1 shows how this energy is distributed.

Table 3.1: Energy stored in magnets and beam for nominal LHC parameters [10].

Energy stored in each main dipole magnet	7.6 MJ
Energy stored in magnet system	10 GJ
Energy stored in main dipole circuit	1.1 GJ
Energy stored in one beam	362 MJ

For comparison: The energy needed to heat and melt one kilogram of copper is 700 kJ. With the energy stored in the magnet system it would be possible to melt almost 15 tons of copper. The energy stored in the LHC exceeds the energy of other particle accelerators by orders of magnitude. Figure 3.1 shows a comparison of the stored beam energy over the momentum in various accelerators [10].

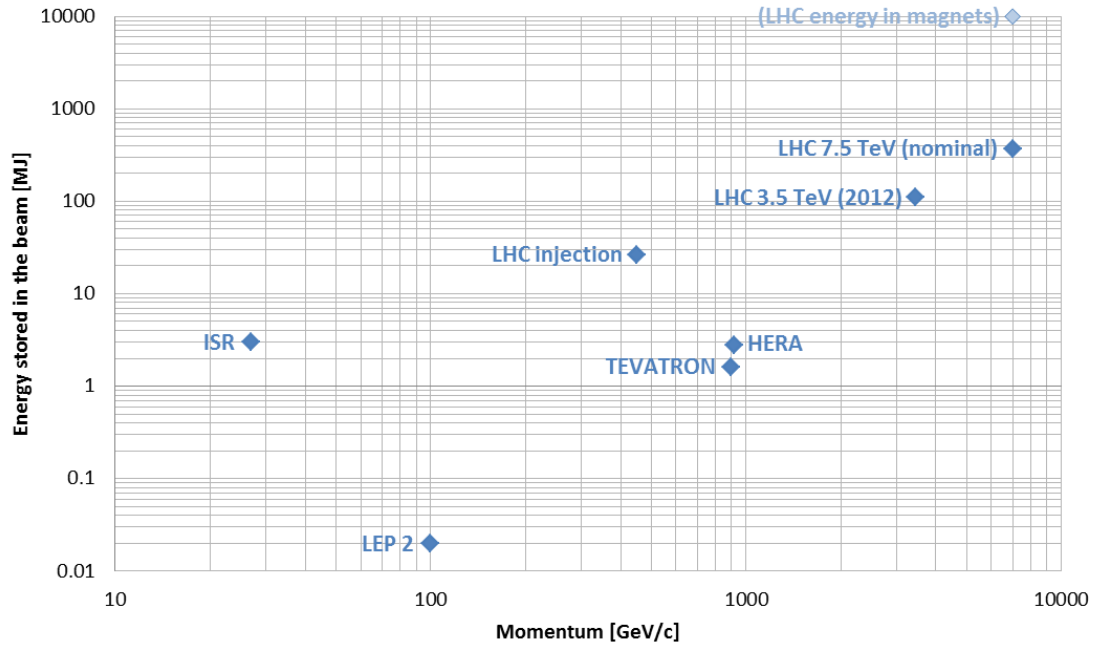


Figure 3.1: Comparison of stored beam energy in various particle accelerators.

3.1.1 Stored Energy in the Magnets

The energy stored in a magnet is given by Equation (3.1), with the inductance of the magnet L and the current I .

$$E = 0.5 \cdot L \cdot I^2 \quad (3.1)$$

At nominal beam energy each main dipole magnet stores an energy of about 7.6 MJ powered by the current $I=12$ kA. To safely handle the energy of the magnet system, the powering of the magnets is split up into eight main circuits related to the eight arcs at the LHC. One hundred and fifty-four dipoles are linked together to a main dipole circuit resulting in a stored energy of slightly over 1.1 GJ per circuit [10].

3.1.2 Stored Energy in the Beams

Due to the particle momentum of 7 TeV/c and the therefore resulting stored beam energy of 362 MJ, uncontrolled losses of even small fractions of the beam could cause magnet quenches and damage the LHC complex. Beam losses can not only directly damage the LHC equipment but also cause quenches, the loss of superconducting of a magnet.

The beam energy is calculated as followed:

$$E_{Beam} = N \cdot n_B \cdot \xi_p \quad (3.2)$$

N ... intensity per bunch

n_b ... number of bunches

ξ_p ... energy of one charged particle

Table 3.2 provides the values for Equation (3.2) at nominal operation:

Table 3.2: Beam parameters at nominal operation.

Formula Symbol	Value
N	$1.15 \cdot 10^{11}$
n_B	2808
ξ_p	7 TeV
E_{Beam}	362 MJ

3.2 Overview of Machine Protection at the LHC

The LHC Machine Protection System consists of a variety of independent subsystems and protects the LHC against the risk of damage due to the sudden release of energy from the beam or the magnet system. Figure 3.2 shows the schematic of the functionality of the LHC MPS and the interdependency of the different sub-systems.

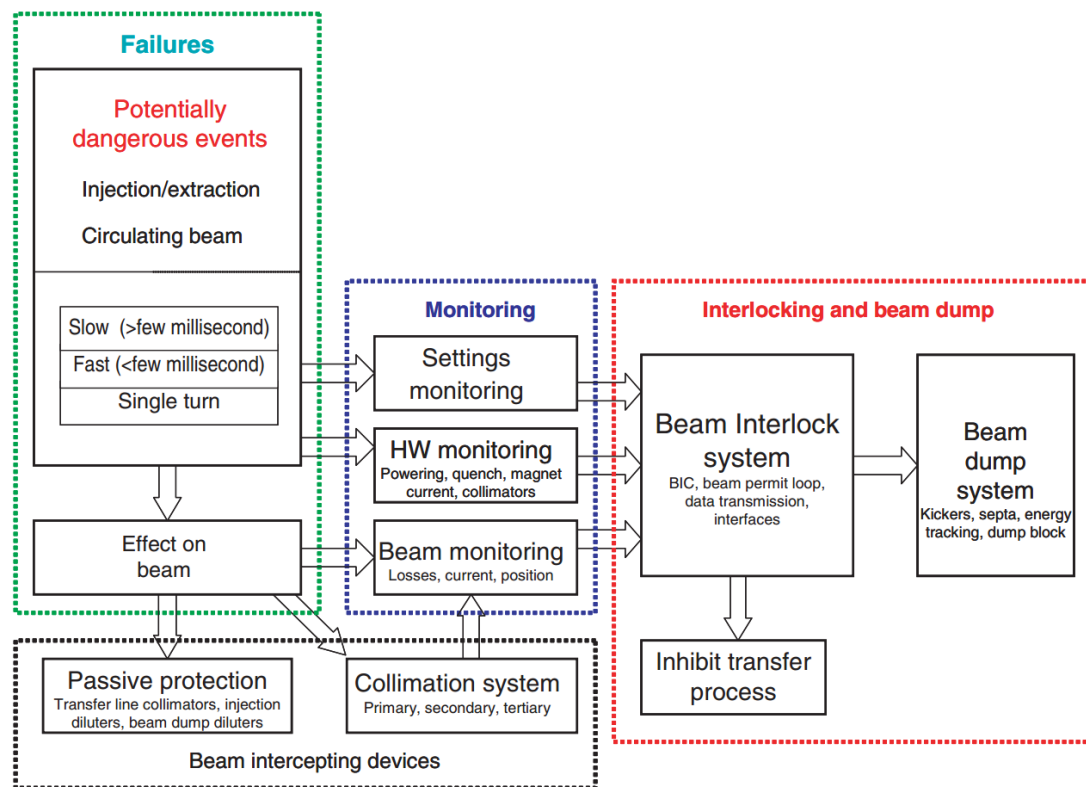


Figure 3.2: The functional blocks of the LHC machine protection system [10].

The LHC MPS continuously checks if the conditions for a safe operation are fulfilled. If these are violated, the MPS dumps the beam. Thus, the beam operation is aborted the MPS also prohibits the injection of unsafe beam intensities if the conditions for safe operation are not fulfilled.

The MPS consists of (see Figure 3.2):

- Systems **monitoring equipment** and beam parameters, e.g. Beam Loss Monitors and Beam Position Monitors. These systems can request a mission abort by sending a beam dump request to the Beam Dumping System via the Beam Interlock System.
- A **Beam Interlock System** to transmit safe condition and dump requests to the LHC Beam Dumping System (see next sub-chapter).
- The **LHC Beam Dumping System** to extract the beams safely in case of a dump request (see Chapter 3.4).
- A collimation system to passively protect magnets against quenches produced by beam losses and damage due to **ultra-fast failures** (less than 3 turns or 250 μ s) [10].

The overall Safety Integrity Level (SIL) of the LHC Machine Protections System exceeds SIL3 as specified in the IEC EN 61508 standard [11]. Table 3.3 provides the failure rates to the four Safety Integrity Levels, from SIL1 to SIL4 with increasing dependability.

Table 3.3: Safety Integrity Levels and according failure probability [11].

SIL	Failure Probability per hour
SIL1	$10^{-5} - 10^{-6}$
SIL2	$10^{-6} - 10^{-7}$
SIL3	$10^{-7} - 10^{-8}$
SIL4	$10^{-8} - 10^{-9}$

The SIL for a system is not only dependant on the failure probability but also on the consequences for an occurring failure. For LHC operation the consequences are rated financially and in terms of efficiency. The four classes for consequences are:

- **Catastrophic**
Consequences can damage the several LHC collimators and superconducting magnets.
- **Critical**
Consequences can damage one or more superconducting magnets.
- **Marginal**
Consequences can destruct collimator jaws.
- **Negligible**
Consequences do not necessarily result in costly damage but reduce efficiency.

Table 3.4 provides a matrix for the SIL based on frequency and consequences.

Table 3.4: SIL Requirements after Risk Classification [11].

		Consequence			
Frequency	Per year	Catastrophic	Critical	Marginal	Negligible
Frequent	1	SIL4	SIL3	SIL3	SIL2
Probable	0.1	SIL3	SIL3	SIL3	SIL2
Occasional	0.01	SIL3	SIL3	SIL2	SIL1
Remote	0.001	SIL3	SIL2	SIL2	SIL1
Improbable	0.0001	SIL3	SIL2	SIL1	SIL1
Not Credible	0.00001	SIL2	SIL1	SIL1	SIL1
Cost [Millions of CHF]		>50	1-50	0.1-1	0-0.1
Downtime [days]		>180	20-180	3-20	0-3

The Beam Interlock System and the Beam Dumping System is explained in more detail in the following sub-chapters.

3.3 The Beam Interlock System (BIS)

The LHC Beam Interlock System gathers information from its clients (users) to provide the beam permit flag for each beam (see list below). The beam permit is given if all users are ready for operation with beam.

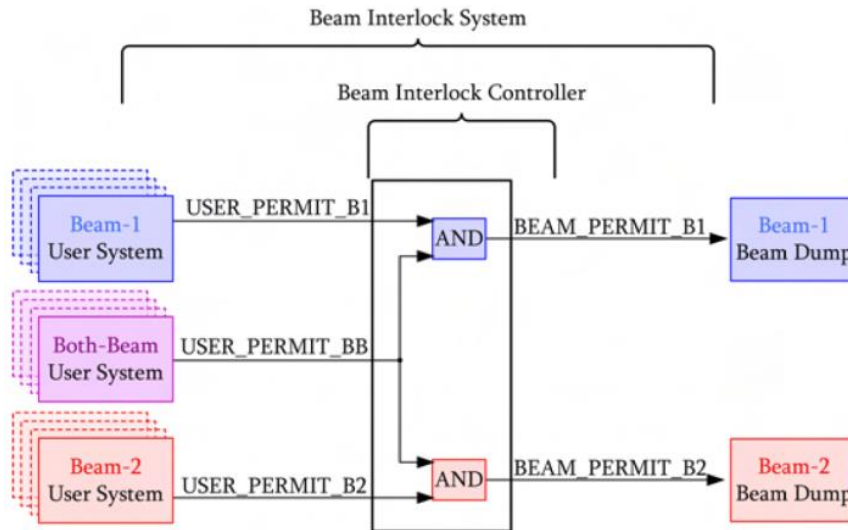


Figure 3.3: Simplified Architecture of the Beam Interlock System [12].

Figure 3.3 shows the schematic layout of the LHC Beam Interlock System. User systems can interlock each beam individually (**Beam-1** and **Beam-2**) or both beams simultaneously (**Both-Beam**). The user permit signals (USER_PERMIT_B1, USER_PERMIT_BB, USER_PERMIT_B2) are forwarded to the Beam Interlock Controllers (BIC).

In total 16 BICs are installed in the LHC tunnel. A 10 MHz signal (BEAM_PERMIT_B1, BEAM_PERMIT_B2) is forwarded between the BICs, clockwise and counter-clockwise, indicating the presence of the beam permit.

Two permit loop generators (CIBG), each with a pair of optical transceivers (CIBO), generate the beam permit signal for each beam. In case of deviation from this signal the beam permit is lost and the BICs around IP6 will trigger the LHC Beam Dumping System (**Beam-1 Beam Dump** and **Beam-2 Beam Dump**) to extract the beam.

Figure 3.4 shows the distribution of the BICs in the LHC, one on the right and left side of each IR. A 17th BIC is installed in the CERN Control Centre to interrupt the BIS loop manually. The BICs are connected by redundant optical fibre links, two per beam, the so called Beam permit loops [9], [12].

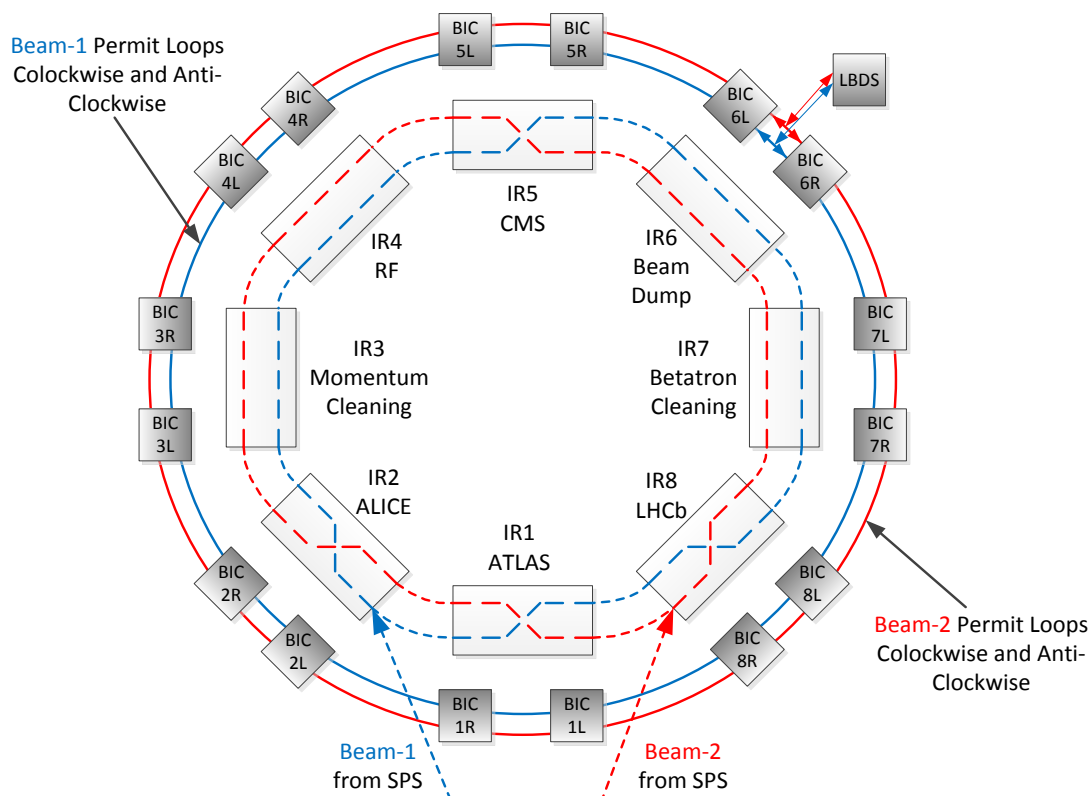


Figure 3.4: Beam permit loops and the BIC distribution around the LHC [12].

Users of the BIS are:

- Powering interlock controllers for superconducting magnets (PIC)
- Powering interlock controllers for normal conducting magnets (WIC)
- LHC experiments
- Radio Frequency System (RF)
- Beam Loss Monitors (BLM)
- Beam Position Monitors (BPM)
- Access System
- Vacuum System (VAC)
- Collimation System (COLL)
- Software Interlock System (SIS)
- Injection System (INJ)
- LHC Beam Dumping System (LBDS)

3.4 The LHC Beam Dumping System (LBDS)

The LHC Beam Dumping System is an essential part of the MPS, which guarantees the safe extraction of the stored beams when the operation has to be interrupted.

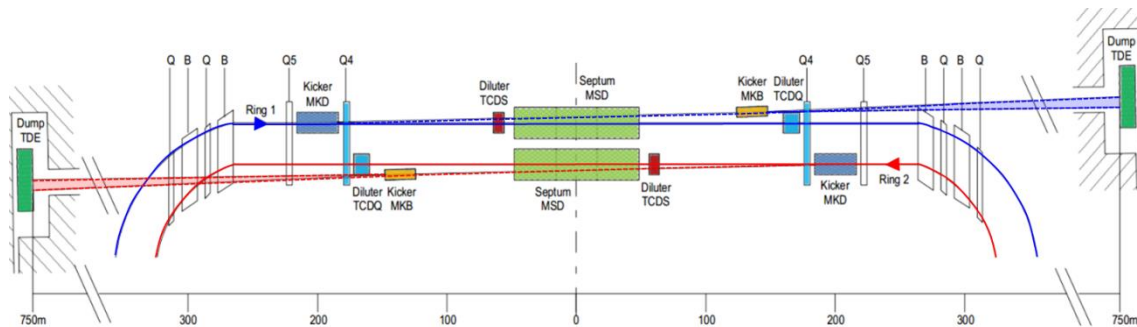


Figure 3.5: Layout of the elements of the LBDS in IR6 [9].

Figure 3.5 shows the layout of the LBDS in IR6 for both beams, rotating clockwise (blue line) and counter-clockwise (red line). The LBDS consist of following accelerator components for each beam [9]:

- Fifteen fast pulsed ejection dump kicker magnet assemblies (MKD):**
 The kicker magnets deflect the entire beam by 0.280 mrad horizontally into the high-field of the Septum Magnet (MSD, see below). The time for the kicker magnets to rise to their nominal energy (rise-time) is less than 3 μs . The kicker rise is synchronised with the particle free gap in the LHC filling pattern which has a length of 3 μs ¹, the so-called abort gap. This is to ensure that all particles are deflected with the full magnet energy and extracted from the LHC.
- Fifteen ejection dump septum magnets (MSD):**
 The MSDs provide a vertical deflection of 2.400 mrad to raise the beam above the cryostat.
- Ten diluter dump kickers (MKB):**
 The MKBs are used to shape the beam into an 'e'-profile (compare Figure 3.6). The bunches are deflected in both, horizontal and vertical directions to dilute the energy density on the dump block due to the impacting beam.
- One dump block (TDE):**
 The TDE is a 7 m long massive graphite dump block located in a cavern at the end of the 975 m long extraction vacuum dump line. It is covered with 1000 t of concrete shielding and the only structure in the LHC complex built to absorb the full beam energy. For nominal beam parameters, the temperature in the TDE is expected to rise up to about 750 °C. To avoid fire the dump is surrounded by nitrogen gas.
- Target Collimator Dump Septum (TCDS):**
 The TCDS is a passive element to protect the septum magnets in case of a beam abort that is not synchronised with the abort gap.

¹ A gap of 3 μs at the speed of light equals about 900 m.

- **Quadrupole magnet Q4 and Target Collimator Dump Quadrupole (TCDQ):**
During a beam abort the quadrupole is additionally to the MKDs used to deflect the beam horizontally. Including the deflection from the MKDs, the total horizontal deflection is 0.300 mrad. The quadrupole is passively protected by the TCDQ.

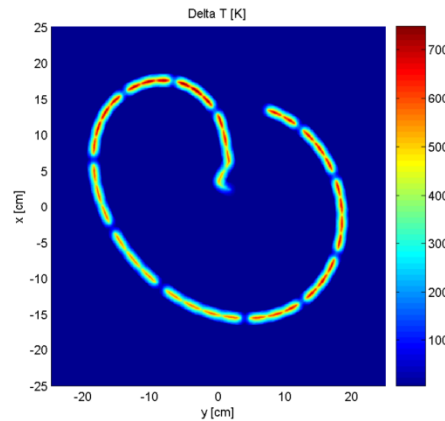


Figure 3.6: Temperature increase in the beam dump block after full beam impact. Notice the e-shape formed by the diluter dump kickers (MKB) [10].

To ensure safe extraction of all particles of the beam, following conditions have to be fulfilled [10]:

- At least fourteen of the fifteen MKDs must operate correctly.
- The MKD rise must be synchronized with the 3 μ s abort gap.
- The beam energy must be tracked by the Beam Energy Meter System (BEMS) and the Beam Energy Tracking System (BETS) and the data must be provided to the MKDs, MKBs and MSDs for proper deflection.
- The closed orbit errors in the dump insertion must be limited to about 4 mm.

Figure 3.7 shows the signal distribution in the central electronics of the LBDS in case of a dump request from the BIS for one beam before LS1.

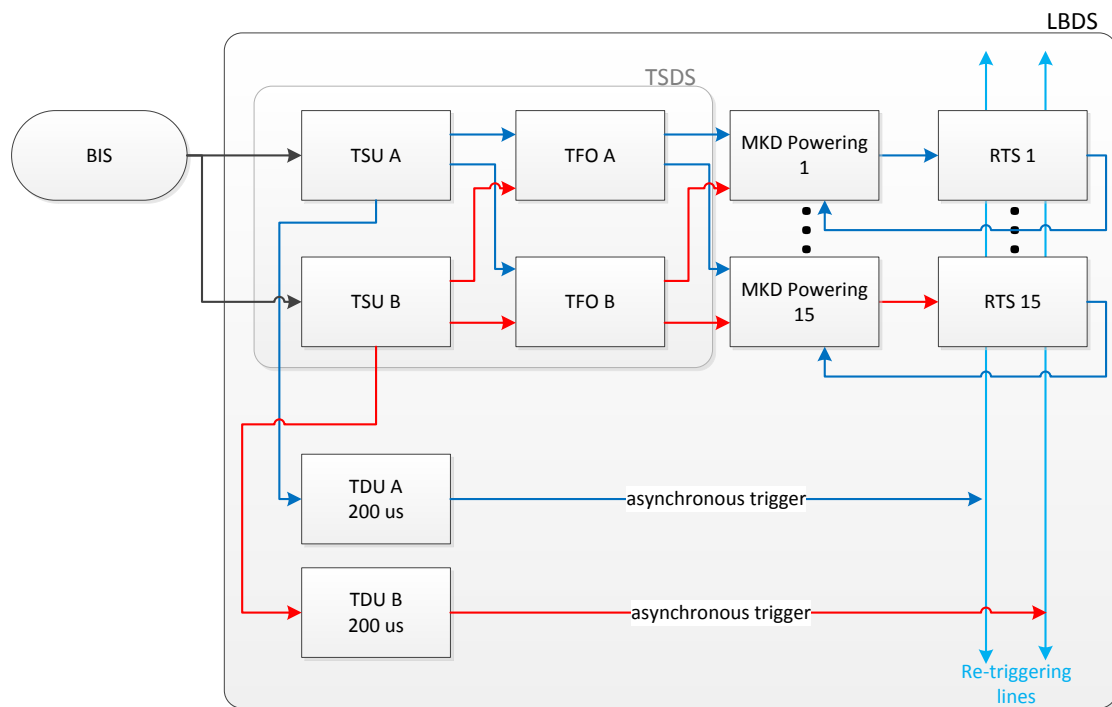


Figure 3.7: Signal distribution in the LBDS.

The functions of the different elements of the central electronics of the LBDS are the following [13]:

- **Trigger Synchronisation Unit (TSU):**
 1. The redundant TSUs will detect a beam dump request from the BIS, synchronise the request with the abort gap and then forward the request to the Trigger Fan-Outs.
 2. Every time the TSU detects a beam dump request, it will trigger the Trigger Delay Unit (TDU) immediately. The trigger sent to the TDU is not synchronised with the abort gap (asynchronous trigger).
- **Trigger Fan-Out (TFO):**

Two redundant TFOs are used to distribute the synchronous dump request to the 15 MKDs, more precisely to the power transfer units (PTU) for the MKDs. The TFOs receive a signal from each TSU. The combination of TSUs and TFOs is called the Trigger Synchronisation and Distribution System (TSDS).
- **MKD Powering:**

Each MKD is activated by redundant PTUs. One PTU will trigger two pulse generators. The PTUs are also connected to the Re-triggering lines.
- **Re-triggering System (RTS):**

The Re-triggering System is another protection layer in the LBDS. As soon as one kicker magnet fires, the Re-triggering system will trigger immediately all PTUs via the Re-triggering Lines. This is to protect the LHC from beam impact

due to a spurious trigger in one kicker magnet. More details can be found in the following sub-section.

- **Trigger Delay Unit (TDU):**

The TDU is triggered immediately through the TSU when the beam permit flag is lost. It delays the incoming signal for 200 μs and then generates an asynchronous trigger directly to the Re-triggering Lines. The Trigger Delay Unit is discussed in greater detail in Chapter 5.2.

The failure modes of the LBDS will be discussed in Chapter 5.1. For a deeper analysis of the LBDS dependability see also ‘Dependability Analysis of a Safety Critical System: The LHC Beam Dumping System at CERN’ [8].

3.4.1 The Re-triggering System

The Re-triggering System is a protection system in case of erratic triggers in the MKDs. If one MKD fires ‘spontaneously’ as a consequence of a failure, the remaining 14 MKDs are triggered with a maximum delay of 750 ns via the Re-triggering Lines. In addition the Re-triggering System is also used to distribute an Asynchronous Beam Dump request from the TDUs 200 μs after the Synchronous Beam Dump request in case of a global failure of the trigger distribution system (TFOs).

An Asynchronous Beam Dump is not synchronised with the abort gap and could therefore produce beam losses that could impact the magnets and the arc aperture due to a scattered beam.

The System itself consists of two independent Re-triggering Lines for each beam and two Re-triggering Boxes (RTB) for each MKD. The RTBs can trigger the powering system of the MKDs.

The Re-triggering System is activated by a rising edge crossing at least 7.5 V. After every beam dump event the presence of the re-trigger signals are checked to verify the correct behaviour of the system [8], [13].

3.5 Direct Link from the BIS to the LBDS Re-triggering Lines

The Trigger Synchronisation and Distribution System (TSDS) and in particular the TSUs are designed redundantly, but can be a single point of failure in case of a common failure mode for the safe extraction of the beam on demand from the LHC BIS. Although the system has been analysed and failure rates have been calculated, a common failure mode in the 12 V power distribution inside the TSU crate was identified. The problem was discovered in the lab, during preparation for the ‘LBDS powering review’ and the beam operation was stopped

until a temporary supervision of the 12 V power supply was implemented. A persistent short-circuit in the +12 V power supply would result in a complete loss of triggering capabilities (synchronous & asynchronous) of both TSUs. The failure would inhibit the dump trigger signal distribution to the TFOs and the TSUs. Thus, there would be no way to safely dump the beam. This is a catastrophic failure scenario which has to be avoided under all circumstances [14].

During LS1 the redundancy of the 12 V power supply will be ensured. As an additional safety level for unknown common failure modes in the TSDS, a connection from the BIS directly to the Re-triggering Lines is foreseen and will also be installed during LS1. This connection will bypass the TSDS and forward asynchronous triggers directly to the Re-triggering System.

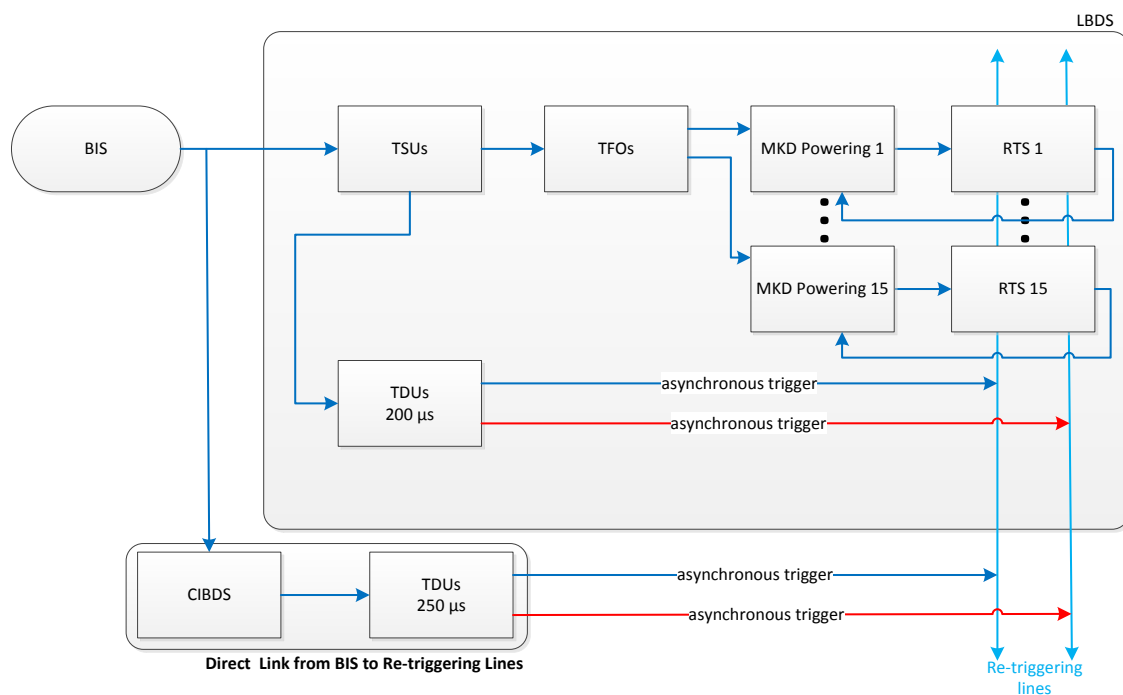


Figure 3.8: Integration of the Direct Link from the BIS to the Re-triggering Lines.

The new system (Direct Link from BIS to Re-triggering Lines in Figure 3.8) will trigger after 250 μs with a tolerance of $\pm 10 \mu\text{s}$. The delay of 250 μs gives enough time to the LBDS to trigger synchronously via the TSDS and asynchronously after 200 μs via the TDUs.

Since this is the third layer of protection after the synchronous trigger and the 200 μs delayed asynchronous trigger, most concerns lie on the impact it could have on machine availability. The installation can cause additional unwanted beam dumps as well as downtime due to component failures requiring replacement of the hardware. Therefore requirements for the new link have been defined [15]. The overall system integration for each beam should not cause more than

- **one Asynchronous Beam Dump every ten years of operation** and
- **two Synchronous Beam Dumps per year.**

To verify these requirements a reliability analysis of the planned system is necessary. It focuses on unwanted beam dumps but covers also other failure modes of the new direct link from the BIS to the Re-triggering Lines.

The new link will consist of two hardware systems with different functions: The Beam Interlock Controller Dumping System (CIBDS) and the Trigger Delay Unit 250 μ s (TDU250).

The main purpose of the TDU250 in the new link is, as the name implies, to delay an incoming signal for 250 μ s as discussed above. Trigger Delay Units are already used in the LBDS to delay a signal for 200 μ s. The new TDU250 is based on the 200 μ s TDU with small adaptations.

The CIBDS will listen to the BIS loop frequency and generate a pulse for the TDU in case of lost beam permit.

The details of the new direct link between the BIS and the LBDS Re-triggering System will be discussed in Chapter 5.

4 Introduction to Reliability

According to the IEEE Standard 610 reliability is defined as

‘The ability of a system or component to perform its required functions under stated conditions for a specified period of time’ [16].

In engineering qualitative as well as quantitative methods are applied to describe the reliability of products, systems and components. Chapter 4 gives an overview of the methods used in this thesis.

4.1 Mathematics of Reliability

Failure times of components and systems can be interpreted as random variables following the rules of probability theory. This sub-chapter describes basic statistical terms and their relevance in reliability analysis.

The **empirical mean** t_m describes the average failure time of identical systems i which fail after times t_i :

$$t_m = \frac{1}{n} \sum_{i=1}^n t_i. \quad (4.1)$$

The **variance** s^2 is a measure for the statistical spread of the failure times t_i around t_m .

$$s^2 = \frac{1}{n-1} \sum_{i=1}^n (t_i - t_m)^2. \quad (4.2)$$

The **standard deviation** s is the square root of the variance. In contrast to the variance, the standard deviation has the same dimension as the failure time.

$$s = \sqrt{s^2}. \quad (4.3)$$

The **density function** $f(t)$ is the distribution of failures over time. The three most common distributions in reliability theory are the normal distribution, the exponential distribution and the Weibull distribution.

The **failure probability** $F(t)$ is defined as:

$$F(t) = \int_0^t f(t)dt. \quad (4.4)$$

The **failure probability** $F(t)$ describes the probability for a failure to occur within a specific time.

The time where the failure probability $F(t)$ for a system is 50% is called the **median** t_{median} .

$$F(t_{median}) = 0.5. \quad (4.5)$$

The **mode** t_{modal} describes most occurring failure time. Using the density function $f(t)$ for failures, the mode is located at the maximum turning point of the density function.

$$f'(t_{modal}) = 0. \quad (4.6)$$

Figure 4.1 shows the mode, median and mean time in the density function.

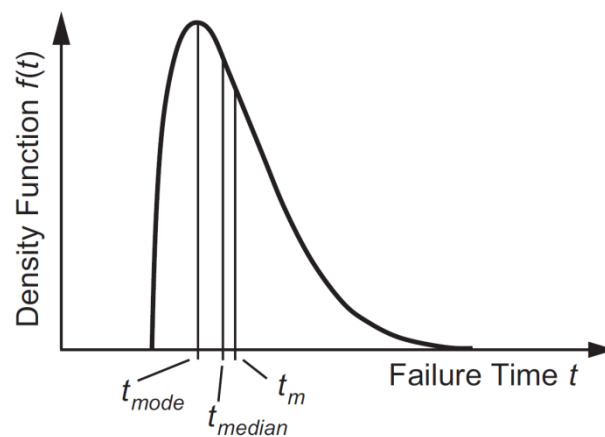


Figure 4.1: Density function with mean, median and mode [17]

The complement of the failure probability is defined as the survival probability or the **reliability** $R(t)$. The reliability function gives the probability for a device not failing prior to the time t and is given by

$$R(t) = 1 - F(t) = 1 - \int_0^t f(t)dt. \quad (4.7)$$

The **failure rate** $\lambda(t)$ is defined as the frequency of system failures:

$$\lambda(t) = \frac{f(t)}{R(t)}. \quad (4.8)$$

For electronic components failure rates are often given in the unit failures in time (FIT). FIT is defined as the number of failures expected in 10^9 h of operation.

The **mean time to failure** *MTTF* describes the expected average time until a failure occurs:

$$MTTF = \int_0^\infty R(t)dt. \quad (4.9)$$

In the special case of constant failure rates the *MTTF* can be described as the inverse of the failure rate:

$$MTTF(\lambda = const) = \frac{1}{\lambda}. \quad (4.10)$$

4.1.1 Normal Distribution

The normal distribution is axially symmetric to the mean, which is congruent to the median and the mode. The density function of the normal distribution is described by

$$f(t) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{(t-\mu)^2}{2\sigma^2}} \quad (4.11)$$

where σ is a scale parameter and μ is the mean of the function. Figure 4.2 shows the probability density function $f(t)$, the failure probability $F(t)$, the reliability $R(t)$ and the failure rate $\lambda(t)$ of the normal distribution for scale parameters $\sigma = 0.5$, $\sigma = 1$ and $\sigma = 2$.

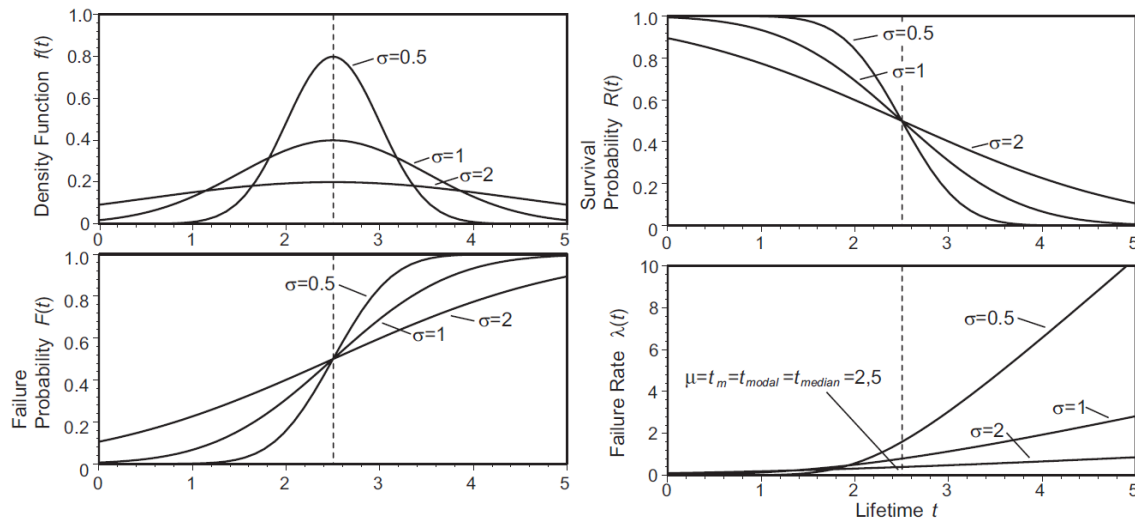


Figure 4.2: Density function, failure probability, survival probability and failure rate of the normal distribution for different values of σ [17].

4.1.2 Exponential Distribution

The exponential distribution is the most common distribution adopted to describe the failure behaviour of electronic components. The only failure rate in the exponential distribution is constant. This depicts random failures over the whole component lifetime. The density function of the exponential distribution is described by

$$f(t) = \lambda e^{-\lambda t} \quad (4.12)$$

$$\text{with} \quad \lambda = \frac{1}{t_m} = \text{const.} \quad (4.13)$$

The reliability and the failure probability of the exponential distribution are defined as

$$R(t) = e^{-\lambda t} \quad (4.14)$$

$$\text{and} \quad F(t) = 1 - e^{-\lambda t}. \quad (4.15)$$

It can be seen that for $t = t_m$ the reliability is $R(t = t_m) = 36.8\%$ and therefore the failure probability $F(t = t_m) = 63.2\%$.

Figure 4.3 depicts the density function, failure probability and the reliability for different failure rates of the exponential distribution.

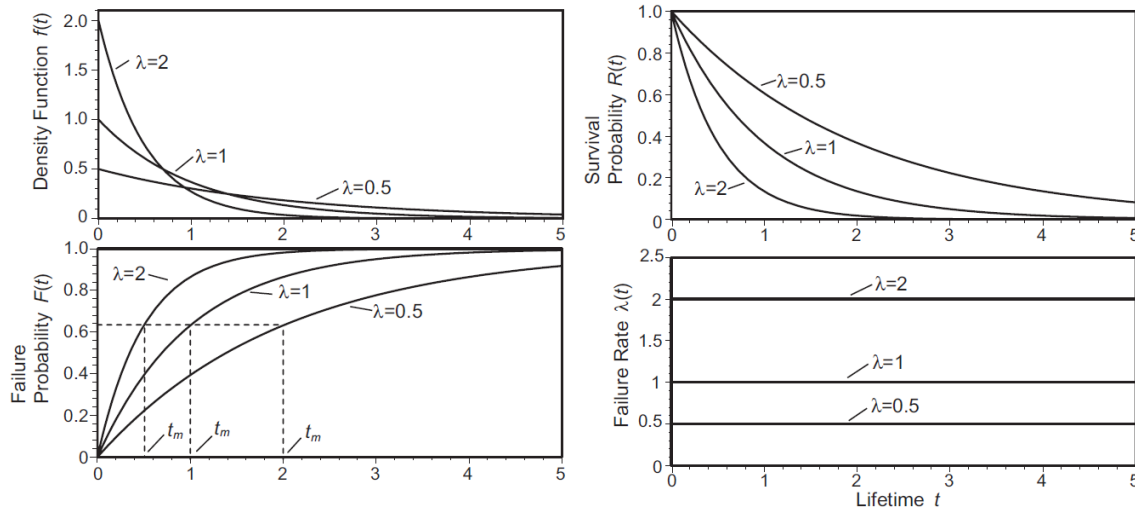


Figure 4.3: Density function, failure probability, survival probability and failure rate of the exponential distribution [17].

4.1.3 Weibull Distribution

The density function of the two-parametric Weibull distribution is defined as

$$f(t) = \frac{b}{T} \left(\frac{t}{T} \right)^{b-1} \cdot e^{-\left(\frac{t}{T} \right)^b}. \quad (4.16)$$

The form of the Weibull distribution density function changes drastically with the value of the shape parameter b . The shape parameter b determines the shape of the curve (see Figure 4.4). The characteristic lifetime T is a scale parameter.

Reliability, failure probability and the failure rate for two-parametric Weibull distribution are described by following equations.

$$R(t) = e^{-\left(\frac{t}{T} \right)^b}. \quad (4.17)$$

$$F(t) = 1 - e^{-\left(\frac{t}{T} \right)^b}. \quad (4.18)$$

$$\lambda(t) = \frac{b}{T} \left(\frac{t}{T} \right)^{b-1}. \quad (4.19)$$

Similar to the exponential distribution, the failure probability for $t = T$ is $F(t = T) = 63.2\%$. Figure 4.4 shows the density function, failure probability, survival probability and failure rate of the Weibull distribution for various shape parameters b .

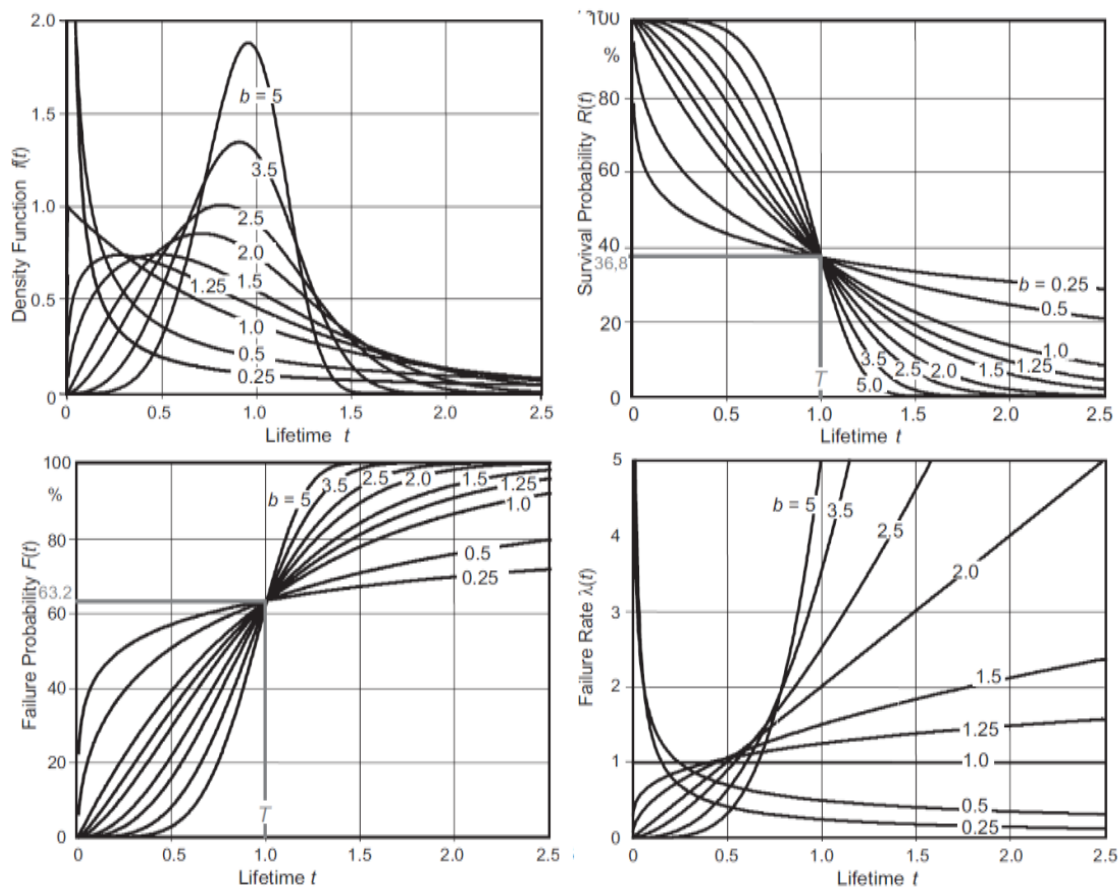


Figure 4.4: Density function, failure probability, survival probability and failure rate of the Weibull distribution [17]

In addition to the two-parametric Weibull distribution, there is also a three-parametric Weibull distribution. The third parameter describes a failure free time t_0 [17].

4.2 Reliability of Electronic Components

Figure 4.5 depicts the so-called bathtub curve which is used to describe the failure behaviour of electronic components.

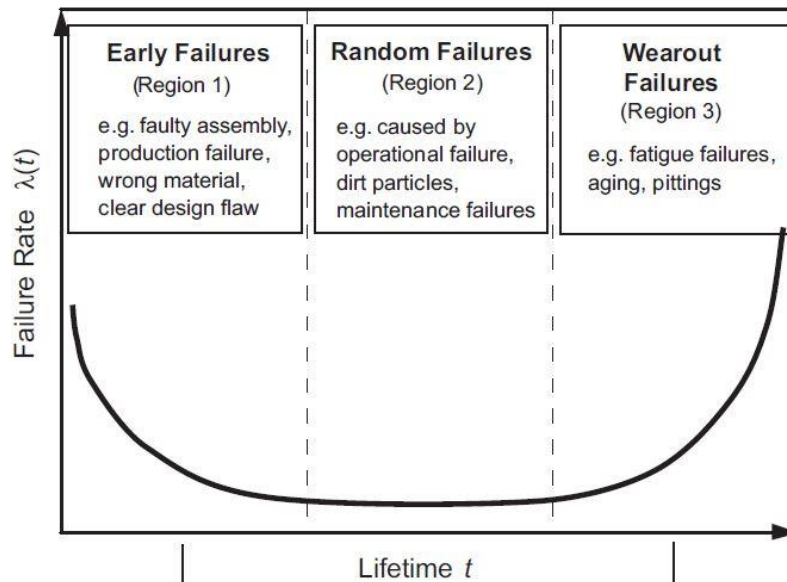


Figure 4.5: Bathtub curve [17]

Three different regions can be identified in the bathtub curve:

- The first region describes early lifetime failures caused mainly by assembly failures or material failures. The failure rate constantly decreases over time.
- In region two the failure rate stays constant. During this phase all failures are assumed to be random. This region is also called the useful lifetime of components.
- The third region describes the failure rates due to wearout. The failure rate in this region increases over time.

Almost all commercial electronic components are pre-tested. This so called burn in test is specified in MIL-STD-883 [18]. Therefore, to estimate failures over time of electronic components and systems constant failure rates can be assumed.

In this thesis two methods are used to derive the failure rates of electronic components.

The first method consists in the calculation of the component failure rates by using the prediction methodology of the Military Handbook for 'Reliability Prediction of Electronic Equipment' (MIL-HDBK-217F) [19]. The *Military Handbook* is widely used for the prediction of failure rates. It uses basic failure rates of different component types (such as integrated circuits (ICs), transistors, diodes, resistors, capacitors, relays, connectors, etc.) based on field data and weighs this failure rate with different factors, e.g. environmental, quality or stress factors. The calculation method of the Military Handbook is included in ISOGRAPH, a software tool for reliability analysis explained in the next sub-chapter.

Since the last update of the *Military Handbook* was 1995 and the fast development of electronic components, especially of semi-conductors, the calculated failure rates can be assumed conservative. Many manufacturers audit their components and provide failure rates gained by accelerated lifetime test.

If this information was available, it has been exploited in addition in the reliability analysis of the components used in the new link between BIS and LBDS.

The failure rates for the components from the *Military Handbook* can vary vastly compared to the manufacturer data.

The failure modes of the components are based on the 'Electronic Reliability Design Handbook' MIL-HDBK-338B [20] and can be found in the Appendix Chapter 8.1.

The calculation method form MIL-HDBK-217F is integrated in the software tool Isograph used in the reliability analysis of the new link between the BIS and the LBDS.

4.3 Isograph

The Isograph Reliability Workbench is a software tool for reliability predictions. It features (amongst others) modules for Failure Mode, Effects and Criticality Analysis (FMECA), Failure Mode and Effects Analysis (FMEA), Fault Tree Analysis (FTA), Weibull Analysis of historical failure data and Reliability Block Diagram Analysis.

Isograph includes a parts library for electronic components based on MIL-HDBK-217F. The prediction module allows calculating the failure rates for the chosen component under defined conditions.

The components and the according failure rates from the prediction module can be exported to the FMECA module. This allows assigning failure modes to the components and defining the failure effects on component level as well as their impact on a system level [21].

In addition the Fault Tree Analysis tool was used to define the failure modes of the LBDS in this thesis.

4.4 Cadence OrCAD Solutions

In order to estimate the impact of component failures on the system behavior, the software modules OrCAD Capture in conjunction with PSpice in Cadence OrCAD Solutions were used to design electrical circuits and simulate behaviors of the hardware for different component failure modes. Examples for the usage of OrCAD Capture in this thesis are given in Chapter 5.

4.5 Fault Tree Analysis

The Fault Tree Analysis and the resulting Fault Tree diagrams represent logical relationships between sub-systems leading to a defined system state, mostly a fault state.

Fault Trees are made using the Top-Down principle. Figure 4.6 shows a general example of a Fault Tree. The top event is the undesired system failure. In the next step possible failures of subsystems leading to the top event are defined. This step is repeated until the lowest subsystem failure is defined, the so called basic event. The different events are connected by logical gates [17].

It is also possible to assign failure and repair data to the system components to gain quantitative information about the failure behaviour of a system.

There are different symbolisms established for the use in the Fault Tree Analysis. The symbolism adopted by Isograph is shown in Figure 4.6.

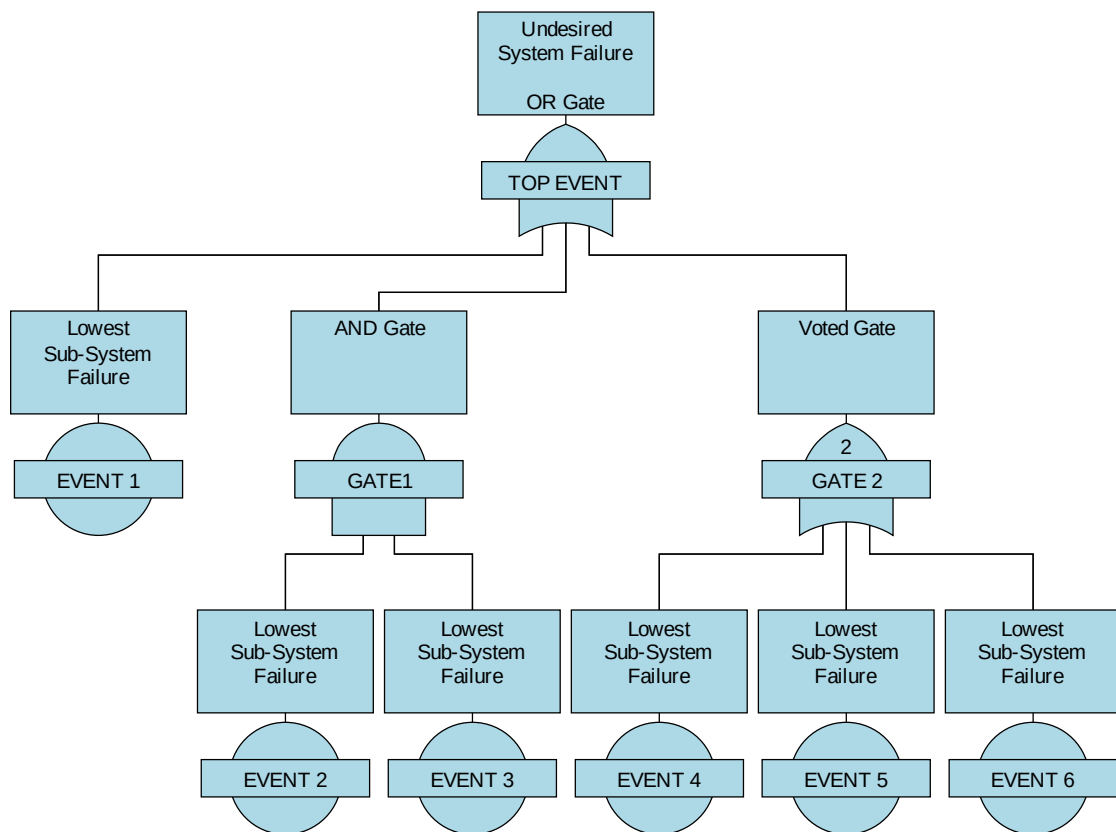


Figure 4.6: Fault Tree in Isograph.

The top event is connected to its subsystem by an OR gate. The events in the circles (Event 1-Event 6) represent failures of the lowest sub-system. The rectangles mark comments on the event. The top event is true if one of the lower events is true:

$$\textit{Top Event} = \textit{Event 1 OR Gate 1 OR Gate 2.} \quad (4.20)$$

Gate 1 is true if both, Event 1 and Event 2 are true. This AND gate can be described as:

$$\textit{Gate 1} = \textit{Event 2 AND Event 3.} \quad (4.21)$$

Gate 2 is a voted gate, marked by the '2' in the gate symbol. It turns true if at least two events are true.

$$\begin{aligned} \textit{Gate 2} = & (\textit{Event 4 AND Event 5}) \textit{ OR } (\textit{Event 5 AND Event 6}) \textit{ OR} \\ & (\textit{Event 4 AND Event 6}) \textit{ OR } (\textit{Event 4 AND Event 5 AND Event 6}). \end{aligned} \quad (4.22)$$

4.6 Failure Mode, Effects, and Criticality Analysis

The Failure Mode, Effects, and Criticality Analysis (FMECA) is a standardised and iterative method for identifying potential failure modes of a system and assigning severities to their consequences. An FMECA module is included in Isograph based on the Military Standard 1629 [22].

The general FMECA procedure includes eight steps:

1. Defining the system;
2. Constructing hierarchical block diagrams;
3. Identifying failure modes of sub-systems;
4. Assigning effects on different system levels to the identified failure modes;
5. Assigning severities to the effects;
6. Assigning quantitative failure mode data, especially failure rates;
7. Rank failure modes in terms of severity and criticality;
8. Producing reports of the analysis.

The FMECA was carried out separately for the two systems in new link from the BIS to the LBDS, the CIBDS and the TDU.

The prediction tool of ISOGRAPH assigns failure rates to components before their failure modes are defined.

Failure modes are assigned to the assembled components according to MIL-HDBK-338B [20]. The failure effects (e.g. Synchronous Beam Dump) of the failed components are defined. The overall failure rate is then split according to the different failure modes as suggested in MIL-HDBK-338B [20]. An example for a resistor failure is given in Table 4.1.

Table 4.1: Resistor failure rates and failure modes according to MIL-HDBK-338B [20].

Component	Failure Rate λ	Failure Mode	Ratio α
Resistor, Film	15.09 FIT	Open	59%
		Parameter Change	36%
		Short	5%

Therefore the failure rate for an open resistor is:

$$\lambda_{Res.,Open} = \alpha_{Open} \cdot \lambda_{Res.} = 0.59 \cdot 15.09 \text{ FIT} = 8.90 \text{ FIT}. \quad (4.23)$$

Severity classification and criticality ranking are standardised in Military Standard 882 [23] but can be customized for the application.

5 Reliability of the Direct Link from the BIS to the LBDS Re-triggering Lines

In this chapter the failure modes of the LBDS will be discussed by means of a Fault Tree Analysis (FTA). The LBDS failure modes are at the same time failure effects of the new direct link from the BIS to the Re-triggering Lines. Figure 5.1 shows an example for the failure mode Asynchronous Beam Dump of the LBDS. The Asynchronous Beam Dump will cause LHC downtime to analyse the origin of the failure and might require maintenance (failure effect). At the same time, the failure mode of the LBDS is a failure effect of a TDU failure (higher level failure effect).

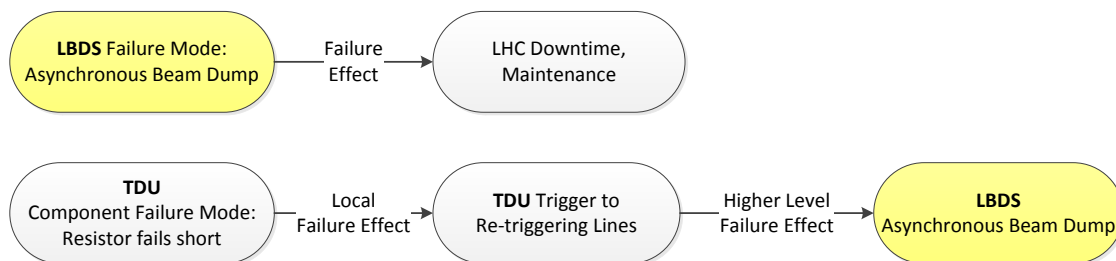


Figure 5.1: Top: example of LBDS failure mode and effect. Bottom: TDU failure mode and effect. The TDU failure effect on a higher level is at the same time a failure mode of the LBDS.

In the second part of this chapter the reliability analysis of the Trigger Delay Unit 250 μ s (TDU250) and the Beam Interlock Controller Dumping System (CIBDS) will be discussed.

5.1 Failure Modes of the LBDS

The Fault Tree Analysis for the LBDS is focusing on internal failures causing beam dumps and unavailability of the system.

5.1.1 Asynchronous Beam Dump

The first level of failures in the LBDS leading to an Asynchronous Beam Dump is shown in Figure 5.2. The triangles indicate that the event has a sub event. The yellow event indicates the contribution of the new link to this failure mode.

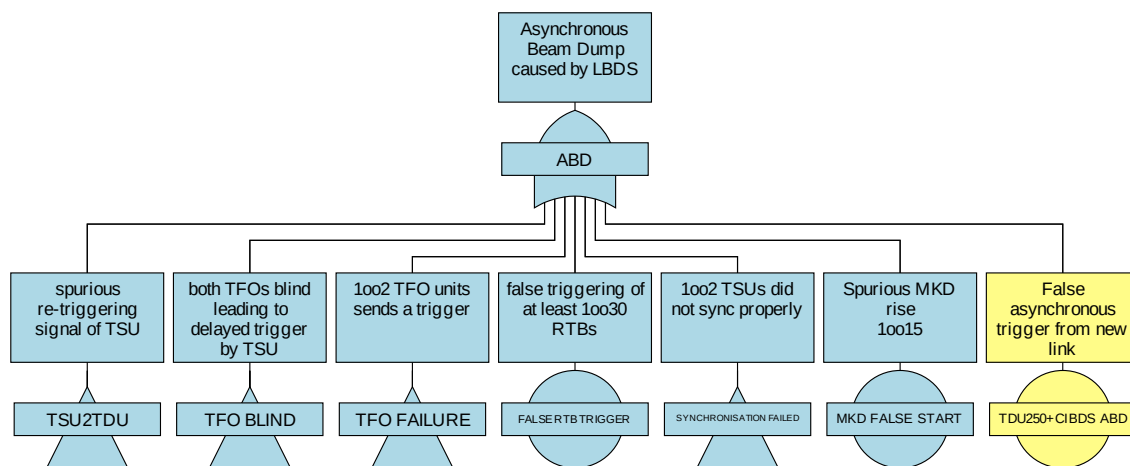


Figure 5.2: Fault Tree Level 1: Asynchronous Beam Dumps caused by the LBDS.

Asynchronous Beam Dumps can occur if

- a TSU sends a spurious trigger to the TDU200 μ s.
- both TFOs are blind. In this case the beam is dumped after 200 μ s via the Re-triggering Lines.
- a TFO sends a spurious trigger to the MKDs.
- a Re-trigger Box sends a spurious trigger.
- the synchronisation fails in the TSUs.
- an MKD rises without a demand.
- the CIBDS or the TDU250 causes an Asynchronous Beam Dump. This fault will be discussed in detail in Chapter 5.2 and 5.3.

Figure 5.3 shows the sub-events for the level 1 fault tree TSU (left) and TFO (right) failures. While it is sufficient if one TSU sends a spurious trigger (OR gate), both TFOs have to be blind at the same time to cause an Asynchronous Beam Dump (AND gate).

The TSUs are directly connected to the TDUs. A spurious trigger in one of the two TSUs without triggering the TFOs will cause an Asynchronous Beam Dump via the TDU and the Re-triggering Lines with a delay of 200 μ s.

If both TFOs are blind at the same time (e.g. due to an undiscovered common failure mode), a beam dump request from the TSUs cannot be forwarded to the PTUs of the kicker magnets. In this failure scenario a beam dump would be initiated by the connected TDUs.

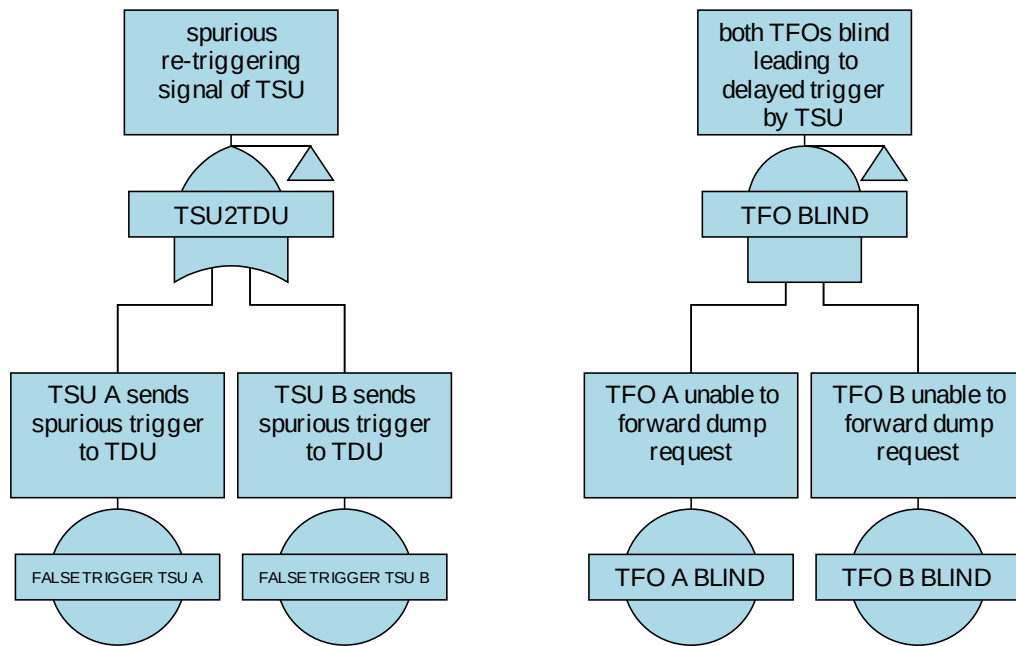


Figure 5.3: Fault Tree Level 2: spurious TSU failure (left) and blind TFO failure (right). Both failures are leading to an Asynchronous Beam Dump.

The third event to cause an Asynchronous Beam Dump is shown in Figure 5.5. Two redundant TFOs are used to distribute the dump request coming from the TSUs to the PTUs of the kicker magnets. If one of the two redundant TFOs sends a false trigger all kicker magnets will rise in less than $4\ \mu\text{s}$ to their nominal energy. This can happen if the subsystems of the TFO, the Trigger Fan-Out Receiver (TFOR) or The Trigger Fan-Out Transceiver (TFOT) are triggering spuriously (see Figure 5.4).

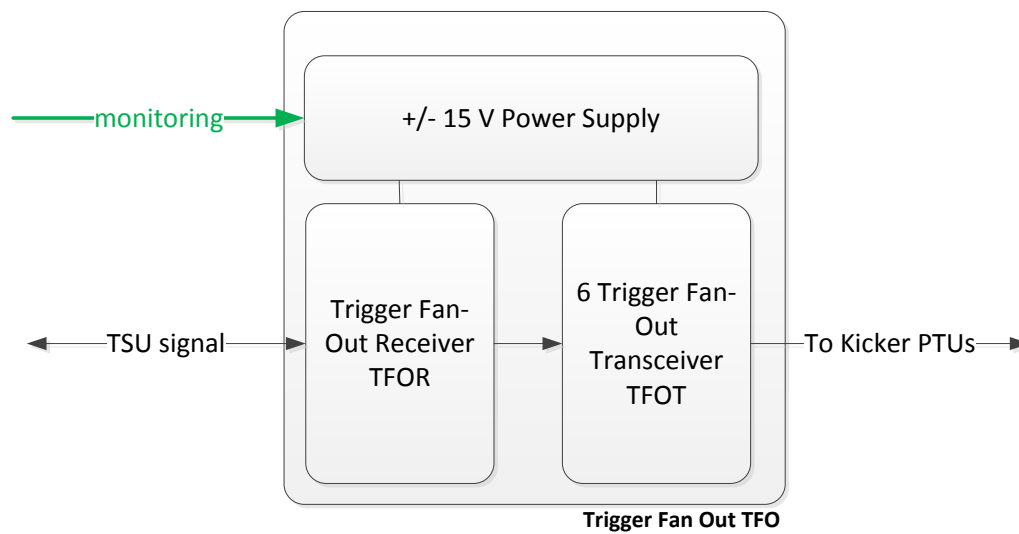


Figure 5.4: Schematic layout of the TFO with its three subsystems.

The TFOR is responsible for acquiring the redundant signals from two TSUs and distributing them to the six TFOTs, which will trigger the PTUs of the kicker magnets [13].

The internal ± 15 V power supply is monitored; a beam dump request will be triggered if the monitored power supply is failing.

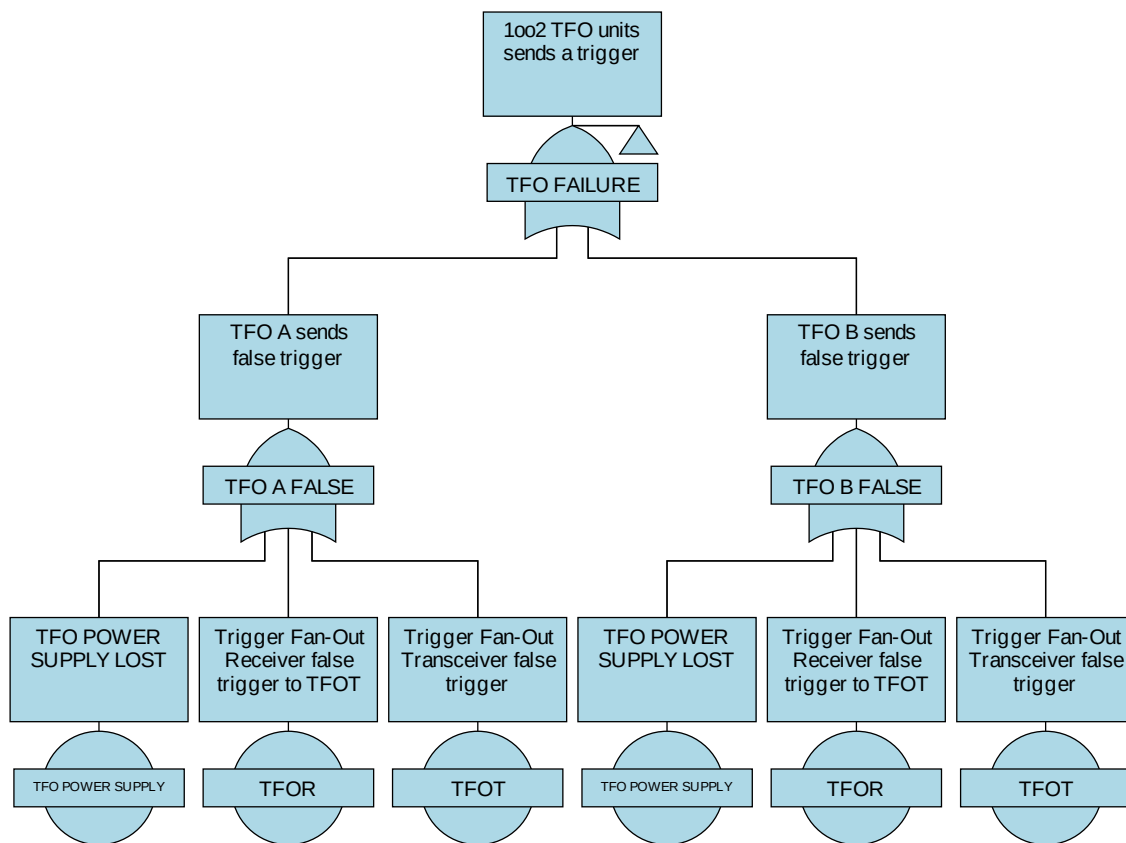


Figure 5.5: Fault Tree: TFO triggering due to a failure in the sub-systems of the TFO.

The TSU consists of four sub-systems (see Figure 5.6):

- The dump requests client interface sub-system (red) detects dump request issued by clients.
- The synchronisation sub-system (orange) synchronizes the kicker magnet triggering with the abort gap in the beam.
- The dump request management sub-system (blue) generates the output pulse.
- The supervisory and diagnostic sub-system (green) cross-checks the correct operation of the TSU with the redundant unit [13].

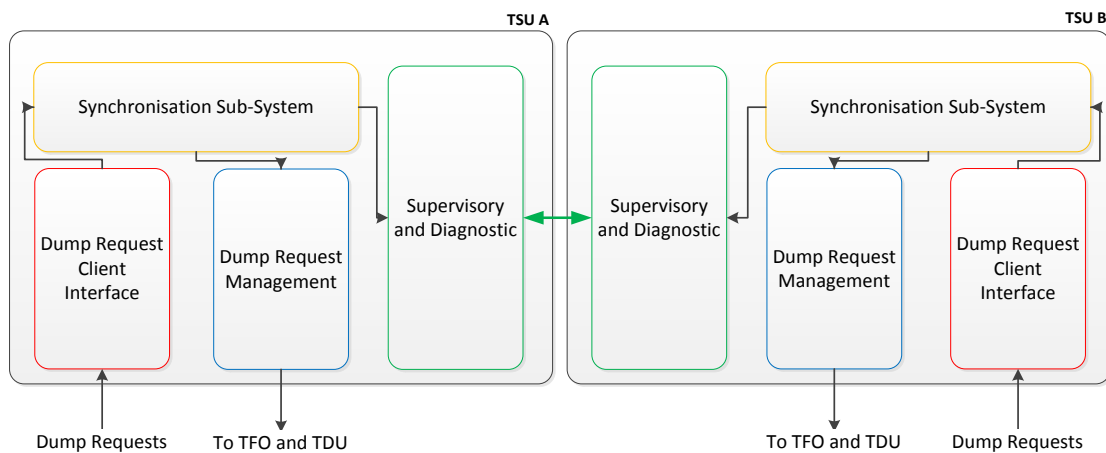


Figure 5.6: Schematic layout and signal paths in and between the two TSUs.

If the supervisory and diagnostic sub-system registers that the synchronisation time of the TSUs differs due to a synchronisation failure in one unit, a beam dump request will be initiated immediately. Figure 5.7 shows the fault tree for this event. If either TSU A or TSU B fails at the synchronisation, the TSUs will trigger an Asynchronous Beam Dump.

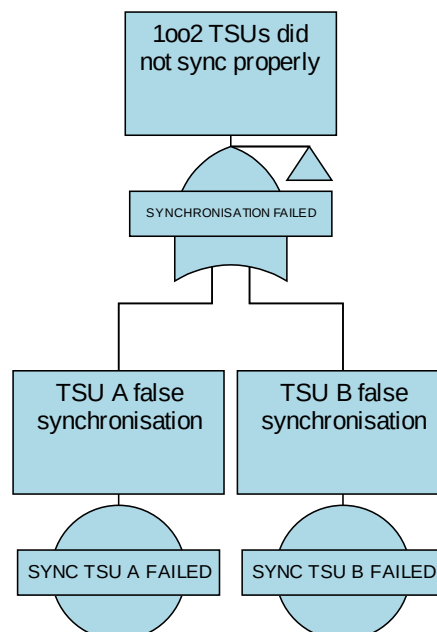


Figure 5.7: Fault Tree of a synchronisation failure in the TSU.

The bottom events in Figure 5.2 include the false triggering of at least one of the thirty Re-triggering Boxes (RTBs). The RTBs are part of the Re-triggering System. A spurious trigger will activate the connected PTU of a kicker magnet and the other kicker magnets will rise within 750 ns (see Chapter 3.4.1 The Re-triggering System).

The remaining bottom event from Figure 5.2 is the spurious rise of at least one of the fifteen MKDs. This will activate the re-triggering box and the other kicker magnets will be activated via the Re-triggering Lines.

5.1.2 Synchronous Beam Dumps

A Synchronous Beam Dump will occur, if one TSU sends a Synchronous Beam Dump request to the TFOs.

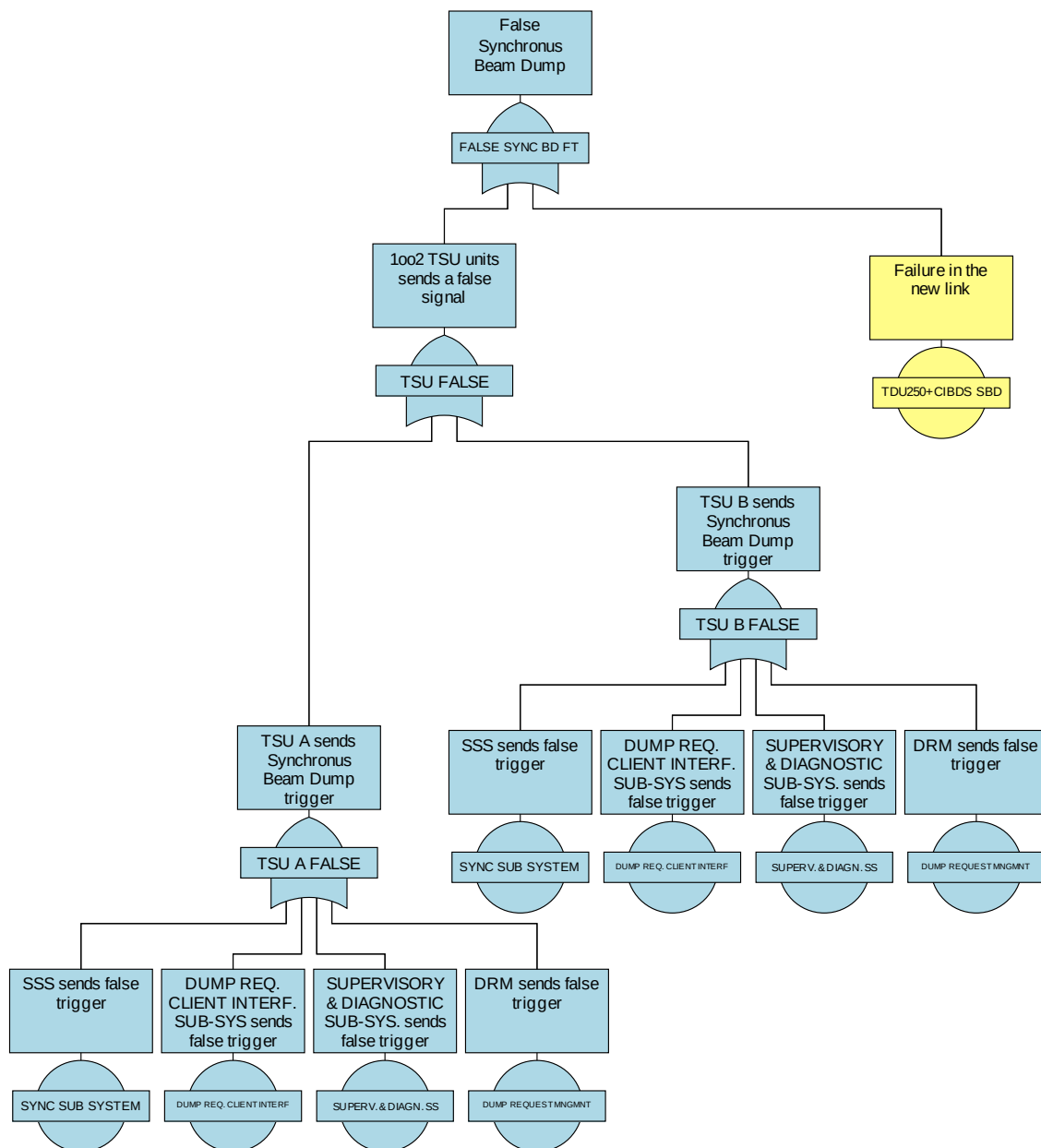


Figure 5.8: Fault Tree of Synchronous Beam Dumps caused by the TSUs in the LBDS.

Figure 5.8 shows a Fault Tree for Synchronous Beam Dumps caused by the TSUs. As long as the Synchronisation Sub-System is working properly, false triggers from the TSUs sub-systems will always cause Synchronous Beam Dumps. The bottom events for each TSU show false triggers from the synchronisation sub-system, the dump requests client interface sub-system, the supervisory and diagnostic sub-system and the dump request management. The failures caused by the new link from the BIS to the LBDS (yellow in Figure 5.8) leading to Synchronous (and also Asynchronous) Beam Dumps will be discussed in detail in Chapter 5.2.

Detectable failures within the LBDS can also cause Synchronous Beam Dumps by opening the BIS loop. These failures are not discussed here since it would exceed the scope of this thesis.

5.1.3 Unable to Dump the Beam

The unavailability of the LBDS on demand is currently the worst case failure scenario for the LHC. In this case the beam could not be extracted anymore and parts of the LHC could be destroyed beyond repair. This scenario has to be avoided under all circumstances.

Figure 5.9 shows the Fault Tree for this failure, which appears if both TSUs fail at the same time. As mentioned in Chapter 3.5, a common failure mode with this consequence was identified in the 12 V power distribution inside the TSU crate. To prevent this failure scenario, the new link from the BIS to the LBDS adds a parallel path from the Beam Interlock System to trigger the kicker magnets for the extraction of the beam.

Only if both TSUs and the new link would be unavailable at the same time this catastrophic failure mode could occur.

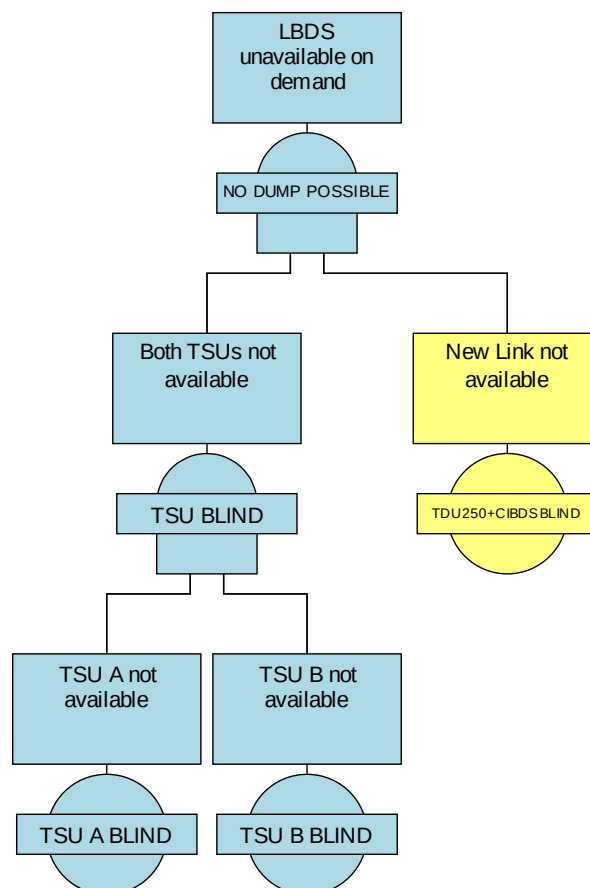


Figure 5.9: Fault Tree: Worst case scenario: LBDS unavailable on demand.

5.2 The Trigger Delay Unit

The 250 μ s Trigger Delay Unit (TDU250) will be used to initiate an Asynchronous Beam Dump directly from the BIS by triggering the Re-triggering Lines (see Chapter 3.4.1).

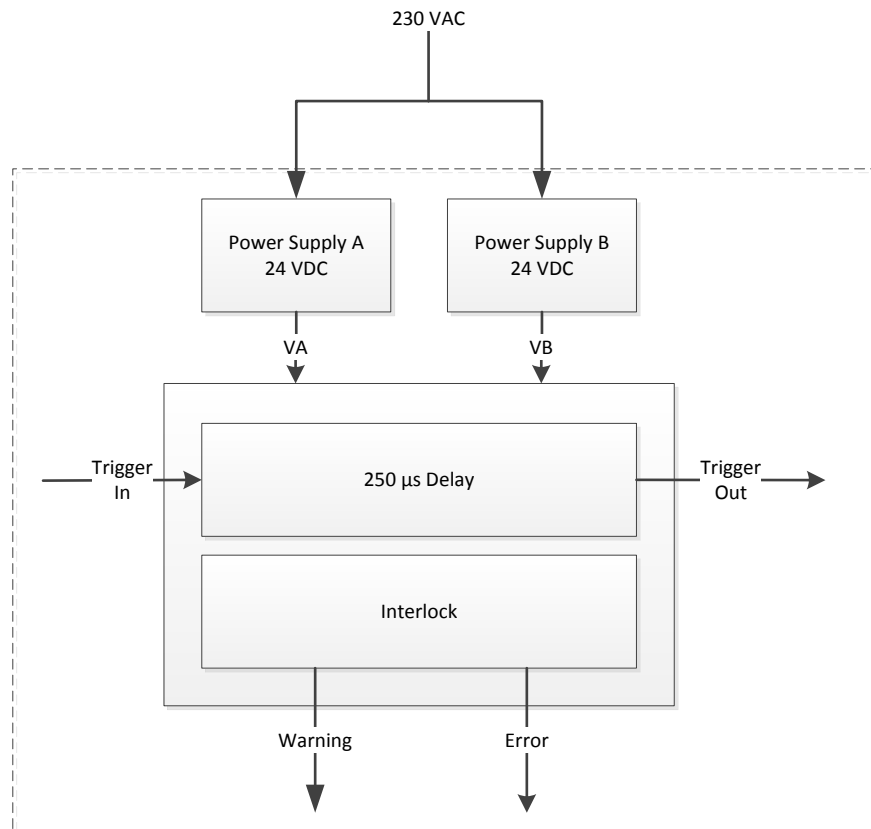


Figure 5.10: Functional Block Diagram 250 μ s Trigger Delay Unit.

Figure 5.10 shows a functional block diagram of the TDU. The unit itself is subdivided into two circuits. The delay circuit is responsible to delay an incoming beam dump request (Trigger In) for 250 μ s and then generate a pulse for the Re-triggering Lines (Trigger Out). The local interlock circuit monitors input and output connections, the power supplies as well as the thyristor voltage in the delay circuit (see Figure 5.13, blue box).

The TDU is powered by two internal 24 VDC power supplies, to assure redundant powering. If one fails the second guarantees the full functionality of the TDU and a warning signal will be generated. The local interlock circuit is monitored by a PLC. In case of a failure it will either open the BIS loop, causing a Synchronous Beam Dump, or block the re-arming of the LBDS after a beam dump, until the problem has been mitigated.

In the case that both 24 VDC power supplies or the mains fail, the supply voltage is maintained by internal capacitors. These allow the TDU to remain operational for up to 30 minutes [24].

In the following the behaviour of the delay and the interlock circuit in case of a failure will be discussed.

The main purpose of this reliability analysis of the TDU250 is to investigate how many additional Synchronous and Asynchronous Beam Dumps it will cause during the LHC operation.

5.2.1 Trigger Delay Circuit

The trigger delay circuit consists only of analogue components. Figure 5.13 shows the layout of the trigger delay circuit (TDC). Note the not mounted components above the inductor L1 (R12, T3, C6, R10, R13, D12 and C9, see dashed box in Figure 5.13). These components were originally planned to decrease the charge time of the capacitors. Their functionality is not used for the TDU250 and therefore these components are not included in the reliability analysis.

The not mounted capacitors C1, C5, C3 and C2 below the inductor L1 (see grey box in Figure 5.13) are placeholders for capacitors to determine the delay time. In the TDU250 at least one capacitor will be connected to the inductor L1, further called CL², at the position of one of these placeholders. The capacitor CL and the inductor L1 form a harmonic oscillator.

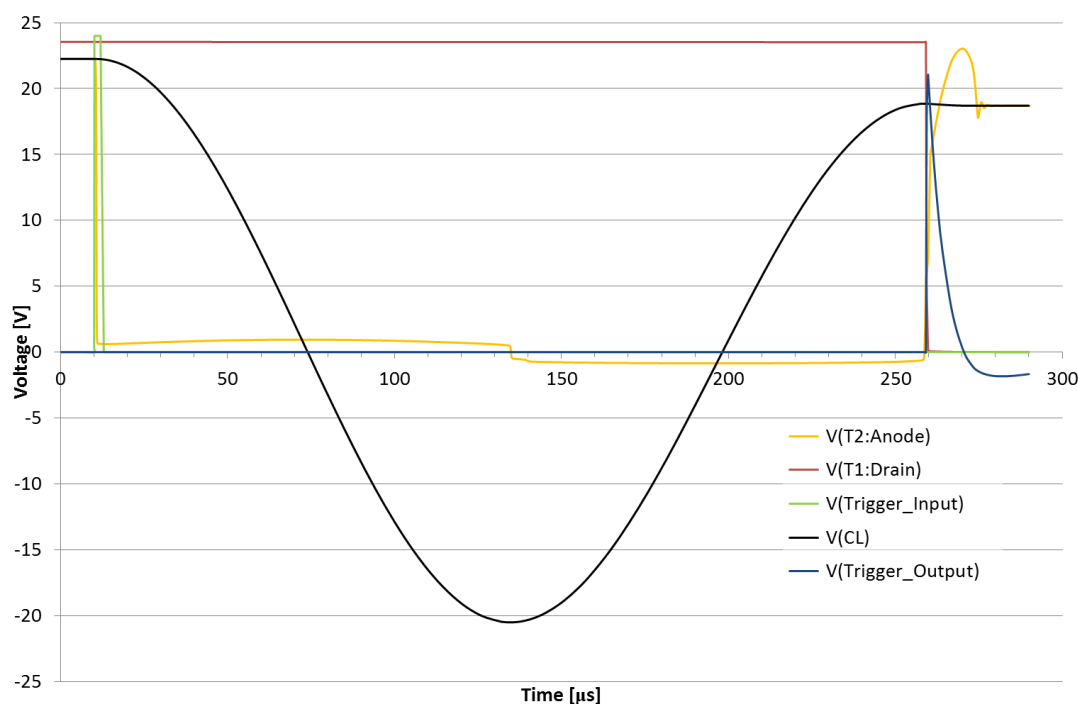


Figure 5.11: Voltage over time against ground in the trigger delay circuit during a trigger cycle.

² The influence of two capacitors is also studied in the reliability analysis; see Influence of two Capacitors in the Harmonic Oscillator on the Reliability, page 67.

Figure 5.11 shows the voltage against ground over time in the trigger delay circuit at different elements after a trigger input. The colours adopted in the graph are also used in Figure 5.13 to highlight the components.

A trigger input pulse from the TSU (green at $10\ \mu\text{s}$) activates the thyristor T2 (orange) and starts the oscillation in the circuit. The black line shows the voltage over the capacitor CL. Note, that the current oscillation is phase-delayed to the voltage oscillation, having its zero crossing at $135\ \mu\text{s}$ (minimum of CL voltage).

For the first half of the $250\ \mu\text{s}$ oscillation the current flows through the thyristor T2. After the zero crossing at $135\ \mu\text{s}$ the current changes direction and flows through the diode D1 while T2 is turned off. At the end of the oscillation T2 blocks the voltage and the rising edge at the thyristor anode V(T2:Anode) activates the MOSFET T1 (red). The now conducting MOSFET causes the drain voltage of T1 to drop to zero. This generates the trigger output (blue) via the trigger transformer TR1 [24].

OrCAD Capture was used to draw the schematics for trigger delay circuit and interlock circuit. The circuits and failure modes of each component were simulated in PSPICE. Figure 5.12 shows a simple example for the simulation of an open resistor R29 ($220\ \text{k}\Omega$) in the interlock circuit by using a time dependant opening switch U5. The switch is closed at the beginning of the simulation and opens after $5\ \mu\text{s}$ (TOPEN = $5\ \mu\text{s}$). This happens before the trigger input (Trigger_Input), which is delayed for $10\ \mu\text{s}$ (TD = $10\ \mu\text{s}$). Other parameters describe the nominal voltage (V1), the trigger voltage (V2), time to rise and fall for the trigger (TR, TF), the trigger width (PW) and the period between triggers (PER, 0 implies a single trigger).

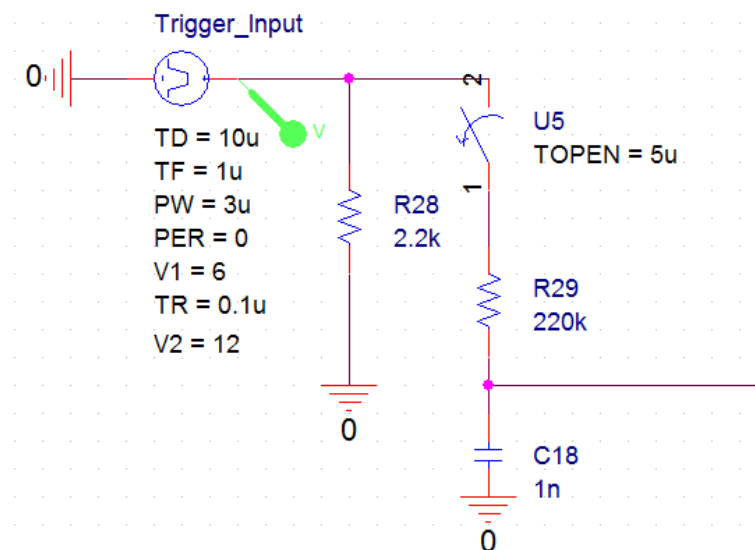


Figure 5.12: OrCAD Capture Circuit, simulation of an open resistor.

Time dependant switches allow determining the point in time when a failure occurs (before a trigger input, at the trigger input, during the oscillation) and analysing its effect on the circuit. This is done by simulating the circuit over time and checking the voltages at important

components in the post analysis of PSPICE. The effects of failed components were assigned to the respective failure modes.

In the following, component failures leading to Asynchronous Beam Dumps, Synchronous Beam Dumps and the unavailability of the TDU250 are discussed.

A list of components and their failure rates in the Trigger Delay Unit can be found in the Appendix 8.2.

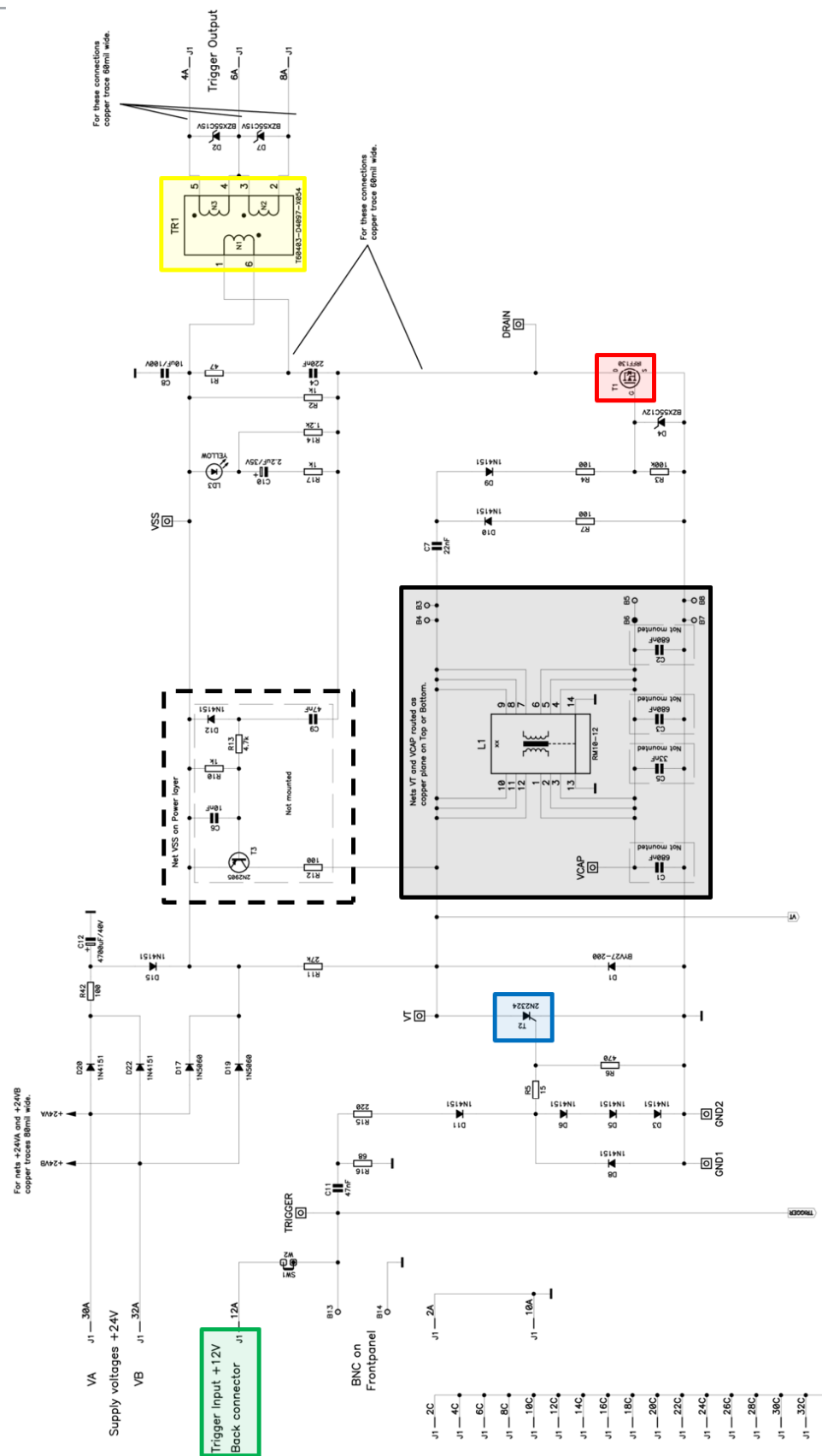


Figure 5.13: Layout of the trigger delay circuit [25].

Asynchronous Beam Dumps

There are two possibilities to cause a false Asynchronous Beam Dump from the trigger delay circuit:

The first possibility occurs if the drain voltage of the MOSFET T1 decays below 16.5 V due to a component failure. This will cause an immediate pulse to the trigger output of at least 7.5 V which is sufficient to activate the PTUs of the kicker magnets.

The MOSFET T1 used in the TDU is of the Quality Level Class JANTXV referring to MIL-PRF-19500 test methods [26]. The total calculated failure rate is 86.88 FIT. The failure mode ‘short’ is split up equally into three possibilities for shorts between source, drain and gate. Two of them will cause Asynchronous Beam Dumps:

Figure 5.14 shows the result of a simulation of the trigger delay circuit in case of a short circuit between gate and drain in T1. The failure occurs at $t = 20 \mu\text{s}$ and the T1 drain voltage (red) drops to 4 V. As a result, the trigger transformer TR1 immediately produces a trigger output (blue). Although the trigger voltage is lower than usual, this would cause an Asynchronous Beam Dump.

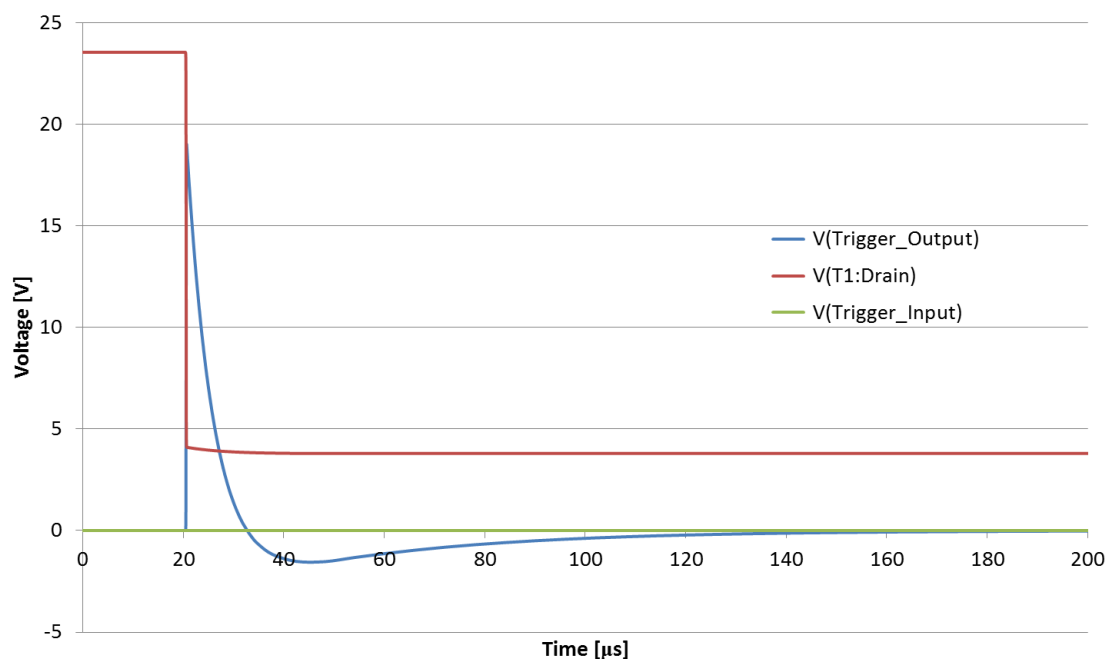


Figure 5.14: Voltage over time against ground, failure mode short from gate to drain in T1 at $t = 20 \mu\text{s}$.

A short between drain and source has the same effect with the only difference that the drain voltage will drop to 0 V. Therefore the amplitude of the trigger output will be higher (see Figure 5.15).

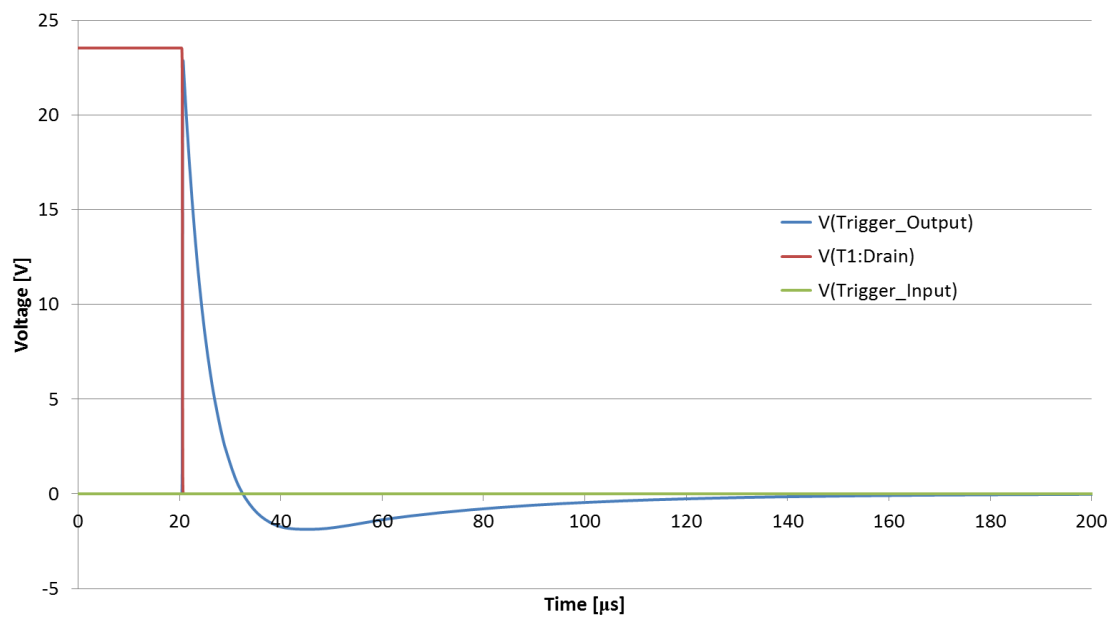


Figure 5.15: Voltage over time against ground, failure mode short from drain to source in T1 at $t = 20 \mu\text{s}$.

Table 5.1 summarizes the failure modes and failure rates of T1, which lead to an Asynchronous Beam Dump.

Table 5.1: T1 MOSFET failures contributing to false Asynchronous Beam Dumps.

T1 MOSFET		
Failure Mode Description	$\lambda_{\text{MIL-HDBK}}$ [FIT]	$\lambda_{\text{Manufacturer}}$ [FIT]
Short Gate to Drain	14.77	n.a.
Short Drain to Source	14.77	n.a.

The second possibility for an Asynchronous Beam Dump occurs if the delay time is too short for the synchronous path of the LBDS to take effect. Determining the delay time, the LC harmonic oscillator is critical in the delay circuit.

The failure rate for the inductor was calculated to 2.16 FIT, the capacitor failure rate was calculated to 12.71 FIT. While there is no manufacturer data available for the inductor, manufacturer WIMA provides failure rates for FKS2 capacitors of 5 FIT. Both components can exhibit the failure modes ‘open’, ‘short’ and ‘parameter change’ [20].

If the path of the LC oscillator is open, this means that either L1 or CL fails ‘open’, an incoming trigger will be forwarded after $\sim 30 \mu\text{s}$ (see Figure 5.16) causing an Asynchronous Beam Dump as the synchronous path of the LBDS cannot act within this time regime. The peak of the trigger output is 11.5 V, which is enough to activate the PTUs of the kicker magnets via the Re-triggering Lines.

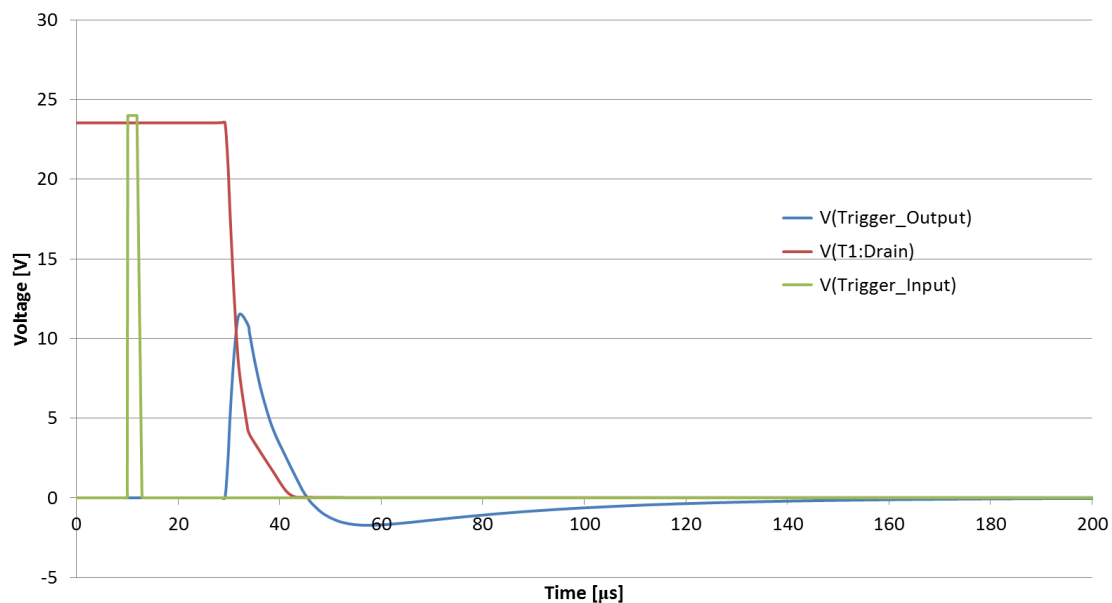


Figure 5.16: Voltage over time against ground in the trigger delay circuit, open CL path failure after trigger input.

A parameter variation of inductance or capacity will result in different delay times. Changes limited to $\pm 10\%$ in the components' characteristics are compatible to the required accuracy of the delay time of $250 \pm 10 \mu\text{s}$. The trigger output signal will be automatically checked after each beam dump. Taking into account that sudden major changes in the components' characteristics are unlikely, most of these failures will be detected and can be mitigated before they will cause an unwanted Asynchronous Beam Dump. However, as a conservative approach, it is assumed that only half of the parameter changes are detectable failures. The other half will be accounted to the Asynchronous Beam Dump failure mode.

Table 5.2 provides the quantitative data for the oscillator failure modes.

Table 5.2: LC failures contributing to false Asynchronous Beam Dumps.

L1 CL harmonic oscillator		
Failure Mode Description	$\lambda_{\text{MIL-HDBK}}$ [FIT]	$\lambda_{\text{Manufacturer}}$ [FIT]
Open L1	0.91	n.a.
Open CL	5.08	2
Parameter Change L1	0.17	n.a.
Parameter Change CL	1.14	0.45

A short in capacitor C7 will cause the drain voltage of the MOSFET to drop to 0 V without an incoming trigger and therefore result in an immediate trigger to the Re-triggering Lines and activate the kicker magnets (see Figure 5.17).

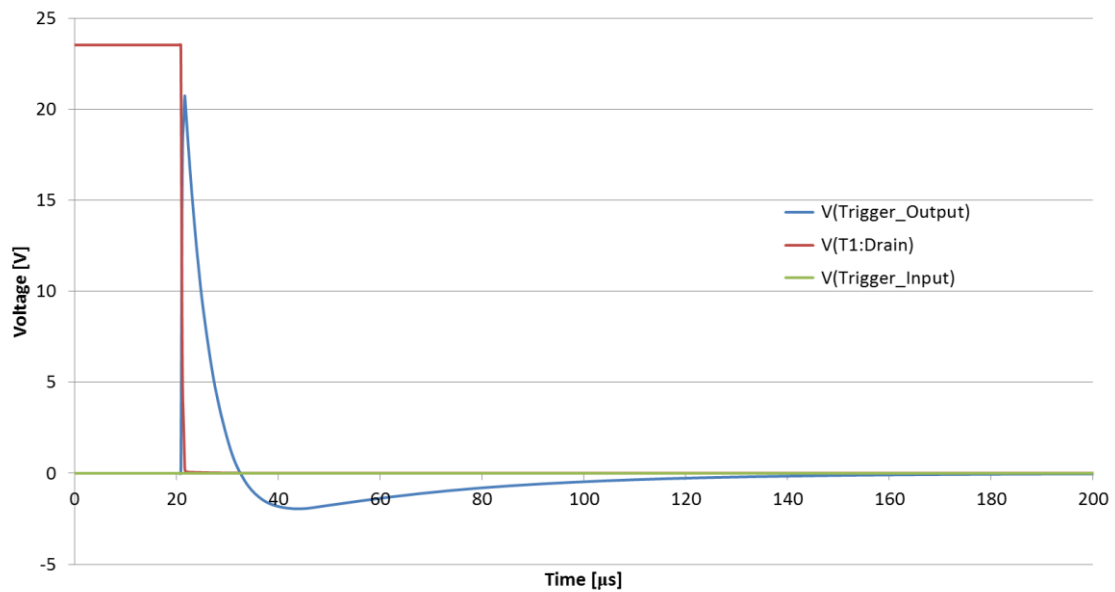


Figure 5.17: Voltage over time against ground in the trigger delay circuit, open capacitor C7 at 20 μ s.

The failure rates for this failure mode are listed in Table 5.3:

Table 5.3: Failure of capacitor C7 contributing to false Asynchronous Beam Dumps.

C7 Polyester Capacitor		
Failure Mode Description	$\lambda_{\text{MIL-HDBK}}$ [FIT]	$\lambda_{\text{Manufacturer}}$ [FIT]
Open C7	3.70	0.8

In the second half of the LC oscillation the current flows through diode D1 (see Figure 5.13, left of L1). An ‘open diode’ D1 shortens the delay to about 150 μ s. Since this time may not be enough for the synchronous LBDS path to take effect the failure mode ‘open diode’ is assigned to the failure effect Asynchronous Beam Dump. The simulation of the delay circuit with an open diode D1 is shown in Figure 5.18.

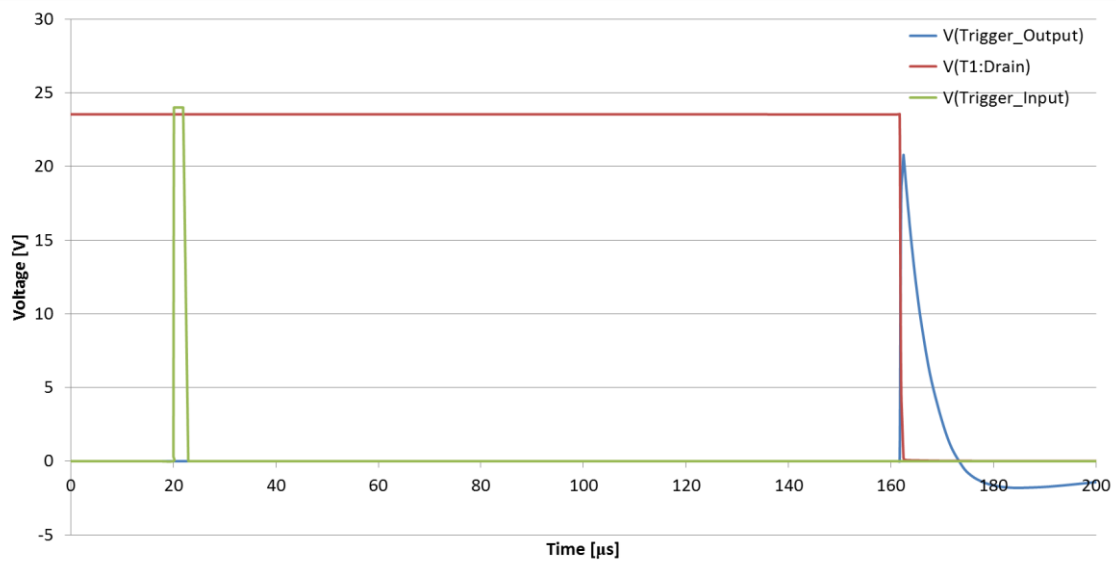


Figure 5.18: Voltage over time against ground in the trigger delay circuit due to open diode D1.

Table 5.4 lists the failure rate to this failure mode.

Table 5.4: Diode D1 failure contributing to Asynchronous Beam Dumps.

D1		
Failure Mode Description	$\lambda_{\text{MIL-HDBK}}$ [FIT]	$\lambda_{\text{Manufacturer}}$ [FIT]
Open D1	4.27	n.a.

The trigger transformer TR1 is forwarding the Asynchronous Beam Dump request to the Re-triggering Lines. The total calculated failure rate for this transformer is with 120.9 FIT dominating the delay circuit. The probability for the failure mode ‘short’ for a transformer is 42 % according to MIL-HDBK-338B [20], therefore the failure rate for shorts in trigger transformer TR1 is 50.78 FIT. Shorts will only cause an Asynchronous Beam Dump if they occur between primary and secondary coils but not within one coil. The transformer is compliant with international standards for reinforced isolation [27], therefore the likelihood of a short between primary and secondary coils is expected to be considerably lower than shortcuts in between the single coils. With a conservative approach, 33 % of all short circuits are expected to appear between primary and secondary coils, compare Table 5.5.

Table 5.5: TR1 failure contributing to false Asynchronous Beam Dumps.

TR1		
Failure Mode Description	$\lambda_{\text{MIL-HDBK}}$ [FIT]	$\lambda_{\text{Manufacturer}}$ [FIT]
Short TR1 (primary to secondary coil)	16.93	n.a.

The total failure rate for an Asynchronous Beam Dump is the sum of the component failure rates presented above. With the calculated data from the military handbook the failure rate is:

$$\lambda_{ABD_TDC_MIL} = \sum \lambda_{i_MIL-HDBK} = \mathbf{61.74 \text{ FIT}}. \quad (5.1)$$

Therefore the MTTF for an Asynchronous Beam Dump due to a failure in the TDU is:

$$MTTF_{ABD_TDC_MIL} = \frac{1}{61.74 \text{ FIT}} \approx \mathbf{1849 \text{ years}}. \quad (5.2)$$

Considering the data from manufacturers, if available, instead of the calculation of the failure rates based on the Military Handbook 217F, the failure rate and the *MTTF* change as follows:

$$\lambda_{ABD_TDC_MAN} = \sum \lambda_{i_Manufacturer} = \mathbf{55.07 \text{ FIT}}. \quad (5.3)$$

$$MTTF_{ABD_TDC_MAN} = \frac{1}{55.07 \text{ FIT}} \approx \mathbf{2073 \text{ years}}. \quad (5.4)$$

Since the interlock circuit does not contribute to the failure mode Asynchronous Beam Dump, the amount of expected Asynchronous Beam Dumps from one TDU250 within 10 years of operation is between 4.8×10^{-3} (Manufacturer) and 5.4×10^{-3} (MIL-HDBK).

Synchronous Beam Dumps

Failures in the trigger delay circuit can also cause Synchronous Beam Dumps. Synchronous Beam Dumps will be triggered by the interlock circuit if the monitored voltage at the thyristor anode falls to 0 V for over 18 ms³. The interlock circuit will generate an error signal and the connected PLC will trigger a beam dump request via the BIS.

Figure 5.19 shows the voltage over time in case of a failure in resistor R11. If this resistor fails to open, the thyristor anode voltage (blue) decays after a few seconds to 0 V. At the same

³ A Schmitt trigger is used in the interlock circuit to monitor the thyristor anode voltage, see Chapter 5.2.2 Local Interlock Circuit - Synchronous Beam Dumps and Figure 5.22. The delay time for the Schmitt trigger to switch is depending on the thyristor anode voltage in case of a failure. The delay time is between 18 ms for 0 V and 82 ms for 4.6 V. Voltages above 4.6 V will not trigger the Schmitt trigger switch.

time, the MOSFET drain voltage (red) stays high. Thus, no Asynchronous Beam Dump will be triggered. This low voltage will be detected by the interlock circuit, which will trigger a Synchronous Beam Dump.

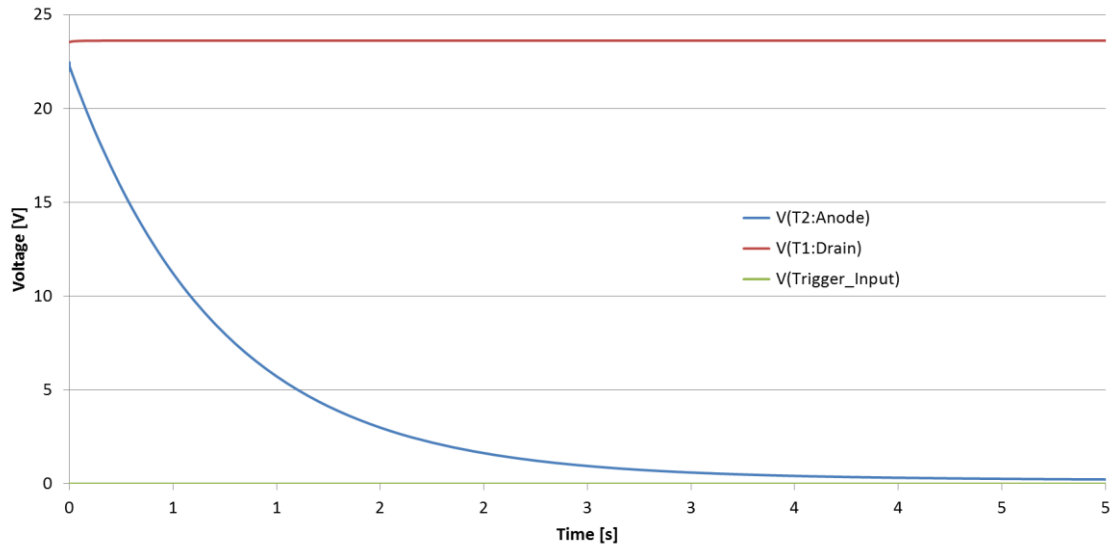


Figure 5.19: Voltage over time against ground in the trigger delay circuit due to open resistor R11. No Trigger Input (green) was used, when the failure was simulated.

Table 5.6 summarizes all component failures and their corresponding failure rates in the trigger delay circuit, which will cause the voltage $V(T2:Anode)$ to decay and stay low. In addition to R11 the capacitors CL and C8 and the diode D1 contribute to the failure mode Synchronous Beam Dump. From the calculated failure rate of 41.97 FIT for the thyristor T2 73 % will result in short circuits but only two of three possible shorts will cause a Synchronous Beam Dump. Therefore 20.42 FIT is contributed by the thyristor T2. These short failures account for almost half of the overall summed Synchronous Beam Dump failure rate in the trigger delay circuit.

Figure 5.20 shows the voltage over time in the trigger delay circuit in case of a short from anode to gate in thyristor T2 at $t = 10 \mu s$. The thyristor anode voltage (blue) falls and begins to oscillate between -0.9 V and +1.2 V. The drain voltage at the MOSFET T1 (red) stays high, thus no trigger output signal is generated (dashed yellow). This failure will be detected by the interlock circuit.

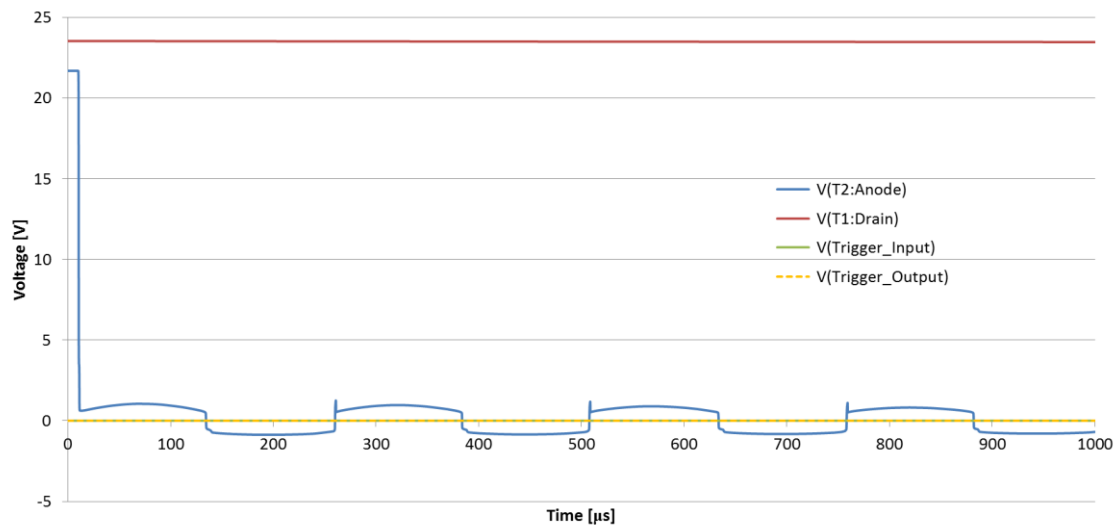


Figure 5.20: Voltage over time against ground in the trigger delay circuit due to a short (anode to gate) in thyristor T2 at $t = 10$ ms.

Table 5.6: Components contributing to Synchronous Beam Dumps in the trigger delay circuit.

R11, C8, CL, D1, T2		
Failure Mode Description	$\lambda_{\text{MIL-HDBK}}$ [FIT]	$\lambda_{\text{Manufacturer}}$ [FIT]
Open R11	4.42	n.a.
Short C8	8.38	0.80
Short CL	5.39	2.10
Short D1	5.81	n.a.
Short T2 (anode to cathode)	10.21	n.a.
Short T2 (anode to gate)	10.21	n.a.

The following equations show the summed failure rates and the resulting $MTTF$, assuming calculated failure rates:

$$\lambda_{SBD_TDC_MIL} = \mathbf{44.42 \text{ FIT.}} \quad (5.5)$$

$$MTTF_{SBD_TDC_MIL} = \frac{1}{44.42 \text{ FIT}} \approx \mathbf{2570 \text{ years.}} \quad (5.6)$$

When the reliability data of the manufacturers is considered the following values are achieved:

$$\lambda_{SBD_TDC_MAN} = \mathbf{33.55 \text{ FIT}}. \quad (5.7)$$

$$MTTF_{SBD_TDC_MAN} = \frac{1}{33.55 \text{ FIT}} \approx \mathbf{3403 \text{ years}}. \quad (5.8)$$

TDU not available on demand

Component failures in the trigger delay circuit can prevent an incoming trigger to be forwarded to the Re-triggering Lines. Thus, the TDU is not available on demand.

The components connected directly to the trigger input, including the high-pass filter (C11 and R16), resistor R15 and diode D11, will mask the trigger in case of a failure by connecting an incoming trigger to ground (short in R16) or interrupting the trigger path (open C11, R15, D11). The contributing failure modes are listed in Table 5.7.

Table 5.7: Components at trigger input, failures contributing to unavailability on demand.

C11, R16, R15, D11		
Failure Mode Description	$\lambda_{\text{MIL-HDBK}}$ [FIT]	$\lambda_{\text{Manufacturer}}$ [FIT]
Open C11	5.38	0.84
Open R15	7.30	n.a.
Open D11	3.85	n.a.
Short R16	0.62	n.a.

The harmonic oscillator (L1 and CL), can also contribute to this failure mode. Shorts in the oscillator inductor L1 prohibit forwarding an incoming trigger.

Table 5.8: LC Oscillator component failures contributing to unavailability on demand.

LC oscillator		
Failure Mode Description	$\lambda_{\text{MIL-HDBK}}$ [FIT]	$\lambda_{\text{Manufacturer}}$ [FIT]
Short L1	0.91	n.a.

More failures, which will prohibit forwarding an incoming trigger, are listed in Table 5.9. Noteworthy is especially the trigger transformer TR1. As it is directly connected to the Re-triggering Lines, an open trigger transformer will cause the TDU250 not to be able to forward signals. With its high failure rate (120.9 FIT) it is the top contributor to the failure mode unavailability on demand if it fails open (42 %, 50.78 FIT).

The second contributor is thyristor T2 which accounts in total 21.54 FIT for two failure modes: An open thyristor T2 (11.33 FIT) as well as a short circuit from the gate to the cathode in T2 (10.21 FIT) will cause the TDU250 to be unavailable on demand.

Table 5.9: Other components contributing to unavailability on demand.

D4, T2, R3, R11, R6, D8, D11, R2, R1, T1, R4, D9, D10, R7, C7, TR1.		
Failure Mode Description	$\lambda_{\text{MIL-HDBK}}$ [FIT]	$\lambda_{\text{Manufacturer}}$ [FIT]
Short D4	3.43	n.a.
Short T2 (gate to cathode)	10.21	n.a.
Short R3	0.12	n.a.
Short R11	0.37	n.a.
Short R6	0.25	n.a.
Short D8	2.34	n.a.
Short D11	2.89	n.a.
Short R2	0.75	n.a.
Short R1	0.62	n.a.
Open T1	4.34	n.a.
Open R4	7.30	n.a.
Open D9	2.26	n.a.
Open D10	3.80	n.a.
Open R7	7.30	n.a.
Open C7	3.89	0.84
Open T2	11.33	n.a.
Open TR1	50.78	n.a.

The summed failure rate of all component failures leading to unavailability on demand of the TDU250 is:

$$\lambda_{TDU_N/A_MIL} = \mathbf{130.04\ FIT} \quad (5.9)$$

$$\lambda_{TDU_N/A_MAN} = \mathbf{122.45\ FIT} \quad (5.10)$$

These failure rates result in the following *MTTFs*:

$$MTTF_{TDU_N/A_MIL} = \frac{1}{130.04\ FIT} \approx \mathbf{878\ years.} \quad (5.11)$$

$$MTTF_{TDU_N/A_MAN} = \frac{1}{122.45 \text{ FIT}} \approx 932 \text{ years.} \quad (5.12)$$

The failure mode ‘unavailability on demand’ only occurs in the trigger delay circuit, therefore the failure rates listed above represent the total failure rate for unavailability on demand for the TDU250.

5.2.2 Local Interlock Circuit

The Trigger Delay Unit interlock circuit is used to monitor both 24 V supply voltages, the input and output connection and the voltage over the thyristor anode in the delay circuit. Figure 5.21 shows the circuit layout of the interlock circuit. The interlock circuit generates a warning signal if at least one supply voltage is too low or an error signal in all other cases (dashed black box, Figure 5.21).

The key-component of this circuit is a Quad 2-Input NAND Schmitt Trigger (IC1, blue, see Figure 5.21). All outputs of IC1 are inverted. The trigger line (yellow) is connected to input 1 of IC1. The trigger line is high active (6V), thus if the trigger line is not connected to the TDU input 1 turns FALSE. This causes an error. The second input monitors the thyristor anode voltage (VT, green). R20, R21 and C13 define the necessary time for VT to stay low in order to turn input 2 to FALSE and an generate an error signal (see Figure 5.22, output 3 (green) turns high 28 ms after the thyristor voltage (blue) drops to 0 V).

The output signal is inverted twice (output 3 and output 4). The logic in the interlock circuit up to output 4 is shown in Table 5.10.

Table 5.10: Truth table for inputs 1 and 2 and output 3 and 4 of IC1.

Input 1 Trigger line monitoring	Input 2 Thyristor voltage monitoring	Output 3 Input 5 Input 6	Output 4
TRUE	TRUE	FALSE	TRUE
TRUE	FALSE	TRUE	FALSE
FALSE	TRUE	TRUE	FALSE
FALSE	FALSE	TRUE	FALSE

Input 8 of IC1 is used to monitor the TDU output connection to the Re-triggering lines (violet). An error signal is generated when output 10 turns TRUE. The dependencies for output 10 are shown in Table 5.11

Table 5.11: Truth table, dependencies for output 10 of IC1.

Input 1 Trigger line monitoring	Input 2 Thyristor voltage monitoring	Input 8 Output connection monitoring	Output 10 Error signal creation
TRUE	TRUE	TRUE	FALSE
TRUE	TRUE	FALSE	TRUE
TRUE	FALSE	TRUE	TRUE
FALSE	TRUE	TRUE	TRUE
FALSE	FALSE	TRUE	TRUE
FALSE	TRUE	FALSE	TRUE
TRUE	FALSE	FALSE	TRUE

Input 12 and 13 are used to monitor the redundant supply voltage (red) of the TDU. A warning signal is generated if at least one of those power supplies fails and output 11 turns TRUE. The warning and error signals are created via transistors and relays located right of output 11 and output 18 (see Figure 5.21). Both signals are generated by identical components.

The interlock circuit is not connected to the Re-triggering Lines. Therefore, failures in the interlock circuit cannot cause Asynchronous Beam Dumps. However, spurious error signals might cause Synchronous Beam Dumps. Furthermore false warning signals, without faulty power supplies in the delay circuit, describe another failure mode. In this case the LHC operation will be interrupted after the next beam dump to replace the TDU250. The failure modes are discussed in detail below.

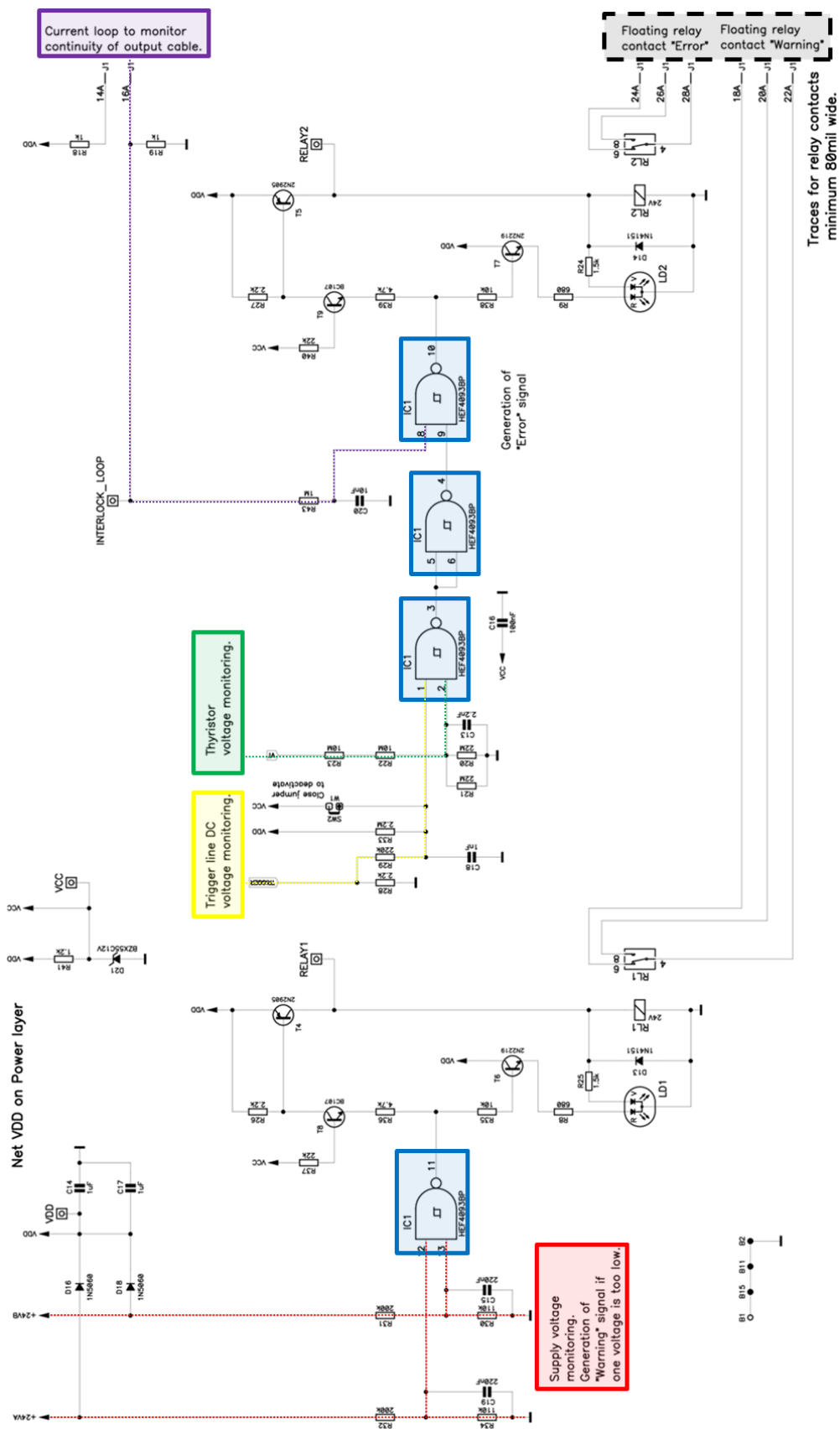


Figure 5.21: Schematics of the interlock circuit [25].

Synchronous Beam Dumps

The Quad 2-Input NAND Schmitt Trigger IC1 is a critical part of the interlock circuit. Six inputs are used to generate error signals and therefore demand Synchronous Beam Dumps.

The first input of IC1 is used to monitor the input connection to the TDU from the CIBDS (trigger line, yellow in Figure 5.21). It is also connected to the VDD 24 V source over a 2.2 M Ω resistor R33. Note that the switch W1 is open. R28 and R29 are used as a voltage divider to generate an offset voltage. Failures in the components before input 1 can connect the trigger line to ground or open the trigger line path and therefore cause a Synchronous Beam Dump (input 1 turns FALSE). The failure rates are listed in Table 5.12.

Table 5.12: Component failures causing Synchronous Beam Dumps for input 1 of IC1.

R28, R29, C18, R33		
Failure Mode Description	$\lambda_{\text{MIL-HDBK}}$ [FIT]	$\lambda_{\text{Manufacturer}}$ [FIT]
Short R28	0.34	n.a.
Short R29	0.12	n.a.
Short R33	0.05	n.a.
Open R29	1.42	n.a.
Open R33	0.65	n.a.
Short C18	3.97	2

The thyristor anode voltage of the delay circuit is monitored using input 2 of IC1 (thyristor voltage monitoring, green in Figure 5.21). Figure 5.22 explains the behaviour of IC1 in case of a low thyristor voltage. The thyristor voltage $V(\text{T2:Anode})$ (blue in Figure 5.22) falls from 24 V to 0 V at $t = 10$ ms. The components R20, R21 and C13 define the decay time of the voltage at input 2 from 5.23 V, which is defined by R22 and R23. The voltage at output 3 (green) turns high (5 V) after about 18 ms when the input voltage falls under the Schmitt trigger threshold, which will produce an error signal.

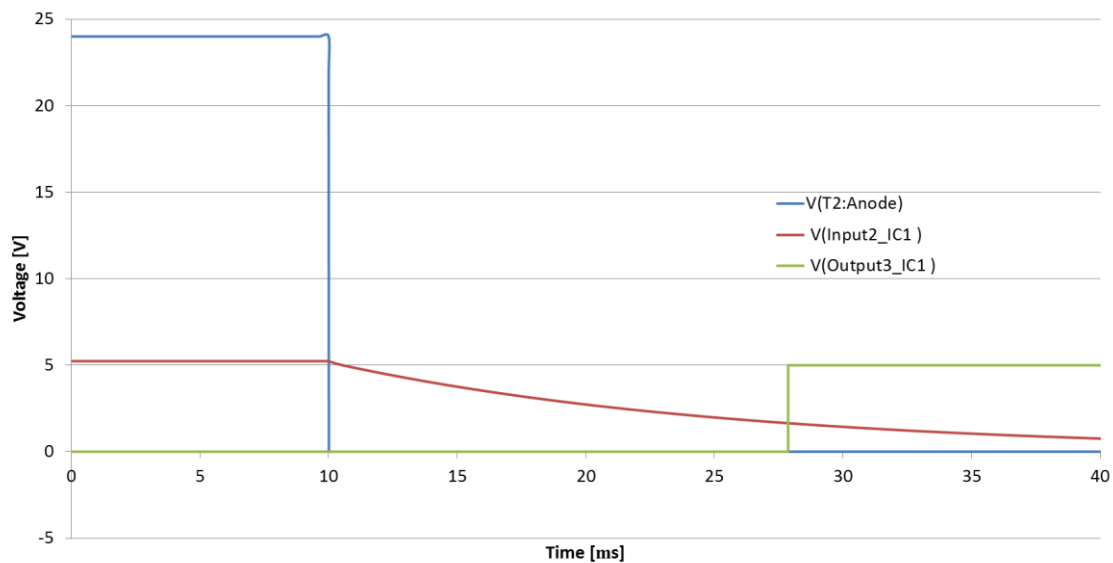


Figure 5.22: Voltage over time against ground, behaviour of IC1 in case of low thyristor voltage.

Most failure modes, like parameter changes or one open resistor, of the components connected to input 2 result in a non-critical change of the time after which IC1 will trigger an error signal. Connecting the voltage monitoring to ground or opening the thyristor monitoring path will cause a Synchronous Beam Dump. As an example, Figure 5.23 shows the behaviour of IC1 in case of a short in R21 or R22 at $t = 5$ ms. In this case the thyristor voltage is connected to ground causing the voltage at input 2 (red) to change to 0 V. The Schmitt trigger switches its state immediately (green). This causes an error signal although the thyristor voltage stays high (blue).

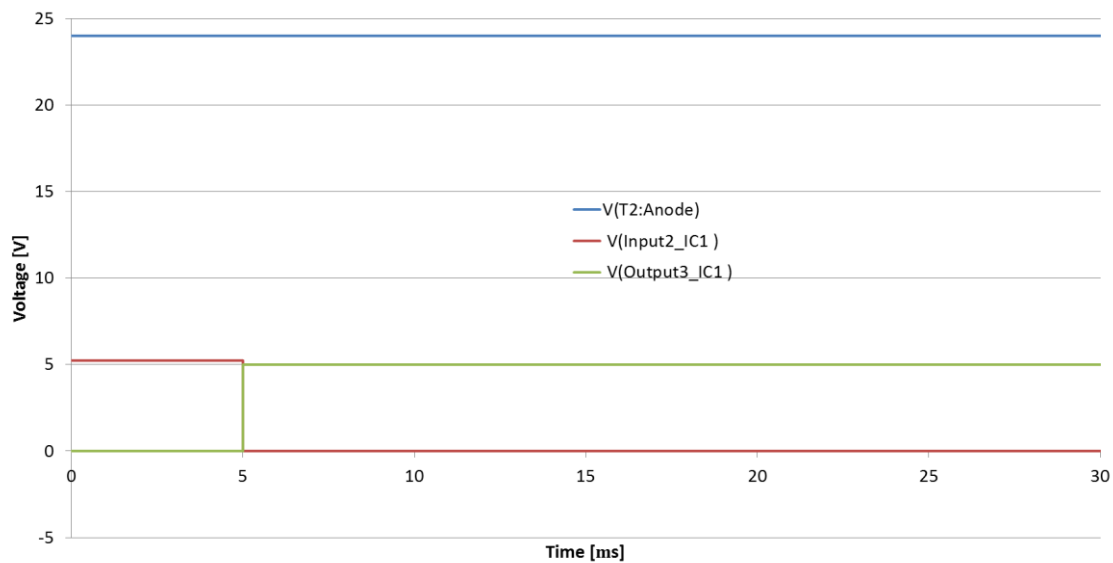


Figure 5.23: Behaviour of IC1 in case of a short in R21 or R22 at $t = 5$ ms. Voltages over time against ground.

All failure modes of the interlock circuit which will trigger an error signal due to a false signal at input 2 of IC1 are listed in Table 5.13.

Table 5.13: Component failures causing Synchronous Beam Dumps for input 2 of IC1.

R20-R23, C13		
Failure Mode Description	$\lambda_{\text{MIL-HDBK}}$ [FIT]	$\lambda_{\text{Manufacturer}}$ [FIT]
Short R20	0.01	n.a.
Short R21	0.01	n.a.
Open R22	0.10	n.a.
Open R23	0.10	n.a.
Short C13	3.89	2

Input 8 of IC1 is used to monitor the connection of the output cable to the Re-triggering Lines (see Figure 5.21, violet). The output cable from the TDU contains two pairs of wires, one for the trigger signal and one for the interlock loop. At the end of the cable the interlock loop must be closed to make sure, that the cable is connected properly [24]. Shorts in the capacitor C20 and the resistor R19 will connect the interlock loop to ground while an open resistor R43 will break the loop. The FITs of these failures are summarized in Table 5.14.

Table 5.14: Component failures causing Synchronous Beam Dumps for input 8 of IC1.

R19, R43, C20		
Failure Mode Description	$\lambda_{\text{MIL-HDBK}}$ [FIT]	$\lambda_{\text{Manufacturer}}$ [FIT]
Short R19	0.34	n.a.
Open R43	2.69	n.a.
Short C20	4.45	0.80

In addition to failures due to components connected to IC1 as discussed above, IC1 itself can cause Synchronous Beam Dumps. The manufacturer NXP Semiconductors provides a failure rate of 2.99 FIT for this device while the calculated failure rate according to MIL-HDB-217F is 29.4 FIT [19]. The failure rates can be distributed on two failure modes: ‘improper output’ (77 %) and ‘no output’ (23 %) [20]. The failure mode ‘improper output’ inverts the expected output signal while the failure mode ‘no output’ turns the output signal into the logic state FALSE.

Failures at the outputs 3, 4 and 10 of IC1 can cause Synchronous Beam Dumps shown in the truth tables above (see Table 5.10 and Table 5.11).

The failure mode ‘Improper outputs’ will always cause a Synchronous Beam Dump while the failure mode ‘no output’ will generate an error signal just at output 4 and 10. The failure mode ‘No output’ at output 3 and output 10 will not cause beam dumps but cause other failure effects: ‘No output’ at output 3 will turn off the monitoring of the thyristor voltage and the trigger line. In this failure mode output 3 is always false, independent from inputs 1 and 2. ‘No output’ at output 10 will additionally turn off the monitoring of the output cables and therefore deactivate the error signal creation. Note, that only six out of eight IC1 inputs and three out of four IC1 outputs are used to generate the error signal. The remaining inputs and outputs are considered in the next chapter ‘Warning Signals’. Table 5.15 shows failure modes for IC1 which will cause Synchronous Beam Dumps.

Table 5.15: IC1 failures causing Synchronous Beam Dumps.

IC1		
Failure Mode Description	$\lambda_{\text{MIL-HDBK}}$ [FIT]	$\lambda_{\text{Manufacturer}}$ [FIT]
Improper Output IC1	16.98	1.73
No Output (output 4) IC1	1.69	0.17

Three transistors are used to generate the error signal. Failure modes of two of them can cause false error signals: Two of three possible shorts in the transistors T5 (short from emitter to collector and from base to emitter) and all shorts in transistor T9 will activate the relay RL2. RL2 is also activated if the failure mode ‘open’ occurs at transistor T9. 27 % of transistor failures account for ‘open’ and 73 % for short. All transistors exhibit calculated failure rates of less than 2 FIT. Their failure modes leading to Synchronous Beam Dump are summarized in Table 5.16.

Table 5.16: Transistor failures causing Synchronous Beam Dumps in the trigger creation.

T5, T9.		
Failure Mode Description	$\lambda_{\text{MIL-HDBK}}$ [FIT]	$\lambda_{\text{Manufacturer}}$ [FIT]
Short T5 (emitter to collector)	0.29	n.a.
Short T5 (base to emitter)	0.29	n.a.
Short T9	0.83	n.a.
Open T9	0.31	n.a.

From the components connected to the transistors only two resistors, R39 and R40, can cause Synchronous Beam Dumps in case of a failure. Table 5.17 summarizes the failure modes and the FITs for these resistors.

Table 5.17: R39, R40 failures causing Synchronous Beam Dumps.

R39, R40		
Failure Mode Description	$\lambda_{\text{MIL-HDBK}}$ [FIT]	$\lambda_{\text{Manufacturer}}$ [FIT]
Short R39	0.11	n.a.
Short R40	0.19	n.a.
Open R39	1.24	n.a.
Open R40	2.29	n.a.

The relay RL2 is the last component in the chain for error singals. When the relay switches, an error signal is forwarded to the connected PLC. According to MIL-HDBK-338B relays fail in the failure modes ‘fails to trip’ (55 %), ‘spurious trip’ (26 %) and ‘short’ (19 %). The most common failure ‘fails to trip’ prevents the relay to switch. It will deactivate the error signal generation in case of a TDU. No Synchronous Beam Dump will be triggered. Spurious trips (RL2 switches without a demand) and short circuits in RL2 will cause Synchronous Beam Dumps by activating the connected PLC. Due to its calculated failure rate of 165.3 FIT it is one of the top contributing components in the interlock circuit to the failure effect Synchronous Beam Dump. Table 5.18 shows the respective failure rates for these failure modes.

Table 5.18: RL2 relay failures causing Synchronous Beam Dumps.

RL2		
Failure Mode Description	$\lambda_{\text{MIL-HDBK}}$ [FIT]	$\lambda_{\text{Manufacturer}}$ [FIT]
Spurious Trip RL2	42.98	n.a.
Short RL2	31.04	n.a.

The sum of the failure rates in the TDU250 interlock circuit is shown below as calculated from the military handbook (5.13), and from the manufacturer data (5.14).

$$\lambda_{SBD_TDIC_MIL} = \mathbf{116.38\ FIT.} \quad (5.13)$$

$$\lambda_{SBD_TDIC_MAN} = \mathbf{92.10\ FIT.} \quad (5.14)$$

The inverse of the failure rates lead to the according *MTTF*, shown in Equations (5.15) and (5.16):

$$MTTF_{SBD_TDIC_MIL} = \frac{1}{116.38\ FIT} \approx \mathbf{981\ years.} \quad (5.15)$$

$$MTTF_{SBD_TDIC_MAN} = \frac{1}{92.10\ FIT} \approx \mathbf{1239\ years.} \quad (5.16)$$

Warning Signals

Warning signals from the interlock circuit related to the loss of one of the two redundant power supplies are not critical for the LHC operation since they do not cause a beam dump. If a warning signal is generated, the re-arming of the LHC will be inhibited in order to replace the faulty power supply. Failures in the components of the interlock circuit can also cause warning signals. In this case the TDU itself must be replaced.

The power supplies are connected to input 12 or input 13 of IC1 respectively. Figure 5.24 shows the behaviour of the circuit in case of a faulty power supply at $t = 10\ ms$. The resistors R32 and R31 respectively limit the 24 V power supply voltage (blue in Figure 5.24) to 5.5 V at input 12 (13, red) of IC1. In the moment when the failure occurs, the input voltage to input 12 (13) begins to decline. The slope is determined by R34 and C19 (R30, C15). The Schmitt trigger output switches after 19 ms to high (green).

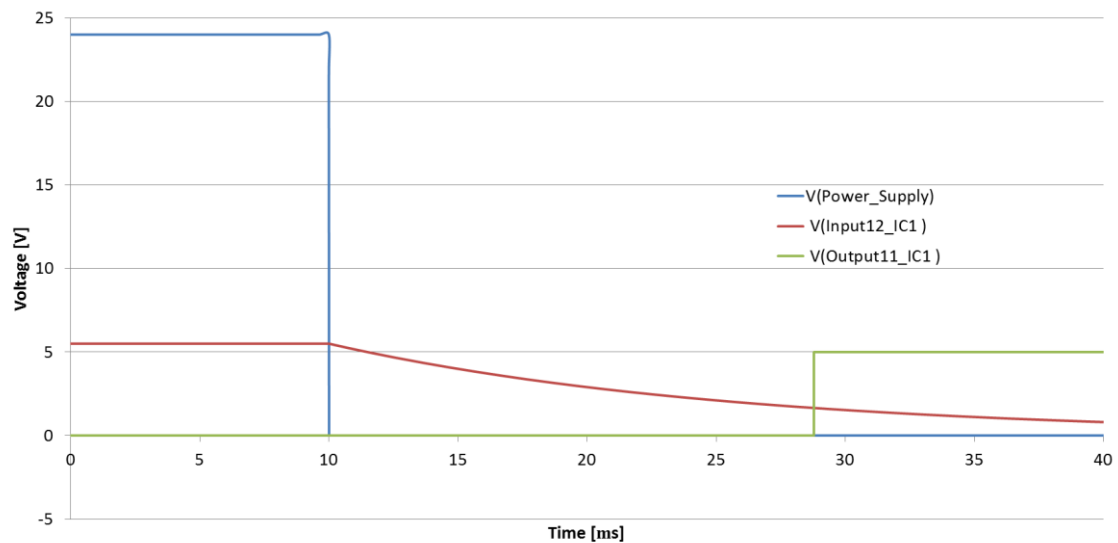


Figure 5.24: Voltage over time against ground, behaviour of IC1 in case of a faulty power supply.

Failures in components connected to inputs 12 and 13 can cause warning signals without a faulty power supplies. While parameter changes in these components result in an uncritical change of the time after which IC1 will trigger a warning signal, other failures will cause warning signals: Shorts in R30, R34, C15 or C19 connect one power supply to ground. An open R31 or R32 will disconnect the power supplies from the inputs of IC1. Both failure modes will lead to low voltage at input 12 or 13 of IC1. Table 5.19 shows corresponding failure rates to these failure modes.

Table 5.19: Component failures causing low voltage for input 12 or 13 of IC1.

R30-R32, R34, C15, C19		
Failure Mode Description	$\lambda_{\text{MIL-HDBK}}$ [FIT]	$\lambda_{\text{Manufacturer}}$ [FIT]
Short R30	0.07	n.a.
Short R34	0.07	n.a.
Short R31	0.14	n.a.
Short R32	0.14	n.a.
Open R31	1.67	n.a.
Open R32	1.67	n.a.
Short C15	4.27	2
Short C19	4.27	2

An ‘improper output’ at output 11 (false high output) of IC1 will also cause the generation of a warning signal by activating the connected transistors, similar to the failure at output 3 of IC1 (Synchronous Beam Dump). If the failure mode ‘no output’ occurs, the power supply

monitoring will be switched off – output 11 will always stay low, independent from inputs 12 and 13. The failure mode and failure rate to cause warning signals are listed in Table 5.20.

Table 5.20: IC1 failures causing warning signals.

IC1		
Failure Mode Description	$\lambda_{\text{MIL-HDBK}}$ [FIT]	$\lambda_{\text{Manufacturer}}$ [FIT]
Improper Output IC1 output 11	5.67	0.58

The components used to create the warning signal are identical to the components to create error signals. Therefore the failure modes listed in Table 5.16 to Table 5.17 are still valid but lead to a warning signal instead of an error signal. The failures are summarized in Table 5.21.

Table 5.21: Failures causing warning signals in the signal creation part.

T4, T8, RL1, R36, R37		
Failure Mode Description	$\lambda_{\text{MIL-HDBK}}$ [FIT]	$\lambda_{\text{Manufacturer}}$ [FIT]
Short T4 (emitter to collector)	0.29	n.a.
Short T4 (base to emitter)	0.29	n.a.
Short T8	0.83	n.a.
Open T8	0.31	n.a.
Spurious Trip RL1	42.98	n.a.
Short RL1	31.04	n.a.
Short R36	0.11	n.a.
Short R37	0.19	n.a.
Open R36	1.24	n.a.
Open R37	2.29	n.a.

The summed failure rates to generate warning signals are shown in the following equations. Equation (5.17) shows the failure rate calculated from the military handbook, Equation (5.18) considers the manufacturer data if available.

$$\lambda_{TDU_WARNING_MIL} = 97.54 \text{ FIT.} \quad (5.17)$$

$$\lambda_{TDU_WARNING_MAN} = 87.91 \text{ FIT.} \quad (5.18)$$

The respective *MTTFs* are given below:

$$MTTF_{TDU_WARNING_MIL} = \frac{1}{97.54 \text{ FIT}} \approx \mathbf{1170 \text{ years.}} \quad (5.19)$$

$$MTTF_{TDU_WARNING_MAN} = \frac{1}{87.91 \text{ FIT}} \approx \mathbf{1299 \text{ years.}} \quad (5.20)$$

5.2.3 Trigger Delay Unit Summary

The reliability analysis of the Trigger Delay Unit has shown that failures of components can cause Synchronous and Asynchronous Beam Dumps. While only the delay circuit can cause Asynchronous Beam Dumps, Synchronous Beam Dumps can be also provoked by the interlock circuit. The failure rate of the TDU250 for causing Asynchronous Beam Dumps with calculated failure rates is

$$\lambda_{ABD_TDU_MIL} = \lambda_{ABD_TDC_MIL} = \mathbf{61.74 \text{ FIT.}} \quad (5.21)$$

Taking into account data from the manufacturers, the failure rate becomes

$$\lambda_{ABD_TDU_MAN} = \lambda_{ABD_TDC_MAN} = \mathbf{55.07 \text{ FIT.}} \quad (5.22)$$

Six components contribute to these failure rates. Figure 5.25 shows their share for the calculated (left) and manufacturer (right) failure rates. The most critical component is MOSFET T1, contributing 48 % respectively 54 %. The trigger transformer TR1, connected directly to the Re-triggering Lines, is the second contributor with 27 % (31 %). The four remaining components (CL, D1, D7 and L1) only account for 25 % (15 %) of the failures.

The amount of expected Asynchronous Beam Dumps from one TDU250 within 10 years of operation is between 4.8×10^{-3} (Manufacturer) and 5.4×10^{-3} (MIL-HDBK).

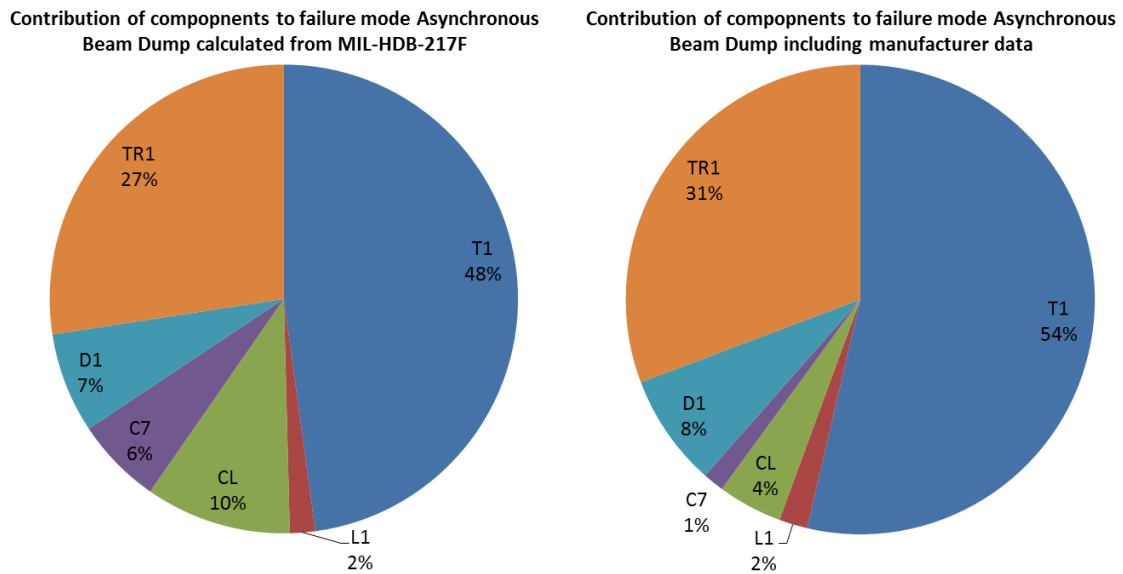


Figure 5.25: Contribution of components of TDU250 to the failure mode Asynchronous Beam Dump. Left: share of components, failure rates calculated from MIL-HDBK-217F. Right: share of components, failure rates complemented with data from manufacturers (if available).

Failure modes of 23 components of the TDU250 contribute to the probability for Synchronous Beam Dumps. Table 5.22 lists these components with their respective failure rates.

Table 5.22: Summary of all components in the TDU250, which contribute to Synchronous Beam Dumps.

Component	$\lambda_{\text{MIL-HDBK}}$ [FIT]	$\lambda_{\text{Manufacturer}}$ [FIT]
C13	3.89	2.00
C18	3.97	2.00
C20	4.45	0.08
C8	8.38	0.80
CL	5.39	.10
D1	5.81	n.a.
IC1	18.67	1.90
R11	4.42	n.a.
R19	0.34	n.a.
R20	0.01	n.a.
R21	0.01	n.a.
R22	0.10	n.a.
R23	0.10	n.a.
R28	0.34	n.a.
R29	1.54	n.a.
R33	0.70	n.a.
R39	1.35	n.a.
R40	2.48	n.a.
R43	2.69	n.a.
RL2	74.02	n.a.
T2	20.42	n.a.
T5	0.58	n.a.
T9	1.14	n.a.

The total failure rate for Synchronous Beam Dumps is the sum of the failure rates of the trigger delay circuit and the interlock circuit. The calculated failure rate (MIL-HDBK-217F) is

$$\lambda_{\text{SBD_TDU_MIL}} = \lambda_{\text{SBD_TDC_MIL}} + \lambda_{\text{SBD_TDIC_MIL}} = \mathbf{160.80 \text{ FIT}}. \quad (5.23)$$

With the failure rates provided from the manufacturers it becomes

$$\lambda_{\text{SBD_TDU_MAN}} = \lambda_{\text{SBD_TDC_MAN}} + \lambda_{\text{SBD_TDIC_MAN}} = \mathbf{125.65 \text{ FIT}}. \quad (5.24)$$

Figure 5.26 shows the share of the different components to the failure mode Synchronous Beam Dump for calculated (left) and manufacturer (right) failure rates. The relay RL2 (46 %), thyristor T2 (13 %) and Schmitt trigger IC1 (11 %) are the top three contributors for only

calculated failure rates. For both RL2 and T2 no manufacturer data was available. The manufacturer NXP provides a failure rate of 2.99 FIT for Schmitt trigger IC1 compared to calculated 29.4 FIT. Therefore the top contributors to the failure mode Synchronous Beam Dump change when this data is considered: The relay RL2 (59 %) is followed by thyristor T2 (16 %) and diode D1 (5 %).

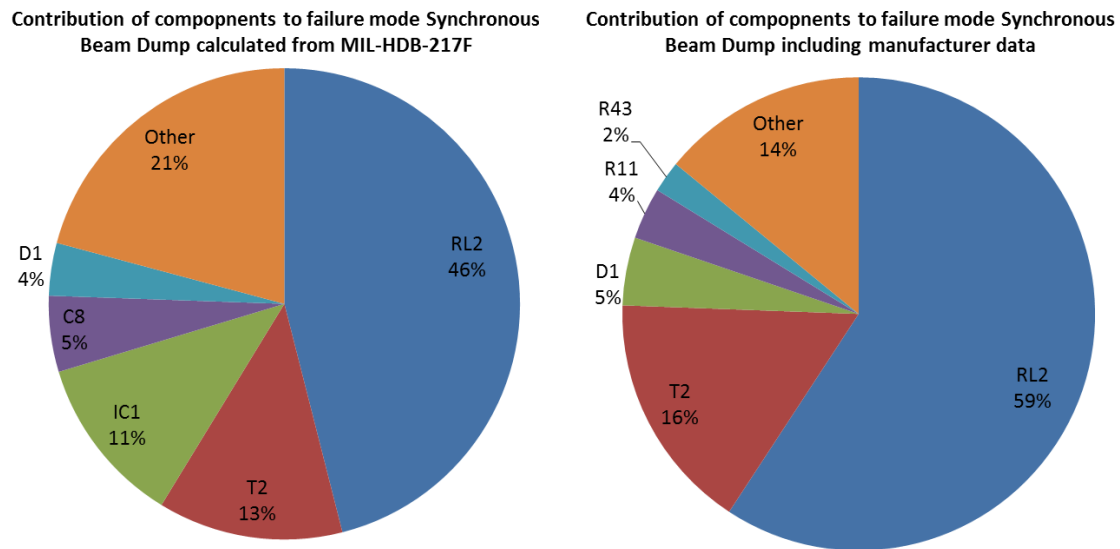


Figure 5.26: Contribution of components of TDU250 to the failure mode Synchronous Beam Dump. Left: share of components, failure rates calculated from MIL-HDBK-217F. Right: share of components, failure rates complemented with data from manufacturers (if available).

Figure 5.27 and Figure 5.28 show the probability over time for the failure mode Asynchronous Beam Dump (red) and Synchronous Beam Dump (blue, straight line) for one TDU250. The curves in Figure 5.27 are based on calculations from the MIL-HDB-217F whereas Figure 5.28 also considers the manufacturer data. The failure Synchronous Beam Dump can occur in the trigger delay circuit (TDC, blue dotted) and in the interlock circuit (TDIC, blue dashed). The prediction depicts a 10 % probability for a Synchronous Beam Dump caused by the TDU250 within a period of 75 years or 96 years with manufacturer data. For Asynchronous Beam the 10 % probability is reached after 195 years or 218 years including manufacturer data.

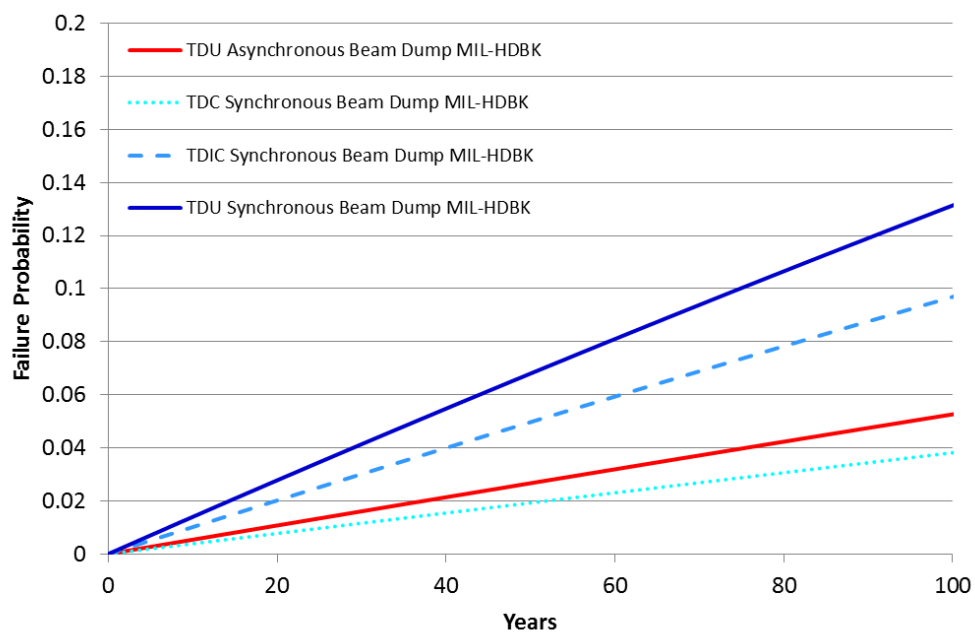


Figure 5.27: Failure probability over time for Synchronous Beam Dumps and Asynchronous Beam Dumps in the TDU250 calculated from MIL-HDBK-217F.

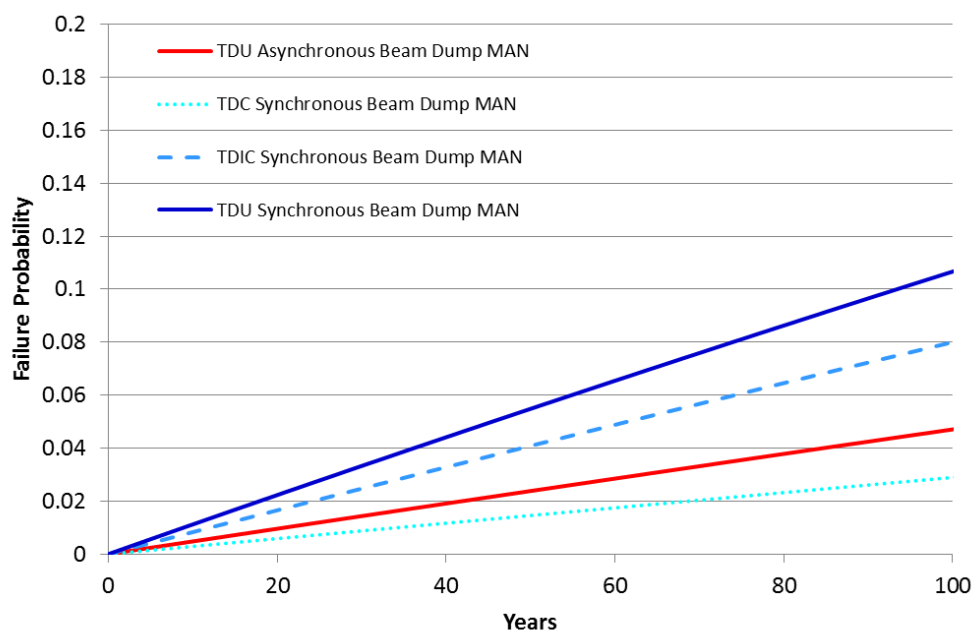


Figure 5.28: Failure probability over time for Synchronous Beam Dumps and Asynchronous Beam Dumps in the TDU250 including failure data from manufacturers.

Only the trigger delay circuit can cause unavailability on demand. In this failure mode, an incoming trigger will not be forwarded to the Re-triggering Lines. This failure can be detected after each beam dump when the signals from the TDU250 are checked. The LHC operation will be paused to replace the faulty TDU. Twenty components contribute to the total failure rate for this mode, shown in Equations (5.25) and (5.26).

$$\lambda_{TDU_N/A_MIL} = \mathbf{130.04\ FIT.} \quad (5.25)$$

$$\lambda_{TDU_N/A_MAN} = \mathbf{122.45\ FIT.} \quad (5.26)$$

Failures in components in the interlock circuit can cause warning signals although the power supplies are faultless. Similar to the unavailability on demand, these failures will cause a stop of LHC operation after the next beam dump. According failure rates are listed below:

$$\lambda_{TDU_WARNING_MIL} = \mathbf{97.54\ FIT.} \quad (5.27)$$

$$\lambda_{TDU_WARNING_MAN} = \mathbf{87.91\ FIT.} \quad (5.28)$$

Table 5.23 summarizes the respective *MTTFs* for the different failure modes of the TDU250.

Table 5.23: *MTTFs* for different failure modes in the TDU250.

	MTTF [years] MIL-HDBK-217F	MTTF [years] Manufacturer Data
Asynchronous Beam Dumps	1849	2073
Synchronous Beam Dumps	710	909
TDU unavailable	875	932
Warning signals	1170	1299

The *MTTF* for all failure modes exceed the expected lifetime of the TDU250 and LHC operation considerably.

Influence of two Capacitors in the Harmonic Oscillator on the Reliability

The results above are based on a Trigger Delay Unit which uses one capacitor and one inductor to determine the delay time of 250 μ s. It is considered to use two capacitors for determining the delay time in the harmonic oscillator instead of one. The influence of two capacitors on the reliability of the TDU is discussed in this chapter.

The period length of one harmonic oscillation is defined as shown in Equation (5.29):

$$T = 2\pi\sqrt{LC}. \quad (5.29)$$

To achieve a delay time of 250 μs with the given inductance of $L1 = 745 \mu\text{H}$ a capacitance of $C = 2.13 \mu\text{F}$ is required.

As an option, it is considered to use two parallel capacitors with capacitance of $CL1 = 680 \text{ nF}$ and $CL2 = 470 \text{ nF}$ since these are more common than 2.13 μF capacitors and therefore widely available to order. The usage of two resistors leads to an equivalent capacitance of

$$CL12 = CL1 + CL2 = 1.150 \mu\text{F}. \quad (5.30)$$

According to Equation (5.29) the inductance for $L2$ is calculated to $L2 = 1.377 \text{ mH}$. The custom inductor in the TDU250 can be adjusted to the required inductance by adding turns to the coil.

Figure 5.29 depicts an excerpt of the trigger delay circuit schematics with one capacitor (left) and the optional two capacitors (right).

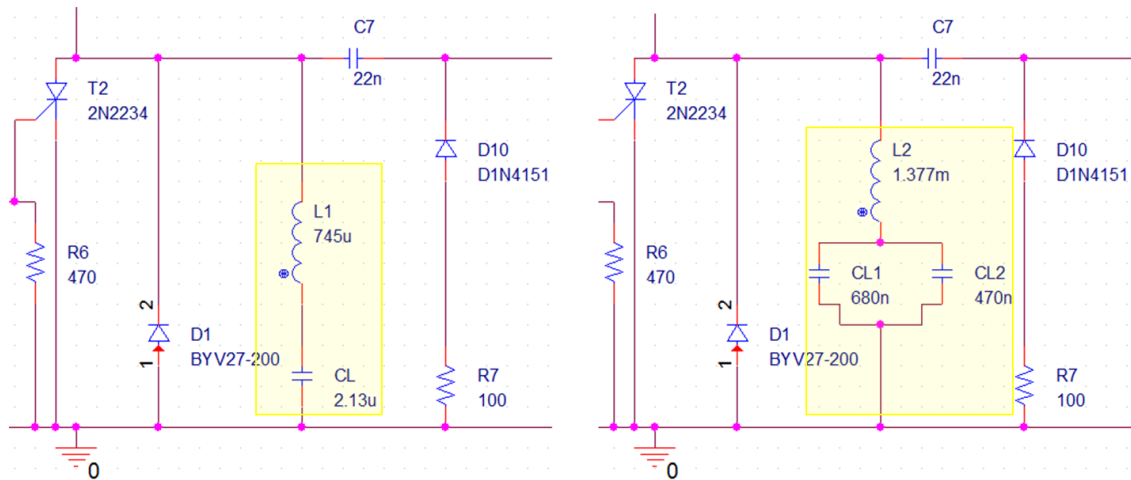


Figure 5.29: Left: LC oscillator in the TDU250 with one capacitor CL. Right: optional LC oscillator in the TDU250 with two capacitors CL1 and CL2.

Since the components are not finally chosen yet, no reliability data from manufacturers is available.

According to MIL-HDBK-217F [19], the calculated failure rate for the inductor is not dependent on the inductance, therefore the failure rate for $L1$ is equal to the failure rate of $L2$:

$$\lambda_{L1_MIL} = \lambda_{L2_MIL} = 2.159 \text{ FIT}. \quad (5.31)$$

The failure rates of capacitors are dependent on their capacitance. With a rated voltage of 63 V for both capacitors CL1 and CL2 the calculated failure rates are

$$\lambda_{CL1_MIL} = \mathbf{11.81\ FIT} \quad (5.32)$$

and

$$\lambda_{CL2_MIL} = \mathbf{11.42\ FIT}. \quad (5.33)$$

The failure modes and their probability for capacitors according to MIL-HDBK-338B are

- 42 % open,
- 40 % short,
- 18 % parameter changes.

Open capacitors will shorten the delay time significantly to 161 μs (open CL1) or 195 μs (open CL2). Therefore they will be accounted to the failure mode Asynchronous Beam Dump. Figure 5.30 shows the voltage over time at different elements in the delay circuit for the failure case open CL1. The trigger input (green) at $t = 10\ \mu\text{s}$ start the oscillation in the circuit. The open capacitor CL1 has the effect that only CL2 determines the delay time (red), therefore the delay for the output signal is shortened, as explained, to 161 μs . The trigger output signal (blue) emerges at $t = 171\ \mu\text{s}$.

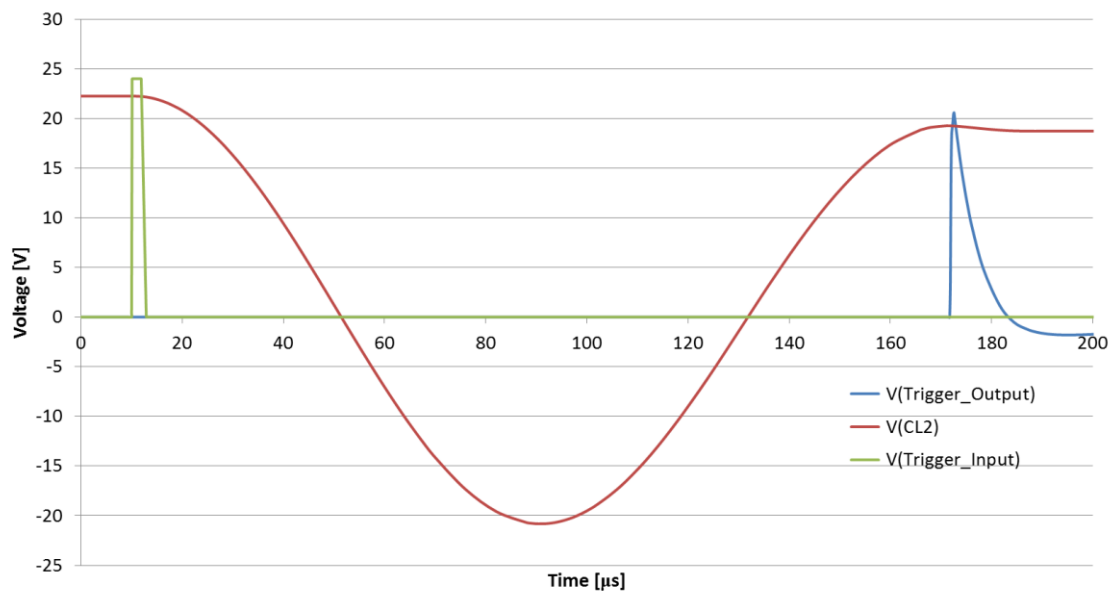


Figure 5.30: Voltage over time against ground in the trigger delay circuit in case of an open capacitor CL1.

Following the assumptions made in Chapter 5.2.1 Asynchronous Beam Dumps concerning parameter changes in the oscillator capacitor, half of the parameter changes are unacceptable and will also be accounted to Asynchronous Beam Dumps. Table 5.24 summarizes the failures of CL1 and CL2 which will cause an Asynchronous Beam Dump.

Table 5.24: Failures in CL1 and CL2 contributing to false Asynchronous Beam Dumps.

CL1, CL2		
Failure Mode Description	$\lambda_{\text{MIL-HDBK}}$ [FIT]	$\lambda_{\text{Manufacturer}}$ [FIT]
Open CL1	4.96	n.a.
Parameter Change CL1	1.0	n.a.
Open CL2	4.80	n.a.
Parameter Change CL2	1.03	n.a.

Shorts in both capacitors CL1 and CL2 will connect the anode of thyristor T2 to ground and therefore cause a Synchronous Beam Dump via the interlock circuit. The failure rates are listed in Table 5.25.

Table 5.25: Failures in CL1 and CL2 contributing to false Synchronous Beam Dumps.

CL1, CL2		
Failure Mode Description	$\lambda_{\text{MIL-HDBK}}$ [FIT]	$\lambda_{\text{Manufacturer}}$ [FIT]
Short CL1	4.72	n.a.
Short CL2	4.57	n.a.

Table 5.26 shows the impact of using two capacitors CL1 and CL2 in the trigger delay circuit on Asynchronous and Synchronous Beam Dumps in comparison to using one capacitor CL.

Table 5.26: Comparison of one and two capacitors in the trigger delay circuit oscillator on the failure modes Asynchronous and Synchronous Beam Dump.

	One capacitor CL $\lambda_{\text{MIL-HDBK}}$ [FIT]	Two capacitors CL1 and CL2 $\lambda_{\text{MIL-HDBK}}$ [FIT]
Asynchronous Beam Dumps	6.22	10.79
Synchronous Beam Dumps	5.39	9.29

The total failure rate for Asynchronous Beam Dumps caused by the TDU will therefore rise to 66.31 FIT with two capacitors in use, which is 7.4 % more than the original failure rate 61.74 FIT. The expected amount of Asynchronous Beam Dumps in ten years of operation is calculated to 5.81×10^{-3} .

The failure rate for Synchronous Beam Dumps in the TDU changes to 164.70 FIT, 2.4 % more than the failure rate with only one capacitor CL (160.80 FIT). The expected amount of Synchronous Beam Dumps per year is calculated to 1.44×10^{-3} .

5.3 Beam Interlock Controller Dumping System

The Beam Interlock Controller Dumping System (CIBDS), located between the BIS and the TDU250, serves three main functions.

- It is used as a detector for the beam permit A and B and will generate a trigger to the TDU when this permit is lost.
- To minimise Asynchronous Beam Dumps in case of spurious triggers, the CIBDS dump request trigger is also connected to a CIBU. Thus, it is also giving a User Permit signal to the BIS [28].
- The CIBDS can mask beam dump requests when the LBDS is operating in Local Mode (Local Mode A and Local Mode B) described in Chapter 5.3.3.

A functional diagram of the CIBDS is shown in Figure 5.31.

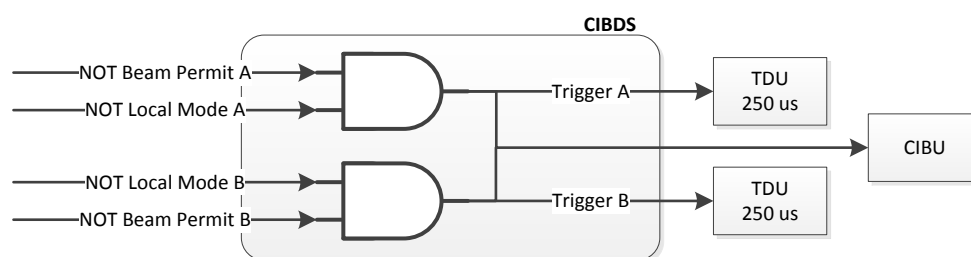


Figure 5.31: Functional diagram of the CIBDS.

The inverted beam permit - and local mode signals are combined via an AND gate. The analogue part of the CIBDS implements above mentioned functions except the detection of the beam permit. Figure 5.32 shows the layout of the CIBDS board. Two CPLDs (IC1 and IC2, not shown in Figure 5.32) detect the beam permits and provide the LOCAL_PERMIT_A and LOCAL_PERMIT_B signals (blue) for the logic gates IC16 and IC20 (green). The logic between the BIS beam permit and the LOCAL_PERMIT is inverted, see Table 5.27. The CPLD output is 0 V if beam permit is given and 3.3 V if beam permit is lost.

Table 5.27: Truth table, LHC beam permit to CIBDS Local Permit.

Beam Permit	LOCAL_PERMIT	CPLD Output
TRUE	FALSE	0 V
FALSE	TRUE	3.3 V

A high output at the logic gates will generate a pulse in the MOSFET Drivers IC4 and IC5 (red). The inverted Outputs 7 of the MOSFET Drivers are used to revoke the BIS User Permit via a CIBU at the connector LM6.

The majority of the components in the circuit (yellow) are used to mask the beam dump requests in LBDS Local Mode.

In the following, the implementations of the different functionalities in the CIBDS are explained and the component failure modes and their effects are analysed. The failure modes of the system will be presented based on the effect they have on the system behaviour.

The main failure effects are:

- False Asynchronous Beam Dumps;
- False Synchronous Beam Dumps;
- Detectable failures causing downtime or maintenance.

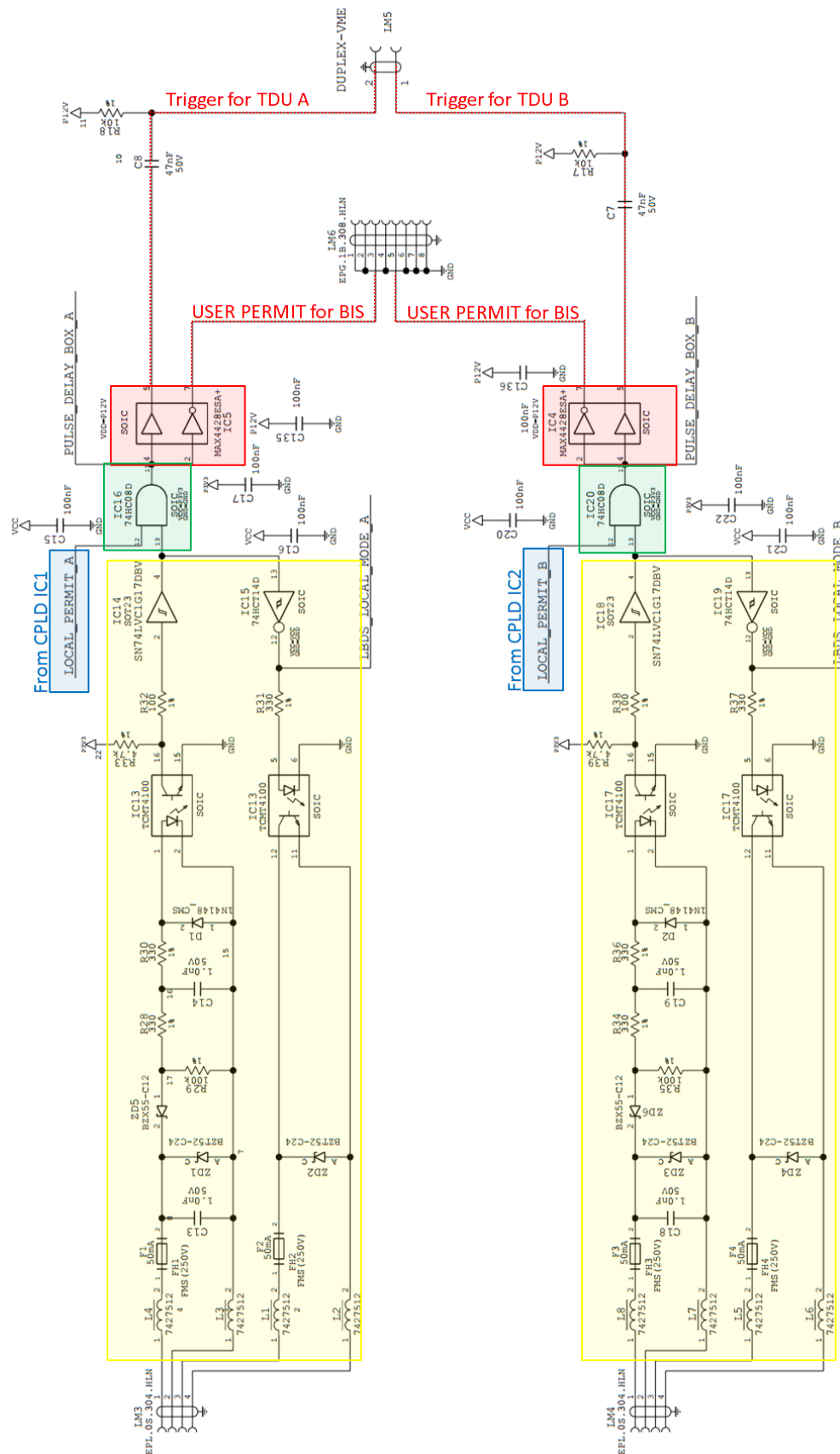


Figure 5.32: CIBDS schematics [25].

5.3.1 Beam Permit Flag

A Complex Programmable Logic Device (CPLD) is used to check the beam permit flag (BPF) of the BIS. It is programmed with a VHDL (VHSIC Hardware Description Language) code. The CPLD listens to the BIS loop and measures the frequency of the optical signal. If it falls under a threshold, the CPLD output will turn high and therefore demand a beam dump request.

The calculated failure rate for the CPLD is 26.08 FIT. The supplier XILINX provides a failure rate of 5 FIT at a confidence level of 60 % according to the latest Device Reliability Report [29]. Table 5.28 provides failure modes and their distribution for the CPLDs according to MIL-HDBK-338B [20].

Table 5.28: CPLD failure modes and their distribution [20].

Device type	Components in Circuit	Failure Mode	Mode Probability
Microcircuit	IC1, IC2	Output Stuck Low	28 %
		Output Stuck High	28 %
		Input Open	22 %
		Output Open	22 %

Asynchronous Beam Dumps are not expected due to failures in the CPLDs since the MOSFET Drivers will open the BIS loop when the CPLDs trigger and hence demand a Synchronous Beam Dump.

Synchronous Beam Dumps

Only one failure mode will lead to a Synchronous Beam Dump request: Open inputs within the CPLDs will induce a beam dump request (output of IC1 turns high). The dump request is distributed simultaneously via the connected MOSFET driver to the TDU and to the CPLD which will open the BIS loop. Table 5.29 shows the failure rates to the failure mode ‘Input Open’.

Table 5.29: Synchronous Beam Dumps caused by the microprocessors IC1 and IC2.

IC1, IC2		
Failure Mode Description	$\lambda_{\text{MIL-HDBK}} [\text{FIT}]$	$\lambda_{\text{Manufacturer}} [\text{FIT}]$
Input Open IC1	5.74	1.10
Input Open IC2	5.74	1.10

The combined failure rate of both CPLDs to cause a Synchronous Beam Dump is therefore

$$\lambda_{\text{SBD_CIBDS_BPF_MIL}} = \mathbf{11.48 \text{ FIT.}} \quad (5.34)$$

Considering the data provided by manufacturer XILINX the failure rate is reduced to

$$\lambda_{SBD_CIBDS_BPF_MAN} = \mathbf{2.20\ FIT}. \quad (5.35)$$

Failures requiring maintenance

Failures of the CPLDs which do not cause a Synchronous Beam Dump will only prohibit the re-arming of the LHC after a beam dump.

The redundant design for the local permit will prevent the CIBDS to go blind if one CPLD fails. A missing output signal from one CPLD will cause one of the connected TDU250s not to trigger. The beam will be dumped via the second TDU250. During the post operational analysis the missing trigger will be identified and the faulty CIBDS needs to be replaced before re-arming the LHC. This failure mode will occur if the output of a CPLD is open or stuck low (CPLD unable to switch its output state from low to high). In case the output is stuck high after a beam dump request, the BIS loop will stay open and the CIBDS needs to be replaced as well. Additionally open inputs of IC1 and IC2 causing a Synchronous Beam Dump will also inhibit re-arming of the LHC since the outputs of CPLDs will permanently stay high. Thus, the failures are accounted to both, Synchronous Beam Dumps and failures requiring maintenance.

Table 5.30 shows the according failure rates for IC1 and IC2 failures leading to maintenance.

Table 5.30: Failures leading to maintenance caused by IC1 and IC2.

IC1, IC2 .		
Failure Mode Description	$\lambda_{MIL-HDBK}$ [FIT]	$\lambda_{Manufacturer}$ [FIT]
Output Open IC1	5.74	1.10
Output Open IC2	5.74	1.10
Output Stuck Low IC1	7.30	1.40
Output Stuck Low IC2	7.30	1.40
Output Stuck High IC1	7.30	1.40
Output Stuck High IC2	7.30	1.40
Input Open IC1	5.74	1.10
Input Open IC2	5.74	1.10

The summed failure rates are shown below calculated from MIL-HDBK-217F and for the data provided from the manufacturer XILINX.

$$\lambda_{MNTNC_CIBDS_BPF_MIL} = \mathbf{52.16\ FIT}. \quad (5.36)$$

$$\lambda_{MNTNC_CIBDS_BPF_MAN} = 10.00 \text{ FIT.} \quad (5.37)$$

5.3.2 Trigger for the TDU250

The trigger for the TDU250 is generated in the Dual High Speed MOSFET Drivers IC4 and IC5. The logic AND gate (Figure 5.32, green) connected to the MOSFET Driver input (red) combines the local beam permit and the LBDS Local Mode signal. If both inputs are TRUE⁴ a trigger is generated and passes via a high-pass filter (C8, R18 and C7, R17) directly to the TDU250 A and B.

Figure 5.33 shows the behaviour of MOSFET driver IC4 during normal operation (left) and in case of a beam dump request (right). The red arrows represent the logic state FALSE, green arrows the logic state TRUE.

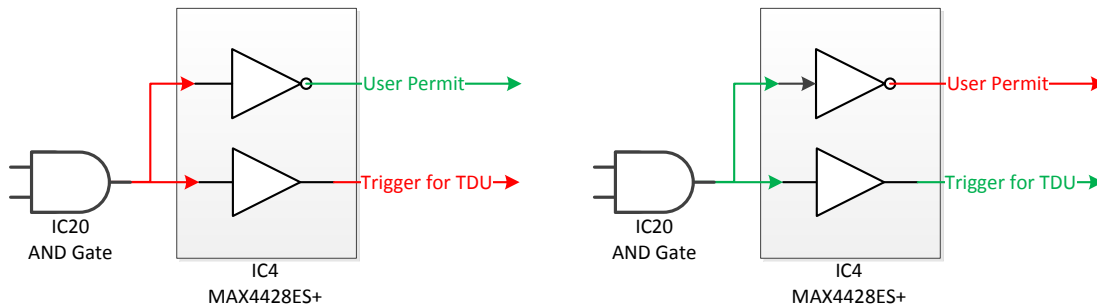


Figure 5.33: IC4 behaviour during normal operation (left) and in case of a beam dump request (right). Red arrows represent the logic state FALSE, green arrows the logic state TRUE.

The inverted outputs of the MOSFET drivers are used to forward the lost beam permit to the connected CIBU [28]. This connection exists to prevent Asynchronous Beam Dumps due to spurious triggers in the CIBDS. However there are failure modes which can cause Asynchronous Beam Dumps.

Asynchronous Beam Dumps

During regular operation output 5 of the MOSFET drivers IC4 and IC5 is low while output 7 is high. In case of an improper output 5, the CIBDS will directly trigger one TDU without opening the BIS loop and the connected TDU will cause an Asynchronous Beam Dumps after 250 μ s (see Figure 5.34).

⁴ When the Beam Permit is lost, LOCAL_PERMIT is TRUE (inverse logic by the CPLDs, see Table 5.27).

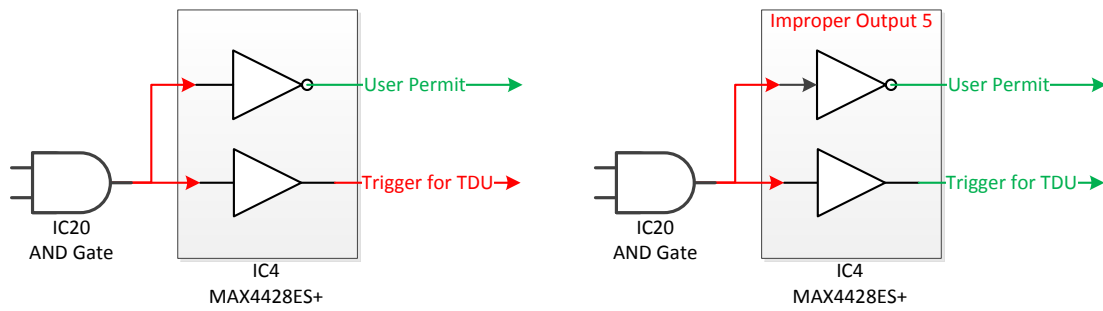


Figure 5.34: IC4 behaviour during normal operation (left) and in case of a failure at output 5 (right). Red arrows represent the logic state FALSE, green arrows the logic state TRUE.

The manufacturer MAXIM provides a failure rate of 1.93 FIT while the failure rate calculated with MIL-HDBK.217F is 12.85 FIT. The failure mode ‘improper output’ accounts for 77 % of the failures. The failure mode is divided evenly between the two outputs of the MOSFET drivers.

Shorts in R17 and R18, located after output 7 of the MOSFET drivers connect the TDU250 to the supply voltage of P12V. This is sufficient to trigger the TDU250s and generate an Asynchronous Beam Dump. The components used in the creation of the trigger for the TDU250 and their failure modes leading to an Asynchronous Beam Dump are listed in Table 5.31.

Table 5.31: Component failures leading to Asynchronous Beam Dumps in the CIBDS trigger creation.

IC4, IC5, R17, R18		
Failure Mode Description	$\lambda_{\text{MIL-HDBK}}$ [FIT]	$\lambda_{\text{Manufacturer}}$ [FIT]
Improper Output IC4 output 5	4.95	0.74
Improper Output IC5 output 5	4.95	0.74
Short R17	0.36	n.a.
Short R18	0.36	n.a.

The failure mode Asynchronous Beam Dump can only be caused in this part of the CIBDS. Therefore the total failure rate for the CIBDS is the same as the summed failure rates of Table 5.31:

$$\lambda_{\text{ABD_CIBDS_MIL}} = 10.62 \text{ FIT.} \quad (5.38)$$

Considering the manufacturer data for the MOSFET drivers IC4 and IC5, the failure rate becomes

$$\lambda_{ABD_CIBDS_MAN} = 2.20 \text{ FIT.} \quad (5.39)$$

Synchronous Beam Dumps

A Synchronous Beam Dump in the trigger creation can only be caused within IC4 and IC5 since these components are directly connected to the CIBU.

The same failure mode causing an Asynchronous Beam Dump can cause a Synchronous Beam Dump at the inverted output 7 of IC4 and IC5. The failure mode ‘improper output’ at output 7 is shown in Figure 5.35. The User Permit for the BIS is revoked (right) and the beam will be dumped via the LBDS.

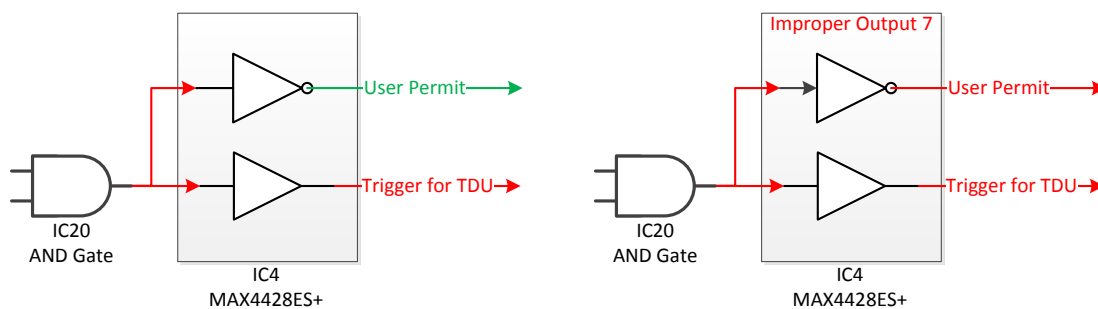


Figure 5.35: IC4 / IC5 behaviour during normal operation (left) and in case of a failure at output 7 (improper output, right). Red arrows represent the logic state FALSE, green arrows the logic state TRUE.

In addition, an open output 7 will also lead to a Synchronous Beam Dump. Both failure modes will open the BIS Loop via a CIBU connected to LM6. Failure rates for the component failures leading to a Synchronous Beam Dump are listed in Table 5.32.

Table 5.32: MOSFET driver failures leading to Synchronous Beam Dumps in the CIBDS trigger creation.

IC4, IC5,		
Failure Mode Description	$\lambda_{\text{MIL-HDBK}}$ [FIT]	$\lambda_{\text{Manufacturer}}$ [FIT]
Improper Output IC4 output 7	4.95	0.74
Improper Output IC5 output 7	4.95	0.74
No Output IC4 output 7	1.48	0.22
No Output IC5 output 7	1.48	0.22

The summed failure rates of Table 5.32 result to the total failure rate for Synchronous Beam Dumps in the trigger production. The total failure rate for component failure rates calculated from MIL-HDBK-217F is

$$\lambda_{SBD_CIBDS_TRIG_MIL} = \mathbf{12.86 \text{ FIT}}. \quad (5.40)$$

With the data provided by the manufacturer data of MAXIM, the failure rate becomes

$$\lambda_{SBD_CIBDS_TRIG_MAN} = \mathbf{1.92 \text{ FIT}}. \quad (5.41)$$

Failures requiring maintenance

Failures in the trigger creation part of the CIBDS can require maintenance after a beam dump in two ways:

- A missing trigger signal from a TDU250. In this case the CIBDS has to be replaced.
- The CIBDS does not give the beam permit after a beam dump.

If output 5 of IC4 or IC5 or one of the ceramic capacitors C7 and C8 are open, the trigger cannot be forwarded to the TDU250. The missing trigger signal will be identified after a beam dump request and the faulty CIBDS has to be replaced. The failures are listed in Table 5.33

Table 5.33: Component failures requiring maintenance due to a missing TDU250 signal.

IC4, IC5, C7, C8		
Failure Mode Description	$\lambda_{\text{MIL-HDBK}}$ [FIT]	$\lambda_{\text{Manufacturer}}$ [FIT]
No Output IC4 output 5	1.48	0.22
No Output IC5 output 5	1.48	0.22
Open C7	6.61	n.a.
Open C8	6.61	n.a.

If output 7 of the MOSFET driver (IC4, IC5) stays low it will trigger a Synchronous Beam Dump and also inhibit the re-arming after the next beam dump (see Table 5.34). This failure mode is therefore assigned to Synchronous Beam Dumps and to failures requiring maintenance.

Table 5.34: Component failures leading to a Synchronous Beam Dump and requiring maintenance due to a missing TDU250 signal.

IC4, IC5,		
Failure Mode Description	$\lambda_{\text{MIL-HDBK}}$ [FIT]	$\lambda_{\text{Manufacturer}}$ [FIT]
No Output IC4 output 7	1.48	0.22
No Output IC5 output 7	1.48	0.22

The total failure rates for failures which require maintenance in the trigger production part of the CIBDS are shown below.

$$\lambda_{\text{MNTNC_CIBDS_TRIG_MIL}} = \mathbf{19.14 \text{ FIT.}} \quad (5.42)$$

$$\lambda_{\text{MNTNC_CIBDS_TRIG_MAN}} = \mathbf{14.10 \text{ FIT.}} \quad (5.43)$$

5.3.3 Trigger Masking in LBDS Local Mode

During technical stops the LBDS needs to perform tests. In this phase the LBDS is in the so-called Local Mode. In the Local Mode the connection between the LBDS and the BIS is masked to prevent a triggering of the kicker magnets from outside the LBDS. This must be preserved with the new link. Therefore the CIBDS checks if the LBDS is in Local Mode to inhibit the pulse generation.

Failures in this path can be critical since they can lead to a blind CIBDS path (wrong assumption of LBDS Local Mode state). Therefore a read back loop is integrated in the CIBDS to ensure the correct signal distribution.

Figure 5.36 shows the functionality of the trigger masking for one of the two local mode signal paths in the CIBDS in the case that the LBDS is not in local mode. Red arrows represent a logical FALSE state while green arrows represent a logical TRUE state. The first optocoupler IC13 inverts this signal⁵ and forwards it via the SCHMITT Trigger IC14 to the logical AND gate IC16. If the beam permit is lost, Local Permit A turns TRUE and IC16 will induce a trigger. The signal from IC14 is sent back to the LBDS PLC via an inverting SCHMITT Trigger IC15⁶ and the second input of the optocoupler IC13. If the LBDS PLC does not read back the same signal as it sent, it will trigger a Synchronous Beam Dump.

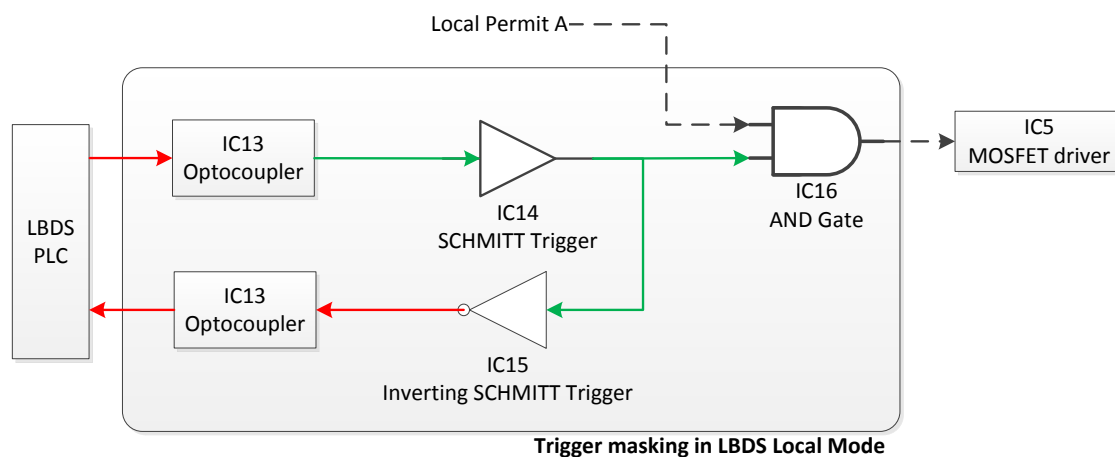


Figure 5.36: Functionality of the trigger masking of the CIBDS, LBDS not in Local Mode. Red arrows represent the logic state FALSE, green arrows the logic state TRUE.

Figure 5.37 shows the functionality of the trigger masking of the CIBDS in case the LBDS operates in local mode. The AND Gate IC16 inhibits a beam dump request since one input is always FALSE.

⁵ The implementation of the signal inversion is shown in Figure 5.40.

⁶ Currently, IC15 is an inverting Schmitt Trigger. It is considered to change this logic in the implementation. In this case, the LBDS PLC would trigger a Synchronous Beam Dump request if outgoing and incoming signals are the same.

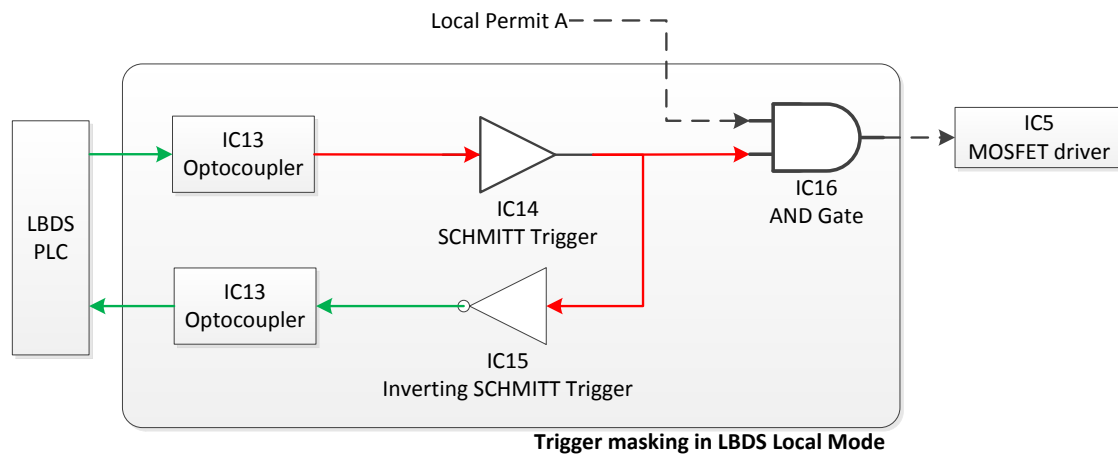


Figure 5.37: Functionality of the trigger masking of the CIBDS, LBDS is operating in Local Mode. Red arrows represent the logic state FALSE, green arrows the logic state TRUE.

Spurious failures in these key components can cause Synchronous Beam Dumps while permanent failures can prohibit the re-arming of the LHC.

Every time when the local mode is switched off, the CIBDS will trigger the TDU250 and hence an Asynchronous Beam Dump. This is a feature to test the functionality of the new system. The Asynchronous Beam Dump will be triggered without a beam in the LHC.

Synchronous Beam Dumps

The AND gates IC16 and IC20 (green in Figure 5.32) are directly connected to the input of the MOSFET drivers IC4 and IC5. According to MIL-HDB-338B [20] failures can cause an ‘improper output’ signal in 77 % of failure cases. The failure mode ‘improper output’ will cause the expected output signal to be inverted.

Figure 5.38 shows the behaviour of IC20 during normal operation (left) and in case of the failure mode ‘improper output’ (right). The LBDS is not in Local Mode and beam permit is given so one input is TRUE (green) while the second input is FALSE (red). IC20 usually does not trigger in this state but is ready to trigger if the beam permit is lost. In case of an improper output signal, the output of IC20 turns TRUE and the connected MOSFET driver will trigger the TDU250.

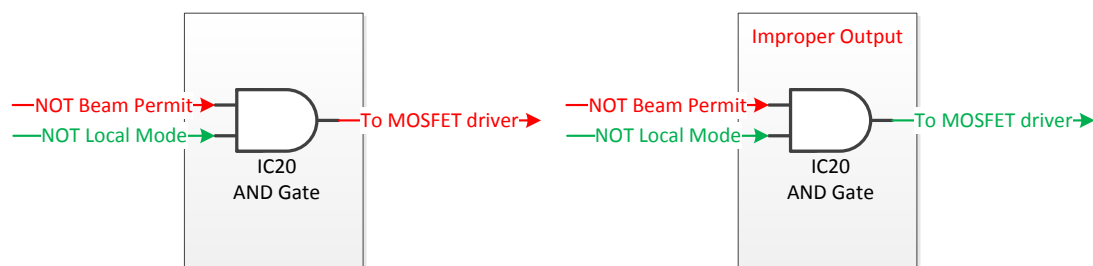


Figure 5.38: IC20 behaviour during normal operation (left) and in failure mode improper output (right). Red arrows represent the logic state FALSE, green arrows the logic state TRUE.

The failure case ‘no output’ (23 %) will cause one of the redundant CIBDS local mode paths to be blind but will not trigger a dump request. In this failure mode the output of the component is stuck low and not able to switch its state.

Manufacturer NXP provides a failure rate of 6.62 FIT for the AND gates IC16 and IC20. The failure rate calculated with MIL-HDBK-217F is 48.81 FIT. Failure modes causing Synchronous Beam Dumps are summarized in Table 5.35.

Table 5.35: AND gate failures in CIBDS causing Synchronous Beam Dumps.

IC16, IC20		
Failure Mode Description	$\lambda_{\text{MIL-HDBK}}$ [FIT]	$\lambda_{\text{Manufacturer}}$ [FIT]
Improper Output IC16	37.58	5.10
Improper Output IC20	37.58	5.10

The single Schmitt trigger buffers IC14 and IC18 made by Texas Instruments serves as a trigger for the AND gates IC16 and IC20. The outputs of IC14 and IC18 are the inverse of the LBDS Local Mode (TRUE if LBDS is not in Local Mode, see Figure 5.36).

The failure mode distribution of the single Schmitt trigger buffers is similar to the AND gates IC16 and IC20 (23 % ‘no output’, 77 % ‘improper output’). During LHC operation, the LBDS PLC does not send an output signal (see Figure 5.39). Optocoupler IC13 is not conducting and the input of IC14 is connected to a 3.3 V power supply⁷. The output of IC14 should be high. In case of an improper output signal of IC14, one input for IC16 is FALSE. In this state, IC16 will not forward dump requests. However, the read back loop via IC15 and IC13 (second input) will indicate to the LBDS PLC a failure in the CIBDS and the LBDS PLC will induce a beam dump request.

⁷ When IC13 is conducting (input of IC13 is TRUE) the 3.3 V supply voltage is connected to ground via the optocoupler emitter, therefore IC14 input will be FALSE, see Figure 5.40.

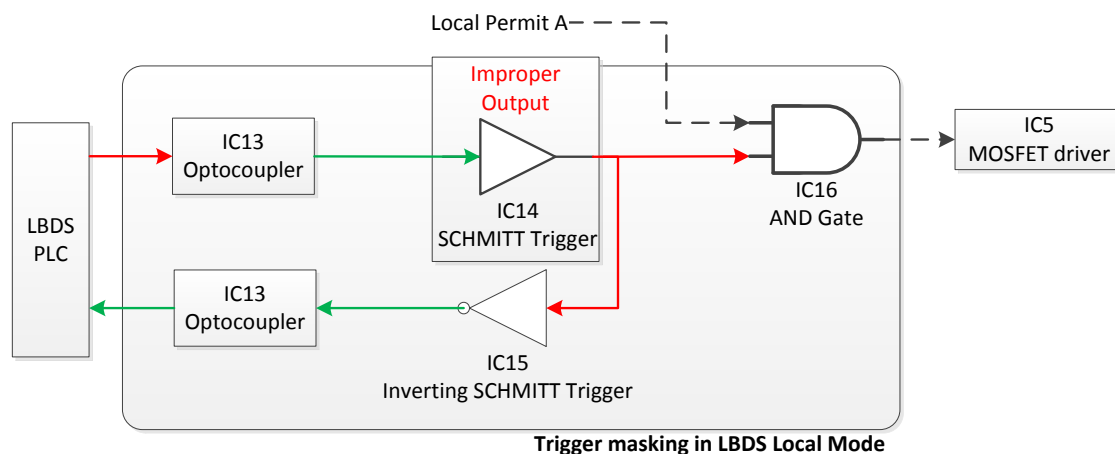


Figure 5.39: Schematic trigger masking functionality CIBDS, LBDS not in Local Mode: Failure at IC14 Schmitt trigger: improper output. Red arrows represent the logic state FALSE, green arrows the logic state TRUE.

The failure mode ‘no output’ will have the same effect to the PLC and will therefore also cause a Synchronous Beam Dump.

Due to the redundant Local Mode paths in the CIBDS, failures in the second Schmitt trigger IC18 will also cause a Synchronous Beam Dump. Texas Instruments provides a failure rate of 0.8 FIT while the calculated failure rate is 23.74 FIT. The failure modes and their failure rates are listed in Table 5.36

Table 5.36: Single Schmitt trigger buffer failures in CIBDS causing Synchronous Beam Dumps.

IC14, IC18		
Failure Mode Description	$\lambda_{\text{MIL-HDBK}}$ [FIT]	$\lambda_{\text{Manufacturer}}$ [FIT]
Improper Output IC14	18.28	0.62
No Output IC14	5.46	0.18
Improper Output IC18	18.28	0.62
No Output IC18	5.46	0.18

The inverting Schmitt triggers IC15 and IC19 of manufacturer NXP are located between the AND gate IC19/ IC20 and the optocouplers IC13/ IC17. An improper output of these inverting Schmitt triggers will produce a Synchronous Beam Dump because of the same reasons as IC14 and IC16: The LBDS PLC will read back a different signal than it sent. The failure mode ‘no output’ will not affect the LHC operation but the failure will be detected when the LBDS switches to Local Mode by the LBDS PLC. The calculated failure rate for an inverting Schmitt trigger is 15.01 FIT. NXP provides a failure rate of 6.62 FIT. The failure rates are summarized in Table 5.37.

Table 5.37: Inverting Schmitt trigger buffer failures in CIBDS causing Synchronous Beam Dumps.

IC15, IC19		
Failure Mode Description	$\lambda_{\text{MIL-HDBK}}$ [FIT]	$\lambda_{\text{Manufacturer}}$ [FIT]
Improper Output IC15	11.56	5.01
Improper Output IC19	11.56	5.01

The TCMT4100 optocoupler produced by Vishay (IC13 and IC17) has four channels. Two of them are used in each Local Mode path of the CIBDS. When the LBDS is not in Local Mode, the LED in the optocoupler is switched off (pins 1 and 2) and the phototransistor is not conducting. Therefore, Schmitt trigger IC14 is connected to the power supply P3V3 (see Figure 5.40). The output of inverting Schmitt trigger IC15 is turned off and the second channel of IC13 is therefore turned off as well (pins 5, 6, 12 and 11).

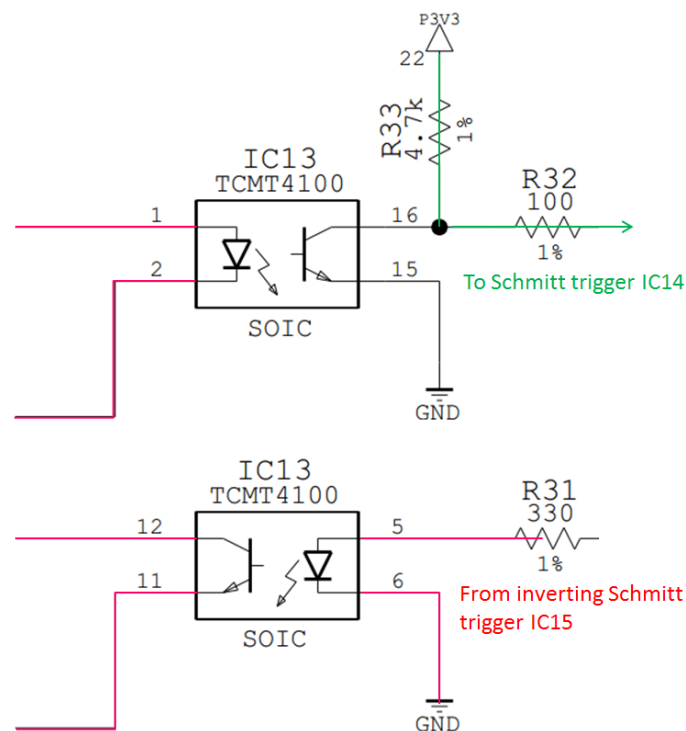


Figure 5.40: Excerpt of the CIBDS circuit layout around IC13, LBDS not in Local Mode. Red arrows represent the logic state FALSE, green arrows the logic state TRUE.

Failures in optocouplers can occur in optoelectronic LEDs and sensors [20]. The total failure rate of IC13 and IC17 will therefore be split up evenly to failure modes of the LED and the sensor. VISHAY provides a failure rate of 4 FIT. The calculated failure rate is 67.62 FIT (MIL-HDBK-217F). Table 5.38 shows the distribution of failures in these optocouplers.

Table 5.38: Optocoupler failure modes and distribution [20].

Device type	Components in Circuit	Failure Mode	Mode Probability
Optoelectronic LED	IC13, IC17	Open	70 %
		Short	30 %
Optoelectronic Sensor	IC13, IC17	Open	50 %
		Short	50 %

When the LBDS is in Local Mode, the phototransistor becomes conductive and the supply voltage is connected to ground. The input of Schmitt trigger IC14 is therefore low. Open LEDs will not change the state of the optocouplers. In addition, shorts in the LEDs are not expected during LHC operation since no current is flowing through the LEDs. Synchronous Beam Dumps are only caused if there is a short in the sensor of channel 1 (pins 15 and 16) of IC13 or IC17. The supply voltage P3V3 will be connected to ground (see Figure 5.41) via the optocoupler sensor. The LBDS PLC will request a beam dump since incoming and outgoing signals are not the same.

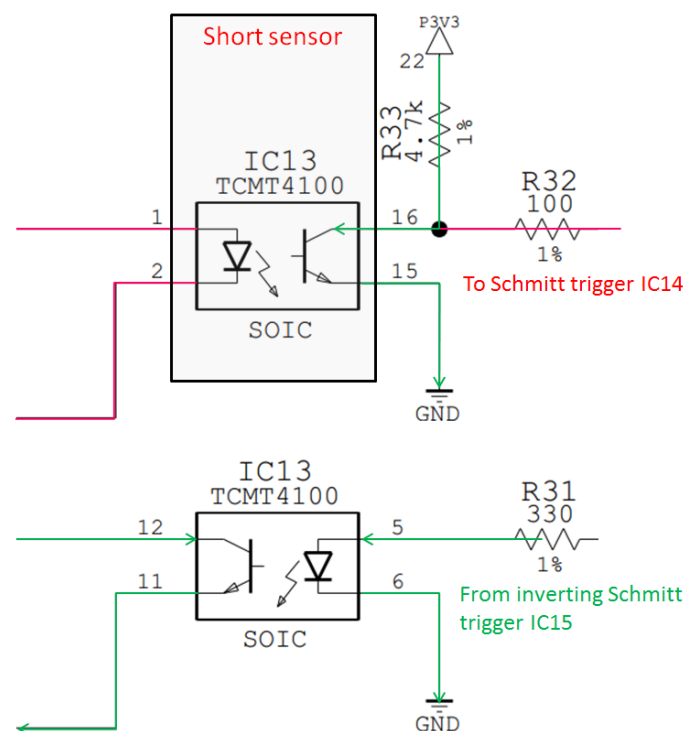


Figure 5.41: Excerpt of the CIBDS circuit layout around IC13, LBDS not in Local Mode. IC13 behaviour in case of a short between pin 15 and pin 16 in channel 1. Red arrows represent the logic state FALSE, green arrows the logic state TRUE.

The failure rate data from VISHAY does not state if it applies for one channel or all channels of the TCMT4100. Therefore, it was decided to apply 4 FIT to each channel split to 2 FIT for the sensor and the LED. The calculated failure rate 67.62 FIT considers both channels and is

also split evenly to the sensors and LEDs. Table 5.39 lists the failures in the optocoupler which will cause a Synchronous Beam Dump.

Table 5.39: Optocoupler failures in CIBDS causing Synchronous Beam Dumps.

IC13, IC17		
Failure Mode Description	$\lambda_{\text{MIL-HDBK}}$ [FIT]	$\lambda_{\text{Manufacturer}}$ [FIT]
Short Sensor IC13 channel 1	8.45	1.00
Short Sensor IC17 channel 1	8.45	1.00

In case of open resistors R32 or R33 (R38 or R39 for redundant path), the Schmitt trigger IC14 (IC19) will be disconnected from power supply P3V3. This can also cause a Synchronous Beam Dump via the LBDS PLC. However, their failure rate is negligible (less than 0.001 FIT) due to their low power stress ratio (rated power divided by operating power). All other components involved in the CIBDS trigger masking are not used if the LBDS is not in local mode. They can therefore not cause beam dumps.

The summed failure rate to cause Synchronous Beam Dumps in the part of the CIBDS used to mask beam dump triggers if the LBDS is in Local Mode, using MIL-HDBK-217F is

$$\lambda_{\text{SBD_CIBDS_LOCAL_MIL}} = \mathbf{162.66 \text{ FIT.}} \quad (5.44)$$

With data provided by the manufacturers the failure rate becomes

$$\lambda_{\text{SBD_CIBDS_LOCAL_MAN}} = \mathbf{23.82 \text{ FIT.}} \quad (5.45)$$

Failures requiring maintenance

The failures leading to a Synchronous Beam Dump can also cause maintenance work if the CIBDS has to be replaced after the caused beam dump. Considering, that shorts and the failure mode ‘improper output’ is spurious but the failure modes ‘no output’ is permanent, only the permanent failure modes will cause maintenance work. This failure mode only appears in Schmitt trigger IC14 and IC18 (see Table 5.40).

Table 5.40: Single Schmitt trigger buffer failures in CIBDS causing Synchronous Beam Dumps and maintenance work.

IC14, IC18		
Failure Mode Description	$\lambda_{\text{MIL-HDBK}}$ [FIT]	$\lambda_{\text{Manufacturer}}$ [FIT]
No Output IC14	5.46	0.18
No Output IC18	5.46	0.18

5.3.4 CIBDS summary

Similar to the TDU250, the CIBDS can cause Asynchronous and Synchronous Beam Dumps in case of component failures. Four components contribute to the failure mode Asynchronous Beam Dump. All of them are in the part of the CIBDS which creates the trigger for the TDU250. The failure rates for an Asynchronous Beam Dump are summed in Equation (5.46) for exclusively calculated failure rates and in Equation (5.47) including the data from the manufacturers:

$$\lambda_{ABD_CIBDS_MIL} = \mathbf{10.62 \text{ FIT}}. \quad (5.46)$$

$$\lambda_{ABD_CIBDS_MAN} = \mathbf{2.20 \text{ FIT}}. \quad (5.47)$$

The share of the different components in the failure mode Asynchronous Beam Dump is displayed in Figure 5.42 (left: calculated with MIL-HDBK-217F, right: manufacturer data). Due to the strongly different failure rates of the MOSFET drivers IC4 and IC5 when comparing the calculated failure rates to the provided manufacturer data, the share of the resistors R17 and R18 rises from 6 % (MIL-HDBK-217F) to 32 % (manufacturer data included).

The *MTTF* for Asynchronous Beam Dumps is 10749 years (MIL-HDKB-217F) and 51889 years respectively (manufacturer data).

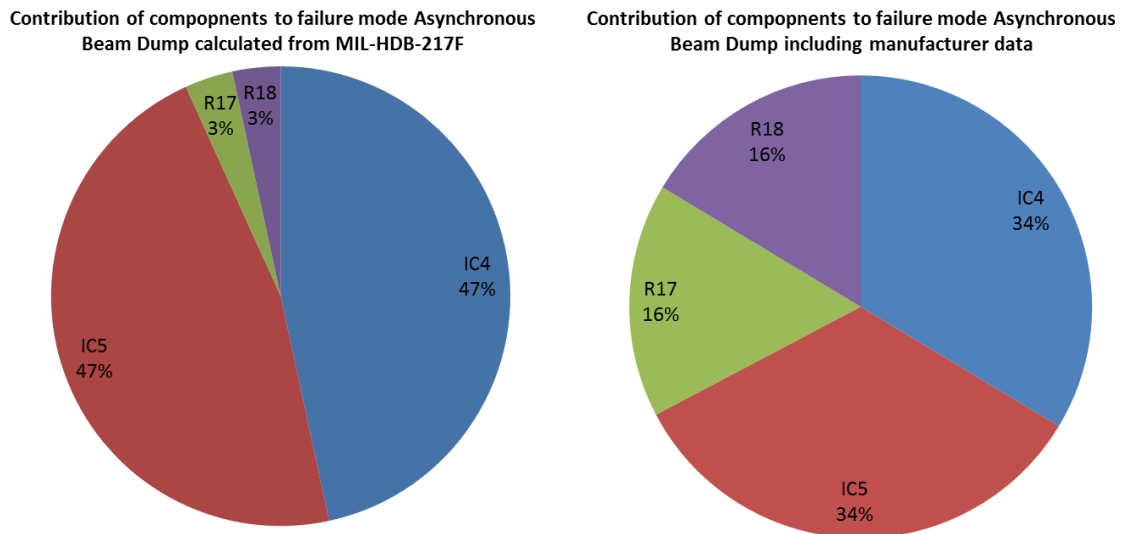


Figure 5.42: Share of the different components in the CIBDS in the failure mode Asynchronous Beam Dump. Left: failure rates calculated from MIL-HDBK-217F. Right: failure rates complemented with data from manufacturers (IC4, IC5).

Three times more components can induce Synchronous Beam Dumps. Table 5.41 lists the components which contribute to this failure mode and their failure effects.

Table 5.41: Summary of all components in the CIBDS whose failure modes can cause Synchronous Beam Dumps.

Component	$\lambda_{\text{MIL-HDBK}}$ [FIT]	$\lambda_{\text{Manufacturer}}$ [FIT]
IC1	5.74	1.1
IC2	5.74	1.1
IC4	6.43	0.96
IC5	6.43	0.96
IC13	8.45	1
IC17	8.45	1
IC15	11.56	5.01
IC19	11.56	5.01
IC18	23.74	0.8
IC14	23.74	0
IC16	37.58	5.1
IC20	37.58	5.1

The sum of the failure rates in Table 5.41 results in the total failure rate for the CIBDS to cause Synchronous Beam Dumps for the calculated failure rates

$$\lambda_{SBD_CIBDS_MIL} = \mathbf{187.00\ FIT}, \quad (5.48)$$

and with the data from the manufacturers

$$\lambda_{SBD_CIBDS_MAN} = \mathbf{27.94\ FIT}. \quad (5.49)$$

Figure 5.43 depicts the share of different components in the total failure rate. The left chart is based on calculated failure rates from MIL-HDBK-217F. Most Synchronous Beam Dumps are hereby caused due to failures in AND gates IC16 and IC20 (each 20 %) followed by the Schmitt trigger IC14 and IC18 (each 13 %).

Taking into account data from the manufacturers, the influence of IC14 and IC18 declines significantly (each 3 %) while the share of inverting Schmitt triggers IC15 and IC19 are equally contributing to Synchronous Beam Dumps as the Schmitt triggers IC16 and IC20 (each 18 %).

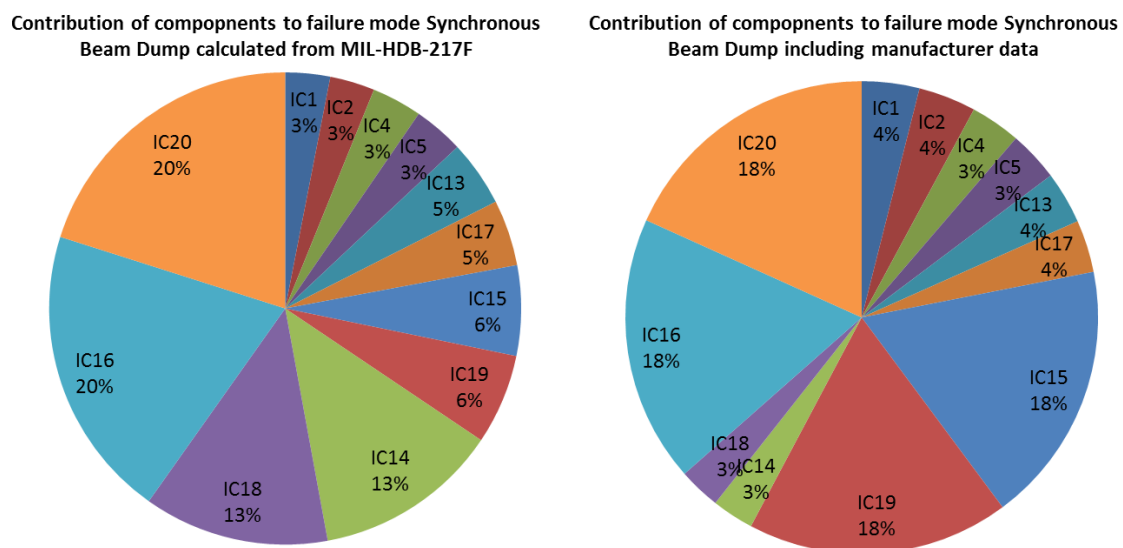


Figure 5.43: Share of different components in the CIBDS in the failure mode Synchronous Beam Dump. Left: failure rates calculated from MIL-HDBK-217F. Right: failure rates complemented with data from manufacturers (if available).

Figure 5.44 shows the probability over time of a Synchronous Beam Dump (blue) and an Asynchronous Beam Dump (red) caused by the CIBDS. Dashed lines show data based on calculations, solid lines show manufacturer data.

With a probability of 10 % a Synchronous Beam Dumps can be expected in the period of 64 years (MIL-HDBK-217F) or 430 years (manufacturer data). During 10 years of operation, 2×10^{-3} (manufacturer data) or 16×10^{-3} respectively (MIL-HDBK-217F) Synchronous Beam Dumps caused by one CIBDS can be expected.

The probability for Asynchronous Beam Dumps caused by the CIBDS is considerably lower compared to the TDU250. In the time period of 100 years the probability for an Asynchronous Beam Dump caused by the CIBDS is lower than 1 %. Within ten years of operation of the LHC the expected total amount of Asynchronous Beam Dumps caused by one CIBDS is 2×10^{-4} (manufacturer data) and 9×10^{-4} respectively (MIL-HDBK-217F).

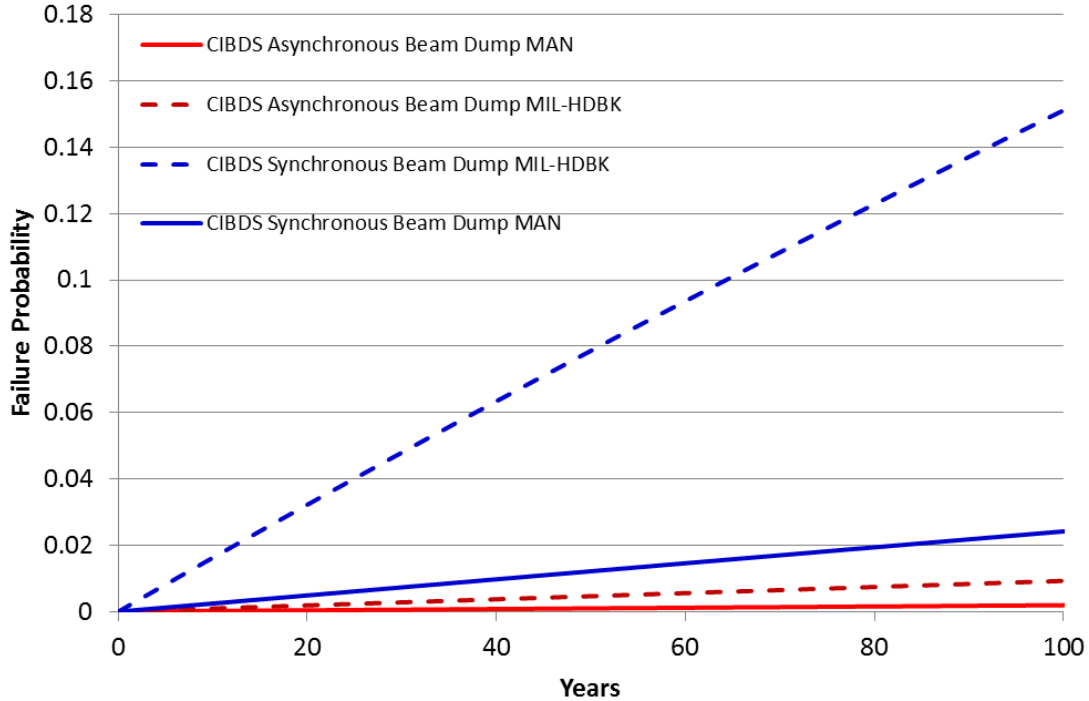


Figure 5.44: Failure probability over time for Asynchronous – and Synchronous Beam Dumps in the CIBDS calculated from MIL-HDBK-217F (dashed line) and including manufacturer data (solid line).

The summed failure rate for required maintenance includes failures in the trigger creation part, the part to receive the beam permit flag and the trigger masking part of the CIBDS. These failures will require the replacement of the faulty CIBDS before the LHC can be re-armed. Note, failure modes of the components requiring maintenance can also induce beam dumps. The failure rate for data calculated with MIL-HDBK-217F is

$$\lambda_{MNTNC_CIBDS_MIL} = \sum \lambda_{MNTNC_i_MIL} = \mathbf{82.22 \text{ FIT.}} \quad (5.50)$$

Taking into account the data from manufacturers, the failure rate becomes

$$\lambda_{MNTNC_CIBDS_MAN} = \sum \lambda_{MNTNC_i_MAN} = \mathbf{24.46 \text{ FIT.}} \quad (5.51)$$

2×10^{-3} (Manufacturer), respectively 7×10^{-3} (MIL-HDBK-217F) failures are expected within ten years of LHC operation which will cause maintenance work.

Table 5.42 summarizes the *MTTFs* for the three discussed failure modes caused by the CIBDS.

Table 5.42: *MTTFs* for Asynchronous Beam Dumps, Synchronous Beam Dumps and Maintenance in the CIBDS.

	MTTF [years] MIL-HDBK-217F	MTTF [years] Manufacturer Data
Asynchronous Beam Dumps	10749	51889
Synchronous Beam Dumps	610	4086
Maintenance	1388	4667

5.4 System Implementation

For the final system implementation, two CIBDS will be used, one for each beam. Figure 5.45 depicts the system implementation of the new link from the BIS to the Re-triggering Lines. In case of a dump request, each CIBDS will forward the trigger to two TDU250s. Each TDU250 is connected to one Re-triggering Line.

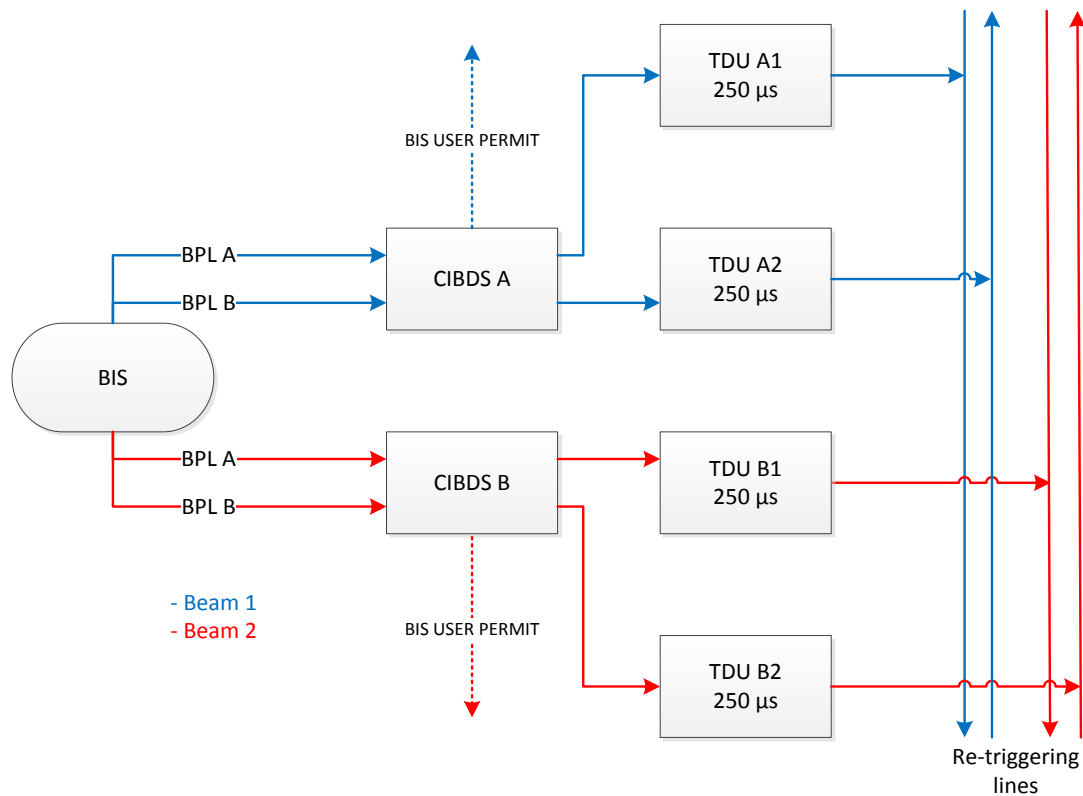


Figure 5.45: System implementation CIBDS and TDU.

The impact on Synchronous and Asynchronous Beam Dumps of the system implementation is discussed in the following chapters.

5.4.1 Connectors of the CIBDS and the TDU250

The CIBDS and the TDU250 are connected via various connectors and cables within the system implementation.

Figure 5.46 shows the front panel of a CIBDS.

- Four optical cables are connected as a part of the redundant BIS Beam permit loops A and B (PERMIT LOOP A and PERMIT LOOP B, blue).
- Two connectors (LM3 and LM4) are used to receive the redundant LBDS Local Mode signal and send it back to the PLC (LBDS LOCAL MODE, red).
- The trigger for both TDU250s passes by connector LM5 (PULSE TO DELAY BOX, green).

- One output connector (LM6) is used for the BIS User Permit for the CIBU (PERMIT TO CIBU, orange).
- The connectors LOCAL PERMIT and TIMING are outputs for monitoring of the CIBDS and not used during LHC operation.

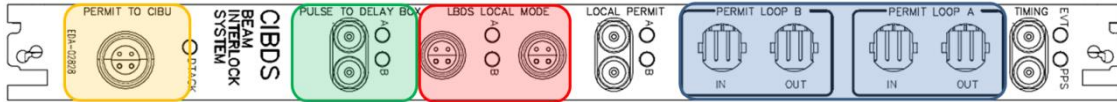


Figure 5.46: CIBDS front panel arrangement.

The optical connectors for the permit loops do not transmit electrical power. Failure modes of these connectors are only related to mechanical anomalies. Therefore they will not be considered. The connectors LM3 and LM4 of the CIBDS are inactive during operation with beam, thus failures in these connectors will not cause beam dumps.

A faulty connector LM6 will revoke the permit to the CIBU and trigger a Synchronous Beam Dump. The calculated failure rate is 5.19 FIT (MIL-HDBK-217F).

The output and input connections of the TDU250 are monitored via the TDU interlock circuit. Disconnecting the cables will cause a Synchronous Beam Dump. Faulty connectors on both sides, the two CIBDS' and the four TDU250s, can cause additional Synchronous Beam Dumps. In total eight connectors are used between the CIBDS' and the TDU250s. Each of the eight connectors exhibits a calculated failure rate of 2.13 FIT (MIL-HDBK-217F).

A 32 contacts right angle male connector (J1) is used to connect the TDU250 to the Re-triggering Lines. The calculated failure rate is 9.01 FIT (MIL-HDBK-217F). In case of a failure in this connector, the TDU250 interlock circuit will send an error signal and therefore trigger a Synchronous Beam Dump.

The total failure rate calculated from MIL-HDBK.217F for four TDU250s and two CIBDS' is

$$\lambda_{SBD_Connectors} = (2 \cdot 5.19 + 8 \cdot 2.13 + 4 \cdot 9.01) \text{ FIT} = \mathbf{63.46 \text{ FIT}}. \quad (5.52)$$

The manufacturers do not serve reliability data for the connectors in use.

5.4.2 Asynchronous Beam Dumps

Two CIBDS and four TDU250 will contribute to the overall failure rate for Asynchronous Beam Dumps. Figure 5.47 shows the Fault Tree for Asynchronous Beam Dumps

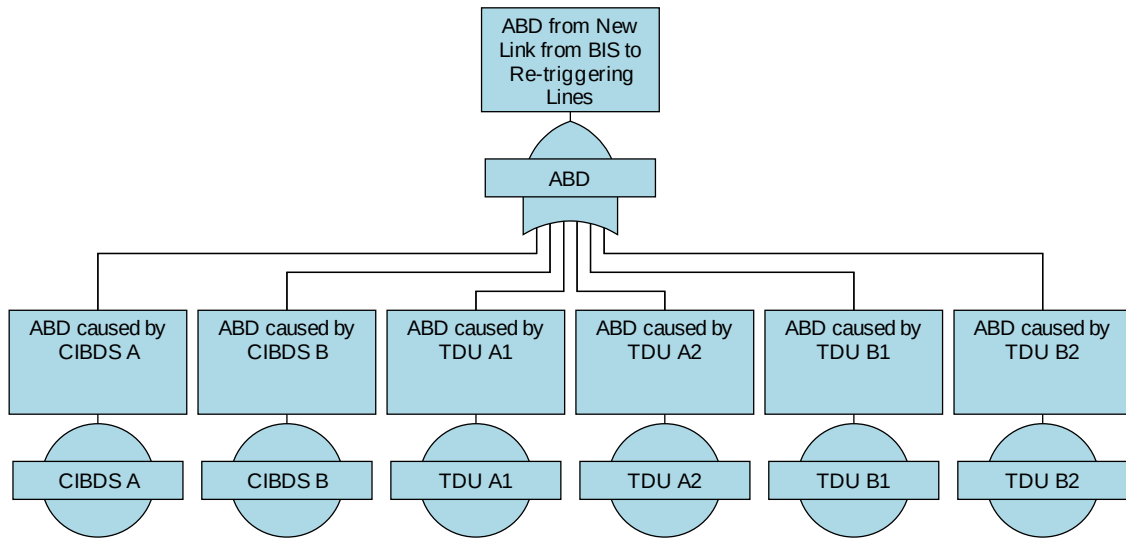


Figure 5.47: Asynchronous Beam Dump Fault Tree for system implementation.

From the Fault Tree for Asynchronous Beam Dumps, Equation (5.53) and Equation (5.54) can be derived. The failure rate for the system calculated from MIL-HDBK-217F is

$$\lambda_{ABD_System_MIL} = 4\lambda_{ABD_TDU_MIL} + 2\lambda_{ABD_CIBDS_MIL} = \mathbf{268.20 FIT}. \quad (5.53)$$

Taking into account the data provided from the manufacturers the failure rate becomes

$$\lambda_{ABD_System_MAN} = 4\lambda_{ABD_TDU_MAN} + 2\lambda_{ABD_CIBDS_MAN} = \mathbf{224.68 FIT}. \quad (5.54)$$

The *MTTF* for Asynchronous Beam Dumps for the system is therefore 426 years calculated from MIL-HDBK-217F and respectively 508 years considering the manufacturer data.

Figure 5.48 (MIL-HDBK-217F) and Figure 5.49 (manufacturer data) show the probability over time for an Asynchronous Beam Dump for the system installation (dark blue). The TDU250s contribute the most to this failure mode (violet: one TDU, light blue: all TDU250s). The contribution to this failure mode of one CIBDS is shown in red and for both CIBDS in green.

Asynchronous Beam Dumps are expected with a probability of 10 % within 45 years or 54 years respectively. In ten years of operation 23.5×10^{-3} (MIL-HDBK-217F) or 19.7×10^{-3} (manufacturer data) can be expected.

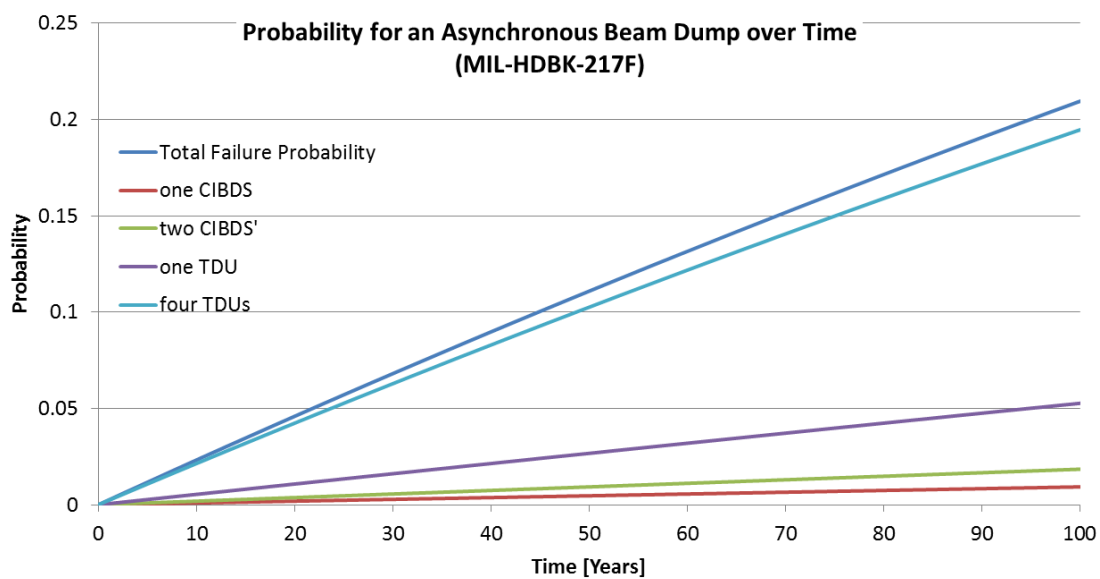


Figure 5.48: Probability for an Asynchronous Beam Dump over time (MIL-HDBK-217F).

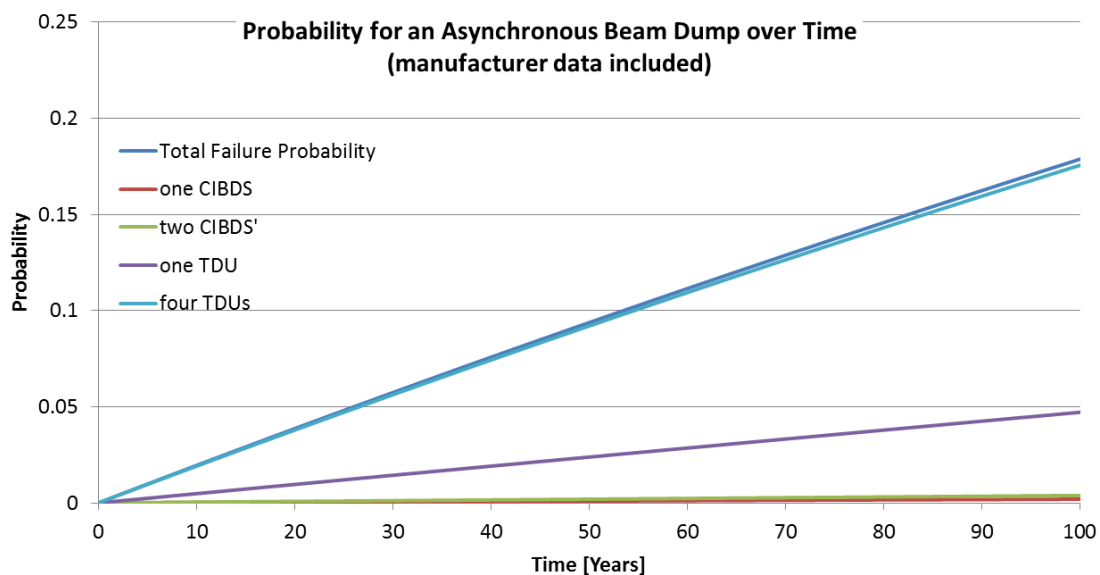


Figure 5.49: Probability for an Asynchronous Beam Dump over time (manufacturer data included).

5.4.3 Synchronous Beam Dumps

The Fault Tree for Synchronous Beam Dumps is similar to the previous Fault Tree. Each CIBDS and TDU250 can cause a Synchronous Beam Dump.

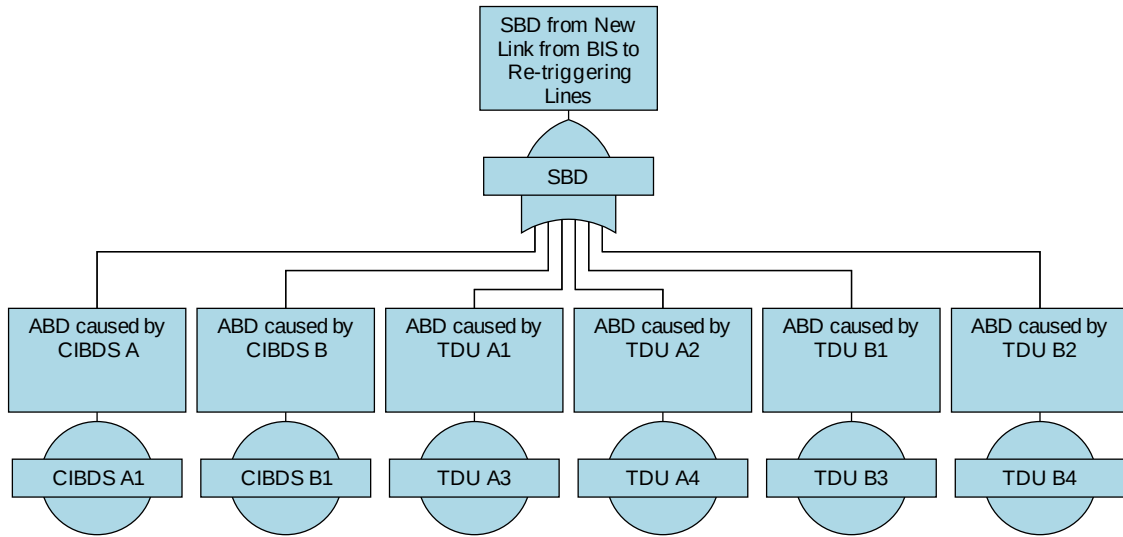


Figure 5.50: Synchronous Beam Dump Fault Tree for system implementation.

Including the failures from the connectors, this leads to a total failure rate of

$$\begin{aligned}\lambda_{SBD_System_MIL} &= 4\lambda_{SBD_TDU_MIL} + 2\lambda_{SBD_CIBDS_MIL} + \lambda_{SBD_Connectors} \\ &= \mathbf{1080.66\ FIT}\end{aligned}\quad (5.55)$$

for the system installation for calculated failure rates from MIL-HDBK-217F and

$$\begin{aligned}\lambda_{SBD_System_MAN} &= 4\lambda_{SBD_TDU_MAN} + 2\lambda_{SBD_CIBDS_MAN} + \lambda_{SBD_Connectors} \\ &= \mathbf{621.94\ FIT}\end{aligned}\quad (5.56)$$

considering the manufacturer data.

The *MTTF* for Synchronous Beam Dumps for the system is calculated to 106 years from MIL-HDBK-217F and respectively 184 years considering the manufacturer data.

Figure 5.51 (MIL-HDBK-217F) and Figure 5.52 (manufacturer data) show the probability over time for a Synchronous Beam Dump. The dark blue line depicts the total failure probability. Similar to Asynchronous Beam Dumps, the four TDU250s (light blue) contribute the most to this failure mode although a single CIBDS (red) is contributing more than one TDU250 (violet). The contribution to this failure mode of two CIBDS is shown in green.

Synchronous Beam Dumps are expected with a probability of 10 % within 11 years or 19 years respectively. In ten years of operation 94.6×10^{-3} (MIL-HDBK-217F) or 54.5×10^{-3} (manufacturer data) Synchronous Beam Dumps can be expected.

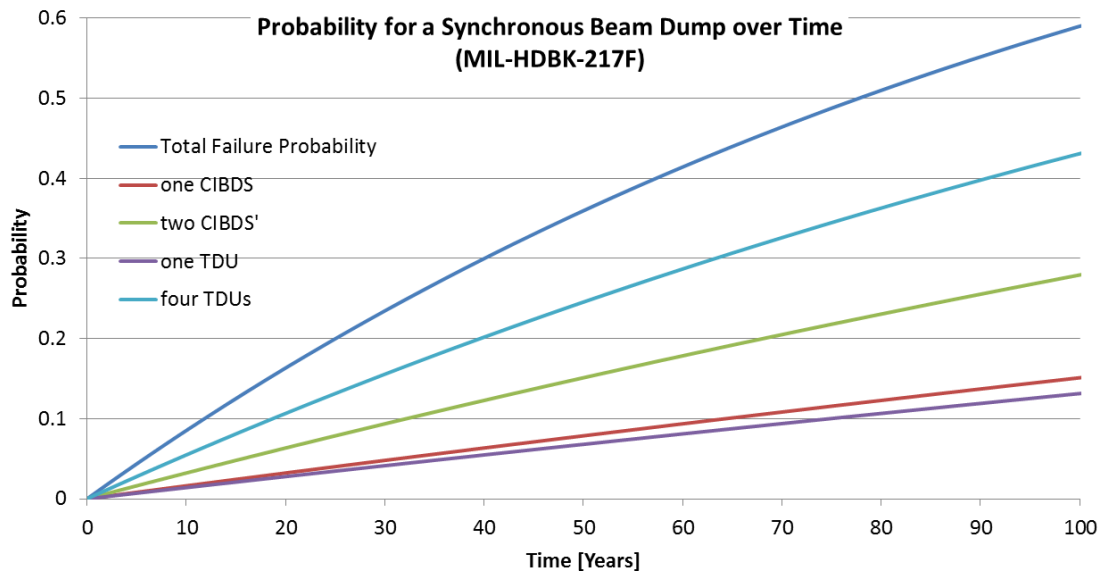


Figure 5.51: Probability for a Synchronous Beam Dump over time (MIL-HDBK-217F).

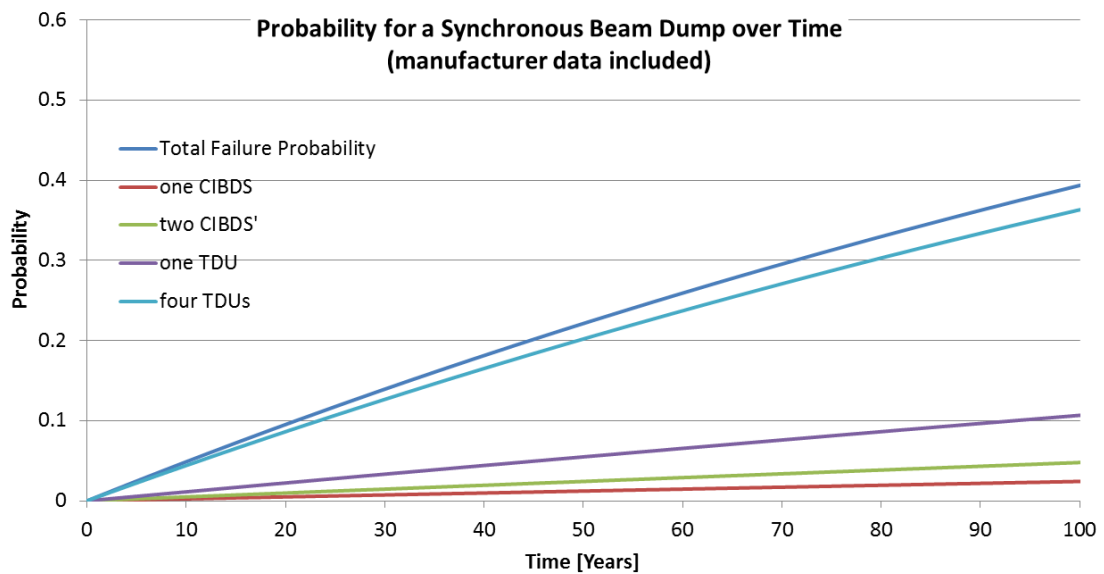


Figure 5.52: Probability for a Synchronous Beam Dump over time (manufacturer data included).

6 Conclusions and Outlook

The new link from the Beam Interlock System to the LHC Beam Dumping System is not only important for improving the safety of the LHC, but it will also influence its availability for physics operation in case of failures in the four TDU250s or the two CIBDS. The reliability analysis has been carried out to calculate the effect of this new safety system on additional beam dumps.

The results show that we can be confident to enhance the protection of the LHC with the new system without compromising the availability. The previously defined limits of one additional Asynchronous Beam Dump in ten years and two additional Synchronous Beam Dumps per year were exceeded by several orders of magnitude. The prediction shows, that in ten years of operation 23.5×10^{-3} (MIL-HDBK-217F) or 19.7×10^{-3} (manufacturer data) Asynchronous Beam Dumps can be expected from the combined installation of the CIBDS' and TDU250s. Only 9.46×10^{-3} (MIL-HDBK-217F) or 5.45×10^{-3} (manufacturer data) Synchronous Beam dumps can be expected per year. The *MTTFs* for both failure modes surpass the expected lifetime of the LHC by far.

While Trigger Delay Units are already used as a part of the LBDS and proved to be very dependable during LHC operation, the CIBDS was built from scratch and the design was adjusted in an iterative process in order to further improve its reliability. A second path for the LBDS local mode was added during the development phase to prevent a single point of failure, which could have led to a blind CIBDS. Moreover the functionality to open the BIS loop was added to reduce the probability of spurious Asynchronous Beam Dumps.

Two CIBDS prototypes were built and are being tested in the lab to further validate the functionality. Meanwhile the new TDU250s are being built. The next goal for the system will be the LHC reliability run without a beam in mid-2014. In this phase, beam dumps are triggered frequently to examine the behavior of the updated LBDS and the new link from the BIS to the LBDS. Additionally the accurate performance of the CIBDS in the LHC arming process will be checked.

The system will be fully implemented and operational for the LHC start-up with beam after Long Shutdown 1 in 2015 and protect the LHC in the very unlikely failure scenario of a blind LBDS against the incapability to dump the beams.

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8 Appendix

8.1 Component failure modes and distribution

Table 8.1: Component failure modes and distribution [MIL-HDBK-338B]

Component type	Failure mode	Failure distribution [%]
Capacitor, Aluminium Electrolytic	Short	53
	Open	35
	Electrolyte leak	10
	Decrease in capacitance	2
Capacitor, Plastic	Open	42
	Short	40
	Change in value	18
Capacitor, Tantalum, Electrolytic	Short	57
	Open	17
	Change in value	14
Coil	Short	42
	Open	42
	Change in value	16
Connector	Open	61
	Poor Contact	23
	Short	16
Diode, general	Short	49
	Open	31
	Parameter change	15
Diode, small signal	Parameter change	58
	Open	24
	Short	18
Diode, Zener, Voltage Regulator	Open	45
	Parameter change	35
	Short	20
Relay	Fails to trip	55
	Spurious trip	26
	Short	19
Resistor, Film	Open	59
	Parameter change	36
	Short	5

Component type	Failure mode	Failure distribution [%]
Transformer	Open	42
	Short	42
	Parameter change	16
Transistor, Bipolar	Short	73
	Open	27
Transistor, FET	Short	51
	Output Low	22
	Parameter Change	17
	Open	5
	Output high	5

8.2 Components in the Trigger Delay Unit 250

Table 8.2: Components in the TDU250 which contribute to LHC failure modes

Component	Description	Failure Rate [FIT]	
		MIL-HDBK-217F	Manufacturer
C11	WIMA MKS2 Polyester Capacitor	12.81	2
C13	WIMA FKS2 Polyester Capacitor	9.71	5
C15	WIMA FKS2 Polyester Capacitor	10.67	5
C18	WIMA FKS2 Polyester Capacitor	9.93	5
C19	WIMA FKS2 Polyester Capacitor	10.67	5
C20	WIMA MKS2 Polyester Capacitor	11.13	2
C7	WIMA FKS2 Polyester Capacitor	9.25	2
C8	VISHAY Polyester Capacitor	20.94	2
CL	WIMA FKS2 Polyester Capacitor	12.71	5
D1	PHILIPS 2A 20V Ultra-Fast Low-Loss Controlled Avalanche Rectifier	11.85	n.a.
D10	Small Signal Diode	15.84	n.a.
D11	Small Signal Diode	16.03	n.a.
D8	Small Signal Diode	13.01	n.a.
D9	Small Signal Diode	9.42	n.a.
IC1	NXP Quad 2-Input NAND SCHMITT Trigger	29.40	2.99
J1	32 Contacts Right Angle Male Connector Type D for Daughter Card	9.01	n.a.
L1	RM10 Core + 12 Pins Coil Former + Clamps	2.16	n.a.
R1	0.6W $\pm$ 1% Metal-Film Resistor	12.37	n.a.
R11	0.6W $\pm$ 1% Metal-Film Resistor	7.49	n.a.
R15	0.6W $\pm$ 1% Metal-Film Resistor	12.37	n.a.
R16	0.6W $\pm$ 1% Metal-Film Resistor	12.37	n.a.
R19	1W $\pm$ 5% Power Metal Film Resistor	6.73	n.a.
R2	1W $\pm$ 5% Power Metal Film Resistor	15.09	n.a.
R20	$\pm$ 5% 0.50W 3500VDC High-Voltage Resistor	0.18	n.a.
R21	$\pm$ 5% 0.50W 3500VDC High-Voltage Resistor	0.18	n.a.
R22	$\pm$ 5% 0.50W 3500VDC High-Voltage Resistor	0.18	n.a.
R23	$\pm$ 5% 0.50W 3500VDC High-Voltage Resistor	0.18	n.a.
R28	0.6W $\pm$ 1% Metal-Film Resistor	6.90	n.a.
R29	0.6W $\pm$ 1% Metal-Film Resistor	2.40	n.a.

Component	Description	Failure Rate [FIT]	
		MIL-HDBK-217F	Manufacturer
R3	0.6W $\pm$ 1% Metal-Film Resistor	2.49	n.a.
R30	0.6W $\pm$ 1% Metal-Film Resistor	1.37	n.a.
R31	0.6W $\pm$ 1% Metal-Film Resistor	2.83	n.a.
R32	0.6W $\pm$ 1% Metal-Film Resistor	2.83	n.a.
R33	0.6W $\pm$ 1% Metal-Film Resistor	1.10	n.a.
R34	0.6W $\pm$ 1% Metal-Film Resistor	1.37	n.a.
R36	0.6W $\pm$ 1% Metal-Film Resistor	2.20	n.a.
R37	0.6W $\pm$ 1% Metal-Film Resistor	3.80	n.a.
R39	0.6W $\pm$ 1% Metal-Film Resistor	2.10	n.a.
R4	0.6W $\pm$ 1% Metal-Film Resistor	12.37	n.a.
R40	0.6W $\pm$ 1% Metal-Film Resistor	3.88	n.a.
R43	0.6W $\pm$ 1% Metal-Film Resistor	4.56	n.a.
R6	0.6W $\pm$ 1% Metal-Film Resistor	4.99	n.a.
R7	0.6W $\pm$ 1% Metal-Film Resistor	12.37	n.a.
RL2	24V 2a 2 Pole (2 Form C / DPDT) Telecom MT2 Relay	165.3	n.a.
T1	IRFF130 100V 8A 0.18R Repetitive Avalanche and dv/dt Rated HEXFET Transistor REF: MIL-PRF-19500/557	86.88	n.a.
T2	MICROSEMI Silicon Controlled Rectifier	41.97	n.a.
T4	PNP Switching Silicon Transistor	1.20	n.a.
T5	PNP Switching Silicon Transistor	1.20	n.a.
T8	NPN Switching Silicon Transistor	1.14	n.a.
T9	NPN Switching Silicon Transistor	1.14	n.a.
TR1	Vacuumschmelze Trigger Transformer	120.9	n.a.

8.3 Components in the CIBDS

Table 8.3: Components in the CIBDS which contribute to LHC failure modes

Component	Description	Failure Rate [FIT]	
		MIL-HDBK-217F	Manufacturer
C7	50V 10% SMD X7R Ceramic Capacitor	30.05	n.a.
C8	50V 10% SMD X7R Ceramic Capacitor	30.05	n.a.
IC1	XILINX High Performance CPLD	26.08	5
IC2	XILINX High Performance CPLD	26.08	5
IC4	MAXIM Dual High-Speed 1.5A MOSFET Driver	12.85	1.93
IC5	MAXIM Dual High-Speed 1.5A MOSFET Driver	12.85	1.93
IC13	VISHAY TCMT4100 Quad Channel Optocoupler	67.62	8
IC17	VISHAY TCMT4100 Quad Channel Optocoupler	67.62	8
IC14	TI Single Schmitt-Trigger Buffer	23.74	0.8
IC18	TI Single Schmitt-Trigger Buffer	23.74	0.8
IC15	NXP Hex Schmitt-Trigger Inverter	15.01	6.62
IC19	NXP Hex Schmitt-Trigger Inverter	15.01	6.62
IC16	NXP Quad 2-Input AND Gate	48.81	6.62
IC20	NXP Quad 2-Input AND Gate	48.81	6.62
LM5	50ohm Size 00 Right Angle LEMO Duplex for PCB with Offset from PCB	5.19	n.a.
LM6	8 Female Contacts 50 Ohm Size 1B Right Angle Receptacle with Key	4.26	n.a.
R17	R0805 10K 1% 0.125W 100PPM	7.23	n.a.
R18	R0805 10K 1% 0.125W 100PPM	7.23	n.a.

8.4 Photographs of the TDU and the CIBDS

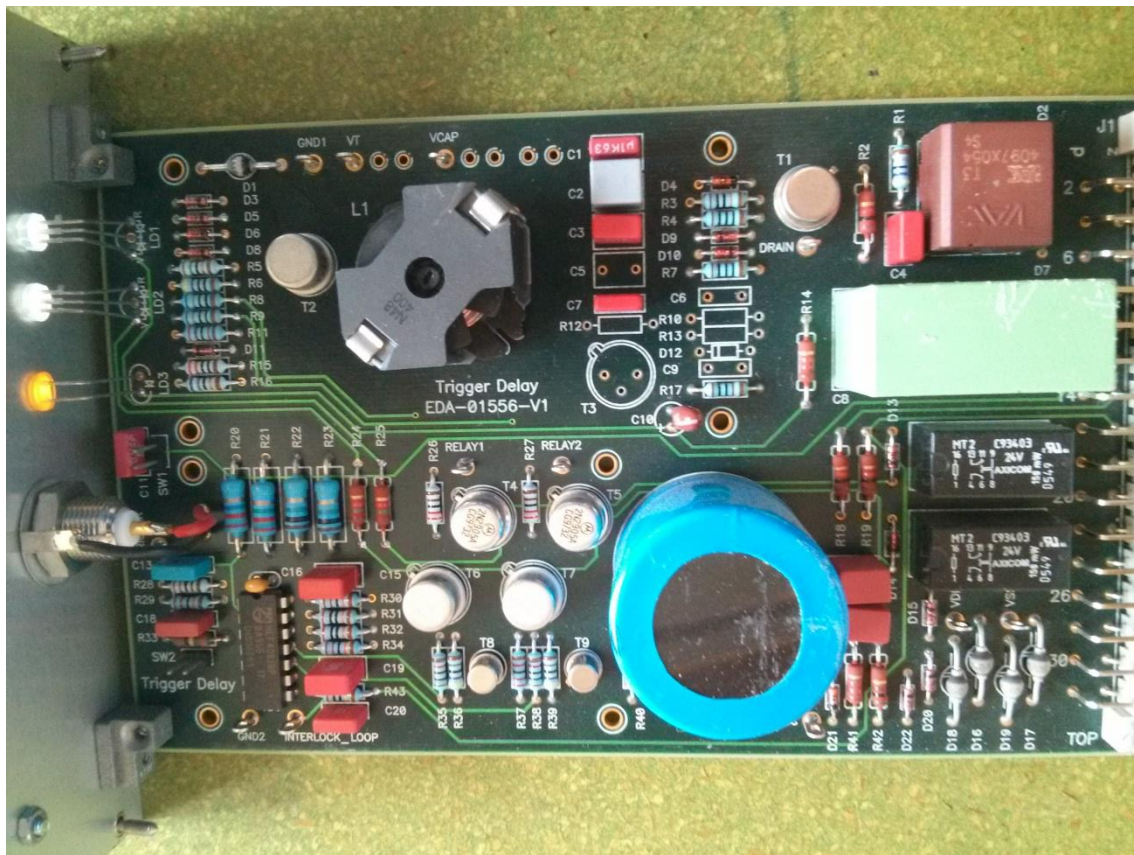


Figure 8.1: Photograph of the Trigger Delay Unit.



Figure 8.2: Photograph of the CIBDS prototype.



Figure 8.3: Photograph of the CIBDS prototype in the testing rack.

8.5 LHC Experiments

Several experiments are distributed at the Large Hadron Collider ring: The four main experiments are ATLAS [30], CMS [31], ALICE [32], LHCb [33] .

For all the experiments the characteristics of the collisions and particles are measured in different ways. If the detector is placed in magnetic fields, the magnetic deflection provides information of electrical charge and momentum of the particle. Furthermore the characteristic tracks of each particle can give insight in mass, velocity and energy. While particles with very high momentum go almost straight through the tracking chambers, low momentum ones go in tight spirals, compare Figure 8.4.

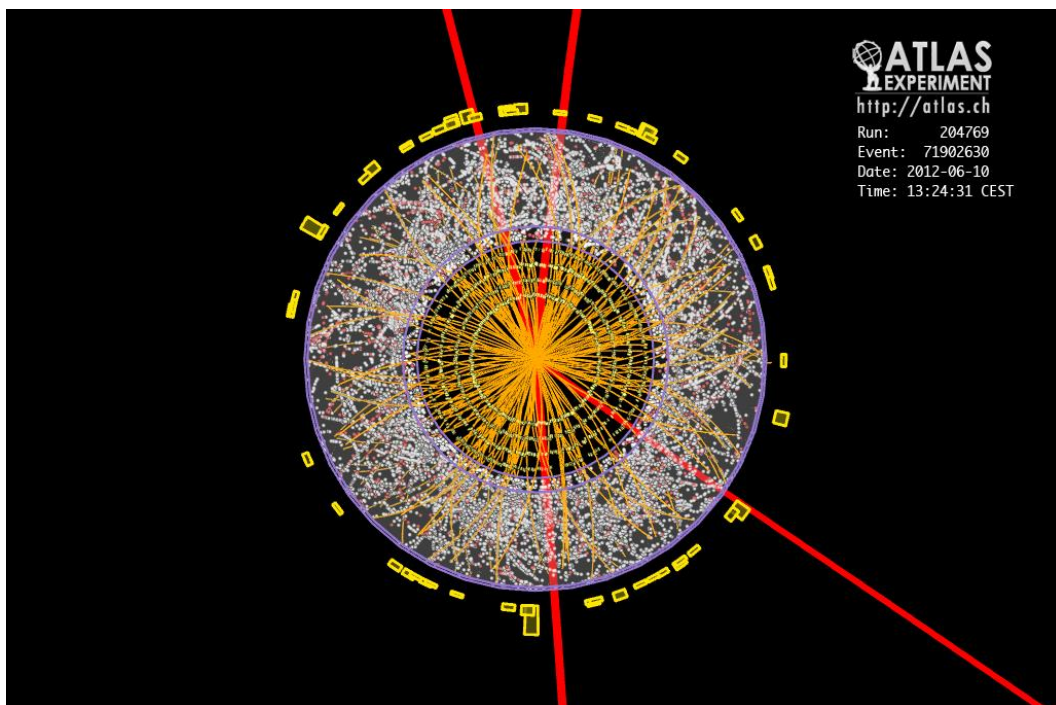


Figure 8.4: An ATLAS Proton-Proton Event where a Higgs Boson decays into four muons (red lines) [1].

With overall 150 million sensors the detectors of the LHC record about 25 million GB of data per year. This chapter should provide a short overview about the four main detectors.

8.5.1 A Toroidal LHC Apparatus (ATLAS)

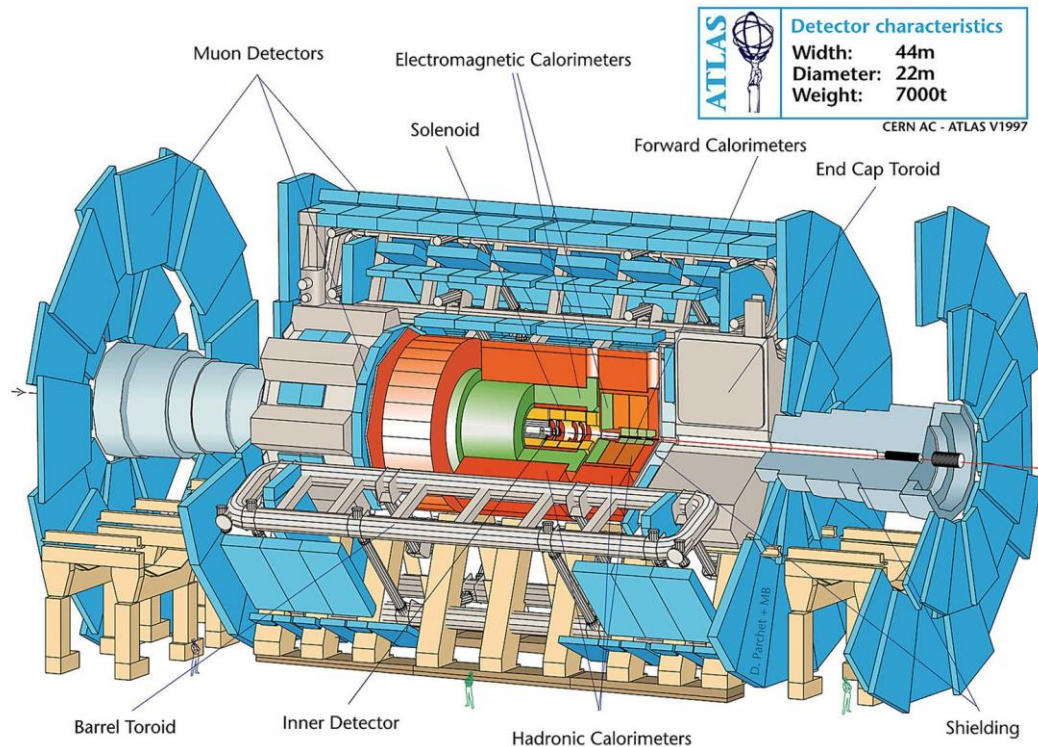


Figure 8.5: ATLAS detector layout [1].

ATLAS is the largest experiment in the LHC located in a cavern 100 m below the surface at Interaction Point 1. It was built for probing a large range of proton and heavy ion collisions, especially the search for the Higgs boson and particles that could make up dark matter. The dimensions of the detector are 25 m in height and 44 m in length. The overall weight of the detector is approximately 7,000 tonnes.

Atlas has an almost cylindrical structure divided into four major parts, see Figure 8.5. The inner detector measures the momentum of charged particles while the calorimeter measures their energy. The muon system identifies and measures the momenta of muons. The magnetic system contains solenoid and toroid magnets to bend the charged particles for the measurements.

Due to the enormous amount of collisions a data processing system is included in the ATLAS experiment. The trigger system selects therefore hundred interesting out of almost one billion collisions per second. These events are channelled and stored by the Data Acquisition System and analysed by the Computing System.

More than three thousand scientists from almost forty countries work on the ATLAS experiment [30] [34].

8.5.2 The Compact Muon Solenoid Experiment (CMS)

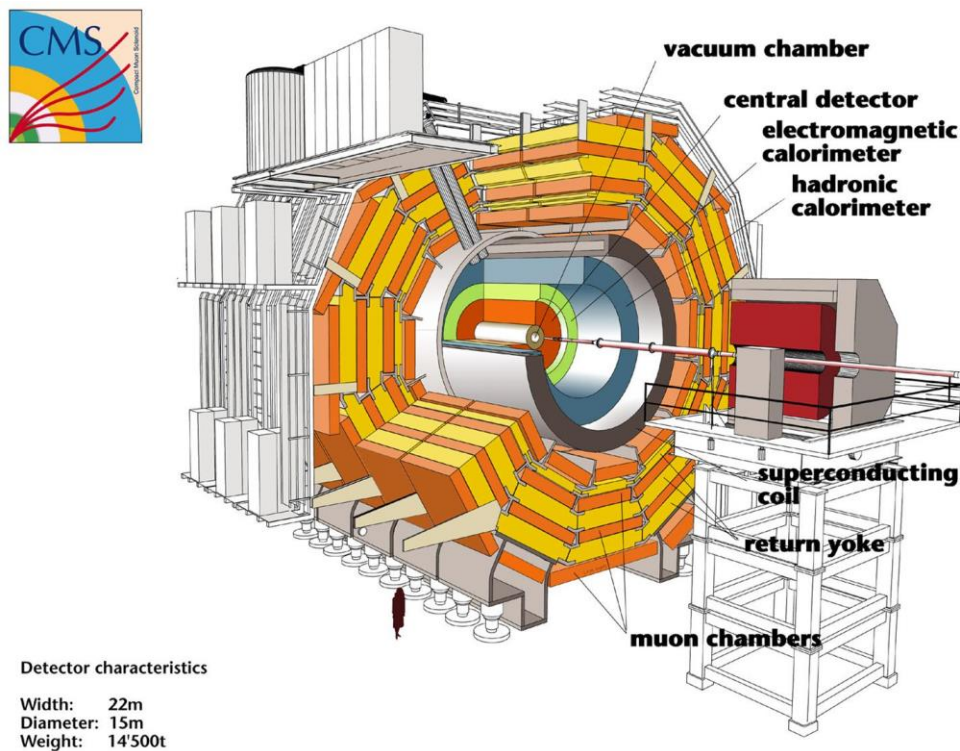


Figure 8.6: CMS detector layout [1].

Besides ATLAS, CMS is the second general-purpose detector to probe proton heavy ion collisions in the LHC complex. A superconducting solenoid is located in the core of CMS, being the biggest magnet that was built in history of mankind. It is surrounded by different layers designed to stop, track or measure different particles. The first step for these particles is a silicon tracker with a resolution of 65 million pixels to chart the position of particles especially short range particles.

In the next layers the electromagnetic and hadronic calorimeters are located, built to measure the energy of photons and electrons and detect particles made up of quarks.

The muon chambers and return yokes are located in the outer part of CMS. The return yokes stop all particles except muons and neutrinos which can be measured in the muon chambers.

Similar to ATLAS, a trigger system is installed to save interesting events.

8.5.3 A Large Ion Collider Experiment (ALICE)

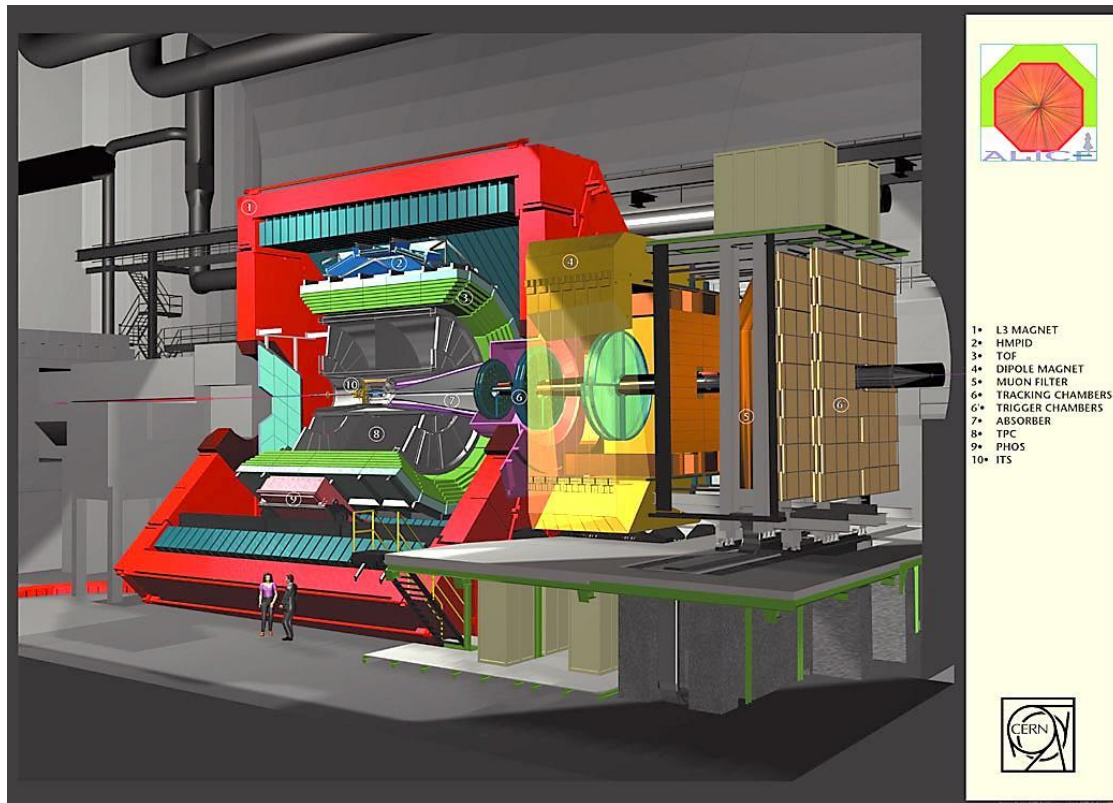


Figure 8.7: ALICE detector layout [1].

The main purpose of the ALICE experiment is to study the collisions of heavy ions in an attempt to produce a new state of matter known as quark-gluon plasma. ALICE will not only collect data at the highest energy densities and temperatures but also with lower energy levels dedicated to proton-nucleus runs.

Several cylindrical detectors (ITS Pixels, ITS Drift, ITS Strips, TPC) measure the passage of particles with electric charge. To recognize the type of particles, other detectors are used to measure the flight time (TOF), the faint light patterns (HMPID) and the radiation (TRD). With this information given, one can differ between electrons, protons, kaons or pions. Muons are discovered by using absorbers to filter other particles. In addition Photon Spectrometers can discover photons sent out during the collisions.

Over 1500 scientists were involved into the development of this 16 m×16 m×26 m big detector. It weighs over ten thousand tonnes and is located in Saint-Genis-Pouilly, France [32], [35].

8.5.4 The Large Hadron Collider beauty experiment (LHCb)

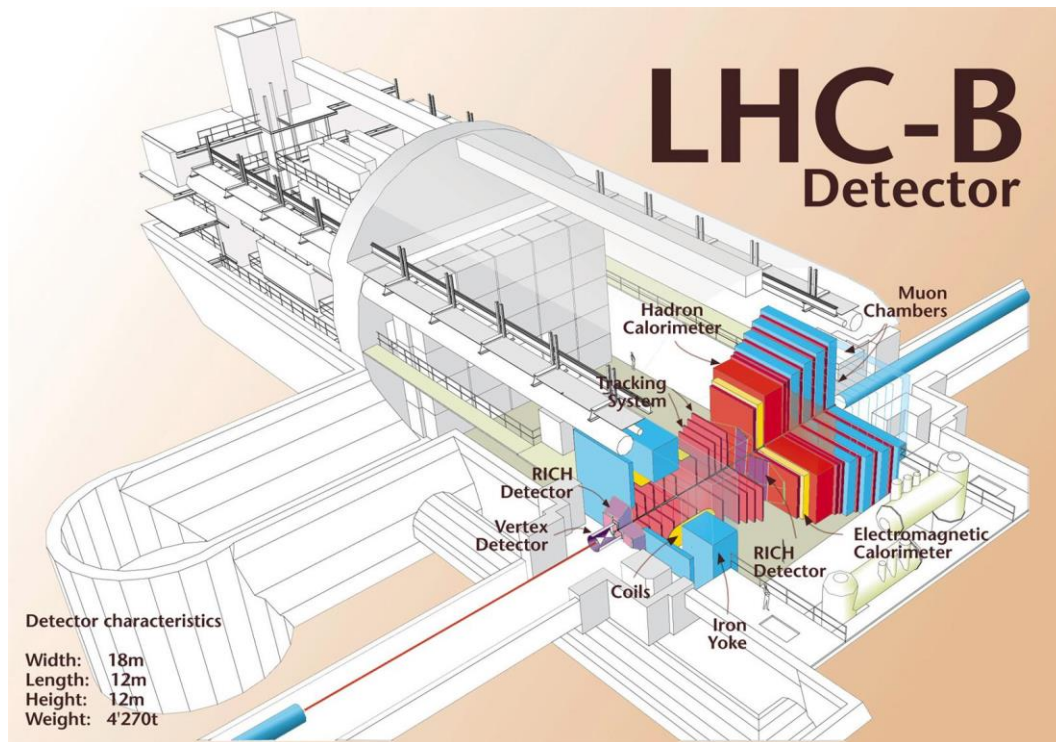


Figure 8.8: LHCb detector layout [1].

Figure 8.7 shows the layout for the LHCb detector. The main purpose of this detector is to study asymmetry between matter and antimatter as well as the parameters of the Charge Parity Violation.

In contrary to the other main experiments, LHCb is the only detector not built in cylindrical layers but rather various sub-detectors placed in a row. The systems are specially designed to filter b-quarks and anti-b-quarks known as B mesons. During beam collisions these B mesons stay close to the beam pipe. The sub-detectors gather information about the identity, trajectory, momentum and energy of each particle generated by a collision. LHCb sub-detectors are VELO, RICH, a silicon tracking system, a Muon system and both electromagnetic and hadronic calorimeters [33], [36].