CMS HGCAL

Train on Track for Particle Detection

Summer Student Report 2023

CMS HGCAL: Train on Track for Particle Detection

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1 Introduction

The High-Granularity Calorimeter (HGCAL) is foreseen to be installed in the Compact Muon Solenoid (CMS) experiment. This is integrated into the pursuit of enhanced performance for the High Luminosity-LHC (HL-LHC) operation. The upgrade involves the replacement of existing calorimeters in the endcaps with a state-of-the-art HGCAL, designed to contend with the notably heightened radiation levels and pileup expected during HL-LHC operation.

The HGCAL will be a 47-layer endcap calorimeter with both electromagnetic (CE-E) and hadronic (CE-H) sections. These sections incorporate Silicon and SiPM(PhotoMultipliers)-on-Tile technology were strategically chosen for the radiation conditions at the upgraded LHC. The absorber layers, essential in both CE-E and CE-H sections, employ a mix of materials, including lead, stainless steel, copper, and copper-tungsten plates, along with stainless steel.

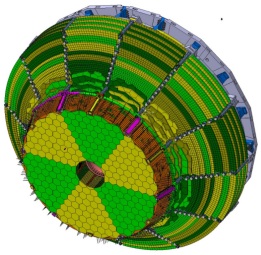

Figure 1: Drawing of HGCAL.

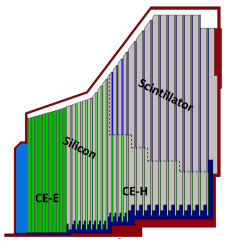

Figure 2: Cross section of HGCAL.

This design also introduces significant benefits for the reconstruction of physics objects, while maintaining the essential resilience to radiation-induced damage. Notably, the high granularity of the detector enables precise particle-flow measurements, extending from the tracker into the calorimeter. This, coupled with its timing capabilities, facilitates the accurate subtraction of energy from pileup events, ensuring excellent energy resolution even in high pileup scenarios. Additionally, the HGCAL's high lateral granularity enhances the identification of narrow jets originating from crucial processes like the vector boson fusion production mode of the Higgs boson, revolutionizing the detection capabilities. Furthermore, the HGCAL demonstrates exceptional capability in electron and photon reconstruction, particularly in forward regions with high pileup conditions. For all the reasons listed above, we can refer to high granularity in 5D.

With these advancements, the HGCAL will play a pivotal role in the upcoming Phase-2 Upgrade, ushering in an era of unprecedented experimental capabilities to meet the challenges posed by the HL-LHC.

1.1 Building blocks

Focusing on CE-E, the third layer of the calorimeter, is composed of 60° cassettes. These cassettes consist of a combination of high-density (HD) and low-density (LD) silicon modules, selected based on

their location within the cassette. A Hex-module, comprising a thermally-conductive CuW baseplate, Kapton^{TM} foil, Si sensor, and Hexaboard PCB (Printed Circuit Boards), is the building block of each layer. The Hexaboard contains multiple HGCAL readout chips (HGCROC) ASIC (Application Specific Integrated Circuit), facilitating on-board signal digitization and subsequent data transfer to the mother-board. Additionally, the Kapton sheet serves the dual purpose of insulating the base plate and providing a bias voltage to the sensor's back side. The baseplate contributes to rigidity and acts as part of the showering material.

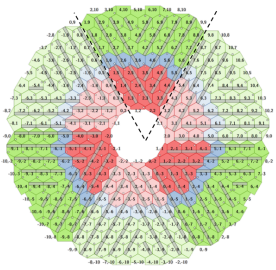

Figure 3: Layer 3.

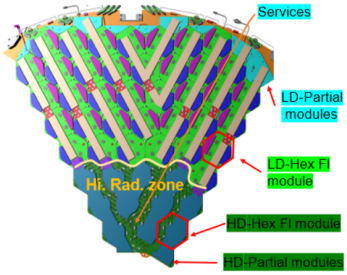

Figure 4: Cassette.

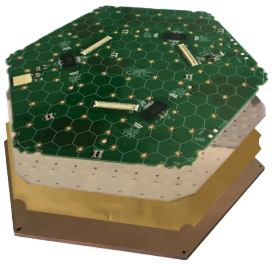

Figure 5: Hex-module.

The silicon section electronics are organised in so-called trains, including engines and wagons. Engines are complex, small, identical, and costly PCBs. Wagons, on the other hand, are simple, large, varied, and inexpensive PCBs. Engines also come in LD and HD varieties, associated with the respective hexaboards. Hexaboards are connected to the engines via a wagon. In the LD region, the hexaboards and wagons are connected via interposers: mezzanine boards, for powering, control, data and trigger-primitive generation, and off-detector transfer. Particular to the system currently being used, the interposer connects to an FPGA that emulates the ECON-D (elink concentrator daq) and the goal is to eliminate the interposer and the ZCU that emulates the ECON-D and just use the ECON-D when it is available. This "train" is the first vertical slice for particle detection.

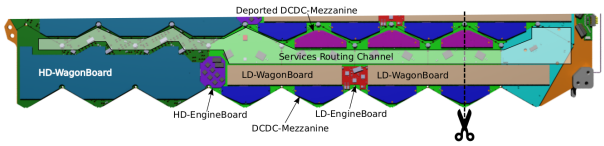

Figure 6: Vertical slice.

The Hexaboard is a complex eight-layer readout PCB equipped with multiple HGCROC ASICs reading the Si diode pads with low noise and large dynamic range. Six HGCROC ASICs are required to read the 432 diode pads on a full-size HD Si sensor, and three on the LD Hexaboard to read the 192 diode pads on a full-size LD Si sensor. In the LD Hexaboard, we have 3 HGCROCs with 78 channels for readout(72 normal channels +4 common mode ones and 2 calibration channels), only 64 of these are used for readout in the LD board. For the TPG (trigger primitive generator), the board is divided into 12 supercells with 4 trigger cells each.

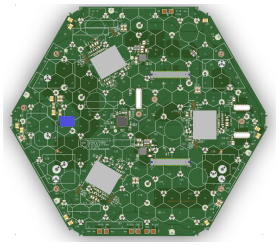

Figure 7: LD Hexaboard.

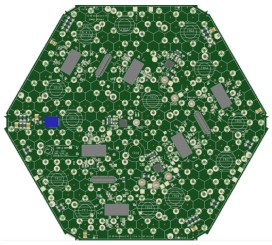

Figure 8: HD Hexaboard.

1.2 Electronics

HGCAL was designed to capture detailed collision data at a rate of 40 MHz, matching the rate of proton bunch collisions. However, each event generates a large amount of data, between 2.5 to 3.5 MB. Storing all of these data is not feasible. To manage this, a quick analysis is done on a lower-resolution stream of data. This determines whether to keep the high-resolution data, which can be read out from the detector at a rate of up to 750 kHz. Only around 7500 events per second are stored in permanent storage after further processing by a software system. There are two separate paths for reading out the different resolution data: the Data Acquisition (DAQ) path handles high-resolution data and the TPG path deals with lower-resolution data and decides when to acquire the high-resolution data. Due to the sheer volume of data, some processing and selection are necessary early in the chain. While part of this process occurs on the detector, where radiation constraints are crucial, some of the electronics are shielded from radiation. This is why the readout process is divided into on-detector frontend (FE) and off-detector backend (BE) electronics. The detector comprises about 6 million channels, all read by the HGCROC ASICs. These ASICs perform three types of signal measurements: Analogue to Digital Converter (ADC) for small charge deposits, Time over Threshold (TOT) for very large deposits that saturate the pre-amplifier, and Time of Arrival (TOA) which measures the timing of the charge deposit.

1.3 DAQ

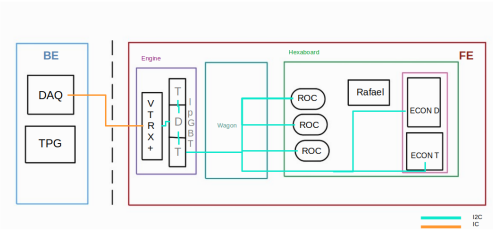

Figure 9: Slow control commands path (downstream).

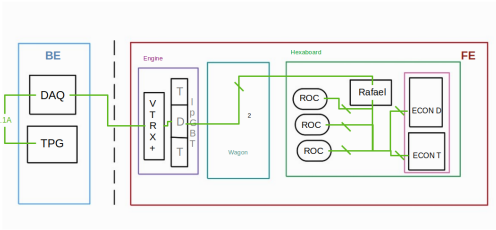

Figure 10: Fast control commands path (downstream).

The HGCROC high-resolution data are sent to the concentrator ASICs ECON-Ds. The ECON-D ASIC is mounted on the wagons in HD regions. In the LD regions, the mezzanine has the ECON-D, responsible for processing the data from the HGCROCs on that LD hexaboard. ECON-D output data is communicated to the DAQ BE. The FE interface with the BE is done via the Low-Power GBT (lpGBT), which provides high-speed bidirectional communication: the downlink (BE to FE, used for control and configuration) and the uplink (FE to BE, used for ECON-D data, Figure 11). The Versatile Link Plus Transceiver (VTRX+) ASIC is used to convert the electrical signals from the lpGBT into

optical signals completing the FE readout chain. The lpGBTs and VTRX+s are mounted on an engine to ensure communication.

The ASICs need to be configured, and these commands can be Fast Control Commands or Slow Control Commands. The FC commands synchronous commands concerning the bunch crossings, and thus they control the data flow in the detector (Figure 10). The SC commands (Figure 9) are asynchronous concerning the bunch crossings and they are used to configure and monitor the FE ASICs parameters.

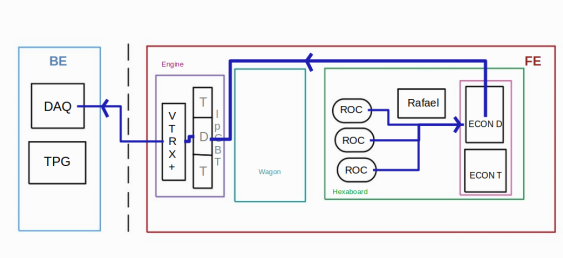

Figure 11: DAQ Readout (upstream).

2 Hexaboard tests

Testing LD hexaboards and doing a performance evaluation starts with an optical inspection in the microscope. Then if everything checks out in the optical inspection we do tests to access the HGCROCs. The noise, pedestal, and the digital modulation through the delta pedestal, are valuated. A phase scan is also performed the TPG DAQ is checked and the power before and after configuration in the ROC's is measured. After this, the boards undergo thermal cycling and return for the same performance tests.

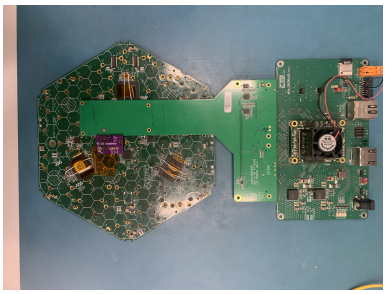

Figure 12: Setup for hexaboard tests (with no connections).

The pedestal is the ADC value associated with the baseline level of the analog signal when there is no actual signal or input present. This value is important because it provides a reference point for distinguishing between the signal and noise. The digital modulation, Δ-pedestal, is the maximum difference of pedestals for varying sampling phases.

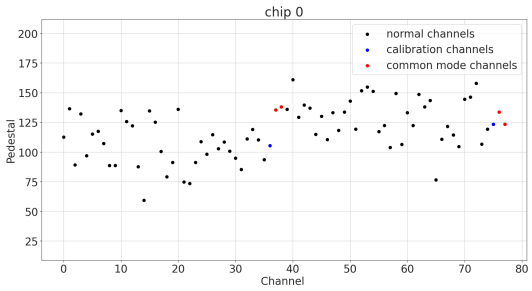

Figure 13: Pedestal in ADC counts (chip 0).

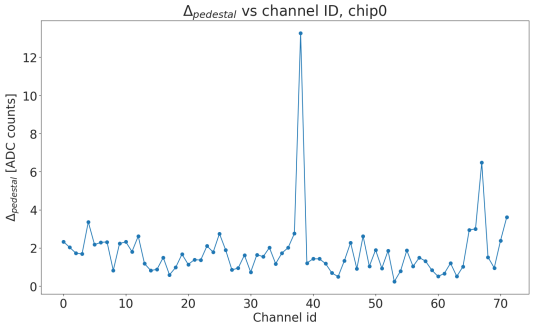

Figure 14: Delta Pedestal (chip 0).

The noise is the standard deviation of the ADC distribution of one HGCROC channel. The mean value of the noise distribution for all channels; ideally, is the average noise value for a chip, as shown in Figure 15.

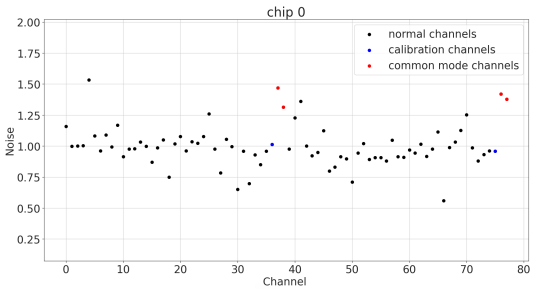

Figure 15: Noise in ADC counts (chip 0).

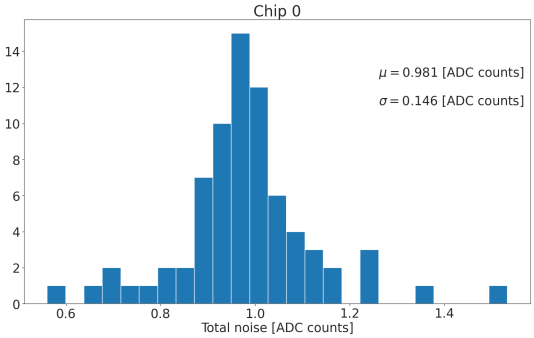

Figure 16: Noise distribution (chip 0).

In summary, noise refers to random fluctuations that can distort a signal, while the pedestal is a reference value around which a signal fluctuates due to factors like noise. Both noise and pedestal are crucial considerations for accurate signal processing and measurement. The results obtained are outstanding compared to the previous versions of these hexaboards which is very positive since HGCAL is going into the production phase.

3 DAQ system

The ECON-D concentrator ASIC was missing in the setup since it is still in production. This would allow a specialized integrated circuit to aggregate or concentrate data from multiple sources into a single output stream. Given that, there is a replacement, an FPGA emulator, that will connect to the hexaboard through the Unicorn Board that monitors the signal integrity. The electrical quality of any signal can be visualized and determined through an eye diagram (Figure 17). The eye diagram is constructed by superpositioning transition edges (rising and falling edges) of several data patterns over one unit interval. It can provide us with several parameters useful for jitter analysis, such as the rise and fall time of the signal, total jitter information, and BER (bit-to-error rate). However we are interested in the best time to sample (decision point). For this, there is a need to adjust the timing of the sampling phase and the link alignment.

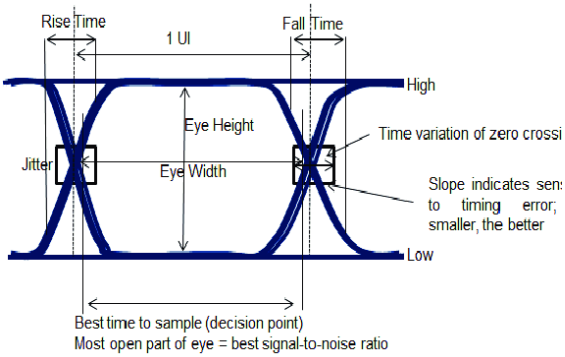

Figure 17: Eye Diagram.

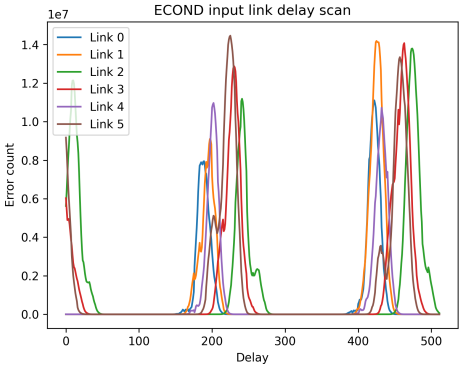

Figure 18: Input link delay scan for ZCU.

It was determined when the FPGA needs to sample the different links by determining the optimal delay. How? There are 6 links from the 3 HGCROCs and they were scanned for the most optimal delay to use. For this, it is plotted an error count vs. delay at which to sample as we can observe in Figure 18. There are two possible eyes to choose from and ideally the delay is the value in the middle of the eye.

4 Module tests

For these tests, the cold probe station from the silicon lab was used, since it was needed to vary the temperatures from room temperature to -40°C. The setup used is shown in Figure 19.

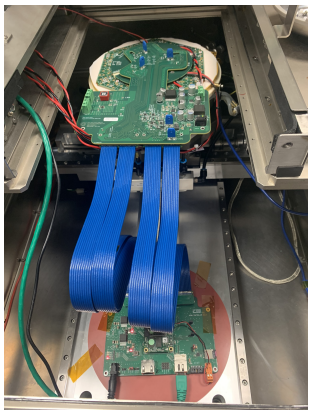

Figure 19: Setup in the cold probe station.

4.1 Non irradiated modules

For one HD module assembled that was not irradiated the same pedestal run that was done for the hexaboard was performed. Some abnormalities were found for half of the chip 3 in all measurements. This was found to be a problem with the FPGA being used and for future reference, the diode pads around chip 3 will not be used for laser measurements.

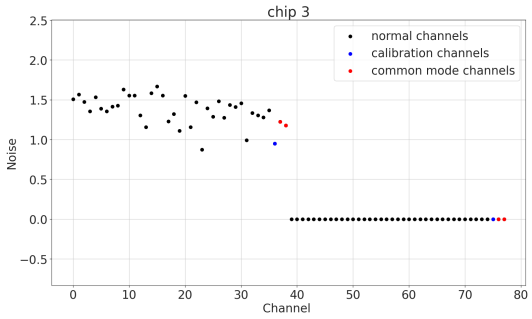

Figure 20: Noise in ADC counts (chip 3).

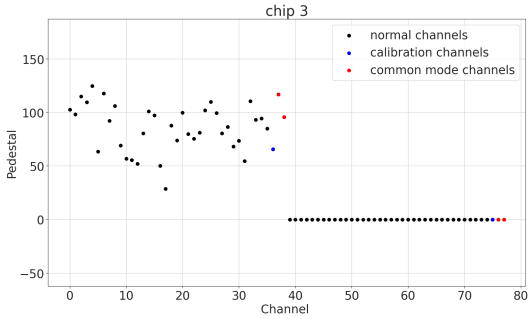

Figure 21: Pedestal in ADC counts (chip 3).

4.2 Irradiated modules

Measurements of current voltage were taken and compared to previous data for bare Hexaboard. Figure 22 shows the bias voltage applied and Figure 23 the effective voltage. The effective voltage was calculated with:

$$\text{Bare} \quad U_E = U - 12000 * I_{tot} \tag{1}$$

$$\text{Module} \quad U_E = U - 30000 * I_{tot} \tag{2}$$

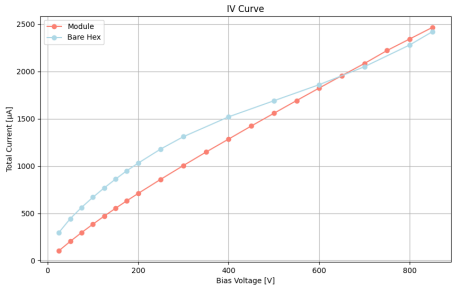

Figure 22: IV curve for bias voltage.

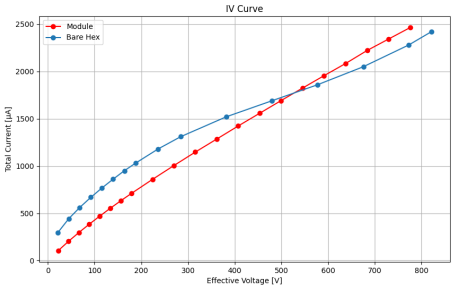

Figure 23: IV curve for effective voltage.

In the modules with irradiated sensors, leakage current compensation is done during calibration. The DC level of HGCROC channels' preamplifier output follows the leakage current which may lead to the dynamic range becoming small. The input DAC is tuned to compensate for this. Input DAC tuned as the lowest DAC value to have ADC pedestal below 150 (reminder: maxi ADC value = 1023). The results obtained for the different channels can be seen in Figure 24. The rest of the results can be found in the Appendix B.

5 Conclusion

In conclusion, the efforts described in this work represent a step in the larger endeavour of constructing the High-Granularity Calorimeter. The subdivision of the readout chain into frontend and backend electronics highlights the complex nature of data processing, balancing radiation constraints with processing capabilities. Looking ahead, forthcoming work will encompass laser tests to evaluate the diode pads and assess leakage current for the irradiated modules, cold box testing to validate module performance, and the assembly of cassettes. Additionally, a pivotal beam test in September will serve as a comprehensive debugging and system testing phase, solidifying the robustness and functionality of the HGCAL components being developed as you read this.

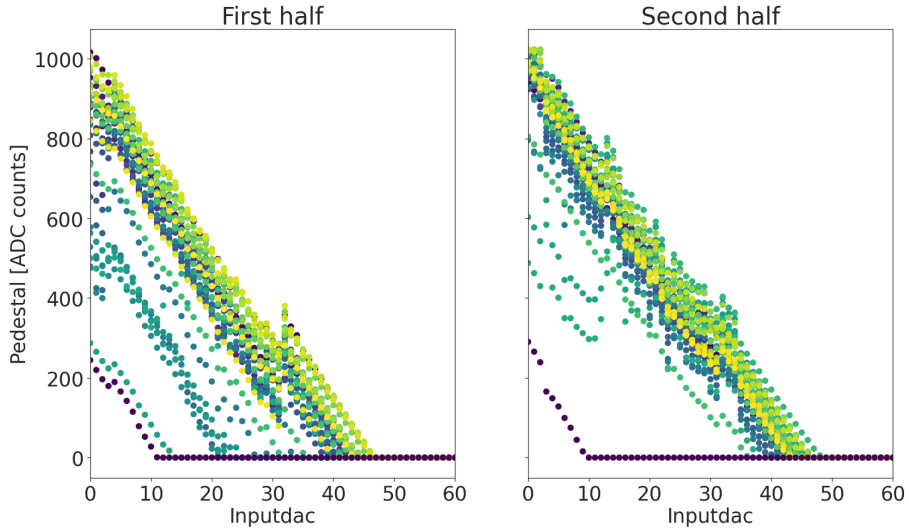

Figure 24: Pedestal vs. Inputdac for -34°C .

Acknowledgements

I wish to thank my supervisors André David and Mehmet Alp for all the help and guidance. I would like to also thank Martim Rosado, Eva Sicking, Milos Vojinovic, Wesley Terril, Oliwia Kaluzinska, Shubbham Dutta, Simon Andersen, Fakhri Khan, Arnaud Steen and Fabio Monti. It was wonderful working with you all.

Bibliography

[1] Pedro Martim Duarte Rosado. Scalable FPGA-based controller of a thousand-ASIC system in the CERN CMS HGCAL detector, 2023. Presented Nov 2022.

[2] CMS Collaboration. The Phase-2 Upgrade of the CMS Data Acquisition and High Level Trigger. Technical report, CERN, Geneva, 2021. This is the final version of the document, approved by the LHCC.

[3] lpGBT Team. *lpGBTv1 Manual*.

[4] The Phase-2 Upgrade of the CMS Endcap Calorimeter. Technical report, CERN, Geneva, 2017.

[5] Fakhri Alam Khan. Design and Performance Optimisation of the Hexaboards for CMS HGCAL On-Cassette Readout Electronics. Technical Report 03, CERN, Geneva, 2023.

[6] André David. Performance of the cms hgcal for lhc phase 2. ICHEP 2022 Bologna, 2022.

[7] CMS Collaboration. Hgcroc3 spec working document 2.0, 2021.

[8] Matt Noy. The cms hgcal silicon region architecture specification and optimisation, 2021.

[9] N Strobbe. Readout electronics for the CMS Phase II Endcap Calorimeter: system overview and prototyping experience. *JINST*, 17(04):C04023, 2022.

[10] Peter Paulitsch. The silicon sensors for the high granularity calorimeter of cms. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 978:164428, 2020.

[11] Simon Andersen. Auto tracking in zcu, 2023.

Appendix

A HB testing

A.1 Data for other chips

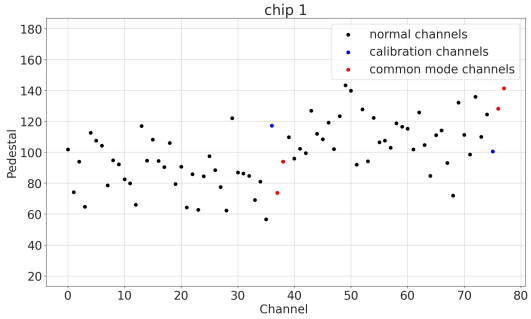

Figure A.1: Pedestal in ADC counts (chip 1).

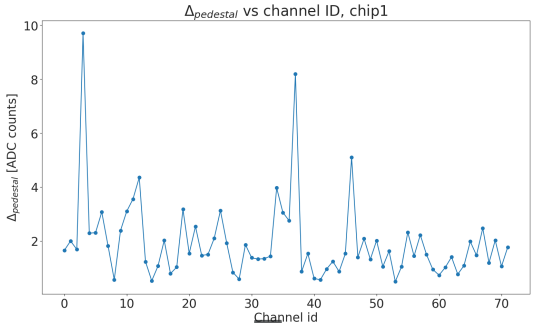

Figure A.2: Delta Pedestal (chip 1).

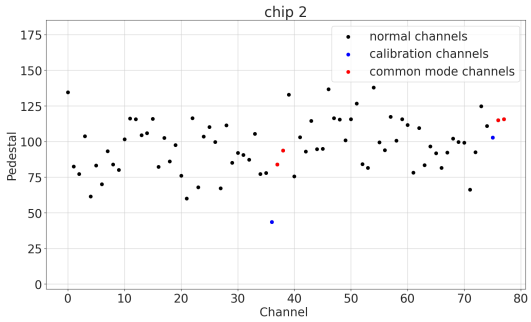

Figure A.3: Pedestal in ADC counts (chip 2).

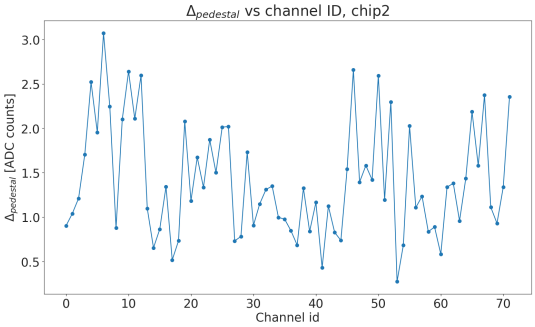

Figure A.4: Delta Pedestal (chip 2).

B Module testing

B.1 Non-irradiated module pedestal run

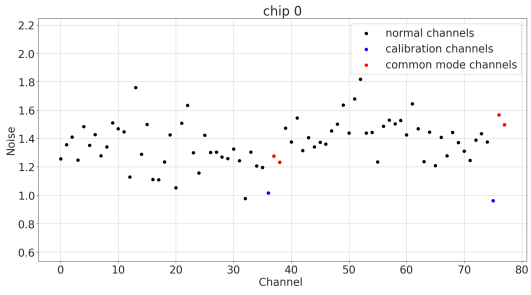

Figure B.1: Noise in ADC counts (chip 0).

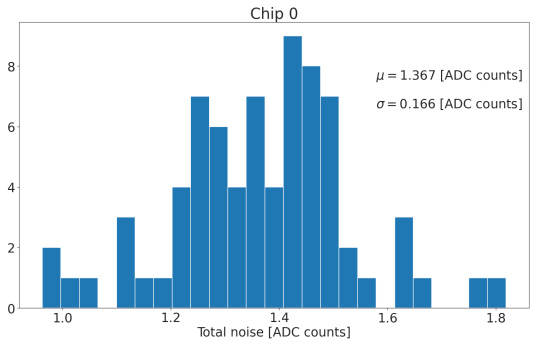

Figure B.2: Noise distribution (chip 0).

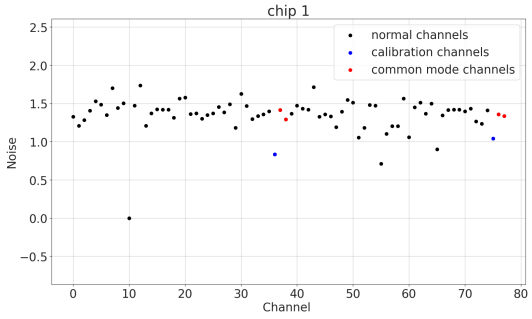

Figure B.3: Noise in ADC counts (chip 1).

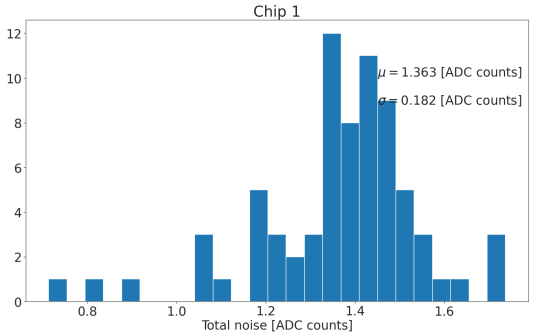

Figure B.4: Noise distribution (chip 1).

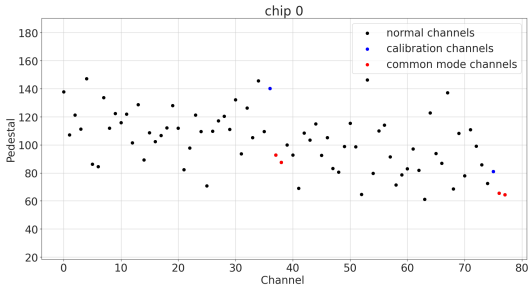

Figure B.5: Pedestal in ADC counts (chip 0).

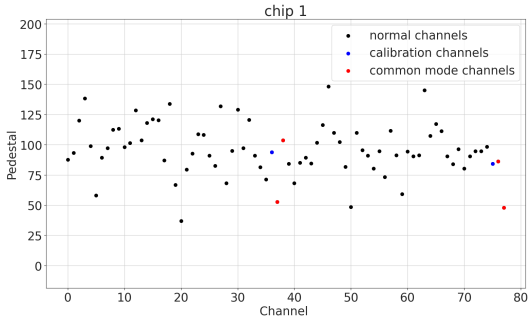

Figure B.6: Pedestal in ADC counts (chip 1).

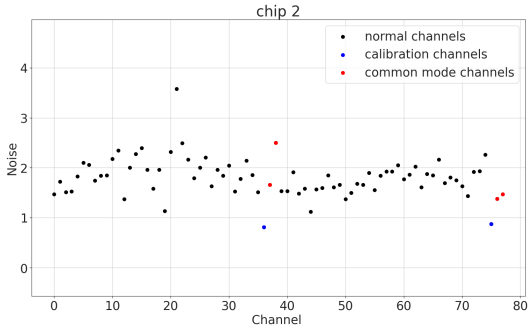

Figure B.7: Noise in ADC counts (chip 2).

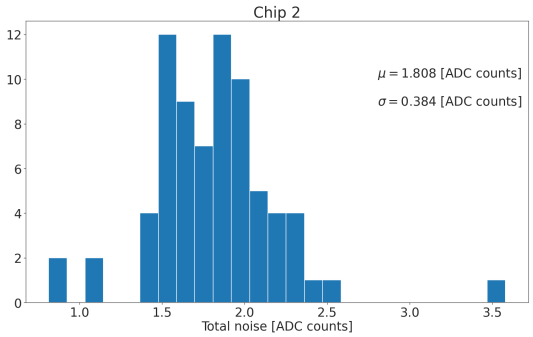

Figure B.8: Noise distribution (chip 2).

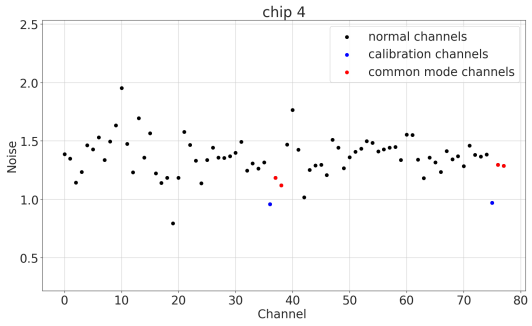

Figure B.9: Noise in ADC counts (chip 4).

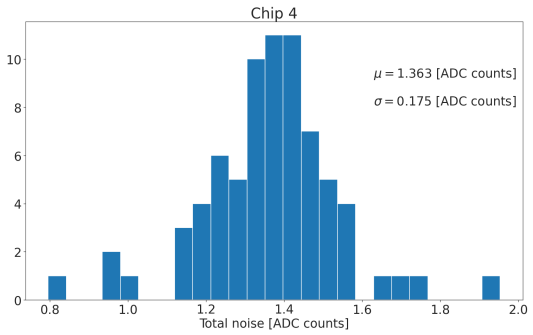

Figure B.10: Noise distribution (chip 4).

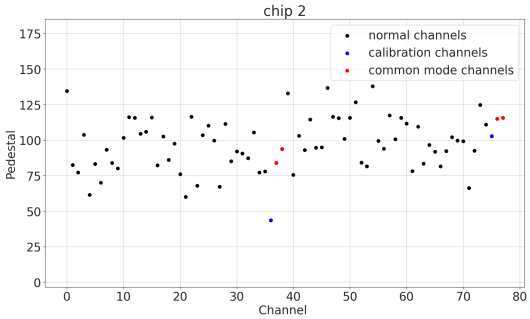

Figure B.11: Pedestal in ADC counts (chip 2).

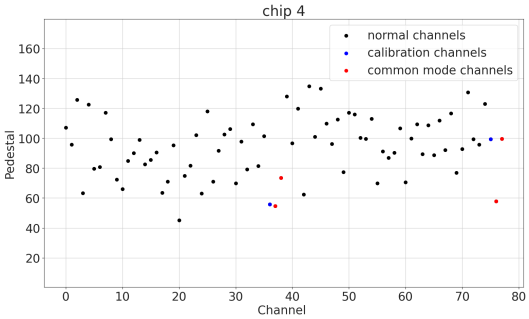

Figure B.12: Pedestal in ADC counts (chip 4).

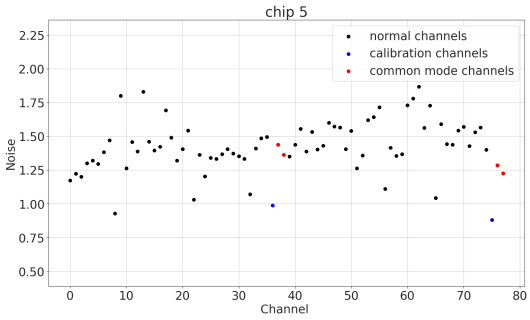

Figure B.13: Noise in ADC counts (chip 5).

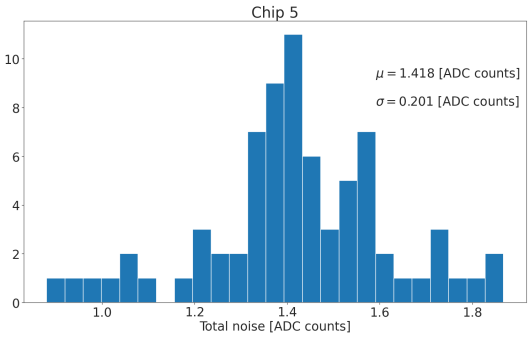

Figure B.14: Noise distribution (chip 5).

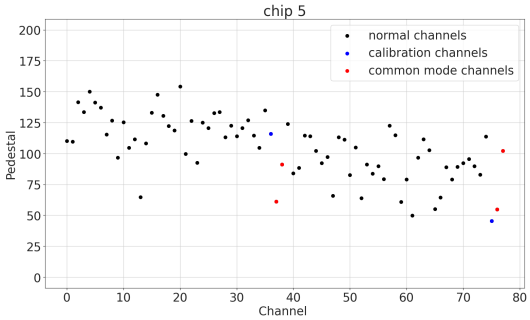

Figure B.15: Pedestal in ADC counts (chip 5).

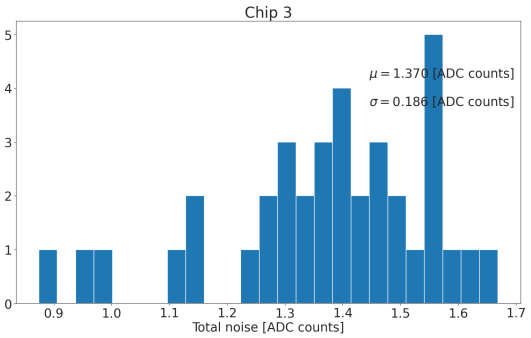

Figure B.16: Noise distribution (chip 3).

B.2 Inputdac scans

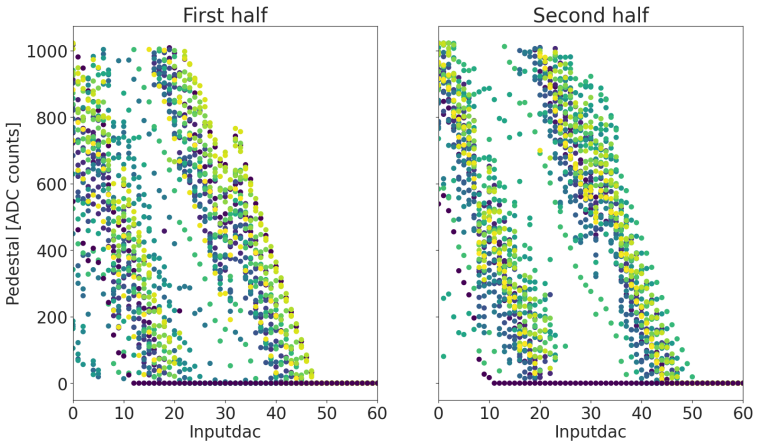

Figure B.17: Pedestal vs. Inputdac for -32°C .

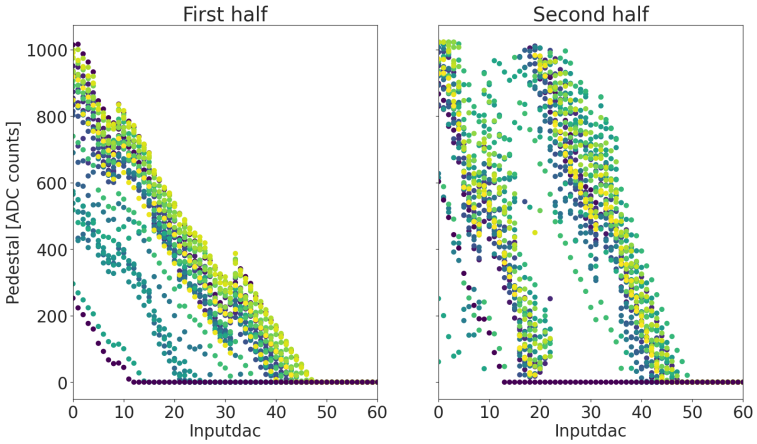

Figure B.18: Pedestal vs. Inputdac for -33°C .

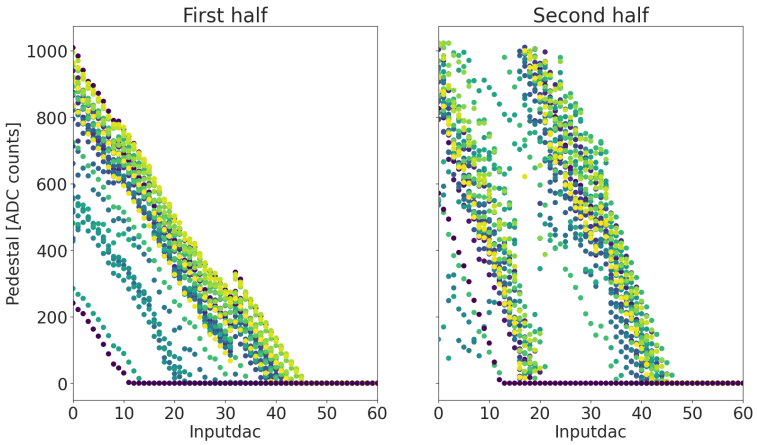

Figure B.19: Pedestal vs. Inputdac for -35°C .