Single Event Effect Testing of Commercial Silicon Power MOSFETs

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CERN-THESIS-2020-190
26/10/2020

Xanthi, October 2020

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Diploma Thesis

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Abstract

Silicon Power MOSFETs, devices designed to handle significant power levels, are widely used as parts of power management electronic systems, distributed along the CERN accelerator complex. However, irradiation can compromise their performance, as under certain bias conditions they are particularly sensitive to destructive Single Event Effects (SEE), caused by a single ionizing particle randomly passing through the sensitive regions of the device. These effects can be distinguished in Single Event Burnouts (SEB) and Single Event Gate Ruptures (SEGR), both of which lead to the complete failure of the power MOSFET and hence of the system in which it is embedded.

The present thesis is devoted to the experimental evaluation of the SEE sensitivity of commercial power MOSFETs, as well as to the study of the effect of certain parameters, related to the device itself (biasing, operational characteristics, technology) and to the irradiation conditions (particle type, energy, LET). For the experimental tests, which involve the irradiation of MOSFETs with beams of energetic particles, a setup that allows for the detection, counting and saving of the SEB-generated pulses, while protecting the devices from catastrophic failure, has been employed. Recent modifications on the test setup have enabled the distinction between SEBs and SEGRs, as well as the on-line characterization of the samples.

Irradiation campaigns have been carried out in a variety of European facilities and involved the exposure of power MOSFETs to high energy proton beams, neutrons with an atmospheric-like spectrum, a mixed-field that is representative of the high-energy accelerator spectra, and lastly to heavy ions of different type and energy. The tested commercial power MOSFETs were selected among candidates interesting for CERN accelerator applications, including parts of different manufacturers and rated voltage capabilities. A detailed compilation of the results obtained, along with relevant comparisons and observations, is included in the thesis.

Keywords: power MOSFETs, Single Event Burnout (SEB), Single Event Gate Rupture (SEGR), non-destructive, protons, neutrons, heavy ions

Acknowledgements

The present thesis constitutes the epilogue of my undergraduate studies and I could not omit acknowledging the contribution of all the people that were part of this fascinating journey. The conversations and interactions with them have decisively broaden my knowledge and interests both on a professional and on a personal level.

Firstly, I would like to thank my professor Filippos Farmakis for his support in utilizing my work as a Technical Student to complete my diploma thesis, as well as for his interest and valuable advice throughout my studies. I would also like to express my gratitude towards my CERN supervisor, Pablo Fernández Martínez. I can only warmly thank him for the constant guidance, his trust in my abilities, and all of our enlightening discussions and shared stories. Likewise, I wholeheartedly thank Rubén García Alía for his decisive role in the project and the unique opportunity provided. A big thanks goes to Salvatore Danzeca and Gilles Foucard for their crucial support to the hardware-related part of the project and especially the preparation of the samples as well as the designing and building of the Test Board. I would also like to thank all the members of the R2E group, who welcomed me from day one and made life in the office or during experimental campaigns much more pleasant.

Of course, an invaluable part of this experience has been all of my friends, both the ones at Greece and the ones I made at CERN, whom I thank for the moral support, the great times we have spent together and the laughs we have shared. Finally and above all, words are not enough to thank my family, my parents and my sister, for their constant love and support.

Contents

1 Introduction

CERN, the European Organization for Nuclear Research, is the largest particle physics laboratory in the world and it was created in 1954. Its main research interest is the discovery and study of new subatomic particles by operating a network of accelerators, whose purpose is to increase the energy of particle beams before delivering them to experiments or the next most powerful accelerator. As of 2019, the accelerator complex consists of six accelerators (LINAC, Booster, LEIR, PS, SPS, LHC), as shown in Fig. 1.1, with LHC (Large Hadron Collider) being the biggest and most powerful one. With a circumference to 27 km and by accelerating and colliding two proton beams of energies up to 7 TeV, LHC led to the discovery of the theorized Higgs boson in 2012, ensuring this way the consistency of the standard model.

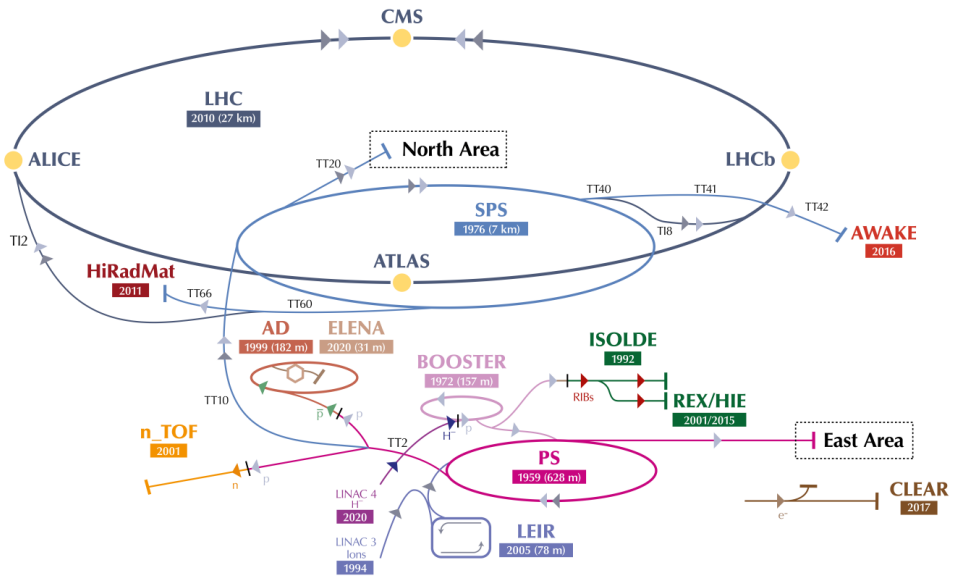


Fig. 1.1: The CERN accelerator complex [1].

The protons are created at the Proton Source, where the hydrogen is gas is broke down to its constituent protons and electrons, and undergo a gradual process of acceleration until they are transferred to the LHC, organized in two beams of opposite directions. In the LHC, after a transit time of approximately 45 minutes, the beams eventually reach their maximum energy and the phase of stable beam is initiated, during which collisions between the opposite-moving protons take place. The duration of an uninterrupted stable beam cycle ranges from 10 to 15 hours and

when the quality of the beam is degraded, the LHC operator decides to interrupt the run through a controlled dump.

However, the beam dumps are not always intentional and in a lot of cases they are caused by unexpected failures, therefore reducing the available stable beam time. On top of that, more delays arise until the technicians locate and resolve the cause of failure, as well as until the operators develop a new stable beam. Taking into consideration, that in 2012 70% of the dumps were of this nature, it is clear that they are a major confinement to the efficiency and the availability of the machine, increasing significantly the cost of operation.

Among the failures that may cause the premature dump, a common one is related to the complex field of radiation that is produced by the beam-machine interactions. In more detail, the generated mixed-field environment is accountable for radiation induced errors in electronic components or systems that are used in the LHC tunnel and its adjacent, partly shielded areas. For instance, in 2011 about 70 beam dumps were provoked by radiation effects on electronic equipment causing a downtime for the machine of about 400 hours [2]. The radiation induced failures on electronic equipment were mainly Single Event Effects (SEE), i.e. stochastic events that are caused by a single ionizing particle, as it will be further explained in Chapter 3.

Therefore, in an attempt to follow up on the radiation related equipment failures and propose mitigation and prevention strategies, the CERN Radiation to Electronics (R2E) project was established. One of its main objectives has been the radiation hardness assurance of Commercial-Of-The-Self (COTS) components before they are used in electronic designs near the LHC, by performing carefully designed radiation tests and exposing them to extreme radiation environments. It is worth noticing that commercial components, rather than radiation hardened ones, are widely used in electronic systems for the LHC, due to their lower cost, higher availability and better compliance with application requirements. Thanks to the efforts in the R2E project, the downtime of the accelerator because of failing electronics was reduced to 250 hours in 2012.

Silicon (Si) power MOSFETs are among the commercial components that are widely used as parts of more complex designs (e.g. DC-DC converters), due to their capability of handling high levels of power. However, they are also particularly sensitive to radiation, and especially destructive SEEs, compromising this way the performance and reliability of the whole system they are integrated into. As a result, their qualification against radiation has been integrated in the activities of the R2E project and defined the aim of this thesis: the characterization of the SEE sensitivity of a variety of COTS Si power MOSFETs. Apart from characterizing the components as radiation tolerant or not, an additional research goal is the investigation of the

beam conditions, as well as the devices' characteristics and potential technology trends that increase the SEE susceptibility. To do so, an already existing test setup will be updated and improved, and a variety of irradiation tests will be performed at European facilities that offer beams of different particles and characteristics.

The content of the thesis is organised as follows:

- Chapter 2 gives a theoretical background on the technology of power MOSFETs, providing more information about their structure and operation principles.

- Chapter 3 gives a theoretical background on the radiation effects on electronics, focusing on destructive SEE, as they are the ones that affect power MOSFETs. A bibliographic review of the most relevant findings in the research community is also provided.

- Chapter 4 describes in detail the experimental methodology for the evaluation of power MOSFETs' response to SEEs. The test setup, as well as the advancements made in the framework of this thesis, are also discussed.

- Chapter 5 provides a summary of the irradiation campaigns performed, including a short description of the facilities visited and the characteristics of the beam they offer. The commercial power MOSFET references that were selected for the tests are also introduced.

- Chapter 6 presents and discusses the experimental results for each power MOSFET reference from all irradiation campaigns.

- Chapter 7 provides a brief summary of the main results, conclusions and possible future steps.

State of the art: Power MOSFETs

2

2.1 Introduction

Due to its low power consumption for gate drive and fast switching speed, the Silicon power MOSFET is the most common power semiconductor device in the world, accounting for 53% of the power transistor market as of 2010 [3]. It was commercially introduced in 1970s and its invention was partly driven by the limitations of bipolar junction transistor (BJT), which was the device of choice in power electronic applications, until that time. The BJT, depicted in Fig. 2.1, has disadvantages which are related to the fact that its operation relies in minority carriers injected in the base to "defeat" recombination and be re-injected in the collector. These disadvantages, briefly discussed below, were overcome with the introduction of power MOSFETs.

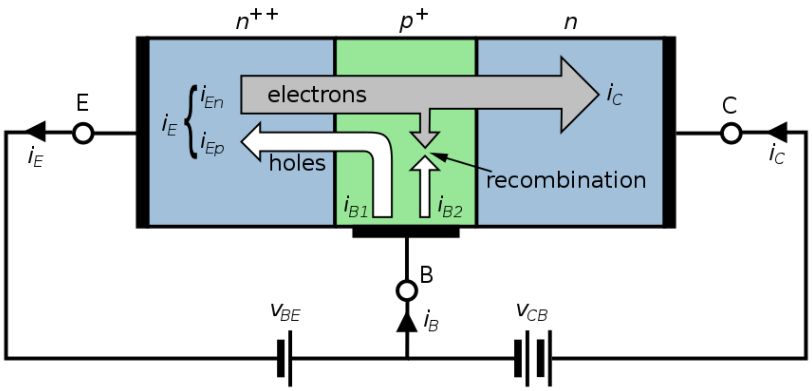


Fig. 2.1: Cross section of a npn Bipolar Junction Transistor and its working principle [4].

First of all, BJTs are associated with large storage times, because of the injected charge in the drift region. In more detail, when a BJT has to be switched off, there is a considerable amount of minority carriers in the base region, with low recombination factor, to be taken care of before the current conduction is stopped. Therefore, the operation speed and the frequency of the device become limited.

Additionally, a BJT is defined as a current driven device and the current gain drops significantly as the collector current increases. This means that the higher the current that must be driven, the higher the supplied current must be. As a result, their efficiency is significantly reduced due to the increased power dissipation. Another

related consequence is the need for complicated, and thus expensive, circuit designs to drive the base.

On top of that, bipolar transistors are prone to destructive failure due to secondary breakdown. When trying to block a lot of power with a BJT, local defects tend to concentrate the current. This induces the localized heating of the silicon. Since the temperature coefficient of the resistivity is negative, local defects create a low resistance path for the current, leading to the sourcing of an even higher current. The temperature of the material is then further increased, until a non-reversible destruction occurs.

Finally, designs using BJTs connected in parallel may be vulnerable; the device with the lowest saturation voltage potentially diverts most of the current, overheating and ultimately resulting in a short-circuit [5].

In conclusion, even if BJTs are still used in applications limited to frequencies of 10 kHz, they have almost disappeared from the cutting-edge applications where overall efficiency is the most important parameter.

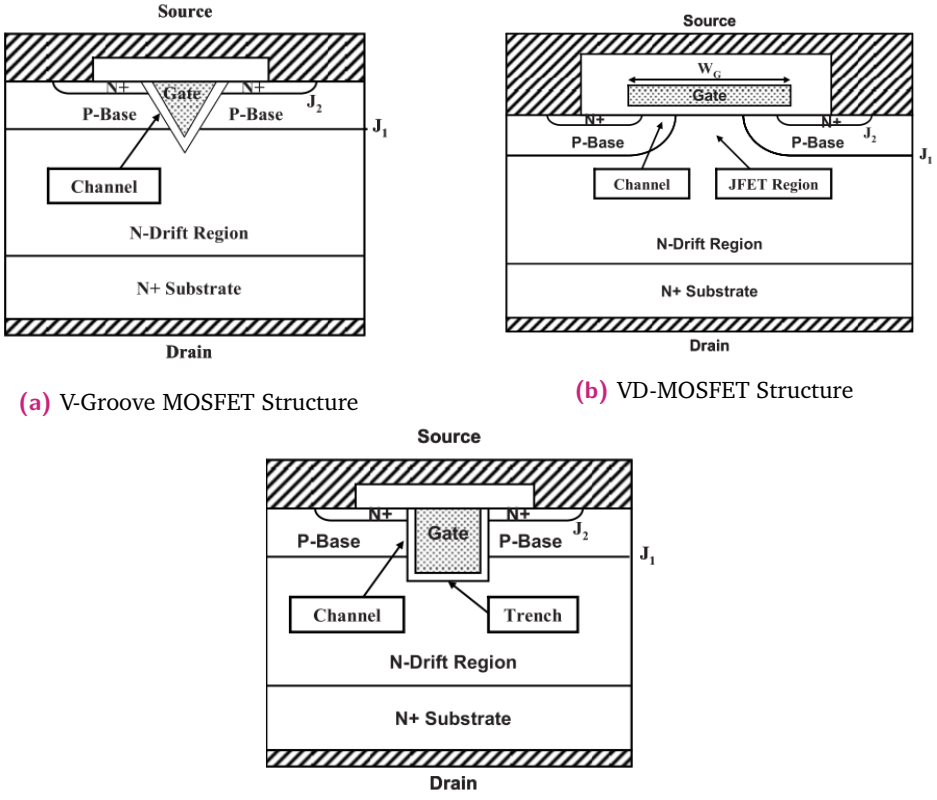
In contrast, power MOSFETs are majority carrier devices with no stored minority charge, therefore they can work at much higher frequencies. Even when fast switching is not the major focus of an application, power MOSFETs are still favored, as they experience much less losses compared to BJTs. Additionally, they can withstand simultaneous application of high current and high voltage without undergoing destructive failure due to second breakdown. Lastly, power MOSFETs can also be paralleled easily because the forward voltage drop increases with increasing temperature, ensuring an even distribution of current among the components [6].

2.2 Structure

The main functionality of a power MOSFET is similar to the standard MOSFET one: they both have three terminals (Gate, Source, Drain) and depending on the external bias of these terminals their operation can be separated into three different modes (Cut-off, Inversion, Saturation). The main difference between them is that a power MOSFET typically features a vertical structure with the Source and Drain on opposite sides of the wafer, which allows them to support higher current and voltage levels. The vertical structure enables the use of thick source and drain electrodes avoiding transport of the current through thin metal fingers, which are typically used at lateral device structures. In addition, the potential distribution within the vertical structure is more favorable for supporting high voltages.

Likewise with standard MOSFETs, power MOSFETs can be distinguished in n-channel and p-channel ones, depending on the majority carriers flowing through the channel when the device is turned-on. However, p-channel power MOSFETs are rarely preferred over their n-channel counterparts, with the only exceptions being applications were a High-Side switch is required or the voltage blocking requirements are low. In general, p-MOSFETs are known to have three times higher resistance when turned-on compared to an identical n-channel one, due to the difference in carriers' mobility. It will also be explained in Section 3.3, that p-MOSFETs are practically immune to Single Event Burnout phenomena, because of their parasitic PNP transistor being less prone to turn-on. As a result, the discussion in this study will be focused on n-type power MOSFETs.

Fig. 2.2 shows the evolution of the power MOSFET design. Despite the differences of the power MOSFET configurations discussed below, their structure is similar. As seen in Fig. 2.2, the N+ Source and Drain regions are separated by the P-Base region. A lightly doped epitaxial layer, called the N- Drift region, followed by the heavily doped N+ Substrate intervene between the P-Base and the Drain electrode. The source metallization covering both the the N+ Source and the P-Base contributes to the suppression of the N-P-N parasitic transistor formed between these regions along with the N-Drift region.



(a) V-Groove MOSFET Structure

(b) VD-MOSFET Structure

(c) U-MOSFET Structure

Fig. 2.2: Power MOSFET structures in the chronological order they appeared [7].

The first power MOSFET structure, introduced in 1969 by Hitachi Ltd., was developed using a V-groove etching process and was named V-Groove MOSFET or V-MOSFET in short (see Fig. 2.2a). The V-groove was formed by using a potassium hydroxide-based etch for silicon, and its angle was determined by the crystal structure of the silicon. However, this structure fell out of favor for two main reasons: The first one was that the potassium of the etching solutions contaminated the gate oxide, producing instabilities during long-term operation of the V-MOSFET structure. The second reason was the fact that the sharp apex at the bottom of the groove caused the development of a local region with high electric field, reducing the breakdown voltage [7, 8].

The first commercially successful power MOSFETs were developed in 1977 by HP Labs, using the double-diffusion process. It is called 'the vertical' or 'VD-MOSFET' and the cross section of the basic cell structure is illustrated in Fig. 2.2b. The device structure is fabricated by starting with a heavily concentrated N+ substrate in order to minimize the bulk portion of the channel resistance. A N- type epitaxial layer is grown on it and then two successive diffusions are made, creating the P-Base and the N+ source of the cell, whose difference in lateral extension defines the channel of the power MOSFET. Both regions are self-aligned to the left-hand side and right-hand side of the gate region during ion implantation to introduce the respective dopants. Next, the thin high quality oxide is grown followed by the phosphorous-doped polysilicon deposition, thus forming the gate. Contact windows are opened on the top, defining the source and the gate terminals, while the whole bottom of the wafer makes the drain contact [7, 5].

The main drawback of the VD-MOSFET structure is that a relatively narrow JFET region is created between the adjacent P-Base regions. That substantially increases the internal resistance and a careful optimization of the gate width is required.

That drawback led Philips Semiconductors in the late 1980s to the invention of the U-MOSFET, or 'trench MOSFET' as it is also called, shown in Fig. 2.2c. This invention was enabled by recent developments in the technology for etching trenches in silicon, used mainly for making charge storage capacitors within DRAM chips. The gate structure in a U-MOSFET, instead of being parallel to the die surface, is now built in a trench, perpendicular to the surface, taking much less space and making the current flow truly vertically. Specifically, the trench extends from the upper surface of the structure through the N+ source and P-base regions into the N-drift region. The gate electrode is placed within the trench after the formation of the gate oxide by thermal oxidation of the bottom and sidewalls. Therefore, and due to the absence of the JFET region, there is a significant reduction of the internal resistance. These power MOSFETs offer 50% size reduction for the same internal resistance or a 35% size reduction maintaining the same current handling capability [7, 5].

As to what regards the cell structure of a power MOSFET, thousands of cells are connected in parallel to effectively create a very wide channel (while retaining the channel length of the individual cell) to achieve the large currents required in the ON state. The gate channel width is particularly relevant to the current handling capability of the power MOSFET and it is defined as the third (Z-axis) dimension of the cell cross sections pictured in Fig. 2.2. In general, most power MOSFETs have a multicellular organization, such as the HEXFET configuration, where diffusion lines trace out of a hexagonal grid pattern visible on top of the die (Fig. 2.3, right). Another alternative configuration, mainly used for U-MOSFETs, is the STRIPFET configuration, where the Polysilicon of the Gate has an elongated linear shape (Fig. 2.3, left).

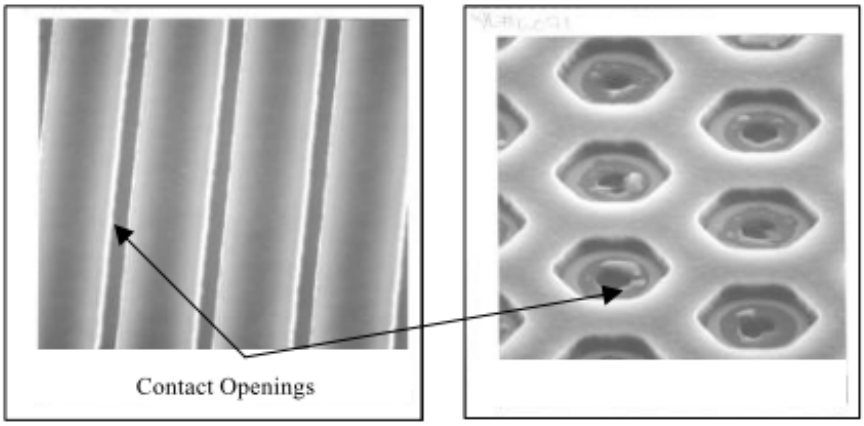
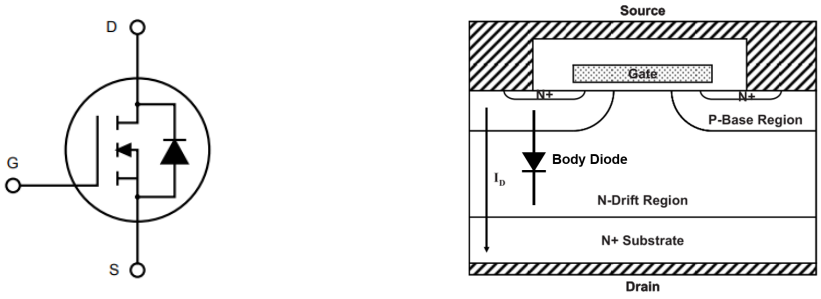


Fig. 2.3: Optical surface views of a stripe cell structure (left) and a hexagonal cell structure (right) [9].

The symbol of a n-channel power MOSFET is depicted in Fig. 2.4a. The connection between the source electrode and P-base region is indicated by the arrow pointing inward in the symbol. The direction of the arrow represents the direction for current flow when the Body Diode in the structure is forward biased. For the n-channel power MOSFET structure, this would occur when the drain potential is negative with respect to the source potential. The Body Diode (depicted in Fig 2.4b) refers to the junction (J1) between the P- Base and the N- Drift region during the third-quadrant operation of the MOSFET. When a negative bias is applied, J1 becomes forward biased, enabling the current flow between the Drain and the Source through the Body Diode [7].

2.3 Operation

The main interest in this study is the first-quadrant operation of the power MOSFET, that is when a positive bias is applied on the Drain node ($V_D > 0$). Depending on



(a) (b)

Fig. 2.4: *(a)* N-channel power MOSFET symbol and *(b)* Schematic of the Body Diode in a power MOSFET cell.

the bias of the Gate (V_G), the power MOSFET can either support a high voltage or carry high-current levels.

In the current-conducting mode, the device can carry high-current levels only when the gate voltage is greater that the threshold voltage of the transistor. The threshold voltage (V_{TH}) is defined as the minimum gate bias required to form a conducting channel between the source and the drain. Gate oxide thickness and doping concentration of the channel are the main parameters that affect the value of the threshold voltage. Therefore, when $V_G > V_{TH}$ an inversion layer at the surface of the P-base region under the gate electrode is created. This inversion layer channel provides a path for transport of electrons from the source to the drain. After passing through the channel, the electrons enter the N-drift region and spread to the entire width of the cell. The maximum current-handling capability is determined by the internal resistance within the structure, as it will be further explained in Subsection 2.4.1.

On the other hand, in the voltage-blocking mode, a high voltage can be supported across the device only when $V_G < V_{TH}$. In this case, the P-N junction J1 formed between the P-base region and the N-drift region (see Fig. 2.2) becomes reverse biased. The voltage is supported mainly within the thick, lightly doped N- drift region.

2.3.1 Current Conducting Mode

The current conducting mode of power MOSFETs can be separated into two regions: the linear one and the saturated one, as it can be seen in Fig. 2.5. Practically, the current starts to saturate when the Drain voltage becomes larger than the applied Gate voltage minus the MOSFET's threshold voltage:

$$V_D \geq V_G - V_{TH}. \tag{2.1}$$

This is when the channel pinch-off takes place.

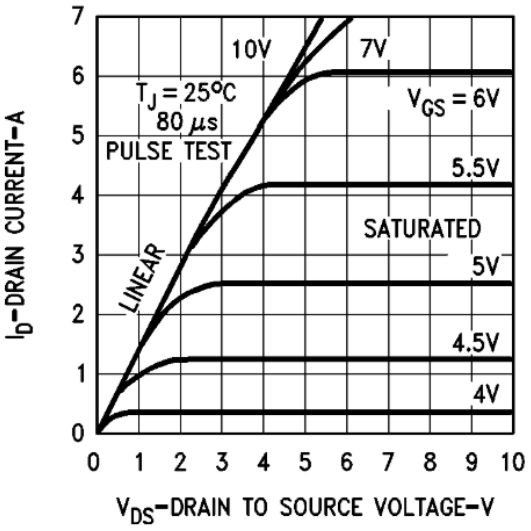


Fig. 2.5: Output characteristics for a power MOSFET with $V_{TH} = 3.5V$. [10]

While at the linear region and for low Gate voltages, the $i - v$ characteristics for the power MOSFET resemble those of a resistor whose value can be modulated by the gate bias. Under these circumstances, the resistance of the channel is much larger than the resistance of the drift region. However at high, compared to V_{TH}, Gate voltages the Drift region resistance becomes dominant and the resistance of the power MOSFET is no longer reduced with increasing Gate bias. This is illustrated in Fig. 2.5, for the cases where $V_G \geq 7V$.

While at the saturated region now, the carriers have reached their maximum velocity. There is a *square-law relationship* between the Drain current and Gate bias, which can be described by:

$$J_{D,sat} = \frac{\mu_{ni} C_{OX}}{W_{Cell} L_{CH}} (V_G - V_{TH})^2, \tag{2.2}$$

where $J_{D,sat}$ is the Drain current per unit area, μ_{ni} is the carrier mobility, C_{OX} is the gate oxide capacitance per unit area, W_{Cell} is the width of the cell pitch and L_{CH} is the length of the channel. Another useful parameter that is commonly used for describing the operation of a power MOSFET structure is its transconductance. The transconductance is defined as the rate of change in the Drain current with incremental Gate voltage and is equal to:

$$g_{fs} = \frac{\Delta I_{DS}}{\Delta V_{GS}} = \frac{\mu_{ni} C_{OX} W}{L_{CH}}. \tag{2.3}$$

A large transconductance is desirable to obtain a high drain current with a small gate bias voltage. In addition, the switching speed of the power MOSFET improves with increasing transconductance [7, 10, 3].

2.3.2 Voltage Blocking Mode

During operation in blocking mode, the Gate electrode is typically shorted to the source electrode ($V_{GS} = 0$) and the applied Drain voltage is supported mainly across the N- Drift region. A particularly important parameter is the Breakdown Voltage (BV_{DSS}), that is the voltage at which the reverse-biased body-drift diode breaks down and significant current starts to flow between the Source and the Drain because of the avalanche multiplication process.

BV_{DSS} depends on a variety of design-parameters, such as the doping profile, the thickness of the cell pitch and the thickness of the different layers. In more detail, a thicker and more lightly doped N- Drift region may support a higher BV_{DSS}, but it will be followed by an unwanted increase of the on-resistance. Additionally, in devices designed to support lower voltages (<50 V), the doping concentration of the P- Base region is comparable with the doping concentration of the N- Drift region, such that a fraction of the applied Drain voltage is supported across a depletion region formed in the P-Base [7]. If the P-Base is not designed thick or heavily-doped enough, the depletion region can punch-through to the N+ Source region and cause lower breakdown. But if it is overdesigned, the channel resistance and threshold voltage will increase, instead [3].

2.4 Electrical Characteristics

The behavior of each power MOSFET is described by a set of characteristics, which are provided by the manufacturer in the Data Sheet. Some of the most relevant characteristics are described in this section.

2.4.1 On-Resistance

The on-resistance of a power MOSFET ($R_{DS(on)}$) defines the amount of current a power MOSFET conducts when turned-on, based on the equation:

$$R_{DS(on)} = V_{DS}/I_{DS}, \tag{2.4}$$

and limits the maximum current-handling capability of the power MOSFET structure. The total on-resistance for the power MOSFET structure is obtained by the addition of all the internal resistances, considering that they are connected in series in the current path between the Source and Drain electrodes. The product of the addition of these internal resistances is described as:

$$R_{DS(on)} = R_{source} + R_{ch} + R_A + R_J + R_D + R_{sub} + R_{wcml}, \tag{2.5}$$

where:
R_{source} is the Source diffusion resistance, R_{ch} is the channel resistance, R_A is the accumulation resistance, R_J is the JFET component resistance of the region between the two body regions of VD-MOSFETs, R_D is the drift region resistance, R_{sub} is the substrate resistance, and R_{wcml} is the sum of resistances related to metallization and bond wires and packaging.

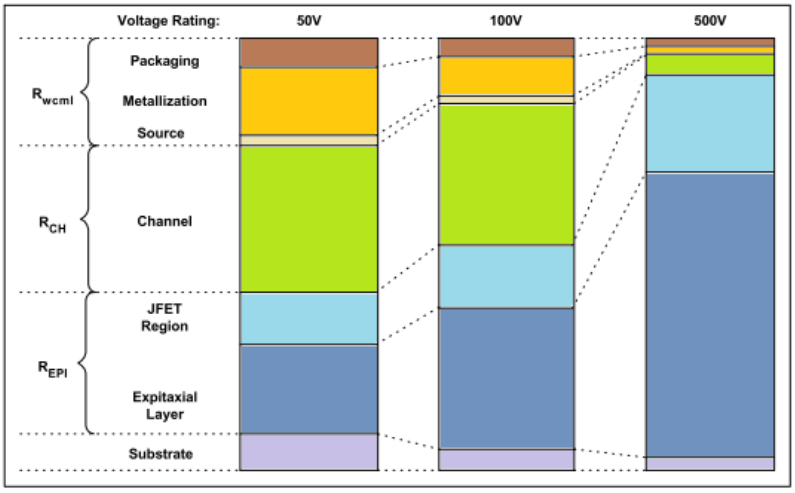


Fig. 2.6: Relevant contribution to $R_{DS(on)}$ with different voltage ratings. [6]

Each one of these internal resistances is accountable for a different percentage of $R_{DS(on)}$, as depicted in Fig.2.6. It is also illustrated how the effect of each internal resistance is altered with changes in the applied Drain Voltage. As it can be seen, at high voltages the $R_{DS(on)}$ is dominated by the resistance of the the epitaxial layer (N-Drift region) and JFET component. This can be explained by the lower background carrier concentration in the epitaxial layer at higher voltages. Moreover, as the applied voltage is decreased, the effect of the channel resistance is mainly enhanced [6].

The channel resistance is also highly dependent on the amount of the gate overdrive and decreases with increasing V_{GS}. When the MOSFET channel turns-on, as V_{GS} becomes larger than V_{TH}, $R_{DS(on)}$ decreases rapidly, but soon reaches a plateau, an indication that the channel is fully turned on and the MOSFET resistance is limited by the rest of the internal components. $R_{DS(on)}$ also increases with temperature due to the decreasing carrier mobility, an important characteristic for device paralleling [3]. Lastly, the device's dimensions also have a significant effect on $R_{DS(on)}$, as a decreasing cell-size leads to lower R_{source}, R_{ch} and R_A, but higher R_{JFET}. The latter increase is explained by the fact that the current is constrained to flow in a narrower region.

2.4.2 Capacitances

The parasitic capacitances of a power MOSFET affect its switching performance, as the turn-on and turn-off times of the device depend on the time required to charge and discharge these capacitances. All the internal capacitances of the device can be incorporated into three main capacitances as shown in Fig. 2.7. These are the Gate-to-Source capacitance (C_{GS}), the Gate-to-Drain capacitance (C_{GD}) and the Drain-to-Source capacitance (C_{DS}). Their values are non-linear, and a function of the device's structure, geometry and bias conditions [3].

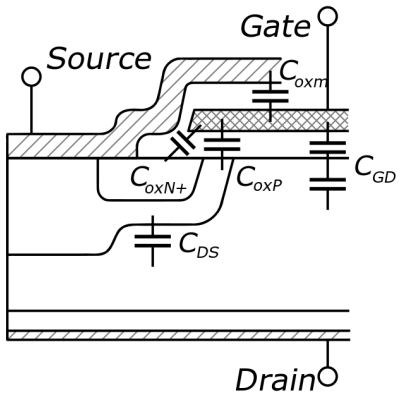


Fig. 2.7: Illustration of the parasitic capacitances of a power MOSFET cell.

In more detail, C_{GD}, or the Miller Capacitance, is made up of the series combination of the gate oxide capacitance and the capacitance of the drain depletion layer beneath the oxide. Its value is a non-linear function of the applied voltage and it is considered an important parameter of the device as it establishes a feedback loop between the input and the output of the circuit. Next, as to what regards C_{GS}, or the Input Capacitance, it exists due to the overlap of the source and the channel regions by the polysilicon gate and is independent of applied voltage. In Fig. 2.7, C_{GS} is equal to the sum of C_{oxN+}, C_{oxP} and C_{oxm}. Finally, the principle component of C_{DS},

or Output Capacitance, is the capacitance of the junction between the P- Base and N- Drift regions and varies inversely with the square root of the Drain-Source bias [8].

The data sheet capacitances are typically defined in terms of the equivalent circuit capacitances as:

- C_{ISS} (Small SignaL Input Capacitance),
  where $C_{ISS} = C_{GS} + C_{GS}$ for $V_D = V_S = 0$

- C_{OSS} (Small Signal Output Capacitance),
  where $C_{OSS} = C_{DS} + C_{GD}$ for $V_G = V_S = 0$

- C_{RSS} (Small Signal Reverse Transfer Capacitance),
  where $C_{RSS} = C_{GD}$

2.4.3 dV/dt capability

When used in a circuit with high operating frequency, it is possible that a power MOSFET undergoes a catastrophic failure due to the rapid changes of the drain voltage. This defines a maximum rate in the increment of the Drain-to-Source voltage to guarantee the safe operation of the device, described by the dV/dt Capability of each power MOSFET. Specifically, there are two possible mechanisms that trigger the dV/dt induced turn-on and they will be explained with the help of Fig. 2.8a. The figure depicts the equivalent circuit of a power MOSFET, where the parasitic capacitances and the parasitic N-P-N BJT are also included.

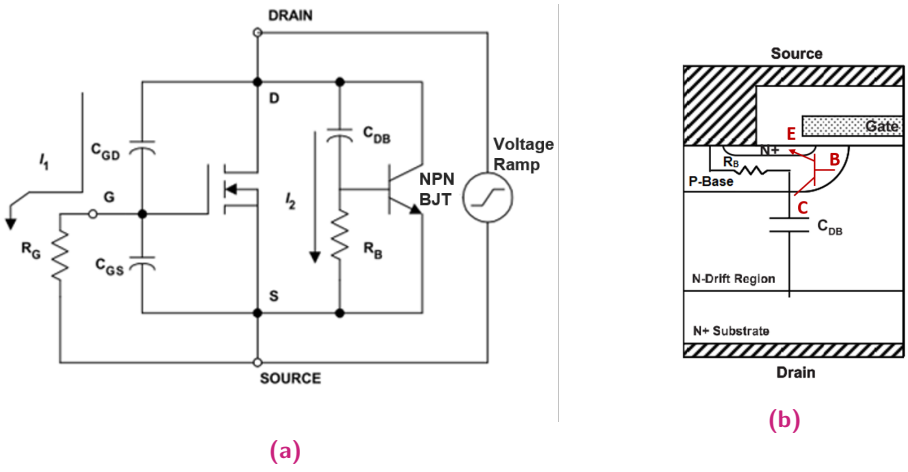


Fig. 2.8: *(a)* Equivalent circuit of Power MOSFETs showing two possible mechanisms for dv/dt induced turn-on and *(b)* Schematic of the Body Diode in a power MOSFET cell.

The first mechanism is activated through the feedback action of the Gate-to-Drain capacitance, C_{GD}. The current flowing through C_{GD} because of a voltage ramp across the device will be equal to:

$$I_1 = C_{DG}\frac{dV}{dt}. \tag{2.6}$$

Additionally, there is a resistance sorting the Gate and the Source, noted as R_G in Fig. 2.8a. Based on Eq. 2.6, the voltage drop across R_G will be equal to:

$$V_{GS} = I_1 R_G = C_{DG}\frac{dV}{dt}R_G. \tag{2.7}$$

Therefore, if this voltage drop is higher than the threshold voltage V_{TH}, the device will be forced into conduction. It is clear that low V_{TH} devices are more prone to dV/dt turn-on. The negative temperature coefficient of V_{TH} is of special importance in applications where high temperature environments are present. In addition, the Gate circuit impedance has to be chosen carefully to avoid this effect. In conclusion, the dV/dt capability for this mechanism is set by:

$$(\frac{dv}{dt})_{max} = \frac{V_{th}}{R_G C_{GD}}. \tag{2.8}$$

The second mechanism for the dV/dt turn-on in MOSFETs is activated through the parasitic N-P-N BJT, which is depicted in Fig. 2.8b. When the power MOSFET is on the voltage blocking mode a depletion region is formed between the P-Base Region and the N-Drift Region. The capacitance associated with this depletion region is denoted as C_{DB} and appears between the Base and the Collector of the BJT. Additionally, the P-Base region of the power MOSFET and consequently the Base of the BJT, despite being heavily doped, still has an inner resistance equal to R_B.

When a voltage ramp appears between the Drain and Source terminals, the capacitance C_{DB} is responsible for a current I_2 flowing through R_B, thus inducing a voltage drop between the the Base and Emitter (V_{BE}) of the BJT. Taking into consideration that a BJT is turned-on when V_{BE} is higher than the built-in potential ($V_{bi} = 0.7V$ for silicon junctions), the dV/dt capability of this mechanism is:

$$(\frac{dv}{dt})_{max} = \frac{V_{bi}}{R_B C_{DB}}. \tag{2.9}$$

This mechanism is key regarding the failure of a Power MOSFET due to Single Event Burnout, as it will be further explained in Chapter 3. Thus, the increasing of the dV/dt capability is of major interest. This requires reducing the value of R_B and can be accomplished by firstly, increasing the P-Base region doping and secondly, reducing the distance current I_2 has to flow laterally before it is collected by the source metallization.

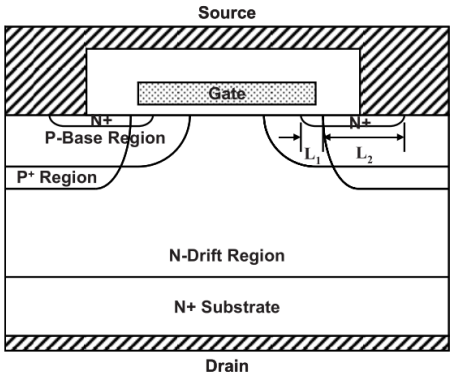


Fig. 2.9: Power VD-MOSFET structure with a deep P+ region [7].

A common approach to reduce the sheet resistance of the P-Base region is the inclusion of a deep, heavily doped P+ region, as the one depicted in Fig. 2.9. Its lateral extension must be restricted to avoid encroachment into the channel and thus to avoid an increase in the threshold voltage of the power MOSFET. It was approximated that for a typical structure, the inclusion of a P+ region reduced the total resistance of the P-Base region by a factor of five. Of course, the dV/dt capability of the device was improved by the same factor [7].

2.5 Other Technologies

Since power MOSFETs were first introduced in the market in the 1970s, a lot of progress has been made in the power electronics community by utilizing emerging technologies and different materials. Some of the most representative structures which compete against traditional Silicon power MOSFETs will be presented in this section alongside their advantages and disadvantages.

i. Insulated-Gate Bipolar Transistors (IGBTs): The Insulated-Gate Bipolar Transistors, IGBTs for short, are vertical devices (the voltage-blocking electrodes are on opposite sides of the wafer) that combine the advantages of BJTs and MOSFETs and are used as switching devices in power electronics applications of 1 kV up to 6.5 kV. In particular, IGBTs are three-terminal devices, that combine an insulated Gate N-channel MOSFET input with a P-N-P bipolar transistor output connected

in a type of Darlington configuration. Thus, the three terminals are labelled as: Collector, Emitter and Gate. Due to its insulated Gate, it is a voltage controlled device with high input impedance and high switching speed. The output switching and conduction characteristics resemble the ones of a bipolar transistor [11, 12].

ii. CoolMOS^{TM}: The technology of CoolMOS^{TM} transistors was introduced by Infineon Technologies AG and combines the low switching losses of a conventional power MOSFET with the on-state losses of an IGBT. Nowadays, CoolMOS transistors are a very popular choice for applications up to 800V. Due to their design, there is linear relationship between their on-resistance and their breakdown voltage, and thus a 600V CoolMOS can have 5 times smaller on-resistance compared to a VD-MOSFET of the same voltage blocking capability. Consequently, a higher current capability per chip area can be achieved along with a lower gate charge. Due to chip shrink and novel internal structure, the CoolMOS technology shows both a very small input capacitance and a strongly non-linear output capacitance, as well. This yields switching losses about 50% lower than those of conventional transistors. One disadvantage of CoolMOS transistors, however, is the poor dynamic behavior of the intrinsic body diode [13, 14].

iii. Laterally Diffused MOS (LDMOS): LDMOS is an asymmetric and lateral double diffused power MOSFET device, meaning that in contrast to the previously discussed devices, the Source and the Drain electrodes are on the same side of the wafer. Its high blocking voltage, along with its short channel length, make LDMOS a popular switching device for systems operating in the Radio Frequency (RF). By having a shorter channel, a high transcoductance can be achieved, which is related to good high-frequency properties. Lastly, a fundamental difference between a conventional power MOSFET and a LDMOS is the connection of the Source to the outside world. Specifically, in the case of VD-MOSFETs, for example, wire bonds must be used to connect the Source to the external circuitry. These wire bonds form a dependant frequency element reducing gain at high frequencies due to negative feedback. On the contrary, the connection of the Source on an LDMOS is formed by diffusing a highly doped p-type region, which acts like an ohmic connection between the Source and the surface of the substrate, eliminating the need for parasitic wire bonds. In conclusion, the advantages of LDMOS devices include their linearity, their negative temperature coefficient, which minimizes the need for external protection circuit, and lastly their convenient incorporation to standard CMOS processes [15, 16].

iv. Silicon Carbide (SiC) Power MOSFETs: In today's technologies, Silicon is the foundation for the production of all kinds of power devices. However, its performance is highly compromised in hostile and hot environments, imposing the need to explore other materials, with higher bandgaps and increased thermal

conductivity, for power-devices manufacturing. The goal is to create devices more robust against disturbances such as heat, radiation or electromagnetic fields.

One of these materials, which has been extensively studied the past several years, is Silicon Carbide (SiC). The key advantage of SiC as a semiconductor material results from the fact that the bonds between the atoms are much stronger. This advantage is usually quantified in terms of a wider energy gap: $3.2V$ for SiC compared to $1.12V$ for Si. However, a more useful parameter to compare materials for the design of power devices is the critical electric field that can be supported by the semiconductor. As such, the critical electric field of SiC is almost 10 times larger than the critical electric field of Si. Practically, the main advantage of SiC MOSFETs is their smaller on-resistances, about 400 lower than that of Silicon devices. Additionally, SiC exhibits an operating temperature of at least 200°C, i.e. 50°C higher than the absolute maximum rating for silicon MOS devices. Sometimes this temperature can go up to 400°C or more. Lastly, 10 times faster switching speeds can be accomplished, resulting in much smaller energy storage capacitors and inductors.

Despite the advantages of SiC devices, the mass production of SiC power MOSFETs has for a long time been prevented by the presence of defects such as micropipes in the crystal structure. Some SiC devices with a structure similar to the one of a VD-MOSFET have already been produced, but their performance is still below the theoretical limit. The key problem is the slow turn-on of the MOSFETs, resulting in smaller than expected Drain currents. One more reliability issue is related to the Gate oxide, as a significant threshold voltage shift in the negative direction with a is observed when a negative bias is applied. That could change the MOSFET from a normally-off to a normally-on device [14, 17, 18].

3 State of the art: Radiation Effects on Electronics

Whenever a solid material is exposed to radiation its properties may be locally altered due to the energized particles depositing part of their energy in the body of the material. The type of interaction of radiation with matter is a rather complex and broad topic and depends on a variety of parameters, such as the mass, charge, and kinetic energy of the particle or the mass, charge, and density of the target material. This is the reason why the functionality of electronic systems is compromised when they are used in extreme radiation environments like the CERN accelerator complex or spacecrafts. Energized particles (i.e. protons, neutrons, heavy ions etc.) affect the operation of semiconductor electronics and lead to effects that can vary from a minor degradation of operating characteristics to even catastrophic failure.

3.1 Interactions between Radiation and Matter

When energetic particles interact with matter, they lose a part or all of their energy via different mechanisms. This topic is quite broad and complex, so only an overview of the most relevant mechanisms is following [19, 20, 21, 22, 23].

The first and most important mechanism is electronic stopping. It refers to the electromagnetic scattering of charged particles through elastic Coulomb collisions between the incident particles and the field of atomic electrons in the material. The result is the excitation of the target atom's electrons, known as direct ionization. The target nuclei remains at a fixed location because the energy transfer is smaller than the energy required to release it from the bond between the atom and its nearest neighboring atoms. Of course, the impacting particle will continue its path inside the target material until its energy is exhausted, thus creating a long ionizing track of electron-hole pairs (ehp).

One key parameter used to characterize the penetration of charged particles is the average energy loss per unit path length ($-dE/dx$), that is the stopping power or stopping force. A variation most commonly used is the mass stopping force, called linear energy transfer (LET) and is defined as *the metric for average energy deposited on the material per unit distance by the impinging particle*. LET is equal to:

$$LET = -\frac{1}{\rho}\frac{dE}{dx}, \tag{3.1}$$

where ρ is the density of the material and the LET unit is given in $MeV \cdot cm^2/mg$. The value of LET depends on both the nature of the particle and the density of the target material. A complete list of the LET values of all ions inside every target material is calculated by the Stopping and Range of Ions in Matter (SRIM) software developed by J. Ziegler [24]. Other Monte Carlo-based softwares, like FLUKA [25] or Geant4 [26], are also able to calculate the LET values.

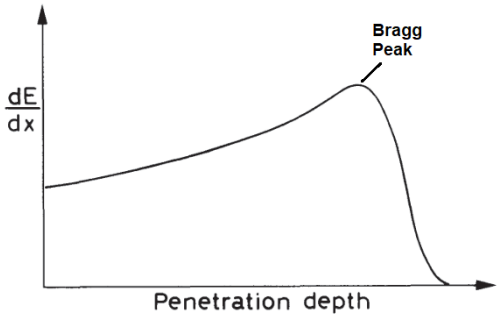


Fig. 3.1: A typical Bragg curve showing the variation of dE/dx as a function of the penetration depth of the particle in matter [19].

The typical shape of LET with respect to the ion track is depicted in Fig. 3.1. It basically shows the amount of ionization created by a heavy particle as function of its position along the slowing-down path. As it can be seen, most of the energy is deposited near the end of the trajectory, at a point called the "Bragg peak". It is clear that as a heavy particle slows down in matter and its kinetic energy is reduced, the rate of its energy loss increases.

On the other hand, when the penetrating particle interacts with the atom's nucleus, we have nuclear interactions, which take place mainly for protons and neutrons; they may also happen for heavy ions, even though it is considered negligible unless it is the end of the ion path. Nuclear interactions are divided into three main categories: elastic scattering, inelastic scattering, and transmutation.

In an elastic collision, the particle gives up a portion of its energy to an atom of the target material, and can dislodge the atom from its lattice position. This process will occur as long as the imparted energy is greater than that required for displacement ($\sim$25 eV for most materials). The displaced atom is referred to as the primary recoil and the recoiling nuclei along with other fragments transport through the semiconductor, losing energy along the way via stopping force. That way they cause the secondary (or indirect) ionization of the material.

During inelastic neutron or proton scattering, which implies the loss of kinetic energy, the impinging particle is captured by the nucleus of the target atom and then it is re-emitted at a lower energy. Consequently, the nucleus is left in an excited state and returns to its normal state by the emission of a gamma ray. Inelastic scattering can also cause the displacement of the target atom.

The transmutation reaction involves capture of the incident neutron or proton by the target nucleus and subsequent emission of another particle, such as a proton or an alpha particle. The remaining atom is thereby transmuted, i.e., converted from one element into another. The nature of reaction products depends on the target material and is relevant when studying the secondary events. For example, when a proton or a neutron impact on silicon, they can generate a variety of different ions, from hydrogen to phosphorus.

3.1.1 Useful Terminology

In order to study further and explain the effects of radiation on electronic components it is essential to introduce some fundamental definitions that will be regularly used from now on. These definitions are [19]:

- Absorbed Dose: Measures the total energy absorbed by the material per unit mass. Its unit of measurement is the *Gray* which is defined as:
  $1\ Gray\ (Gy) = 1\ Joule/kg$. A somewhat older unit for the absorbed dose, which is no longer actively used in Europe, is the *rad*, where $1\ rad = 0.01\ Gy$. It should be noted that the absorbed dose gives no indication of the rate at which the irradiation occurred nor the specific type of radiation.

- Range: Describes the distance a particle will travel in a material before it loses all of its energy. Depends on the type of the material (its density), the particle type and its energy. While it is not possible to calculate the range value, estimations can be made based on the particle's initial energy and its energy loss per unit length.

- Flux (ϕ): The rate of incident particles on a material measured in $[particles/cm^2/sec]$.

- Fluence (Φ): The time integral of flux over a specified period of time measured in $[particles/cm^2]$.

3.2 Overview of Radiation Effects on Electronics

Upon considering the various types of particles, particle energy ranges, and the variety of interactions that can occur, the situation might seem exceedingly complex in terms of effects produced in irradiated materials and devices. However, independently of the exact type of interactions that may take place, the effects of radiation on the behavior of electronic components or systems can be divided into two main categories: Cumulative and Stochastic effects.

Cumulative effects are gradual effects that take place during the whole lifetime of the electronics exposed in the radiation environment. In other words, the electronic device will exhibit failure only when the accumulated fluence has reached the device's tolerance limits. Cumulative effects can be manifested via two ways: Total Ionizing Dose Effects (analyzed in Subsection 3.2.1) and Displacement Damage Effects (analyzed in Subsection 3.2.2). On the other hand, Stochastic Events or Single Event Effects (SEE), as they are most commonly called, cause the perturbation of the behavior of electronic devices or systems because of the passing of a single ionizing particle. SEE will be presented in more detail in Subsection 3.2.3.

3.2.1 Total Ionizing Dose Effects

Total Ionizing Dose (TID) Effects are cumulative radiation effects that are caused by the ionization of insulating films used in modern IC technologies. Therefore, they affect both MOS devices, due to the thin silicon dioxide films employed in these technologies, and bipolar devices as well, due to the presence of field and passive oxides. However, the following analysis of the degradation caused by TID will focus on the SiO_2 layer of MOS structures. In summary, ionizing radiation passing through the gate SiO_2 films can *(i)* lead to the buildup of positive charge in the oxide layer, *(ii)* produce electronic states at the $Si - SiO_2$ interface, and *(iii)* create electron traps in the oxide. These effects are manifested as a shift of the threshold voltage and a degradation of the channel's mobility.

For better understanding the evolution of TID events, let's consider a n-channel MOS device whose Gate is positively biased. Thus, an electric field is created along the Gate oxide and an inversion layer of minority carriers (electrons) is formed below the $Si - SiO_2$ interface. The time-dependant response of such a device to radiation can be organized in four major processes along with the help of Fig. 3.2. These processes can be summarised as:

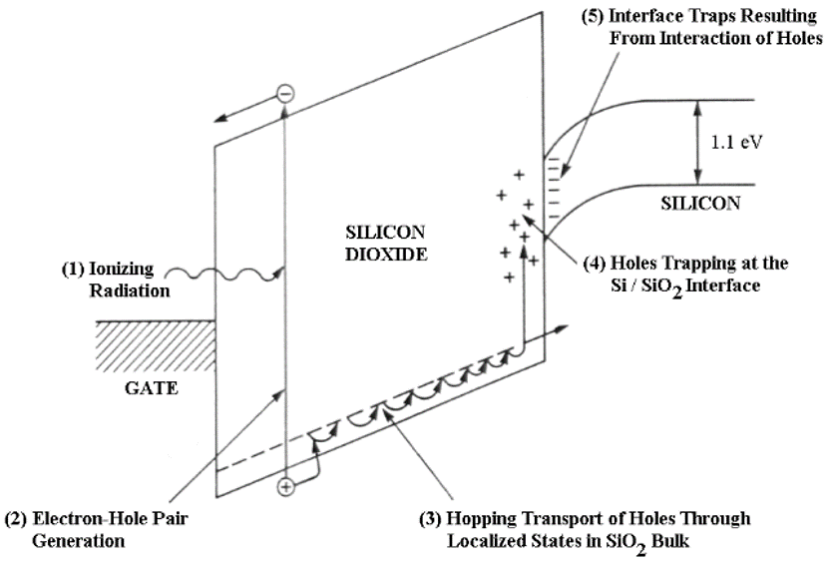


Fig. 3.2: Schematic energy band diagram of SiO_2 MOS structure for positive gate bias, indicating major physical processes underlying radiation response [21].

1. The impinging radiation causes the creation of electron-hole pairs in SiO_2. Some of them are recombined almost immediately, but due to the existing electric field most of the electrons are swept out of the oxide and collected by the Gate electrode in a matter of picoseconds. However, as holes have lower mobility than electrons, they appear as relatively immobile. Because of their accumulation, a smaller Gate voltage is required to create an inversion layer of electrons, and thus the threshold voltage undergoes a negative shift.

2. Holes start to slowly transport through the oxide, towards the $Si - SiO_2$ interface. This stochastic, hopping transport of the holes can go on for a period of few microseconds up to seconds depending on the temperature, the applied field and the oxide thickness.

3. Eventually, holes reach the interface and some of them are collected by the body of the Si. However, a percentage of them is captured in deep, long-living trap states. These trapped holes cause a remnant negative voltage shift, which can persist for hours or even years. But even these stable trapped holes undergo a gradual annealing, which is enhanced with increased temperature.

4. The fourth major component of MOS radiation response is the radiation-induced buildup of interface traps right at the $Si - SiO_2$ interface. These traps are localized states with energy levels in the Si band-gap and it is observed that they are negatively charged. Interface traps are highly dependent on oxide processing, and other variables, such as the applied field and temperature.

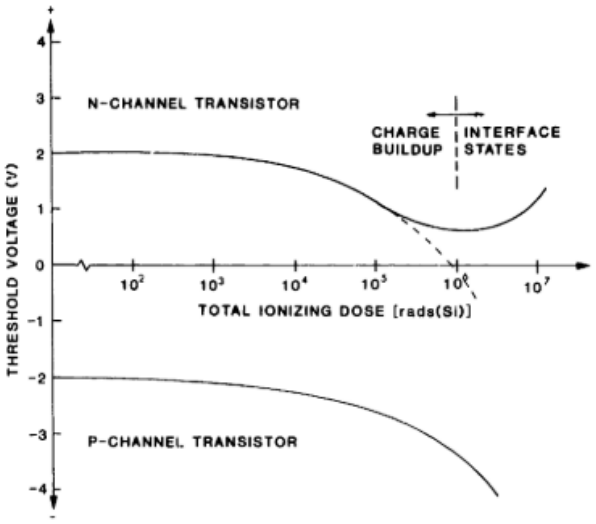


Fig. 3.3: Illustration of the effect of positive charge buildup and interface state production on the threshold voltage in irradiated n- and p- channel MOS transistors [20].

As to what regards the effects of TID on the behavior of MOS devices, it is clear that the threshold voltage is majorly affected. This is also illustrated in Fig. 3.3 for both n-channel and p-channel MOS transistors. In the p-channel case, the buildup of positive charge in the gate oxide requires a higher voltage to be applied on the Gate in order to create an inversion layer, and thus the absolute value of the threshold voltage is increased. On the other hand, in the n-channel case, the buildup of positive charge makes it easier to create an inversion layer of electrons, resulting in a lower threshold voltage value as the radiation dose is increased. Interestingly, at doses higher than 10^6 rad (10^4 Gy), a turn-around in the curve is possible, due to the formation of negatively charged interface states which compensate for for a portion of of the built-up positive charge. The exact dose at which this effect occurs is highly dependant on the manufacturing process. The dashed line in Fig. 3.3, indicates the case the voltage turn-around does not take place early enough, and the device is goes from enhancement-mode to depletion-mode.

Lastly, the mobility of the channel is also degraded due to TID, even though these effect becomes relevant for relatively high ionizing doses ($> 10^5$ Gy) and is more severe for wet-grown hardened oxides (typically field oxides) rather than dry-grown ones (typically gate oxides). The mobility degradation is caused by the presence of both trapped oxide charge near the $Si - SiO_2$ interface and interface states, which lead to the additional scattering of the carriers when transported along the channel [20, 21, 27].

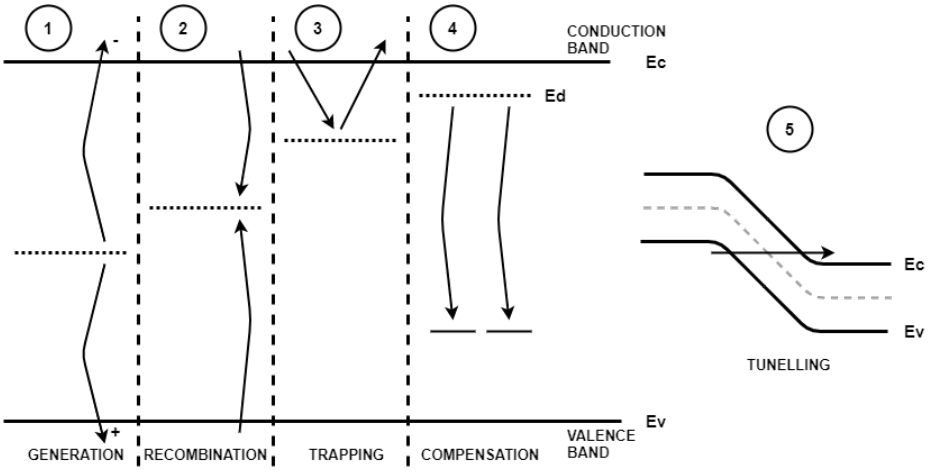


Fig. 3.4: Illustration of five effects that can occur due to the presence of defect centers in the silicon bandgap [20].

3.2.2 Displacement Damage Effects

Displacement Damage (DD) effects are also cumulative radiation effects that are related to dislodging atoms from their normal lattice position when energetic particles pass through a material. Even though both neutrons and energetic particles can cause displacement damage, the effects of neutrons are more important, as they do not interact directly with the electrons in the target material, and only lose energy through nuclear interactions. This is the reason why particle fluence is often expressed in terms of an equivalent $1MeV$ neutron fluence, which is that fluence of $1MeV$ neutrons that would produce the same electronic effect as the irradiation conditions used in a particular study. Of course, after the displacement of an atom, both the recoiling atom and the scattered primary particle, will keep losing energy in the material, resulting in a cascade of displaced secondary atoms and/or the ionization of the material. Displacement damage affects mainly the silicon body of bipolar and MOS devices. However, effects on MOS devices only become significant for fluences of $10^{15}n/cm^2$ or even higher levels. For bipolar devices DD effects are mainly manifested as a degradation of the gain and the lifetime of a transistor because of the mechanisms described next.

A minimum energy of $25eV$ transferred to the nucleus of an atom is enough to cause the displacement of the atom. The absence of the atom from its normal lattice site is called a "vacancy", while the displaced atom finally stops in a non-lattice position, called an "interstitial". Regions containing large numbers of relatively closely spaced defects can also occur, and such grouping is termed a defect cluster. This kind of disturbance of the lattice periodicity gives increase to new energy levels in the bandgap, altering significantly the electrical properties of the device. The effects

that can occur due to the presence of radiation-induced defect centers in the silicon bandgap are illustrated in Fig. 3.4 and are summarized as:

1. Generation of electron-hole pairs through a level near the midgap. Introduction of such centers is the mechanism for leakage current increases in Si devices.

2. Recombination of electron-hole pairs, where the defect captures a carrier of one polarity, followed by a second capture of the opposite polarity. These recombination centers reduce the lifetime of minority carriers, which is the dominant mechanism for gain degradation in bipolar transistors.

3. Temporary trapping of carriers at a typically shallow level, increasing the transfer inefficiency in charge-coupled devices.

4. Compensation of donors or acceptors by radiation-induced centers. This process is called carrier removal, because it reduces the majority carrier concentration. A possible effect on the electric characteristics of a bipolar device is the increase of its internal resistance.

5. Tunneling of carriers through a potential barrier by means of defect levels. This defect assisted (or trap assisted) tunneling process can cause device currents to increase.

3.2.3 Single Event Effects

Single Event Effects (SEE) are stochastic effects that cause the perturbation of the behavior of electronic devices, circuits and/or electronic systems because of the passing of a single energetic particle.

In more detail, as the particle passes through the material, it deposits part or all of its energy through direct or indirect ionization, and a column of electron-hole pairs (ehp) is created along its track. The energy deposited in the material is related to the LET of the particle, as it was already described in Subsection 3.1. SEEs are usually generated in reverse-biased p-n junctions of the devices, where, due to the existing electric field, ehp avoid recombination and start moving in opposite directions. The carrier collection process relies on the well-known carrier transfer processes, i.e. drift and diffusion, but special attention should be paid to the deformation of the electrostatic potential, often called "field funneling" [21]. Eventually, ehp are collected into circuit nodes in the form of transient currents and may trigger already existing failure mechanisms. Depending on a variety of parameters, related both to the technology of the device and the irradiation conditions as well, errors caused

by SEE can be distinguished in soft (non-destructive) ones, which can be reset by applying correct signals to the device, and hard (destructive) ones. Hard errors are usually related to increased currents flowing through the device, which may be sufficient for metal traces to vaporize, bond wires to fuse open, and silicon regions to be melted due to thermal runaway.

In summary, the most commonly observed SEEs are [28, 29, 30, 31]:

- Soft (Non-Destructive) SEEs:
  - Single Event Upsets (SEUs): Single particle induced bit flip in digital storage elements such as memories and flip-flops. The collected charge from the energy deposition changes the amount of charge stored on the nodes (capacitors) of the storage element, leading to a logic state different from the original. This event induces no damage to the basic element which can be re-written with the right value.
  - Multiple Cell Upset (MCU) and Multiple Bit Upset (MBU): It is possible that a single particle lead to multiple upsets in a digital storage element. The responsible mechanism is the lateral diffusion of the charge deposited by radiation, and its collection in sensitive volumes around the strike location. Multiple Cell Upsets (MCUs) occur when two or more bits (physically adjacent or not) become corrupted. If these bits are also in the same logical word, the effect is known as Multiple Bit Upset (MBU). The latter mechanism is considered more hazardous, because even though memories are often protected from errors with an error-correction code (ECC), this protection no longer works properly when the number of errors in the same word exceeds the maximum number that the code can detect and collect.
  - Single Event Transient (SET): A short term voltage spike, originally formed by the electric field separation of the charge generated by a particle passing through or near a circuit junction. The voltage pulse may propagate in analog, digital or mixed-signal circuitry, competing with the legitimate signal flow. Since the propagating pulse is not technically a change of "state", one should differentiate between SET and SEU.
- Hard (Destructive) SEEs:
  - Single Event Latchup (SEL): It is a potentially catastrophic condition which affects multi-layered pnpn devices such as the thyristor or CMOS

IC technologies. The simplest model for SEL is the two transistor model, where two BJTs are interconnected such that the collector current of each BJT feeds the base current of the other. In such structure, an increase in pnp collector current gives an increase in the npn base current. This in turn increases the the collector current of the npn, which gives an increase in the pnp base current. This positive feedback is such that, if the overall gain of the thyristor pnpn is high enough, any perturbation (for instance, an ionizing particle strike) turning on one of the parasitic BJT structures can trigger latchup. This way, a low resistance path develops between power supply and ground of a device, that remains after the triggering event is removed. Once latched, the high current condition will continue until power is removed from the device or it fails catastrophically. The use of a current monitoring and a power control circuit allows the power to be shut down quickly after the latchup is detected in order to protect the device against thermal destruction.

- Single Event Burnout (SEB): A failure mechanism observed in power bipolar transistors and MOSFETs. These devices are sensitive to SEBs in their OFF-state. In that case, the device is blocking a high drain-source (collector-emitter) voltage. The passage of an ionizing particle induces a current transient, turning on the parasitic bipolar structure in the MOSFET or the main transistor in the BJT. At that point, a regenerative feedback mechanism might set in, and the current increases until second breakdown and finally permanent device destruction. A key component of the regenerative feedback is the avalanche-generated current in the collector region of the parasitic (or main) BJT.

- Single Event Gate Rupture (SEGR): A failure mechanism caused by the passage of heavy ions through the neck region of power MOSFETs, which creates a conducting path in the gate oxide, when the device is in the OFF-state. The charges created by the heavy ion crossing the semiconductor are collected and propagate up to the insulator interface making the electric field across the dielectric dangerously large. If it exceeds a critical value, a localized gate rupture may occur. Once the rupture is initiated, current flow through the gate oxide to the polysilicon of the gate results in a thermal runaway condition, locally melting the silicon, dielectric and polysilicon.

Because the experimental results presented in Chapter 6 concern specifically SEB and SEGR events in commercial Silicon power MOSFETs, a further description of their mechanism and dependencies will be provided in sections 3.3 and 3.4 respectively.

3.3 Single Event Burnout in power MOSFETs

The mechanism related to Single Event Burnouts (SEBs) was first introduced in 1985 by T. Wrobel *et. al.* in [32], where they observed that the avalanche breakdown of a VD-MOSFET structure could be initiated at bias levels far below the rated breakdown voltage of the device and they introduced the term of "Current Induced Avalanche (CIA)". The term SEB was introduced a year later by Waskiewicz *et.al.* in [33], where they presented the first experimental results of irradiation with Californium-252. Since then, extensive work has be done to understand the mechanism of SEB, explain its dependencies and create accurate models. The most relevant for this thesis findings will be summarised in this Section.

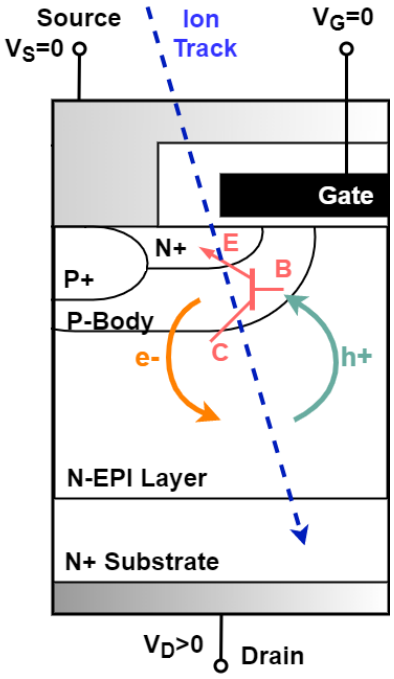


Fig. 3.5: Cross-sectional layout a VD-MOSFET during a SEB event. The parasitic bipolar junction transistor (BJT) inherent to the VD-MOSFET has the N+ Source as its Emitter, the P-body as its Base, and the N-Epi Layer as its Collector.

The basic mechanism of SEB is illustrated in Fig. 3.5, in which an n-type power MOSFET is assumed to be struck by a single radiation particle while it is kept in the OFF state. The figure also includes the parasitic BJT of the device, which is supposed to be kept turned-off by short-circuiting its Base (P-Body of the MOSFET) with its Emitter (N+ Source of the MOSFET) through the Source metallization. When the MOSFET is struck by the particle, the electrons and holes generated are collected into the Drain and Body terminals, respectively. Due to the inherent resistance of the Body region (R_B) and the hole current flowing through it, it is possible that the voltage drop between the Base and the Emitter becomes larger than 0.7

V (the built-in potential) and therefore the BJT is turned-on. This way, a further injection of electrons in the N-EPI Layer is caused. The electrons injected into this region may create ehps through the impact ionisation process while moving towards the Drain terminal. The resultant holes move to the Base region, and a feedback loop is established. If the loop is regenerative, the current will increase rapidly until a permanent short is created between the Source and the Drain of the device. Otherwise, the current die out with no lasting damage to the device. Whether the feedback loop is regenerative depends on a variety of parameters, such as the bias of the device, the radiation features, the gain of the BJT, the value of R_B, and the avalanche multiplication in the N-EPI Layer [34].

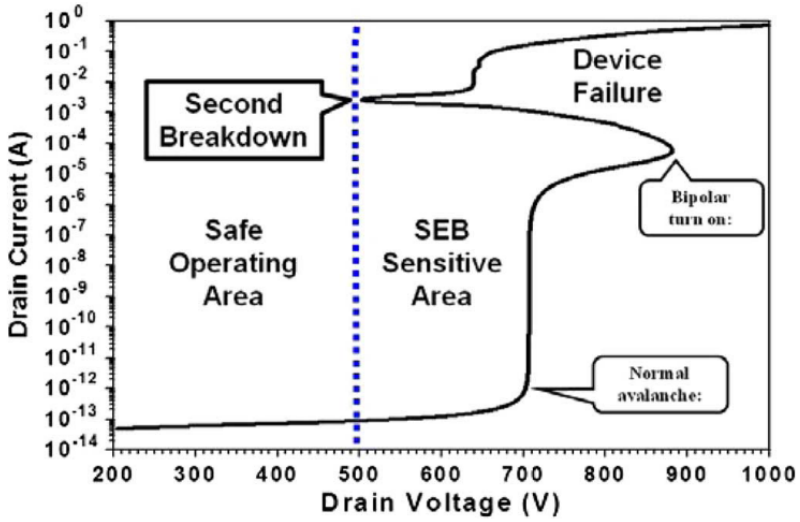


Fig. 3.6: Quasi-stationary avalanche curve from TCAD simulations of a VD-MOSFET. Depiction of the transition from its normal off-state operation into avalanche breakdown, into bipolar turn-on, and finally into second breakdown [35].

The mechanism can be further understood through the work of Liu *et. al.* in [36] and Fig. 3.6, which depicts a pictorial illustration of a MOSFET current-voltage characteristic at different stages of breakdown, simulated under quasi-stationary conditions. Without the effect of ionising radiation, the parasitic BJT can be turned-on as soon as the Drain voltage is increased beyond a certain point, i.e. the breakdown voltage where the avalanche phenomenon is initiated (aprox. 700V in this example). After that point, the device rapidly reaches the current-voltage condition that triggers second breakdown and causes catastrophic failure. Second breakdown refers to sudden decrease in the MOSFET's blocking voltage capability with an uncontrolled increase in the current. Now, under the effect of ionising radiation, the device can experience a SEB as soon as it is biased at a voltage higher than the required one for a second breakdown (approx. 500 V in the example) and the energy deposition from a particle is such that the transient current is high enough to turn-on the BJT.

There are two interesting points that arise from this simulation. The first point is that it proves that the ionising radiation only triggers an already existing failure mechanism in a power MOSFET, which is related to the existence of the parasitic BJT. The second point is that a voltage threshold is defined, the SEB threshold voltage ($V_{th|SEB}$), which distinguishes the Safe Operating Area from the SEB Sensitive Area. If $V_{th|SEB}$ is known and a device is biased at a lower value, it can be assumed that it will be SEB resistant. However, calculating $V_{th|SEB}$ through the above mentioned simulations is usually not possible, as an extensive knowledge of the device's technology (thickness and doping profiles of the various layers) is required. So instead, it is approximated experimentally by exposing the device of interest to different irradiation conditions.

The first analytical model to study the effect of the device's parameters was developed in 1987 by Hohl and Galloway in [37], where they concluded that the electric field inside the lightly doped Epitaxial region was the main contributor to SEB sensitivity. Two years later, Hohl and Johnson explored the changes in the electric field density during a SEB event. According to them, the electric field peak is initially located at the Base-Collector interface, but shifts towards the Epitaxial layer-Substrate homojunction as the event progresses. This shift of the electric field is followed by a rapid increase in holes generation at the same location, contributing to the self-sustained avalanche [34]. As to what regards the most sensitive area of a device, it was proved by Dachs *et. al.* in 1994 through 2D Medici simulations [38], that a power MOSFET is the most susceptible to SEBs when the particle passes through the neck and channel regions furthest from the Body contact [39].

The next step in the research community was to investigate the radiation characteristics and conditions that affect the SEB sensitivity of a device, with heavy ions being the main interest, as they were the major concern for space applications (cosmic rays, etc.). Stassinopoulos *et. al.* showed that the critical parameter for a burnout is the charge distribution along the track as well as the collected charge in the Epi Layer, rather than the surface LET of the ion used [40]. So, in contrast to surface LET, the average LET in the Epi region, which is strongly related to the ionized charge, is a more accurate term to describe the SEB sensitivity. A simple explanation is that the higher the ionized charge, the higher the transient currents in the device will be and thus the parasitic BJT will turn on for lower Drain voltages. However, recent tests performed by Liu *et. al.* suggest that there is an even better correlation between the SEB failure voltage and the atomic number Z of an ion, with heavier ions being more dangerous for power MOSFETs [41]. Another recent study by Luu *et.al.* focused on the influence of the ion's range and noticed that there was a higher sensitivity to SEBs when the range of the ionizing track passed through the entire epitaxial layer [42]. Apart from heavy ions, both protons [43] and neutrons [44] can generate SEBs, mainly through indirect ionization mechanisms, as described in Sec. 3.1. Lastly, the

operating temperature of the device should also be taken into consideration when studying its SEB susceptibility. Specifically, when the temperature is increased, the impact ionization rate decreases, causing a reduced hole current flow into the base region. This way, the device becomes less prone to SEBs [45].

As to what regards the protection of power MOSFETs from SEBs, there have been proposed several design processes and operation techniques that may decrease the SEB susceptibility of a device. Apparently, derating a power MOSFET and keeping it biased to a safe Drain voltage, much lower than the Rated one, is a first approach to protecting it from SEBs. Early studies postulated that operating a MOSFET in dynamic mode could make it less sensitive to burnouts [46], event though later work showed that the sensitivity does not depend on the static or dynamic mode of operation [47]. In terms of technology, p-channel MOSFETs seem to be completely immune to SEBs due to the lower impact ionization coefficient of holes compared to electrons [32]. Additionally, the introduction of a p+ plug (as described in Sec. 2.4.3) acts to reduce the Base resistance of the BJT, making it less easy to turn on. A more recent approach to reduce SEB vulnerability is the inclusion of a buffer layer between the Epitaxial layer and the Substrate, as it changes the electric field distribution and lowers the maximum electric field [48]. Of course, this comes with a cost at the on-resistance of the device. Lastly, the STRIPFET configuration outweighs the HEXFET one when considering their SEB sensitivity. In the cell structure (HEXFET), if the source terminal is poorly contacted, it becomes much more likely that the parasitic BJT turns on during an avalanche breakdown event. On the other hand, the planar stripe structure (STRIPFET) reduces, almost eliminates, the likelihood for this to happen [49].

3.4 Single Event Gate Rupture

Single Event Gate Rupture (SEGR) describes the condition where Gate oxide fails under the neck region (the region between body diffusions) of a power MOSFET due to the passage of an energetic heavy ion. The phenomenon takes place when the device is in the OFF state, with positive bias being applied on the Drain, and negative or zero bias being applied on the Gate node. Even though the underlying mechanism is still not completely understood today [35], two are the main physical responses that are considered responsible: the epitaxial response and the oxide response.

For the first response, the epitaxial layer, which supports high electric fields within the device, is the main interest. During the OFF-state, a depletion layer is formed in the Epi layer, preventing the the high Drain voltage from reaching the dielectric interface. When a heavy ion passes through the device, ehps are created along its

track, with the holes being pooled at the $Si - SiO_2$ interface and the electrons being swept down into the Drain substrate, as shown in Fig. 3.7. The result is that the heavy ion track acts as a resistive short and a portion of the Drain potential (referred to as $V_{COUPLED}$) is coupled to the Epi layer-dielectric interface. $V_{COUPLED}$ induces an electric field across the dielectric, which is added to the already existing field caused by the applied V_{GS} [50, 35].

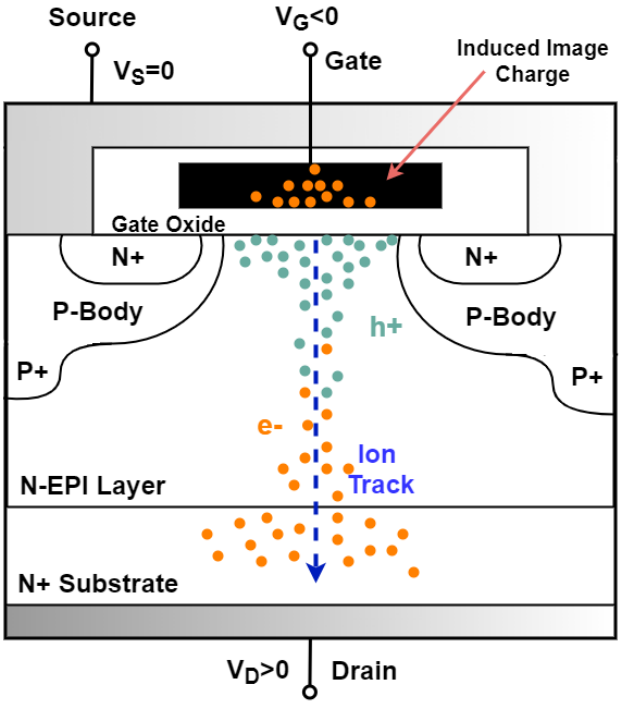


Fig. 3.7: Cross-sectional layout a VD-MOSFET during a SEGR event.

The oxide response focuses on the lowering of the electric field required to cause the breakdown of the oxide. This is caused by the ionized charge trapped in the oxide and the new lower voltage (V_{CRIT}) that can be sustained by the dielectric is well described by the Titus-Wheatley equation [51]:

$$V_{CRIT} = \frac{(E_{BD})(T_{OX})}{1 + \frac{Z}{44}}, \tag{3.2}$$

where E_{BD} is the intrinsic dielectric breakdown field $[V/cm^2]$, T_{OX} is the dielectric thickness $[cm^2]$, and Z is the atomic number of the heavy ion. Interestingly, the oxide SEGR response depends only on the type of the ion rather than its LET or energy. If the oxide finally breaks down, the collected holes discharge through oxide, heating the structure locally. When the breakdown lasts long enough, a permanent short-circuit through the oxide is created.

As it is expected, SEGR sensitivity depends on a variety of parameters, related both to the device's technology and to the irradiation conditions. Early studies compared the SEGR response of p-channel and n-channel power MOSFETs and found out that the type of majority carriers in the channel did not really affect the device' sensitivity under similar irradiation conditions [52]. On the other hand, the oxide thickness seems to play a major role in the susceptibility of a device to Gate Rupture. Specifically, there is discrimination between thin Gate oxides (<30 nm) and thicker ones (>30 nm). For the former case, thin oxides appear less susceptible to SEGR due to increased dielectric strength, with the oxide defects and trapped charges being of significant importance. For the latter case, it has been shown that V_{CRIT} scales proportionally with the dielectric thickness, with the quality of the oxide having little impact to the SEGR response [35]. Considering now the SEGR dependence on the device's bias and the ionLET, a quite enlightening plot was published by Wheatley *et. al.* in 1994, shown in Fig. 3.8 [53]. In more detail, the plot correlates the SEGR failure Drain voltage ($V_{th|SEGR,D}$) with the SEGR failure Gate voltage ($V_{th|SEGR,G}$) and the atomic number (Z) of the passing heavy ion (or the ion's LET).

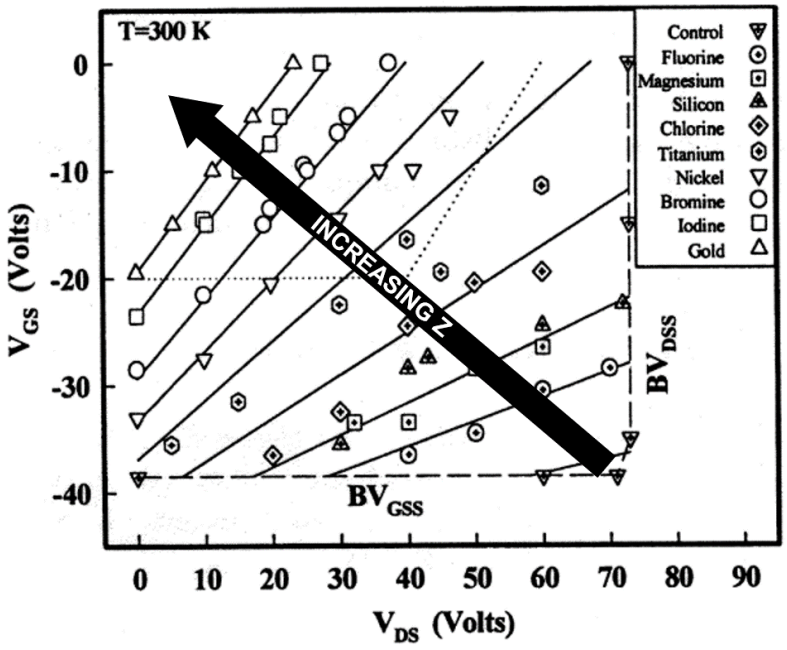


Fig. 3.8: Dependence of SEGR on Gate and Drain bias voltages and ion LET (or ion's atomic number) [53].

It is observed that by increasing the applied Drain bias, $V_{th|SEGR,G}$ decreases linearly for a given ion and LET. It can be also noted that with increasing LET or heavier ions, the curves move up and to the left, an indication that SEGR occurs for lower values of $V_{th|SEGR,G}$ and $V_{th|SEGR,D}$. Lastly, recent studies show that SEGR can be

produced both by high-energy (1 GeV) protons [54] and by accelerated neutrons [55], as well.

4 Experimental Methodology

4.1 Non-Destructive approach for testing SEBs

One drawback of SEE testing on power MOSFETs is that the Device Under Test (DUT) is completely destroyed during the test, and must consequently be replaced after it. This time consuming intervention reduces the available beam-time at the irradiation facilities, other than adding a further level of uncertainty in data treatment, because of the part-to-part variability. It also increases the cost of the test campaign and the time dedicated to preparation, especially if the samples have to undergo specific procedures (like decapsulation) before they are irradiated. For this reason it is extremely useful to have options for non destructive test procedures, like the "current-limiting" method proposed for SEB testing in 1987 by Oberg and Wert [56]. This method is based on the placement of a current-limiting load resistor between the Drain voltage source and the Drain node of the DUT as seen in Fig. 4.1a. This way, it is possible for a single device to undergo multiple SEBs, by making sure that the high currents leading to its destruction would be limited. As a result, Oberg and Wert were able to study the shape of a non destructive SEB-induced current pulse for the first time, noticing that the level of the current registered could not be supplied through the 1 $k\Omega$ load resistor that they used for their experiment. Their conclusion was that the pulses saved were due to the discharge of the parasitic capacitance of the power MOSFET itself, which, however, was not high enough to cause the failure of the device. They also introduced an informal proof that a nondestructive current pulse would be registered if and only if an actual burnout was initiated.

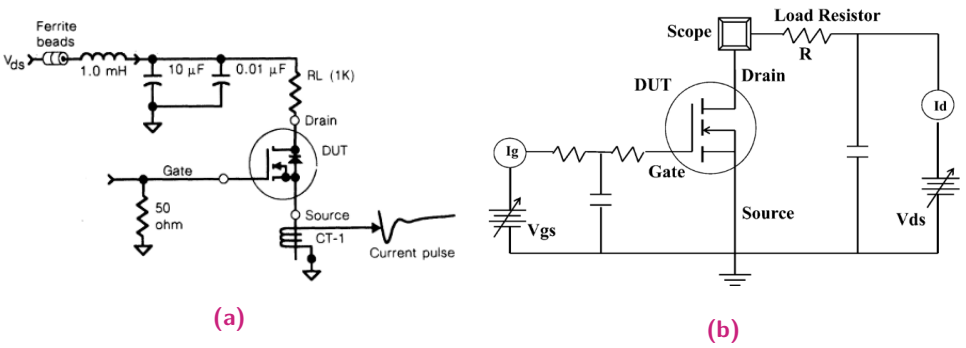


Fig. 4.1: Schematic of the non destructive circuitry for SEB testing used by *(a)* Oberg and Wert in [56] and *(b)* Liu *et. al.* in [57].

However, despite this protective approach being soon adopted in the SEB testing community, the effect of the load resistor, added in series with the Drain node, was not evaluated until 2012 by S. Liu *et al.* in [57]. In more detail, by using the circuit seen in Fig. 4.1b, they explained the fundamentals of the protective mechanism and studied its effect on the experimental results.

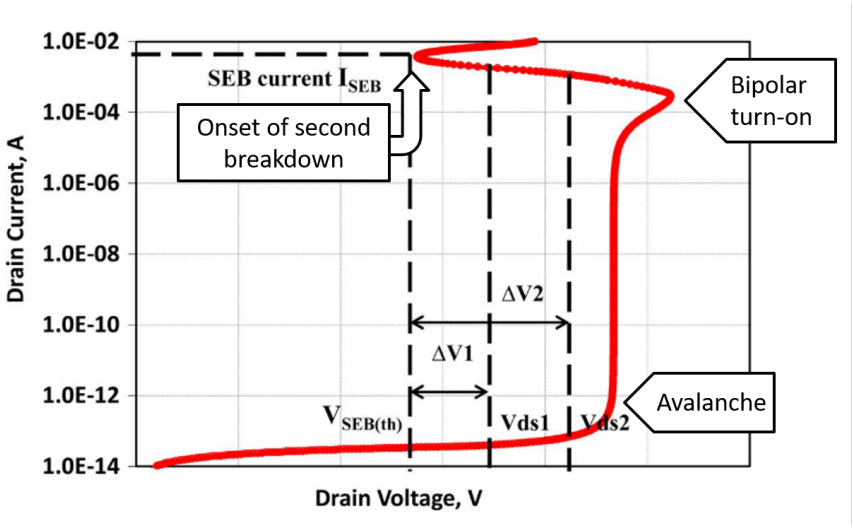


Fig. 4.2: Quasi-Stationary Avalanche Simulation of a power MOSFET.

In order to evaluate the required resistance to protect a power MOSFET, let's consider the circuit of Fig. 4.1b where a load resistor R is placed between the voltage source and the Drain. The device is susceptible to SEBs when the voltage applied on its Drain node (V_{DS}) is higher than the SEB threshold voltage ($V_{SEB|th}$), as explained in Sec.3.3. When an ionizing particle causes the BJT to turn on, a transient current I_T is flowing through the DUT, reducing its effective resistance and making it comparable to the value of R. Therefore, the protection mechanism is based on a voltage divider created between the DUT's resistance and the load resistor R. Assuming that I_T is smaller than the Burnout current (see I_{SEB} in Fig. 4.2), the DUT is protected if the voltage drop on R is sufficient to reduce the voltage on the DUT below $V_{SEB|th}$. If not, a higher value of R should be selected to guarantee the protection of the device. This approach is described by equation 4.1 and underlines that selecting the proper value of R requires the estimation of $V_{SEB|th}$ and I_{SEB} through destructive SEB tests.

$$I_T - (V_{ds} - V_{SEB|th})/R < I_{SEB} \tag{4.1}$$

It should also be mentioned that although a high-value resistor will surely provide effective protection against SEB, an extremely high load resistance may yield false counting of SEB events during the SEB cross section evaluation. It was considered in

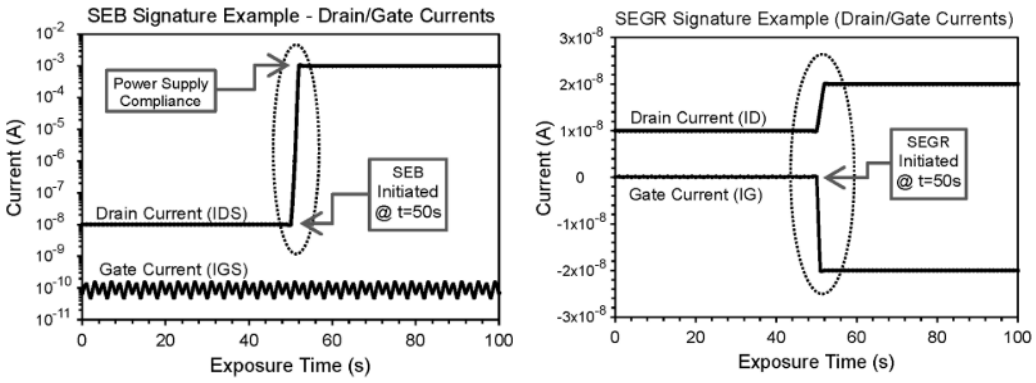
Liu's study that a SEB occurred when the voltage at the device's Drain dropped to 80% of the total applied voltage. Then, they considered the case such a voltage drop was registered when using a very high resistor (i.e. higher than 500 $k\Omega$). However, they noticed, that under these circumstances and based on Eq. 4.1, I_T was calculated to be much smaller than the minimum current to turn-on the BJT (I_{BJT} in Fig. 4.2). Thus, it was concluded that the registered voltage drop could not be attributed to a SEB, despite the initial consideration. For Liu's set of experiments a resistor of just 1 $k\Omega$ was proven to provide the needed protection against destructive SEBs.

As to what regards SEGR, there is not a documented method or circumvention circuit up-to-date that can protect a power MOSFET from the destructive effects of Gate Rupture once the phenomenon has been triggered.

4.2 General Approach for SEE Irradiation Tests

The experimental approach for evaluating the SEE sensitivity of commercial Si Power MOSFETs in the framework of the R2E project's activities, was based on a Test Method Standard published in 2013 [58]. The fundamental concepts of this approach will be briefly described here, so that the sections following will be put in a broader perspective.

Multiple power MOSFET devices, attached on a test board like the one in Fig. 4.1b and biased in their off-state, are exposed to varied irradiation conditions and their sensitivity to SEBs and SEGRs is evaluated simultaneously. The test board is a mounting interface between the test instrumentation and the DUTs. It enables the application of V_{DS} and V_{GS} on the DUTs, as well as the monitoring of I_{DS} and I_{GS}. As explained in section 4.1, despite being able to protect the DUTs from SEB-caused failure, the circumvention circuit can not prevent the MOSFET's destruction from SEGR. As a result, multiple SEBs can be registered for one DUT, while on the other hand, a DUT is unusable after a single SEGR. Non-Destructive SEBs are registered and counted by an oscilloscope connected to the Drain node of the device. The oscilloscope is triggered by the SEB-induced voltage drop on its input. Still, the circumvention circuit can not guarantee the protection of every power MOSFET reference against destructive SEBs for all circumstances. The way to distinguish a destructive SEB from a SEGR is illustrated in Fig. 4.3. During the SEB response, I_{DS} is increased by several orders of magnitude, passing from a level of μA to mA or even more, while I_{GS} remains relatively constant. On the other hand, during the SEGR response, both I_{DS} and I_{GS} show a similar, but not as high, increase.



(a) (b)

Fig. 4.3: *(a)* A typical Drain and Gate current response during a destructive SEB in comparison to *(b)* a typical Drain and Gate response during SEGR [35].

As to what regards SEB testing, the first relevant parameter obtained is the SEB threshold voltage ($V_{SEB|th}$), i.e. the minimum voltage that must be applied on the Drain node of the DUT to become SEB-sensitive. For its estimation, the DUTs are initially biased at a relatively safe V_{DS} and are exposed to radiation until a predefined fluence is accumulated. If no events are registered at the end of the experimental run, the bias is slightly increased and the DUTs are irradiated again to the specified fluence level. This process is repeated until the first SEB occurrence, provided that V_{DS} remains smaller than or equal to the rated voltage of the device (V_{RATED}). Thus, $V_{SEB|th}$ is set equal to the applied V_{DS} when the first SEB is registered. Otherwise, if no events are registered for all voltage steps, the DUT is considered SEB-tolerant if and only if the required level of fluence was reached for each step.

Calculating the DUT's SEB cross-section is also important for the characterization of the SEB sensitivity of a power MOSFET. The cross-section, measured in $[cm^2]$, represents the sensitive die area of a device and is expressed as the ratio of the number of events to the total particle fluence (Φ). In case multiple DUTs are tested simultaneously and the number of SEBs is referring to the events that took place in all of them cumulatively, the value of the cross-section is normalized by dividing it with the number of DUTs tested, as described by Eq. 4.2. Additionally, when during a run, less than 50 SEBs are counted, the upper and lower limits of the cross-section are calculated based on a Poisson distribution with 95% confidence level [59]. The deviation of the counted SEBs is calculated based on the values in Tab. 4.1.

$$\sigma = \frac{\#_{SEBs}}{\Phi \cdot \#_{DUTs}} \left[cm^2\right] \tag{4.2}$$

N	95% Limits lower	upper
0	0.0	3.7
1	0.1	5.6
2	0.2	7.2
3	0.6	8.8
4	1.0	10.2
5	1.6	11.7
6	2.2	13.1
7	2.8	14.4
8	3.4	15.8
9	4.0	17.1
10	4.7	18.4
11	5.4	19.7
12	6.2	21.0
13	6.9	22.3
14	7.7	23.5
15	8.4	24.8
16	9.4	26.0

N	95% Limits lower	upper
17	9.9	27.2
18	10.7	28.4
19	11.5	29.6
20	12.2	30.8
21	13.0	32.0
22	13.8	33.2
23	14.6	34.4
24	15.4	35.6
25	16.2	36.8
26	17.0	38.0
27	17.8	39.2
28	18.6	40.4
29	19.4	41.6
30	20.2	42.8
31	21.0	44.0
32	21.8	45.1
33	22.7	46.3

N	95% Limits lower	upper
34	23.5	47.5
35	24.3	48.7
36	25.1	49.8
37	26.0	51.0
38	26.8	52.2
39	27.7	53.3
40	28.6	54.5
41	29.4	55.6
42	30.3	56.8
43	31.1	57.9
44	32.0	59.0
45	32.8	60.2
46	33.6	61.3
47	34.5	62.5
48	35.3	63.6
49	36.1	64.8
50	37.0	65.9

Tab. 4.1: Poisson distribution margin limits with 95% of confidence margin.

As to what regards SEGR testing, the process for the estimation of $V_{th|SEGR}$ is exactly the same as the one described above for SEBs. Since a power MOSFET is destroyed once a SEGR has been triggered, it is not possible to get a statistically accurate value of its cross-section, unless a significant number of components is tested and destroyed. However, in some cases it might by useful to express the sensitivity of a DUT to Gate Rupture in terms of the fluence accumulated (Fluence-To-Failure or FTF) or time passed (Time-To-Failure or TTF) until the destructive event took place.

Lastly, by performing the same test on the same power MOSFET reference under different irradiation conditions it is possible to identify patterns for the dependence of the cross section and $V_{SEB|th}$ on parameters like the type of ionizing particle, energy, LET, etc. Alternatively, by exposing different power MOSFET references to the same irradiation conditions it is aspired to identify potential technology trends that are related to the SEE sensitivity.

4.3 Test Board Design

The first version of the Test Board (Board 1) for evaluating the SEE response of Si power MOSFETs features the circuit depicted in Fig. 4.4 and was based on the circuit used by Oser *et al.* in [60]. The protective mechanism introduced in Section 4.1 is employed in this case, as well. During irradiation, fixed voltage bias (V_{DS}) is applied at the MOSFET's Drain, while the Gate and the Source are grounded to keep the DUT in the OFF state. When, under the occurrence of a SEB, the parasitic

bipolar transistor is turned ON, the protection circuit intervenes to prevent the power MOSFET from entering a secondary breakdown.

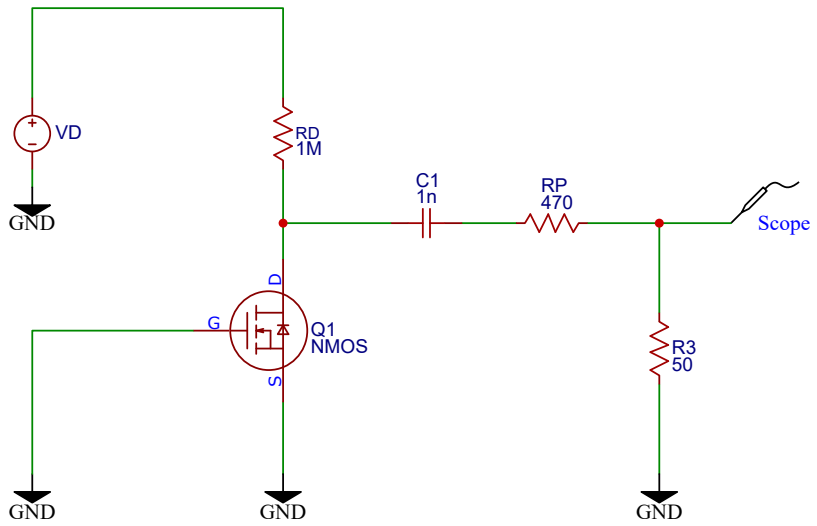


Fig. 4.4: Schematic of Board 1, the first version of the circuit used to evaluate SEE on power MOSFETs.

As explained in 4.1, resistor R_D protects the MOSFET by limiting the drain current and performing a de-rating on the Drain-Source voltage during the occurrence of a SEB. Its value should be selected for each power MOSFET reference separately, in order to shift the V_{DS} below $V_{SEB|th}$ and guarantee that I_T would be smaller than I_{SEB} (see 4.1). However, since no information were available for the power MOSFETs tested in this thesis, a resistor of 1 $M\Omega$ was considered high enough to guarantee a high drop of V_{DS}, even when small transient currents would occur.

The de-coupling capacitor C1, equal to 1 nF, acts to propagate the SEB generated pulses towards the scope, enabling this way their counting and identification. As the current provided by the power supply is limited by R_D, the discharge of the capacitor is the main source of energy when a SEB takes place. The protective resistor R_P, equal to 470 Ω, is also added in series with C1 to significantly limit the current flow towards the power MOSFET by a few orders of magnitude. Lastly, reflections on the transmission line are avoided by using a 50 Ω matching resistor on the scope input (R_3). This acquisition method has the advantage of being able to transmit the signal over a long line without additional components and without modifying the load on the power MOSFET. Moreover, the oscilloscope is protected by the high DC voltage. The pulses originated for every SEB are saved by the scope. The shape of this pulses depends on both the technology of the power MOSFET and the values of the other circuit elements. Four devices can be tested simultaneously with the described Test Board; their Drain nodes are connected to the same power supply but each power

MOSFET is connected through an individual transmission line to a different channel of the oscilloscope.

Specifically, the seamless attaching of different DUTs on the test board is accomplished through specially designed daughter boards. Each power MOSFET part (of DPAK package) is soldered on a daughter board, which maps its Drain, Gate, Source, and Ground electrodes to a male 4-pin header connector. In turn, the test board has four female 4-pin header connectors soldered on it, into which the daughter boards can be temporarily plugged. In some cases, a proper manipulation of the power MOSFETs is required, before they are soldered on their daughter board. For example, for specific irradiation conditions the samples must be decapsulated and have their silicon die exposed.

This Test Board was successfully used during the first irradiation campaigns, but some of its limitations lead to the designing of a second, upgraded version.

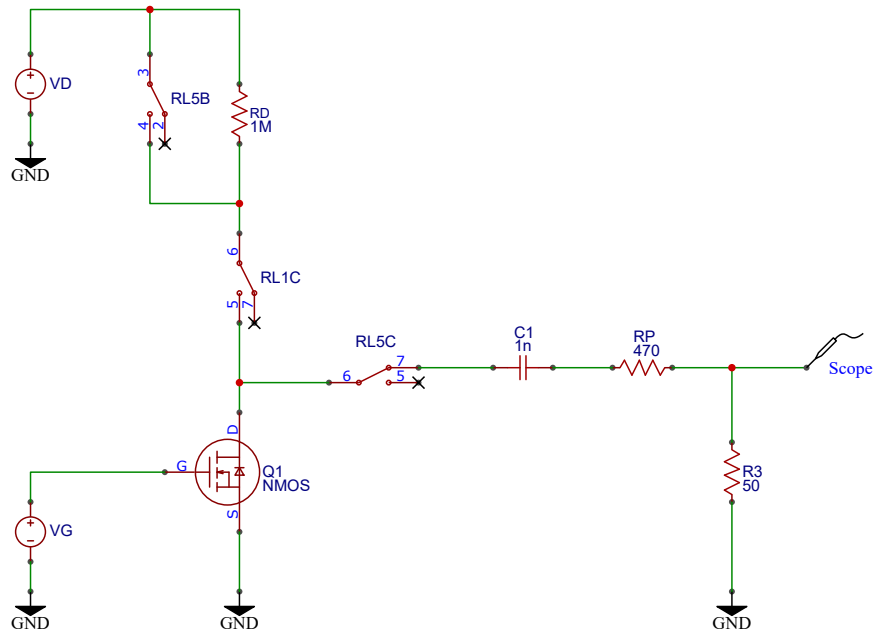


Fig. 4.5: Schematic of Board 2, the second version of the circuit used to evaluate SEE on power MOSFETs. The position of the switches represents the case 0 Volts are applied to the coil of the relays.

First of all, as the Gate node was directly connected to the ground, it was not possible to monitor I_{GS}, disabling the possibility of distinguishing a destructive SEB from a SEGR. Additionally, there was not the possibility to perform the electrical characterization of the DUTs while they were mounted on the Test Board. The characterization is considered particularly useful, on the one hand before the irradiation campaign, to confirm that the samples performance has not been affected by the manipulation, soldering or decapsulation processes, and on the other hand during the irradiation

campaign, to evaluate the effects of the Total Ionizing Dose (TID) on the response of the power MOSFETs. Performing the on-line characterization of the DUTs would require firstly applying voltage directly on the Drain and Gate node (without the interference of any passive components) and secondly disconnecting the Drain node from the part of the circuit that leads to the oscilloscope.

Both of these limitations were resolved with the second version of the Test Board (Board 2), whose schematic is depicted in Fig. 4.5. As it can be observed, the additions on the previous schematic were a voltage source in the Gate electrode, and three switches (RL1C, RL5B, and RL5C). The voltage source enabled the monitoring of I_{GS} during irradiation and the biasing of the Gate node for the electrical characterization of the DUTs. In addition, it allows testing under different Gate bias conditions (e.g. with negative Gate bias), which might be relevant for some SEGR studies. Although this option was not explored in the present study. Regarding the switches, the one named RL1C was used to disconnect the DUT from the Drain Bias, while the ones named RL5B and RL5C short-circuit R_D and detach the DUT from the circumvention circuit, respectively. The physical implementation of Test Board 2, along with labels on its structural parts, is shown in Fig. 4.6

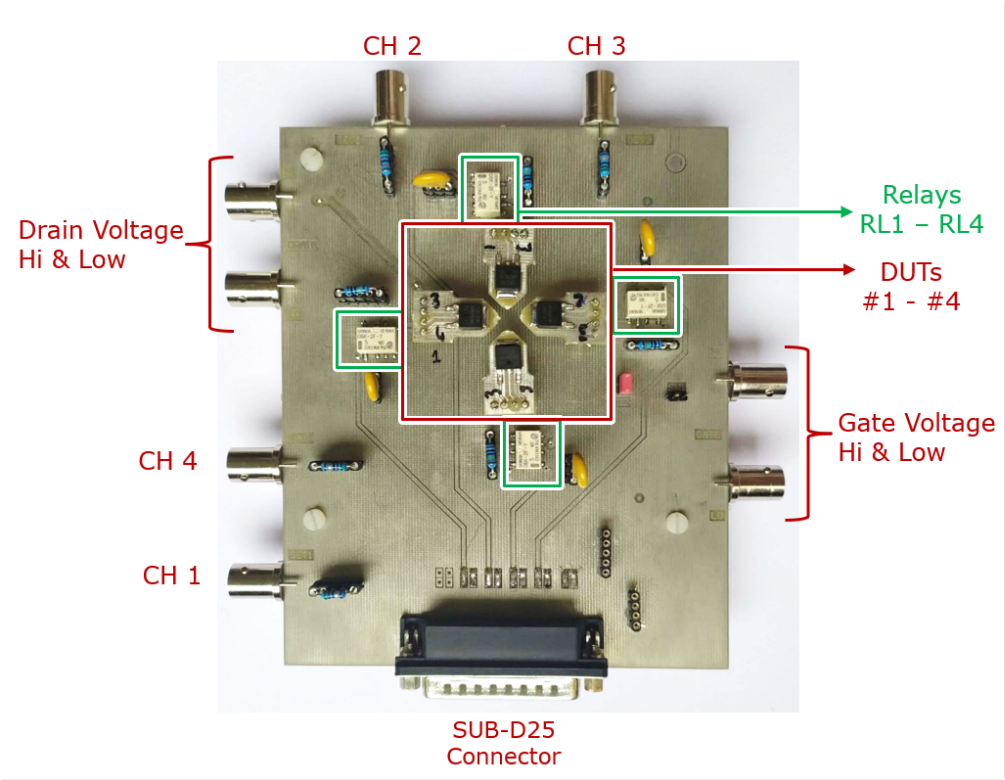


Fig. 4.6: Close picture of the physical implementation of Test Board 2.

Exploring further the functionality of the switches, they are implemented through Double Pole Double Throw (DPDT) relays. A DPDT relay encloses two switches that

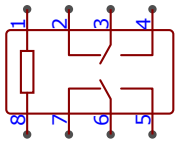


Fig. 4.7: Schematic of the wiring of a Double Pole Double Throw (DPDT) relay.

Tab. 4.2: Specifications of the relay switches mounted on the Test Board.

Reference	Manufacturer	Model	Rated Coil Voltage (V)	Rated Current (mA)	Operation Voltage	Power Consumption (mW)
G6K-2G-Y	OMRON	Highly Insulated	5	21.1	80% of rated voltage	100

are controlled by the same coil, and its design is illustrated in Fig. 4.7. For Test Board 2, 8 relays (RL1 - RL8) are used in total, two for each power MOSFET, and their specifications can be looked over in Tab. 4.2. Specifically, DUT #1 is connected to RL1 and RL5, DUT #2 is connected to RL2 and RL6, DUT #3 is connected to RL3 and RL7, and DUT #4 is connected to RL4 and RL8. Relays RL1 up to RL4 correspond to RL1C, shown in Fig. 4.5, and they are used to connect and disconnect the Drain of each DUT from the power supply. They were soldered on the top side of the test board and they can be distinguished in Fig. 4.6. Notice that for each relay only one of the switches is used in this case. For Relays RL5 up to RL8, both of the enclosed switches are employed, and they correspond to RL5B and RL5C, shown in Fig. 4.5. The two switches are activated simultaneously and, as it was explained in the previous paragraph, they are used to short-circuit R_D and detach each DUT from the circumvention circuit. Relays RL5-RL8 were soldered on the bottom side of the test board.

The control of all relays is accomplished through the pins a SUB-D25 connector, which is also soldered on the test board (see Fig. 4.6). The correlation between the DB 25 pins and the relays on Board 2 is depicted in Fig. 4.8. As shown, relays RL1 up to RL4, are controlled from a separate voltage pin (pin 17, 21, 23, and 25, respectively), while relays RL5 up to RL8 are all controlled from the same pin (pin 12) in order to enable the electrical characterization of all the devices.

4.4 Development of the Relays-Control Board

As soon as the second version of the test board was introduced, it was clear that an effective and practical way to control the relays on it was needed. As seen in Fig. 4.8

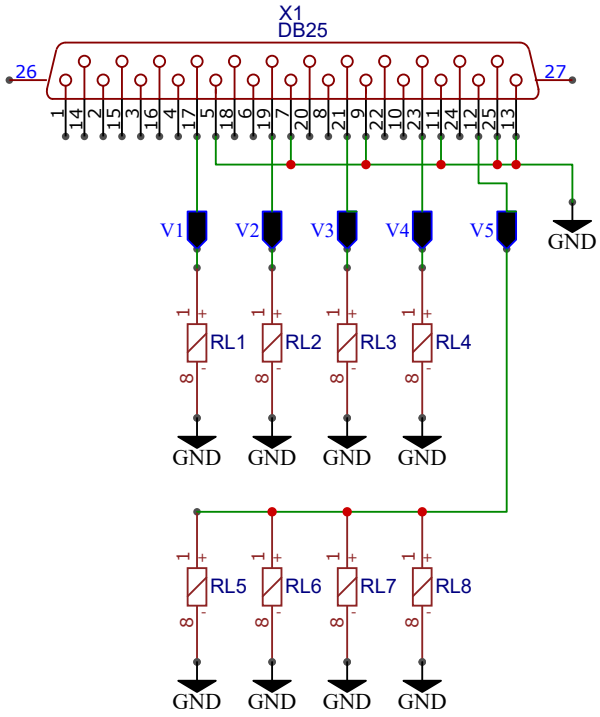


Fig. 4.8: Schematic of the connections between the relays of Board 2 and the pins of the SUB D25 Connector.

the main objective was to control the voltage applied on specific pins of a SUB D25 connector. An already existing solution for this requirement was based on powering the relays through a DC Power Supply, which would be connected to the Test Board via a custom made SUB D25-to-Banana clips cable. It was an excellent solution for a previously used Test Board, which required the control of only four relays from four separate SUB D25 pins, and under the condition that a four-channel power supply was available. This way, each pin was connected to one channel of the DC Power Supply and their output could be controlled remotely.

However, in the case of the current Test Board, the control of five pins was required and only a two-channel power supply was available. That meant, that if the previously mentioned custom cable was used and both channels of the DC Power Supply were permanently biased at $5V$, the energizing of each relay should be accomplished manually by connecting the respective banana plug to the power output. An extra layer of difficulty was added in case the custom cable was not long enough to reach the control room and thus the DC power supply should be placed inside the irradiation room. That way, the dynamic control of the relays was practically impossible.

Therefore, it was clear that a new approach to control the Test Board's relays was imperative. Some prerequisites were taken into account for the design of this new approach. First of all, the power requirements for energizing the relays should be covered. Placing sensitive electronic equipment and instruments inside the irradiation room should also be avoided. Additionally, using a commercially available cable, whose length could be larger than $20m$, would be preferred. Lastly, the control of each relay, and consequently of the voltage on each pin of the SUB D25 connector, should be preferably done remotely with a computer.

The above mentioned requirements were satisfied with the development of a new board based on the Arduino microcontroller, which will be called the "Relay-Control Board". Its schematic can be seen in Fig. 4.9.

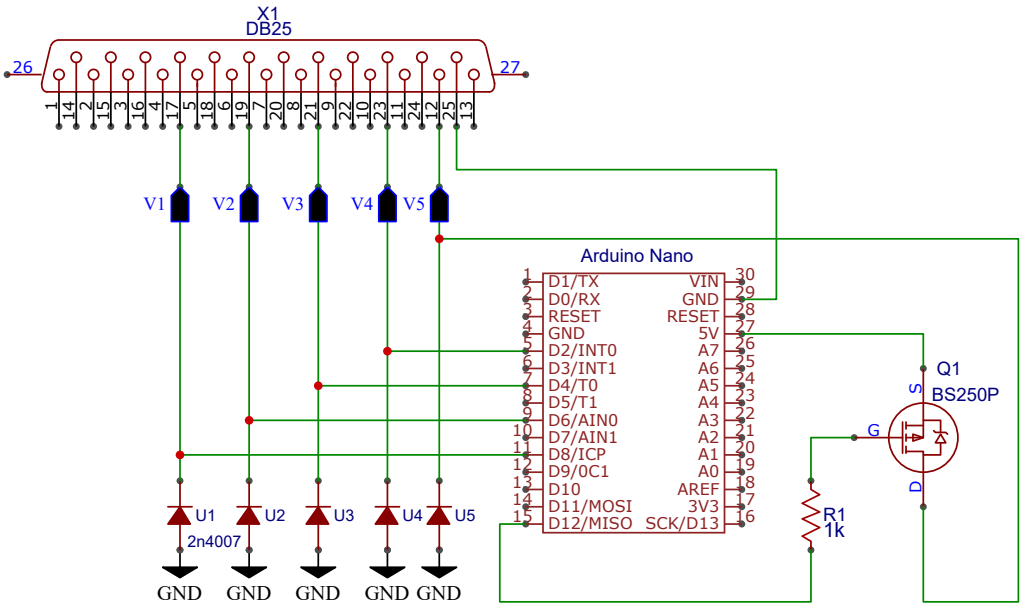


Fig. 4.9: Schematic of the Arduino-based board used to control the position of the relays on the test board.

The Arduino microcontroller has 14 digital pins whose value can be set to HIGH (5V) or LOW (0V). Each digital pin can provide up to $40mA$, while the total current from all I/O pins together should be less than $200mA$. There is also a +5V output pin, which is not connected through the microcontroller, and it can thus source significantly more power, up to $400mA$ when powered by a USB [61].

Based on the information in Tab. 4.2, the rated coil voltage of each relay is $5V$ and their rated current is $21.1mA$. The relays can also operate at 80% of their rated voltage, i.e. $4V$, drawing a slightly higher current in this case, equal to approximately $25mA$. Therefore, considering the worst-case scenario, it can be assumed that each one of RL1 up to RL4 (see Fig. 4.8) requires $5V$ and $25mA$ to function properly.

However, as RL5 up to RL8 are connected in parallel, they will cumulatively consume $100mA$ under a bias of $5V$.

Taking these current consumption limitations into consideration, it is possible to use four digital pins (e.g. D2, D4, D6 and D8) to power and control directly each one of $RL1 - RL4$. Relays $RL5 - RL8$ are powered through the +5V pin and are controlled by means of a p-channel MOSFET that is also included in the circuit. A p-channel MOSFET was selected in particular because the load, here the relay, is directly connected to the ground, and a High Side switch should be implemented [62]. The p-MOSFET is controlled from a dedicated digital pin of the Arduino (D12), as shown in Fig. 4.10 in more detail. Considering that the Source is permanently connected to the +5V pin ($V_S = 5V$), the p-channel MOSFET is turned-on when $V_{D12} = V_G = 0V$ ($V_{GS} = -5V$), setting $V5 = V_D = 5V$ and thus energizing $RL5 - RL8$. On the contrary, when $V_{D12} = V_G = 5V$ ($V_{GS} = 0V$), the PMOS is turned off, setting $V5 = V_D = 0V$.

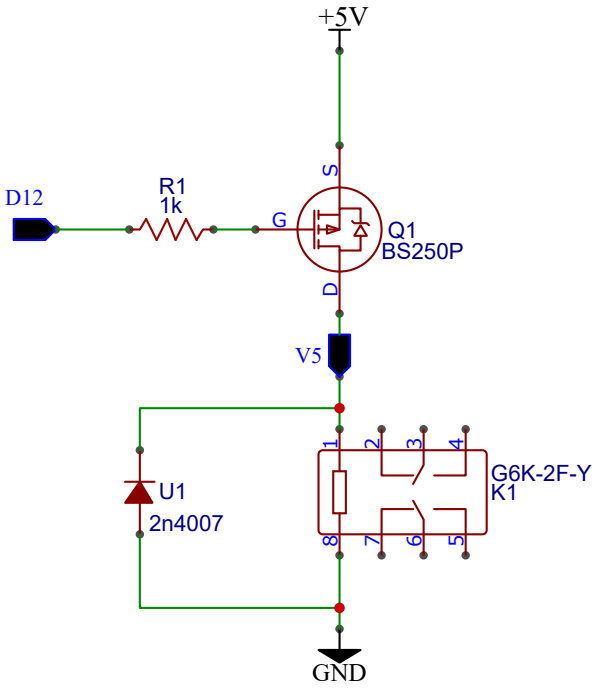


Fig. 4.10: Simplified circuit demonstrating the control of RL5-RL8 using the +5V Arduino pin as the power source and a p-MOSFET as a switch. The p-MOSFET's gate is driven by a digital pin of the Arduino (D12).

Finally, U1, the diode placed across the coil of the relay, is called "flyback diode" and protects the microcontroller from voltage spikes seen across inductive loads when their supply current is suddenly reduced or interrupted.

The connection between the Test Board and the Relay-Control Board is accomplished through a simple male/female DB25-DB25 cable, which is commercially available and already provided by many irradiation facilities. Additionally, it was tested that the voltage drop because of the internal resistance of a $20m$ cable was less than $1V$, securing the seamless control of the relays. A commercial DB25 Breakout Board was used to adapt the pins of the SUB D25 connector to header pins that could be soldered on a breadboard. A closer picture of the first prototype of the Relay-Control board can be seen in Fig. 4.11.

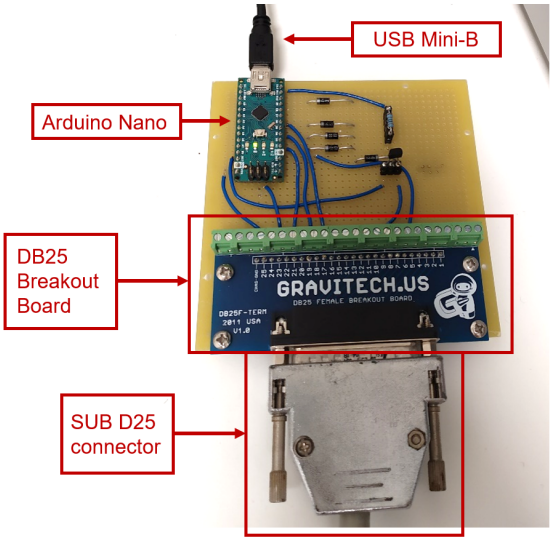


Fig. 4.11: Close picture of the first prototype of the Relay-Control Board

4.5 Experimental Setup and Software

Fig. 4.12 illustrates the experimental setup and the connections between the test board and the rest of the required equipment. As shown, there is no need to place any instruments inside the irradiation room or close to the beam, avoiding this way their dose exposure and possible contamination. The arrows in the Figure indicate the flow of information between different parts of the setup, while the connections between the Test Board and the used instruments were made with RG58 (50 Ω impedance) BNC cables, apart from the DB25 Male/Female cable that was used in combination with the Relays-Control Board. The placement of the experimental equipment in the control room is pictured in Fig. 4.13.

A side-by-side picture of Board 1 and Board 2 placed in the irradiation room can be seen on Fig. 4.14. In the center of each board, the four small daughter boards can be spotted. In both cases, the boards are placed in front of the beam thanks to a metallic frame and a plexiglass sheet attached on it. The Test Board is screwed

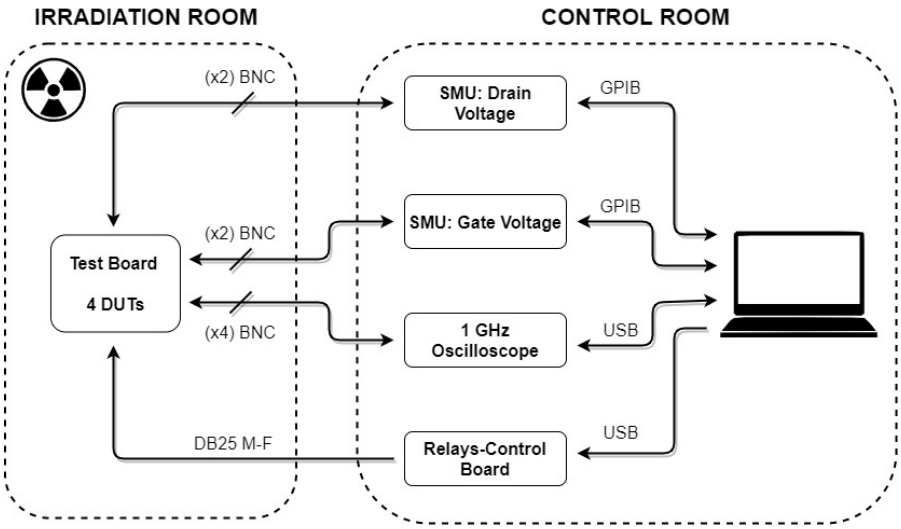


Fig. 4.12: Schematic of the experimental setup for the evaluation of SEBs on power MOSFETs.

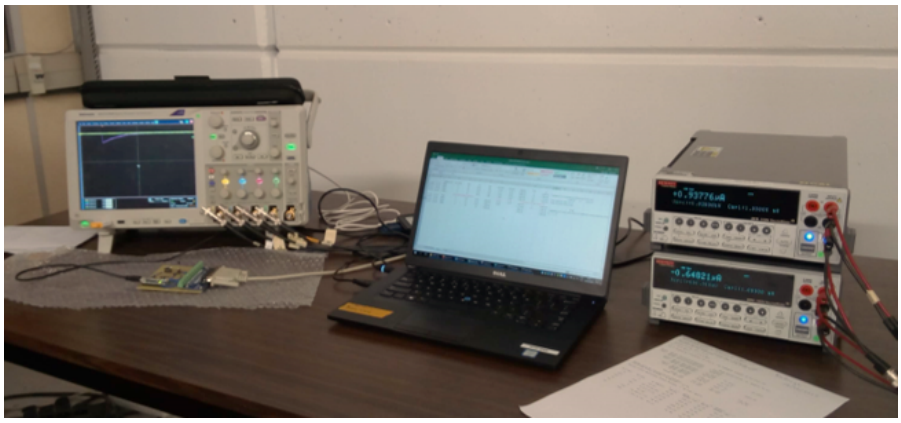


Fig. 4.13: Photo of the experimental equipment placed in the control room during irradiation.

on the plexiglass sheet and is always facing the beam vertically. Particular attention should be paid so that the power MOSFETs are irradiated with the center of the beam. In conclusion, thanks to the effort in the preparation of the instrumentation, the only thing remaining in the irradiation room is the test board.

The Relays-Control Board, being based on the Arduino microcontroller, was controlled from the external PC through the Arduino IDE. During the irradiation tests, RL1 up to RL4 were energized, so that the Drains of all four DUTs were connected to the power supply. In case a DUT failed during the test, it was possible to disconnect just this one, and keep testing the rest, without having to physically intervene with the experiment. For the characterization, RL5 up to RL8 were energized to short-

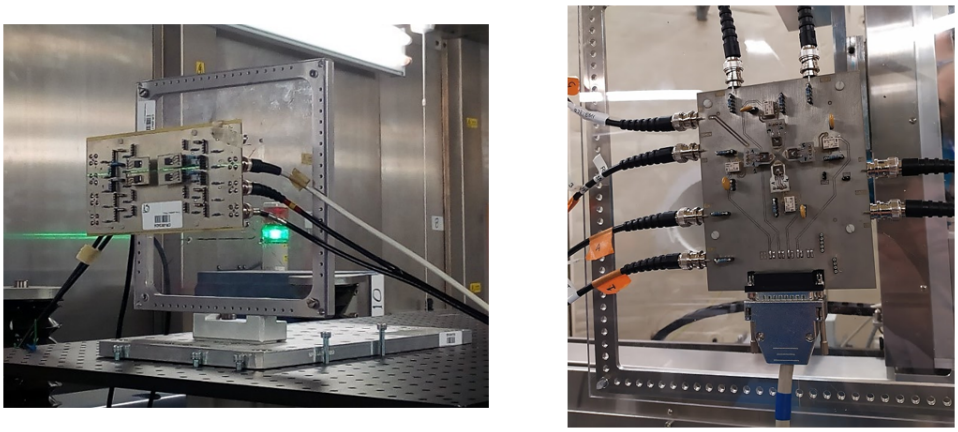


Fig. 4.14: Photo of Board 1 (left) and Board 2 (right) placed inside the irradiation room, in front of the beamline.

circuit R_D and detach the circumvention circuit for all DUTs and then depending on which DUT would be characterized, one of RL1 up to RL4 was also energized.

Two Source Measure Units (SMU) Keithley 2410 were used to bias the Drain and the Gate of the power MOSFETs and monitor the supplied current. As the board allows for testing up to four components in parallel, the current registered with the SMUs was the addition of I_{DS} and I_{GS} current flowing through the DUTs. During irradiation, monitoring I_{GS} was essential to determine if a Single Event Gate Rupture (SEGR) had taken place.

Both SMUs were controlled from the same python script (script 1) running on the user's latptop, taking advantage of the GPIB connection system. When running the script for irradiation testing, the user had to define *(i)* the reference of the power MOSFET that was tested, *(ii)* the required voltage that should be supplied by the SMUs, *(iii)* the duration of the experimental run, and *(iv)* how often the values of I_{DS} and I_{GS} should be measured and saved. Of course all of these information were saved on a separate file for the later analysis of the results.

During the irradiation, the control software run the following steps:

1. The Gate Bias V_{GS} was set equal to zero for the duration of the test

2. Starting Drain voltage bias (V_0) was applied and held for the selected irradiation time (t_{irr})

3. Output currents I_{DS} and I_{GS} were repeatedly measured and registered according to the selected readout time (t_{read})

4. Once t_{irr} is reached, the Drain voltage bias is increased by a certain value $V_i = V_0 + \Delta V$

5. Steps 2 to 4 are repeated until the measurements at the final Drain voltage bias (V_F) are completed.

t_{irr} was typically selected to accumulate a target fluence per voltage bias step (Φ_{step}). Alternatively, the experimental run for a specific voltage bias was manually interrupted as soon as enough statistics had been gathered. Depending on the rate of SEB events, t_{read} was set to obtain an acquisition every 1 to 10 seconds. In turn, $V0$, ΔV and V_F were selected to cover a relevant range of bias voltages for each MOSFET reference. It should also be noted that the voltage applied on the Drain node of the DUT was slightly smaller than the one provided by the SMU. This was attributed to the cable distance and the resistive divider caused by the leakage current of the device. It was empirically calculated that the bias of the DUT was 10% smaller than the one provided by the SMU.

SEB induced pulses were observed and registered with an oscilloscope Tektronix DPO 4104B (4 channels, 1 GHz, 5 GS/s). The acquisition was triggered every time the voltage signal exceeded -200 mV in any on the channels. The pulses of the four channels, as well as the timestamp, were saved for every trigger thanks to another python script (script 2) running on the external PC connected to the scope via USB. It should be noted that the acquisition of the pulses from the oscilloscope was the main bottleneck of the whole experimental process. Based on empirical measurements, approximately 1 sec was required until the acquisition process was complete and a new pulse could be registered. As a result, the flux of the beam during each experiment should be carefully selected so that the saturation of the instrument, and the subsequent underestimation of the cross-section, could be avoided.

During the characterization, a separate python script (script 3) was controlling both of the SMUs. The electrical characteristics that were considered useful were (*i*) the Gate threshold voltage $V_{GS(th)}$, (*ii*) the Drain-to-Source leakage current (I_{DSS}) and (*iii*) the static Drain-to-Source On-Resistance $R_{DS(on)}$.

- For the calculation of $V_{GS(th)}$, the evolution of $I_{DS} = f(V_{GS})$ for $V_{DS} = V_{GS}$ is registered by the SMUs

- For the calculation of I_{DSS}, the evolution of $I_{DS} = f(V_{DS})$ for $V_{GS} = 0$ is registered by the SMUs

- For the calculation of $R_{DS(on)}$, the evolution of $I_{DS} = f(V_{DS})$ for $V_{GS} \gg V_{GS(th)}$ is registered by the SMUs

The variation of V_{DS} and V_{GS} was controlled by the python script based on the information provided in the Data Sheet of each power MOSFET reference. When running the script, and after adjusting the position of the relays, the user just had to select the reference that was mounted on the Test Board and the characterization of the first DUT was initiated. Then, the script was paused, waiting for the user to readjust the position of the relays, and the characterization of the next DUT was initiated once again.

4.6 SEB Circuit-level Simulation

Modeling techniques have been a powerful tool in the radiation-effects community in an attempt to further understand the underlying mechanisms of SEEs. The vast majority of publications employ technology computer-aided design (TCAD) tools to create 2D or 3D geometrical models of the semiconductor structure to be analyzed, define the material properties based on physics models, and solve numerically the equations that come up from the radiation-induced carrier generation in the device. The main advantage of device-level TCAD modeling is the increased accuracy due to inclusion of detailed physical phenomena, as well as spatial effects and interactions. Nevertheless, the specialized software required to run these simulations, as well as their computational intensity are two major limiting factors.

An alternative that overcomes these limitations, are circuit-level simulations of SEEs that are based on compact model-based solutions of electronic circuits. The main tool used in this case is SPICE, a widely accessible, general-purpose circuit simulation program. Of course, this approach comes with reduced accuracy, as less physical details can be taken into consideration, underlying that the completeness of a model is a constant trade-off between its usability and efficiency [22, 63].

A circuit-level simulation of SEBs was first introduced by J. Liu *et. al.* in [64] and the model they proposed is based on the circuit of Fig.4.15. The model focuses on the parasitic BJT of the power MOSFET and isolates it from the rest of the device. The parameters required for the simulation of the parasitic BJT can be extrapolated, provided that the structure of the power MOSFET (dimensions and doping of its layers) is known. Rb is a resistor whose value depends on the various strike locations where the charge was deposited, and Cbe, Cbc correspond to the depletion capacitances of the Base-Emitter junction and Base-Collector junction, respectively. When an ionizing particle hits the device, the RC circuit is charged

and if the voltage drop across Rb becomes large enough, the BJT is turned on and current Ic starts to flow through the Collector.

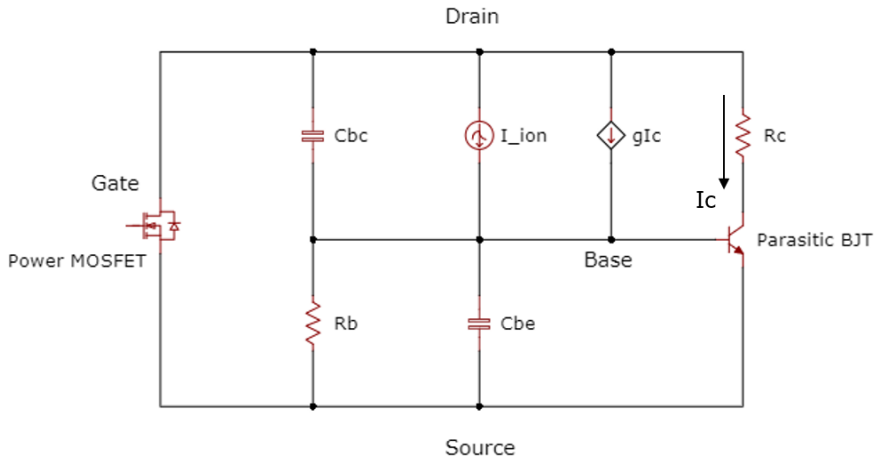


Fig. 4.15: Circuit Level simulation of SEB proposed by J. Liu in [64].

The simulation of the, rather complicated, charge generation and collection processes was extensively studied by Massengill in [65], who proposed that the most accurate model would be a double-exponential time-dependent current pulse, described by the following equation:

$$I(t) = I_0[e^{-\alpha t} - e^{-\beta t}], \tag{4.3}$$

and illustrated in Fig. 4.16. In the SPICE simulation, the current source is denoted as I_{ion} and the appropriate values of α and β have to be empirically derived. This approach focuses on the critical charge (Q_c) that must be delivered on the electronic component to create an error condition, and ignores other parameters, such as the particle type, energy, LET, or type of charge collection. Additionally, the regenerative feedback mechanism, which is crucial to whether a SEB will take place or not, is simulated with a current-dependent current source (gIc in Fig. 4.15). It takes the current flowing through the Collector of the BJT, multiplies it by a factor of g and then feeds it back in the Base of the BJT. The parameter g is expressing the avalanche multiplication process and should be empirically approximated. Further additions in the same model were done by Walker *et. al* in [66] in order to include the thermal effects due to the increased power dissipation during a SEB.

The simplified version of the model was employed by Oser *et. al.* [60] who incorporated it in their non-destructive circuit (see Sec. 4.3), in order to improve the understanding on the SEB processes and particularly the influence of the auxiliary components. The circuit is shown on Fig. 4.17. In their work, they tried to tune

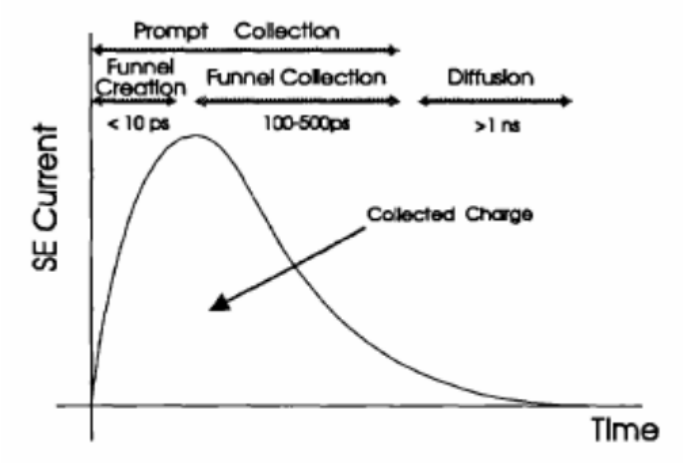


Fig. 4.16: Typical shape of the Single Event charge collection current at a junction [65].

the parameters of the model so that the simulated transient voltage drop across $R3$ would be the same as experimental pulses saved by an oscilloscope. The same Drain bias ($V_D = 100V$) and values of auxiliary components ($RD = 1M\Omega$, $C1 = 1nF$, $Rp = 100\Omega$, and $R3 = 50\Omega$) were used both for the experiment and the simulation. As to what regards the parasitic BJT, it seems that they used the same model J. Liu did in [64], even though different power MOSFET references were simulated. This is attributed to the fact that limited information is available regarding the structure of commercial devices, and especially for their parasitic components, without employing reverse engineering techniques. As a result, the matching between the simulated and experimental pulse could only be accomplished through the proper selection of Rb (equal to 56 Ω), the initial charge deposition by the ionising particle (modeled as a double-exponential current pulse: amplitude $= 50mA$, rise time $= .3ns$, fall time $= 1ns$) and the regenerative feedback mechanism (modeled as current-controlled current source: gain = 0.2). The model of the transmission line was added in the framework of this thesis, in an attempt to include possible effects and losses caused by the long BNC coaxial cables used to transfer the signals from the Test Board to the oscilloscope. By using the OrCAD-PSpice software [67], the simulation of transmission line effects is simplified, as it provides pre-built distributed models for a huge variety of coaxial cables. The model of RG58 coaxial cable was used in the SPICE circuit to match the ones used during irradiation campaigns. During the simulation, the only variant parameter was its length.

The model provided satisfactory results and useful insight regarding the turning-on and the turning-off of the BJT. However, when the above mentioned circuit was used with a different Rp (470 Ω instead of 100 Ω), the simulated pulse and the respective experimental one were no longer identical. Therefore, the model presented in this section can be used complementarily to experimental results and as a tool to support

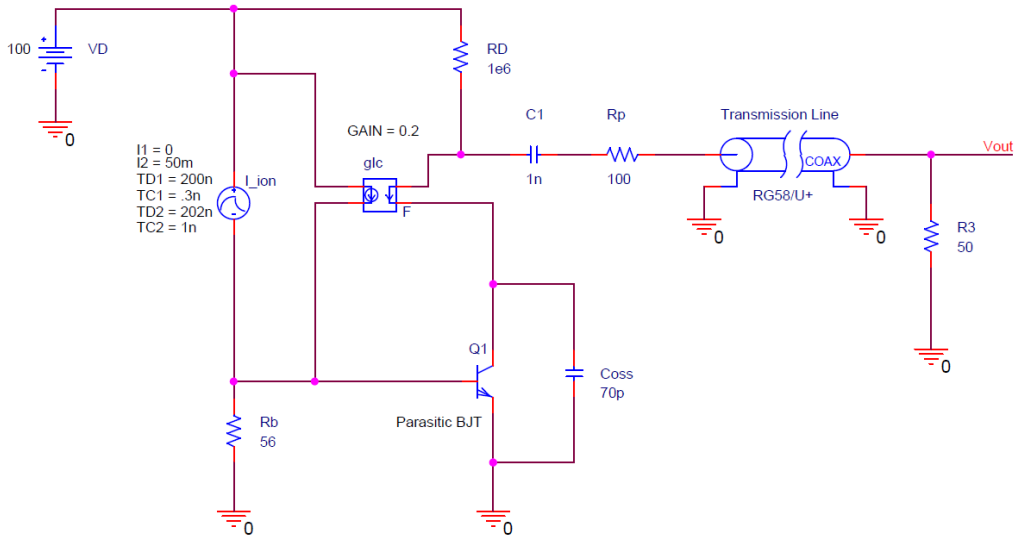


Fig. 4.17: Circuit level simulation of SEB, incorporated in non-destructive test circuit [60].

their analysis in a qualitative way. It can not be considered though a highly accurate or predictive tool. And this is not unexpected, as details which are very important in the SEB evolution (such as the structure of the parasitic BJT, the distribution of the electric field in the device, temperature increases, power dissipation etc.) are not taken into consideration by the model.

5 Irradiation Campaigns

Commercial off-the-shelf (COTS) silicon power MOSFETs have been irradiated with different particles and energy ranges in various European Irradiation facilities as part of the CERN R2E project's activities.

5.1 Irradiation Facilities

Tab. 5.1 summarizes the irradiation facilities that were visited in the scope of this work. Relevant information included is the type of the offered particle, the energy range, the LET (for the heavy ions tests), as well as the date of the experiment. These facilities and beam characteristics were selected, so that the SEE response of power MOSFETs could be evaluated under a variety of irradiation conditions. A more detailed description of each irradiation facility and the characteristics of the beams they offer is given in Subsections 5.1.1 up to 5.1.4.

5.1.1 CHARM (G0)

The CERN High Energy Accelerator Mixed-field facility (CHARM) enables the exposure of radiation components and systems to a radiation environment similar to the one of particle accelerators [68]. The radiation field is generated through the interaction of a 24 GeV/c proton beam, extracted from the Proton Synchrotron (PS), with a metallic target. Particle composition and intensity is defined by 3 parameters: *(i)* the test position within the facility, *(ii)* the position of the four shielding walls within the facility, and *(iii)* the choice of one of the three available targets, or no target in the beam. Therefore, depending on the facility configuration, the radiation field can also be used to test for different space- and ground level applications [69]. During the tests performed in the scope of this work, DUTs were placed at the G0 position, located at 87° with respect to the incoming beam on the target. A relatively soft ($H_{10\%} = 194MeV$) neutron-dominated field is present at this position [70].

Tab. 5.1: Summary of the irradiation facilities, particle beams, energies and LETs used during the R2E test campaigns .

Facility	Particle Type	Energy MeV (n, p^+) MeV/u (ions)	LET $MeV \cdot cm^2/mg$	Test Date
CHARM (G0)	Mixed Field (n, p^+, etc.)	194 ($H_{10\%}$)	–	Jun. 2018
ChipIr	Neutrons	283 ($H_{10\%}$)	–	Mar. 2019
KVI-CART	Protons	186 124 80 40	–	Jun. 2019
KVI-CART	^{129}Xe	21	44	Nov. 2019
	^{40}Ar	14 26	8 5.2	
	^{12}C	90	0.24	
GANIL	^{136}Xe	7 17 46	59 44 27	Feb. 2020

5.1.2 ChipIr

ChipIr (for Chip Irradiation) is a neutron irradiation facility and part of the ISIS Neutron and Muon Source at the Rutherford Appleton Laboratory (Didkot, UK) [71]. The facility's beamline has been optimized to mimic the atmospheric neutron spectrum and is dedicated to the irradiation of electronic components and systems for the study of SEEs. The atmospheric neutron spectrum is particularly interesting for terrestrial and avionic applications, to whom high energy neutrons impose a significant threat.

For the production of the beam, high-energy protons (accelerated up to 800 MeV in the ISIS synchrotron) are collided against a tungsten target to produce neutrons. The fast neutron ($E_n > 1MeV$) beam is then collided with a secondary scatterer, which optimizes the hard atmospheric-like spectrum and minimizes the the gamma-ray flux. Eventually, the neutron beam that is delivered to the ChipIr facility has a spectrum up to 800 MeV, with a spectral hardness ($H_{10\%}$) of 283 MeV [70]. During the test campaign, the High Energy Hadron (HEH) flux, i.e. the flux of Hadrons (neutrons, protons, pions, and kaons) with energy above 10 MeV, in the test position was measured to be:

$$HEH_{eq}Flux(E_n > 10MeV) \approx 3.6 \cdot 10^6 cm^{-2} s^{-1}. \quad (5.1)$$

The delivered flux is approximately 10^9 times higher compared to the sea-level atmospheric neutron flux, enabling accelerated tests [72]. Additionally, the beam size can vary, but in the case of this study it was selected to cover a 70 $\times$ 70 mm^2 surface area, ensuring the uniform irradiation of the tested devices. The neutrons were delivered in spills, pulsed at 10 Hz, with two 70 ns-wide bunches separated 360 ns apart. Lastly, the actual flux for each experiment was measured spill per spill with a silicon diode placed at the hole through which the beam enters the facility and corrected by a factor that accounted for the distance and in-air attenuation.

5.1.3 KVI-CART

KVI-CART (Kernfysisch Versneller Instituut - Center for Advanced Radiation Technology) is a research institution located in Groningen (the Netherlands). Its mission is to perform basic research on subatomic and astroparticle physics, as well as application-driven research on accelerator physics and physics in medicine [73]. The central facility of KVI-CART is AGOR, a superconducting (K600) cyclotron that can accelerate both light and heavy ions. In addition, beams of protons with a maximum energy of 190 MeV can be produced using a CUSP ion source [74]. The DUTs are placed in the AGOR Facility for Irradiation of Materials (FIRM), where they are irradiated by the in-air beamline.

As to what regards proton irradiation, primary energies in the range of 40 MeV to 190 MeV can be provided by the facility. Specifically, protons can be accelerated at a primary energy of 190, 66.5 or 30 MeV, which can be then degraded by means of several combinations of Aluminium slabs of different thickness. Eventually, almost all energies between 10 and 184 MeV can be provided, with a typical resolution of a few MeV due to the scatter in air, scattering system and energy degraders. After traversing about 3m of air, the energies at the position of the DUTs are typically 5-10 MeV lower depending on the scatter system used. In the framework of the R2E proton test campaign, a primary proton beam of 190 MeV was degraded to 186, 124, and 80 MeV. A primary 66.5 MeV proton beam was also degraded to 40 MeV.

Both circular and rectangular fields are available at KVI. The standard irradiation field has a diameter of 70 mm and homogeneity of better than $\pm 30\%$ [75], but rectangular fields with any surface area between 20 $\times$ 20 mm^2 and 100 $\times$ 100 mm^2 can also be provided. The maximum flux depends on the field size and energy at

DUT. Specifically, it can be adjusted in the $10^3 - 10^8\ p/cm^2/s$ range, even though a flux of $10^9\ p/cm^2/s$ can also be attained for the smallest (in terms of area) and non degraded beams. For the R2E power MOSFET proton tests, a rectangular beam with area equal to 100 $\times$ 100 mm^2 and flux equal to $10^7\ p/cm^2/s$ was selected for each proton energy.

As to what regards heavy ion irradiation, KVI-CART has been providing heavy ion beams at several energies (ranging from about 8 MeV/u to 90 MeV/u) since 2018 [76]. There are two cocktails of ions at different energies that can be provided by the cyclotron. Light elements (He, C, O, Ne) can be accelerated at a primary energy of 90 MeV/u, whereas heavy elements (Xe, Kr, Ar and Ne) can be accelerated at a primary energy of 30 MeV/u. Depending on the chosen ion and the degradation of its primary energy, the LET range can vary from 0.025 up to 60 $MeV \cdot cm^2/mg$. The flux of the lighter elements can be tuned in the $10^3 - 10^7$ range, while the flux of the heavier elements can be tuned in the $10^2 - 10^4$ range.

During the tests performed in the scope of this work, selected power MOSFET references were irradiated with Xenon ions (^{129}Xe) (primary energy of 20.8 MeV/u delivered on the DUTs), Argon ions (^{40}Ar) (primary and degraded energy of 26.4 and 13.8 MeV/u delivered on the DUTs, respectively), and Carbon ions (^{12}C) (primary energy of 90 MeV/u delivered on the DUTs), as it is also shown on Tab. 5.1. A rectangular beam of area equal to 30 $\times$ 30 mm^2 was used for all tests.

5.1.4 GANIL

The Grand Accélérateur National d'Ions Lourds (GANIL), or Large Heavy Ion National Accelerator is a research center in Caen (France), that provides heavy ion beams for nuclear and atomic physics, astrophysics, material science and radiobiology [77]. It is amongst the five largest laboratories in the world that conduct research on these topics, and by having five operating cyclotrons, up to six experiments can be simultaneously run in different experimental areas using stable beams.

Among the experimental areas, G4 is a cave dedicated to industrial applications, where the in-air irradiation of electronic components with medium and high energy beams is possible. SEE testing is possible with ions as ^{36}Ar,^{86}Kr,^{129}Xe and ^{208}Pb in a wide LET range (16 to 96 $MeV \cdot cm^2/mg$). It should be noted that during an irradiation campaign, only a single ion species at a single primary energy is available, even though the actual kinetic energy and LET of the ion can be varied over an extended range. This can be accomplished either by introducing thin foils of aluminium (25 up to 1000 μm) or by adjusting the air distance between the component and the beam-exit window (53 up to 200 mm). The beam has an

instantaneous size of 1 $\times$ 4 cm^2 and two scanning magnets (Horizontal & Vertical) allow an irradiation area of about 50 $\times$ 4 cm^2. The flux can get values from few tens of $ions/cm^2/sec$ up to approximately 10^4 $ions/cm^2/s$.

During the tests performed in the scope of this work, Xenon ions of primary energy equal to 50 MeV/u were used. Due to the air distance from the beam-exit window, the energy on the DUTs was 46 MeV/u with a primary LET of 27 $MeV \cdot cm^2/mg$. The beam was also degraded by means of thin Aluminium slabs, resulting in additional energies equal to 17 and 7 MeV/u. The maximum LET delivered on the devices was estimated to be 59 $MeV \cdot cm^2/mg$.

5.2 Commercial Power MOSFETs tested

A list of all the power MOSFET references that have been tested throughout all irradiation campaigns is compiled in Tab. 5.2. The list includes the maximum Drain voltage that can be applied in the OFF-State (V_{Rated}), the maximum current that can be conducted in the 0N-State (I_D), and the on-resistance (R_{on}). Additional relevant information is the foundry that manufactures the device and the implemented technology, as well. From now on the references will be referred to by the Short Name that is indicated in the Table. A visual representation of the power MOSFETs' different characteristics is also depicted in Fig 5.1.

Tab. 5.2: Characteristics of power MOSFET tested references.

Short Name	Reference	Foundry	V_{Rated} $[V]$	I_D $[A]$	R_{on} $[\Omega]$	Technology
MOS A	IRFR4105ZPbF [78]	IR	55	30	0.0245	HEXFET
MOS B	STD10NF10 [79]	ST	100	13	0.13	STripFET
MOS C	IRFB4310 [80]	IR	100	140	0.0056	HEXFET
MOS D	IPD70N10S3L [81]	Infineon	100	70	0.0115	OptiMOS
MOS E	IRLR120NPbF [82]	IR	100	10	0.185	HEXFET
MOS F	IRFR420PbF [83]	Vishay	500	2.4	3	N/A

Due to the limited available beam time offered by the irradiation facilities, it was not possible to test every reference under all irradiation conditions. Tab. 5.3 compiles the power MOSFET references that have been tested in each irradiation campaign. In the table it is also indicated which one of the two Test Board versions, that were described in detail in Sec.4.3, was used at each irradiation campaign. It should be noted that for the heavy ion test campaigns (at KVI and GANIL) the decapsulation of the samples was required to directly expose the silicon die to the ions. This was necessary because the ion's range has a strong dependence on the density and the

thickness of the materials on its path. Therefore, there would be a high risk of not having any ion arrive to the die if the package was not removed. On top of that, the ion's energy and LET would be significantly changed, to the point that it would be difficult to know what was the precise LET delivered in the active area of the components. This is not a problem for protons and neutron irradiations, where the degradation due to the packaging is negligible and therefore the samples don't need to be delidded. A detailed description of the data collected from each irradiation campaign will be presented in Chapter 6.

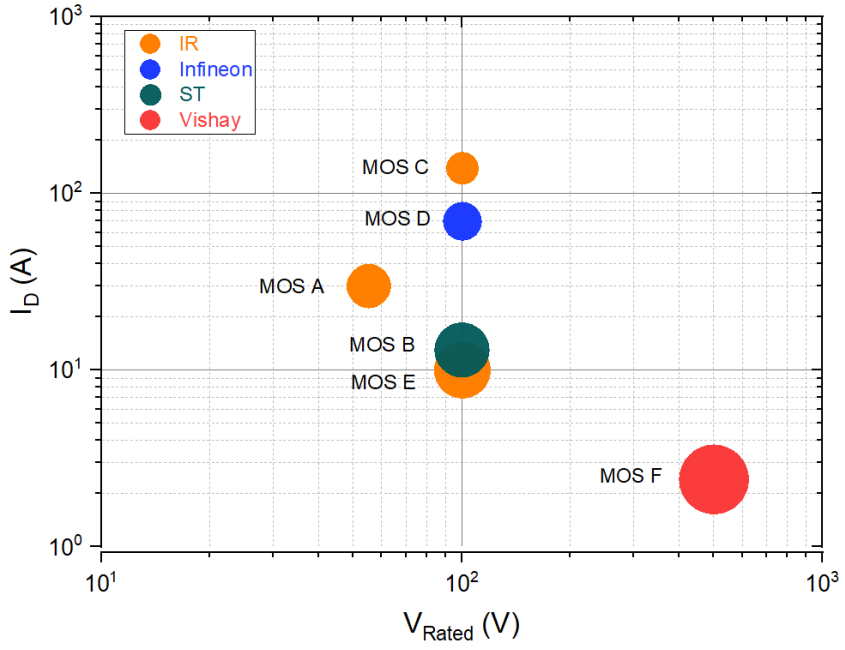


Fig. 5.1: Visual comparison of the characteristics of the tested power MOSFETs. The two axes correspond to V_{Rated} and I_D in logarithmic scale. The area of the scatter points corresponds to the common logarithm of their R_{on} expressed in $m\Omega$. The color of the scatter points corresponds to the manufacturer.

Tab. 5.3: COTS power MOSFET references tested in each irradiation campaign.

	MOS Reference						Test Board
	A	B	C	D	E	F	
ChipIr (n)	✓	✓	✓	✓	✓	✓	1
CHARM (MF)		✓					1
KVI (p^+)	✓	✓					1
KVI (Xe)		✓		✓			2
KVI (Ar, C)	✓						2
GANIL (Xe)	✓	✓		✓			2

6 SEE on Power MOSFETs: Test Campaigns Results

6.1 Neutrons - Mixed Field Irradiations

Every power MOSFET reference studied in this work was tested in the neutron atmospheric field of ChipIr. Tab. 6.1 summarizes the experimental runs carried out during the test campaign, including information about the number of samples tested for each reference, the average flux, and the range of the voltage steps applied on the Drain of the DUTs. In summary, non-destructive SEB events were registered for MOS A, MOS B, and MOS F. No events, neither destructive nor non-destructive were registered for MOS D and MOS E. Lastly, high current started flowing through the MOS C samples while at the 0FF-state, indicating their destruction due to a SEB.

Tab. 6.1: Experimental Runs performed at ChipIr for the evaluation of SEE on power MOSFETs.

Run	Device	# of DUTs	Average Flux $n/cm^2/s$	Voltage Range $[V]$	Comments
1	MOS A	4	$3.6 \cdot 10^6$	$43 - 54$	Non-Destructive SEBs
2	MOS B	3		$80 - 99$	Non-Destructive SEBs
3	MOS C	2		$63, 72$	Destructive Events
4	MOS D	4		$85, 99$	No Events
5	MOS E	1		$72 - 104$	No Events
6	MOS F	1		$225 - 405$	Non-Destructive SEBs

Fig. 6.1 summarizes the data gathered during the experimental runs by depicting the estimated SEB cross-section values for references A, B, C, and F as a function of the normalized (V_{DS}/V_{Rated}) bias voltage. For the sake of comparison, the same table includes the calculated cross-section of MOS B, under the effect of CHARM's mixed field. The SEB sensitivity seems to increase for the devices that are rated for

higher voltages, both in terms of $V_{SEB|th}$ (SEBs start occurring for a smaller ratio of V_{DS}/V_{Rated}), and in terms of cross-section (the die area that is sensitive to SEBs is larger).

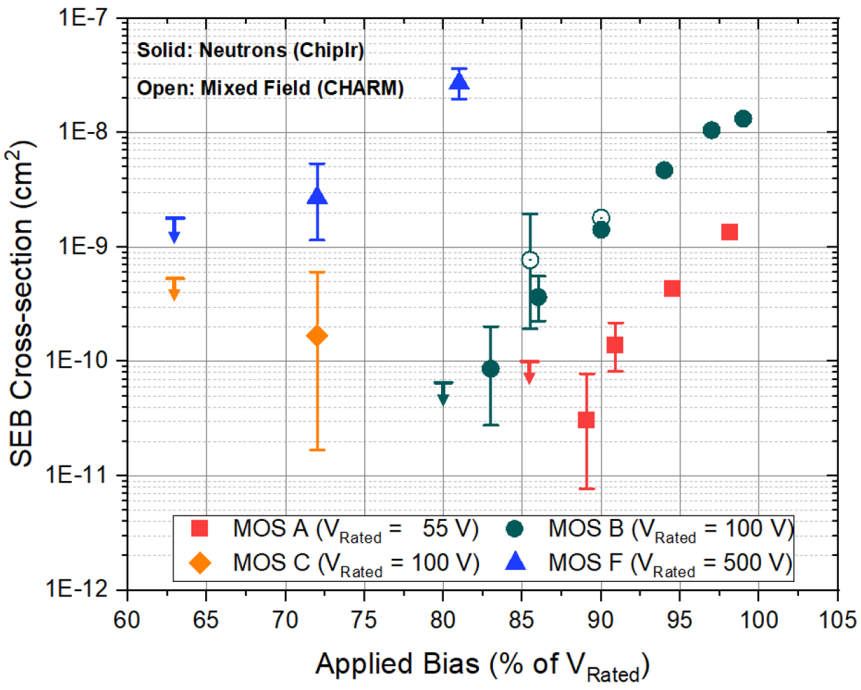


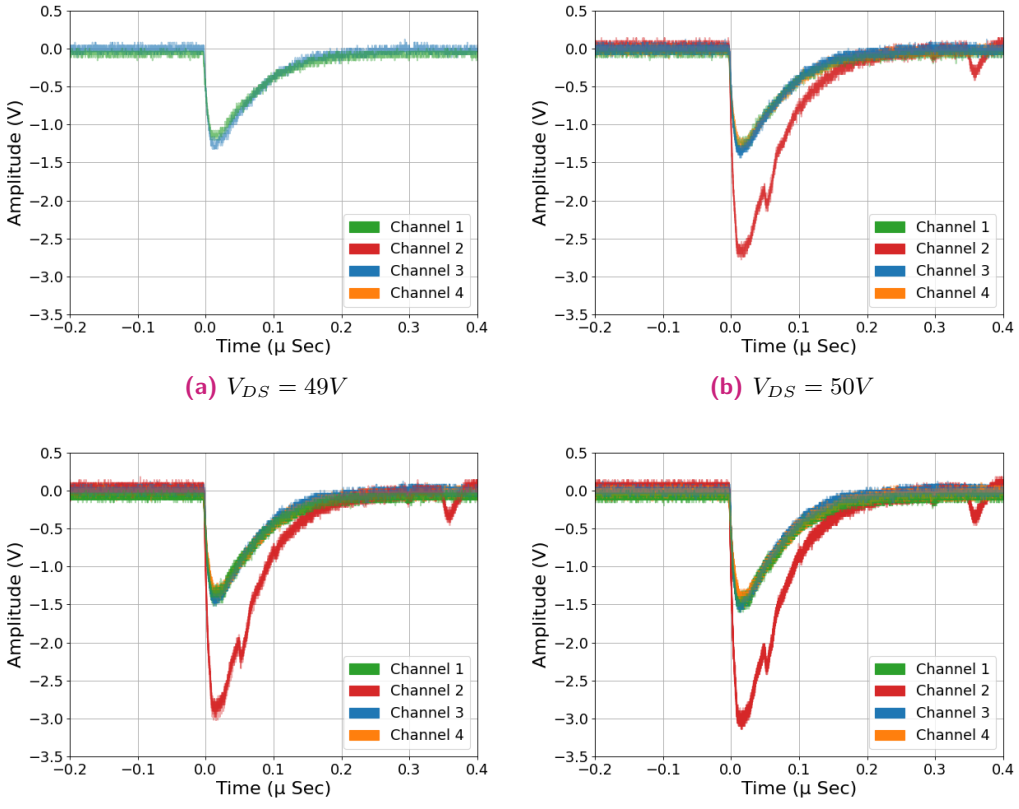
Fig. 6.1: Measured SEB cross-sections as a function of the normalized bias, for all tested references at the ChipIr neutron atmospheric field (solid symbols) and the CHARM mixed particle field (open symbols).

6.1.1 Results for MOS A

Table 6.2 gathers the number of SEBs observed for each bias step, along with the estimated cross-section values, during the irradiation of MOS A. The accumulated fluence for each bias step is listed in the table, as well. As described in Subsection 4.2, for the cases with less than 50 observed SEBs, lower and upper limits of the cross-sections were calculated using a Poisson distribution with 95% confident level. When zero events were registered for a specific voltage step, an upper limit of the cross-section was calculated using the same distribution. These points are depicted in Fig. 6.1 with a short horizontal line and an arrow facing downwards attached at its middle. It can also be seen at Tab. 6.2 that no SEBs were observed for a bias below 49 V. As it was explained in Section 4.2, a significantly high fluence was accumulated for each bias step (in this case higher than $1.0 \cdot 10^{10} n/cm^2$) in order to define the bias threshold for which the device becomes SEB sensitive. Therefore, for this Run it is considered that $V_{SEB|th} = 49V$.

Tab. 6.2: Number of SEBs and estimated cross-section values for MOS A at ChipIr. 4 DUTs were placed on the Test Board.

V_{DS} $[V]$	Φ_{step} $[n/cm^2]$	SEB	Cross-section $[cm^2]$		
			Real	Lower	Upper
43	$1.29 \cdot 10^{10}$	0	–	–	$7.19 \cdot 10^{-11}$
45	$1.29 \cdot 10^{10}$	0	–	–	$7.16 \cdot 10^{-11}$
47	$9.24 \cdot 10^{9}$	0	–	–	$1.00 \cdot 10^{-10}$
49	$3.26 \cdot 10^{10}$	4	$3.07 \cdot 10^{-11}$	$7.67 \cdot 10^{-12}$	$7.82 \cdot 10^{-11}$
50	$3.26 \cdot 10^{10}$	18	$1.38 \cdot 10^{-10}$	$8.20 \cdot 10^{-11}$	$2.18 \cdot 10^{-10}$
52	$3.24 \cdot 10^{10}$	56	$4.32 \cdot 10^{-10}$	–	–
54	$3.12 \cdot 10^{10}$	168	$1.35 \cdot 10^{-9}$	–	–



(a) $V_{DS} = 49V$ (b) $V_{DS} = 50V$

(c) $V_{DS} = 52V$ (d) $V_{DS} = 54V$

Fig. 6.2: Signal waveforms corresponding to non-destructive SEBs observed in Run 1 at ChipIr for four MOS A parts, under increasing V_{DS} bias.

Additionally, the pulses registered by the oscilloscope for each voltage step are shown on Fig. 6.2. Each pulse color corresponds to a different channel of the scope, and therefore, to a different DUT, experiencing the Burnouts. The red pulses, which

correspond to DUT #2, stand out in this case, as they are almost two times as high as the rest ones. The fact that only the pulses produced by DUT#2 have this characteristic, indicates that this shape is attributed to the technology of the sample or the components that intervene between the sample and the scope, rather than the biasing or the irradiation conditions. In case such a behavior is observed in a future experiment, it is recommended to change the position of the divergent sample and repeat the test, in order to define whether the characteristic pulse was produced because of the sample or the channel. On the contrary, the pulses saved by channels 1, 3 and 4 show great similarity in terms of shape and size for all voltage steps. The slight increase of the pulse amplitude with increasing V_{DS} was expected and can be attributed to the higher electric field that exists across the epitaxial layer when the parasitic BJT is turned on.

6.1.2 Results for MOS B

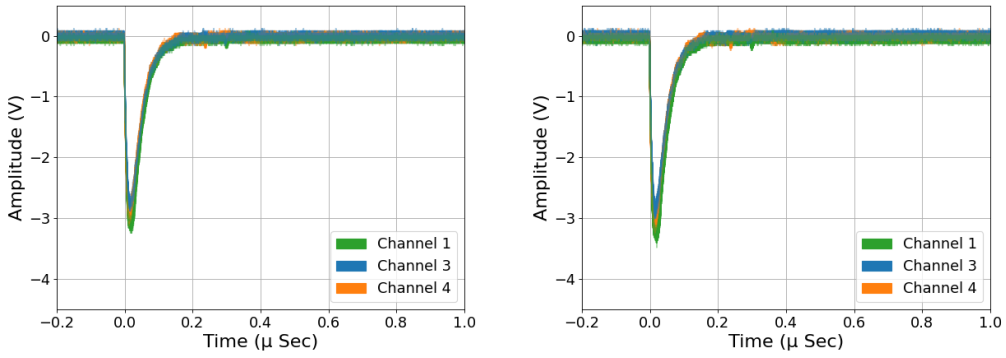
Table 6.3 gathers the number of SEBs observed for each bias step, along with the estimated cross-section values, during the irradiation of MOS B. The accumulated fluence for each bias step is listed in the table, as well. Based on the information of Tab. 6.3 we establish that $V_{SEB|th} = 83V$. MOS B was also tested at the mixed particle field of CHARM, providing the results presented in Tab. 6.4. In particular, only a couple of biases were applied on MOS B at CHARM, and SEBs were observed for both of them, making in it impossible to approximate $V_{SEB|th}$ in this case. However, the estimated cross-section of MOS B in the neutrons-dominated field of CHARM is in a good agreement with the respective cross-section values in the field of neutrons of ChipIr. This is also illustrated in Fig. 6.1, where the data obtained at CHARM are depicted with open symbols.

Tab. 6.3: Number of SEBs and estimated cross-section values for MOS B at ChipIr. 3 DUTs were placed on the Test Board.

V_{DS} $[V]$	Φ_{step} $[n/cm^2]$	SEB	Cross-section $[cm^2]$		
			Real	Lower	Upper
80	$1.89 \cdot 10^{10}$	0	–	–	$6.54 \cdot 10^{-11}$
83	$1.93 \cdot 10^{10}$	5	$8.64 \cdot 10^{-11}$	$2.76 \cdot 10^{-11}$	$2.02 \cdot 10^{-10}$
86	$1.91 \cdot 10^{10}$	21	$3.66 \cdot 10^{-10}$	$2.27 \cdot 10^{-10}$	$5.58 \cdot 10^{-10}$
90	$1.91 \cdot 10^{10}$	81	$1.42 \cdot 10^{-9}$	–	–
94	$1.91 \cdot 10^{10}$	270	$4.71 \cdot 10^{-9}$	–	–
97	$1.87 \cdot 10^{10}$	592	$1.05 \cdot 10^{-8}$	–	–
99	$1.86 \cdot 10^{10}$	741	$1.33 \cdot 10^{-8}$	–	–

Tab. 6.4: Number of SEBs and estimated cross-section values for MOS B at CHARM. 4 DUTs were placed on the Test Board.

V_{DS} $[V]$	Φ_{HEHeq} $[cm^{-2}]$	SEB	Cross-section $[cm^2]$		
			Real	Lower	Upper
86	$1.30 \cdot 10^{9}$	4	$7.70 \cdot 10^{-10}$	$1.92 \cdot 10^{-10}$	$1.96 \cdot 10^{-9}$
90	$9.67 \cdot 10^{10}$	513	$1.33 \cdot 10^{-9}$	–	–



(a) $V_{DS} = 90V$ **(b)** $V_{DS} = 94V$

(c) $V_{DS} = 97V$ **(d)** $V_{DS} = 99V$

Fig. 6.3: Signal waveforms corresponding to non-destructive SEBs observed in Run 2 at ChipIr for three MOS B parts, under increasing V_{DS} bias.

Further information can be provided by the signal pulses saved by the scope during the irradiation of MOS B at ChipIr, shown in Fig. 6.3. The duration of the pulses remains relatively constant for all voltage steps, while the average amplitude rises from $3.01V$ for $V_{DS} = 90V$, to $3.37V$ for $V_{DS} = 99V$. One can also observe the pulse that is initiated after $t = 0.3\mu sec$ in Fig. 6.3d, meaning that at $t = 0$ a SEB was triggered on DUT #1 and less than $0.4\mu sec$ later a second SEB was triggered on the same DUT. Therefore, it is clear that the rate of burnouts was higher than the acquisition rate of the system, leading to an underestimation of the cross-section for biases close to the rated voltage. This can also be confirmed from Fig. 6.1, where

the point that corresponds to the highest applied bias on MOS B (99 % of V_{Rated}) seems to deviate from the trend that is established by the previous points.

Additionally, a type of pulse with amplitude close to 4 V and duration close to 0.6 μsec is noticed in the plots that correspond to the two highest V_{DS} steps. They appear to different channels (both channel 3 and channel 4) and the mechanism that led to their creation is not clear yet. The SPICE simulation of the non-destructive circuit was employed in an attempt to provide some insight into the underlying mechanism, but no combination of parameters, that would cause such a drastic change to the shape of the pulse, could be found. The main quest that arises is defining the energy source for this event, having in mind that the saved pulse is basically the voltage drop on a 50 Ω resistor because of the discharge of a 1 nF capacitor every time the parasitic BJT turns-on. It is postulated that the underlying mechanism is closely related to the high flux of neutrons and rate of SEBs.

6.1.3 Results for MOS F

Tab. 6.5: Number of SEBs and estimated cross-section values for MOS F at ChipIr. 1 DUT was placed on the Test Board.

V_{DS} $[V]$	Φ_{step} $[n/cm^2]$	SEB	Cross-section $[cm^2]$		
			Real	Lower	Upper
225	$4.06 \cdot 10^9$	0	–	–	$9.10 \cdot 10^{-10}$
270	$2.05 \cdot 10^9$	0	–	–	$1.80 \cdot 10^{-9}$
315	$2.07 \cdot 10^9$	0	–	–	$1.79 \cdot 10^{-9}$
360	$2.95 \cdot 10^9$	8	$2.71 \cdot 10^{-9}$	$1.15 \cdot 10^{-9}$	$5.36 \cdot 10^{-9}$
405	$1.59 \cdot 10^9$	430	$2.71 \cdot 10^{-8}$	$1.96 \cdot 10^{-8}$	$3.65 \cdot 10^{-8}$

One device of the MOS F reference, rated for 500 V, was also tested in the irradiation field of ChipIr. Table 6.5 gathers the number of SEBs observed for each bias step, along with the estimated cross-section values. The accumulated fluence for each bias step is listed in the table, as well. The run was intentionally interrupted while testing at $V_{DS} = 405V$, i.e. at 81% of the rated voltage, after a great increase of the measured I_{DS} was registered in the SMU. The sample kept experiencing non-destructive SEBs, even after the current increase, thus eliminating the possibility of a destructive SEE. On the contrary, the current drift was attributed to the thickness of the PCB lines and the 1 nF capacitor (C1), neither of whom was designed to handle such high voltages. It should be noted that, since Test Board 1 was used during this irradiation campaign, Test Board 2 was designed to withstand higher voltages, up to 1 kV. Nevertheless, it was still possible to estimate the value of the SEB threshold

voltage, ($V_{SEB|th} = 360$), as well as the cross-section as a function of the applied bias up to the tested value.

6.1.4 Results for MOS C, MOS D, and MOS E

A different behavior was observed in the two parts of MOS C reference during their irradiation with spallation neutrons. During the first bias step ($V_{DS} = 63V$), a fluence of $6.80 \cdot 10^9 n/cm^2$ was accumulated without observing any SEEs. During the second bias step ($V_{DS} = 72V$) though, both of the samples experienced destructive events, manifested by two incremental steps of the I_{DS} registered by the SMU. Fig. 6.4 shows the value of I_{DS} as a function of time, where $t = 0$ corresponds to the moment 72 V started being applied on the Drain of the samples. At the beginning, the added leakage current of the DUTs has a value close to $1 \cdot 10^{-4} mA$, until $t = 5.7min$ when the destruction of the first sample occurs and I_{DS} rises to $5.9 \cdot 10^{-2} mA$. Almost ten minutes later, at $t = 16.2min$, the second sample is also destroyed and I_{DS} becomes equal to $1.2 \cdot 10^{-1} mA$. As no significant increase in the gate current was observed, the events are identified as SEBs, and not as SEGR. It was also possible to get an estimation for the SEB threshold voltage for MOS C ($V_{SEB|th}$ = 72 V), and the cross-section area too, as shown in Tab. 6.6.

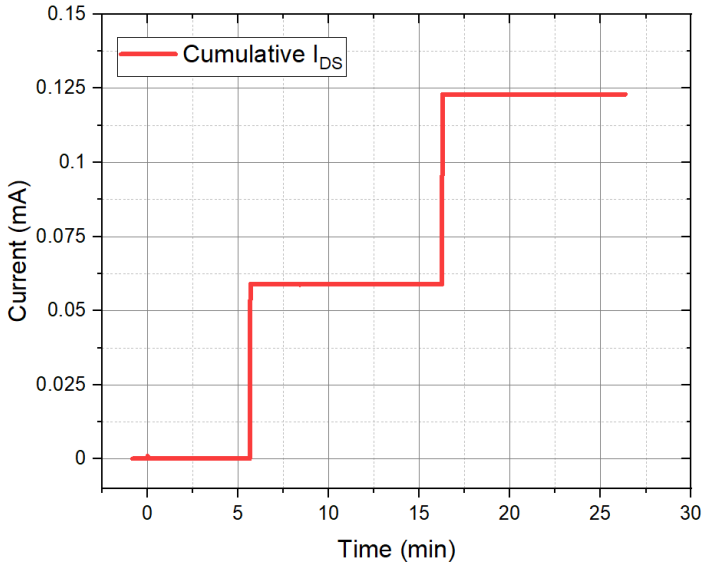


Fig. 6.4: Current flowing through the Drain of two MOS C samples, while biased at 72 V at ChipIr. The sharp steps indicate the occurrence of destructive SEEs.

Lastly, no SEBs were observed for the MOS D and MOS E samples. One MOS E sample was biased at 104 V (4 V higher than its rated voltage) until a fluence up to $6.49 \cdot 10^9 n/cm^2$ was accumulated. Similarly, two samples of the MOS D reference

were biased at their rated voltage for a neutrons fluence equal to $9 \cdot 10^{10} n/cm^2$. The estimated upper limits for their SEB cross-section were calculated and can be looked over in Tab. 6.7.

Tab. 6.6: Number of SEBs and estimated cross-section values for MOS C at ChipIr. 2 DUTs were placed on the Test Board.

V_{DS} $[V]$	Φ_{step} $[n/cm^2]$	SEB	Cross-section $[cm^2]$		
			Real	Lower	Upper
63	$6.80 \cdot 10^9$	0	–	–	$5.30 \cdot 10^{-10}$
72	$5.92 \cdot 10^9$	2	Destructive Events		
			$1.69 \cdot 10^{-10}$	$1.69 \cdot 10^{-11}$	$6.08 \cdot 10^{-10}$

Tab. 6.7: Estimated upper limit for the SEB cross-section at the highest test bias, for MOS E and MOS D.

Device	# of DUTs	Maximum V_{DS} $[V]$	Φ_{step} $[n/cm^2]$	Cross-section $[cm^2]$
				Upper Limit
MOS E	1	104	$6.46 \cdot 10^9$	$5.73 \cdot 10^{-10}$
MOS D	4	99	$9 \cdot 10^{10}$	$4.02 \cdot 10^{-11}$

It is also worth making a comparison between the results observed for MOS C and MOS E. Both references are designed by the same manufacturer (IR), are rated for the same Drain bias (100 V) and have the same cell structure (HEXFET). Their difference lies on the maximum current that can be driven in the ON-state (140 A for MOS C and 10 A for MOS E). The device with the highest current rating could not be protected by the circumvention circuit and experienced destructive SEBs, while on the other hand, no SEBs were observed for the device with the lower current rating.

6.2 Proton Irradiations

Power MOSFET references MOS A and MOS B were tested under the effect of protons with different degraded energies at KVI-CART. The experimental Runs performed are summarized in Tab. 6.8, including information about the number of devices tested for each reference, the protons selected energies, the voltage steps applied on the Drain of the DUTs, and the protons flux. The main objective of the test campaign was to repetitively test the same references, under the same biasing conditions, varying just the energy of the protons. This way, the effects of protons and their energy on the SEE susceptibility of power MOSFETs could be experimentally estimated. Only non-destructive SEB events occurred during the tests.

Tab. 6.8: Experimental Runs performed with protons at KVI for the evaluation of SEE on power MOSFETs.

Run	Device	# of DUTs	Proton Energy $[MeV]$	Voltage Steps $[V]$	Flux $[p/cm^2/s]$
1	MOS A	3	186	$[45, 49, 50, 54]$	$1.0 \cdot 10^7$
2			80		
3			40		
4	MOS B	3	186	$[72, 81, 90, 99]$	
5			124		
6			80		

6.2.1 Results for MOS A

Table 6.9 gathers the number of SEBs observed for each bias step, for all experimental runs carried out with reference MOS A. The estimated cross-section is included in the table, too. The samples were exposed to protons of degraded energies equal to 186, 80, and 40 MeV. For each energy, the same Drain bias steps (45, 49, 50, 54 V) were applied and the fluence accumulated during each step was $1.0 \cdot 10^{10} p/cm^2$. This high accuracy regarding the fluence was achieved because the beam was automatically stopped as soon as a pre-defined value was accumulated. Fig. 6.5 represents the calculated cross-sections for MOS A as a function of the normalized Drain bias, for all energies used in the test campaign.

Tab. 6.9: Number of SEBs and estimated cross-section values for MOS A at KVI under proton irradiation. 3 DUTs were placed on the Test Board.

Proton Energy $[MeV]$	V_{DS} $[V]$	Φ_{step} $[p/cm^2]$	SEB	Cross-section $[cm^2]$		
				Real	Lower	Upper
186	45	$1.0 \cdot 10^{10}$	0	–	–	$1.23 \cdot 10^{-10}$
	49		3	$1.00 \cdot 10^{-10}$	$2.00 \cdot 10^{-11}$	$2.93 \cdot 10^{-10}$
	50		6	$2.00 \cdot 10^{-10}$	$7.33 \cdot 10^{-11}$	$4.37 \cdot 10^{-10}$
	54		47	$1.57 \cdot 10^{-9}$	$1.15 \cdot 10^{-9}$	$1.75 \cdot 10^{-9}$
80	45	$1.0 \cdot 10^{10}$	0	–	–	$1.23 \cdot 10^{-10}$
	49		1	$3.33 \cdot 10^{-11}$	$3.33 \cdot 10^{-12}$	$1.87 \cdot 10^{-10}$
	50		3	$1.00 \cdot 10^{-10}$	$2.00 \cdot 10^{-11}$	$2.93 \cdot 10^{-10}$
	54		54	$1.80 \cdot 10^{-9}$	–	–
40	45	$1.0 \cdot 10^{10}$	0	–	–	$1.23 \cdot 10^{-10}$
	49		0	–	–	$1.23 \cdot 10^{-10}$
	50		0	–	–	$1.23 \cdot 10^{-10}$
	54		6	$2.00 \cdot 10^{-10}$	$7.33 \cdot 10^{-11}$	$4.36 \cdot 10^{-10}$

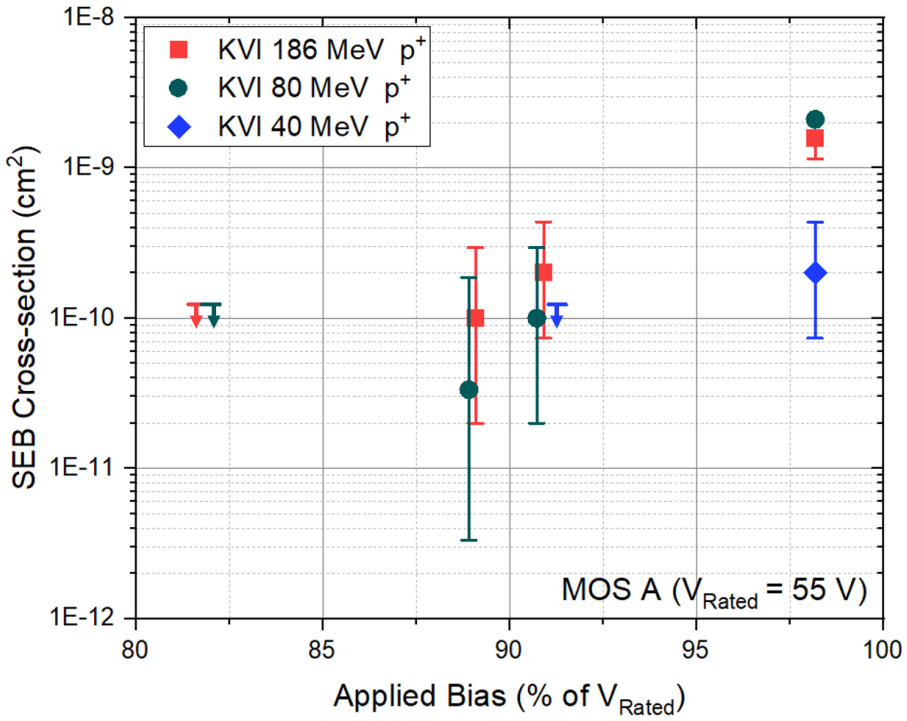


Fig. 6.5: Measured SEB cross-sections as a function of the normalized bias, for MOS A after irradiation with protons of different energies at KVI-CART. The scatter points that correspond to the same Applied Bias are artificially shifted from the actual x-value so that they are more distinguishable.

An increase of $V_{SEB|th}$ with lowering energy is evident in this case, as it shifts from 49 V, for 186 and 80 MeV protons, to 54 V for the lowest energy tested of 40 MeV. In terms of cross-section, there is an indication that the calculated value for the highest applied voltage is higher for lower proton energies. Specifically, an increment of 15% (from $1.57 \cdot 10^{-9}$ to $1.8 \cdot 10^{-9} cm^2$) was observed when the energy was decreased from 186 to 80 MeV. As to what regards the 40 MeV protons, the number of SEBs observed at the highest applied voltage ($54V$) was significantly lower compared to the number of SEBs during the irradiations with higher energies: 6 SEBs vs. 54 and 47 SEBs, for the 40, 80, and 186 MeV irradiations, respectively. This suggests that for increasingly high proton energies (higher than 80 MeV) the sensitive area has a slight decreasing tendency, but for relatively low energies (40 MeV) the sensitive area drops noticeably. Lastly, there is good agreement between the SEB sensitivity of MOS A under the effect of the neutrons environment of ChipIr and the 186 MeV protons of KVI. In both cases, $V_{SEB|th}$ is equal to 49 V, while the cross-section for $V_{DS} = 54V$ is equal to $1.35 \cdot 10^{-9} cm^2$ and $1.57 \cdot 10^{-9} cm^2$, respectively. This indicates that the same mechanisms takes place in the production of SEBs under proton and neutron irradiations. Neutrons can only produce SEBs by indirect ionization, and

the fact that the cross-section for protons is very similar, seems to indicate that direct ionization does not play a relevant role in SEB production with protons.

6.2.2 Results for MOS B

Table 6.10 gathers the number of SEBs observed for each bias step, for all experimental Runs carried out with reference MOS B. The estimated cross-section is included in the Table, too. The samples were exposed to protons of primary and degraded energies equal to 186, 124, and 80 MeV. For each energy, the same Drain bias steps (72, 81, 90, 99 V) were applied and the fluence accumulated during each step was $1.0 \cdot 10^{10} p/cm^2$. Fig. 6.6 represents the calculated cross-sections for MOS B as a function of the normalized Drain bias, for all energies used in the test campaign.

Tab. 6.10: Number of SEBs and estimated cross-section values for MOS B at KVI under proton irradiation. 3 DUTs were placed on the Test Board.

Proton Energy $[MeV]$	V_{DS} $[V]$	Φ_{step} $[p/cm^2]$	SEB	Cross-section $[cm^2]$		
				Real	Lower	Upper
186	72	$1.0 \cdot 10^{10}$	0	–	–	$1.23 \cdot 10^{-10}$
	81		6	$2.00 \cdot 10^{-10}$	$7.33 \cdot 10^{-11}$	$4.37 \cdot 10^{-10}$
	90		79	$2.63 \cdot 10^{-9}$	–	–
	99		532	$1.77 \cdot 10^{-8}$	–	–
124	72	$1.0 \cdot 10^{10}$	0	–	–	$1.23 \cdot 10^{-10}$
	81		6	$2.00 \cdot 10^{-10}$	$7.33 \cdot 10^{-11}$	$4.37 \cdot 10^{-10}$
	90		84	$2.80 \cdot 10^{-9}$	–	–
	99		605	$2.02 \cdot 10^{-8}$	–	–
80	72	$1.0 \cdot 10^{10}$	0	–	–	$1.23 \cdot 10^{-10}$
	81		0	–	–	$1.23 \cdot 10^{-10}$
	90		84	$2.80 \cdot 10^{9}$	–	–
	99		725	$2.42 \cdot 10^{-8}$	–	–

The indication that the SEB threshold voltage increases with lowering proton energy is supported in this case, too. Specifically, $V_{SEB|th}$ shifts from 81 V for 186 and 124 MeV protons to 90 V for 80 MeV protons. Additionally, the increment of the cross-section value for $V_{DS} = V_{Rated}$ with lower proton energies is even more distinct for MOS B. In this case, a 36% increment (from $1.77 \cdot 10^{-8}$ to $2.42 \cdot 10^{-8} cm^2$) is observed in σ_{sat} when the impinging energies passes from 186 MeV to 80MeV. Lastly, a good agreement of the SEB sensitivity under the effect of the neutrons of ChipIr and the 186 MeV protons of KVI is observed for MOS B, as well. From the test at ChipIr it was calculated that $V_{SEB|th} = 83V$ and $\sigma_{sat} = 1.33 \cdot 10^{-8} cm^2$,

compared to the respective values ($V_{SEB|th} = 81V$ and $\sigma_{sat} = 1.77 \cdot 10^{-8}$) that were extracted during the test with 186 MeV protons.

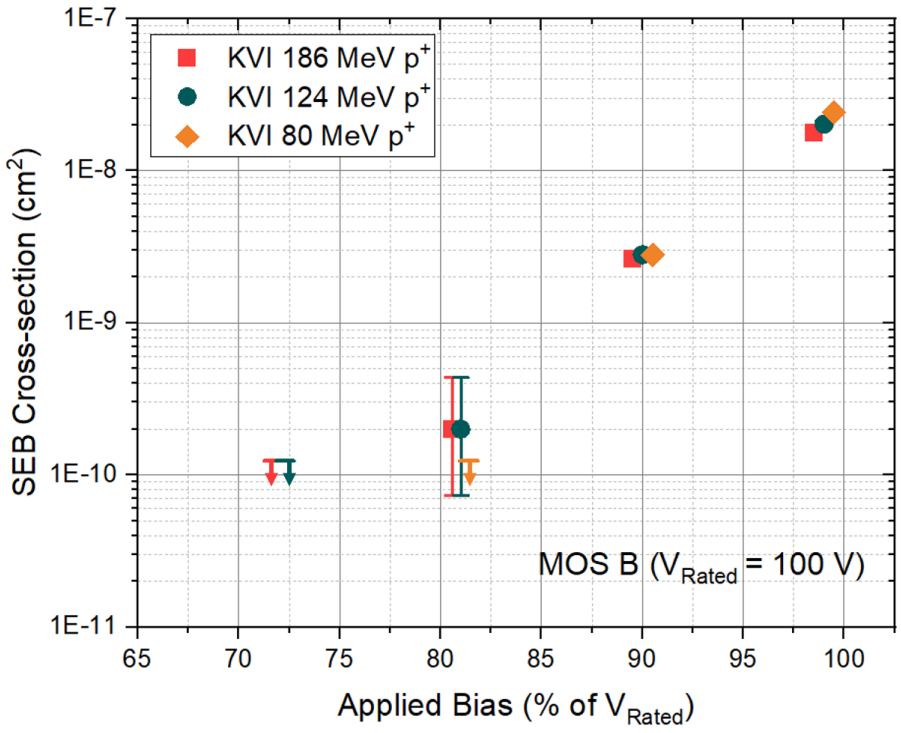
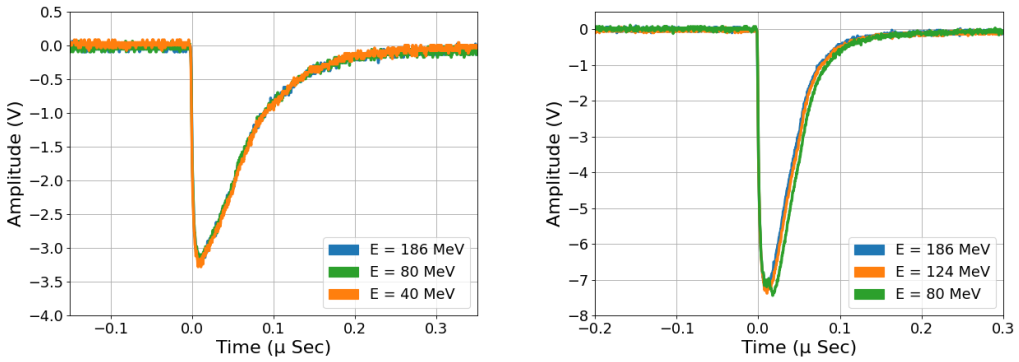


Fig. 6.6: Measured SEB cross-sections as a function of the normalized bias, for MOS B after irradiation with protons of different energies at KVI-CART. The scatter points that correspond to the same Applied Bias are artificially shifted from the actual x-value so that they are more distinguishable.

The registered SEB pulses for both MOS A and MOS B are represented in Fig. 6.7. For MOS A, the pulses collected for 40, 80, and 186 MeV irradiations with the devices biased at 54 V (98% of V_{Rated}) are compared. For MOS B, the pulses collected for 80, 124, and 186 MeV irradiations with the devices biased at 99 V (99% of V_{Rated}) are compared. No significant differences in amplitude or pulse-length were observed among the pulses corresponding to the same reference, stressing the fact that the beam conditions act on the SEB occurrence probability, but, once the SEB mechanism is activated, the development of the event is mainly driven by the circuit parameters.

When comparing the pulses produced by MOS A and MOS B under proton irradiation while biased at their rated voltage (Fig. 6.7) with the respective ones obtained at ChipIr (see Fig. 6.2d and Fig. 6.3d), a difference in their amplitude is evident. In particular, the average amplitude of the pulses obtained during the irradiation of MOS A for $V_{DS} = 54V$ is $-1.71V$ at ChipIr and $-3.23V$ at KVI, establishing a 88.8% absolute increase. In turn, the average amplitude of the pulses obtained during



(a) MOS A, $V_{DS} = 54V$ **(b)** MOS B, $V_{DS} = 99V$

Fig. 6.7: Signal waveforms corresponding to non-destructive SEBs observed for MOS A and MOS B under proton irradiation at KVI, for the highest bias and different proton energies

the irradiation of MOS B for $V_{DS} = 99V$ is $-3.36V$ at ChipIr and $-7.28V$ at KVI, establishing a 116.6% increase. However in both cases, the same Test Board and passive components were used, while the differences in the energy deposited by protons and neutrons are not capable of explaining such a drastic difference in the the size of the pulses.

Thus, the remaining difference of the two test campaigns is the type of connection between the Test Board and the oscilloscope. Both facilities provided patch panels with BNC connectors between the irradiation room and the control room, which were employed to establish the connection between the Test Board and the oscilloscope. It is expected that the two facilities used cables of different length and quality to connect the patch panels and transmit the acquired signals, even though specific information is not available. Cable losses introduced by the transmission lines could be a significant factor that affects the shape of the transient pulse [84]. Additionally, the transmission line can be considered as a passive component connected in series with the 1 nF decoupling capacitor, i.e. the main source of energy during the non-destructive SEB. Therefore, the characteristics of the cable can not only affect the transmission of the pulse but also its generation and evolution.

The SEB circuit-level model, presented in Subsection 4.6, has been employed to evaluate the effect of the transmission line's length on the shape of the transient pulse during the Burnout. Fig. 6.8 depicts the difference in the pulse's shape when the length of the transmission line was changed from 25m to 60m. The amplitude shifts from $-18.66V$ to $-9.09V$, establishing a decrease to the half of its initial value. In this case, a shift in the pulse's length is also observed that does not conform with the experimental data. Of course, it has to be noted that the circuit-level model is

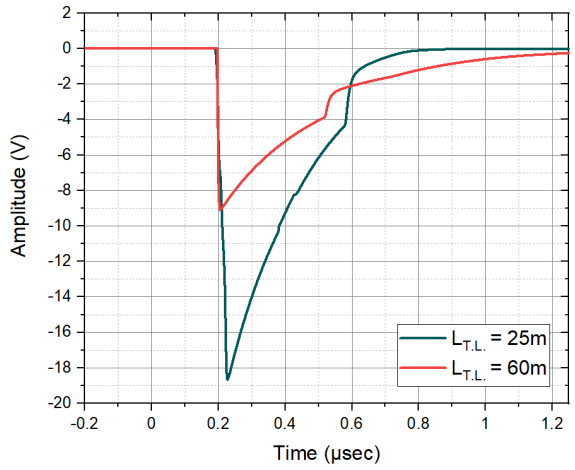


Fig. 6.8: Signal waveforms corresponding to non-destructive SEBs produced by SPICE simulations, for varying length (25 and 60 m) of the transmission line.

not a highly accurate or predictive tool, but a way to qualitatively assess the effect of the cables' length, instead.

6.3 Heavy Ion Irradiations

Power MOSFET references MOS A, MOS B, and MOS D were tested under the effect of different heavy ions with various energies and LETs at KVI-CART and GANIL. The experimental Runs performed are summarised in Tab. 6.11, including information about the tested reference, the ion species, their energy and LET, the range of the bias applied on the Drain, and the beam flux.

In summary, KVI irradiations were carried out with 26 and 14 MeV/u ^{40}Ar ions (5.5 and 8 $MeV \cdot cm^2/mg$, respectively), 90 MeV/u ^{12}C ions (0.24 $MeV \cdot cm^2/mg$) and ^{129}Xe ions (44 $MeV \cdot cm^2/mg$). ^{136}Xe was the only ion used in GANIL with energies of 46, 17 and 7 MeV/u (27, 44 and 59 $MeV \cdot cm^2/mg$, respectively). Non-destructive SEB events occurred during the majority of the experimental runs, apart from Run 7 and Run 9, highlighted with red color in Tab. 6.11. As it will be further discussed later, destructive events, which are postulated to be SEGR, took place during these runs. It should also be mentioned that, for all heavy ion irradiations the decapsulation of the samples was required to expose the silicon die to the ions.

Tab. 6.11: Experimental Runs performed with heavy ions at KVI and GANIL for the evaluation of SEE on power MOSFETs. The rows highlighted in red color show the Runs where destructive events took place.

Run	Device	Ion	Energy $[MeV/u]$	LET $[MeV \cdot cm^2/mg]$	Voltage Range $[V]$	Flux $[p/cm^2/s]$
1	MOS A	^{136}Xe	7	59	$23-29$	$2.0 \cdot 10^2 - 8.0 \cdot 10^3$
2			17	44	$25-32$	$2.0 \cdot 10^2 - 8.0 \cdot 10^3$
3			46	27	$27-41$	$2.0 \cdot 10^2$
4		^{40}Ar	14	8	$32-54$	$2.0 \cdot 10^2 - 2.0 \cdot 10^4$
5			26	5.2	$32-54$	$2.0 \cdot 10^2 - 2.0 \cdot 10^4$
6		^{12}C	90	0.24	$41-54$	$5.0 \cdot 10^6$
7	MOS B	^{129}Xe	21	44	63	$2.0 \cdot 10^4$
8		^{136}Xe	46	27	$23-63$	$4.0 \cdot 10 - 3.0 \cdot 10^2$
9	MOS D	^{129}Xe	21	44	90	$2.0 \cdot 10^4$

6.3.1 Results for MOS A

Table 6.12 gathers the number of SEBs observed for each bias step, for MOS A reference when tested with 14 MeV/u Argon ions, 26 MeV/u Argon ions, and 90 MeV/u Carbon ions at KVI. The estimated cross-sections are included in the table, as well.

A voltage threshold ($V_{SEB|th}$) is evident for all irradiation conditions, with no observed SEBs below it. In particular, MOS A showed a $V_{SEB|th} = 36V$ for the highest LET equal to 8 $MeV \cdot cm^2/mg$. The same value was observed for the intermediate LET of 5.2 $MeV \cdot cm^2/mg$, whereas the value increased up to 45 V when the LET was reduced to 0.24 $MeV \cdot cm^2/mg$. In turn, the calculated cross-section values for the highest applied voltage (σ_{SAT}) tended to increase when the LET of the heavy ions was also increased. Hence, an 82% reduction (from $1.81 \cdot 10^{-3}$ to $3.17 \cdot 10^{-4} cm^2$) was observed in σ_{SAT} when the ion LET passed from 8 to 5.2 $MeV \cdot cm^2/mg$. Accordingly, there was a reduction of nearly four orders of magnitude (from $3.17 \cdot 10^{-4}$ to $2.03 \cdot 10^{-8} cm^2$) in σ_{SAT} when the ion LET passed from 5.2 to 0.24 $MeV \cdot cm^2/mg$. However, this last drastic change can not be attributed just to the LET of the ions, as their atomic number Z was also decreased (from $Z = 40$ for the Argon ions to $Z = 12$ for the Carbon ions). A third factor that contributed to the change of the sensitive area, and is closely related to the change of LET and Z, is the change in the main mechanism of interactions between the

Tab. 6.12: Number of SEBs and estimated cross-section values for MOS A at KVI under irradiation with 14 MeV/u and 26 MeV/u Ar ions and 90 MeV/u C ions.

V_{DS} $[V]$	Φ_{step} $[p/cm^2]$	# of DUTs	SEB	Cross-section $[cm^2]$		
				Real	Lower	Upper
^{40}Ar Ions - 14 MeV/u - 8 $MeV \cdot cm^2/mg$						
32	$9.60 \cdot 10^6$	2	0	–	–	$1.93 \cdot 10^{-7}$
36	$9.60 \cdot 10^6$	2	55	$2.86 \cdot 10^{-6}$	–	–
41	$7.20 \cdot 10^5$	2	132	$9.17 \cdot 10^{-5}$	–	–
45	$1.20 \cdot 10^5$	2	109	$4.54 \cdot 10^{-4}$	–	–
50	$7.20 \cdot 10^4$	2	119	$8.26 \cdot 10^{-4}$	–	–
54	$3.60 \cdot 10^4$	2	130	$1.81 \cdot 10^{-3}$	–	–
^{40}Ar Ions - 26 MeV/u - 5.2 $MeV \cdot cm^2/mg$						
32	$9.60 \cdot 10^6$	2	0	–	–	$1.93 \cdot 10^{-7}$
36	$1.08 \cdot 10^7$	2	11	$5.09 \cdot 10^{-7}$	$2.50 \cdot 10^{-7}$	$9.12 \cdot 10^{-7}$
41	$1.20 \cdot 10^6$	2	50	$2.08 \cdot 10^{-5}$	$1.54 \cdot 10^{-5}$	$2.75 \cdot 10^{-75}$
45	$1.20 \cdot 10^6$	2	114	$4.75 \cdot 10^{-5}$	–	–
47	$1.20 \cdot 10^5$	2	21	$8.75 \cdot 10^{-5}$	$5.42 \cdot 10^{-5}$	$1.33 \cdot 10^{-4}$
50	$1.20 \cdot 10^5$	2	34	$1.42 \cdot 10^{-4}$	$9.79 \cdot 10^{-5}$	$1.98 \cdot 10^{-4}$
54	$1.20 \cdot 10^5$	2	76	$3.17 \cdot 10^{-4}$	–	–
^{12}C Ions - 90 MeV/u - 0.24 $MeV \cdot cm^2/mg$						
41	$2.00 \cdot 10^9$	1	0	–	–	$1.85 \cdot 10^{-9}$
45	$2.00 \cdot 10^9$	1	5	$2.50 \cdot 10^{-9}$	$8.0 \cdot 10^{-10}$	$5.85 \cdot 10^{-9}$
50	$2.00 \cdot 10^9$	1	12	$6.0 \cdot 10^{-9}$	$3.10 \cdot 10^{-9}$	$1.05 \cdot 10^{-8}$
54	$1.72 \cdot 10^9$	2	70	$2.03 \cdot 10^{-8}$	–	–

particles and the material, passing from direct ionization to indirect ionization. This is also supported by the fact that the sensitivity of MOS A under the effect of Carbon ions starts to resemble its sensitivity under the effect of protons and neutron, where indirect ionization is the dominant mechanism.

Accordingly, Table 6.13 gathers the number of SEBs observed for each bias step, for MOS A reference when tested at GANIL with Xenon ions of energies 7, 17, and 46 MeV/u and LETs equal to 59, 44 and 27 $MeV \cdot cm^2/mg$, respectively. The estimated cross-sections are included in the table, as well. For the tests with the two highest LETs, a SEB threshold voltage equal to 27 V was evident. As to what regards the test with the lowest LET of 27 $MeV \cdot cm^2/mg$, 2 SEB events were registered during the smallest bias step of 27 V. Considering that the accumulated fluence for that bias step was high enough ($1.0 \cdot 10^7 cm^2$), it can be extrapolated that $V_{SEB|th}$ would be close, and slightly less than 27 V for this LET, as well. Considering now the cross-section value for the highest applied bias, it converges for all ion energies to

Tab. 6.13: Number of SEBs and estimated cross-section values for MOS A at GANIL under irradiation with 46, 17 and 7 MeV/u Xe ions.

V_{DS} $[V]$	Φ_{step} $[p/cm^2]$	# of DUTs	SEB	Cross-section $[cm^2]$		
				Real	Lower	Upper
^{136}Xe Ions - 7 MeV/u - 59 $MeV \cdot cm^2/mg$						
23	$9.00 \cdot 10^5$	3	0	–	–	$1.37 \cdot 10^{-6}$
25	$1.00 \cdot 10^7$	3	0	–	–	$1.23 \cdot 10^{-7}$
27	$5.00 \cdot 10^5$	3	16	$1.07 \cdot 10^{-5}$	$6.27 \cdot 10^{-6}$	$1.73 \cdot 10^{-5}$
28	$3.00 \cdot 10^5$	3	93	$1.03 \cdot 10^{-4}$	–	–
29	$1.05 \cdot 10^5$	3	212	$6.70 \cdot 10^{-4}$	–	–
^{136}Xe Ions - 17 MeV/u - 44 $MeV \cdot cm^2/mg$						
25	$9.78 \cdot 10^6$	3	0	–	–	$1.26 \cdot 10^{-7}$
27	$1.00 \cdot 10^7$	3	19	$6.33 \cdot 10^{-7}$	$3.83 \cdot 10^{-7}$	$9.87 \cdot 10^{-7}$
28	$3.00 \cdot 10^6$	4	93	$7.75 \cdot 10^{-6}$	–	–
30	$2.08 \cdot 10^5$	4	203	$2.43 \cdot 10^{-4}$	–	–
32	$6.82 \cdot 10^4$	4	210	$7.70 \cdot 10^{-4}$	–	–
^{136}Xe Ions - 46 MeV/u - 27 $MeV \cdot cm^2/mg$						
27	$1.0 \cdot 10^7$	3	2	$6.67 \cdot 10^{-8}$	$6.67 \cdot 10^{-9}$	$2.40 \cdot 10^{-7}$
30	$1.0 \cdot 10^7$	3	152	$5.07 \cdot 10^{-6}$	–	–
32	$3.0 \cdot 10^5$	4	29	$2.42 \cdot 10^{-5}$	$1.62 \cdot 10^{-5}$	$3.47 \cdot 10^{-5}$
33	$2.72 \cdot 10^5$	4	202	$1.86 \cdot 10^{-4}$	–	–
41	$6.0 \cdot 10^3$	4	20	$8.33 \cdot 10^{-4}$	$5.08 \cdot 10^{-4}$	$1.28 \cdot 10^{-34}$

an average around $7.50 \cdot 10^{-4} cm^2$. However, it can be observed that for irradiations with Xe ions of higher LET, σ_{SAT} is reached for smaller applied bias, i.e. 29 V for 59 $MeV \cdot cm^2/mg$, 32 V for 44 $MeV \cdot cm^2/mg$, and 41 V for 27 $MeV \cdot cm^2/mg$. Lastly, neither of the tests went too close to 55 V, the rated voltage of MOS A, mainly because of the saturation of the acquisition system, even for very low fluxes. A sensitive area close to the whole area of the silicon die can be expected at V_{Rated} for the highest LETs.

The estimated cross-sections as a function of the normalized Drain bias are depicted in Fig. 6.9 for all tests and ions, both at KVI and at GANIL. The visualization of the data helps to identify a particular trend: the fact that $V_{SEB|th}$ seems to have a strong dependence on the ion species, rather than the ion's energy or LET. This comes in agreement with Liu's observations in [41], who notices that the determining factor of the SEB failure voltage is the test ion species. Additionally, it is clear on Fig. 6.9 that curves which correspond to higher LETs are shifted towards the left. This can be explained in a better way by defining V_{SAT}, i.e. the voltage for which

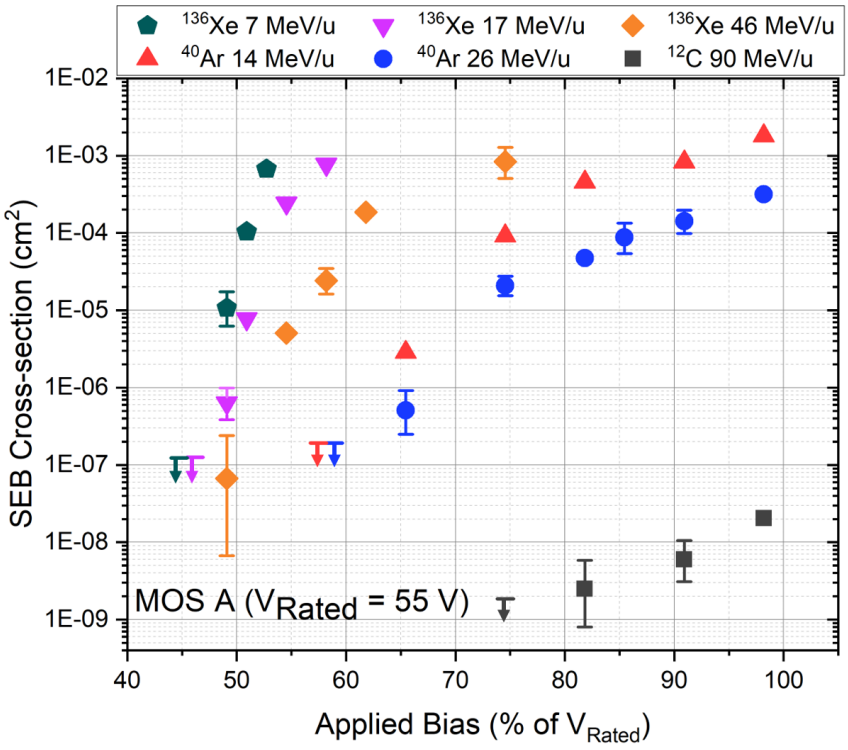


Fig. 6.9: Measured SEB cross-sections as a function of the normalized bias, for MOS A after irradiation with heavy ions of different energies at KVI and GANIL.

$\sigma_{SEB} > 1 \cdot 10^{-4}$. In Fig. 6.10, V_{SAT} for each irradiation is plotted as a function of the ion's LET, showing a strong asymptotic dependence between these two values.

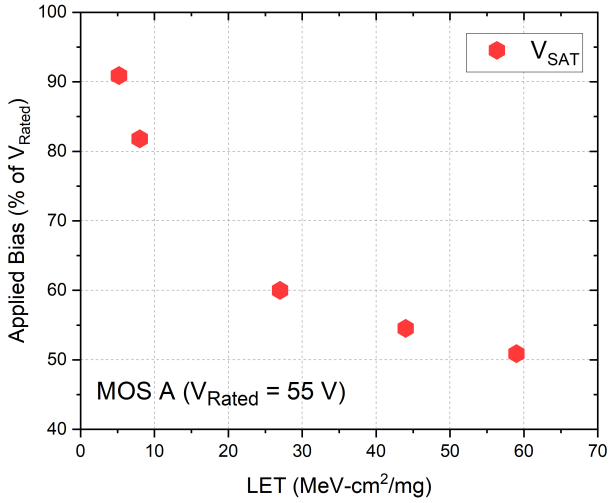


Fig. 6.10: Normalized V_{SAT}, the bias for which $\sigma_{SEB} > 1 \cdot 10^{-4}$, as a function of the ion's LET, for MOS A after irradiation with heavy ions at GANIL and KVI.

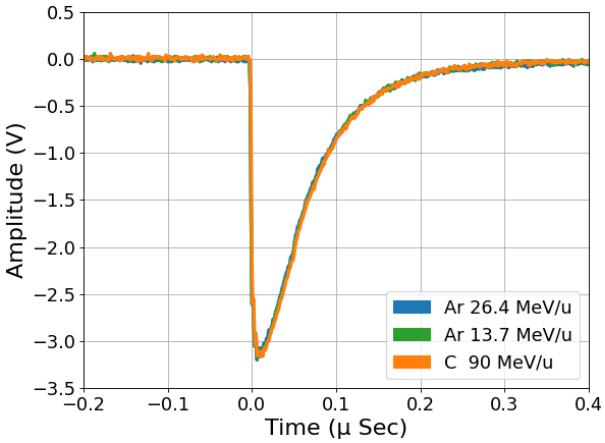


Fig. 6.11: Signal waveforms corresponding to non-destructive SEBs observed for MOS A under irradiation with heavy ions at KVI and $V_{DS} = 54V$.

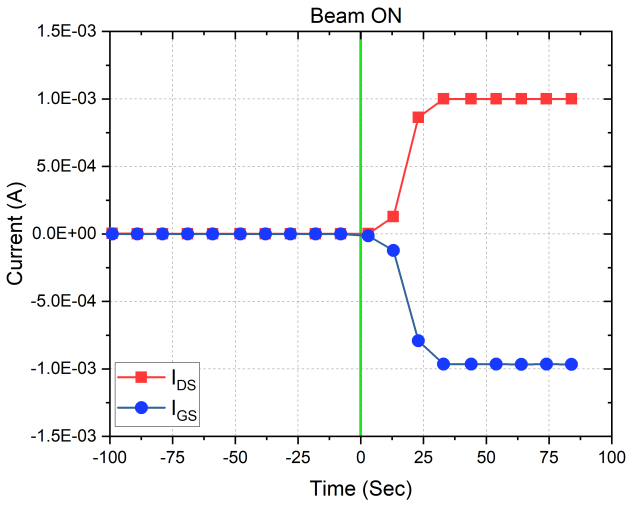
Lastly, the pulses registered by the oscilloscope for MOS A ($V_{DS} = 54V$), when irradiated with Argon and Carbon ions at KVI, are shown on Fig. 6.11. As before, the pulses are the same in shape and size, proving that, once it has been triggered, the evolution of the Burnout is independent of the ion species or its energy and it is fully driven by the circuit features.

6.3.2 Results for MOS B and MOS D

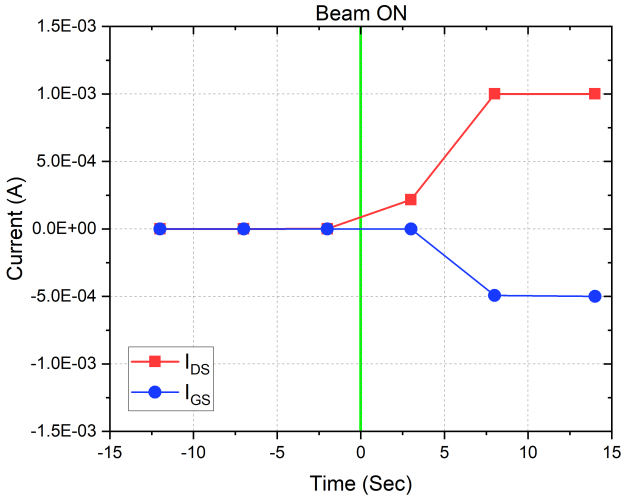
During the test campaign with heavy ions at KVI-CART, samples of MOS B and MOS D were irradiated with 22 MeV/u Xenon ions with LET equal to 44 $MeV \cdot cm^2/mg$. In both cases, a steep increase of the measured currents, I_{DS} and I_{GS}, was registered in the two SMUs as soon as the beam was turned on. This was an immediate indication that a destructive SEE took place. The current increment registered for MOS B and MOS D is presented in Fig. 6.12a and Fig. 6.12b, respectively.

Specifically, during the irradiation of MOS D, three samples were placed on the test board and V_{DS} was set equal to 90 V, i.e. 90% of V_{Rated} ($V_{GS} = 0$). In Fig. 6.12, t=0 sec corresponds to the moment the beam was turned-on and it can be observed that I_{DS} started increasing before I_{GS} did, reaching the compliance of the SMU (1 mA) approximately 8 sec later. I_{GS} did not reach the compliance of the SMU and was equal to half the value of I_{DS} (0.5 mA) when the experimental run was aborted. Similarly, during the irradiation of MOS B, three samples were placed on the test board and the Drain bias was set equal to 63 V, i.e. 63% of V_{Rated}. In this case, it can be observed that I_{DS} and I_{GS} reached the SMU's compliance ($1mA$) simultaneously and approximately 33 sec after the beam was turned on. The increase of current

flowing through the Gate classifies the events as SEGR, as it was explained in detail in Sec.4.2.



(a) MOS B



(b) MOS D

Fig. 6.12: I_{DS} and I_{GS} plotted against time during the irradiation of MOS B and MOS D with 22 MeV/u Xenon ions at KVI. t=0 sec corresponds to the moment the heavy ion beam was turned on. The steep increase of I_{GS} in both cases is associated with SEGR.

For irradiation test with MOS B, the experimental run was immediately interrupted, and without changing the bias conditions, the first step was to isolate each one of the DUTs, by means of the relay switches employed on Test Board 2. This was done to see whether the current increase was similar for each sample. Indeed, I_{DS} and I_{GS} had reached the compliance value in all three samples and remained the same even

after the beam was turned off. The characterization of the DUTs followed, in order to observe the changes in the electrical characteristics before and after a SEGR.

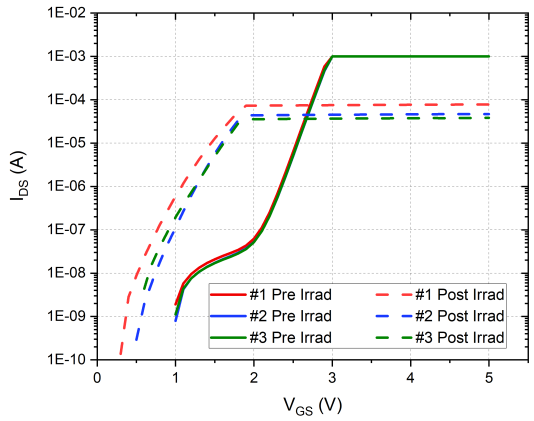
Specifically, Fig. 6.13a shows the plot of the transfer characteristic of MOS B, which is used for the estimation of V_{th}. It is calculated that before irradiation $V_{th} = 2.8V$, which is close to the typical value of 3 V mentioned in the data-sheet. On the contrary, after irradiation, I_{DS} plateaus between 50 and 100 μA, even though the compliance of the SMU was set equal to 1 mA. Additionally, a 1.1 V shift of the graphs towards the left is observed, setting V_{th} post irradiation equal to 1.7 V. The shift of V_{th} is expected and attributed to TID effects, as explained in Sec. 3.2.1. However, the plateau of I_{DS} at a lower lever is related to the Gate Rupture and the fact that the destroyed oxide can not support anymore an electric field high enough to create an inversion layer.

Furthermore, Fig. 6.13b shows the conduction characteristic curve, while V_{GS} is set equal to 10 V. Before the irradiation of the DUTs, and since V_{GS} is significantly higher than V_{th}, the MOS B samples are turned-on and as soon as V_{DS} becomes larger than 0.5 V, I_{DS} reaches the SMU's compliance (0.25 mA). On the contrary, after the irradiation of the DUTs, current starts flowing through the Drain of the samples only after V_{DS} becomes higher than 0.7V, while it promptly plateaus between 10 μA and 100 μA. This converges with the plateau seen in Fig. 6.13a.

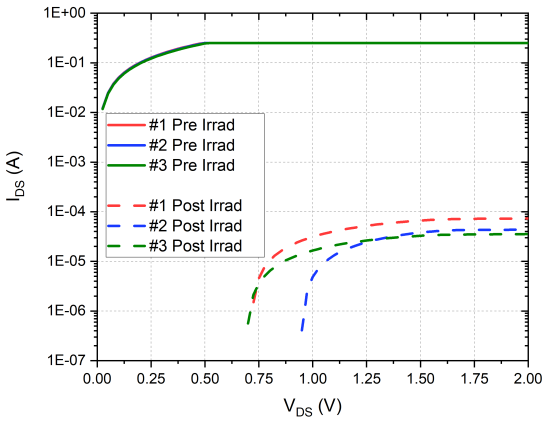
Lastly, Fig. 6.13c shows the evolution of I_{DS} as a function of V_{DS}, while V_{GS} is set equal to 0. Therefore, the MOS B samples are in their off-state, and the dark current I_{DSS} is equal to the Drain current at V_{Rated}, i.e. 100V for MOS B. Before irradiation, $I_{DSS} = 4\mu A$ for DUT #1 and DUT #3 and $I_{DSS} = 100\mu A$ for DUT #2. Taking into consideration the decapsulation of the devices, and the subsequent increase of the photocurrents, the above-mentioned values of I_{DSS} are justified when compared to the value of $I_{DSS} = 1\mu A$ that is given in the data-sheet. On the other hand, after irradiation, I_{DS} at 100V is limited by the compliance of the SMU, indicating that I_{DSS} would be significantly higher than 1 mA.

Moving on, MOS B was also tested under the effect of 46 MeV/u Xenon ions at GANIL. In this case, no destructive events were observed and Table 6.14 gathers the accumulated fluence, along with the number of SEBs observed for each bias step. The estimated cross-section values are listed in the table, as well. SEBs were registered for an applied Drain bias as low as 23 V (i.e. 23% of V_{Rated}) and thus it was not possible to define $V_{SEB|th}$ for these experimental conditions. The estimated cross-section at the highest applied bias (33 V or 33% of V_{Rated}) was equal to $5.03 \cdot 10^{-4} cm^2$. The calculated cross-section values as a function of the normalized Drain bias are also depicted in Fig. 6.14. Lastly, a bias step equal to 63% of V_{Rated} was also applied on the Drain of the DUTs. Several non-destructive SEB events

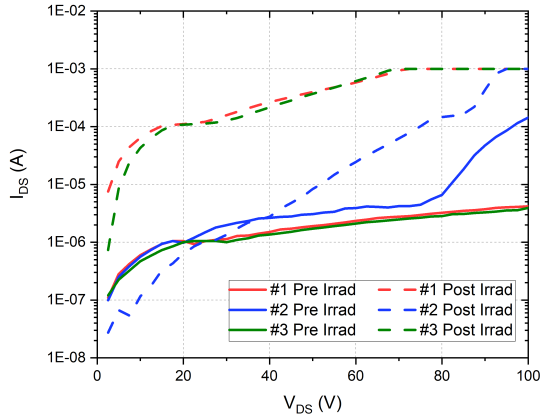
were registered, but their rate was too high to get an accurate estimation of the cross-section.



(a) $I_{DS} = f(V_{GS})$ for $V_{DS} = V_{GS}$.



(b) $I_{DS} = f(V_{DS})$ for $V_{GS} = 10V$.



(c) $I_{DS} = f(V_{DS})$ for $V_{GS} = 0V$.

Fig. 6.13: Electrical characterization plots of three MOS B samples before and after their irradiation with 22 MeV/u Xenon ions at KVI.

Tab. 6.14: Number of SEBs and estimated cross-section values for MOS B at GANIL under irradiation with 46 MeV/u Xenon heavy ions. 3 DUTs were placed on the Test Board.

^{136}Xe Ions - 46 MeV/u - 27 $MeV \cdot cm^2/mg$					
V_{DS} $[V]$	Φ_{step} $[p/cm^2]$	SEB	Cross-section $[cm^2]$		
			Real	Lower	Upper
23	$3.00 \cdot 10^5$	3	$3.33 \cdot 10^{-6}$	$6.67 \cdot 10^{-7}$	$9.78 \cdot 10^{-6}$
27	$1.50 \cdot 10^5$	27	$6.00 \cdot 10^{-5}$	$3.96 \cdot 10^{-5}$	$8.71 \cdot 10^{-5}$
30	$1.00 \cdot 10^5$	62	$2.07 \cdot 10^{-4}$	–	–
32	$7.11 \cdot 10^4$	66	$3.10 \cdot 10^{-4}$	–	–
33	$2.19 \cdot 10^4$	33	$5.03 \cdot 10^{-4}$	$3.46 \cdot 10^{-4}$	$7.06 \cdot 10^{-4}$

It is worth mentioning that the SEB sensitive area of MOS B when irradiated with 46 MeV/u Xe ions ($V_{DS} = 23\%\ of\ V_{Rated}$) is more than four orders of magnitude larger than its SEB sensitive area when exposed to neutrons or protons ($V_{DS} = 99\%\ of\ V_{Rated}$). Additionally, as to what regards SEGR sensitivity of a power MOSFET, it is indicated that the ion's LET plays a major role. Both at KVI and at GANIL, MOS B samples were irradiated with Xenon ions while biased at 63% of their rated voltage. In the first case, the LET was equal to 44 $MeV \cdot cm^2/mg$ and a postulated SEGR took place as soon as the beam was turned on. In the latter case, the LET was equal to 27 $MeV \cdot cm^2/mg$ and only non-destructive SEBs were registered.

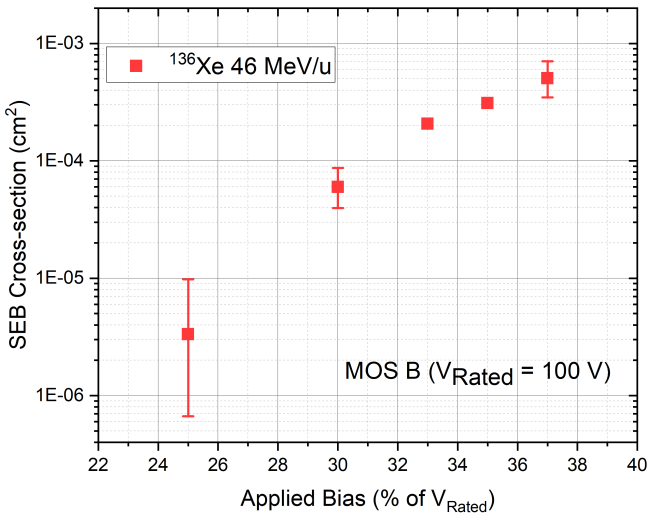


Fig. 6.14: Measured SEB cross-section as a function of the normalized bias, for MOS B after irradiation with 46 MeV/u Xenon heavy ions at GANIL.

7 Conclusions and Outlook

7.1 Thesis Summary

The present thesis is devoted to the experimental evaluation of the SEE sensitivity of commercial silicon power MOSFETs, depending on their bias and technology, as well as the radiation environment. A series of irradiation tests, that expand over a range of species, energies, and LET values, has been performed on selected power MOSFET references, representative of different technologies and characteristic performances. The metrics used to evaluate their SEE sensitivity are their cross-section at different voltage bias ($\sigma_{SEE}(V_{DS})$) and the minimum Drain bias required to start observing SEEs ($V_{SEE|th}$). Specifically, the SEEs that affect the behavior of power MOSFETs and have been studied in the scope of this thesis are SEBs and SEGRs.

To do so, an experimental setup that allows for the detection of both SEBs and SEGRs, while its able to distinguish between them, has been employed. The setup enables the protection of power MOSFETs against SEBs, so that the same samples can be used for the whole experiment, although their destruction is unavoidable once a SEGR had been initiated. Additionally, the setup allows for the counting of SEB events, as well as the saving of a representative pulse. Further improvements have been made in order to enable the on-line electrical characterization of the tested references, the isolation of failing devices, and the distinction between a destructive SEB and a SEGR.

Most of the SEE observed corresponded to non-destructive SEBs, proving the efficiency of the circumvention circuit, although destructive SEBs and SEGRs were also observed. Some of the tested parts were completely immune to SEEs for most irradiation conditions. The selection of the auxiliary components, especially of R_D and C1, is critical, since they might completely suppress the SEB generation or they might not provide adequate protection. As to what regards the SEB representative pulse, it has been confirmed that its shape does not depend on the radiation conditions, as the ionizing particle just triggers the turn-on of the parasitic BJT. The evolution of the phenomenon is more dependent on the technology of the power MOSFET and the characteristics of the circuit's passive components, including the transmission line. A limitation of the setup would be its acquisition rate, since in some cases

an underestimation of the cross-section was observed, even for the lowest particle flux.

It has also been observed that the references rated for higher voltages become SEB sensitive when a smaller percentage of their V_{Rated} is applied on their Drain, while their asymptotic cross-section values are also higher, establishing this was a correlation between V_{Rated} and SEB sensitivity. Furthermore, there is a good agreement in the radiation response of the DUTs under the effect of the mixed particle field, the neutron spallation beam and the high-energy proton beam. This suggests that the same mechanism takes place in the production of SEBs under proton and neutron irradiations. Neutrons can only produce SEBs by indirect ionization, and the fact that the cross section for protons is very similar, seems to indicate that direct ionization does not play a relevant role in SEB production with protons. Especially for protons, the cross-section and $V_{SEB|th}$ values measured for each device were similar for energies above 80 MeV. However, for lower energies an increase of both $V_{SEB|th}$ and of the cross-section at V_{Rated} was observed, possibly connected to the prevalence of secondary interactions.

Heavy ions are drastically more dangerous to power MOSFETs than protons or neutrons. For example, when irradiating one of the references with ions of the highest LET, $V_{SEB|th}$ was almost half the value measured with high-energy protons. Operating this reference without risk of failure (in its safe-operating area) in a heavy ions environment would require its significant de-rating ($V_{DS} \ll V_{Rated}$). Similarly, the cross-section at the highest voltage step was more than 5 orders of magnitude larger, meaning that practically the whole active area of the device was sensitive to SEE. It is also observed that, for heavy ion tests, $V_{SEB|th}$ depends mainly on the ion species, while the slope of the of the graph that corresponds to the cross-section as a function of the applied bias strongly depends on the ion's LET. The only SEGR events observed, also took place during irradiation with heavy ions, causing the destruction of the devices as soon as the beam was turned on. The electrical characterization of the samples afterwards confirmed that the current flowing while they were turned-on was significantly lower than the expected, indicating that despite the applied Gate bias, an inversion layer could not be created at the channel region. Therefore, the high impedance of the Gate, the main feature of a power MOSFET, was destroyed.

7.2 Future Work

Even though the study of SEE on power MOSFETs is not a recent topic of research interest, the rapid advances in the semiconductor microelectronic industry, as well as the increasing application requirements in radiation environments result in a

continuous need for evaluation of the SEE sensitivity both on a theoretical and on an experimental level. Following up on the topic of this thesis, there are three potential research directions that would be of interest.

The first direction could be the continuation of the experimental tests with new power MOSFET technologies of different operational characteristics. Since the information provided by the manufacturers are typically limited, this endeavor could be supported by reverse engineering techniques, so that a meaningful association of SEE sensitivity with technology could be made. Furthermore, tests in a wider range of radiation environments could also be pursued. Thanks to the developments in the experimental board, that were performed in the scope of this thesis, the setup is ready for testing new components, as it is more versatile, simpler to use, and with its limitations better understood.

The second direction could be related to the evaluation of how the experimental setup affects the measurements. It has to be confirmed that the samples which did not experience any events under most irradiation conditions did so because they are radiation tolerant and not because the circumvention circuit did not provide enough energy to them. It is worth checking if the same behavior would be noticed with larger capacitors connected on the circuit. In turn, it could be further investigated whether another combination of passive components would prevent the destruction of the samples that could not be protected from SEBs.

Lastly, the third direction is related to the simulation of SEEs and particularly SEBs on power MOSFETs. Some efforts have been made in this study to further explore the possibilities of the SEB circuit-level model, integrated into the protective circuit, however significant limitations were observed due to the absence of modeling of secondary events. An alternative to that could be the creation of a mixed-mode simulation, where a TCAD model of the power MOSFET would be connected to the rest of the compact model-based circuit. The TCAD simulation of SEBs on power MOSFETs has already been explored, but not with the sample protected from a non-destructive circuit. For the parameter tuning of such a mixed-mode simulation, the data gathered from the irradiation campaigns presented in this thesis, and especially the shape of the transient SEB-representative pulses, would be particularly useful.

7.3 Contributions

This thesis has been completed in the framework of a Technical Studentship at CERN from March 2019 until April 2020 and the work presented is attributed to both personal and collaborative activities. Personal efforts were focused on increasing

the efficiency of the experimental setup both on a hardware and on a software level. Hardware improvements included the introduction of Test Board 2 and the designing and building of the Relays-Control board in order to reduce the complexity of the experimental methodology and facilitate the acquisition of more relevant data. Software improvements were focused on the efficient remote control of all instruments and resolving of unexpected errors. The goal was to create the simplest possible process to be followed by the experimenters. Technical support was provided during the irradiation campaigns, while the organization, analysis and visualization of the gather data were also among individual responsibilities. Furthermore, early efforts were made to explore the potential of the circuit−level model of SEBs and to run SPICE simulations, complementarily to the experimental data. Part of the work performed during this thesis was presented by the author as a poster contribution at the 15th International School on the Effects of Radiation on Embedded Systems for Space Applications (SERESSA 2019) under the title:

"**Study of the SEB Sensitivity of Commercial Silicon Power MOSFETs through Non-Destructive Measurements**" Papadopoulou, A.; Fernández-Martínez, P.; Kastriotou, M.; Danzeca, S.; Foucard, G.; Tsiligiannis, G.; García Alía, R.

Lastly, the author contributed to a data workshop paper (REDW-117) for the Radiations Effects on Components and Systems 2020 (RADECS 2020) conference under the title:

"**SEE Testing on commercial power MOSFETs**" Fernández-Martínez, P.; Papadopoulou, A.; Danzeca, S.; Foucard, G.; García Alía, R.; Kastriotou, M.; Cazzaniga, C.; Tsiligiannis, G.; Gaillard, R.

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List of Figures

List of Tables