Digital Power Consumption Estimations for CHIPIX65 Pixel Readout Chip

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1 Introduction

New hybrid pixel detectors with improved resolution capable of dealing with hit rates up to 3 GHz/cm^2 will be required for future High Energy Physics experiments in the Large Hadron Collider (LHC) at CERN. Given this, the RD53 collaboration works on the design of the next generation pixel readout chip needed for both the ATLAS and CMS detector phase 2 pixel upgrades. For the RD53 demonstrator chip in 65nm CMOS technology, different architectures are considered. In particular the purpose of this work is estimating the power consumption of the digital architecture of the readout ASIC developed by CHIPIX65 project of the INFN National Scientific Committee. This has been done with modern chip design tools integrated with the VEPIX53 simulation framework that has been developed within the RD53 collaboration in order to assess the performance of the system in very high rate, high energy physics experiments.

2 Average power estimations

The evaluation of the digital power consumption of the CHIPIX65 readout chip is focused on a single 4 by 4 pixel region (PR) of the matrix of 4096 pixels that is divided into 16 macro-columns, each of 16 PRs. The power is averaged over 500μs chosen as the simulation window in which the VCD files needed for the calculation are extracted. In fact, these files provide to the power signoff tool information about the switching activity of the logic being tested. Different activity conditions are taken into account:

- with hits (3GHz/cm^2 hit rate) and triggers (1MHz trigger rate);
- without hits and triggers (only clock sent to the logic);
- with hits (3GHz/cm^2 hit rate) and no triggers;
- with triggers (1MHz trigger rate) but no hits;

This allows us to understand the impact of hit rate, trigger rate and only the clock on power. Concerning the scenario with which the tools are configured it is the typical multi-mode multi-corner (MMMC) that defines the operative conditions and the reference libraries provided by the foundry:

- RC Corner: RC_TYPICAL (qrcTechFile);
- Liberty Timing Library: tcbn65lptc_ecsm;
- Operating Conditions: VDD 1.2V, temperature 25 °C;

Details on the power consumption in different activity conditions are reported in table1 where digital logics for both the analog front-ends developed by Torino (TO) and Pavia (PV) INFN Institutes are considered (in equal parts in the pixel array). The very high power consumption on the clock tree is mainly due to the buffers: in reference to the normal operative condition with hits and triggers, the buffers need 50.4% (68μW) of the total amount of power for TO and 39.5% (47.83μW) for PV. Most of the remaining clock tree power refers to the ripple counters of the time over threshold (ToT) and the pixel fixed dead time (15CCs) that the tool includes as clock tree elements. When only the

	Logic		Clock Tree		Total		per Pixel	
	TO	PV	TO	PV	TO	PV	TO	PV
Hits and Triggers	42.34μW (31.38%)	53.22μW (43.94%)	92.61μW (68.62%)	67.88μW (56.06%)	**134.9μW**	**121.1μW**	8.43μW	7.57μW
Only Clock	35.6μW (27.95%)	45.92μW (40.98%)	91.7μW (72.05%)	66.18μW (59.02%)	**127.3μW**	**112.1μW**	7.95μW	7μW
No hits and Triggers	36.3μW (28.35%)	46.62μW (41.35%)	91.7μW (71.65%)	66.18μW (58.65%)	128μW	112.8μW	8μW	7.05μW
Hits and No Triggers	37.83μW (29.18%)	48.19μW (42.1%)	91.77μW (70.82%)	66.31μW (57.9%)	129.6μW	114.5μW	8.1μW	7.16μW

Table 1: Digital average power estimations in different activity conditions for the logics relating to both the analog front-ends.

clock is sent to the logic there isn't a significant decrease in power due to the clock because the clock is not gated into the hit logic of the pixels.

When a particle hits the pixels, the charge collected by the sensor is digitalized as ToT provided by a counter into the hit logic of each pixel. The table3 reports a comparison between the digital power consumptions of 4 by 4 PRs that store ToT values with 4bits and 5bits. The power gain using one flip flop less for each ToT counter is almost 5% for both the logics under test and the post placement density gain is 6%.

	Density	
	TO	PV
4bits-TOT	71.14%	66.12 %
5bits-TOT	77.47%	72.3 %

Table 2: Post-placement density check.

		Hits and Triggers			Only Clock		
		Logic	Clock Tree	Total	Logic	Clock Tree	Total
TO	4bits	40.05μW (31.27%)	88.05μW (68.73%)	**128.1μW**	33.24μW (27.61%)	87.15μW (72.39%)	**120.4μW**
	5bits	42.34μW (31.38%)	92.61μW (68.62%)	**134.9μW**	35.6μW (27.95%)	91.7μW (72.05%)	**127.3μW**
PV	4bits	49.98μW (43.74%)	64.3μW (56.26%)	**114.3μW**	42.97μW (40.81%)	62.32μW (59.19%)	**105.3μW**
	5bits	53.22μW (43.94%)	67.88μW (56.06%)	**121.1μW**	45.92μW (40.98%)	66.18μW (59.02%)	**112.1μW**

Table 3: Comparison between the digital average power estimations considering 4bits and 5bits for the TOT.

3 Dynamic power analysis

Focusing on the logic for the TO analog front-end, because of the higher average power consumption, we can observe the power evolution over time with the use of power profiles. It is necessary to know the maximum current/power visible to the serial powering system and evaluate the efficiency of the on-chip decoupling. Power variations are averaged over different time resolutions (1ns, 25ns, 100ns, 1μs, 10μs) in a simulation window of 500μs and all the activity conditions have been analyzed. In the right side of each figure there is information on the maximum percentage of the average power reachable by the peaks and in the upper right side of each histogram the maximum power needed by the PR being tested. As expected and shown in the following figures the hits (3 GHz/cm^2 hit rate) have the most impact on peaks while in the activity condition without hits and triggers we have lower peaks since only the clock is sent to the logic.

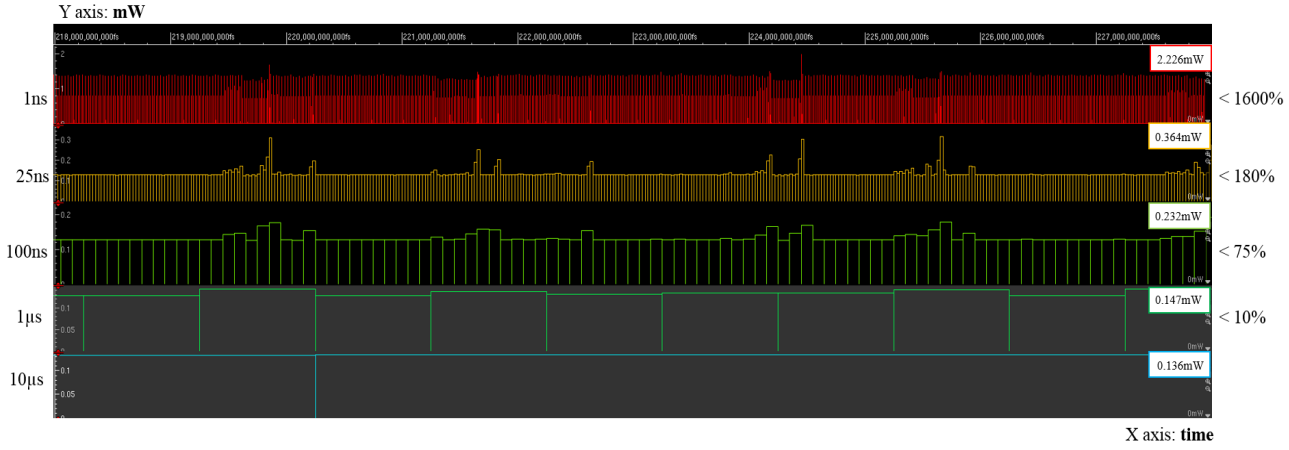

Figure 1: Power profiles in the activity condition with hits and triggers (zoom on shorter simulation window).

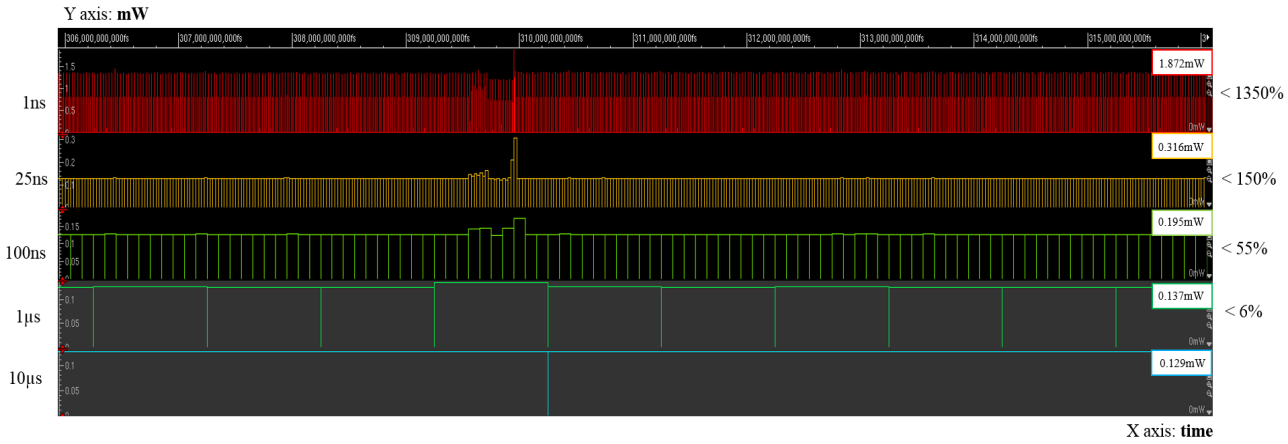

Figure 2: Power profiles in the activity condition with hits and no triggers (zoom on shorter simulation window).

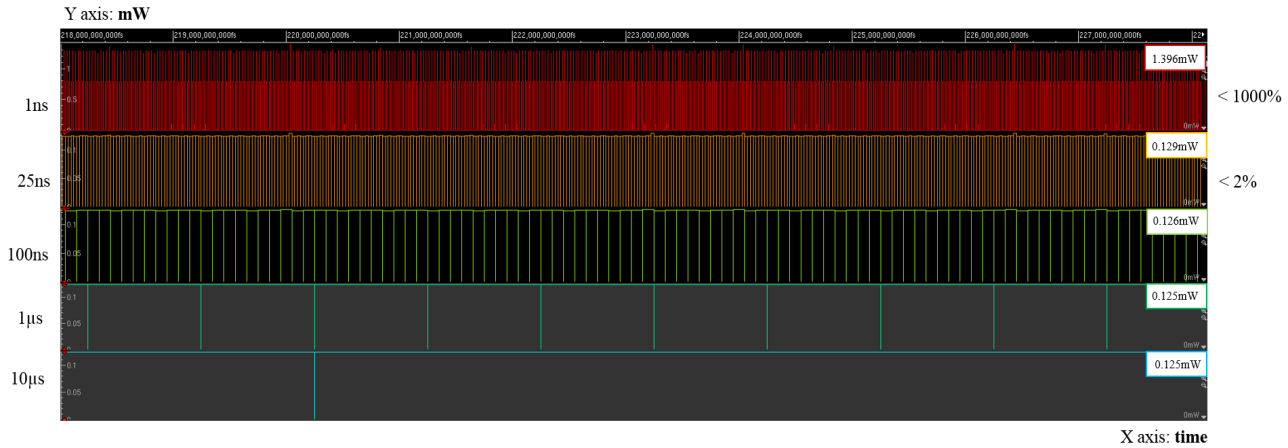

Figure 3: Power profiles in the activity condition with only clock (zoom on shorter simulation window).

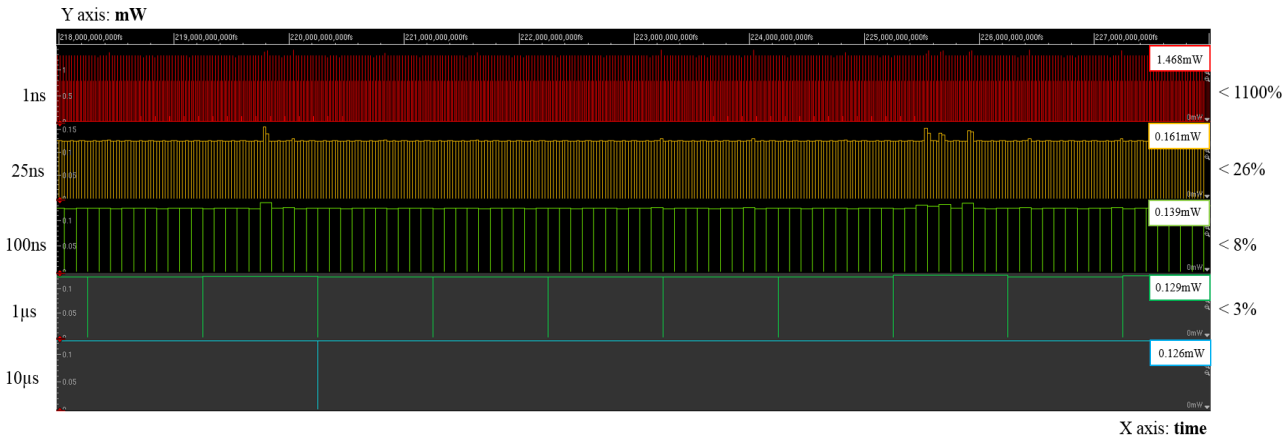

Figure 4: Power profiles in the activity condition with no hits and triggers (zoom on shorter simulation window).

4 Conclusions

The main target in the design of the next generation of pixel readout chip for the ATLAS and CMS detector phase 2 pixel upgrades is the lowest possible power consumption which can assure not significant power fluctuation. Therefore, average and dynamic power consumption estimations for the extremely high hit rates required are useful to guide digital design optimization and studying the reliability of the power scheme at system level.