DISSERTATION
submitted to the
Combined Faculties for the Natural Sciences and for Mathematics
of the Ruperto-Carola University of Heidelberg, Germany
for the degree of
Doctor of Natural Sciences

presented by
Dipl.-Phys. Daniel Baumeister
born in
Aschaffenburg, Germany

Oral examination: 29.1.2003

Development and Characterisation of a Radiation Hard Readout Chip for the LHCb-Experiment

Referees: Prof. Dr. Werner Hofmann
Prof. Dr. Johanna Stachel

für Katja

Zusammenfassung

Innerhalb der vorliegenden Arbeit wurden Teile des strahlenharten Auslesechips *Beetle* entwickelt und sowohl vor als auch nach Bestrahlung charakterisiert. Zu den Entwicklungen zählte der analoge Speicher mit dem dazugehörigen Auslese-Verstärker, sowie Komponenten der digitalen Steuerlogik. Es wurde eine zum I^2C-Standard kompatible Schnittstelle sowie die Logik zur Steuerung der Auslese eines Ereignisses implementiert. Der konsistente Einsatz von dreifach-redundanter Logik zusammen mit einer Fehler-Selbstkorrektur gewährleistet die Robustheit des *Beetle* Chips gegenüber Zustandsänderungen eines Speicherelements, die durch ein einzelnes Teilchen induziert werden (Single-Event Upset).
Der *Beetle* ASIC ist ein 128 Kanal Auslesechip für Silizium-Streifen Detektoren. Die analoge Eingangsstufe besteht aus einem ladungsempfindlichen Vorverstärker und einem CR-RC Pulsformer. Die äquivalente Rauschladung beträgt $\mathrm{ENC} = 497\,\mathrm{e}^- + 48.3\,\mathrm{e}^-/\mathrm{pF}\cdot\mathrm{C}_{in}$. Der analoge Speicher ist eine Kapazitäts-Matrix, der eine Latenzzeit von maximal $4\,\mu$s gewährleistet. Die 128 Kanäle werden über einen Stromtreiber in 900 ns vom Chip übertragen. Neben dem Signalpfad, der durch den analogen Speicher führt, stellt der *Beetle* Chip eine schnelle Diskriminierung des geformten Eingangspulses bereit. Eine Bestrahlung des *Beetle1.1* bis 45 Mrad zeigte kein funktionales Versagen und nur leichte Verschlechterungen im analogen Verhalten. Die Chip-Version 1.2 erfüllt die Anforderungen des Vertex Detektors (VELO), des Inneren Spurdetektors (ITR) und der RICH Detektoren des LHCb Experiments.

Abstract

Within this doctoral thesis parts of the radiation hard readout chip *Beetle* have been developed and characterised, before and after irradiation. The design work included the analogue memory with the corresponding readout amplifier as well as components of the digital control circuitry. An interface compatible with the I^2C-standard and the control logic for event readout have been implemented. A scheme has been developed which ensures the robustness of the *Beetle* chip against Single-Event Upset (SEU). This includes the consistent use of triple-redundant memory devices together with a self-triggered correction in parts of the circuit.
The *Beetle* ASIC is a 128 channel pipelined readout chip for silicon strip detectors. The front-end consists of a charge-sensitive preamplifier and a CR-RC pulse shaper. It features an equivalent noise charge of $\mathrm{ENC} = 497\,\mathrm{e}^- + 48.3\,\mathrm{e}^-/\mathrm{pF}\cdot\mathrm{C}_{in}$. The analogue memory is a switched capacitor array, which provides a latency of max. $4\,\mu$s. The 128 channels are transmitted off chip in 900 ns via a current driver. Beside the pipelined readout path, the *Beetle* provides a fast discrimination of the front-end pulse. A total ionising dose irradiation of *Beetle1.1* up to 45 Mrad showed no functional failure and only slight degradation in the analogue performance. Chip version 1.2 fulfils the requirements of the vertex detector (VELO), the inner tracker (ITR) and the RICH detectors of the LHCb experiment.

Contents

1 $\mathcal{CP}$ Violation **1**

2 The LHCb Experiment **7**
2.1 Physics Perspective . . . 7
2.2 The LHCb Detector . . . 8
2.3 Radiation Levels at LHCb . . . 17
2.4 The Trigger and Readout System of LHCb . . . 18

3 Radiation Hard VLSI Electronics **21**
3.1 Radiation Damage in Microelectronic Devices . . . 21
3.1.1 Technology Scaling . . . 22
3.1.2 Cumulative Effects in MOS Transistors . . . 23
3.1.3 Cumulative Effects in Bipolar Transistors . . . 30
3.1.4 Single Event Effects . . . 33
3.2 Radiation Hard VLSI Circuit Design . . . 38
3.2.1 Choice of Process Technology . . . 38
3.2.2 Layout Techniques . . . 39
3.2.3 Analogue Circuit Design . . . 41
3.2.4 Redundancy . . . 42
3.2.5 Error Detection and Correction Codes . . . 42

4 The Beetle Readout Chip **47**
4.1 Silicon Strip Detectors and their Readout . . . 47
4.2 Requirements on a Silicon Microstrip Readout Chip for LHCb . . . 57
4.3 Beetle Chip Architecture . . . 60
4.4 Components . . . 64
4.4.1 Front-end . . . 64
4.4.2 Comparator . . . 68
4.4.3 Pipeline and Pipeline Readout Amplifier . . . 70
4.4.4 Multiplexer . . . 75
4.4.5 Output Buffer . . . 76
4.4.6 Bias Generators . . . 77
4.4.7 Control Logic . . . 80
4.5 The Beetle Chip Family . . . 88
4.6 Single Event Upset Robustness . . . 98

5 Chip Characterisation **103**
5.1 Pre-irradiation Performance . . . 103
5.1.1 Pulse shaping . . . 104
5.1.2 Maximum Input Charge Rate . . . 105
5.1.3 Noise . . . 106
5.1.4 Pipeline Homogeneity . . . 109
5.1.5 Random Trigger Test . . . 110
5.2 Irradiation Results . . . 111
5.2.1 Total Ionising Dose Irradiation Test . . . 111
5.2.2 Single Event Upset Irradiation Test . . . 115

6 Summary **119**

A The Beetle Reference Manual v1.1 **121**

B The Beetle Reference Manual v1.2 **143**

Bibliography **171**

List of Figures

1.1 Box diagrams for the K^0 and B^0-system . . . 3
1.2 Tree and penguin diagram for the "golden decay" . . . 3
1.3 Two unitarity triangles in the Wolfenstein's parametrisation . . . 6

2.1 Layout of the LHCb spectrometer . . . 9
2.2 Angular correlations of $b\overline{b}$-pairs in proton-proton collisions at the LHC . . . 10
2.3 Arrangement of the VELO sensors along the beam axis . . . 11
2.4 Layout of the VELO Roman pot configuration . . . 12
2.5 Detailed view of the secondary vacuum container . . . 13
2.6 Schematic drawing of one VELO module . . . 13
2.7 Schematic of the strip layout of the VELO R- and ϕ-sensors . . . 13
2.8 Photographs of a VELO hybrid assembled with *Beetle1.1* chips . . . 14
2.9 Layout of an Inner Tracker station . . . 15
2.10 Schematic layout of a 2-sensor silicon ladder . . . 16
2.11 Photography of an ITR hybrid assembled with *Beetle1.1* chips . . . 16
2.12 Mass spectrum of $B_d^0 \to \pi^+\pi^-$ and of $B_s^0 \to D_S^-K$ without and with RICH . . . 17
2.13 Layout of RICH1 (left) and RICH2 (right) . . . 18
2.14 Total hadron flux for VELO stations 7 and 25 . . . 19
2.15 Architecture of the LHCb trigger and DAQ system . . . 20

3.1 Energy band diagram of a Metal-Oxide-Semiconductor structure . . . 24
3.2 Hole trapping in the oxide of a MOS structure . . . 24
3.3 Model for hole trapping in SiO_2 with E' centre formation . . . 25
3.4 Schematic of possible hole transport mechanisms in SiO_2 . . . 25
3.5 Threshold voltage shift of an NMOS and PMOS transistor vs. accumulated dose 27
3.6 Variation of the subthreshold slope under irradiation . . . 27
3.7 Leakage currents in NMOS transistors . . . 27
3.8 Reduction of the mobility as a function of interface-trap density . . . 28
3.9 Energy dependence of non-ionising energy loss in silicon . . . 31
3.10 DC current gain of a *npn* and *pnp* transistor before and after irradiation . . . 32
3.11 Spectral noise density of an integrated preamplifier before and after irradiation 32
3.12 Relative degradation of the gain for various devices under irradiation . . . 32
3.13 Funnelling . . . 34
3.14 Response of a *pn*-junction to the penetration of an ionising particle . . . 34
3.15 Measured SEU cross-section of shift registers under heavy-ion irradiation . . . 35
3.16 Measured SEU cross section for various types of static flip-flops . . . 35
3.17 Hardening an SRAM cell by increasing the feedback resistance . . . 36

3.18 Formation of a parasitic thyristor structure in CMOS technologies 37
3.19 Shift of the flatband voltage V_{FB} per unit dose 38
3.20 Variation of the density of interface traps D_n per unit dose 38
3.21 Principle drawing of the geometry of a linear and an enclosed transistor 39
3.22 Layout principle of guard rings around MOS transistors 40
3.23 Biasing with forced currents 41
3.24 Inherent compensation of threshold voltage shifts in a current mirror 41
3.25 3-bit code representation in a cube 43
3.26 Block diagram of a possible control logic implementing the *Hamming* code . . . 46

4.1 Energy loss per path length as a function of kinetic energy 49
4.2 Experimental energy loss distributions 49
4.3 Partly and full depletion of a *pn*-junction 51
4.4 Cross section of an AC-coupled silicon strip detector 52
4.5 Signal acquisition with a charge sensitive amplifier (CSA) 54
4.6 Output pulses of shapers with multiple integration stages: $\tau_{int} = \text{const.}$ 56
4.7 Output pulses of shapers with multiple integration stages: $T_p = \text{const.}$ 56
4.8 Passive and and active implementation of the CR-RC shaper 57
4.9 Schematic block diagram of the *Beetle* chip 61
4.10 Readout paths of the *Beetle* chip 62
4.11 Layout of the *Beetle1.2* chip version and its corresponding floor plan 64
4.12 Schematic of the *Beetle* front-end formed by the preamplifier, shaper and buffer 65
4.13 Basic amplifier stages 66
4.14 Transient response of the front-end 67
4.15 Generic cascade of two amplifier stages 67
4.16 Schematic of the test pulse injection circuit 68
4.17 Schematic block diagram of the comparator 69
4.18 Schematic of a pipeline cell 70
4.19 Layout principle of the pipeline 71
4.20 C-V-characteristic of the NMOS capacitor used in the pipeline cells 72
4.21 Schematic of the pipeline readout amplifier 73
4.22 Timing sequence of the readout control signals 74
4.23 Schematic of the pipeamp's reset and multiplexer's track-and-hold switch . . . 74
4.24 Amplifier core of the pipeamp 74
4.25 Transient simulation output of the pipeamp 75
4.26 Schematic diagram of the multiplexer 76
4.27 Schematic of the fully differential current output driver 77
4.28 Regulated cascode current source 78
4.29 Principle schematic of the current digital-to-analogue converter 79
4.30 Schematic of the voltage digital-to-analogue converter 80
4.31 Hierarchy levels of the *Beetle* control logic 81
4.32 I^2C-transfer sequences for accessing the *Beetle* registers 83
4.33 State diagram of the finite state machine *Ctrl* of *Beetle*'s interface circuit . . . 84
4.34 State diagram of the Write- and Read-Decoder FSM of *Beetle*'s interface circuit 85
4.35 Configuration of a *Beetle* register 85
4.36 Principle of the derandomising trigger buffer 86
4.37 Correlation between the derandomising buffer's flag bits and the pipeline pointers 87

4.38 Transistor layout styles used in the various front-end implementations 91
4.39 Analogue output signal of a *Beetle1.0* chip 92
4.40 Simulation of the baseline variation in the *Beetle1.0* chip 92
4.41 Measured and simulated output response of the pipeamp on the *BeetlePA1.0* test chip 93
4.42 Analogue output signal of a *Beetle1.1* chip 94
4.43 Output signal of the binary pipelined readout path on *Beetle1.1* 94
4.44 Readout behaviour of *Beetle1.1* at nominal and low trigger rates 95
4.45 Readout timing scheme in *Beetle1.1* and *Beetle1.2* 96
4.46 Readout behaviour of *Beetle1.1* for two triggers 96
4.47 Analogue readout sequence of *Beetle1.2* 97
4.48 Readout behaviour of *Beetle1.2* for consecutive and non-consecutive triggers . . 97
4.49 Principle schematic of a triple redundant flip-flop 100
4.50 Principle schematic of a flip-flop featuring a self-triggered SEU correction . . . 100
4.51 Principle schematic of an integrated D-type flip-flop 101
4.52 Detailed schematic of the *TRFDFF* flip-flop 102
4.53 Simulation result of a self-triggered correction process 102

5.1 Schematic of the charge injection circuit on the *Beetle* test boards 104
5.2 Receiver circuits for analogue and binary *Beetle* output signals 104
5.3 Laboratory test setup 105
5.4 Front-end output signal of *Beetle1.1* obtained from a pulse shape scan 106
5.5 Front-end output signal of *Beetle1.2* 106
5.6 Transient response on a delta-shaped input signal 107
5.7 Equivalent noise charge of the *Beetle1.2* front-end 108
5.8 Surface plots of the pipeline pedestals of a *Beetle1.1* chip 109
5.9 Pedestal distributions of the complete capacitor array for 3 *Beetle1.1* chips . . . 109
5.10 Setup of the TID irradiation test performed with the *Beetle* chips 112
5.11 Pulse shape variation as a function of dose 112
5.12 Pulse shape parameters of *Beetle1.1* as a function of dose 113
5.13 Pulse shape parameters of front-end set 2c as a function of dose 114
5.14 Block schematic of the *BeetleSR1.0* test chip 115
5.15 Layout and floor plan of the *BeetleSR1.0* test chip 115
5.16 Energy loss and range of helium ions in silicon 118
5.17 Scheme of the SEU irradiation setup for *BeetleSR1.0* 118

A.1 Schematic block diagram of the *Beetle* readout chip 125
A.2 Example of a receiver circuit for the analogue output signals 126
A.3 Types of reset on *Beetle1.1* 127
A.4 Analogue readout mode 128
A.5 Binary readout mode 128
A.6 Readout mode for less demanding readout speed requirements 128
A.7 Readout timing scheme 129
A.8 Connection scheme of *Beetle* chips in a daisy chain 129
A.9 I^2C-bus write and read sequences for accessing registers on the *Beetle* 131
A.10 Bidirectional level shifter circuit 132
A.11 Bit assignment of the configuration registers *ROControl* and *CompControl* . . 132

A.12 Pad layout of *Beetle1.1* 134

B.1 Schematic block diagram of the *Beetle* readout chip 147
B.2 Example of a receiver circuit for the analogue and binary output signals 148
B.3 *Beetle1.2* readout modes 150
B.4 Readout timing schemes 151
B.5 I^2C-bus write and read sequences for accessing registers on the *Beetle* 154
B.6 Bidirectional level shifter circuit 155
B.7 Bit assignment of the configuration registers *ROControl* and *CompControl* . . 155
B.8 Pad layout of *Beetle1.2* 157

List of Tables

1.1 Quark masses and coupling strengths 5

2.1 Expected number of events after reconstruction 8
2.2 Precision on the angles of the unitarity triangle 8
2.3 Detector technologies employed in the LHCb experiment 10
2.4 Calculated radiation levels in the LHCb cavern 20

3.1 Constant-field scaling of various process parameters 22
3.2 Summary of radiation effects in CMOS devices 29
3.3 Categories of Single Event Effects 33
3.4 LET values for various ion types 36
3.5 Possible *Hamming* code syndromes 45

4.1 Charge transfer efficiency for different detector capacitances 55
4.2 Key parameters of the LHCb detectors to be read out by the *Beetle* chip 58
4.3 Basic specifications of the LHCb front-end electronics 59
4.4 Requirements on the *Beetle* readout chip 59
4.5 Comparison of the HELIX128 and *Beetle* readout chips 88
4.6 Members of the *Beetle* chip family 89
4.7 Overview of the essential design parameters of the various *Beetle* front-ends . . 90
4.8 Truth table of the triple redundant flip-flop 99

5.1 Key parameters of the *Beetle* readout chip 103
5.2 Front-end pulse shape parameters 104
5.3 Measured pulse shape parameters of *Beetle1.2* 105
5.4 Equivalent noise charge of front-end set 2c 108
5.5 TID irradiation steps for the various *Beetle* chips 111

A.1 DC characteristics of *Beetle1.1* 126
A.2 Mapping of analogue input channels to comparator output channels on *Beetle1.1* 130
A.3 Bias and configuration registers of *Beetle1.1* 133

B.1 DC characteristics of *Beetle1.2* 148
B.2 Header bits in *Beetle1.2*'s data burst 149
B.3 Mapping of analogue input channels to comparator output channels on *Beetle1.2* 152
B.4 Channel sequence for write and read access to the shift registers 154
B.5 Bias and configuration registers of *Beetle1.2* 156

Introduction

The matter asymmetry in our universe, i.e. the dominance of matter over antimatter, requires three ingredients (after *Sakharov* [Sak67]):

- the violation of baryon-number conservation, which means the decay of the proton,
- the violation of $\mathcal{CP}$-symmetry,
- a thermal non-equilibrium at the electro-weak phase transition ($\approx 10^{-5}$ s after the big bang).

To illustrate these requirements, consider the proton-decay reactions [Sch02]

$$H: \quad e^- p \longrightarrow e^- e^+ \pi^0 \longrightarrow 4\gamma, \tag{1}$$
$$\bar{H}: \quad e^+ \bar{p} \longrightarrow e^+ e^- \pi^0 \longrightarrow 4\gamma. \tag{2}$$

The final states are $\mathcal{CP}$-eigenstates. $\mathcal{CP}$-violation allows different decay rates $\Gamma(H) < \Gamma(\bar{H})$ resulting in a surplus of matter. In a thermal equilibrium, $4\gamma \longrightarrow \bar{H}$ would annihilate the leftover matter H, whereas a thermal non-equilibrium would red-shift the γ-energies below the creation threshold. The search for antimatter-dominated regions in the universe, e.g. the search for primordial anti-Helium with the AMS-Experiment [AMS], showed no antimatter so far.

The violation of $\mathcal{CP}$-symmetry is a key mechanism. It has first been shown in 1964 in the system of neutral K-mesons [Chr64] and in 2000 in the B-meson system [Bab00, Bel00]. LHCb is a precision measurement experiment for $\mathcal{CP}$-violation and rare decays in the B-system at the future LHC collider. B-mesons will be created in pp collisions at $\sqrt{s}$ =14 TeV with a large production cross section of 500 μb and detected with a single-arm spectrometer.

Typical of all LHC experiments is the detector operation in a very hostile radiation environment which puts additional demands on the detectors and the corresponding readout electronics concerning radiation hardness. Especially the innermost detector components, which are close to the beam pipe are subject to high particle fluxes. Special design considerations have to be taken, in order to ensure the proper operation of the devices for several years.

A readout chip for the silicon strip detectors (vertex detector and inner tracker) and the RICH detectors of LHCb has been developed in the ASIC-laboratory in Heidelberg in cooperation with NIKHEF Amsterdam and the University of Oxford. This work describes the development and characterisation of the first three iterations of this radiation hard readout chip, named *Beetle.*

An introduction to $\mathcal{CP}$-violation is given in chapter 1, followed by an overview description of the experimental apparatus of the LHCb experiment in chapter 2. The basic processes in

microelectronic devices induced by radiation will be discussed in chapter 3 including the consequences on circuit performance. Chapter 4 will detail the architecture of the *Beetle* readout chip on a circuit schematic level together with an overview of the various chip versions and their basic characteristics. The measurement results for the chip version 1.1 before and after irradiation will be presented in chapter 5.

Chapter 1

$\mathcal{CP}$ Violation

Introduction

Symmetries play an important role in physics. They are directly linked to conservation laws which is expressed in *Noether's theorem* [Noe18]. For example, the invariance of physics laws under a transformation in time is equivalent to the conservation of energy, the invariance under global gauge transformations involves the conservation of electric charge. Symmetries can be distinguished in *discrete* and *continuous* symmetries according to the eigenvalue spectrum of the corresponding transformation operator. Examples for continuous symmetries are the invariance under space translation, resulting in momentum conservation or the invariance under rotation which is equivalent to the conservation of angular momentum. Three fundamental discrete symmetries exist:

- parity transformation $\mathcal{P}$, which is the space reflection at the coordinate origin ($\vec{r} \rightarrow -\vec{r}$),
- charge conjugation $\mathcal{C}$, which exchanges a particle by it's antiparticle ($p \rightarrow \bar{p}$) and
- time-inversion $\mathcal{T}$, which inverts the direction of time ($t \rightarrow -t$).

$\mathcal{P}$ [Wu57], $\mathcal{C}$ and $\mathcal{T}$ [Ang98] are each violated separately. The weak interaction couples only to left-handed fermions and right-handed anti-fermions (V − A-theory). One says, that parity is *maximally* violated. As a direct consequence charge conjugation is no valid symmetry under weak interactions. $\mathcal{C}$ would transfer a left-handed fermion (f_L) to a left-handed anti-fermion ($\bar{f}_L$).

The combined transformation $\mathcal{CP}$ was believed to be a valid symmetry ($f_L \xrightarrow{\mathcal{CP}} \bar{f}_R$), until Christenson et al. [Chr64] observed the violation of $\mathcal{CP}$ in the K^0-system. In contrast to $\mathcal{P}$ which is maximally violated, $\mathcal{CP}$-violation is a tiny effect.

General principles of relativistic field theory require the invariance under the combined transformation $\mathcal{CPT}$ ($\mathcal{CPT}$*-theorem* [Lüd57, Pau55]). If $\mathcal{CPT}$ is conserved, particles and antiparticles have the same masses, the same absolute value of charge and the same magnetic moment. Tests of $\mathcal{CPT}$ compare e.g. the mass difference of K^0 and $\bar{K^0}$. It is at the time [PDG00]

$$\frac{|m_{K^0} - m_{\bar{K^0}}|}{\langle m_{K^0} \rangle} \leq 10^{-18}. \tag{1.1}$$

Provided, that $\mathcal{CPT}$ invariance is valid, $\mathcal{CP}$-violation and $\mathcal{T}$-violation are equivalent.

$\mathcal{CP}$-violation can occur via the mixing of $\mathcal{CP}$ eigenstates, called *indirect* $\mathcal{CP}$-violation, represented in the K^0-system by the complex parameter ϵ as well as in the decay process called *direct* $\mathcal{CP}$-violation, represented in the K^0-system by the parameter ϵ'. A third kind of $\mathcal{CP}$-violation is due to the interference of mixing and decay.

Neutral Kaon System

K-mesons are created in the strong interaction, e.g. $\pi^- p \rightarrow K^0\Lambda$, but decay in a weak process ($K^0 \rightarrow \pi^+\pi^-, \pi^0\pi^0$) by the exchange of W-bosons. The K-meson can make a transition to it's own antiparticle via a second order weak process ($K \rightleftharpoons \bar{K}$). Fig. 1.1 (a) depicts the corresponding Feynman graphs of lowest order, the so-called box-diagrams. As a consequence, the eigenstates of the strong interaction $|K^0\rangle$ and $|\bar{K}^0\rangle$ mix and the mass-eigenstates, i.e. the real particles are linear combinations of them. Since $\mathcal{CP}|K^0\rangle = -|\bar{K}^0\rangle$ and $\mathcal{CP}|\bar{K}^0\rangle = -|K^0\rangle$, the eigenstates of the strong interaction are no $\mathcal{CP}$-eigenstates. As can be easily verified, $|K_1\rangle = 1/\sqrt{2}(|K^0\rangle - |\bar{K}^0\rangle)$ and $|K_2\rangle = 1/\sqrt{2}(|K^0\rangle + |\bar{K}^0\rangle)$ are $\mathcal{CP}$-eigenstates to the eigenvalues $+1$ and -1 resp. Two different K-mesons are observed with strongly differing life times. The $|K_S\rangle$ (S: *short*) meson has a life time of 0.89×10^{-10} s, the $|K_L\rangle$ (L: *long*) of 5.17×10^{-8} s [PDG00]. The dominating hadronic decay mode of $|K_S\rangle$ is into 2 pions, of $|K_L\rangle$ into 3 pions. A 2 pion system is a $\mathcal{CP}$-eigenstate to the eigenvalue $+1$, a 3 pion system to -1. The conservation of $\mathcal{CP}$-symmetry means, that $|K_1\rangle$ only decays into 2 pions and $|K_2\rangle$ only into 3. Christenson, Cronin and Fitch investigated the decay of the long-lived Kaon $|K_L\rangle$ [Chr64]. They found, that $|K_L\rangle$ decays predominantly into 3 pions, but also with a small fraction into 2 pions (they found about 50 decays). This means, that $|K_L\rangle$ is not a $\mathcal{CP}$-eigenstate and is unequal to $|K_2\rangle$. The experimental observation can be explained by a mixing of $|K_1\rangle$ and $|K_2\rangle$ to $|K_L\rangle$ and is called *indirect* $\mathcal{CP}$-violation.

$$|K_L\rangle = \frac{1}{\sqrt{1+|\epsilon|^2}}(|K_2\rangle + \epsilon|K_1\rangle) \tag{1.2}$$

with
$|\epsilon| = 2.3 \times 10^{-3}$.

In the same way, $|K_S\rangle$ is a mixture: $|K_S\rangle = 1/(\sqrt{1+|\epsilon|^2})(|K_1\rangle + \epsilon|K_2\rangle)$.

Looking at the semi-leptonic decay modes of the $|K_L\rangle \longrightarrow \pi^+e^-\bar{\nu}_e, \pi^-e^+\nu_e$, one finds, that the $|K_L\rangle$ decays more often (by the fraction 3.3×10^{-3}) into a positron than into an electron. Since $\mathcal{CP}$ transforms $\pi^+e^-\bar{\nu}_e$ into $\pi^-e^+\nu_e$, this is a violation of $\mathcal{CP}$-symmetry. Classical electrodynamics is invariant under the change of sign of all electrical charges. Note, that the semi-leptonic decay of the $|K_L\rangle$ makes an absolute difference between matter and antimatter and it enables an unambiguous and convention-free definition of positive charge [Gri96]: *It is the charge, which is carried by the lepton being created preferentially in the decay of the long-lived neutral kaon.*

The amplitude of $\mathcal{CP}$-violation in the decay (direct $\mathcal{CP}$-violation) is denoted ϵ'. Two experiments, *NA48* at CERN and *kTeV* at Fermilab, have investigated direct $\mathcal{CP}$-violation in the K^0-system by measuring K^0_S and K^0_L-decays into two pions. The final result of NA48 is [Bat02]

$$\Re(\frac{\epsilon'}{\epsilon}) = (14.7 \pm 2.2) \times 10^{-4}. \tag{1.3}$$

This shows, that ϵ' is significantly $\neq 0$ and $\mathcal{CP}$-violation is part of the weak interaction.

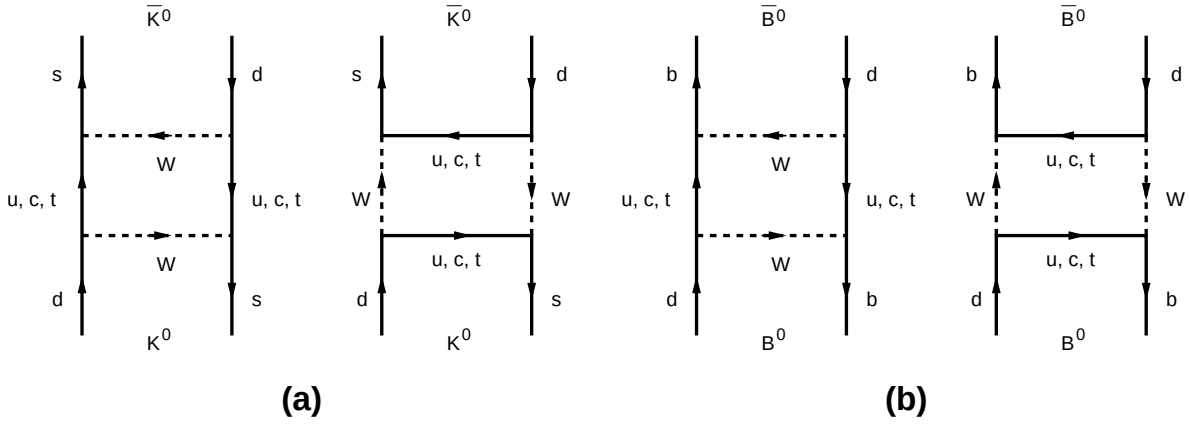


Figure 1.1: Box diagrams for the K^0 (a) and B^0-system (b).

Neutral B-meson System

Measurements of $\mathcal{CP}$-violation in the B-meson system compare the decay modes of a particle X and it's antiparticle $\bar{X}$ into the same $\mathcal{CP}$-eigenstate ϕ_{CP}. Different decay rates of particle and antiparticle violate $\mathcal{CP}$-symmetry. The physical observable is the "$\mathcal{CP}$-asymmetry"

$$A_{CP} = \frac{\Gamma(X \to \phi_{CP}) - \Gamma(\bar{X} \to \phi_{CP})}{\Gamma(X \to \phi_{CP}) + \Gamma(\bar{X} \to \phi_{CP})}. \tag{1.4}$$

The box-diagrams for B-mixing are depicted in fig. 1.1 (b). In the B-meson system, $\mathcal{CP}$-violation can be investigated in a multitude of decay channels (cf. section 2.1). The decay into the final state $\phi_{CP} = J/\Psi K_S$ is called "golden decay". In many channels, strong and electromagnetic corrections ("penguin diagrams") contribute to the weak decay amplitude. For the channel $B/\bar{B} \to J/\Psi K_S$ the penguin contributions do not destroy the $\mathcal{CP}$ phase to be measured. Fig. 1.2 shows the Feynman graphs of lowest order for the "golden decay" of the B-meson.

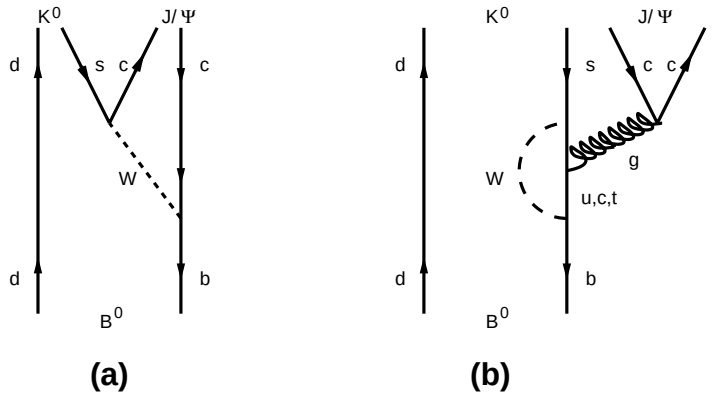


Figure 1.2: Tree (a) and penguin diagram (b) for the "golden decay".

The experimental signature of the "golden decay" is

$$B \rightleftharpoons \bar{B} \rightarrow J/\Psi K_S \rightarrow l^+ l^- \pi^+ \pi^- . \tag{1.5}$$

The lepton and pion final states are reconstructed, while the flavour of the B-meson is determined by *tagging*. This method uses the empirical rule $\Delta S = \Delta Q_l$ (the change in strangeness S is equal to the change in electric charge of the leptons Q_l) to identify the B-meson flavour from the electric charge of the decay lepton of the second B-meson.

Standard Model Description

The charged currents (W^+, W^-) do not couple to the neutral current (g, γ, Z) or flavour eigenstates

$$\begin{pmatrix} u \\ d \end{pmatrix}, \begin{pmatrix} c \\ s \end{pmatrix}, \begin{pmatrix} t \\ b \end{pmatrix} \tag{1.6}$$

but to the charged current eigenstates

$$\begin{pmatrix} u \\ d' \end{pmatrix}, \begin{pmatrix} c \\ s' \end{pmatrix}, \begin{pmatrix} t \\ b' \end{pmatrix}. \tag{1.7}$$

The negatively charged states are a linear combination of the flavour eigenstates which is described by the Cabibbo-Kobayashi-Maskawa (CKM) matrix [Kob73].

$$\begin{pmatrix} d' \\ s' \\ b' \end{pmatrix} = \begin{pmatrix} V_{ud} & V_{us} & V_{ub} \\ V_{cd} & V_{cs} & V_{cb} \\ V_{td} & V_{ts} & V_{tb} \end{pmatrix} \begin{pmatrix} d \\ s \\ b \end{pmatrix} \equiv \mathbf{V_{CKM}} \begin{pmatrix} d \\ s \\ b \end{pmatrix} \tag{1.8}$$

It is a complex 3×3 matrix, which has in principle 18 independent parameters. General principles require the unitarity of the matrix which reduces the number of parameters to 9. Additional 5 out of the 9 can be transformed into phases in the quark wave functions. This results in 4 independent parameters. In an n dimensional space a rotation can be expressed by $\frac{1}{2}n(n-1)$ Euler-type angles. Hence, the 4 parameters of the CKM-matrix are 3 real angles and 1 complex phase. This complex phase is the source of $\mathcal{CP}$-violation in the Standard Model. A real mixing matrix is not able to explain $\mathcal{CP}$-violation. This is also the reason, why $\mathcal{CP}$-violation requires 3 quark generations. For only 2 generations the mixing is described by 1 real parameter (the Cabibbo-angle)[1].

A widely used approximation of the CKM-matrix is a parametrisation after Wolfenstein [Wol83] in terms of the sine of the Cabibbo-angle $\lambda = \sin \vartheta_C$. It nicely shows the hierarchy of the quark transitions.

[1] Kobayashi and Maskawa published their model [Kob73] at a time where only three quarks were known.

$$\mathbf{V_{CKM}} = \begin{pmatrix} 1-\frac{1}{2}\lambda^2 & \lambda & \lambda^3 A(\rho - i\eta) \\ -\lambda & 1-\frac{1}{2}\lambda^2 & \lambda^2 A \\ \lambda^3 A(1-\rho-i\eta) & -\lambda^2 A & 1 \end{pmatrix} + \mathcal{O}(\lambda^4) \sim \begin{pmatrix} 1 & \lambda & \lambda^3 \\ \lambda & 1 & \lambda^2 \\ \lambda^3 & \lambda^2 & 1 \end{pmatrix} \quad (1.9)$$

with
$\lambda = \sin\vartheta_C \approx 0.22$ (ϑ_C: Cabibbo-angle)
η, ρ, A (real) parametrisation parameters

The unitarity condition $VV^\dagger = 1$ results in 6 equations of the type $A + B + C = 0$ which can be visualised as triangles in the complex (η, ρ) plane. $\mathcal{CP}$-violation is proportional to the area of these triangles which is $\mathcal{O}(\lambda^6)$. Hence, $\mathcal{CP}$-violation is of the order 10^{-4}. Only in 2 of the 6 triangles all three sides are of comparable magnitude $\mathcal{O}(\lambda^3)$, while in the remaining triangles, one side is suppressed with respect to the others by $\mathcal{O}(\lambda^2)$ or $\mathcal{O}(\lambda^4)$. The two orthogonality relations resulting in "non-squashed" triangles are:

$$V_{ud}V_{ub}^* + V_{cd}V_{cb}^* + V_{td}V_{tb}^* = 0 \quad \text{(1st and 3rd column)} \quad (1.10)$$
$$V_{tb}V_{ub}^* + V_{ts}V_{us}^* + V_{td}V_{ud}^* = 0 \quad \text{(3rd and 1st row)} \quad (1.11)$$

Dividing eq. 1.10 by $V_{cd}V_{cb}^*$ puts one side of the triangle on the real axis of the (η, ρ) plane. Fig. 1.3 depicts the two triangles corresponding to the relations 1.10 and 1.11. $\eta \neq 0$ means a non-zero area of the triangle and therefore violation of $\mathcal{CP}$ in the Standard Model. The angles of the triangle are correlated to the transition amplitudes by

$$\alpha \equiv \arg\left(\frac{V_{td}V_{tb}^*}{V_{ud}V_{ub}^*}\right), \ \beta \equiv \arg\left(\frac{V_{cd}V_{cb}^*}{V_{td}V_{tb}^*}\right), \ \gamma \equiv \arg\left(\frac{V_{ud}V_{ub}^*}{V_{cd}V_{cb}^*}\right). \quad (1.12)$$

The $\mathcal{CP}$-asymmetry for the "golden channel" $B/\bar{B} \to J/\Psi K_S$ is directly linked to the angle β of the unitarity triangle.

$$A_{CP} = \frac{\Gamma(B \to J/\Psi K_S) - \Gamma(\bar{B} \to J/\Psi K_S)}{\Gamma(B \to J/\Psi K_S) + \Gamma(\bar{B} \to J/\Psi K_S} = \sin(2\beta)\sin(\Delta M t) \quad (1.13)$$

with
ΔM: mixing parameter describing the oscillation frequency of $B/\bar{B}$.

The amplitudes of the box diagrams (fig. 1.1) contributing to K- and B-mixing are proportional to the product of the quark masses and the corresponding CKM-matrix elements. For K-mixing this is $m_q V_{qd} V_{qs}^*$, for B-mixing $m_q V_{qd} V_{qb}^*$ (with $q = u, c, t$). As table 1.1 clarifies, K-mixing is dominated by the c-quark, while in B-mixing mainly the t-quark contributes.

q	m_q/GeV	$V_{qd}V_{qs}^*$	$V_{qd}V_{qb}^*$
u	0.01	λ	λ^3
c	1.5	λ	λ^3
t	175	λ^5	λ^3

Table 1.1: Quark masses and coupling strengths.

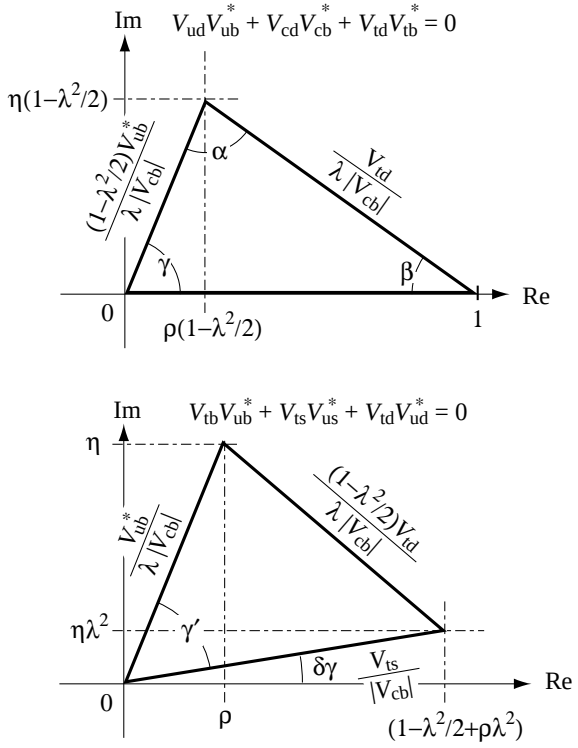


Figure 1.3: The two "non-squashed" unitarity triangles in the Wolfenstein's parametrisation with an approximation valid up to $\mathcal{O}(\lambda^5)$ [LHC98]. The upper triangle corresponds to eq. 1.10, the lower one to eq. 1.11.

Status of Measurements

The latest results (summer 2002) for $\sin(2\beta)$ are presented by the *BaBar* [Bab02] and *Belle* [Bel02] experiments, which operate at asymmetric-energy e^+e^--colliders at the Υ(4S) resonance ($\sqrt{s}$ =10.5 GeV).

$$\begin{array}{ll} \text{Belle:} & \sin(2\beta) = 0.719 \pm 0.074(\text{stat}) \pm 0.035(\text{syst}) \\ \text{BaBar:} & \sin(2\beta) = 0.741 \pm 0.067(\text{stat}) \pm 0.034(\text{syst}) \end{array} \tag{1.14}$$

The measurements are obtained from 88×10^6 produced $B\bar{B}$ pairs in case of BaBar and 85×10^6 in case of Belle and show a good accordance. In consideration of earlier results from OPAL (CERN), ALEPH (CERN) and CDF (Fermilab) the world average is

$$\sin(2\beta) = 0.734 \pm 0.054. \tag{1.15}$$

These direct measurements fit well to indirect measurements out of the unitarity of the CKM-matrix, which predict $0.6 \leq \sin(2\beta) \leq 0.9$.

The future LHCb experiment will measure more than the "golden decay" and perform redundant measurements of *all* angles in the unitarity triangles. The high statistics will allow to investigate $\mathcal{CP}$-violating effects beyond the Standard Model.

Chapter 2

The LHCb Experiment

LHCb is a next-generation experiment to study B-physics in pp-collisions at LHC. It is a precision measurement experiment for $\mathcal{CP}$-violation and rare decays in the B-meson system, being able to perform redundant measurements of all angles in the unitarity triangle and to test the Standard Model of electroweak interaction with unpredecedented precision. This calls for a high statistics experiment capable of studying $\mathcal{CP}$-violation in both B^0 and B_s^0 systems. LHCb provides the following capabilities:

- trigger sensitivity to both leptonic and hadronic final states,
- particle identification for p, K, π, μ and e,
- precise reconstruction of primary and b-hadron vertices,
- tracking system with good momentum resolution.

This chapter will give an overview of the expected physics performance of LHCb, of the various detector components and the trigger and data acquisition system. The emphasis is on the components being readout by the *Beetle* chip.

2.1 Physics Perspective

The LHCb-experiment plans to operated at a pp centre-of-mass energy of 14 TeV and a bunch crossing frequency of 40 MHz with an average luminosity of $\mathcal{L} = 2 \times 10^{32}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. At this luminosity, single pp-interactions will dominate, which simplifies the physics analysis. The $b\overline{b}$-production cross section $\sigma_{b\overline{b}}$ is $\approx 500\,\mu$b, which is far larger than at any existing machines. For example, the production rate for b-quarks is three orders of magnitude smaller at the e^+e^- B-factories *BaBar* and *Belle*, which operate at the $\Upsilon(4\mathrm{S})$ resonance ($\sqrt{s}$ =10.5 GeV), and also the expected value for coming runs of the Tevatron at Fermilab is a factor 15 smaller. From the total inelastic cross section $\sigma_{tot} = 100$ mb the ratio of events with b quarks is 5×10^{-3}. Hence, at LHCb 100,000 B-mesons/s are produced at an interaction rate of 40 MHz. They are hidden in 200 times more non-B events. An overview of the expected event numbers for some relevant decay channels is given in table 2.1, the corresponding precision on the angles in the unitarity triangle is listed in table 2.2.

Decay Modes	Visible Br. fraction	Offline Reconstr.
$B^0_d \to \pi^+\pi^-$ + tag	0.7×10^{-5}	6.9 k
$B^0_d \to K^+\pi^-$	1.5×10^{-5}	33 k
$B^0_d \to \rho^+\pi^-$ + tag	1.8×10^{-5}	551
$B^0_d \to J/\psi K_S$ + tag	3.6×10^{-5}	56 k
$B^0_d \to \overline{D}^0 K^{*0}$	3.3×10^{-7}	337
$B^0_d \to K^{*0}\gamma$	3.2×10^{-5}	26 k
$B^0_s \to D^-_s\pi^+$ + tag	1.2×10^{-4}	35 k
$B^0_s \to D^-_s K^+$ + tag	8.1×10^{-6}	2.1 k
$B^0_s \to J/\psi\phi$ + tag	5.4×10^{-5}	44 k

Table 2.1: Expected number of events after reconstruction from one year (10^7 s) of data taking with an average luminosity of $2 \times 10^{32}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ [LHC98].

Parameter	Decay Mode	σ [1 year]	Exploited features of LHCb
$\beta+\gamma$	B^0_d and $\overline{B}^0_d \to \pi^+\pi^-$; no penguin	0.03	K/π separation
$(=\pi-\alpha)$	penguin/tree= 0.20 ± 0.02	0.03–0.16	K/π separation
β	B^0_d and $\overline{B}^0_d \to J/\psi K_S$	0.01	-
$\gamma - 2\delta\gamma$	B^0_s and $\overline{B}^0_s \to D^\pm_s K^\mp$	0.05–0.28	K/π separation and σ_t
γ	$B^0_d \to \overline{D}^0 K^{*0}, D^0 K^{*0}, D_1 K^{*0}$ and $\overline{B}^0_d \to \overline{D}^0 \overline{K}^{*0}, D^0 \overline{K}^{*0}, D_1 \overline{K}^{*0}$	0.07–0.31	K/π separation
$\delta\gamma$	B^0_s and $\overline{B}^0_s \to J/\psi\phi$	0.01	σ_t
x_s	B^0_s and $\overline{B}^0_s \to D^\pm_s\pi^\mp$	up to 90 (95% CL)	σ_t

Table 2.2: Precision on the angles of the unitarity triangle and related parameters expected from the LHCb experiment in one year of data taking [LHC98].

2.2 The LHCb Detector

"The perfect detector is the empty detector."
U. Straumann

The LHCb detector is a single-arm spectrometer with an angular coverage from approximately 10 mrad to 300 mrad in the bending and 250 mrad in the non-bending plane. Fig. 2.1 depicts the layout of the apparatus. The detector geometry is motivated by the kinematics of the $b\overline{b}$-production. At high energies the $b\overline{b}$-pairs are produced predominantly in a forward or backward cone with small angles to the incoming proton beam (fig. 2.2). The forward geometry has additional advantages [Nak02]: an open geometry allows easy installation and maintenance and the transverse momentum trigger (p_T trigger) is more efficient in the forward region than in the central region, since the momenta are mainly carried by longitudinal components. A good decay time resolution for reconstructed hadrons can be achieved, since b-hadrons in the forward region have higher momentum compared to the central region (for an average momentum of 80 GeV/c, the decay length is about 7 mm).

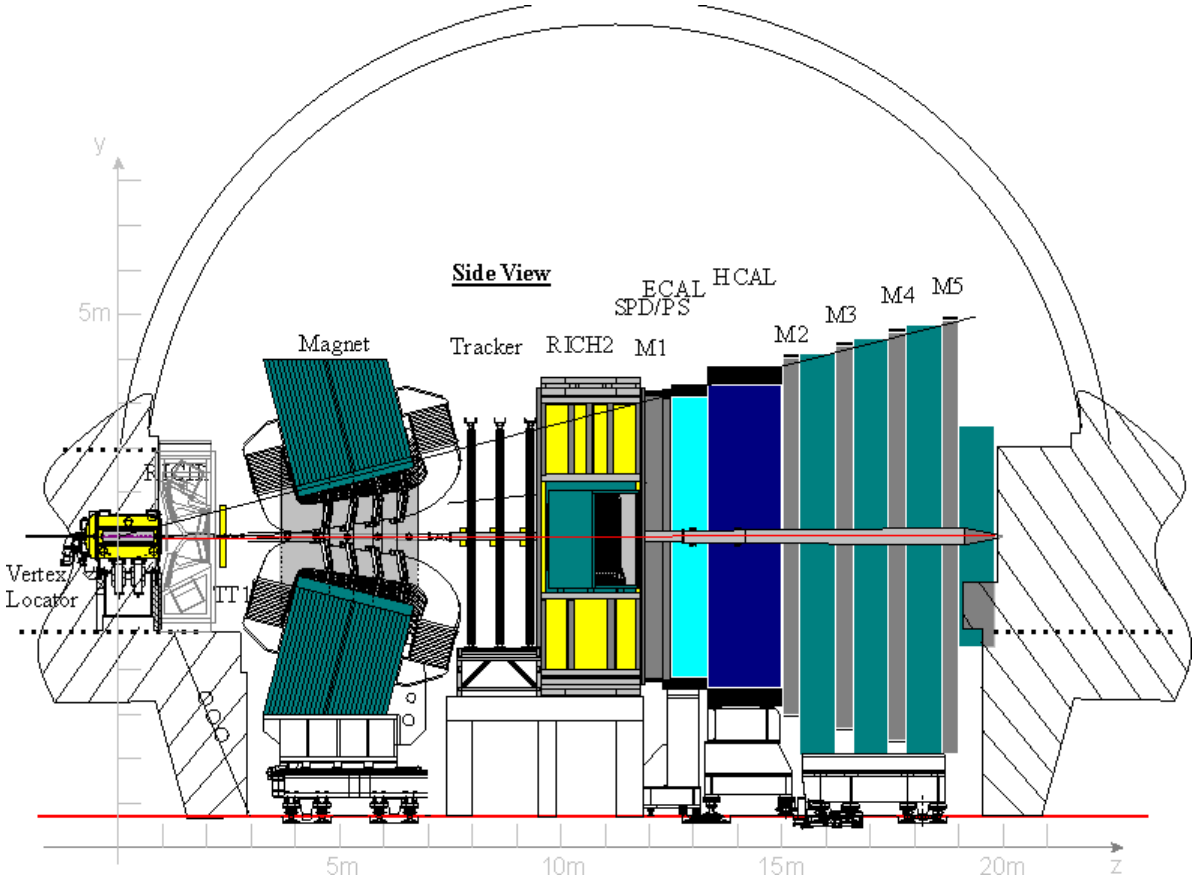


Figure 2.1: Layout of the LHCb spectrometer in the side view (cut in the non-bending plane), placed in the LHC Intersection-8 experimental area.

The spectrometer will be installed in the Intersection-8 experimental area at the future LHC collider. It has a length of 19.7 m and comprises a vertex detector system (VELO), including a pile-up veto counter (VETO), a tracking system (inner and outer tracker), aerogel and gas RICH[1] counters, an electromagnetic calorimeter (ECAL) with a preshower detector, a hadronic calorimeter (HCAL) and a muon detector. Table 2.3 lists all LHCb detector components with the chosen technology and the number of readout channels.

The design luminosity of LHCb is $\mathcal{L} = 2 \times 10^{32}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. Therefore, LHCb will be able to start it's full physics program from the beginning of LHC operation. Due to special beam optics the design value can be kept, even if LHC approaches the nominal luminosity of $10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$.

A warm dipole magnet provides a field integral of 4 Tm. The magnetic field is oriented vertically and has a maximum value of 1.1 T. The polarity of the magnetic field can be changed to control systematic errors in the $\mathcal{CP}$-violation measurements due to left-right asymmetries of the detector. The beam pipe in the region of the LHCb-experiment is subdivided into three sections. Around the interaction point a large vacuum tank with a length 1.7 m and a diameter

[1] Ring-Imaging Cherenkov
[2] Resistive Plate Chamber
[3] Multi Wire Proportional Chamber

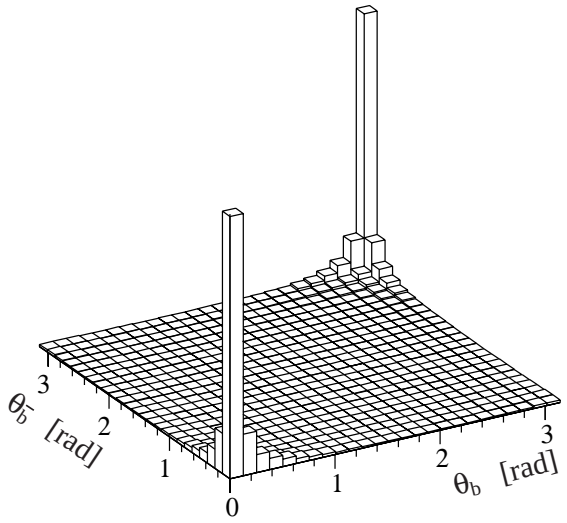


Figure 2.2: Angular correlations of $b\bar{b}$-pairs in proton-proton collisions at the LHC. Most of the heavy quark pairs are emitted in the same hemisphere with small angles (< 500 mrad) to the incoming proton beams (calculated by PYTHIA event generator) [LHC98].

component	technology	no. of channels
Vertex Detector	r-ϕ-silicon sensors	205,000
Inner Tracker	silicon-strip detectors	350,000
Outer Tracker	straw tubes	104,000
RICH1	Aerogel, C_4F_{10}	172,000
RICH2	CF_4	268,000
ECAL	lead/scint. "shashlik"	6,000
HCAL	iron/scint. tiles	1,500
Muon-system	RPC[2]and MWPC[3]	26,000

Table 2.3: Detector technologies employed in the LHCb experiment [Sch02].

of 1 m accommodates the vertex detector system. This part is followed by two conical sections, the first being 1.4 m long with a 25 mrad opening angle, the second one having a length of 16 m with a 10 mrad opening angle.

The detector design presented in the technical proposal [LHC98] and described here has been subject to intensive re-optimisation to reduce the material budget and therefore multiple-scattering. The main efforts are the change of the beam pipe material from aluminium to Al-Be alloy in order to reduce the radiation length and minimise the occupancies of the tracking and RICH detectors. The detector materials in the VELO, the tracking and the RICH systems are reduced to minimise multiple-scattering.

Vertex Detector System

The primary task of the vertex detector system is the reconstruction of the primary vertex, the reconstruction of tracks which do not originate from the primary vertex and the reconstruction of the secondary vertex, i.e. the decay vertex of the B-meson. The primary vertex resolution is 42 μm in the z-direction and 10 μm perpendicular to the beam. The decay length of the B-mesons can be determined, depending on the decay channel, with a precision between 220 μm and 375 μm [VEL01].

The vertex detector system consists in total of 27 stations of silicon microstrip sensors. 25 stations form the VErtex LOcator (VELO), 2 stations are positioned upstream and are dedicated to detect bunch crossings with more than one *pp*-interaction (pile-up veto counter: VETO). The stations are split in two halves covering 182° of azimuthal angle. They are slightly overlapping and placed perpendicular to the beam. The VELO part uses two different strip layouts, r- and ϕ-measuring sensors. The VETO counter uses only r-measuring sensors. Fig. 2.3 depicts the arrangement of the sensors along the beam axis.

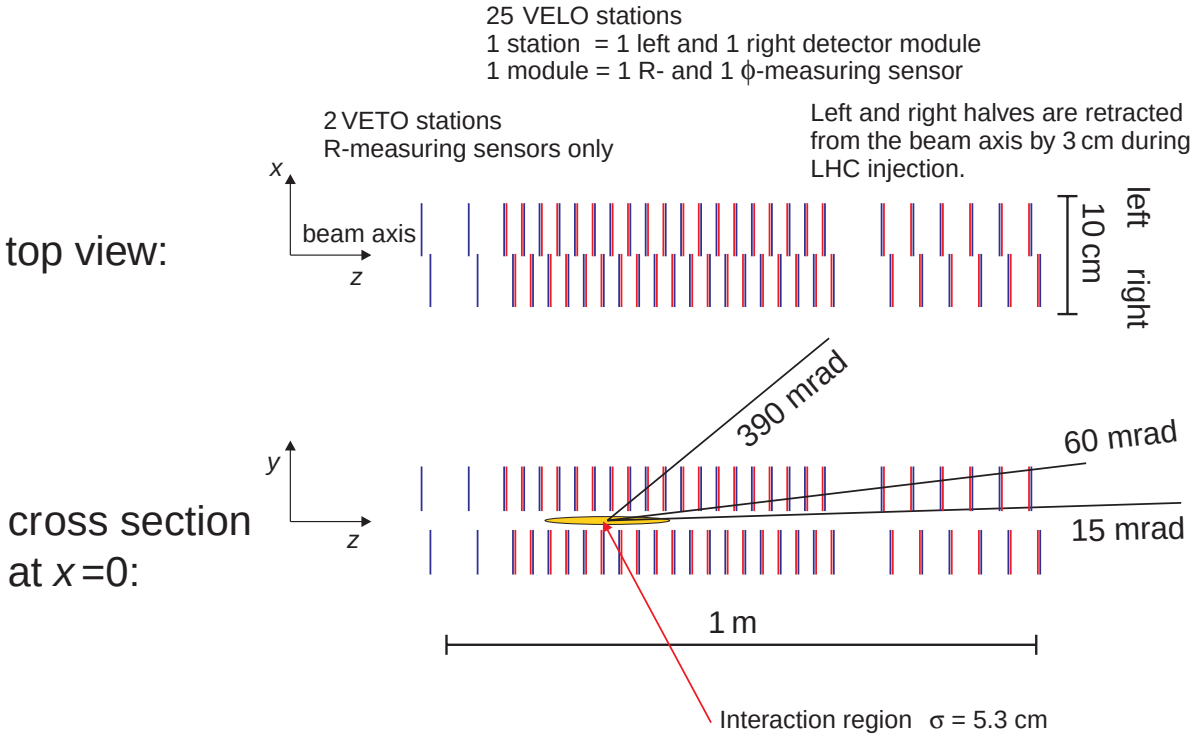


Figure 2.3: Arrangement of the VELO sensors along the beam axis [VEL01].

The detector modules are placed in *Roman pots* out of 250 μm thick aluminium foil acting as RF shield against the circulating proton bunches. The *Roman pots* themselves maintain a secondary vacuum to avoid the risk of explosion. The closest distance between a strip sensor and the beam is 8 mm, which is less than the aperture required by the LHC machine during injection. Hence, the detector modules are retractable by 3 cm. Fig. 2.4 shows the vertex detector tank with the retractable modules. Details of the *Roman pot* configuration in the vicinity of the beam pipe are shown in fig. 2.5. The corrugations close to the beam axis are needed to minimise the material seen by tracks before the first interaction in the silicon sensor. The corrugations at the side allow an overlap between left and right detector half.

Due to it's close distance to the interaction region, the VELO silicon sensors will be subject to a harsh radiation environment. At the innermost radius of 8 mm the particle flux is dominated be charged particles reaching levels of $10^{14} n_{eq}/cm^2$ per year (where n_{eq} is the damage equivalent of 1 MeV neutrons). The particle flux is strongly dependent on radius ($\propto r^{-\alpha}$, with $\alpha = 1.6 \ldots 2.1$), as depicted in fig. 2.14. These considerations have led to the choice of n-strip detectors on n-bulk material (n-on-n) with AC coupling to the electronics and polysilicon

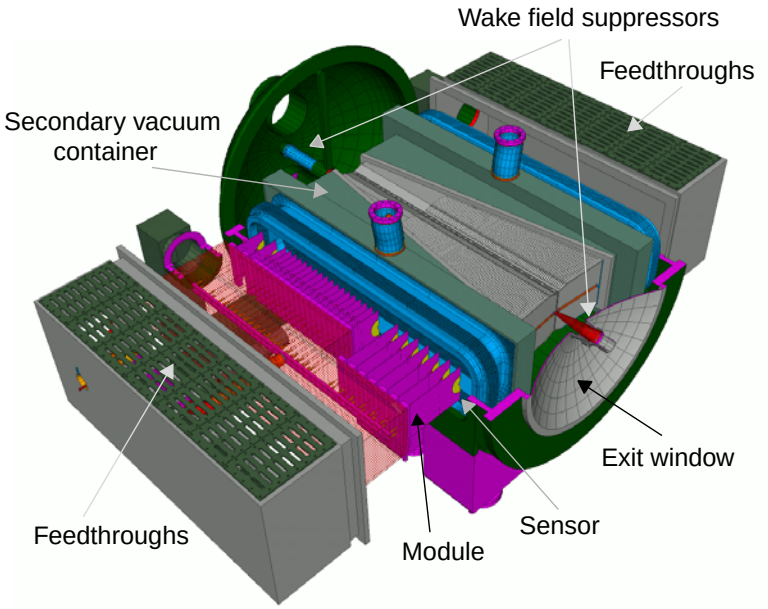


Figure 2.4: Layout of the VELO Roman pot configuration [VEL01]. One detector half is not installed to make the sensors visible.

biasing (cf. section 4.1). It is expected, that the silicon sensors have to be replaced every 3 years.

The strip layout with azimuthal (r-measuring) and radial (ϕ-measuring) strips has been chosen to optimise the speed of the pattern recognition in the L1 trigger. The length of the strips is varying to restrict the occupancy below 1% everywhere. The schematic of the two types of strip layouts is shown in fig. 2.7. Note, that for r-measuring sensors with azimuthal strips the strip length and therefore the capacitive input load of the front-end electronics is varying as a function of radius. Care should be taken, that groups of 128 strips connected to one readout chip have only slight variations in the strip length. Since the *Beetle*'s front-end bias parameters are common to all 128 input channels, this ensures to find a set of bias parameters which is suitable for all input channels. The number of strips per half-disc is 2,048. Hence, one silicon sensor is read out by 16 front-end chips. Fig. 2.6 shows a VELO module, consisting of a silicon sensor, the corresponding readout chips carried by a hybrid and the mechanical support structures. A photograph of a *Beetle*-hybrid carrying 16 *Beetle1.1* chips is depicted in fig. 2.8.

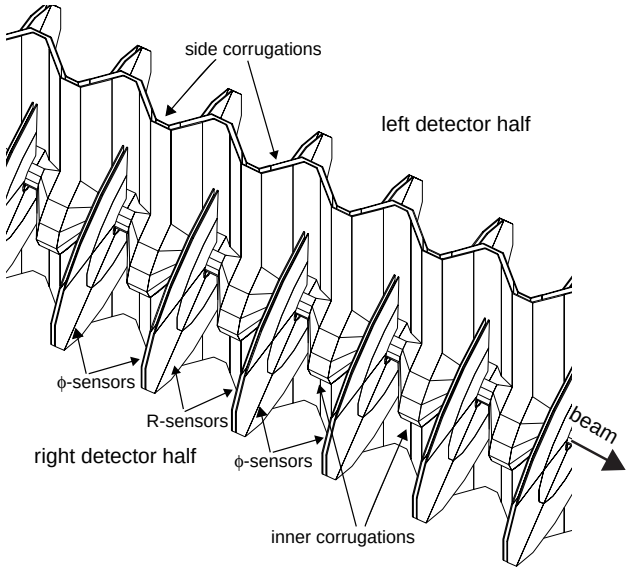


Figure 2.5: Detailed view of the secondary vacuum container [VEL01]. The corrugations close to the beam axis are needed to minimise the material seen by tracks before the first measurement point. The corrugations at the side allow an overlap between left and right detector half.

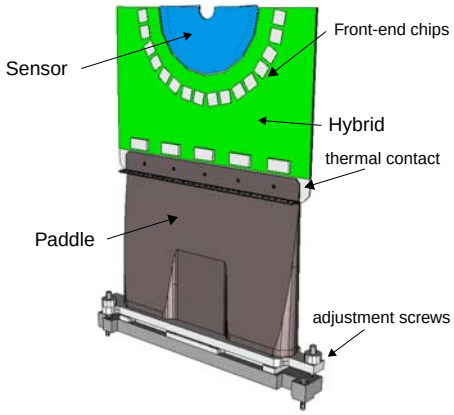


Figure 2.6: Schematic drawing of one VELO module, showing the silicon sensor and the hybrid with 16 readout chips [VEL01].

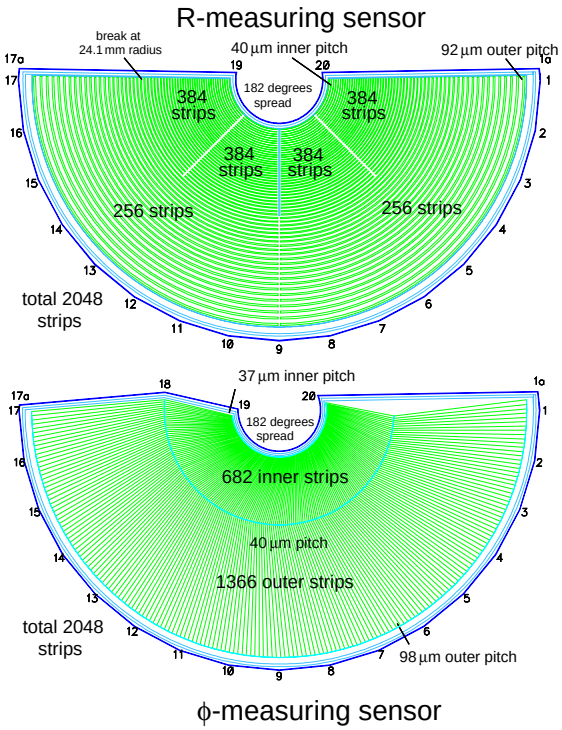


Figure 2.7: Schematic of the strip layout of the realistic R- and ϕ-sensors, not showing the routing lines [VEL01].

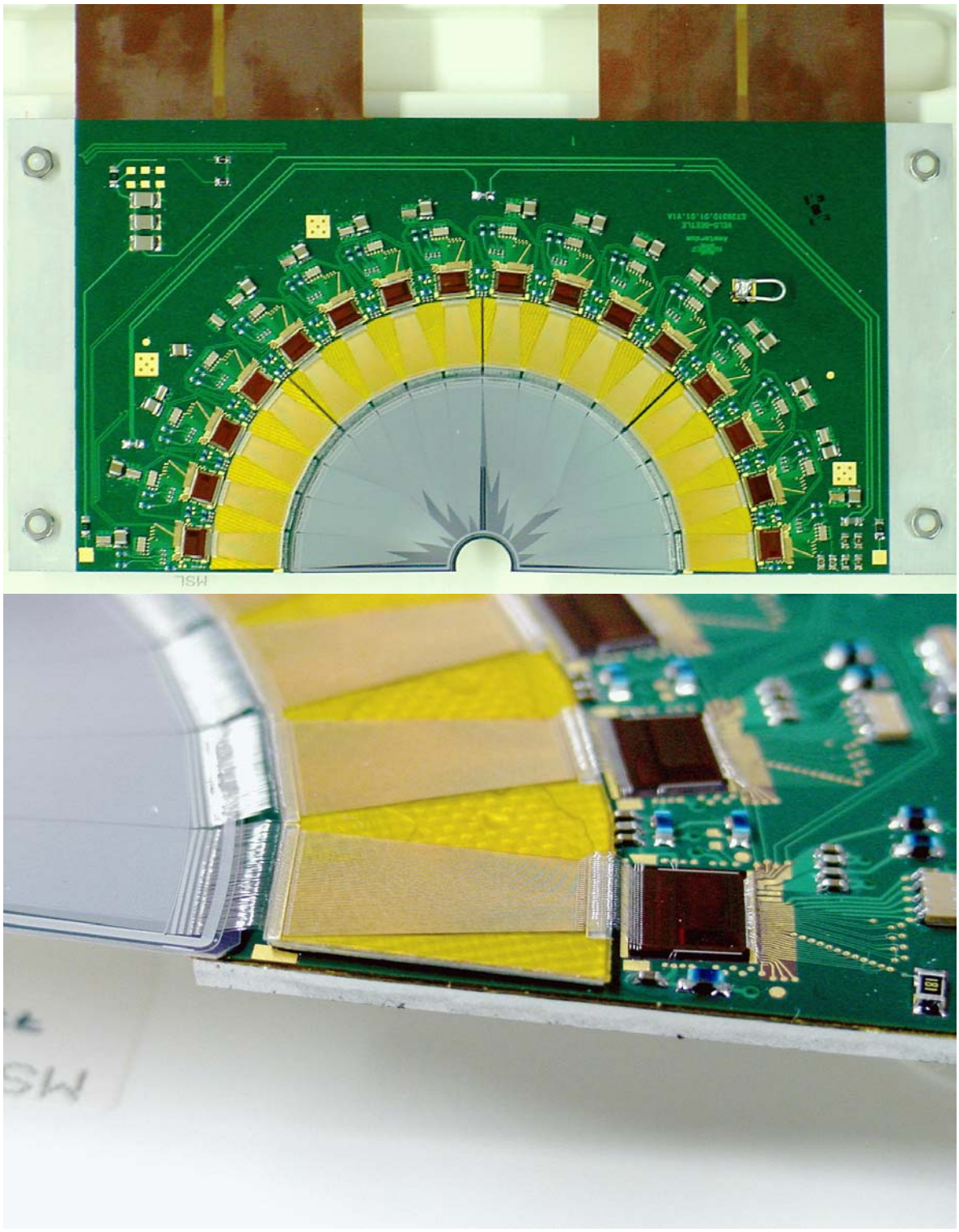


Figure 2.8: Photographs of a VELO hybrid assembled with *Beetle1.1* chips [NIK].

Inner Tracker

Efficient and precise reconstruction of charged particle tracks is a key requirement of the LHCb experiment, to achieve a high trigger and event reconstruction efficiency. For example [ITR02], in the decay channel $B_s^0 \to D_s^-(K^+K^-\pi^-)K^+$ 4 final state particles plus a tagging particle from the complementary B-meson have to be reconstructed with an efficiency of more than 90%. In addition, high momentum resolution is required, to precisely determine the invariant mass of the B-mesons. With a momentum resolution of $\delta p/p = 0.4\%$ an invariant mass resolution of $10\,\mathrm{MeV/c^2}$ can be achieved (in the channel $B_s^0 \to D_s^- K^+$).

The tracking system of LHCb is divided into two parts, to match the high track density close to the beam pipe. The boundary between inner and outer tracker was chosen such, that the occupancy of the outer tracker is limited to 15% [Nak02]. The Inner Tracker (ITR) is formed by the stations T1-T3 and is part of the Silicon Tracker which additionally includes station TT (cf. fig. 2.1). The ITR covers a cross-shaped region around the beam pipe (fig. 2.9). Silicon strip detectors with p-strips on an n-bulk are used. The total sensitive silicon area is $4.2\,m^2$ [ITR02]. Compared to the VELO, radiation damage is of far less importance, since the sensors are several cm away from the beam pipe. In order to minimise the number of readout channels, a large strip pitch of $\sim 200\,\mu m$ together with long readout strips of 22 cm has been chosen. A ladder is formed by two silicon sensors, which are read out by 3 *Beetle* chips (fig. 2.10). The chips are carried by a ceramic hybrid and attached to the silicon sensors via a pitch adapter.

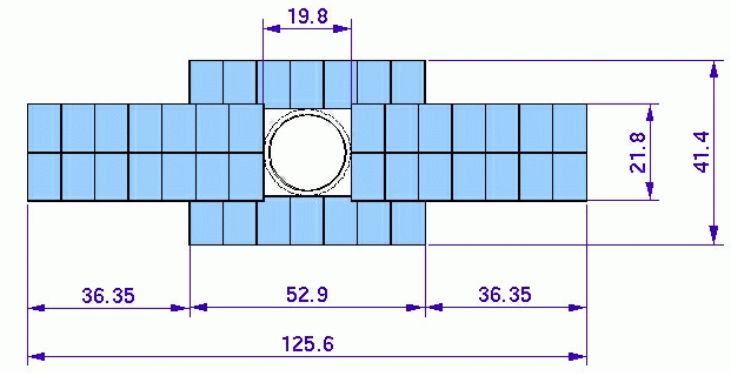


Figure 2.9: Layout of an Inner Tracker station. The dimensions are in cm [Ste02].

The length of the readout strips of 22 cm constitutes a high capacitive input load to the *Beetle*'s preamplifier. The total strip capacitance, i.e. the sum of strip-to-backplane and strip-to-strip capacitance, is $\sim 1.5\,\mathrm{pF/cm}$ [Leh02], which results in an input load of $\sim 33\,\mathrm{pF}$. Special emphasis has been placed on the *Beetle* front-end design, in order to cope with these high load capacitances.

Fig. 2.11 depicts a photography of the inner tracker hybrid used in the test beam in 2002. Three *Beetle1.1* chips read out the silicon sensor.

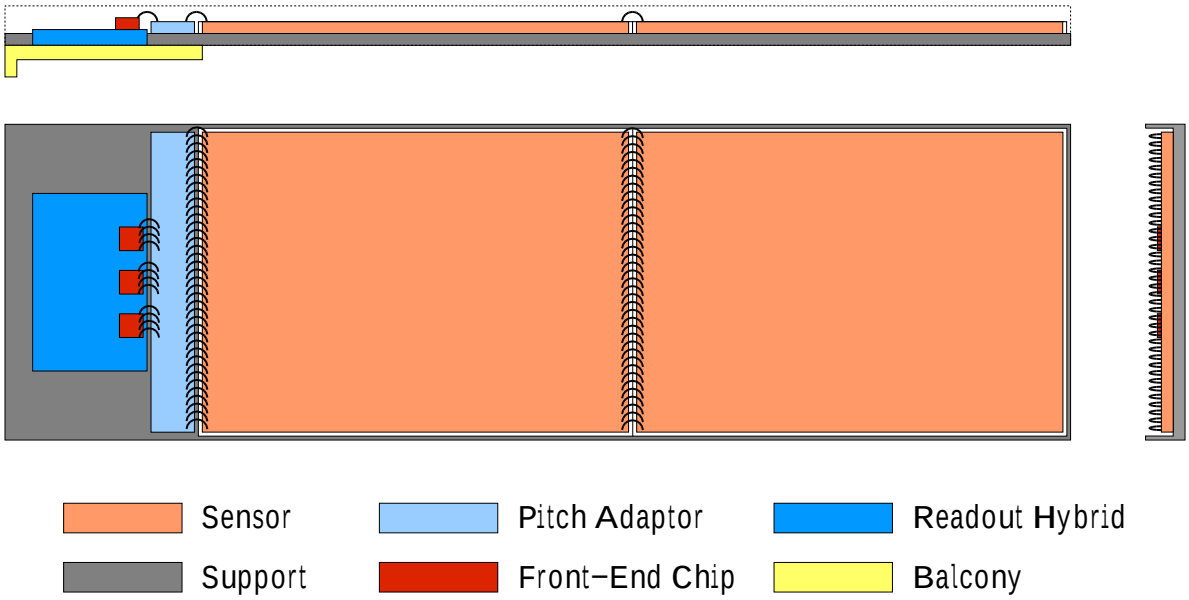


Figure 2.10: Schematic layout of a 2-sensor silicon ladder [Ste02].

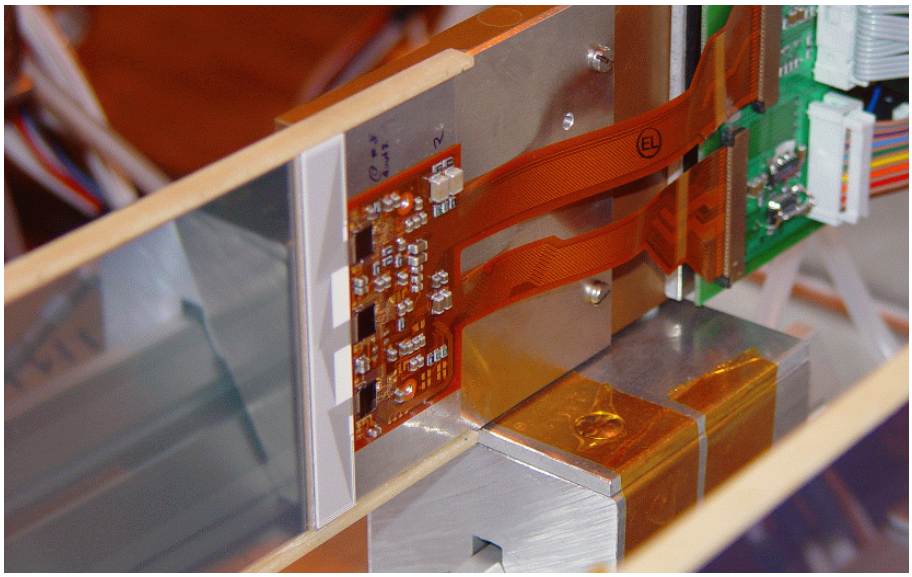


Figure 2.11: Photography of an ITR hybrid used in the 2002 test beam. Three *Beetle1.1* chips read out the silicon sensor [ITR].

RICH

Particle identification is an essential requirement of the LHCb experiment. For $\mathcal{CP}$-violation measurements, the distinction between pions and kaons is important. For example [RIC00], the detection of the channel $B_d^0 \to \pi^+\pi^-$ requires the rejection of $B_d^0 \to K^+\pi^-$, $B_s^0 \to K^-\pi^+$ and $B_s^0 \to K^+K^-$, which have the same topology. The two left pictures in fig. 2.12 show the mass spectrum of $B_d^0 \to \pi^+\pi^-$ without and with particle identification by the RICH. Another important channel is $B_s^0 \to D_s^{\mp}K^{\pm}$ which is used to extract the $\mathcal{CP}$ angle γ. The background from $B_s^0 \to D_s^-\pi^+$ dominates by a factor of ~ 15. The mass spectrum of $B_s^0 \to D_s^{\mp}K^{\pm}$ without and with RICH application is depicted in the two right pictures of fig. 2.12.

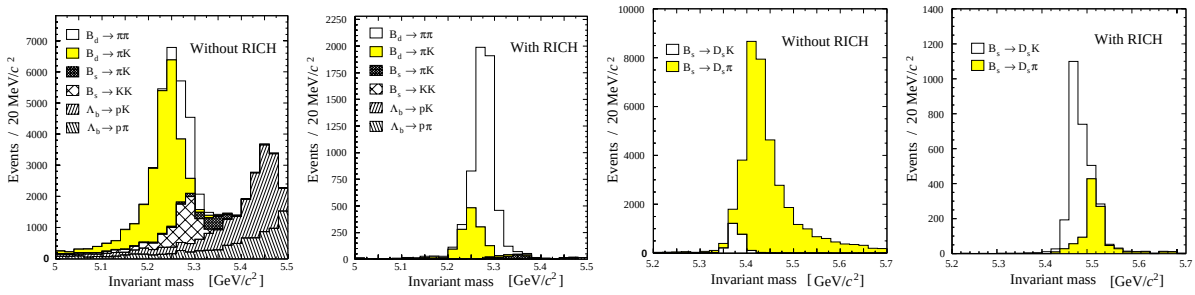


Figure 2.12: Mass spectrum of $B_d^0 \to \pi^+\pi^-$ (left) and of $B_s^0 \to D_S^-K$ (right) without and with RICH respectively [RIC00].

The required momentum range to be covered by the RICH detectors is $1 - 150\,\mathrm{GeV/c}$. The upper limit required for π−K separation is determined by $B_d^0 \to \pi^+\pi^-$. 90% of the pions have $p < 150\,\mathrm{GeV/c}$. The lower momentum limit of $1\,\mathrm{GeV/c}$ is defined by tagging kaons and tracks of high multiplicity decays. To cover the whole momentum range three radiators with different refractive indices are used. RICH1 uses silica aerogel (n=1.03) and C_4F_{10} gas (n=1.0014). It covers the momentum range up to $70\,\mathrm{GeV/c}$. The angular acceptance matches the one from the complete spectrometer. RICH1 is positioned in front of the magnet and the shielding wall. RICH2 covers a momentum range of $15 - 150\,\mathrm{GeV/c}$ using gaseous CF_4 (n=1.0005) and is placed between the tracking stations and the calorimeter system. The schematic layout of both RICH detectors is shown in fig. 2.13.

The photodetectors, which collect the Cherenkov light are placed outside the acceptance. As a baseline, pixel hybrid photo detectors (HPD) are used, which are read out with a dedicated 1,024 channel binary pixel chip in deep-submicron CMOS technology. As a back-up, multianode photomultiplier tubes (MaPMT) are foreseen. They will be read out by the *Beetle* chip.

2.3 Radiation Levels at LHCb

The vertex detector system is subject to the highest particle fluxes in the LHCb cavern. The innermost detector regions of the VELO experience a particle flux which is equivalent to 1.3×10^{14} 1 MeV neutrons per cm^2 (fig. 2.14).

The radiation levels in the LHCb cavern have been calculated with the *FLUKA* [FLU] software [Rad]. Table 2.4 summarises the total dose and particle fluxes in the place of the detector hybrids for the VELO and ITR systems.

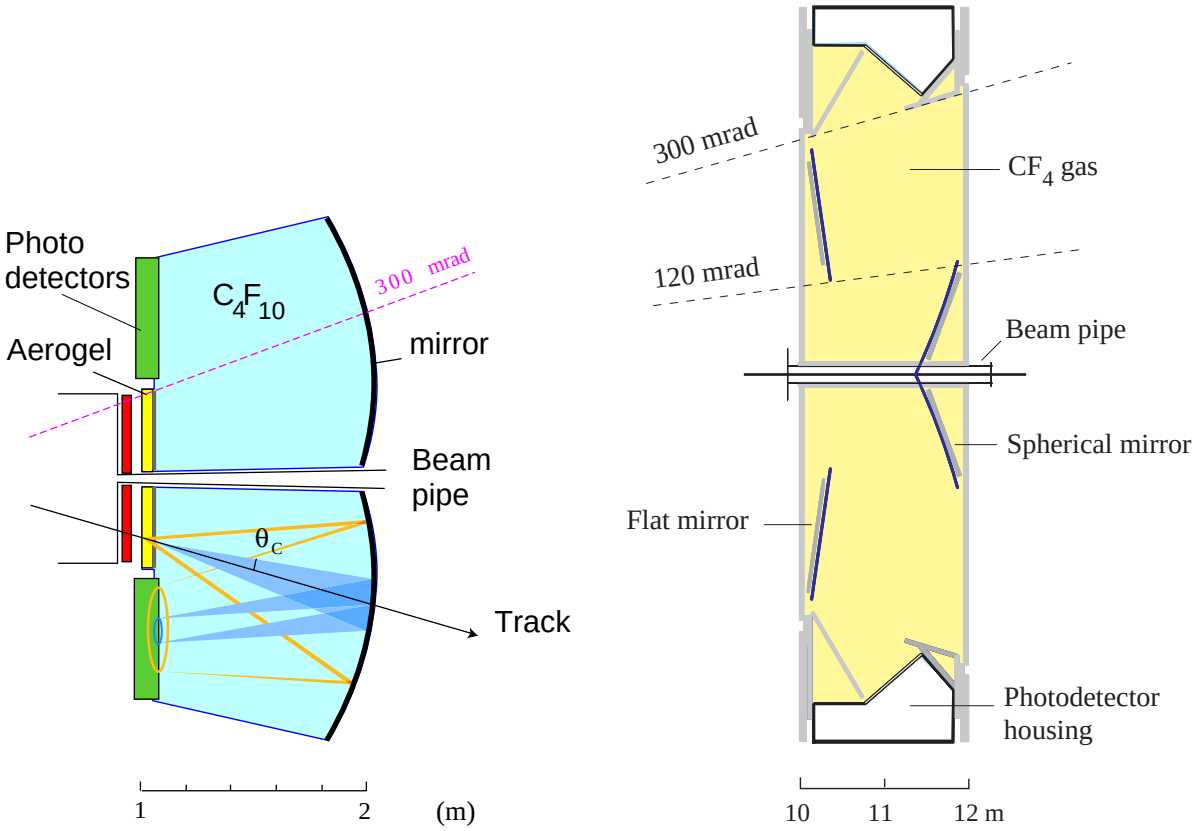


Figure 2.13: Layout of RICH1 (left) and RICH2 (right) [RIC00].

2.4 The Trigger and Readout System of LHCb

LHCb uses a multi-level trigger and data acquisition (DAQ) system. It's task is the reduction of the primary data rate of 40 TB/s to a reasonable level for storage. The trigger decision is subdivided into 4 levels (see fig. 2.15):

- *Level-0* is a hardware trigger with a fixed latency of max. 4 μs. At an input rate of 40 MHz (bunch-crossing frequency) events from the ECAL, HCAL and muon detectors are processed. The VETO detector rejects events with more than one primary pp-interaction. The trigger algorithm searches for electrons, photons, muons and hadrons with a high transverse momentum (high-p_T), which is significant for B-events. High transverse momenta are $1-2$ GeV/c, which is large compared to typically $p_T \approx 300$ MeV/c in hadronic interactions. The output rate is 1 MHz, which means a reduction of data by a factor 40 in this first stage.

- *Level-1* is a software trigger operating at an input rate of 1 MHz with a variable latency of up to 256 μs. Data from the VELO, the Inner and Outer Tracker detectors are used, to reconstruct the secondary vertices on the one hand and to confirm the high-p_T-track of *Level-0* on the other. The output rate is 40 kHz, resulting in a reduction-factor of 25.

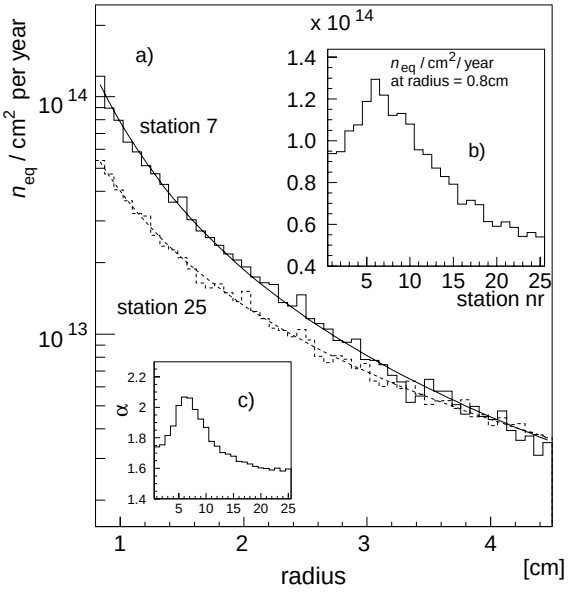


Figure 2.14: Total hadron flux normalised to the damage of neutrons of 1 MeV for VELO stations 7 and 25 as a function of radius [VEL01]. The radial dependence follows well $r^{-\alpha}$. The parameter α is plotted in c) as a function of the station number. b) shows the flux per year at a radius of 8 mm as a function of the station number.

- *Level-2* is also realised in software, providing a latency of up to 10 ms at an input rate of 40 kHz. The vertex reconstruction of the previous stages is revised by correlating the tracks of the vertex detector and the tracking detectors.
- *Level-3* completes the event building at an input rate of 5 kHz using the complete detector information. The final states are reconstructed. The latency of this stage is variable up to 200 ms, the *Level-3* accept rate is 200 Hz.

The overall reduction-factor of the four trigger levels is 2×10^5, resulting in a data storage rate of 20 MB/s. The reduction in the data rate is even one order of magnitude larger (2×10^6) due to zero-suppression.

	x [m]	y [m]	z [m]	total dose [Mrad]	1 MeV eq. neutrons $[10^{13}\mathrm{cm}^{-2}]$	hadrons > 20 MeV $[10^{13}\mathrm{cm}^{-2}]$
VELO						
	$r = 0.05 - 0.1$		$-0.2 - 0.8$	$5.8 - 2.5$	$9.0 - 4.1$	$14 - 5.6$
Inner Tracker						
TT	$-0.7 - 0.7$	$-0.68 - 0.68$	$2.29 - 2.34$	$7.0 - 0.37$	$8.7 - 0.66$	$13 - 0.47$
T1				$1.1 - 0.49$	$1.2 - 0.58$	$1.4 - 0.55$
T2				$0.83 - 0.34$	$1.1 - 0.57$	$1.1 - 0.52$
T3				$0.95 - 0.37$	$1.2 - 0.62$	$1.1 - 0.46$

Table 2.4: Calculated total dose and particle fluxes in 10 years of operation in the place of the detector hybrids for the VELO and ITR systems [Rad].

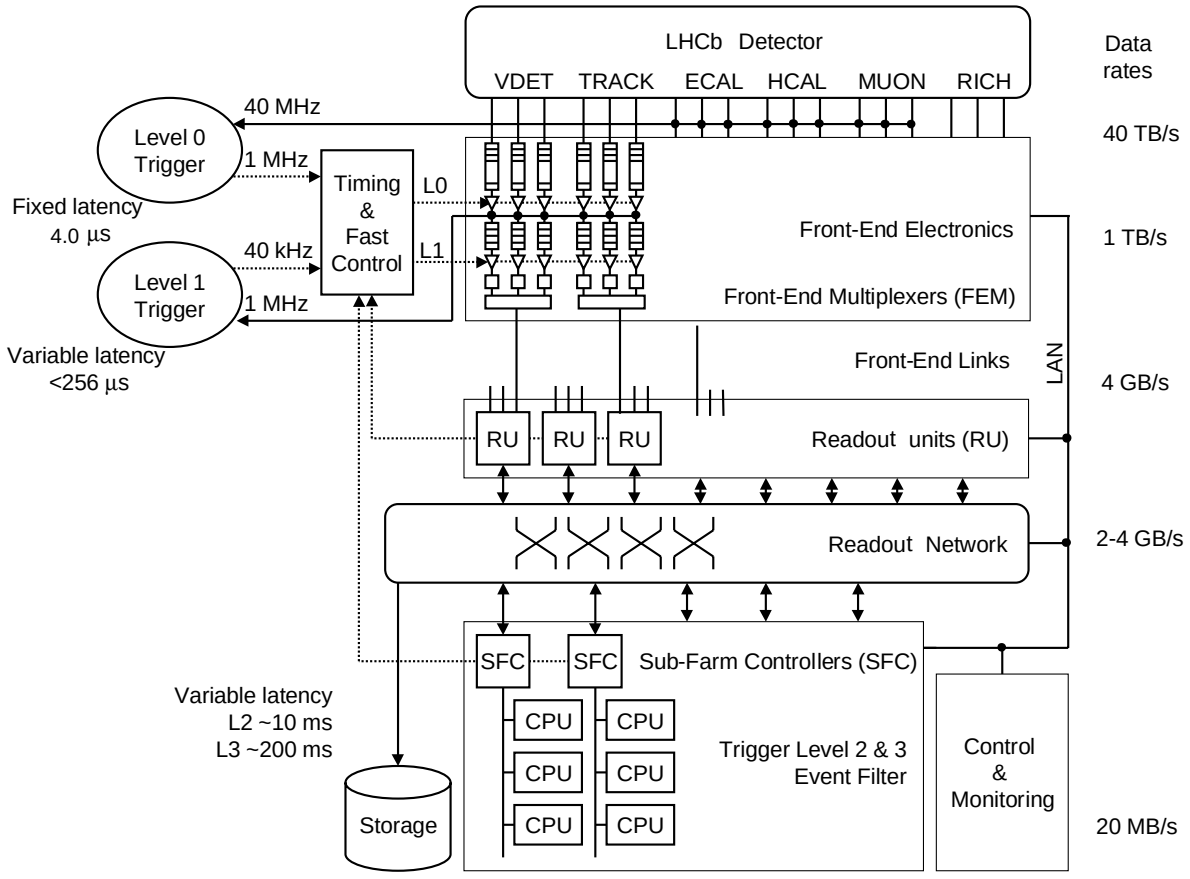


Figure 2.15: Architecture of the LHCb trigger and DAQ system [LHC98].

Chapter 3

Radiation Hard VLSI Electronics

Radiation resistant[1] electronics is used in space applications, e.g. space flight missions or satellites, avionics, nuclear power plants instrumentation, military applications and high energy physics experiments. The radiation environments of these applications differ in radiation type, energy, dose and fluence and make quite distinct demands on the electronic devices.

High energy physics experiments of the LHC generation deal with dose rates of up to 10 Mrad/a and fluences of $10^{15} cm^{-2}$ (neutrons and hadrons). These hostile radiation environments require radiation hard electronics especially for the innermost detector regions which are close to the beam pipe. The complexity of today's electronic readout systems for silicon strip or pixel detectors, which are usually used in high fluence environments, requires the application of VLSI (Very Large Scale Integration) circuits. The major effects of radiation on integrated circuits will be discussed in this chapter, though the treatment will be restricted to *silicon* devices which comprise the bulk of radiation hard electronics.

3.1 Radiation Damage in Microelectronic Devices

Radiation effects in (micro)electronic devices can be categorised into *cumulative* effects and *single event effects* (SEE). Cumulative radiation damage is a gradual effect which occurs during the complete lifetime of a device. It is subdivided into ionising (*total ionising dose*) and non-ionising (*displacement*) damage. Potentially all kinds of electronic components are subject to total ionising dose (TID) effects which primarily depend on the absorbed energy, independent of the type of radiation[2]. Displacement damage depends on the energy and momentum transfer of incident particles to lattice atoms and is mainly an issue in bipolar transistors and optoelectronic devices. Since the non-ionising energy loss (NIEL) depends on mass and energy of the incident radiation, displacement damage must be specified for a certain radiation type. Single Event Effects are caused by the passage of a *single particle* through a sensitive area of the device. They are distinguished into *destructive* and *non-destructive* effects. The latter ones result in a temporary malfunction or the change of a logic state in digital memories. In the following, cumulative effects will be discussed in detail for MOS and bipolar transistors

[1] Devices coping with doses up to a few hundred krad are usually designated as radiation *tolerant*, for doses of several Mrad the term radiation *hard* is used.

[2] Dose is defined as absorbed energy per mass and is measured in Gy = J/kg = 100 rad = 10^4 erg/g. Since the charge liberated by a given energy depends on the material (e.g. the electron-hole pair creation energy is 3.6 eV in silicon and 17 eV in SiO_2), the absorber under study has to be specified (e.g. rad(Si), rad(SiO_2)).

respectively. The treatment of single event effects will be restricted to those being relevant for deep-submicron CMOS technologies.

3.1.1 Technology Scaling

Technology scaling, i.e. the changing of the device parameters from one process generation to the next, has both beneficial and detrimental effects on radiation hardness. Hence, scaling aspects will be shortly treated here. The three major objectives of technology scaling are an increase of the transistor density, a higher circuit speed, i.e. a decreased gate delay, and a reduction in power consumption. VLSI technology generations are characterised by their minimum structure width, which is in case of MOS technologies the length of the gate electrode. For technologies below $0.8\,\mu$m minimum structure width the underlying scaling principle in going to the next process generation is the so-called *constant-field scaling*. All geometrical dimensions and process parameters are scaled in a way, that the electric fields in the device remain unchanged. Compared to *constant-voltage scaling* which keeps the power supply voltage constant, the risk of gate-oxide breakdown is avoided. Table 3.1 lists the scaling factors of various device parameters for a constant-field scaling by factor k. Present technology scaling uses a factor $k \approx 1.43$ ($1/k = 0.7$), i.e. a 30 % parameter change.

parameter		factor		
vertical dimensions	d	k^{-1}		
lateral dimensions	W, L	k^{-1}		
voltages	V	k^{-1}		
impurity concentrations		k		
gate (die) area	$\propto (W \times L)$	k^{-2}	$\doteq$	0.49
transistor density	$\propto (W \times L)^{-1}$	k^{2}	$\doteq$	2
capacitance (per unit area)	$\propto (W \times L)/d$	k^{-1} (k)	$\doteq$	0.7 (1.43)
drain current I_D	$\propto (W/L \times V^2/t_{ox})$	k^{-1}	$\doteq$	0.7
gate delay (frequency f)	$(C \times V)/I$	$k^{-1}(k)$	$\doteq$	0.7 (1.43)
power	$C \times V^2 \times f$	k^{-2}	$\doteq$	0.48
power density	$(C \times V^2 \times f)/(W \times L)$	1		
power-delay product	$(C^2 \times V^3 \times f)/I$	k^{-3}	$\doteq$	0.34

Table 3.1: Constant-field scaling of various process parameters. The numerical values are given for $k \approx 1.43$.

A beneficial effect of scaling concerning radiation hardness is the higher tolerance of total ionising dose (section 3.2.1). Process modifications beside scaling, like an epitaxial substrate (highly doped substrate), trench isolations between active devices and retrograde wells (wells with a special doping profile), reduce the sensitivity to Single Event Latch-up (section 3.1.4). A deficiency due to scaling is an increased susceptibility to Single Event Upset (section 3.1.4). Note, that the expression for power consumption given in table 3.1 is valid only for *digital* systems ($P_{digital} = V^2 C f$). In *analogue* circuits the power consumption is given by [Vit02]:

$$P_{analogue} = 8 k_B T f \cdot \frac{S}{N} \cdot \frac{V_S}{V_{pp}} \tag{3.1}$$

with
S/N the signal-to-noise ratio,
f the signal frequency,
V_S the supply voltage,
V_{pp} the signal swing.

A minimum is reached for rail-to-rail signal swing, i.e. $V_{pp} = V_S$. $P^{min}_{analogue} = 8k_BTfS/N$ which is independent of the supply voltage and only depends on thermal noise ($\propto k_BT$), signal-to-noise ratio and bandwidth. Hence, a decrease in supply voltage does not reduce analogue power consumption and may even lead to an increase. The threshold voltage V_{th} is not scaled down as fast as the supply voltage in order to maintain low leakage currents [Enz02]. This leads to a decrease of the overdrive voltage ($V_{gs} - V_{th}$) which can be compensated by an increase of the oxide capacitance C_{ox} or of the transistor aspect ratio W/L but moves the operation points from strong to moderate or even weak inversion.

3.1.2 Cumulative Effects in MOS Transistors

In contrast to bulk devices like e.g. silicon detectors, MOS transistors are *surface devices*. The active structures (diffusion region, conducting channel) penetrate only a few micrometres into the silicon bulk which has typically a depth of 300 μm. Displacement damage primarily causes a reduction in minority carrier lifetime in the silicon substrate. Since the properties of MOS transistors do not significantly depend on the minority carrier lifetime, MOSFETs are relative insensitive to displacement damage. In general, displacement damage in MOS devices is of secondary concern. The primary source of device degradation under irradiation is damage by ionisation in the surface layers. It will be treated more detailed in the subsequent section.

Total Ionising Dose Effects

The part of a MOS transistor which is most sensitive to ionising radiation is the *insulator layer* (silicon dioxide) between the silicon substrate and the electrodes. It has a depth of a few nanometres[3] underneath the gate electrode (gate oxide) and some 10 nm above the source and drain diffusion regions (field oxide). Typically, field oxides are an order of magnitude thicker than gate oxides. Two basic radiation-induced effects exist [Dre89]:

- *trapping of holes* in the silicon oxide near the Si/SiO_2 interface,
- Si/SiO_2 *interface traps* producing inter-bandgap states in the silicon.

Fig. 3.1 depicts the energy band diagram of a MOS structure with a positive gate bias. The processes (1) to (3) depict the generation of hole traps in the oxide, (4) indicates the formation of interface traps which result in inter-bandgap states. An ionising particle penetrating the oxide generates electron-hole pairs (1) (the pair creation energy in SiO_2 is 17±1 eV). Electrons have a $10^4 - 10^{11}$ times higher mobility (depending on temperature and electric field) in SiO_2 compared to holes ($\mu_n^{SiO_2} \approx 20\,cm^2V^{-1}s^{-1}$) and escape out of the oxide in the order of 1 ps. The electron velocity in SiO_2 saturates at about $10^7\,cm/s$. The fraction of holes remaining from recombination with electrons is subject to a transport mechanism through localised states in the silicon oxide (2). Two possible hole transfer mechanisms are the trap-mediated valence band

[3] 6.2 nm in case of the 0.25 μm CMOS process the *Beetle* is fabricated in.

hole conduction and a hopping transport via direct hole tunnelling between localised trap sites (fig. 3.4). In case of a positive gate voltage the holes propagate towards the Si/SiO_2 interface. The time scale for this process is in the order of 1 s at room temperature. At the interface a fraction of the holes is captured in long-term traps (3). This causes a remnant negative voltage shift (e.g. in threshold voltage V_{th} or flatband voltage V_{FB}) which is insensitive to the silicon surface potential and which can persist in time for hours to years. The voltage shift is the most commonly observed form of radiation damage in MOS devices. The buildup of interface traps at the Si/SiO_2 boundary (4) also contributes a voltage shift component which depends on the silicon surface potential.

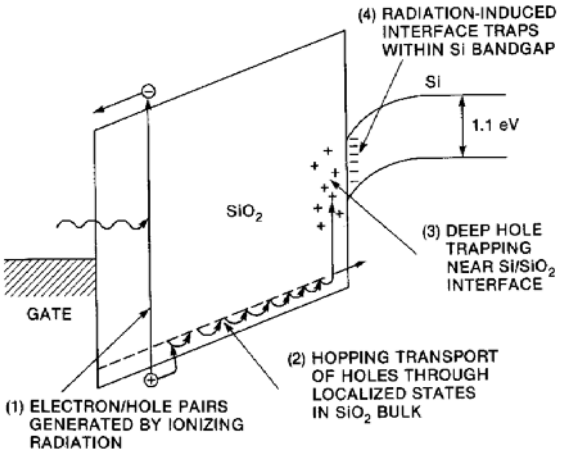


Figure 3.1: Energy band diagram of a Metal-Oxide-Semiconductor structure with a positive gate voltage applied [McL89].

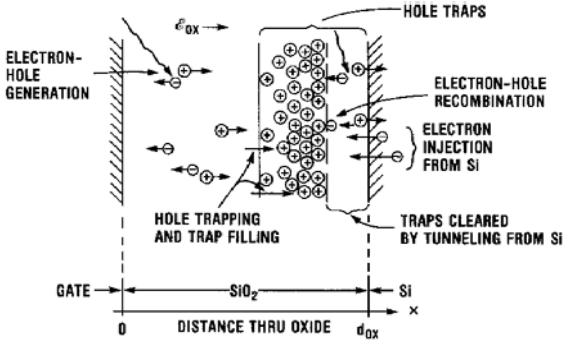


Figure 3.2: Hole trapping in the oxide of a MOS structure under positive gate bias ($d_{ox} = t_{ox}$) [McL89].

The microscopic nature of hole traps is the so-called E' *centre* which is a trivalent silicon defect associated with an oxygen vacancy in the SiO_2 structure created under irradiation. The Si/SiO_2 interface is extremely sharp, i.e. the transition from silicon to SiO_2 takes place in one atomic layer[4]. However, the first $1 - 4$ nm of oxide is a region of strained bonds with the presence of *oxygen vacancy* defects (E_1' centres in which the silicon atoms are directly bonded together without an oxygen atom in between them: $O_3 \equiv Si–Si \equiv O_3$). A hole encountering such a strained bond may break it and recombine with one of the bonding electrons (fig. 3.3). A positive charged structure results which relaxes into the E_1' centre configuration. This process is reversible if an electron is supplied to reform the Si-Si bond (annealing).

The trapped holes in the silicon oxide are not permanently captured. Two different *annealing* processes exist. The hole discharge by *tunnelling* at temperatures below about 150° C is slow (with a roughly $\log(t)$ behaviour) and shows a bias dependency. The *thermal* annealing (typical temperatures are 150° to 350° C) is rapid and strongly temperature-dependent.

The second major radiation damage effect in MOS devices is due to Si/SiO_2 *interface traps*. The interface between the crystalline silicon and the amorphous oxide is deficient of oxygen, resulting in strained and dangling silicon bonds. These dangling bonds give rise to interface traps or -states with energy levels within the silicon bandgap (the pre-irradiation interface-trap density is in the range of $10^9 - 10^{10}\, cm^{-2}$ but extremely dependent on processing details).

[4]Results from electron spin resonance (ESR) and X-ray photoelectron spectroscopy (XPS)

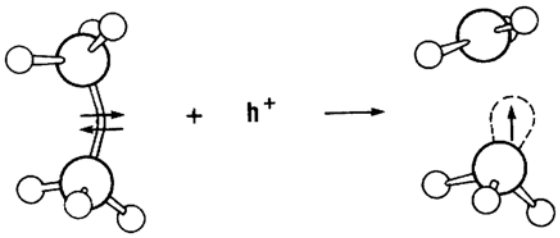


Figure 3.3: Model for hole trapping in SiO_2 with E' centre formation [McL89].

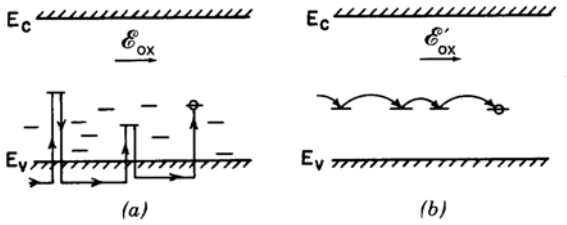


Figure 3.4: Schematic of possible hole transport mechanisms in SiO_2. (a) trap-mediated valence band hole conduction, (b) phonon-assisted hopping transport via direct tunnelling between localised trap sites within the SiO_2 bandgap [McL89].

Ionising radiation can induce additional interface traps. They are classified as either donors or acceptors with possible charge states being positive, neutral or negative. The most favoured model identifies interface states in the upper part of the bandgap as acceptors, in the lower part as donors.

The buildup of interface states depends on a multitude of variables, like dose, dose rate, electric field, temperature, radiation energy, oxide thickness t_{ox} etc. Only a few comments should be made here on dose D and t_{ox}: the dependence on dose follows a $D^{2/3}$ law. Thin oxides help hardening a circuit, since the trap creation follows a t_{ox}^n dependence, with $n = 0.5 - 2.0$ in a t_{ox}-range of 15 to 100 nm.

The microscopic nature of interface traps is identified as *paramagnetic centres* in MOS structures. They are very similar to E' centres. One centre, called P_{b0}, is a "trivalent silicon", i.e. a silicon atom bonded to three other silicon atoms with a single dangling orbital perpendicular to the Si/SiO_2-interface ($\cdot Si{\equiv}Si_3$). The P_{b1} center is interpreted as a $\cdot Si{\equiv}Si_2O$ structure.

Consequences on Device Characteristics

MOS transistors exposed to ionising radiation suffer degradation in their performance parameters. They experience

- a shift in threshold voltage,
- a decrease in gain (transconductance g_m) and speed (slope of the $I - V$ characteristic)
- and an increase of leakage currents.

This section will detail the parameter changes and relate them to the primary radiation effects discussed above.

Both basic radiation effects related with the oxide layer of a MOS structure, hole trapping and interface states, are contributing to a voltage shift in the electrical characteristics, i.e. in the threshold voltage V_{th}. The various processes contributing to the buildup of a (negative) shift in V_{th} due to hole trapping in the silicon oxide are shown schematically in fig. 3.2 for a MOS structure with oxide thickness t_{ox} and positive gate bias. Most of the holes generated in

the oxide are captured by hole traps within a distance of $2-5\,\mathrm{nm}$ from the silicon. The shift in V_{th} resulting from the trapped holes is given by

$$\Delta V_{th} = -\frac{q}{\epsilon_{ox}} t_{ox} \rho_A^{ptr}, \tag{3.2}$$

where ρ_A^{ptr} is the (trapped) hole charge density per unit area referred to the Si/SiO_2 interface given by

$$\rho_A^{ptr} = \frac{1}{t_{ox}} \int_0^{t_{ox}} n_{ptr}(x) x dx \tag{3.3}$$

with n_{ptr} being the local density of trapped holes. Applying several assumptions, an analytical form for ΔV_{th} can be derived [McL89]. Representing the density of hole traps N_{ptr} by an average density $\langle N_{ptr} \rangle$ extending a distance $\delta x \ll t_{ox}$ from the Si/SiO_2 interface, assuming uniform hole generation in the oxide and a positive gate bias and neglecting any recombination processes (electron/trapped-hole recombination and trap filling by electrons), it follows, that

$$\Delta V_{th}(\mathcal{E}_{ox}, E) = -\frac{q}{\epsilon_{ox}} \cdot K_g(E) \cdot f_y(\mathcal{E}_{ox}, E) \cdot f_{tr}(\mathcal{E}_{ox}) \cdot t_{ox}^2 \cdot D(E) \propto t_{ox}^2 \tag{3.4}$$

with
$\mathcal{E}_{ox}$ the effective electrical field in the oxide,
E the energy of the ionising radiation,
K_g the charge generation coefficient,
f_y the fraction of generated charge that remains free,
f_{tr} the fraction of radiation generated holes that are trapped,
t_{ox} the thickness of the silicon oxide,
D the accumulated dose in Gy.

This square-dependence of the V_{th}-shift on oxide thickness in MOS structures is indicated by the dashed line in fig. 3.19. This model is valid for oxide thicknesses $t_{ox} > 10\,\mathrm{nm}$, where the assumption $\delta x \ll t_{ox}$ (δx is the distance of hole traps to the Si/SiO_2 interface) is still applicable. For thinner oxides, trapped holes are rapidly removed by *tunnelling* (fig. 3.19).

Fig. 3.5 shows the shift in V_{th} as a function of dose. At low accumulated doses ($< 10^5\,\mathrm{rad(Si)}$) the contribution of trapped oxide charges dominates and results in a decrease of V_{th}. Above $10^5\,\mathrm{rad(Si)}$ negatively charged acceptor (for NMOS) and positively charged donor interface traps (for PMOS) transistors are formed. For NMOS transistors this results in a turnaround (or "rebound") of the V_{th}-shift, PMOS devices continue their threshold voltage decrease.

A geometrical effect influencing the radiation hardness of a MOS device is the presence of leakage paths in a standard, i.e. linear, MOS transistor. In LOCOS[5] CMOS technology a thick field-oxide (the thickness t_{fox} is typically an order of magnitude large than the gate-oxide thickness t_{ox}) is used to define the channel width and to isolate the active devices from each other. It also allows interconnection layers to be routed on top without inadvertently forming a conductive channel at the silicon surface. Under irradiation, the field-oxide traps more charges than the gate-oxide (t_{ox}^2-dependence, cf. eq. 3.4). For oxide layers over p-type substrate, i.e. n-channel isolation, the threshold voltage can be reduced below zero, which turns the device on and leakage currents will flow. Two possible leakage paths exist: an "end-around" leakage between source and drain and a leakage between the n-channel source and the n-well (in a p-substrate, n-well technology). The latter effect is independent of the gate voltage and

[5] LOCal Oxidation on Silicon

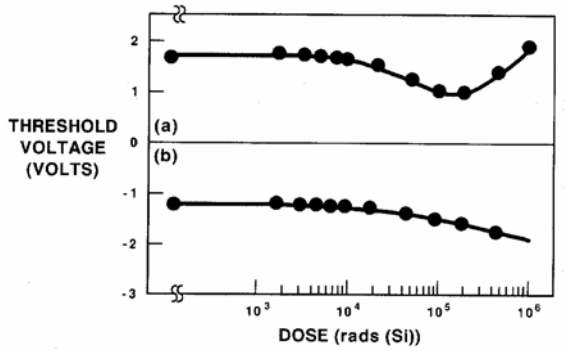


Figure 3.5: Threshold voltage shift of an NMOS (a) and PMOS (b) transistor vs. accumulated dose [Win89].

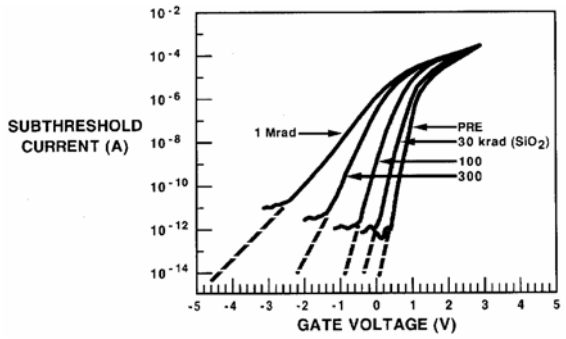


Figure 3.6: Variation of the subthreshold slope under irradiation [Win89].

contributes to the overall leakage of the integrated circuit. The "end-around" leakage is caused by trapped holes in the transition region of field- and gate-oxide, called *"bird's beak"* due to the profile of the oxide (see fig. 3.7). As a result, parasitic transistors in parallel to the active device are present, as indicated in fig. 3.7.

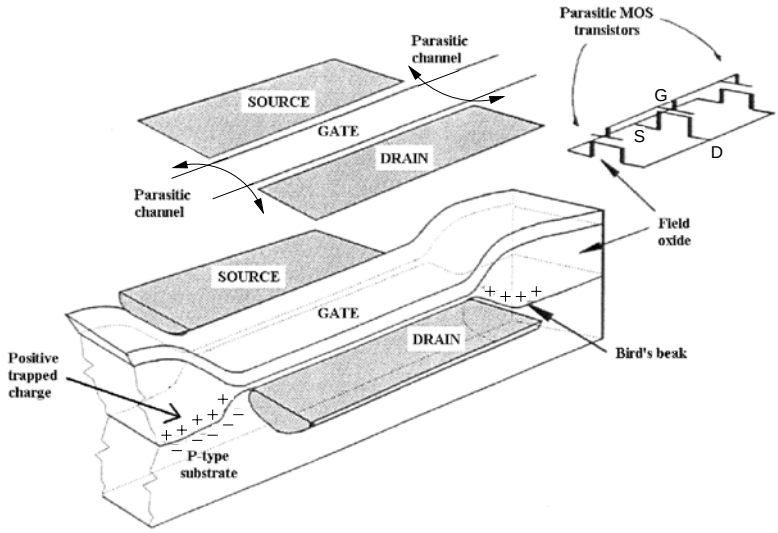


Figure 3.7: Leakage currents in NMOS transistors through parasitic paths between source and drain. The transition region from gate- to field-oxide is called *bird's beak* due to it's profile [Gai95].

Radiation-induced interface traps modify the $I-V$ characteristics of a transistor. Sweeping the gate voltage results in filling or clearing interface states which modifies the voltage needed to generate a certain surface potential in the silicon. In the subthreshold region, typical changes are a decrease of the $I-V$ *slope* (fig. 3.6), which affects the switching speed of a FET (a higher swing in gate voltage is required to bring the transistor to strong inversion). In strong

inversion, the $I-V$ slope suffers from a *degradation of mobility* as a consequence of interface traps. Experimental data (fig. 3.8) can be fitted by the empirical expression

$$\mu = \frac{\mu_0}{1+\alpha\cdot\Delta n_{it}} \propto D^{-2/3} \tag{3.5}$$

where μ_0 is the value before irradiation, $\alpha = (8\pm 2)\times 10^{-13}\, cm^2$, $\Delta n_{it} \propto D^{2/3}$ is the interface-trap density and D the accumulated Dose in Gy. A reduction of mobility leads to a degradation of subthreshold slope, transconductance, circuit speed, etc.

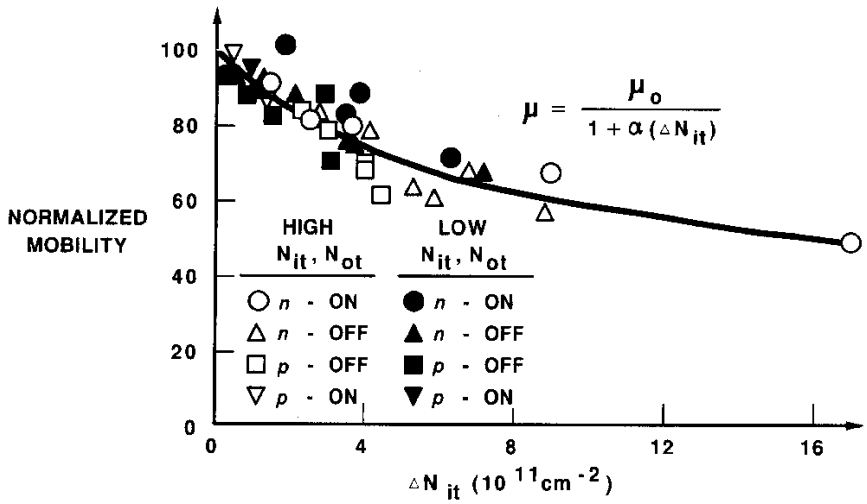


Figure 3.8: Reduction of the mobility as a function of interface-trap density [Win89].

The small-signal transconductance $g_m = \delta i_D/\delta v_{GS}|_{v_{GS}=V_{GS}}$ (the slope of the $i_D - v_{GS}$ characteristic at the bias point V_{GS}) is given by

$$g_m = k_n'\frac{W}{L}(V_{GS}-V_{th}) = \sqrt{2k_n'\frac{W}{L}I_D} = \frac{2I_D}{V_{GS}-V_{th}} \tag{3.6}$$

with $k_n' = \mu_n C_{ox}$. Depending on the bias condition, the degradation of g_m resulting from a mobility reduction is

$$g_m|_{V_{GS}=const.} = \frac{g_{m0}}{1+\alpha\cdot\Delta n_{it}} \quad \text{for fixed voltage biasing} \tag{3.7}$$

$$g_m|_{I_D=const.} = \frac{g_{m0}}{\sqrt{1+\alpha\cdot\Delta n_{it}}} \quad \text{for fixed current biasing.} \tag{3.8}$$

Hence, constant current biasing is less sensitive to mobility degradation.

The only effect of *non-ionising* radiation damage in MOS devices is an increase of leakage currents in reverse-biased *pn*-junctions. As will be detailed in section 3.1.3, displacement damage causes the creation of mid-bandgap states which increases the dark current of diodes [Spi96]

$$I_R = I_{R0} + \alpha \cdot \phi \cdot A \cdot d_{junction}, \tag{3.9}$$

with
I_{R0} the reverse current before irradiation,
α the damage coefficient dependent on particle type and fluence ($\alpha \approx 3 \cdot 10^{-17}$ for 650 MeV protons and $\alpha \approx 2 \cdot 10^{-17}$ for 1 MeV neutrons),
ϕ the particle fluence,
A the detector area,
$d_{junction}$ the thickness of the depletion region.

Table 3.2 summarises the performance parameter changes in MOS transistors due to radiation together with the corresponding primary radiation effects.

consequence on device characteristic	primary radiation effect			
	trapped charges in field oxide	trapped charges in gate oxide	Si/SiO_2 interface states	bulk doping
NMOS	leakage currents	neg. V_{th}-shift	reduction of g_m pos. V_{th}-shift degradation of sub-threshold slope	leakage currents in *pn*-junctions
PMOS	reduction of W_{eff}	neg. V_{th}-shift	reduction of g_m neg. V_{th}-shift degradation of sub-threshold slope	leakage currents in *pn*-junctions

Table 3.2: Summary of radiation effects in CMOS devices.

3.1.3 Cumulative Effects in Bipolar Transistors

Total Ionising Dose Effects

TID effects in bipolar transistors are related to the oxide isolation (field oxide) at the silicon surface which is necessary to avoid cross-coupling between adjacent devices. Trapped charges in the oxide and Si-SiO_2-interface states are the primary radiation damages (cf. 3.1.2). Devices most sensitive to these effects are *lateral* BJTs[6]. Usually it is desirable to have both MOS and bipolar transistors available in the same process technology. BiCMOS technologies (with a *p*-substrate and *n*-wells) provide a lateral *pnp*-transistor which is compatible with the CMOS process. Emitter, base and collector of the *pnp*-transistor are arranged along the surface with large area exposure to the oxide. Leakage currents along the surface increase the base current and in turn degrade the gain (see fig. 3.12). Vertical bipolar transistors are far less susceptible to ionising radiation, since they are embedded into the silicon bulk.

An effect not present in MOS devices is the dependency of ionising radiation damage in bipolar transistors on the *dose rate*. The effect shows an extreme variability in different processes, i.e. it is not existent in some and strong in others. Where it is present, an enhanced degradation at *low* dose rates appears. The source of this effect are trapped charges in the oxide above the base-emitter junction.

Displacement Damage

Displacement damage depends on the mass and energy of the incident particle and creates *defect clusters* in the lattice. About 20 eV need to be transferred to a silicon atom to release it from it's lattice position. A 1 MeV neutron for example, transfers about 60 to 70 keV to the silicon recoil atom which in turn displaces about 1000 other atoms in a region of 0.1 μm size [Spi96]. The non-ionising energy loss (NIEL) for a variety of particles has been calculated. The relative damage is depicted in fig. 3.9.
Displacement damage results in three effects:

- formation of *mid-bandgap states* which give rise to carrier generation or recombination. Electrons or holes can be emitted from the mid-gap state or captured[7]. Which mechanism dominates depends on the relative concentration of carriers and defect states. In depletion regions of reverse-biased *pn*-junctions mid-gap states contribute to the leakage current due to charge generation. In forward biased regions, like the base-emitter junction of a BJT, or non-depleted regions, mid-gap states enable recombination which leads to a loss of charge carriers.

- creation of *states near the bandgap edges* which lead to charge trapping.

- change in the *doping* characteristics influences the width of depletion layers or the voltage necessary to achieve full depletion.

[6] Bipolar Junction Transistor
[7] Without these intermediate states a transition of an electron from the valence to the conduction band is extremely improbable (in case of silicon), since silicon is an indirect semiconductor. The mid-gap states work like "stepping stones".

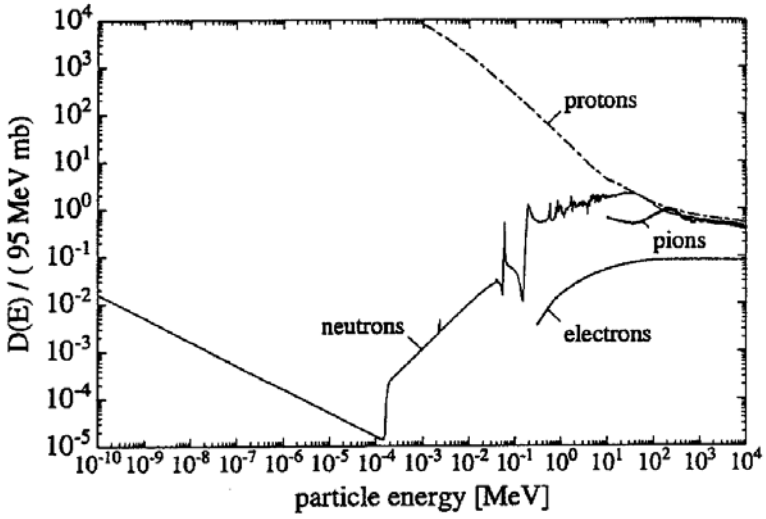


Figure 3.9: Energy dependence of non-ionising energy loss (NIEL) in silicon for various types of radiation [Lut99, Vas00]. The ordinate shows *displacement damage cross section D* normalised to the value for 1 MeV neutrons of 95 MeVmb. D is equivalent to NIEL: $D = 100\,MeVmb = 2.144\,keVcm^2g^{-1}$ = NIEL (NIEL-scaling hypothesis).

Consequences on Device Characteristics

The most important consequence of irradiation on the device characteristics of bipolar transistors is the *degradation of DC current gain* at low currents. The formation of *mid-bandgap states* by displacement damage accounts for that. The base-emitter junction of a BJT is usually forward-biased giving a high carrier concentration in the conduction band. The mid-gap states capture free carriers and give rise to recombination. The degradation of DC current gain depends on the emitter current density, since the fractional carrier loss is related to the relative concentration of carriers and defect states. Fig. 3.10 shows the DC current gain of a *npn* and *pnp* transistor before and after irradiation with 800 MeV protons to a fluence of $1.2 \times 10^{14}\,cm^{-2}$. For a given collector current, a small device will suffer less degradation in DC current gain. Smaller devices give rise to a higher thermal noise contribution which has to be considered carefully. Also a reduced base width helps hardening the device, since the probability of recombination depends on the transit time through the junction region. For example, at a current density of $2\,\mu A/\mu m^2$ the degradation in gain is 60% for the *pnp* transistor.
Also a noise degradation has been measured. Fig. 3.11 shows the spectral noise density of an integrated preamplifier before and after irradiation with 800 MeV protons to a fluence of $1.2 \times 10^{14}\,cm^{-2}$.

A consequence of ionising radiation damage is the degradation of the gain β of the BJT. A measurement for various devices is presented in fig. 3.12.

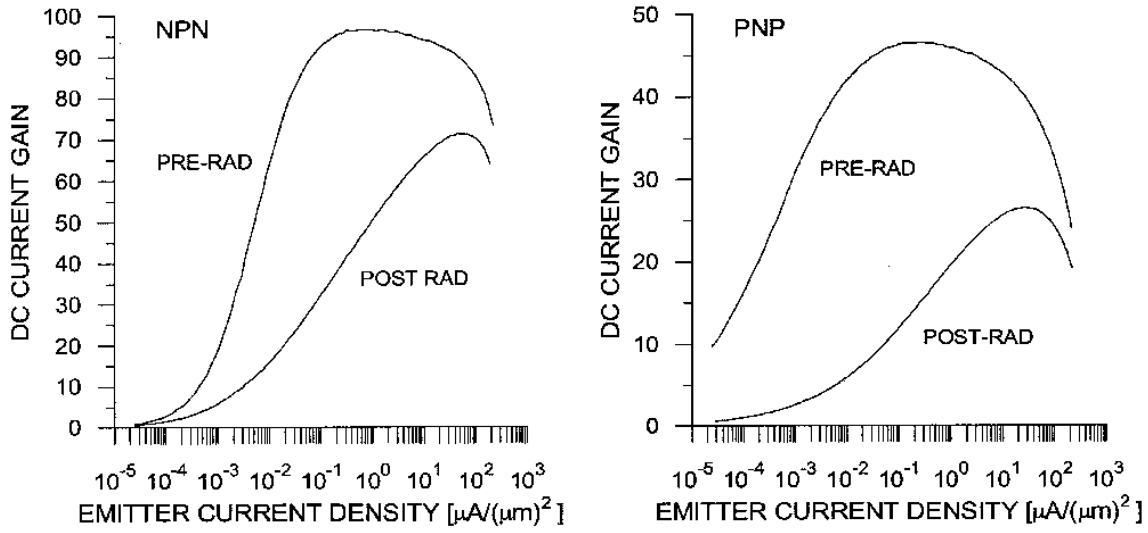


Figure 3.10: DC current gain of a *npn* and *pnp* transistor before and after irradiation with 800 MeV protons to a fluence of $1.2 \times 10^{14}\, cm^{-2}$ [Kip94].

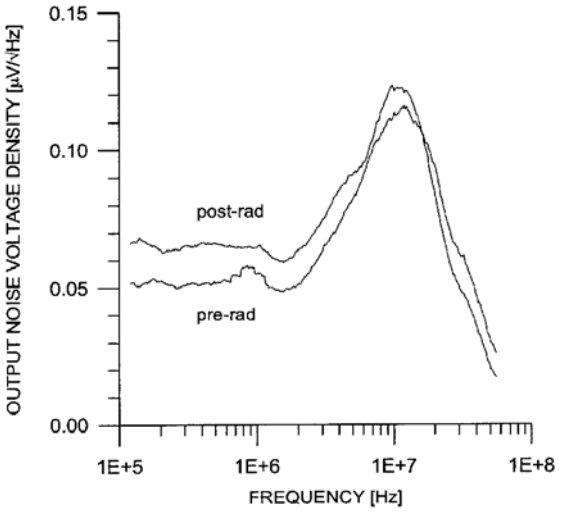


Figure 3.11: Spectral noise density of an integrated preamplifier before and after irradiation with 800 MeV protons to a fluence of $1.2 \times 10^{14}\, cm^{-2}$ [Kip94].

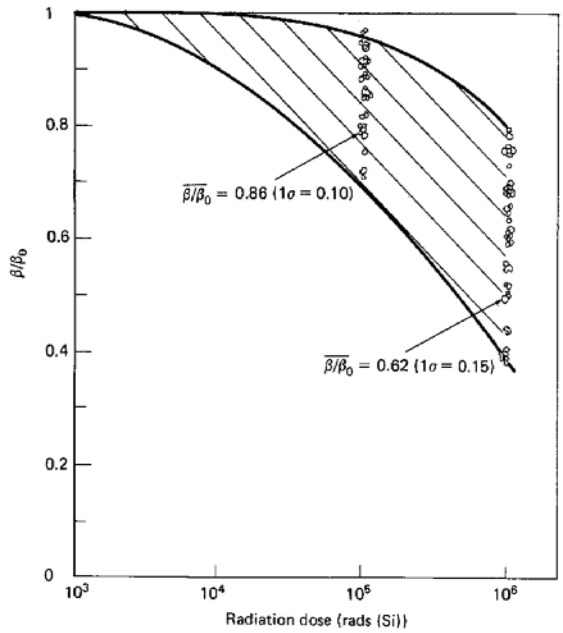


Figure 3.12: Relative degradation of the current-gain β for various devices under irradiation [Mes86].

3.1.4 Single Event Effects

Single Event Effects (SEE) are initiated by the interaction of a *single particle* with a very localised region of the electronic device. They have been studied since the late 1970's with the discovery of memory errors in terrestrial [May78] and space [Bin75] environments. Single Event Effects can be classified into *non-destructive effects*, resulting in so-called soft errors and *destructive effects* producing hard errors. Table 3.3 lists the various categories of SEEs [Wea02, Fac99b, Ker89].

Non-Destructive Effects			
name		sensitive device	description
SEU	Single Event Upset	digital ICs	change of the logic state of a latch or a memory cell
SET	Single Event Transient	combinational logic, op. amps.	temporary deviation of an analogue signal (the analogue equivalent of SEU)
SED	Single Event Disturb	digital ICs	temporary disturb of digital information
Destructive Effects			
name		sensitive device	description
SEB(O)	Single Event Burnout	power transistors (double-diffused (DMOS) FETs and BJTs)	power devices are triggered in the OFF state by a particle induced current transient. A parasitic or the main bipolar structure is turned on and a positive feedback mechanism generates a destructive current by impact-ionisation (avalanches).
SEDF	Single Event Dielectric Failure	CMOS	heavy-ion-induced catastrophic failure of DRAM or SRAM devices. Similar to the SEGR phenomenon.
SEGR	Single Event Gate Rupture	power MOSFETs	A heavy-ion-induced localised dielectric breakdown of the gate oxide occurring in the transistor's OFF state ($V_{gs} < 0$)
SEL	Single Event Latch-up	CMOS, BJT	The triggering of a (parasitic) thyristor[8], typically a combination of active and parasitic devices, by a particle hit. The thyristor usually operates between the power supplies and may sustain destructive high currents.
SES	Single Event Snapback	CMOS	Switching a *pn*-junction to *avalanche mode* sustains a high current. Snapback does not involve a positive feedback (SCR structure); imposes a maximum supply voltage constraint.

Table 3.3: Categories of Single Event Effects.

In CMOS deep-submicron technologies like the one used for the *Beetle* chip (0.25 μm CMOS) only two effects are of importance: *Single Event Upset* and *Single Event Latch-up*. They will

[8] also: Silicon Controlled Rectifier (SCR)

be discussed in detail in the following. SEDF could be an issue in future CMOS technologies if constant-voltage scaling is applied and the electric field across the gate oxide increases. In all experiments with 0.25 μm CMOS devices no SEDF was observed so far [Ane00]. SET and SED are only of secondary concern, since they are transient, non-destructive effects. SES has not been observed in 0.25 μm CMOS technology so far.

Single Event Upset: SEU

An incoming ionising particle creates along it's path electron-hole pairs by Coulomb-scattering with the lattice atoms. In case of an electric field the created charge carriers will be separated and collected on a circuit node. Sensitive nodes are formed by reverse biased *pn*-junctions.

The charge collection dynamics [Mas93, Pet97] have two contributions: a fast ($\mathcal{O}$(100 ps)) and a slow component ($\mathcal{O}$(ns)). The rapid collection process is due to drift in the depletion region of the *pn*-junction. The slow contribution arises from diffusion in the device's bulk. The region where charge collection by drift occurs can be significantly extended by an effect called *"funnelling"* [Mes97]. A particle track penetrating the junction and depletion regions of an active device produces a track of electron-hole pairs. The presence of the created charge carriers distorts temporarily the equipotential surfaces of the depletion layer electric fields in the vicinity of the track. This distortion results in a nesting of funnel-shaped equipotential surfaces that can extend deep into the substrate bulk (figs. 3.13, 3.14). The funnelling of equipotentials produces a large potential gradient resulting in an enhanced charge collection to the SEU-sensitive device node.

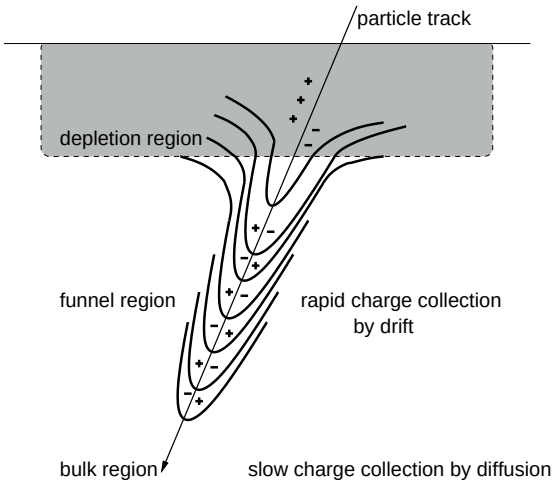


Figure 3.13: *Funnelling*: enhanced charge collection by funnel-shaped equipotentials extending deep into the substrate bulk [Mes86].

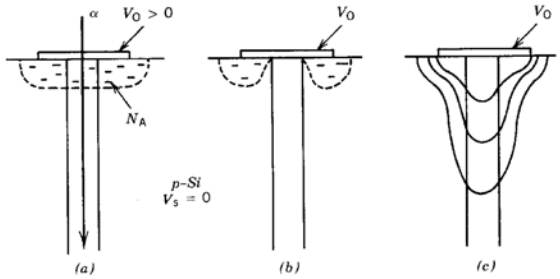


Figure 3.14: Response of a *pn*-junction to the penetration of an ionising particle (a) [Ker89]. The depletion region is neutralised by the plasma column (b). (c) shows the extension of the equipotential lines down the particle track.

The energy deposited by an incident particle is expressed in terms of energy loss per path length dE/dx (also stopping power) in units of keV/μm or *linear energy transfer* (LET =

$dE/\rho dx$) in units of $\mathrm{eV\,cm^2\,mg^{-1}}$ (where ρ is the density of the material). Since in silicon 3.6 eV are needed to create an electron-hole pair, the minimum or critical charge relates to the energy by $Q_{crit} = e \cdot E_{crit}/3.6\,eV$. The critical LET is given by $\mathrm{LET}_{crit} = E_{crit}/\rho_{Si} d$ with d being the sensitive depth, which is $0.5 - 2\,\mu$m [Huh00].

The SEU sensitivity is characterised by experimentally determine the cross-section σ_{SEU}. The experimental data can be represented by a *Weibull* fit:

$$\sigma = \sigma_{sat} \left(1 - \exp \left\{ - \left[\frac{E - E_{crit}}{W} \right]^S \right\} \right) \tag{3.10}$$

where
σ_{sat} is the saturation value of the SEU cross section,
E_{crit} is the SEU threshold energy level,
W, S are fitting parameters.

Figs. 3.15 and 3.16 show measurement results of SEU cross-section for different types of shift-registers and static D-flip-flops [Fac99a]. A Weibull-fit has been applied to the data points. The cross-section curve indicates the sensitive area of a device at a given particle energy. The static shift register without a clock applied showed the lowest sensitivity to SEU. A comparison between a standard flip-flop, an "oversized" one where some transistors have been enlarged to increase the node capacitance and the current driving capability and an "overloaded" flip-flip, which uses additional metal-to-metal capacitances at sensitive nodes on top of the cell, has been performed. The modified cells show a lower sensitivity to SEU, with the "overloaded" flip-flop being the most effective, at the cost of reduced speed and higher power consumption.

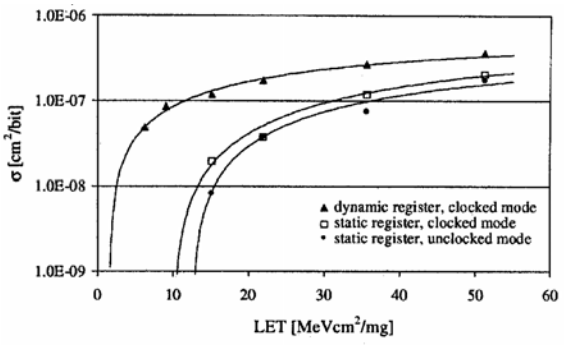


Figure 3.15: Measured SEU cross-section of dynamic and static shift registers under heavy-ion irradiation. The applied clock frequency was 30 MHz [Fac99a].

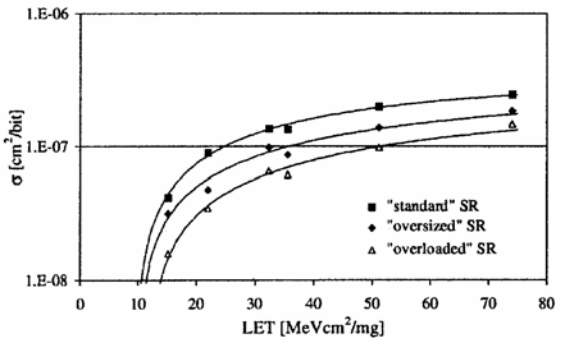


Figure 3.16: Measured SEU cross section for various types of static flip-flops [Fac99a]. The difference is explained in the text.

Taking a critical LET from fig. 3.16 of $\mathrm{LET}_{crit} \approx 10\,MeV cm^2 mg^{-1}$ and assuming a sensitive depth of $0.5 - 2\,\mu m$ [Huh00], the critical charge can be estimated to $Q_{crit} = 50 - 200\,\mathrm{fC} = 320 - 1,300\,\mathrm{ke^-}$.

Potential candidates to create an upset are *heavy ions* which have a large stopping power or *hadrons* as protons, pions and neutrons which have a low dE/dx but may create an SEU by nuclear interactions. The recoil atom of the inelastic interaction triggers the SEU. Table 3.4 gives some figures for LET for various particles [Hal00].

Ion type	Si	Si	Cl	Ni	Br
LET $[MeVcm^2mg^{-1}]$	9	10.4	12.9	30	39.4

Table 3.4: LET values for various ion types at a kinetic energy of $\approx 100\,\mathrm{MeV}$ [Hal00].

Hardening integrated circuits to SEU [Ker89] can be achieved by technological measures and/or device- and circuit design approaches. Basically, an upset can be prevented technologically by either reducing the maximum collectable charge on a node below the critical charge or by raising Q_{crit} to a level which is not reachable in the intended environment. This can be achieved by the use of an epitaxial substrate, i.e. a heavily doped bulk, or a Silicon-On-Insulator (SOI) technology which reduce the depth of the sensitive charge collection volume. In general, device- and circuit-hardening techniques increase cell area and/or decrease cell speed. Hardening approaches include the increase of node capacitances, the decoupling of elements by gate resistors or -diodes or, in case of SRAM[9] cells, the use of resistors or diodes in the drain-drain leg of complementary SRAM cells (fig. 3.17).

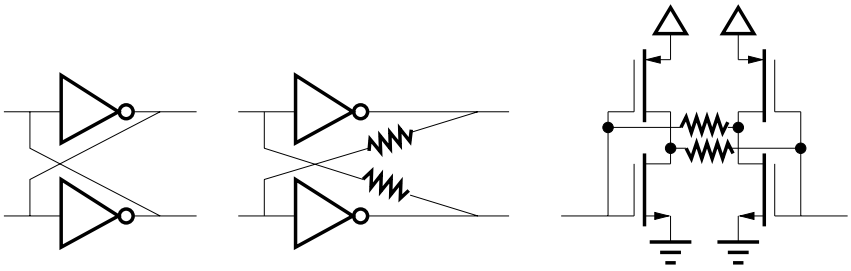


Figure 3.17: Hardening an SRAM cell by increasing the feedback resistance.

Process scaling increases the sensitivity to Single Event Upset. Since both the node capacitance C_n and the node voltage V_n scale with k^{-1} (cf. table 3.1), the critical charge scales with k^{-2}. Q_{crit} can be kept constant by increasing the device area.

Single Event Latch-up: SEL

The device structures that are present in standard CMOS technology inherently comprise a *pnpn* sandwich structure. Together with typical CMOS device pairs (NMOS/PMOS transistors) parasitic bipolar transistors are formed which can make up a silicon-controlled rectifier (thyristor). Fig. 3.18 illustrates the cross section of a CMOS device pair with the accompanying parasitic structures [All87, Gra01]. Beside the NMOS and PMOS transistor a lateral *npn* (*Q2*) and a vertical *pnp* (*Q1*) bipolar transistor are present. In normal operation, all the *pn*-junctions in the structure a reverse biased. If the two BJTs enter the active region for some reason and the configuration satisfies several conditions (see below), the thyristor is switched on and shortens the power supplies which results in a destructive current, unless the supply current is limited. This high current state is called *latch-up*. The thyristor structure provides a *positive feedback* since the collector of the *npn* transistor is connected to the base of the *pnp* transistor and vice versa (fig. 3.18, right). An increase of the base current in *Q2* by Δi, e.g. due

[9] Static Random Access Memory

to the ionisation of a penetrating particle, results in a rise of the collector current by $\beta_{npn}\Delta i$. This current is pulled out of the base of *Q1* (if R_n is ignored). The collector current of *Q1* is $\beta_{npn}\beta_{pnp}\Delta i$ and flows into the base of *Q2* (ignoring R_p). The current direction of the circuit's response is the same as the initial disturbance, which makes the feedback positive.

To generate a *latch-up*, the response of the circuit to the initial disturbance has to grow continously. The following conditions have to be satisfied:

- The loop gain has to be greater than unity. If R_n and R_p are large and the currents through the resistors can be neglected compared to the base currents, the gain in the loop is $\beta_{npn}\beta_{pnp} \stackrel{!}{\geq} 1$.
- One of the *pn*-junctions of the *pnpn* structure must become forward biased.
- The circuit connected to the BJT emitters must be capable of sinking and sourcing a current greater than the holding current I_h (fig. 3.18 c) of the SCR.

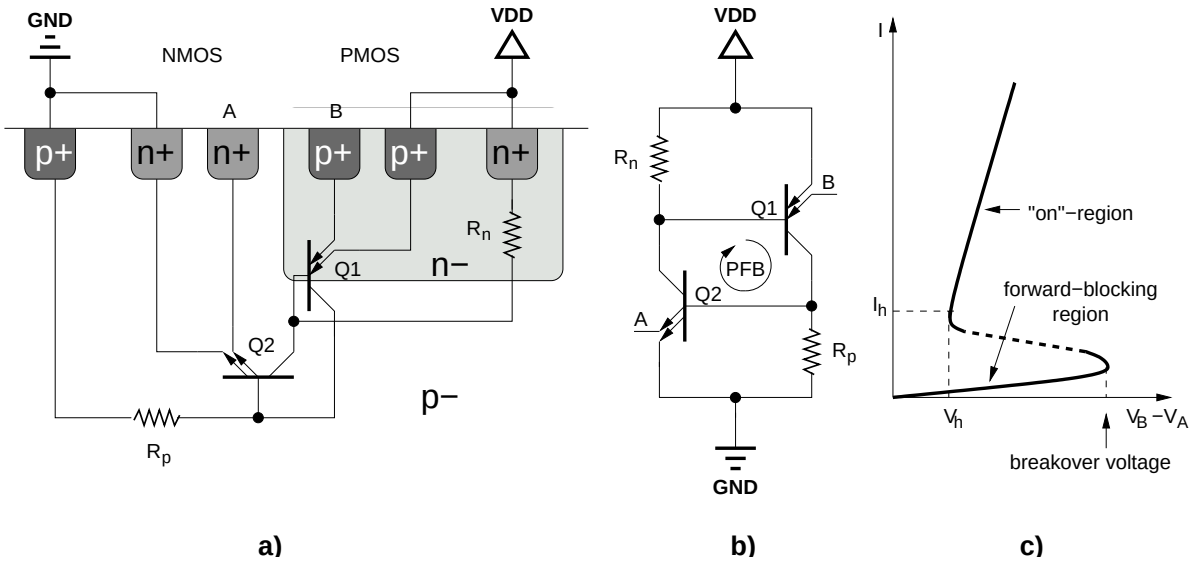


Figure 3.18: Cross section (a) of a typical CMOS device pair with inherently present bipolar transistors. The corresponding thyristor circuit schematic is shown in b). The positive feedback loop is labelled *PFB*. c) depicts the $I - V$ characteristic of the *pnpn* structure.

To prevent latch-up the loop gain of the parasitic *pnpn* structure has to be decreased. This can be achieved technologically and/or by circuit layout. A geometrical separation of the CMOS device pair helps to reduce the β_{npn} value since the base of the lateral BJT increases. Another approach is to reduce the resistances R_n and R_p because more current has to flow through them to produce a sufficiently high voltage drop to forward bias the base-emitter junctions of *Q1* or *Q2*. This can be achieved by adding substrate- or well contacts or surrounding the MOS devices with guard rings (see section 3.2.2). The use of an epitaxial substrate, i.e. a heavily doped bulk, reduces the depth of the sensitive charge collection volume and therefore limits the current amplitude. An SOI technology in combination with trench isolations[10] completely isolates the active devices and avoids parasitic *pnpn*-structures.

[10]STI=shallow trench isolation

An initialised *latch-up* can be interrupted by promptly cutting the power supply to the circuit. This prevents a destruction and the circuit can be returned to the operational condition. A latch-up protection by controlling the supply current is for example implemented in the ALICE silicon strip detector ladder end cap modules [Klu01]. The time needed to switch off the power supply is $25\,\mu s$.

3.2 Radiation Hard VLSI Circuit Design

3.2.1 Choice of Process Technology

The long-term charge trapping responsible for a shift in the threshold voltage is dominated by hole traps in the oxide. Advances in MOS process technology, quite apart from radiation hardening efforts, have served to reduce the density of hole traps, e.g. by cleaner and low-growth-temperature oxides. The inherent sensitivity to irradiation can be drastically reduced by scaling down the device dimensions (figs. 3.19 and 3.20). Below an oxide thickness of $\approx 12\,\text{nm}$ the square-dependence of the threshold-shift ΔV_{th} on the oxide thickness loses validity due to tunnelling of trapped charges out of the oxide (cf. section 3.1.2). Also the number of radiation-induced interface states drops strongly for $t_{ox} < 12\,\text{nm}$.

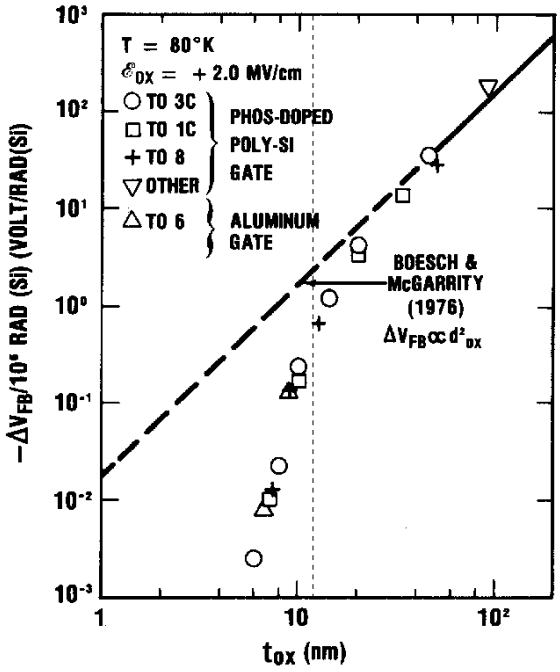


Figure 3.19: Shift of the flatband voltage V_{FB}[12]after an accumulated dose of 1 Mrad as a function of the gate-oxide thickness t_{ox} of various MOS structures [Sak84].

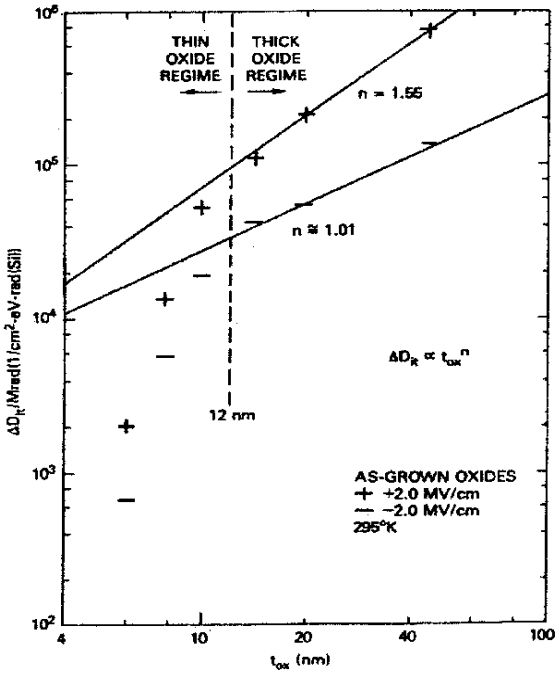


Figure 3.20: Variation of the density of interface traps D_n after an accumulated dose of 1 Mrad as a function of the gate-oxide thickness t_{ox} of various MOS structures [Sak86].

[12]The flatband voltage is the voltage that has to be applied to the gate electrode to create a flat energy band inside the silicon. V_{FB} relates to the threshold voltage V_{th0} with $V_{th0} = V_{th}(V_{bs} = 0) = V_{FB} + 2|\phi_F| + \gamma\sqrt{2|\phi_F|}$, where ϕ_F is the surface potential (Fermi potential) and γ is the bulk threshold parameter.

3.2.2 Layout Techniques

Enclosed Gate Structures

MOS field effect transistors using an *enclosed gate*, also called *edgeless* transistors (ELT), avoid parasitic paths between source and drain, and therefore eliminate any leakage currents. Fig. 3.21 depicts the principle drawing of the geometry.

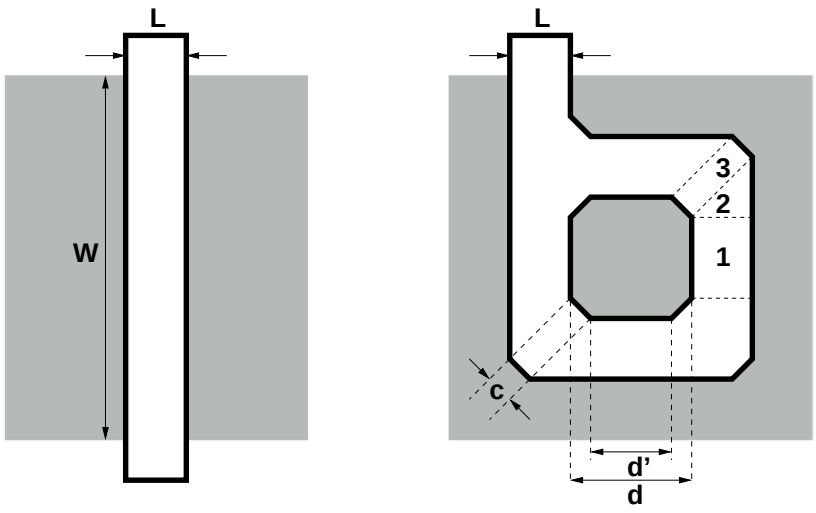


Figure 3.21: Principle drawing of the geometry of a linear (left) and an enclosed (right) transistor.

Looking at the enclosed gate structure of fig. 3.21 the question arises what the width W of the ELT is. A model has been developed [Fac98, RD49, Gir98] which parametrises the width as

$$\left(\frac{W}{L}\right)_{eff} = 4 \cdot \underbrace{\frac{2\alpha}{\ln \frac{d'}{d'-2\alpha L}}}_{1} + 2K \cdot \underbrace{\frac{1-\alpha}{1.13 \cdot \ln \frac{1}{\alpha}}}_{2} + 3 \cdot \underbrace{\frac{\frac{d-d'}{2}}{L}}_{3}, \tag{3.11}$$

where
$\left(\frac{W}{L}\right)_{eff}$ is the *effective* aspect ratio of the enclosed transistor,
L is the (drawn) length of the transistor,
d, d' are the geometrical lengths depicted in fig. 3.21,
α, K are fitting parameters: $\alpha = 0.05$; $K = 3.5$ for $L \leq 0.5\,\mu$m, $K = 4$ for $L > 0.5\,\mu$m.

The three contributions are labelled in fig. 3.21. The first term (1) encounters the linear part between two corners. Term 3 represents the rectangular region of a corner, while term 2 describes the triangular corner segment. The precision of the model is about 94% for short transistors and even better for long devices [Fac98].

Beside the advantage of suppressing leakage currents in NMOS transistors, several disadvantages exist using ELT:

- a special modelling is necessary,
- a minimum aspect ratio exists ($(W/L)_{min} \approx 2.3$ which is reached for L $\geq 7\,\mu$m): transistors with long channels (large L, small W) are not possible,
- increased area consumption,
- larger parasitic capacitances.

A linear transistor is a completely symmetric device which is not the case for an ELT. The two diffusion regions differ in area, and therefore in output conductance and in gate-diffusion overlap capacitance. The outer region acting as source provides a higher output conductance but also a larger overlap capacitance. This asymmetry increases with gate length. These two issues are conflicting and have to be traded off against each other in circuit design. Often MOSFETs have their source connected to the power supply (*Gnd* is case of NMOS transistors and *Vdd* in case of PMOS devices). These transistors usually connect the outer diffusion region as source in order to use the larger parasitic capacitance for blocking the supply line.

Guard Rings

The systematic use of guard rings prevents the creation of thyristor structures (cf. section 3.1.4) and hence the triggering of a Single Event Latch-up (SEL). Guard rings surround the active devices and provide a low-impedance connection to the local substrate, which is (in a p-substrate process with n-wells) the wafer substrate in case of NMOS transistors and the n-well in case of PMOS transistors. That way they reduce the substrate's and well's resistance to the power supplies (R_p and R_n in fig. 3.18) and additionally increase the distance of the diffusion regions (n^+ resp. p^+) to adjacent MOS transistors. Fig. 3.22 demonstrates the layout principle. The disadvantage of using guard rings is the higher area consumption. A logic gate integrating guard rings needs about 60% more area.

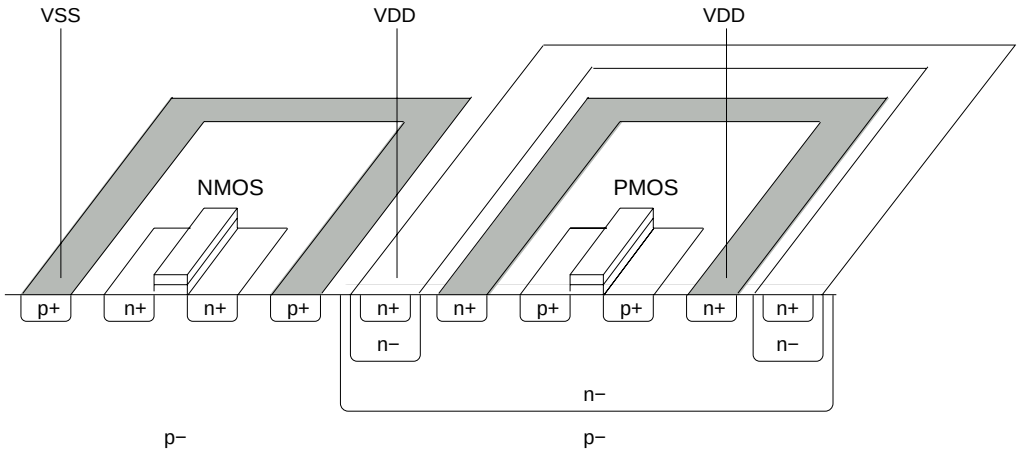


Figure 3.22: Layout principle of guard rings (grey) around MOS transistors.

3.2.3 Analogue Circuit Design

Beside the layout aspects mentioned above, several measures in *circuit design* can be taken to minimise the consequences of radiation effects. The basic goal is to assure a stable operation point of the analogue stages. This is achieved by biasing the amplifiers by currents instead of voltages. Variations in the device parameters, e.g. a shift of the threshold voltage or an increase of leakage currents, are compensated by the use of current mirrors. Fig. 3.23 shows an example schematic of a folded-cascode amplifier with it's bias structure. A shift in threshold voltage is inherently compensated as depicted in fig. 3.24, since the effect is present in both branches of a current mirror.

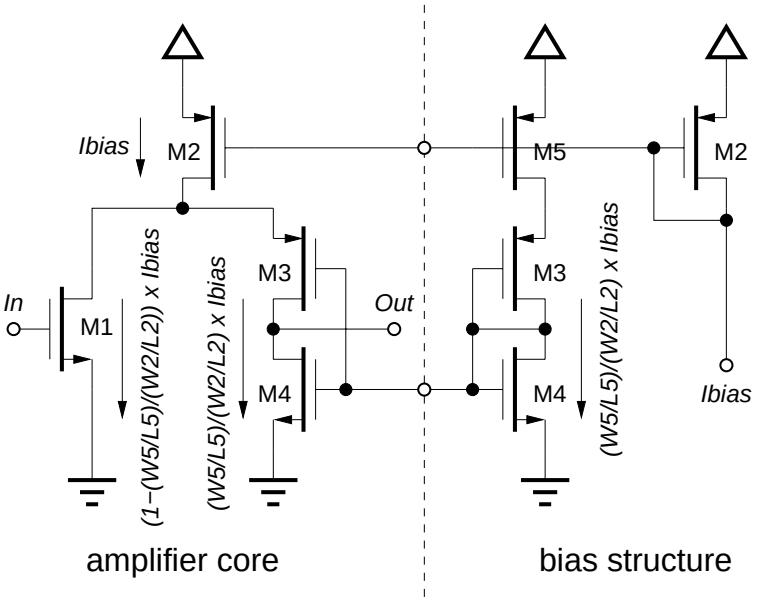


Figure 3.23: Biasing a folded cascode with constant currents.

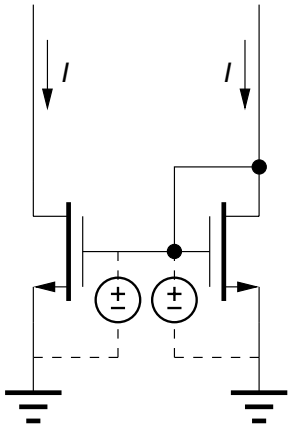


Figure 3.24: Inherent compensation of threshold voltage shifts in a current mirror.

In cases where a voltage control is necessary, e.g. for the feedback transistor (resistor) of a charge-sensitive amplifier (fig. 4.12), the potential is not fixed but tunable. During long term operation an adjustment can be taken to compensate e.g. for radiation induced V_{th}-shifts.

Several analogue stages on the *Beetle* chip, e.g. the current source (section 4.4.6) or the voltage digital-to-analogue converters (section 4.4.6), use (ohmic) resistors made of *polysilicon*. Compared to n-well resistors which feature an about 50% larger sheet resistance, polysilicon resistors are due to their poly-crystalline structure *radiation hard*. At the grain boundaries, a bending of the energy band is present [Wag92] which results in a potential barrier limiting the current flow. Displacement damage of incident particles is responsible for radiation effects in resistors. Radiation induced defects in the lattice reduce the mean free path length of the charge carriers. In poly-crystalline silicon the current flow beyond the grain boundaries is determined by the bending of the energy bands and unaffected by lattice defects.

3.2.4 Redundancy

The basic idea of the redundancy approach for a circuit robustness against SEU is the representation of a digital bit not only be a single device, e.g. a flip-flop or an SRAM cell, but at least by three devices. The state of the represented bit is defined by the majority of the states of the corresponding devices. For a majority voting of three flip-flop outputs Q_i (i = 1,2,3) the bit value is defined by $Q_1 \cdot Q_2 + Q_1 \cdot Q_3 + Q_2 \cdot Q_3$[13] (see section 4.6 for details).

For finite state machines, one mechanism to at least detect corrupted data in a state register is the so-called *one-hot state encoding*. Hereby, a state is encoded by only *one* set bit. For n states, n instead of $[\log_2(n)]$ bits are needed. A number of set bits depart from 1 can be detected and an adequate action, e.g. a reset, be taken.

3.2.5 Error Detection and Correction Codes

Error Detection and Correction (EDC) codes are a widely spread technique in RAM memories and signal transmission systems. An error in a digital system is the corruption of data from its correct value to some other value, caused by a physical failure. The effect of failures on data are predicted by *error models*, the simplest one being the *independent error model*. In this model a single physical failure is assumed to result in a single error, i.e. affecting a single bit of data. Checking codes can be divided in *error-detecting* and *error-correcting* codes. The latter ones are able to localise the bit error and correct it.

A code using n-bit strings has 2^n possible words. In order to *detect* an error, the 2^n words are divided in valid and non-valid code words (non-code words). A system using error-detection only operates with (valid) code words. The detection of a non-code word indicates an error.

N-Cubes and *Hamming* Distance

An n-bit code can be represented as an n-cube [Wak94]. Each code word takes one of 2^n vertices labelled with the n-bit code strings. Each vertex is adjacent to n other vertices whose labels differ from the actual vertex in only one bit. n-cubes help visualising certain coding and logic minimisation problems. For example, the problem to design an n-bit *Gray-code*[14] is equivalent to finding a path along the edges of the n-cube that visits each vertex exactly once (fig. 3.25 a). The *distance* (also called *Hamming distance*) between two n-bit strings is the number of bit positions in which they differ. In terms of an n-cube, the distance is the minimum length between the two corresponding vertices. This concept is crucial in the design and understanding of EDC codes.

A code is simply a subset of the vertices of the n-cube. In order to detect all single errors, no code word can be immediately adjacent to another code word vertex. In terms of the concept of distance this can be stated, that the minimum distance between all possible pairs of code words has to be 2. Fig. 3.25 b) and c) demonstrate a minimum-distance-1 and minimum-distance-2 3-bit code.

Parity Bit

In general, *n+1* bits are needed to construct a single-error-detecting code with 2^n code words. To obtain a minimum-distance-2 code, one more bit, called *parity bit*, is added to the *n infor-*

[13] The dot $\cdot$ represents an AND connection, the plus + a logic OR.

[14] A *Gray-code* is a code where only one bit is allowed to change from one code word to the next.

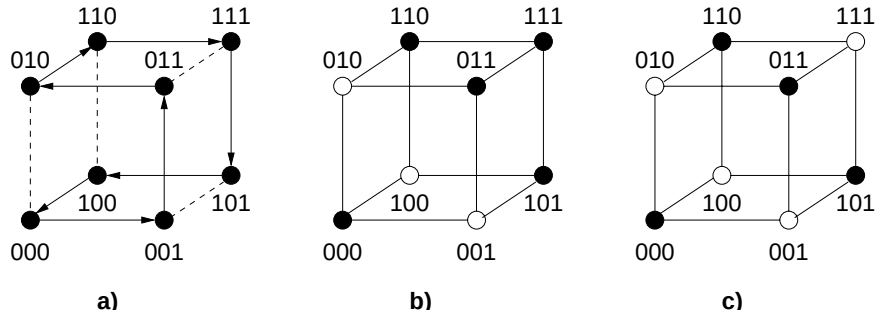


Figure 3.25: 3-bit code representation in a cube [Wak94]. a) Traversing the 3-cube in *Gray-code* order b) 3-bit code with a minimum distance of 1: not all single errors are detected. c) 3-bit code with a minimum distance of 2: detects all single errors. Code words are represented by •, non-code words by ∘.

mation bits. The parity bit is chosen that way, that the total number of 1s in the *(n+1)*-bit code is even (even-parity code) or odd (odd-parity code). The parity bit is the modulo-2 total of the digits (or modulo-2 addition). The circuit implementation uses exclusive-OR gates. These codes are also called 1-bit parity codes. In the example of fig. 3.25 c) one bit of the 3-bit code words can be interpreted as the (even) parity of the corresponding 2-bit string.

1-bit parity codes can detect single or any *odd* number of errors. 2-bit errors are not detectable. Other codes, with minimum distances greater than 2, are able to detect multiple errors and/or to locate the error bit position.

Error-Correction

By using more than one parity bit, codes can be constructed that are able to *correct* single errors and detect multiple errors. A code with a minimum distance of $2k + l + 1$ can be used to correct errors that affect up to k bits and to detect errors in up to l additional bits [Wak94, Roh95]. For example, in a minimum-distance-3 code ($k = 1$, $l = 0$) there are, in terms of the n-cube, at least 2 non-code words between each pair of code words. The non-code word produced by a 1-bit error will be closer to the originally code word than to any other one. The correction procedure will be a change of the non-code word to the nearest code word.

Hamming Code

In 1950, *R. W. Hamming* described a general method for constructing codes with a minimum distance of 3 [Wak94, Roh95, Tie93], called *Hamming code*. The number of parity bits i that is required to correct single errors in j data bits is determined by

$$2^i \geq i + j + 1. \tag{3.12}$$

With i parity bits (in the following also called check bits) 2^i bit numbers can be specified. The total code length is *i+j*. One more bit is needed to account for the bit numbering scheme for encoding which is presented below. For example, for 8-bit and 10-bit data words 4 parity bits are needed, a 16-bit data word requires 5 parity bits. The relative portion of the parity bits in the total code length is the smaller the larger the data word length is. For example, for $121 - 247$ data bits only 8 parity bits are required.

A minimum distance-k code requires $(k-1)$ times more non-code words than code words. Hence, the introduction of $(k-1)$ parity bits is sufficient for a code implementation. For a minimum distance-3 *Hamming* code eq. 3.12 claims more than 2 check bits. These additional parity bits allow a simple decoding procedure as will be shown below.

Every data bit contributes to at least two parity bits. An error in a data bit results in a change of the associated parity bits which allows to infer to the affected bit position. An error in a parity bit will show up as the change of a single parity bit. The *encoding*, i.e. the assignment of the data bits to the parity bits, is described by a check-bit matrix, called *Hamming* matrix $\mathcal{H}$. In the following the encoding- and decoding procedure will be detailed for 8-bit wide data words (which corresponds to the register width on the *Beetle)*. The check-bit matrix $\mathcal{H}$ is written as[15]

$$P = \begin{bmatrix} p_3 \\ p_2 \\ p_1 \\ p_0 \end{bmatrix} = \mathcal{H} \otimes D = \begin{bmatrix} 1 & 1 & 1 & 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 1 & 1 & 1 & 0 \\ 0 & 1 & 1 & 0 & 1 & 1 & 0 & 1 \\ 0 & 1 & 0 & 1 & 1 & 0 & 1 & 1 \end{bmatrix} \otimes \begin{bmatrix} d_7 \\ \vdots \\ d_0 \end{bmatrix}. \tag{3.13}$$

This representation of the *Hamming* matrix can be obtained by numbering the $i+j$ (12) bit positions of the code word C from 1 to $i+j$ (12). Starting the numbering from 1 instead of 0 requires the additional bit in eq. 3.12. This turns to account in a simplified decoding. Any position which is a power of two is a parity bit, the remaining positions are data bits ($C = [d_7, d_6, d_5, d_4, p_3, d_3, d_2, d_1, p_2, d_0, p_1, p_0]$). The construction rule for the *Hamming* matrix $\mathcal{H}$ reads, that a data bit is assigned to a parity bit, if the position number (in binary representation) has a 1 in the same bit as the parity bit. For example, bit d_6 (position index $11 = 1011_2$) is assigned to the parity bits p_3, p_1 and p_0. Out of the $2^{i+j} = 2^{12} = 4096$ possible words, only $2^i = 2^8 = 256$ are (valid) code words.

For *decoding*, i.e. identifying the error bit position, the so-called error word or *syndrome* S is generated. It is the bitwise parity of the original check bit word P and the actual parity word P'.

$$S = S[3:0] = [s_3, s_2, s_1, s_0] = P \oplus P' \tag{3.14}$$

If no error occurs, $S = 0$. Table 3.5 lists the possible syndromes. The described construction scheme of the *Hamming* matrix $\mathcal{H}$ has the advantage, that the syndrome directly encodes the error bit position. The decoding of the bit position number is done by building the products of the syndrome bits. The *flip* word[16] F indicates the flipped data bit by a 1. The *correction* can be easily done by applying the exclusive-OR of the actual data and the flip word ($D \oplus F$).

$$\begin{aligned} F = F[7:0] = [\ & \overline{s_0} \cdot \overline{s_1} \cdot s_2 \cdot s_3,\ s_0 \cdot s_1 \cdot \overline{s_2} \cdot s_3,\ s_0 \cdot \overline{s_1} \cdot s_2 \cdot \overline{s_3},\ s_0 \cdot \overline{s_1} \cdot \overline{s_2} \cdot s_3, \\ & s_0 \cdot s_1 \cdot s_2 \cdot \overline{s_3},\ \overline{s_0} \cdot s_1 \cdot s_2 \cdot \overline{s_3},\ s_0 \cdot \overline{s_1} \cdot s_2 \cdot \overline{s_3},\ s_0 \cdot s_1 \cdot \overline{s_2} \cdot \overline{s_3}\ ] \end{aligned} \tag{3.15}$$

The minimum distance of the presented code is three, since at least a 3-bit change has to be made to a code word to obtain another code word. Single or double bit errors will result in non-code words. A minimum distance-3 Hamming code only *corrects* reliably for single bit errors. A double bit error will be detected as an error condition but is not distinguishable from a single error and the resulting syndrome may indicate a wrong error bit as should be demonstrated in the following example. A transition from the data word `10110110` to `11010110`

[15] $\otimes$ represents a standard matrix multiplication with the addition replaced by an exclusive-OR.

[16] The dot $\cdot$ represents an AND connection, the over line a logic negation (NOT).

syndrome S				description
s_3	s_2	s_1	s_0	
0	0	0	0	no error
0	0	0	1	parity bit error (p_0)
0	0	1	0	parity bit error (p_1)
0	1	0	0	parity bit error (p_2)
1	0	0	0	parity bit error (p_3)
0	0	1	1	(single) data bit error (d_0)
0	1	0	1	(single) data bit error (d_1)
0	1	1	0	(single) data bit error (d_2)
0	1	1	1	(single) data bit error (d_3)
1	0	0	1	(single) data bit error (d_4)
1	0	1	0	(single) data bit error (d_5)
1	0	1	1	(single) data bit error (d_6)
1	1	0	0	(single) data bit error (d_7)
1	1	0	1	multiple data bit error
1	1	1	0	multiple data bit error
1	1	1	1	multiple data bit error

Table 3.5: Possible *Hamming* code syndromes.

which is an error in the bit positions 6 and 5 will give the syndrome `0001`. This will be falsely interpreted as a single bit error of the parity bit p_0 (table 3.5). The definite detection of double bit errors can be achieved by extending the minimum distance-3 Hamming code to minimum distance-4. This is done by adding one more parity bit so that the parity of all code word bits is even. A single bit error is characterised by a syndrome $S \neq 0$ and an odd parity, a double bit error by $S \neq 0$ and an even parity. Similar to the minimum distance-3 code, a 3-bit error is not distinguishable from a single error. In general, the correction of errors using Hamming codes is limited to single bit errors.

The block schematic of a possible circuit implementation of the described *Hamming* code scheme on the *Beetle* is depicted in fig. 3.26. The *Encoder* generates the 4 check bits of each data byte and stores them in flip-flops at the time of the register programming via the I^2C-interface. In case of a bit error, which is indicated by the change of the corresponding register's parity, a trigger is generated (*EC Trigger Generator*) and the register address is encoded (*Priority Encoder*) with the priority of lower register addresses. The module *Syndrome Generator* reads the affected data byte via the internal parallel bus and generates the syndrome using the previously stored parity bits. This is decoded by the module *Syndrome Decoder*. The data correction and the write operation to the register is performed by *Corrector*.

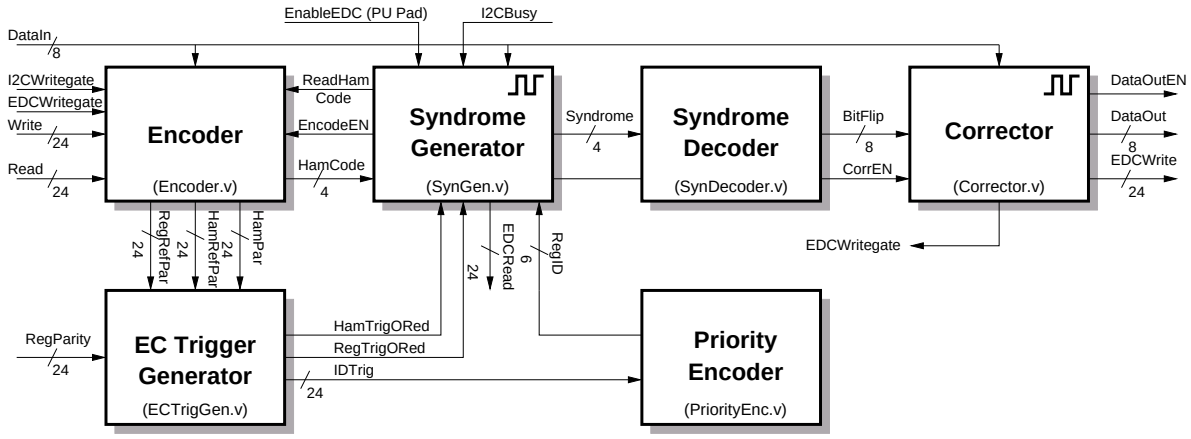


Figure 3.26: Block diagram of a control logic implementing the *Hamming* code. The widths correspond to the parameters on *Beetle1.2*, i.e. number of register = 24, data width = 8. The blocks showing a clock symbol are sequential circuits (finite state machines), the others use combinational logic.

Chapter 4

The Beetle Readout Chip

> **beetle**[1] `/'bi:tl/` *n* any of several types of insect, often large and black, with hard wing-cases.
> **beetle**[2] `/'bi:tl/` *n* tool like a hammer, with a heavy head for beating, crushing, etc.
> *(Oxford Advanced Learner's Dictionary)*

This chapter details after an introduction to silicon detectors and their readout electronics the architecture of the *Beetle* readout chip. The circuitry of the major subcomponents are described. It will be referred to *Beetle1.2* unless otherwise noted.
In the context of this work, both analogue and digital circuits have been developed: the pipeline with the corresponding pipeline readout amplifier, the programming interface and several building blocks of the logic controlling event storage and readout. For the digital parts of the circuit a scheme has been developed and implemented which ensures a robustness against Single Event Upset.

4.1 Silicon Strip Detectors and their Readout

A semiconductor detector is a solid state ionisation chamber which can be used for energy, position or radiation-level measurement. In particular silicon detectors play an increasingly important role in particle detectors as position measurement devices. They provide the necessary high spatial resolution to separate secondary vertices of heavy particles containing c- or b-quarks. At LHC and future colliders the detectors have to operate in very hostile radiation environments, which puts additional demands on their design concerning radiation damage.

Semiconductor materials have unique properties which are not accessible with other radiation detectors:

- A small excitation energy of a few eV results in a large number of charge carriers per unit energy loss. In silicon, the average energy for creating an electron-hole pair is 3.6 eV which is an order of magnitude smaller than the ionisation energy of gases ($\sim 30\,\mathrm{eV}$)[1].
- The high density ($\rho_{Si} = 2.33\,\mathrm{g/cm^3}$) leads to a large energy loss per traversed length of the ionising particle. A minimum ionising particle (MIP) loses on average 3.8 MeV/cm in

[1] Only the excitation of phonons or the breakup of Cooper pairs needs less energy ($\sim meV$).

silicon. This enables the possibility to built thin detectors that still produce large enough signals.

- Due to the high mobility of electrons and holes ($\mu_n^{Si} = 1450\,cm^2/Vs$, $\mu_p^{Si} = 450\,cm^2/Vs$), the charge collection time is small (~ 10 ns). This allows the use in high-rate environments.

Charge carrier generation

The basic process of generating mobile charge carriers in particle detectors is by charged particles traversing the detector material. Through inelastic scattering with electrons the incident charged particles lose part of their energy. The mean ionisation energy loss per path length (also called stopping power) is given by the Bethe-Bloch formula [Bet30, Blo33]. It is written here including corrections for density and shell effects [Leo94].

$$\frac{dE}{dx} = 2\pi N_0 r_e^2 m_e c^2 \rho \frac{Z}{A}\frac{z^2}{\beta^2}\left[\ln\left(\frac{2m_e\gamma^2c^2\beta^2W_{max}}{I^2}\right) - 2\beta^2 - \delta - 2\frac{C}{Z}\right] \tag{4.1}$$

where
$2\pi N_0 r_e^2 m_e c^2 = 0.1535$ MeVc^2/g;
x is the path length in cm;
$r_e = \frac{q^2}{4\pi m_e c^2} = 2.817 \times 10^{-13}$cm is the classical electron radius;
$m_e = 511$ keV/c^2 is the electron mass;
$N_0 = 6.022 \times 10^{23}$mol^{-1} is Avogadro's number;
I is the effective ionisation potential averaged over all electrons: $I_{Si} = 173$ eV;
Z is the atomic number of the medium: $Z_{Si} = 14$;
A is the atomic weight of the medium: $A_{Si} = 28.1$;
ρ is the density of medium: $\rho_{Si} = 2.33$ g/cm^3;
z is the charge of a traversing particle;
$\beta = \frac{v}{c}$ is the velocity of the traversing particle in units of speed of light;
$\gamma = \frac{1}{\sqrt{1-\beta^2}}$;
δ is a density correction;
C is a shell correction;
$W_{max} = \frac{2m_e c^2\beta^2\gamma^2}{1+2s\gamma+s^2} \approx 2m_e c^2\beta^2\gamma^2$ for$M \gg m_e$ is the maximum energy transfer in a single collision, with $s = \frac{m_e}{M}$ and M the mass of the incident particle.

At low particle energies the energy loss is proportional to $1/\beta^2$, at high energies it rises with $\ln(\beta^2)$. A particle depositing a minimum of energy per path length is called a *minimum ionising particle* (MIP).

The Bethe-Bloch formula only gives the *average* energy loss per path length (fig. 4.1). Statistical fluctuations lead to an energy loss distribution (fig. 4.2), first derived by Landau [Lan44, Bak87].

In silicon, the average energy ϵ for creating an electron-hole pair is 3.62 eV at T = 300 K. This is 3 times larger than the band gap energy of silicon ($E_g = 1.12$ eV): To promote an electron from the valence band to the conduction band using an energy equal to the minimum band gap spacing requires a momentum transfer from the lattice, since silicon is an indirect semiconductor, i.e. the valence band maximum is not at the same position in momentum space

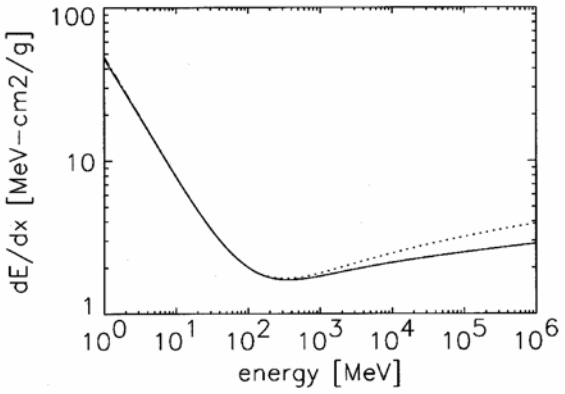


Figure 4.1: Energy loss per path length of a charged pion in silicon as a function of kinetic energy with (continuous line) and without (dashed line) shell and density corrections applied [Lut99].

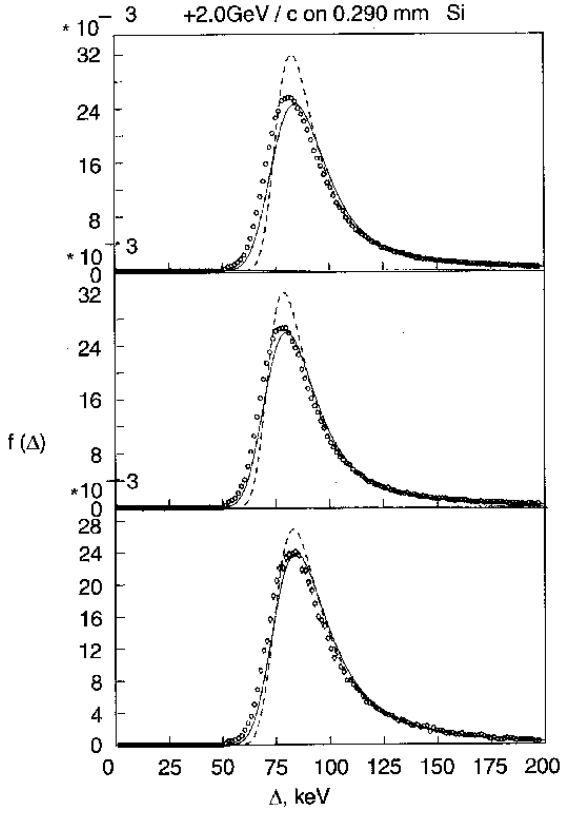


Figure 4.2: Experimental energy loss distributions for 2 GeV/c positrons (top), pions (middle) and protons (bottom) in silicon. Theoretical expectations from *Landau* (dashed) and *Bak* (solid line) are given for comparison [Lut99].

than the conduction band minimum. For a given radiation energy, the number of electron-hole pairs will fluctuate around a mean value N given by

$$N = \frac{E}{\epsilon} \tag{4.2}$$

with E the absorbed energy in the detector. The variance in the number of charge carrier pairs N can be parametrised by

$$\langle \Delta N^2 \rangle = F \cdot N \tag{4.3}$$

with F the Fano factor [Fan47, Sho52]. For $F = 1$ the variance is formal similar with Poisson's statistics which is coincidental. The reason for this fluctuation is the variation in the fraction of deposited energy which ends up in electron-hole generation and phonon excitation. For silicon $F = 0.115$ [Leo94]. If all radiation energy were converted in charge pairs, their number will be fixed and F would be zero. A Fano factor significantly below unity indicates, that the charge creation dominates over the conversion in thermal energy (phonon excitation). A minimum ionising particle (e.g. $1 - 2$ MeV electrons, $200 - 300$ MeV charged pions) loses in silicon $\approx 295\,\mathrm{eV}/\mu\mathrm{m}$, which results in the creation of about 83 electron-hole pairs per μm.

Charge Collection

In order to collect the generated charge carriers one has to separate them in an electric field to avoid recombination to photons or phonons. The signal detected at the electrodes is formed *not* at the time when the electrons and holes reach the electrodes but already during their separation in the electric field by charge influence. A semiconductor detector basically operates as a reverse-biased diode. By joining together oppositely doped semiconductor materials, a *pn*-junction is created which shows diode characteristics. At the junction of *p*- and *n*-material a region free of mobile charge carriers builds up, the *depletion region*, which constitutes the sensitive volume of the detector: the majority charge carriers in each material diffuse into the opposite doped bulk. Electrons will diffuse from the n into the p region and holes vice versa. A negative charge will build up in the p region and a positive in the n region which creates an electric field counteracting the diffusion. This process continues until diffusion and drift currents are equal. Due to the electric field, the transition region of n and p material is free of mobile charge carriers. The remaining doping atoms contribute with their nuclear charge to the *space-charge* or *depletion* region. Applying an external voltage to the *pn*-junction results in a variation of the width d of the depletion layer (eq. 4.4).

$$d = \sqrt{\frac{2\epsilon\epsilon_0}{q} \cdot \frac{n_A + n_D}{n_A n_D} \cdot (V_{bi} - V_B)} \propto \sqrt{V_B} \tag{4.4}$$

where
d is the depletion depth;
n_A is the doping concentration of acceptors;
n_D is the doping concentration of donors;
$\epsilon_0 = 8.854 \cdot 10^{-12}$ F/m is the permittivity of free space;
ϵ is the permittivity of the medium: $\epsilon_{Si} = 1.04 \cdot 10^{-10}$ F/m;
q is the elementary charge;
$V_{bi} = \frac{k_B T}{q} \ln \frac{n_A n_D}{n_i^2}$ is the built-in voltage or diffusion voltage of the *pn*-junction: ~ 0.5 V;
V_B is the external bias voltage;
n_i is the intrinsic charge carrier concentration: $n_i^{Si} \sim 10^{10}\ cm^{-3}$ at T = 300 K.

Putting the *p*-side on a negative potential relative to the *n*-side biases the diode in reverse direction. This increases the width of the depletion region and therefore the sensitive detector volume. Simultaneously the detector capacitance (eq. 4.5) decreases.

$$C_{sb} = \epsilon_0 \epsilon \frac{A}{d} = A \cdot \sqrt{\frac{n_A n_D}{n_A + n_D} \cdot \frac{q\epsilon_0\epsilon}{2(V_{bi} - V_B)}} \propto \frac{1}{\sqrt{V_B}} \tag{4.5}$$

with
C_{sb} the strip-to-backplane capacitance;
A the area of the depletion layer.

A full depletion (fig. 4.3), i.e. the depletion width d equals the detector width, of the detector volume is very desirable, since

- the charge collection efficiency (CCE), i.e. the signal, is $\propto d$,
- the noise is $\propto C_{sb} \propto 1/d$,
- the resolution is decreased by charge spread in a partly depleted detector volume.

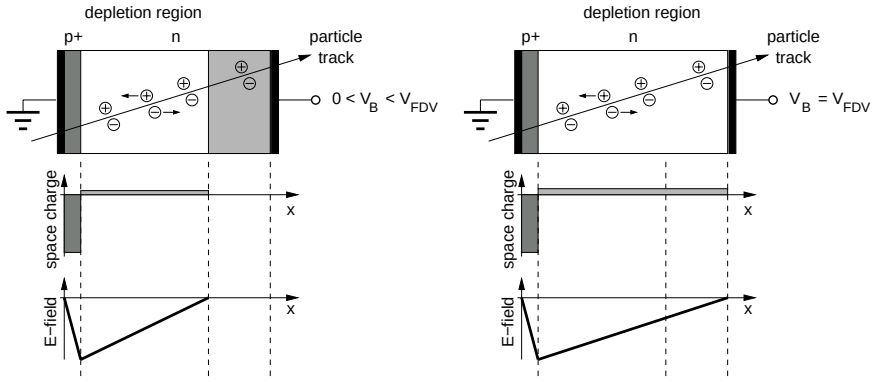


Figure 4.3: Partly and full depletion of a *pn*-junction.

Spatial Resolution

To achieve a high spatial resolution a large-area diode is segmented into strips or pixels which are read out separately. Pixels provide in comparison with strips a "true" two dimensional readout and help to avoid ambiguities ('ghost hits') at high track multiplicities. Pixel detectors with typical pixels sizes of $50 \times 300\,\mu m^2$ up to $1 \times 1\,mm^2$ provide a finer granularity compared to strip detectors. They are used in environments with a high demand on pattern recognition or large track densities. The pixels are, in contrast to strips, DC-coupled and bump-bonded to the read out electronics. An aluminium sphere with a diameter of $\sim 20\,\mu$m establishes the electrical contact. An AC coupling between a pixel or strip and the readout electrode is usually done by separating both with an isolation layer out of SiO_2 and Si_3N_4. In order to avoid charge transfer through fringing capacitances to neighbouring pixels or strips, the coupling capacitance has to be large compared to the pixel-to-pixel (strip-to-strip) capacitance. For pixels this would require a comparable thin isolation layer, which is hard to achieve.

In strip detectors, the pitch of the strips usually matches the diffusion width of the charge carriers, which is proportional to $\sqrt{\text{mobility} \times \text{drift time}}$, assuming a Gaussian distribution with an RMS value of the projected distribution given by $\sigma = \sqrt{2Dt_{drift}} = \sqrt{2\frac{k_B T}{q}\mu t_{drift}}$ (with D the diffusion constant and μ the mobility of the charge carriers). For a $300\,\mu$m thick silicon detector this is about $10\,\mu$m. For *vertexing* the pitch can be as small as $25\,\mu$m. Reading out each individual strip in this high density condition is difficult. This problem is avoided by connecting only every k^{th} strip to the electronics. Typical applications use $k = 2$, which yields in a readout pitch of $50\,\mu$m. The charge collected on the non-connected, interpolating strips is divided capacitively between the neighbouring readout channels according to their relative position. The DC potential of the interpolating strips has to be kept at the same level as the readout strips. Otherwise the interpolating strips would adjust their potential to a value, that they do not collect any charge. The biasing can be achieved by a high ohmic connection to the readout strips. Also resistive charge division is possible, but the resistors contribute to the noise and therefore degrade the position resolution. Fig. 4.4 shows a cross section of a single- and double-sided strip detector. In the case of strips on both sides of the detector (and an *n*-type substrate) the *n*-strips have to be isolated against each other to avoid shorts due to electron-accumulation below the insulating oxide[2]. The electron layer is caused by trapped

[2]Note, that the strips are only isolated for a fully depleted detector volume.

positive charges in the oxide (cf. section 3.1.2). The strip insulation can be achieved by p-type structures, either as homogeneous surface doping (*p-spray*) or as strips in between the $n+$-implants (*p-stop*). Both types are drawn in fig. 4.4, whereas only one is used in a dedicated detector. Another method is the use of MOS structures in between the $n+$-strips, which are negatively biased and therefore disrupt the electron layer [Lut99].

For biasing the diffusion regions, three choices exist: the implementation of *poly-silicon resistors* (as depicted in fig. 4.4) which are radiation hard but at the cost of area, the use of *punch-through*, which suffers from radiation damage and is difficult to operate or the integration of *implanted resistors*, which are radiation hard but only usable on the p-side (in an n-bulk) [Lut99, Abt01].

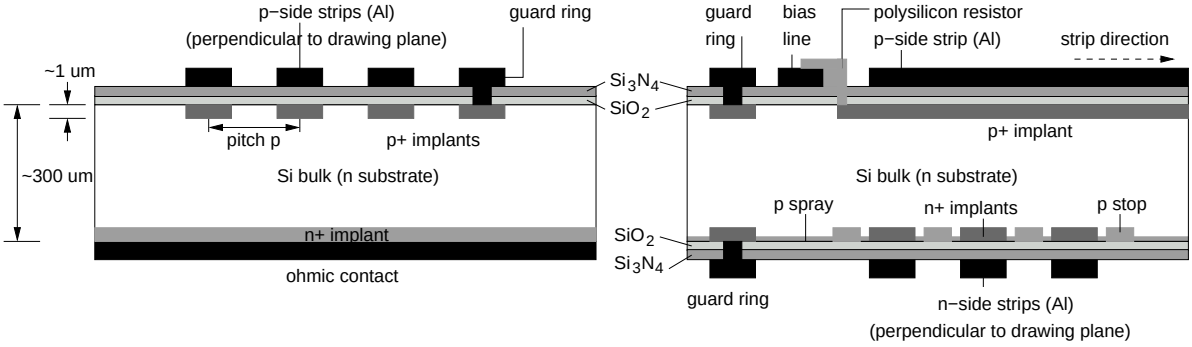


Figure 4.4: Cross section (not to scale) of an AC-coupled single-sided (left) and double-sided (right) silicon strip detector. The AC-coupling is usually established by two isolation layers (SiO_2, Si_3N_4) to reduce the risk of shorts due to defects. In case of the double-sided detector the strips on the two detector faces are crossed. Both, *p-stop* and *p-spray* layers, are drawn whereas only one of them is used in a dedicated detector.

The precision of the position measurement mainly depends on the strip spacing and the signal readout. Using *binary*[3] readout, i.e. it is only distinguished if a strip is hit or not, the resolution is given for a strip pitch p by

$$\langle \Delta x^2 \rangle = \frac{1}{p} \int_{-p/2}^{+p/2} x^2 dx = \frac{p^2}{12}. \tag{4.6}$$

Typical strip pitches are $20 - 200$ μm, which results in resolutions of $\approx 6 - 60$ μm.

The spatial resolution can be improved using *analogue* readout, i.e. evaluating the signal height. The strip pitch has to be chosen sufficiently small, that the signal charge is, due to diffusion, collected on more than one strip. The coordinate is determined by interpolation, e.g. calculating the centre of gravity of the charge cloud. Here, the precision Δx is limited by the signal-to-noise (S/N) performance of the readout electronics

$$\Delta x \approx \frac{p}{S/N}. \tag{4.7}$$

[3]Binary is used in this work in definition to digital as a *1 bit* digital information.

Detector Noise Sources

The two main contributing noise sources in silicon detectors are *leakage currents* and detector *capacitances*. The detector's dark current is of concern in directly coupled electronics. With DC coupling, the input amplifier has to sink the detector's dark current, which can lead to pedestal shifts, a reduction of the dynamic range or even a saturation of the input stage. AC coupling avoids these drawbacks. Only the AC part of the signal current is used, while the DC-component is coupled to the bias network of the detector.

In highly segmented strip or pixel detectors, the strip-to-strip capacitance C_{ss} is dominating over the strip-to-backplane capacitance C_{sb} (eq. 4.5). For strip pitches of $25 - 100\,\mu$m, C_{ss} is typically $1 - 2\,$pF/cm in silicon [Spi01]. The strip-to-backplane capacitance C_{sb} is about 20% of C_{ss}. A direct coupled input amplifier has to provide a low input impedance to reduce the transfer of charge through fringing capacitances to neighbouring strips. In case of AC coupling between the detector and the electronics, the coupling capacitance has to be large compared to C_{ss}.

Radiation Damage in Silicon Sensors

Silicon detectors can be characterised as reverse-biased *pn*-junctions. Defect states, which are created in the silicon bulk due to displacement damage, create *mid-bandgap states* (cf. section 3.1.3) and enable charge carrier transfer to the conduction band and therefore increase the dark current of the diode [Lut99]. Defect complexes additionally act as *trapping centres* which result in a signal decrease. A *change in the doping concentration* affects the width of the depletion region (eq. 4.4) or increases the full deleption voltage.

The increased detector leakage current has several consequences:

- increased power consumption,
- increased shot noise,
- increased DC signal current.

For long integration times the increased DC signal current can drive the subsequent amplifier into saturation. The detector leakage current is strongly temperature dependent ($I_R(T) \propto T^2 e^{-E/2k_BT}$, E being the electron-hole creation energy). Hence, cooling is the simplest technique to reduce leakage currents. Cooling from room temperature to 0° C reduces the diode's dark current by a factor of 6. The most powerful approach against leakage currents is the segmentation of the detector.

Signal Acquisition

The detector signal is a short current pulse with a typical duration of $0.1 - 30\,$ns for $10 - 300\,\mu$m thick silicon detectors. The total charge Q_s contained in the detector current pulse $I_s(t)$ is proportional to the energy deposited in the detector

$$Q_s = \int I_s(t)dt \propto E. \tag{4.8}$$

Three basic input amplifier configurations exist:

- charge sensitive amplifier (CSA)
  The CSA actively integrates the detector current on the amplifier *feedback* capacitor (fig. 4.5 a). This is the best configuration concerning noise. In addition the CSA features a purely resistive input impedance.

- voltage amplifier
  The signal current is integrated on the *detector* capacitance itself. The voltage across the capacitor is amplified. Since the amplifier output voltage depends on the detector capacitance C_d,
  $$V_o = -A\frac{Q_s}{C_d + C_i}, \tag{4.9}$$
  this configuration is only of interest if C_d is constant, i.e. the depletion depth is constant. Temperature fluctuations and radiation damage can lead to a variation of C_d. Beside this, the voltage amplifier is more noisy than the charge sensitive loop.

- current amplifier
  The signal current is directly amplified and converted into a voltage. The main disadvantage of this loop configuration is the inductive input impedance [Gat84], which limits the use with large capacitive loads. The current amplifier is also more noisy than the CSA.

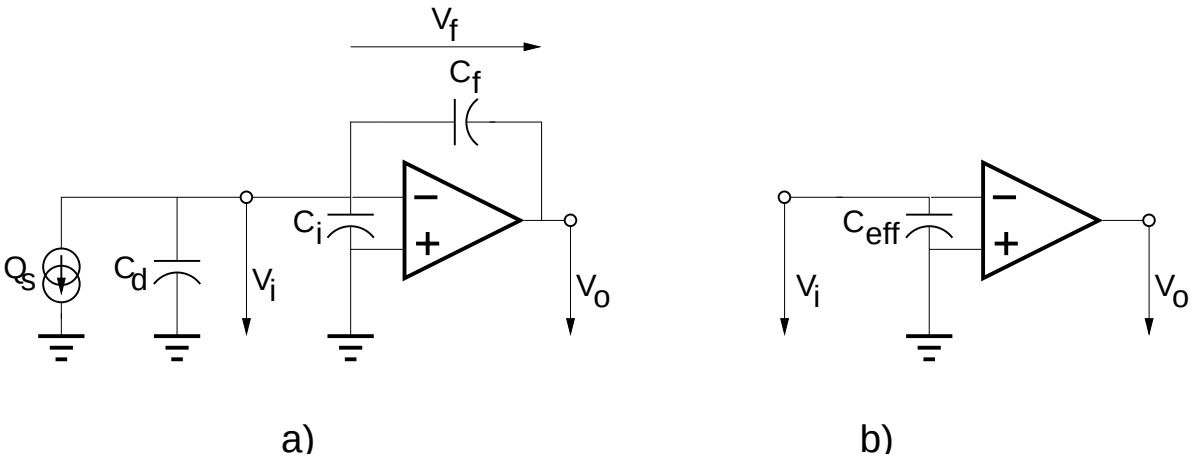


Figure 4.5: Signal acquisition with a charge sensitive amplifier (CSA). The detector is represented by a current source in parallel with a capacitance.

The input transistor of the CSA mainly contributes with it's gate-source capacitance C_{gs} and gate-bulk capacitance C_{gb} to the capacitive input load $C_i = C_{gs} + C_{gb}$ (fig. 4.5 a). Since the gate oxide capacitance per area is an order of magnitude higher than the gate-diffusion overlap capacitance per area, C_{gs} dominates C_i. The output voltage of a charge sensitive amplifier follows from $V_i - V_o - V_f = 0$, $V_o = -A_v V_i$ (A_v: open loop voltage gain) and $Q_s = Q_f + Q_d + Q_i$:

$$V_o = -\frac{Q_s}{C_f + \frac{1}{A_v}(C_f + C_i + C_d)} \overset{A_v \gg 1}{\approx} -\frac{Q_s}{C_f} \tag{4.10}$$

For low frequencies the input impedance of the CSA is represented by the *effective* or *dynamic* input capacitance $C_{eff} = C_f(1 + A_v) + C_i$ (cf. fig. 4.5 b). The signal charge Q_s is divided between the detector capacitance C_d and C_{eff} ($Q_s = (C_d + C_{eff})V_i = -\frac{1}{A_v}(C_d + C_{eff})V_o$). The efficiency for transferring charge from the detector to the amplifier is given by

$$\frac{Q_{eff}}{Q_s} = \frac{Q_{eff}}{Q_{eff} + Q_d} = \frac{C_{eff}}{C_{eff} + C_d} = \frac{1}{1 + \frac{C_d}{C_{eff}}} = \frac{1}{1 + \frac{C_d}{C_i + C_f(1+A_v)}} \overset{C_{eff} \gg C_d}{\longrightarrow} 1, \tag{4.11}$$

where Q_d is the charge remaining on the detector. A low input impedance, i.e. high input capacitance, is important for a complete charge transfer to the electronics. Table 4.1 gives a numerical example for $C_f = 400$ fF, $C_i = (8.74 + 1.35)$pF and $A_v = 3.8 \cdot 10^3$, which are the corresponding parameters of the *Beetle* preamplifier (front-end set 2c, see table 4.7). The effective input capacitance is calculated as $C_{eff} = 1.53\,\text{nF}$.

C_d	Q_{eff}/Q_s
10 pF	99.4 %
30 pF	98.1 %
60 pF	96.2 %

Table 4.1: Charge transfer efficiency for different detector capacitances.

An incomplete charge transfer to the electronics results in a loss of sensitivity and possible crosstalk within the detector to neighbouring channels.

Signal Processing

Signal processing in our context means *filtering* and *sampling* the amplified input signal. A filter modifies the frequency spectrum of a propagated pulse. In the following, this topic is referred to as pulse *shaping*. Shaping the amplifier output signal has mainly two reasons:

1. pile-up prevention
   The response of a charge sensitive amplifier on a delta-shaped current pulse $I_s\delta(t)$ is a voltage step with a fast exponential rise. Since the charge integrated on the feedback capacitance has to be removed to avoid saturation of the amplifier, a resistive feedback network is usually used to discharge C_f. This feedback resistor produces an exponential tail of the CSA output pulse with a time constant τ of a few μs to 100 μs. The large time constant of the tail causes the problem of *pile-up*: if further input signals arrive within τ, their output signal will add to the tail of the predecessor pulse, which produces distortion. Shortening the pulse tail by shaping avoids this problem.

2. signal-to-noise optimisation
   A restriction of the bandwidth broadens the pulse and results in an improved signal-to-noise ratio.

These two objectives are conflicting: the first one aims at *decreasing* the pulse width, the second one at *increasing* it. For a certain application also the dynamic range and power consumption have to be considered.

CR-(RC)^n Pulse Shaping

CR-RC pulse shaping is a widely used technique. The frequency spectrum is confined by filtering low frequencies by differentiation (CR) and high frequencies by integration (RC). The form of the output pulse is called *semi-Gaussian*. A theoretical 18% improvement of the signal-to-noise ratio w. r. t. simple CR-RC shaping can be achieved if the pulse has ideal Gaussian form. But this is not realizable electronically [Leo94]. However, with a network of one CR differentiation stage and a series of many RC integrating stages (CR-RC-RC-RC-... = CR-(RC)^n) a pulse can be produced which is close to a Gaussian shape. Figs. 4.6 and 4.7 show the output pulse of shapers with multiple integration stages. In fig. 4.6 all integration stages have the same time constant $\tau_{int} = (RC)_{int}$, whereas in fig. 4.7 the peaking time is constant. This is achieved by varying the integration time constant of subsequent stages according to $\tau_{n+1} = \frac{1}{n+1}\tau_n$ [Spi01]. The pulses are more symmetrical with a faster return to the baseline. This improves the rate capability at the same peaking time, provided that the preceding preamplifier is not limited by saturation.

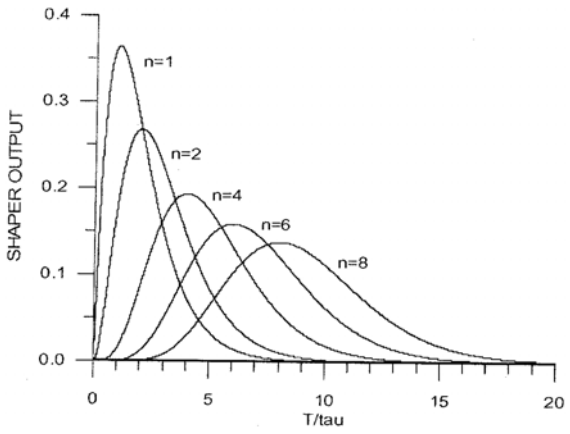


Figure 4.6: Output pulses of shapers with multiple integration stages. The integration time constant is the same for all stages [Spi01].

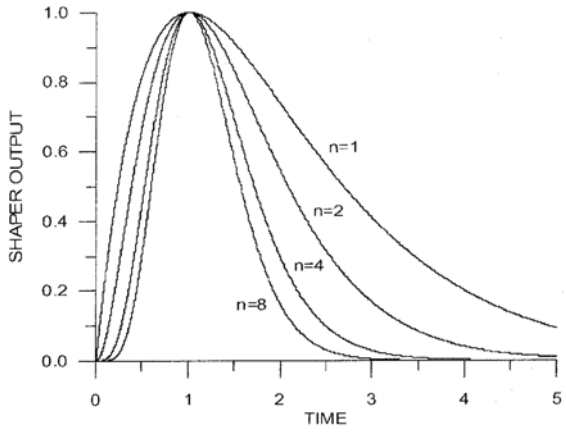


Figure 4.7: Output pulses of shapers with multiple integration stages. The integration time constant of subsequent stages is varied according to $\tau_{n+1} = \frac{1}{n+1}\tau_n$ [Spi01].

The disadvantage of Gaussian pulses is their larger width compared to RC shaped pulses, which can cause overlap problems at high count rates. The peaking time of the shaper has to match the primary signal width. Otherwise a loss in signal amplitude occurs, which is called 'ballistic deficit'.

With $n = 1$ one obtains the simplest shaper configuration: the CR-RC shaper (n is also referred to as the order of the shaper). Fig. 4.8 shows the passive and active implementation of the filter. The corresponding transfer functions are of second order, i.e. the denominator polynom is of order 2. Note that the passive implementations depicted in fig. 4.8 a) and b) have the same transfer functions for correctly chosen R_i, C_i.

They are given by

$$\frac{V_o}{V_i} = \frac{s\tau_1}{1+s\tau_1+sR_1C_2+s\tau_2+s^2\tau_1\tau_2} \quad \text{for configuration a)} \tag{4.12}$$

$$\frac{V_o}{V_i} = \frac{s\tau_1}{1+s\tau_1+sR_1C_2+sR_2C_1+s^2\tau_1\tau_2} \quad \text{for configuration b)} \tag{4.13}$$

(with $\tau_1 = R_1C_1, \tau_2 = R_2C_2$).

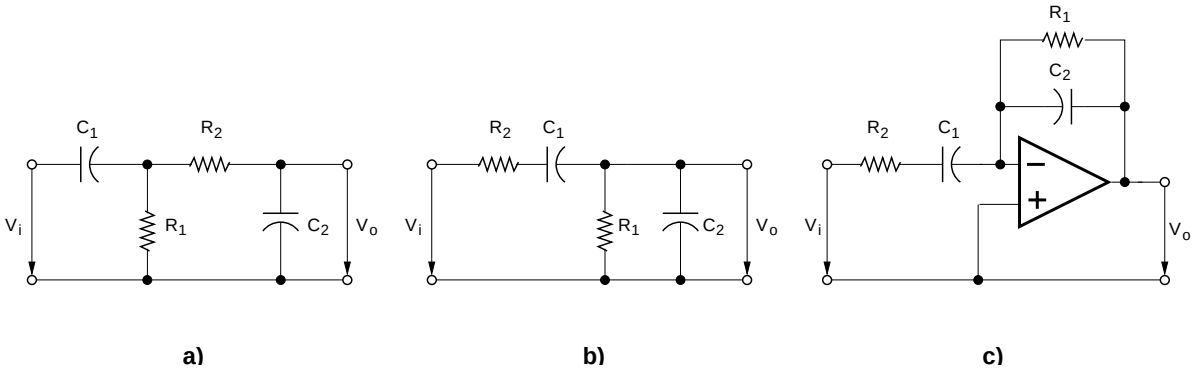


Figure 4.8: Passive (a) and (b) and active (c) implementation of the CR-RC shaper.

4.2 Requirements on a Silicon Microstrip Readout Chip for LHCb

The requirements on the *Beetle* readout chip are determined on the one hand by the parameters of the detectors to be read out and their aimed tracking or particle identification performance, and on the other side by the constraints of the standardised LHCb readout system. The latter ones are common to all electronic components in the corresponding trigger level. The *Beetle* as readout chip for the VELO, the inner tracker and the RICH is part of the L1 trigger electronics and has therefore to provide the L0 latency. As readout chip for the pile-up veto counters it operates within the L0 trigger. Table 4.2 summarises the key parameters of the three LHCb detectors to be read out by the *Beetle.* The constraints set by the LHCb readout system are listed in table 4.3, while the resulting *Beetle* specifications are given in table 4.4.

The chip's input pitch adapts to the average strip pitch of the VELO sensors. The sampling frequency equals the LHC bunch crossing frequency and also defines the shaper's peaking time. The pulse remainder, the undershoot settling time and the signal-to-noise ratio are related to the hit finding efficiency. Depending on the channel occupancy, a long undershoot reduces the signal and results in an efficiency loss. The maximum input charge rate directly correlates with the occupancy. The maximum tolerable power consumption is limited by the cooling power of the VELO, where the *Beetle* operates in the secondary vacuum. The pedestal variations per channel along the pipeline contribute to the chip's signal-to-noise performance, but can be

[4] Multianode Photo Multiplier Tube
[5] assuming 10% occupancy and an input signal of 24,000 el.
[6] Joint Test Action Group [IEE01]

	VELO	Inner Tracker	RICH
technology	silicon strip (r-ϕ) single-sided, n-on-n	silicon strip single-sided, p-on-n	MaPMT[4] n.a.
no. of channels	204,800	$\sim$ 350,000	224,256
channel pitch	$37 - 98\,\mu$m	$\sim 200\,\mu$m	n.a.
channel occupancy	$\sim 1\%$	$\sim 3\%$	$\leq 4\%$
detector thickness	$300\,\mu$m/$220\,\mu$m	$300\,\mu$m	n.a.
detector capacitance	$10 - 30$ pF	~ 30 pF	~ 2 pF
charge of a MIP	22,500 el./16,000 el.	22,500 el.	$\sim$ 300,000 el.
typical signal	1 MIP	1 MIP	1 MIP
coupling to readout electronics	AC	AC	DC
total accumulated dose	≤ 10 Mrad	≤ 10 Mrad	≤ 100 krad
average dose rate	2 Mrad/a	2 Mrad/a	3 krad/a
SEU rate at average dose rate	$< 10^{-6}$ Hz	—	—
operation environment	secondary vacuum	air/nitrogen	air
ambient temperature	-10 to $+25^\circ$ C	$\approx 5^\circ$ C	$\approx 25^\circ$ C

Table 4.2: Key parameters of the LHCb detectors [VEL01, ITR02, RIC00] to be read out by the *Beetle* chip.

separated from the front-end contribution by having pedestal look-up tables for the pipeline columns. The pedestal uniformity across the channels as well as the common-mode noise only affect the dynamic range.

parameter	value	description
bunch crossing frequency	40.08 MHz	
max. level 0 (L0) trigger rate	1.1 MHz	
L0 latency	4 μs	= 160 clock periods
L0 gap	none	no. of bunch crossings after a L0 trigger with no further L0 trigger acceptance
L0 derandomiser depth	16	These parameters are chosen to have negligible dead-time at a trigger rate of 1 MHz (900 ns = (32 + 4)×25 ns)
L0 derandomiser readout time	900 ns	
reading back front-end registers	yes	
no. of L0 resets	1	

Table 4.3: Basic specifications of the LHCb front-end electronics [FEP].

input channel pitch	50 μm
sampling frequency	40.08 MHz
front-end peaking time $t^{0/100}$	$\leq$ 25 ns
pulse remainder in next bunch crossing	$<$ 30 %
signal-to-noise (S/N) ratio after 10 Mrad	$>$ 14
input charge range without saturation	$\pm$ 110,000 electrons
tolerable input charge rate	$>$ 15 nA[5]
power consumption	$\leq$ 6 mW/channel
max. latency	4 μs
acceptable trigger rate	1 MHz
acceptance of consecutive triggers	yes
depth of trigger buffer	16
dead-timeless readout	yes
readout time per event	$\leq$ 900 ns
required linearity	$\geq$ 95%
driving capability of analogue output	$\approx$ 10 m
acceptable total ionising dose	$\geq$ 10 Mrad (= 100 kGy)
SEU detection and correction	yes
synchronisation check	yes
programming interface	I^2C/JTAG[6]

Table 4.4: Requirements on the *Beetle* readout chip.

4.3 Beetle Chip Architecture

Microstrip readout chips can be categorised [Feu99] as *pure front-end chips*, integrating amplifiers and sometimes discriminators, *analogue multiplexer chips*, which implement amplifiers followed by a sample and hold stage and an analogue multiplexer, *analogue pipeline chips* integrating a preamplifier and shaper per channel followed by a switched capacitor array for intermediate storage and an analogue multiplexer, *binary pipeline chips* propagating the discriminated amplifier signal through a digital pipeline and multiplexer and finally *digitising pipeline chips* which are basically analogue pipeline chips with an integrated analogue to digital converter (ADC).

The *Beetle* chip can be operated as an *analogue or* alternatively as a *binary pipeline chip*. It implements the basic RD20 front-end electronics architecture [Bre94a, Bre94b, Hor93]. Figure 4.9 shows the schematic block diagram of the chip. 128 channels are integrated, each consisting of a low-noise charge-sensitive preamplifier, an active CR-RC pulse shaper and a buffer. They form the analogue front-end. A comparator discriminates the front-end's output pulse. The threshold is adjustable per channel and input signals of both polarities can be processed. The memory for intermediate storage (pipeline) is realized as a switched-capacitor array of 130×187 cells, using the gate oxide capacitance of a transistor. Writing to the pipeline is synchronous to the LHC bunch-crossing frequency at 40 MHz. The memory provides a programmable latency of maximum 160 clock periods and integrates a derandomising trigger buffer of 16 stages. A resetable charge-sensitive amplifier (pipeamp) retrieves the stored signal from the pipeline and transfers it to a (analogue) multiplexer for serialisation. The multiplexer can operate in three different modes carrying the 128 channels on either 4, 2 or 1 output port. Within a readout time of minimum 900 ns, differential current drivers bring the serialised data off chip. The output of a sense channel is subtracted from the analogue data to compensate common mode effects. A test channel enables direct access to two nodes of the analogue signal path: the output of the preamplifier and the output of the pipeline readout amplifier (fig. 4.9).

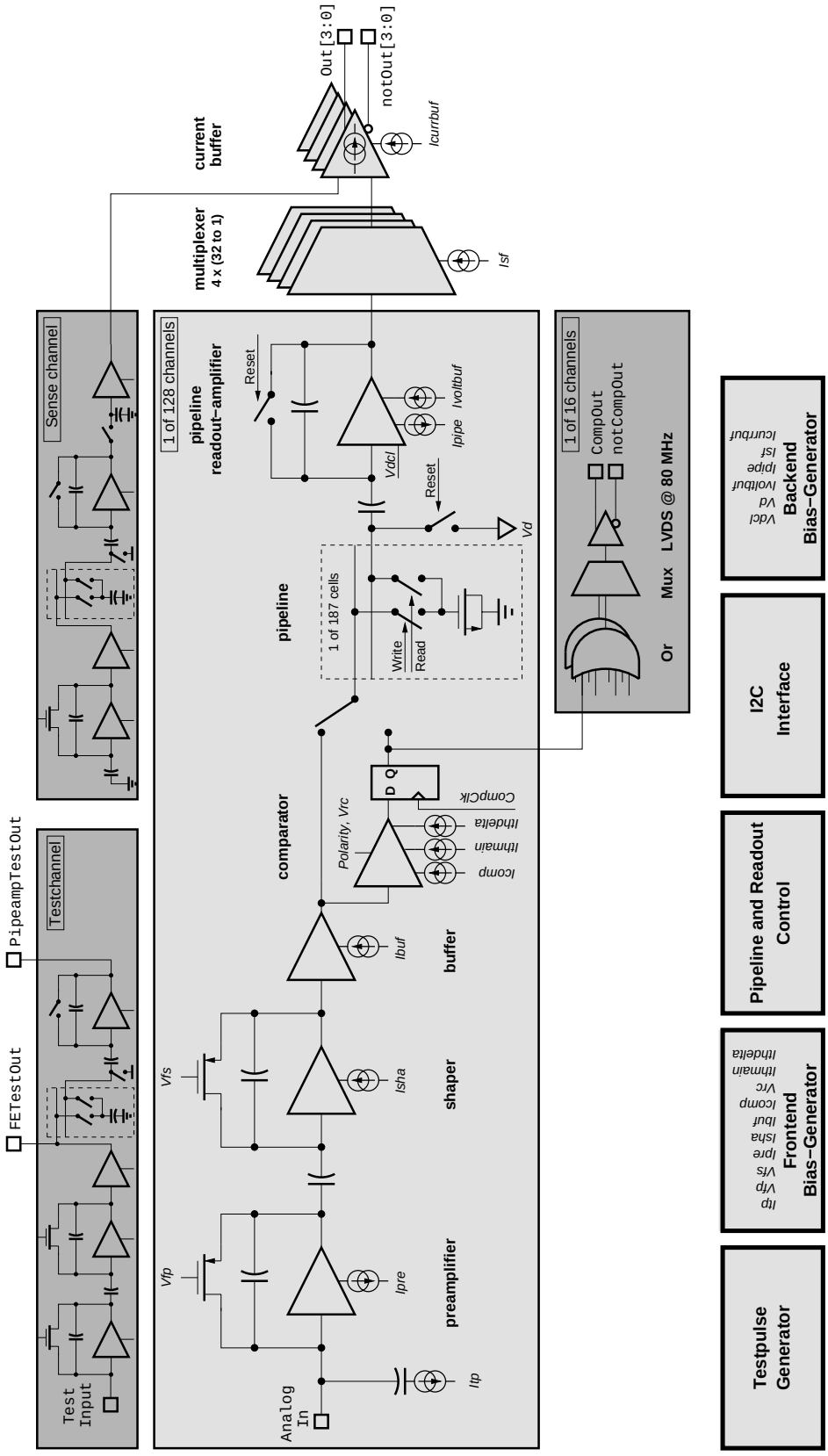


Figure 4.9: Schematic block diagram of the *Beetle* chip.

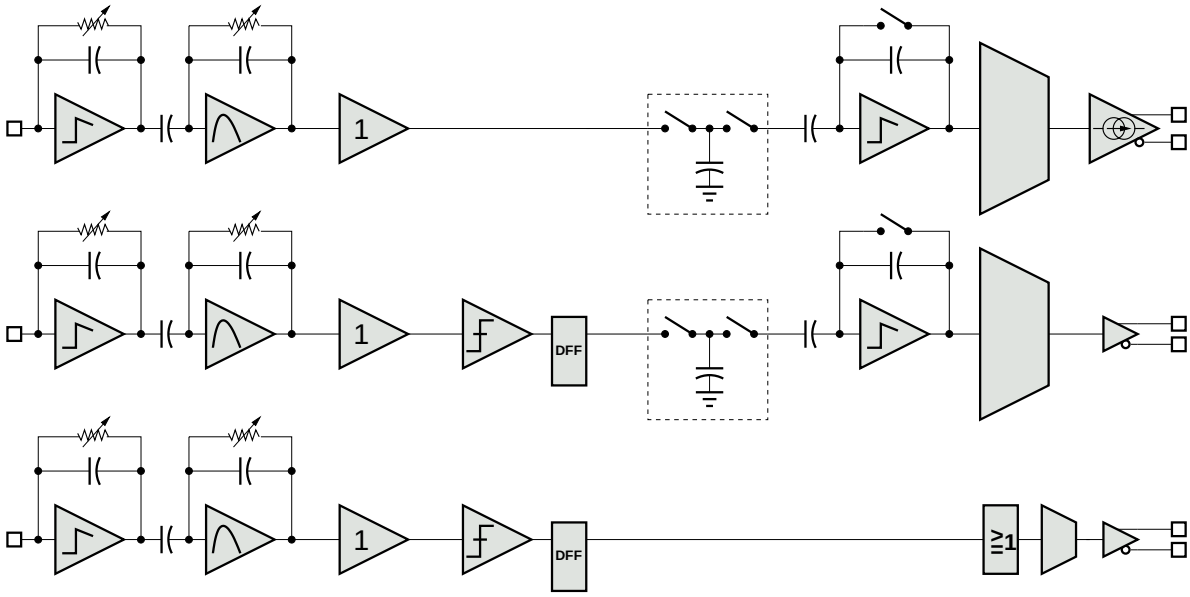


Figure 4.10: Readout paths of the *Beetle* chip. From top to bottom: analogue pipelined, binary pipelined, prompt binary path.

The chip provides three different signal readout paths (see fig. 4.10):

- The *analogue pipelined readout* (fig. 4.10, top) propagates the analogue output of the front-end to the pipeline. The semi-Gaussian pulse is sampled with the sampling clock (*Sclk*), i.e. the LHC bunch crossing clock, at 40 MHz at its maximum and stored on a pipeline capacitance. Reading out a triggered event is performed via the pipeamp, multiplexer and current buffer(s).

- For the *binary pipelined readout* (fig. 4.10, middle) the front-end's output is discriminated. The logic output levels of the comparator are represented by analogue voltages matching the dynamic range of the pipeline and the pipeamp. The further signal path equals the analogue pipelined one, beside the fact that data is transmitted with doubled rate, i.e. nominally with 80 MHz. The output characteristics meet the LVDS standard [LVD97].

- The *prompt binary readout* (fig. 4.10, bottom) uses the discriminator output. Four adjacent comparator channels are logically ORed, synchronised with the comparator clock (*CompClk*), multiplexed by a factor of 2 and routed off the chip via low voltage differential signalling (LVDS) ports at double data rate (80 MHz).

In total 5 voltages and 11 currents are needed for biasing the analogue stages. On-chip digital-to-analogue converters (DACs) generate these bias currents and voltages with a resolution of 8 bits. An integrated stabilised current source provides the necessary reference current.

For test and calibration purposes a charge injector with adjustable pulse height is implemented on each channel (including the test channel).

The *Beetle* chip performs *single sampling* of the shaped pulse, i.e. the pulse maximum is sampled and stored on a capacitor. A logic circuitry controls the corresponding switches. The pipeline is operated as a ring buffer. In each bunch crossing the pulse amplitudes of the

130 channels (128 channels plus test channel plus common-mode sense channel) are stored in a pipeline column. After 187 cycles, which corresponds to the pipeline depth, previous events are overwritten, unless an external trigger has occurred in the meantime. An incoming trigger stores the pipeline location, i.e. the column number, in the derandomising trigger buffer (FIFO) and marks the pipeline column. This trigger mark prevents the corresponding column to be overwritten. Beside event storage the second task of the control logic is the readout of a triggered event. For that, several control signals have to be applied to the pipeline readout amplifier and the multiplexer. After finishing a readout sequence the marked pipeline column is released and the entry in the FIFO is removed.

For applications which do not require a high readout speed, several *Beetle* chips can be configured in a *daisy chain* sharing their output lines. The chain is formed by two token paths. The position (first, intermediate, last) of an individual chip in the daisy chain is defined by a register.

The programming interface of the chip meets the I^2C-standard [Phi95]. This allows writing and *reading* the *Beetle* registers, which is an important requirement to the LHCb front-end electronics (cf. sec. 4.2).

The chip is fabricated in a standard CMOS[7] technology featuring a 0.25 μm lithography which results in an *effective* minimum gate length of 0.18 μm. The bulk is formed of a p-doped epitaxial layer on a strongly p-doped ($p+$) substrate. Three metal layers for interconnection, one for capacitors and one polysilicon layer are available. This allows, beside NMOS and PMOS transistors, to build polysilicon resistors[8] and (linear) metal-metal capacitors which are important devices for analogue circuit design. The gate oxide thickness is 62 Å, the nominal supply voltage is 2.5 V.

The die has a size of 5.5×6.1 mm^2 in case of *Beetle1.0* and *Beetle1.1* and 5.1×6.1 mm^2 for *Beetle1.2*. The layout with the corresponding floor plan is depicted in fig. 4.11. The placement of the building blocks follows to some extend the signal path (figs. 4.9, 4.10): Located at the left edge of the die are the fourfold staggered 128 analogue input pads with a pitch of 40.24 μm, followed by ESD[9] protection diodes. With a channel-to-channel pitch of 40.24 μm the test pulse injection circuit, the front-end and the comparator link up. Below this part the front-end bias generator circuitry is placed. After the comparator, the channel-to-channel pitch is reduced to 30.0 μm, which requires a pitch adaptor. The pipeline with the pipeamp and the multiplexer follow. The area below the reduced pitch region is used for locating the digital circuitry (pipeline and readout control, I^2C-interface) and the back-end bias generators. At the right edge of the die the output pads, power supply pads, probe and control pads are placed. The pads on the top and bottom side of the chip provide the LVDS comparator outputs and the (separate) comparator power supply pads (see appendix A and B for a detailed pad map). If no comparator outputs are used, pads on the top and bottom side do not need to be bonded. This allows an overall pitch of 50 μm when mounting several chips side by side.

[7] Complementary Metal Oxide Semiconductor: complementary means, that transistors using electrons (NMOS) as well as those using holes (PMOS) as majority charge carriers are available. MOS represents the sequence of layers at the gate electrode.

[8] Also n-well resistors are available, but those are in comparison with polysilicon resistors not radiation hard (cf. section 3.2.3).

[9] Electrostatic discharge

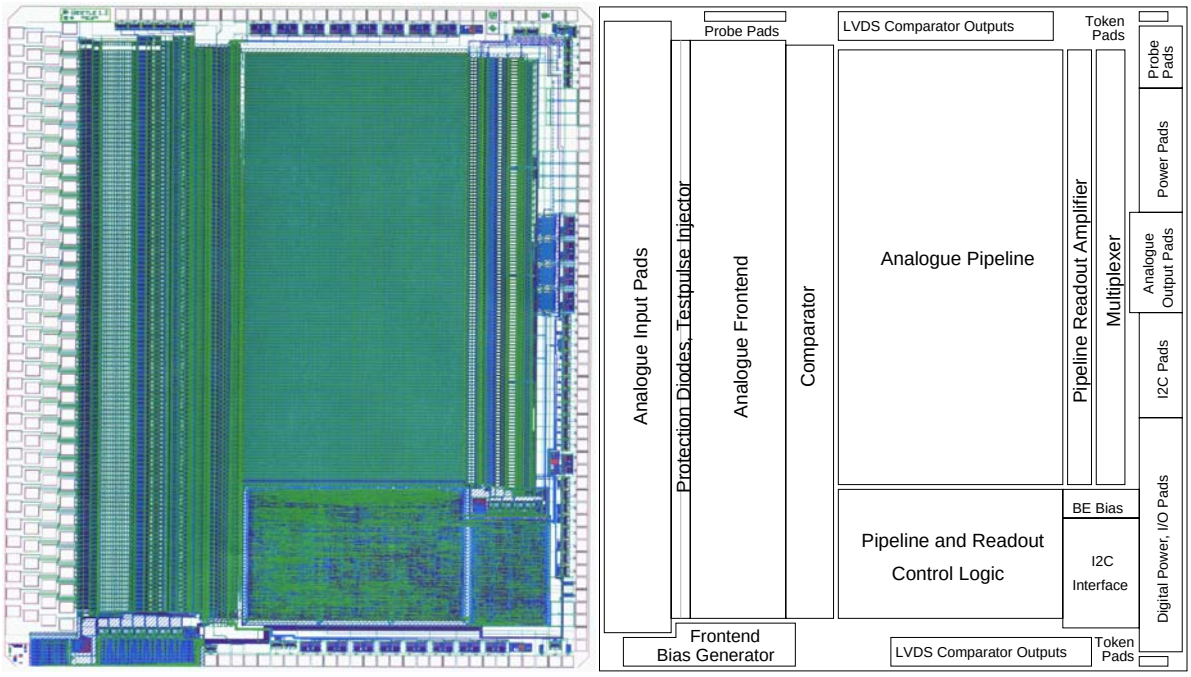


Figure 4.11: Layout of the *Beetle1.2* chip version and its corresponding floor plan. The die size is $(5.1 \times 6.1)\text{mm}^2$.

4.4 Components

This section details the schematics of the main *Beetle* components. The underlying design concepts are described and discussed. The order follows the signal flow. The schematics show the physical devices (transistors, capacitors, resistors) plus the main contributing parasitic capacitances[10].

4.4.1 Front-end

The analogue front-end is formed by a charge sensitive preamplifier, a CR-RC shaper and a source follower as buffer. It has been developed by *E. Sexauer* [Sex01] and improved by *S. Löchner* [Löc03]. Fig. 4.12 depicts the schematic of the three stages. The amplifier core of the preamplifier as well as the shaper is a *folded cascode*. Fig. 4.13 depicts three basic amplifier stages: the common-source, the (linear) cascode and the folded cascode. A *cascode* consists of a common-source stage followed by a common-gate stage. It combines two transistors (a wide input transistor and a narrower cascode transistor) to obtain

- the high transconductance and low noise of a wide transistor,
- the high output resistance and low output capacitance of a narrow transistor,
- the reduced capacitance between output and input.

[10]Parasitic capacitances are either formed within a MOS transistor by overlapping gate and diffusion areas or by interconnecting lines coupling to neighbouring structures.

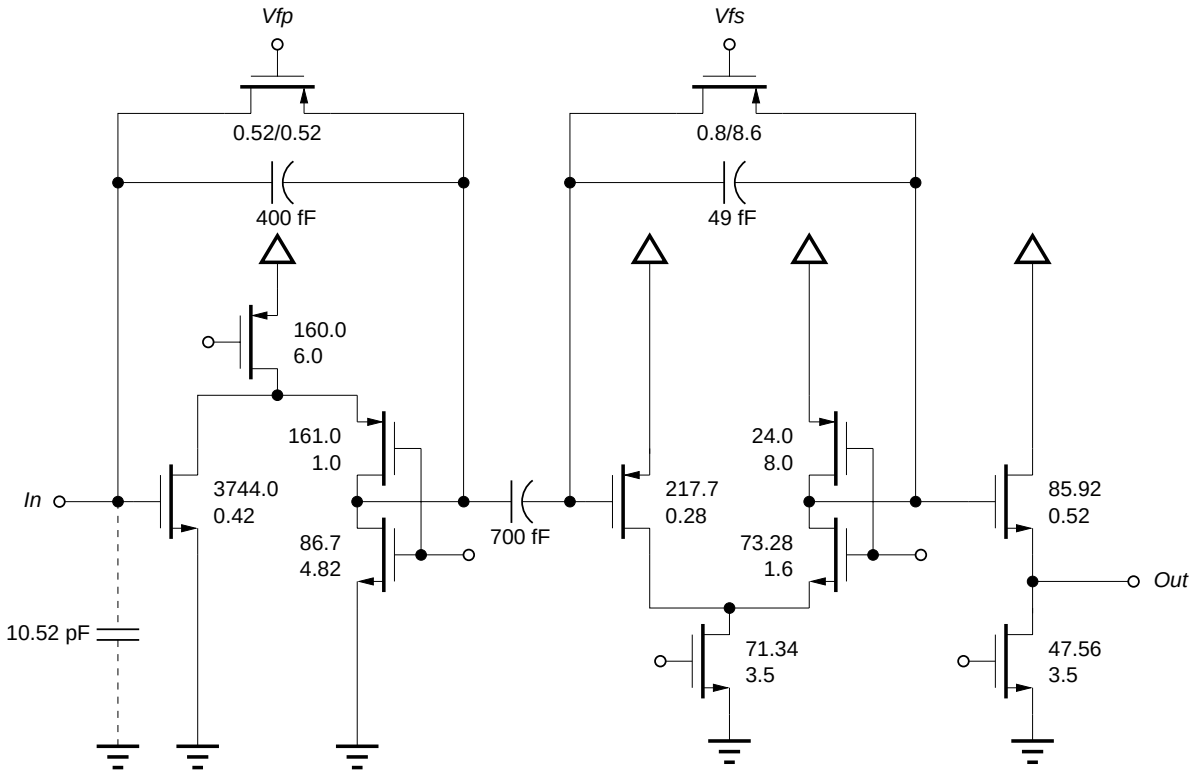


Figure 4.12: Schematic of the *Beetle* front-end formed by the preamplifier, shaper and buffer. The transistor dimensions (W/L) correspond to the front-end implemented in *Beetle1.2* (set 2c in table 4.7). The parasitic capacitance at the input is the sum of the gate-oxide capacitance (C_{ox}=8.74 pF), the gate-source overlap capacitance (C_{gs}=1.35 pF) and the interconnection capacitance (C_{int}=0.43 pF).

For low noise applications the input transistor requires a high drain current, which has to flow through the whole chain in case of the linear cascode. This reduces the output resistance since the cascode transistor has to operate at this high current. The *folded cascode* overcomes this problem by using a cascode transistor *complementary* to the input device. This requires an additional (active) load for the cascode transistor but allows it to operate at a lower current, i.e. a higher output resistance.

The main disadvantage of folded cascodes is their poor or non-existing power supply rejection (PSR). The source contact of the input transistor is connected to one of the supply voltages depending on the transistor type. This node acts as the non-inverting input of the amplifier. A variation on the power supply lines is amplified like a signal. It is therefore important to establish stable power supplies with variations small compared to the expected signals.

The response of the front-end to a delta-shaped current pulse and a current pulse of a silicon sensor is shown in fig. 4.14. The primary current pulse results from a model of a 300 μm thick silicon sensor with a bias voltage applied, which is 10 V above the depletion voltage. A charge of 3.6 fC is injected. Clearly visible is the 'ballistic deficit' caused by a primary signal width, which is comparable to the shaper peaking time. The resulting loss in signal amplitude is $\approx 5\%$.

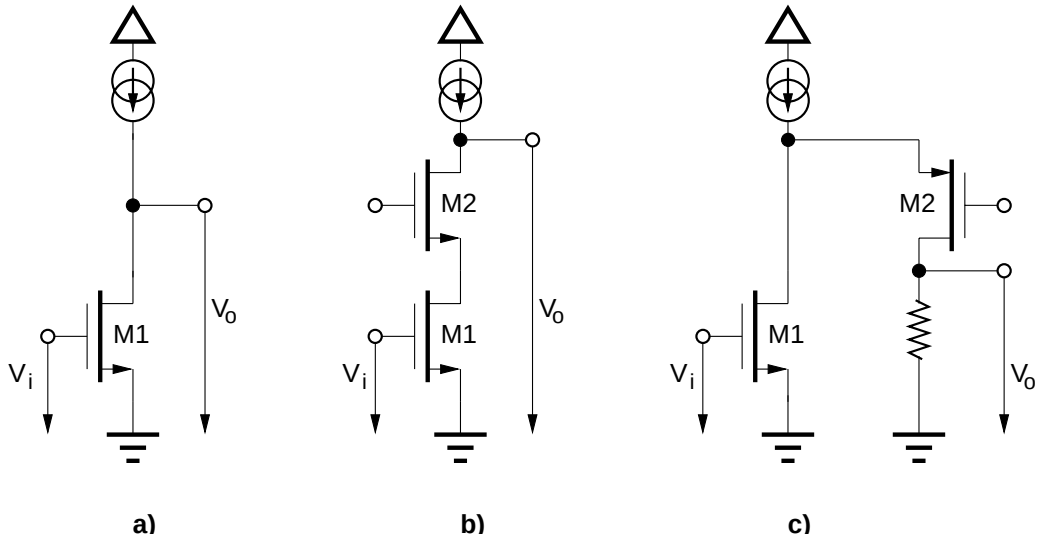


Figure 4.13: Basic amplifier stages. The source-follower (a), the (linear) cascode (b) and the folded cascode (c) (Only the configurations using an NMOS transistor as input device are shown).

Preamplifier

In a well designed cascade, i.e. series connection, of amplifier stages the noise is determined by the *first* stage. Consider a series of 2 amplifiers with gain A_i and input noise[11] levels N_i (see fig. 4.15). The input signal-to-noise ratio $(\frac{S}{N})_{in} = \frac{S}{N_1}$. The output signal-to-noise ratio is given by

$$\left(\frac{S}{N}\right)^2_{out} = \frac{(A_2A_1S)^2}{(A_2A_1N_1)^2 + (A_2N_2)^2} = \frac{S^2}{N_1^2 + (\frac{N_2}{A_1})^2} = \left(\frac{S}{N}\right)^2_i \cdot \frac{1}{1 + (\frac{N_2}{A_1N_1})^2} \overset{A_1 \gg 1}{\longrightarrow} \left(\frac{S}{N_1}\right)^2, \tag{4.14}$$

assuming uncorrelated noise.

With a high gain in the first amplifier stage, the signal-to-noise ratio at the output is dominated by the first stage. The same argument can be applied to the input stage itself. The main contributing noise source is therefore the *input transistor* of the preamplifier, assuming a sufficient high gain. The thermal noise of the channel resistance is the dominating noise source. The equivalent noise charge (ENC) is given as a function of the input capacitance C_p by [Nyg91]

$$\frac{\text{ENC}}{C_p} = \sqrt{\frac{8(1+\eta)}{3}\frac{k_BT}{T_s \cdot g_m}} \quad [C/F], \tag{4.15}$$

where

g_m is the (gate-source) transconductance,

g_{mb} is the bulk-source transconductance,

$\eta = \frac{g_{mb}}{g_m}$ and T_s is the shaping time ($= 25\,\text{ns}$).

[11] A noisy amplifier can be represented by a noiseless one with a series and a parallel noise source at its input. The two noise sources can be partly or even completely correlated.

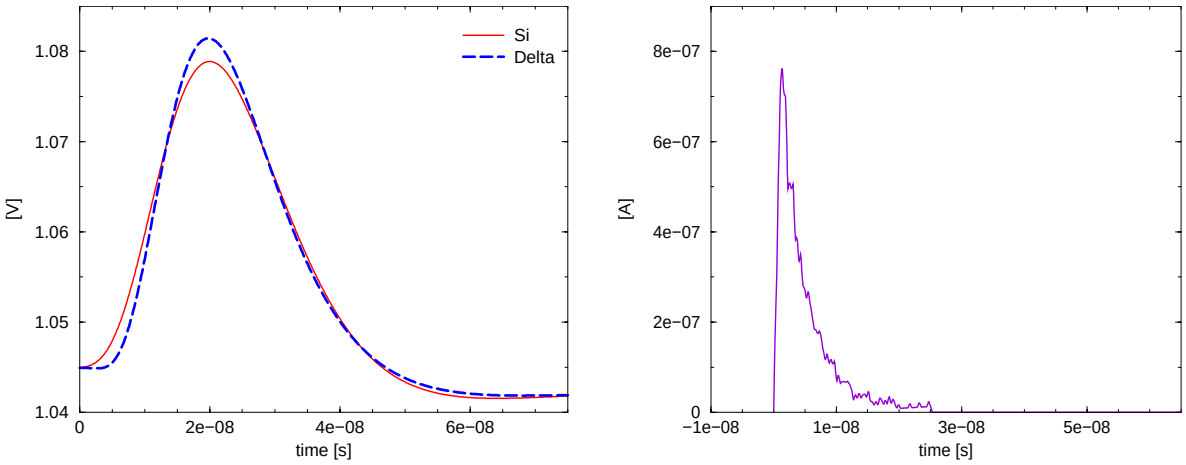


Figure 4.14: Left: Transient response of the front-end to a delta-shaped current pulse (dashed line) and a current pulse of a silicon sensor (solid line). Right: Simulated primary current pulse of a silicon sensor. The data of the sensor pulse has been provided by *P. Sievers* [Sie02].

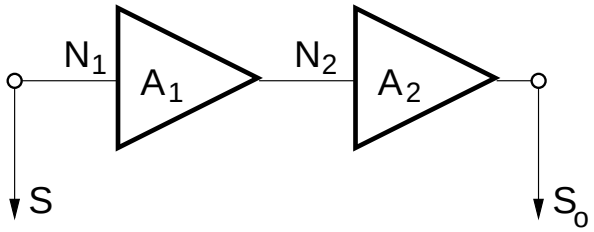


Figure 4.15: Cascade of two amplifier stages. In a well designed system the noise is defined by the first stage.

For the *Beetle* front-end (set 2c, cf. table 4.7) the equivalent noise charge is calculated at a bias current of 600 μA to ENC/C_p = 46.7 e^-/pF. Flicker noise can be neglected, since the subsequent shaping stage attenuates low frequencies due to its band pass characteristic. For a low-noise amplifier, the transconductance g_m has to be large. Since g_m of a transistor is $\propto W/L$ (eq. 3.6), a short transistor length L of the input transistor is desirable. The length of the NMOS input transistors has been chosen substantially bigger than the minimum possible feature size of the technology ($L_{eff} = 0.24\,\mu m$) to avoid *short channel effects*[12]. The width W of the input transistor has been chosen as 3.744 mm, which is achieved in the layout by connecting 156 devices of $W/L = 24/0.42$ in parallel. The input FET for it's own takes in an area of about 8,500 μm^2.

[12]For example, *drain induced barrier lowering*, *channel length modulation*, *punch through*, *threshold voltage roll-off*, *mobility reduction*.

Test Stimulus and Calibration

In a system with a high number of electronic channels it is often difficult to apply an external test stimulus to individual or all front-end amplifiers. Therefore an *on-chip* test stimulus generation has been implemented. This allows a calibration as well as a connectivity check on a system level. The testpulse circuit is shown in fig. 4.16. Four different testpulse types are generated which form a step like pattern. The steps correspond to +2, +1, −1, −2 times the input signal amplitude. This pattern couples periodically to the 128 channels and the test channel. The amplitude of the injected pulse is adjustable via the *Itp* register. Each channel can be selected to inject a test pulse into the front-end. This is controlled by a 128 bit register (*TpSelect*) implemented as a shift register (cf. section 4.4.7). All four circuit types are represented in fig. 4.16: for a unit step the coupling capacitors are 100 fF, for a double step 200 fF. A positive step uses the signal distribution (`CK, notCK`) indicated by '+', a negative step the one labelled '−'. The two NMOS transistors with their gate fixed to the positive supply voltage serve as active loads.

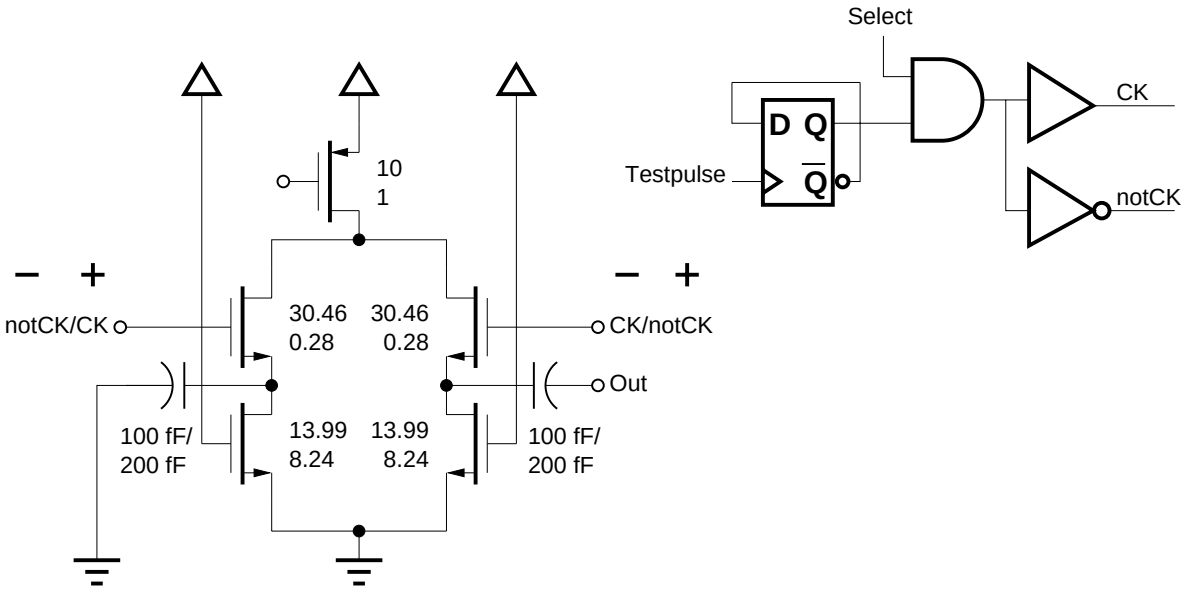


Figure 4.16: Schematic of the test pulse injection circuit. Four variations exist (+2, +1, −1, −2): for a unity step height the coupling capacitors are 100 fF, for a double unity step 200 fF. A positive step uses the signal distribution (`CK, notCK`) indicated by '+', a negative step the one labelled '−'. The two NMOS transistors with their gate fixed to the positive supply voltage serve as active loads.

4.4.2 Comparator

The front-end's output pulse has a DC-offset of about 1 V which varies from channel to channel due to doping fluctuations. In order to discriminate the shaped pulse with a resolution of some 1,000 electrons (a MIP having some 10,000 electrons), it is necessary to eliminate the varying DC component of the pulse. This can be accomplished in two ways [Ver99a]:

- AC-coupling
  By introducing a CR-high-pass filter between the front-end and the comparator the DC-component can be removed. The filter resistor is connected in this scheme to a reference voltage half the supply voltage. Also the threshold voltage will refer to this reference voltage.

  The used technology provides only two supply voltages, 2.5 V and 0 V. The reference voltage has therefore to be generated on chip. Guaranteeing a stable voltage halfway the supply voltage which shows no channel variations is not easy. In addition, realizing a sufficient small transit frequency, i.e. a large time constant, needs resistances in the order of MΩ since integrated capacitances are limited to about 10 pF. With long channel transistors operating in the ohmic region this can be accomplished.

- DC-level extraction
  By low-pass filtering the shaper pulse the DC-component is extracted. In a subsequent stage this is added to or subtracted from the threshold.

The *Beetle* comparator (designed by *Hans Verkooijen*) [Ver99b] uses the latter approach. It consists of an integrator, a threshold generator, a discriminator, a synchronisation stage and a level shifter (fig. 4.17).

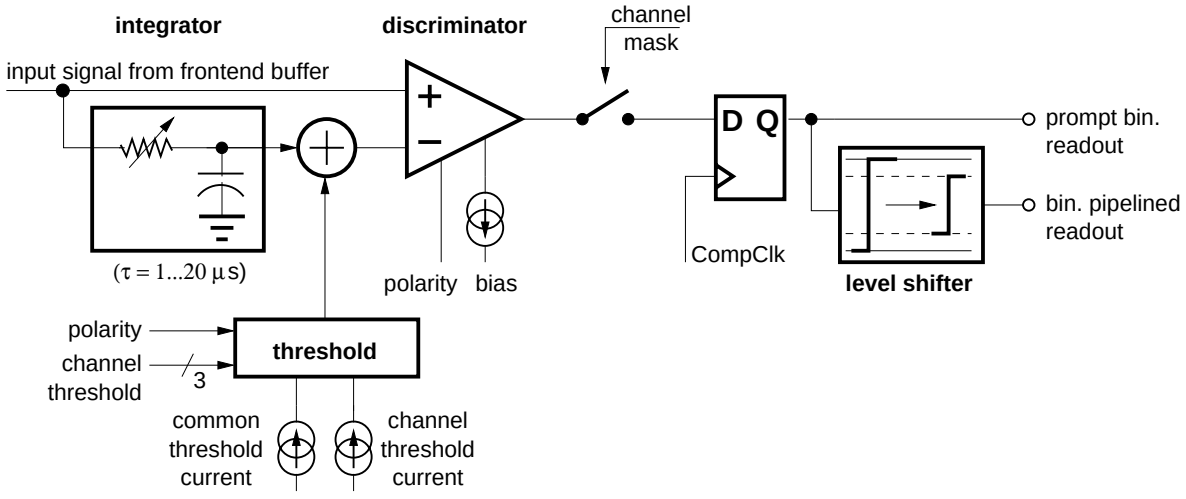


Figure 4.17: Schematic block diagram of the comparator.

The DC-offset is extracted by low-pass filtering the front-end output pulse with a time constant τ of a few μs. In *Beetle1.0* and *Beetle1.1* $\tau = 5\,\mu s$, in *Beetle1.2* the time constant is adjustable between 1 and 20 μs. The varying DC-offset is added to the threshold voltage in each channel. The threshold level is adjustable per channel with a resolution of 3 bits. The discriminator core itself consists of 2 differential amplifiers. A switch allows the detection of input signals of both polarities. The discriminator's output is synchronised to the *CompClock*, which may differ from the *Sclk* by a phase. The comparator features two threshold modes: in *track mode* the output is as long active as the input signal is above the threshold, in *pulse mode* the output is active for exactly one clock cycle. After the synchronisation stage the comparator's signal path is split into the prompt binary and the binary pipelined path. The

latter one includes additionally a level shifter which transforms the rail-to-rail logic levels (0/2.5 V) to 1.122 V resp. 1.346 V. This matches the dynamic range of the pipeline and the pipeamp. Each channel can be masked, so that it does not contribute to the further signal processing. The 128 mask bits are accessible via a shift register (cf. section 4.4.7).

4.4.3 Pipeline and Pipeline Readout Amplifier

The pipeline is a switched capacitor array of 130 × 187 cells[13] working as a ring buffer. The number of rows is made up by the 128 channels, one test channel and one common-mode sense channel (cf. fig. 4.9). The number of columns is given by the maximum trigger latency of 160 sampling intervals, the integrated trigger buffer of 16 stages plus a logic overhead of 17 intervals ($187 = 160 + 16 + ((\frac{16}{2} + 1) + 1) + 1$). Section 4.4.7 details the derivation of the pipeline depth. Each cell consists of two NMOS port transistors and a MOS capacitor (MOSCAP) using the gate-source capacitance of an NMOS transistor. Figure 4.18 depicts the schematic of a storage cell.

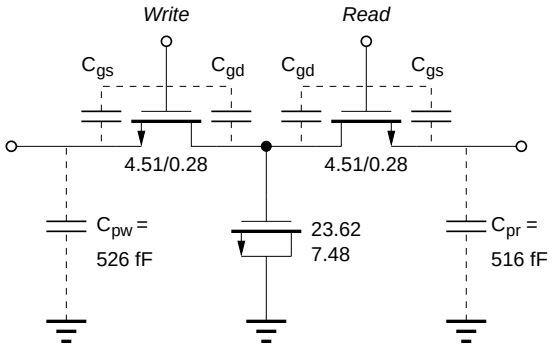


Figure 4.18: Schematic of a pipeline cell.

The layout principle of the pipeline is demonstrated in fig. 4.19. Two neighbouring rows are flipped with respect to each other. This ensures, that the input and output lines of one channel which are shared by all columns are maximally separated. The input resp. output lines of two adjacent channels are located close together and separated from the other type of line by the storage capacitance. This configuration reduces the possibility of cross talk from the input to the output line or vice versa.

MOS Capacitance

The gate-source capacitance of a transistor is not constant but depends on the voltage across its nodes. The capacitance C between gate and source/drain can be regarded as the series of the gate oxide capacitance C_{ox} and the capacitance of the diffusion layer C_D underneath the gate. Depending on the voltage across the nodes a depletion or inversion layer builds up.

Figure 4.20 shows the voltage dependency, the so-called $C-V$-*curve*, of the NMOS capacitor used as storage device in the pipeline. Three regions can be distinguished: in the *accumulation* region electrons are swept out of the gate region and holes are accumulated. In the *depletion* region all mobile charge carriers are removed underneath the gate and a depletion layer is

[13] (129 × 186) in case of *Beetle1.0* and (130 × 186) in case of *Beetle1.1*.

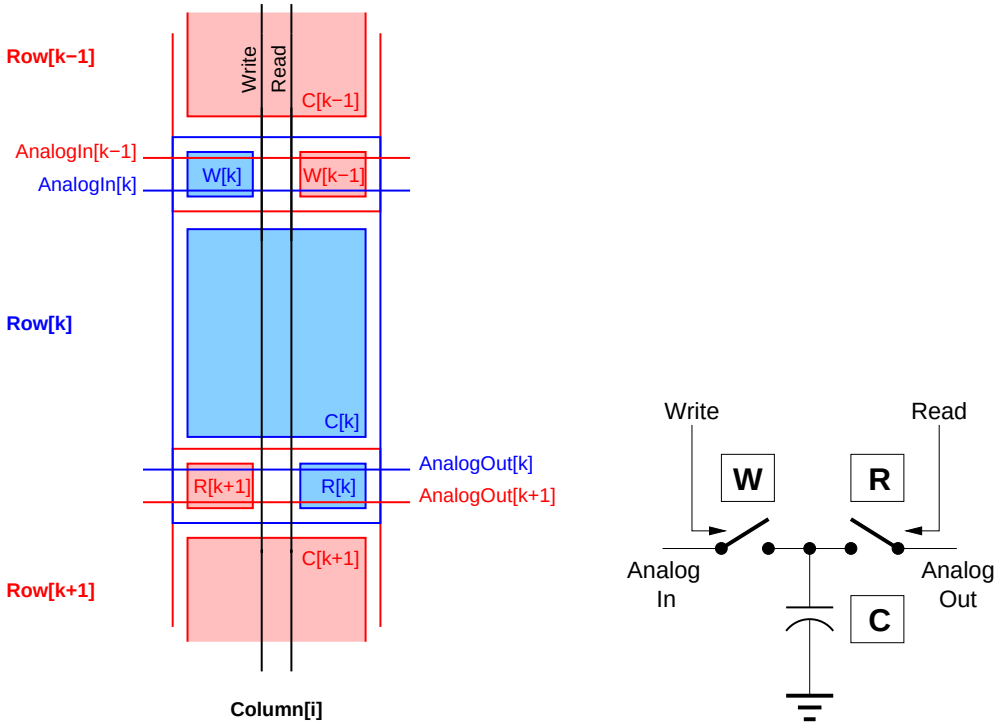


Figure 4.19: Layout principle of the pipeline. One storage cell with the adjacent cells in the same column is shown. The schematic clarifies the legend.

created. This results in a decrease of the total capacitance. For $V_g - V_s > V_{th}$ the MOSCAP is operated in the *inversion* region, where an inversion layer exists. The voltage dependence of the total capacitance C per unit area is given by [Gre86]

$$C = C_{ox} \parallel C_D = \frac{C_{ox}C_D}{C_{ox} + C_D} = C_{ox}\frac{1}{\sqrt{1 - \frac{2\epsilon_{ox}^2(V_g - V_s)}{q \cdot n_D \cdot \epsilon_{Si} \cdot t_{ox}^2}}} \quad [\frac{F}{cm^2}]. \tag{4.16}$$

The NMOS capacitor of a pipeline cell operates in the inversion region. The DC operating point corresponds to the DC offset of the front-end resp. comparator and is about 1.1 V.

It is desirable to use voltage-independent capacitors like poly(silicon)-poly(silicon) or metal-metal capacitors. In the used process technology metal-metal capacitors (MIMCAP) are available, which are formed by the second routing metal layer (M2) and a special metal layer dedicated to capacitors (Q2). The technology design rules restrict the total Q2 area to a certain limit which would have been exceeded with a pipeline using metal-metal capacitors. The advantage of MOS capacitors is their high capacitance per unit area of C_{ox}=5.56 fF/μm^2 compared to $\approx$ 0.7 fF/μm^2 of MIMCAPs which allows a compact cell layout.

MOS Switch

MOS transistors operated as switches differ from ideal switches in three effects: charge injection, clock feedthrough and a finite on-resistance. Associated with the on-resistance is a thermal noise contribution. *Charge injection* occurs when the switch is turned off. The charge of the conductive transistor channel is removed and collected on the source and drain. *Clock*

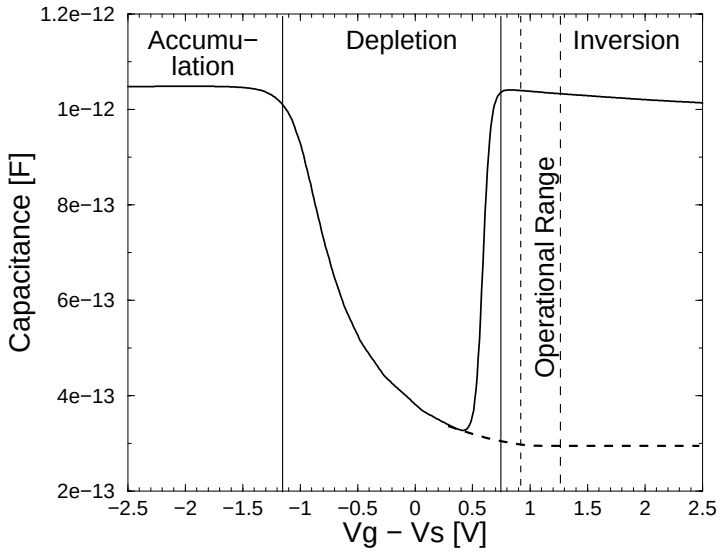


Figure 4.20: Low frequency capacitance-voltage dependency of the NMOS capacitor used in the pipeline cells. The dashed curve indicates the high-frequency behaviour described by eq. 4.16. The operational range is indicated by dashed lines.

feedthrough is an effect due to the existing gate-source resp. gate-drain overlap capacitances (C_{gs}, C_{gd}) (cf. fig. 4.18). The signal at the gate electrode couples through this parasitic capacitances to the other nodes of the switch. Usually transistors with minimum dimensions are used as switches. The overlap capacitances for this minimum size devices are small ($\sim 10\,\mathrm{fF}$). Also the *on-resistance* can be kept small ($\sim 500\,\Omega$) using short channel transistors.

Several compensation techniques exist which minimise the effect of charge injection.

- Dummy device
  Shorted transistors with half the gate area of the primary switch are controlled with the inverted clock. At the time when the primary switch is opened and releases Q/2 of its channel charge Q to each of its nodes the dummy transistor is closed and absorbs this charge.

- Complementary switch (also called CMOS-switch or transmission gate)
  An NMOS and PMOS transistor are put in parallel and operated with opposite clock signals. One MOSFET compensates the charge injection of the other. This scheme also reduces the voltage drop across the switch and increases the dynamic range.

Except the switches in the pipeline which are single-transistor devices, all switches in the *Beetle* chip use a combination of the above mentioned techniques: complementary transistors with shorted transistors on each node. An example schematic is shown in fig. 4.23.

Pipeamp

To access the information stored in a pipeline cell, two major configurations are possible:

- voltage readout
  The voltage across the pipeline capacitance is amplified with a (voltage) amplifier and directly fed into the multiplexer. This scheme has the disadvantage of charge division between the storage and the parasitic capacitance of the read line.

- charge readout
  A CSA retrieves the stored charge. The CSA output voltage depends only on the feedback capacitance.

The *Beetle* implements a charge readout of the pipeline. The pipeamp is a resetable charge sensitive amplifier which is AC-coupled to the pipeline. It retrieves the charge from the pipeline storage capacitor and transfers it to the multiplexer's hold capacitor (see fig. 4.21). The track-and-hold stage guarantees the *same* integration time for *all* channels. Unlike the preamplifier and the shaper which are continuously operated using a feedback resistance, the pipeamp is set to its operation point by a switch. If a readout is triggered, the reset is released for five clock cycles. After one pause cycle the pipeline read switch is closed (*Read* = 1), which enables the charge transfer to the amplifier. Three clock cycles later (= 75 ns) the output voltage is sampled on the multiplexer's input capacitance (*Track/Hold* = 0)[14]. The pipeamp is reset in between two pipeline readouts to avoid a shift in the DC operation point due to leakage currents. As can be seen from fig. 4.22 the pipeamp's risetime is constrained to 75 ns.

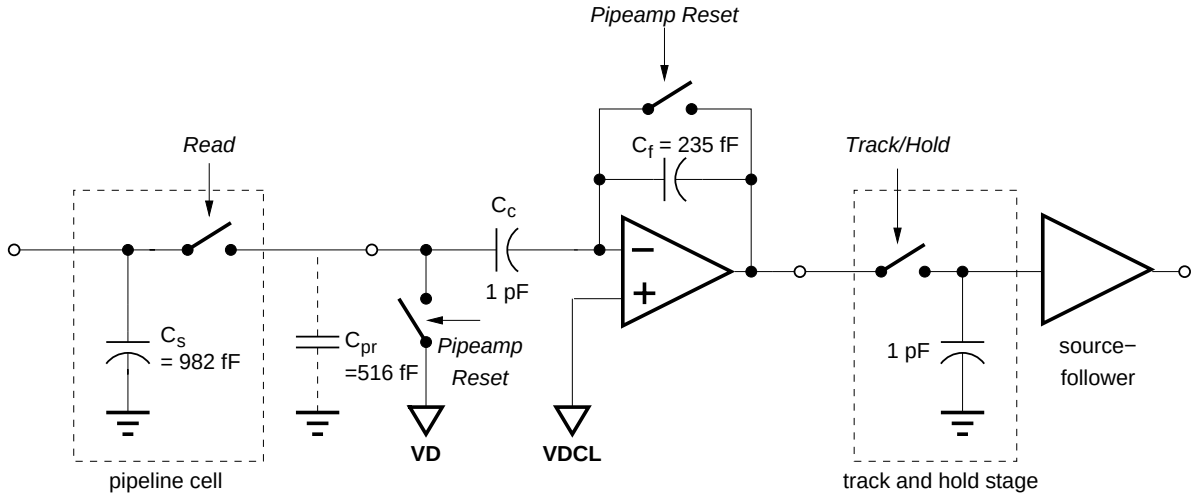


Figure 4.21: Schematic of the pipeline readout amplifier with a corresponding pipeline cell and the subsequent track and hold stage of the multiplexer. The pipeamp's core is detailed in fig. 4.24. The detailed schematic of the switches is shown in fig. 4.23.

The pipeamp's core is also a *folded cascode* (cf. section 4.4.1). The detailed schematic is given in fig. 4.24. For biasing the amplifier one current and two voltages are needed. The `Vd`

[14]The multiplexer is switched back to track mode (*Track/Hold* = 1) after finishing the serialisation of the 128 channels, i.e. nominally after 800 ns (cf. section 4.4.4).

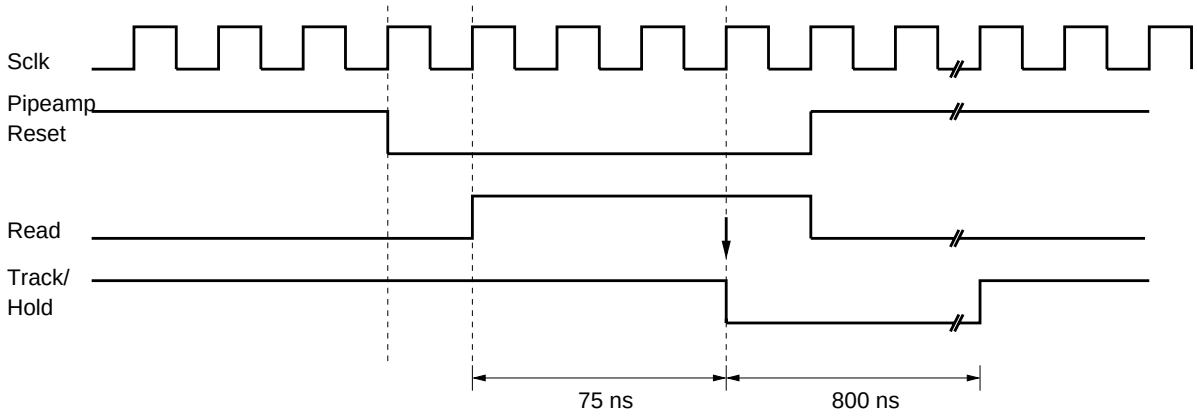


Figure 4.22: Timing sequence of the readout control signals. The arrow indicates the sampling point of the pipeamp's output. The time intervals correspond to the case of nominal LHCb readout speed, i.e. $Rclk = Sclk = 40\,\mathrm{MHz}$.

bias voltage represents the DC potential of the pipeline read line which is identical to the front-end's output DC-offset. The pipeamp is reset in between two readout sequences to this potential to avoid a drift of the operation point due to leakage currents. The `Vdcl` bias voltage works as the non-inverting input of the CSA. It shifts the operating point towards the dynamic range of the pipeline. Both voltages have to sink a current, i.e. they need to be buffered. For the `Vd` voltage this is done for all 130 channels in common, the `Vdcl` node is buffered in each channel separately. Source followers are used for this.

Fig. 4.25 shows the transient output response of the pipeamp to input signals in a range of $\pm 10\,\mathrm{MIP}$ ($= \pm 110{,}000\ e^-$).

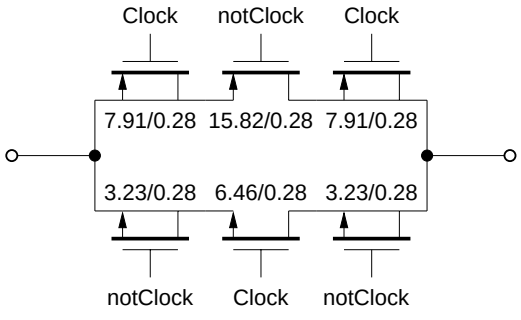


Figure 4.23: Schematic of the pipeamp's reset and multiplexer's track-and-hold switch.

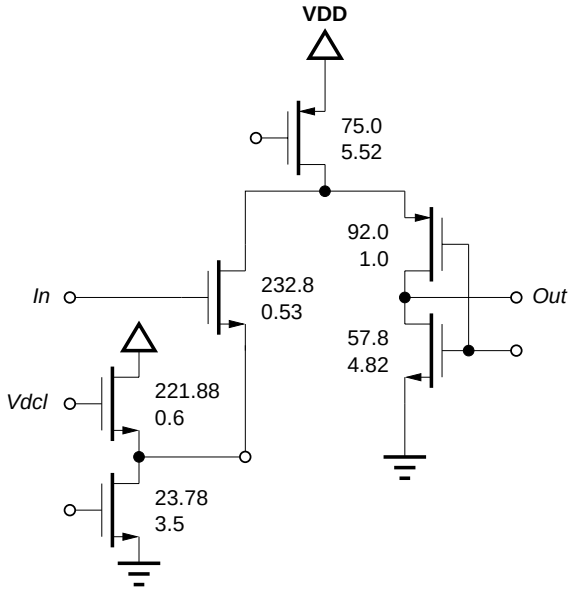


Figure 4.24: Amplifier core of the pipeamp.

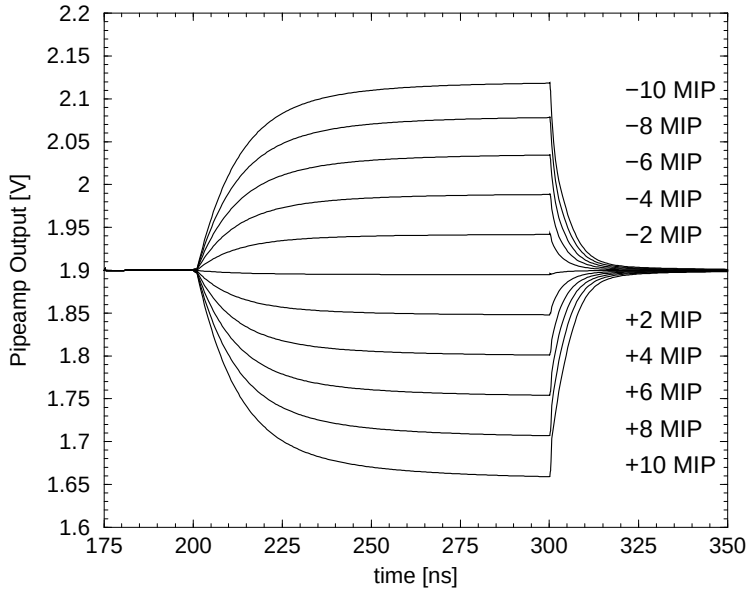


Figure 4.25: Transient simulation output of the pipeamp. The range of the input charge is ± 10 MIP=$\pm$110,000 e^-.

4.4.4 Multiplexer

The multiplexer has been originally designed by *E. Sexauer* and substantially improved by *S. Löchner*. It's task is the serialisation of the 128 parallel channels. It operates with the readout clock (*Rclk*) which is at maximum equal to the sampling clock, i.e. 40 MHz. The time for bringing the signals of one triggered bunch-crossing off chip is limited by the LHCb experiment to 900 ns (cf. section 4.2). Using the *nominal data rate*, i.e. running with a clock frequency of 40 MHz and transmitting data synchronous to one edge of the clock, limits the serialisation factor to 32 (32×25 ns $= 800$ ns). An increase by a factor of 2 at the same clock frequency can be obtained using *double data rate*, i.e. transferring data synchronous to both clock edges with effectively 80 MHz.

The multiplexer provides three operation modes:

- analogue mode
  4 ports are running in parallel, each carrying 32 channels. The readout works with nominal data rate and needs 800 ns. This is the analogue option for the VELO and inner tracker detectors.

- Binary mode
  2 ports are running in parallel, each carrying 64 channels. The readout works with double data rate and needs 800 ns. This is the operation mode for RICH's MaPMT option.

- Test mode
  1 port is carrying 128 channels. The readout lasts 3.2 μs. This mode is for applications with less demanding readout speed requirements or the need for a minimum number of output lines.

The multiplexer's internal structure reflects the modes of operation. The schematic diagram is depicted in fig. 4.26. Groups of 32 input channels are first serialised onto one of four internal buses which are then multiplexed depending on the readout mode onto 4, 2 or 1 output ports. The output of the predecessor stage (pipeamp) is sampled onto a capacitance and buffered by a source follower. The multiplexing onto the internal 32 channel bus is controlled by the output of a flip-flop. The flip-flops of all 128 channels form a shift-register. The control bit (*ReadBit*) is shifted with the *Rclk* from channel to channel. The source follower is necessary to drive the capacitive load of the 32 channel bus line and the switches of the other channels contributing to the same bus ($C_p = C_b + 31 \times C_{sw} = 157\,\text{fF} + 31\times\ 9.6\,\text{fF} = 455\,\text{fF}$).

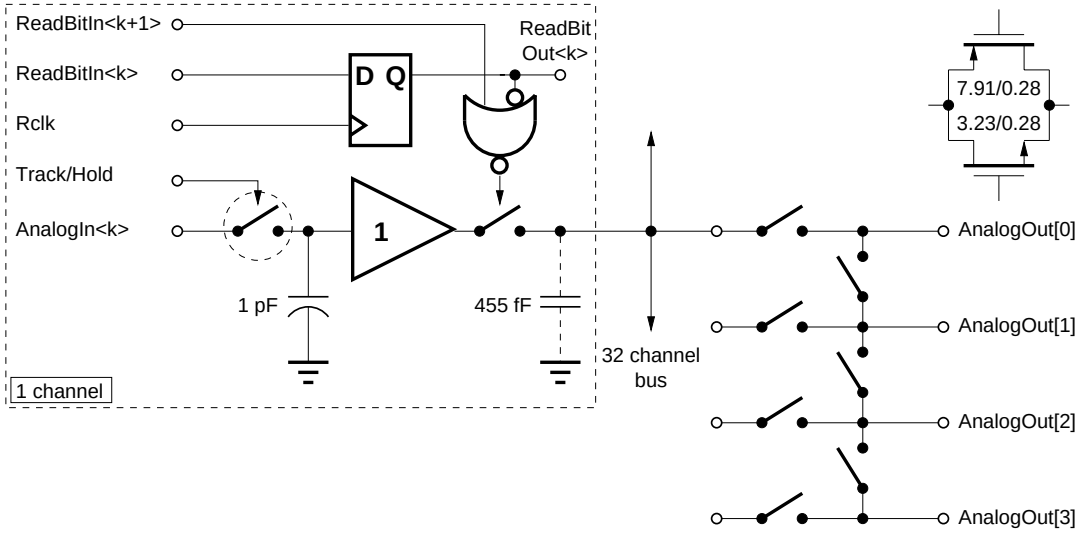


Figure 4.26: Schematic diagram of the multiplexer. The encircled switch symbol represents a complementary switch with dummy transistors on both source and drain (detailed schematic is shown in fig. 4.23), the other switches are standard transmission gates as depicted at the top.

Special care has been taken concerning charge injection of the switches. Complementary switches with dummy transistors on both source and drain are used (see section 4.4.3). The switching action between neighbouring channels is controlled in such a way, that opening a switch takes place at the same time when closing the switch of the subsequent channel. This is achieved by ORing the *ReadBitIn* bits of adjacent channels (cf. fig. 4.26). The channel charge released by the opening switch is absorbed by the closing one since the switches are connected via the 32 channel bus.

The readout mode and -speed is controlled via the registers *ROCtrl* and *RclkDivider* (see appendices A and B for details).

4.4.5 Output Buffer

The output buffer (designed by *H. Verkooijen* and *S. Löchner*) has to drive the *Beetle*'s output signals to the successive electronic stage in the readout chain. This is usually an analogue-to-digital converter (ADC). In case of the VELO it is located about 1 m from the *Beetle* chip, in case of the inner tracker detector about 5 m [Ste02]. If reading out the RICH detector, binary

signals are transmitted, which are detected by a standard LVDS receiver in a few cm distance. Hence, the output buffer features two modes of operation: in *analogue mode* a fully differential transconductance amplifier (OTA) puts the data off chip, in *binary mode* a transmitter meeting the LVDS standard is used. In both cases a current is delivered which has the advantage of a reduced power consumption compared to a voltage amplifier. Also from the circuit's stability point of view a current amplifier is preferable since it is not sensitive to high capacitive loads. The circuit schematic is given in fig. 4.27. The design makes intensive use of NMOS transistors with a threshold voltage close to 0 V ($\approx$ 10 mV). They allow a large signal swing or dynamic range.

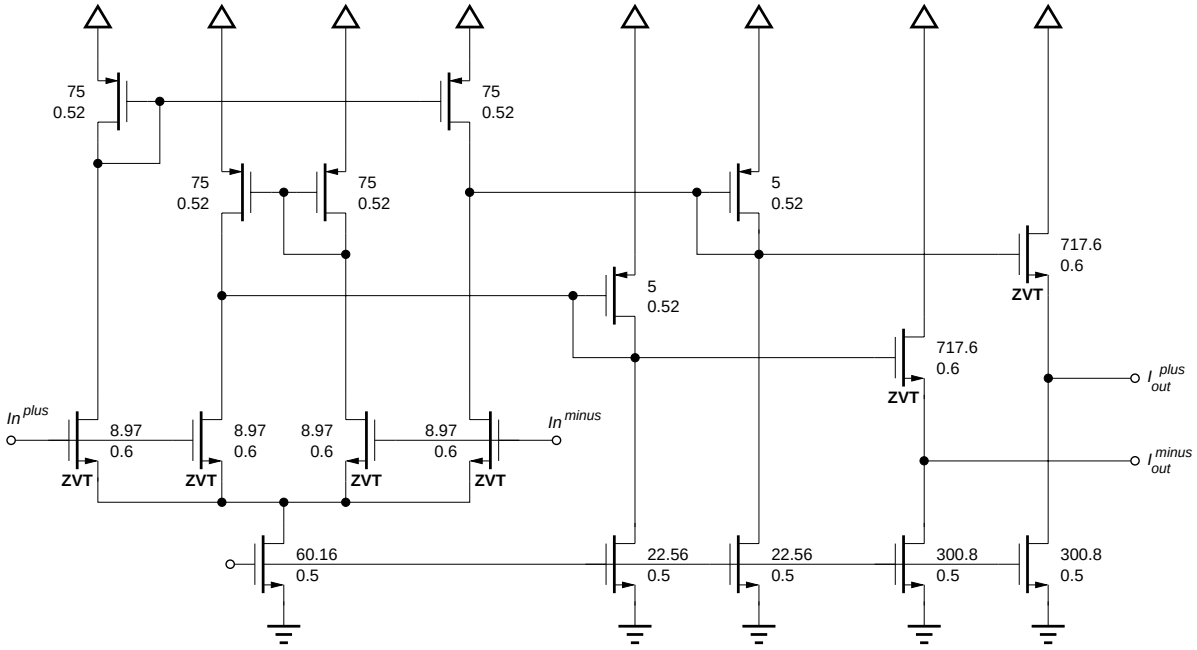


Figure 4.27: Schematic of the fully differential current output driver. The NMOS transistors carrying the label *ZVT* have a threshold voltage close to 0 V ($\approx$ 10 mV).

4.4.6 Bias Generators

In large systems like high energy physics experiments with thousands of readout chips it is difficult to provide a high number of stable and adjustable bias currents and voltages. Therefore it is desirable to generate them on-chip. The basic requirements are

- stability: temperature variations and irradiation damage effects should be compensated by an adequate circuit design,
- linearity: in between the required dynamic range (at maximum rail-to-rail) the output should be linear,
- resolution: most demanding is the comparator threshold level of 7.9 μA/LSB. All other stages do not require a resolution of a few LSB.

For biasing the *Beetle*'s analogue stages 11 currents and 5 voltages are needed. They are generated on-chip by 8-bit digital-to-analogue converters (designed by *N. Smale* [Sma03]). The digital inputs are controlled by registers accessible via the I^2C-interface.

Current Source

The integrated current source provides the necessary reference current for the current DACs. It uses a *regulated cascode* configuration (fig. 4.28). The nominal output current is 126.2 μA. The regulated cascode current source performs a very high output resistance which is given by[15] [Gei90]

$$R_o \simeq r_{ds2} \cdot \frac{g_{m1} g_{m4}}{g_{ds1}(g_{ds4} + g_3)}. \tag{4.17}$$

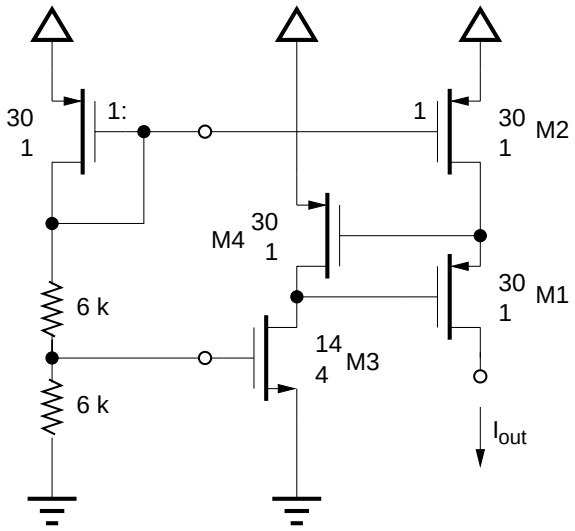


Figure 4.28: Regulated cascode current source. The 6 kΩ resistors are made of polysilicon.

The cascode is formed by the transistors M1 and M2, with M2 being the active load of M1. The feedback loop consisting of M1, M4 and M3 stabilises the drain-source voltage of the load transistor M2 and thus increases the AC output resistance of M2. M3 and M4 are forming a (common-source) amplifier, while M1 works as source-follower. The branch with the diode-connected PMOS transistor and the two 6 kΩ polysilicon resistors biases the transistors M2 and M3 in the saturation region.

Current DAC

The current DAC consists of binary-weighted current sources which are formed by PMOS transistors operated in the ohmic region. Figure 4.29 depicts the principle schematic. The label m at the transistor symbols denotes the multiplicity, i.e. the number of devices connected in parallel. The output current is the sum of the binary weighted PMOS drain-source currents. The transistor gates are switched between the positive supply voltage (OFF state) and a reference voltage V_{ref} of 1.293 V (ON state) which biases the PMOS transistor in the ohmic

[15] if all transistors operate in the saturation region and neglecting bulk effects

region. V_{ref} is derived from the current source's output current by a current mirror. In total 256 ($= 1 + \sum_{i=0}^{7} 2^i$) transistors with identical dimensions (W/L = 1.28/1.52) are used. They are arranged in the layout in a *"common centroid"* configuration. Hereby, the devices are placed in the geometrical centre of identical neighbours. This homogeneous structure guarantees a good matching. The transistor in fig. 4.29 with its gate fixed to the positive supply voltage is only present for a layout reason, namely to complete the "common centroid" arrangement.

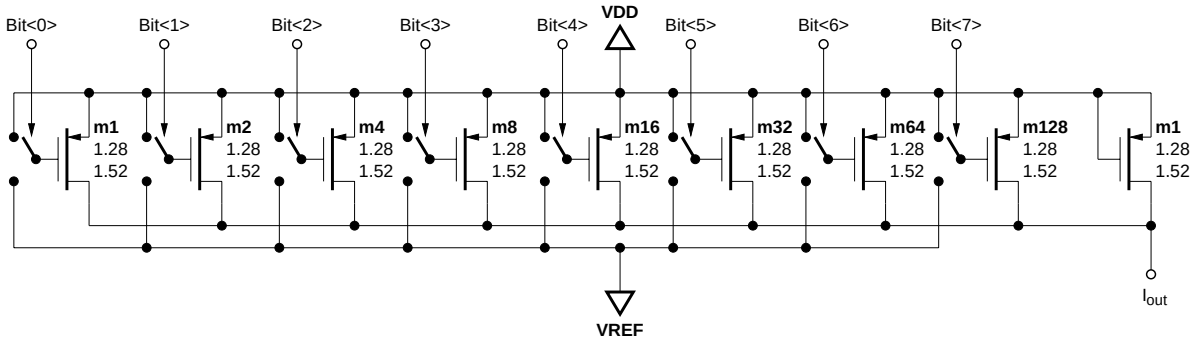


Figure 4.29: Principle schematic of the current digital-to-analogue converter. The label m at the transistor symbols denotes the multiplicity, i.e. the number of devices connected in parallel. The voltage V_{ref} is derived from the current source's output current by a current mirror.

The maximum output current of the DAC is linked with the on-chip current source and amounts to 2.03 mA. The differential non-linearity (DNL) has been measured on the test chip *BeetleBG1.0* as 7 μA [Sex01] which corresponds to 0.9 LSB. The DAC under test had a width of 10 bits. Concerning the differential non-linearity, the result can be transferred to the 8-bit version, since the 2 chopped LSBs do not contribute to the DNL.

Voltage DAC

The voltage DACs use a *R-2R ladder* configuration (see fig. 4.30). The resistor chain connected between the power supplies (at the left side of fig. 4.30) is equivalent to a voltage source of $V_{dd}/2$ with an output resistance of R. Together with the series resistor R and the 2 resistors connected to the node V_0 this forms a voltage divider of factor 2. V_0 being 0 V results in a voltage at node V_{n0} of $\frac{V_{dd}/2}{2} = \frac{V_{dd}}{4}$. For $V_0 = V_{dd}$, V_{n0} is given by $\frac{V_{dd}}{2} + \frac{V_{dd}/2}{2} = \frac{3}{4}V_{dd}$. In general it is

$$V_{nk} = \begin{cases} \frac{V_{n(k-1)}}{2} & \text{for } V_k = 0\,V \\ \frac{V_{n(k-1)}}{2} + V_{n(k-1)} = \frac{3}{2}V_{n(k-1)} & \text{for } V_k = V_{dd} \end{cases} \tag{4.18}$$

The output voltage as a function of the applied binary 8-bit number is then given by

$$V_{out} = \frac{V_{dd}}{2^{n+1}} \cdot (1 + \frac{1}{V_{dd}} \sum_{i=0}^{n-1} 2^{i+1} V_i) = \frac{2.5\,V}{2^{8+1}} \cdot (1 + \frac{1}{2.5\,V} \sum_{i=0}^{7} 2^{i+1} V_i) = 4.88\,mV \cdot (1 + \frac{1}{2.5\,V} \sum_{i=0}^{7} 2^{i+1} V_i), \tag{4.19}$$

where
n=8 is the resolution,
i=0 represents the least significant bit (LSB),

i=7 represents the most significant bit (MSB),
V_i is the voltage associated with the ith bit: V_i=0 V resp. 2.5 V for the ith bit = 0 resp. 1.

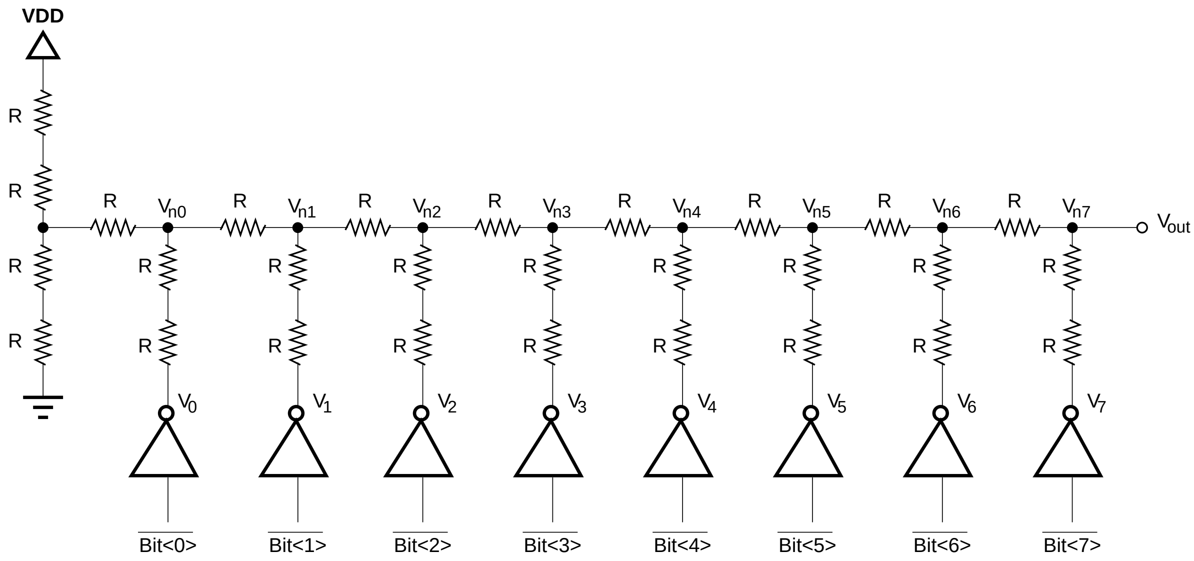


Figure 4.30: Schematic of the voltage digital-to-analogue converter. The value of the resistor is 8.5 kΩ.

The resistors are made of non-silicided[16] polysilicon which has a sheet resistance of $R_\square = \frac{R}{\square} \approx 210\,\frac{\Omega}{\square}$. The 28 identical polysilicon resistors are placed in the layout in a *"common centroid"* arrangement. The advantage of the R-2R configuration compared to a binary-weighted DAC is, that only resistors with a ratio of 2:1 are used which is more practical to accomplish. The binary-weighted resistor ladder configuration has the disadvantage of a large ratio of component values. The ratio of the MSB resistor to the LSB one is $R_{MSB}/R_{LSB} = 2^{-(n-1)}$. For a 8-bit DAC this is 1/128 which means that R_{MSB} has to have a relative accuracy with respect to R_{LSB} of ± 0.78%. The process variations of polysilicon resistors are in the order of 20%.

The dynamic range of the voltage DAC is rail-to-rail, i.e. 2.5 V, with a negligible offset error. The resolution amounts 9.8 mV, while the differential non-linearity has been measured on the test chip *BeetleBG1.0* as 11 mV [Sex01] which corresponds to about 1.1 LSB. The DAC under test had a width of 10 bits. Concerning the differential non-linearity, the result can be transferred to the 8-bit version, since the 2 chopped LSBs do not contribute to the DNL. The source of the non-linearity is the output resistance of the inverters, which load the "2R"-branches of the resistor ladder.

4.4.7 Control Logic

The digital circuitry can be classified into two parts according to the used *clock*: the *slow control* works within the I^{2}C-clock domain with about 100 kHz implementing the programming interface with the corresponding decoders for accessing the registers. The *fast control* is running in the sampling clock domain with 40 MHz and handles the storage and readout of an event.

[16] A silicide is an alloy of silicon and metal, e.g. $TiSi_2$ or $CoSi_2$.

Both parts are also separated in the layout of the chip (cf. fig. 4.11). Fig. 4.31 summarises the hierarchy levels of the *Beetle*'s control logic. The modules carrying the label 'H' are adapted from the HELIX128 readout chip [Fal98, Tru00] (cf. section 4.5) and only slightly modified.

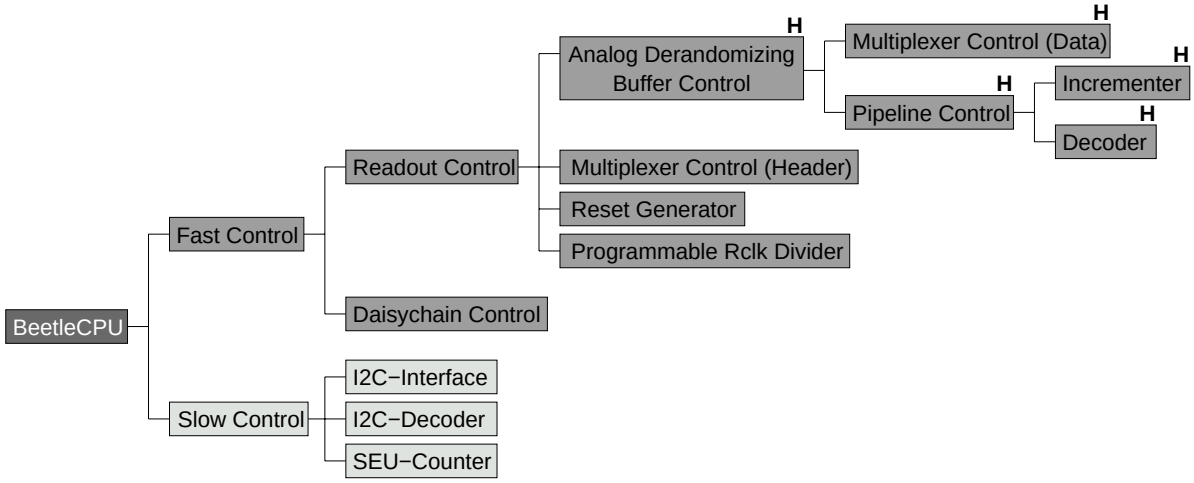


Figure 4.31: Hierarchy levels of the *Beetle* control logic. The modules carrying the label 'H' are adapted from the HELIX128 readout chip.

The logic functionality is described within the hardware description language (HDL) *Verilog*[17] [Tho96]. The complete logic is synthesised, i.e. the schematic is generated automatically based on the HDL description, using the *Synopsys* [Syn00] software. The placement and routing of the logic standard cells[18] is done with *Silicon Ensemble* [SE].

Slow Control

The chip's programming interface meets the I^2C-standard[19] [Phi95]. The I^2C-bus is a synchronous, serial system with two *bidirectional* wires, serial data (SDA) and serial clock (SCL). Data is transferred synchronous to the clock. The two bus lines are connected with pull-up resistors to a positive supply voltage. The bus performs a wired-AND connection of its participants. The output stages of the bus devices must therefore have open-drain or open-collector output stages. A device on the bus is accessed via an unique address which can be either 7 or 10 bits wide[20]. Beside this individual access a broadcast mode (called *general call*) is possible, where all devices on the bus are written simultaneously. Data is transferred with the most

[17] At first, the logic circuitry was described (pipeline control by N. Smale [Sma03]) within *VHDL* (Very High Speed Integrated Circuit HDL) [Leh98]. This was motivated by the plan to integrate a model of the *Beetle* into an overall simulation of the LHCb L0 and L1 readout system [Chr99] which is also modelled with *VHDL*. The fact, that the pipeline control circuitry based on the *VHDL* description consumed about a factor 2 more area gave preference to the *Verilog* based circuit description. An investigation of the reason for the difference in area consumption has not been undertaken due to a lack of time.

[18] The *layout* of logic library cells is standardised: the gate area is a multiple of a unit cell which allows an automated placement. The in- and outputs of the cells have defined connectivity layers and access directions which enables a software aided routing between the cells.

[19] I^2C= Inter Integrated Circuits

[20] The 7 bit address space has 112 entries (8...119), the 10 bit address space 1024 entries (0...1023).

significant bit (MSB) first in frames of 8 bits. After each frame the receiver device has to acknowledge the transfer with one dedicated bit.

The *Beetle*'s interface is a *standard mode I^2C-slave* device performing a transfer rate of 100 kbit/s and operating in the 7-bit address space. This allows to access the chip with a commercially available interface.

A register access is controlled by two decoders, one for writing resp. reading. They use an address pointer featuring a *self-incrementing* function: the pointer register contains the address of the register to be written or read first. After each transferred data frame the address pointer is internally incremented by one. This allows the consecutive access to registers with adjacent addresses. The pointer register itself remains unchanged, i.e. a new transfer will start at the same pointer position (see appendices A and B for a more detailed description).

Fig. 4.32 shows the transfer sequences for a write and read access. Each 8 bit frame is followed by an acknowledge bit (A). After the initialisation of the bus (S) by the bus master the chip's address with a bit (R/$\overline{W}$) indicating the transfer direction is transmitted followed by the pointer byte and the data. In write mode the pointer byte has to join indispensablely, followed by the data. After the transfer of one data frame, the pointer addresses the successive register because of its self-incrementing function. The transfer is terminated again by the master (P). In read mode two possibilities exist:

- Preset pointer
  After initialising the transfer and sending the chip address with the corresponding direction bit for reading (R/$\overline{W}$ = 1), data is immediately read out. The address pointer has been set in a previous transfer.

- Pointer set followed by immediate readout
  After initialising the transfer and sending the chip address, the pointer byte is transmitted. The I^2C-bus is re-initialised (Sr), the chip address is sent and data is read out.

The broadcast mode (general call addressing) is only possible when writing to the registers. In this mode the slave address '0' is transmitted followed by an additional byte, the pointer byte and the data (fig. 4.32). Provided, that several chips have to be written with the same data, the broadcast mode is a very useful tool in large systems.

The interface circuit is built up by an unidirectional shift register for the slave address (*AddrShiftReg*), a bidirectional one for data (*DataShiftReg*), a module generating (*AckGenerator*) and one checking (*AckChecker*) the acknowledge bits on the bus[21]. The module (*StartStopDetector*) senses the bus for transfer initialisation and termination. A handshake procedure (*StartHandshake*) sensitises the interface after an initialisation to a repeated start condition (Sr) on the bus. A finite state machine (FSM) (*Ctrl*) controls the previous mentioned modules. The corresponding state diagram is shown in fig. 4.33. The state transitions indicated by solid lines are synchronous to the (negative edge) of the clock (SCL), the dashed lines represent

[21]The acknowledge bit 'A' on the I^2C-bus can be high (*Not-Acknowledge*) or low (*Acknowledge*). In *write mode* the master-transmitter sets the SDA line to high after each 8-bit frame. The slave-receiver acknowledges by pulling down the line for one clock cycle. In *read mode* the situation is vice versa. The slave-transmitter sets SDA to high, while the master-receiver pulls the line down. A repeated-start- (Sr) or a stop-condition (P) is announced by the master-receiver by a *Not-Acknowledge*. Therefore the slave-transmitter has to check the acknowledge bits on the bus: depending on the acknowledge type it has either to apply the MSB of a new data frame (A = 0) or to set SDA to high (A = 1). The latter action allows the master-receiver to generate in the next clock cycle the corresponding control bit (Sr or P).

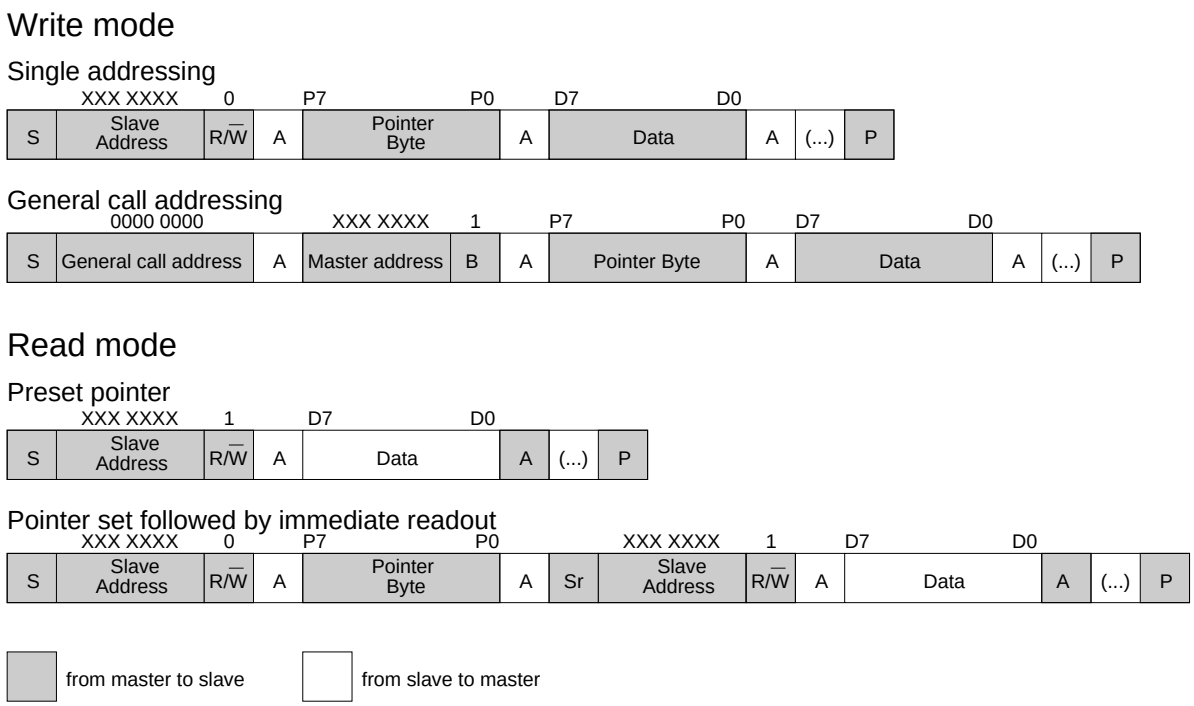


Figure 4.32: I^{2}C-transfer sequences for accessing the *Beetle* registers. Each transferred 8 bit frame is acknowledged by the slave (*Beetle)* with one bit (A).

asynchronous transitions. A chip-reset (`Reset`) initialises the FSM to the *idle* state (ID). The `Start` strobe (generated by module *StartStopDetector*) acts like a reset and asynchronously puts the state machine into state *read address* (RA) where the slave address is shifted in. After eight clock cycles the acknowledge bit is set in state *address acknowledge* (AA) to high or low depending if the transmitted address byte equals the chip address. If the chip has been addressed, it reads or sends data in state *read data* (RD) or *send data* (SD) resp. depending on the transfer direction bit R/$\overline{W}$. In case of not being addressed the FSM performs a transition to the *idle* state, in case of a *general call* the state GC is taken. After eight shift operations the corresponding acknowledge bit is generated (R/$\overline{W}$ = 0) in state *send acknowledge* (SA) or received (R/$\overline{W}$ = 1) in state *receive acknowledge* (RA). In the next clock cycle the state machine is back in state SD or RD to either shift another data byte or to remain there in case of a transfer termination. A new transfer will (asynchronously) 'reset' the FSM to state RA. In between a transfer initialisation and a termination a signal (*I2CBusy*) is generated which indicates a busy I^{2}C-bus. This signal is used to control the register access between the I^{2}C-interface and the SEU correction mechanism (see section 4.6).

The I^{2}C-decoders generate from the actual pointer address one write- and one read strobe (1 over N decoding). The configuration of a *Beetle* register is shown in fig. 4.35. The decoder's write strobe serves as register clock, the read strobe controls the tristate buffers[22]. The write- as well as the read decoder use a *gated* combinational 1 over N decoder core which is controlled by a FSM. The advantage of this decoding structure is the need for only one flip-flop namely

[22]A tristate buffer features *three* output levels: logic-low (L), logic-high (H) and high-ohmic (Z). The latter one allows a simple implementation of bidirectional lines.

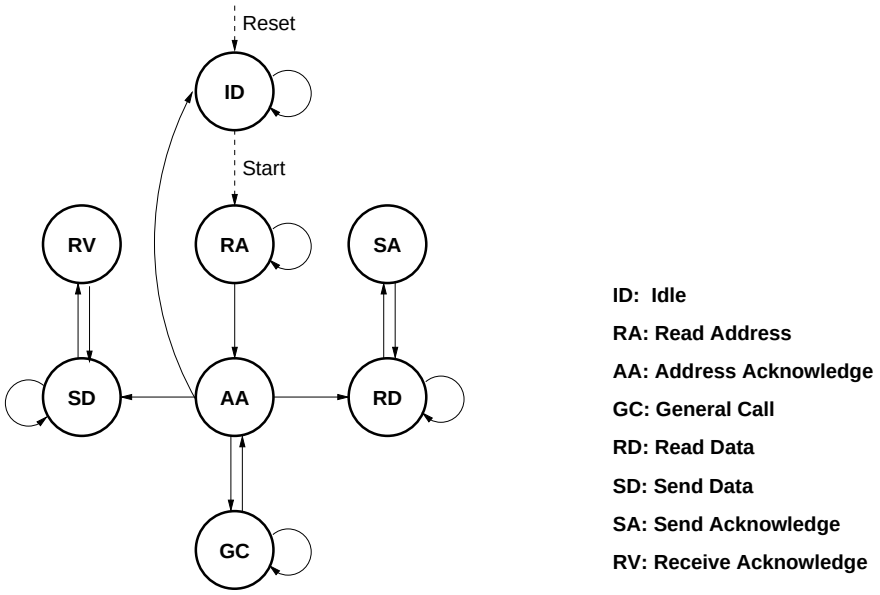


Figure 4.33: State diagram of the finite state machine *Ctrl* of *Beetle*'s interface circuit. The various states and branches are explained in the text. The state transitions indicated by solid lines are synchronous to the (negative edge) of the SCL clock, the dashed lines represent asynchronous transitions.

for the gate, independent of the decoder width. This minimises the number of bits sensitive to SEU, and simultaneously guarantees decoder output signals free of glitches. The state diagrams of the two decoder FSMs are depicted in fig. 4.34. The corresponding clock signals are generated by the I^2C-interface (module *Ctrl*). The write decoder is split in two parts operating at different clock edges.

Three registers on *Beetle1.2* (*TpSelect*, *CompMask*, *CompCtrl*) slightly differ from the configuration shown in fig. 4.35. They are operated as *shift registers*: a 128-bit register is segmented in 16 8-bit registers. A consecutive access to the corresponding register address shifts the data in 8-bit frames. The 8 MSBs of the 128-bit register are readable, which allows a verification of the shifted data.

Fast Control

The fast control circuit accomplishes three tasks: the *storage* of front-end or comparator signals in the pipeline, the *readout* of triggered events via pipeamp and multiplexer and the *control of a daisy chain* of several chips sharing their output lines.

In the following the basic operation principle of event storage and readout is explained. From the control logic's point of view the pipeline is an one-dimensional array of 187 columns[23], each controlled by a write and a read strobe. A *pipeline write pointer* references in each sampling clock cycle a certain column. The pointer address is decoded (1 over 187) and operates the write switches of the corresponding pipeline storage cells. A *pipeline trigger pointer* follows the write pointer in a fixed distance of *(latency+1)* columns. In this way, an incoming trigger

[23] 186 in case of *Beetle1.0* and *Beetle1.1*

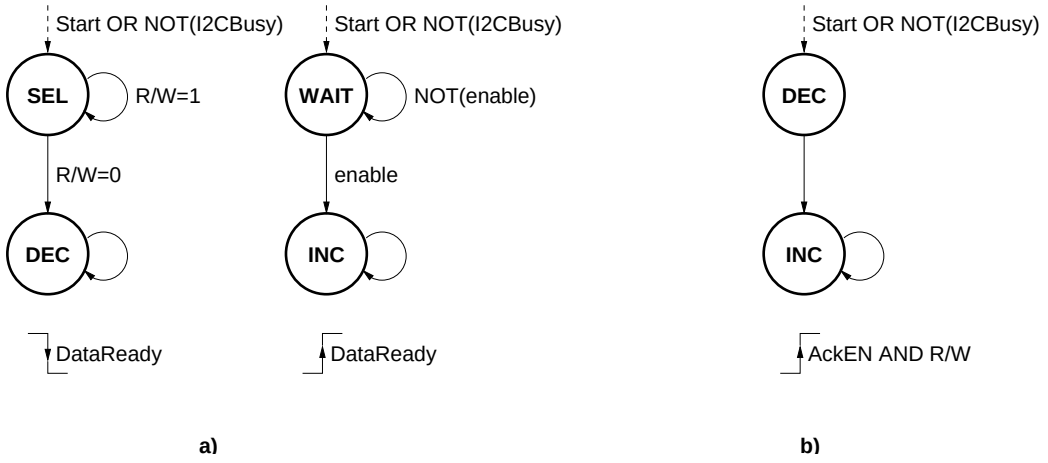


Figure 4.34: State diagram of the *WriteDecoder* (a) and *ReadDecoder* (b) FSM of *Beetle*'s interface circuit. The clocks are generated by the I^2C-interface (module *Ctrl*). The write decoder operates on both clock edges.

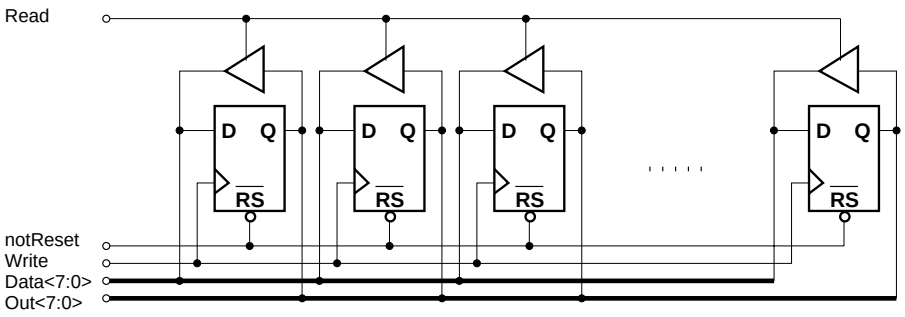


Figure 4.35: Configuration of a *Beetle* register. The triangular symbol represents a tristate buffer.

(which is delayed by *latency* clock cycles) references the corresponding event. Associated with the pipeline is a *derandomising trigger buffer*. It has 16 entries, each consisting of an 8-bit word for storing a pipeline address and three associated flag bits: write-inhibition bit (*WriteInh*), trigger-inhibition bit (*TrigInh*) and release-column bit (*RelCol*). Write and read operations to the derandomising buffer are performed in the order 'first-in first-out' (FIFO). The buffer entries are referenced by two FIFO pointers, a write and a read pointer (fig. 4.36).

An incoming trigger causes the following actions: the pipeline column number (PCN) referenced by the trigger pointer is stored in a free entry of the derandomising buffer addressed by the FIFO write pointer. The three associated flag bits are set (fig. 4.37 a). The write pointer skips during it's next passage the triggered column and prevents thereby the data from being overwritten. The trigger pointer also leaps over this pipeline location to preserve the latency, i.e. the distance between the two pipeline pointers. If no readout is executed and the FIFO read pointer references a buffer entry with the three flag bits set, the readout sequence is started (cf. fig. 4.22): the pipeline readout amplifier is released from it's reset state, the pipeline address stored in the corresponding FIFO entry is decoded and 1 out of 187 read strobes is operated.

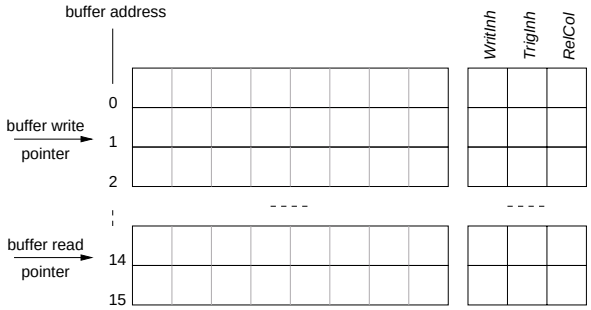


Figure 4.36: Principle of the derandomising trigger buffer. A write and a read pointer reference the buffer entries. Associated with each entry are three flag bits: write-inhibition bit (*WriteInh*), trigger-inhibition bit (*TrigInh*) and release-column bit (*RelCol*).

After the pipeamp's settling time the multiplexer's track-and-hold stage is switched to hold mode and the serialisation process is started.

At the end of a readout sequence the flag bits associated to a buffer entry are released gradually: first the write-inhibition bit is cleared (fig. 4.37 b), which means that data in the corresponding column can be overwritten during the next write pointer passage. Triggering this column at that time is still prohibited. Only when the write pointer has passed this column the trigger-inhibition bit is released (fig. 4.37 c). This prevents triggering data of previous bunch crossings. The release-column bit is cleared, if the return-token from the daisy chain has arrived (see below). This finally releases the column lock, clears the buffer entry and increments the FIFO read pointer. At this time the column can be triggered anew (fig. 4.37 d). The release-column flag needs not necessarily be cleared at last. In general, three cleared flag bits release the column lock.

In each clock cycle the pipeline write and trigger pointer need a valid address to reference in the next cycle. A simple address incrementing is not possible in general, since triggered columns result in prohibited addresses. Two modules, *Write-Incrementer* and *Trigger-Incrementer* (fig. 4.31) calculate new valid addresses for the write and trigger pointer respectively. Each clock cycle the *Incrementer* has to put out an address which is higher than the address of the last cycle but not equal to any prohibited address stored in the derandomising buffer. For a 160 columns deep pipeline and a FIFO of 16 stages, the probability to find a prohibited address is $16/160 = 1/10$. Hence it is sufficient to generate $1 + 1/10$, i.e. 2 new numbers per clock cycle. They are stored in a so-called *look-ahead buffer*, provided there are free entries. The depth of this buffer is determined by the situation of 16 consecutive triggers. With a depth n of the derandomising buffer, the depth of the look-ahead buffer is fixed to $((\frac{n}{2}+1)+1)$. A detailed derivation of this relation can be found in [Tru00]. The total depth of the pipeline is the sum of

- the maximum latency, i.e. 160 sampling intervals,
- the depth n of the derandomising trigger buffer, i.e. n=16 entries,
- the depth $((\frac{n}{2} + 1) + 1)$ of the pipeline look-ahead buffer, i.e. 10, and
- 1 clock cycle for trigger synchronisation.

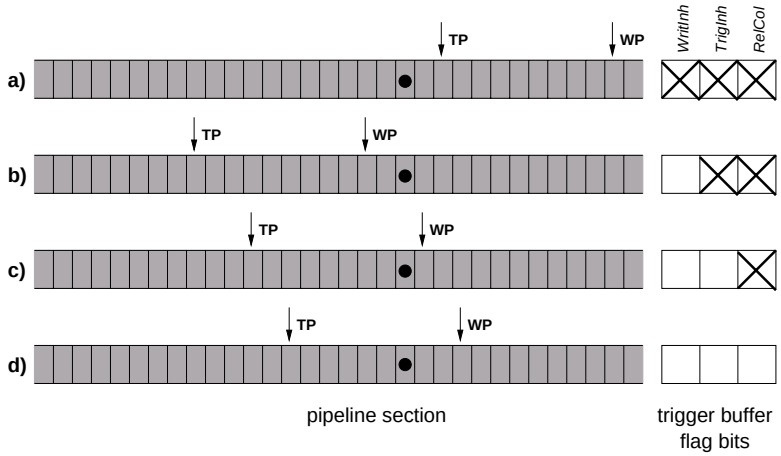


Figure 4.37: Correlation between the derandomising buffer's flag bits and the pipeline write (WP) and trigger pointer (TP). The filled circle should mark the triggered pipeline column. a) readout of triggered column is executed, b) readout sequence is finished but the write pointer has not yet passed the triggered column, c) write pointer has passed, so the corresponding column contains new data, d) release-column bit from daisy chain has arrived which enables triggering to this pipeline location.

The number of pipeline columns therefore calculates to $160 + 16 + ((\frac{16}{2} + 1) + 1) + 1 = 187$.

The (externally accessible) *FifoFull* signal indicates, that the *Beetle* cannot accept further triggers. This bit is the trigger-inhibition bit (*InhTrig*) referenced by the FIFO write pointer. If no further triggers can be accepted, the *InhTrig* bit of each FIFO entry is active. The FIFO write pointer references an active bit and so the *FifoFull* signal is active.

The passage of column number '0' of the pipeline write and trigger pointer is indicated by two signals *WriteMon* and *TrigMon*. They are externally accessible and allow a verification of the chip's latency, since their distance is *latency+1* clock cycles.

The daisy chain concept allows several chips to share their output lines. This is for applications which do not require a high readout speed but a minimum number of transmission lines. A chip can be configured via I^2C-bus to be the first (*DaisyFirst*), an intermediate or the last (*DaisyLast*) chip in the chain. The chain is formed by two paths: a token and a return-token path. The first chip in the chain starts it's readout on a trigger and sends a readout token to the successor chip in the chain after finishing the readout. All chips except the first start their readout sequence on an incoming token. The return path is necessary to keep synchronicity in the chain. The last chip sends a return-token which propagates through all chain elements. An incoming return-token releases the corresponding FIFO entry and enables a new readout. This happens simultaneously in all chips of the chain, beside some line propagation delays of a few ns. The length of the chain is only limited by the fact that the maximum return-token delay has to be less than one *Sclk* period, i.e. < 25 ns.

4.5 The Beetle Chip Family

The development of the *Beetle* chip started in late 1998 with two test chips implementing front-end amplifiers and biasing structures. It is based on the HELIX128 chip [Fal98, Tru00] used for the experiments HERA-*B* [Her95], ZEUS [Zeu] and HERMES [Her] at HERA[24]. The HELIX128 chip is fabricated in the AMS[25] 0.8 μm CMOS process. The *Beetle* gained a lot from the experience with the HELIX chip. Especially the control logic for event storage and readout has been adapted by the *Beetle.* Table 4.5 contrasts the two chips.

	HELIX128	*Beetle*
nom. sampling frequency	10 MHz	40 MHz
shaper peaking time	100 ns	25 ns
ENC	400 el. + 39.4 el./pF	450 el. + 47 el./pF
latency	128	160
trigger buffer depth	8	16
radiation tolerance	$\approx$ 400 krad	$>$ 10 Mrad
process technology	0.8 μm CMOS	0.25 μm CMOS
readout speed	20 MHz	40 MHz
readout time per event	$\geq$ 3.4 μs	$\geq$ 900 ns
daisy chained readout	yes	yes
comparator trigger signal	yes (open drain outputs)	yes (LVDS outputs)
binary pipelined path	no	yes
SEU protection	no	yes
standard interface	no	yes

Table 4.5: Comparison of the HELIX128 and *Beetle* readout chips.

The *Beetle* chip family has grown so far (end of 2002) to 3 members of readout chips (*Beetle1.0* - *Beetle1.2*) and 8 (2 $\times$ 2) mm^2 chips implementing test structures and prototype components. Table 4.6 lists all family members.

Front-end Developments

The central component on the *Beetle,* the analogue front-end, has gone through several iterations with in total 20 variations implemented on 4 test chips. The essential design parameters of the different front-end sets are put together in table 4.7. *BeetleFE1.0* integrates the sets 1,2 and 4, *BeetleFE1.1* the sets 2a-e and *BeetleFE1.2* the sets 5a-i and set 6. The various front-ends mainly differ in the type of input transistor, it's dimension and layout. Three different layout styles are used (see fig. 4.38): a *rectangular* shape of the gate, an *enclosed* gate structure and a gate forming a *waffle* pattern. An enclosed gate has the advantage of suppressing leakage currents (cf. section 3.2.2) in case of NMOS transistors and providing a maximum transconductance per junction area, whereas the waffle transistor has a large W/L per area and low series resistance for gate, source and drain.

[24] A derivation of the HELIX128 chip, the *CIPix* chip [Bau99, Löc98, Sta00], is used in the central inner proportional chamber (CIP) of the H1 experiment [H1].

[25] Austria Mikro Systeme

chip name	submission date	chip size [mm^2]	description
BeetleFE1.0	May 1999	2×2	front-end test chip
BeetleBG1.0	May 1999	2×2	bias generator test chip
Beetle1.0	April 2000	5.5×6.1	readout chip
BeetleCO1.0	April 2000	2×2	comparator test chip
BeetlePA1.0	April 2000	2×2	pipeamp test chip
BeetleMA1.0	April 2000	2×2	front-end test chip
Beetle1.1	March 2001	5.5×6.1	readout chip
BeetleFE1.1	May 2001	2×2	front-end test chip
BeetleFE1.2	May 2001	2×2	front-end test chip
BeetleSR1.0	May 2001	2×2	SEU robust test chip
Beetle1.2	April 2002	5.1×6.1	readout chip

Table 4.6: Members of the *Beetle* chip family.

The readout chips *Beetle1.0* and *Beetle1.1* implement front-end set 4. Measurements performed on this front-end [Bak01b] revealed a saturation of the preamplifier at input charge rates of $\approx 2\,\mathrm{nA}$ which is too small for the expected channel occupancies of the VELO ($I_{in} \approx 0.7\,\mathrm{nA}$) and inner tracker detector ($I_{in} \approx 4\,\mathrm{nA}$) of LHCb (cf. table 4.2). In addition, the front-end doesn't satisfy the required specifications on the pulse peaking time and pulse remainder in the next bunch crossing.

Beetle1.0

Beetle1.0 is the first prototype of a complete readout chip. It was submitted in April 2000. This chip version has to be patched, e.g. with a focused ion beam (FIB), to be functional. A layout error in a tristate buffer of the control circuitry prevents programming the chip via the I^{2}C-bus. The chip's internal data bus is permanently forced to logic 0. Due to a bug in the extraction software, this error was not discovered by the available checking tools. A focused ion beam patch has been applied to a single die [FEI]. The patch however enables only a write access to the chip. The chip registers cannot be read back. Fig. 4.39 shows the output signal of the patched die using the analogue pipelined readout path. All 128 channels are multiplexed on one port. The figure is an overlay of different events with input signals corresponding to 1, 2, 3, 4 and 7 MIPs applied to 7 single and a group of 4 adjacent channels of the chip. On the figure the different input levels are clearly visible on the group of 4 channels. The header is correctly encoded but has wrong voltage levels due to a bug in the multiplexer. The baseline variation has been reproduced in simulation (fig. 4.40) by introducing a resistive voltage divider network between the `Vdcl` nodes of the pipeline readout amplifier (cf. fig.4.9). The channel-to-channel resistance has been chosen to $100\,\mathrm{m}\Omega$, which corresponds to the resistance of the connecting metal line (*Metal-z*, $R_{\square}^{Mz} = 0.05\,\Omega$). The `Vdcl` node of all 128 channels is shorted, commonly buffered and externally blocked by a capacitor (nom. 100 nF). This is to avoid channel-to-channel variations due to mismatch. Any difference in the `Vdcl` potentials will be cancelled between the channels. Since the `Vdcl`-node sinks 90% of the pipeamp bias current, the baseline shift is due to a voltage drop on the common `Vdcl`-bias line.

name	preamplifier input FET			preamplifier feedback FET		shaper feedback cap.
	type	*layout*	*W/L*	*type*	*W/L*	
set 1	PMOS	rectangular	2004/0.28	PMOS	0.52/50.38	90 pF
set 2	PMOS	rectangular	4009/0.28	PMOS	0.52/50.38	48.8 pF
set 4	NMOS	enclosed	3737/0.42	PMOS	0.52/50.38	48.8 pF
set 2a-c	NMOS	enclosed	3744/0.42	PMOS	0.52/50.56,1,0.52	49.7 pF
set 2d-e	NMOS	enclosed	3744/0.42	PMOS	0.52/1,0.52	20.6 pF
set 5a	PMOS	waffle	8310/0.28	PMOS	0.52/50	15.0 pF
set 5b	PMOS	waffle	8310/0.28	PMOS	0.52/50	18.75 pF
set 5c	PMOS	waffle	8310/0.28	PMOS	0.52/50	37.5 pF
set 5d	PMOS	waffle	7123/0.28	PMOS	0.52/50	18.75 pF
set 5e	PMOS	waffle	7123/0.28	PMOS	0.52/50	37.5 pF
set 5f	PMOS	rectangular	5852/0.28	PMOS	0.52/50	18.75 pF
set 5g	PMOS	rectangular	5852/0.28	PMOS	0.52/50	37.5 pF
set 5h	PMOS	waffle	5936/0.28	PMOS	0.52/50	18.75 pF
set 5i	PMOS	waffle	5936/0.28	PMOS	0.52/50	37.5 pF
set 6a	NMOS	enclosed	3667/0.42	NMOS	0.52/50	48.8 pF
set 6b	NMOS	enclosed	3667/0.42	NMOS	4.24/404.48	48.8 pF

Table 4.7: Overview of the essential design parameters of the various *Beetle* front-ends.

The reduction of the signal gain by about a factor 4 is linked to a wiring error between the 32-channel blocks of the multiplexer.

Investigations on the *BeetlePA1.0* test chip which implements the pipeline readout amplifier with access to all internal nodes revealed a bug in the layout of the transmission gate used to reset the amplifier. The same error is present in the switches of the multiplexer: a shorted transistor which is used as dummy device in the transmission gate is incorrectly wired. This causes the injection of charge into the amplifier's input which results in shifting it's operating point. This error was not detected by the layout versus schematic (LVS) check, because edgeless shorted transistors are not extracted as physical devices. Fig. 4.41 contrasts the measured and simulated performance of the pipeamp on *Beetle1.0*. The layout error has been emulated in the testbed schematic.

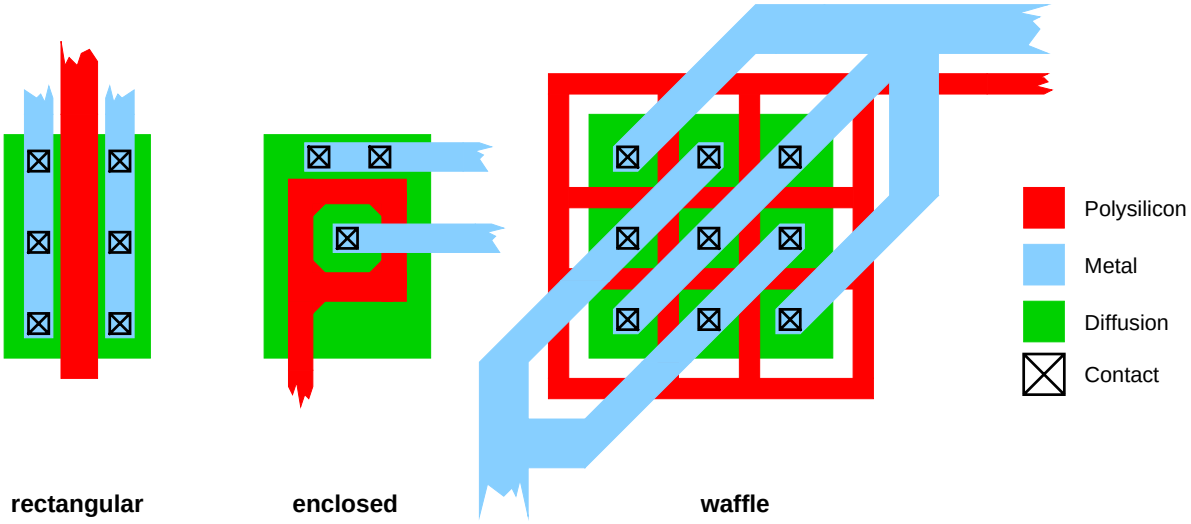


Figure 4.38: Transistor layout styles used in the various front-end implementations.

Beetle1.1

Due to the high costs of a FIB patch and the limited performance of *Beetle1.0* a successor version was developed. The intention of *Beetle1.1* (submitted in March 2001) was to fix all known bugs and to avoid the implementation of new features unless they are critical for the complete design. The following design changes have been applied:

- the layout of the tristate buffers in the control circuitry has been modified,
- a source follower has been added to each pipeamp channel to buffer the `Vdcl` bias node,
- the layout of the transmission gate used in the pipeamp and multiplexer has been modified,
- a wiring error in the multiplexer has been resolved.

Beside the above mentioned bug fixes some minor changes have been done: the *Beetle* uses a delay element for the SDA-line to assure timing constraints of the I^2C-protocol. In *Beetle1.0* this delay is a digital shift register running with the sampling clock (*Sclk*). In *Beetle1.1* it has been replaced by an analogue one. This enables a programming of the chip via I^2C-bus without applying a clock other than the I^2C-clock *SCL*. The layout of the pipeline has been modified to reduce crosstalk between the pipeline's in- and output bus (see section 4.4.3). The test channel additionally includes the pipeline and the pipeamp. The output of the pipeamp can be probed on a (buffered) pad.

The output signal of the analogue and binary pipelined readout path is shown in fig. 4.42 and 4.43 respectively. The first eight bits of the data stream encode the pipeline column number. Column number 176 has been triggered, which is clearly visible in the data header of plot 4.42. Input signals corresponding to 2 MIPs are applied to 7 single and two groups of 2 adjacent channels of the chip. The voltage levels of the header correspond to ± 2 MIPs. The reason for the slight variation of the baseline in fig. 4.42 of approx. 1/3 MIP could not been

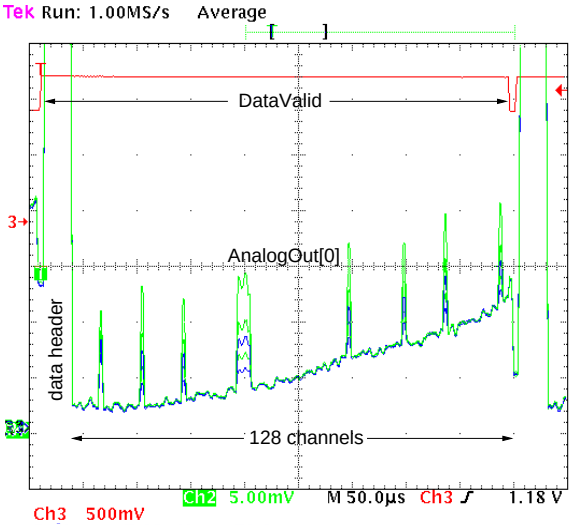


Figure 4.39: Analogue output signal of a *Beetle1.0* chip. All 128 channels are multiplexed on one port. Input signals corresponding to 1, 2, 3, 4 and 7 MIPs have been applied to 7 single and a group of 4 adjacent channels of the chip. The readout speed is set to 1.25 MHz.

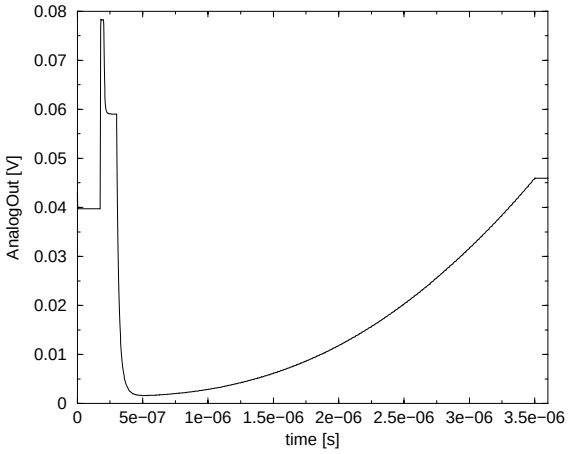


Figure 4.40: Simulation of the baseline variation in the *Beetle1.0* chip. A resistive voltage divider network between the `Vdcl` nodes of the 128 channels has been introduced to the test bench to reproduced the observed effect.

revealed so far. In binary pipelined readout the output signal levels correspond to 0 and 10 MIPs respectively. The detailed measurement results of *Beetle1.1* are presented in chapter 5.

Beside the limited performance of the front-end of *Beetle1.1*, which will be detailed in chapter 5, the chip showed an unwanted behaviour at *low trigger rates*, i.e. $\nu_{trigger} \leq 1\,kHz$, and at *consecutive triggers*. Fig. 4.44 shows on the left a readout sequence at nominal trigger rate ($\mathcal{O}(1\,\text{MHz})$), on the right a readout burst at low trigger rate. Three effects are visible (the positive peaks correspond to input signals): large negative peaks exist, which have exactly a distance of 32 clock cycles, i.e. 800 ns. The baseline varies very strongly for small channel numbers (front part) and saturates to a plateau for high channel numbers (back part). The large negative peaks have been identified as a short-time floating of the multiplexer's internal 32 channel bus (cf. 4.26). Four of such peaks exist with a distance of 32 clock cycles to each other which reflects the internal structure of the multiplexer. By changing the control sequence of several switches the effect has been patched in the successor version 1.2. The strong baseline variation has been linked to leakage currents in the multiplexer's track-and-hold capacitor (cf. fig. 4.26) which occur if the corresponding switch is in hold mode in between two non-consecutive readout sequences. By revising the control scheme of this switch (fig. 4.45) the baseline variations could be eliminated and do not show up in *Beetle1.2*.

The readout behaviour at consecutive triggers is shown in fig. 4.46. External coupling to 11 channels is used. Two readout frames are acquired, whereas only the first one comprises real input signals while no input data has been provided to the second trigger. There is a carry-over of roughly 30% of the pulse amplitude to the second frame accompanied by a signal

[27] Nominal trigger rate is $\mathcal{O}(1\,\text{MHz})$, low trigger rate is $\leq 1\,\text{kHz}$.

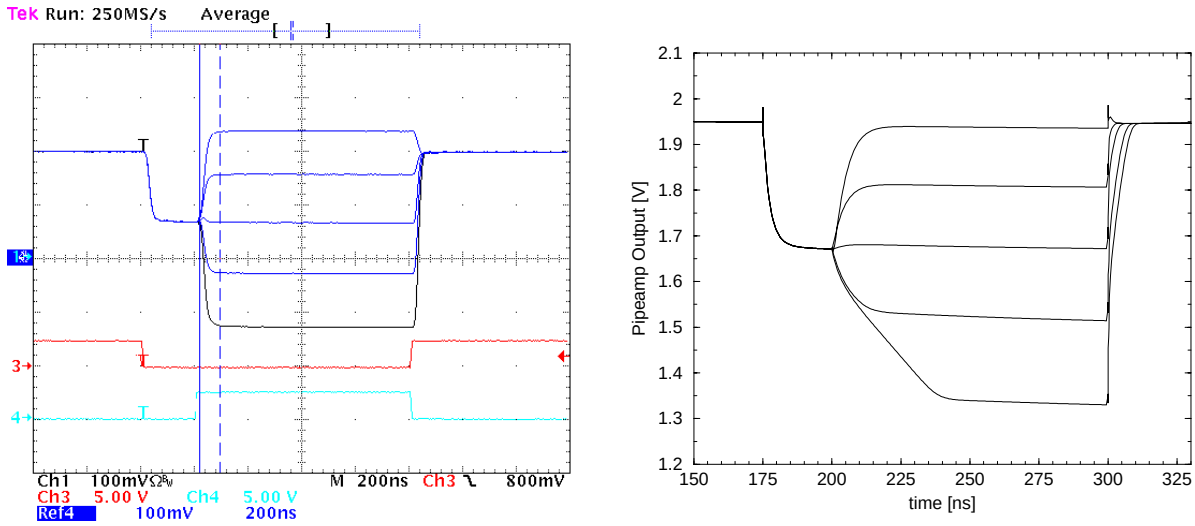


Figure 4.41: Measured (left) and simulated (right) output response of the pipeamp on the *BeetlePA1.0* test chip. The layout error has been emulated in the testbed schematic. Input signals corresponding to (from top to bottom) −10, −5, 0, +5, +10 MIP have been applied.

inversion. A sampling of the front-end pulse's remainder can be excluded. This would also not explain for the change in polarity. A possible explanation will be given in section 4.5 when the behaviour of *Beetle1.2* at consecutive triggers is discussed.

Beetle1.2

A further readout chip iteration was mainly driven by the limited performance of the *Beetle1.1* front-end (see section 5.1.1) and the need to implement a scheme for Single Event Upset protection. Front-end *set 2c* has been integrated on *Beetle1.2*[28] (cf. table 4.7). It features a smaller preamplifier feedback resistance and hence a higher max. input charge rate (see section 5.1.2). The shaper rise time is well below 25 ns especially for capacitive input loads of 30 pF and more. The total number of flip-flops on the chip increased by a factor of 3 to *3429* (cf. section 4.6). Beside these two main motives the following changes have been applied:

- Restriction of the readout time to 900 ns.
  The burst of 128 channels of data plus 16 header bits takes 900 ns. At consecutive triggers, i.e. subsequent readouts, the data bursts join directly without any gap.

- Introduction of a power-up reset.
  A reset which is active on power-up is introduced. The duration is controllable via an external capacitance (see appendix B for details).

- LVDS mode of the current output driver.
  Beside the analogue output mode of the current buffer a binary one has been integrated which meets the LVDS standard.

[28] The identical design was submitted and tested before on *BeetleFE1.1*.

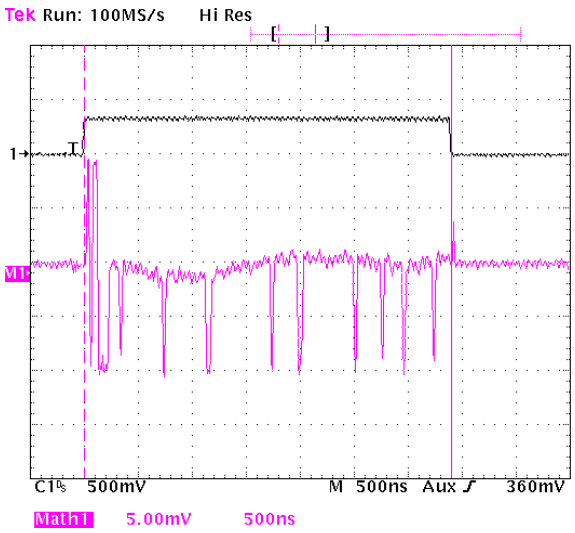


Figure 4.42: Analogue output signal of a *Beetle1.1* chip. All 128 channels are multiplexed with 40 MHz on one port. Input signals corresponding to 2 MIPs have been applied to 7 single and two groups of 2 adjacent channels of the chip.

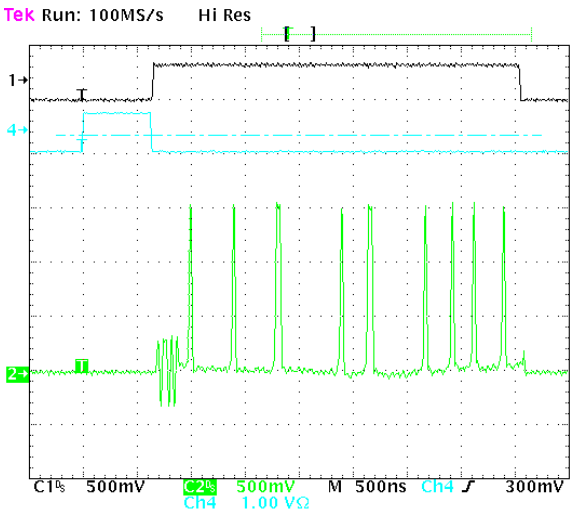


Figure 4.43: Output signal of the binary pipelined readout path. All 128 channels are multiplexed on one port. The header is encoded with ±2 MIPs. The logic levels of the binary channels are represented by 0 and 10 MIPs respectively.

- On-chip trigger synchronisation.
  The trigger input signal is synchronised on-chip to the *negative* edge of the sampling clock.
- Hard-wired I^2C-chip address.
  The I^2C-address is defined via bond pads.
- Reduction of DAC resolution from 10 to 8 bits.
- Increase of the max. deliverable bias current to 2 mA.

Fig. 4.47 shows the analogue readout sequence of *Beetle1.2*. The data header contains in comparison to the previous readout chip versions 16 bits (8 information bits plus the 8-bit pipeline column number; see appendix B for details).

As already mentioned above, *Beetle1.2* shows no particular behaviour at low trigger rates. The performance of subsequent readout sequences is anyhow different for consecutive and non-consecutive triggers. Fig. 4.48 depicts the readout behaviour for both cases. Two data frames are acquired each, whereas only the first one comprises real input signals while no input data has been provided to the second trigger. For non-consecutive triggers, the output is as expected: signals are visible in the first frame, but not in the second. For consecutive triggers, two effects are present in the second readout frame: a carry-over of roughly 30% of the signal amplitude of the first frame accompanied by a change in the signal polarity, and a strong variation of the baseline for higher channel numbers. A sampling of the front-end pulse's remainder can (again) be excluded. The first effect is also present in *Beetle1.1*.

A comparison of the readout control sequences in *Beetle1.1* and *Beetle1.2* (fig. 4.45) reveals a possible explanation for the signal carry-over. In *Beetle1.1* as well as for the consecutive

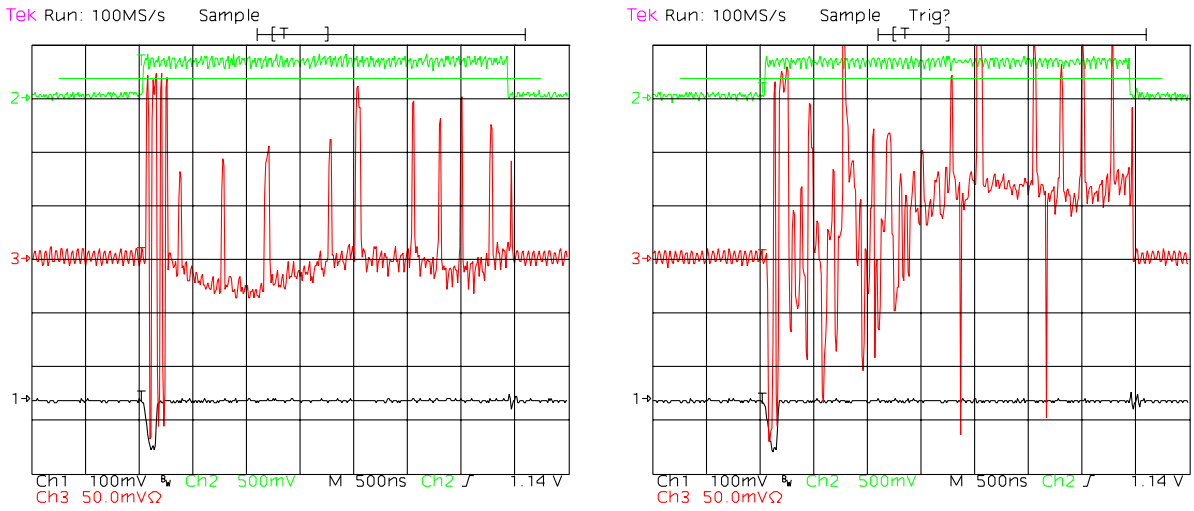


Figure 4.44: Readout behaviour of *Beetle1.1* at nominal (left) and low (right) trigger rates[27]. The various effects are explained in the text.

readout in *Beetle1.2* the switch of the multiplexer's track-and-hold stage (`Track/Hold`) and the pipeamp's reset (`Pipeamp Reset`) are operated at the same time (cf. fig. 4.21). While the track-and-hold stage returns to track-mode, the pipeamp is released from it's reset state. At this time, the charge stored on the hold capacitance is transferred to the input of the pipeamp. The fed back signal is attenuated according to the ratio of the pipeamp feedback capacitance (235 fF) and the multiplexer hold capacitance (1 pF) and additionally inverted, since the pipeamp is an inverting amplifier. At the next trigger, this signal charge will be read out. The resulting "transfer factor" is -0.235, which is in accordance with the experimental observation. The strong baseline variation for higher channel numbers in the second readout frame in fig. 4.48 could not yet been clarified.

A potential source of the baseline variation in a single-triggered readout frame (fig. 4.47, left) are *return currents on the ground-net*, which create voltage drops across channel-to-channel resistances. They can be avoided by low-ohmic power connections or by routing the power lines of each channel in a *star configuration*.

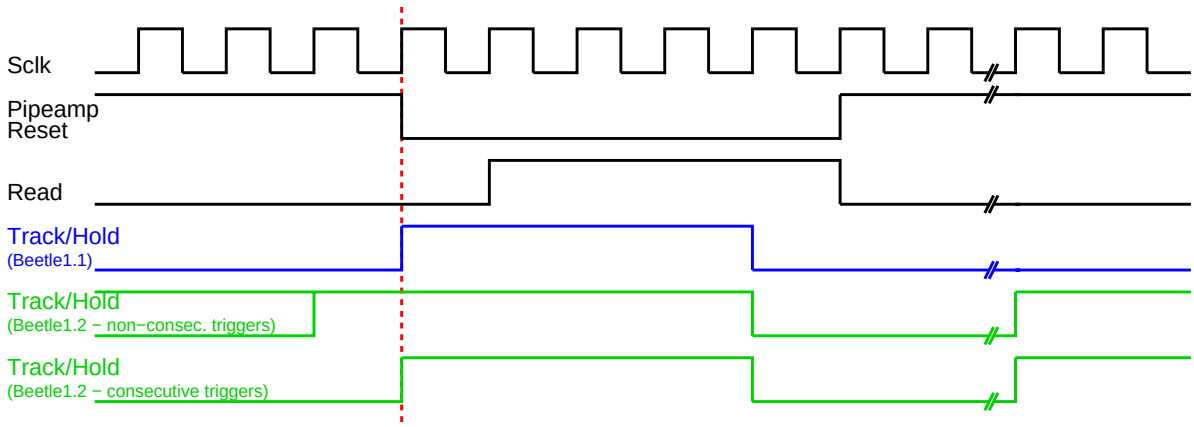


Figure 4.45: Readout timing scheme in *Beetle1.1* and *Beetle1.2*. Signals with no specification of the chip version are the same for both chips. In the case of non-consecutive triggers in *Beetle1.2*, the transition from hold-mode (`Track/Hold=0`) to track-mode (`1`) depends on the distance of the previous trigger. At latest, `Track/Hold` returns to 1 one clock cycle before `Pipeamp Reset` is released, which is indicated above.

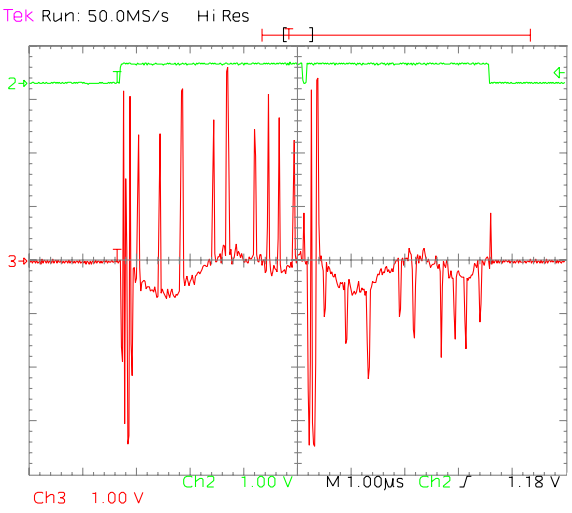


Figure 4.46: Readout behaviour of *Beetle1.1* for two triggers with external input signals applied. The plot shows two acquired readout frames, whereas only the first one comprises real input signals while no input data has been provided to the second trigger. The output is identical for consecutive and non-consecutive triggers.

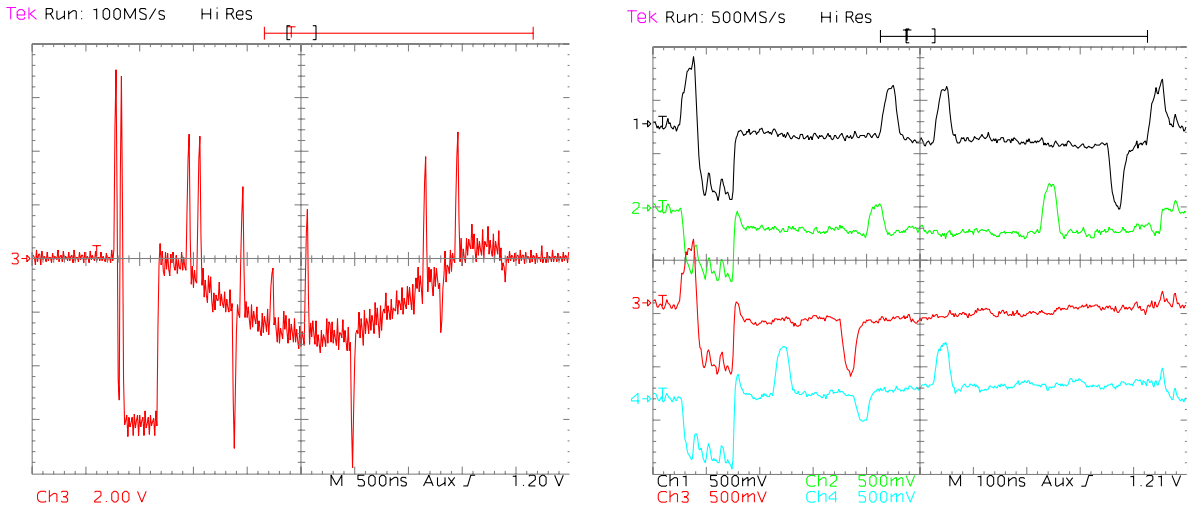


Figure 4.47: Analogue readout sequence of *Beetle1.2*. Left: 128 channels carried by one port. Right: 128 channels carried on 4 ports in parallel. All types of test pulses, i.e. +2, +1, −2, −1, have been applied to in total 10 channels.

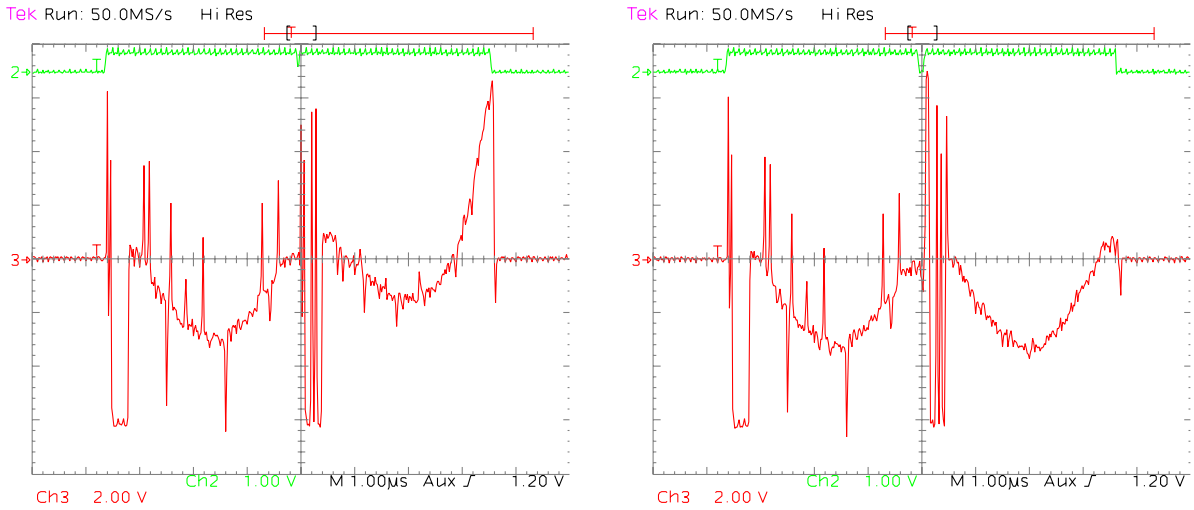


Figure 4.48: Readout behaviour of *Beetle1.2* for consecutive (left) and non-consecutive (right) triggers with internal test pulses applied. Both plots show two acquired readout frames, whereas only the first one comprises real input signals while no input data has been provided to the second trigger.

4.6 Single Event Upset Robustness

The parts on the *Beetle* chip which are sensitive to Single Event Upset (SEU) are digital memory devices realized as D-type flip-flops. They can be distinguished into *quasi-static* and *clocked* devices. The *quasi-static flip-flops* form the digital to analogue converter's (DAC) registers (in total $16 \times 8 = 128$ bits) and the *Beetle* configuration registers (in total $4 \times 8 = 32$ bits). They are clocked only, when a register write access via the programming interface occurs (cf. fig. 4.35). Compared to the 40 MHz bunch crossing frequency, the time scale of write accesses via the I^2C-bus is large ($\sim 10\,\mu s$) (therefore the term *quasi-static* is used). Even though the number of sensitive bits of all registers is small, a change in the logic state can have severe consequences. For example, a change of a bit of the register defining the preamplifier bias current can immediately change the operating point of the amplifier. A change in the logic level of a configuration register bit can switch the chip into another operation mode, e.g. from analogue to binary pipelined readout. A protection mechanism is therefore necessary. The so-called *clocked flip-flops* are used within the control logic to form the state registers of finite state machines, the derandomising buffer (FIFO) and internally used shift-registers and counters. These flip-flops are clocked with the sampling clock or a small fraction of it. Especially a change in the logic level of a state register bit can cause the logic to stop running correctly. The state machine may perform a transition to a certain state at the wrong time or even reach an undefined state in which it is stuck.

The total number of bits in *Beetle1.2*'s control logic is 520 (451 in the fast control and 69 in the slow control)[29]. The main contributors are the trigger buffer (FIFO) with its associated flag bits with 176 bits ($= 16 \times (8+3)$) and the *look-ahead* buffers of the pipeline with 144 bits ($= 2 \times ((\frac{16}{2}+1) \times 8)$).

The choice of a specific mechanism to prevent the propagation of an SEU error through the circuit has to meet several constraints:

- topology of sensitive building blocks
  The SEU sensitive devices are distributed over the chip area (cf. fig. 4.11): the bias registers are split into a front-end part which is located in the lower left chip corner and a back-end part placed at the right edge of the chip. They have a distance of several millimetres. The configuration registers and all other sensitive flip-flops are spread in the logic block underneath the pipeline, the pipeamp and the multiplexer.

- available area
  Especially the front-end bias registers are limited in area. They are constrained by the front-end at top and the control logic at right.

- error latency
  The error latency, i.e. the time between the occurrence of an upset and the detection and correction, should be one sampling clock cycle or less to avoid an error transfer to the next bunch crossing.

For both the quasi-static and the clocked registers the *redundancy* approach using *majority voting flip-flops* has been chosen (cf. section 3.2). The advantage of this approach compared

[29] In *Beetle1.0* and *Beetle1.1* 659 bits (500 in the fast control and 159 in the slow control) are implemented. The different number of bits compared to the chip version 1.2 is mainly due to a modified decoder scheme in the I^2C-decoders.

to an EDC code like e.g. *Hamming*-coding (cf. section 3.2.5), is the *local* implementation and the very *small error latency*. Large-scale routing or the implementation of the EDC logic at a few places is avoided. An EDC logic also needs several clock cycles for a correction step.

Two types of redundant flip-flops are utilised:

- A triple redundant flip-flop using majority voting and featuring one output (Q). This flip-flop will be referred to as *TRDFF*.
- A triple redundant flip-flop which has two outputs: one is the majority of the three internal flip-flops (Q), the other one (F) indicates, if the logic states of the internal flip-flops are not equal. This flip-flop is named *TRFDFF*.

Fig. 4.49 shows the block schematic of the flip-flop of type *TRFDFF*. *TRDFF* is a subset of this. The corresponding truth table is shown in table 4.8. The combinational logic inside the flip-flops is represented by

$$\begin{aligned} Q &= \overline{A}\cdot B\cdot C + A\cdot\overline{B}\cdot C + A\cdot B\cdot\overline{C} + A\cdot B\cdot C \\ &= \overline{A}\cdot B\cdot C + A\cdot\overline{B}\cdot C + A\cdot B = B\cdot\underbrace{(A+\overline{A}\cdot C)}_{\equiv(A+C)} + A\cdot\overline{B}\cdot C \\ &= A\cdot B + C\cdot\underbrace{(B+A\cdot\overline{B})}_{\equiv(A+B)} = A\cdot B + A\cdot C + B\cdot C = \overline{\overline{A\cdot B}\cdot\overline{A\cdot C}\cdot\overline{B\cdot C}} \qquad (4.20) \\ F &= \overline{A}\cdot\overline{B}\cdot C + \underbrace{\overline{A}\cdot B\cdot\overline{C} + \overline{A}\cdot B\cdot C}_{\equiv\overline{A}\cdot B} + \underbrace{A\cdot\overline{B}\cdot\overline{C} + A\cdot\overline{B}\cdot C}_{\equiv A\cdot\overline{B}} + A\cdot B\cdot\overline{C} \\ &= \overline{A}\cdot\underbrace{(\overline{B}\cdot C + B)}_{\equiv(C+B)} + A\cdot\underbrace{(\overline{B}+B\cdot\overline{C})}_{\equiv(\overline{B}+\overline{C})} = \overline{A}\cdot B + A\cdot\overline{B} + \overline{A}\cdot C + A\cdot\overline{C} \\ &= A\oplus B + A\oplus C = \overline{\overline{A\oplus B}\cdot\overline{A\oplus C}}. \qquad (4.21) \end{aligned}$$

The advantage of the transformation of the primary sum of products (SOP) is, that a *fully balanced* equation results. The corresponding implementation with logic gates avoids *glitches* which occur if the propagation delays of signals contributing to one gate are not equal.

A	B	C	Q	F
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	1
1	0	0	0	1
1	0	1	1	1
1	1	0	1	1
1	1	1	1	0

Table 4.8: Truth table of the triple redundant flip-flop with an additional output (F) indicating the change of an internal logic state. A, B and C represent the output nodes of the internally used standard flip-flops (cf. fig. 4.49).

Self-triggered Correction

The output F of the *TRFDFF* type flip-flop allows the implementation of a *self-triggered correction* mechanism. Fig. 4.50 demonstrates the principle. The flip-flop output as well as the F-output are fed back to the data and clock input respectively. A switch selects between the external inputs and the feedback loop. The control strobes are derived from the I^2C-transfer. As long as the I^2C-bus is busy the external flip-flop inputs are selected, a free bus activates the feedback loop. While switching between the two signal paths one has to take care on the sequence of the data and clock control strobe. A transition from external to internal signal paths first has to activate the data port and then, with a delay corresponding to the flip-flop setup time ($t_{su} \approx 200\,\text{ps}$), the clock port. This guarantees, that in the moment of switching a meanwhile occurred SEU cannot trigger the flip-flop and violate the setup time. In the other case, the switching from internal to external signals, the clock port has to be switched before the data port. This avoids a self-triggering of the flip-flop while external data is present at the D input.

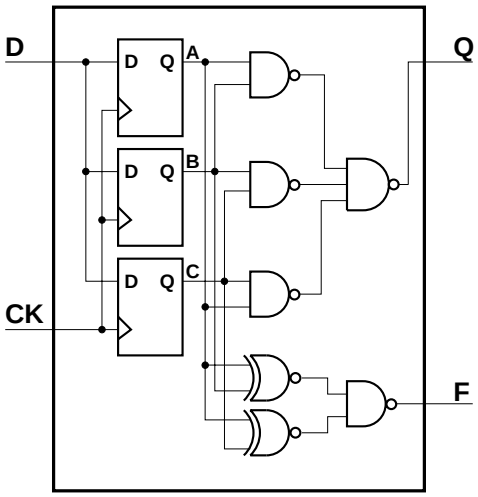


Figure 4.49: Triple redundant flip-flop with an additional output (F) indicating the change of an internal logic state. The internal flip-flops are out of a standard cell library.

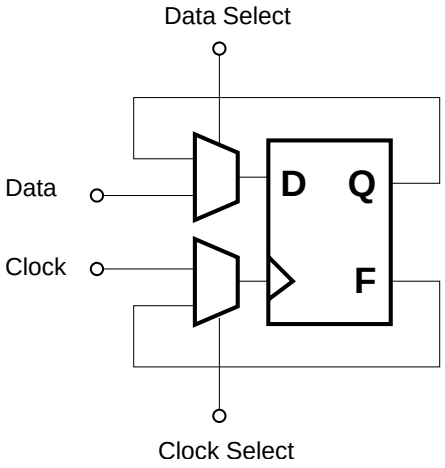


Figure 4.50: Principle schematic of a flip-flop featuring a self-triggered SEU correction. The multiplexers, i.e. switches, select between an external access and the feedback loop.

The principle schematic of an integrated CMOS[30] flip-flop is shown in fig. 4.51. The detailed schematic of the *TRFDFF* flip-flop is given in fig. 4.52. The dynamic behaviour after the injection of a charge to a sensitive node is shown in fig. 4.53. Usually the injection current pulse is modelled featuring an exponential rise and fall [Fac99b]. In the presented simulation it has been approximated by a triangular pulse. A total charge of 500 fC has been injected in 500 ps to node `SLO` (cf. fig. 4.52), which is forced to change it's state for 1.2 ns. The flip-indication bit `F` is active for 1.34 ns which is well above the minimum clock width for a resetable flip-flip in this process technology of 0.403 ns[31]. The flip-flop output `Q` remains unchanged all

[30] In textbooks about digital circuits a flip-flop is mostly based on (N)AND or (N)OR gates. Compared to the schematic presented in fig. 4.51 this requires a higher number of transistors (34 compared to 24).

[31] The quoted numbers are for typical process parameters. Even for process variations resulting in a higher device speed, the width of the self-correction clock is a factor 2 above the minimum tolerable clock width.

the time. The injected charge is about a factor 2.5 higher compared to the estimation from measurement results in section 3.1.4.

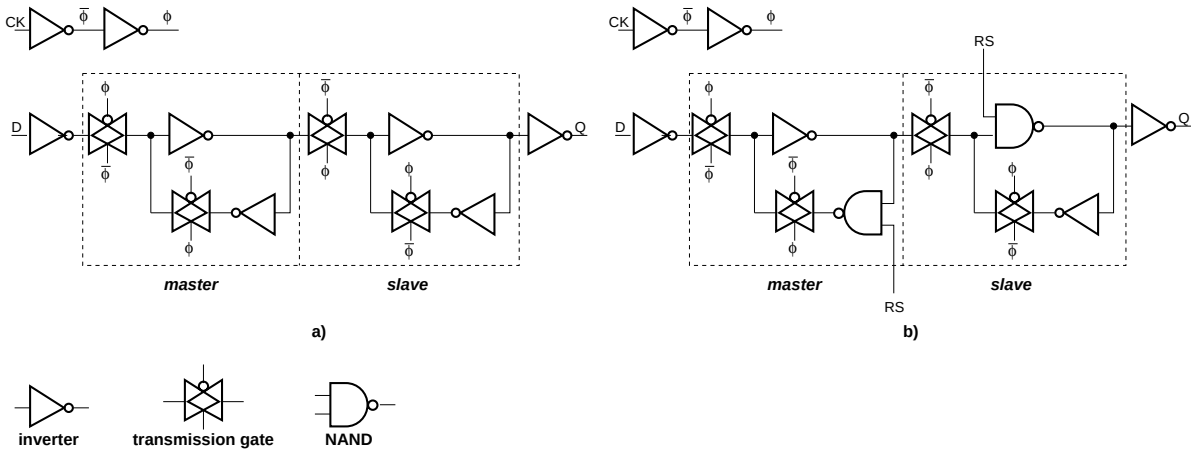


Figure 4.51: Principle schematic of an integrated D-type flip-flop without (a) and with (b) asynchronous reset. The three building elements are explained at the bottom.

Single Event Upset Counter

An 8-bit counter is integrated in *Beetle1.2* to indicate the number of occurred Single Event Upsets. The counter output is readable via the I^2C-bus. The two least significant bits (LSB) are additionally transferred in the header of the analogue output stream. This allows a fast monitoring of SEUs during readout. An I^2C-write access to the counter register resets it. All *Beetle* registers, including the shift-registers *CompChTh*, *CompMask* and *TpSelect*, are contributing to the SEU counter. The bits used in the logic control circuits are *not* taken into account. The counter clock is generated as the logic OR connection of the flip-flops' F-output.

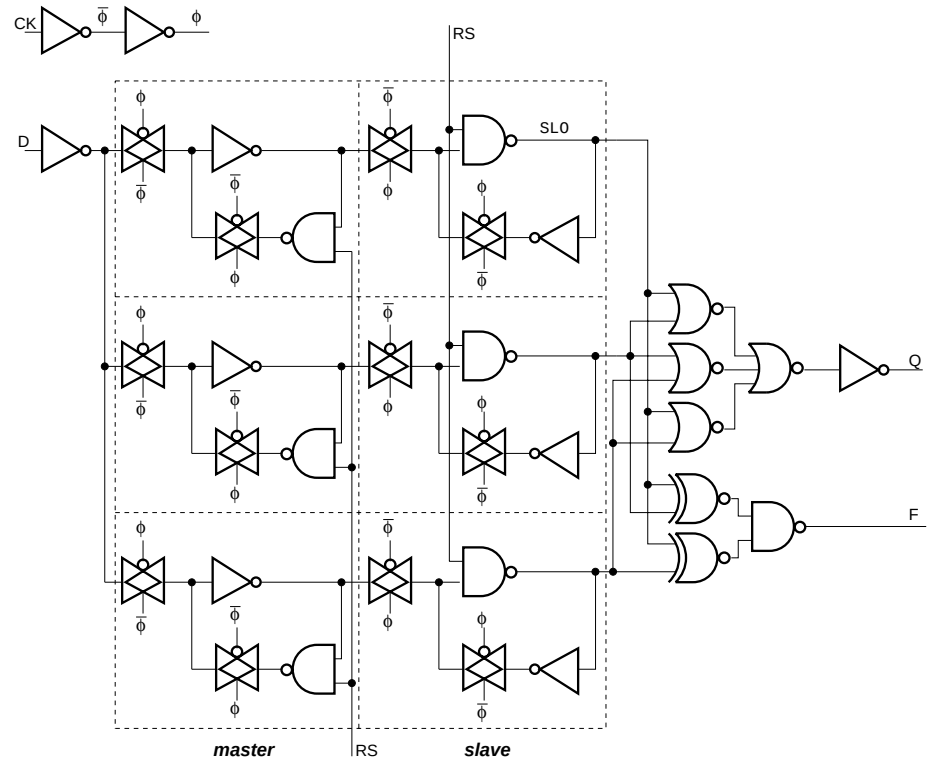


Figure 4.52: Detailed schematic of the *TRFDFF* flip-flop.

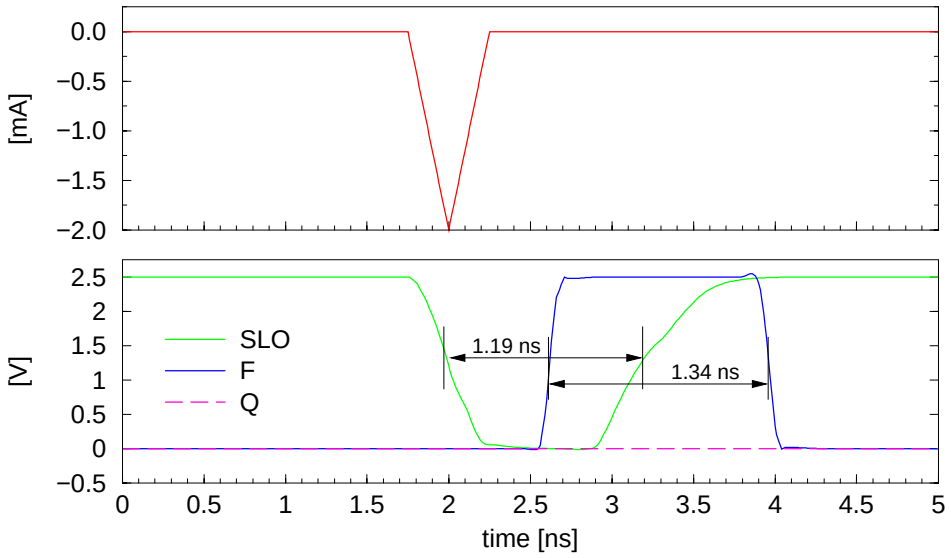


Figure 4.53: Simulation result of a self-triggered correction process. A total charge of 500 fC has been injected as a triangular pulse with a width of 500 ps. The disturbance of the sensitive node (`SLO`) takes 1.2 ns. The clock (`F`) triggering the self-correction has a width of 1.34 ns, which is well above the required minimum width defined by the process technology. The flip-flop output `Q` remains unchanged all the time.

Chapter 5

Chip Characterisation

This chapter presents the measurement results obtained with the readout chip versions *Beetle1.1* and *Beetle1.2* as well as with the test chips *BeetleFE1.1* and *BeetleSR1.0*. The key parameters of the *Beetle* resulting from the requirements on the chip (cf. section 4.2) are summarised in table 5.1.

parameter	description
$t_r(C_p, \mathrm{D})$	shaper rise time (10−90%) as a function of capacitive input load and dose
$t_p(C_p, \mathrm{D})$	shaper peaking time (0−100%) as a function of capacitive input load and dose
$V_p(C_p, \mathrm{D})$	shaper peaking voltage as a function of capacitive input load and dose
$\mathrm{R}(C_p, \mathrm{D})$	pulse remainder 25 ns after the peak as a function of capacitive input load and dose
$\mathrm{ENC}(C_p)$	equivalent noise charge as a function of capacitive input load
$\dot{Q}_{max}$	max. input charge rate
PHP	pipeline homogeneity for pedestals
PHG	pipeline homogeneity for gain

Table 5.1: Key parameters of the *Beetle* readout chip.

5.1 Pre-irradiation Performance

For a standalone characterisation of the readout chip, i.e. without a silicon detector applied to it's input, the *Beetle* chip is glued[1] on a gold-plated test PCB[2] which is designed to carry two chips. The test PCB allows the charge injection to 12 input channels. The corresponding circuit is shown in fig. 5.1. With the component sizes given in fig. 5.1 a voltage step of 2.6 V at the input results in an injected charge of Q_{inj} = 22,700 e^-. Beside this, the test PCB implements passive components for blocking the power supply lines. The test PCB itself is carried by another board integrating the analogue resp. binary receiver circuitry (fig. 5.3) and a level shifter circuit for the I^2C-bus (see appendices A and B for details). For analogue output signals the *CLC400* [Nat01] transimpedance amplifier is used, binary signals are acquired with the *DS90C032* [Nat98] LVDS receiver. The two receiver circuits are depicted in fig 5.2.

[1] A two-component epoxy glue is used (Polytec EPO-TEK H20S [Pol]).

[2] Printed Circuit Board

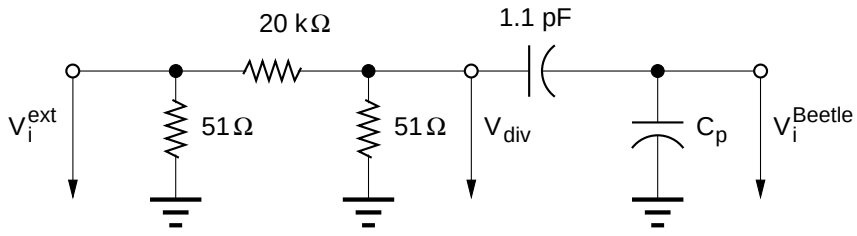


Figure 5.1: Schematic of the charge injection circuit on the *Beetle* test boards. The resistive divider is placed on the carrier board, while the coupling and load capacitances are located on the test PCB, directly in front of the chip inputs.

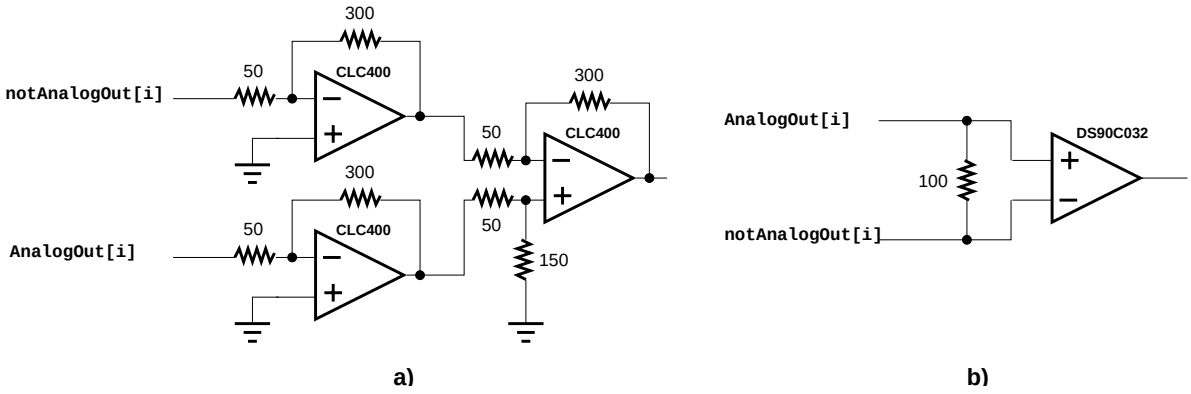


Figure 5.2: Receiver circuits for analogue (a) and binary (b) *Beetle* output signals.

5.1.1 Pulse shaping

The front-end pulse is characterised by three parameters: peaking time t_p $(0-100\%)$, peaking voltage V_p and remainder R, which is the ratio between the signal voltage 25 ns after the peak and V_p. The peaking time is sometimes hard to measure since the starting point of the pulse is not well defined, so the rise time t_r $(10-90\%)$ is quoted in addition.

Information about the front-end's pulse shape can be obtained on a *Beetle* readout chip from either the test channel output `FETestOut` (cf. fig. 4.9) or from a *pulse shape scan*. Here, the front-end's output is read out via the pipelined path while the preamplifier input signal is shifted w. r. t. the sampling clock. The pulse shape is defined by 5 parameters listed in table 5.2 with the corresponding "standard" settings.

Parameter	Description	"standard" setting	
Ipre	preamplifier bias current	600	μA
Isha	shaper bias current	80	μA
Ibuf	buffer bias current	80	μA
Vfp	preamplifier feedback voltage	0	V
Vfs	shaper feedback voltage	0	V

Table 5.2: Front-end pulse shape parameters.

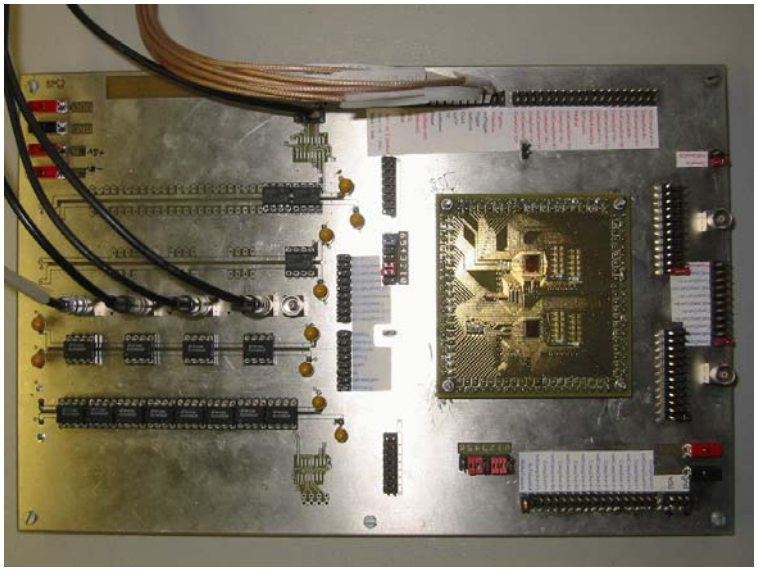


Figure 5.3: Photography of the laboratory test setup. Two *Beetle* chips are glued on a PCB which is mounted on a second board carrying the output receiver circuits.

Fig. 5.4 depicts the front-end output signal obtained from a pulse shape scan at a capacitive input load of $\sim 3\,\mathrm{pF}$. The parameter *Vfs* is varied. The peaking time for both pulses exceeds 30 ns which is in disagreement to simulation results. The reason for this discrepancy is identified in a saturation of the preamplifier bias current generator. Fig. 5.6 shows a measurement on *Beetle1.1* for load capacitances varying between 3 pF and 32 pF at the test channel's output as well as the result of a pulse shape scan.

The new front-end development (set 2c) overcomes the problem of $t_p > 25\,\mathrm{ns}$ and $R > 30\%$. Fig. 5.5 shows the front-end output pulse of *Beetle1.2* measured at the test channel output (`FETestOut`), table 5.3 lists the corresponding pulse shape parameters. Even for high capacitive loads, the peaking time is well below 25 ns, the remainder is $< 30\%$ for $C_p < 35\,\mathrm{pF}$.

C_p [pF]	V_p [mV]	t_p [ns]	t_r [ns]	R [%]
3	36.70	20.50	12.93	3.94
13	30.52	22.00	14.54	13.02
26	26.36	23.00	15.82	23.84
36	23.19	23.25	16.10	30.85
51	19.68	23.75	16.96	40.06

Table 5.3: Measured pulse shape parameters of *Beetle1.2*.

5.1.2 Maximum Input Charge Rate

The maximum input charge rate has been measured by superimposing a DC current to the AC input pulse. This has been accomplished with a variable resistor of several MΩ between the amplifier's input node and the positive supply voltage (2.5 V). The DC current, at which

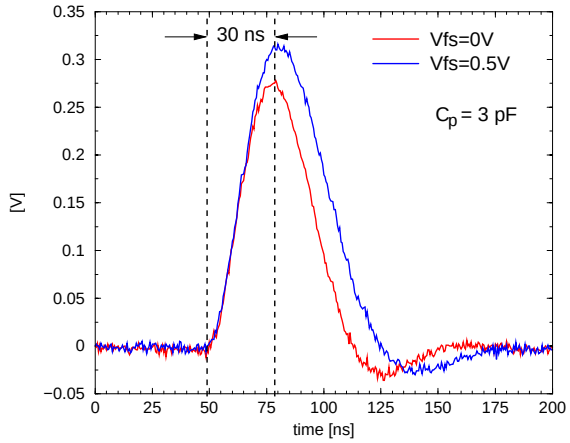


Figure 5.4: Front-end output signal of *Beetle1.1* obtained from a pulse shape scan. Two different bias parameter sets with varying *Vfs* have been chosen ($Ipre = 600\,\mu$A, $Isha = Ibuf = 80\,\mu$A, $Vfp = 0$ V). The offset is subtracted.

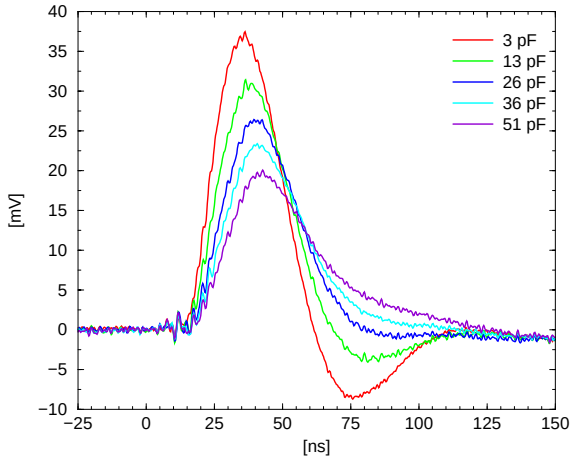


Figure 5.5: Front-end output signal of *Beetle1.2* measured at the test channel output (`FETestOut`) [Löc03]. The load capacitance is varied between 3 pF and 51 pF.

the front-end output starts to degrade, determines the limiting charge rate. $\dot{Q}_{max}$ has been measured to 312 nA for *Beetle1.2*.

5.1.3 Noise

Noise measurements have been performed in two ways:

- *Method 1*: Sampling at the front-end output: The output of the front-end is directly accessed on the *Beetle* readout chips at the test channel (`FETestOut`, cf. fig. 4.9)
- *Method 2*: Sampling at the analogue output (`AnalogOut`) of the chip.

For the noise measurements, the input of the preamplifier has been connected to ground at the node V_{div} of the injection circuit (fig. 5.1). Note, that the coupling capacitance C_c is in parallel to C_p and contributes to the parallel load. The measurement procedures will be described shortly.

Method 1: Sampling at the front-end output Samples at two positions of the signal shape are acquired. One sampling point is at the baseline long before the peak positions, the other point is the peak position itself[3]. The difference of both values is calculated per sample in order to reject common-mode effects. In total 5000 samples are acquired. The RMS of the resulting distribution defines the noise voltage $\sqrt{2}v_n$.

[3]This distinction is not essential. Since no input pulse is present, any two sampling points can be used.

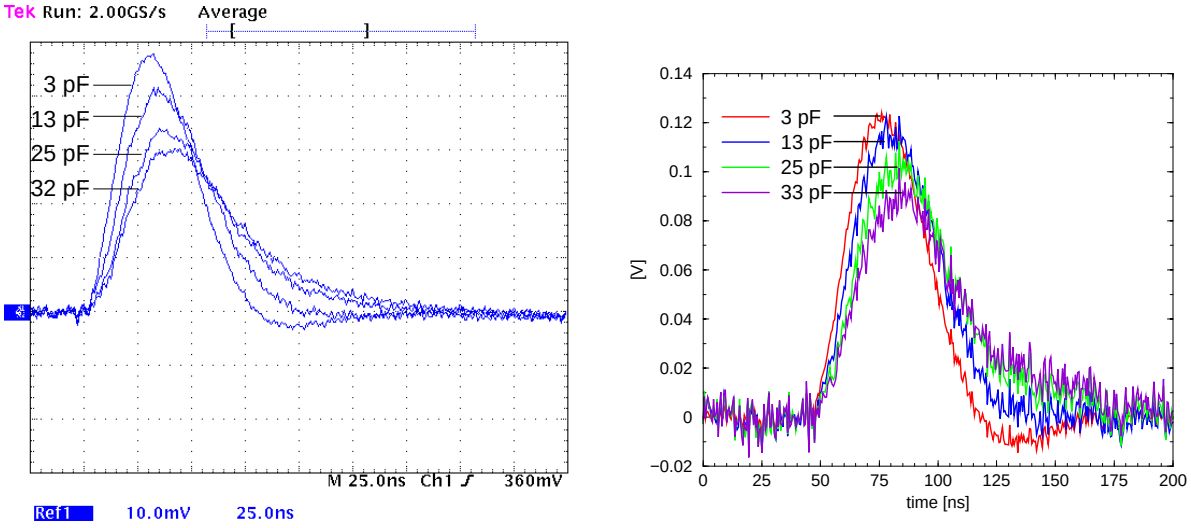


Figure 5.6: Transient response on a delta-shaped input signal measured at the *Beetle1.1*'s test channel (left) as well as extracted from a pulse shape scan (right). Load capacitances of 3 pF, 13 pF, 25 pF and 32 pF have been applied to the preamplifier's input.

The equivalent noise charge ENC is determined from the noise voltage v_n, via

$$\mathrm{ENC} = \frac{v_n}{A_Q} = \frac{v_n}{V_p/Q_{in}} \quad [e^-], \tag{5.1}$$

with
v_n the noise voltage ([V]),
A_Q the charge gain ([V/e^-]),
V_p the peak voltage of the shaped pulse ([V]),
Q_{in} the injected input charge ([e^-]).

Method 2: Sampling at the chip output Samples of 12 channels V_{ij}^k ($i = 1 \ldots 6, j = 1, 2$) are acquired. The 12 channels are grouped into 6 pairs of neighbouring channels having the same capacitive input load. In total 5000 samples per channel are taken. The mean value per channel $\langle V_{ij} \rangle$ is subtracted from each sample V_{ij}^k in order to reject channel-to-channel variations (ΔV_{ij}^k). The samples of two channels with the same input load are subtracted from each other ($\frac{1}{\sqrt{2}}(V_{i1}^k - V_{i2}^k)$) to eliminate common-mode effects. The noise voltage is calculated after eq. 5.2. The equivalent noise charge is determined after eq. 5.1.

$$v_{n,i} = \sqrt{\frac{1}{N}\sum_{k=1}^{N}(\Delta V_i^k - \langle \Delta V_i^k \rangle)^2} \tag{5.2}$$

with
$N = 5000$ the number of samples per channel,
$\Delta V_i^k = 1/\sqrt{2}(\Delta V_{i1}^k - \Delta V_{i2}^k)$ (common-mode rejection),
$\Delta V_{ij}^k = V_{ij}^k - \langle V_{ij} \rangle$ (rejection of channel-to-channel variations).

Extensive measurements have been done on the noise performance of front-end set 2c on the *BeetleFE1.1* test chip. The identical design is implemented on the *Beetle1.2* readout chip. Table 5.4 lists the results of three independent measurements, the corresponding plots are shown in fig. 5.7. The "Heidelberg" value is measured according to method 1.

Heidelberg	$\mathrm{ENC} = 483\,\mathrm{e}^- + 45.7\,\mathrm{e}^-/\mathrm{pF} \cdot \mathrm{C}_{in}$
NIKHEF	$\mathrm{ENC} = 429\,\mathrm{e}^- + 47.0\,\mathrm{e}^-/\mathrm{pF} \cdot \mathrm{C}_{in}$
Zürich	$\mathrm{ENC} = 436\,\mathrm{e}^- + 47.7\,\mathrm{e}^-/\mathrm{pF} \cdot \mathrm{C}_{in}$

Table 5.4: Equivalent noise charge of front-end set 2c.

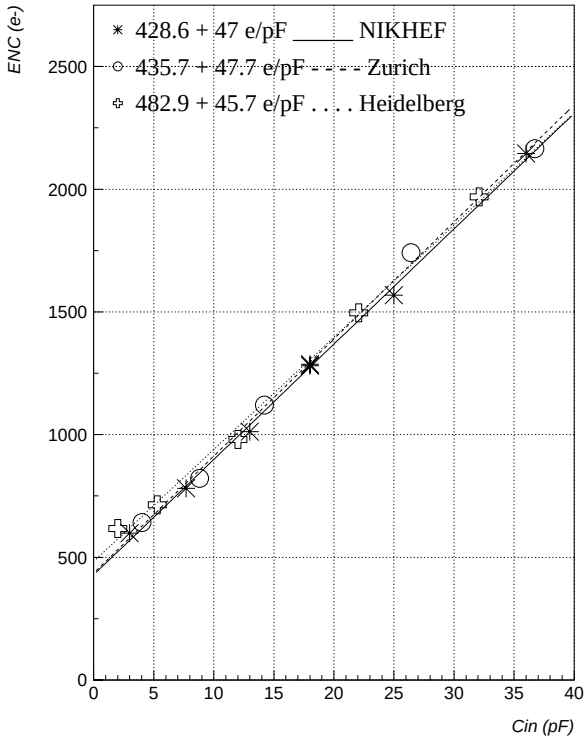


Figure 5.7: Equivalent noise charge as function of the load capacitance of the *Beetle1.2* front-end (measured on the *BeetleFE1.1* test chip) [Jan01].

A measurement of the identical front-end, but on the test channel of *Beetle1.2*, obtained [Bak02]

$$\mathrm{ENC} = 496.7\,\mathrm{e}^- + 48.3\,\mathrm{e}^-/\mathrm{pF} \cdot \mathrm{C}_{in}, \tag{5.3}$$

which is in good agreement to the noise figures of *BeetleFE1.1*. Applying method 2 (sampling at `AnalogOut`), a noise figure of

$$\mathrm{ENC} = (810 \pm 20)\,\mathrm{e}^- + (43 \pm 2)\,\mathrm{e}^-/\mathrm{pF} \cdot \mathrm{C}_{in} \tag{5.4}$$

is obtained for *Beetle1.1*. The data acquisition for the described analysis is done for a fixed pipeline column number. The slope is, within the error margin, compatible with the results obtained from direct front-end measurements (table 5.4). The large offset in eq. 5.4 can be explained by a noise contribution of the external receiver circuit. A receiver stage with a higher gain should reduce this effect.

5.1.4 Pipeline Homogeneity

The pipeline homogeneity of *Beetle1.1* has been investigated concerning *pedestal variations* and the *gain uniformity*.

Pedestals

The pedestal value of all 128×186 = 23,808 pipeline cells has been determined by taking the average of 5000 samples per cell. The input channels were floating, i.e. not bonded. Fig. 5.8 shows as an illustration the surface plot of the pipeline pedestals of a *Beetle1.1* chip. The "S-shaped" variation of the readout baseline (cf. fig. 4.44, left) is clearly visible in the left plot where the raw data is shown. In the right plot of fig. 5.8 the baseline variation is corrected. The pedestal distribution of the complete pipeline of 3 *Beetle1.1* chips is depicted in fig. 5.9. The RMS-value is $\leq 1.85\,\mathrm{mV}$ which corresponds to $380\,\mathrm{e}^-$. The pedestal variation per channel is $\leq 2.36\,\mathrm{mV}$ corresponding to $485\,\mathrm{e}^-$. Note, that by taking the average over the acquired samples per cell, noise cancels. Therefore, the resulting RMS-value in electrons can be smaller than the equivalent noise charge.

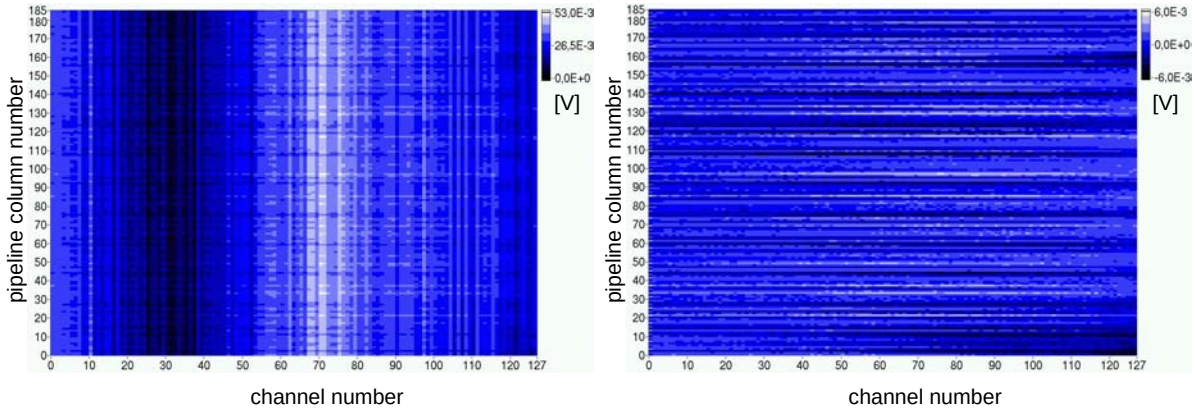


Figure 5.8: Surface plots of the pipeline pedestals of a *Beetle1.1* chip. The left plot depicts the raw data. The variation of the readout baseline along the channels is clearly visible. In the right plot the baseline variation is corrected.

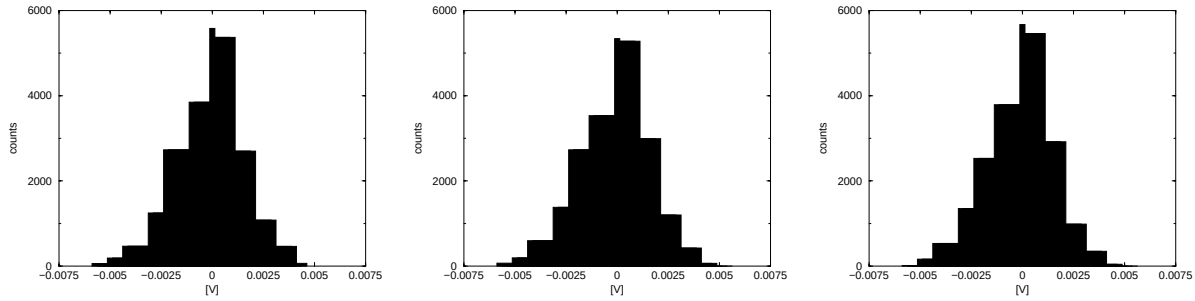


Figure 5.9: Pedestal distributions of the complete capacitor array for 3 *Beetle1.1* chips.

Gain

The gain uniformity has been determined in two ways, where 12 channels are bonded to an external signal source:

- Two independent measurements, with and without input pulses applied, are performed. The voltage difference determines the gain.
- A pulse shape scan over all pipeline columns is done. The gain is extracted from the pulse's peaking voltage.

Both measurement procedures provide consistent results. The RMS-value of the obtained distributions is $\leq 1.22\,\mathrm{mV}$ which corresponds to $250\,\mathrm{e}^-$.

5.1.5 Random Trigger Test

A test of the logic circuitry which controls event storage and readout (*FastControl*) was performed on *Beetle1.1* as well as *Beetle1.2* [Löc03]. The aim of the test, was to prove the correct processing of an arbitrary sequence of triggers. Therefore, a random trigger was applied to the chip. It should be emphasised, that this test only reveals *functional errors* inside the logic. A correct timing behaviour is only checked incidentally. This can be done more easily with periodical triggers or the application of a clock frequency higher than the nominal 40 MHz (over-clocking test). As a consequence, the test can be performed at clock frequencies smaller than 40 MHz and be scaled to the nominal frequency. It should also be mentioned, that the trigger rejection ratio is no characteristic of the chip but only depends on the distribution of generated triggers. The random trigger is generated by discriminating the output of a noisy amplifier. The number of generated triggers is compared to the number of readout bursts and the number of rejected triggers, i.e. triggers which are sent while the trigger fifo is full (`FifoFull = 1`). *Beetle1.1* as well as *Beetle1.2* successfully passed the test with $\mathcal{O}(10^{12})$ triggers. *Beetle1.2* operated at 40 MHz sampling clock frequency, while *Beetle1.1* performed this test at $Sclk = 20\,\mathrm{MHz}$ due to setup constraints.

5.2 Irradiation Results

The readout chip version *Beetle1.1* was subject to a total ionising dose irradiation test with an accumulated dose of 45 Mrad(SiO_2). No functional errors have been observed and only slight performance degradations occurred. A Single Event Upset test was performed with the test chip *BeetleSR1.0* using 33 MeV alpha particles. SEU events have been observed but a determination of an SEU cross section was not possible due to a misalignment of the setup. In the following the details of the experiments will be described.

5.2.1 Total Ionising Dose Irradiation Test

The TID irradiation test was performed in October 2001 at the X-ray irradiation facility of CERN's microelectronics group [Mic01a]. In total 4 *Beetle1.1* readout chips and 2 *BeetleFE1.1* front-end test chips have been irradiated. Fig. 5.10 shows a photography of the irradiation setup. The distance between collimator exit window and chip surface was $\sim$ 1 cm. A dose of 45 Mrad(SiO_2) has been accumulated at maximum for one chip. Table 5.5 summarises the irradiation steps for the various chips. Two *Beetle1.1* chips (labelled '*R*') have been kept at room temperature all the time, while the other two (labelled '*A*') have been annealed at 100 °C in between the irradiation periods and continously for one week after irradiation. The two *BeetleFE1.1* chips were not subject to annealing.

step	integral dose [Mrad(SiO_2)]				
	Beetle1.1-R1	*Beetle1.1*-A1	*Beetle1.1*-R2	*Beetle1.1*-A2	*BeetleFE1.1*
1	0.1	0.1	0.5	0.5	3.3
2	0.2	0.2	1	1	6.7
3	0.5	0.5	2	2	10
4	1	1	4	4	—
5	2	2	6	6	—
6	5	5	8	8	—
7	10	10	10	10	—
8	15	15	—	—	—
9	20	20	—	—	—
10	30	30	—	—	—
11	45[4]	—	—	—	—

Table 5.5: TID irradiation steps for the various *Beetle* chips. The label '*R*' indicates operation at room temperature, while '*A*' represents annealing at 100 °C in between the irradiation periods.

The X-ray tube has been operated at an anode voltage of 40 kV. The relation between dose rate and tube current is given by [Mic01b]

$$\dot{D}\,[\mathrm{rad}(SiO_2)/\mathrm{min}] = 89 + 664.93 \cdot I_{tube}\,[\mathrm{mA}]. \tag{5.5}$$

The power consumption of the *Beetle* chips has been monitored during irradiation. A significant increase could not been detected.

[4]This last step has been performed at an anode voltage of 50 kV. The corresponding calibration function is given by $\dot{D}\,[\mathrm{rad}(SiO_2)/\mathrm{min}] = 79 + 791.41 \cdot I_{tube}\,[\mathrm{mA}]$ [Mic01b].

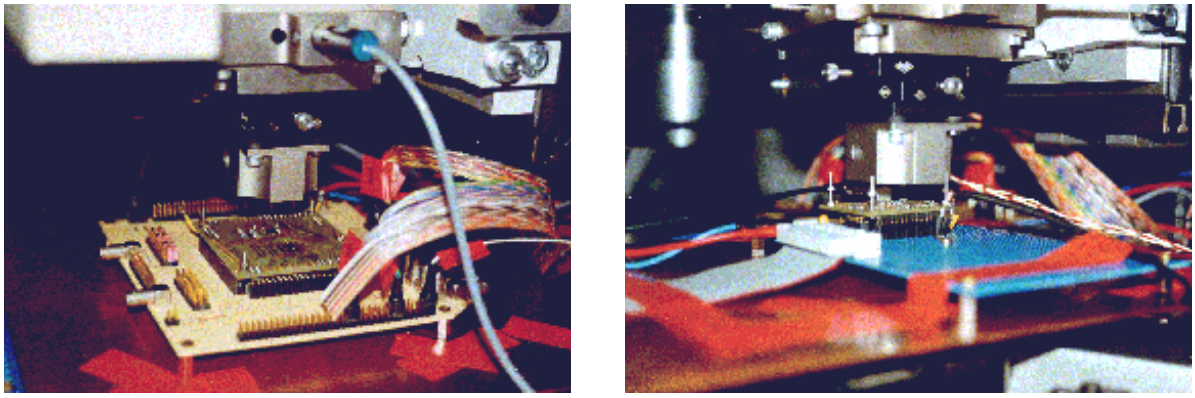


Figure 5.10: Setup of the total ionising dose irradiation test performed with *Beetle1.1* (left) and *BeetleFE1.1* (right). The distance between collimator exit window and chip surface was $\sim 1\,\text{cm}$.

For this test, 12 input channels have been coupled to the injection circuit (channel numbers 6, 15, 25, 28, 42, 48, 55, 72, 80, 89, 111, 118). Groups of 2 channels had the same capacitive input load varying between 3 pF and 52 pF. After each irradiation step, a pulse shape scan has been performed. During irradiation the chip has been operated, i.e. was continously reading out.

Fig. 5.11 shows the pulse shapes of *Beetle1.1*-R1 for different doses at 3 pF input load. After 45 Mrad, the peaking time increased by 4.5 ns and the peaking voltage decreased by $\sim 15\%$. The pulse shape parameters peaking time t_p, peaking voltage V_p, remainder R and offset voltage V_{os} for different C_p as a function of dose are depicted in fig. 5.12. The annealing procedure, which kept 2 chips for one week at 100°C, showed no significant effects on the pulse shapes. Fig. 5.13 shows the pulse shape parameters t_p, t_r, V_p and R of *BeetleFE1.1* as a function of dose. Up to the accumulated dose of 10 Mrad, no significant changes can be determined.

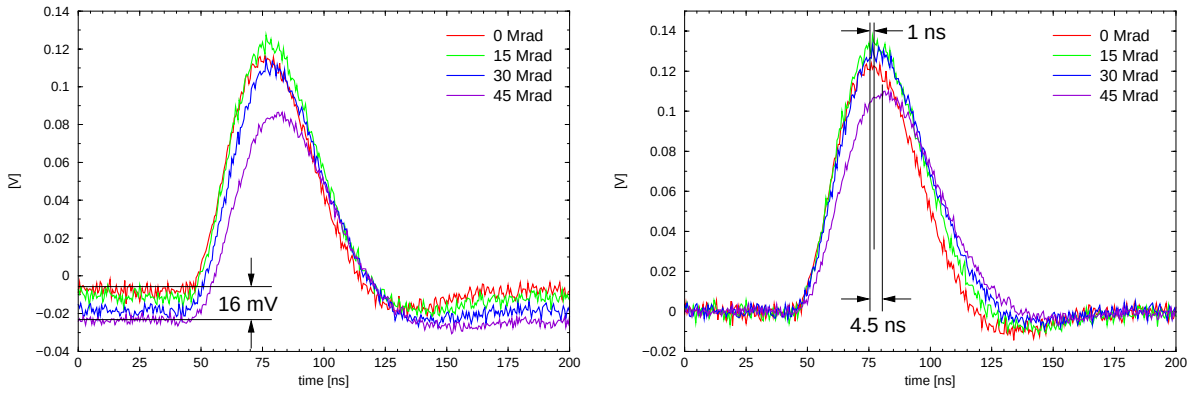


Figure 5.11: Pulse shape variation of chip *Beetle1.1*-R1 as a function of dose. In the right plot, the offset variation is corrected.

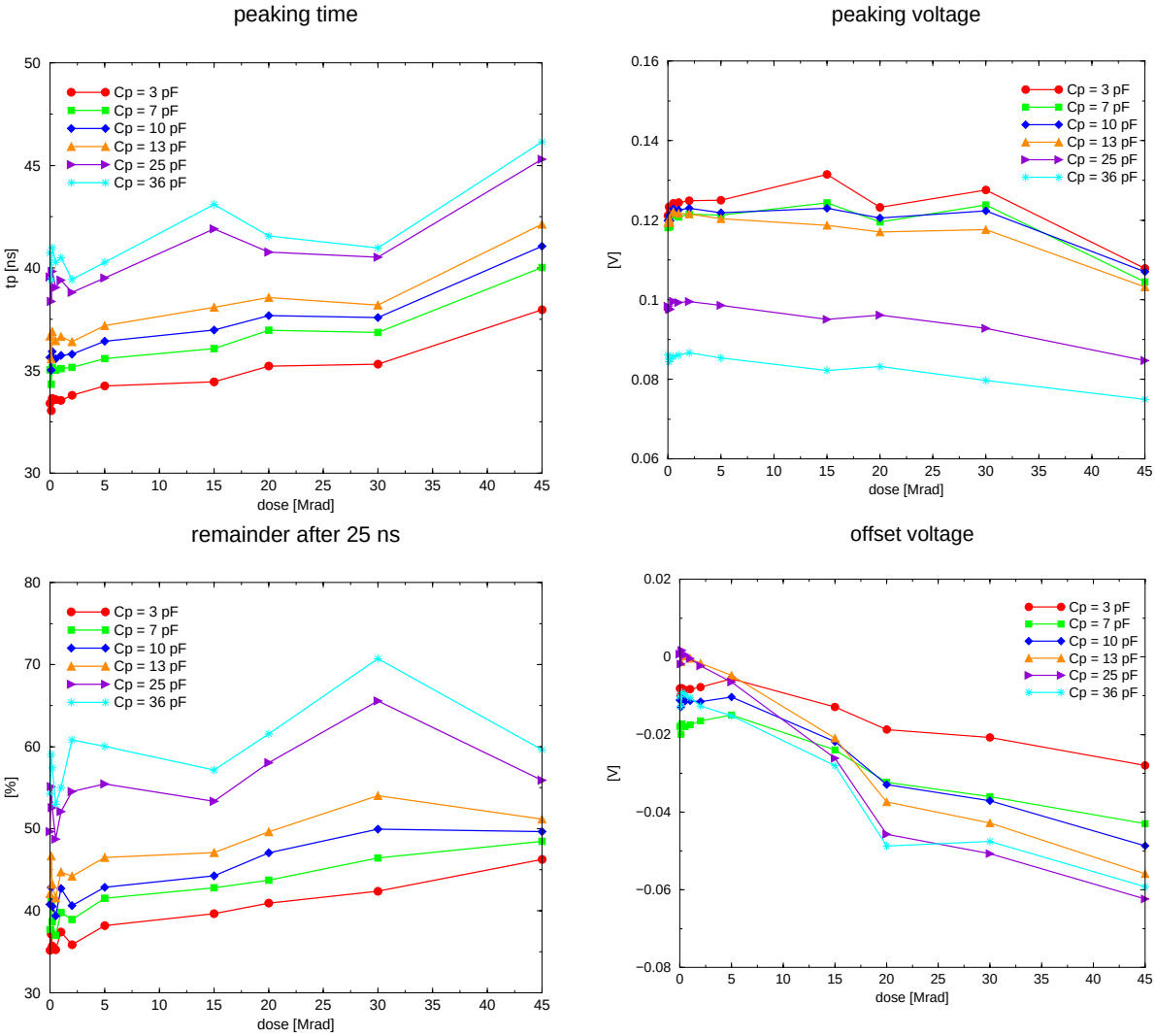


Figure 5.12: Peaking time, peaking voltage, pulse remainder and offset shift obtained from a pulse shape scan on *Beetle1.1* as a function of dose.

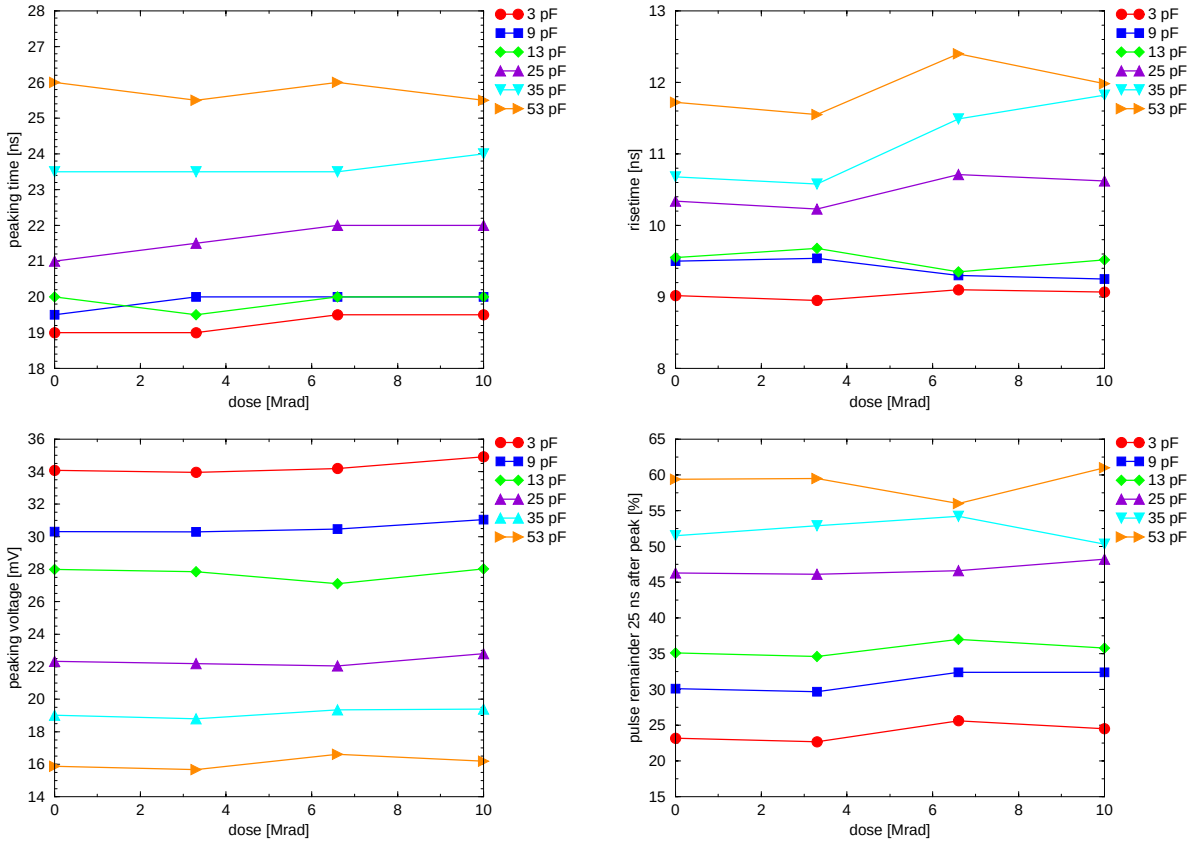


Figure 5.13: Peaking time, rise time, peaking voltage and pulse remainder of front-end set 2c on *BeetleFE1.1* as a function of dose [Löc03].

5.2.2 Single Event Upset Irradiation Test

In June 2002 an SEU irradiation test has been performed with the *BeetleSR1.0* chip at the accelerator facility of the Max-Planck Institute for Nuclear Physics in Heidelberg. The chip has been irradiated with 33 MeV alpha particles. Before detailing the test procedure, the device under test will be described briefly.

BeetleSR1.0

BeetleSR1.0 is a 2×2 mm^2 test chip submitted in May 2001 (see table 4.6). It integrates two types of I^2C-interfaces, a standard and an SEU robust one using triple redundant logic, and two memory blocks consisting of 34 8-bit registers each (fig. 5.14). The layout of the chip with the corresponding floor plan is shown in fig. 5.15. The registers forming the memory blocks use standard flip-flops without any redundancy.

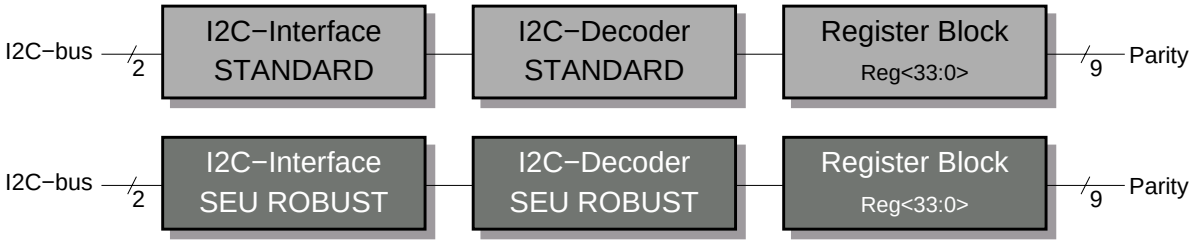


Figure 5.14: Block schematic of the *BeetleSR1.0* test chip.

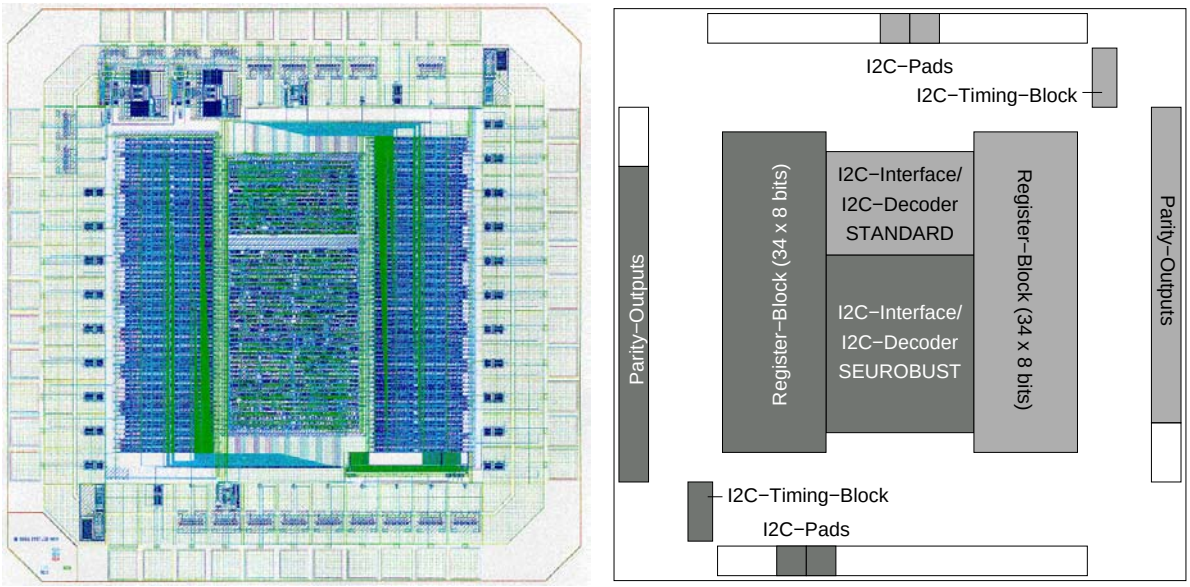


Figure 5.15: Layout (left) and floor plan (right) of the *BeetleSR1.0* test chip.

Each of the two interface circuits can be accessed via separate I^2C-ports. Nine parity bits per register block are generated, where 8 of them are the parity of 4 registers (`Parity[7:0]`)

and 1 the parity of 2 (`Parity[8]`). Information about a change in the register content can be obtained in two ways: either by reading the registers via I^2C-bus or by detecting a change of a parity bit.

Motivation and Measurement Procedure

The goals of the SEU irradiation test were

- a counting of the overall upsets in the two memory blocks,
- a comparison of the performance of the standard and SEU-robust interface circuits and
- a determination of the SEU-cross section for the flip-flop (D-flip-flop with asynchronous reset) used in the memories.

The measurement procedure foresaw a permanent read access to the I^2C-interfaces. A transmission error was interpreted as an upset in the logic. Additionally, changes in the parity bits were counted and directly revealed upsets in the memory contents. Test runs in the laboratory showed a stable and reliable operation of the I^2C-interfaces. In 24 hours with several 10^6 read operations no transmission errors occurred.

Irradiation Setup

In order to create a Single Event Upset in a sensitive volume of the circuit, a certain energy has to be deposited (cf. section 3.1.4). Taking a critical LET of $15\,\mathrm{MeVcm^2mg^{-1}}$ [Fac99a] the threshold for the stopping power in silicon ($\rho_{Si} = 2.33\,\mathrm{g/cm^3}$) is $dE/dx|_{crit} \approx 35\,\mathrm{MeV/cm}$. The Max-Planck Institute for Nuclear Physics (MPIK) provides an accelerator facility for protons and several ion species. For Helium ions a maximum kinetic energy of 33 MeV is achievable. 33 MeV Helium ions have a range in silicon of $\sim 500\,\mu\mathrm{m}$ and a mean energy loss of $\sim 400\,\mathrm{MeV/cm}$ (see fig. 5.16).

Taking an SEU cross section per bit of $\sigma = 2 \times 10^{-16}\mathrm{cm^2}$ [Fac02], the number of bits N$\sim$ 500 and a beam current of 3 nA focused to $1\,\mathrm{cm^2}$, the rate of Single Event Upsets created by He^{2+}-ions is estimated to $\sim 1\,\mathrm{mHz}$.

The setup was located at the *L5* beam line of MPIK's tandem accelerator. The *BeetleSR1.0* chip was positioned on a frame behind a silicon strip sensor, an aperture of 2.5 mm diameter and three thin metal foils (fig. 5.17). This composition was mounted on a movable platform and positioned inside a vacuum vessel. The task of the silicon strip sensor and the metal foils were a determination of the particle flux.

The material, which the alpha particles have to pass before they impinge on the chip is approximately $10\,\mu$m (Si) + $10\,\mu$m (Fe) + $12\,\mu$m (Ni) + $10\,\mu$m. The latter figure is the material on the chip above the SEU-sensitive silicon volume, estimated from the manufacturer's process data to $\approx 10\,\mu$m (a sequence of poly-crystalline silicon, SiO_2, aluminium, oxide nitride and polyimide).

Outcome

Two chips were irradiated in succession at a beam current varying between 3 nA and 14 nA. Both irradiated chips showed strong malfunctions due to irradiation. The current consumption dropped for both chips from about 20 mA before irradiation to < 0.1 mA afterwards. The SEU robust interface of chip 1 was not addressable any more and the memory linked to the standard interface showed varying contents. On chip 2, the parity outputs were oscillating after irradiation. The I^2C-transmission line for chip 2 showed permanent errors from the beginning of installation, i.e. also before irradiation. This prevented a comparison of the performance of the two interface circuits. A too large beam current probably destroyed the chips by heating, which could explain the drop of the power consumption to nearly 0.

Several drawbacks have been identified after the irradiation period: the positioning of the setup-platform with a stepping motor was underlying large uncertainties and a misalignment between the aperture and the chip existed, which led to an inhomogeneous irradiation of the chip area.

Nevertheless, there was a period of ~ 4 hours, where useful data was acquired. In total 128 upsets in the registers of the two memories of chip 2 were detected by counting the number of parity changes. The distribution of upsets showed a left-right asymmetry between the two memories, which results from the misalignment of aperture and chip. The left memory (linked to the SEU-robust interface) showed 126 upsets, while the right memory (linked to the standard interface) was subject to 2 bit flips (cf. fig. 5.15). From the quoted numbers an average upset rate of ~ 9 mHz results. This compares well to the estimated number of 1 mHz for a beam current of 3 nA. The beam current for the data taking period was around 8 nA.

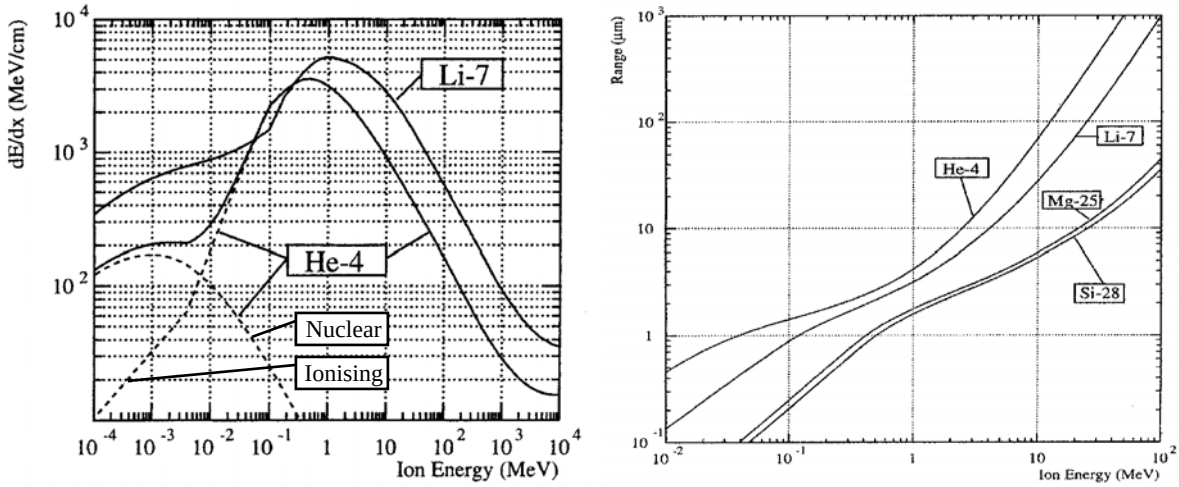


Figure 5.16: Left: Energy loss of helium (and lithium) ions in silicon ($\rho = 2.33\,g/cm^3$) as a function of kinetic energy. Right: Range of helium (and some other) ions in silicon as a function of kinetic energy [Huh00].

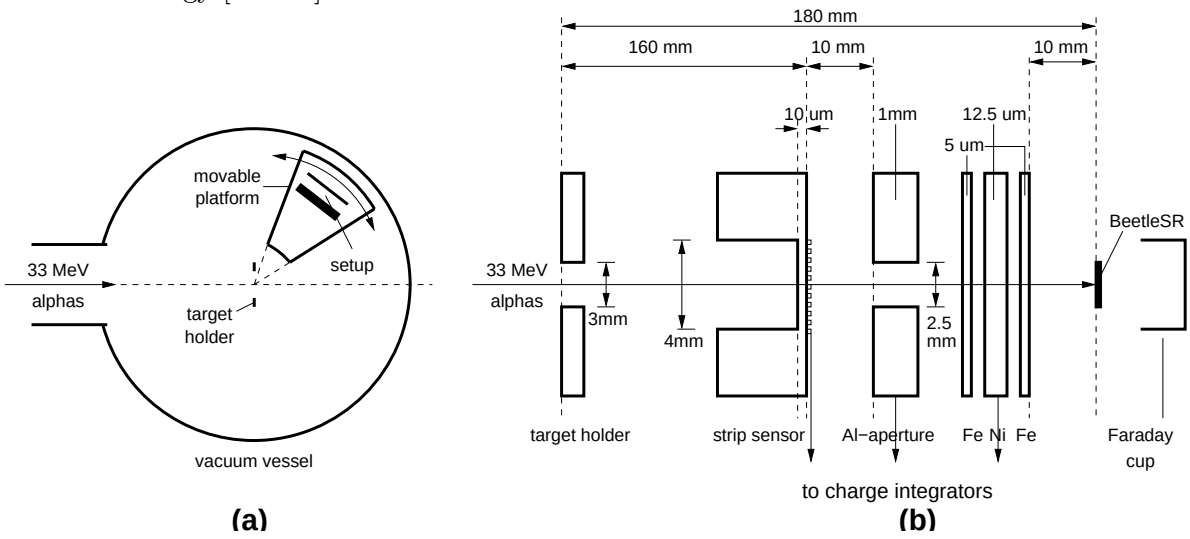


Figure 5.17: Scheme of the SEU irradiation setup for *BeetleSR1.0*. (a) Top view on the vacuum vessel with the target holder and the movable platform carrying the setup. (b) Arrangement of silicon sensor, aperture, metal foils and chip.

Chapter 6

Summary

Conclusion

The *Beetle* readout chip provides an analogue or binary pipelined readout as well as prompt binary information of the front-end pulse discrimination which will be used in the pile-up VETO trigger. The choice of a deep-submicron process technology with a thin gate oxide ($t_{ox} \approx 62\,\text{Å}$) and the consistent use of enclosed NMOS transistors establishes a total ionising dose radiation hardness in excess of 45 Mrad. CMOS latch-up is suppressed due to the implementation of guard-rings. The continuous use of triple-redundant logic ensures a robustness against Single Event Upset, which has become a major concern in all LHC experiments. The analogue memory enables a maximum trigger latency of $4\,\mu$s or 160 sampling clock intervals. Up to 16 consecutive events can be read out without dead-time. The control circuitry consistently using SEU-robust flip-flops showed a stable operation with periodical as well as random triggers.

In the context of this work, the following contributions have been made:

- a programming interface compatible with the I^2C-standard, which allows the use of commercial devices to control the *Beetle* chip,
- a decoder logic for the *Beetle* registers, which enables write and read operations. A pointer mechanism allows the consecutive access to registers without addressing each register separately,
- the readout control logic has been adapted from the HELIX128 chip to the requirements of the LHCb experiment,
- a scheme has been developed and implemented, which ensures the robustness against Single Event Upsets. The use of triple-redundant logic featuring a self-correction in parts of the circuitry has been favoured compared to a Hamming EDC code implementation,
- the analogue memory making use of MOS gate-capacitances together with the corresponding readout amplifier (pipeamp) has been designed,
- the *Beetle1.1* chip has been irradiated up to 45 Mrad and characterised concerning pulse shaping, noise and digital functionality,
- beside three iterations of the readout chip (*Beetle1.0–1.2*), a test-chip (*BeetleSR1.0*) has been developed, which was intended to characterise the robustness of the circuitry against

SEU. An irradiation test with a 33 MeV α-particle beam has been performed with this chip.

The latest version of the *Beetle* readout chip (*Beetle1.2*) fulfils all the requirements of the VELO, the inner tracker (ITR) and the RICH detectors of LHCb, as well as the front-end electronics specifications of LHCb. The front-end's equivalent noise charge is

$$\mathrm{ENC} = 497\,\mathrm{e}^- + 48.3\,\mathrm{e}^-/\mathrm{pF} \cdot \mathrm{C}_{in}.$$

Beetle1.1 has been integrated on a 16-chip hybrid module and operated successfully in a test-beam with a silicon sensor attached to it's inputs.

Outlook

The robustness of the logic circuitry of *Beetle1.2* against SEU has to be proven in a particle beam. The on-chip counter for Single Event Upsets together with the possibility to read the register contents via $\mathrm{I}^2\mathrm{C}$-bus, provides an easy method to detect and identify upsets in the chip registers. An SEU in the control logic will most probably lead to a malfunction in the readout and can be detected by monitoring the chip's latency and the pipeline column number together with the header information bits. Also operating two or several chips in parallel and checking the synchronicity can be used to identify upsets in the control logic.

The performance of *Beetle1.2* under total ionising dose irradiation should be shown beyond 50 Mrad to reveal the limits of the technology.

Despite the good pulse shaping and noise performance of *Beetle1.2* two major deficiencies remain: the behaviour at consecutive triggers and the variation of the readout baseline. A further chip iteration is planned for February 2003, which will overcome these drawbacks. Due to the expected high chip yield of $> 75\%$, a chip production will result in about 45,000 perfect chips, i.e. chips with no dead channel or pipeline cell.

Appendix A

The Beetle Reference Manual v1.1

LHCb 2001-046
ELECTRONICS
April 30, 2002

The Beetle Reference Manual

— chip version 1.1 —

NIELS VAN BAKEL[1], DANIEL BAUMEISTER[2] [1], MARTIN VAN BEUZEKOM[1], JO VAN DEN BRAND[1], MARTIN FEUERSTACK-RAIBLE[6], NEVILLE HARNEW[3], WERNER HOFMANN[2], EDDY JANS[1], SANDER KLOUS[1], KARL-TASSO KNÖPFLE[2], SVEN LÖCHNER[2] [2], MICHAEL SCHMELLING[2], EDGAR SEXAUER[5], NIGEL SMALE[3], ULRICH TRUNK[4], HANS VERKOOIJEN[1]
— [1]NIKHEF / FREE UNIVERSITY AMSTERDAM —
[2]MAX-PLANCK-INSTITUTE FOR NUCLEAR PHYSICS, HEIDELBERG —
[3]UNIVERSITY OF OXFORD —
[4]PHYSICS INSTITUTE, UNIVERSITY OF HEIDELBERG —
[5] NOW AT DIALOG SEMICONDUCTORS, KIRCHHEIM-NABERN, GERMANY
[6] NOW AT FUJITSU MIKROELEKTRONIK GMBH, DREIEICH-BUCHSCHLAG, GERMANY

revised version

This paper details the port definitions, electrical specifications, modes of operation and programming sequences of the 128 channel readout chip *Beetle*. It refers to the chip versions 1.0 and 1.1 which are except bug fixes identical. The chip is developed for the LHCb experiment and fulfils the requirements of the silicon vertex detector, the inner tracker, the pile-up veto trigger and the RICH detector in case of multi-anode photomultiplier readout. It integrates 128 channels with low-noise charge-sensitive preamplifiers and shapers. The risetime of the shaped pulse is 25 ns with a 30% remainder of the peak voltage after 25 ns. A comparator per channel with configurable polarity provides a binary signal. Four adjacent comparator channels are being ORed and brought off chip via LVDS ports. Either the shaper or comparator output is sampled with the LHC-bunch-crossing frequency of 40 MHz into an analogue pipeline with a programmable latency of max. 160 sampling intervals and an integrated derandomising buffer of 16 stages. For analogue readout data is multiplexed with up to 40 MHz onto 1 or 4 ports. A binary readout mode operates at up to 80 MHz output rate on two ports. Current drivers bring the serialised data off chip. The chip can accept trigger rates of up to 1 MHz to perform a dead-timeless readout within 900 ns per sample. For testability and calibration purposes, a charge injector with adjustable pulse height is implemented. The bias settings and various other parameters can be controlled via a standard I^2C-interface.

[1]Email: baumeis@asic.uni-heidelberg.de
[2]Email: loechner@asic.uni-heidelberg.de

Contents

A.1 Document Edition History 124
A.2 Chip Version History 124
A.3 Chip Architecture 124
A.4 Electrical specifications 126
A.4.1 DC characteristics 126
A.4.2 Analogue output characteristics 126
A.5 Modes of operation 127
A.5.1 Reset modes 127
A.5.2 Readout modes 127
A.5.3 Operation in daisychain 128
A.5.4 Operation with internal testpulses 128
A.5.5 Comparator operation 129
A.6 Slow Control 130
A.6.1 I^2C-Interface 130
A.6.2 Bias and configuration registers 131
A.7 Pad Description 134
A.7.1 Front pads 134
A.7.2 Top pads 135
A.7.3 Bottom pads 136
A.7.4 Backside pads 137
A.8 List of known problems and bugs 139
A.8.1 Beetle1.0 139
A.8.2 Beetle1.1 139

A.1 Document Edition History

This manual describes the chip versions 1.0 and 1.1. It refers to *Beetle1.1* unless otherwise noted.

Version	Date	Author	Description
1.0	22.04.2001	DB, SL	document created
1.1	30.04.2002	DB, SL	errors fixed: input pad pitch is 40.24 μm, fig. A.11 modified receiver circuit schematic (fig. A.2) I^2C-general call sequence added to fig. A.9 description of internal testpulse operation added (sect. A.5.4) updated list of known problems and bugs

A.2 Chip Version History

Version	Submission Date	Changes relating to previous version
Beetle1.0	April 2000	
Beetle1.1	March 2001	test channel extended till pipeline readout amplifier (pipeamp) output modified pipeline layout analogue delay element for I^2C-SDA line added modified pipeamp modified bias network of pipeamp modified multiplexer modified tristate buffer in control circuit

A.3 Chip Architecture

The *Beetle* can be operated as analogue or alternatively as binary pipelined readout chip. It implements the basic RD20 front-end electronics architecture [1]. Fig. A.1 shows a schematic block diagram of the chip.

The chip integrates 128 channels. Each channel consists of a low-noise charge-sensitive preamplifier and an active CR-RC pulse shaper. The risetime of the shaped pulse is ≤ 25 ns, the spill-over left 25 ns after the peak at most 30%. A comparator per channel provides a binary signal. It features a configurable polarity and an individual threshold level. Four adjacent comparator channels are ORed together, latched, multiplexed by a factor of 2 and routed off the chip via low voltage differential signalling (LVDS) ports at 80 MHz. Either the shaper- or the comparator output is sampled with the LHC bunch-crossing frequency at 40 MHz into an analogue pipeline with a programmable latency of max. 160 sampling intervals and an integrated multi-event buffer of 16 stages. The signal stored in the pipeline is transfered to the multiplexer via a resetable charge-sensitive amplifier. Within a readout time of 900 ns current drivers bring the serialised data off chip. The output of a dummy channel is subtracted from the analogue data to compensate common mode effects. All amplifier stages are biased by forced

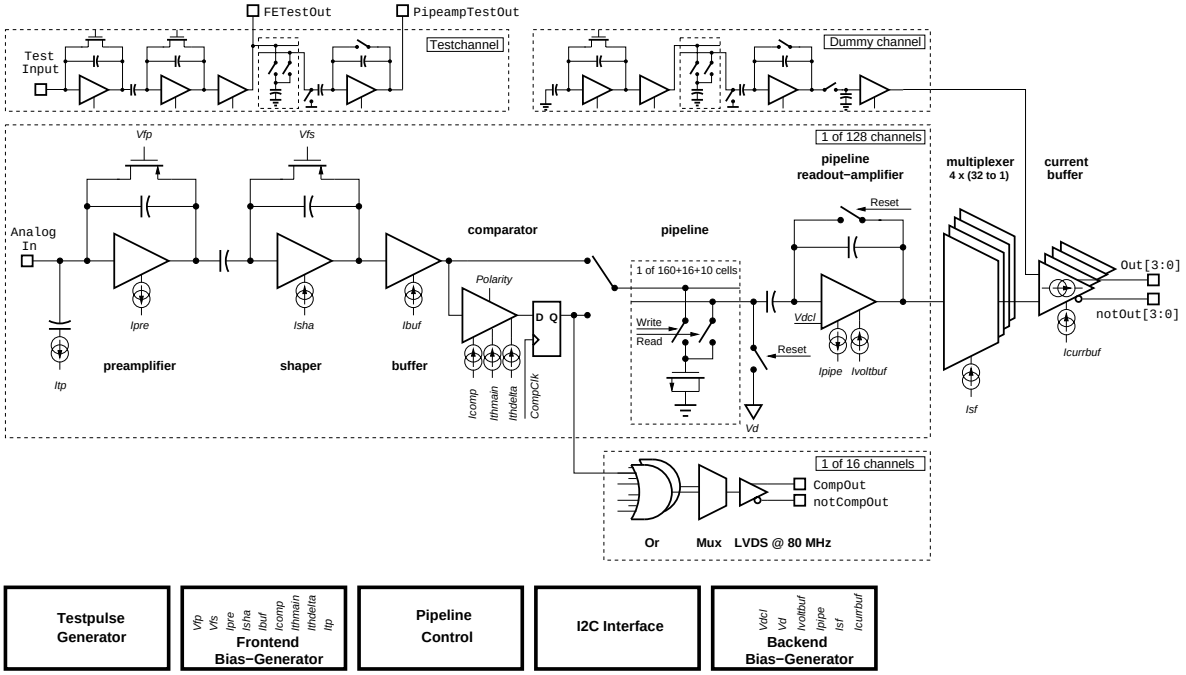


Figure A.1: Schematic block diagram of the *Beetle* readout chip.

currents. On-chip digital-to-analogue converters (DACs) with 10 bit resolution generate the bias currents and voltages. For test and calibration purposes a charge injector with adjustable pulse height is implemented on each channel. The bias settings and various other parameters like the trigger latency can be controlled via a standard I^2C-interface [3]. All digital control and data signals, except those for the I^2C-ports, are routed via LVDS ports.

The chip is fabricated in 0.25 μm standard CMOS technology and has a die size of (5.5×6.1) mm^2. The analogue input pads have a pitch of 40.24 μm. If no comparator outputs are used, pads on the sides of the chip do not need to be bonded. This allows an overall pitch of 50 μm when mounting the chips side by side.

A.4 Electrical specifications

A.4.1 DC characteristics

Supply	Min.[V]	Nom.[V]	Max. [V]	Description
Vdda	2.2	2.5	2.7	Positive analogue supply
Gnda	0	0	0	Negative analogue supply
Vddd	2.2	2.5	2.7	Positive digital supply
Gndd	0	0	0	Negative digital supply
VddPre	2.2	2.5	2.7	Positive preamplifier supply
Gnd	0	0	0	Detector ground
VddComp	2.2	2.5	2.7	Positive comparator output supply
GndComp	0	0	0	Negative comparator output supply

Table A.1: DC characteristics of *Beetle1.1*.

A.4.2 Analogue output characteristics

The output level of the analogue output driver is 46 mV ± 2.8 mV/MIP[3] measured over 56 Ω to ground. Fig. A.2 gives an example of a receiver circuit using the CLC400 transimpedance amplifier [2].

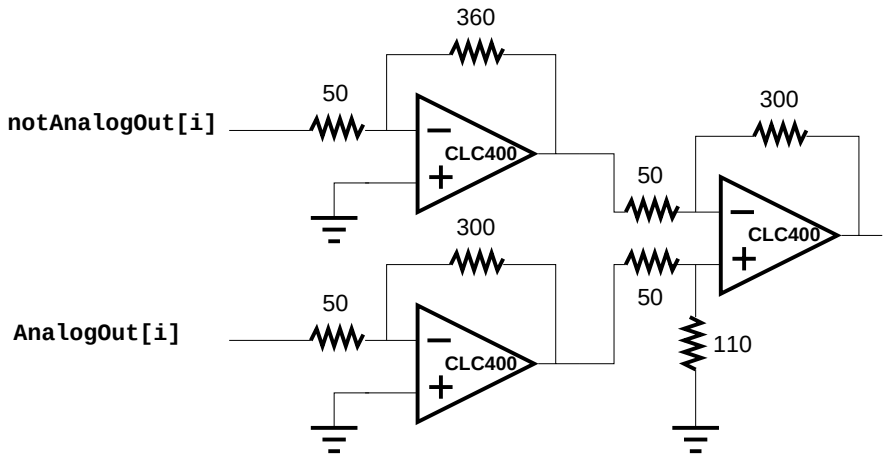


Figure A.2: Example of a receiver circuit for the analogue output signals using the CLC400 transimpedance amplifier.

[3] 1 MIP = 11,000 electrons in 150 μm silicon.

A.5 Modes of operation

A.5.1 Reset modes

Two different types of reset exist on *Beetle1.0* and *Beetle1.1*, which are differentiated by the duration of the active external reset with respect to the system clock. The external trigger port has to be inactive (i. e. `Trigger`=0, `notTrigger`=1) while applying `Reset`.

- Readout reset (cf. fig.A.3 a))
  It is generated by activating `Reset` for exactly 2 `Clock` cycles. It resets the Write- and Trigger pointers of the pipeline, removes all entries from the read-out fifo and stops any running read-out process immediately. The data currently submitted is lost.

- Power up reset (cf. fig.A.3 b))
  It is generated by activating `Reset` for 4 `Clock` cycles or longer. It resets all internal registers to default values. E. g. the DAC registers for the bias currents are set to 0 (no current). This is mainly to reduce power consumption during power up. Power up reset also switches the Beetle into the "Idle" state, i. e. the write pointer and the trigger pointer do not circulate and no triggers are accepted.

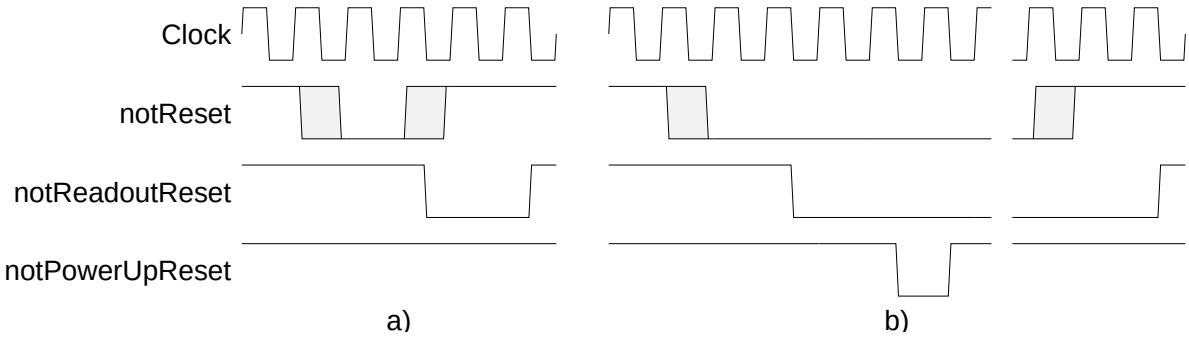


Figure A.3: Types of reset on *Beetle1.1*: a) Readout reset, b) Power up reset

A.5.2 Readout modes

Beetle1.1 provides three different readout modes:

1. Analogue readout in 900 ns on 4 ports

2. Binary readout in 900 ns on 2 ports

3. Analogue readout in 3.4 μs on 1 port (for applications with less demanding readout speed requirements).

Fig. A.4 - A.6 show the assignment of the header bits and analogue input channels to the output channels in the different modes. The readout timing behaviour is depicted in fig. A.7.

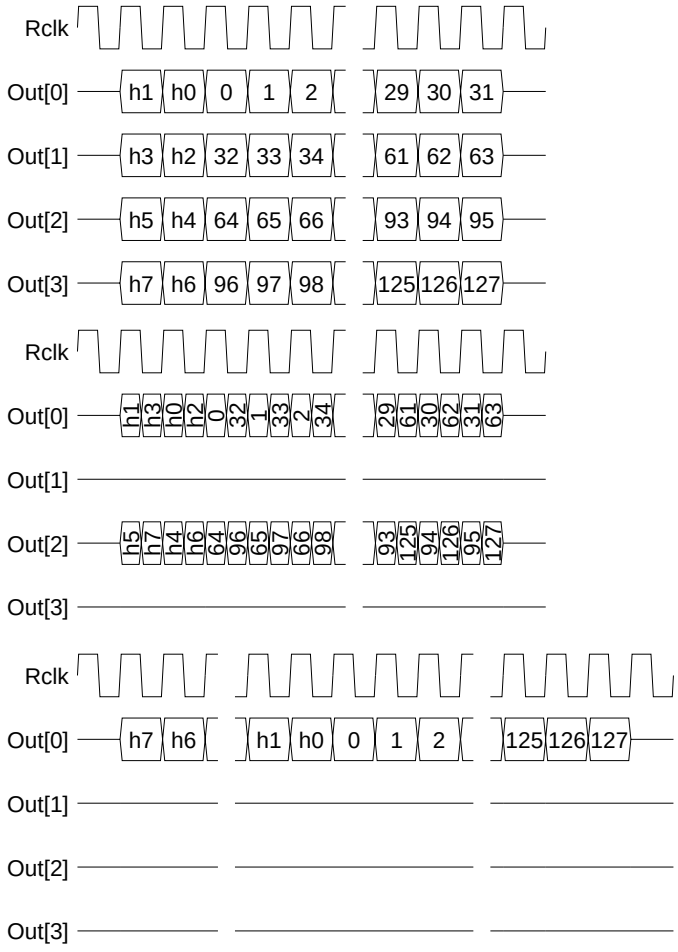


Figure A.4: Analogue readout mode: 32 analogue channels are multiplexed onto 4 ports with up to 40 MHz.

Figure A.5: Binary readout mode: 64 binary channels are multiplexed onto 2 ports with up to 80 MHz.

Figure A.6: Readout mode for less demanding readout speed requirements: 128 analogue channels are multiplexed onto 1 port with up to 40 MHz.

A.5.3 Operation in daisy chain

The token ports `T1A`, `T1B`, `T2A`, and `T2B` handle two tasks:

1. They form a daisy chain for generating the chip address for programming via the I^2C-interface.
2. They form a daisy chain for the read-out.

The daisy chain is built by connecting the `T1A` port to the `T2A` port of the neighbouring chip and connecting the `T1B` port to the `T2B` port of the next but the neighbouring chip (see fig. A.8).

A.5.4 Operation with internal test pulses

Test pulses can be injected into the preamplifier with an on-chip generator. A step like pattern corresponding to +2, +1, −1 and −2 times the input signal amplitude is coupled modulo 4 to the 128 channels. Via the `Testpulse` port a toggle flip-flop is triggered: an input pulse on this port generates a rising edge of the internal testpulse signal, a succeeding input pulse results in a falling edge of the testpulse. The amplitude of the injected pulse can be adjusted with the *Itp* bias registers (cf. table A.3).

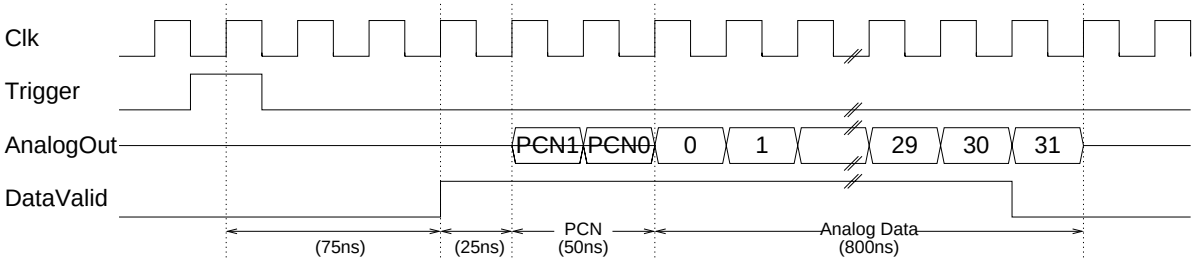


Figure A.7: Readout timing scheme.

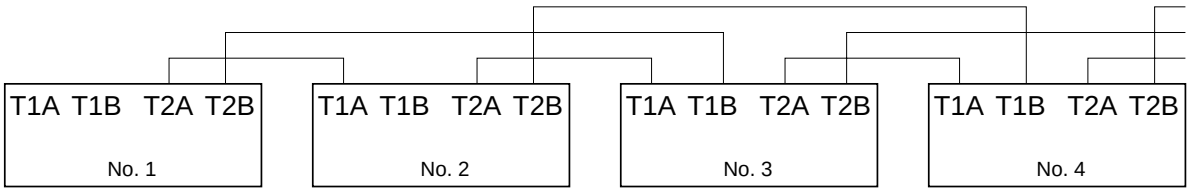


Figure A.8: Connection scheme of *Beetle* chips in a daisy chain.

A.5.5 Comparator operation

The comparator circuit consists of an integrator, a threshold generator and a discriminator. The integrator extracts the DC-offset of the shaped pulse with a time constant of 5 μs. This offset varies from channel to channel and is added to the threshold voltage. The threshold level is adjustable per channel with a resolution of 3 bits.

Comparator configuration

The comparator is configured via the register *CompControl* (see table A.3 and fig. A.11). *CompOutMode* defines the mode of operation of the comparator. *CompOutMode*=0 selects the analogue mode, in which the output of the front-end amplifier is transferred to the pipeline. In binary mode (*CompOutMode*=1) the comparator output is fed into the pipeline. *CompDisable*=1 turns off the comparator's bias current. *CompPolarity* selects between an inverting (0) or non-inverting (1) comparator operation. *CompMode* switches between two different kinds of output signal. With *CompMode*=0 the output is as long active as the comparator input signal is above the threshold level. With *CompMode*=1 the output is only one CompClk cycle active, independent of the time, which the input signal is above the threshold.

Threshold adjustment

The threshold level is generated from two programmable currents. *Ithmain* (register addresses 2 and 3) determines the global threshold, which is common to all channels. *Ithdelta* (register addresses 0 and 1) defines an additional delta voltage. The 3 MSBs of the configuration register *CompControl* `ThDelta[2:0]` (fig. A.11) select the number of delta voltages which are being added to the global threshold voltage. `ThDelta[2:0]` is adjustable per channel. To define the delta threshold voltage of all channels, the *CompControl* register has to be programmed 128

times consecutively. A shift mechanism provides the bits to the channels in the order Ch[0], Ch[1], ..., Ch[127].

Comparator channel mapping

The comparator outputs are LVDS drivers. Each driver sends data of two combined comparator groups, the first group during the high phase of `Clk`, the second during the low phase. The mapping of the channels to the comparator outputs is shown in table A.2.

CompOut No.	High phase of Clk	Low phase of Clk
CompOut[15]	Ch[127], Ch[126], Ch[125], Ch[124]	Ch[123], Ch[122], Ch[121], Ch[120]
CompOut[14]	Ch[119], Ch[118], Ch[117], Ch[116]	Ch[115], Ch[114], Ch[113], Ch[112]
CompOut[13]	Ch[111], Ch[110], Ch[109], Ch[108]	Ch[107], Ch[106], Ch[105], Ch[104]
CompOut[12]	Ch[103], Ch[102], Ch[101], Ch[100]	Ch[99], Ch[98], Ch[97], Ch[96]
CompOut[11]	Ch[95], Ch[94], Ch[93], Ch[92]	Ch[91], Ch[90], Ch[89], Ch[88]
CompOut[10]	Ch[87], Ch[86], Ch[85], Ch[84]	Ch[83], Ch[82], Ch[81], Ch[80]
CompOut[9]	Ch[79], Ch[78], Ch[77], Ch[76]	Ch[75], Ch[74], Ch[73], Ch[72]
CompOut[8]	Ch[71], Ch[70], Ch[69], Ch[68]	Ch[67], Ch[66], Ch[65], Ch[64]
CompOut[7]	Ch[63], Ch[62], Ch[61], Ch[60]	Ch[59], Ch[58], Ch[57], Ch[56]
CompOut[6]	Ch[55], Ch[54], Ch[53], Ch[52]	Ch[51], Ch[50], Ch[49], Ch[48]
CompOut[5]	Ch[47], Ch[46], Ch[45], Ch[44]	Ch[43], Ch[42], Ch[41], Ch[40]
CompOut[4]	Ch[39], Ch[38], Ch[37], Ch[36]	Ch[35], Ch[34], Ch[33], Ch[32]
CompOut[3]	Ch[31], Ch[30], Ch[29], Ch[28]	Ch[27], Ch[26], Ch[25], Ch[24]
CompOut[2]	Ch[23], Ch[22], Ch[21], Ch[20]	Ch[19], Ch[18], Ch[17], Ch[16]
CompOut[1]	Ch[15], Ch[14], Ch[13], Ch[12]	Ch[11], Ch[10], Ch[9], Ch[8]
CompOut[0]	Ch[7], Ch[6], Ch[5], Ch[4]	Ch[3], Ch[2], Ch[1], Ch[0]

Table A.2: Mapping of analogue input channels to comparator output channels on *Beetle1.1*.

A.6 Slow Control

A.6.1 I^{2}C-Interface

The chip's slow control interface is a standard mode I^{2}C-slave device performing a transfer rate of 100 kbit/s. The chip address, necessary to access a single device via the I^{2}C-bus, is assigned in a self-programming procedure on power-up using a daisy chain of several chips (cf. section A.5.3).

The internal registers are being accessed via a *pointer register*. This contains the address of the register to be written or read first. The pointer is internally incremented by 1 after each transferred data frame. In this way registers with adjacent addresses can be accessed consecutively. The pointer register itself remains unchanged, i.e. a new transfer will start at the same pointer position. Fig. A.9 explains the transfer sequences in write and read mode. Data is always transferred with the most significant bit (MSB) first. In write mode the chip address is transmitted after initialising the transfer, followed by the pointer byte and the data. After the transmission of one data frame, the pointer addresses the successive register because

of its auto-incrementing function. A 10 bit register allocates 2 addresses in the address space. The MSBs (D[9:2]) occupy the lower address (cf. table A.3). The transfer of the pointer byte is obligatory in write mode. In read mode there are two versions:

- Preset pointer
  After initialising the transfer and sending the chip address data is immediately read out. The pointer has been set in a previous transfer.

- Pointer set followed by immediate read-out
  After initialising the transfer and sending the chip address the pointer byte is transferred. The I^{2}C-bus is re-initialised, the chip address is sent and data is read out.

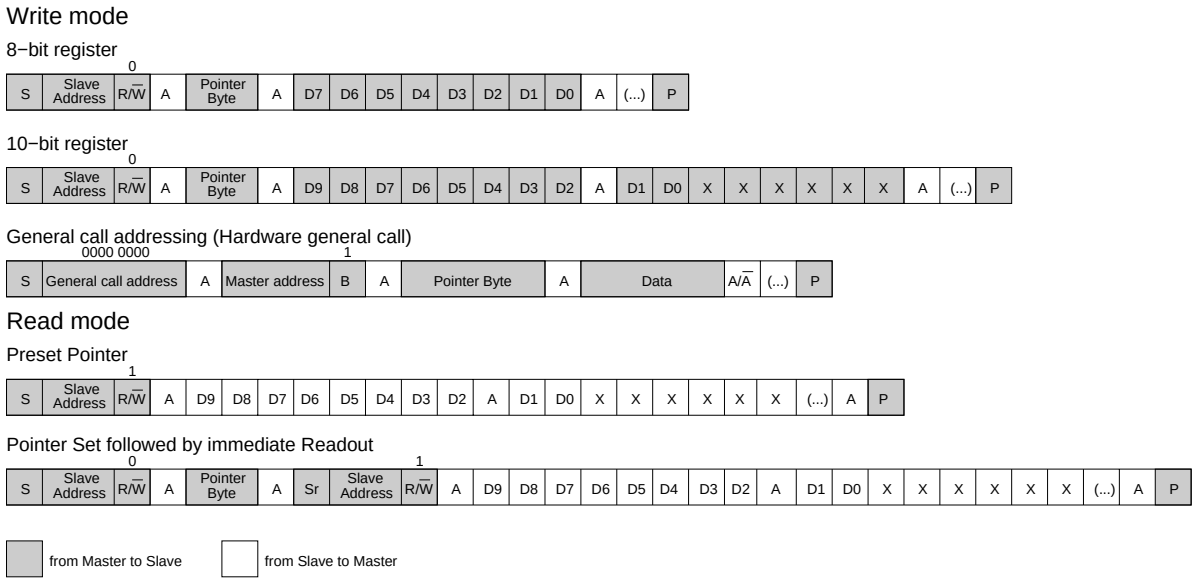


Figure A.9: I^{2}C-bus write and read sequences for accessing registers on the *Beetle*.

Commercially available I^{2}C-devices usually operate at 3.3 V or 5 V. To interconnect these devices with a *Beetle* I^{2}C-interface a bidirectional level shifter is necessary. A simple solution to this problem is the use of a discrete MOS-FET for each bus line [4]. Fig. A.10 illustrates the level shifter circuit. An example for a single MOS-FET device is type BSN20 from Philips Semiconductors.

A.6.2 Bias and configuration registers

Beetle1.0 and *Beetle1.1* contain 34 8-bit registers with the addresses $0-32$ and 37. The register addresses $33-36$ are presently not used but reserved for future purposes. Table A.3 lists all registers with their nominal value and register content. A LSB corresponds to 0.977 μA for currents and 2.44 mV for voltages. Registers $0-29$ are bias registers for the analogue stages. Register 30 defines the latency which has to be ≥ 10 for reasonable chip operation. After changing the latency it is mandatory to apply a *Readout Reset* to the chip. Register 32 defines the ratio between the readout clock `Rclk` and the sampling clock `Sclk`. Each LSB reduces

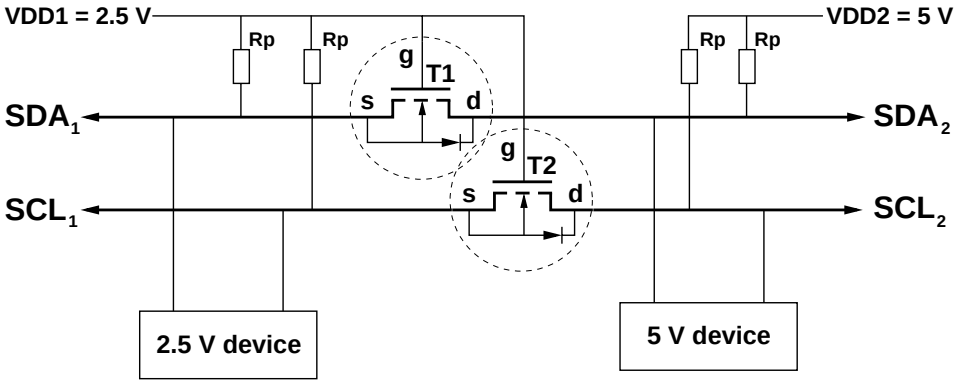
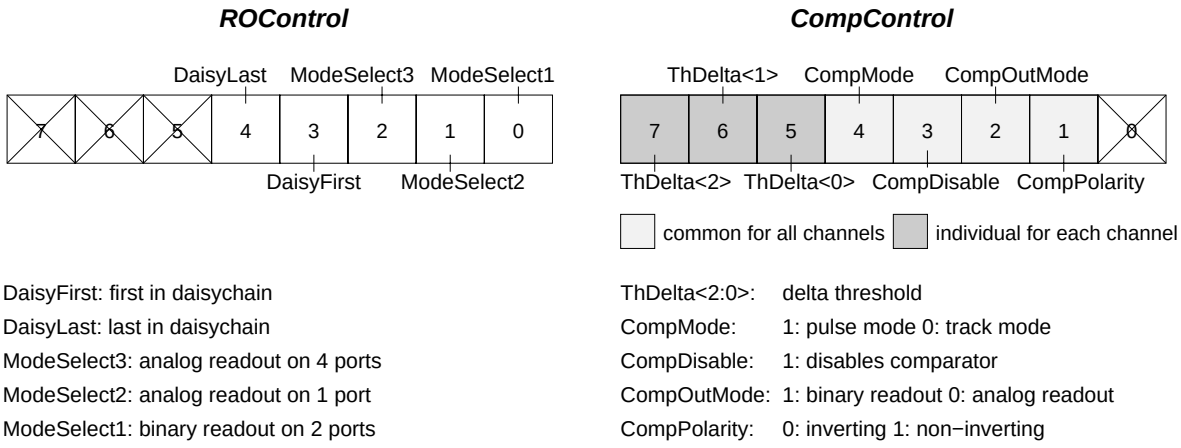


Figure A.10: Bidirectional level shifter circuit to connect two different voltage level sections of an I^2C-bus system. An example for a single MOS-FET device is type BSN20 from Philips Semiconductors.

the frequency of `Rclk` with respect to `Sclk` by a factor of 2. The register value is modulo 8, a 0 means, that `Sclk` and `Rclk` have the same frequency. The registers 31 and 37 select the chip's mode of operation (readout mode, daisy chain configuration) and define the comparator configuration. Fig. A.11 shows the detailed bit assignment of the registers *ROControl* and *CompControl*.



DaisyFirst: first in daisychain
DaisyLast: last in daisychain
ModeSelect3: analog readout on 4 ports
ModeSelect2: analog readout on 1 port
ModeSelect1: binary readout on 2 ports

ThDelta<2:0>: delta threshold
CompMode: 1: pulse mode 0: track mode
CompDisable: 1: disables comparator
CompOutMode: 1: binary readout 0: analog readout
CompPolarity: 0: inverting 1: non−inverting

Figure A.11: Bit assignment of the configuration registers *ROControl* and *CompControl*. All switches are active-high. 1 enables the switch, 0 disables it.

Register Address	Register Name	Nominal Value	Register content
0	Ithdelta MSBs		0x00
1	Ithdelta LSBs	3.2 μA	0xC0
2	Ithmain MSBs		0x01
3	Ithmain LSBs	4 μA	0x00
4	Icomp MSBs		0x0A
5	Icomp LSBs	40 μA	0x80
6	Ibuf MSBs		0x14
7	Ibuf LSBs	80 μA	0x80
8	Isha MSBs		0x14
9	Isha LSBs	80 μA	0x80
10	Ipre MSBs		0x99
11	Ipre LSBs	600 μA	0x80
12	Itp MSBs		0x00
13	Itp LSBs	0 μA	0x00
14	Vfs MSBs		0x33
15	Vfs LSBs	500 mV	0x40
16	Vfp MSBs		0x00
17	Vfp LSBs	0 V	0x00
18	Icurrbuf MSBs		0x19
19	Icurrbuf LSBs	100 μA	0x80
20	Isf MSBs		0x33
21	Isf LSBs	200 μA	0x40
22	Ipipe MSBs		0x19
23	Ipipe LSBs	100 μA	0x80
24	Ivoltbuf MSBs		0x99
25	Ivoltbuf LSBs	600 μA	0x80
26	Vdcl MSBs		0x66
27	Vdcl LSBs	1 V	0x80
28	Vd MSBs		0x70
29	Vd LSBs	1.1 V	0xC0
30	Latency	160	0xA0
31	ROControl	cf. fig A.11	0x1C
32	RclkDivider	0	0x00
37	CompControl	cf. fig A.11	0x0A

Table A.3: Bias and configuration registers of *Beetle1.1*. Register addresses 33-36 are presently not used but reserved for future purposes.

A.7 Pad Description

A reference number has been assigned to each pad. The numbering starts in the upper left corner of the die (with the analogue input pads left) and runs counterclockwise (cf. fig.A.12). The following tables summarise the signals and explain them.

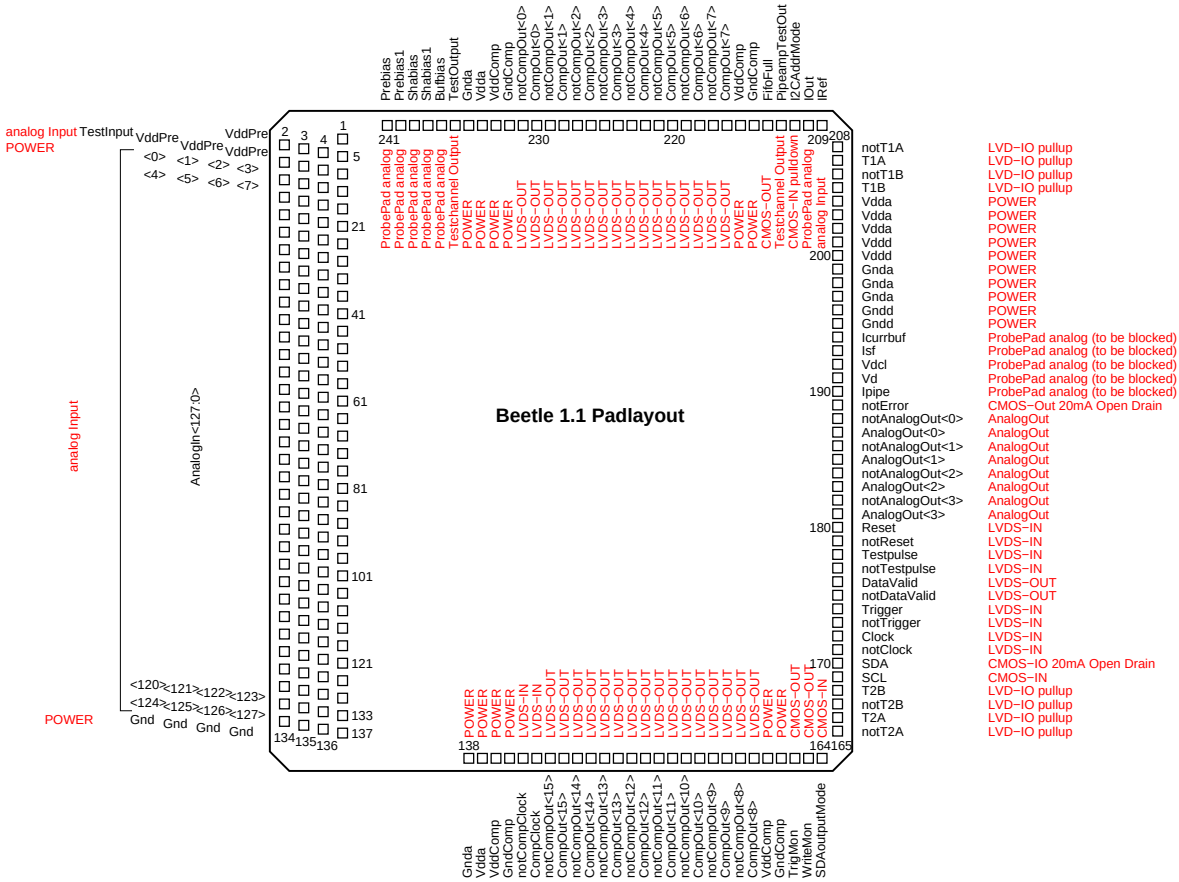


Figure A.12: Pad layout of *Beetle1.1*. The die size is $(5.5 \times 6.1)\,\mathrm{mm}^2$.

A.7.1 Front pads

Ref.no.	Pin name	Type	Description
1	`VddPre`	input	positive preamplifier supply
2	`TestInput`	input	input of test channel
3 - 5	`VddPre`	input	positive preamplifier supply
6	`AnalogIn<0>`	input	input of channel 0
7	`AnalogIn<1>`	input	input of channel 1
⋮	⋮	⋮	⋮
133	`AnalogIn<127>`	input	input of channel 127
134 - 137	`Gnd`	input	detector ground

A.7.2 Top pads

Ref.no.	Pin name	Type	Description
241	Prebias	output	analogue probe pad
240	Prebias1	output	analogue probe pad
239	Shabias	output	analogue probe pad
238	Shabias1	output	analogue probe pad
237	Bufbias	output	analogue probe pad
236	TestOutput	output	front-end output of test channel
235	Gnda	input	negative analogue supply
234	Vdda	input	positive analogue supply
233	VddComp	input	positive comparator supply
232	GndComp	input	negative comparator supply
231	notCompOut<0>	LVDS output	comparator output channel 0
230	CompOut<0>	LVDS output	comparator output channel 0
229	notCompOut<1>	LVDS output	comparator output channel 1
228	CompOut<1>	LVDS output	comparator output channel 1
227	notCompOut<2>	LVDS output	comparator output channel 2
226	CompOut<2>	LVDS output	comparator output channel 2
225	notCompOut<3>	LVDS output	comparator output channel 3
224	CompOut<3>	LVDS output	comparator output channel 3
223	notCompOut<4>	LVDS output	comparator output channel 4
222	CompOut<4>	LVDS output	comparator output channel 4
221	notCompOut<5>	LVDS output	comparator output channel 5
220	CompOut<5>	LVDS output	comparator output channel 5
219	notCompOut<6>	LVDS output	comparator output channel 6
218	CompOut<6>	LVDS output	comparator output channel 6
217	notCompOut<7>	LVDS output	comparator output channel 7
216	CompOut<7>	LVDS output	comparator output channel 7
215	VddComp	input	positive comparator supply
214	GndComp	input	negative comparator supply
213	FifoFull	CMOS output	indicates full derandomising buffer
212	PipeampTestOut	output	analogue probe pad: pipeamp output of test channel
211	I2CAddrMode	CMOS input (pull-down)	selects between 7-bit and 10-bit I^2C-address (default: 7-bit address)
210	IOut	output	analogue probe pad
209	IRef	input	reference current for current source

A.7.3 Bottom pads

Ref.no.	Pin name	Type	Description
138	Gnda	input	negative analogue supply
139	Vdda	input	positive analogue supply
140	VddComp	input	positive comparator supply
141	GndComp	input	negative comparator supply
142	notCompClock	LVDS input	comparator clock
143	CompClock	LVDS input	comparator clock
144	notCompOut<15>	LVDS output	comparator output channel 15
145	CompOut<15>	LVDS output	comparator output channel 15
146	notCompOut<14>	LVDS output	comparator output channel 14
147	CompOut<14>	LVDS output	comparator output channel 14
148	notCompOut<13>	LVDS output	comparator output channel 13
149	CompOut<13>	LVDS output	comparator output channel 13
150	notCompOut<12>	LVDS output	comparator output channel 12
151	CompOut<12>	LVDS output	comparator output channel 12
152	notCompOut<11>	LVDS output	comparator output channel 11
153	CompOut<11>	LVDS output	comparator output channel 11
154	notCompOut<10>	LVDS output	comparator output channel 10
155	CompOut<10>	LVDS output	comparator output channel 10
156	notCompOut<9>	LVDS output	comparator output channel 9
157	CompOut<9>	LVDS output	comparator output channel 9
158	notCompOut<8>	LVDS output	comparator output channel 8
159	CompOut<8>	LVDS output	comparator output channel 8
160	VddComp	input	positive comparator supply
161	GndComp	input	negative comparator supply
162	TrigMon	CMOS output	indicates if pipeline trigger pointer passes column 0
163	WriteMon	CMOS output	indicates if pipeline write pointer passes column 0
164	SDAoutputMode	CMOS input (pull-up)	selects between an analogue or digital SDA-line delay stage (default: analogue stage)

A.7.4 Backside pads

Ref.no.	Pin name	Type	Description
208	notT1A	LVDS input/output	Token for address/readout daisy chain
207	T1A	LVDS input/output	Token for address/readout daisy chain
206	notT1B	LVDS input/output	Token for address/readout daisy chain
205	T1B	LVDS input/output	Token for address/readout daisy chain
204	Vdda	input	positive analogue supply
203	Vdda	input	positive analogue supply
202	Vdda	input	positive analogue supply
201	Vddd	input	positive digital supply
200	Vddd	input	positive digital supply
199	Gnda	input	negative analogue supply
198	Gnda	input	negative analogue supply
197	Gnda	input	negative analogue supply
196	Gndd	input	negative digital supply
195	Gndd	input	negative digital supply
194	Icurrbuf	output	analogue probe pad (to be blocked)
193	Isf	output	analogue probe pad (to be blocked)
192	Vdcl	output	analogue probe pad (to be blocked)
191	Vd	output	analogue probe pad (to be blocked)
190	Ipipe	output	analogue probe pad (to be blocked)
189	notError	CMOS output	on chip error signal
188	notAnalogOut<0>	output	analogue output channel 0
187	AnalogOut<0>	output	analogue output channel 0
186	notAnalogOut<1>	output	analogue output channel 1
185	AnalogOut<1>	output	analogue output channel 1
184	notAnalogOut<2>	output	analogue output channel 2
183	AnalogOut<2>	output	analogue output channel 2
182	notAnalogOut<3>	input	analogue output channel 3
181	AnalogOut<3>	input	analogue output channel 3
180	Reset	LVDS input	system reset
179	notReset	LVDS input	system reset
178	Testpulse	LVDS input	test pulse
177	notTestpulse	LVDS input	test pulse
176	DataValid	LVDS output	indicates presence of valid data on AnalogOut
175	notDataValid	LVDS output	indicates presence of valid data on AnalogOut
174	Trigger	LVDS input	trigger
173	notTrigger	LVDS input	trigger

Ref.no.	Pin name	Type	Description
172	Clock	LVDS input	system clock
171	notClock	LVDS input	system clock
170	SDA	CMOS input/output (open-drain)	I^2C-bus data port
169	SCL	CMOS input	I^2C-bus clock port
168	T2B	LVDS input/output	Token for address/readout daisy chain
167	notT2B	LVDS input/output	Token for address/readout daisy chain
166	T2A	LVDS input/output	Token for address/readout daisy chain
165	notT2A	LVDS input/output	Token for address/readout daisy chain

A.8 List of known problems and bugs

A.8.1 Beetle1.0

The chip has to be patched e.g. with a focused ion beam to be functional. This is due to an error in the tristate buffers inside the control circuit. In addition the following errors occurred:

1. charge injection of transmission gate inside pipeline readout amplifier and multiplexer
2. insufficient biasing of pipeline readout amplifier
3. connection error inside multiplexer
4. I^2C-Interface requires 40 MHz sampling clock in SDA delay stage
5. readout daisy chain not correctly implemented
6. readout time at consecutive triggers > 900 ns
7. high-ohmic preamplifier feedback limits input charge rate
8. shaping time at high capacitive input loads > 25 ns
9. baseline fluctuations in analogue readout data stream at low trigger rates (i. e. 1 kHz and below)
10. missing on-chip trigger synchronisation

A.8.2 Beetle1.1

The problems described in sect. A.8.1, 5).-10.) are also present in *Beetle1.1* because the corresponding design elements have been retained unchanged from *Beetle1.0*.

Bibliography

[1] R. Brenner et al., Nucl. Instr. and Meth. A339 (1994) 564

[2] CLC400, Fast Settling, Wideband Low Gain Monolithic Op Amp, National Semiconductor

[3] The I^2C-bus and how to use it, Philips Semiconductors, 1995

[4] Bi-directional level shifter for I^2C-bus and other systems, Application Note AN97055, Philips Semiconductors, 1998

Appendix B

The Beetle Reference Manual v1.2

The Beetle Reference Manual

— chip version 1.2 —

NIELS VAN BAKEL[1], DANIEL BAUMEISTER[2] [1], MARTIN VAN BEUZEKOM[1], JO VAN DEN BRAND[1], MARTIN FEUERSTACK-RAIBLE[6], NEVILLE HARNEW[3], WERNER HOFMANN[2], EDDY JANS[1], SANDER KLOUS[1], KARL-TASSO KNÖPFLE[2], SVEN LÖCHNER[2] [2], MICHAEL SCHMELLING[2], EDGAR SEXAUER[5], NIGEL SMALE[3], ULRICH TRUNK[4], HANS VERKOOIJEN[1]
— [1]NIKHEF / FREE UNIVERSITY AMSTERDAM —
[2]MAX-PLANCK-INSTITUTE FOR NUCLEAR PHYSICS, HEIDELBERG —
[3]UNIVERSITY OF OXFORD —
[4]PHYSICS INSTITUTE, UNIVERSITY OF HEIDELBERG —
[5] NOW AT DIALOG SEMICONDUCTORS, KIRCHHEIM-NABERN, GERMANY
[6] NOW AT FUJITSU MIKROELEKTRONIK GMBH, DREIEICH-BUCHSCHLAG, GERMANY

proprietary version

This paper details the port definitions, electrical specifications, modes of operation and programming sequences of the 128 channel readout chip *Beetle*. The chip is developed for the LHCb experiment and fulfils the requirements of the silicon vertex detector, the inner tracker, the pile-up veto trigger and the RICH detector in case of multi-anode photomultiplier readout. It integrates 128 channels with low-noise charge-sensitive preamplifiers and shapers. The peaking time of the shaped pulse is 25 ns with a 30% remainder of the peak voltage after 25 ns. A comparator per channel with configurable polarity provides a binary signal. Four adjacent comparator channels are being ORed and brought off chip via LVDS ports. Either the shaper or comparator output is sampled with the LHC-bunch-crossing frequency of 40 MHz into an analogue pipeline with a programmable latency of max. 160 sampling intervals and an integrated derandomising buffer of 16 stages. For analogue readout data is multiplexed with up to 40 MHz onto 1 or 4 ports. A binary readout mode operates at up to 80 MHz output rate on two ports. Current drivers bring the serialised data off chip. The chip can accept trigger rates of up to 1.1 MHz to perform a dead-timeless readout within 900 ns per sample. For testability and calibration purposes, a charge injector with adjustable pulse height is implemented. The bias settings and various other parameters can be controlled via a standard I^2C-interface.

[1]Email: baumeis@kip.uni-heidelberg.de
[2]Email: loechner@kip.uni-heidelberg.de

Contents

B.1 Document Edition History 146
B.2 Chip Version History 146
B.3 Chip Architecture 147
B.4 Electrical specifications 148
B.4.1 DC characteristics 148
B.4.2 Analogue output characteristics 148
B.5 Modes of operation 149
B.5.1 Reset modes 149
B.5.2 Readout modes 149
B.5.3 Operation in daisychain 149
B.5.4 Operation with internal testpulses 150
B.5.5 Comparator operation 150
B.5.6 Single Event Upset counter 152
B.6 Slow Control 153
B.6.1 I^2C-Interface 153
B.6.2 Bias and configuration registers 153
B.7 Pad Description 157
B.7.1 Front pads 158
B.7.2 Bottom pads 162
B.7.3 Backside pads 163
B.7.4 Top pads 165
B.8 List of known problems and bugs 167

B.1 Document Edition History

This manual describes the chip version 1.2. For versions 1.0 and 1.1 please refer to the corresponding version of this manual (appendix A).

Version	Date	Author	Description
1.2	18.11.2002	DB, SL	document created

B.2 Chip Version History

Version	Submission Date	Changes relating to previous version
Beetle1.0	April 2000	
Beetle1.1	March 2001	test channel extended till pipeline readout amplifier (pipeamp) output modified pipeline layout analogue delay element for I^2C-SDA line added modified pipeamp modified bias network of pipeamp modified multiplexer modified tristate buffer in control circuit
Beetle1.2	April 2002	implementation of a new front-end (set 2c of *BeetleFE1.1*) restriction of readout time to 900 ns introduction of a power-up reset additional LVDS mode of current output buffer on-chip trigger synchronisation increase of pipeline depth by 1 hard-wired I^2C-chip address (defined via bond pads) introduction of SCHMITT-triggers in the I^2C-pads reduction of DAC resolution from 10 to 8 bits increase of max. deliverable bias current to 2 mA

B.3 Chip Architecture

The *Beetle* can be operated as analogue or alternatively as binary pipelined readout chip. It implements the basic RD20 front-end electronics architecture [1]. Fig. B.1 shows a schematic block diagram of the chip.

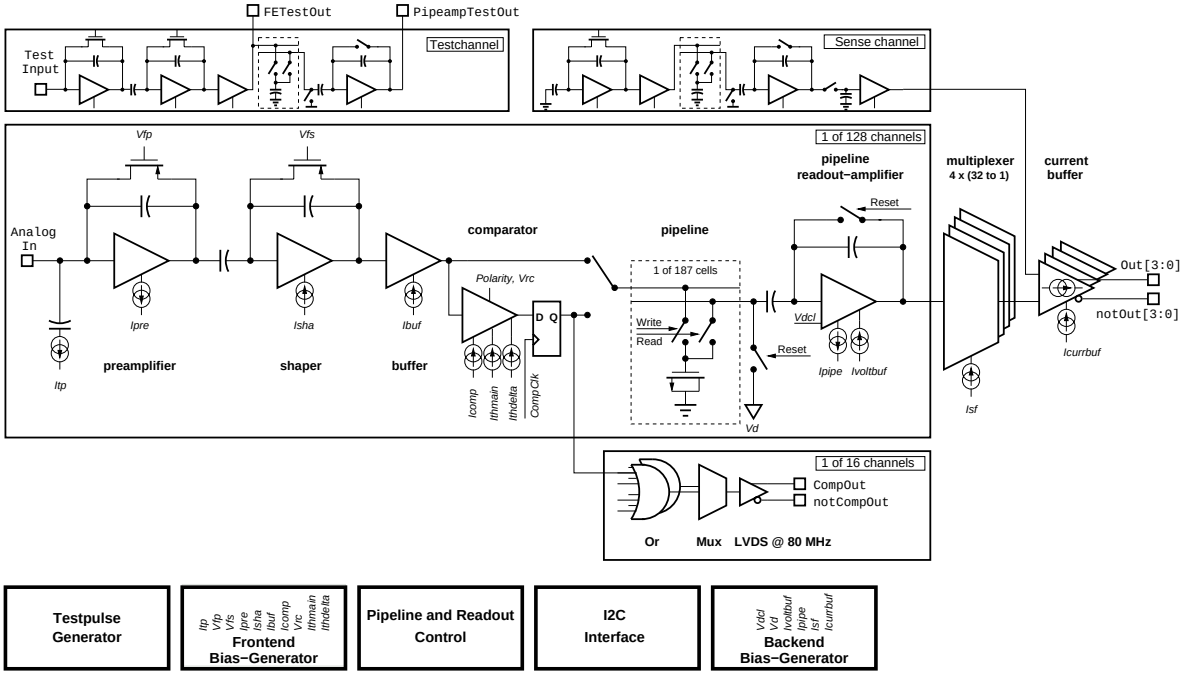


Figure B.1: Schematic block diagram of the *Beetle* readout chip.

The chip integrates 128 channels. Each channel consists of a low-noise charge-sensitive preamplifier and an active CR-RC pulse shaper. The risetime of the shaped pulse is ≤ 25 ns, the spill-over left 25 ns after the peak at most 30%. A comparator per channel provides a binary signal. It features a configurable polarity and an individual threshold level. Four adjacent comparator channels are ORed together, latched, multiplexed by a factor of 2 and routed off the chip via low voltage differential signalling (LVDS) ports at 80 MHz. Either the shaper- or the comparator output is sampled with the LHC bunch-crossing frequency at 40 MHz into an analogue pipeline with a programmable latency of max. 160 sampling intervals and an integrated multi-event buffer of 16 stages. The signal stored in the pipeline is transfered to the multiplexer via a resetable charge-sensitive amplifier. Within a readout time of 900 ns current drivers bring the serialised data off chip. The output of a dummy channel is subtracted from the analogue data to compensate common mode effects. All amplifier stages are biased by forced currents. On-chip digital-to-analogue converters (DACs) with 8 bit resolution generate the bias currents and voltages. For test and calibration purposes a charge injector with adjustable pulse height is implemented on each channel. The bias settings and various other parameters like the trigger latency can be controlled via a standard I^2C-interface [4]. All digital control and data signals, except those for the I^2C-ports, are routed via LVDS ports.

The chip is fabricated in 0.25 μm standard CMOS technology and has a die size of (5.1×6.1) mm^2. The analogue input pads have a pitch of 40.24 μm. If no comparator outputs are used,

pads on the sides of the chip do not need to be bonded. This allows an overall pitch of 50 μm when mounting the chips side by side.

B.4 Electrical specifications

B.4.1 DC characteristics

Supply	Min. [V]	Nom. [V]	Max. [V]	Description
Vdda	2.2	2.5	2.7	Positive analogue supply
Gnda	0	0	0	Negative analogue supply
Vddd	2.2	2.5	2.7	Positive digital supply
Gndd	0	0	0	Negative digital supply
VddPre	2.2	2.5	2.7	Positive preamplifier supply
GndPre	0	0	0	Negative preamplifier supply (detector ground)
VddComp	2.2	2.5	2.7	Positive comparator output supply
GndComp	0	0	0	Negative comparator output supply

Table B.1: DC characteristics of *Beetle1.2*.

B.4.2 Analogue output characteristics

Fig. B.2 gives an example of a receiver circuit for analogue signals using the CLC400 transimpedance amplifier [2] and binary signals using the DS90C032 [3] LVDS receiver.

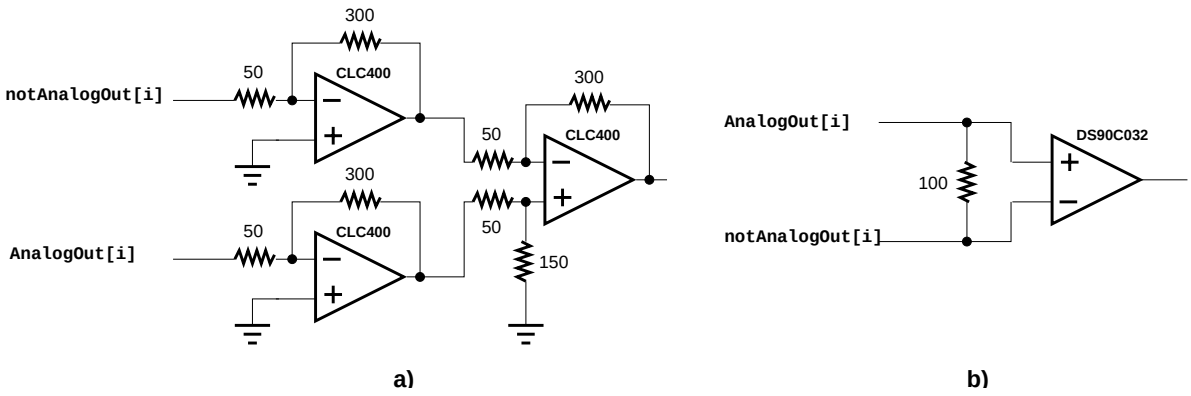


Figure B.2: Example of a receiver circuit for the analogue (a) and binary (b) output signals. In case of analogue signals the CLC400 transimpedance amplifier is used, in case of binary signals the DS90C032 LVDS receiver.

B.5 Modes of operation

B.5.1 Reset modes

Two different types of reset exist on *Beetle1.2*.

- *Power-up reset* is active immediately when the chip's power is switched on. The reset's time-constant, i.e. the time between "power-on" and the reset becoming inactive, can be adjusted via an external capacitance connected to the `PowerupReset` pad. For example, C_{ext} =10 nF (100 nF) results in a time constant $\tau = 28$ ms (280 ms). All *Beetle* registers are reset to 0 and the I^2C-interface is initialised.
- *External reset* follows the `Reset` port (see section B.7.3). It resets the pipeline write and trigger pointer to column number 0 and initialises the control logic's state machines. The rising edge of `Reset` re-initialises the I^2C-interface.

B.5.2 Readout modes

Beetle1.2 provides three different readout modes:

1. Analogue readout in 900 ns on 4 ports
2. Binary readout in 900 ns on 2 ports
3. Analogue readout in 3.6 μs on 1 port (for applications with less demanding readout speed requirements).

Fig. B.3 shows the assignment of the header bits and analogue input channels to the output channels in the different modes.

The meaning of the various header bits is given in table B.2, the readout timing behaviour is depicted in fig. B.4.

Bit	Description
I0	leading bit: always active
I1	(even) parity of pipeline column number (PCN)
I2	ActiveEDC: indicates active error and correction (EDC) logic
I3	parity of register *CompChTh*
I4	parity of register *CompMask*
I5	parity of register *TpSelect*
I6-I7	2 LSBs of register *SEUcounter*
P0-P7	Pipeline Column Number

Table B.2: Header bits in *Beetle1.2*'s data burst.

B.5.3 Operation in daisy chain

The daisy chain allows several chips to share one, two or four output lines. It consists of two signal paths, a *token* and a *return token* path. They are built up by connecting the `RoTokenOut` (`RoReTokenIn`) pad of one chip with the `RoTokenIn` (`RoReTokenOut`) of the neighbouring chip.

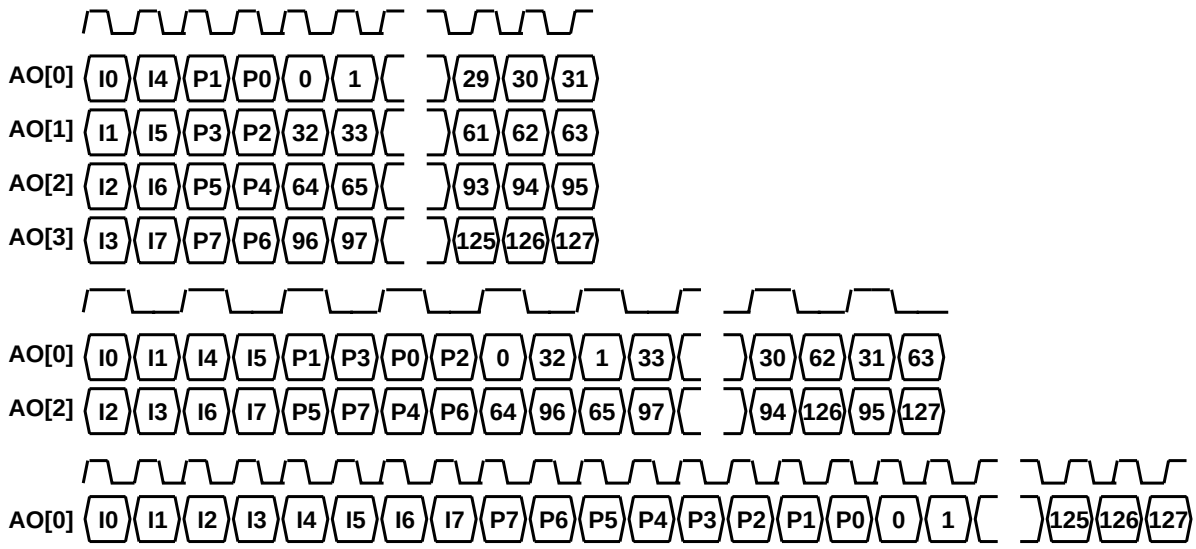


Figure B.3: *Beetle1.2* readout modes. From top to bottom: Analogue readout mode: 32 analogue channels are multiplexed onto 4 ports with up to 40 MHz, Binary readout mode: 64 binary channels are multiplexed onto 2 ports with up to 80 MHz, Readout mode for less demanding readout speed requirements: 128 analogue channels are multiplexed onto 1 port with up to 40 MHz.

The chip position in the chain has to be configured in the *ROCtrl* register. A chip can be the first (`DaisyFirst`=1), an intermediate or the last (`DaisyLast`=1) in the daisy chain.

B.5.4 Operation with internal test pulses

Test pulses can be injected into the preamplifier with an on-chip generator. A step like pattern corresponding to +2, +1, −1 and −2 times the input signal amplitude is coupled modulo 4 to the 128 channels. Via the `Testpulse` port a toggle flip-flop is triggered: an input pulse on this port generates a rising edge of the internal testpulse signal, a succeeding input pulse results in a falling edge of the testpulse. The amplitude of the injected pulse can be adjusted with the *Itp* bias registers (cf. table B.5).

B.5.5 Comparator operation

The comparator circuit consists of an integrator, a threshold generator and a discriminator. The integrator extracts the DC-offset of the shaped pulse with a variable time constant between 1 and 20 μs, which can be adjusted via the *Vrc* register (cf. table B.5). The DC-offset varies from channel to channel and is added to the threshold voltage. The threshold level is adjustable per channel with a resolution of 3 bits.

Comparator configuration

The comparator is configured via the register *CompControl* (see table B.5 and fig. B.7). *CompOutMode* defines the mode of operation of the comparator. *CompOutMode*=0 selects the analogue mode, in which the output of the front-end amplifier is transferred to the pipeline.

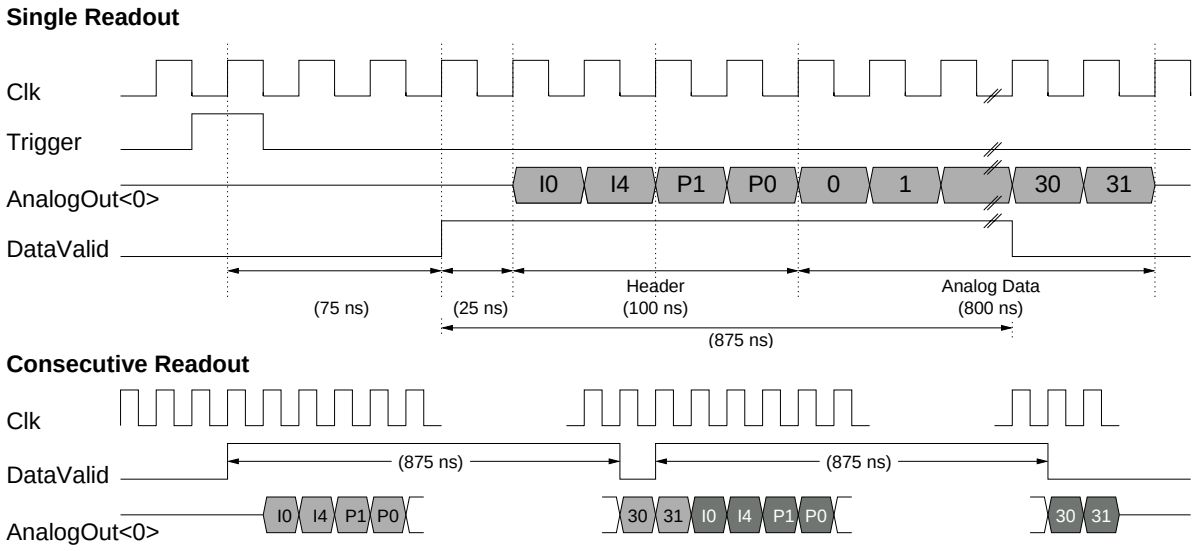


Figure B.4: Readout timing schemes of the analogue readout mode on 4 ports. Only channel 0 is depicted. The upper plot shows a single readout burst, the lower the case of consecutive readout.

In binary mode (*CompOutMode*=1) the comparator output is fed into the pipeline. *CompDisable*=1 turns off the comparator's bias current. *CompPolarity* selects between an inverting (0) or non-inverting (1) comparator operation. *CompMode* switches between two different kinds of output signal. With *CompMode*=0 the output is as long active as the comparator input signal is above the threshold level. With *CompMode*=1 the output is only one CompClk cycle active, independent of the time, which the input signal is above the threshold.

Threshold adjustment

The threshold level is generated from two programmable currents. *Ithmain* (register address 8) determines the global threshold, which is common to all channels. *Ithdelta* (register address 7) defines an additional delta voltage.

The comparator threshold register (*CompChTh*, address 20) selects the number of delta voltages which are being added to the global threshold voltage. This register is operated as a shift register. The bits `CompChTh[2:0]` are being assigned to channel *k*, the bits `CompChTh[6:4]` to channel *k+1*. To define the delta threshold voltage of all channels, the *CompChTh* register has to be programmed 64 times consecutively. A shift mechanism provides the bits to the channels in the order (Ch[0], Ch[1]), (Ch[2], Ch[3]),..., (Ch[126], Ch[127]).

Comparator channel mapping

The comparator outputs are LVDS drivers. Each driver sends data of two combined comparator groups, the first group of ORed channels during the high phase of `Clk`, the second during the low phase. The mapping of the channels to the comparator outputs is shown in table B.3.

CompOut No.	High phase of Clk	Low phase of Clk
CompOut[15]	Ch[127]∨Ch[126]∨Ch[125]∨Ch[124]	Ch[123]∨Ch[122]∨Ch[121]∨Ch[120]
CompOut[14]	Ch[119]∨Ch[118]∨Ch[117]∨Ch[116]	Ch[115]∨Ch[114]∨Ch[113]∨Ch[112]
CompOut[13]	Ch[111]∨Ch[110]∨Ch[109]∨Ch[108]	Ch[107]∨Ch[106]∨Ch[105]∨Ch[104]
CompOut[12]	Ch[103]∨Ch[102]∨Ch[101]∨Ch[100]	Ch[99]∨Ch[98]∨Ch[97]∨Ch[96]
CompOut[11]	Ch[95]∨Ch[94]∨Ch[93]∨Ch[92]	Ch[91]∨Ch[90]∨Ch[89]∨Ch[88]
CompOut[10]	Ch[87]∨Ch[86]∨Ch[85]∨Ch[84]	Ch[83]∨Ch[82]∨Ch[81]∨Ch[80]
CompOut[9]	Ch[79]∨Ch[78]∨Ch[77]∨Ch[76]	Ch[75]∨Ch[74]∨Ch[73]∨Ch[72]
CompOut[8]	Ch[71]∨Ch[70]∨Ch[69]∨Ch[68]	Ch[67]∨Ch[66]∨Ch[65]∨Ch[64]
CompOut[7]	Ch[63]∨Ch[62]∨Ch[61]∨Ch[60]	Ch[59]∨Ch[58]∨Ch[57]∨Ch[56]
CompOut[6]	Ch[55]∨Ch[54]∨Ch[53]∨Ch[52]	Ch[51]∨Ch[50]∨Ch[49]∨Ch[48]
CompOut[5]	Ch[47]∨Ch[46]∨Ch[45]∨Ch[44]	Ch[43]∨Ch[42]∨Ch[41]∨Ch[40]
CompOut[4]	Ch[39]∨Ch[38]∨Ch[37]∨Ch[36]	Ch[35]∨Ch[34]∨Ch[33]∨Ch[32]
CompOut[3]	Ch[31]∨Ch[30]∨Ch[29]∨Ch[28]	Ch[27]∨Ch[26]∨Ch[25]∨Ch[24]
CompOut[2]	Ch[23]∨Ch[22]∨Ch[21]∨Ch[20]	Ch[19]∨Ch[18]∨Ch[17]∨Ch[16]
CompOut[1]	Ch[15]∨Ch[14]∨Ch[13]∨Ch[12]	Ch[11]∨Ch[10]∨ Ch[9]∨Ch[8]
CompOut[0]	Ch[7]∨Ch[6]∨Ch[5]∨Ch[4]	Ch[3]∨Ch[2]∨Ch[1]∨Ch[0]

Table B.3: Mapping of analogue input channels to comparator output channels on *Beetle1.2*.

B.5.6 Single Event Upset counter

A 8-bit counter is integrated in *Beetle1.2* to indicate the number of occurred single event upsets. The counter output is readable via the I^2C-bus (cf. B.6.2). The two least significant bits are additionally transferred in the header of the analogue output stream (fig. B.3, table B.2). This allows a fast monitoring of SEUs during readout. An I^2C-write access to the counter register resets it. All *Beetle* registers, including the shift-registers *CompChTh*, *CompMask* and *TpSelect*, are contributing to the SEU counter. The bits used in the logic control circuits are *not* taken into account.

B.6 Slow Control

B.6.1 I²C-Interface

The chip's slow control interface is a standard mode I²C-slave device performing a transfer rate of 100 kbit/s. The chip address, necessary to access a single device via the I²C-bus, is assigned via the address pads `I2CAddr[6:0]` (cf. section B.7.3).

The internal registers are being accessed via a *pointer register*. This contains the address of the register to be written or read first. The pointer is internally incremented by 1 after each transferred data frame. In this way registers with adjacent addresses can be accessed consecutively. The pointer register itself remains unchanged, i.e. a new transfer will start at the same pointer position. Fig. B.5 explains the transfer sequences in write and read mode. Data is always transferred with the most significant bit (MSB) first. In write mode the chip address is transmitted after initialising the transfer, followed by the pointer byte and the data. After the transmission of one data frame, the pointer addresses the successive register because of its auto-incrementing function. The registers with addresses $20 - 23$ have an exceptional status. The registers $20 - 22$ are implemented as 128-bit shift-registers (cf. B.6.2), register 23 is the output of the SEU counter. A write access to this register resets it to 0. Hence, the auto-incrementing of the address pointer is only performed for addresses ≤ 19. Starting from addresses ≤ 20, the pointer will stop at address 20. To access a higher address, the corresponding register has to be addressed directly.

The transfer of the pointer byte is obligatory in write mode. In read mode there are two versions:

- Preset pointer
  After initialising the transfer and sending the chip address data is immediately read out. The pointer has been set in a previous transfer.

- Pointer set followed by immediate read-out
  After initialising the transfer and sending the chip address the pointer byte is transferred. The I²C-bus is re-initialised, the chip address is sent and data is read out.

Commercially available I²C-devices usually operate at 3.3 V or 5 V. To interconnect these devices with a *Beetle* I²C-interface a bidirectional level shifter is necessary. A simple solution to this problem is the use of a discrete MOS-FET for each bus line [5]. Fig. B.6 illustrates the level shifter circuit. An example for a single MOS-FET device is type BSN20 from Philips Semiconductors.

B.6.2 Bias and configuration registers

Beetle1.2 contains 24 8-bit registers with the addresses $0 - 23$. Table B.5 lists all registers with their nominal value and register content. A LSB corresponds to $8\,\mu$A for currents and 9.8 mV for voltages, except for register *Vrc* where a LSB is 4.9 mV. Registers $0 - 15$ are bias registers for the analogue stages. Register 16 defines the latency which has to be ≥ 10 and ≤ 160 for reasonable chip operation. A change of the latency register will only be taken over after applying a chip reset (`Reset`-port). Register 18 defines the ratio between the readout clock `Rclk` and the sampling clock `Sclk`. The ratio R = `Rclk`/`Sclk` is $1/(RclkDiv{+}1)$ and allows `Rclk` frequencies from 40 MHz down to ≈ 156 kHz. $RclkDiv{=}0$ means, that `Sclk` and

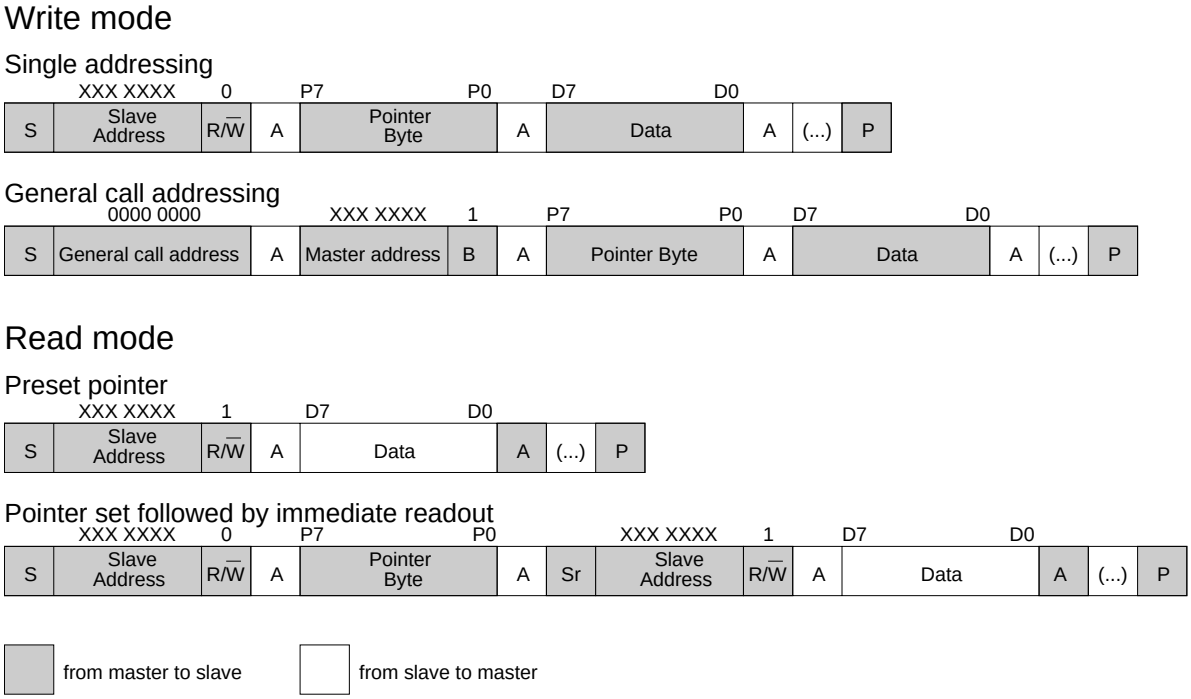


Figure B.5: I^{2}C-bus write and read sequences for accessing registers on the *Beetle*.

`Rclk` have the same frequency. The registers 17 and 19 select the chip's mode of operation (readout mode, daisy chain configuration) and define the comparator configuration. Fig. B.7 shows the detailed bit assignment of the registers *ROControl* and *CompControl*. Registers $20 - 22$ (*CompChTh, CompMask, TpSelect*) are operated as shift-registers: *CompMask* and *TpSelect* form a 128-bit register each, segmented in 16 8-bit registers, *CompChTh* establishes a 512 ($= 128 \times 4$) bit register divided into 64 8-bit registers, whereas only 6 of the 8 bits per frame are assigned (cf. section B.5.5). A consecutive write-access to the corresponding register address shifts the data in 8-bit frames starting from the largest channel number (see table B.4). A read access to such a register returns the bits corresponding to channels $7 - 0$ in case of *CompMask* and *TpSelect* and $1 - 0$ in case of *CompChTh*. This allows a verification of the shifted data. Register 23 is the output of the SEU counter. A write access to this register resets the content to 0. Note, that the two LSB of the register *SEUcounts* are transmitted in the header (`I[7-6]`) of the analogue output stream (cf. B.5.2).

	write access	read access
CompMask	Ch[127:120], Ch[119:112], ...	Ch[7:0]
TpSelect	Ch[127:120], Ch[119:112], ...	Ch[7:0]
CompChTh	Ch[127:126], Ch[125:124], ...	Ch[1:0]

Table B.4: Channel sequence for write and read access to the shift registers *CompMask, TpSelect* and *CompChTh*.

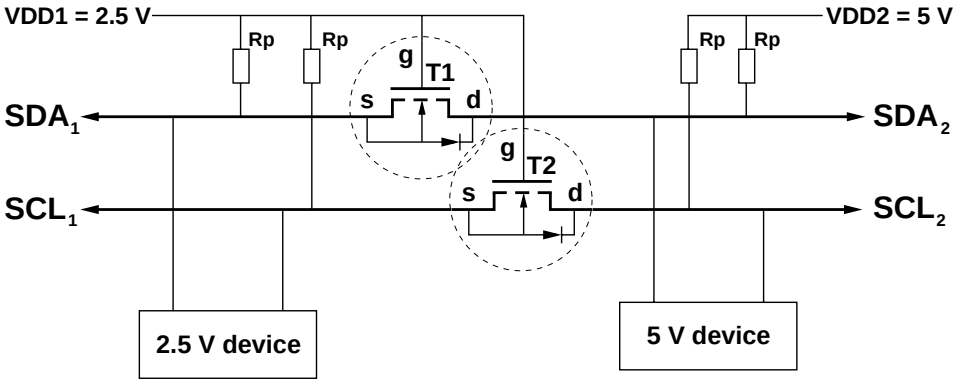
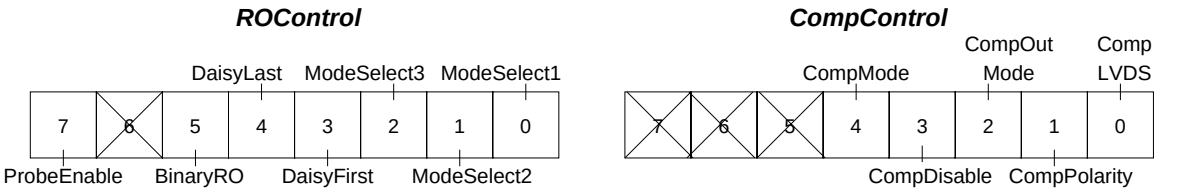


Figure B.6: Bidirectional level shifter circuit to connect two different voltage level sections of an I^2C-bus system. An example for a single MOS-FET device is type BSN20 from Philips Semiconductors.



DaisyFirst: first chip in daisychain
DaisyLast: last chip in daisychain
ModeSelect3: analogue readout on 4 ports
ModeSelect2: analogue readout on 1 port
ModeSelect1: binary readout on 2 ports
ProbeEnable: 1: enables probe pads
BinaryRO: 1: binary mode of current driver

CompMode: 1: pulse mode 0: track mode
CompDisable: 1: disables comparator
CompOutMode: 1: binary readout 0: analogue readout
CompPolarity: 0: inverting 1: non−inverting
CompLVDS: 1: disables comparator LVDS output drivers

Figure B.7: Bit assignment of the configuration registers *ROControl* and *CompControl*. All switches are active-high. 1 enables the switch, 0 disables it.

Reg. ID	Reg. Name	Nominal Value	Reg. content	Description
0	Itp	0 μA	0x00	test pulse bias current
1	Ipre	600 μA	0x4C	preamplifier bias current
2	Isha	80 μA	0x0A	shaper bias current
3	Ibuf	80 μA	0x0A	front-end buffer bias current
4	Vfp	0 V	0x00	preamplifier feedback voltage
5	Vfs	0 V	0x00	shaper feedback voltage
6	Icomp	40 μA	0x05	comparator bias current
7	Ithdelta	—	—	current defining incremental comparator threshold
8	Ithmain	—	—	current defining common comparator threshold
9	Vrc	0 V	0x00	comparator RC time constant
10	Ipipe	100 μA	0x0D	pipeamp bias current
11	Vd	1 V	0x66	pipeamp reset potential
12	Vdcl	1.1 V	0x70	pipeamp reference voltage
13	Ivoltbuf	200 μA	0x1A	pipeamp buffer bias current
14	Isf	200 μA	0x1A	multiplexer buffer bias current
15	Icurrbuf	1200 μA	0x99	current output buffer bias current
16	Latency	160	0xA0	trigger latency
17	ROCtrl	cf. fig. B.7		readout control
18	RclkDiv	0	0x00	ratio between `Rclk` and `Sclk`
19	CompCtrl	cf. fig. B.7		comparator control
20	CompChTh	—	—	comparator channel threshold, shift register implementation
21	CompMask	0	0x00	comparator mask, shift register implementation
22	TpSelect	0	0x00	testpulse selection, shift register implementation
23	SEUcounts	—	—	sum of single event upsets

Table B.5: Bias and configuration registers of *Beetle1.2*.

B.7 Pad Description

A reference number has been assigned to each pad. The numbering starts in the upper left corner of the die (with the analogue input pads left) and runs counterclockwise (cf. fig. B.8). The following tables summarise the signals and explain them. The pad coordinates reference the lower left corner of the pad opening, which is $120\,\mu m \times 95\,\mu m$ in case of the front pads and $95\,\mu m \times 95\,\mu m$ for all others. The origin of the coordinate system is defined by the lower left chip corner $(0, 0)$. The dimensions of the chip die are $5{,}100\,\mu m \times 6{,}100\,\mu m$.

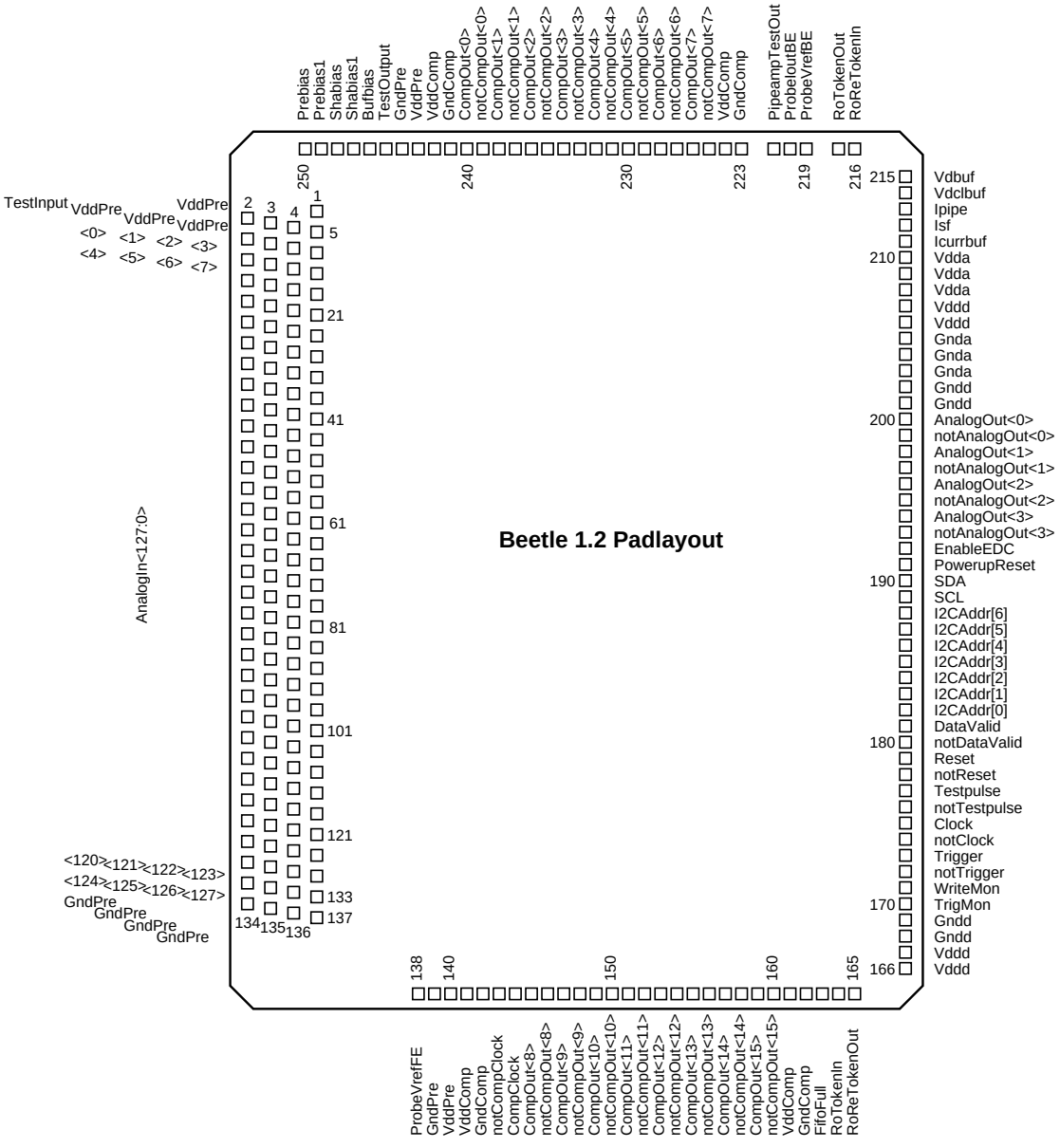


Figure B.8: Pad layout of *Beetle1.2*. The die size is $(5.1 \times 6.1)\,\mathrm{mm}^2$.

B.7.1 Front pads

Ref.no.	Pin name	Coordinates		Type	Description
		x [μm]	y [μm]		
1	VddPre	490.00	5836.30	power input	positive preamplifier supply
2	TestInput	25.00	5796.06	input	input of test channel
3	VddPre	180.00	5755.82	power input	positive preamplifier supply
4	VddPre	335.00	5715.58	power input	positive preamplifier supply
5	VddPre	490.00	5675.34	power input	positive preamplifier supply
6	AnalogIn[0]	25.00	5635.10	input	input of channel 0
7	AnalogIn[1]	180.00	5594.86	input	input of channel 1
8	AnalogIn[2]	335.00	5554.62	input	input of channel 2
9	AnalogIn[3]	490.00	5514.38	input	input of channel 3
10	AnalogIn[4]	25.00	5474.14	input	input of channel 4
11	AnalogIn[5]	180.00	5433.90	input	input of channel 5
12	AnalogIn[6]	335.00	5393.66	input	input of channel 6
13	AnalogIn[7]	490.00	5353.42	input	input of channel 7
14	AnalogIn[8]	25.00	5313.18	input	input of channel 8
15	AnalogIn[9]	180.00	5272.94	input	input of channel 9
16	AnalogIn[10]	335.00	5232.70	input	input of channel 10
17	AnalogIn[11]	490.00	5192.46	input	input of channel 11
18	AnalogIn[12]	25.00	5152.22	input	input of channel 12
19	AnalogIn[13]	180.00	5111.98	input	input of channel 13
20	AnalogIn[14]	335.00	5071.74	input	input of channel 14
21	AnalogIn[15]	490.00	5031.50	input	input of channel 15
22	AnalogIn[16]	25.00	4991.26	input	input of channel 16
23	AnalogIn[17]	180.00	4951.02	input	input of channel 17
24	AnalogIn[18]	335.00	4910.78	input	input of channel 18
25	AnalogIn[19]	490.00	4870.54	input	input of channel 19
26	AnalogIn[20]	25.00	4830.30	input	input of channel 20
27	AnalogIn[21]	180.00	4790.06	input	input of channel 21
28	AnalogIn[22]	335.00	4749.82	input	input of channel 22
29	AnalogIn[23]	490.00	4709.58	input	input of channel 23
30	AnalogIn[24]	25.00	4669.34	input	input of channel 24
31	AnalogIn[25]	180.00	4629.10	input	input of channel 25
32	AnalogIn[26]	335.00	4588.86	input	input of channel 26
33	AnalogIn[27]	490.00	4548.62	input	input of channel 27
34	AnalogIn[28]	25.00	4508.38	input	input of channel 28
35	AnalogIn[29]	180.00	4468.14	input	input of channel 29
36	AnalogIn[30]	335.00	4427.90	input	input of channel 30
37	AnalogIn[31]	490.00	4387.66	input	input of channel 31
38	AnalogIn[32]	25.00	4347.42	input	input of channel 32
39	AnalogIn[33]	180.00	4307.18	input	input of channel 33
40	AnalogIn[34]	335.00	4266.94	input	input of channel 34
41	AnalogIn[35]	490.00	4226.70	input	input of channel 35

Ref.no.	Pin name	Coordinates		Type	Description
		x [μm]	y [μm]		
42	AnalogIn[36]	25.00	4186.46	input	input of channel 36
43	AnalogIn[37]	180.00	4146.22	input	input of channel 37
44	AnalogIn[38]	335.00	4105.98	input	input of channel 38
45	AnalogIn[39]	490.00	4065.74	input	input of channel 39
46	AnalogIn[40]	25.00	4025.50	input	input of channel 40
47	AnalogIn[41]	180.00	3985.26	input	input of channel 41
48	AnalogIn[42]	335.00	3945.02	input	input of channel 42
49	AnalogIn[43]	490.00	3904.78	input	input of channel 43
50	AnalogIn[44]	25.00	3864.54	input	input of channel 44
51	AnalogIn[45]	180.00	3824.30	input	input of channel 45
52	AnalogIn[46]	335.00	3784.06	input	input of channel 46
53	AnalogIn[47]	490.00	3743.82	input	input of channel 47
54	AnalogIn[48]	25.00	3703.58	input	input of channel 48
55	AnalogIn[49]	180.00	3663.34	input	input of channel 49
56	AnalogIn[50]	335.00	3623.10	input	input of channel 50
57	AnalogIn[51]	490.00	3582.86	input	input of channel 51
58	AnalogIn[52]	25.00	3542.62	input	input of channel 52
59	AnalogIn[53]	180.00	3502.38	input	input of channel 53
60	AnalogIn[54]	335.00	3462.14	input	input of channel 54
61	AnalogIn[55]	490.00	3421.90	input	input of channel 55
62	AnalogIn[56]	25.00	3381.66	input	input of channel 56
63	AnalogIn[57]	180.00	3341.42	input	input of channel 57
64	AnalogIn[58]	335.00	3301.18	input	input of channel 58
65	AnalogIn[59]	490.00	3260.94	input	input of channel 59
66	AnalogIn[60]	25.00	3220.70	input	input of channel 60
67	AnalogIn[61]	180.00	3180.46	input	input of channel 61
68	AnalogIn[62]	335.00	3140.22	input	input of channel 62
69	AnalogIn[63]	490.00	3099.98	input	input of channel 63
70	AnalogIn[64]	25.00	3059.74	input	input of channel 64
71	AnalogIn[65]	180.00	3019.50	input	input of channel 65
72	AnalogIn[66]	335.00	2979.26	input	input of channel 66
73	AnalogIn[67]	490.00	2939.02	input	input of channel 67
74	AnalogIn[68]	25.00	2898.78	input	input of channel 68
75	AnalogIn[69]	180.00	2858.54	input	input of channel 69
76	AnalogIn[70]	335.00	2818.30	input	input of channel 70
77	AnalogIn[71]	490.00	2778.06	input	input of channel 71
78	AnalogIn[72]	25.00	2737.82	input	input of channel 72
79	AnalogIn[73]	180.00	2697.58	input	input of channel 73
80	AnalogIn[74]	335.00	2657.34	input	input of channel 74
81	AnalogIn[75]	490.00	2617.10	input	input of channel 75
82	AnalogIn[76]	25.00	2576.86	input	input of channel 76
83	AnalogIn[77]	180.00	2536.62	input	input of channel 77
84	AnalogIn[78]	335.00	2496.38	input	input of channel 78

Ref.no.	Pin name	Coordinates		Type	Description
		x [μm]	y [μm]		
85	AnalogIn[79]	490.00	2456.14	input	input of channel 79
86	AnalogIn[80]	25.00	2415.90	input	input of channel 80
87	AnalogIn[81]	180.00	2375.66	input	input of channel 81
88	AnalogIn[82]	335.00	2335.42	input	input of channel 82
89	AnalogIn[83]	490.00	2295.18	input	input of channel 83
90	AnalogIn[84]	25.00	2254.94	input	input of channel 84
91	AnalogIn[85]	180.00	2214.70	input	input of channel 85
92	AnalogIn[86]	335.00	2174.46	input	input of channel 86
93	AnalogIn[87]	490.00	2134.22	input	input of channel 87
94	AnalogIn[88]	25.00	2093.98	input	input of channel 88
95	AnalogIn[89]	180.00	2053.74	input	input of channel 89
96	AnalogIn[90]	335.00	2013.50	input	input of channel 90
97	AnalogIn[91]	490.00	1973.26	input	input of channel 91
98	AnalogIn[92]	25.00	1933.02	input	input of channel 92
99	AnalogIn[93]	180.00	1892.78	input	input of channel 93
100	AnalogIn[94]	335.00	1852.54	input	input of channel 94
101	AnalogIn[95]	490.00	1812.30	input	input of channel 95
102	AnalogIn[96]	25.00	1772.06	input	input of channel 96
103	AnalogIn[97]	180.00	1731.82	input	input of channel 97
104	AnalogIn[98]	335.00	1691.58	input	input of channel 98
105	AnalogIn[99]	490.00	1651.34	input	input of channel 99
106	AnalogIn[100]	25.00	1611.10	input	input of channel 100
107	AnalogIn[101]	180.00	1570.86	input	input of channel 101
108	AnalogIn[102]	335.00	1530.62	input	input of channel 102
109	AnalogIn[103]	490.00	1490.38	input	input of channel 103
110	AnalogIn[104]	25.00	1450.14	input	input of channel 104
111	AnalogIn[105]	180.00	1409.90	input	input of channel 105
112	AnalogIn[106]	335.00	1369.66	input	input of channel 106
113	AnalogIn[107]	490.00	1329.42	input	input of channel 107
114	AnalogIn[108]	25.00	1289.18	input	input of channel 108
115	AnalogIn[109]	180.00	1248.94	input	input of channel 109
116	AnalogIn[110]	335.00	1208.70	input	input of channel 110
117	AnalogIn[111]	490.00	1168.46	input	input of channel 111
118	AnalogIn[112]	25.00	1128.22	input	input of channel 112
119	AnalogIn[113]	180.00	1087.98	input	input of channel 113
120	AnalogIn[114]	335.00	1047.74	input	input of channel 114
121	AnalogIn[115]	490.00	1007.50	input	input of channel 115
122	AnalogIn[116]	25.00	967.26	input	input of channel 116
123	AnalogIn[117]	180.00	927.02	input	input of channel 117
124	AnalogIn[118]	335.00	886.78	input	input of channel 118
125	AnalogIn[119]	490.00	846.54	input	input of channel 119
126	AnalogIn[120]	25.00	806.30	input	input of channel 120
127	AnalogIn[121]	180.00	766.06	input	input of channel 121

Ref.no.	Pin name	Coordinates		Type	Description
		x [μm]	y [μm]		
128	`AnalogIn[122]`	335.00	725.82	input	input of channel 122
129	`AnalogIn[123]`	490.00	685.58	input	input of channel 123
130	`AnalogIn[124]`	25.00	645.34	input	input of channel 124
131	`AnalogIn[125]`	180.00	605.10	input	input of channel 125
132	`AnalogIn[126]`	335.00	564.86	input	input of channel 126
133	`AnalogIn[127]`	490.00	524.62	input	input of channel 127
134	`GndPre`	25.00	484.38	power input	negative preamplifier supply (detector ground)
135	`GndPre`	180.00	444.14	power input	negative preamplifier supply (detector ground)
136	`GndPre`	335.00	403.90	power input	negative preamplifier supply (detector ground)
137	`GndPre`	490.00	363.66	power input	negative preamplifier supply (detector ground)

B.7.2 Bottom pads

Ref.no.	Pin name	Coordinates		Type	Description
		x [μm]	y [μm]		
138	ProbeVrefFE	1754.12	37.50	output	analogue probe pad for front-end current source
139	GndPre	1869.12	37.50	power input	negative preamplifier supply (detector ground)
140	VddPre	1984.12	37.50	power input	positive preamplifier supply
141	VddComp	2099.12	37.50	power input	positive comparator supply
142	GndComp	2214.12	37.50	power input	negative comparator supply
143	notCompClock	2329.12	37.50	LVDS input	comparator clock
144	CompClock	2444.12	37.50	LVDS input	comparator clock
145	CompOut[8]	2559.12	37.50	LVDS output	comparator output ch. 8
146	notCompOut[8]	2674.12	37.50	LVDS output	comparator output ch. 8
147	CompOut[9]	2789.12	37.50	LVDS output	comparator output ch. 9
148	notCompOut[9]	2904.12	37.50	LVDS output	comparator output ch. 9
149	CompOut[10]	3019.12	37.50	LVDS output	comparator output ch. 10
150	notCompOut[10]	3134.12	37.50	LVDS output	comparator output ch. 10
151	CompOut[11]	3249.12	37.50	LVDS output	comparator output ch. 11
152	notCompOut[11]	3364.12	37.50	LVDS output	comparator output ch. 11
153	CompOut[12]	3479.12	37.50	LVDS output	comparator output ch. 12
154	notCompOut[12]	3594.12	37.50	LVDS output	comparator output ch. 12
155	CompOut[13]	3709.12	37.50	LVDS output	comparator output ch. 13
156	notCompOut[13]	3824.12	37.50	LVDS output	comparator output ch. 13
157	CompOut[14]	3939.12	37.50	LVDS output	comparator output ch. 14
158	notCompOut[14]	4054.12	37.50	LVDS output	comparator output ch. 14
159	CompOut[15]	4169.12	37.50	LVDS output	comparator output ch. 15
160	notCompOut[15]	4284.12	37.50	LVDS output	comparator output ch. 15
161	VddComp	4399.12	37.50	power input	positive comparator supply
162	GndComp	4514.12	37.50	power input	negative comparator supply
163	FifoFull	4629.12	37.50	CMOS output	indicates full derandomising buffer
164	RoTokenIn	4744.12	37.50	CMOS input	readout token input in daisy-chain mode
165	RoReTokenOut	4859.12	37.50	CMOS output	readout return token output in daisy-chain mode

B.7.3 Backside pads

Ref.no.	Pin name	Coordinates		Type	Description
		x [μm]	y [μm]		
166	Vddd	4974.62	184.72	power input	positive digital supply
167	Vddd	4974.62	299.72	power input	positive digital supply
168	Gndd	4974.62	414.72	power input	negative digital supply
169	Gndd	4974.62	529.72	power input	negative digital supply
170	TrigMon	4974.62	644.72	CMOS output	indicates if trigger pointer passes column 0
171	WriteMon	4974.62	759.72	CMOS output	indicates if write pointer passes column 0
172	notTrigger	4974.62	874.72	LVDS input	trigger
173	Trigger	4974.62	989.72	LVDS input	trigger
174	notClock	4974.62	1104.72	LVDS input	sampling clock
175	Clock	4974.62	1219.72	LVDS input	sampling clock
176	notTestpulse	4974.62	1334.72	LVDS input	test pulse
177	Testpulse	4974.62	1449.72	LVDS input	test pulse
178	notReset	4974.62	1564.72	LVDS input	system reset
179	Reset	4974.62	1679.72	LVDS input	system reset
180	notDataValid	4974.62	1794.72	LVDS output	indicates presence of valid data on AnalogOut
181	DataValid	4974.62	1909.72	LVDS output	indicates presence of valid data on AnalogOut
182	I2CAddr[0]	4974.62	2024.72	CMOS input (pull-down)	chip address bit 0
183	I2CAddr[1]	4974.62	2139.72	CMOS input (pull-down)	chip address bit 1
184	I2CAddr[2]	4974.62	2254.72	CMOS input (pull-down)	chip address bit 2
185	I2CAddr[3]	4974.62	2369.72	CMOS input (pull-down)	chip address bit 3
186	I2CAddr[4]	4974.62	2484.72	CMOS input (pull-down)	chip address bit 4
187	I2CAddr[5]	4974.62	2599.72	CMOS input (pull-down)	chip address bit 5
188	I2CAddr[6]	4974.62	2714.72	CMOS input (pull-down)	chip address bit 6
189	SCL	4974.62	2829.72	CMOS input	I2C-bus clock port
190	SDA	4974.62	2944.72	CMOS input/output	I2C-bus data port
191	PowerupReset	4974.62	3059.72	block input/output	block pad for power-up reset

Ref.no.	Pin name	Coordinates		Type	Description
		x [μm]	y [μm]		
192	EnableEDC	4974.62	3174.72	CMOS input (pull-up)	enables Error Detection and Correction
193	notAnalogOut[3]	4974.62	3289.72	output	analogue output ch. 3
194	AnalogOut[3]	4974.62	3404.72	output	analogue output ch. 3
195	notAnalogOut[2]	4974.62	3519.72	output	analogue output ch. 2
196	AnalogOut[2]	4974.62	3634.72	output	analogue output ch. 2
197	notAnalogOut[1]	4974.62	3749.72	output	analogue output ch. 1
198	AnalogOut[1]	4974.62	3864.72	output	analogue output ch. 1
199	notAnalogOut[0]	4974.62	3979.72	output	analogue output ch. 0
200	AnalogOut[0]	4974.62	4094.72	output	analogue output ch. 0
201	Gndd	4974.62	4209.72	power input	negative digital supply
202	Gndd	4974.62	4324.72	power input	negative digital supply
203	Gnda	4974.62	4439.72	power input	negative analogue supply
204	Gnda	4974.62	4554.72	power input	negative analogue supply
205	Gnda	4974.62	4669.72	power input	negative analogue supply
206	Vddd	4974.62	4784.72	power input	positive digital supply
207	Vddd	4974.62	4899.72	power input	positive digital supply
208	Vdda	4974.62	5014.72	power input	positive analogue supply
209	Vdda	4974.62	5129.72	power input	positive analogue supply
210	Vdda	4974.62	5244.72	power input	positive analogue supply
211	Icurrbuf	4974.62	5359.72	block output	analogue probe pad (to be blocked)
212	Isf	4974.62	5474.72	block output	analogue probe pad (to be blocked)
213	Ipipe	4974.62	5589.72	block output	analogue probe pad (to be blocked)
214	Vdclbuf	4974.62	5704.72	block output	analogue probe pad (to be blocked)
215	Vdbuf	4974.62	5819.72	block output	analogue probe pad (to be blocked)

B.7.4 Top pads

Ref.no.	Pin name	Coordinates		Type	Description
		x [μm]	y [μm]		
216	RoReTokenIn	4859.12	5967.52	CMOS input	readout return token input in daisy-chain mode
217	RoTokenOut	4744.12	5967.52	CMOS output	readout token output in daisy-chain mode
219	ProbeVrefBE	4514.12	5967.52	output	analogue probe pad for back-end current source
220	ProbeIoutBE	4399.12	5967.52	output	analogue probe pad for back-end current source
221	PipeampTestOut	4284.12	5967.52	output	pipeamp output of test channel
223	GndComp	4054.12	5967.52	power input	negative comparator supply
224	VddComp	3939.12	5967.52	power input	positive comparator supply
225	notCompOut[7]	3824.12	5967.52	LVDS output	comparator output ch. 7
226	CompOut[7]	3709.12	5967.52	LVDS output	comparator output ch. 7
227	notCompOut[6]	3594.12	5967.52	LVDS output	comparator output ch. 6
228	CompOut[6]	3479.12	5967.52	LVDS output	comparator output ch. 6
229	notCompOut[5]	3364.12	5967.52	LVDS output	comparator output ch. 5
230	CompOut[5]	3249.12	5967.52	LVDS output	comparator output ch. 5
231	notCompOut[4]	3134.12	5967.52	LVDS output	comparator output ch. 4
232	CompOut[4]	3019.12	5967.52	LVDS output	comparator output ch. 4
233	notCompOut[3]	2904.12	5967.52	LVDS output	comparator output ch. 3
234	CompOut[3]	2789.12	5967.52	LVDS output	comparator output ch. 3
235	notCompOut[2]	2674.12	5967.52	LVDS output	comparator output ch. 2
236	CompOut[2]	2559.12	5967.52	LVDS output	comparator output ch. 2
237	notCompOut[1]	2444.12	5967.52	LVDS output	comparator output ch. 1
238	CompOut[1]	2329.12	5967.52	LVDS output	comparator output ch. 1
239	notCompOut[0]	2214.12	5967.52	LVDS output	comparator output ch. 0
240	CompOut[0]	2099.12	5967.52	LVDS output	comparator output ch. 0
241	GndComp	1984.12	5967.52	power input	negative comparator supply
242	VddComp	1869.12	5967.52	power input	positive comparator supply
243	VddPre	1754.12	5967.52	power input	positive preamplifier supply
244	GndPre	1639.12	5967.52	power input	negative preamplifier supply (detector ground)
245	TestOutput	1524.12	5967.52	output	front-end output of test channel

Ref.no.	Pin name	Coordinates		Type	Description
		x [μm]	y [μm]		
246	`Bufbias`	1409.12	5967.52	output	analogue probe pad
247	`Shabias1`	1294.12	5967.52	output	analogue probe pad
248	`Shabias`	1179.12	5967.52	output	analogue probe pad
249	`Prebias1`	1064.12	5967.52	output	analogue probe pad
250	`Prebias`	949.12	5967.52	output	analogue probe pad

B.8 List of known problems and bugs

1. readout behaviour at consecutive triggers
2. the last chip in a daisy chain (*DaisyLast*) is sensitive to external signals on the return token port: pad `RoReTokenIn` needs to be grounded for proper chip operation for the last chip in the chain
3. division factor between *Rclk* and *Sclk* (R=*Sclk*/*Rclk*) is restricted to ≤ 2
4. large bias current of the analogue output driver (factor 5 larger compared to predecessor version *Beetle1.1*)
5. the variation of the readout baseline

Beside a fix of the above mentioned problems and bugs, a further chip version will integrate 5 V compatible I^2C-pads, which will render superfluous any external (radiation hard) level shifting devices.

Bibliography

[1] R. Brenner et al., Nucl. Instr. and Meth. A339 (1994) 564

[2] CLC400, Fast Settling, Wideband Low Gain Monolithic Op Amp, National Semiconductor

[3] National Semiconductor, DS90C032 LVDS Quad CMOS Differential Line Receiver, June 1998

[4] The I^2C-bus and how to use it, Philips Semiconductors, 1995

[5] Bi-directional level shifter for I^2C-bus and other systems, Application Note AN97055, Philips Semiconductors, 1998

Bibliography

[Abt01] I. Abt, Silicon Detectors, Lecture Notes, ICFA School on Instrumentation in Particle Physics, Faure, South Africa, April 2001

[All87] P.E. Allen, D. R. Holberg, CMOS Analog Circuit Design, Oxford University Press, 1987

[AMS] `http://ams.cern.ch/AMS/`

[Ane00] G. Anelli, Design and characterization of radiation tolerant integrated circuits in deep submicron CMOS technologies for the LHC experiments, Thesis, Institut National Polytechnique de Grenoble, 2000

[Ang98] A. Angelopoulos et al., First direct observation of time-reversal non-invariance in the neutral-kaon system, CPLEAR Collaboration, Phys. Lett. B444 (1998) 43

[Bab00] BaBar Collaboration, A Study of Time-Dependent CP-Violating Asymmetries in $B^0 \to J/\Psi K_s^0$ and $B^0 \to \Psi(2S)K_s^0$ Decays, arXiv:hep-ex/0008048

[Bab02] BaBar Collaboration, Measurement of the CP Asymmetry Amplitude $\sin 2\beta$, arXiv:hep-ex/0207042

[Bak87] J. F. Bak et al., Large departures from Landau distributions for high-energy particles traversing thin Si and Ge targets, Nucl. Phys. B288 (1987) 681

[Bak01b] N. van Bakel et al., Investigation of the characteristics and radiation hardness of the Beetle1.0 FrontEnd chip, revised LHCb-note 2001-037, VELO, 2001

[Bak02] N. van Bakel et al., Performance of the Beetle Readout Chip for LHCb, Proceedings of the 8th Workshop on Electronics for LHC Experiments, CERN/LHCC/2002-34 (2002) 121

[Bat02] J. R. Batley et al., A precision measurement of direct CP violation in the decay of neutral kaons into two pions, Phys. Lett. B544 (2002) 97

[Bau99] D. Baumeister, Entwicklung und Charakterisierung eines ASICs zur Kathodenauslese von MWPCs für das H1-Experiment bei HERA, Diploma Thesis, Universität Heidelberg (1999)

[Bel00] Belle Collaboration, A Measurement of CP Violation in B^0 Meson Decays with Belle, arXiv:hep-ex/0010008

[Bel02] Belle Collaboration, Improved Measurement of Mixing-induced CP Violation in the Neutral B Meson System, arXiv:hep-ex/0208025

[Bet30] H. A. Bethe, Zur Theorie des Durchgangs schneller Korpuskularteilchen durch Materie, Ann. d. Phys. 5 (1930) 325

[Bin75] D. Binder et al., Satellite Anomalies from Galactic Cosmic Rays, IEEE Trans. Nucl. Sci. Vol. 22 No. 6 (1975) 2675

[Blo33] F. Bloch, Bremsvermögen von Atomen mit mehreren Elektronen, Z. Phys. 81 (1933) 363

[Bre94a] R. Brenner et al., Design and performance of an analog delay and buffer chip for use with silicon strip detectors at LHC, Nucl. Instr. and Meth. A339 (1994) 564

[Bre94b] R. Brenner et al., Performance of a LHC front-end running at 67 MHz, NIM A339 (1994) 447

[Chr64] J. H. Christenson et al., Evidence for the 2π Decay of the K_2^0-Meson, Phys. Rev. Lett. 13 (1964) 138

[Chr99] J. Christiansen, I. Garcia, Simulation of the LHCb front-end, LHCb Technical Note, LHCb 99-047, 1999

[Dre89] P. V. Dressendorfer, T. P. Ma, Introduction, in: P. V. Dressendorfer, T. P. Ma (Editors), Ionizing Radiation Effects in MOS Devices and Circuits, Wiley, 1989

[Enz02] C. Enz, MOS Transistor Modeling for Low-Voltage and Low-Power Circuit Design, Course Notes, Low-Voltage Analog CMOS IC Design, EPFL Lausanne, June 2002

[Fal98] W. Fallot-Burghardt, A CMOS Mixed-Signal Readout Chip for the Microstrip Detectors of HERA-B, Thesis, Universität Heidelberg, 1998

[Fac98] F. Faccio et al., Total Dose and Single Event Effects (SEE) in a 0.25 μm CMOS Technology, CERN/LHCC/98-36 (1998) 105

[Fac99a] F. Faccio et al., SEU effects in registers and in a Dual-Ported Static RAM designed in a 0.25 μm CMOS technology for applications in the LHC, CERN/LHCC/99-33 (1999) 571

[Fac99b] F. Faccio, Radiation Effects in the Electronics for CMS, Tutorial Script, CERN, 1999

[Fac02] F. Faccio, personal communications

[Fan47] U. Fano, Ionization yield of radiations II: The fluctuations of the number of ions, Phys. Rev. 72 (1947) 26

[FEI] FEI Deutschland GmbH, `http://www.feicompany.com`

[FEP] Key parameters and features of LHCb front-end electronics
`http://lhcb-elec.web.cern.ch/lhcb-elec/html/key_parameters.htm`

[Feu99] M. Feuerstack-Raible, Overview of microstrip read-out chips, NIM A447 (2000) 35

[FLU] http://pcfluka.mi.infn.it/

[Gai95] R. Gaillard, J.-L. Leray, O. Musseau et al., Techniques de durcissement des composant, circuits, et systemes electroniques, Notes of the Short Course of the 3rd European Conference on Radiation and its Effects on Components and Systems, Arcachon (France), 1995

[Gat84] E. Gatti, P.F. Manfredi, Present Trends and Realisations in Readout Electronics for Semiconductor Detectors in High Energy Physics, NIM A226 (1984) 142

[Gei90] R. L. Geiger, P. A. Allen, N. R. Strader, VLSI Design Techniques for Analog and Digital Circuits, McGraw-Hill, 1990

[Gir98] A. Giraldo, Evaluation of Deep Submicron Technologies with Radiation Tolerant Layout for Electronics in LHC Experiments, Thesis, University of Padua, 1998 http://wwwcdf.pd.infn.it/cdf/sirad/giraldo/tesigiraldo.html

[Gra01] P. R. Gray et al., Analysis and design of analog integrated circuits, Wiley, 2001

[Gre86] R. Gregorian, G. Temes, Analog MOS Integrated Circuits for Signal Processing, Wiley, 1986

[Gri96] D. Griffiths, Einführung in die Elementarteilchenphysik, Akademie Verlag, Berlin 1996

[Hal00] G. Hall, APV25 Status and Results, IVth International Meeting on Front End Electronics for High Resolution Tracking Detectors, Perugia 2000

[Her95] The HERA-B collaboration, HERA-B Technical Design Report, DESY-PRC 95/01, 1995

[Her] http://www-hermes.desy.de/

[Hor93] R. Horrisberger et al., A novel readout chip for silicon strip detectors with analog pipeline and digitally controlled analog processing, NIM A326 (1993) 92

[Huh00] M. Huhtinen, F. Faccio, Computational method to estimate Single Event Upset rates in an accelerator environment, NIM A450 (2000) 155

[H1] H1 Collaboration, The H1-Detector at HERA, NIM A386 (1997) http://www-h1.desy.de/

[IEE01] IEEE 1149.1-2001 Test Access Port and Boundary-Scan Architecture, 2001

[ITR] http://lhcb.web.cern.ch/lhcb-track/html/innertracker/photos.htm

[ITR02] LHCb Inner Tracker Technical Design Report, CERN/LHCC/2002-029, November 2002

[Jan01] Plot prepared by E. Jans, NIKHEF, 2001

[Ker89] S. E. Kerns with contributions from B. D. Shafer, Transient-Ionization and Single-Event Phenomena, in: P. V. Dressendorfer, T. P. Ma (Editors), Ionizing Radiation Effects in MOS Devices and Circuits, Wiley, 1989

[Kip94] I. Kipnis et al., An Analog Front-End Bipolar Transistor IC for the SDC Silicon Tracker", IEEE Trans. Nucl. Sci. Vol. 41 No. 4 (1994) 1095

[Klu01] R. Kluit et al., Design of ladder EndCap electronics for the ALICE ITS SSD, Proceedings of the Seventh Workshop on Electronics for LHC Experiments, Stockholm, Sweden, CERN/LHCC/2001-034 47

[Kob73] M. Kobayashi, T. Maskawa, CP-Violation in the Renormalizable Theory of Weak Interaction, Prog. Theor. Phys. 49, 652 (1973)

[Lan44] L. Landau, J. Phys. (USSR) 8 (1944) 201

[Leh98] G. Lehmann et al., Schaltungsdesign mit VHDL, Franzis, Feldkirchen, 1998

[Leh02] F. Lehner at al., Description and Evaluation of Multi-Geometry Silicon Prototype Sensors for the LHCb Inner Tracker, LHCb-note 2002-038, 2002

[Leo94] W.R. Leo, Techniques for nuclear and particle physics experiments: a how-to approach, Springer 1994

[LHC98] LHCb Collaboration, LHCb Technical Proposal, CERN/LHCC 98-4, 1998

[Löc98] S. Löchner, Charakterisierung und Entwicklung eines CIP-Auslese-ASIC für das H1-Upgrade-Projekt 2000, Diploma Thesis, Universität Heidelberg (1998)

[Löc03] S. Löchner, Thesis in preparation

[Lüd57] G. Lüders, Ann. Phys. 2 (1957) 1

[Lut99] G. Lutz, Semiconductor radiation detectors: device physics, Springer 1999

[LVD97] National Semiconductors, LVDS Owner's Manual, Design Guide, Spring 1997

[Mas93] L. Massengill, IEEE Nuclear and Space Radiation Effects Conference (NSREC) 1993, Short Course, SEU Modeling and Prediction Techniques, 1993

[May78] T.C. May, M. H. Wodds, Alpha-Particle-Induced Soft Errors in Dynamic Memories, Proceedings of the 1978 IEEE International Reliability Physics Symposium (1978)

[McL89] F. B. McLean, H. E. Boesch Jr., T. R. Oldham, Electron-Hole Generation, Transport, and Trapping in SiO_2, in: P. V. Dressendorfer, T. P. Ma (Editors), Ionizing Radiation Effects in MOS Devices and Circuits, Wiley, 1989

[Mes86] G. C. Messenger, M. Ash, The Effects of Radiation on Electronic Systems, Van Nostrand Reinhold, New York 1986

[Mes97] G. C. Messenger, M. Ash, Single Event Phenomena, Chapman & Hall, 1997

[Mic01a] `http://proj-xraymic.web.cern.ch/proj-XrayMIC/`

[Mic01b] `http://proj-xraymic.web.cern.ch/proj-XrayMIC/calibration.htm`

[Nak02] T. Nakada, Status of the LHCb experiment, LHCb-note 2002-004, 2002

[Nat98] National Semiconductor, DS90C032 LVDS Quad CMOS Differential Line Receiver, June 1998

[Nat01] National Semiconductor, CLC400 Fast Settling, Wideband Low Gain Monolithic Op Amp, Data Sheet, February 2001

[NIK] `http://www.nikhef.nl/pub/experiments/bfys/lhcb/vertex/hybrid.html`

[Noe18] E. Noether, Nachr. Ges. Wiss., Göttingen 1918, 171

[Nyg91] E. Nygård et al., CMOS low noise amplifier for microstrip readout, Design and results, NIM A301 (1991) 506

[PDG00] Particle Data Group, Particle Physics Booklet, July 2000
`http:pdg.lbl.gov/`

[Pau55] W. Pauli, Niels Bohr and the Development of Physics, W. Pauli, Editor, McGraw-Hill, New-York 1955

[Pet97] E. L. Peterson, IEEE Nuclear and Space Radiation Effects Conference (NSREC) 1997, Short Course, Single-Event Analysis and Prediction, 1997

[Phi95] The I^2C-bus and how to use it, Philips Semiconductors, 1995

[Pol] Polytec GmbH, Waldbronn, Germany, EPO-TEK H20S, data sheet,
`http://www.polytec.com/polytec-com/index.html`

[Rad] `http://lhcb-background.web.cern.ch/lhcb-background/`

[RIC00] Technical Design Report LHCb RICH, 2000, CERN/LHCC/2000-037 (2000)

[RD49] 3rd RD49 Status Report, Study of Radiation Tolerance of ICs for LHCb, CERN/LHCC/2000-003 (2000)

[Roh95] H. Rohling, Einführung in die Informations- und Codierungstheorie, Teubner Stuttgart, 1995

[Sak67] A. D. Sakharov, JETP Lett. 6 (1967) 21

[Sak84] N. S. Saks et al., Radiation Effects in MOS Capacitors with Very Thin Oxides at 80 K, IEEE Trans. Nucl. Sci. Vol. 31, No. 6 (1984) 1249

[Sak86] N. S. Saks et al., Generation of Interface States by Ionizing Radiation in Very Thin MOS Oxides, IEEE Trans. Nucl. Sci. Vol. 33, No. 6 (1986) 1185

[Sch02] M. Schmelling, The LHCb Experiment, Four Seas Conference, Thessaloniki, Greece, April 2002

[SE] Silicon Ensemble, Cadence Design Systems Inc.

[Sex01] E. Sexauer, Development of Radiation Hard Readout Electronics for LHCb, Thesis, Universität Heidelberg, 2001

[Sho52] W. Shockley, Statistics of the recombination of holes and electrons, Phys. Rev. 87 (1952) 835

[Sie02] P. Sievers, personal communications

[Sma03] N. Smale, Thesis in preparation

[Spi96] H. Spieler, Introduction to Radiation-Resistant Semiconductor Devices and Circuits, 1996, `http://www-physics.lbl.gov/~spieler`

[Spi01] H. Spieler, Radiation Detectors and Signal Processing, Heidelberg 2001, Lecture Notes

[Sta00] U. Stange, Charakterisierung und Weiterentwicklung des CIPix, Diploma Thesis, Universität Heidelberg (2000)

[Ste02] O. Steinkamp, The Silicon Inner Tracker for LHCb, LHCb-note 2002-019, 2002

[Syn00] Synopsys Online Documentation v2000.11, Synopsys Inc., 2000

[Tho96] D. Thomas, P. Moorby, The Verilog Hardware Description Language, Kluwer Academic Publishers, 3rd Edition, 1996

[Tie93] U. Tietze, Ch. Schenk, Halbleiter-Schaltungstechnik, Springer 1993

[Tru00] U. Trunk, Development and Characterisation of the Radiation tolerant HELIX128-2 Readout Chip for the HERA-B Microstrip Detectors, Thesis, Universität Heidelberg, 2000

[Vas00] A. Vasilescu, G. Lindstroem, Displacement Damage in Silicon, on-line compilation `http://sesam.desy.de/members/gunnar/Si-dfuncs.html`

[VEL01] Technical Design Report LHCb VELO, 2001. CERN/LHCC/2001-011 (2001)

[Ver99a] H. Verkooijen, Technical Report about the status of the comparator on the Beetle chip, NIKHEF Amsterdam, July 1999

[Ver99b] H. Verkooijen, Technical report about the status of the comparator on the Beetle chip, NIKHEF Amsterdam, November 1999

[Vit02] E. Vittoz, Limits to Low-Voltage Analog Design, Course Notes, Low-Voltage Analog CMOS IC Design, EPFL Lausanne, June 2002

[Wag92] H. G. Wagemann, Halbleiter, in: Lehrbuch der Experimentalphysik, Bergmann, Schäfer, Bd. 6 Festkörper, de Gruyter, Berlin, New York 1992

[Wak94] J. F. Wakerly, Digital Design Principles and Practices, 2nd Edition, Prentice-Hall, 1994

[Wea02] T. Weatherford, IEEE Nuclear and Space Radiation Effects Conference (NSREC) 2002, Short Course, From Carriers to Contacts, A Review of SEE Charge Collection Processes in Devices, 2002

[Win89] P. S. Winokur, Radiation-Induced Interface Traps, in: P. V. Dressendorfer, T. P. Ma (Editors), Ionizing Radiation Effects in MOS Devices and Circuits, Wiley, 1989

[Wol83] L. Wolfenstein, Parametrization of the Kobayashi-Maskawa Matrix, Phys. Rev. Lett. 51, (1983) 1945

[Wu57] C. S. Wu et al., Experimental Test of Parity Conservation in Beta Decays, Phys. Rev. Lett. 105, (1957) 1413

[Zeu] `http://www-zeus.desy.de/`

Danke

Mein besonderer Dank gilt meiner Frau ***Katja*** für all das, was sich in Worten nicht ausdrücken lässt. Ihre Liebe, Unterstützung und Geduld waren Grundlage für ein erfolgreiches Arbeiten.

Prof. Dr. Werner Hofmann danke ich für die Aufnahme als Doktorand. Die Betreuung war durch grosse Freiräume und Eigenständigkeit gekennzeichnet, die ich sehr geschätzt habe.

Prof. Dr. Johanna Stachel möchte ich für die prompte und freundliche Übernahme des Zweitgutachtens danken.

Prof. Dr. Michael Schmelling danke ich für die sehr angenehme Betreuung und Zusammenarbeit und seine grosse Hilfsbereitschaft. Danke für das kritische Korrekturlesen dieser Arbeit.

Prof. Dr. Karl-Tasso Knöpfle möchte ich für die Betreuung in den wöchentlichen Gruppensitzung der HERA-*B*-VDS/LHCb Gruppe am MPIK danken. Seine wissenschaftliche Arbeitsweise haben mich geprägt und motiviert.

Dr. Ulrich Trunk danke ich für die kollegiale Zusammenarbeit. Danke für die Hilfestellungen bei fortgeschrittenen Problemen mit LaTeX und der stetigen Verfügbarkeit als "designer on demand".

Sven Löchner danke ich im Besonderen. Seine Hilfsbereitschaft kennt nahezu keine Grenzen und reicht von der Anlieferung von Cola bis zur Bereitstellung von Scannern, Druckern, Routern, USV, etc. Die gemeinsame Entwicklung der drei Chip-Iterationen, sowie die Bestrahlungstests, haben auch in stressigen Phasen immer Spass gemacht. Danke für das Korrekturlesen dieser Arbeit.

Der Auslese-Chip Gruppe des ASIC-Labors, ***Uwe Stange***, ***Harald Deppe***, ***Andre Srowig***, möchte ich für die gute Arbeitsatmosphäre und den wöchentlichen Austausch und Diskussionen danken. Uwe empfehle ich nachwievor, morgens ein Frühstück einzunehmen, um nicht schon um 11.30 Uhr von Magenknurren in die Mensa getrieben zu werden.

Dr. Christian Bauer und ***Dr. Bernhard Schwingenheuer*** danke ich für die vielen Ratschläge aus langjährigen Erfahrungen mit dem HELIX Chip bei HERA-*B*. Sie waren stets Ansprechpartner für Fragen und Probleme aller Art. Die schnelle Beschaffung von Elektronik-Bauteilen durch Christian beseitigte vielfach materielle und zeitliche Engpässe.

Der ***HERA-B-VDS/LHCb Gruppe des MPIK*** danke ich für die angenehme Atmosphäre in den wöchentlichen Gruppensitzungen und die lehrreichen Einblicke in die Datenanalyse.

Dr. Edgar Sexauer danke ich für die schöne Zusammenarbeit in den Anfangsphasen des *Beetle* und die Einführungen in analoges Schaltungsdesign.

Thanks to ***Nigel Smale*** for the nice time during his visits in Heidelberg, inside and outside the laboratory. Since he still not yet learned German, I write this in English. Hope this will change in the near future!

Der ***VELO-Gruppe am NIKHEF*** sowie der ***ITR-Gruppe in Zürich*** möchte ich für die gute Zusammenarbeit danken. Die holländische Gastfreundlichkeit nach langen Sitzungen soll hier besondere Erwähnung finden.

Der ***Vision-Gruppe*** des ASIC-Labors möchte ich für die gute Zusammenarbeit und die schönen Abende beim monatlichen ASIC-Treffen im "Gilberts" danken.

Ralf Achenbach danke ich für die Unterstützung bei allen "bond-spezifischen" Problemen sowie Fragen der Messtechnik. Seiner stetigen Fürsorge für die Bond-Maschine ist es zu verdanken, dass Chips in kürzester Zeit in Betrieb genommen werden können, ohne langwierige Justierung, Nadelreinigung, Einfädel-Übungen etc.

Michael Keller und seinem Nachfolger ***Markus Dorn*** danke ich für die Administration der "Cadence"-Datenbank und die schnelle Behebung von Netzwerkproblemen.