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The Link-Board Control in the RPC Trigger System for the CMS Experiment

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ACADEMIC DISSERTATION

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Abstract

The Compact Muon Solenoid (CMS) will be a general-purpose detector designed to run at the highest luminosity at CERN's Large Hadron Collider (LHC). The CMS detector has been optimized for the search of the Higgs Boson over a mass range from 90 GeV to 1 TeV, but it also allows detection of a wide range of possible signatures from alternative electro-weak symmetry breaking mechanism.
The importance of using a powerful Detector Control System (DCS) has much increased with the size and complexity of High-Energy detectors.
The generation of detectors for the LHC experiments puts further requirements onto the front-end I/O system due to the inaccessibility of the equipment and the hostile environment concerning radiation and magnetic field.
All of the CMS components shall be controllable. This control system will not only be used during the data taking periods but also during the test, calibration and standby periods and during part of the shutdown periods.
The work described in this thesis concerns the Link-Board control (in the RPC trigger system) through a 'Control Board' (CB), a small PCB (Printed-Circuit Board) containing, among others, the CCU (Communication and Control Unit) chip, developed at CERN by the CMS Tracker control group. In the final part of this work I will present the results from different tests in which the prototypes of the RPC electronic readout system were used.

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Introduction

At CERN (the European Organization for Nuclear Research) in Geneva, a new particle collider, the LHC (Large Hadron Collider), has been designed and is being built. The LHC project consists primarily of the addition to the already existing LEP (Large Electron–Positron collider) tunnel of a superconducting magnet system with two beam channels.

While LEP collided electrons and positrons with a centre-of-mass energy of up to 200 GeV, the LHC is designed to bring two proton beams into collision, resulting in 14 TeV centre-of-mass collisions. As experiments are more and more complex, the amount of data taken for one interaction becomes very large. In the case of the CMS (Compact Muon Solenoid) experiment at the LHC, 40 Tbytes/s originating from 10^8 channels have to be read out and stored in pipelines. A multi-level triggering system is used to reduce the amount of data that is stored for further analysis. The first-level (L1) muon trigger is one of the most important parts in the CMS detector design for the discovery of new physics. It has to reduce the LHC input rate of 40 MHz to no more than 25 kHz.

The CMS Collaboration has chosen resistive-plate chambers (RPCs) as dedicated detectors for the first-level muon trigger system. They will be located at the outer surface of the cylindrical CMS detector, both in the barrel and endcap muon stations, and they will be exposed to an average dose of 10 Gy over 10 years of LHC operation at the luminosity of 10^{34} cm^{-2} s^{-1}.

The RPCs will be used in the L1 of the trigger system to indicate when interesting patterns of muon tracks emerge from the interaction point. These patterns of muon tracks, together with the information from various other subdetectors, are used to choose potentially interesting data from the entire detector, including the RPCs themselves. The CMS RPC readout system is made up of four components: the Front-End Boards, the Link Board, the Splitter Board and the Trigger and Readout Boards. This thesis is focused on the Link Board, which is the heart of the data transmission, control and calibration features of the system. In particular, the aim of this work was to find a solution for the final implementation of the Link-Board control.

All the CMS components must be controllable. This control system will be used during the data-taking periods as well as during the test, calibration and standby periods, and also during part of the shutdown periods. The purpose of the Detector Control System (DCS) of the CMS experiment is to control high and low voltages, gas, cooling and temperature in each subdetector, to control the downloading of all necessary constants and programs to the front-end cards, and to control the calibration of the data taking within the local Data Acquisition (DAQ) of each subdetector. Using guidelines provided by the DCS, each of the subdetector groups defines the data acquisition and control functions it needs for a subdetector.

The work described in this thesis concerns the Link-Board control through a ‘Control Board’ (CB), a small PCB (Printed-Circuit Board) containing, among others, the CCU

(Communication and Control Unit) chip, developed at CERN by the CMS Tracker control group. In this way the Link-Board control in the RPC system will be compatible with the general CMS DCS. In the final part of this work I will present the results from different tests in which the prototypes of the RPC electronic readout system were used.

The thesis is organized as follows:

An overview of the physics studies that will be done at the LHC is given in Chapter 1, together with a description of the LHC collider and CMS detector.

The general CMS L1 muon trigger and its performance are given in Chapter 2**.**

Chapter 3 is dedicated to the general description of the DCS architecture. The hardware and software tools needed for the control and their connection in a big experiment such as CMS are also described.

An overview of the RPC system is discussed in Chapter 4, where a detailed description of its front-end electronics is given. In this chapter the Link Board will also be fully described.

Chapter 5 is entirely dedicated to the Link-Board control and to the research evolution that was done before arriving at the final solution, the CB.

The CB will be presented in Chapter 6, mainly focused on the control technical requirements in the Link-Board system, and on the description of the board itself.

Chapter 7 contains the experimental results obtained from different tests performed at CERN and made with a full readout chain in an LHC-like test beam.

The results from the RPCs cosmic-rays test made in Bari are presented in Chapter 8.

Since the LBs will be located on the detector, the transmitting side of the link will be subject to ionizing radiation and high-energy particles, which can cause both long-term radiation damage and single-event upsets. Since the RPCs and their electronics will be located on the outer surface of the CMS detector, the doses are relatively low, and standard commercial components can be used to a certain extent. However, irradiation tests are required for all components chosen for the production version to ensure that they will function satisfactorily throughout the 10-year lifetime of the experiment. These tests were done at the Jyväskylä Accelerator Laboratory; the results and data analyses are discussed in Chapter 9.

The final remarks and the main results of my research work are outlined in the Conclusions.

1 The LHC and the CMS experiment

1.1 Theoretical introduction

1.1.1 Fundamental interactions and elementary particles

The fundamental constituents of matter are called ‘elementary particles’. The word ‘elementary’ is used in the sense that such particles have no inner structure, i.e. they are point-like [1]. All fundamental particles in nature can be divided into two categories, fermions and bosons (see Fig. 1).
A fermion is any particle that has odd-half-integer (1/2, 3/2, …) intrinsic angular momentum (spin). As a consequence of this odd-half-integer angular momentum, fermions obey a rule called the ‘Pauli exclusion principle’, which states that no two fermions can exist in the same state (identical spin, colour charge, angular momentum, etc.) at the same place and time. Electrons, protons and neutrons are all fermions. More generally all the fundamental matter particles, quarks and leptons, and the composite particles, baryons, are fermions.
A boson is instead a particle that has integer spin (0, 1, 2, …). All the particles that carry a force are bosons, as are those composite particles with an even number of fermion constituents (like mesons).
Elementary particles are then characterized by the way they interact with one another.

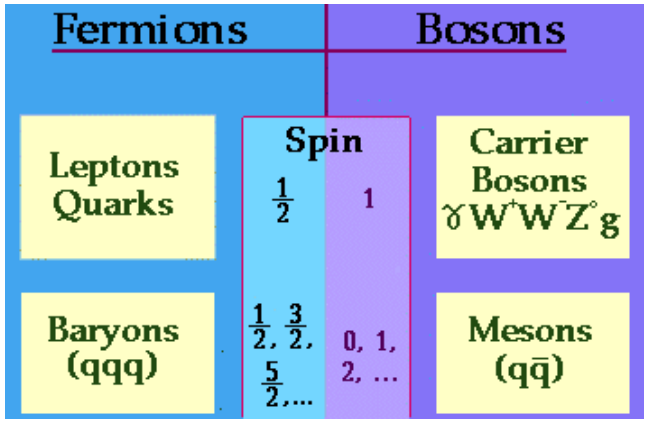


Figure 1 Fermions and bosons chart

Four different fundamental interactions are known: electromagnetic, weak, strong and gravitational.
The single basic force responsible for the structure of the atom is the ‘electromagnetic interaction’. This single force, together with the laws of quantum mechanics, which tell

us, through the Schrödinger equation and the Pauli principle, how the particles behave under its action, determines completely all chemical and biological properties of matter.
With the discovery of the internal structure of the nucleus, however, the situation became complicated, since a new fundamental force, the 'strong interaction', hitherto unobserved in any macroscopic experiment, was needed to explain how the nucleons were held together in a nucleus. The strong interaction is thus called because it is apparently stronger at short distances than the electromagnetic interaction.
In addition to the strong interaction, which is necessary to hold together the constituents of the nucleus, there is a 'weak interaction', which causes certain elementary particles to decay to other elementary particles. As an example of decay through the weak interaction, the neutron decays to a proton with the emission of an electron and a massless particle known as the 'neutrino'.
The fourth and weakest fundamental force is the 'gravitational interaction'. All of the elementary particles, including the massless photon and the neutrino, take part in the gravitational interaction. However, on the elementary particles scale the gravitational interaction is negligible with respect to the other forces.

1.1.2 The Standard Model of particle physics

In the last three decades, significant progress has been made in the identification of fundamental particles and the unification of their interactions. This remarkable result is summarized by what is now called the Standard Model (SM), formulated in the 1970s.
According to the SM, three types of particles can be distinguished: quarks, leptons and force-carrying bosons. The quarks and leptons are fermions, spin ½ particles that obey the so-called Fermi–Dirac statistics. They can be grouped into three families of increasing mass scale. Each family consists of four particles, two leptons and two quarks. Also the antiparticles of these particles exist, i.e. objects with the same mass and lifetime as their corresponding particle, but with opposite sign of charge and magnetic moment.
The known elementary leptons are given in Table 1, together with the non-zero lepton numbers. The masses are quoted in energy units, i.e. the value of the rest energy mc^2, in eV or MeV. The muon μ and the lepton τ are heavier, unstable versions of the electron. The muon μ was discovered as a component of the cosmic radiation in 1937 [1]. The muons are decay products of short-lived mesons (pions), which are integral-spin particles produced in the upper atmosphere by primary cosmic-ray protons from space. The τ lepton was first observed in accelerator experiments in 1975. These three 'flavours' of charged lepton are paralleled by three flavours of neutral lepton (neutrino). The upper limits to the neutrino masses are all small with respect to those of the corresponding charged leptons, with which they are produced in association in weak interactions. In the SM, neutrinos are assumed to be massless. Charged leptons undergo both electromagnetic and weak interactions, while neutrinos interact only weakly.

Generation	Lepton name	Charge	Mass [MeV][3]	Lepton number
First generation	e electron ν_e electron neutrino	–1 0	0.511 ~ 0	$L_e=1$ $L_e=1$
Second generation	μ muon ν_μ muon neutrino	–1 0	105.658 < 0.17	$L_\mu=1$ $L_\mu=1$
Third generation	τ tau ν_τ tau neutrino	–1 0	1777 < 24	$L_\tau=1$ $L_\tau=1$

Table 1: The leptons (spin ½). The antiparticle of the electron is called the positron.

Generation	Flavour name	Charge	Mass [GeV]	Additional non–zero quantum number
First generation	*d* down *u* up	–1/3 +2/3	0.002–0.005 0.002–0.008	I_z= -1/2 I_z= 1/2
Second generation	*s* strange *c* charm	–1/3 +2/3	0.1–0.3 1.0–1.6	S= –1 C= 1
Third generation	*b* bottom *t* top	–1/3 +2/3	4.1–4.5 180 ± 12	B= –1 T= 1

Table 2 The quarks (spin ½). The masses of the quarks are not very well defined. The given masses are the so-called 'current quark masses', which are relevant to kinematics in hard processes.

Boson	Charge	Mass [GeV]	Force
8 gluons	0	0	Strong
$W^{\pm}$	±1	80.33	Weak
Z^0	0	91.19	Weak
Photon (γ)	0	0	Electromagnetic

Table 3 The force-carrying bosons (spin 1).

The known elementary quarks are given in Table 2. All quarks have baryon number 1/3. The additional non-zero quantum numbers, describing the quark flavour, are also given in Table 2. Quarks do not exist as free particles and thus the definition of mass is somewhat indirect. Two types of quarks combinations are established as existing in nature:

Baryon = qqq (three-quark state)
Meson = $q\bar{q}$ (quark–antiquark pair)

These strongly interacting quark composites are collectively referred to as 'hadrons'.

Quarks are held together by an exchange of neutral gluons (Table 3), the carriers of the strong force, and the 'constituent' quark masses include all such quark-binding effects.
The quantum number I_z is called the isospin. Each quark has an additional quantum number called colour, for which three values are possible.
Leptons can occur freely in space, while quarks occur only in a bound state (all naturally occurring particles are colourless, meaning that either the total amount of each colour is zero or all the colours are present in equal amounts).
There exist bound states of three quarks (baryons, qqq), of three antiquarks (antibaryons, $\overline{qqq}$) and of a quark with an antiquark ($q\bar{q}$). The bound states of quarks are also referred to as hadrons. The only existing stable baryon is the proton (uud). The neutron (udd) is only stable when bound in a nucleus. The mesons are always unstable. The π and K mesons are relatively long-lived and can be detected directly in particle physics experiments.
The force-carrying bosons are spin 1 particles. Each of three forces playing a role in particle physics has its own bosons (Table 3).

1.1.3 Interactions in the Standard Model

The electromagnetic force couples to the electric charge and is mediated by the photon. All charged particles are subject to the electromagnetic force. The strong force couples to colour and is mediated by eight gluons. All coloured particles (quarks and gluons) are subject to the strong force. Owing to the strong force, a 'sea' of gluons and short-lived quark–antiquark pairs surround the valence quarks in the bound state of a hadron. The $W^{\pm}$ and Z^0 bosons (massive vector bosons) carry the weak force. All leptons and quarks are subject to the weak force.
In all interactions the electric charge, colour, baryon number and lepton number are conserved. The quark flavour is a conserved quantity in the strong and electromagnetic interaction but not in the weak interaction.
In the Grand Unified Theory (GUT) it is assumed that the strong, weak and electromagnetic interactions unify at a very high-energy scale $M \sim O(10^{15}\text{GeV})$. If also the gravitational force (produced by mass) is included in the grand unification, also this force should be carried by a hypothetical particle of spin 2, the graviton. Until now, however, the graviton has not been observed.

1.1.4 Beyond the Standard Model

The Standard Model incorporates the fundamental fermions (three pairs of quarks and three of leptons), the interactions between them being mediated by gauge fields carried by the bosons $W^{\pm}$, Z^0 and γ of the electroweak sector and, between the quarks only, by the gluons g of the strong sector. The SM has been outstandingly successful in accounting for essentially all the data from laboratory experiments to date. However, there are a number of shortcomings and problems with the SM, which does not explain its

most obvious features: the pattern of masses and forces, the different generations of particles, and the relationship between the quarks and leptons.
Theorists are working on ideas going beyond the SM, which unify all of the forces at high energies. So far, however, we have experimental evidence only for the unification of the electromagnetic and weak forces. The currently favoured idea in unification is 'supersymmetry', in which each of the known particles has a heavier supersymmetric partner (the mathematics of particle physics is built on the concept of fundamental symmetries in nature). Another idea to unify the forces involves the existence in our Universe of more dimensions than the three of space and one of time we know about.
In some minimal extensions of the SM, neutral Z or charged W force-carrying bosons are included, with masses up to 6 TeV. Simulations show that if such charged bosons exist, their mass could be measured with an accuracy (for the LHC experiment) of about 50–100 GeV.
In many theoretical models beyond the SM, leptoquarks are predicted, inspired by the symmetry between the quark and lepton generations. These particles carry both lepton and baryon quantum numbers and hence couple to both leptons and quarks, making transitions between quarks and leptons possible. Moreover, each fermion generation is associated with a different leptoquark. Simulations show that these leptoquarks could be observed easily at the LHC if their mass is below 1 TeV.

1.2 The Large Hadron Collider

1.2.1 The LHC project

During the last few decades there has been enormous progress in the understanding of the basic composition of matter. As described in the previous sections, the theory of fundamental particles and their interactions, the Standard Model, answers many of the questions on the structure and stability of matter. The Higgs particle, needed to introduce a mechanism for mass generation in the SM, has not yet been observed.
The search for the Higgs particle in the largest possible mass range is probably the main motivation for the construction of the Large Hadron Collider (LHC). However, experiments will also investigate such questions as the search for heavy W– and Z–like objects, supersymmetric particles, compositeness of the fundamental fermions, CP violation in b decays and studies of the top quark [2].
The LHC project, approved by the CERN Council in December 1994, will be installed in the 27 km circumference tunnel formerly used by LEP, the Large Electron–Positron collider, at CERN (see Fig. 2). The LHC is a remarkably versatile accelerator. It should collide proton beams with energies around 7-on-7 TeV at beam crossing points of unsurpassed brightness, providing the experiments with high interaction rates. It can also collide beams of heavy ions such as lead, with total collision energy in excess of 1250 TeV.
At present, four main experiments are proposed to run at the LHC. The two largest, Compact Muon Solenoid (CMS) and A Toroidal LHC ApparatuS (ATLAS) are general-

purpose experiments that take different approaches, in particular to the detection of muons.
CMS is built around a very high field solenoid magnet; its relative compactness derives from the fact that there is a massive iron yoke so that the muons are detected by their bending over a relatively short distance in a very high magnetic field.
The ATLAS experiment is substantially bigger and essentially relies upon an air-cored toroidal magnet system for the measurement of the muons.
Two more special-purpose experiments have been approved to start their operation at the switch on of the LHC machine: the Large Ion Collider Experiment (ALICE) and the LHC-b experiment.
ALICE is a dedicated heavy-ion detector that will exploit the unique physics potential of nucleus–nucleus interactions at LHC energies. At these extreme collision energies, a new phase of matter, the quark–gluon plasma, could be produced.
The LHC-b collaboration is building a forward collider detector dedicated to the study of CP violation and other rare phenomena in the decays of beauty particles.

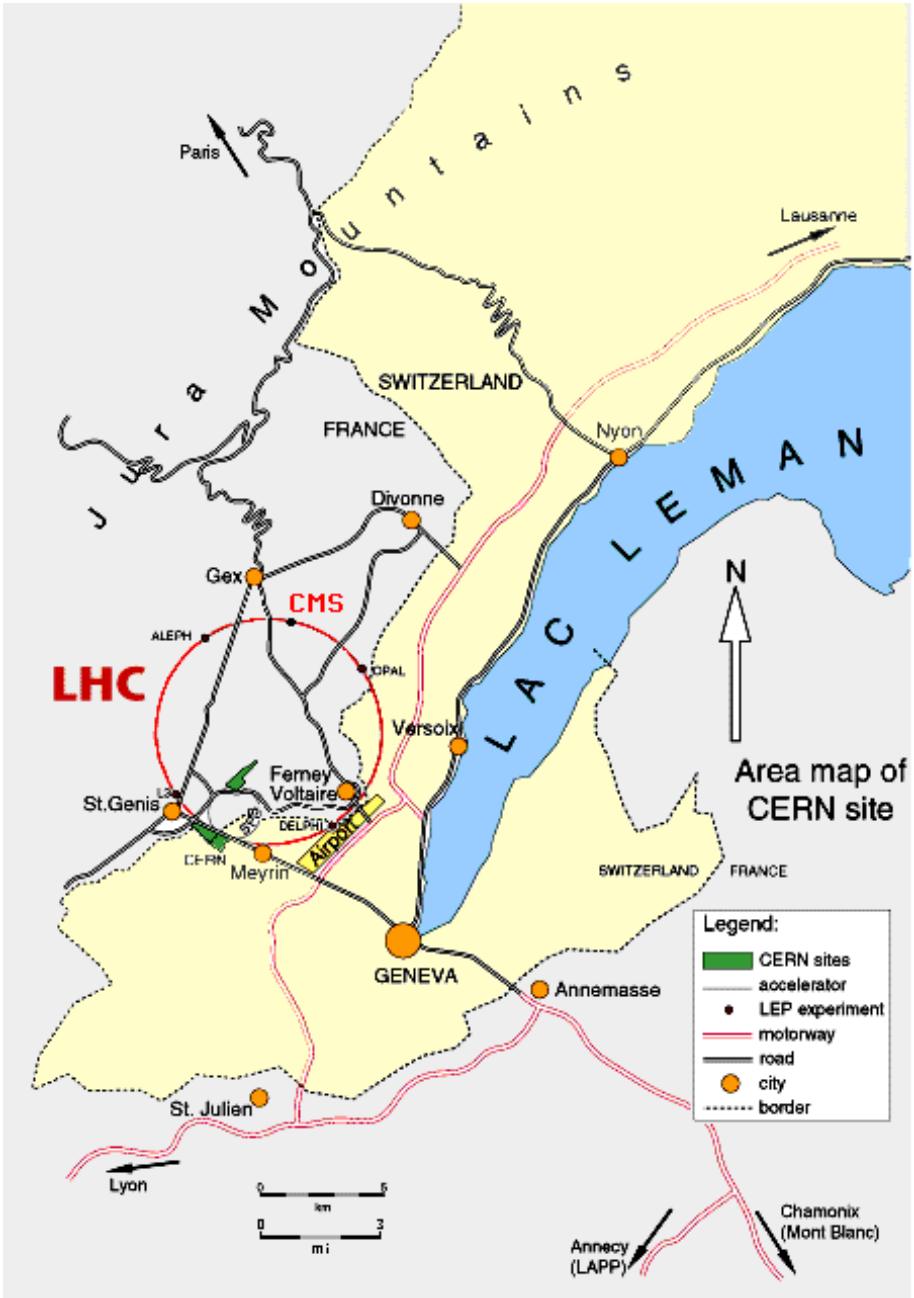


Figure 2 The Large Hadron Collider situation

1.2.2 General considerations

From the particle physics point of view, two parameters define the performance of a collider: the centre-of-mass energy and the luminosity. The former increases with the energy of the colliding particles, the latter is proportional to the number of collisions per second. In a circulating accelerator, the momentum p of a charged particle is related to the bending field B and the radius of curvature of its trajectory ρ by

p [GeV/c] = 0.3 B [T] ρ [m].

The only practical way of obtaining the high magnetic fields required is to use superconducting materials. Since the cross section for the production of massive particles varies as $1/E^2$ (E is the mass of the particle), the LHC has to be designed for the largest possible luminosity. In a circular accelerator, the particles are concentrated into bunches. If there are k_b bunches spread around the machine, each containing N particles, the luminosity L is defined as

$$L = \frac{N^2 k_b f \gamma}{4\pi\varepsilon_n \beta^*} F ,$$

where f is the revolution frequency, γ the relativistic factor, ε_n the normalized transverse emittance, β^* the betatron function at the interaction point, and F is the reduction factor caused by the finite crossing angle.
As can be seen from the previous equation, the luminosity increases as the number of particles per bunch and the total number of bunches in the machine are increased, and the intersection area is reduced. The most important limitation to the luminosity comes from the beam–beam interactions when the particles are at the intersection point, or near to it, since at this point the Coulomb forces tend to deflect the particles from their ideal orbits. If the bunches are very closely separated and the crossing angle is small, then the Coulomb forces act even as the bunches pass each other outside the interaction point.
The LHC luminosity will be 10^{34} cm^{-2} s^{-1}and an average of 17 events will occur at the beam crossing frequency of 25 ns.

1.2.3 Layout of the LHC machine

The layout of the LHC machine is shown in Fig. 3 (a full description of its layout can be found in [3]).

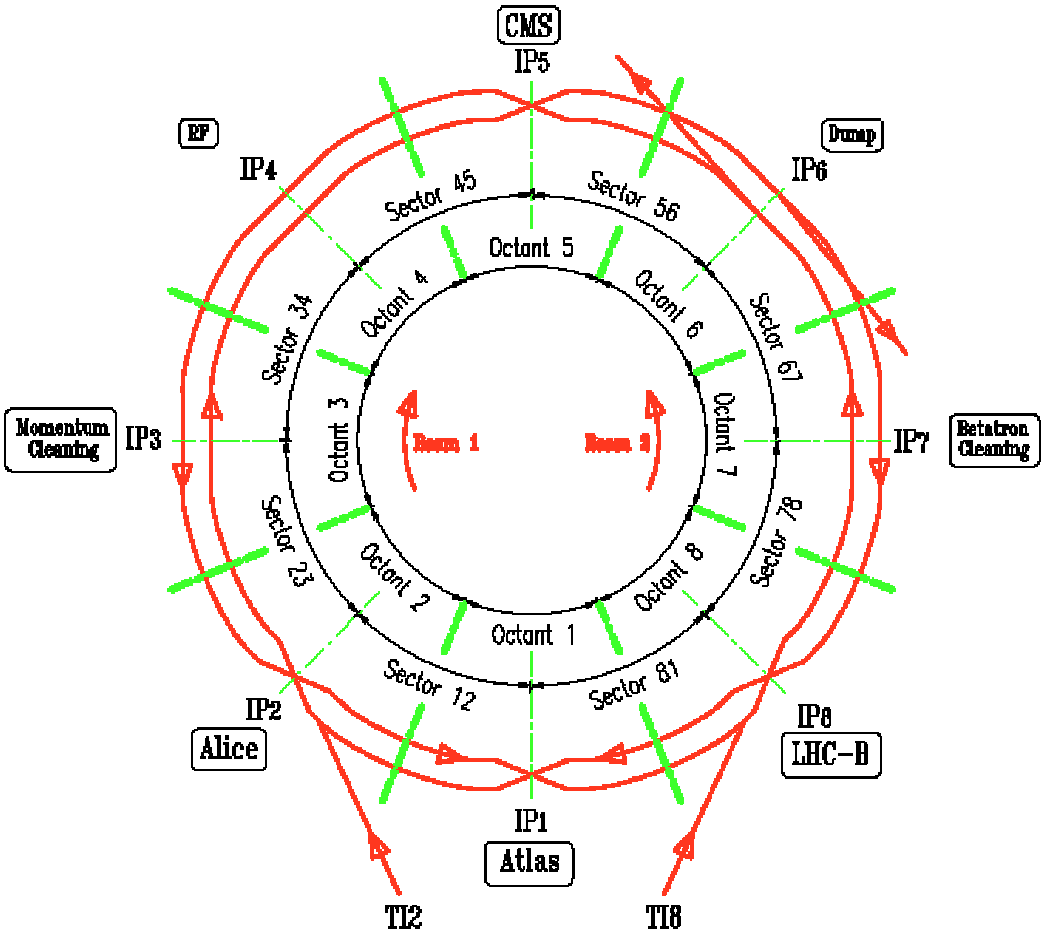


Figure 3 LHC machine layout

The ring is divided into octants, at the centre of which the beams can intersect, IP1–IP8 (only four of eight possible crossing regions are used for physics).
The ATLAS and CMS experiments are situated at points 1 and 5 respectively, while the ALICE and LHC-b experiments are situated at points 2 and 8 respectively.
All four of these intersections are equipped with so-called high-luminosity insertions that focus the beams down to very small dimensions.
At points 2 and 8 the beams will be injected into the machine. The points that are unused for experiments contain essential elements for the operation of the machine: RF, beam cleaning and beam dump.
The parts of the machine between intersection points are called ‘sectors’. The central region of each of the sectors is equipped with the bending magnets that keep the protons in their orbit. Each sector has an ‘arc’ of bending magnets, where an arc is made up of 23

cells, each containing six 14.2 m long bending dipoles. Also included in the cell is a pair of oppositely polarized quadrupoles, which have the essential role of maintaining the particles in orbit by focusing and defocusing the protons.
In addition, each arc contains a number of sextupole/dipole correctors to compensate for the inevitable inaccuracies in the main dipoles. At each end of the arcs there are dispersion suppressors, consisting of four quadrupoles interleaved with four pairs of standard bending dipoles. The combination of dispersion suppressor, arc and second dispersion suppressor constitutes the bending region of the machine.

1.2.4 Physics searches at the LHC

The fundamental goal of the LHC, and perhaps of all present-day high-energy colliders, is to uncover and explore the physics behind electroweak symmetry breaking. The new high-energy regime also offers a unique opportunity to look for the unknown and (in some cases) unexpected, while the very high cross sections and resulting event rates make the LHC a true factory for the production of particles such as the top quark.
The study of electroweak symmetry breaking involves the following steps:

- Discover (or exclude) the single Higgs boson of the SM and/or the multiple Higgs boson of supersymmetry;
- Discover (or exclude) supersymmetry in essentially the full theoretically allowed mass range;
- Discover (or exclude) new dynamics at the TeV scale.

As for new phenomena, there is a true multitude of them, some being perhaps less well motivated than others. Examples (always at the ~1–10 TeV scale) are:

- Possible new electroweak gauge bosons with masses below several TeV;
- New quarks or leptons;
- Extra dimensions with a mass scale of a few TeV.

Finally, high-rate phenomena can be used to measure precisely the properties of heavy flavours. There is even some place for b physics, at low luminosity.
The main physics studies at the LHC [4] are briefly described in the following sections.

1) **Higgs boson physics**

The search for the SM Higgs boson has motivated much of the design of the two experiments (ATLAS and CMS) at the LHC. There is only one free parameter in the SM Higgs: its mass. All other properties of the SM Higgs are fixed once its mass is known. The current limit on the Higgs mass, obtained from experiments at LEP, is $m_H > 114.5$ GeV. The SM Higgs boson is searched at the LHC in various decay channels, the choice of which is given by the signal rates and the signal-to-background ratios in the various mass regions.

The most suitable Higgs decay channels in the various possible mass ranges are presented below; they can also be seen in Fig. 4.

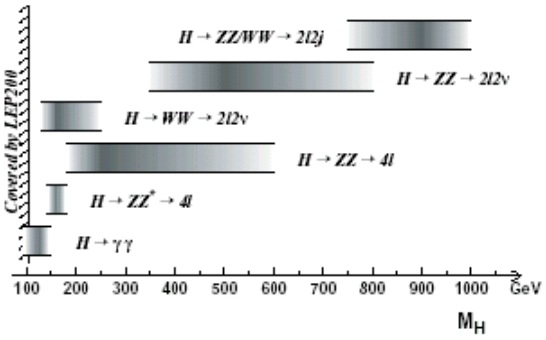


Figure 4 Most useful experimental signatures for Higgs search at the LHC and the corresponding mass ranges

a) Low Higgs mass ($m_H \leq 130$ GeV): the most promising channel for the low Higgs masses is the decay to $\gamma\gamma$ *(*$H \rightarrow \gamma\gamma$*)*, which has a tiny branching fraction but the promise of a very narrow mass peak. Excellent photon-energy resolution is thus required to observe this signal. At low Higgs masses, Higgs production in association with a W or $t\bar{t}$ can also be useful. The cross section is substantially reduced, but the presence of additional particles provides a proportionally larger reduction in the background. Events are required to have an isolated lepton arising from the decay of the W (or top quark). This lepton can be used to determine the vertex position. Finally, the dominant decay of a Higgs boson, if its mass is below $2m_W$, is to be $b\bar{b}$.

b) Intermediate Higgs mass (130 GeV/ $\leq m_H \leq 2m_Z$): in this mass range the useful channels appear to be $H \rightarrow ZZ^* \rightarrow 4l$ and $H \rightarrow WW^{(*)} \rightarrow ll\nu\nu$ ($l = e,\mu$). The latter becomes more important around the WW production threshold, where the ZZ^* mode is suppressed. Below $2m_Z$, the event rate is small and the background reduction more difficult, as one or both Z–bosons are off shell. For $m_H < 2m_Z$ the main background arises from $t\bar{t}$, $Zb\bar{b}$ and ZZ^*/γ^* production. The $t\bar{t}$ background can be reduced by lepton isolation and by lepton–pair invariant mass cuts. The $Zb\bar{b}$ background can be suppressed by isolation requirements. The ZZ^* process is an irreducible background.

c) High Higgs mass ($m_H > 2m_Z$): the most useful decay mode is H $\rightarrow$ ZZ. For high masses the natural Higgs width becomes large. The main background is continuum ZZ production. As the Higgs mass increases, its width further increases and its production rate falls, so that one must turn to decay channels with a larger branching fraction.

2) Top–quark physics

Statistics severely limits the current top-quark studies at the Tevatron (Fermilab, USA). This means that the mass of the top quark cannot be determined very accurately. At the LHC, thousands of top quarks are produced per day. The mass of the top quark can be measured to an accuracy of about 3%, limited by theoretical uncertainties rather than statistics. Also the decay channels can be studied in detail.
The LHC will be a top factory, with about 10^7 $t\bar{t}$ pairs produced per year at a luminosity of 10^{33} cm^{-2} s^{-1}. The $t\bar{t}$ pairs can be produced, for example, according to the diagrams of Fig. 5. This would result in about 200,000 reconstructed $t\bar{t} \rightarrow (l\nu b)(jjb)$ events and 20,000 clean $e\mu$ events. The top mass may be reconstructed from the $(l\nu b)(jjb)$ final state using the invariant mass of the 3-jet system. The large statistics available at the LHC will provide sensitivity to non-standard or rare top decays.

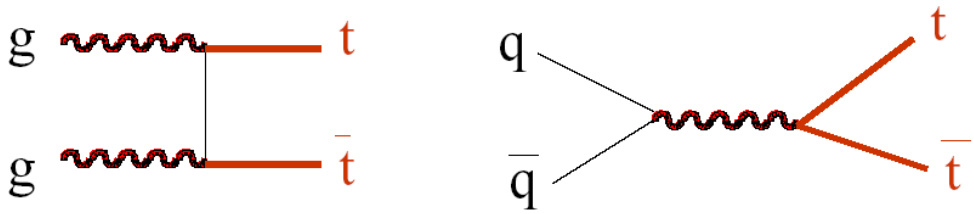


Figure 5 Two of the Feyman diagrams for the production of $t\bar{t}$ pairs

3) B physics

The huge $b\bar{b}$ production at the LHC offers the possibility to explore a wide range of b-physics channels. The main difficulty is represented by the fact that the leptons from *b* decays are quite soft and so suffer from the huge background of pion, kaon and charm (semi) leptonic decays. Muons appear to be much more useful than electrons, since for the same energy thresholds they are more easily identifiable. The large number of pile-up events at highest luminosity will render b-event reconstruction a very hard task. For this reason it is foreseen that the most suitable LHC phase for b physics will be the early one, when the luminosity will be about 10^{32}–10^{33} cm^{-2} s^{-1} (low-luminosity phase of the LHC).

4) **Supersymmetric particles**

If supersymmetry (SUSY) exists at the electroweak scale, its discovery at the LHC should be straightforward. The SUSY cross section is dominated by gluinos and squarks, which decay through a series of steps into the lightest supersymmetric particle (LSP). These decay chains lead to a variety of signatures involving multiple jets, leptons, photons, heavy flavours, W and Z bosons, and missing energy.
The combination of a large production cross section and distinctive signatures make it easy to separate SUSY from the SM background.

5) **Physics beyond the SM**

The ATLAS and CMS experiments will also be sensitive to a variety of other possible extensions of the SM. Some of the new phenomena are the following:

- New vector bosons W and Z can be searched for the LHC for masses up to 5–6 TeV;
- The discovery potential for first-generation leptoquarks extends up to ~ 1.5 TeV;
- Excited quarks should be detected up to masses of the order of 5–6 TeV.

1.3 The Compact Muon Solenoid detector at the LHC

1.3.1 Introduction

The concept of a compact detector for the LHC, based on a solenoid, the Compact Muon Solenoid detector, was presented in October 1990 at the LHC Workshop in Aachen [4]. For a high-luminosity proton–proton machine, it is natural that the muon detection system be optimized first. All types of magnetic configurations were studied and the requirement for a compact design led to the choice of a strong magnetic field; the only practical magnet that can generate such a very strong magnetic field is a solenoid.
The CMS detector has been designed to distinguish cleanly the diverse signatures from new physics by identifying and precisely measuring muons, electrons and photons over a large energy range and at high luminosity.
The ability to trigger on and reconstruct muons at the highest luminosities is central to the concept of CMS, which is characterized by a simplicity of design, with one magnet whose solenoidal field facilitates precision tracking in the central-barrel region and triggering on muons through their bending in the transverse plane.

1.3.2 General detector-design considerations

The CMS detector (shown in Fig. 6) has a diameter of about 14 m, a length of 20 m and a weight of 12,000 tons [5], [6]. The magnet inside the detector will have a 4-Tesla field in a solenoidal volume of 6 m diameter and about 12 m length. The detector has four major subsystems:

1. The tracking subsystem, which includes a silicon vertex detector;
2. The electromagnetic calorimeter (ECAL), made of lead tungstate crystals;
3. The hadron calorimeter (HCAL), made of brass and scintillator;
4. The muon subsystem.

In addition, the detector has to have a data acquisition system, a trigger system, and on-line and off-line computing.
Before describing the various detector elements, some useful and important remarks should be noted.
The pseudorapidity η is a measure of angle and is defined by $\eta = \ln(\tan(\theta/2))$, where θ is the angle between the outgoing particle and the undeflected beam. The term 'barrel', 'endcap' and 'forward' are used to describe angular ranges and parts of detectors. A barrel detector sits in the centre of the experiment and typically covers an angular range of $-45° < \theta < 45°$. An endcap detector would cover the approximate angular range of $15° < \theta < 45°$ (if it were located on the positive side). Forward is used to describe detectors for particles within 15° of the beam axis.
In the barrel, the choice of a drift chamber as tracking detector was dictated by the low expected rate and by the relatively low intensity of the local magnetic field.
A cathode strip chamber, instead, has been chosen for the endcaps, since it is capable of providing precise space and time information in the presence of a high magnetic field and a high particle rate.
Finally, resistive-plate chambers (located both in the barrel and in the endcaps) have a very short-time response and, consequently, they can provide an unambiguous assignment of the bunch-crossing.

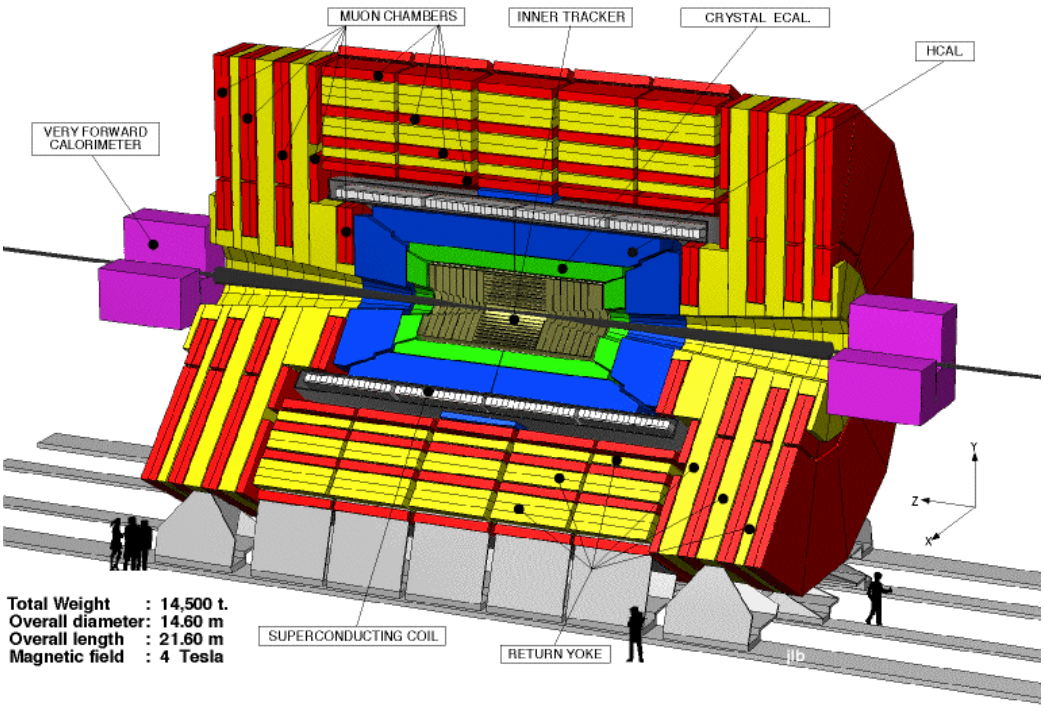


Figure 6 The Compact Muon Solenoid (CMS) detector

1.3.3 The CMS tracking system

Robust tracking and detailed vertex reconstruction are expected to play an essential role in an experiment designed to address the full range of physics, which can plausibly be accessed at the LHC.

The inner tracking detectors [7] are designed to reconstruct high-p_T muons, electrons, and hadrons, with high momentum resolution and high efficiency in the range of $|\eta| < 2.5$. They are also designed to allow the identification of tracks coming from detached vertices. High redundancy and low occupancy are needed to achieve these goals, leading to a highly granular design, with layers of silicon pixels close to the beam pipe, where the density of tracks is large, and layers of silicon strips further away from the beam pipe. The inner tracker extends up to a radius of 115 cm over a length of approximately 270 cm on each of the interaction points.

1) The pixel detector is shown in Fig. 7; it consists of two-barrel layers and two disks on each side of the barrel. Its main purpose is to measure the impact parameter of charged tracks in order to achieve efficient tagging of jets originating from the decay of heavy hadrons containing *b* and *c* quarks, and for top-quark studies.

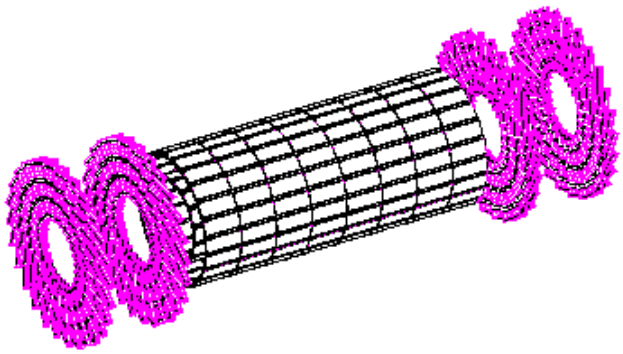


Figure 7 Perspective view of the pixel system in the high-luminosity configuration

The detector will consist of *n*-type pixels on an *n*-type substrate: the pixels will be of squared shape (150 μm × 150 μm) with a width of 250 μm. By interpolation between the signals deposited in several adjacent pixels, a spatial resolution of $\sigma(x) \sim 15$ μm can be achieved. In the barrel, three layers of silicon pixels can be placed at distances of 4.3 cm, 7.2 cm and 11.0 cm from the beam line. At the very beginning of the data taking (when the LHC will run at low luminosity), the silicon pixel detector will be equipped with two inner layers; at high luminosity only two outer layers will be installed. In the endcaps, two disks at positions $z = \pm 325$ mm and $z = \pm 465$ mm will cover a radial range of $r = 6$ cm up to $r = 15$ cm. In the endcaps, where tracks are normal to the pixel surface, and electric and magnetic fields are parallel, the detector blades are tilted by 20º.

2) The silicon strip detector (SSD) [8] **(**shown in Fig. 8) consists of an inner part, organized in four-barrel layers (Tracker Inner Barrel, TIB), at each side of which there are three minidisks (Tracker Inner Disks, TIDs), an outer part composed of six-barrel layers (Tracker Outer Barrel, TOB) surrounding the TIB, and an endcap region with nine disks in each endcap (Tracker Endcap, TEC).
Its design is based on the microstrip technology: *p*+ strips are implanted on *n*-type bulk sensors with a < 100 > crystal lattice orientation.
The whole silicon strip detector (SSD) has a total active surface of 170 m^2, instrumented with about 11×10^6 channels. Signals are read out by a charge-sensitive amplifier, whose output voltage is sampled at a beam crossing rate of 40 MHz. The samples are stored in an analogue pipeline. An analogue circuit enables the measurements of the signal amplitude according to the trigger. Pulse-height data are transmitted to the control room through a ~ 100 m long optical cable after having been converted by a laser device. The electrical pulses are converted back to electric signals and digitized in a 10-bit ADC. The final processed data are stored in a local memory until required for the higher-level trigger processing.

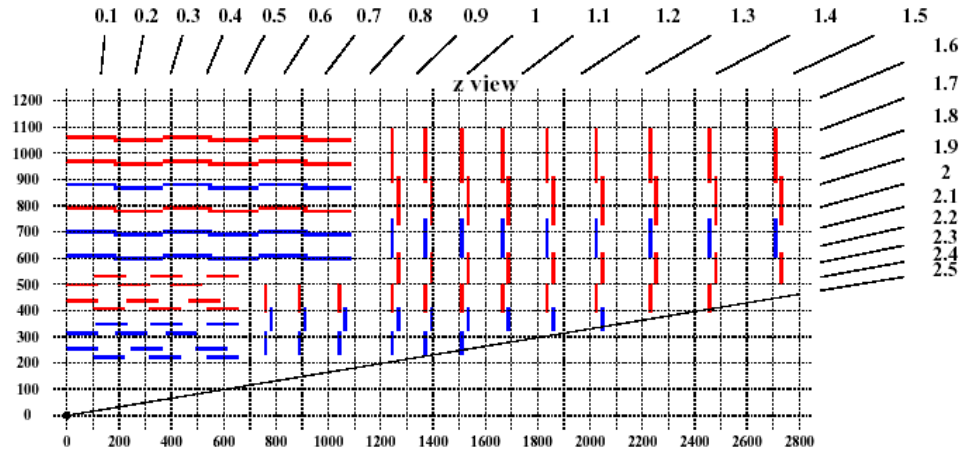


Figure 8 Longitudinal view of the silicon strip detector (one quarter)

1.3.4 The calorimeters

Calorimeters play a central role in 'general-purpose detectors' for high-energy proton–proton colliders such as ATLAS and CMS at the LHC: they allow us to trigger, measure, and identify electrons, photons and jets, and to detect the missing energy, i.e. to tag and, to a certain extent, to measure escaping neutrinos or other non-interacting particles. They also complement muon detection (energy loss, trigger).

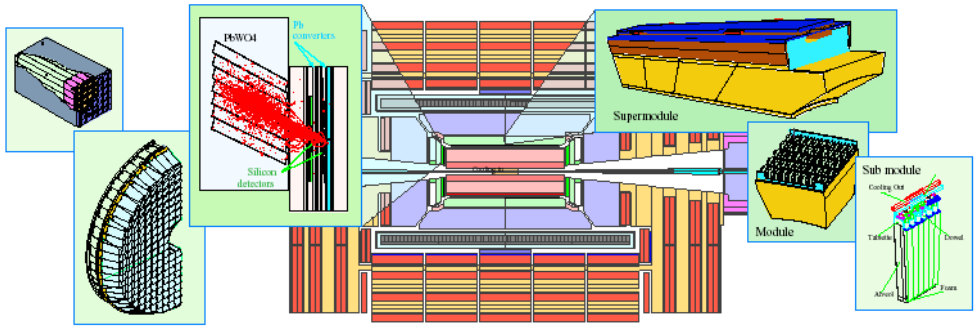


Figure 9 The electromagnetic calorimeter

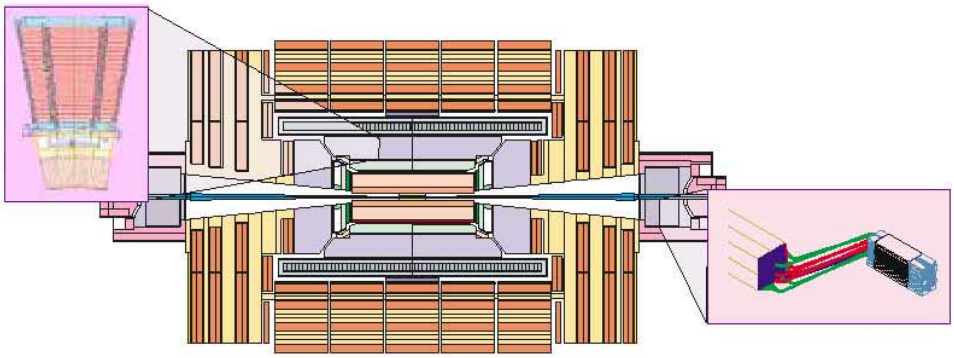


Figure 10 The hadronic calorimeter

Electrons, photons and hadrons will be stopped by the calorimeters, allowing their energy to be measured. The first layer is designed to measure the energies of electrons and photons with high precision. Since these particles interact electromagnetically, it is called the electromagnetic calorimeter (ECAL) (see Fig. 9). Particles that interact through the strong interaction, hadrons, deposit most of their energy in the next layer, the hadronic calorimeter (Fig. 10). The calorimeters for CMS have two distinct structures. The electromagnetic compartment [9] consists of a single crystal of $PbWO_4$, which is read out by an avalanche photodiode (APD). The hadronic compartment [10] is a sampling calorimeter where the absorber is brass, while the active sampling is done by means of scintillators. The scintillator light is wavelength-shifted and read out by hybrid photodiodes (HPD).

1.3.5 The muon system

The CMS muon system illustrated in Fig. 11 consists of five wheels surrounding the magnet and two endcaps. The four-barrel muon stations and the four-endcap muon stations are integrated in the iron return yoke of the magnet. The system will provide coverage over the pseudorapidity from 0 to 2.4.

The muon system [11] has three main purposes: muon identification, muon trigger, and muon (signed) momentum measurement. It is composed of four muon stations interleaved with the flux return iron yoke plates and is divided in a barrel part ($|\eta| < 1.2$), and two endcap parts ($0.9 < |\eta| < 2.4$).

The CMS muon system uses three different technologies to detect and to measure the muons: drift tubes (DTs) in the barrel region, cathode strip chambers (CSCs) in the

endcap region, and resistive-plate chambers (RPCs) both in the barrel and in the endcap regions.

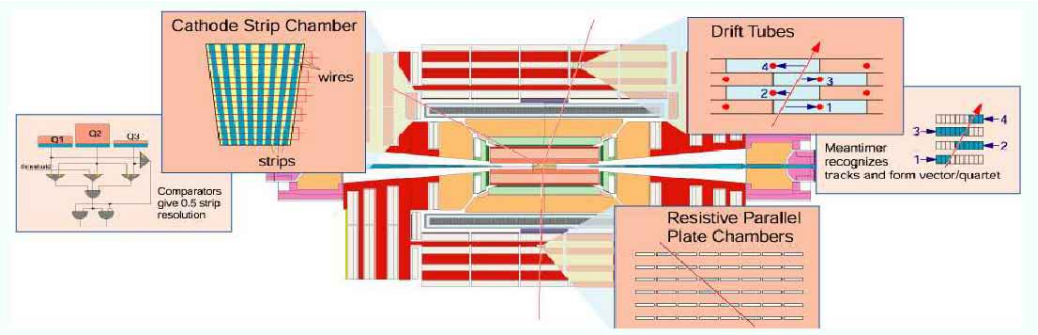


Figure 11 The CMS muon system

1) The drift tubes used in the CMS experiment are drift chambers of 4×1.1 cm^2 and a maximum drift distance of 2 cm, filled with an Ar–CO_2 mixture. They consist of aluminium cathodes 1.2 mm thick and 9.6 mm long, and stainless steel anode wires of 50–μm diameter strung at the centre of the tubes. Their functioning is shown in Fig. 12. Their use is foreseen in the barrel part only, where the expected particle rate is lower than 10 Hz/cm^2, allowing a response time of the order of 400 ns with cell occupancy below 1 %. Each barrel muon chamber is composed of twelve layers of drift tubes grouped into three superlayers of four layers each, the first and the third measuring the φ coordinate of the muon crossing point, whereas the second measures the z-coordinate. The distance of the two outer superlayers is maximized to 23 cm in order to achieve the best angular resolution: since the spatial resolution of each layer is better than 250 μm, the resulting resolution in the muon direction measurement in the transverse plane is about 1 mrad. The first three-barrel muon stations contain 60 such chambers, while 70 are put into the outermost station.

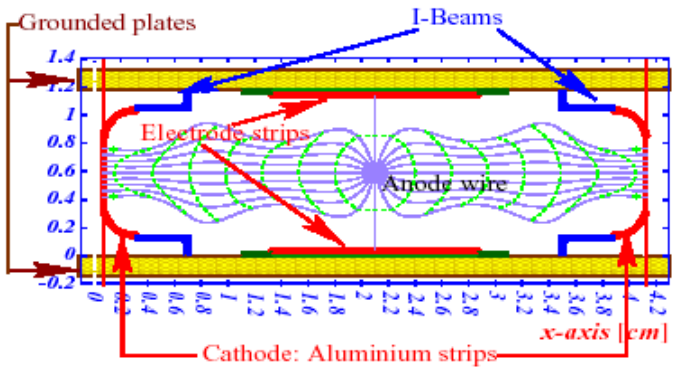


Figure 12 Current cell designs showing the geometry of several components and isochronous lines

2) The cathode strip chambers [11] are used in the endcap regions where the magnetic field is very intense (up to several Tesla) and very inhomogeneous.

A CSC is a multiwire proportional chamber in which the cathode is subdivided into strips (see Fig. 13). Gold-plated anode wires, parallel to the cathode plane and perpendicular to the strips, are strung in the middle of each tube. An avalanche developed near a wire induces a distributed charge on the cathode strips. The track position can be reconstructed with the centre-of-mass method of interpolating the fractions of charge picked up by the strips. These counters are well suited to the conditions met in the endcap part of the muon system, i.e. rates up to 1 kHz/cm^2 and a high magnetic field. The chambers, trapezoidal and filled with an Ar–CO_2–CF_4 mixture, have the cathode strips displaced radially in order to get information on the φ coordinate. The signals collected by the wires are read out to measure the radial coordinate and to provide bunch-crossing identification. The CSCs are grouped into modules of six layers each: the modules are arranged in series of concentric rings around the beam line. The innermost station is built of three rings, while the others are built of two rings, overlapping in φ to avoid dead areas in the azimuthal angle. The precision is 75 μm in the two inner rings of the innermost station, and 150 μm everywhere else.

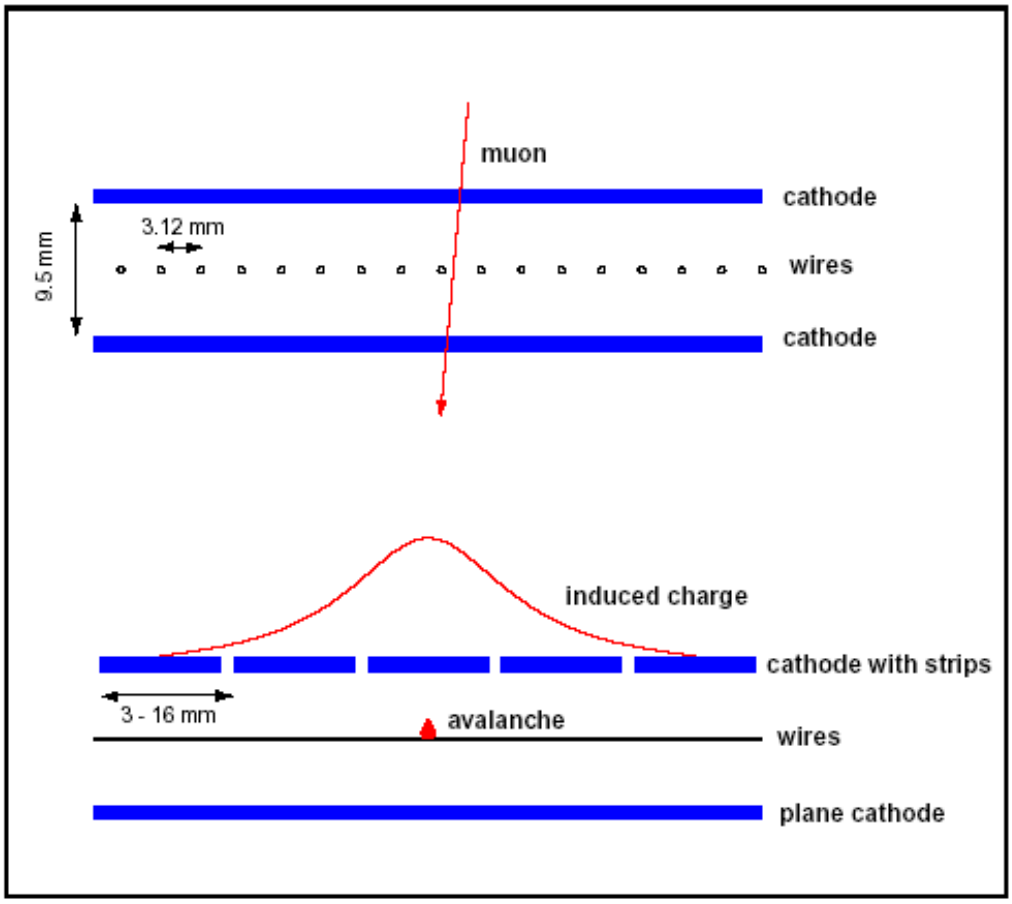


Figure 13 Principle of coordinate measurement with a cathode strip chamber

2 The CMS muon trigger

2.1 Introduction

In general, the purpose of the trigger system of an experiment is the selection of all interesting events from an overwhelming background [12].
For the nominal LHC design luminosity of $10^{34}\,cm^{-2}s^{-1}$, an average of 17 events occur at the beam-crossing frequency of 25 ns. This input rate of 10^9 interactions every second must be reduced, by a factor of at least 10^7, to 100 Hz, the maximum rate that can be archived by the on-line computer farm.
In the CMS experiment the rate will be reduced in two steps. The first step of reduction is performed by the L1 Trigger [13], a large system of fully pipelined custom-built electronics, which processes data from every bunch-crossing without dead time. Based on coarsely segmented data from the calorimeters and muon systems, the L1 Trigger reduces the rate below 100 kHz, while the full high-precision data are kept in front-end pipelines. Triggered events are passed to the readout buffers in order to be analysed by the high-level trigger [14] algorithms running on a farm of commercial processors.

2.2 General structure of the CMS trigger and DAQ

The CMS trigger and data acquisition system (TriDAS) is designed to inspect the detector information at the full crossing frequency and to select events at a maximum rate of $O(10^2\,Hz)$ for archiving and later off-line analysis. The CMS DAQ has to read out all front-end electronics, to assemble the data from each bunch-crossing into a single stand-alone data structure, to provide these data to the processing elements that execute the high-level trigger (HLT) selection and forward the events accepted by the processor farm to the on-line computing services, which contain, among others, the mass storage.
The DAQ system provides the first place where the entire information from the physics collision can be inspected. It is also the place where the complete picture of the detector response to the collisions can be monitored, thus providing early feedback to physicists running the experiment.
The DAQ is therefore the system that implements the two crucial functions that eventually determine the reach of the physics program: event selection, and control and monitoring of the detector elements. The architecture of the CMS DAQ is shown in Fig. 14.

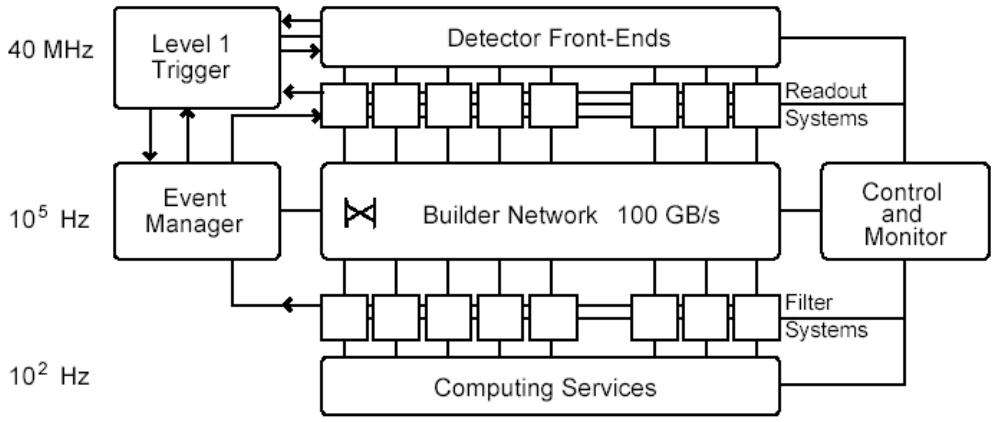


Figure 14 Architecture of the CMS DAQ system

It consists of the following elements [14]:

1. **Detector front-ends**: the modules that store the data from the detector front-end electronics upon the reception of a Level-1 Trigger Accept signal. The front-ends are the responsibility of the corresponding subdetectors;
2. **Readout systems**: the modules that read the data from the detector front-end system. The data are stored, until they are sent to the processor, which will analyse the event;
3. **Builder network**: the collection of networks that provides the interconnections between the readout and the filter systems;
4. **Filter systems**: the processors, which are provided by the readout. They execute the HLT algorithms to select the events to be kept for off-line processing;
5. **Event manager**: the entity responsible for controlling the flow of data (events) in the DAQ systems;
6. **Computing services**: all the processors and networks that receive filtered events as well as a small fraction of rejected events from the filter farms;
7. **Controls**: all the entities responsible for the user interface and the configuration and monitoring of the DAQ.

2.3 The first-level (L1) trigger

2.3.1 Introduction

The CMS L1 trigger is implemented on custom programmable hardware. It runs dead-time-free and has to take an Accept/Reject decision for each bunch-crossing, i.e. every 25 ns.

The L1 trigger is divided into three subsystems: the calorimeters trigger, the muon system and the global trigger, analysed in detail in the next chapters.
The muon trigger is further subdivided into three independent systems:

- Four stations of drift tubes (DTs) chambers with bunch-crossing identifying capabilities provide precision-tracking measurements throughout the barrel region, each station consisting of twelve staggered layers of drift tubes;
- Four disks of cathode strip chambers (CSCs) cover the two endcaps, each disk consisting of six layers of chambers;
- Six layers of double-gap resistive-plate chambers (RPCs) mounted on the DT stations and four layers mounted on the CSC stations provide additional complementary information with superior timing resolution.

A schematic view of the components of the L1 trigger is shown in Fig. 15.

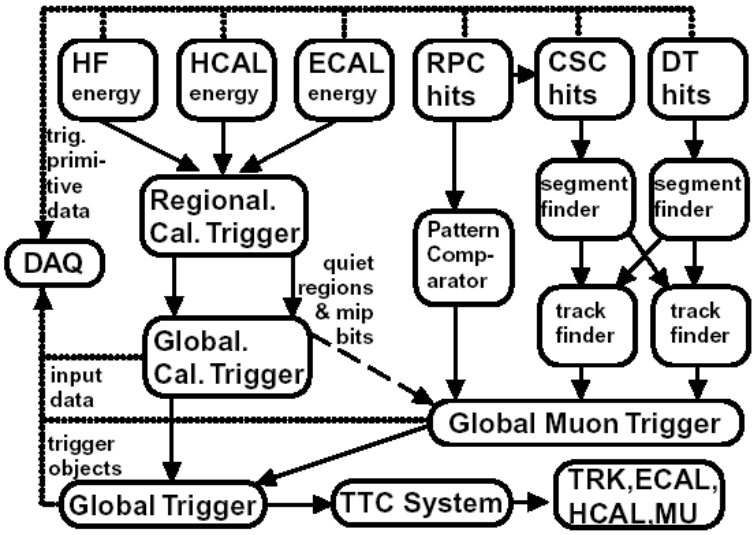


Figure 15 Overview of the level-1 trigger

The calorimeter and muon triggers do not perform any selection themselves. They identify 'trigger objects' of different types: isolated and non-isolated electrons/photons, forward, central and τ–jets and muons with an isolation flag.
The four best candidates of each type are selected and sent to the global trigger (GT), together with the measurement of their position, direction, and transverse energy. The GT also receives the total and missing transverse-energy measurement and count the number of jets above programmable thresholds from the calorimeter trigger. The GT selects events according to programmable trigger conditions, which can include requirements of the presence of several different objects with energies or momenta above predefined thresholds.

2.3.2 Calorimeter trigger

The L1 calorimeter trigger system [13], which is detailed in Fig. 16, detects electrons/photons and jets as well as the total and missing transverse energy by using coarsely segmented data from the calorimeters.
Additionally, it provides two bits of information to the L1 muon trigger for each calorimeter region, a minimum-ionizing-particle (MIP) bit denoting an energy deposit compatible with the passage of a minimum-ionizing particle such as a muon through the region, and a 'quiet' bit denoting whether a certain minimum energy was deposited in the region. No distinction can be made between electrons and photons since there is no tracker available at L1.

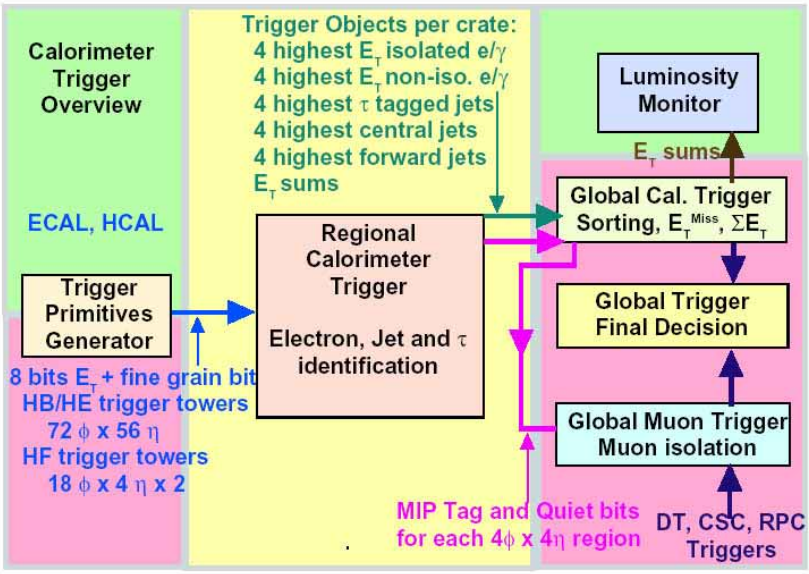


Figure 16 Overview of the calorimeter trigger system

The L1 calorimeter trigger system consists of regional and global processors. The regional system processes the electromagnetic and hadronic trigger tower sums from the calorimeter front-end electronics; it delivers regional information on electrons, photons, jets and partial energy sums to the global calorimeter L1 trigger system. The regional system begins after the data from the front-end electronics have been received on optical fibres and translated to signals on copper ends with cables that transmit the results to the calorimeter global L1 trigger system.
More specifically, the calorimeter trigger is based on trigger towers of size 0.087×0.087 in the $\eta-\varphi$ space in the central region, and somewhat larger for $|\eta| > 2$. This size represents a single readout tower in the hadron calorimeter (HCAL), and 5×5 crystals in the electromagnetic calorimeter (ECAL) barrel. The tower energy sums are formed by the ECAL, HCAL and forward hadronic calorimeter (HF) trigger primitive generator circuits, from the individual calorimeter cell energies. For the ECAL, these energies are

accompanied by a bit indicating the transverse extent of the electromagnetic energy deposit. For the HCAL, the energies are accompanied by a bit indicating the presence of minimum-ionizing energy. The top four candidates from each class of calorimeter trigger are sent to the global trigger.

2.3.3 Muon trigger

The CMS detector is a general-purpose detector specifically optimized for muon measurements; this is performed by DTs located outside of the magnet coil in the barrel region and by the CSCs in the forward region. The CMS muon system is also equipped with RPCs dedicated to triggering. The basic tasks of the CMS muon trigger are muon identification, transverse-momentum measurement and bunch-crossing identification. It is represented schematically in Fig. 17.

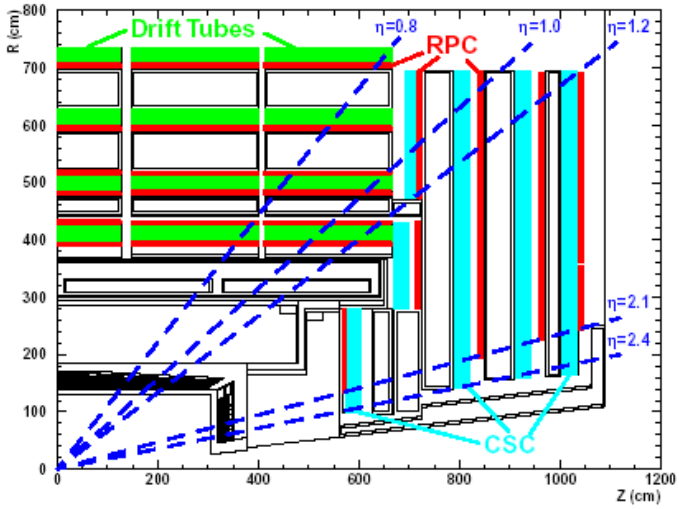


Figure 17 Longitudinal cut of the CMS muon system

The L1 muon trigger [13] uses all three kinds of muon detectors (as shown in the previous picture): drift tubes, cathode strip chambers and resistive plate chambers. The excellent spatial precision of DTs and CSCs ensures sharp momentum threshold. Their multilayer structure provides a possibility of effective background rejection. RPCs are dedicated trigger detectors. Their superior time resolution ensures unambiguous bunch-crossing identification.
The muon trigger system consists of the following items:

- Drift-tube trigger
- Cathode-strip-chambers trigger
- Pattern comparator trigger (PACT) based on resistive-plate chambers
- Global muon trigger

Each of the L1 muon systems has its trigger logic. The RPC strips are connected to a PACT, which is projective in η and φ. The barrel muon DTs are equipped with bunch and track identifier (BTI) electronics that find track segments from coincidences of aligned hits in four layers of one DT superlayer.

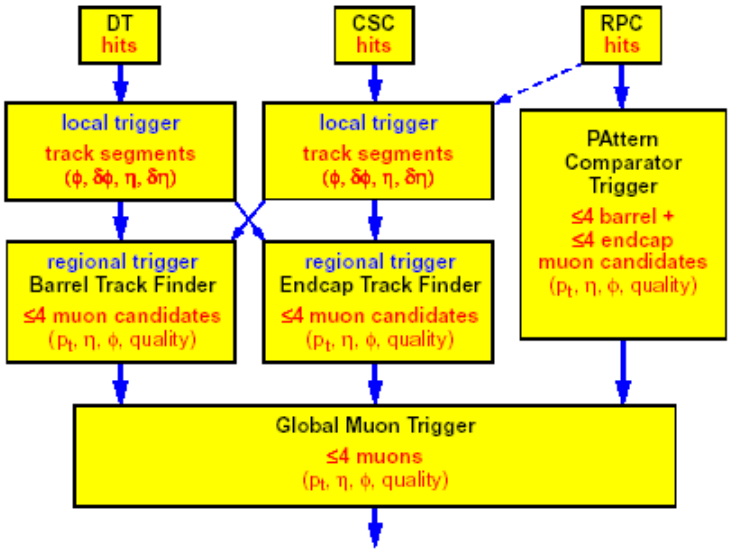


Figure 18 Muon trigger data flow

As shown in Fig. 18, DT and CSC electronics first process the information from each chamber locally. They are therefore called local triggers. As a result, one vector (position and angle) per muon station is delivered. Vectors from different stations are collected by the track finder (TF), which combines them to form a muon track and assigns to these a transverse-momentum value. Up to 4 best (highest- p_T and quality) muon candidates from each system are selected and sent to the global muon trigger (GMT).

In the case of RPCs there is no local processing apart from synchronization and cluster reduction. Hits from all stations are collected by the so-called PACT logic. If they are aligned along a possible muon track, a p_T value is assigned and the information is sent to the muon sorter. The RPC muon sorter selects the four highest- p_T muons from the barrel and four from the endcaps and sends them to the GMT. The GMT compares the information from the DT/CSC track finder and RPC PACT. So-called quit and MIP bits delivered by the calorimeter trigger are used to form a possible isolated muon trigger.

The four highest- p_T muons in the whole event are then transmitted to the global trigger. Finally, transverse-momentum thresholds are applied by the global trigger for all trigger conditions.

2.3.4 Specific requirements for the first level muon trigger

The task of the muon trigger is difficult because of the presence of severe background. There are three main sources of background: proton-proton interactions themselves, beam losses because of limited LHC aperture and cosmic rays [11]. These sources produce various effects in the detectors, such as track (a set of aligned segments from several muon stations), track segment (a set of aligned hits within one muon station), correlated hit (caused by a genuine muon or its secondary) and uncorrelated hit (caused by phenomenon not related to a given muon).
Genuine muon rates from various sources are given in the Figure 19 and Figure 20:

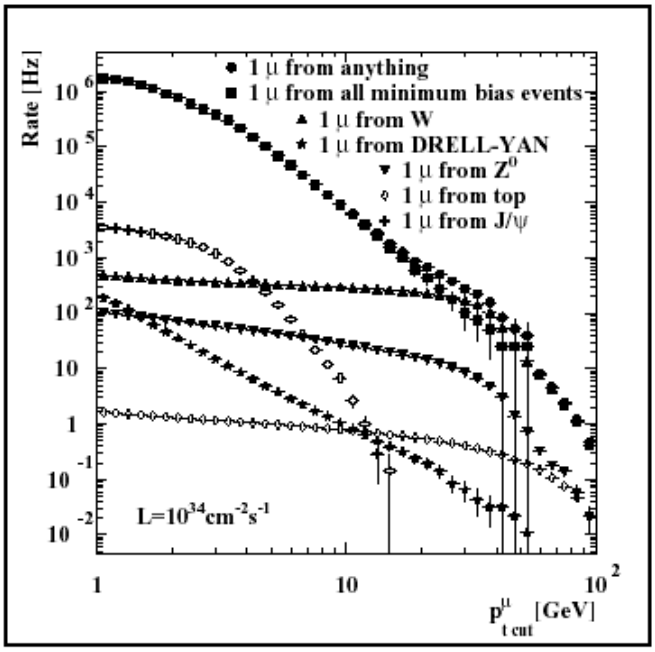


Figure 19 Single muon rates (|η| < 2.4)

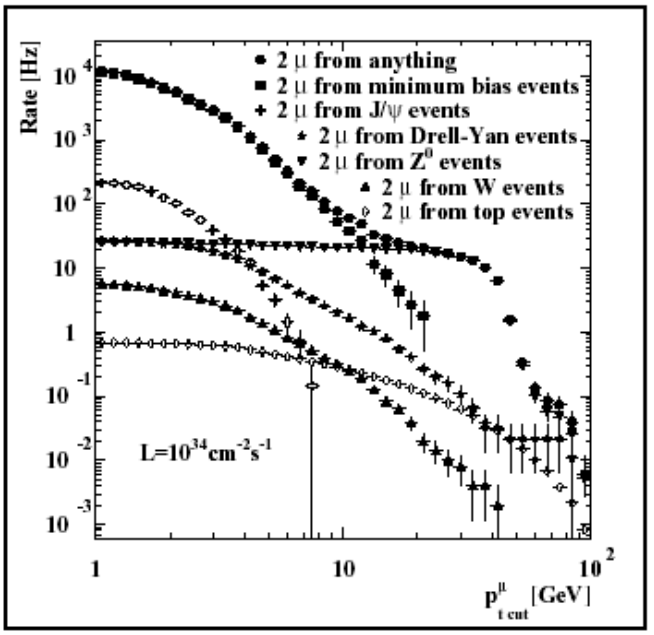


Figure 20 Double muon rates (|η| < 2.4)

Specific requirements for the first level muon trigger are the following:
1) Geometrical coverage: up to |η| = 2.4**,** in order to cover the entire area of the muon system.
2) Latency: < 3.2 μs. Total trigger processing should stay within the length of the tracker pipelines, i.e., 128 bunch crossings. This implies that the trigger algorithms cannot be too complicated.
3) Trigger dead time: not allowed. Every bunch crossing has to be processed in order to maintain the high efficiency crucial for many physics channels with low cross section.
4) Maximal output rate: < 15 kHz for luminosities < 10^{34} cm^{-2} s^{-1}. Maximal second level input rate is 100 kHz. Uncertainties in estimates of cross sections and luminosity variations during a single run requires a large safety margin. By design, the average first level output rate should not exceed 30 kHz, shared between muon and calorimeter triggers. About 5-10 kHz is assigned for the single muon trigger. This implies a rejection factor of ~10^{-5} at the highest luminosity.
5) Low p_t reach: should be limited only by muon energy loss in the calorimeters. It is equal to about 4 GeV in the barrel and it decreases with |η| down to ~2.5 GeV. This is required mainly for b-quark physics at L = 10^{33} cm^{-2} s^{-1}.
6) The highest possible p_T cut: ~50-100 GeV. The expected threshold needed to restrict the single muon trigger rate to 5-10 kHz at L = 1034 cm^{-2} s^{-1} is 15–20 GeV. Uncertainties in estimates of cross sections and background levels requires a large safety margin. Increasing the threshold from 15-20 GeV to 50-100 GeV reduces the rate by an order of magnitude.
7) Background rejection: single muon trigger rate due to background should not exceed the rate of prompt muons from heavy quark decays at the nominal threshold (15-20

GeV). This is necessary to maintain the rejection factor stated above. The prompt muon rate is irreducible except for channels where the isolation criterion can be applied.
8) Isolation: transverse energy E_T deposited in each calorimeter region of $D\eta \times D\varphi = 0.35 \times 0.35$ around a muon is compared with a threshold.
This function is needed to suppress the rate of background and prompt muons from heavy quark decays when triggering on muons not accompanied by jets.
9) Output to the Global Trigger: up to 4 highest p_T muons in each event. In principle, only 3 muons are necessary for the Global Trigger to perform single- and multiobject cuts including the three-muon trigger. By delivering 4 muons we reduce the probability that a low p_T isolated muon will not be selected because of the presence of higher pt non-isolated muons. This way we also reduce the probability of accepting ghosts instead of real muons.

2.3.5 Global trigger

The ultimate task of the L1 GT is therefore to decide whether to accept or reject an event and to generate the corresponding L1 Accept signal (L1A) [15].

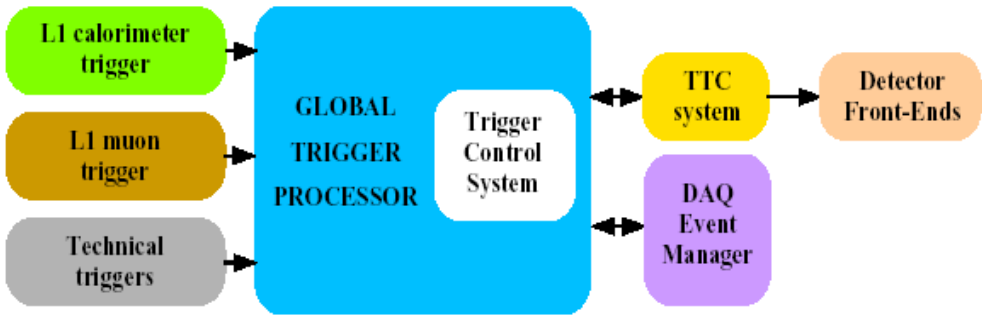


Figure 21 Global trigger environment

The GT environment is shown in Fig. 21. The GT processor is a custom-built electronics system. The timing, trigger and control (TTC) optical network sends the L1A signal to all readout units of the subsystems to move data of the current bunch-crossing from their pipeline or ring buffers into derandomizing memories. Later, all or part of the bx-data will be fetched by the data acquisition, first to run higher-level trigger algorithms and finally to store the accepted events.
In the specific case of the muon trigger system, the task of the GMT is to combine the results of all subsystems by finding the best four muons in every bunch-crossing and to transmit them to the GT.

2.4 Trigger control

2.4.1 Requirements

The trigger control system (TCS) is presented in Fig. 22. It is logically located between the L1 GT and the CMS readout and data acquisition system [16].
The main task of the TCS is to control the delivery of L1As generated by the GT, depending on the status of the readout electronics and the data acquisition. This status is derived from local state machines that emulate the front-end buffers occupation, as well as from direct information transmitted back by the CMS subsystems through the trigger throttling system (TTS). The TCS is also responsible for generating synchronization and fast Reset commands, as well as for controlling the delivery of test and calibration triggers. The TCS uses the TTC network to distribute information to the subsystems.

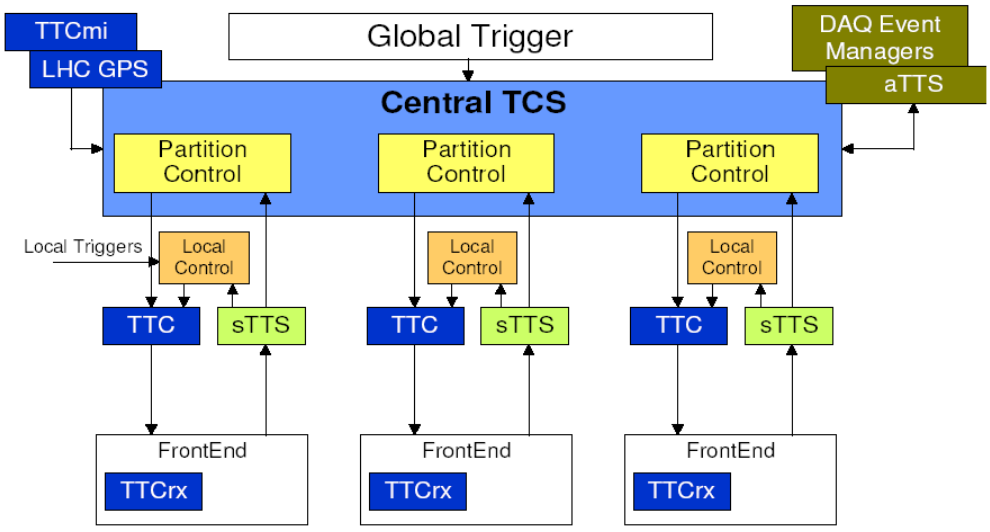


Figure 22 Overview of the trigger control system

The TCS is organized in partitions, each corresponding to a major component of a subdetector, to which it distributes L1A and other TTC commands and from which it collects TTS signals.
The software configuration allows us to consider both partitions and partition groups, each one of these matching a DAQ partition. Partitioning requires that the TTC and TTS trees be organized in branches (partitions), with master units at the top allowing independent operation of the partition groups.

2.4.2 Architecture

The main TCS components are shown in Fig. 23. They are:

1) The central trigger controller, which is physically located in the GT rack. It consists of the central trigger controller module in the GT main 9U VME crate, the sTTS receiver modules and the front-end pipeline-derandomizer emulator modules. Synchronous trigger throttling system (sTTS) receivers and emulator modules are housed in 6U VME crates. The functions of the central TCS are the following: to control the delivery of the L1A, based on the verification of trigger rules, on the emulation of the front-end buffers and on the sTTS status, to generate the fast commands to be distributed to the subdetectors by the TTC network, to collect the sTTS fast monitoring feedback from the subsystems, and to generate the appropriate action when necessary, to generate calibration and test trigger sequences and, finally, to monitor the experiment dead time.

2) The local trigger controller (LTC), which is physically located in the subdetector trigger control crate (6U VME), which contains also the TTCci (TTC-CMS interface) and trigger encoder and transmitter (TTCex) modules. The LTC allows the control of the partitions of a subdetector, replacing the central TCS in its functionality. The LTC controls up to six TTC partitions, but it is not required to run multiple-partition groups in parallel. One single partition group or DAQ partition can run at a given time.

3) TTCci module: The TTCci is the CMS version of the TTCvi module. The TTCci is the top element of each of the 32 TTC partitions. It provides the interface between the (central or local) TC and the TTC destinations for transmission of L1A and fast commands. Switching between central and local trigger control is achieved by software programming. For test purposes, the TTCci can operate in stand-alone mode.

4) Fast merging module: The FMM is the building block that allows the construction of the sTTS tree. Its purpose is to perform logical operations on 32 groups of the 4 TTS binary signals. The result of the functions is available on 2 outputs (4 TTS lines each). The result of these operations can be summed in the next module. Finally, the result of the sum will constitute the input to the central and local TCs (one per partition).

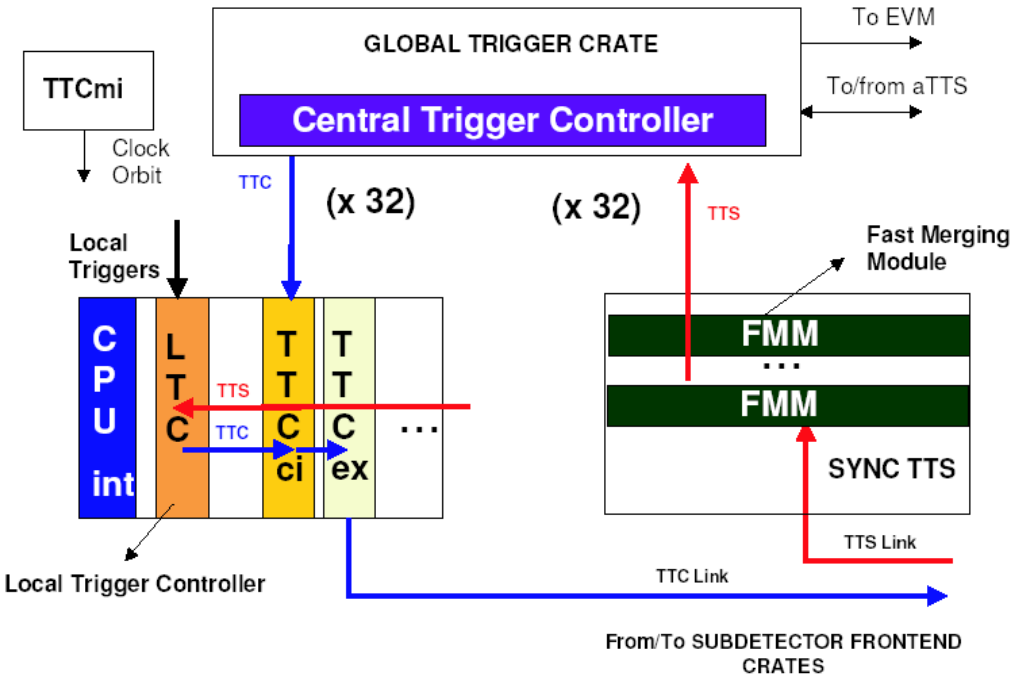


Figure 23 Trigger control architecture

2.4.3 Trigger control interfaces

The TCS has the following interfaces to external subsystems:

1. **Interface to the GT**, from which it receives the L1A information: after the GT processing, a decision is made to issue a L1 Accept or Reject for each bunch-crossing. The GT has the ability to define 128 programmable trigger conditions that are based on the trigger objects (electrons/photons, jets, muons, E_T sums) computed by the trigger system subcomponents. The TCS receives from the GT the results of the eight final L1As to be distributed to the various partitions.

2. **Interface to LHC machine Clock and Orbit signals** and beam pickup interface: The LHC Clock and Orbit signals are distributed from the Prevessin Control Room to the LHC experiments through single-mode optical fibres. In the experiment Counting Room, the Clock and Orbit signals are recovered by circuitry (LHCrx module) in the TTC machine interface (TTCmi) crate. Fanout modules (TTCcf) in the TTCmi crate are used to distribute the Clock and Orbit

signals to nearby crates housing the TCS and the subdetectors TTCvi/TTCex modules (top elements of each subdetector partition TTC network).

3. **Interface to the TTC network**, to distribute L1A and fast commands to the subdetector partitions: the TTC system provides for the distribution of timing, trigger and fast control signals using two time-multiplexed channels transmitted over an optical passive distribution network. The first channel is used to transmit the L1A signal whereas the second transmits other fast commands. Both channels have a bandwidth of 40 Mbits/s.

4. **Interface to the fast monitoring network,** to collect information on the status of the front-end electronics: the subdetector partitions send to the TCS information on their status. This status is characterized by digital signals such as Ready, Busy, Error, Warning Overflow, etc. The fast monitoring network will transport and combine the status signal of individual components that imply a reaction from TCS within the time scale of the L1A rate. The partitions status signals are updated at 40 MHz using hardware state machines to deduce the partition status from the state of their individual components. The fast monitoring signals are sent to the TCS in parallel LVDS.

5. **Interface to the DAQ event manager**, to transmit L1A and fast commands and to receive feedback status information: the interface to the DAQ event manager follows a similar model as the interface to the subdetector partitions. The TCS sends to the event manager all 128 algorithm bits and for each partition a 4-bit trigger type indicating the partitions that have received the L1A signal. For the physics trigger, the procedure is to read the data and send them to the higher-level trigger processors. Some physics triggers (e.g. low-threshold single electrons) are used for detector calibration and are sent to a special data stream. The event manager will be located in the surface Control Room, whereas the TCS will be placed in the underground Counting Room.

6. **Interface to run-control/detector-control system**: the next chapter will be entirely dedicated to the detector-control system interface.

3 The Detector Control System

3.1 Introduction

The main aim of the detector control system (DCS) is to ensure the correct operation of the CMS experiment, so that the data taken with the apparatus are of high quality. The scope of the DCS is therefore very wide and includes all subsystems and other individual elements involved in the control and monitoring of the detector, its active elements, the electronics on and off the detector, the complete set-up of the experiment as well as the communications with the accelerator. The DCS also plays a major role in the protection of the experiment from any adverse occurrences. Many of the functions provided by the DCS are needed at all times, and as a result some parts of the DCS must function continually, on a 24-hour basis, during the entire year [17].
The primary function of the DCS will be the overall control of the detector status and its environment. In addition the DCS has to communicate with external entities, in particular with the run control and monitoring system (RCMS), which is in charge of the overall control and monitoring of the data-taking process, and of the accelerator.

3.2 General system requirements

The major system-wide requirements on the CMS DCS are [14]:

1. Most importantly, reliability: this requires safe power, redundant and reliable hardware in numerous places;
2. The system must be modular and hierarchical;
3. It has to be partitionable in order to allow independent control of individual subdetectors or parts of them;
4. The system needs automation features so as to speed up the execution of commonly executed actions and also to avoid mistakes, mostly human, in such repetitive actions;
5. The system must be easy to operate: a few non-expert people should be able to control the routine operations of the experiment;
6. The system must be scalable: it must be possible to integrate new subdetectors or subdetector parts;
7. It must provide generic interfaces to other systems, e.g. the accelerator or the RCMS.
8. The system must be easy to maintain. This requirement strongly favours the use of commercial hardware and software components;
9. It must be homogeneous, which will greatly facilitate its integration, maintenance and possible upgrades, and have a uniform ‘look and feel’ throughout all of its parts;
10. The system has to provide a possibility for remote control via the Internet to allow non-CERN-resident detector groups to do maintenance and control from their home laboratory.

Beyond these general system-wide requirements, there are a few others resulting from the specific design and implementation of the various subdetectors. Then, the particular DCSs of individual subdetectors have to be connected to the central DCS supervisor hierarchy. For this reason they have to provide certain well defined interface functions.

3.3 Architecture

The DCS is organized in layers, as shown in Fig. 24. From the top, there are the surface Control Room and the underground Electronics Rooms, which are also accessible during operation, house workstations for operation and servers for functions such as database, communication with external systems, etc. [18]. CMS will use the commercial SCADA (Supervisory Control And Data Acquisition) system for the upper part of the DCS. The lower part, instead, will consist of the front-end I/O system, which is located in the experimental cavern and is not accessible during operation. This part reads out individual sensors and actuators, but also supervises devices such as power supplies or gas instrumentation as well as more complex equipment such as alignment systems. The interconnection between the two parts of the DCSs is done either via standardized protocols over a local area network, or by using fieldbus technology.

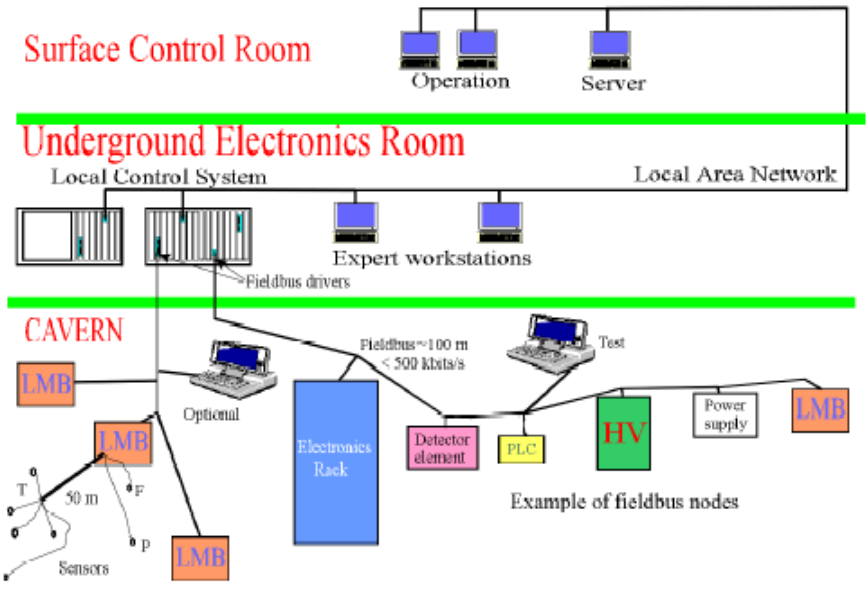


Figure 24 The DCS general architecture

3.4 Hardware and software components

3.4.1 SCADA

A typical control system for an experiment is organized in two main layers: the front-end layer and the supervision layer as shown in Fig. 25. The front-end layer is responsible for giving access to the equipment, while the supervision offers an interface to the different human users and high-level operations of the experiment. In the case of the CMS experiment, the supervision layer is based on a commercial tool, the supervisory control and data acquisition systems or SCADA [19],[20].

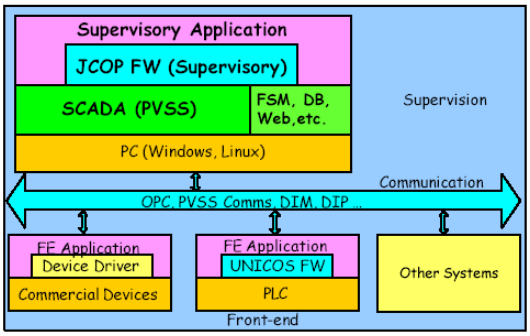


Figure 25 SCADA layers

SCADA is a commercial software used extensively in industry for the supervision and control of industrial processes. SCADA systems are now also penetrating the experimental physics laboratories for the controls of ancillary systems such as cooling, ventilation and power dissipation.
Two of the most important characteristics of the SCADA system are its capability to collect data from any kind of installation and its ability to control these facilities by sending (limited) control instructions.
The standard SCADA functionality can be summarized as follows:

1. Data acquisition;
2. Data logging and archiving;
3. Access control mechanism;
4. Human-machine interface, including many standard features such as alarm display.

Figure 26 shows the typical hardware architecture with the connection layers in a SCADA system.

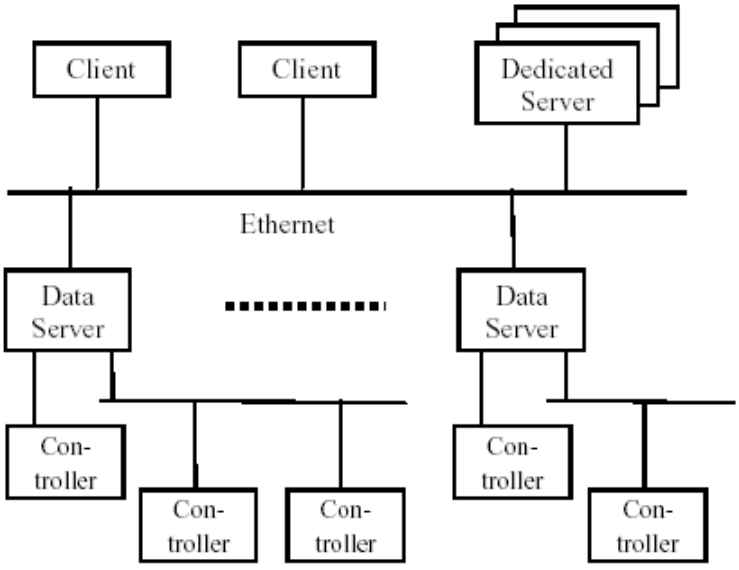


Figure 26 The CMS connection layers in the SCADA system

Two basic layers can be distinguished in a SCADA system: the 'client layer', which caters for the man-machine interaction, and the 'data-server layer', which handles most of the process data control activities (see Fig. 26). The data servers communicate with devices in the field through process controllers [21].
The latter, e.g. programmable logic controllers (PLCs), are connected to the data servers either directly or by networks or fieldbuses. Data servers are connected to each other and to client stations via an Ethernet local area network (LAN).

3.4.2 PVSS II internal database

PVSS II is a commercial SCADA system manufactured by the Austrian Company ETM [22]. It has been chosen by CERN to be the SCADA system for all LHC experiments. Its architecture is shown in Fig. 27. Besides the typical SCADA functionality, such as data acquisition, logging and archiving, alarm handling, access, control mechanism and a man-machine interface, PVSS II has the following capabilities: it can run in a highly distributed manner, it has multiplatform support (WNT and Linux), it is device-oriented and it has an advanced scripting facility. PVSS II contains an internal 'real-time' database, working on the object-oriented data-point concept. The data-point is the basic data container of a variable and could be a simple type (integer, float, etc.) or a complex type such as an array or a reference to another data-point [23].

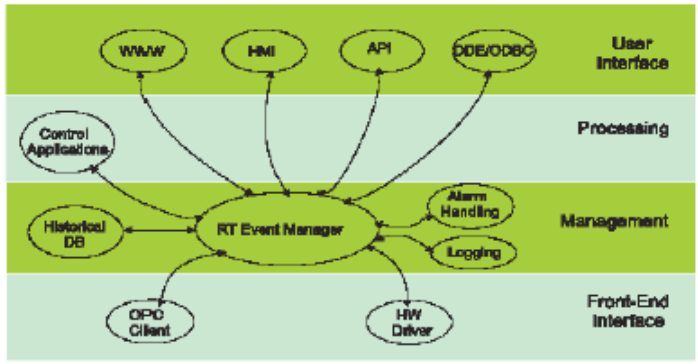


Figure 27 PVSS II system architecture

The application programming interface (API) of PVSS II consists of a C++ class library; it provides an interface to the external world, to access the data-points. Furthermore, PVSS II is capable of running scripts, which are triggered by an update of a data-point. They are interpreted and have a C or C++ like syntax.

3.4.3 External database

Since the amount of data for the front-end configuration is too big to be stored in the SCADA database, an external one will be used in CMS for managing such data. However, this database should be completely integrated into the SCADA framework; it should be accessible from the SCADA so that the SCADA features (e.g. alarming or logging) can be fully exploited. For prototyping, Oracle 9i was selected as the external database manager.

3.5 Connections to external systems: Interface to the DAQ system

A communication mechanism between DAQ and the DCS is needed for several purposes. During normal physics data taking, the DCS will act as a slave to the RCMS and will therefore have to receive commands and send back status information. Partitions will also have to be synchronized between the DAQ and the DCSs: the RCMS will instruct the DCS to set up specific partitions, which will be put under the control of the RCMS. Furthermore, alarms will be sent from one system to the others.
Following these requirements a native access from the cross-platform DAQ framework (XDAQ) to PVSS II, through the so-called API manager, has been chosen. XDAQ is a software product line that has been designed to match the diverse requirements of data-acquisition application scenarios of the CMS experiment [24]. These include the central

DAQ, subdetector local DAQ system for commissioning, debugging, configuration, monitoring and calibration purposes, test beam and detector production installations, as well as design verification and demonstration purposes.
Through this interface the DCS can access various functions of XDAQ, including direct access to PCI and VME systems, database products and run control services. This solution provides access to the whole PVSS II system, so that any kind of data can be exchanged between XDAQ and PVSS II in both directions. This fits all current and future requirements, since it uses the most generic interface to PVSS II.
Another aspect to be considered is the connection between the LHC and technical services. The LHC data interchange working group (LDIWG) has been created to define a communication mechanism for the exchange of information between independent services at CERN. This mechanism will be used to receive information about the LHC machine and the technical services in the experiments. The CERN joint controls project (JCOP) group will provide an interface in PVSS II for this mechanism.

4 The RPC system for the CMS experiment

4.1 Introduction

Resistive-plate chambers (RPCs) are gaseous parallel-plate detectors of ionizing particles, whose good spatial resolution is comparable to that of scintillators. In modern language, the original RPCs were single-gap counters operated in streamer mode. Soon, the double-gap structure was introduced to improve the detection efficiency along with the avalanche mode of operation, which extends its counting-rate capabilities.
RPCs have been approved as dedicated detectors for the muon trigger systems in both ATLAS and CMS experiments, where they will be operated in avalanche mode. The main CMS RPCs technical requirements are reported in Table 4, and Figs. 28 to 30 show one of the Bari RPCs prototypes at different stages of its construction.

Efficiency	$> 95\%$
Time resolution	≤ 3 ns (98% within 20 ns)
Average cluster size	≤ 2 strips
Rate capability	≥ 1 kHz/cm^2
Power consumption	< 2-3 W/m^2
Operation plateau	> 300 V
# Streamers	$< 10\%$

Table 4 CMS RPCs technical requirements

The trigger based on such a detector has to perform three basic functions simultaneously: to identify candidate muon track(s), to assign a bunch–crossing to the candidate track(s), and to estimate their transverse momenta.
In the streamer operation mode, the electric field inside the gap is kept intense enough to generate limited discharges localized near the crossing of the ionizing particle. The rate capability obtained in such operational conditions is limited (~ 100 Hz/cm^2) and not adequate for the LHC [25].
In the avalanche operation mode, instead, the electric field across the gap (and consequently the gas amplification) is reduced, and robust signal amplification is introduced at the front-end level.

Figure 28 A technician assembling a RPC

Figure 29 A view of the RPC at the Bari University laboratory

Figure 30 A different view of the Bari RPC

4.2 The working principle of the RPC

In this section the relevant detector parameters and the basic physical principle of RPCs will be discussed. A more detailed description of the RPCs can be found in [26].
The simplest configuration of the RPC detector is shown in Fig. 31.

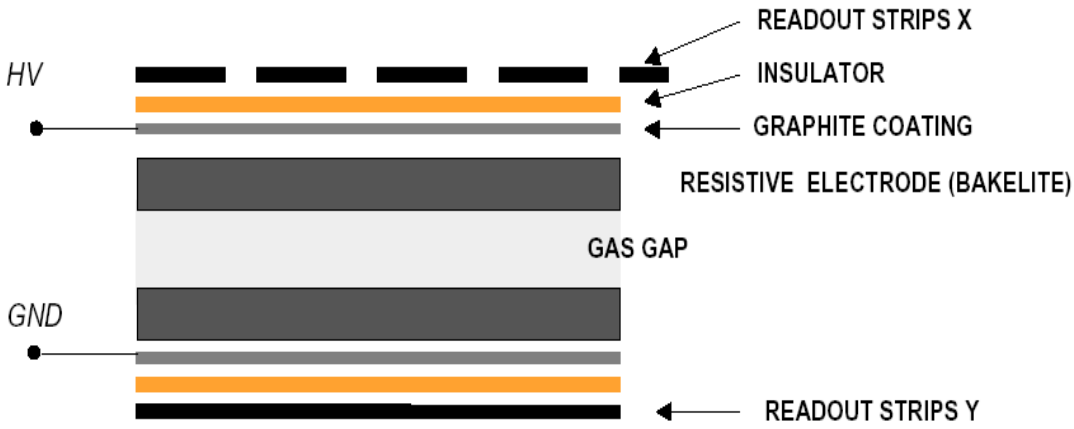


Figure 31 RPC detector configuration

The planar electrodes, made out of a resistive material (typically bakelite) having a bulk resistivity of $10^{10} - 10^{12}\ \Omega$ cm, are separated by a few mm.
The electrode resistivity mainly determines the rate capability, while the gap width determines the time performance.
Figure 32 shows the operation principle of the RPC, which can be explained as follows: the electrodes are connected to a HV generator in order to create a uniform and intense electric field (about 5 kV/mm) in the gap between them. A thin layer of graphite is coated over the external surface of the electrodes to permit uniform application of the high voltage. A generic gas mixture could be composed of argon, isobutene and an electronegative gas like freon, which may serve the purpose of limiting the amount of free charge in the gas. The strips are generally glued on the external surface of the gap, from which they are separated by a layer of insulator. Two different sets of strips oriented in orthogonal directions can be glued on both sides of the detector to obtain measurements in both directions [27].

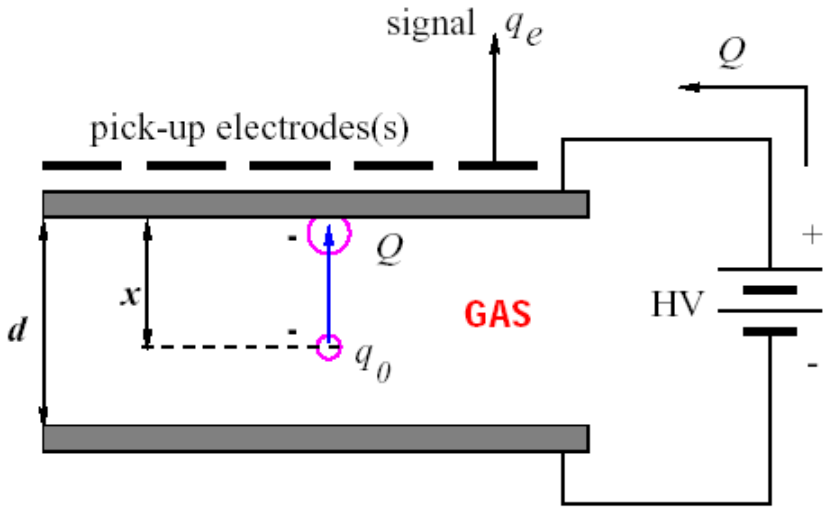


Figure 32 Principle of the RPC

For triggering purposes, the muon-momentum measurement by tracks bending in the magnetic field is much more important than the precise measurements of the muon direction. The solenoidal magnetic field bends tracks in the r–φ plane (plane perpendicular to the beam pipe). To find this bending, it is sufficient to measure the φ coordinate in several points of the track. For this reason the RPC detectors in CMS have strips, which measure only in one dimension. In the central (barrel) region of the CMS detector, the RPCs have strips parallel to the beam pipe, while in the endcap regions they are perpendicular to the beam pipe, with radial strips.

4.3 The RPC system: general overview and requirements

The principle of the pattern comparator trigger, or PACT, is illustrated in Fig. 33.
The RPC PACT [28] is based on the spatial and temporal coincidence of hits in four muon stations. We shall call such a coincidence a 'candidate track' or a 'hit pattern'. Because of energy-loss fluctuations and multiple scattering, there are many possible hit patterns in the RPC muon stations for a muon track of definitive transverse-momentum emitted in a certain direction. Therefore, the PACT should recognize many spatial patterns of hits for a muon of given transverse-momentum muon. In order to trigger on a particular hit pattern left by a muon in the RPCs, the PACT electronics performs two functions. It requires a time coincidence of hits in at least 3 out of 4 muon stations in a given direction and assigns a p_T value to them. The coincidence gives the bunch-crossing assignment of a candidate track that matches the spatial distribution of these hits with one

of many possible predefined patterns for muons with defined transverse momenta. The p_T value is thus given.

The solenoidal magnetic field bends tracks in the r–φ plane. A pattern of hits recorded by RPCs is used to determine the p_T of the muon by the pattern comparator (PAC) processor. The PAC ASIC is the device that fulfills the requirements of the PACT algorithm. In general, the PAC can be considered as a kind of content addressable memory (CAM). For every input value (54 signals from 4 layers of muon chambers), a 7-bit code (the highest-momentum-muon code) is presented. Up to 160 patterns can be programmed into the PAC for each hit from the reference plane. Programmable elements are shown as the red points in Fig. 34.

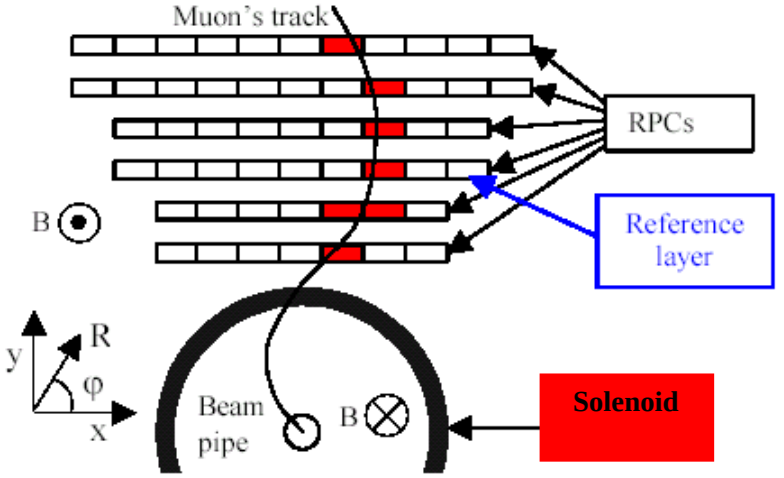


Figure 33 Principle of the PACT

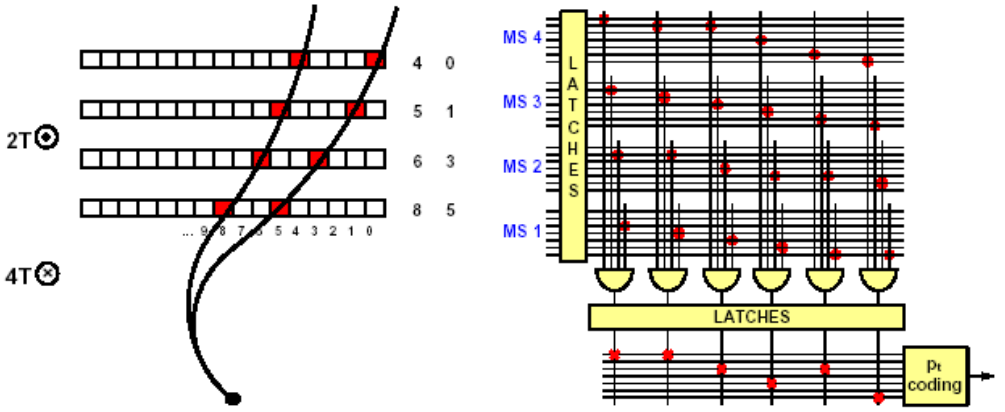


Figure 34 RPC trigger principle

4.4 RPC front-end electronics

4.4.1 Overview

The RPC trigger system can be conceptually divided into two parts:

- The optical communication system (OCS), which is responsible for bunch-crossing assignment of RPC data and for the transfer of data to the trigger electronics, and
- The main trigger electronics, housed in the underground Counting Room.

The input (information from the RPC) is processed and delivered to the trigger system by front-end boards (FEBs), which can be seen in Fig. 35.
In the RPC front–end electronics [13] there will be about 12,000 FEBs handling 16 channels each. Each FEB contains two front-end chips (FEC), each of which is an 8-channel ASIC consisting of amplifier, discriminator, monostable and differential line driver. The RPC readout strips are connected to FEBs by kapton foils, whose shapes are optimized to obtain the right channel characteristic impedance and to have the same arrival time for all channels at the front-end input.
Data communication from the on-detector electronics to the Counting Room is organized as follows: the RPC signals from FEBs are sent through a low-voltage differential signalling (LVDS) twisted-pair cables over a distance of typically 5 m to link boards (LBs) mounted on the detector. Here the data are synchronized with a TTC clock, providing bunch-crossing identification. The data are then compressed and time-multiplexed in order to reduce the number of optical links. The data are transmitted to the underground Counting Room, approximately 90 m distant, and fanned out to a number of trigger crates. At the transmitting end, the data transfer is based on an arrangement of master link boards (MLBs) and slave link boards (SLBs).
The SLB compresses the data and sends them through an LVDS twisted-pair cable to an MLB. Each MLB is connected to not more than two SLBs. The MLB compresses its own data, merges them with the SLB data and transmits them to the Counting Room through an optical fibre. In the counting room the data from each fibre are converted again to LVDS cables and split between several trigger boards (TBs). Decompression on a TB is performed by a link demultiplexer (LDEMUX).
The TB forwards data to the L1 trigger, while readout boards (RBs) handle the pipeline storage for the data acquisition system [29].

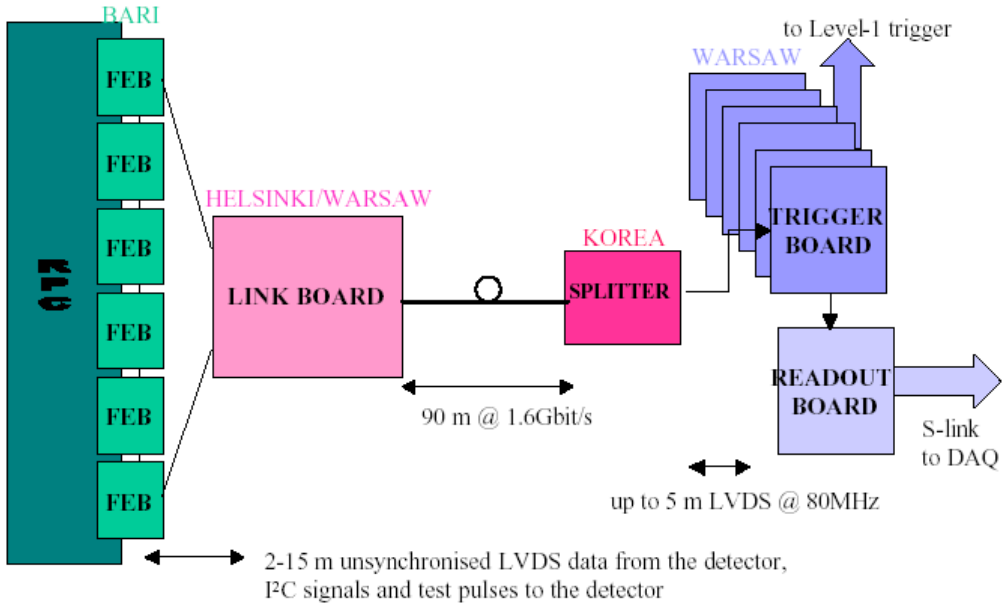


Figure 35 RPC front-end system

4.4.2 Data compression/decompression scheme

As already seen in a previous chapter, the trigger algorithm is based on muon-track search and classification in raw data from the RPCs grouped in four muon stations in the CMS magnet yoke. A huge interconnection network is needed to fulfil this task. It can be built in the Control Room only, approximately 120 m away from the detector. The data compression/decompression scheme is proposed to reduce the number of links needed for their transfer from the detector to the Control Room.
Many different styles of data compression are possible. The ones used in the RPC system are shown in Fig. 36.
Data are divided into equal-length data partitions. Each non-empty partition is sent together with its partition number and delay value. The latter defines the delay (in bunch-crossing) of the partition just being sent relative to the bunch-crossing associated with a given data word. The non-empty partitions of every data word are sent in descending order, starting from the partition of the highest number. An example of compression/decompression scheme is presented in Fig. 37, and a detailed explanation of it can be found in [30].

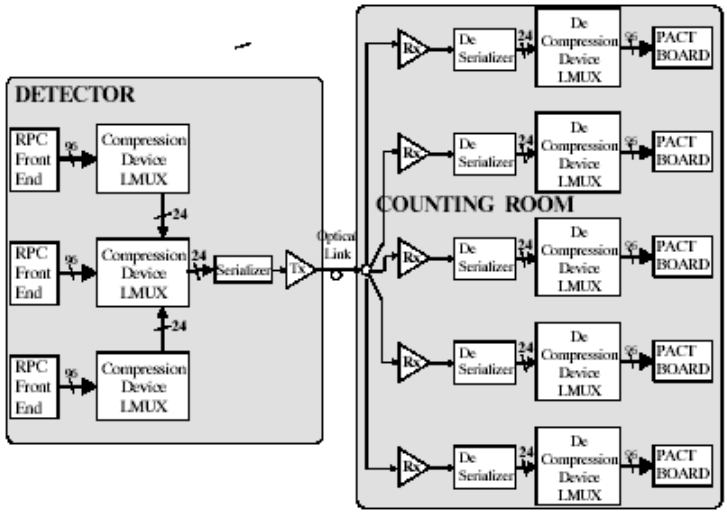


Figure 36 Functional blocks of electronics of the RPC-based muon trigger system

The scheme will be implemented using Xilinx FPGAs (Field Programmable Gate Arrays) as the LMUX/LDEMUX devices.
LMUX realizes the data compression algorithm (materialized in Fig. 38), whereas the LDEMUX realizes the data decompression algorithm (see Fig. 39).

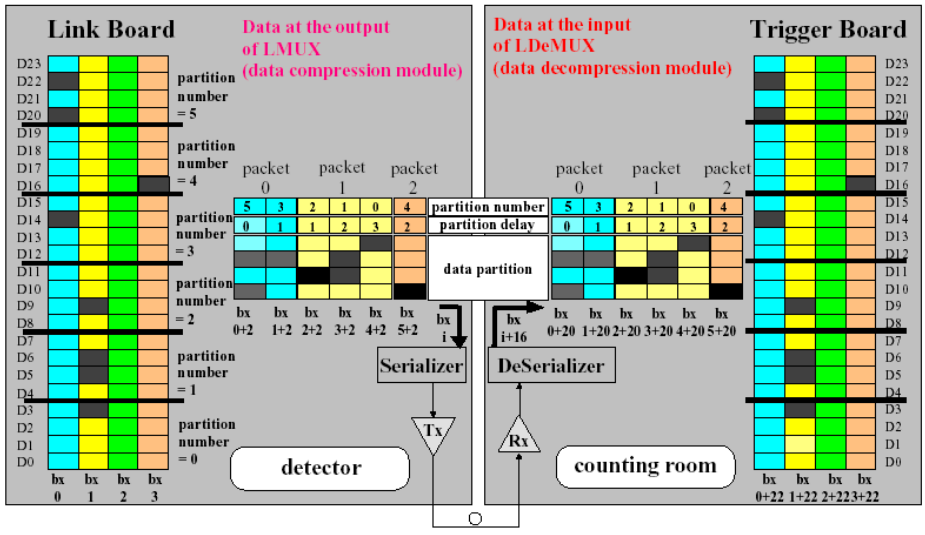


Figure 37 Example of compressed/decompressed data

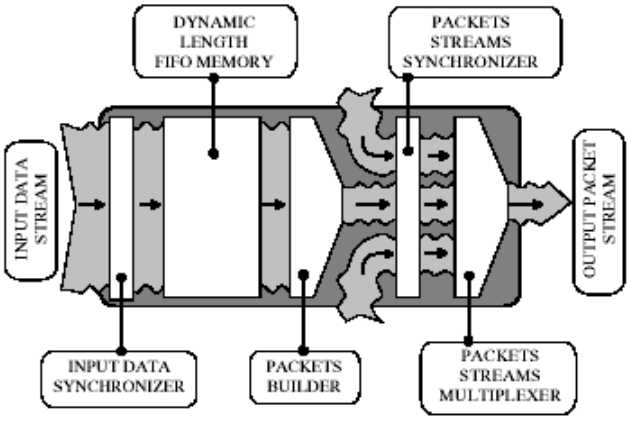


Figure 38 Data compression circuit

The data compression scheme in the LMUX FPGA is based on dividing the RPCs into partitions of 12 strips, and sending only those containing hits. New data are introduced into the device for each bunch-crossing. A block of input latches synchronizes the RPC data with an internal clock and stores them into an RPC output register (ROR). Data possessing at least one non-empty position are stored in a FIFO memory. Data from the FIFO are then shifted to the packet constructor, which selects non-empty partitions and supplies them with partition numbers and delay values. Sending of the current data word is aborted when the maximal delay value is reached. In this case, the last partition has an overload flag set to indicate that the data word being sent is not complete. When the packet constructor has no non-empty partition to send, an empty partition is sent with a non−existent partition number. The data from LMUX are sent to the serializer and optical fibre transmitter. The LDEMUX structure is presented in Fig. 39.

A single LDEMUX circuit works for one chamber only. Only partitions from the selected chambers are accepted (the chamber number is compared with the base number). The accepted partitions are fed into the shift registers. A shift register consists of D+1 positions, where D is the maximum delay value. Each position of the shift register has a delay index assigned to it, with values from 0 to D. If the partition's delay value is equal to the delay index then the partition data are shifted, by the LDEMUX, to the output data buffer, according to the partition number.

A partition that was sent immediately by LMUX, i.e. one with zero delay value, is fed into LDEMUX when it reaches the end of the shift registers (delay index = 0). On the contrary, the partition with the maximum delay value will be fed into LDEMUX immediately. The method provides compensation of delays between the LMUX and LDEMUX circuits. When LDEMUX receives a 'broken' data packet (with set overload flag), the output data are modified according to a special algorithm (for example, all bits of the data word are put to zero) [13].

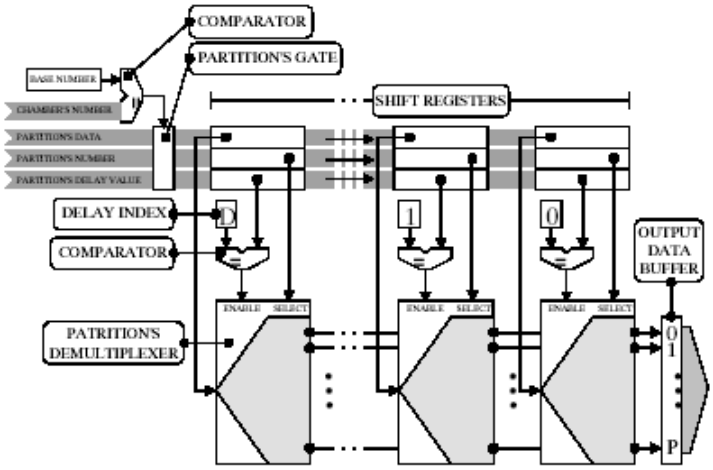


Figure 39 Data decompression circuit

4.4.3 The Link Board description

In the data transmission system of the RPC, the signals from FEBs are sent through an LVDS twisted-pair cable to the LBs, of which a prototype is shown in Fig. 40.
Each LB receives data from up to 6 FEBs = 96 channels. To further cut down the number of fibre-optic links required in the system, two kinds of LB are used, slave and master. The division into SLBs and MLBs depends on the occupancy of the detector, which varies considerably between its different parts. In the places where the hit rate is highest, only MLBs are used. The SLB compresses the data and sends them through an LVDS twisted–pair cable to a MLB, each of which is connected to no more than two SLBs, as shown in Fig. 41. The MLB compresses its own data, merges them with the SLB data and transmits them to the Counting Room through an optical fibre. In the Counting Room the data from each fibre are converted again to LVDS and split between several TBs. All LBs will be housed in Link Boxes (LBxs) located around the CMS iron yoke. The only exception is the case of those LBs serving chambers in the RE1/1 sector. The limited length of standard LVDS cables (~ 10 m) forces us to place those LBs in the corner between barrel and endcap hadron calorimeters. Standard LBxs cannot be used here because of these severe space limitations. In order to gain some space, a smaller number of so-called large link boards (LLBs) is foreseen. Each LLB receives data from 8 FEBs = 128 channels. There are two optical fibres coming out of every three LLBs.

Special Large Link Boxes (LLBxs) for the RE1/1 sector are then placed in the corner between barrel and endcap hadron calorimeter and six LLBs will be housed in each box. Two of them are MLLB, each sending data to two optical fibres and each receiving data from two SLLBs.
The RE1/2,3 and RE2 chambers will be mounted on the opposite surfaces of the same iron disk YE1. Therefore they will have common LBxs. There are 12 such boxes in each endcap, each serving 30° and housing 6 MLB +10 SLB = 16 LBs.
The RE3 and RE4 chambers will be connected to six LBxs in each endcap, each serving 60° and housing 6 MLB + 10 SLB = 16 LBs.
An inventory of several of these LBs, according to their position, is presented in Tables 5 to 7.

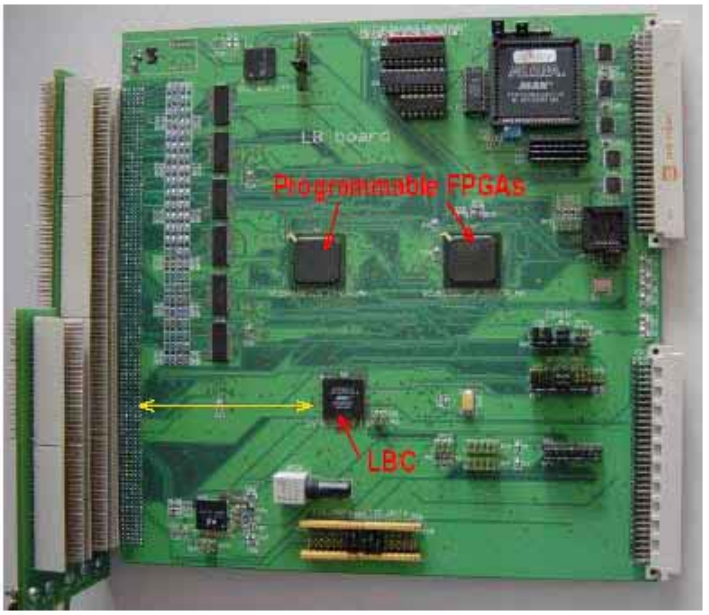


Figure 40 A link board prototype

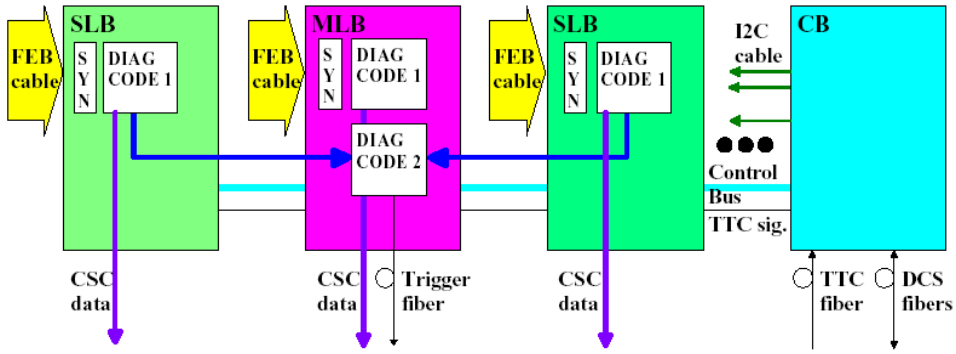


Figure 41 Connections between slave link boards and master link board

Sectors	LBxs	MLB	SLB	MLB + SLB	CB
Sectors 4, 10	1	5	10	15	2
Sectors 1–3, 5–9,11–12	1	5	8	13	2
Wheel	12	60	100	160	24
Barrel	60	300	500	800	120

Table 5 Inventory of the LBs system in the barrel

RE11	Per LBxs			Per 2 endcaps		
	Δφ	MLB/RE11	CB/RE11	LBxs	MLB/RE11	CB/RE11
	60º	6	1	12	72	12

Table 6 Inventory of the LLBs in RE1/1

Sectors	Per LBxs					Per 2 endcaps				
	Δφ	MLB	SLB	MLB+ SLB	CB	LBxs	MLB	SLB	MLB+ SLB	CB
RE1/2/3 + RE2	30º									
RE3	60º	6	10	16	2	12	72	120	192	24
(RE5)	30º	4	6	10	2	24	96	144	240	48
Total without RE5						48	288	480	768	96
Total with RE5						72	384	624	1008	144

Table 7 Inventory of the LBs in the endcaps

The overall inventory of the Link System is given in Table 8, where the number of boards and links without RE5 are given, together with those including RE5 (in parenthesis).

Sector	MLB	SLB	MLB/RE11	CB	Fibres
Barrel	300	500	----	120	300
Endcap	288 (384)	480 (624)	72	108 (156)	384 (480)
Total	588 (684)	980 (1124)	72	228 (276)	684 (780)

Table 8 Inventory of the whole LBs system

More detailed information on the Link Board System can be found in [31], where different documents contain also a full description of the subdivision of sectors (for the RPC system)

4.4.4 Link Boards boxes

A link board box is a mechanical enclosure, which will contain link boards (see Fig. 42), control board (to be described later) and backplane. Link boxes will be located on the balconies around the detector, except for the RE1/1 sector, where they will be placed in the nose of the endcap. The LBxs receives the FEB data and control them. It will share LV power supplies with FEBs.
Two different types of LBxs will be used in the experiment:

- Custom-made LBxs for the RE1/1 region, and
- VME crate link boxes for the rest of the system.

If some boards need to be changed while the experiment is running, an access to the enclosure is guaranteed from the top. All external cables, fibres, and cooling services are routed from the same side of the box.

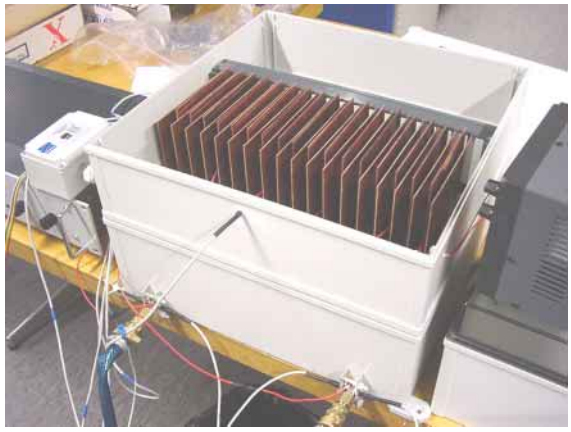


Figure 42 Prototype of the link board box

4.4.5 Splitter system in the Counting Room electronics

The RPC trigger logic is naturally divided into 12 sectors of 30° each, with one sector of one η-tower treated by one trigger board. Since a bent muon track does not respect the chamber boundaries, the cones in which the PAC processors find the candidates overlap. Therefore, most of the chambers have to be connected to several trigger boards, and the data received from one MLB have to be distributed to several destinations to ensure the proper functioning of the trigger. One link has to be split to different trigger boards serving up to two sectors in ϕ and up to four towers in η, and to the readout board as well. The task of distributing the signal to several destinations is performed by a splitter board, which is a simple module consisting of a fibre optic receiver, a deserializer and nine LVDS connections to transfer the data to the trigger and readout boards. The output of the deserializer device is directly fed to the LVDS drivers. Not all LVDS interfaces are used on all splitter boards. These will be located in the 8U extra space left in the trigger crates, making the distance to the TBs very short.
The first prototype of the SB is now under tests in Finland (at the Lappeenranta University of Technology), and a photograph of it is shown in Fig. 43.

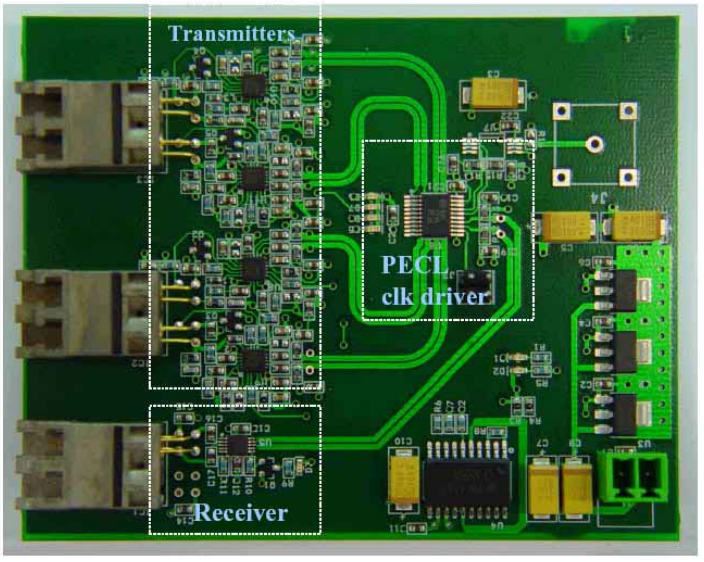


Figure 43 First prototype of the splitter board

5 The link-board control

The detector control system for the RPC detectors provides the possibility for transmission of control and diagnostic information to other systems supporting the RPC detectors.

5.1 Link-board control requirements

The main functionalities of the DCS RPC are the following:

1) HV RPC and LV DCS for the chamber and FEB;
2) RPC TC DCS (Trigger Crate Control), which controls 14 VME crates in 8 racks in the CMS Counting Room (lower floor);
3) RPC LB DCS, which comprises the control of the link board and FEB.

The LB DCS branch is used to [32]:

- **Configurate FPGAs (present) on the LBs, via Flash memory**. There are three FPGAs on the LB that need to be reconfigured quite often because of single-event upsets (SEU). Data from an ACTEL antifuse FPGA configured to act as the fieldbus interface will be sent to the Flash memory and then to the FPGAs to be loaded. The first step will require a data transfer of 3 Mbyte, which will not be done very frequently (once a day) and the connection required is unidirectional (to the LB). The data are to be loaded from the Flash memory onwards to the FPGA approximately every 4 min. Irradiation tests are required so as to determine this time interval.
- **Set LB control register (in FPGA)**,
- **Control TTCrx settings,**
- **Control GOL (optical transmitter) settings.** The GOL chip present on the LB is basically a simple 32-bit serializer with an integrated PLL. It takes a parallel input of 32 bits at an LHC clock rate of 40.08 MHz and sends it out at a baud rate of 1.6 Gbits/s**.** The GOL settings are controlled through I^2C. The settings that can be controlled include VCSEL driver current, PLL charge–pumps current and PLL lock time.
- **Allow an access to the LB test data (histograms, status register).** After previous operation, we will need to read histograms and rates from the LB every hour. Both of these operations will require about 800 bytes, which means approximately 2 Kbytes in total.
- **Access to the FEB control, via I^2C.**

5.2 Possible solutions for the LB control

After an investigation of the requirements needed to control the link board (discussed in the previous chapters), different approaches to the problem have been studied and considered. In the following chapters their implementation in the link board system will be described, together with the analysis which led me to reject them and to adopt, as final solution, a dedicated control board, which will be fully described in Chapter 6.

5.2.1 Description of the fieldbus technique

The fieldbus is a process-control network used for interconnecting sensors, actuators and control devices to one another. Typically, a twisted-pair cable (able to reduce external noise) connects the Control Room equipment with a number of field devices. Using a fieldbus, many devices can be connected to a single pair of wires, so that the installation costs are reduced.
Fieldbuses are widely used in industry, as they provide connections with the equipment deployed in the industrial control area such as PLCs, distributed I/O, etc. [33].
Communication specifications are often fixed with reference to the open system interconnect (OSI) layered model (Fig. 44). A fieldbus is specified according to the simplified OSI model, consisting of three layers: physical layer (PHL), data link layer (DLL) and application layer (APL). Layers 2 and 7 are implemented mostly by software and are therefore often called the 'communication stack'.

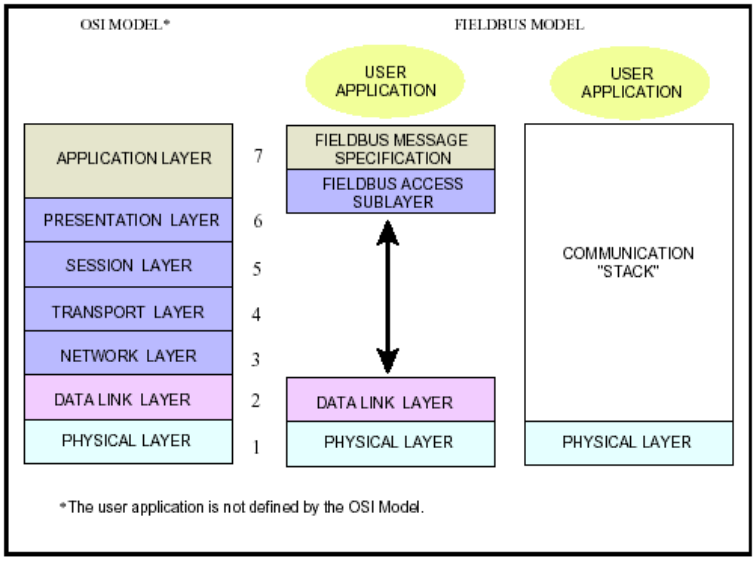


Figure 44 OSI layered communications module

The PHL is a mechanism that is used to receive and transmit electrical or optical signals to and from the medium so that data, consisting of ones and zeros, are transmitted from one node to the others. The PHL governs wires, signals, waveform, voltage, and everything related to electricity and optics.
The DLL is a mechanism to transfer data from a node to the other nodes that need the data. It also manages the priority of such transfer requests and orders them. The DLL interests are data address, priority, medium control, and everything related to message transfer.
Finally the APL consists of two sublayers, the fieldbus access sublayer (FAS), which manages data transfer, and the fieldbus message specification (FMS), which encodes and decodes user data.
The CERN fieldbus working group has selected three fieldbuses that can be used for LHC experiments: CAN, Profibus and WorldFIP. I will describe only the latter.

5.2.2 The WorldFIP fieldbus

The idea of using the fieldbus implementation to control the LBs in the RPC trigger system has been the first approach to the problem. After a comparison between the three fieldbuses recommended by CERN, the decision to use the WorldFIP fieldbus was taken. Before describing the LB solution, it is convenient to introduce the WorldFIP technology and its main properties.
WorldFIP (WF) is a network protocol designed to provide links between level 0 (sensors/actuators) and level 1 (PLCs, controllers, etc.) in automation systems. It is an open system that makes it possible to interconnect devices from different constructors. A WF network interconnects stations with two types of functionalities: bus arbitration and production/consumption functions. WF supports two basic types of transmission services: exchange of identified variables and exchange of messages. The exchange of identified variables services are based on a producer/distributor/consumer (PDC) protocol.
The WorldFIP PHL ensures the transfer of bits of information from one device to all other devices connected to the bus. The transmission medium can be a shielded twisted-pair wire or an optical fibre. The WorldFIP factory provides a set of hardware and software components designed or selected for achieving a low cost and easy implementation of different kinds of solution.
The WorldFIP hardware interface is made up of two complementary components: communications controllers and line tools. The communications controllers include the protocol mechanism. Each component proposes a list of services organized in three categories related to:

1. the bus arbitrator function;
2. the station function;
3. the network management.

Examples of communications controllers are FIPIU2, FULLFIP2, and MICROFIP chips.

Line tools cover the part of the PHL that depends on the communications medium used. Examples of line tools are FIELDRIVE, CREOL, FIPOPTIC–TS etc… [34].

5.2.3 The fieldbus solution for the LB control

The MICROFIP VY27257 (used in the first implementation of the LB control system) is an ASIC solution implementing the WorldFIP protocol, to be used in field devices able to communicate at three standard speeds: 31.25 Kbits/s, 1 Mbit/s and 2.5 Mbits/s. It can be configured as a station, and is then not able to run the bus arbitrator. The MICROFIP chip is packaged in the MQFP100 standard solution, and the 3.3 V or 5 V nominal power supply can be selected. The chip is able to operate with or without associated microcontroller (see Fig. 45), using FIELDRIVE or CREOL tools.

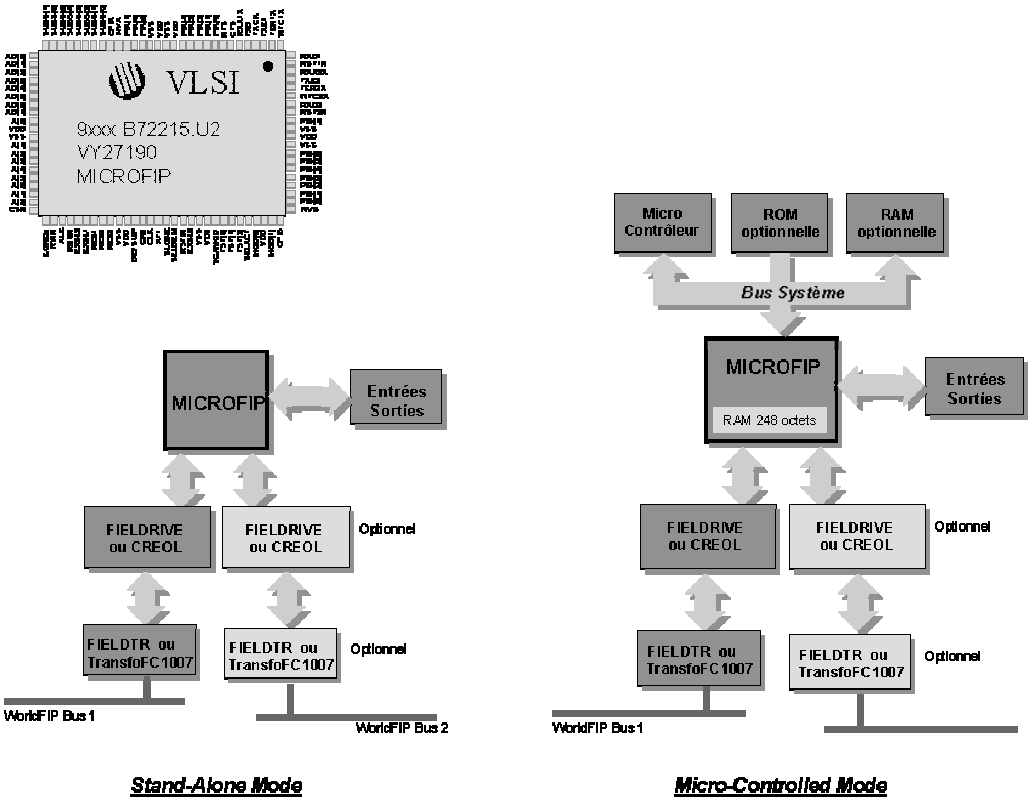


Figure 45 The Microfip working principle in stand-alone and microcontrolled modes

The two ways to run the Microfip, without or with microcontroller, are respectively identified as stand-alone and microcontrolled. Microfip operating in stand-alone mode allows direct interfacing with the process inputs and outputs through two 8-bit bidirectional ports. The port states are directly mapped on the network, using one produced variable for inputs, and one consumed variable for outputs. Many of the microcontrollers operating with a Microfip need no external logical glue. The use of the microprocessor is also simplified. In this mode the variables are configured using the Microfip control registers through the user-microcontroller interface.

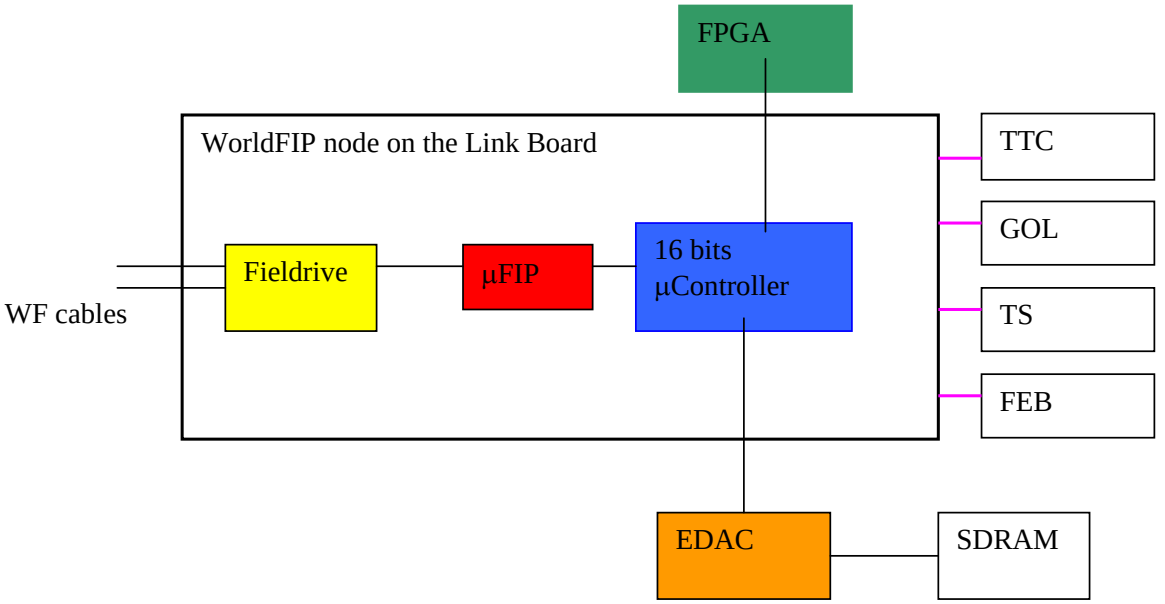


Figure 46 The WorldFIP node to be housed on each link board

Figure 46 shows the first control implementation system studied for the LB. The system consists of a microcontroller, the Microfip chip, the Fieldrive tool, the error detection and correction (EDAC) chip, few I^2C connections (pink lines), an FPGA and a SDRAM. All the above components should be housed on each LB.
The Microfip chip, working in microcontrolled mode, is connected from one side to the microcontroller, from the other side to the Fieldrive chip, which normally provides an interface between a communications controller (in this specific case, the Microfip) and a galvanic insulation transformer.
On the reception line the differential signal is first filtered, then Fieldrive generates the detection signal that informs the Microfip of the presence of a signal on the network.

The Fieldrive chip is then connected to the WF fieldbus through different cables and connectors.

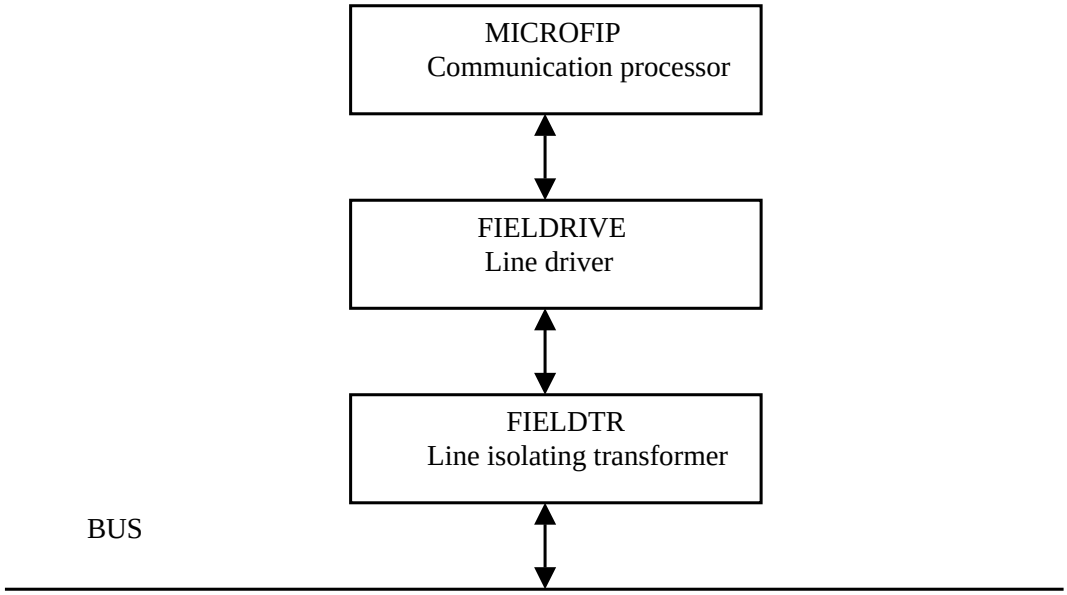


Figure 47 WorldFIP fieldbus subscriber connection

The communication processors (FULLFIP2, MICROFIP, etc.) must be connected to the bus through a line driver such as Fieldrive, which is especially designed to adapt the logical signal of the communication processor input/output with the signal of the WF fieldbus. Moreover, it is recommended in most applications to ensure a galvanic isolation between the bus and the line driver with a transformer such as FIELDTR (see scheme in Fig. 47). The insertion of a capacitor between the bus and the FIELDTR line-isolating transformer avoids transformer saturation by an eventual continuous current component (bus powered networks). The connection of the subscriber to the bus is generally made with a D-Sub 9-pin male connector.
In Fig. 48 is shown an example of the implementation of a fieldbus connection.

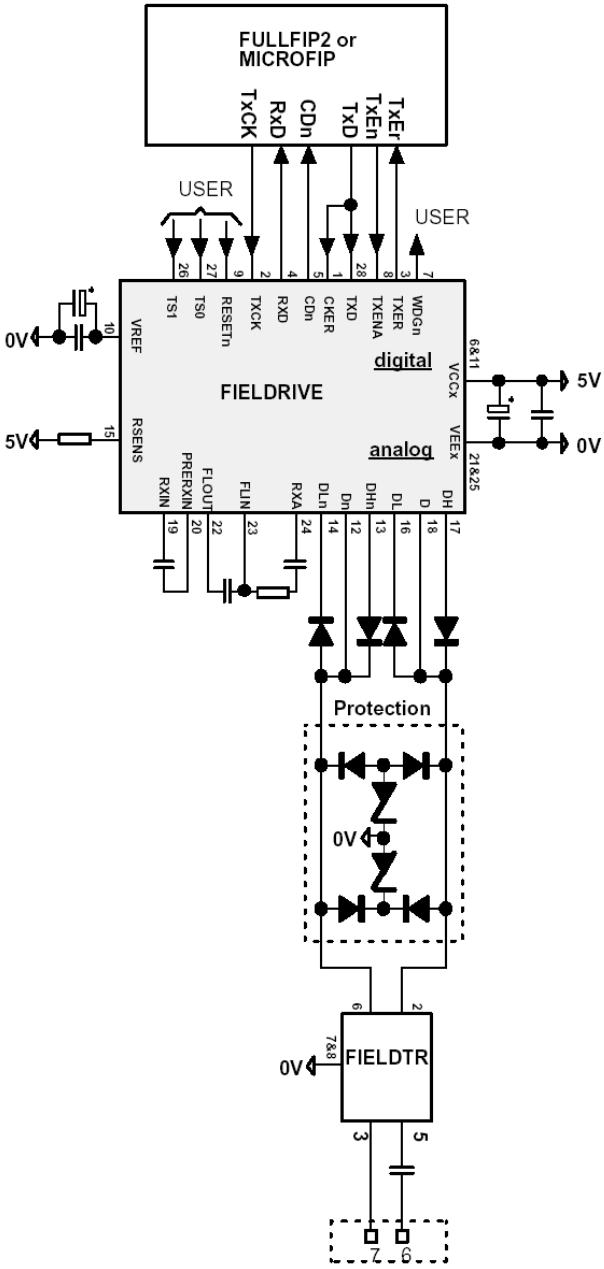


Figure 48 Example of implementation of a fieldbus connection

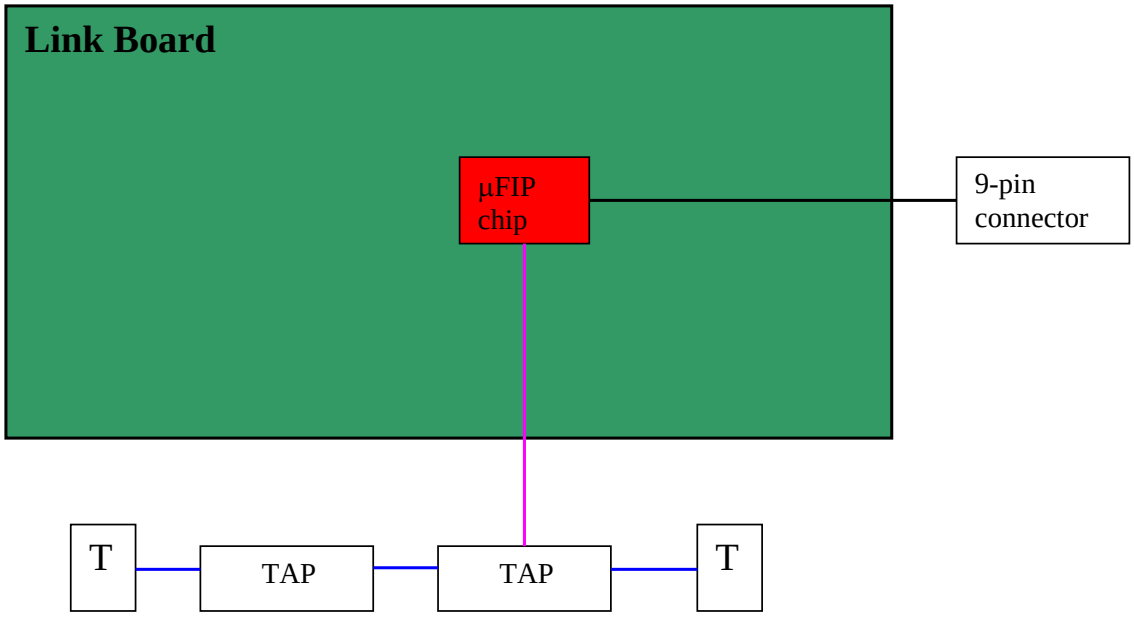


Figure 49 Cables and connectors connection on the LB only related to the WF node

The WF cable system consists of a trunk cable (in blue in Fig. 49) with drop cables (in pink in Fig. 49) connecting to each node. The drop cables are connected to the trunk by TAP boxes. A node may be connected to its drop cable in either of two ways:

- Subminiature 9-pin D-type connector, for use in benign environments,
- Circular connector, for harsh environment.

The trunk cable requires a terminating impedance (T in Fig. 49) at each end; this is physically small, and for convenience is normally included in the TAP boxes of the nodes located at the ends of the trunk cable.

After studying this solution for the LB, it was noted that using a WF node for each LB would have required a more expensive implementation, and more technical problems in case it would have been necessary to replace a component during the experiment. Then, a second and easier approach was considered: to use a unique node, able to control several LBs together.

Many searches led me to consider the ATLAS control solution, through the so-called embedded local monitor board (ELMB), described in the next chapter. If we adopted it for the RPC trigger system, a control board would have been able to control more LBs at the same time.

5.2.4 ELMB (from Atlas experiment) description

The ELMB [35][36] is a general-purpose plug-on board to be used in LHC detectors for a range of different FE control and monitoring tasks. It was developed by the ATLAS DCS group, but it will be used in the LHC-b experiment as well. The size of the printed–circuit board is 50 × 67 mm. The board is equipped with two connectors, one with 100 pins, the other with 40 pins. The ELMB is based on the CAN (control area network) serial bus system; it is radiation-tolerant, so that it can be used in a magnetic field. The ELMBs will be connected via the CAN bus, using the CANopen protocol for communication with a PC. Using a commercial CAN card, the data are passed into the PC. An OLE (object linking and embedding) for process control (OPC) server, which acts like a driver, makes the information available to one or many OPC clients. For data taking, monitoring and storing, CERN has chosen the commercial supervisory control and data acquisition (SCADA) package PVSS II. A block diagram of the ELMB is shown in Fig. 50.
The ELMB is divided into three sections: the CAN, the DIGITAL and the ADC parts. They are independently powered and separated with optocouplers to prevent current loops. Each one of the three parts is equipped with a low-dropout (LDO) 80 mA voltage regulator. These regulators provide current and thermal limitations, which is a useful feature for their protection against single-event latchup (SEL) errors.

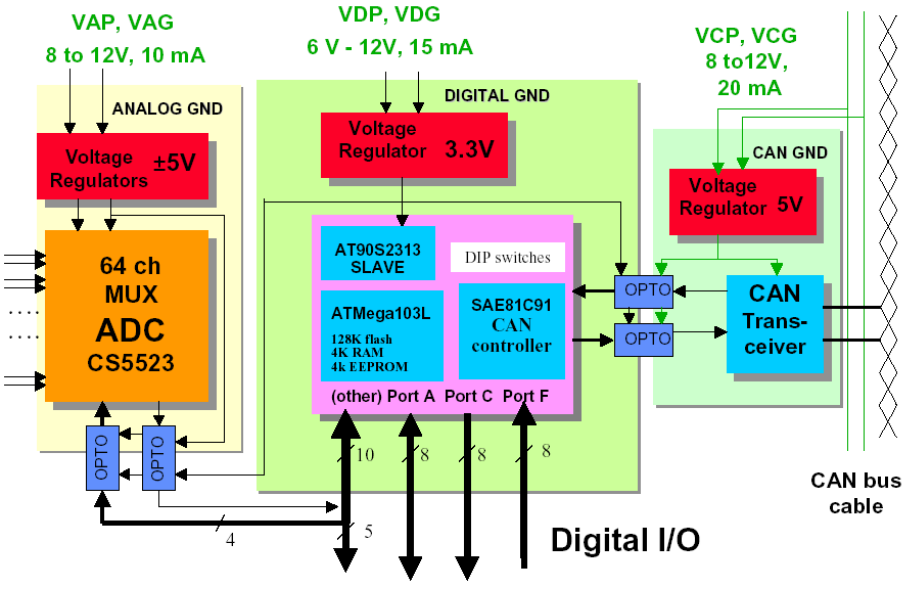


Figure 50 Block diagram of the ELMB

1) The CAN part

The CAN is one of the three standard CERN fieldbuses. CAN is especially suited for sensor readout and control functions in the implementation of a distributed control system because of its reliability, of the availability of inexpensive controller chips from different suppliers, its ease of use and wide acceptance by industry. The error-checking mechanism of CAN is of particular interest in the LHC environment where bit errors due to SEE will occur. The CAN controller registers a node's error and evaluates it statistically in order to take appropriate measures. These may be extended to disconnecting the CAN node that produces too many errors.
The on-board CAN controller is the Infineon SAE81C91, a so-called 'full-CAN controller' with buffers for 16 messages. It is connected to the CAN bus via high-speed optocouplers to an interface circuit (Philips PCA82C250), which translates the logic levels to CAN levels. This bipolar integrated circuit has an operating temperature range of −40 °C to 125 °C and contains several protection features. The microcontrollers communicate with the CAN controller by a serial interface.

2) The DIGITAL part

The local intelligence of the ELMB is provided by two microcontrollers of the AVR family of 8-bit processors, manufactured by ATMEL. The ELMB's main processor is the Atmega103L running at 4 MHz. This CMOS integrated circuit contains on-chip 128 Kbytes of Flash memory, 4 Kbytes of SRAM, 4 Kbytes of EEPROM and a range of peripherals including timers/counters and general-purpose I/O pins. The main monitoring and control applications are running on this processor.
The second on-board microcontroller is a much smaller member of the same AVR family, the AT90S2313 with 2 Kbytes Flash memory, 128 bytes of SRAM and 128 bytes of EEPROM. The main purpose of this processor is to provide in-system programming (ISP) via CAN for the Atmega103L processor. In addition it monitors the operation of the main processor and takes control of the ELMB if necessary. This feature is one of the protections against the SEE. In turn, the Atmega103L monitors the operation of the AT90S2313 and provides ISP for it. Fig 51 shows the front side of the ELMB.

3) The ADC part

A 16-bit differential delta-sigma ADC with 7-bit gain control (Crystal CS5523) is used and placed at the back of the printed-circuit board.
The CS5523 is a highly integrated CMOS circuit, which contains an instrumentation chopper stabilized amplifier, a digital filter, and calibration circuits. 16 CMOS analog differential multiplexers expand the number of inputs to 64. The AD680JR from analog devices supplies a stable voltage reference. The ADC input can handle a range between +4.5 and −4.5 V.

Figure 51 The ELMB front side

Figure 52 shows the back of the printed-circuit board with the ADC, the voltage reference and 16 multiplexer circuits.
The implementation of the ELMB in the LB system is shown in Fig. 53: both in the case of the barrel and in the case of the endcaps, the maximum number of LBs housed in one box is 16. There is need for at least two ELMBs in each box, the internal connection between several LBs being made through a local bus, and a maximum number of 8 LBs being connected to the same ELMB. The situation in RE1/1 will be different: in this case there are 6 LLBs in each box, which means that only one ELMB will be needed to control all of them [35].

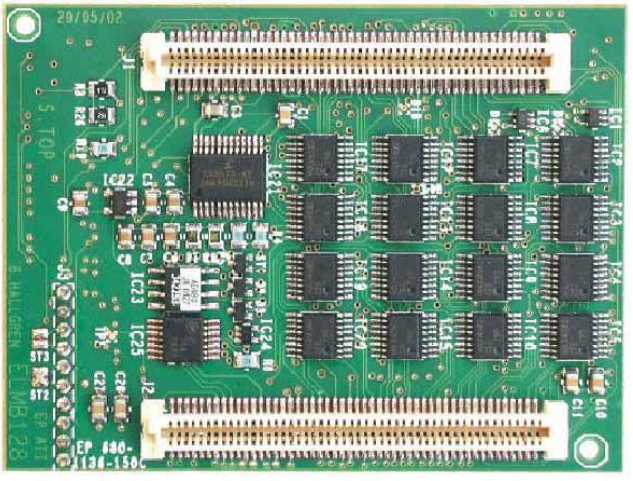


Figure 52 The back of the ELMB

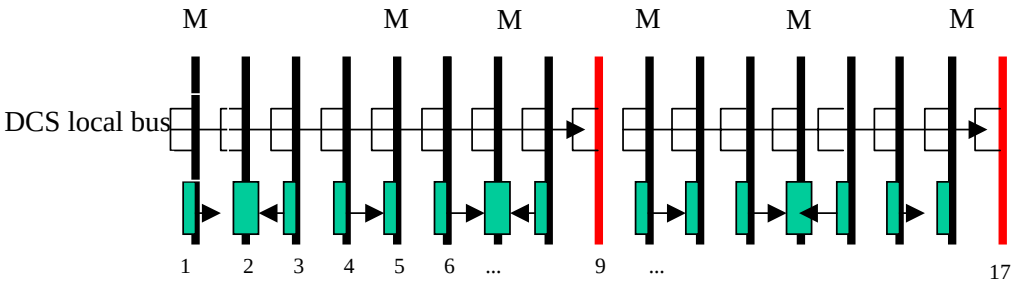


Figure 53 ELMB possible implementation in the LB system

5.2.5 Description of control module and front-end control module

The second possibility for the control of the LBs is to use the system developed in CMS for the control of the tracker. The internal tracker control system consists of three main functional elements [38]:

1) A network based on a simple token-ring architecture between the Control Room and the embedded electronics,
2) A front-end controller (FEC) card in the Control Room VME crate,
3) A communication and control unit (CCU).

A general block diagram of the tracker readout organization is shown in Fig. 54.
The front-end module contains the analog ASICs directly attached to the detectors as well as all the multiplexing and driving electronics needed to send the analog information outside. This module also contains the optoelectronic element needed to transform the electrical signal into light.
The front-end digitizer (FED) module, external to the detector, houses the digitization logic and the L1 of digital buffering in the DAQ tree.
The control module provides the local distribution of timing signals and contains the electronics that controls the front-end module. It also receives the timing information and distributes it to the FE module.
In the control module, the CCU receives information from an optical link via the Link Controller interface and converts this into the two bus protocols used on the module, i.e. the I^2C protocol and the parallel-bus (Pbus) protocol. Other interfaces supported by the CCU are a simple 8-bit wide memory-oriented, non-multiplexed bus, a programmable parallel interface, which can be used to control or read switches or other semistatic elements, and a decoded trigger port, for trigger information encoded in the FEC unit.
One CCU ASIC mounted on a CCUM is dedicated to a set of tracker front–end modules.

To complete the overview of the previous picture, a short description of the FEC is needed.
The FEC is used for the slow control link in the CMS tracker. It is implemented as a PMC module, i.e. a piggyback board with a PCI interface. The FEC is the master of the network and uses two fibres for sending the timing and data signals to the slave modules, which in turn use two fibres to transmit a return clock and the return data back. The fibre connections and the I^2C connections between CCUs are doubled to provide redundancy [39].

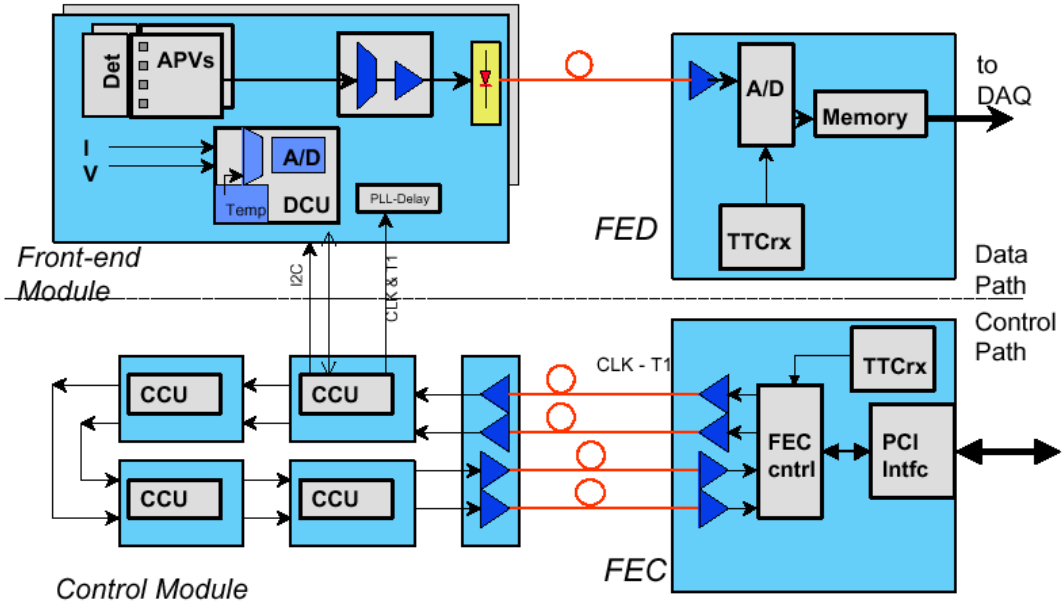


Figure 54 Tracker readout scheme

5.3 Conclusions

The idea to use a solution similar to the one used in the tracker system has been accepted by our Collaboration and, for the final LB implementation, we will use the CCU chip to control the LBs. It will be put on a dedicated board, the control board, described in the next chapter.

6 The Control Board design

6.1 Introduction and technical requirements

The main functionalities of the slow control system of the RPC detector, schematized in Fig. 55, are [40]:

1. Communication with managing host;
2. Transmission of the control and diagnostic data to and from the FEBs through an I^2C interface;
3. Transmission of the control and diagnostic data to and from the LBs;
4. Refreshing of the configuration of the programmable FPGA chips.

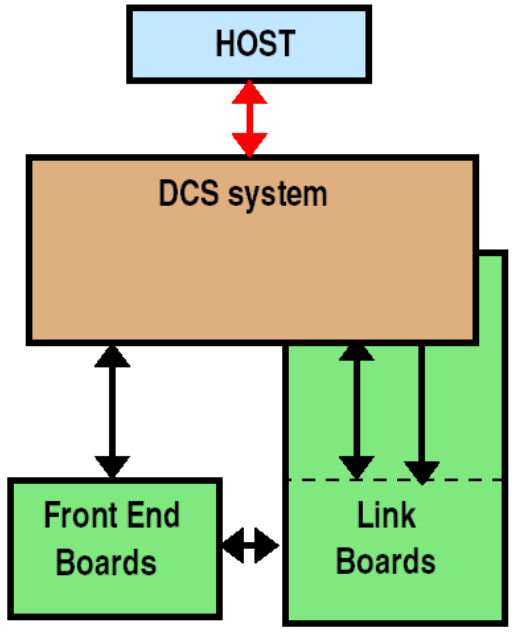


Figure 55 Slow-control architecture in the RPC system

Additional requirements are:

• High level of radiation hardness obtained with:
  – Proper technology;
  – Proper structure (redundant logic, error–correcting codes, ...);
  – Proper algorithms (detection of correctable errors, refreshing memory content, ...);

• The radiation-caused errors should be detected and corrected, when possible.

As with all CMS front-end electronics, all these requirements must be considered in the light of the high radiation environment in which they will have to function. This sets special constraints on the solutions considered. The basic unit in the RPC Link DCS is a set of one control board (CB) and up to eight LBs in its control. They are connected by a local bus (LBus). The main element in this system is the CB, which is responsible for all of the link control operations. Its key components are the TTCrx (trigger and timing control) chip that receives timing and trigger data, the CCU25 (communications and control unit, 25–μm technology), which controls all the communication between external managing units and the local interfaces, I^2C and the LBus and finally the control board controller (CBC), which essentially provides an interface between the CCU25 and the LBus. These are all designed in radiation-hard technology.

6.2 Structure of the system

The RPC slow-control system consists of a single CB servicing up to 8 LBs (two CBs per LBx). The CB is connected to the outer world through the CCU chip and the TTCrx chips.
The CCU chip provides the communication with the managing host and drives the local interfaces: I^2C and LBus. Since CCU has limited capabilities regarding the distribution of TTC broadcast commands, an additional TTCrx chip is required.
On each LB a dedicated link board controller is located, which interfaces the LB internal registers with the LBus, assures the configuration and cyclic reconfiguration of FPGAs, and manages the memory storing the configuration data.
The DCS will use 9 CCU chains, each consisting of a single FEC board, and up to 27 LBxs with the structure shown in Fig. 56. The system consists of four parts:
1) The CB, equipped with the CCU and CBC, divided in two chips (control board interface controller and control board peripheral controller);
2) Additionally the CB distributes the clock signal for the TTCrx chips located on the LBs;
3) The LBC interfaces the LB chips with the LBus and configures the FPGA chips;
4) The CB is connected to a maximum of 8 LBs via the LBus, the asynchronous bus with 16 address lines and 16 data lines.

Since the DCS is essential for the correct operation of the detector support system, special measures have been taken to ensure the radiation hardness of the system.

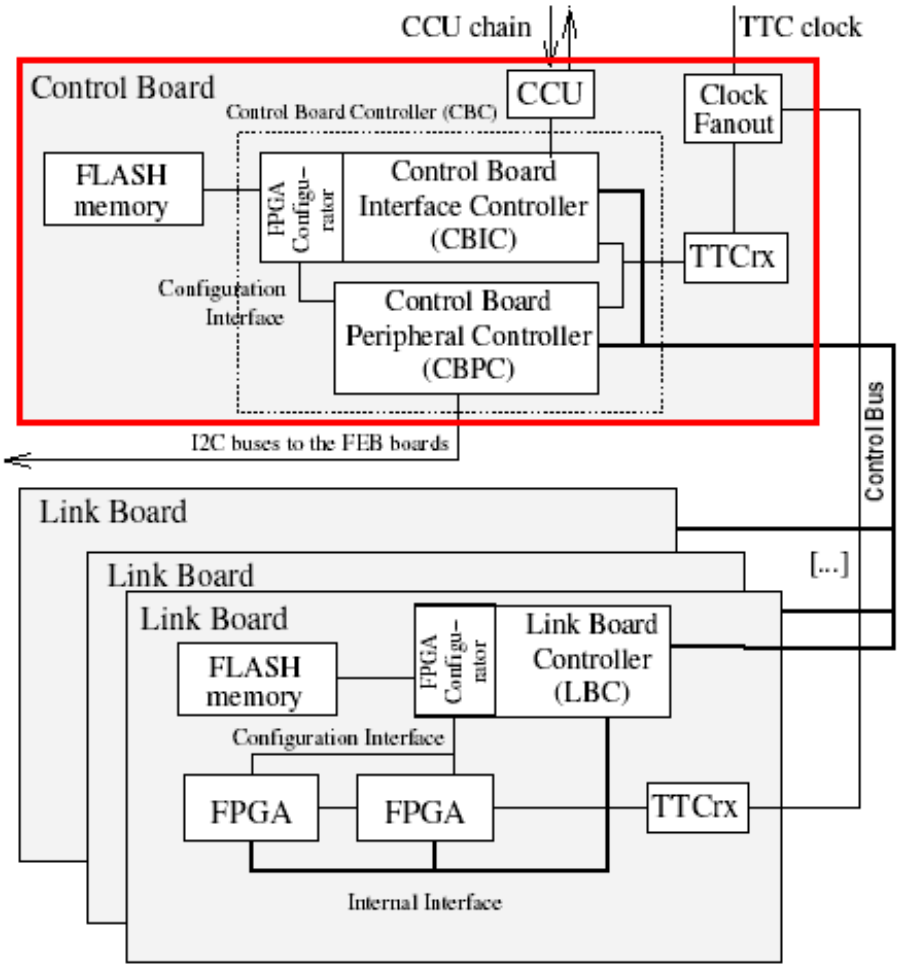


Figure 56 Structure of the DCS in the RPC trigger system

6.3 Design of the first prototype of the control board

6.3.1 Components description

Each CB will contain a CCU chip, TTCrx chips and some additional interfacing logic integrated in the CBC. This CBC is implemented in a radiation-hard programmable chip (e.g. antifuse-based FPGA). Its purpose is mainly interfacing the CCU and TTCrx with the LBus.

The CCU25 chip, manufactured in a special radiation–hard technology, is the heart of the system and is merely complemented by the TTCrx chip. It is by configuration an ASIC, which features numerous types of bus interfaces for connecting to both the managing host and the local communication system. The CCU25 chip is used to ensure communication between the managing host and the DCS. This chip offers a wide range of communication ports, but in our case only the memory port is used for this purpose. The CCU memory port offers the asynchronous bus with 16 address lines and 8 data lines. According to the documentation, the memory port is theoretically able to provide a communication speed of 4 MB/s.

The TTCrx chip [41] is ASIC-designed as part of the overall trigger and timing distribution system for the LHC experiments.
The TTC system basically distributes properly encoded:

- The basic LHC 40.08 MHz clock frequency
- The experiment L1 trigger signal
- User-defined slow-control information

The TTCrx also contains several internal registers used for the control and monitoring of its operation.

The reprogrammable FPGA chips are widely used in the RPC electronic systems. The radiation may destroy the configuration data of these chips and, therefore, they need to be periodically reprogrammed. The FPGA configurator core provides a possibility to configure the FPGA chips with the data stored in the Flash memory, or with the data sent through the LBus (e.g. directly from the host computer through the CCU chip).
To accomplish this task, the FPGA configurator core contains the Flash memory controller able to write data into the Flash memory, to read data from the memory and to control their integrity. The data kept in the Flash memory are protected with the ECC code, which allows the detection of problems of data corruption before the data are useless. The data-protection scheme allows for the correction of single-bit corruption and the detection of two-bit corruption. The whole configuration data are additionally protected with the checksum, so it is unlikely that the corrupted data will be used to configure the FPGA chip. When data corruption is detected, the FPGA configurator notifies the managing host that the data in its Flash memory need to be refreshed.

The first CB prototype is shown in the photograph of Fig. 57, and its implementation in Fig. 58.

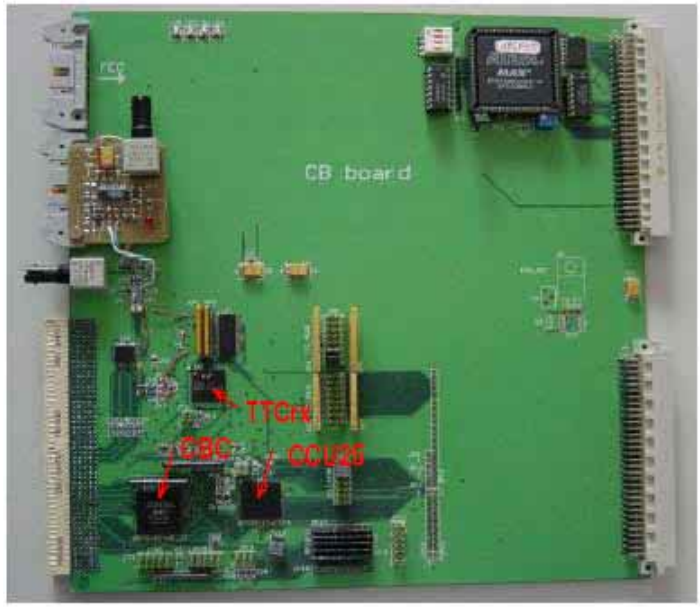


Figure 57 The control board prototype

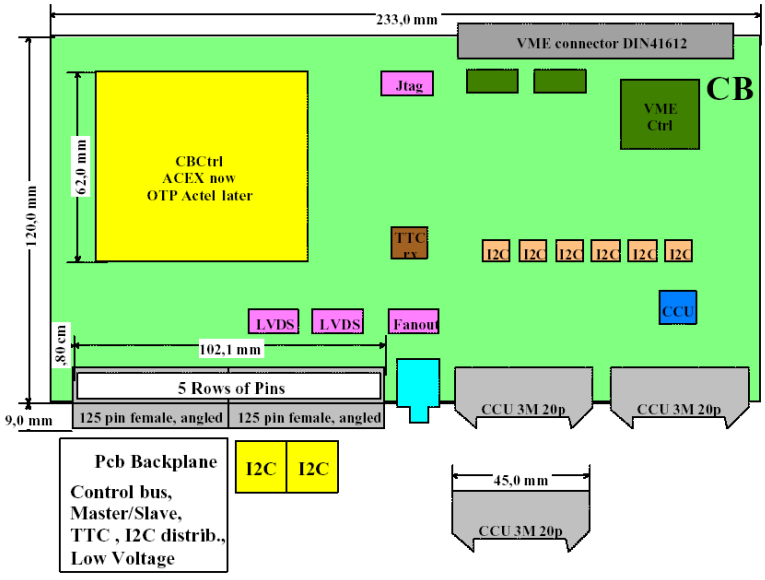


Figure 58 The CB implementation

6.3.2 Control-board controller

The essential part of the CB is the CBC, which links the CCU chip with other interfaces used in the DCS.
The CBC performs the following tasks:

• Interfacing between the CCU memory port interface and the LBus; because the DCS LBus uses the 16-bit data bus, while the CCU memory port uses the 8-bit data bus, linking these two buses requires a special logic. Each LBus transfer requires two LBus transfers (the first one for bits 0…7 and the second one for bits 8…15). However, some register may use only the bits 0…7 (e.g. in the case of the I^2C controller core). A special mode is therefore provided, where each memory port transfer corresponds to only one LBus transfer.

• Interfacing between the managing host and the FEBs; the FEB chips use the I^2C interface to send/receive the control and diagnostic data. In the first version of the DCS, the built-in CCU I^2C controller was supposed to drive the I^2C buses. Unfortunately the tests performed during the last months have shown that this controller lacks the functionalities (e.g. multibyte transfers), which are essential for the communication with FEBs. It is therefore necessary to add another I^2C core, which can fully support the requirements of FEBs communication.
To improve the flexibility of the CBC, the design has been divided into two parts:

1) The Control Board Interface Controller (CBIC), which implements the essential functionalities of the CBC (interfacing between the CCU and the LBs and configuration of the reprogrammable FPGAs). To improve the radiation hardness of the system, this core is implemented in the radiation-hard antifuse FPGA and uses the redundant logic with the SEU detection system;

2) The Control Board Peripheral Controller (CBPC), which implements the advanced functionalities of the CBC. For flexibility reasons it is implemented in the reprogrammable FPGA (Xilinx family). The configuration data for the CBPC are stored in the Flash memory, allowing for a periodical fast reconfiguration of the CBPC chip (the previous tests have shown that for the Xilinx Spartan IIE 300 series chips, the reconfiguration time was below 30 ms).

6.4 The link-board controller

The central part of the LB is the LBC, which is implemented on a single radiation-tolerant FPGA. The LBC interfaces the internal interface used for the on-board communication between the FPGA chips, with the LBus used to transfer data between the LBs and the CB.

The second functionality of the LBC is to refresh the configuration of the reprogrammable FPGA chips located on the LB. This task is accomplished with the FPGA configurator included in the LBC.
To increase the radiation hardness of the DCS, the LBC uses the redundant logic with the SEU detection system.

6.5 The control software

The main goals of the control software are:

1. To perform the subsystem run control;
2. To implement the subsystem DCS;
3. To perform on-line monitoring of the subsystem;
4. To provide the tools needed to perform on and off detector-diagnostic tests;
5. To provide a repository for storing information about the state, the history, etc., of each hardware item;
6. To provide the tools needed to perform the analysis of the whole subsystems, e.g. to find possible causes of the lack of input from one particular strip;
7. To perform the subsystem calibration;

The software system will consist of the following components.

Subsystem DCS

The task of the subsystem DCS will include the control and monitoring of power supplies in the VME crates, LBxs and their proper cooling, and the control and monitoring of the HV on RPCs. The DCS subsystem will be integrated and connected to the global DCS by using the PVSS II software.

Subsystem run control

Subsystem run control (RC) will be implemented as several XDAQ applications. XDAQ will be used to integrate the subsystem RC with the global RC. Accesses to hardware will be mostly implemented on top of the internal interface library, which provides transparent communication with hardware and seamless integration with the VHDL code used in the preparation of firmware for the hardware devices.
RC data (FPGA boot files, setting of registers, etc.) will be stored in a database. Dedicated applications will be developed in order to prepare and browse the configuration data sets needed for different types of runs, such as calibration runs, diagnostic runs, different physics runs. An especially challenging element in this area seems to be the translation of muon patterns and their corresponding momenta, calculated during simulation, into algorithms implemented in VHDL codes.

On-line monitoring

An important feature of the RPC trigger system is its on-line monitoring and diagnostic capabilities. Standard diagnostic blocks, such as counters, histograms, selective readout, implemented in VHDL, are used throughout the system. The purpose of the on-line monitoring is to control, readout, and archive and analyse the data collected by the diagnostic blocks. In case of severe problems encountered during physics runs, an alarm can be submitted to the RC.
On-line monitoring software will be built on top of the internal interface library. It will especially make use of its support for standard diagnostic tools.

7 Experimental results from tests at CERN

7.1 Introduction

Data synchronization is an important aspect of the trigger and readout systems of the LHC experiments [42]. The design of the FE readout and L1 trigger there follows a synchronous pipeline model: the detector data are stored in pipeline buffers at LHC frequency, waiting for the L1 decision, while data from calorimeters and muon detectors are processed by a distributed, pipelined, tree-like processor that computes the L1 decision. The trigger system is based on the assumption that, at the input of every processing stage, data are synchronized and belong to the same bunch-crossing. The monitoring of the bunch number of trigger data flowing in the trigger pipeline is of the greatest importance. The system operates with a single clock frequency, the LHC frequency.

Despite the use of test data and other non-beam synchronization procedures, the only way to be sure about the trigger and detectors readout synchronization is to use the detector data themselves. Therefore, the test of the synchronization procedures can only be done with a particle beam that has a bunch structure similar to that of the LHC, capable of inducing signals in the CMS prototype detectors with a time structure similar to what will happen at the LHC.

7.2 Results from the October 2001 tests

7.2.1 Purpose of the tests

During October 2001, the prototypes of RPCs, FEBs, LB, and TB were tested at the CERN GIF (gamma irradiation facility) beam site. The Super Proton Synchrotron (SPS) accelerator was run in a special synchronous 40.08 MHz mode imitating LHC operation, and the clock was distributed to the sites using modules especially developed for this purpose.

The LHC-like beam was available in the X5 experimental area at CERN, where the RPC trigger system, equipped with prototypes of the readout electronics very close to the final designs, was tested.

A prototype link with a reduced functionality link board (LBrf) and on-line monitoring software was built for the test-beam experiments and the main focus was on the synchronization and diagnostics features of the LB.

The main aim of these tests was to study the behaviour of all prototypes in conditions similar to those expected in the final experiment.

7.2.2 The gamma irradiation facility area

This facility is a test area in which large high-energy particle detectors are exposed to a particle beam in the presence of an adjustable high-background flux of photons, simulating the background conditions that these detectors will suffer in their operating environment at the LHC. The GIF is situated in the SPS West Area, at the downstream end of the X5 test beam. The zone is surrounded by a concrete wall, 8 m high and 80 cm thick. A schematic layout of the GIF zone is shown in Fig. 59. The photons are produced by a strong radioactive source, which is installed in the upstream part of the zone, 5 m away from the end, and housed inside a lead container, which includes a precisely shaped collimator, designed to permit irradiation of a 6 m × 6 m area at 5 m distance from the source. A thin lens-shaped lead filter, mounted at the exit face of the source housing, renders the outcoming flux uniform in the vertical plane, orthogonal to the beam direction.

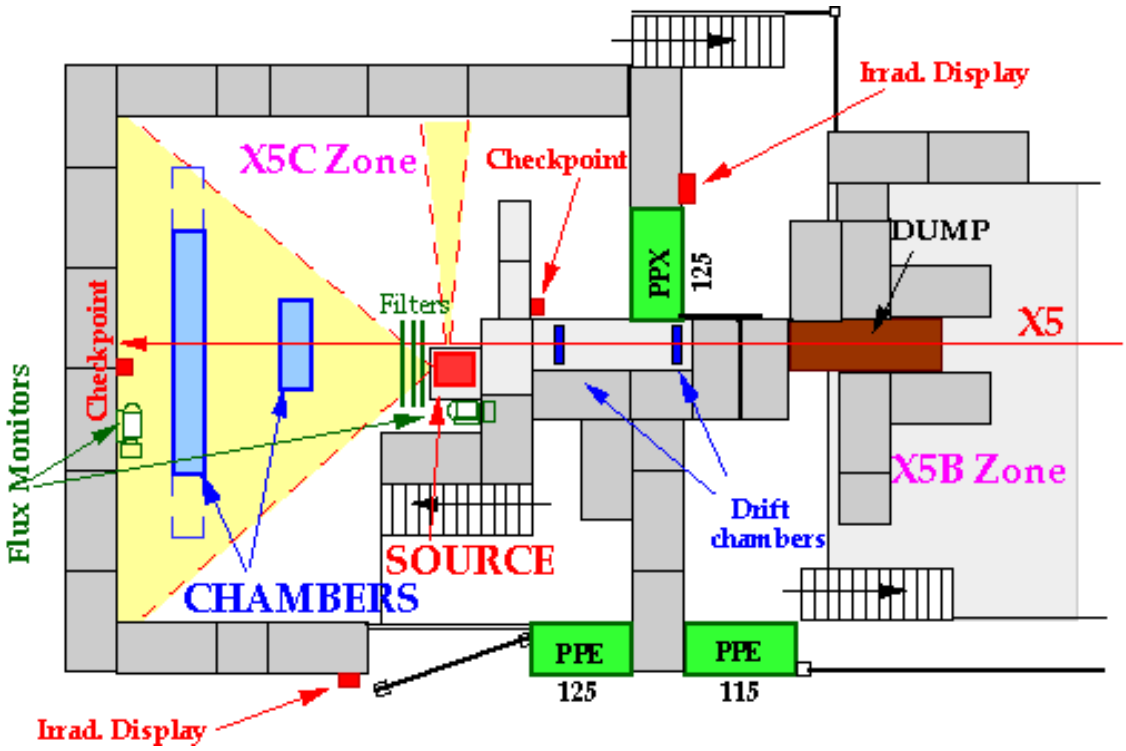


Figure 59 Schematic layout of the GIF zone

7.2.3 Description of the experimental set-up

.
From the RPC side, four different preproduction RPC detectors were tested: one medium chamber (with 2 bigaps, each one of dimensions 2500 × 130 cm^2) and three small chambers (with 1 bigap and dimensions 50 × 50 cm^2). The medium chamber was equipped with two rows of six FEBs each, the small chambers with 30 strips and 15 strips respectively[1].
The FEBs were connected to the reduced-functionality LB (LBrf) prototype via 20 m of standard-quality twisted-pair flat cable.
The LBrf used in the test was a 6U VME module having three Altera ACEX series FPGAs, several LVDS interfaces and mezzanine connectors for a fibre-optic link interface and an interface card for receiving the accelerator clock. This LB prototype is called 'reduced-functionality LB' since it lacks some features that will be needed on the final board.
The data transmission from the FEBs (located on the RPC detectors) to the LBs was in LVDS instead of fibre-optic link, since the time available for the tests was very short. The LBrf reading out the detectors was first connected to another LBrf, then to a TB prototype.
The FPGAs were loaded through the VME bus using an SBS VME-PCI interface. The software for controlling this process, for setting options on the LBrf and for reading out the information from it was written in the C++ language, complete with an intuitive graphical user interface (GUI). The software was developed in parallel with the VHDL codes, including synchronization of the FEB data to the TTC clock (or to an on-board oscillator for stand-alone laboratory set up), building of histograms from these data and a compression algorithm for the data transmission [43].
The distribution of clock, trigger and fast signals is performed by the TTC network, by using two time-division-multiplexed channels transmitted over an optical passive distribution network. Channel A (Fig. 60) is used to transmit the L1A signal, whereas channel B transmits other fast commands. Both channels have a bandwidth of 40 Mbits/s.
The top elements of each partition are the TTCvi and the TTCex modules. The TTCvi propagates the L1A and distributes various types of programmable commands. The TTCex module encodes both channels A and B from the TTCvi.
The clock from the TTCmi crate is plugged directly into the TTCex modules. At reception, optical receivers with a pin diode and an amplifier generate an electrical signal at the TTCrx chip input. The TTCrx chip provides at its output the 40 MHz LHC clock, the L1A Accept (L1A) trigger and fast commands data.
Fig. 61 shows the system layout including the optical part, represented by the GOL (Giga Optical Link) chip.

[1] Private communication from F. Loddo, RPC group, University of Bari.

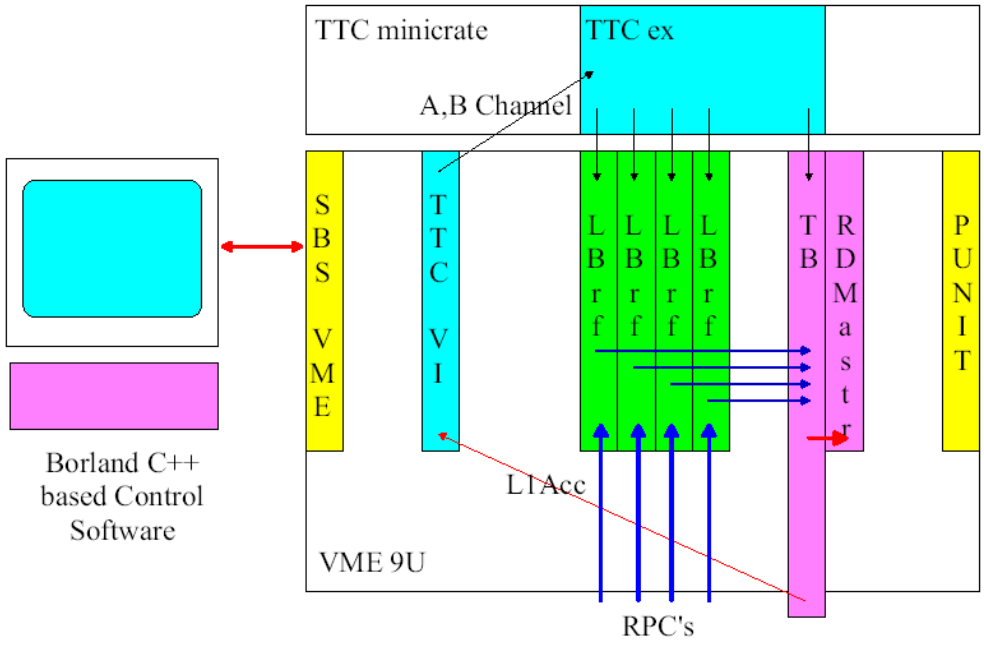


Figure 60 The experimental test set-up scheme

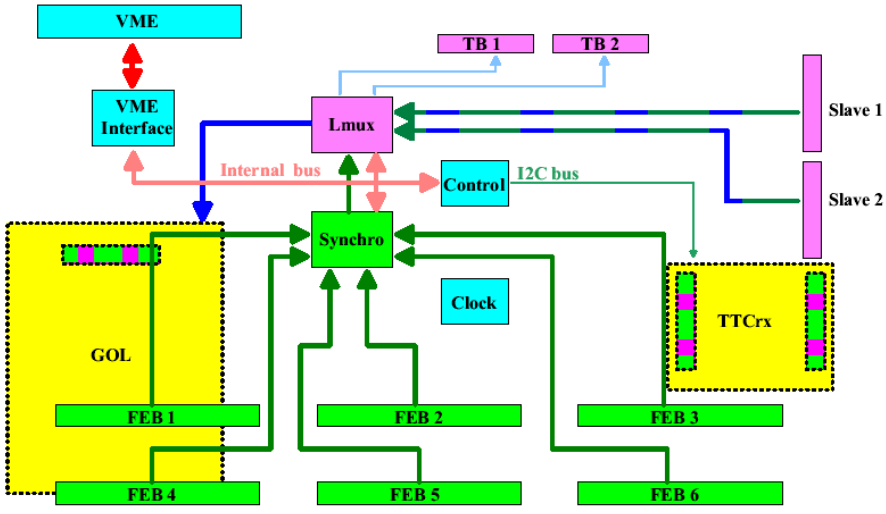


Figure 61 System layout including the optical part

7.2.4 Results

The following Figs. 62 to 64 show the signals obtained during these October 2001 tests for different chambers.

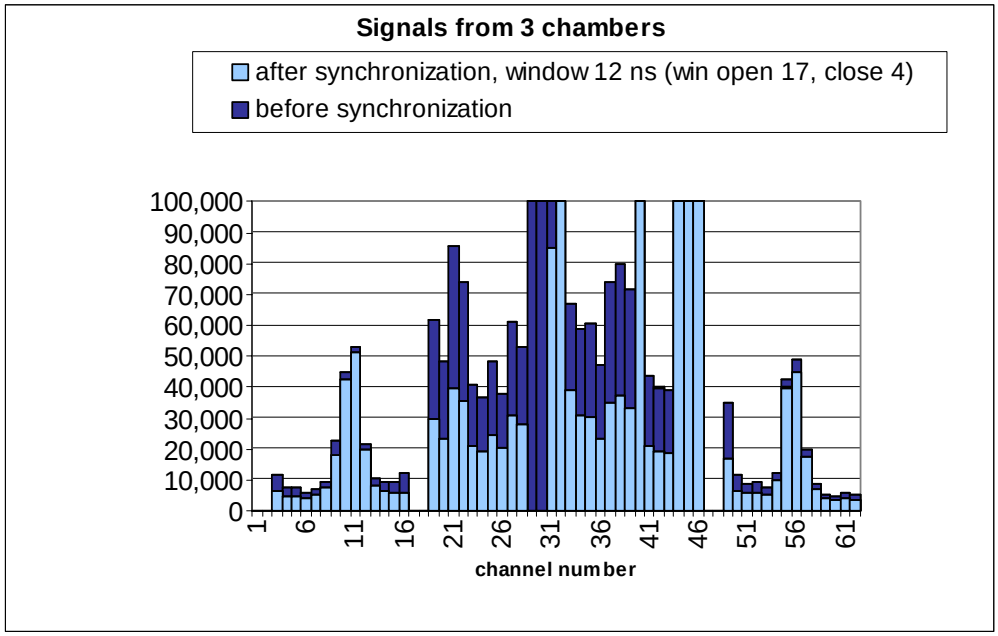
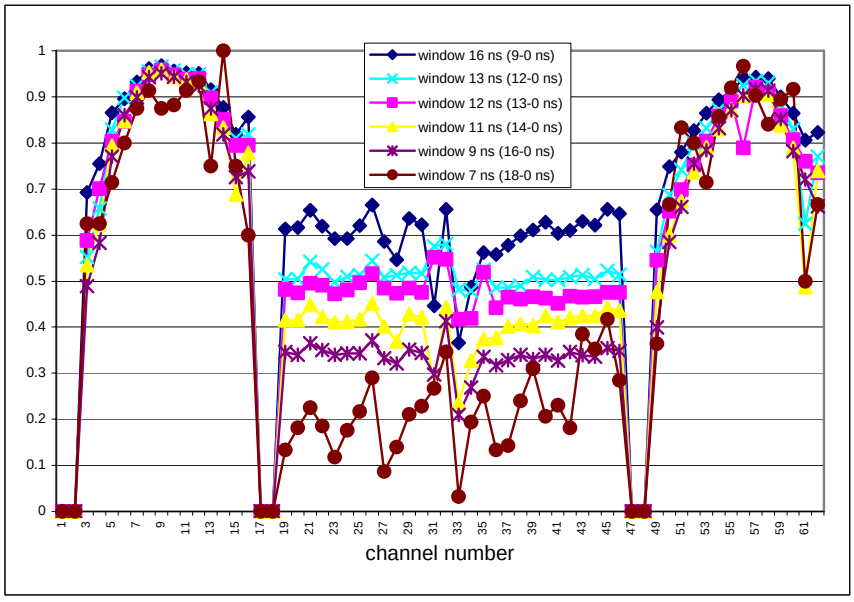


Figure 62 Signal from the different chambers during one SPS cycle (17 s)

In Fig. 62 we can see the profile of the three different chambers used during the test: on the left side there are signals coming from the small chamber, in the middle signals coming from the medium chamber and on the right signals coming from the other small chamber.

The beam had a width of 4–5 strips in the middle of the chambers. Signals on the edges of chambers came from noise, clusters and streamers.



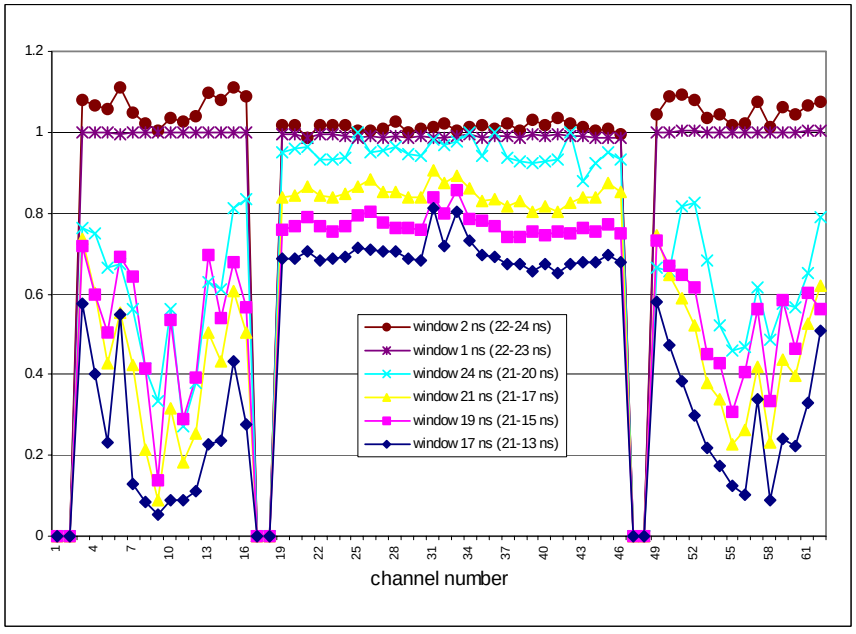
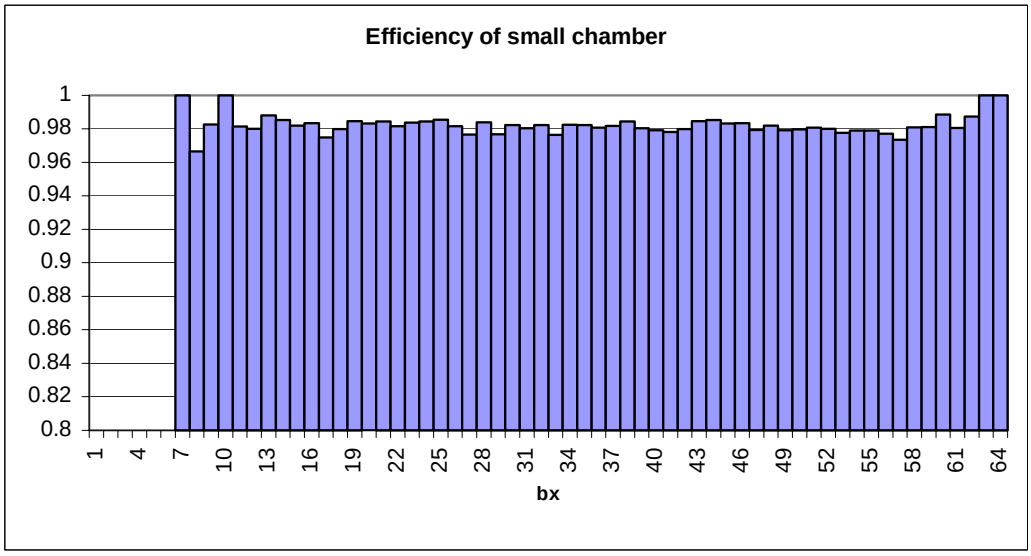


Figure 63 Results of synchronization efficiency tests with different window lengths

Figure 63 shows the synchronization efficiency for different widths and positions of the same window. In the upper part of the diagram we can see the beam inside the time window; in the lower part the beam is outside it. In some cases, we found the efficiency for the chamber larger than 1: this effect was due to an improper synchronization, by which some events were counted twice.



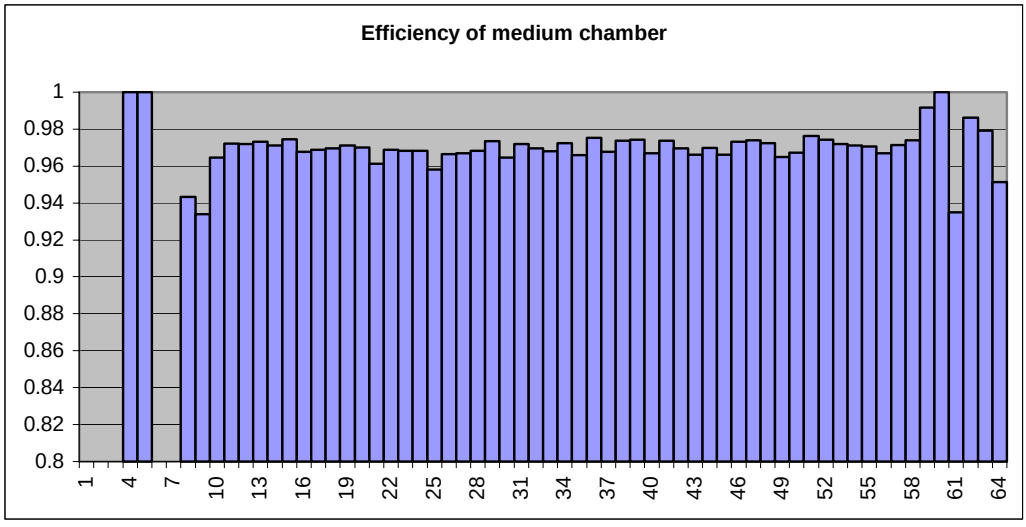


Figure 64 Efficiency of small and medium chambers

Figure 64 shows the efficiency of the small and medium chambers. In both cases, this was calculated as the ratio of the histogram of coincidence of three chambers to that of the other two. For example, if we call the tested chambers as ‘small 1’, ‘medium’ and ‘small 3’, the efficiency of the chamber ‘small 1’ was calculated as the ratio of the histograms of coincidence of the three chambers over the histograms for medium chamber and small 3 chamber.
In Fig. 65 we report the number of hits in the strips of three chambers during one SPS cycle (17 s) in three different situations: with no beam, with a poor beam and with a normal beam. The first histogram was taken during the SPS cycle without muon beam. It can be seen that the chambers noise is very small: few hits per channel in the small chambers and few tens of hits in the medium chamber (except for a few very noisy channels). The second histogram was taken during a cycle with a poor muon beam (few thousands of muons). In the medium chamber it is possible to recognize the beam profile and the number of hits in the edge channels. In the third histogram, taken during the cycle with a normal, high-intensity beam (few tens of thousands of muons), it is hard to recognize the beam profile in the chamber[2]. One can also notice that there are many more hits on the edges of small chambers than in the case of the pure beam [44].

[2] Private communication from K. Bunkowski, University of Warsaw, Poland

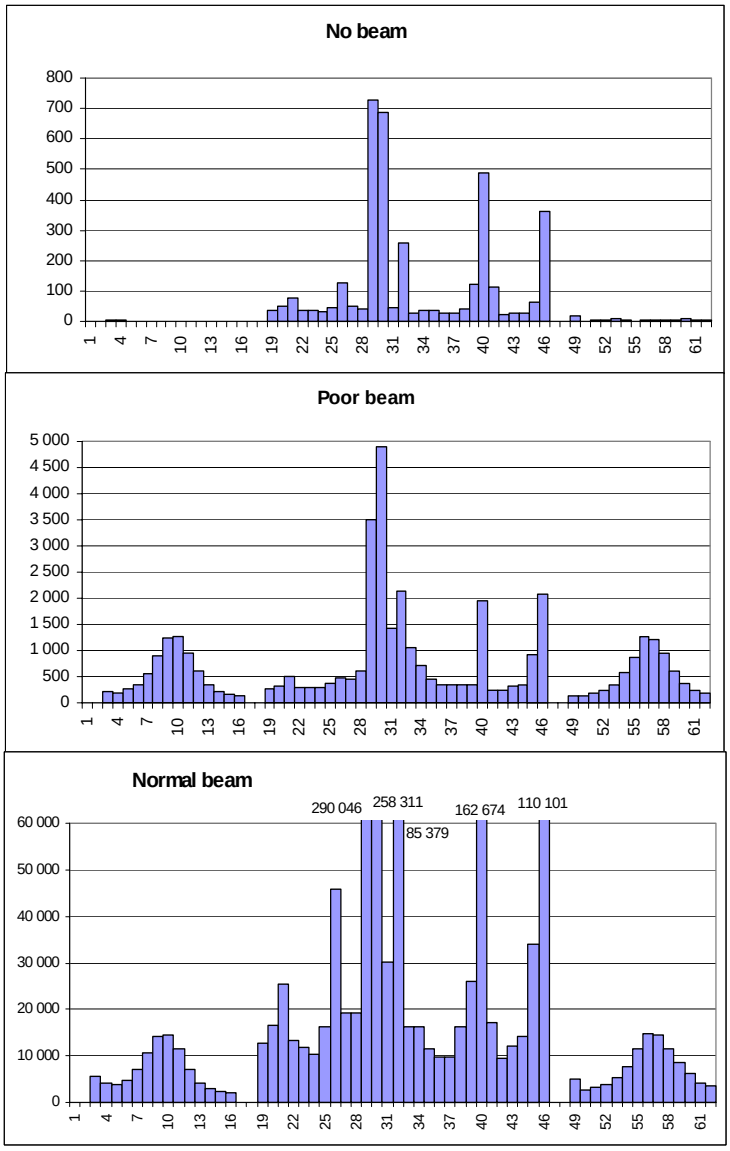


Figure 65 Number of hits in strips for three chambers in different beam conditions

7.2.5 Conclusions

The main task of these tests was to evaluate the quality of the signal received from the RPCs.
Looking at the results we can conclude that no problems were observed in the signal quality, which was a surprisingly positive result. Also, the synchronization algorithm developed for one of the LB FPGAs gave very good results. Concerning the functionality of the RPCs during the tests, the synchronization was found to be easy in the SPS muon beam with oiled RPCs. Testing of the FEB–LB interface was very important since it has been shown that several important modifications had to be implemented on the FEB and LB, related to the I^2C control and the grounding scheme. These modifications were tested later, as described in sections 7.3 and 7.4.

7.3 Results from the May 2003 tests

7.3.1 Purpose of the tests

The second 25 ns synchronous beam tests were done at CERN in May 2003. The aim of the test was to analyse the performance of the RPCs under a flux of muons, and the behaviour of the new readout electronics connected to the chambers.

Figure 66 Structure of the test beam time

The test was performed in a synchronous, 25 ns, LHC-like, muon or pion beam. The muon beam spot at the RPC surface had a diameter of about 10 cm, and there were usually about 1000 particles per spill. The pion beam was larger, and its intensity was a few thousand particles per spill. The structure of the test beam time used during the test is shown in Fig. 66.

7.3.2 Description of experimental set-up and software tools

From the RPC side, the set-up consisted, as shown in Fig. 67 and Fig. 68, of chambers of four different sizes in the irradiation area, six TDC (time-to-digital converter) modules and one computer (for data acquisition) in the CMS Control Room. The properties of the RPCs during the tests were as shown in Table 9.

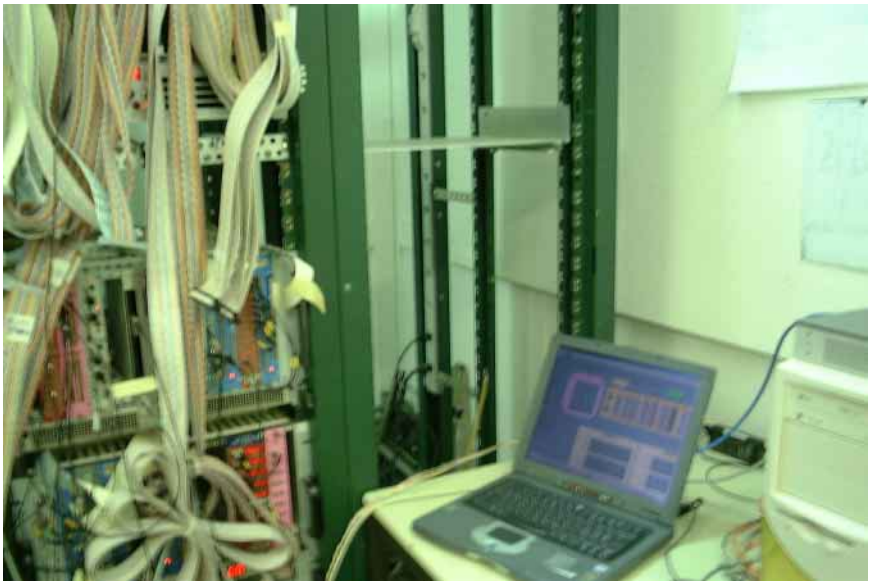


Figure 67 The RPC set-up in the CMS Control Room

	RB3		RB3		RB1		RB2	
Strips width	3.5 cm		3.5 cm		2.27 cm		2.93 cm	
Strips length	124 cm		124 cm		125 cm		125 cm	
Front–end boards channels	FEB 1		FEB 1		FEB 3		FEB 4	
	0 1 : 14 15	not connected connected not connected	0 1 : 14 15	not connected connected not connected	0 1 : 14	not conn. conn.	0 1 2 : 15	not conn. not conn. connected
	FEB 2		FEB 2		FEB 4		FEB 5	
	16 17 : 30 31	not connected connected not connected	16 17 : 30 31	not connected connected not connected	16 17 : 30 31	not conn. conn. not conn.	0 1 2 30 31	not conn. not conn. connected

Table 9 RPC properties: strip dimensions and connection of strips to the FEBs channels

Figure 68 Photograph of RPCs in the GIF area

In the FE electronics set-up we had two new LB prototypes (with Spartan IIE series chips instead of the Altera chips used in the previous prototypes) and one CB prototype (with the Flash memory tested in Jyväskylä) and the CCU chip implemented on the CB for the first time. LBs and CB were housed together in a VME crate (see Fig. 69). Each LB had 64 active input channels, and two RPCs were connected to each LB.

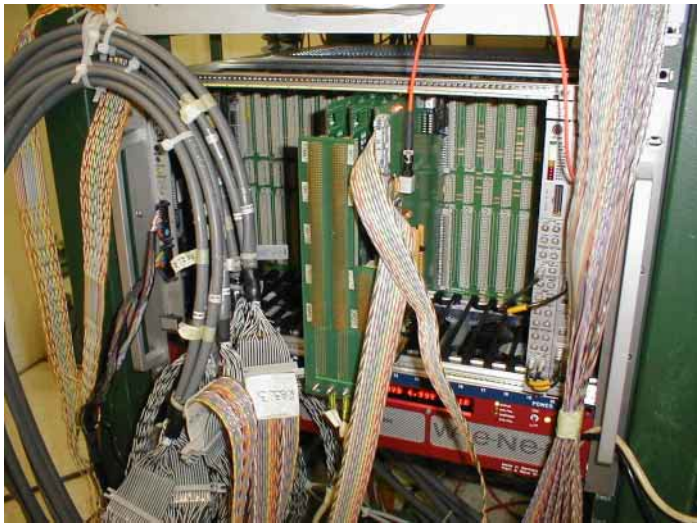


Figure 69 Photograph of LB and CB in the VME crate

Let us denote by RB1, RB2, RB3–43 and RB3–21 the four chambers, and with LB2 and LB3 the two LBs (see Fig. 70).
Chambers RB1 and RB2 were connected to LB3, while the two RB3 chambers were connected to LB2.
The LBs were connected to the TTC system by the TTCrx chip, located on the CB. The TTC provided a clock that was synchronous with the beam and the orbit signal that indicated the beginning of each train (proton bunches generally are grouped in 'trains'). The clock needed to perform the synchronization of the signal from the chambers ('window open' and 'window closed') was also provided by a TTCrx chip. The TTC signal L1A was used for sending the signals from the scintillators to the LB.
The CB and the LBs were controlled by C++ software. Two ways of communication with the boards were possible: by VME or CCU. During the test, VME control (SBS VME controller under Linux) was used. The CCU chip was electrically connected to PCI FEC driven by Linux. A remote process control (RPC) protocol was used. The CCU memory port interface was used to drive the CBC FPGA. This control was functioning and used for FPGA bit streams download (to the local LB memory) as well as for an access to the local backplane bus. Full speed of the memory port access (block mode) was not achieved, and the reason for this has yet to be investigated.

The control of the FPGA was performed via the local communication system internal interface, which is an integrated environment enabling automatic mapping of registers and memory addresses into software.
The graphical user interface of the control application enabled the setting of all parameters of the LBs and a real-time view of the histograms [45].

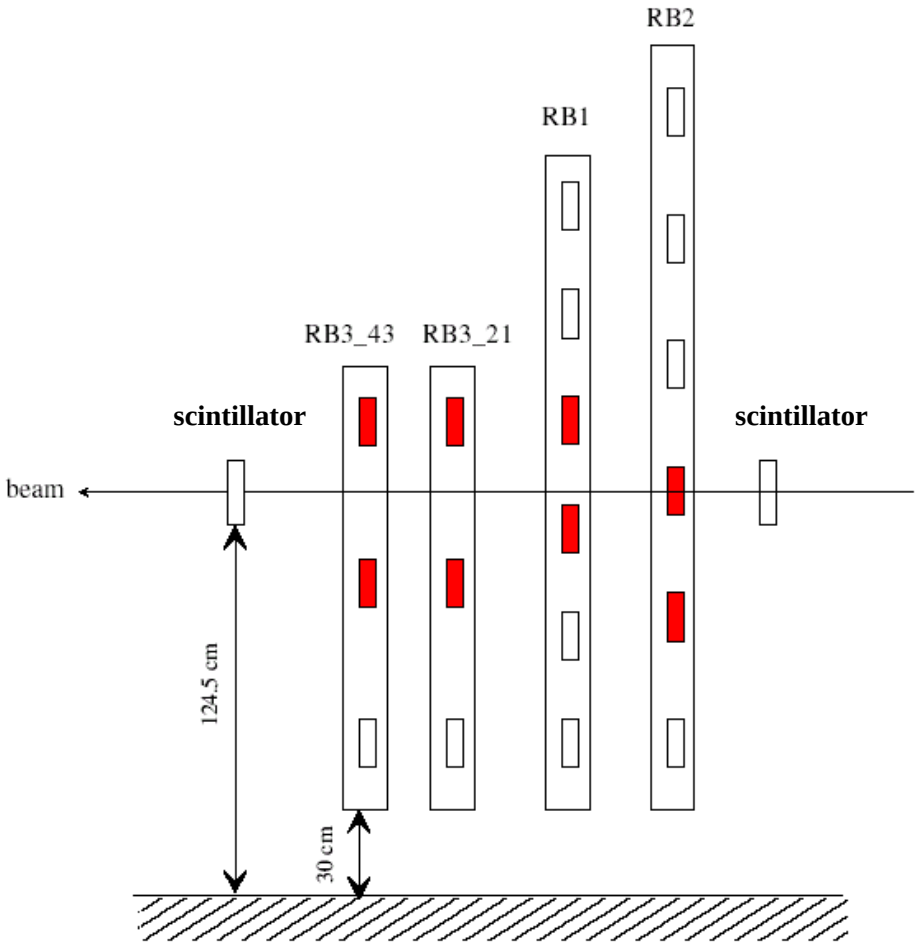


Figure 70 The layout of the RPCs during the tests. The red rectangles denote the FEBs connected to the LBs.

7.3.3 Functionalities of the test system

Five histograms were implemented on the LBs (see Fig. 71):

- One of signals in the synchronization window (count of the number of signals from chambers in the synchronization window for each channel);
- One of all signals from chambers (for each channel);
- One of the ratio of signals in the synchronization window to all signals (for each channel);
- One of 'bx history' (bunch-crossing history), which is the accumulated number of signals in consecutive 128 bx at the beginning of each orbit;
- One called 'snapshots', that is the history of 128 bunch crossings for each channel.

The LBs could histogram the signals that were in coincidence with an external trigger, e.g. that from the scintillator signals.
The signals from the chambers could be delayed by programmed intervals, this function being useful when synchronizing the chamber signals with the trigger one.
The snapshots enabled us to observe the position of the time edges, or lengths of the signals.
All histograms could be displayed by control application in two modes: showing the total number of signals from the beginning of the run, or showing the increment in a specified time interval (i.e. signals rate).

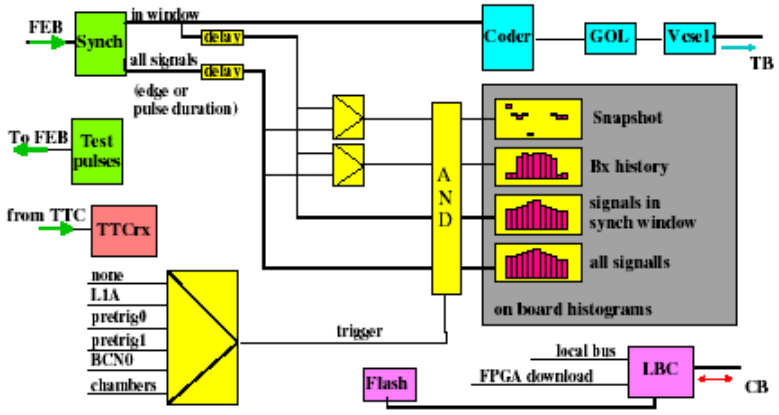


Figure 71 Link-board functionality

The application could perform the automatic runs by storing the data into files. During these runs the position of synchronizations clocks 'window open' and 'window closed' could be automatically changed in programmed steps.
The LBs sent test pulses to the FEBs (the number of test pulse signals was four times smaller than the number of input channels). The test pulse signals sent to the FEBs were triggered by test pulses from the LBs (one test pulse triggers four output FEB channels). This function enabled us to measure the skew of signals caused by FEBs and cables.
The test pulses could also be directly sent to the input channels of the LBs, by using special cables. This enables the measurement of the signals skew caused by the differences of path lengths on boards, and by routing the signals inside the FPGA.
During the test, the CB controlled the FEBs by way of an I^2C interface. Six CCU I^2C channels were used to drive 6 I^2C FEB chains. Each I^2C chain communicated with a FEB I^2C distribution box (controlling one RPC). CCU I^2C signals were buffered and converted to the LVDS levels (Philips buffer, P82B96 and LVDS converters 75LVDS387, 75LVDS386). The CB was able to access the FEB I^2C, but it was not able to realize word I^2C transfers, which is required by the FEB I^2C slaves (DACs). A possible solution investigated could be to move the I^2C master on the CB to the CBC FPGA.

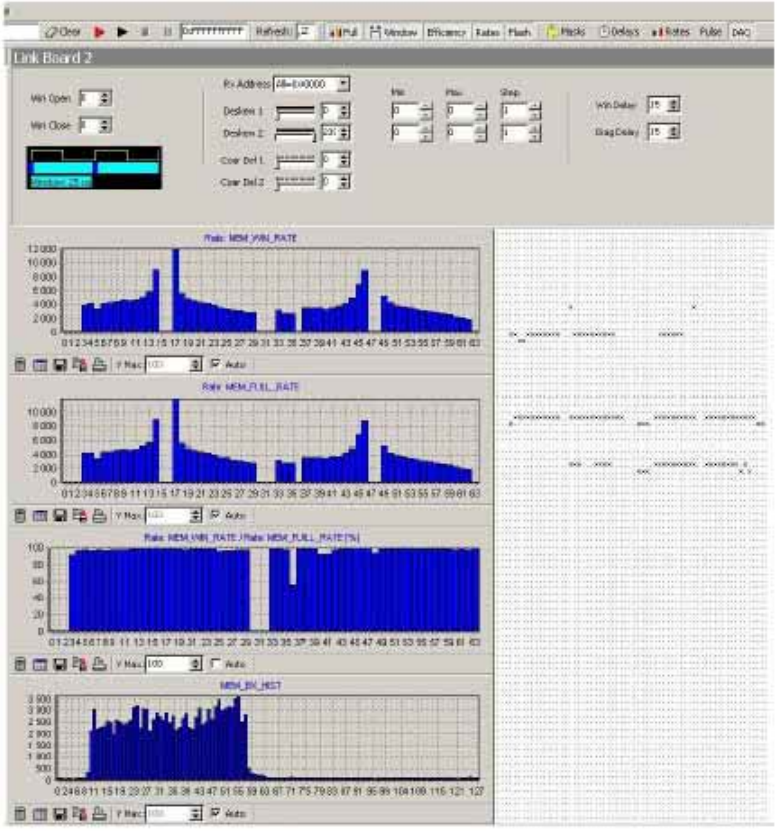


Figure 72 The screenshot of the control application main window

In Fig. 72, the first histogram from the top shows the signals in the synchronization window (it is possible to see two chambers, and the pion beam in the middle of each chamber). The second histogram represents all signals, while the third shows the ratio between the first two. Finally, in the last histogram the bx history can be seen.
On the right side of Fig. 72 is shown the 'snapshot' (the horizontal axis being the channel number, the vertical axis the bx number), the huge clusters and the streamers.
The lack of signals in channels 15 and 16 and 47 and 48 was due to the fact that the input channels of the FEBs (every FEB has 16 channels, all of them connected to the LB) were not connected to the strips.

7.3.4 Test results

The time position of the test pulses was measured by changing the delay of the 'window open' clock, when the signals appeared on the 'in window' histograms (see Fig. 73).

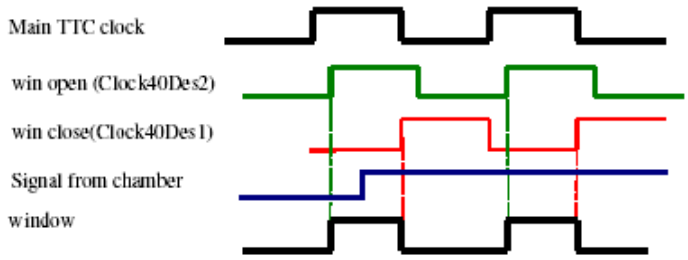


Figure 73 The synchronization of the signal from the chamber performed by the synchronizer circuit

Figure 74 shows the ratio of signals in the synchronization window to all test-pulse signals for different positions of the 'window open' clock (for one channel). This measurement shows the sharpness of the synchronization window edge for the LB2.

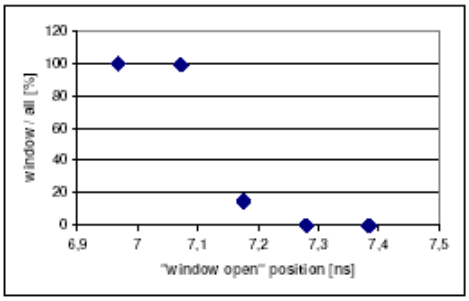


Figure 74 The ratio of signals in the synchronization window to all test-pulse signal

In Fig. 75, we can see one test-pulse signal directly connected to each input LB channel. The observed skew between channels is correlated with the length of the paths on the PCB from LVDS converters to the synchronizer chip on LB2.

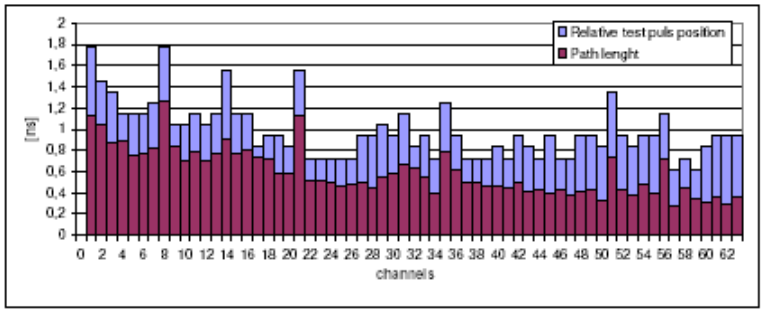


Figure 75 Test-pulse signal

Finally, Fig. 76 shows the time position of the test pulses received from the FEBs. In this case the observed skew between channels is the summary effect of LBs PCB paths length and properties of the cables and FEBs. The blue crosses show the mean of the four channels (four FEB channels were triggered by one test pulse from the LB).

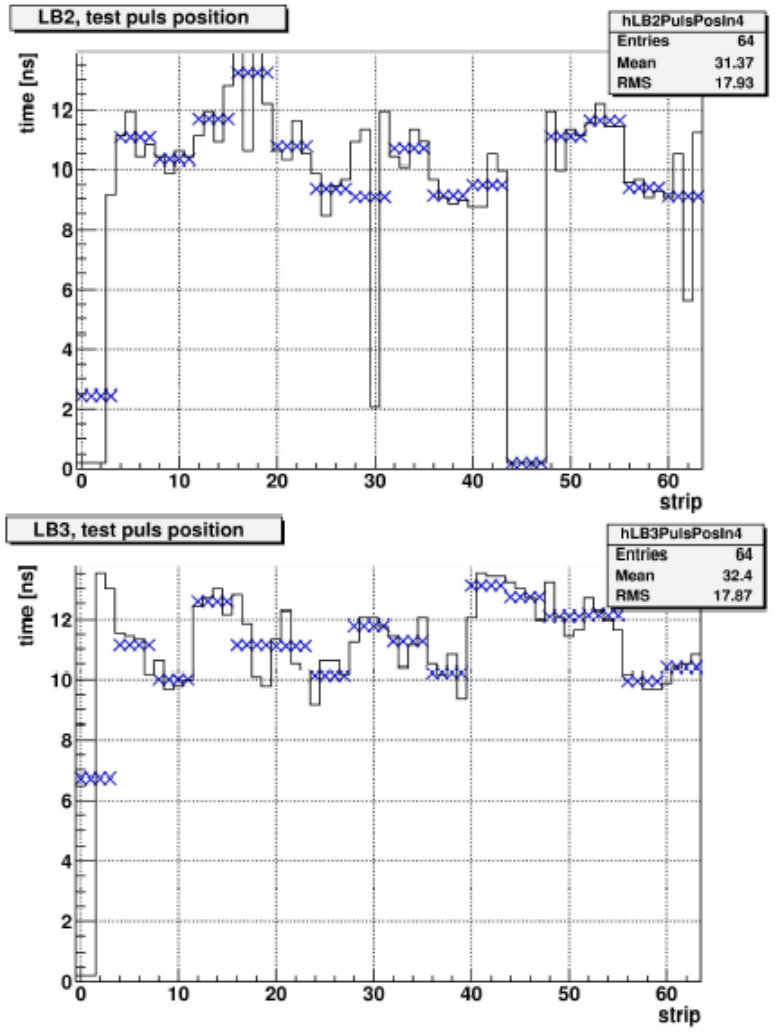


Figure 76 Time position of the test pulses received from the FEBs

The muon-beam profile is shown in Fig. 77: the profile on the left is related to LB2, while the one on the right is related to LB3.
The bunch-crossing history histogram can be seen in Fig. 78, where the train of 48 bunch crossings is shown. These data were taken in coincidence with a scintillator trigger.

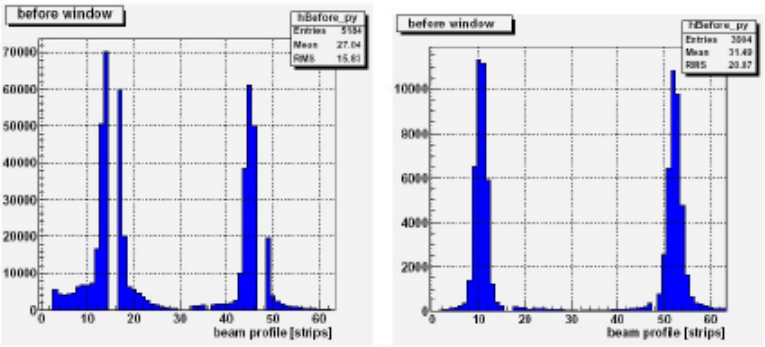


Figure 77 Muon-beam profile

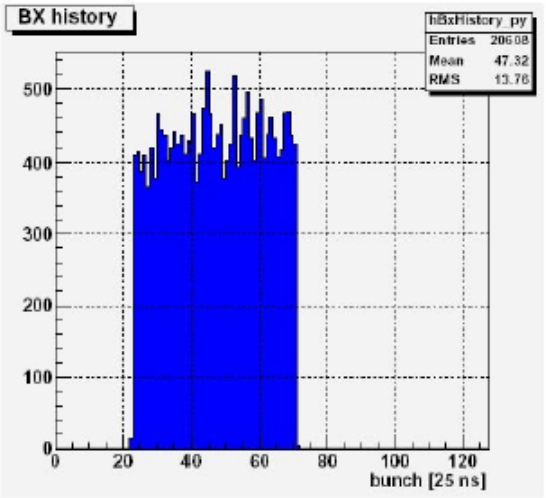


Figure 78 'bx history' histogram

Figure 79 and 80 show, respectively, the ratio of chamber-noise signals in the synchronization window to all signals measured without a beam (the ratio is proportional to the window width), and the beam-bunch time shape scanned with a 1 ns window.

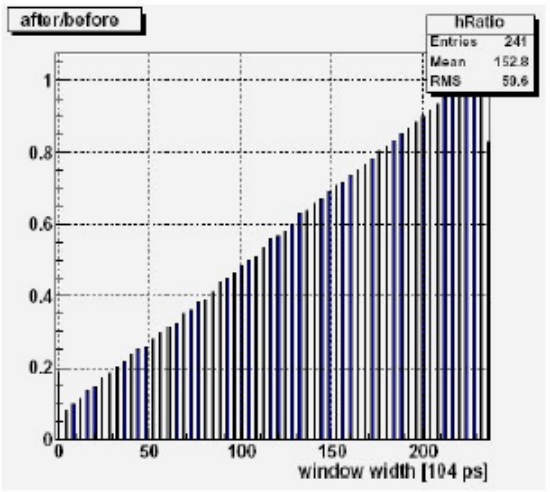


Figure 79 Chamber noise signals

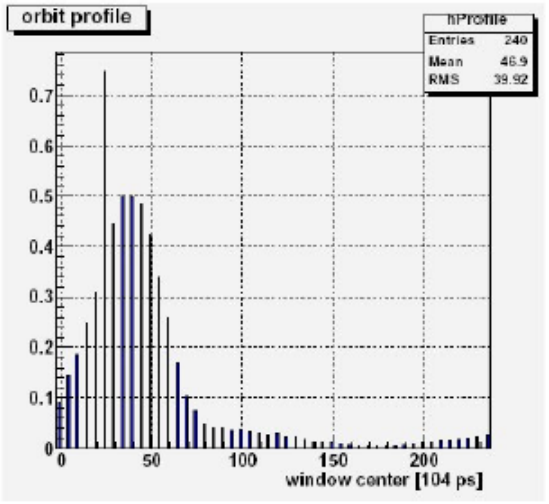


Figure 80 Beam-bunch time shape

7.4 Conclusions

As results of these tests, we can say that the histograms and snapshots have worked well and have proved their usefulness in testing the performance of the chambers. The synchronization of the signals from the chambers worked very well. The sharpness of the synchronization window edges is of the order of 30 ns (which is a sufficiently small

value). The window width is proportional to the difference of delays of ‘window open’ and ‘window closed’, as expected.
The skew of the test-pulses signals (~ 4 ns) is mainly caused by a skew of the test-pulses output. The differences of return-pulses position triggered by the same test pulse are 1–2 ns, which can be attributed to a skew caused by the cables.
It should be possible to reduce the skew of the input channels and the output of the test pulses by fixing the path length on a LB PCB.
After these improvements, the synchronization part of the project should meet the requirements.
All needed TTCrx signals were distributed correctly.
The CCU control of the backplane bus was functioning, but some improvement in the speed of block transfer has to be made.
CB CCU I^2C communication is working, but does not provide word I^2C transfer. The I^2C master on the CB must be moved from the CCU to the CBC FPGA.

8 Experimental results from the RPCs cosmic–ray tests at Bari University

8.1 Introduction

The RPCs are wireless parallel-plate detectors that will be used in the CMS experiment for the muon trigger system. One of them is shown in the photograph of Fig. 81. The RPCs combine good spatial resolution with an excellent time resolution and make the muon trigger capable of identifying a muon track, measure its transverse momentum, and relate it to the correct bunch-crossing.

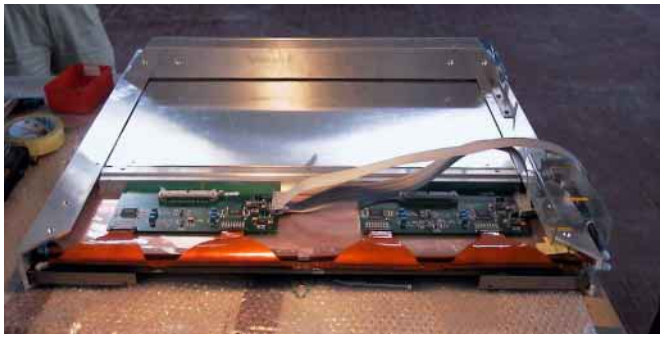


Figure 81 An RPC detector

To guarantee the good quality of the RPCs before sending them to CERN, a test procedure was developed at the University of Bari, Italy, to measure the performance of the produced detectors.
In this chapter the tests made for the barrel CMS RPCs will be described. A more detailed description of the procedure can be found in [46]. The RPCs that underwent the tests without showing a pathological behaviour were accepted to form the four-layers RPC trigger system of the central part of CMS. Before starting on the description of the experimental set–up and presenting the results of the tests, I will describe the CMS barrel RPC geometry [47].

8.2 The CMS barrel RPC geometry

A total number of 480 barrel RPCs have to be produced and tested for the CMS experiment. Depending on the layer of the trigger system, four different RPC stations are designed: RB1 and RB2 (the nearest to the beam pipe) and RB3 and RB4.

RB1 and RB2 consist of two double-gap layers denoted as *in* and *out*, depending on their distance from the beam pipe. Stations RB3 and RB4 contain only one double-gap layer. The technical characteristics of each kind of chamber are described below:

a) The chambers of station **RB1** consist of two double gaps named *forward* (FW) and *backward* (BW), held together by aluminium profiles. The overall dimensions of the RB1 chambers are 2080 × 2455 mm^2. The two subtypes of RB1 chambers (which we have denoted as *in* and *out*) have a strip length of 2080 mm. In particular, the 'RB1 *in'* has 90 readout strips while the 'RB1 *out*' has 84 strips. They will both have six FEBs per double gap, for a total of twelve FEBs per chamber.

b) The chambers of station **RB2** (also denoted as subtype *in* and subtype *out*) have a strip length of 2500 mm, but a different number of strips. In particular, 'RB2 *in*' chambers have 90 strips per double gap, with a pitch of 273 mm, while the 'RB2 *out*' chambers have 84 strips per double gap, with a pitch of 29.33 mm. Each of the two RB2 chamber subtypes consists of either two (FW and BW, denoted as RB2–2) or three double gaps (FW, CE and BW, denoted as RB2–3). All RB2 chambers have six FEBs per double gap and total dimensions of 2500 × 2455 mm^2.

c) **RB3** chambers consist of two double gaps (FW and BW), each equipped with 42 strips that have a pitch of 34.8 mm and a length of 1500 mm. They have three FEBs per gap (i.e. six FEBs per chamber). The overall dimension of the RB3 is 1500 × 2455 mm^2.

d) The RPCs of the **RB4** station are subdivided into three types, each equipped with two double gaps (FW and BW). The dimensions (and characteristics) of the three types are: 1500 × 2455 mm^2 (with three FEBs per double gap and 36 strips), 2000 × 2455 mm^2 (with three FEBs per double gap and 48 strips), and 2500 × 2455 mm^2 (with 5 FEBs per double gap and 60 strips), respectively.

8.3 Description of the experimental set-up

The experimental area where the RPC detectors are tested and partially assembled is located in the Department of Physics of the University of Bari, Italy. Here a special hall has been set up to allow the operation of the chambers and the performance tests with cosmic rays to study the chambers efficiency, cluster size, noise rate and dark–current measurements. The hall of 250–m^2 area is equipped with a crane, a power supply system, a gas distribution, a data acquisition system and a meteo station. The temperature is kept as constant as possible by an air-conditioning system. All data are remotely monitored and acquired in the Control Room, which is located in the same experimental hall.
The test set-up consists of the following systems:

1) Trigger system. The muon-trigger system is based on two double layers of scintillators covering an area of up to 150 × 40 cm^2. Four scintillators (S1, S2, S3 and S4) were used during the tests: S1 and S2 were housed on the top of a metallic tower, S3 and S4 at the bottom of the same tower. They were connected to each other by a logical

AND. The RPCs were also situated in the metallic tower (see Fig. 82), which can accept up to 10 chambers, and were covered with metallic plates to decrease the noise coming from external sources. The trigger signal is formed by taking the logical AND of the scintillators.

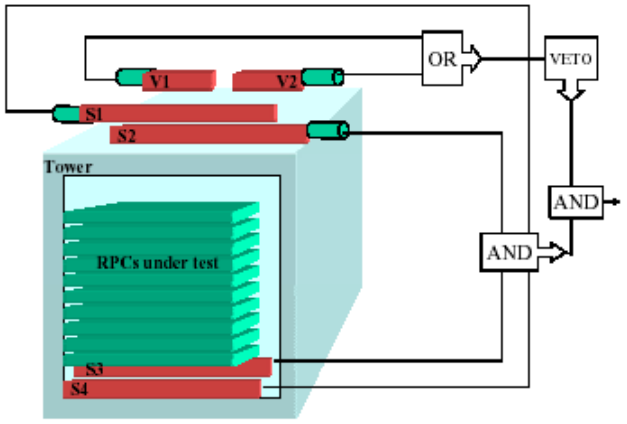


Figure 82 Trigger system scheme

2) High-voltage system. The HV power-supply distribution was based on the multichannel CAEN–SY1527 block, with internal processor and network connection. Dedicated software with graphical user interface was built to monitor and to record the values of the high–voltage channels. Each chamber (see Fig. 83) was served by two HV channels.

3) Data-acquisition system. This consisted of two VME crates connected by two VME extenders. On the crates, a total of thirty 64-channel TDC modules were mounted. Each TDC processed signals from four FEBs. An external 40 MHz clock pulse (emulating the 25 ns LHC bunch-crossing time) and the trigger pulses fed two master TDCs located in the crates, which distributed the signal to the other TDCs through the VME backplane. TDCs were programmed in the so-called ‘common-stop’ configuration, in which the trigger must be delayed with respect to the strips signals.

4) Gas System. A freon-based gas mixture was used during the data taking for the tests.

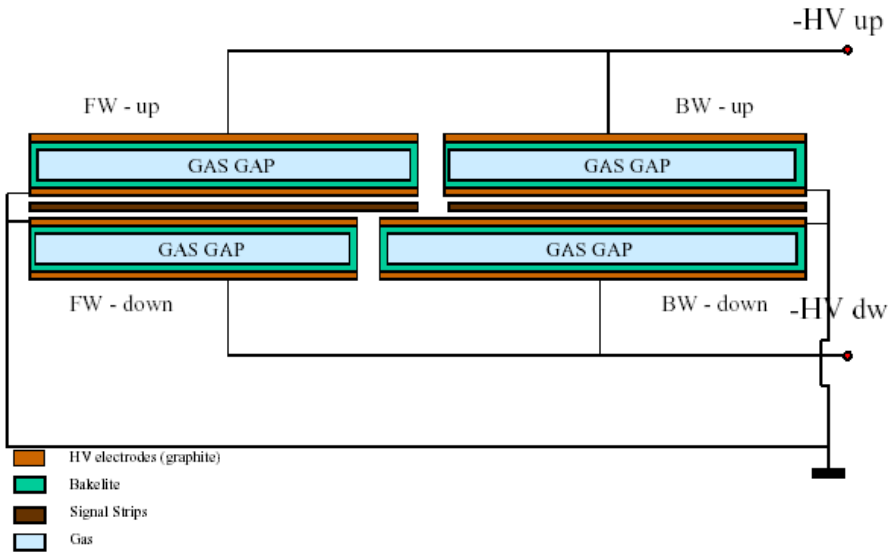


Figure 83 High-voltage supply diagram

Figure 84 Tower of RPCs in the experimental hall in Bari

8.4 Results

After the chambers were assembled, they were installed in the tower (Fig. 84) for the first experimental phase: the conditioning. The gas mixture is then flushed until the total gas volume is at least three times the chambers gas volume. The HV is then supplied increasingly, in steps of 1 kV, every 15 min. The first collection of muon data is used to detect mechanical or/and electrical problems (such as dead strips, disconnected cables, faulty FEB and grounding), so that they can be fixed immediately.
Data are then collected by aligning the chamber parts to the trigger system. About 150,000 triggers are taken for each chamber under test. The first set of runs is taken with both HV layers on, the second with only one layer on. Runs are taken at the nominal HV values of 9.2, 9.4, 9.6, 9.8 and 10 kV. These measurements are listed in Fig. 85.

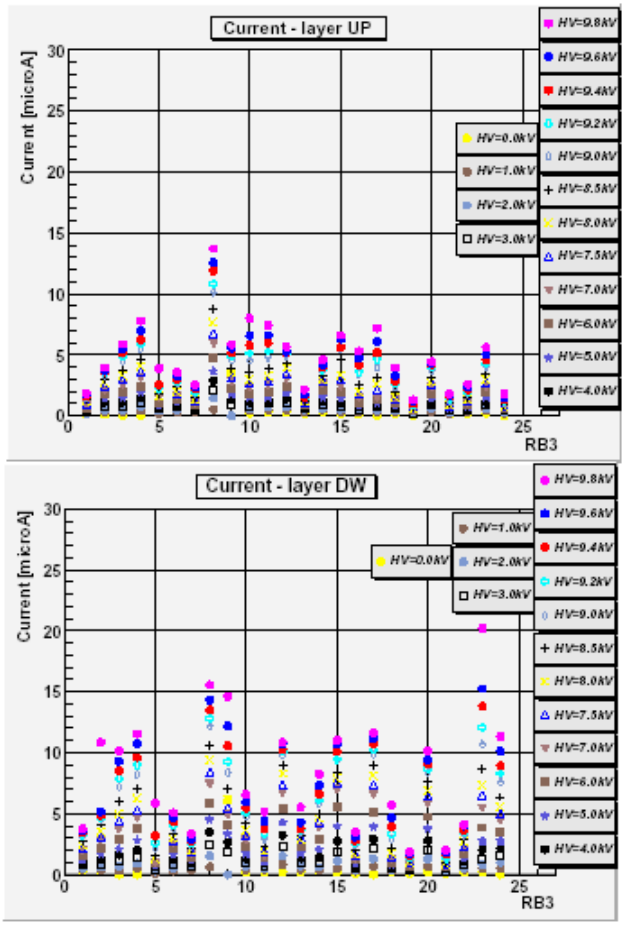


Figure 85 Currents in layers 'up' and 'down' measured for different values of the HV for 24 RB3 chamber channels

To get an optimal trigger performance, it is necessary to measure standard parameters with predefined theoretical values. For example, the efficiency ε is one of the most important parameters for the RPCs, and its value is required to be greater than 95% in an operating plateau of 300 V. Its evaluation is done from the events observed in a 100 ns time window in coincidence with a triggering muon.
In Fig. 86 the efficiency curves for a set of RB3 double-gap chambers tested are reported. The chambers reach 95% efficiency for a HV value of ~ 9.5 kV.
The distributions obtained for the first 24 RB3 chambers are shown in Fig. 87. The curves in Fig. 88 are typical efficiencies for the double-gap and the two single-gap operation modes of a chamber.

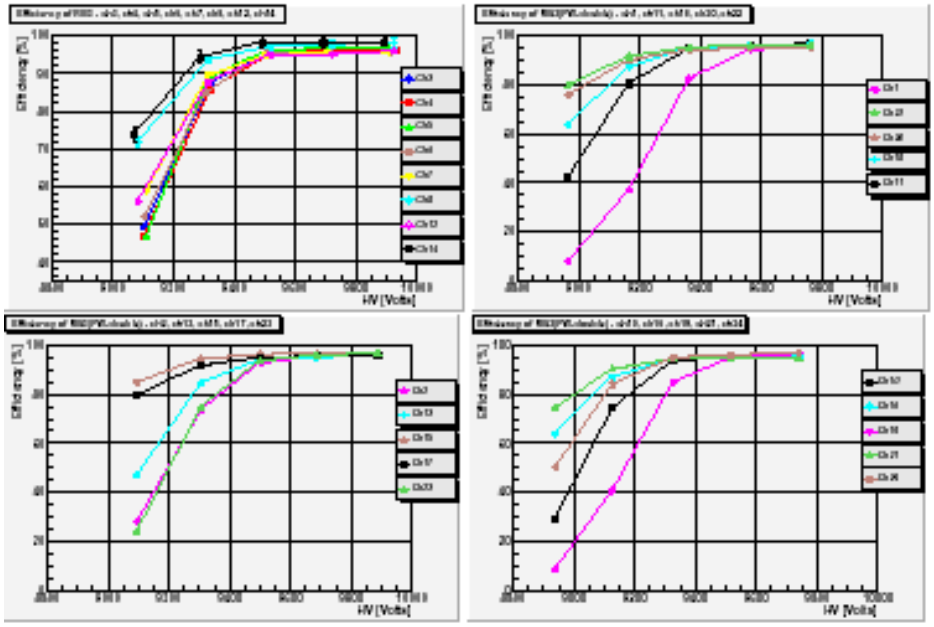


Figure 86 Double-gap efficiency of the FW part of the RB3 chambers

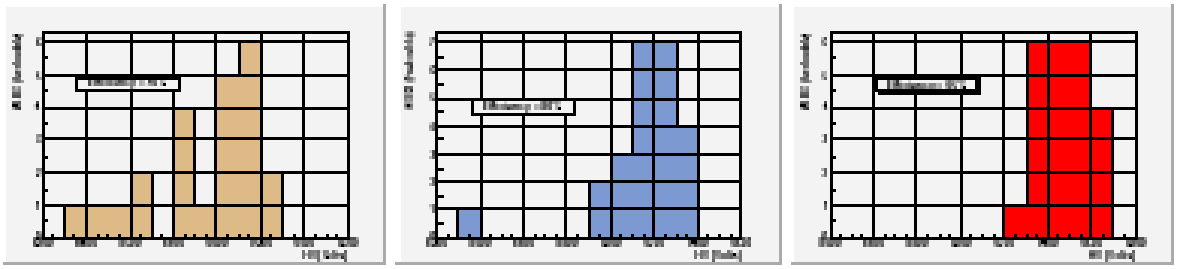


Figure 87 Distributions of the 50%, 80% and 95% efficiency voltage for the first 24 RB3 chambers

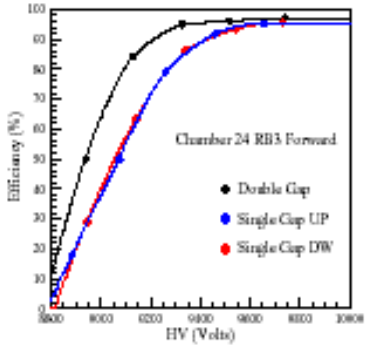


Figure 88 Typical efficiency curves for a chamber operated in different gap modes

A muon traversing the RPC fires strips that form clusters. The cluster size, defined as the number of adjacent strips in the cluster, determines the spatial resolution of the RPCs. When the average cluster size is ≤ 2 within the time gate of 25 ns, an optimal trigger performance is achieved.

Figures 89–91 present the average value of the cluster size as a function of the HV for RB3, RB2 and RB1 chambers, respectively.

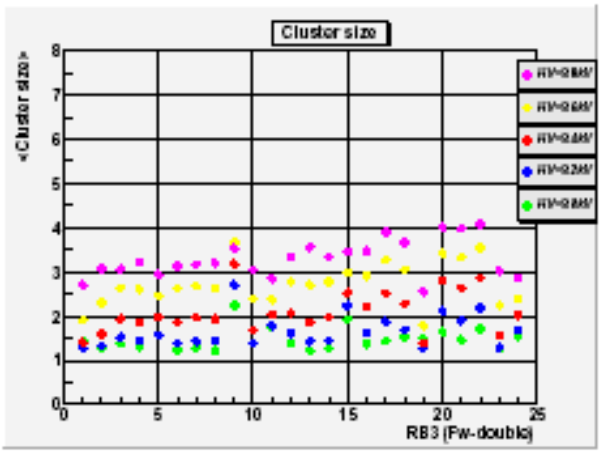


Figure 89 Cluster size of the first 24 RB3 chambers for different HV values

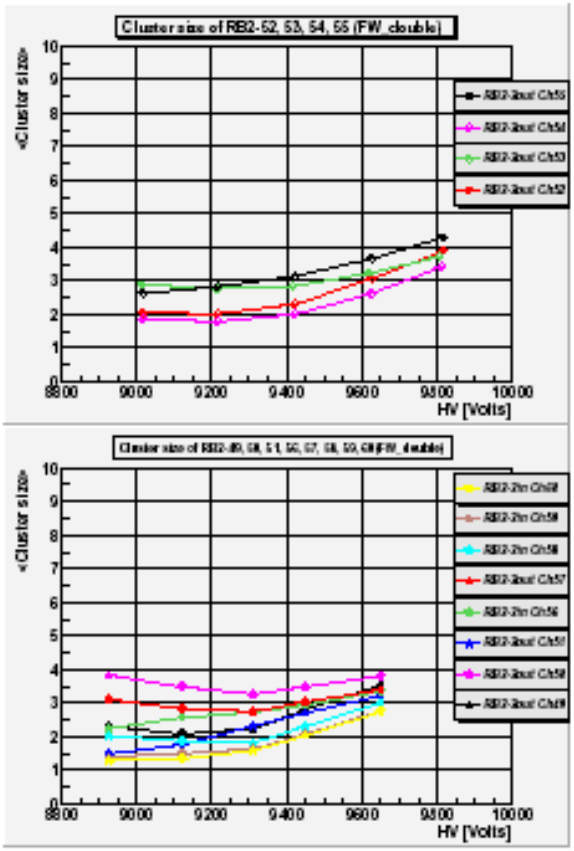


Figure 90 Cluster size of the first 24 RB2 chambers for different HV values

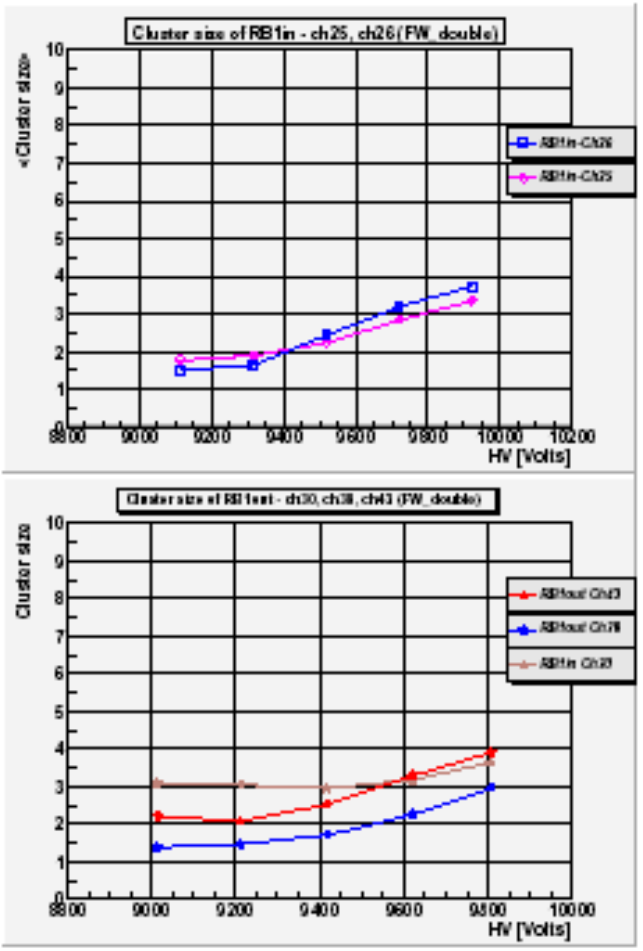


Figure 91 Cluster size of the first 24 RB1 chambers for different HV values

8.5 Conclusions

The values obtained on the tested RB chambers satisfy the requirements on the RPCs. The high efficiency and the good cluster size obtained from the tests show a chamber response that fully satisfies the CMS operation conditions. These chambers will therefore be brought to CERN for the final installation.

9 Experimental results from irradiation tests at the Jyväskylä Accelerator Laboratory

9.1 Introduction

The nominal luminosity of the LHC, 10^{34} cm^{-2} s^{-1}, together with the 7 TeV beam energy, will create a very hostile radiation environment, which all subdetectors will have to deal with. It has been known since the first LHC prestudies that the inner tracker and very forward calorimeters of the LHC experiments will be confronted with unprecedented radiation levels. The endcap calorimeters and the muon spectrometer will also suffer from the environment. In CMS, because of the strong solenoidal field and the massive iron yoke, the barrel calorimetry and barrel muon spectrometry are the subsystems least affected by background and radiation-damage effects.
The hostile radiation environment implies that a lot of attention has to be devoted to selecting sufficiently radiation-hard materials for all components.

9.2 The radiation environment in CMS

In addition to the physics requirements, the design of the various detector subsystems is also constrained by their operation in a high–radiation environment. Predicting particle fluences and doses at future hadron collider experiments is important for estimating:

a) The detector counting rates or occupancies (determined by convolving the predicted particle energy spectra with detector–sensitivity functions);
b) The radiation damage to detectors and electronics;
c) Single-event upset (SEU) phenomena in the electronics.

In Figs. 92 and 93, we show the particle fluxes and spectra (known from previous simulations) in the regions where boxes containing LBs and CBs will be placed.

Particle type	ME1/1–HE/1	Cavern above endcap
Charged hadrons (protons) (E = 10–100 MeV)	3.6×10^1 cm^{-2} s^{-1}	1.6 cm^{-2} s^{-1}
Neutrons E > 20 MeV	1.1×10^3 cm^{-2} s^{-1}	84 cm^{-2} s^{-1}
Neutrons E = 2–20 MeV	7.2×10^2 cm^{-2} s^{-1}	93 cm^{-2} s^{-1}
Neutrons E > 100 keV	4.4×10^3 cm^{-2} s^{-1}	370 cm^{-2} s^{-1}
Neutrons E < 100 keV	1.1×10^4 cm^{-2} s^{-1}	650 cm^{-2} s^{-1}
Neutrons total	1.7×10^4 cm^{-2} s^{-1}	1100 cm^{-2} s^{-1}

Table 10 Particle fluxes in the regions of the CMS detector set-up where the LBxs will be placed

As we can see from Table 10, the majority of particles are low-energy neutrons. From the point of view of their influence on the electronic devices, high-energy neutrons (E > 20 MeV) are very similar to protons. At these energies strong interactions with nucleons are very important. Therefore proton-beam tests of radiation effects give a very good prediction of the influence of the high-energy neutrons on electronic components in CMS.

Low-energy neutrons are copiously produced in the nuclear laboratories by a scattering of protons or deuterons on low-atomic-mass nuclei targets.

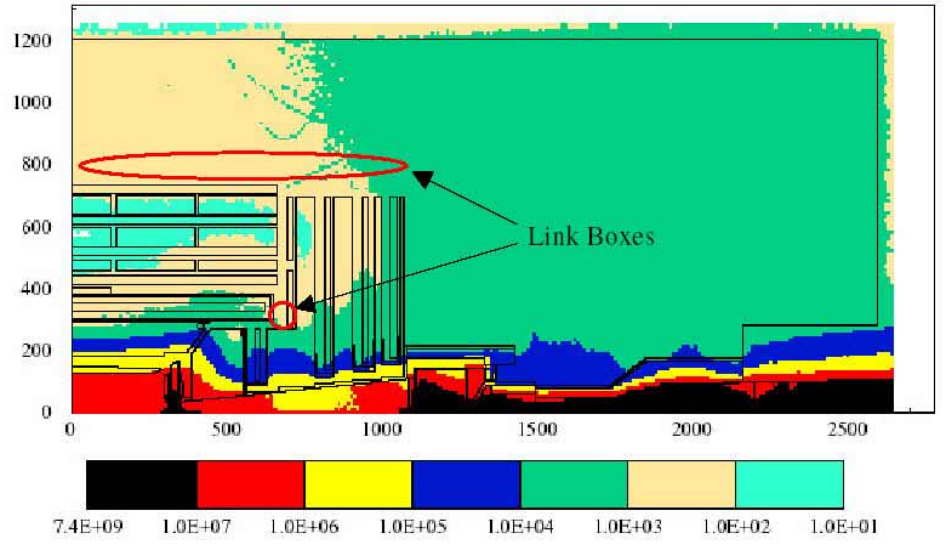


Figure 92 General overview of neutron fluxes in the CMS area (values given in cm^2/s at the LHC peak luminosity)

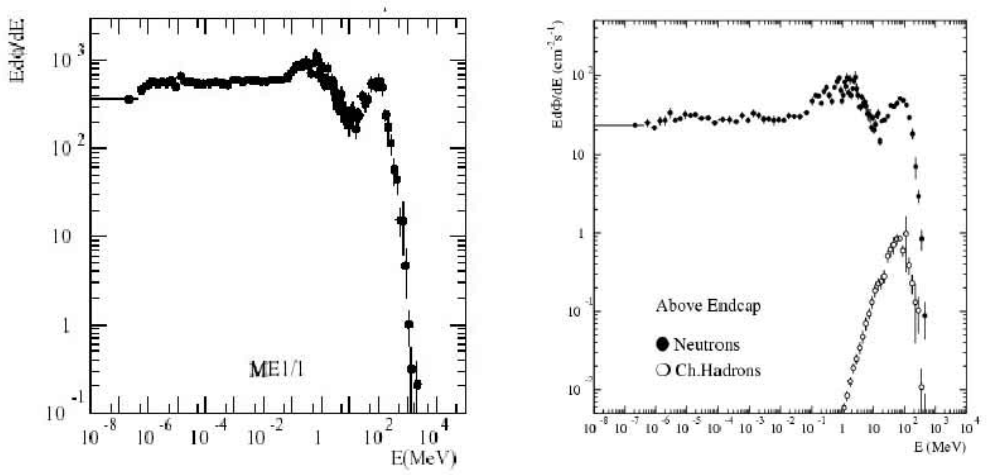


Figure 93 Neutrons and charged hadrons energy spectra

In the RPC trigger electronic system, LBs and CBs will be placed in the CMS cavern, mostly on the detector surface, some inside endcaps, between muon station ME1/1 and the hadron calorimeter HE/1. These boards will be in a radiation field composed mainly of thermal neutrons and high-energy hadrons (E = 10–100 MeV).
The most important electronic devices used on these boards are FPGA chips and memories that will store the FPGAs configuration data. The goal of the irradiation tests, performed at the Jyväskylä Laboratory irradiation facility and described in this chapter, was to predict the behaviour of this electronics in the radiation environment, and to find methods for error mitigation.
Before introducing the tests method and results, I will give a description of possible damaging effects on commercial components and discuss the SEU phenomenon.

9.3 Radiation-damage effects on commercial components

Radiation effects on electronic devices can be divided in two main categories: cumulative effects and single-event effects (SEE). Both categories are shown in Fig. 94.
The cumulative effects are due to the creation or activation of microscopic defects in the device, and they can be divided in total ionizing dose (TID) and displacement damage [48].

9.3.1 Cumulative effects

1) Total ionizing dose (TID): TID effects on modern integrated circuits cause the threshold voltage of MOS transistors to be altered by trapped charges in the silicon dioxide gate insulator. For submicron devices, these trapped charges can potentially 'escape' by tunnelling effects. Leakage currents are also generated at the edge of (N)MOS transistors and potentially between neighbours *n*-type diffusions. Commercial digital CMOS processors can normally stand a few krad without any significant increase in power consumption. Modern submicron technologies tend to be more resistant to total dose effects than older technologies (in some cases up to several hundred krad). High performance analog devices (e.g. amplifiers, ADC, DAC) may be affected at quite low doses. The total dose is measured in rad or gray (1 gy = 100 rad).

2) Displacement damage: Hadrons may displace atoms (whence the expression displacement effect) in the silicon lattice of active devices and thereby affect their functioning. Bipolar devices and especially optical devices (e.g. lasers, LEDs, optical receivers, opto-couplers) may be very sensitive to this effect. CMOS integrated circuits are normally not considered to suffer degradation by displacement damage. The total effect of different types of hadrons at different energies is normalized to 1 MeV neutrons using the NIEL (non-ionizing energy loss) equivalent.

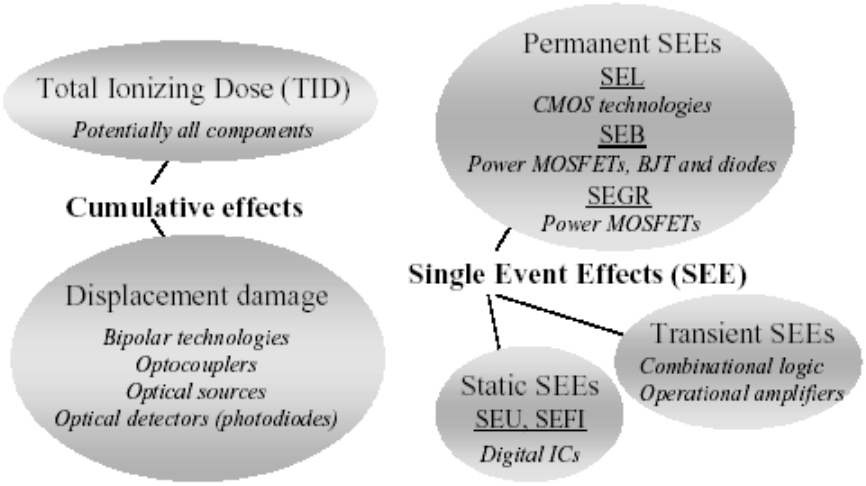


Figure 94 Summary of radiation effects

9.3.2 Single-event effects

SEEs are instead due to the direct ionization of a single particle, able to deposit sufficient energy in ionization processes to disturb the operation of the device.

1) Single-event latchup (SEL): Bulk CMOS technologies (not silicon on insulator) have parasitic bipolar transistors that can be triggered by a locally deposited charge to generate a kind of short circuit between power supply and ground. CMOS processes are made to prevent this from occurring under normal operating conditions, but a local charge deposition from a traversing particle may potentially trigger this effect. SEL may be limited to a small region or may propagate, thus affecting large parts of the chip. The large currents caused by this short-circuit effect can permanently damage the components if they are not externally protected against the large short-circuit current and the related power dissipation.

2) Single-event burnout (SEB): SEB refers to destructive failures of power MOSFETs in high-power applications. For experimental physics applications this failure mechanism is normally associated to failures in the main switching transistors of switching mode power supplies.

3) Single-event upset (SEU) corresponds to a soft error (data corruption) appearing in a device because of the energy deposited in the silicon by an ionizing particle. The SEU phenomenon will be discussed in detail in the next section.

9.4 Single-event upset phenomenon

In the very hostile environment created by the LHC, a SEU could become an important issue. It is a well-established fact that a SEU is caused by a very high energy deposition in a small volume of the electronics chip. The charge released along the ionizing particle path, or at least a fraction of it, is collected at one of the microcircuit nodes, and the resulting transient current might generate a SEU. The most sensitive regions of a microelectronic device are the reverse-biased *p/n* junctions, where the high electric field is very effective in collecting the charge by drift. The charge is also collected by diffusion, and some of it recombines before being collected.
SEU is a non-destructive phenomenon, which concerns in general every memory element temporarily storing a logic state. Typical examples of circuits affected by SEU are random–access memories (SRAMs and DRAMs), registers, microprocessors, programmable logic units, digital-signal processors, etc. Figure 95 shows the mechanism of a SEU.
The evaluation of the SEU sensitivity, is carried out by placing the device under a beam of particles and measuring its cross section σ, defined at normal incidence as:

$$\sigma = \frac{N_{events}}{\Phi}$$

where Φ is the total particle fluence, and N_{events} is the number of events (SEU) counted during the test. Cross-section curves typically represent the σ of the device as a function of either the linear energy transfer, or LET (for a heavy-ion experiment), or the energy of the incoming particles (for a proton experiment) [49].

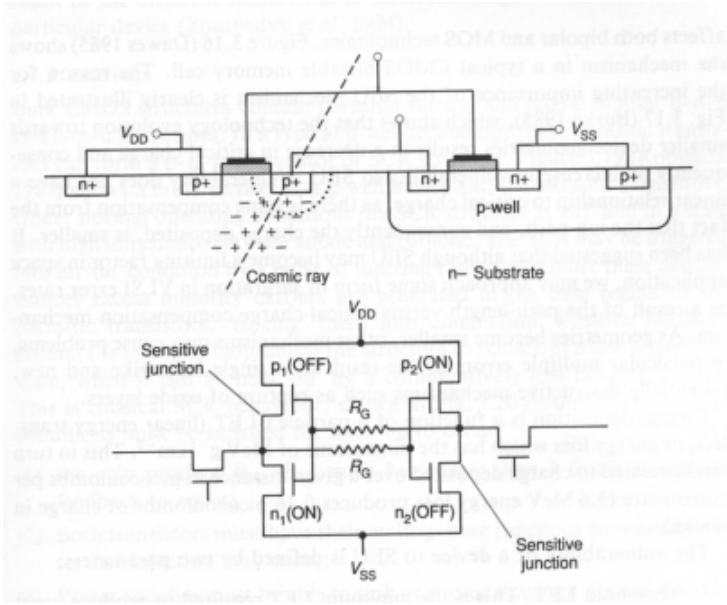


Figure 95 The SEU mechanism in a typical CMOS bistable memory cell

9.4.1 SEU in SRAM-based FPGAs

Programmable logic devices, and more specifically field programmable gate arrays (FPGA), are replacing traditional logic circuits, offering the advantages of high integration: small size, low power, and high reliability. FPGAs based on SRAM technology offer an additional advantage: they can be reprogrammed an unlimited number of times, even in the end-user system. In these FPGAs, a multitude of latches, (also called memory cells or RAM bits), define all logic functions and on-chip interconnects. Since the behaviour of an SRAM-based FPGA is determined by the bitstream loaded and stored in it, the effect of a SEU may drastically alter the correct operation of FPGAs; see how in Fig. 96.
When analysing SEU effects in SRAM-based devices, two complementary aspects should be considered:

1) SEUs may alter the memory elements embedded in the design, for example, the content of a register in the data path, or the content of the state register of a control unit.

2) SEUs may alter the content of the memory storing the device configuration information, for example, the content of a look-up table (LUT) inside a configurable logic block (CLB), or the routing of a signal in a CLB or between two CLBs.

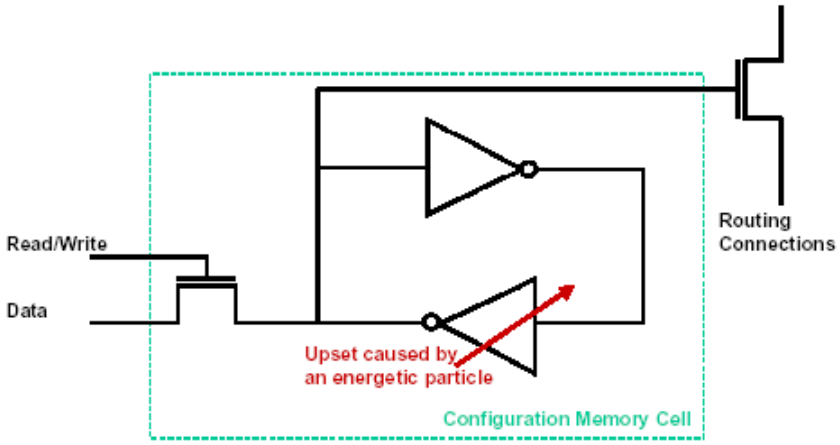


Figure 96 A SRAM configuration element (switch) in a programmable device

9.4.2 Radiation errors in Flash memories

The basic structure of a Flash memory cell uses a dual sandwiched gate structure, interposing a floating gate between the body of the device and the control gate.
In Flash memories, SEU effects are dominated by errors in their complex internal architecture rather than in the non-volatile storage array. Previous test runs have shown that no errors are produced when the devices are irradiated in an unpowered mode, and that errors in the memory array can only be produced for high LET of the incoming particle (of order 40 MeV cm^2 mg^{-1}). Since errors occur mostly in the complex control circuitry, the functional consequences of the SEU can be multiple. The circuit often requires a power cycling to recover the correct functionality. Sometimes a steep increase in the current consumption is observed during or even after irradiation, probably because of the logic conflicts in some internal registers, address or buffer. Seldom, this current can also be high enough to destroy the device. Compared to DRAMs and SRAMs, the sensitivity of Flash memories is nevertheless generally much lower. The threshold charges for upset is considerably higher (LET of 7 MeV cm^2 mg^{-1} or more), and the cross section is much lower because only a small portion of the circuit, containing the control

logic, is sensitive. Proton test data show a cross section of typically 100–1000 times smaller than DRAMs or SRAMs.

9.5 Results from Jyväskylä irradiation tests

9.5.1 Purpose of the tests

The aim of the tests was to study the behaviour of different components to be used in the final version of the CB and LB in the RPC trigger system, to measure their radiation sensitiveness and to investigate the errors structure, in order to optimize the EDAC algorithms.
The components tested were: a Flash memory (Am29F160D) and a SDRAM memory (ISSI IS42S16400) that will be put on the CB and will be used to store the FPGA configuration, and a device placed on the Memec Spartan–IIE development kit board that will be put in the final version of the LB. Three Spartan boards were tested. The tests were performed at the Cyclotron of the Jyväskylä Accelerator Laboratory, in Finland. Two sets of tests were made: with protons of 30 MeV and then with protons of 50 MeV.

9.5.2 Radiation-effects facility (RADEF) at the Jyväskylä Accelerator Laboratory

The RADEF includes a special beam line dedicated to irradiation studies of semiconductor components and devices [50]. It consists of a vacuum chamber, shown in Fig. 97, including component movement apparatus and the necessary diagnostic equipment required for the beam quality and intensity analysis.

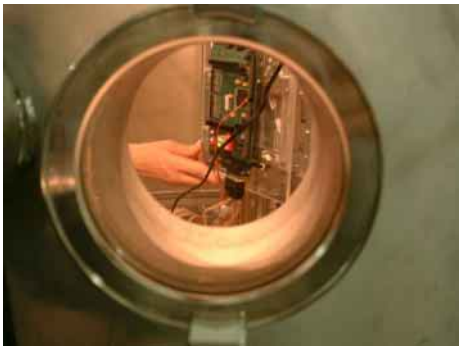


Figure 97 A view of the vacuum chamber

The cyclotron is a versatile, sector-focused accelerator of beams from hydrogen to xenon, equipped with three external ion sources: two electron cyclotron resonance (ECR) ion sources designed for high-charge-state heavy ions, and a multicusp ion source for intense beams of protons. The ECR is especially valuable in the study of SEEs in semiconductor devices. For heavy ions, the maximum energy attainable can be determined using the formula $130q^2/m$, where q is the ion charge and m is the mass. Protons can also be used for total dose tests or radiation hardness (RadHard) studies in an energy range from a few MeV up to ~ 65 MeV.

The irradiation of the components is performed in a vacuum chamber of inside diameter 75 cm and a height of 81 cm. The chamber, along with the beam-line construction and beam diagnostic equipment, is shown in the picture of Fig. 98.

The vacuum in the chamber is achieved after 15 min of pumping, and the inflation takes only a few minutes. The position of the components installed in the linear movement apparatus inside the chamber can be adjusted in the x, y and z directions. The possibility of rotation around the y-axis is provided by a round table. The free movement area reserved for the components is 25 cm × 25 cm, which allows the performance of several consecutive irradiations for several different components without breaking the vacuum. The assembly is equipped with a standard mounting fixture. The adapters required accommodating the special board configurations, and the vacuum feed-throughs can also be made in the laboratory's workshops. The chamber has an entrance door, which allows rapid changing of the circuit board or individual components. A CCD camera with a magnifying telescope is located at the other end of the beam line to ensure accurate positioning of the components. The coordinates are stored in a computer memory, allowing fast positioning of various targets during the test.

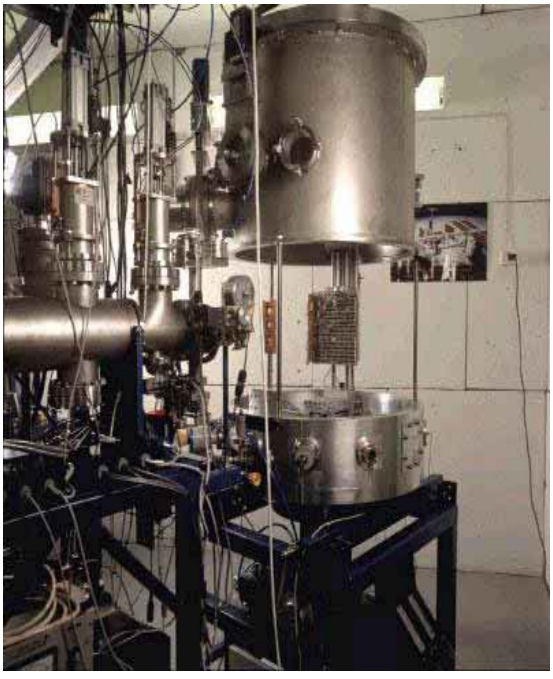


Figure 98 Chamber and beam equipment

9.5.3 The tests

1) FPGA tests

The first device we tested was the Xilinx Spartan–IIE (XC2S300E) (test procedure explained also in [37]). The chip is made in 0.18-μm technology, supplied with 1.8 V, containing 6912 logic cells, and having 1,875,648 configuration bits. It enables the read-back and verification of the configuration bits.
The configuration is the process of loading a design bit-stream into the FPGA internal configuration memory, while the read-back is the process of reading out those data. The read-back is quite an important operation since SEUs can be detected by it.
The tested chip was placed on the Memec Spartan–IIE Development kit board and was programmed by a JTAG interface.

During the irradiation the board was positioned perpendicularly to the beam, which was focused so as to irradiate only the Xilinx chip. Since the distance between irradiation area and control room is ~ 15 m, an extender of the JTAG cable that connected the mezzanine card and the Altera Byte Blaster plugged into the PCs parallel port was developed.
Two kinds of tests were performed [51]:

a) Test with read-back

The goal of this test was to find the cross section for SEUs in configuration SRAM cells. The device was loaded and then, during the irradiation, the configuration bits were read-back every minute and compared with loaded bits. The number of upset bits was recorded. The results of this test are reported in Table 11 (they are in good agreement with results found in [37]).

Beam energy	Chip	Dose [1/cm^2]	SEU number	σ/device [cm^2]	σ/bit [cm^2]
30 MeV	#1	1.2×10^{12}	25046	2.0×10^{-8}	1.1×10^{-14}
	#2	2.5×10^{12}	43859	1.7×10^{-8}	9.3×10^{-14}
	#3	1.6×10^{12}	29068	1.9×10^{-8}	1.0×10^{-14}
50 MeV	#3	3.4×10^{10}	770	2.3×10^{-8}	1.2×10^{-14}

Table 11 Results of a SEU test in configuration bits

b) Test with dedicated logic

This test was made to measure the cross section for dynamic SEU in flip-flops and to recognize the vulnerability of the design for the errors in configuration bits. The FPGA was configured with a design containing a 5504-bit shift register (see Fig. 99). The input of the shift register was driven with a repeating pattern of four '0' followed by four '1'. The XOR gate comparing the output of the register with its input indicated the errors. The design utilized about 90% of FPGA resources. The outputs of the registers and the XOR gate were observed on the scope.
In Fig. 100 we can see the normal operation (a), the expected dynamic SEU signal (b), the shift register broken off and linked to another part of the register (c) and the shift register broken off (d).

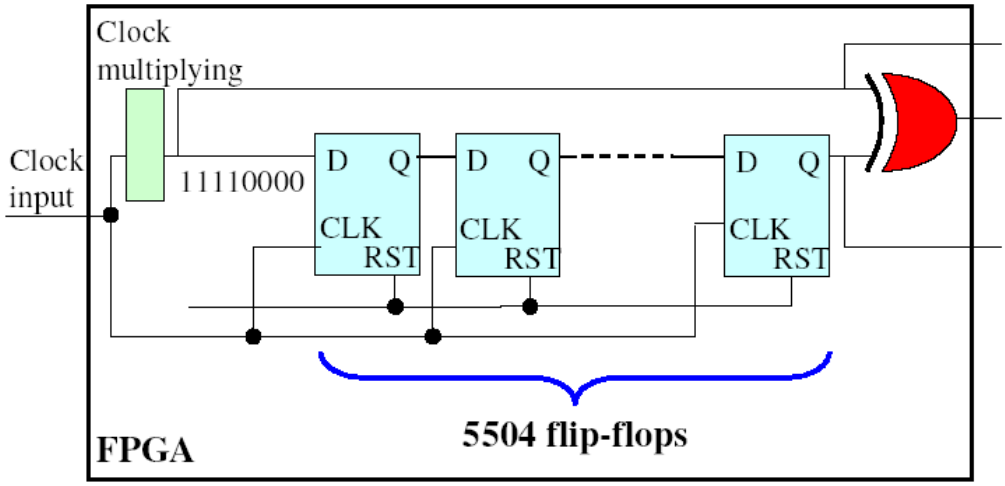


Figure 99 The schematic drawing of the shift-register design used for testing the dynamic SEU

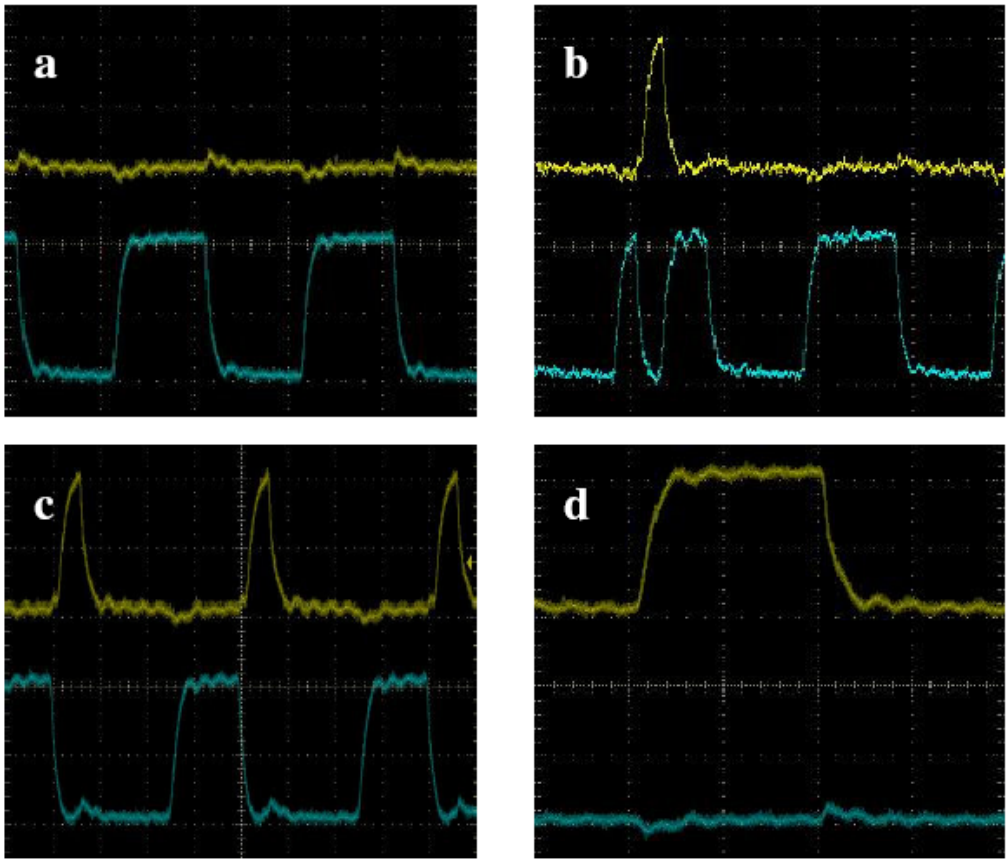


Figure 100 Performance of the shift-register design observed on the scope. The upper signal (yellow) is the output of the XOR; the bottom part (in blue in this picture) is the output of the shift register.

The test procedure was the following:

- The device under test was loaded with configuration data. After programming, it started its operation;
- Immediately after loading, the read-back of the configuration bits started (this function runs in the background and it does not affect the performance of the FPGA), and the number of upsets was recorded;
- When the signals on the scope indicated the permanent corruption of the design (see Fig. 100), the second read-back was started.

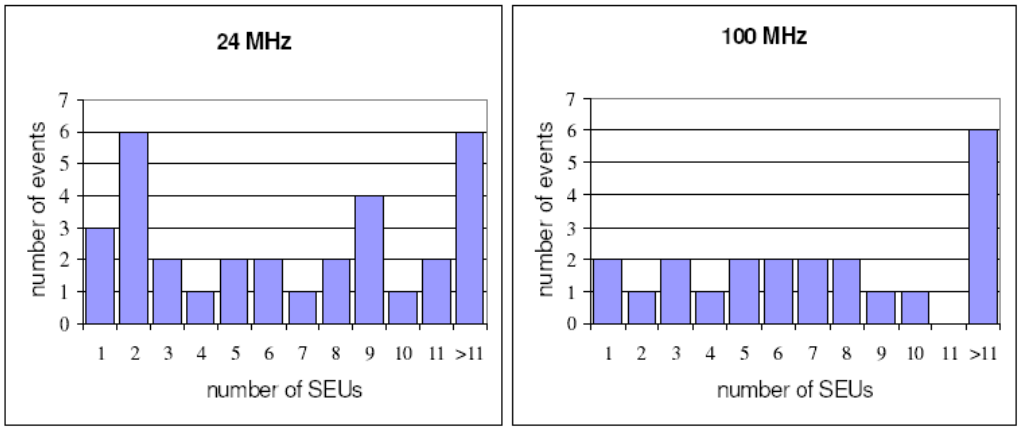


Figure 101 Number of SEUs in configuration bits after detecting the shift-register breaking

The beam was set for very low intensity (~ 7.5×10^6 p/cm^2/s) and thus induced only a few SEUs in configuration bits per minute. The programming took about 10 s, so it could be done with the beam on, because only single errors could occur during programming time, which did not affect the chip operation. Tests were performed with two different frequencies: 24 MHz and 100 MHz. No dynamic SEUs were observed in either case. Figure 101 shows the distribution of SEU numbers in configuration bits after detecting the shift–register breaking. In several cases we observed that, after some successive reprogramming, the output of the shift register remained in the same, wrong state, in spite of the read–back showing 0 or single errors. Turning off the power restored the functionality of the chip. This phenomenon was observed four times during the test at 24 MHz, and three times during the test at 100 MHz.

2) Tests of memories

Two types of memory have been tested:

- SDRAM memory (ISSI IS42S16400), 64 Mbits, 0.18 µm, 3.3 V
- FLASH memory (AMD AM29LV160D), 16 Mbits

The experiments were performed using the dedicated PCB, containing an AVR microcontroller, an Altera FPGA, a SDRAM memory chip and a ZIF (zero insertion force) pocket for removable Flash memory and for providing connections to the PC by RS232 and JTAG ports.
The FPGA chip (Altera ACEX 1K EP1K100FC256) was used to implement the memory controllers. The AVR microcontroller (AT90S8515) was used to execute tests of the

memories and reporting errors to the PC by serial port. The PC was running the appropriate software to control tests routine and to configure AVR and FPGA.
Memories were tested dynamically: the whole memory was filled with 16-bit words of pseudo-random values. During the irradiation, the read-back of the data stored in memory was performed. The reading phase was repeated many times, consecutively. In the SDRAM memory, a word containing corrupted data was rewritten immediately upon detection of the error. Auto-refresh was performed with a frequency of 2.4 kHz. Tests were run with a few different beam intensities.

3) Test results for Flash memory

The memories that were tested under irradiation survived without any errors. The irradiation beam intensity was 6×10^7 protons/cm^{-2}/s^{-1} up to dose of 1.2×10^{11} cm^{-2}. Errors appeared during the irradiation with higher beam intensity (see Table 12). These errors occurred sequentially. The first mistakes appeared in the four oldest bits, then in the eight oldest, and so on.

FLASH #	First Errors		Complete damage	
	After dose [protons/cm^2]	Beam current	After dose [protons/cm^2]	Beam current
FLASH # 1	7.583×10^{11}	~ 3.5×10^9	7.967×10^{11}	~ 3.5×10^9
FLASH # 2	5.95×10^{11}	~ 3.5×10^8	6.49×10^{11}	~ 3.5×10^8
FLASH # 3	6.32×10^{11}	~ 3.25×10^8	NOT OBSERVED	

Table 12 Doses and beam currents for errors in Flash memories

At the end, the read value of all bits was '1'. This complete damage of memory appeared after the dose presented in Table 12. It is highly probable that these errors are a result of the dynamic destruction of the Flash memory internal logic. But without complete information from the manufacturer it is hard to prove this conjecture. Only zero to one upsets were observed.
In the case of FLASH #3, after the first errors were noticed, the beam was turned off. The number of errors increased a little bit more and then started decreasing from 337,939 to 68 wrong bits, over 1 hour. Tests executed a few days after the irradiation experiments revealed that the Flash memories stored the correct, programmed data and that the errors disappeared. However, the Erase function was still not working. This was probably caused by the destruction of the charge pump.

4) Test results for SDRAM memory

Complete, permanent destruction of memory was not observed. Only bit upsets appeared, but no stuck bits. There was one test in which a huge amount of writing errors occurred. These errors were reported when AVR read corrupted data from the memory and tried to rewrite them with the correct value, but the written data still did not agree with the correct value. This means that stuck bits might have occurred, but, more probably, it was a dynamic SEU in AVR or FPGA, caused by secondary particles. The number of zero to one upsets was approximately the same as the number of one to zero upsets. For SDRAM #2 there were about 20% of errors with multiple-bit flips in one word.
The obtained cross sections for these memories were:

- SDRAM #1 – 2.37×10^{-9} cm^2/device
- SDRAM #2 – 1.59×10^{-9} cm^2/device

These low values of cross sections may be an effect of the high frequency of memory refresh. Capacitors were charged to proper voltage level so often that ionized particles could not change their potentials.
Figs. 102 and 103 show, respectively, the pre-prototype and the prototype of the control board, irradiated during different tests at Jyväskylä Accelerator Laboratory.

Figure 102 The pre-prototype of the control board

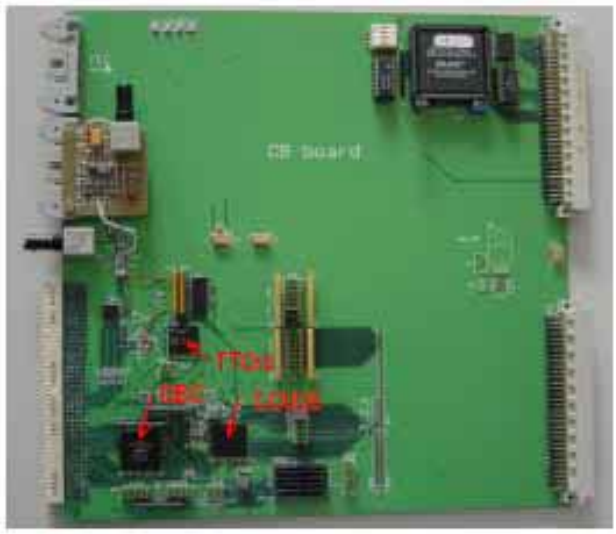


Figure 103 The prototype of the control board

9.5.4 Conclusions

Dynamic SEUs were not observed during the test. This result does not mean that such errors could not appear in a tested chip. It rather indicates that dynamic SEUs are much less probable than in configuration bits. The test also shows that few upsets in configuration bits may cause the corruption of the design. But this is not so surprising if we think that most of the configuration bits program the interconnections between elements of FPGA.
The results obtained during the tests enable us to estimate the expected SEUs rate induced by high-energy hadrons in CMS. Taking the worst result ($\sigma = 2.3 \times 10^{-8}$ cm^2/device) and particle fluxes from the previous tables (total charged hadrons and high–energy neutrons), we have

- In the ME1/1 – HE/1 region ($\varphi = 1.2 \times 10^3$ cm^2s^{-1}) –**1 SEU in 10 h per device**
- On balconies on the detector ($\varphi = 1.0 \times 10^2$ cm^2s^{-1}) – **0.08 SEU in 10 h per device**

The link system will contain 72 LBs in ME1/1 – HE/1, and 1568 LBs on the balconies. Since there are 2 FPGAs on each LB, we obtain:

- In the ME1/1 – HE/1 region – **14 SEUs in 1h for 144 devices**

- On balconies on the detector – **26 SEUs in 1h for 3136 devices**

The planned frequency of the FPGA of a reloading every 10 min should guarantee that at most a few SEUs would be accumulated in all LB FPGAs, which should not affect the system performance.
The tests proved that Flash memories are resistant enough to high–energy hadrons; during the test they survived without any errors a dose that exceeds a few times the expected dose in the ME1/1 – HE/1 region of CMS. The Flash memories will be used on the final Control Boards.

Figure 104 Myself during the night shift of data taking for the test runs at Jyväskylä.

Conclusions

The work presented in this thesis concerned the control of the Link Board in the RPC system of the CMS experiment at the LHC.
The whole project was realized in collaboration with the University of Bari, Italy, the University of Warsaw and the Warsaw University of Technology, Poland.
The CMS experiment includes three muon subsystems based on different types of muon chambers: drift tubes in the barrel, cathode strip chambers in the endcaps and additional layers of RPCs both in the barrel and in the endcaps. All three muon subsystems participate in the first-level trigger.
The CMS RPC readout system is made up of four components: the front-end board, the link board, the splitter board and the trigger and readout boards. The link board can be considered, in the system, as the heart of the data transmission, control and calibration features. Data from the RPCs are collected from the LB via short twisted-pair cables. The major task of the LB is to transmit these data to the trigger and readout boards, located in the Control Room. For each subdetector of the CMS experiment, it is necessary to continuously monitor the status of several parameters in the front-end electronics. In case of malfunction, an alarm generated by each subsystem must be reported to the DCS of the experiment.
My research activity has been focused on the control of the LB and it is recounted in this thesis according to the following plan.
After a theoretical introduction and a description of the LHC machine and of the CMS detector, the performance of the L1 Muon trigger of CMS was shown.
The DCS requirements, together with its architecture, were described in Chapter 3, before introducing the general overview of the RPC system.
The RPC Front-End electronics was presented in Chapter 4, followed by a detailed description of the Link Board in Chapter 5. There, I have listed and analysed the evolution of the research I have been perusing in the last years, through different approaches.
The first step was to consider the fieldbus solution: the WorldFIP immediately appeared as the fieldbus that could be the most appropriate for the requirements of our system.
Because of the cost of the implementation and, mainly, following the suggestion from the CMS Collaboration to adopt a solution compatible with the rest of the subsystems, I considered the tracker control solution, implemented by the CCU ASIC chip, which controls and monitors the embedded front-end electronics of the whole system. Its implementation on the control board has been fully analysed and tested during the last two years and it now represents the best solution for the control of the Link Board, described in Chapter 6.
The CMS trigger system has a tree-like structure in which the data flow through the entire chain should be synchronous, driven by the 40.08 MHz clock of the LHC. Testing the synchronization procedures is for this reason very important, and it can only be done with a particle beam that has a structure similar to that of the LHC, so as to simulate what will happen during the LHC operation.

Experimental test results obtained from these kinds of tests, which we made for the prototypes designed for the Front-End electronics of the RPC system, were presented in Chapter 7.
To gain a better knowledge of the RPCs working principle, I asked our colleagues involved in their construction to participate in some tests performed at the University of Bari. The results of RPC cosmic-rays tests were described in Chapter 8.
Chapter 9 was focused on the different irradiation tests performed in Finland, in which we had the possibility to define the final implementation of the Link-Board and Control-Board design.
The production of the Link Boards and Control Boards for the CMS experiment will start in April 2004 and they should be ready by November 2004.

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Acronyms and Abbreviations

ADC	Analog to digital converter
ALICE	A large ion collider experiment
APD	Avalanche photodiode
API	Application programming interface
APL	Application layer
ASIC	Application specific integrated circuit
bx	Bunch crossing
BTI	Bunch and track identifier
CAN	Control area network
CAM	Content addressable memory
CB	Control board
CBC	Control board controller
CBIC	Control board interface controller
CBPC	Control board peripheral controller
CCU	Communication and control unit
CCUM	Communication and control unit module
CLB	Configurable logic block
CMOS	Complementary metal oxide silicon
CMS	Compact muon solenoid
CSC	Cathode strip chamber
DAC	Digital to analog converter
DAQ	Data acquisition
DCS	Detector control system
DLL	Data link layer
DRAM	Dynamic random access memory
DT	Drift tube
ECAL	Electromagnetic calorimeter
ECC	Error checking and correction
ECR	Electron cyclotron resonance
EDAC	Error detection and correction
EEPROM	Electrically erasable programmable read-only memory
ELMB	Embedded local monitor board
FE	Front end
FEB	Front-end board
FEC	Front–end controller
FEC	Front–end chip
FED	Front–end driver

FIFO	First in, first out buffer
FMM	Fast merging module
FPGA	Field programmable gate array
GIF	Gamma irradiation facility
GOL	Gigabit optical link
GMT	Global muon trigger
GT	Global trigger
GUT	Grand unified theory
ISP	In-system programming
JCOP	Joint controls project
JTAG	Joint test action group
L1	Level 1
L1A	Level 1 accept
LAN	Local area network
LB	Link board
LBC	Link-board controller
LBrf	Reduced-functionality link board
LBus	Local bus
LBxs	Link board boxes
LCT	Local charged track
LDIWG	LHC data interchange working group
LDEMUX	Link demultiplexer
LDO	Low dropout
LET	Linear energy transfer
LEP	Large electron positron collider
LHC	Large hadron collider
LHCrx	LHC receiver module
LLB	Large link board
LLBxs	Large link Board boxes
LMUX	Link multiplexer
LSP	Lightest supersymmetric particle
LTC	Local trigger controller
LV	Low voltage
LVDS	Low voltage differential signalling
MIP	Minimum ionizing particle
MLB	Master link board
MOSFET	Metal-oxide semiconductor field-effect transistor

NIEL	Non–ionizing energy loss
OCS	Optical communication system
OLE	Object linking and embedding
OPC	Object process control
OSI	Open-system interconnect
PAC	Pattern comparator ASIC
PACT	Pattern comparator trigger
PBUS	Parallel bus
PCB	Printed circuit board
PCI	Personal computer interface
PDC	Producer/distributor/consumer protocol
PHL	Physical layer
PLC	Programmable logic controller
PLL	Phase locked loop
PMC	PCI mezzanine card
PVSS	Prozessvisualisierung und steuerung system
RADEF	Radiation facility
RadHard	Radiation hardness
RB	Readout board
RC	Run control
RCMS	Run control and monitoring system
RF	Radio frequency
RPC	Resistive-plate chamber
SB	Splitter board
SCADA	Supervisory control and data acquisition
SDRAM	Synchronous dynamic random access memory
SEB	Single-event burnout
SEE	Single-event effect
SEL	Single-event latchup
SEU	Single-event upset
S(L)LB	Slave (large) link board
SM	Standard model
SPS	Super proton synchrotron accelerator
SRAM	Static random access memory
SSD	Silicon strip detector
sTTS	Synchronous trigger throttling system
SUSY	Supersymmetry
TB	Trigger board

TC	Trigger crate
TCS	Trigger control system
TDC	Time to digital converter
TEC	Tracker endcap
TF	Track finder
TIB	Tracker inner barrel
TID	Tracker inner disk
TID	Total ionizing dose
TOB	Tracker outer barrel
TriDAS	Trigger and data acquisition system
TTC	Timing trigger and control
TTCcf	TTC fanout module
TTCci	CMS version of TTCvi
TTCex	TTC encoder and transmitter
TTCmi	Machine interface TTC
TTCrx	TTC receiver ASIC
TTCvi	TTC VME interface
TTS	Trigger throttle system
VME	Versa module eurocard
VHDL	Very high speed integrated-circuit hardware description language
WF	WorldFIP
XDAQ	Cross DAQ

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