



Summer Student Report

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Analysis of testbeam data of monolithic CMOS pixel sensor for ATLAS upgrade

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Mini-MALTA CMOS Pixel detector prototypes developed in TowerJazz 180 nm CMOS imaging process were measured at the DESY electron beam facility in April 2019 with electrons of 3 to 5 GeV. Up to five different samples were measured with NIEL doses of up to $2 \times 10^{15} \text{ n}_{eq} \text{ cm}^2$. This note reports an improved offline analysis using a 3 planes and a GBL track reconstruction algorithm. The results show an improved efficiency with respect to the preliminary data analysis performed at the time of the test-beam.

1 Introduction

Silicon monolithic sensors based on CMOS technology represents a promising solution for the next generation detectors including the ones for the High Luminosity LHC upgrade [1]. Their advantages consist in easier and cheaper manufacturing and assembly, smaller material budget and power consumption with respect to current hybrid technologies.

MiniMALTA [2] is a monolithic CMOS sensor with small ($3 \times 3 \mu m^2$) collection electrode. It consists of a matrix containing 16×64 square pixels with a pitch size of $36.4 \mu m$; it measures $1.7 \times 5 mm^2$. It represents an updated version of the full-size MALTA [3] chip (512×512 pixels) implementing several improvements over the previous version.

It is subdivided into 8 sectors (16×64 pixels each), with different design choices for both the sensor and the front end electronics:

- the 4 sectors on the right side contain a front end electronic similar to the original MALTA chip, while the left side employ improved transistors
- the bottom sectors have the same sensor as MALTA while the bottom-middle and the top sectors introduce modification of the sensor implants designed to improve the charge collection after irradiation
- the top-middle sector are non functioning due to manufacturing issues

This leaves with 6 different sectors. This note report the result of the analysis of test-beam data aiming at characterizing the hit efficiency of the various sectors as a function of different irradiation dose of the chip.

2 Experimental setup

The measurements were performed with EUDAQ DURANTA beam telescope at the DESY facility with an electron beam energy configurable from 3 to 5 GeV. The experimental setup is summarized in Figure 1. It consist of:

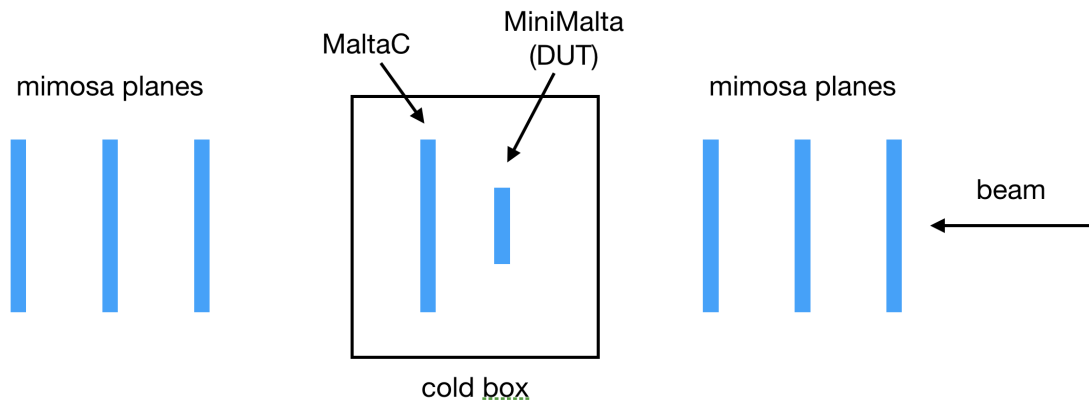


Figure 1: A schematic view of the position of the various element in the beam telescope.

- the MiniMALTA chip (device under test / DUT) is positioned inside a cold box cooled by dry-ice
- inside the cold box a MALTA chip is also positioned behind the DUT. This plane was also used as a source of trigger to collect the events. In addition a "region of interest" is set on the MALTA plane to limit the acceptance to a region that covers the MiniMALTA chip
- on both sides of the cold box a set of 3 MIMOSA¹ plane is assembled

2.1 list of chip tested

Several chips have been tested corresponding to different radiation level and chip configuration. The configuration is primarily specified by two parameters:

- substrate voltage (SUB): voltage applied to deplete the sensitive region of the chip.
- threshold of the front-end discriminator: IDB is a 8-bit DAC controlling the reference current of the main front-end discrimination circuit. Higher values represent a larger threshold.

In addition several beam energies have been tested in order to characterise the performance of the beam telescope. A summary can be found in the Table 1.

Chip	dose (n_{eq}/cm^2)	Beam Energy (GeV)	SUB (V)	IDB	Runs List
W2R11	0	3,4,5	2	20,50,100	1152-1183
W1R2	$1 \cdot 10^{15}$	3,4,5	2,6,10	40,100,250	1187-1377
W4R1	$1 \cdot 10^{15}$	5	10	40	1532-1545
W2R3	$2 \cdot 10^{15}$	5	10	30,60,160	1458-1521
W5R3	$2 \cdot 10^{15}$	5	6,10,15	40	1522-1531

Table 1: List of chip tested together with the beam conditions and main parameters

3 Analysis methodology

The key quantity to measure is the hit efficiency of the chip which is the fraction of time an incoming charge particle produces a signal above threshold which is then registered by the chip.

Hits recorded in planes other than the DUT are used to reconstruct tracks; the track is then extrapolated to the DUT plane to obtain an expected "intercept" (predicted location of the passage of the track particle). The DUT hit efficiency is defined as the fraction of intercepts that contains a real hit in the detector within a given distance.

The data were analysed real time during the test-beam with a very non-refined version of the analysis. This work presents a more optimised version of the analysis using the following improvements:

¹ MIMOSA is another CMOS chip with pitch size 18 μm .

- **mimosa planes cleanup:** before producing tracks, a cleanup procedure is applied to the data originating from the MIMOSA planes by only selecting events which overlap in space with the region of interest of MALTA as well as removing very noisy pixels. Such procedure is particularly useful in significantly improving the execution time of the tracking step especially since a more complex algorithm has been adopted.
- **tracking improvement:** the old analysis used a straight line tracking algorithm which is not suitable for low energy electrons since they are subjected to multiple scattering. The new analysis uses a GBL (General Broken Line) Tracking [4] which significantly improved the resolution by taking into account potential scattering at each material surface in front of the beam (even when a plane is not explicitly used in the tracking). Figure 2 shows a comparison of the unbiased residual on the DUT plane (distance between track extrapolation position and actual hit position on the plane) for a given run in the old and new analysis. The resolution improves from 50 to 15 μm . Such improvement has been shown to not depend on the beam energy and similar performance are obtained when the GBL algorithm is properly aware of the beam energy.

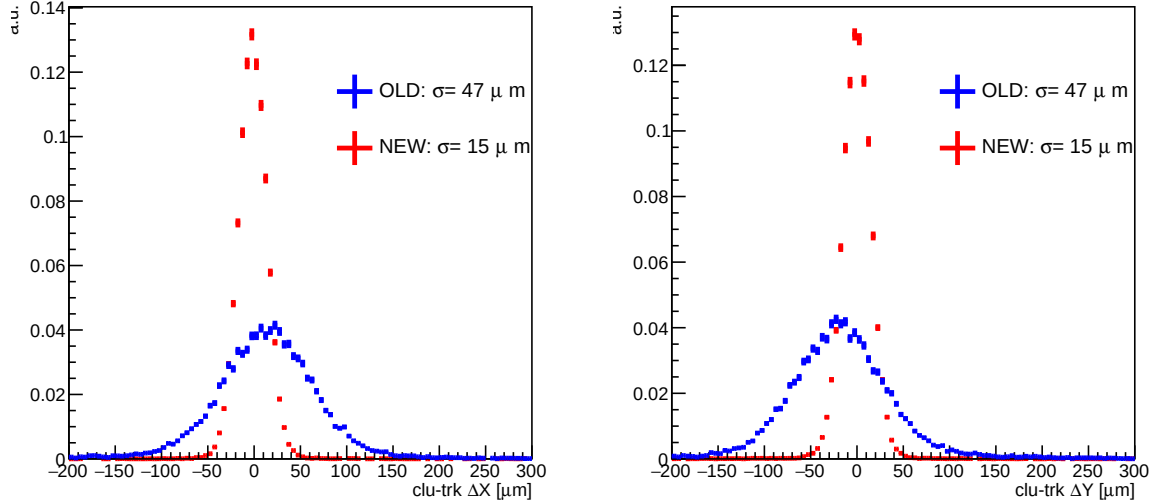


Figure 2: Comparison of unbiased track-cluster residual for the x (left) and y (right) dimension between the old and the new analysis.

The improved resolution allows us to use a cut of:

$$\Delta R = \sqrt{(\Delta X)^2 + (\Delta Y)^2} < 80 \mu\text{m} \quad (1)$$

to define the match between the intercept and the hit in the plane (plot).

- **number of planes:** given the low energy of the beam and the multiple scattering it was shown that using 7 planes to build the track does not bring any benefits. Therefore only three planes are considered when building the tracks: one MIMOSA plane in the front closest to the cold box, the MALTA plane and the MIMOSA plane on the back closest to the cold box. This configuration allows to speed up the tracking as well as improving the number of reconstructed tracks. Due to the GBL algorithm, tracks are considered valid if they satisfy:

$$\chi^2/nDOF < 10 \quad (2)$$

where nDOF is the number of degree of freedom of the track equal to 2 in our configuration².

- **fiducial region and cleaning:** when computing the efficiency its important to exclude region of the chip that can introduce biases on the measurement. This is the case for the border of the chip and disable pixels in the matrix. Due to the improved resolution of the GBL tracking, a very tight fiducial definition has been implemented. Only intercepts which are $15\ \mu m$ from the border of each sector as well as $36\ \mu m$ away from the center of any disable pixels are considered for the efficiency calculation. The original analysis did not have any special treatment for disabled pixels and a border region of $60\ \mu m$ thus resulting in a much smaller usable region and therefore lower statistics.

4 Results

All the configurations described in Table 1 have been re-analised, but only a selection of the results will be presented.

4.1 Comparison with previous analysis

Figure 3 shows the comparison between the old and the new analysis on a given configuration for the W1R2 chip irradiated to $1 \cdot 10^{15}\ n_{eq}/cm^2$. The main result of the test-beam is visible in the plot; there is a significant improvement in efficiency between a sector using the old MALTA-like technology (bottom right) and sectors with the modified technologies (top and middle left). In particular, a similar improvement in efficiency is seen between the right and left sector (the improved transistor allows to achieve a lower threshold for the same overall configuration) and between the bottom to the top 2 sectors (the modification of the sensors improves the charge collection at the edges of the chip).

Three clear features can be seen in the comparison: the improvement in statistical error, the increased coverage and the improvement in efficiency for sectors that contained disabled pixels. Such features are present for all the configurations that have been reconstructed.

4.2 Efficiency dependency on beam energy

Figure 4 shows that the efficiency measured on the non irradiated chip for a given configuration is independent on the beam energy. Since the beam rate strongly decreases with increasing energy, the lower 3 GeV value is the more optimal for future measurements.

4.3 Efficiency dependency on SUB voltage

Figure 5 shows the hit efficiency for the sectors of chip W1R2 as a function of the substrate voltage. A sharp drop of the efficiency is shown at 2 Volt with respect to the other configurations. This is compatible with the fact that a too low voltage is affecting the capability of the ionisation charge to be efficiently collected by the small electrode.

² The number of degree of freedom is given by the formula $2 * nPoint - 4$

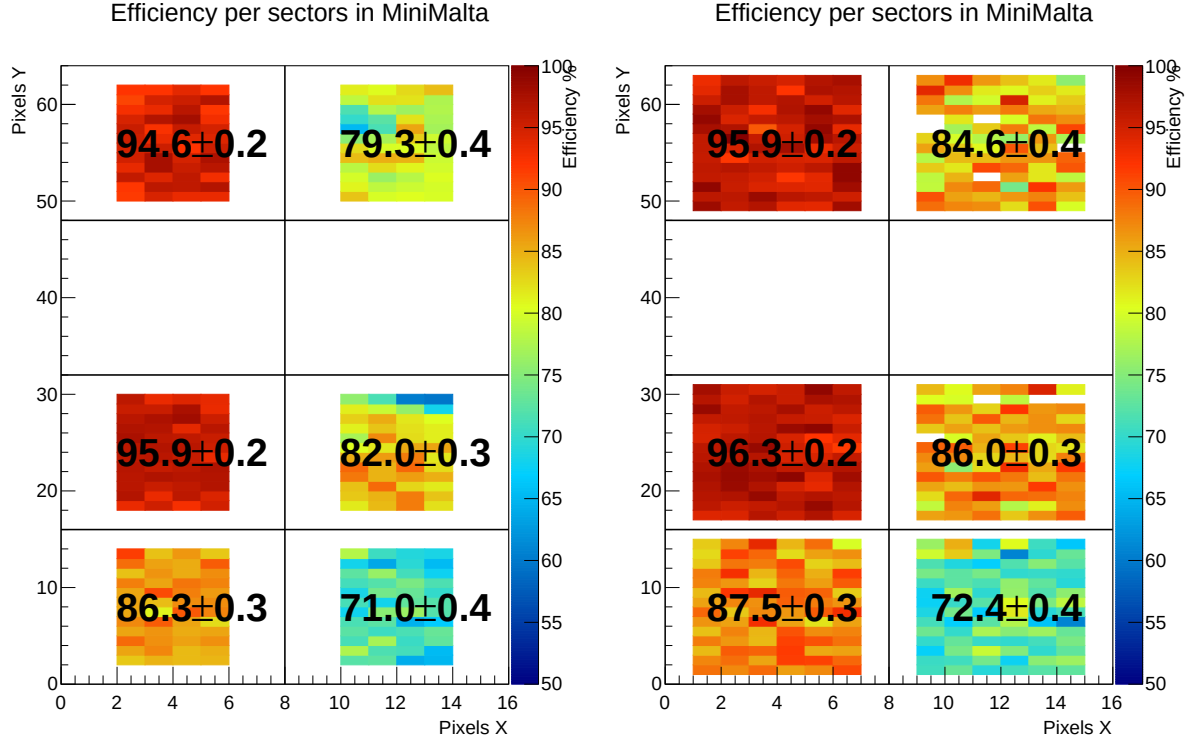


Figure 3: Hit efficiency of the W1R2 chip for the configuration with SUB=-6 V and IDB=250. The (left) plot shows the result of the original analysis while the (right) plot the result of the improved analysis.

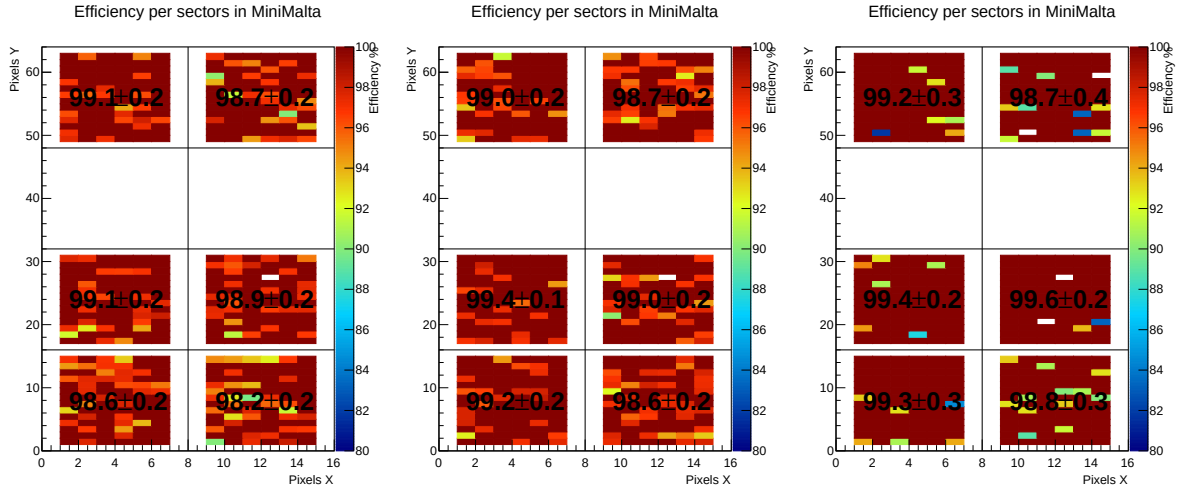


Figure 4: Hit efficiency of the non irradiated chip (W2R11) for different beam energies: (left) 3 GeV, (middle) 4 GeV, (right) 5 GeV. The SUB voltage is set to 2 Volt, while IDB is set to 20. The integral efficiency of each sector is reported in the plot.

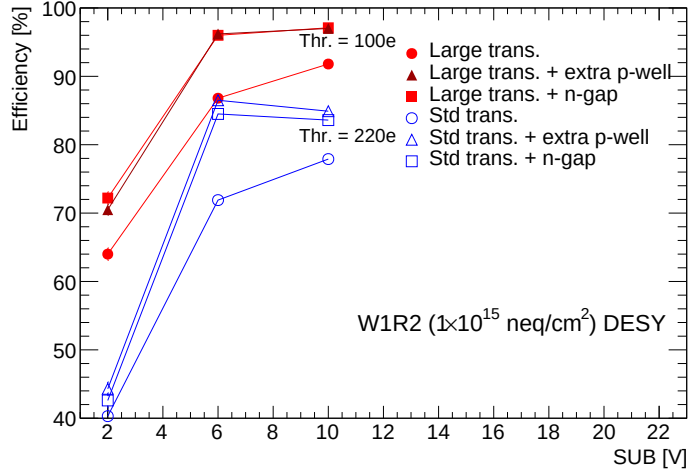


Figure 5: Efficiency of the various MiniMALTA sectors for a chip irradiated to $1 \cdot 10^{15} \text{ neq/cm}^2$ as a function of the substrate bias voltage.

5 Conclusion

Data from the 2019 test-beam campaign of the Mini-MALTA samples has been re-analysed. Improved resolution is observed.

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