Universität Bonn

Physikalisches Institut

Characterization of the Joined ATLAS and CMS RD53A Pixel Chip

Mark Hendrik Standke

This thesis aims to give a performance overview of the RD53A Hybrid pixel detector readout chip. The chip is manufactured in 65nm CMOS technology and the first large scale prototype for future chips incorporated into the pixel detectors of ATLAS and CMS. The chip has been tested bare with regards to its digital and analog performance. In addition to that the effect of different data acquisition systems on chip performance has been studied.

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Contents

CHAPTER 1

Introduction

In high energy physics, it is crucial to constantly increase an instruments discovery potential. This applies not only to small high energy particle experiments, but also to the largest machine ever build: The **L**arge **H**adron **C**ollider (LHC) located near Geneva-Switzerland. The LHC is a proton-proton collider running since 2010 with its four large experiments ATLAS, CMS, ALICE and LHCb. The upcoming major upgrade at LHC to **H**igh **L**uminosity- **L**arge **H**adron Collider (HL-LHC) will increase its luminosity by 5 to 7 times its nominal luminosity in 2016 and double its center of mass energy since 2011 [1]. Figure 1.1 shows the projects time line. In order to measure the increased amount of events provided by HL-LHC, detector upgrades are inevitable. This thesis will introduce and test the new generation of readout electronics for hybrid pixel detectors specified by the RD 53 collaboration. The tested chip is a joined prototype of ATLAS and CMS implemented in 65 nm CMOS technology. It is designed to find the best analog and digital pixel readout design in terms of radiation hardness, power consumption and readout performance for future chips incorporated into CMS and ATLAS.

Figure 1.1: Time line regarding the HL-LHC upgrade[1] © HL-LHC Project

CHAPTER 2

The ATLAS Detector

Particle detection is one of the most critical steps in high energy particle research. The non triviality is emphasized by the sheer size and complexity of particle detectors such as ATLAS or CMS. Those detectors detect particles produced during high energy collisions with incredible accuracy. Based on the acquired data, the tracks and class of every produced particle is reconstructed. This allows the operating physicists to gather information about the processes taking place under conditions comparable to the big bang.
A particle detector consists of innumerable components, which make up, lower order, but already highly complex detection sub-systems. The highest order ATLAS sub detection systems are discussed in the following Section 2.1.

2.1 ATLAS Structure

ATLAS is an abbreviation for **A** **T**oroidal **L**HC **A**pparatu**S** and one of two high energy multipurpose detectors at the LHC. ATLAS consists of many detector layers, which cylindrically surrounds one of the four collision points at the LHC. It monitors the energy and path of each produced particle. With its length of 44 m and height of 25 m it is the largest detector at CERN. A cross section of the detector can be seen in Figure 2.1.
The sub detector systems are classified into three major subgroups, each detecting another particle group or particle property. In the following abstract each of the detection systems will be explained.

2.1.1 The Muon-Spectrometer

The outer most detection system is the so called Muon Spectrometer. This detector reconstructs the trajectory and momentum of minimal ionizing particles such as muons. Muons are not subject to the strong force and are relatively heavy. Therefore they tend to emit very little bremsstrahlung and are the only particles well detectable beyond the calorimeters. To achieve high precision and accuracy in the muon detector, it is subdivided into four measurement systems. The **monitored drift tubes** (MDTs) as well as the **cathode strip chamber** (CSCs), which are responsible for taking high resolution spacial images. The **resistive plate chambers** (RPCs) as well as **thin gap chambers** (TGCs), which have low spacial resolution, but high time resolution. The combination of the four systems ensures high

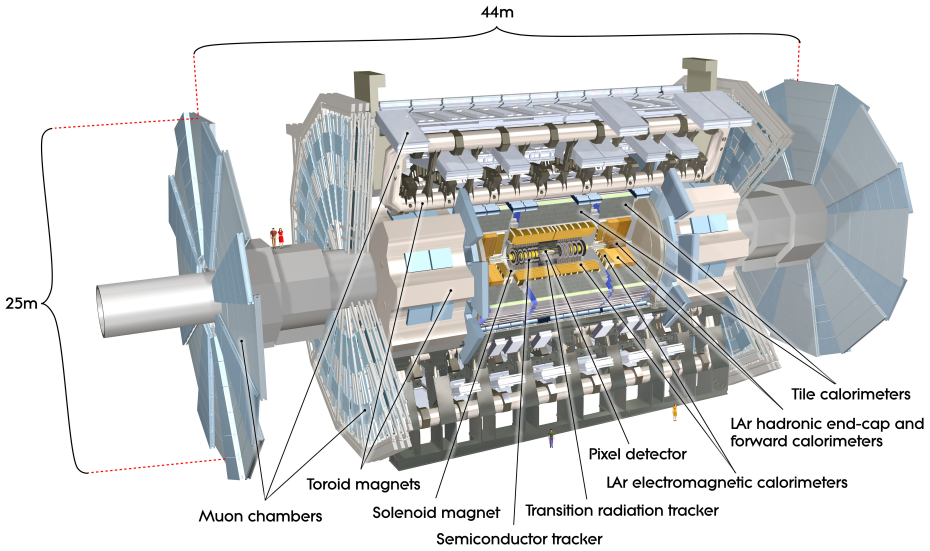


Figure 2.1: Cross section of the ATLAS detector. [2]

accuracy of muons moving in the additional toroidal magnetic field, which penetrates the muon detector.

2.1.2 The Calorimeter-System

Surrounded by the Muon Spectrometer we find the so called Calorimeter-System, which is designed to measure the energy of all traversing particles.
The calorimeter is designed to stop the particles and therefore absorb as much energy of not only charged but also uncharged particles. This is achieved by two independent calorimeter systems, which both contain material with a short mean free interaction path for either hadronic or electromagnetically interacting particles, as well as adequately large interaction volumes. The **hadronic calorimeter** is directly enclosed by the Muon Spectrometer and consists of two alternating layers of passive material such as steel which scatter the traversing particles due to hadronic interaction and an active scintillator material, which detects the produced particle showers. This setup is designed to measure the energy of hadronic interacting particles such as jets or hadronic decaying tau's.
Inside the hadronic calorimeter we find the **electromagnetic calorimeter** which measures mainly electromagnetically interacting particles such as electrons and photons. For this purpose it houses alternating layers of passive absorber material such as lead as well as liquid argon. The photon interaction with the lead leads to electromagnetic showers, while the argon is ionized and used to produce a signal which combined with another signals is proportional to the energy of the particle deposited in the detector.

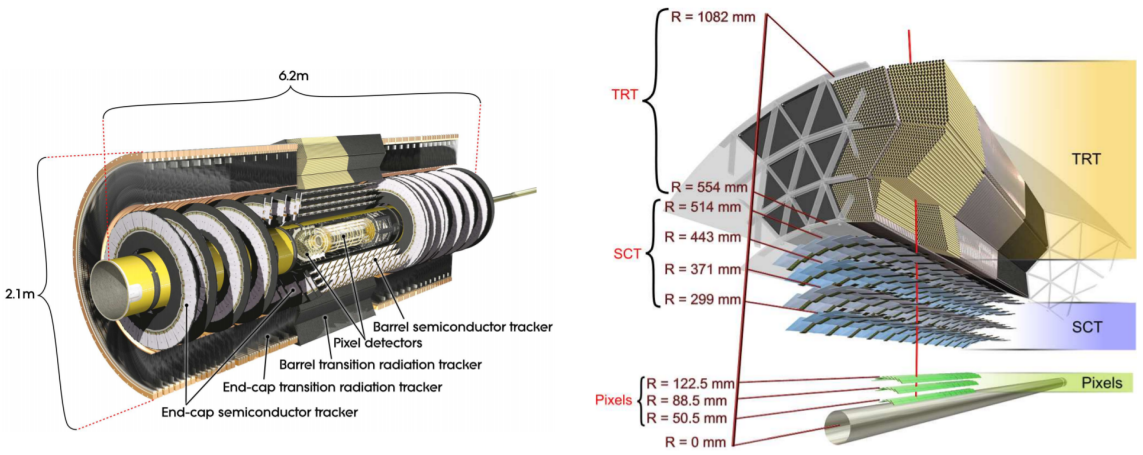
2.1.3 The Inner Detector

The detector closest to the collision point is the so called Inner Detector, which serves to reconstruct the track and momentum of electrically charged particles as well as their collision vertices. For this purpose it contains a transition radiation tracker (TRT), a silicone strip detector (SCT), as well as a pixel detector unit. This whole setup is enclosed into a solenoid magnetic field, which deflects the particles based on their charge and momentum.(see Fig. 2.2)[3].

The inner tracker's shell consists of a TRT detector, which consists of approximately 370000 thin tubes filled with a xenon, carbon dioxide and oxygen gas mixture. In the center of each tube an anode wire can be found. The detector works just like a drift chamber, in which charged particles ionize gas particles along their track. The hereby produced signal is readout by the wires and enables a computer to reconstruct the particle's track. The multiple scattering of the particle is hereby minimized, due to the gas mixtures low interaction cross section. Additionally the gaps between the tubes are filled with a material, which produces transition radiation if high energy particles traverse it. From the transition radiation signals strength, it is easy to differentiate for example muons and electrons.

Inside the transition radiation detector a four layer silicone strip detector (SCT) is placed. This is constructed as a tube with 5.5m length and a radius between 29.9cm and 51.4cm. It consists of silicon strips with a width of 80μm and a length between 5 cm and 12cm. Those strips are arranged in multiple layers with small varying angle between each layer. This design enables point like particle detection at reasonable resolution and speed.

Closest to the beam tube we find the pixel detector which has to cope with the highest radiation dose and track reconstruction rate, how this is achieved is discussed in Section 2.2.



(a) (b)

Figure 2.2: 2.2(a) The inner detector in longitudinal view 2.2(b) in radial view.[3]

2.2 The Pixel Detector

The current pixel detector consists of three layers with more than 80 million silicon-semiconductor pixels, each 0.4mm x 0.05mm in size. Combined they make up a detection unit with a radius between 50.5mm and 122.5mm. This kind of arrangement was chosen to be ideal in order to manage the high particle track density close to the beam tube. To minimize these errors even further and increase the vertex accuracy, the ATLAS collaboration decided to upgrade the pixel detector after Run 1. This was done by inserting an additional layer, the Insertable B-Layer (IBL), which was installed inside the Run 1 pixel detector and mounted on a new, smaller beam pipe. The IBL has smaller pixels with reduced thickness and different processing electronics, which provides charge measurements with lower resolution and dynamic range at a much higher rate. As stated in the beginning of Section 2.2, the pixel detector reconstructs a particle's path by correlating hits on each of the three pixel layers. Ideally each of the layers absorbs very small fractions of a particle's energy to minimize the distortion of the calorimeters measurement. One has to differentiate between charged particle detection and photon detection due to their fundamentally different interaction with matter. Whereas charged particles interact via material ionization, Cherenkov light emission and transition radiation. All three interactions are based on electromagnetic interaction. Their mean energy loss per penetration depth is described by the Bethe-Bloch-Formula [4]. High energy photons interact almost solely by pair creation. Pair creation is only possible if a photons energy is bigger than twice an electrons mass. This results in an electron positron-pair production, near an atoms nucleus's electric field. For the detection of such electron pairs, or ionized material, which can develop into showers inside a detector, ATLAS uses so called hybrid pixel detector modules. Opposed to monolithic detectors, where sensor and readout are on the same substrate, in hybrid detector modules sensor and readout are separated on two different chips. This has the advantage of choosing the ideal technology for sensor and readout chip independently, while maintaining very high readout frequencies at minimal power consumption. In order to connect the two chips, they are bump bonded, which corresponds to a soldering principle where each sensor pixel is connected to one readout circuit via inter chip connection. Figure 2.3 shows a front end chip, bump bonded to a sensor. In the upper half of pictures 2.3 a pixels sensor part is displayed which is a fully depleted diode in operation. Here one sees an n on n sensor, the depletion zone of which extends from the n - p transition to the bottom n on n transition. The depletion voltage applied to the back of the sensor therefore needs to be high enough to deplete the whole chip. The depletion zone is free of unbound charges due to recombination of the electron excess with hole excess between the n and p part. In case a charged particle crosses the detector it separates charge in form of electrons and electron holes, corresponding to the Bethe Bloch- equation [4] or pair creation. In the depletion zone the negatively charged electrons are then attracted by the n + on the bottom. The collected charge is guided to a bonding panel where it is transferred to the Front End-chip. The signal processing on the Front End-chip will be described in Chapter 3.1. Pixel separation is achieved on the n + side by p-spray. The p + backside implant is the same for all pixels.

2.3 The Inner Tracker upgrade

The tremendous increase in luminosity of the HL-LHC, as described in Chapter 2, makes a detector upgrade inevitable. The detector has to be capable of reconstructing tracks in dense track environments of $\approx$ 200 vertices per 30cm and cope with the enormous radiation levels associated with it [6]. As

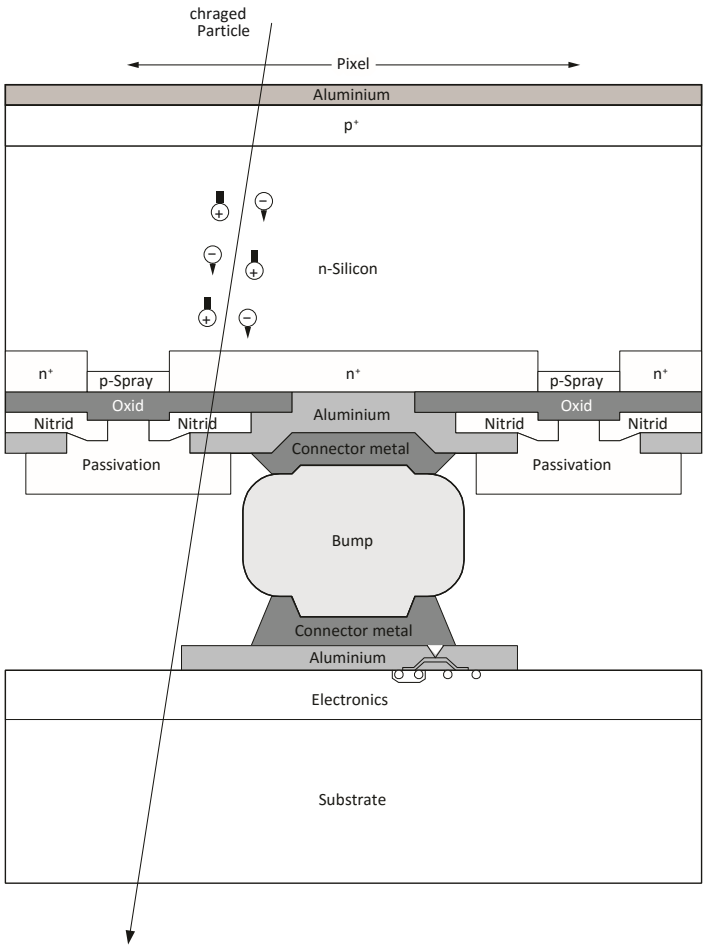


Figure 2.3: A cross-section of a sensor bump bonded to a Front End [5]. On the top one sees an n on n sensor, which is crossed by a charged particle. The middle depicts a soldered bump-ball and the bottom shows the Front End.

a consequence the new inner tracker (ITK) will solely consist of silicon -strip and -hybrid pixel detectors. Figure 2.4 shows a proposed design for the new inner tracker. The red lines indicate pixel detector layers which start to incline to very low and very high η's. This results in better η resolution. The current design for sees five pixel layers and four strip layers. This thesis will focus on the characterization of the prototype chip incorporated into the new pixel detector readout and its requirements set by the RD53 collaboration.

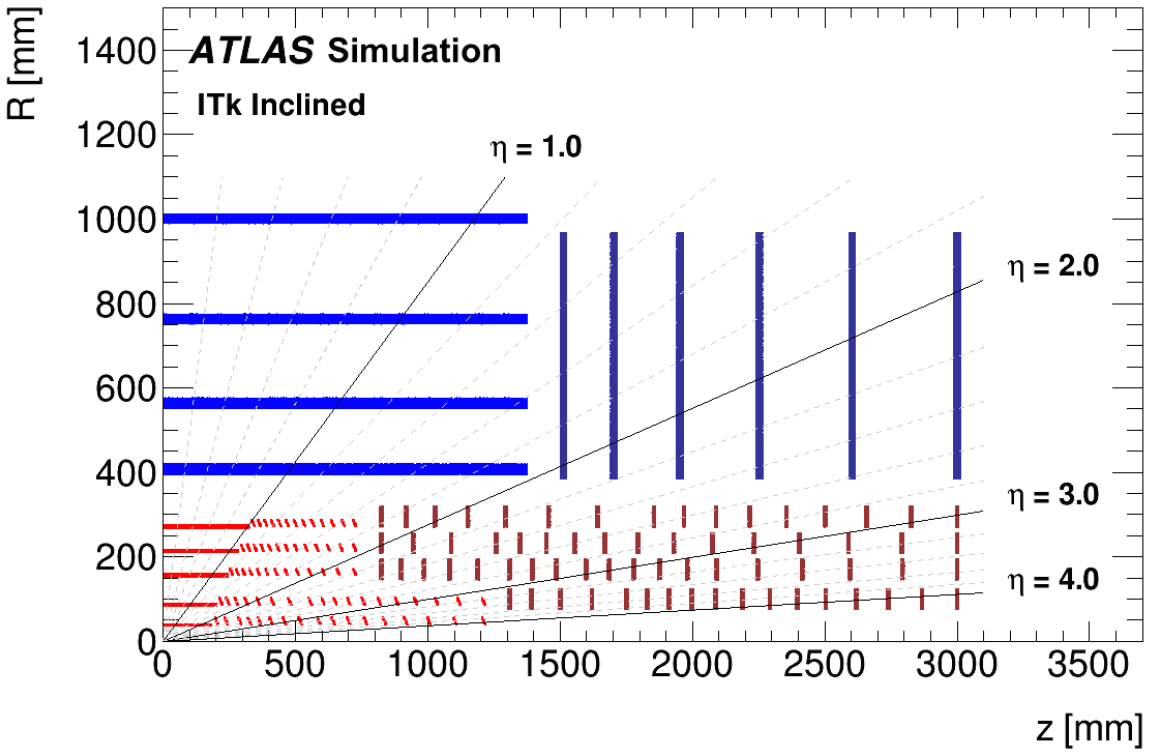


Figure 2.4: A scheme for the newly proposed ATLAS-ITK. Red lines indicate silicon pixel layers, while blue lines indicate silicone strip detectors [7]. A transition radiation detector will no longer be included.

CHAPTER 3

RD53A - Hybrid Pixel Readout Chip

The RD53A is a hybrid pixel readout chip. It is the first joined ATLAS and CMS prototype chip to demonstrate the novel analog Front End capabilities in 65nm technology. The 65nm CMOS technology has been introduced in 2006. This technology is currently offering the most promising way to get a cost efficient and power saving pixel readout chip meeting the required readout and environmental specifications set by the RD53 collaboration.

3.1 The RD53 Collaboration

RD stands for **R**esearch and **D**evelopment in reference to one of over 50 RD collaborations at CERN, that supply and design, tools and innovations needed to constantly improve and optimize the LHC. The RD53 collaboration's goal is to develop the tools and designs needed to produce the next generation of pixel readout chips needed by ATLAS and CMS at the HL-LHC [8]. Currently the first joint ATLAS and CMS pixel chip prototype, called "RD53A" is in the hardware testing phase. Both experiments have manufactured an individual first prototype prior to this chip. The so called Chipix chip for CMS and the Fe65-p2 chip for ATLAS. The main contributing institutes for Chipix were INFN Turino and Bergamo, while the Lawrence Berkeley National Laboratory and the University of Bonn were the main collaborators for Fe65-p2. The specifications for the common demonstrator are fixed in the "RD53A Integrated Circuit Specifications" [9]. This thesis goal is to test RD53A's performance in terms of the performance parameters stated in Table 3.1.

Circuit Property	RD53A -specification
Min stable Threshold	600 e^-
Threshold Dispersion	60 e^-
In-time Threshold	1200 e^-
Noise	$\sim$ 70 e^-
Power Consumption	$< 4\mu$A analog current consumption per pixel at 1.2 V

Table 3.1: Table with specifications for RD53A. Goal is to find a configuration for each Front End type that matches all set criteria. [9]

3.2 RD53A - Circuitry

RD53A features analog and digital circuitry on the same chip. Objective of this thesis is the characterization of the chips analog components. The analog components can be structured into two subgroups. The analog periphery and analog Front Ends. The Front Ends make up the pixel matrix to three equal parts. Figure 3.1 indicates the three flavors each featuring a different analog circuit implementation. The Synchronous Front End, which is described in Section 3.2.2 can be found on the left marked in red, the Linear Front End, described in section 3.2.2, can be found in the middle marked in green and the Differential Front End, described in Section 3.2.2 can be found on the right marked in blue. The whole chip measures 20 mm x 11.8 mm including the end of column logic and features a matrix size of 400 x 192 pixels. This is half of the aimed chip size of approximately 20mm x 20mm and 400 x 384 pixels for RD53B. A single pixel has a size of 50μm x 50 μm. All three Front End flavours share a common design feature. The so called analog island in a digital sea. This feature is also illustrated in Figure 3.1 by the two smaller images. Those display a zoom into the pixel matrix making the difference between the fully synthesized digital core (aka. digital sea) and the clear repeating patterns of the analog islands visible. The picture in the yellow frame represents roughly a single pixel, with the analog part marked in blue and the digital part marked in green. The grey square (BP*) on the top right of the analog Front End is a bump pad which connects the RD53A Front End to a sensor. In order to prevent digital noise to couple into the analog core they are not only spatially separated, but also surrounded by an additional deep n well, which prevents any unwanted charge flow between the analog and digital part. The analog periphery can be found on the bottom of Figure 3.1.

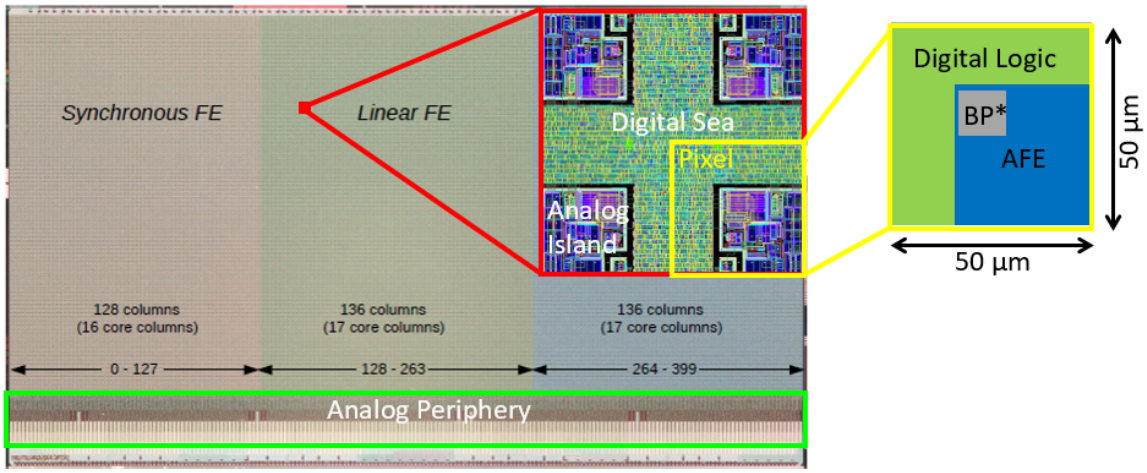


Figure 3.1: Shows an illustration of the RD53A chip, which is composed of three individual Front End flavours, they are called: Synchronous, Linear and Differential Front End. The column numbers are indicated at the bottom of each flavour [10]. The two smaller images illustrate the spacial separation between digital and analog components inside the pixel. The left image is a zoom into the pixel matrix, showing four analog pixels and the digital seas between them, while the smaller right picture illustrates the size of one pixel. The grey box in the top right of the analog Front End (BP*) illustrates a bump pad for connection to the sensor chip.

3.2.1 Analog Periphery

The analog periphery is used to supply reference currents via band gaps, measure chip internal voltages and currents, as well as temperatures and received radiation dose. In this chapter the so called monitoring block, consisting of a multiplexer and an analog to digital converter (ADC), as well as the chip internal temperature sensors will be described.

Monitoring block

The monitoring block of RD53A is designed for digitization of important internal parameters, such as internal voltages and currents, as well as environmental parameters such as temperatures and total irradiated dose. For this task the monitoring block uses two main components [10].

1. Two input stage multiplexers to map up to 57 different signals to the ADC as shown in Figure 3.2(a).
2. A 12 bit Successive Approximation Register (SAR) analog to digital converter (ADC) as shown in Figure 3.2(b).

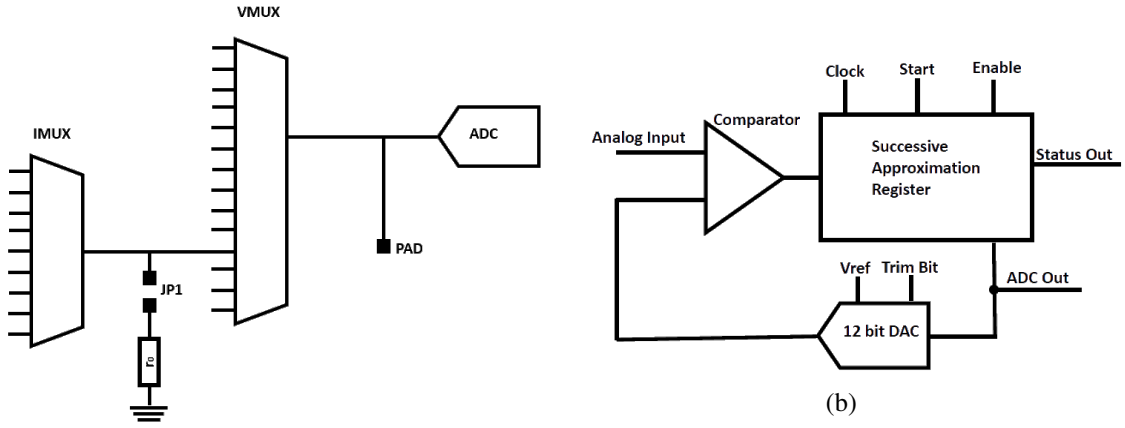


Figure 3.2: 3.2(a) General build up of the monitoring block containing all elements as enumerated in 3.2.1 The multiplexer is composed of a current multiplexer (IMUX) and a voltage multiplexer (VMUX). 3.2(b) Zoom into the 12 bit ADC block.

Figure 3.2(a) shows the **analog multiplexer** consisting of two stages. One is connected directly to the input of the ADC (VMUX), while the second one is connected to one of the inputs of the second stage multiplexer (IMUX). This second stage multiplexer is used to measure currents and therefore has an additional high resistive connection to ground. Both multiplexer outputs are routed to external pads (JP1 and PAD) for external measurement. The **Successive Approximation Register (SAR) analog to digital converter (ADC)** is shown in Figure 3.2(b). It consists of three major components, the comparator, a 12 bit DAC and a SAR. First the comparator takes the analog input signal and compares it to the signal of a 12 bit DAC. Based on the comparator output the SAR performs a binary search and either switches on or off certain registers of the 12bit DAC, which converges step by step towards

the analog input signal. The status output of the SAR thereby gives the measured ADC value. The clock drives the SAR at 312kHz, while the enable bit activates the SAR and the start bit activates a measurement. It is important to note, that the 12 bit DAC consists of two six bit DACs which can be tuned individually by an external trim bit to minimize the non linearity of the ADC. The trim bit hereby changes the step width of the lower 6 bit register to match the step width of the higher 6 bit register. How the trim bit influences the non linearity of the ADC was measured in Section 6.1.

Temperature Sensors

The temperature sensors of RD53A are diode sensors. The chip contains four of them at the locations indicated in yellow in Figure 3.3(a). The grey area hereby represents the chip area, while the blue area is the carrier printed circuit board (PCB). The red rectangle marked as NTC corresponds to a Negative Temperature Coefficient Thermistor (NTC) mounted on the PCB. This will be used as temperature reference during calibration. Figure 3.3(b) shows a circuit diagram of the current sources of the temperature sensor and the sensor diode. The current source, marked as 4 bit DAC determines the current going through the sensor diode. The ADC is connected to V_{OUT} and measures the voltage to ground. A temperature measurement is conducted by applying a low current followed by a high current to the sensor and measuring the voltage in both cases. The voltage slope ΔV between the two measured points is temperature dependent and follows the relation described in Equation 3.1 [11].

$$T[^\circ C] = \frac{e}{N_f \cdot k_B \cdot \ln 15} \cdot \Delta V - 273.15^\circ C \tag{3.1}$$

T hereby corresponds to the temperature in °C, e to the electron charge in Coulomb, k_B to the Boltzmann constant, ΔV to the Voltage slope in one measurement and N_f to a parameter, which has to be determined experimentally.

$$\Delta T[^\circ C] = \frac{e}{k_B \cdot \ln 15} \sqrt{\left(\frac{\Delta\Delta V}{N_f}\right)^2 + \left(\frac{\Delta V \cdot \Delta N_f}{N_f^2}\right)^2} \tag{3.2}$$

Equation 3.2 is derived from 3.1. $\Delta\Delta V$ hereby corresponds to the standard deviation of 10 voltage measurements. ΔN_f to the standard deviation of all N_f measurements of the given sensor in this scan. For the conversion from the measured ADC value to voltage Equation 3.3 is used. This conversion value was acquired from multiple measurements as described in Section 5.1. Figure 5.1(a) shows the slope and y interception of one of the measurements in the bottom right corner. Section 6.2 shows the results of the temperature calibration.

$$\Delta V[\mathrm{V}] = 0.19 \times 10^{-4} \cdot \Delta ADC + 8.21 \times 10^{-4} \tag{3.3}$$

3.2.2 Analog Front Ends

The analog Front Ends cover the largest part of the chip. A derivative of the circuit shown in Figure 3.4(a) can be found in each pixel. This circuit is used to process the charges received over the bump pad from the sensor as described in Figure 2.3. The three analog Front Ends each consist of a charge sensitive amplifier (CSA), as well as a comparator circuit. Figure 3.4(a) shows the basic working

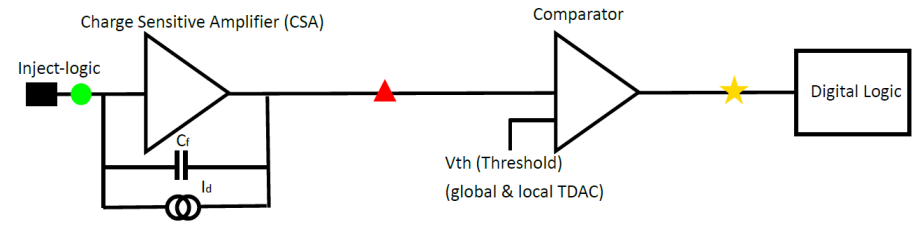
(a) (b)

Figure 3.3: 3.3(a) Locations of the temperature sensors of RD53A. 3.3(b) Schematics for one temperature sensor.

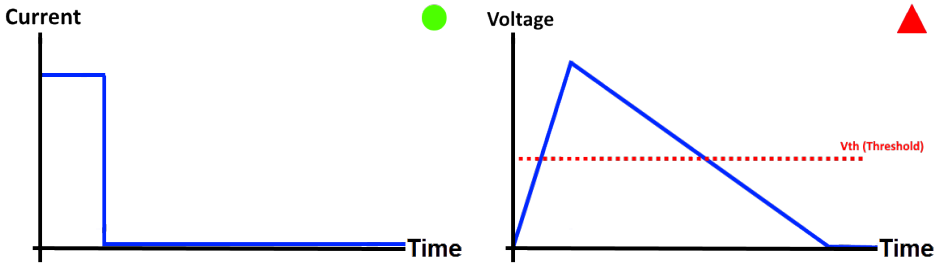
principle of such a circuit. The injection logic, or sensor diode injects charge into the CSA at the point of the green circle. The corresponding signal can be found in Figure 3.4(b). This charges the C_f capacitance until the current spike drops back to zero. This effect is also visible at the CSA output (red triangle), by the rising voltage slope shown in Figure 3.4(c). As soon as the current signal drops back to zero, the discharging effect of the constant current source I_d becomes visible, as the falling slope on the right of Figure 3.4(c) indicates. The triangular signal is then fed into a comparator, which compares the incoming signal to a reference voltage, called threshold. This threshold consists of a global component, which is constant for all pixels, and a local (TDAC) component, which can be adjusted for each pixel individually to compensate for process variations. Figure 3.4(d) shows the output of the comparator at the yellow star, which is either high or low. The comparator output is low, as long as the triangular signal is below threshold and rises to high, as long as the triangular signal is over the threshold. This time is called Time over Threshold time (ToT). This signal is then sent into the digital chip domain for further processing.

Synchronous Analog Front End

The name of the Synchronous Front End is derived from its AC coupling (C_{ac}) to a synchronous comparator. Figure 3.5(a) shows the Front Ends analog circuitry. The discharge of the CSA hereby gets taken care of by the Krummenacher Circuit [12] surrounding the CSA. This circuits output is visible in Figure 3.5(c). This signal is processed by a so called differential preamplifier, due to its comperating and moderate amplification properties. Its output signal can be seen in Figure 3.5(d). The preamplifier uses a so called auto zeroing process to compensate for local threshold variations. During the auto zeroing all switches surrounding the preamplifier are closed and the auto zeroing capacitances C_{az} are charged, until the voltage potential in front of the preamplifier and behind the preamplifier are on the same level. During operation the switches are open and the capacitances slowly discharge. Therefore this operation has to be repeated multiple times a second. The preamplifier signal is processed inside the Front Ends digital domain, which digitizes the signal according to the output shown in Figure 3.5(e). The crossing points of the two differential signals shown in Figure 3.5(d) hereby correspond to the threshold. As long as the orange signal is higher than the blue signal, the comparator signal remains low, as soon as the blue signals gets larger than the orange signal, the comparator signal gets high. The performance of this circuit can be influenced by the currents and

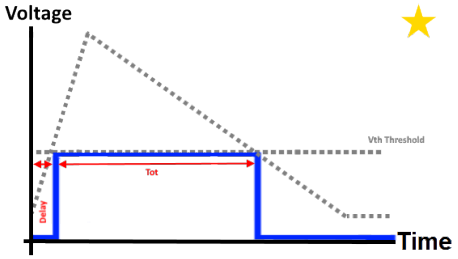


(a) General Front End Schematics



(b) Injection Signal

(c) CSA Output



(d) Comparator Output

Figure 3.4: 3.4(a) General schematics of an analog Front End. From left to right the charge input via detector diode or injection input, a charge sensitive amplifier (CSA) and a comparator, which outputs the analog signal for digitization is visible. 3.4(b) Signal produced from the sensor diode. 3.4(c) Signal after the charge sensitive amplifier. 3.4(d) Output signal of the comparator stage. 3.4(d) Signal after the comparator.

voltages supplied. The supply voltages and currents all end on "_SYNC" in Figure 3.5(a) and are each controlled by an individual DAC. A short description of each DAC and the default value can be found in Table 3.2. The here mentioned voltages and currents are the ones varied in Chapter 6 "Results".

Linear Analog Front End

The Linear Front End's name is derived from its linear pulse amplification in front of the discriminator stage. Figure 3.6(a) shows the Front End's analog circuitry. The discharge of the CSA hereby gets taken care of by the Krummenacher Circuit surrounding the CSA. This circuits output is visible in Figure 3.6(c). The signal is then processed by an operational transconductance amplifier (OTA), which amplifies the input signal and shifts the output current proportional to the applied threshold voltage. The output can be seen in Figure 3.6(d). The grey dotted lines hereby show the effect of the local threshold (TDAC) parameter, which shifts the signal according to a current offset up or down. In the following the signal is digitized as described in Section 3.2.2. The signal after the comparator

DAC Name	Recommended Value [13]	Description
IBIASP1_SYNC	80	Bias current of the main branch of the CSA
IBIASP2_SYNC	120	Bias current of the splitting branch of the CSA
IBIAS_SF_SYNC	80	CSA source follower bias
IBIAS_KRUM_SYNC	40	Krummenacher feedback current
IBIAS_DISC_SYNC	300	Preamplifier bias current
ICTRL_SYNCT_SYNC	100	Oscillator delay line bias current
VBL_SYNC	400	Baseline voltage for offset components
VTH_SYNC	105	Threshold voltage
REF_KRUM_SYNC	450	Krummenacher voltage reference

Table 3.2: Recommended settings according to the Synchronous Front End manual [13].

is displayed in Figure 3.6(e). The performance of this circuit can be influenced by the currents and voltages supplied. The supply voltages and currents all end on "_LIN" in Figure 3.6(a) and are each controlled by an individual DAC. A short description of each DAC and the default value can be found in Table 3.3. The here mentioned voltages and currents are the ones varied in Chapter 6 "Results".

DAC Name	Recommended Value [14]	Description
PA_IN_BIAS_LIN	300	Preamplifier Bias current
FC_BIAS_LIN	20	Folded cascode branch current
KRUM_CURR_LIN	32	Krummenacher current
LDAC_LIN	130	I_{DAC} step size
COMP_LIN	110	Comparator bias current
REF_KRUM_LIN	300	Krummenacher reference voltage
Vthreshold_LIN	345	Global threshold voltage

Table 3.3: Table with recommended settings according to the Linear Front End operation manual [14].

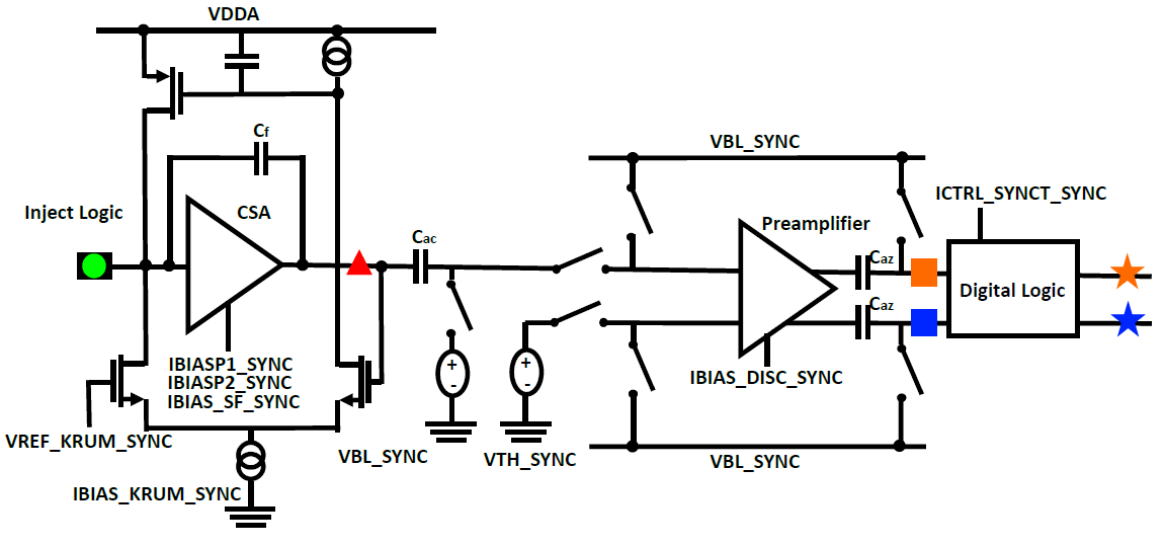
Differential Analog Front End

The Differential Front End's name is derived from its differential precomparator design. Figure 3.7(a) shows the Front End's analog circuitry. The CSA is marked as preamplifier in Figure 3.7(a). The output of the preamplifier is shown in Figure 3.7(c). This signal is processed by a differential amplifier, marked as precomparator. The precomparator amplifies the two signals and shifts the signals up or down based on the global and local threshold parameters. The precomparator output is then processed by the comparator for further digitization, as Figure 3.7(e) shows. The crossing points of the two differential signals shown in Figure 3.7(d) hereby correspond to the threshold. As long as the orange signal is higher than the blue signal, the comparator signal remains low, as soon as the blue signals gets larger than the orange signal, the comparator signal gets high. The performance of this circuit can be influenced by the currents and voltages supplied. The supply voltages and currents all end on "_DIFF" in Figure 3.7(a) and are each controlled by an individual DAC. A short description of each DAC and the default value can be found in Table 3.4. The here mentioned voltages and currents are the ones varied in Chapter 6 "Results".

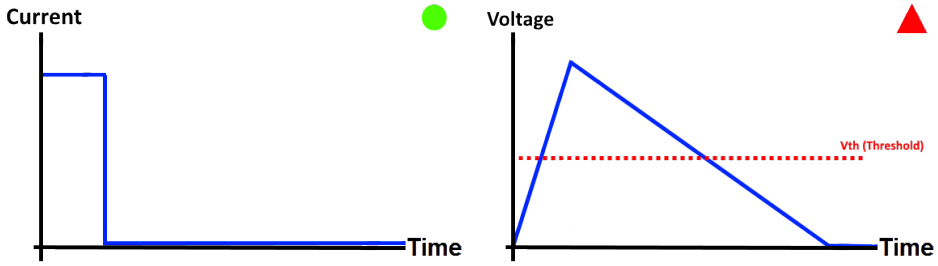
The performance of this circuit can be influenced by the currents and voltages supplied at the corresponding DAC. A short description of each DAC and the default value can be found in Table 3.4.

DAC Name	Recommended Value [15]	Description
PRMP_DIFF	533	Preamp input stage current
FOL_DIFF	542	Preamplifier output follower current
PRECOMP_DIFF	512	Precomparator tail current
COMP_DIFF	528	Comparator total current
VFF_DIFF	140	Preamp feedback current
VTH1_DIFF	200	Negative branch voltage offset
VTH2_DIFF	100	Positive branch voltage offset
LCC_DIFF	20	Leakage current compensation current

Table 3.4: Table with recommended settings according to the Differential Front End operation manual [15].

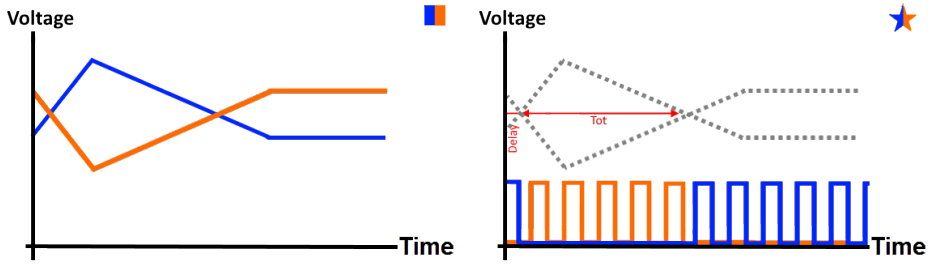


(a) Synchronous Front End Schematics



(b) Injection Signal

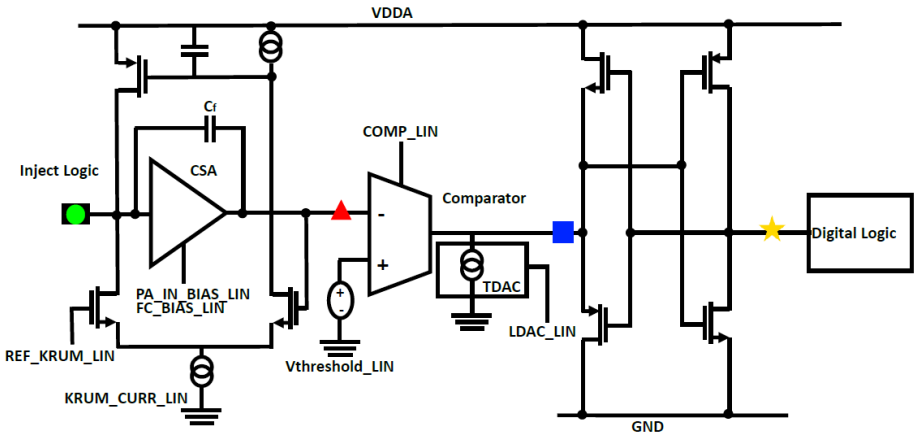
(c) CSA Output



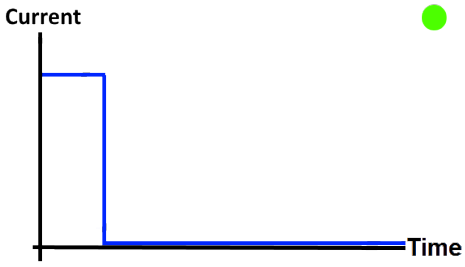
(d) Differential Amplifier Output

(e) Latch Output

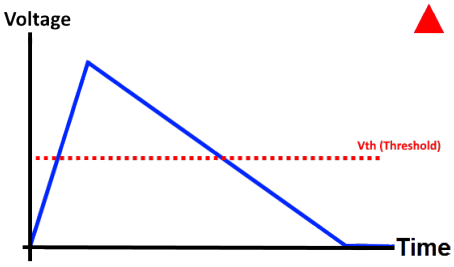
Figure 3.5: 3.5(a) Schematics of the Synchronous Front End's analog part [13]. From left to right the current input via detector diode or injection input, a charge sensitive amplifier, a differential amplifier and the latch, which digitizes our analog signal is visible. 3.5(b) Signal coming from the sensor diode. 3.5(c) Signal after the preamplifier. 3.5(d) Two output signals of the differential amplifier. 3.5(e) Digitized signal after the Latch.



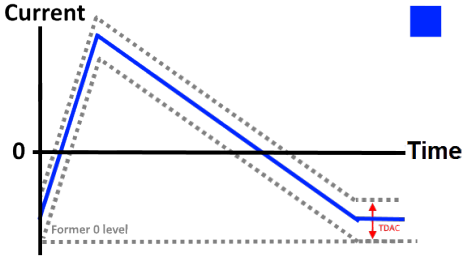
(a) Linear Front End Schematics



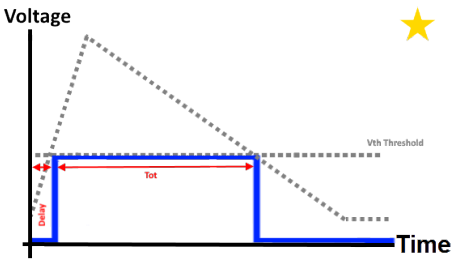
(b) Injection Signal



(c) CSA Output

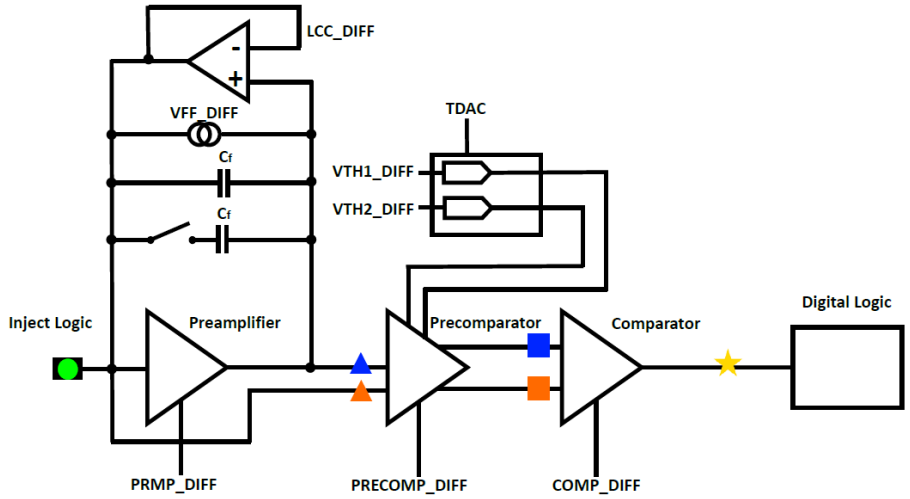


(d) Trans-conductance (Discriminator) Output

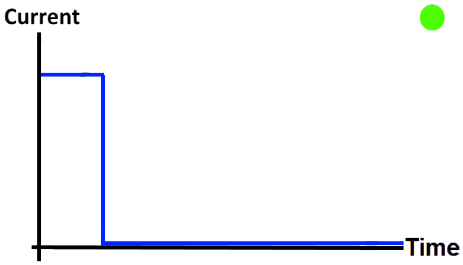


(e) Comparator Output

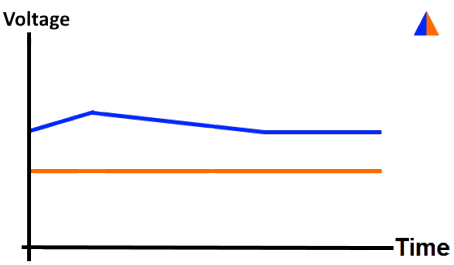
Figure 3.6: 3.6(a) Schematics of the Linear Front End's analog part [14]. From left to right the charge input via detector diode or injection input, a charge sensitive amplifier, a trans-conductance stage and the discriminator, which outputs the analog signal for digitization is visible. 3.6(b) Signal produced from the sensor diode. 3.6(c) Signal after the CSA. 3.6(d) Output signals of the trans-conductance stage. 3.6(e) Signal after the comparator.



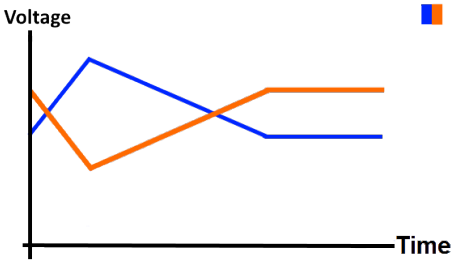
(a) Differential Front End Schematics



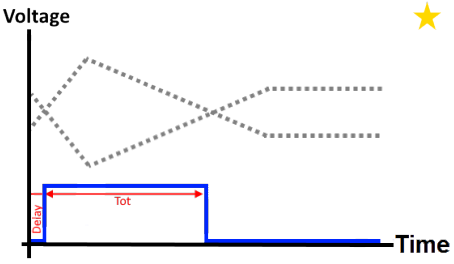
(b) Injection Signal



(c) Preamplifier Output



(d) Precomparator Output



(e) Comparator Output

Figure 3.7: 3.7(a) Schematics of the Differential Front End's analog part. From left to right the current input via detector diode or injection input, a charge sensitive amplifier, a differential precomparator and the comparator is visible. 3.7(b) Signal coming from the sensor diode. Figure 3.7(c) Signal after the preamplifier. 3.7(d) Output signals of the precomparator. 3.7(e) Digital signal after the comparator.

CHAPTER 4

Setup

For the characterization of RD53A two major data acquisition systems (DAQs) have gained popularity within the RD53 community. One of them is BDAQ53 - developed at Silab - University of Bonn and one is developed by the Lawrence Berkeley National Laboratory in Berkeley. This DAQ is called YARR. Both Setups will be compared on the analysis and data readout level. Figure 4.1 shows the comparison setup. On the left the RD53A single chip card is displayed. This card is identical for both BDAQ53 and YARR measurements. The data is then taken once with YARR and once with BDAQ53. The outcome is then compared with the same analysis software in order to eliminate fitting, plotting and interpretation errors. However, first of all the function of the analysis software has been verified. For this test simulated data was created to compare the outcome of the analyzed data between both DAQs.

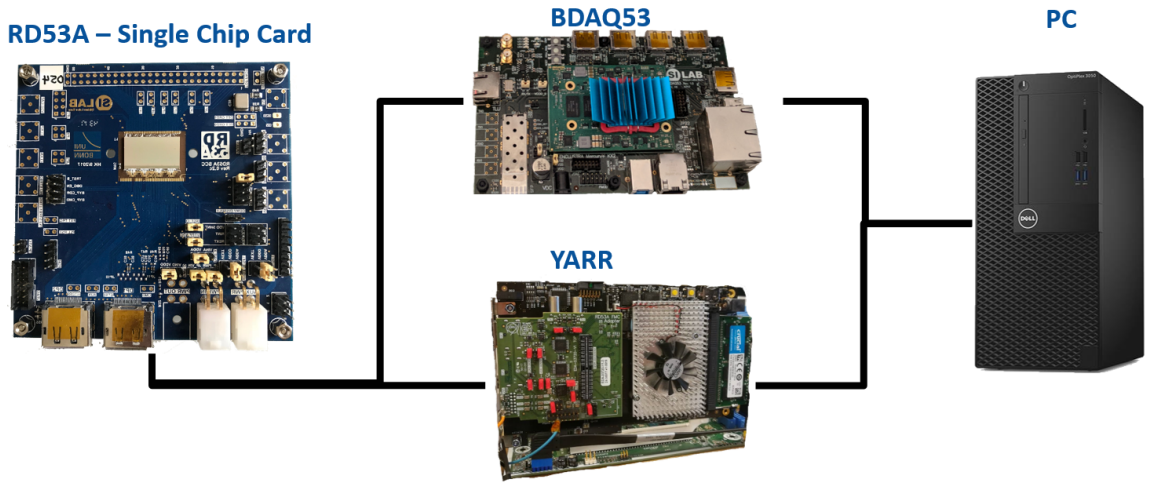


Figure 4.1: Sketch of the used setups during all measurements presented in this thesis. On the left a single chip card with RD53A, with the two readout systems BDAQ53 (top) and YARR (bottom) as well as the readout PC on the right.

4.1 Single Chip Card

The single chip card (SCC) is a printed circuit board, which carries a single RD53A as shown in the center of Figure 4.2. On the bottom the connectors for power and DAQ communication are visible. The negative temperature thermistor (NTC) right next to the chip is used for temperature measurements. Other than that the SCC houses all components to configure the chip via jumpers and measure internal signals via external pads.

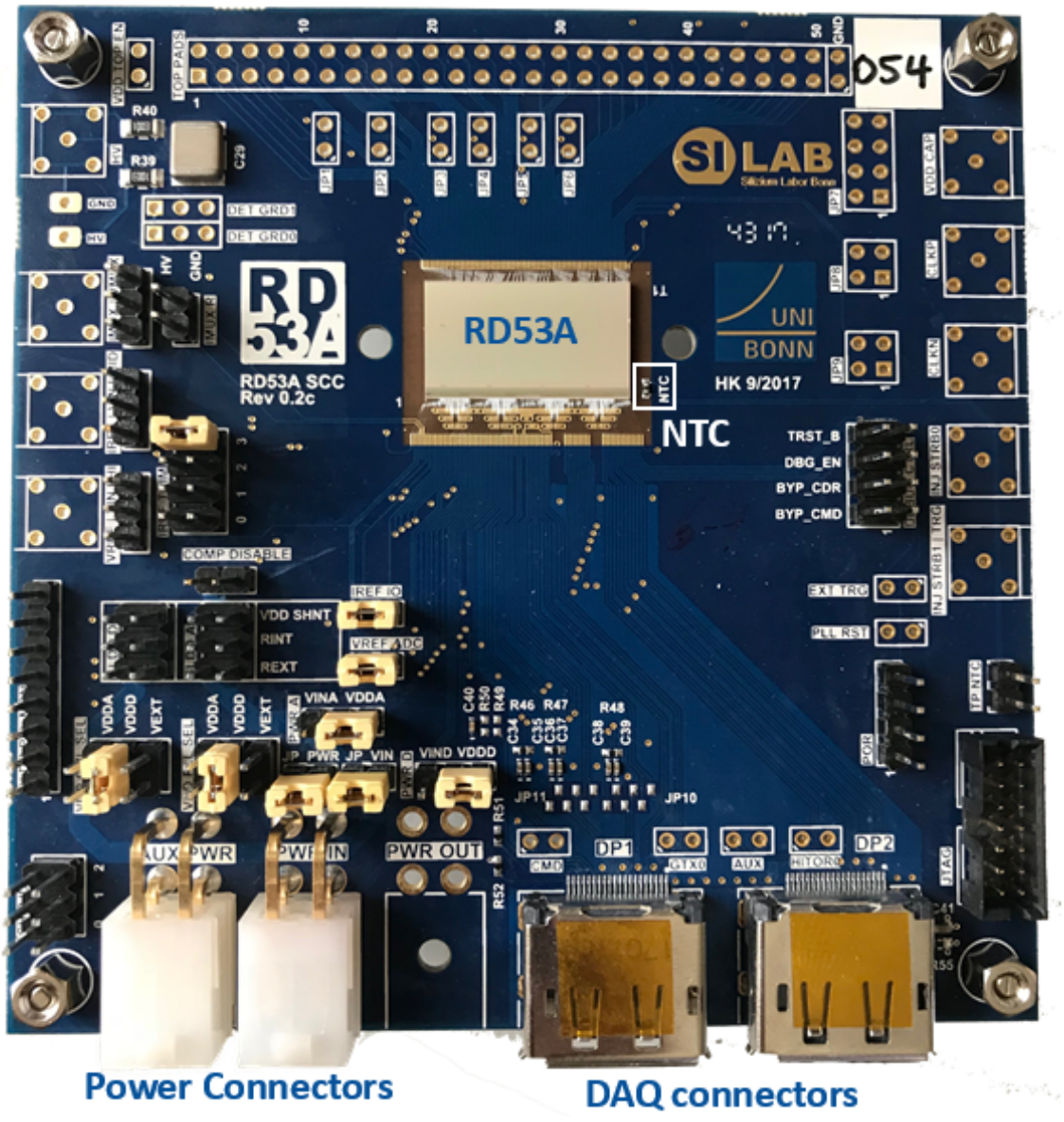


Figure 4.2: Single Chip Card (SCC) with mounted RD53A and its most important connectors and the negative temperature thermistor (NTC).

4.2 YARR

The YARR system is a C++ based DAQ with emphasis on high universality with full detector scalability in mind. Thanks to its slim and modular C++ design it is able to support older chip generations such as the FE-I4 and Fe65-P2. For computer communication YARR uses four PCIe lanes. For communication with RD53A it houses four Mini-DisplayPorts, which are mounted on an FMC adapter card. The adapter card is mounted on a commercial PCIe FPGA card, such as the Trenz TEF-1001. Figure 4.3 shows the whole YARR board, with the PCIe connector on the bottom, the Mini-DisplayPort adapter card on the left, the Kintex 7 FPGA in the center and a common 6 pin power connector on the top right.

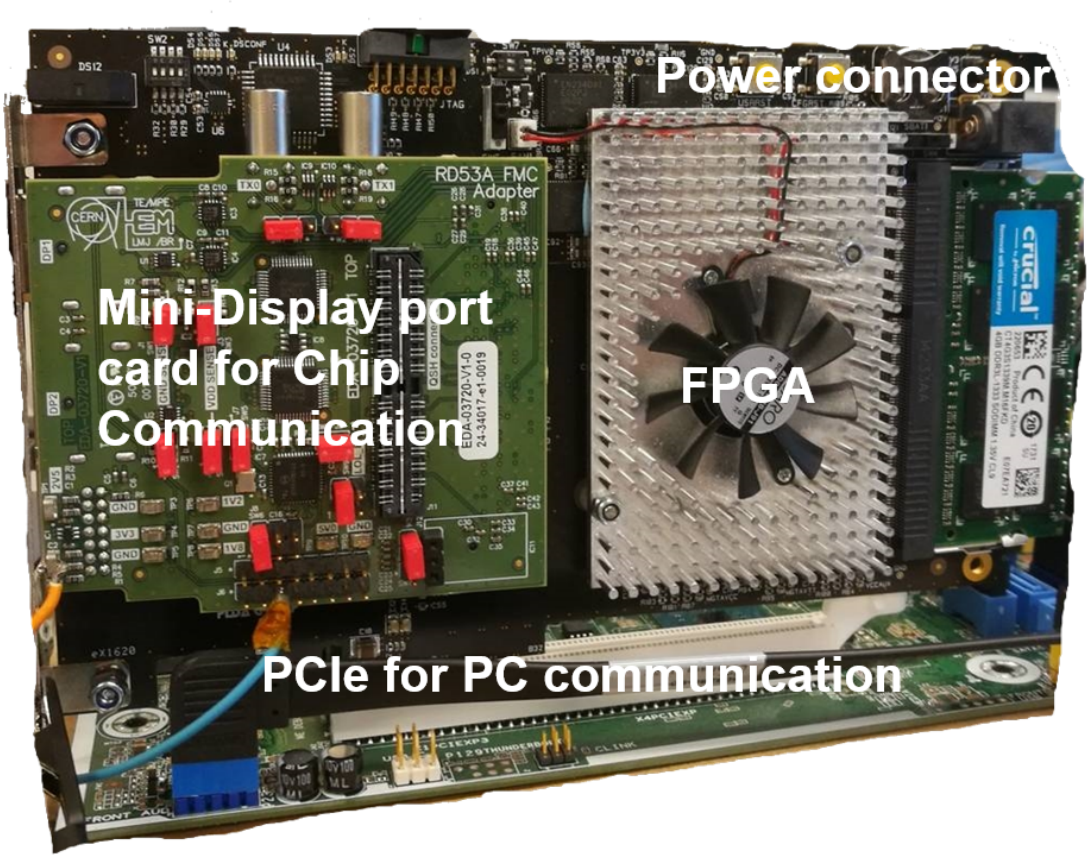


Figure 4.3: YARR-FPGA board with an FMC to Mini-DisplayPort adapter card. The most important connectors for power, computer communication and chip communication are labelled at the corresponding positions.

4.3 BDAQ53

The BDAQ53 system is a Python based data acquisition system (DAQ) which is specifically designed for chip debugging and testing purpose with emphasis on lab testing in terms of quick debugging

feedback. Thanks to its integrated plotting class as well as highly modular Python design it enables users to quickly adapt scans to their needs without the need to touch deeper code abstraction layers. The BDAQ53 hardware is composed of a comercial FPGA-board on a custom baseboard. This is used to establish communication with the computer via TCP/IP over an RJ-45 port as shown in the bottom of Figure 4.4. In the center of the figure the FPGA with its mounted cooler is visible. The used FPGA is a Kintex 7, which is supplied with power using the bottom 5V power connector, alternatively the USB port can be used for powering. On the top the board features four DisplayPort connectors. These are used to connect to the RD53 single chip card, which is illustrated in Figure 4.2. These can be used to readout up to four chips. All BDAQ53 measurements shown in this thesis have been conducted with this hardware platform.

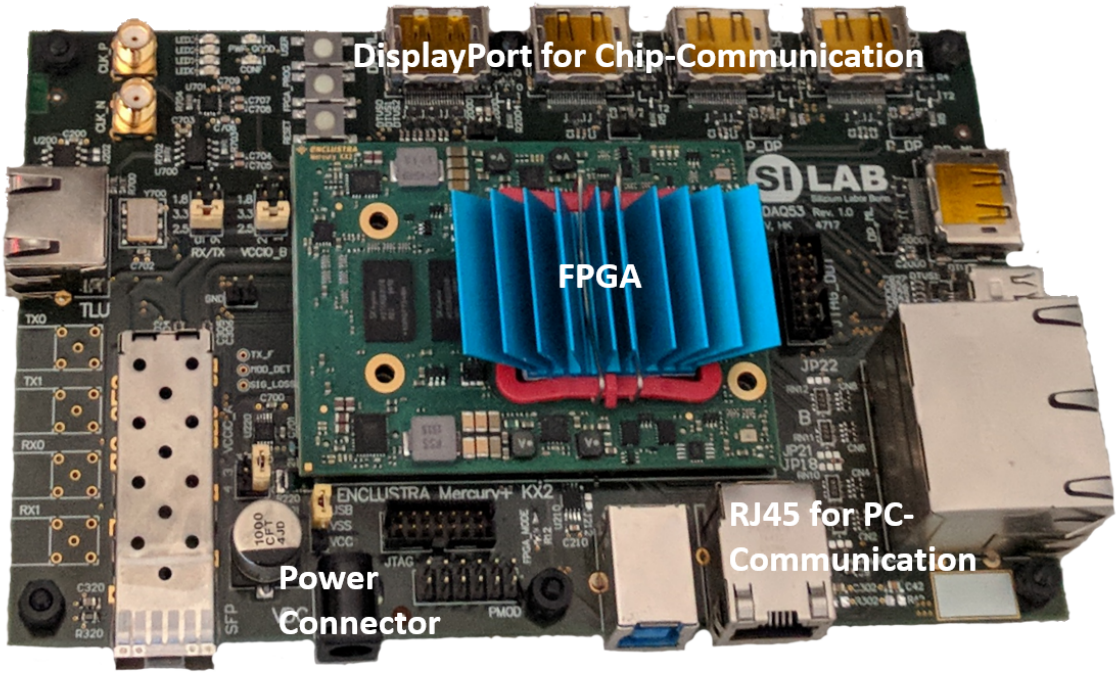


Figure 4.4: BDAQ53 board with its main FPGA component in the middle, and the most important connectors for power, computer communication and chip communication labelled at the corresponding positions.

4.4 Analysis Comparison

Both DAQs have an integrated analysis class. In YARR the raw data is live analyzed, the raw binary data is not saved. This leads to a decrease of storage consumption. In BDAQ53 the raw binary data is stored to disk and analyzed offline. This allows for simple and uncomplicated re analysis of all scans. To verify the functionality of the analysis classes, the results of both systems were compared after entering the same raw data. Both analysis classes delivered the same results based on the same analog scan raw data. This means that plain raw data analysis is identical in both systems. The functionality

of an analog scan is explained in Section 5.3. To compare the fitting during a threshold scan, which is explained in Section 5.4. A comparison based on simulated ideal threshold data was conducted. The comparison of the fitting routines can be found in Table 4.1. Two sets of simulated data were produced, one with 10 e-steps and one with 50 e- steps. The Start-Parameters column displays the parameters specified in the simulation, which is the expected outcome for both analysis routines. The Threshold- and Noise- Mean hereby corresponds to the mean threshold and noise of all pixels within the matrix, while the Threshold- and Noise- Sigma corresponds to the sigma over all pixels within the matrix.

	Start-Parameters [e-]	YARR [e-]		BDAQ53 [e-]	
Step-Size		10 e-	50 e-	10 e-	50 e-
Threshold Mean	1000.00 e-	999.94 e-	1000.59	999.94 e-	1000.49
Threshold Sigma	100.00 e-	101.04 e-	101.92	100.95 e-	101.72
Noise Mean	75.00 e-	74.83	74.38	70.66	71.36
Noise Sigma	10.00 e-	10.78	11.57	10.17	10.49

Table 4.1: BDAQ53 vs. YARR fit comparison Table. Both DAQs deliver agreeing results, except for a slight noise underestimation in BDAQ53.

Table 4.1 shows matching results for threshold means and sigmas. However, for the noise estimation we see a systematic underestimate of noise of around $\sim 5\%$ in BDAQ53. Despite the higher accuracy of the YARR analysis class, all comparison scans between YARR and BDAQ53 were analyzed with the BDAQ53 analysis class, due to its capability to analyze data offline. Additionally all plots were produced with the BDAQ53 internal plotting class in order to unbias visual comparison. Two types of scans will be compared for each Front End. First of all an analog scan, explained in Section 5.3 will be conducted.

4.5 Analog Scan Comparison

YARR and BDAQ53 both have analog scan capabilities. The analog scan procedure is explained in Section 5.3. Figure 4.5 shows the YARR scan on the left side, while the BDAQ53 scan results are displayed on the right side. For better comparability the raw data has been analyzed and plotted by the BDAQ53 analysis and plotting class.

The occupancy maps in Figure 4.5(a) and 4.5(b) show the occupancy per pixel on the z axis. The expected total occupancy is 192*400*100 = 7680000. In the YARR scan, a few pixels which have received more injections than expected are visible. Especially in the Synchronous Front End few pixels, which received zero hits are observed. In total an occupancy excess of 6000 injections in the YARR scan is visible. On the right few pixels received one more hit than expected. In total an occupancy excess of four injections in the BDAQ53 scan. Figure 4.5(c) and 4.5(d) show the ToT distribution for all enabled pixels. On the left all received hits have a high ToT value of seven and higher. On the right a similar shape is visible, with a missing ToT seven bin and additional bin at zero. The hits in bin zero corresponds to the four noise hits, which were previously mentioned in the BDAQ53 occupancy excess. Therefore those hits are expected to be noise hits. Figure 4.5(e) and 4.5(f) show at what relative bunch crossing ID (BCID) which hit occurred. One BCID hereby corresponds to a time window of 25ns, which indicates when each hit occurred. On the left all hits were received within six BCIDs, while the right indicates to receive all hits within five BCIDs. The shape of mentioned five

BCIDs is the same. Therefore bin six in Figure 4.5(e) is suspected to contain most of the excess 6000 injections. This indicates non optimized timing of the injection with systematic additional injections in YARR. The offset between the two graphs is caused by the sending of different trigger patterns (16 for YARR and 32 for BDAQ53).

4.6 Threshold Scan Comparison

This chapter contains the comparison of YARR and BDAQ53 threshold scans. How a threshold scan works is explained in Section 5.4. The threshold scans will be compared for each Front End individually. The Differential Front End was operated over the whole matrix. Tables 4.2, 4.3 and 4.4 show a summary of all measured values. Before each scan the corresponding Front End was tuned to 1500 e- either with YARR or BDAQ53. The configuration file including all DAC settings and pixel masks were then converted into the corresponding other readout systems input format.

Front End		Synchronous Front End			
Tuning	Threshold Scan	Th. Mean	Th. Disp.	Noise Mean	Noise Disp.
	BDAQ53	1403 e-	76 e-	82 e-	8 e-
	YARR	1555 e-	89 e-	90 e-	10 e-

Table 4.2: Outcome of a threshold scan once for YARR and once for BDAQ53 for the Synchronous Front End

Table 4.2 shows a threshold scan conducted with YARR and with BDAQ53, with the same Front End register values and the same masking. The YARR scan features significantly more noise, at higher noise- and threshold- dispersion. The mean threshold also increases by $\sim$ 150 e-. This is an additional hint to the non optimized injection timing, especially, since the Synchronous Front End's threshold (-dispersion) and noise (-dispersion) strongly depends on the injection timing. Figure 4.6 shows that the YARR injection is constantly scattered over at least two BCID, while in BDAQ53 the injection timing is consistently in one single BCID.

Front End		Linear Front End			
Tuning	Threshold Scan	Th. Mean	Th. Disp.	Noise Mean	Noise Disp.
BDAQ53	BDAQ53	1515 e-	58 e-	68 e-	7 e-
BDAQ53	YARR	1598 e-	107 e-	77 e-	10 e-
YARR	BDAQ53	1474 e-	107 e-	70 e-	7 e-
YARR	YARR	1584 e-	66 e-	78 e-	10 e-

Table 4.3: Outcome of a tuning and threshold scan for YARR and BDAQ53, conducted with the Linear Front End

Table 4.3 shows a tuning and threshold scan each conducted with YARR and BDAQ53 with the same masking and register settings for the Linear Front End. The noise and noise dispersion is consistent among the threshold scans, which were conducted with the same DAQ. The threshold dispersion is consistent among the tunings. However if the Tuning was conducted with the other DAQ the threshold dispersion rises to $>$ 100 e-. Here the same injection timing effect as discussed for the Synchronous Front End is observed. Additionally a threshold gradient as displayed in Figure 4.7

can be observed for any threshold scan conducted with the opposite DAQ than the tuning. From this we can conclude, that the YARR tuning is capable of compensating the injection delay. This also explains our similar results in threshold and threshold dispersion when comparing YARR/YARR and BDAQ53/BDAQ53 data. All in all both DAQs produce acceptable tunings for the Linear Front End. The configuration and masking is however due to timing differences not interchangeable.

Front End		Differential Front End			
Tuning	Threshold Scan	Th. Mean	Th. Disp.	Noise Mean	Noise Disp.
BDAQ53	BDAQ53	1559 e-	57 e-	40 e-	5 e-
BDAQ53	YARR	1565 e-	63 e-	39 e-	5 e-
YARR	BDAQ53	1609 e-	53 e-	40 e-	5 e-
YARR	YARR	1617 e-	55 e-	39 e-	5 e-

Table 4.4: This table shows the outcome of a tuning and threshold scan for YARR and BDAQ53, conducted with the Differential Front End

Table 4.4 shows a tuning and threshold scan each conducted with YARR and BDAQ53 with the same masking and register settings for the Differential Front End. Here agreement between the DAQs in terms of threshold (-dispersion), as well as noise (-dispersion) is observed. However looking at the BCID plot in Figure 4.8 the same behavior as observed in Figure 4.6 is visible. An additional BCID bin below the four dominant bins. The large BCID dispersion originates from a large timing dispersion, which is a characteristic of the Differential Front Ends Comparator in R53A described in Appendix A.2. At the same time this is the reason for the small impact on threshold and tuning, since the inter pixel timing dispersion is more dominant than the timing dispersion introduced by the DAQ. This hypothesis is confirmed by Figure 4.9, which shows the same threshold gradient over the pixel matrix as the Linear Front End in Figure 4.7 for YARR threshold scans.

4.7 Conclusion

Both DAQs are capable of operating the chip. The produced results are within the expected errors, as long as each scan is conducted with each DAQ's native tuning. Differences in DAQ clocking speed, command composition and fitting however lead to differences in the operation and tuning of the chip. Therefore tuning masks and register configuration are not interchangeable. Due to the homogeneous injection of BDAQ53 this DAQ will be used throughout the rest of the thesis.

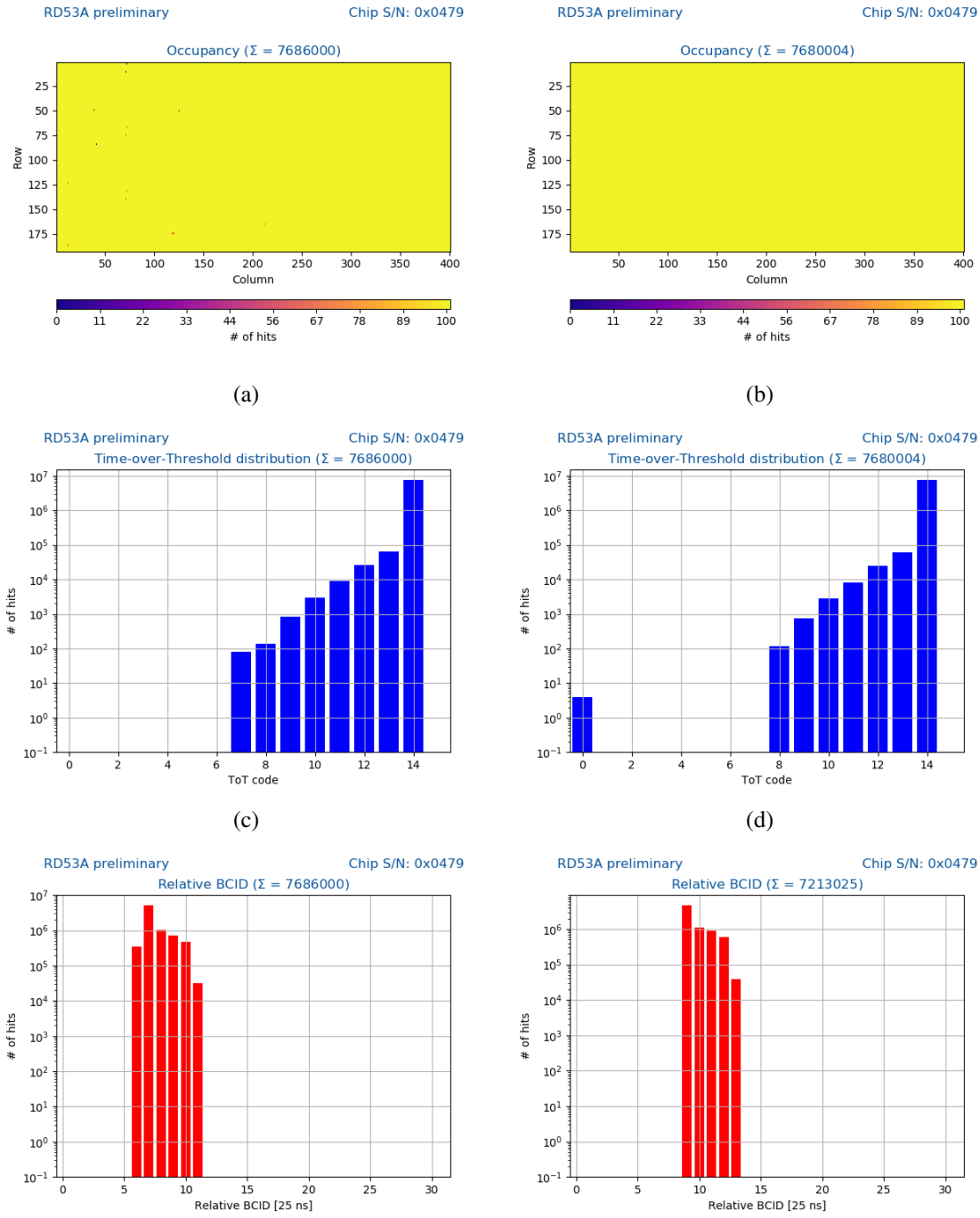
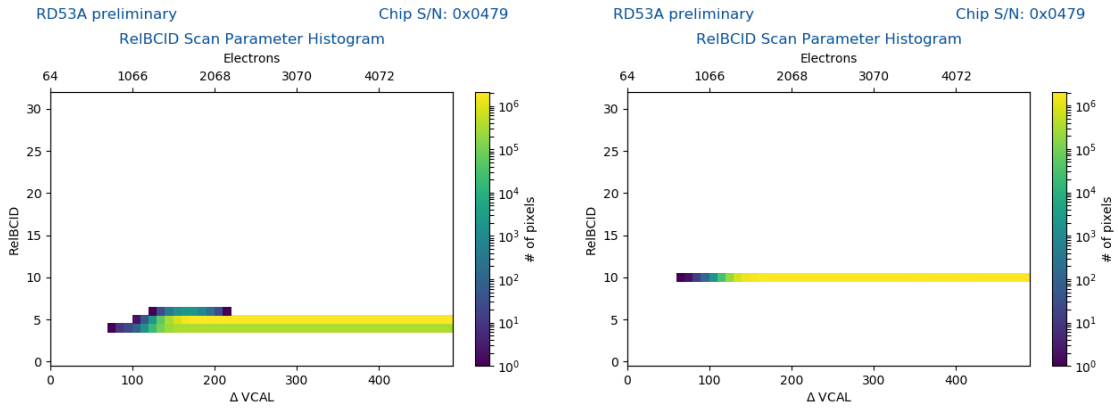
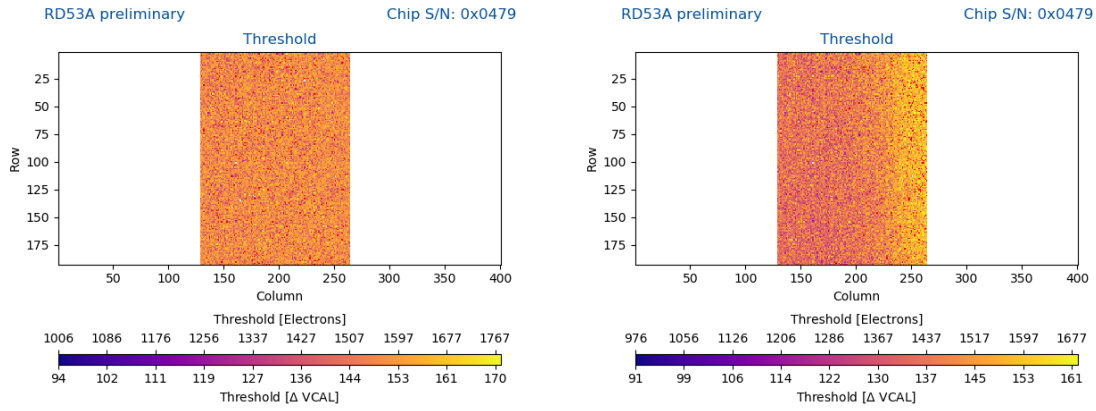


Figure 4.5: Analog scan comparison between YARR (left) and BDAQ53 (right). 4.5(a) and 4.5(b) show the occupancy per pixel. 4.5(c) and 4.5(d) show the ToT distribution of all pixels. 4.5(e) and 4.5(f) show the BCID distribution for all pixels.



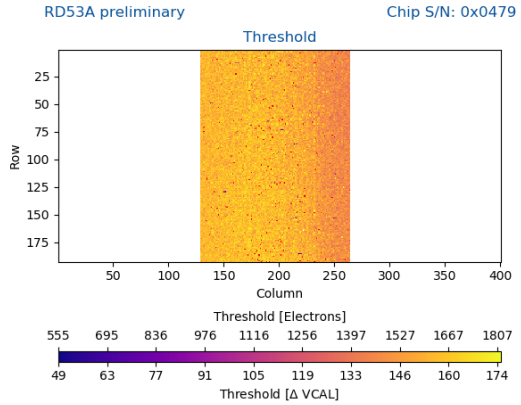
(a) (b)

Figure 4.6: 4.6(a) BCID distribution over all injected charges for YARR. Figure 4.6(b) shows the same plot for BDAQ53.

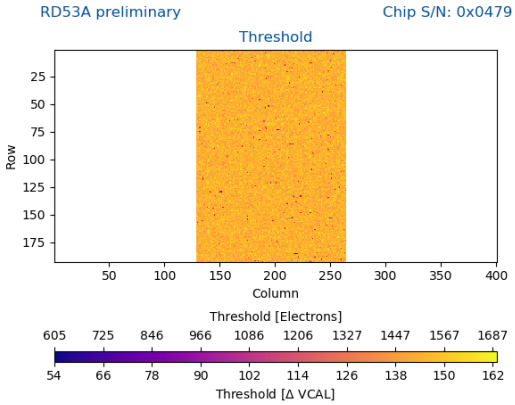


(a)

(b)

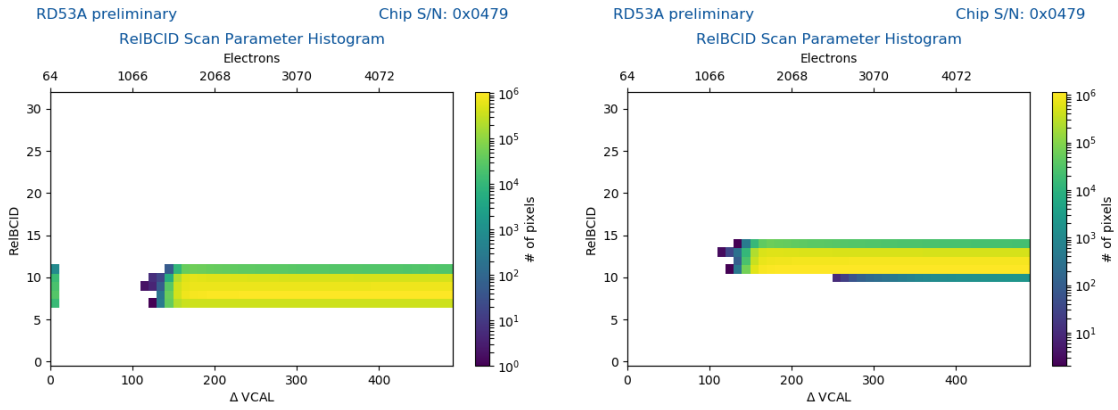


(c)



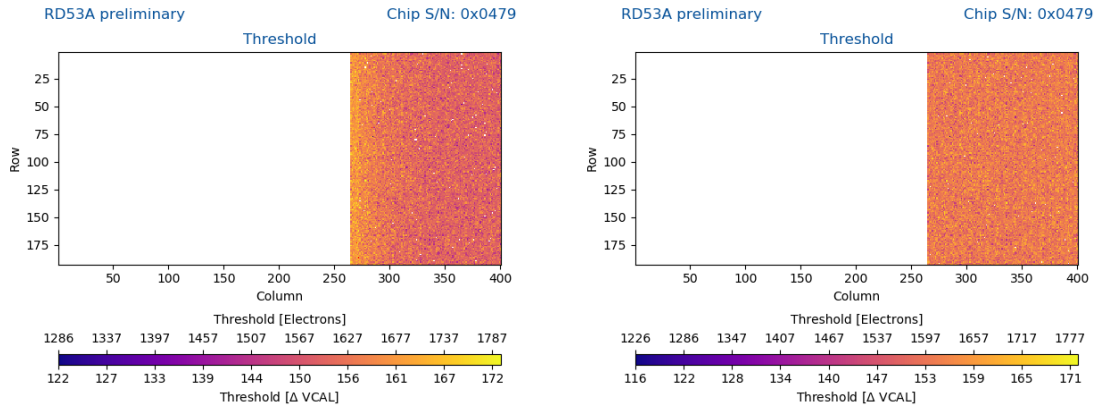
(d)

Figure 4.7: 4.7(a) Threshold map for a YARR tuning and YARR threshold scan. 4.7(b) threshold map for a YARR tuning and BDAQ53 threshold scan. 4.7(c) threshold map for a BDAQ53 tuning and YARR threshold scan. Figure 4.7(d) shows the threshold map for a BDAQ53 tuning and BDAQ53 threshold scan. All measurements were conducted with the Linear Front End.



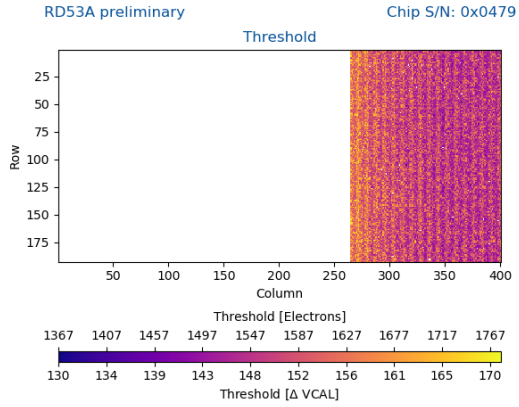
(a) (b)

Figure 4.8: 4.8(a) BCID distribution over all injected charges for a BDAQ53 tuning and YARR threshold scan. 4.8(b) Same plot for a BDAQ53 threshold scan.

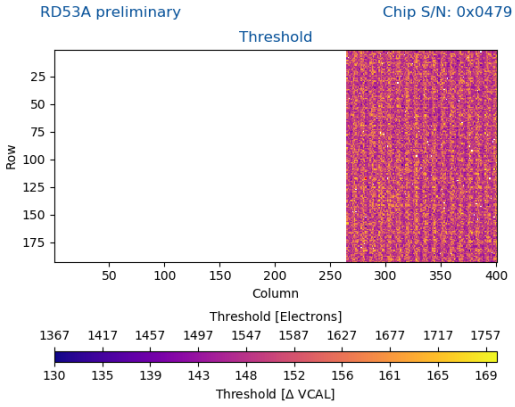


(a)

(b)



(c)



(d)

Figure 4.9: 4.9(a) Threshold map for a YARR tuning and YARR threshold scan. 4.9(b) Threshold map for a YARR tuning and BDAQ53 threshold scan. 4.9(c) Threshold map for a BDAQ53 tuning and YARR threshold scan. 4.9(d) Threshold map for a BDAQ53 tuning and BDAQ53 threshold scan. All measurements were conducted with the Differential Front End

CHAPTER 5

Measurement Routines

In this chapter all measurement routines used during this thesis will be introduced. Each scan will be discussed with respect to its technical realization and its output parameters using exemplary output plots.

5.1 ADC Non-Linearity Scan

The non-linearity scan is used to estimate the relative linearity and non-linearity of RD53As internal ADC for different trim bit settings. It is not designed to make final performance conclusions concerning the absolute differential or integral non-linearity of the ADC. The routine is using a high precision low noise Digilent DA3 16-bit DAC, with an inaccuracy of ±1 bit [16]. The integral non linearity is defined as the maximum deviation from the ideal straight line of the ADC, a mathematical representation of this is shown in Equation 5.2 [17]. The differential non linearity is a measure of the homogeneity of the ADC's subsequent digitization, a mathematical representation of this is shown in Equation 5.1 [17].

To measure the non-linearity of RD53As internal ADC, the signal of the corresponding Digilent DAC is routed to the ADC and measured for each single value of the DAC. This high resolution is crucial in order to estimate the step width between each ADC bit. After acquiring the data, a linear fit is applied and the step width between each data point is calculated. The differential non-linearity (DNL) shows the difference in step width in relation to the previous step. It is calculated as shown in Equation 5.1. Figure 5.1(b) shows the corresponding output. Figure 5.1(c) shows the integral non-linearity (INL) which is the sum of all DNL's up to this point.

$$\mathrm{DNL}(x) = s(x) - s(x-1) - 1LSB \qquad s(x) := \text{step size} \tag{5.1}$$

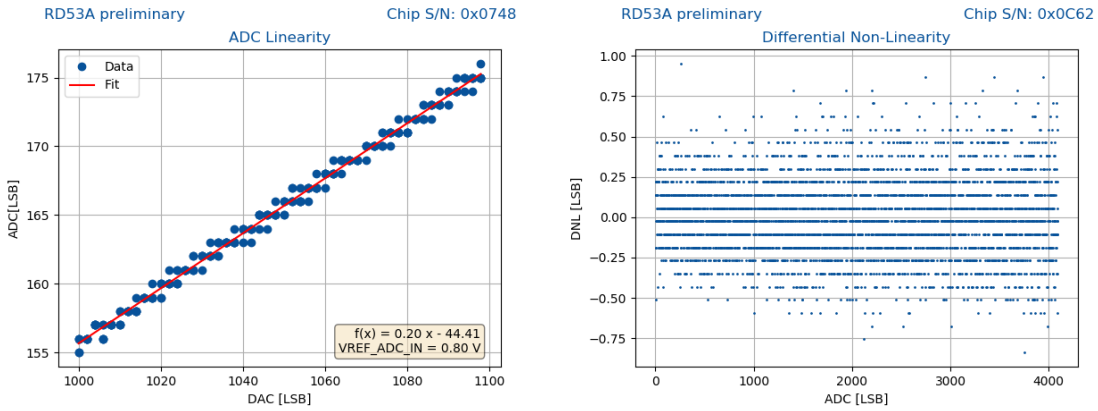
$$\mathrm{INL}(x) = \sum_{n=0}^{x} \mathrm{DNL}(n) \tag{5.2}$$

In order to estimate the non-linearity of the integral ADC, the input of the ADC is routed to an external pad on the single chip card. The external DAC is then connected to the pad and changes its voltage bit by bit over the whole ADC range. The resolution of the external DAC is higher than the one of the internal ADC which leads to the acquisition of a stair pattern as shown in Figure 5.1(a). This is

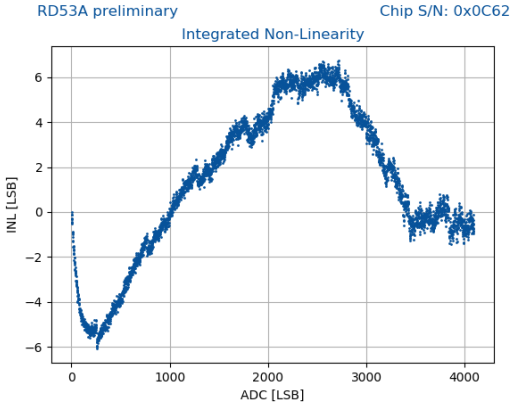
used to calculate the stair width s(x) as defined in Equation 5.1. The absolute DNL and INL of each register is then defined as shown in Equation 5.3 and Equation 5.4. The INL looks rather large in this case, which could be related to non ideal setup parameters. Therefore this measurement series will only consider relative differences between in DNL and INL between different trim bit settings. Representative absolute measurements can be found here [18], [19], [20].

$$|\mathrm{DNL}| = \max(\mathrm{DNL}) + |\min(\mathrm{DNL})| \tag{5.3}$$

$$|\mathrm{INL}| = \max(\mathrm{INL}) + |\min(\mathrm{INL})| \tag{5.4}$$



(a) (b)



(c)

Figure 5.1: 5.1(a) Magnification of the scan range. The step wise resolution of the ADC is clearly visible. 5.1(b) Differential non-linearity of the ADC over the whole scan range. 5.1(c) Integral non-linearity over the whole scan range.

5.2 Temperature Scan

The temperature scan is used to determine the N_f factor as described in Equation 3.1. This is done by measuring the voltage slope at two different bias currents of each temperature sensor in a temperature range from -40 °C to +60°C with the RD53A internal ADC. Before each scan the ADC reference voltage is tuned to 0.9V. Previous to the scan the NTC was calibrated with a Sensiron SHT-71 temperature sensor. Figure 5.2 shows the calibration curve. Both sensors measure the same temperature within two degrees of accuracy. For the NTC calibration the beta model was used [21]. To improve even heat distribution over the chip and the NTC a 3 mm thick copper plate was mounted under the single chip card covering NTC and chip. The copper plate had an additional heat sink and fan on top to optimize heat exchange with the ambient air. Before each measurement the temperature in the climactic chamber had to fluctuate less than 1 °C for 3 min in a row. Figure 5.3(a) shows the output of a temperature scan with measured NTC temperature on the x-axis and the measured internal RD53A temperatures on the y-axis. N_f was hereby estimated for each sensor individually as the average over all measurements. The error bars are calculated using Gaussian error propagation as noted in Equation 3.2.

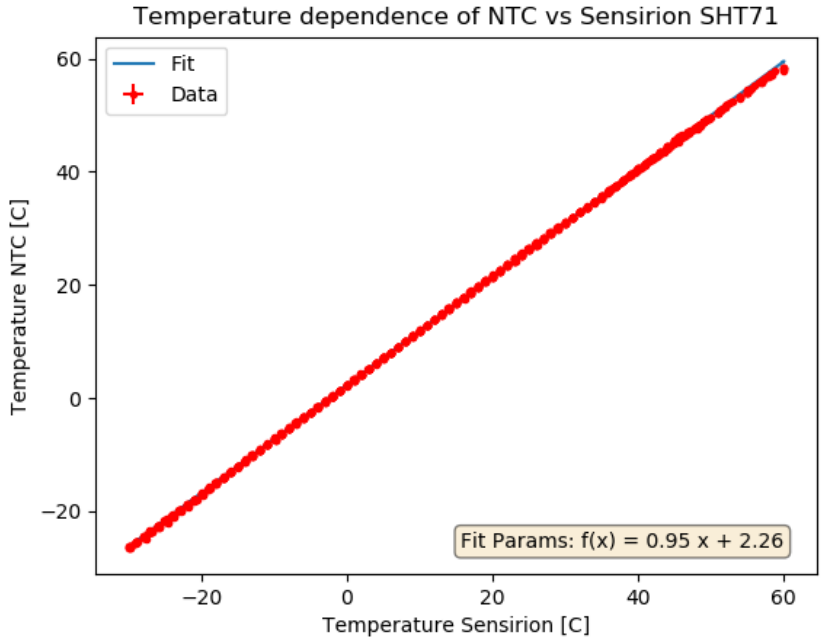
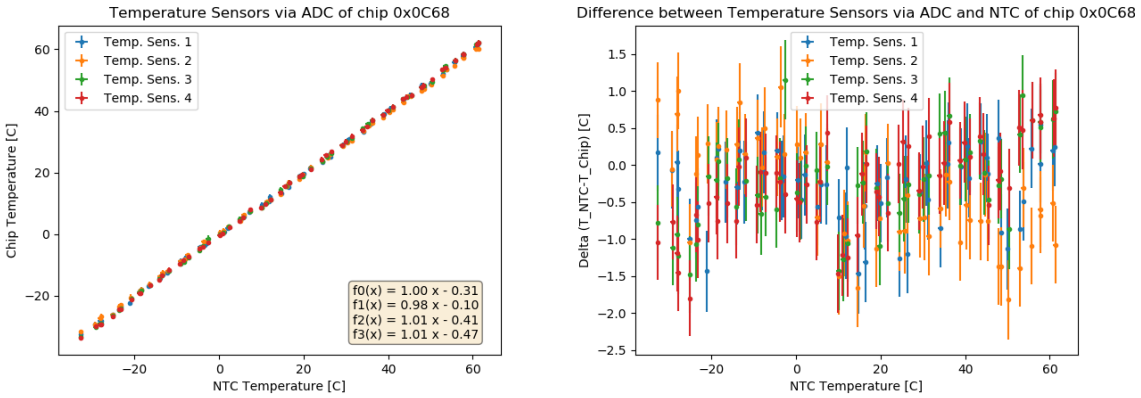


Figure 5.2: Temperature calibration curve between NTC and the Sensiron SHT-71 temperature sensor.



(a) (b)

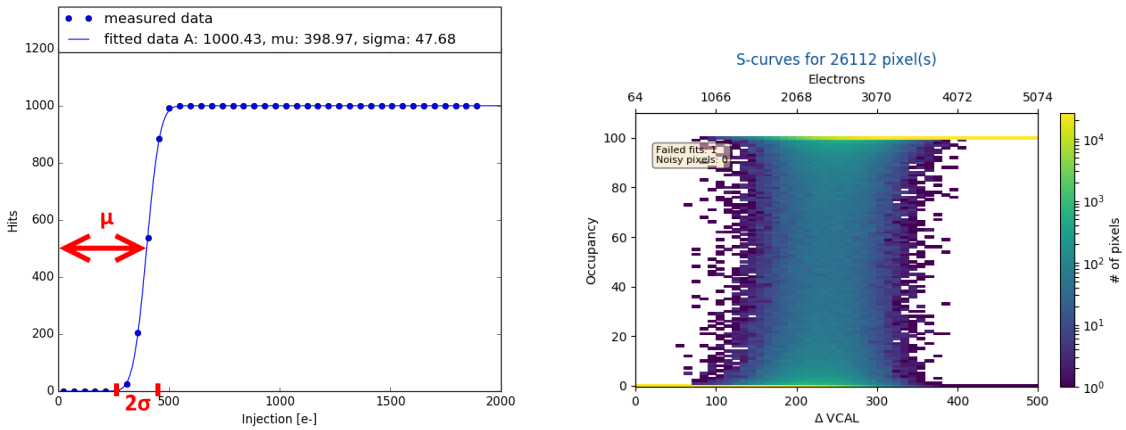
Figure 5.3: 5.3(a) Measured temperature with the external NTC and the internal temperature sensors. 5.3(b) Difference between the measured NTC and ADC temperatures.

5.3 Analog Scan

The analog scan is used to verify each pixel's analog responsiveness. This is achieved by injecting a predefined charge multiple times into each pixel. The occupancy of the scan is the sum of all injections over all pixels. In addition to that the Time over Threshold (ToT) as described in Section 3.2.2 is histogrammed. Furthermore the timing of each received injection is measured in 25 ns intervals. This timing distribution is shown in the BCID histogram as shown in Figure 4.5(f). An exemplary output of the occupancy map, ToT histogram and BCID histogram from an analog scan can be found in Section 4.5.

5.4 Threshold Scan

The threshold scan is used to measure a chip's threshold. This is achieved by one time constant configuration of the chip, while scanning over multiple injection charges. The injection voltage in the RD53A is generated by a differential injection circuit as described in [9]. The difference between the VCAL_MED and VCAL_HIGH registers is hereby proportional to the injected voltage ΔVCAL. Here one ΔVCAL step corresponds to ~10 electrons. This conversion factor has been estimated by measurements of the VCAL registers considering the injection capacitance of 8.2 fF [22].



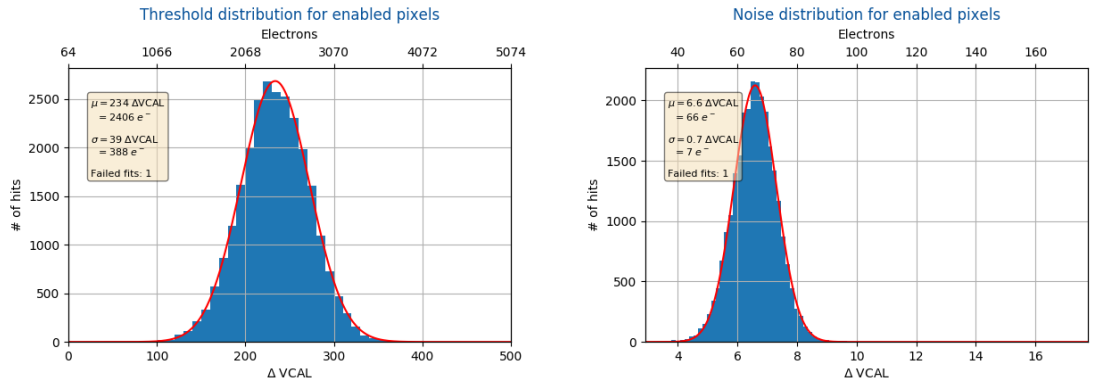
(a) (b)

Figure 5.4: 5.4(a) Amount of hits for a single pixel depending on the injected charge. The μ parameter hereby corresponds to the threshold and one σ corresponds to the noise level of the pixel. 5.4(b) Overlay of multiple pixels S-curves. All of these are fitted and histogrammed, to get a statistical feeling for the threshold dispersion over the pixel matrix.

During a threshold scan, each pixel is injected and then triggered 100 times. During analysis the injection parameter ΔVCAL (VCAL_HIGH-VCAL_MED) vs. each pixel's occupancy is plotted. From this a so called S-curve plot as shown in Figure 5.4(a) is derived. This is used to fit S-curves to each of the pixels. The mean of the S-curve hereby corresponds to the threshold (μ), while the sigma (σ) of the S-curve corresponds to the noise of the pixel, A is the height of the S-curve. Figure 5.4(b) shows the measured S-curves for all pixels. Equation 5.5 is used to fit the S-curves.

$$S - curve(x) = \frac{A}{2} \cdot \frac{erf(x-\mu)}{\sqrt{2}\sigma} + \frac{A}{2} \tag{5.5}$$

The σ and μ is then histogrammed in two separate plots in order to acquire the so called threshold and noise distribution shown in Figure 5.5(a) and 5.5(b). The mean (μ) of Figure 5.5(a) hereby corresponds to are the threshold requirement of Table 3.1. The width (σ) of the curve corresponds to the threshold dispersion and the mean of Figure 5.5(b) to the noise requirement.



(a) (b)

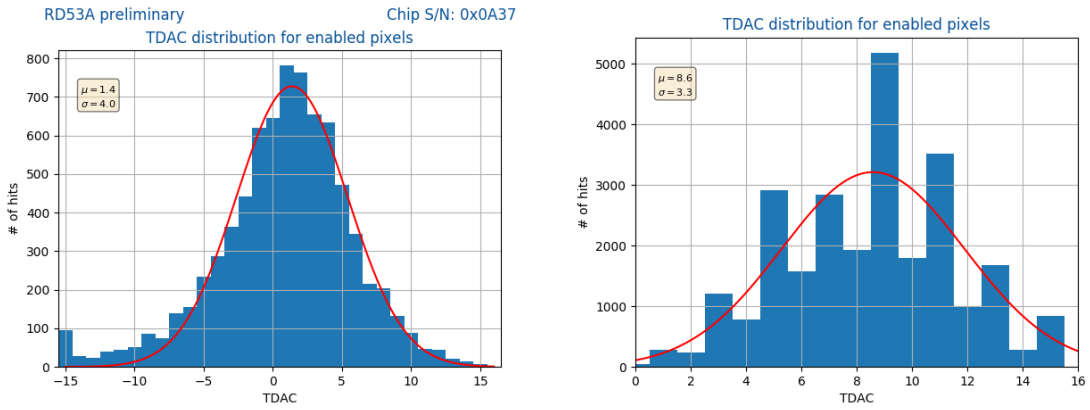
Figure 5.5: 5.5(a) Threshold distribution generated by the fit of the S-curves as described in 5.4. 5.5(b) Noise distribution. The Gaussian fits show the mean and width of the overall noise and threshold distribution of this un-tuned chip.

The Gaussian dispersion in this plot is related to process variation. Each transistor behaves differently, leading to slight voltage and charge offsets in each pixel. These inaccuracies are assumed to be Gaussian distributed, which is confirmed by the given plot. For the Gaussian fit, the fit function in Equation 5.6 is used. A hereby corresponds to the peak, with μ being the mean and σ being the width of the distribution.

$$G(x) = A \cdot \frac{e^{-(x-\mu)^2}}{2 \cdot \sigma^2} \tag{5.6}$$

5.5 Noise Tuning

The noise tuning is used to estimate the minimum stable threshold performance of each Front End. During the procedure the local threshold of each Front End (TDAC) is set to the highest possible value. Afterwards the global threshold value is lowered step by step, until 0.1% of the pixels in each Front End are noisy. From that point on the global threshold is fixed and the local threshold (TDAC) of all pixels that have zero occupancy are lowered. All pixels that now have higher occupancy than zero are shifted back up to the last TDAC setting where they had zero occupancy.



(a) (b)

Figure 5.6: 5.6(a) TDAC distribution of the Differential Front End. 5.6(b) the TDAC distribution of the Linear Front End

This process is repeated until all pixels have occupancy zero at their lowest possible TDAC setting. It is important to note, that the highest threshold in the Linear Front End corresponds to a TDAC value of 0, while a TDAC setting of 15 is the lowest possible threshold. In the Differential Front End the highest possible TDAC setting is 15 , with -15 corresponding to the minimum threshold. The Synchronous Front End solves the local threshold tuning by a procedure called auto zeroing, which is explained in Section 3.2.2. In case of the Synchronous Front End only the global threshold is tuned to the minimal value. From the noise tuning a so called TDAC mask is acquired, which is applied to each Front End to achieve the optimal TDAC settings for the lowest possible threshold. Figure 5.6(a) shows a TDAC distribution for the Differential Front End, while Figure 5.6(b) shows a TDAC distribution for the Linear Front End. The distribution in the Linear Front End has a noticeable zig-zag pattern due to a non-linearity of the TDAC least significant bit (LSB) steps.

5.6 Injection Delay Scan

The injection delay scan is used to estimate the injection delay over the pixel matrix in order to compensate for injection delay during the in-time threshold scan. Table 5.1 shows the simulated injection delay over the pixel matrix. This delay is implemented by design in order to minimize unexpected high current consumption, due to simultaneous injection. In the analysis a correction map for the row wise injection delay is derived and applied to the in-time threshold scan.

Core columns	Offsets (ns)																
0-15 (sync.)	2.3	2.0	1.6	1.4	1.2	1.0	0.8	0.8	0.4	0.4	0.0	0.0	0.2	0.6	0.9	1.2	
16-32 (lin.)	0.6	1.0	1.2	1.6	1.8	2.1	2.1	2.3	2.6	2.7	3.2	3.4	3.5	3.8	4.3	4.5	4.5
33-49 (diff.)	4.8	5.2	6.0	6.1	6.3	6.4	6.6	6.9	7.1	7.6	8.0	8.2	8.5	8.7	8.8	9.1	9.2

Table 5.1: Simulated injection delay distributed over the core columns of RD53A. [9].

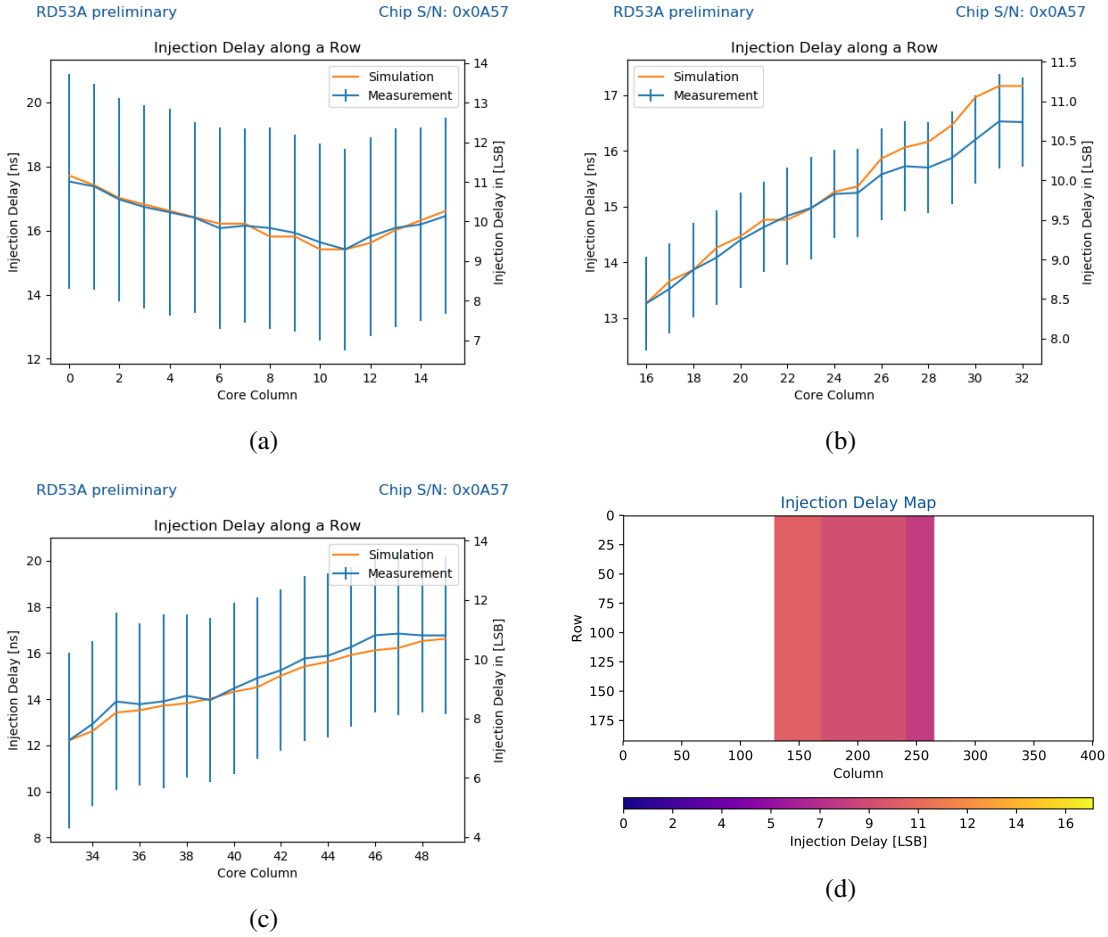


Figure 5.7: 5.7(a), 5.7(b) and 5.7(c) Injection timing as a function of core columns. The orange data is taken from Table 5.1. Figure 5.7(d) shows a timing delay map of the Linear Front End, which is generated previous to each in-time threshold scan.

Figure 5.7(a) shows the correlation between the simulated injection delay in orange and the measured injection delay in blue for the Synchronous Front End. The errorbars appear wide due to an additional timing dispersion along a pixel row and in addition to Front End specific timing dispersion. It is important to mention that the given technique only allows for relative timing measurement, which led to the decision to offset the simulated data to the lowest measured data. Good agreement between simulation and measurement is visible. Figure 5.7(b) and Figure 5.7(c) show the same measurement for the Linear and Differential Front End. Figure 5.7(d) shows an injection delay map generated by the injection delay scan, which shows the three injection timing areas of the Linear Front End. During the in-time threshold scan the injection timing will be adjusted based on this measurement.

5.7 In-Time Threshold Scan

The in-time threshold scan is used to measure the charge which each Front End can detect within 25ns after injection. It operates just like a threshold scan. It adjusts the injection timing based on the timing map as shown in Figure 5.7(d). In the analysis only hits, which are received within a 25 ns time window are considered. After applying the injection timing criterions, the output of this scan looks just like the one of the threshold scan, as shown in Section 5.4. The mean and the standard deviation are again estimated with a Gaussian fit according to Equation 5.6.

5.8 Power Scan

The power scan is used to measure the current consumption per pixel. RD53A has two main power distribution circuits in order to minimize the noise coupling from digital into analog components. The voltage for both analog and digital components should be around 1.2 V. In order to estimate the power consumption of a single pixel, both currents are measured. However the chip has many other components which are consuming power and are responsible for communication and vital chip functions. Those can therefore not be deactivated. Instead an offset current measurement is conducted. The offset (O) is estimated by minimizing the power consumption of the pixel matrix. Followed by this measurement, the pixel matrix is activated and a second measurement is conducted (P). Here the current consumption of the whole chip including the pixel matrix is measured. The difference between the two measurements divided by the amount of active pixels (N) then gives the current consumption per pixel A(N). Equation 5.7 summarizes the approach.
There are two methods to deactivate a Front End. The Synchronous and Linear Front End have the option to deactivate individual pixels with a deactivate bit, which interrupts their power supply. The Differential Front End has no such register and therefore is deactivated by setting all analog Front End related biases to 0.

$$A(N) = \frac{P - O}{N} \tag{5.7}$$

5.9 Time-over-Threshold Scan

This scan is designed to measure the time over threshold as a function of discharge current over the charge integrating capacitance in the preamplifier. These capacitances are labeled as C_f in the Figures 3.5(a), 3.6(a), 3.7(a). The scan injects a constant charge into the pixels and measures the ToT as a function of discharge current. Figure 5.8 shows this behavior for all three Front Ends. The scan parameters can be found in Appendix A.1. Figure 5.8(a) and Figure 5.8(b) show an increase of ToT for high settings in the register, which is not expected. This effect limits the usable register range to (0,160] for the Synchronous Front End and (0,130] for the Linear Front End. These plots give the register range, which will be used during ToT tuning Section 5.10.

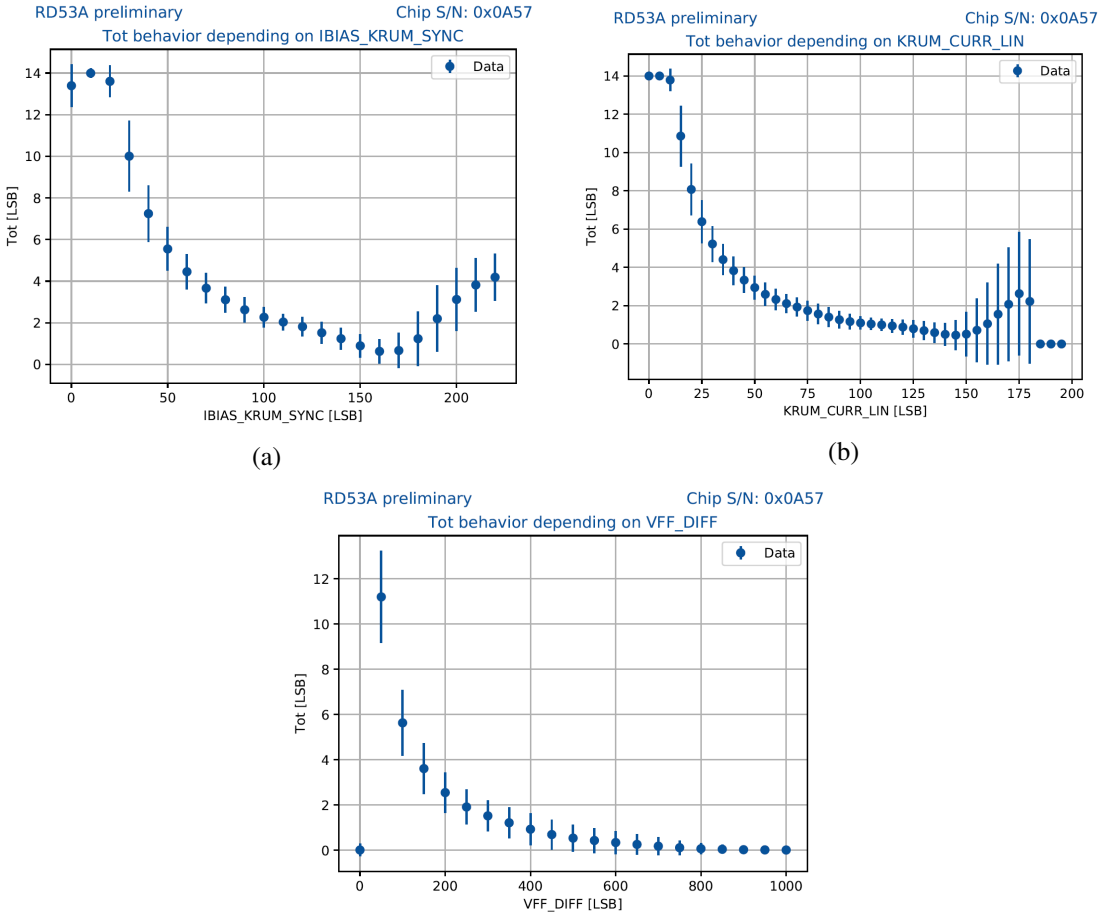


Figure 5.8: 5.8(a) ToT behavior of the Synchronous Front End as a function of the discharge current register IBIAS_KRUM_SYNC, 5.8(b) ToT behavior of the Linear Front End as a function of the discharge current register KRUM_CURR_LIN. 5.8(c) Same measurement for the Differential Front End as a function of the discharge current register VFF_DIFF.

5.10 Time over Threshold Tuning

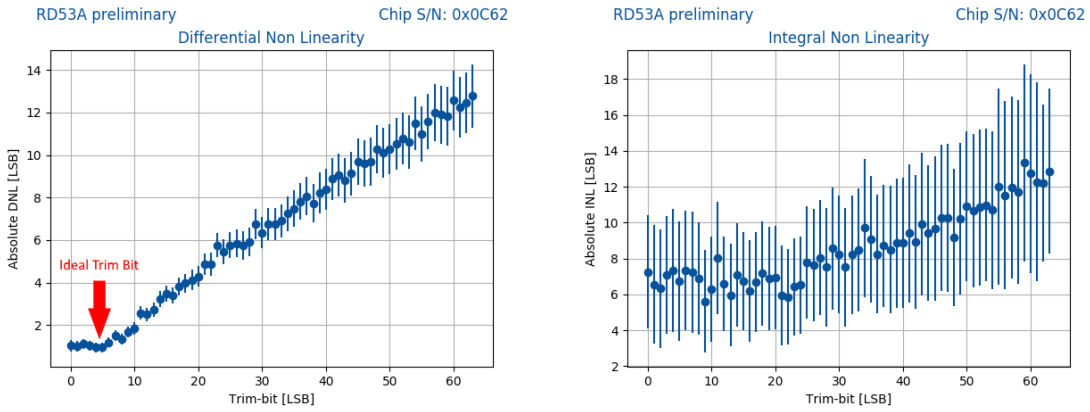
The Time over Threshold (ToT) tuning algorithm is used to tune the charge integrating capacitance (C_f) discharge current of each Front End to the corresponding discharge value. For that a binary search algorithm is used. This narrows down the ideal ToT setting for the requested charge. During the scan a constant charge is injected into each pixel. Afterwards the mean ToT is measured. This mean is compared to the target ToT and based on that the corresponding discharge current registers: IBIAS_KRUM_SYNC, KRUM_CURR_LIN or VFF_DIFF is adjusted. It returns the ideal register setting for the requested ToT.

CHAPTER 6

Results

6.1 Analog to Digital Converter

The internal analog to digital converter (ADC) of RD53A is part of the monitoring block as explained in Section 3.2.1. It is designed to monitor internal chip currents and voltages, as well as readout temperatures and radiation sensors. In order to ensure a high level of accuracy, the ADC can be trimmed by a six bit trim register, each bit changing the step width on one of the six least significant bits in the ADC. Goal is to find the minimum DNL based on the ADC trim bit setting. For that reason a non-linearity scan as described in Section 5.1 is conducted for each trim bit setting. Figure 6.1(a) and Figure 6.1(b) show how the differential- and integral- non-linearity changes based on the trim bit setting.



(a) (b)

Figure 6.1: 6.1(a) Differential non-linearity of the integrated ADC as a function of the trim bit setting. 6.1(b) Integral non-linearity of the integrated ADC as a function of the trim bit setting.

This measurement was conducted on five chips in total. To decrease the total measurement time the trim bit scan range was lowered from [0:64] to [2:13] and the non-linearity scan range went from ADC bit 0 to ADC bit 2048, this ensures the activation of each bit in the ADC at least once. Additionally each data point of the ADC was measured 5 times in order to reduce noise and get better statistics.

Table 6.1 shows the ideal trim bit settings with the lowest absolute DNL for the measured chips. Those values do not necessarily represent the absolute lowest achievable values for INL, as the following measurements show [18], [19], [20].

Chip	Trim Bit	Absolute DNL
0x0C62	4/5	1
0x074B	5	0.78
0x0747	4/5	1
0x0748	5	0.80
0x0751	6	0.92

Table 6.1: This table shows the trim bit setting with the lowest DNL for the five measured chips

According to Table 6.1 the trim bit can be set to five in most cases. Therefore all following measurements will be conducted with trim bit setting five.

6.2 Temperature Sensors

The internal temperature sensors of RD53A are part of the monitoring block as explained in Section 3.2.1. They are designed to monitor the chips internal temperature. This is done as described in Section 5.2. In Equation 3.1 there is a free parameter N_f, which needs to be determined to estimate the temperature. This is done by measuring the temperature of the NTC and the voltage slope of each individual sensor over a temperature range from –40 °C and 60 °C. The individual estimation of N_f for each individual sensor, results in a temperature accuracy of less than ±4°C over the whole scan range. Figure 6.2 shows the N_f distribution for five chips over 2000 measurements between –40 °C and 60 °C. The mean hereby is 1.310 ± 0.014. This results in an accuracy of ±8.42 °C at an average ADC value of 1200 (228 mV). This error is dominated by the large uncertainty in N_f. Table 6.2 shows the ideal N_f factors for each measured chip. All in all the estimation of a common N_f parameter over all measured chips and temperature range has been proven suboptimal. An estimation of the N_f factors for each individual sensor and chip delivers a much higher accuracy.

Chip ID	Sensor 1	Sensor 2	Sensor 3	Sensor 4
0x0452	1.307 ± 0.008	1.298 ± 0.007	1.291 ± 0.009	1.309 ± 0.006
0x0A5B	1.304 ± 0.007	1.297 ± 0.007	1.328 ± 0.002	1.315 ± 0.005
0x0C68	1.300 ± 0.002	1.301 ± 0.003	1.295 ± 0.003	1.290 ± 0.003
0x0C88	1.316 ± 0.003	1.310 ± 0.003	1.311 ± 0.004	1.316 ± 0.002
0x045A	1.340 ± 0.002	1.322 ± 0.006	1.332 ± 0.003	1.310 ± 0.009
All	1.313 ± 0.015	1.307 ± 0.011	1.301 ± 0.018	1.308 ± 0.011

Table 6.2: Optimal Nf value for each measured temperature sensor.

In general the temperature sensors work. Their accuracy is within ±4 °C under ideal conditions and ±8 °C with an averaged N_f value for all sensors. For temperature estimation each temperature sensor should be calibrated individually.

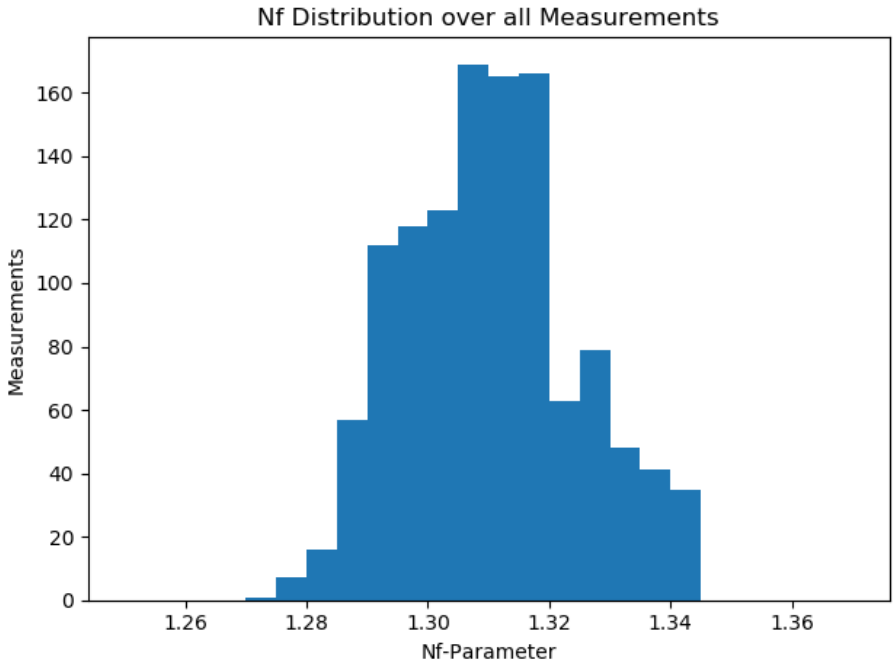


Figure 6.2: N_f distribution for five chips over 2 000 measurements between −40 °C and 60 °C. The mean of the distribution is 1.310 with a standard deviation of 0.014.

6.3 Front End Behavior

Goal of this thesis is the estimation of the optimal performance of each Front End at the given power settings. In order to find the ideal settings to meet given power requirements and compare the operation of the chip with simulation, the first set of measurements scanned over all register values to see how they affect performance and power consumption. These measurements have been conducted at room temperature and are therefore meant for a relative comparison between the three Front Ends. Performance parameters such as minimal tune-able threshold, threshold dispersion, in-time threshold, the according noise distributions as well as power consumption were used as benchmark parameters as set in Table 3.1. The general chip and environmental parameters are listed in Table 6.3. The shown results agree with a second set of measurements with chip 0x0A37.

Parameter	Value
$I_{ref}[\mu A]$	4.03
Direct Powering [V]	1.3
Temperature [°C]	22 (room temperature)
Irradiated Dose [Mrad]	0
Sensor	MPP W4-50x50, 100µm, PT
Chip ID	0x0A57

Table 6.3: Environmental and chip parameters for the following measurement series.

6.3.1 Plot Description

During the measurement series the following scans are conducted:

1. Noise Tuning (see Section: 5.5): To tune each Front End to its minimal stable threshold and dispersion
2. Threshold Scan (see Section: 5.4):To measure each Front Ends minimal stable threshold
3. Injection Delay Scan (see Section: 5.6): To determine the injection delay over the pixel matrix
4. In-Time threshold Scan (see Section: 5.7):To measure each Front Ends in-time threshold
5. Power Scan (see Section: 5.8):To measure the current consumption of digital and analog components of the chip

From these five measurements four types of plots are derived. In order to enhance comparability between the Front Ends, all plots are scaled the same way. Values that are outside the plotted rage are mentioned in the plot caption. The x-axis shows the parameter which was changed. Tables 3.2, 3.3 and 3.4 show what bias each parameter influences. The top left Plot 6.3(a) shows the minimal tun-able threshold in blue triangles. The error bars and green dots hereby correspond to the threshold dispersion at the given parameter. The amount of failed S-curve fits in percent is plotted in black squares. The read horizontal dashed line shows the specification for RD53 in Threshold (600 e-) and Threshold dispersion (60 e-). The top right Plot 6.3(b) shows the measured in-time threshold in blue triangles. Here the error bars represent the in-time threshold dispersion. The black squares show the amount of failed S-curve fits during the in-time threshold scan in percent. The green dots show the value for the global threshold, which the Front End was tuned to. The bottom left Plot 6.3(c) shows the noise in blue triangles. The noise dispersion is indicated by the blue error bars. The black squares represent the analog current consumption per pixel in μA, while the green dots represent the digital power consumption per pixel in μA. The bottom right Plot 6.3(d), is used as control panel indicating the tuning quality. For an ideal tuning all points should remain close to zero. The blue triangles show how many pixels in percent were not touched during tuning and remain in the highest or lowest TDAC bin. The black squares show how many pixels received more hits than injections during the threshold scan. The green dots indicate how many pixels in percent lie outside the Gaussian fit for the threshold distribution. In all four plots the vertical dashed red line indicates the original standard value for the measured register as stated in Table A.1. The horizontal red dotted line indicates the specification as stated in Table 3.1. In the following the most important register parameters for each Front End will be compared.

6.3.2 Synchronous Front End

The Synchronous Front End as described in Section 3.2.2 has nine global DACs, with four performance influencing registers. In the following the measurements over these four registers will be discussed. The other five measurements can be found in Appendix A.3 and will not be discussed explicitly, due to their either small influence on performance or declaration as reference voltages. The Synchronous Front End has one main pre-amplifier bias "IBIAS_SF_SYNC", as well as one bias register for the main amplifier branch "IBIAS_SP1_SYNC". Additionally it has one bias register for the splitting branch

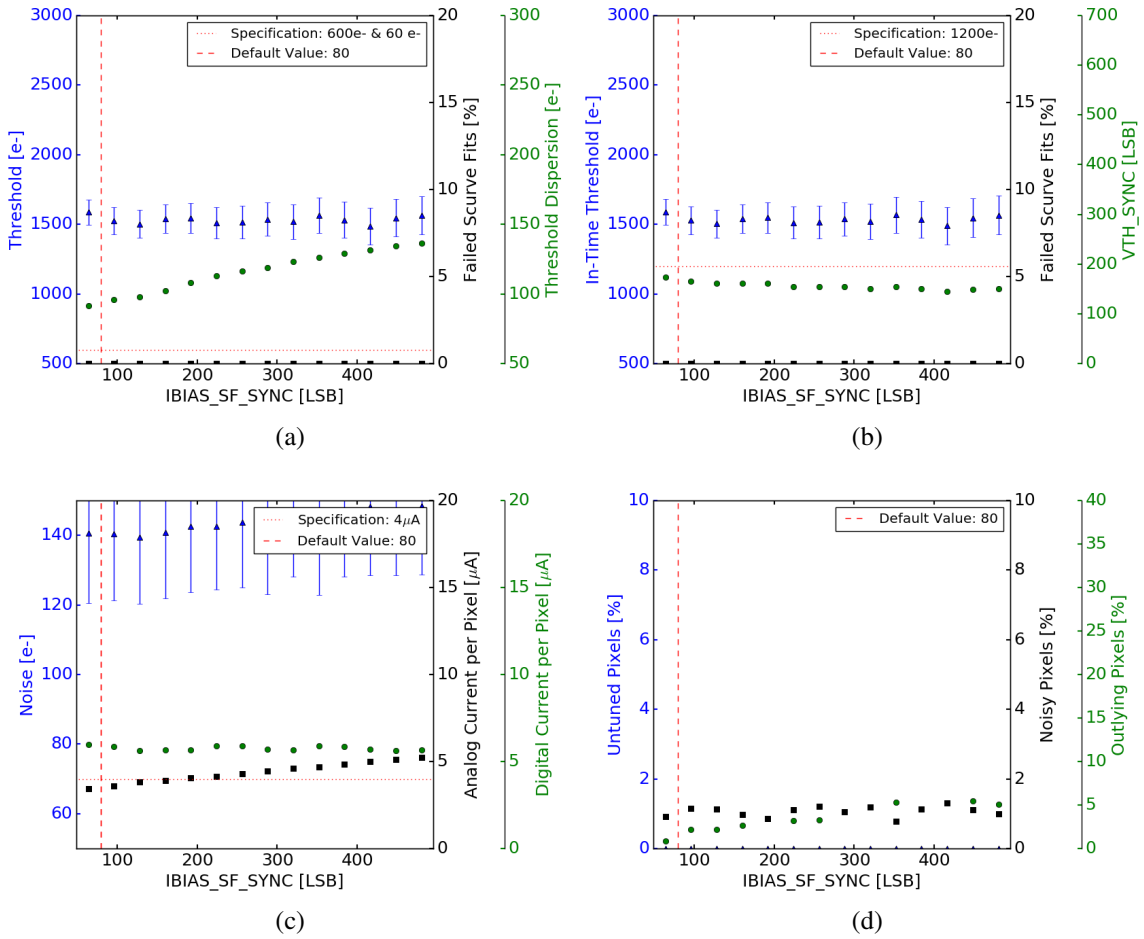


Figure 6.3: Overview of the Synchronous Front End performance depending on the supplied pre-amplifier current IBIAS_SF_SYNC 3.2.

"IBIAS_SP2_SYNC" of the charge sensitive amplifier. The three registers influence on threshold, in-time threshold, as well as noise and power as can be found in Figures 6.3, 6.4 and 6.5.

Figure 6.3(a) shows a constant behavior of the threshold, as indicated by the blue triangles. The threshold dispersion, linearly increases, as indicated by the green circles. The amount of failed S-curve fits remains close to 0% over the full scan range. Figure 6.3(b) shows a constant behavior in in-time-threshold, as well as the tuning outcome on the VTH_Sync register. The amount of failed S-curves is still 0%. Figure 6.3(d) shows constant noise behavior over the full IBIAS_SF_SYNC range. This Figure also indicates a linear relation between the analog current consumption of the chip and IBIAS_SF_SYNC. The digital current consumption remains constant. Figure 6.3(d), shows a constant relation between IBIAS_SF_SYNC and the amount of untuned pixels, noisy pixels and outlying pixels. Over all this register works as expected within the measured operation range of [64:496]. For the final measurement a register setting of 50 was chosen in order to minimize power consumption.

Figure 6.4(a) shows an optimization trade-off between threshold and threshold dispersion. While the threshold dispersion has its minimum at low IBIASP1_SYNC values and saturates towards higher

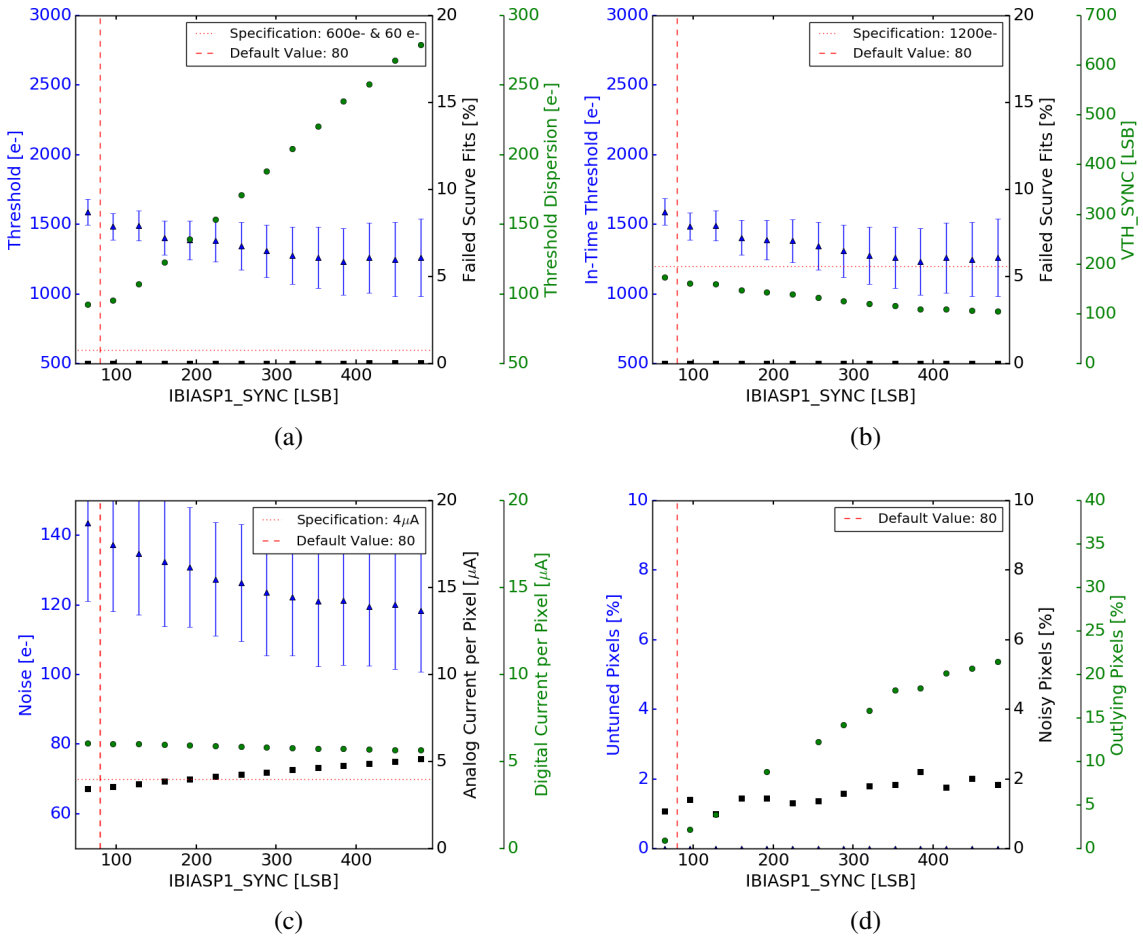


Figure 6.4: Overview of the Synchronous Front End performance depending on the supplied bias current of the main CSA branch IBIASP1_SYNC 3.2.

values, the threshold mean follows the opposite trend. Here the lowest mean is achieved for high IBIASP1_SYNC values, while the highest can be found at low IBIASP1_SYNC values. However this behavior is explained considering Figure 6.4(c). Here a saturating behavior between IBIASP1_SYNC and noise is observed. These lower noise at higher DAC values enables the Front End to be operated at lower thresholds, while trading some of its threshold performance for broader threshold dispersion. Figure 6.4(b) shows better in-time threshold performance for higher IBIASP1_SYNC values. Figure 6.4(d) shows the amount of outlying pixels steadily increasing. This is an indicator for less Gaussian threshold and noise distributions. All in all this register performs as it should within the measured DAC range of [64:496]. For the final performance measurement a register value of 80 was chosen to minimize power consumption and threshold dispersion.

Figure 6.5(a) shows a falling threshold behavior, saturating at 1100 e-, while maintaining a threshold dispersion of less than 100 e-. Figure 6.5(b) shows the in-time threshold with similar behavior, at a steeper slope. Additionally the chip can be tuned to lower global thresholds, which is related to the decreasing noise level, as displayed in 6.5(c). This plot also shows constant current consumption of the

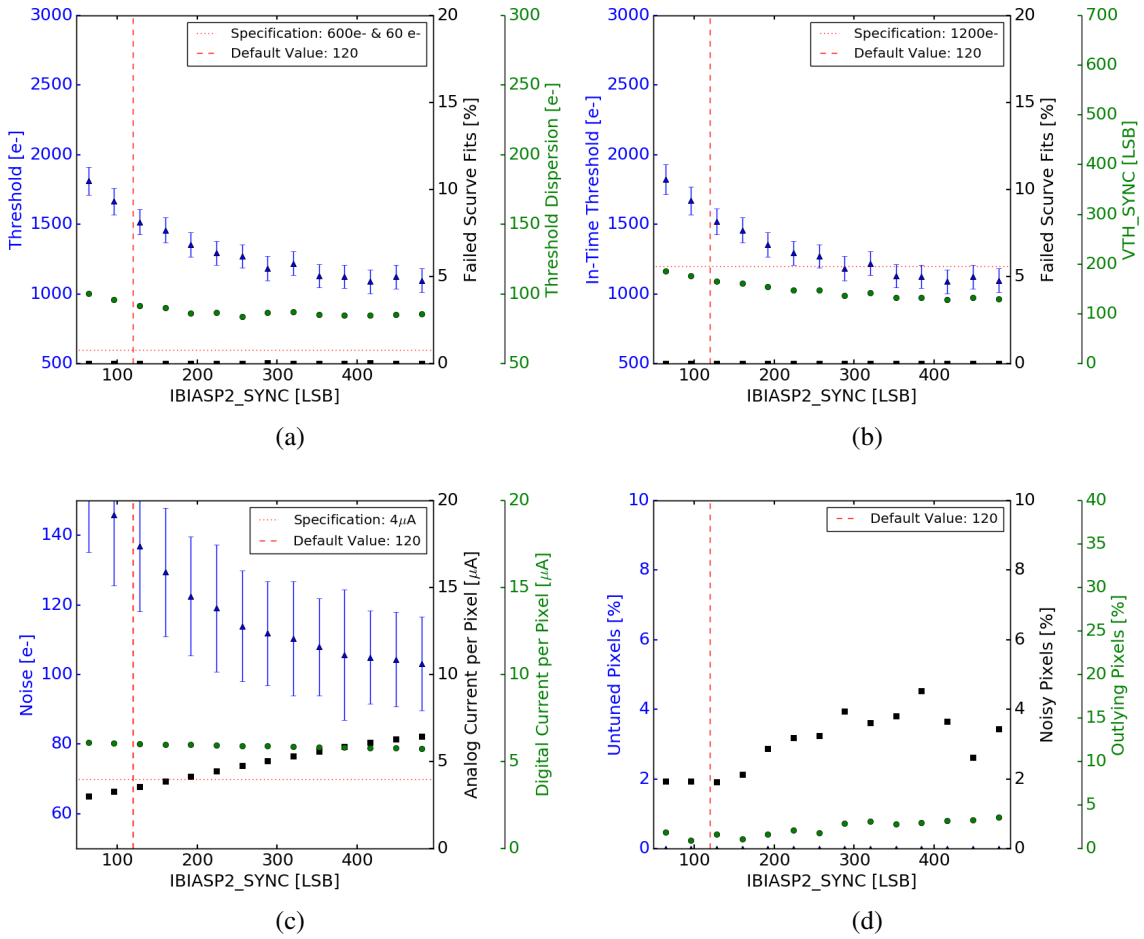


Figure 6.5: Overview of the Synchronous Front End performance depending on the supplied bias current of the splitting CSA branch IBIASP2_SYNC 3.2.

digital components and a linear increase in current consumption for the analog components. Figure 6.5(d) shows a rather linear increase in noisy pixels, which is related to the lower global threshold value which was used for higher IBIASP2_SYNC settings and degradation of the Gaussian threshold distribution, as the green dots indicate. All in all this register behaves as expected in the scanned range [64:496]. For the final performance measurement a register value of 120 was chosen to minimize power consumption.

The IBIAS_KRUM_SYNC register, which controls the discharge current of the charge integrating capacitance of the Synchronous Front End, is labeled as Cf in Figure 3.5(a). This register is used to tune the ToT of the injected signal. Figure 6.6(a) shows an increase of the threshold, with increasing IBIAS_KRUM_SYNC. The in-time threshold in Figure 6.6(b) increases in the same manner, since faster discharge currents also makes low charge detection harder. Instead an increasing noise level can be observed, as shown in Figure 6.6(c). The amount of noisy and outlying pixels decreases for higher IBIAS_KRUM_SYNC values. A significant increase in noisy and outlying pixels is the consequence. This is shown in Figure 6.6(d). All in all this register behaves as expected in the scanned range

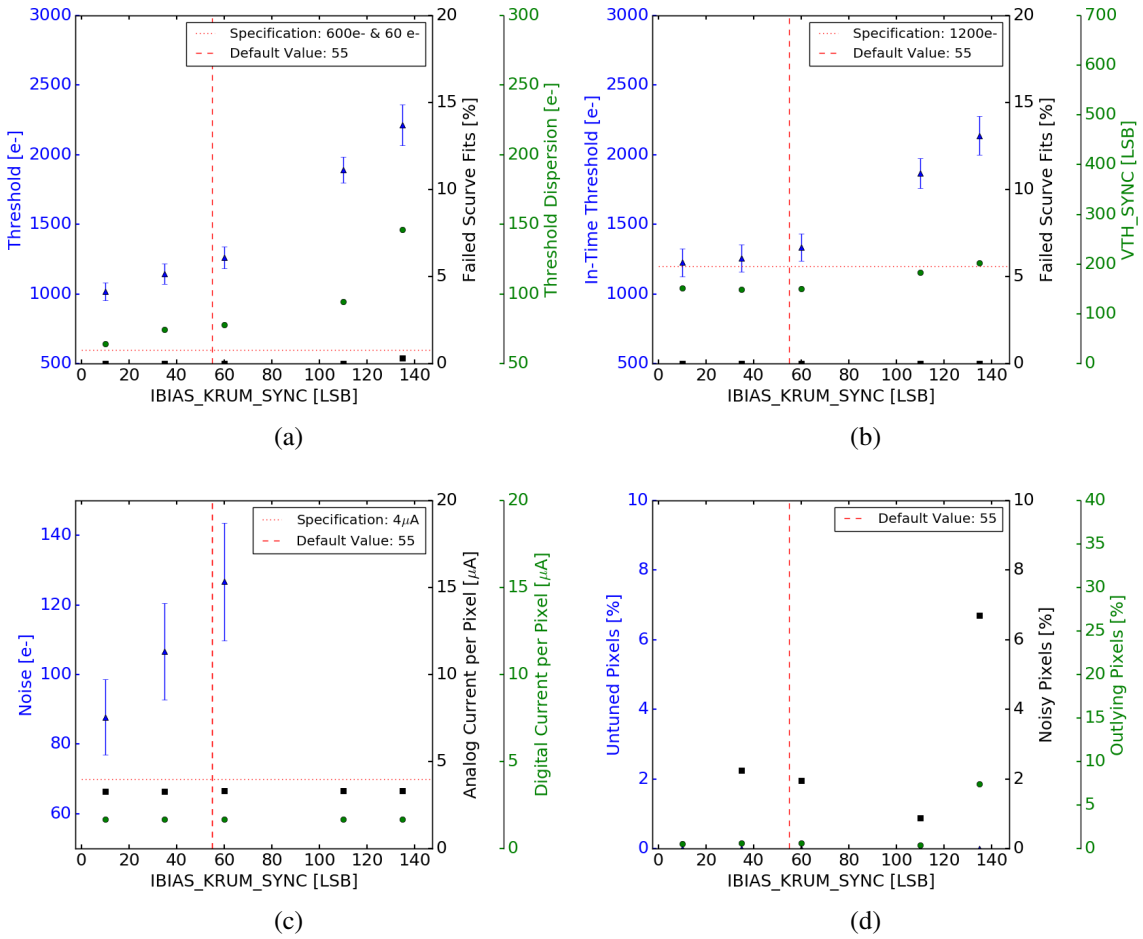


Figure 6.6: Overview of the Synchronous Front End performance depending on the charge injection capacitance discharge current IBIAS_KRUM_SYNC 3.2. The maximum Noise value is (228 ± 48) e.

(0:112]. However, Figure 5.8(a) shows unexpected ToT behavior for register values >160. Therefore this register should only be operated in a range (0:160]. For the final performance measurement this register was tuned to deliver a ToT of 133 ns at an injected charge of 6 000 e. This corresponds to a DAC setting of ~65 for the final measurement.

Conclusion

All in all the Synchronous Front End fulfills all specifications as mentioned in Table 3.1 except for the minimum tun-able threshold. The more important in-time threshold of 1200 e- can be achieved. Additionally the usable register range is fairly limited compared to the Differential Front End. Between threshold and in-time threshold there is no observable difference at sufficient supplied current.

6.3.3 Linear Front End

The Linear Front End as described in Section 3.2.2 has seven global DAC's, with four performance influencing biases. In the following the measurements over these four registers will be discussed. The other two measurements will not be discussed, due to their either small influence on performance or declaration as reference voltages. The Linear Front End has one main pre-amplifier bias "PA_IN_BIAS_LIN", one discharge current register "KRUM_CURR_LIN", which discharges the charge integrating capacitance Cf as indicated in Figure 3.6(a). One local threshold trimming DAC "LDAC_LIN", which determines the step width of one TDAC value. As well as one comparator bias register "COMP_LIN". The four registers influence on threshold, in-time threshold, as well as noise and power as can be found in Figures 6.7, 6.8, 6.9 and 6.10.

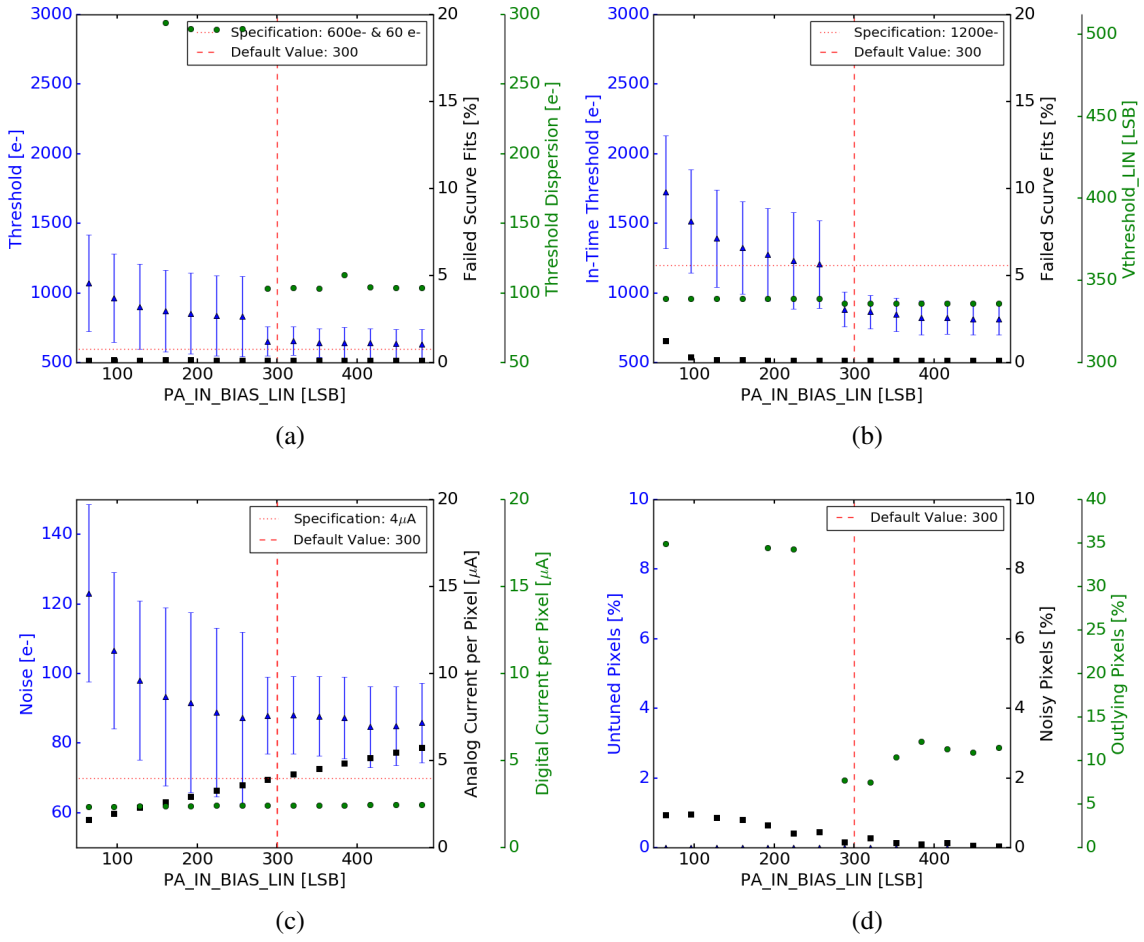


Figure 6.7: Overview of the Linear Front End performance depending on the supplied pre-amplifier bias current PA_IN_BIAS_LIN 3.3. The maximum percentage of outlying pixels is 63%.

The PA_IN_BIAS_LIN register, which controls the pre-amplifier bias current of the Linear Front End leads to a falling minimum tun-able threshold for higher bias values, as shown in Figure 6.7(a). In-time threshold behaves the same way, with an offset of around 300 e as shown in Figure 6.7(b).

Noise has the same falling behavior as shown in Figure 6.7(c). The power consumption as displayed in Figure 6.7(c) scales linearly with the pre-amplifier bias. Figure 5.5(a) indicates, a better tuning behavior for higher bias values. All four panels show a jump at a bias value around 300. In all cases the performance increases for all PA_IN_BIAS_LIN values above that point. This indicates that the circuit is not working as intended for values that are lower than ~300. Beyond this point the performance gain in terms of threshold, in-time threshold and noise is rather low especially considering the analog current consumption gain. All in all this register should be operated in a range between [300:460]. For the final measurement a value of 270 was chosen to minimize current consumption.

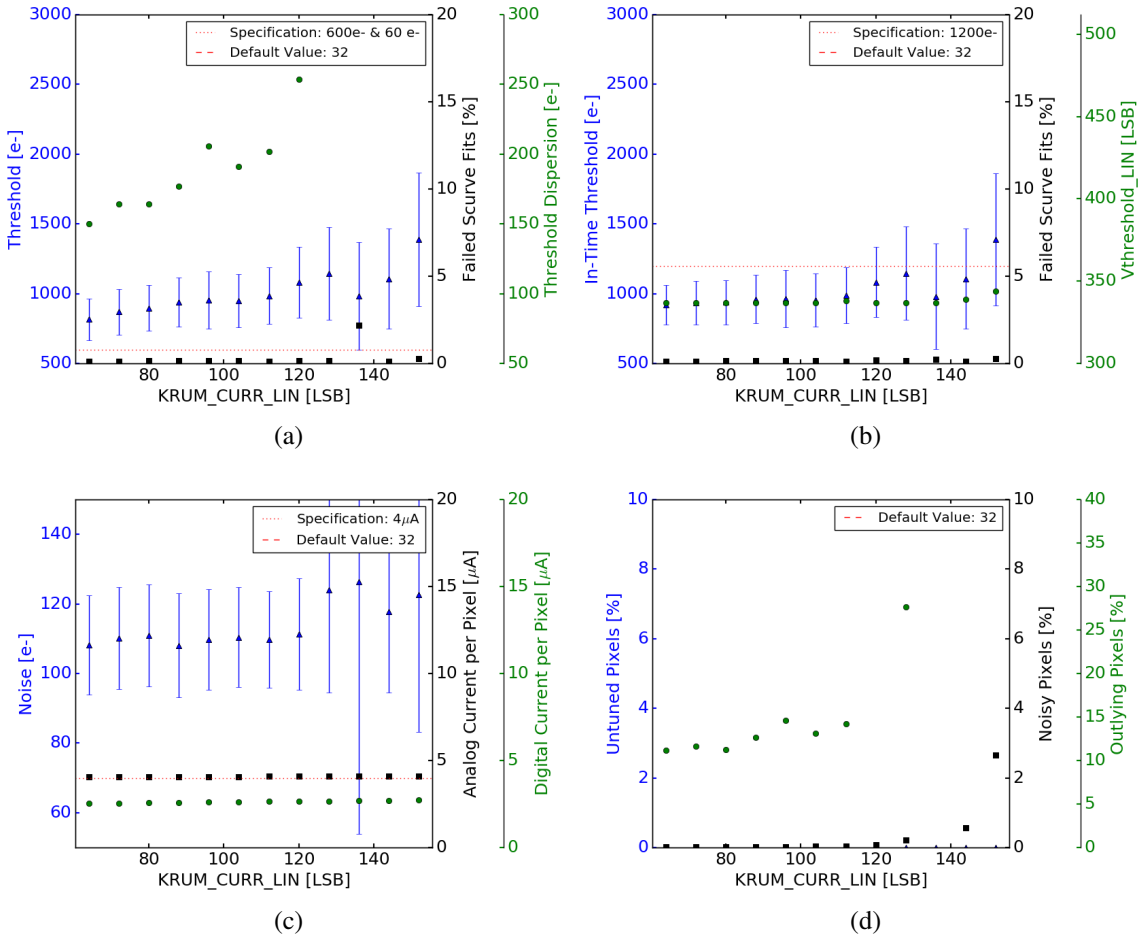


Figure 6.8: Overview of the Linear Front End performance depending on the charge injection capacitance discharge current KRUM_KURR_LIN 3.3. The maximum percentage of outlying pixels is 65%.

The KRUM_KURR_LIN register, which controls the discharge current of the charge integrating capacitance of the Linear Front End, labeled as Cf in Figure 3.6(a), is used to tune the ToT of the injected signal. Figure 6.8(a) shows an increase of the threshold, with increasing KRUM_KURR_LIN, from 130 anomalous behavior is observed. The in-time threshold in Figure 6.6(b) increases in the same manor. Additionally an increase in noise is observed, as shown in Figure 6.8(c). The amount of noisy and outlying pixels remains constant, as Figure 6.8(d) shows. Figure 5.8(b) shows an additional

sweep over this register, showing the time over threshold (Tot) distribution on the y- axis. With the other plots this confirms a non expected rise of the ToT value for register values >130. All in all this register should be operated in a range between (0:130]. For the final measurement, this register was tuned to deliver a ToT of 133 ns at an injected charge of 6 000 e. This corresponds to a DAC setting of ~37 for the final measurement.

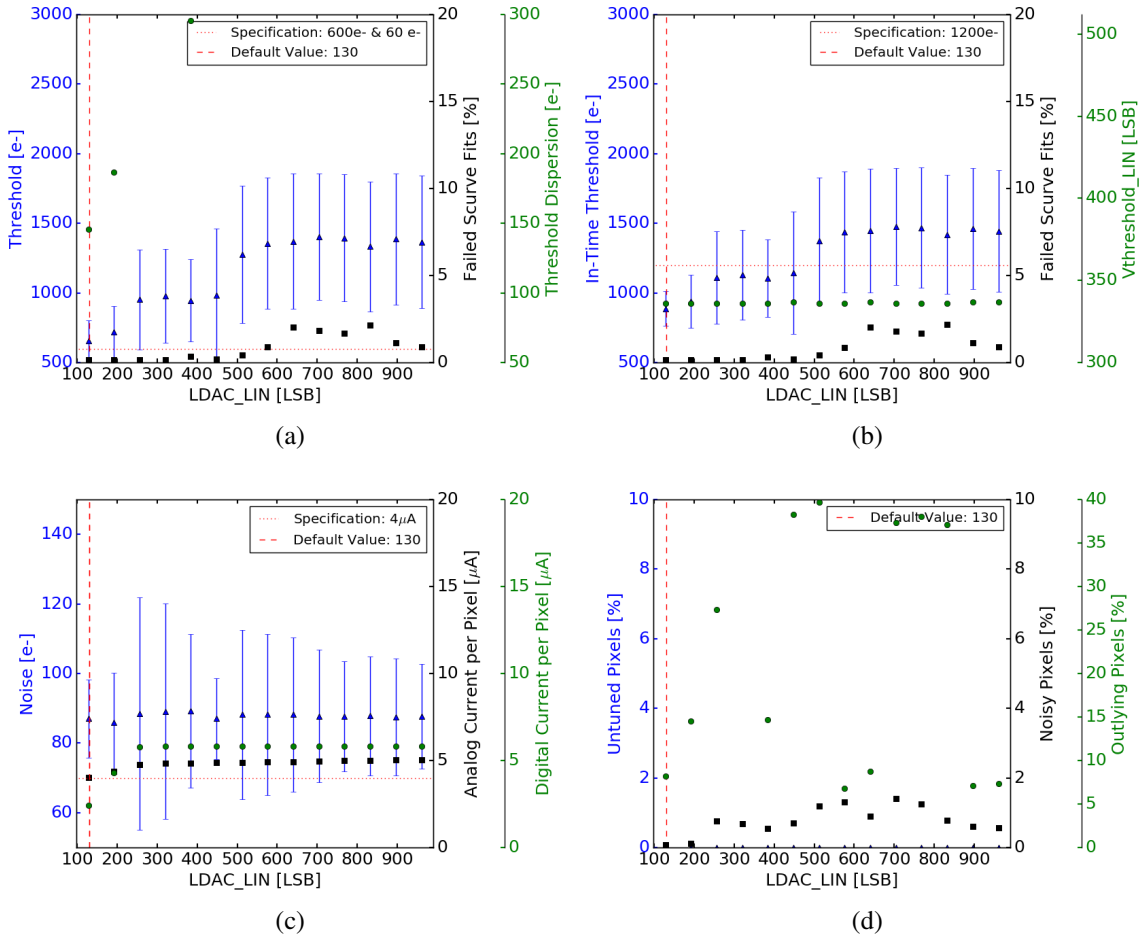


Figure 6.9: Overview of the Linear Front End performance depending on the local current offset step width LDAC_LIN 3.3. The maximum threshold dispersion is 492 e- and the maximum percentage of outlying pixels is 56%.

The LDAC_LIN register, which controls the constant current offset in each individual pixel of the Linear Front End has a linearly increasing influence on threshold and threshold dispersion. The behavior for LDAC_LIN between 0 LSB and 200 LSB shows the expected behavior. The behavior for LDAC_LIN > 200 LSB however is atypical and indicates non-linear behavior of the DAC. This can be seen in Figure 6.9(a), where a jump in threshold dispersion around 200 LSB is observed. At around 500 the chip is untunbale and the threshold dispersion gets larger than 400 e-. Figure 6.9(b) shows the same behavior in in-time-threshold dispersion and an increase in in-time-threshold from 100 LSB to 320 LSB. Noise stays rather constant. Power consumption, which the green circles and

black squares indicate, show a linear power consumption increase between 100 LSB and 320 LSB and a saturation for values higher than 320 LSB as Figure 6.9(c) indicates. Figure 6.9(d) shows a linear increase of outlying pixels for values between 0 LSB and 200 LSB. The amount of noisy pixels stays rather low in the trust worthy LDAC_LIN range. All in all this register should only be operated in a range between (90:200]. For the final measurement, this register was chosen to be operated at 155 to get the maximum dynamic TDAC range at the given current consumption.

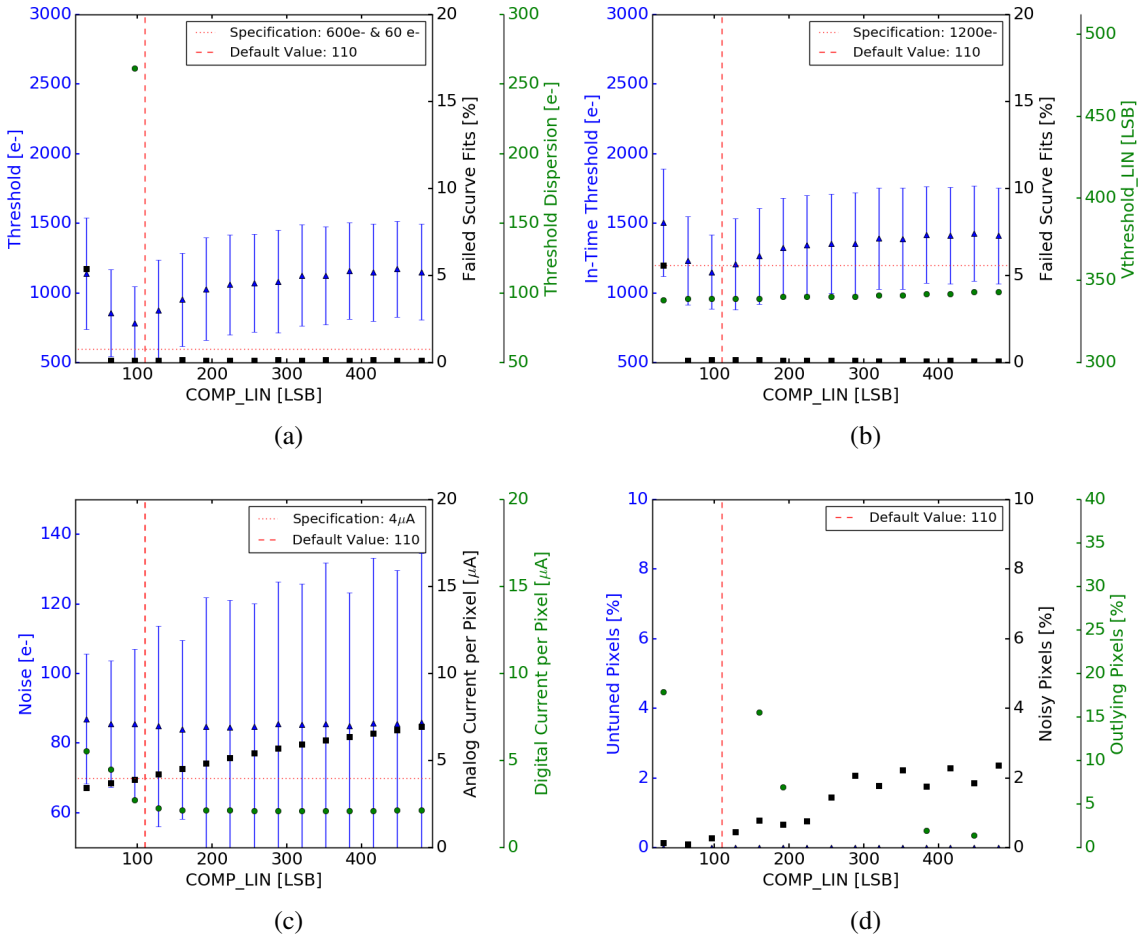


Figure 6.10: Overview of the Linear Front End performance depending on the reference current for the comparator stage COMP_LIN 3.3. The maximum of Outlying pixels is 67%.

The COMP_LIN register, which controls the comparator current in the Linear Front End has a decreasing influence on threshold and dispersion up to roughly 100 LSB and thereafter increases it with a saturation value of around 1000e-. This is shown in figure 6.10(a). The amount of failed fits stays low. Figure 6.10(b) shows the same behavior in in-time threshold and dispersion. There is no measurable influence on the threshold DAC as the green dots indicate. Figure 6.10(c) shows a small drop in noise for increased COML_LIN values, but saturates rather fast. The power increase in VDDA is linear over the full range. Figure 6.10(d) shows a maximum of outlying pixels at roughly 100 LSB thereafter it converges to 0. The amount of noisy pixels increases linearly. All in all the

register shows a minimum threshold dispersion at 110 with few noisy pixels. Over the rest of the range the threshold dispersion increases, with small influence on in-time threshold. All in all this register should be operated at values around 110. For the final measurement, this register was chosen to be operated at 90 to lower current consumption.

Conclusion

All in all the Linear Front End fulfills all specifications as mentioned in Table 3.1. Some of its registers feature a very narrow operating range, which gives little room for optimization. Additionally the tuning is complicated, especially at low temperatures. Furthermore the Linear Front End showed the largest difference between threshold and in-time threshold.

6.3.4 Differential Front End

The Differential Front End as described in Section 3.2.2 has eight global DAC's with four performance influencing biases. In the following the measurements over these four registers will be discussed. The other four measurements will not be discussed, due to their either small influence on performance or declaration as reference voltages. The Differential Front End has one main pre-amplifier bias "PRMP_DIFF", one discharge current register "VFF_DIFF", which discharges the charge integrating capacitance Cf as indicated in Figure 3.7(a). One local threshold trimming DAC "LDAC_LIN", which determines the step width of one TDAC value. As well as one comparator bias register "COMP_LIN". The four registers influence on threshold, in-time threshold, as well as noise and power as can be found in Figures 6.11, 6.12, 6.13 and 6.14.

The PRMP_DIFF register, which controls the bias current of the pre-amplifier of the Differential Front End shows a lowering effect on minimal tun-able threshold for increasing bias values. The threshold dispersion remains constant over the whole range. This behavior is shown in Figure 6.11(a). Figure 6.11(b) shows the same behavior for in-time threshold with a small offset in the beginning. The black squares in the upper two plots indicate a constantly low amount of failed S-curve fits. Figure 6.11(c) shows falling noise levels saturating around 70 e, while the analog current consumption increases linearly at a constant digital current consumption. Figure 6.11(d) shows a low amount of un-tuned and outlying pixels over the whole range. The amount of noiys pixels however is between 11 % and 17 %. These pixels however show low noise levels with less than 10 hits more than injected. All in all this register can be operated over the whole range. For the final measurement, this register was chosen to be operated at 511 LSB.

The VFF_DIFF register, which controls the discharge current of the charge integrating capacitance of the Differential Front End, labeled as Cf in Figure 3.7(a), is used to tune the ToT of the injected signal. Figure 6.12(a) shows an increase in the minimal tun-able threshold, with increasing VFF_DIFF. The in-time threshold in Figure 6.12(b) increases in the same manor. Additionally a noise increase is observed, while VDDD and VDDA remain constant, as shown in Figure 6.12(c). The amount of noisy pixels decreases, together with the amount of untuned pixels. The amount of outlying pixels is however increasing, according to Figure 6.12(d). Figure 5.8(c) shows the impact of the "VFF_DIFF" register on Tot.This plot shows a nice ToT drop for higher "VFF_DIFF" values over the whole range. All in all this register can be operated over the whole range. For the final measurement, this register was tuned to deliver a ToT of 133 ns at an injected charge of 6 000 e. This corresponds to a DAC setting of ~89 for the final measurement.

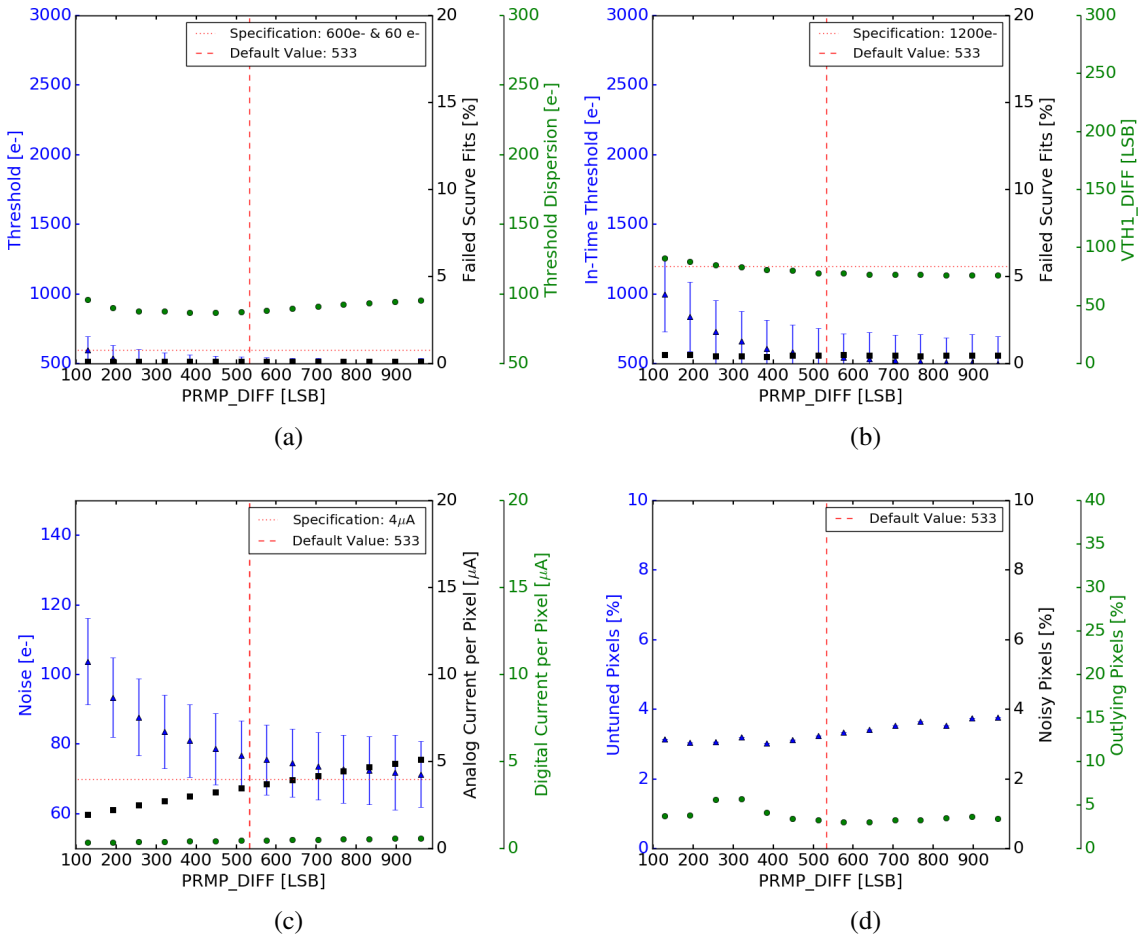


Figure 6.11: Overview of the Differential Front End performance depending on the supplied pre-amplifier bias current PRMP_DIFF 3.4. The amount of noisy pixels is constantly between 11 % and 17 %.

The PRECOMP_DIFF register, which controls the pre-comparator tail current of the Differential Front End has a linearly increasing influence on threshold and threshold dispersion. This behavior of PRECOMP_DIFF can be observed in Figure 6.13(a). The threshold dispersion slowly increases with higher values, while the minimum tun-able threshold reamains constantly below 500 e-. Figure 6.13(b) shows a decrease in failed scurve and for increasing DAC values. This indicates good tunability for values larger than 500 LSB. The threshold DAC value (green dots) is also constantly decreasing due to the broader TDAC step width with increasing PRECOMP_DIFF. Figure 6.13(c) shows falling noise for higher DAC values and a linear increase in analog power consumption. Figure 6.13(d) confirms the observations from former plots and shows better tuning results with higher PRECOMP_DIFF value. All in all this register can be operated over the whole range. For the final measurement, this register was chosen to be operated at 390 to reduce the load on the comparator input and optimize timing performance.

The COMP_DIFF register, which controls the Total comparator current has little influence on threshold as Figure 6.14(a) shows. The minimum stable threshold stays constantly below 500 e-. The

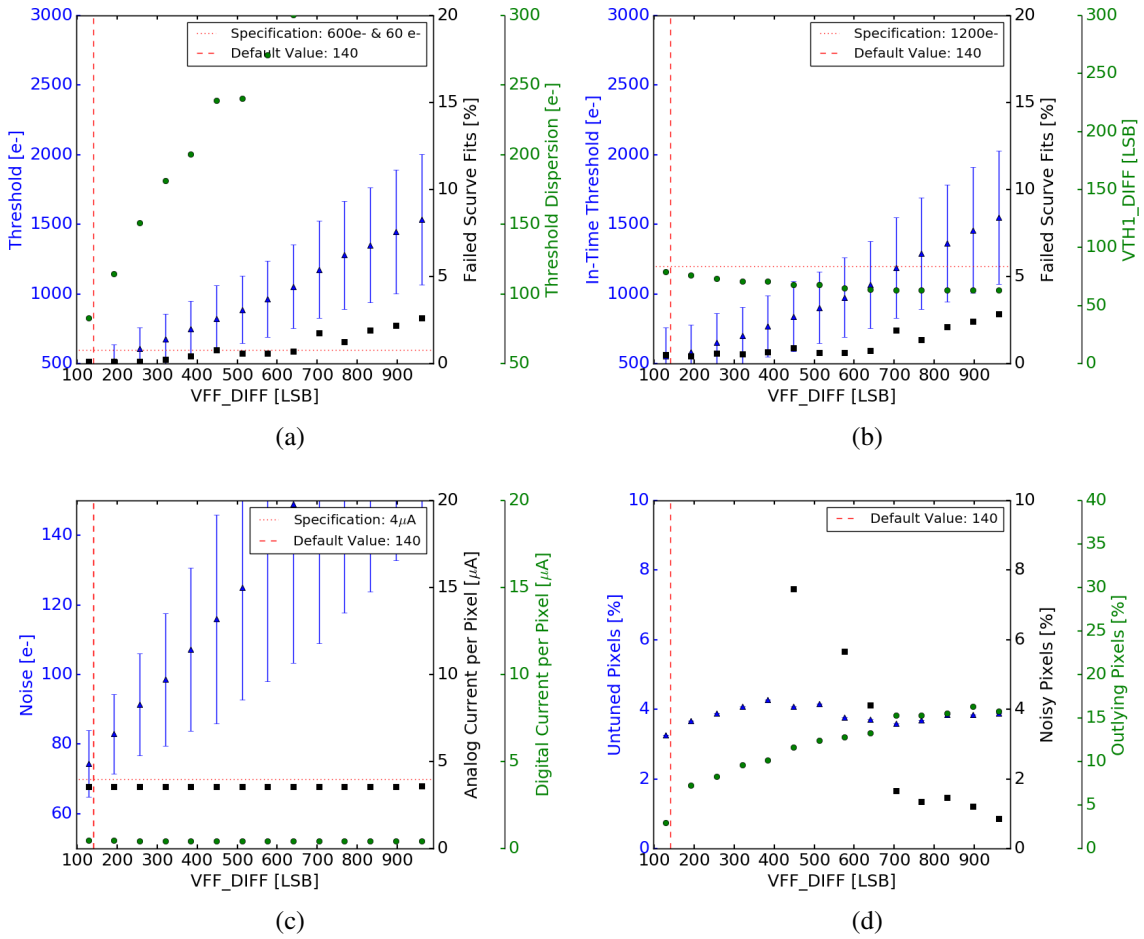


Figure 6.12: Overview of the Differential Front End performance depending on the charge injection capacitance discharge current VFF_DIFF 3.4. The maximal amount of noisy pixels is 20 %

in-time threshold and in-time threshold dispersion decreases as Figure 6.14(b) shows. The amount of failed S-curves also decreases. The global threshold setting increases with increasing COMP_DIFF setting. Figure 6.14(c) shows an increase in power with decreasing noise. Figure 6.14(d) shows a decreasing amount of outlying and untuned pixels. The amount of well tuned pixels saturates at ~ 550 LSB. All in all this register can be operated over the whole range. For the final measurement, this register was chosen to be operated at 1023, due to the lowest in-time threshold dispersion at this point. In RD53B design enhancements are expected to lower the timing dispersion and therefore lower the COMP_DIFF value.

Conclusion

All in all the Differential Front End fulfills all specifications as mentioned in Table 3.1. In general this Front End had troubles achieving the in-time threshold under certain bias settings. However low threshold operation, a wide adjustment range of all bias registers and low noise levels distinguishes

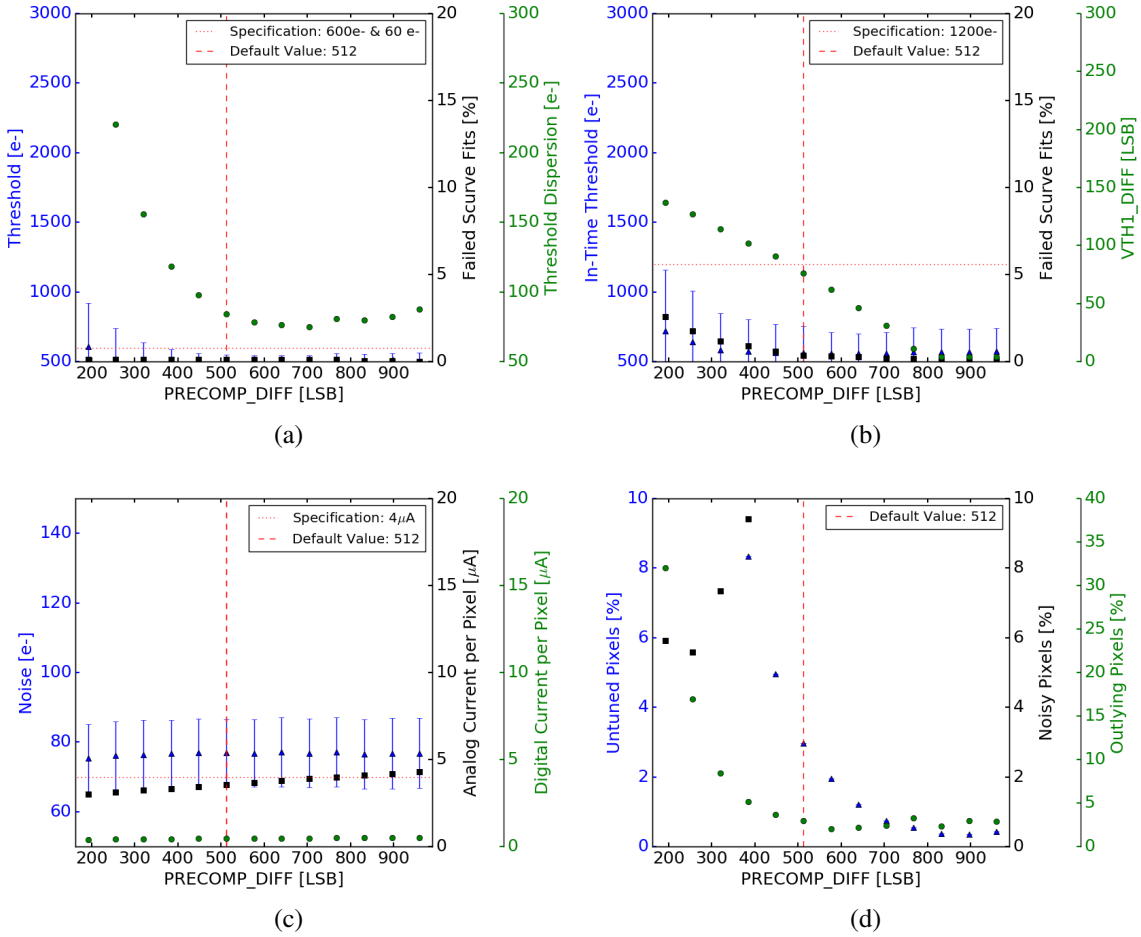


Figure 6.13: Overview of the Differential Front End performance depending on the tail current of the pre-comparator PRECOMP_DIFF 3.4. The maximal amount of noisy pixels is 20 %

this Front End from the others.

6.3.5 Final Set of Measurements

The previously introduced measurement series was used to derive the ideal settings for all Front Ends with a maximal current consumption per pixel of 4.0 μA. This measurement compares all three Front Ends at equal power settings of 4 μA current consumption under realistic environmental conditions such as LDO mode with VDDD and VDDA tuned to 1.2 V and Iref tuned to 4 μA, as well as $-20\,^{\circ}$C ambient temperature. Table 6.5 summarizes the environmental conditions. Table 6.4 summarizes the ideal DAC settings per Front End as extracted from Section 6.3.

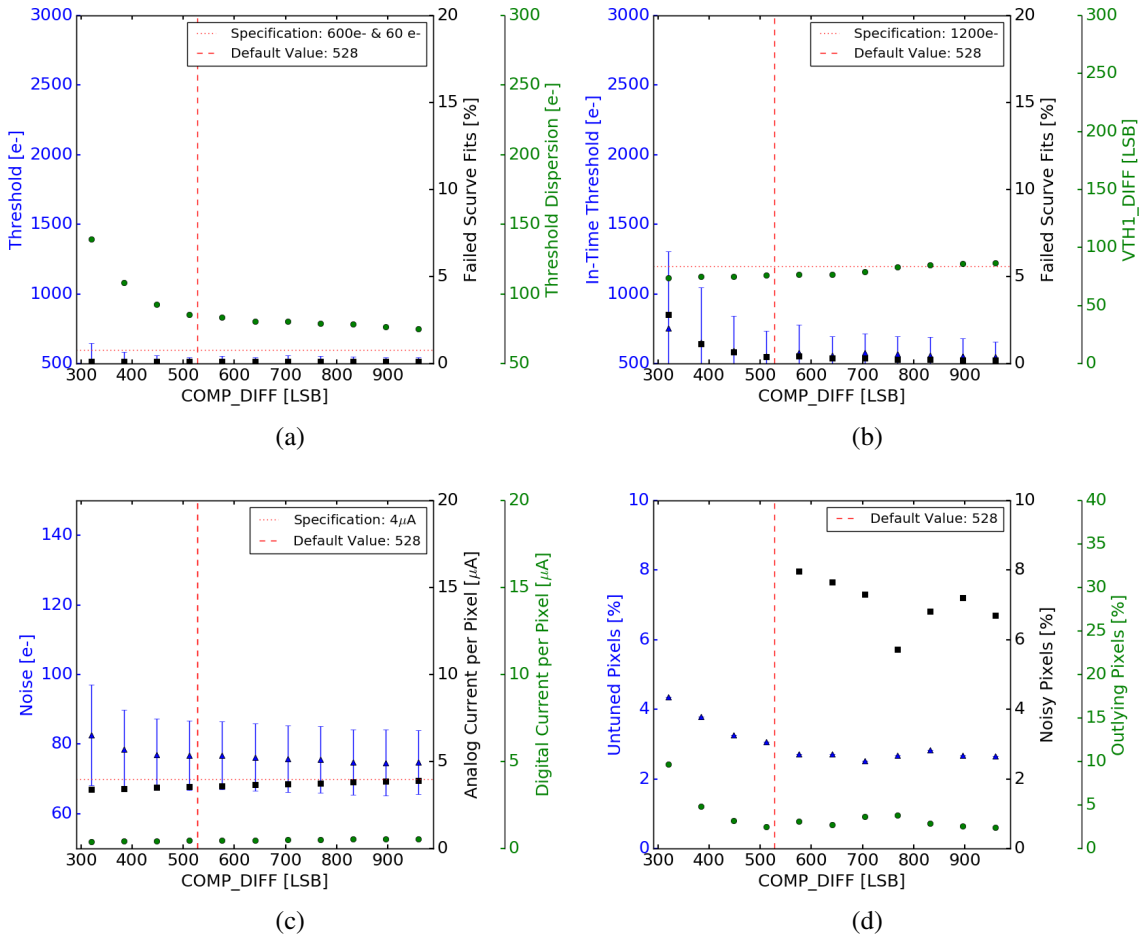


Figure 6.14: Overview of the Differential Front End performance depending on comparator bias COMP_DIFF 3.4. The maximal amount of noisy pixels is 100 %

Synchronous Front End		Linear Front End		Differential Front End	
Register	Value	Register	Value	Register	Value
IBIASP1_SYNC	80	PA_IN_BIAS_LIN	270	PRMP_DIFF	511
IBIASP2_SYNC	120	FC_BIAS_LIN	20	FOL_DIFF	542
IBIAS_SF_SYNC	50	KRUM_CURR_LIN	37	PRECOMP_DIFF	390
IBIAS_KRUM_SYNC	65	LDAC_LIN	155	COMP_DIFF	1023
IBIAS_DISC_SYNC	200	COMP_LIN	90	VFF_DIFF	89
ICTRL_SYNCT_SYNC	100	REF_KRUM_LIN	300	VTH1_DIFF	209
VBL_SYNC	360	Vthreshold_LIN	326	VTH2_DIFF	100
VTH_SYNC	91			LCC_DIFF	100
VREF_KRUM_SYNC	450			CONF_FE_DIFF	2

Table 6.4: This Table shows the operation parameters for all of RD53A's Front Ends, for a 50x50 sensor chip at -20°C.

Parameter	Value
$I_{ref}[\mu A]$	4.00
VDDD and VDDA in LDO Powering [V]	1.2
Temperature [°C]	-22
Irradiated Dose [Mrad]	0
Sensor	MPP W4-50-50x100, 100µm, PT
Chip ID	0x0B87 / 0x0A57

Table 6.5: This Table shows the environmental and chip parameters for the final Front End comparison measurement series.

Front Ends	Synchronous	Linear	Differential
Threshold Mean [e-]	1 014	1 020	1 323
Threshold Std. [e-]	84	183	73
In-Time Threshold Mean [e-]	1 569	1 406	1 450
In-Time Threshold Std. [e-]	127	204	129
Noise [e-]	148	77	74
Noise Std. [e-]	15	12	9
Current consumption per Pixel [μA]	4.2	3.71	3.71
Disabled Pixels [%]	6.59	4.82	0.0
Noise Occupancy	1.12×10^{-6}	2.10×10^{-6}	0.0
Overdrive [e-]	549	383	103

Table 6.6: This table shows a summary of the final measurement series comparing the performance of all three Front Ends at ~4.0 μA current consumption per pixel.

Table 6.6 shows the final performance measurements of all three RD53A Front Ends at a current consumption of ~4.0 μA. All Front Ends were tuned to an in-time threshold of 1500 e- with the Linear Front end having the broadest threshold dispersion and the Differential Front End having the narrowest. Additionally an increased noise occupancy of the Synchronous and Linear Front End is observed. This is visible in the noise distribution, noise occupancy and disabled pixels row. The ToT was tuned to 133 ns at an injected charge of 6 000 e. All these parameters are achieved by a measured current consumption of 4.2 μA per pixel for the Synchronous Front End and 3.71μA for the Linear and Differential Front End. The Overdrive row shows the difference between the measured mean threshold and mean in-time threshold. Here lower values are better due to more headroom to operate at low in-time thresholds.

CHAPTER 7

Conclusion

In general all three Front Ends fulfill most of the important requirements stated in the "RD53A Integrated Circuit Specifications" [9]. Table 7.1 summarizes the RD53A specifications and summarizes whether the specifications were able to be achieved (+) in the final measurement of Section 6.3 or not (o). The current consumption tab considers, whether the in time threshold was achieved at less than 4 μA.

Circuit Property	Specs	Synchronous	Linear	Differential
Min. stable Threshold [e^-]	600	o	+	+
Threshold Dispersion [e^-]	60	+	o	+
In-time Threshold [e^-]	1200	+	+	+
Noise [e^-]	~ 70	o	+	+
Current Consumption [μA]	< 4	o	+	+

Table 7.1: Performance comparison Table between RD53A Front Ends.

Overall the performance of the Front Ends meet the requirements set by the RD53A collaboration. Table 7.1 confirms the observations from Section 6.3. The Synchronous Front End appears to be the noisiest, with the highest current consumption. The Linear Front End performs well at minimum tun-able threshold, in-time threshold and noise, with a broad threshold dispersion. The Differential Front End performs best or equal in five categories. However non of these observations include measurements with irradiated chips.

The characterization of the joined ATLAS and CMS RD53A pixel chip was a success. Both commonly used DAQ systems for RD53A deliver comparable results within the measured threshold and noise dispersion as Chapter 4 shows. For future DAQ implementations an agreement on common injection timing and frequency would be recommended. RD53A's ADC delivers sufficient accuracy to measure internal voltages and currents as Section 3.2.1 shows. The temperature measurement works with an accuracy of ±4 °C if each temperature sensor is calibrated individually and an accuracy of ±8 °C for an averaged N_f value as explained in Section 5.2.
All in all RD53A is a solid demonstrator chip, whose multiple analog Front End designs offer the unique opportunity to benchmark not only the Front Ends, but also their data acquisition systems.

APPENDIX A

Appendix

A.1 Default Parameters

The default parameters are a set of parameters, which were extracted from the analog Front End manuals. [13], [14], [15]. If not stated differently, Table A.1 shows the default parameters used throughout this thesis.

Synchronous Front End		Linear Front End		Differential Front End	
Register	Value	Register	Value	Register	Value
IBIASP1_SYNC	80	PA_IN_BIAS_LIN	300	PRMP_DIFF	533
IBIASP2_SYNC	120	FC_BIAS_LIN	20	FOL_DIFF	542
IBIAS_SF_SYNC	80	KRUM_CURR_LIN	32	PRECOMP_DIFF	512
IBIAS_KRUM_SYNC	55	LDAC_LIN	130	COMP_DIFF	528
IBIAS_DISC_SYNC	300	COMP_LIN	110	VFF_DIFF	140
ICTRL_SYNCT_SYNC	100	REF_KRUM_LIN	300	VTH1_DIFF	150
VBL_SYNC	400	Vthreshold_LIN	350	VTH2_DIFF	100
VTH_SYNC	110			LCC_DIFF	20
VREF_KRUM_SYNC	450			CONF_FE_DIFF	2

Table A.1: This table shows the recommended operation parameters for all of RD53A's front ends, as extracted from the Front End manuals. [13], [14], [15]

A.2 Differential Front End - Good Pixel Mask

The pixel matrix of RD53A consists of so called digital cores, which consist of 8x8 pixels. The Differential Front End matrix consists of 17x24 digital cores. The analog part of the Differential Front End was made in full custom mode (by hand). The digital part, was fully synthesized. This led to the optimization of the connection between the comparator output and digital pixel according to a routing algorithm. Due to the set boundary conditions, this resulted in a large variation in the lengths of the connections between the comparator output and each pixels digital input. The resistance of a connection is proportional to the length of a connection, which leads, combined with a parasitic capacitance shown in Figure A.1 at the comparator output, to a low pass filter like behavior. This

results in slower rising times, slower falling times, as well as a general shift of the signals at the comparator output, based on the pixels position within a digital core. The difference between the ideal and measured signal is shown in Figure A.2.
This issue can be easily resolved by adding an additional buffer between the analog and digital part. For that reason the performance of the Differential Front End will only be estimated by pixels which behave as expected in RD53B. For that reason a "good pixel mask" was designed, which shows what pixels inside a digital core will be used for characterization. Figure A.3 shows which pixels within a digital core will be used for characterization.

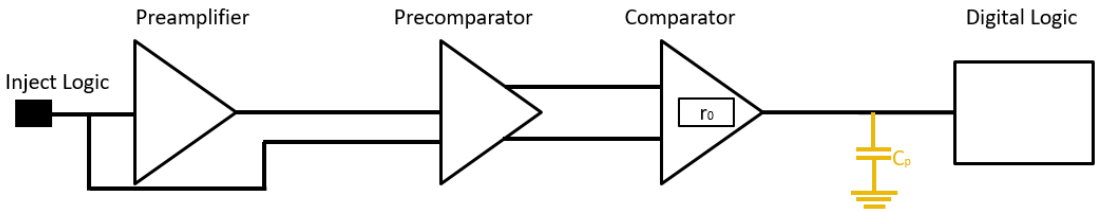


Figure A.1: This Figure shows the parasitic capacitance at the comparator output of the Differential Front End.

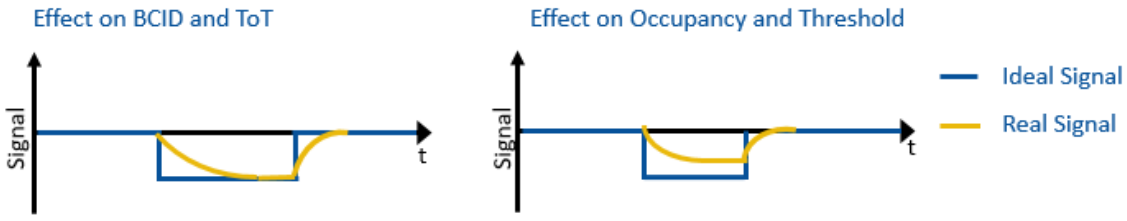


Figure A.2: This Figure shows the low pass filter effect of the parasitic capacitance on the ideal signal.

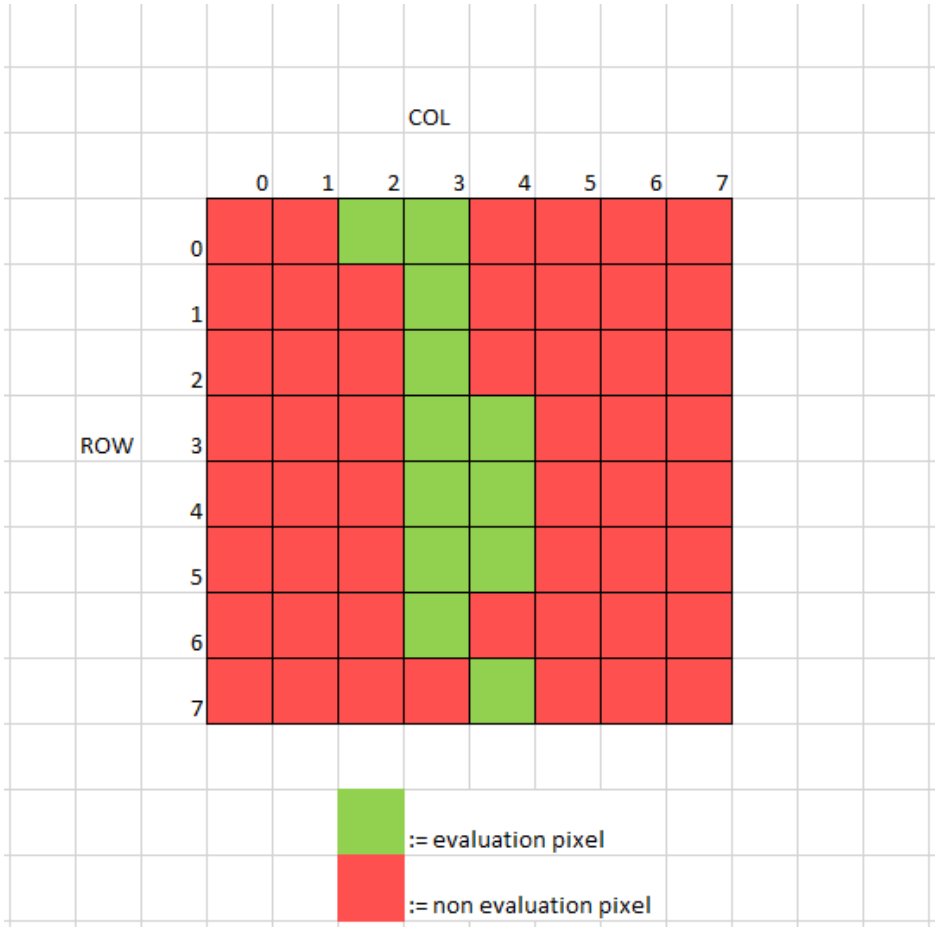


Figure A.3: This Figure shows the usable pixels for characterization in green and the other pixels in red.

Figure A.2 shows the effect of the parasitic capacitance on the comparator signal. The two effects observed are a shift, as well as a reduced amplitude of the signal. The timing effect leads to an increased systematic Front End timing dispersion, while the reduced amplitude effect leads to a systematic threshold increase effect for pixels with high output comparator resistance. It is important to note, that the falling edge of the comparator is slower than the rising edge of the comparator due to its internal design.

A.3 Synchronous Front End Register Measurements

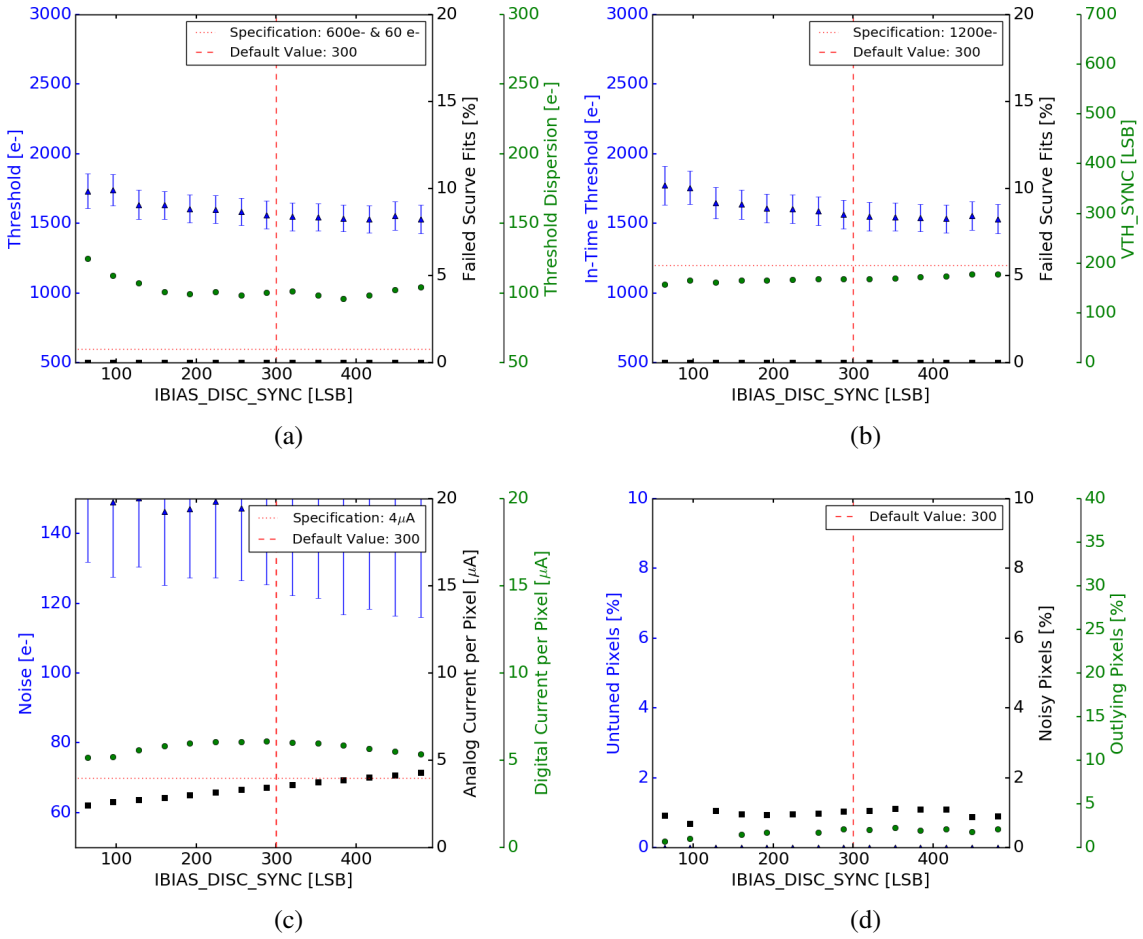


Figure A.4: Overview of the Synchronous Front End performance depending on preamplifier bias current IBIAS_DISC_SYNC.

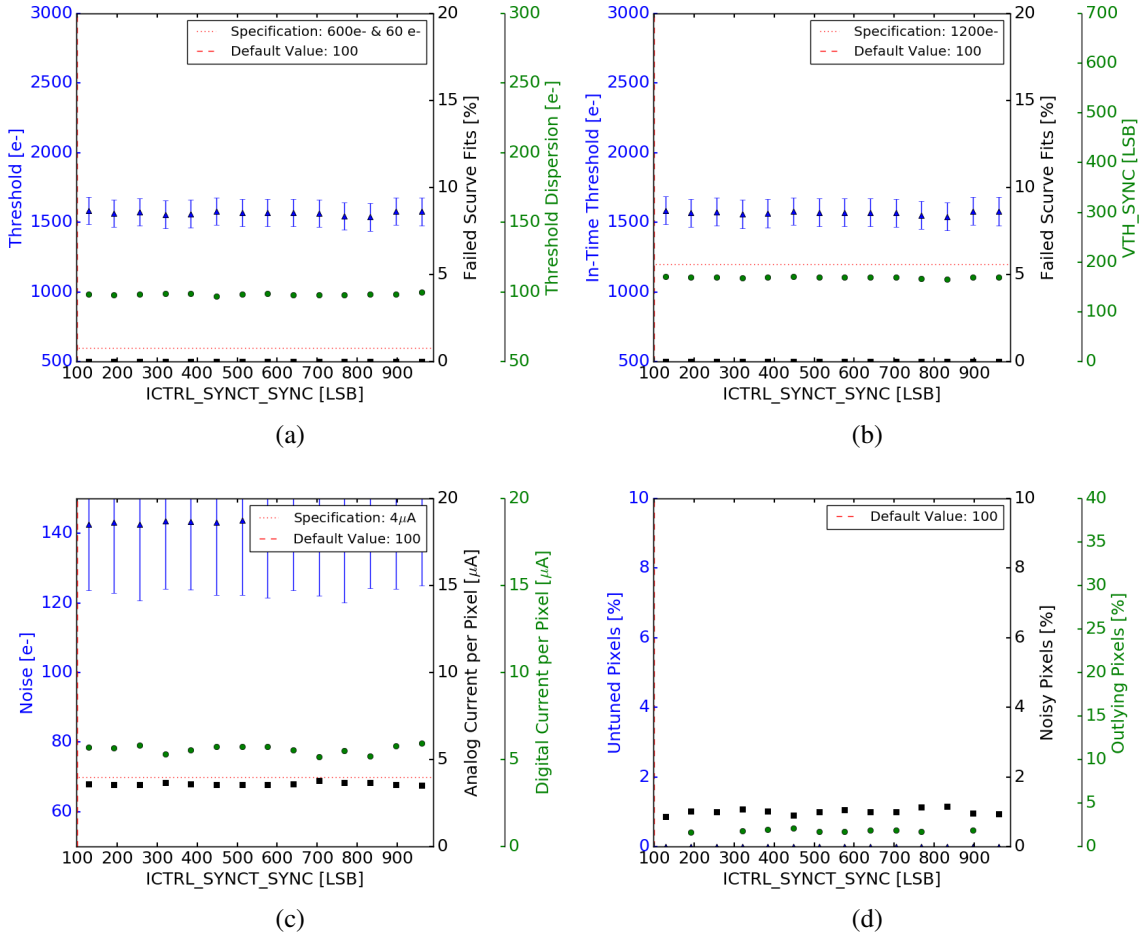


Figure A.5: Overview of the Synchronous Front End performance depending on oscillator delay line bias current ICTRL_SYNCT_SYNC.

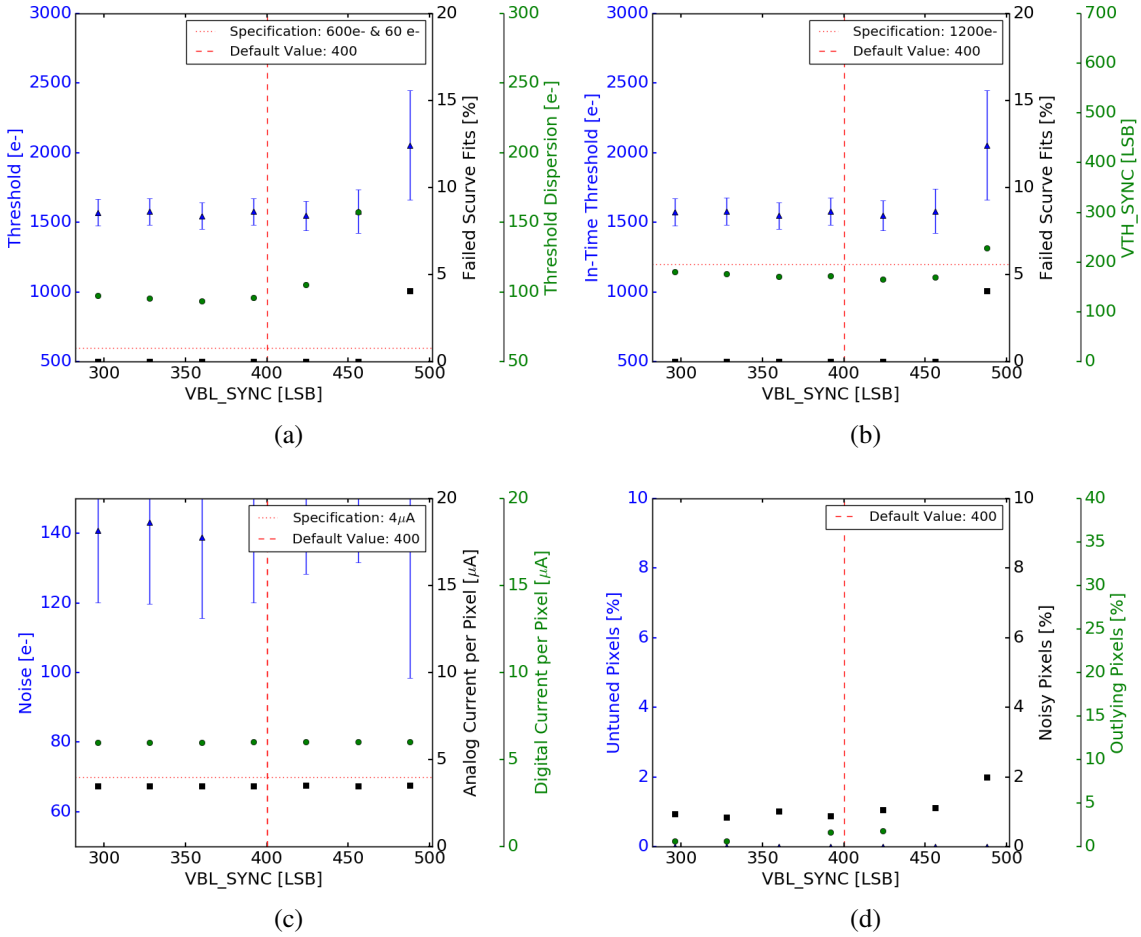


Figure A.6: Overview of the Synchronous Front End performance depending on baseline voltage for offset components VBL_SYNC.

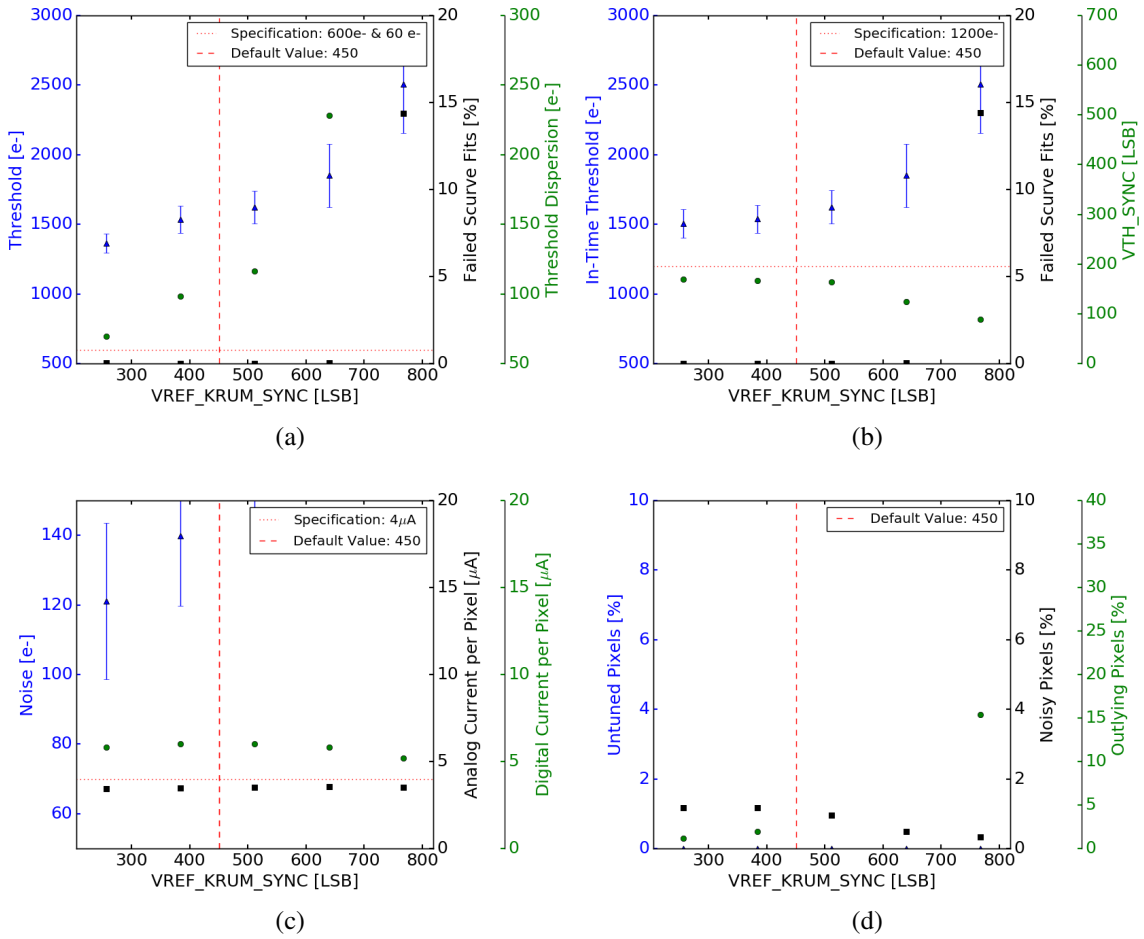


Figure A.7: Overview of the Synchronous Front End performance depending on Krummenacher voltage reference VREF_KRUM_SYNC.

A.4 Linear Front End Register Measurements

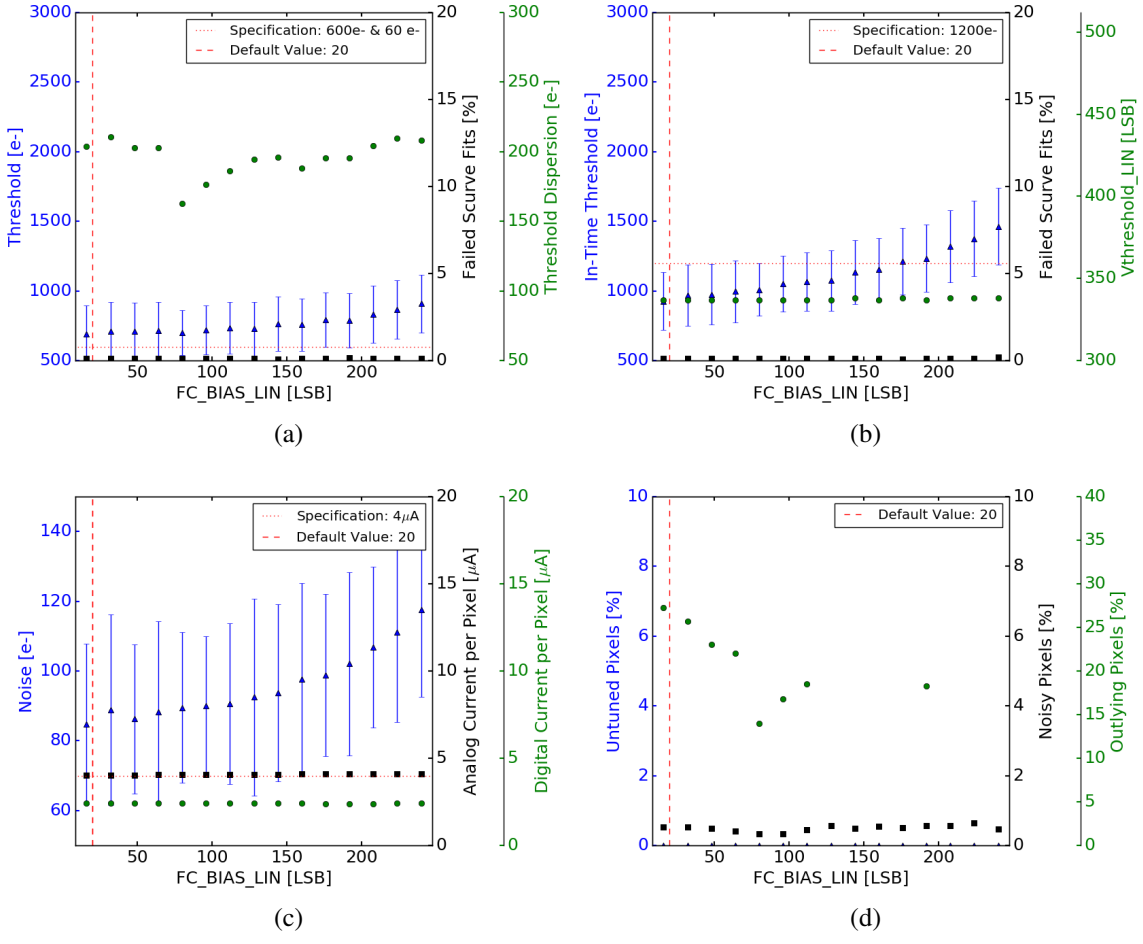


Figure A.8: Overview of the Linear Front End performance depending on folded cascode branch current inside CSA FC_BIAS_LIN.

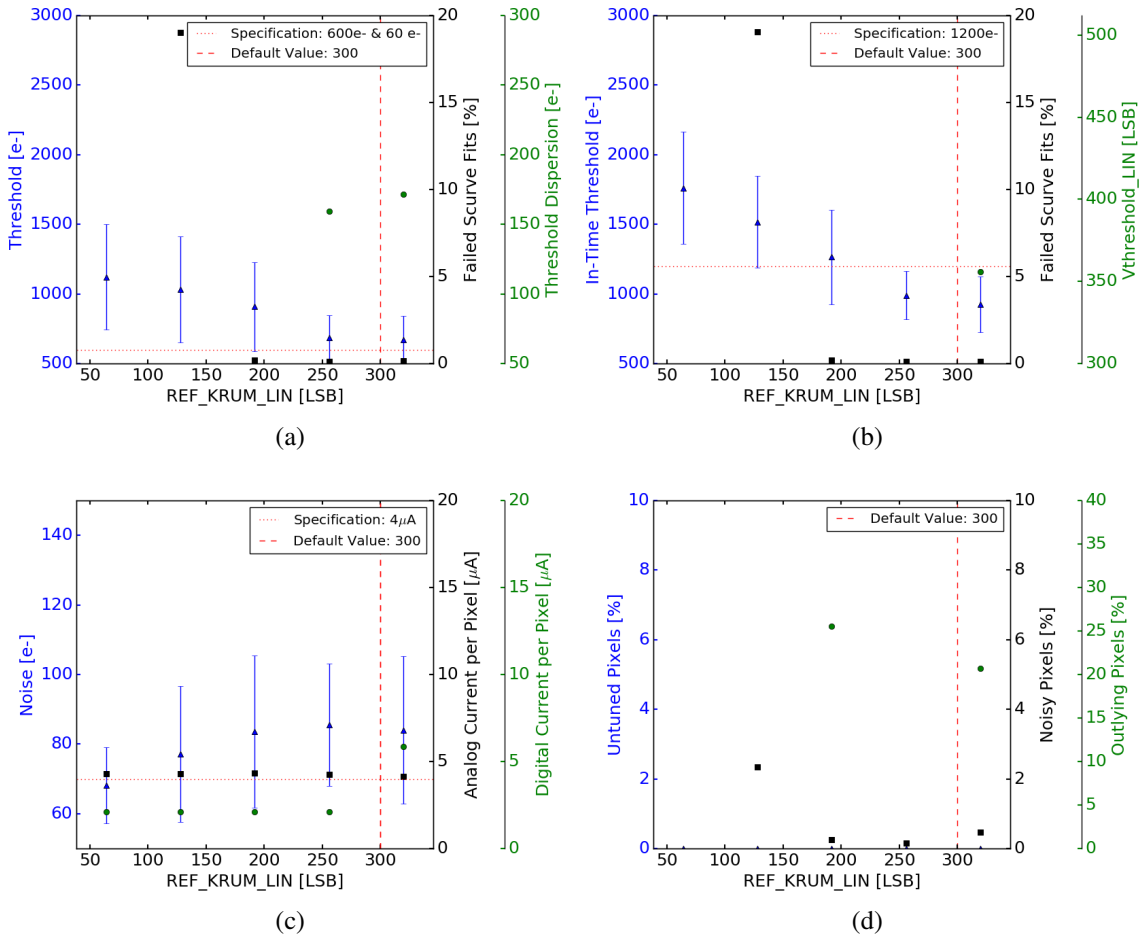


Figure A.9: Overview of the Linear Front End performance depending on Krummenacher voltage reference REF_KRUM_LIN.

A.5 Differential Front End Register Measurements

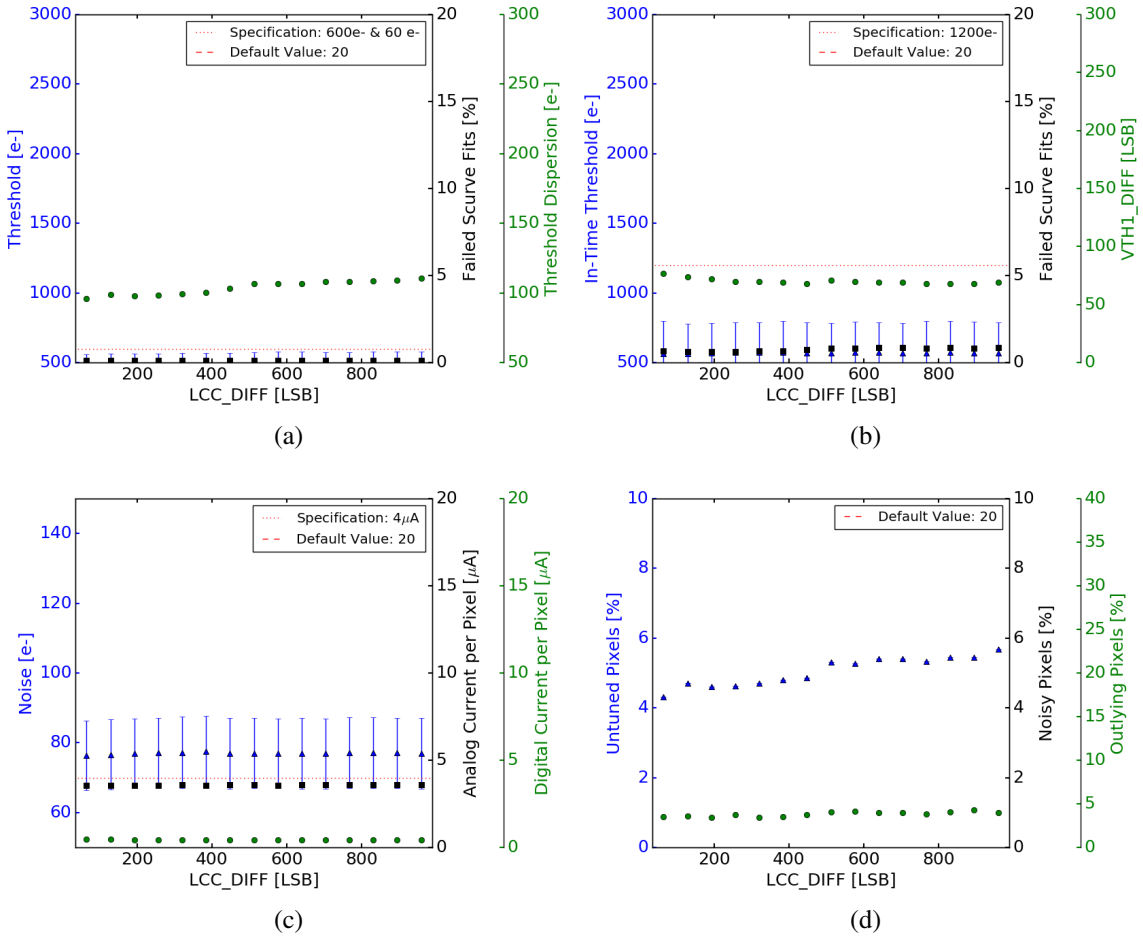


Figure A.10: Overview of the Differential Front End performance depending on leakage current compensation current LCC_DIFF.

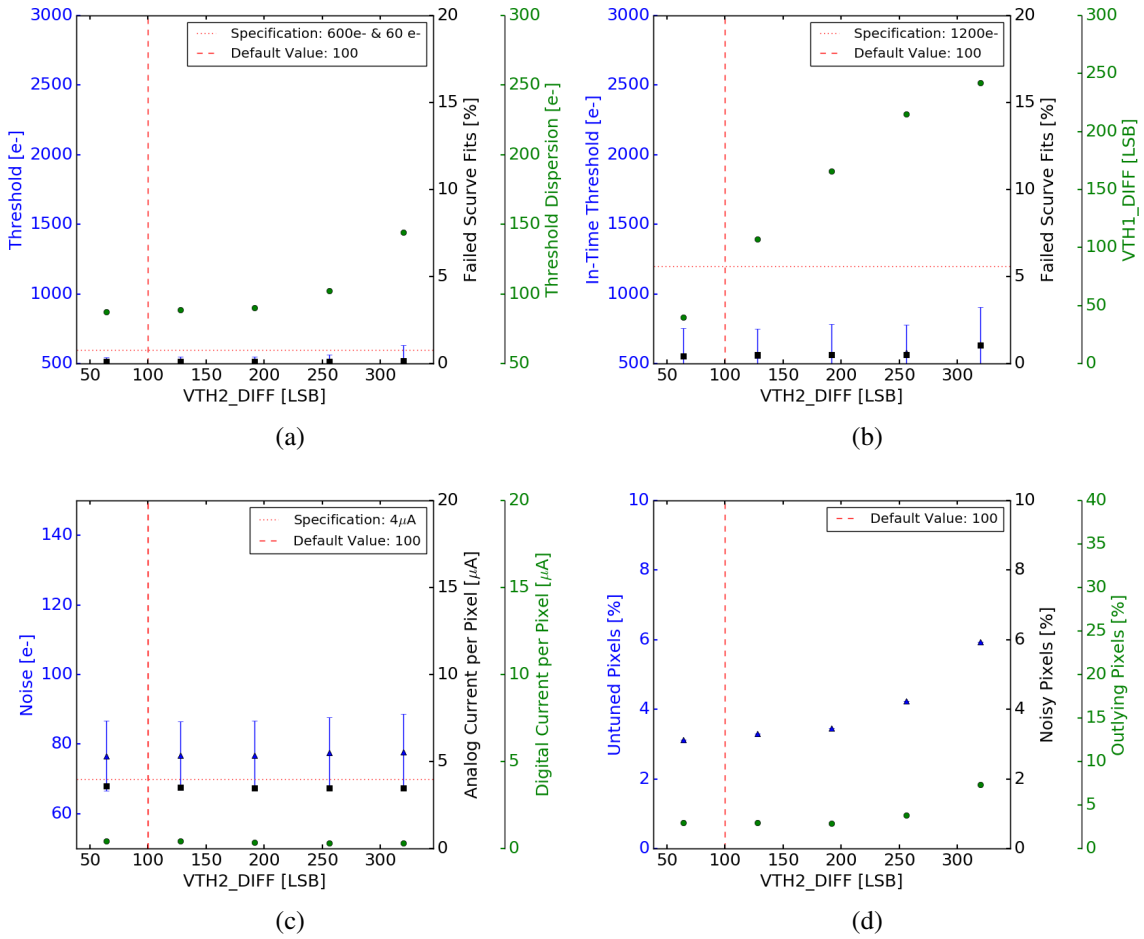


Figure A.11: Overview of the Differential Front End performance depending on positive branch offset voltage VTH2_DIFF.

Bibliography

[1] *The HL-LHC project*, Checked on 21.02.2019, URL: http://hilumilhc.web.cern.ch/about/hl-lhc-project.

[2] *Computer generated image of the whole ATLAS detector*, Checked on: 21.02.2019, URL: http://cds.cern.ch/record/1095924.

[3] *The ATLAS Experiment at the CERN Large Hadron Collider*, Checked on: 21.02.2019, URL: http://iopscience.iop.org/article/10.1088/1748-0221/3/08/S08003/meta#citations.

[4] H. Kolanoski and N. Wermes, *Teilchendetektoren: Grundlagen und Anwendungen*, Springer Spektrum, 2016, URL: https://cds.cern.ch/record/2134031.

[5] J. Janssen and F. Lütticke, *Versuch 520: Halbleiterdetektoren*, Lastupdated: February 20th 2018.

[6] *The Phase-II ATLAS ITk pixel upgrade*, Checked on: 21.02.2019, URL: http://iopscience.iop.org/article/10.1088/1748-0221/12/07/C07023/meta.

[7] *ATLAS page for the Pixel TDR plots approved by LHCC in April 2018*, Checked on: 21.02.2019, URL: https://atlas.web.cern.ch/Atlas/GROUPS/PHYSICS/PLOTS/ITK-2018-001/.

[8] *RD53 Website*, Checked on: 21.02.2019, URL: https://rd53.web.cern.ch/RD53/.

[9] M. Garcia-Sciveres, *RD53A Integrated Circuit Specifications*, tech. rep. CERN-RD53-PUB-15-001, CERN, 2015, URL: https://cds.cern.ch/record/2113263.

[10] M. Garcia-Sciveres, *The RD53A Integrated Circuit*, tech. rep. CERN-RD53-PUB-17-001, CERN, 2017, URL: https://cds.cern.ch/record/2287593.

[11] *RD53A Temperature measurements preliminary*, Checked on 21.02.2019, URL: https://indico.cern.ch/event/708552/contributions/2982835/attachments/1639045/2616263/2018_24april_TEMPSENS.pdf.

[12] F. Krummenacher, *Pixel detectors with local intelligence: an IC designer point of view*, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment **305** (1991) 527–532, ISSN: 0168-9002, URL: http://www.sciencedirect.com/science/article/pii/016890029190152G.

[13] E. Monteil, *SYNC FE – TESTING SPECIFICATIONS*, Checked on: 21.02.2019, URL: https://twiki.cern.ch/twiki/pub/RD53/RD53ATesting/SYNC_FE__TESTING_SPECIFICATIONS.pdf.

[14] L. Gaioni, *Linear Analog Front-end Guidelines and Recommendations*, Checked on: 21.02.2019, URL: https://twiki.cern.ch/twiki/pub/RD53/RD53ATesting/LIN_AFE_guidelines.pdf.

[15] M. Standke, *Guide to the RD53A - Differential Front End*, Checked on: 21.02.2019, URL: https://twiki.cern.ch/twiki/pub/RD53/RD53ATesting/Diff_userguide.pdf.

[16] *AD5541A Datasheet*, Checked on 21.02.2019, URL: https://www.analog.com/media/en/technical-documentation/data-sheets/AD5541A.pdf.

[17] W. M. C. Sansen, *Analog Design Essentials (The International Series in Engineering and Computer Science)*, Springer-Verlag, 2006, ISBN: 0387257462.

[18] *Linearity RD53A ADC*, Checked on 21.02.2019, URL: https://gitlab.cern.ch/RD53-Testing/RD53A/issues/40.

[19] *DNL RD53A ADC*, Checked on 21.02.2019, URL: https://gitlab.cern.ch/RD53-Testing/RD53A/issues/41.

[20] *INL RD53A ADC*, Checked on 21.02.2019, URL: https://gitlab.cern.ch/RD53-Testing/RD53A/issues/42.

[21] *NTC Thermistor Beta*, Checked on: 21.02.2019, URL: https://www.ametherm.com/thermistor/ntc-thermistor-beta.

[22] M. E. Lauritzen, *RD53A Injection Capacitance Measurement*, Checked on: 21.02.2019, URL: https://twiki.cern.ch/twiki/pub/RD53/RD53APublicPlots/0x072A_Cap_Measurement.pdf.

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